



Data Sheet

ATBM6022

Single-chip IEEE 802.11b/g/n 1T1R Wireless
Network Controller with USB Interface

WRITTEN	CHECKED	APPROVED
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**REVISION HISTORY**

Revision Number	Revision Date	Changes	
		Item	Description
V1.0	2018-01-15		Official release version

FCC warning**Compliance Information:**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: 1. This device may not cause harmful interference, 2. This device must accept any interference received, including interference that may cause undesired operation. Any changes or modifications to this device not expressly approved by Altobeam(China) Inc. For compliance could void the user's authority to operate the equipment.

Note:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced technician for help.

If the module's FCC ID is not visible when installed in the host, or if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: “Contains Transmitter Module FCC ID: 2AOXX-ATBM602X” or “Contains FCC ID: 2AOXX-ATBM602X” must be used.

SIMPLIFIED EU DECLARATION OF CONFORMITY

This product can be used across EU member states.

Hereby, we Altobeam(China) Inc. Declare that the device is in compliance with Directive 2014/53/EU.

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1 Overview

1.1 General description

ATBM6022 is a highly integrated 802.11/b/g/n WLAN SOC with USB interface (USB 1.0/1.1/2.0 compliant). The ATBM6022 provides a complete solution for wireless LAN application with remarkable performance and reliability.

ATBM6022 supports all data rates of IEEE 802.11b, 802.11g, and 802.11n. Features includes one spatial stream transmission, short guard interval (400ns GI), and transmission over 20MHz and 40MHz bandwidth.

ATBM6022 WLAN MAC supports 802.11e for multimedia applications, 802.11i security, and 802.11n for enhanced MAC protocol efficiency. Frame aggregation techniques such as A-MPDU are also supported for improving throughput performance. Power saving mechanisms such as Legacy Power Save, and U-APSD are implemented to reduce power consumption.

ATBM6022 is fully compatible with WiFi- Alliance, WMM, WPS and P2P specifications.

FCC Radio Frequency Exposure distance statement Important Note: To comply with the FCC RF exposure compliance requirements, no change to the antenna or the device is permitted. Any change to the antenna or the device could result in the device exceeding the RF exposure requirements and void user's authority to operate the device. Caution: Exposure to Radio Frequency Radiation. To comply with FCC/IC RF exposure compliance requirements, a separation distance of at least 20 cm must be maintained between the antenna of this device and all persons.

Product Size: 13.0mm (L) *12.2mm (W)* 1.5mm (H).(Tolerance=0.2mm)

1.2 Block diagram

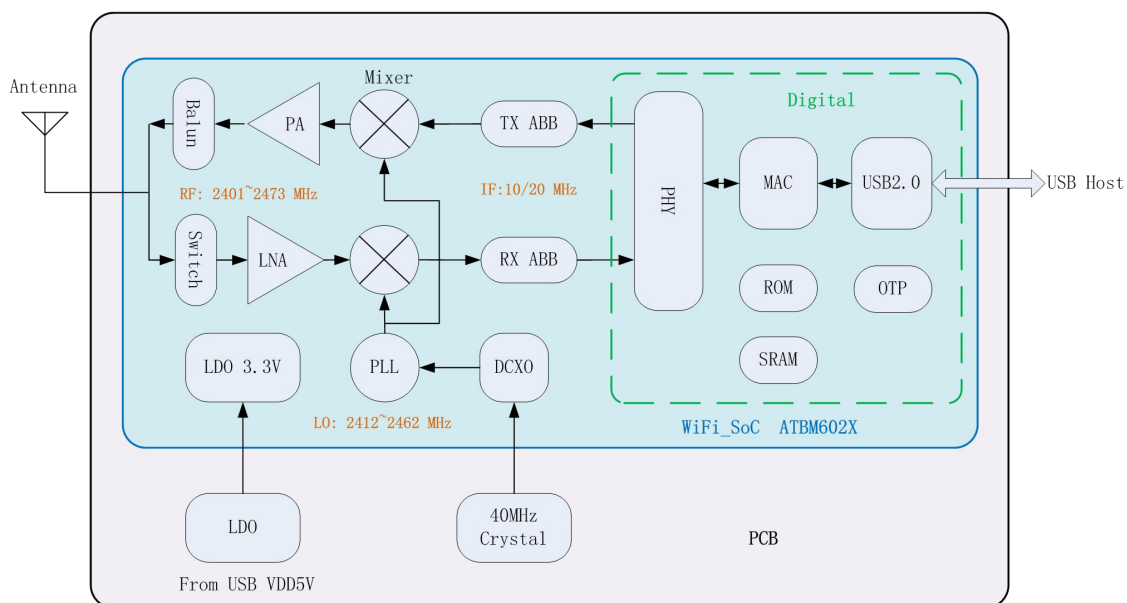


Figure 1 ATBM6022 Block diagram

1.3 ATBM6022 feature list

- ATBM6022 includes Wi-Fi protocol accelerator, USB device interface, peripheral interface and Power-Management Subsystem
- WLAN MAC, a 1T1R capable WLAN baseband, and WLAN RF in a single chip
- Integrated PA, LNA, Balun and T/R switch to maximum reduce BOM cost
- Integrated LDO on chip to simplify power source and reduce BOM cost, only 3.3V power is needed
- Support STA and AP function
- Support BSS, P2P and Miracast function
- Compatible with 802.11 b/g/e/i/n/w specifications
- Compatible with 802.11n Legacy mode, mix mode and green field mode
- Support A-MPDU transmit and receive for throughput improvement
- Support A-MSDU reception
- Support STBC stream reception
- Support Short-GI of 802.11n
- Supports both 20MHz and 40MHz bandwidth transmission
- PS-Poll and U-APSD Power Save mechanism at BSS
- Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for radio frequency front-end
- Hardware Crypto Engine for Advanced Fast Security, Including WEP, TKIP, AES and 802.11w
- USB device interface speed up to 480Mbps (USB1.0/1.1/2.0 compliant)
- 32bit CPU core speed up to 160MHz
- I2C master/slave, UART, SPI master, PWM and GPIO interface
- Support 40.0MHz crystal with internal oscillator
- 32.768kHz on-chip crystal
- 5x5mm², 32pin QFN package

2 Pin Information

2.1 Pin map

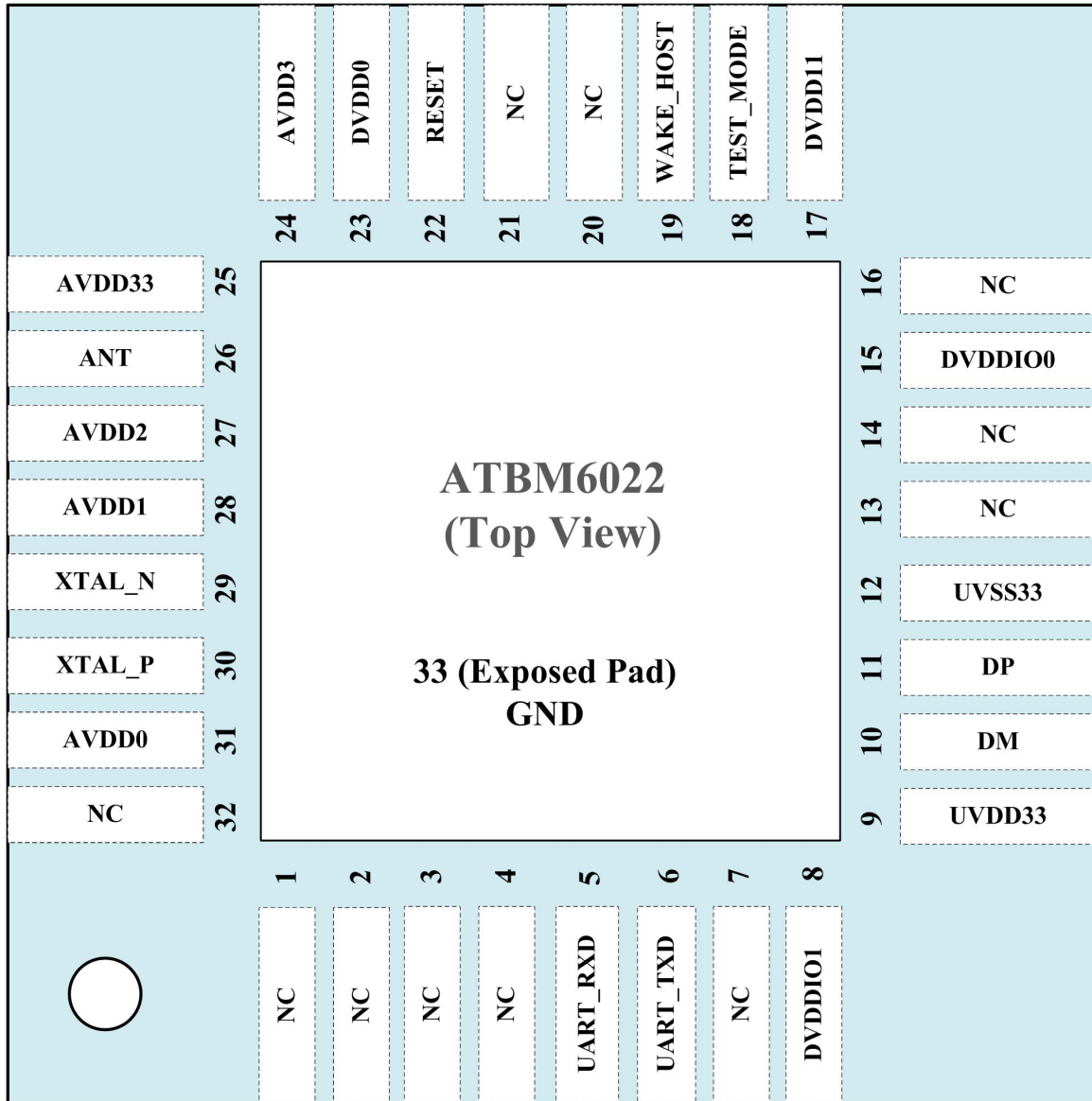


Figure 2 ATBM6022 pin map (Top View)

2.2 Pin table

Pin Number	Pin Name	Number of Pin(s)	Type	Pin Description
USB interface				
10	DM	1	I/O	USB transceiver differential signal
11	DP	1	I/O	USB transceiver differential signal
Power supply				
8	DVDDIO1	1	PWR	VDD 3.3V/1.8V for digital IO
9	UVDD33	1	PWR	VDD 3.3V for USB transceiver
15	DVDDIO0	1	PWR	VDD 3.3V/1.8V for digital IO
17	DVDD11	1	PWR	VDD1.1V for digital core. It is only connected with decouple capacitance. Digital core power is supplied by LDO on chip to reduce power source for BOM cost reduction.
23	DVDD0	1	PWR	VDD 3.3V/1.8V for LDO power for digital core. This LDO generates 1.1V core power from 3.3V or 1.8V power.
24	AVDD3	1	PWR	VDD 3.3V/1.8V for analog circuit
25	AVDD33	1	PWR	VDD 3.3V for analog. It must be 3.3V only.
27	AVDD2	1	PWR	VDD 3.3V/1.8V for analog circuit
28	AVDD1	1	PWR	VDD 3.3V/1.8V for analog circuit
31	AVDD0	1	PWR	VDD 3.3V/1.8V for analog circuit
GPIO				
19	WAKE_HOST	1	I/O	ATBM6022 wake up host output pin/GPIO2
6	UART_TXD	1	I/O	UART Tx data output pin/GPIO1
5	UART_RXD	1	I/O	UART Rx data input pin/GPIO3
Reset				
22	RESET	1	Input	Hardware reset pin, low active
Test Mode				
18	TEST_MODE	1	Input	Test mode selection, left it floating in normal mode.
Clock				
29	XTAL_N	1	Input	40MHz Crystal input
30	XTAL_P	1	Output	40MHz Crystal output
Antenna Interface				
26	ANT	1	I/O	2.4GHz radio signal input/output from/to antenna
GND				
12	UVSS33	1	GND	Ground for USB transceiver
33 (Exposed Pad)	GND	1	GND	Ground for digital power supplies

Pin Number	Pin Name	Number of Pin(s)	Type	Pin Description
Others				
1	NC	11	Output	These pins are used for test mode, left them floating in normal mode.
2	NC		Output	
3	NC		Output	
4	NC		Output	
7	NC		Output	
13	NC		Output	
14	NC		Output	
16	NC		Output	
20	NC		Output	
21	NC		Output	
32	NC		Output	

3 Electrical Characteristics

3.1 Absolute maximum rating

Parameter	Description	Min	Max	Unit
AVDD33/UVDD33	Digital and analog 3.3V power supplies voltage	-0.3	5.0	V
DVDDIO0/1 DVDD0 AVDD0/1/2/3	Digital and analog 3.3V or 1.8V power supplies voltage	-0.3	5.0	V
T _{stg}	Storage temperature	-60	150	°C
T _j	Junction temperature		125	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded.

3.2 Thermal data

Parameter	Description	Value	Unit
T _{oper}	Operating ambient temperature range	-40 ~ +85	°C
R _{thjc}	Junction-case thermal resistance	15.6	°C/W
R _{thja}	Junction-ambient thermal resistance	30.9	°C/W

3.3 DC electrical characteristics

Parameter	Description	Min	Typical	Max	Unit
UVDD33	USB transceiver operating voltage	2.97	3.3	3.63	V
AVDD33	Analog module 3.3V operating voltage	2.97	3.3	3.63	V
DVDDIO0/1	Digital module 3.3V operation voltage	2.97	3.3	3.63	V
DVDD0	Digital module 1.8V operating voltage	1.62	1.8	1.98	V
AVDD0/1/2/3	Analog module 3.3V operating voltage	2.97	3.3	3.63	V
	Analog module 1.8V operating voltage	1.62	1.8	1.98	V
V _{IL}	Low level input voltage (I, I/O)	-0.3		0.8	V
V _{IH}	High level input voltage (I, I/O)	2.0		3.6	V
V _{T+}	Schmitt trig Low to High threshold (I, I/O)	1.54	1.65	1.74	V
V _{T-}	Schmitt trig High to Low threshold (I, I/O)	0.95	1.02	1.09	V
V _{OL}	Low level output voltage (O, I/O)			0.4	V
V _{OH}	High level output voltage (O, I/O)	2.4			V
I _{GPO}	GPOs, STATUS			4	mA

Note: Exposure beyond recommended operating conditions may affect device reliability.

3.4 Requirements to peripheral circuits

3.4.1 Power supply modules

Type	Module	Parameter	Requirement	Unit
3.3V only power supply	3.3V power module	Rated voltage	3.3	V
		Voltage tolerance	≤10	%
		Rated current	≥500	mA
		Ripple	<120	mV
3.3V and 1.8V power supply	3.3V power module	Rated voltage	3.3	V
		Voltage tolerance	≤10	%
		Rated current	≥300	mA
		Ripple	<120	mV
	1.8V power module	Rated voltage	1.8	V
		Voltage tolerance	≤10	%
		Rated current	≥200	mA
		Ripple	<120	mV

3.4.2 External crystal and peripheral circuit

If a 40MHz external crystal is used, the required specification of the crystal should be as below:

Parameter	Description	Min	Typical	Max	Unit
Frequency	Nominal frequency		40.0000		MHz
Tolerance	Frequency measured at 25°C±3°C		±50	±80	ppm
ESR	Equivalent series resistance			40	Ω
C _{Load}	Load capacitance	8		16	pF
C _{Shunt}	Shunt capacitance		5		pF
DL	Drive level		120		μW
Aging	Aging per year in 10 years		±5		ppm
Temp Drift	Drift of frequency over the operating temperature range		±50	±80	ppm

4 Interface timing specification

4.1 USB attach and HS handshake behaviors

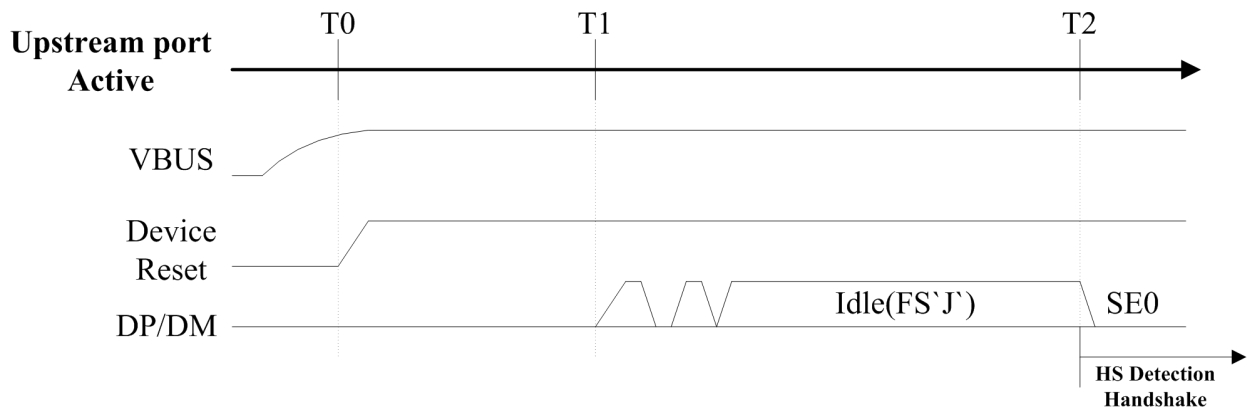


Figure 3 USB Attach Behavior

USB attach and reset timing values are shown as below.

Timing Parameter	Description	Value
T0	VBUS valid	0(Reference)
T1	Maximum time from the VBUS valid(>4.01V) to when the device signals the attachment.	$T0 + 100ms\{T_{sigatt}\} > T1$
T2(HS Reset T0)	De-bounce interval The device enters the HS detection handshake protocol	$T1 + 100ms\{T_{attdb}\} < T2$

4.2 HS handshake detection

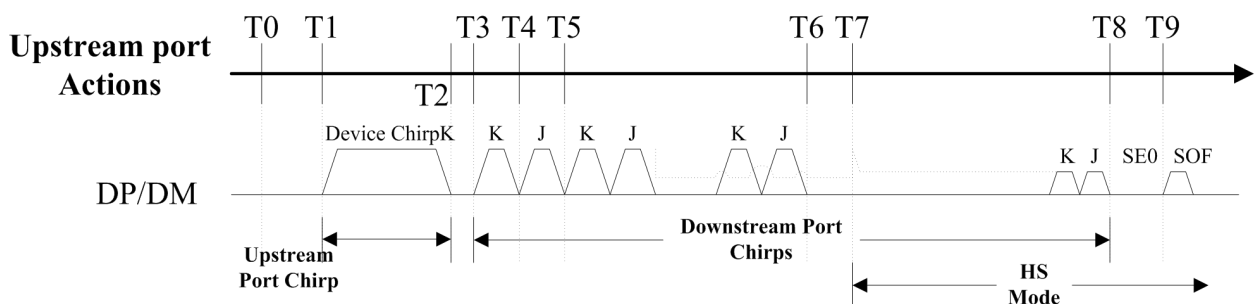


Figure 4 HS detection handshake timing behavior

Reset timing values are shown as below.

Timing Parameter	Description	Value
T0	HS handshake begins. D+ pull-up is enabled; HS termination is disabled.	0(Reference)
T1	Device asserts Chirp-K on the bus.	$T0 < T1 < HS\ Reset\ T0 + 6ms\ \{T_{uchend-Tuch}\}$

T2	Device removes Chirp-K from the bus. Minimum width:1.0ms	$T0+1.0ms\{Tuch\}<T2<HS$ Reset $T0+7.0ms\{Tuchend\}$
T3	The downstream port asserts Chirp-K on the bus.	$T2<T3<T2+100us\{Twdch\}$
T4	The downstream port toggles Chirp-K to Chirp-J on the bus.	$T3+40us\{Tdchbit(Min.)\}<T4<$ $T3+60us\{Tdchbit(Max.)\}$
T5	The downstream port toggles Chirp-J to Chirp-K on the bus.	$T4+40us\{Tdchbit(Min.)\}<T5<$ $T6+60us\{Tdchbit(Max.)\}$
T6	Device detects the downstream port chirp.	T6
T7	Downstream port chirp detected by the device Device removes D+ pull-up, asserts HS terminations, reverts to the HS default state, and waits for the end of a reset.	$T6<T7<T6+500us\{T\{wth\}\}$
T8	Terminate downstream port Chirp K-J sequence (Repeating T4 and T5)	$T9-500us\{Tdchse0(Max.)\}<T8$ $<T9-100us\{Tdchse0(Min.)\}$
T9	The earliest time that the downstream port may end the reset; and the latest time at which the device may remove the D+ pull-up, assert the HS terminations, and revert to the HS default state.	HS resets $T0+10ms\{Tdrst(Min.)\}$

5 Mechanical Data

5.1 Chip package drawing

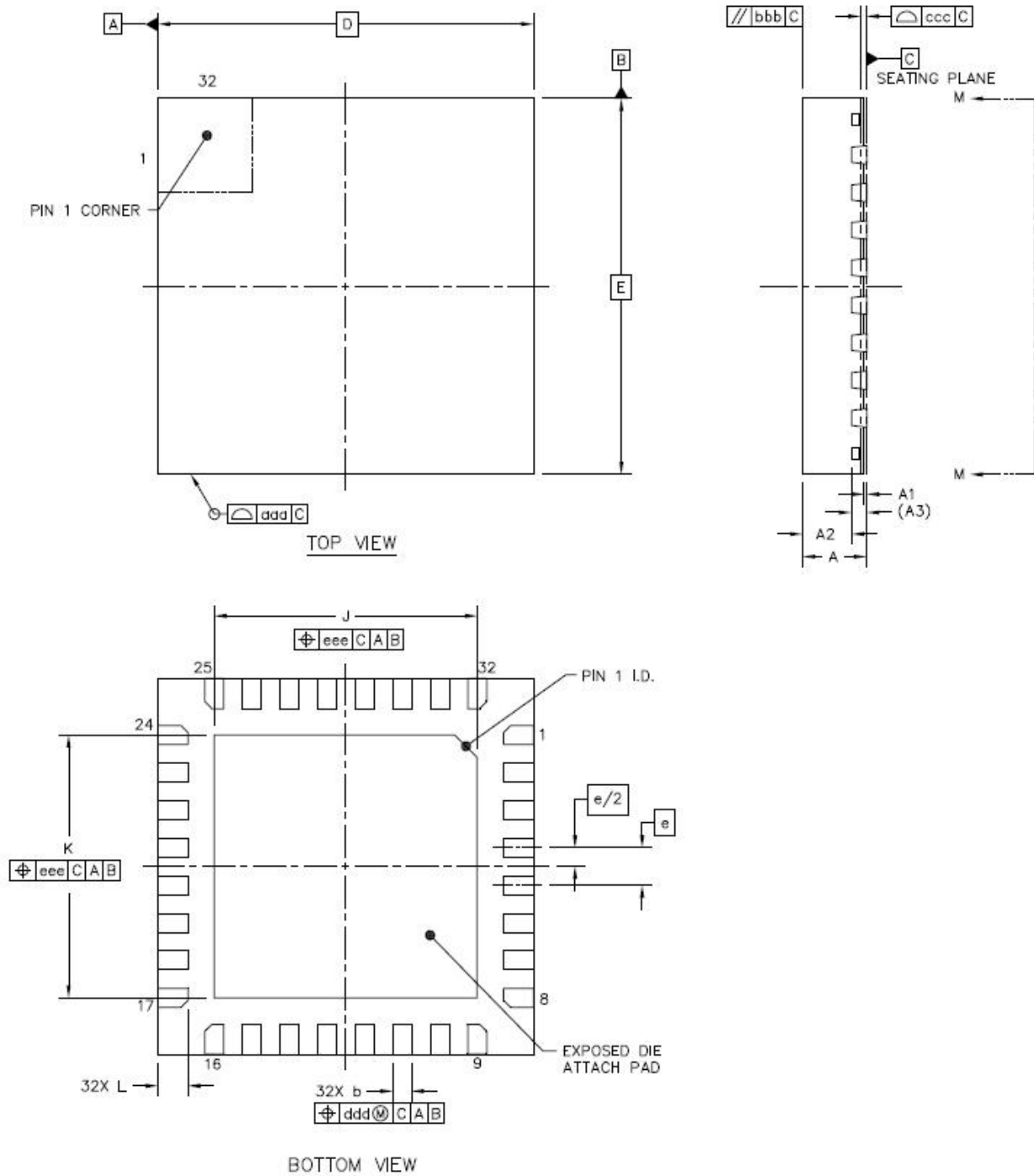


Figure 5 ATBM6022 package drawing

5.2 Dimensions of packaging parameters (unit: mm)

		SYMBOL	MIM	NOM	MAX
TOTAL THICKNESS		A	0.7	0.8	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		B	0.2	0.25	0.3
BODY SIZE	X	D	5 BSC		
	Y	E	5 BSC		
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	J	3.3	3.45	3.6
	Y	K	3.3	3.45	3.6
LEDA LENGTH		L	0.3	0.4	0.5
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSE PAD OFFSET		eee	0.1		

1. RF layout guidelines

This section provides required guidelines for PCB designs incorporating the ATBM602X module. The ATBM602X module is certified with a PCB edge SMA connector and antenna match tuning network as shown in Figure 1 and 2. The antenna match tuning network is composed of C5, C6 and L1, as shown in Figure 3.

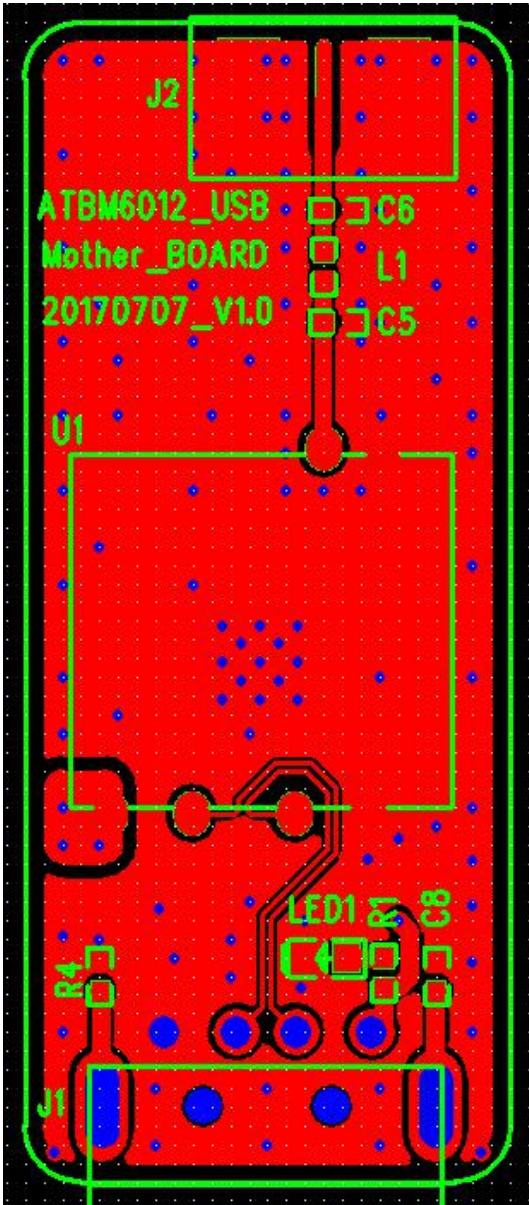


Figure 1: Top Layer

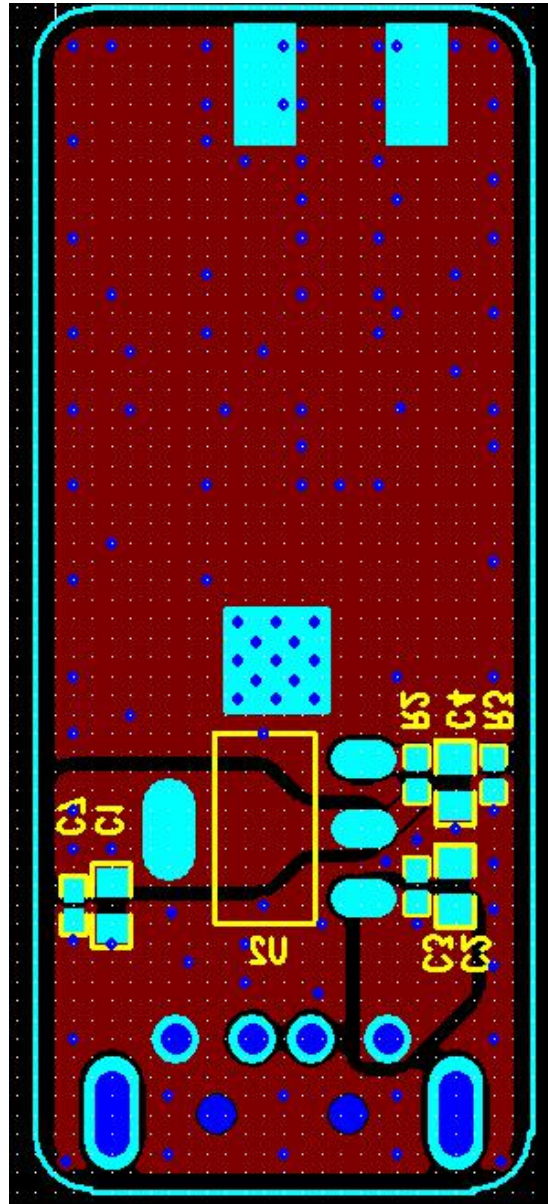


Figure 2: Bottom Layer

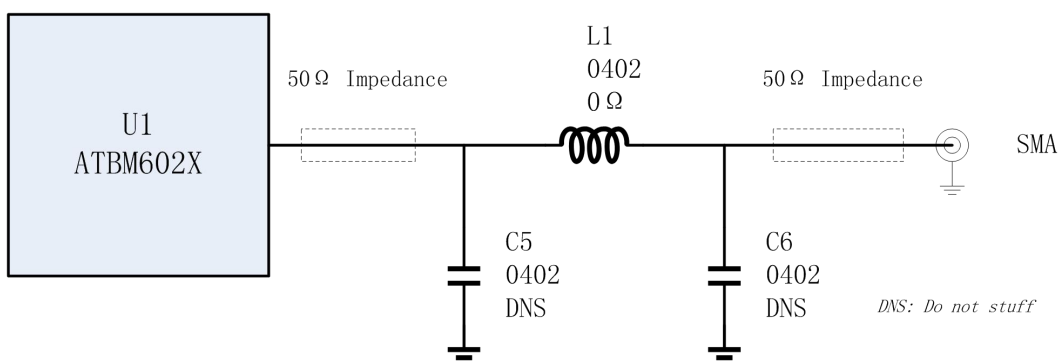


Figure 3: Antenna match tuning network schematic

Figure 4 shows the entire RF trace and SMA layout. The RF trace must be a 50 Ω impedance controlled transmission line which is referenced to a solid, unbroken ground. The trace width and distance to the ground plane must be adjusted to achieve the target impedance. The trace must be shielded by applying stitching vias along the edge of the ground pour on both sides of the RF trace.

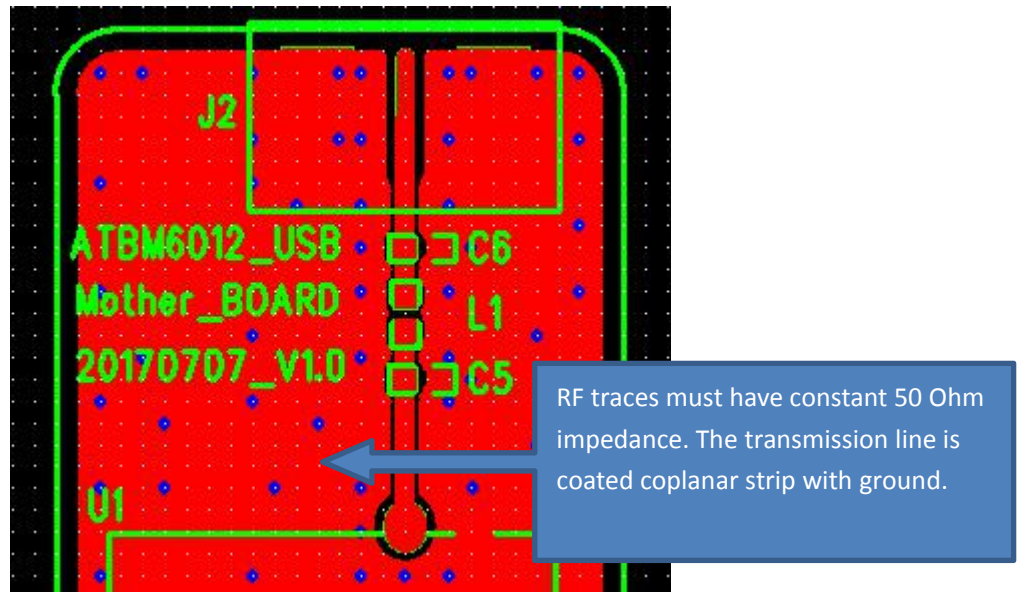


Figure 4: RF trace from module to antenna

Figure 5 shows the required PCB layer stack information and 50 Ω transmission line dimension. This layer stack up must be matched precisely including material type, dielectric constant, dielectric thickness, and copper thickness. The trace dimensions that must be followed precisely, including trace width, and routing

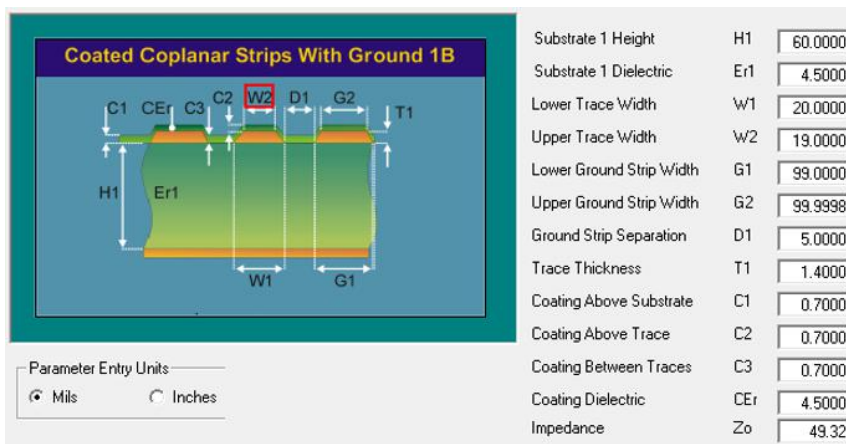


Figure 5: ATBM602X PCB layer stack (Dielectric material: FR-4)

2. Approved Antenna

The antenna in Table 1 is tested and approved for use with the ATBM602X Module. According to the FCC Permissive Change Policy (178919 D01)

Additional antennas that are equivalent may be substituted, and then marketed without a Class II permissive change... Equivalent antennas must be of the same type (e.g., yagi, dish, etc.), must be of equal or less gain than an antenna previously authorized under the same grant of certification (FCC ID), and must have similar in-band and out-of-band characteristics (consult specification sheet for cutoff frequencies).

Table1 : ATBM602X Module Approved Antenna

Part Number	Type	Gain	Impedance
-------------	------	------	-----------

ZWex-17	Dipolar	2.0dBi	50Ω
---------	---------	--------	-----

3. Test procedure for design verification

After the design is fabricated the following measurements should be executed to verify the design:

- a. Mechanical measurement of dimensions specified in the transmission line dimensions diagrams above
- b. Obtain and review the detailed layer stack up solution used for the build from the PCB manufacturer that specifies dielectric thicknesses and target dielectric constants for substrate materials.

AltoBeam Applications Engineers are available to review Layout designs to ensure compliance and optimal RF performance.

4. Production test procedures for ensuring compliance

During production test for the host device, The ATBM602X module is to be activated in maximum power transmit mode and the conducted RF output power at the SMA connector is to be measured using a Spectrum Analyzer, RF Power Meter or other appropriate RF measurement equipment. The conducted output power should not exceed the output power specified in the ATBM602X Data Guide. If a conducted output power test is not possible on the host device, an equivalent radiated output power test may be used.