AMN11100

WHDI™ Transmitter Module Datasheet

Version 1.0

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Revision History

Version	Date	Description
0.1	-	Initial Release
0.5	19-Jun-07	Added Design Guidelines Updated Reset Mechanism Updated Two-Wire Serial Bus Protocol Definition
0.6	19-June-07	Added Mechanical Dimensions
1.0	06-Nov-07	Added FCC certification and compliance Added Table 2 Updated Table 4

Chapter 1

Introduction

The AMN11100 is the first generation of WHDI™ transmitter board based on AMIMON's AMN2110 baseband transmitter chip. The AMN11100 WHDI™ wireless transmitter module, together with the AMN12100 wireless receiver module, presents the ultimate solution for converting any High Definition (HD) system into a wireless one. This add-on module enables wireless A/V applications that easily fit into the living room and eliminate traditional A/V wiring. The ultimate HD video and audio quality and robustness are unmatched by any other wireless technology, and present a true alternative to cable. The WHDI system transmits *uncompressed* video and audio streams wirelessly and thus simplifies and eliminates system issues experienced with any other known wireless-based solutions, such as lip-sync, large buffers and other burdens like retransmissions or error propagation.

1.1 Features

- **Uncompressed and uncompromised HD video quality, using AMIMON's baseband chipsets:**
  - AMN2110: WHDI™ Baseband Transmitter
- **WHDI – Wireless High Definition Interface:**
  - Digital video: 30-bit RGB or YCrCb
  - Digital audio: I2S and SPDIF
  - Two-Wire serial bus slave interface
  - Two interrupt lines
- **Supports any uncompressed video resolutions, including:**
  - HD: 720p, 1080i, 1080p, 576i, 576p, 480p, 480i
  - PC: VGA (640x480), SVGA (800x600), XGA (1024x768)
  - Panel: 854x800, 1280x768, 1366x768
- **Audio:**
  - Up to 3Mbps audio stream:
    - I2S: Two PCM channels (sampled up to 48 KHz x 24 bit)
    - SPDIF: Including AC-3, DTS
- **Strong 256-bit AES encryption**
- **User-defined two-way channel with minimum 10 Kbps for data and control**
- **Less than 1mSec latency between source and sink**
- **Small mechanical footprint:**
  - With PCB integrated antennas.
  - Optional external antennas

- **RF characteristics:**
  - MIMO technology, using 5GHz unlicensed band, 18MHz bandwidth.
  - Coexists with 802.11a/n and 5.8GHz cordless devices.
  - Support for Automatic Transmission Power Control (ATPC).
  - No line of sight needed between transmitter and receiver. It has a range of over 30 meters, suitable for almost any room.
  - 14mW typical transmission power.
  - Maximum 45mW transmission power.
- **Power requirements:**
  - 3.3V (±5%), ~5.6W
- **Certification & Compliance:**
  - This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
  - Any changes or modifications not expressly approved by Amimon for compliance could void the user's authority to operate the equipment.
  - This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
    - Reorient or relocate the receiving antenna.
    - Increase the separation between the equipment and receiver.
    - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
    - Consult the dealer or an experienced radio/TV technician for help.
- **Caution:** The module should be positioned so that personnel in the area for prolonged periods may safely remain at least 20 cm (8 in) in an uncontrolled environment from the module. Observe FCC OET Bulletin 56 “Hazards of radio frequency and electromagnetic field” and Bulletin 65 “Human exposure to radio frequency electromagnetic fields.”

Chapter 2

Overview

The AMN11100 WHDI Video Source Unit (VSU) is designed to modulate and transmit downstream video and audio content over the wireless medium and receive a control channel over the wireless upstream. The modulation uses 18MHz bandwidth and is carried over the 5GHz unlicensed band. Figure 1 displays a block diagram of the AMN11100. The inputs to the VSU are digital uncompressed video, digital audio and control, all via the WHDI connector. It has a MIMO design of four wireless output channels and a slow rate data input wireless channel. The MiniMAC uC is responsible for the control and the management.

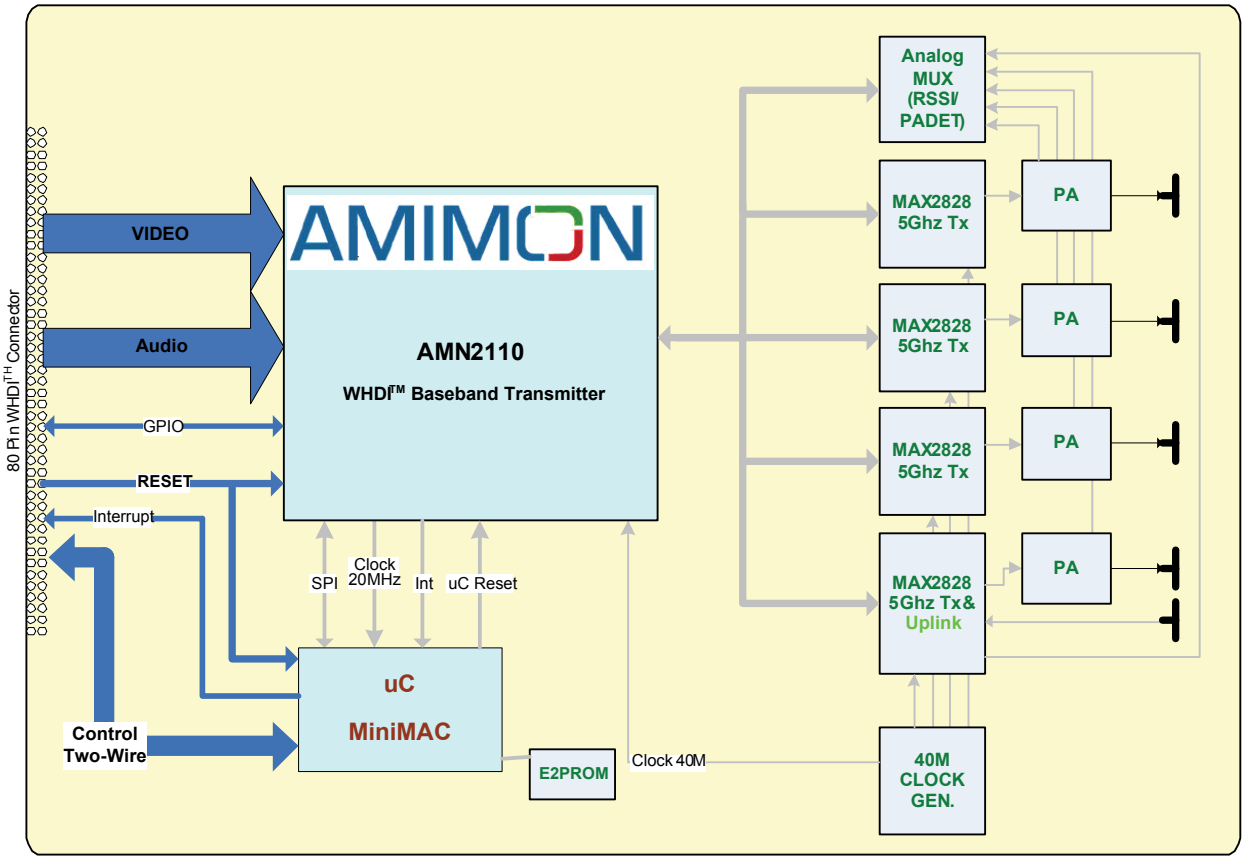


Figure 1: AMN11100 Block Diagram

The main building blocks of the AMN11100 are as follows:

- **AMN2110 WHDI Baseband Transmitter,** as briefly described on page 4
- **LPC2103 Mini-MAC µController,** as briefly described on page 4
- **MAX2828 5GHz (802.11a) Transceiver,** as briefly described on page 5
- **Power Amplifier (PA),** as briefly described on page 5
- **Board Connector (WHDI Connector),** as described on page 5
- **E2PROM,** as described on page 5
- **40MHz Clock Gen,** as described on page 5

2.1 AMN2110 WHDI Baseband Transmitter

The AMN2110 WHDI™ baseband transmitter chip is the *heart* of the AMN11100 WHDI transmitter module. The AMN2110 interfaces the A/V source through the WHDI connector, and is controlled on board by the MiniMAC uC.

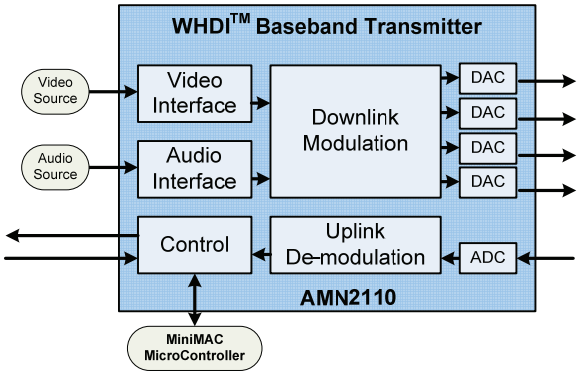


Figure 2: WHDI Baseband Transmitter Chipset

The AMN2110 is based on MIMO technology transmitting through up to four output channels. Four digital-to-analog converters and one analog-to-digital converter are embedded within the chip.

The AMN2110 internal PLL accepts an input clock frequency of 40MHz. The input frequency is multiplied and then used as an internal system clock.

2.2 LPC2103 Mini-MAC µController

The LPC2103 microcontroller is based on a 16-bit/32-bit ARM7TDMI-S CPU, with embedded 32kB high-speed memory. It is used as an external microcontroller for implementing the MAC layer of the WHDI link.

The LPC2103 internal PLL accepts an input clock frequency of 20MHz and generates an internal 60MHz system clock.

2.3 MAX2828 5GHz (802.11a) Transceiver

The VSU has four MAX2828 chips embedded in it. The MAX2828 is a single-chip, RF transceiver IC designed specifically for single-band 4.9GHz to 5.875GHz, OFDM, 802.11 WLAN applications. It includes all the circuitry necessary to implement the RF transceiver function, providing a fully integrated receive path, transmit path, VCO, frequency synthesizer and baseband/control interface. Only the PA, RF switches, RF bandpass filters (BPF), RF BALUNs and a small number of passive components are required to form the complete RF front-end solution.

AMIMON's WHDI™ technology uses the low cost and high availability of the 802.11a/n RF to allow low-cost RF for the video modem. Future generations of the WHDI modem will use an AMIMON-designed, cost-efficient, single-chip, integrated RFIC for multiple transmits on the transmitter side and a single-chip, integrated RFIC for multiple receivers on the receiver side.

2.4 Power Amplifier (PA)

In order to extend the operating range for the AMN11100, the RF transmitter uses power amplifiers. Each power amplifier has an output power detector for TPC purposes. Amimon has implemented Anadigics AWL6951 PA on the AMN11100.

2.5 Board Connector (WHDI™ Connector)

For information regarding the connector specification and pin-outs, see section 4.1, *AMN11100 Board Connector (WHDI Connector)*, page 15.

2.6 E2PROM

The E2PROM is currently a system option, enabling mating and authentication in a multipoint design environment.

2.7 40MHz Clock Gen

An on-board 40MHz TCXO is connected to the MAX2828 chipsets and the AMN2110 baseband. The clock is then divided by two by the AMN2110 and supplied to the LPC2103 uC.

Chapter 3

Interfaces

3.1 Video Data Input and Conversions

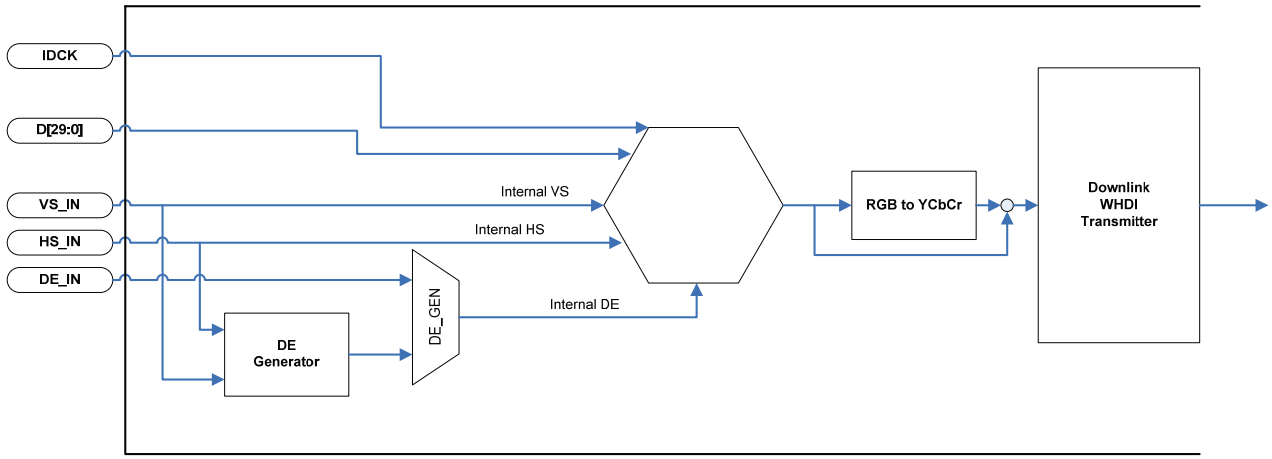


Figure 3: Video Data Processing Path

Figure 3 shows the stages for processing video data through the AMN2110. The HSYNC and the VSYNC input signals are mandatory. The DE input signal is optional and can be created with the DE generator using the HSYNC and the VSYNC pulses.

The video input data is uncompressed digital video up to 3*10 bits in width.

Important: *When connected to a 3*8 bits source, connect the appropriate LSBs to GND*.

The video interface provides a direct connection to the outputs from an HDMI receiver or from an MPEG decoder. The appropriate registers must be configured to describe which format of video to input into the AMN11100. Refer to the appropriate programmer's reference guide for more details.

DATA Enable (DE) Generator

The AMN2110 includes logic to construct the DE signal from the incoming HSYNC, VSYNC and clock. Registers are programmed to enable the DE signal to define the size of the active display region.

Color Space Converter

The AMN11100 can receive either RGB or YCbCr color space. For more details, you may refer to the MAC registers in the programmer's reference guide.

Common Video Input Format

Table 1 describes the common supported video input resolutions.

Table 1: Common Supported Video Input Resolutions

Color Space	Video Format	Bus Width	Input Pixel Clock (MHz)				
			480i	480p	XGA	720p	1080i
RGB/YCbCr	4:4:4	24	27	27	65	74.25	74.25

3.1.1 Video Channel Mapping

The 30 bit video input signals are mapped to the RGB and YCbCr color space according to the options described in the following table:

Table 2: Video Channel Mapping

Option	D[29:20]	D[19:10]	D[9:0]
#1	RED (Cr)	GREEN (Y)	BLUE (Cb)
#2	RED (Cr)	BLUE (Cb)	GREEN (Y)
#3	GREEN (Y)	RED (Cr)	BLUE (Cb)
#4	GREEN (Y)	BLUE (Cb)	RED (Cr)
#5	BLUE (Cb)	RED (Cr)	GREEN (Y)
#6	BLUE (Cb)	GREEN (Y)	RED (Cr)

The AMN11100 allows any of the input video channels options. The first option is the default from power-up. In order to change the video channel mapping, please refer to the appropriate programmer's reference guide.

3.1.2 Video Interface Input Timing Diagram

3.1.2.1 Timing Requirements

Important: *The following parameters relate to the AMN2110 baseband chipset and not to the entire AMN11100 board.*

Table 3: : Video Interface

Symbol	Parameter	MIN	TYP	MAX	Units
T_{DCKCYC}	DCLK period	12.8		40	ns
$T_{DCKFREQ}$	DCLK frequency	25		78.125	MHz
$T_{DCKDUTY}$	DCLK duty cycle	40%		60%	ns
T_{DCKSUR}	Setup time to DCLK rising edge	0.7			ns
T_{DCKHDR}	Hold time to DCLK rising edge	1.1			ns
T_{DCKSUF}	Setup time to DCLK falling edge	1.5			ns
T_{DCKHDF}	Hold time to DCLK falling edge	0.5			ns

3.1.2.2 Timing Diagram

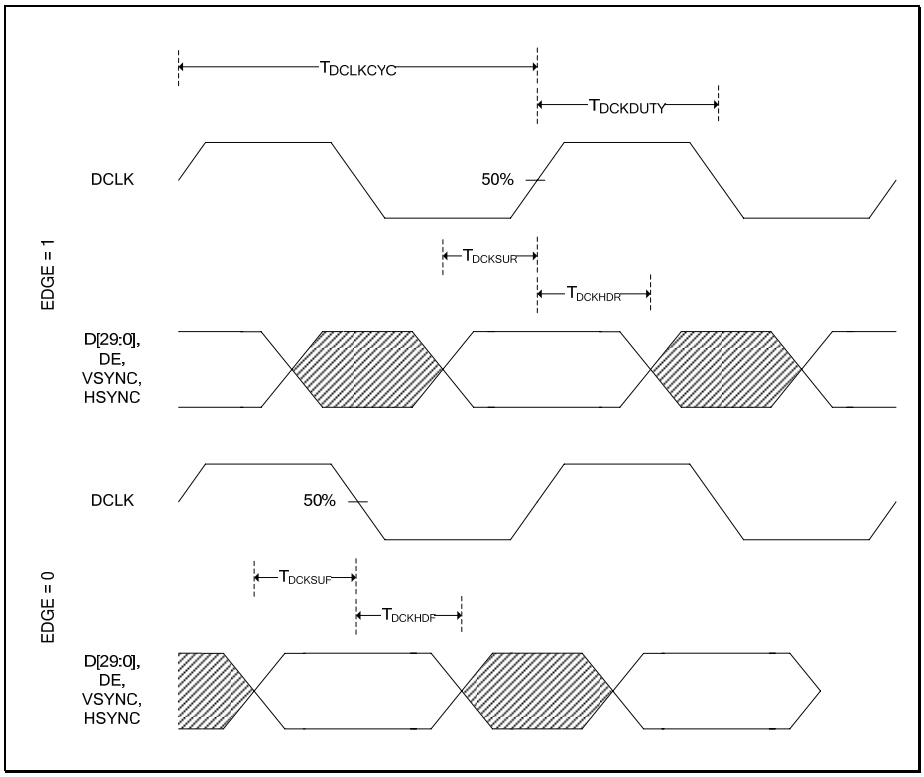


Figure 4: Timing Diagram

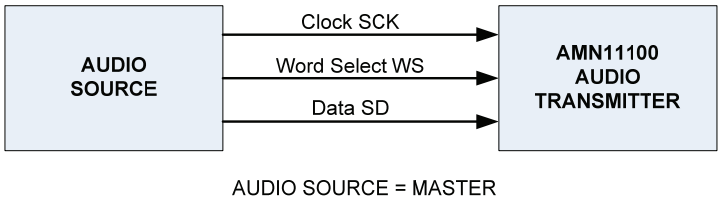
3.2 Audio Data Capture

AMN11100 transports an explicit audio master clock with appropriate data-over-the-wireless link. No constraints exist for a coherent video and audio clock, where coherent means that the audio and the video clock must have been created from the same clock source. The AMN11100 can accept digital audio from either SPDIF or I2S inputs.

The AMN11100 supports two channel audio sampling frequencies of up to 48KHz and of up to 32 bits per sample.

3.2.1 I²S Bus Specification

The AMN11100 supports a standardized communication structure inter-IC sound (I^2S) bus. As shown in Figure 5, the bus has three lines: continuous serial clock (SCK), word select (WS) and serial data (SD). The external device generating SCK and WS is the audio source.



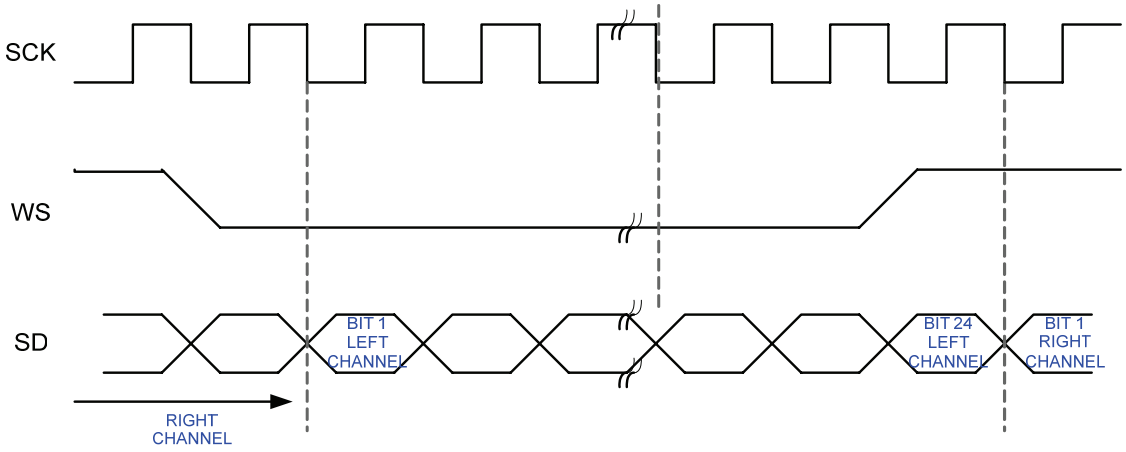


Figure 5: I^2S Simple System Configurations and Basic Interface Timing

The AMN11100 supports an I^2S format of up to 32 bits for each channel (left and right). The serial data is latched into the AMN11100 on the leading (LOW to HIGH) edge of the clock signal. The WS is also latched on the leading edge of the clock signal. The WS line should change one clock period before the first bit of the channel is transmitted.

The AMN1110 transmits explicit clock SD and WS and does not process the audio content. The input audio at the transmitter end is mirrored to the receiver end. The source may have different word lengths, up to 32 bits. However, the AMN11100 always samples and transmits 24 bits over the wireless link.

3.2.1.1 Timing Requirements

Table 4: I2S Audio Interface Timing Requirements

Symbol	Parameter	MIN	TYP	MAX	Units
T_{SCKCYC}	SCK period	325		976	ns
$T_{SCKFREQ}$	SCK frequency	1.024		3.072	MHz
$T_{SCKDUTY}$	SCK duty cycle	40		60	%
$T_{DCKSETUP}$	Setup time to SCK rising edge	25			ns
$T_{DCKHOLD}$	Hold time to SCK rising edge	25			ns

3.2.1.2 Timing Diagram

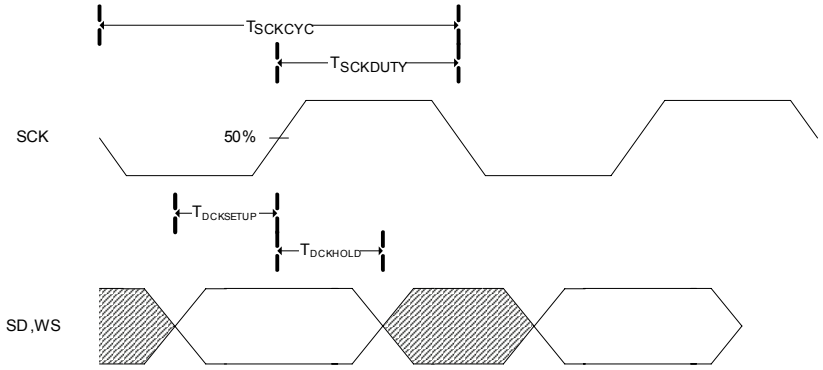


Figure 6: I²S Input Timings

3.2.2 S/PDIF Bus

3.2.2.1 Timing Requirements

The AMN11100 does not require the SPDIF clock. The clock is produced internally by sampling the SPDIF data input at a high clock rate and processing it.

Table 5: Audio Interface Timing Requirements

Symbol	Parameter	Condition	MIN	TYP	MAX	Units
T_{SPCYC}	SPDIF data sampling rate		162		488	ns
T_{SPFREQ}	SPDIF data sampling freq		2.048		6.144	MHz

3.3 Management Buses and Connectors

3.3.1 Two-Wire Serial Bus Interface

The WHDI application observes and controls the AMN11100 via a Two-Wire interface and an interrupt line connecting the application microcontroller and the AMN11100 MiniMAC microcontroller. The protocol of the Two-Wire bus for the WHDI application / MiniMAC interface is described in the following sections.

The Two-Wire bus is bidirectional and, as its name implies, has only two wires: a Serial Clock Line (SCL) and a Serial Data Line (SDA). The Two-Wire architecture includes master and slave devices. The master initiates a data transfer on the bus and generates the clock signal. The AMN11100 MiniMAC operates as a slave device. Each slave device is recognized by a unique address and can operate as either a receive-only device or a transmitter with the ability to both receive and send information.

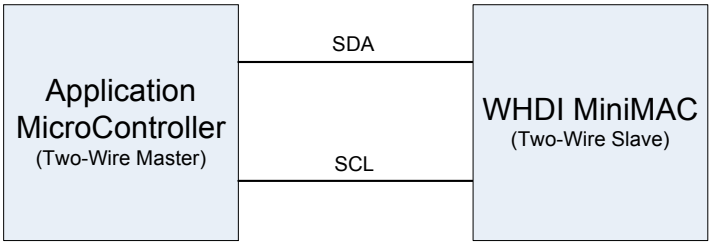


Figure 7: Two-Wire Application / MiniMAC Connection

On top of the Two-Wire low level operation described in sections 3.3.1.2 and 3.3.1.3, the WHDI application and the MiniMAC microcontrollers communicate with each other in a defined protocol, which avoids all possibilities of confusion. The protocol defines command oriented transactions between the application and the WHDI MiniMAC. Each Two-Wire command has a predefined data byte length and is defined to be exactly one Two-Wire transaction long.

3.3.1.1 Device Addresses

The MiniMAC device address may be altered by two jumpers on VDU/VSU board.

Table 6: Device Addresses

Device	Address
MiniMAC uC	0x62 or 0x82 or 0x90 or 0x70 (Board configuration dependant)

Alternatively, the device address can be set in the MAC SW in advance.

3.3.1.2 MiniMAC uC Write Operation

Figure 8 demonstrates a write transaction which sends 2 data bytes and which ends with the master stop bit. Each write transaction sends 1 or more data bytes to the MiniMAC, beginning at an explicit 2 bytes long address. Multiple data bytes may be written as the MiniMAC stores the received register data until the master sends a stop bit. The MiniMAC updates the register value upon a successful termination of a write transaction.

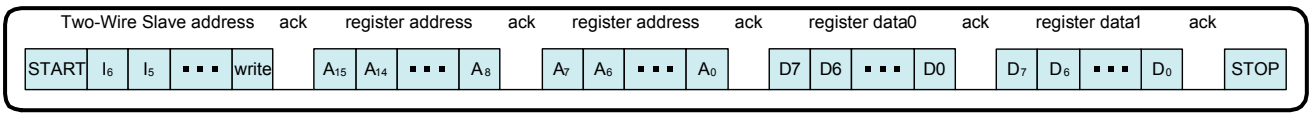


Figure 8: Two-Wire MiniMAC Write Commands

3.3.1.3 MiniMAC uC Read Operation

This operation reads from a specific 2-byte address. The read transaction is divided into two parts. In the first part, the Two-Wire master sends a write command to the slave containing only the required start address. (The address is always 2 bytes long.) In the second part, multiple bytes may be read from consecutive addresses. The MiniMAC puts the appropriate data on the Two-Wire bus and the internal address is automatically incremented. A stop bit is sent by the master only when the entire transaction has been completed.

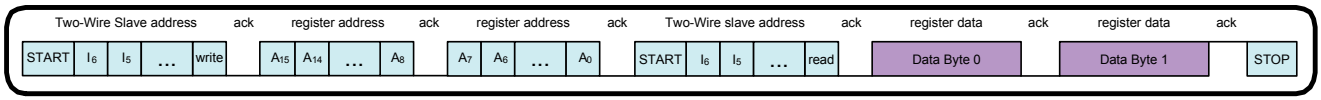


Figure 9: Two-Wire Read Command

3.3.1.4 WHDI Application / MiniMAC Protocol

The WHDI programmer's reference defines the MiniMAC registers data structure. Each register has an associated group ID and index offset address.

The group ID and the index offset are each 1 byte long. Together they define a register address that is 2 bytes long.

Each register has an attributed length (in byte units). All registers within the same group have the same length.

A Two-Wire transaction to a specific register includes 2 bytes of register address and the register data bytes. The register is written in one transaction. If the transaction terminates ahead of time or is too long, the MiniMAC issues an error interrupt and does not store the received values. The register is read in one transaction, as described in section 3.3.1.3. If the read transaction finishes ahead of time, the MiniMAC issues an error interrupt.

3.3.2 Interrupts

There is one interrupt connected to the WHDI connector. The interrupt source is the AMN2110 MiniMAC uC. For details about the interrupt, please refer to the *Programmer's User Guide*.

3.4 Reset and Wake-up Timer

The AMN11100 has one hard $\overline{RESET}$ input pin connected directly to the AMN2110 and through a MicroPower circuit to the LPC2103 uC, as described in Figure 10. Upon power up, the MicroPower circuit asserts the uC reset pin for about 150msec. Assertion of the LPC2103 reset starts its internal wake-up timer, causing the internal chip reset to remain asserted until the external reset is de-asserted, the 20MHz clock runs, a fixed number of clocks have passed and the on-chip flash controller has completed its initialization.

When the LPC2103 internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined reset values. The processor initializes the AMN2110 baseband chipset. After the reset is de-asserted for TBD msec, it is ready to operate.

The wake-up timer monitors the 20MHz clock in order to check whether it is safe to begin code execution.

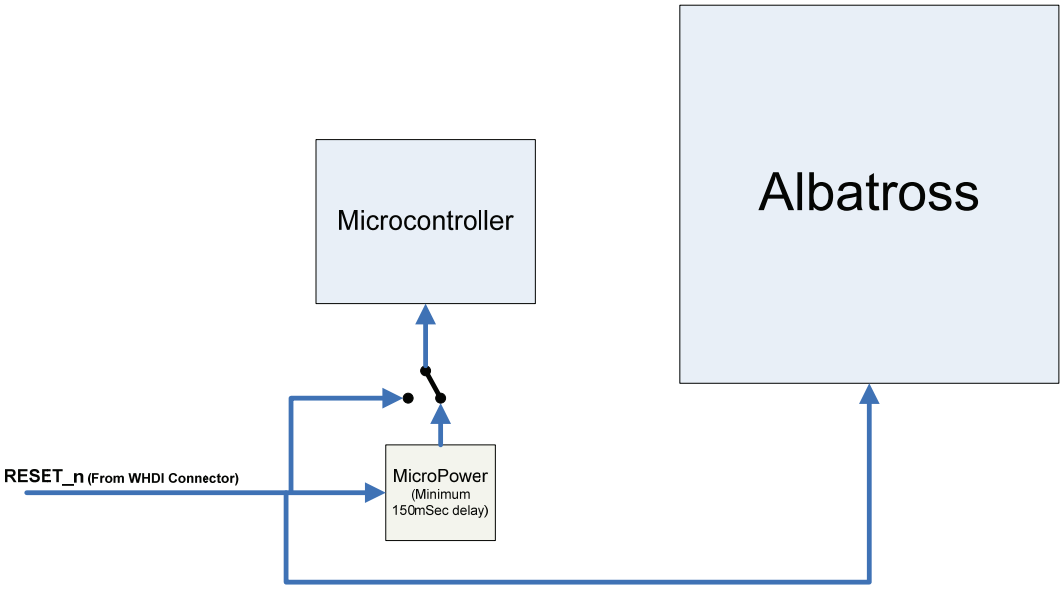


Figure 10: Reset Mechanism

Chapter 4

WHDI Connector Pin-Outs

4.1 Signals

Table 7: WHDI Connector Signals

# of Pins	Pin Name	Description / Functionality	Group	Direction	Remarks
				Tx	
30	D[29:0]	30-bit RGB (10:10:10) or YCrCb (10:10:10)	Video	In	
1	DCLK	Video data clock	Video	In	Up to 78.125 MHz
1	DE	Data enable	Video	In	
1	H_SYNC	Horizontal sync	Video	In	
1	V_SYNC	Vertical sync	Video	In	
1	SPDIF	SPDIF audio interface	Audio	In	
1	SD	I^2S audio interface Serial Data signals	Audio	In	
1	SCLK	I^2S continuous serial clock	Audio	In	Up to 3.072Mbps
1	WS(LRCLK)	I^2S Word Select (Left/right clock) which defines also the sampling rate	Audio	In	
1	MCLK	I^2S master clock coherent to WS according to specified ratio	Audio	NA	Rate is adjustable on RX side
1	SDA	Two-wire Serial Bus Data (Slave Mode)	Control	I/O	Control I/F for WHDI
1	SCL	Two-wire Serial Bus Clock (Slave Mode)	Control	In	Control I/F for WHDI
1	INT	Interrupt from WHDI module	Control	Out	
1	$\overline{RESET}$	Reset / Power-down line	Control	In	
1	TBD6	TBD6	NA	NA	
6	TBD[5:0]	TBD0, TBD1, TBD4, TBD5 are reserved in AMN11100, AMN12100 as an **option** for external power rail to the on board uC	TBD	TBD	
8	3.3V	VCC	Power	Power	300 mA maximum rating per pin
6	3.3V_OR_5V	High Power rail pins, In AMN11100, AMN12100 connect these power rail pins to the 3.3V power rail	Power	Power	For board designed as "High-Power" PA connect this rail to 5V, For Rx (AMN12100) connect to 3.3V
15	GND	Ground	Power	Power	

†Data in this table is preliminary.

4.2 Connector Schematics

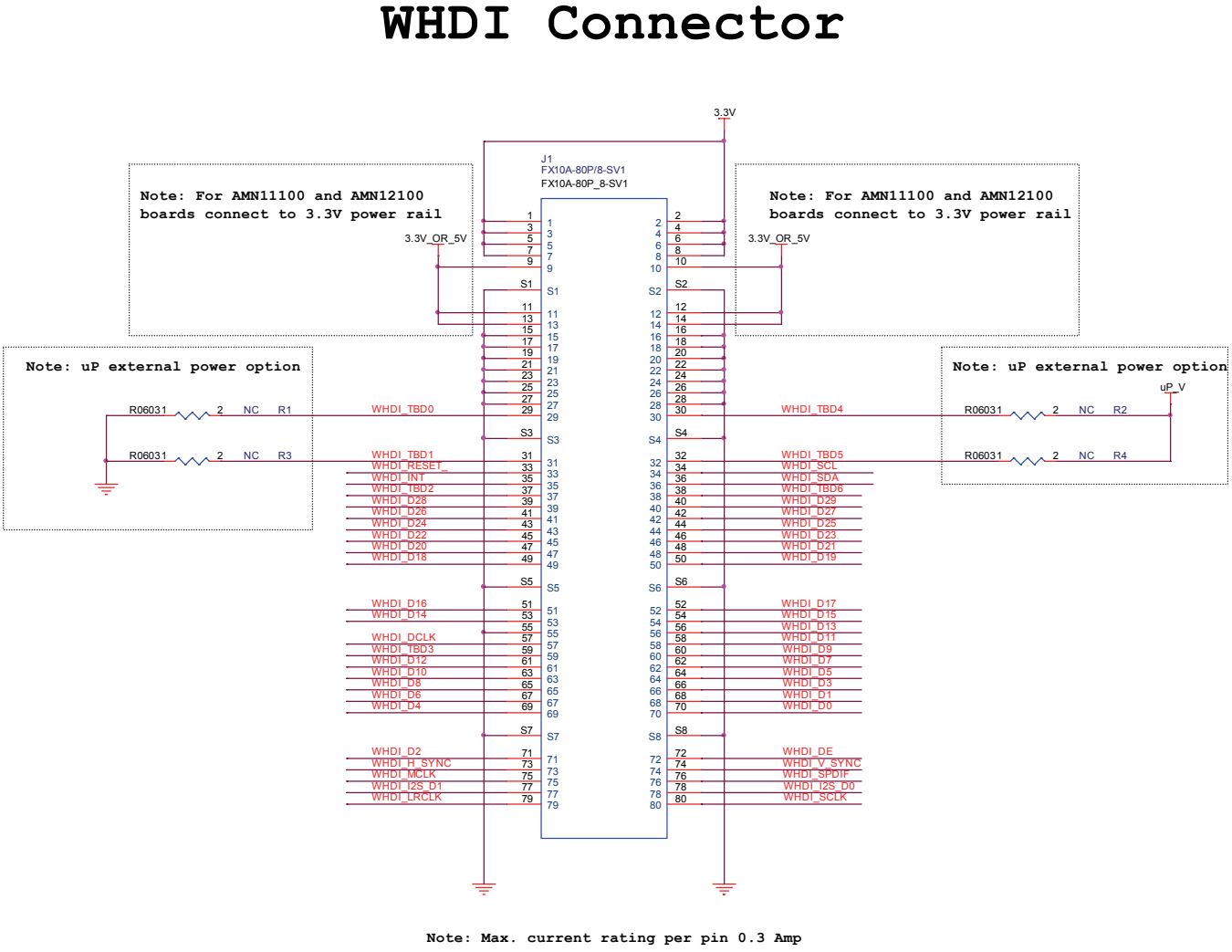


Figure 11: WHDI Connector

4.3 Pin List

Table 8: Tx WHDI Connector Pin List

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	3.3V	31	1.8V(*)	61	D12
2	3.3V	32	1.8V(*)	62	D7
3	3.3V	33	$\overline{RESET}$	63	D10
4	3.3V	34	SCL	64	D5
5	3.3V	35	INT	65	D8
6	3.3V	36	SDA	66	D3
7	3.3V	37	N.C	67	D6
8	3.3V	38	N.C	68	D1
9	3.3V_OR_5V(**)	39	D28	69	D4
10	3.3V_OR_5V(**)	40	D29	70	D0
11	3.3V_OR_5V(**)	41	D26	71	D2
12	3.3V_OR_5V(**)	42	D27	72	DE
13	3.3V_OR_5V(**)	43	D24	73	HSYNC
14	3.3V_OR_5V(**)	44	D25	74	VSYNC
15	GND	45	D22	75	N.C
16	GND	46	D23	76	SPDIF
17	GND	47	D20	77	N.C
18	GND	48	D21	78	I2S_D0
19	GND	49	D18	79	LRCLK
20	GND	50	D19	80	SCLK
21	GND	51	D16		
22	GND	52	D17		
23	GND	53	D14		
24	GND	54	D15		
25	GND	55	GND		
26	GND	56	D13		
27	GND	57	DCLK		
28	GND	58	D11		
29	1.8V(*)	59	N.C		
30	1.8V(*)	60	D9		

(*) Optional – Contact Amimon Ltd. for more details.

(**) These lines should be connected to a 3.3V power supply. An option for a 5V power supply exists for extended range. Extended range requires a different AMN1110 version. Contact Amimon Ltd. for further details.

Chapter 5

Electrical Specifications

5.1 Operating Conditions and Electrical Characteristics

The following tables describe the operating conditions and electrical characteristics required for working with the AMN11100.

Table 9: Absolute Maximum Ratings over Operating Case Temperature Range

Supply input-voltage range, VI	0 to 3.6 V
Ambient temperature range	0°C to 70°C
Storage temperature range, Tstg	-40°C to 125°C

Table 10: Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Unit
DV_{DD}	Module supply voltage	3.15	3.3	3.45	V
V_{SS}	Supply ground	0			V
V_{IH}	High-level input voltage	0.7 DV_{DD}			V
V_{IL}	Low-level input voltage			0.3 DV_{DD}	V
V_{OH}	High-level output voltage (DV_{DD} = MIN, I_{OH} = MAX)	0.8 DV_{DD}			V
V_{OL}	Low-level output voltage (DV_{DD} = MIN, I_{OL} = MAX)			0.22 DV_{DD}	V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
T_C	Operating case temperature	0		70	°C

Table 11: Electrical Characteristics over Recommended Range of Supply Voltage and Operating Conditions

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_I	Input current	V_I = V_{SS} to DV_{DD}			±20	µA
I_{OZ}	Off-state output current	V_O = DV_{DD} or 0 V			±20	µA
I_{DVDD}	Module supply	DV_{DD} = Max., Video Clock = 75 MHz, with activity on all I/O terminals and transmitting in maximum power.			1800	mA
C_i	Input capacitance				10	pF
C_o	Output capacitance				10	pF

Chapter 6

Design Guidelines

6.1 Digital Layout Recommendation

To better understand the layout guidelines, please refer to the AMN11100 schematics which are part of the HDK package.

6.1.1 Stuck up

Recommended stuck up for 10 layers design:

- Total thickness 1.6mm
- Tolerance: 10%

Table 12: Digital Layout Recommendation

				Conductor Width [mil]				Control Impedance [ohm]					
StuckUp				Before				Stripline		Differential		Layer	
	thickness	Scale		Required		Design		Before		Before			
Title	Des.	Oz/mil	Layer	line	space	line	space	Required	Design	Required	Design	Type	No
Cu	0.5	Oz	CS	5	0	5.25	5.25	0	0	100	100	SIG	L1
Space	7	mil		15	30	14	31	0	0	50	48		
Cu	0.5	Oz	L2	11	0	12	0	50	50	0	0	GND	L2
Space	4	mil		0	0	0	0	0	0	0	0		
Cu	0.5	Oz	L3	5	6	4.25	6.75	0	0	100	100	SIG	L3
Space	7	mil		6	0	5	0	50	50	0	0		
Cu	0.5	Oz	L4	0	0	0	0	0	0	0	0	GND	L4
Space	4	mil		0	0	0	0	0	0	0	0		
Cu	0.5	Oz	L5	0	0	0	0	0	0	0	0	VCC	L5
Space	9	mil		0	0	0	0	0	0	0	0		
Cu	0.5	Oz	L6	5	6	4.5	6.5	0	0	100	100	SIG	L6
Space	4	mil		6	0	5.5	0	50	50	0	0		
Cu	0.5	Oz	L7	0	0	0	0	0	0	0	0	GND	L7
Space	7	mil		0	0	0	0	0	0	0	0		
Cu	0.5	Oz	L8	5	6	4.25	6.75	0	0	100	100	SIG	L8
Space	4	mil		6	0	5	0	50	50	0	0		
Cu	0.5	Oz	L9	11	0	12	0	50	50	0	0	GND	L9
Space	7	mil		15	30	14	31	0	0	50	48		
Cu	0.5	Oz	PS	5	0	5.25	5.25	0	0	100	100	SIG	L10

6.1.2 General Guidelines

- Keep traces as short as possible.
- Traces should be routed over full solid reference plans.
- Sensitive lines like reset and clocks should be routed with special care.
  - These lines should be routed over full solid power plans (ground or power).
  - Traces should be routed at least 2 times the trace width away from other lines in the same routing layer.
  - Place a series resistor ~30 ohm at the clock source.
- Keep digital signals away from the analog side.

6.1.3 WHDI Lines

- Place series resistors on all output lines (near the outputs pins).
- Series resistors on input lines are unnecessary. (The series resistors should be placed on the interface board.)

6.1.4 Power and Ground

- Use a solid ground plan.
- Ground plans separation is unnecessary.
- Place decoupling capacitors near power pins. (Refer to the schematics and BOM for recommended values.)
- Analog power pins should be filtered with ferrite beads. (Refer to the schematics and BOM for recommended values.)

6.1.4.1 Power Rails/Pins Summary for AMN2110 Chip:

- Analog:
  - 1.2 Volt:
  - Pins names:
    - DA10_0_AVDD1V2
    - DA10_1_AVDD1V2
    - DA10_2_AVDD1V2
    - DA10_3_AVDD1V2
    - AD8_AVDD1V2
    - AD10_AVDD1V2_0
    - AD10_AVDD1V2_1
    - PLL_AVDD
  - 3.3 Volt:
  - Pins:
    - DA10_0_AVDD3V3_0
    - DA10_0_AVDD3V3_1
    - DA10_1_AVDD3V3_0
    - DA10_1_AVDD3V3_1
    - DA10_2_AVDD3V3_0
    - DA10_2_AVDD3V3_1
    - DA10_3_AVDD3V3_0
    - DA10_3_AVDD3V3_1
- Digital:
  - 1.2 Volt:
  - Pins names:
    - VDD_0 to VDD_9 (total 10 pins)
  - 3.3 Volt:
  - Pins:
    - VDD_IO_0 to VDD_IO_14 (total 15 pins)

6.2 RF Design Recommendation

6.2.1 RF Components

All passive components must have compatible performance with components used in the Amimon reference design.

6.2.2 Power Management

The power management is divided such that each channel has independent filtered power supply of 2.85Vdc. Figure 1 shows the power scheme of the RF section of the transmitter.

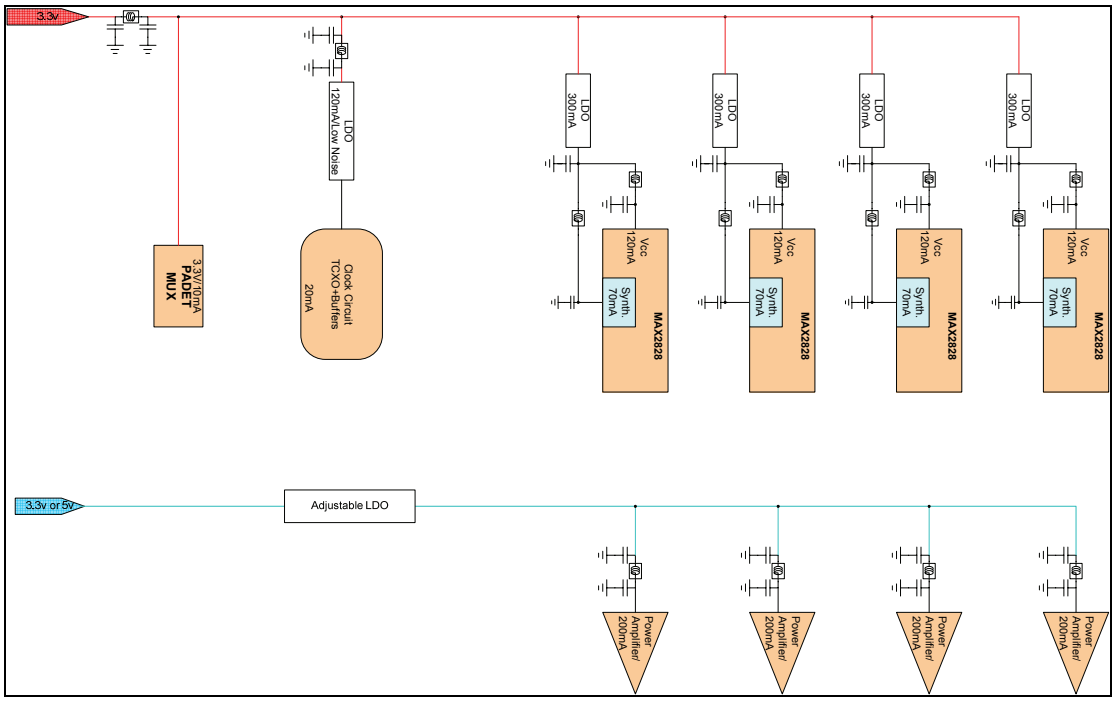


Figure 12: Transmitter RF Power Scheme

6.2.3 Device Application Notes

For the best performance, follow the application guidelines of the chosen devices.

Regarding the MAX2828 transceiver, follow the Application Note AN3630 that can be downloaded from Maxim-ic website.

6.2.4 Antennas

The design of the antennas and matching is performed individually for each product. Changing board stack-up or outline of the RF section can impact the system performance and a matching procedure should be performed.

Chapter 7

Mechanical Dimensions

The following shows the mechanical dimensions for the AMN11100:

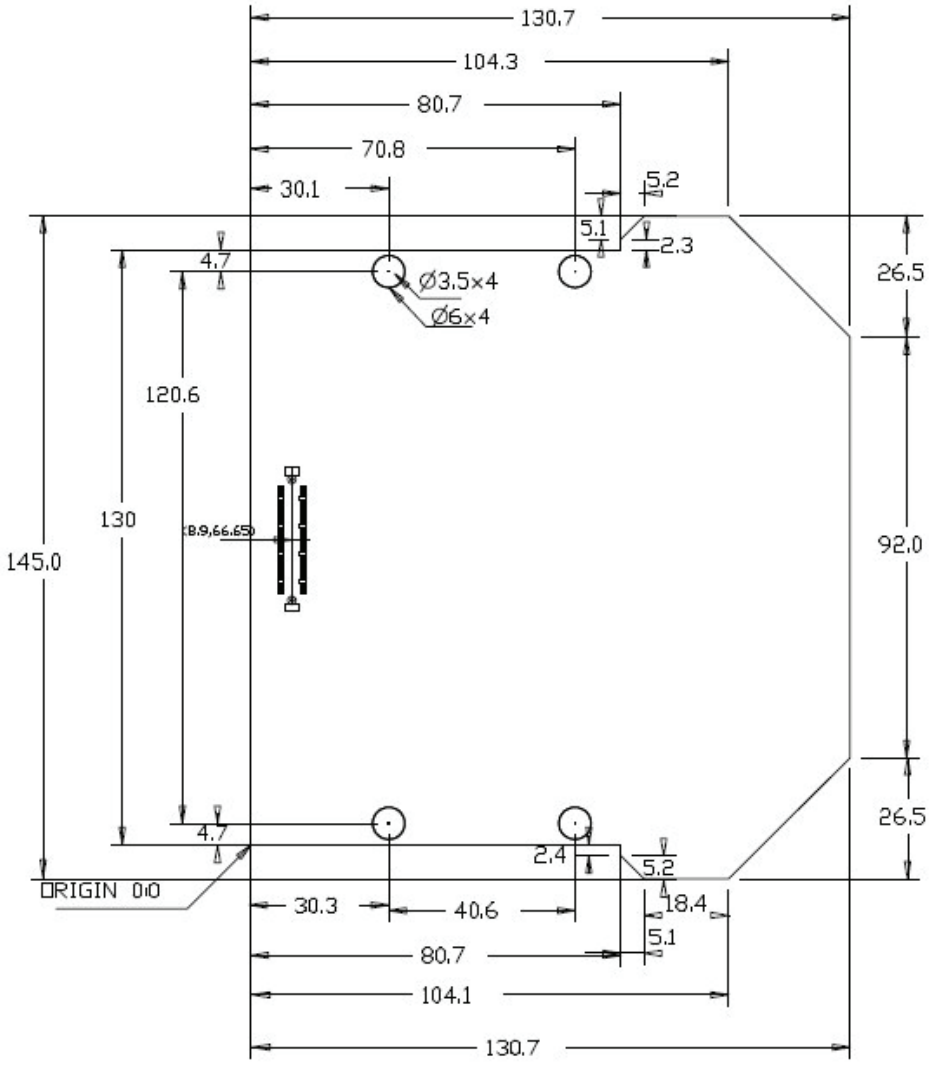


Figure 13: Mechanical Dimensions