

AMN12310

WHDI™ Receiver

Module Datasheet

Version 0.5

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Revision History

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0.2	15.6.08	Revision <ul style="list-style-type: none"> • Board Mechanical size • Reset and Wake-up Timer modified • RF frame modified • Power switch on RF removed • Operating Conditions and Electrical Characteristics modified • AMN11310 Block Diagram modified • Unhide Certification & Compliance • Power requirements • Mini-MAC changed to MAC. • WHDI Module Configuration • Connector Schematics • Stack up • Test Points and Jumpers
0.3	20.7.08	<ul style="list-style-type: none"> • Fixed link to STMF datasheet p-18. • Fixed Table 1: Rx WHDI Connector Pin List • Fixed recommended stack up table p- 29
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0.5	2.9.08	<ul style="list-style-type: none"> • Change in FCC chapter

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Preliminary

Chapter 1

Introduction

The AMN12310 is the second generation of WHDI™ receiver board. It is based on AMIMON's WHDI receiver chipset: the AMN2210 baseband receiver and the AMN3210 RFIC receiver.

The AMN12310 WHDI™ wireless receiver module, together with the AMN11310 wireless transmitter module, presents the ultimate solution for converting any High Definition (HD) system into a wireless one. These add-on modules enable wireless A/V applications that easily fit into the living room and eliminate traditional A/V wiring. The perfect HD video and audio quality and the high robustness are unmatched by any other wireless technology, and present a true alternative to cable. The WHDI system transmits *uncompressed* video and audio streams wirelessly and thus simplifies and eliminates system issues, such as: lip-sync, large buffers and other burdens like retransmissions or error propagation.

1.1 Features

- **Uncompressed and uncompromised HD video quality, using AMIMON's baseband chipsets:**
 - AMN2210: WHDITM Baseband Receiver
 - AMN3210: WHDITM RFIC Receiver
- **WHDI – Wireless High Definition Interface:**
 - Digital video: 30-bit RGB or YCrCb
 - Digital audio: I2S and SPDIF
 - Two-wire serial bus slave interface
 - One interrupt line
- **Supports any uncompressed video resolutions, including:**
 - HD: 720p, 1080i, 1080p, 576i, 576p, 480p, 480i
 - PC: VGA (640x480), SVGA (800x600), XGA (1024x768)
 - Panel: 854x800, 1280x768, 1366x768
- **Audio:**
 - Up to 3Mbps audio stream:
 - I2S: Two PCM channels (sampled up to 48 KHz x 24 bit)
 - SPDIF: Including AC-3, DTS
- **Strong 256-bit AES encryption**
- **User-defined two-way channel with minimum 10 Kbps for data and control**
- **Less than 1mSec latency between source and sink**

- **Small mechanical footprint:**
 - With PCB integrated antennas
- **RF characteristics:**
 - MIMO technology, using 5GHz unlicensed band, 18MHz bandwidth.
 - Coexists with 802.11a/n and 5.8GHz cordless devices.
 - Support for Automatic Transmission Power Control (ATPC).
 - No line of sight needed between transmitter and receiver. It has a range of over 30 meters, suitable for almost any room.
 - 14mW typical transmission power of the uplink channel.
 - Maximum 45mW transmission power of the uplink channel.
 - Minimum -65 dBm received signal power for successful operation
- **Current consumption**
 - Option to to disable 40MHz digital clock to AMN2210 from AMN3210.
- **Power requirements:**
 - 3.3V ($\pm 5\%$), ~4.2W
- **Certification & Compliance:**
 - FCC
 - This product is for indoor use only in the band of 5.15-5.25GHz.
 - This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
 - Any changes or modifications not expressly approved by Amimon for compliance could void the user's authority to operate the equipment.
 - This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
 - Reorient or relocate the receiving antenna.
 - Increase the separation between the equipment and receiver.
 - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
 - Consult the dealer or an experienced radio/TV technician for help.
 - MIC
 - This device has complied with Japan Radio law:
 - Item 19-11 of Article 1 paragraph 1 of certification ordinance.
 - Item 19-3 of Article 1 paragraph 1 of certification ordinance.

- **Caution:** The module should be positioned so that personnel in the area for prolonged periods may safely remain at least 20 cm (8 in) in an uncontrolled environment from the module.

Preliminary

Chapter 2

Overview

The AMN12310 WHDI Video Display Unit (VDU) is designed to be at the receiver end of the WHDI downstream. The AMN12310 receives wireless downstream transmission, demodulates it and regenerates the video, audio and control content transmitted by the AMN11310 WHDI transmitter. The receiver works at the 5GHz unlicensed band. Figure 1 displays a block diagram of the AMN12310. It has an MIMO design of five wireless input channels, and one slow rate output wireless channel, which generates an upstream channel for data content transmissions. The outputs from the VDU are digital uncompressed video, digital audio and control, all via the WHDI connector. The MAC uC is responsible for the control and the management.

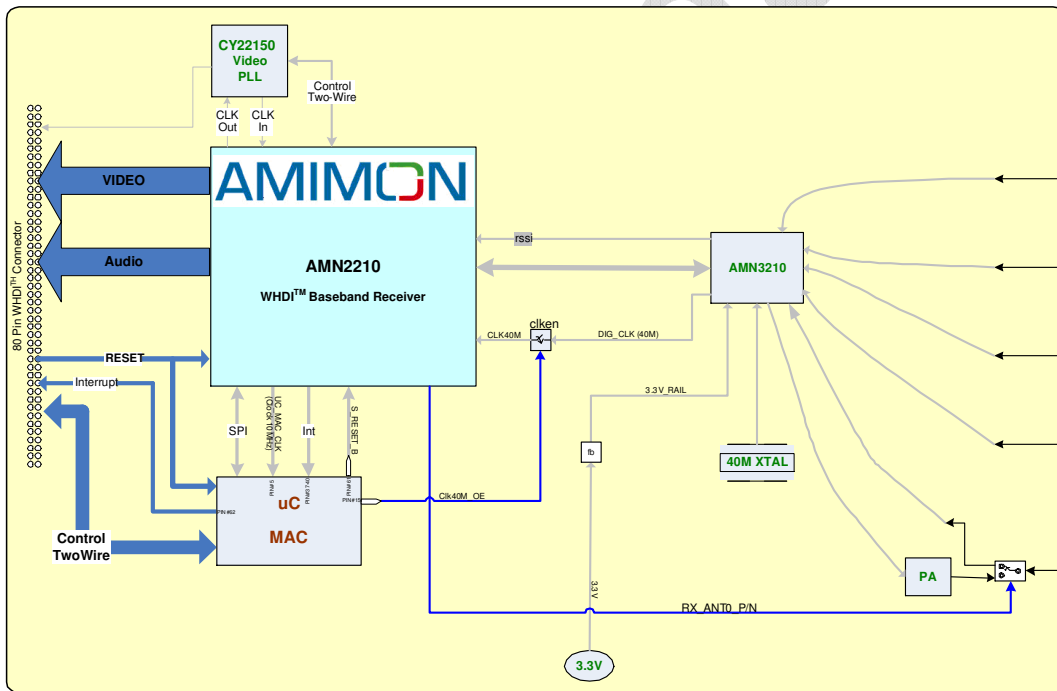


Figure 1: AMN12310 Block Diagram



The main building blocks of the AMN12310 are as follows:

- **AMN2210 WHDI Baseband Receiver**, as briefly described on page 12
- **STM32F MAC μ Controller**, as briefly described on page 12
- **AMN3210 WHDI™ 5GHz Transceiver**, as briefly described on page 13
- **Power Amplifier (PA)**, as briefly described on page 13
- **Board Connector (WHDI™ Connector)**, as described on page 13
- **Clock enable switch for input 40M clock to AMN2110**, as described on page 13
- **40MHz Crystal Oscillator**, as described on page 13
- **CY22150 External Video PLL**, as described on page 14

2.1 AMN2210 WHDI Baseband Receiver

The AMN2210 WHDI™ baseband receiver chip is the *heart* of the AMN12310 WHDI Receiver module. The AMN2210 interfaces the A/V source through the WHDI connector, and is controlled on board by the MAC uC.

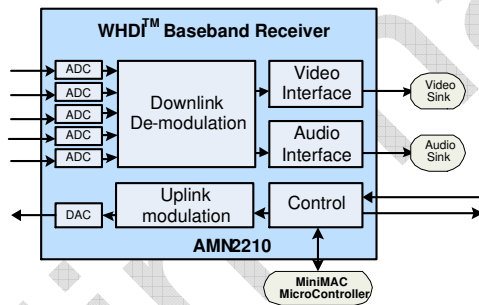


Figure 2: WHDI Baseband Receiver Chipset

The AMN2210 is based on MIMO technology receiving up to five input channels. Five analog-to-digital converters and one digital-to-analog converter are embedded within the chip.

The AMN2210 internal PLL accepts an input clock frequency of 40MHz. The input frequency is multiplied and then used as an internal system clock.

2.2 STM32F MAC μ Controller

The STM32F Microcontroller is based on an ARM 32-bit Cortex™-M3 CPU, with 128 Kbytes of embedded Flash memory. It is used as an external microcontroller for implementing the MAC layer of the WHDI link.

The STM32F Internal PLL accepts an input clock frequency of 10MHz and generates an internal 60MHz system clock. The STM32F also has the option to work with an internal 4-to-16 MHz crystal oscillator.

2.3 AMN3210 WHDI™ 5GHz Transceiver

The VDU uses AMN3210 WHDI receiver chip. The AMN3210 is a fully integrated Zero-IF MIMO receiver specifically designed for WHDI applications using OFDM modulation for single-band 4.9GHz to 5.9GHz. The device includes:

- Five Complete Downlink Zero-IF Receivers
- One Uplink Direct Conversion Transmitter
- Integrated Synthesizer/VCO
- Internal DC Servo Loops
- RSSI, RF and Baseband Control Interface
- Power Management Unit
- 3-Wire SPI Interface

To complete RF front-end solution, the AMN3210 uses external PA, RF Band Pass Filters (BPF), RF BALUNs and a few passive components.

2.4 Power Amplifier (PA)

In order to extend the operating range for the AMN12310 upstream, the RF transmitter uses a power amplifier. The power amplifier has an output power detector for TPC purposes.

AMN12310 uses Sharp IRM053U7 PA.

2.5 Board Connector (WHDI™ Connector)

For information regarding the connector specification and pin-outs see section 4.1, *Signals*, page 26.

2.6 Clocks

2.6.1 40MHz Crystal Oscillator

An on-board 40MHz crystal oscillator is connected to the AMN3210 chip.

2.6.2 40Mhz Digital Clock

AMN3210 drives the 40MHz clock to the baseband AMN2210 through a buffer (with output enable).

This clock is named DIG_CLK. The control to the output buffer is named Clk40M_OE.

2.6.3 10Mhz Micro Controller Clock

The DIG_CLK (40MHz) clock is divided by four by the AMN2210 and generates 10MHz that drives the STM32F UC.

2.7 CY22150 External Video PLL

An external PLL is used for re-generating the video clock. The PLL receives a lower speed clock (generally limited to 10 MHz), which is generated inside the AMN2210 according to the video parameters. The PLL multiplies the clock to the desired speed dictated by the incoming video format (for example: 74.25Mhz for 720p or 1080i).

Preliminary

Chapter 3

Interfaces

3.1 Video Data Input and Conversions

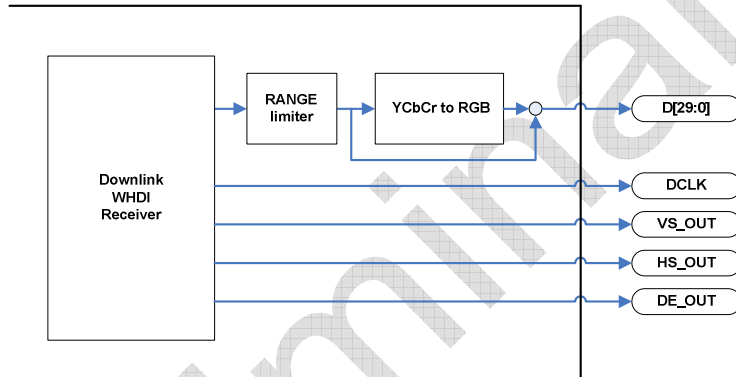


Figure 3: Video Data Receiver Path

Figure 3 shows the basic control over the video data output. Essentially the receiver mirrors the video format of the transmitter end and so most of the configurations are done on the transmitter end.

The video output data is uncompressed digital video up to 3*10 bits in width. The video interface provides a direct connection to the inputs of a display device, an HDMI transmitter, or any other video interface device.

Color Space Converter

The receiver can output either RGB or YCbCr color space. For more details, you may refer to the MAC registers in the programmer's reference guide.

Color Range Limiter

The YCbCr data range can be limited to 16-235.

Common Video Output Format

Table 2 lists the common supported video output resolutions.

Table 2: Common Supported Video Input Resolutions

Color Space	Video Format	Bus Width	Input Pixel Clock (MHz)				
			480i	480p	XGA	720p	1080i
RGB/YCbCr	4:4:4	24	27	27	65	74.25	74.25

Video Channel Mapping

The 30 bit video output signals are mapped to the RGB and YCbCr color space according to the options described in the following table:

Table 3: Video Channel Mapping

Option	D[29:20]	D[19:10]	D[9:0]
#1	RED (Cr)	GREEN (Y)	BLUE (Cb)
#2	RED (Cr)	BLUE (Cb)	GREEN (Y)
#3	GREEN (Y)	RED (Cr)	BLUE (Cb)
#4	GREEN (Y)	BLUE (Cb)	RED (Cr)
#5	BLUE (Cb)	RED (Cr)	GREEN (Y)
#6	BLUE (Cb)	GREEN (Y)	RED (Cr)

The AMN123100 allows any of the output video channels options. The first option is the default from power-up. In order to change the video channel mapping, refer to the appropriate programmer's reference guide.

3.2 Video Interface Output Timing Diagram

3.2.1 Timing Requirements

Important: The following parameters relate to the AMN2210 baseband chipset and not to the entire AMN12310 board.

Table 4: Video Interface

Symbol	Parameter	MIN	TYP	MAX	Units
TDCKCYC	DCLK period	12.5		40	Ns
TDCKFREQ	DCLK frequency	25*		80	MHz
TDCKDUTY	DCLK duty cycle	40%		60%	Ns
TDCKPDR	Propagation delay after DCLK rising edge	1.0		4.0	Ns
TDCKPDF	Propagation delay after DCLK falling edge	1.0		4.0	Ns

* It is possible to support lower clock frequency using an external PLL for video clock generation.

3.2.1.1 Timing Diagram

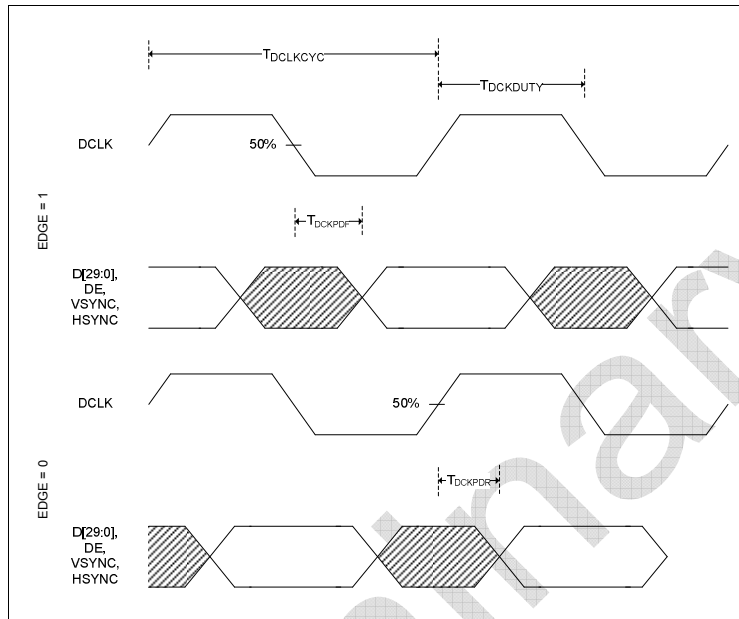


Figure 4: Timing Diagram

3.3 Audio Data Capture

AMN12310 audio processing logic block receives the audio stream from the WHDI wireless link and regenerates the appropriate clock and data. If the transmitter end was configured to SPDIF audio interface, then the audio is output on the receiver side through the SPDIF. The same is true for the I²S interface.

No constraints exist for a coherent video and audio clock, where *coherent* means that the audio and the video clock must have been created from the same clock source. The AMN12310 supports two-channel audio-sampling frequencies of up to 48 KHz, 32 bits per sample.

3.3.1 I²S Bus Specification

The AMN12310 supports a standardized communication structure inter-IC sound (I²S) bus. As shown in Figure 5, the bus has three lines: continuous serial clock (SCK), word select (WS) and serial data (SD). In addition, it has a MCLK signal which is synchronized to and a multiple of the WS. The external device generating SCK and WS is the AMN12310.

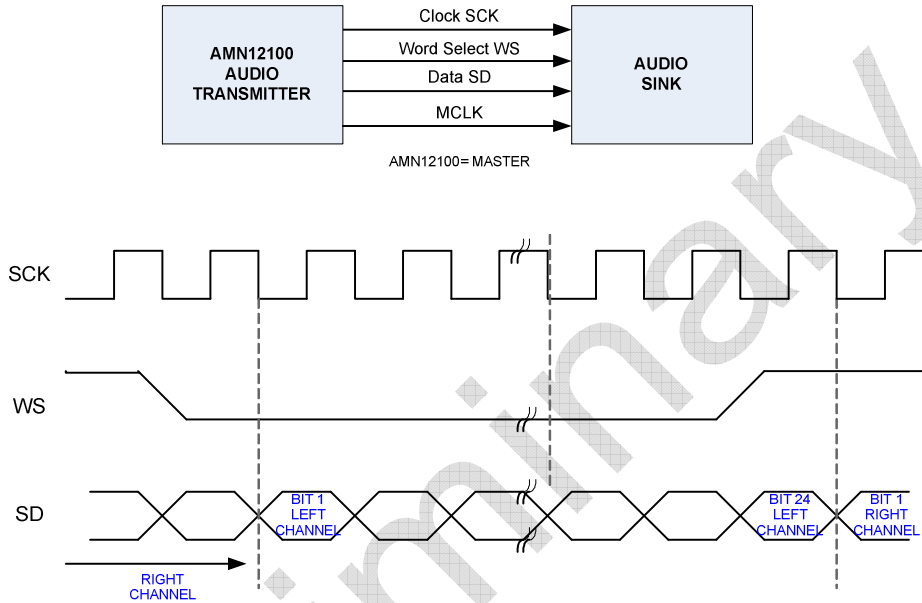


Figure 5: I²S Simple System Configurations and Basic Interface Timing

The AMN12310 outputs exactly 32 bits for each channel (left and right). By default, the serial data is valid on the leading (LOW to HIGH) edge of the clock signal, but it can also be configured to be valid on the edge (HIGH to LOW) of the clock signal. The WS is also valid by default on the leading edge of the clock signal. The WS line changes one clock period before the first bit of the transmitted channel.

The AMN12310 mirrors the transmitter's end audio inputs and so the MSB and the LSB position are defined at the audio source at the transmitter side. In case the audio samples in the transmitter are less than 32 bits long, they are padded with zeroes to generate receiver output samples of 32 bits.

3.3.1.1 MUTE

The AMN12310 has an error detection mechanism. It outputs a high MUTE signal in case of bad audio reception (bad frames).

3.3.1.2 Timing Requirements

Table 5: Audio Interface Output Timing

Symbol	Parameter	MIN	TYP	MAX	Units
TSCKCYC	SCK period	325		976	ns
TSCKFREQ	SCK frequency	1.024		3.072	MHz
TSCKDUTY	SCK duty cycle	40		60	%
TDCKPDR	Propagation delay after SCK rising edge			25	ns
TDCKPDF	Propagation delay after SCK falling edge			25	ns

3.3.1.3 Timing Diagram

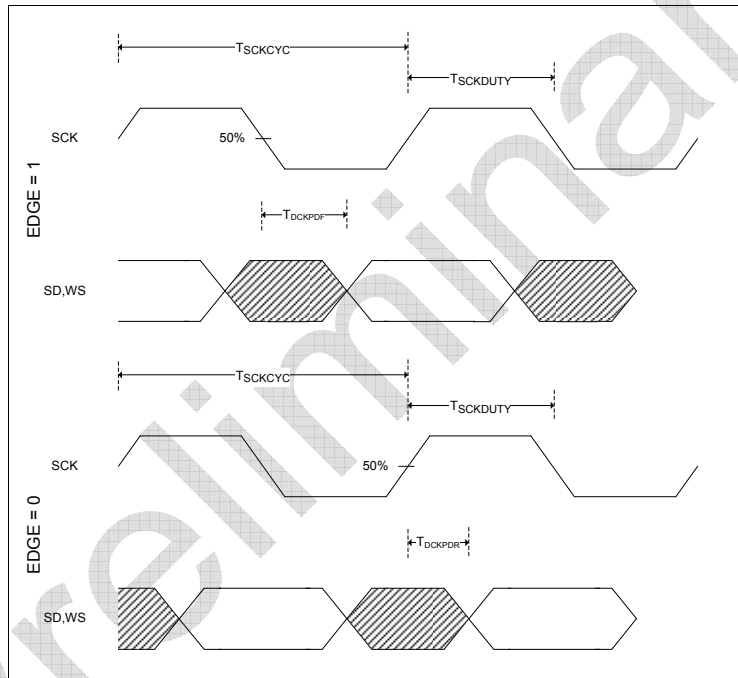


Figure 6: I²S Output Timings

3.3.1.4 MCLK Specifications

In addition, AMN2210 outputs a MCLK signal which is synchronized to and a multiple of the WS. The default configuration of the MCLK frequency is 256 times the sampling frequency of the audio signal. For example, if the audio sampling frequency is 48 KHz, the MCLK frequency will be 12.288 MHz. The following table provides the specification of the MCLK –

Table 6: MCLK timing.

Symbol	Parameter	MIN	TYP	MAX	Units
T _{MCKCYC}	MCK period	244.14		81.38	ns
T _{MCKFREQ}	MCK frequency	4.096*		12.288**	MHz
T _{MCKDUTY}	MCK duty cycle	40		60	%
T _{DOCKPDR}	Propagation delay after MCK rising edge			25	ns
T _{DOCKPDF}	Propagation delay after MCK falling edge			25	ns
T _{JITTER-CYC-CYC}	Cycle-to-cycle jitter***		5		ns

* The minimum frequency is obtained by using the minimum audio sampling frequency of 32 KHz and the minimum clock rate multiplication of 128.

** The maximum frequency is obtained by using the minimum audio sampling frequency 48 KHz and the minimum clock rate multiplication of 256.

*** The cycle-to-cycle jitter is based on the system clock of the AMN2210, which is 200 MHz.

3.4 Management Buses and Connectors

3.4.1 Two-Wire Serial Bus Interface

The WHDI application observes and controls the AMN12310 via a Two-Wire interface and an interrupt line connecting the application microcontroller and the AMN12310 MAC microcontroller. The protocol of the Two-Wire-bus for the WHDI application / MAC interface is described in the following sections.

The Two-Wire bus is bidirectional and, as its name implies, it has only two wires: a Serial Clock Line (SCL) and a Serial Data Line (SDA). The Two-Wire architecture includes master and slave devices. The master initiates a data transfer on the bus and generates the clock signal. The AMN12310 MAC operates as a slave device. Each slave device is recognized by a unique address and can operate as either a receive-only device or a transmitter with the ability to both receive and send information.

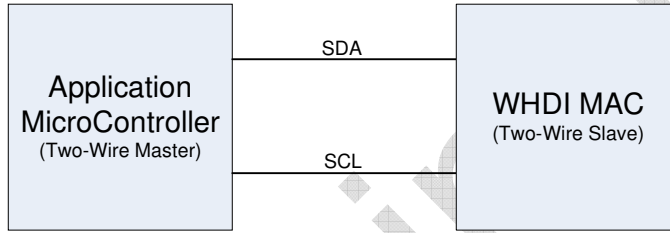


Figure 7: Two-Wire/Application-MAC Connection

On top of the Two-Wire low level operation described in sections 3.4.1.3 and 3.4.1.4, the WHDI Application and the MAC microcontrollers communicate with each other in a defined protocol, which avoids all possibilities of confusion. The protocol defines command oriented transactions between the application and the WHDI MAC. Each Two-Wire command has a predefined data byte length and is defined to be exactly one Two-Wire transaction long.

3.4.1.1 Two-Wire Timing

Generally, the clock frequency of the bus is dictated by the slowest device on the Two-Wire interface. However, the selected MAC supports the 100 KHz SCL frequency rate.

Refer to STM32F Two-wire reference application note for detailed description of the physical protocol and timing.

<http://www.st.com/stonline/products/literature/ds/13587.pdf>, pp 55-59.

3.4.1.2 Device Addresses

The MAC device address may be altered by two jumpers on VDU/VSU board.

Table 7: Device Addresses

Device	Address
MAC μ C	0x62 or 0x82 or 0x90 or 0x70 (Board configuration dependant)

Alternatively, the device address can be set in the MAC SW in advance.

3.4.1.3 MAC uC Write Operation

Figure 8 demonstrates a write transaction which sends 2 data bytes and which ends with the master stop bit. Each write transaction sends one or more data bytes to the MAC, beginning at an explicit 2 bytes long address. Multiple data bytes may be written as the MAC stores the received register data until the master sends a stop bit. The MAC updates the register value upon a successful termination of a write transaction.

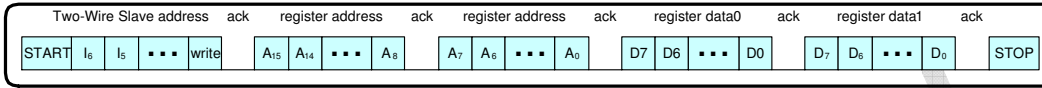


Figure 8: Two-Wire MAC Write Commands

3.4.1.4 MAC uC Read Operation

This operation reads from a specific 2- byte address. The read transaction is divided into two parts. In the first part, the Two-Wire master sends a write command to the slave containing only the required start address. (The address is always 2 bytes long.) In the second part, multiple bytes may be read from consecutive addresses. The MAC puts the appropriate data on the Two-Wire bus and the internal address is automatically incremented. A stop bit is sent by the master only when the entire transaction has been completed.

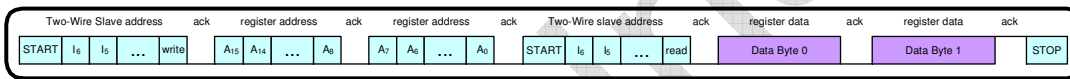


Figure 9: Two-Wire Read Command

3.4.1.5 WHDI Application/MAC Protocol

The WHDI programmer’s reference defines the MAC registers data structure. Each register has an associated group id and index offset address.

The group id and the index offset are each 1 byte long. Together they define a register address that is 2 bytes long.

Each register has an attributed length (in byte units). All registers within the same group have the same length.

A Two-Wire transaction to a specific register includes 2 bytes of register address and the register data bytes. The register is written in one transaction. If the transaction terminates ahead of time or is too long, the MAC issues an error interrupt and does not store the received values. The register is read in one transaction, as described in section 3.4.1.4. If the read transaction finishes ahead of time, the MAC issues an error interrupt.

3.4.2 Interrupts

There is one interrupt connected to the WHDI connector. The interrupt source is the AMN2210 MAC uC. For details about the interrupt, please refer to the programmer’s user guide. . The interrupt active polarity is set in SW or by configuration resistors on board – see 3.4.3.

3.4.3 WHDI Module Configuration

In order to distinguish between boards and by the SW, there is an on board ID that can be read by the STM32F.

Amimon Project Part Number	WHDI_MODULE_ID (Details)								Comments
	Tx="0", Rx="1"		Interrupt Polarity: "0"=falling, "1"=rising		I2C Address: "00"=0x62, "01"=0x72, 10'=0x60, 11"=0x70		MODULE_ID		
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
AMN11310 Rev. 2.0	1	0	0	0	0	0	0	0	
AMN12310 Rev. 2.0	1	0	1	0	0	0	1	0	

3.5 Reset and Wake-up Timer

The AMN11100 has one hard *RESET* input pin connected directly to the AMN2110 and to the STM32F uC, as described in Figure 11. Assertion of the STM32F reset switches the clock of uC to the internal oscillator until the Albatross does not assert an INIT_DONE interrupt. Assertion of the Albatross reset enables the generation of the 10 MHz clock. After a hard reset, the MAC asserts the SW reset signal which just clears the registers without resetting the clock generation scheme.

When the INIT_DONE is asserted, it indicates the completion of the Albatross initialization and that the 10 MHz clock is stable. At that point, the uC switches to the external clock source from the Albatross and enable communication with the application microcontroller.

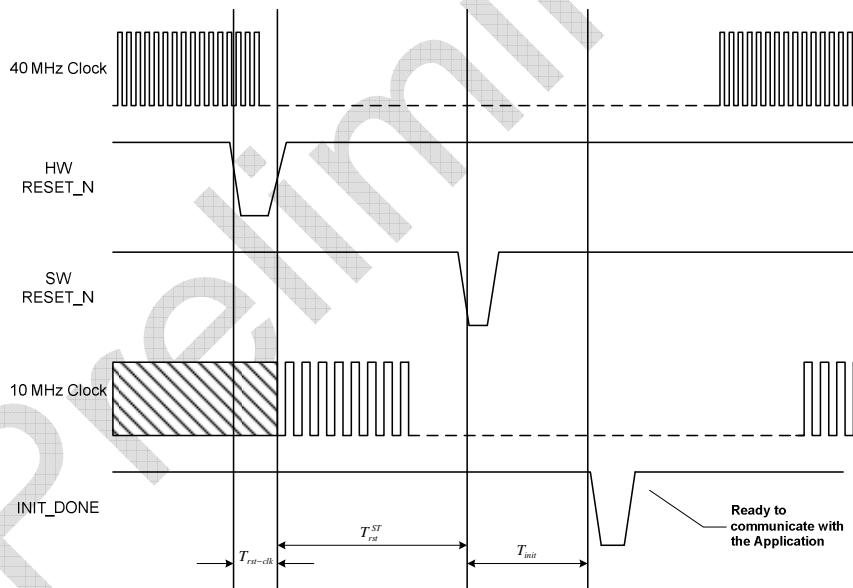


Figure 10: Reset Time Diagram



The following table specifies the timing parameters -

Table 8: Reset Timing Requirements

Symbol	Parameter	Condition	MIN	TYP	MAX	Units
T _{RST-CLK}	Time from assertion of the HW reset until valid clock is generated	40 MHz clock is valid – few us after power up		300		ns
T _{ST,RST}	Time from assertion of the HW reset until the STM32F completes the internal initialization	Power is stable		4.5		ms
T _{INIT}	Time from assertion of the HW/SW reset until the AMN2210 completes the internal initialization			1.7		ms

The following figure specifies the reset schema and related signals -

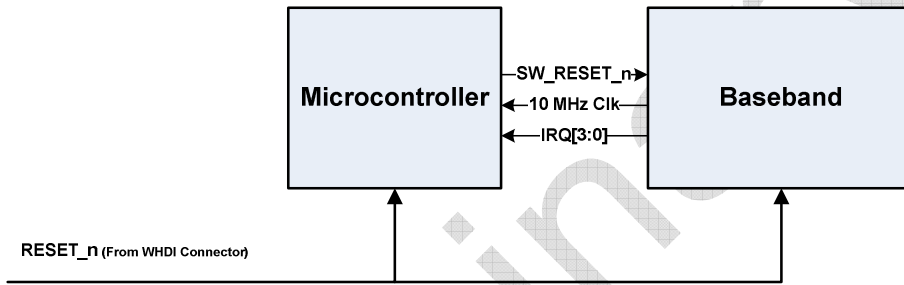


Figure 11: Reset Mechanism

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Chapter 4

WHDI Connector Pins

4.1 Signals

Table 9: WHDI Connector Signals

# of Pins	Pin Name	Description/Functionality	Group	Direction	Remarks
30	D[29:0]	30-bit RGB (10:10:10) or YCrCb (10:10:10)	Video	Out	
1	DCLK	Video data clock	Video	Out	Up to 78.125 MHz
1	DE	Data enable	Video	Out	
1	H_SYNC	Horizontal sync	Video	Out	
1	V_SYNC	Vertical sync	Video	Out	
1	SPDIF	SPDIF audio interface	Audio	Out	
1	SD	I ² S audio interface Serial Data signals	Audio	Out	
1	SCLK	I ² S continuous serial clock	Audio	Out	Up to 3.072Mbps
1	WS(LRCLK)	I ² S Word Select (Left/right clock) which defines also the sampling rate	Audio	Out	
1	MCLK	I ² S master clock coherent to WS according to specified ratio	Audio	Out	Rate is adjustable on RX side
1	SDA	Two-wire Serial Bus Data (Slave Mode)	Control	I/O	Control I/F for WHDI
1	SCL	Two-wire Serial Bus Clock (Slave Mode)	Control	In	Control I/F for WHDI
1	INT	Interrupt from WHDI module	Control	Out	
1	\overline{RESET}	Reset / Power-down line	Control	In	
1	MUTE (TBD6)	MUTE signal	Audio	Out	Signals audio error and can be used by the next audio device down the line to mute the audio when errors occur
2	TBD[5:4]	TBD4, TBD5, are reserved in, AMN12310 as an option for RS232 connection to STM32F UART2.	TBD	TBD	
8	3.3V	VCC	Power	Power	300 mA maximum rating per pin
17	GND	Ground	Power	Power	



4.2 Connector Schematics

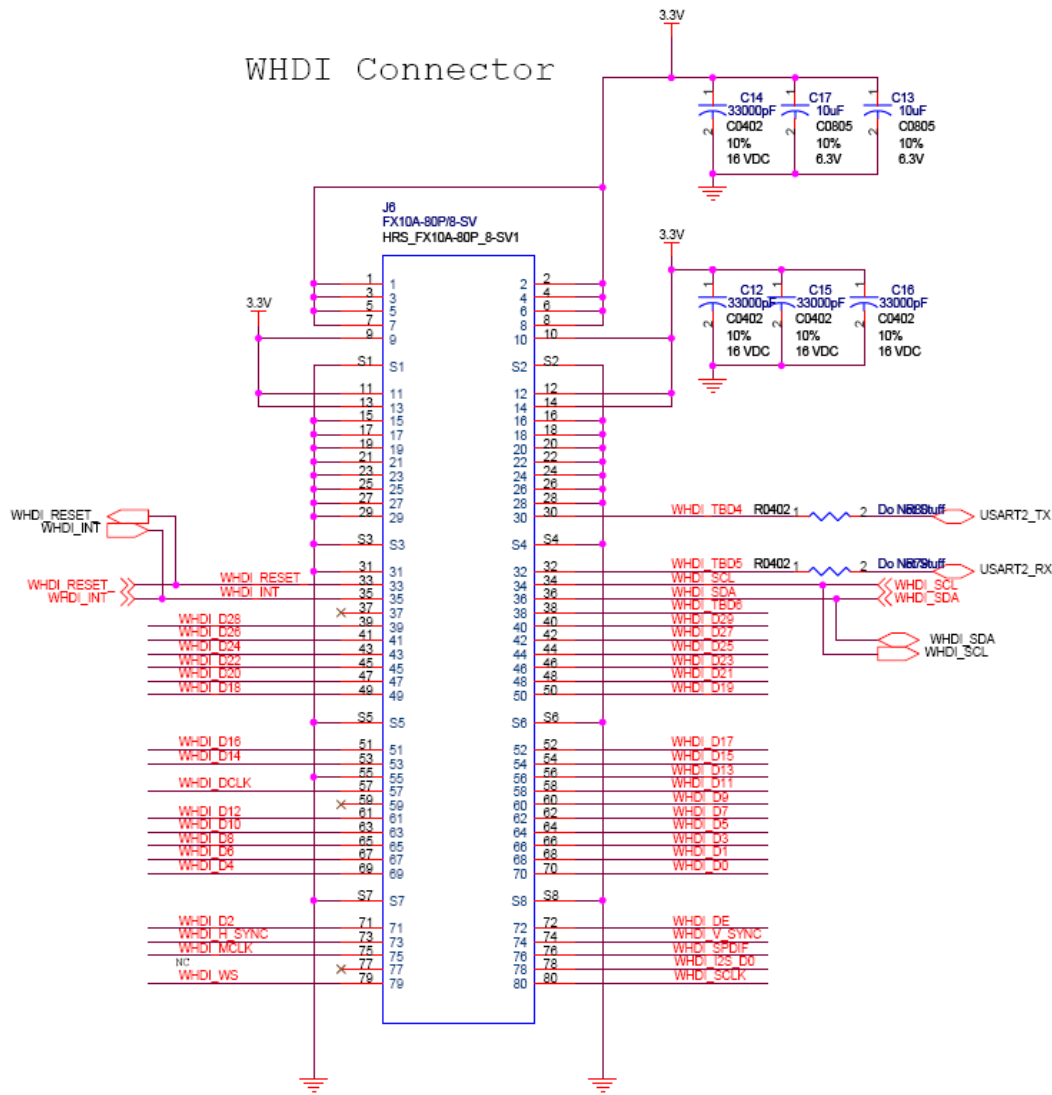


Figure 12: WHDI Connector

4.3 Pin List

Table 10: Rx WHDI Connector Pin List

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	3.3V	2	3.3V	41	WHDI_D26	42	WHDI_D27
3	3.3V	4	3.3V	43	WHDI_D24	44	WHDI_D25
5	3.3V	6	3.3V	45	WHDI_D22	46	WHDI_D23
7	3.3V	8	3.3V	47	WHDI_D20	48	WHDI_D21
9	3.3V	10	3.3V	49	WHDI_D18	50	WHDI_D19
11	3.3V	12	3.3V	51	WHDI_D16	52	WHDI_D17
13	3.3V	14	3.3V	53	WHDI_D14	54	WHDI_D15
15	GND	16	GND	55	GND	56	WHDI_D13
17	GND	18	GND	57	WHDI_DCLK	58	WHDI_D11
19	GND	20	GND	59	NC	60	WHDI_D9
21	GND	22	GND	61	WHDI_D12	62	WHDI_D7
23	GND	24	GND	63	WHDI_D10	64	WHDI_D5
25	GND	26	GND	65	WHDI_D8	66	WHDI_D3
27	GND	28	GND	67	WHDI_D6	68	WHDI_D1
29	GND	30	WHDI_TBD4	69	WHDI_D4	70	WHDI_D0
31	GND	32	WHDI_TBD5	71	WHDI_D2	72	WHDI_DE
33	WHD_RESET_	34	WHDI_SCL	73	WHDI_H_SYNC	74	WHDI_V_SYNC
35	WHDI_INT	36	WHDI_SDA	75	WHDI_MCLK	76	WHDI_SPDIF
37	NC	38	MUTE (TBD6)	77	NC	78	WHDI_I2S_D0
39	WHDI_D28	40	WHDI_D29	79	WHDI_LRCLK	80	WHDI_SCLK

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Chapter 5

Electrical Specifications

5.1 Operating Conditions and Electrical Characteristics

The following tables describe the operating conditions and electrical characteristics required for working with the AMN12310.

Table 11: Absolute Maximum Ratings over Operating Case Temperature Range

Supply input-voltage range, V_I	0 to 3.6 V
Ambient temperature range	0°C to 70°C
Storage temperature range, T_{stg}	-40°C to 125°C

Table 12: Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Unit
DV_{DD}	Module supply voltage	3.15	3.3	3.45	V
V_{SS}	Supply ground	0			V
V_{IH}	High-level input voltage	0.7 DV_{DD}			V
V_{IL}	Low-level input voltage			0.3 DV_{DD}	V
V_{OH}	High-level output voltage ($DV_{DD} = \text{MIN}$, $I_{OH} = \text{MAX}$)	0.8 DV_{DD}			V
V_{OL}	Low-level output voltage ($DV_{DD} = \text{MIN}$, $I_{OL} = \text{MAX}$)			0.22 DV_{DD}	V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
T_a	Operating ambient temperature	0		70	°C

Table 13: Electrical Characteristics over Recommended Range of Supply Voltage and Operating Conditions

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_I	Input current	$V_I = V_{SS}$ to DV_{DD}			±20	μA
I_{OZ}	Off-state output current	$V_O = DV_{DD}$ or 0 V			±20	μA
I_{DVDD}	Module supply	$DV_{DD} = \text{Max.}$, Video Clock = 74.25 MHz, with activity on all I/O terminals			1500	mA
C_i	Input capacitance				10	pF
C_o	Output capacitance				10	pF



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Chapter 6

Design Guidelines

6.1 Digital Layout Recommendation

To better understand the layout guidelines, please refer to the AMN12310 Schematics which are part of the HDK package.

6.1.1 Stack Up

Recommended stack up for six layers design:

- Total thickness: 1.15mm
- Tolerance thickness: 10%

Table 14: Digital Layout Recommendation

Lay. No.	Layer Name	Layer Stack-up	Unit	Control Impedance/Notes
1	Component side (CS)	1-1.5	oz	1) Trace Width -14mil, Separation -12 mil (to ground plane) - 50 OHM COPLANAR. 2) Trace Width - 5.5 mil, Separation between differential lines – 5.5 mil, differential impedance - 103 OHM. 3) Trace Width – 5 mil, Separation between differential lines – 6 mil, differential impedance - 107 OHM.
	Space	8.6	mil	
2	Ground	2	oz	
	Space	4	mil	
3	Ground	2	oz	
	Space	4	mil	
4	Power / Ground	2	oz	
	Space	4	mil	
5	Ground	2	oz	
	Space	8.6	mil	
6	Print Side (PS)	1-1.5	oz	Trace Width - 5mil, Separation between differential lines – 6 mil, differential impedance - 107 OHM.
Board Thickness				1.15 MM +/- 10%
Material				FR4 HITG



6.1.2 General Guidelines

- Keep traces as short as possible.
- Traces should be routed over full solid reference planes.
- Sensitive lines like reset and clocks should be routed with special care.
 - These lines should be routed over full solid power planes (ground or power).
 - Traces should be routed at least two times the trace width away from other lines in the same routing layer.
 - Place a series resistor ~30 ohm at the clock source.
- Keep digital signals away from the analog side.

6.1.3 WHDI Lines

- Place series resistors on all output lines (near the outputs pins).
- Series resistors on input lines are unnecessary. (The series resistors should be placed on the interface board.)

6.1.4 Power and Ground

- Use a solid ground plane.
- Ground planes separation is unnecessary.
- Place decoupling capacitors near power pins. (Refer to the schematics and BOM for recommended values.)
- Analog power pins should be filtered with ferrite beads. (Refer to the schematics and BOM for recommended values.)
- Add as many ground vias as possible, for better ground connections between layers and better heat dissipation.

6.2 RF Design Recommendation

6.2.1 RF Components

All passive components must have compatible performance with components used in the Amimon reference design.

6.2.2 Power Management

The RF power rail 3.3V_RAIL is separated from the digital power rail 3.3 with ferrite bead.

6.3 Test Points and Jumpers

Reference Name	Type	Functionality	Reference Name	Type	Functionality
TP1	SMD	RXHP_3	TP28	TH	3.3V
TP2	SMD	RXHP_4	TP29	SMD	3.3V
TP3	SMD	RFSPi_CLK	TP30	SMD	MAC_TRST
TP4	SMD	RFSPi_DOUT	TP31	SMD	MAC_TDI
TP5	SMD	RSSI_DETECT	TP32	SMD	MAC_TCK
TP6	SMD	LD	TP33	SMD	GND
TP7	SMD	SPI_CS	TP34	SMD	GND
TP8	TH	GND	TP35	SMD	3.3V
TP9	SMD	CLK40M	TP36	SMD	ALBATROSS_TDO
TP10	TH	GND	TP37	SMD	GND
TP11	SMD	GND	TP38	SMD	3.3V
TP12	SMD	GND	TP39	SMD	3.3V
TP13	TH	GND	TP40	SMD	HW_ID_0
TP14	SMD	GND	TP41	SMD	HW_ID_1
TP15	SMD	3.3V	J1	SMD	RF- UFL CON
TP16	SMD	GND	J2	SMD	RF- UFL CON
TP17	TH	1.2V	J3	SMD	RF- UFL CON
TP18	SMD	RXHP_1	J4	SMD	RF- UFL CON
TP19	SMD	RXHP_0	J5	SMD	RF- UFL CON
TP20	SMD	UC_MAC_CLK	J6 -CONNECTOR	SMD	WHDI_CON
TP21	TH	GND	J7 -CONNECTOR	SMD	UC JTAG
TP22	SMD	GND	JP1 pin 1-2	JUMPER	MAC_TXD
TP23	SMD	3.3V	JP1 pin 2-3	JUMPER	ALB_TXD
TP24	SMD	3.3V	JP2 pin 1-2	JUMPER	MAC_RXD
TP25	SMD	MAC_RST	JP2 pin 2-3	JUMPER	ALB_RXD
TP26	SMD	MAC_TMS	JP3	JUMPER	BOOT0
TP27	SMD	3.3V	SW1	SWITCH	RF_TEST_SW

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Chapter 7

Mechanical Dimensions

The following shows the mechanical dimensions for the AMN12310:

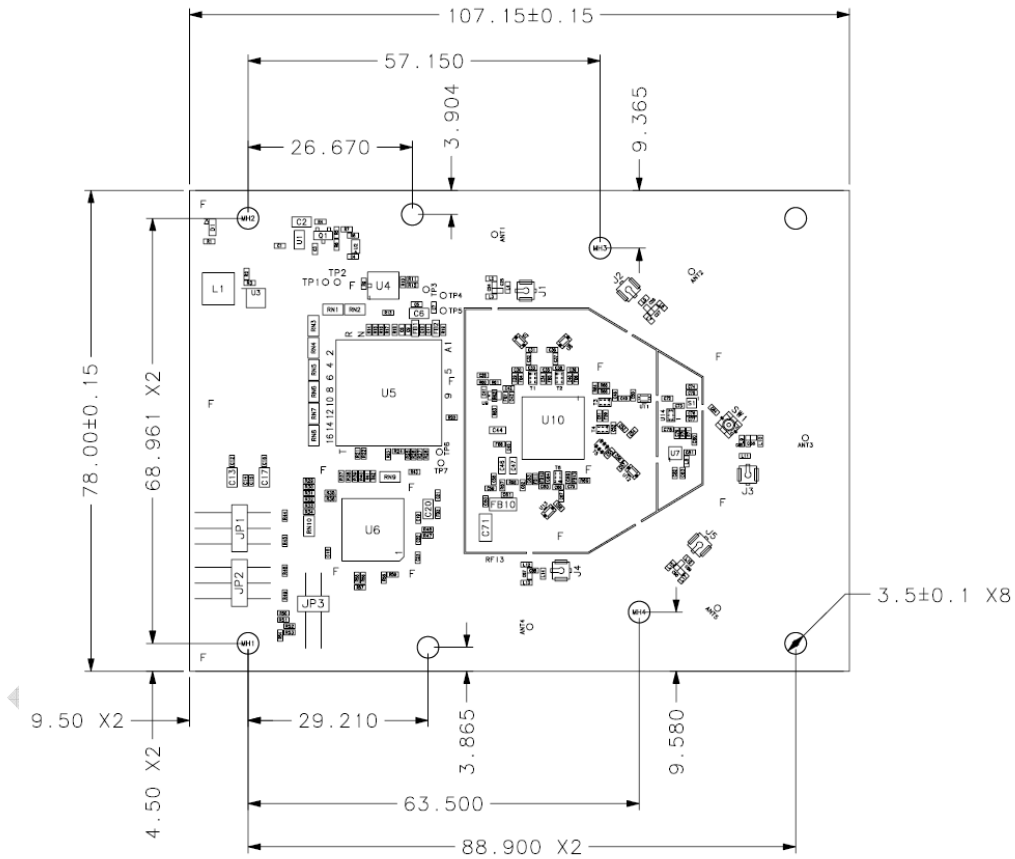


Figure 13: Mechanical Dimensions Top View



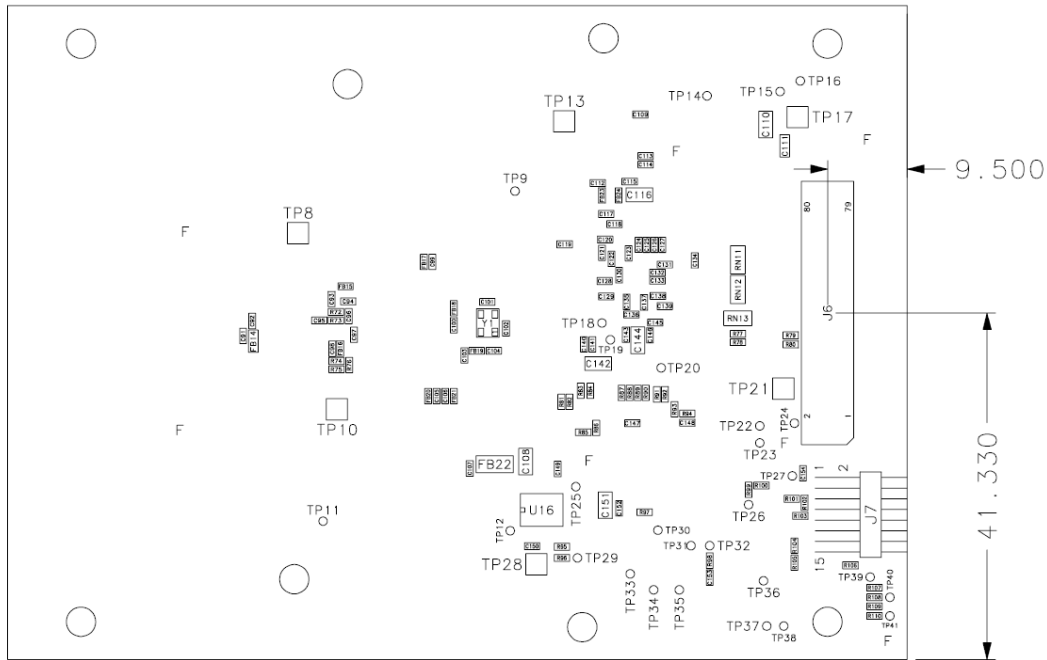


Figure 14: Mechanical Dimensions Bottom View

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7.1 RF Shield frame and cover

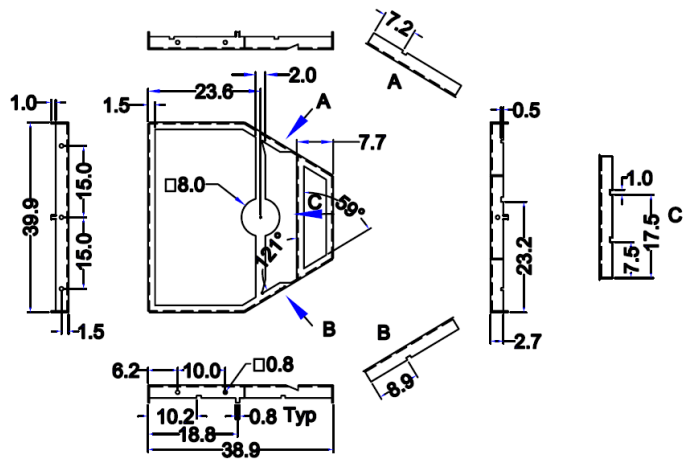


Figure 15: RF-Shield Frame

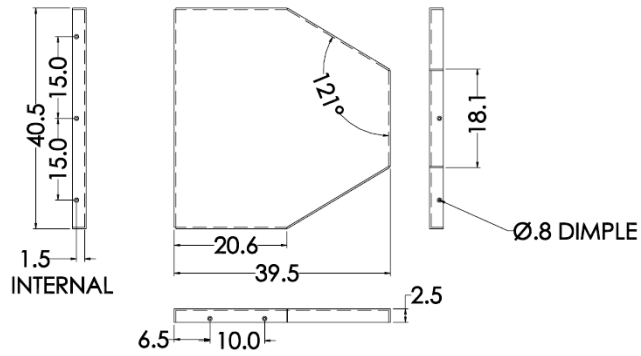


Figure 16: RF-Shield Cover

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