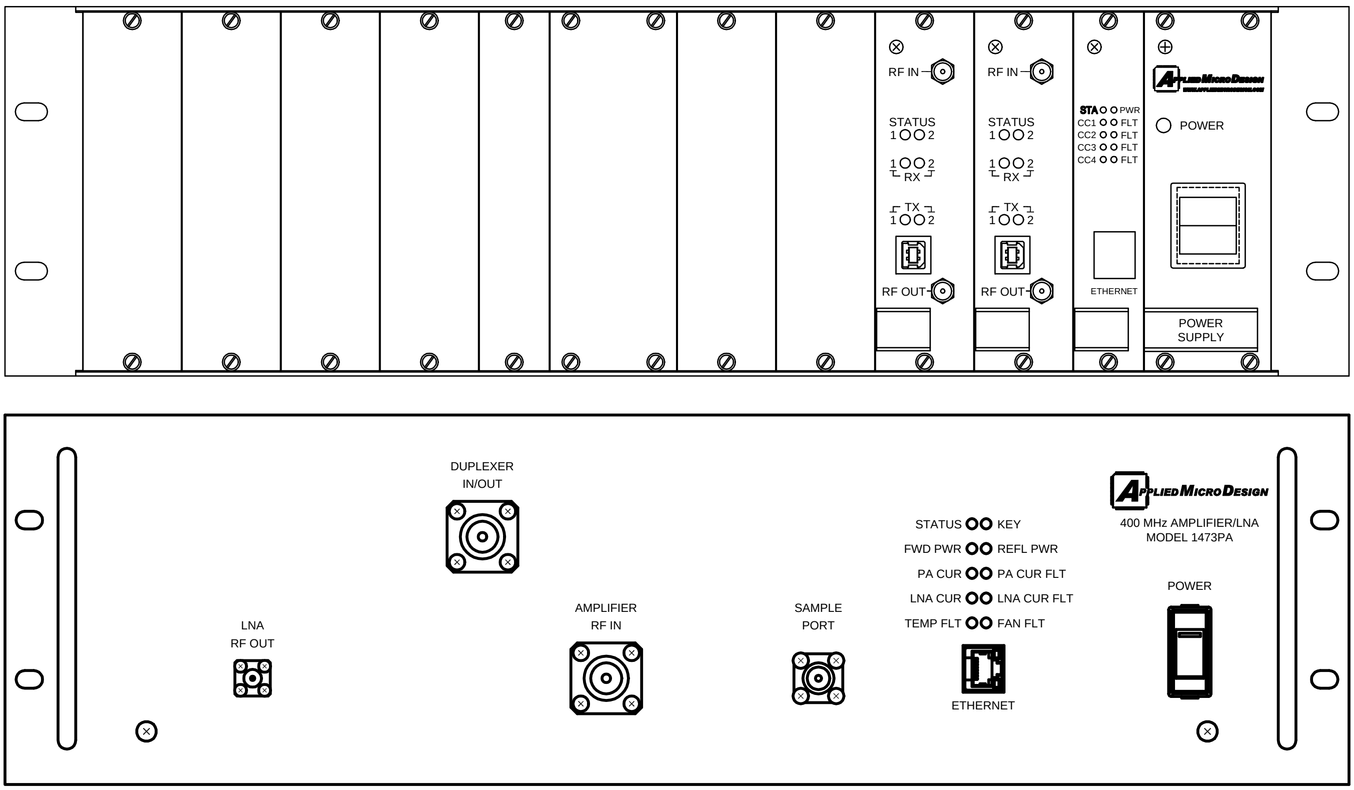
Montclair State University

MSU Head End System

Channelized Bi-Directional Amplifer

User’s Manual

rev 2



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Notes, Cautions, and Warnings

This is a Class B Booster.

Part 90 (Class B) Signal Boosters
WARNING. This is **NOT** a **CONSUMER** device. It is designed for installation by **FCC LICENSEES** and **QUALIFIED INSTALLERS**. You **MUST** have an **FCC LICENSE** or express consent of an FCC Licensee to operate this device. You **MUST** register Class B signal boosters (as defined in 47 CFR 90.219) online at **www.fcc.gov/signal-booster/registration**. Unauthorized use may result in significant forfeiture penalties, including penalties in excess of $100,000 for each continuing violation.

⚠ **Invisible laser light is used on these equipment.**

DO NOT look directly into the fiber optic connectors when unit is in operation.

Connect RF Output to existing Distributed Antenna System (DAS) cable only.

DO NOT operate equipment with unauthorized antennas, cables, and/or coupling devices.

DO NOT operate equipment unless all RF connectors are secure.

DO NOT operate equipment unless it has been installed and inspected by a qualified radio technician.

Contact Information

For more information contact the FCC at:

https://signalboosters.fcc.gov/signal-boosters/

F.2 PART 90 CLASS B SIGNAL BOOSTERS Licensees and signal booster operators are required to register existing Class B signal booster installations with the FCC by November 1, 2014. After November 1, 2014, operation of an existing, unregistered Class B signal booster will be unauthorized and subject to enforcement action. Any new Class B signal booster installed after November 1, 2014 must be registered prior to operation. To encourage compliance with this new requirement, registration will be free of cost to the operator and/or licensee.[R11], [R9]

FCC Part 90 Class B Signal Booster Registration & Discovery website:

https://signalboosters.fcc.gov/signal-boosters/

Description

There are two major elements to the MSU system; the Head End (HE) hardware and the Remote Hardware. There is one HE and multiple remotes.

Each Remote consists of a single Fiber-Fed Power Amplifier chassis. The Remote chassis contains a Down Link Power Amplifier, and Up Link LNA, and a Fiber Optic Transmitter and Receiver.

The Head End consists of a Fiber-Fed Power Amplifier (FFPA) chassis, a DSP Chassis, and Fiber Optic Chassis. The FFPA chassis contains an Up Link Power Amplifier, a Down Link LNA, and a Duplexer. The DSP Chassis contains one each Uplink and Down Link DSP filter cards. The Fiber Optic Chassis contains a FO Transmitter and FO Receiver for each Remote

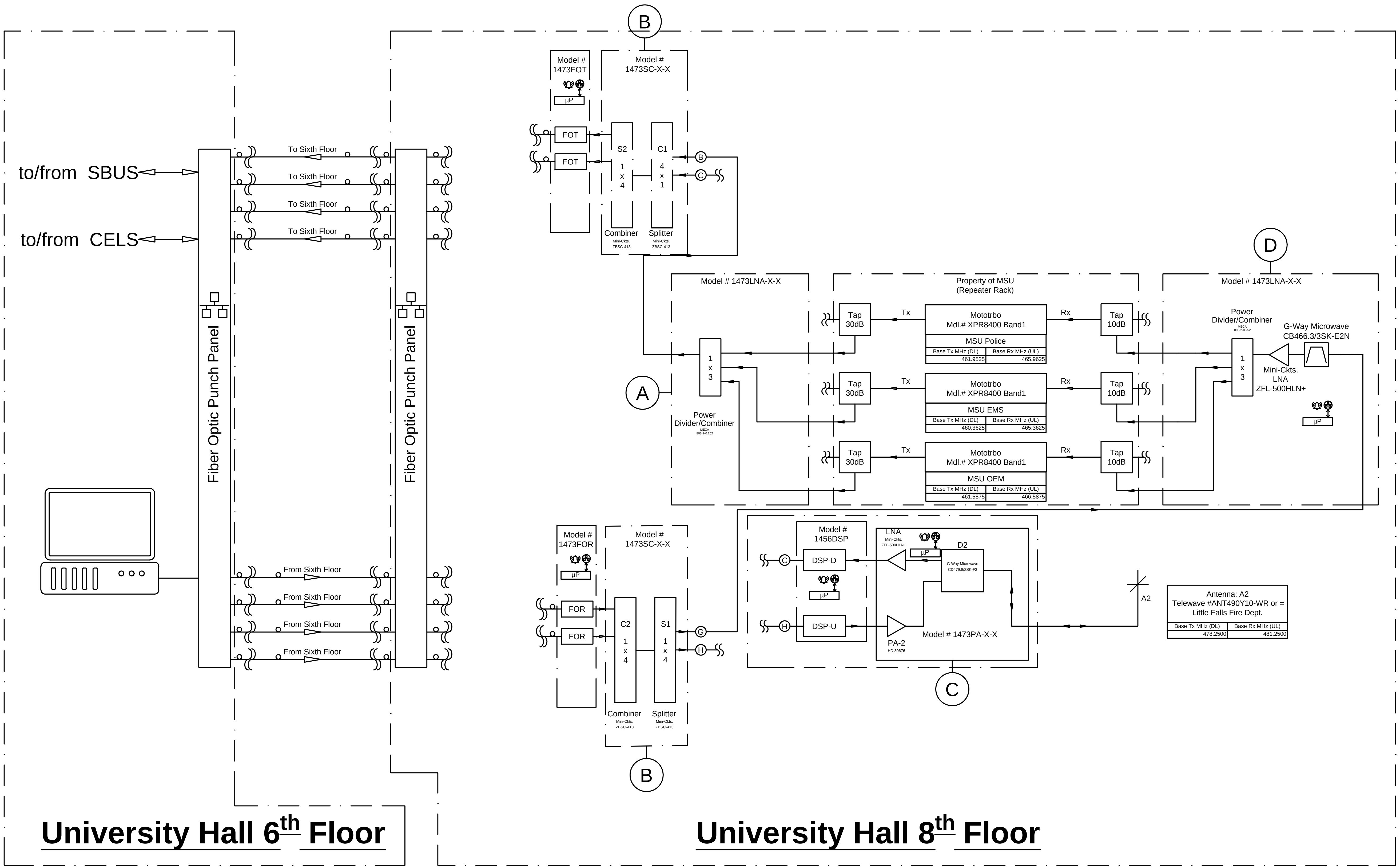
In the Uplink (UL) path, signals from portable radios are input to the Remote DAS. These signals are amplified in a Low Noise Amplifier (LNA) and converted to light by a Fiber Optic Transmitter in the Remote chassis, and transmitted to the Head End via fiber optic cable. In the Head End rack, the light from the fiber optic cable is converted back to RF by a Fiber Optic Receiver; the RF is filtered in the UL DSP Card and the filtered signal is input to the power amplifier module. The amplified RF is fed to the outside antenna via a duplexer.

In the Downlink (DL) path, signals from user radios (Motorola radios that are FCC certified) are input to the Head End LNA. These signals are filtered in the DL DSP Card, combined with signals from a Motorobo repeater, converted to light by a HE Fiber Optic Transmitter, and transmitted to the FFPA via fiber optic cable. In the Remote chassis, the light from the fiber optic cable is converted back to RF by a Fiber Optic Receiver, and the RF is input to a power amplifier module. The amplified RF is input to a bandpass filter; the filtered RF feeds the Distributed Antenna System (DAS) in the building where the remote hardware is located.

A Sample Port on the front panel of the FFPA allows the user to sample the signal without interrupting main line communications. The Sample Port is 40 dB below the main RF output port.

The FFPA has a processor board that monitors overall chassis operation. The processor board controls the enable signal to the amplifier and monitors forward power, reverse power, current, fan status and heat sink temperature. Forward and reverse power are derived from directional couplers built into the amplifier modules.
Heat sink temperature is derived from a thermistor mounted onto the heat sink and amplifier current from a sense resistor in series with the +28-volt power input. The fan has a built-in stopped rotor line which is input to the processor board.

The processor board features optional remote monitoring capability via Ethernet. The Graphical User Interface (GUI) of the Network Management System (NMS) computer can display the status of the amplifier and provide control.



CELL GAIN

68 WHITE STREET #265 RED BANK, NJ

732-889-4671

Revisions			
Date	Drawn By	Revision Notes	Aprvd. By
2/19	MTJ	Removed FOT/R from MSU line.	
		Added rack demarcations.	
		Added freq. tables at antennas.	
		Notated MSU ownership of repeaters.	
3/2	MTJ	Added 8th to 6th connection diagram	
3/5	MTJ	Integrated AMDi Design Changes	
3/15	MTJ	Removed EMR unit and CD 481 unit. Added CD479.8/2SK-F3 LNA&PA unit	
5/03	MTJ	Added Tap data to MSU Radio	

Site Name/Address:

MSU

Project:

University Hall Block Diagram

Scale: N/A

Sheet Size: D

Sheet #: 1 of 1

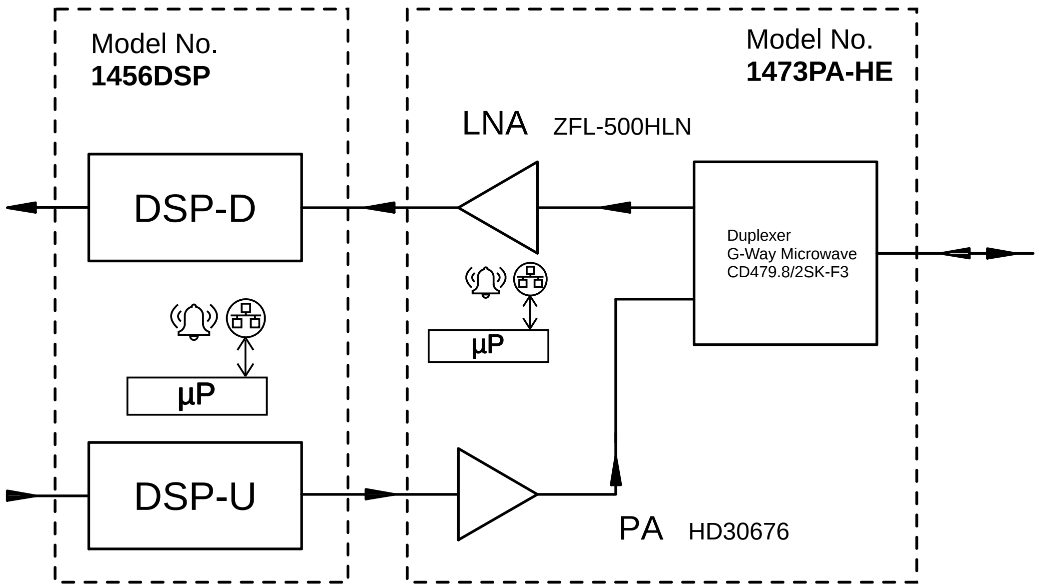
Date: 02/15/2016

Drawn By: Matt Jacobs

Drawing #: MSUHEBD001 rev.4

DOWNLINK

478.2500 MHz



UPLINK

481.2500 MHz

1473PA-HE and 1456DSP Block Diagram

System Specification

Specifications - PA/LNA

Uplink

Frequency:	481.2500 MHz
Type:	Class AB
Bandwidth:	18 MHz
Gain:	40 dB
N.F.:	7 dB
Max. Power Output:	20 dBm
ALC:	30 dBm
Harmonics:	> 60 dBc, 2nd and 3rd
OIP3:	+55 dBm
Impedance:	50 Ohms
Load VSWR:	Infinite, no damage

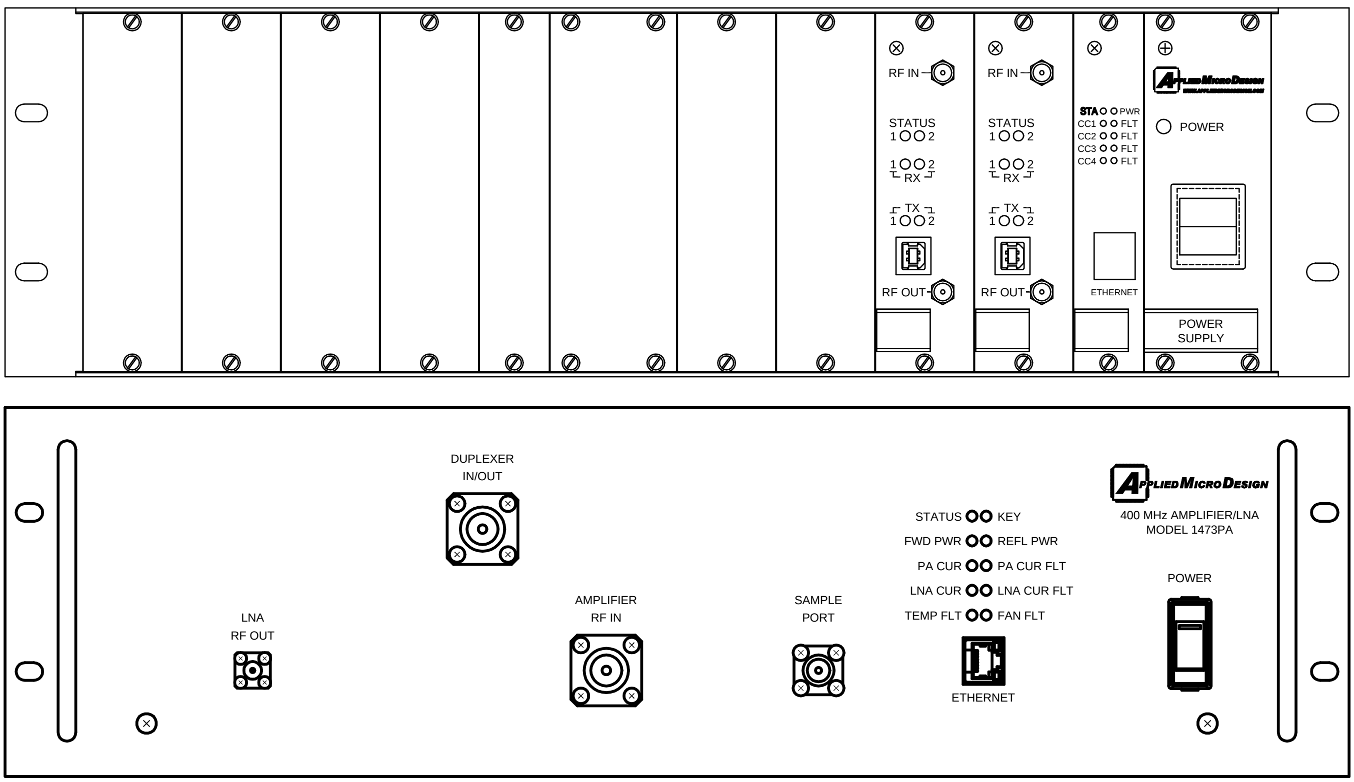
Downlink:

Frequency:	478.2500 MHz
Type:	Linear
Bandwidth:	16 MHz
Gain:	19 dB
NF:	4 dB
Impedance:	50 Ohms
Input Level:	-90 dBm to -10 dBm

Power Supply:	115 V AC
Current:	< 2A
Operating Temp:	-30° to +60° C
Size:	19” x 5.22” x 16”

* With fiber link gain of zero

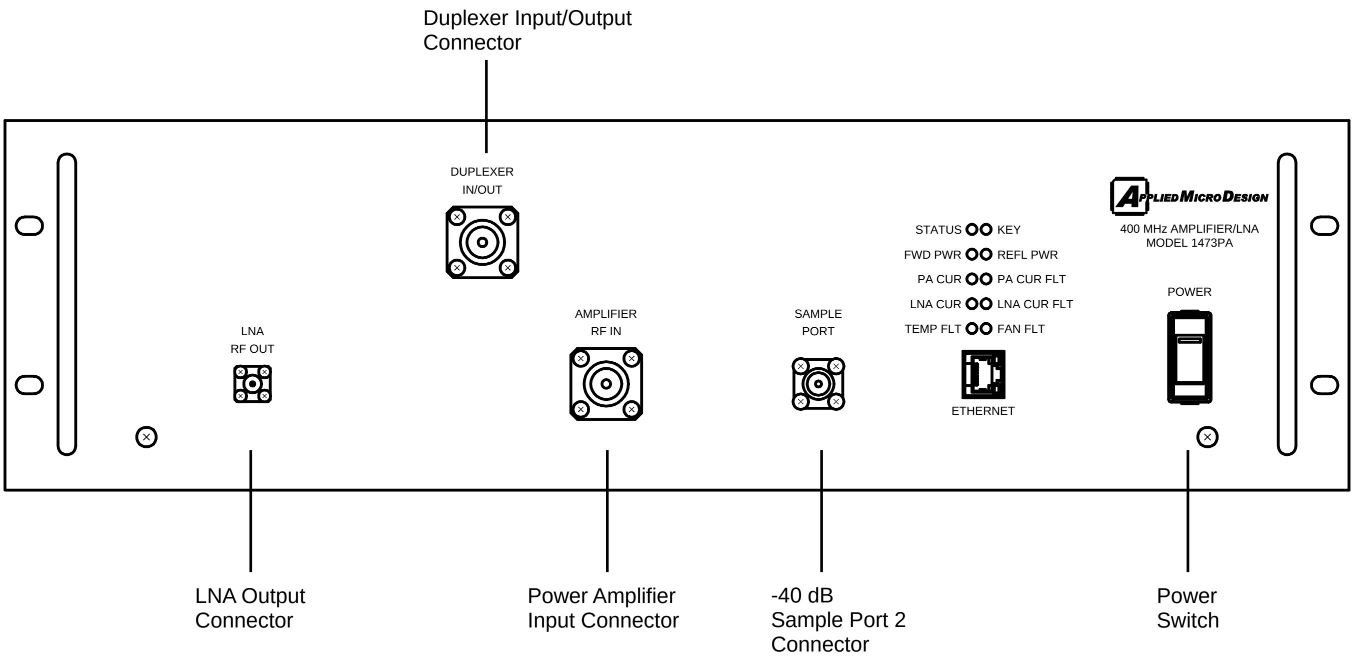
Features



- power amplifier automatic level control (ALC)
- high power amplifier gain
- high power amplifier Third-Order Intercept Point (OIP3)
- sample port at 40 dBc
- channelized DSP filtering
- signal automatic gain control (AGC) via DSP

Head End PA/LNA - Front Panel and Indicators

Model No. 1473PA-HE



steady: amplifer/LNA is operating

STATUS ● ● KEY

steady: amplifier is enabled

FWD PWR ● ● REFL PWR

PA CUR FLT ● ● LNA CUR FLT

FOT FLT ● ● FOR FLT

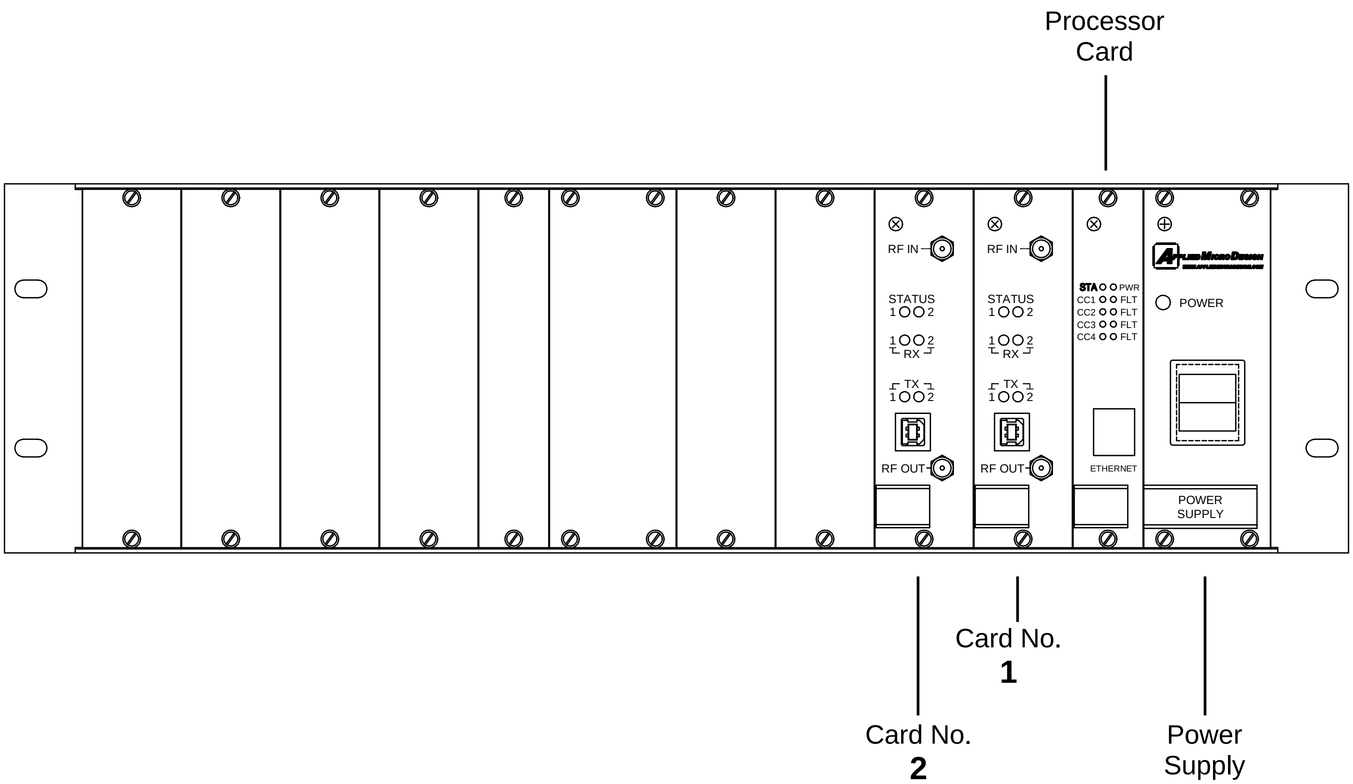
TEMP FLT ● ● FAN FLT

steady: amplifier or LNA is operating normally

steady: amplifier or LNA has either current, reverse power or temperature fault

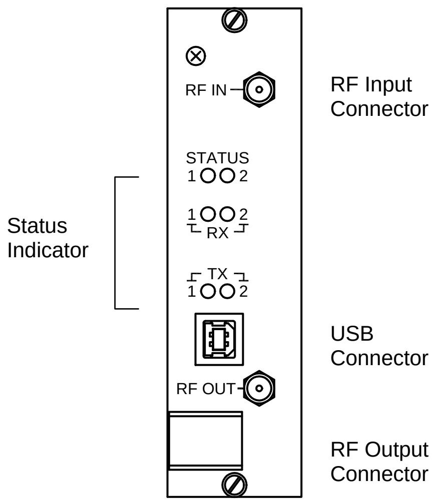
DSP - Front Panel

Model No. 1456DSP

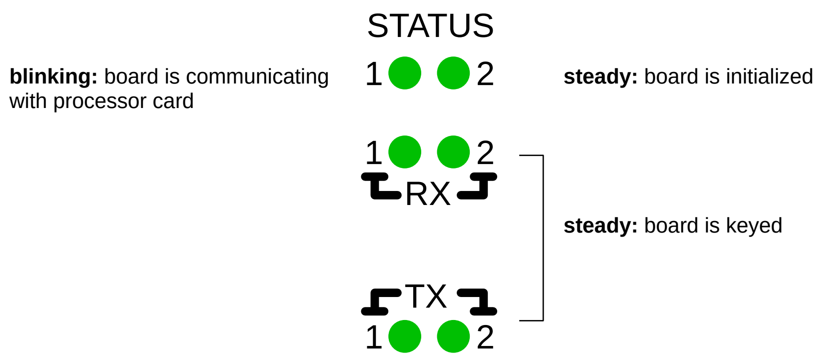


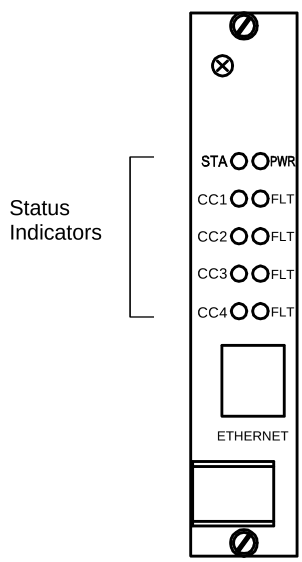
DSP - Indicators

Model No. 1456DSP



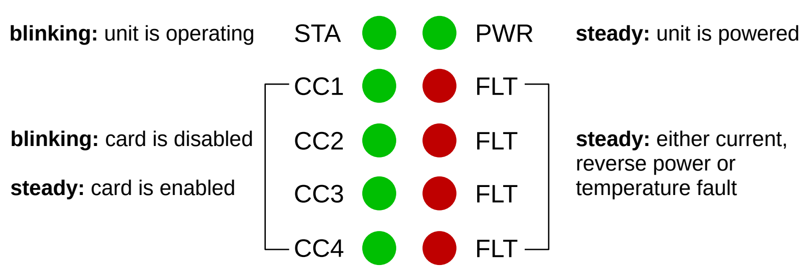
DSP Card





Processor Card

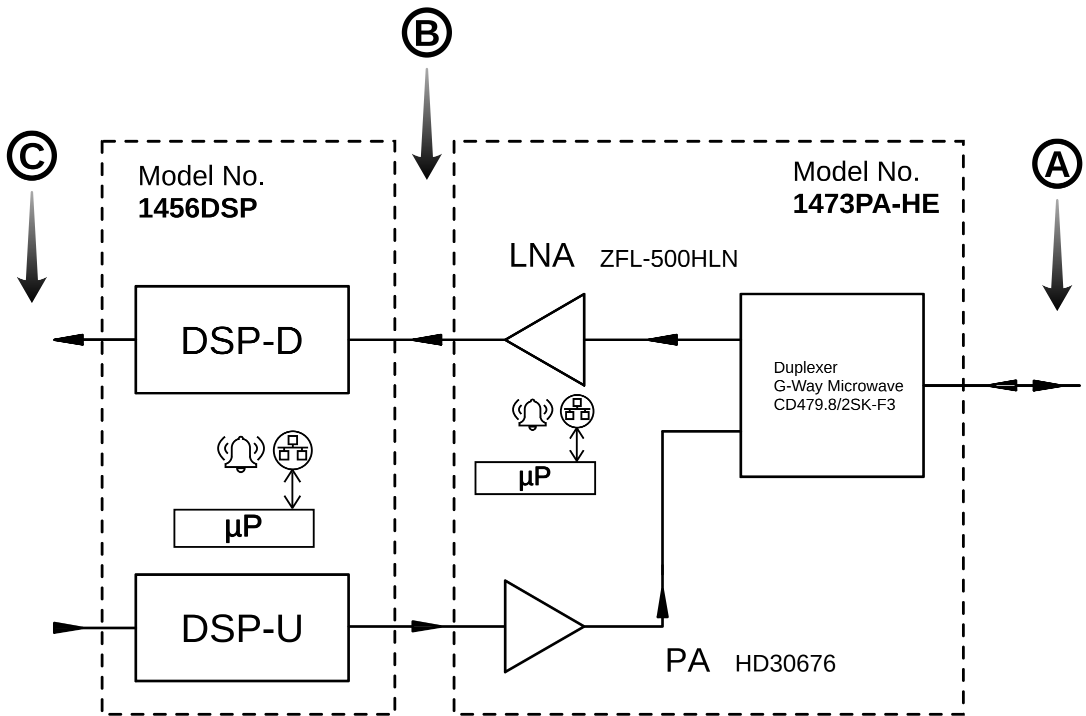
L.E.D. columns blink alternately until processor card establishes communication with DSP cards.



Downlink

The Downlink chain of the Head End consists of a Duplexer, a Low-Noise Amplifier (LNA) and a digital signal processor (DSP) card. The RF signal is applied to “ A “ shown below at the Duplexer Input/Output port.

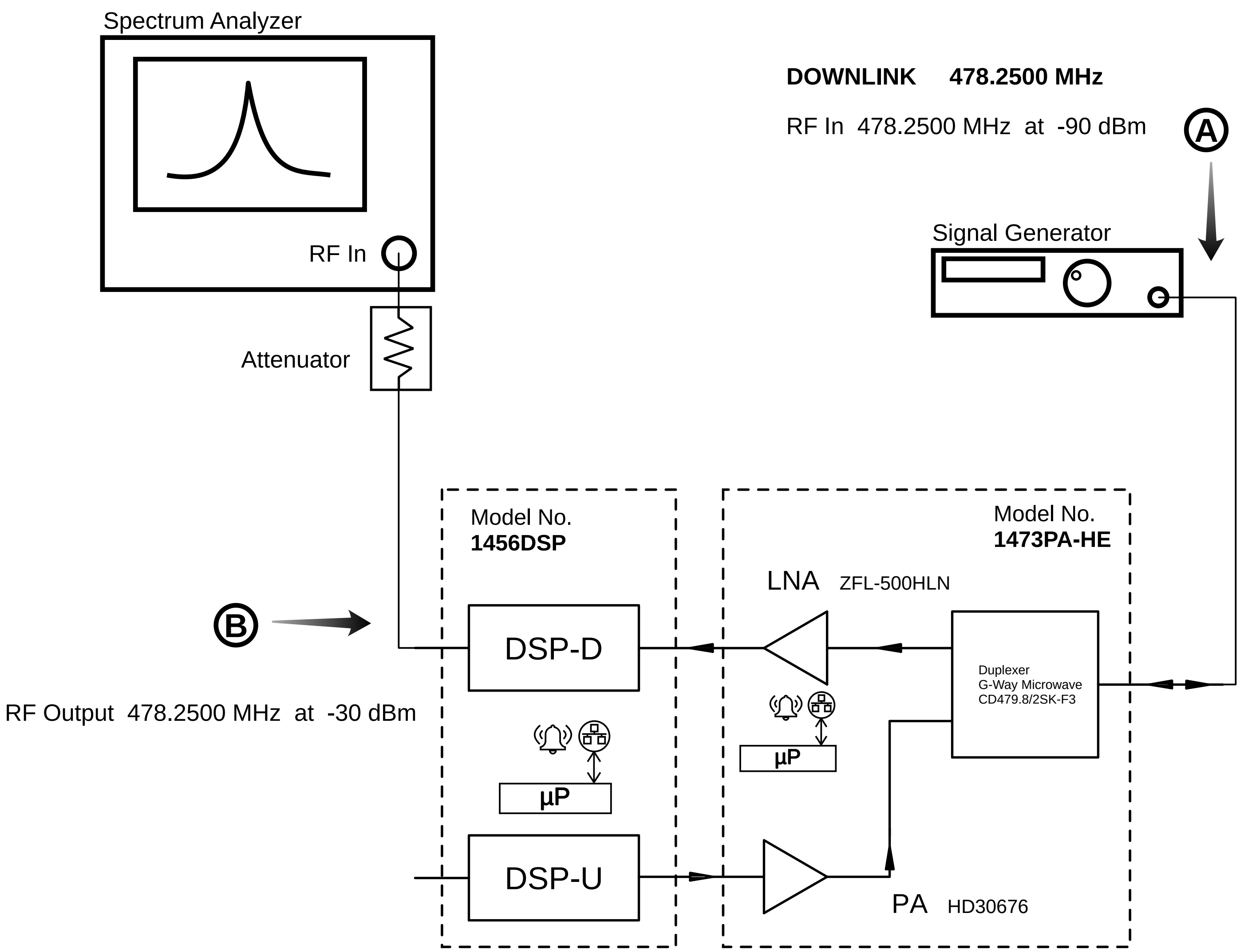
The Duplexer separates the Downlink signals from the Uplink signals. The Downlink port of the Duplexer is connected to the input of the LNA. The RF signal is amplified by the LNA and comes out at a higher level at “ B. “ The RF signal from the LNA is fed into the DSP card for filtering and level adjustment to ensure the signal level is always constant at “ C. “



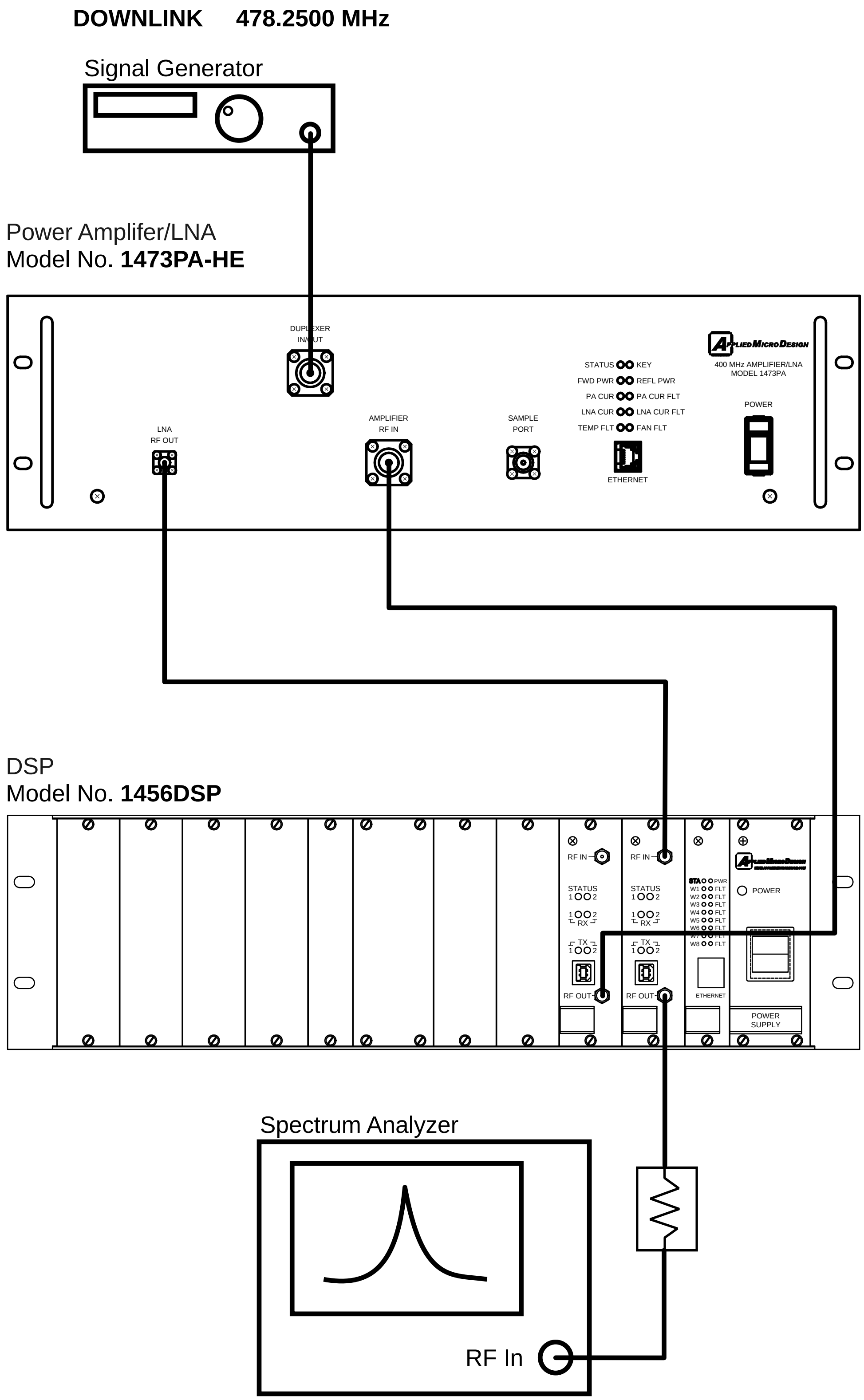
Downlink Test

Shown below is a test set-up of the Downlink chain of the Head End. The signal generator is set for 478.2500 MHz with a level of -90 dBm. The signal generator output is applied to the Duplexer Input/Output port of the 1473PA-HE at " A. "

The RF Output of the DSP is connected to a spectrum analyzer. The expected signal level at " B " is around -30 dBm.



Downlink Test Set-Up



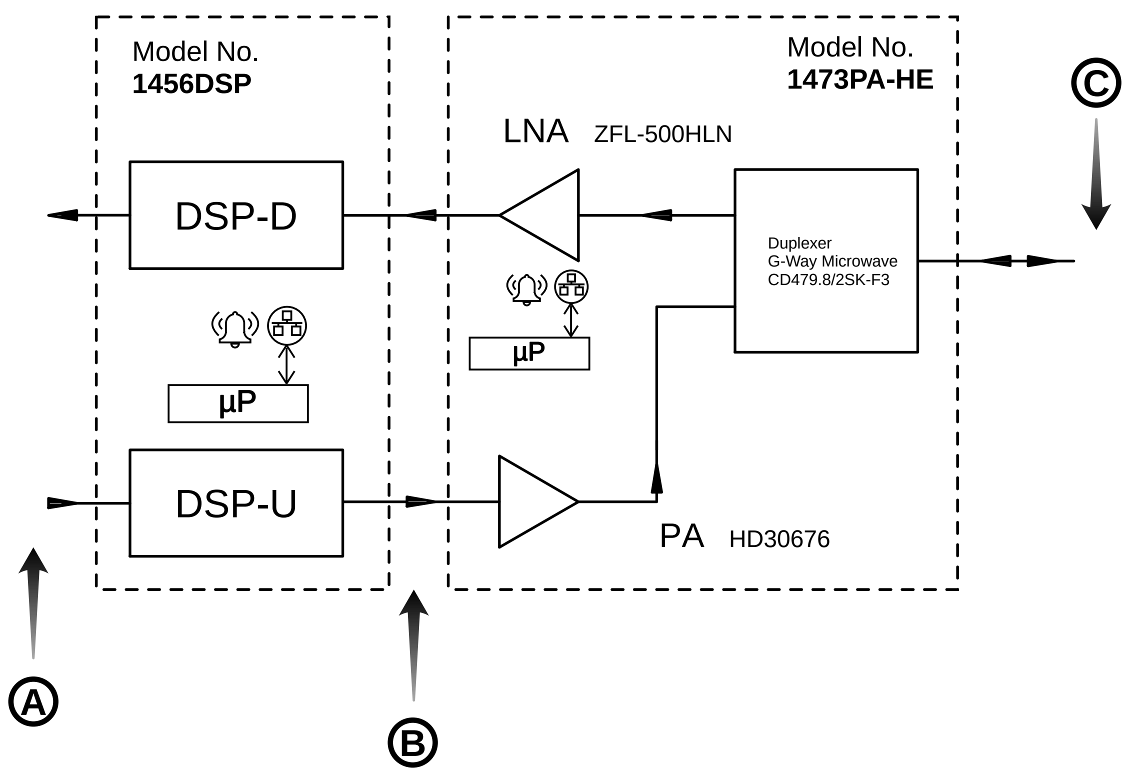
Uplink

The Uplink chain of the Head End consists of a digital signal processor (DSP) card, a Low-Noise Amplifier (LNA) and a Duplexer. The RF signal is applied to " A " shown below at the DSP RF In port.

The RF signal is fed into the DSP card for filtering and level adjustment to ensure the signal level is always constant at " B. " The signal goes into the power amplifier and is fed into the Uplink port of the Duplexer. The Duplexer separates the Downlink signals from the Uplink signals. The signal comes out at " C. "

The amplifier has an Automatic Level Control (ALC) feature. This feature limits the power amplifier output in case the input to the amplifier exceeds the required level.

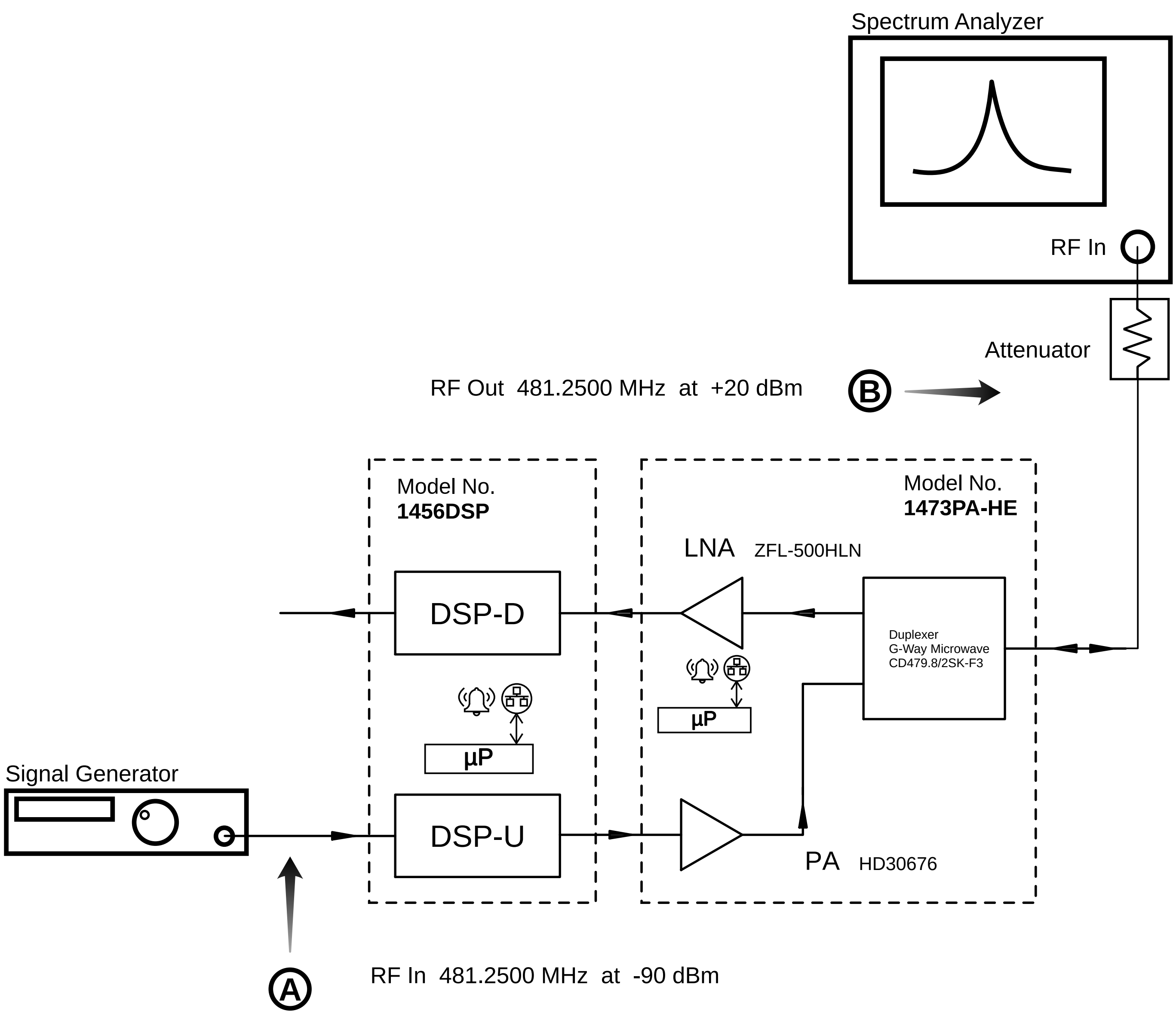
The power amplifier ALC level is set to +30 dBm.



Uplink Test

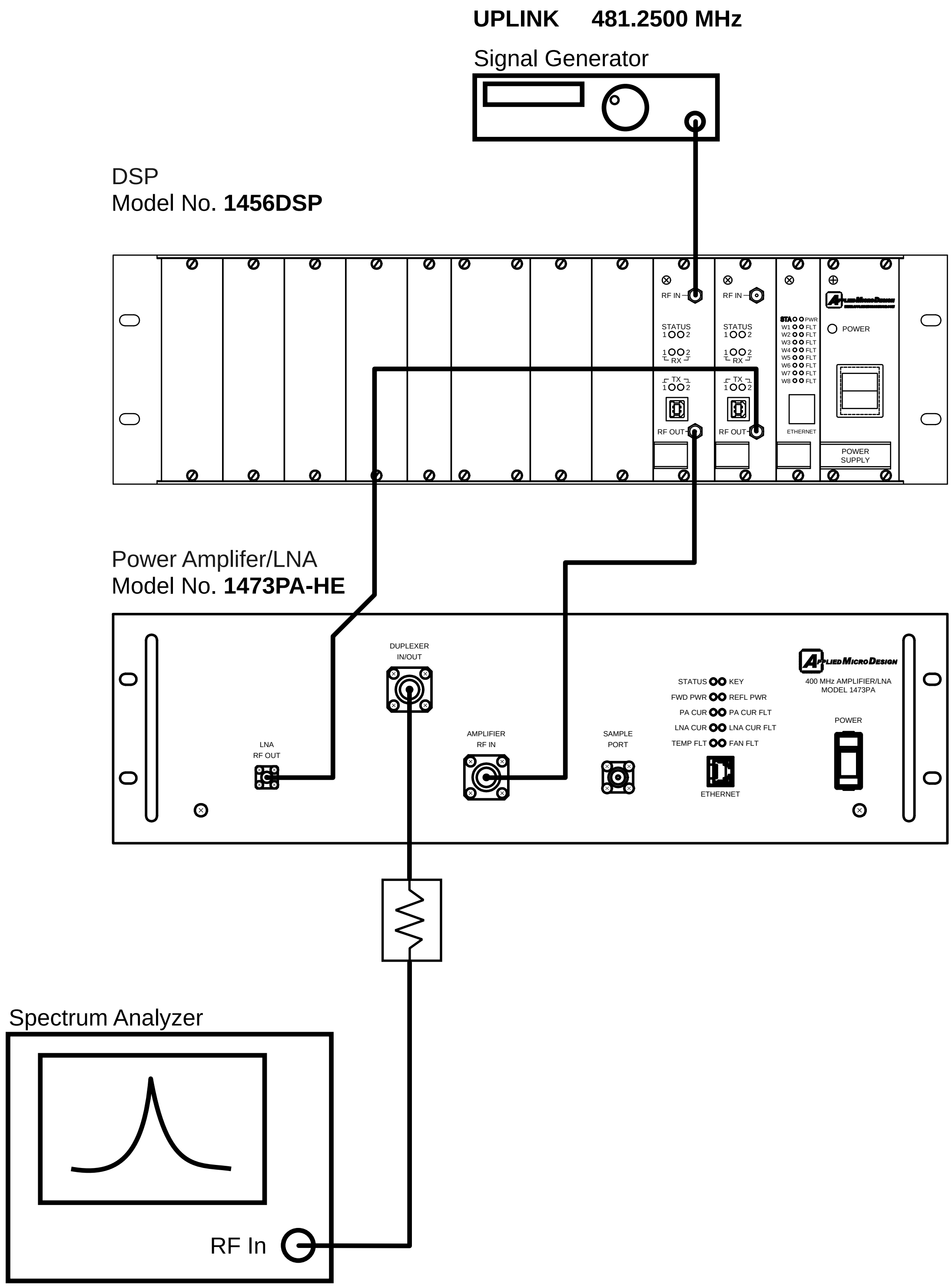
Shown below is a test set-up of the Uplink chain of the Head End. The signal generator is set for 481.2500 MHz with a level of -90 dBm. The signal generator output is applied to the DSP Input port at “ A. “

The Duplexer Input/Output port is connected to a spectrum analyzer. The expected signal level at “ B “ is around +20 dBm.



UPLINK 481.2500 MHz

Uplink Test Set-Up



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