Intel® 820 Chipset

Design Guide

July 2000

Order Number: 290631-004

Contents

Figures

Tables

Revision History

Revision	Description	Date
-001	Initial Release.	November 1999
-002	• Added dual-processor schematics (Appendix B). • Uni-processor schematics have been updated (Appendix A). See the schematic revision history page at the end of Appendix A for details. - The following update is not in the schematic revision history. Cap C249 (schematic page 9) has been changed from 0.022 uF to 0.047 uF.	December 1999
-003	• Updated the text descriptions in the two paragraphs in Section 4.2.3, “MCH to DRCG”. • Updated the first paragraph in Section 2.6.2.5, “RSL Signal Layer Alternation“.	January 2000
-004	• Minor edits for clarity	July 2000

This page is intentionally left blank.

1

Introduction

This page is intentionally left blank.

Introduction 1

The Intel® 820 Chipset Design Guide provides design recommendations for systems using the Intel® 820 chipset. This includes motherboard layout and routing guidelines, system design issues and requirements, debug recommendations, and board schematics. The design recommendations should be used during system design. The guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues.

The Intel board schematics in Appendix A (uni-processor) and Appendix B (dual-processor) can be used as references for board designers. A feature list is provided at the beginning of each appendix. Although these schematics cover specific designs, the core schematics for each chipset component remains the same for most Intel® 820 chipset platforms. The appendices provides a set of reference schematics for each chipset component, in addition to common motherboard options. Additional flexibility is possible through other permutations of these options and components.

1.1 About This Design Guide

This design guide is intended for hardware designers who are experienced with PC architectures and board design. The design guide assumes that the designer has a working knowledge of the vocabulary and practices of PC hardware design.

- This chapter introduces the designer to the purpose and organization of this design guide, and provides a list of references of related documents. This chapter also provides an overview of the Intel® 820 chipset.
- Chapter 2, "Layout/Routing Guidelines"—This chapter provides a detailed set of motherboard layout and routing guidelines for designing an Intel® 820 chipset based platform. The motherboard functional units are covered (e.g., chipset component placement, system bus routing, system memory layout, display cache interface, hub interface, IDE, AC’97, USB, interrupts, SMBUS, PCD, LPC/FWH Flash BIOS, and RTC).
- Chapter 3, "Advanced System Bus Design"— AGTL+ guidelines and theory of operation are discussed. This chapter also provides more detail about the methodologies used to develop the guidelines.
- Chapter 4, "Clocking"— This chapter provides motherboard clocking guidelines (e.g., clock architecture, routing, capacitor sites, clock power decoupling, and clock skew).
- Chapter 5, "System Manufacturing"— This chapter includes board stackup requirements.
- Chapter 6, "System Design Considerations"— This chapter includes guidelines regarding power delivery, decoupling, thermal, and power sequencing.
- Appendix A, "Reference Board Schematics: Uni-Processor "— This appendix provides a set of schematics for Uni-processor designs. A feature list for the board design is also provided.
- Appendix B, "Reference Board Schematics: Dual-Processor "— This appendix provides a set of schematics for dual-processor designs. A feature list for the board design is also provided.

1.2 References

- *Intel® 820 Chipset: Intel® 82820 Memory Controller Hub (MCH)* Datasheet (Order Number: 290630)
- *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet (Order Number: 290655)
- *Intel® 82802AB/82802AC FirmWare Hub (FWH)* Datasheet (Order Number: 290658)
- *Pentium® II Processor AGTL+ Guidelines* (Order Number: 243330)
- *Pentium® II Processor Power Distribution Guideline (*Order Number: 243332)
- *Pentium® II Processor Developer's Manual* (Order Number: 243341)
- *Pentium® III Processor Specification Update* (latest off of website)
- *AP 907 Pentium III processor Power Distribution Guidelines* (Order Number 245085)
- *AP-585 Pentium II Processor AGTL+ Guidelines* (Order Number: 243330)
- *AP-587 Pentium II Processor Power Distribution Guidelines* (Order Number: 243332)
- *CK97 Clock Synthesizer Design Guidelines* (Order Number 243867)
- *PCI Local Bus Specification*, Revision 2.2
- *Universal Serial Bus Specification*, Revision 1.0
- *VRM 8.4 DC-DC Converter Design Guidelines* (when available)

1.3 System Overview

The Intel® 820 chipset is the third generation desktop chipset designed for Intel's SC242 architecture and the first chipset to support the 4X capability of the AGP 2.0 Interface Specification and 400 MHz Direct RDRAM. The 400 MHz, 16 bit, *double clocked* Direct RDRAM interface provides 1.6 GB/s access to main memory. A new chipset component interconnect, the hub interface, is designed into the Intel® 820 chipset to provide more efficient communication between chipset components.

Support of AGP 4X, 400 MHz Direct RDRAM and the hub interface provides a balanced system architecture for the Pentium III processor, minimizing bottlenecks and increasing system performance. By increasing memory bandwidth to 1.6 GB/s through the use of 400 MHz Direct RDRAM and increasing graphics bandwidth to 1 GB/s through the use of AGP 4X, the Intel® 820 chipset delivers the data throughput necessary to take advantage of the high performance provided by the powerful Pentium III processor.

In addition, the Intel® 820 chipset architecture enables a new security and manageability infrastructure through the Firmware Hub component.

The ACPI compliant Intel® 820 chipset platform can support the *Full-on*, *Stop Grant*, *Suspend to RAM*, *Suspend to Disk*, and *Soft-off* power management states. Through the use of an appropriate LAN device, Intel® 820 chipset also supports *Wake on LAN** for remote administration and troubleshooting.

The Intel® 820 chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of Intel chipsets. This removes many of the conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true *plug-and-play* for the Intel® 820 chipset platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use *software*

configurable AC'97 audio and modem coder/decoders (codecs) instead of the traditional ISA devices. The ISA bus can be implemented through the use of the optional 82380AB PCI-ISA bridge.

The Intel® 820 chipset contains two *core* components: the Memory Controller Hub (MCH) and the I/O Controller Hub (ICH). The MCH integrates the 133 MHz processor system bus controller, AGP 2.0 controller, 400 MHz Direct RDRAM controller and a high-speed hub interface for communication with the ICH. The ICH integrates an UltraATA/66 controller, USB host controller, LPC interface controller, FWH Flash BIOS interface controller, PCI interface controller, AC'97 digital controller and a hub interface for communication with the MCH. The Intel® 820 chipset provides the data buffering and interface arbitration required to ensure that system interfaces operate efficiently and provide the system bandwidth necessary to obtain peak performance with the Pentium III processor.

1.3.1 Chipset Components

This section provides an overview of the 82820 Memory Controller Hub (MCH) and the 82801AA I/O Controller Hub (ICH). Additional functionality can be provided using the 82380AB PCI-ISA bridge.

Memory Controller Hub (MCH)

The MCH provides the interconnect between the Direct RDRAM and the system logic. It integrates the following functions:

- Support for single or dual SC242 processors with 100 MHz or 133 MHz System Bus
- 256 MHz, 300 MHz, 356 MHz or 400 MHz Direct RDRAM interface supporting 1 GB of Direct RDRAM
- 4X, 1.5V AGP interface (3.3V 1X, 2X and 1.5V 1X, 2X devices also supported)
- Downstream hub interface for access to the ICH

In addition, the MCH provides arbitration, buffering and coherency management for each of these interfaces. Refer to Chapter 2, "Layout/Routing Guidelines" for more information regarding these interfaces.

I/O Controller Hub (ICH)

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions. The ICH integrates the following functions:

- Upstream hub interface for access to the MCH
- 2 channel Ultra ATA/66 Bus Master IDE controller
- USB controller
- I/O APIC
- SMBus controller
- FWH interface (FWH Flash BIOS)
- LPC interface
- AC'97 2.1 interface
- PCI 2.2 interface
- Integrated System Management Controller
- Alert on LAN*

The ICH also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces. Refer to Chapter 2, "Layout/Routing Guidelines" for more information on these interfaces.

ISA Bridge (82380AB)

For legacy needs, ISA support is an optional feature of the Intel® 820 chipset. Implementations that require ISA support can benefit from the enhancements of the Intel® 820 chipset while "ISA-less" designs are not burdened with the complexity and cost of the ISA subsystem.

The Intel® 820 chipset platform with optional ISA support takes advantage of the 82380AB ISA bridge. The bridge is a PCI to ISA bridge and resides on the PCI bus of the ICH.

1.3.2 Bandwidth Summary

Table 1-1 provides a summary of the bandwidth requirements for the Intel® 820 chipset.

Table 1-1. Intel® 820 Chipset Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (Bytes)	Bandwidth (MB/s)
Processor Bus	133	1	133	8	1066
RDRAM	266/300/356/400	2	533/600/711/800	2	1066/1200/1422/1600
AGP 2.0	66	4	266	4	1066
Hub Interface	66	4	266	1	266
PCI 2.2	33	1	33	4	133

1.3.3 System Configuration

The following figures show typical platform configurations using the Intel® 820 chipset.

Figure 1-1. Intel® 820 Chipset Platform Performance Desktop Block Diagram

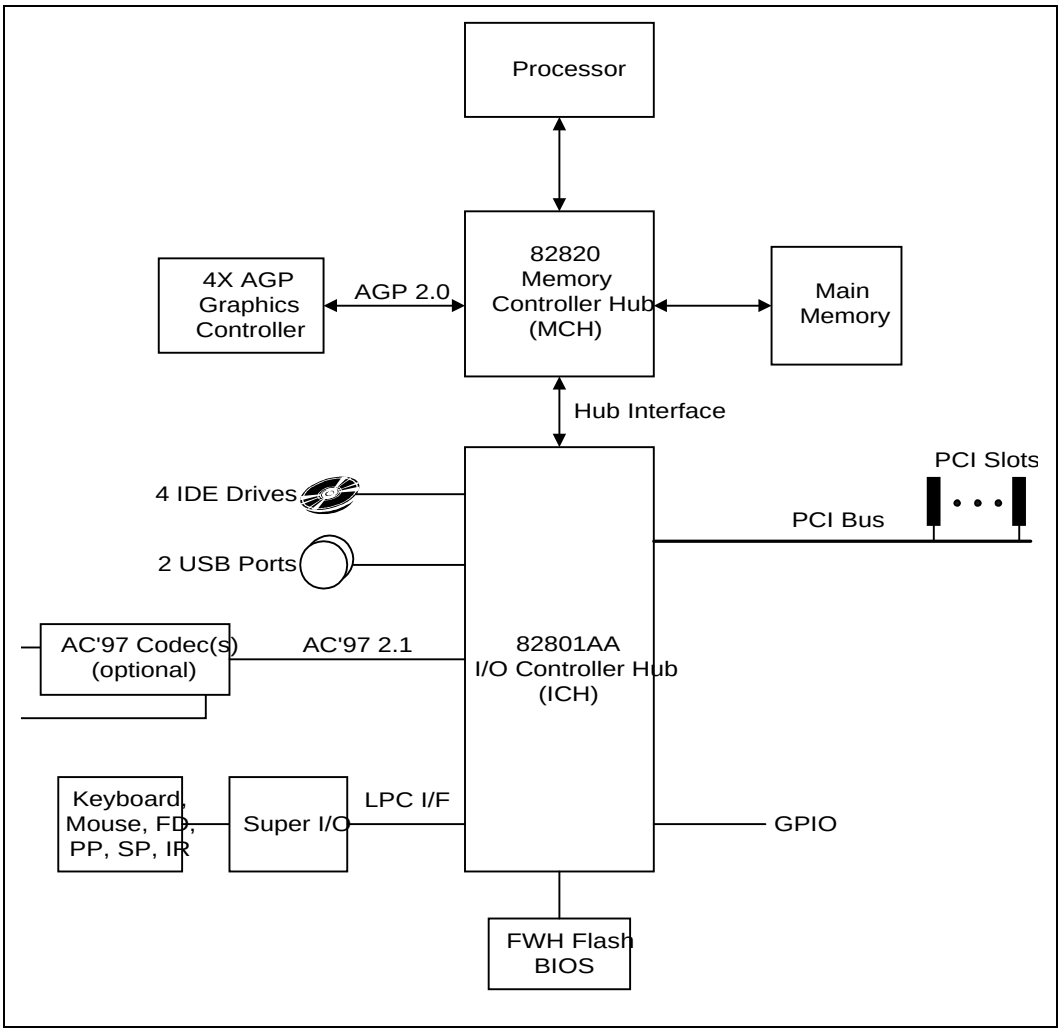


Figure 1-2. Intel® 820 Chipset Platform Performance Desktop Block Diagram (with ISA Bridge)

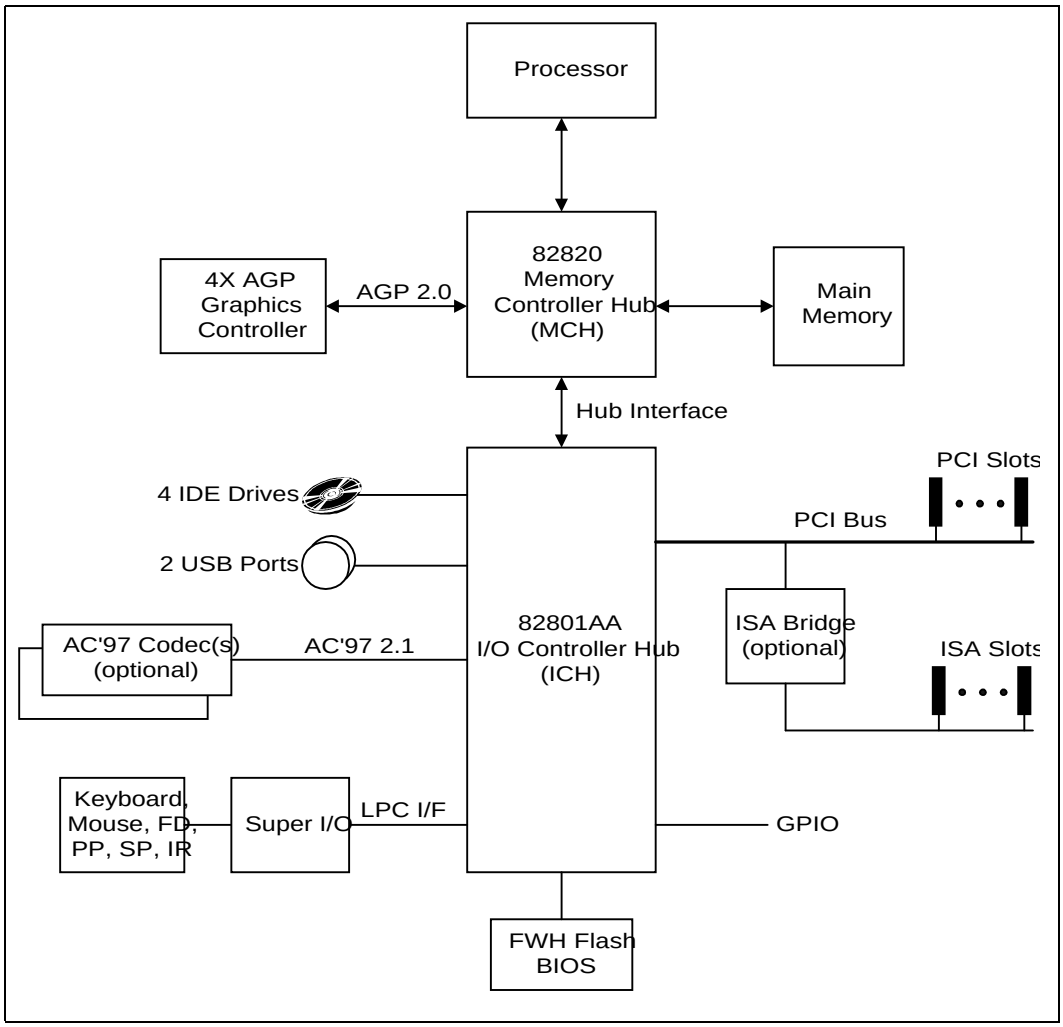
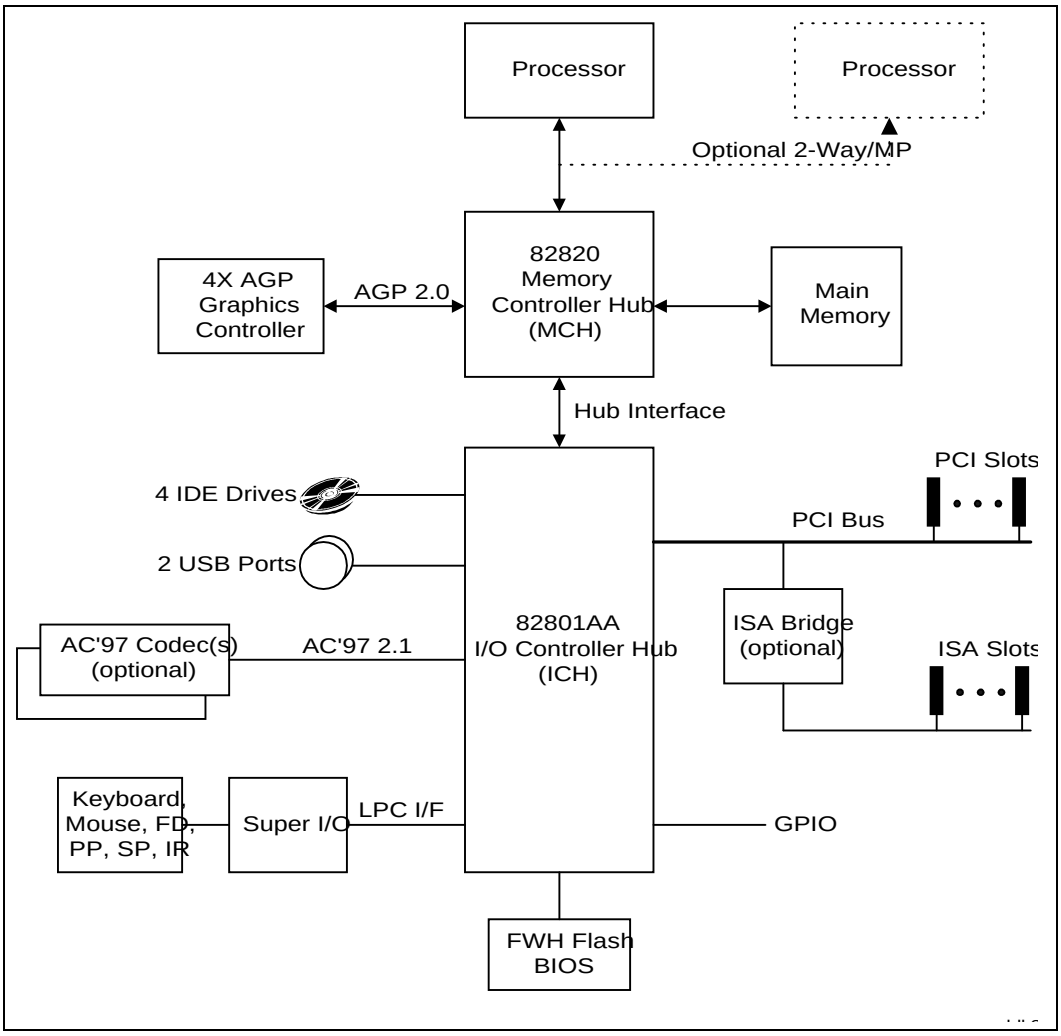


Figure 1-3. Intel® 820 Chipset Platform Dual-Processor Performance Desktop Block Diagram



1.4 Platform Initiatives

1.4.1 Direct Rambus*

The Direct Rambus* (RDRAM) initiative provides the memory bandwidth necessary to obtain optimal performance from the Pentium III processor as well as a high-performance AGP graphics controller. The MCH RDRAM interface supports 266 MHz, 300 MHz, 356 MHz, and 400 MHz operation; the latter delivers 1.6 GB/s of theoretical memory bandwidth; twice the memory bandwidth of 100 MHz SDRAM systems. Coupled with the greater bandwidth, the RDRAM protocol, which is heavily pipelined, provides substantially more efficient data transfer. The RDRAM memory interface can achieve greater than 95% utilization of the 1.6 GB/s theoretical maximum bandwidth.

In addition to RDRAM's performance features, the new memory architecture provides enhanced power management capabilities. The *powerdown* mode of operation enables Intel® 820 chipset based systems to cost-effectively support *suspend-to-RAM*.

1.4.2 Streaming SIMD Extensions

The Pentium III processor provides 70 new Streaming SIMD (single instruction, multiple data) Extensions. The Pentium III new extensions are floating point SIMD extensions. Intel MMX™ technology provides integer SIMD extensions. The Pentium III processor new extensions complement the Intel MMX™ technology SIMD extensions and provide a performance boost to floating-point intensive 3D applications.

1.4.3 AGP 2.0

The AGP 2.0 interface, along with Direct Rambus* memory technology, allows graphics controllers to access main memory at over 1 GB/s; twice the AGP bandwidth of previous AGP platforms. AGP 2.0 provides the infrastructure necessary for *photorealistic 3D.* In conjunction with Direct Rambus* and the Pentium III processor new Streaming SIMD Extensions, AGP 2.0 delivers the next level of 3D graphics performance.

1.4.4 Hub Interface

As I/O speeds increase, the demand placed on the PCI bus by the I/O bridge has become significant. With the addition of AC'97 and ATA/66, coupled with the existing USB, I/O requirements will begin to impact PCI bus performance. The Intel® 820 chipset's hub interface architecture ensures that the I/O subsystem, both PCI and the integrated I/O features (IDE, AC'97, USB, etc.), receives adequate bandwidth. By placing the I/O bridge on the hub interface instead of PCI, the hub architecture ensures that both the I/O functions integrated into the ICH and the PCI peripherals obtain the bandwidth necessary for peak performance. In addition, the hub interface's lower pin count allows a smaller package for the MCH and ICH.

1.4.5 Manageability

The Intel® 820 chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

TCO Timer

The ICH integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# which the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

CPU Present Indicator

The ICH looks for the CPU to fetch the first instruction after reset. If the CPU does not fetch the first instruction, the ICH will reboot the system at the *safe-mode* frequency multiplier.

ECC Error Reporting

Upon detecting an ECC error, the MCH can send one of several messages to the ICH. The MCH can instruct the ICH to generate either an SMI#, NMI#, SERR#, or TCO interrupt.

Function Disable

The ICH provides the ability to disable the following functions: AC'97 Modem, AC'97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.

Intruder Detect

The ICH provides an input signal (INTRUDER#) that can be attached to a switch that is activated by the system case being opened. The ICH can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

SMBus

The ICH integrates an SMBus controller. The SMBus provides an interface to manage peripherals (e.g., serial presence detection (SPD) on RIMMs and thermal sensors).

Alert on LAN*

The ICH supports Alert on LAN*. In response to a TCO event (intruder detect, thermal event, CPU not booting) the ICH sends a message over ALERTCLK and ALERTDATA. A LAN controller can decode this alert message and send a message over the network to alert the network manager.

1.4.6 AC'97

The *Audio Codec'97* (AC'97) Specification defines a digital link that can be used to attach an *audio codec* (AC), a *modem codec* (MC), an *audio/modem codec* (AMC), or both an AC and an MC. The AC'97 Specification defines the interface between the system logic and the audio or modem codec known as the *AC'97 Digital Link*.

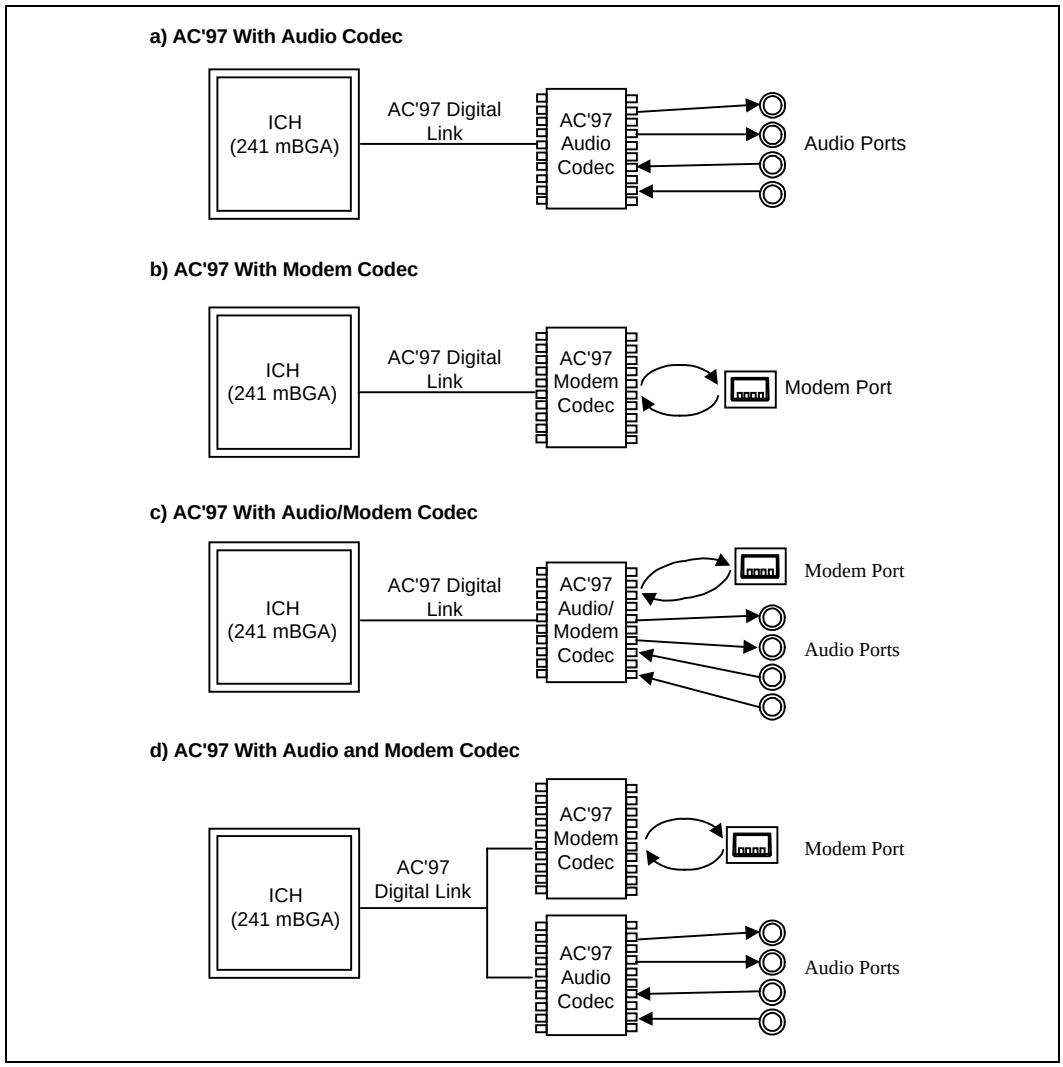
The ability to add cost-effective audio and modem solutions is important as the platform migrates away from ISA. In addition, the AC'97 audio and modem components are software configurable. This reduces configuration errors. Intel® 820 chipset's AC'97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC'97 digital link. Using Intel® 820 chipset's integrated AC'97 digital link reduces cost and eases migration from ISA.

By using an audio codec, the AC'97 digital link allows for cost-effective, high-quality, integrated audio on the Intel® 820 chipset platform. In addition, an AC'97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC'97. Intel® 820 chipset's integrated digital link allows two external codecs to be connected to the ICH. The system designer can provide audio with an audio codec (Figure 1-4a) or a modem with a modem codec (Figure 1-4b). For systems requiring both audio and a modem, there are two solutions. The audio codec and the modem codec can be integrated into a single Audio Modem Codec (AMC) (Figure 1-4c), or separate audio and modem codecs can be connected to the ICH (Figure 1-4d).

Modem implementation for different countries must be considered as telephone systems may vary. By using a split design, the audio codec can be on-board and the modem codec can be placed on a riser. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

The digital link in the ICH is AC'97 Rev. 2.1 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

Figure 1-4. (a-d) AC'97 Connections



1.4.7 Low Pin Count (LPC) Interface

In the Intel® 820 chipset platform, the super I/O component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost super I/O designs. The LPC super I/O component requires the same feature set as traditional super I/O components. It should include a keyboard and mouse controller, floppy disk controller and serial and parallel ports. In addition to the super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In a system with ISA audio, the game port typically existed on the audio card. The fifteen pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your super I/O vendor for a comprehensive list of devices offered and features supported.

In addition, depending on system requirements, a device bay controller and USB hub could be integrated into the LPC super I/O component. For systems requiring ISA support, an ISA-IRQ to serial-IRQ converter is required. Potentially, this converter could be integrated into the super I/O.

This page is intentionally left blank

2

Layout and Routing Guidelines

This page is intentionally left blank.

Layout/Routing Guidelines 2

This chapter documents motherboard layout and routing guidelines for Intel® 820 chipset based systems. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

Caution: **If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design.** Even when the guidelines are followed, critical signals should still be simulated to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely. **Any deviation from these guidelines must be simulated!**

2.1 General Recommendations

The trace impedance typically noted (i.e., 60 Ω ±10%) is the "nominal" trace impedance. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. In addition, the PCB should be fabricated as documented in Section 5.3, "Stackup Requirement" on page 5-1 of this document.

All recommendations in this section (except where noted) assume 5 mil wide traces. If trace width is greater than 5 mils then the trace spacing requirements must be adjusted accordingly (linearly). For example, this section recommends routing most AGP signals with 5 mil traces on 20 mil spaces (1:4). If 6 mil traces are used, then 24 mil spaces must be used (also 1:4). Using a wider trace (and therefore wider spaces) will make routing more difficult.

Additionally, these routing guidelines are created using the *stack-up* described in section Section 5.3, "Stackup Requirement" on page 5-1. If this stack-up is not used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

2.2 Component Quadrant Layout

The quadrant layouts shown are approximate and the exact ball assignments should be used to conduct routing analysis. These quadrant layouts are designed for use during component placement.

Figure 2-1. MCH 324-uBGA Quadrant Layout (Top View)

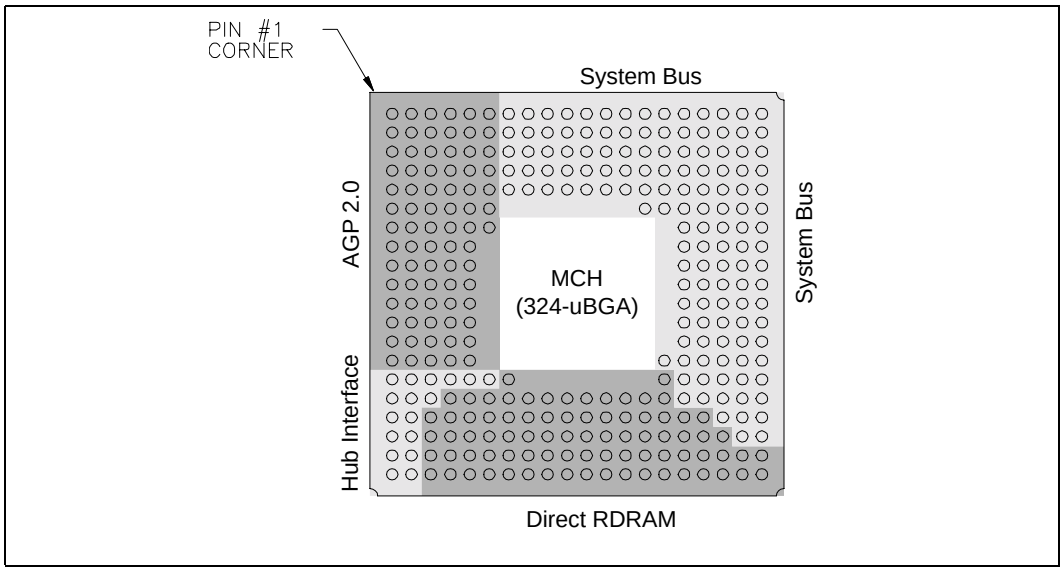
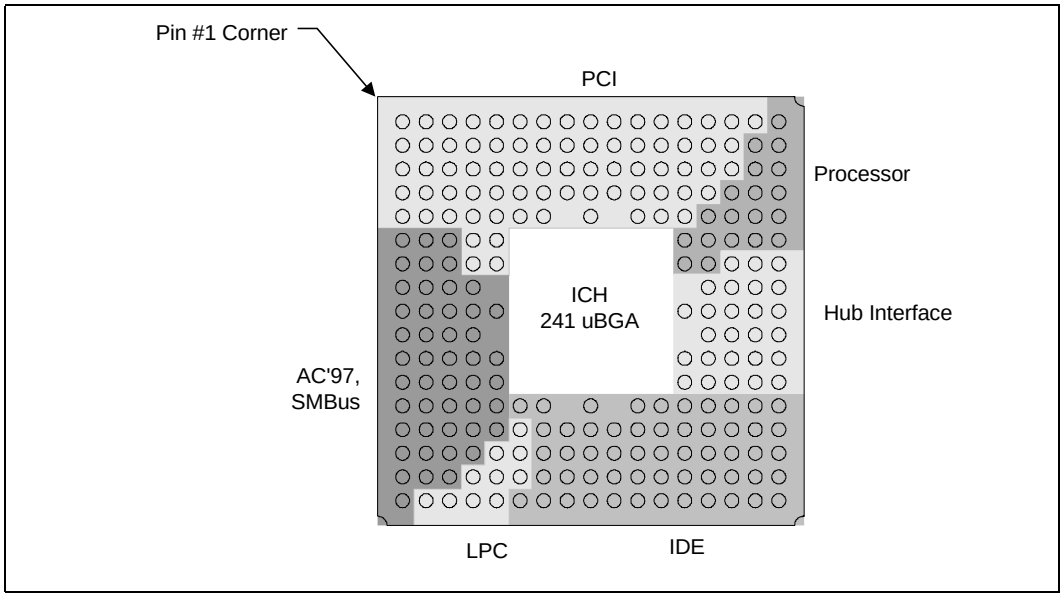


Figure 2-2. ICH 241-uBGA Quadrant Layout (Top View)

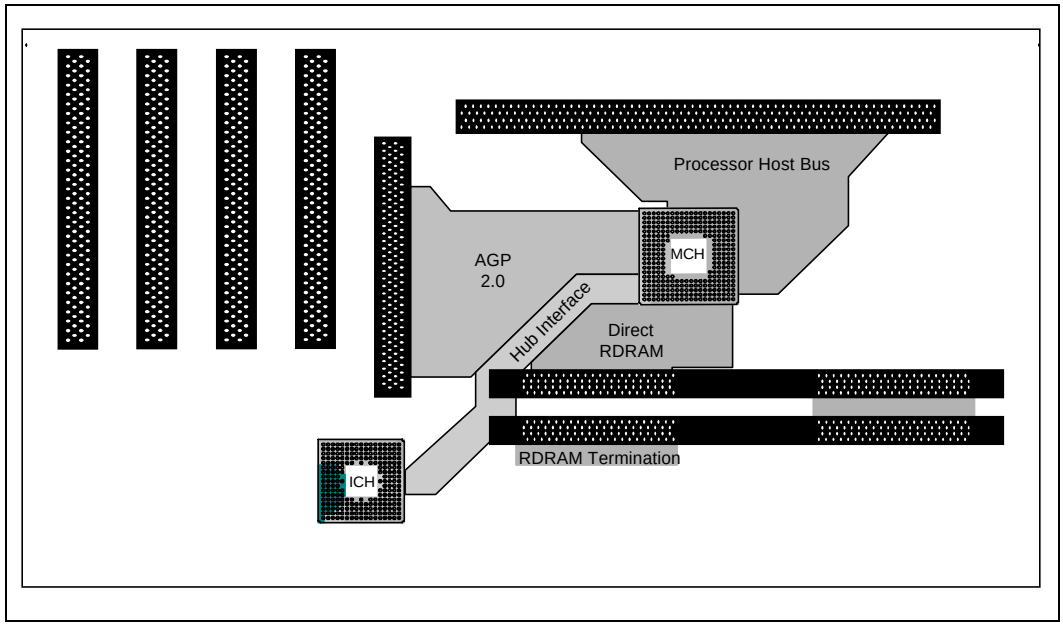


2.3 Intel® 820 Chipset Component Placement

Notes:

1. The ATX placements and layouts shown in Figure 2-3 is recommended for single (UP) Intel® 820 chipset based system design.
2. The trace length limitation between critical connections will be addressed later in this document.
3. The figure is for ***reference only.***

Figure 2-3. Sample ATX MCH/ICH Component Placement



2.4 Core Chipset Routing Recommendations

Figure 2-4 and Figure 2-5 show MCH core routing examples.

Figure 2-4. Primary Side MCH Core Routing Example (ATX)

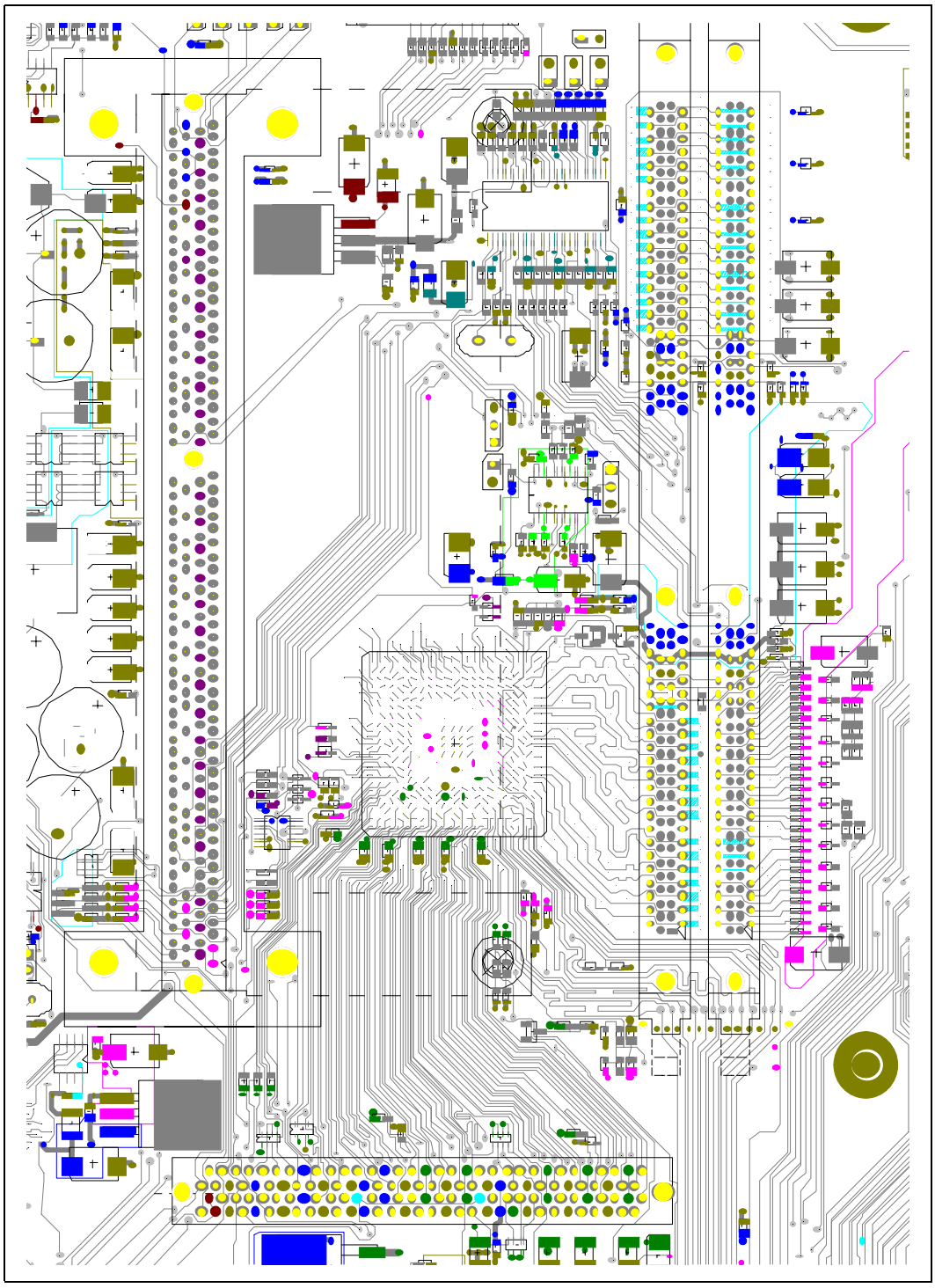
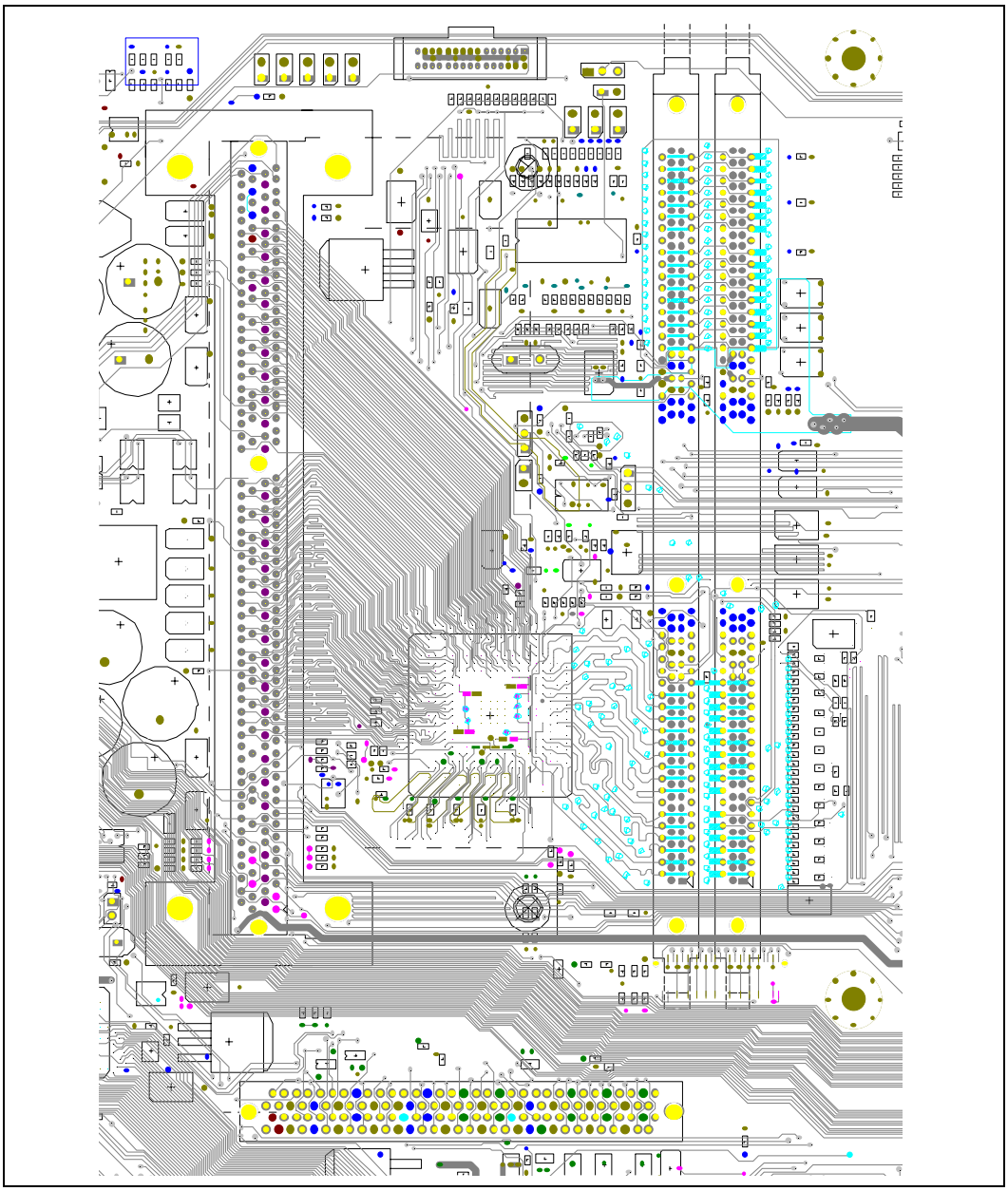


Figure 2-5. Secondary Side MCH Core Routing Example (ATX)

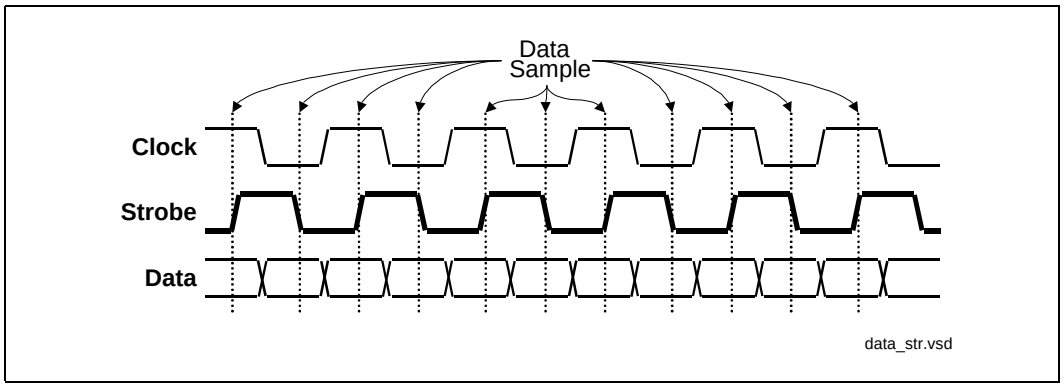


2.5 Source Synchronous Strobing

Source synchronous strobing is one of the technologies used in AGP 4X, Direct RDRAM and hub interface that allow very high data transfer rates. As buses get faster, and cycle times get shorter, the propagation delay is becoming a limiting factor in bus speed. Source synchronous strobing is used to minimize the impact of propagation delay (T_{prop}) on maximum bus frequency.

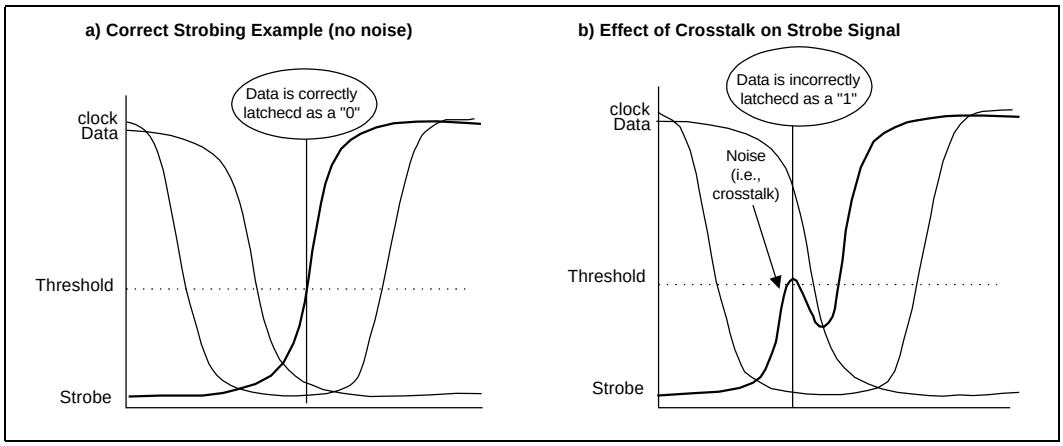
A source synchronous strobed interface uses strobe signals (instead of the clock) to indicate that data is valid. Refer to Figure 2-6 for an example.

Figure 2-6. Data Strobing Example



For a source synchronous strobed interface, it is *very important* that the strobe signals are routed carefully. These signals must be very clean (free of noise). Data signals are typically latched on the rising or falling edge of the strobe signal (or both). If there is noise on these signals, it could cause an extra “edge” to be detected, thus latching incorrect data. Refer to Figure 2-7 for examples.

Figure 2-7. Effect of Crosstalk on Strobe Signal



Some buses have more than one strobe (i.e., AGP). The AGP 1.0 specification (1X and 2X mode) employs 3 strobe signals. These three strobe signals are each used to strobe different *data* signals. That is, each strobe has an associated set of *data* signals. The associations for AGP 1.0 (AGP 2X) are documented in Table 2-1. Refer to Section 2.7, “AGP 2.0” on page 2-31 for more information on AGP 2.0 (AGP 4X, 1.5v).

Table 2-1. AGP 2X Data/Strobe Association

Data	Associated Strobe
AD[15:0] and C/BE[1:0]#	AD_STB0
AD[31:16] and C/BE[3:2]#	AD_STB1
SBA[7:0]	SB_STB

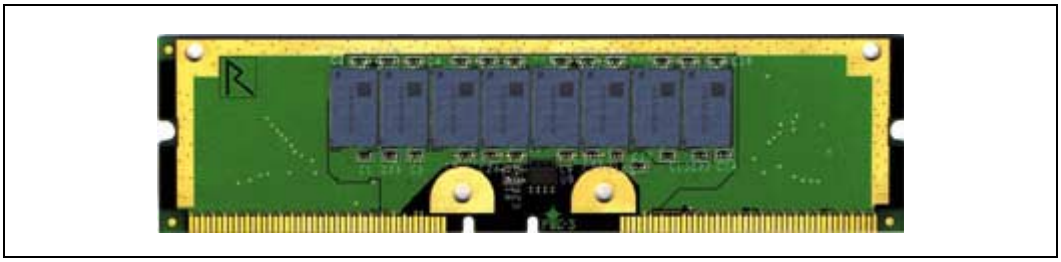
In this example, the lower address signals (AD[15:0]) are sampled on the rising and falling edges of AD_STB0, while the upper address signals (AD[31:16]) are sampled on the rising and falling edges of AD_STB1.

When routing strobes and their associated data lines, trace length mismatch is very important (in addition to noise immunity). The primary benefit of source synchronous strobing is that the data and the strobe arrive at the receiver simultaneously. Thus, a strobe and its associated data signals have very critical length mismatch requirements. With well matched trace lengths (as well as matched impedance), the propagation delay for the strobe, and the propagation delay for the data will be very close. Hence, the strobe and the data arrive at the receiver simultaneously. For some interfaces, the trace length mismatch requirement is less than 0.25 inch.

2.6 Direct Rambus* Interface

The Direct Rambus* Channel is a multi-symbol interconnect. Due to the length of the interconnect and the frequency of operation, this bus is designed to allow multiple command and data packets to be present on a signal wire at any given instant. The driving device sends the next data out before the previous data has left the bus.

Figure 2-8. RIMM Diagram



The nature of the multi-symbol interconnect forces many requirements on the bus design and topology. First and foremost, a drastic reduction in reflected voltage levels is required. The interconnect transmission lines must be terminated at their characteristic impedance, or the reflected voltage resulting from a mismatch in impedance will degrade signal quality. These reflections will reduce noise and timing margins, and reduce the maximum operating frequency of the bus. Potentially, the reflections could create data errors.

Due to the tolerances of components such as PCBs, connectors, and termination resistors, there will be some reflected voltage on the interconnect. In this multi-symbol interconnect, timings are pattern dependent due to the reflections interfering with the next transfer.

Additionally, coupled noise can greatly affect the performance of high-speed interfaces. Just as in source synchronous designs, the odd and even mode propagation velocity change creates skew between the clock and data or command lines which reduces the maximum operating frequency of the bus. Efforts must be made to significantly decrease crosstalk, as well as the other sources of skew.

To achieve these bus requirements, the Direct Rambus* channel is designed to operate as a transmission line; all components, including the individual RDRAMs, are incorporated into the design to create a uniform bus structure that can support up to 33 devices (including the MCH) running at 800 MegaTransfers/second (MT/s).

2.6.1 Stackup

The perfect matching of transmission line impedance and uniform trace length are essential for the Direct RDRAM interface to work properly. Maintaining 28 Ω (±10%) loaded impedance for every RSL (Direct Rambus* Signaling Level) signal has changed the requirements for trace width and prepreg thickness for the Intel® 820 chipset platform (refer to Section 5.3, “Stackup Requirement” on page 5-1).

Achieving a 28 Ω nominal impedance with a traditional 7 mil prepreg requires 28 mil wide traces. These traces are too wide to break out of the two rows of RSL balls on the MCH. To reduce trace width, a 4.5 mil thick prepreg is required. This thinner prepreg allows 18 mil wide traces to meet the 28 Ω (±10%) nominal impedance requirement. Refer to Section 5.3, “Stackup Requirement” on page 5-1 for detailed stackup requirements.

2.6.2 Direct Rambus* Layout Guidelines

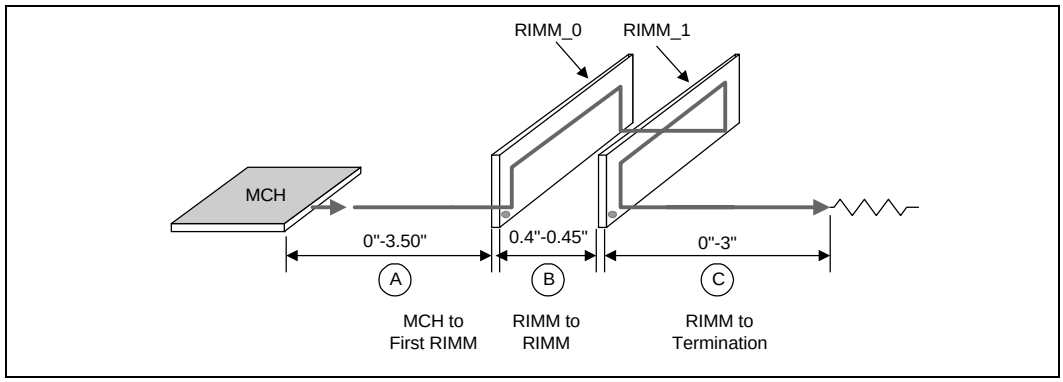
The signals on the Direct Rambus* Channel are broken into three groups: RSL signals, CMOS signals, and Clocking signals. The signal groups are:

- RSL Signals
  - DQA[8:0]
  - DQB[8:0]
  - RQ[7:0]
- CMOS Signals
  - CMD (high-speed CMOS signal)
  - SCK (high-speed CMOS signal)
  - SIO
- Clocking Signals
  - CTM, CTM#
  - CFM, CFM#

2.6.2.1 RSL Routing

The RSL signals enter the first RIMM on the left side, propagate through the RIMM, and exit on the right. The signal continues through the rest of the existing RIMMs until it is terminated at V_{term}. All unpopulated slots must have continuity modules in place to ensure that the signals propagate to the termination.

Figure 2-9. RSL Routing Dimensions



To maintain a nominal 28 Ω trace impedance, the RSL signals must be 18 mils wide. To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace routed between adjacent RSL signals. The 10 mil ground isolation traces must be connected to ground with a via every 1”. A 6 mil gap is required between the RSL signals and the ground isolation trace. These signals must be length matched to ±10 mils in line section “A” and ±2 mils in both line sections labeled “B” using the trace length matching methods in Section 2.6.2.6, “Length Matching Methods” on page 2-21. To ensure uniform trace lines, trace width variation must be uniform on all RSL signals at every neck-down for each line section. All RSL signals must have the same number of vias. It may be necessary to place vias on RSL signals where they are not necessary to meet this via loading requirement (i.e., dummy vias).

Table 2-2. Placement Guidelines for Motherboard Routing Lengths

Reference	Trace Description	Maximum Trace Length (in.)
A	MCH to first RIMM Connector	0” to 3.50”
B	RIMM to RIMM	0.4” – 0.45”
C	RIMM to Termination	0” to 3”

Figure 2-10 shows a top view of the trace width/spacing requirements for the RSL signals.

Figure 2-10. RSL Routing Diagram

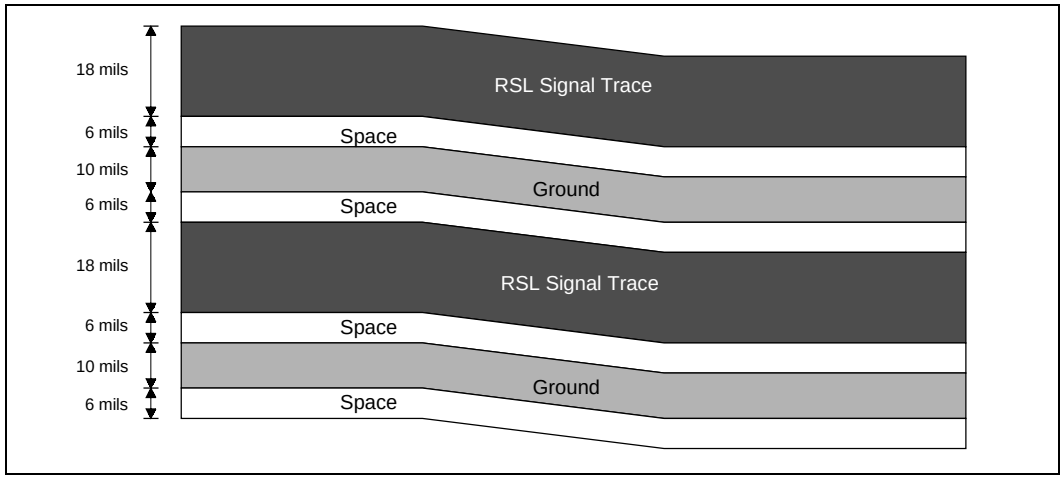


Figure 2-11 and Figure 2-12 show a top view of an example RSL breakout and route.

Figure 2-11. Primary Side RSL Breakout Example

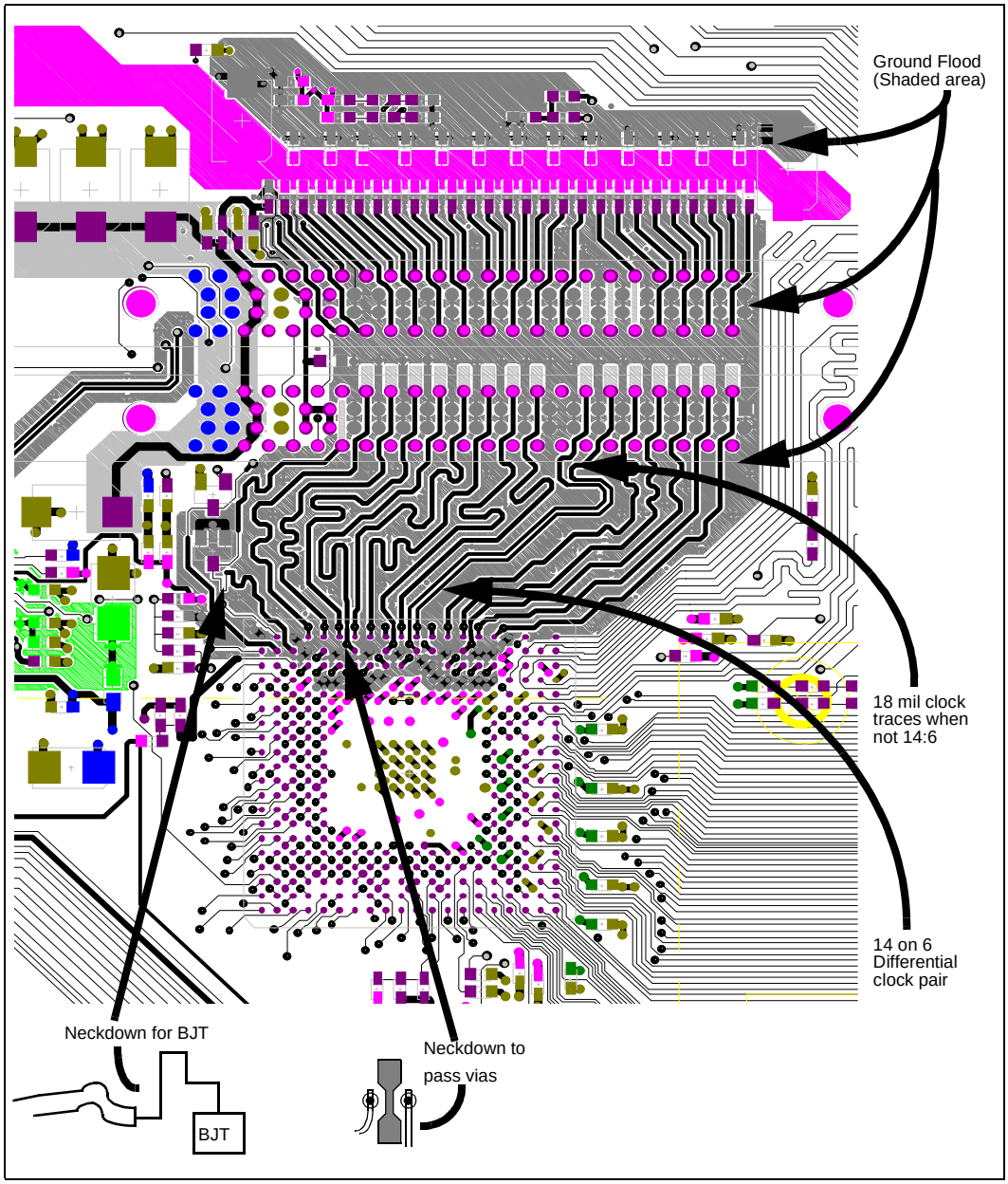
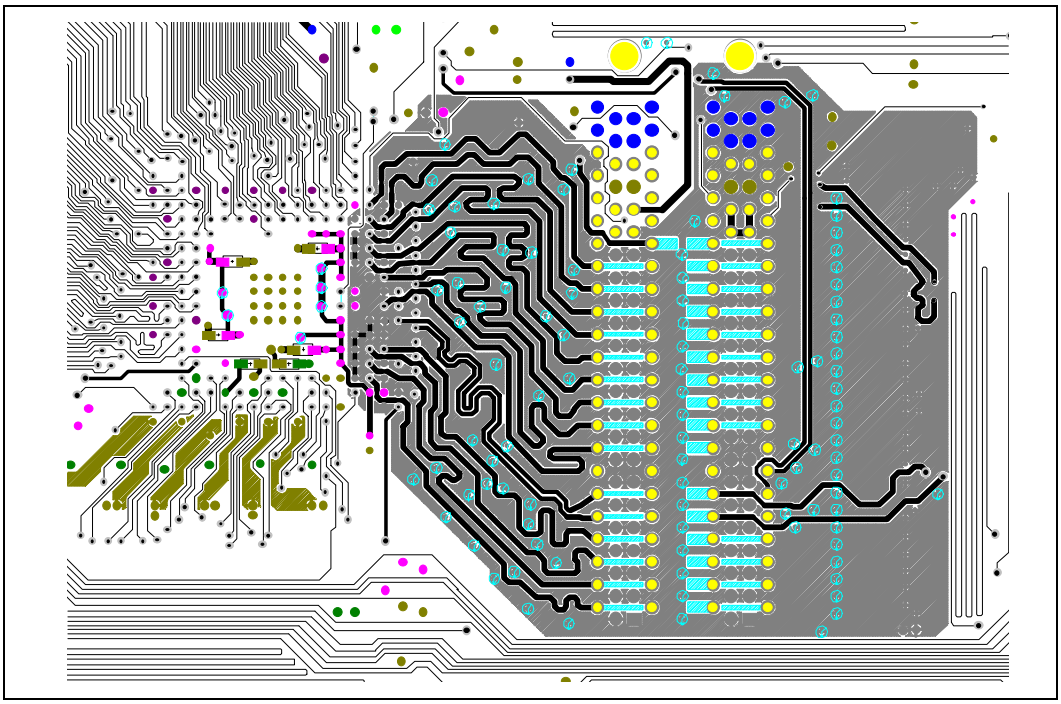


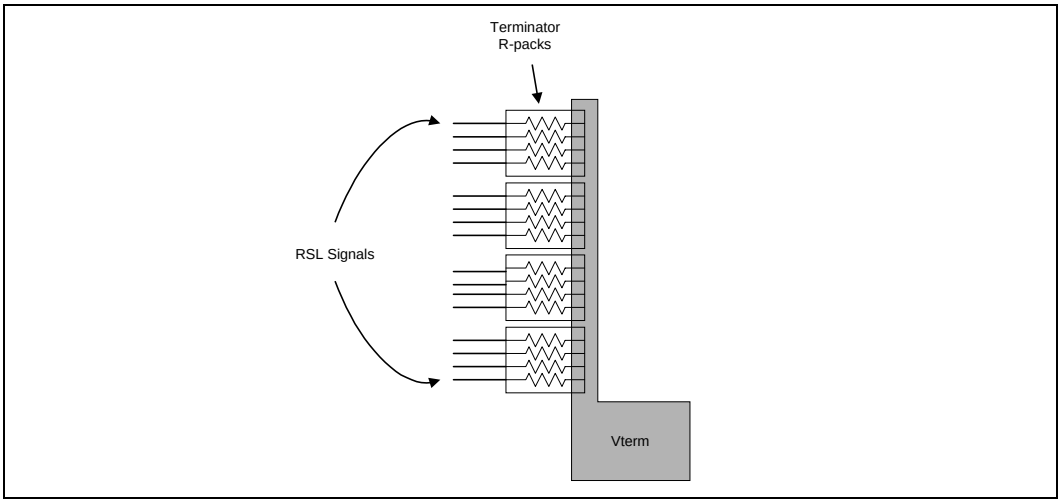
Figure 2-12. Secondary Side RSL Breakout Example



2.6.2.2 RSL Termination

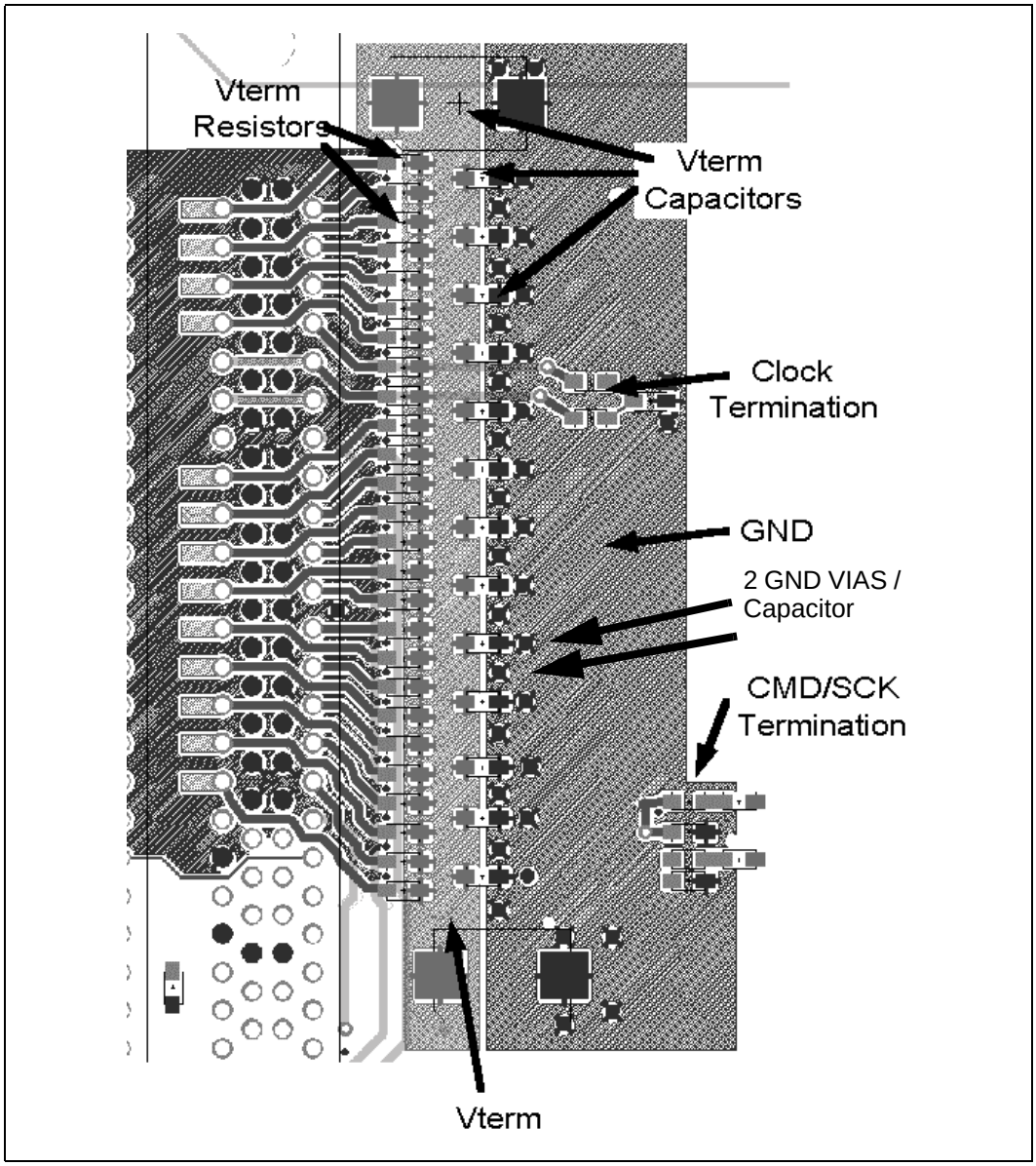
All RSL signals must be terminated to 1.8V (Vterm) using 27Ω-2% or 28Ω-1% resistors at the end of the channel opposite the MCH. Resistor packs are acceptable. Vterm must be decoupled using high speed bypass capacitors (one 0.1 µF ceramic chip capacitor per two RSL lines) near the terminating resistors. Additionally, bulk capacitance is required. Assuming a linear regulator with approximate 20 ms response time, two 100 µF tantalum capacitors are recommended. The trace length between the last RIMM and the termination resistors should be less than 3". Length matching in this section of the channel is not required. The Vterm power island should be at LEAST 50 mils wide. This voltage does not need to be supplied during suspend-to-RAM.

Figure 2-13. Direct RDRAM Termination



Note: It is necessary to compensate for the slight difference in electrical characteristics between a dummy via and a real via. Refer to Section 2.6.2.7, “VIA Compensation” on page 2-23 for more information on Via Compensation.

Figure 2-14. Direct Rambus* Termination Example



2.6.2.3 Direct Rambus* Ground Plane Reference

All RSL signals must be referenced to GND to provide an optimal current return path. The direct Rambus ground plane reference must be continuous to the Vterm capacitors. The ground reference island under the RSL signals must be continuous from the last RIMM to the back of the termination capacitors. Choose the reference island shape such that power delivery to the components is not compromised. The return current will flow through the Vterm capacitors into the ground island and under the RSL traces. Any split in the ground island will provide a sub-optimal return path. In a 4 layer board, this will require the Vterm island to be on an outer layer. The Vterm island should ALWAYS be placed on the top layer. Refer to Section 6.2, “Power Plane Splits” on page 6-7 for an example of power plane splits.

Figure 2-15. Incorrect Direct Rambus* Ground Plane Referencing

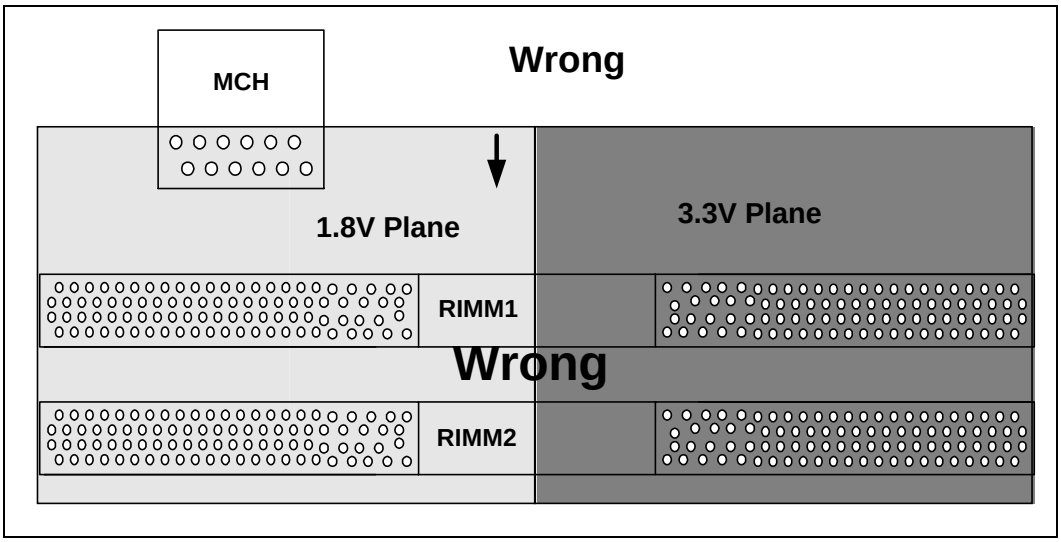
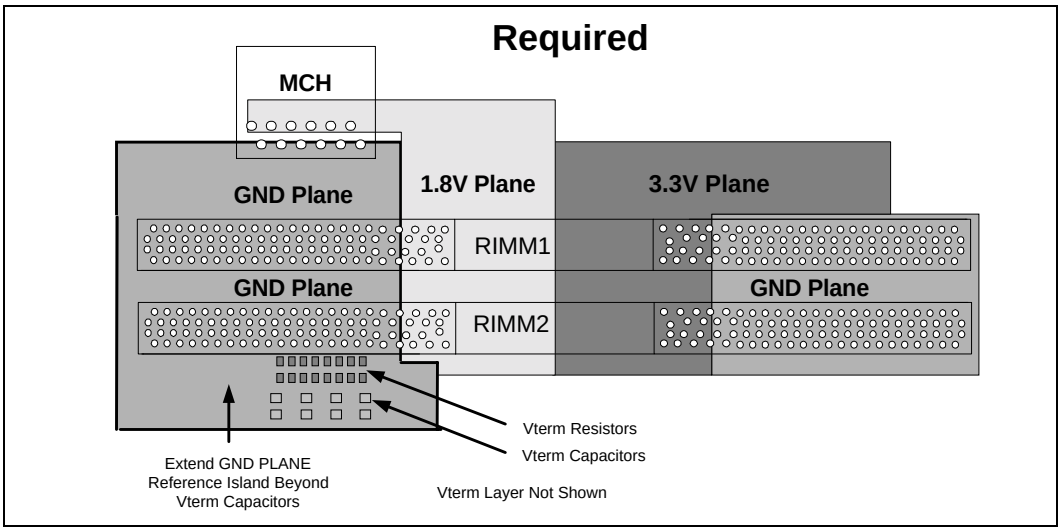


Figure 2-16. Direct Rambus Ground Plane Reference



The ground reference island under the RSL signals MUST be connected to the ground pins on the RIMM connector and the ground vias used to connect the ground isolation on the 1st and 4th layers.

All 4 layers of the motherboard require correct grounding between the RSL signals on the motherboard:

- Layer 1 = Ground Isolation
- Layer 2 = Ground Plane
- Layer 3 = Ground Reference in the Power Plane
- Layer 4 = Ground Isolation

All ground vias and pins MUST be connected to all 4 layers.

2.6.2.4 Direct Rambus* Connector Compensation

The RIMM connector inductance causes an impedance discontinuity on the Direct Rambus* channel. This may reduce voltage and timing margin.

To compensate for the inductance of the connector, approximately 0.65 pF–0.85 pF compensating capacitive tab (C-TAB) is required on each RSL connector pin. This compensating capacitance must be added to the following connector pins at each connector:

LCTM	LCTM#
RCTM	RCTM#
LCFM	LCFM#
RCFM	RCFM#
LROW[2:0]	RROW[2:0]
LCOL[4:0]	RCOL[4:0]
RDQA[8:0]	LDQA[8:0]
RDQB[8:0]	LDQB[8:0]
SCK	CMD

This can be achieved on the motherboard by adding a copper tab to the specified RSL pins at each connector. The target value is approximately 0.65 pF–0.85 pF. The copper tab area for the recommended stackup was determined through simulation. The placement of the copper tabs can be on any signal layer, independent of the layer on which the RSL signal is routed.

Equation is an approximation that can be used for calculating copper tab area on an outer layer.

Equation 2-1. Approximate Copper Tab Area Calculation

$$\text{Length} * \text{Width} = \text{Area} = C_{plate} * \text{Thickness of prepreg} / [(\varepsilon_0)(\varepsilon_r)(1.1)]$$

Where:

— $\varepsilon_0 = 2.25 \times 10^{-16}$ Farads/mil
— ε_r = Relative dielectric constant of prepreg material
— Thickness of prepreg = Stackup dependent
— Length, Width = Dimensions in mils of copper plate to be added
— Factor of 1.1 accounts for fringe capacitance.

Based on the stackup requirement in Section 5.3, “Stackup Requirement” on page 5-1 the copper tab area should be 2800 to 3600 sq mils. Different stackups require different copper tab areas. Table 2-3 shows example copper tab areas.

Table 2-3. Copper Tab Area Calculation

Dielectric Thickness (D)	Separation Between Signal Trace & Copper Tab	Minimum Ground flood	Air Gap between Signal & GND Flood	Compen-sating Capacitance in pF	Copper Tab (C-TAB) Area (A) In sq mils	C-TAB Shape (mils)
4.5	6	10	6	0.65	2800	140 L x 20 W 70 L x 40 W

Based on Equation 1, the tab area is 2800 sq mils, where ε_r is 4.2 and D is 4.5. These values are based on 2116 prepreg material.

Note that more than one copper tab shape may be used. The tab dimensions are based on copper area over the ground plane. The actual length and width of the tabs may be different due to routing constraints (e.g., if tab must extend to center of hole, or antipad); however, each copper tab should have equivalent area. For example, the copper tabs in Figure 2-17 have the following dimensions, when measured tangent to the antipad:

Inner C-TAB = 140 (length) x 20(width)

Outer C-TAB = 70 (length) x 40 (width)

The following figures show a routing example of tab compensation capacitors. Note that ground floods around the RIMM pins must not be interrupted by the capacitor tabs, and they must be connected to avoid discontinuity in the ground plane as shown.

Figure 2-17. Connector Compensation Example

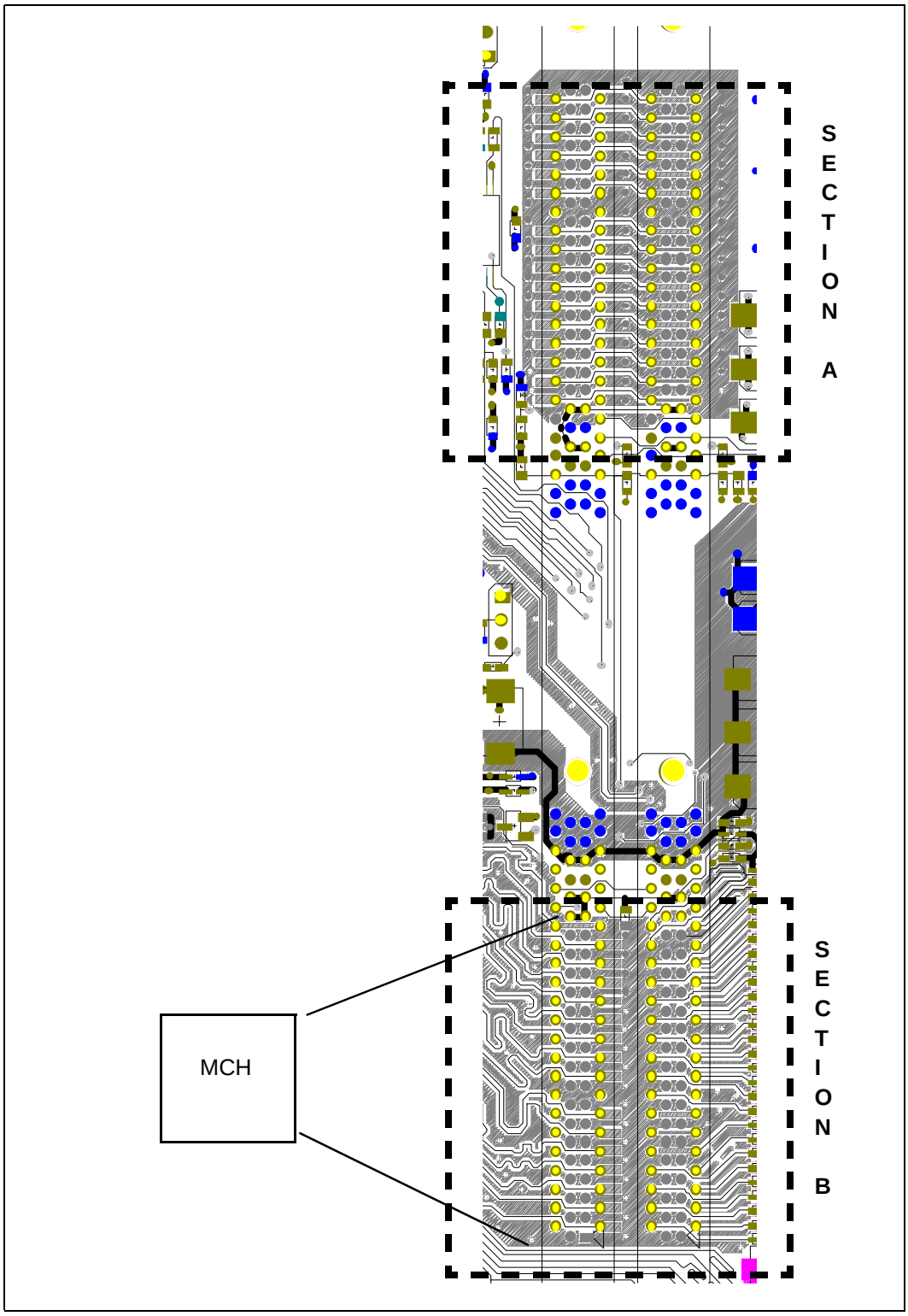
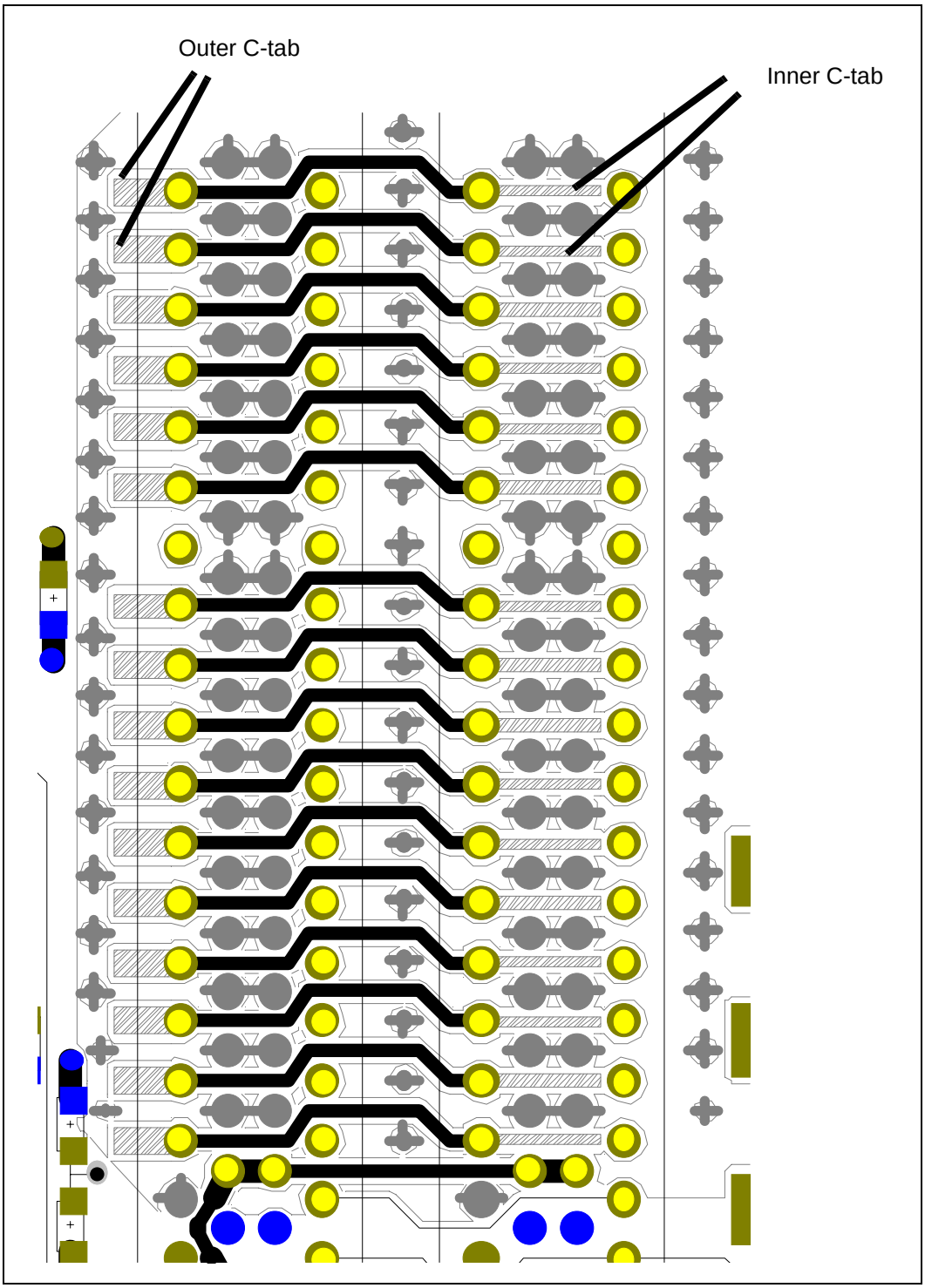
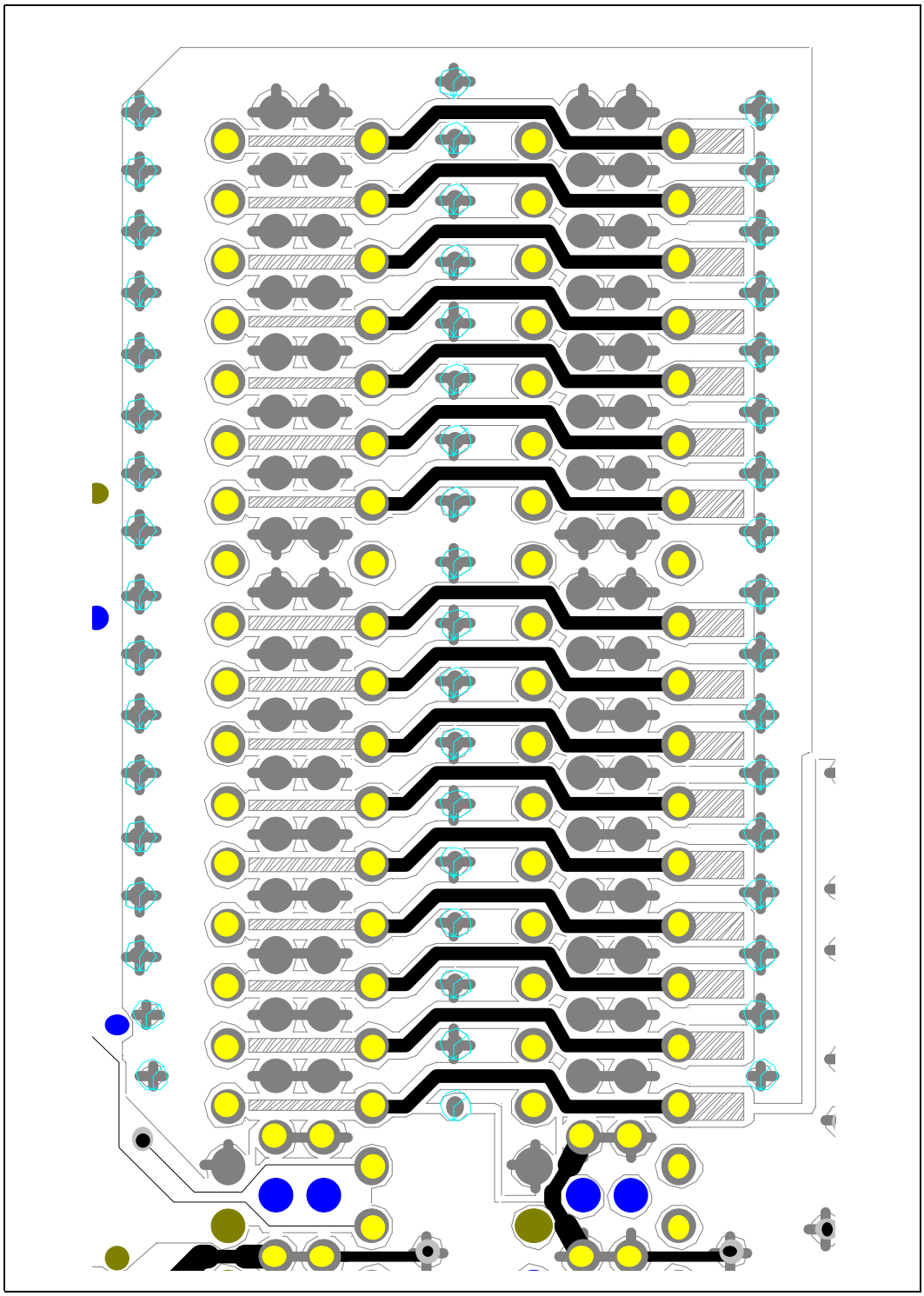


Figure 2-18. Section A[1], Top Layer



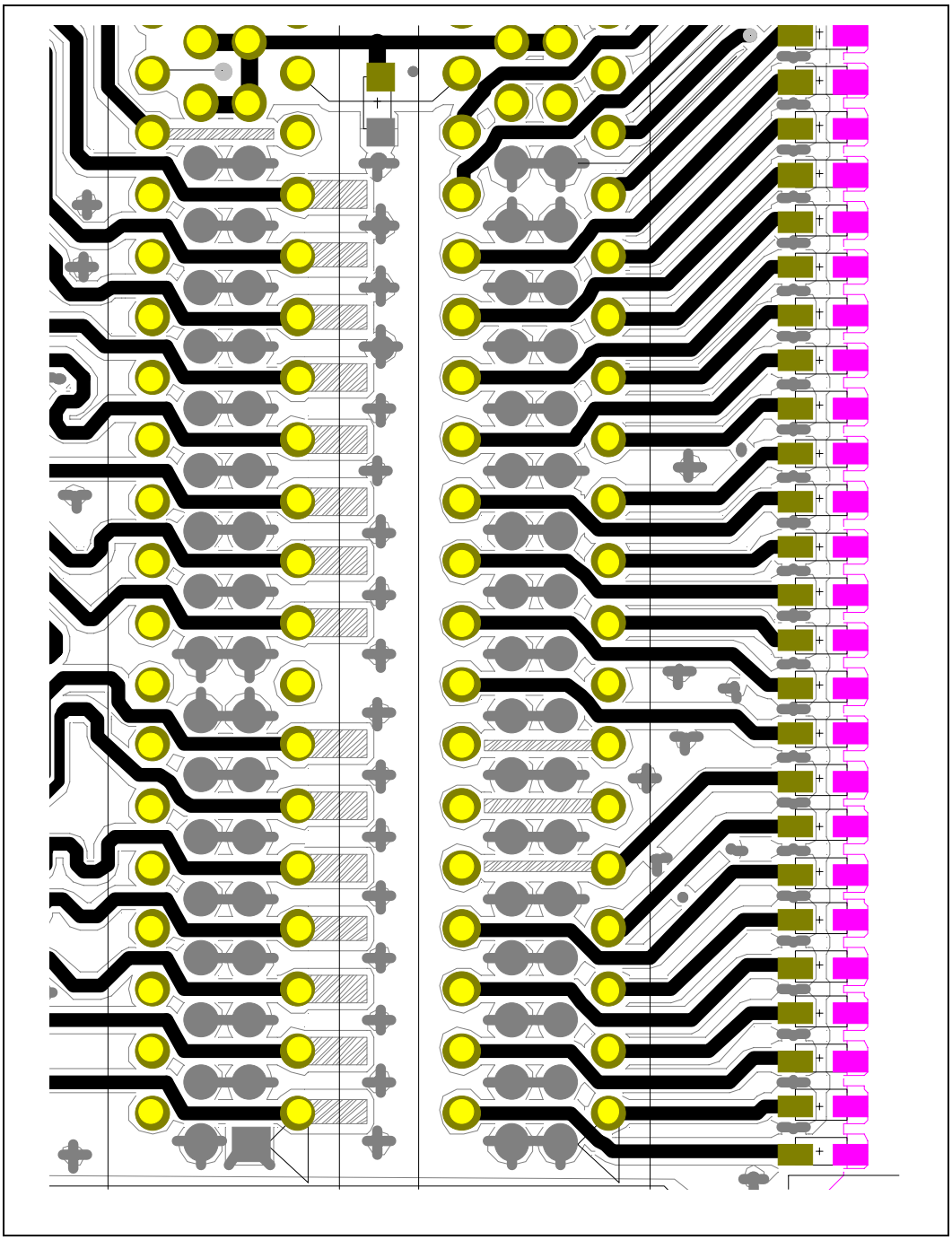
NOTES:
1. Refer to Figure 2-17. Ground flood removed from picture for clarity

Figure 2-19. Section A[1], Bottom Layer



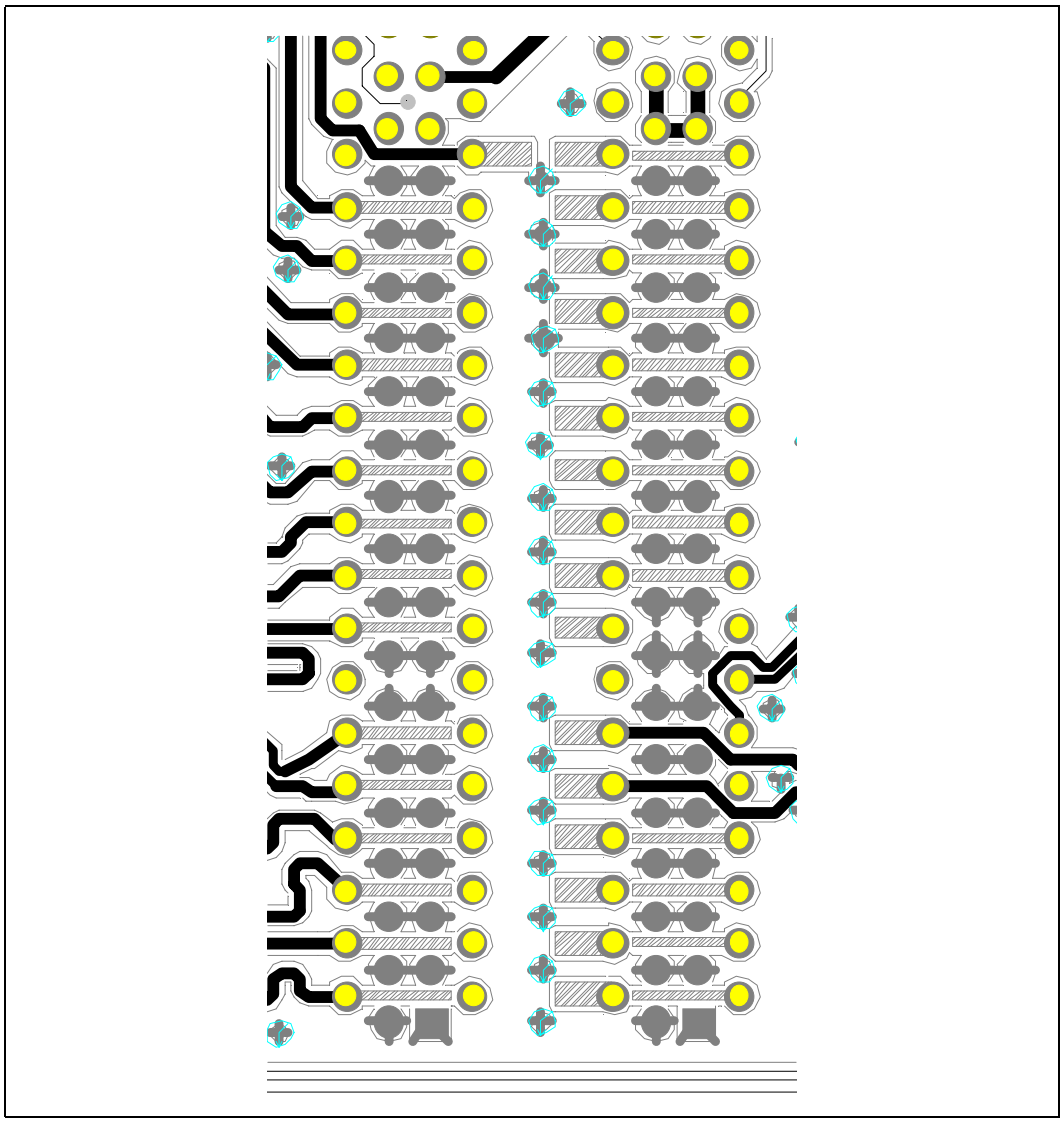
NOTES:
1. Refer to Figure 2-17. Ground flood removed from picture for clarity

Figure 2-20. Section B[1], Top Layer



NOTES:
1. Refer to Figure 2-17. Ground flood removed from picture for clarity

Figure 2-21. Section B[1], Bottom Layer



NOTES:
1. Refer to Figure 2-17. Ground flood removed from picture for clarity

2.6.2.5 RSL Signal Layer Alternation

RSL signals must alternate layers as they are routed through the channel. If a signal is routed on the primary layer from the MCH to the first RIMM socket, it must be routed on the secondary layer from the first RIMM to the second RIMM as shown in Figure 2-22 (signal B). If a signal is routed on the secondary layer from the MCH to the first RIMM socket, it must be routed on the primary layer from the first RIMM to the second RIMM as shown in Figure 2-22 (signal A). Signals to the termination resistors can be routed on either layer from the last RIMM.

Figure 2-22. RSL Signal Layer Alternation

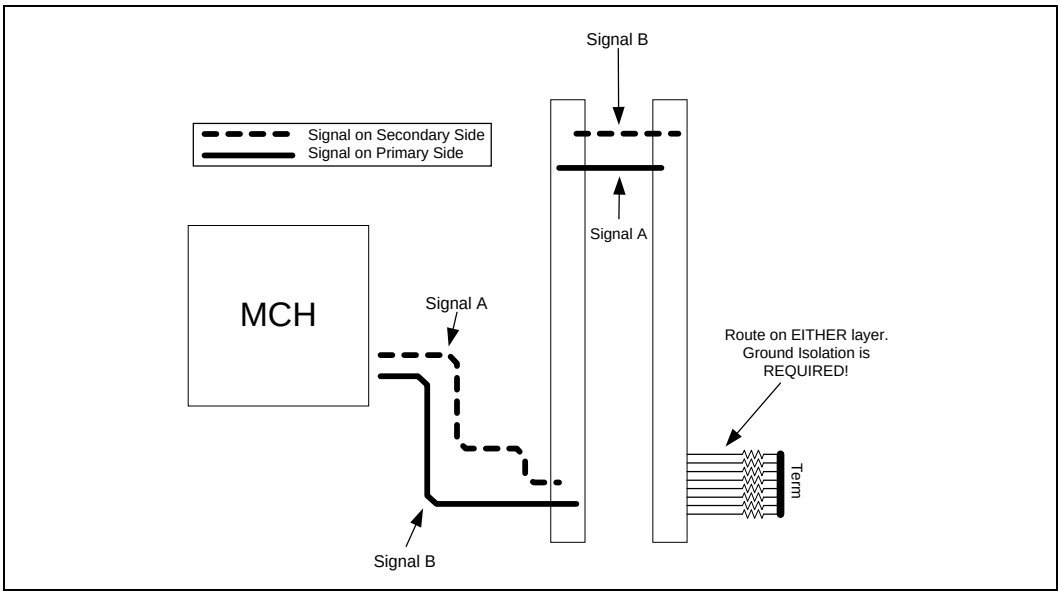


Table 2-4. RSL Routing Layer Requirements

	MCH to 1st RIMM	1st RIMM to 2nd RIMM
Method 1	Primary Side	Secondary Side
Method 2	Secondary Side	Primary Side

2.6.2.6 Length Matching Methods

In order to allow for greater routing flexibility, the RSL signals require *pad-to-pin* length matching between the MCH and the first connector. If the trace lengths are matched between the balls of the MCH and the pin of RIMM connector, the length mismatch between the pad (on the die) and the ball has not been accounted. However, given the *package dimension*, a representation of the length from the pad to the ball, the routing can compensate for this *package mismatch*. Therefore, the *board length mismatch* can be increased.

The RSL channel requires matching trace lengths from pad-to-pin within ±10 mils.

Given these definitions:

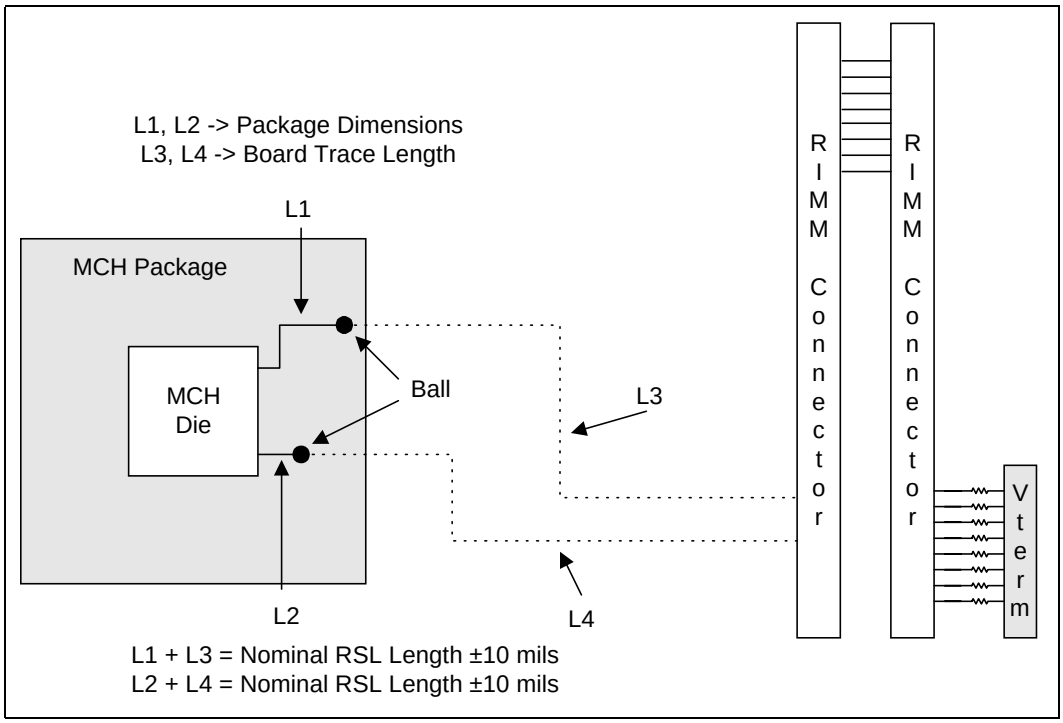
- *Package Dimension:* a representation of the length from the pad to the ball.
- *Board Trace Length:* the trace length on the board.
- *Nominal RSL Length:* the length to which all signals are matched. (note: there is not necessarily a trace that is EXACTLY to nominal length, but all RSL signals must be matched to within ±10mil of a nominal length). The *Nominal RSL Length* is an arbitrary length (within the limits of the routing guidelines) to which all the RSL signals will be matched (within 10 mils).

ALL RSL signals must meet the following equation.

Equation 2-2. RDRAM RSL Signal Trace Length Calculation

Package Dimension + Board Trace Length = Nominal RSL Length ± 10mils

Figure 2-23. RDRAM Trace Length Matching Example



NOTE: Refer to the *Intel® 820 Chipset: Intel® 82820 Memory Controller Hub (MCH)* Datasheet for component package dimensions.

The RDRAM clocks (CTM, CTM#, CFM and CFM#) must be longer than the RDRAM signals due to their increased trace velocity (because they are routed as a differential pair). To calculate the length for each clock, the following formula should be used:

Equation 2-3. RDRAM Clock Signal Trace Length Calculation

Clock Length = Nominal RSL Signal Length (package + board) * 1.021

Using this formula, the clock signals will be 21 mils/inch longer than the Nominal Length. The lengthening of the clock signals, to compensate for their trace velocity change, ONLY applies to routing between the MCH and the first RIMM. The clock signals should be matched in length to the RSL signals between RIMMs. Refer to Chapter 4, “Clocking” for more detailed clock routing guidelines.

The high-speed CMOS signals must be length matched to the RSL signals within 1200 mils (1.2 in) due to a timing requirement between CMOS and RSL signals during NAP Exit and PDN Exit.

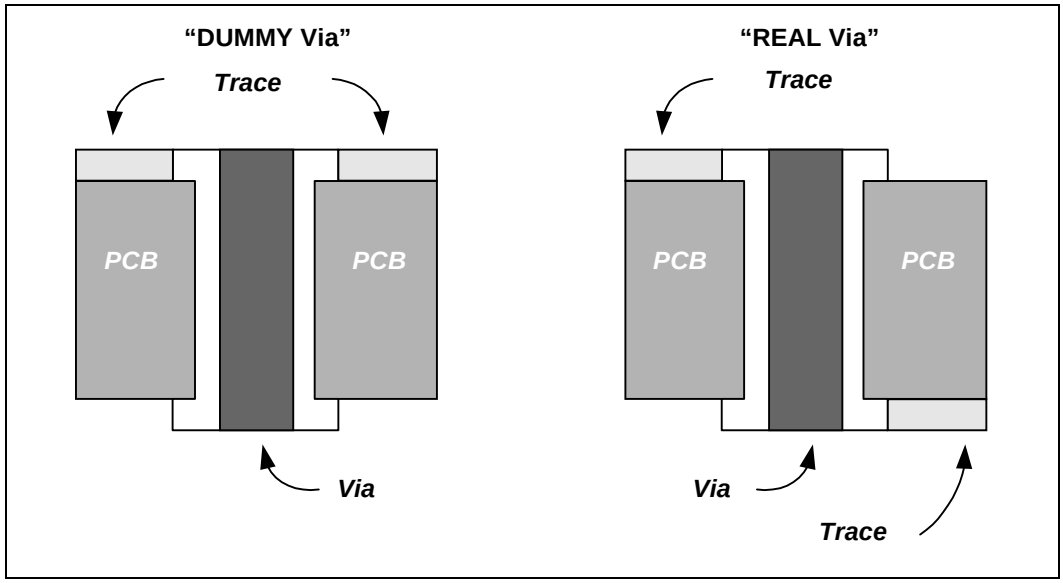
It is necessary to compensate for the slight difference in electrical characteristics between a dummy via and a real via. Refer to the following section for more information on Via Compensation.

2.6.2.7 VIA Compensation

As described in Section 2.8.2, “Strobe Signals” on page 2-44, all signals must have the same number of vias. As a result, each trace will have 1 via (near the BGA pad) because some of the RSL signals must be routed on the bottom of the motherboard. Therefore, it is necessary to place a dummy via on all signals that are routed on the top layer. Because the electrical characteristics of a dummy via do not match the electrical characteristics of a real via exactly, additional compensation must be performed on each signal that has a dummy via. Each signal with a dummy via must have 25 mils of additional trace length. That is: *a real via = a dummy via + 25 mils of trace length*.

This 25 mils of additional trace length must be added to each signal routed on the top layer after length matching, as documented in Section 2.6.2.6, “Length Matching Methods” on page 2-21.

Figure 2-24. "Dummy" Via vs. Real "Via"



2.6.2.8 Length Matching & Via Compensation Example

Table 2-5 can be used to ensure that the RSL signals are the correct length.

Note: 2000 mils was chosen as an EXAMPLE Nominal RSL Length.

Table 2-5. Line Matching and Via Compensation Example[1,2,3,4,5,6,7,8,9,10]

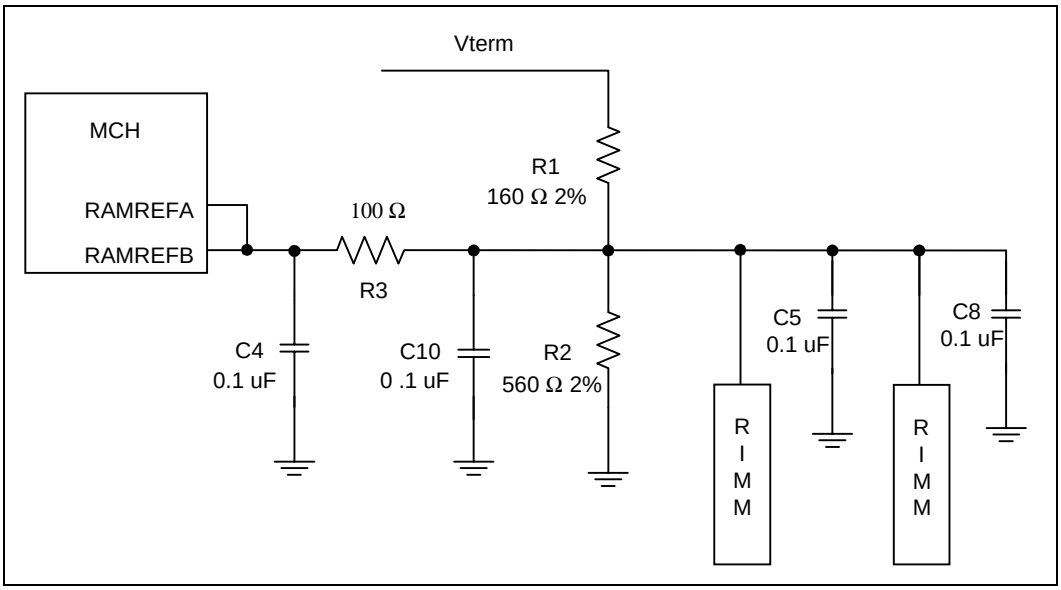
Signal	Ball on MCH	Nominal RSL Length (mils)	Package Dimension (mils)	Motherboard Trace Length when Routed on Bottom (i.e., Real Via)		Motherboard Trace Length when Routed on Top (i.e., Dummy Via)		Recommended To Route On
				Min (mils)	Max (mils)	Min (mils)	Max (mils)	
				Formula A		Formula B		
DQA0	A13	2000	138.14	1851.86	1871.86	1876.86	1896.86	Top
DQA1	C13	2000	19.11	1970.89	1990.89	1995.89	2015.89	Bottom
DQA2	A14	2000	163.16	1826.84	1846.84	1851.84	1871.84	Top
DQA3	C14	2000	39.87	1950.13	1970.13	1975.13	1995.13	Bottom
DQA4	B14	2000	97.54	1892.46	1912.46	1917.46	1937.46	Top
DQA5	C15	2000	62.67	1927.33	1947.33	1952.33	1972.33	Bottom
DQA6	A15	2000	186.11	1803.90	1823.90	1828.90	1848.90	Top
DQA7	C16	2000	95.70	1894.30	1914.30	1919.30	1939.30	Bottom
DQA8	A16	2000	230.20	1759.81	1779.81	1784.81	1804.81	Top
DQB0	C7	2000	39.56	1950.44	1970.44	1975.44	1995.44	Bottom
DQB1	B7	2000	95.83	1894.17	1914.17	1919.17	1939.17	Top
DQB2	C6	2000	63.49	1926.51	1946.51	1951.51	1971.51	Bottom
DQB3	A6	2000	153.69	1836.31	1856.31	1861.31	1881.31	Top
DQB4	C5	2000	97.33	1892.67	1912.67	1917.67	1937.67	Bottom
DQB5	A5	2000	191.43	1798.57	1818.57	1823.57	1843.57	Top
DQB6	B5	2000	152.47	1837.53	1857.53	1862.53	1882.53	Bottom
DQB7	A4	2000	237.71	1752.29	1772.29	1777.29	1797.29	Top
DQB8	C4	2000	138.29	1851.71	1871.71	1876.71	1896.71	Bottom
RQ0	A7	2000	179.49	1810.51	1830.51	1835.51	1855.51	Top
RQ1	C8	2000	27.12	1962.88	1982.88	1987.88	2007.88	Bottom
RQ2	A8	2000	162.21	1827.79	1847.79	1852.79	1872.79	Top
RQ3	C9	2000	5.80	1984.20	2004.20	2009.20	2029.20	Bottom
RQ4	B9	2000	71.70	1918.30	1938.30	1943.30	1963.30	Top
RQ5	A9	2000	133.88	1856.12	1876.12	1881.12	1901.12	Bottom
RQ6	A10	2000	122.20	1867.81	1887.81	1892.81	1912.81	Top
RQ7	C10	2000	0.00	1990.00	2010.00	2015.00	2035.00	Bottom
				FORMULA C		FORMULA D		
CFM	A12	2000	132.37	1906.85		1932.37		Bottom
CFM#	B12	2000	64.63	1976.02		2001.54		Bottom
CTM	B11	2000	56.06	1984.76		2010.29		Top
CTM#	A11	2000	126.34	1913.01		1938.53		Top

NOTES:
1. Signals connecting to the *"A"* side of the RIMM connector (i.e., A1, A2, A3, etc.) should be routed on the top (primary side) of the motherboard;
2. Signals connecting to the "B" side of the RIMM connector should be routed on bottom (solder side).
3. These trace lengths ONLY apply from MCH to the 1st RIMM. All signals must match EXACTLY from RIMM to RIMM.
4. Clock trace lengths include 1.021 trace velocity factor.
5. Formula *A* min: Motherboard Trace = (Nominal RSL Length - Package Dimension) - 10 mil
6. Formula *A* max: Motherboard Trace = (Nominal RSL Length - Package Dimension) + 10 mil
7. Formula *B* min: Motherboard Trace = (Nominal RSL Length - Package Dimension) - 10 mil + 25 mil
8. Formula *B* max: Motherboard Trace = (Nominal RSL Length - Package Dimension) + 10 mil + 25 mil
9. Formula *C*: Motherboard Trace = (Nominal RSL Length - Package Dimension) * 1.021
10. Formula *D*: Motherboard Trace = (Nominal RSL Length - Package Dimension + 25 mil) * 1.021

2.6.3 Direct Rambus* Reference Voltage

The Direct Rambus* reference voltage (RAMREF) must be generated as shown in Figure 2-25. RAMREF should be generated from a typical resistor divider using 2% tolerance resistors. Additionally, RAMREF must be decoupled locally at EACH RIMM connector, at the resistor divider and at the MCH. Finally, as shown in Figure 2-25, a 100 Ω series resistor is required near the MCH. The RAMREF signal should be routed with a 10 mil wide trace.

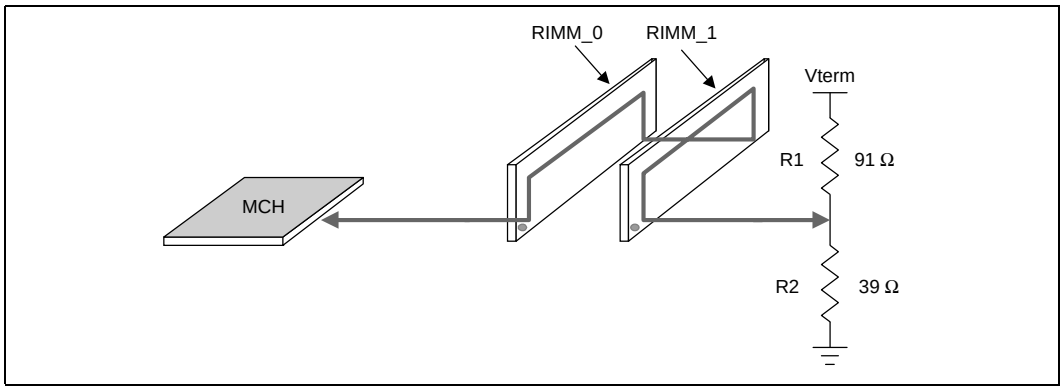
Figure 2-25. RAMRef Generation Example Circuit



2.6.4 High-speed CMOS Routing

- The high-speed CMOS signals (CMD & SCK) must be routed using 28 Ω traces. Using the recommended stackup, these signals will be 18 mils wide.
- The high-speed CMOS signals must be length matched to the RSL signals within 1200 mils (1.2in) due to a timing requirement between CMOS and RSL signals during NAP Exit and PDN Exit.
- The high-speed CMOS signals require termination as shown in Figure 2-26 due to the buffer strengths in the MCH.
- The resistors must be 91 Ω pullup and 39 Ω pulldown; they also must 2% or better for S3 mode reliability. The trace impedances remain 28 Ω.

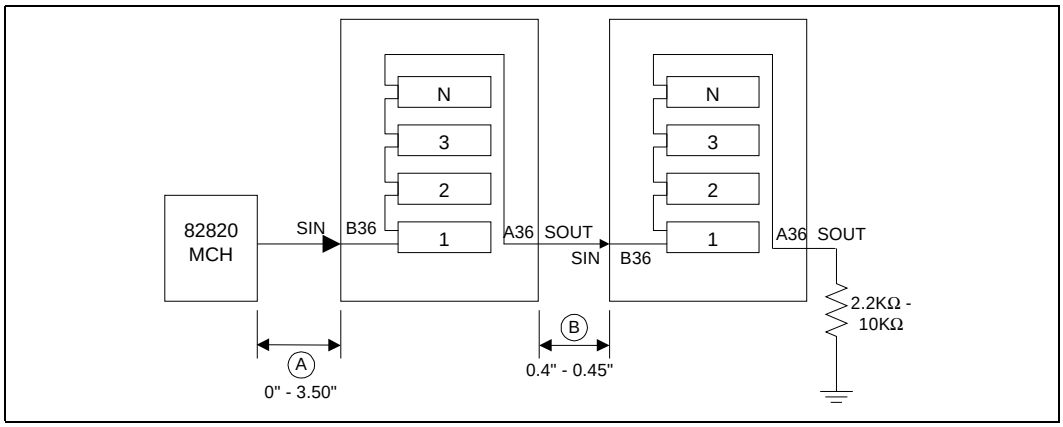
Figure 2-26. High-Speed CMOS Termination



2.6.4.1 SIO Routing

The SIO signal must be routed from RIMM to RIMM as shown in Figure 2-17. The SIO signal requires a 2.2 KΩ – 10 KΩ terminating resistor on the SOUT pin of the last RIMM. SIO is routed with a standard 5 mil wide 60 Ω trace. The motherboard routing lengths for the SIO signal are the same as RSL signals (see Figure 2-17).

Figure 2-27. SIO Routing Example



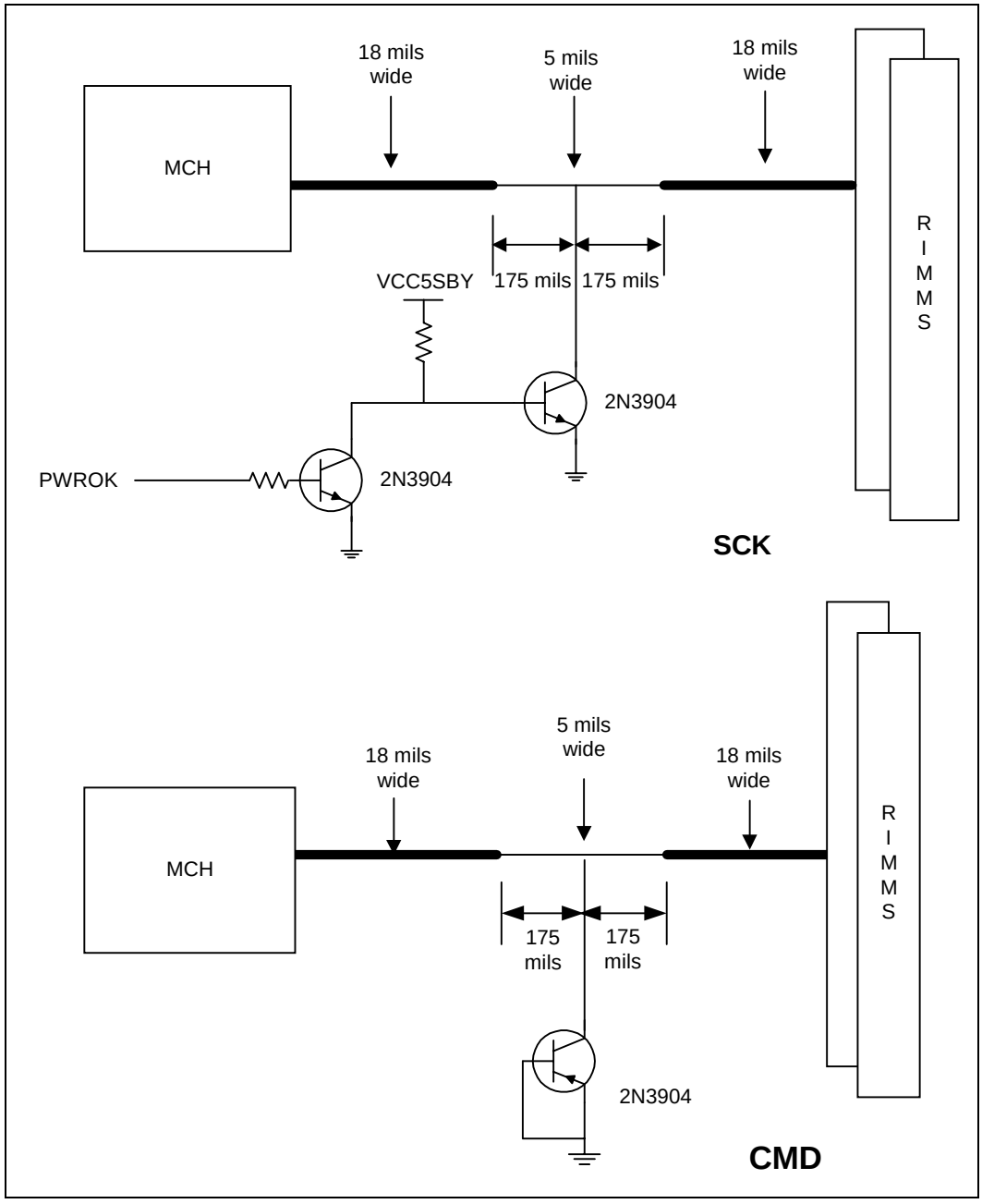
2.6.4.2 Suspend-to-RAM Shunt Transistor

When an Intel® 820 chipset system enters or exits Suspend-to-RAM, power will be ramping to the MCH (i.e., it will be powering-up or powering-down). When power is ramping, the state of the MCH outputs is not guaranteed. Therefore, the MCH could drive the CMOS signals and issue CMOS commands. One of the commands (the only one the RDRAMs would respond to) is the powerdown exit command. To avoid the MCH inadvertently taking the RDRAMs out of power-down due to the CMOS interface being driven during power ramp, the SCK (CMOS clock) signal must be shunted to ground when the MCH is entering and exiting Suspend-to-RAM. This shunting can be accomplished using the NPN transistor shown in circuit shown in Figure 2-28. The transistor should have a Cobo of 4 pf or less (i.e., MMBT3904LT1).

In addition, to match the electrical characteristics on the SCK signal, the CMD signal needs a *dummy* transistor. This transistor's base should be tied to ground (i.e., always turned off).

To minimize impedance discontinuities, the traces for CMD and SCK must have a neckdown from 18 mil traces to 5 mil traces for 175 mils on either side of the SCK/CMD attach point as shown in Figure 2-28.

Figure 2-28. RDRAM CMOS Shunt Transistor



2.6.5 Direct Rambus* Clock Routing

Refer to Chapter 4, "Clocking" for Intel® 820 chipset platform Direct Rambus* clock routing guidelines.

2.6.6 Direct Rambus* Design Checklist

Use the following checklist as a final check to ensure the motherboard incorporates solid design practices. This list is only a reference. For correct operation, all of the design guidelines within this document must be followed.

Table 2-6. Signal List

RSL Signals	High-Speed CMOS Signals	Serial CMOS Signal	Clocks
DQA[8:0] DQB[8:0] RQ[7:0]	CMD SCK	SIO	CTM CTM# CFM CFM#

- Ground Isolation Well Grounded
  - — Via to ground every ½ inch around edge of isolation island
  - — Via to ground every ½ inch between RIMMs
  - — Via to ground every ½ inch between signals (from MCH to first RIMM)
  - — Via between every signal within 100mils of the MCH edge and the connector edge
  - — No unconnected ground floods
  - — All ground isolation at least 10 mils wide
  - — Ground isolation fills between *serpentines*
  - — Ground isolation not *broken* by C-TABs
  - — Ground isolation connects to the ground pins in the middle of the RIMM connectors
  - — Ground isolation vias connect on all 4 layers and should NOT have thermal reliefs
  - — Ground pins in RIMM connector connect on all 4 layers
- Vterm Layout Yields Low Noise
  - — Solid Vterm island is on top layer – do not split this plane
  - — Ground island (for ground side of Vterm caps) is on top
  - — Termination Resistors connect DIRECTLY to the Vterm island on the top layer (without vias)
  - — Decoupling Vterm is CRITICAL!
  - — Decoupling capacitors connect to top layer Vterm island and top layer ground island directly (see layout example)
  - — Use AT LEAST 2 vias per decoupling capacitor in the top layer ground island
  - — Use 2 x 100 uF TANTALUM capacitors to decouple Vterm (Aluminum/Electrolytic capacitors are too slow!)
  - — High-frequency decoupling capacitors MUST be spread-out across the termination island so that all termination resistors are near high-frequency capacitors
  - — 100uF TANTALUM capacitors should be at each end of the Vterm island
  - — 100uF TANTALUM capacitors must be connected to Vterm island directly
  - — 100uF TANTALUM capacitors must have AT LEAST 2 vias/cap to ground

  - — Vterm island should be 50 – 75 mils wide
  - — Vterm island should not be broken
  - — If any RSL signals are routed out of the last RIMM (towards termination) on the bottom side (even for a short distance), ensure Ground Reference Plane (on the third layer) is continuous under the termination resistors/capacitors
  - — Ensure current path for power delivery to the MCH does not go through the Vterm island
- CTM/CTM# Routed Properly
  - — CTM/CTM# are routed differentially from DRCG to last RIMM
  - — CTM/CTM# are ground isolated from DRCG to last RIMM
  - — CTM/CTM# are ground referenced from DRCG to last RIMM
  - — Vias are placed in ground isolation and ground reference every ½”
  - — When CTM/CTM# serpentine together, they MUST maintain EXACTLY 6 mils spacing
- Clean DRCG Power Supply
  - — 3.3V DRCG power flood on the top layer. This should connect to each
  - — High frequency (0.1 uF) capacitors are near the DRCG power pins. One capacitor next to each power pin.
  - — 10uF bulk *tantalum* capacitor near DRCG connected directly to the 3.3V DRCG power flood on the top layer
  - — Ferrite bead isolating DRCG power flood from 3.3V main power also connecting directly to the 3.3VDRCG power flood on the top layer
  - — Use 2 vias on the ground side of each
- Good DRCG Output Network Layout
  - — Series resistors (39 Ω) should be VERY near CTM/CTM# pins
  - — Parallel resistors (51 Ω) should be very near series resistors
  - — CTM/CTM# should be 18mils wide from the CTM/CTM# pins to the resistors
  - — CTM/CTM# should be 14 on 6 routed differential as soon as possible after the resistor network
  - — When not 14 on 6, the clocks should be 18 mils wide
  - — Ensure CTM/CTM# are ground referenced and the ground reference is connected to the ground plane every ½” to 1”
  - — Ensure CTM/CTM# are ground isolated and the ground isolation is connected to the ground plane every ½” to 1”
  - — Ensure 15 pf EMI capacitors to ground are removed (the pads are not necessary and removing the pads provides more space for better placement of other components)
  - — Ensure the 4 pf EMI capacitor is implemented (but do not assemble the capacitor)
- Good RSL Transmission Lines
  - — RSL traces are 18 mils wide
  - — When RSL traces neck down to exit MCH BGA, the minimum width is 15 mils and the neckdown is no longer than 25 mils in length
  - — RSL traces do NOT neckdown when routing into the RIMM connector
  - — If tight serpentining is necessary, 10 mil ground isolation MUST be between serpentine segments (i.e., an RSL signal CAN NOT serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines).
  - — RSL traces do not cross power plane splits. RSL signals must also not be routed *on next to* a power plane splits (e.g., the RSL signals on the 4th layer can not be routed directly below the ground isolation split on the 3rd layer)
  - — Uniform ground isolation flood is exactly 6 mils from the RSL signals at all times

  - — ALL RSL, CMD/SCK and CTM/CTM#/CFM/CFM# signals have CTABs on each RIMM connector pin
  - — All RSL signals are routed adjacent to a ground reference plane. This includes all signals from the last RIMM to the termination. If signals are routed on the bottom from the last RIMM to the termination, the ground reference plane on the 3rd layer MUST extend under these signals AND include the ground side of the Vterm decoupling capacitors.
  - — CTABs must not cross (or be on top of) power plane splits. They must be ENTIRELY referenced to ground.
  - — At least 10 mils ground flood isolation required around ALL RSL signals (ground isolation must be exactly 6 mils from RSL signals). Ground flood recommended for isolation. This ground flood should be as close to the MCH (and the 1st RIMM) as possible. If possible connect the flood to the ground balls/pins on the MCH/connector.
- Clean V_{REF} Routing
  - — Ensure 1 x 0.1 uF capacitor on V_{REF} at each connector
  - — Use 10 mil wide trace (6 mils minimum)
  - — Do not route V_{REF} near high-speed signals
- RSL Routing
  - — All signals must be length matched within ±10 mils of the Nominal RSL Length (note: use the table in the *Intel® 820 chipset: 82820 Memory Controller Hub (MCH)* Datasheet to verify trace lengths). Ensure that signals with a dummy via are compensated correctly.
  - — ALL RSL signals must have 1 via near the MCH BGA pad. Signals routed on the secondary side of the MB will have a “real via” while signals routed on the primary side will have a “dummy via”. Additionally, all signals with a dummy via must have an additional trace length of 25 mils.
  - — “B” side RIMM connector signals are routed on the secondary side of the motherboard. “A” side RIMM connector signals are routed on the primary side of the motherboard.
  - — Signals must “alternate” layers as shown in the following table.

If Signal Routed from MCH to the 1st RIMM on:	Then Route Signal from 1st RIMM to Next RIMM on:
Primary Side	Secondary Side
Secondary Side	Primary Side

- Clock Routing
  - — Clock signals must be routed as a differential pair. The traces must be 14 mils wide and 6 mils apart (with no ground isolation) when they are routed as a differential pair. For very short sections under the MCH and under the 1st RIMM, it will not be possible to route as a differential pair. In these sections, the clocks signals MUST neck up to 18 mils and be ground isolated with at least 10 mils ground isolation.
  - — Clock signals must be length compensated (using the 1.021 length factor described in Section 2.7.3, “2X/4X Timing Domain Routing Guidelines” on page 2-33). Ensure that each clock pair is length matched within ±2 mils.
  - — When clock signals serpentine, they must serpentine together (to maintain differential 14:6 routing).
  - — 22 mils ground isolation required on each side of the differential pair.

2.7 AGP 2.0

For detailed AGP Interface functionality (protocols, rules and signaling mechanisms, etc.) refer to the latest *AGP Interface Specification revision 2.0*, which can be obtained from http://www.agpforum.org. This document focuses only on specific Intel® 820 chipset platform recommendations.

The AGP Interface Specification revision 2.0 enhances the functionality of the original AGP Interface Specification (revision 1.0) by allowing 4X data transfers (4 data samples per clock) and 1.5 volt operation. In addition to these major enhancements, additional performance enhancement and clarifications, such as *fast write* capability, are included in the *AGP Interface Specification, Revision 2.0*. The Intel® 820 chipset is the first Intel chipset that supports the enhanced features of AGP 2.0.

The 4X operation of the AGP interface provides for "quad-pumping" of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses. That is, data is sampled four times during each 66 MHz AGP clock. This means that each data cycle is ¼ of a 15 ns (66 MHz) clock or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2X operation, data is sampled twice during a 66 MHz clock cycle; therefore, the data cycle time is 7.5 ns.

To allow for these high speed data transfers, the 2X mode of AGP operation uses source synchronous data strobing (refer to Section 2.5, "Source Synchronous Strobing" on page 2-5). During 4X operation, the AGP interface uses differential source synchronous strobing.

With data cycle times as small as 3.75 ns, and setup/hold times of 1 ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great, or there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5V) requires even more noise immunity. For example, during 1.5V operation, V_{ilmax} is 570 mv. Without proper isolation, crosstalk could create signal integrity issues.

2.7.1 AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: *1X timing domain signals*, *2X/4X timing domain signals* and *miscellaneous signals*. Each group has different routing requirements. In addition, within the *2X/4X timing domain signals*, there are three sets of signals. All signals in the 2X/4X timing domain must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. However, trace length matching requirements only need to be met within each set of 2X/4X timing domain signals.

Signal groups

- 1X Timing Domain
  - CLK (3.3V)
  - RBF#
  - WBF#
  - ST[2:0]
  - PIPE#
  - REQ#
  - GNT#
  - PAR
  - FRAME#
  - IRDY#
  - TRDY#
  - STOP#
  - DEVSEL#
- 2X/4X Timing Domain

  Set #1
  - AD[15:0]
  - C/BE[1:0]#
  - AD_STB0
  - AD_STB0# (used in 4X mode ONLY)

  Set #2
  - AD[31:16]
  - C/BE[3:2]#
  - AD_STB1
  - AD_STB1# (used in 4X mode ONLY)

  Set #3
  - SBA[7:0]
  - SB_STB
  - SB_STB# (used in 4X mode ONLY)
- Miscellaneous, Async
  - USB+
  - USB-
  - OVRCNT#
  - PME#
  - TYPDET#
  - PERR#
  - SERR#
  - INTA#
  - INTB#

Table 2-7. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1X	Associated Strobe in 2X	Associated Strobes in 4X
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1X mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this section the term *data* refers to AD[31:0], C/BE[3:0]# and SBA[7:0]. The term *strobe* refers to AD_STB[1:0], AD_STB#[1:0], SB_STB and SB_STB#. When the term *data* is used, it is referring to one of the three sets of data signals. When the term *strobe* is used, it is referring to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (*1X timing domain signals*, *2X/4X timing domain signals* and *miscellaneous signals)* will be addressed separately.

2.7.2 1X Timing Domain Routing Guidelines

- The AGP 1X timing domain signals (refer to Signal Groups previously shown) have a maximum trace length of 7.5 inches. This maximum applies to ALL of the signals listed as 1X timing domain signals in Signal Groups section.
- AGP 1X timing domain signals can be routed with 5 mil minimum trace separation.
- There are no trace length matching requirements for 1X timing domain signals.

2.7.3 2X/4X Timing Domain Routing Guidelines

These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

The maximum line length and length mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6”) and the long AGP interfaces (e.g., > 6” and < 7.25”) are documented separately. The maximum length allowed for the AGP interface is 7.25 inches.

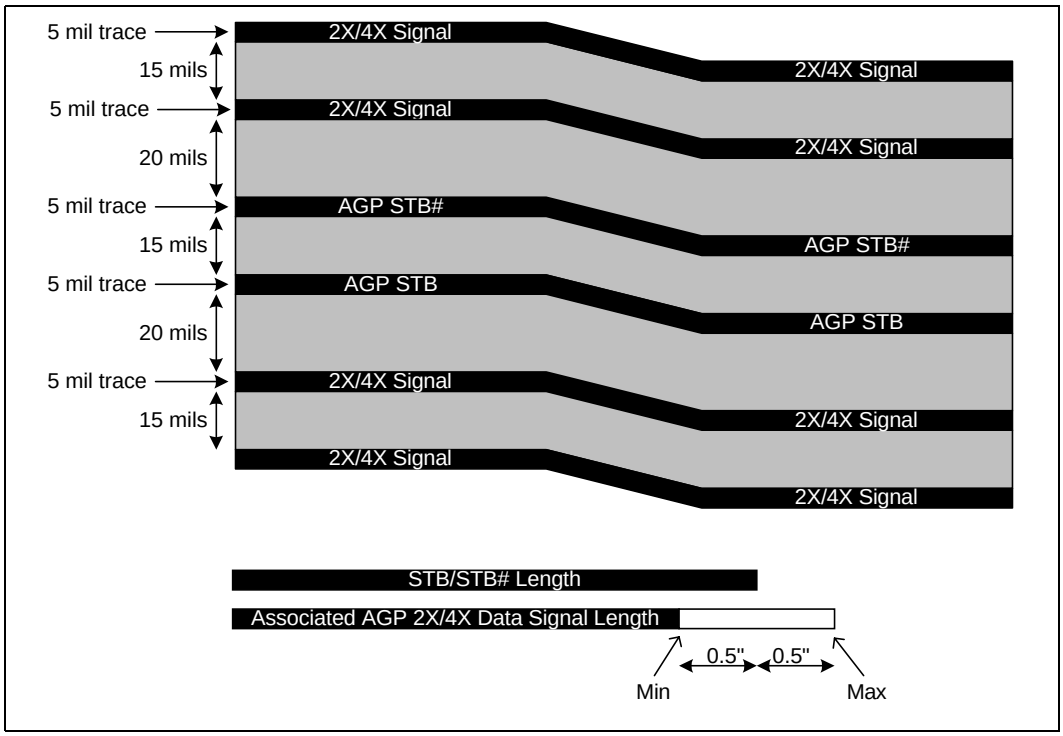
Interfaces < 6”

If the AGP interface is less than 6 inches, a minimum 1:3 trace spacing is required for 2X/4X lines (data and strobes). These 2X/4X signals must be matched their associated strobe within ±0.5 inches. These guidelines are for designs that require less than 6 inches between the AGP connector and the MCH.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3” long, the data signals which are associated to those strobe signals (e.g., AD[15:0] and C/BE[2:0]#), can be 4.8” to 5.8” long. Another strobe set (e.g., SB_STB and SB_STB#) could be 4.2” long, and the data signals which are associated to those strobe signals (e.g., SBA[7:0]), can be 3.7” to 4.7” long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1” (i.e., a strobe and its compliment must be the same length within 0.1”).

Figure 2-29. AGP 2X/4X Routing Example for Interfaces < 6”



Interfaces > 6” and < 7.25”

Longer lines have more crosstalk; therefore, to reduce skew, longer line lengths require a greater amount of spacing between traces. For line lengths greater than 6 inches and less than 7.25 inches, 1:4 routing is required for all data lines and strobes. For these designs, the line length mismatch must be less than ±0.125” within each signal group (between all data signals and the strobe signals).

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5” long, the data signals which are associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#), can be 6.475” to 6.625” long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2” long, and the data signals that are associated with those strobe signals (e.g., SBA[7:0]), can be 6.075” to 6.325” long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them.

This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1” (i.e., a strobe and its compliment must be the same length within 0.1”).

All AGP Interfaces

The 2X/4X Timing Domain Signals can be routed with 5 mil spacing when breaking out of the MCH. The routing must widen to the documented requirements within 0.3” of the MCH package. When matching trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

Reduce line length mismatch to insure added margin. In order to reduce trace to trace coupling (cross talk), separate the traces as much as possible. All signals in a signal group should be routed on the same layer. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.

2.7.4 AGP 2.0 Routing Summary

Table 2-8. AGP 2.0 Routing Summary[1,2]

Signal	Maximum Length	Trace Spacing (5 mil traces)	Length Mismatch	Relative To	Notes
1X Timing Domain	7.5”	5 mils	No Requirement	N/A	None
2X/4X Timing Domain Set#1	7.25”	20 mils	±0.125”	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	7.25”	20 mils	±0.125”	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	7.25”	20 mils	±0.125”	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length
2X/4X Timing Domain Set#1	6”	15 mils[1]	±0.5”	AD_STB0 and AD_STB0#	AD_STB0, AD_STB0# must be the same length
2X/4X Timing Domain Set#2	6”	15 mils[1]	±0.5”	AD_STB1 and AD_STB1#	AD_STB1, AD_STB1# must be the same length
2X/4X Timing Domain Set#3	6”	15 mils[1]	±0.5”	SB_STB and SB_STB#	SB_STB, SB_STB# must be the same length

NOTES:
1. Each strobe pair must be separated from other signals by at least 20 mils
2. These guidelines apply to board stackups with 10% impedance tolerance

2.7.5 AGP Clock Routing

The maximum total AGP clock skew (between the MCH and the graphics component) is 1 ns for all data transfer modes. This 1 ns includes skew and jitter which originates on the motherboard, add-in card, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but at all points on the clock edge that fall in the switching range. The 1 ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew (the motherboard designer shall determine how the 0.9 ns is allocated between the board and the synthesizer). For Intel® 820 chipset platform AGP clock routing guidelines, refer to Chapter 4, “Clocking”.

2.7.6 General AGP Routing Guidelines

The following routing guidelines are recommended for an optimal system design. The main focus of these guidelines is to minimize signal integrity problems on the AGP interface of the 82820 MCH. The guidelines below are not intended to replace thorough system validation on Intel® 820 chipset based products.

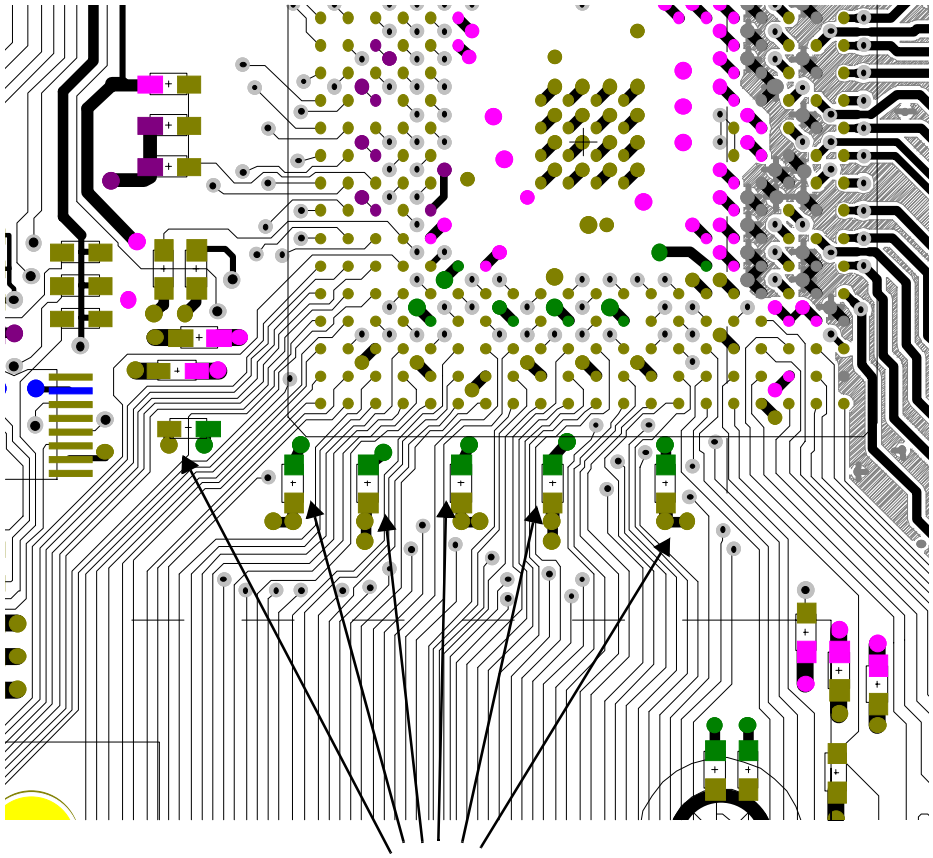
Recommendations

Decoupling

- For VDDQ decoupling, a minimum of six (6) 0.01 uF capacitors are required and at least four (4) must be within 70 mils of the outer row of balls on the MCH. (see Figure 2-30).
- Evenly distribute placement of decoupling capacitors among the AGP interface signal field.
- Use a low ESL ceramic capacitor (e.g., 0603 body type, X7R dielectric).
- In addition to the minimum decoupling capacitors, bypass capacitors should be placed at vias that transition AGP signals from one reference signal plane to another. *On a typical four layer PCB design the signals transition from one side of the board to the other.*
- One extra 0.01 uF capacitor is required per 10 vias. The capacitor should be placed as close to the center of the via field as possible.
- Ensure that the AGP connector is well decoupled as described in the *AGP Design Guide, Revision 1.0 (Section 1.5.3.3).*

Note: To add the decoupling capacitors close as possible to the MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short a distance as possible (1” maximum).

Figure 2-30. Top Signal Layer



Ground Reference

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the MCH to an AGP connector (or to an AGP video controller if implemented as a "down" solution) utilizing a minimum number of vias on each net; AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT# and ST[2:0].

In addition to the minimum signal set listed above, it is strongly recommended that half of all your AGP signals be reference to ground depending on board layout. An ideal design would have the complete AGP interface signal field referenced to ground.

The recommendations above are not specific to any particular PCB stackup, but are applied to all Intel® Chipset designs.

2.7.7 VDDQ Generation and TYPEDET#

AGP specifies two separate power planes (VCC and VDDQ). VCC is the core power for the graphics controller. VCC is **always** 3.3V. VDDQ is the interface voltage. In AGP 1.0 implementations VDDQ was also 3.3V. For the designer developing an AGP 1.0 motherboard, there is no distinction between VCC and VDDQ as both are tied to the 3.3V power plane on the motherboard.

AGP 2.0 requires that these power planes be separate. In conjunction with the 4X data rate, the AGP 2.0 Interface Specification provides for low-voltage (1.5V) operation. The AGP 2.0 Specification implements a TYPEDET# (type detect) signal on the AGP connector that determines the operating voltage of the AGP 2.0 interface (VDDQ). The motherboard must provide either 1.5V or 3.3V to the add-in card depending on the state of the TYPEDET# signal (refer to Table 2-9. The 1.5V low-voltage operation applies ONLY to the AGP interface (VDDQ); VCC is **always** 3.3V.

Note: The motherboard provides 3.3V to the Vcc pins of the AGP connector. If the graphics controller needs a lower voltage, then the add-in card must regulate the 3.3V VCC voltage to the controller's requirements. The graphics controller may ONLY power AGP I/O buffers with the VDDQ power pins.

The TYPEDET# signal indicates whether the AGP 2.0 interface operates 1.5 volts or 3.3 volts. If TYPEDET# is floating (no connect) on an AGP add-in card, the interface is 3.3 volts. If TYPEDET# is shorted to ground, the interface is 1.5 volts.

Table 2-9. TYPDET#/VDDQ Relationship

TYPEDET# (on add-in card)	VDDQ (supplied by MB)
GND	1.5V
N/C	3.3V

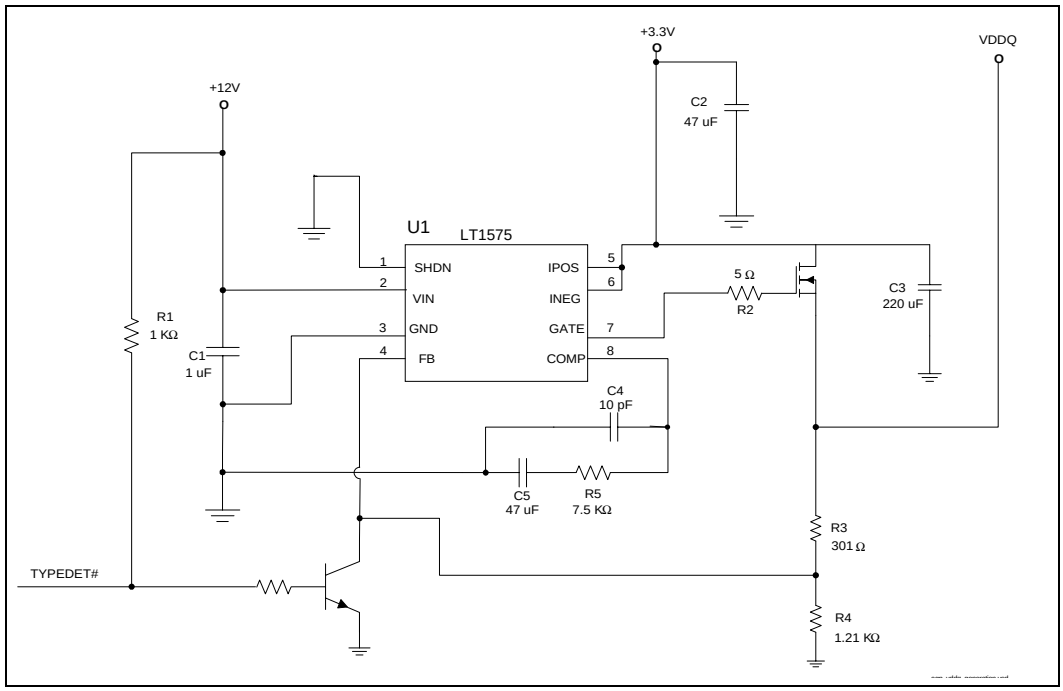
As a result of this requirement, the motherboard must provide a *flexible* voltage regulator. This regulator must supply the appropriate voltage to the VDDQ pins on the AGP connector. For specific design recommendations, refer to the schematics in Appendix A, "Reference Design Schematics: Uni-Processor" and Appendix B, "Reference Design Schematics: Dual-Processor". VDDQ generation and AGP V_{REF} generation must be considered together. Before developing VDDQ generation circuitry, refer to the AGP 2.0 Interface Specification.

Figure 2-31 demonstrates one way to design the VDDQ voltage regulator. This regulator is a linear regulator with an external, low R_{DS-ON} FET. The source of the FET is connected to 3.3V. This regulator will convert 3.3V to 1.5V or pass 3.3V depending on the state of TYPEDET#. If a linear regulator is used, it must draw power from 3.3V (not 5V) in order to control thermals (i.e., 5V regulated down to 1.5V with a linear regulator will dissipate approximately 7W at 2A). Because it must draw power from 3.3V and, in some situations, must simply pass that 3.3V to VDDQ (when a 3.3V add-in card is placed in the system), the regulator MUST use a low R_{dson} FET.

AGP 1.0 modified $VDDQ3.3_{min}$ to 3.1V. Using an ATX power supply; the $3.3V_{min}$ is 3.168V. Therefore, 68 mV of drop is allowed across the FET at 2A. This corresponds to a FET with an R_{dson} of 34 mW.

How does the regulator switch? The feedback resistor divider is set to 1.5V. When a 1.5V card is placed in the system, the transistor is off and the regulator regulates to 1.5V. When a 3.3V card is placed in the system, the transistor is on, and the feedback is pulled to ground. When this happens, the regulator drives to gate of the FET to nearly 12V. This turns the FET on and passes 3.3V - 2A * R_{DS-ON} to VDDQ.

Figure 2-31. AGP VDDQ Generation Example Circuit



2.7.8 V_{REF} Generation for AGP 2.0 (2X and 4X)

V_{REF} generation for AGP 2.0 will be different depending on the AGP card type used. The 3.3V AGP cards generate V_{REF} locally (i.e., they have a resistor divider on the card that divides VDDQ down to V_{REF}) as shown in Figure 2-32. To account for potential differences between VDDQ and GND at the MCH and graphics controller, 1.5V cards use source generated V_{REF} (i.e., the V_{REF} signal is generated at the graphics controller and sent to the MCH, and another V_{REF} is generated at the MCH and sent to the graphics controller). Refer to Figure 2-32.

Both the graphics controller and the MCH are required to generate V_{REF} and distribute it through the connector (1.5V add-in cards only). There are two pins defined on the AGP 2.0 universal connector to allow this V_{REF} passing. These pins are:

- V_{REF}GC - Vref from the graphics controller to the chipset
- V_{REF}CG - Vref from the chipset to the graphics controller

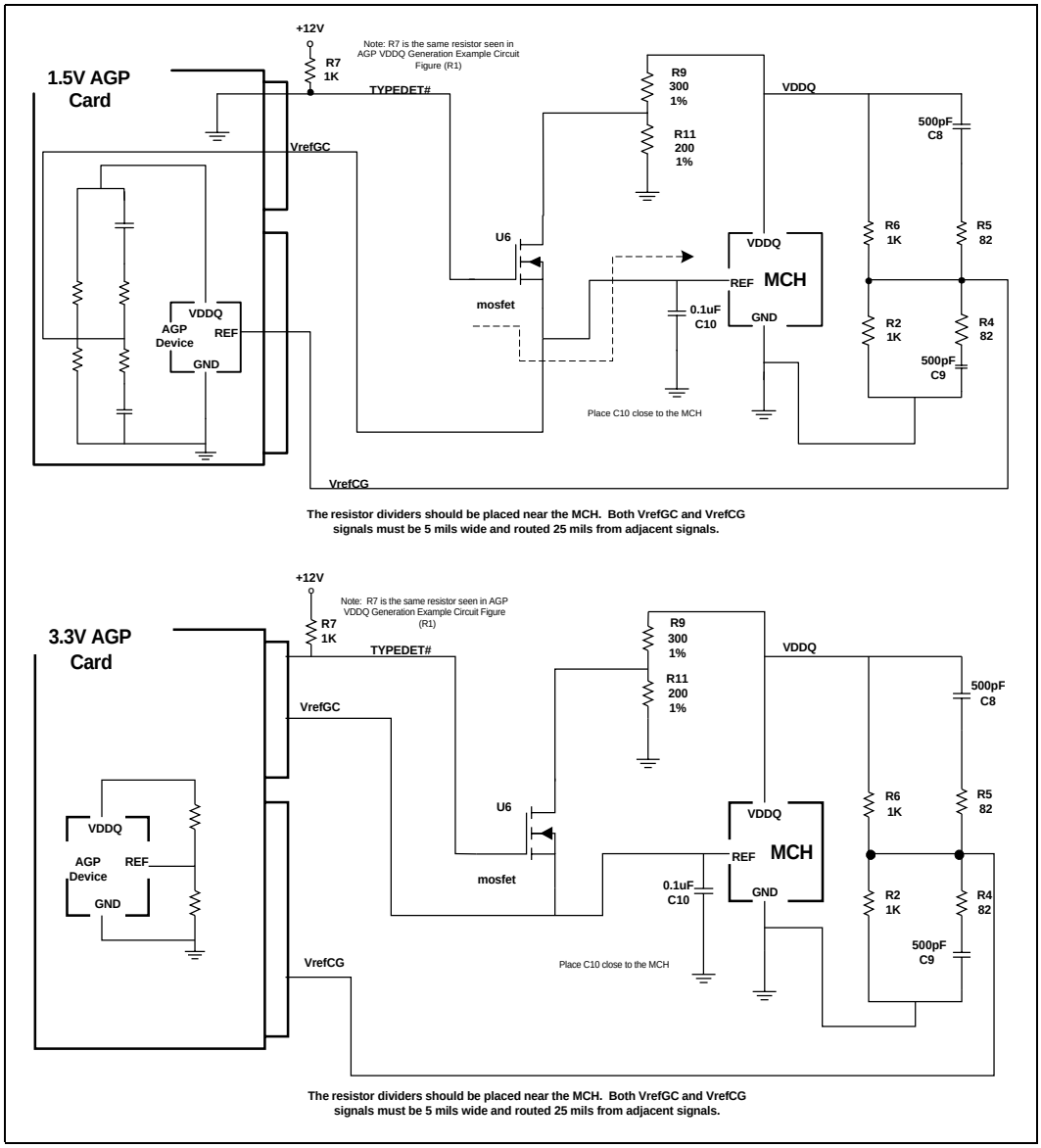
To preserve the common mode relationship between the V_{REF} and data signals, it is important the routing of the two Vref signals must be matched in length to the strobe lines within 0.5 inches on the motherboard and within 0.25 inches on the add-in card.

The voltage divider networks consists of AC and DC elements as shown in the figure.

The V_{REF} divider network should be placed as close to the AGP interface as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the V_{REF} signals must be a minimum of 25 mils to reduce cross-talk and maintain signal integrity.

During 3.3V AGP 2.0 operation, V_{REF} must be 0.4VDDQ. However, during 1.5V AGP 2.0 operation, Vref must be 0.5VDDQ. This requires a flexible voltage divider for V_{REF}. Various methods of accomplishing this exist, and one such example is shown in Figure 2-32.

Figure 2-32. AGP 2.0 VREF Generation & Distribution



The flexible V_{REF} divider shown in Figure 2-32 uses a FET switch to switch between the locally generated V_{REF} (for 3.3V add-in cards) and the source generated V_{REF} (for 1.5V add-in cards).

Usage of the source generated V_{REF} at the receiver is optional and is a product implementation issue which is beyond the scope of this document.

2.7.9 Compensation

The MCH AGP interface supports resistive buffer compensation (RCOMP). Tie the GRCOMP pin to a 40 Ω 2% (or 39 Ω 1%) pull-down resistor (to ground) via a 10 mil wide, very short (<0.5”) trace.

2.7.10 AGP Pull-ups

AGP control signals require pull-up resistors to VDDQ on the motherboard to ensure they contain stable values when no agent is actively driving the bus. The signals requiring pull-up resistors are:

- 1X Timing Domain Signals
  - FRAME#
  - TRDY#
  - IRDY#
  - DEVSEL#
  - STOP#
  - SERR#
  - PERR#
  - RBF#
  - PIPE#
  - REQ#
  - WBF#
  - GNT#
  - ST[2:0]

  It is critical that these signals are pulled up to VDDQ (NOT 3.3V).

  The trace stub to the pull-up resistor on 1X timing domain signals should be kept to less than 0.5 inch to avoid signal reflections from the stub.

  The strobe signals require pull-up/pull-downs on the motherboard to ensure they contain stable values when no agent is driving the bus.

  Note: INTA# and INTB# should be pulled to 3.3V – not VDDQ.

- 2X/4X Timing Domain Signals
  - AD_STB[1:0] (pull-up to VDDQ)
  - SB_STB (pull-up to VDDQ)
  - AD_STB[1:0]# (pull-down to ground)
  - SB_STB# (pull-down to ground)

  The trace stub to the pull-up/pull-down resistor on 2X/4X timing domain signals should be kept to less than 0.1 inch to avoid signal reflections from the stub.

  The pull-up/pull-down resistor value requirements are shown in the table below:

Rmin	Rmax
4 KΩ	16 KΩ

  The recommended AGP pull-up/pull-down resistor value is 8.2 KΩ.

2.7.10.1 AGP Signal Voltage Tolerance List

The following signals on the AGP interface are 3.3V tolerant during 1.5V operation:

- PME#
- INTA#
- INTB#
- GPERR#
- GSERR#
- CLK
- RST

The following signals on the AGP interface are 5V tolerant (refer to the USB specification):

- USB+
- USB-
- OVRCNT#

The following signal is a special AGP signal. It is either Grounded or No Connected on an AGP card.

- TYPEDET#

Note: **All other signals on the AGP interface are in the VDDQ group. They are not 3.3V tolerant during 1.5V AGP operation.**

2.7.11 Motherboard / Add-in Card Interoperability

Currently, there are three AGP connectors:

- 3.3V AGP connector
- 1.5V AGP connector
- Universal AGP connector.

To maximize add-in flexibility, implementing the universal connector in Intel® 820 chipset based system is strongly recommended. All add-in cards are either 3.3V or 1.5V cards. Due to timings, 4X transfers at 3.3V are not allowed.

Table 2-10. Connector/Add-in Card Interoperability

	1.5V Connector	3.3V Connector	Universal Connector
1.5V Card	Yes	No	Yes
3.3V Card	No	Yes	Yes

Table 2-11. Voltage/Data Rate Interoperability

	1X	2X	4X
1.5V VDDQ	Yes	Yes	Yes
3.3V VDDQ	Yes	Yes	No

2.8 Hub Interface

The MCH and ICH ball assignments have been optimized to simplify hub interface routing. It is recommended that the hub interface signals be routed directly from the MCH to the ICH on the top signal layer (they do not need to be run through vias) (refer to Figure 2-4).

The hub interface is broken into two signal groups: data signals and strobe signals. These groups are:

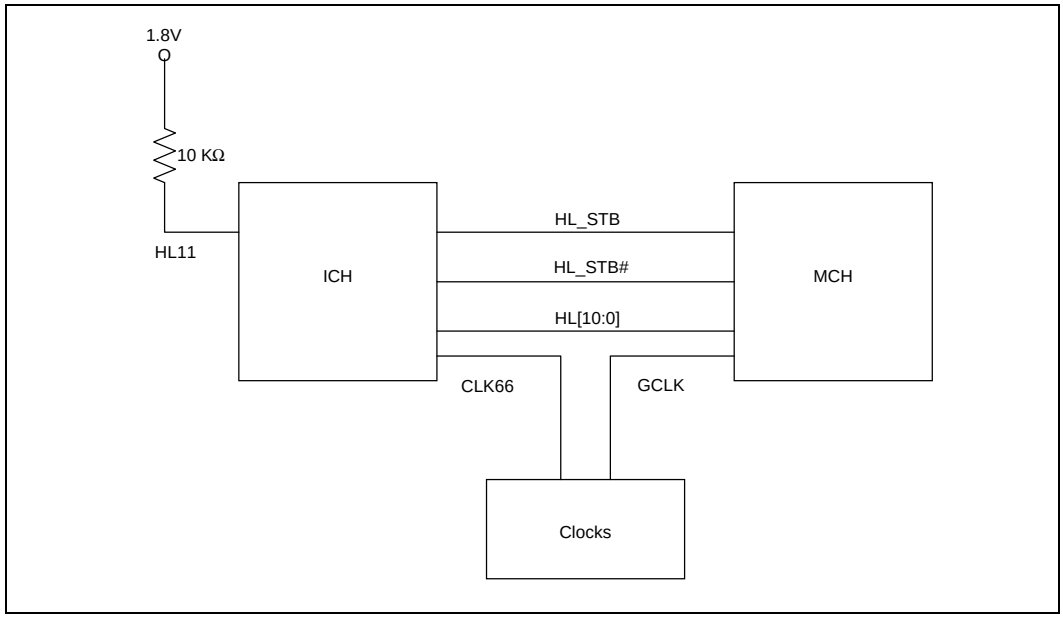
- Data Signals
  - HL[10:0]
- Strobe Signals
  - HL_STB
  - HL_STB#

Note: HL_STB/HL_STB# is a differential strobe pair.

There are no pull-ups or pull-downs required on the hub interface.

Each signal must be routed such that it meets the guidelines documented for the signal group to which it belongs.

Figure 2-33. Hub Interface Signal Routing Example



2.8.1 Data Signals

The Hub interface data signals (HL[10:0]) should be routed 5 on 20. These signals can be routed 5 on 15 for navigation around components or mounting holes. In order to break-out of the MCH uBGA and the ICH uBGA, the hub interface data signals can be routed 5 on 5. The signals must be separated to 5 on 20 within 300 mil of the uBGA package.

The maximum trace length for the hub interface data signals is 7". These signals must each be matched within ±0.1" of the HL_STB and HL_STB# signals.

2.8.2 Strobe Signals

Due to their differential nature, the hub interface strobe signals should be 5 mils wide and routed 20 mils apart. This strobe pair should be a minimum of 20 mils from any adjacent signals. The maximum length for the strobe signals is 7" and the two strobes must be the same length. Additionally, the trace length for each data signal must be matched to the trace length of the strobes with ±0.1".

2.8.3 HREF Generation/Distribution

HREF is the hub interface reference voltage. It is 0.5 * 1.8V = 0.9V ±2%. It can be generated using a single HREF divider or locally generated dividers (as shown in Figure 2-34 and Figure 2-35). The resistors should be equal in value and rated at 1% tolerance (to maintain 2% tolerance on 0.9V). The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. The recommended range for the resistor value is from minimum 100 ohm to maximum 1K ohm (300 ohm shown in example).

The single HREF divider should not be located more than 4" away from either MCH or ICH. If the single HREF divider is located more than 4" away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HREF divider should be bypassed to ground at each component with a 0.01 uF capacitor located close to the component HREF pin. If the reference voltage is generated locally, the bypass capacitor needs to be close to the component HREF pin.

Figure 2-34. Single Hub Interface Reference Divider Circuit

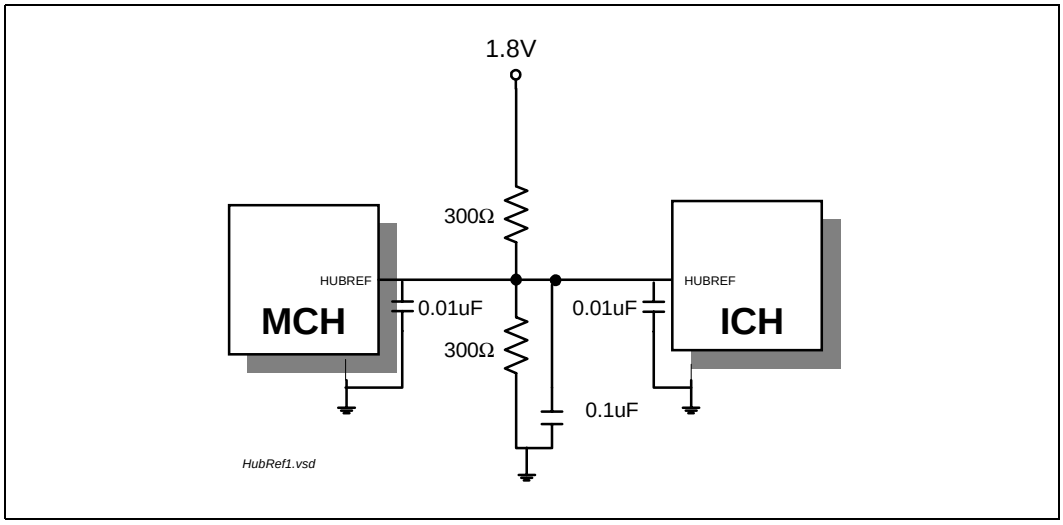
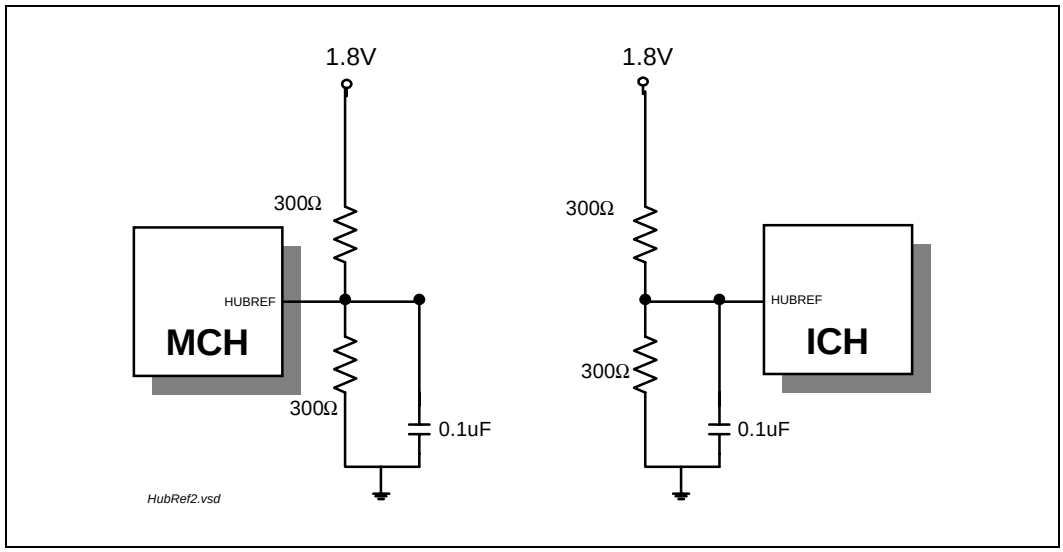


Figure 2-35. Locally generated Hub Interface Reference Dividers



2.8.4 Compensation

There are two options for the ICH hub interface compensation (HLCOMP). HLCOMP is used by the ICH to adjust buffer characteristics to specific board characteristics. Refer to the ICH Datasheet for details on compensation. It can be used as either Impedance Compensation (ZCOMP) or Resistive Compensation (RCOMP). The guidelines are below:

- **RCOMP:** Tie the COMP pin to a 40 Ω 2% (or 39 Ω 1%) pull-up resistor (to 1.8V) via a 10 mil wide, very short (<0.5”) trace.
- **ZCOMP:** The COMP pin must be tied to a 10 mil trace that is AT LEAST 18” long. This trace must be unterminated and care should be taken when routing the signal to avoid crosstalk (15–20 mil separation between this signal and any adjacent signals is recommended). This signal may not cross power plane splits.

The MCH also has a hub interface compensation pin. This signal (HLCOMP) can be routed using either the RCOMP method or ZCOMP method described for the ICH.

2.9 System Bus Design

2.9.1 100/133 MHz System Bus

First, determine the approximate location of the processor and the chip set on the base board. An example topology is shown in Figure 2-36. This example "star" topology is valid for 133 MHz and 100 MHz 2-way processor/Intel® 820 chipset designs. The 82820 MCH should be placed electrically in the center of the bus. The SC242 connectors should be placed on either end of the bus to allow the processors to terminate each end.

Table 2-12 below provides segment descriptions and length recommendations for the investigated topology shown in Figure 2-36. Segment lengths are defined at the pins of the devices or components. For 2-way processor / Intel® 820 chipset designs, a termination card must be placed in the unused slot when only one processor is populated. This is necessary to ensure signal integrity requirements are met.

Figure 2-36. Intel® Pentium® III Processor Dual Processor Configuration

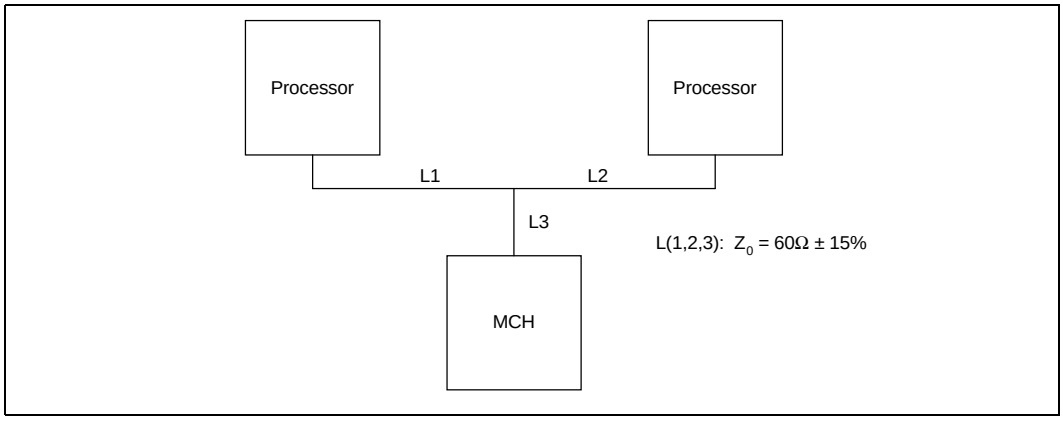
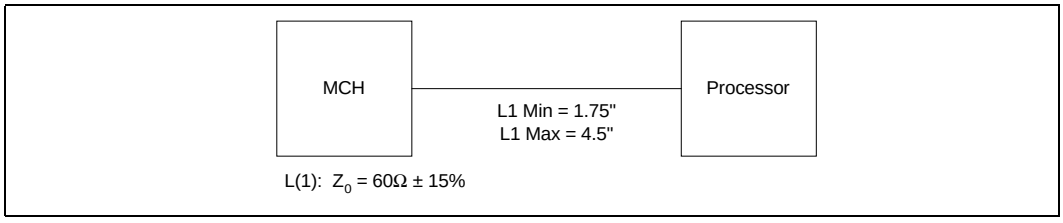


Table 2-12. Segment Descriptions and Lengths for Figure 2-36

Segment	Description	Min length (inches)	Max length (inches)
L1	SC242 connector to Centerpoint	1.5	3.0
L2	SC242 connector to Centerpoint	1.5	3.0
L3	Chip set breakout stub	0.0	1.5
L1+L3 or L2+L3	SC242 distance from MCH	2.0	4.5
L1 + L2	SC242 spacing		5.5

Figure 2-37 shows the topology and trace lengths required for single processor designs.

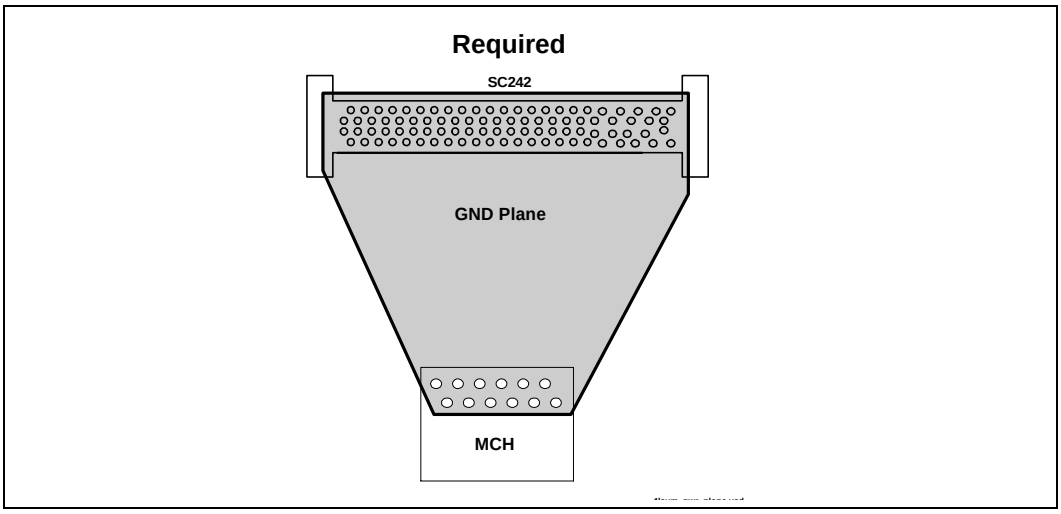
Figure 2-37. Intel® Pentium® III Processor Uni-Processor Configuration



2.9.2 System Bus Ground Plane Reference

All system bus signals must be referenced to GND to provide optimal current return path. The ground reference must be continuous from the MCH to the SC242 connector. This may require a GND reference island on the plane layers closest to the signals. Any split in the ground island will provide a sub-optimal return path. In a 4 layer board, this will require the VCCID island to be on an outer signal layer. Figure 2-38 shows a four layer motherboard power plane with ground reference for system bus signals.

Figure 2-38. Ground Plane Reference (Four Layer Motherboard)



2.10 S.E.C.C. 2 Grounding Retention Mechanism (GRM)

Intel is enabling a new S.E.P.P. (Single Edge Processor Package) style retention mechanism which will provide a grounding path for the heatsink on processors in the S.E.C.C. 2 package. This solution is referred to as the S.E.C.C.2 (Single Edge Contact Cartidge 2) Grounding Retention Mechanism (GRM). OEMs who choose to utilize this new solution will need to add grounding pads on the primary side of the motherboard which will interface with the enabled GRM. If the motherboard or heat sink do not have the proper interfaces, the GRM may not be utilized to its full ability and damage could occur to the motherboard.

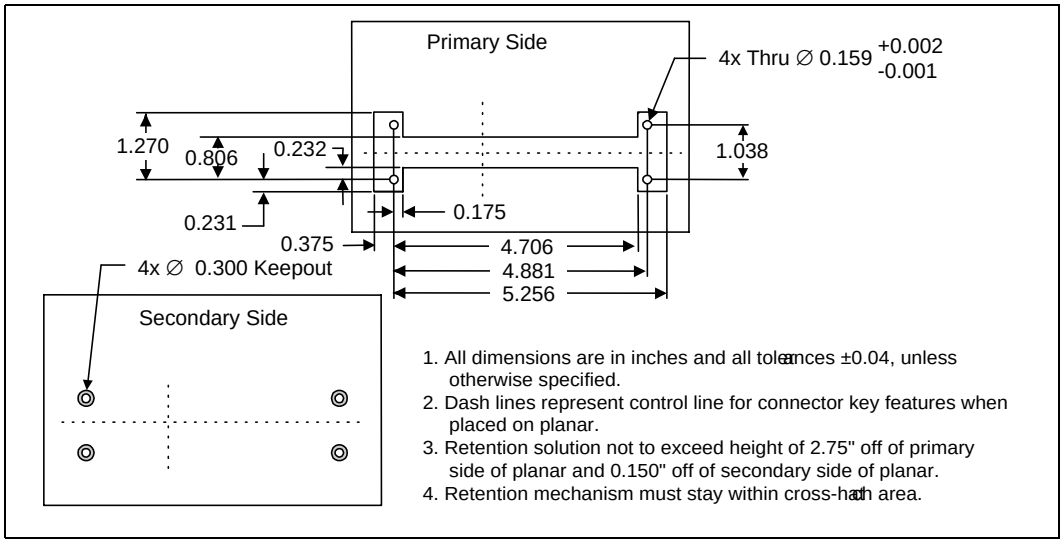
The most notable interface requirement to accommodate the GRM is the addition of grounding pads around two of the Retention Mechanism (RM) mounting holes within the existing RM keep-out zone on the motherboard. The other interface is a contact area on the heat sink flanges. The interface size and locations for the motherboard are discussed in detail further in this section.

The reference design GRM is asymmetric, and requires 0.159” mounting holes. To minimize the impact to trace routing, only two ground pads are required. This makes it necessary to key the GRM to prevent the ground clips from being installed on the soldermask instead of the grounding pads. This keying is accomplished by making the GRM asymmetric. The requirement for the 0.159” mounting holes is for the supported plastic fastener attachment mechanism.

Motherboard Interfaces

Figure 2-39 shows the Hole Locations and Keepout Zones For Support Components (from the motherboard surface to 0.100” above the motherboard surface.).

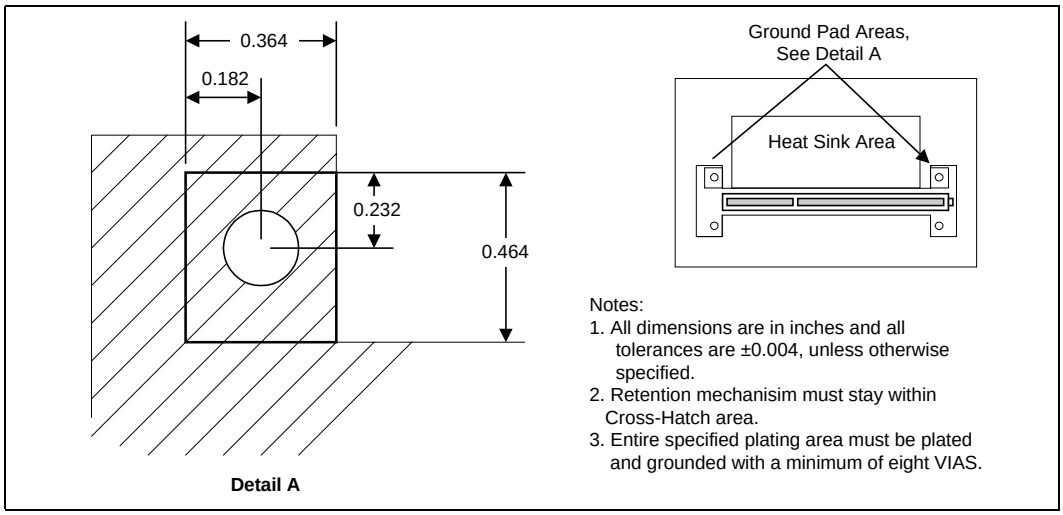
Figure 2-39. Hole Locations and Keepout Zones For Support Components[1,2]



NOTES:
1. The dashed lines represent the centerlines for the connector keying features.
2. Drawing not to scale

Figure 2-40 shows the dimensions of the grounding pad needed to ground the heat sink.

Figure 2-40. Grounding Pad Dimensions for the SECC2 GRM



NOTE: Drawing not to scale.

It is not recommended to use the GRM without the minimum size ground pads in the correct locations. If the GRM is used without the correct pads, then there is a high risk that the metal clip that grounds to the motherboard will be touching the solder mask on the top layer of the board, and possibly short out traces immediately beneath the solder mask, resulting in board failure. The required thickness of the pad is less than 0.001” (using 1/2 oz. copper).

2.11 Processor CMOS Pullup Values

Table 2-13 contains the pullup values for the Intel® Pentium® III processor with the Intel® 820 chipset. This table supports both single and dual processor configurations.

Table 2-13. Processor and 82820 MCH Connection Checklist[1,2]

CPU Pin	UP Pin Connection (CPU0)	DP Pin Connection (CPU1)
AGTL+ Signals		
A[35:3]# [1]	Connect A[31:3]# to MCH. Leave A[35:32]# as N/C (not supported by chipset).	Connect A[31:3]# to 2nd processor
ADS# [1]	Connect to MCH	Connect to 2nd processor
AERR#	Leave as N/C (not supported by chipset).	Leave as N/C
AP[1:0]#	Leave as N/C (not supported by chipset).	Leave as N/C
BERR#	Leave as N/C (not supported by chipset).	Leave as N/C
BINIT#	Leave as N/C (not supported by chipset).	Leave as N/C
BNR# [1]	Connect to MCH	Connect to 2nd processor
BP[3:2]#	Leave as N/C	Leave as N/C
BPM[1:0]	Leave as N/C	Leave as N/C
BPRI# [1]	Connect to MCH	Connect to 2nd processor
BREQ0# (BR0#)	10 Ω pull down to GND	See and
BREQ1# (BR1#)	Leave as N/C	See and
D[63:0]# [1]	Connect to MCH	Connect to 2nd processor
DBSY# [1]	Connect to MCH	Connect to 2nd processor
DEFER# [1]	Connect to MCH	Connect to 2nd processor
DEP[7:0]#	Leave as N/C (not supported by chipset).	Leave as N/C
DRDY# [1]	Connect to MCH	Connect to 2nd processor
HIT# [1]	Connect to MCH	Connect to 2nd processor
HITM# [1]	Connect to MCH	Connect to 2nd processor
LOCK# [1]	Connect to MCH	Connect to 2nd processor
REQ[4:0]# [1]	Connect to MCH	Connect to 2nd processor
RESET# [1]	Connect to MCH, 240 Ω series resistor to ITP	Connect to 2nd processor
RP#	Leave as N/C (not supported by chipset).	Leave as N/C
RS[2:0]# [1]	Connect to MCH	Connect to 2nd processor
RSP#	Leave as N/C (not supported by chipset).	Leave as N/C
TRDY# [1]	Connect to MCH	Connect to 2nd processor

Table 2-13. Processor and 82820 MCH Connection Checklist[1,2] (Continued)

CPU Pin	UP Pin Connection (CPU0)	DP Pin Connection (CPU1)
CMOS Signals		
A20M#	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
FERR#	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
FLUSH#	150 Ω pull up to Vcc2.5 (not used by chipset).	Connect to 2nd processor
IERR#	150 Ω pull up to Vcc2.5 if tied to custom logic or leave as N/C (not used by chipset).	Connect to 2nd processor
IGNNE#	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
INIT#	150 Ω pull up to Vcc2.5, connect to ICH and FWH Flash BIOS	Connect to 2nd processor
LINT0/INTR	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
LINT1/NMI	150 Ω pull up to Vcc2.5, connect to ICH	Connect to 2nd processor
PICD[1:0]	150 Ω pull up to Vcc2.5, connect to ICH	Two 300–330 Ω pull ups to Vcc2.5 located at each end of trace. Connect to 2nd processor
PREQ#	~200–330 Ω pull up to Vcc2.5, connect to ITP pin 16	~200–330 Ω pull up to Vcc2.5, connect to ITP pin 20
PWRGOOD	150–330 Ω pull up to 2.5V, output from the PWRGOOD logic	Connect to 2nd processor
SLP#	150 Ω pull up to Vcc2.5, connect to ICH	
SMI#	150 Ω pull up to Vcc2.5, connect to ICH	
STPCLK#	150 Ω pull up to Vcc2.5, connect to ICH	
THERMTRIP#	150 Ω pull up to Vcc2.5 and connect to power off logic or ASIC, or leave as N/C	Connect to 2nd processor. Could tie separately to a monitoring ASIC.
TAP Signals		
PRDY#	150 Ω pull up to V_{TT}, 240 Ω series resistor to ITP pin 18	150 Ω pull up to V_{TT}, 240 Ω series resistor to ITP pin 22
TCK	1k Ω pull up to Vcc2.5, 47 Ω series resistor to ITP pin 5	Each processor should receive a separately buffered copy of TCK from the ITP. Tank circuit is optional for signal integrity. See
TDO	150 Ω pull up to Vcc2.5 and connect to ITP 10	TDO of CPU1 is connected to the ITP TDO pin 10. Pull up both sets of TDI/TDO nets as described.
TDI	~150–330 Ω pull up to Vcc2.5 and connect to ITP pin 8	TDI of CPU0 is connected to the ITP pin 8, TDI of CPU1 is connected to TDO of CPU0. Pull up both sets of TDI/TDO nets as described.
TMS	1 KΩ pull up to Vcc2.5, 47 Ω series resistor to ITP pin 7	Each processor should receive a separately buffered copy of TMS from the ITP. Tank circuit is optional for signal integrity. See
TRST#	~680 Ω pull down, connect to ITP pin 12	Connect to 2nd processor

Table 2-13. Processor and 82820 MCH Connection Checklist[1,2] (Continued)

CPU Pin	UP Pin Connection (CPU0)	DP Pin Connection (CPU1)
Clock Signals		
BCLK	Connect to CK133. 22 – 33 Ω series resistor (Though OEM needs to simulate based on driver characteristics). To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to the MCH and processor.	Use separate BCLK from TAP and CPU0, or use ganged clock. Terminate as described.
PICCLK	Connect to CK133. 22 – 33 Ω series resistor (Though OEM needs to simulate based on driver characteristics)	Use separate PICCLK from CPU0. Terminate as described.
Other Signals		
BSEL0	100/133 MHz support: 220 Ω pull up to 3.3V, connected to PWRGOOD logic such that a logic low on BSEL0 negates PWRGOOD	Connect to 2nd processor
BSEL1	220 Ω pull up to 3.3V, connect to CK133 SEL133/100# pin. Connect to MCH HL10 pin via 8.2 KΩ series resistor.	Connect to 2nd processor
EMI[5:1]	Tie to GND. Zero ohm resistors are an option instead of direct connection to GND.	Implement in same manner as CPU0.
SLOTOCC#	Tie to GND, leave it N/C, or could be connected to powergood logic to gate system from powering on if no processor is present. If used, 1 KΩ – 10 KΩ pull up to any voltage.	Implement in same manner as CPU0.
TESTHI	1 K –100 KΩ pull up to Vcc2.5 If a legacy design pulls this up to VCC_{CORE}, use a 1 KΩ – 10 KΩ pull up	Implement in same manner as CPU0.
VID[4:0]	Connect to on-board VR or VRM. For on-board VR, 10 KΩ pull up to power-solution compatible voltage required (usually pulled up to input voltage of the VR). Some of these solutions have internal pull-ups. Optional override (jumpers, ASIC, etc.) could be used. May also connect to system monitoring device.	Implement in same manner as CPU0. CPU0 and CPU1 should have different VR/VRMs.
Power		
VCC_{CORE}	Connect to core voltage regulator. Provide high & low frequency decoupling.	Implement in same manner as CPU0.
V_{TT}	Connect to 1.5V regulator. Provide high and low frequency decoupling.	Implement in same manner as CPU0.
No Connects		
Reserved	The following pins must be left as no-connects: A16, A47, A88, A113, A116, B12, B20, B76, and B112.	Implement in same manner as CPU0.

NOTES:
1. For single processor designs, the AGTL+ bus can be dual-ended or single-ended termination based on simulation results. Single-ended termination is provided by the processor.
2. This checklist supports Intel® Pentium® II processors at all current speeds, Intel® Pentium® III processors to a FMB guideline of 19.3A, and future Intel® Pentium® III processors to the current FMB guideline of 18.4A.

Figure 2-41. TCK/TMS Implementation Example for DP Designs

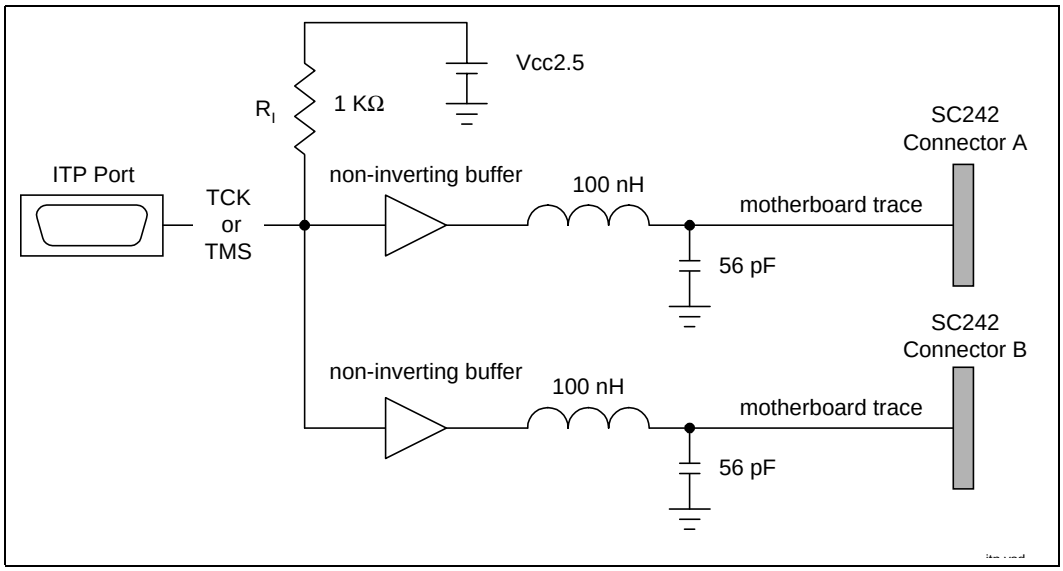


Table 2-14. Bus Request Connection Scheme for DP Intel® 820 Chipset Designs

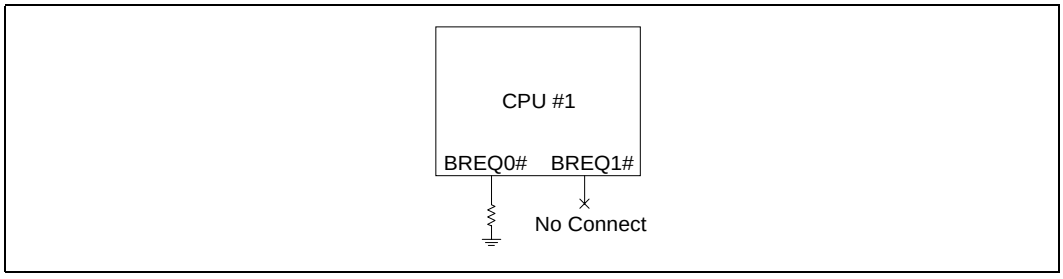
Bus Signal	Agent 0 Pins	Agent 1 Pins
BREQ0#	BR0#	BR1#
BREQ1#	BR1#	BR0#

2.12 Additional Host Bus Guidelines

BREQ Pins

UP Systems: For uni-processor systems, the BREQ0 pin should be pulled down to ground through a 10 Ω resistor. The BREQ1 pin should be left as a no-connect.

Figure 2-42. Single Processor BREQ Strapping Requirements



DP Systems: For dual processor systems, BREQ0# (to one of the processors) needs to be driven for *arbitration ID* strapping. Refer to Figure 2-43 for an example of the BREQ connections in a DP system. It is a requirement that the on-board logic tri-state BREQ0# after the arbitration ID strapping is complete. Additionally, BREQ0# and BREQ1# are *high-speed AGTL+* signals and the loading characteristics of the on-board logic must be considered even when the logic is tri-stated.

Figure 2-43. Dual-Processor BREQ Strapping Requirements

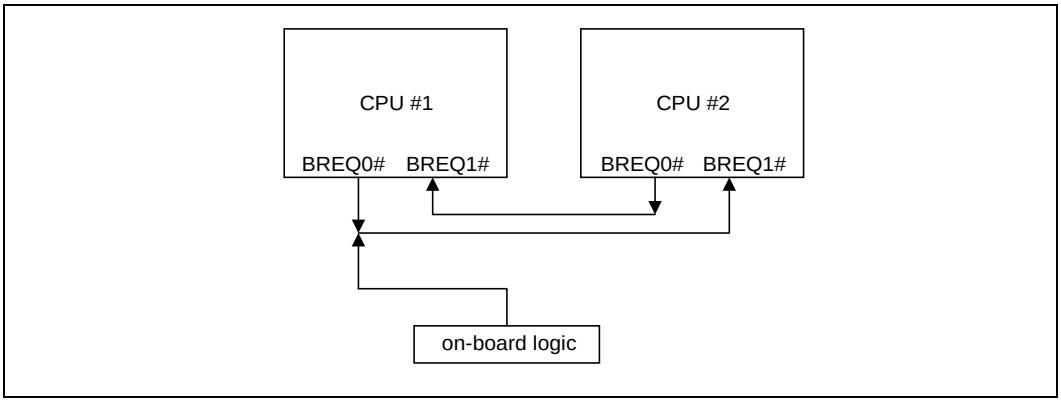
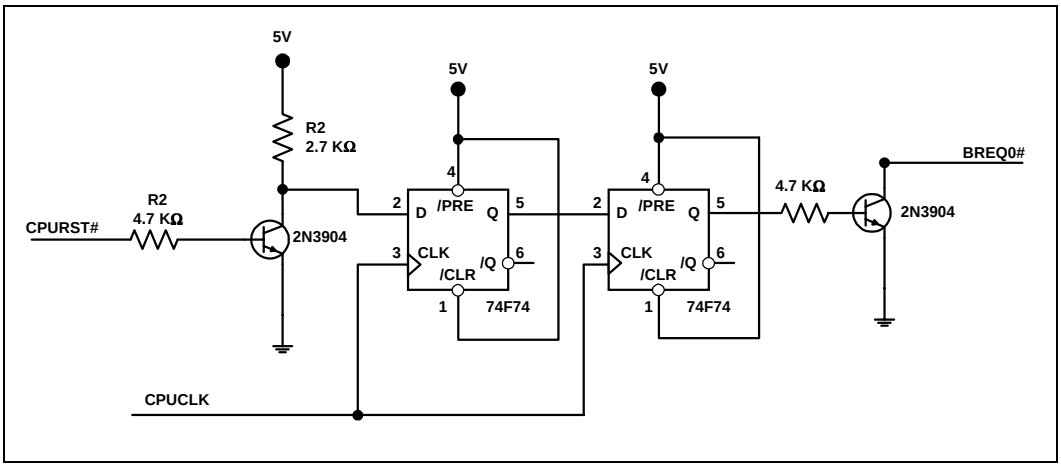


Figure 2-44. BREQ0# Circuitry for DP Systems



This circuit holds BREQ0 low for two clocks after the deassertion of reset. The 2N3904 connected to BREQ0 should be connected to the BREQ0 AGTL trace with a very short stub. Additionally, the series current limiting resistor on CPURESET should be attached to the CPURESET trace with a very short stub.

External Circuit Recommendation for HA7 Strapping for IOQ Depth of 1

For debug purpose, the external logic to set the IOQ depth of 1 on the front side bus may be needed. Do not add this circuit for production since overall system performance will be degraded. The external logic for HA7# strapping is very similar to the BREQ0 strapping that is described in the previous section.

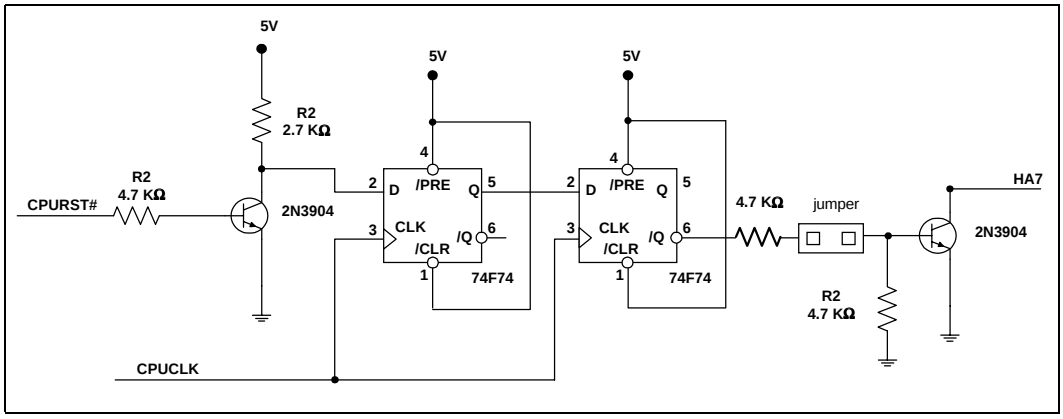
The timing requirement of HA7# strapping is also similar to BREQ0 strapping for the hold time after the deassertion of RESET# (RSTIN# signal from MCH). The value of the strapping needs to be held for a minimum of 2 host clocks after the deassertion of RSTIN#. Refer to the latest version of the processor datasheets for complete description on the timing requirement.

The recommendation for the layout and the schematic example are shown below. Layout guidelines are:

- Place the transistor and stub as close as possible to MCH (or place the transistor pad on top of trace)
- The max stub for transistor is less than 0.25”
- The recommended loading of transistor is less than 5 pf.
- For dual processor design, the stub is recommended to place on the stub of the MCH and as close as possible to the MCH, and is less than 0.25”

Note: This circuit is only recommended for the debug situation that requires to set the IOQ depth equal to 1. For the production, do not add this circuit, since the overall system performance will be degraded. Also, Intel does not guarantee the above layout recommendation will work under the worst case condition.

Figure 2-45. HA7# Strapping Option Example Circuit (For Debug Purposes Only)



In-Target Probe (ITP)

It is important that all of the processor electrical characteristic requirements are met. It is recommended that prototype boards implement the ITP connector.

Logic Analyzer Interface (LAI)

Note that 1 KΩ resistors that are used to pull-up several processor signals in the schematics in Appendix A, “Reference Design Schematics: Uni-Processor” and Appendix B, “Reference Design Schematics: Dual-Processor” (e.g., HINIT#, IGNNE#, SMI#, etc.) preclude use of the Intel Pentium III processor LAI. The Intel Pentium III processor LAI will function correctly with these 1 KΩ pull-up resistors.

Minimizing Crosstalk on the AGTL+ Interface

The following general rules will minimize the impact of crosstalk in the high speed AGTL+ bus design:

- Maximize the space between traces. Maintain a minimum of 0.010” between traces wherever possible. It may be necessary to use tighter spacings when routing between component pins.
- Avoid parallelism between signals on adjacent layers.
- Since AGTL+ is a low signal swing technology, it is important to isolate AGTL+ signals from other signals by at least 0.025”. This will avoid coupling from signals that have larger voltage swings, such as 5V PCI.
- Select a board stack-up that minimizes the coupling between adjacent signals.
- Route AGTL+ address, data and control signals in separate groups to minimize crosstalk between groups. The Pentium III processor uses a split transaction bus. In a given clock cycle, the address lines and corresponding control lines could be driven by a different agent than the data lines and their corresponding control lines.

Additional Considerations

- Distribute V_{TT} with a wide trace. A 0.050” minimum trace is recommended to minimize DC losses. Route the V_{TT} trace to all components on the host bus. Be sure to include decoupling capacitors. Guidelines for V_{TT} distribution and decoupling are contained in “Slot 1 Processor Power Distribution Guidelines.”
- Place resistor divider pairs for V_{REF} generation at the MCH component. No V_{REF} generation is needed at the processor(s). V_{REF} is generated locally on the processor. Be sure to include decoupling capacitors. Guidelines for V_{REF} distribution and decoupling are contained in “Slot 1 Processor Power Distribution Guidelines.”
- Special Case AGTL+ signals for simulation: There are six AGTL+ signals that can be driven by more than one agent simultaneously. These signals may require extra attention during the layout and validation portions of the design. When a signal is asserted (driven low) by two agents on the same clock edge, the two falling wave fronts will meet at some point on the bus. This can create a large undershoot, followed by ringback which may violate the ringback specifications. This “wired-OR” situation should be simulated for the following signals: AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

2.13 Ultra ATA/66

This section contains guidelines for connecting and routing the ICH IDE interface. The ICH has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH has integrated the 33 Ω series resistors that have been typically required on the IDE data signals running to the two ATA connectors.

The IDE interface can be routed with 5 mil traces on 5 mil spaces, and must be less than 8 inches long (from ICH to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5” shorter than the longest IDE signal (on that channel).

Cable

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6” away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **ICH Placement:** The ICH must be placed equal to or less than 8 inches from the ATA connector(s).
- **PC99 requirement:** Support Cable Select for master-slave configuration is a system design requirement for Microsoft* PC99. CSEL signal needs to be pulled down at the host side by using a 470 Ω pull-down resistor for each ATA connector.

2.13.1 Ultra ATA/66 Detection

The Intel® 820 chipset supports many Ultra DMA modes including ATA/66. The Intel® 820 chipset needs to determine the installed IDE device mode and the type of cable to configure its own hardware and software to support it.

A new IDE cable is required for Ultra ATA/66. This cable is an 80 conductor cable; however the 40 pin connectors do not change. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground… All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40 pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

To determine if ATA/66 mode can be enabled, the Intel® 820 chipset requires the system BIOS to attempt to determine the cable type used in the system. The BIOS does this in one of two ways:

- Host Side Detection
- Device Side Detection

If the BIOS detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the Intel® 820 chipset and the IDE device. Otherwise, the BIOS can only enable modes that do not require an 80-conductor cable (e.g., Ultra ATA/33 Mode).

After determining the Ultra DMA mode to be used, the BIOS will configure the Intel® 820 chipset hardware and software to match the selected mode.

2.13.2 Ultra ATA/66 Cable Detection

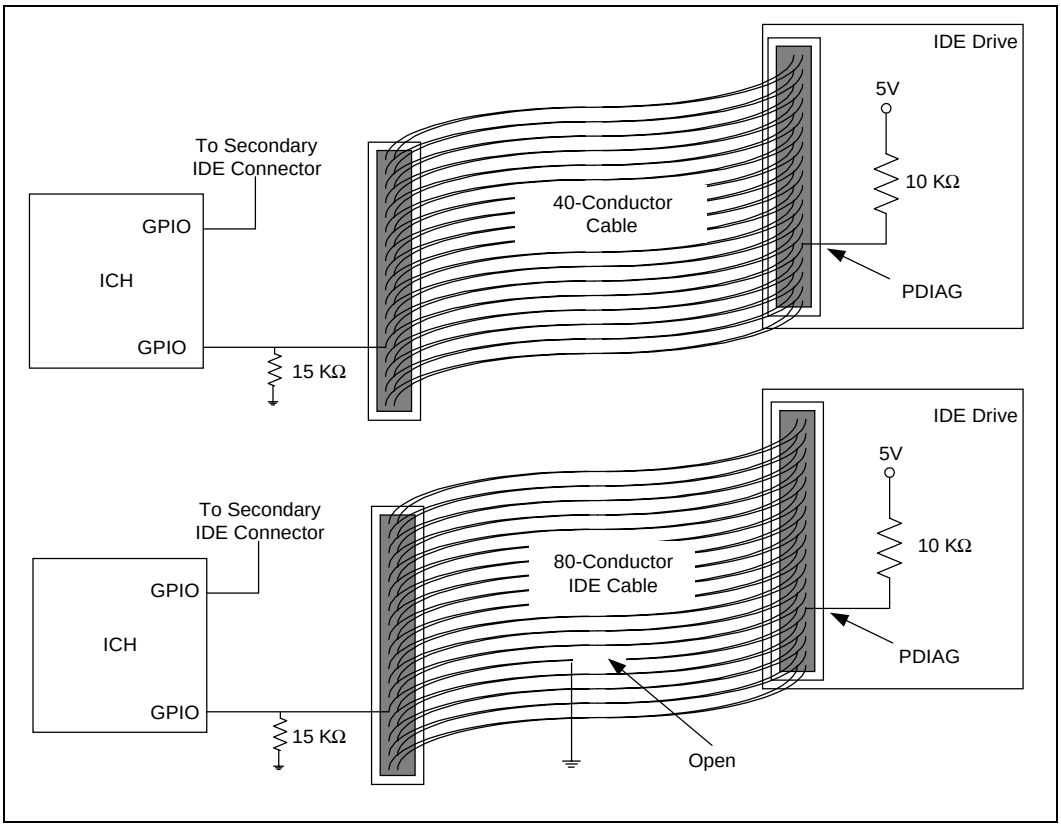
The Intel® 820 chipset can use two methods to detect the cable type. Each mode requires a different motherboard layout.

Host-Side Detection (BIOS Detects Cable Type Using GPIOs)

Host side detection requires the use of two GPI pins (1 per IDE controller). The proper way to connect the PDIAG/CBLID signal of the IDE connector to the host is shown in Figure 2-46. All IDE devices have a 10 KΩ pull-up resistor to 5 volts. The GPI and GPIO pins on the ICH and GPI pins on the FWH Flash BIOS are not 5 volt tolerant. This requires a resistor divider so that 5 volts will not be driven to the ICH or FWH Flash BIOS pins. The proper value of the series resistor is 15 KΩ (as shown in Figure 2-46). This creates a 10 KΩ / 15 KΩ resistor divider and produces approximately 3 volts for a logic high.

This mechanism allows the host, after diagnostics, to sample PDIAG/CBLID. If PDIAG/CBLIB is high then there is 40-conductor cable in the system and ATA modes 3 and 4 should not be enabled. If PDIAG/CBLID is low then there is an 80-conductor cable in the system.

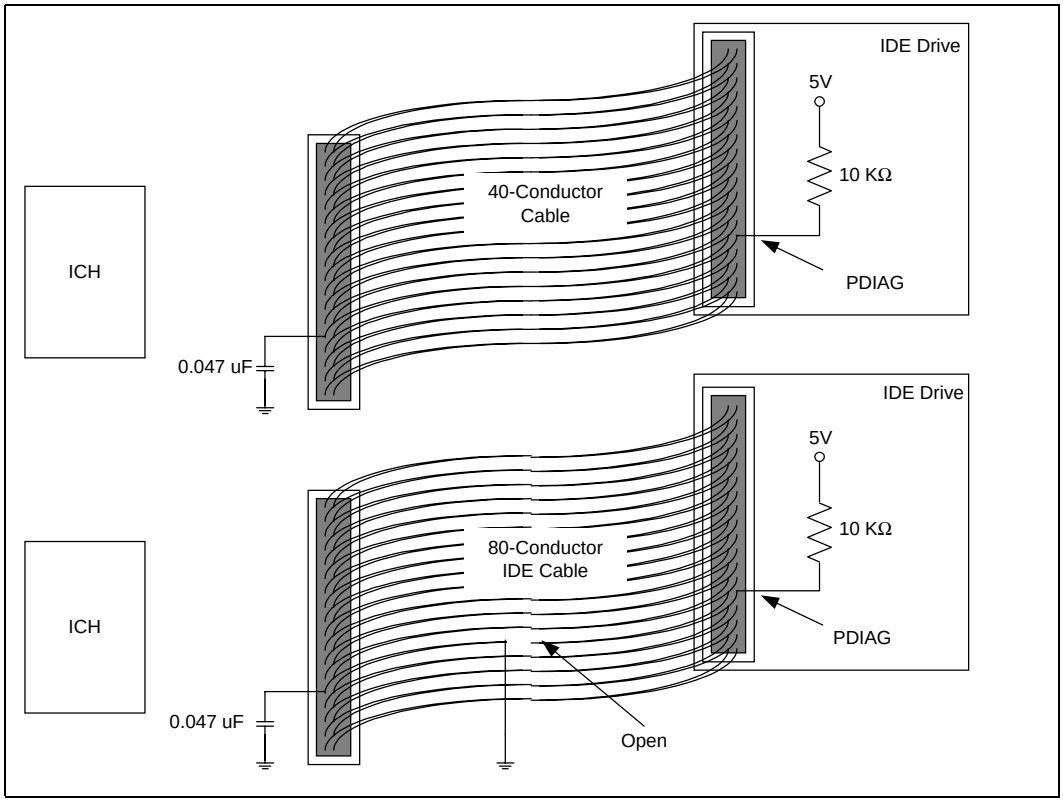
Figure 2-46. Host-Side IDE Cable Detection



Device-Side Detection (BIOS Queries IDE Drive for Cable Type)

Device side detection requires only a 0.047 uF capacitor on the motherboard as shown in Figure 2-47. This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3 or 4 drive will drive PDIAG/CBLID low and then release it (pulled up through a 10 KΩ resistor) The drive will sample the PDIAG signal after releasing it. In an 80-conductor cable, PDIAG/CBLID is not connected through and, therefore, the capacitor has no effect. In a 40-conductor cable, PDIAG/CBLID is connected though to the drive. Therefore, the signal rises more slowly. The drive can detect the difference in rise times and it reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

Figure 2-47. Drive-Side IDE Cable Detection



Layout for BOTH Host-Side and Drive-Side Cable Detection

It is possible to layout for both Host-Side and Drive-Side cable detection and decide the method to be used during assembly. Figure 2-48 shows the layout that allows for both host-side and drive-side detection.

- For Host-Side Detection:
  - R1 is a 0 Ω resistor
  - R2 is a 15 KΩ resistor
  - C1 is not stuffed
- For Drive-Side Detection:
  - R1 is not stuffed
  - R2 is not stuffed
  - C1 is a 0.047 uF capacitor

Figure 2-48. Layout for Host- or Drive-Side IDE Cable Detection

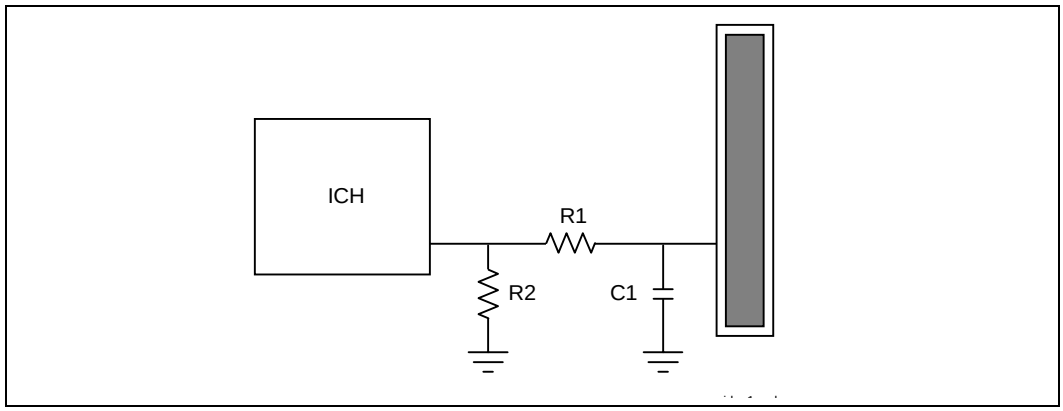
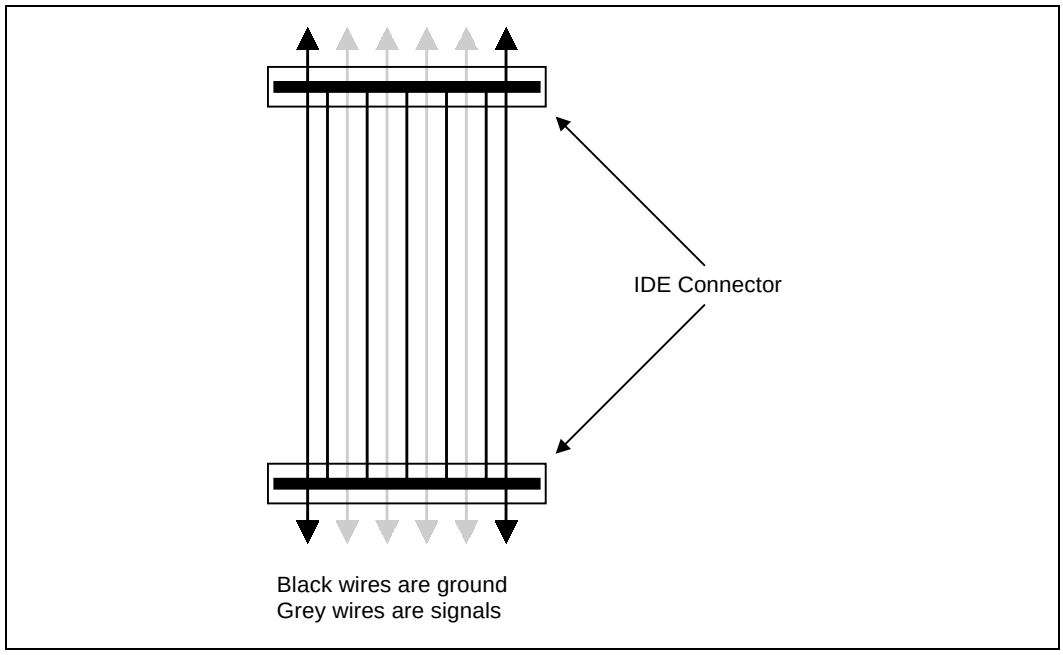


Figure 2-49. Ultra ATA/66 Cable



2.13.3 Ultra ATA/66 Pullup/Pulldown Requirements

- 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 KΩ to 10 KΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC5.
- A 10 KΩ pull-down resistor is required on PDD7 and SDD7 (as required by the ATA-4 specification).
- A 5.6 KΩ pull-down resistor is required on PDDREQ# and SDDREQ# (as required by the ATA-4 specification).
- A 1K Ω pull-up resistor is required on PIORDY and SIORDY (as required by the ATA-4 specification).

Figure 2-50. Resistor Requirements for Primary IDE Connector

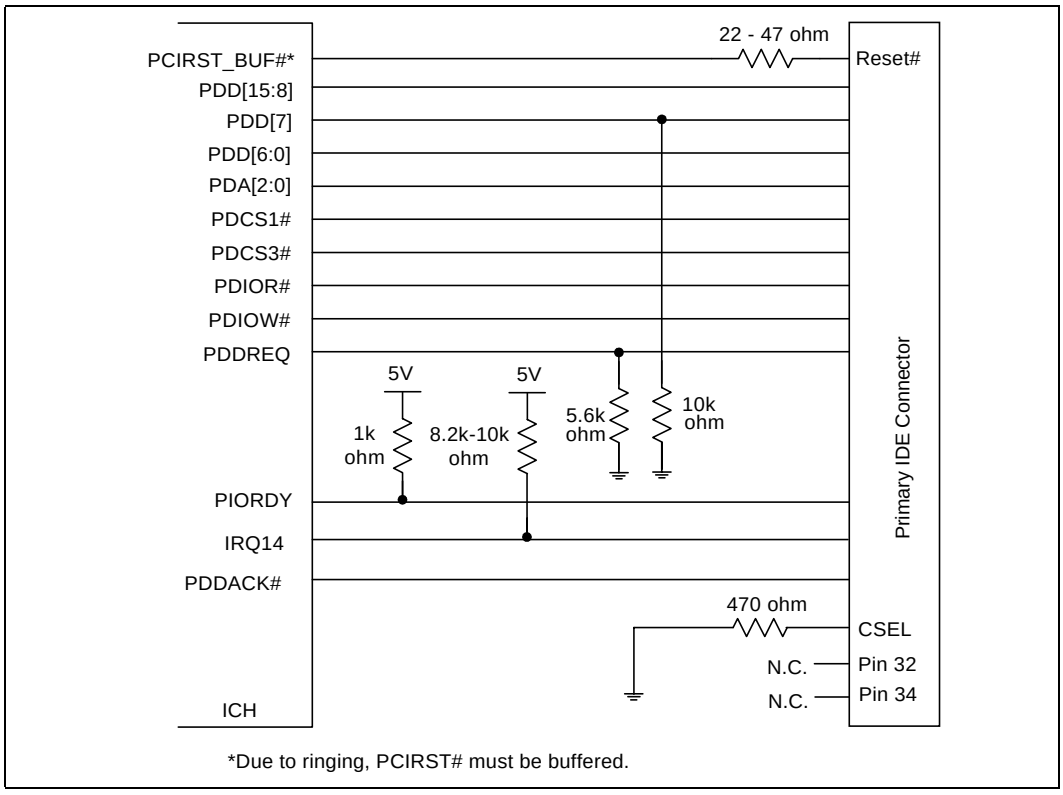
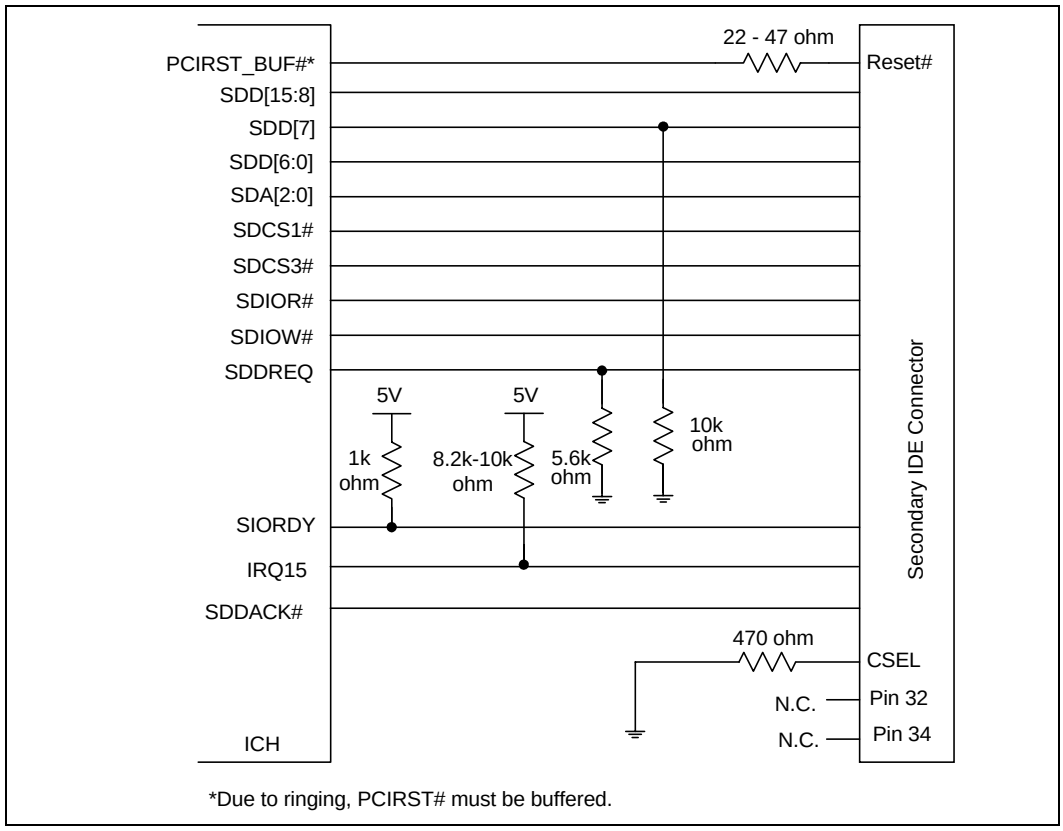


Figure 2-51. Resistor Requirements for Secondary IDE Connector



2.14 AC'97

The ICH implements an AC'97 2.1 compliant digital controller. Any codec attached to the ICH AC-link must be AC'97 2.1 compliant as well. Contact your codec IHV for information on 2.1 compliant products. The AC'97 2.1 specification is on the Intel website. The ICH supports the following combinations of codecs:

Table 2-15. ICH Codec Options

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

As shown in the table, the ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC cannot be present.

Intel has developed a common connector specification known as the Audio/Modem Riser (AMR). This specification defines a mechanism for allowing OEM plug-in card options.

The AMR specification provides a mechanism for AC'97 codecs to be on a riser card. This is important for modem codecs as it helps ease international certification of the modem.

For increased part placement flexibility, there are two routing methods for the AC'97 interface: the *tee* topology and the *daisy-chain* topology. The AC'97 interface can be routed using 5 mil traces with 5 mil space between the traces.

Figure 2-52. Tee Topology AC'97 Trace Length Requirements

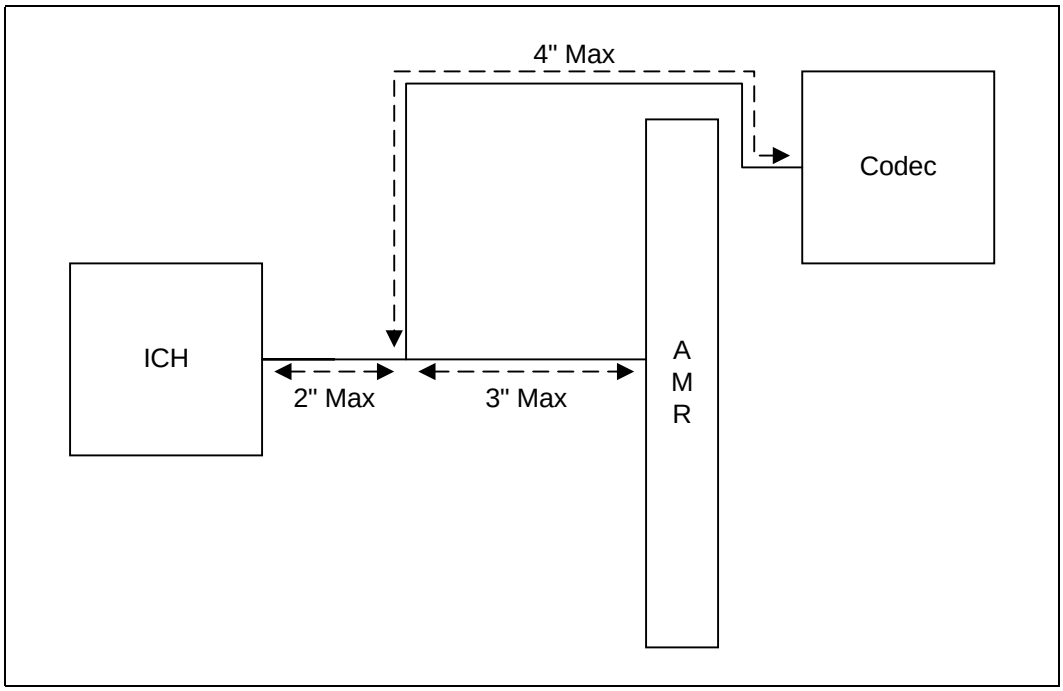
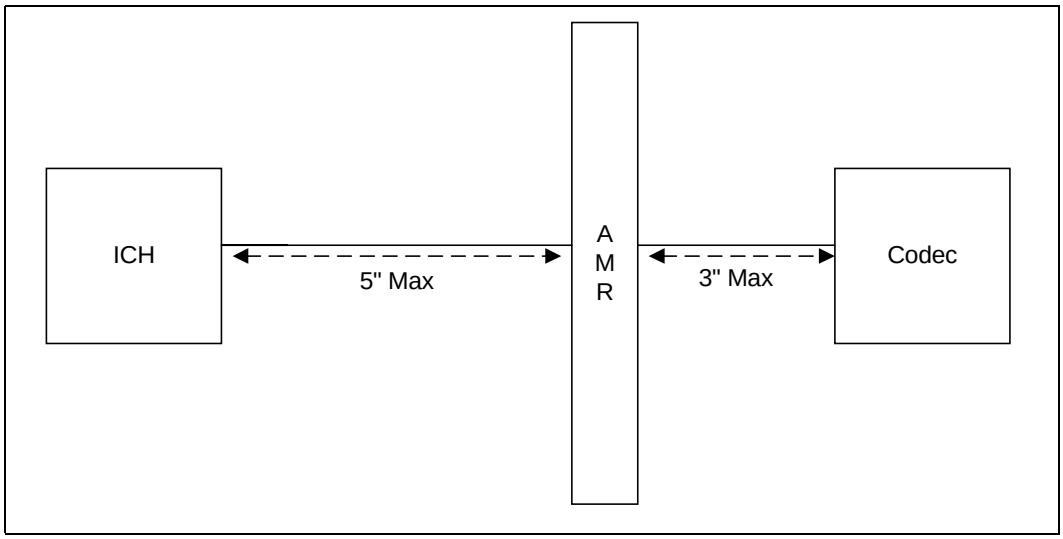


Figure 2-53. Daisy-Chain Topology AC'97 Trace Length Requirements



Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH), and any other codec present. That clock is used as the timebase for latching and driving data.

On the Intel® 820 chipset platform, the ICH supports Wake on Ring from S1, S3, and S4 via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH has weak pulldowns/pullups that are only enabled when the AC-Link Shut Off bit in the ICH is set. This will keep the link from floating when the AC-link is off, or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, BITCLK and AC_SDOUT will be driven by the codec and ICH respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec. If there is an onboard codec only (i.e., no AMR), then the unused SDIN pin should have a weak (10 KΩ) pulldown to keep it from floating. If an AMR is used, any SDIN signal that could be no connected (e.g., with no codec, both can be NC), then both SDIN pins must have a 10 KΩ pulldown.

Table 2-16. AC'97 SDIN Pulldown Resistors

System Solution	Pullup Requirements
On-board Codec Only	Pulldown the SDIN pin that is NOT connected to the codec
AMR Only	Pulldown BOTH SDIN pins
BOTH AMR and On-board Codec	Pulldown any SDIN pin that could be NC*

NOTE: If the on-board codec can be disabled, both SDIN pins must have pulldowns. If the on-board codec can not be disabled, only the SDIN not connected to the on-board codec requires a pulldown.

2.14.1 AC'97 Signal Quality Requirements

In a lightly loaded system (e.g., single codec down), AC'97 signal integrity should be evaluated to confirm that the signal quality on the link is acceptable to the codec used in the design. A series resistor at the driver and a capacitor at the codec can be implemented in order to compensate for any signal integrity issues. The values used will be design dependent and should be verified for correct timings. The ICH AC-link output buffers are designed to meet the AC'97 2.1 specification with the specified load of 50pF.

2.14.2 AC'97 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH0/ICH platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. These recommendations do not represent the only implementation or a complete checklist, but provides recommendations based on the ICH0/ICH platform.

- Codec Implementation
  - The motherboard can implement any valid combination of codecs on the motherboard and on the riser. For ease of homologation, it is recommended that a modem codec be implemented on the AMR module; however, nothing precludes a modem codec on the motherboard.
  - Only one primary codec can be present on the link. A maximum of two present codecs can be supported in an ICH0/ICH platform.
  - If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground.
  - The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
  - Components (e.g., FET switches), buffers, or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so will potentially interfere with timing margins and signal integrity.
  - If the motherboard requires that an AMR module override a primary codec down, a means of preventing contention on the AC-link must be provided for the onboard codec.
  - The ICH0/ICH supports Wake on Ring* from S1-S4 states via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pulldowns will prevent the inputs from floating, therefore external resistors are not required. The ICH0/ICH does not wake from the S5 state via the AC'97 link.
  - The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active—they should be pulled to ground through a weak (approximately 10 KΩ) pull-down resistor. If the AC-link is disabled (by setting the shut-off bit to 1), then the ICH0/ICH's internal pull-down resistors are enabled, and thus there is no need for external pull-down resistors. However, if the AC-link is to be active, then there should be pull-down resistors *on any SDATAIN signal that has the potential of not being connected to a codec*. For example, if a dedicated audio codec is on the motherboard, and cannot be disabled via a hardware jumper or stuffing option, then its SDATAIN signal does not need a pull-down resistor. If however, the SDATAIN signal has no codec connected, or is connected to an AMR slot, or is connected to an onboard codec that can be hardware disabled, then the signal should have an external pull-down resistor to ground.
- AMR Slot Special Connections
  - AUDIO_MUTE#: No connect on the motherboard.
  - AUDIO_PWRDN: No connect on the motherboard. Codecs on the AMR card should implement a powerdown pin, per the AC'97 2.1 specification, to control the amplifier.
  - MONO_PHONE: Connect top onboard audio codec if supported.
  - MONO_OUT/PC_BEEP: Connect to SPKR output from the ICH0/ICH, or MONO_OUT from onboard codec.
  - PRIMARY_DN#: See discussion above.
  - +5VDUAL/+5VSB: Connect to VCC5 core on the motherboard, unless adequate power supply is available. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
  - S/P-DIF_IN: Connect to ground on the motherboard.
  - AC_SDATAIN[3:2]: No connect on the motherboard. The ICH0/ICH supports a maximum of two codecs, which should be attached to SDATAIN[1:0].
  - AC97_MSTRCLK: Connect to ground on the motherboard.
- The ICH0/ICH provides internal weak pulldowns. Therefore, the motherboard does not need to provide discrete pulldown resistors.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

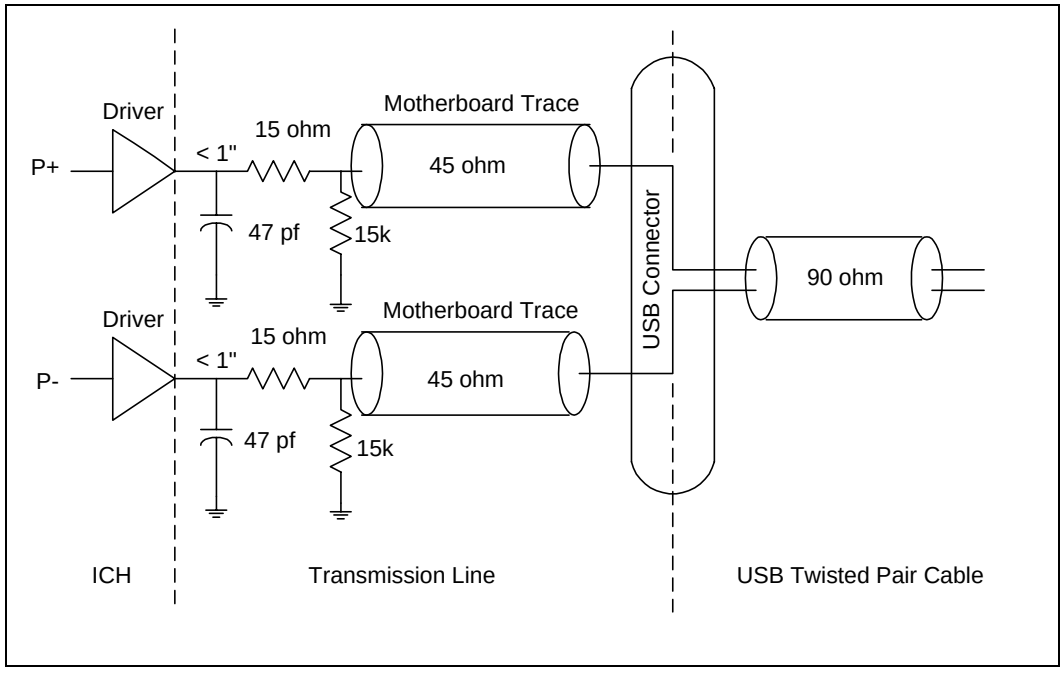
2.15 USB

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15 KΩ pulldown resistors on both P+/P- data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH (<1 inch). These series resistors are required for source termination of the reflected signal.
- 47 pF caps must be placed as close to the ICH as possible and on the ICH side of the series resistors on the USB data lines (P0+/-, P1+/-). These caps are there for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 KΩ ±5% pulldown resistors should be placed on the USB side of the series resistors on the USB data lines (P0+/-, P1+/-), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0+/-, P1+/- signals should be 45 Ω (to ground) for each USB signal P+ or P-. Using the stackup recommended in section Section 5.3, “Stackup Requirement” on page 5-1. USB requires 9 mils traces. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90 Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI.

Figure 2-54 illustrates the recommended USB schematic.

Figure 2-54. USB Data Signals



Recommended USB trace characteristics

- Impedance 'Z_0' = 45.4 Ω
- Line Delay = 160.2 ps
- Capacitance = 3.5 pF
- Inductance = 7.3 nH
- Res @ 20° C = 53.9 mOhm

2.16 ISA (82380AB)

2.16.1 ICH GPIO connected to 82380AB

At reset, the ICH LPC Bridge defaults to subtractive decode. Since the LPC bridge logically sits on PCI there will be two subtractive decode bridges in systems with the 82380AB (which is also a subtractive decode device). A GPO that defaults high (i.e., ICH GPO 21) must be connected to the NOGO signal on the 82380AB. Asserting NOGO prevents the 82380AB from subtractively decoding cycles on the PCI bus. The BIOS must configure the 82380AB, program the ICH to positively decode LPC cycles, and release the NOGO signal to the 82380AB.

2.16.2 Sub Class Code

Both the LPC Bridge and the 82380AB have the same Sub Class code indicating an ISA bridge. This can not be handled by the OS's PCI PnP code. The ICH provides the ability to hide IDSEL to the 82380AB. ICH A22 must be connected to the 82380AB IDSEL signal. After the BIOS configures the 82380AB, it will set a bit in the ICH that hides the 82380AB from the OS by not asserting the IDSEL (A22) to the 82380AB during OS enumeration.

2.17 IOAPIC Design Recommendation

UP systems not using the IOAPIC should follow these recommendations:

- On the ICH
  - — Connect PICCLK directly to ground
  - — Connect PICD0, PICD1 to ground through a 10 KΩ resistor
- On the CPU
  - — PICCLK must be connected from the clock generator to the PICCLK pin on the processor
  - — Connect PICD0 to 2.5V through 10 KΩ resistors
  - — Connect PICD1 to 2.5V through 10 KΩ resistors

2.18 SMBus/Alert Bus

The **Alert on LAN*** signals can be used as:

- **Alert on LAN* signals:** 4.7 KΩ pullup resistors to 3.3VSB are required.
- **GPIOs:** Pullup resistors to 3.3VSB and the signals must be allowed to change states on powerup (e.g., on power-up, the ICH drives *heartbeat* messages until the BIOS programs these signals as GPIOs). The value of the pullup resistors depends on the loading on the GPIO signal.
- **Not Used:** 4.7 KΩ pullup resistors to 3.3VSB are required.

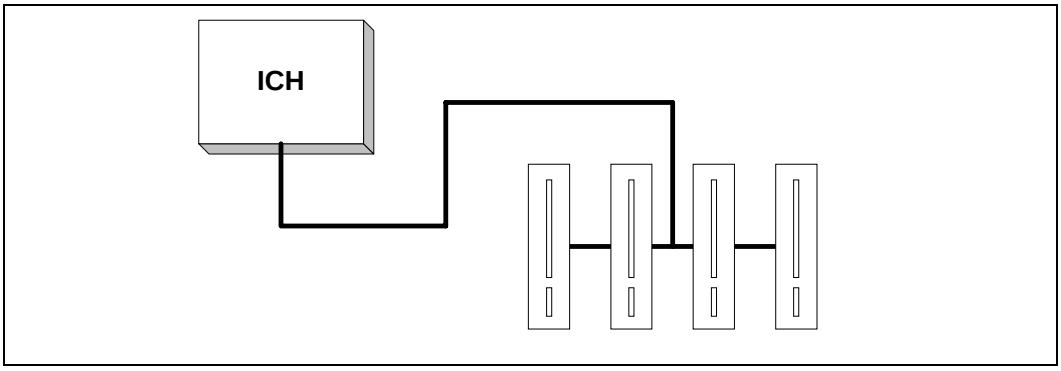
If the SMBus is used only for the three SPD EEPROMs (one on each RIMM), both signals should be pulled up with a 4.7 KΩ resistor to 3.3V.

2.19 PCI

The ICH provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH supports six PCI Bus masters (excluding the ICH), by providing six REQ#/GNT# pairs. In addition, the ICH supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 2-55. PCI Bus Layout Example



2.20 RTC

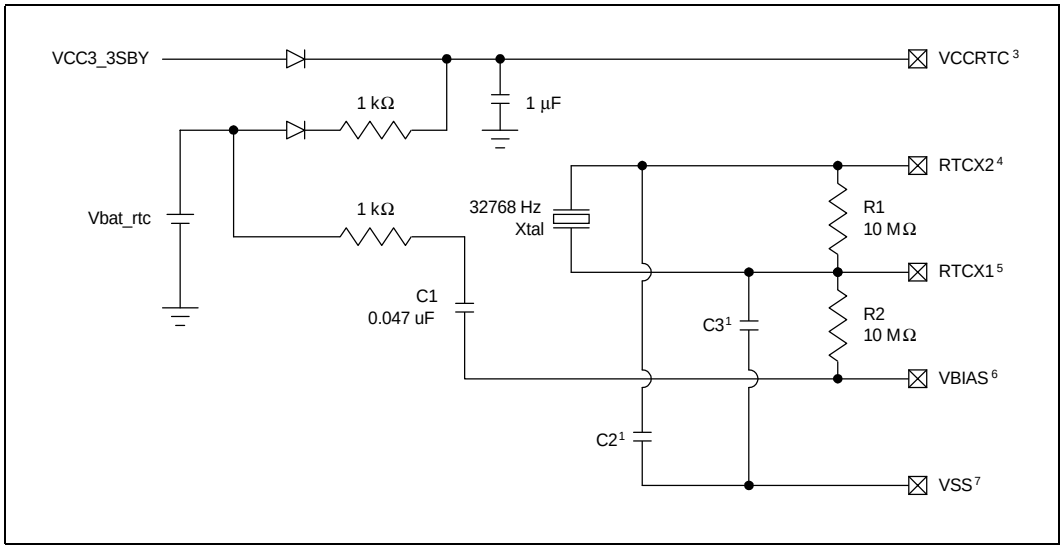
The ICH contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time, and storing system data in its RAM when the system is powered down.

This section will present the recommended hookup for the RTC circuit for the ICH. **This circuit is not the same as the circuit used for the PIIX4.**

2.20.1 RTC Crystal

The ICH RTC module requires an external oscillating source of 32.768 KHz connected on the RTCX1 and RTCX2 pins. Figure 2-56 documents the external circuitry that comprises the oscillator of the ICH RTC.

Figure 2-56. External Circuitry for the ICH RTC[2]



NOTES:
1. The exact capacitor value needs to based on what the crystal maker recommends.
2. This circuit is not the same as the one used for PIIX4.
3. VCC_{RTC}: Power for RTC Well
4. RTCX2: Crystal Input 2 – Connected to the 32.768 KHz crystal.
5. RTCX1: Crystal Input 1 – Connected to the 32.768 KHz crystal.
6. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current which is mirrored throughout the oscillator and buffer circuitry.
7. VSS: Ground

2.20.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C1 needs to be 0.047 uF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC will be.

Equation 2-4 can be used to choose the external capacitance values (C2 and C3):

Equation 2-4. External Capacitance Calculation

$$Cload = (C2 * C3)/(C2+C3) + Cparasitic$$

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain the 32.768 kHz.

2.20.3 RTC Layout Considerations

- Keep the RTC lead lengths as short as possible; around ¼ inch is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Do not route switching signals under the external components (unless on the other side of the board).
- The oscillator VCC should be clean; use a filter, such as an RC lowpass, or a ferrite inductor.

2.20.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system.

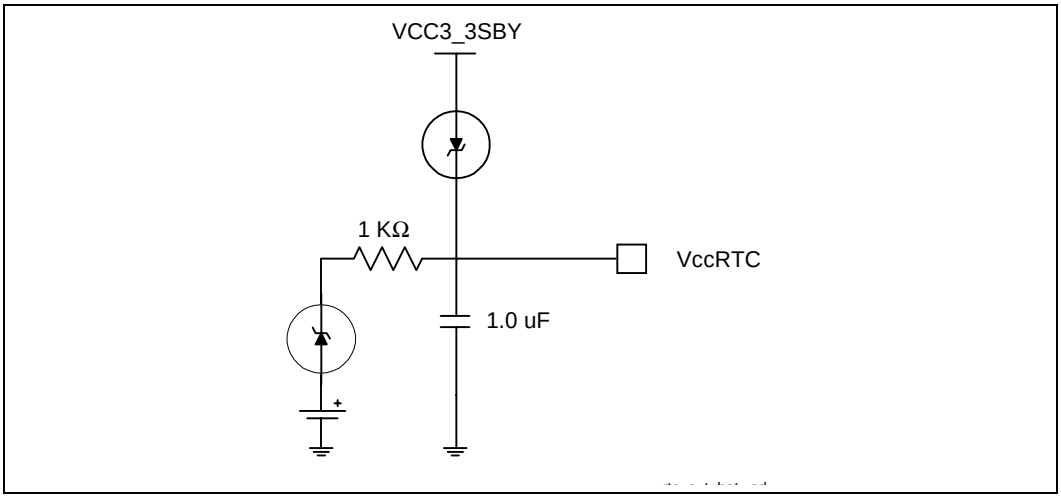
Example batteries are Duracell 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 uA, the battery life will be at least:

170,000 uAh / 3 uA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0V to 3.3V.

The battery must be connected to the ICH via an isolation schottky diode circuit. The schottky diode circuit allows the ICH RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 2-57 is an example of a diode circuitry that is used.

Figure 2-57. Diode Circuit Connecting RTC External Battery

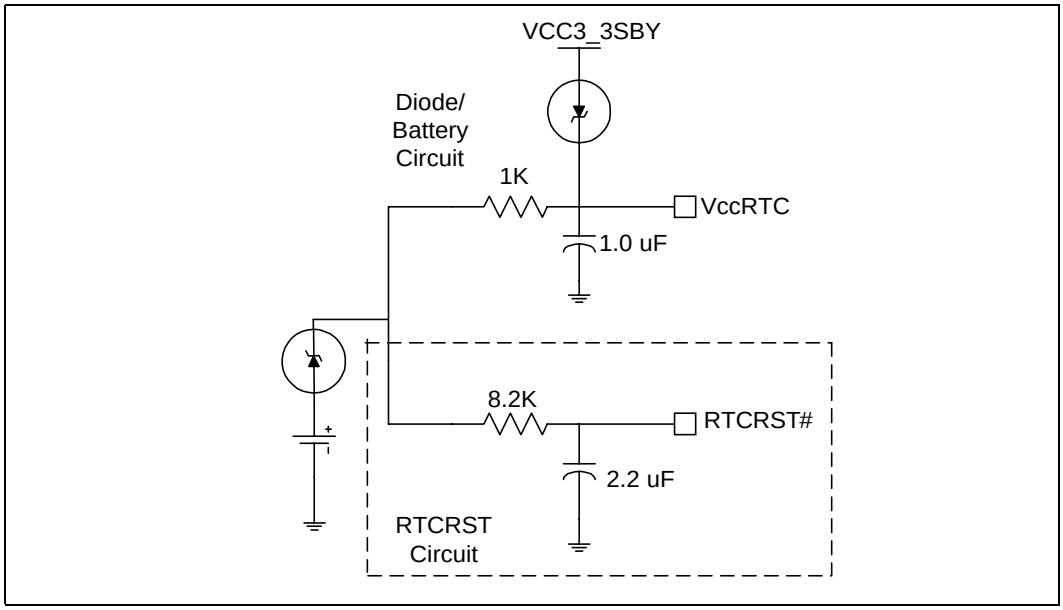


A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby increase the RTC accuracy.

2.20.5 RTC External RTCRST Circuit

The ICH RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10-20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

Figure 2-58. RTCRST External Circuit for the ICH RTC



This RTCRST# circuit is combined with the diode circuit (Figure 2-57) which allows the RTC well to be powered by the battery when the system power is not available. Figure 2-56 is an example of this circuitry that is used in conjuction with the external diode circuit.

2.20.6 RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1”, the shorter the better
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them)
- Put a ground plane under all of the external RTC circuitry
- Do not route any switching signals under the external components (unless on the other side of the ground plane)

2.20.7 VBIAS DC Voltage and Noise Measurements

- Steady state VBIAS will be a DC voltage of about 0.38V ±0.06V.
- VBIAS will be “kicked” when the battery is inserted to about 0.7–1.0V, but it will come back to its DC value within a few ms.
- Noise on VBIAS must be kept to a minimum, 200 mV or less.
- VBIAS is very sensitive and cannot be directly probed; it can be probed through a 0.01 uF capacitor.
- Excess noise on VBIAS can cause the ICH internal oscillator to misbehave or even stop completely.
- To minimize noise of VBIAS, it is necessary to implement the routing guidelines described above and the required external RTC circuitry.

This page is intentionally left blank.

3

Advanced System Bus Design

This page is intentionally left blank.

Advanced System Bus Design 3

Section 2.9, “System Bus Design” on page 2-46 describes the recommendations for designing Intel® 820 chipset based platforms. This chapter discusses more detail about the methodology used to develop the guidelines. Section 3.2, “AGTL+ Design Guidelines” on page 3-4 discusses specific system guidelines. This is a step-by-step methodology that Intel has successfully used to design high performance desktop systems. Section 3.3, “Theory” on page 3-15 introduces the theories that are applicable to this layout guideline. Section 3.4, “More Details and Insight” on page 3-19 contains more details and insights. The items in Section 3.4 expand on some of the rationale for the recommendations in the step-by-step methodology. This section also includes equations that may be used for reference.

3.1 Terminology and Definitions

Term	Definition
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors for providing the high logic level and termination. The processor AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. Additionally, the processor Single Edge Connector (S.E.C.) cartridge contains 56 Ω pull-up resistors to provide termination at each bus load.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. The results in performance of an electronic component that may change as a result of corners include (but are not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner would mean having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner would mean having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.

Term	Definition
Cross-talk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Cross-talk - coupling which creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. • Forward Cross-talk - coupling which creates a signal in a victim network that travels in the same direction as the aggressor's signal. • Even Mode Cross-talk - coupling from multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Cross-talk - coupling from multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Edge Finger	The cartridge electrical contact that interfaces to the SC242 connector.
Flight Time	Flight Time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be: • The time difference between a signal at the input pin of a receiving agent crossing V_{REF} (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.), and the output pin of the driving agent crossing V_{REF} if the driver was driving the Test Load used to specify the driver's AC timings. See Section for details regarding flight time simulation and validation. The V_{REF} Guardband takes into account sources of noise that may affect the way an AGTL+ signal becomes valid at the receiver. See the definition of the V_{REF} Guardband. • **Maximum and Minimum Flight Time** - Flight time variations can be caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, cross-talk, V_{TT} noise, V_{REF} noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of *Simultaneous Switching Output (SSO)* and packaging effects. • The **Maximum Flight Time** is the largest flight time a network will experience under all variations of conditions. Maximum flight time is measured at the appropriate V_{REF} Guardband boundary. • The **Minimum Flight Time** is the smallest flight time a network will experience under all variations of conditions. Minimum flight time is measured at the appropriate V_{REF} Guardband boundary. For more information on flight time and the V_{REF} Guardband, see the *Pentium® II Processor Developer's Manual.*
GTL+	GTL+ is the bus technology used by the Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) technology. See thePentium® II *Processor Developer's Manual* for more details of GTL+.

Term	Definition
Network	The trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between extreme bus agents on the network and does not include the distance connecting the end bus agents to the termination resistors.
Overdrive Region	Is the voltage range, at a receiver, located above and below V_{REF} for signal integrity analysis. See the *Intel® Pentium® II Processor Developer's Manual* for more details.
Overshoot	Maximum voltage allowed for a signal at the processor core pad. See each processor's datasheet for overshoot specification.
Pad	A feature of a semiconductor die contained within an internal logic package on the S.E.C cartridge substrate used to connect the die to the package bond wires. A pad is only observable in simulation.
Pin	A feature of a logic package contained within the S.E.C. cartridge used to connect the package to an internal substrate trace.
Ringback	Ringback is the voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, etc. See the respective processor's datasheet for ringback specification.
Settling Limit	Defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. See the respective processor's datasheet for settling limit specification.
Setup Window	Is the time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
Simultaneous Switching Output (SSO) Effects	Refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "pushout"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the trunk terminating at the pad of an agent.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, terminating at agent pads.
Undershoot	Maximum voltage allowed for a signal to extend below V_{ss} at the processor core pad. See the respective processor's datasheet for undershoot specifications.
Victim	A network that receives a coupled cross-talk signal from another network is called the victim network.
V_{REF} Guardband	A guardband (ΔV_{REF}) defined above and below V_{REF} to provide a more realistic model accounting for noise such as cross-talk, V_{TT} noise, and V_{REF} noise.

3.2 AGTL+ Design Guidelines

The following step-by-step guideline was developed for systems based on two processor loads and one Intel 82820 MCH load. Systems using custom chipsets will require timing analysis and analog simulations specific to those components.

The guideline recommended in this section is based on experience developed at Intel while developing many different Intel Pentium® Pro processor family and Intel Pentium III processor-based systems. Begin with an initial timing analysis and topology definition. Perform pre-layout analog simulations for a detailed picture of a working “solution space” for the design. These pre-layout simulations help define routing rules prior to placement and routing. After routing, extract the interconnect database and perform post-layout simulations to refine the timing and signal integrity analysis. Validate the analog simulations when actual systems become available. The validation section describes a method for determining the flight time in the actual system.

Guideline Methodology:

- Initial Timing Analysis
- Determine General Topology, Layout, and Routing
- Pre-Layout Simulation
  - — Sensitivity sweep
  - — Monte Carlo Analysis
- Place and Route Board
  - — Estimate Component to Component Spacing for AGTL+ Signals
  - — Layout and Route Board
- Post-Layout Simulation
  - — Interconnect Extraction
  - — Inter-Symbol Interference (ISI), Cross-talk, and Monte Carlo Analysis
- Validation
  - — Measurements
  - — Determining Flight Time

3.2.1 Initial Timing Analysis

Perform an initial timing analysis of the system using Equation 3-1 and Equation 3-2 shown below. These equations are the basis for timing analysis. To complete the initial timing analysis, values for clock skew and clock jitter are needed, along with the component specifications. These equations contain a multi-bit adjustment factor, M_{ADJ}, to account for multi-bit switching effects such as SSO pushout or pull-in that are often hard to simulate. These equations **do not** take into consideration all signal integrity factors that affect timing. Additional timing margin should be budgeted to allow for these sources of noise.

Equation 3-1. Setup Time

$$T_{CO\_MAX} + T_{SU\_MIN} + CLK_{SKEW} + CLK_{JITTER} + T_{FLT\_MAX} + M_{ADJ} \leq \text{Clock Period}$$

Equation 3-2. Hold Time

$$T_{CO\_MIN} + T_{FLT\_MIN} - M_{ADJ} \geq T_{HOLD} + CLK_{SKEW}$$

Symbols used in Equation 3-1 and Equation 3-2:

— T_{CO_MAX} is the maximum clock to output specification[1].

— T_{SU_MIN} is the minimum required time specified to setup before the clock[1].

— CLK_{JITTER} is the maximum clock edge-to-edge variation.

— CLK_{SKEW} is the maximum variation between components receiving the same clock edge.

— T_{FLT_MAX} is the maximum flight time as defined in Section 3.1, “Terminology and Definitions” on page 3-1.

— T_{FLT_MIN} is the minimum flight time as defined in Section 3.1, “Terminology and Definitions” on page 3-1.

— M_{ADJ} is the multi-bit adjustment factor to account for SSO pushout or pull-in.

— T_{CO_MIN} is the minimum clock to output specification[1].

— T_{HOLD} is the minimum specified input hold time.

Note: The Clock to Output (T_{CO}) and Setup to Clock (T_{SU}) timings are both measured from the signals last crossing of V_{REF}, with the requirement that the signal does not violate the ringback or edge rate limits. See the respective Processor’s datasheet and thePentium® II*l Processor Developer’s Manual* for more details.

Solving these equations for T_{FLT} results in the following equations:

Equation 3-3. Maximum Flight Time

$$T_{FLT\_MAX} \leq \text{Clock Period} - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ}$$

Equation 3-4. Minimum Flight Time

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ}$$

There are multiple cases to consider. Note that while the same trace connects two components, component A and component B, the minimum and maximum flight time requirements for component A driving component B as well as component B driving component A must be met. The cases to be considered are:

- Processor driving processor
- Processor driving chipset
- Chipset driving processor

A designer using components other than those listed above must evaluate additional combinations of driver and receiver.

Table 3-1. AGTL+ Parameters for Example Calculations[1,2]

IC Parameters	Intel® Pentium® III processor core at 133 MHz Bus	Intel 82820 MCH	Notes
Clock to Output maximum (T_{CO_MAX})	2.7	3.6	4
Clock to Output minimum (T_{CO_MIN})	-0.1	0.5	4
Setup time (T_{SU_MIN})	1.2	2.27	3,4
Hold time (T_{HOLD})	0.8	0.28	4

NOTES:
1. All times in nanoseconds.
2. **Numbers in table are for reference only.** These timing parameters are subject to change. Please check the appropriate component documentation for valid timing parameter values.
3. T_{SU_MIN} = 1.9 ns assumes the **82**820 MCH sees a minimum edge rate equal to 0.3 V/ns.
4. The Pentium III substrate nominal impedance is set to 65 Ω ±15%. Future Pentium III processor substrate may be set at 60 Ω ±15%

Table 3-1 lists the AGTL+ component timings of the processors and 82820 MCH defined at the pins. These timings are for reference only.

Table 3-2 gives an example AGTL+ initial maximum flight time and Table 3-3 is an example minimum flight time calculation for a 133 MHz, 2-way Pentium III processor/Intel 820 chipset system bus. Note that assumed values for clock skew and clock jitter were used. Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.

Intel highly recommends adding margin as shown in the "M_{ADJ}" column to offset the degradation caused by SSO push-out and other multi-bit switching effects. The "Recommended T_{FLT_MAX}" column contains the recommended maximum flight time after incorporating the M_{ADJ} value. If edge rate, ringback, and monotonicity requirements are not met, flight time correction must first be performed as documented in the *Pentium® II Processor Developer's Manual* with the additional requirements noted in Section 3.5, "Definitions of Flight Time Measurements/Corrections and Signal Quality" on page 3-24. The commonly used "textbook" equations used to calculate the expected signal propagation rate of a board are included in Section 3.2, "AGTL+ Design Guidelines" on page 3-4.

Simulation and control of baseboard design parameters can ensure that signal quality and maximum and minimum flight times are met. Baseboard propagation speed is highly dependent on transmission line geometry configuration (stripline vs. microstrip), dielectric constant, and loading. This layout guideline includes high-speed baseboard design practices that may improve the amount

of timing and signal quality margin. The magnitude of M_{ADJ} is highly dependent on baseboard design implementation (stackup, decoupling, layout, routing, reference planes, etc.) and needs to be characterized and budgeted appropriately for each design.

Table 3-2 and Table 3-3 are derived assuming:

- CLK_{SKEW} = 0.2 ns (Note: Assumes clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together ("ganging") at clock driver output pins, and the PCB clock routing skew is 150 ps. System timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together and a clock driver that meets the CK98 clock driver specification is being used.)
- CLK_{JITTER} = 0.250 ns

Some clock driver components may not support ganging the outputs together. Be sure to verify with your clock component vendor before ganging the outputs. See the appropriate Intel 820 chipset documentation for details on clock skew and jitter specifications. Refer to Section 2.6.2, "Direct Rambus* Layout Guidelines" on page 2-8 and Chapter 4, "Clocking" for host clock routing details.

Table 3-2. Example T_{FLT_MAX} Calculations for 133 MHz Bus[1]

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}[3]
Processor[4]	Processor[4]	7.50	2.7	1.20	0.20	0.250	0.40	2.75
Processor[4]	82820 MCH	7.50	2.7	2.27	0.20	0.250	0.40	1.68
82820 MCH	Processor[4]	7.50	3.63	1.20	0.20	0.25	0.40	1.82

NOTES:
1. All times in nanoseconds.
2. BCLK period = 7.50 ns @ 133.33 MHz.
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
   - SSO push-out or pull-in.
   - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
   - Cross-talk on the PCB and internal to the package can cause variation in the signals.

   There are additional effects that **may not** necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:
   - The effective board propagation constant (S_{EFF}), which is a function of:
     - Dielectric constant (ε_r) of the PCB material.
     - The type of trace connecting the components (stripline or microstrip).
     - The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a **component** of the flight time **but not necessarily equal to** the flight time.
4. Processor values specified in this table are examples only. Refer to the appropriate processor datasheet for specification values.

Table 3-3. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	Clk_{SKEW}	T_{CO_MIN}	Recommended T_{FLT_MIN}
Processor[2]	Processor[2]	0.8	0.2	-0.1	1.2
Processor[2]	82820 MCH	0.28	0.2	-0.1	.58
82820 MCH	Processor[2]	0.8	0.2	0.5	.5

NOTES:
1. All times in nanoseconds.
2. Processor values specified in this table are examples only. Refer to the appropriate processor datasheet for specification values.

3.2.2 Determine General Topology, Layout, and Routing Desired

After calculating the timing budget, determine the approximate location of the processor and the chipset on the base board (see Section 2.9, “System Bus Design” on page 2-46).

3.2.3 Pre-Layout Simulation

3.2.3.1 Methodology

Analog simulations are recommended for high speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working “solution space” that meets flight time and signal quality requirements. The layout recommendations in the previous sections are based on pre-layout simulations conducted at Intel. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulation can be reduced.

Intel recommends running simulations at the **device pads** for signal quality and at the **device pins** for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

3.2.3.2 Sensitivity Analysis

Pre-layout analysis includes a sensitivity analysis using parametric sweeps. Parametric sweep analysis involves varying one or two system parameters while all others such as driver strength, package, Z_0, and S_0 are held constant. This way, the sensitivity of the proposed bus topology to varying parameters can be analyzed systematically. Sensitivity of the bus to minimum flight time, maximum flight time, and signal quality should be covered. Suggested sweep parameters include trace lengths, termination resistor values, and any other factors that may affect flight time, signal quality, and feasibility of layout. Minimum flight time and worst signal quality are typically analyzed using fast I/O buffers and interconnect. Maximum flight time is typically analyzed using slow I/O buffers and slow interconnects.

Outputs from each sweep should be analyzed to determine which regions meet timing and signal quality specifications. To establish the working solution space, find the common space across all the sweeps that result in passing timing and signal quality. The solution space should allow enough design flexibility for a feasible, cost-effective layout.

3.2.3.3 Monte Carlo Analysis

Perform a Monte Carlo analysis to refine the passing solution space region. A Monte Carlo analysis involves randomly varying parameters (independent of one another) over their tolerance range. This analysis intends to ensure that no regions of failing flight time and signal quality exists between the extreme corner cases run in pre-layout simulations. For the example topology, vary the following parameters during Monte Carlo simulations:

- Lengths L1 through L3
- Termination resistance R_{TT} on the processor cartridge #1
- Termination resistance R_{TT} on the processor cartridge #2
- Z_0 of traces on processor cartridge #1
- Z_0 of traces on processor cartridge #2
- S_0 of traces on processor cartridge #1
- S_0 of traces on processor cartridge #2
- Z_0 of traces on baseboard
- S_0 of traces on baseboard
- Fast and slow corner processor I/O buffer models for cartridge #1
- Fast and slow corner processor I/O buffer models for cartridge #2
- Fast and slow package models for processor cartridge #1
- Fast and slow package models for processor cartridge #2
- Fast and slow corner 82820 MCH I/O buffer models
- Fast and slow 82820 MCH package models

3.2.3.4 Simulation Criteria

Accurate simulations require that the actual range of parameters be used in the simulations. Intel has consistently measured the cross-sectional resistivity of the PCB copper to be approximately 1 Ω*mil^2/inch, not the 0.662 Ω*mil^2/inch value for annealed copper that is published in reference material. Using the 1 Ω*mil^2/inch value may increase the accuracy of lossy simulations.

Positioning drivers with faster edges closer to the middle of the network typically results in more noise than positioning them towards the ends. However, Intel has shown that drivers located in all positions (given appropriate variations in the other network parameters) can generate the worst-case noise margin. Therefore, Intel recommends simulating the networks from all driver locations, and analyzing each receiver for each possible driver.

Analysis has shown that **both fast and slow corner conditions** must be run for both rising and falling edge transitions. The fast corner is needed because the fast edge rate creates the most noise. The slow corner is needed because the buffer's drive capability will be a minimum, causing the V_{OL} to shift up, which may cause the noise from the slower edge to exceed the available budget. Slow corner models may produce minimum flight time violations on rising edges if the transition starts from a higher V_{OL}. So, Intel **highly recommends** checking for minimum and maximum flight time violations with both the fast and slow corner models. The fast and slow corner I/O buffer models are contained in the processor and Intel 820 chipset electronic models provided by Intel.

The transmission line package models must be inserted between the output of the buffer and the net it is driving. Likewise, the package model must also be placed between a net and the input of a receiver model. Editing the simulator's net description or topology file generally does this.

Intel has found wide variation in noise margins when varying the stub impedance and the PCB's Z0 and S0. Intel therefore recommends that PCB parameters are controlled as tightly as possible, with a sampling of the allowable Z0 and S0 simulated. The Intel® Pentium® III processor nominal effective line impedance is 65 Ω ±15%. Future Intel® Pentium® III processor effective line impedance (Z_{EFF}) may be 60 Ω ±15%. Intel recommends the baseboard nominal effective line impedance to be at 60 Ω ±15% for the recommended layout guidelines to be effective. Intel also recommends running uncoupled simulations using the Z_0 of the package stubs; and performing fully coupled simulations if increased accuracy is needed or desired. Accounting for cross-talk within the device package by varying the stub impedance was investigated and was not found to be sufficiently accurate. This lead to the development of full package models for the component packages.

3.2.4 Place and Route Board

3.2.4.1 Estimate Component To Component Spacing for AGTL+ Signals

Estimate the number of layers that will be required. Then determine the expected interconnect distances between each of the components on the AGTL+ bus. Using the estimated interconnect distances, verify that the placement can support the system timing requirements.

The required bus frequency and the maximum flight time propagation delay on the PCB determine the maximum network length between the bus agents. The minimum network length is independent of the required bus frequency. Table 3-2 and Table 3-3 assume values for CLK_{SKEW} and CLK_{JITTER} - parameters that are controlled by the system designer. To reduce system clock skew to a minimum, clock buffers that allow their outputs to be tied together are recommended. Intel strongly recommends running analog simulations to ensure that each design has adequate noise and timing margin.

3.2.4.2 Layout and Route Board

Route the board satisfying the estimated space and timing requirements. Also stay within the solution space set from the pre-layout sweeps. Estimate the printed circuit board parameters from the placement and other information including the following general guidelines:

- Distribute V_{TT} with a power plane or a partial power plane. If this cannot be accomplished, use as wide a trace as possible and route the V_{TT} trace with the same topology as the AGTL+ traces.
- Keep the overall length of the bus as short as possible (but do not forget minimum component-to-component distances to meet hold times).
- Plan to minimize cross-talk with the following guidelines developed for the example topology given (signal spacing recommendations were based on fully coupled simulations - spacing may be decreased based upon the amount of coupled length):
  - — Use a spacing to line width to dielectric thickness ratio of at least 3:1:2. If $\varepsilon_r = 4.5$, this should limit coupling to 3.4%.
  - — Minimize the dielectric process variation used in the PCB fabrication.
  - — Eliminate parallel traces between layers not separated by a power or ground plane.

Figure 3-3 contains the trace width:space ratios assumed for this topology. The cross-talk cases considered in this guideline involve three types: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+. Intra-group AGTL+ cross-talk involves interference between AGTL+ signals within the same group (See Section 3.4, "More Details and Insight" on page 3-19 for a description of the different AGTL+ group types). Intergroup AGTL+ cross-talk involves

interference from AGTL+ signals in a particular group to AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ cross-talk is when CMOS and AGTL+ signals interfere with each other.

Table 3-4. Trace Width Space Guidelines

Cross-talk Type	Trace Width:Space Ratio
Intragroup AGTL+ (same group AGTL+)	5:10 or 6:12
Intergroup AGTL+ (different group AGTL+)	5:15 or 6:18
AGTL+ to non-AGTL+	5:20 or 6:24

The spacing between the various bus agents causes variations in trunk impedance and stub locations. These variations cause reflections that can cause constructive or destructive interference at the receivers. A reduction of noise may be obtained by a minimum spacing between the agents. Unfortunately, tighter spacing results in reduced component placement options and lower hold margins. Therefore, adjusting the inter-agent spacing may be one way to change the network's noise margin, but mechanical constraints often limit the usefulness of this technique. Always be sure to validate signal quality after making any changes in agent locations or changes to inter-agent spacing.

There are six AGTL+ signals that can be driven by more than one agent simultaneously. These signals may require more attention during the layout and validation portions of the design. When a signal is asserted (driven low) by two or more agents on the same clock edge, the two falling edge wave fronts will meet at some point on the bus and can sum to form a negative voltage. The ring-back from this negative voltage can easily cross into the overdrive region. The signals are AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

This document addresses AGTL+ layout for both 1 and 2-way 133 MHz/100 MHz processor/ Intel® 820 chipset systems. Power distribution and chassis requirements for cooling, connector location, memory location, etc., may constrain the system topology and component placement location; therefore, constraining the board routing. These issues are not directly addressed in this document. Section 1.2, "References" on page 1-2 contains a listing of several documents that address some of these issues.

3.2.4.3 Host Clock Routing

Host clock nets should be routed as point-to-point connections through a series resistor placed as close to the output pins of the clock driver as possible. The value of the series resistor is dependent on the clock driver characteristic impedance. However, a value of 33 Ω is a good starting point. Table 3-5 provides the trace length recommendations for this topology. “H” indicates the length of the host clock trace starting from the clock driver output pin and ending at the SC242 connector BCLK pin. Note that the clock route from the clock driver to the Intel 82820 MCH will require an additional trace length of approximately 4.6” to compensate for the additional propagation delay along the processor host clock path (SC242 connector plus processor cartridge trace). This value of 4.6” assumes a propagation speed of 180 ps/in.

Table 3-5. Host Clock Routing

Clock Net	Trace length
Clock driver to SC242 connector	H
Clock driver to Intel 82820 MCH	H + (clock delay from the processor edge to core) + connector delay

3.2.4.4 APIC Data Bus Routing

Intel recommends using the in-line topology shown in Figure 3-1 and Figure 3-2 for the APIC Data signals, PICD[1:0]. For dual-processor systems, the network should be dual-end terminated with 330 Ω resistors. The combined routing lengths of L1 plus L2 should be between 0.0” and 12.0”.

Figure 3-1. PICD[1,0] Uni-Processor Topology

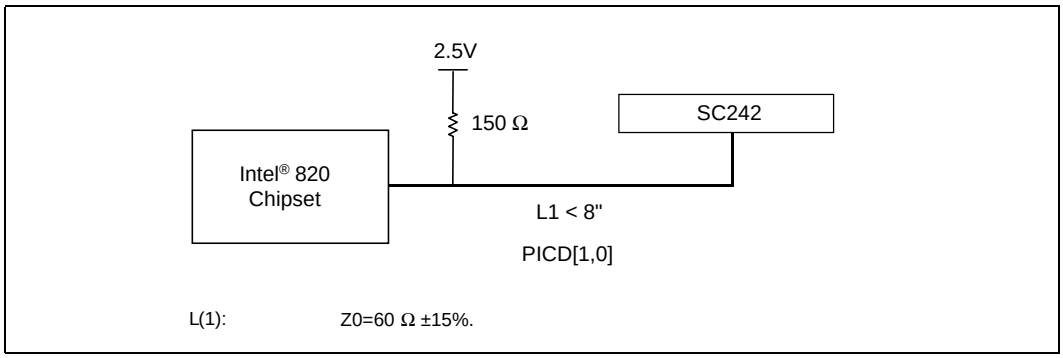
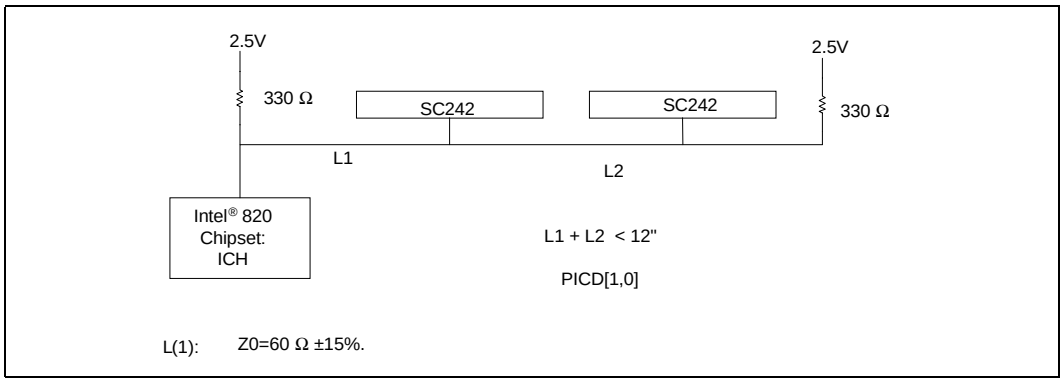


Figure 3-2. PICD[1,0] Dual-Processor Topology



3.2.5 Post-Layout Simulation

Following layout, extract the interconnect information for the board from the CAD layout tools. Run simulations to verify that the layout meets timing and noise requirements. A small amount of "tuning" may be required; experience at Intel has shown that sensitivity analysis dramatically reduces the amount of tuning required. The post layout simulations should take into account the expected variation for all interconnect parameters.

Intel specifies signal integrity **at the device pads** and therefore recommends running simulations at the device pads for signal quality. However, Intel specifies core timings **at the device pins,** so simulation results at the device pins should be used later to correlate simulation performance against actual system measurements.

3.2.5.1 Intersymbol Interference

Intersymbol Interference (ISI) refers to the distortion or change in the waveform shape caused by the voltage and transient energy on the network when the driver begins its next transition.

Intersymbol Interference (ISI) occurs when transitions in the current cycle interfere with transitions in subsequent cycles. ISI can occur when the line is driven high, low, and then high in consecutive cycles (the opposite case is also valid). When the driver drives high on the first cycle and low on the second cycle, the signal may not settle to the minimum V_{OL} before the next rising edge is driven. This results in improved flight times in the third cycle. Intel performed ISI simulations for the topology given in this section by comparing flight times for the first and third cycle. ISI effects do not necessarily span only 3 cycles so it may be necessary to simulate beyond 3 cycles for certain designs. After simulating and quantifying ISI effects, adjust the timing budget accordingly to take these conditions into consideration.

3.2.5.2 Cross-Talk Analysis

AGTL+ cross-talk simulations can consider the processor core package, Intel 82820 MCH package, and SC242 connectors as non-coupled. Treat the traces on the processor cartridge and baseboard as fully coupled for maximum cross-talk conditions. Simulate the traces as lossless for worst case cross-talk and lossy where more accuracy is needed. Evaluate both odd and even mode cross-talk conditions.

AGTL+ Cross-talk simulation involves the following cases:

- Intra-group AGTL+ cross-talk
- Inter-group AGTL+ cross-talk
- Non-AGTL+ to AGTL+ cross-talk

3.2.5.3 Monte Carlo Analysis

Perform a Monte Carlo analysis on the extracted baseboard. Vary all parameters recommended for the pre-layout Monte Carlo analysis within the region that they are expected to vary. The range for some parameters will be reduced compared to the pre-layout simulations. For example, baseboard lengths L1 through L7 should no longer vary across the full min and max range on the final baseboard design. Instead, baseboard lengths should now have an actual route, with a length tolerance specified by the baseboard fabrication manufacturer.

3.2.6 Validation

Build systems and validate the design and simulation assumptions.

3.2.6.1 Measurements

Note that the AGTL+ specification for signal quality is at the **pad** of the component. The expected method of determining the signal quality is to run analog simulations for the pin and the pad. Then correlate the simulations at the pin against actual system measurements at the pin. Good correlation at the pin leads to confidence that the simulation at the pad is accurate. Controlling the temperature and voltage to correspond to the I/O buffer model extremes should enhance the correlation between simulations and the actual system.

3.2.6.2 Flight Time Simulation

As defined in Section 3.1, "Terminology and Definitions" on page 3-1, flight time is the time difference between a signal crossing V_{REF} at the input pin of the receiver, and the output pin of the driver crossing V_{REF} were it driving a test load. The timings in the tables and topologies discussed in this guideline assume the actual system load is 50 Ω and is equal to the test load. While the DC loading of the AGTL+ bus in a DP mode is closer to 25 Ω, AC loading is approximately 29 Ω since the driver effectively "sees" a 56 Ω termination resistor in parallel with a 60 Ω transmission line on the cartridge.

Figure 3-3. Test Load vs. Actual System Load

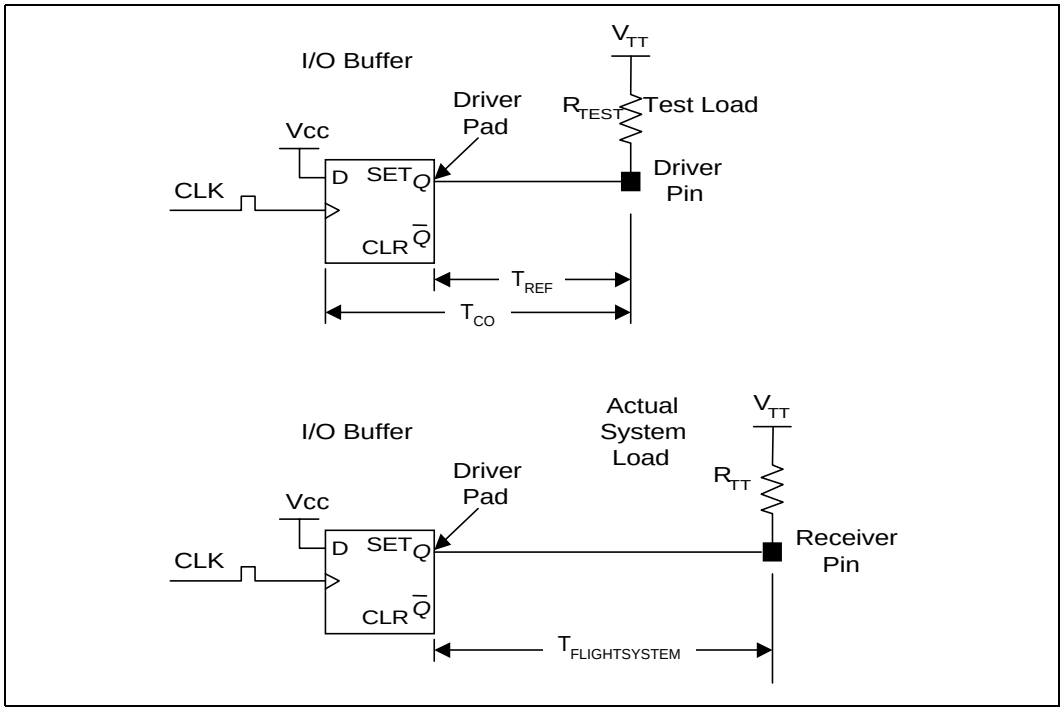


Figure 3-3 above shows the different configurations for T_{CO} testing and flight time simulation. The flip-flop represents the logic input and driver stage of a typical AGTL+ I/O buffer. T_{CO} timings are specified at the driver pin output. $T_{FLIGHT-SYSTEM}$ is usually reported by a simulation tool as the time from the driver pad starting its transition to the time when the receiver's input pin sees a valid data input. Since both timing numbers (T_{CO} and $T_{FLIGHT-SYSTEM}$) include propagation time from the pad to the pin, it is necessary to subtract this time (T_{REF}) from the reported flight time to avoid

double counting. T_{REF} is defined as the time that it takes for the driver output pin to reach the measurement voltage, V_{REF}, starting from the beginning of the driver transition at the pad. T_{REF} must be generated using the same test load for T_{CO}. Intel provides this timing value in the AGTL+ I/O buffer models.

In this manner, the following *valid delay* equation is satisfied:

Equation 3-5. Valid Delay Equation

$$\text{Valid Delay} = T_{CO} + T_{FLIGHT\text{-}SYS} - T_{REF} = T_{CO\text{-}MEASURED} + T_{FLIGHT\text{-}MEASURED}$$

This valid delay equation is the total time from when the driver sees a valid clock pulse to the time when the receiver sees a valid data input.

3.2.6.3 Flight Time Hardware Validation

When a measurement is made on the actual system, T_{CO} and flight time do not need T_{REF} correction since these are the actual numbers. These measurements include all of the effects pertaining to the driver-system interface and the same is true for the T_{CO}. Therefore the addition of the measured T_{CO} and the measured flight time must be equal to the valid delay calculated above.

3.3 Theory

3.3.1 AGTL+

AGTL+ is the electrical bus technology used for the processor bus. This is an incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at each load. The processor AGTL+ drivers contain a full-cycle active pull-up device to improve system timings. The AGTL+ specification defines:

- Termination voltage (V_{TT}).
- Receiver reference voltage (V_{REF}) as a function of termination voltage (V_{TT}).
- processor termination resistance (R_{TT}).
- Input low voltage (V_{IL}).
- Input high voltage (V_{IH}).
- NMOS on resistance (RON_N).
- PMOS on resistance (RON_P).
- Edge rate specifications.
- Ringback specifications.
- Overshoot/Undershoot specifications.
- Settling Limit.

3.3.2 Timing Requirements

The system timing for AGTL+ is dependent on many things. Each of the following elements combine to determine the maximum and minimum frequency the AGTL+ bus can support:

- The range of timings for each of the agents in the system.
  - Clock to output [T_{CO}]. (Note that the system load is likely to be different from the "specification" load therefore the T_{CO} observed in the system might not be the same as the T_{CO} from the specification.)
  - The minimum required setup time to clock [T_{SU_MIN}] for each receiving agent.
- The range of flight time between each component. This includes:
  - The velocity of propagation for the loaded printed circuit board [S_{EFF}].
  - The board loading impact on the effective T_{CO} in the system.
- The amount of skew and jitter in the system clock generation and distribution.
- Changes in flight time due to cross-talk, noise, and other effects.

3.3.3 Cross-talk Theory

AGTL+ signals swing across a smaller voltage range and have a correspondingly smaller noise margin than technologies that have traditionally been used in personal computer designs. This requires that designers using AGTL+ be more aware of cross-talk than they may have been in past designs.

Cross-talk is caused through capacitive and inductive coupling between networks. Cross-talk appears as both backward cross-talk and as forward cross-talk. Backward cross-talk creates an induced signal on a victim network that propagates in a direction opposite that of the aggressor's signal. Forward cross-talk creates a signal that propagates in the same direction as the aggressor's signal. On the AGTL+ bus, a driver on the aggressor network is not at the end of the network; therefore it sends signals in both directions on the aggressor's network. Figure 3-4 shows a driver on the aggressor network and a receiver on the victim network that are not at the ends of the network. The signal propagating in each direction causes cross-talk on the victim network.

Figure 3-4. Aggressor and Victim Networks

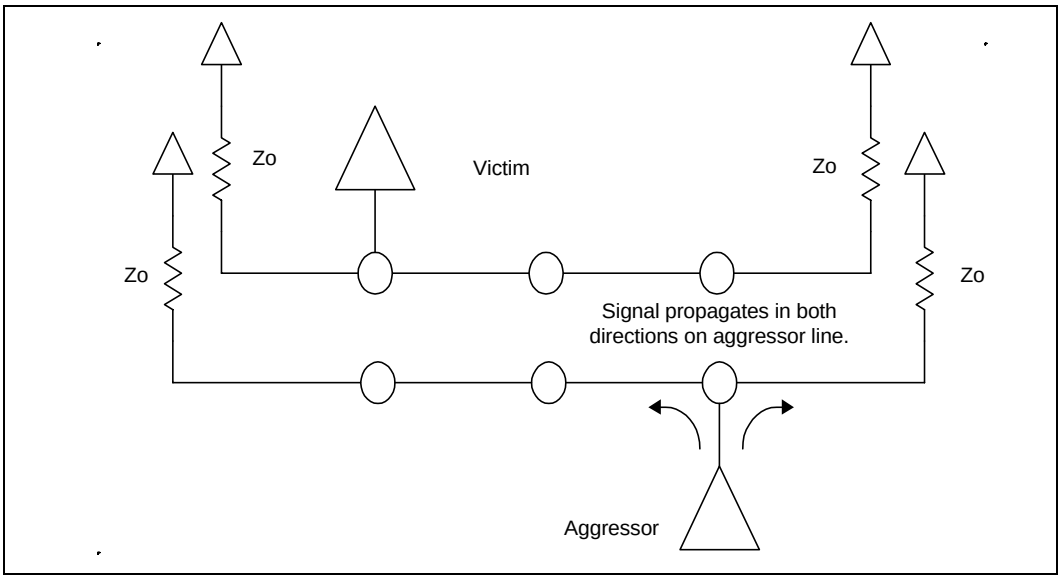
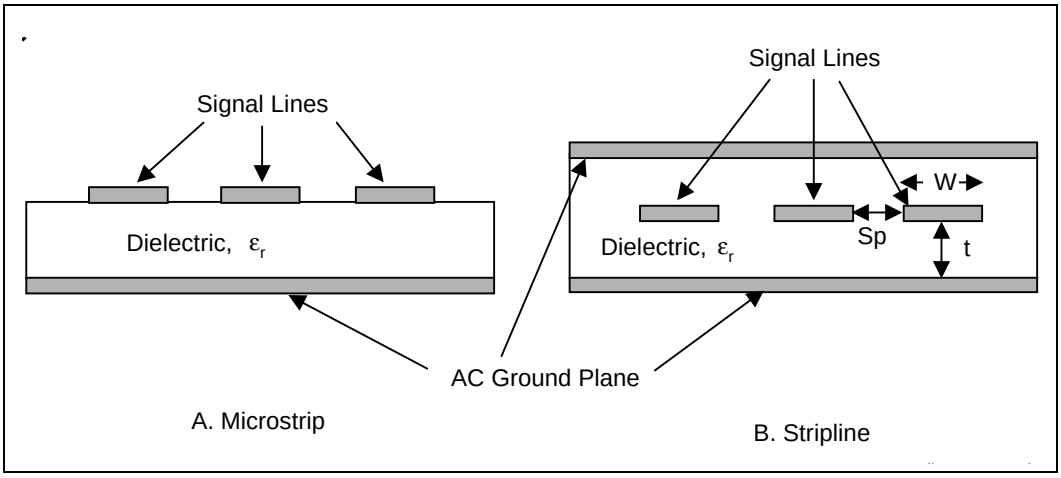


Figure 3-5. Transmission Line Geometry: (A) Microstrip (B) Stripline



Additional aggressors are possible in the z-direction, if adjacent signal layers are not routed in mutually perpendicular directions. Because cross-talk-coupling coefficients decrease rapidly with increasing separation, it is rarely necessary to consider aggressors that are at least five line widths separated from the victim. The maximum cross-talk occurs when all the aggressors are switching in the same direction at the same time.

There is cross-talk internal to the IC packages, which can also affect the signal quality.

Backward cross-talk is present in both stripline and microstrip geometry's (see Figure 3-5). A way to remember which geometry is stripline and which is microstrip is that a stripline geometry requires **stripping** a layer away to see the signal lines. The backward coupled amplitude is proportional to the backward cross-talk coefficient, the aggressor's signal amplitude, and the coupled length of the network up to a maximum that is dependent on the rise/fall time of the aggressor's signal. Backward cross-talk reaches a maximum (and remains constant) when the

propagation time on the coupled network length exceeds one half of the rise time of the aggressor's signal. Assuming the ideal ramp on the aggressor from 0% to 100% voltage swing, and the fall time on an unloaded coupled network, then:

$$LengthforMaxBackwardCrosstalk = \frac{\frac{1}{2} \times FallTime}{BoardDelayPerUnitLength}$$

An example calculation follows when the fast corner fall time is 3 V/ns and board delay is 175 ps/inch (2.1 ns/foot):

Fall time = 1.5 V÷3 V/ns = 0.5 ns

Length for Max Backward Cross-talk

= ½ * 0.5 ns * 1000 ps/ns ÷175 ps/in

= 1.43 inches

Agents on the AGTL+ bus drive signals in each direction on the network. This causes backward cross-talk from segments on two sides of a driver. The pulses from the backward cross-talk travel toward each other and meet and **add** at certain moments and positions on the bus. This can cause the voltage (noise) from cross-talk to double.

3.3.3.1 Potential Termination Cross-Talk Problems

The use of commonly used "pull-up" resistor networks for AGTL+ termination may not be suitable. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). These packages generally have too much inductance to maintain the voltage/current needed at each resistive load. Intel recommends using discrete resistors, resistor networks with separate power/ground pins for each resistor, or working with a resistor network vendor to obtain resistor networks that have acceptable characteristics.

3.4 More Details and Insight

3.4.1 Textbook Timing Equations

The “textbook” equations used to calculate the propagation rate of a PCB are the basis for spreadsheet calculations for timing margin based on the component parameters. These equations are:

Equation 3-6. Intrinsic Impedance

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \quad (\Omega)$$

Equation 3-7. Stripline Intrinsic Propagation Speed

$$S_{0\_STRIPLINE} = 1.017 * \sqrt{\varepsilon_r} \quad (\text{ns/ft})$$

Equation 3-8. Microstrip Intrinsic Propagation Speed

$$S_{0\_MICROSTRIP} = 1.017 * \sqrt{0.475 * \varepsilon_r + 0.67} \quad (\text{ns/ft})$$

Equation 3-9. Effective Propagation Speed

$$S_{EFF} = S_0 * \sqrt{1 + \frac{C_D}{C_0}} \quad (\text{ns/ft})$$

Equation 3-10. Effective Impedance

$$Z_{EFF} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}} \quad (\Omega)$$

Equation 3-11. Distributed Trace Capacitance

$$C_0 = \frac{S_0}{Z_0} \quad (\text{pF/ft})$$

Equation 3-12. Distributed Trace Inductance

$$L_0 = 12 * Z_0 * S_0 \quad (\text{nH/ft})$$

Symbols for Equation 3-5 through Equation 3-12:

- S_0 is the speed of the signal on an unloaded PCB in ns/ft. This is referred to as the board propagation constant.
- $S_{0\ MICROSTRIP}$ and $S_{0\ STRIPLINE}$ refer to the speed of the signal on an unloaded microstrip or stripline trace on the PCB in ns/ft.
- Z_0 is the intrinsic impedance of the line in Ω and is a function of the dielectric constant (ε_r), the line width, line height and line space from the plane(s). The equations for Z_0 are not included in this document. See the *MECL System Design Handbook* by William R. Blood, Jr. for these equations.
- C_0 is the distributed trace capacitance of the network in pF/ft.
- L_0 is the distributed trace inductance of the network in nH/ft.
- C_D is the sum of the capacitance of all devices and stubs divided by the length of the network's trunk, not including the portion connecting the end agents to the termination resistors in pF/ft.
- S_{EFF} and Z_{EFF} are the effective propagation constant and impedance of the PCB when the board is "loaded" with the components.

3.4.2 Effective Impedance and Tolerance/Variation

The impedance of the PCB needs to be controlled when the PCB is fabricated. The method of specifying control of the impedance needs to be determined to best suit each situation. Using stripline transmission lines (where the trace is between two reference planes) is likely to give better results than microstrip (where the trace is on an external layer using an adjacent plane for reference with solder mask and air on the other side of the trace). This is in part due to the difficulty of precise control of the dielectric constant of the solder mask, and the difficulty in limiting the plated thickness of microstrip conductors, which can substantially increase cross-talk.

The effective line impedance (Z_{EFF}) is recommended to be 60 Ω ±15%, where Z_{EFF} is defined by Equation 3-10.

3.4.3 Power/Reference Planes, PCB Stackup, and High Frequency Decoupling

3.4.3.1 Power Distribution

Designs using the Pentium III processor require several different voltages. The following paragraphs describe some of the impact of two common methods used to distribute the required voltages. Refer to the *Flexible Motherboard Power Distribution Guidelines* for more information on power distribution.

The most conservative method of distributing these voltages is for each of them to have a dedicated plane. If any of these planes are used as an "AC ground" reference for traces to control trace impedance on the board, then the plane needs to be AC coupled to the system ground plane. This method may require more total layers in the PCB than other methods. A 1-ounce/ft^2 thick copper is recommended for all power and reference planes.

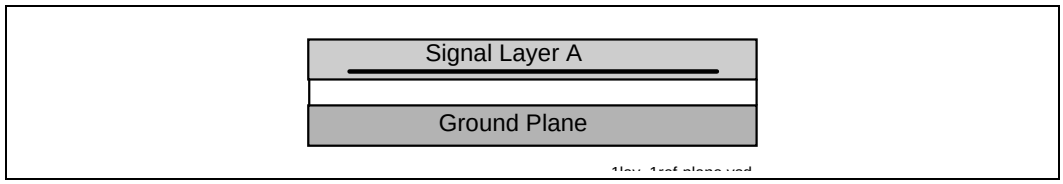
A second method of power distribution is to use partial planes in the immediate area needing the power, and to place these planes on a routing layer on an as-needed basis. These planes still need to be decoupled to ground to ensure stable voltages for the components being supplied. This method has the disadvantage of reducing area that can be used to route traces. These partial planes may also

change the impedance of adjacent trace layers. (For instance, the impedance calculations may have been done for microstrip geometry, and adding a partial plane on the other side of the trace layer may turn the microstrip into a stripline.)

3.4.3.2 Reference Planes and PCB Stackup

It is **strongly recommended** that baseboard stackup be arranged such that AGTL+ signals are referenced to a ground (VSS) plane, and that the AGTL+ signals do not traverse multiple signal layers. Deviating from either guideline can create discontinuities in the signal's return path that can lead to large SSO effects that degrade timing and noise margin. Designing an AGTL+ platform incorporating discontinuities will expose the platform to a risk that is very hard to predict in pre-layout simulation. Figure 3-6 shows the ideal case where a particular signal is routed entirely within the same signal layer, with a ground layer as the single reference plane.

Figure 3-6. One Signal Layer and One Reference Plane



When it is not possible to route the entire AGTL+ signal on a single VSS referenced layer, there are methods to reduce the effects of layer switches. The best alternative is to allow the signals to change layers while staying referenced to the same plane (see Figure 3-7). Figure 3-8 shows another method of minimizing layer switch discontinuities, but may be less effective than Figure 3-7. In this case, the signal still references the same type of reference plane (ground). In such a case, it is important to stitch (i.e., connect) the two ground planes together with vias in the vicinity of the signal transition via.

Figure 3-7. Layer Switch with One Reference Plane

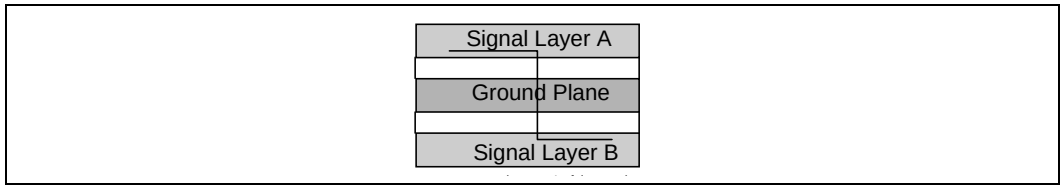
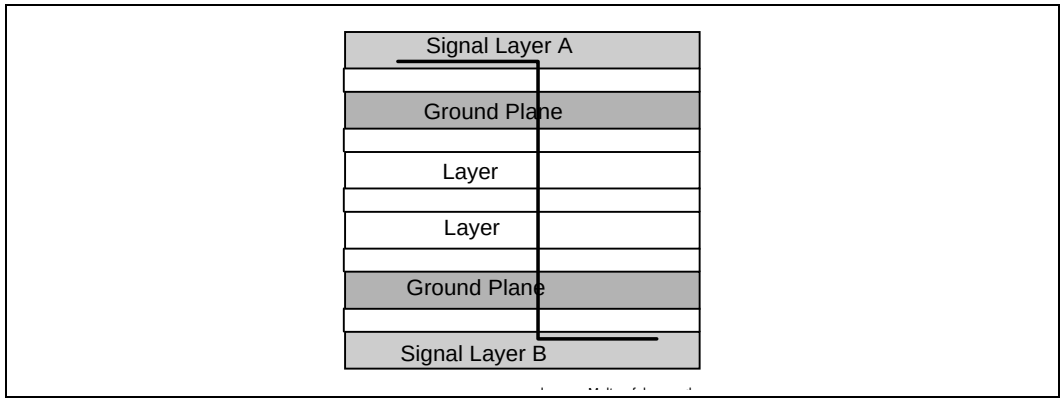


Figure 3-8. Layer Switch with Multiple Reference Planes (same type)



When routing and stackup constraints require that an AGTL+ signal reference VCC or multiple planes, special care must be given to minimize the SSO impact to timing and noise margin. The best method of reducing adverse effects is to add high-frequency decoupling wherever the transitions occur, as shown in Figure 3-9 and Figure 3-10. Such decoupling should, again, be in the vicinity of the signal transition via and use capacitors with minimal effective series resistance (ESR) and effective series inductance (ESL). When placing the caps it is recommended to space the VSS and VCC vias as close as possible and/or use dual vias since the via inductance may sometimes be higher than the actual capacitor inductance.

Figure 3-9. Layer Switch with Multiple Reference Planes

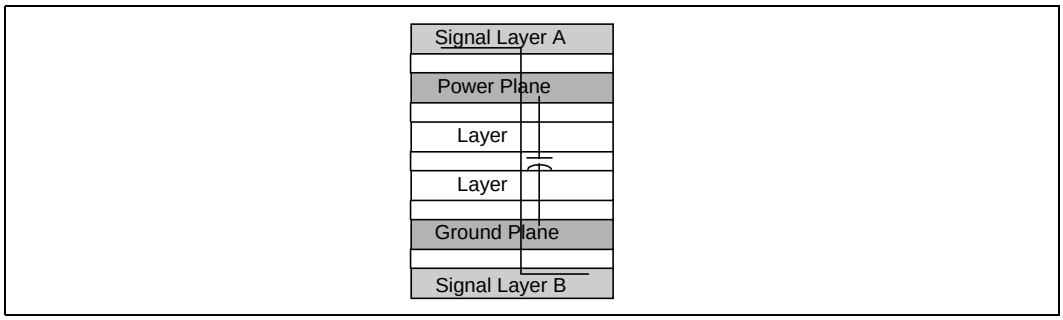
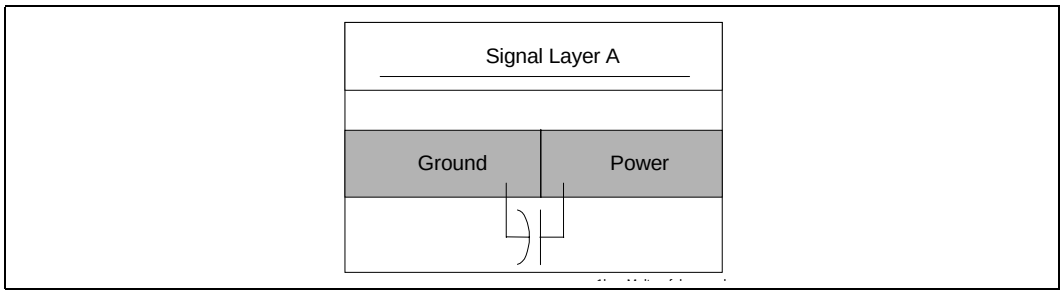


Figure 3-10. One Layer with Multiple Reference Planes



3.4.3.3 High Frequency Decoupling

This section contains several high frequency decoupling recommendations that will improve the return path for an AGTL+ signal. These design recommendations will very likely reduce the amount of SSO effects.

Just as layer switching and multiple reference planes can create discontinuities in an AGTL+ signal return path, discontinuities may also occur when a signal transitions between the baseboard and cartridge. Therefore, providing adequate high-frequency decoupling across VCC_{CORE} and ground at the SC242 connector interface on the baseboard will minimize the discontinuity in the signal's reference plane at this junction. Note that these additional high-frequency decoupling capacitors are in addition to the high-frequency decoupling already on the processor.

Transmission line geometry also influences the return path of the reference plane. The following are decoupling recommendations that take this into consideration:

- A signal that transitions from a stripline to another stripline should have close proximity decoupling between all four reference planes.
- A signal that transitions from a stripline to a microstrip (or vice versa) should have close proximity decoupling between the three reference planes.
- A signal that transitions from a stripline or microstrip through vias or pins to a component (Intel 82820 MCH, etc.) should have close proximity decoupling across all involved reference planes to ground for the device.

3.4.3.4 SC242 Connector

Intel studies indicate that the use of thermal reliefs on the connector pin layout pattern (especially ground pins) should be minimized. Such reliefs (cartwheels or wagon-wheels) increase the net ground inductance and reduce the integrity of the ground plane to which many signals are referenced. Increased ground inductance has been shown to aggravate SSO effects. Also, the anti-pad diameters (clearance holes in the planes) for the signal pins should be minimized since large anti-pads also reduce the integrity of the ground plane and increase inductance.

Some additional layout and EMI-reduction guidelines regarding the SC242 connector follow:

- Extend power/ground planes up to the SC242 connector pins.
- Extend the reference planes for AGTL+ and other controlled-impedance signals up to the SC242 connector pins.
- Minimize or remove thermal reliefs on power/ground pins.
- Route V_{TT} power with the widest signal trace or mini-plane as possible. Place decoupling caps across V_{TT} and ground in the vicinity of the connector pins.
- Use a ground plane under the principal component side of the baseboard (and secondary side if it contains active components).
- Distribute decoupling capacitors across power and ground pins evenly around the connector (less than 0.5 inch spacing) on the primary and secondary sides.
- Minimize serpentine traces on outer layers.

3.4.4 Clock Routing

Analog simulations are required to ensure clock net signal quality and skew is acceptable. The system clock skew must be kept to a minimum (The calculations and simulations for the example topology given in this document have a total clock skew of 200 ps and 150 ps of clock jitter). For a given design, the clock distribution system, including the clock components, must be evaluated to ensure these same values are valid assumptions. Each processor's datasheet specifies the clock signal quality requirements. To help meet these specifications, follow these general guidelines:

- Tie clock driver outputs if clock buffer supports this mode of operation.
- Match the electrical length and type of traces on the PCB (microstrip and stripline may have different propagation velocities).
- Maintain consistent impedance for the clock traces.
  - — Minimize the number of vias in each trace.
  - — Minimize the number of different trace layers used to route the clocks.
  - — Keep other traces away from clock traces.
- Lump the loads **at the end** of the trace if multiple components are to be supported by a single clock output.
- Have equal loads at the end of each network.

The **ideal** way to route each clock trace is on the same single inner layer, next to a ground plane, isolated from other traces, with the same total trace length, to the same type of single load, with an equal length ground trace parallel to it, and driven by a zero skew clock driver. When deviations from ideal are required, going from a single layer to a pair of layers adjacent to power/ground planes would be a good compromise. The fewer number of layers the clocks are routed on, the smaller the impedance difference between each trace is likely to be. Maintaining an equal length

and parallel ground trace for the **total length of each** clock ensures a low inductance ground return and produces the minimum current path loop area. (The parallel ground trace will have lower inductance than the ground plane because of the mutual inductance of the current in the clock trace.)

3.5 Definitions of Flight Time Measurements/ Corrections and Signal Quality

Acceptable signal quality must be maintained over all operating conditions to ensure reliable operation. Signal Quality is defined by four parameters: Overshoot, Undershoot, Settling Limit, and Ringback. Timings are measured at the pins of the driver and receiver, while signal integrity is observed at the receiver chip pad. When signal integrity at the pad violates the following guidelines and adjustments need to be made to flight time, the adjusted flight time obtained at the chip pad can be assumed to have been observed at the package pin, usually with a small timing error penalty.

3.5.1 V_{REF} Guardband

To account for noise sources that may affect the way an AGTL+ signal becomes valid at a receiver, V_{REF} is shifted by ΔV_{REF} for measuring minimum and maximum flight times. The V_{REF} Guardband region is bounded by V_{REF}-ΔV_{REF} and V_{REF}+$\Delta V_{REF.}$ ΔV_{REF} has a value of 100 mV, which accounts for the following noise sources:

- Motherboard coupling
- V_{TT} noise
- V_{REF} noise

3.5.2 Ringback Levels

The example topology covered in this guideline assumes ringback tolerance allowed to within 200 mV of 2/3 V_{TT}. Since V_{TT} is specified with approximate total ±11% tolerance, this implies a 2/3 V_{TT} (V_{REF}) range from approximately 0.89 V to 1.11 V. This places the absolute ringback limits at:

- 1.3 V (1.1 V + 200 mV) for rising edge ringback
- 0.69 V (0.89 V – 200 mV) for falling edge ringback

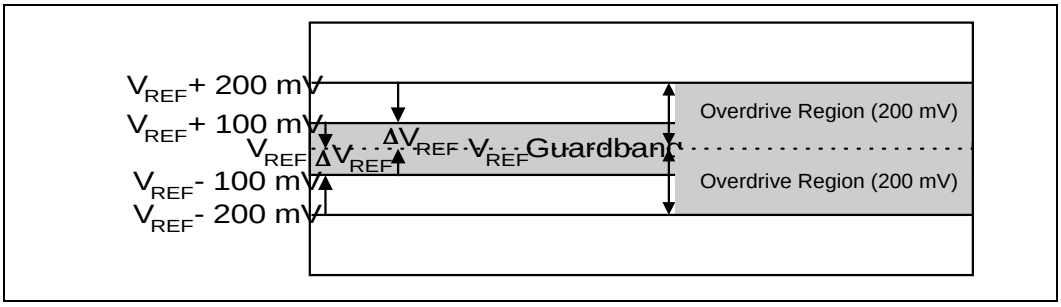
A violation of these ringback limits requires flight time correction as documented in the *Intel® Pentium® II Processor Developer's Manual*.

3.5.3 Overdrive Region

The overdrive region is the voltage range, at a receiver, from V_{REF} to V_{REF} + 200 mV for a low-to-high going signal and V_{REF} to V_{REF} - 200 mV for a high-to-low going signal. The overdrive regions encompass the V_{REF} Guardband. So, when V_{REF} is shifted by ΔV_{REF} for timing measurements, the overdrive region **does not** shift by ΔV_{REF}. Figure 3-11 depicts this relationship. Corrections for edge rate and ringback are documented in the *Intel® Pentium® II Processor Developer's Manual*. However, there is an exception to the documented correction method. The *Intel®Pentium® II Processor Developer's Manual* states that extrapolations should be made from the last crossing of the overdrive region back to V_{REF}. Simulations performed on this topology

should extrapolate back to the appropriate V_{REF} Guardband boundary, and not V_{REF}. So, for maximum rising edge correction, extrapolate back to $V_{REF} + \Delta V_{REF}$. For maximum falling edge corrections, extrapolate back to $V_{REF} - \Delta V_{REF}$.

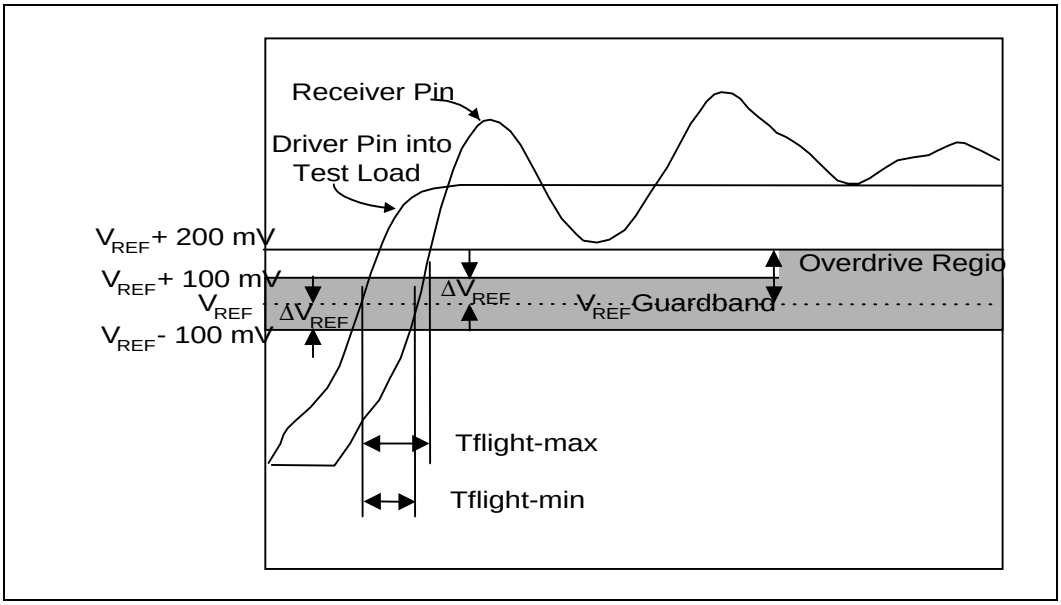
Figure 3-11. Overdrive Region and V_{REF} Guardband



3.5.4 Flight Time Definition and Measurement

Timing measurements consist of minimum and maximum flight times to take into account that devices can turn on or off anywhere in a V_{REF} Guardband region. This region is bounded by V_{REF}-ΔV_{REF} and V_{REF}+ΔV_{REF}. The minimum flight time for a rising edge is measured from the time the driver crosses V_{REF} when terminated to a test load, to the time when the signal first crosses V_{REF}-ΔV_{REF} at the receiver (see Figure 3-12). Maximum flight time is measured to the point where the signal first crosses V_{REF}+ΔV_{REF}, assuming that ringback, edge rate, and monotonicity criteria are met. Similarly, minimum flight time measurements for a falling edge are taken at the V_{REF}+ΔV_{REF} crossing and maximum flight time is taken at the V_{REF}-ΔV_{REF} crossing.

Figure 3-12. Rising Edge Flight Time Measurement



3.6 Conclusion

AGTL+ routing requires a significant amount of effort. Planning ahead and leaving the necessary time available for correctly designing a board layout will provide the designer with the best chance of avoiding the more difficult task of debugging inconsistent failures caused by poor signal integrity. Intel recommends planning a layout schedule that allows time for each of the tasks outlined in this document.

4

Clocking

This page is intentionally left blank.

Clocking 4

4.1 Clock Generation

There are two clock generator components required in an Intel® 820 chipset based system. The Direct Rambus* Clock Generator (DRCG) generates clock for the Direct Rambus* interface while the CK133 component generates clocks for the rest of the system. Clock synthesizers that meet the Intel CK98 Clock Specification are suitable for an Intel® 820 chipset based system. The CK133 generates the clocks listed in Table 4-1.

Table 4-1. Intel® 820 Chipset Platform System Clocks

Number	Name on CK133	Used for	Routed to	Name on Receiver	Frequency	Voltage
4	CPUCLK[0-3]	System Bus Clock	2 Processors	CLK	100/133 MHz	2.5V
			MCH	HCLKIN		
			ITP	BCLK		
3	APIC[0-2]	APIC Bus Clock	2 Processors	PICCLK	33 MHz	2.5V
			ICH	APICCLK		
8	PCICLK[1-7,F]	PCI Bus Clock	5 PCI Devices	CLK	33 MHz	3.3V
		PCI, LPC, FWH Flash BIOS Bus Clock	ICH	PCICLK		
		FWH Flash BIOS Interface Clock	FWH Flash BIOS	CLK		
		LPC Interface Clock	LPC	CLK		
4	3V66[0-3]	Hub Interface/AGP Bus Clock	MCH	CLK66	66 MHz	3.3V
		Hub Interface Clock	ICH	CLK66		
		AGP Bus Clock	AGP device/ slot	CLK		
		Unused	N/A	N/A		
2	REF[0-1]	Internal ICH Logic	ICH	CLK14	14 MHz	3.3V
		Internal Super I/O Logic	Super I/O	Vendor Specific		
1	48 MHz	USB	ICH	CLK48	48 MHz	3.3V
2	CPU_DIV2[0-1]	DRCG Reference Clock	DRCG	REFCLK	50/66 MHz	2.5V
		Unused	N/A	N/A		

The CK133 is a mixed voltage component. Some of the output clocks are 3.3V and some of the output clock are 2.5V. As a result, the CK133 device requires both 3.3V and 2.5V. These power supplies should be a clean as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines.

The MCH uses the same clock for hub interface and AGP. It is important that the hub interface/AGP clocks are routed to ensure the skew requirements are met between:

- The MCH hub interface/AGP clock and the AGP connector (or device)

- The MCH hub interface/AGP clock and the ICH hub interface clock.

The DRCG reference clock operates at one-half the CPU clock frequency. It is an input into the DRCG and is used to generate the Direct RDRAM “Clock to Master” differential pair (CTM, CTM#).

The DRCG generates one pair of differential Direct RDRAM Clocks (CTM, CTM#) from the reference clock generated by the CK133. In addition, the DRCG uses phase information provided by the MCH to phase align the direct RDRAM clock with the CPU clocks. This phase alignment information is provided to the DRCG via the SYNCLKN and PCLKM pins.

Figure 4-1. Intel® 820 Chipset Platform Clock Distribution

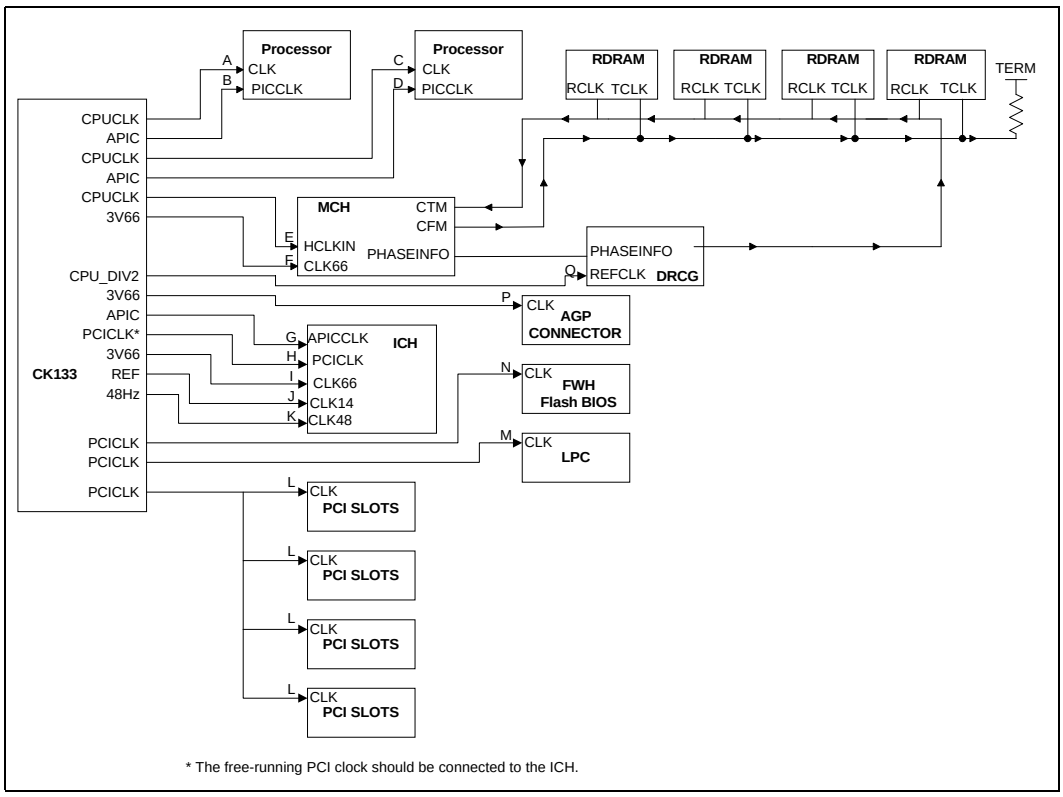


Table 4-2. Intel® 820 Chipset Platform Clock Skews

Clock Symbols See Figure 4-1	Relationship	Skew						Notes
		Pin-to-Pin (ps)		Board (ps)		Total (ps)		
		Min	Max	Min	Max	Min	Max	
A leads C, A leads E (or C leads E)	SC242 HCLK to SC242 HCLK (DP ONLY) And SC242 HCLK to MCH HCLK (DP ONLY)	-175	+175	-125	+125	-300	+300	1, 7
A leads E	SC242 HCLK to MCH HCLK (UP ONLY)	0	0	-125	+125	-125	+125	2, 3, 7
P leads F	MCH CLK66 to AGP graphics device AGPCLK	0	0	-125	+125	-125	+125	4, 8
L leads another L (or L leads H)	PCICLK to PCICLK	-500	+500	-1500	+1500	-2000	+2000	
I leads H	ICH CLK66 leads ICH PCICLK	+1500	+4000	-500	+500	+1000	+4500	
F leads I	ICH CLK66 to MCH CLK66	-250	250	-125	+125	-375	+375	8
Worst case skew between H, L, M and N	Worst case FWHCLK, LPCCLK, PCICLK	-500	+500	-1500	+1500	-2000	+2000	5
B leads D, B leads G	Processor PICCLK leads Processor PICCLK And Processor PICCLK leads ICH APICCLK	-250	+250	-125	+125	-375	+375	6

NOTES:
1. DP Only
2. UP: MCH and CPU clock drivers are tied together to eliminate pin-to-pin skew. –175 and +175 pin-to-pin skew only apply to DP.
3. UP Only
4. Clock drivers tied together to eliminate pin-to-pin skew.
5. The skew between any PCICLK clocks on any two inputs in the system.
6. The skew between any APIC clocks on any two inputs in the system.
7. If SSC is enabled, an additional ±40ps must is added to the pin-to-pin skew
8. If SSC is enabled, an additional ±60ps must is added to the pin-to-pin skew

Figure 4-2 shows the Intel® 820 chipset clock length routing guidelines.

Figure 4-2. Intel® 820 Chipset Clock Routing Guidelines[1,2]

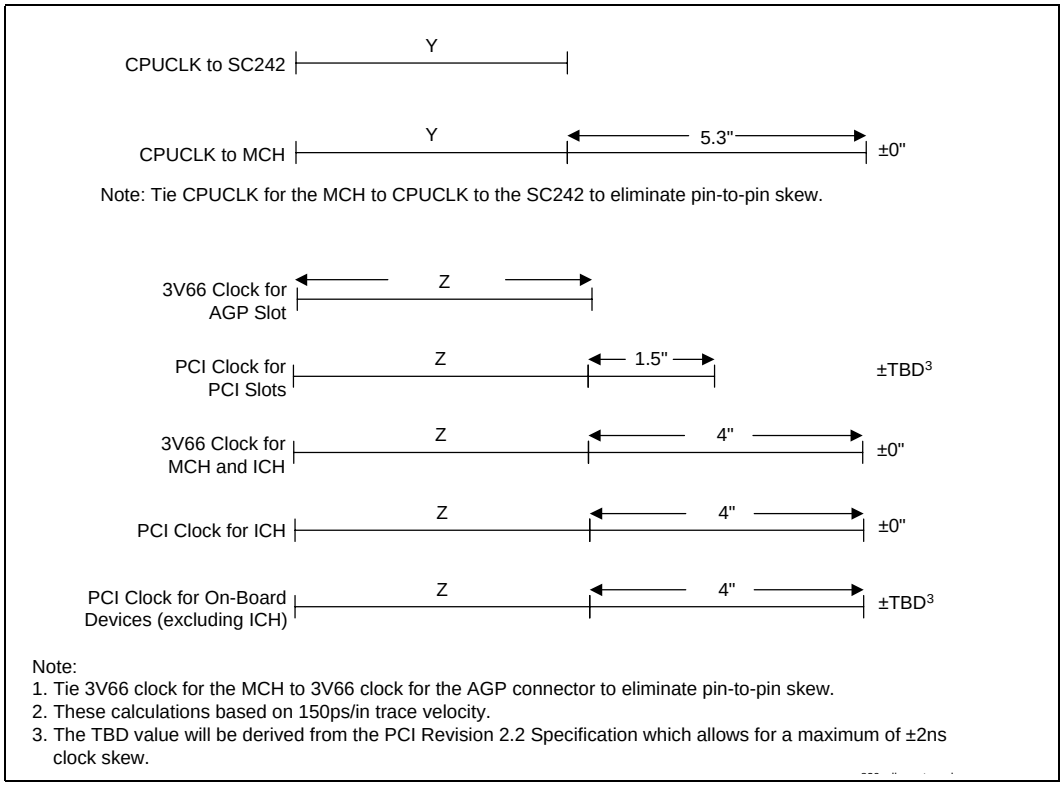


Table 4-3. Intel® 820 Chipset Platform System Clock Cross-Reference

CK133/DRCG Pin Name	Component	Pin Name
PCICLK	PCI Slot	CLK
	PCI Slot	CLK
	PCI Slot	CLK
	PCI Slot	CLK
	PCI Slot	CLK
	ICH	PCICLK-F
	LPC Super I/O	CLK
	FWH Flash BIOS	CLK
3V66	MCH	GCLKIN
	ICH	CLK66
	AGP Connector (on-board device)	CLK
48 MHz	ICH	CLK48
CPUCLK	CPU	BCLK
	CPU	BCLK
	MCH	HCLKIN
CPU_div2	DRCG	Refclk
APIC	CPU	PICCLK
	CPU	PICCLK
	ICH	APICCLK
Clk/ClkB[1]	RDRAMs	
	MCH	CTM/CTM#
CFM/CFM#[1,2]	RDRAMs	
PclkM	MCH	HCLKOUT
SynclkN	MCH	RCLKOUT

NOTES:
1. Differential Clocking Pair
2. CFM/CFM# driven by MCH

4.2 Component Placement and Interconnection Layout Requirements

Detailed explanation of layout requirements for each interconnections are provided in the following sections:

- Crystal to CK133
- CK133 to DRCG
- MCH to DRCG
- DRCG to RDRAM channel

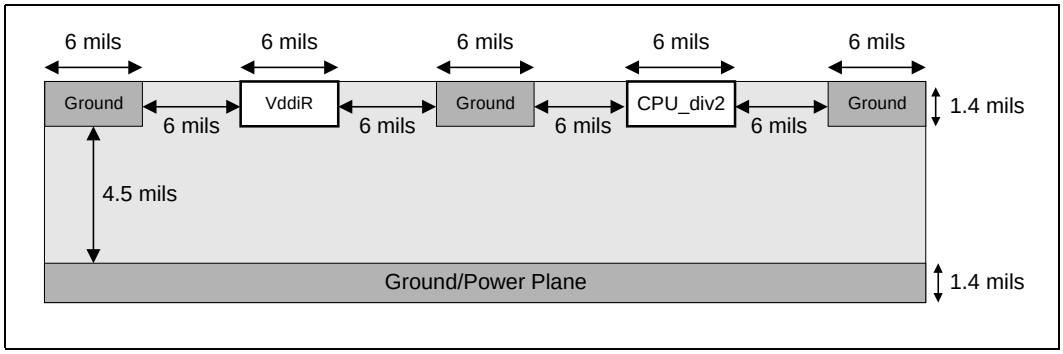
4.2.1 14.318 MHz Crystal to CK133

The distance between the crystal and the CK133 should be minimized. The maximum trace length is 500 mils.

4.2.2 CK133 to DRCG

- CPU_div2
- VDDIR – Used as a reference for 2.5V signaling

Figure 4-3. CK133 to DRCG Routing Diagram

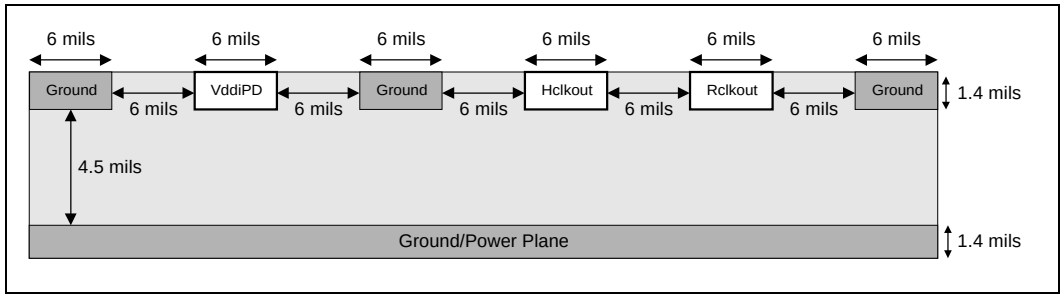


VddIR and CPU_div2 must be routed as shown in Figure 4-3. Note that the VddiR pin can be connected directly to 2.5V near the DRCG if the 2.5V plane extends near the DRCG. However, if a 2.5V trace must be used, it should originate at the CK133 and be routed as shown.

4.2.3 MCH to DRCG

- PclkM
- PclkN
- VddIPD

Figure 4-4. MCH to DRCG Routing Diagram

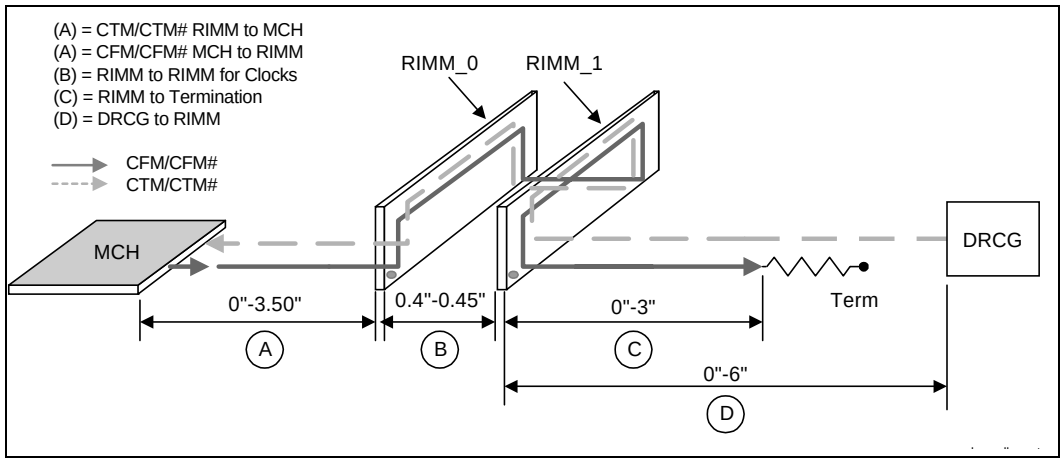


The Hclkout, Rclkout and VddiPD should be routed as shown in Figure 4-4. Note that the VddiPD pin can be connected directly to 1.8V near the DRCG if the 1.8V plane extends near the DRCG. However, if a 1.8V trace must be run, it should originate at the MCH and be routed as shown.

The maximum length for Hclkout and Rclkout is 6". Additionally, Hclkout and Rclkout must be length matched (to each other) within 50 mils. These signals should be routed on the same layer. If the signals must switch layers, then BOTH signals should change layers together.

If VddiPD is connected to the 1.8V plane using a via (e.g., a trace is not run from the MCH), Hclkout and Rclkout must still be routed differentially and ground isolated.

Figure 4-5. Direct Rambus* Clock Routing Dimensions



4.2.4 DRCG to RDRAM Channel

The Direct Rambus* clock signals (CTM/CTM# and CFM/CFM#) are high-speed, impedance matched transmission lines. The Direct Rambus* clocks begin at the end of the Direct Rambus* channel and propagate to the controller as CTM/CTM# (see Figure 4-5), where it loops back as CFM/CFM#. Table 4-4 lists the placement guidelines.

Table 4-4. Placement Guidelines for Motherboard Routing Lengths

Direct Rambus* Clock Routing Length Guidelines				
Clock	**From**	**To**	**Length (inches)**	**Section***
CTM/CTM#	DRCG	Last RIMM Connector	0.000 – 6.000	D
	RIMM	RIMM	0.400 – 0.450	B
	1st RIMM Connector	Chipset	0.000 – 3.500	A
CFM/CFM#	Chipset	1st RIMM Connector	0.000 – 3.500	A
	RIMM	RIMM	0.400 – 0.450	B
	Last RIMM Connector	Termination	0.000 – 3.000	C

NOTE: * Refer to Figure 4-5

Trace Geometry

In Sections labeled ‘A’ and ‘D’ (Figure 4-5) the clock signals (CTM/CTM# and CFM/CFM#) must be 14 mils wide and routed as shown in Figure 4-6. For all other sections (‘B’ and ‘C’) the clock signals must be routed with 18 mil wide traces. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. The 22 mil ground isolation traces must be connected to ground with a via every 1”. A 6 mil gap is required between the clock signals and the ground isolation traces. For the section labeled “A” in Figure 4-5, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clocks faster trace velocity as described in Section 2.6.2.1, “RSL Routing” on page 2-8. The CTM/CTM# and the CFM/CFM# differential signal pairs must be length matched to ±2 mils in line section labeled ‘A’ and for the line sections labeled ‘B’ using the trace length methods in Section 2.6.2.1, “RSL Routing” on page 2-8. For the section labeled ‘D’ the trace length matching for CTM/CTM# is ±2 mils, **and for the section labeled ‘C’, ±2 mil trace length matching is required for the CFM/CFM# signals.**

The CTM/CTM# signals must be ground referenced (with a continuous ground island/plane) from the DRCG to the Last RIMM.

4.2.5 Trace Length

For the section labeled “A” in Figure 4-5 (1st RIMM to MCH and MCH to 1st RIMM), CTM/CTM# and CFM/CFM# must be length matched within ±2 mils (exact trace length matching is recommended). **Package trace compensation (as described in** Section 2.6.2.1, “RSL Routing” on page 2-8**), via compensation, and RSL signal layer alternation must** also be completed on the clock signals. Additionally, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clocks faster trace velocity as described in Section 2.6.2.1.

For the line sections labeled ‘B’ (Figure 4-5) (RIMM to RIMM) the clock signals must be matched within ±2 mils to the trace length of every RSL signal. Exact length matching is preferred.

For the line section labeled ‘D’ (DRCG to Last RIMM) the CTM/CTM# must be length matched within ±2 mils (exactly is recommended), **and for the section labeled ‘C’, ±2 mil trace length matching is required for the CFM/CFM# signals.**

Note: Total trace length matching for the entire CTM/CTM# signal trace (Sections A+B+D) and for the CFM/CFM# signal trace (Sections A+B) is ±2 mils (exact length matching is recommended).

Figure 4-6. Differential Clock Routing Diagram (Section ‘A’, ‘C’, & ‘D’)

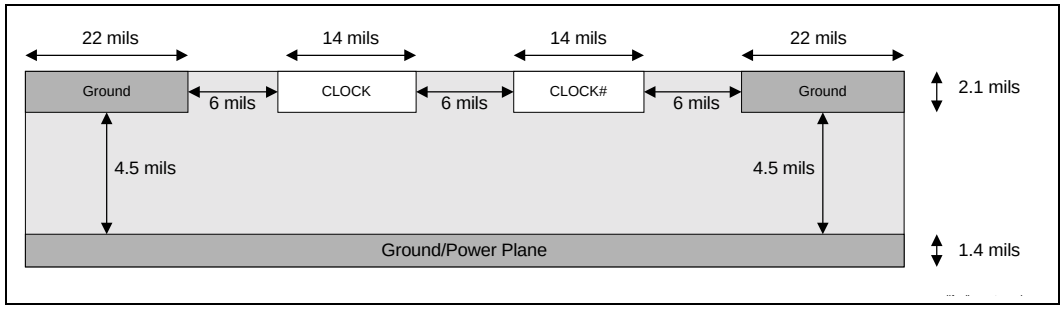
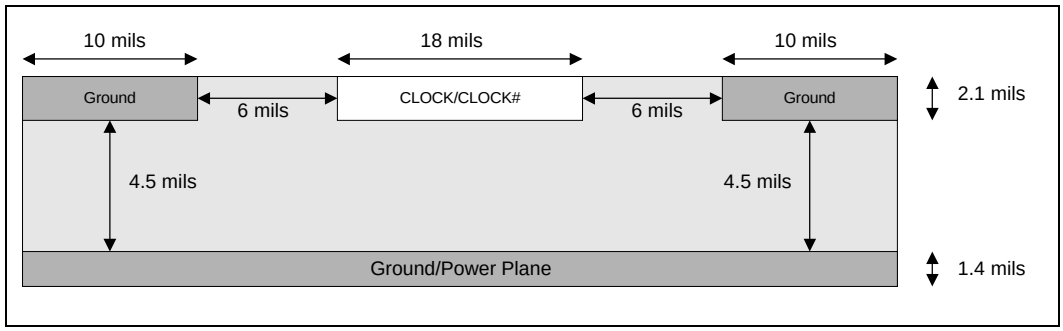
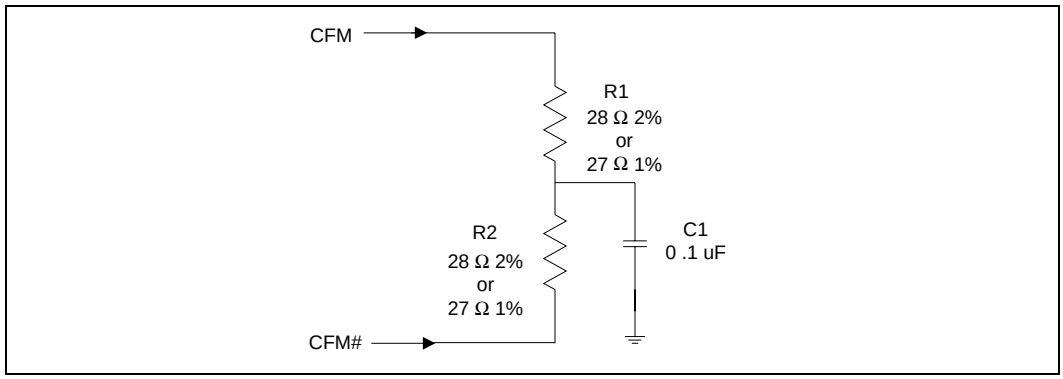


Figure 4-7. Non-Differential Clock Routing Diagram (Section ‘B’)



The CFM/CFM# differential pair signals require termination using either 27 Ω 1% or 28 Ω 2% resistors and a 0.1 uF capacitor as shown in Figure 4-8.

Figure 4-8. Termination for Direct Rambus* Clocking Signals CFM/CFM#



4.3 DRCG Impedance Matching Circuit

The external DRCG impedance matching circuit is shown in Figure 4-9. The values for the elements are listed in Table 4-5.

Figure 4-9. DRCG Impedance Matching Network

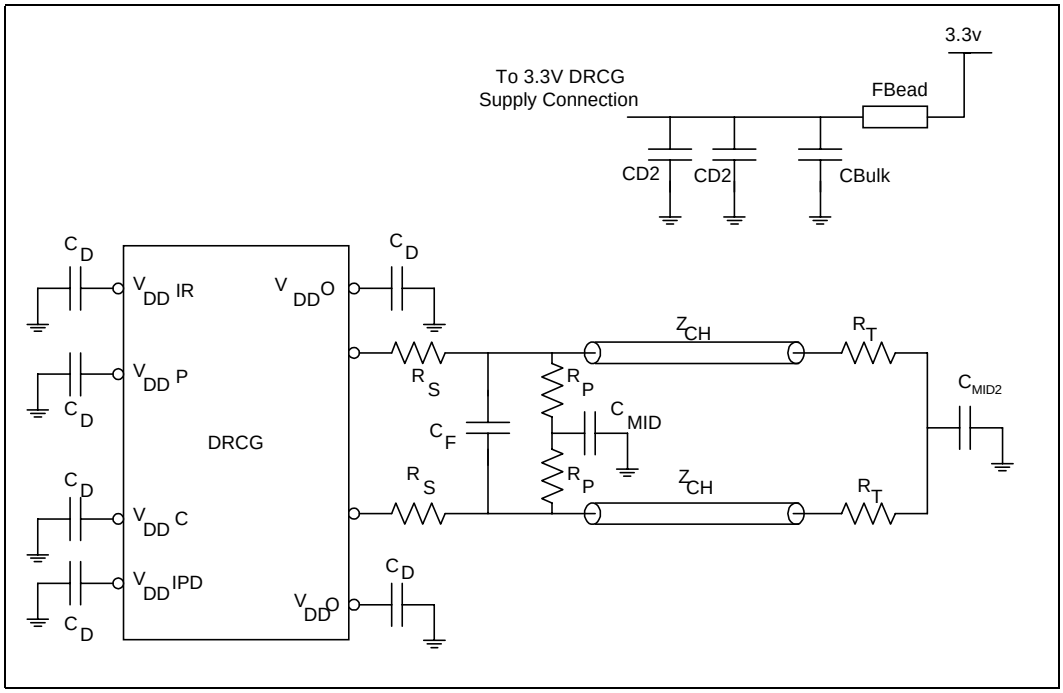


Table 4-5. External DRCG Component Values[1,2]

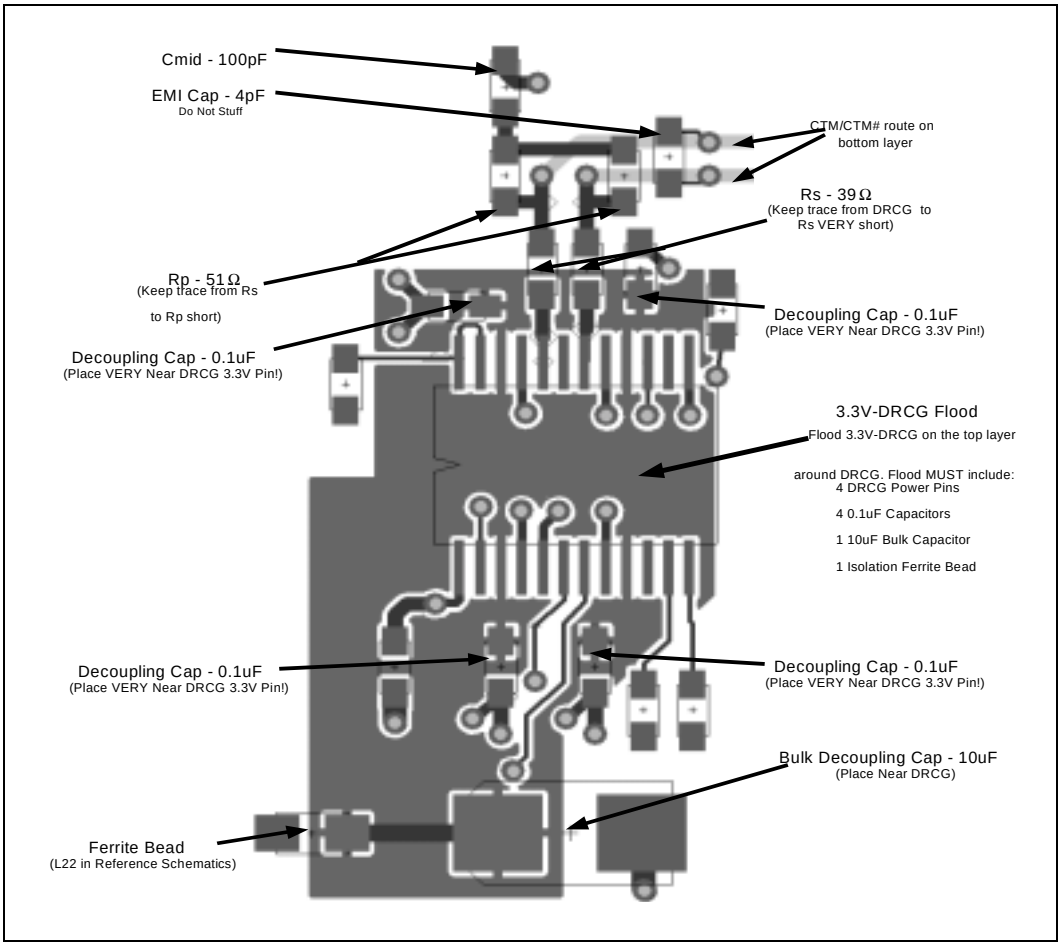
Component	Nominal Value	Notes
C_D	0.1 uF	Decoupling caps to ground
R_S	39 Ohms	Series termination resistor
R_P	51 Ohms	Parallel termination resistor
C_{MID}, C_{MID2}	0.1 uF	Virtual ground caps
R_T	27 Ohms	End of channel termination
C_F	4 pF	Do not stuff
FBead	50 Ohms at 100 MHz	Ferrite bead
CD2	0.1 uF	Additional 3.3V decoupling caps
CBulk	10 uF	Bulk cap on device side of ferrite bead

NOTES:
1. The ferrite bead and 10 uF bulk cap combination improves jitter and helps to keep the clock noise away from the rest of the system.
2. 0.1 uF capacitors are better than 0.01 uF or 0.001 uF caps for DRCG decoupling.

The circuit shown in Figure 4-9 is required to match the impedance of the DRCG to the 28 Ω channel impedance. More detailed information can be found in the Direct Rambus Clock Generator Specification.

4.3.1 DRCG Layout Example

Figure 4-10. DRCG Layout Example



4.4 AGP Clock Routing Guidelines

The AGP clock must be routed with 20 mil spacing to all other signals and it must meet the length guidelines in Figure 4-2.

4.5 Series Termination Resistors for CK133 Clock Outputs

All used outputs require series termination resistors. The recommended resistor value will be defined by simulations. The stub length to the CK133 of these resistors can be compromised to make room for decoupling caps. The rule is to keep all resistor stubs within 250 mils of the CK133. If routing rules allow, Rpacks can be used if power dissipation is not exceeded for the Rpack.

4.6 Unused Outputs

All unused clock outputs must be tied to ground through a series resistor approximately the impedance of the output buffer (shown below.) The intent of these resistors is to terminate the unused outputs to eliminate EMI.

Table 4-6. Unused Output Termination

Buffer Name	VCC Range (V)	Impedance (Ohms)	If Unused Output Termination to VSS
CPU, CPU_Div2, IOAPIC	2.375 - 2.625	13.5 - 45	30 Ohms
48 MHz, REF	3.135 - 3.465	20 - 60	40 Ohms
PCI, 3V66	3.135 - 3.465	12 - 55	33 Ohms

4.7 Decoupling Recommendation for CK133 and DRCG

Some CK133 vendors may integrate the XTAL_IN and XTAL_OUT frequency adjust capacitors. However, pads should be placed on the board for these external capacitors for testing/debug.

To further reduce jitter and voltage supply noise, the addition of a ferrite filter with 2 caps (10 uF and 0.1 uF) on both the 2.5V and 3.3V planes close to the clock devices is recommended. This applies to both DRCG and CK133.

4.8 DRCG Frequency Selection and the DRCG+

4.8.1 DRCG Frequency Selection Table and Jitter Specification

To allow additional flexibility in board design, Intel has enabled a variation of the DRCG labeled the *DRCG+*. The device has the same specifications, pinout and form-factor as the existing DRCG device document. There are two modifications made to the DRCG+.

1. The DRCG+ Mult[0:1] select table has changed to modify two of the multiplier ratios. The DRCG+ will support 133/356 MHz using 66 MHZ DRCG+ input clock and a 16/3 multiplier. An additional 9/2 multiplier allows 133/300 MHz (not supported by the Intel® 820 chipset). Support for 300 MHz and 400 MHz memory bus is unchanged. The following table lists the DRCG Ratio.

Table 4-7. DRCG Ratio

Mult[0:1]	DRCG	DRCG+
0:0	4:1	9:2
0:1	6:1	6:1
1:0	8:3	16:3
1:1	8:1	8:1

2. The Intel® 820 chipset supports the following ratios and can be supported by the DRCG and DRCG+ or derivative devices. Contact your DRCG vendor for information on DRCG, DRCG+, and derivative products.

100 MHz Host Bus		133 MHz Host Bus	
Frequency	**Multiplier**	**Frequency**	**Multiplier**
100 / 300	6:1	133 / 266	4:1
100 / 400	8:1	133 / 356	16:3
		133 / 400	6:1

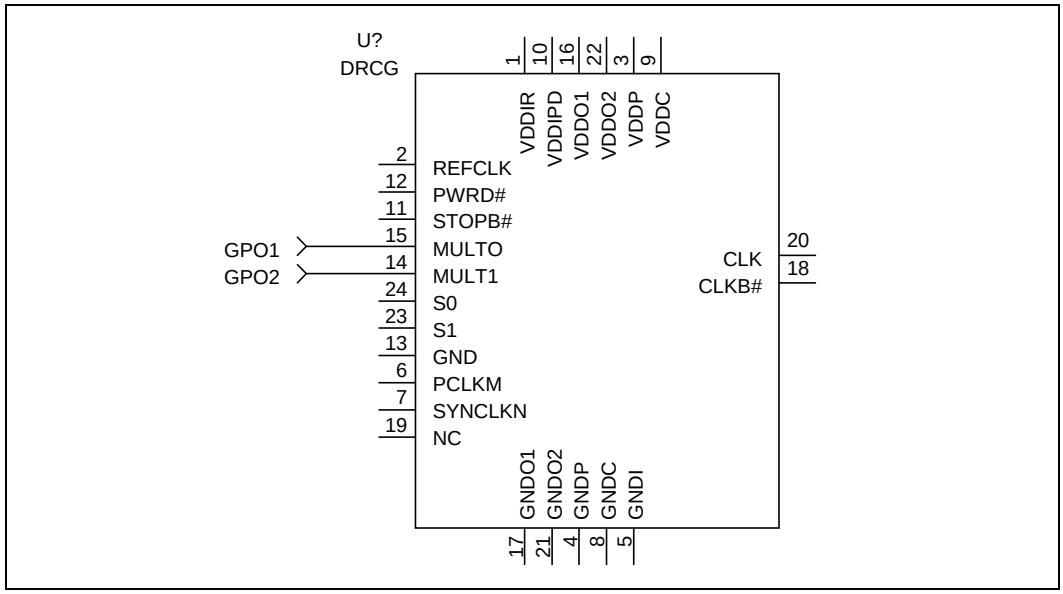
3. The jitter timing specifications are expanded to encompass both the component specification (for DRCG or derivative products) and the channel specification. Follow the component specification when measuring jitter at the DRCG output resistor. Follow the channel jitter guidelines when measuring jitter at the MCH or at the termination for CFM/CFM# on the RDRAM interface.

Output Frequency (MHz)	Component Jitter Specification	Channel Jitter Guidelines
400	50 ps	100 ps
356	60 ps	110 ps
300	70 ps	120 ps
266	80 ps	130 ps

4.8.2 DRCG+ Frequency Selection Schematic

DRCG+ frequency selection can be accomplished using two GPIOs connected to the MULT[0:1] pins as shown in Figure 4-11. This allows selection of all frequencies supported by the Intel® 820 chipset.

Figure 4-11. DRCG+ Frequency Selection



This page is intentionally left blank.

5

System Manufacturing

This page is intentionally left blank.

System Manufacturing 5

5.1 In Circuit FWH Flash BIOS Programming

All cycles destined for the FWH Flash BIOS appear on PCI. The ICH hub interface to PCI Bridge puts all processor boot cycles out on PCI (before sending them out on the FWH Flash BIOS interface to the FWH Flash BIOS). If the ICH is set for subtractive decode, these boot cycles can be accepted by a positive decode agent out on PCI. The enables the ability to boot from of a PCI card that positively decodes these memory cycles. To boot from a PCI card it is necessary to keep the ICH in subtractive decode mode. If a PCI boot card is inserted and the ICH is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot from a ROM behind the 82380AB. Once you have booted from the PCI card, you could potentially program the FWH Flash BIOS in circuit and program the ICH CMOS.

5.2 FWH Flash BIOS Vpp Design Guidelines

The Vpp pin on the FWH Flash BIOS is used for programming the flash cells. The FWH Flash BIOS supports Vpp of 3.3V or 12V. If Vpp is 12V, the flash cells will program about 50% faster than at 3.3V. However, the FWH Flash BIOS only supports 12V Vpp for 80 hours. The 12V Vpp would be useful in a programmer environment that is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3V on the motherboard.

5.3 Stackup Requirement

5.3.1 Overview

The Intel® 820 chipset platform requires a board stackup with a 4.5 mil prepreg. This change in dimension (previously, typically 7 mil) is required because of the signaling environment used for Direct RDRAM, AGP 2.0 and hub interface. The RDRAM Channel is designed for 28 Ω and mismatched impedance will cause signal reflections which will reduce voltage and timing margins. For example, with a 2X clock at 400 MHz operation, which equals a 1.25 ns sampling window, only 100 ps is allotted for total channel timing error. Channel error results not only from PCB impedance, but also PCB and Z_0 process variation. Therefore, it is critical to attain the required 28 Ω impedance.

5.3.2 PCB Materials

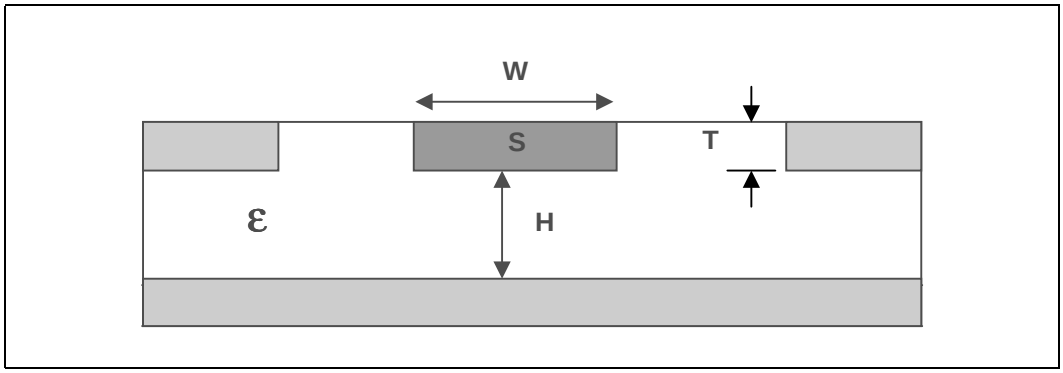
PCB tolerances determine Z_0 variation. Those tolerances include trace width, pre-preg thickness, plating thickness, and dielectric constant. Pre-preg type impacts H tolerance and ε_r including single ply, 2-ply, and resin content.

To design to the correct Z_0 variation, PCB's typically need to meet the following (see Table 5-2):

- Height tolerance ±10% (~ 0.4 mil)
- Width tolerance ±2.5% (~ 0.4 mil)
- ε_r tolerance ±5% (~0.2)

Stackup Requirement: 28Ω ±10%

Figure 5-1. 28Ω Trace Geometry



5.3.3 Design Process

To meet the tight tolerances required a good design process to use is:

- Specify the material to be used
- Calculate board geometries for the desired impedance - or use the example stackup provided
- Build test boards and coupons
- Measure board impedance using a TDR and follow Intel's Impedance Test Methodology Document (found on developer.intel.com)
- Measure geometries with cross-section
- Adjust design parameters and/or material as required
- Build a new board, re-measure the key parameters and be prepared to generate one or two board iterations

This process will require iteration: design, build, test, modify, build, test…

5.3.4 Test Coupon Design Guidelines

Characterization and understanding of the trace impedance is critical for delivering reliable systems at the increased bus frequencies. Incorporating a test coupon design into the motherboard makes testing simpler and more accurate. The test coupon pattern must match the probe type being used.

The location of the test coupon is listed in order of preference below:

- 1st Choice (Ideal Location) = Memory section of the motherboard
- 2nd Choice = Any section of the motherboard
- 3rd Choice = Separate location in the panel

The Intel Impedance Test Methodology Document should be used to ensure boards are within the 28Ω ±10% requirement. The Intel Controlled Impedance Design and Test Document should be used for the test coupon design and implementation. These documents can be found at:

http://developer.intel.com/design/chipsets/memory/rdram.htm

— Select “Application Notes”

5.3.5 Recommended Stackup

Though numerous variations of stackup are possible, it is recommended that the following should be used as a starting point:

W=18 mil, H=4.5 mil, T=2.0, 1 ply 2116 pre-preg

For other possibilities see Table 5-1 and following figures:

Table 5-1. 28Ω Stackup Examples

Sample	Zo	H	W	T	SM(max)	Resin %
1	27.1	4.3	18.0	2.1	0.6	53.0
2	28.1	3.8	18.5	1.6	1.2	72.0
3	28.6	4.8	19.0	2.5	0.7	61.0

5.3.6 Inner Layer Routing

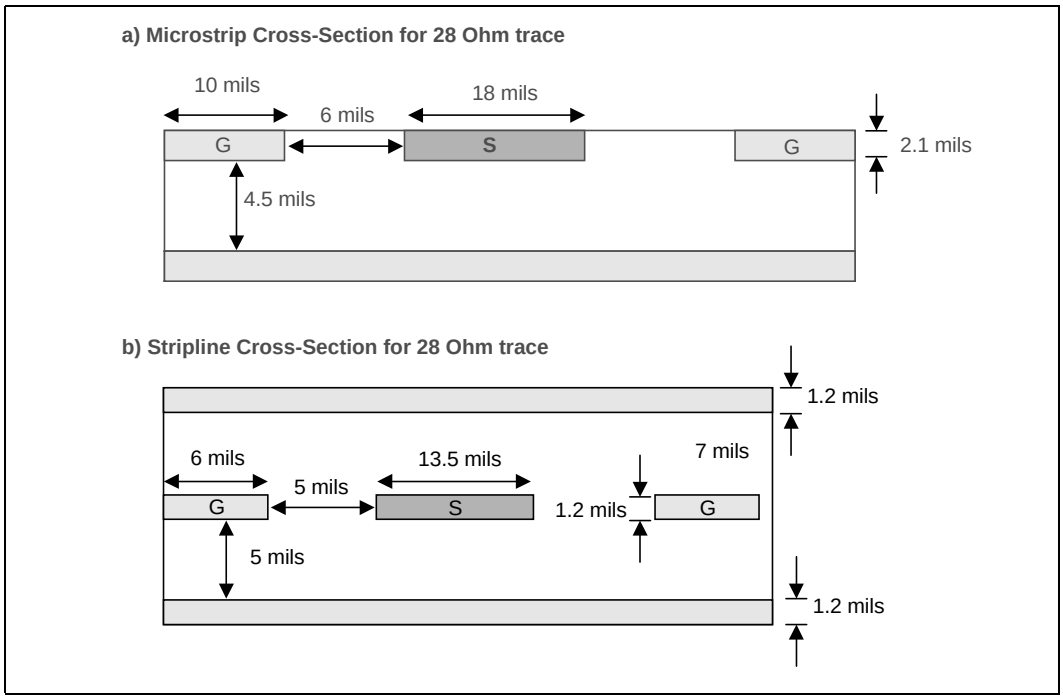
Inner Layer Routing also has many possible stackups. For Inner Layer Routing, it is recommended to use the following as a starting point:

W=13.5 mil, H1=7 mil, H2=5, T=1.2

With these parameters, initial TDR should fall within acceptable limits - 28 Ω ±10%

Figure 5-2 shows examples of both Stripline and Microstrip cross sections.

Figure 5-2. (a,b) Microstrip and Stripline Cross-section for 28 Ω Trace



Note: Don't forget ground floods and stitching

5.3.7 Impedance Calculation Tools

The 3D Field Solvers (e.g., those by HP, Ansoft, Sonnet, and Polar) are the most accurate for calculating impedance. Z calculators based on equations (zcalc) are also fairly accurate. The differences are shown in Table 5-2.

Table 5-2. 3D Field Solver vs ZCALC

	#1	#2	#3	#4	#5	#6
H	4.5	4.5	4.2	4.8	4.5	4.5
W	18	18	18	18	17	19
W1	18.1	18.1	18.1	18.1	17.1	19.1
T	1.4	2.8	1.4	1.4	1.4	1.4
Ɛr	4.5	4.5	4.5	4.5	4.5	4.5
Z0(3D)	29.0	28.4	27.6	30.4	30.2	27.9
Z0(zcalc)	29.1	28.7	27.7	30.4	30.2	28.0

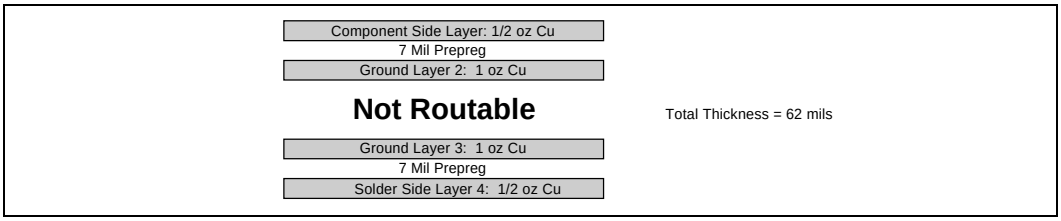
5.3.8 Testing Board Impedance

The *Intel Impedance Test Methodology Document* should be used to ensure boards are within the 28 Ω ±10% requirement. This document can be found at: http://developer.intel.com.

5.3.9 Board Impedance/Stackup Summary

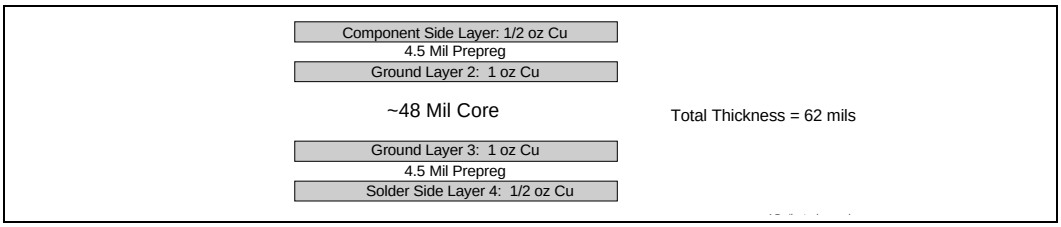
1. ***7628 Cloth, 1 ply 0.007" when cured with 40% resin*** is the most popular and highest volume PCB in production today. This stackup will make routing impossible.
   - Fab Construction (4 Layers)
   - Z_o = 70 Ω ± 15%

Figure 5-3. 7 mil Stackup (Not Routable)



2. ***2116 Cloth, 1 ply 0.0045" when cured with 53% resin*** is the second largest volume in production today. Due to the impedance & layout requirement of traces for Direct RDRAM, AGP 2.0, and hub interface, this stackup is recommended for Intel® 820 chipset platform design.
   - Fab Construction (4 Layers)
   - Z_o = 60 ohms ± 10%

Figure 5-4. 4.5 mil Stackup



This page is intentionally left blank.

6

System Design Considerations

This page is intentionally left blank.

System Design Considerations 6

6.1 Power Delivery

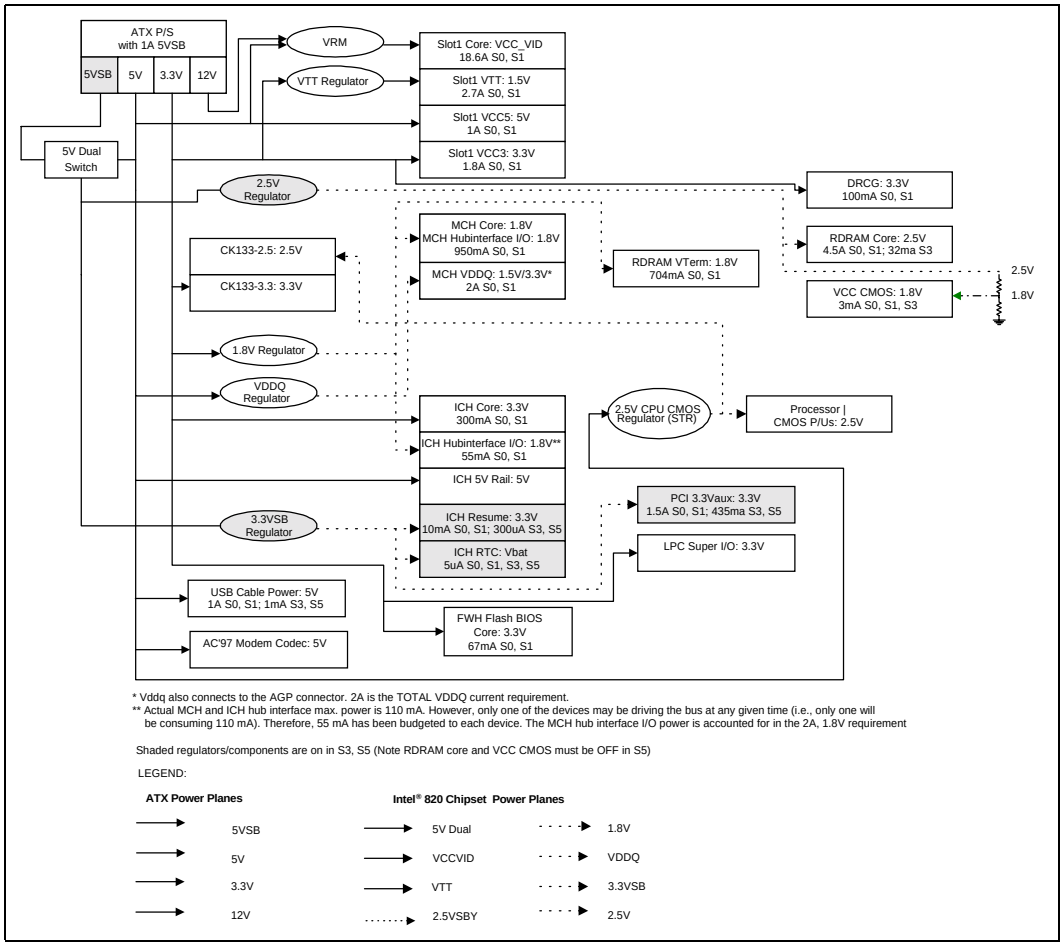
6.1.1 Terminology and Definitions

Term	Definition
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered. This state is used in the Reference Board (refer to Appendix A, "Reference Design Schematics: Uni-Processor" or Appendix B, "Reference Design Schematics: Dual-Processor") to satisfy the S3 ACPI power management state.
Full-power operation	During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state and the S1 (CPU stop-grant state) state.
Suspend operation	During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Power rails	An ATX power supply has 6 power rails: +5V, -5V, +12V, -12V, +3.3V, 5VSB. In addition to these power rails, several other power rails are created with voltage regulators on the Intel® 820 Chipset Reference Board.
Core power rail	A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed *directly* from the ATX power supply are: ±5V, ±12V and +3.3V.
Standby power rail	A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is: 5VSB (5V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail	A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3VSB is usually derived (on the motherboard) from 5VSB using a voltage regulator (on the Intel® 820 Chipset Reference Board, 3.3VSB is derived from 5V_DUAL).
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

6.1.2 Intel® 820 Chipset Customer Reference Board Power Delivery

Figure 6-1 shows the power delivery architecture for the Intel® 820 Chipset Reference Board. This power delivery architecture supports the “Instantly Available PC Design Guidelines” via the suspend-to-RAM (STR) state. During STR, only the necessary devices are powered. These devices include: main memory, the ICH resume well, PCI wake devices (via 3.3V aux) and USB (USB can only be powered if sufficient standby power is available). To ensure that enough power is available during STR, a thorough power budget must be completed. The power requirements must include each device’s power requirements, both in suspend and in full-power. The power requirements must be compared against the power budget supplied by the power supply. Due to the requirements of main memory and PCI 3.3V aux (and possibly other devices in the system), it is necessary to create a dual power rail.

Figure 6-1. Intel® 820 Chipset Power Delivery Example



The examples given in this Design Guide are only examples. There are many power distribution methods that achieve the similar results. It is critical, when deviating from these examples in any way, to consider the effect of the change.

In addition to the power planes provided by the ATX power supply, an *instantly available* Intel® 820 chipset based system (using Suspend-to-RAM*)* requires 7 power planes to be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the Intel® 820 Chipset Reference Board will have a *5V Dual Switch*.

5V Dual Switch

This switch powers the *5V Dual plane* from the 5V core ATX supply during full-power operation. During Suspend-to-RAM, the 5V Dual plane is powered from the 5V Standby power supply.

Note: The voltage on the 5V Dual plane **is not 5V!** There is a resistive drop through the 5V Dual Switch that must be considered. Therefore, NO COMPONENTS should be connected directly to the 5V Dual plane. On the Intel® 820 chipset Reference Board, the only devices connected to the 5V Dual plane are voltage regulators (to regulate to lower voltages).

Note: This switch is not required in a Intel® 820 chipset based system that does not support Suspend-to-RAM (STR).

VCC_{VID}

This power plane is used to power the SC242 processor. Refer to the latest revisions of:

- *VRM 8.4 DC-DC Converter Design Guidelines*
- *Slot 1 Power Delivery Guidelines*

Note: This regulator is required in ALL designs.

V_{TT}

This power plane is used to power the AGTL+ termination resistors. Refer to the latest revisions of:

- *Intel® Pentium® III Processor* Datasheet

Note: This regulator is required in ALL designs.

2.5VSBY

The 2.5VSBY power plane is used to power the RDRAM core and the VCMOS rail on the RDRAMs. The RDRAM core requires approximately 4.5A maximum average DC current at 2.5V (refer to Section 6.1.3, “64/72Mbit RDRAM Excessive Power Consumption” on page 6-5). In the Intel® 820 Chipset Reference Board, the 2.5VSBY plane is derived from the 5V Dual power plane using a switching regulator. It is important, that during the maximum load-step of 2A, the maximum voltage fluctuation is less than 50 mV. The maximum 2.5V tolerance is 125 mV, however during any 10 uS period, the voltage can not fluctuate more than 50 mV. The high-frequency bypassing requirements are met using capacitors on the RIMM itself. Low frequency bypass requirements vary depending on the voltage regulator used. Using a switching regulator, with a relatively slow response time, the low frequency bypass recommendation is: 8 100 uF bulk capacitors (0.1Ω ESR) near the RIMM connectors. These capacitors must be placed near the RIMM connector. Preferably spread the capacitors around where 2.5V connects to the RIMMs.

The VCMOS rail requires a maximum of 3ma at 1.8V. This rail MUST be powered during Suspend-to-RAM and therefore, the VCMOS rail can not be connected to the MCH core power. Because the current requirements of VCMOS are so low, a resistor divider can be used to generate VCMOS from 2.5VSBY. The resistor divider should be 36 Ω (top) / 100 Ω (bottom). Additionally, it should be bypassed with a 0.1 µF chip capacitor.

The Intel® 820 Chipset Reference Board is using a switching regulator from 5V Dual. It may be possible to use a linear regulator to regulate from 3.3VSB, however the thermal characteristics must be considered. Additionally, a low drop out linear regulator would be necessary. If 2.5VSBYis regulated from 3.3VSB, it is important the 3.3VSB regulator can supply enough current for all the 3.3VSB device requirements as well as the 2.5VSBY requirements.

Refer to the 1.8V power plane information for 1.8V and 2.5V power sequencing requirement.

Note: Refer to section Section 6.1.3, “64/72Mbit RDRAM Excessive Power Consumption” on page 6-5 for more details.

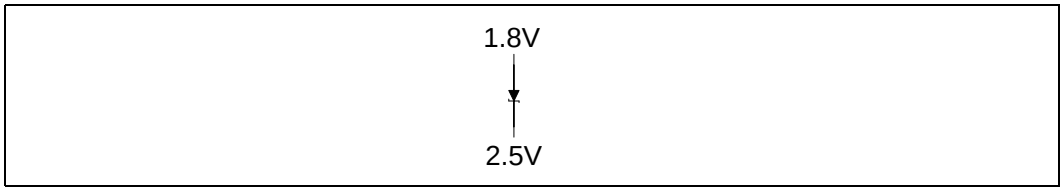
Note: This regulator is required in ALL designs, however in systems that do not support STR, the 2.5V rail would be powered from either the 3.3V or 5V core well.

1.8V

The 1.8V plane powers the MCH core, the ICH hub interface I/O buffers and the RDRAM termination resistors. This power plane has a total power requirement of approximately 1.7A. The 1.8V plane should be decoupled with a 0.1 uF and a 0.01 uF chip capacitor at *each* corner of the MCH and with a single 1 uF and 0.1 uF capacitor at the ICH. Additionally, the 1.8V plane should be decoupled at the RDRAM termination as shown in Section 2.6.2, “Direct Rambus* Layout Guidelines” on page 2-8.

Power MUST NOT be applied to the RDRAM termination resistors (Vterm) prior to applying power to the RDRAM Core (2.5VSBY in this design). This can be guaranteed by placing a Schottky diode between 1.8V and 2.5V as shown in Figure 6-2.

Figure 6-2. 1.8V and 2.5V Power Sequencing (Schottky Diode)



Note: This regulator is required in ALL designs.

VDDQ

The VDDQ plane is used to power the MCH AGP interface and the graphics component AGP interface. Refer to the *AGP Interface Specification Revision 2.0* (http://www.agpforum.org).

Note: This regulator is required in ALL designs (unless the design does not support 1.5V AGP, and therefore does not support 4X AGP).

For the consideration of component long term reliability, the following power sequence is required while the AGP interface of MCH is running at 3.3V. If the AGP interface is running at 1.5V, the following power sequence requirement is no longer applicable. The power sequence requirements are:

1. During the power-up sequence, the 1.8V must ramp up to 1.0V BEFORE 3.3V ramps up to 2.2V
2. During the power-down sequence, the 1.8V CAN NOT ramp below 1.0V BEFORE 3.3V ramps below 2.2V
3. The same power sequence recommendation also applies to the entrance and exit of S3 state, since MCH power is completely off during the S3 state.

System designers need to be aware of this requirement while designing the voltage regulators and selecting the power supply. For further details on the voltage sequencing requirements, refer to the latest *Intel® 820 Chipset: 82820 Memory Controller Hub (MCH)* datasheet.

3.3VSB

The 3.3VSB plane powers the suspend well of the ICH and the PCI 3.3Vaux suspend power pins. The 3.3Vaux requirement state that during suspend, the system must deliver 375mA to each wake-enabled card and 20 mA to each non wake-enabled card. During full-power operation, the system must be able to supply 375 mA to EACH card. Therefore, the total current requirement is:

- Full-power Operation: 375 mA * number of PCI slots
- Suspend Operation: 375+20 * (number of PCI slots – 1)

In addition to the PCI 3.3V aux, the ICH suspend well power requirements must be considered as shown in Figure 6-1.

Note: This regulator is required in ALL designs.

2.5V

The 2.5V plane powers the CPU CMOS pull-up resistors. These pull-up resistors must not be powered when the system is in S3 (because the ICH core is powered down). Therefore, this power plane must be separate from the 2.5VSBY regulator. The total current requirement is approximately 180 mA. This power plane could also be implemented using a FET switch from 2.5VSBY (and controlled by SLP_S3#). If using a FET switch, the resistive drop across the FET switch should be considered.

Note: This regulator is not required in a Intel® 820 chipset based system that does not support Suspend-to-RAM (STR).

6.1.3 64/72Mbit RDRAM Excessive Power Consumption

Some 64/72Mbit RDRAM devices interpret non-broadcast, device-directed commands as broadcast commands. These commands are the SET_FAST_CLOCK, SET_RESET, and CLEAR_RESET commands. RDRAM devices consume more current during these initialization steps than during normal operation. As a result of these devices accepting device directed commands as broadcast commands, the device can not be reset/initialized serially. All devices must be reset/initialize simultaneously. This will result in excessive current draw during the initialization of memory. The amount of excessive current will depend on the number of devices and frequency used. The worst case current draw is 7.5A, in a system with 32 devices and a frequency of 400 MHz. There are two potential solutions:

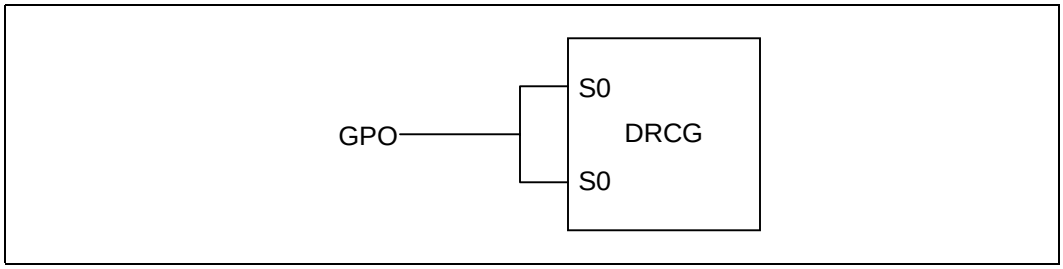
1. Reduce the clock frequency during initialization (Section 6.1.3.1, “Option 1: Reduce the Clock Frequency During Initialization” on page 6-6);
2. Increase the current capability of the 2.5V voltage regulator (Section 6.1.3.2, “Option 2: Increase the Current Capability of the 2.5V Voltage Regulator” on page 6-6).

6.1.3.1 Option 1: Reduce the Clock Frequency During Initialization

Tie a single core well GPO with a default high state to both the S0 and S1 pins of the DRCG (i.e., tie S0 and S1 together and then connect to a GPO as shown in Figure 6-3). When the core power supply to the system is turned on, the DRCG enters a test mode and the output frequency will match the input REFCLK frequency. For details on this DRCG mode, refer to the latest DRCG specification. By slowing down the DRCG output clock, the power consumption from the 2.5V power supply is reduced. After the SetR/ClrR commands have been issued, the BIOS drives the GPO low to bring the DRCG back to normal operation.

Note: If a default low GPO is used, on power up, all the devices may come up in the standby state at full speed; thus, requiring more power.

Figure 6-3. Use a GPO to Reduce DRCG Frequency



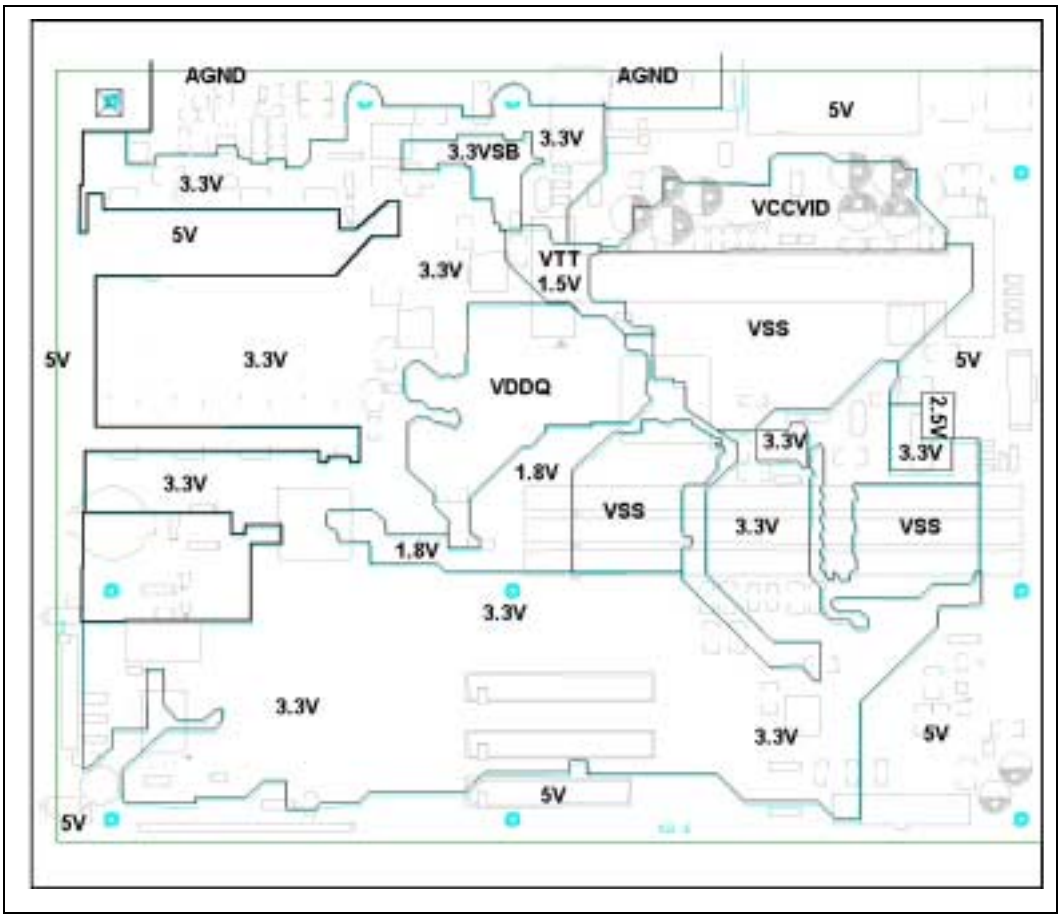
6.1.3.2 Option 2: Increase the Current Capability of the 2.5V Voltage Regulator

The second implementation option requires that the 2.5V power supply be modified to maintain the maximum amount of current required by a fully populated RDRAM channel (~7.5A).

6.2 Power Plane Splits

Figure 6-4 shows an EXAMPLE of the power plane splits on an Intel® 820 chipset platform.

Figure 6-4. Power Plane Split Example



6.3 Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus. Refer to the Intel® 820 Chipset Application Note: *Thermal Design Considerations*, for the thermal measurement methodology.

The thermal design power numbers for the MCH, MTH, and the ICH are listed in Table 6-1.

Table 6-1. Intel® 820 Chipset Component Thermal Design Power

Component	Thermal Design Power (133/400 MHz)
MCH	3.5W ±15%
MTH	2.5W ±15%
ICH	1.3W ±15%

6.4 Glue Chip 3 (Intel® 820 Chipset Glue Chip)

To reduce the component count and BOM cost of the Intel® 820 chipset platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The Glue Chip 3 is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- PWROK signal generation
- Control circuitry for Suspend To RAM
- Power Supply power up circuitry
- RSMRST# generation
- Backfeed cutoff circuit for suspend to RAM
- 5V reference generation
- Flash FLUSH# / INIT# circuit
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- Voltage translation for Audio MIDI signal
- Audio-disable circuit
- Voltage translation for DDC to monitor
- Tri-state buffers for test

More information regarding this component is available from the following vendors:

Table 6-2. Glue Chip 3 Vendors

Vendor Intel	Contact	Contact Information
Fujitsu Microelectronics	Customer Response Center	3545 North 1st Street, M/S 104 San Jose, CA 95134-1804 *fax:* 1-408-922-9179 *email:* fmicrc@fmi.fujitsu.com
Mitel Semiconductor	Mitel Semiconductor	http://www.mitelsemi.com

A

Reference Board Schematics: Uni-Processor

This page is intentionally left blank.

Reference Design Schematics: Uni-Processor A

A.1 Reference Design Feature Set

The reference schematics feature the following core feature set:

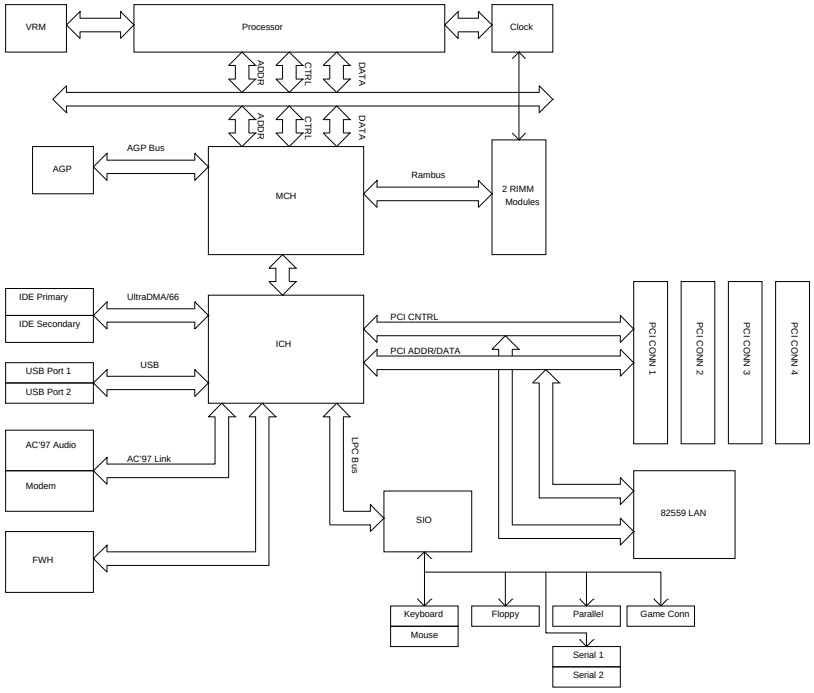
- Intel® 820 Chipset
  - — Memory Controller Hub (MCH)
  - — I/O Controller Hub (ICH)
  - — FWH Flash BIOS Interface
- Support for the Pentium III (SC242) Processor
  - — 100/133 MHz System Bus Frequency
  - — Debug Port
- IOAPIC Integrated into the ICH
- Direct RDRAM Memory Interface
  - — 266 MHz, 300 MHz, 356 MHz and 400 MHz Direct RDRAM Support
- 4 PCI Add-in Slots
  - — Via 4 REQ/GNT pairs (ICH supports 6 REQ#/GNT# pairs)
- AGP Universal Connector
  - — 3.3V - 1X,2X signaling
  - — 1.5V – 1X, 2X, 4X signaling
- 2 IDE Connectors with Ultra ATA/66 Support
- 2 USB Connectors
- ATX Power Connector
- LPC Ultra I/O
  - — Floppy Disk Controller
  - — 1 Parallel Port, 2 Serial Ports
  - — Keyboard Controller
- AC‘97 Bus Connector and Audio Codec
- WfM Support
- Integrated System Management
- Integrated Power Management
  - — ACPI Rev. 1.0 Compliant
  - — APM Rev. 1.2 Compliant
- Pentium III on-board VRM 8.4 compliant regulator
- 4 Layer Design

INTEL(R) 820 CHIPSET
UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS
REV F (2 RIMM)

Note that these schematics are preliminary and are subject to change.

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.01
intel® PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 10:42	SHEET: 1 OF 36

Block Diagram



Device Table

REFERENCE DESIGNATOR	DEVICE TYPE	GATES USED	SHEET NUMBER
U20	74LVC06A	A, B, C	31
U14	74LVC07A	A, B, C	18, 29
U19	74LVC07A	A, C, D	18, 22
U3	74LVC08A	A, B	15, 31
U15	74LVC14a	A, B, C, D	31
U18	74LS132	B, C	29, 31
U13	82820 (ICH)		8, 9
U10	82820 (MCH)		6, 7
U5	82559		16
U8	93C46A		16
U2	AD1881		13
U11	CK133		5
U12	DRCG		5
U16	FWH		10
U4, U6	GD75232		25
U1	LM4880		14
U17	LPC47B27X		12
U9	ADM1021		3
U7	TPS2042		23

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
BLOCK DIAGRAM

REV: 1.01

intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

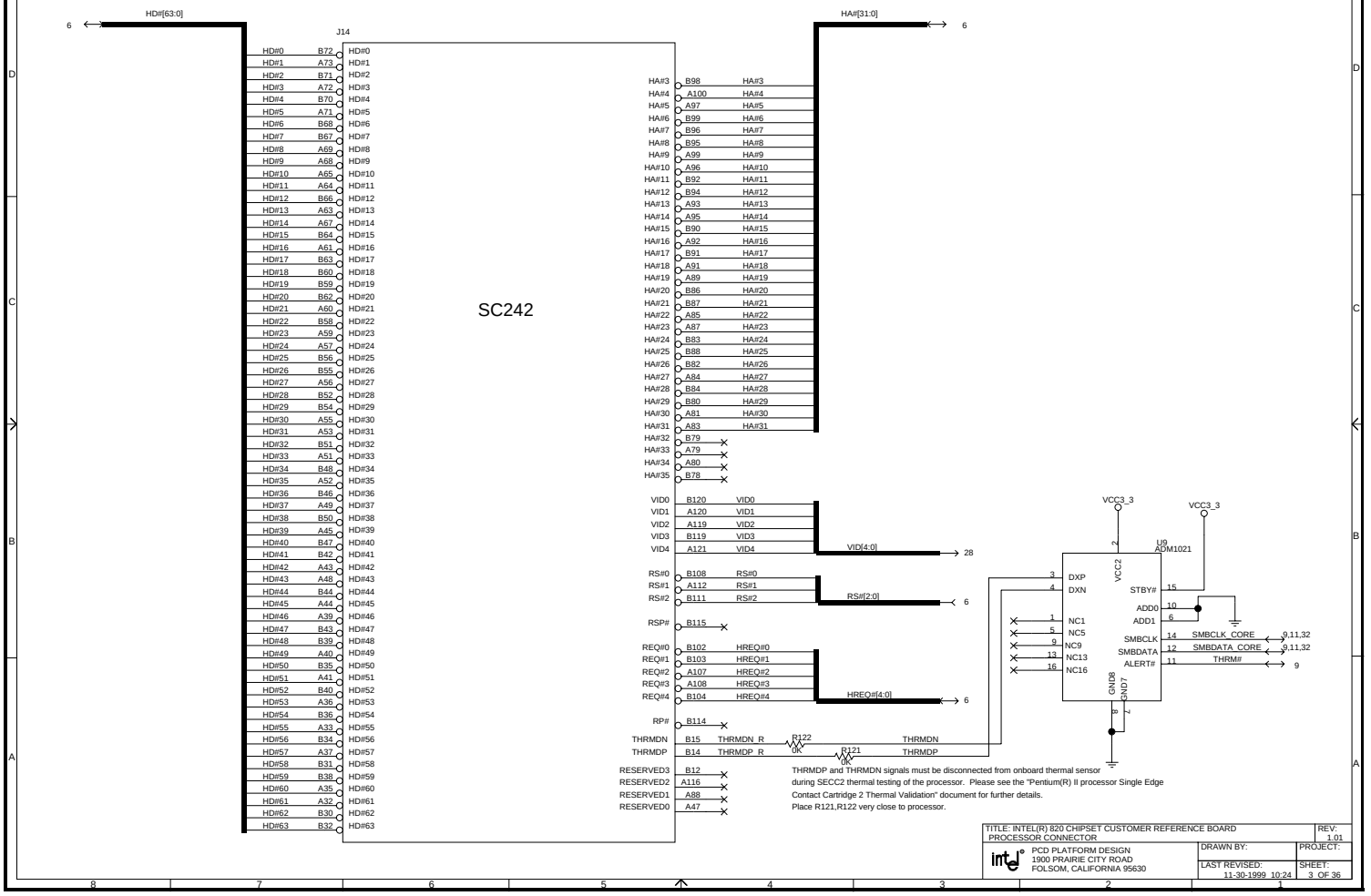
DRAWN BY:

PROJECT:

LAST REVISED: 11-18-1999 10:50

SHEET: 2 OF 36

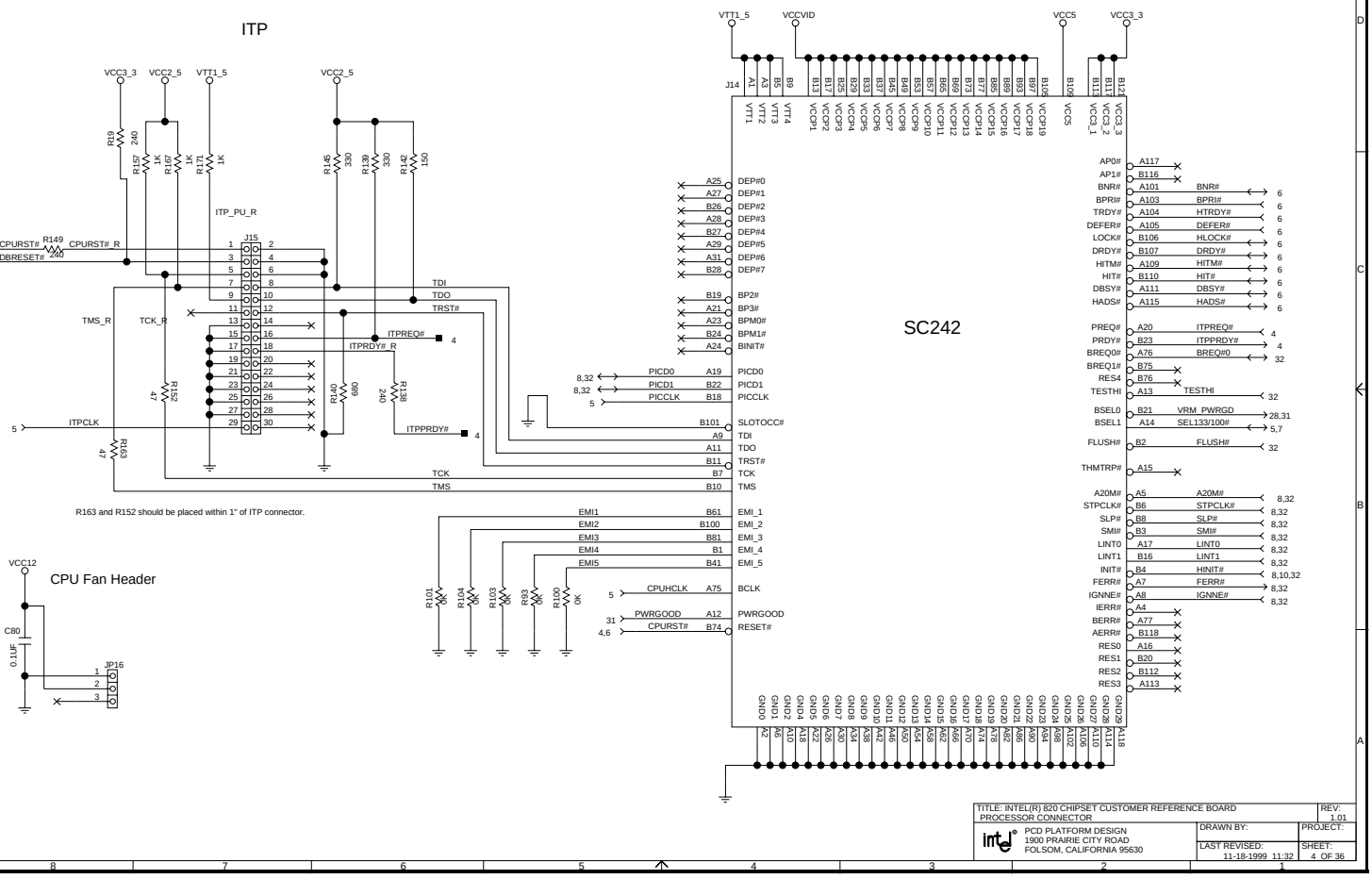
Processor Connector



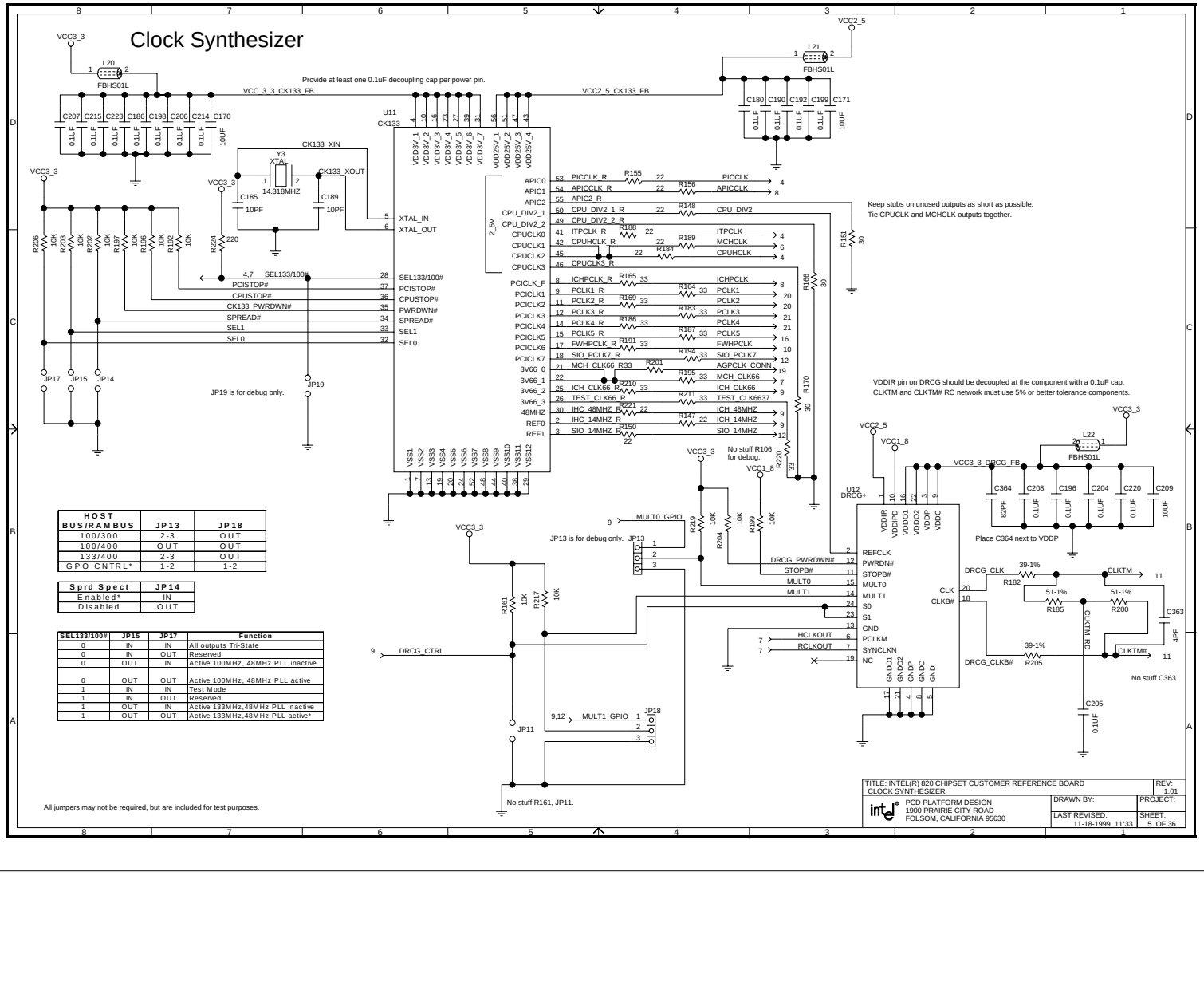
THRMDP and THRMDN signals must be disconnected from onboard thermal sensor during SECC2 thermal testing of the processor. Please see the "Pentium(R) II processor Single Edge Contact Cartridge 2 Thermal Validation" document for further details.
Place R121,R122 very close to processor.

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD PROCESSOR CONNECTOR		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-30-1999 10:24	SHEET: 3 OF 36

Processor Connector



TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD PROCESSOR CONNECTOR		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 11:32	SHEET: 4 OF 36

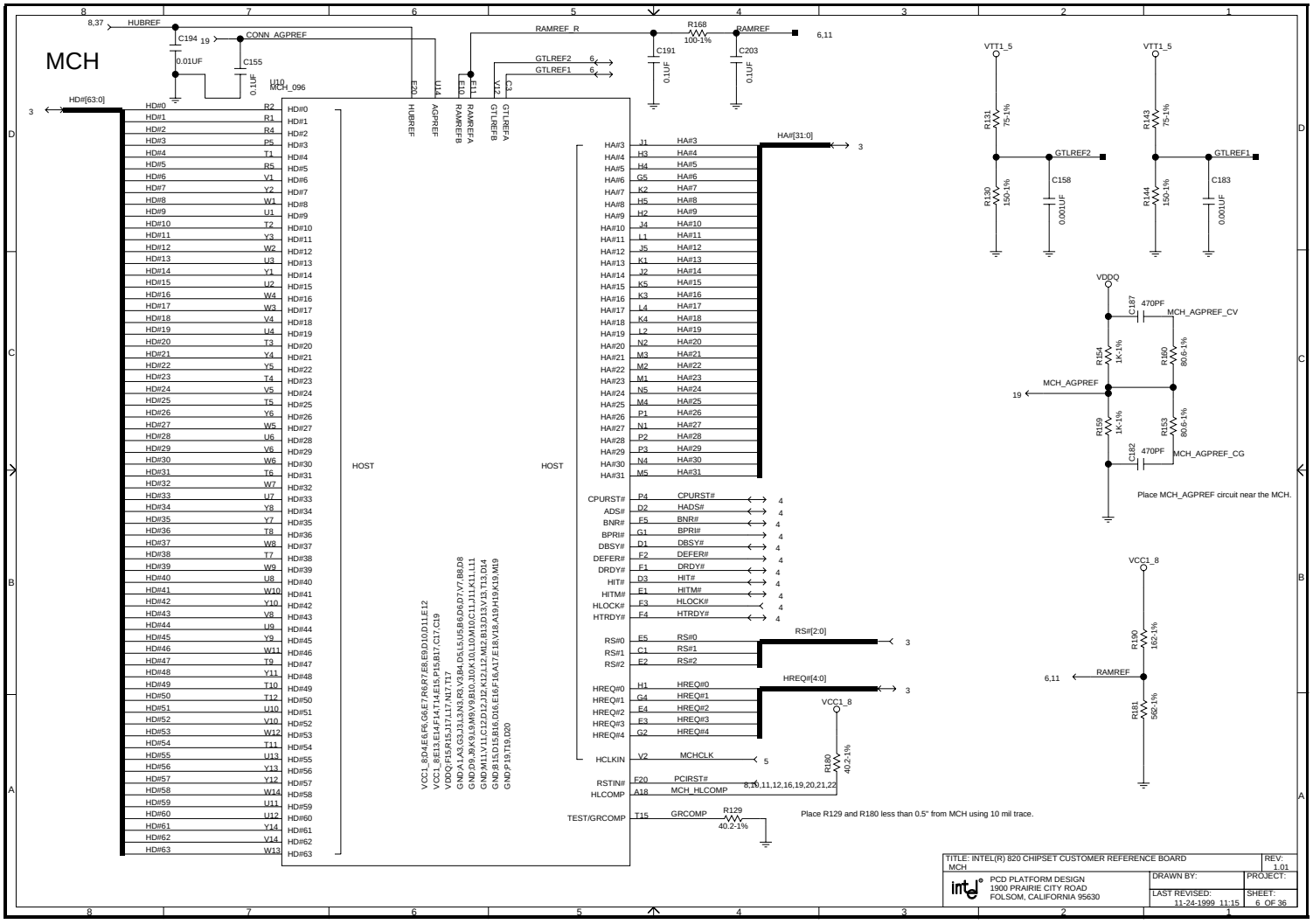


HOST BUS/RAMBUS	JP13	JP18
100/300	2-3	OUT
100/400	OUT	OUT
133/400	2-3	OUT
GPO CNTRL*	1-2	1-2

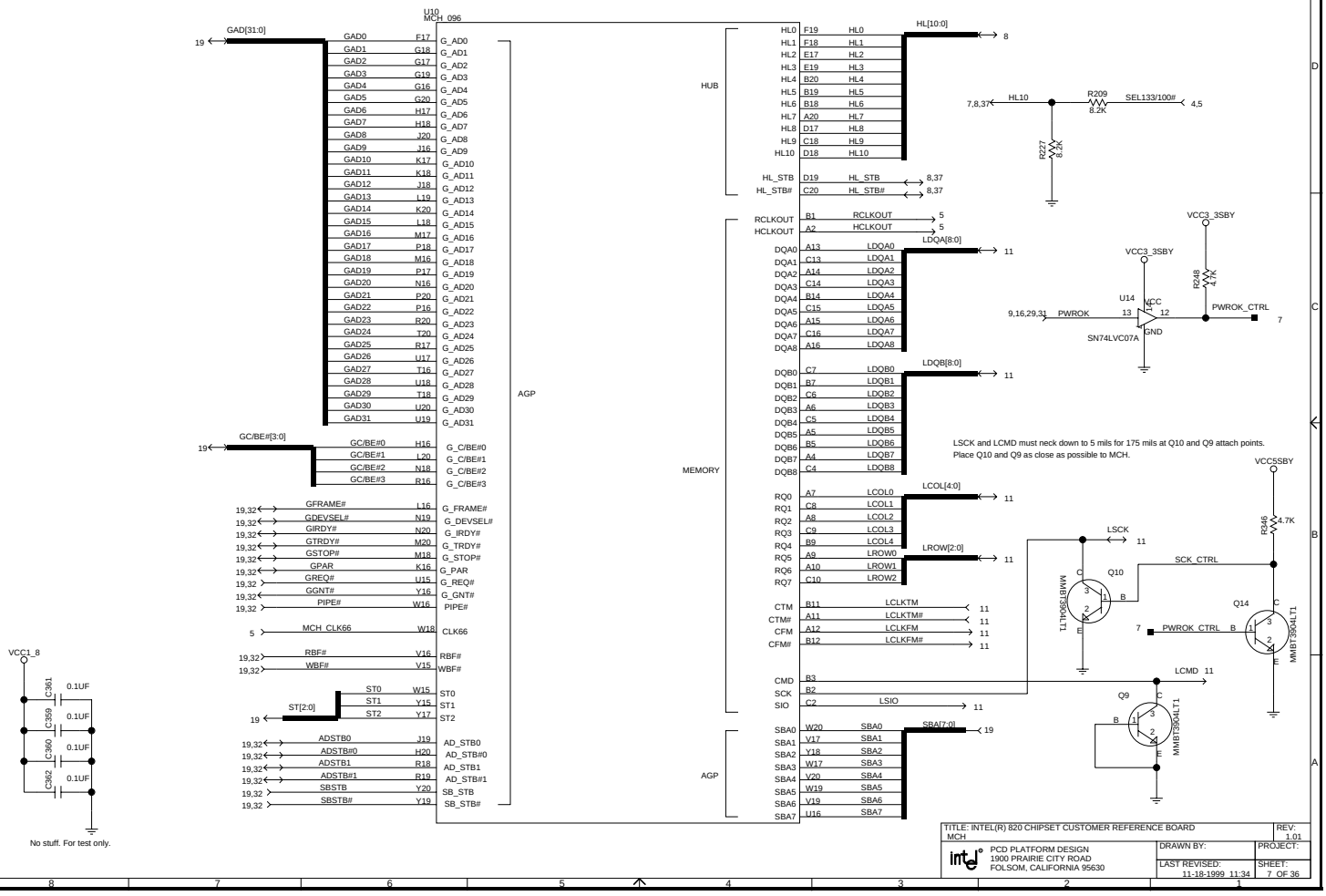
Sprd Spect	JP14
Enabled*	IN
Disabled	OUT

SEL133/100#	JP15	JP17	Function
0	IN	IN	All outputs Tri-State
0	IN	OUT	Reserved
0	OUT	IN	Active 100MHz, 48MHz PLL inactive
0	OUT	OUT	Active 100MHz, 48MHz PLL active
1	IN	IN	Test Mode
1	IN	OUT	Reserved
1	OUT	IN	Active 133MHz,48MHz PLL inactive
1	OUT	OUT	Active 133MHz,48MHz PLL active*

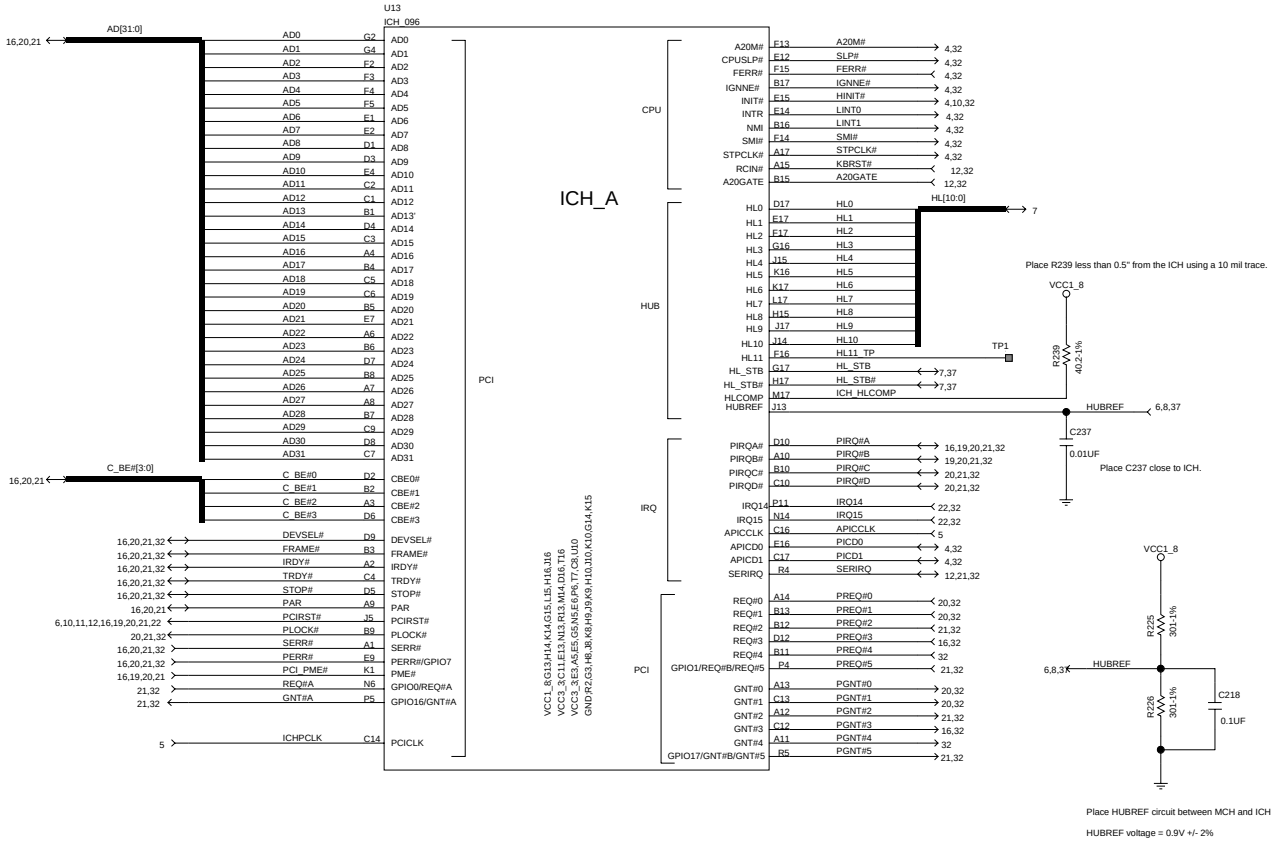
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD CLOCK SYNTHESIZER	REV: 1.01
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: / PROJECT:
LAST REVISED: 11-18-1999 11:33	SHEET: 5 OF 36


MCH
8,37 HUBREF
C194 0.01UF
19 CONN_AGPREF
C155 0.1UF
U10 MCH_096
HD#[63:0]
3
HD#0 R2
HD#1 R1
HD#2 R4
HD#3 P5
HD#4 T1
HD#5 R5
HD#6 V1
HD#7 Y2
HD#8 W1
HD#9 U1
HD#10 T2
HD#11 Y3
HD#12 W2
HD#13 U3
HD#14 Y1
HD#15 U2
HD#16 W4
HD#17 W3
HD#18 V4
HD#19 U4
HD#20 T3
HD#21 Y4
HD#22 Y5
HD#23 T4
HD#24 V5
HD#25 T5
HD#26 Y6
HD#27 W5
HD#28 U6
HD#29 V6
HD#30 W6
HD#31 T6
HD#32 W7
HD#33 U7
HD#34 Y8
HD#35 Y7
HD#36 T8
HD#37 W8
HD#38 T7
HD#39 W9
HD#40 U8
HD#41 W10
HD#42 Y10
HD#43 V8
HD#44 U9
HD#45 Y9
HD#46 W11
HD#47 T9
HD#48 Y11
HD#49 T10
HD#50 T12
HD#51 U10
HD#52 V10
HD#53 W12
HD#54 T11
HD#55 U13
HD#56 Y13
HD#57 Y12
HD#58 W14
HD#59 U11
HD#60 U12
HD#61 Y14
HD#62 V14
HD#63 W13
HOST
HHREF C20
HVREF U14
RAMREF_R
R168 100-1%
RAMREF 6,11
C191 0.1UF
C203 0.1UF
GTLREF2 6
GTLREF1 6
RAMREFB E10
RAMREFA E11
GTLREFB V12
GTLREFA C3
VCC1_8:A5,E6,F6,G6,E7,R6,R7,E8,E9,D10,D11,E12
VCC1_8:E13,E14,F14,T14,E15,F15,B17,C17,G19
VDDQ:P15,R15,J17,L17,N17,T17
GND:A1,A3,G3,J13,N3,R3,V3,B4,D5,L5,U5,B6,D6,D7,V7,B8,D8
GND:D9,J9,K9,L9,M9,V9,B10,J10,K10,M10,C11,J11,K11,L11
GND:M11,V11,B12,D12,J12,K12,M12,B13,J13,V13,T13,D14
GND:J14,L14,T14,D15,E15,D16,E16,F16,A17,E18,V18,A19,H19,K19,M19
GND:P19,T19,D20
HA#[31:0] 3
HA#3 J1
HA#4 H3
HA#5 H4
HA#6 G5
HA#7 K2
HA#8 H5
HA#9 H2
HA#10 J4
HA#11 L1
HA#12 J5
HA#13 K1
HA#14 J2
HA#15 K5
HA#16 K3
HA#17 L4
HA#18 K4
HA#19 L2
HA#20 N2
HA#21 M3
HA#22 M2
HA#23 M1
HA#24 N5
HA#25 M4
HA#26 P1
HA#27 N1
HA#28 P2
HA#29 P3
HA#30 N4
HA#31 M5
CPURST# P4 4
ADS# D2 4
BNR# F5 4
BPRI# G1 4
DBSY# D1 4
DEFER# F2 4
DRDY# F1 4
HIT# D3 4
HITM# E1 4
HLOCK# F3 4
HTRDY# F4 4
RS#[2:0] 3
RS#0 E5
RS#1 C1
RS#2 E2
HREQ#[4:0] 3
HREQ#0 H1
HREQ#1 G4
HREQ#2 E4
HREQ#3 E3
HREQ#4 G2
HCLKIN V2 MCHCLK 5
RSTIN# F20 PCIRST# 8,10,11,12,16,19,20,21,22
HLCOMP A18 MCH_HLCOMP
TEST/GRCOMP T15 GRCOMP R129 40.2-1%
Place R129 and R180 less than 0.5" from MCH using 10 mil trace.
VTT1_5
R131 75-1%
R120 150-1%
C158 0.001UF
GTLREF2
R143 75-1%
R144 150-1%
C183 0.001UF
GTLREF1
VDDQ
C187 470PF
MCH_AGPREF_CV
R154 1K-1%
R160 80.6-1%
MCH_AGPREF
19
R159 1K-1%
R153 80.6-1%
C182 470PF
MCH_AGPREF_CG
Place MCH_AGPREF circuit near the MCH.
VCC1_8
R190 162-1%
6,11 RAMREF
R181 562-1%
R180 40.2-1%
VCC1_8
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
MCH
REV: 1.01
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-24-1999 11:15
SHEET: 6 OF 36

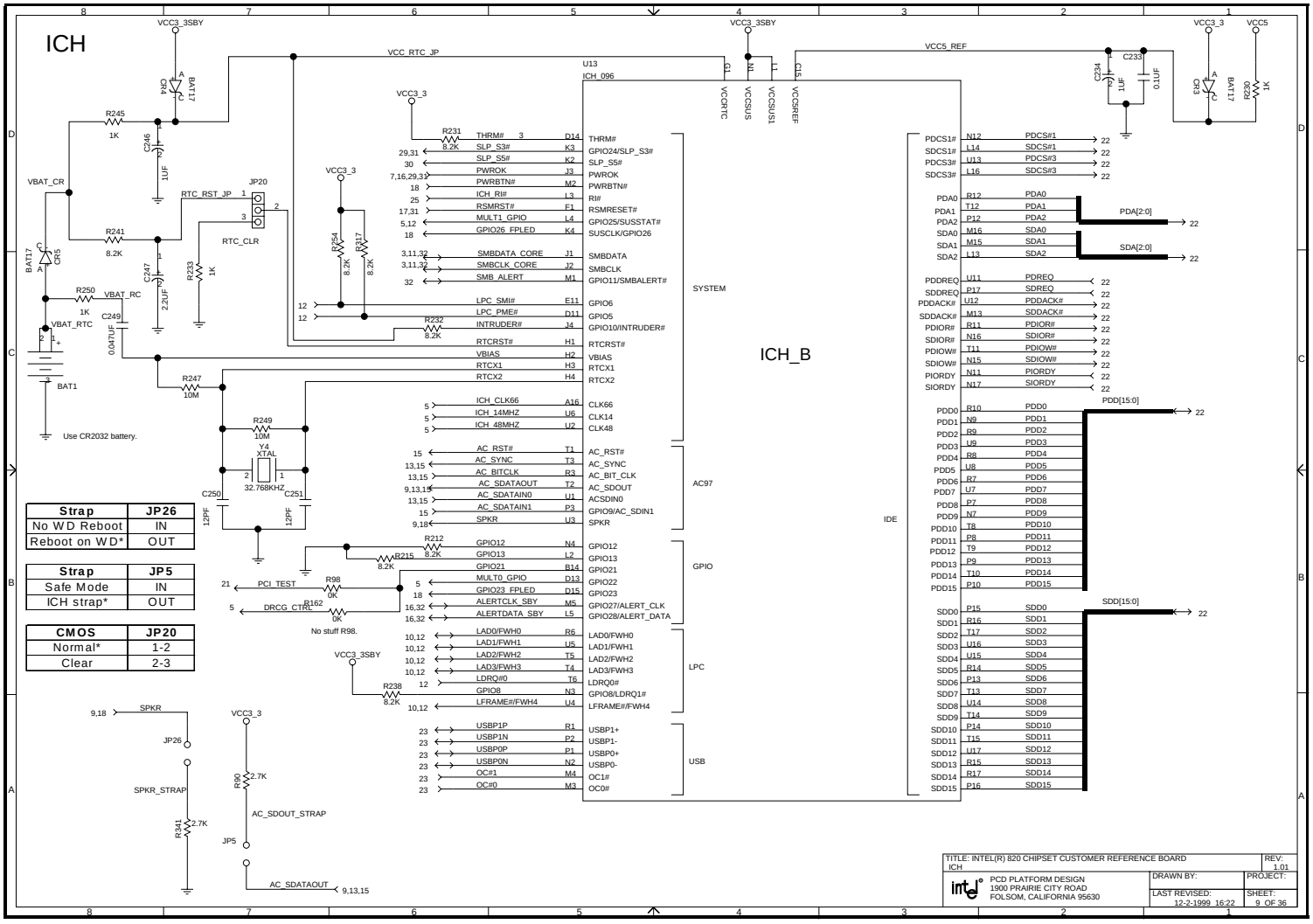
MCH


U10
MCH_096
GAD[31:0]
GC/BE#[3:0]
HUB
AGP
MEMORY
HL[10:0]
LDQA[8:0]
LDQB[8:0]
LCOL[4:0]
LROW[2:0]
SBA[7:0]
LSCK and LCMD must neck down to 5 mils for 175 mils at Q10 and Q9 attach points.
Place Q10 and Q9 as close as possible to MCH.
SN74LVC07A
MMBT3904LT1
No stuff. For test only.
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
MCH
REV: 1.01
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-18-1999 11:34
SHEET: 7 OF 36

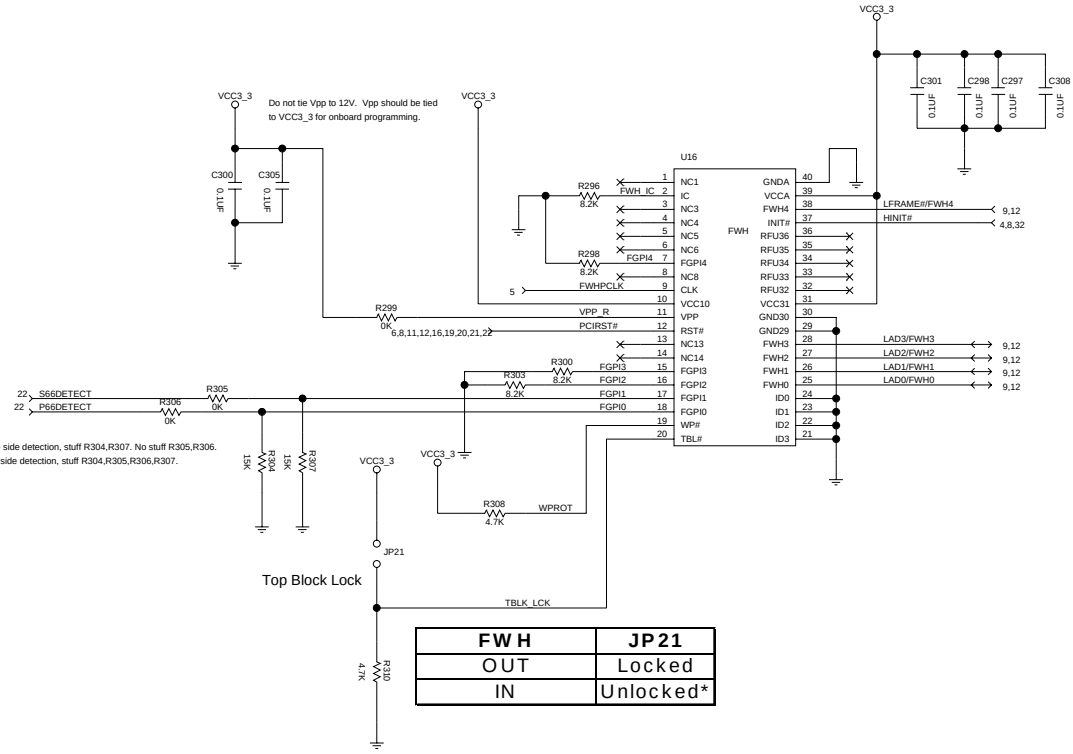
ICH



TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD ICH	REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PROJECT:
LAST REVISED: 11-24-1999 11:14	SHEET: 8 OF 36


ICH
ICH_B
VCC3_3SBY
VCC_RTC_JP
VCC5_REF
VCC3_3
VCC5
U13
ICH_096
BAT17
R245
1K
C246
1UF
VBAT_CR
RTC_RST_JP
JP20
RTC_CLR
R241
8.2K
C247
2.2UF
R233
1K
R250
1K
VBAT_RC
C249
0.047UF
VBAT_RTC
BAT1
Use CR2032 battery.
R247
10M
R249
10M
Y4
XTAL
32.768KHZ
C250
12PF
C251
12PF
C234
1UF
C233
0.1UF
R230
1K
R231
8.2K
R254
8.2K
R317
8.2K
R232
8.2K
THRM#
SLP_S3#
SLP_S5#
PWROK
PWRBTN#
ICH_RI#
RSMRST#
MULT1_GPIO
GPIO26_FPLED
SMBDATA_CORE
SMBCLK_CORE
SMB_ALERT
LPC_SMI#
LPC_PME#
INTRUDER#
RTCRST#
VBIAS
RTCX1
RTCX2
ICH_CLK66
ICH_14MHZ
ICH_48MHZ
AC_RST#
AC_SYNC
AC_BIT_CLK
AC_SDATAOUT
AC_SDATAIN0
AC_SDATAIN1
SPKR
GPIO12
GPIO13
GPIO21
MULT0_GPIO
GPIO23_FPLED
ALERTCLK_SBY
ALERTDATA_SBY
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
LDRQ#0
GPIO8
LFRAME#/FWH4
USBP1P
USBP1N
USBP0P
USBP0N
OC#1
OC#0
SYSTEM
AC97
GPIO
LPC
USB
IDE
PDCS1#
SDCS1#
PDCS3#
SDCS3#
PDA0
PDA1
PDA2
SDA0
SDA1
SDA2
PDA[2:0]
SDA[2:0]
PDDREQ
SDDREQ
PDDACK#
SDDACK#
PDIOR#
SDIOR#
PDIOW#
SDIOW#
PIORDY
SIORDY
PDD[15:0]
SDD[15:0]
Strap | JP26
No WD Reboot | IN
Reboot on WD* | OUT
Strap | JP5
Safe Mode | IN
ICH strap* | OUT
CMOS | JP20
Normal* | 1-2
Clear | 2-3
PCI_TEST
DRCG_CTRL
R98
0K
R162
0K
No stuff R98.
SPKR
JP26
SPKR_STRAP
R90
2.7K
R341
2.7K
AC_SDOUT_STRAP
JP5
AC_SDATAOUT
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
ICH
REV: 1.01
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 12-2-1999 16:22
SHEET: 9 OF 36

FWH



FWH	JP21
OUT	Locked
IN	Unlocked*

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
FWH

REV: 1.01

PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY:

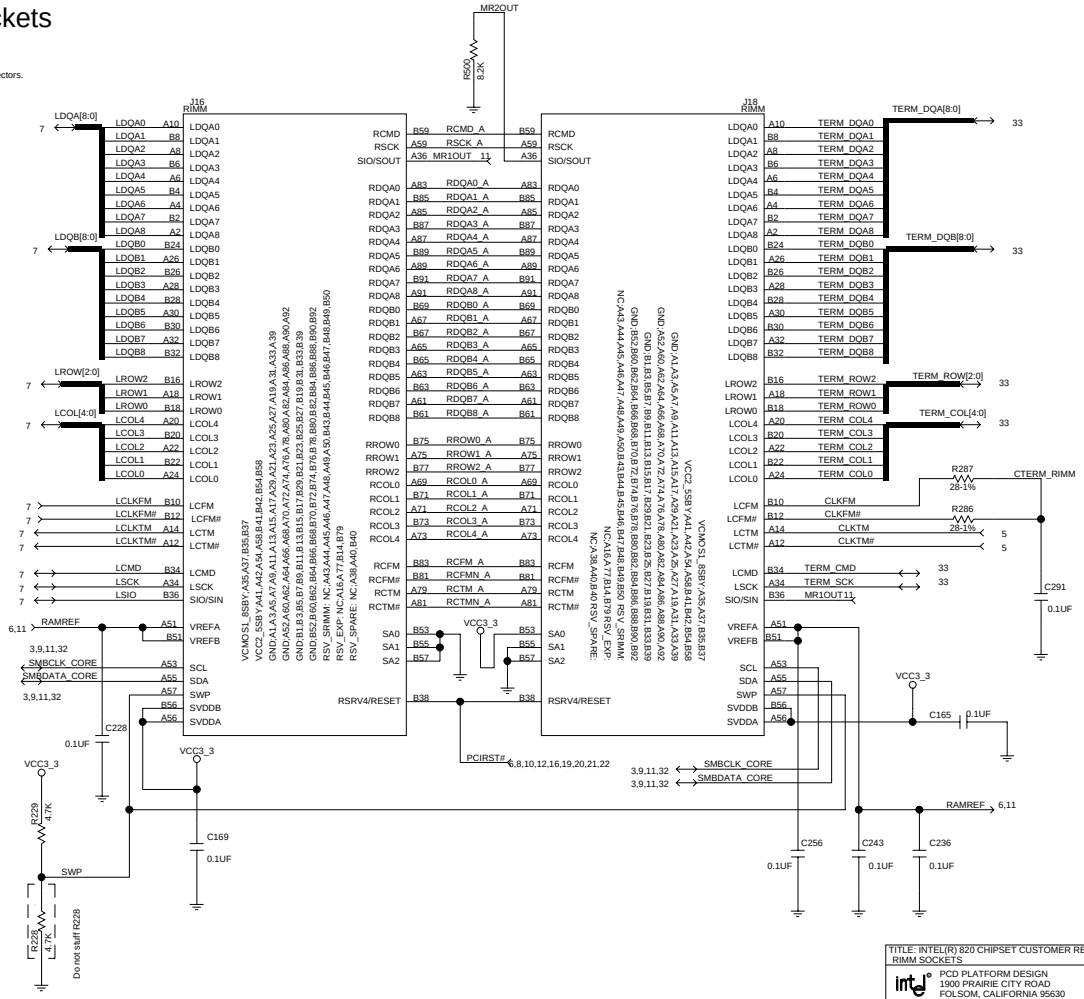
PROJECT:

LAST REVISED: 11-18-1999 10:44

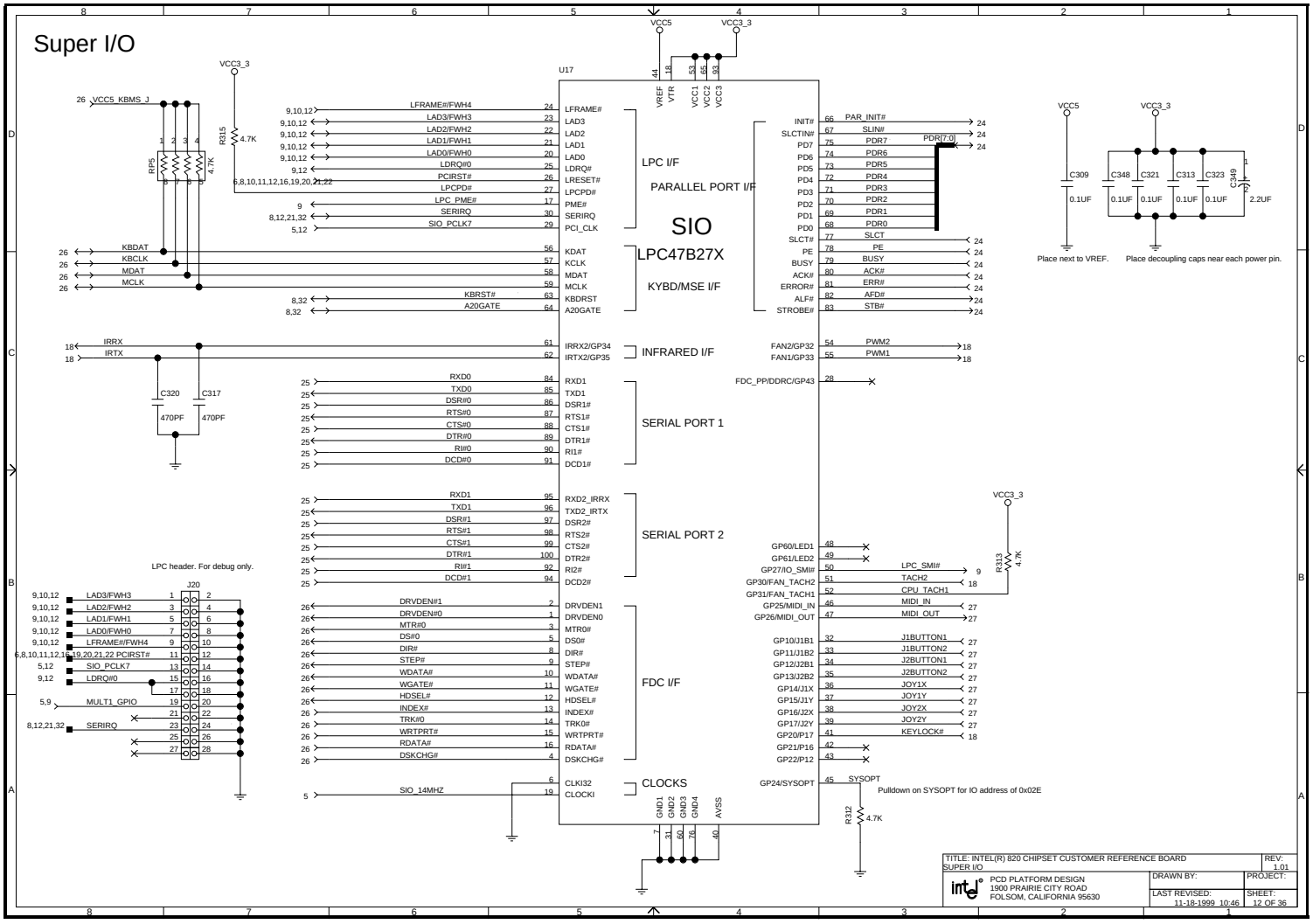
SHEET: 10 OF 36

2 RIMM Sockets

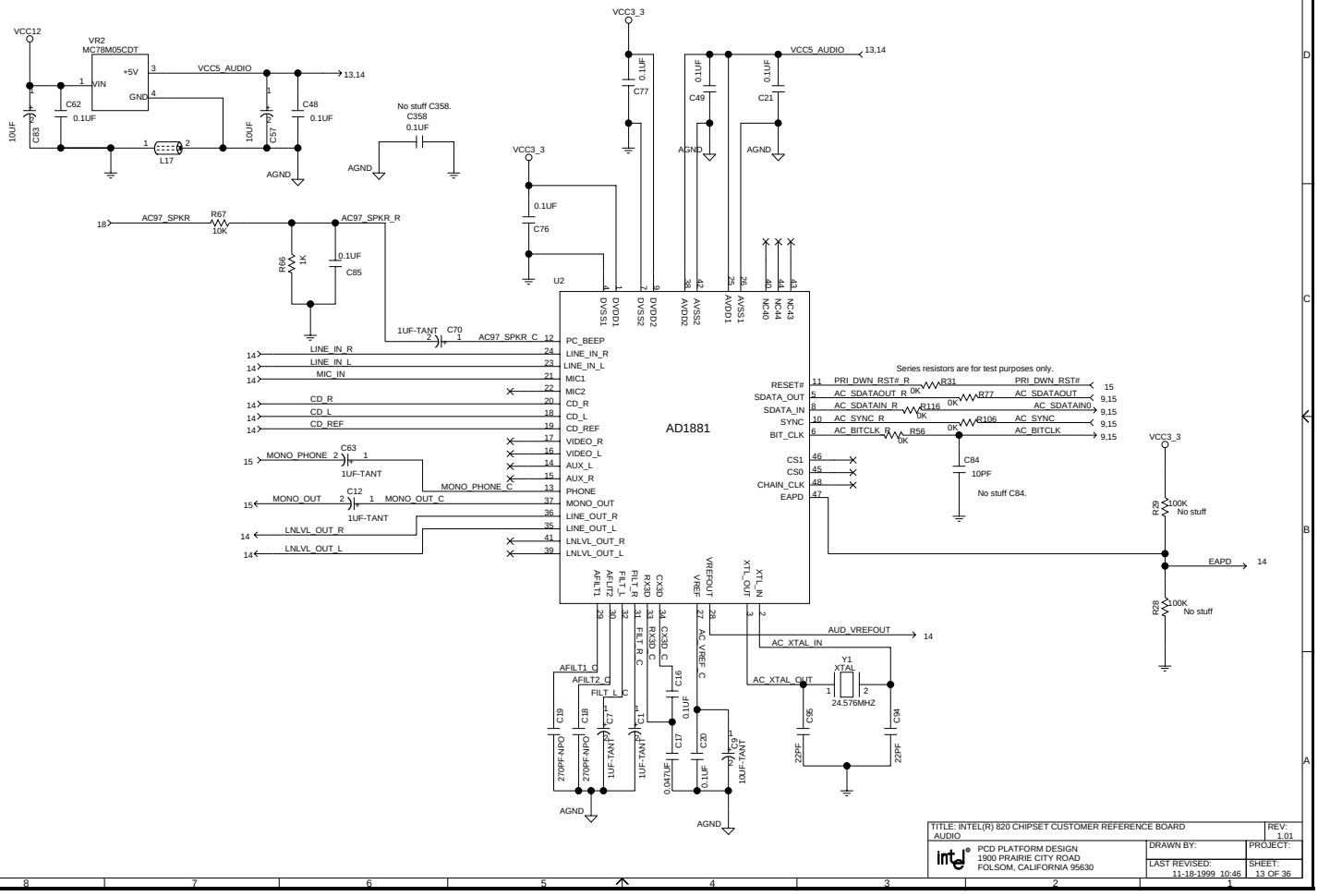
As shown, RIMMs are 184-pin connectors.



TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD RIMM SOCKETS	REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PROJECT:
	LAST REVISED: 11-24-1999 13:14 SHEET: 11 OF 36

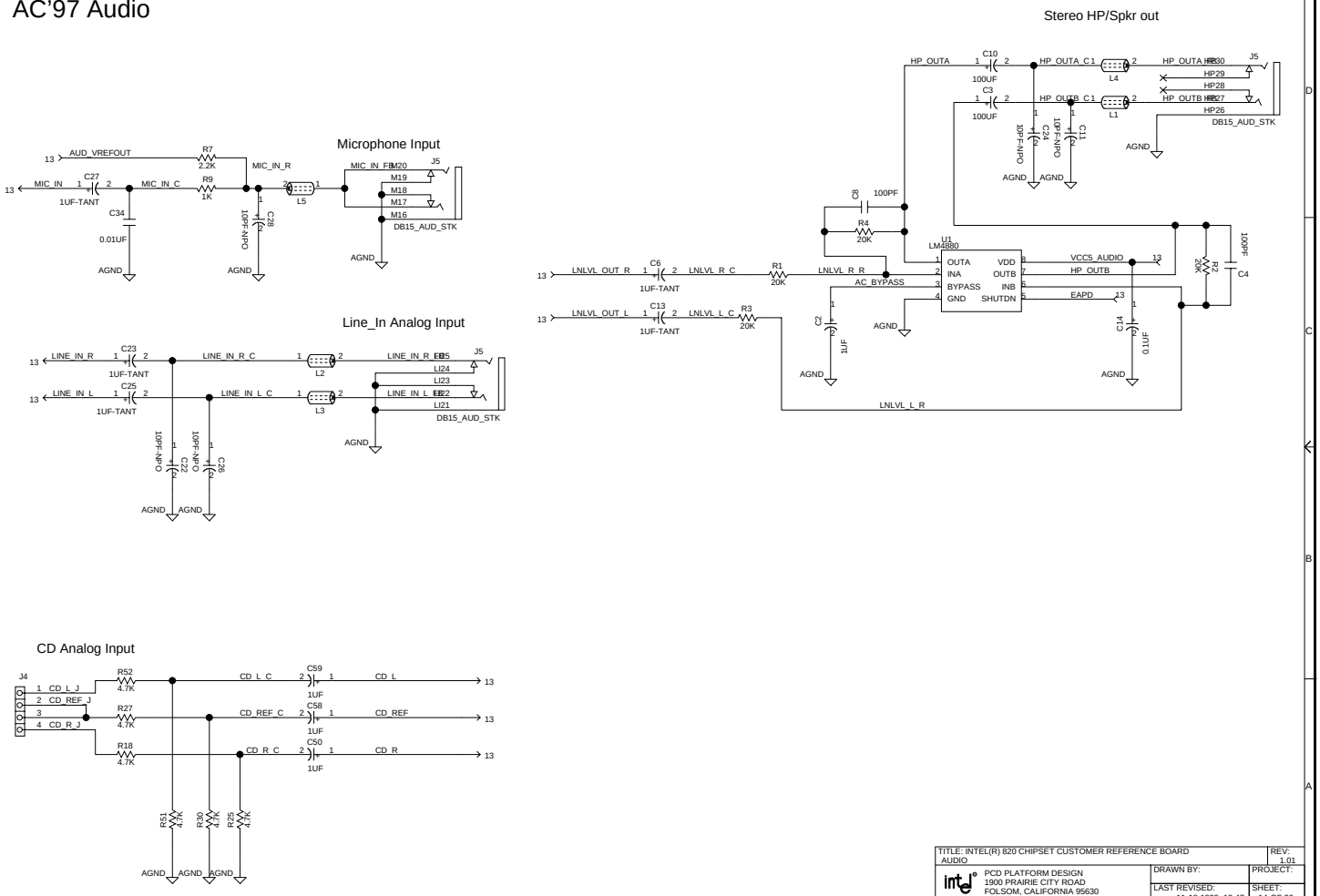

Super I/O
U17
SIO
LPC47B27X
LPC I/F
PARALLEL PORT I/F
KYBD/MSE I/F
INFRARED I/F
SERIAL PORT 1
SERIAL PORT 2
FDC I/F
CLOCKS
LFRAME#/FWH4
LAD3/FWH3
LAD2/FWH2
LAD1/FWH1
LAD0/FWH0
LDRQ#0
PCIRST#
LPCPD#
LPC_PME#
SERIRQ
SIO_PCLK7
KBDAT
KBCLK
MDAT
MCLK
KBRST#
A20GATE
IRRX
IRTX
RXD0
TXD0
DSR#0
RTS#0
CTS#0
DTR#0
RI#0
DCD#0
RXD1
TXD1
DSR#1
RTS#1
CTS#1
DTR#1
RI#1
DCD#1
DRVDEN#1
DRVDEN#0
MTR#0
DS#0
DIR#
STEP#
WDATA#
WGATE#
HDSEL#
INDEX#
TRK0#
WRTPRT#
RDATA#
DSKCHG#
SIO_14MHZ
PAR_INIT#
SLIN#
PDR[7:0]
SLCT#
PE
BUSY
ACK#
ERROR#
ALF#
STROBE#
PDR7
PDR6
PDR5
PDR4
PDR3
PDR2
PDR1
PDR0
FAN2/GP32
FAN1/GP33
PWM2
PWM1
FDC_PP/DDRC/GP43
GP60/LED1
GP61/LED2
GP27/IO_SMI#
GP30/FAN_TACH2
GP31/FAN_TACH1
GP25/MIDI_IN
GP26/MIDI_OUT
GP10/J1B1
GP11/J1B2
GP12/J2B1
GP13/J2B2
GP14/J1X
GP15/J1Y
GP16/J2X
GP17/J2Y
GP20/P17
GP21/P16
GP22/P12
GP24/SYSOPT
LPC_SMI#
TACH2
CPU_TACH1
MIDI_IN
MIDI_OUT
J1BUTTON1
J1BUTTON2
J2BUTTON1
J2BUTTON2
JOY1X
JOY1Y
JOY2X
JOY2Y
KEYLOCK#
SYSOPT
Pulldown on SYSOPT for IO address of 0x02E
LPC header. For debug only.
J20
MULT1_GPIO
SERIRQ
VCC5_KBMS_J
VCC5
VCC3_3
R315
4.7K
RP5
C320
C317
470PF
C309
C348
C321
C313
C323
C349
0.1UF
2.2UF
Place next to VREF.
Place decoupling caps near each power pin.
R313
R312
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
SUPER I/O
REV: 1.01
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-18-1999 10:46
SHEET: 12 OF 36

AC’97 Audio



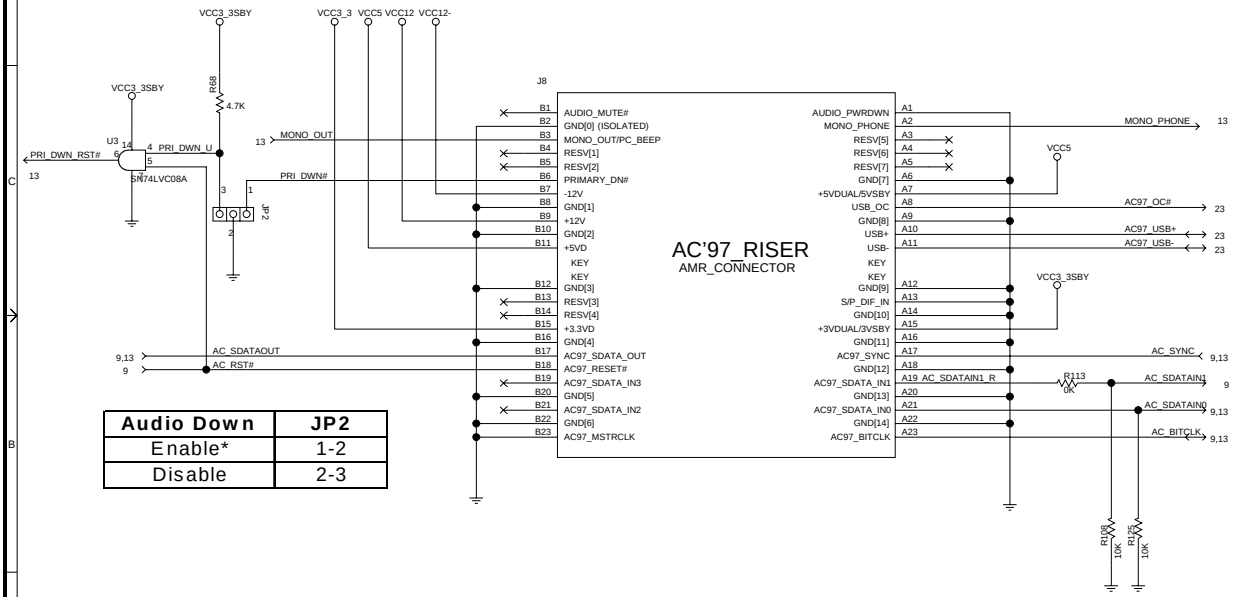
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD AUDIO		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 10:46	SHEET: 13 OF 36

AC'97 Audio



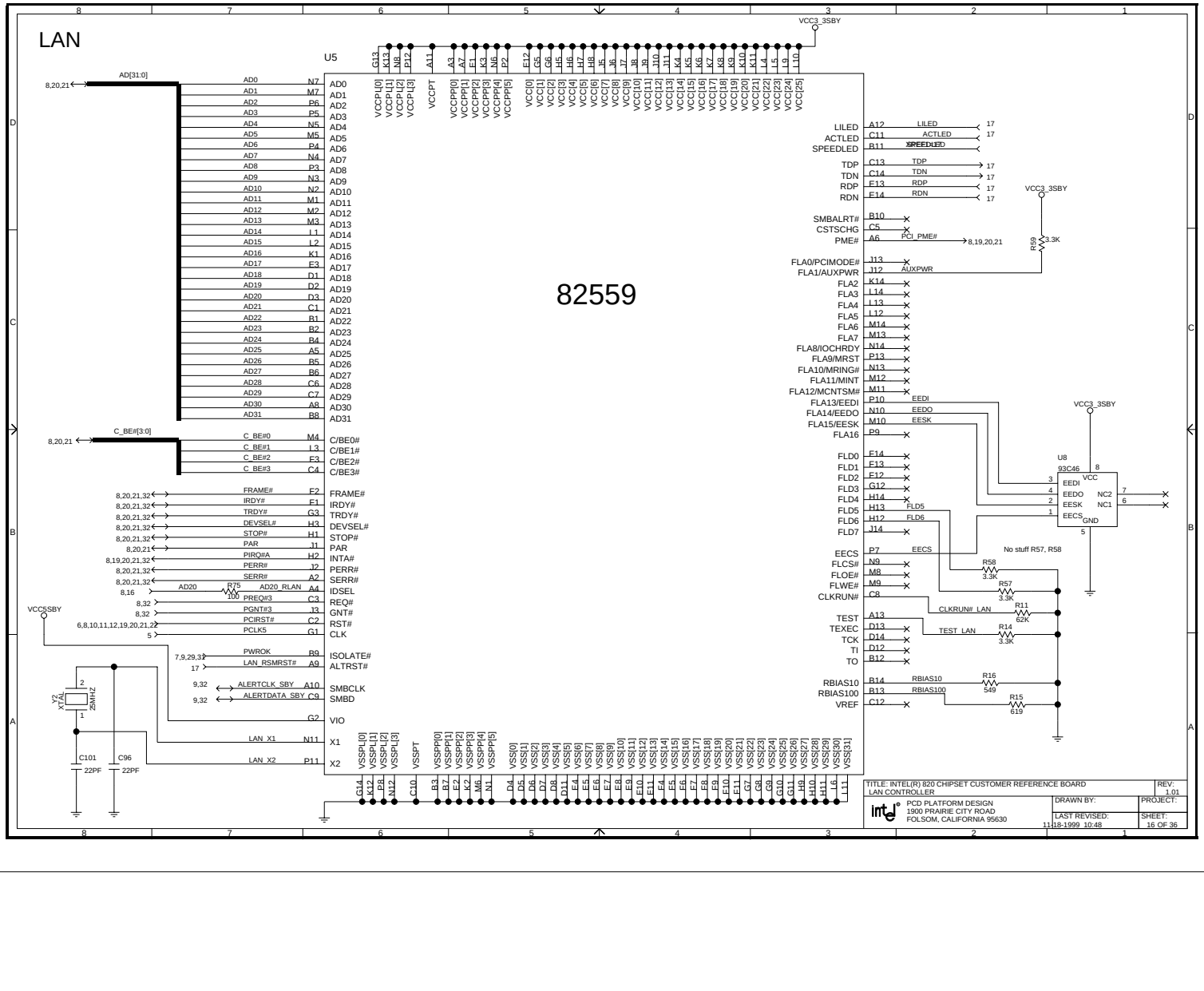
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD AUDIO		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 10:47	SHEET: 14 OF 36

AC’97 Audio/Modem Riser

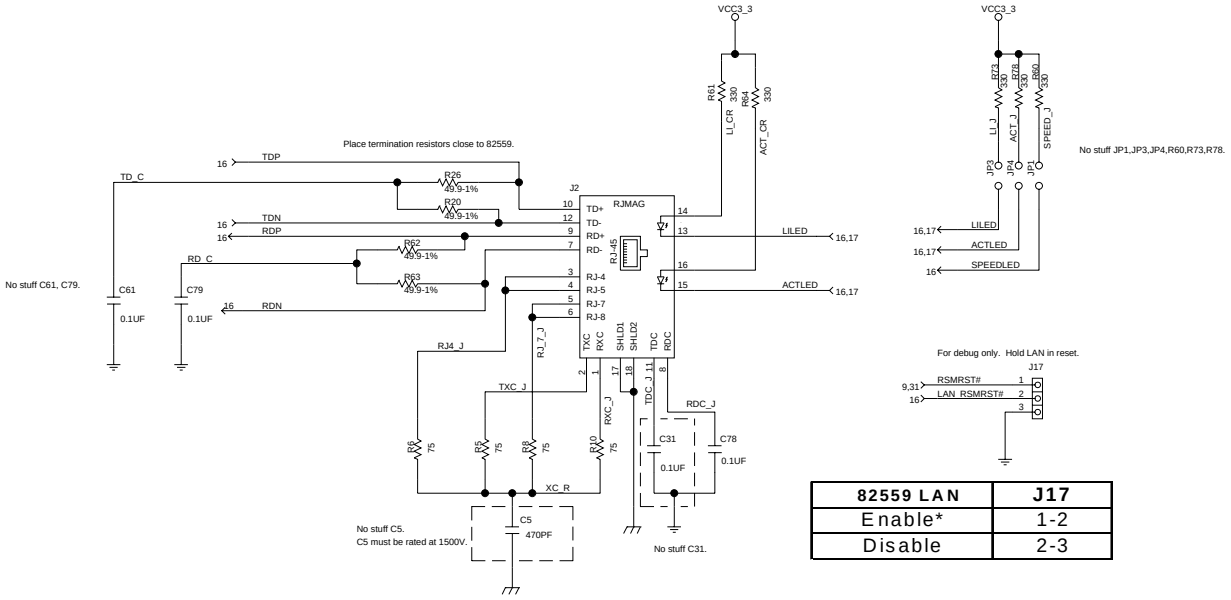


Audio Down	JP2
Enable*	1-2
Disable	2-3

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD AUDIO/MODEM RISER		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED:	SHEET: 15 OF 36


LAN
U5
82559
VCC3_3SBY
AD[31:0]
C_BE#[3:0]
VCC5SBY
U8
93C46
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
LAN CONTROLLER
REV: 1.01
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-18-1999 10:48
SHEET: 16 OF 36

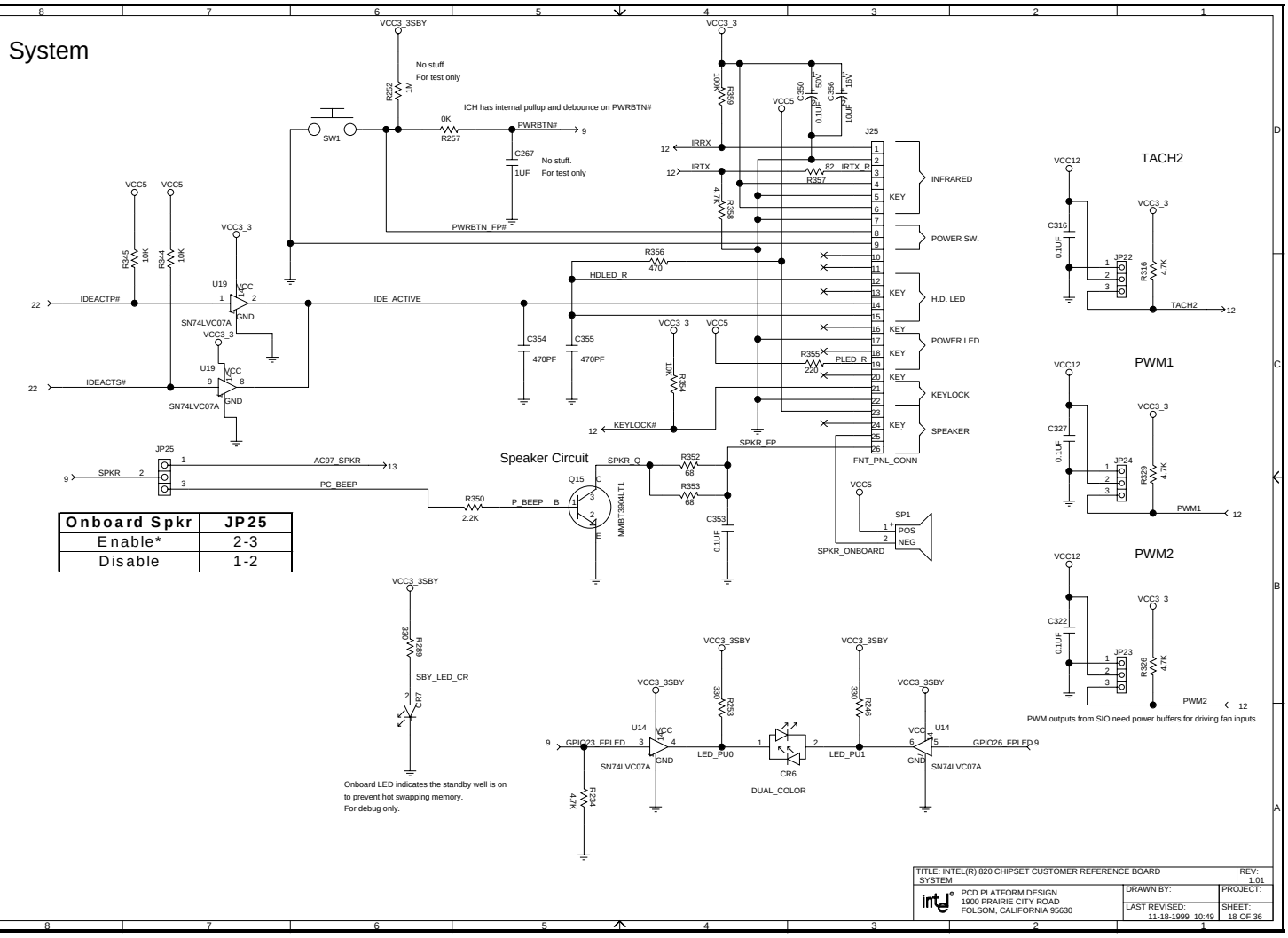
LAN



82559 LAN	J17
Enable*	1-2
Disable	2-3

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD LAN		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 10:48	SHEET: 17 OF 36

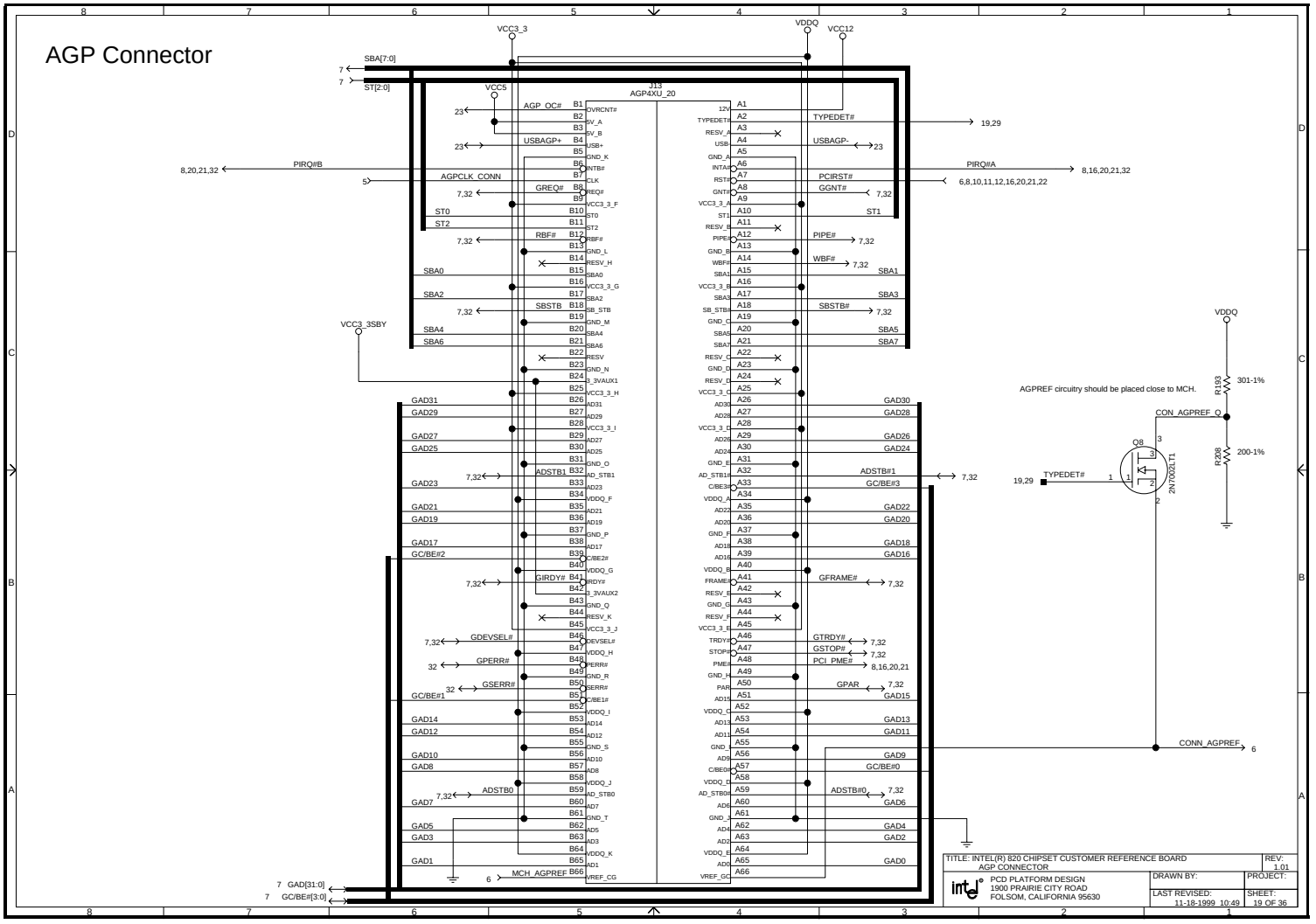
System



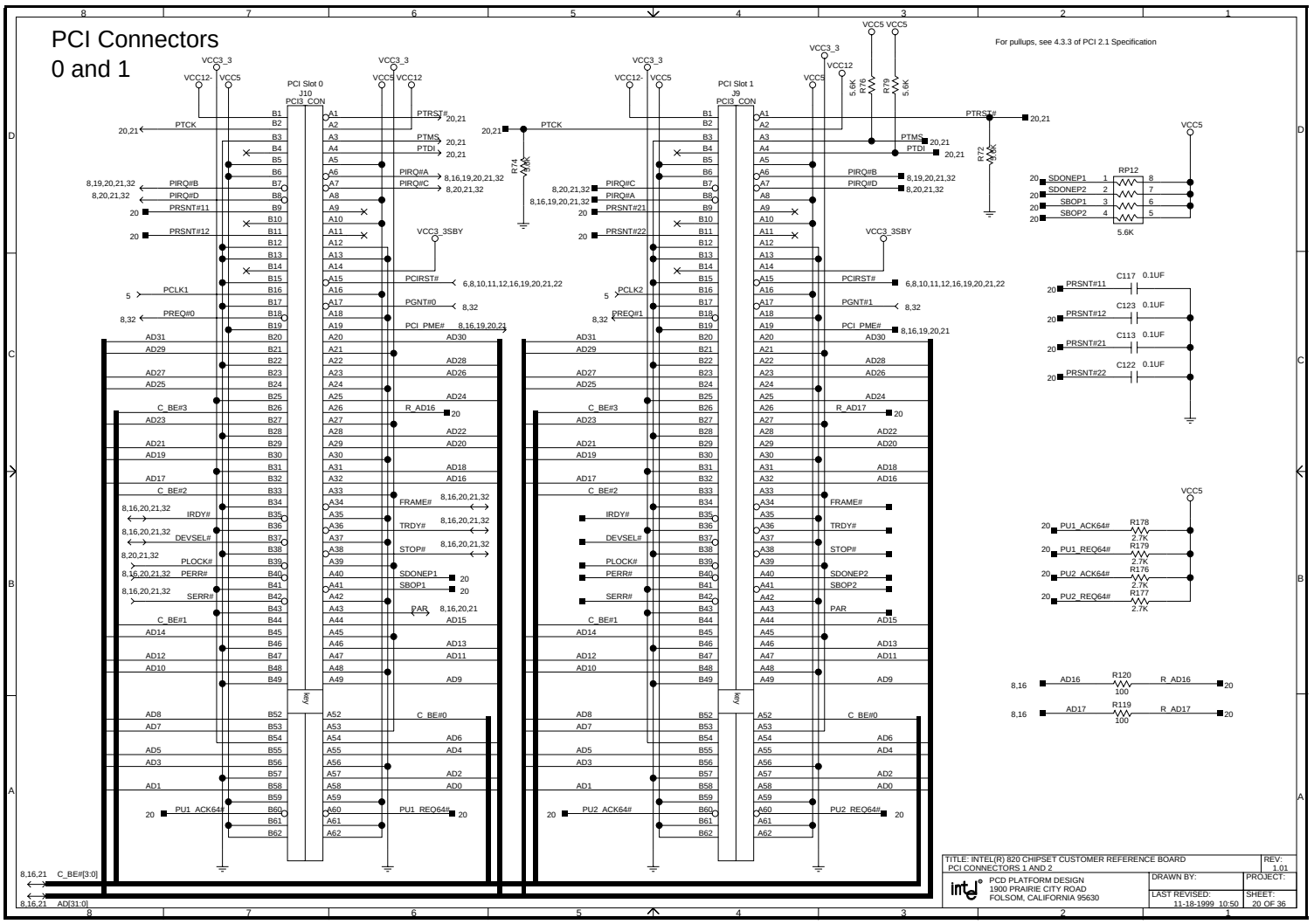
Onboard Spkr	JP25
Enable*	2-3
Disable	1-2

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD SYSTEM		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 10:49	SHEET: 18 OF 36

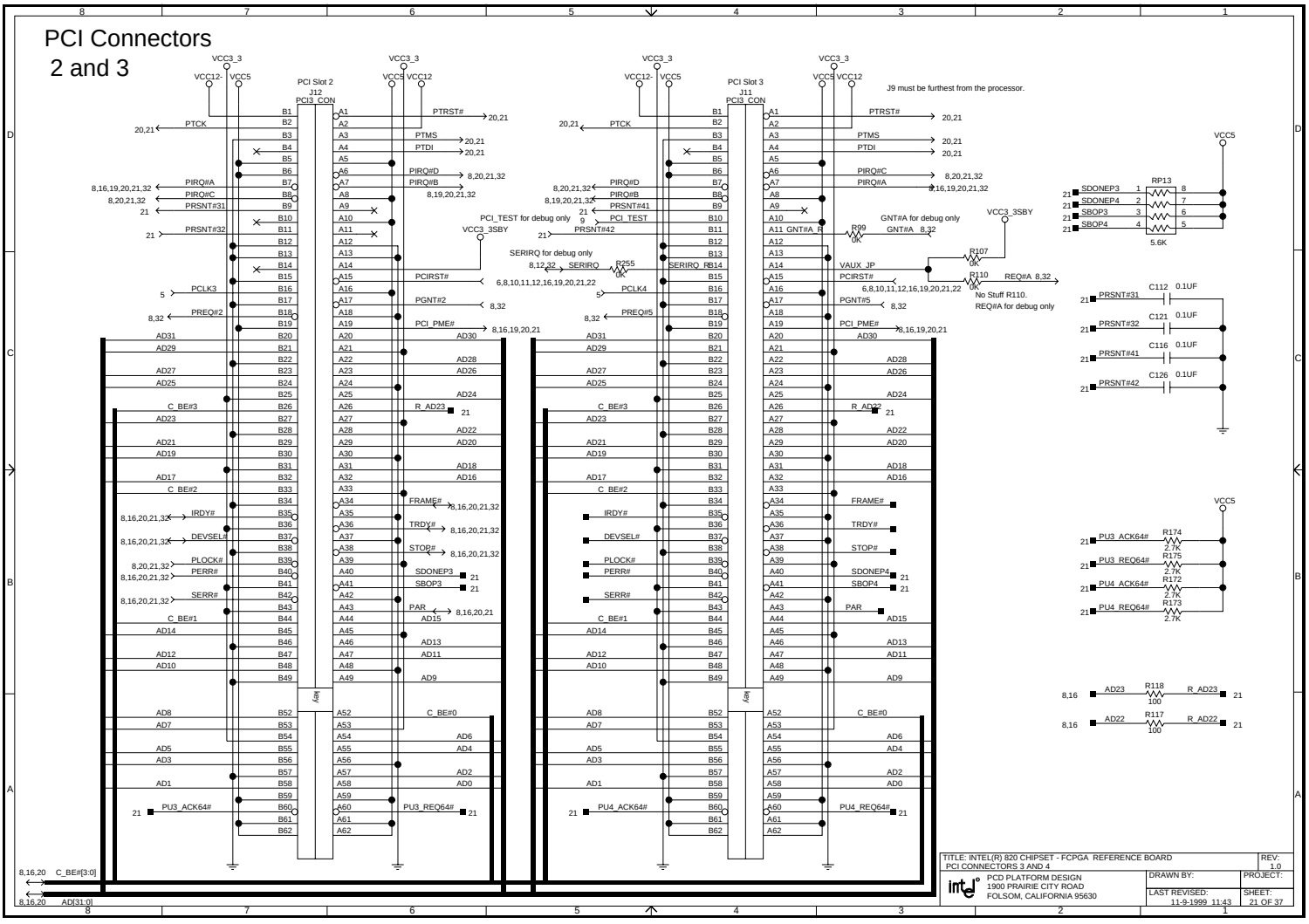
AGP Connector



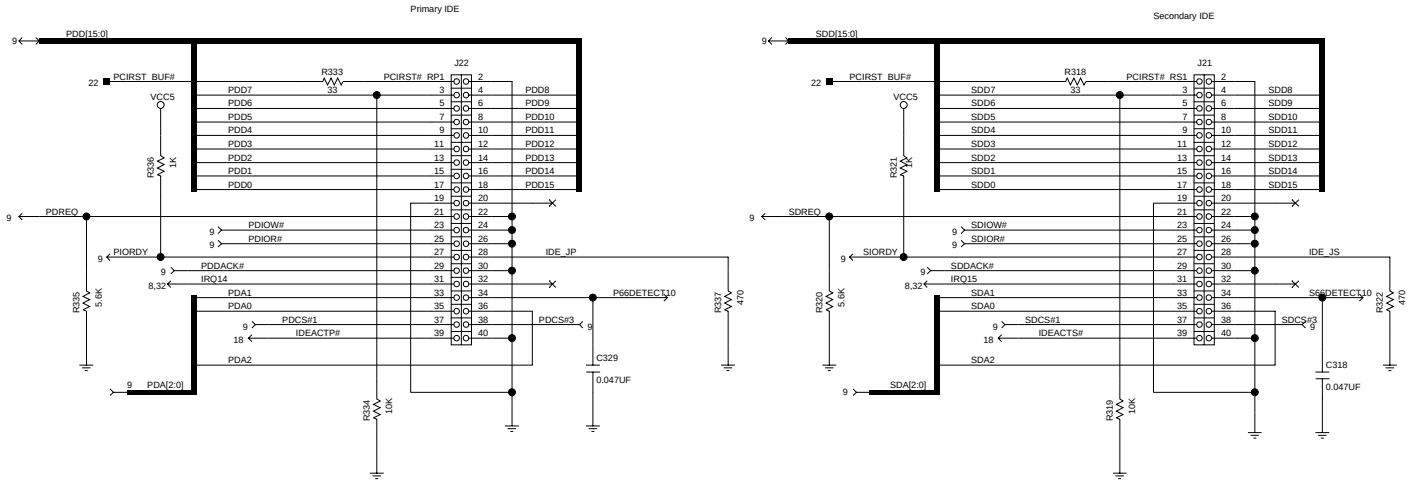
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD AGP CONNECTOR	REV: 1.01
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: / PROJECT:
LAST REVISED: 11-18-1999 10:49	SHEET: 19 OF 36


PCI Connectors
0 and 1
For pullups, see 4.3.3 of PCI 2.1 Specification
PCI Slot 0
J10
PCI3_CON
PCI Slot 1
J9
PCI3_CON
VCC3_3
VCC12-
VCC5
VCC12
VCC3_3SBY
PTRST#
PTCK
PTMS
PTDI
PIRQ#A
PIRQ#B
PIRQ#C
PIRQ#D
PRSNT#11
PRSNT#12
PRSNT#21
PRSNT#22
PCIRST#
PCLK1
PCLK2
PGNT#0
PGNT#1
PREQ#0
PREQ#1
PCI_PME#
AD31
AD29
AD27
AD25
C_BE#3
AD23
AD21
AD19
AD17
C_BE#2
IRDY#
DEVSEL#
PLOCK#
PERR#
SERR#
C_BE#1
AD14
AD12
AD10
AD8
AD7
AD5
AD3
AD1
C_BE#0
AD6
AD4
AD2
AD0
FRAME#
TRDY#
STOP#
SDONEP1
SBOP1
PAR
R_AD16
R_AD17
AD30
AD28
AD26
AD24
AD22
AD20
AD18
AD16
AD15
AD13
AD11
AD9
PU1_ACK64#
PU1_REQ64#
PU2_ACK64#
PU2_REQ64#
Key
R74
R72
R78
R79
5.6K
RP12
SDONEP1
SDONEP2
SBOP1
SBOP2
C117
C123
C113
C122
0.1UF
R178
R179
R176
R177
2.7K
R120
R119
100
8,16,21 C_BE#[3:0]
8,16,21 AD[31:0]
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD
PCI CONNECTORS 1 AND 2
REV: 1.01
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-18-1999 10:50
SHEET: 20 OF 36

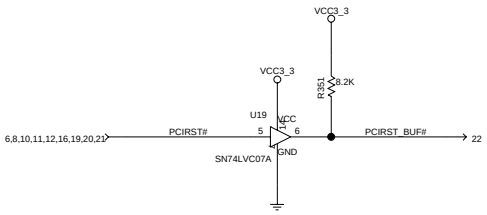
PCI Connectors 2 and 3



IDE Connectors

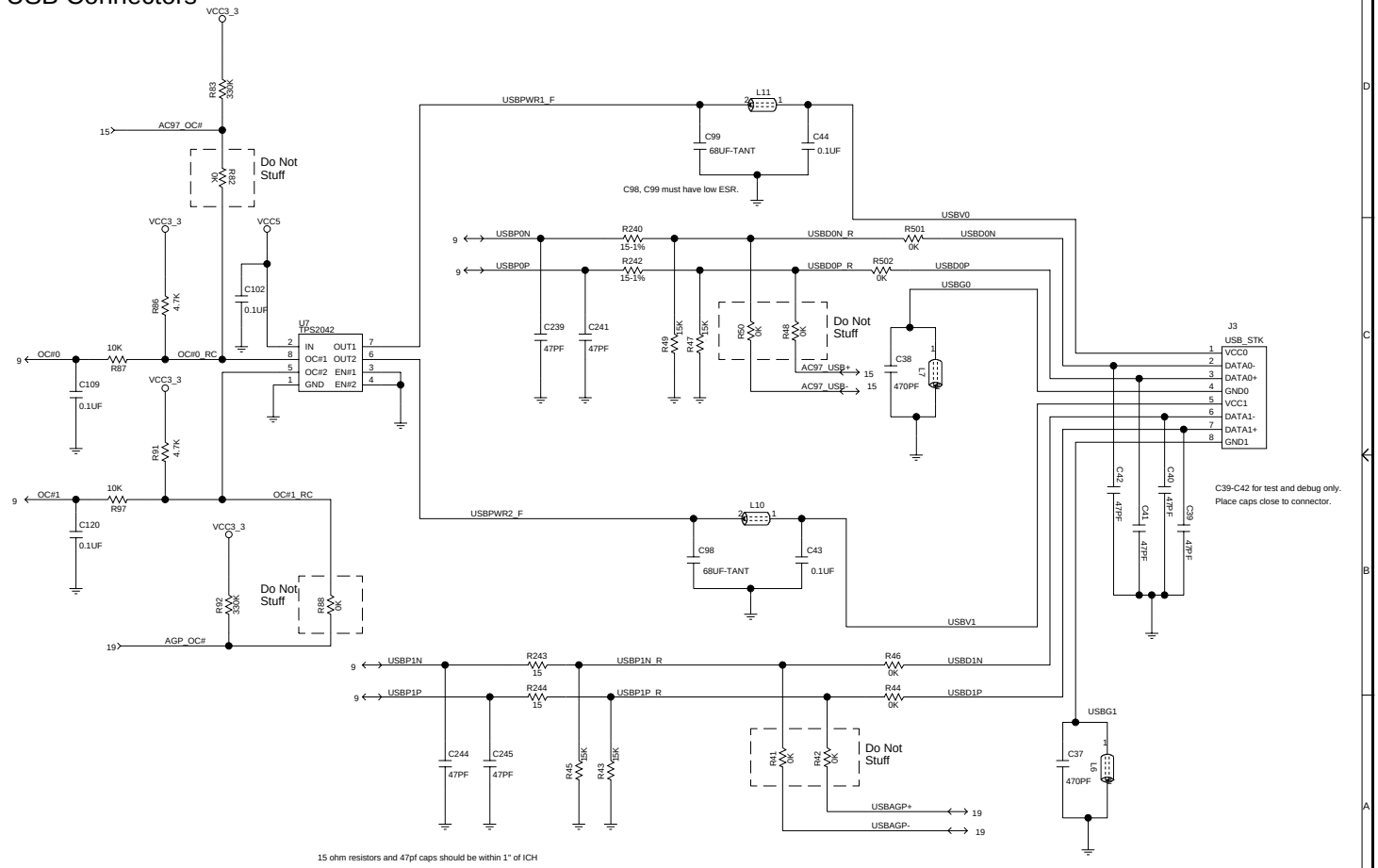


For drive side detection, stuff C329,C318.
For host side detection, no stuff C329,C318.
P66DETECT and S66DETECT can be connected to a GPI for BIOS cable detection.



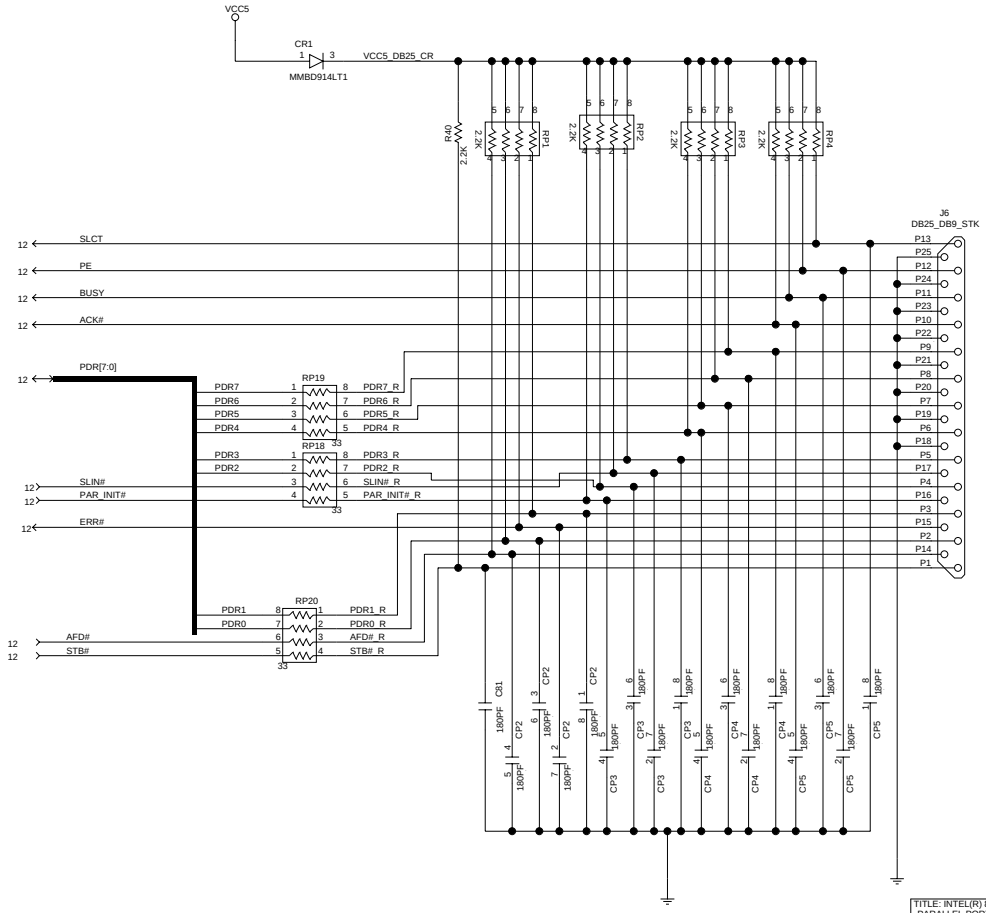
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD IDE CONNECTORS		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 10:51	SHEET: 22 OF 36

USB Connectors



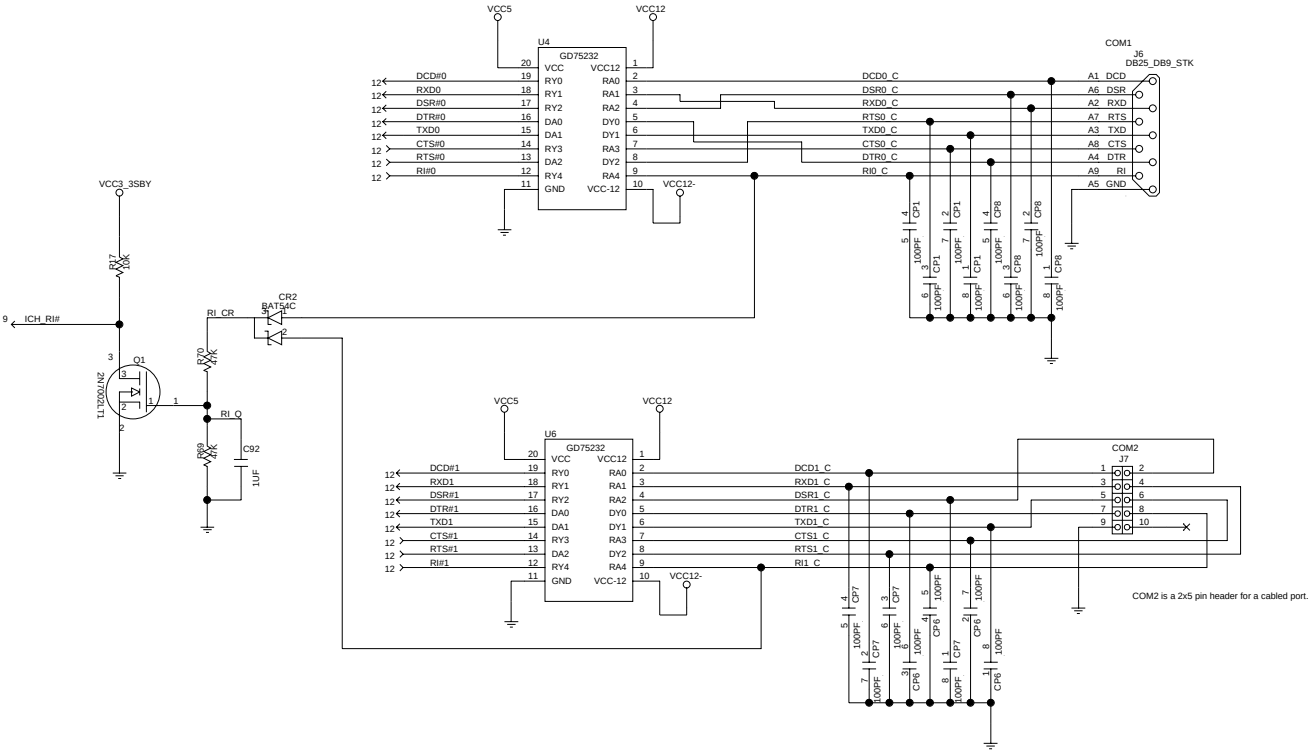
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD USB CONNECTORS		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 10:57	SHEET: 23 OF 36

Parallel Port



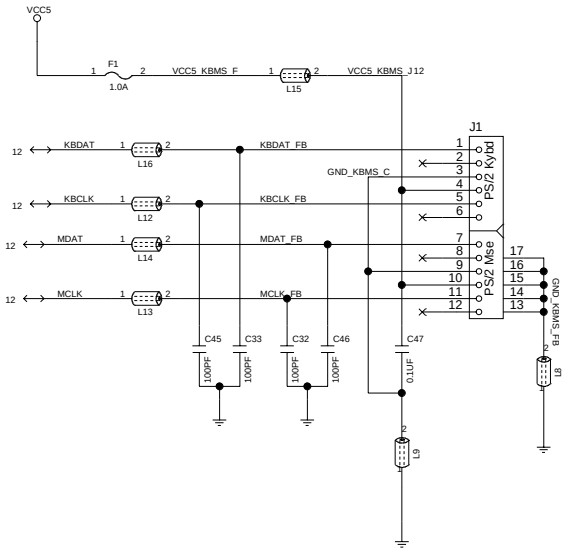
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD PARALLEL PORT		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 11:22	SHEET: 24 OF 36

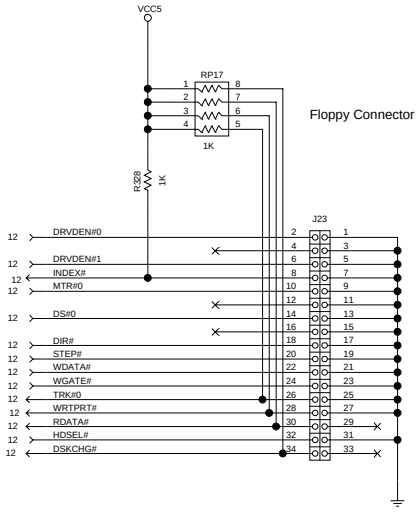
Serial Ports



TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD SERIAL PORTS		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 11:22	SHEET: 25 OF 36

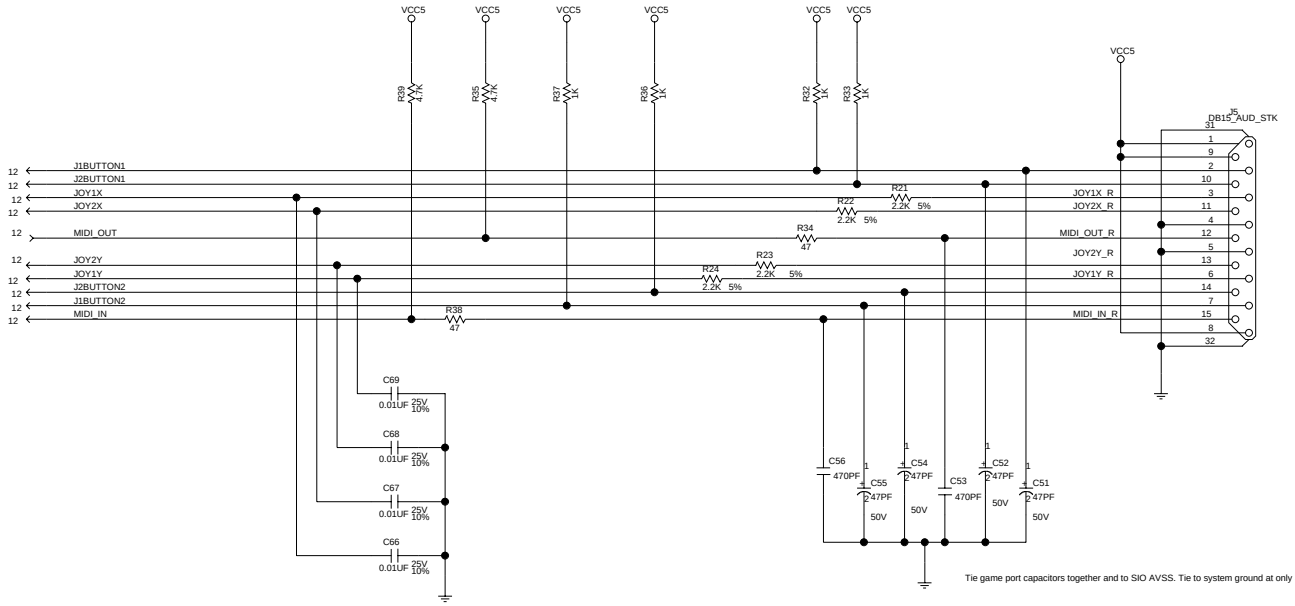
Keyboard/Mouse/Floppy





TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD KEYBOARD/MOUSE/FLOPPY		REV: 1.01
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 11:23	SHEET: 26 OF 36

Game Port

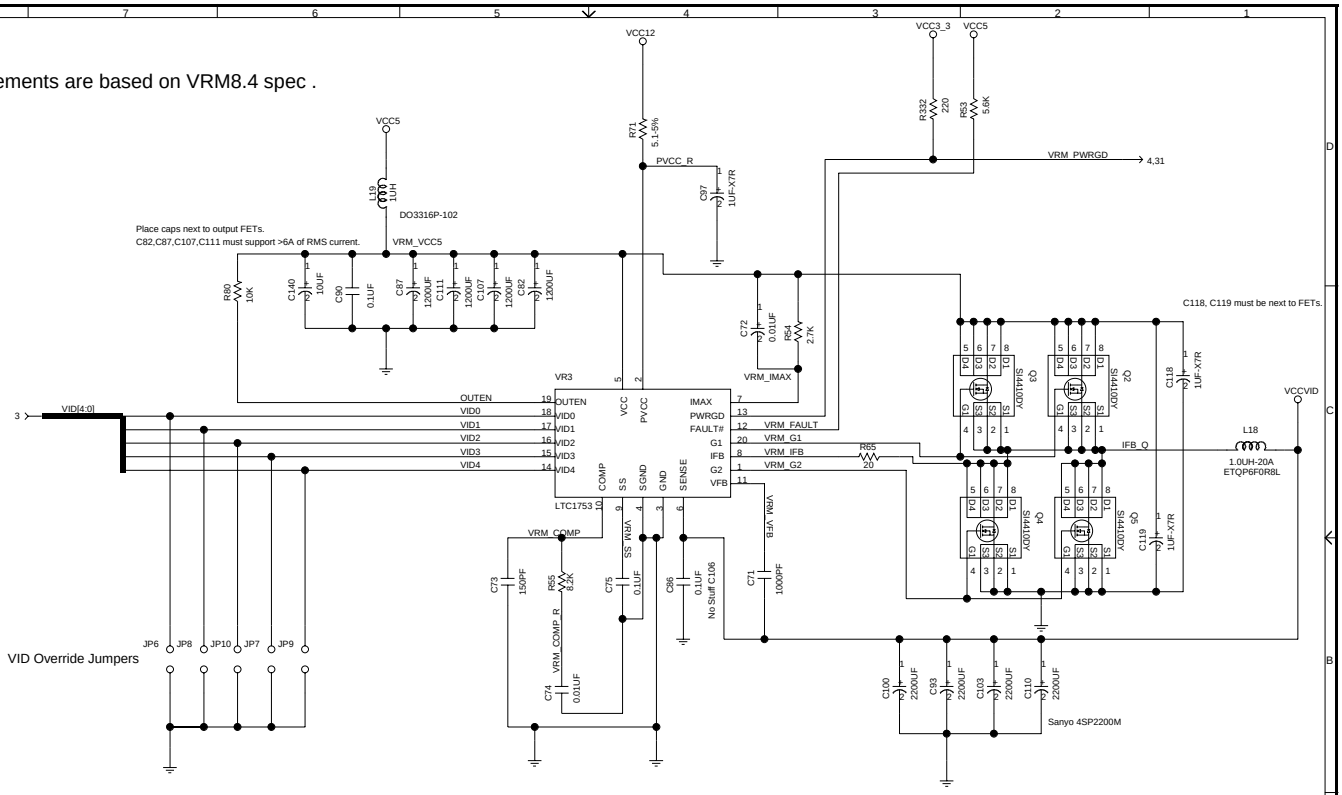


Tie game port capacitors together and to SIO AVSS. Tie to system ground at only a single point.

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD GAME PORT		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED:	SHEET: 27 OF 36

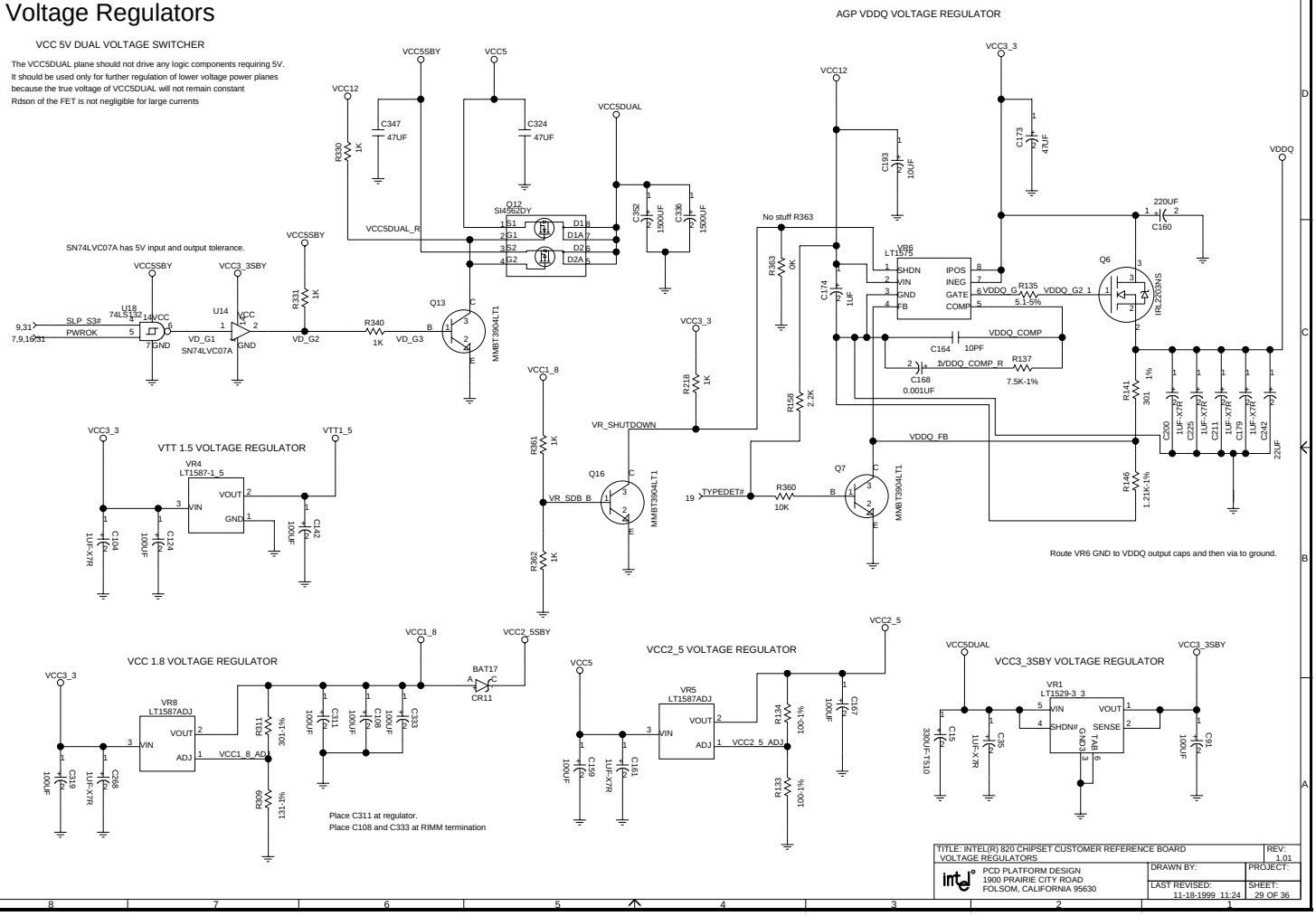
VRM

VRM requirements are based on VRM8.4 spec .

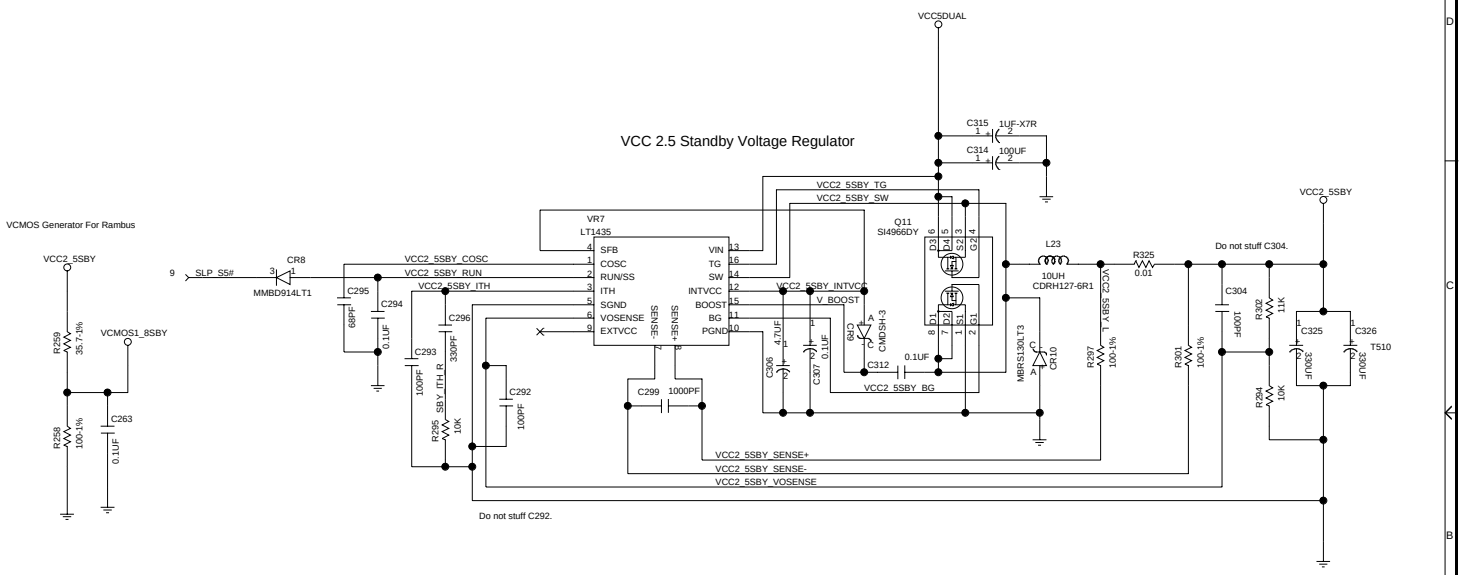


TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD VRM 8.2		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 11:24	SHEET: 28 OF 36

Voltage Regulators

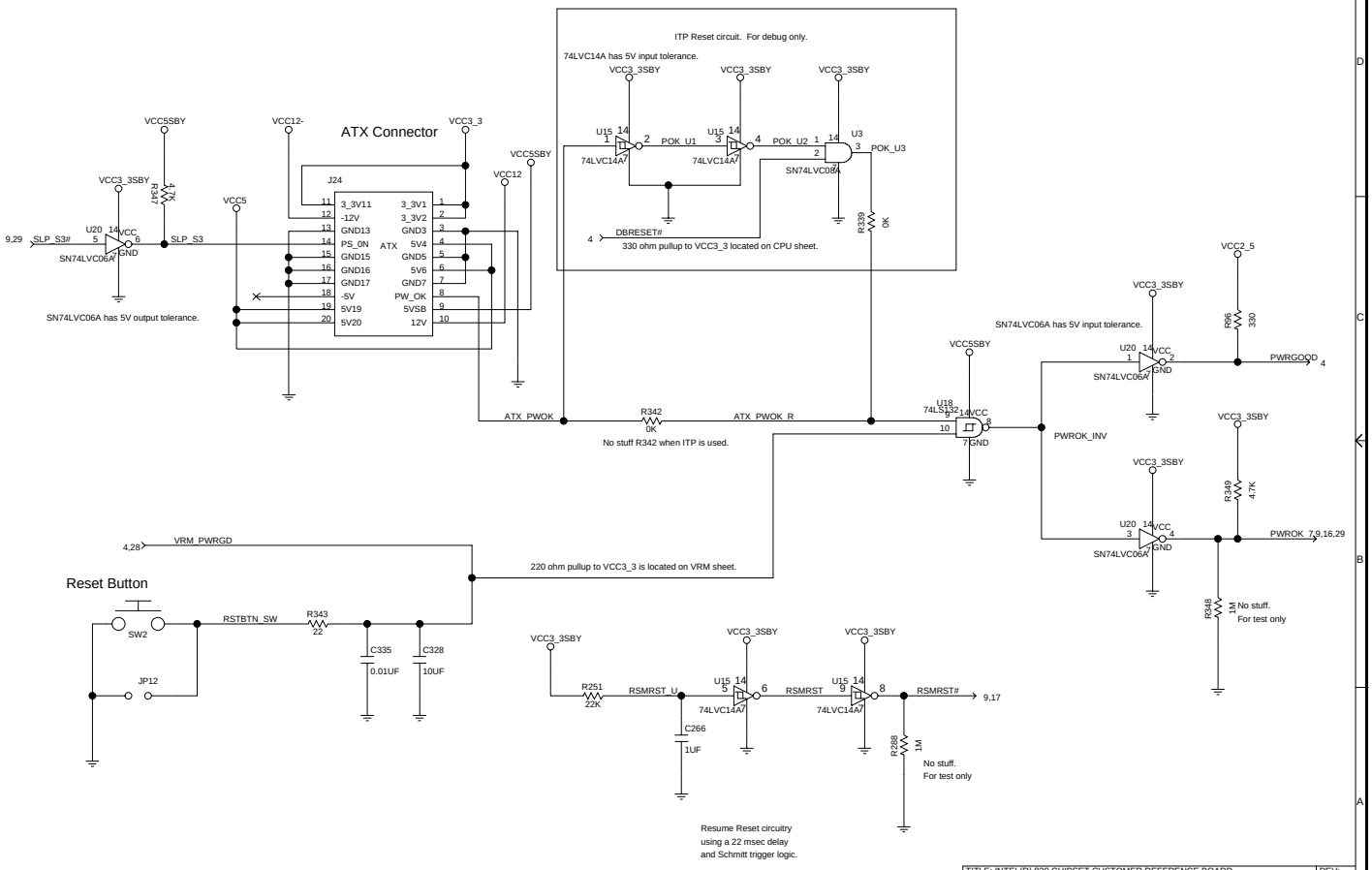


Voltage Regulators



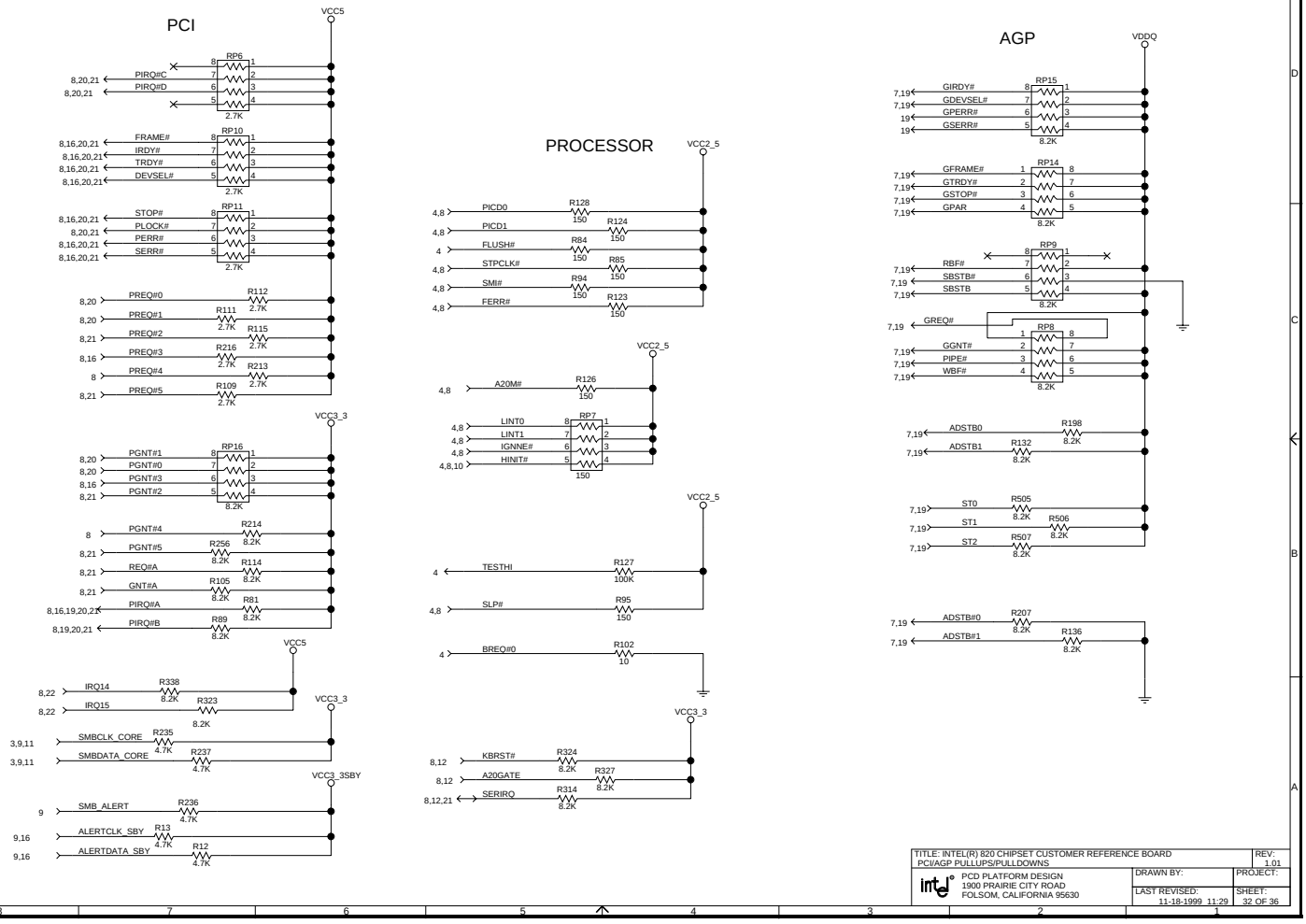
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD VOLTAGE REGULATORS		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 11:28	SHEET: 30 OF 36

Power Connector



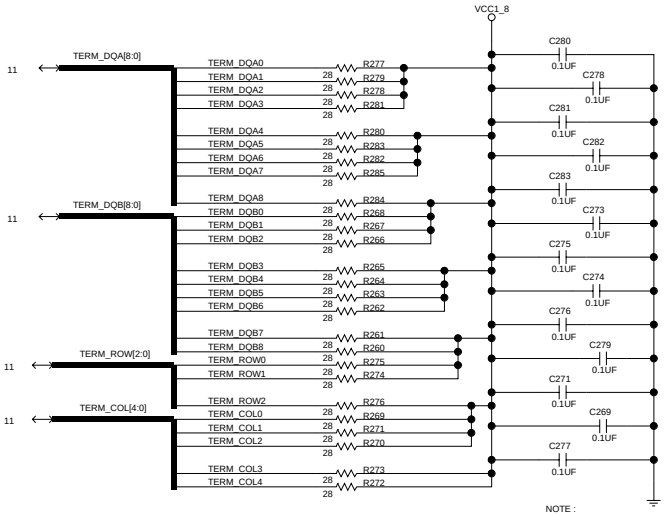
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD POWER CONNECTOR		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 11:28	SHEET: 31 OF 36

PCI/AGP Pullups/Pulldowns



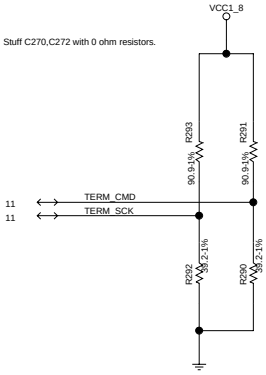
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD PCI/AGP PULLUPS/PULLDOWNS		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 11:29	SHEET: 32 OF 36

Rambus Termination



NOTE :

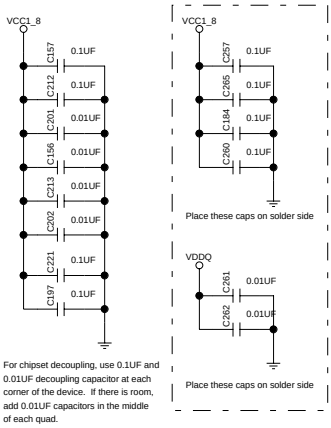
Use one 0.1uF cap
per two RSL signals.



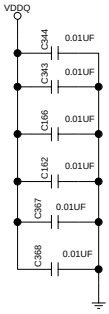
TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD RAMBUS TERMINATION		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 14:01	SHEET: 33 OF 36

Decoupling

MCH Decoupling

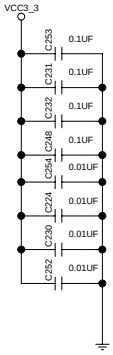


For chipset decoupling, use 0.1UF and 0.01UF decoupling capacitor at each corner of the device. If there is room, add 0.01UF capacitors in the middle of each quad.

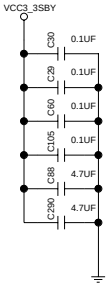


Place VDDQ capacitors within 70 mils of outer balls of MCH.

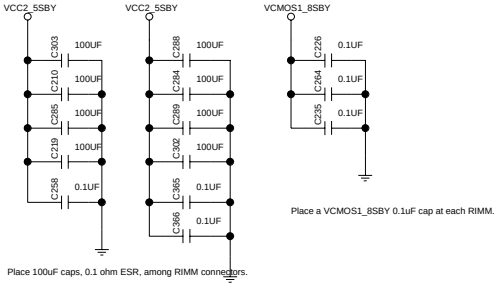
ICH Decoupling



82559 Decoupling.



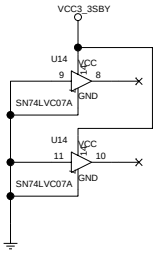
RIMM Decoupling

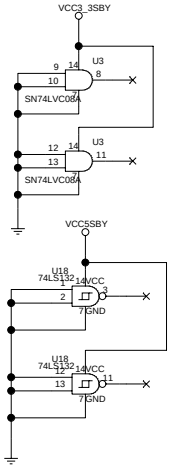


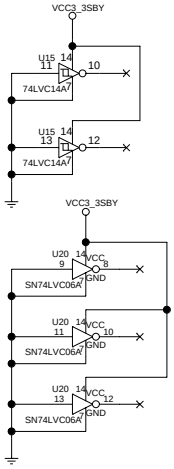
Place 100uF caps, 0.1 ohm ESR, among RIMM connectors.

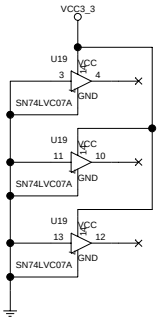
Place a VCMOS1_8SBY 0.1uF cap at each RIMM.

Un-used Gates



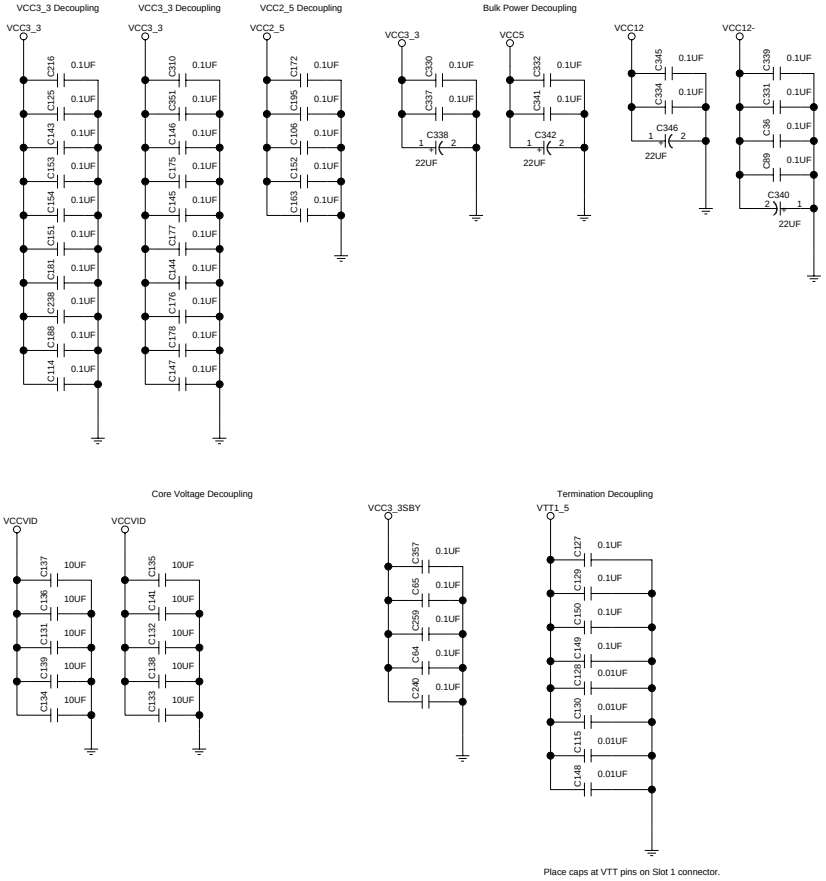






TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD DECOUPLING		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-30-1999 10:26	SHEET: 34 OF 36

Decoupling



Place caps at VTT pins on Slot 1 connector.

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD BULK DECOUPLING		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-18-1999 11:31	SHEET: 35 OF 36

Revision History

Revision 1.01

Pg 6 Modified MCH_AGPREF circuit, changed 432 ohm to 1K ohm and 62 ohm to 80.6 ohm.
Changed value of capacitor C194 from 0.1uF to 0.01uF.

Pg 8 Modified HUBREF circuit, deleted R222, R223 & C217, changed C218 from 470pF to 0.1uF.

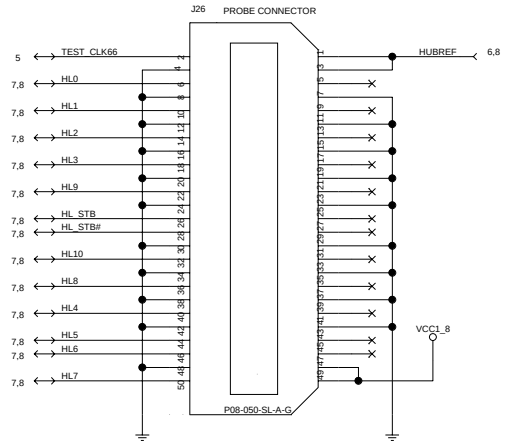
Pg 11 Modified RIMM connectors to eliminate 3.3V, added 0.1uF decoup caps to SVDDA & SVDDB on each RIMM.

Pg 33 Modified CMD and SCK termination values. Removed 470pF capacitors, Changed 93 ohm to 90.9 ohm,
and changed 39 ohm to 39.2 ohm resistors.

Pg 34 Deleted 3.3V decoupling for RIMM connectors. Added solder side decoup for MCH.
Changed VDDQ cap values from 0.1uF to 0.01uF.

TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD REVISION HISTORY		REV: 1.01
intel® PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-24-1999 11:38	SHEET: 36 OF 36

Hub Link Connector
For debug only.



TITLE: INTEL(R) 820 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.01
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED:	SHEET: 37 OF 36

B

Reference Board Schematics: Dual-Processor

This page is intentionally left blank.

Reference Design Schematics: Dual-Processor B

B.1 Reference Design Feature Set

The reference schematics feature the following core feature set:

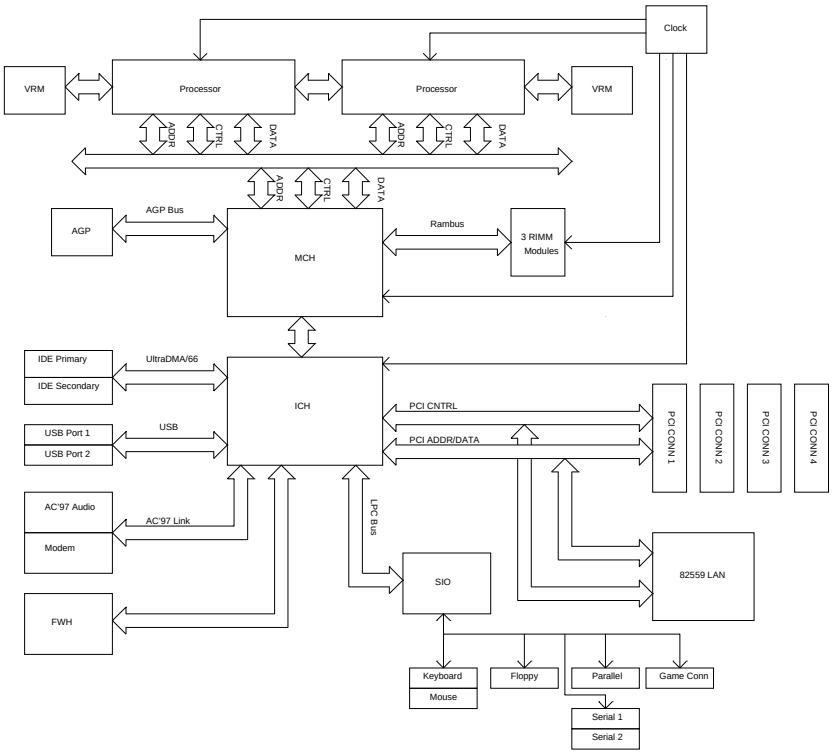
- Intel® 820 Chipset
  - — Memory Controller Hub (MCH)
  - — I/O Controller Hub (ICH)
  - — FWH Flash BIOS interface
- Support for the two Pentium III (SC242) Processors
  - — 100/133 MHz System Bus Frequency
  - — Debug Port
- IOAPIC Integrated into the ICH
- Direct RDRAM Memory Interface
  - — 266 MHz, 300 MHz, 356 MHz and 400 MHz Direct RDRAM Support
  - — 2 RIMM Sockets
- 4 PCI Add-in Slots
  - — Via 4 REQ/GNT pairs (ICH supports 6 REQ#/GNT# pairs)
- AGP Universal Connector
  - — 3.3V - 1X,2X signaling
  - — 1.5V – 1X, 2X, 4X signaling
- 2 IDE Connectors with Ultra ATA/66 Support
- 2 USB Connectors
- ATX Power Connector
- LPC Ultra I/O
  - — Floppy Disk Controller
  - — 1 Parallel Port, 2 Serial Ports
  - — Keyboard Controller
- AC‘97 Bus Connector and Audio Codec
- WfM Support
- Integrated System Management
- Integrated Power Management
  - — ACPI Rev. 1.0 Compliant
  - — APM Rev. 1.2 Compliant
- Pentium III on-board VRM 8.4 compliant regulator
- 4 Layer Design

INTEL(R) 820 CHIPSET
DUAL PROCESSOR CUSTOMER REFERENCE SCHEMATICS

Note that these schematics are preliminary and are subject to change.

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD		REV: 3.03
intel® PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:43	SHEET: 1 OF 38

Block Diagram



Device Table

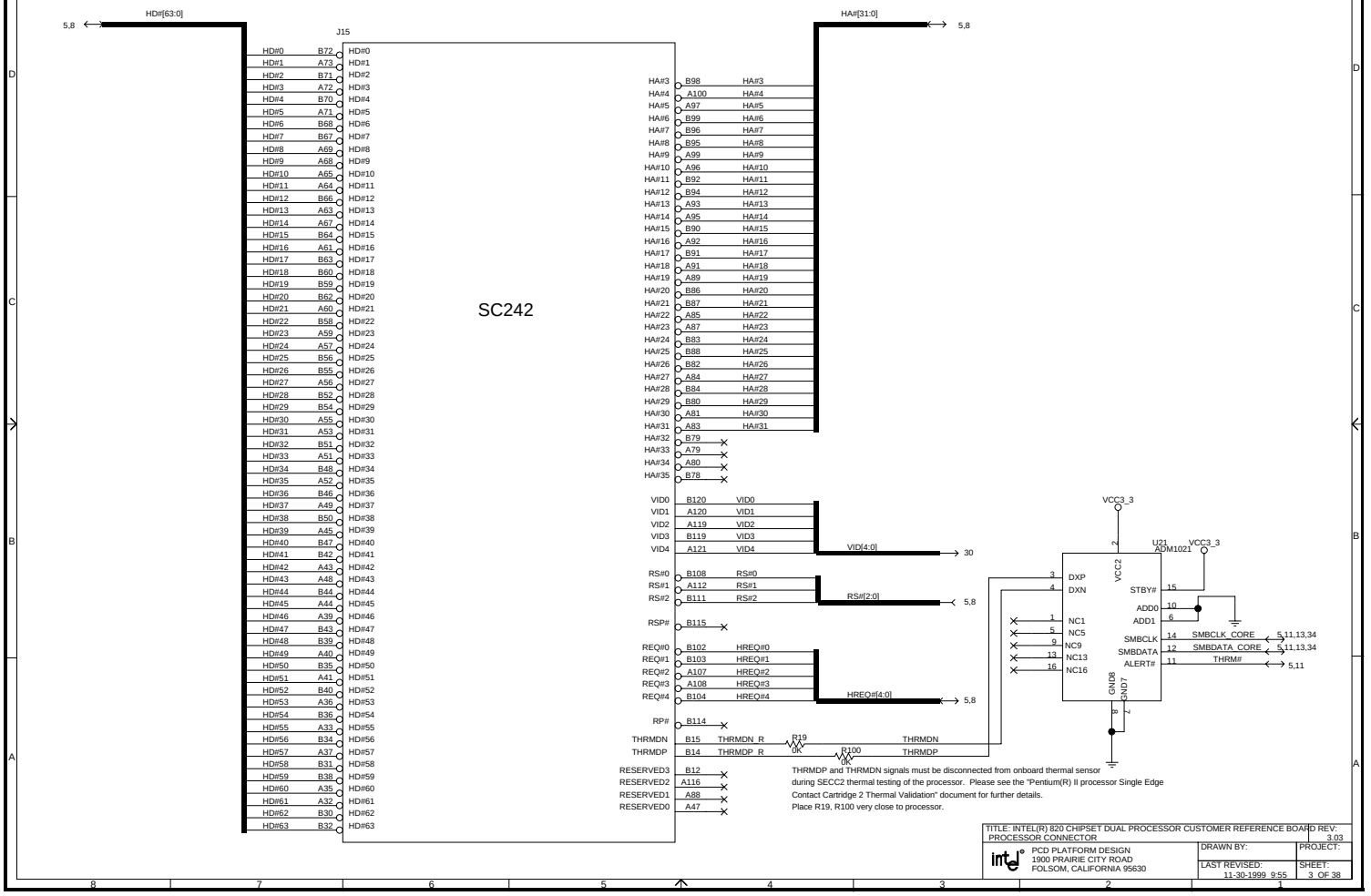
REFERENCE DESIGNATOR	DEVICE TYPE	GATES USED	SHEET NUMBER
U20	74LVC06A	A, B, C, D, E, F	33, 36
U14	74LVC07A	A, B, C, D, E, F	9,20,31,36
U19	74LVC07A	A, B, C, D, E, F	20,24,36
U3	74LVC08A	A, B, C, D	36, 33, 17
U9	74LVC08A	A, B	33
U26	74LVC08A	A	33
U15	74LVC14a	A, B, C, D, E, F	33, 36
U23	74LVC14a	A, B, C, D	33
U18	74LS132	A, B, C, D	31, 33, 36
U22	74LVC07A	A, B	33
U25	74F74	A, B	4
U13	82801 (ICH)		10, 11
U10	82820 (MCH)		8, 9
U5	82559		18
U24	93C46A		18
U2	AD1881		15
U11	CK133		7
U12	DRCG		7
U16	FWH		12
U4, U6	GD75232		27
U1	LM4880		16
U17	LPC47B27X		14
U21	ADM1021		3
U8	ADM1021		5
U7	TPS2042		25

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
BLOCK DIAGRAM

intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

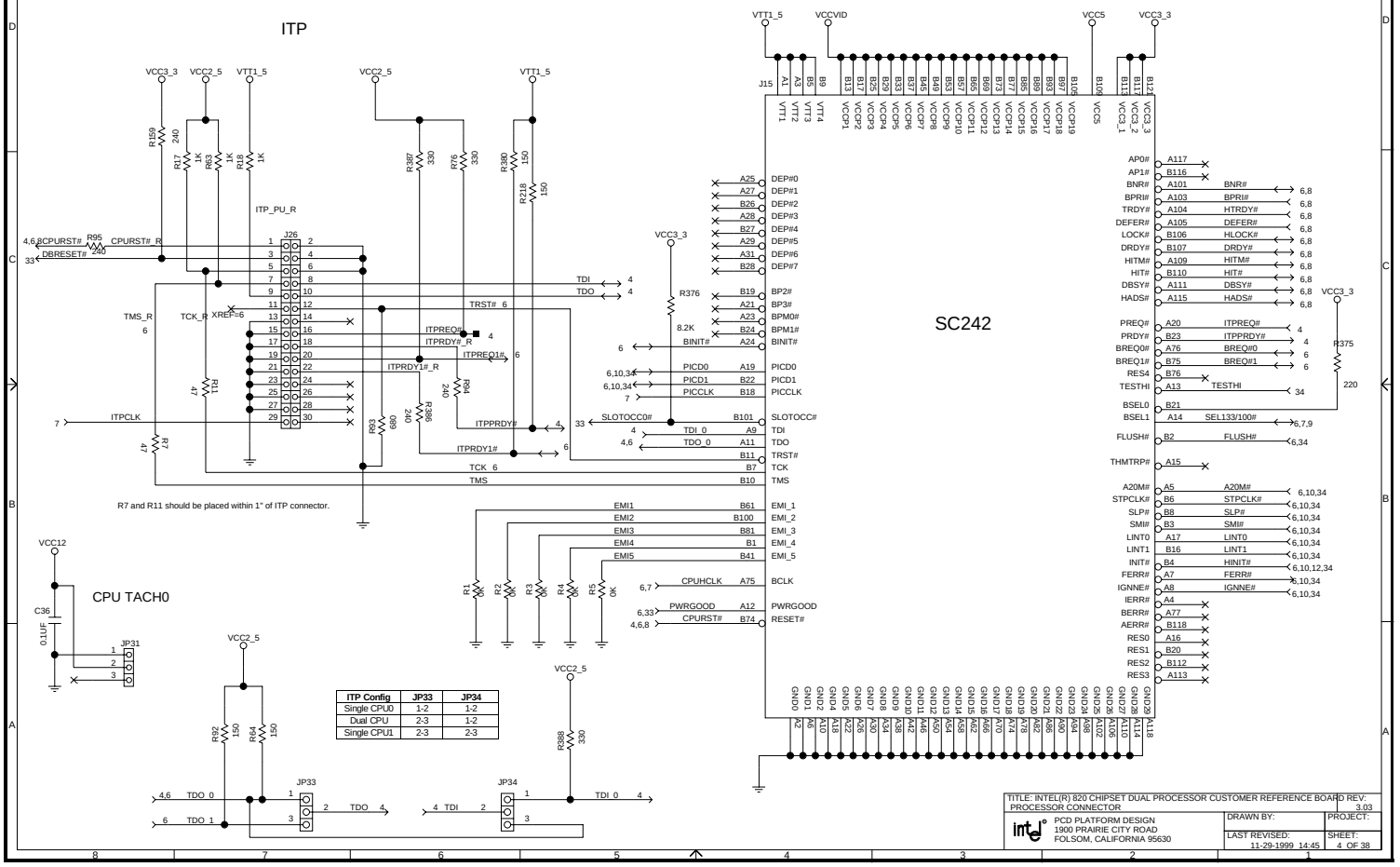
DRAWN BY: | PROJECT:
LAST REVISED: 11-29-1999 14:43 | SHEET: 2 OF 38

Processor Connector 0

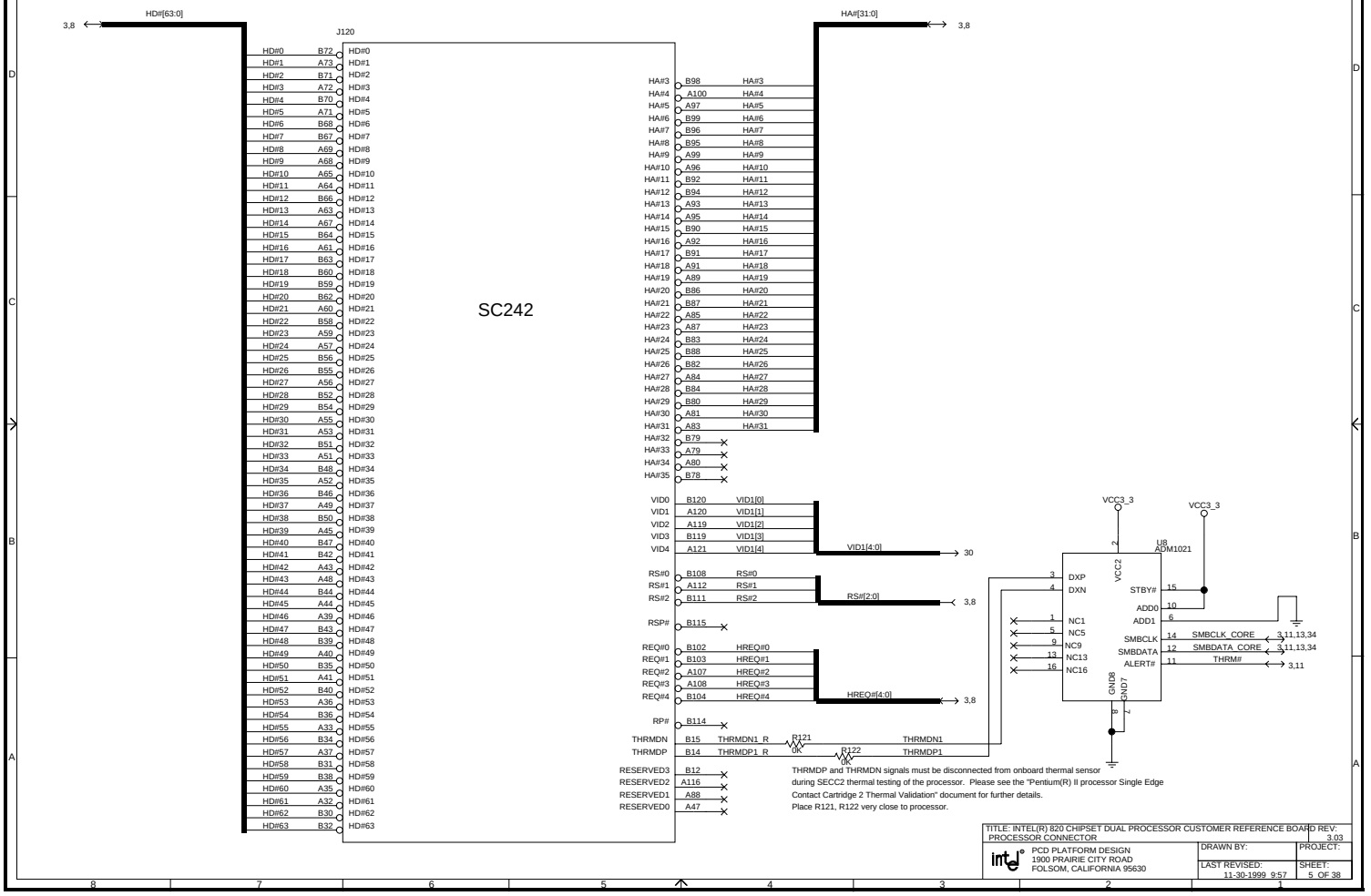


TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 PROCESSOR CONNECTOR	
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PROJECT: LAST REVISED: 11-30-1999 9:55 SHEET: 3 OF 38

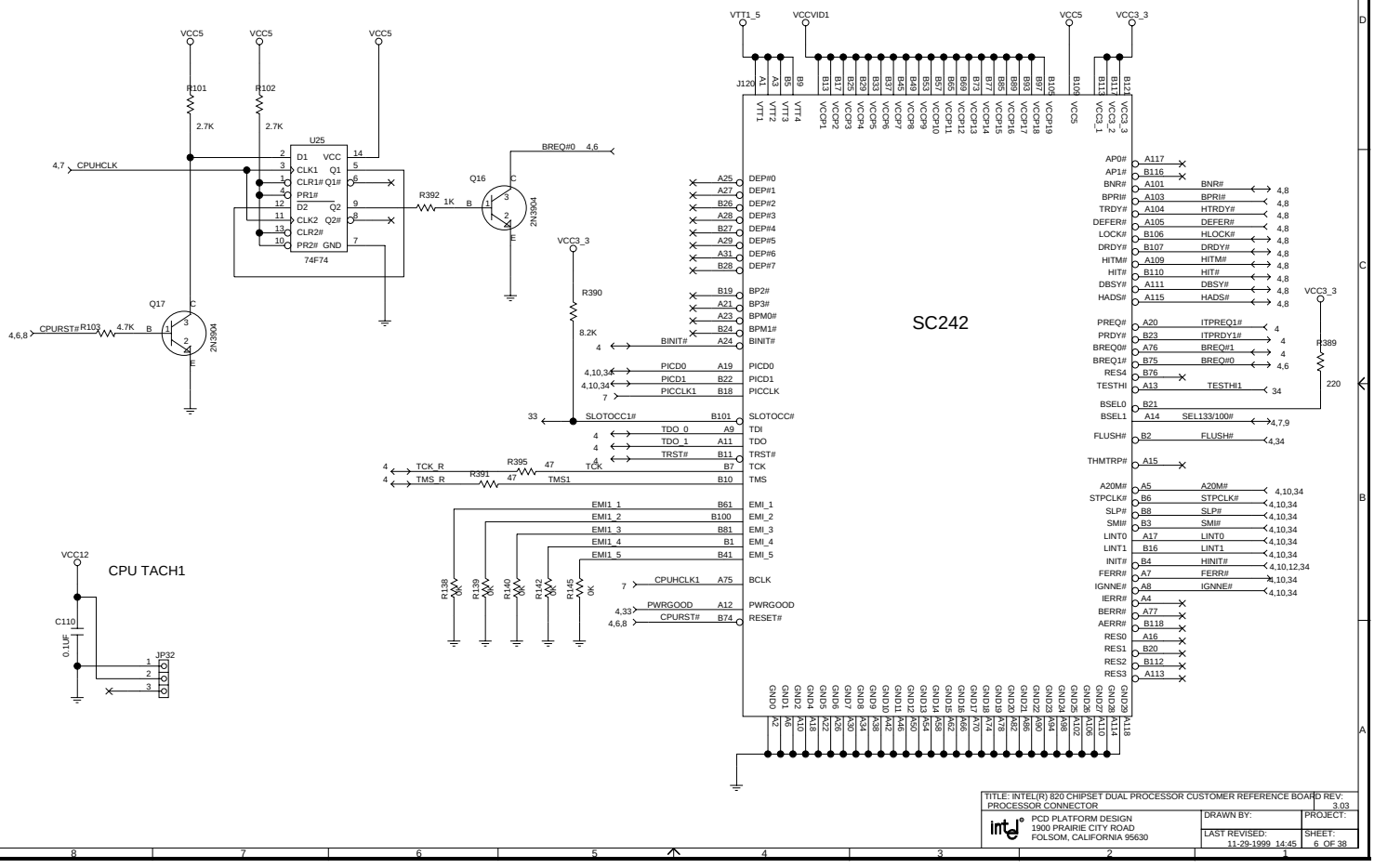
Processor Connector 0

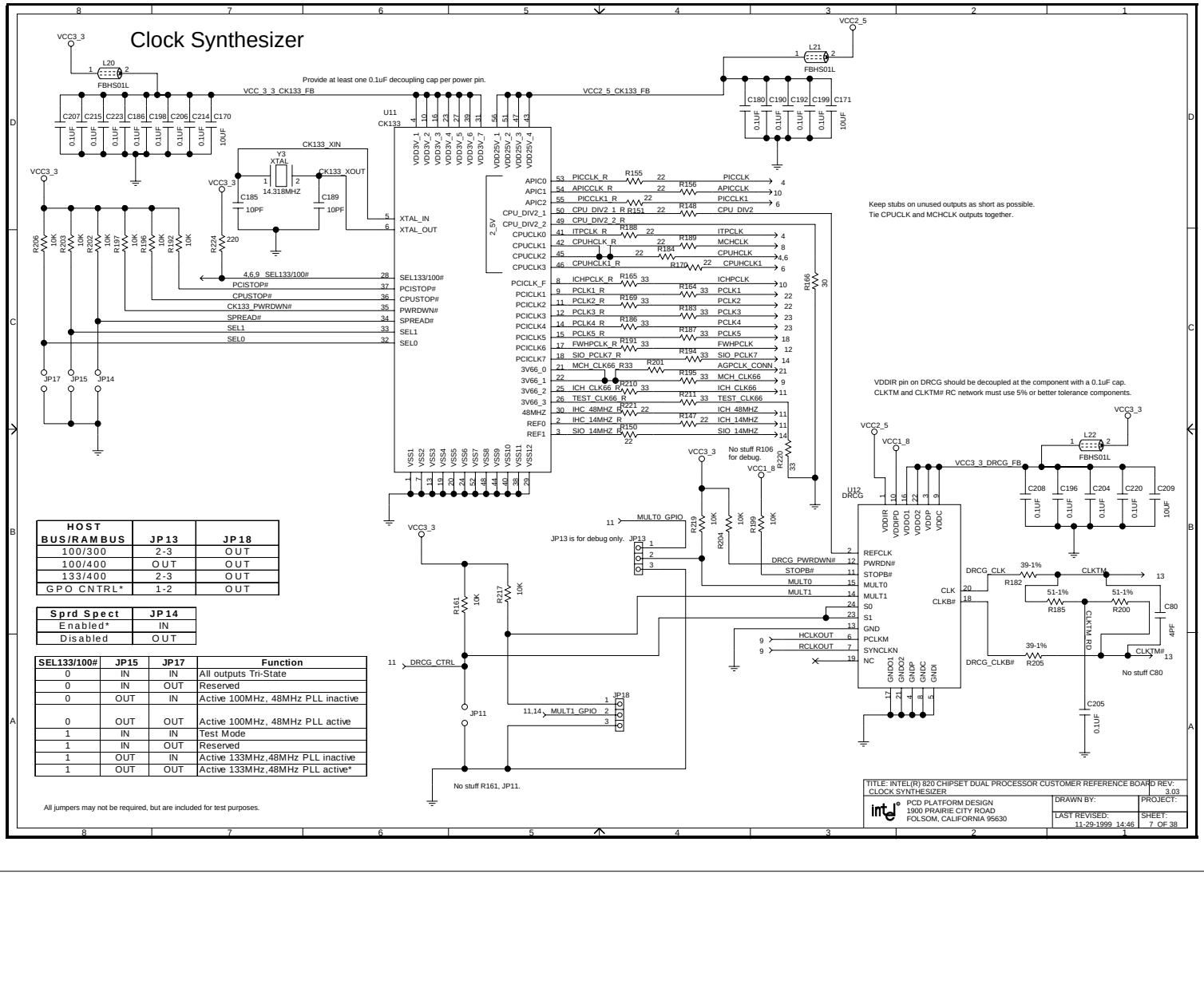


Processor Connector 1



Processor Connector 1



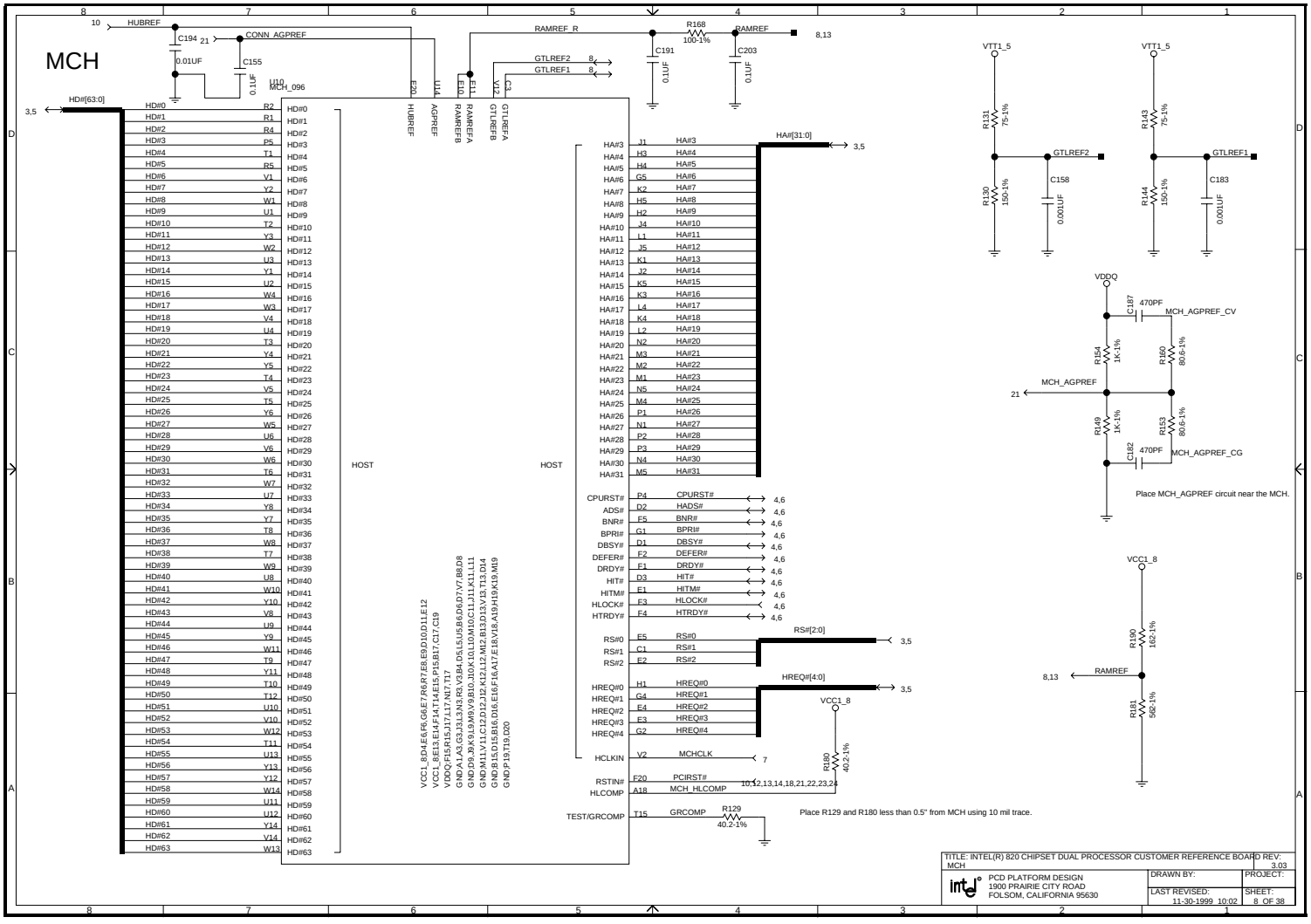


HOST BUS/RAMBUS	JP13	JP18
100/300	2-3	OUT
100/400	OUT	OUT
133/400	2-3	OUT
GPO CNTRL*	1-2	OUT

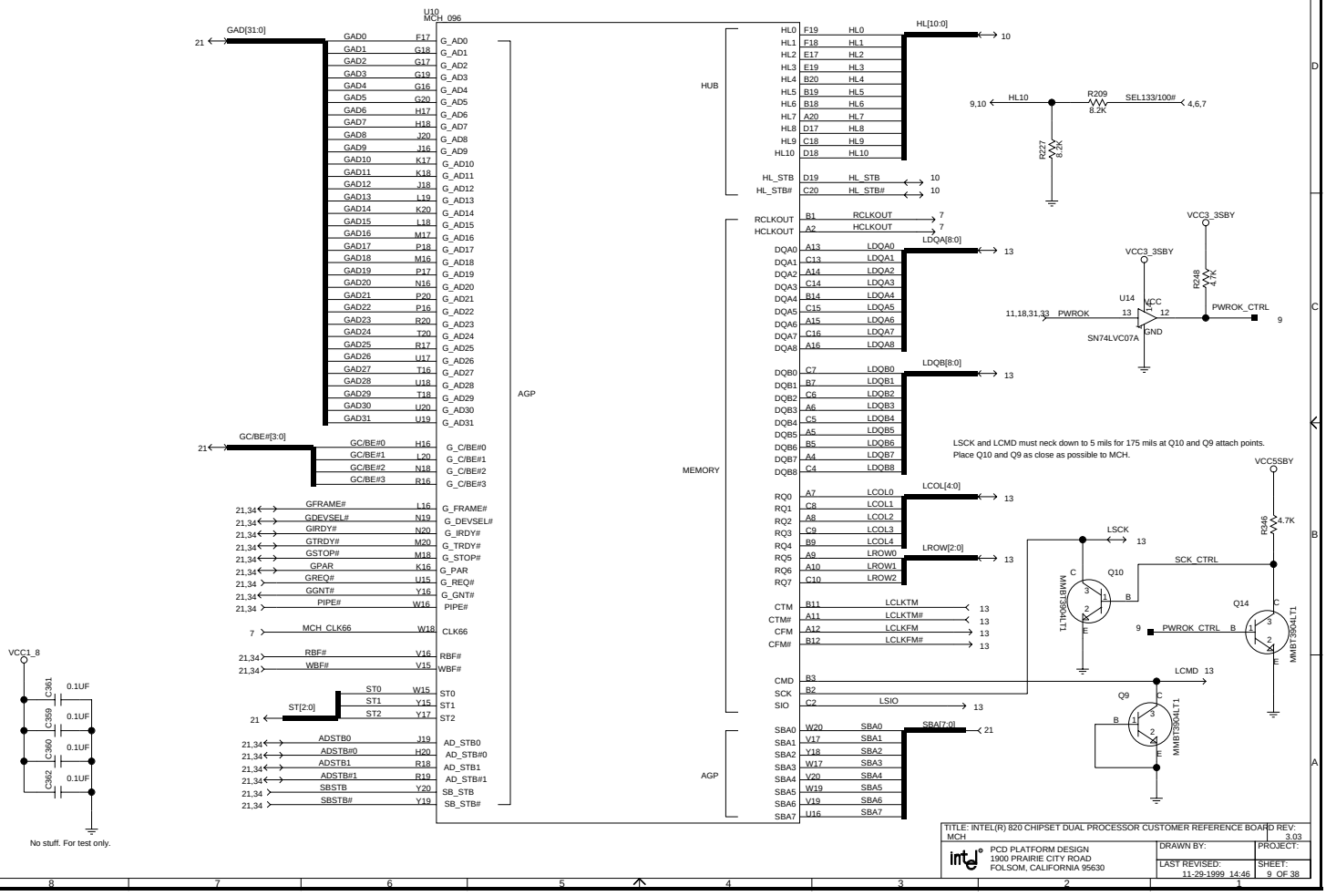
Sprd Spect	JP14
Enabled*	IN
Disabled	OUT

SEL133/100#	JP15	JP17	Function
0	IN	IN	All outputs Tri-State
0	IN	OUT	Reserved
0	OUT	IN	Active 100MHz, 48MHz PLL inactive
0	OUT	OUT	Active 100MHz, 48MHz PLL active
1	IN	IN	Test Mode
1	IN	OUT	Reserved
1	OUT	IN	Active 133MHz,48MHz PLL inactive
1	OUT	OUT	Active 133MHz,48MHz PLL active*

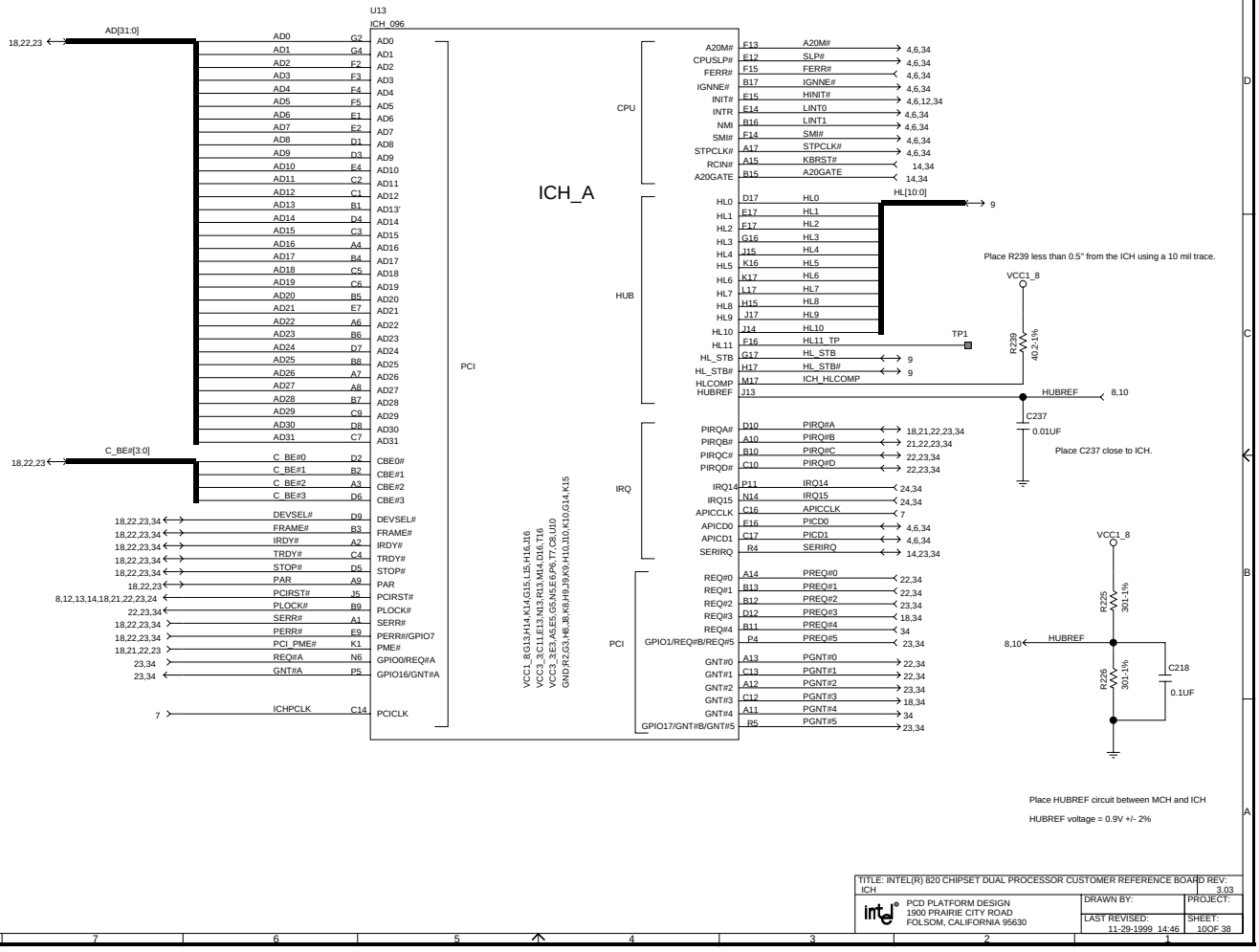
All jumpers may not be required, but are included for test purposes.


MCH
HUBREF
CONN_AGPREF
C194
0.01UF
C155
0.1UF
U10
MCH_096
RAMREF_R
R168
100-1%
RAMREF
C191
0.1UF
C203
0.1UF
GTLREF2
GTLREF1
HD#[63:0]
HOST
HA#[31:0]
VTT1_5
R131
75.1%
R120
150-1%
C158
0.001UF
R143
75.1%
R144
150-1%
C183
0.001UF
VDDQ
C187
470PF
MCH_AGPREF_CV
R154
1K-1%
R160
80.6-1%
MCH_AGPREF
R149
1K-1%
R153
80.6-1%
C182
470PF
MCH_AGPREF_CG
Place MCH_AGPREF circuit near the MCH.
VCC1_8
R190
162-1%
RAMREF
R181
562-1%
CPURST#
ADS#
BNR#
BPRI#
DBSY#
DEFER#
DRDY#
HIT#
HITM#
HLOCK#
HTRDY#
RS#[2:0]
HREQ#[4:0]
HCLKIN
MCHCLK
RSTIN#
PCIRST#
HLCOMP
MCH_HLCOMP
TEST/GRCOMP
GRCOMP
R129
40.2-1%
R180
40.2-1%
Place R129 and R180 less than 0.5" from MCH using 10 mil trace.
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
MCH
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-30-1999 10:02
SHEET: 8 OF 38

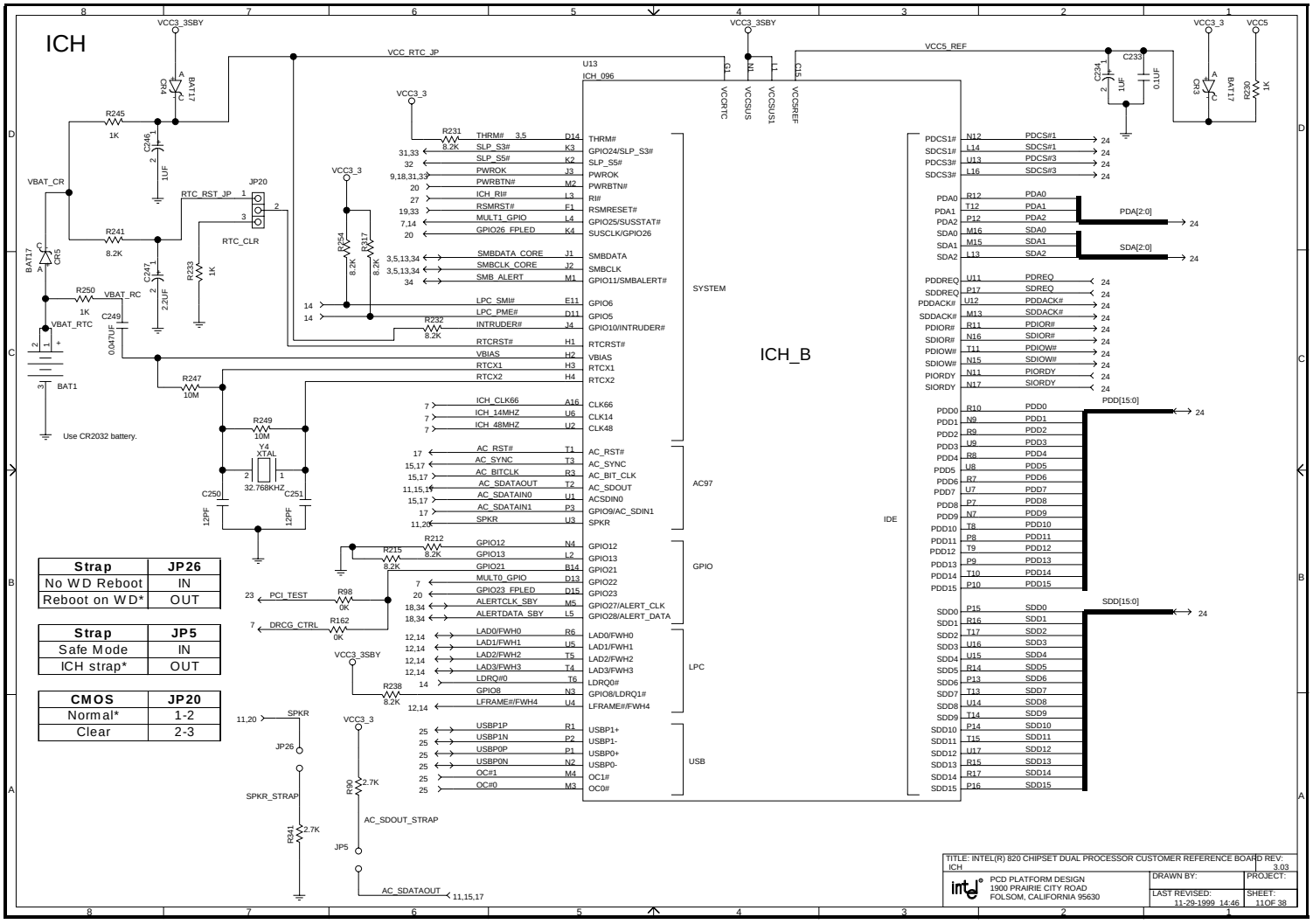
MCH


U10
MCH_096
GAD[31:0]
GC/BE#[3:0]
AGP
HUB
MEMORY
HL[10:0]
LDQA[8:0]
LDQB[8:0]
LCOL[4:0]
LROW[2:0]
SBA[7:0]
LSCK and LCMD must neck down to 5 mils for 175 mils at Q10 and Q9 attach points.
Place Q10 and Q9 as close as possible to MCH.
VCC1_8
No stuff. For test only.
VCC3_3SBY
VCCSSBY
SN74LVC07A
MMBT3904LT1
PWROK_CTRL
SCK_CTRL
LSCK
LCMD
LSIO
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
MCH
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-29-1999 14:46
SHEET: 9 OF 38

ICH



TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03	
ICH	
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PROJECT: LAST REVISED: 11-29-1999 14:46 SHEET: 10OF 38



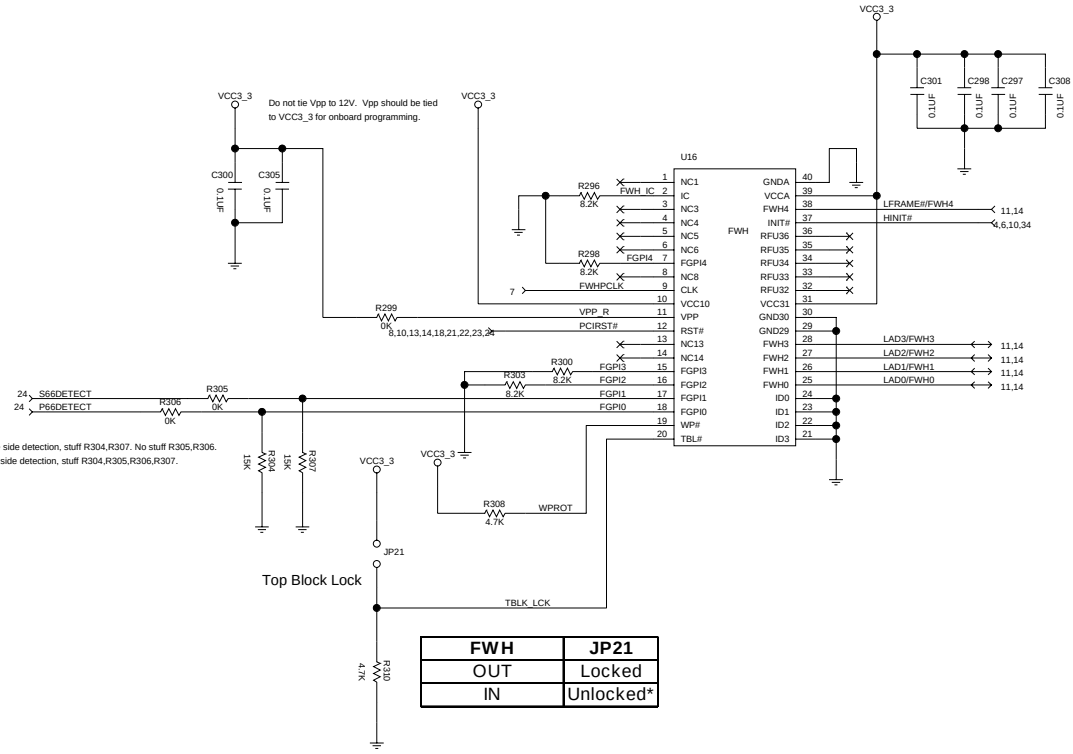
Strap	JP26
No WD Reboot	IN
Reboot on WD*	OUT

Strap	JP5
Safe Mode	IN
ICH strap*	OUT

CMOS	JP20
Normal*	1-2
Clear	2-3

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
ICH
intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-29-1999 14:46
SHEET: 11OF 38

FWH



FWH	JP21
OUT	Locked
IN	Unlocked*

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
FWH

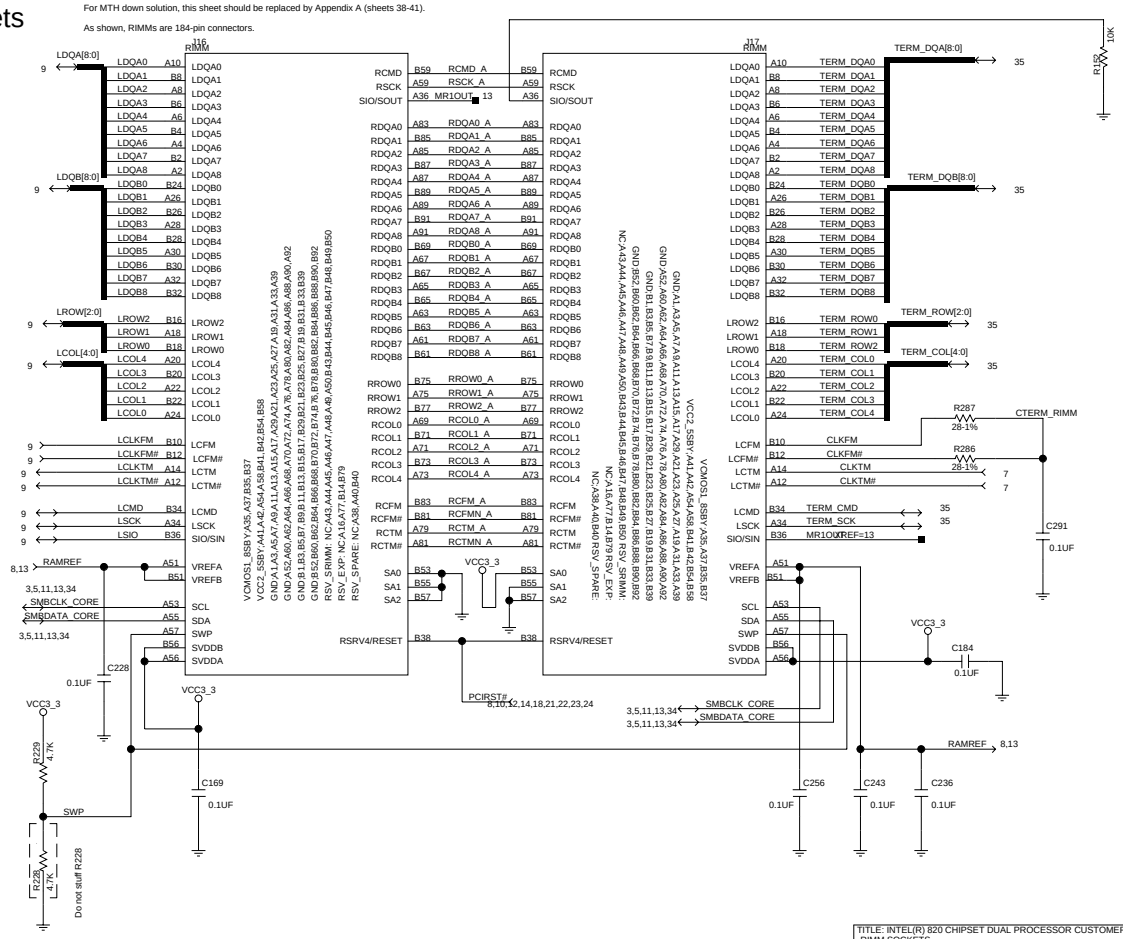
intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY: | PROJECT:
LAST REVISED: 11-29-1999 14:46 | SHEET: 12 OF 38

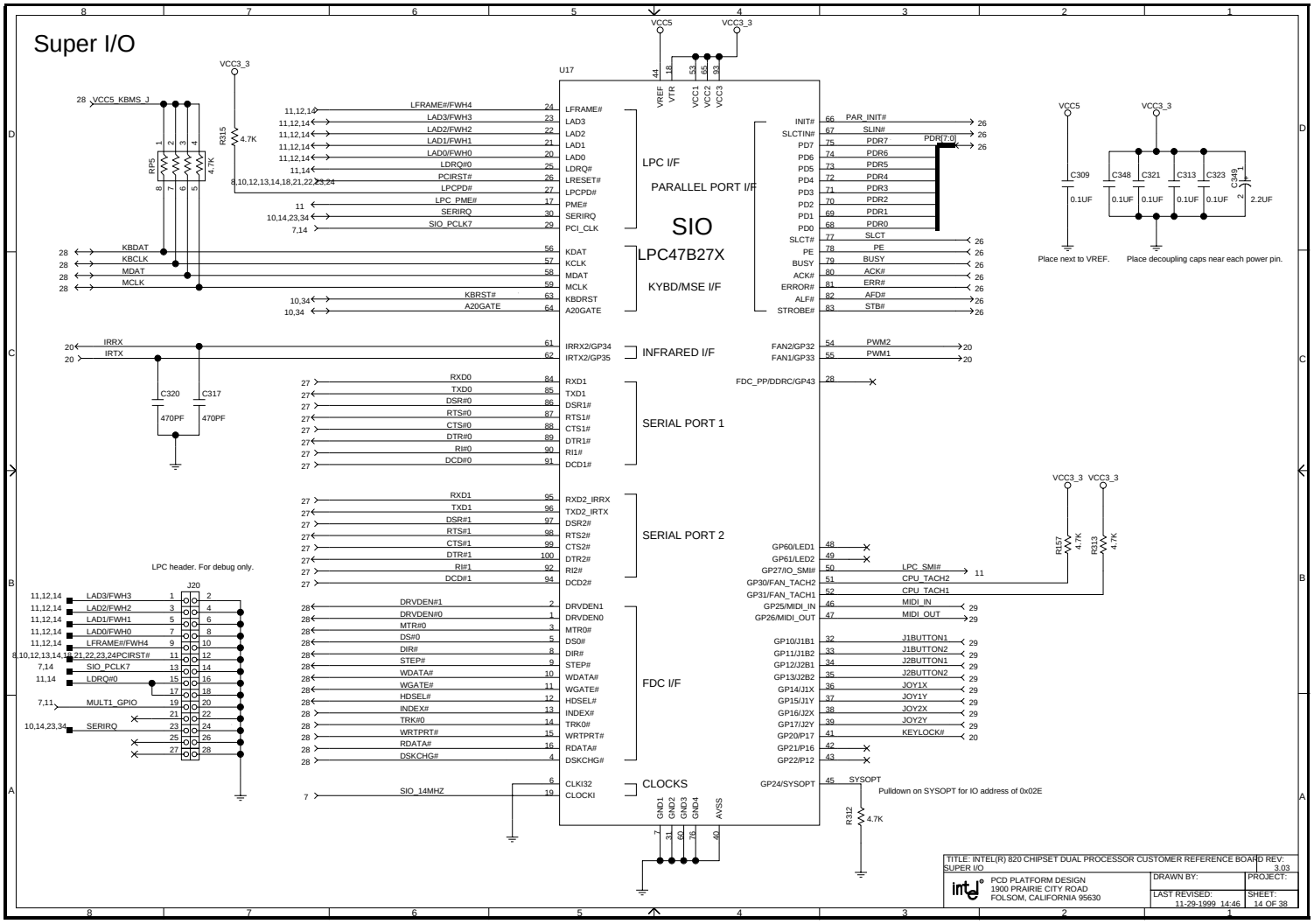
RIMM Sockets

For MTH down solution, this sheet should be replaced by Appendix A (sheets 38-41).

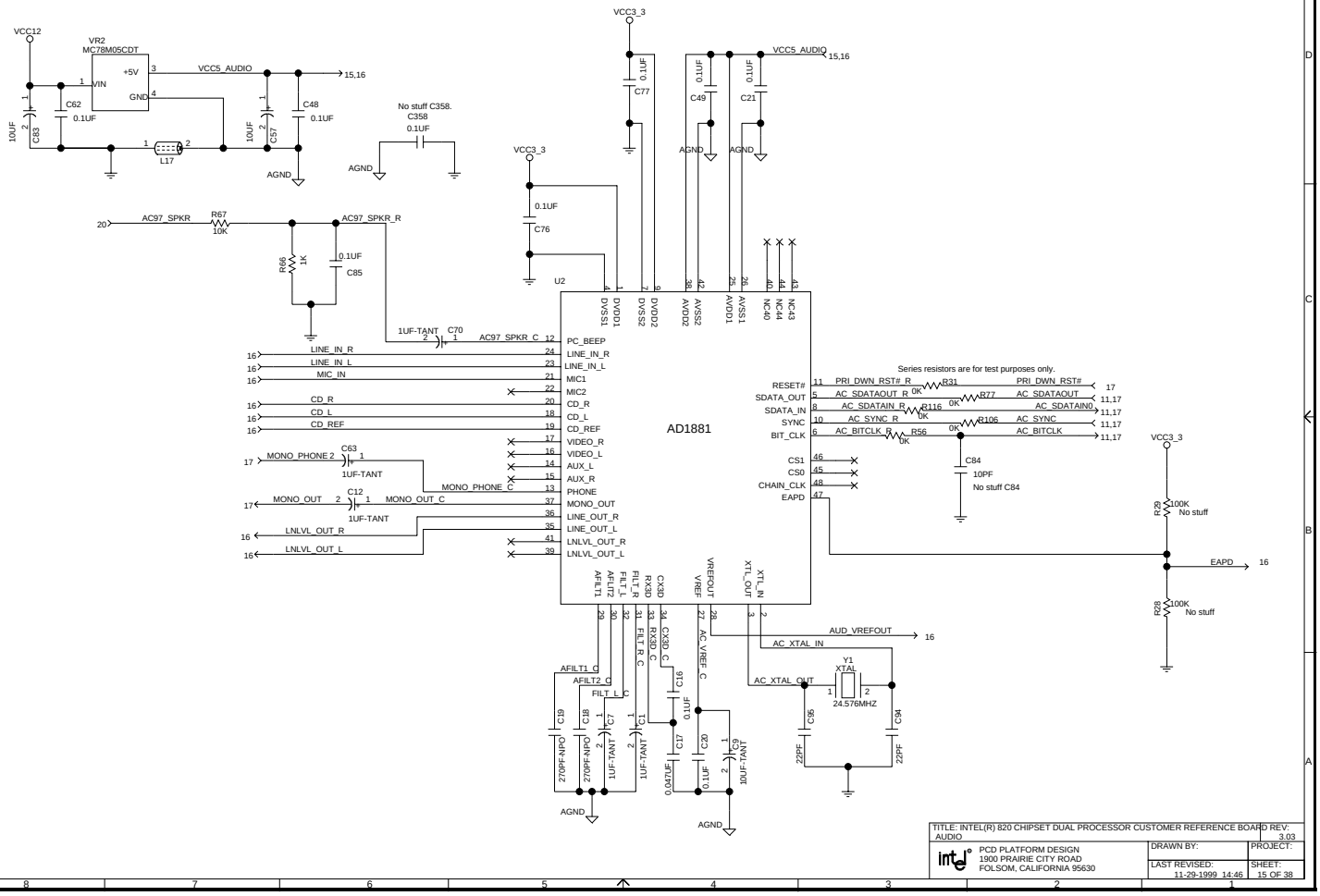
As shown, RIMMs are 184-pin connectors.



TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 RIMM SOCKETS	
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PROJECT: LAST REVISED: 11-29-1999 14:46 SHEET: 13 OF 38

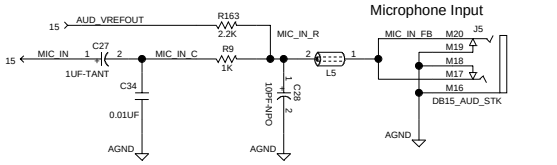

Super I/O
U17
SIO
LPC47B27X
LPC I/F
PARALLEL PORT I/F
KYBD/MSE I/F
INFRARED I/F
SERIAL PORT 1
SERIAL PORT 2
FDC I/F
CLOCKS
LFRAME#/FWH4
LAD3/FWH3
LAD2/FWH2
LAD1/FWH1
LAD0/FWH0
LDRQ#0
PCIRST#
LPCPD#
LPC_PME#
SERIRQ
SIO_PCLK7
KBDAT
KBCLK
MDAT
MCLK
KBRST#
A20GATE
IRRX
IRTX
RXD0
TXD0
DSR#0
RTS#0
CTS#0
DTR#0
RI#0
DCD#0
RXD1
TXD1
DSR#1
RTS#1
CTS#1
DTR#1
RI#1
DCD#1
DRVDEN#1
DRVDEN#0
MTR#0
DS#0
DIR#
STEP#
WDATA#
WGATE#
HDSEL#
INDEX#
TRK#0
WRTPRT#
RDATA#
DSKCHG#
SIO_14MHZ
PAR_INIT#
SLIN#
PDR[7:0]
PDR7
PDR6
PDR5
PDR4
PDR3
PDR2
PDR1
PDR0
SLCT#
PE
BUSY
ACK#
ERROR#
ALF#
STROBE#
AFD#
STB#
FAN2/GP32
FAN1/GP33
PWM2
PWM1
FDC_PP/DDRC/GP43
GP60/LED1
GP61/LED2
GP27/IO_SMI#
GP30/FAN_TACH2
GP31/FAN_TACH1
GP25/MIDI_IN
GP26/MIDI_OUT
GP10/J1B1
GP11/J1B2
GP12/J2B1
GP13/J2B2
GP14/J1X
GP15/J1Y
GP16/J2X
GP17/J2Y
GP20/P17
GP21/P16
GP22/P12
GP24/SYSOPT
LPC_SMI#
CPU_TACH2
CPU_TACH1
MIDI_IN
MIDI_OUT
J1BUTTON1
J1BUTTON2
J2BUTTON1
J2BUTTON2
JOY1X
JOY1Y
JOY2X
JOY2Y
KEYLOCK#
SYSOPT
Pulldown on SYSOPT for IO address of 0x02E
LPC header. For debug only.
J20
MULT1_GPIO
SERIRQ
VCC5_KBMS_J
VCC5
VCC3_3
R315
4.7K
RP5
R157
R313
C309
C348
C321
C313
C323
C349
0.1UF
2.2UF
Place next to VREF.
Place decoupling caps near each power pin.
C320
C317
470PF
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
SUPER I/O
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-29-1999 14:46
SHEET: 14 OF 38

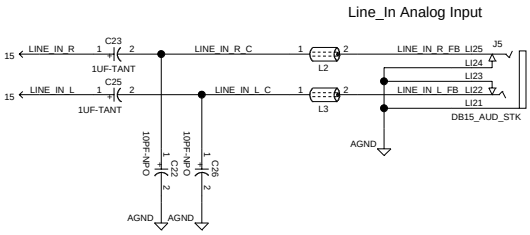
AC'97 Audio

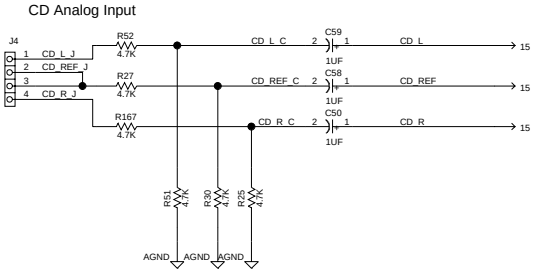


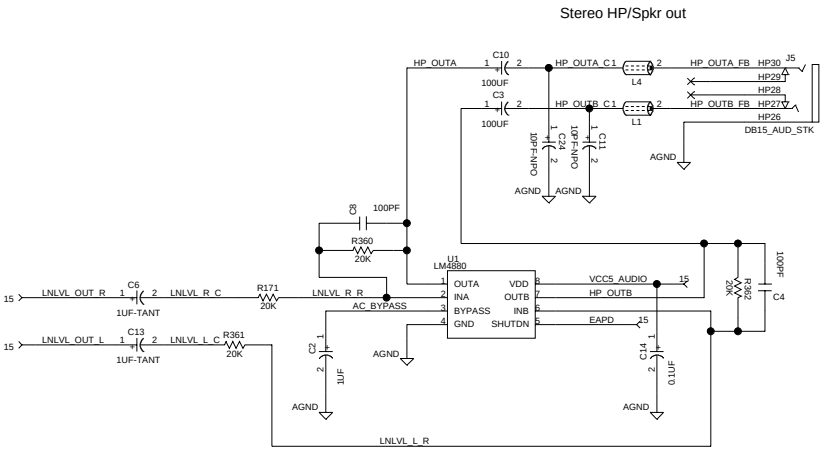
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03			
AUDIO			
intel	PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
		LAST REVISED: 11-29-1999 14:46	SHEET: 15 OF 38

AC'97 Audio



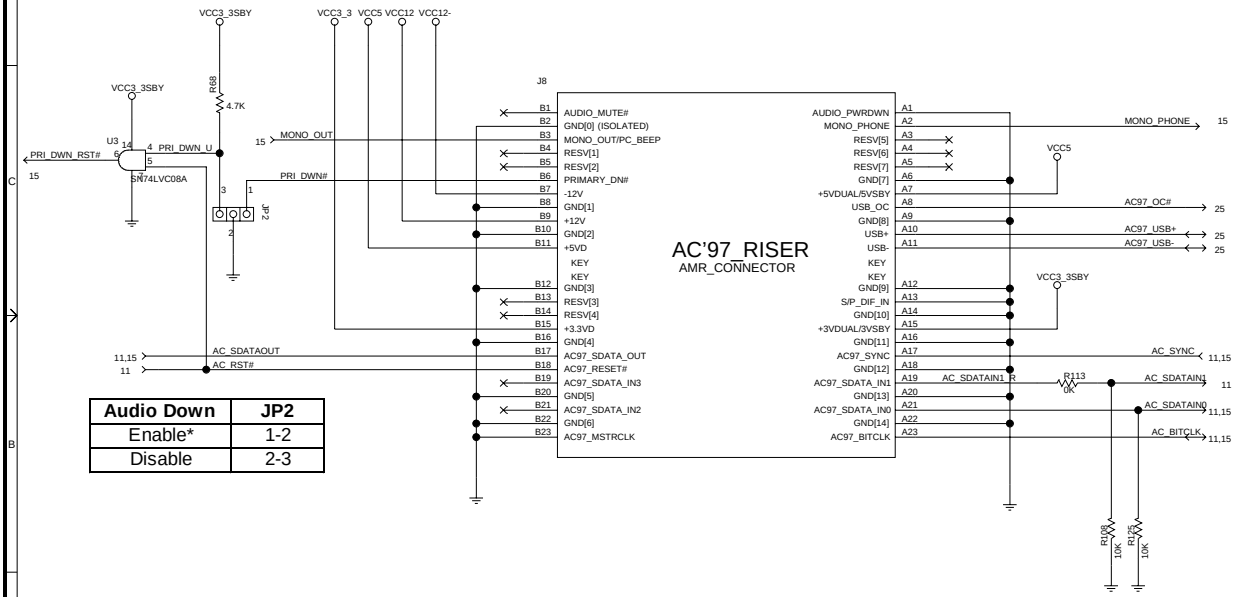






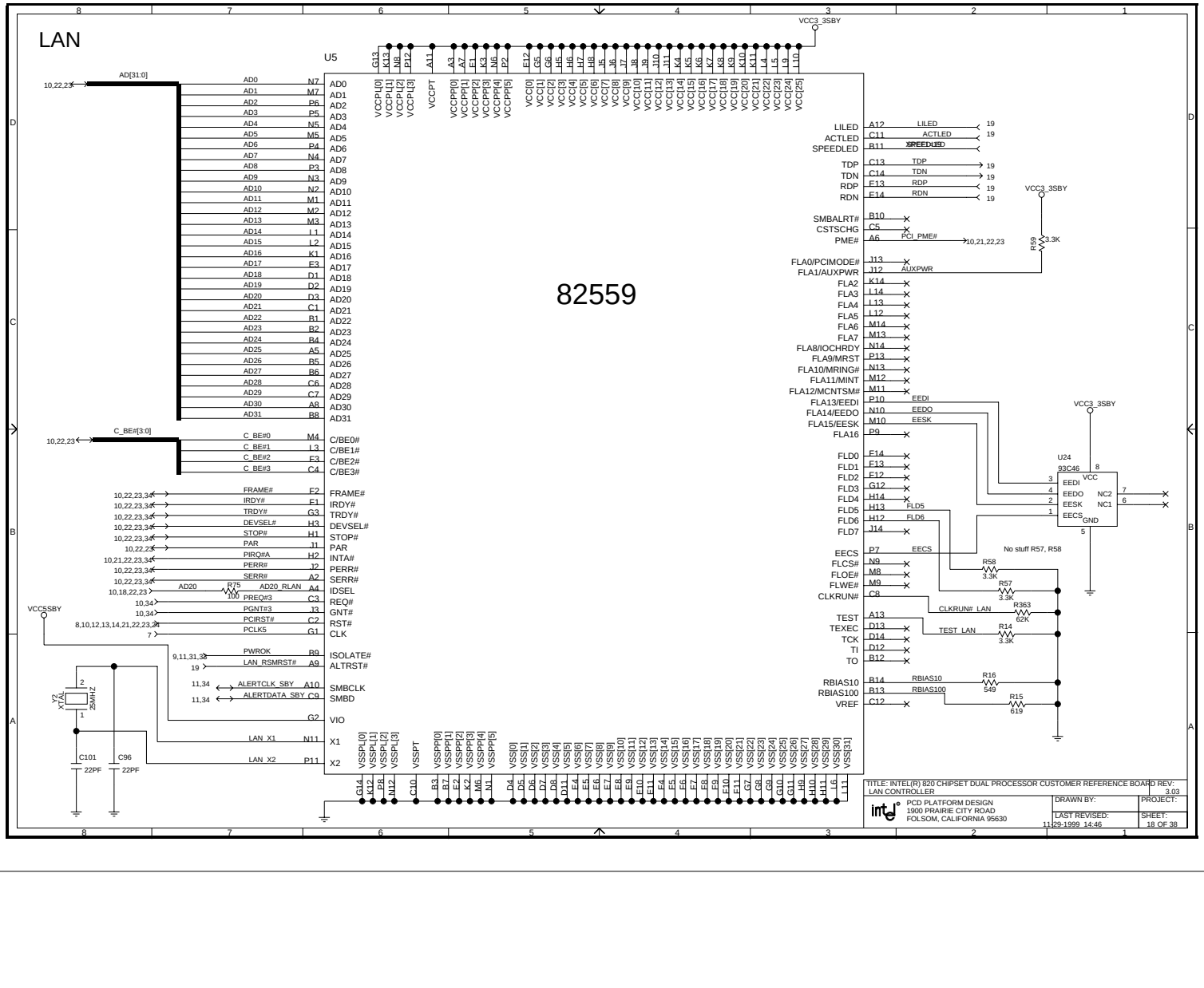
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03		
AUDIO		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 16 OF 38

AC’97 Audio/Modem Riser

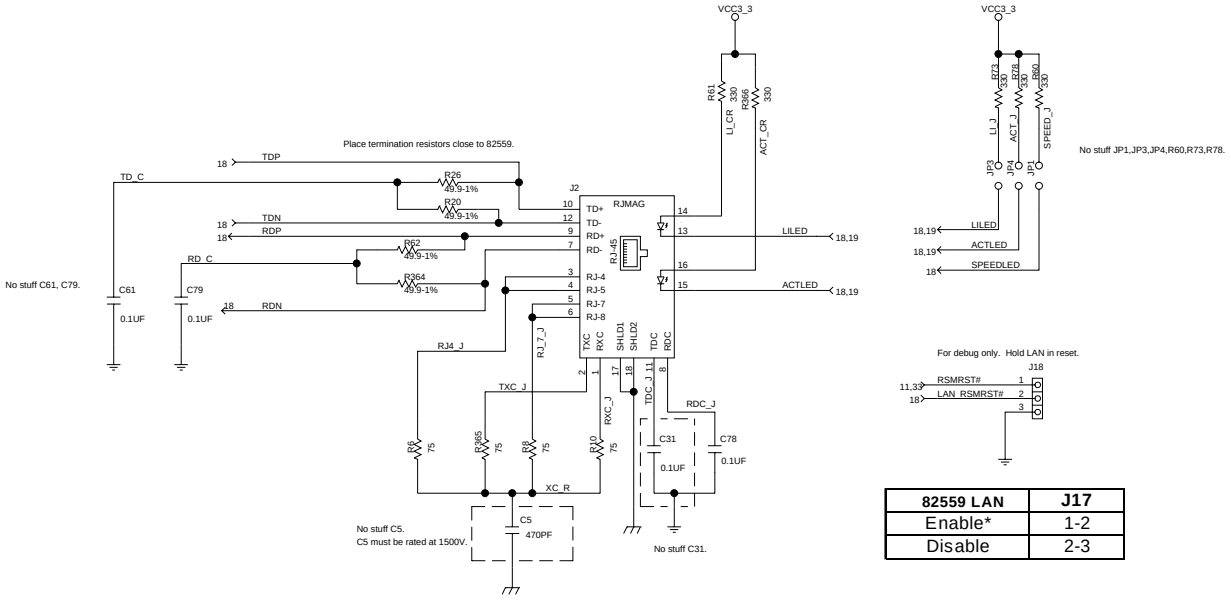


Audio Down	JP2
Enable*	1-2
Disable	2-3

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 AUDIO/MODEM RISER		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: LAST REVISED:	PROJECT: SHEET: 17 OF 38


LAN
U5
82559
VCC3_3SBY
AD[31:0]
C_BE#[3:0]
VCC5SBY
LILED
ACTLED
SPEEDLED
TDP
TDN
RDP
RDN
SMBALRT#
CSTSCHG
PME#
FLA0/PCIMODE#
FLA1/AUXPWR
FLA2
FLA3
FLA4
FLA5
FLA6
FLA7
FLA8/IOCHRDY
FLA9/MRST
FLA10/MRING#
FLA11/MINT
FLA12/MCNTSM#
FLA13/EEDI
FLA14/EEDO
FLA15/EESK
FLA16
FLD0
FLD1
FLD2
FLD3
FLD4
FLD5
FLD6
FLD7
EECS
FLCS#
FLOE#
FLWE#
CLKRUN#
TEST
TEXEC
TCK
TI
TO
RBIAS10
RBIAS100
VREF
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PAR
PIRQ#A
PERR#
SERR#
AD20
AD20_RLAN
PREQ#3
PGNT#3
PCIRST#
PCLK5
PWROK
LAN_RSMRST#
ALERTCLK_SBY
ALERTDATA_SBY
LAN_X1
LAN_X2
C101
22PF
C96
22PF
Y2
XTAL
25MHZ
R59
3.3K
R58
3.3K
R57
3.3K
R363
62K
R14
3.3K
R16
549
R15
619
No stuff R57, R58
CLKRUN# LAN
TEST_LAN
U24
93C46
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
LAN CONTROLLER
PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PROJECT:
LAST REVISED: 11-29-1999 14:46
SHEET: 18 OF 38

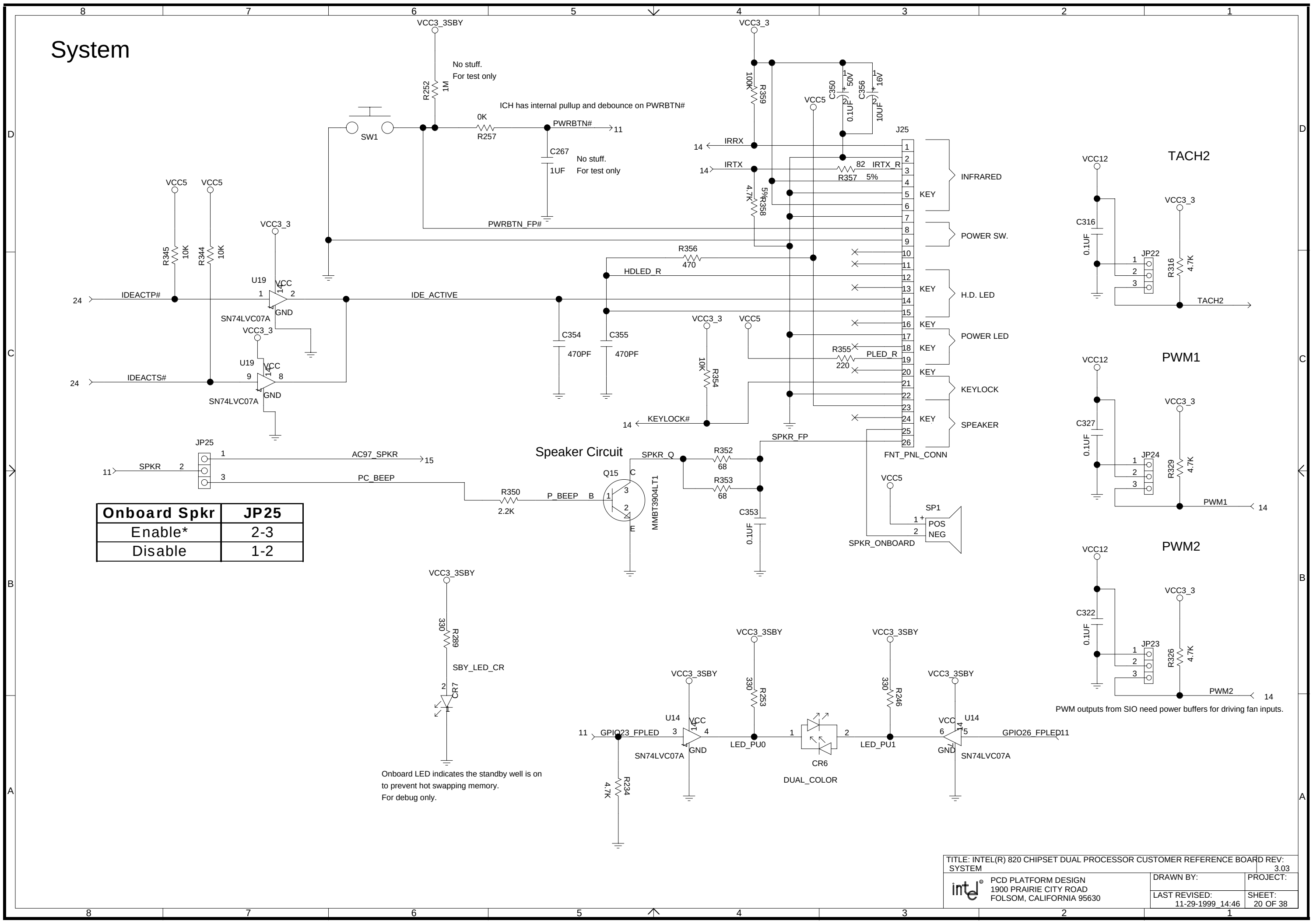
LAN



82559 LAN	J17
Enable*	1-2
Disable	2-3

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 LAN		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 19 OF 38

System



Onboard Spkr	JP25
Enable*	2-3
Disable	1-2

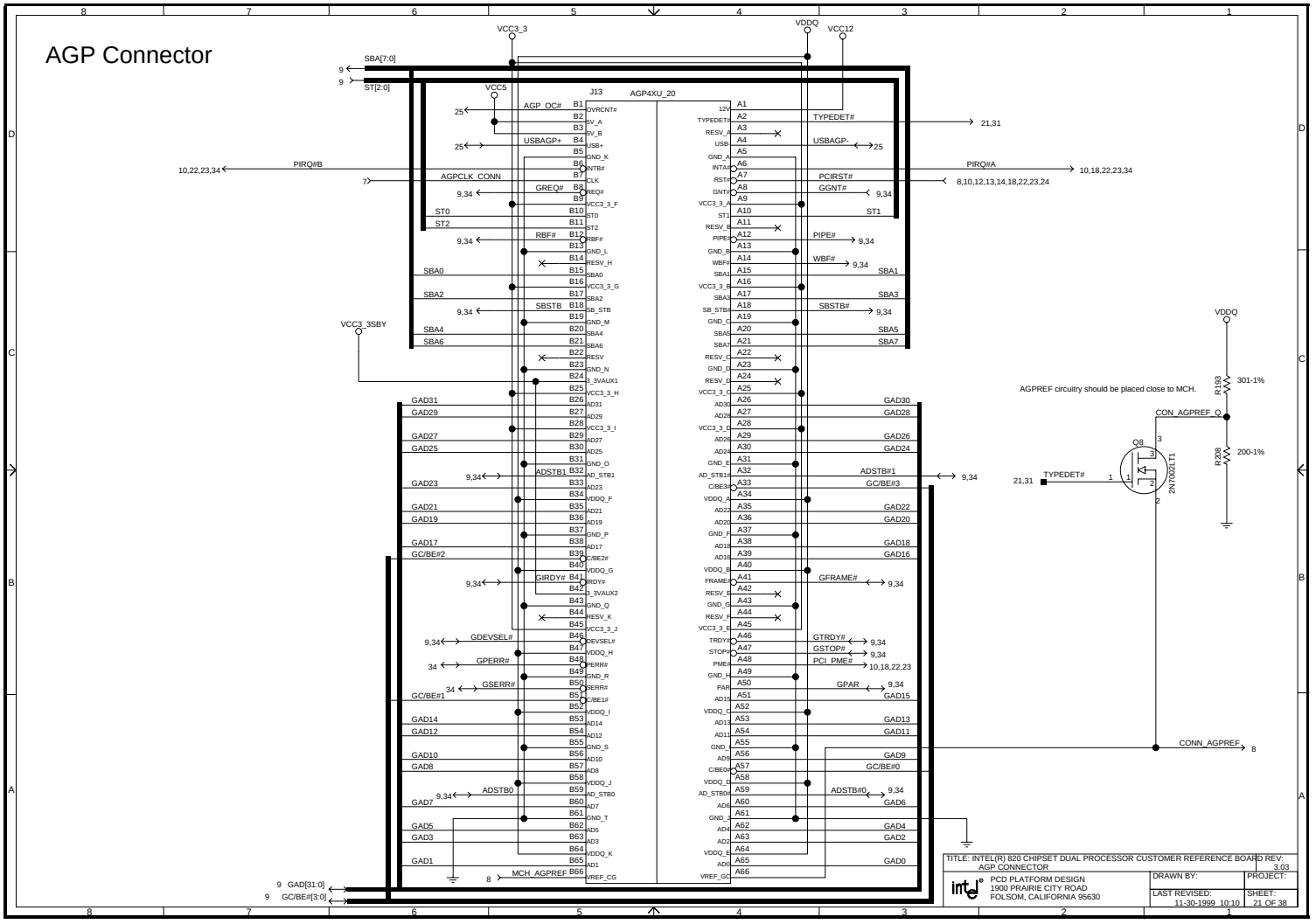
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
SYSTEM

intel® PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

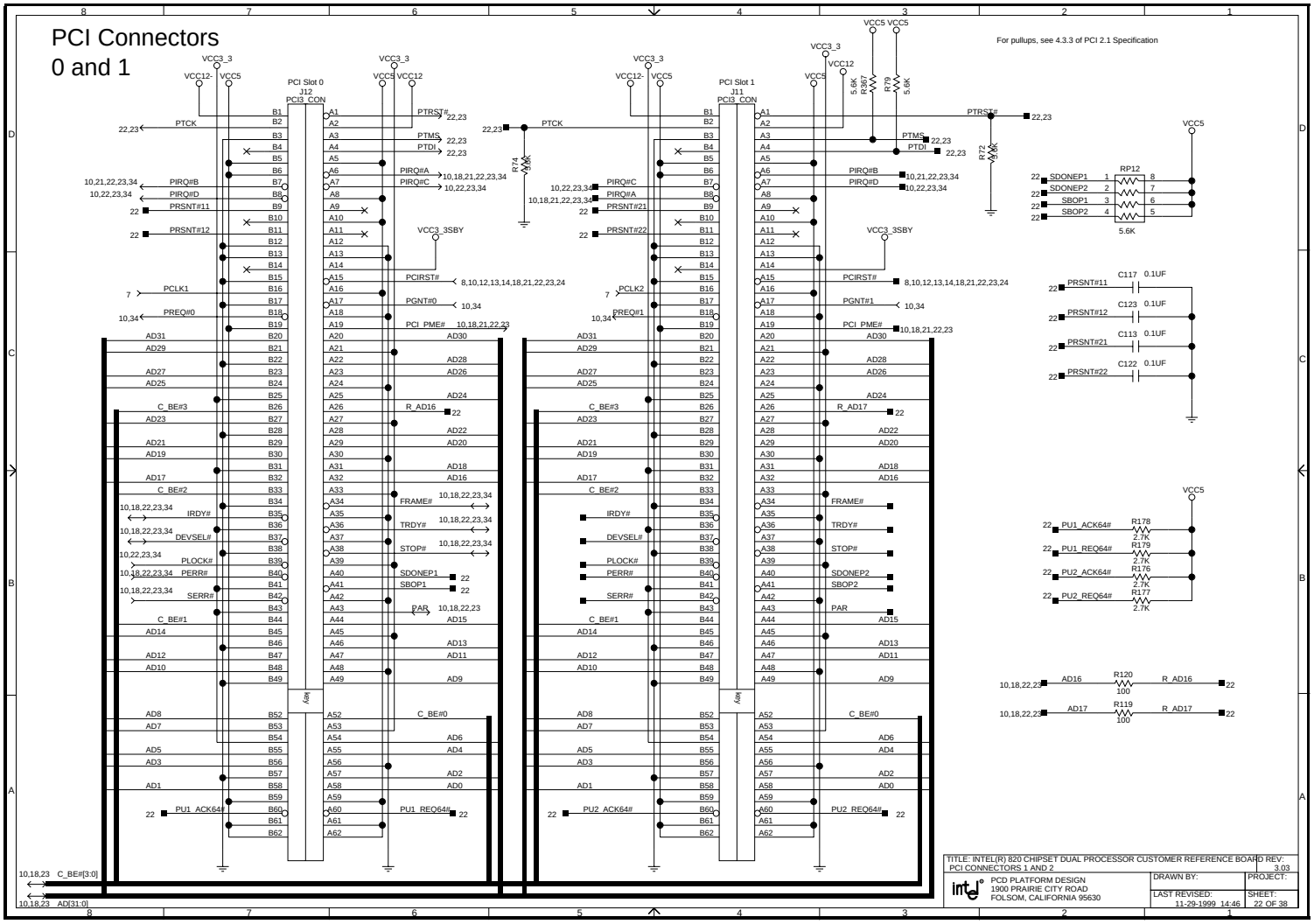
DRAWN BY: PROJECT:

LAST REVISED: 11-29-1999_14:46 SHEET: 20 OF 38

AGP Connector



PCI Connectors 0 and 1

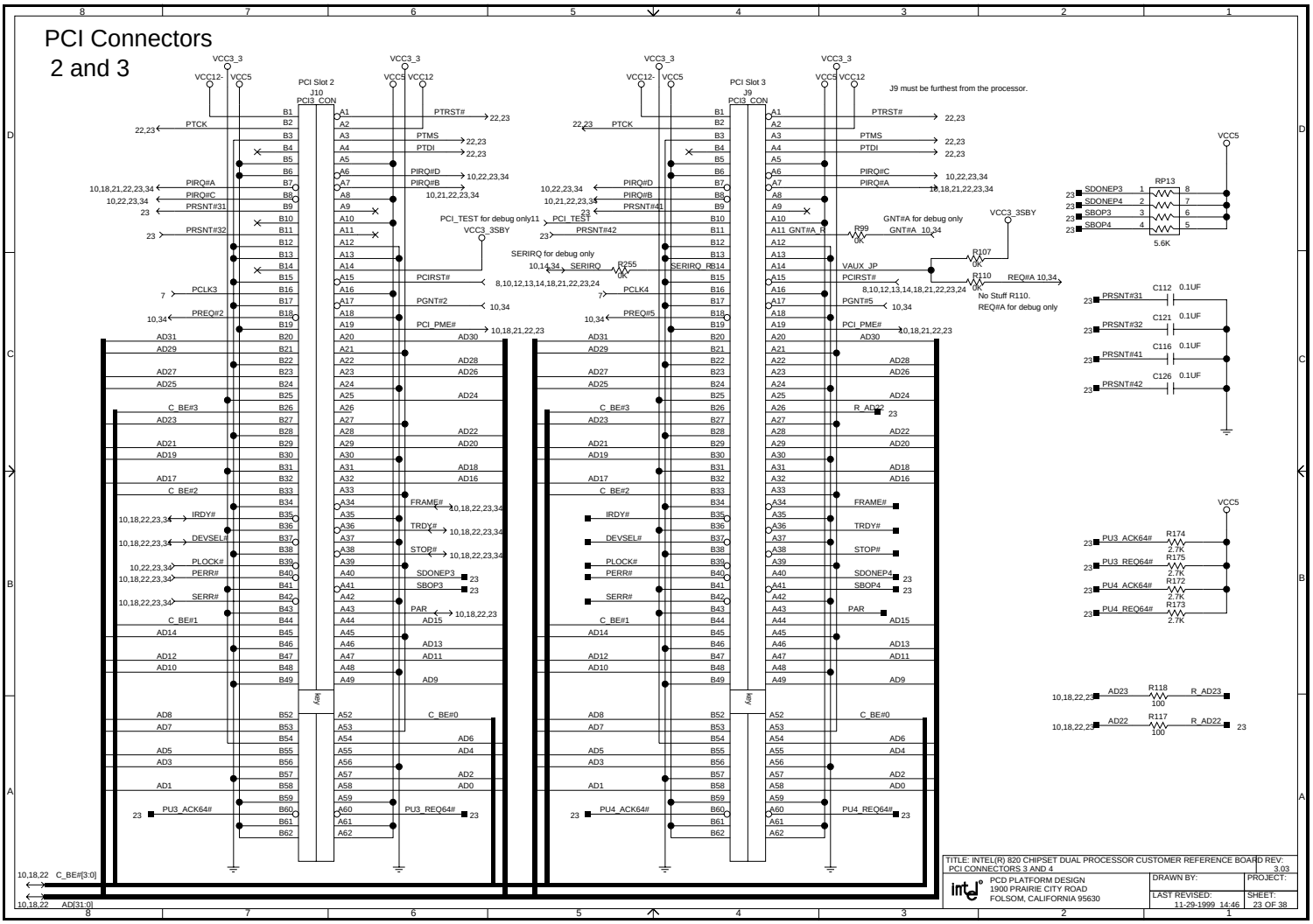


TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
PCI CONNECTORS 1 AND 2

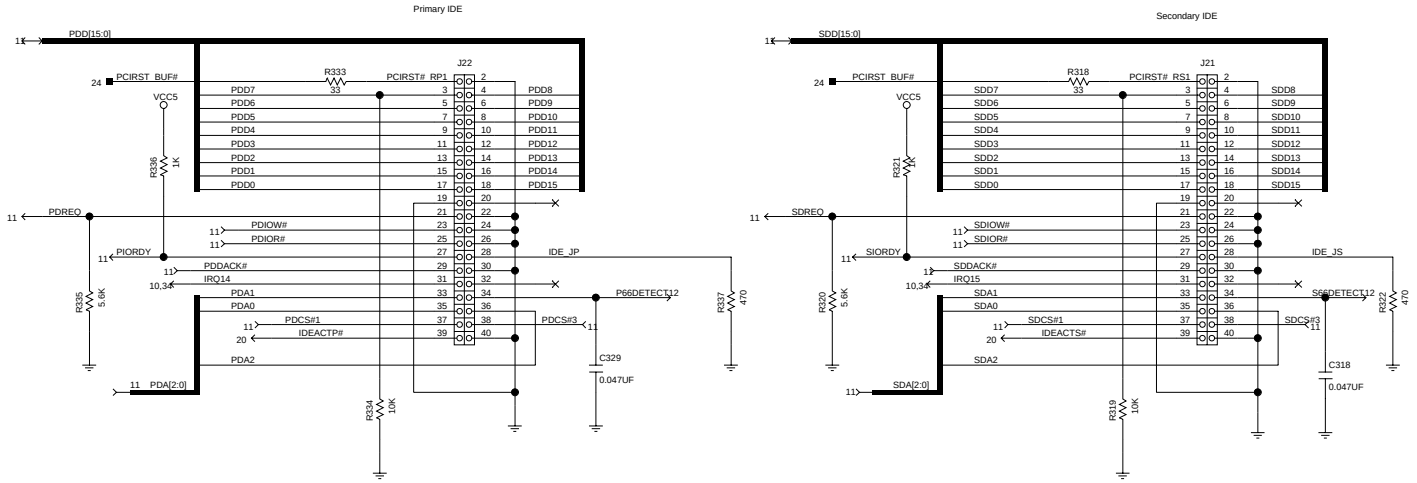
intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY: | PROJECT:
LAST REVISED: 11-29-1999 14:46 | SHEET: 22 OF 38

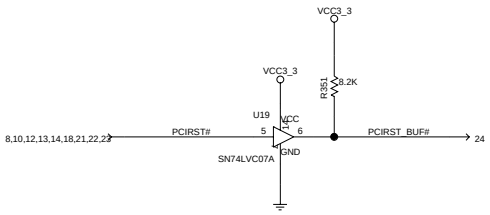
PCI Connectors 2 and 3



IDE Connectors

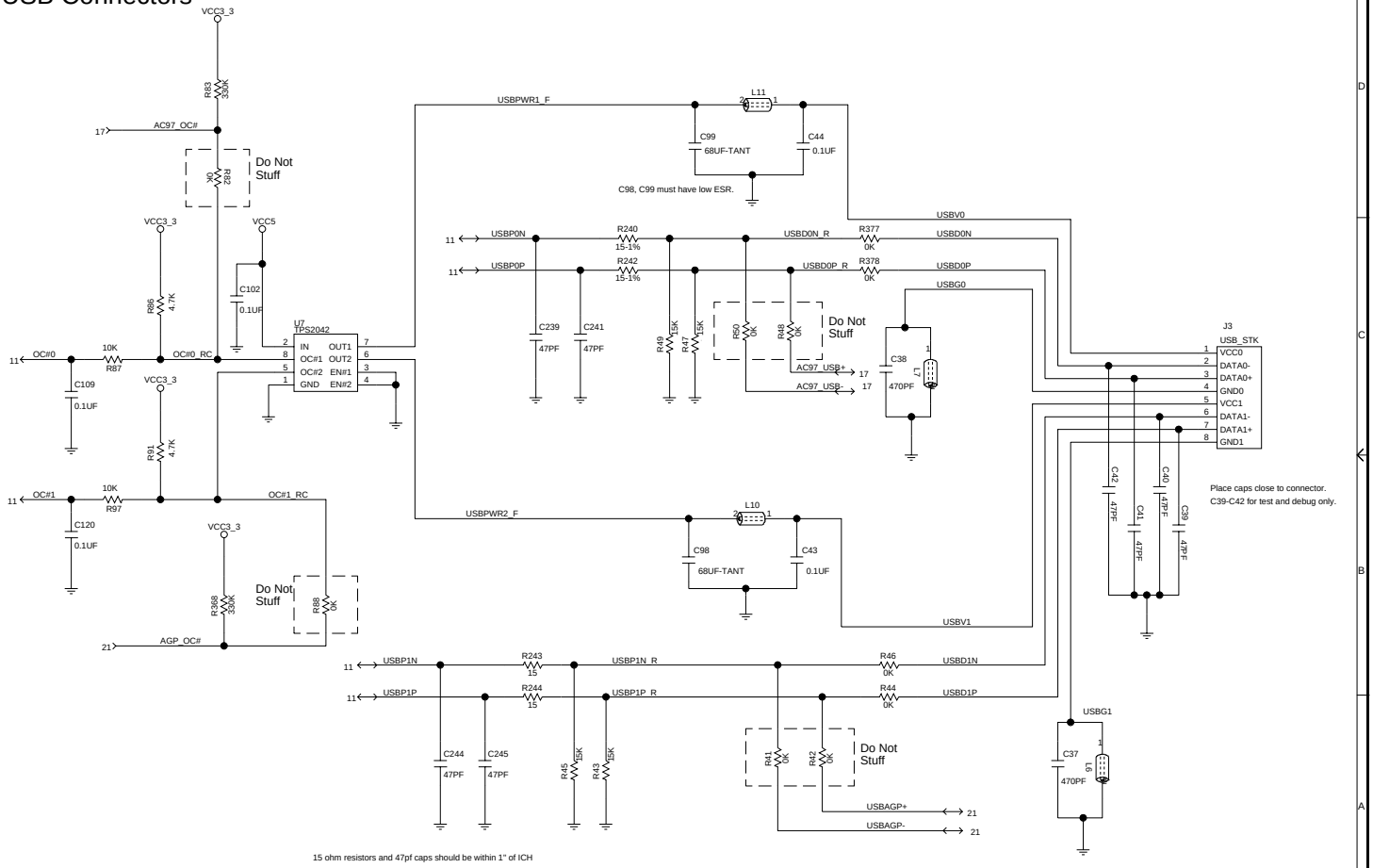


For drive side detection, stuff C329,C318.
For host side detection, no stuff C329,C318.
P66DETECT and S66DETECT can be connected to a GPI for BIOS cable detection.



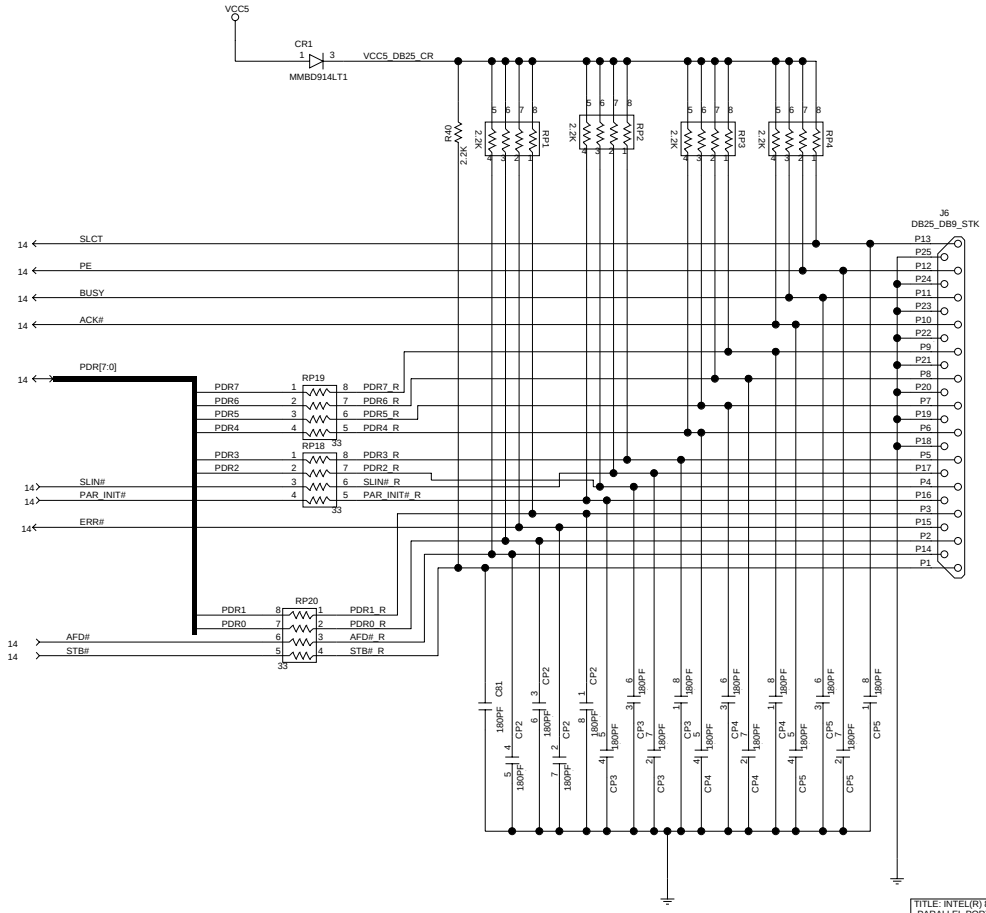
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 IDE CONNECTORS		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 24 OF 38

USB Connectors



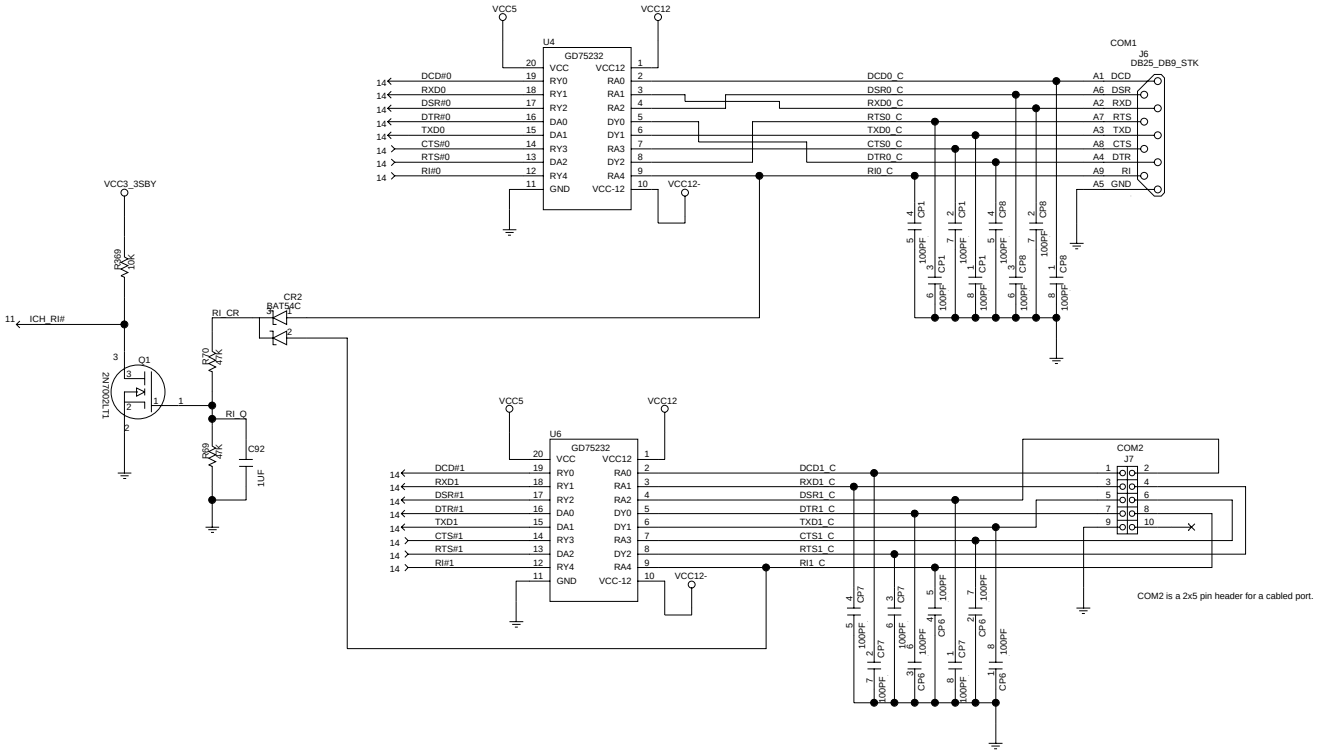
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 USB CONNECTORS		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 25 OF 38

Parallel Port



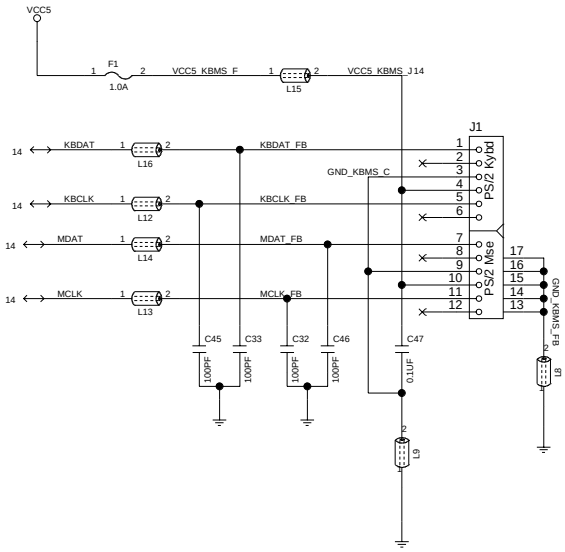
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 PARALLEL PORT		
intel® PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 26 OF 38

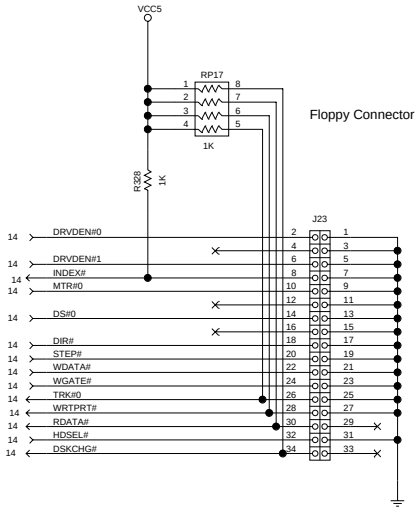
Serial Ports



TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 SERIAL PORTS		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 27 OF 38

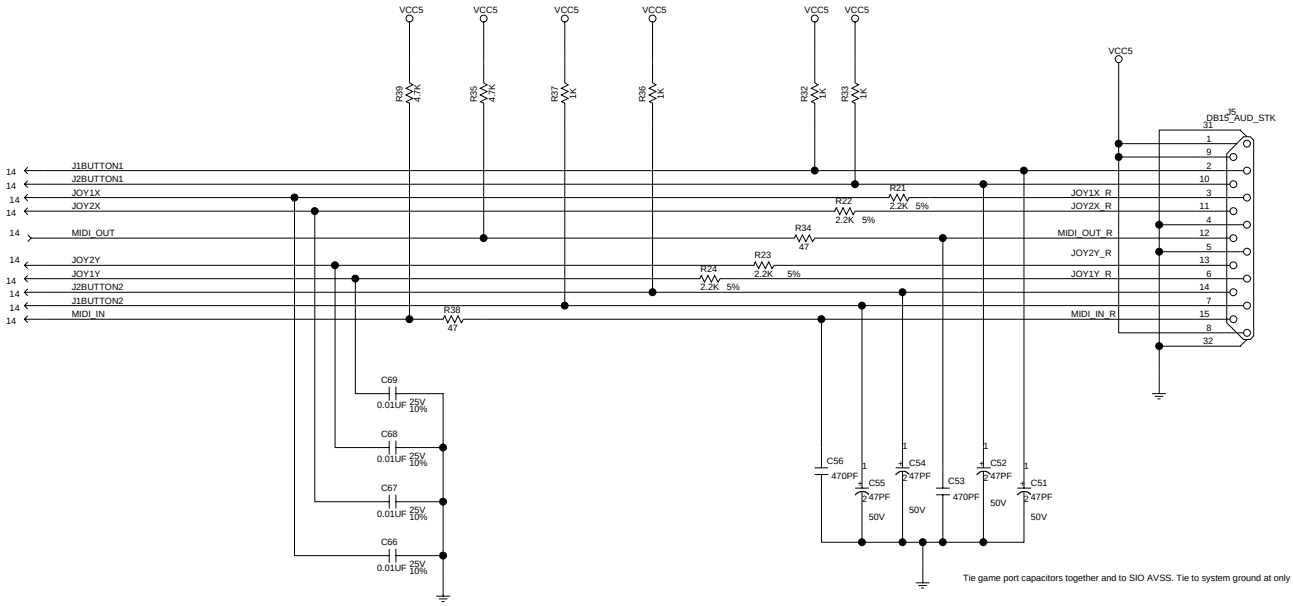
Keyboard/Mouse/Floppy





TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 KEYBOARD/MOUSE/FLOPPY		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 28 OF 38

Game Port

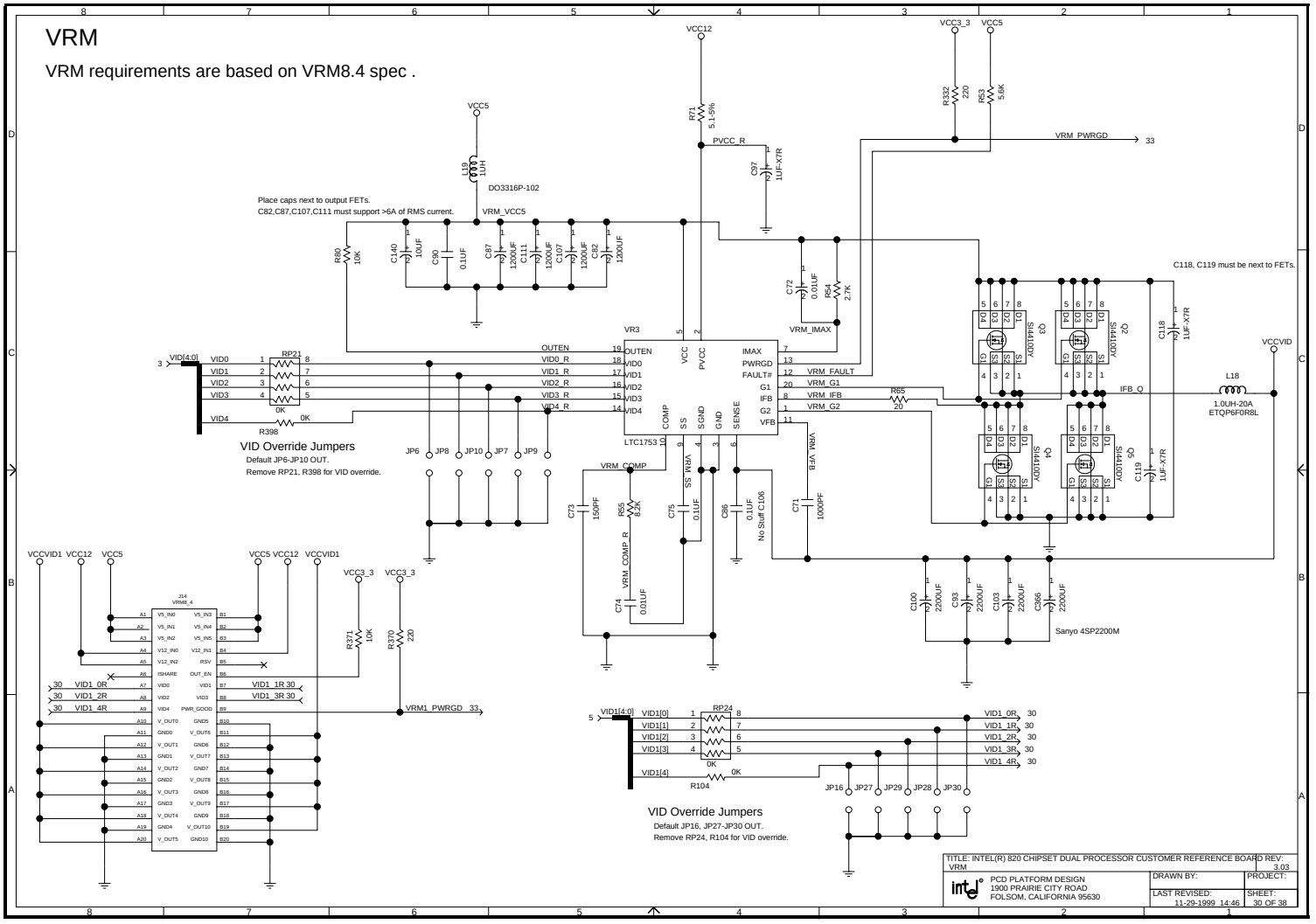


Tie game port capacitors together and to SIO AVSS. Tie to system ground at only a single point.

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 GAME PORT			
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:	
	LAST REVISED:	SHEET: 29 OF 38	

VRM

VRM requirements are based on VRM8.4 spec .



TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
VRM

intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

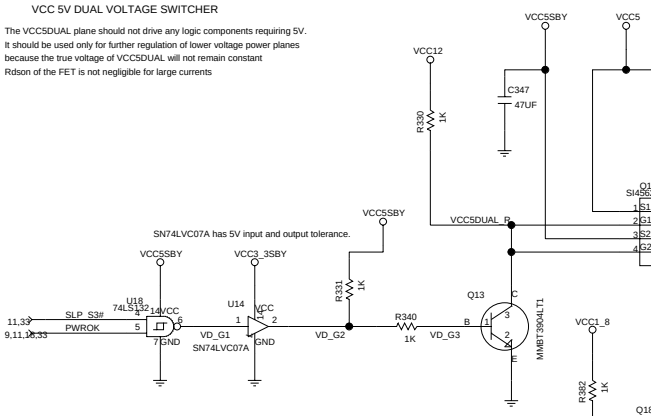
DRAWN BY: | PROJECT:
LAST REVISED: 11-29-1999 14:46 | SHEET: 30 OF 38

Voltage Regulators

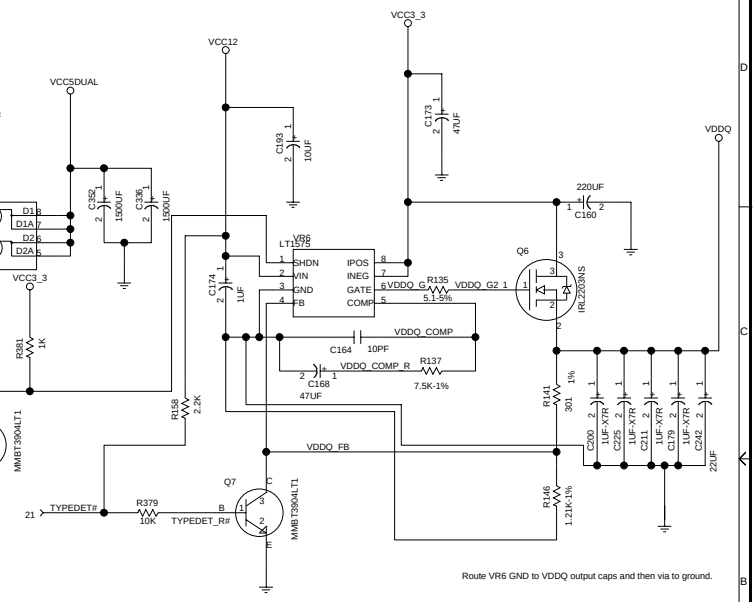
VCC 5V DUAL VOLTAGE SWITCHER

The VCC5DUAL plane should not drive any logic components requiring 5V.
It should be used only for further regulation of lower voltage power planes
because the true voltage of VCC5DUAL will not remain constant
Rdson of the FET is not negligible for large currents

SN74LVC07A has 5V input and output tolerance.

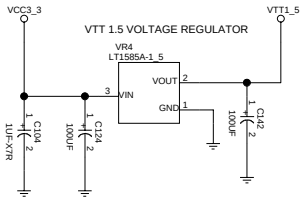


AGP VDDQ VOLTAGE REGULATOR

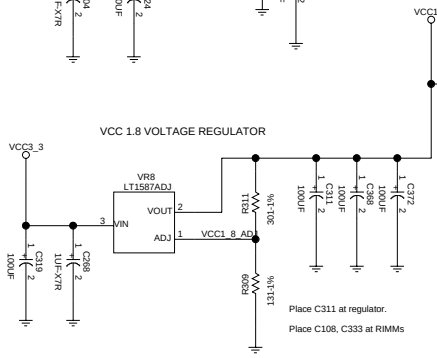


Route VR6 GND to VDDQ output caps and then via to ground.

VTT 1.5 VOLTAGE REGULATOR



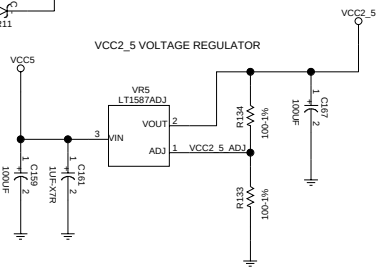
VCC 1.8 VOLTAGE REGULATOR



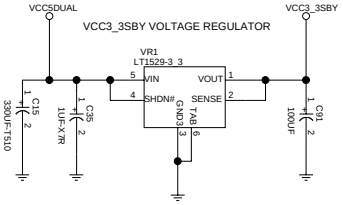
Place C311 at regulator.

Place C108, C333 at RIMMs

VCC2_5 VOLTAGE REGULATOR

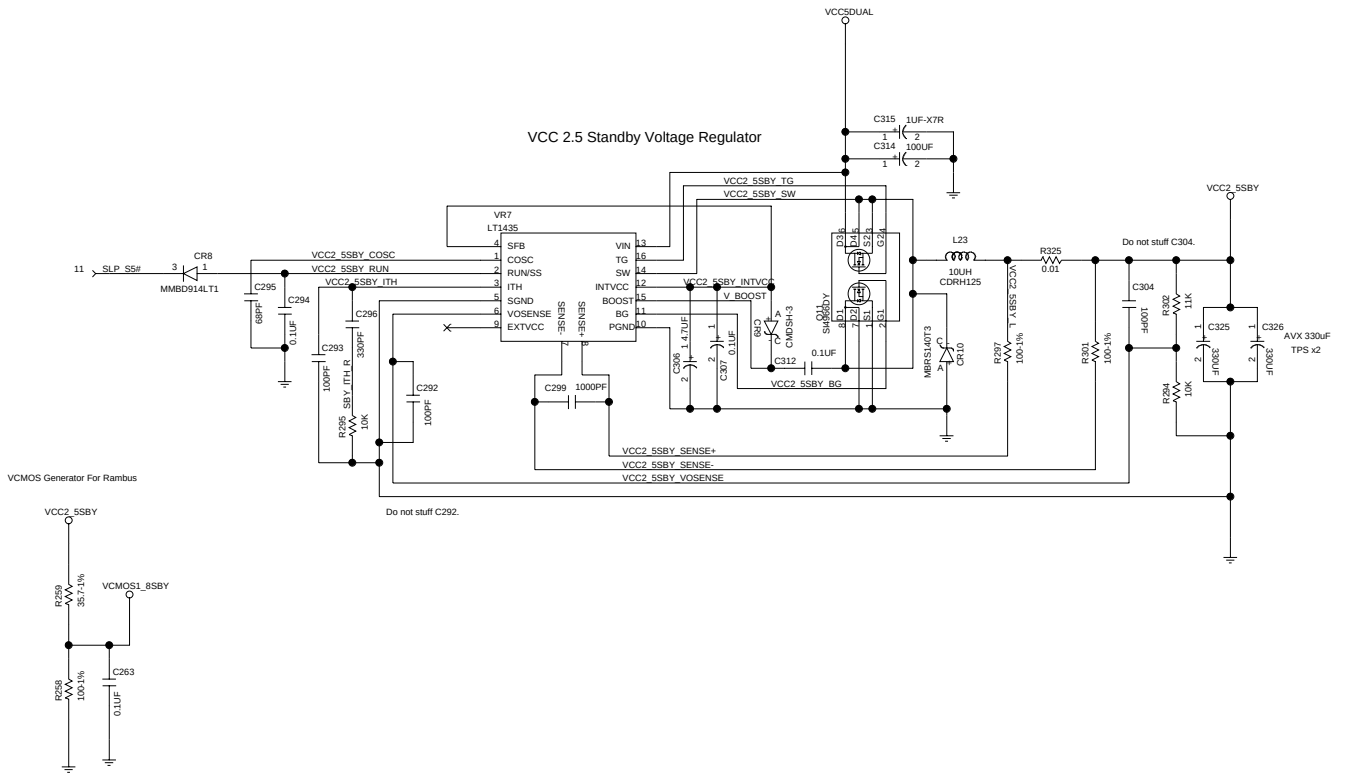


VCC3_3SBY VOLTAGE REGULATOR



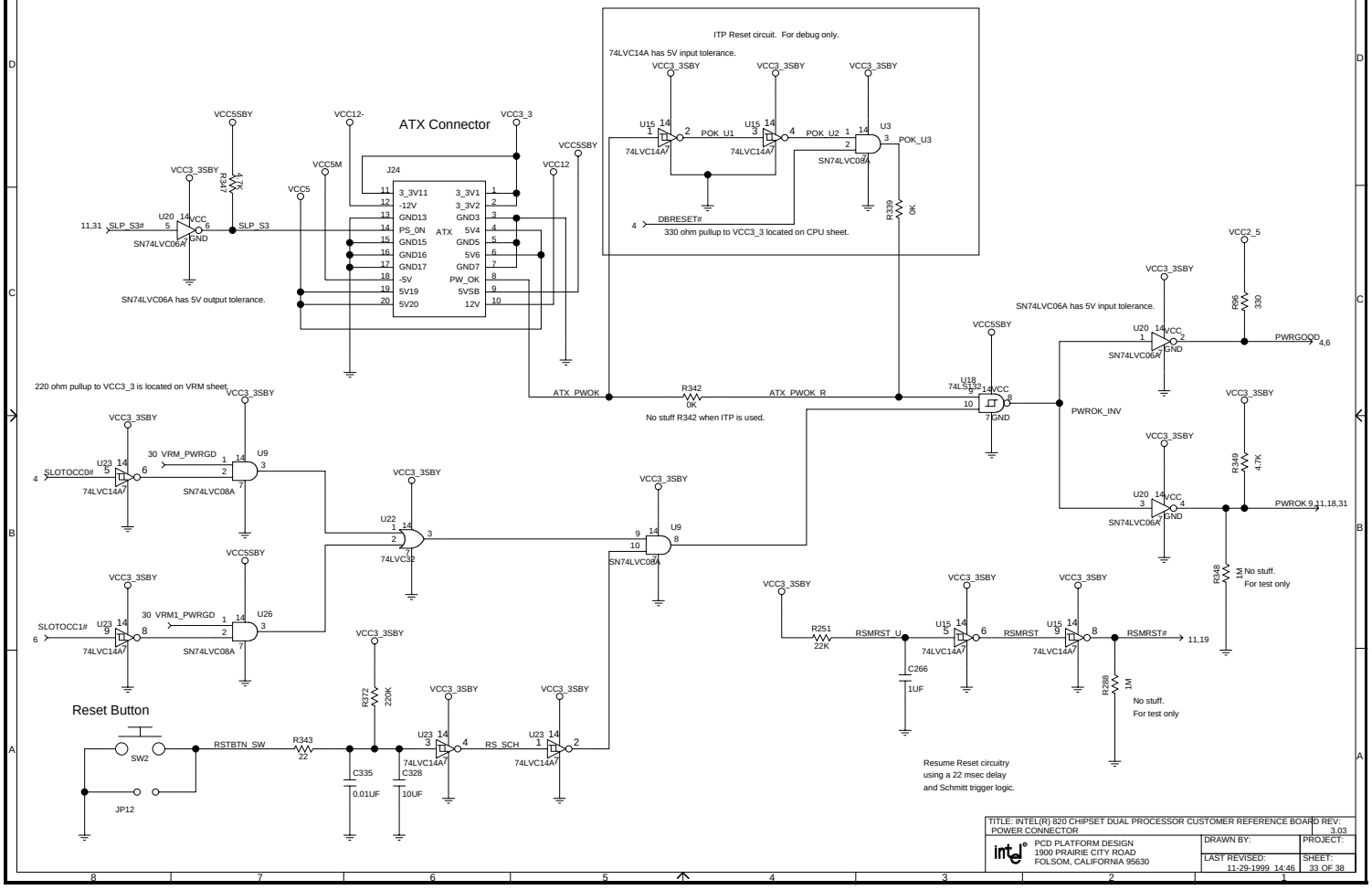
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD VOLTAGE REGULATORS		REV: 3.03
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 31 OF 38

Voltage Regulators



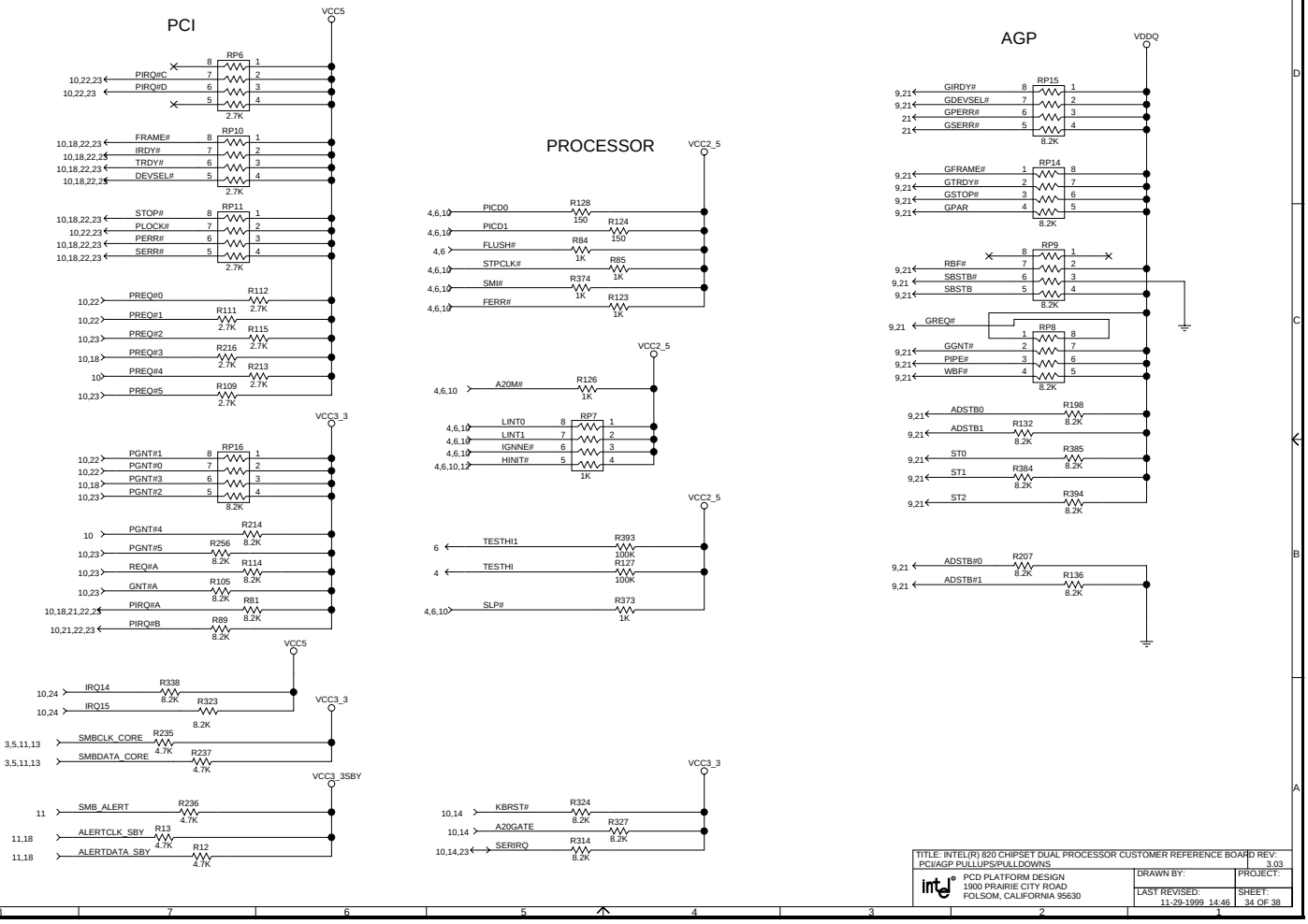
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 VOLTAGE REGULATORS		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 32 OF 38

Power Connector



TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 POWER CONNECTOR		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 33 OF 38

PCI/AGP Pullups/Pulldowns

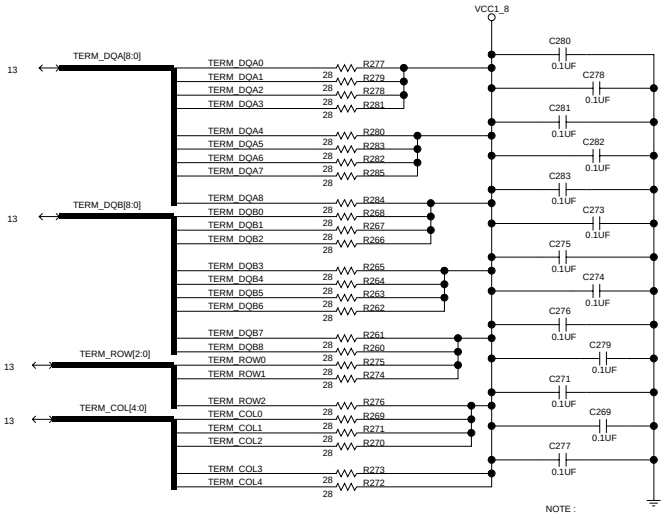


TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03
PCI/AGP PULLUPS/PULLDOWNS

intel PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

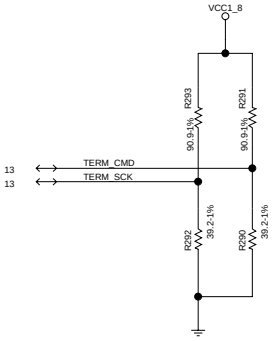
DRAWN BY: | PROJECT:
LAST REVISED: 11-29-1999 14:46 | SHEET: 34 OF 38

Rambus Termination



NOTE :

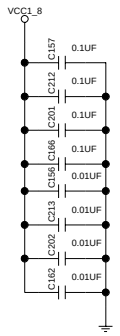
Use one 0.1uF cap
per two RSL signals.



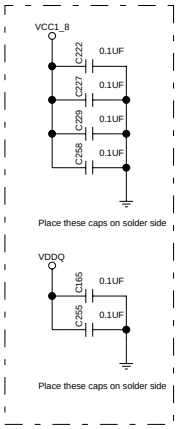
TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD RAMBUS TERMINATION		REV: 3.03
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:46	SHEET: 35 OF 38

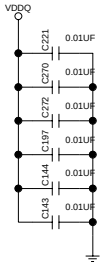
Decoupling

MCH Decoupling



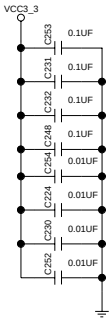
For chipset decoupling, use 0.1UF and 0.01UF decoupling capacitor at each corner of the device. If there is room, add 0.01UF capacitors in the middle of each quad.



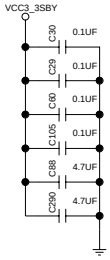


Place VDDQ capacitors within 70 mils of outer balls of MCH.

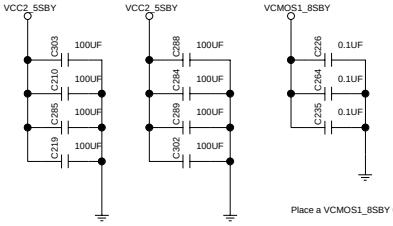
ICH Decoupling



82559 Decoupling.



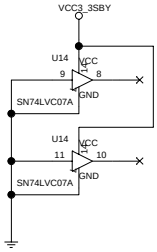
RIMM Decoupling

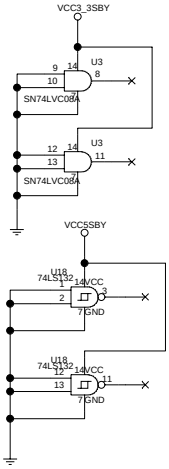


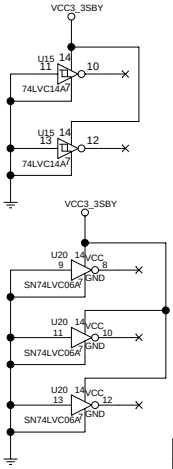
Place 100uF caps, 0.1 ohm ESR, among RIMM connectors.

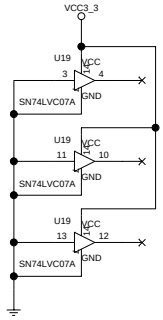
Place a VCMOS1_8SBY 0.1uF cap at each RIMM.

Un-used Gates



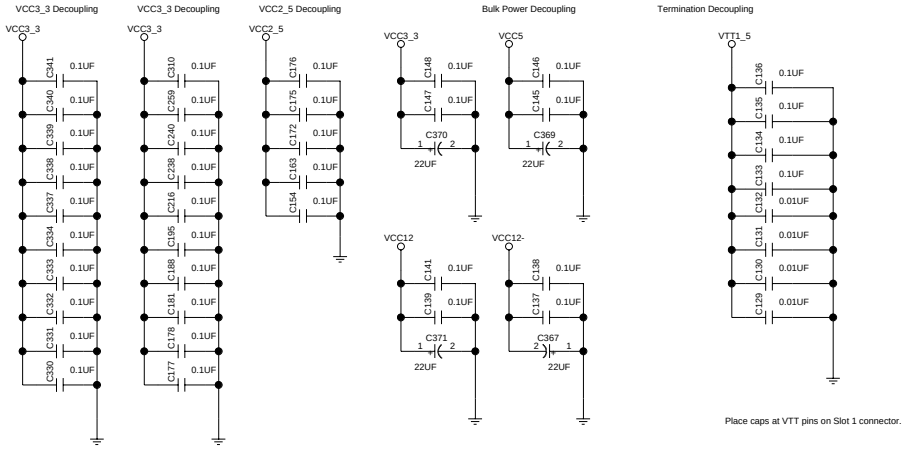


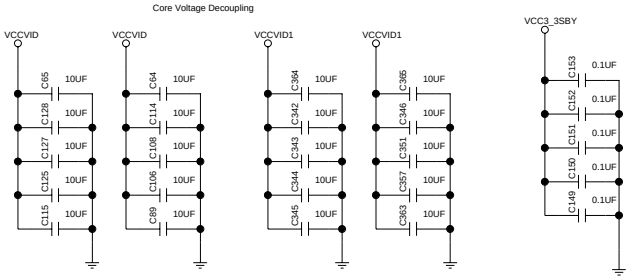




TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REV: 3.03 DECOUPLING		
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:44	SHEET: 36 OF 38

Bulk Decoupling





TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD BULK DECOUPLING		REV: 3.03
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:44	SHEET: 37 OF 38

Revision History

Pg 8 Modified MCH_AGPREF circuit, changed 432 ohm to 1K ohm and 62 ohm to 80.6 ohm.
Changed value of capacitor C194 from 0.1uF to 0.01uF.

Pg 10 Modified HUBREF circuit, deleted R222, R223 & C217, changed C218 from 470pF to 0.1uF.

Pg 13 Modified RIMM connectors to eliminate 3.3V, added 0.1uF decoup caps to SVDDA & SVDDB on each RIMM.

Pg 35 Modified CMD and SCK termination values. Removed 470pF capacitors, Changed 93 ohm to 90.9 ohm,
and changed 39 ohm to 39.2 ohm resistors.

Pg 36 Deleted 3.3V decoupling for RIMM connectors. Added solder side decoup for MCH.
Changed VDDQ cap values from 0.1uF to 0.01uF.

TITLE: INTEL(R) 820 CHIPSET DUAL PROCESSOR CUSTOMER REFERENCE BOARD REVISION HISTORY		REV: 3.03
intel PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	PROJECT:
	LAST REVISED: 11-29-1999 14:44	SHEET: 38 OF 38

Intel around the world

United States and Canada
Intel Corporation
Robert Noyce Building
2200 Mission College Boulevard
P.O. Box 58119
Santa Clara, CA 95052-8119
USA
Phone: (800) 628-8686

Europe
Intel Corporation (UK) Ltd.
Pipers Way
Swindon
Wiltshire SN3 1RJ
UK

Phone:

England	(44) 1793 403 000
Germany	(49) 89 99143 0
France	(33) 1 4571 7171
Italy	(39) 2 575 441
Israel	(972) 2 589 7111
Netherlands	(31) 10 286 6111
Sweden	(46) 8 705 5600

Asia-Pacific
Intel Semiconductor Ltd.
32/F Two Pacific Place
88 Queensway, Central
Hong Kong, SAR
Phone: (852) 2844 4555

Japan
Intel Kabushiki Kaisha
P.O. Box 115 Tsukuba-gakuen
5-6 Tokodai, Tsukuba-shi
Ibaraki-ken 305
Japan
Phone: (81) 298 47 8522

South America
Intel Semicondutores do Brazil
Rue Florida, 1703-2 and CJ22
CEP 04565-001 Sao Paulo-SP
Brazil
Phone: (55) 11 5505 2296

For more information
To learn more about Intel Corporation, visit our site on the World Wide Web at www.intel.com