DUAL-BAND 0033 PLANAR

Antenna Layout Guide

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INTRODUCTION

This document provides guidance for creating the layout for the Dual-band 0033 Planar Antenna. It is critical that CEL reviews the layout prior to release for fabrication.

GENERAL RF GUIDELINES

1. To maintain a characteristic impedance of 50 Ohm on RF traces:
    a. Route RF traces on the same layer as the components. Because most RF components are mounted on the top or bottom layer of the PCB, RF traces should also be routed on the same layer.
    b. Maintain a continuous ground plane directly beneath RF traces.
    c. Maintain ground copper clearance at least one RF trace width away from the RF trace.
    d. Keep RF traces at least one RF trace width away from board edges and/or cutouts.
    e. Check for open stubs, particularly when bypassing a circuit.
    f. Maintain a short, smooth and neat path for RF traces.
    g. If bends are required, use mitered or arc bends. Do not use right-angle bends.
    h. Avoid width discontinuities owing to component pads in the RF trace.
    i. If trace width discontinuities cannot be avoided, miter or taper the trace width to ensure a smooth transition from the smaller to the larger width.
    j. Avoid use of thermal reliefs on RF traces.
    k. To maintain adequate isolation from RF traces.
    l. Route traces that carry other digital and analog signals away from the RF trace and its ground reference.
    m. Maintain as much separation between the traces associated with RF input and RF output as the design permits.
    n. Maintain a via fence around the RF traces to minimize unintentional radiated emissions.

GROUND LAYOUT

2. To maintain a good ground layout:
    a. Ensure that the layer directly adjacent to the layer that contains RF traces has a continuous ground plane. Because most RF components are mounted on the top or bottom layer of the PCB with RF traces routed on the same layer, the ground directly beneath the traces must be continuous.
    b. Ensure at least one via that stitches ground planes on as many layers as possible is placed as close as possible to each component pad that connects to ground.
    c. Maintain a via fence along the perimeter of the board to minimize unintentional radiated emissions.
    d. Use stitching vias in non-RF areas to ensure that the grounds on all layers are tied.

POWER LAYOUT

3. To maintain good power layout:
    a. Use at least one decoupling capacitor on the power supply input to the module. It is recommended that the required bulk capacitance value of at least 4.7 µF capacitor is chosen.
    b. Optionally, a second decoupling capacitor with a capacitance that is an order of magnitude smaller than that of the bulk capacitor can be placed in parallel. The purpose of the capacitor with smaller capacitance is to improve the ability of the capacitor to shunt high frequency noise produced by the module.
    c. Place decoupling capacitors as close to the module input as possible.
    d. Ensure that the trace width of the power supply feeding the module is as wide as the design permits. The purpose of maintaining a wide trace width is to minimize resistance between the power supply and the module.

DIGITAL INTERFACE

4. To maintain good signal integrity on digital interface(s):
    a. Minimize coupling to power planes by keeping high speed digital traces away from power traces.
    b. Minimize coupling to other digital traces by maintaining adequate physical separation between each trace.
    c. Minimize coupling to RF traces by maintaining adequate physical separation between digital and RF traces.

RF TRACE

1. To maintain good RF performance:
    a. Maintain a characteristic impedance of 50 Ohm between the antenna port and the RF port on the stamp module.
    b. Minimize RF trace length to minimize attenuation and phase dispersion.
    c. Minimize discontinuities by routing RF traces on the same layer as the components. Because most RF components are mounted on the top or bottom layer of the PCB, RF traces should also be routed on the same layer.
    d. Avoid changing layers on RF traces using vias.
    e. Use of either ground-backed coplanar waveguide or microstrip structure is recommended for RF traces
    f. Refer to GENERAL RF GUIDELINES section for additional layout guidance.

ANTENNA IMPLEMENTATION EXAMPLE

This section illustrates the step-by-step process of integrating the antenna into an example design.

1. Calculate the required trace width to maintain a 50 Ohm characteristic impedance.
    a. Obtain the board stack up and determine the thickness and relative permittivity of the dielectric between the RF trace and its reference ground(s). Depending on the RF trace structure, the gap between the adjacent ground on the same layer may need to be included in the calculation.

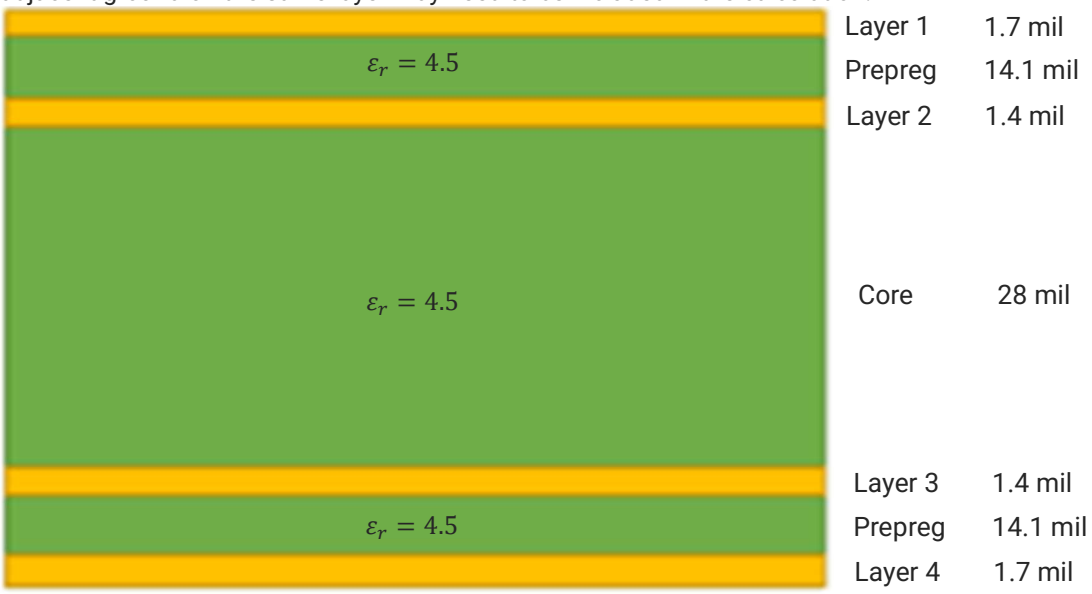

Figure 1. Example of board stackup (not drawn to scale).

In **Figure 1**, an example board stackup is shown. In this example, the module is placed on layer 1. Using the guidelines, the RF trace should be routed on layer 1. The reference ground for the RF trace

is therefore layer 2. There is also going to be a ground pour on the top layer, so there will be a gap between the RF trace and ground pour. This is known as a ground-backed coplanar waveguide (CPWG) construction. The relative permittivity of the dielectric contained between layers 1 and 2 is $\varepsilon_r = 4.5$. The thickness of the dielectric separating layers 1 and 2 is 14.1 mil.

b. Use a characteristic impedance calculator to determine the required trace width based on the stack up and construction of the RF trace.

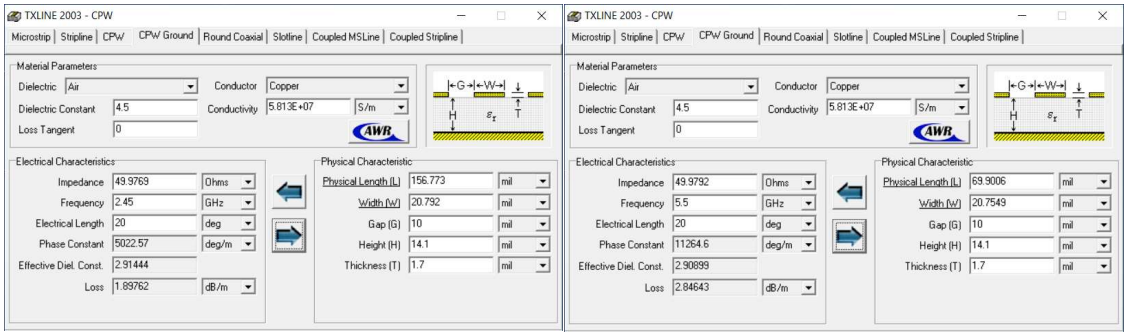

Figure 2. Transmission line calculator to determine the trace width.

In **Figure 2**, an example of a transmission line calculator determining the required trace width to maintain a 50 Ohm characteristic impedance of a CPWG construction is shown. The relative permittivity, frequency, gap, height of the dielectric and thickness of the conductor were entered into the calculator. At both 2.45 GHz and 5.5 GHz, the trace width required to maintain a 50 Ohm characteristic impedance is 20.7 mil. As the impedance is slightly below the desired 50 Ohm characteristic impedance, it is acceptable in this case to round the calculated trace width down to better approximate 50 Ohm characteristic impedance. Therefore, a trace width of 20 mil with a 10-mil gap on either side of the RF trace was chosen.

c. Place the antenna at the center of the longest host board edge. Clear out any conductor(s) directly beneath the antenna. In addition, maintain the board edge-to-copper clearance constraint when placing the antenna.

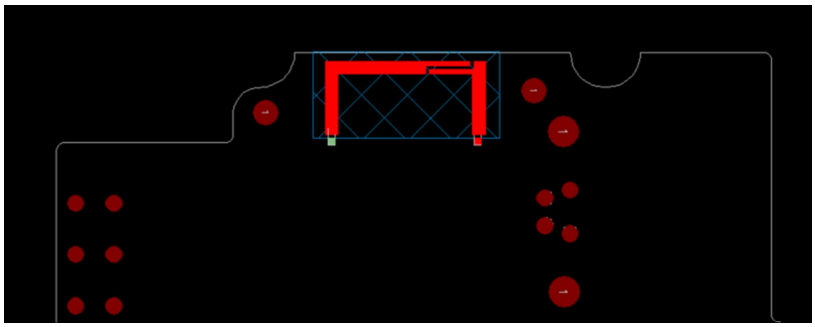

Figure 3. Antenna placement at the center of the longest edge of the host board.

In **Figure 3**, an example is shown of an antenna placement along the side of the longest edge of the host board. Notice that the edge of the antenna closest to the board edge is inset to maintain the board edge-to-copper clearance requirement. A typical board edge-to-copper clearance requirement is 10 mil.

d. Place the impedance matching components starting from the antenna port, running along the bottom edge of the antenna in a manner that produces as few discontinuities as the design permits.

Figure 4. Impedance matching component placement.

In **Figure 4**, an example is shown of the impedance matching component placement, which runs along the bottom edge of the antenna. Ensure that the component pads through which the RF will pass is aligned to minimize discontinuities.

In this example, size 0402 (in) components were spaced as shown in **Figure 5**.

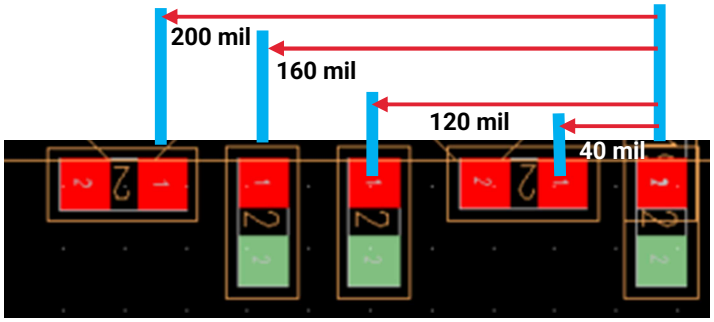

Figure 5. Example of the spacing between each impedance matching component.

e. Route a trace with the width as previously calculated from the input of the impedance matching network to the RF port of the module. Ensure that the RF trace is short, smooth and neat.

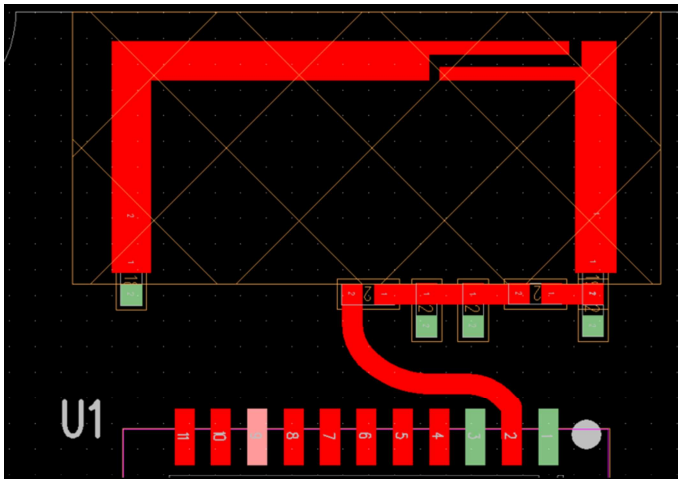

Figure 6. Routing traces from the RF port on the module, through the impedance matching network to the antenna port.

In **Figure 6**, an example is shown of routing a trace from the RF port on the module, through the impedance matching network to the input port of the antenna. Note that there are no discontinuities between the trace width and the pad size of the impedance matching components. Also note that the trace between the RF port on the module and the input of the impedance matching network has swept bends and does not use right-angled bends. Swept bends minimize RF discontinuities when trace turns are required.

In this example, the pad size of the 0402 (in) components were chosen because the pad size of 20 mil x 20 mil matches the 20-mil trace width required to maintain a 50 Ohm characteristic impedance. Therefore, the transmission line width minimizes discontinuities from changes in trace width.

The offset between the RF port on the module and the input port of the impedance matching network is shown in **Figure 7**. The path length of the swept trace (highlighted in pink in **Figure 7**) between the RF port on the module and the impedance matching network is **250 mil**.

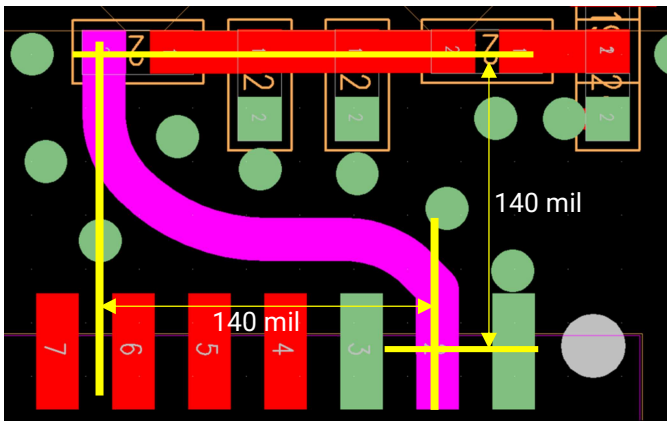

Figure 7. Offset between RF port on module and the input port of the impedance matching network.

f. Ensure that the RF trace to ground copper clearance on the same layer maintains the same gap as previously calculated.

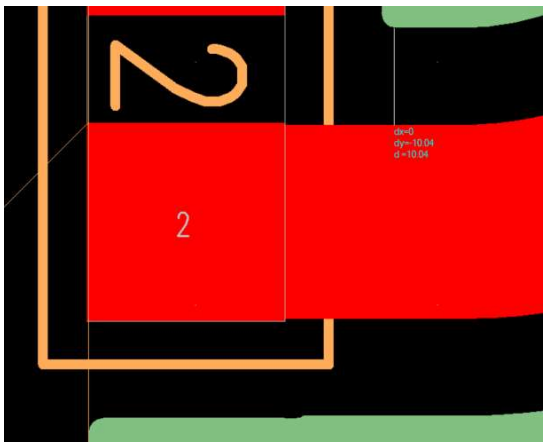

Figure 8. Illustration of the clearance gap between ground (green) and the RF trace (red) on the same layer.

In **Figure 8**, an example is shown of the clearance between the RF trace and the ground on the same layer. Ensure that copper-to-trace clearance between the RF trace and the ground is maintained between the RF port on the module, through the impedance matching network and to the antenna port. Ensure that the copper-to-trace clearance is set to the distance calculated previously using the transmission line calculator.

In this example, the gap clearance was set to **10 mil**.

g. Place at least one ground via in proximity of each ground pad of impedance matching components and along the perimeter of the copper pour keep out around the antenna.

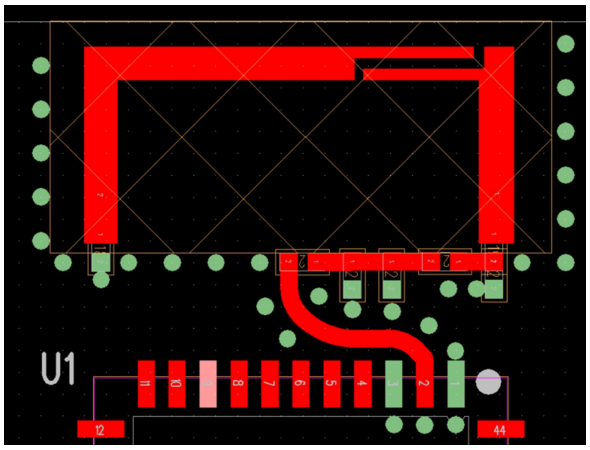

Figure 9. Ground via (green circles) placement around the antenna.

In **Figure 9**, an example is shown of the ground via placement around the antenna. The path of the placement of ground vias starts around the copper keep out and runs along the RF trace and impedance matching components and end behind the RF port on the module.

In this example, the vias were placed on a grid of **25 mil spacing**. Some of the vias, however, could not meet the via-to-copper clearance requirement and needed to be moved off the snap grid.

GENERAL ANTENNA GUIDELINES

1. To maintain good antenna performance:
    a. Ensure that conductors are not present within the reactive nearfield of the antenna.
    b. Ensure that magnetic materials are not present within the reactive nearfield of the antenna.
    c. Ensure that any dielectric that does not have a relative permittivity similar to that of free space (ε_r=1.0) is not present within the reactive nearfield of the antenna.
    d. Ensure that the antenna is not contained within a conductive enclosure.
    e. Keep the antenna as far away from the human body as the design permits.

ANTENNA IMPEDANCE MATCHING NETWORK

The purpose of an impedance matching network is to ensure that the maximum amount of real power is transferred from the RF port on the module to the input port of the antenna. Since impedance is a function of frequency, the physical placement of the components and transmission line lengths are critical to ensure maximum power transfer. Deviating from the antenna implementation example may require changes to the impedance matching network to ensure maximum power transfer.

Component values for the antenna implementation example are shown in **Figure 10**.

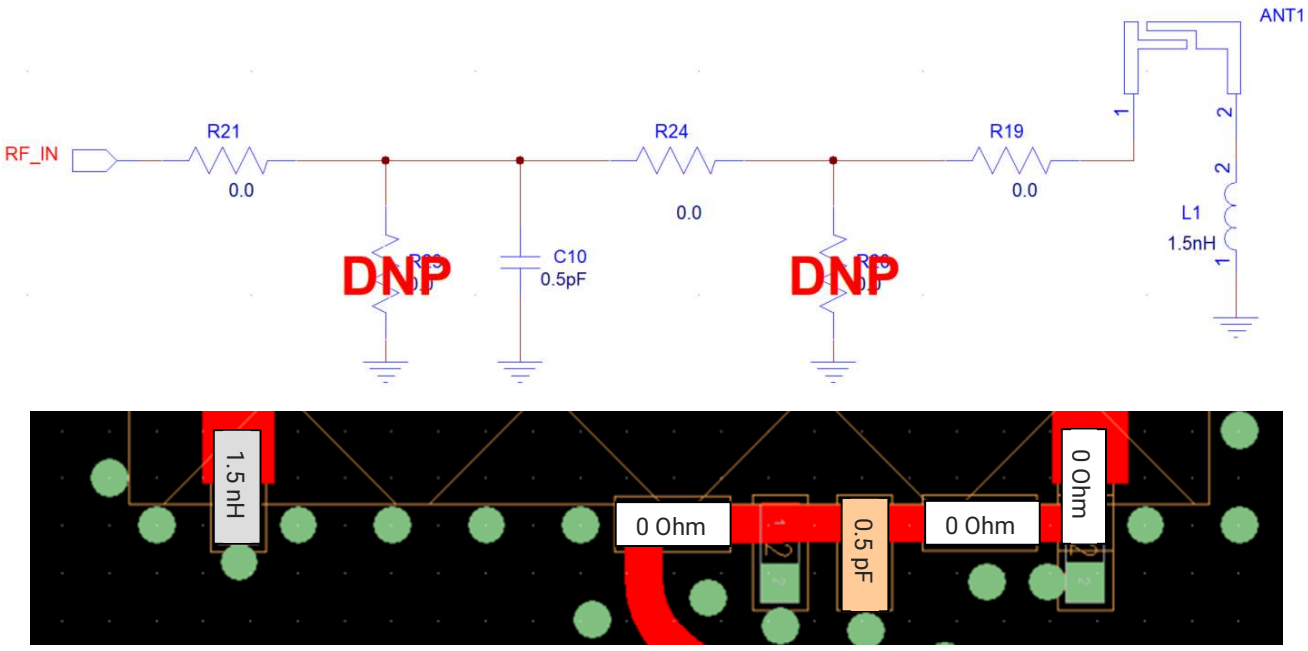

Figure 10. Impedance matching components for the antenna placement example.

GENERAL GUIDELINES FOR EMI REDUCTION

1. To minimize unintentional radiated emissions
    a. Keep analog and digital circuits in separate areas.
    b. Identify traces that carry high-speed signals and their return paths. Treat all high-speed traces as current loops. Note that a smaller loop area is better than maintaining short trace lengths.
    c. Orient adjacent-layer traces perpendicularly to reduce crosstalk.
    d. Route and maintain critical traces on internal layers to reduce emissions and improve immunity to external noise. RF traces, however, should be routed on outer layers to avoid the use of vias.
    e. Keep all trace lengths as short as the design permits.
    f. Keep traces, especially ones that carry high-speed signals or RF, as straight as the design permits.
    g. If trace turns are necessary, use mitered or swept bends. Do not use right-angle bends.
    h. Route supply voltages in a manner that minimizes capacitive coupling to other supply voltages. This can occur if power planes overlap on adjacent layers.
    i. Maintain a low ground impedance by providing as much ground plane as possible without discontinuities.
    j. Use as many ground vias as possible to connect all ground planes together.
    k. Maximize the width of power traces to ensure that the target current is supported.
    l. Place decoupling capacitors as close to the target power pins as practicable. Keep the capacitors on the same side when the design permits to minimize the series inductance introduced by vias.
    m. Use appropriate capacitance values for the target circuit.
    n. Use different capacitance values in parallel to maximize the frequency range for which the decoupling capacitors can shunt high frequency noise.

REVISION HISTORY

Previous Versions	Changes to Current Version	Page(s)
0030-02-16-00-001 (Issue A) January 16, 2025	Initial release	N/A

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