AW-CM389NF

IEEE 802.11 2X2 MIMO a/b/g/n/ac Wireless LAN + Bluetooth + NFC NGFF Module

Datasheet

Version 0.9

Document release	Date	Modification	Initials	Approved
Version0.1	2013/08/13	Initial version	Kai Wu	Chihhao Liao
Version0.2	2013/10/08	1. Update Pin Map 2. Update Interface Configuration straps	Alex Yu	Chihhao Liao
Version0.3	2013/11/07	1. Update Pin Map 2. Update Pin Definition 3. Update Dimension	Alex Yu	Chihhao Liao
Version0.4	2013/11/19	1. Update “2 Electrical Characteristic” 2. Update “3-1 SDIO Interface” 3. Update “4 Pin Definition” 4. Update “5 Mechanical Information” 5. Add “2-2.1 The interface pins power supply”	Alex Yu	Chihhao Liao
Version0.5	2013/12/03	Add “4 Pin Definition’s Notes”	Alex Yu	Chihhao Liao
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Version0.7	2013/12/11	1. Update “1-2 Block Diagram” 2. Update “5-2 Module Footprint”	Alex Yu	Chihhao Liao
Version0.8	2014/03/20	1. Update “1-4 Bluetooth Standard” 2. Update “5-1 Mechanical Information” 3. Update “2-3 Clock Specification” 4. Update “5-2 Module Footprint” 5. Add “7. Shipping Information”	Alex Yu	Chihhao Liao
Version0.9	2014/04/14	1. Update “1-4 Specifications Table” 2. Update “5-1 Mechanical Information”	Alex Yu	Chihhao Liao

1. General Description

1-1. Product Overview and Functional Description

AzureWave Technologies, Inc. introduces the IEEE 802.11ac/a/b/g/n 2X2 MIMO WLAN & Bluetooth & NFC NGFF module --- **AW-CM389NF**. The module is targeted to mobile devices including **Notebook, TV, Tablet and Gaming Device** which need small package module, low power consumption, multiple interfaces and OS support. By using AW-CH389, the customers can easily enable the Wi-Fi, and BT embedded applications with the benefits of **high design flexibility, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11ac/a/b/g/n standard, the AW-CM389NF uses Direct Sequence Spread Spectrum (**DSSS**), Orthogonal Frequency Division Multiplexing (**OFDM**), **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-CH389. In addition to the support of **WPA/WPA2** and **WEP** 64-bit and 128-bit encryption, the AW-CM389NF also supports the **IEEE 802.11i** security standard through the implementation of **Advanced Encryption Standard** (**AES)/Counter Mode CBC-MAC Protocol (CCMP),** Wired Equivalent Privacy (**WEP)** with Temporal Key Integrity Protocol (**TKIP**), Advanced Encryption Standard (**AES**)/Cipher-Based Message Authentication Code (**CMAC**), and WLAN Authentication and Privacy Infrastructure (**WAPI**) security mechanisms.

For the video, voice and multimedia applications the AW-CM389NF support **802.11e Quality of Service** (**QoS).** The device also supports **802.11h Dynamic Frequency Selection (DFS)** for detecting radar pulses when operating in the 5GHz range.

For Bluetooth operation, AW-CM389NF is **Bluetooth 4.0 (supports Low Energy).**

AW-CM389NF supports **SDIO, PCIE, USB,** and high speed **UART interfaces** for WLAN and Bluetooth to the host processor.

AW-CM389NF is suitable for multiple mobile processors for different applications with the support **cellular phone co-existence**.

AW-CM389NF module adopts Marvell's latest highly-integrated dual-band WLAN & Bluetooth SoC---**88W8897**. All the other components are implemented by all means to reach the mechanical specification required.

Note: Interface supports and combinations as shown below:

Scenario	WLAN	BT/NFC	BT_AMPS	Firmware Download I/F	Firmware Download Mode	Configuration*
1	SDIO	SDIO	SDIO	SDIO	Serial	CON[3:0]=b'0111
2	SDIO	SDIO	--	SDIO	Serial	CON[3:0]=b'0001
3	SDIO	UART	SDIO	SDIO or UART	Serial	CON[3:0]=b'1101
4	SDIO	UART	SDIO	SDIO + UART	Parallel	CON[3:0]=b'0010
5	SDIO	UART	--	SDIO or UART	Serial	CON[3:0]=b'0100
6	USB	USB	USB	USB	Serial	CON[3:0]=b'0110
7	USB	UART	USB	USB or UART	Serial	CON[3:0]=b'1010
8	USB	UART	--	USB + UART	Parallel	CON[3:0]=b'1000
9	PCIe	UART	--	PCIe + UART	Parallel	CON[3:0]=b'1111
10	PCIe	UART	--	PCIe or UART	Serial	CON[3:0]=b'1100
11	PCIe	USB	USB	PCIe	Serial	CON[3:0]=b'1110

***Configuration pins:**

Configuration	Pin No	Pin Name
CON[3]	13	CONFIG_HOST[3]
CON[2]	10	CONFIG_HOST[2]
CON[1]	9	CONFIG_HOST[1]
CON[0]	8	CONFIG_HOST[0]

1-3. Key feature:

Small footprint: 12mm(L) x 16mm(W) x 1.4 mm(H)
SDIO3.0, G-SPI, USB interfaces support for WLAN
High speed UART,PCM/Inter-IC Sound(I2S) and SDIO3.0, USB for Bluetooth
Bluetooth 4.0 complaint with Bluetooth 2.1 + Enhanced Data Rate (EDR)
Audio Codec interface support
Cellular phone co-existence support
Multiple power saving modes for low power consumption
IEEE 802.11i for advanced security
Quality of Service (QoS) support for multimedia applications
Drip-in WLAN Linux drivers are Android ready and validated on Android based systems.
Support for Linux kernel versions up to 2.6.32.
Support for BlueZ v4.47 Bluetooth profiles stack used in Android Éclair
Simultaneous AP-STA
Support China WAPI
Lead-free design

1-4. Specifications Table

Model Name	AW-CM389NF
Product Description	**2x2 MIMO Wireless LAN + Bluetooth + NFC Combo Module**
WLAN Standard	IEEE 802.11 a/b/g/n/ac, Wi-Fi compliant
Bluetooth Standard	Bluetooth 4.0 complaint with Bluetooth 2.1+Enhanced Data Rate (EDR)
NFC Standard	Full protocol support for ISO 14443A/B, ISO 18092, ISO 15693, NFCIP-1, NFC Forum, EMV contactless targets with data rates up to 848 Kbps
Host Interface	USB 2.0 for WLAN and Bluetooth
Major Chipset	Marvell 88W8897
Dimension	12mm x 16mm x 1.4mm
Weight	TBD
Package	LGA
Operating Conditions	
Voltage	3.3V+- 10%
Temperature	Operating: -20 ~ 70°C ; Storage: -40 ~ 85°C
Electrical Specifications	
Frequency Range	2.4 GHz ISM radio band / 5 GHz Unlicensed National Information Infrastructure (U-NII) band
Number of Channels	802.11a: USA, Taiwan – 12/4 Most European Countries –19 Japan – 4 802.11b: USA, Canada and Taiwan – 11 Most European Countries – 13 France – 4 802.11g: USA, Canada and Taiwan – 11 Most European Countries – 13 Japan – 13 802.11n(HT20): Channel 1~14(2412~2484) 802.11n(HT40): Channel 1~7(2422~2472)
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM for WLAN GFSK (1Mbps), /4 DQPSK (2Mbps) and 8DPSK (3Mbps) for Bluetooth
Output Power	WLAN G band: 11b:16dBm +/- 2dBm(11M) 11g:14dBm +/- 2dBm (54M) 11n:HT20 13dBm +/- 2dBm(MCS7) HT40 11dBm +/- 2dBm(MCS7) WLAN A band: 11a: 13dBm +/- 2dBm(54M) 11n:HT20 12dBm +/- 2dBm(MCS7) HT40 10dBm +/- 2dBm(MCS7) 11ac: 8dBm +/- 2dBm(MCS9) Bluetooth: Class 2

	Main Connector: WLAN Aux Connector: WLAN + BT
	WLAN G band : **11b:-83dBm (11M)** **11g:-72dBm (54M)** **11n:HT20 -68dBm (MCS7)** **HT40 -65dBm (MCS7)** **WLAN A band:** **11a: -67dBm (54M)** **11n:HT20 -67dBm (MCS7)** **HT40 -64dBm(MCS7)** **11ac: -54dBm(MCS9)** **Bluetooth:** **DH1:-70dBm** **3DH5:-70dBm**
	CSMA/CA with ACK
	WLAN **802.11b: 1, 2, 5.5, 11Mbps** **802.11a/g: 6, 9, 12, 18, 24, 36, 48, 54Mbps** **802.11n: up to 150Mbps-single** **802.11n: up to 300Mbps-2x2 MIMO** **802.11ac:up to 192.6Mbps (20MHz channel)** **802.11ac:up to 400Mbps (40MHz channel)** **802.11ac:up to 866.7Mbps (80MHz channel)** **Bluetooth** **Bluetooth 2.1+EDR data rates of 1,2, and 3Mbps** **NFC** **NFC data rates up to 848Kbps**
	TBD
	Open Space: ~300m ; Indoor: ~100m for WLAN **Minimum 10 m indoor for Bluetooth** **The transmission speed may vary according to the environment)**
	WAPI **WEP 64-bit and 128-bit encryption with H/W TKIP processing** **WPA/WPA2 (Wi-Fi Protected Access)** **AES-CCMP hardware implementation as part of 802.11i security standard**
	Linux(Android), Windows, More information please contact Azurewave FAE.
	Bluetooth and cell phone(GSM/DCS/WCDMA/UMTS/3G) co-existence

2. Electrical Characteristic

2-1. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Units
Pin73/ VIO	Host I/O power supply	-- -- --	-- -- --	1.8 2.5 3.3	2.2 3.0 4.0	V
Pin44/ VIO_SD	SDIO power supply	-- --	-- --	1.8 3.3	2.2 4.0	V
Pin5/ 3V3_VBAT	LDO VBAT input	--	--	3.3	5.0	V
Pin72/ 3V3_USB	LDO USB VBAT input	--	--	3.3	4.0	V
Pin4/ 3V3_RF	LDO RF VBAT input	--	--	3.3	4.0	V

2-2. Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Pin73/ VIO	1.8V/2.5V/3.3V digital I/O power supply	-- -- --	1.62 2.25 2.97	1.8 2.5 3.3	1.98 2.75 3.63	V
Pin44/ VIO_SD	1.8V/3.3V digital I/O SDIO power supply	-- --	1.62 2.97	1.8 3.3	1.98 3.63	V
Pin5/ 3V3_VBAT	LDO VBAT input	--	2.7	3.3	5.0	V
Pin72/ 3V3_USB	LDO USB VBAT input	--	2.97	3.3	3.63	V
Pin4/ 3V3_RF	LDO RF VBAT input	--	2.97	3.3	3.63	V

2-2.1 The interface pins power supply

The NFC interface pins are powered from the module's chip LDO 1.8V voltage supply internal.

The SDIO host interface pins are powered from the chip VIO_SD (pin 44) 1.8V/3.3V voltage supply.

- SDIO Defauld Speed, High Speed Modes (3.3V)
- SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)
- SDR104 Mode (208MHz) (1.8V)

The PCI Express host interface pins are powered from the module's chip LDO 1.8V voltage supply internal.

The USB2.0 host interface pins are powered from the 3V3_USB (pin 72) 3.3V voltage supply.

The UART Tx and Rx pins are powered from the VIO (pin 73) voltage supply.

The GPIO pins are powered from the VIO (pin 73) voltage supply (GPIO [9:8] from 3.3V voltage internal).

The clocked serial pins are powered from the module's chip LDO 1.8V voltage supply internal.

The audio pins are powered from the chip VIO (pin 73) voltage supply.

2-3. Clock Specifications

2-3.1 External Sleep Clock Timing

External Sleep Clock is necessary for two reasons:

1. Auto frequency Detection.
   This is where the internal logic will bin the Ref clock source to figure out what is the reference clock frequency is. This is done so no strapping is needed for telling 8897 what the ref clock input is.
2. Allow low current modes for BT to enter sleep modes such as sniff modes.
   The AW-CM389NF external sleep clock pin is powered from the 3.3V voltage supply.

Symbol	Parameter	Min	Typ	Max	Units
CLK	Clock Frequency Range	32 or 32.768 - 50ppm	32 or 32.768	32 or 32.768 +50ppm	KHz
T_{HIGH}	Clock high time	40	--	--	ns
T_{LOW}	Clock low time	40	--	--	ns
T_{RISE}	Clock rise time	--	--	5	ns
T_{FALL}	Clock fall time	--	--	5	ns

2-4. Reset Configuration

The AW-CM389NF is reset to its default operating state under the following conditions:

Power-on reset (POR)

Software/Firmware reset

External pin reset (RESETn)

2-4-1. Internal Reset

The AW-CM389NF device is reset, and the internal CPU begins the boot sequence when any of the following internal reset events occur:

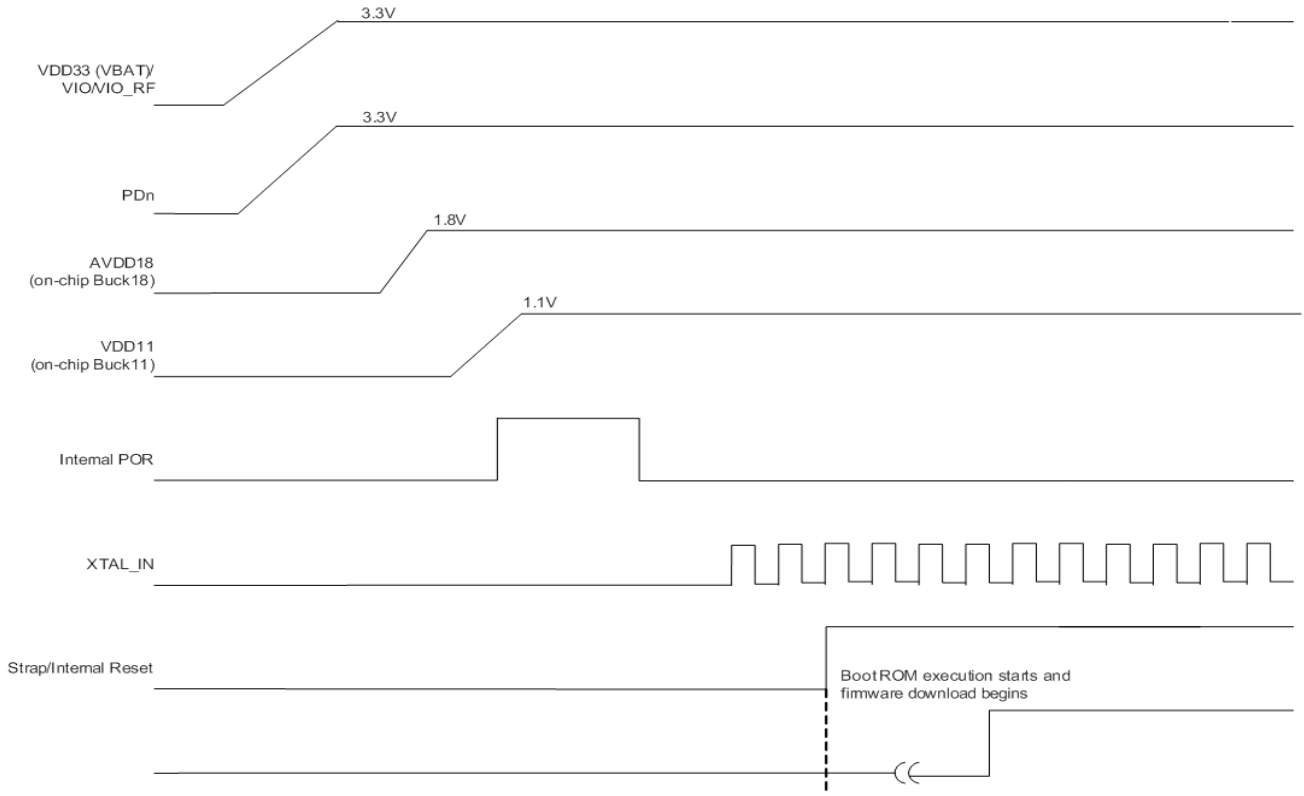
Device receives power and VDDL supplies rise (triggers internal POR circuit)

External pin (PDn) assertion will generate POR

2-4-2. External Reset

The AW-CM389NF is reset when PDn pin is asserted low and the internal CPU begins the boot sequence when the PDn pin transitions from low to high.

2-5. Power up Timing Sequence



3. Host Interfaces

3-1. SDIO Interface

The AW-CM389NF supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless module device.

The AW-CM389NF acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

Supports SDIO 3.0 Standard

On-chip memory used for CIS

Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes

Special interrupt register for information exchange

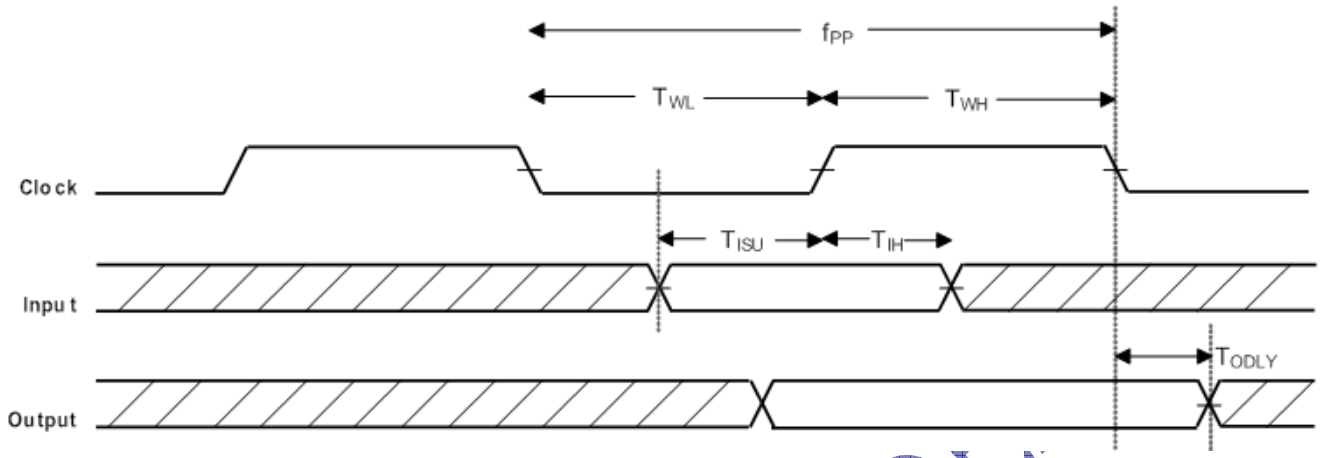
Allows card to interrupt host

3-1-1. SDIO Interface Signal Description

Pin Name	Signal Name	Type	Description
SD_CLK	CLK	I/O	SDIO 1-bit mode: Clock SDIO SPI mode: Clock
SD_CMD	CMD	I/O	SDIO 1-bit mode: Command line SDIO SPI mode: Data input
SD_DAT[3]	DAT3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (active low)
SD_DAT[2]	DAT2	I/O	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPII mode: Reserved
SD_DAT[1]	DAT1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt
SD_DAT[0]	DAT0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data output

3-1-2. Default Speed, High Speed Modes (3.3V)

SDIO Protocol Timing Diagram – Default Speed Mode (3.3V)



SDIO Protocol Timing Diagram – HighSpeed Mode (3.3V)

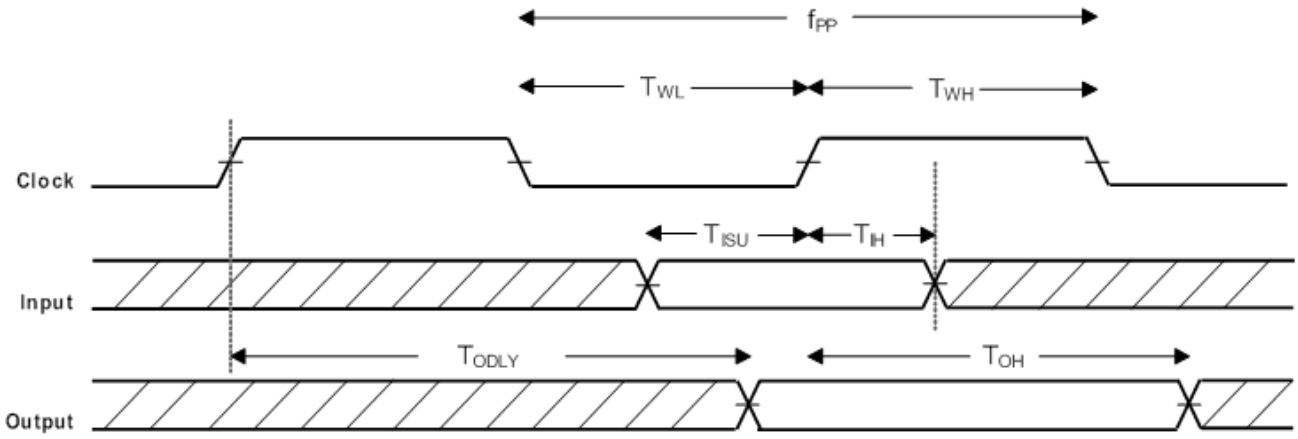


Table shows SDIO Timing Data—Default Speed, High Speed Modes (3.3V)

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency	Default Speed	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WL}	Clock Low Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{WH}	Clock High Time	Default Speed	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Default Speed	5	--	--	ns
		High Speed	6	--	--	ns
T_{IH}	Input Hold Time	Default Speed	5	--	--	ns
		High Speed	2	--	--	ns
T_{ODLY}	Output Delay Time CL ≤ 40 pF (1 card)	Default Speed	--	--	14	ns
		High Speed	---	-1	4	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

3-1-3. SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)

SDIO Protocol Timing Diagram – SDR12,SDR25,SDR50 Modes (up to 100MHz) (1.8V)

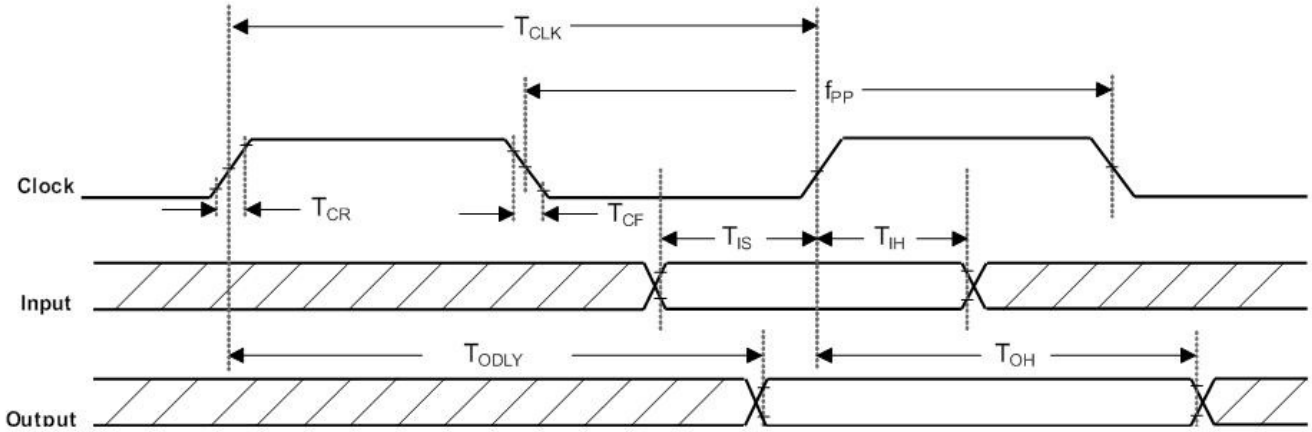


Table shows SDIO Timing Data—SDR12,SDR25,SDR50 Modes (up to 100MHz) (1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time $C_L \leq 30$ pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	--	--	ns

3-1-4. SDR104 Modes (208MHz) (1.8V)

SDIO Protocol Timing Diagram –SDR104 Mode (208MHz)

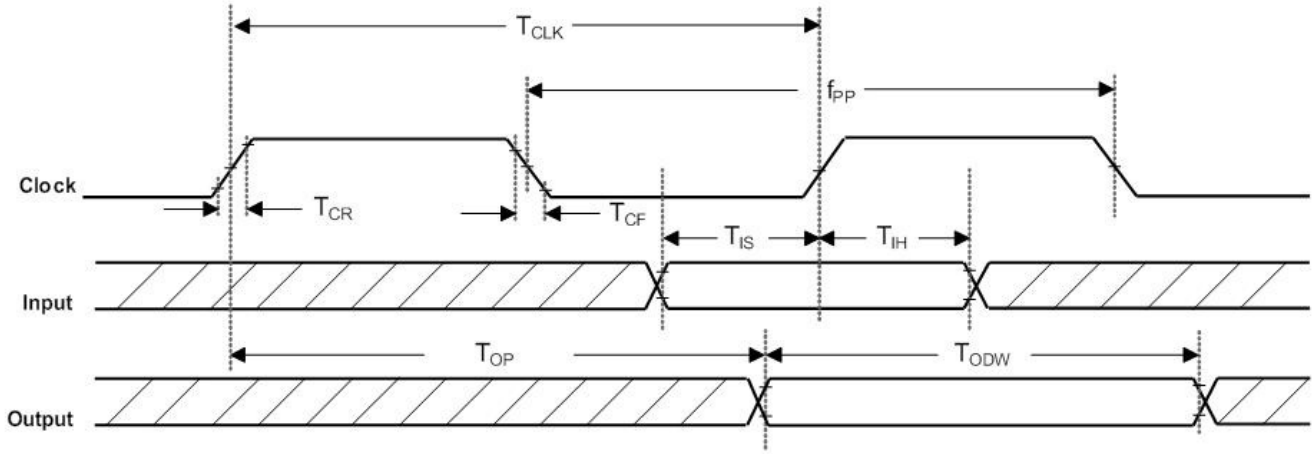


Table shows SDIO Timing Data—SDR104 Mode (208MHz)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR104	0	--	208	MHz
T_{IS}	Input setup time	SDR104	1.4	--	--	ns
T_{IH}	Input hold time	SDR104	0.8	--	--	ns
T_{CLK}	Clock time	SDR104	4.8	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	--	--	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	--	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	--	--	ns

3-2. PCI Express Interface

3-2-1 Differential Tx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 PPM. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Tx_DIFFpp}	Differential peak-to-peak output voltage $V_{Tx\_DIFFpp} = 2*\|V_{TX-D+} - V_{TX-D-}\|$	0.800	--	1.2	V
$V_{Tx\_DE\_RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	db
T_{Rx_EYE}	Minimum Tx eye width	0.75	--	--	UI
$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.125	UI
T_{Tx_RISE}, T_{Tx_FALL}	D+/D- Tx output rise/fall time	0.125	--	--	UI
$V_{Tx\_CM\_DC\_ACTIVE\_IDLE\_DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle	0-	-	100	mV
$V_{Tx\_CM\_DC\_LINE\_DELTA}$	Absolute delta of DC common mode voltage between D+ and D-	0-	-	25	mV
$V_{Tx\_IDLE\_DIFFp}$	Electrical idle differential peak output voltage	0	--	20	mV
$V_{Tx\_RCV\_DETECT}$	Voltage change allowed during receiver detection	--	--	600	mV
$V_{Tx\_DC\_CM}$	Tx DC common mode voltage	--	--	3.6	V
I_{Tx_SHORT}	Tx short circuit current limit	--	--	90	mA
$T_{Tx\_IDLE\_MIN}$	Minimum time spent in electrical idle	50	--	--	UI
$T_{Tx\_IDLE\_SET\_TO\_IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	--	--	20	UI
$T_{Tx\_IDLE\_TO\_DIFF\_DATA}$	Maximum time to transition to valid Tx specifications after leaving an electrical idle condition	--	--	20	UI
RL_{Tx_DIFF}	Differential return loss	10	--	--	dB
RL_{Tx_CM}	Common mode return loss	6	--	--	dB
C_{Tx}	AC coupling capacitor	75	--	200	nF
$T_{Crosstalk}$	Crosstalk random timeout	0	--	1	ms

3-2-2 Differential Rx Output Electricals

Symbol	Parameter	Min	Typ	Max	Units
UI	Unit interval Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations.	399.98	400	400.12	ps
V_{Rx_DIFFpp}	Differential peak-to-peak voltage $V_{Rx\_DIFFpp} = 2*\|V_{RX-D+} - V_{RX-D-}\|$	0.175	--	1.2	V
T_{Rx_EYE}	Minimum receiver eye width	0.4	--	--	UI
$T_{Rx\_EYE\_MEDIAN\_MAX\_JIT}$	Maximum time between jitter median and maximum deviation from median	--	--	0.3	UI
$V_{Rx\_CM\_ACp}$	AC peak common mode input voltage	--	--	150	mV
RL_{Rx_DIFF}	Differential return loss	10	--	--	dB
RL_{Rx_CM}	Common mode return loss	6	--	--	dB
$Z_{Rx\_DIFF\_DC}$	DC differential input impedance	80	100	120	Ω
Z_{Rx_DC}	DC input impedance	40	50	60	Ω
$Z_{Rx\_HIGH\_IMP\_DC\_POS}$	Powered down DC input impedance positive	50	--	--	k
$Z_{Rx\_HIGH\_IMP\_DC\_NEG}$	Powered down DC input impedance negative	1	--	--	kΩ
$V_{Rx\_IDLE\_DET\_DIFFpp}$	Electrical idle detect threshold	65	--	175	mV
$T_{Rx\_IDLE\_DET\_DIFF\_ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time	--	--	10	ms
L_{Rx_SKEW}	Total skew	---	-2	0	ns

3-3. USB Interface

The USB device interface is compliant with the Universal Serial Bus Specification, Revision 2.0, April 27, 2000. A USB host uses the USB cable bus and the USB 2.0 device interface to communicate with the chip.

The main features of the USB device interface include:

High/full speed operation (480/12 Mbps)

Suspend/host resume/device resume (remote wake-up)

Built-in DMA engine that reduces interrupt loads on the embedded processor and reduces the system bus bandwidth requirement for serving the USB device operation

The USB 2.0 device interface is designed with 3.3V signal level pads.

3-3-1. USB 2.0 Device Interface Description

Table shows the signal mapping between the AW-CM389NF and the USB Specification, Revision 2.0.

Pin Name	USB 2.0 Specification Pin Name	Description
Pin72/ 3V3_USB	VBUS	USB Bus Power Supply On-board regulator regulates voltage from VBUS level to voltage levels used by USB PHY.
	GND	USB Bus Ground Common ground on SoC device.
Pin70/ USB_DP	D+	USB Bus Data Plus One of the differential data pair.
Pin69/ USB_DM	D-	USB Bus Data Minus One of the differential data pair.

3-3-2. USB 2.0 Device Functional Description

The device controller uses internal Scatter/Gather DMA engine to transfer the transmit packet from internal SRAM to USB and the receive packet from USB to internal SRAM. The Device IN Endpoint DMA (DIEPDMAn) and Device OUT Endpoint DMA (DOEPDMAn) registers are used by the DMA engine to access the base descriptor. The application is interrupted after the programmed transfer size extracted from the descriptors is transmitted or received. By using registers, interrupts, and special data structures, the device controller can communicate with the device controller driver (application/software) about bus states, host request, and data transfer status. The device controller driver also has all of the routines to respond to the device framework commands issued by a USB host, so it controls the attachment, configuration, operation, and detachment of the device.

3-4. High-Speed UART Interface

The AW-CH389 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data. Table shows the rates supported.

The UART interface features include:

FIFO mode permanently selected for transmit and receive operations

Two pins for transmit and receive operations

Two flow control pins

Interrupt triggers for low-power, high throughput operation

The UART interface operation includes:

Upload boot code to the internal CPU (for debug purposes)

Support diagnostic tests

Support data input/output operations for peripheral devices connected through a standard UART interface

UART Baud Rates Supported

Baud Rate				
1200	38400	460800	1500000	3000000
2400	57600	500000	1843200	3250000
4800	76800	921600	2000000	3692300
9600	115200	1000000	2100000	4000000
19200	230400	1382400	2764800	--

3-4-1. UART Interface Signal Description

Table shows the standard UART signal names on the device.

Signal Name	16550 Standard Pin Name	Description
Data Bus		
UART_SIN	SIN	Serial data input from modem, data set, or peripheral device
UART_SOUT	SOUT	Serial data output from modem, data set, or peripheral device
Modem Control		
UART_RTSN	RTS	Request To Send output to modem, data set, or peripheral device (active low)
UART_CTSN	CTS	Clear To Send input from modem, data set, or peripheral device (active low)

3-4-2. UART Interface Functional Description

3-3-2-1. Booting from UART

When booting from the UART, the AW-CH389 device has the following requirements:

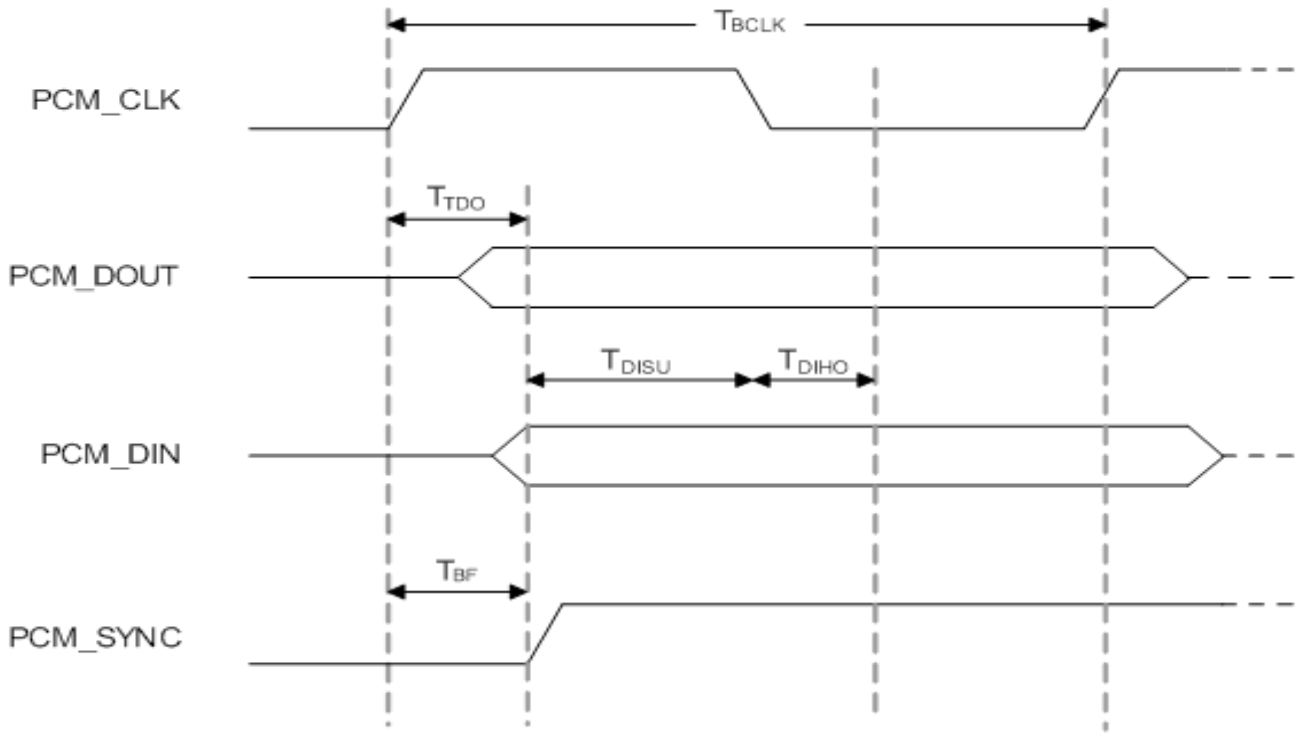
System Requirement	Description
Number of data bits	8 bits
Stop bits	1 bit
Parity	No parity
Baud Rate	115200

3-4-2-2. UART as Test Port

Test diagnostic programs may be uploaded to the CPU through the UART interface. During execution, the diagnostic program transmits performance and status information through the UART by performing a write to the PBU address space designated to the UART.

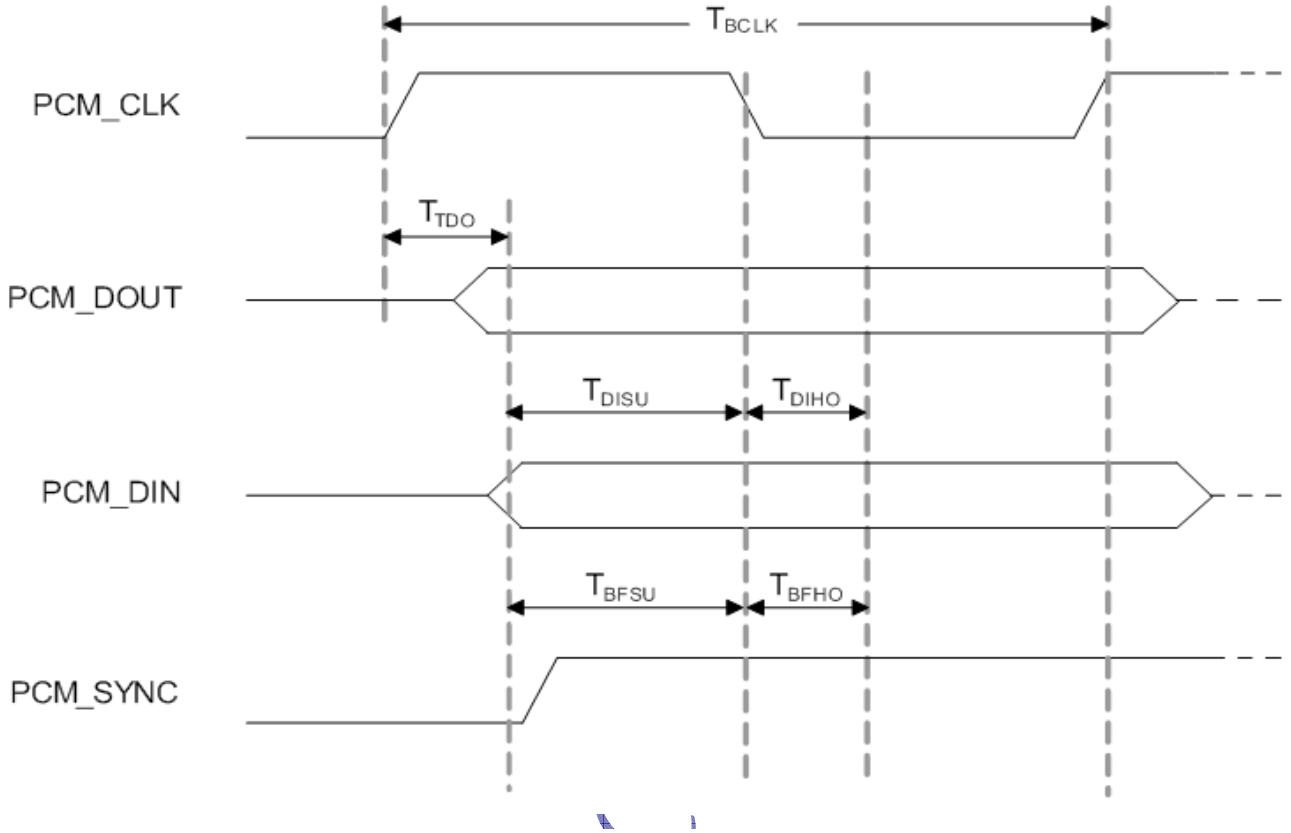
3-5. PCM Interface

3-5-1. PCM Timing Specification – Master Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	15	ns
T_{DISU}	--	--	20	--	--	ns
T_{DIHO}	--	--	15	--	--	ns
T_{BF}	--	--	--	--	15	ns

3-5-2. PCM Timing Specification – Slave Mode



Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{BCLK}	--	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	--	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	--	--	--	3	--	ns
T_{DO}	--	--	--	--	30	ns
T_{DISU}	--	--	15	--	--	ns
T_{DIHO}	--	--	10	--	--	ns
T_{BFSU}	--	--	15	--	--	ns
T_{BFHO}	--	--	10	--	--	ns

4. Pin Definition

Pin No	Definition	Basic Description	Type
1	TMS	JTAG controller select	
2	TCK	JTAG test clock	
3	TDI	JTAG test data(input)	I
4	3V3_RF	3.3V Analog RF Power Supply	I
5	3V3_VBAT	3.3V VBAT system power supply input	I
6	GND	System Ground Pin	
7	TDO	JTAG test data(output)	O
8	CONFIG_HOST[0]	Configuration: CONFIG_HOST[0]	
9	CONFIG_HOST[1]	Configuration: CONFIG_HOST[1]	
10	CONFIG_HOST[2]	Configuration: CONFIG_HOST[2]	
11	GPIO[1]/LTE_SOUT	UART_LTE_SOUT (output)	I
12	GPIO[2]/LTE_SIN	UART_LTE_SIN (input)	I
13	CONFIG_HOST[3]	Configuration: CONFIG_HOST[3]	
14	GPIO[10]/NFC_NOT_ALLOWED(I)	GPIO[10] (input/output)	
15	NFC_WI_IN	SE I/O for NFC-WI or DCLB, depending on the configuration	I/O
16	NFC_SW1_VDDIN	Supply from device to UICC thru integrated power switch CSP only	I/O
17	GND	System Ground Pin	
18	NFC_SWP2_IO	SE I/O for SWP, NFC-WI, or DCLB, depending on the configuration	I/O
19	NFC_SWP1_IO	UICC Single Wire Protocol I/O CSP only	I/O
20	GND	System Ground Pin	
21	NFC_SWP1_Vout	Supply to UICC from device thru integrated power switch CSP only.	I/O
22	NFC_SWP2_Vout	Supply from NFC to embedded SE CSP only.	I/O
23	GND	System Ground Pin	
24	NFC_ANTN	Antenna Interface, negative input/output	I/O
25	NFC_ANTP	Antenna Interface, positive input/output	I/O
26	GND	System Ground Pin	
27	SLP_CLK	Sleep Clock Input Used for WLAN and Bluetooth low- power modes. External sleep clock of 32.768 KHz must be used for auto reference clock calibration and for WLAN/Bluetooth low power operation.	I

Pin No	Definition	Basic Description	Type
28	GPIO[13]/NFC/BT IRQ(O)	GPIO[13] (input/output)	
29	PCIE_WAKEn	PCIe wake signal (output) (active low)	O
30	PCIE_CLKREQn	PCIe clock request (input/output) (active low)	I/O
31	GPIO[12]/PCIE_PERSTn	PCIe host indication to reset the device (input) (active low)	I
32	GND	System Ground Pin	
33	PCIE_RCLK_N	PCI Express Differential Clock Input—Negative	I
34	PCIE_RCLK_P	PCI Express Differential Clock Input—Positive	I
35	GND	System Ground Pin	
36	PCIE_TX_N	PCI Express Transmit Data—Negative	O
37	PCIE_TX_P	PCI Express Transmit Data—Positive	O
38	GND	System Ground Pin	
39	PCIE_RX_N	PCI Express Receive Data—Negative	I
40	PCIE_RX_P	PCI Express Receive Data—Positive	I
41	GND	System Ground Pin	
42	GPIO[0]/CLK_REQ	GPIO[0] (input/output)	O
43	GPIO[11]/NFC_ACTIVE(O)	GPIO[11] (input/output)	
44	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply	I
45	PDn	Full Power Down (input) (active low)	I
46	GPIO[3]/WLAN IRQ(O)	GPIO[3] (input/output)	I
47	SD_DAT[3]	SDIO Data line Bit[3]	I/O
48	SD_DAT[2]	SDIO Data line Bit[2]	I/O
49	SD_DAT[1]	SDIO Data line Bit[1]	I/O
50	SD_DAT[0]	SDIO Data line Bit[0]	I/O
51	SD_CMD	SDIO Command/response (input/output)	I/O
52	SD_CLK	SDIO Clock input	I
53	NC	No Connect	
54	GPIO[6]	UART_CTSn (input)	I
55	GPIO[4]	UART_SOUT (output)	O
56	GPIO[5]	UART_SIN (input)	I
57	GPIO[7]	UART_RTSn (output)	O
58	GPIO[22]/PCM_SYNC	GPIO[22] (input/output)	I/O

Pin No	Definition	Basic Description	Type
59	GPIO[19]/PCM_IN	GPIO[19] (input/output)	I
60	GPIO[20]/PCM_OUT	GPIO[20] (input/output)	O
61	GPIO[21]/PCM_CLK	GPIO[21] (input/output)	I/O
62	GND	System Ground Pin	
63	GPIO[14]	GPIO[14] (input/output)	
64	GPIO[8]/WLAN_LED	LED_OUT_WLAN (output)	O
65	GPIO[9]/BT_LED	LED_OUT_BT (output)	O
66	NFC_SDA	I/O for external EEPROM using 2-wire protocol CSP only.	I/O
67	NFC_CLK	Serial clock for external EEPROM using 2-wire protocol CSP only.	I/O
68	GND	System Ground Pin	
69	USB_DM	USB Serial Differential Data Negative	I/O
70	USB_DP	USB Serial Differential Data Positive	I/O
71	GND	System Ground Pin	
72	3V3_USB	3.3V Power Supply	I
73	VIO	Digital I/O Power Supply	I
74	GND	System Ground Pin	
75	GND	System Ground Pin	
76	GND	System Ground Pin	
77	GND	System Ground Pin	
78	GND	System Ground Pin	
79	GND	System Ground Pin	
80	GND	System Ground Pin	
81	GND	System Ground Pin	
82	GND	System Ground Pin	
83	GND	System Ground Pin	
84	GND	System Ground Pin	
85	GND	System Ground Pin	
86	GND	System Ground Pin	
87	GND	System Ground Pin	
88	GND	System Ground Pin	
89	GND	System Ground Pin	

Pin No	Definition	Basic Description	Type
90	GND	System Ground Pin	
91	GND	System Ground Pin	
92	GND	System Ground Pin	
93	GND	System Ground Pin	
94	GND	System Ground Pin	
95	GND	System Ground Pin	
96	GND	System Ground Pin	
G1	GND	System Ground Pin	
G2	GND	System Ground Pin	
G3	GND	System Ground Pin	
G4	GND	System Ground Pin	
G5	GND	System Ground Pin	
G6	GND	System Ground Pin	
G7	GND	System Ground Pin	
G8	GND	System Ground Pin	
G9	GND	System Ground Pin	
G10	GND	System Ground Pin	
G11	GND	System Ground Pin	
G12	GND	System Ground Pin	
G13	GND	System Ground Pin	
G14	GND	System Ground Pin	
G15	GND	System Ground Pin	
G16	GND	System Ground Pin	
G17	GND	System Ground Pin	
G18	GND	System Ground Pin	
G19	GND	System Ground Pin	
G20	GND	System Ground Pin	
G21	GND	System Ground Pin	
G22	GND	System Ground Pin	
G23	GND	System Ground Pin	
G24	GND	System Ground Pin	

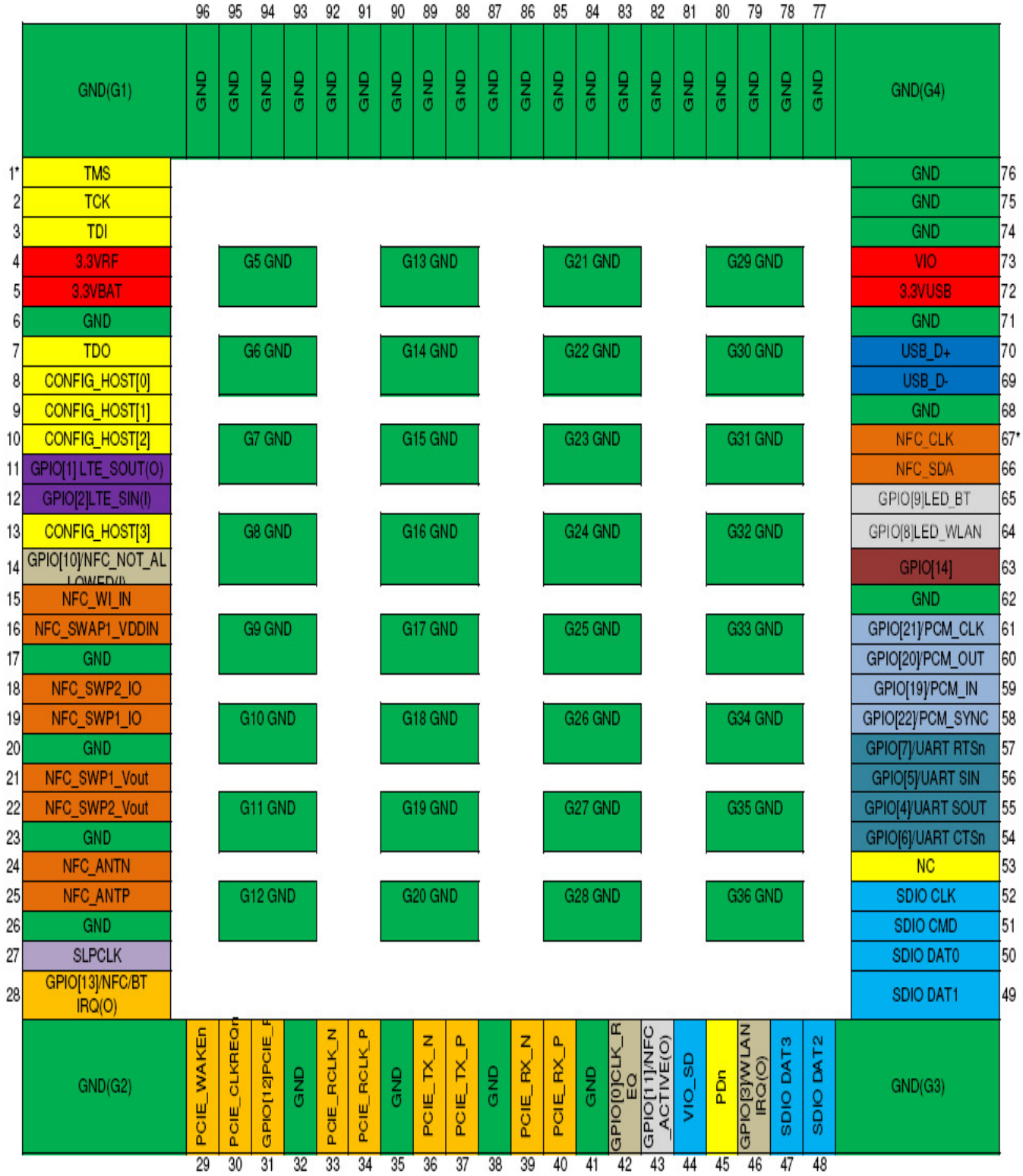
Pin No	Definition	Basic Description	Type
G25	GND	System Ground Pin	
G26	GND	System Ground Pin	
G27	GND	System Ground Pin	
G28	GND	System Ground Pin	
G29	GND	System Ground Pin	
G30	GND	System Ground Pin	
G31	GND	System Ground Pin	
G32	GND	System Ground Pin	
G33	GND	System Ground Pin	
G34	GND	System Ground Pin	
G35	GND	System Ground Pin	
G36	GND	System Ground Pin	

Notes:

1. SDIO signals should have 50 ohm impedances.
2. For SDIO interface, 33ohm inline resistor may be needed to help with signal integrity.
3. For GPIO[8] ,it's internal pull up to VIO-RF(3.3V).
4. For GPIO[9] ,it's internal pull up to VIO-RF(3.3V).
5. For PDn pin ,please pull up resistor(51k ohm) to hots or VBAT(3V3).
6. For SDIO interface, the pull up value is between 10K to 100K ohm according to the SDIO v3.0 SPEC.
7. PCIE Impedance targets: Single-ended Z of 60 ohms +- 15% . Differential Impedance of ~100 ohm +- 20%.
8. USB Impedance targets: D+/D- are differential and should have 90ohms impedance.
9. For NFC _SWP1_VDDIN ,please reserve a bypass capacitor(0.1 uF 0402) on the main board.
10. For GPIO[3] pin ,please pull up resistor(10k ohm) to VIO.

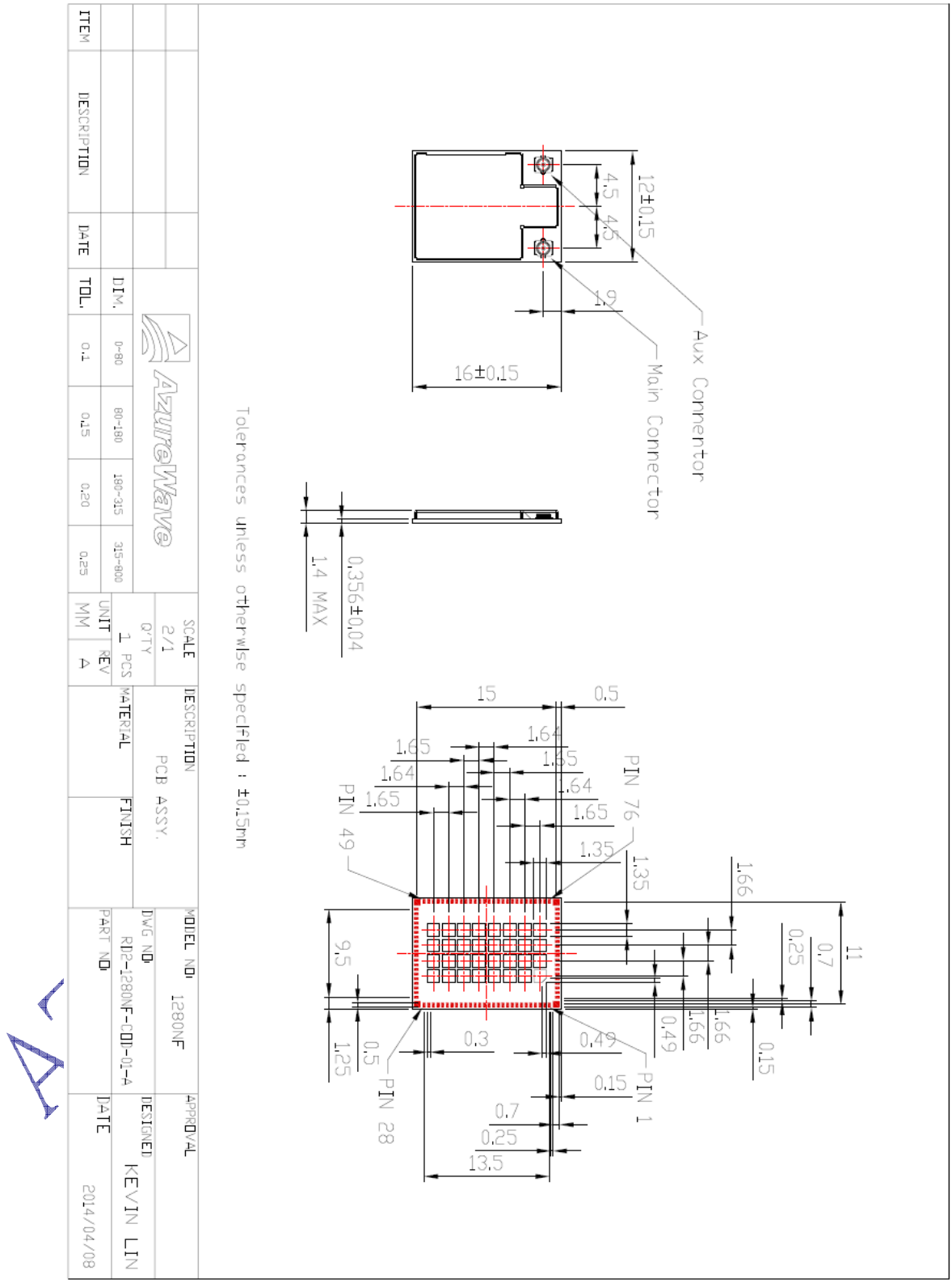
4-1 Pin Map

AW-CM389NF Top View Pin Map



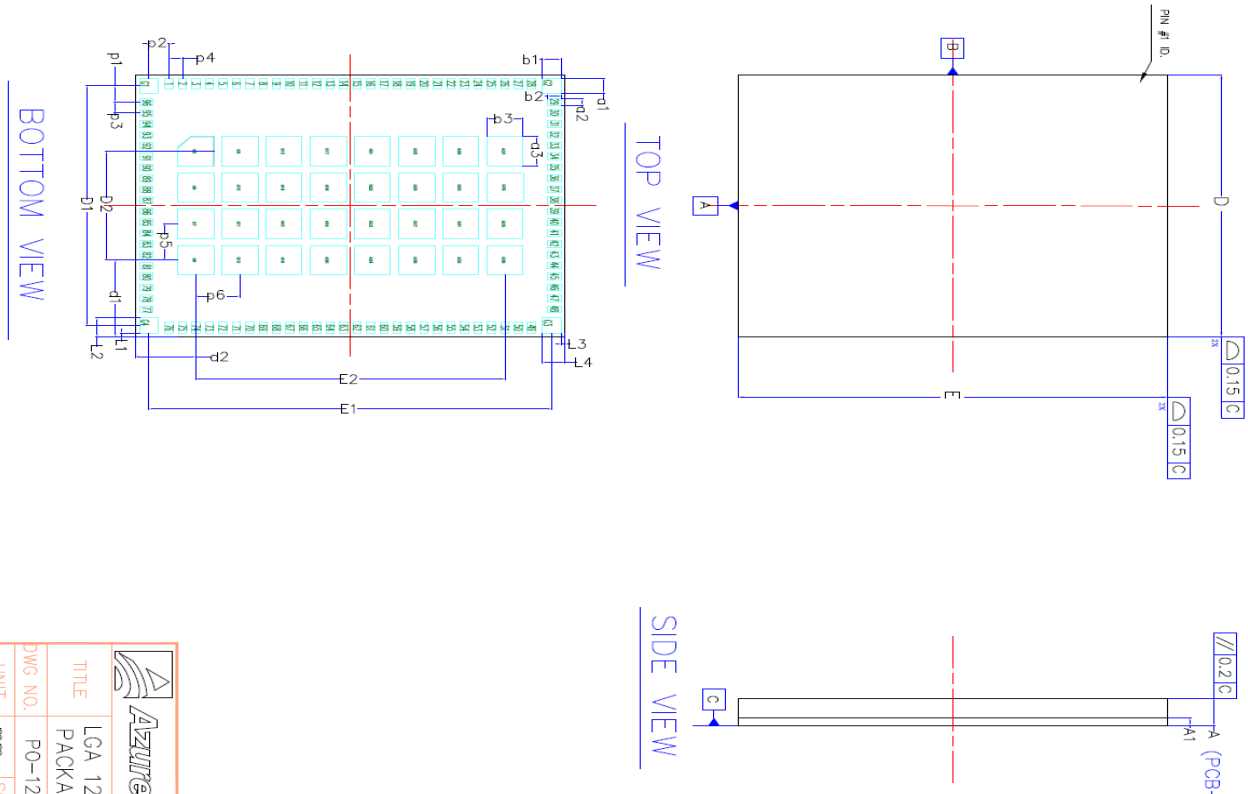
5. Mechanical Information

5-1. Package Outline Drawing



5-2. Module Footprint

AW-CM389NF PCB Layout Footprint



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.156	1.256	1.356	0.046	0.049	0.053
A1	0.316	0.356	0.396	0.012	0.014	0.016
D	11.900	12.000	12.100	0.469	0.472	0.476
D1	–	11.000BSC	–	–	0.433BSC	–
D2	–	4.987BSC	–	–	0.196BSC	–
E	15.900	16.000	16.100	0.626	0.630	0.634
E1	–	15.000BSC	–	–	0.591BSC	–
E2	–	11.520BSC	–	–	0.454BSC	–
p1	–	0.750BSC	–	–	0.030BSC	–
p2	–	0.750BSC	–	–	0.030BSC	–
p3	–	0.500BSC	–	–	0.020BSC	–
p4	–	0.500BSC	–	–	0.020BSC	–
p5	–	1.662BSC	–	–	0.065BSC	–
p6	–	1.650BSC	–	–	0.065BSC	–
d1	3.456	3.506	3.556	0.136	0.138	0.140
d2	2.190	2.240	2.290	0.086	0.088	0.090
d1	0.650	0.700	0.750	0.026	0.028	0.030
q2	0.250	0.300	0.350	0.010	0.012	0.014
q3	1.300	1.350	1.400	0.051	0.053	0.055
b1	0.650	0.700	0.750	0.026	0.028	0.030
b2	0.450	0.500	0.550	0.018	0.020	0.022
b3	1.300	1.350	1.400	0.051	0.053	0.055
L1	0.100	0.150	0.200	0.004	0.006	0.008
L2	0.800	0.850	0.900	0.031	0.033	0.035
L3	0.100	0.150	0.200	0.004	0.006	0.008
L4	0.800	0.850	0.900	0.031	0.033	0.035

ALL DIMENSIONS ARE IN MILLIMETERS.

AzureWave Technologies(Shanghai) Inc.

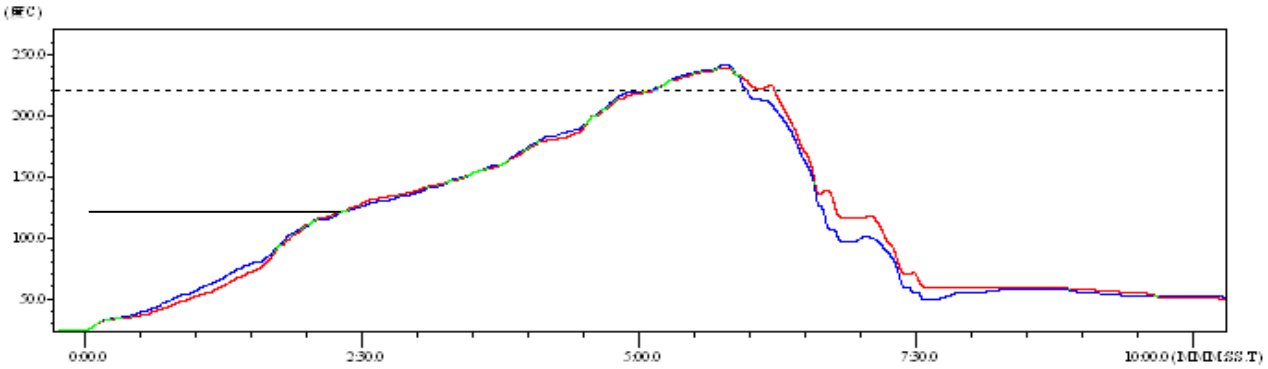
TITLE	LGA 12x16x0.356 132PIN PACKAGE OUTLINE DWG	DRN	Merry Pan 25/Dec/13
		DEN	Merry Pan 25/Dec/13
DWG NO.	PO-12801-01	REV.	00
		CHK	
UNIT	mm	SCALE	1:1
		PAGE	2/2
		APD	

NR.TOL: NA

6. Package Information

6-1. Recommended Reflow Profile

Reflow Soldering Profile



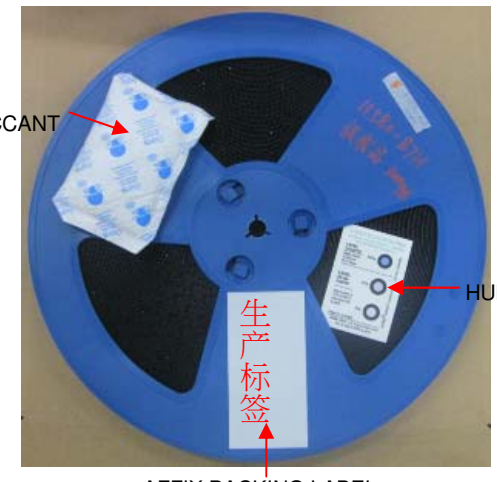
No	Item	Temperature(℃)	Time(sec)
1	Reflow Time	Time of above 220℃	35~55sec
2	Peak-Temp	260℃ max	

Note:

1. **Recommend to supply N_2 for reflow oven**
2. **N_2 atmosphere during reflow (O_2<300ppm)**

7. Shipping Information

7-1



7-2

7-3

7-4

7-5

1 Carton= 5 Boxes

7-6

AFFIX PACKING LABEL

Note: 1 tape reel = 1 box = 1,500pcs

1 carton = 5 boxes = 5 * 1,500pcs=7,500pcs

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Operations in the 5.15-5.25GHz band are restricted to indoor usage only.

Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling
This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains FCC ID: TLZ-CM389NF. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Manual Information To the End User
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

低功率電波輻射性電機管理辦法

第十二條 經型式認證合格之低功率射頻電機，非經許可，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。

第十四條 低功率射頻電機之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。

前項合法通信，指依電信法規定作業之無線電通信。

低功率射頻電機須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

在 5.25-5.35 秭赫頻帶內操作之無線資訊傳輸設備，限於室內使用。

1. 本模組於取得認證後將依規定於模組本體標示審驗合格標籤。

2. 系統廠商應於平台上標示「本產品內含射頻模組：  XXXyyyLPDzzzz-x」字樣。

Industry Canada statement:

This device complies with RSS-210 of the Industry Canada Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Ce dispositif est conforme à la norme CNR-210 d'Industrie Canada applicable aux appareils radio exempts de licence. Son fonctionnement est sujet aux deux conditions suivantes: (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

Radiation Exposure Statement:

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling
This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 6100A-CM389NF

Plaque signalétique du produit final
Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 6100A-CM389NF

Manual Information To the End User
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final
L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.