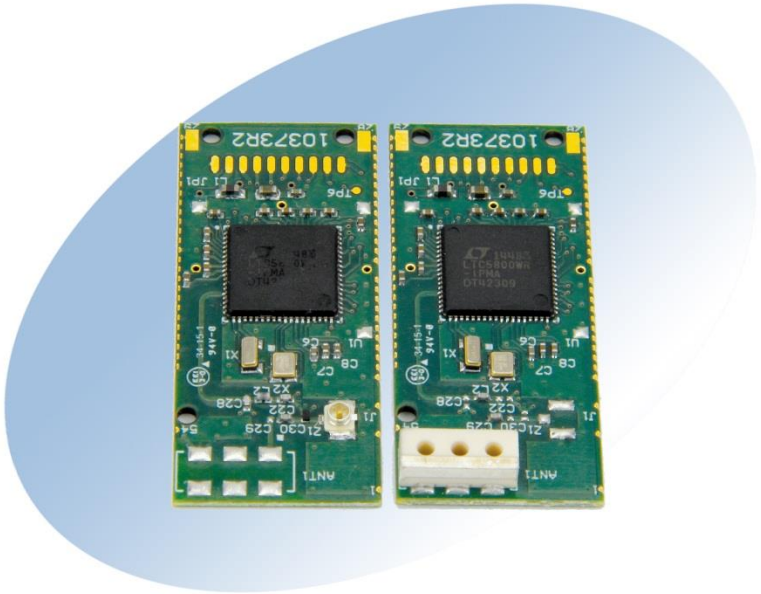
SmartMesh® IP Node 2.4GHz

(MESH RF IoT Module)

802.15.4e Wireless Node Module



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NETWORK FEATURES

Complete **Radio Transceiver, Embedded Processor**, and **Networking Software** for Forming a Self-Healing Mesh Network

SmartMesh® Networks Incorporate:

- Time Synchronized Network-Wide Scheduling
- Per Transmission Frequency Hopping
- Redundant Spatially Diverse Topologies
- Network-Wide Reliability and Power Optimization
- NIST Certified Security

SmartMesh Networks Deliver:

- >99.999% Network Reliability Achieved in the Most Challenging RF Environments
- Sub 50µA Routing Nodes

Compliant to 6LoWPAN Internet Protocol (IP) and IEEE 802.15.4e Standards

505-10368-00/505-10369-00 FEATURES

Industry-Leading Low Power Radio Technology with:

- 4.5mA to Receive a Packet
- 5.4mA to Transmit at 0dBm
- 9.7mA to Transmit at 8dBm

RF Modular Certifications include USA, Canada, EU and Japan.

PCB Assembly with Chip Antenna (505-10368-00) or with U.FL Antenna Connector (505-10369-00).

DESCRIPTION

SmartMesh IP™ wireless sensor networks are self-managing, low power Internet Protocol (IP) networks built from wireless nodes called motes. The 505-10368-00/505-10369-00 is the IP mote product in the WSM2400®* family of IEEE 802.15.4e printed circuit board assembly solutions, featuring a highly-integrated, low power radio as well as an ARM Cortex-M3 32-bit microprocessor running Dust's embedded SmartMesh IP networking software.

Both the 505-10368-00 (with chip antenna) and the 505-10369-00 (with U.FL connector), are designed for surface mount assembly. With Dust's time-synchronized SmartMesh IP networks, all motes in the network may route, source or terminate data, while providing many years of battery powered operation. The SmartMesh IP software provided with the 505-10368-00/505-10369-00 is fully tested and validated, and is readily configured via a software Application Programming Interface.

SmartMesh IP motes deliver a highly flexible network with proven reliability and low power performance in an easy-to-integrate platform.

SMARTMESH NETWORK OVERVIEW

A SmartMesh network consists of a self-forming multi-hop mesh of nodes, known as motes, which collect and relay data, and a network manager that monitors and manages network performance and security, and exchanges data with a host application.

SmartMesh networks communicate using a time slotted channel hopping (TSCH) link layer, pioneered by Dust Networks. In a TSCH network, all motes in the network are synchronized to within less than a millisecond. Time in the network is organized into time slots, which enables collision-free packet exchange and per-transmission channel-hopping. In a SmartMesh network, every device has one or more parents (e.g. mote 3 has motes 1 and 2 as parents) that provide redundant paths to overcome communications interruption due to interference, physical obstruction or multi-path fading. If a packet transmission fails on one path, the next retransmission may try on a different path and different RF channel.

A network begins to form when the network manager instructs its on-board Access Point (AP) radio to begin sending advertisements—packets that contain information that enables a device to synchronize to the network and request to join. This message exchange is part of the security handshake that establishes encrypted communications between the manager or application, and mote. Once motes have joined the network, they maintain synchronization through time corrections when a packet is acknowledged.

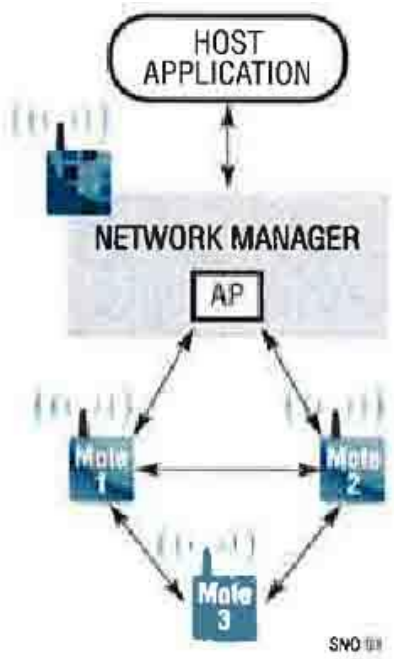

Figure 1. Mesh Network

An ongoing discovery process ensures that the network continually discovers new paths as the RF conditions change. In addition, each mote in the network tracks performance statistics (e.g. quality of used paths, and lists of potential paths) and periodically sends that information to the network manager in packets called health reports.

The Network Manager uses health reports to continually optimize the network to maintain >99.999% data reliability even in the most challenging RF environments. The use of TSCH allows SmartMesh devices to sleep in between scheduled communications and draw very little power in this state. Motes are only active in time slots where they are scheduled to transmit or receive, typically resulting in a duty cycle of < 1%. The optimization software in the Network Manager coordinates this schedule automatically. When combined with the WSM2400 low power radio, every mote in a SmartMesh network—even busy routing ones—can run on batteries for years. By default, all motes in a network are capable of routing traffic from other motes, which simplifies installation by avoiding the complexity of having distinct routers vs non-routing end nodes. Motes may be configured as non-routing to further reduce that particular mote's power consumption and to support a wide variety of network topologies.

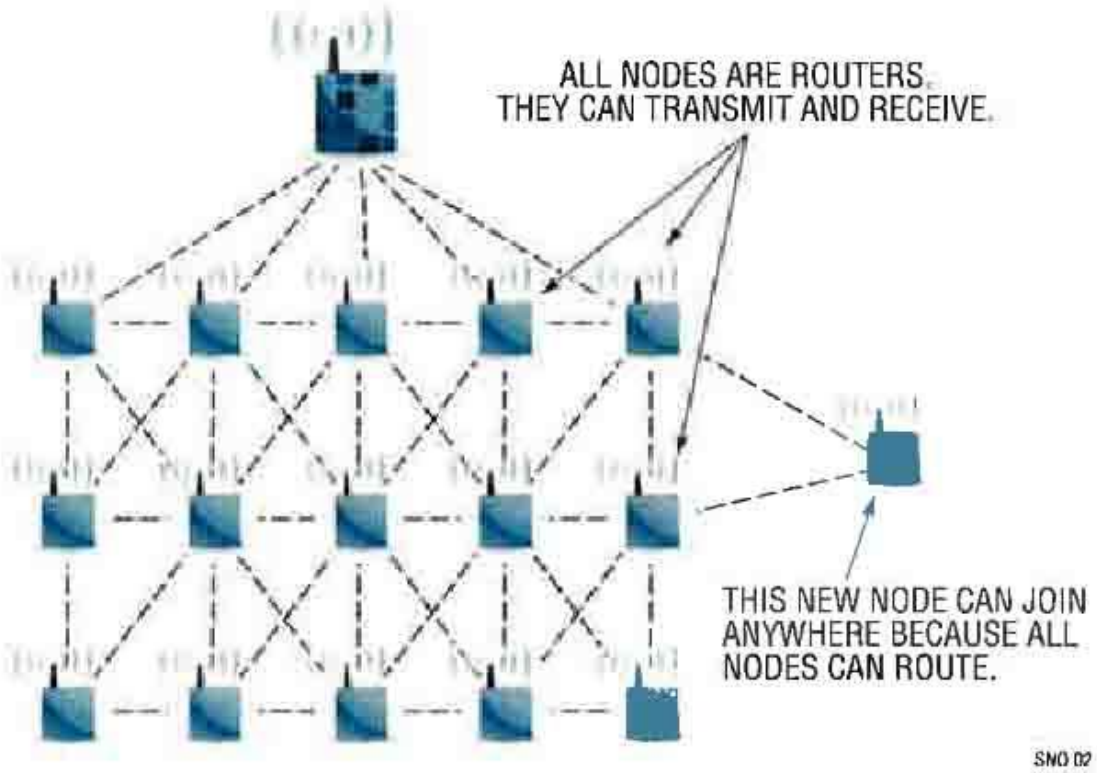

Figure 2. Mesh network

At the heart of SmartMesh motes and network managers is the WSM2400 IEEE 802.15.4e System-on-Chip (SoC), featuring Dust Networks' highly integrated, low power radio design, plus an ARM Cortex-M3 32-bit microprocessor running SmartMesh networking software. The SmartMesh networking software comes fully compiled yet is configurable via a rich set of Application Programming Interfaces (APIs) which allows a host application to interact with the network, e.g. to transfer information to a device, to configure data publishing rates on one or more motes, or to monitor network state or performance metrics. Data publishing can be uniform or different for each device, with motes being able to publish infrequently or faster than once per second as needed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage on VSUPPLY.....3.76V

Input Voltage on AI_0/1/2/3 Inputs.....1.80V

Voltage on Any Digital I/O pin..... –0.3V to VSUPPLY + 0.3V

Input RF Level..... +10dBm

Storage Temperature Range (Note 3)..... –55°C to 105°C

Operating Temperature Range.....–40°C to 85°C

CAUTION: This part is sensitive to electrostatic discharge (ESD). It is very important that proper ESD precautions be observed when handling the 505-10368-00/505-10369-00.

RECOMMENDED OPERATING CONDITIONS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VSUPPLY	Supply Voltage	Including Noise and Load Regulation	●	2.1		3.76	V
	Supply Noise	50Hz to 2MHz	●			250	mV
	Operating Relative Humidity	Non-Condensing	●	10		90	% RH
	Temperature Ramp Rate While Operating in Network		●	–8		+8	°C/min

Table 1. Recommended operating conditions

DC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

OPERATION/STATE	CONDITIONS		MIN	TYP	MAX	UNITS
Power-on Reset	During Power-On Reset, Maximum 750µs + VSUPPLY Rise Time from 1V to 1.9V			12		mA
Doze	RAM on, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Active			1.2		µA
Deep Sleep	RAM on, ARM Cortex-M3, Flash, Radio, and Peripherals Off, All Data and State Retained, 32.768kHz Reference Inactive			0.8		µA
In-Circuit Programming	RESETn and FLASH_P_ENn Asserted, IPCS_SCK at 8MHz			20		mA
Peak Operating Current +8dBm +0dBm	System Operating at 14.7MHz, Radio Transmitting, During Flash Write. Maximum Duration 4.33 ms.			 30 26		 mA mA
Active	ARM Cortex M3, RAM and Flash Operating, Radio and All Other Peripherals Off. Clock Frequency of CPU and Peripherals Set to 7.3728MHz, VCORE = 1.2V			1.3		mA
Flash Write	Single Bank Flash Write			3.7		mA
Flash Erase	Single Bank Page or Mass Erase			2.5		mA
Radio Tx +0dBm +8dBm	Current with Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to 7.3728MHz.			 5.4 9.7		 mA mA
Radio Rx	Current with Autonomous MAC Managing Radio Operation, CPU Inactive. Clock Frequency of CPU and Peripherals Set to			4.5		mA

Table 2. DC characteristics

RADIO SPECIFICATIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency Band		●	2.4000		2.4835	GHz
Number of Channels		●		15		
Channel Separation		●		5		MHz
Channel Center Frequency	Where k = 11 to 25, as Defined by IEEE 802.4.15	●		2405 + 5•(k-11)		MHz
Modulation	IEEE 802.15.4 Direct Sequence Spread Spectrum (DSSS)					
Raw Data Rate		●		250		kbps
Range (Note 4) Indoor Outdoor Free Space	25°C, 50% RH, +2dBi Omni-Directional Antenna, Antenna 2m Above Ground			 100 300 1200		 m m m

Table 3. Radio specifications

RADIO RECEIVER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Sensitivity	Packet Error Rate (PER) = 1% (Note 5)		–93		dBm
Receiver Sensitivity	PER = 50%		–95		dBm
Saturation	Maximum Input Level the Receiver Will Properly Receive Packets		0		dBm
Adjacent Channel Rejection (High Side)	Desired Signal at –82dBm, Adjacent Modulated Channel 5MHz Above the Desired Signal, PER = 1% (Note 5)		22		dBc
Adjacent Channel Rejection (Low Side)	Desired Signal at –82dBm, Adjacent Modulated Channel 5MHz Below the Desired Signal, PER = 1% (Note 5)		19		dBc
Alternate Channel Rejection (High Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Above the Desired Signal, PER = 1% (Note 5)		40		dBc
Alternate Channel Rejection (Low Side)	Desired Signal at –82dBm, Alternate Modulated Channel 10MHz Below the Desired Signal, PER = 1% (Note 5)		36		dBc
Second Alternate Channel Rejection	Desired Signal at –82dBm, Second Alternate Modulated Channel Either 15MHz Above or Below, PER = 1% (Note 5)		42		dBc
Co-Channel Rejection	Desired Signal at –82dBm, Undesired Signal is an 802.15.4 Modulated Signal at the Same Frequency, PER = 1%		–6		dBc
LO Feed Through			–55		dBm
Frequency Error Tolerance (Note 6)			±50		ppm
Symbol Error Tolerance			±50		ppm
Received Signal Strength Indicator (RSSI) Input Range			–90 to –10		dBm
RSSI Accuracy			±6		dB
RSSI Resolution			1		dB

Table 4. Radio receiver characteristics

RADIO TRANSMITTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Power	Delivered to a 50Ω load				
High Calibrated Setting			8		dBm
Low Calibrated Setting			0		dBm
Spurious Emissions	Conducted Measurement with a 50Ω Single-Ended Load, +8dBm Output Power. All Measurements Made with Max Hold.				
30MHz to 1000MHz	R_{BW} = 120kHz, V_{BW} = 100Hz		<–70		dBm
1GHz to 12.75GHz	R_{BW} = 1MHz, V_{BW} = 3MHz		–45		dBm
2.4GHz ISM Upper Band Edge (Peak)	R_{BW} = 1MHz, V_{BW} = 3MHz		–37		dBm
2.4GHz ISM Upper Band Edge (Average)	R_{BW} = 1MHz, V_{BW} = 10Hz		–49		dBm
2.4GHz ISM Lower Band Edge	R_{BW} = 100kHz, V_{BW} = 100kHz		–45		dBc
Harmonic Emissions	Conducted Measurement Delivered to a 50Ω Load, Resolution Bandwidth = 1MHz, Video Bandwidth = 1MHz				
2nd Harmonic			–50		dBm
3rd Harmonic			–45		dBm

Table 5. Radio transmitter characteristics

DIGITAL I/O CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 7)		MIN	TYP	MAX	UNITS
V_{IL}	Low Level Input Voltage		●	–0.3		0.6	V
V_{IH}	High Level Input Voltage	(Note 8)	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
V_{OL}	Low Level Output Voltage	Type 1, $I_{OL(MAX)}$ = 1.2mA	●			0.4	V
		Type 2, Low Drive, $I_{OL(MAX)}$ = 2.2mA	●			0.4	V
		Type 2, High Drive, $I_{OL(MAX)}$ = 4.5mA	●			0.4	V
V_{OH}	High Level Output Voltage	Type 1, $I_{OH(MAX)}$ = –0.8mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
		Type 2, Low Drive, $I_{OH(MAX)}$ = –1.6mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
		Type 2, High Drive, $I_{OH(MAX)}$ = –3.2mA	●	VSUPPLY – 0.3		VSUPPLY + 0.3	V
	Input Leakage Current	Input Driven to VSUPPLY or GND			50		nA
	Pull-Up/Pull-Down Resistance				50		kΩ

Table 6. Digital I/O characteristics

TEMPERATURE SENSOR CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Offset	Temperature Offset Error at 25°C			±0.25		°C
Slope Error				±0.033		°C/°C

Table 7. Temperature sensor characteristics

ANALOG INPUT CHAIN CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Variable Gain Amplifier						
	Gain			1		8	
	Gain Error					2	%
	Offset-Digital to Analog Converter (DAC)						
	Full-Scale				1.80		V
	Resolution				4		Bits
DNL	Differential Non-Linearity					2.7	mV
	Analog to Digital Converter (ADC)						
	Full-Scale, Signal				1.80		V
	Resolution				1.8		mV
	Offset	Mid-Scale			1.4	12	LSB
DNL	Differential Non-Linearity					1	LSB
INL	Integral Non-Linearity					1	LSB
	Settling Time	10kΩ Source Impedance				10	µs
	Conversion Time					20	µs
	Current Consumption				40		µA
	Analog Inputs (Note 9)						
	Load				20		pF
	Series Input Resistance				1		kΩ

Table 8. Analog input characteristics

SYSTEM CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Doze to Active State Transition				5		µs
	Doze to Radio Tx or Rx				1.2		ms
Q_{CCA}	Charge to Sample RF Channel RSSI	Charge Consumed Starting from Doze State and Completing an RSSI Measurement			4		µC
Q_{MAX}	Largest Atomic Charge Operation	Flash Erase, 21ms Max Duration	●			200	µC
	RESETn Pulse Width		●	125			µs
	Total Capacitance					6	µF
	Total Inductance					3	µH

Table 9. System characteristics

UART AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Permitted R_X Baud Rate Error	Both Application Programming Interface (API) and Command Line Interface (CLI) UARTs	●	–2		2	%
	Generated T_X Baud Rate Error	Both API and CLI UARTs	●	–1		1	%
$t_{RX\_RTS\ to\ RX\_CTS}$	Assertion of UART_RX_RTSn to Assertion of UART_RX_CTSn, or Negation of UART_RX_RTSn to Negation of UART_RX_CTSn		●	0		2	ms
$t_{CTS\_R\ to\ RX}$	Assertion of UART_RX_CTSn to Start of Byte		●	0		20	ms
$t_{EOP\ to\ RX\_RTS}$	End of Packet (End of the Last Stop Bit) to Negation of UART_RX_RTSn		●	0		22	ms
$t_{BEG\_TX\_RTS\ to\ TX\_CTS}$	Assertion of UART_TX_RTSn to Assertion of UART_TX_CTSn		●	0		22	ms
$t_{END\_TX\_CTS\ to\ TX\_RTS}$	Negation of UART_TX_CTSn to Negation of UART_TX_RTSn			2			Bit Period
$t_{TX\_CTS\ to\ TX}$	Assertion of UART_TX_CTSn to Start of Byte		●	0		2	Bit Period
$t_{EOP\ to\ TX\_RTS}$	End of Packet (End of the Last Stop Bit) to Negation of UART_TX_RTSn		●	0		1	Bit Period
$t_{RX\_INTERBYTE}$	Receive Inter-Byte Delay		●			100	ms
$t_{TX\ to\ TX\_CTS}$	Start of Byte to Negation of UART_TX_CTSn		●	0			ns

Table 10. UART AC characteristics

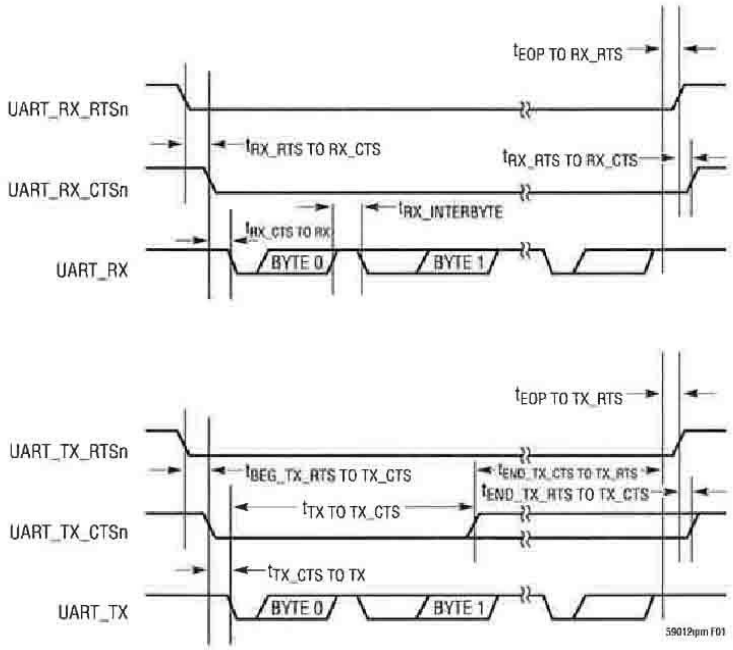

Figure 3. API UART Timing

TIMEn AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{STROBE}	TIMEn Signal Strobe Width		●	125			µs
$t_{RESPONSE}$	Delay from Rising Edge of TIMEn to the Start of Time Packet on API UART		●	0		100	ms
t_{TIME_HOLD}	Delay from End of Time Packet on API UART to Falling Edge of Subsequent TIMEn		●	0			ns
	Timestamp Resolution (Note 10)		●		1		µs
	Network-Wide Time Accuracy (Note 11)		●		±5		µs

Table 11. Timen AC characteristics

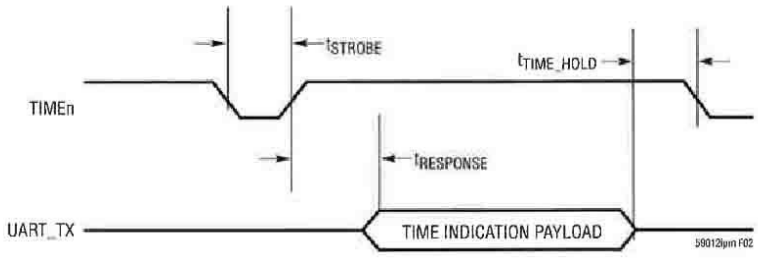

Figure 4. Timestamp Timing

RADIO_INHIBIT AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{RADIO_OFF}	Delay from Rising Edge of RADIO_INHIBIT to Radio Disabled		●			20	ms
$t_{RADIO\_INHIBIT\_STROBE}$	Maximum RADIO_INHIBIT Strobe Width		●			2	s

Table 12. Radio inhibit ac characteristics

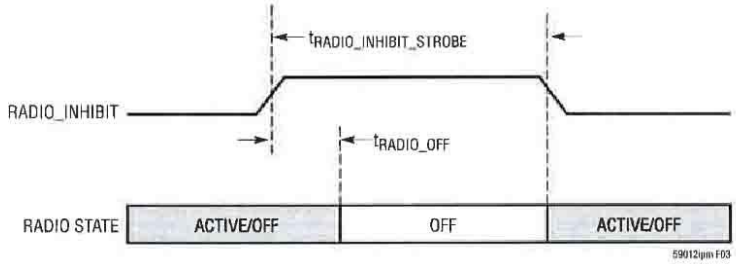

Figure 5. Radio Inhibit Timing

FLASH AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{WRITE}	Time to Write a 32-Bit Word (Note 12)		●			21	µs
t_{PAGE_ERASE}	Time to Erase a 2kB Page (Note 12)		●			21	ms
t_{MASS_ERASE}	Time to Erase 256kB Flash Bank (Note 12)		●			21	ms
	Data Retention	25°C 85°C 105°C		100 20 8			Years Years Years

Table 13. Flash AC characteristics

FLASH SPI SLAVE AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VSUPPLY = 3.6V unless otherwise noted. (Note 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{FP\_EN\_to\_RESET}$	Setup from Assertion of FLASH_P_ENn to Assertion of RESETn		●	0			ns
t_{FP_ENTER}	Delay from the Assertion RESETn to the First Falling Edge of IPCS_SSn		●	125			µs
t_{FP_EXIT}	Delay from the Completion of the Last Flash SPI Slave Transaction to the Negation of RESETn and FLASH_P_ENn		●	10			µs
t_{SSS}	IPCS_SSn Setup to the Leading Edge of IPCS_SCK		●	15			ns
t_{SSH}	IPCS_SSn Hold from Trailing Edge of IPCS_SCK		●	15			ns
t_{CK}	IPCS_SCK Period		●	50			ns
t_{DIS}	IPCS_MOSI Data Setup		●	15			ns
t_{DIH}	IPCS_MOSI Data Hold		●	5			ns
t_{DOV}	IPCS_MISO Data Valid		●	3			ns
t_{OFF}	IPCS_MISO Data Tri-State		●	0		30	ns

Table 14. Flash SPI slave characteristics

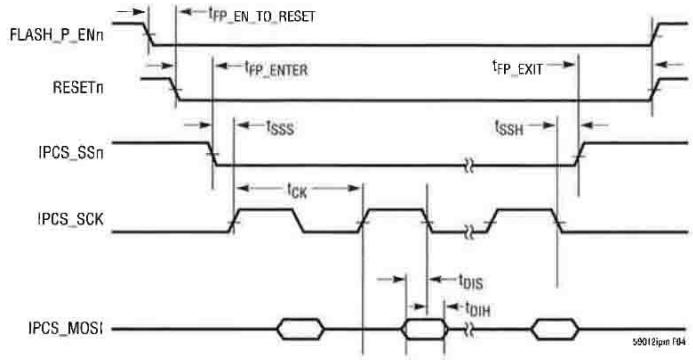

Figure 6. Flash programming interface timing

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: ESD (electrostatic discharge) sensitive device. ESD protection devices are used extensively internal to WSM2400. However, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 3: Extended storage at high temperature is discouraged, as this negatively affects the data retention of WSM2400's calibration data. See the FLASH Data Retention section for details.

Note 4: Actual RF range is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, and near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, range varies.

Note 5: As Specified by IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs) http://standards.ieee.org/findstds/standard/802.15.4-2011.html.

Note 6: IEEE Std. 802.15.4-2006 requires transmitters to maintain a frequency tolerance of better than ±40 ppm.

Note 7: Per-pin I/O types are provided in the Pin Functions section.

Note 8: VIH maximum voltage input must respect the VSUPPLY maximum voltage specification.

Note 9: The analog inputs to the ADC can be modeled as a series resistor to a capacitor. At a minimum the entire circuit, including the source impedance for the signal driving the analog input should be designed to settle to within ¼ LSB within the sampling window to match the performance of the ADC..

Note 10: Network time accuracy is a statistical measure and varies over the temperature range, reporting rate and the location of the device relative to the manager in the network. See the Typical Performance Characteristics section for a more detailed description.

Note 11: Code execution from flash banks being written or erased is suspended until completion of the flash operation.

Note 12: Guaranteed by design. Not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

Network motes typically route through at least two parents the traffic destined for the manager. The supply current graphs shown in Figure 8 include a parameter called descendants. In these graphs the term descendants is short for traffic-weighted descendants and refers to an amount of activity equivalent to the number of descendants if all of the network traffic directed to the mote in question. Generally the number of descendants of a parent is more typically 2x or more, than the number of traffic-weighted descendants. For example, with reference to Figure 7, Network Graph mote P1 has 0.75 traffic-weighted descendants. To obtain this value notice that mote D1 routes half its packets through mote P1 adding 0.5 to the traffic weighted descendant value; the other half of D1's traffic is routed through its other parent, P2. Mote D2 routes half its packets through mote D1 (the other half going through parent P3), which we know routes half its packets to moteP1, adding another 0.25 to the traffic-weighted descendant value for a total traffic-weighted descendant value of 0.75

As described in the Application Time Synchronization section, WSM2400 provides two mechanisms for applications to maintain a time base across a network. The synchronization performance plots that follow were generated using the more precise TIMEn input. Publishing rate is the rate a mote application sends upstream data. Synchronization improves as the publishing rate increases. Baseline synchronization performance is provided for a network operating with a publishing rate of zero. Actual performance for applications in network will improve as publishing rates increase. All synchronization testing was performed with the 1-hop mote inside a temperature chamber. Timing errors due to temperature changes and temperature differences both between the manager and this mote and between this mote and its descendants therefore propagated down through the network. The synchronization of the 3-hop and 5-hop motes to the manager was then affected by the temperature ramps even though they were at room temperature. For 2°C/minute testing the temperature chamber was cycled between –40°C and 85°C at this rate for 24 hours. For 8°C/minute testing, the temperature chamber was rapidly cycled between 85°C and 45°C for 8 hours, followed by rapid cycling between –5°C and 45°C for 8 hours, and lastly, rapid cycling between –40°C and 15°C for 8 hours.

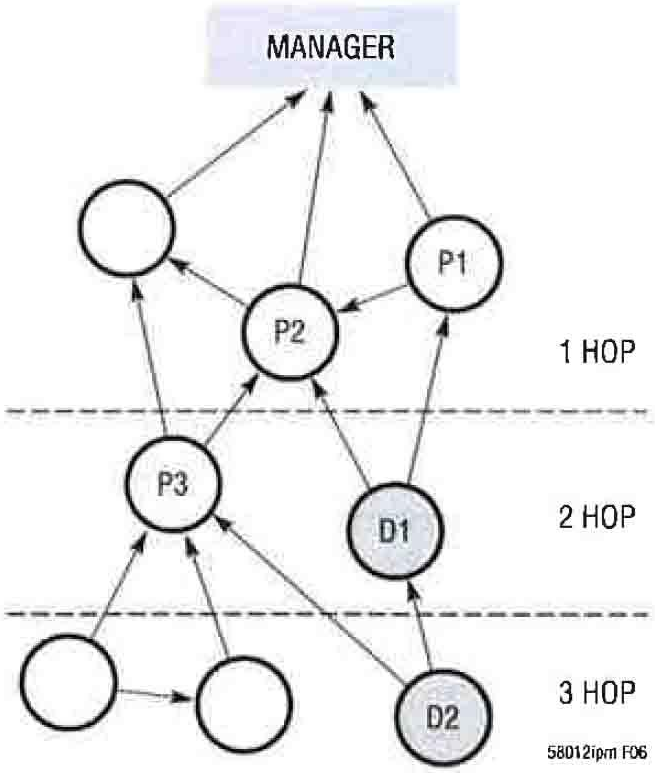

Figure 7. Mesh network

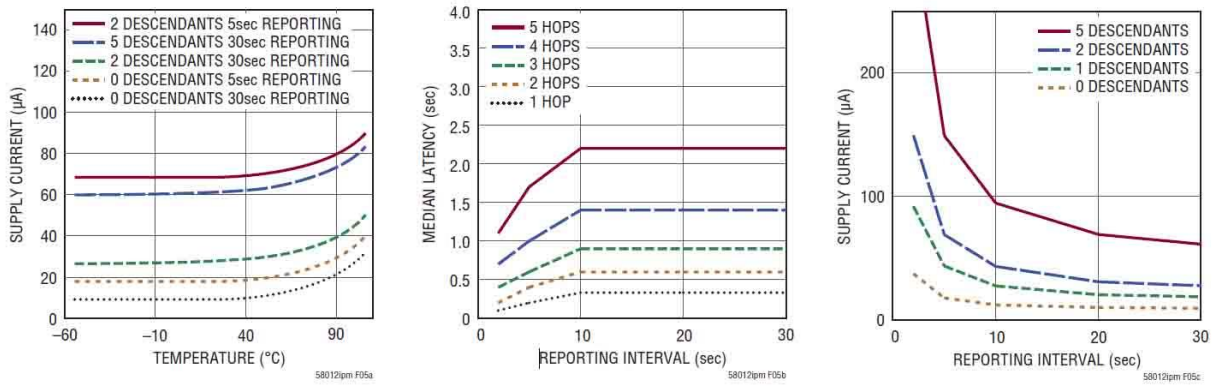

Figure 8. Example network graphs

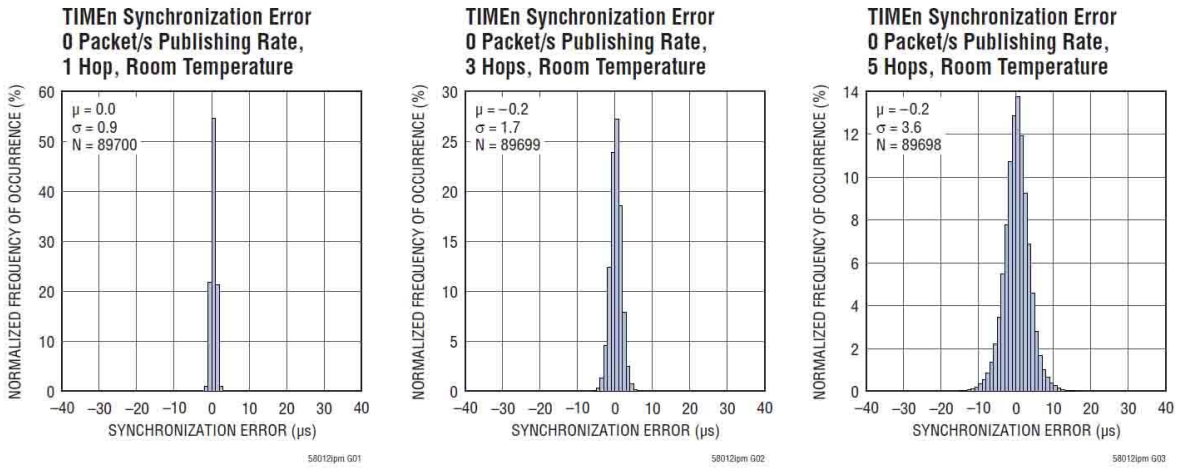

Figure 9.

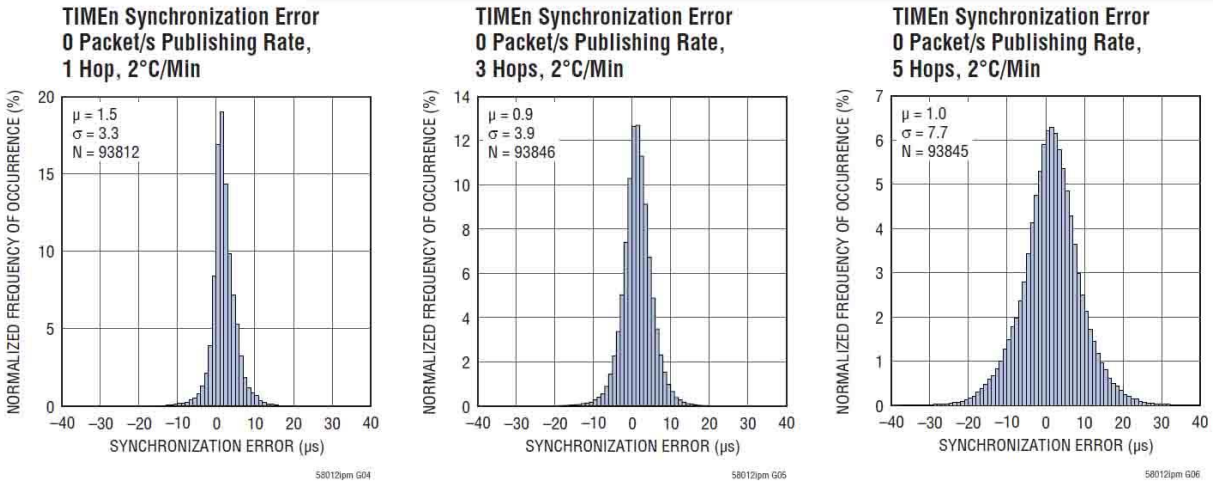

Figure 10.

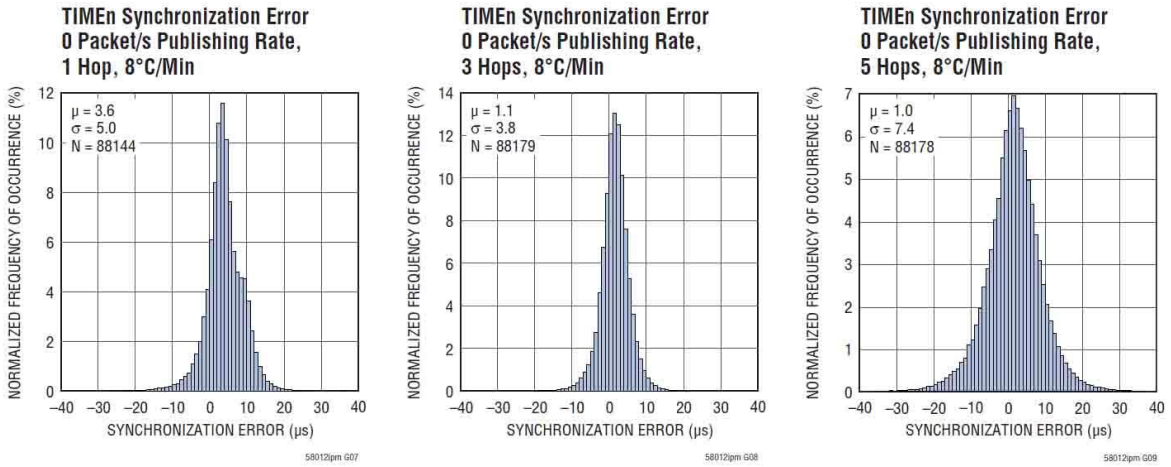

Figure 11.

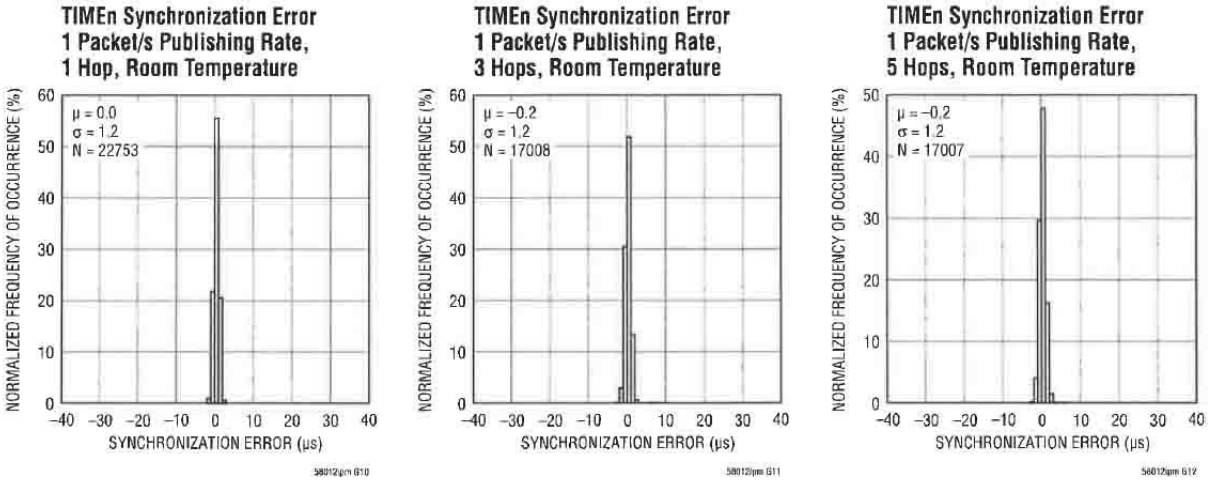

Figure 12.

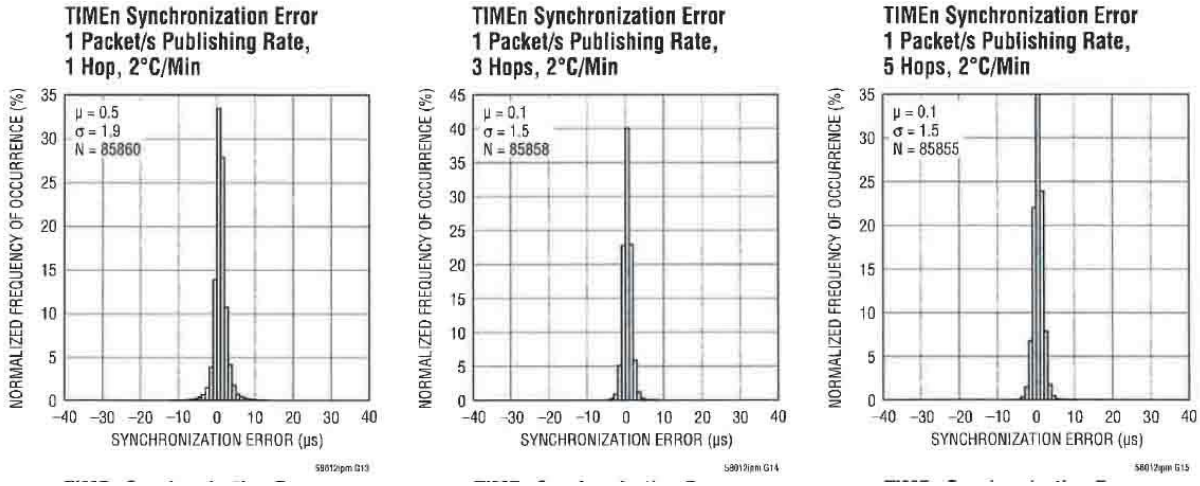

Figure 13.

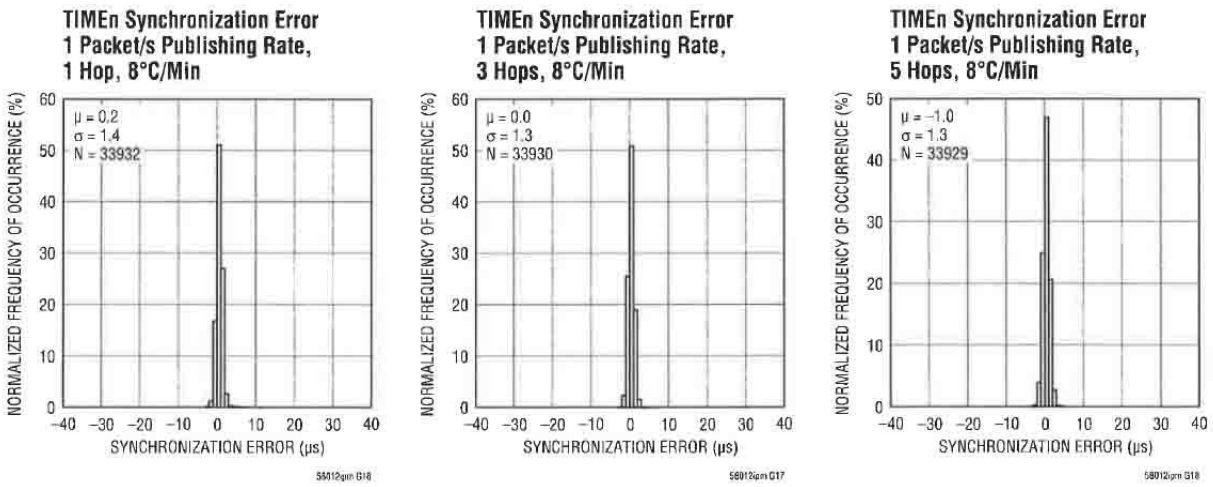

Figure 14.

As described in the SmartMesh Network Overview section, devices in network spend the vast majority of their time inactive in their lowest power state (doze). On a synchronous schedule a mote will wake to communicate with another mote. Regularly occurring sequences which wake, perform a significant function and return to sleep are considered atomic. These operations are considered atomic as the sequence of events cannot be separated into smaller events while performing a useful function. For example, transmission of a packet over the radio is an atomic operation. Atomic operations may be characterized in either charge or energy. In a time slot where a mote successfully sends a packet, an atomic transmit includes setup prior to sending the message, sending the message, receiving the acknowledgment and the post processing needed as a result of the message being sent. Similarly in a time slot when a mote successfully receives a packet, an atomic receive includes setup prior to listening, listening until the start of the packet transition, receiving the packet, sending the acknowledge and the post processing required due to the arrival of the packet.

To ensure reliability each mote in the network is provided multiple time slots for each packet it nominally will send and forward. The time slots are assigned to communicate upstream with at least two different motes. When combined with frequency hopping this provides temporal, special and spectral redundancy. Given this approach a mote will often listen for a message that it will never receive, since the time slot is not being used by the transmitting mote. It has already successfully transmitted the packet. Since typically 3 time slots are scheduled for every 1 packet to be sent or forwarded, motes will perform more of these atomic “idle listens” than atomic transmit or atomic receive sequences. Examples of transmit, receive and idle listen atomic operations are shown below.

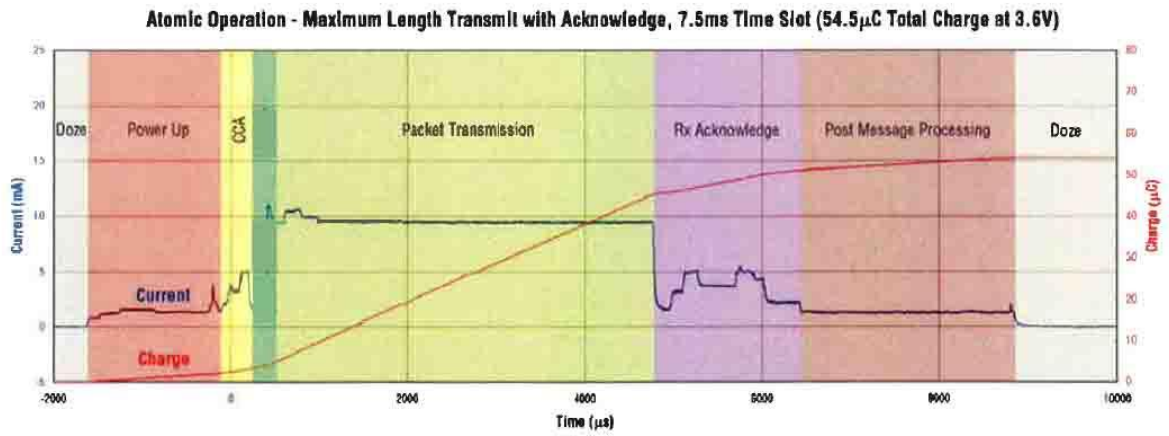

Figure 15.

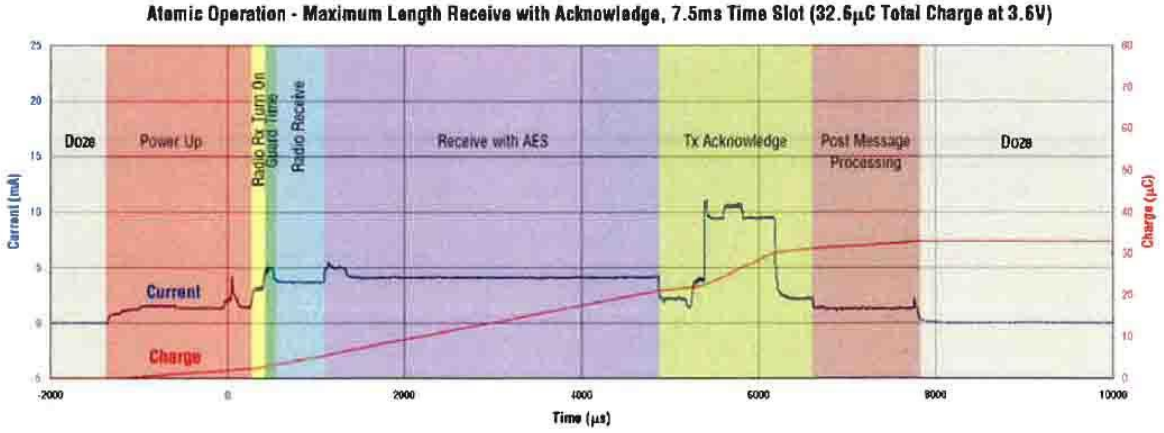

Figure 16

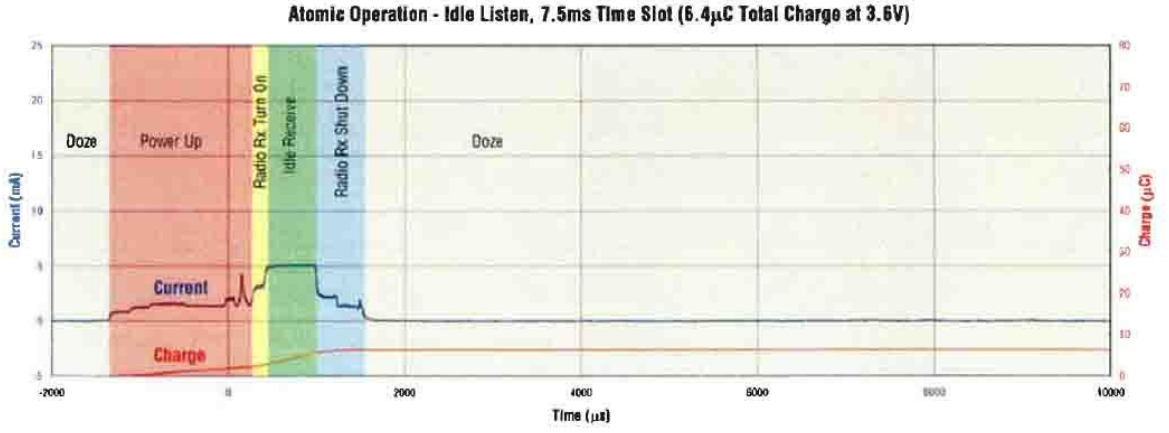

Figure 17

PIN FUNCTIONS

The following table organizes the pins by functional groups. For those I/O with multiple functions the alternate functions are shown on the second and third line in their respective row. The **No** column provides the pin number. The second column lists the function. The **Type** column lists the I/O type. The **I/O** column lists the direction of the signal relative to WSM2400. The **Pull** column shows which signals have a fixed passive pull-up or pull-down. The **Description** column provides a brief signal description.

NOTE: Pin functions shown in italics are currently not supported in software

No.	Power Supply	Type	I/0	PULL	Description
1	GND	Power	-	-	Ground Connection
2	GND	Power	-	-	Ground Connection
3	GND	Power	-	-	Ground Connection
4	GND	Power	-	-	Ground Connection
15	GND	Power	-	-	Ground Connection
28	GND	Power	-	-	Ground Connection
29	GND	Power	-	-	Ground Connection
41	GND	Power	-	-	Ground Connection
53	GND	Power	-	-	Ground Connection
54	GND	Power	-	-	Ground Connection
35	VSUPPLY	Power	-	-	Power Supply Input to WSM2400

No.	Radio	Type	I/0	PULL	Description
37	RADIO_INHIBIT GPIO15	1(Note 14)	I I/O	-	Radio Inhibit General Purpose Digital I/O
39	GPIO17	1	I/O	-	General Purpose Digital I/O
40	GPIO18	1	I/O	-	General Purpose Digital I/O
42	GPIO19	1	I/O	-	General Purpose Digital I/O
-	Antenna	N/A	N/A	-	Chip Antenna/U.FL Connector

No.	Analog	Type	I/0	PULL	Description
43	AI_0	Analog	I	-	Analog Input 0
44	AI_1	Analog	I	-	Analog Input 1
46	AI_2	Analog	I	-	Analog Input 2
45	AI_3	Analog	I	-	Analog Input 3

No.	Reset	Type	I/0	PULL	Description
47	RESETn	1	I	UP	Reset input, Active Low

No.	JTAG	Type	I/0	PULL	Description
48	TDI	1	I	UP	JTAG Test Data In
49	TDO	1	O	-	JTAG Test Data Out
50	TMS	1	I	UP	JTAG Test mode Select
51	TCK	1	I	DOWN	JTAG Test Clock

No.	GPIOs (NOTE 14)	Type	I/0	PULL	Description
52	DP4 (GPIO23)	1	I/O	-	General Purpose Digital I/O
5	DP3 (GPIO22) *TIMER8_EXT*	1	I/O *I*	- -	General Purpose Digital I/O *External Input to 8-Bit Timer/Counter*
6	DP2 (GPIO21) *LPTIMER_EXT*	1	I/O *I*	- -	General Purpose Digital I/O *External Input to Low Power Timer/Counter*
8	DP0 (GPIO0) *SPIM-SS-2n*	1	I/O *O*	- -	General Purpose Digital I/O *SPI Master Slave Select 2, Active Low*
23	DP1 (GPIO20) *TIMER16_EXT*	1	I/O *I*	- -	General Purpose Digital I/O *External Input to 16-Bit Timer/Counter*

No.	SPECIAL PURPOSE	Type	I/0	PULL	Description
7	SLEEPn GPIO14	1(Note 14)	I I/O	- -	Deep Sleep, Active Low General Purpose Digital I/O
27	PWM0 *TIMER16_OUT* GPIO16	2	O *O* I/O	- - -	Pulse Width Modulator 0 *16-Bit Timer/Counter Match Output/PWM* General Purpose Digital I/O
36	TIMEn GPIO1	1(Note 14)	I I/O	- -	Time Capture Request, Active Low General Purpose Digital I/O

No.	CLI	Type	I/0	PULL	Description
9	UARTC0_TX	2	O	-	CLI UART 0 Transmit
11	UARTC0_RX	1	I	UP	CLI UART 0 Receive

No.	SPI MASTER	Type	I/0	PULL	Description
10	SPIM-MISO GPIO11	1	I I/O	- -	SPI Master(MISO) Master In Slave Out Port General Purpose Digital I/O
13	SPIM_MOSI GPIO10	2	O I/O	- -	SPI Master(MOSI) Master Out Slave In Port General Purpose Digital I/O
16	SPIM_SCK GPIO9	2	O I/O	- -	SPI Master(SCK) Serial Clock Port General Purpose Digital I/O
22	SPIM_SS_1n GPIO13	1	O I/O	- -	SPI Master Slave Select 1, Active Low General Purpose Digital I/O
18	SPIM-SS_0n GPIO12	1	O I/O	- -	SPI Master Slave Select 0, Active Low General Purpose Digital I/O

No.	IPCS SPI/FLASH PROGRAMMING	Type	I/0	PULL	Description
12	IPCS_MISO *TIMER16_OUT* GPIO6	2	I *O* I/O	- - -	SPI_Flash Emulation, Master In Slave Out *16-Bit Timer/Counter Math Output/PWM* General Purpose Digital I/O
14	IPCS_MOSI *TIMER16_EXT* GPIO5	1	I *I* I/O	- - -	SPI_Flash Emulation, Master Out Slave In *External Input to 16-Bit Timer/Counter* General Purpose Digital I/O
21	IPCS_SCK *TIMER8_EXT* GPIO4	1	I *I* I/O	- - -	SPI_Flash Emulation, Serial Clock *External Input to 8-Bit Timer/Counter* General Purpose Digital I/O
17	IPCS_SSn *LPTIMER_EXT* GPIO3	1	I *I* I/O	- - -	SPI_Flash Emulation Slave Select, Active Low *External Input to Low Power Timer/Counter* General Purpose Digital I/O
20	FLASH_P_ENn	1	I	UP	Flash Programming Enable, Active Low

No.	I^2C/1-WIRE/SPI SLAVE	Type	I/0	PULL	Description
19	SPIS_MISO UARTC1_TX 1_Wire	2	O O I/O	- - -	SPI Slave (MISO) Master In Slave Out CLI UART 1 Transmit 1 Wire Master
24	SPIS_MOSI UARTC1_RX GPIO26	1	I I I/O	- - -	SPI Slave (MOSI) Master Out Slave In CLI UART 1 Receive General Purpose Digital I/O
26	SPIS_SCK SCL	2	I I/O	- -	SPI Slave (SCK) Serial Clock I^2C Serial Clock
25	SPIS_SSn SDA	2	I I/O	- -	SPI Slave Select, Active Low I^2C Serial Data

No.	API UART	Type	I/0	PULL	Description
30	UART_RX_RTSn	1 (Note 14)	I	-	UART Receive, Request to Send, Active Low
31	UART_RX_CTSn	1	O	-	UART Receive, Clear to Send, Active Low
32	UART_RX	1 (Note 14)	I	-	UART Receive
33	UART_TX_RTSn	1	O	-	UART Transmit, Request to Send, Active Low
34	UART_TX_CTSn	1 (Note 14)	I	-	UART Transmit, Clear to Send, Active Low
38	UART_TX	2	O	-	UART Transmit

	Note 14: These inputs are always enabled and must be driven or pulled to a valid state to avoid leakage

	Note 15: See also pins 13, 18, and 23 for additional GPIO ports

VSUPPLY: System and I/O Power Supply. Provides power to the module. The digital-interface I/O voltages are also set by this voltage.

ANTENNA: Multiplexed Receiver Input and Transmitter Output Pin. The impedance presented to the U.FL connector should be 50Ω, single-ended with respect to ground.

AI_0, AI_1, AI_2, AI_3: Analog Inputs. These pins are multiplexed to the analog input chain. The analog input chain, as shown in Figure 18, is software-configurable and includes a variable-gain amplifier, an offset-DAC for adjusting input range, and a 10-bit ADC. Valid input range is between 0V to 1.8V. Analog inputs can be sampled as described in section Signal/Data Acquisition and Control.

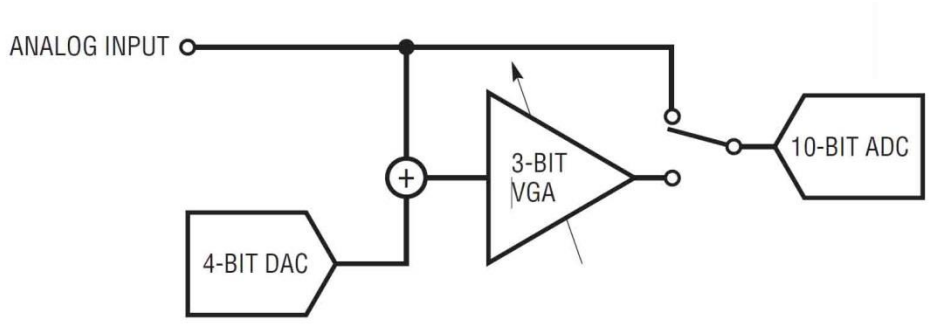

Figure 18. Analog input chain

RESETn: The asynchronous reset signal is internally pulled up. Resetting WSM2400 will result in the ARM Cortex M3 rebooting and loss of network connectivity. Use of this signal for resetting WSM2400 is not recommended, except during power-on and in-circuit programming.

RADIO_INHIBIT: RADIO_INHIBIT provides a mechanism for an external device to temporarily disable radio operation. Failure to observe the timing requirements defined in the RADIO_INHIBIT AC Characteristics section may result in unreliable network operation. In designs where the RADIO_INHIBIT function is not needed. The input must either be tied, pulled or actively driven low to avoid excess leakage.

TMS, TCK, TDI, TDO: JTAG Port Supporting Software Debug and Boundary Scan.

SLEEPn: The SLEEPn function is not currently supported in software. The SLEEPn input must either be tied, pulled or actively driven high to avoid excess leakage.

UART_RX, UART_RX_RTSn, UART_RX_CTSn, UART_TX, UART_TX_RTSn, UART_TX_CTSn: The API UART interface includes bidirectional wake up and flow control. Unused input signals must be driven or pulled to their inactive state.

TIMEn: Strobing the TIMEn input is the most accurate method to acquire the network time maintained by WSM2400. WSM2400 latches the network time stamp with sub-microsecond resolution on the rising edge of the TIMEn signal and produces a packet on the API serial port containing the timing information.

UARTC0_RX, UARTC0_TX: The CLI UART provides a mechanism for monitoring, configuration and control of WSM2400 during operation.

GPIO3, GPIO4, GPIO5, GPIO6, GPIO20, GPIO21, GPIO22, GPIO23, GPIO26: General purpose I/Os that can be sampled or driven as described in the Signal/Data Acquisition and Control section.

FLASH_P_ENn, IPCS_SSn, IPCS_SCK, IPCS_MISO, IPCS_SSn: The In-Circuit Programming Control System (IPCS) bus enables in-circuit programming of WSM2400's flash memory. IPCS_SCK is a clock and should be terminated appropriately for the driving source to prevent overshoot and ringing.

OPERATION

The 505-10368-00/505-10369-00 is the world's most energy efficient IEEE 802.15.4 compliant platform, enabling battery and energy harvested applications. With a powerful 32-bit ARM Cortex-M3, best-in-class radio, flash, RAM and purpose-built peripherals, WSM2400 provides a flexible, scalable and robust networking solution for applications demanding minimal energy consumption and data reliability in even the most challenging RF environments.

Shown in Figure 19, WSM2400 integrates purpose-built peripherals that excel in both low operating-energy consumption and the ability to rapidly and precisely cycle between operating and low-power states. Items in the gray shaded region labeled Analog Core correspond to the analog/RF components.

POWER SUPPLY

WSM2400 is powered from a single pin, VSUPPLY, which powers the I/O cells and is also used to generate internal supplies. WSM2400's two on-chip DC/DC converters minimize WSM2400's energy consumption while the device is awake. To conserve power the DC/DC converters are disabled when the device is in low power state. WSM2400's power supply conditioning architecture, including the two integrated DC/ DC converters and three integrated low dropout regulators, provides excellent rejection of supply noise. WSM2400's operating supply voltage range is high enough to support direct connection to lithium-thionyl chloride (Li-SOCl2) sources and wide enough to support battery operation over a broad temperature range.

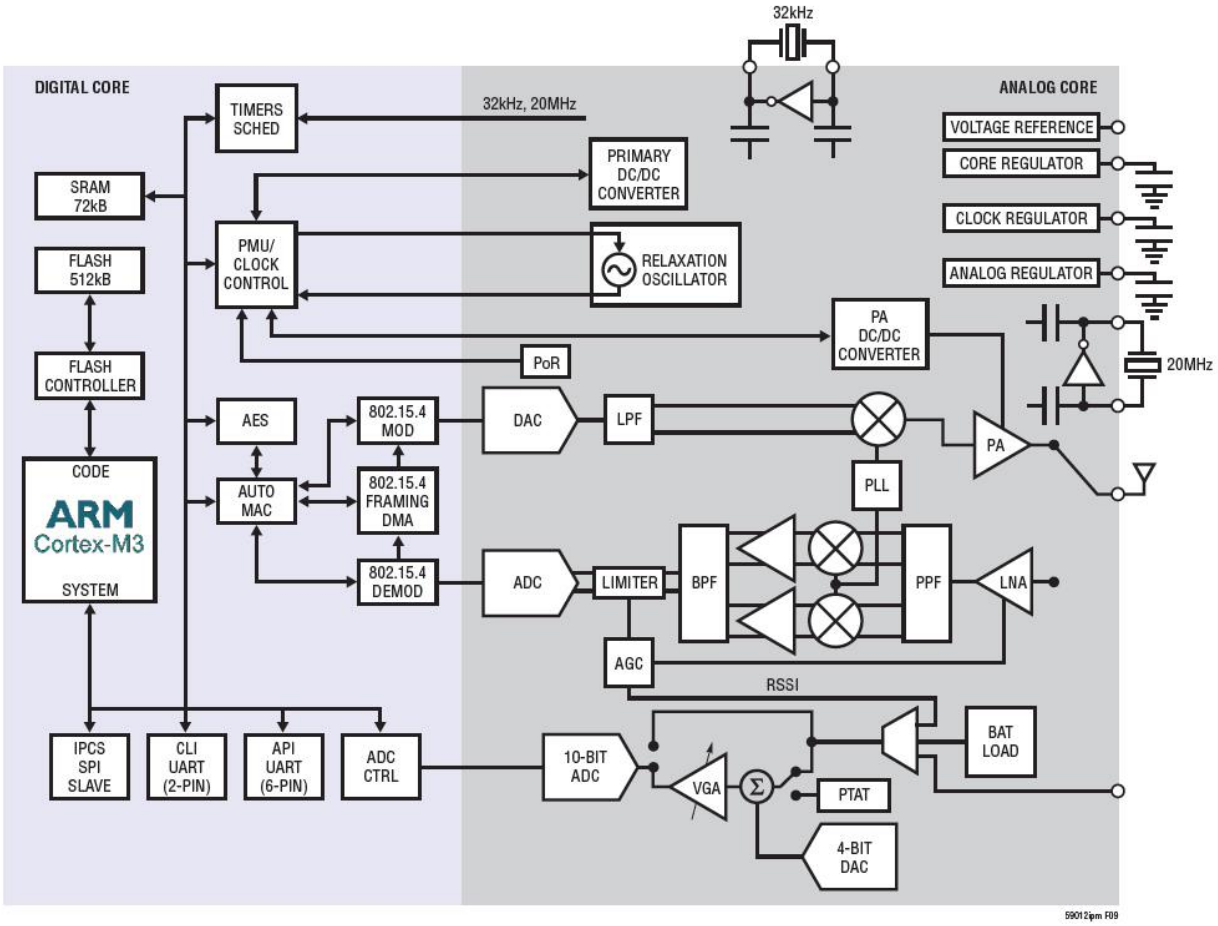

Figure 19. WSM2400 block diagram

SUPPLY MONITORING AND RESET

WSM2400 integrates a Power-on Reset (PoR) circuit. As the RESETn input pin is nominally configured with an internal pull-up resistor, no connection is required. For a graceful shutdown, the software and the networking layers should be cleanly halted via API commands prior to assertion of the RESETn pin.

WSM2400 includes a soft brown-out monitor that fully protects the flash from corruption in the event that power is removed while writing to flash. Integrated flash supervisory functionality, in conjunction with a fault tolerant file system, yields a robust non-volatile storage solution.

PRECISION TIMING

A major feature of WSM2400 over competing 802.15.4 product offerings is its low-power dedicated timing hardware and timing algorithms. This functionality provides timing precision two to three orders of magnitude better than any other low-power solution available at the time of publication. Improved timing accuracy allows motes to minimize the amount of radio listening time required to ensure packet reception thereby lowering even further the power consumed by SmartMesh networks. WSM2400's patented timing hardware and timing algorithms provide superior performance over rapid temperature changes, further differentiating WSM2400's reliability when compared with other wireless products. In addition, precise timing enables networks to reduce spectral dead time, increasing total network throughput.

APPLICATION TIME SYNCHRONIZATION

In addition to coordinating time slots across the network, which is transparent to the user, WSM2400's timing management is used to support two mechanisms to share network time. Having an accurate, shared, network-wide time base enables events to be accurately time stamped or tasks to be performed in a synchronized fashion across a network. WSM2400 will send a time packet through its serial interface when one of the following occurs:

- WSM2400 receives an API request to read time
- The TIMEn signal is asserted

The use of TIMEn has the advantage of being more accurate. The value of the timestamp is captured in hardware relative to the rising edge of TIMEn. If an API request is used, due to packet processing, the value of the timestamp may be captured several milliseconds after receipt of the packet due to packet processing. See the TIMEn AC Characteristics section for the time function's definition and specifications.

TIME REFERENCES

WSM2400 includes three clock sources: an internal relaxation oscillator, a low power oscillator designed for a 32.768kHz crystal, and the radio reference oscillator designed for a 20MHz crystal.

RELAXATION OSCILLATOR

The relaxation oscillator is the primary clock source for WSM2400, providing the clock for the CPU, memory subsystems, and all peripherals. The internal relaxation oscillator is dynamically calibrated to 7.3728 MHz. The internal relaxation oscillator typically starts up in a few µs, providing an expedient, low

energy method for duty cycling between active and low power states. Quick start-up from the doze state, defined in the State Diagram section, allows WSM2400 to wake up and receive data over the UART and SPI interfaces by simply detecting activity on the appropriate signals.

32.768kHz Crystal Once WSM2400 is powered up and the 32.768kHz crystal source has begun oscillating, the 32.768kHz crystal remains operational while in the active state, and is used as the timing basis when in doze state. See the State Diagram section for a description of WSM2400's operational states.

20MHZ CRYSTAL

The 20 MHz crystal source provides a frequency reference for the radio, and is automatically enabled and disabled by WSM2400 as needed.

RADIO

WSM2400 includes the lowest power commercially available 2.4GHz IEEE 802.15.4e radio by a substantial margin. (Please refer to the Radio Specifications section for power consumption numbers.). WSM2400's integrated power amplifier is calibrated and temperature compensated to consistently provide power at a limit suitable for worldwide radio certifications. Additionally, WSM2400 uniquely includes a hardware-based autonomous MAC that handles precise sequencing of peripherals, including the transmitter, the receiver, and Advanced Encryption Standard (AES) peripherals. The hardware-based autonomous Media Access Controller (MAC) minimizes CPU activity, thereby further decreasing power consumption.

UARTS

The principal network interface is through the application programming interface (API) UART. A Command-Line Interface (CLI) is also provided for support of test and debug functions. Both UARTs sense activity continuously, consuming virtually no power until data is transferred over the port and then automatically returning to their lowest power state after the conclusion of a transfer.

API UART PROTOCOL

The API UART protocol was created with the goal of supporting a wide range of companion Multipoint Control Units (MCUs) while reducing power consumption of the system. The receive half of the API UART protocol includes two additional signals in addition to UART_RX: UART_RX_ RTSn and UART_RX_CTSn. The transmit half of the API UART protocol includes two additional signals in addition to UART_TX: UART_TX_RTSn and UART_TX_CTSn. The API UART protocol is referred to as Mode 4. In the Figures accompanying the protocol descriptions, signals driven by the companion processor are drawn in black and signals driven by WSM2400 are drawn in blue.

UART MODE 4

UART Mode 4 incorporates level sensitive flow control on the TX channel and requires no flow control on the RX channel, supporting 115200 baud. The use of level sensitive flow control signals enables higher data rates with the option of using a reduced set of the flow control signals; however, with the companion processor must negate UART_TX_CTSn prior to the end of the packet and wait at least tRX_RTS to RX_CTS between sending packets. See the UART AC Characteristics section for complete timing specifications. Packets are HDLC encoded with one stop bit and no parity bit. The use of the RX flow control signals (UART_RX_RTSn and UART_RX_CTSn) for Mode 4 are optional. The flow control signals for the TX channel are shown in Figure 20. UART Mode 4 Transmit Flow Control. Transfers are initiated by WSM2400 asserting UART_TX_RTSn. The UART_TX_CTSn signal may be actively driven by the companion processor when ready to receive a packet or UART_TX_CTSn may be tied low if the companion processor is always ready to receive a packet. After detecting a logic '0' on UART_TX_CTSn WSM2400 sends the entire packet. Following the transmission of the final byte in the packet WSM2400 negates UART_TX_RTSn and waits for a minimum period defined in the UART AC Characteristics section before asserting UART_TX_RTSn again. For details on the timing of the UART protocol, see the UART AC Characteristics section.

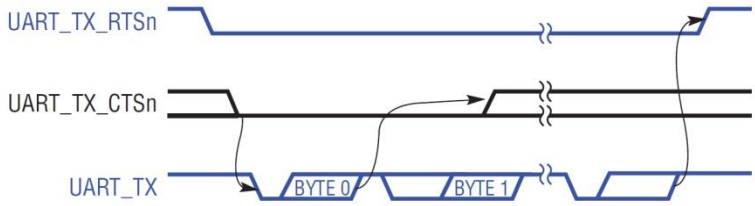

Figure 20. UART Mode 4 flow control

CLI UART

The Command Line Interface (CLI) UART port is a two wire protocol (TX and RX) that operates at a fixed 9600 baud rate with one stop bit and no parity. The CLI UART interface is intended to support command line instructions and response activity.

AUTONOMOUS MAC

WSM2400 was designed as a system solution to provide a reliable, ultralow power, and secure network. A reliable network capable of dynamically optimizing operation over changing environments requires solutions that are far too complex to completely support through hardware acceleration alone. As described in the Precision Timing section, proper time management is essential for optimizing a solution that is both low power and reliable. To address these requirements WSM2400 includes the autonomous MAC, which incorporates a coprocessor for controlling all of the time critical radio operations. The autonomous MAC provides two benefits: first, preventing variable software latency from affecting

network timing and second, greatly reducing system power consumption by allowing the CPU to remain inactive during the majority of the radio activity. The autonomous MAC, provides software independent timing control of the radio and radio related functions, resulting in superior reliability and exceptionally low power.

SECURITY

Network security is an often overlooked component of a complete network solution. Proper implementation of security protocols is significant in terms of both engineering effort and market value in an OEM product. WSM2400 system solutions provide a FIPS-197 validated encryption scheme that includes authentication and encryption at the MAC and network layers with separate keys for each mote. This not only yields end-to-end security, but if a mote is somehow compromised, communication from other motes is still secure. A mechanism for secure key exchange allows keys to be kept fresh. To prevent physical attacks, WSM2400 includes hardware support for electronically locking devices, thereby preventing access to WSM2400's flash and RAM memory and thus the keys and code stored therein.

TEMPERATURE SENSOR

WSM2400 includes a calibrated temperature sensor on chip. The temperature readings are available locally through WSM2400's serial API, in addition to being available via the network manager. The performance characteristics of the temperature sensor can be found in the Temperature Sensor Characteristics section.

RADIO INHIBIT

The RADIO_INHIBIT input enables an external controller to temporarily disable the radio software drivers (for example, to take a sensor reading that is susceptible to radio interference). When RADIO_INHIBIT is asserted the software radio drivers will disallow radio operations including clear channel assessment, packet transmits, or packet receipts. If the radio is active in the current timeslot when RADIO_INHIBIT is asserted the radio will be disabled after the present operation completes. For details on the timing associated with RADIO_INHIBIT, see the RADIO_INHIBIT AC Characteristics section.

FACTORY INSTALLED SOFTWARE

This product is provided with software programmed into the device. Devices can be configured via either the CLI or API ports.

FLASH DATA RETENTION

WSM2400 contains internal flash (non-volatile memory) to store calibration results, unique ID, configuration settings and software images. Flash retention over the operating temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections. Nondestructive storage above the operating temperature range of –40°C to 85°C is possible; although, this may result in a degradation of retention characteristics. The degradation in flash retention for temperatures >85°C can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

Where:

AF = acceleration factor

Ea = activation energy = 0.6eV

$k = 8.625 \bullet 10^{-5}$eV/°K

Figure 21. Equation

TUSE = is the specified temperature retention in °C
TSTRESS = actual storage temperature in °C

Example: Calculate the effect on retention when storing at a temperature of 105°C.
TSTRESS = 105°C
TUSE = 85°C

AF = 2.8

So the overall retention of the flash would be degraded by a factor of 2.8, reducing data retention from 20 years at 85°C to 7.1 years at 105°C.

State Diagram In order to provide capabilities and flexibility in addition to ultralow power, WSM2400 operates in various states, as shown in Figure 22. WSM2400 State Diagram and described in this section. State transitions shown in red are not recommended.

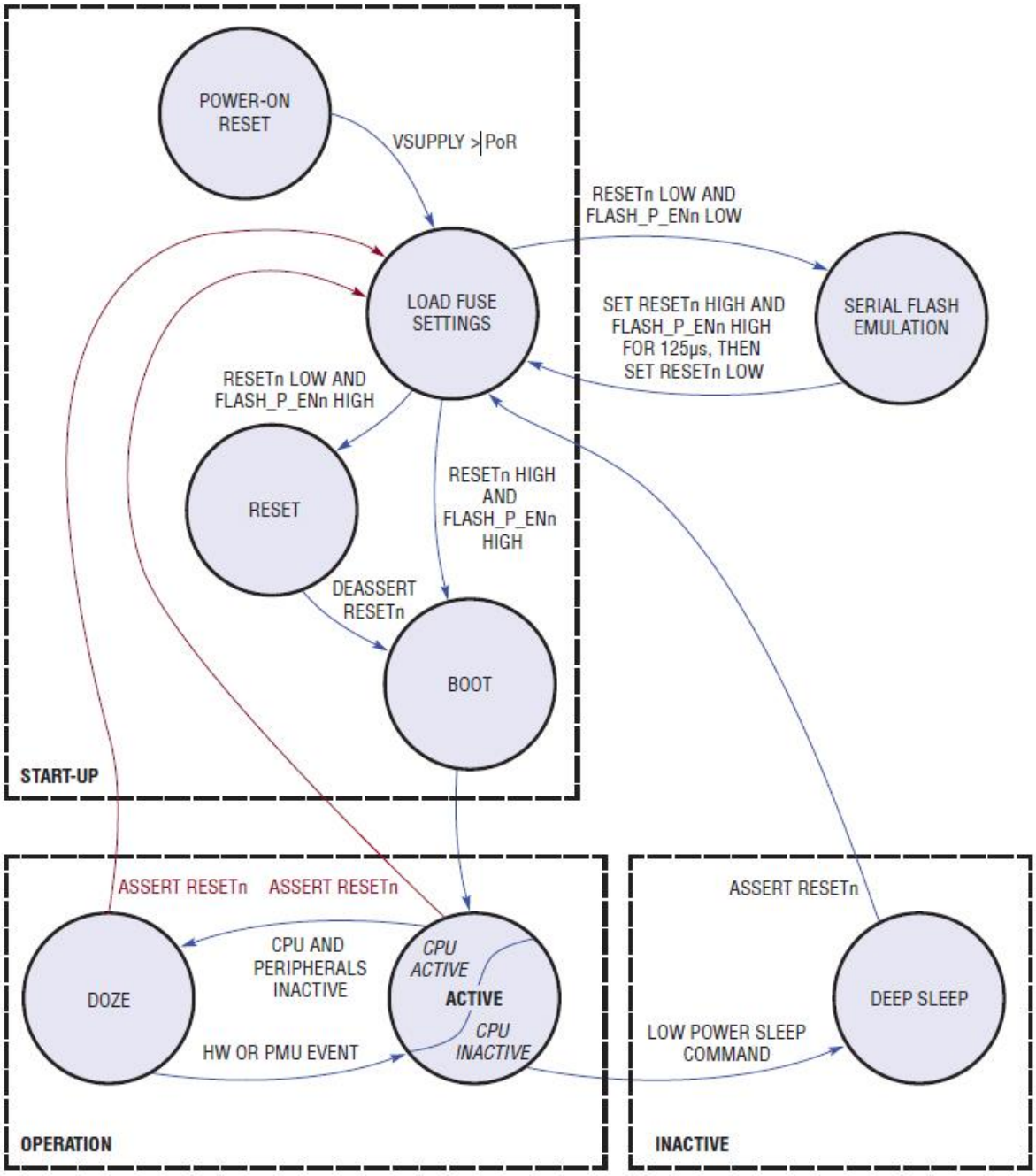

Figure 22. WSM2400 state diagram

START-UP

Start-up occurs as a result of either crossing the power-on reset threshold or asserting RESETn. After the completion of power-on reset or the falling edge of an internally synchronized RESETn, WSM2400 loads its fuse table which, as described in the previous section, includes setting I/O direction. In this state, WSM2400 checks the state of the FLASH_P_ENn and RESETn and enters the serial flash emulation mode if both signals are asserted. If the FLASH_P_ENn pin is not asserted but RESETn is asserted, WSM2400 automatically reduces its energy consumption to a minimum until RESETn is released. Once RESETn is de-asserted, WSM2400 goes through a boot sequence, and then enters the active state.

SERIAL FLASH EMULATION

When both RESETn and FLASH_P_ENn are asserted, WSM2400 disables normal operation and enters a mode to emulate the operation of a serial flash. In this mode, its flash can be programmed.

OPERATION

Once WSM2400 has completed start-up, WSM2400 transitions to the operational group of states (active/CPU active, active/ CPU inactive, and Doze). There, WSM2400 cycles between the various states, automatically selecting the lowest possible power state while fulfilling the demands of network operation.

ACTIVE STATE

In the active state, WSM2400's relaxation oscillator is running and peripherals are enabled as needed. The ARM Cortex-M3 cycles between CPU-active and CPU-inactive (referred to in the ARM Cortex-M3 literature as sleep now mode). WSM2400's extensive use of DMA and intelligent peripherals that independently move WSM2400 between active state and doze state minimizes the time the CPU is active, significantly reducing WSM2400's energy consumption.

DOZE STATE

The doze state consumes orders of magnitude less current than the active state and is entered when all of the peripherals and the CPU are inactive. In the doze state WSM2400's full state is retained, timing is maintained, and WSM2400 is configured to detect, wake, and rapidly respond to activity on I/Os (such as UART signals and the TIMEn pin). In the doze state the 32.768kHz oscillator and associated timers are active.

APPLICATIONS INFORMATION

SIGNAL/DATA ACQUISITION AND CONTROL

SmartMesh IP software includes embedded application support for sampling temperature, WSM2400's ADC and GPIO inputs, and support for actuating GPIO outputs. The Onchip Application Protocol (OAP) enables these functions via data packets sent through the network manager over the air, removing the need for a microprocessor connected to the mote or embedded software development on WSM2400.

SOLDERING INFORMATION

The 505-10368-00 and 505-10369-00 are suitable for both eutectic PbSn and RoHS-6 reflow. The maximum reflow soldering temperature is 260°C. A more detailed description of layout recommendations, assembly procedures and design considerations is included in the 505-10368-00 and 505-10369-00 Hardware Integration Guide.

FCC, INDUSTRY CANADA, SAFETY INFORMATION AND WARNINGS

FCC COMPLIANCE STATEMENT

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

INDUSTRY CANADA COMPLIANCE STATEMENT

This Class B digital apparatus complies with Canadian ICES-003. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil numérique de la classe B est conforme à la norme IECS -003 du Canada . Le fonctionnement est soumis aux deux conditions suivantes : (1) ce dispositif ne peut pas provoquer d'interférences et (2) cet appareil doit accepter toute interférence , y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.

FCC RF RADIATION EXPOSURE STATEMENT

WARNING: These B+B SmartWorx devices radiate radio frequency energy at a level below the United States FCC radio frequency exposure limits. Nevertheless, this device should be used in such a manner that the potential for human contact during normal operation is minimized.

MODIFICATION WARNING

US FCC Modification warning (FCC Part 15.21) Warning: changes or modifications to this equipment not expressly approved by B+B SmartWorx could void the user’s authority to operate the equipment. In addition, damage or performance problems resulting from modification may not be covered under warranty.

ADVANTECH B+B SMARTWORX TECHNICAL SUPPORT

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