OEM/Integrators Installation Manual

BCM-LA100-AS

Revision 0.1 DRAFT – 2019/03/18

CONFIDENTIAL INFORMATION

BnCOM Co.,Ltd.

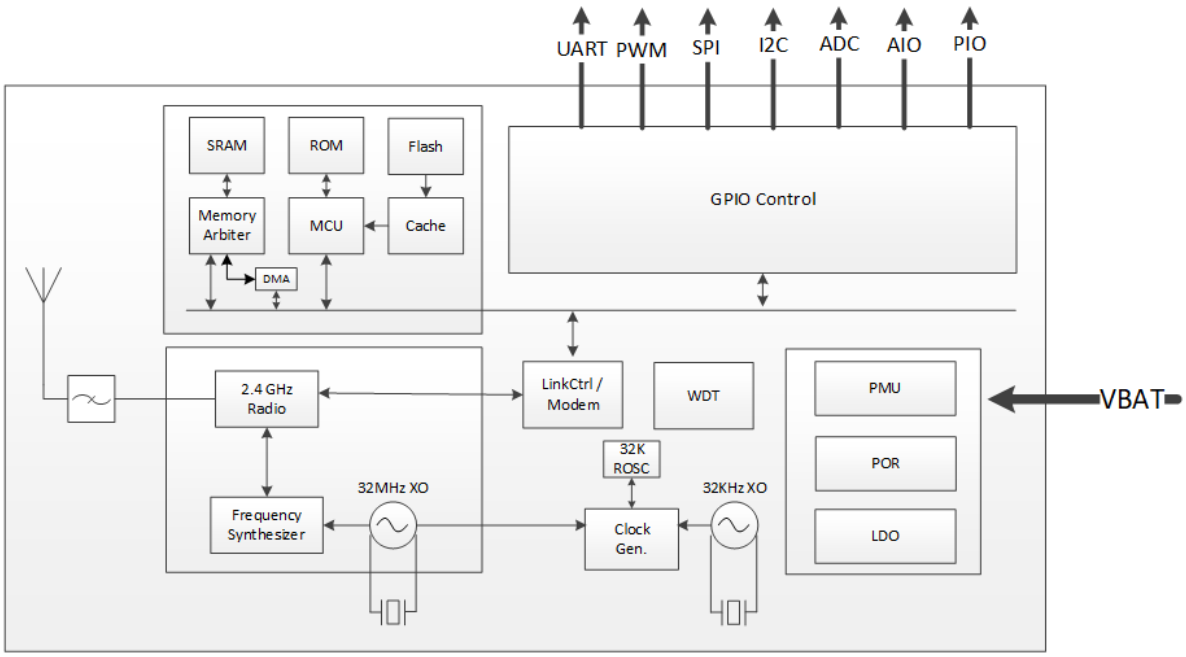
List of Contents

1. General

1.1 Overview

This specification covers Bluetooth module which complies with Bluetooth specification version 5.0 and integrates RF & Baseband controller in small package. This Module has deployed Airoha AB1611 chipset.

All detailed specification including pin outs and electrical specification may be changed without notice.



1.2 Features

■ Bluetooth® Ver5.0 specification compliant

■ 2Mbps, Long Range, ADV extention, SIG Mesh

■ Embedded 32-bit MCU with 16/72MHz clock rate

■ Embedded 4Mbit Flash

■ 64KB SRAM

■ 9 AIO support (12bit)

■ 21 GPIO support

■ Integrate 16-bits, 16KHz Mic ADC for voice search/input applications

■ Integrate 1.8V switching regulator and 1.8V LDO regulator

■ Ultar-low power consumption for battery enabled applications

■ Competitive Size: 11mm x 16mm x 2.5mm : 54Pin

■ Operating temperature range (MAX -30℃ ~ 85℃)

1.3 Application

■ 2.4GHz Bluetooth Low Energy Systems

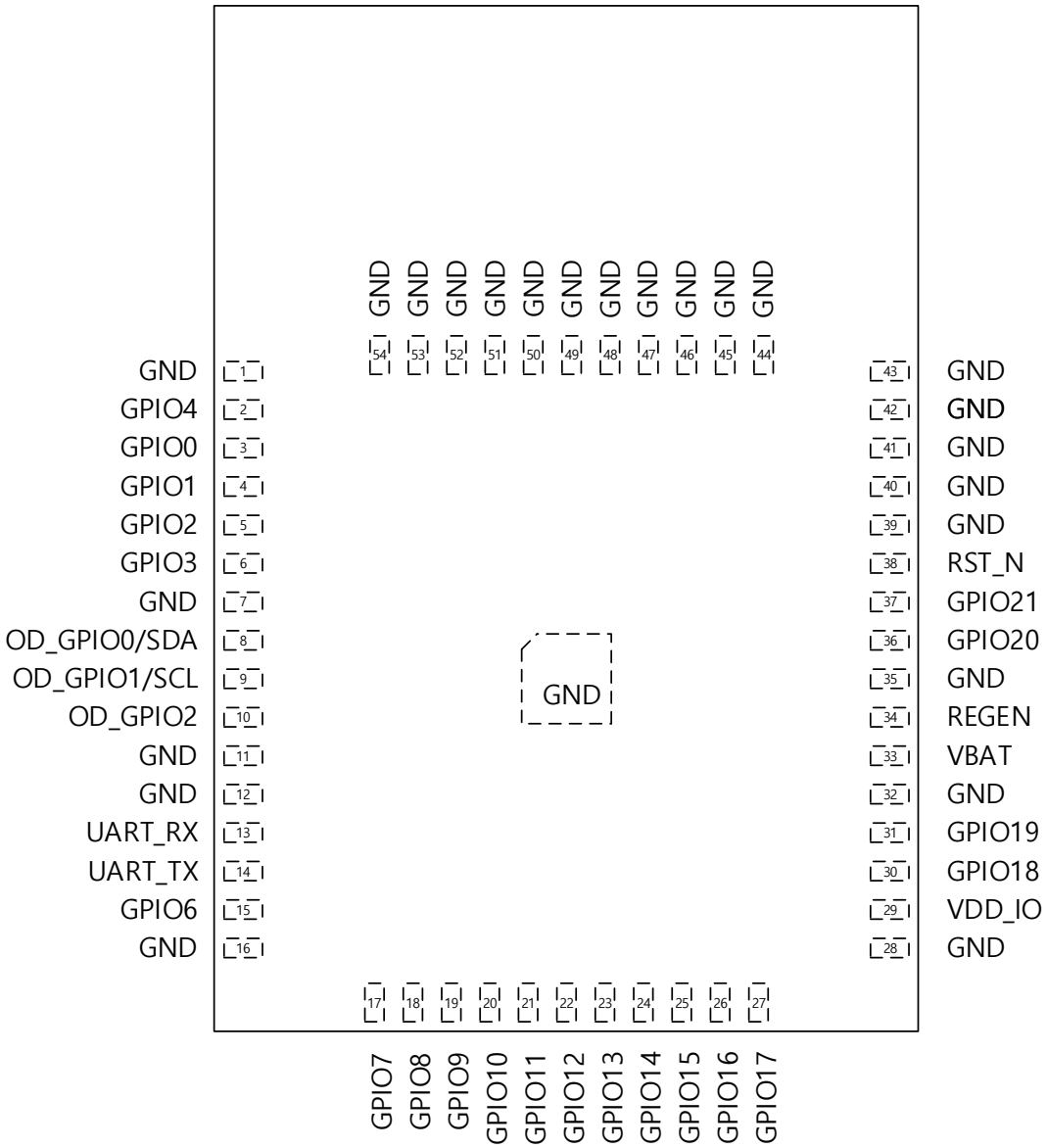
■ SIG Mesh

■ Beacon

■ Smart Home

■ Mobile Phone Accessories

1.3 Pin Configuration



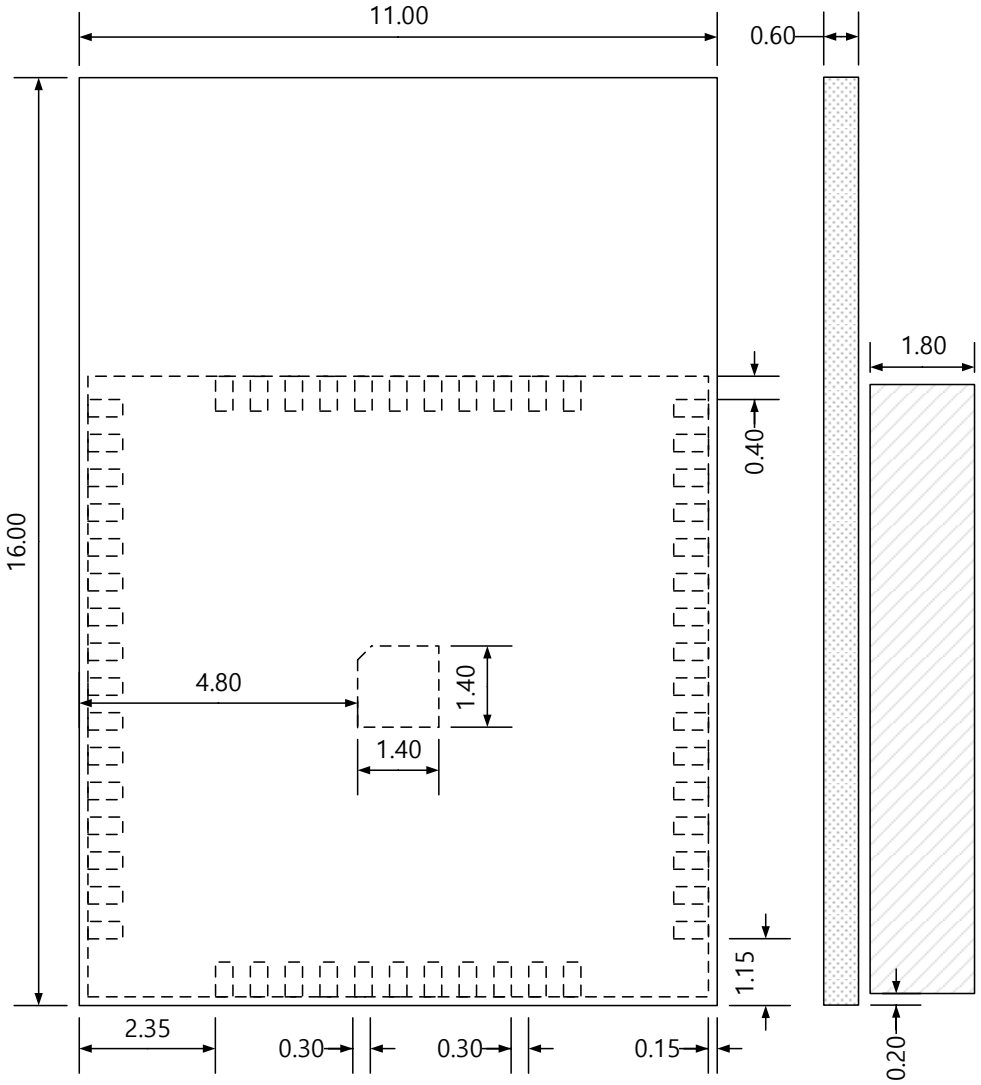
Pin Configuration (TOP VIEW)

1.4 Device Terminal Functions

Function				Pin Name	Pin No.	Pin type	Description
Power management unit	REGEN			REGEN	34	input	Chip enable
	VBAT			VBAT	33	Supply 1.9V ~ 3.6V	VCC for LDO and Buck
	VDD_IO			VDD_IO	29	Supply 1.7V ~ 3.6V	VCC for IO
	RST_N			RST_N	38	input, Digital	Global reset, active low (Pull high resistor: 137Kohm)
	Ground			GND	1, 7,11,12,16, 28,32,35,39,40, 41,42,43,44,45, 46,47,48,49,50, 51,52,53,54,55	Ground	
GPIO0	GPIO0			GPIO0	3	input/output	Programmable input/output line
GPIO1	GPIO1			GPIO1	4	input/output	Programmable input/output line
GPIO2	GPIO2			GPIO2	5	input/output	Programmable input/output line
GPIO3	GPIO3			GPIO3	6	input/output	Programmable input/output line
GPIO4	GPIO4			GPIO4	2	input/output	Programmable input/output line
GPIO6	GPIO6			GPIO6	15	input/output	Programmable input/output line
GPIO7	GPIO7			GPIO7	17	input/output	Programmable input/output line
GPIO8	GPIO8			GPIO8	18	input/output	Programmable input/output line
GPIO9	GPIO9			GPIO9	19	input/output	Programmable input/output line
GPIO10	GPIO10			GPIO10	20	input/output	Programmable input/output line
GPIO11	GPIO11			GPIO11	21	input/output	Programmable input/output line
GPIO12	GPIO12			GPIO12	22	input/output	Programmable input/output line
GPIO13	GPIO13	AIO		GPIO13	23	input/output	Programmable input/output line
GPIO14	GPIO14	AIO		GPIO14	24	input/output	Programmable input/output line
GPIO15	GPIO15	AIO		GPIO15	25	input/output	Programmable input/output line
GPIO16	GPIO16	AIO		GPIO16	26	input/output	Programmable input/output line
GPIO17	GPIO17	AIO		GPIO17	27	input/output	Programmable input/output line
GPIO18	GPIO18	AIO	XO32K	GPIO18	30	input/output	Programmable input/output line
GPIO19	GPIO19	AIO	XO32K	GPIO19	31	input/output	Programmable input/output line
GPIO20	GPIO20	AIO		GPIO20	36	input/output	Programmable input/output line
GPIO21	GPIO21	AIO		GPIO21	37	input/output	Programmable input/output line
OD_GPIO0	OD_GPIO0	I2C_SDA		OD_GPIO0/SDA	8	input/output Open Drain	Programmable input/output line
OD_GPIO1	OD_GPIO1	I2C_SCK		OD_GPIO1/SCL	9	input/output Open Drain	Programmable input/output line
OD_GPIO2	OD_GPIO2			OD_GPIO2	10	input/output Open Drain	Programmable input/output line
UART_RX		UART_RX		UART_RX	13	input, Digital	UART RX
UART_TX		UART_TX		UART_TX	14	Output, Digital	UART TX

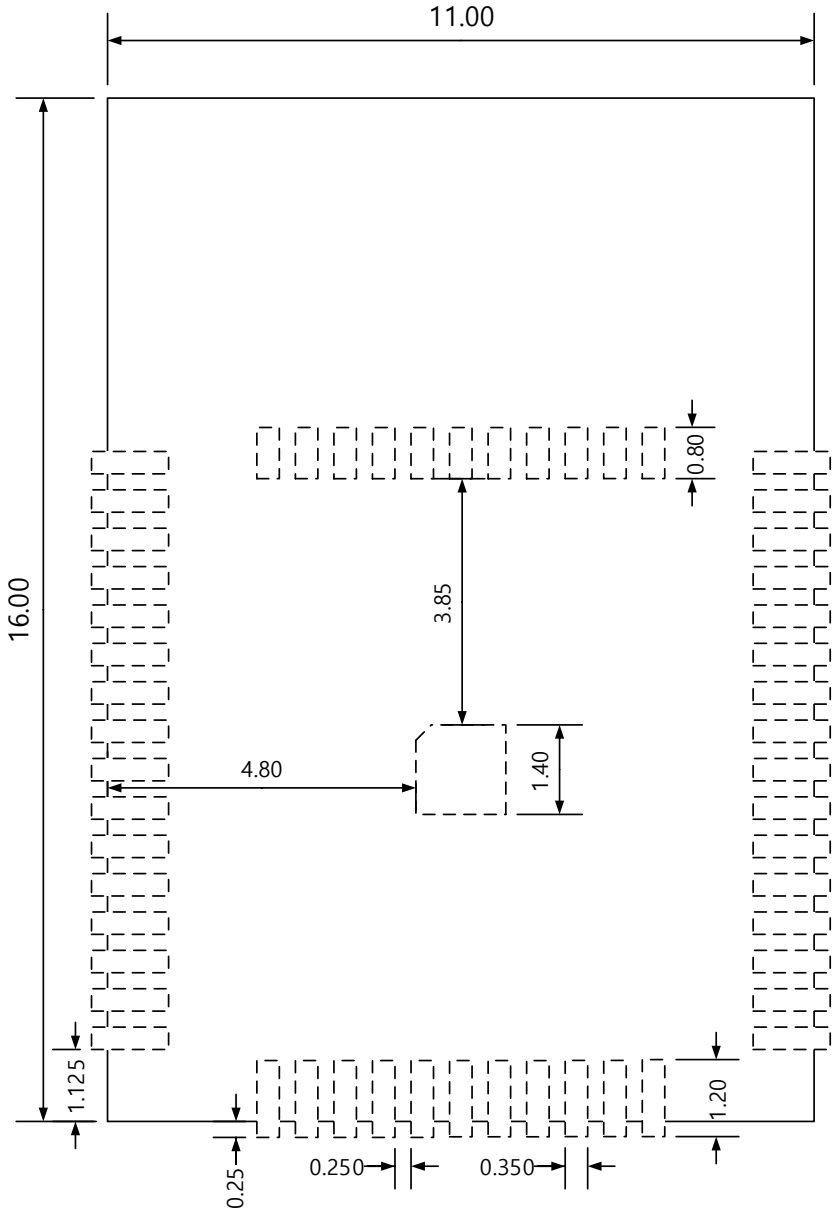
1.5 Package Dimensions & Land Pattern

- **unit = mm**
- **General Tolerances = ±0.2mm**



BCM-DA100-AS Package Dimensions

● **unit = mm**



< Land Pattern >

2. Characteristics

2.1 Electrical Characteristics

■ Absolute Maximum Ratings

ITEM		Min	Max	Unit
Storage Temperature range		-40	85	℃
Battery	VBAT	-0.3	3.6	V
VDD_IO		-0.3	3.6	V

■ Recommended Operating Conditions

ITEM		Min	TYP	Max	Unit
Operating Temperature range		-30	20	85	℃
Battery	VBAT	1.9		3.6	V
VDD_IO		1.7		3.6	V

■ Digital Terminals

ITEM	Min	TYP	Max	Unit
Input Voltage Levels				
Input logic level low (V_{IL})	0	-	0.3*VDDIO	V
Input logic level high (V_{IH})	0.7*VDDIO	-	VDDIO+0.4	V
Output Voltage Levels (1.7V≦VDDIO≦3.6V)	**Min**	**TYP**	**Max**	**Unit**
output logic level low (V_{OL}) , I_O = 4.0mA	-	-	0.2	V
output logic level high (V_{OH}), I_O = -4.0mA	VDDIO-0.2	-	-	V

2.2 RF Characteristics

■ Transmitter

Specification	Condition	Min	Typ	Max	Unit
Output transmit power	CH0	-	9.5	-	dBm
	CH39	-	9.5	-	dBm
	CH78	-	9.5	-	dBm
In-band emissions	≥ ±3MHz	-	-30	-	dBm
	+2MHz	-	-20	-	dBm
	-2MHz	-	-20	-	dBm
	≤ -3MHz	-	-30	-	dBm
Modulation characteristics	Δf1avg	225		275	KHz
	Percent of Δf2max > 185KHz	99.9		100	%
	Δf2avg/Δf1avg	-	1	-	
Center freq. deviation, Fn (n=0,1,2,.....k)		-150	-	+150	KHz
Freq. drift, |F0-Fn| (n=2,3,4,.....k)		-50	-	+50	KHz
Initial freq. drift, |F1-F0|		-20	-	+20	KHz
Max. freq. dirft rate, |Fn-Fn-5| (n=6,7,8,....k)		-20	-	+20	KHz/50us
Harmonics (cable mode)		-	-45	-	dBm

■ Receiver

Specification	Condition	Min	Typ	Max	Unit
Sensitivity	CH0	-	-92/-94	-	dBm
	CH39	-	-92/-94	-	dBm
	CH78	-	-92/-94	-	dBm
Maximum input level		-10	-	-	dBm
Co-Channel interference, C/I		-	-	21	dB
Adjacent channel interference, C/I	F=F0+1MHz	-	-	15	dB
	F=F0-1MHz	-	-	15	dB
	F=F0+2MHz	-	-	-17	dB
	F=F0-2MHz (image+1)	-	-	-15	dB
	F=F0+3MHz	-	-	-27	dB
	F=F0-3MHz (image+1)	-	-	-9	dB
Inermodulation		-50	-	-	dBm
Blocking	20-2000MHz	-30	-	-	dBm
	2003-2399MHz	-35	-	-	dBm
	2484-2997MHz	-35	-	-	dBm
	3000-12750MHz	-30	-	-	dBm
PER report integrity		-	50	-	%

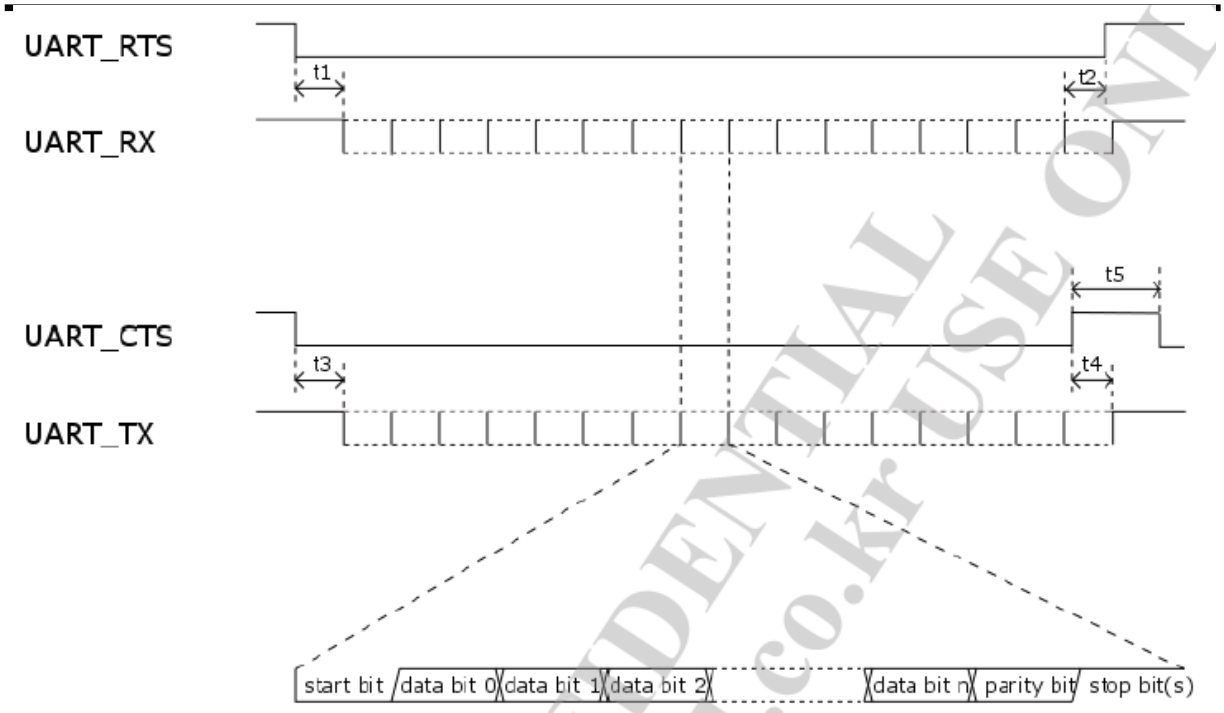
3. Terminal Description

3.1 UART Interface

BCM-LA100-AS supports two UARTs. One is dedicated pin and the other can be configured via GPIOs. The UART interface supports flexible configurations as shown below. There are local FIFOs and DMA Which provide high throughput serial communication. The UART also supports the hardware flow control. When it is enabled, two additional signal, UART_RTS and UART_CTS, are required. To provide the maximum flexibility, both UART_RTS and UART_CTS can be configured via any available GPIOs.

Configuration Parameters	Supported Values
Data Length	8bit
Flow Control	Hardware RTS/CTS None
Parity	Even Odd None
Number of stop bits	1 or 2
Baud rate	1200 2400 4800 9600 19200 38400 57600 76800 115200 230400 460800 921600 1228800 2000000

[UART configuration parameters]



[UART timing diagram]

Symbol	Description	Min	Max	Unit
t1	RTS low to start receiving	0	-	us
t2	Last 2 byte received to RTS high	-	1	byte
t3	CTS low to start transmitting	0.5	1.5	bit
t4	CTS high to stop transmitting	-	1	byte
t5	CTS-high pulse width	1	-	bit

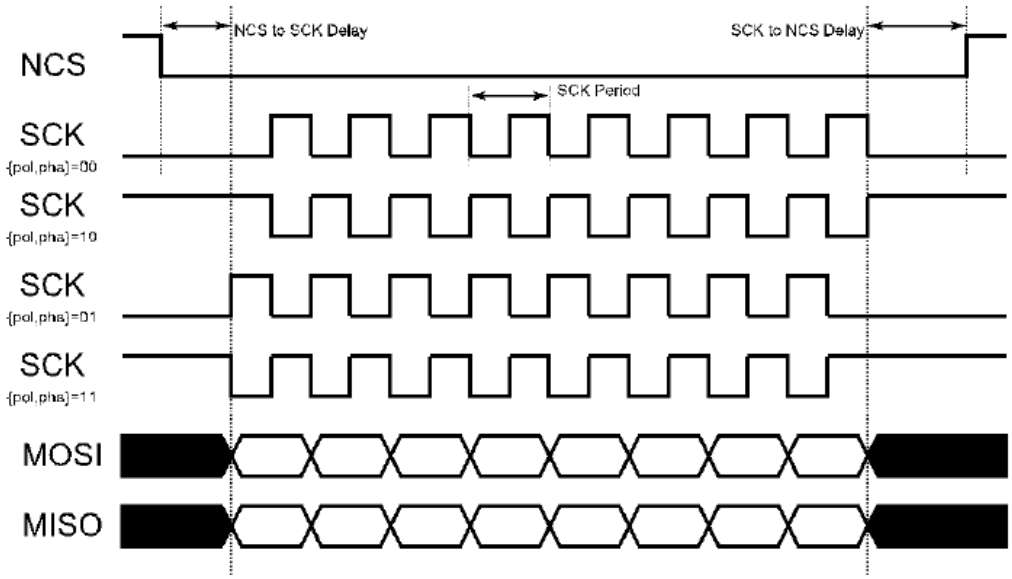
3.2 SPI Interface

The SPI communicates with external devices.
The 3-wire and 4-wire mode SPI interface are supported.
SPI_MOSI is the data I/O pin of the SPI interface when the 3-wire mode is selected.
The SPI interface is shared with GPIOs and the mapping tables are listed below.

GPIO pin	SPI Master mode 0	SPI Master mode 1
GPIO6	SPI_CSN	
GPIO7	SPIO_MOSI	
GPIO8	SPI_MISO	
GPIO9	SPI_SCK	
GPIO12		SPI_CSN
GPIO13		SPI_MOSI
GPIO14		SPI_MISO
GPIO15		SPI_SCK

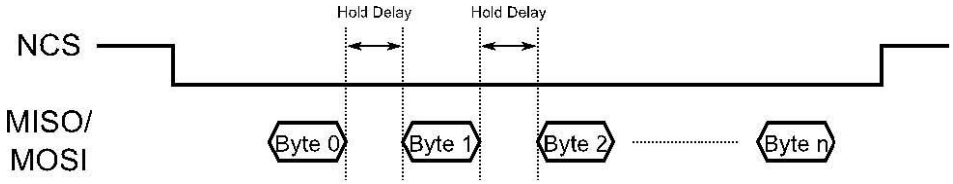
[SPI GPIO mapping table]

The SPI interface provides much flexibility that can fit most SPI slave devices.
The polarity and phase of SCK can be both programmed and results in four combinations.
The NCS to SCK delay, the SCK to NCS delay and SCK period are also programmed.
The timing relationships of SPI interface are illustrated below.



[SPI interface Timing Diagram]

The SPI interface also supports multiple bytes in single transfer. A Hold Delay can be set between each byte, as shown in the following figure.

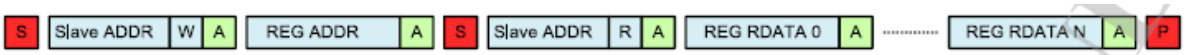


[SPI interface Multiple Bytes Transfer]

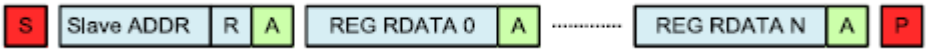
3.3 I2C Interface

The I2C is master interface. It supports 100, 400 and 800Khz clock rates. For controlling EEPROM, A write protect (WP) signal is also supported through GPIO. The I2C interface provides several data formats and can fit various I2C peripherals. Sequential read and write are supported to improve throughputs.

[I2C write transfer for 8-bit register addressing mode]



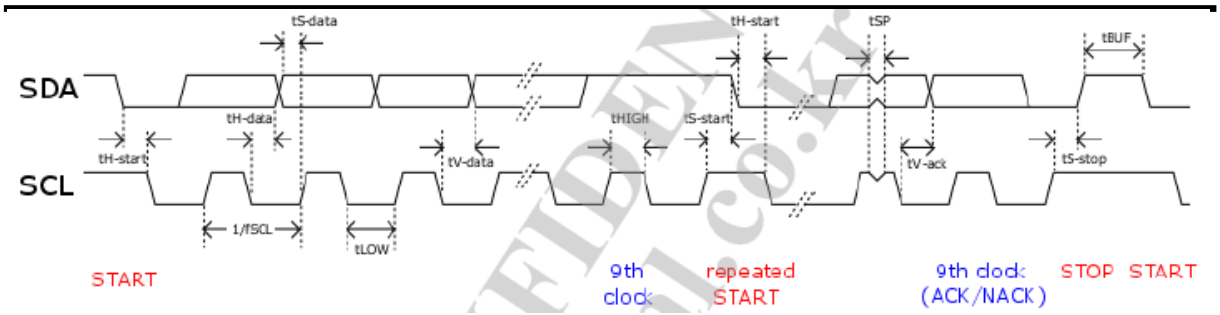
[I2C read transfer for 8-bit register addressing mode]



[I2C reads transfer with current address for 8-bit register addressing mode]

[I2C write transfer for 16-bit register addressing mode]

[I2C read transfer for 16-bit register addressing mode]



[Definition of timing on the I2C bus]

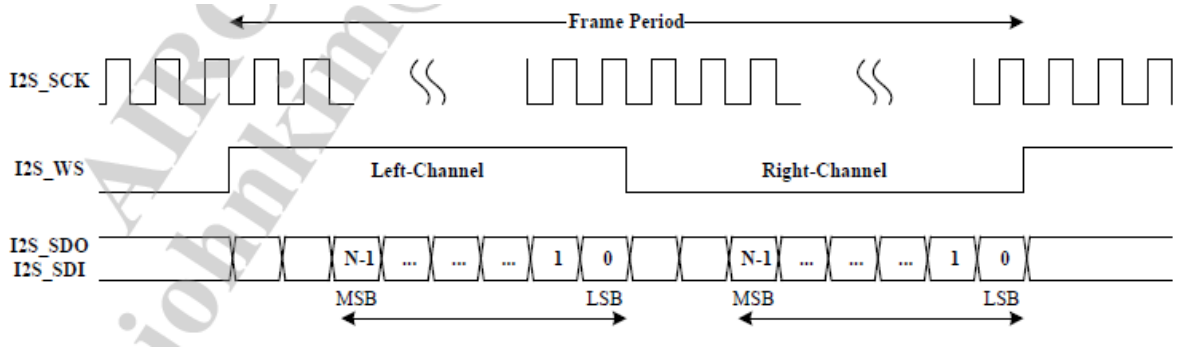
Symbol	Description	Standard-mode		Fast-mode		Fast-mode Plus		unit
		min	max	min	max	min	max	
fSCL	SCL clock frequency	0	100	0	400	0	800	KHz
tLOW	LOW period of the SCL clock	5.00	-	1.58	-	0.67	-	us
tHIGH	HIGH period of the SCL clock	5.00	-	0.92	-	0.58	-	us
tS-start	Set-up time for a repeated START condition	6.33	-	1.33	-	0.67	-	us
tH-start	Hold time for a START or repeated START condition	1.33	-	0.50	-	0.25	-	us
tH-data	Hold time for data	0	-	0	-	0	-	us
tS-data	Set-up time for data	250	-	100	-	50	-	us
tV-data	Data valid time	1.00	1.00	0.58	0.58	0.17	0.17	us
tV-ack	Data valid acknowledge time	1.00	1.00	0.58	0.58	0.17	0.17	us
tS-stop	Set-up time for STOP condition	1.00	8.00	0.50	2.00	0.25	1.00	us
tBUF	Bus free time between a START & STOP condition	3.33	-	0.83	-	0.42	-	us
tSP	Pulse width spikes must be suppressed by the input filter	0	83.3	0	83.3	0	83.3	ns

[Description of the symbols]

3.4 I2S Interface

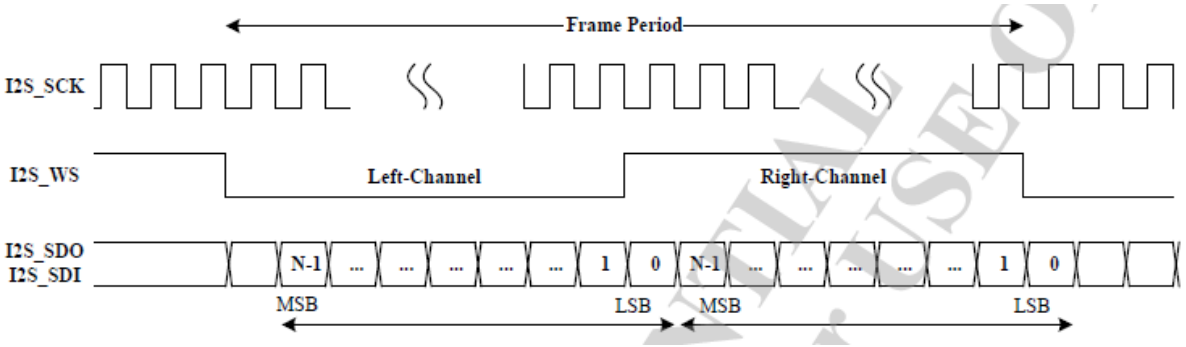
The I2S is a simple serial interface for sending stero audio bit streams. BCM-LA100-AS supports three I2S modes. The timing diagrams for the three modes are shown in the following diagram.

Right Justified Mode (Supports N=32/24/16-Bit)



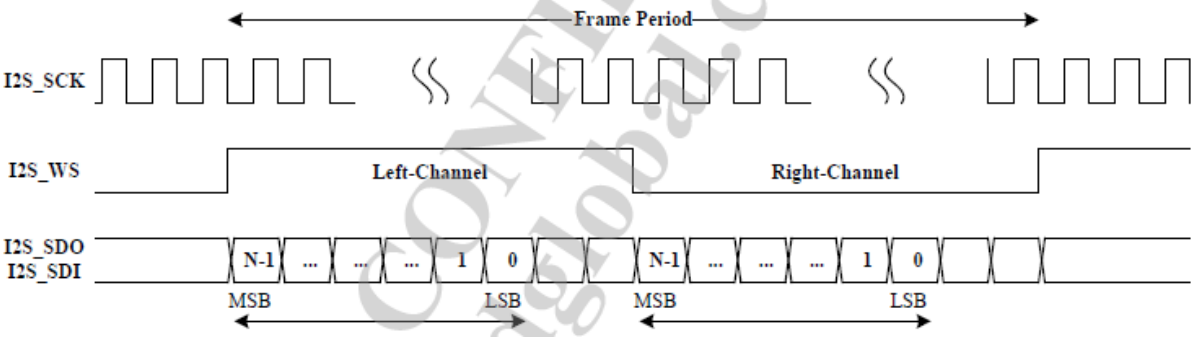
[Right justified mode]

I2S Justified Mode (Supports N=32/24/16-Bit)

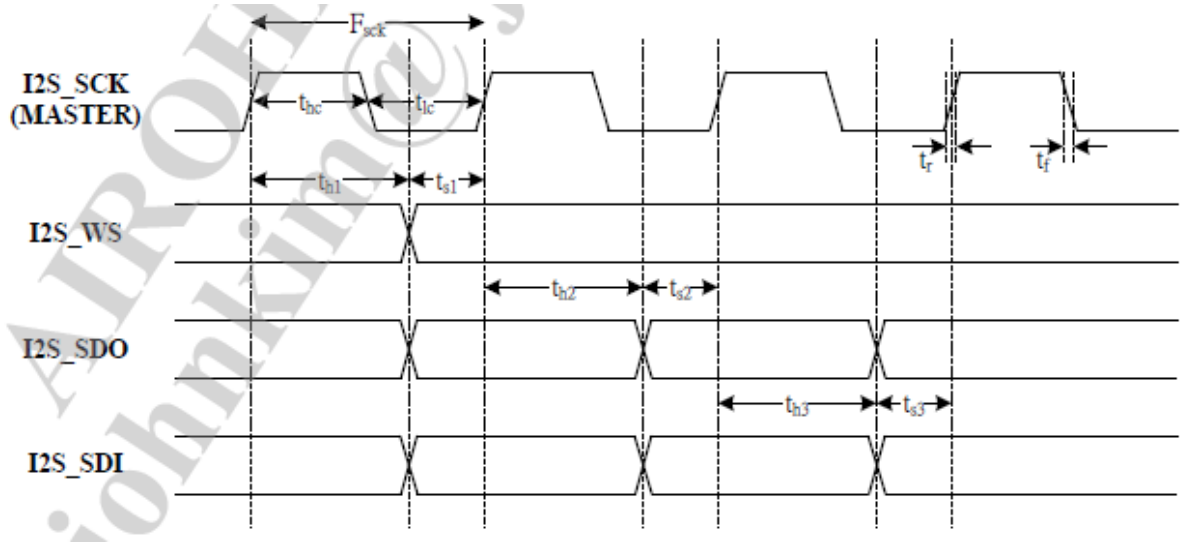


[I2S justified mode]

Left Justified Mode (Supports N=32/24/16-Bit)



[Left justified mode]

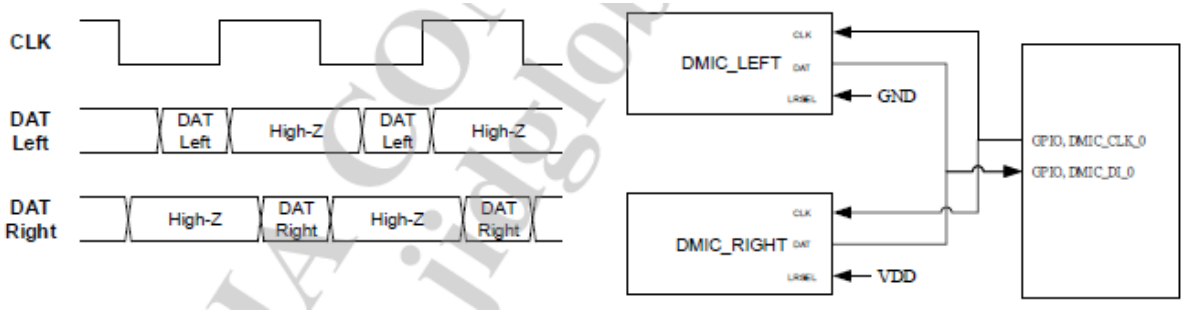


[Timing for I2S master mode]

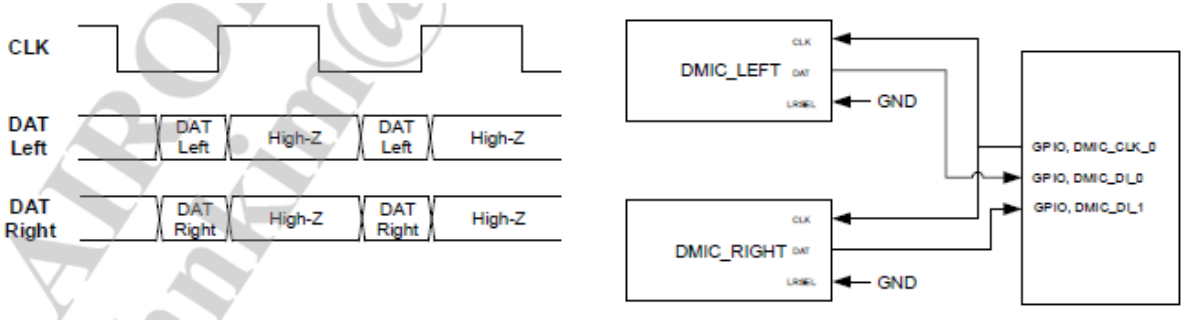
Symbol	Description	min
Fsck	Clock-Frequency	16K
thc	Clock high	240ns
tic	Clock low	240ns
ts1	Set-up time	20ns
th1	Hold time	20ns
ts2	Set-up time	20ns
th2	Hold time	20ns
ts3	Set-up time	20ns
th3	Hold time	20ns
tr	Rise time (10% - 90%, 30pF)	8ns
tf	Fall time (90% - 10%, 30pF)	8ns

3.5 DMIC

BCM-LA100-AS supports two DMIC and two wire mode. One is one-wire mode that left and right channel use one share data pin. Another two-wire mode that left and right channel use different data pin. Timing diagrams and interface connection are drawn below. The sample phase for each wire mode is also programmable.



[DMIC timing diagram and one-wire mode connection]



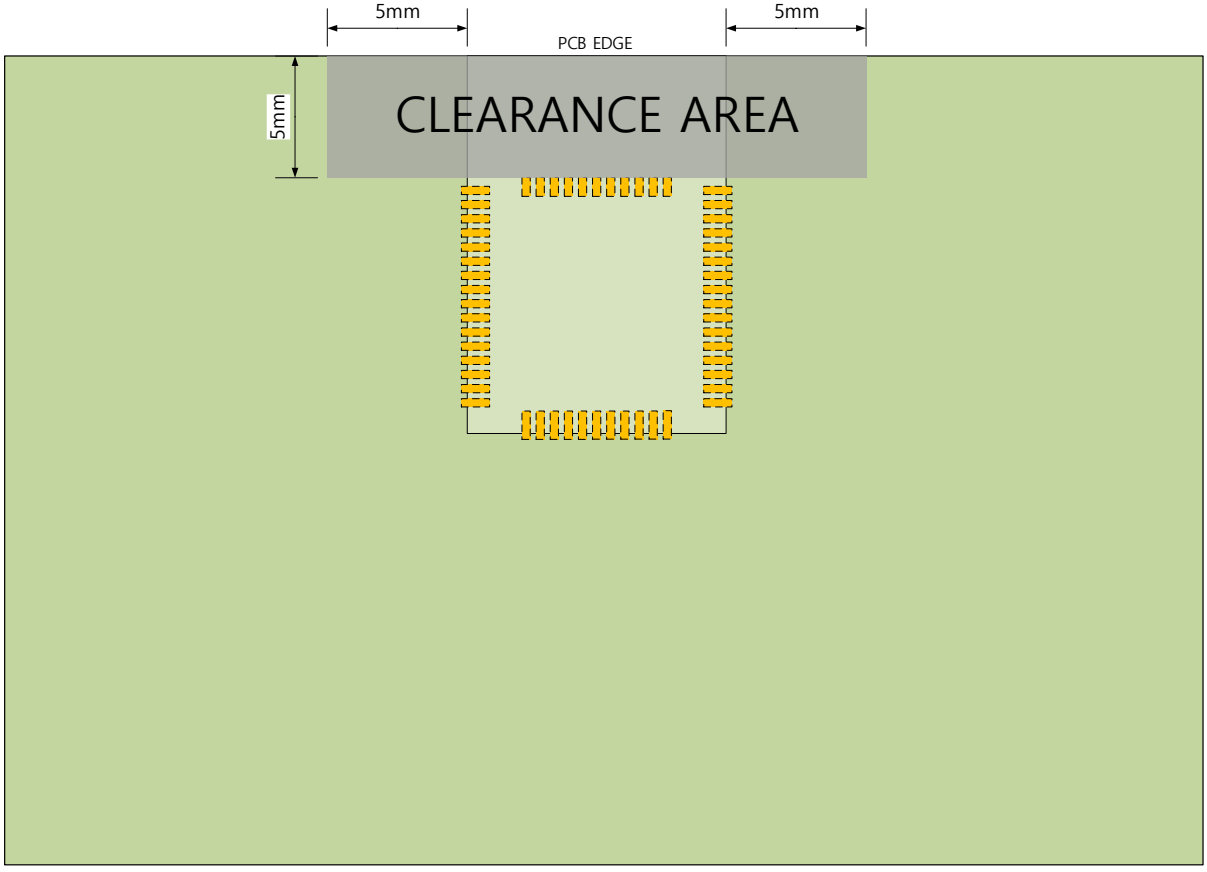
[DMIC timing diagram and two-wire mode connection]

Wire Mode	Channel	Valid	Sample Phase	LRSEL
One-Wire	DMIC_L	Falling CLK	Rising CLK	GND
	DMIC_R	Rising CLK	Falling CLK	VDD
Two-Wire	DMIC_L	Falling CLK	Rising CLK	GND
	DMIC_R	Falling CLK	Rising CLK	GND

4. Layout Guide

4.1 Layout Guide

For optimal performance of the antenna place the module at the outside of the PCB
Do not place any metal (traces, components, battery etc.) within the clearance area of the antenna. Connect all the GND pins directly to a solid GND plane. Place the GND vias as close to the GND pins as possible. Use good layout practices to avoid any excessive noise coupling to signal lines or supply voltage lines. Avoid placing plastic or any other dielectric material closer than 5 mm from the antenna. Any dielectric closer than 5 mm from the antenna will detune the antenna to lower frequencies.



5. Reflow Temperature Profile

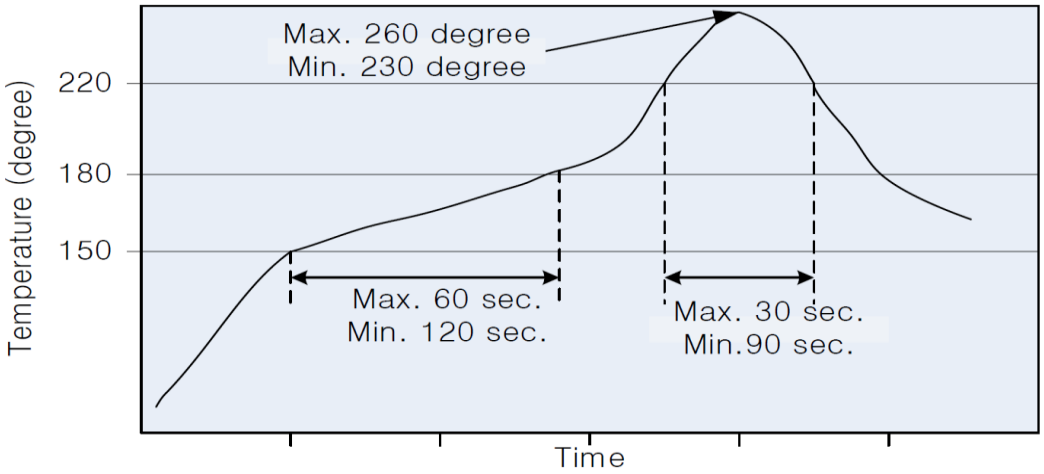
Recommended solder reflow profile are shown in below and follow the lead-free profile I accordance with JEDEC Std 20C.

Table lists the critical reflow temperatures.

Flux residue remaining from board assembly can contribute to electrochemical migration over time.

This depends on number of factors, including flux type, amount of flux residue remaining after reflow, and stress conditions during product use, such as temperature, humidity, and potential difference between pins.

Care should be taken in selecting production board/module assembly processes and materials, taking into account these factors.

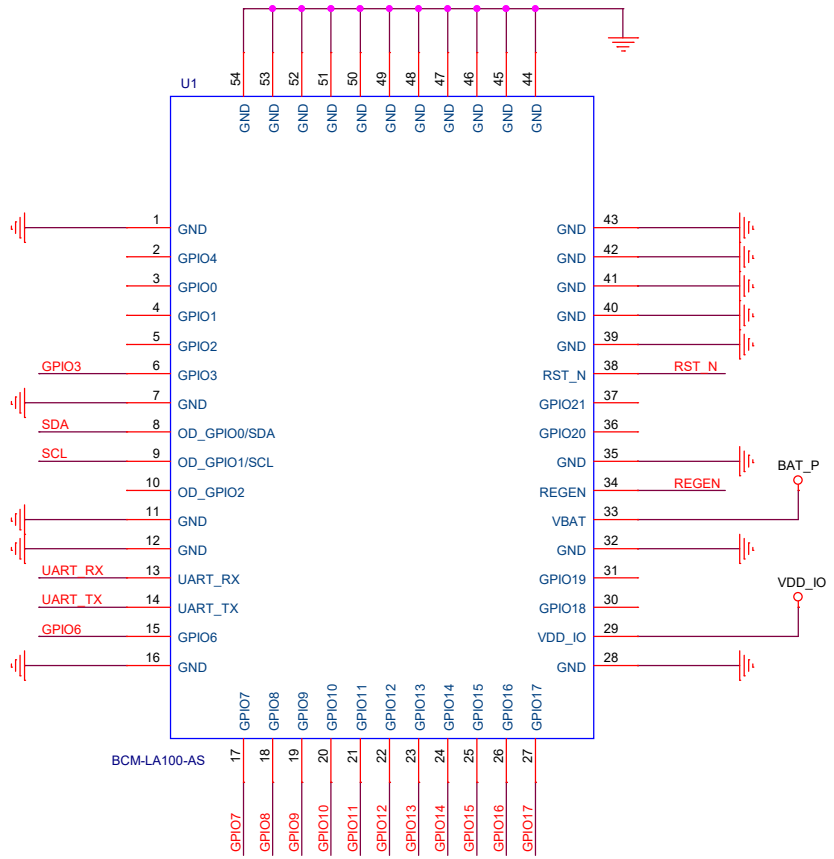


Process Step	Lead-Free Solder
Ramp rate	3°C/sec
Preheat	Max. 150°C to 180°C, 60 to 180 sec
Time above liquidus	+220°C 30 to 90 sec
Peak temperature	+255°C ±5°C
Time within 5°C of peak temperature	10 to 20 sec
Ramp-down rate	6°C/sec max

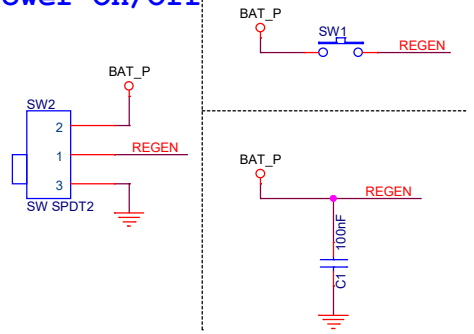
WARNING : For BCM-LA100-AS.

If you have reflow process multiple times in your product, you must be proceed this module in the final reflow process. If not the Shield can will drop out.

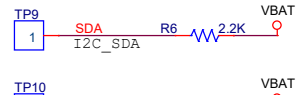
6. Example – Application Schematic



Power On/Off

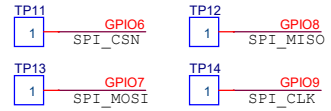


I2C Interface

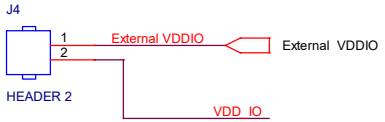


OD_GPIO1:
Pull up resistor (2.2K)
to VBAT if unused.

SPI Interface

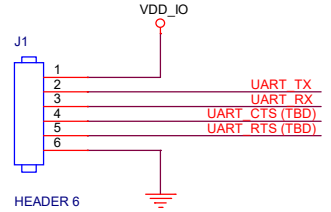


VDDIO SOURCE

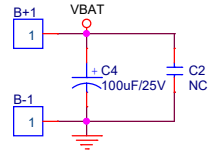


For GPIO Source Voltage
Input Range : 1.7V - 3.6V

UART



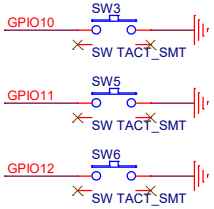
Dry Battery



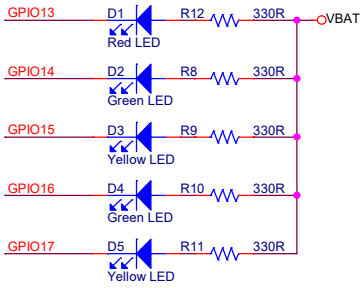
Test Points

enter RF test mode
short to GND before power on

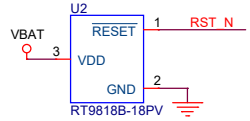
Key

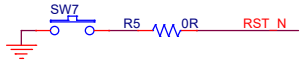


LED

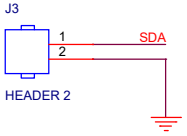


Reset





Engineer Mode



Enter Engineer Mode : Short SDA & GND

Support Funtion
- Firmware downlaod

Title	BCM-LA100-AS	
Size B	Document Number	Rev 0.1
Date: Sunday, March 17, 2019	Sheet 1 of 1	

FCC MODULAR APPROVAL INFORMATION EXAMPLES for Manual

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference.

(2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

OEM INTEGRATION INSTRUCTIONS:

This device is intended only for OEM integrators under the following conditions:

The module must be installed in the host equipment such that 20 cm is maintained between the antenna and users, and the transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the internal on-board antenna that has been originally tested and certified with this module. External antennas are not supported. As long as these 3 conditions above are met, further transmitter test will not be required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). The end-product may need Verification testing, Declaration of Conformity testing, a Permissive Class II Change or new Certification. Please involve a FCC certification specialist in order to determine what will be exactly applicable for the end-product.

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. In such cases, please involve a FCC certification specialist in order to determine if a Permissive Class II Change or new Certification is required.

Upgrade Firmware:

The software provided for firmware upgrade will not be capable to affect any RF parameters as certified for the FCC for this module, in order to prevent compliance issues.

End product labeling:

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains FCC ID: 2APDI-BCM-LA100-AS".

Information that must be placed in the end user manual:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.