REV	Description	DATE	BY
C	1. Improved layout for the USB PHY. 2. Removed unused parts from the design. 3. Added current measurement function to the TWL4030. 4. Added filter caps to the VBUS rail input and output. 5.Changed U9 & U11 package to the QFN..	8/14/08	GC
C1	1. Added J12 and J13 to provide access to the RGB TTL signals on the LCD. 2. Added 5 filter caps. 3. Moved the USB Host port from Port1 to Port2. 4. Deleted R1. 5. Added 10K pulldown to USB reset signal. 6. Added 10K pulldown resistors as ID function to determine board type by reading these pins. 7. Added series resistor, R53, in the CLK line of the HSUSB clock line. May be removed after testing.	10/1/08	GC
C2	1. Moved the McBSP3_DX signal to pin AB26. 2. Moved the McBSP3_DR signal to pin AB25. 3. Moved the McBSP3_CLKX signal to pin AD25. 4. Changes were to allow access to three PWM signals from OMAP3530.	12/16/08	GC
C3	1. Added series resistor to BKBAT. 2. Added TP to BKBAT to allow access for battery. 3. Added a 47pf CAP and 3.3uH inductor to the S-Video feedback resistors.	2/11/2009	GC
C3A	1. Switched to TPS65950 based on the availability of the parts. 2. Made the batttery an installed component. Removed parallell resistor.	4/21/2009	GC
C3B	1. Corrected J4 and J5 symbol for the RGB interface.No electrical changes were made. 2. Removed battery as an installed component due to availability issues.	4/30/2009	GC
C4	1. Added C141, 22uF in parallell with C97. 2. Added option to allow the USB PHY and CLKOUT to be powered from the VIO_1V8 rail or the VAUX2 rail from the TPS65950. Default is VIO_1V8 rail. 3. Changed 1.8V filter CAP on USB PHY to 22uf. 4. Made R113 a DNI and installed R112.	10/5/2009	GC
C4A	1. Made R67 an installed inductor and made R68 a DNI. Switched to LDO powered EHCI USB Phy.	11/5/2009	GC

CONTENTS

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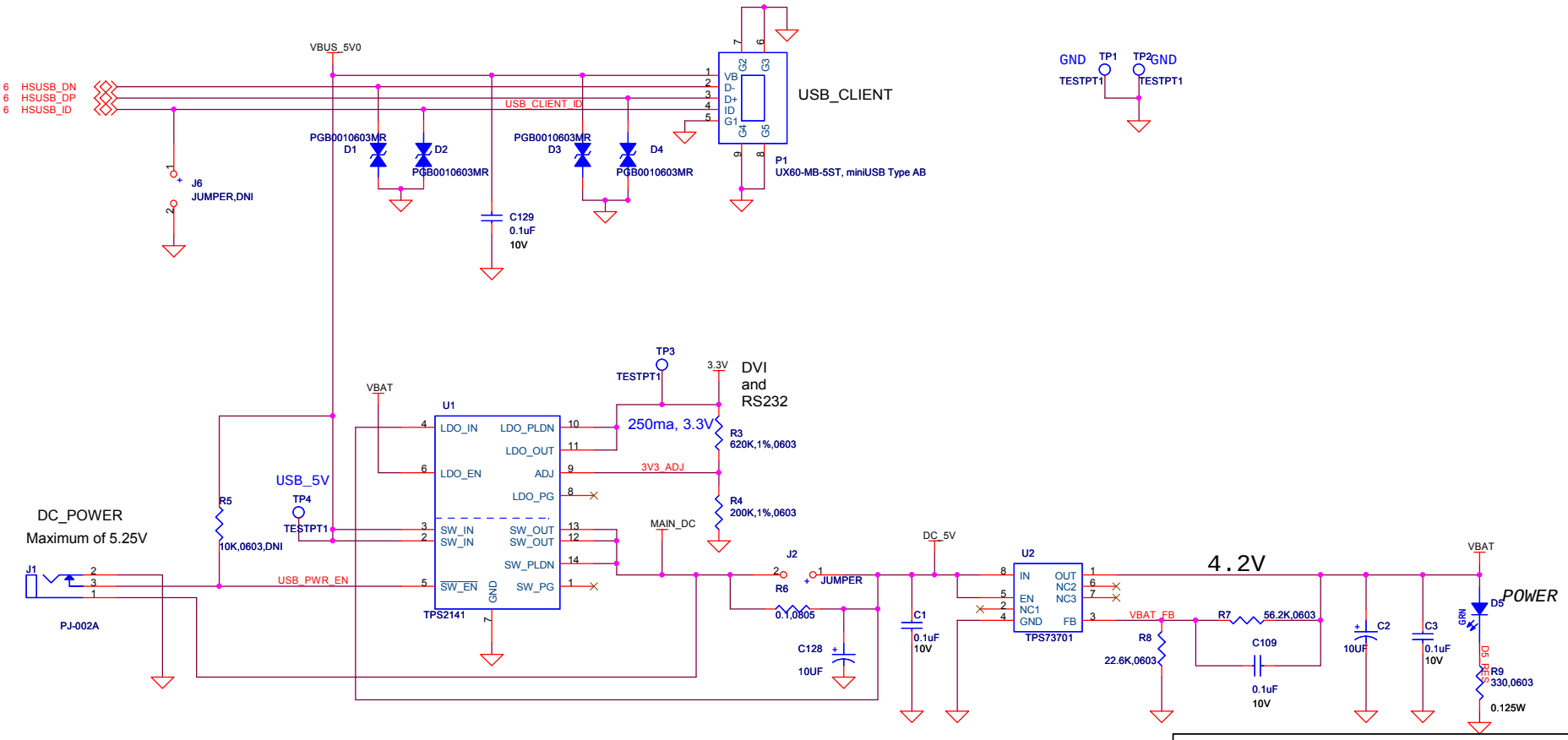

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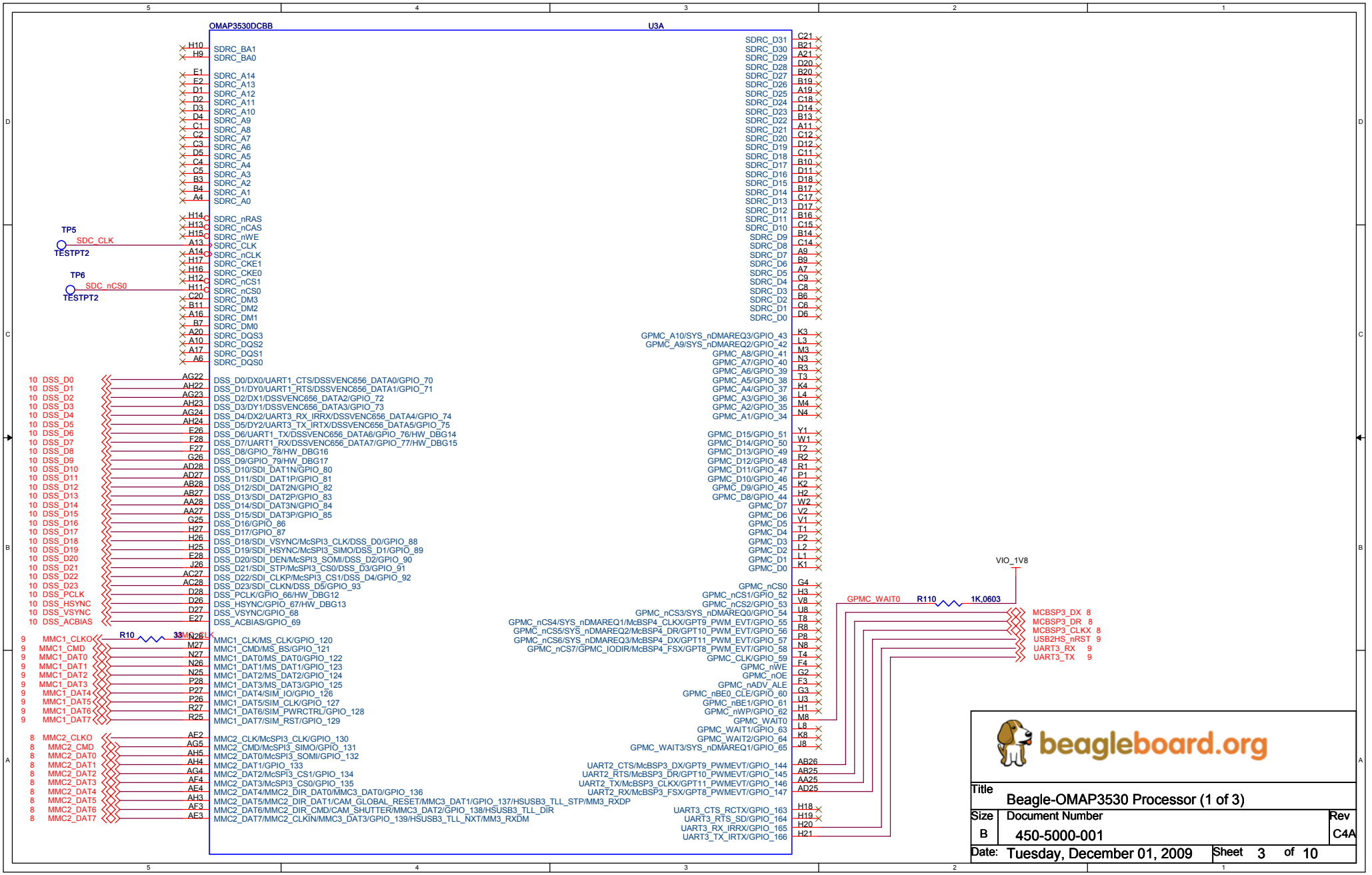
OMAP3530DCBB
U3A
SDRC_BA1
SDRC_BA0
SDRC_A14
SDRC_A13
SDRC_A12
SDRC_A11
SDRC_A10
SDRC_A9
SDRC_A8
SDRC_A7
SDRC_A6
SDRC_A5
SDRC_A4
SDRC_A3
SDRC_A2
SDRC_A1
SDRC_A0
SDRC_nRAS
SDRC_nCAS
SDRC_nWE
SDRC_CLK
SDRC_nCLK
SDRC_CKE1
SDRC_CKE0
SDRC_nCS1
SDRC_nCS0
SDRC_DM3
SDRC_DM2
SDRC_DM1
SDRC_DM0
SDRC_DQS3
SDRC_DQS2
SDRC_DQS1
SDRC_DQS0
TP5
SDC_CLK
TESTPT2
TP6
SDC_nCS0
TESTPT2
DSS_D0/DX0/UART1_CTS/DSSVENC656_DATA0/GPIO_70
DSS_D1/DY0/UART1_RTS/DSSVENC656_DATA1/GPIO_71
DSS_D2/DX1/DSSVENC656_DATA2/GPIO_72
DSS_D3/DY1/DSSVENC656_DATA3/GPIO_73
DSS_D4/DX2/UART3_RX_IRRX/DSSVENC656_DATA4/GPIO_74
DSS_D5/DY2/UART3_TX_IRTX/DSSVENC656_DATA5/GPIO_75
DSS_D6/UART1_TX/DSSVENC656_DATA6/GPIO_76/HW_DBG14
DSS_D7/UART1_RX/DSSVENC656_DATA7/GPIO_77/HW_DBG15
DSS_D8/GPIO_78/HW_DBG16
DSS_D9/GPIO_79/HW_DBG17
DSS_D10/SDI_DAT1N/GPIO_80
DSS_D11/SDI_DAT1P/GPIO_81
DSS_D12/SDI_DAT2N/GPIO_82
DSS_D13/SDI_DAT2P/GPIO_83
DSS_D14/SDI_DAT3N/GPIO_84
DSS_D15/SDI_DAT3P/GPIO_85
DSS_D16/GPIO_86
DSS_D17/GPIO_87
DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_D0/GPIO_88
DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_D1/GPIO_89
DSS_D20/SDI_DEN/McSPI3_SOMI/DSS_D2/GPIO_90
DSS_D21/SDI_STP/McSPI3_CS0/DSS_D3/GPIO_91
DSS_D22/SDI_CLKP/McSPI3_CS1/DSS_D4/GPIO_92
DSS_D23/SDI_CLKN/DSS_D5/GPIO_93
DSS_PCLK/GPIO_66/HW_DBG12
DSS_HSYNC/GPIO_67/HW_DBG13
DSS_VSYNC/GPIO_68
DSS_ACBIAS/GPIO_69
R10
33
MMC1_CLK/MS_CLK/GPIO_120
MMC1_CMD/MS_BS/GPIO_121
MMC1_DAT0/MS_DAT0/GPIO_122
MMC1_DAT1/MS_DAT1/GPIO_123
MMC1_DAT2/MS_DAT2/GPIO_124
MMC1_DAT3/MS_DAT3/GPIO_125
MMC1_DAT4/SIM_IO/GPIO_126
MMC1_DAT5/SIM_CLK/GPIO_127
MMC1_DAT6/SIM_PWRCTRL/GPIO_128
MMC1_DAT7/SIM_RST/GPIO_129
MMC2_CLK/McSPI3_CLK/GPIO_130
MMC2_CMD/McSPI3_SIMO/GPIO_131
MMC2_DAT0/McSPI3_SOMI/GPIO_132
MMC2_DAT1/GPIO_133
MMC2_DAT2/McSPI3_CS1/GPIO_134
MMC2_DAT3/McSPI3_CS0/GPIO_135
MMC2_DAT4/MMC2_DIR_DAT0/MMC3_DAT0/GPIO_136
MMC2_DAT5/MMC2_DIR_DAT1/CAM_GLOBAL_RESET/MMC3_DAT1/GPIO_137/HSUSB3_TLL_STP/MM3_RXDP
MMC2_DAT6/MMC2_DIR_CMD/CAM_SHUTTER/MMC3_DAT2/GPIO_138/HSUSB3_TLL_DIR
MMC2_DAT7/MMC2_CLKIN/MMC3_DAT3/GPIO_139/HSUSB3_TLL_NXT/MM3_RXDM
SDRC_D31
SDRC_D30
SDRC_D29
SDRC_D28
SDRC_D27
SDRC_D26
SDRC_D25
SDRC_D24
SDRC_D23
SDRC_D22
SDRC_D21
SDRC_D20
SDRC_D19
SDRC_D18
SDRC_D17
SDRC_D16
SDRC_D15
SDRC_D14
SDRC_D13
SDRC_D12
SDRC_D11
SDRC_D10
SDRC_D9
SDRC_D8
SDRC_D7
SDRC_D6
SDRC_D5
SDRC_D4
SDRC_D3
SDRC_D2
SDRC_D1
SDRC_D0
GPMC_A10/SYS_nDMAREQ3/GPIO_43
GPMC_A9/SYS_nDMAREQ2/GPIO_42
GPMC_A8/GPIO_41
GPMC_A7/GPIO_40
GPMC_A6/GPIO_39
GPMC_A5/GPIO_38
GPMC_A4/GPIO_37
GPMC_A3/GPIO_36
GPMC_A2/GPIO_35
GPMC_A1/GPIO_34
GPMC_D15/GPIO_51
GPMC_D14/GPIO_50
GPMC_D13/GPIO_49
GPMC_D12/GPIO_48
GPMC_D11/GPIO_47
GPMC_D10/GPIO_46
GPMC_D9/GPIO_45
GPMC_D8/GPIO_44
GPMC_D7
GPMC_D6
GPMC_D5
GPMC_D4
GPMC_D3
GPMC_D2
GPMC_D1
GPMC_D0
GPMC_nCS0
GPMC_nCS1/GPIO_52
GPMC_nCS2/GPIO_53
GPMC_nCS3/SYS_nDMAREQ0/GPIO_54
GPMC_nCS4/SYS_nDMAREQ1/McBSP4_CLKX/GPT9_PWM_EVT/GPIO_55
GPMC_nCS5/SYS_nDMAREQ2/McBSP4_DR/GPT10_PWM_EVT/GPIO_56
GPMC_nCS6/SYS_nDMAREQ3/McBSP4_DX/GPT11_PWM_EVT/GPIO_57
GPMC_nCS7/GPMC_IODIR/McBSP4_FSX/GPT8_PWM_EVT/GPIO_58
GPMC_CLK/GPIO_59
GPMC_nWE
GPMC_nOE
GPMC_nADV_ALE
GPMC_nBE0_CLE/GPIO_60
GPMC_nBE1/GPIO_61
GPMC_nWP/GPIO_62
GPMC_WAIT0
GPMC_WAIT1/GPIO_63
GPMC_WAIT2/GPIO_64
GPMC_WAIT3/SYS_nDMAREQ1/GPIO_65
UART2_CTS/McBSP3_DX/GPT9_PWMEVT/GPIO_144
UART2_RTS/McBSP3_DR/GPT10_PWMEVT/GPIO_145
UART2_TX/McBSP3_CLKX/GPT11_PWMEVT/GPIO_146
UART2_RX/McBSP3_FSX/GPT8_PWMEVT/GPIO_147
UART3_CTS_RCTX/GPIO_163
UART3_RTS_SD/GPIO_164
UART3_RX_IRRX/GPIO_165
UART3_TX_IRTX/GPIO_166
VIO_1V8
GPMC_WAIT0
R110
1K,0603
MCBSP3_DX 8
MCBSP3_DR 8
MCBSP3_CLKX 8
USB2HS_nRST 9
UART3_RX 9
UART3_TX 9
beagleboard.org
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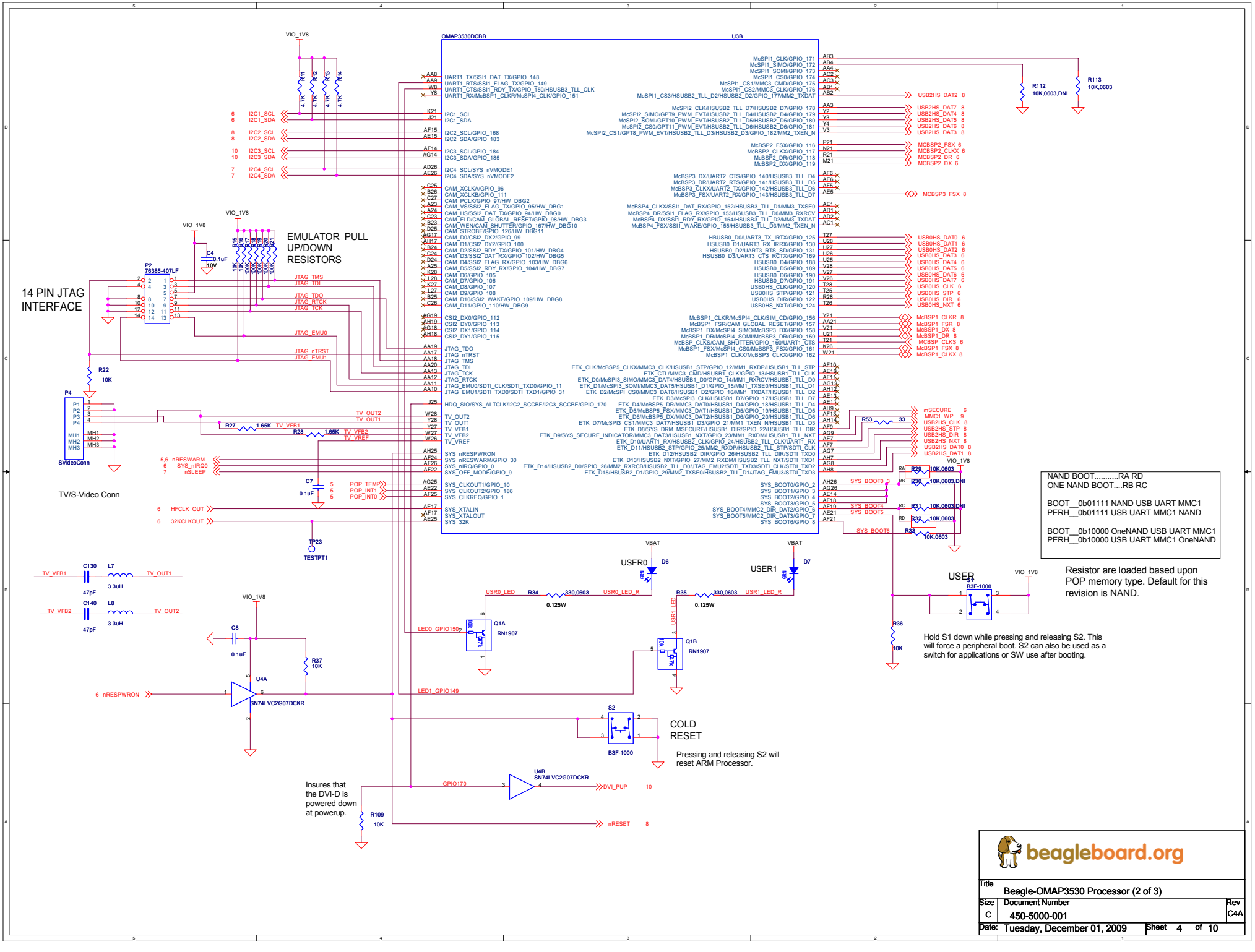
OMAP3530DCBB
U3B
14 PIN JTAG INTERFACE
EMULATOR PULL UP/DOWN RESISTORS
TV/S-Video Conn
USER0
USER1
USER
COLD RESET
Pressing and releasing S2 will reset ARM Processor.
Insures that the DVI-D is powered down at powerup.
Hold S1 down while pressing and releasing S2. This will force a peripheral boot. S2 can also be used as a switch for applications or SW use after booting.
NAND BOOT.....RA RD
ONE NAND BOOT....RB RC
BOOT__0b01111 NAND USB UART MMC1
PERH__0b01111 USB UART MMC1 NAND
BOOT__0b10000 OneNAND USB UART MMC1
PERH__0b10000 USB UART MMC1 OneNAND
Resistor are loaded based upon POP memory type. Default for this revision is NAND.
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Title
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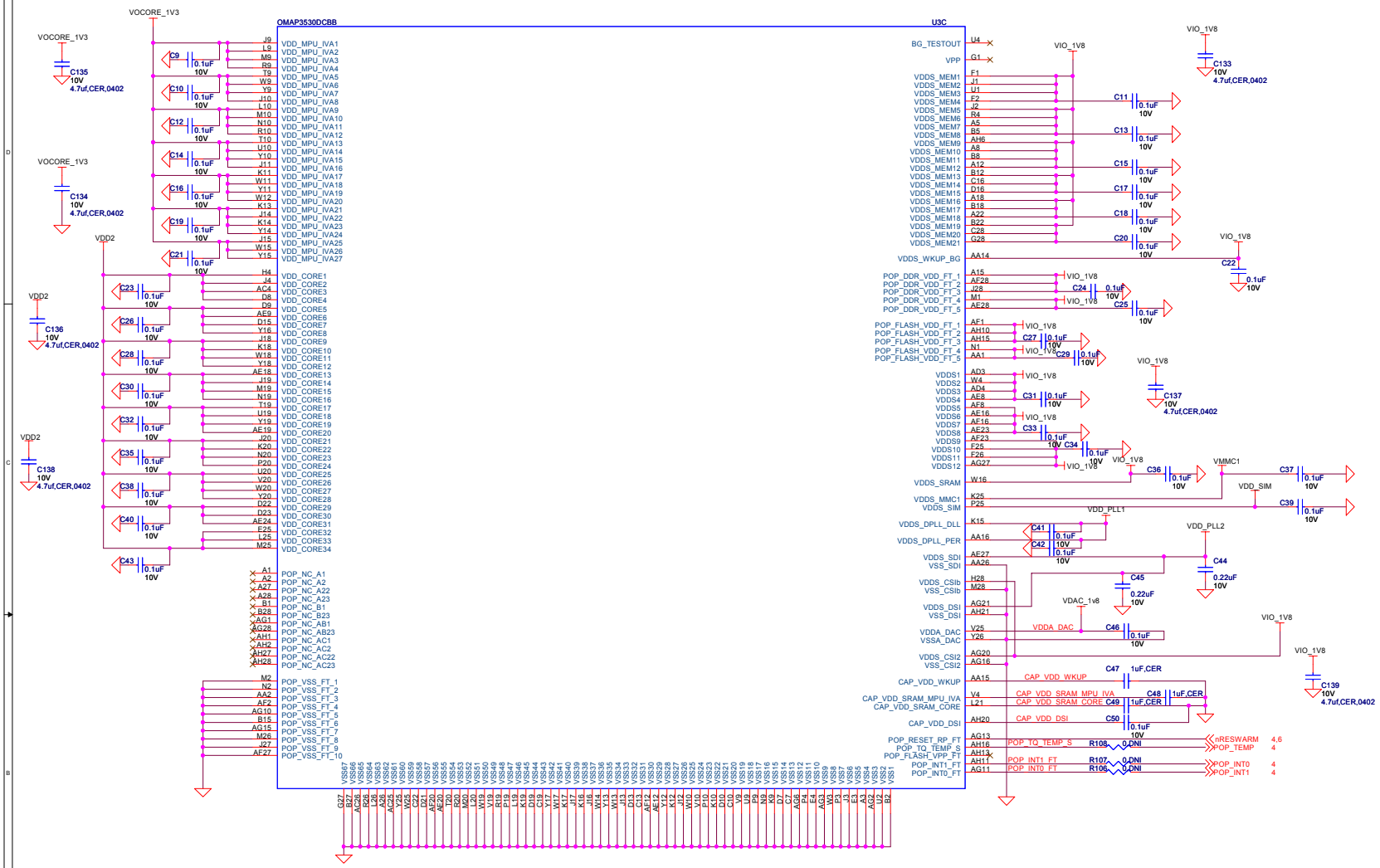

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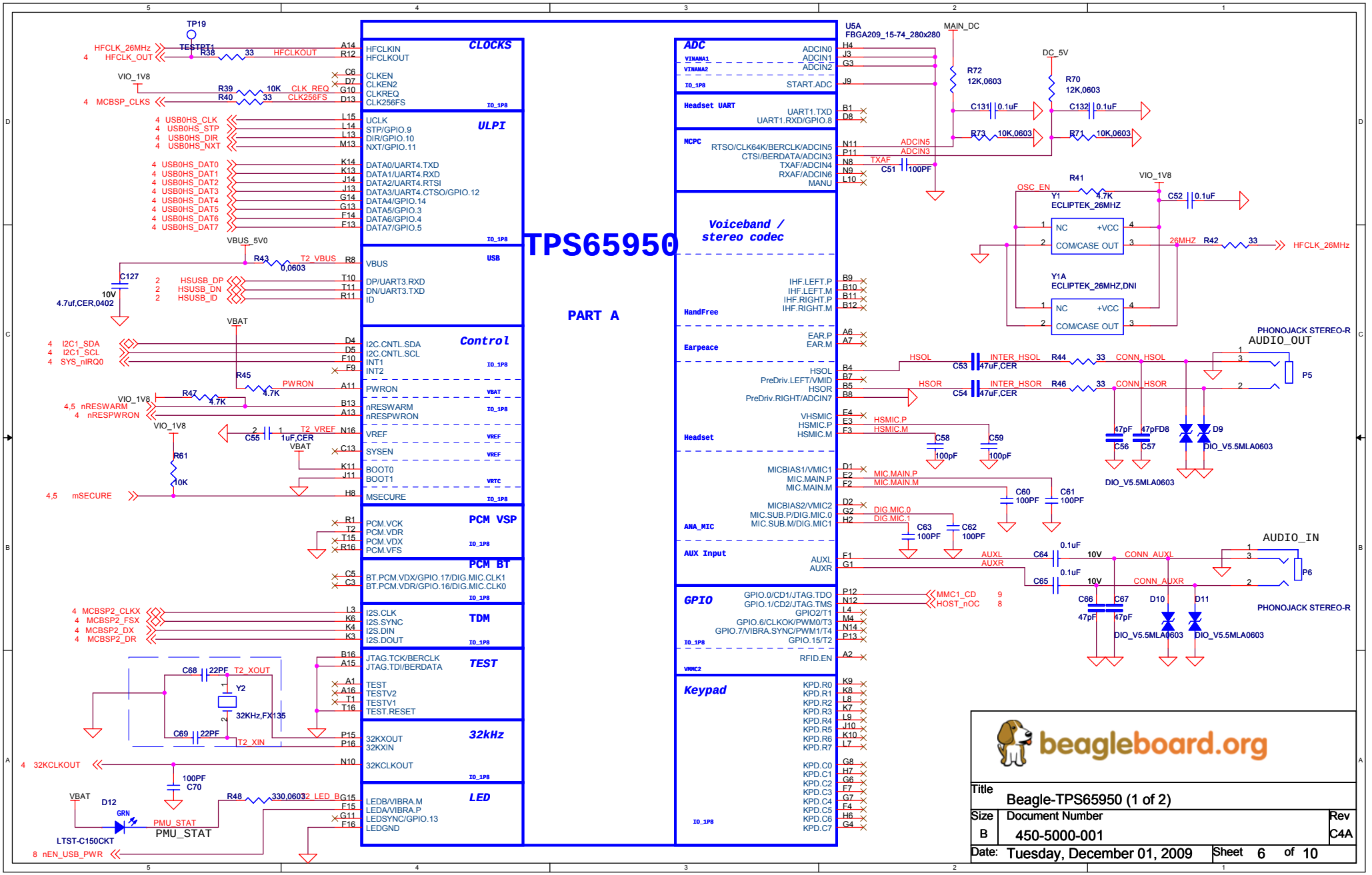
TPS65950
PART A
CLOCKS
HFCLKIN
HFCLKOUT
CLKEN
CLKEN2
CLKREQ
CLK256FS
ULPI
UCLK
STP/GPIO.9
DIR/GPIO.10
NXT/GPIO.11
DATA0/UART4.TXD
DATA1/UART4.RXD
DATA2/UART4.RTSI
DATA3/UART4.CTSO/GPIO.12
DATA4/GPIO.14
DATA5/GPIO.3
DATA6/GPIO.4
DATA7/GPIO.5
USB
VBUS
DP/UART3.RXD
DN/UART3.TXD
ID
Control
I2C.CNTL.SDA
I2C.CNTL.SCL
INT1
INT2
PWRON
nRESWARM
nRESPWRON
VREF
SYSEN
BOOT0
BOOT1
MSECURE
PCM VSP
PCM.VCK
PCM.VDR
PCM.VDX
PCM.VFS
PCM BT
BT.PCM.VDX/GPIO.17/DIG.MIC.CLK1
BT.PCM.VDR/GPIO.16/DIG.MIC.CLK0
TDM
I2S.CLK
I2S.SYNC
I2S.DIN
I2S.DOUT
TEST
JTAG.TCK/BERCLK
JTAG.TDI/BERDATA
TEST
TESTV2
TESTV1
TEST.RESET
32kHz
32KXOUT
32KXIN
32KCLKOUT
LED
LEDB/VIBRA.M
LEDA/VIBRA.P
LEDSYNC/GPIO.13
LEDGND
ADC
ADCIN0
ADCIN1
ADCIN2
START.ADC
Headset UART
UART1.TXD
UART1.RXD/GPIO.8
MCPC
RTSO/CLK64K/BERCLK/ADCIN5
CTSI/BERDATA/ADCIN3
TXAF/ADCIN4
RXAF/ADCIN6
MANU
Voiceband / stereo codec
IHF.LEFT.P
IHF.LEFT.M
IHF.RIGHT.P
IHF.RIGHT.M
HandFree
EAR.P
EAR.M
Earpeace
HSOL
PreDriv.LEFT/VMID
HSOR
PreDriv.RIGHT/ADCIN7
VHSMIC
HSMIC.P
HSMIC.M
Headset
MICBIAS1/VMIC1
MIC.MAIN.P
MIC.MAIN.M
MICBIAS2/VMIC2
MIC.SUB.P/DIG.MIC.0
MIC.SUB.M/DIG.MIC1
ANA_MIC
AUX Input
AUXL
AUXR
GPIO
GPIO.0/CD1/JTAG.TDO
GPIO.1/CD2/JTAG.TMS
GPIO2/T1
GPIO.6/CLKOK/PWM0/T3
GPIO.7/VIBRA.SYNC/PWM1/T4
GPIO.15/T2
RFID.EN
Keypad
KPD.R0
KPD.R1
KPD.R2
KPD.R3
KPD.R4
KPD.R5
KPD.R6
KPD.R7
KPD.C0
KPD.C1
KPD.C2
KPD.C3
KPD.C4
KPD.C5
KPD.C6
KPD.C7
U5A
FBGA209_15-74_280x280
MAIN_DC
DC_5V
R72 12K,0603
R70 12K,0603
C131 0.1uF
C132 0.1uF
R73 10K,0603
R71 10K,0603
C51 100PF
R41 4.7K
Y1 ECLIPTEK_26MHZ
Y1A ECLIPTEK_26MHZ,DNI
C52 0.1uF
26MHZ
R42 33
HFCLK_26MHz
OSC_EN
VIO_1V8
AUDIO_OUT
PHONOJACK STEREO-R
P5
C53 47uF,CER
C54 47uF,CER
R44 33
R46 33
C58 100pF
C59 100pF
C56 47pF
C57 47pFD8
D9
DIO_V5.5MLA0603
C60 100PF
C61 100PF
C63 100PF
C62 100PF
AUDIO_IN
P6
C64 0.1uF
C65 0.1uF
C66 47pF
C67 47pF
D10
D11
MMC1_CD
HOST_nOC
TP19
TESTPT1
R38 33
C6
D7
G10
D13
R39 10K
R40 33
CLK_REQ
CLK256FS
VBUS_5V0
R43 0,0603
T2_VBUS
C127 10V 4.7uf,CER,0402
HSUSB_DP
HSUSB_DN
HSUSB_ID
VBAT
R45 4.7K
PWRON
R47 4.7K
C55 1uF,CER
T2_VREF
R61 10K
mSECURE
C68 22PF
T2_XOUT
Y2
32KHz,FX135
C69 22PF
T2_XIN
100PF C70
D12
GRN
LTST-C150CKT
R48 330,0603
PMU_STAT
nEN_USB_PWR
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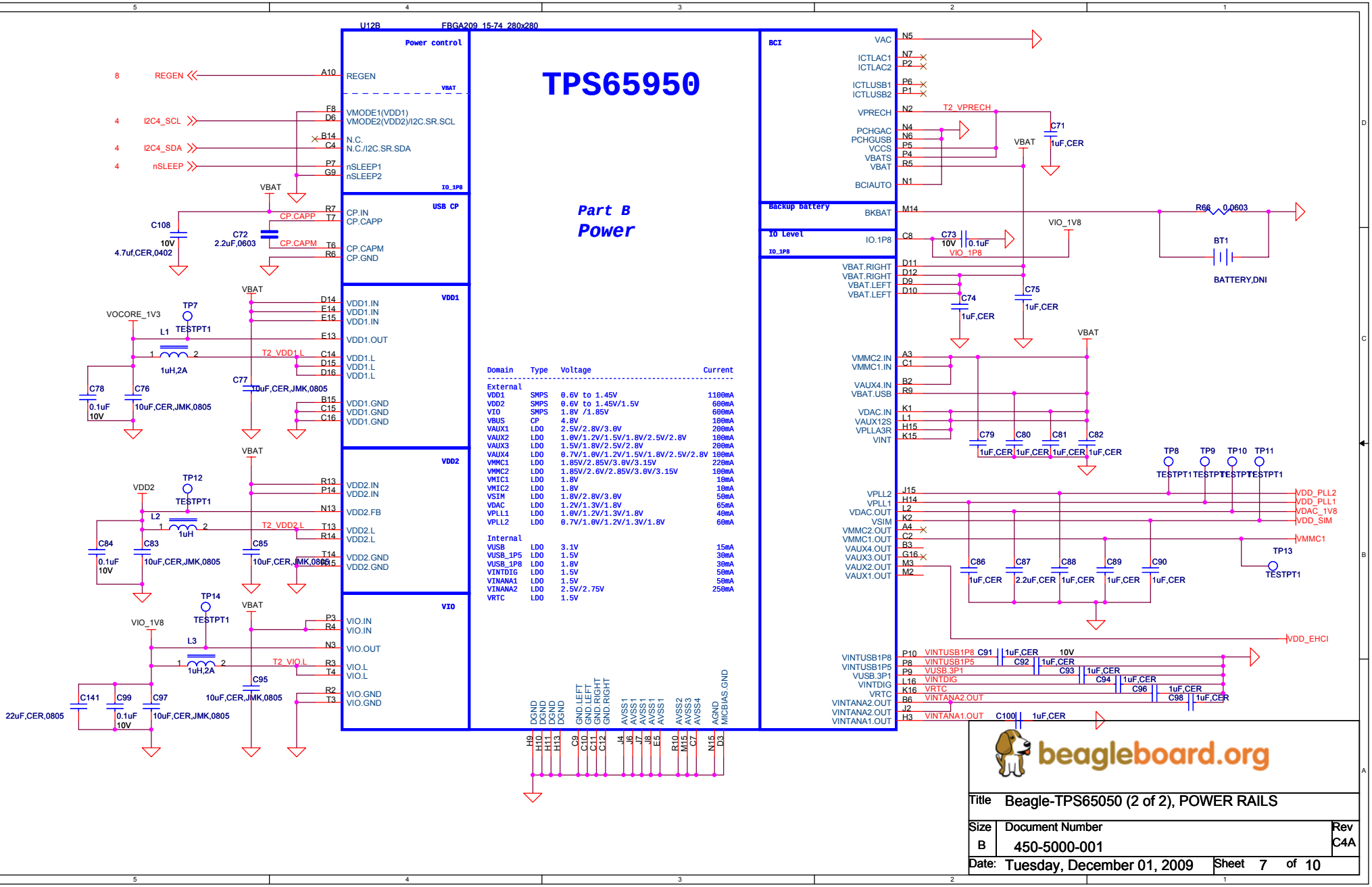
U12B
FBGA209_15-74_280x280
TPS65950
Part B
Power
Power control
USB CP
VDD1
VDD2
VIO
BCI
Backup Battery
IO Level
REGEN
VMODE1(VDD1)
VMODE2(VDD2)/I2C.SR.SCL
N.C.
N.C./I2C.SR.SDA
nSLEEP1
nSLEEP2
CP.IN
CP.CAPP
CP.CAPM
CP.GND
VDD1.IN
VDD1.OUT
VDD1.L
VDD1.GND
VDD2.IN
VDD2.FB
VDD2.L
VDD2.GND
VIO.IN
VIO.OUT
VIO.L
VIO.GND
VAC
ICTLAC1
ICTLAC2
ICTLUSB1
ICTLUSB2
VPRECH
PCHGAC
PCHGUSB
VCCS
VBATS
VBAT
BCIAUTO
BKBAT
IO.1P8
VBAT.RIGHT
VBAT.LEFT
VMMC2.IN
VMMC1.IN
VAUX4.IN
VBAT.USB
VDAC.IN
VAUX12S
VPLLA3R
VINT
VPLL2
VPLL1
VDAC.OUT
VSIM
VMMC2.OUT
VMMC1.OUT
VAUX4.OUT
VAUX3.OUT
VAUX2.OUT
VAUX1.OUT
VINTUSB1P8
VINTUSB1P5
VUSB.3P1
VINTDIG
VRTC
VINTANA2.OUT
VINTANA1.OUT
Domain Type Voltage Current
External
VDD1 SMPS 0.6V to 1.45V 1100mA
VDD2 SMPS 0.6V to 1.45V/1.5V 600mA
VIO SMPS 1.8V /1.85V 600mA
VBUS CP 4.8V 100mA
VAUX1 LDO 2.5V/2.8V/3.0V 200mA
VAUX2 LDO 1.0V/1.2V/1.5V/1.8V/2.5V/2.8V 100mA
VAUX3 LDO 1.5V/1.8V/2.5V/2.8V 200mA
VAUX4 LDO 0.7V/1.0V/1.2V/1.5V/1.8V/2.5V/2.8V 100mA
VMMC1 LDO 1.85V/2.85V/3.0V/3.15V 220mA
VMMC2 LDO 1.85V/2.6V/2.85V/3.0V/3.15V 100mA
VMIC1 LDO 1.8V 10mA
VMIC2 LDO 1.8V 10mA
VSIM LDO 1.8V/2.8V/3.0V 50mA
VDAC LDO 1.2V/1.3V/1.8V 65mA
VPLL1 LDO 1.0V/1.2V/1.3V/1.8V 40mA
VPLL2 LDO 0.7V/1.0V/1.2V/1.3V/1.8V 60mA
Internal
VUSB LDO 3.1V 15mA
VUSB_1P5 LDO 1.5V 30mA
VUSB_1P8 LDO 1.8V 30mA
VINTDIG LDO 1.5V 50mA
VINANA1 LDO 1.5V 50mA
VINANA2 LDO 2.5V/2.75V 250mA
VRTC LDO 1.5V
T2_VPRECH
T2_VDD1_L
T2_VDD2_L
T2_VIO_L
VOCORE_1V3
VIO_1V8
VDD_PLL2
VDD_PLL1
VDAC_1V8
VDD_SIM
VMMC1
VDD_EHCI
BATTERY,DNI
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Title Beagle-TPS65050 (2 of 2), POWER RAILS
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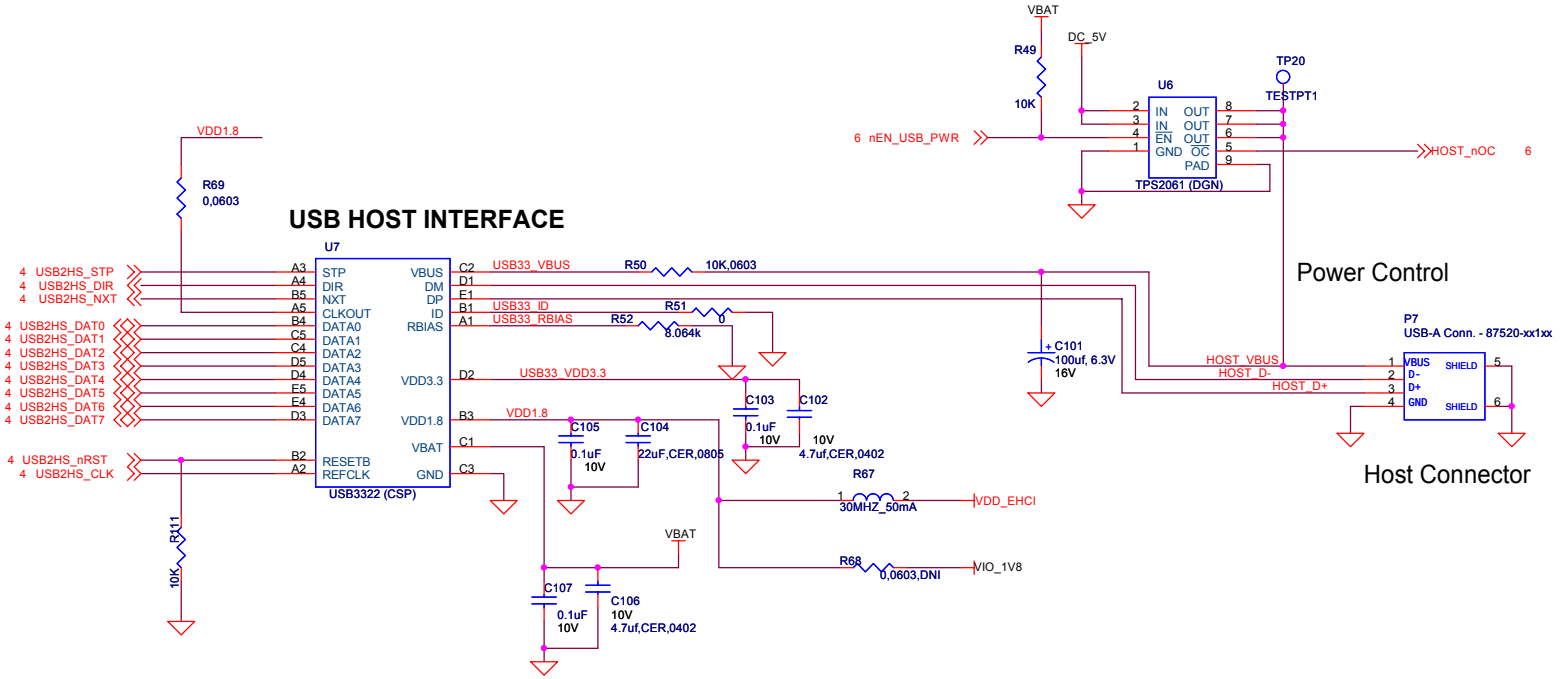

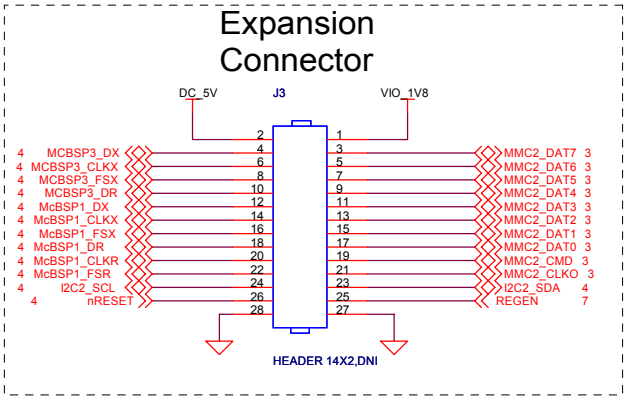

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Title	Beagle-USB Host and Expansion Connector.	
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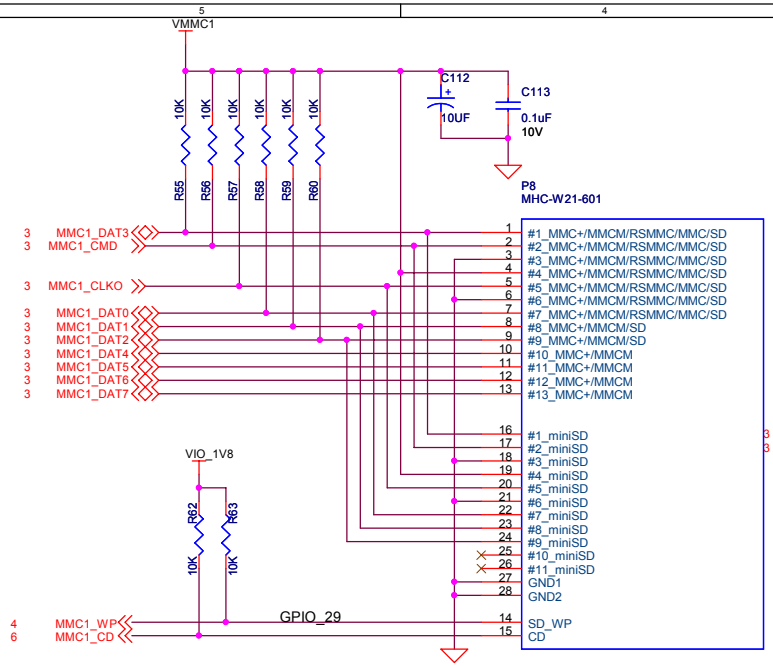
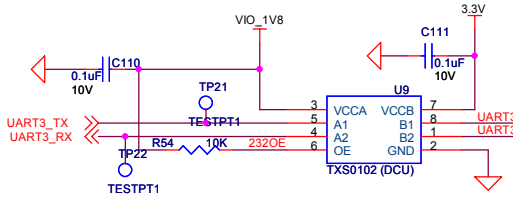
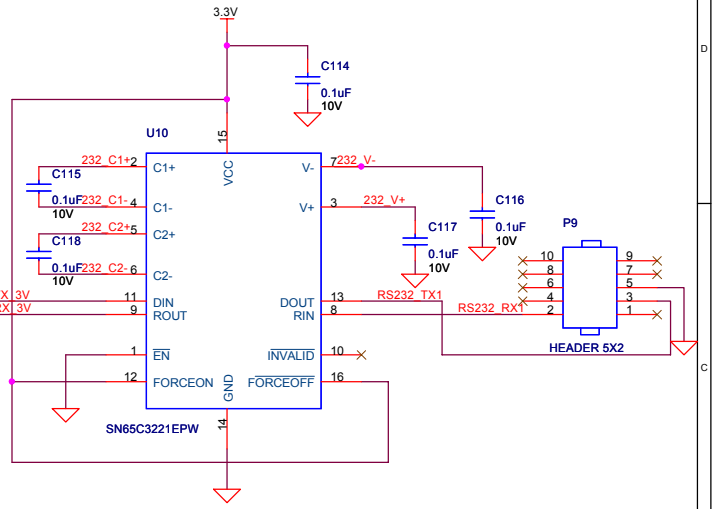
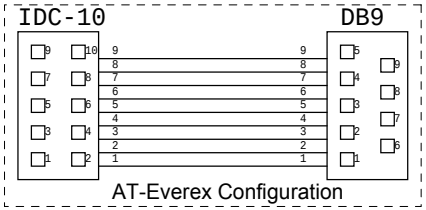


SD/MMC Connector 6 in 1
MMC+, MMCMobile, SD,
MMC, miniSD, RS-MMC



UART3 Serial Port





AT-Everex Configuration

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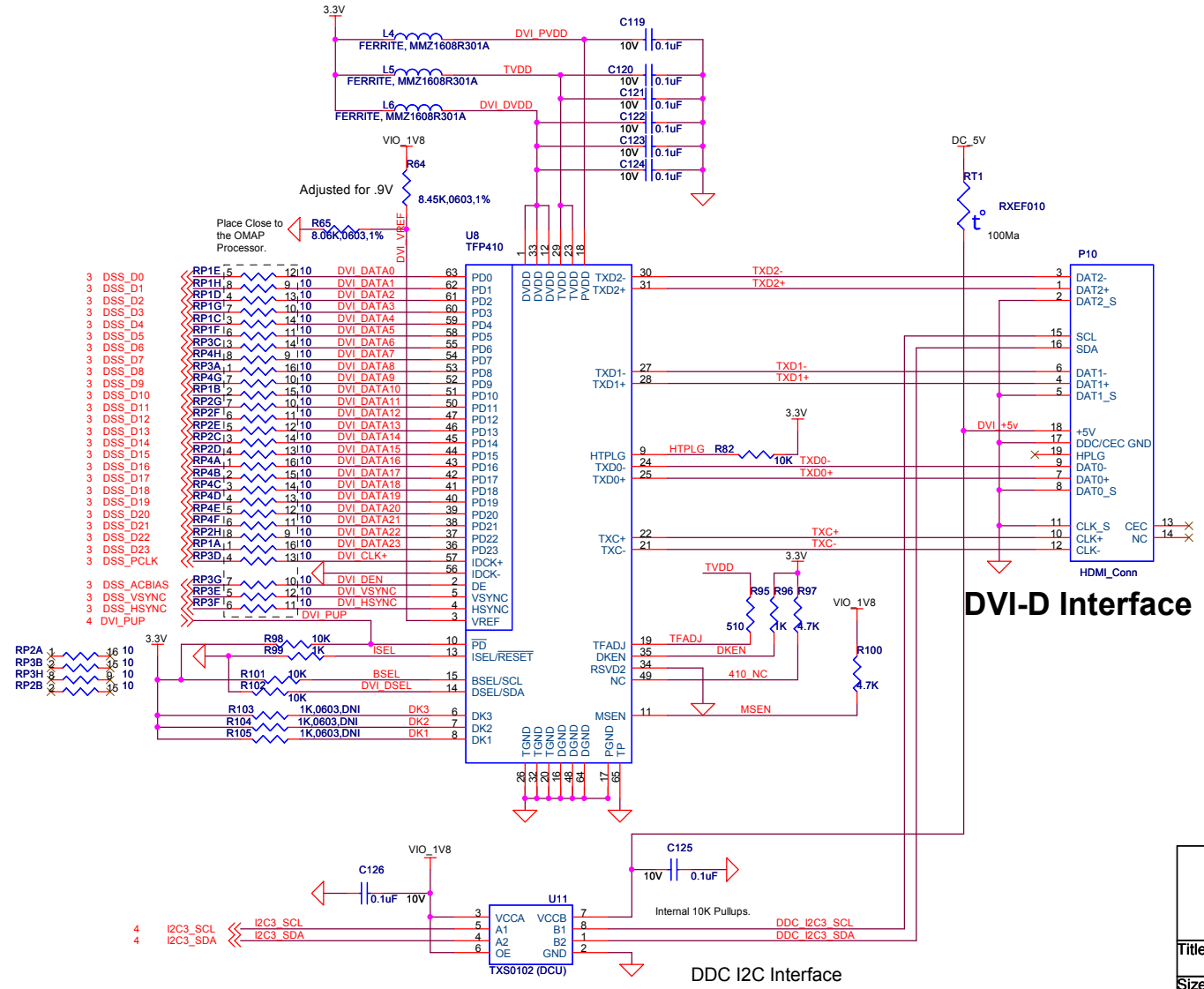

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