User's Manual

Under Development Confidential

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RTK00V2XRC7746SFS

User's Manual: Hardware

— Preliminary —

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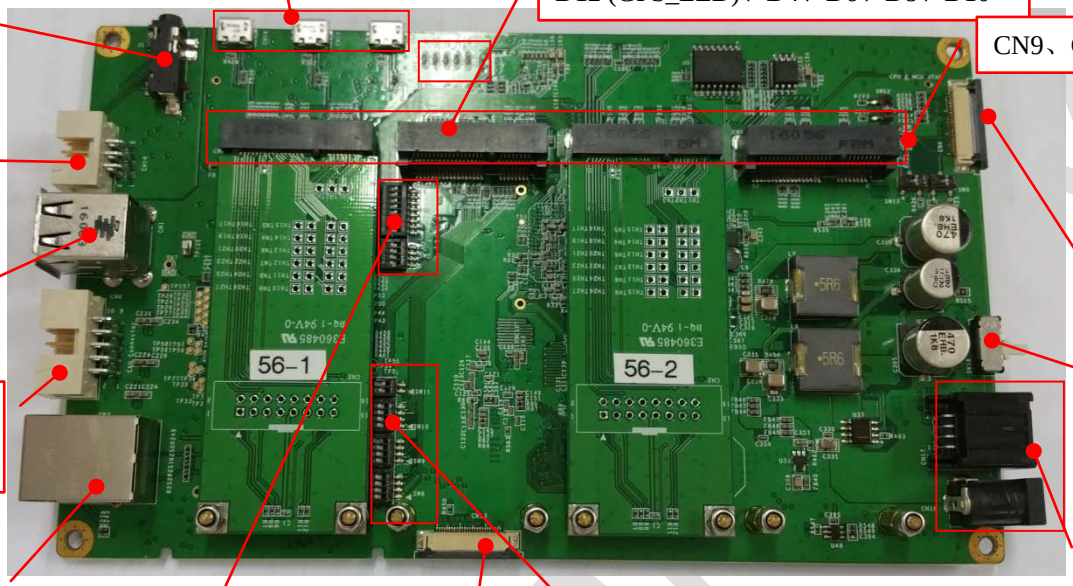
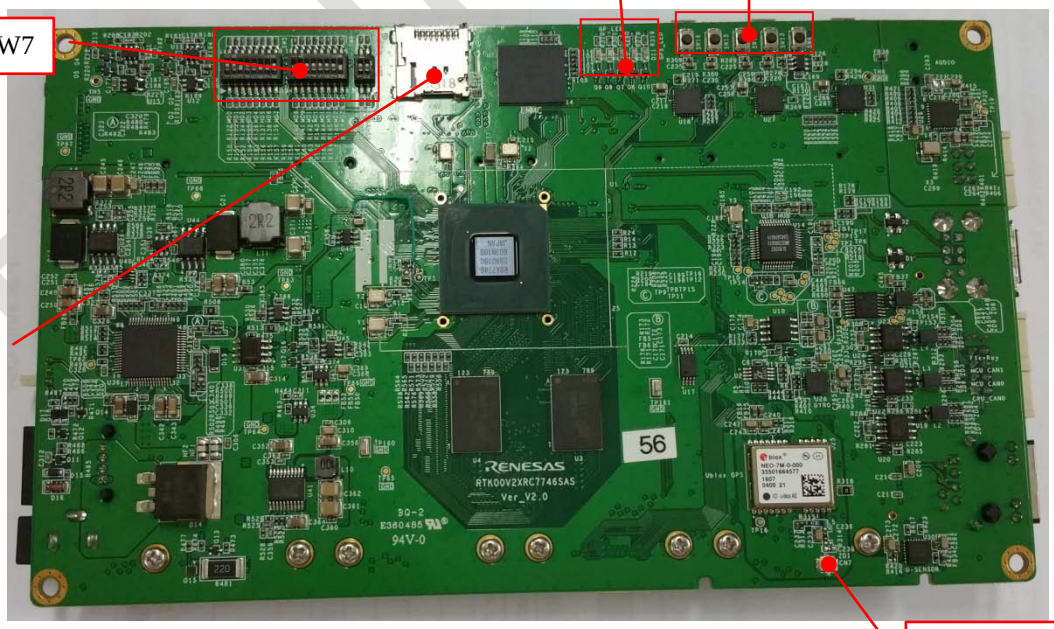
1 Overview

The Tethys board is R-Car W2H-specific evaluation board that can be used to evaluate systems using the R-Car W2H and to develop operating systems, device drivers, and applications. Using the Tethys board allows developers to efficiently conduct required tasks such as evaluating the performance of R-Car W2H-based systems, thus greatly reducing turn-around times in product development.





1.1 Features

1.1.1 Features of the Tethys Board

Table 1 Features of the Tethys Board

Item	Description
CPU	・U1:R-Car W2H (Operating clock: ARM 1.0GHz(Max), SH-4AL 260MHz)
MCU	・U32:RH850F1H/F1L (Operating clock: RH850F1H 120MHz, RH850F1L 60MHz)
Audio Interfaces	・J1: (1) L/R Audio output for SSI0 (2) Microphone input for SSI1
Connectors	・CN6:CAN & Flexray Connector(Flexray not support) ・CN7:GPS ANT Connector ・CN14:HSM Connector(not support) ・CN13:ETNB Connector (not support)
PCIE Connectors	・CN9:Mini PCIE Connector for V2X Sub Board ・CN8:Mini PCIE Connector for EtherAVB Sub Board(not support) ・CN12:Mini PCIE Connector for V2X Sub Board ・CN11:Standard Mini PCIE
Debugger Interfaces	・CN4:26 pin FPC connector for CPU and MCU. ・CN10:UART-USB for Debug ・CN5:UART-USB for CPU Debug ・CN16:UART-USB for MCU Debug
Network Interfaces	・CN3:10M/100M Ethernet connector for Ethernet MAC
Storage Interfaces	・CN1:USB2.0 type A receptacle x 2 ・CN2:SD card slots for SDHI2 ・eMMC memory for MMC
Power Supply	・CN17 or CN18: DC 12V input

1.1.2 Functions of the Tethys Board

Table 2 List of Tethys Board Functions

Board Function	Tethys
RAM	DDR3 I/F : DDR3-SDRAM 1066MHz 1 GB x2
USB 2.0	USB2.0 CH0 : USB2.0 type A
	USB2.0 CH1 : USB2.0 type A
SDHI	SDHI0 : Mini PCIE Connector for V2X Sub Board
	SDHI2 : SD card slots , Mini PCIE Connector for V2X Sub Board
SCIF	SCIF0_D/HSCIF0_B : (1) Mini PCIE Connector for V2X Sub Board , (2) UART-USB
	SCIF3_B/HSCIF2 : Mini PCIE Connector for V2X Sub Board
	SCIF2_B(Debug serial) : UART-USB for CPU Debug
	SCIF5_C : GPS Module
ROM(QSPI)	QSPI0 : SPI Flash 64MB
	QSPI1 : SPI Flash 4MB
Ether MAC / Ether AVB	Ether MAC : RJ45 Connector
	Ether AVB : Mini PCIE Connector for Ether AVB Sub Board (Ether AVB not support)
HSCIF	HSCIF1_A : Mini PCIE Connector for Ether AVB Sub Board (Ether AVB not support)
	SCIF0_D/HSCIF0_B : (1) Mini PCIE Connector for V2X Sub Board , (2) UART-USB
	SCIF3_B/HSCIF2 : Mini PCIE Connector for V2X Sub Board
I2C	I2C1_A/SPI : HSM Connector (not support)
	I2C1_A : G-Sensor , Gyro , MCU
SSI	SSI0,1,2,9 : Audio CODEC
MSIOF	MSIOF1_B : MCU [Flexray (not support)、Ethernet AVB not support]
MMC	MMC : eMMC(8GB)
PCI Express	Mini PCIE Connector
CAN	W2H CAN channel support, RH850 CAN0/1 support ,Flexray not support
Debug I/F	DBG : TO Sub Connector
VCC	Power Block

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1.2 Usage Notes

1.2.1 Specifications of the Tethys Board

When the AC adapter is connected to the outlet, the 12V DC power is supplied to the Tethys board and some of the circuitry start operating. Setting the ACC switch (SW18) to the ON side after that leads to the generation of various power supply levels including 5V DC and 3.3V DC from the 12V DC power.

- Take particular care to ensure the correct configurations of the jumpers and switches mounted on the Tethys board. Incorrect configurations may damage on-board devices.
- For power supply to the Tethys, be sure to use the power supply that comes with it. Applying a voltage greater than 12 V may damage devices on the Tethys board.
- There are sequences for turning on and off the power supply to the Tethys board. Be sure to obey the notes below when using the Tethys board.

(1) When turning on the power

Be sure to confirm that the ACC switch (SW18) is off before plugging the AC adapter into the power source.

It is prohibited to plug the AC adapter into a power source while the ACC switch (SW18) is on.

(2) When turning off the power

Be sure to turn off the ACC switch (SW18) before unplugging the AC adapter from the power source.

It is prohibited to unplug the AC adapter from the power source while the ACC switch (SW18) is on.

- The AC adapter that comes with the Tethys board can supply current up to 3A at 12V. If you intend sub board to PCIe connect on Tethys board, ensure that this does not lead to supply current exceeding 3A.

  If the system configuration is such that the current supply does exceed 3A, prepare a separate stabilized DC power supply that can supply more current at 12V.
- Regarding the dedicated socket for the R-Car W2H, neither disconnect it from nor connect it to the Tethys board; also, regarding the R-Car W2H, neither remove it from nor insert it in the dedicated socket. Both actions lead to malfunctions of R-Car W2H operation on the board due to loosening of contacts between the socket and the board and between the socket and the R-Car W2H.

1.3 Board Configuration

The Tethys board is composed of a single board whose size is 185 mm ×110 mm

1.3.1 Block Diagram of the Tethys Board

Figure 1 shows a block diagram of the Tethys board

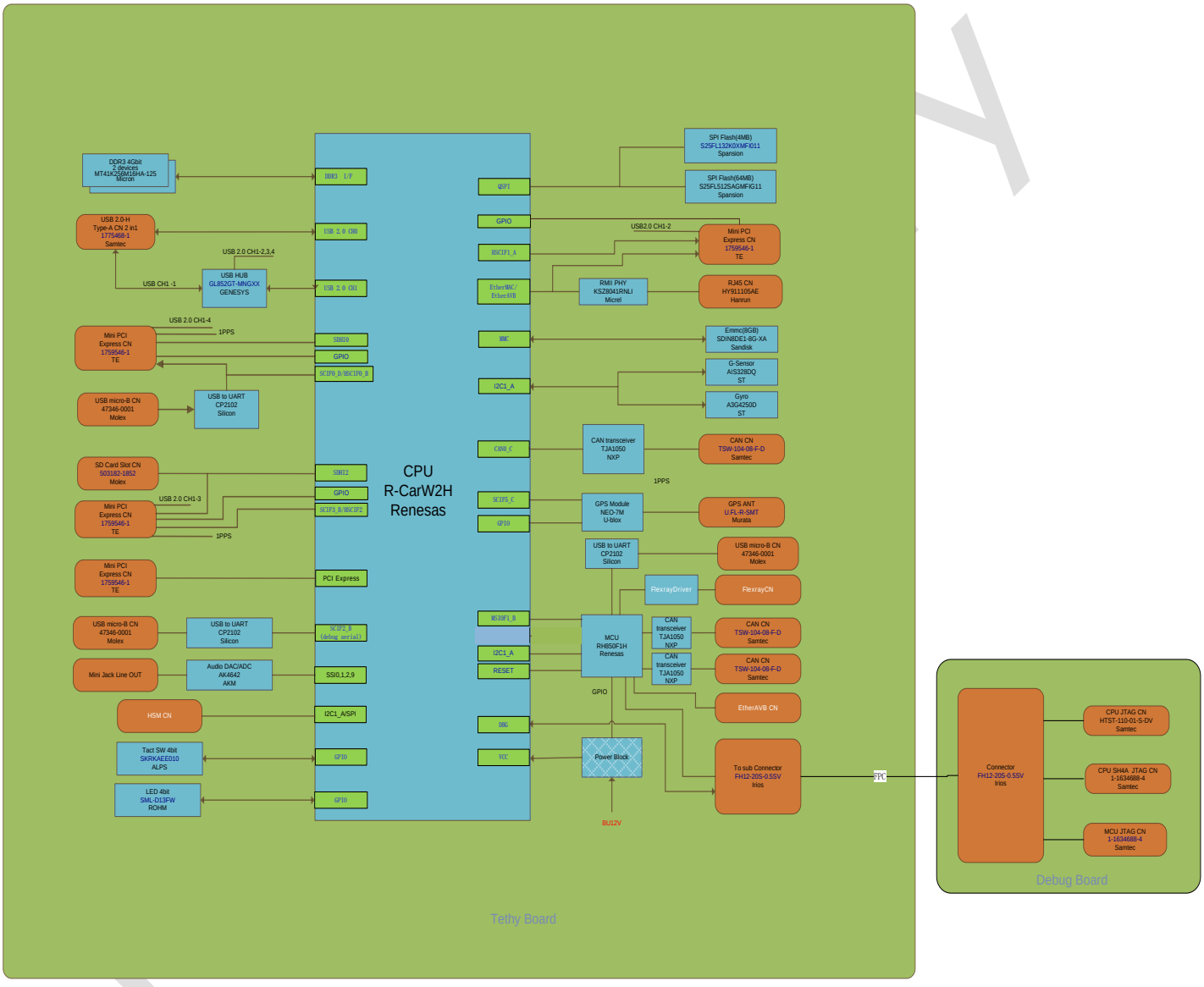


Figure 1 Block Diagram of the Tethys Board

Notice:

- White text means not support the function
  (HSM CN, Flexray_CN, EtherAVB CN)

2 Operating condition and antenna characteristic

2.1 Operating condition

Table 3 shows the operating condition. To use the Tethys board system, please keep the condition.

Table 3 Operating Condition

Item	Min	Typ	Max	Units
Input Voltage	7	12	25	V
Consumption Current	200	450	3000(*1)	mA
Operating Temperature	-25	25	+85	Degree C
V2X antenna Frequency range	5860		5920	MHz
V2X antenna VSWR			2.0	
V2X antenna Gain		2M Cable Type: (1)3.0(without cable loss) (2) -1.0(with cable loss) Rod Type: (1)5.0		dBi
V2X antenna Cable Loss		4.0 (L=2m)		dB
GPS antenna Center Frequency		1575 ± 3		MHz
GPS antenna VSWR			2.0	
GPS antenna Bandwidth	20			MHz
GPS antenna Gain		30		dB
Storage Temperature	-25		85	Degree C
Operating Humidity	25		85(*2)	%

Notice:

- (*1): 3000mA is the maximum current of AC adapter. If user need more current for Tethys board, user need prepare stable big current AC adapter.
- (*2):Humidity: No condensation.

3 Specifications of Interface Modules on the Tethys Board

This section describes the main function of the Tethys board, which includes the following sections:

3.1 Mode Setting

3.1.1 Specifications

The operating mode of the R-CarW2H is set by a power-on reset. For details on the operating mode, see the documents related to the R-CarW2H operating mode specifications.

3.1.2 MD0 Pin -Selection of Free-Running Mode or Step-Up Mode

Do not change the initial setting at shipment (MD0=0).

3.1.3 MD [3:1] Pins-Selection of Boot Device

These pins select the boot device.

MD3	MD2	MD1	Selection of Boot Device
0	0	0	External ROM boot (area 0)
0	0	1	eMMC boot via SDHI1
0	1	0	Serial flash ROM boot via QSPI; 16Kbytes transferred at 48.75 MHz
0	1	1	Reserved
1	0	0	Serial flash ROM boot via QSPI; 16Kbytes transferred at 39 MHz
1	0	1	Reserved
1	1	0	Serial flash ROM boot via QSPI; 4 Kbytes transferred at 39 MHz
1	1	1	Reserved

3.1.4 MD4 Pin-Selection of CS0 Space Size

This pin selects whether the area 0 space (CS0) is used as a normal space (64 Mbytes) or an expanded space (128 Mbytes).

MD4	Area Division
0	Area 0: 64 Mbytes
1	Area 0: 128 Mbytes

3.1.5 MD5 Pin-Reserved

Do not change the initial setting at shipment (MD5=1).

3.1.6 MD[7:6] Pins-Selection of Master Boot Processor

These pins select the master boot processor.

MD7	MD6	Selection of Master Boot Processor
0	0	Setting prohibited
0	1	Booted through CPU0 in CA7.
1	0	Booted through SH-4AL in 32-bit mode
1	1	Setting prohibited

3.1.7 MD8 Pin-Selection of Area 0 Space Data Bus Width

This pin sets the data bus width of the area 0 space (CS0) to 8 bits or 16 bits. Select the data bus width of the boot device connected to the LBSC.

MD8	EXBUS Area 0 Data Bus Width
0	8-bit bus
1	16-bit bus

3.1.8 MD9 Pin-Selection of Crystal Resonator or Crystal Oscillator

This pin selects either a crystal resonator or a crystal oscillator to be connected to the EXTAL/XTAL pins. A crystal oscillator (Y2: 20 MHz) is mounted on the Tethys board by default.

MD9	EXTAL/XTAL Pin Setting
0	An external clock is input to the EXTAL pin.
1	A crystal resonator is connected to the EXTAL and XTAL pins.

3.1.9 MD21, MD20, MD11, MD10, and MDT[1:0] Pins-Switching of JTAG, SDHI1, and SDHI2

These pins select the debugging function through the JTAG connector (CN4) or the SD card slot for the SDHI1. The debugging through the SDHI1 or SDHI2 is possible by the combination of MD pin settings in the R-CarW2H specifications.

MD10	MD[21:20]	MD11	MDT[1:0]	JTAG	MMC	SDHI2
0	00	-	--	Boundary scan	Normal function	Normal function
0	01	-	--	Reserved	Reserved	Reserved
0	10	0	--	Coresight (*1)	Normal function	Normal function
0	10	1	00	Coresight (*1)	Reserved	Reserved
0	10	1	01	Coresight (*1)	SH-4AL	Normal function
0	10	1	10	Coresight (*1)	Reserved	Reserved
0	10	1	11	Coresight (*1)	Normal function	SH-4AL
0	11	0	--	SH-4AL	Normal function	Normal function
0	11	1	00	SH-4AL	Coresight (*1)	Normal function
1	00	-	--	Reserved	Reserved	Reserved
1	01	0	--	Reserved	Reserved	Reserved
1	01	1	01	Reserved	Reserved	Reserved
1	10	-	--	Reserved	Reserved	Reserved
1	11	-	--	Reserved	Reserved	Reserved

(*1) “Coresight” is an abbreviation of “Coresight debug port”.

3.1.10 MD[14:13] Pins-Frequency Mode Setting

These pins select the frequency mode. A crystal oscillator (Y2: 20 MHz) is mounted on the Tethys board. Do not change the initial setting at shipment (MD14 = 0, MD13 = 0).

MD14	MD13	EXTAL Frequency	EXTAL Divider	PLL0 Multiplication Ratio	PLL1 Multiplication Ratio	PLL3 Multiplication Ratio
0	0	20 MHz	× 1	×80 VCO = 1600 MHz	×78 VCO = 1560 MHz	×50 VCO = 1000 MHz
0	1	26 MHz	× 1	×60 VCO = 1560 MHz	×60 VCO = 1560 MHz	×56 VCO = 1456 MHz
1	0	Prohibited setting				
1	1	30 MHz	× 1	×52 VCO = 1560 MHz	×52 VCO = 1560 MHz	×50 VCO = 1500 MHz

3.1.11 Initial Values of Mode Setting Pins on Tethys Board

The following table shows the Initial Values of Mode Setting Pins on the Board, and how the individual mode pins are set:

MD Pins	Initial Value	Initial Function	Setting Method
MD0	0	-	Set by a dip switch
MD[3:1]	010	Boot from the QSPI(48.75 MHz/16-Kbyte transfer)	Set by a dip switch
MD4	0	CS0 space size (64 Mbytes)	Set by a dip switch
MD5	1	-	Set by a dip switch
MD[7:6]	01	Cortex-A7 boot	Set by a dip switch
MD8	1	CS0 space data bus width (16 bits)	Set by a dip switch
MD9	1	Crystal resonator is used.	Set by a dip switch
MD10, MD[21:20], MD11, MDT[1:0]	0,10,0,00	JTAG = Coresight SDHI1 and SDHI2 = Normal function	Set by a dip switch
MD[14:13]	00	Input frequency = 20 MHz	Set by a dip switch

3.2 DDR3-SDRAM Interface (DBSC)

3.2.1 Specifications

The Tethys board incorporates two 4-Gbit DDR3-SDRAMs (16-bit bus width) and operates at a maximum speed of DDR3-1000. The Tethys board can support memory size up to 2GB (8-Gbit memory x 2) and the data bus width is 32 bits x1. The DDR3-SDRAMs are allocated to the address space from H'01_0000 0000 to H'01_FFFF FFFF in the R-CarW2H. The address ranges from H'00_40000000 to H'00_BFFF FFFF can be accessed by default as a mirror area of H'01_0000 0000 to H'01_7FFF FFFF.

Table 4 DDR3-SDRAM Interface Specifications

Controller	On-chip external bus controller for DDR3-SDRAM (DBSC) in the R-Car W2H
Product name	MT41K256M16HA-125 AAT:E from Micron DDR3-1600 (x 16 bits, 4 Gbits) x 2 pcs
Power supply voltage	1.50 V
Capacity	H'01_0000 0000 to H'01_FFFF FFFF
Bus width	32-bit data bus
Memory bus frequency(R-Car W2H Spec.)	DDR3-1000

3.2.2 Signal Connections between R-Car W2H and DDR3-SDRAMs

Table 5 Signal Connections between R-Car W2H and DDR3-SDRAMs

R-Car W2H	**DDR3-SDRAM (U3)**	**DDR3-SDRAM (U4)**
	D[31:16]	**D[15:0]**
M0DQ[31:16]	DQ[15:0]	--
M0DQ[15:0]	--	DQ[15:0]
M0A[15:0]	A[15:0]	←
M0BA[2:0]	BA[2:0]	←
M0CK1、M0CK1#	CK、CK#	--
M0CK0、M0CK0#	--	CK、CK#
MCKE1	CKE	--
MCKE0	--	CKE
M0CS1#	CS#	--
M0CS0#	--	CS#
M0WE#	WE#	←
M0RAS#	RAS#A	←
M0CAS#	CAS#	←
M0DQS3、M0DQS3#	UDQS、UDQS#	--
M0DQS2、M0DQS2#	LDQS、LDQS#	--
M0DQS1、M0DQS1#	--	UDQS、UDQS#

M0DQS0、M0DQS0#	--	LDQS、LDQS#
M0DM3、M0DM2	UDM、LDM	--
M0DM1、M0DM0	--	UDM、LDM
M0ODT1	ODT	--
M0ODT0	--	ODT
M0RESET#	RESET#	←

3.2.3 Block Diagram

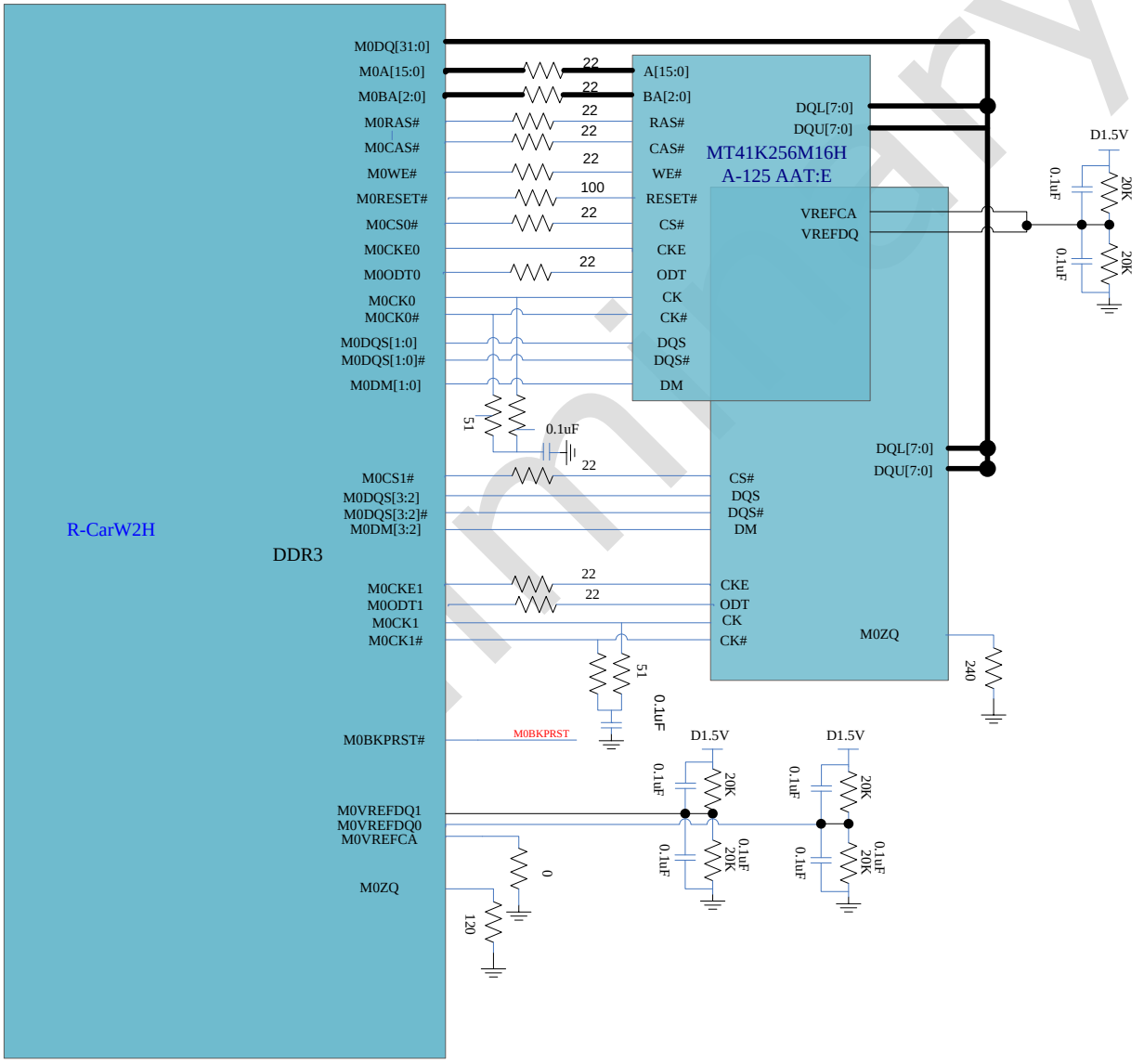


Figure 2 Block Diagram of the DDR3-SDRAM Interface

3.3 SPI-Flash Interface (QSPI)

3.3.1 Specifications

The Tethys board incorporates 512-Mbit and 32-Mbit SPI flash memory devices manufactured by Spansion. These flash memory devices are connected to the QSPI of the R-CarW2H's pin of (GP1_21/QSPI0_SSL/WE1#). And the connection is controlled by SW9 When the 512-Mbit SPI flash memory is to be assessed, set SW9 pin 3 and 6 short, and when the 32-Mbit SPI flash memory is to be accessed, set SW9 pin 4 and 8 short. Do not short them at the same time.

Table 6 SPI-Flash Interface Specifications

Flash memory interfaces	QSPI0 and QSPI1 in the R-Car W2H
QSPI0 devices	U5:S25FL512SAGMFIG11 (512 Mbits, 8-/16-bit data width) from Spansion ×1 pcs U6:S25FL132K0XMFI011(32Mbits, 8-/16-bit data width) from Spansion ×1 pcs
Operating voltage	D3.3 V_FLASH = 3.3V
Capacity	512-Mbit and 32-Mbit
Mapping area (512-Mbit)	0x0000000~0x3ffffff
Mapping area (32-Mbit)	0x0000000~0x3fffff

3.3.2 Block Diagram

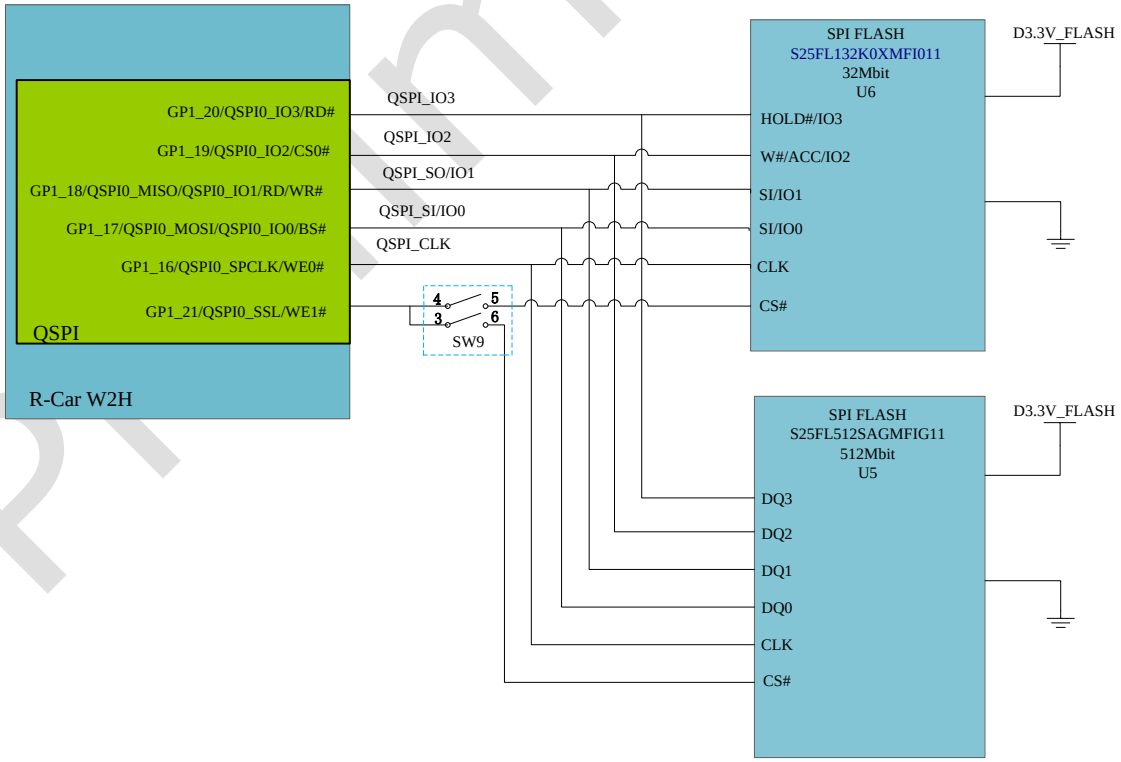


Figure 3 Block Diagram of the SPI-Flash Interface

3.4 Audio Codec Interfaces (SSI0, SSI1)

3.4.1 Specifications

The Tethys board incorporates an audio codec (AK4642EN, U29) which is connected to SSI0 and SSI1 of the R-Car W2H. For details on the SSI, see the R-CarW2H Hardware Manual. For details on the AK4642EN, see the datasheet published by Asahi Kasei Micro devices.

Table 7 SSI Codec Specifications

Controller	On-chip SSI0and SSI1 in the R-CarW2H
Audio codec	AK4642EN (U29) from AKM I2C bus : Interface 1 I2C slave address: 0x25 for read, 0x24 for write (CAD0= 0)
Master/slave mode	AK4642EN: Master/slave selectable(slave mode by default)
Audio connector	MIC IN (J1) LINE-OUT(J1)

3.4.2 Block Diagram

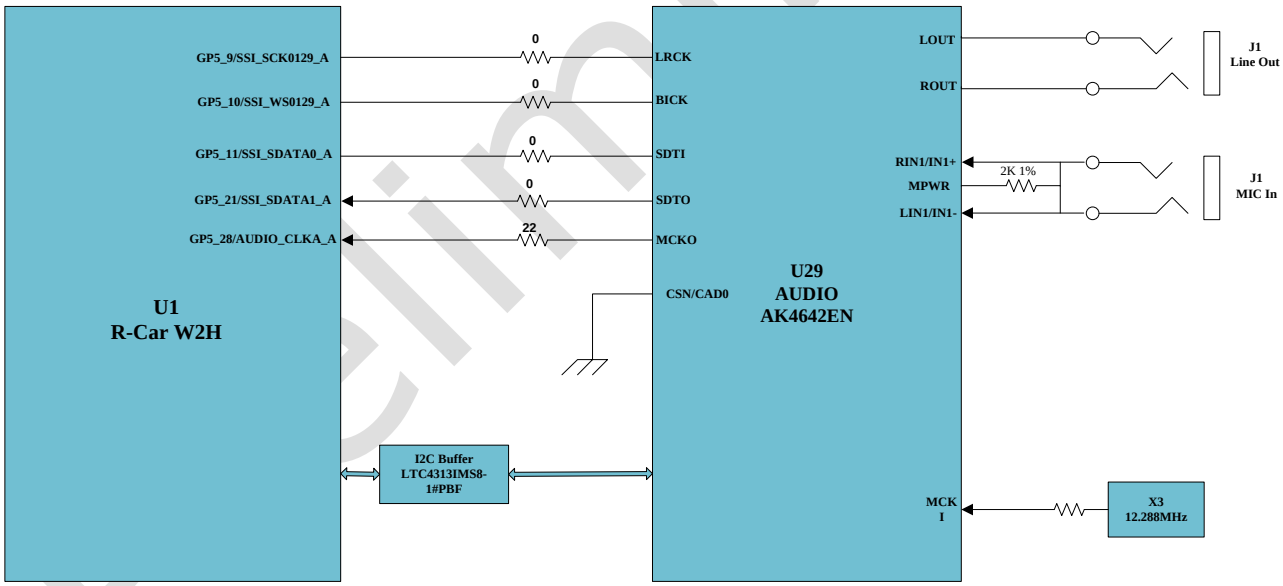


Figure 4 Block Diagram of the Audio Codec Interface

3.5 eMMC Memory Interface (eMMC)

3.5.1 Specifications

The Tethys board incorporates an eMMC memory SDIN8DE1-8G-XA manufactured by SanDisk that is connected to the on-chip MMC interface of the R-CarW2H.For details on the MMC, see the R-CarW2H Hardware Manual.

Table 8 eMMC Memory Interface (eMMC) Specifications

MMC controller	On-chip MMC in the R-Car W2H
Interface voltage control	D3.3V_eMMC=3.3V
eMMC memory	SDIN8DE1-8G-XA(U7) from SanDisk Capacity:8GB

3.5.2 Block Diagram

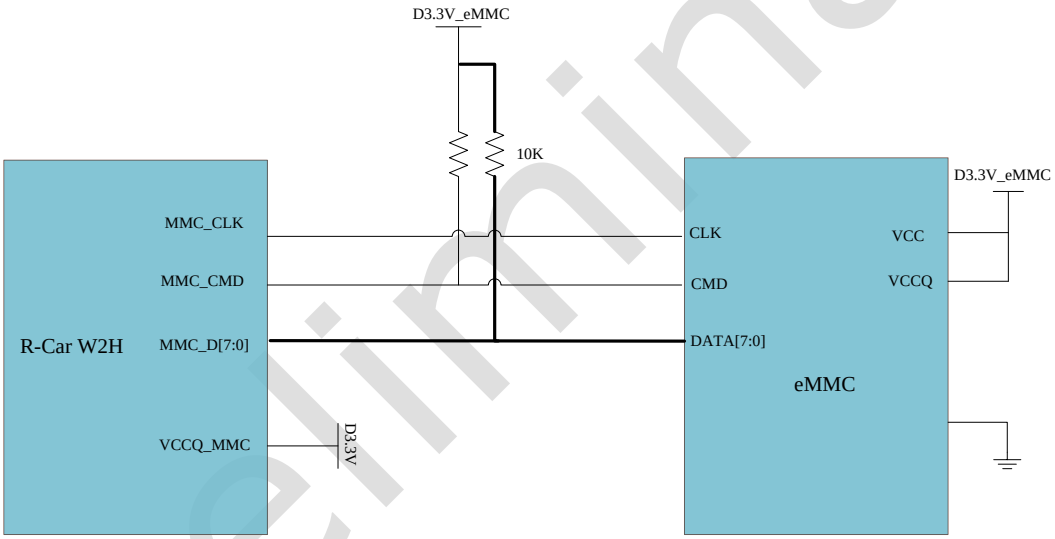


Figure 5 Block Diagram of the eMMC Memory Interface

3.6 SD Card Host Interface (SDHI2)

3.6.1 Specifications

The Tethys board incorporates a SD card slot (CN2) and a mini-PCI Express CN (CN12) for the on-chip SD card host interface (SDHI2) of the R-CarW2H. For details on the SDHI2, please refer to the R-CarW2H hardware manual. CN12 and CN2 can not be used at the same time.

Table 9 Specifications of SD Card Host Interface (SDHI2)

SD Host Interface	On-chip SDHI2 in the R-Car W2H
Voltage control for VDD	VCCQ_SD2 =3.3V/1.8V it can be switched by software , D3.3V=3.3V
SD Card Slot	503182-1852(CN2) from Molex

3.6.2 Block Diagram

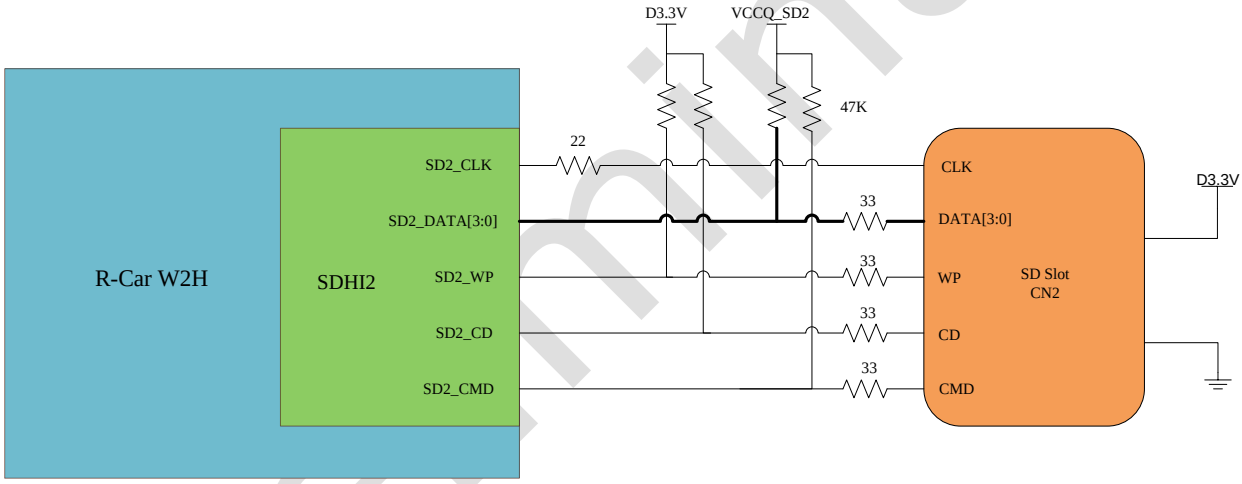


Figure 6 Block Diagram of the SDHI2 Interface

3.7 Mini PCI Express Interface

3.7.1 Specifications

The Tethys board incorporates four mini PCIE interface manufactured by TE. One Mini-PCI Express CN(CN9) is connected to SDHI0, GPIO, SCIF0 and the HSCIF0 of the R-CarW2H, another Mini-PCI Express CN(CN12) is connected to SDHI2, GPIO, SCIF3 and the HSCIF2 of the R-CarW2H, and the third Mini-PCI Express CN(CN8) is connected to the Ether MAC/EtherAVB, GPIO and the HSCIF1 of the R-CarW2H, The fourth Mini-PCI Express CN(CN11) acts as a standard Mini-PCI Express signal connector and transmits the standard Mini-PCI Express signals. There are also USB 2.0 signals and 1pps signal connected to the mini PCIE connectors.

3.7.2 The Mini PCIE connector signal configuration are shown as below:

3.7.2.1 CN9 of figure 7 signal assignments are shown as below:

Pin NO.	Signal	I/O	Remark	Pin NO.	Signal	I/O	Remark
1	C2X0_DCMODE	O	GPIO	2	D3.3V	PO	Power
3	N.C.	-		4	GND	-	Power
5	PCIE_5.0V	PO	Power	6	PCIE_5.0V	PO	Power
7	C2X0_RESETB	O	GPIO	8	GPS_1PPS/ C2X0_GPIO_B3	I/O	GPS 1PPS input or GPIO
9	GND	-	Power	10	C2X0_GPIO_B2	I/O	GPIO
11	RX0_D/ C2X_RXD	I	UART from CPU or USB2UART	12	C2X0_GPIO_B1	I/O	GPIO
13	TX0_D/ C2X_TXD	O	UART from CPU or USB2UART	14	C2X0_GPIO_B0	I/O	GPIO
15	GND	-	Power	16	C2X0_STATE	I	C2X state
17	N.C.	-		18	GND	-	Power
19	N.C.	-		20	C2X0_GPIO_A6	I/O	GPIO
21	GND	-	Power	22	C2X0_GPIO_A5	I/O	GPIO
23	HRX0_B	I	UART from CPU	24	PCIE_5.0V	PO	Power
25	HTX0_B	O	UART from CPU	26	GND	-	Power
27	GND	-	Power	28	PCIE_5.0V	PO	Power
29	GND	-	Power	30	C2X0_GPIO_A4	I/O	GPIO
31	MD10/HCTS0#	I/O	UART from CPU	32	C2X0_GPIO_A3	I/O	GPIO
33	MD11/HRTS0#	I/O	UART from CPU	34	GND	-	Power
35	GND	-	Power	36	N.C	-	
37	SD0_CLK	O	SD0 clock	38	N.C	-	
39	SD0_WP	I	SD0 write protect	40	GND	-	Power
41	SD0_CD	I	SD0 card detect	42	C2X0_GPIO_A2	I/O	GPIO

43	SD0_DATA3	I/O	SD0 data3	44	C2X0_GPIO_A1	I/O	GPIO
45	SD0_DATA2	I/O	SD0 data2	46	C2X0_GPIO_A0	I/O	GPIO
47	SD0_DATA1	I/O	SD0 data1	48	PCIE_5.0V	PO	Power
49	SD0_DATA0	I/O	SD0 data0	50	GND	-	Power
51	SD0_CMD	I/O	SD0 command	52	D3.3V	PO	Power

3.7.2.2 CN12 of figure 7 signal assignments are shown as below:

Pin NO.	Signal	I/O	Remark	Pin NO.	Signal	I/O	Remark
1	C2X1_DCMODE	O	GPIO	2	D3.3V	PO	Power
3	N.C.	-		4	GND	-	Power
5	PCIE_5.0V	PO	Power	6	PCIE_5.0V	PO	Power
7	C2X1_RESETB	O	GPIO	8	GPS_1PPS/ C2X1_GPIO_B3	I/O	GPS 1PPS input or GPIO
9	GND	-	Power	10	C2X1_GPIO_B2	I/O	GPIO
11	RX3_B	I	UART from CPU	12	C2X1_GPIO_B1	I/O	GPIO
13	TX3_B	O	UART from CPU	14	C2X1_GPIO_B0	I/O	GPIO
15	GND	-	Power	16	C2X1_STATE	I	C2X state
17	N.C.	-		18	GND	-	Power
19	N.C.	-		20	C2X1_GPIO_A6	I/O	GPIO
21	GND	-	Power	22	C2X1_GPIO_A5	I/O	GPIO
23	HRX2	I	UART from CPU	24	PCIE_5.0V	PO	Power
25	HTX2	O	UART from CPU	26	GND	-	Power
27	GND	-	Power	28	PCIE_5.0V	PO	Power
29	GND	-	Power	30	C2X1_GPIO_A4	I/O	GPIO
31	HCTS2#	I/O	UART from CPU	32	C2X1_GPIO_A3	I/O	GPIO
33	HRTS2#	I/O	UART from CPU	34	GND	-	Power
35	GND	-	Power	36	USB1_DM3	I/O	USB data negative
37	SD2_CLK	O	SD0 clock	38	USB1_DP3	I/O	USB data positive
39	SD2_WP	I	SD0 write protect	40	GND	-	Power
41	SD2_CD	I	SD0 card detect	42	C2X1_GPIO_A2	I/O	GPIO
43	SD2_DATA3	I/O	SD0 data3	44	C2X1_GPIO_A1	I/O	GPIO
45	SD2_DATA2	I/O	SD0 data2	46	C2X1_GPIO_A0	I/O	GPIO
47	SD2_DATA1	I/O	SD0 data1	48	PCIE_5.0V	PO	Power
49	SD2_DATA0	I/O	SD0 data0	50	GND	-	Power
51	SD2_CMD	I/O	SD0 command	52	D3.3V	PO	Power

3.7.2.3 CN8 of Figure 7 signal assignments are shown as below:

Pin NO.	Signal	I/O	Remark	Pin NO.	Signal	I/O	Remark
1	AVB_TX_ER	O	Transmit error signal	2	D3.3V	PO	Power
3	AVB_MDIO	I/O	Management information transmit/receive data	4	GND	-	Power
5	PCIE_5.0V	PO	Power	6	PCIE_5.0V	PO	Power
7	AVB_GPIO6 (AVB_CRS)	I/O	GPIO	8	ETH_CRS_DV/ AVB_RX_DV	I	Receive data enable signal
9	GND	-	Power	10	ETH_RX_ER/ AVB_RXD3	I	Receive data signal
11	AVB_PHY_INT	I	PHY interrupt signal	12	ETH_TXD0/ AVB_RX_ER	I	Reception error signal
13	AVB_MDC	O	Management information transfer clock signal	14	ETH_RXD1/ AVB_RXD1	I	Receive data signal
15	GND	-	Power	16	ETH_MDIO/ AVB_RXD2	I	Receive data signal
17	AVB_TX_CLK	I	Transmit clock signal	18	GND	-	Power
19	C2X1_RESETB/ AVB_GTX_CLK	O	GMII transmit clock signal	20	ETH_REF_CLK/ AVB_RX_CLK	I	Receive clock signal
21	GND	-	Power	22	AVB_RESETn	O	GPIO
23	HRX1_A	I	High speed uart	24	PCIE_5.0V	PO	Power
25	HTX1_A	O	High speed uart	26	GND	-	Power
27	C2X1_GPIO_A1/ AVB_TXD7	O	Transmit data signal	28	PCIE_5.0V	PO	Power
29	C2X1_GPIO_B0/ AVB_TXD6	O	Transmit data signal	30	GTXREFCLK	O	GMII reference clock signal
31	HCTS1#_A	I/O	High speed uart	32	ETH_RXD0/ AVB_RXD0	I	Receive data signal
33	HRTS1#_A	I/O	High speed uart	34	GND	-	Power
35	C2X1_GPIO_B1/ AVB_TXD5	O	Receive data signal	36	USB1_DM2	I/O	USB data negative
37	AVB_TXD3	O	Transmit data signal	38	USB1_DP2	I/O	USB data positive
39	AVB_TXD0	O	Transmit data signal	40	GND	-	Power
41	AVB_TXD1	O	Transmit data signal	42	AVB_GPIO5 (AVB_RXD7)	I/O	GPIO
43	AVB_TXD2	O	Transmit data signal	44	ETH_TX_EN/ AVB_GPIO3	I/O	GPIO

					(AVB_RXD6)		
45	C2X1_GPIO_B2/ AVB_TXD4	O	Transmit data signal	46	AVB_GPIO4 (AVB_COL)	I/O	GPIO
47	ETH_LINK/ AVB_GPIO1 (AVB_RXD4)	I/O	GPIO	48	PCIE_5.0V	PO	Power
49	ETH_TXD1/ AVB_GPIO2 (AVB_RXD5)	I/O	GPIO	50	GND	-	Power
51	AVB_TX_EN	O	GPIO	52	D3.3V	PO	Power

3.7.2.4 CN11 of figure 7 signal assignments are shown as below:

Pin NO.	Signal	I/O	Remark	Pin NO.	Signal	I/O	Remark
1	N.C	-		2	D3.3V	PO	Power
3	N.C	-		4	GND	-	Power
5	N.C	-		6	D1.5V	PO	Power
7	N.C	-		8	N.C	-	
9	GND	-	Power	10	N.C	-	
11	PCIe_CLKN	I	PCIe clock minus	12	N.C	-	
13	PCIe_CLKP	I	PCIe clock plus	14	N.C	-	
15	GND	-	Power	16	N.C	-	
17	N.C	-		18	GND	-	Power
19	N.C	-		20	N.C	-	
21	GND	-	Power	22	N.C	-	
23	PCIe_RXN	I	PCIe receive data minus	24	D3.3V	PO	Power
25	PCIe_RXP	I	PCIe receive data plus	26	GND	-	Power
27	GND	-	Power	28	D1.5V	PO	Power
29	GND	-	Power	30	I2C1-SCL	I/O	I2C clock
31	PCIe_TXN	O	PCIe transmit data minus	32	I2C1-SDA	I/O	I2C data
33	PCIe_TXP	O	PCIe transmit data plus	34	GND	-	Power
35	GND	-	Power	36	USB1_DM4	I/O	USB data negative
37	N.C	-		38	USB1_DP4	I/O	USB data positive
39	N.C	-		40	GND	-	Power
41	N.C	-		42	N.C	-	
43	N.C	-		44	N.C	-	
45	N.C	-		46	N.C	-	
47	N.C	-		48	D1.5V	PO	Power
49	N.C	-		50	GND	-	Power

51	N.C	-		52	D3.3V	PO	Power

3.7.3 Block Diagram

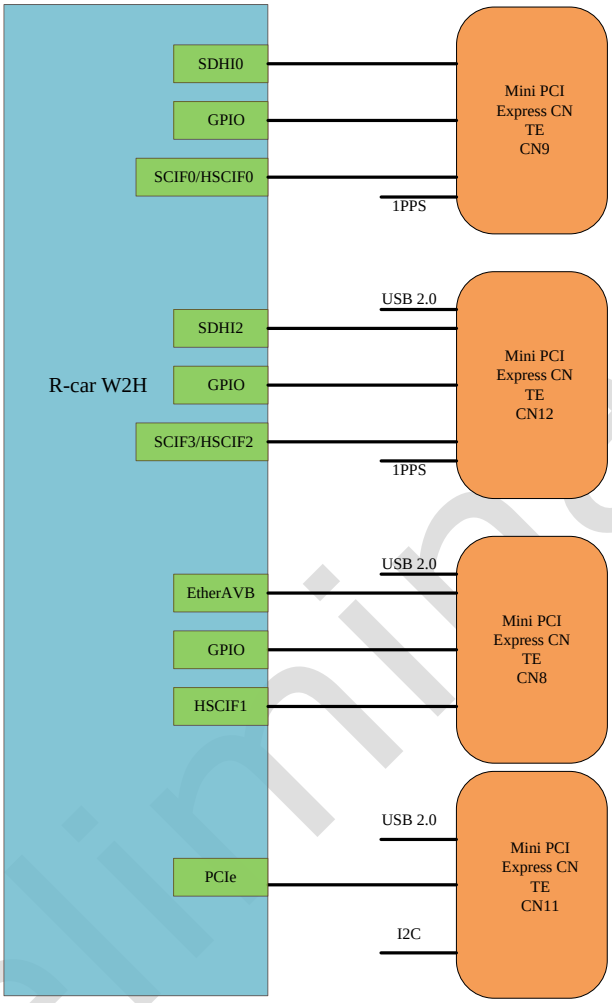


Figure 7 Block Diagram of Mini PCI Express Interface

3.8 USB to UART

3.8.1 Specifications

The Tethys board incorporates three USB to UART bridges: One is connected to a mini PCIE connector, one is connected to the R-CarW2H and another is connected to the MCU. Users can control and debug the Tethys board through the USB port.

Table 10 USB to UART Specifications

USB controller	On-chip SCIF2(debug) function controller in the R-Car W2H, MCU，and Mini PCI express CN
USB to UART IC	CP2102-GM from Silicon
USB function connector	47346-0001 from Molex x 3pcs
Common mode filter with ESD protection diode	PRTR5V0U2X from NXP x 3pcs

3.8.2 Block Diagram

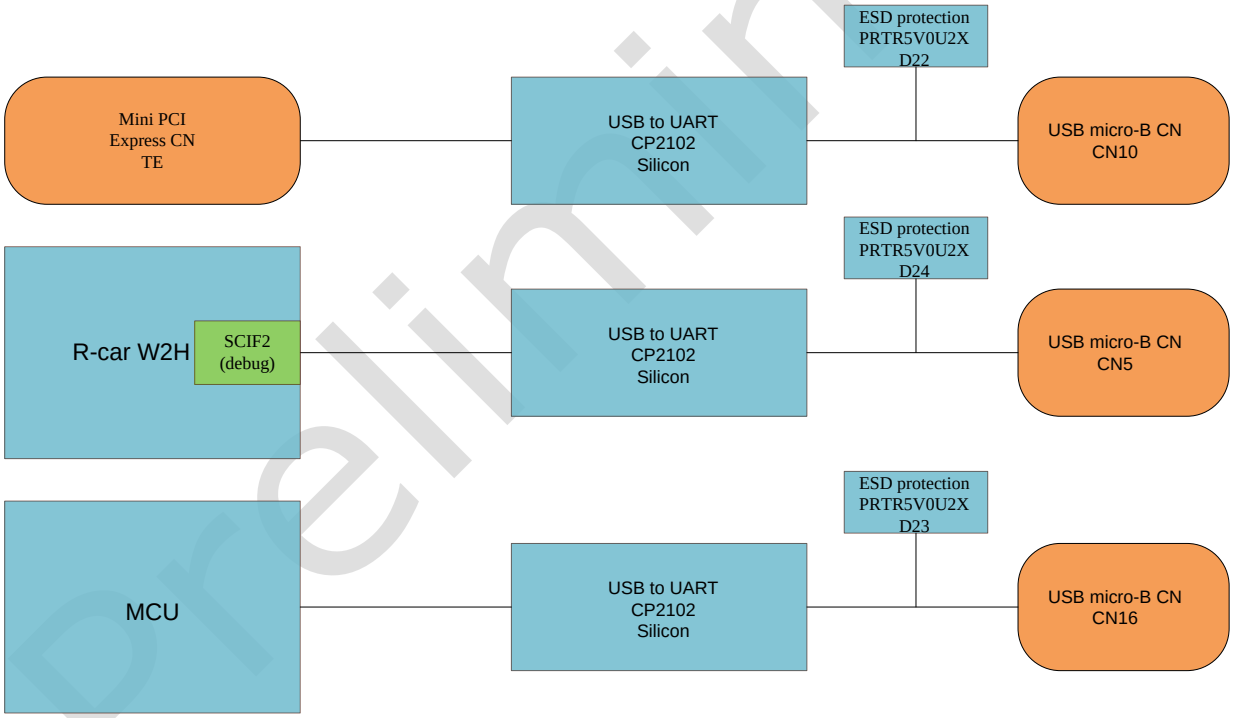


Figure 8 Block Diagram of the USB to UART

3.9 USB2.0 Interface

3.9.1 Specifications

The Tethys board incorporates two A Type USB Connectors for the USB2.0 host interface. The USB0 of the R-CarW2H is connected to a USB 2.0 type A port directly. The USB1 of the R-CarW2H is connected to the GL852GT which manufactured by Genesys to expand 4 USB 2.0. The expand 1 port of the GL852GT is connected to a USB 2.0 type A port. There is a switch IC for the two USB ports' power supply. The other 3 USB port of the GL650USB are connected to the three of four mini PCIE connectors separately.

Table 11 USB2.0 Interface

USB controller	On-chip USB2.0 function controller in the R-Car W2H
USB Power Switch	BD2066FJ-LBE2 from ROHM
USB host connector x 2	On-chip USB2.0 interface1 in the R-Car W2H 1759546-1 from TE x 2
USB Hub	GL852GT-MNGXX from Genesys
Common mode filter with ESD protection diode	PRTR5V0U2X from NXP

3.9.2 Block Diagram

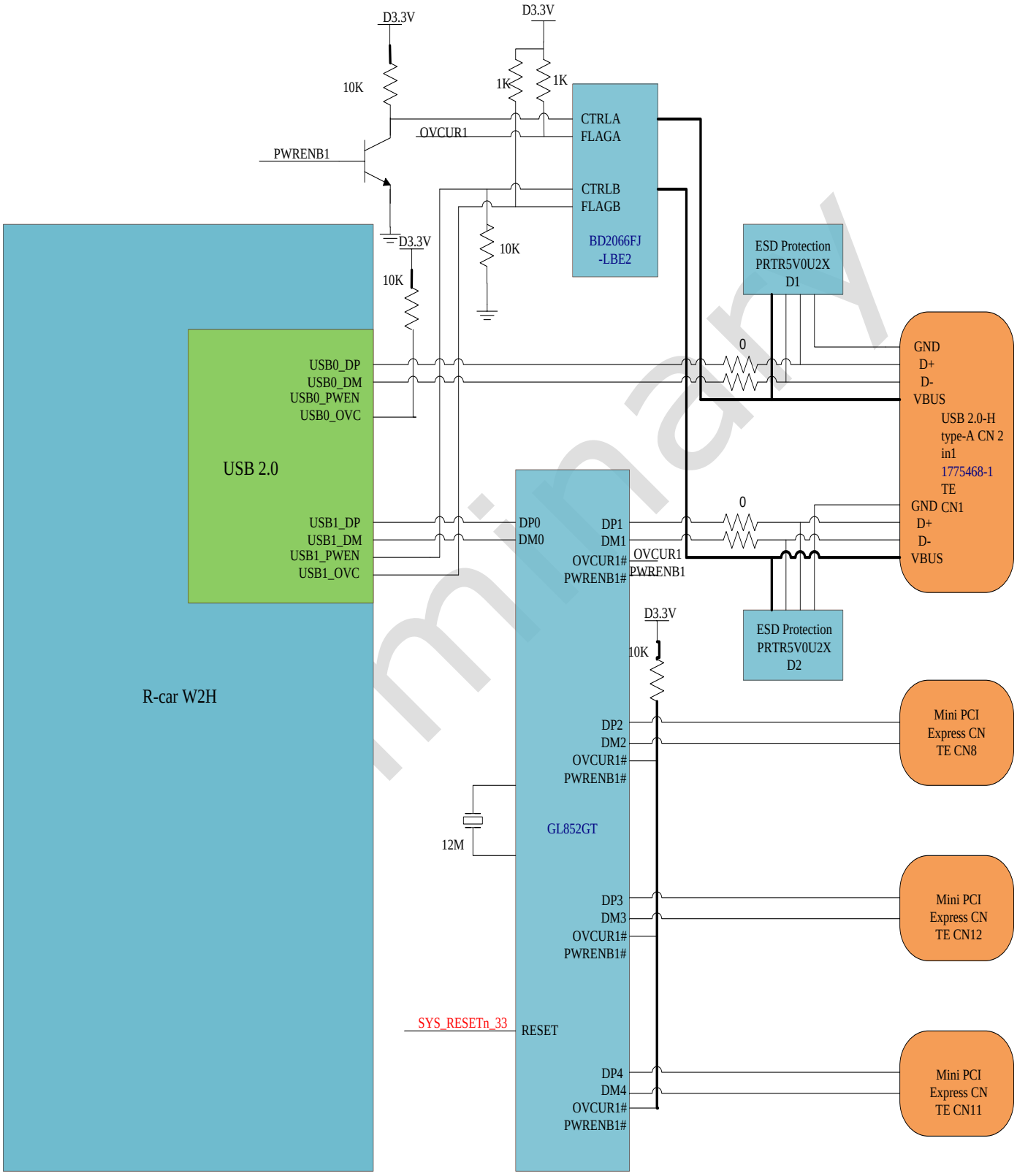


Figure 9 Block Diagram of the USB2.0 Interface

3.10 Debug Interface

The JTAG connector can be found in the debug sub board including CPU Debug connector,JTAG debug connector and MCU JTAG connector through 26 pin FPC (CN4) connector.

3.10.1 CPU debug

3.10.1.1 Specifications

The R-CarW2H incorporates three debugger interfaces: one is a 26-pin connector (DBG) incorporates ARM core and Real-time processing core for connection to the JTAG emulator, one USB-B connector and the third EtherMAC for connection to the host PC.

The SW3 and SW12 switch 2-3 short is for normal operation and 2-1 short for CPU JTAG Debug.

On the Tethys board, the SCIF2 of the R-CarW2H are used as debug serial interfaces by connecting the USB-B connector to the host PC through a USB cable. The SCIF2 of the R-CarW2H is connected to the USB-B connector via the USB to UART Bridge CP2102. The R-CarW2H incorporates the EtherMAC that supports 100Base-T or 10Base-T compliant with IEEE 802.3u. On the Tethys board, the EtherMAC signals are connected to the RMII PHY interface (KSZ8041RNLI) manufactured by Micrel.

Table 12 CPU debug Specifications

Control Interface	CPU JTAG Debug.
Debug Interface	CN4: IMSA-9632S-26Y801 from IRISO
operating conditions	SW3 and SW12 switch 2-1 short

3.10.1.2 Block Diagram

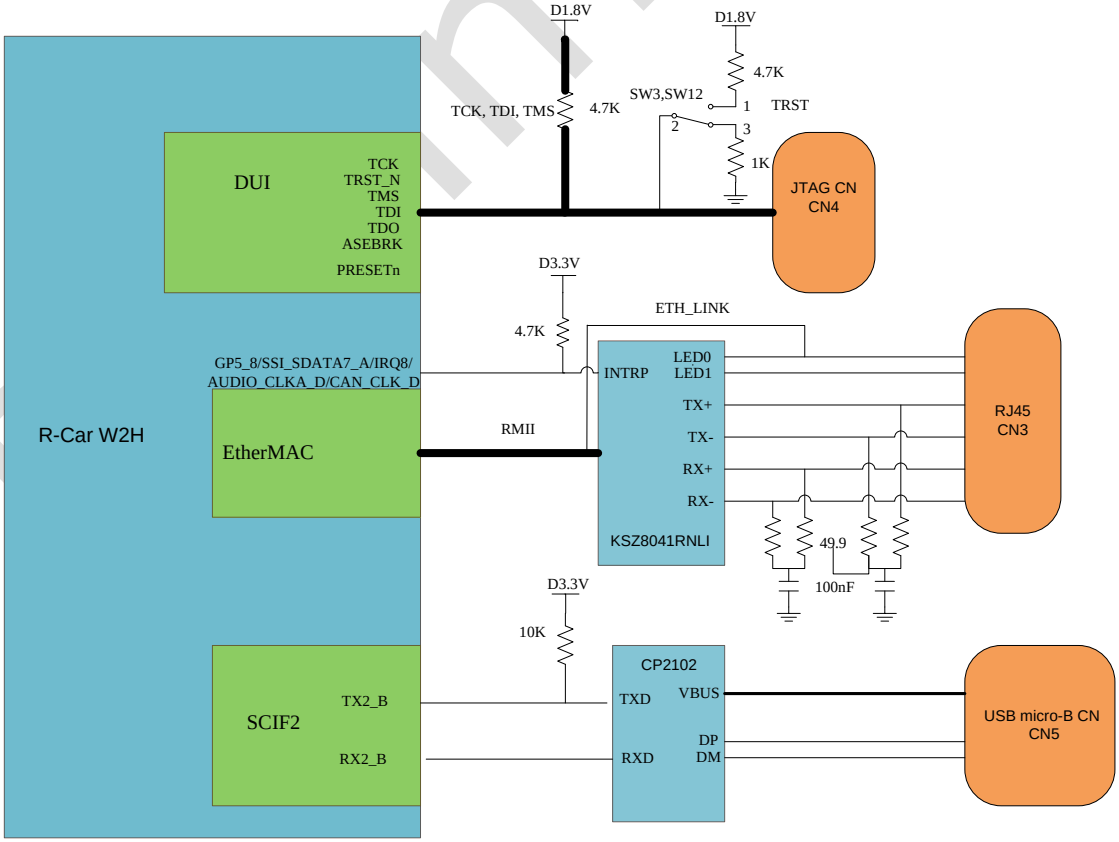


Figure 10 Block Diagram of the CPU debug

3.10.2 CPU JTAG2 debug

3.10.2.1 Specification

On the Tethys board, the R-CarW2H has the CPU JTAG2 debug interface. The SW12 switch 2-3 short is for normal operation and 2-1 short for CPU JTAG2 debug

Table 13 CPU JTAG2 debug

Control Interface	CPU JTAG2
Debug Interface	CN4: IMSA-9632S-26Y801 from IRISO
operating conditions	The SW12 switch 2-1 short The SW1 switch 9-8 short, switch 10-7 short The SW2 switch 8-1 short, switch 7-2 short, switch 6-3 short, switch 5-4 short

3.10.2.2 Block Diagram

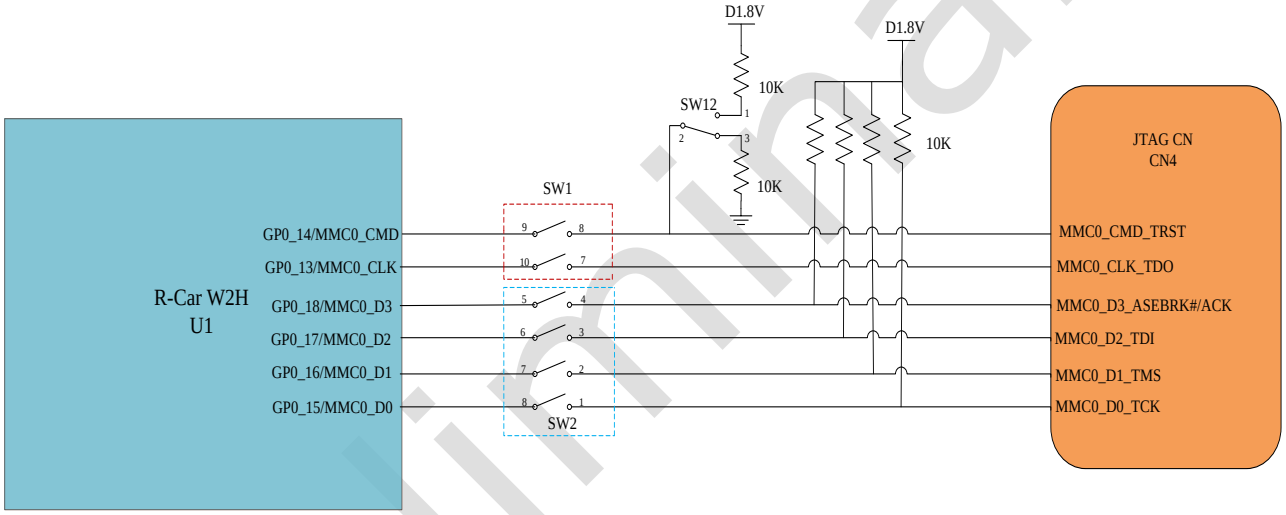


Figure 11 Block Diagram of the CPU JTAG2 (SH-4AL) debug

3.10.3 MCU debug

3.10.3.1 Specifications

On the Tethys board, the RH850 F1H / F1L has the JTAG interface and provides the serial programming function. The serial programming function is used to test the connection between the devices mounted on the printed-circuit board. The SW17 switch 2-3 short is for normal operation and 2-1 short for MCU Debug.

Table 14 MCU debug Specification

Control Interface	MCU Debug
Debug Interface	CN4: IMSA-9632S-26Y801 from IRISO
operating conditions	The SW17 switch 2-1 short for MCU Debug

3.10.3.2 Block Diagram

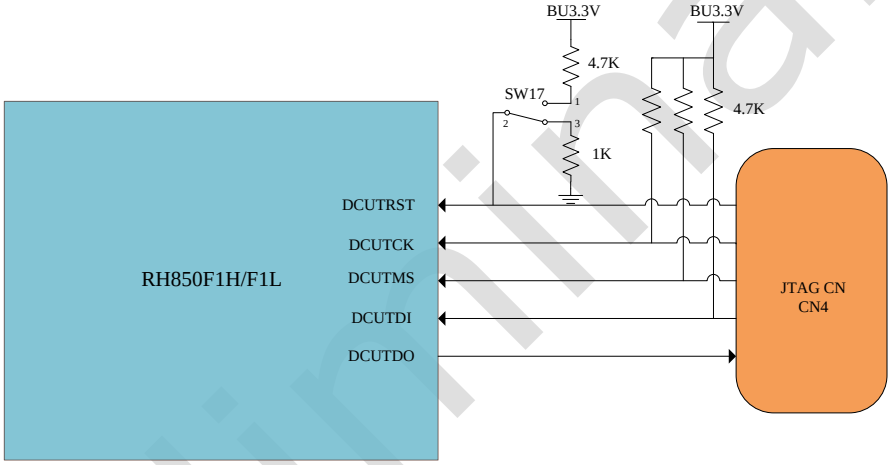


Figure 12 Block Diagram of the MCU debug

3.11 GYRO/G-SENSOR

3.11.1 Specifications

The A3G4250D manufactured by ST is a low-power 3-axis angular rate sensor able to provide unprecedented stability at zero rate level and sensitivity over temperature and time. The AIS328DQ is an ultra low-power high performance 3-axis linear accelerometer. The CPU communicates with the A3G4250D and AIS328DQ through its I2C1 and GPIOs.

Table 15 GYRO/G-SENSOR Specifications

Controller	R-car W2H
Control Interface	The A3G4250D and AIS328DQ from ST
Supply voltage	D3.3V=3.3V

3.11.2 Block Diagram

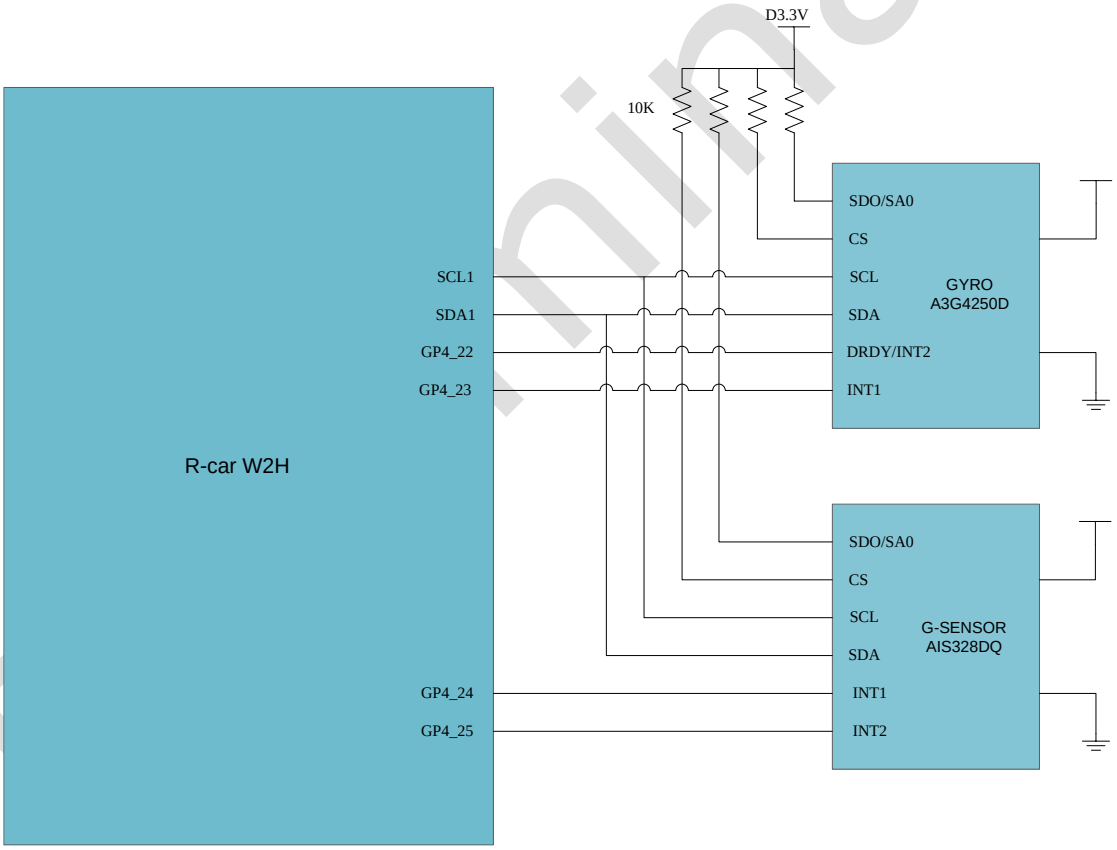


Figure 13 Block Diagram of the GYRO/G-SENSOR

3.12 I2C Interfaces

3.12.1 Specifications

The R-Car W2H incorporates five I2C interfaces (3.3 V). Since the R-Car W2H uses LVTTL-type I/O buffers on I2C interfaces, it cannot directly drive an I2C bus with a relatively high load capacitance (e.g. 100 pF).

While the above restriction applies to interfaces of the R-Car W2H, the design of the Tethys board calls for multiple I2C devices being connected to I2C interfaces 1. In order to compensate for the driving ability of the R-Car W2H, the Tethys board incorporates an LTC4313IMS8-1#PBF I2C buffer manufactured by Linear Technology, through which each I2C device is connected to the I2C interface for the device.

The following devices are connected to each I2C interface on the Tethys board.

Table 16 List of I2C Devices

I2C Controller	On-chip I2C controllers in the R-CarW2H
I2C devices through I2C interface 1	Through LTC4313IMS8-1#PBF (U2) from Linear Technology U17: 24LC64EST from Microchip U28: A3G4250D from ST U29: AK4642EN from AKM U30: AIS328DQ from ST U32: RH850F1H/F1L from Renesas CN11: 1759546-1 from TE for PCIE Express CN14: HTST-103-04-S-D-RA from Samtec for HSM

3.12.2 List of Slave Addresses

The table below lists the slave addresses of the I2C devices on the Tethys board

Table 17 List of I2C Slave Addresses

I2C Interfaces	Ux/CNx	Device		Slave Addresses										Note
				Binary								Hexadecimal		
				SA7	SA6	SA5	SA4	SA3	SA2	SA1	R/W#	RD	WR	
1	U17	24LC64EST	I2C EEPROM for MAC address	1	0	1	0	0	0	0	x	0xA1	0xA0	*1
	U28	A3G4250D	GYRO	1	1	0	1	0	1	1	x	0xD7	0xD6	*2
	U29	AK4642EN	AUDIO	0	0	1	0	0	1	0	x	0x25	0x24	*3
	U30	AIS328DQ	G-SENSOR	0	0	1	1	0	0	1	x	0x33	0x32	*4
	U32	RH850F1H/F1L	MCU	--	--	--	--	--	--	--	--	--	--	*5
	CN11	Mini PCIE	Connector	--	--	--	--	--	--	--	--	--	--	
	CN14	HSM CN	Connector	--	--	--	--	--	--	--	--	--	--	-

Note:

*1 Pins 3 to 1 (A [2:0]) = GND

*2 Pin 8 to 12 (RESERVED [5:1]) = GND

*3 Pin 8 (CSN/CAD0) = GND

*4 Pin 25(EP) and Pin 4 (RESERVED1) = GND

*5 I2C no use

3.12.3 Block Diagram

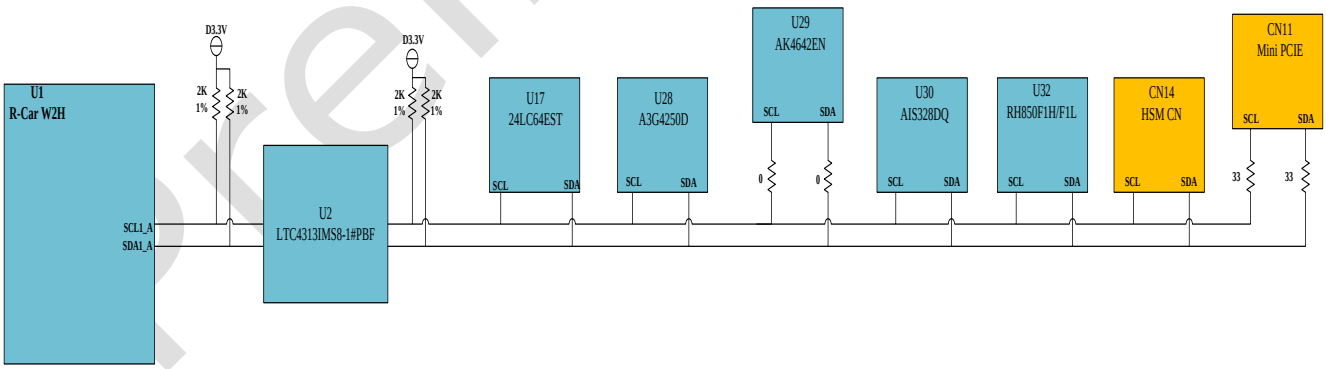


Figure 14 Block Diagram of the I2C Interfaces

3.13 GPS Module

3.13.1 Specifications

The NEO-7P /7M/M8L manufactured by UBLOX is a high performance GPS module. It has high performance active antenna. It communicates with the CPU through the SCIF5 interface.

3.13.2 Block Diagram

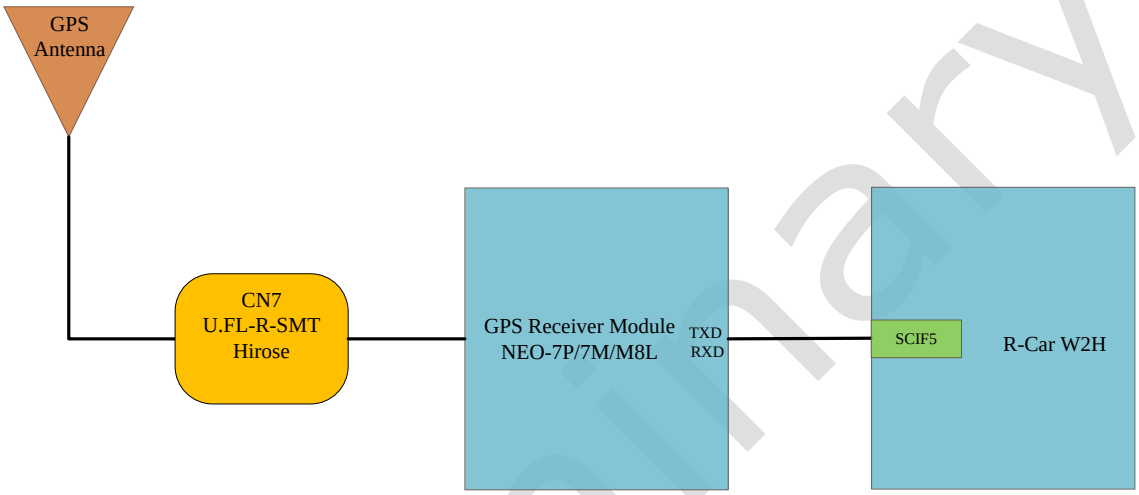


Figure 15 Block Diagram of the GPS module

3.14 CAN and Flexray Interface

3.14.1 Specifications

On the Tethys board, there are three CAN bus, one is connected to the R-CarW2H, and another two are connected to the MCU. The high speed CAN driver TJA1050 manufactured by NXP is used for the two CAN bus.

On the Tethys board, there are one Flexray bus connected to the MCU. The high speed Flexray driver TJA1082 manufactured by NXP is used for the Flexray bus.

Table 18 CAN and Flexray Interface Specifications

Controller	R-Car W2H and RH850F1H/F1L， if mounting RH850F1L, not Flexray function
Control Interface	CN6: HTST-105-04-S-D-RA from Samtec
CAN Transceiver Interface	TJA1050 from NXP
Flexray Transceiver Interface	TJA1082 from NXP

3.14.2 Block Diagram

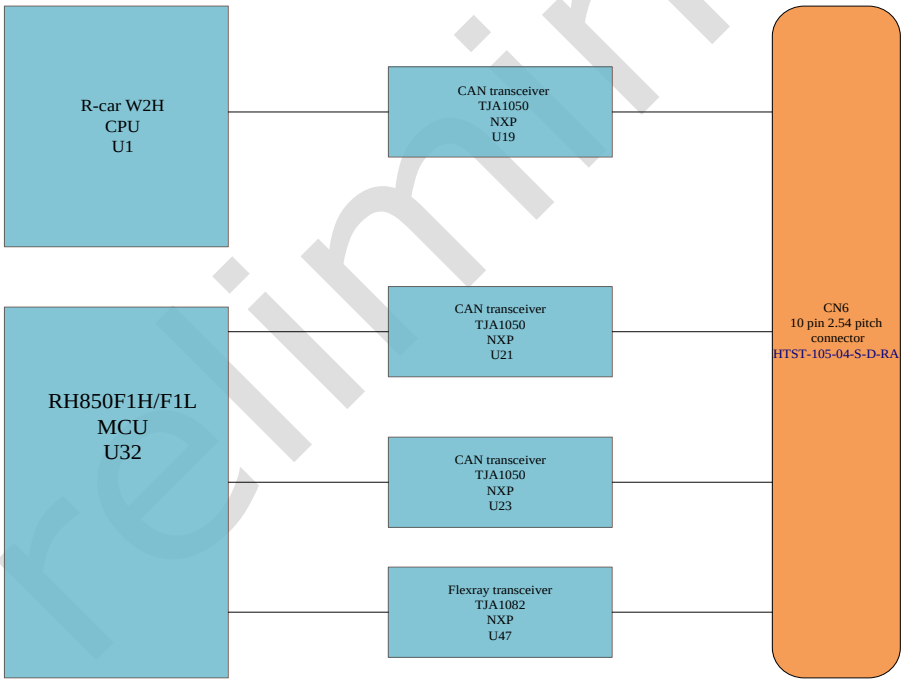


Figure 16 Block Diagram of the CAN and Flexray Interface

The 10 pin connector (CN6) pin assignment is shown as below:

CN6 PIN Number	Signal	Remark
1	CPU_CAN0_H	HIGH-level CAN bus line
2	CPU_CAN0_L	LOW-level CAN bus line
3	MCU_CAN0_H	HIGH-level CAN bus line
4	MCU_CAN0_L	LOW-level CAN bus line
5	MCU_CAN1_H	HIGH-level CAN bus line
6	MCU_CAN1_L	LOW-level CAN bus line
7	BP	Flexray bus line plus
8	BM	Flexray bus line minus
9	GND	Ground
10	GND	Ground

3.15 LEDs and Switches

3.15.1 Specifications

The Tethys board incorporates four bits of tactile switches, and four bits of LEDs (eight LEDS for 4 GPIO place both top and bottom side of the PCB) for debugging and status indication. They are connected to the GPIO pins of the R-CarW2H. Besides, there are two LEDS control by the GPS 1PPS signal to indicate the GPS work status. The LED controlled by R-CarW2H port and GPS 1PPS signal correspondingly is shown as the table below,

LED	R-CarW2H **PORT**	Color
D3&D4	GP5_4	Green
D5&D6	GP5_5	Green
D7&D8	GP5_6	Green
D9&D10	GP5_7	Green

LED	Signal	Color
D11&D12	GPS_1PPS	Green

The tactile switch controlled by R-CarW2H or MCU port correspondingly is shown as the table below,

Tact SW	R-CarW2H or MCU PORT
SW13	GP5_0
SW14	GP5_1
SW15	GP5_2
SW16	GP5_3
SW4	MCU reset

There are other Switches are listed as below:

Table 19 DIP Switches default setting is as below table

DIP Switch	**Description**	**Function**		Default setting	
				ON(Short)	**OFF(Open)**
SW1	eMMC interface and RL JTAG Select switch	eMMC	JTAG		
		SW1: 1-16 short	SW1: 1-16 open	○	
		SW1: 2-15 short	SW1: 2-15 open	○	
		SW1: 3-14 short	SW1: 3-14 open	○	
		SW1: 4-13 short	SW1: 4-13 open	○	
		SW1: 5-12 short	SW1: 5-12 open	○	
		SW1: 6-11 short	SW1: 6-11 open	○	
		SW1: 7-10 open	SW1: 7-10 short		○
		SW1: 8-9 open	SW1: 8-9 short		○

SW2	MMC interface and RL JTAG Select switch	JTAG		eMMC		
		SW2: 1-8 short		SW2: 1-8 open		○
		SW2: 2-7 short		SW2: 2-7 open		○
		SW2: 3-6 short		SW2: 3-6 open		○
		SW2: 4-5 short		SW2: 4-5 open		○
SW5	Mode select switch		Mode=0	Mode=1		
		MD0	SW5: 1-16 short	SW5: 1-16 open	○	
		MD1	SW5: 2-15 short	SW5: 2-15 open	○	
		MD2	SW5: 3-14 short	SW5: 3-14 open		○
		MD3	SW5: 4-13 short	SW5: 4-13 open	○	
		MD4	SW5: 5-12 short	SW5: 5-12 open	○	
		MD5	SW5: 6-11 short	SW5: 6-11 open		○
		MD6	SW5: 7-10 short	SW5: 7-10 open		○
		MD7	SW5: 8-9 short	SW5: 8-9 open	○	
SW6	Mode select switch		Mode=0	Mode=1		
		MD8	SW6: 1-16 short	SW6: 1-16 open		○
		MD9	SW6: 2-15 short	SW6: 2-15 open		○
		MD10	SW6: 3-14 short	SW6: 3-14 open	○	
		MD11	SW6: 4-13 short	SW6: 4-13 open	○	
		MD13	SW6: 5-12 short	SW6: 5-12 open	○	
		MD14	SW6: 6-11 short	SW6: 6-11 open	○	
		MD20	SW6: 7-10 short	SW6: 7-10 open	○	
		MD21	SW6: 8-9 short	SW6: 8-9 open		○
SW7	Mode select switch		Mode=0	Mode=1		
		MDT0	SW7: 1-4 short	SW7: 1-4 open	○	
		MDT1	SW7: 2-3 short	SW7: 2-3 open	○	
SW8	EtherMAC and EtherAVB Selected switch	EtherMAC		Ether/EtherAVB:		
		SW8: 1-8 short		SW8: 1-8 open	○	
		SW8: 2-7 short		SW8: 2-7 open	○	
		SW8: 3-6 short		SW8: 3-6 open	○	
		SW8: 4-5 short		SW8: 4-5 open	○	
SW9	1.EtherMAC and EtherAVB Selected switch 2.512Mbit or 32Mbit SPI FLASH Selected	EtherMAC		Ether/EtherAVB		
		SW9: 1-8 short		SW9: 1-8 open	○	
		SW9: 2-7 short		SW9: 2-7 open	○	
		SW9: 3-6 short		SW9: 3-6 open	○	
		SW9: 4-5 short		SW9: 4-5 open		○
		QSPI0(512Mbit) Default		QSPI1 (32Mbit)		

	switch	SW9 : 3-6 short	SW9 : 3-6 open	○	
		SW9 : 4-5 open	SW9 : 4-5 short		○
SW10	EtherMAC and EtherAVB Selected switch	Ether/EtherAVB	EtherMAC		
		SW10: 1-8 open	SW10: 1-8 short	○	
		SW10: 2-7 open	SW10: 2-7 short	○	
		SW10: 3-6 open	SW10: 3-6 short	○	
		SW10: 4-5 open	SW10: 4-5 short	○	
SW11	EtherMAC and EtherAVB Selected switch	Ether/EtherAVB	EtherMAC		
		SW11: 1-4 open	SW11: 1-4 short	○	
		SW11: 2-3 not use	SW11: 2-3 not use		○

Table 20 Slide Switches default setting is as below table:

Slide Switch	Description	Function		Default setting	
				ON(Short)	OFF(Open)
SW3	JTAG Debug/Normal Operation select switch	JTAG Debug	Normal operation		
		SW3: 1-2 short	SW3: 1-2 open		○
		SW3: 2-3 open	SW3: 2-3 short	○	
SW12	JTAG Debug/Normal Operation select switch	JTAG2 Debug	Normal operation		
		SW12: 1-2 short	SW12: 1-2 open		○
		SW12: 2-3 open	SW12: 2-3 short	○	
SW17	JTAG Debug/Normal Operation select switch	MCU JTAG Debug	Normal operation		
		SW17: 1-2 short	SW17: 1-2 open		○
		SW17: 2-3 open	SW17: 2-3 short	○	
SW18	Power switch	System power			
		ON	OFF		
		SW18: 2-3 short	SW18: 2-3 open		○
		SW18: 1-2 open	SW18: 1-2 short	○	

3.16 Connection between CPU and MCU

3.16.1 Specifications

The Tethys board have a MCU to control the Power sequence and Reset sequence. The power sequence and reset sequence are shown as Figure 23 and Figure 21 respectively in the next chapter.

The Tethys and MCU connection include MSIOF0 and I2C1 and RESET signal. The corresponding signals are shown as below:

HSCIF2 connection:

Rcar-W2H Signal	MCU signal
MSIOF0_RXD_A	P11_9/CSIG1SO/RLIN35RX/INTP15/PWGA49O/TAUB1I13/TAUB1O13/MEMC0CS1
MSIOF0_SCK_A	P11_10/CSIG1SC/PWGA50O/TAUB1I15/TAUB1O15/MEMC0CS2/ETNB0COL
MSIOF0_TXD_A	P11_11/CSIG1SI/RLIN25TX/PWGA51O/TAUB1I0/TAUB1O0/MEMC0CS3/ETNB0RXDV

I2C connection:

Rcar-W2H Signal	MCU signal
I2C1-SDA	P0_11/RIIC0SDA/DPIN12/CSIH1CSS2/TAUB0I8/TAUB0O8/RLIN26RX/PWGA34O
I2C1-SCL	P0_12/RIIC0SCL/DPIN13/PWGA45O/TAUB0I10/TAUB0O10/CSIG0SI/RLIN26TX

The CPU reset signal is controlled by MCU GPIO. That is P1_0/RLIN33RX/INTP13.

3.16.2 Block Diagram

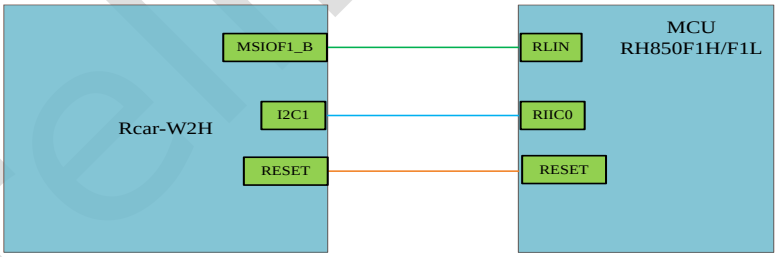


Figure 17 Block Diagram of the Connection between CPU and MCU

3.17 Clock system

The Tethys board uses the crystal oscillators and resonators shown below.

3.17.1 Clock Signals Supplied to the R-Car W2H

Table 21 List of Clock Signals and Crystals for the R-Car W2H

NO.	Xn	Supply voltage	R-car W2H pin name	Frequency	Description	Part number	Manufacturer	Type
1	X1	3.3V	GP1_22/EX_WAIT0/CAN_CLK_B/SCIF_CLK_A	14.7456MHz	SCIF clock	SG-8003CE14.745600MHzPCL	Epson	Oscillator
2	X2	3.3V	GP3_11/RX0_B/SCL0_C/AVB_GTXREFCLK/ETH_MDC	125.00MHz	AVB_GTXREFCLK	SG-8003CE125.000000MHzPCL	Epson	Oscillator
3	Y1		USB_XTAL , USB_EXTAL	48MHz	USB clock	FA-238A48.000MHz10	Epson	Crystal
4	Y2	-	XTAL , EXTAL	20.00MHz	CPU main clock	FA-238A20.000000MHz10	Epson	Crystal

3.17.2 Differential Clock Signals Supplied to the R-Car W2H

Table 22 List of Differential Clock Signals Supplied to the R-Car W2H

NO.	R-Car W2H Pin Assignment	R-car W2H pin name	Clock Driver Pin Name	Signal Type
1	AC12	CLKP	REFCLK-	Differential signal
2	AB12	CLKN	REFCLK+	

3.17.3 Clock Signals Supplied to Devices Other than R-Car W2H

Table 23 List of Clocks and Crystals other than for R-Car W2H

NO.	Xn	Device	Device pin name	Frequency	Description	Part number	Manufacturer	Type
1	X3	AK4642EN	MCKI	12.288MHz	Audio Clock	SG-8003CE12.288000MHzPCL	Epson	Oscillator
2	Y3	GL852GT(USB Hub)	X1 , X2	12MHz	USB Hub Clock	FA-238A12.000000MHz10	Epson	Crystal
3	Y4	KSZ8041RNLI	XI , XO	25MHz	Ethernet clock	FA-238A25.0000MHz18	Epson	Crystal
4	Y5	RH850F1H/F1L	X1 , X2	12MHz	MCU main clock	FA-238A12.000000MHz10	Epson	Crystal
5	Y6	RH850F1H/F1L	XT1 , XT2	32.768kHz	MCU sub clock	FC-13A32.768000kHz12.5	Epson	Crystal

3.17.4 Block Diagram

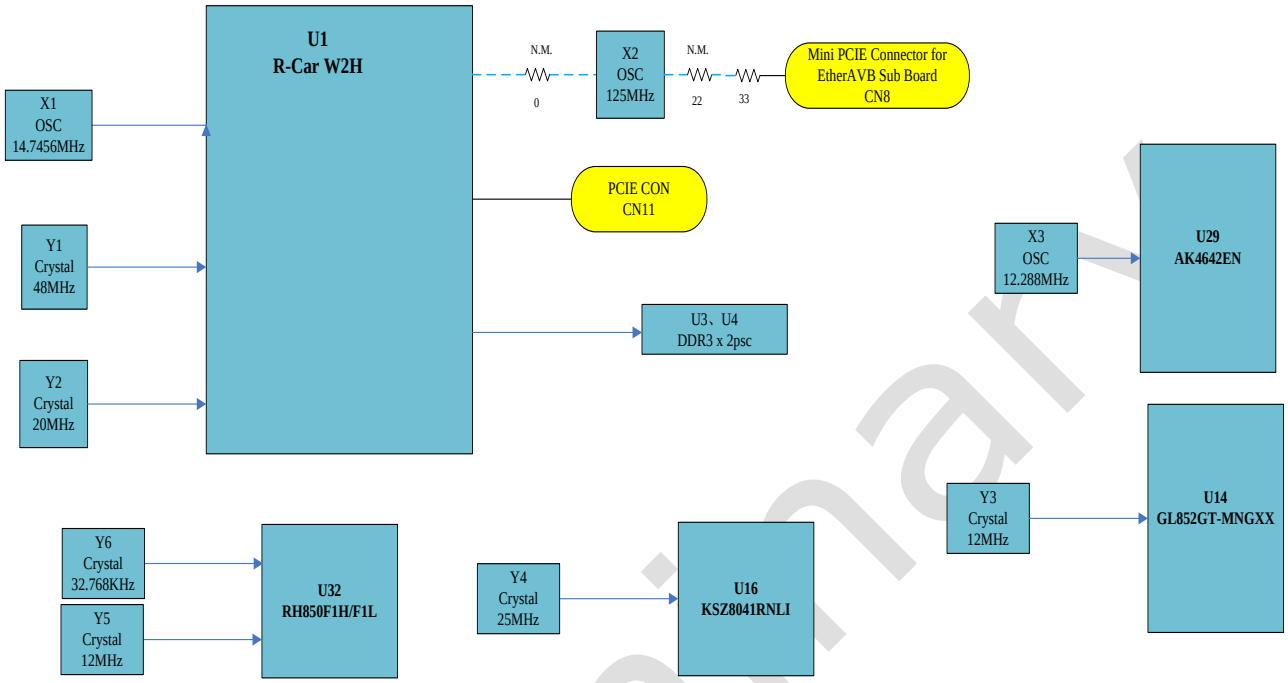


Figure 18 Block Diagram of the Clock system

3.18 External Interrupts

3.18.1 Specifications

The R-Car W2H has external interrupt input pins which are NMI, GP4_22, GP4_23, GP4_24, GP4_25, and GP5_8. For details on the external interrupts, please refer to the R-Car W2H Hardware Manual.

The Tethys board uses NMI as external interrupt input pin, GP4_22, GP4_23, GP4_24, GP4_25, and GP5_8 as GPIO interrupts.

These pins should be used as active-low signals in programs.

The devices and connectors of the interrupt request sources on the Tethys board are shown below table 24.

Table 24 External Interrupts Specifications

Interrupt Pin	Other pin function	Devices that Output Interrupt Request	Connectors
NMI	——	Test point TP5	——
GP4_22	RX3_A/SCL1_C/MSIOF1_RXD_B /AUDIO_CLKA_C/SSI_SDATA4_B	GYRO U28 A3G4250D from ST	——
GP4_23	TX3_A/SDA1_C/MSIOF1_TXD_B /AUDIO_CLKB_C/SSI_WS4_B		
GP4_24	SCL2_A/MSIOF1_SCK_B /AUDIO_CLKC_C/SSI_SCK4_B	G-SENSOR U30 AIS328DQ from ST	——
GP4_25	SDA2_A/MSIOF1_SYNC_B /AUDIO_CLKOUT_C		
GP5_8/IRQS#	SSI_SDATA7_A/ AUDIO_CLKA_D/CAN_CLK_D	ETHERNET KSZ8041RNLI from Micrel	——

3.18.2 Block Diagram

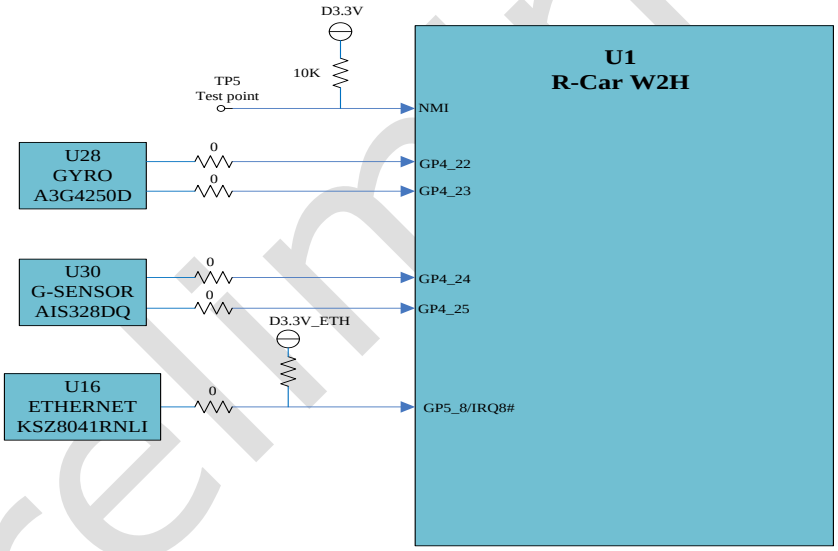


Figure 19 Block Diagram of the External Interrupts

3.19 Reset System

3.19.1 Specifications

On the Tethys board, the MCU power-on reset signal is cleared by the reset IC TPS3808G01DBVT, 389ms after the D3.3V power supply has settled. Also a power-on reset signal can be generated by pushing the push switch (SW4). The reset signal is level-shifted from 3.3 V to 1.8 V by the HD74LV1G08ACME and is input to the PRESET# pin of the R-CarW2H.

Table 25 Reset System Specifications

Reset IC	TPS3808G01DBVT from TI ● Threshold voltage: 1.7415V ● Reset delay time : 389ms (Reset delay time=CT (nF)/175+0.0005 (s))

3.19.2 Block Diagram

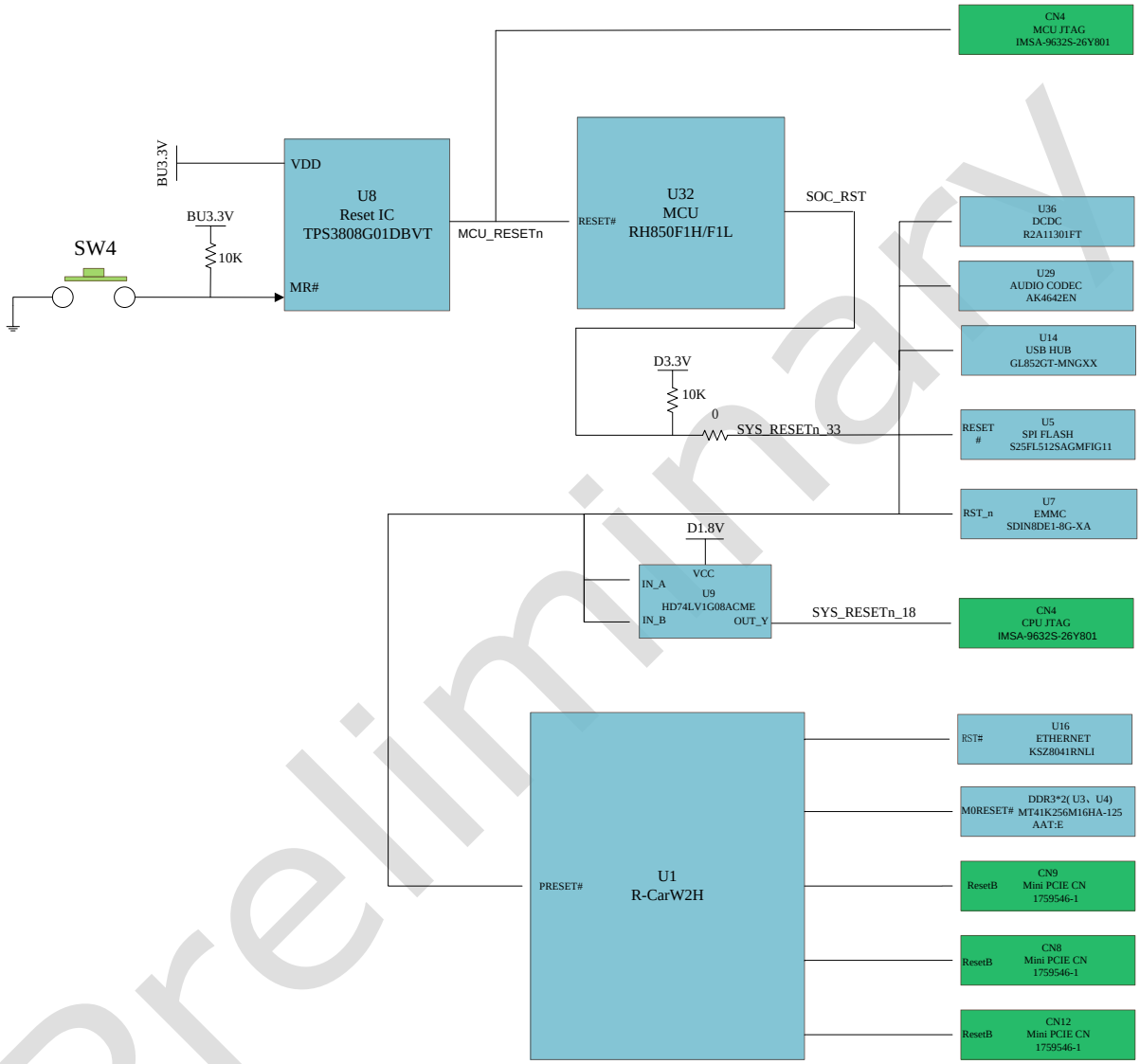


Figure 20 Block Diagram of the Reset System

3.19.3 Reset Sequence

The Reset sequence is shown below:

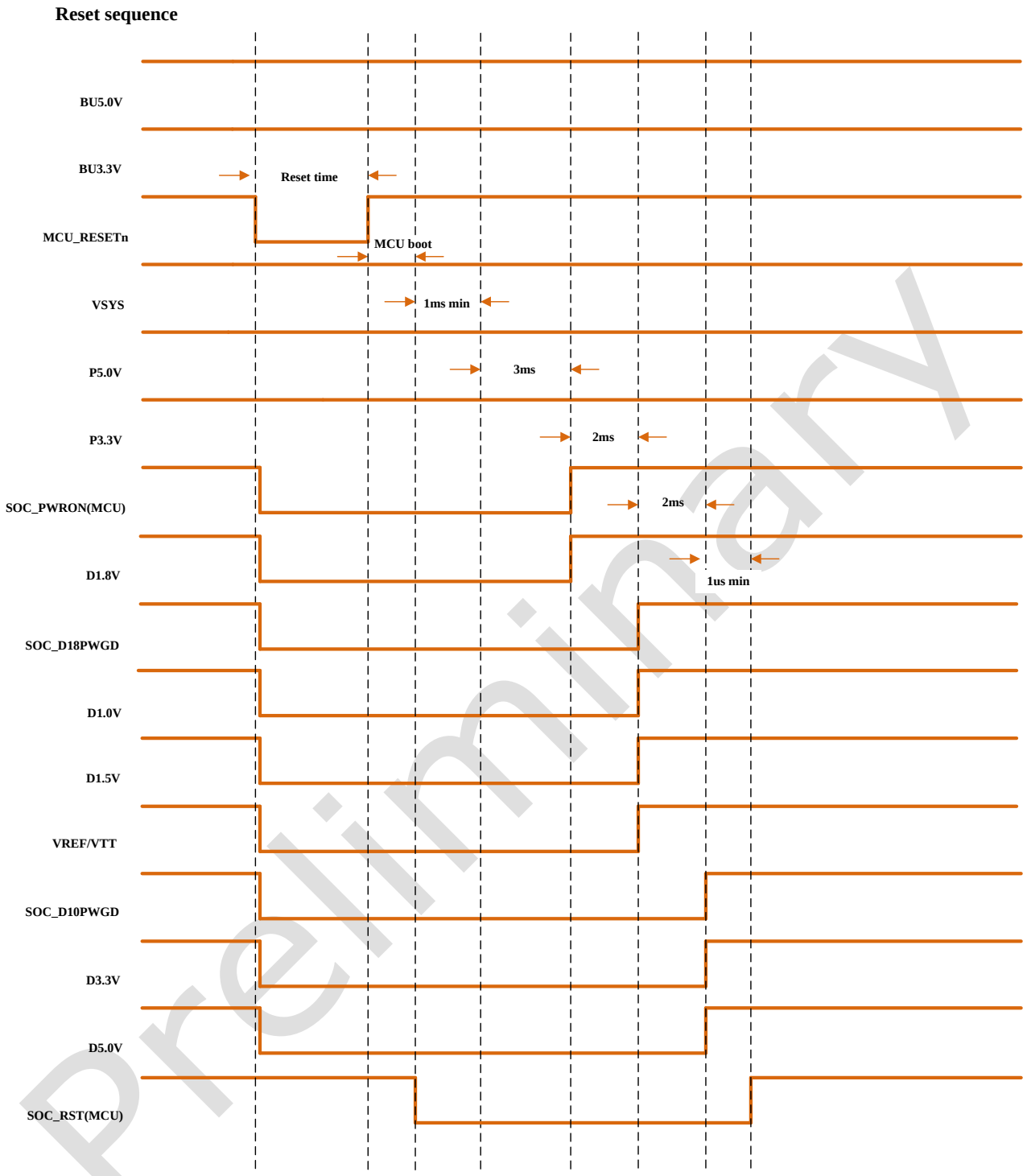


Figure 21 The Reset Sequence

3.20 Power system

3.20.1 Specifications

The Tethys board operates on a single BU12V power supply. The power supplies used for the Tethys board are generated by the switching regulators and low-dropout regulators. Because the maximum output current of the AC adapter attached for Tethys board is 3A at 12v input status, please make sure not to exceed 3A for all sub-board inserted in extending interface connector such as mini PCIE etc. If end user need more current AC adapter, please prepare over 6A/12V stable AC adapter by end user.

Table 26 List of the Switching Controllers and Regulators on the Tethys Board

Vin	Vout	Switching Controller/Regulator	Power MOSFET	ACC Switch Control
Power Supply BU12V Through CN17 or CN18 (1*)	BU12.0V	_____	_____	Not supported
BU12.0V	VSYS	Renesas R2A11301FT (U36)	Renesas HAT2210R (U35 and U37)	supported
	BU5.0V			supported
	P3.3V			supported
	PCIE_5.0V	Texas Instruments TPS54531DDA(U26)		supported
VSYS	P5.0V	Vishay Siliconix Si3433CDV-T1-E3(U34)		supported
BU5.0V	BU3.3V	RICOH RP111N331D-TR-AE(U33)		supported
P3.3V	D3.3V	Vishay Siliconix SI3433CDV-T1-E3(U40)		supported
	D1.5V	Texas Instruments TPS3808G01DBVT(U45)		supported
	D2.5V	RICOH RP111N251D-TR-AE(U46)		supported
P5.0V	D1.2V	Texas Instruments TPS54531DDA(U44)		supported
	D1.8V	SEMTECH SC183CULTRT(U38)		supported
	D5.0V	Vishay Siliconix Si3433CDV-T1-E3(U43)		supported
D3.3V	VCCQ_SD2	RICOH RP111N181D-TR-AE(U12)		supported
	VCCQ_SD0	Vishay Siliconix		Supported

		SI3433CDV-T1-E3(U13)		
BU3.3V	BU3.3V_MCU			supported

(1*) CN17 and CN18 are 12V power connectors , use can choose one connector according to the demand

3.20.2 Block Diagram

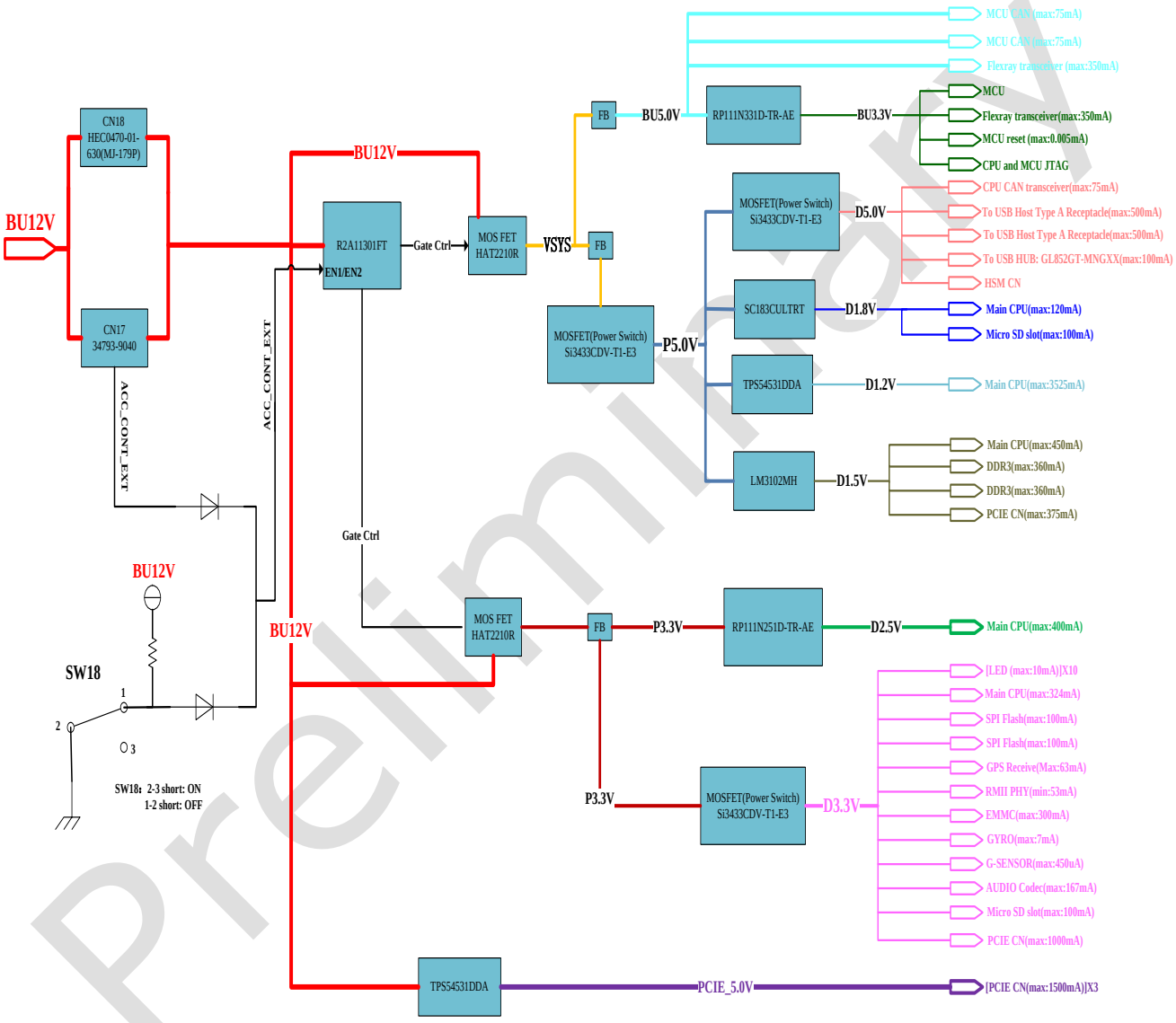


Figure 22 Block Diagram of the Power System

3.20.3 Power Sequence

There are no restrictions on the power-on sequence. Ensure that all other power supplies rise from the ground (VSS**) within 300 ms of any single power supply rising from the ground (VSS**) . We do power up sequence as the Tethys power up sequence. The diagram of the sequence for turning on the power to the Tethys board is shown as below

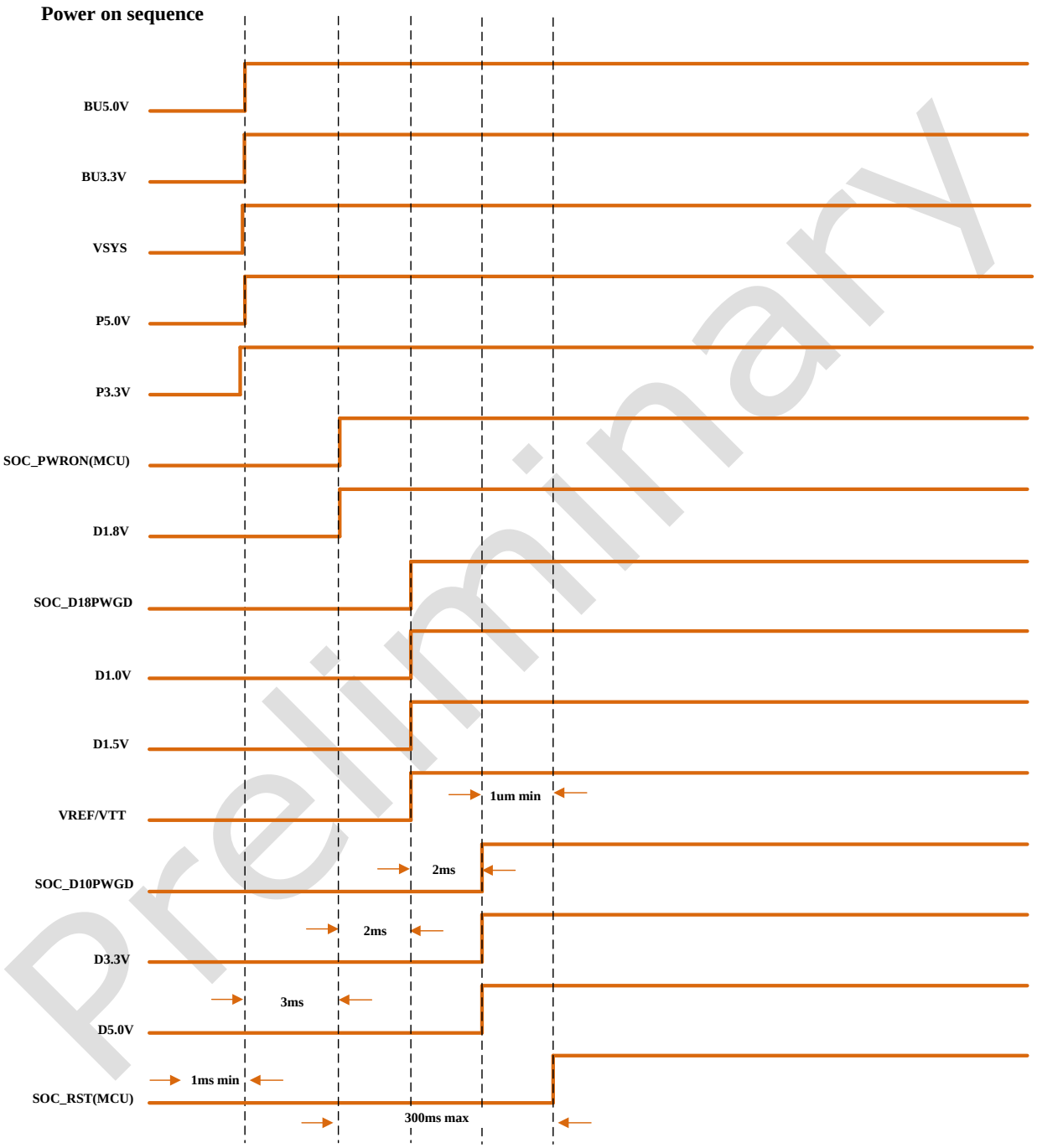


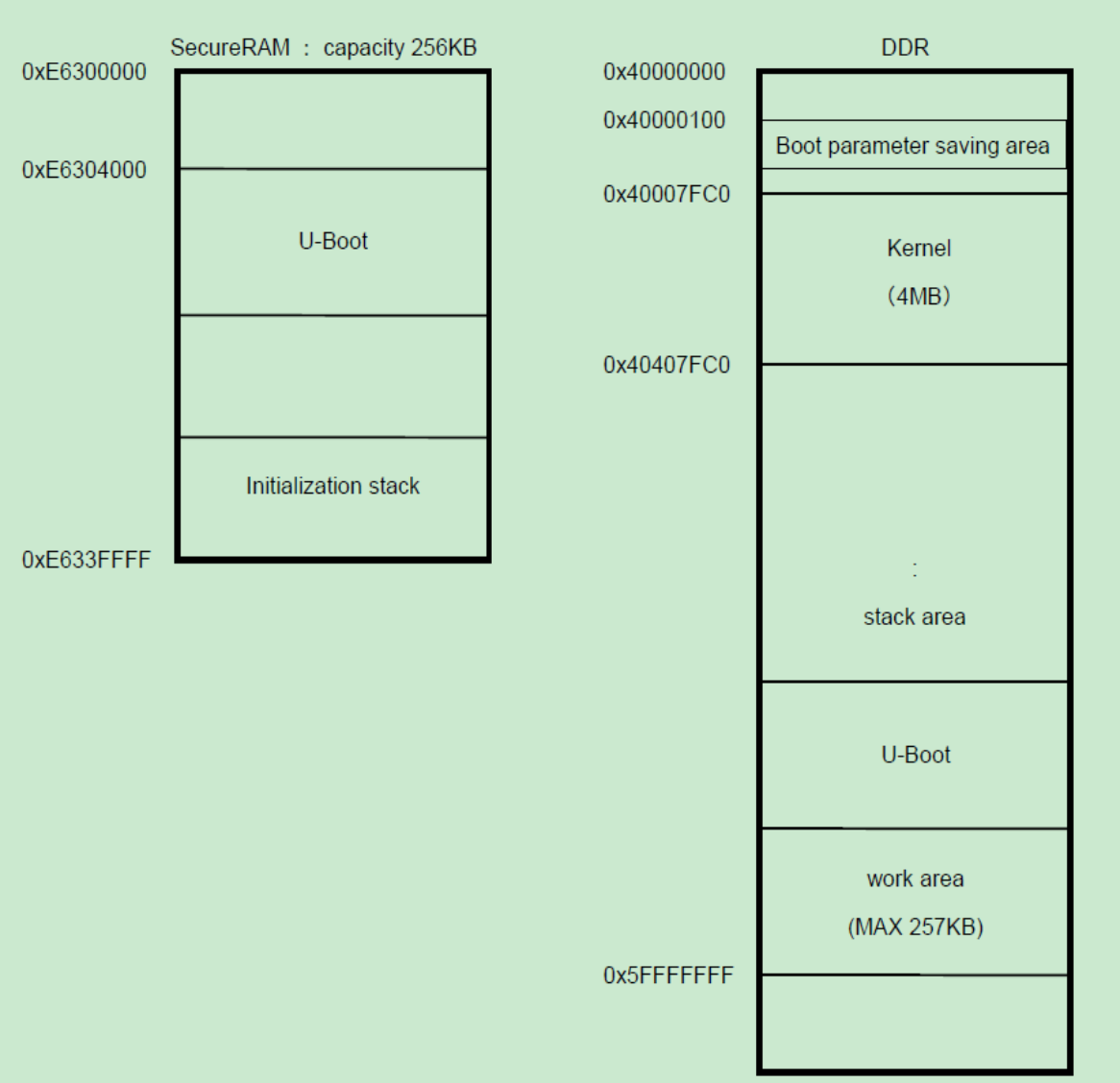
Figure 23 The Power Sequence

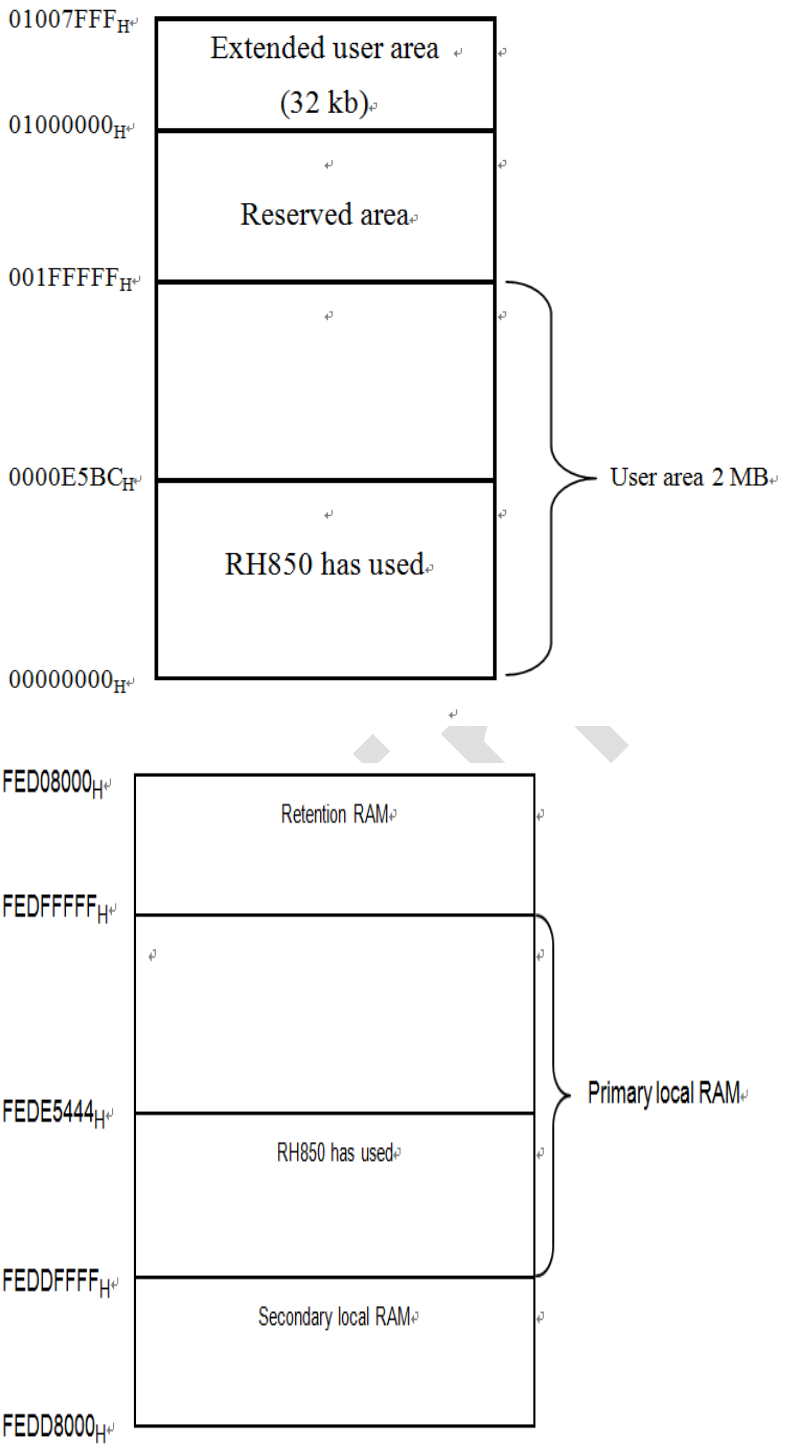
There are no restrictions on the power-off sequence. Ensure that all other power supplies fall to the ground (VSS**) level within 300 ms of any single power supply being turned off. We do the power off sequence as the Tethys power off sequence , turn off the power supplies in reverse order of the power-on sequence.

4 Memory map

4.1 Specifications

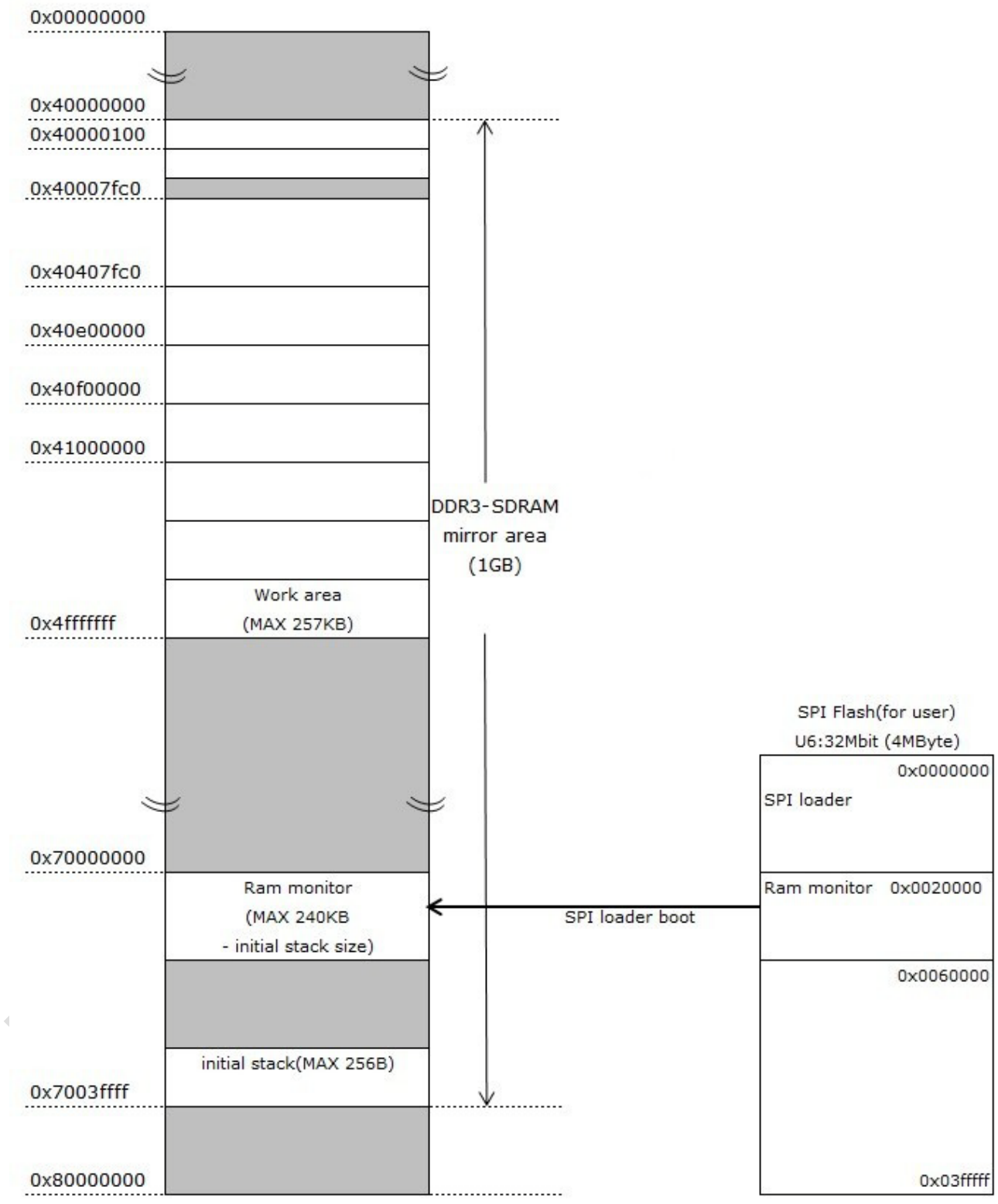
Memory map for R-CarW2H boot loader is shown below. The maximum size of U-Boot is the value that subtracted Initialization stack from 240Kbytes. The maximum size of initialization stack is 256Kbytes.



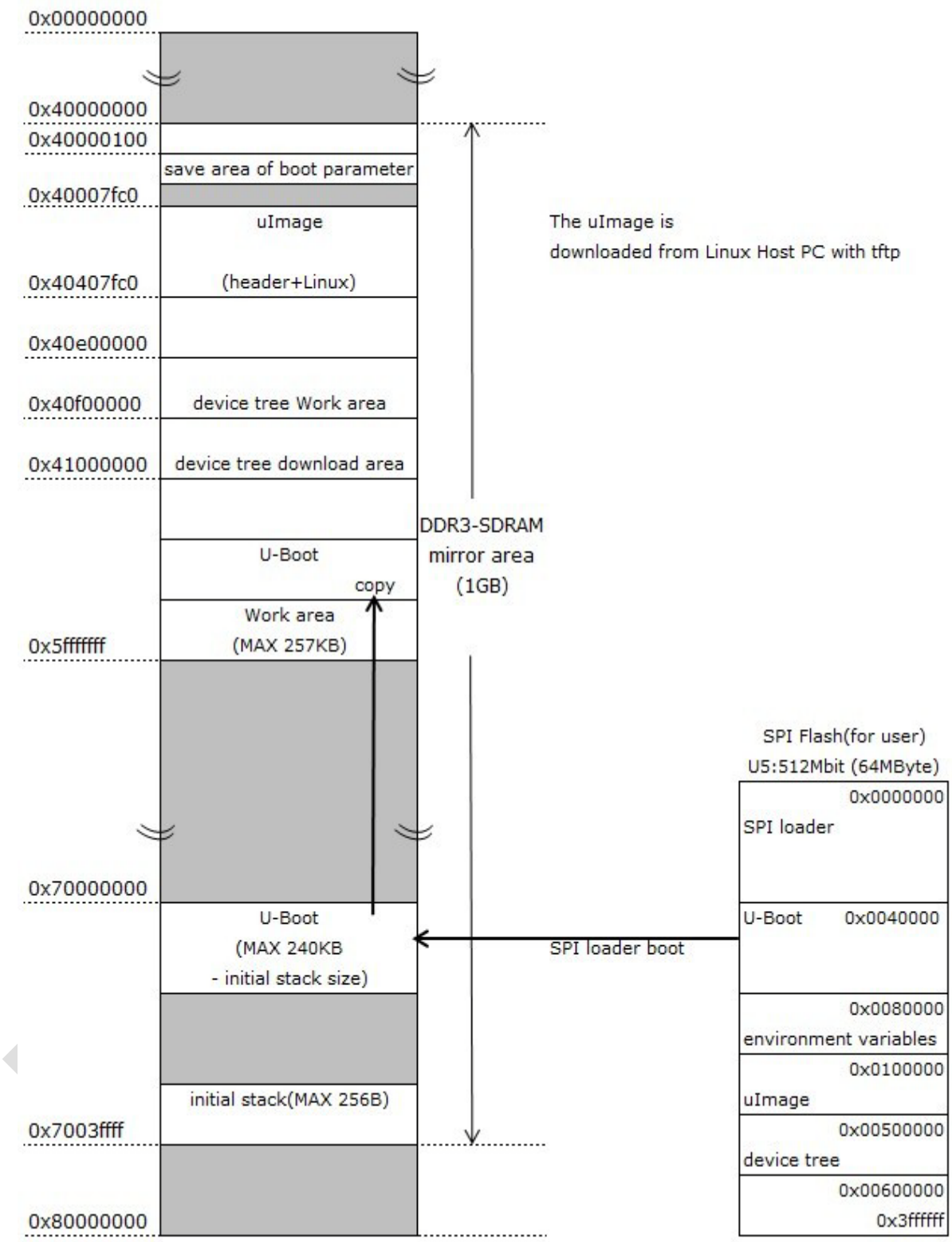


Memory map for RH850F1H/F1L is shown in the above figure. The user area of the code flash memory of the RH850F1H/F1L is 2MB. A single block of 32-Kbyte extended user area is also incorporated.
RH8500F1H/F1L includes three types of the local RAM: Primary local RAM, Secondary local RAM, Retention RAM. RH850's data memory uses Primary local RAM which is RAM area that can be accessed with speed.

Memory map for 32MB SPI flash is shown below:



Memory map for 512MB SPI flash is shown below:

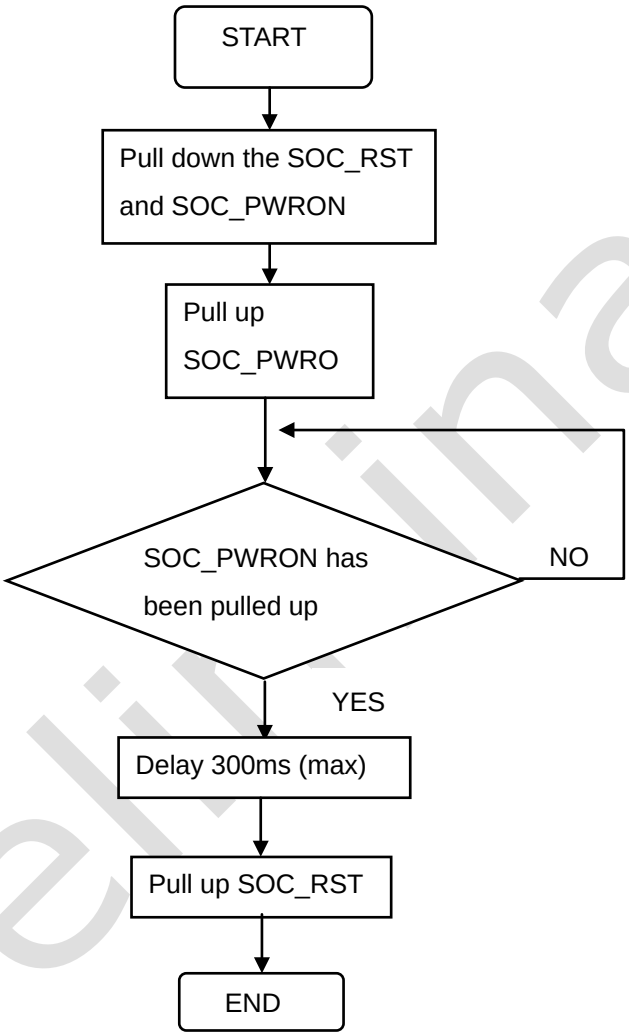


4.2 Function

These codes of RH850 have realized four functions as follows.

4.2.1 Control the power of the Tethys Custom Board.

The flow chart is as follows:



4.2.2 Realize the UART with the baud rate of 115200

This UART uses RLIN31 of RH850's LIN/UART interface.

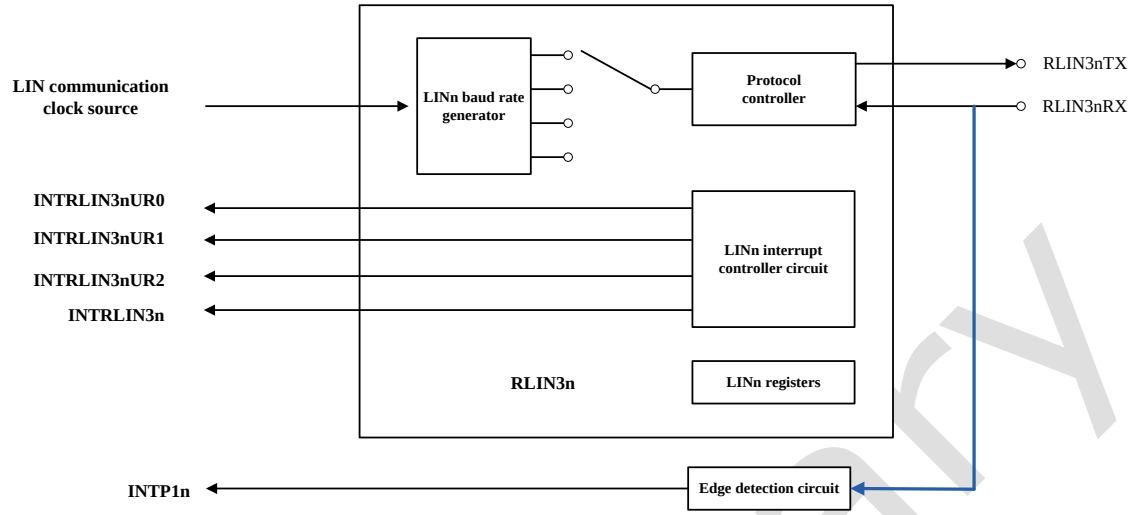


Figure shows LIN/UART interface (in UART mode) transmission operations as follows

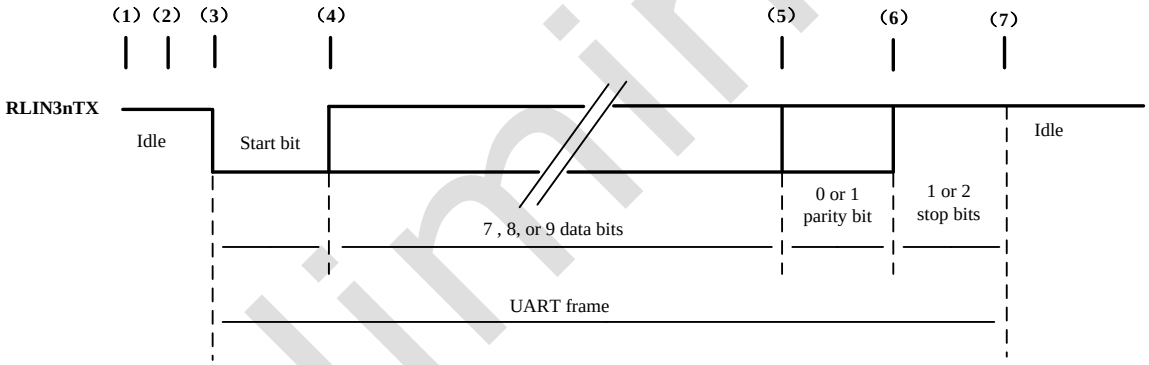
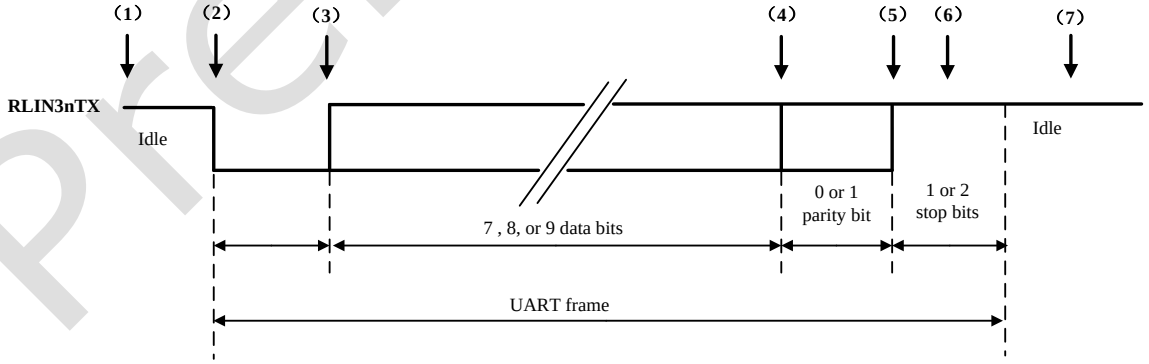


Figure shows the LIN/UART interface (in UART mode) reception operation as follows.



(about [NSPB],[IBS]'s definition, please refer to [r01uh0445ej0100_rh850f1h.pdf] page 937,859's description).

This UART's operations are as follows:

1. 15 : The NSPB bits select the number of sampling in one Tbit (reciprocal of the bit rate).
2. Noise filter ON: The noise filter is enabled when receiving data
3. Non-parity, 8bit, 1stop.
4. No space: The IBS bits set the width of the space between the UART frame in UART buffer transmit

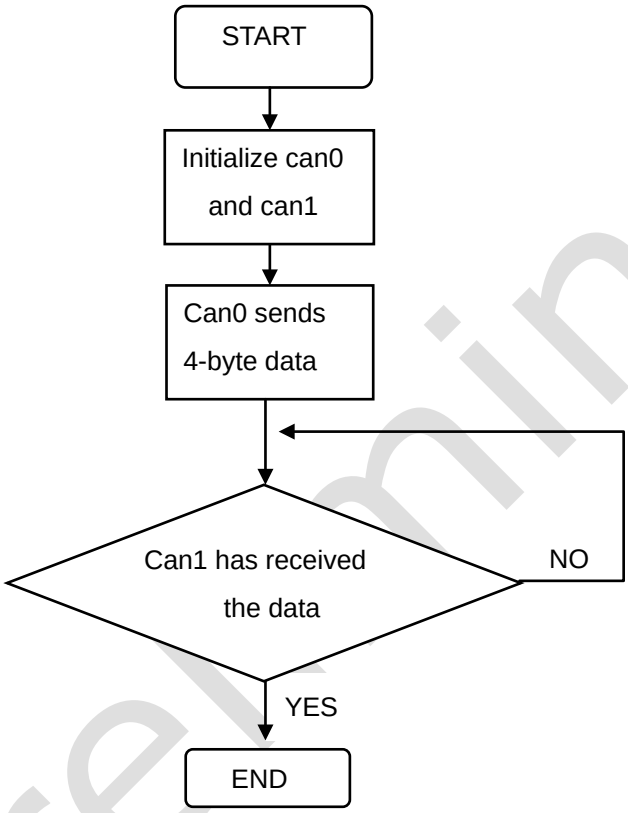
4.2.3 Realize an asynchronous serial with baud rate of 1M between RH850 and CPU.

This UART uses RLIN30 of RH850's LIN/UART interface. The operations are same as above.

4.2.4 Make CAN0 and CAN1 working with baud rate of 1M

1. CAN0 sends 4-byte data only once.
2. CAN1 receives the data coming from CAN0.
3. Once CAN1 receives, the wave form can not be monitored.

The flow chart is as follows



5 Outline Diagrams of the Tethys Board

5.1 Tethys Board dimension

The Tethys board dimension is shown as below (Unit: mm):

Board : 1.6 mm

Board : 8 Layers

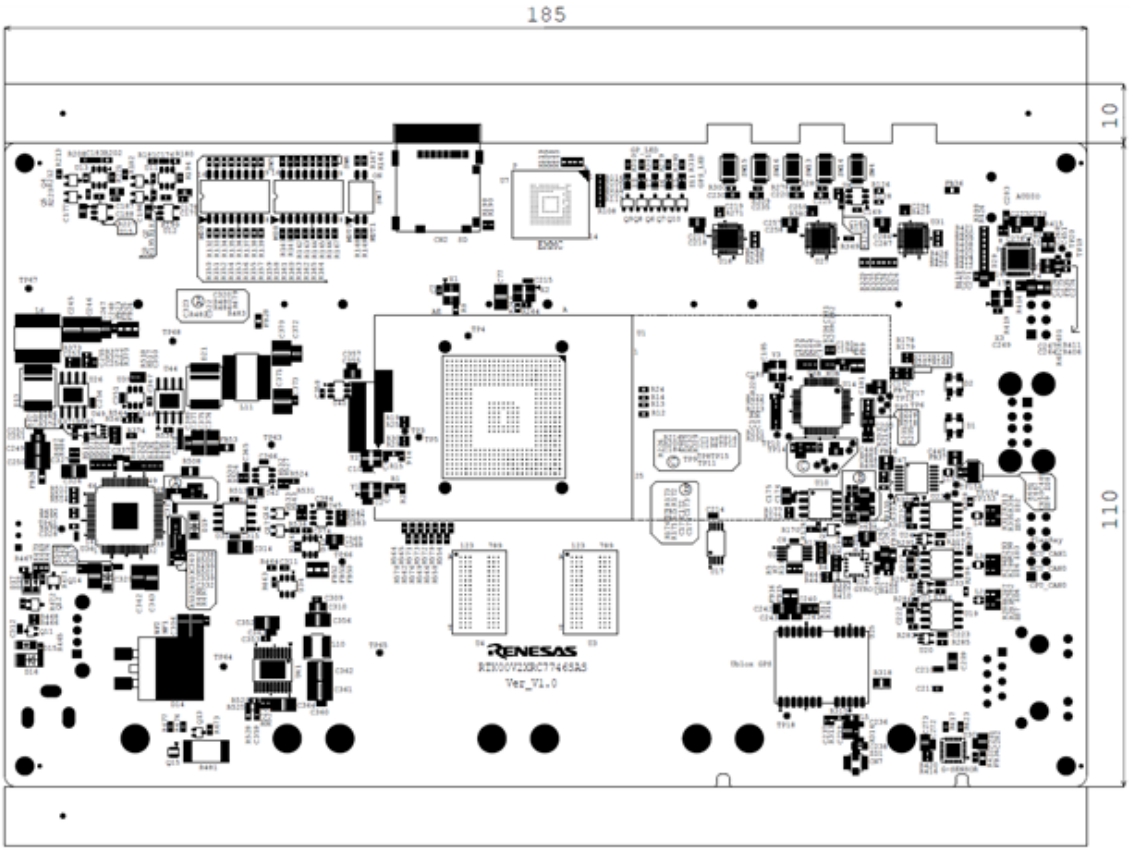


Figure 24 The Tethys board dimension

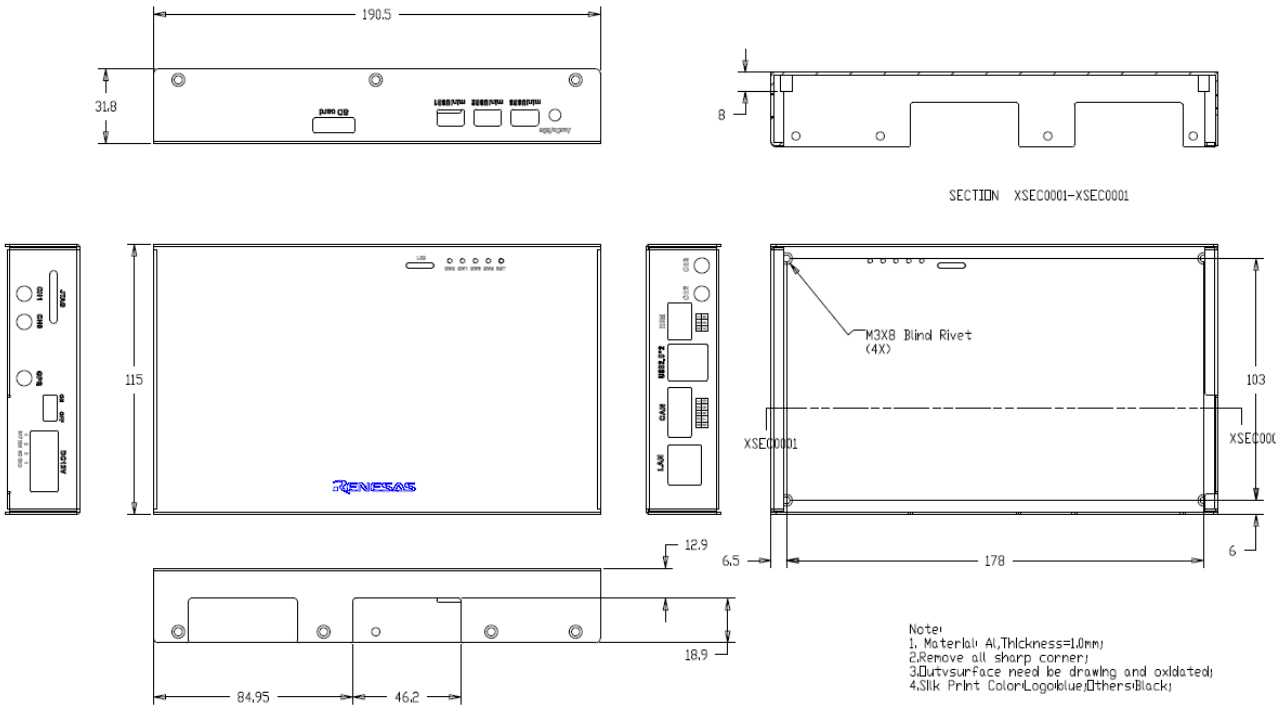
5.2 The weight of the Tethys Board

Condition	Weight (Unit : g)
Screw (total)	4
Spacer (two piece)	4
Shell	165
Heat dissipation silica gel	4
Board	143
RF Cable (15cm, four piece)	16
RF Cable (20cm, one piece)	5
Tethys assembly(total)	341

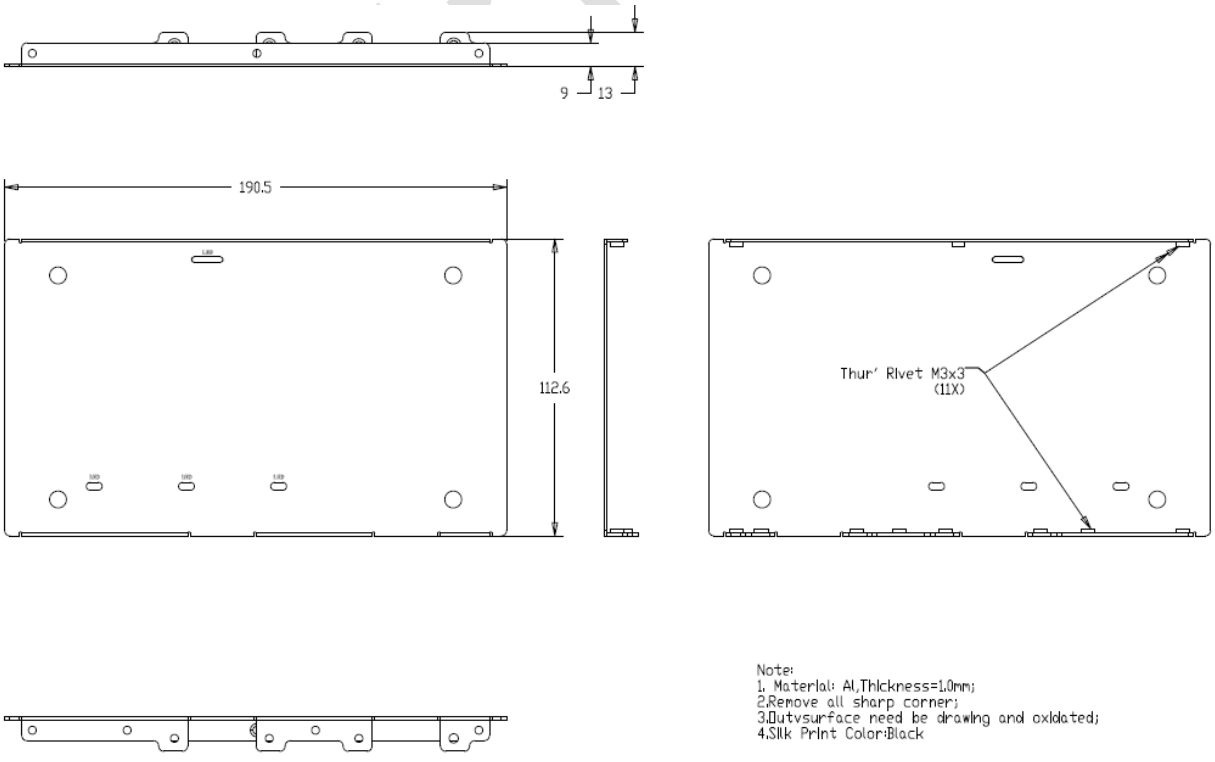
5.3 Tethys ID dimension

The ID of Tethys board dimension is shown as below (Unit: mm):

Base Panel size

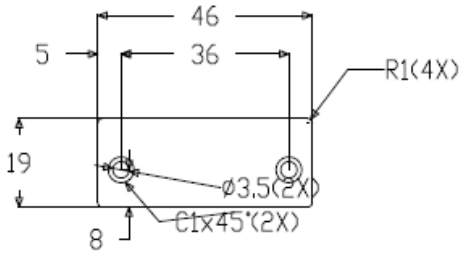


Cover Panel size:

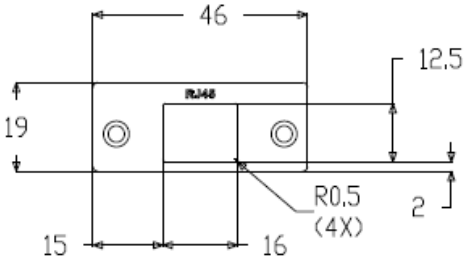


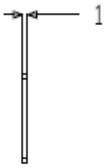
Side Cover size (Option)

Panel-Blank

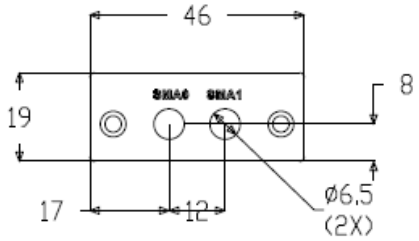


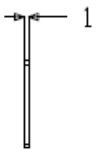
Panel-Ethernet





Panel-Coaxial

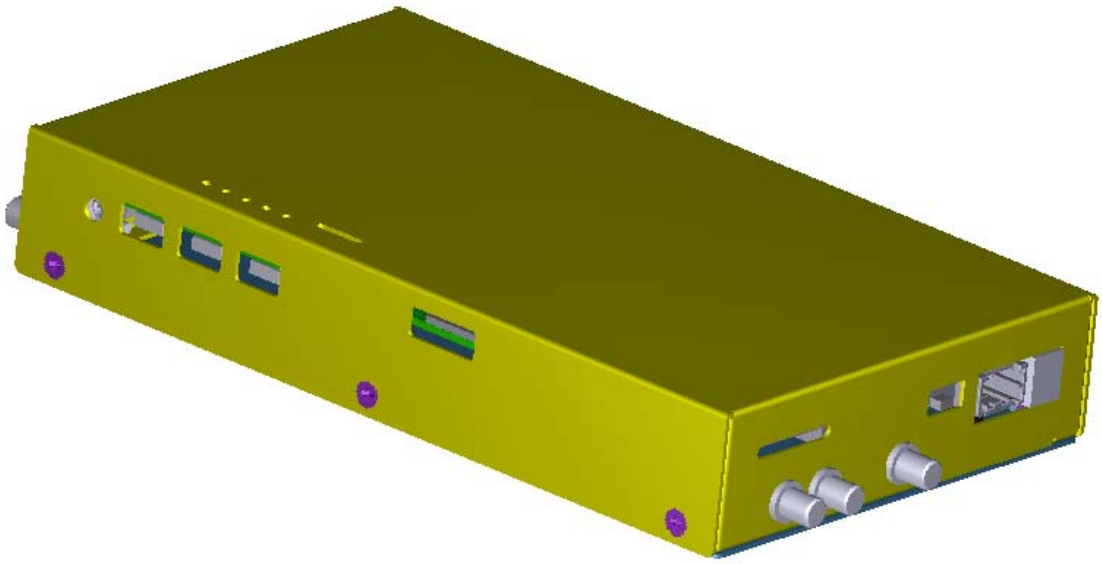




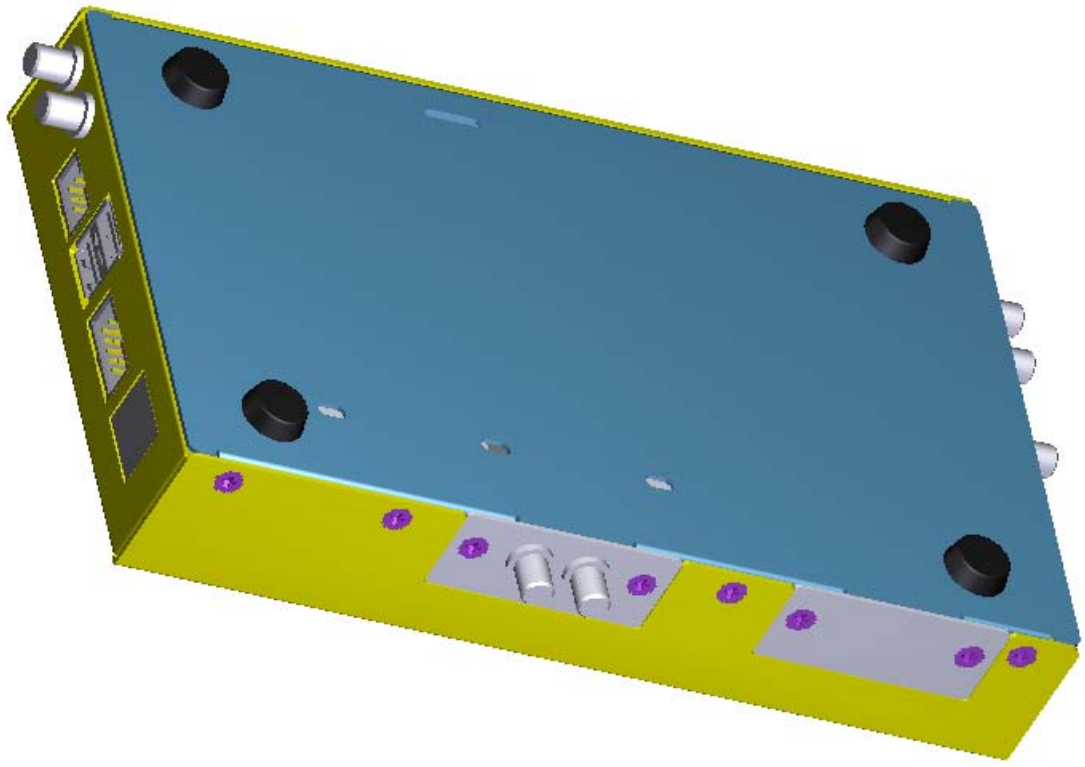
5.4 Tethys assembly

The assembly pictures of Tethys board are shown as below

Top side view:



Bottom side view:



Top Side View：

Bottom Side View：

Left Side View

Right View Side

Front Side View

Back Side View

V2X RF Cable/GPS RF Cable connection image internal AL case

6 Board connectors

6.1 TOP side connectors

The top side connector is shown as the picture in the following.

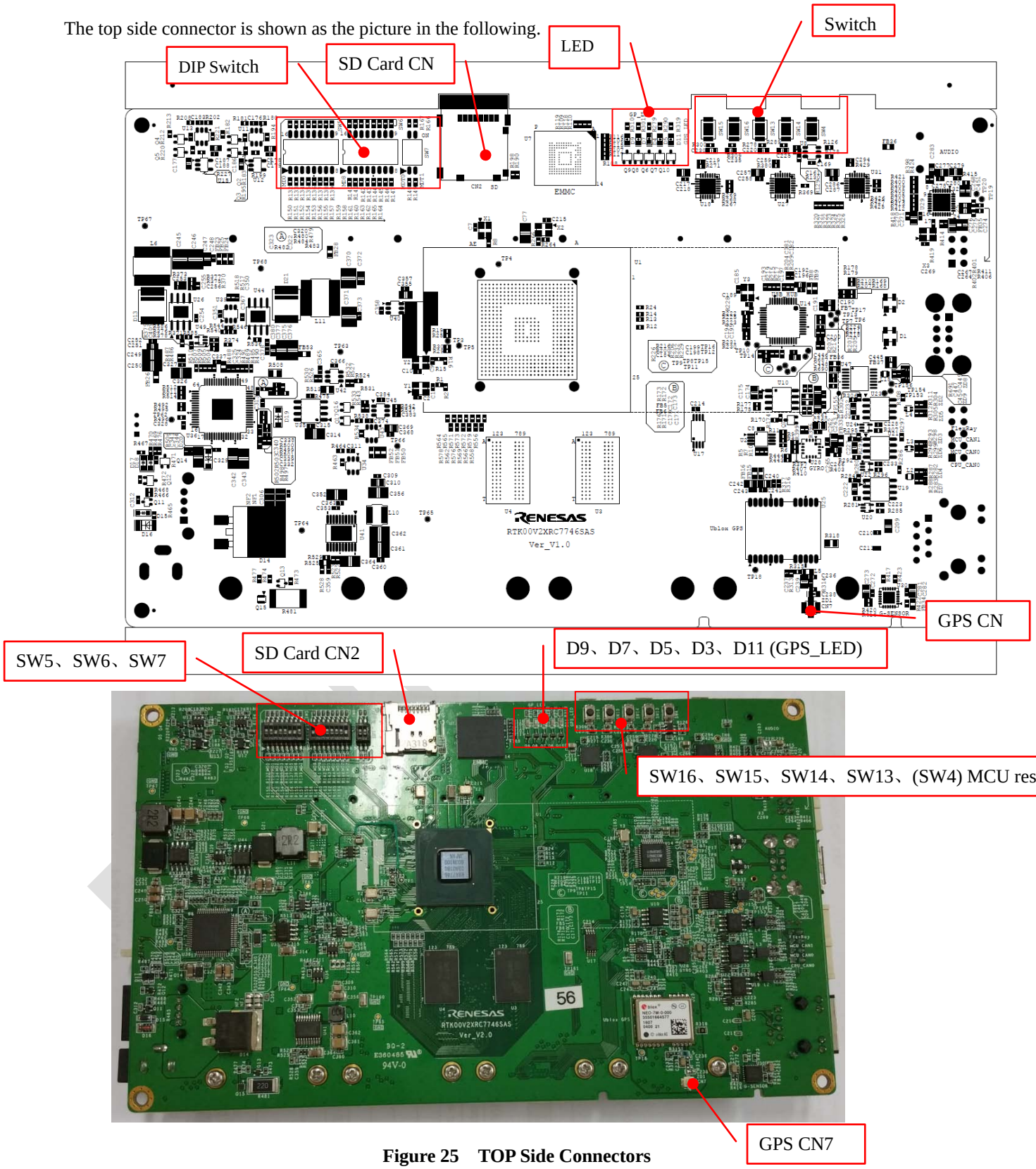


Figure 25 TOP Side Connectors

6.2 Bottom side connectors

The bottom side connectors are shown as the picture in the following.

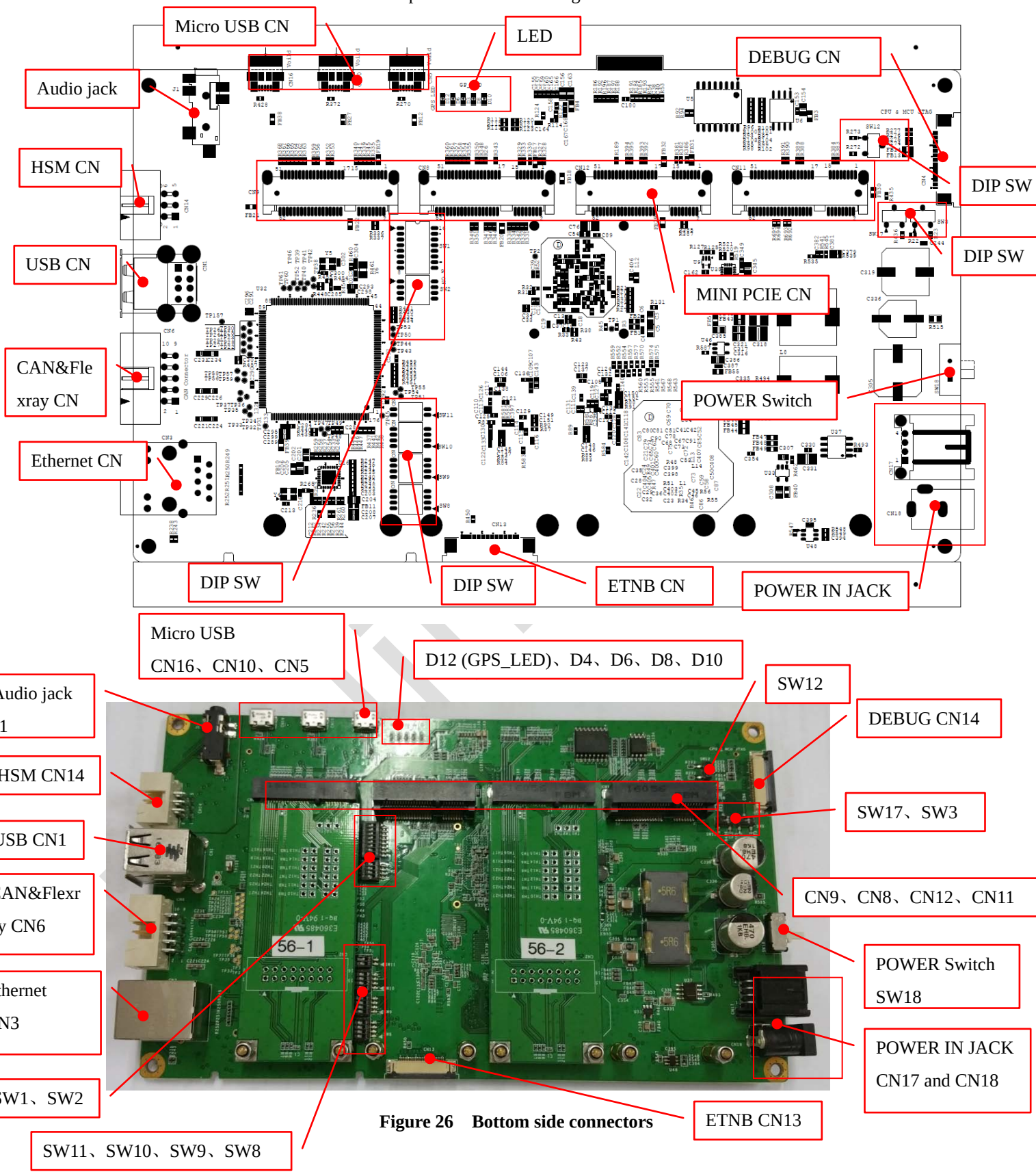


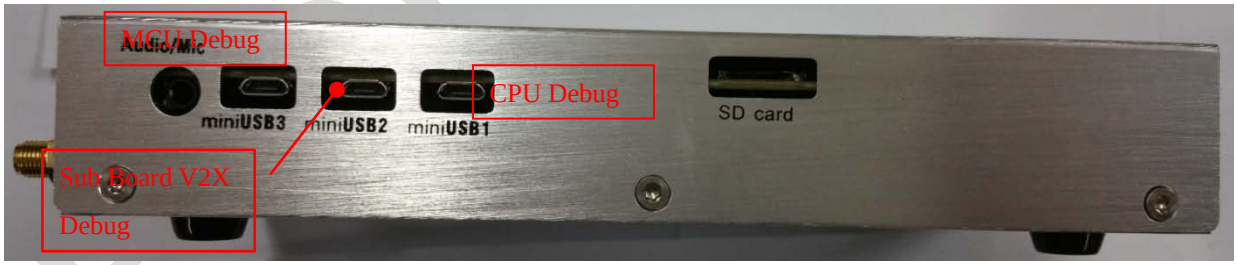
Figure 26 Bottom side connectors

6.3 The details of connectors

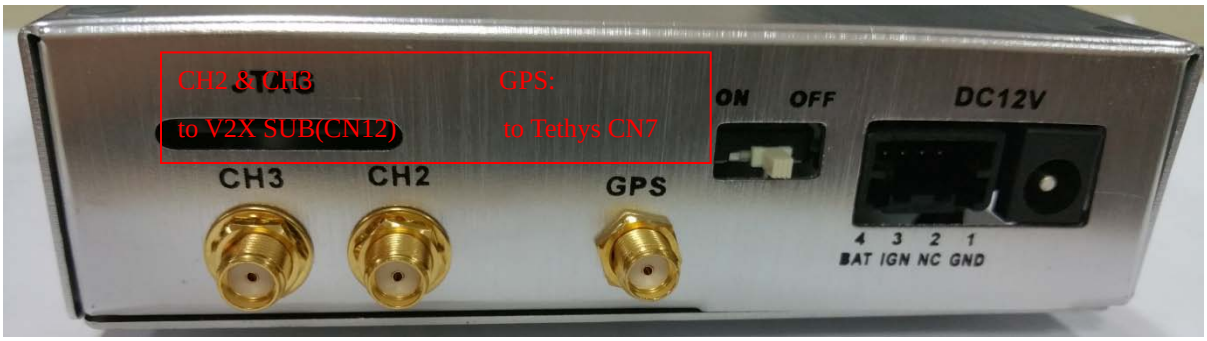
(1) There are two USB connectors, the CN1B is corresponding to Tethys from HUB and CN1A is corresponding to Tethys from W2H respectively as the picture shown above.

(2) The CAN pin assignments are shown as below:

CN6 PIN Number	Signal	Remark
1	CPU_CAN0_H	HIGH-level CAN bus line
2	CPU_CAN0_L	LOW-level CAN bus line
3	MCU_CAN0_H	HIGH-level CAN bus line
4	MCU_CAN0_L	LOW-level CAN bus line
5	MCU_CAN1_H	HIGH-level CAN bus line
6	MCU_CAN1_L	LOW-level CAN bus line
7	BP	Flexray bus line plus
8	BM	Flexray bus line minus
9	GND	Ground
10	GND	Ground

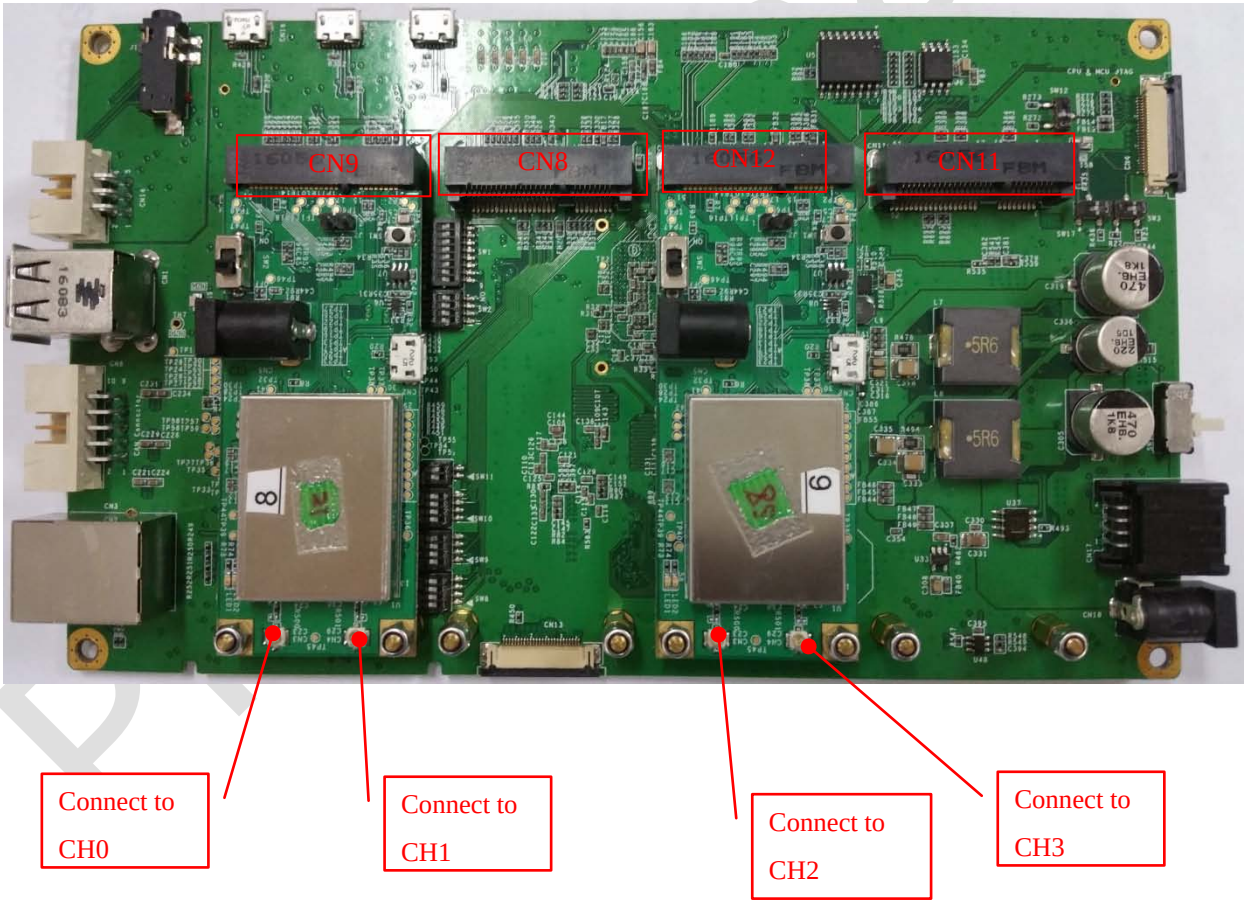


As the picture shown above, there are there USB2UART connectors From the left to right as the figure shown, they are for MCU debug, sub board V2X debug and CPU debug respectively.



As the picture shown above, there are five RF connectors to the antenna. In the inner connection, the CH2 and CH3 are for the V2X sub-board which is inserted in Tethys MINI PCIE connector CN12, the CH0 and CH1 are for the V2X sub-board which is inserted in the Tethys MINI PCIE connector CN9. The GPS is for Tethys GPS module antenna connector CN7 at the top side.

One possible connection is shown as the picture in the following picture:



7 Appendix

7.1 USB debug Cable

USB debug Cable Length：1.5m, This USB cable is used for Micro USB type B connector CN5, CN10, CN16 for debug on V2X main board. This cable can be inserted to miniUSB1/miniUSB2/miniUSB3 connector .

Figure 27 Image of USB debug cable

7.2 AC Adapter

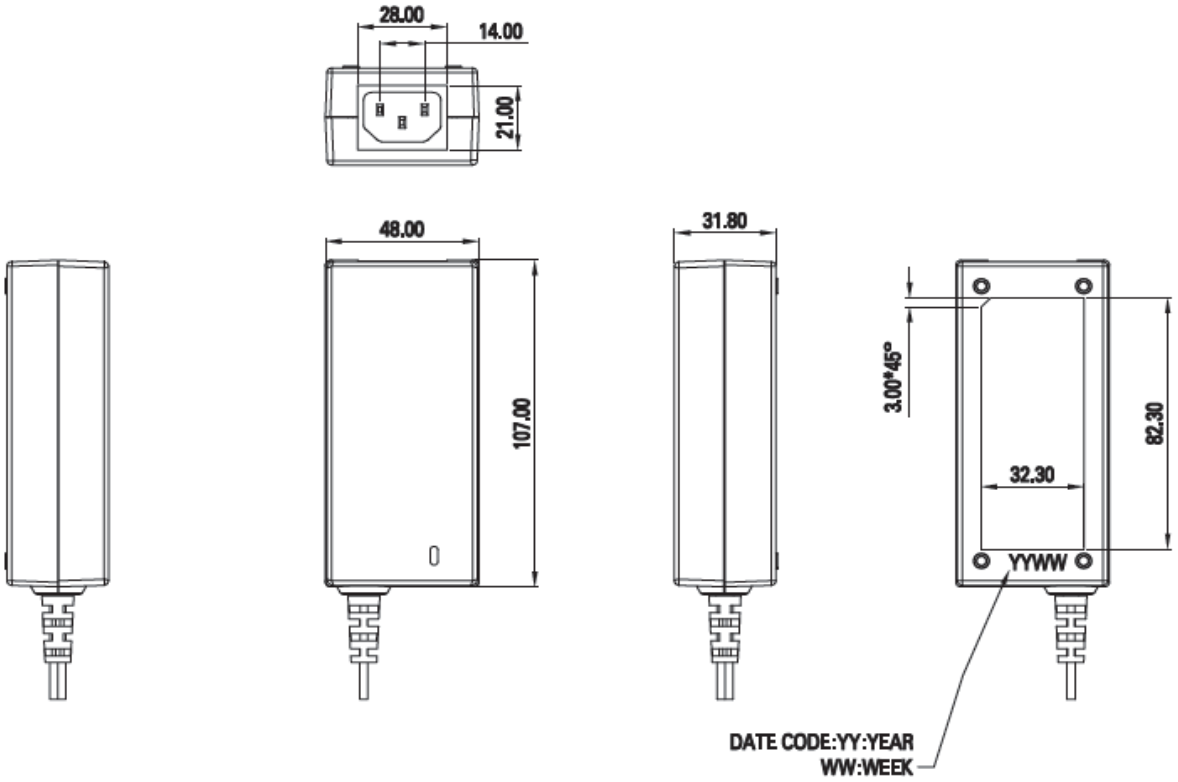
This 12V AC adapter is used for power supply to the Tethys .

7.2.1 Specifications

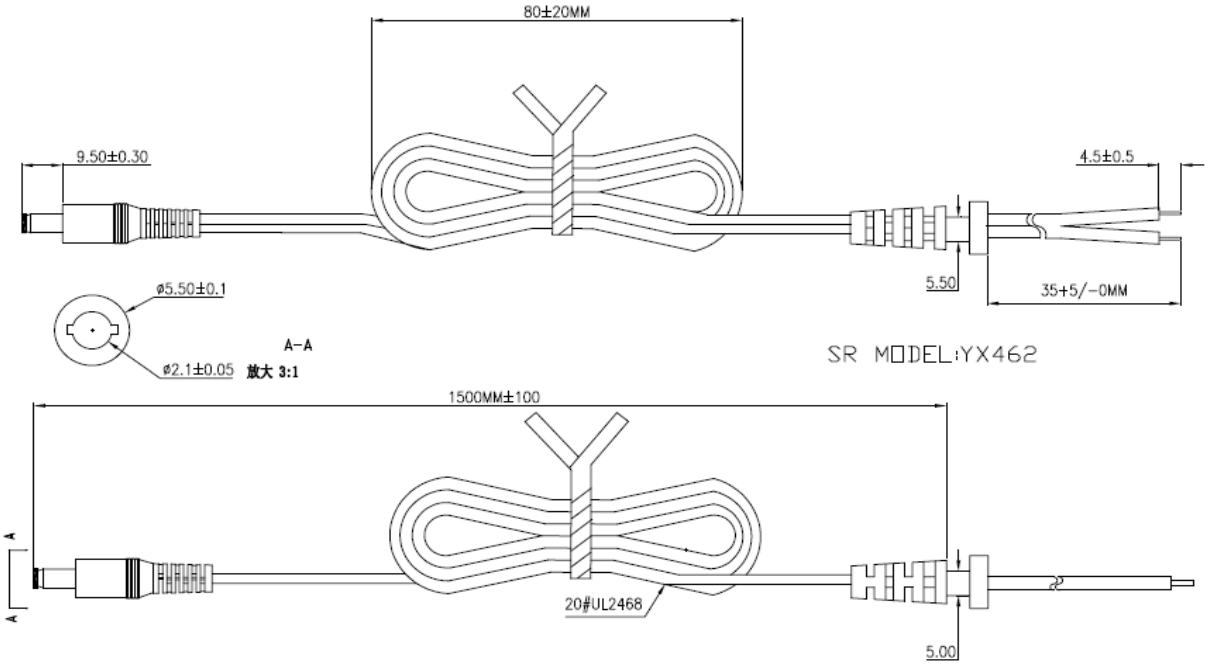
Item	Specification
Part Number	GPE048A-120300-W
Manufacturer	GOLDEN PROFIT ELECTRONICS LTD
Input voltage range	90-264V AC
Input frequency range	63/47 Hz
AC input current	1A Max .@100V AC
AC input power saving	0.075W Max .@230V AC at no load
Inrush Current	60 A Max .@100VAC (Cold start） 90 A Max .@230VAC (Cold start）
Leakage current	0.25mA Max
Output voltage	12V
Max. load current	3A
Min. load current	0A
Output voltage	12 V± 5%
Output ripple & noise	12 V± 5%
Total output power	36 W
Operating Temp	0~40℃
Storage Temp	–25℃ to 85℃

7.2.2 Mechanic Size and Picture

Mechanic Size：



Cable Spec：



LOG Image：

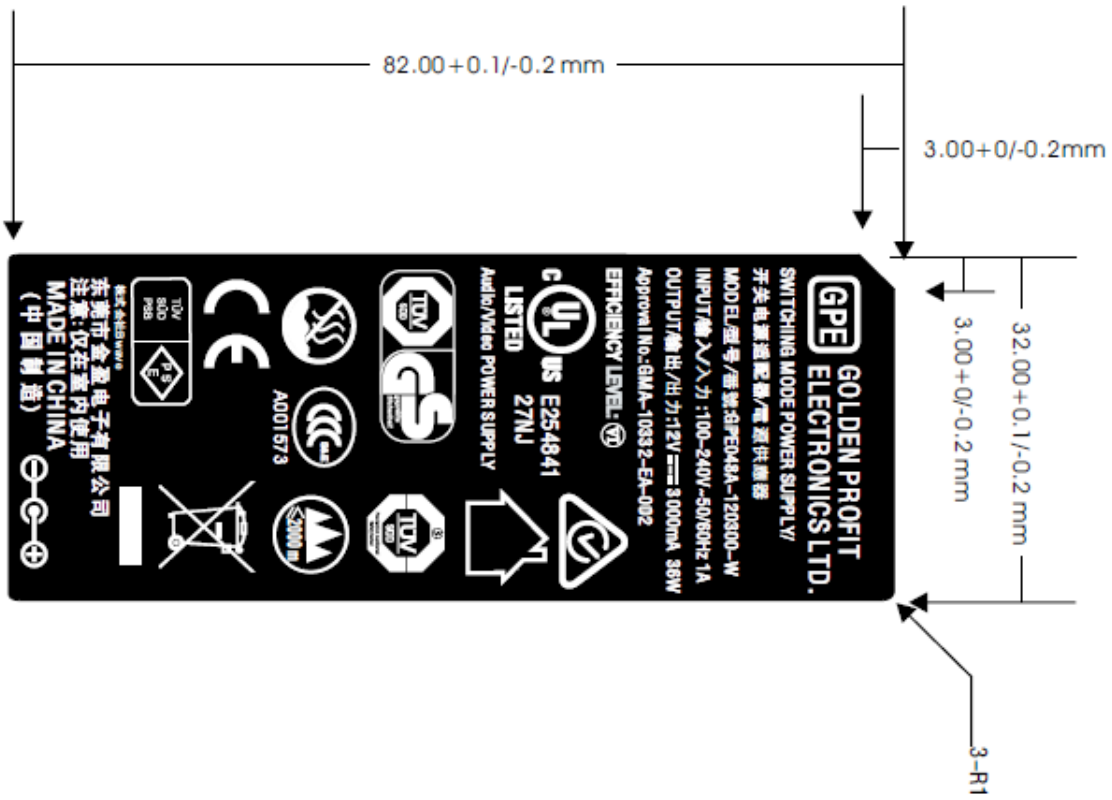


Figure 28 Power Adapter ID LOG specification

Figure 29 Image of Power Adapter

7.3 GPS antenna

7.3.1 Specification

About GPS antenna specification, please refer to the following data:

Table 27 Antenna Specification for GPS module

Item	Specification
Part Number	DAM1575 A4D1
Manufacturer	Taiwan ACC
Cable Length	5m
Center Frequency	1575MHz ± 3MHz
VSWR	Maximum 2.0
Bandwidth	Minimum 20MHz
IF Resister	50ohm
Peak Gain	4 dBic(base on 70mm x 70mm ground plane)
Gain coverage	≥-4dBic at -90°<θ<+90°（over 75% volume）
Polarity	RHCP
Power consumption	1 watt
Gain	30dB(typical)
Noise parameter	1.5dB(typical)
Material	Copper
Plating treatment	Gold plating
Male/Female	Male
Filter	-24dB(±100mHz)
DC voltage	3-5.0V ±0.25V
DC current	Maximum 16mA
Weight	≤110 g
Size	50x50x17 mm3
Cable type	rg174, 5m
IF Type	SMA
Color	Black
Work temperature	-40℃~ +85℃
Save temperature	-40℃~ +85℃
Vibration	sine wave, 1g(0-p) 10-150-10Hz for each axis
Humidity	95%~100%, no condensation

This GPS antenna connect the SMA connector labeled GPS in the case. Cable Length： 5m

Figure 30 Image of GPS Antenna from Bottom view

Figure 31 Image of GPS Antenna from Top view

7.4 V2X Antenna1 with 2m cable

7.4.1 Specification

About V2X antenna specification, please refer to the following data:

Table 28 Antenna Specification for V2X (2m cable)

Item	Specification
Part Number	6073F00005
Manufacturer	Signal Plus
Frequency Range	5860~ 5920MHz
Polarization	Horizontal
Impedance	50 Ohm
VSWR	2.0 Max
Gain	3.0dBi(without cable loss) -1.0dBi(with cable loss)
Cable Loss	4.0dB(L=2m)
Radiation	Omni Directional
Cable length	2m
Antenna Cap	ABS
Color	Black
Connector	SMA Plug Standard
Material	Copper
Plating treatment	Gold plating
Male/Female	Male
Operating Temp	-.20℃ ~ +65℃
Storage Temp	-.30℃ ~ +75℃

This Antenna's radiation pattern is described as below figures.

3D Chamber:

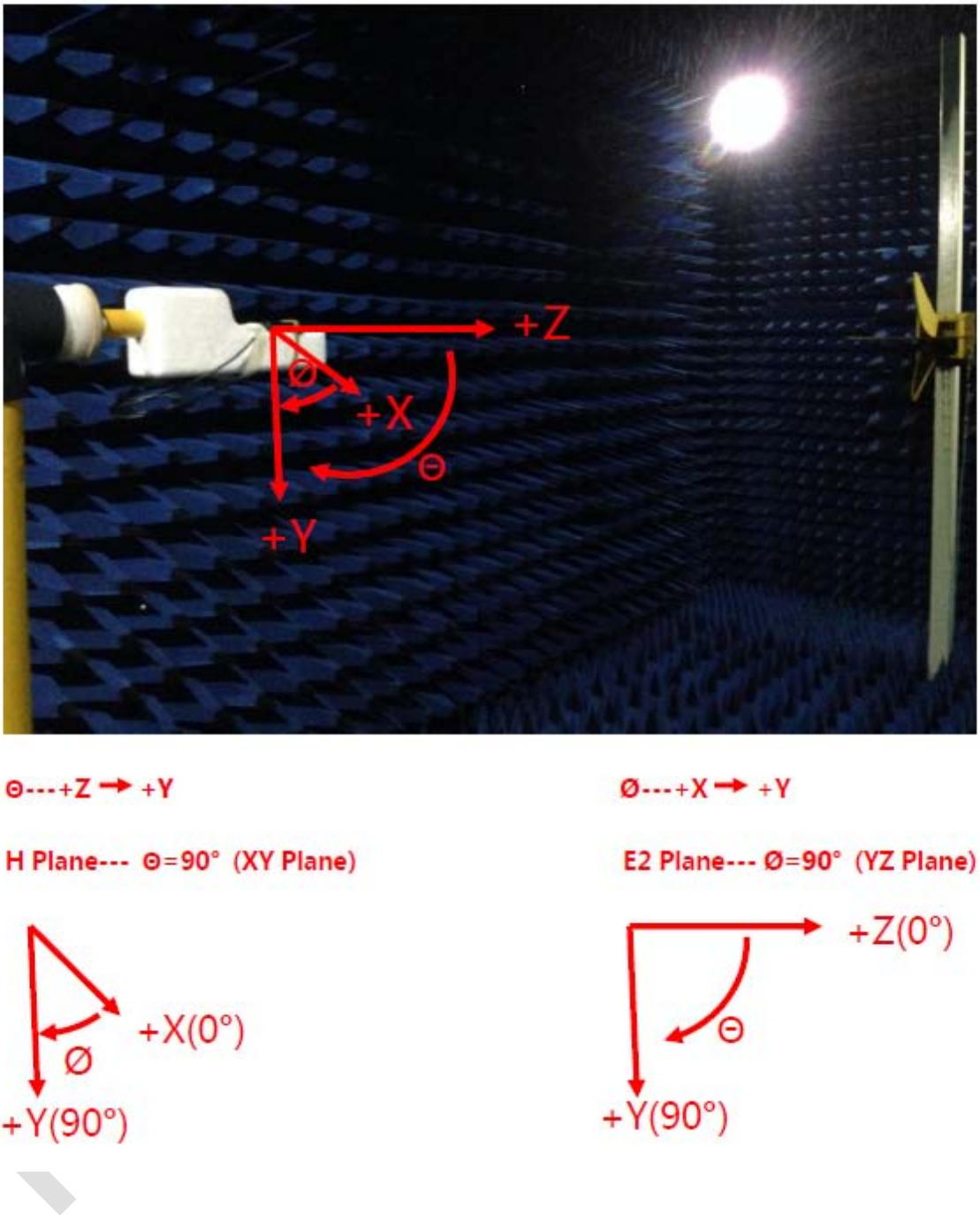


Figure 32 V2X Antenna Test Chamber description

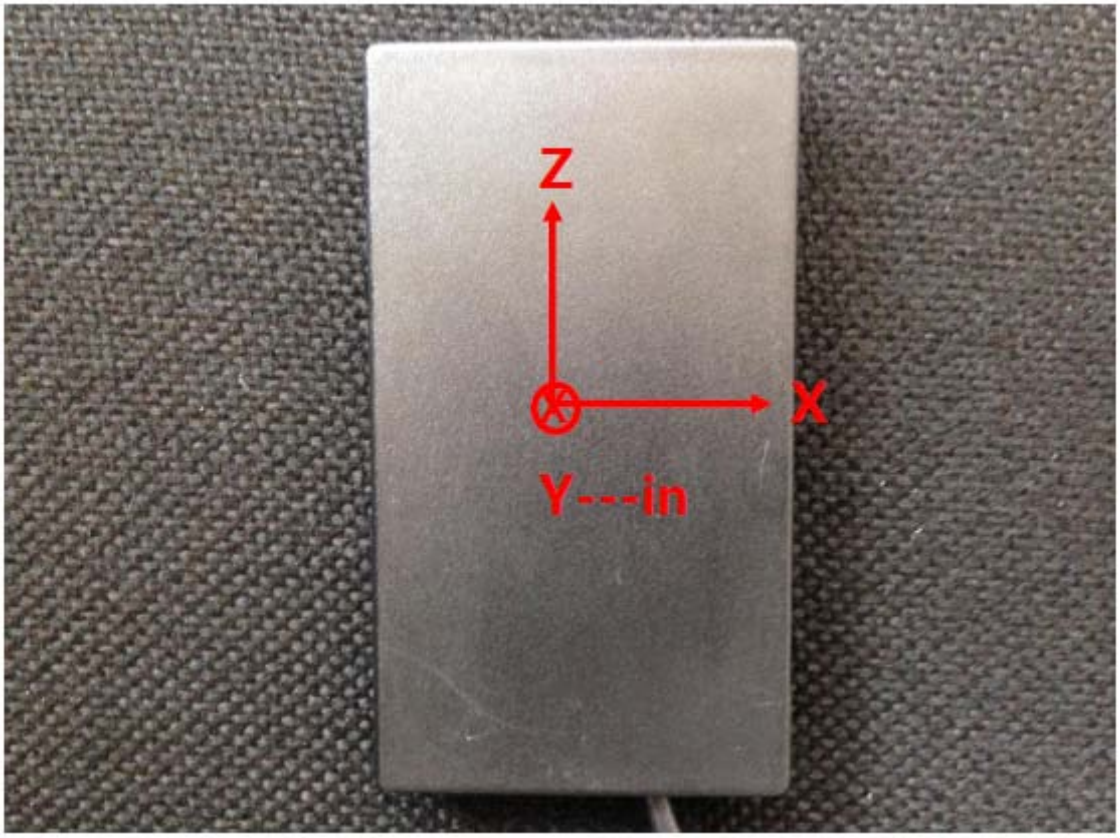
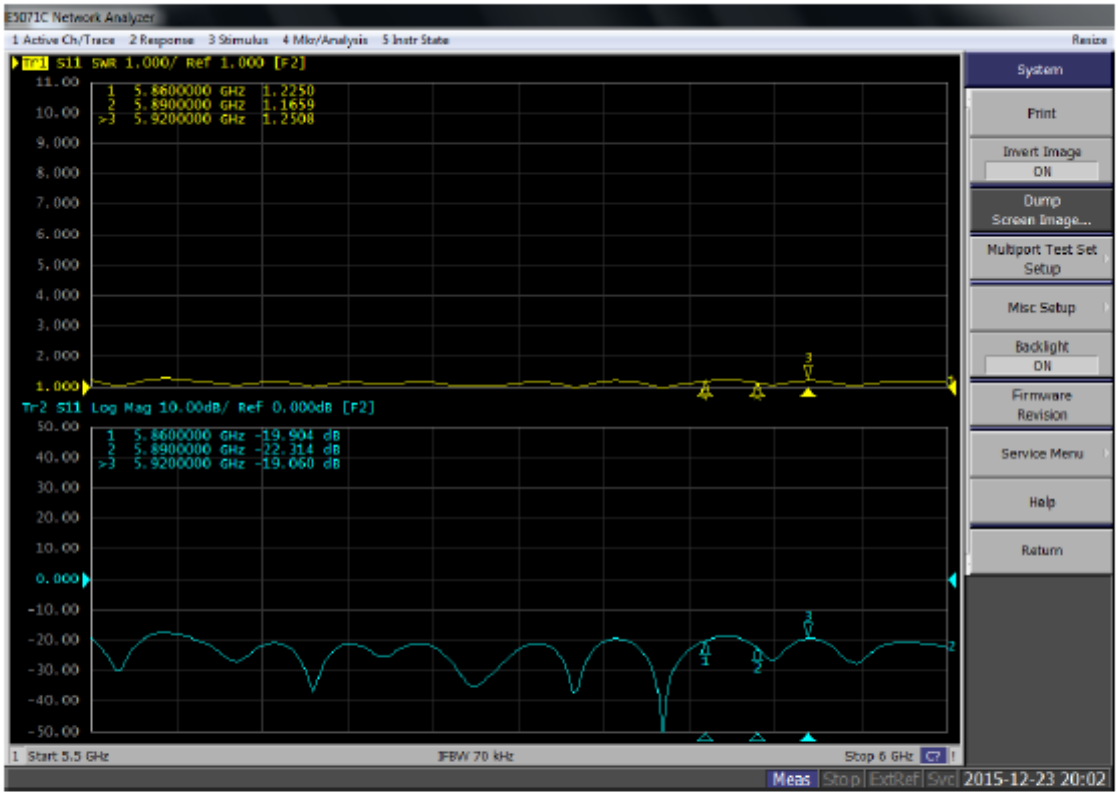


Figure 33 V2X Antennal test axis definition description

VSWR (S11) :



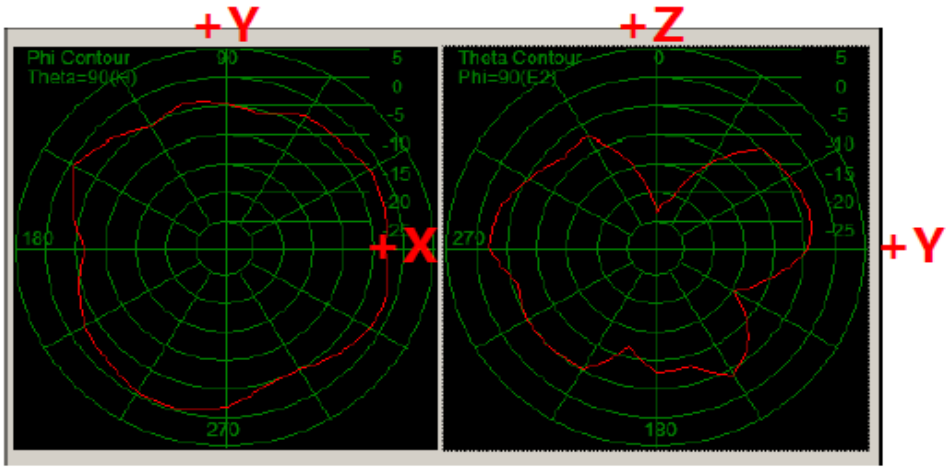
Data:(with cable loss)

Freq.（MHZ）	5860	5890	5920
VSWR	1.22	1.16	1.25
Gain（dBi）	0.5	0.5	0.6
Eff.	34%	33%	36%

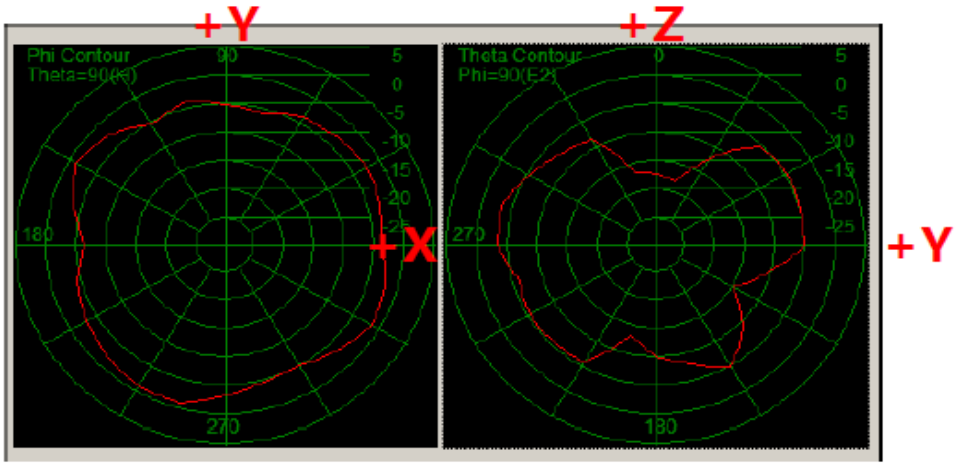
Figure 34 V2X Antennal VSWR test character

2D Radiation Pattern

X-Y Plane 5860MHz Y-Z Plane



X-Y Plane 5890MHz Y-Z Plane



X-Y Plane 5920MHz Y-Z Plane

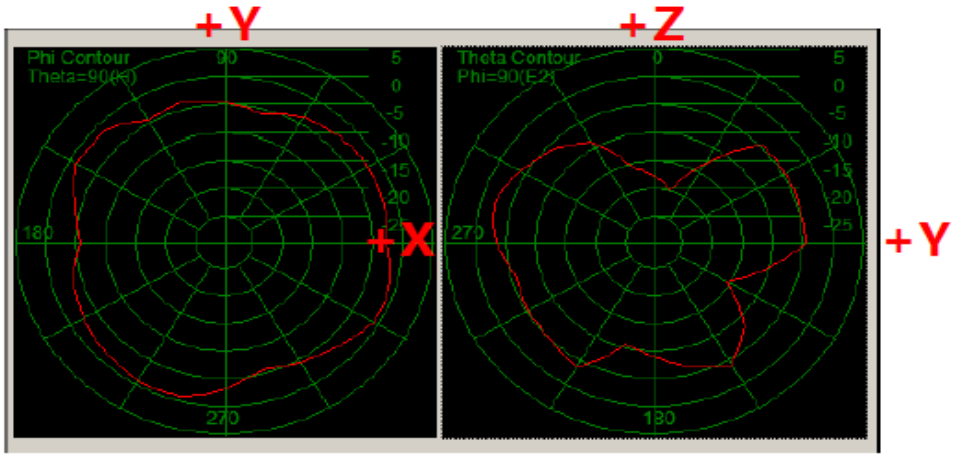


Figure 35 V2X Antennal 2D radiation pattern

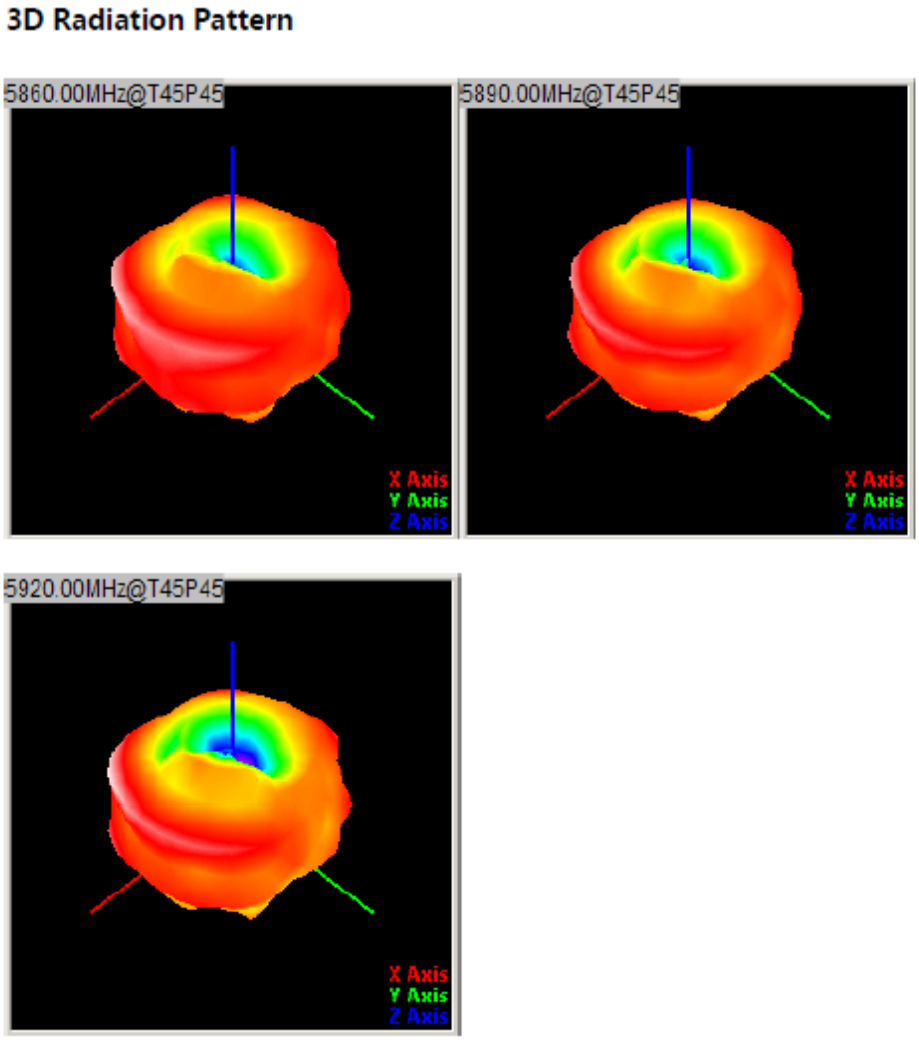


Figure 36 V2X Antennal 3D radiation pattern

This V2X antenna connects with the SMA connector labeled CH0, CH1 in the case by default while delivery.

Cable Length: 2m

Figure 37 Image of V2X Antenna1 from Bottom view

Figure 38 Image of V2X Antenna1 from Top view

7.5 V2X Antenna (Rod Type)

7.5.1 Specification

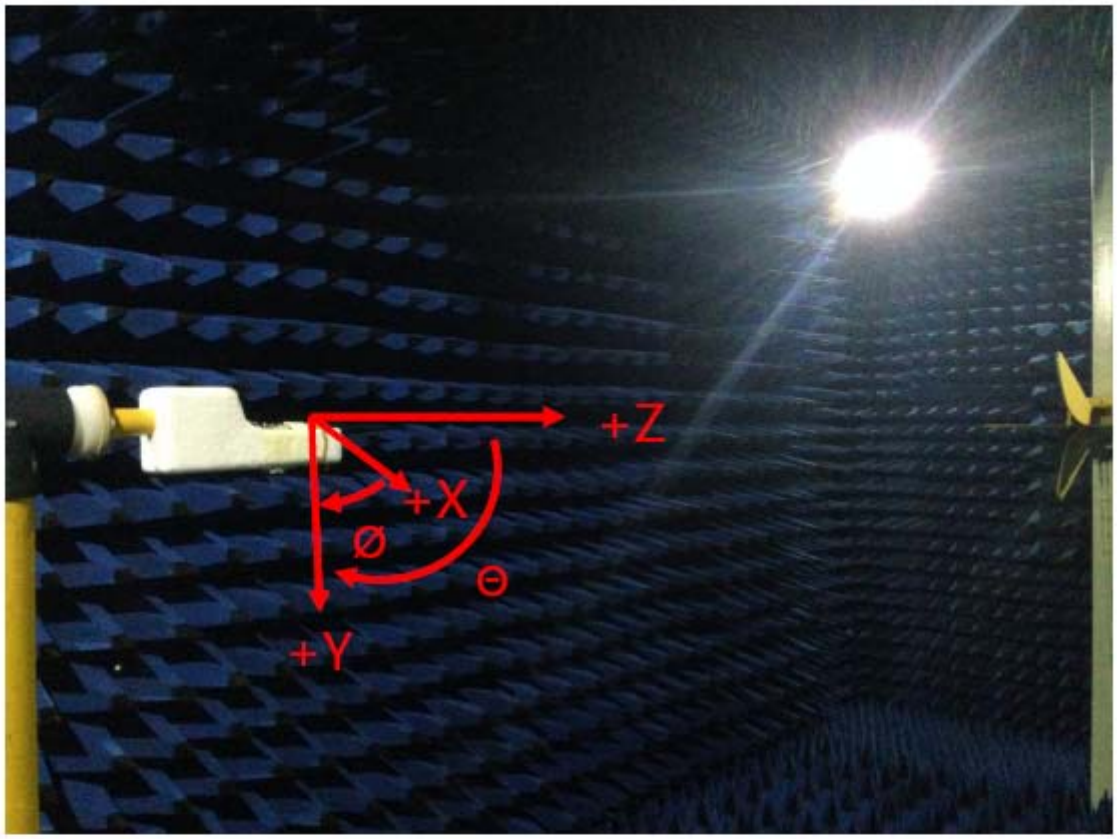
About 5.9GHz V2X antenna specification, please refer to the following data:

Table 29 Antenna Specification for V2X (Rod Type)

Item	Specification
Part Number	6073F00006
Manufacturer	Signal Plus
Frequency Range	5860~ 5920MHz
Polarization	Vertical
Impedance	50 Ohm
VSWR	2.0 Max
Gain	5.0dBi
Cable Loss	0.5dB (with SMA)
Radiation	Omni Directional
Color	Black
Connector	SMA Plug Standard
Material	nickel
Plating treatment	nickel plating
Male/Female	Male
Operating Temp	-.20℃ ~ +65℃
Storage Temp	-.30℃ ~ +75℃

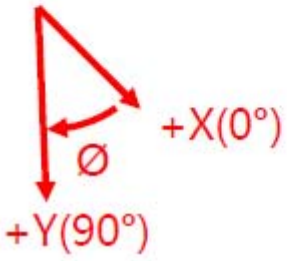
This Antenna's radiation pattern is described as below figures.

3D Chamber:



Θ---+Z → +Y

H Plane--- Θ=90° (XY Plane)



Ø---+X → +Y

E2 Plane--- Ø=90° (YZ Plane)

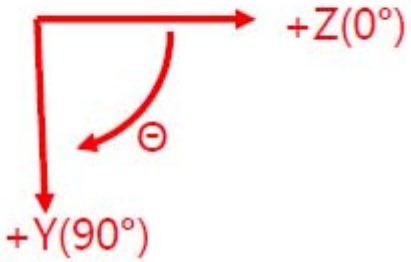


Figure 39 V2X Antenna2 Test Chamber description

Antenna :

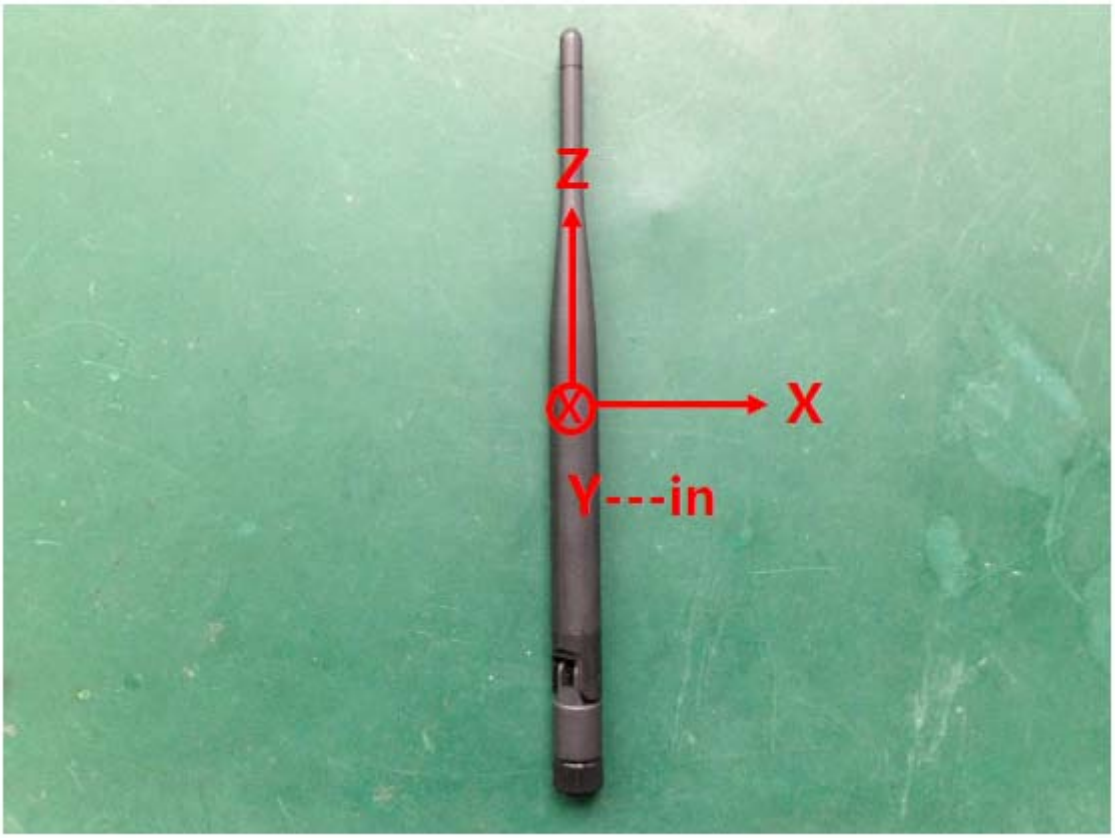
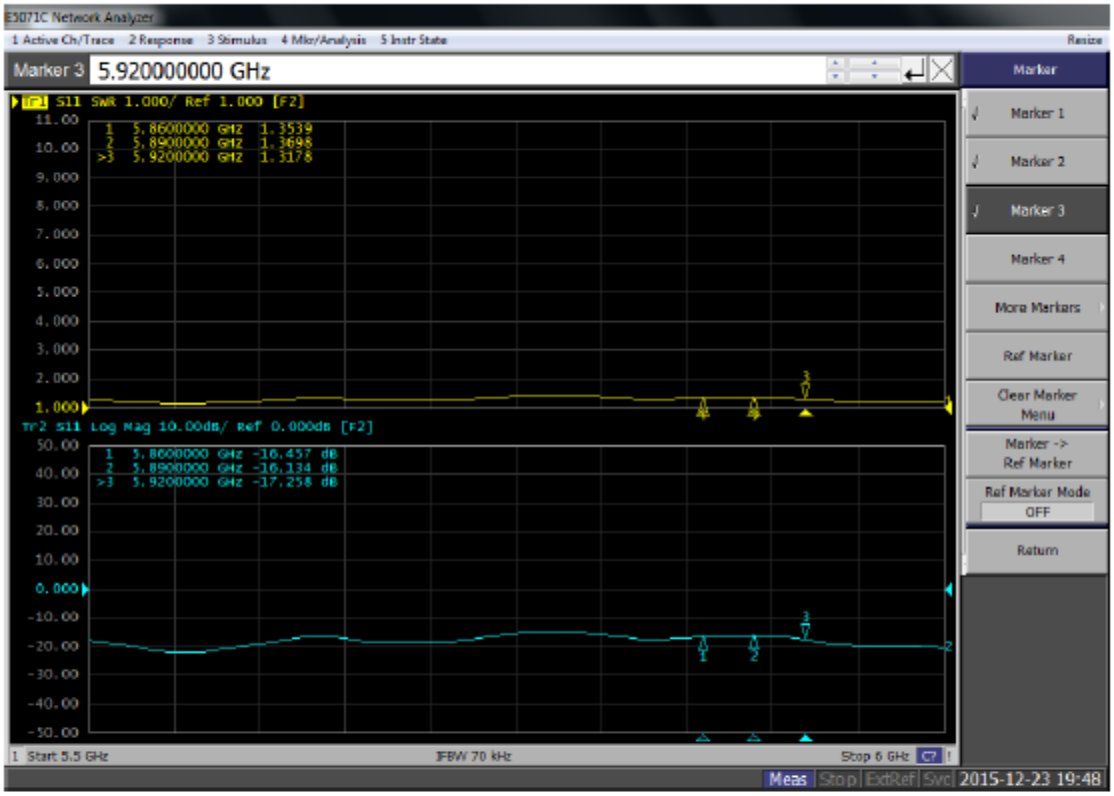


Figure 40 V2X Antenna2 test axis definition description

VSWR (S11) :



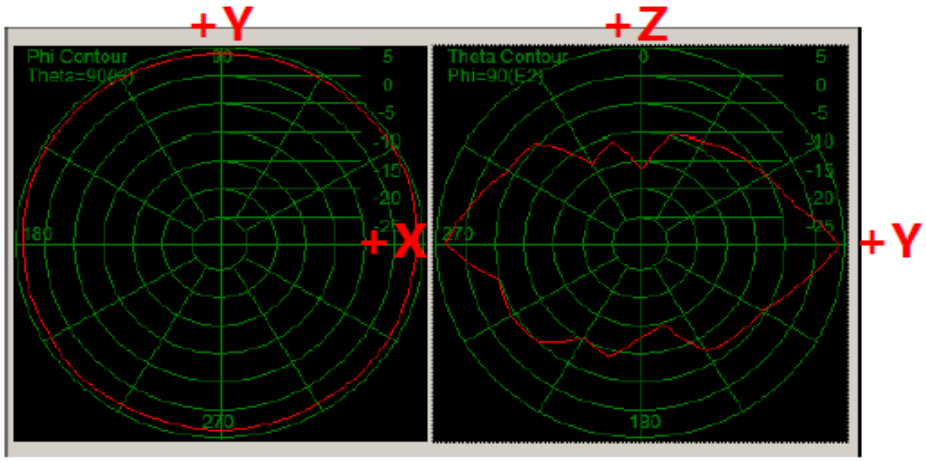
Data:(with cable loss)

Freq.（MHZ）	5860	5890	5920
VSWR	1.35	1.36	1.31
Gain（dBi）	4.6	4.6	5.1
Eff.	62%	62%	67%

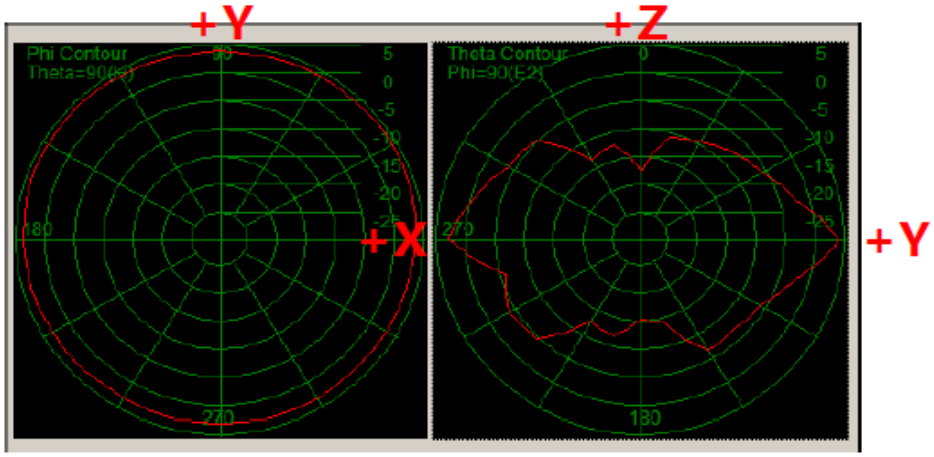
Figure 41 V2X Antenna2 VSWR test character

2D Radiation Pattern

X-Y Plane 5860MHz Y-Z Plane



X-Y Plane 5890MHz Y-Z Plane



X-Y Plane 5920MHz Y-Z Plane

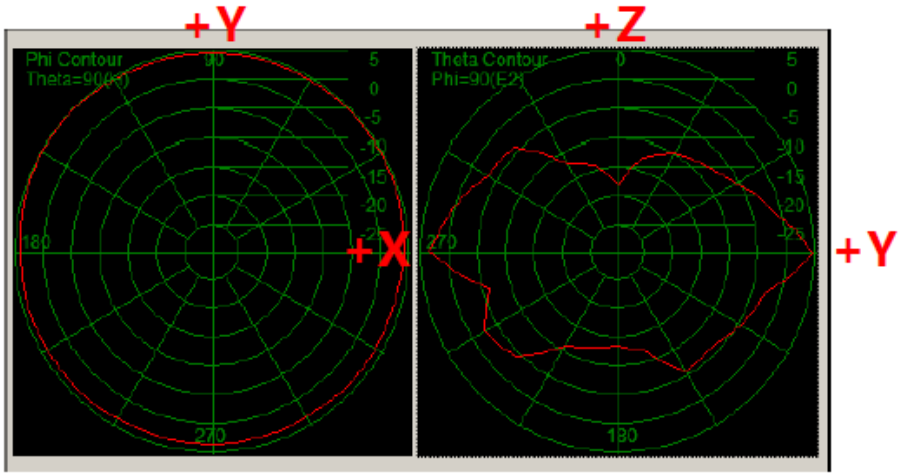


Figure 42 V2X Antenna2 2D radiation pattern

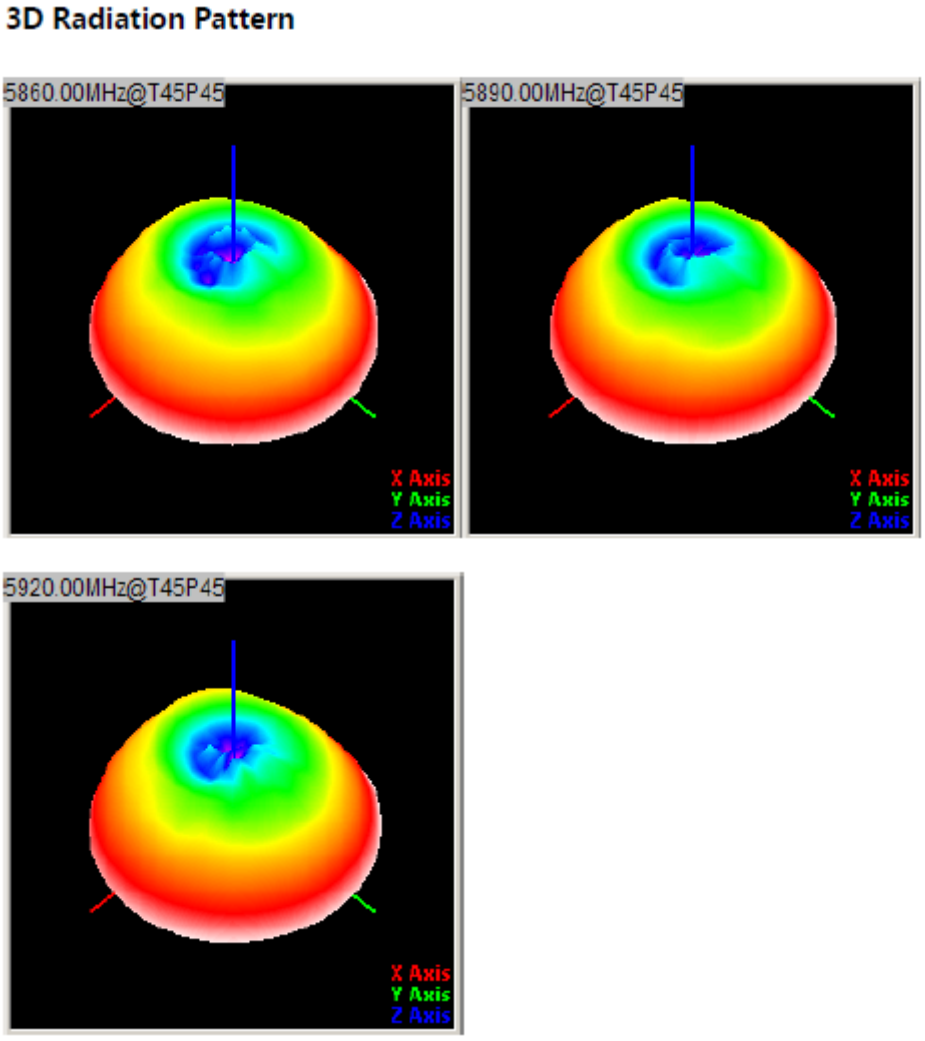


Figure 43 V2X Antenna2 3D radiation pattern

Figure 44 Image of V2X Antenna2 (SMA rotate 90 degree)

Figure 45 Image of V2X Antenna2 (SMA rotate 0 degree)

7.6 RF Cable

7.6.1 Specification

About RF Cable specification, please refer to the following data:

Table 30 RF Cable Specification for GPS module & RF Board

Item	Specification
Frequency Range	0~ 6GHz
Impedance	50 Ohm
VSWR	1.4 Max
Cable Loss	1.3dB Max
Cable length	(1)13~15cm for V2X (2)20cm for GPS
Cable Type	U.FL-LP-088
Connector	SMA
Material	Copper
Plating treatment	Gold plating
Male/Female	Female
Operating Temp	-.40℃ ~ +90℃
Storage Temp	-.40℃ ~ +70℃

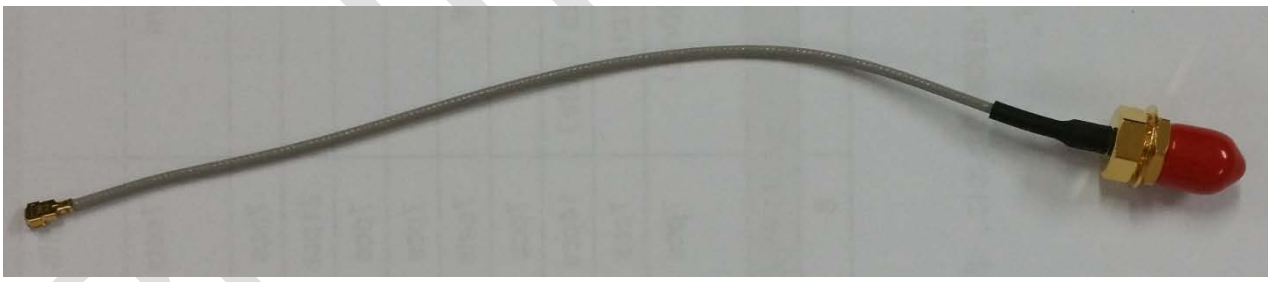


Figure 46 RF Cable

7.7 JTAG Debug Board with FPC Cable

7.7.1 Specifications

Connecter	Function	Debugger	Manufacturer
CN1	CPU JTAG	ARM JTAG ICE Debugger	ARM JTAG ICE Vendor
CN4	CPU JTAG2(SH-4A)	E10A	Renesas (Japan)
CN3	MCU JTAG	E1	Renesas (Japan)

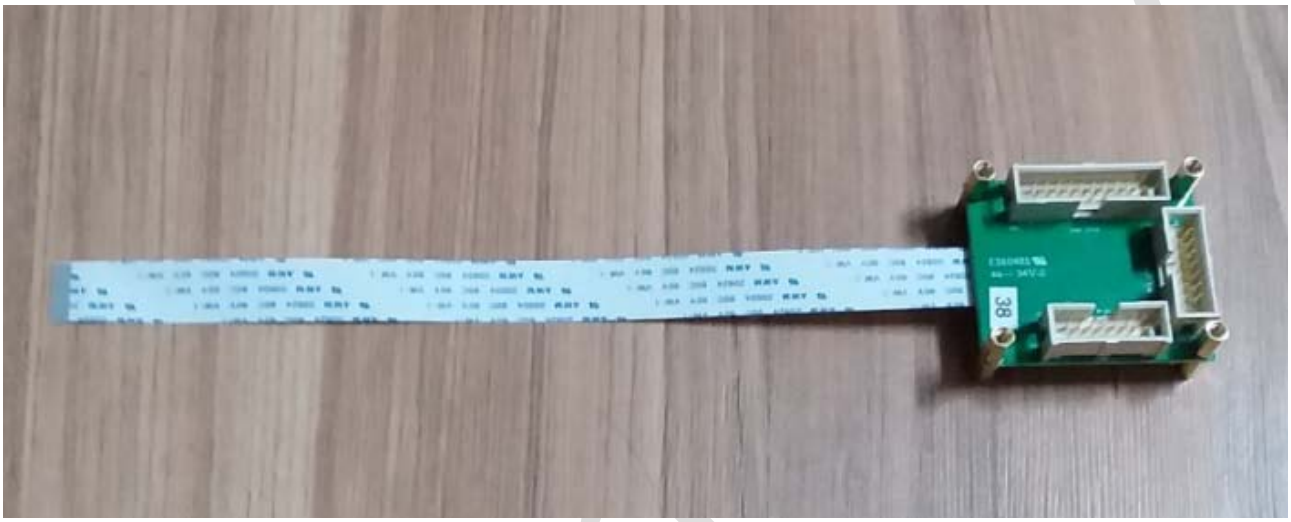


Figure 47 JTAG Debug Board with FPC Cable for W2H & RH850 MCU

7.7.2 Block Structure

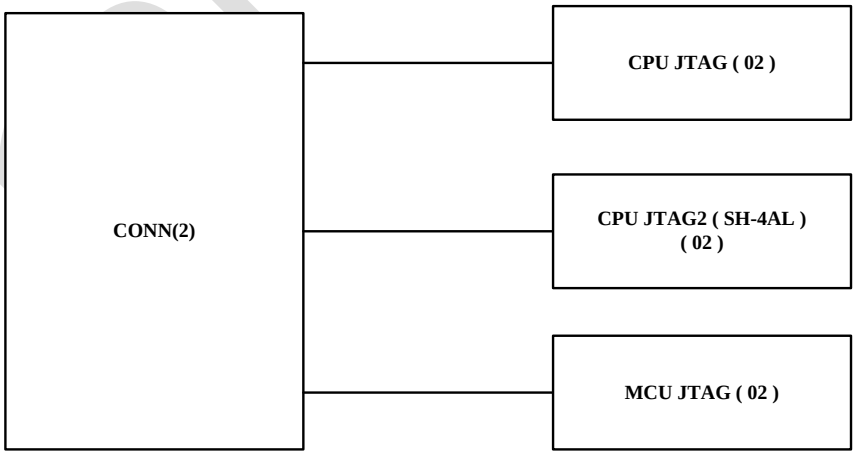


Figure 48 JTAG Debug Board block structure

7.7.3 Block Diagram

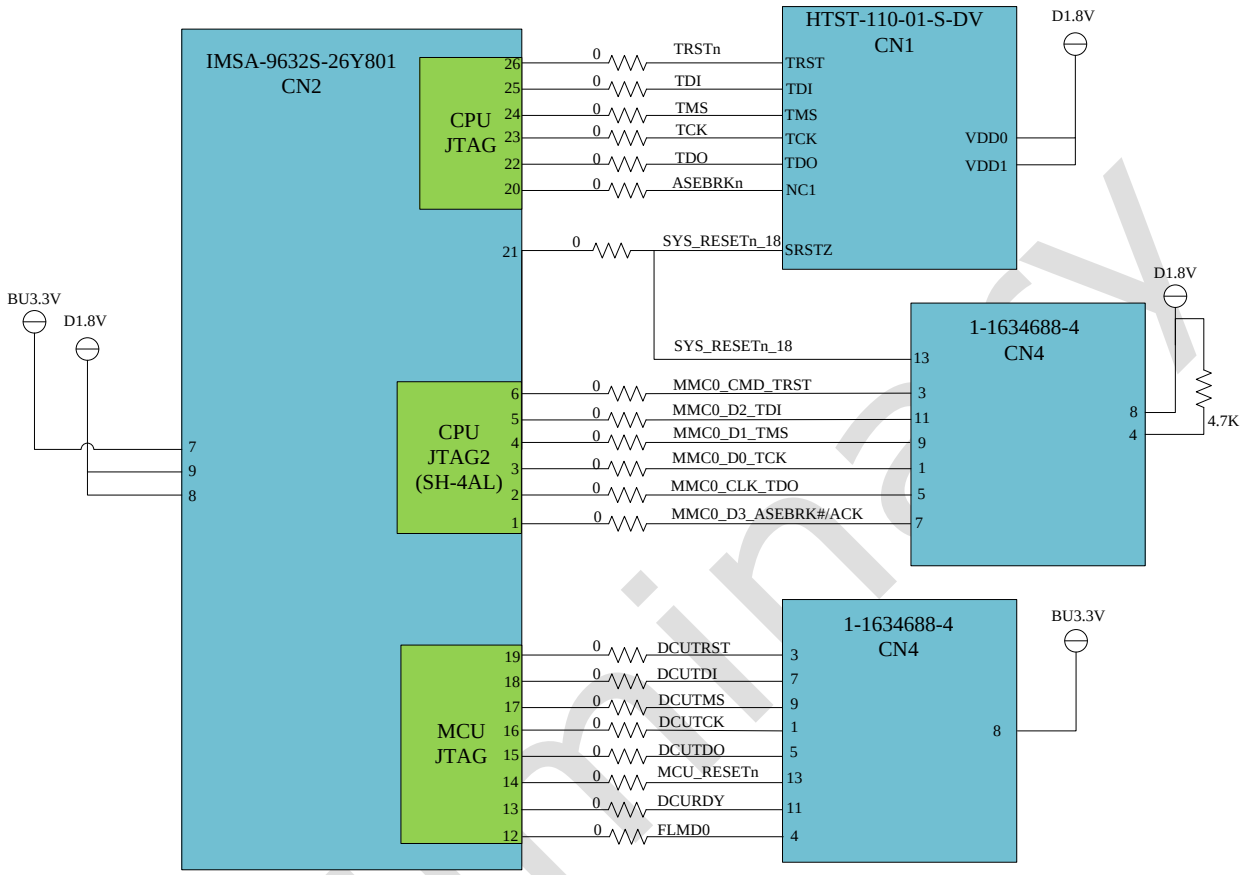


Figure 49 Block Diagram of the JTAG Debug Board

7.8 V2X Connection board

This sub board can be connected to CN9 or CN12 to extend SD socket IF.

Top side view:

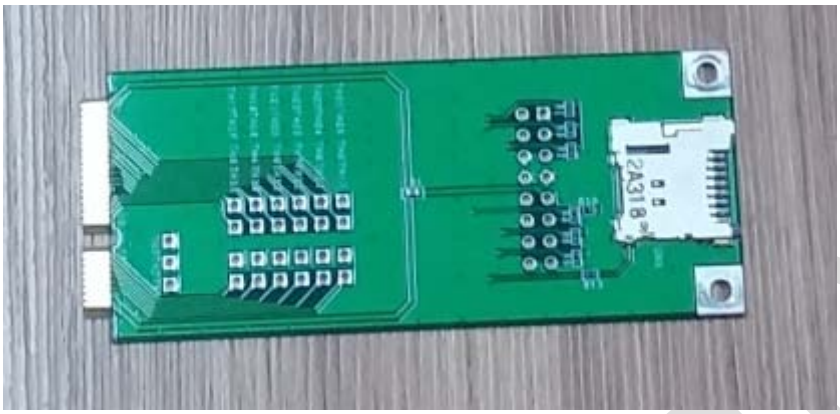


Figure 50 Top side view of V2X Connection board

Bottom side view:

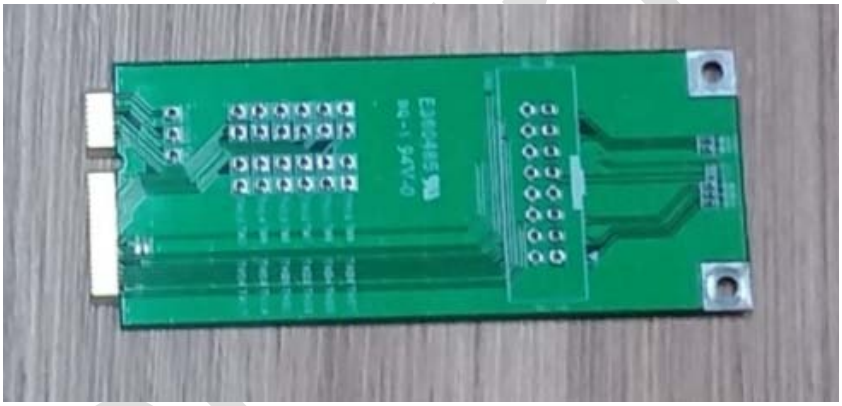


Figure 51 Bottom side view of V2X Connection board

7.8.1 Board Structure

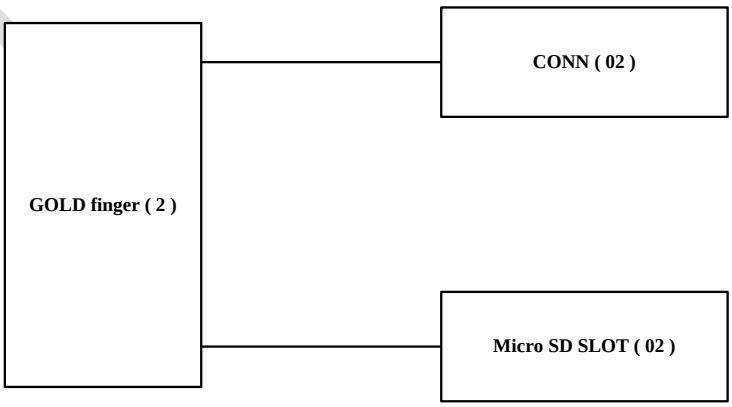


Figure 52 Block structure of V2X Connection board

7.8.2 Block Diagram

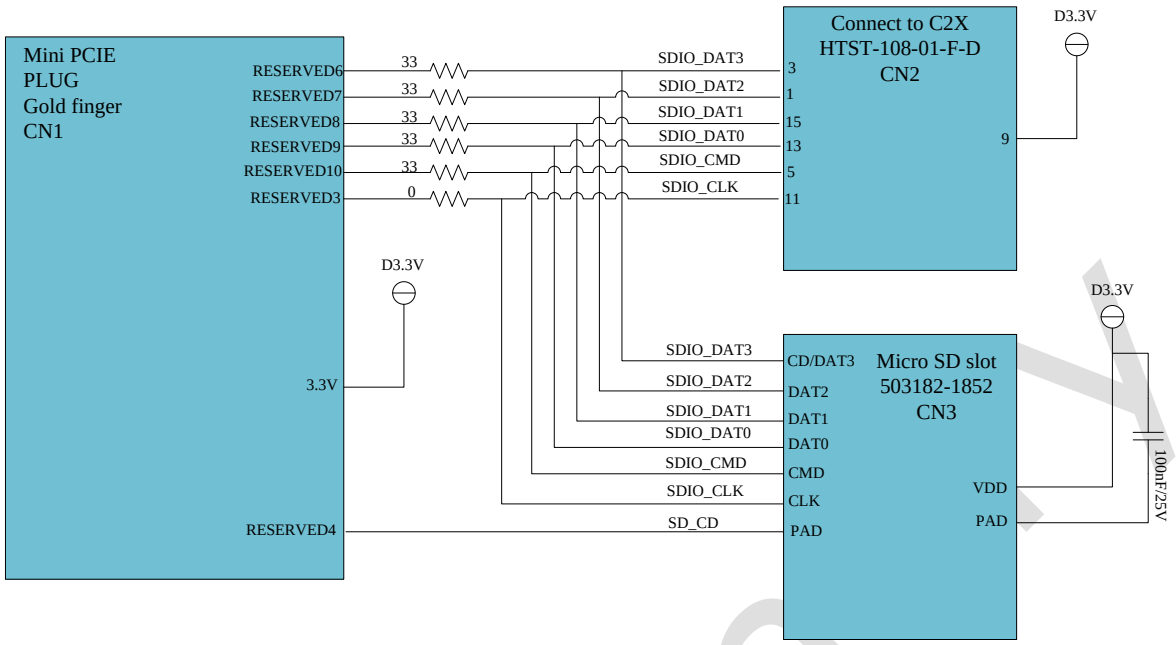
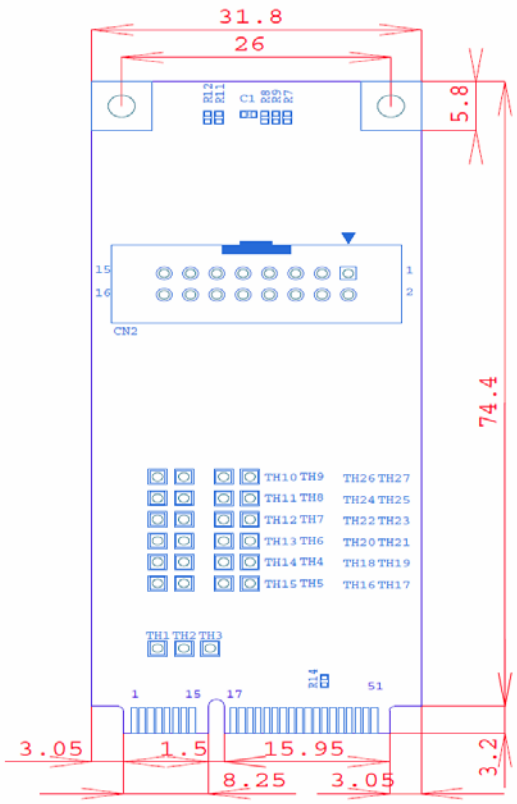


Figure 53 Block Diagram of the V2X Connection board

7.8.3 Block dimension



7.9 Sub board Tortuga wireless module board dimension

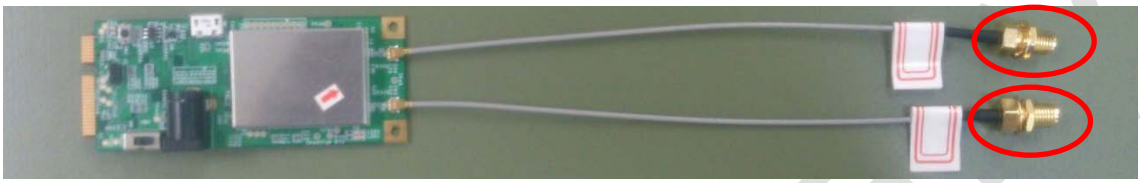
The Tethys board can connect to Tortuga wireless module through MINI PCIE interface transfer board, and the transfer sub board dimension is shown as below(Unit: mm): Please connect this board to CN9, CN12.

7.9.1 RF characteristic

*1 typical operating condition (Just informative, not guaranteed.):

*1 HW = Tortuga7, Ta = 25°C, VDD3V3 =3.3V, VDD1V2 =1.2V, VDD5V0=5.0V

*1 Measurement point is circled in red in the figure below



(1) Receive characteristic

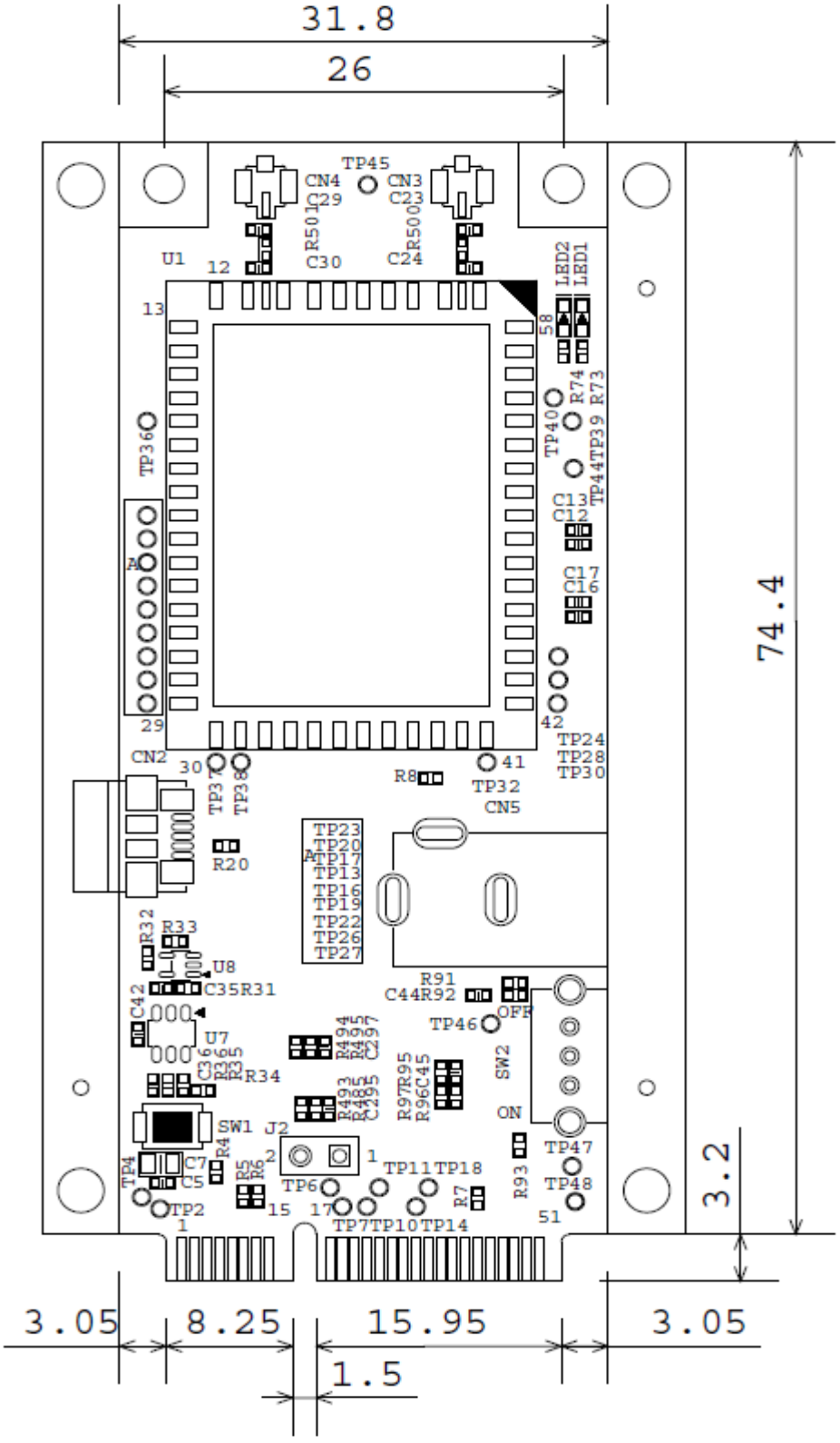
	Min	Typ	Max	Unit	Condition
Frequency range	5850		5925	[MHz]	
Input VSWR		2.0		-	5890MHz
Minimum Sensitivity (Diversity off)		-94		[dBm]	Data rate = 3Mbps
		-93		[dBm]	Data rate = 6Mbps
		-87		[dBm]	Data rate = 12Mbps
		-77		[dBm]	Data rate = 27Mbps
Minimum Sensitivity (Diversity on)		-94		[dBm]	Data rate = 3Mbps
		-94		[dBm]	Data rate = 6Mbps
		-87		[dBm]	Data rate = 12Mbps
		-80		[dBm]	Data rate = 27Mbps
Maximum Input Level (Diversity off)		-20		[dBm]	Data rate = 27Mbps
Maximum Input Level (Diversity on)		-20		[dBm]	Data rate = 27Mbps
Adjacent channel rejection (Diversity off)		30		[dB]	Data rate = 3Mbps
		29		[dB]	Data rate = 6Mbps
		28		[dB]	Data rate = 12Mbps
		18		[dB]	Data rate = 27Mbps
Nonadjacent Adjacent channel rejection (Diversity off)		44		[dB]	Data rate = 3Mbps
		41		[dB]	Data rate = 6Mbps
		36		[dB]	Data rate = 12Mbps
		27		[dB]	Data rate = 27Mbps

(2) Transmit characteristic

Ta = 25°C, VDD3V3 =3.3V, VDD1V2 =1.2V, VDD5V0=5.0V

	Min	Typ	Max	Unit	Condition
Frequency range	5850		5925	[MHz]	
Output VSWR		2.0			5890MHz
Maximum out put Power(ANT_B)		24		[dBm]	5890MHz
Maximum out put Power(ANT_A)		-8		[dBm]	5890MHz
Minimum out put Power(ANT_B)		-7		[dBm]	5890MHz
Minimum out put Power(ANT_A)		-35		[dBm]	5890MHz
Output Power control range		30		[dB]	5890MHz
Power control step		0.5		[dB]	
Relative constellation error		-28		[dB]	Data rate = 3Mbps
		-28			Data rate = 6Mbps
		-28			Data rate = 12Mbps
		-28			Data rate = 27Mbps
Spectrum Mask (in band)		-31		[dBr/100 KHz] @5890 MHz	4.5MHz<f<5.0MHz offset Pout = 24dBm
		-33			5.0MHz<f<5.5MHz offset Pout =24dBm
		-36			5.5MHz<f<10.0MHz offset ±5.5MHz Pout= 24dBm
		-54			10.0MHz<f<15.0MHz offset Pout=24dBm

7.9.2 Board Dimension



Top Side

Bottom Side

7.10 Side cover option of case

AL Case includes the following 2 sets of side cover option which will be used depending on the sub board type, which is inserted in CN8 or CN11 connector on Tethys board.

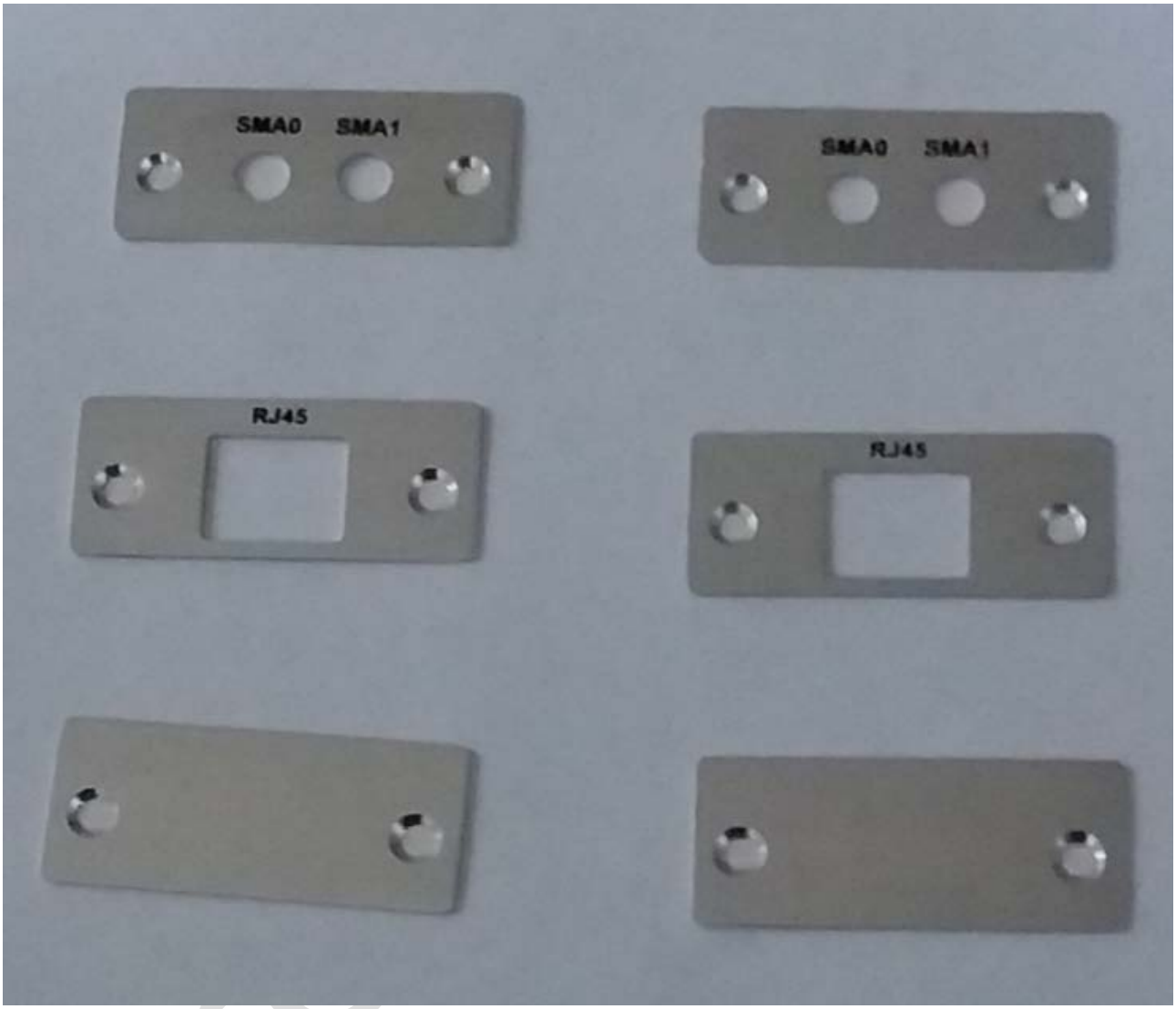


Figure 54 Side cover option of case

7.11 Acronyms and Abbreviations

Appendix 1 Acronyms and Abbreviations

Acronym/Abbreviation	Description
AC	Alternating Current
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DDR	Double Data Rate
eMMC	Embedded Multi Media Card
ESD	Electronic Static Discharge
FPC	Flexible Printed Circuit
JTAG	Joint Test Action Group
GMII	Gigabit Media Independent Interface
GPS	Global Position System
GPIO	General-Purpose I/O
HSM	Hierarchical Storage Management
HSCIF	High-speed Serial Communication Interface with FIFO
I2C	Inter－Integrated Circuit
LED	Light-Emitting Diode
LVTTL	Low-Voltage Transistor-Transistor Logic
MCU	Microprogrammed Control Unit
MMC	Multi Media Card
PCIE	Peripheral Component Interface Express
QSPI	Queued Serial Peripheral Interface
RAM	Random Access Memory
ROM	Read Only Memory
SCIF	Serial Communication Interface with FIFO
SDHI	SD Host Interface
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SOC	System On Chip
SPI	Serial Peripheral Interface
SSI	Serial Sound Interface
UART	Universal Asynchronous Receiver Transmitter
USB 2.0	Universal Serial Bus2.0

VCC	Volt Current Condenser
VSWR	Voltage Standing Wave Ratio
PO	Power output

8 Regulatory Warning Statements

Federal Communication Commission Interference Statement:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1)This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

NOTE: The antenna which installed within the module cann't be changed. Any antenna replacement is class II change required. The device is restricted to indoor environment, the antenna cann't be extened in other ways. The height of the antenna is prohibited to be under 8 meters.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate this equipment.

This transmitter must not be co located or operating in conjunction with any other antenna or transmitter.
For operation within the 5860MHz~5920Mhz frequency range, it is restricted to indoor environment. This device meets all the other requirements specified in Part 90 of the FCC Rules

Radiation Exposure Statement:

The product comply with the FCC portable RF exposure limit set forth for an uncontrolled environment and are safe for intended operation as described in this manual. The further RF exposure reduction can be achieved if the product can be kept as far as possible from the user body or set the device to lower output power if such function is available.

Integrator Instructions:

EUT name: Tethys

FCC ID: 2AHMN-Tethys

Model name: RTK00V2XRC7746SAS

Additional Regulatory Conformance Testing and/or Submissions

Required by the Integrator:

The OEM integrator is responsible for additional system-level EMI/EMC and Product Safety testing and certification that applies in the U.S. and other countries to the host system containing the Module. This includes, but is not limited to, Federal

Communications Commission ("FCC") Part 15 Class B Digital Emissions, and ETSI EN 301 489-17.

These system-level EMC tests are to be done with the Module installed and included in the scope of the submission.

European Community R&TTE

Notice: Observe the national local regulations in the location where the device is to beused. This device may be restricted for use in some or all member states of the European Union (EU).

The device complies with RF specifications when the device used at least 20cm from human body.

The users has to turn off the 5.9GHz WiFi in outdoor environment.

Sound pressure warning:

Use careful with the earphone maybe possible excessive sound pressure from earphones and headphones can cause hearing loss

Caution:

Risk of electric Shock, dry location use only

Adapter description:

Adapter shall be installed near the equlpment and shall be easlly accessible.

The plug considered as disconnect device of adapter.

USB description:

The product shall only be connected to a USB Interface of version USB2.0

Website and Support

Renesas Electronics Website

http://www.renesas.com/

Inquiries

http://www.renesas.com/contact/

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.0	Nov 29 2016	all	New Created

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