User's Manual

Under Development Confidential

GAC-B-17-0004

RTK00V2X720MTORS7J

User's Manual: Hardware

— Preliminary —

Renesas Electronics
www.renesas.com

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Introduction

RTK00V2X720MTORS7J(Tortuga) is an evaluation board for RTK00V2X7200MPIN7J (V2X wireless module). Tortuga can be used as standalone without the need of Host board, and be evaluated RF performance of V2X wireless module. Tortuga also be used in conjunction with the Host board.

V2X wireless module has optimized function to realize IEEE802.11p PHY layer function. This product conforms not only to 802.11p standard but 1609.4 and ETSI standard. This module provides cost effective, low power and small form factor solution for communication unit manufacture.

Overview

Tortuga is an evaluation board for V2X wireless module(including Renesas' ASSP and suitable component). V2X wireless module has optimized function to realize ETSI EN 302 571/ ETSI EN 302 663 PHY/MAC layer function. This product provides cost effective, low power and small form factor solution to communication unit manufacture.
V2X wireless module includes radio transceiver, PA, LNA , antenna switch, Filters and peripherals.

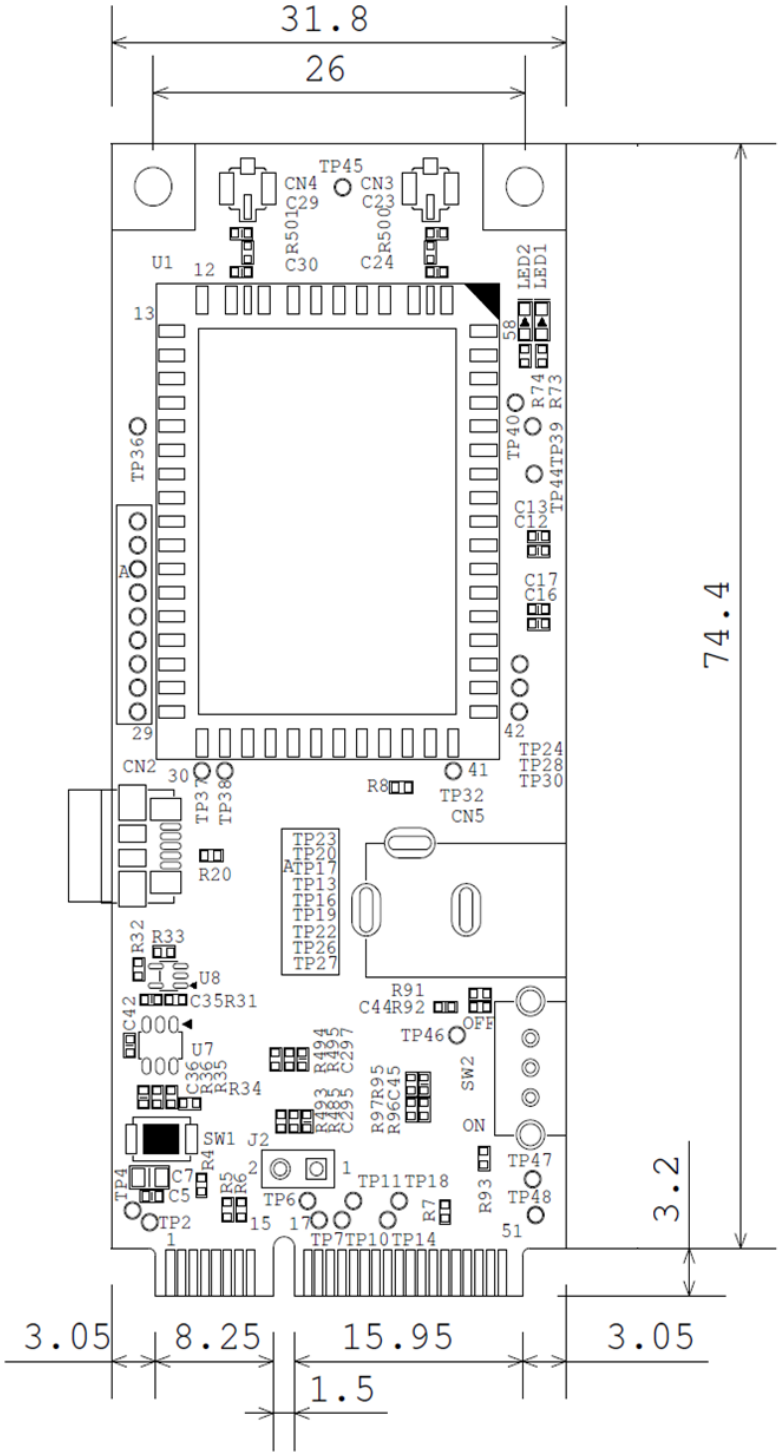
Feature
- Support Standard: ETSI EN 302 571/ ETSI EN 302 663 / IEEE802.11p™ -2010<15.July.2010> PHY/MAC protocol with Firmware
- Operational Frequency band: 5.9GHz
- Using 32bit CPU core, Operating Frequency: up to 160MHz
- Internal memory: RAM/128kByte, ROM/32kByte, EEPROM/512Byte
- Mini PCIE Connector
- SDIO interface for host CPU
- UART interfaces
- USB interfaces
- Integrate Function for ETSI EN 302 571/ ETSI EN 302 663
  OFDM Modulator/ Demodulator with Maximum Ratio Converting diversity
  MAC hardware accelerator
- Power Supply: 12V from AC Adapter or 5.0V from Host board
- Peak Power Consumption (at 12 V)
  TYP:
  - Listen mode : TBD (diversity on)/TBD(diversity off)
  - Rx mode : TBD (diversity on)/TBD(diversity off)
  - Tx mode : TBD (@24dBm)
- Operating Temperature
  Ta = -40 to +85 degree

Contents

1. Dimension and Layout

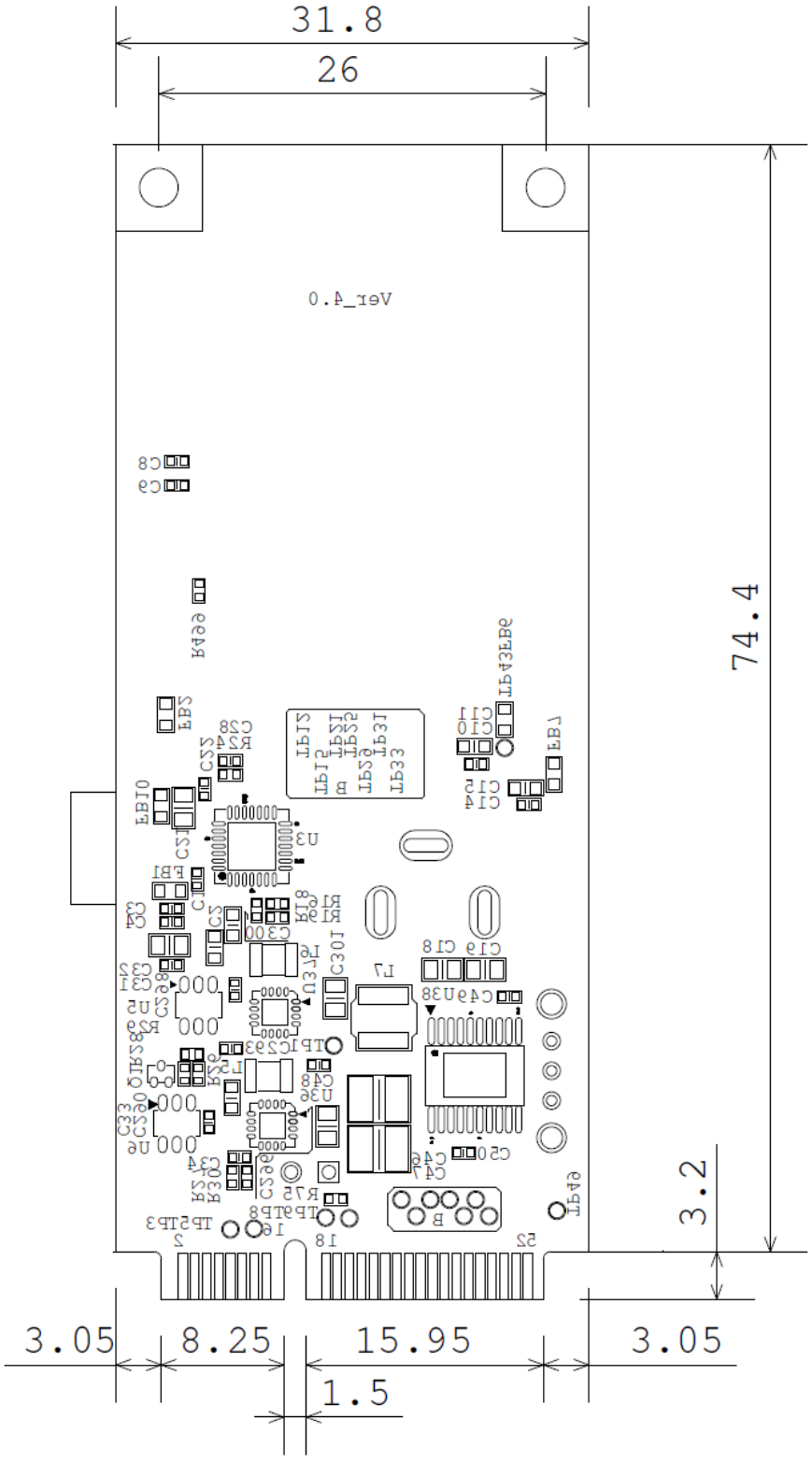
1.1 Board layout information

Figure1. Board top view information



Unit: mm

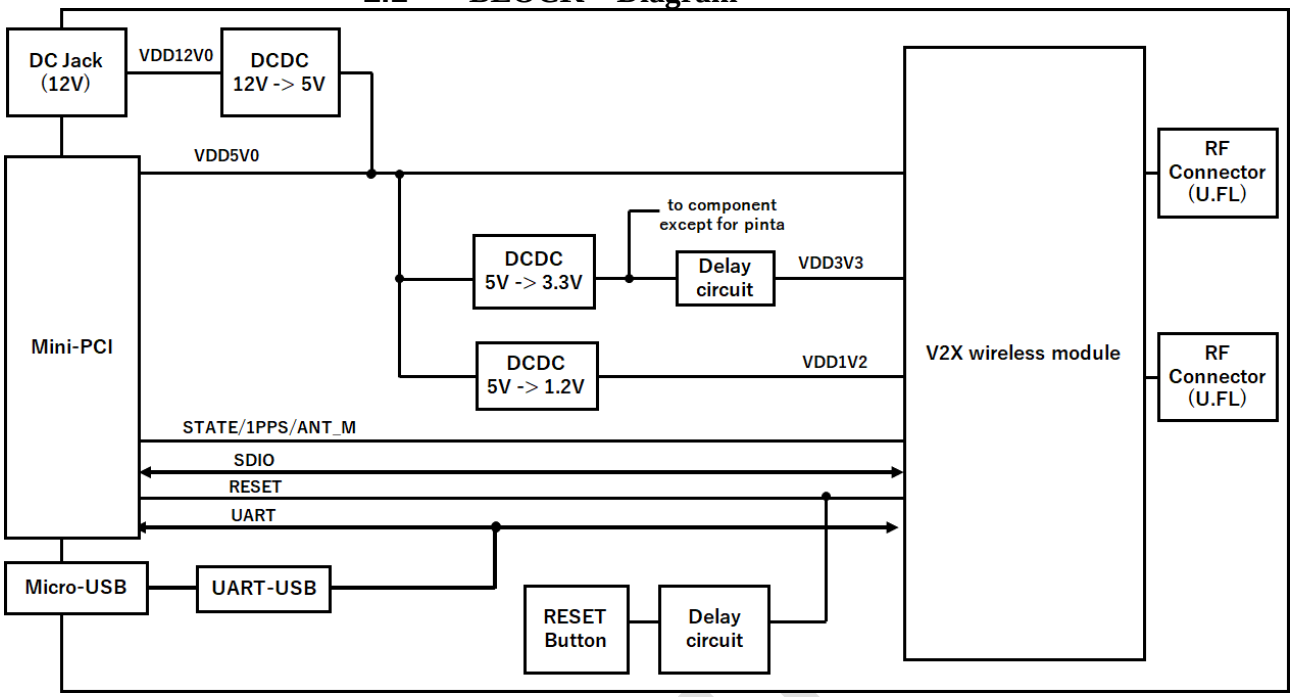
Figure2. Board bottom view information

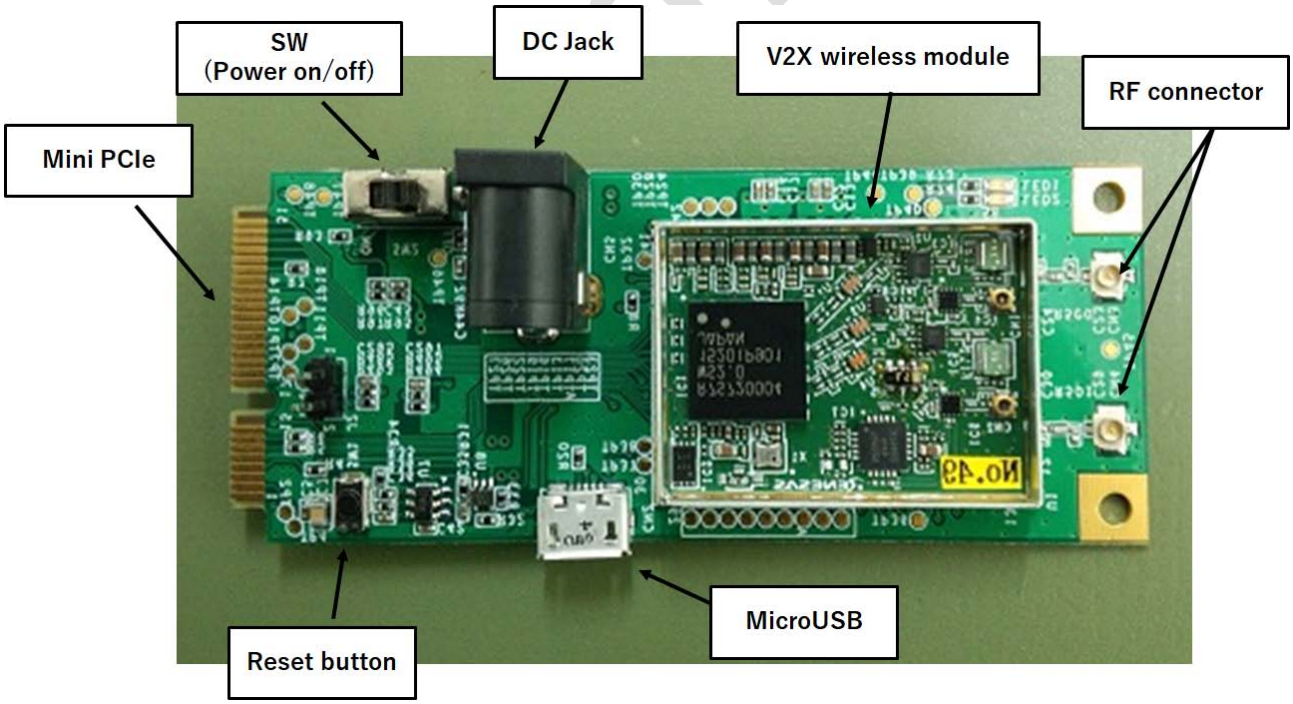


Unit: mm

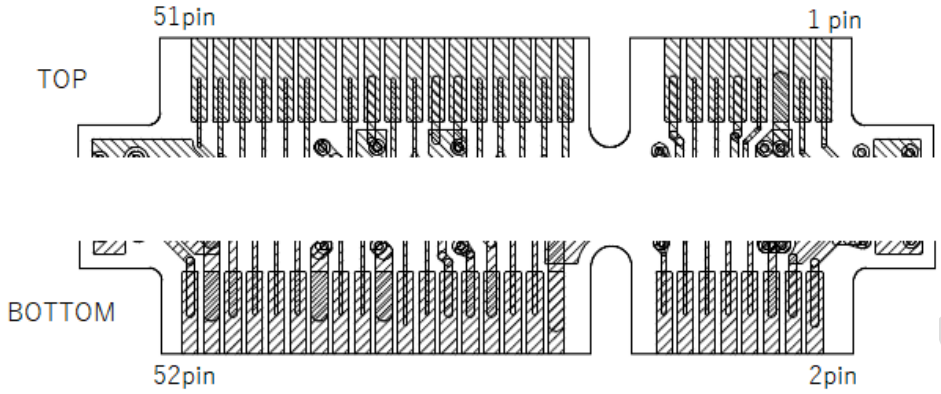
2. Board description

2.1 BLOCK Diagram





2.2 Mini PCIE pin information



Pin	Pin Name	I/O	Functional	Description
1	RESERVE	I/O	-	No connection(only connected to test pin)
2	RESERVE	I/O	-	No connection
3	RESERVE	I/O	-	No connection(only connected to test pin)
4	GND	-	GND	GND
5	5.0V	-	Voltage Supply	5V voltage supply
6	5.0V	-	Voltage Supply	5V voltage supply
7	RESET	I	CMOS Schmitt Trigger Input (with Pull-Up)	System reset input (Low Active)
8	1PPS	I	CMOS Schmitt Trigger I (with Pull-Down)	If you don't use, select open.
9	GND	-	GND	GND
10	RESERVE	I/O	-	No connection(only connected to test pin)
11	UART0_TXD	O	CMOS Output	UART0 Tx signal [TXD]
12	ANT_M	I	CMOS Schmitt Trigger I (with Pull-Up)	RX Diversity Enable selects. - High : Diversity - Low : Single_ANT B If you don't use, select open.
13	UART0_RXD	I	CMOS Schmitt Trigger Input	UART0 Rx signal [RXD]
14	RESERVE	I/O	-	No connection(only connected to test pin)
15	GND	-	GND	GND
16	STATE	O	CMOS Output	Status indication signal
17	RESERVE	I/O	-	No connection(only connected to test pin)
18	GND	-	GND	GND
19	RESERVE	I/O	-	No connection(only connected to test pin)
20	RESERVE	I/O	-	No connection(only connected to test pin)
21	GND	-	GND	GND
22	RESERVE	I/O	-	No connection(only connected to test pin)
23	RESERVE	I/O	-	No connection(only connected to test pin)
24	5.0V	-	Voltage Supply	5V voltage supply
25	RESERVE	I/O	-	No connection(only connected to test pin)
26	GND	-	GND	GND
27	GND	-	GND	GND
28	5.0V	-	Voltage Supply	5V voltage supply
29	GND	-	GND	GND
30	RESERVE	I/O	-	No connection(only connected to test pin)
31	RESERVE	I/O	-	No connection(only connected to test pin)
32	RESERVE	I/O	-	No connection(only connected to test pin)
33	RESERVE	I/O	-	No connection(only connected to test pin)
34	GND	-	GND	GND
35	GND	-	GND	GND
36	RESERVE	I/O	-	No connection(only connected to test pin)

Pin	Pin Name	I/O	Functional	Description
37	SDIO_CLK	I	CMOS Schmitt Trigger Input (with Pull-Up)	SDIO clock [CLK]
38	RESERVE	I/O	-	No connection(only connected to test pin)
39	RESERVE	I/O	-	No connection(only connected to test pin)
40	GND	-	GND	GND
41	GND	-	GND	GND(Pull Down
42	RESERVE	I/O	-	No connection(only connected to test pin)
43	SDIO_DAT3	I/O	CMOS I/O with Pull-Up	SDIO data [DAT3]
44	RESERVE	I/O	-	No connection(only connected to test pin)
45	SDIO_DAT2	I/O	CMOS I/O with Pull-Up	SDIO data [DAT2]
46	RESERVE	I/O	-	No connection(only connected to test pin)
47	SDIO_DAT1	I/O	CMOS I/O with Pull-Up	SDIO data [DAT1]
48	5.0V	-	Voltage Supply	5V voltage supply
49	SDIO_DAT0	I/O	CMOS I/O with Pull-Up	SDIO data [DAT0]
50	GND	-	GND	GND
51	SDIO_CMD	I/O	CMOS I/O with Pull-Up	SDIO command [CMD]
52	RESERVE	I/O	-	No connection

2.3 Power Supply

Tortuga are powered from the HOST board if used in conjunction with the HOST board.
For standalone operation Tortuga are powered from the AC adapter(12V/2A).

2.4 Usage for standalone operation

Please refer to the “UW2b Tortuga test TP quick manual“ for usage of standalone operation.

3. Function details

*VDD1V2 / VDD3V0 / VDD5V0 / VDD12V0 described in this chapter are correspond to symbol described in “2.1 Block diagram”.

3.1 Absolute Maximum Rating

Item	Symbol	Maximum Rate	Unit	Condition
Supply Voltage	VDD12V0	-0.3 ~ +43.5	[V]	From DC jack
	VDD5V0	-0.3 ~ +6.0	[V]	From Mini PCIE

3.2 Electrical Characteristics

Operation Temperature

Item	Symbol	Min	Typ	Max	Unit	Condition
Operation temperature	Ta		+25		[°C]	

Operation Voltage

Item	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	VDD12V0		12		[V]	From DC jack
	VDD5V0	4.75	5	5.25	[V]	From mini PCIE

DC characteristic

Ta = 25°C, standalone operation, VDD12V0=12V(AC adapter)

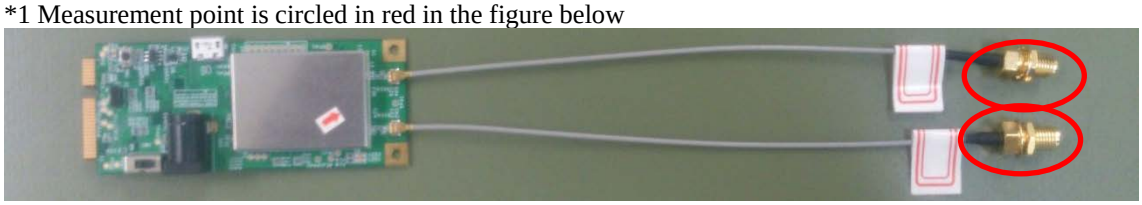
Item	Symbol	Min	Typ		Max	Unit	Condition
Current consumption (diversity off)	VDD12V0		TBD			[mA]	Listen mode
			TBD			[mA]	Rx mode
			TBD			[mA]	Tx mode (@24dBm)
Current consumption (diversity on)	VDD12V0		TBD			[mA]	Listen mode
			TBD			[mA]	Rx mode
			TBD			[mA]	Tx mode (@24dBm)

3.3 RF characteristic

*1 typical operating condition (Just informative, not guaranteed.):

*1 HW = Tortuga7, Ta = 25°C, standalone operation, VDD12V0=12V(AC adapter)

*1 Measurement point is circled in red in the figure below



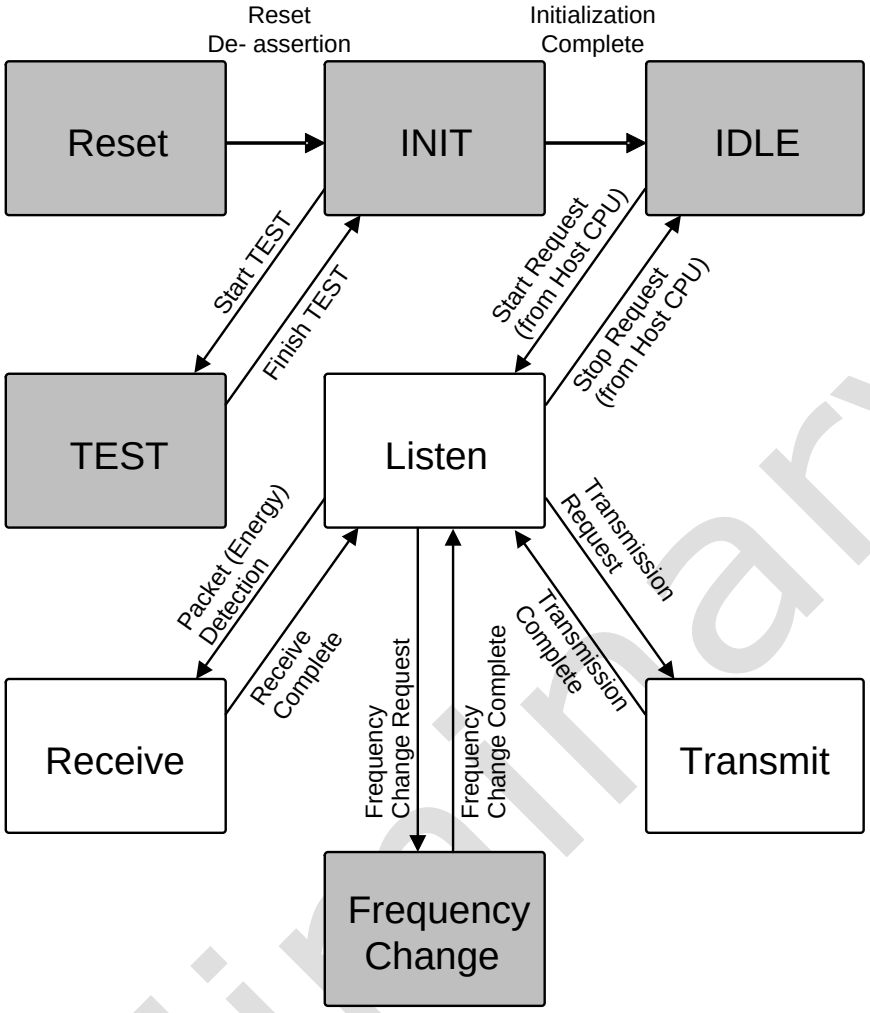
3.3.1 Receive characteristic

	Min	Typ	Max	Unit	Condition
Frequency range	5850		5925	[MHz]	
Input VSWR		2.0		-	5890MHz
Minimum Sensitivity (Diversity off)		-94		[dBm]	Data rate = 3Mbps
		-93		[dBm]	Data rate = 6Mbps
		-87		[dBm]	Data rate = 12Mbps
		-77		[dBm]	Data rate = 27Mbps
Minimum Sensitivity (Diversity on)		-94		[dBm]	Data rate = 3Mbps
		-94		[dBm]	Data rate = 6Mbps
		-87		[dBm]	Data rate = 12Mbps
		-80		[dBm]	Data rate = 27Mbps
Maximum Input Level (Diversity off)		-20		[dBm]	Data rate = 27Mbps
Maximum Input Level (Diversity on)		-20		[dBm]	Data rate = 27Mbps
Adjacent channel rejection (Diversity off)		30		[dB]	Data rate = 3Mbps
		29		[dB]	Data rate = 6Mbps
		28		[dB]	Data rate = 12Mbps
		18		[dB]	Data rate = 27Mbps
Nonadjacent Adjacent channel rejection (Diversity off)		44		[dB]	Data rate = 3Mbps
		41		[dB]	Data rate = 6Mbps
		36		[dB]	Data rate = 12Mbps
		27		[dB]	Data rate = 27Mbps

3.3.2 Transmit characteristic

	Min	Typ	Max	Unit	Condition
Frequency range	5850		5925	[MHz]	
Output VSWR		2.0			5890MHz
Maximum out put Power(ANT_B)		24		[dBm]	5890MHz
Maximum out put Power(ANT_A)		-8		[dBm]	5890MHz
Minimum out put Power(ANT_B)		-7		[dBm]	5890MHz
Minimum out put Power(ANT_A)		-35		[dBm]	5890MHz
Output Power control range		30		[dB]	5890MHz
Power control step		0.5		[dB]	
Relative constellation error		-28		[dB]	Data rate = 3Mbps
		-28			Data rate = 6Mbps
		-28			Data rate = 12Mbps
		-28			Data rate = 27Mbps
Spectrum Mask (in band)		-31		[dBr/100 KHz] @5890MHz	4.5MHz<f<5.0MHz offset Pout = 24dBm
		-33			5.0MHz<f<5.5MHz offset Pout =24dBm
		-36			5.5MHz<f<10.0MHz offset ±5.5MHz Pout= 24dBm
		-54			10.0MHz<f<15.0MHz offset Pout=24dBm

3.4 Mode Transfer Definition and sub board control



Mode	State	Note
Reset	Reset assert.	Transfer from the mode to the Reset mode by reset signal
INIT	Initialize RF block, internal register and other function.	Initialized LSI function after booting firmware
IDLE	Waiting start request from Host CPU	—
Listen	Waiting the packet indication.	Transfer the Receive mode by detecting the receive signal power, or transfer the Transmit mode by internal transmit request, or transfer the IDLE mode by stop request from Host CPU
Receive	Receive signal processing.	—
Transmit	Transmit signal processing.	—
Frequency Change	Changing Tx/Rx frequency.	—
TEST	Test mode.	Operate loop back calibration and other test for performance optimization

The MAC firmware and BBWLAN control the external RF circuits via the control pins ANT_SW_P, ANT_SW_N,

PAEN(Pin name = PAPE) and RFCNTL. The operation of these external RF circuit control pins according to the internal transceiver state and/or operation inside RF block are summarized in Fig. 3 and Fig. 4.

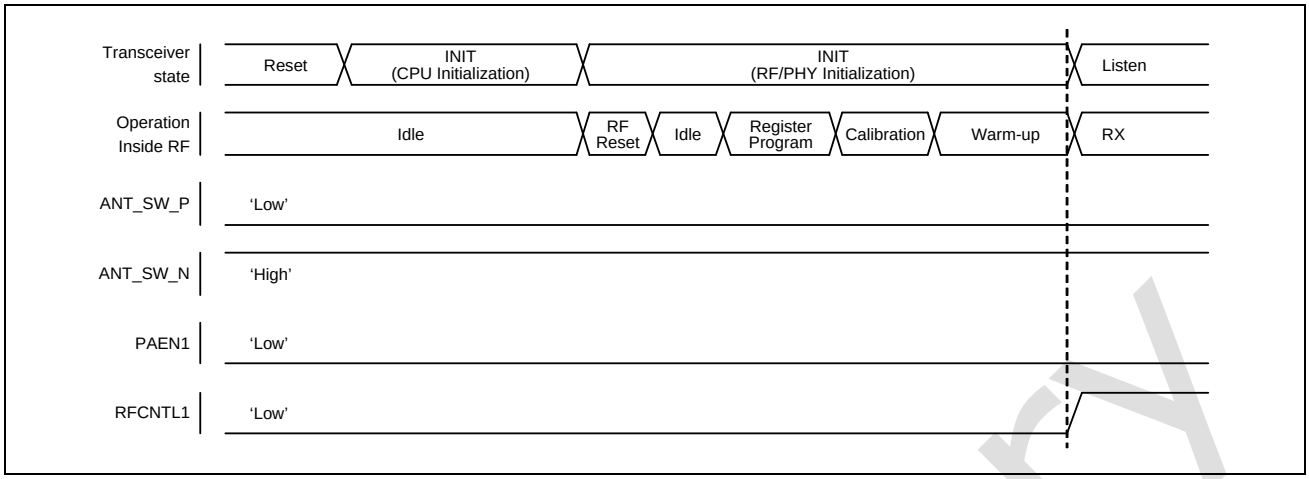


Figure 3 Operation of the External RF Circuit Control Pins (Reset and Initialization)

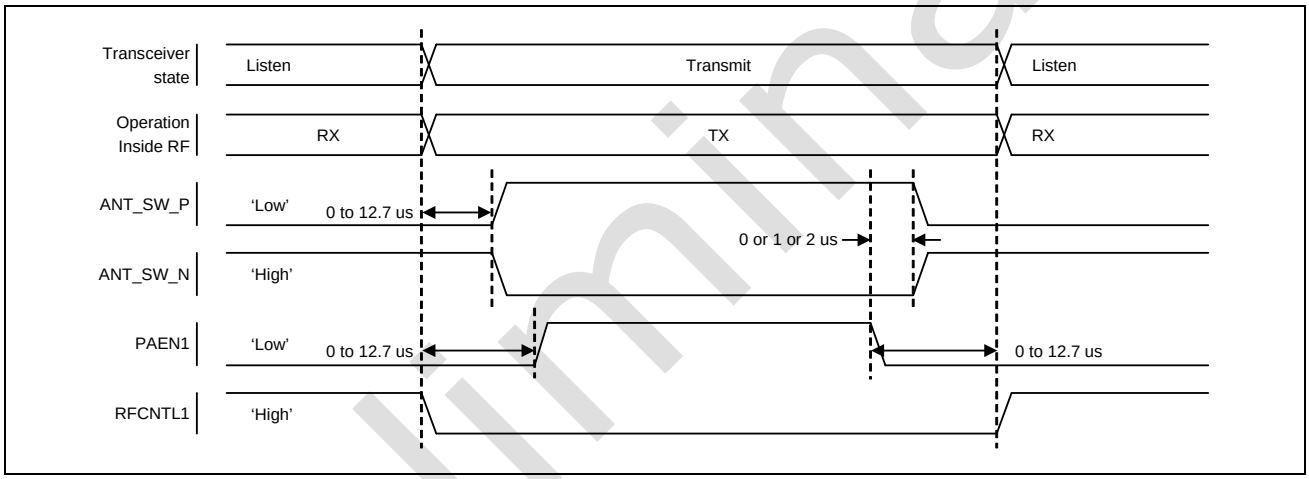


Figure 4 Operation of the External RF Circuit Control Pins (Transmission and Listening)

Remarks)

*1) The assertion timings of ANT_SW_P/N and PAEN1 can be tuned from 0 to 12.7us independently.

*2) RFCNTL2, PAEN2, ANT_M pins are reserved for the future as an optional function which might be realized by the MAC firmware. The detail operations are not defined in this hardware document.

3.5 Power up/down, Reset, WDT sequence

3.5.1 Power On / Off Sequence

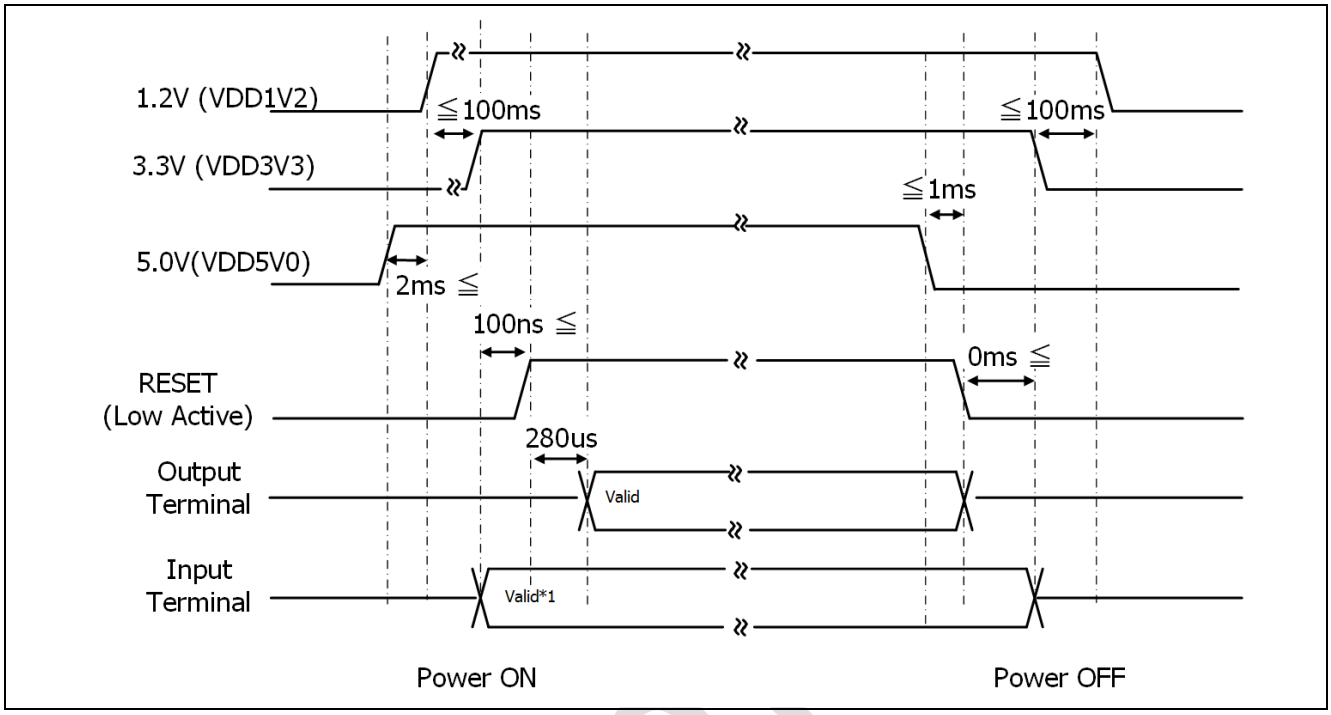
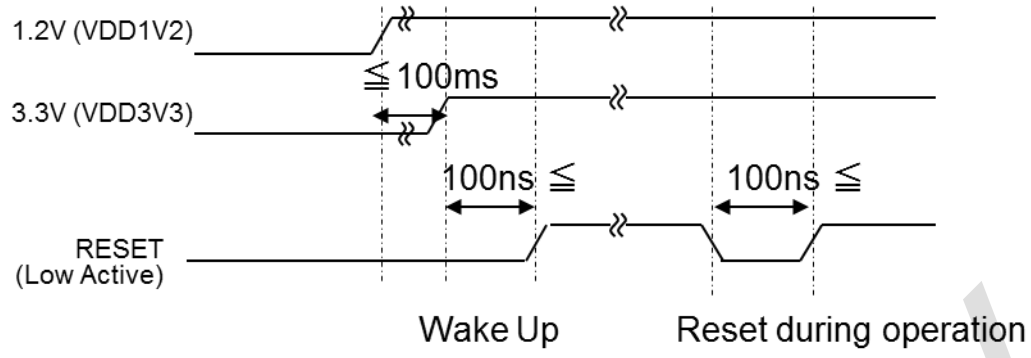


Figure 5 Operation of the External RF Circuit Control Pins (Transmission and Listening)

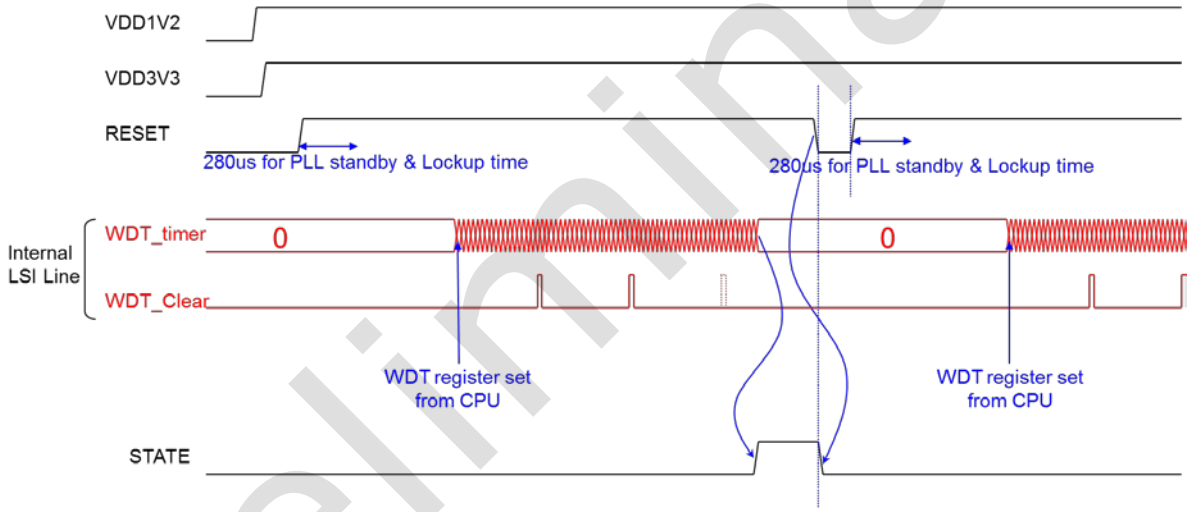
*1 “Valid” to module input pin in the figure means drive valid data (or pull-up/down) from external.
*2 each input signal level to Input from external shall not exceed VDD+0.3V (VDD3V3, VDD1V2,VDD5V0) correspondingly. .
*3 until 280us after reset release, output pin is not defined. After that, it drives initial value for each pin.
For power supply on, apply power in the order, 5.0V , 1.2V , 3.3V, and after passed more than 100ns of Low level, RESET is released. In order to PLL reset and to stabilize PLL oscillation, after about 280us, clock is supplied to LSI. For power off, the reverse order shall be done, i.e. RESET is “Active”, and switch off 5.0V , 3.3 V and 1.2 V.

3.5.2 Reset sequence



With making RESET pin ”Low”, LSI reset is executed. To be surely reset, hold RESETB level ”Low” for minimum 100ns. Also for reset under operation, control RESET level ”Low” for minimum 100ns.

3.5.3 WDT Reset timing



When Watch-dog time (WDT) counter becomes overflow, STATE signal output “High”, and informs WDT flow over to host CPU software. Then LSI stops as reset status. Host CPU software is able to re-start LSI with external RESET signal.

3.6 Logic interface AC Characteristics

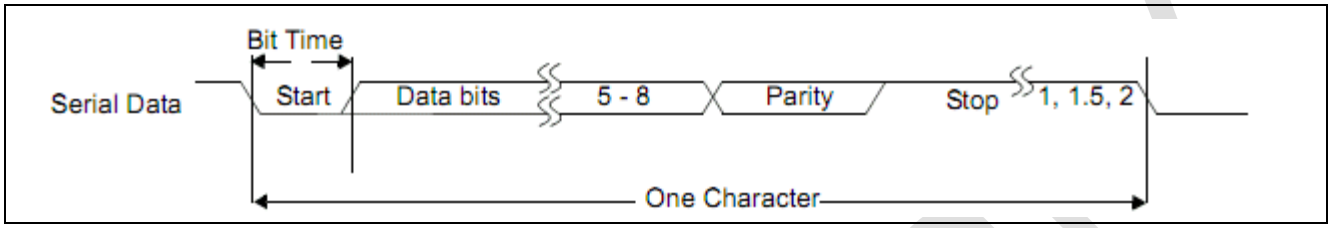
3.6.1 UART sequence

UART Interface characteristic

Ta = 25°C, VDD12V0

Item	Symbol	Min	Typ	Max	Unit	Condition
Baud rate	fUTRXD	50		128000	bps	
Bit Time	tUTRXD	7.81		20000	us	tUTRXD=1/fUTRXD

UART Serial Data Format



Baud Rate (bps)	Hex Divisor Setting	Bit Time (us)
50	0x61A8	20000.00
75	0x411B	13333.33
110	0x2C64	9090.91
134.5	0x244E	7434.94
150	0x208D	6666.67
300	0x1047	3333.33
600	0x0823	1666.67
1200	0x0412	833.33
1800	0x02B6	555.56
2000	0x0271	500.00
2400	0x0209	416.67
3600	0x015B	277.78
4800	0x0104	208.33
7200	0x00AE	138.89
9600	0x0082	104.17
19200	0x0041	52.08
38400	0x0021	26.04
56000	0x0016	17.86
57600	0x0016	17.36
115200	0x000B	8.68
128000	0x000A	7.81

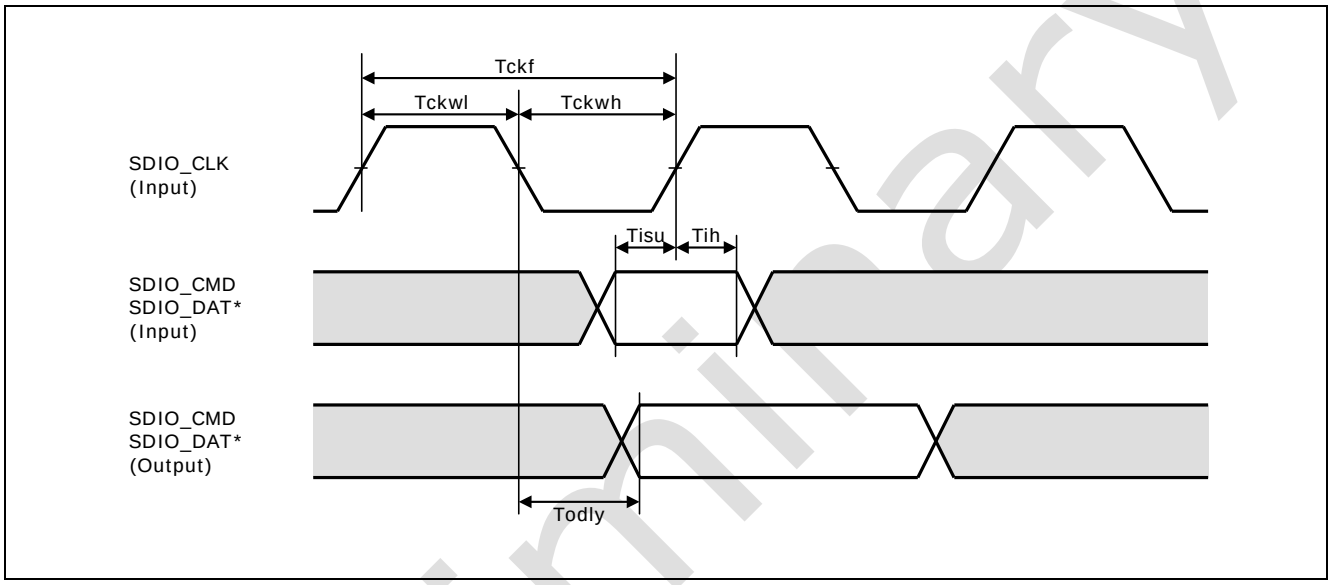
3.6.2 SDIO sequence

SDIO Interface characteristic

Ta = 25°C, VDD12V0

Item	Symbol	Min	Typ	Max	Unit	Condition
Clock frequency	Tckf			25	MHz	
Clock low position holding time	Tckwl	10			ns	
Clock high position holding time	Tckwh	10			ns	
Input set-up time	Tisu	5			ns	
Input holding time	Tih	5			ns	
Output delay time	Todly	0		14	ns	CL=25pF

SDIO Timing Format



3.6.3 1PPS sequence

1PPS Interface characteristic

Ta = 25°C, VDD12V0

Item	Symbol	Min	Typ	Max	Unit	Condition
PPS period	Tppsp	—	1.0	—	sec	—
PPS low position holding time	Tppsl	1.0	—	—	us	—
PPS high position holding time	Tppsh	1.0	—	—	us	—

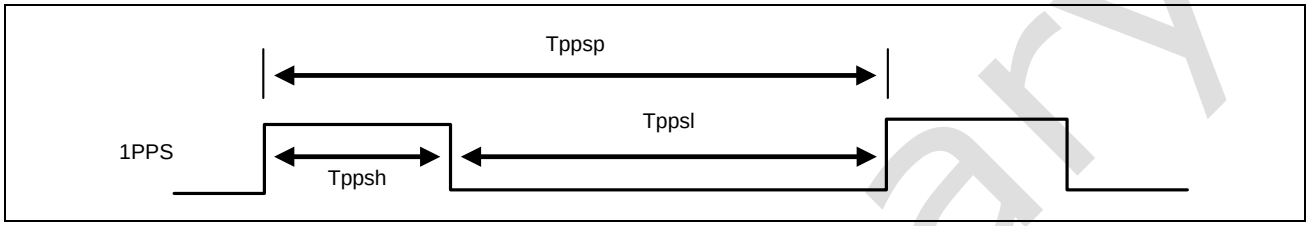


Figure 6 1PPS Interface Timing Format

Remark)

This interface is valid for the United States area. For the Europe area, this information can be ignored.

4. Appendix – Validation configuration information

Equipment information

No	Name	Information
1	VSA	FSQ-26(R&S)
2	VSG	E4438C(Agilent)
3	PC	Versa Pro VB-D(NEC)

5. Regulatory Warning Statements

Federal Communication Commission Interference Statement:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1)This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void

the user's authority to operate this equipment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
For operation within the 5860MHz~5920Mhz frequency range, it is restricted to indoor environment. This device meets all the other requirements specified in Part 90 of the FCC Rules

Caution: Risk of electric Shock, dry location use only

Radiation Exposure Statement:

The product comply with the FCC portable RF exposure limit set forth for an uncontrolled environment and are safe for intended operation as described in this manual. This equipment should be installed and operated with minimum distance of 20 cm between the radiator and your body. The further RF exposure reduction can be achieved if the product can be kept as far as possible from the user body or set the device to lower output power if such function is available.

Integrator Instructions

EUT Name: Tortuga
FCC ID: 2AHMN-W2R
Model Name: RTK00V2X720MTORS7J

Additional Regulatory Conformance Testing and/or Submissions Required by the Integrator:

The OEM integrator is responsible for additional system-level EMI/EMC and Product Safety testing and certification that applies in the U.S. and other countries to the host system containing the Module. This includes, but is not limited to, Federal Communications Commission ("FCC") Part 15 Class B Digital Emissions, and ETSI EN 301 489-17.
These system-level EMC tests are to be done with the Module installed and included in the scope of the submission.

European Community R&TTE

CE0560 ⓘ

Notice: Observe the national local regulations in the location where the device is to beused. This device may be restricted for use in some or all member states of the European Union (EU).

The device complies with RF specifications when the device used at least 20cm from human body.
The users has to turn off the 5.9GHz WiFi in outdoor environment.

ORIGINAL EQUIPMENT MANUFACTURER (OEM) NOTES

- The OEM must certify the final end product to comply with unintentional radiators (FCC Sections 15.107 and 15.109) before declaring compliance of the final product to Part 15 of the FCC rules and regulations. Integration into devices that are directly or indirectly connected to AC lines must add with Class II Permissive Change.

- The OEM must comply with the FCC labeling requirements. If the module's label is not visible when installed, then an additional permanent label must be applied on the outside of the finished product which states: "Contains transmitter module FCC ID: 2AHMN-W2R. Additionally, the following statement should be included on the label and in the final product's user manual: "This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interferences, and (2) this device must accept any interference received, including interference that may cause undesired operation."

- The module is limited to installation in mobile or fixed applications. Separate approval is required for all other operating configurations, including portable configuration with respect to Part 2.1093 and different antenna configurations.

- A module or modules can only be used without additional authorizations if they have been tested and granted under the same intended end-use operational conditions, including simultaneous transmission operations. When they have not been tested and granted in this manner, additional testing and/or FCC application filing may be required. The most straightforward approach to address additional testing conditions is to have the grantee responsible for the certification of at least one of the modules submit a permissive change application. When having a module grantee file a permissive change is not practical or feasible, the following guidance provides some additional options for host manufacturers. Integrations using modules where additional testing and/or FCC application filing(s) may be required are: (A) a module used in devices requiring additional RF exposure compliance information (e.g., MPE evaluation or SAR testing); (B) limited and/or split modules not meeting all of the module requirements; and (C) simultaneous transmissions for independent collocated transmitters not previously granted together.

This Module is full modular approval, it is limited to OEM installation ONLY.
Integration into devices that are directly or indirectly connected to AC lines must add with Class II Permissive Change.
(OEM) Integrator has to assure compliance of the entire end product includ the integrated Module.
Additional measurements (15B) and/or equipment authorizations (e.g Verification) may need to be addressed depending on co-location or simultaneous transmission issues if applicable.
(OEM) Integrator is reminded to assure that these installation instructions will not be made available to the end user of the final host device.

Revision Record	RTK00V2X720MTORS7J User's Manual : Hardware

Rev.	date	Change summary	
		Page	**Details**
1.0	17.Jan.2017		1st Documents (Hisataka TAKAGI)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

— The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

— The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

— The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

— The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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