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MLU290-M5 Intelligent Accelerating Card Product Manual

V0.2.0

Preliminary

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1.2. Version

1Table 1.1 Version Record

Document name	MLU290-M5 Intelligent Accelerating Card Product Manual
Version number	V0.2.0
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1.3. Update history

V0.2.0

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Update:

- Initial version

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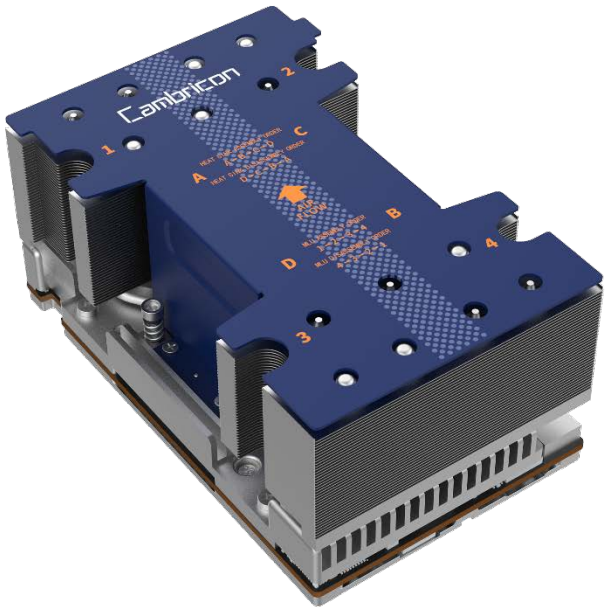
2. Overview

MLU290-M5 is the first high performance Intelligent Accelerating Card for cloud data center in cambricon, which provides excellent performance and energy efficiency ratio. At the same time it supports heavy tasks such as deep learning training, large-scale data analysis, artificial intelligence reasoning and so on. MLU290-M5 supports cambricon adaptive precision training and provides up to 512 TOPs INT8 hashrate to align the data accuracy of training and reasoning business. MLU290-M5 provides inter-chip high speed interconnection technology CCLINK, supports cross-system direct connection, which can build large scale training clusters easily.The new vMLU function fully supports SRIOV, which can provide services by multiple virtual instances to give full play to computing efficiency.



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3. Product Specification Overview

3.1 Overview of Product Specification Parameters

MLU290-M5 Intelligent Accelerating Card specification parameters are as follows:

1Table 3.1 MLU290-M5 Specification Parameters

Specification indicators	Note
Product model	MLU290-M5
Core architecture	Cambricon MLUv02
Core frequency	1GHz
Integer speed (INT8)	512TOPS (Dense)
Calculation accuracy support	INT16,INT8,INT4,FP32,FP16
Video decoding	Support
Memory capacity	32GB
Memory width	4096- bit
Memory bandwidth	1024GB/s
System interface	PCI Express 4.0x16, lane reversal supported
PCI identifier	PCIE Vendor ID 0xCABC PCIE Device ID 0x0290 PCIE Sub-Vendor ID xCABC 0 PCIE Sub-System ID 0x0012
CCLINK interface	6Ports
CCLINK bandwidth	600GB /S
TDP power consumption	350W
ECC protection	Yes
Heat dissipation scheme	Passive

3.2 Overview of structure specifications

MLU290-M5 Intelligent Accelerating Card structure specifications:

2Table 3.2 MLU290-M5 Structure Specification

Specification indicators	Note
Card shape	102 mm*165mm,OAM standard
Card Weight	1.47 Kg
Minimum chip pressure	30PSI
Maximum chip pressure	60PSI
Partner labelling area	16.1mm*40.2mm

3.3 Overview of Power Supply Specifications

MLU290-M5 Intelligent Accelerating Card power specifications:

3Table 3.3 MLU290-M5 Power Supply Specifications

Specification indicators	Note
Input voltage	DC54V±5%, 6.48 A±5%
Electrical data peak processing (EDPp)	1.6X TDP ≤2ms 1.5X TDP ≤5ms 1.2X TDP ≤10ms 1.1X TDP ≤20ms

3.4 Overview of heat dissipation specifications

MLU290-M5 Intelligent Accelerating Card heat dissipation specifications:

4Table 3.4 MLU290-M5 Heat dissipation Specifications

Specification indicators	Note
MLU maximum operating temperature (Tj)	95℃
MLU slowdown temperature (Tj)	97℃
MLU shutdown temperature (Tj)	100℃
MLU power reduction ratio	1/2 to 1/8

3.5 Overview of interface specifications

MLU290-M5 Intelligent Accelerating Card interface specifications:

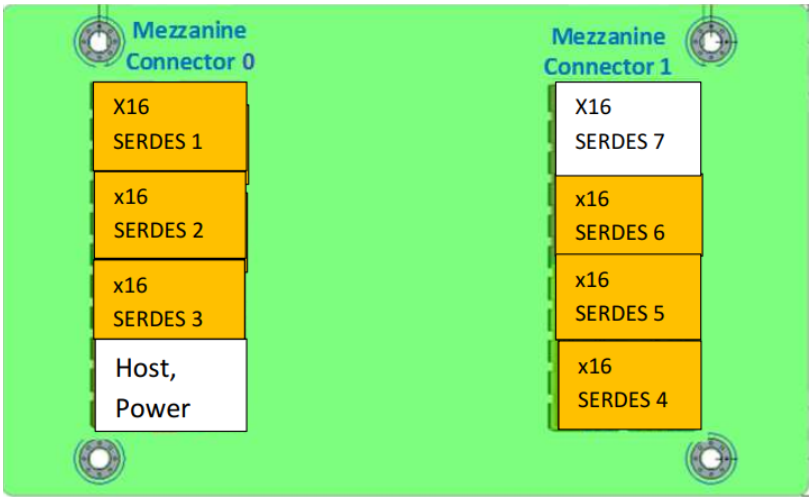
5Table 3.5 MLU290-M5 Interface Specification

Interface	Note
PCIE Base address	PF (1,64 bit): BAR0：256MB prefetchable BAR2：256MB prefetchable BAR4：256MB prefetchable VF (4,64 bit): BAR0：256MB prefetchable BAR2：256MB prefetchable BAR4：256MB prefetchable
SMBus (8bit address)	0 x8E (Write) 0x8F (Read)

4. Electrical specifications

4.1 Connector pin description

MLU290-M5 Intelligent Accelerating Card using two 688-pin Molex Mirror Mezz snap connectors.The design impedance of the connector is 90Ω±5%, which can be compatible with both 85Ω and 100Ω protocols. The signal and power are connected to the main board through this connector, and the connector pin area is divided as follows:



1Figure 4.1 Connector pin area division

The connector pins are shown in the following table:

1Table 4.1 MLU290-M5 connector arrangement of pin 0

Signal	Direction of signal	Signal description	Voltage
PWR_54V	I	MLU290-M5 power input pin which support 40V-60V power supply	40V-60V
PVREF[1:0]	O	MLU290-M5 JTAG interface, I/O signal and voltage indication signal ,1.8 V.	1.8V
PETp/n [15:0]	O	PCIE signal sending. MLU290-M5 send, baseboard receive.Make sure that AC	/

		coupling capacitor is placed near the fastener connector of the baseboard. The recommended capacitance value is 220 nF	
PERp/n [15:0]	I	PCIE signal receiving. MLU290-M5 receive, baseboard send. Make sure that AC coupling capacitor is placed near the sending chip or fastener connector of the baseboard. The recommended capacitance value is 220 nF	/
PE_REFCLKp/n	I	PCIE 100MHz reference clock	/
PERST#	I	MLU290-M5 reset signal, low level effective	3.3V
HOST_PWRGD	I	Baseboard power good indication signal	3.3V
MODULE_PWRGD	O	MLU290-M5 power good indication signal	3.3V
PWRBRK#	I	Power brake, reduce to 1/4 of current power consumption, low level effective	3.3V
MODULE_ID[4:0]	I	MLU290-M5 slot ID. MLU290-M5 internal default 10KΩ pull-up resistor	3.3V
I2C_SLV_D	I/O	I2C data signal, MLU290-M5 works in slave mode	3.3V
I2C_SLV_CLK	I	I2C clock signal, MLU290-M5 working in slave mode	3.3V
I2C_SLV_ALERT#	O	I2C alarm signal, MLU290-M5 works in slave mode	3.3V
UART_TXD	O	MLU290-M5 MCU UART serial port output	3.3V
UART_RXD	I	MLU290-M5 MCU UART serial port input	3.3V
JTAG0_TRST	I	MLU290-M5 JTAG0 TRST reset signal	1.8V
JTAG0_TMS	I	MLU290-M5 JTAG0 TMS mode selection signal	1.8V
JTAG0_TCK	I	MLU290-M5 JTAG0 TCK clock signal	1.8V
JTAG0_TDO	O	MLU290-M5 JTAG0 TDO data output signal	1.8V
JTAG0_TDI	I	MLU290-M5 JTAG0 TDI data input signal	1.8V
PRSNT0#	O	MLU290-M5 fastener connector 0 in position signal, MLU290-M5 default 1KΩ pull-down resistor. Recommend 10KΩ pull-up resistor on baseboard.	1.8V or 3.3V
MANF_MODE#	I	Undefined functions	3.3V
FW_RECOVERY#	I	Undefined functions	3.3V
TEST_MODE#	I	Test mode. NC is acceptable	1.8V or 3.3V
RFU	/	Reserved pin	/

2Table 4.2 MLU290-M5 connector arrangement of pin 1

Signal	Direction of signal	Signal description	Voltage voltage

SERDES_4Tp/n [15:0]	O	CCLINK4[15:0] transmit signal	/
SERDES_4Rp/n [15:0]	I	CCLINK4[15:0] receiving signal	/
SERDES_5Tp/n [7:0]	O	CCLINK5[7:0] transmit signal	/
SERDES_5Rp/n [7:0]	I	CCLINK5[7:0] receiving signal	/
SERDES_6Tp/n [15:0]	O	CCLINK6[15:0] transmit signal	/
SERDES_6Rp/n [15:0]	I	CCLINK6[15:0] receiving signal	/
SERDES_7Tp/n [15:8]	O	CCLINK7[15:8] transmit signal	/
SERDES_7Rp/n [15:8]	I	CCLINK7[15:8] receiving signal	/
AUX_156M_REFCLKp/n	I	CClink 156.25MHz reference clock	/
PWRRDT#[1:0]	I	TDP power setting pin, 3.3V pull-up is provided by the baseboard. 11：L0 level, normal TDP power consumption 350 W default. 10：L0 level,TDP power consumption reduced to 300 W. 01:L2 level,TDP power consumption reduced to 250 W. 00:L3 level,TDP power consumption reduced to 200 W.	3.3V
THERMTRIP#	O	MLU290-M5 over-temperature alarm, which will trigger MLU290-M5 automatically shut down, please check the chassis fault (such as fan fault) and then restart the device, low level effective	3.3V
LINK_CONFIG[4:0]	I	Serdes link configuration topology, MLU290-M5 internal default 10 K pull-up	3.3V
PE_BIF[1:0]	O	Indication of PCIE interface bit width : MLU290-M5 default 00 00-1 x16(default) 01-2 x8 00-4 x4 00- Reserved	3.3V or 1.8V
PLINK_CAP	O	Support of PCIE port protocol : MLU290-M5 default 0 0= Only support PCIE protocol(default) 1= Support other protocols, reserved	3.3V or 1.8V
PRSNT1#	O	MLU290-M5 fastener connector 1 in position, MLU290-M5 default 1KΩ pull-down resistor . Recommend 10KΩ pull-up resistor on baseboard.	3.3V or 1.8V
SCALE_DEBUG_EN	O	Undefined functions	3.3V
DEBUG_PORT_PRSNT#	I	Baseboard debug port in position indication signal. NC is acceptable.	1.8V
RFU	/	Reserved pin	

Note:connector signal pin list and pin map see attached document.

4.2 Power supply requirements

4.2.1 Input power supply

MLU290-M5 Intelligent Accelerating Card input power requirements:

3Table 4.3 MLU290-M5 Input Power Specification

Input voltage	Input Current
54V±5%	6.48 A±5%

Note:

1.The voltage value shall be the test value at the connector;

2.If the input voltage is low, the current value needs to be raised to meet TDP 350W specification;

4.2.2 Peak current of power supply

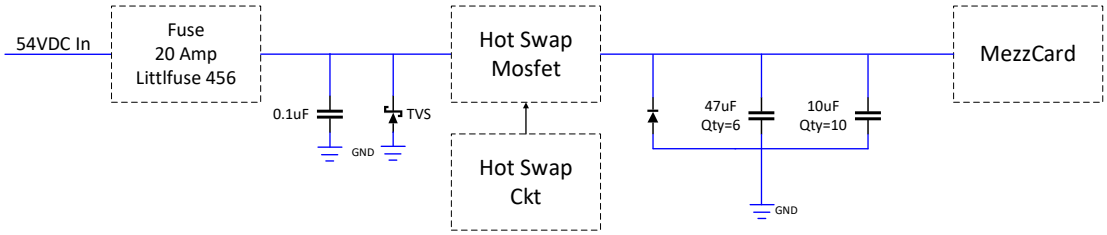
MLU290-M5 Intelligent Accelerating Card is able to reduce power consumption adjustment for transient power changes above the μs level. the power regulator can support power fluctuations within the ms level (e.g .1.2 x TDP).

4 Table 4.4 MLU290-M5 EDPp Specification

EDP	Duration
1.6*TDP	⩽2 ms
1.5*TDP	⩽5 ms
1.2*TDP	⩽10 ms
1.1*TDP	⩽20 ms

4.2.3 HSC protection circuit

MLU290-M5 Intelligent Accelerating Card input voltage is DC 54V.Hot Swap Controllers (HSC) is required on the baseboard to provide slow start, short circuit protection and over-current/voltage protection for MLU290-M5. It is recommended to provide a separate HSC for each MLU290-M5. The transient power consumption need to support more than 2 ms within 1.6 *TDP.The block diagram of HSC is as follows:

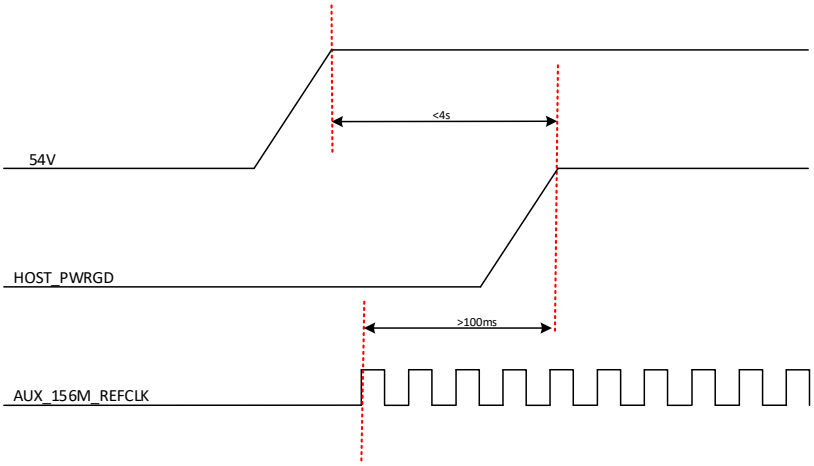


2Figure 4.2 HSC block diagram

LM5069 and LM5066I of TI are recommended by the HSC controller.The selection of MOS should focus on SOA curve. Infineon IPB017N10N5LF and Nexperia PSMN4R8-100BSE are recommended.

4.2.4 Power on time sequence

When MLU290-M5 Intelligent Accelerating Card power on normally with DC 54V voltage,the HOST_PWRGD signal is sent out after the reference clock (156.25MHz) is stable.Detailed timing sequence is as follows:



3Figure 4.3 Power on Timing Sequence

4.3 Signal description

4.3.1 Clock signal

AUX_156M_REFCLKp/n receiving support LVPECL,LVDS,CML,HCSL and other common differential level signal input.As a CCLINK high-speed SERDES reference clock, its phase noise jitter is required less than 270fs.

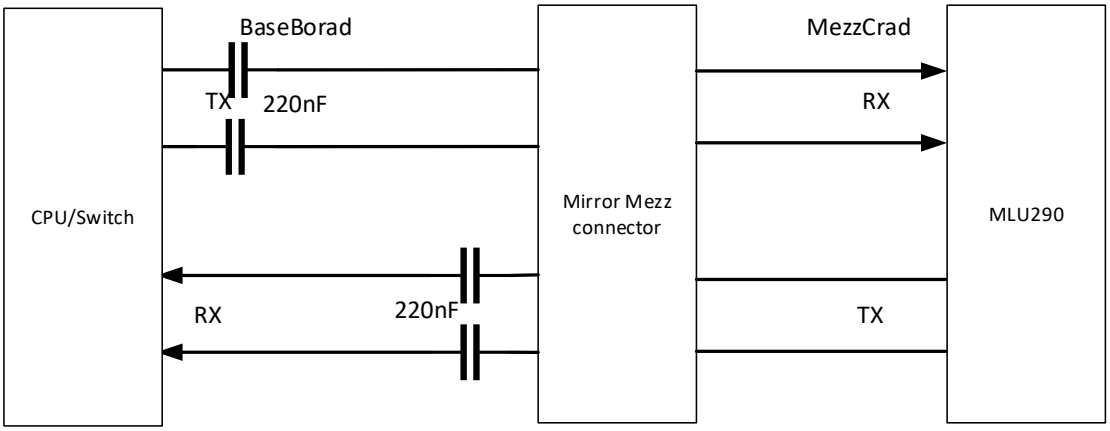
5 Table 4.5 AUX_156M_REFCLK Specifications

Parameters	Conditions	Minimum value	Typical values	Maximum value	Units

Frequency	--	100	156.25	400	MHz
Frequency offset	--	-100	--	100	PPM
Maximum voltage value	--	--	--	3.3	V
Minimum voltage value	--	GND	--	--	V
Differential swing	--	0.15	--	1.3	V
Duty cycle	--	45	50	55	%
Phase noise jitter	12KHz –20MHz	--	--	270	fs RMS

4.3.2 PCIE signal

MLU290-M5 Intelligent Accelerating Card supports PCIE GEN4.0 x16 bit width default.There is no AC coupling capacitor in MLU290-M5. Sending and receiving AC coupling capacitors are placed on the baseboard and the value range is 176nF-265nF (220nF recommended). The placement position reference diagram is as follows:



4Figure 4.4 PCIE AC Coupled Capacitance

PE_REFCLK reference clock shall meet the requirements of PCIE GEN4.0 specification, phase noise jitter should be less than 0.5 ps.

6Table 4.6 PE_REFCLK Specifications

Signal	Direction of signal	Signal description
PETp/n [15:0]	O	PCIE sending signal. MLU290-M5 send, baseboard receive.
PERp/n [15:0]	I	PCIE receiving signal. MLU290-M5 receive, baseboard send.

PE_REFCLKp/n	I	PCIE 100MHz reference clock

4.3.3 CCLINK signal

CCLINK is an internal connection link between MLU290-M5 Intelligent Accelerating Cards.The maximum transmission rate of CCLINK can be 50 Gbps PAM4, which is compatible with OAM specifications. SERDE _[3：1]R/T[15:0],SERDE _5R/T[15:8] and SERDE _7R/T[7:0] are not used in MLU290-M5. The 48 pairs of serdes in the table below are used， which are compatible with combine topology. For detailed internal connection topology please refer to the reference topology chapter.

7Table 4.7 CCLINK Signal description

Signal	Direction of signal	Signal description
SERDES_4Tp/n [15:0]	O	CCLINK4[15:0] transmit signal
SERDES_4Rp/n [15:0]	I	CCLINK4[15:0] receiving signal
SERDES_5Tp/n [7:0]	O	CCLINK5[7:0] transmit signal
SERDES_5Rp/n [7:0]	I	CCLINK5[7:0] receiving signal
SERDES_6Tp/n [15:0]	O	CCLINK6[15:0] transmit signal
SERDES_6Rp/n [15:0]	I	CCLINK6[15:0] receiving signal
SERDES_7Tp/n [15:8]	O	CCLINK7[15:8] transmit signal
SERDES_7Rp/n [15:8]	I	CCLINK7[15:8] receiving signal

4.3.4 Other signals

4.3.4.1 SMBUS signal

I2C_SLV_D /CLK/ALERT# satisfy the SMBus protocol and supports 400KHz max, with 8 bit addresses of 0x8E(write)/0x8F(read). MLU290-M5 works in slave mode.

8Table 4.8 SMBUS Signal description

Signal	Direction of signal	Signal description
I2C_SLV_D	I/O	I2C data signal
I2C_SLV_CLK	I	I2C clock signal
I2C_SLV_ALERT#	O	I2C alarm signal

SMBUS registers are described as follows:

9Table 4.9 SMBUS Register description

Register definition	Address	Reading and writing	Note
Card power consumption	0x01	RO	Power consumption, float, unit W
Card Temperature	0x02	RO	Card temperature,float, unit ℃
Chip temperature	0x03	RO	Chip temperature,float, unit ℃
power brake	0x05	WO	Main frequency reduce to 25% of current value when write 0x04, and recover to the frequency before reducing when write 0x01.
PCIE Vendor ID and Device ID	0xA0	RO	[15:0] Vendor ID ： 0xCABC [31:16] Device ID ： 0x0290
PCIE Sub-Vendor ID and Sub-System ID	0xA1	RO	[15:0] Sub-Vendor ID ： 0xCABC [31:16] Sub-System ID ： 0x0042
PCIE _negotiated_speed	0xA2	RO	Display PCIE negotiation rate, e.g .0 x 04 indicate gen4 16GT/s
PCIE_negotiated_link_width	0xA3	R O	Display PCIE negotiation width, e.g .0 x16 means X16.
Type of card	0xF0	RO	Display card type
Manufacturer	0xF1	RO	Display equipment manufacturer number
Hardware version number	0xF2	RO	Display hardware version number
Firmware version number	0xF3	RO	Show firmware version number, e.g .0 x04420100 means master chip version number 0x04, card type 0x42, master version number 0x01, sub version number 0x0 and patch number 0x0.
Manufacturing time	0xF4	RO	Display manufacturing time, e.g .0 x2006 means manufactured in June 2020
Serial number	0xF5	RO	Display the serial number of the device, e.g .0 x30001 indicating a serial number of 30001

4.3.4.2 THERMTRIP# overtemperature alarm signal

THERMTRIP# is triggered when MLU290-M5 chip junction temperature is over 100℃, which is irreversible after effective. It is recommended to trigger fan full speed when the chip temperature of MLU290-M5 is below 93℃, trigger power drop to 1/2 when chip temperature rises to 97℃, trigger power drop to 1/4 when chip temperature rises to 98℃ , trigger power drop to 1/8 when chip temperature rises to 99℃.If the chip temperature rises to 100℃, which means the power reduction measures fail, the system may have fan failure or other catastrophic failures. At this time MLU290-M5 will pull down the THERMTRIP# signal to alarm baseboard management system. MLU290-M5 will automatically cut off the power supply for shutdown protection after 1s.

THERMTRIP# signal will continue to be low after effective. It is recommended to confirm manually on site, and restart the system after troubleshooting.

4.3.4.3 Power Configuration Signal

MLU290-M5 Intelligent Accelerating Card provides two power configuration pins:PWRBRK# and PWRRDT#[1：0].PWRBRK# is based on the current power consumption and responses fast.When low-level is effective,it is reduced to 1/4 of the current power consumption.PWRRDT#[1：0] is a hardware implementation mode of power capping, which can set 4 types of TDP power consumption: 350 W, 300W, 250W, 200. It is recommended that the baseboard should be pulled up to 3.3V by default to obtain better performance.

The MLU290-M5 Intelligent Accelerating Card also supports setting the upper limit of TDP power consumption by sending power capping instructions through the I2C interface, and the setting range is 175 W-350W.

10Table 4.10 Power Configuration Signal Description

Signal	Direction of signal	Signal description
PWRBRK#	I	Power brake,power is reduced to 1/4 of current power consumption, low level is effective
PWRRDT#[1:0]	I	TDP power setting pin, baseboard must provide default 3.3 V high level 11 - L0 level, normal TDP power consumption 350 W, default 10 - L1 level,TDP power consumption reduced to 300 W 01 - L2 level,TDP power consumption reduced to 250 W 00 - L3 level,TDP power consumption reduced to 200 W

4.3.4.4 Other configuration signals

11Table 4.11 Other configuration signals descriptions

Signal	Direction of signal	Signal description
MODULE_ID[4:0]	I	MLU290-M5 slot ID. MLU290-M5 internal default 10 K pull up
LINK_CONFIG[4:0]	I	Serdes link configuration topology, MLU290-M5 internal default 10 K pull up
PE_BIF[1:0]	O	PCIE interface bit width indication: MLU290-M5 default 00 00-1 x16(default) 01-2 x8 00-4 x4 00- Reserved
PLINK_CAP	O	Support of PCIE port protocol: MLU290-M5 default value is 0 0= Only support PCIE protocol (default) 1= Support other agreements , reserved

4.3.4.5 Reserved signals

The following signals are defined in OAM protocol, but not used in MLU290-M5,which are recommended to NC.

12Table 4.12 Reserved signal description

Signal	Direction of signal	Signal description
SCALE_DEBUG_EN	O	Undefined functions
DEBUG_PORT_PRSNT#	I	Baseboard debug port in position indicator signal. NC
MANF_MODE#	I	Undefined functions
FW_RECOVERY#	I	Undefined functions

TEST_MODE#	I	Test mode. NC
RFU	/	Reserved pin
NC	/	Suspension pin

5. Heat dissipation specifications

5.1 Heat dissipation instructions

MLU290-M5 Intelligent Accelerating Card adopts passive heat dissipation mode.

5.2 Maximum operating temperature

Maximum operating temperature means the recommended maximum operating temperature (junction temperature Tj) of MLU290-M5. Junction temperature is obtained through the chip built-in temperature sensor at the software interface through instructions. It is recommended to control the maximum operating temperature of the main chip of MLU290-M5 below 95℃.

5.3 Slowdown temperature

Slowdown temperature means the temperature point which the IPU frequency is reduced.The slowdown temperature of MLU290-M5 is 97℃.

5.4 Shutdown temperature

Shutdown temperature means the temperature point which the power is cut off. The shutdown temperature should not be triggered during normal operation, and the system may have a catastrophic damage when the shutdown temperature is triggered. The shutdown temperature of MLU290-M5 is 100℃.

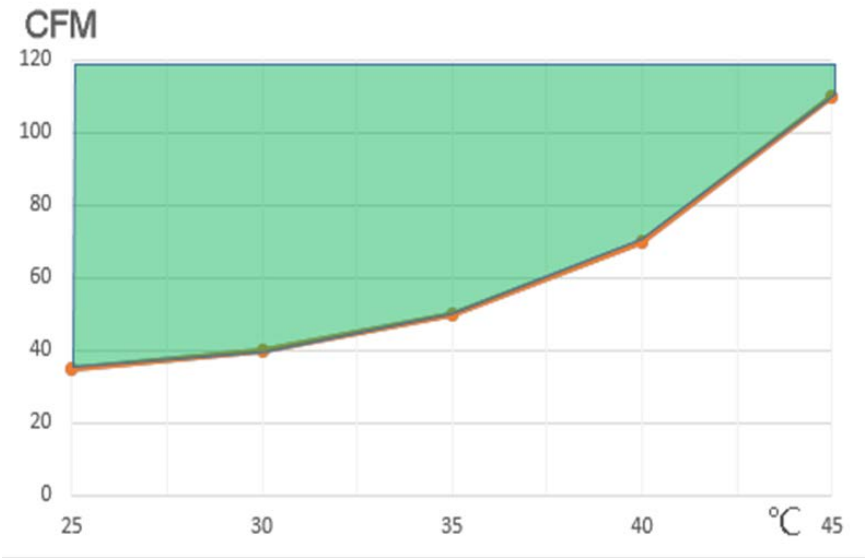
When the chip junction temperature of MLU290-M5 reaches 100℃, the THERMTRIP# signal will be triggered and the power supply of MLU290-M5 will be cut off after 1s. After the power is cut off, it is recommended to eliminate the heat dissipation problem manually before restart.

5.5 Air inlet temperature requirements

The required environment temperature of MLU290-M5 is 0-45℃. The minimum air volume requirements of radiator under main temperature conditions is shown in the table below:

51Figure 1. Minimum air volume requirement VS Air inlet temperature table for MLU290-M5

Air inlet temperature (℃)	Radiator Minimum Air Volume Requirements (CFM)
25	35
30	40
35	50
40	70
45	110



51Figure 1. Minimum air volume requirement vs Air inlet temperature

It is recommended to use MLU290-M5 Intelligent Accelerating Card in green area.

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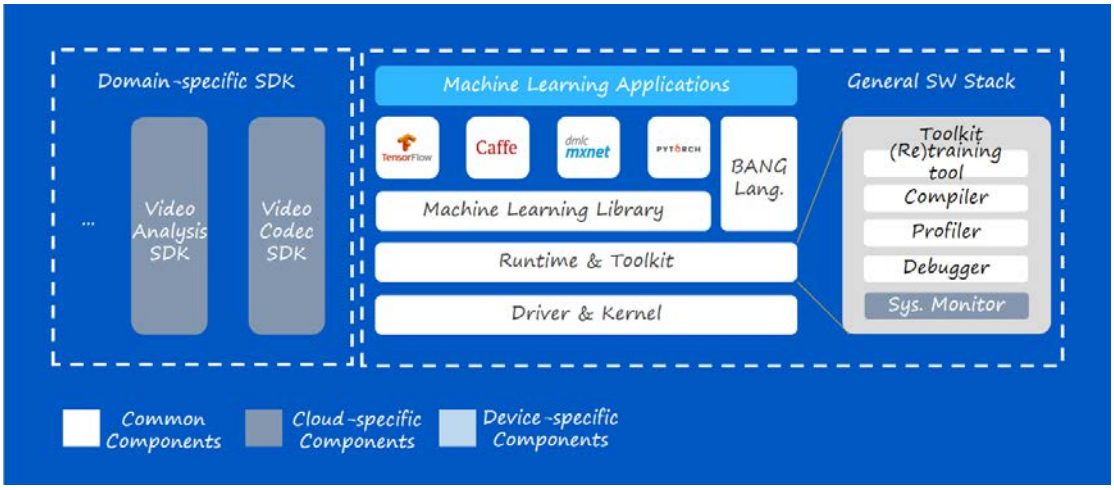
6. Cambricon NeuWare development environment

NeuWare fully supports various mainstream programming frameworks (e.g. TensorFlow 、Caffe 、PyTorch and MXNet). Users can easily develop and deploy deep learning applications on cambricon MLU290-M5. At the same time, the NeuWare provides a complete runtime system and driver software to facilitate the rapid integration of the system.

NeuWare also provides a range of tools including application development, function debugging, performance tuning, etc. Among them, application development tools include machine learning library, runtime library, compiler, model retraining tool and specific field (such as video analysis field) SDK; function debugging tools can meet different levels of debugging requirements such as programming framework and function library; performance tuning tools include performance profiling tools and system monitoring tools.



1Figure 6.1 Cambricon NeuWare

7. Compliance

MLU290-M5 Intelligent Accelerating Card is compliant with the regulations listed in this chapter. The compliance marks can be found on the labels of each devices.

FCC statement

This device complies with Part 15 of the FCC Rules.

Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

CE statement

- This product must not be used in residential areas.

- This product may cause interference if used in residential areas. Such use must be avoided unless the user takes special measures to reduce electromagnetic emissions to prevent interference to the reception of radio and television broadcasts.