Product Development

TRX Integration Guide.

450-470MHz FSK version

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Revision History

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1. Introduction

1.1. Purpose

This Document will provide the design constraints for the inclusion of the 7700H TRX into a Cattron-Theimeg Inc. product capable of meeting the requirements of FCC part 90, DOD chapter 5.3.2, ETSI 300-220v2.1.1, this module will be configured by software and cover the frequency ranges of 450MHz to 470MHz. and power ranges 1mW to 500mW.

Modulation schemes supported will be, 2GFSK and 2RCFSK.

This design is to be based on the latest generation Analog Devices ADF7021 High Performance Narrowband ISM Transceiver IC.

1.2. Scope

- This document is to define the requirements for this TRX to maintain operation within FCC rules and approved operation, to include.
- Transceiver interface.
- Supported protocols.
- Hardware target size.
- Software requirements.
- Operating band.
- Exi testing and approvals.

1.3. Definitions, Acronyms, Abbreviations

1.3.1. Definitions

- **Anomaly**. Anything observed in the documentation or operation of software that deviates from expectations based on previously verified software products or reference documents. A critical anomaly is one that must be resolved before the V&V effort proceeds to the next life- cycle phase.
- **Third Party Testing.** The verification testing required to be carried out by an authorized body.

1.3.2. Acronyms

- ETSI European Telecommunication Standards Institute
- EN European Norm (legal obligation)
- FCC Federal Communication Commission
- DOD Department of Defense USA
- CAT800 Modulation Protocol consisting of 3 distinct states
- 2GFSK Modulation consisting of two distinct states and Gausian modified rate of change.
- 2RCFSK Modulation consisting of two distinct states and Raised Cosine modified rate of change
- URM Universal Radio Module
- EPH Current generation of CTI encoder design.
- Exi Intrinsically safe approvals.
- SDD Software Design description

- SRS system Requirements Specification
- SVVP Software Verification and Validation Plan
- SVVR Software Verification and Validation Report
- V&V Verification and Validation
- EMC Electromagnetic Compatibility
- SRD Short Range Device

1.3.3. Abbreviations

none

1.4. References

1. EN300-220v2.1.1
2. FCC/DOD5.3.5.2 Emission Mask
3. ADF7021 Preliminary Technical Datasheet 7700 Agile attachment
4. Drawing current EPH encoder 84C-0149 7700 Agile attachment
5. RF2155 Programmable Gain Power Amp 7700 Data sheet Agile attachment.
6. EN301-489 EMC Short Range Devices (SRD's)

1.5. Overview

1.5.1. Notation Conventions

Throughout this document, functionality may be listed using the following syntactical conventions:

- The use of "shall" implies a requirement that must be implemented.

2. Overall Description

2.1. Product Perspective

This Radio module version is constrained to 450-470MHz, 0dBm to 27dBm, FSK modulation and 30% maximum duty cycle.

The Radio modules is to achieve full interchangeability between product model lines, maintaining mechanical and software interfaces as well as physical dimensions is a general objective.

2.1.1. User Interfaces

All interface between this module and the User will be software controlled by the product hosting this module. Features such as Frequency, Power and Modulation are all controlled by the Host device.

2.1.2. Hardware Interfaces

This product will have two hardware interfaces, these are the RF Port and a 50 pin I/O connector carrying the microcontroller interface and power lines.

The 50 pin interface will have a

- 4 wire serial interface, consisting of Clock in, Data out, Data in and Load.
- Power: Vbat, 3V3 synth and E2Prom 3-5V
- I2C interface to store personality.
- Power control interface consisting of 2 wire power set and one wire PA amp on
- Data I/O 1 wire out 1 wire in
- Chip enable 1 wire.

2.1.3. Software Interfaces

This module will require the configuration of 15 Data Registers by the operating firmware that set the operating parameters.

The AE system will provide the operational parameters to the operating firmware.

- Frequency,
- Power,
- Tx/Rx Mode.

2.2. Product Functions

- The Product shall have the capacity to hold a permanent configuration file
- The Product shall be software configurable
- The Operating frequency shall be Programmable
- The Modulation scheme shall be programmable
- The Modulation Deviation shall be programmable
- The Transmit Power shall be programmable
- The Transmit Power envelope Ramp rate shall be Programmable on both the rising and falling edges.

2.3. User Characteristics

Operators: Require no knowledge of this part, all configuration is taken care of in the engineered product.

Technicians: The programming of this device is effected by the connected encoder, the encoder can choose to program the device according to it's own programming or it can take the configuration table from the eeprom on the radio module.

Therefore the radio module may be independently programmed with the register table, or programmed by the controller housing it.

2.4. Constraints

This subsection describes any items that limit the developer's options. These include:

- FCC Part 90 rules
- ETSI EN300-220v2.1.1 (or later)
- EN301-489
- DOD Chapter 5.3.2 rules
- Exi limitations imposed on individual components, e.g. maximum capacitance or inductance.
- Interconnectivity compatibility with URM physical interface.
- Interconnectivity compatibility with URM programming interface.
- Physical size for interchangeability with Unity products and current Cattron Toggle and Paddle.
- RF Connector type MMCX
- Limitation of Human body exposure.

2.5. Assumptions and Dependencies

It is assumed that this device may need to be revised if any of the constraint's change.

It is also assumed that the requirements of narrow banding will ultimately force the use of 3GFSK or 4GFSK and a consequential upgrade in decoder receiver technology.

Any actual changes will require further FCC submissions for approvals.

3. Specific Requirements

3.1. External Interface Requirements

3.1.1. Interfaces

3.1.1.1 50 Pin Header I/O.

PIN	Label	Description
1,2	RFVBAT	Switched Battery voltage to RF Deck, 5V5 min – 16V max.
3,4	GND	
5-14	N/C	
15	SWD	O/P, Sync Word Detect, asserts High, (may be programmed Low), when a specific data frame is received. May be used to lock to talkback message on CAT800.
16-19	N/C	
20	DATCLK	I/O, Clock, When in RX mode leading edge is synchronous with RX Data, When in TX mode data is latched in on leading edge. IF in UART mode used to output TX Data.
21	ENA	I/P, Enable RF deck when High.
22	GND	
23	PAON	I/P, RF Power ON and switch to TX mode when High.
24	PLE	I/P, Load Enable, Control Data is latched into registers when High
25	TRDAT	Data I/O when synchronous, RX data OUT when asynchronous.
26	TXD	TX in when asynchronous (Fit R35)
27	3V3	Regulated input for synthesizer.
28	3V3/5V	Regulated input for E2PROM
29	N/C	
30	PCLK	I/P, Control Register Clock, data clocked on rising edge.
31	PDI	I/P, Control Register data read in.
32	PDO	O/P, Control Register data read out, MSB first.
33	RXD1	May be used to output Received Data (Fit R35).
34	MUX	O/P, TRX status, multi use.
35-37	N/U	
38	SDA	TRX E2PROM
39	SCL	TRX E2PROM
40	N/U	
41	G8	I/P, PA +8dB Gain, assert High
42	N/U	
43	G16	I/P, PA +16dB Gain, assert High
44-50	N/U	

3.1.1.2 RF Antenna Port

- MMCX type connector.

3.1.2. Software Interface Requirements

Software requirements are generally as required to implement the interface indicated above, more specifically

The RXD and TXD lines will need to have a direct microprocessor interface with baud rates able to cope with the maximum communication rate, a variable dependant on operating mode, this version is limited to 4,000baud.

Power Amplifier control consisting of PWR LSB, PWR MSB and PA-ON may be implemented through a latch, (further power control is available through the Synthesizer control registers.)

Standby will power down the RF device and can be implemented through a latch.

The I2C interface has no specific speed requirements but security of data transferred shall be verified.

3.2. System Features

3.2.1. EEPROM

Onboard EEPROM for storing one or more defined RF Personalities.

3.2.1.1. EEPROM Functional Requirements

- I2C Bus
- Memory Size 8KB
- CRC Data Protection HD>6

3.2.1.2. EEPROM Repository

The EEPROM on this module may be configured to hold a personality database of the registers required for the synthesizer programming as well as various yet to be defined configuration data, such information may include

Power, including a gain calibration value.

Frequency , or a table of Frequencies

Skip frequency table

Data Format.

3.2.2. Programmable Output Power

- Synthesizer output power is programmable by internal register 2. between, OFF, -16dBm and +13dBm.
- Power Amplifier gain control is also programmable by setting the two gain bits for gains in 8dB steps between, 0dB and +24dB.
- Care needs to be taken to ensure maximum dynamic range from the synthesizer is maintained to control switching transients when power ramping is implemented, the Gain settings of the final amplifier are set to ensure no more than 3dB of signal drive compression from the ADF7021.
- PA Ramp rate is set to 64 codes/bit. For 4KB and 32codes/bit for 2KB.

3.2.3. Software Configurable

- All aspects of Synthesizer operation are software configurable, both in Transmit and Receive modes, refer to the ADF7021 data sheet for full and up to date details.

3.2.4. Low Cost VCO

- In this version the VCO is internal to the synthesizer and operating at twice the output frequency.

3.3. Performance Requirements

3.3.1. Frequency Range

- 450MHz to 470MHz

3.3.2. Switching range

- Switching range to be >= + - 200kHz

3.3.3. Alignment Ranges

- 450-470MHz

3.3.4. Power

- Programmable from 0dBm to 27dBm

3.3.5. Frequency Error and Drift

Under Extreme conditions

Portable -20C to +55C and simultaneous 1.3Vnom and 0.85Vnom.

Fixed equipment mains powered -20C to +55C and simultaneous +-10% Vac

Frequency error or drift

Frequency separation(kHz)	Frequency error limit (kHz)	
	> 300 MHz to 500 MHz	> 500 MHz to 1 000 MHz
6,25	±0,75	±0,75
10/12,5	±1,50	±1,50

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3.3.6. Adjacent and co channel power

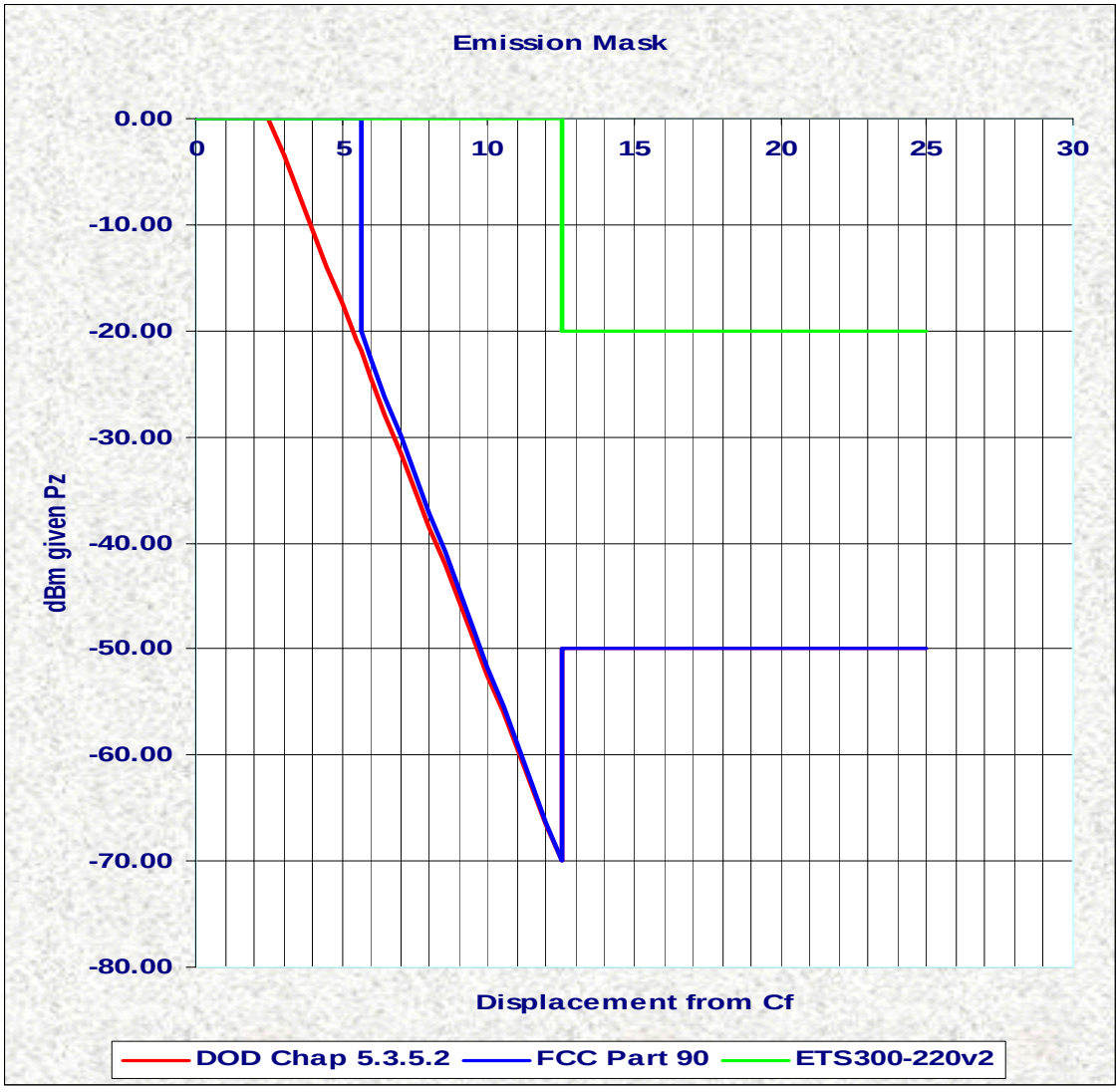
- With test modulation representative of normal operational modulation (baud rate and deviation) shall fall within the limits defined in USA DOD Chapter 5.3.5.2 Emissions mask

  Where P is measured power, Pz is Carrier power un-modulated, Fc is Centre frequency, Ft = Test frequency.

  P(dBc)=Pz for Ft from Fc to Fc + - 2.5kHz where Pz=carrier power when un- modulated.

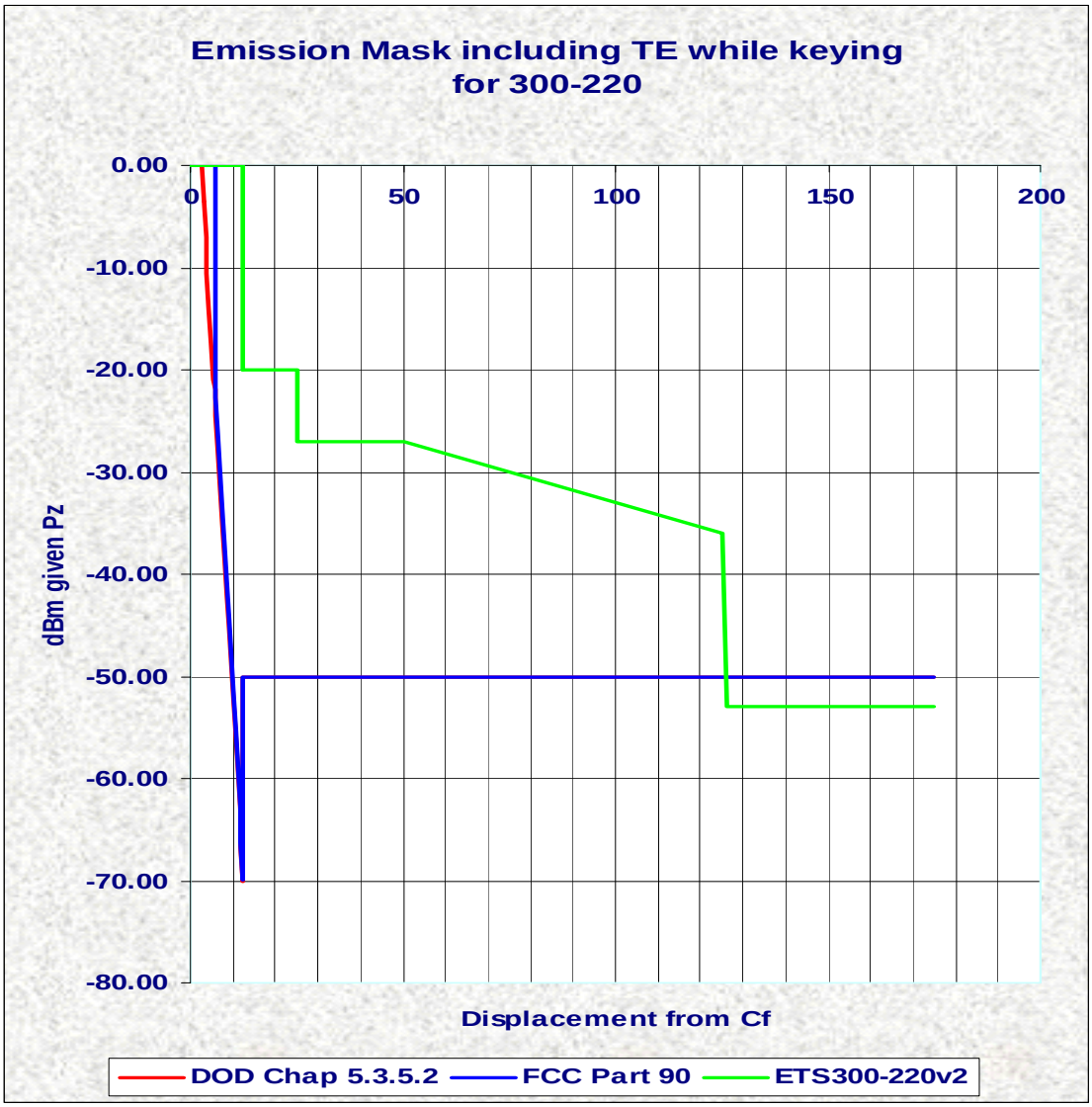
  P for Ft =Fc+ - 2.5kHz to Fc + - 12.5kHz, P(dBc)= -7*(Fd-2.5)

  P= the lesser of -50dBm or -70dBc for Ft>= Fc+ - 12.5kHz



3.3.7. Transient Emissions

- Carried out with the transmitter operating both normally, i.e. keying and modulating with normal data and in test modulation modes. To meet the requirements of ETSI 300-220v2.1.1 (or later)
- Alternate channel (2nd channel away) -40dBc without the need to exceed -27dBm.
- 4X and 10X Channel -50dBc without the need to exceed -36dBm.
- FCC Part 90.214 Transient frequency behavior.



3.3.8. Modulation

The unit shall be capable of the following modulation schemes, adjustable by programming.

- 2GFSK and RC2FSK with and without CAT800 protocol q-sync capability, i.e. able to generate during transmission after a calibration toggle sequence a short un-modulated center frequency carrier, before resumption of normal 2GFSK
- Programmable deviation.

NB: The product of Modulating rate and Deviation shall not exceed 8K5 / 2

3.3.9. Keying

The module shall be capable of continuously keying between a transmitting and low power mode. On Off time will depend on many factors but typically would be a 10% or less duty cycle, maximum duty cycle at full power must be <=30%, this imposes the requirement for the VCO to lock in <=5mS. (for CAT800 systems), verified by software prior to PA ON.

3.4. Design Constraints

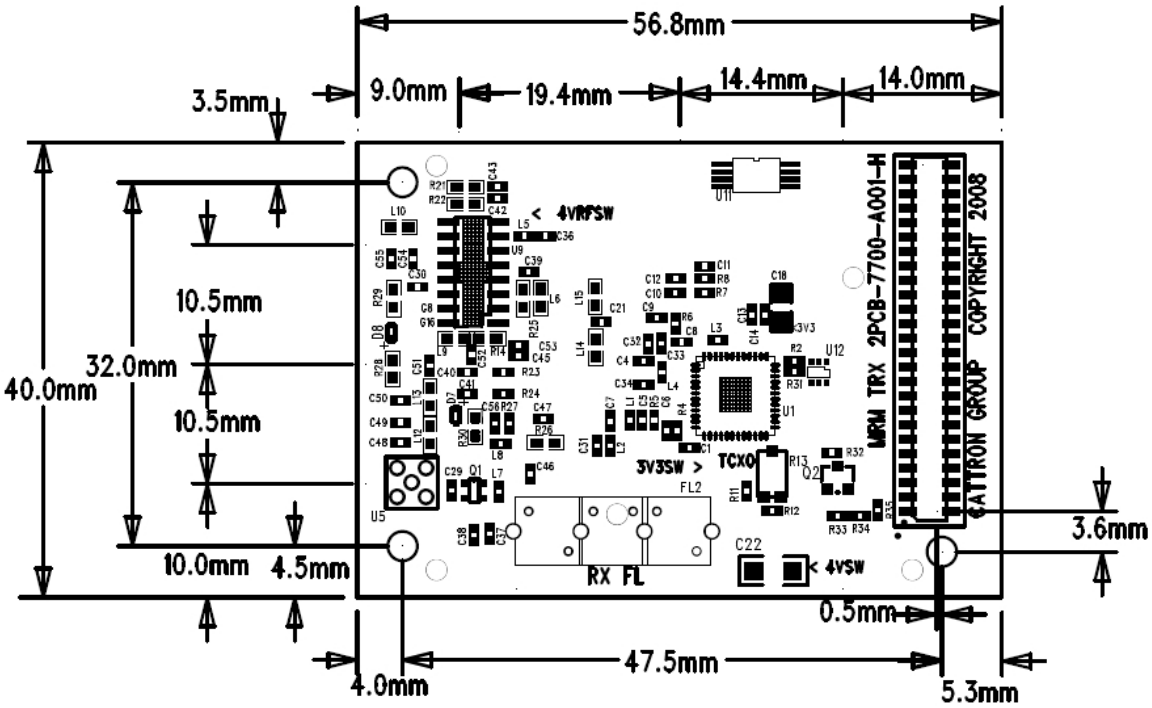
3.4.1. Standards Compliance

- EN300-220 v2.1.1 or later @10mW, (normal keyed modulation applies)

  EN301-489-3 EMC Immunity Short Range Devices
- FCC Part 90 @ 500mW, (normal keyed modulation applies)
- DOD 5.3.5.2 @ 500mW, (normal keyed modulation applies)
- EN61000-6-2:2001 EMC Immunity
- SARS Human body exposure limits.

3.4.2. Mechanical Dimensions

7700H TRX outline



3.4.3. Power Requirements

There are three power sources required for operation

VBat : 5V-16Vdc @500mA

The module power consumption will vary with output power.

Maximum requirements for Vbat used to supply the PA will be 500mA at 27dB. during transmit.

Maximum duty cycle will be <30%, typically <10% with a consequential overall reduction in average power.

3V3: 3V+- 10% @ 100mA

3V3 EEPROM : 3V+-10% @ 100mA

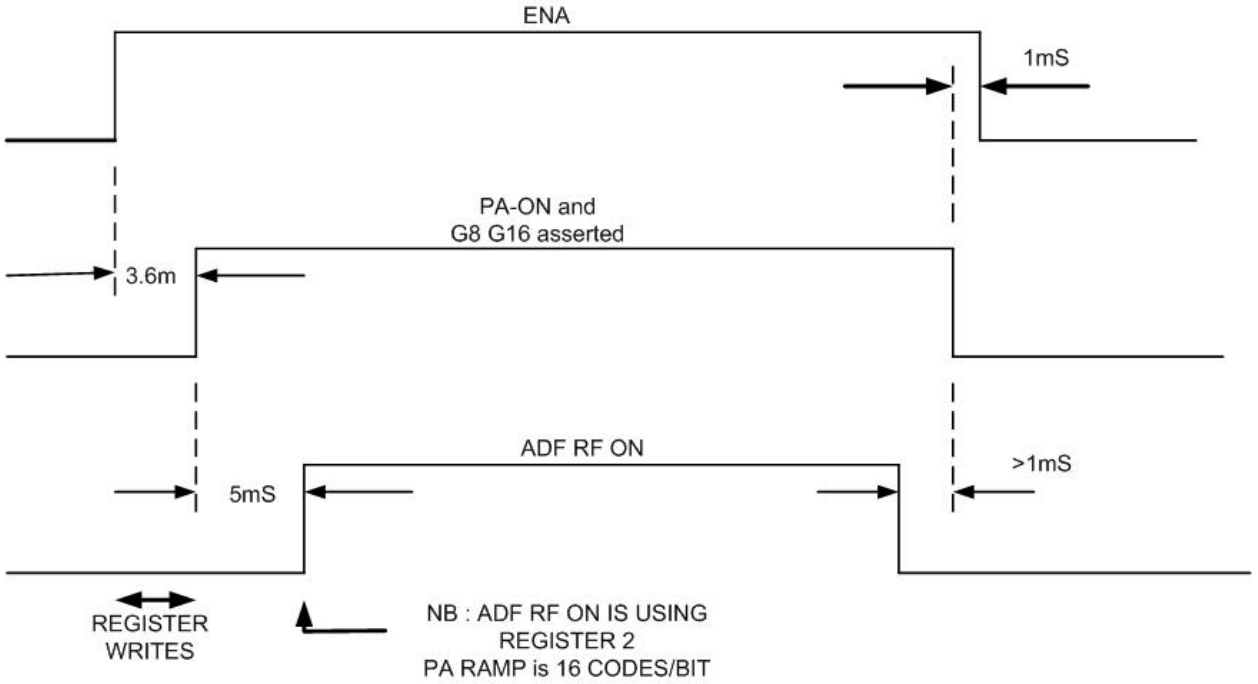
3.4.4. Software Requirements

3.4.4.1. Overall Timing TX Mode

The control of the ENA, PA-ON, G8 and G16 lines need to be sequenced to comply with the following general sequence. Before progressing to the next state it must be verified by read back that the prior stage is complete, i.e. Regulator ready, VCO ready, etc, otherwise use the following timings.

Note that due to digital filtering latency it is necessary to maintain RF ON and DATA CLK for a number of clock cycles after completion of data loading, typically this latency will not exceed 5 clock cycles, failure to do this may result in early termination of tx data.

Overall Timing diagram



3.4.4.2. Register Program Sequence TX Mode

After CE low, Wait for MUX input to indicate regulator ready (default)
Wait for 3mS for all to settle
Note TCXO frequency is 14.31818MHz.

1. **Program Register 0 and register 1**

2. **Program Registers 2**
   2.7 PA OFF=0
3 **Program Register 1,**
4. **Program Register 3**
5. **Program Register 0,**
6 **Set PA_ON = 1** switches on PA, & Ant SW to TX, Wait 5mS
7 **Program Register 2,**
   2.7 PA enable = 1 ***SWITCH ON PA***
   2.6-2.4 Modulation scheme = 001 or 101
8 **Output Data**
9 **Program Registers 2**
   2.7 PA OFF=0
   Continue clocking data 0 for 6 cycles.
10 **Set PA_ON = 0 switches off PA, & Ant SW to RX,**
11 **Take CE low powers down RF deck**

***** product of Modulation rate and deviation must not exceed 8K5 / 2***

3.5. System Attributes

3.5.1. Reliability

All design aspect of this module shall be maintained within Agile along with all supporting documentation and data sheets for future reference.

Maintenance of, Manufacturing, Re-design, Approvals and Testing and continuous improvement shall fall within the requirements of the quality control system.

3.5.2. Availability

P.O.S.T and ongoing system checks should be employed to check system availability and continued stability.

3.5.3. Security

The data within the onboard EEPROM, personality array shall be protected by a CRC with a HD>=6

3.5.4. Maintainability

As most aspects of this module are software configurable, little maintenance is likely to be needed, Tuning is minimized

Specific configuration data may be stored within the Personality EEPROM.

Adjustments are minimal, and likely to be limited to TCXO and RX Helical adjustment. and in the case of a Power amplifier equipped version Helical Filter tuning.

3.5.5. Portability

It is envisaged that all Radio modules will be transferable between different encoders and decoders.