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# Small Receiver Transmitter Module
# RFM307

**Radio Transceiver Description V1.0**

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# 1.0 Introduction

This document describes in detail the implementation of the RFM307 transceiver module used in the SmaRT product line. It is assumed that the reader has some hardware and software background related to microprocessor based embedded systems.

# 2.0 General Description

The RFM307 transceiver module provides wireless communication functions in a general purpose module that is incorporated into various control system products typically covered by FCC Part 15.212, configured as split systems. The module is composed of a single shielded printed circuit board (PCB) assembly. An RF transceiver integrated circuit (RFIC) implements the active RF circuits, while passive components provide RF filtering and DC power bypassing. A linear pass regulator IC provides DC power pre-regulation to reduce possible RF noise associated with the active RF circuits of the IC. An SPI serial digital interface and several digital I/O signals provide for control of the functions of the RFIC. The programmable control IC can be any microcontroller that has sufficient software program capacity, an SPI serial port, several digital I/O bits and compatible electrical specifications.

The RFIC provides a general capacity to send and receive digital data packets in a manner suitable to the 2.4GHz ISM band. Carrier modulation is Direct Sequence Spread Spectrum (DSSS) compatible with the IEEE 802.15.4 ZigBee standard(s), as supported by the RFIC that is installed. The packet data contents are define by the application software which may implement a standardized or proprietary communications protocol, as required.

The RFM307 does not include an antenna as part of the module.

The radio transceiver module is identified as a Cervis Inc. proprietary product 07420307-A-0, which is not intended for resale.

# 3.0 Transceiver Block Diagrams

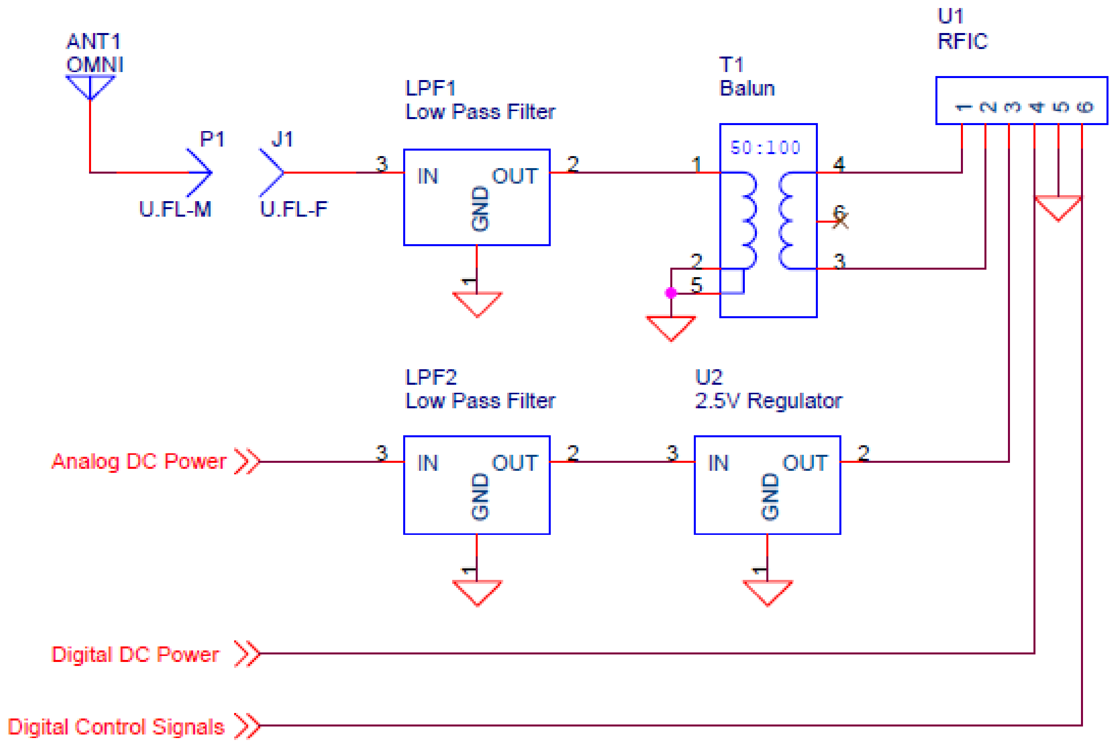


*Figure 1. Block Diagram of RFM307, no pa lna*

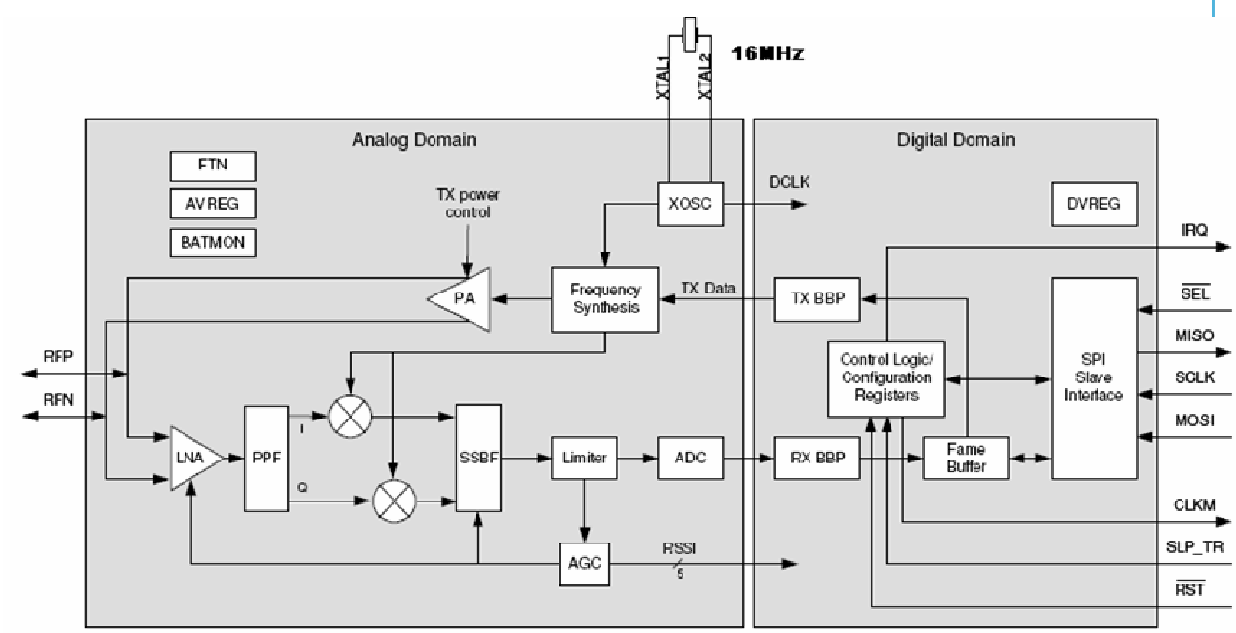


*Figure 2. Block Diagram Atmel AT86RF230 Transceiver (from data sheet)*

The RFIC utilized in the RFM307 is AT86RF230, manufactured by Atmel. The RFIC is a "low-power 2.4 GHz radio transceiver especially designed for ZigBee/IEEE 802.15.4 applications" according to the AT86RF230 Data Sheet. Most, if not all, subsequent information is derived from the AT86RF230 Data Sheet. The transceiver IC is capable of operating in the frequency range of 2405MHz to 2480MHz, divided into 16 pre-defined channels. The adjustable transmission power is stated to be -17dBm to +3dBm, +/-3dBm. All RF functions are controlled by an external programmed controller that can read and write the RFIC's internal control registers, accessed via the SPI serial digital control interface and digital I/O control signals. See the manufacturer's data for additional details.

# 4.0 Transceiver Theory of Operation

## 4.1 Power Supply

The RFM307 requires DC power from external regulated sources provided by the host application hardware. The RFIC is internally divided into digital and analog sections, each provided with an internal linear DC regulator. Power for the digital sections of the RFIC is bypassed using ceramic capacitors and connected to the RFIC Digital Power Input, which sets the voltage levels used for the external digital interface signals. The RFIC internal linear pass regulator further conditions the power used for internal digital circuits, such as the control registers. Power for the analog sections of the RFIC is filtered by an LC Pi-network, pre-regulated by the provided external linear pass regulator, and connected to the RFIC Analog Power Input. The RFIC internal linear pass regulator further conditions the power used for internal analog circuits, such as RF amplifier and the synthesizer VCO. By this arrangement, The RFM307 can accept a wide range of DC power sources, +2.7Vdc to +3.3Vdc, and thus connect to a wide variety of host applications, yet still provide excellent and consistent RF performance.

## 4.2 Host Interface

The host control interface is primarily via the SPI serial digital control port. Additional digital control signals are provided. All digital signals are fully buffered inside the RFIC to isolate the RF circuits from the digital control signals.

## 4.3 Receiver Function

*(From the AT86RF230 Data Sheet)*

The AT86RF230 receiver is split into an analog radio front end and a digital base band processor (RX BBP).

The RF signal is amplified by an internal low noise amplifier (LNA) and converted down to an intermediate frequency by a mixer. Channel selectivity is performed using an integrated band pass filter. A limiting amplifier (Limiter) provides sufficient gain to overcome the DC offset of the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal with 3 dB granularity. The IF signal is sampled and processed further by the digital base band receiver.

The RX BBP performs additional signal filtering and signal synchronization. The frequency offset of each frame is calculated by the synchronization unit and is used during the remaining receive process to correct the offset. The receiver is designed to handle frequency and symbol rate deviations up to ±120 ppm, caused by combined receiver and transmitter deviations. Finally the signal is demodulated and the data are stored to the Frame Buffer.

## 4.4 Transmitter Function

*(From the AT86RF230 Data Sheet)*

The AT86RF230 transmitter consists of a digital base band processor (TX BBP) and an analog radio front end. The TX BBP reads the frame data from the Frame Buffer and performs the bit-to symbol and symbol-to-chip mapping as specified by IEEE 802.15.4 in section 6.5.2.

The O-QPSK modulation signal is generated and fed into the analog radio front end. The fractional-N frequency synthesizer (PLL) converts the baseband transmit signal to the RF signal, which is amplified by the internal power amplifier (PA). The PA output is internally connected to bidirectional differential antenna pins (RFP, RFN), so that no external antenna switch is needed.

## 4.5 Antenna Connection

The RFM307 PCB provides a connection path between the RFIC antenna pins and the physical connection to the application antenna. The unbalanced RFIC 100 Ohm antenna port pins (RFP, RFN) are connected to a monolithic ceramic balun which converts the signal into 50 Ohm unbalanced. The unbalanced signal is then conducted via microstrip transmission line to a monolithic ceramic low-pass filter. The output of the low-pass filter is further conducted to the antenna port, which can be either the provided unique U.FL coaxial cable jack or a solder terminal on the edge of the module's PCB. There is a DC blocking capacitor between the balun and the low pass filter to protect the circuit from damage if a power source is inadvertently connected to the antenna circuit.

Typical antennas are low gain omni-directional, such as monopoles, dipoles and similar arrangements. An internally mounted antenna is typically provided as part of the host application hardware. An external port with a suitably unique connector can be provided for mounting situations where a provided antenna needs to be mounted in a better location.

# 5.0 Tune-Up Procedure

In general, tune-up of the AT86RF230 is pre-determined in software. Insurance that the radio device is tuned to the correct frequency and adheres to the proper output level is based on the architecture of the transceiver – including the external components - and the limits of the software. No manually variable passive components are used in the design. Variations in frequency, receive mode, and output level are determined in software through the configuration of specific register or memory locations. Register values are set prior to the execution of the main application loop.

The Atmel AT86RF230 has two receive modes of operation – Basic and Extended. The mode of receive operation commonly used by the host applications, such as the SmaRT 2.4GHz Base Unit BU-200H, is Basic Mode. To set Basic Mode of receive operation, the AT86RF230 requires that register location 0x02 be set to 0x06. The ability to change this register is not available to the end user and is pre-determined in the application code. It cannot be changed during normal use of the product.

The AT86RF230 has three transmit modes of operation – Basic, Extended and Test modes. In any mode, there are sixteen specific output power levels that can be selected – +3dBm, +2.6dBm, +2.1dBm, +1.6dBm, +1.1dBm, +0.5dBm, -0.2dBm, -1.2dBm, -2.2dBm, -3.2dBm, -4.2dBm, -5.2dBm, -7.2dBm, -9.2dBm, -12.2dBm, -17.2dBm. The host applications, such as the SmaRT 2.4GHz Base Unit BU-200H, operate in Extended transmit mode only and uses two power level settings: +3dBm and -17.2dBm. In Active Mode (application mode), the host application operates the AT86RF230 in Extended transmit mode at +3dBm whereby memory location 0x05 is set to 0x80. In Association Mode (application mode), where the communication frequency between nodes is determined, the host application operates the AT86RF230 in Extended transmit mode at -17.2dBm whereby memory location 0x05 is set to 0x8F. In either case, the modification of transmit mode and output power level is determined in software and no manual tuning is required.

The AT86RF230 is able to transmit and receive on 16 distinct frequencies - between 2405MHz to 2480MHz. Each channel is spaced by 5MHz beginning at 2405MHz. In Association Mode, the communication frequency between nodes is determined. By default, the AT86RF230 is configured to listen at 2405MHz. This is established in software by setting the bottom four bits in memory location 0x08 within the transceiver to 0x0B. During Association Mode, the user – through software – has the ability to change the communication frequency to 2410MHz, 2415MHz, 2420MHz, 2425MHz, 2430MHz, 2435MHz, 2440MHz, 2445MHz, 2450MHz, 2455MHz, 2460MHz, 2465MHz, 2470MHz, 2475MHz, or 2480MHz. The range of frequencies is limited by hardware and is a function of the circuit design and the value stored in a specific register location.

A buffered test point, pin 37, is available to measure the crystal oscillator frequency without affecting the oscillator. For all practical purposes, physical tuning is never required when the specified components are installed in the circuit. It is possible to trim the primary crystal by varying the load capacitors and/or using the RFIC's selectable internal trim capacitors, should that ever be necessary.

 

# 6.0 Labels

The RFM307 transceiver module and products the incorporate the RFM307 transceiver module must be properly labeled.

The RFM307 module must be labeled with the following statement:

| |
|---|
| Cervis SmaRT 2.4GHz Module<br><br>FCC ID: LOBSRF307 |

The product label must include the following statement:

| |
|---|
| FCC statements:<br><br>15.19 – Two Part Warning<br><br>This device complies with Part 15 of the FCC rules. Operation is subject to the following conditions:<br><br>(1) This device may not cause harmful interference and<br><br>(2) This device must accept any interference received, including interference that may cause undesired operation.<br><br>15.21 – Unauthorized Modification<br><br>NOTICE: The manufacturer is not responsible for any unauthorized modifications to this equipment made by the user. Such modifications could void the user's authority to operate this equipment.<br><br>Contains FCC ID: LOBSRF307 |

# 7.0 Specifications

### *RFM307 General Specifications*

| Item | Description |
|---|---|
| **Digital Power** | Regulated +2.7 – 3.3 VDC, 20mA max |
| **Analog Power** | Regulated +2.7 – 3.3 VDC, 20mA max |
| **Digital I/O Signals** | "CMOS" logic levels |
| **TX RF Power** | -17.2dBm to +3dBm, +/-3dBm |
| **TX RF Power Max.** | Not to exceed +6dBm |
| **Frequency Accuracy** | 2405-2480 MHz, 5 MHz channel spacing +/-100kHz |
| **Modulation** | DSSS |
| **Size** | 25mm W x 26mm H x 5mm T |
| **Connector** | U.FL female jack or PCB pad |
| **Antenna** | Low gain omni, provided as original equipment |

# 8.0 Signals and Connections

### *RFM307 Pins and Signals*

| Pin | Description |
|---|---|
| **1-16,20,22-24,28,30,31** | Ground connection |
| **32** | Digital Power input, regulated +2.7 – 3.3 VDC, 20mA max |
| **29** | Analog Power input, regulated +2.7 – 3.3 VDC, 20mA max |
| **21** | 2.4 GHz RF antenna connection (alternate to J2) |
| **34** | Serial select input, active low, 1M pullup |
| **19** | Serial clock input |
| **17** | Serial data input |
| **18** | Serial data output |
| **33** | Interrupt output, active low, 1M pullup |
| **35** | Reset input, active low, 1M pullup |
| **36** | Sleep/TR input, 1M pulldown |
| **37** | RFIC buffered clock output |
| **26** | Gain select, 1M pulldown (reserved) |
| **27** | PA enable, active high, 1M pulldown (reserved) |
| **J2** | 2.4 GHz RF antenna coax connector (alternate to pin 21) |

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SmaRT devices are manufactured by CERVIS, Inc.