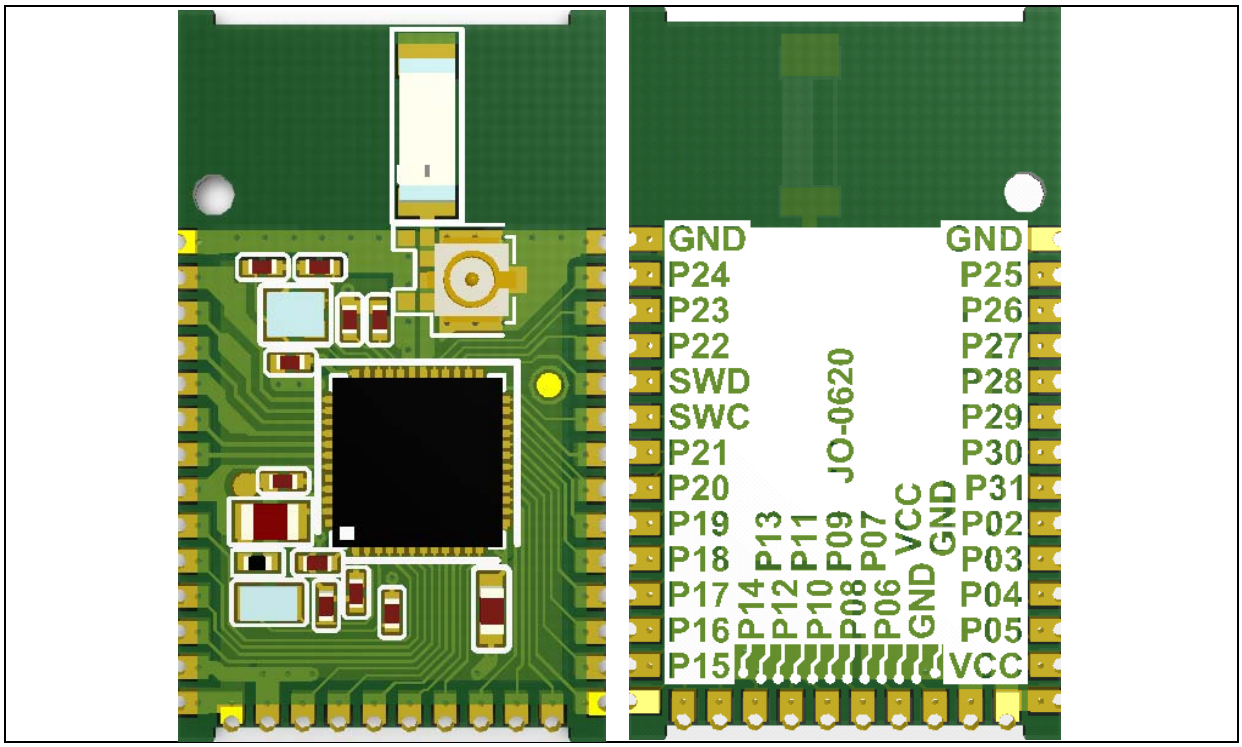
目录

FCC ID: SI8-BLE0305C2P
Product: Bluetooth Low Energy Module（BLE）
Model(s): BLE0305C2P

Revision History

Revision	Date	Description/Changes
1.0	2018-05-30	First release
		(Added / Changes / Merged / Deleted)

1. Features

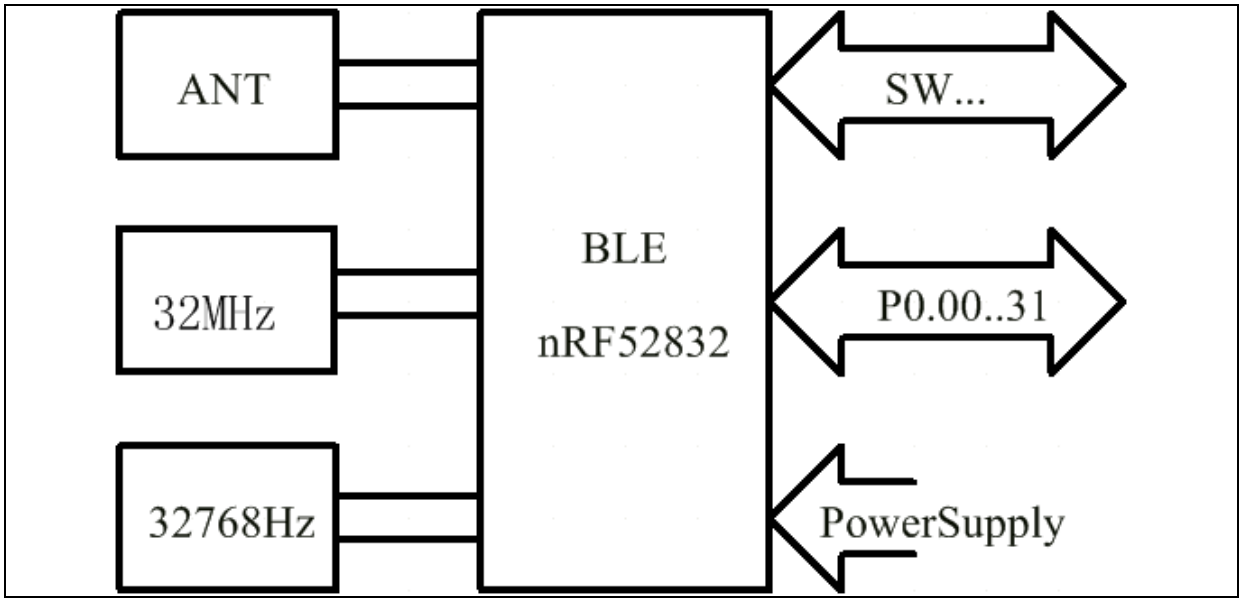


- Surface-mount, Size: 15.24mm×26.035mm = 600mil×1025mil

2. Product Description

For more information on Jinou's wireless platform solutions for Bluetooth, see Jinou's homepage (www.jinoux.com).

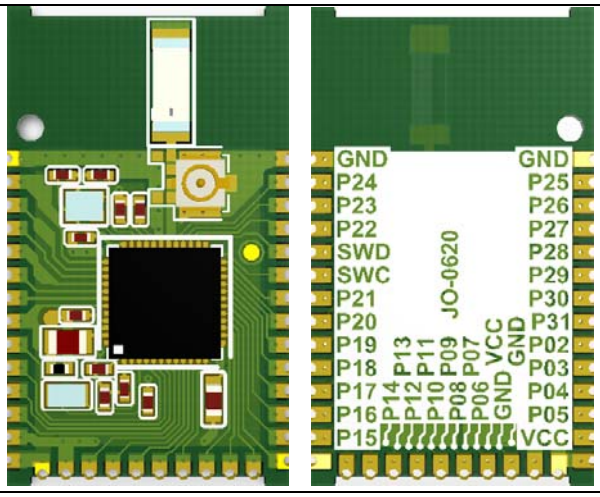
3. Block Diagram



4. Pin Descriptions

Device Terminal Functions(设备接线端列表)

序号	说明		说明	序号
1	GND		GND	38
2	P25		P24	37
3	P26		P23	36
4	P27		P22	35
5	P28		SWD	34
6	P29		SWC	33
7	P30		P21	32
8	P31		P20	31
9	P02		P19	30
10	P03		P18	29
11	P04		P17	28
12	P05		P16	27
13	VCC		P15	26
14	GND		P14	25



15	16	17	18	19	20	21	22	23	24
GND	VCC	P06	P07	P08	P09	P10	P11	P12	P13

Device Terminal Functions(设备接线端功能描述)

No.	Name	Type	Description
	P00 XL1	Digital I/O Analog input	General purpose I/O Connection for 32.768 kHz crystal (LFXO)
	P01 XL2	Digital I/O Analog input	General purpose I/O Connection for 32.768 kHz crystal (LFXO)
	P02 AIN0	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
	P03 AIN1	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
	P04 AIN2	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
	P05 AIN3	Digital I/O Analog input	General purpose I/O SAADC/COMP/LPCOMP input
	P06	Digital I/O	General purpose I/O
	P07	Digital I/O	General purpose I/O
	P08	Digital I/O	General purpose I/O
	NFC1 P09	NFC input Digital I/O	NFC antenna connection General purpose I/O**1
	NFC2 P10	NFC input Digital I/O	NFC antenna connection General purpose I/O**1
	P11	Digital I/O	General purpose I/O
	P12	Digital I/O	General purpose I/O
	P13	Digital I/O	General purpose I/O
	P14 TRACEDATA[3]	Digital I/O	General purpose I/O Trace port output
	P15 TRACEDATA[2]	Digital I/O	General purpose I/O Trace port output
	P16 TRACEDATA[1]	Digital I/O	General purpose I/O Trace port output
	P17	Digital I/O	General purpose I/O
	P18 TRACEDATA[0] / SWO	Digital I/O	General purpose I/O Trace port output / Single wire output
	P19	Digital I/O	General purpose I/O
	P20	Digital I/O	General purpose I/O

	TRACECLK		Trace port clock output
	P0.21 nRESET	Digital I/O	General purpose I/O Configurable as pin reset
	P22	Digital I/O	General purpose I/O
	P23	Digital I/O	General purpose I/O
	P24	Digital I/O	General purpose I/O
	P25	Digital I/O	General purpose I/O
	P26	Digital I/O	General purpose I/O
	P27	Digital I/O	General purpose I/O
	P0.28 AIN4	Digital I/O Analog input	General purpose I/O**2 SAADC/COMP/LPCOMP input
	P0.29 AIN5	Digital I/O Analog input	General purpose I/O**2 SAADC/COMP/LPCOMP input
	P0.30 AIN6	Digital I/O Analog input	General purpose I/O**2 SAADC/COMP/LPCOMP input
	P0.31 AIN7	Digital I/O Analog input	General purpose I/O**2 SAADC/COMP/LPCOMP input
	SWDCLK OR SWC	Digital input	Serial wire debug clock input for debug and programming
	SWDIO OR SWD	Digital I/O	Serial wire debug I/O for debug and programming
	VCC	Power	Ground
	GND	Power	Power supply

**1 See GPIO located near the radio for more information.
**2 See NFC antenna pins for more information.

1 GPIO located near the radio

Radio performance parameters, such as sensitivity, may be affected by high frequency digital I/O with large sink/source current close to the Radio power supply and antenna pins.
Table 5: GPIO recommended usage for module identify some GPIO that have recommended usage guidelines to maximize radio performance in an application.

Table 5: GPIO recommended usage for module

Recommended usage	Low drive, low frequency I/O only.
Included GPIO	P22, P23, P24, P25, P26, P27, P28, P29, P30, P31.

2 NFC antenna pins

Two physical pins can be configured either as NFC antenna pins (factory default), or as GPIOs, as shown below.

NFC pad name	GPIO
NFC1	P09
NFC2	P10

When configured as NFC antenna pins, the GPIOs on those pins will automatically be set to DISABLE state and a protection circuit will be enabled preventing the chip from being damaged in the presence of a strong NFC field. The protection circuit will short the two pins together if voltage difference exceeds approximately 2V.

For information on how to configure these pins as normal GPIOs, see NFCT — Near field communication tag on page 416 and UICR — User information configuration registers on page 54. Note that the device will not be protected against strong NFC field damage if the pins are configured as GPIO and an NFC antenna is connected to the device. The pins will always be configured as NFC pins during power-on reset until the configuration is set according to the UICR register.

These two pins will have some limitations when configured as GPIO. The pin capacitance will be higher on these pins, and there is some current leakage between the two pins if they are driven to different logical values. To avoid leakage between the pins when configured as GPIO, these GPIOs should always be at the same logical value whenever entering one of the device power saving modes. See Electrical specification.

5. Electrical Specifications

5.1. Absolute Maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

	Min	Max	Unit
Supply voltages			
VCC	-0.3	+3.9	V
GND		0	V
I/O pin voltage			
VI/O, VCC ≤3.6 V	-0.3	VCC+0.3V	V
VI/O, VCC >3.6 V	-0.3	3.9	V
NFC antenna pin current			
INFC1/2		80	mA
Radio			
RF input level		10	dBm
Storage temperature	-40	+125	℃
MSL (moisture sensitivity level)		2	
ESD HBM (human body model)		4000	V
ESD CDM (charged device model)		1000	V
Flash memory			
Endurance (Write/Erase cycles)	10000		
Retention (at 40℃)	10		years

5.2. Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
Voltage at POWER pin(VCC)	2.7	3.3	3.6	V
Voltage at digital pins(P00 - P31)	-0.3	-	VCC+0.3V	V
Abs(NFC1 - NFC2)			2	V
Operating temperature	-40	25	85	℃

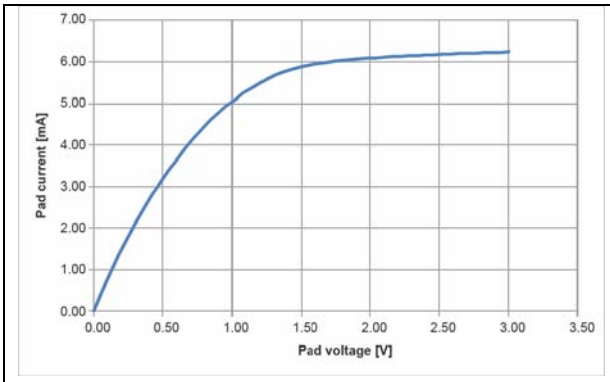
5.3. Electrical Characteristics

GPIO Electrical Specification

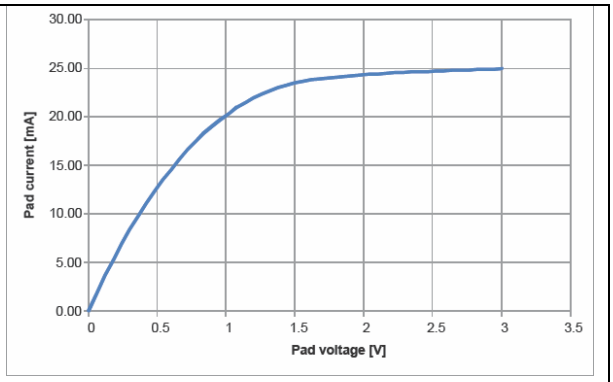
Symbol	Description	Min	Typ	Max	Units
V_{IH}	Input high voltage	0.7* VCC		VCC	V
V_{IL}	Input low voltage	GND		0.3*VCC	V
$V_{OH, HDH}$	Output high voltage, high drive, 5 mA, VCC >= 2.7 V	VCC-0.4		VCC	V
$V_{OL, HDH}$	Output low voltage, high drive, 5 mA, VCC >= 2.7 V	GND		GND+0.4	V
$I_{OL, HDH}$	Current at GND+0.4 V, output set low, high drive, VCC >= 2.7 V	6	10	15	mA
$I_{OH, HDH}$	Current at VCC-0.4 V, output set high, high drive, VCC >= 2.7 V	6	9	14	mA
$t_{RF, 15pF}$	Rise/fall time, low drive mode, 10-90%, 15 pF load1		9		nS
$t_{RF, 25pF}$	Rise/fall time, low drive mode, 10-90%, 25 pF load1		13		nS
$t_{RF, 50pF}$	Rise/fall time, low drive mode, 10-90%, 50 pF load1		25		nS
$t_{HRF, 15pF}$	Rise/Fall time, high drive mode, 10-90%, 15 pF load1		4		nS
$t_{HRF, 25pF}$	Rise/Fall time, high drive mode, 10-90%, 25 pF load1		5		nS
$t_{HRF, 50pF}$	Rise/Fall time, high drive mode, 10-90%, 50 pF load1		8		nS
R_{PU}	Pull-up resistance	11	13	16	KΩ

R_{PD}	Pull-down resistance	11	13	16	KΩ
C_{PAD}	Pad capacitance		3		pF
C_{PAD_NFC}	Pad capacitance on NFC pads		4		pF
I_{NFC_LEAK}	Leakage current between NFC pads when driven to different states		2	10	uA

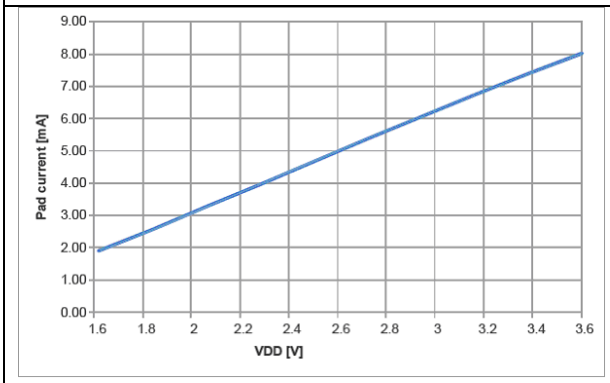
The current drawn from the battery when GPIO is active as an output is calculated as follows:
I_{GPIO}=VCC C_{load} f
C_{load} being the load capacitance and “f” is the switching frequency.



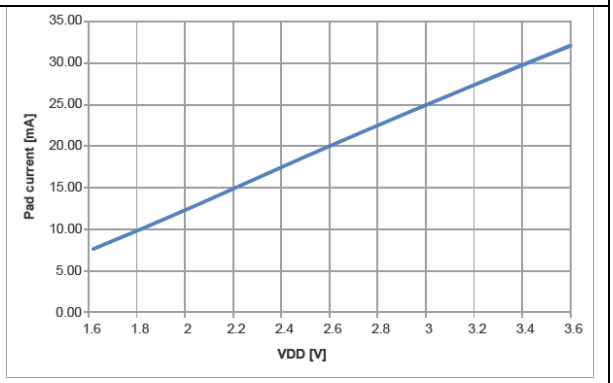
GPIO drive strength vs Voltage, standard drive, VCC = 3.0 V



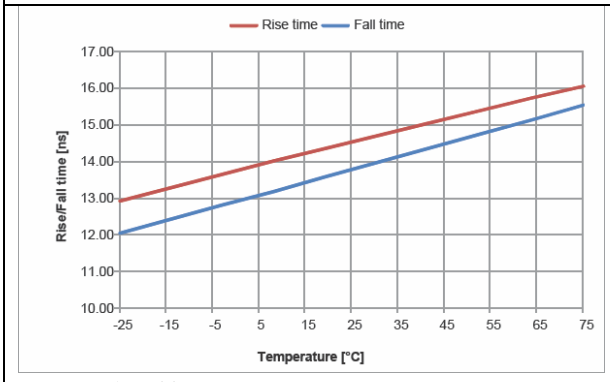
GPIO drive strength vs Voltage, high drive, VCC = 3.0 V



Max sink current vs Voltage, standard drive



Max sink current vs Voltage, high drive



Rise and fall time vs Temperature, 10%-90%, 25pF load capacitance, VCC = 3.0 V

6. Radio Characteristics

6.1. General Radio Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
f_{OP}	Operating frequencies	2360		2500	MHz
$f_{PLL, PROG, RES}$	PLL programming resolution		2		KHz
$f_{PLL, CH, SP}$	PLL channel spacing		1		MHz
$f_{DELTA, 1M}$	Frequency deviation @ 1 Msps		±170		KHz
$f_{DELTA, BLE, 1M}$	Frequency deviation @ BLE 1Msps		±250		KHz
$f_{DELTA, 2M}$	Frequency deviation @ 2 Msps		±320		KHz
$f_{DELTA, BLE, 2M}$	Frequency deviation @ BLE 2 Msps		±500		KHz
fsk_{SPS}	On-the-air data rate	1		2	Msps

6.2. Radio current consumption (Transmitter)

Symbol	Description	Min.	Typ.	Max.	Units
$I_{TX, PLUS4dBM}$	TX only run current PRF = +4 dBm		16.6		mA
$I_{TX, 0dBM}$	TX only run current PRF = 0dBm		11.6		mA
$I_{TX, MINUS4dBM}$	TX only run current PRF = -4 dBm		9.3		mA
$I_{TX, MINUS8dBM}$	TX only run current PRF = -8 dBm		8.4		mA
$I_{TX, MINUS12dBM}$	TX only run current PRF = -12 dBm		7.7		mA
$I_{TX, MINUS16dBM}$	TX only run current PRF = -16 dBm		7.3		mA
$I_{TX, MINUS20dBM}$	TX only run current PRF = -20 dBm		7.0		mA
$I_{TX, MINUS40dBM}$	TX only run current PRF = -40 dBm		5.9		mA
$I_{START, TX}$	TX start-up current, PRF = 4 dBm		8.8		mA

Symbol	Description	Min.	Typ.	Max.	Units
$I_{TX, PLUS4dBM, DCDC}$	TX only run current (DCDC, 3V) PRF =+4 dBm		7.5		mA
$I_{TX, 0dBM, DCDC}$	TX only run current (DCDC, 3V)PRF = 0dBm		5.3		mA
$I_{TX, MINUS4dBM, DCDC}$	TX only run current DCDC, 3V PRF = -4dBm		4.2		mA
$I_{TX, MINUS8dBM, DCDC}$	TX only run current DCDC, 3V PRF = -8 dBm		3.8		mA
$I_{TX, MINUS12dBM, DCDC}$	TX only run current DCDC, 3V PRF = -12 dBm		3.5		mA
$I_{TX, MINUS16dBM, DCDC}$	TX only run current DCDC, 3V PRF = -16 dBm		3.3		mA
$I_{TX, MINUS20dBM, DCDC}$	TX only run current DCDC, 3V PRF = -20 dBm		3.2		mA
$I_{TX, MINUS40dBM, DCDC}$	TX only run current DCDC, 3V PRF = -40 dBm		2.7		mA
$I_{START, TX, DCDC}$	TX start-up current DCDC, 3V, PRF = 4 dBm		4.0		mA

6.3. Radio current consumption (Receiver)

Symbol	Description	Min.	Typ.	Max.	Units
$I_{RX, 1M}$	RX only run current 1Msps / 1Msps BLE		11.7		mA
$I_{RX, 2M}$	RX only run current 2Msps / 2Msps BLE		12.9		mA
$I_{START, RX, LDO}$	RX start-up current (LDO 3V)		7.5		mA

Symbol	Description	Min.	Typ.	Max.	Units
$I_{RX, 1M, DCDC}$	RX only run current (DCDC, 3V) 1Msps / 1Msps BLE		5.4		mA
$I_{RX, 2M, DCDC}$	RX only run current (DCDC, 3V) 2Msps / 2Msps BLE		5.8		mA
$I_{START, RX, DCDC}$	RX start-up current (DCDC 3V)		3.5		mA

6.4. Transmitter specification

Symbol	Description	Min.	Typ.	Max.	Units
P_{RF}	Maximum output power		4	6	dBm
P_{RFC}	RF power control range		24		dB
P_{RFCR}	RF power accuracy			±4	dB
$P_{RF1,1}$	1st Adjacent Channel Transmit Power 1 MHz (1 Msps Nordic proprietary mode)		-25		dBc
$P_{RF2,1}$	2nd Adjacent Channel Transmit Power 2 MHz (1 Msps Nordic proprietary mode)		-50		dBc
$P_{RF1,2}$	1st Adjacent Channel Transmit Power 2 MHz (2 Msps Nordic proprietary mode)		-25		dBc
$P_{RF2,2}$	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps Nordic proprietary mode)		-50		dBc
$P_{RF1,2,BLE}$	1st Adjacent Channel Transmit Power 2 MHz (2 Msps BLE mode)		-20		dBc
$P_{RF2,2,BLE}$	2nd Adjacent Channel Transmit Power 4 MHz (2 Msps BLE mode)		-50		dBc

6.5. Receiver operation

Symbol	Description	Min.	Typ.	Max.	Units
$P_{RX,MAX}$	Maximum received signal strength at < 0.1% BER		0		dBm
$P_{SENS,IT,1M}$	Sensitivity, 1Msps nRF mode [16]		-93		dBm
$P_{SENS,IT,SP,1M,BLE}$	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER=1E-3 [17]		-96		dBm
$P_{SENS,IT,LP,1M,BLE}$	Sensitivity, 1Msps BLE ideal transmitter >=128 bytes BER=1E-4 [18]		-95		dBm
$P_{SENS,IT,2M}$	Sensitivity, 2Msps nRF mode [19]		-89		dBm
$P_{SENS,IT,SP,2M,BLE}$	Sensitivity, 2Msps BLE ideal transmitter, Packet length <=37bytes		-93		dBm
$P_{SENS,DT,SP,2M,BLE}$	Sensitivity, 2Msps BLE dirty transmitter, Packet length <=37bytes		-93		dBm
$P_{SENS,IT,LP,2M,BLE}$	Sensitivity, 2Msps BLE ideal transmitter >= 128bytes		-92		dBm
$P_{SENS,DT,LP,2M,BLE}$	Sensitivity, 2Msps BLE dirty transmitter, Packet length >= 128bytes		-92		dBm

**16 Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

**17 As defined in the Bluetooth Core Specification v4.0 Volume 6: Core System Package (Low Energy Controller Volume)

**18 Equivalent BER limit < 10E-04

**19 Typical sensitivity applies when ADDR0 is used for receiver address correlation. When ADDR[1...7] are used for receiver address correlation, the typical sensitivity for this mode is degraded by 3dB.

6.6. selectivity

RX selectivity with equal modulation on interfering signal[20]

**20 Wanted signal level at PIN = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented

Symbol	Description	Min.	Typ.	Max.	Units
$C/I_{1M,co-channel}$	1Msps mode, Co-Channel interference		9		dB
$C/I_{1M,-1MHz}$	1 Msps mode, Adjacent (-1 MHz) interference		-2		dB
$C/I_{1M,+1MHz}$	1 Msps mode, Adjacent (+1 MHz) interference		-10		dB
$C/I_{1M,-2MHz}$	1 Msps mode, Adjacent (-2 MHz) interference		-19		dB
$C/I_{1M,+2MHz}$	1 Msps mode, Adjacent (+2 MHz) interference		-42		dB
$C/I_{1M,-3MHz}$	1 Msps mode, Adjacent (-3 MHz) interference		-38		dB
$C/I_{1M,+3MHz}$	1 Msps mode, Adjacent (+3 MHz) interference		-48		dB
$C/I_{1M,\pm 6MHz}$	1 Msps mode, Adjacent (≥6 MHz) interference		-50		dB
$C/I_{1MBLE,co-channel}$	1 Msps BLE mode, Co-Channel interference		6		dB
$C/I_{1MBLE,-1MHz}$	1 Msps BLE mode, Adjacent (-1 MHz) interference		-2		dB
$C/I_{1MBLE,+1MHz}$	1 Msps BLE mode, Adjacent (+1 MHz) interference		-9		dB
$C/I_{1MBLE,-2MHz}$	1 Msps BLE mode, Adjacent (-2 MHz) interference		-22		dB
$C/I_{1MBLE,+2MHz}$	1 Msps BLE mode, Adjacent (+2 MHz) interference		-46		dB
$C/I_{1MBLE,>3MHz}$	1 Msps BLE mode, Adjacent (≥3 MHz) interference		-50		dB
$C/I_{1MBLE,image}$	Image frequency Interference		-22		dB
$C/I_{1MBLE,image,1MHz}$	Adjacent (1 MHz) interference to in-band image frequency		-35		dB
$C/I_{2M,co-channel}$	2Msps mode, Co-Channel interference		10		dB

$C/I_{2M,-2MHz}$	2 Msps mode, Adjacent (-2 MHz) interference		6		dB
$C/I_{2M,+2MHz}$	2 Msps mode, Adjacent (+2 MHz) interference		-14		dB
$C/I_{2M,-4MHz}$	2 Msps mode, Adjacent (-4 MHz) interference		-20		dB
$C/I_{2M,+4MHz}$	2 Msps mode, Adjacent (+4 MHz) interference		-44		dB
$C/I_{2M,-6MHz}$	2 Msps mode, Adjacent (-6 MHz) interference		-42		dB
$C/I_{2M,+6MHz}$	2 Msps mode, Adjacent (+6 MHz) interference		-47		dB
$C/I_{2M,\geq 12MHz}$	2 Msps mode, Adjacent (≥12 MHz) interference		-52		dB
$C/I_{2MBLE,co-channel}$	2 Msps BLE mode, Co-Channel interference		7		dB
$C/I_{2MBLE,\pm 2MHz}$	2 Msps BLE mode, Adjacent (±2 MHz) interference		0		dB
$C/I_{2MBLE,\pm 4MHz}$	2 Msps BLE mode, Adjacent (±4 MHz) interference		-47		dB
$C/I_{2MBLE,\geq 6MHz}$	2 Msps BLE mode, Adjacent (≥6 MHz) interference		-49		dB
$C/I_{2MBLE,image}$	Image frequency Interference		-21		dB
$C/I_{2MBLE,image,2MHz}$	Adjacent (2 MHz) interference to in-band image frequency		-36		dB

6.7. RX intermodulation

RX intermodulation[21]

**21 Wanted signal level at PIN = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of the interferers where the sensitivity equals BER = 0.1% is presented.

Symbol	Description	Min.	Typ.	Max.	Units
$P_{IMD,1M}$	IMD performance, 1 Msps (3 MHz, 4 MHz, and 5 MHz offset)		-33		dBm
$P_{IMD,1M,BLE}$	IMD performance, BLE 1 Msps (3 MHz, 4 MHz, and 5 MHz offset)		-30		dBm
$P_{IMD,2M}$	IMD performance, 2 Msps (6 MHz, 8 MHz, and 10 MHz offset)		-33		dBm
$P_{IMD,2M,BLE}$	IMD performance, BLE 2 Msps (6 MHz, 8 MHz, and 10 MHz offset)		-32		dBm

6.8. Radio timing

Symbol	Description	Min.	Typ.	Max.	Units
t_{TXEN}	Time between TXEN task and READY event after channel FREQUENCY configured		140		uS
$t_{TXEN,FAST}$	Time between TXEN task and READY event after channel FREQUENCY configured (Fast Mode)		40		uS
$t_{TXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX and mode is set to 1Msps		6		uS
$t_{TXDISABLE,2M}$	Time between DISABLE task and DISABLED event when the radio was in TX and mode is set to 2Msps		4		uS
t_{RXEN}	Time between the RXEN task and READY event after channel FREQUENCY configured in default mode		140		uS
$t_{RXEN,FAST}$	Time between the RXEN task and READY event after channel FREQUENCY configured in fast mode		40		uS
t_{SWITCH}	The minimum time taken to switch from RX to TX or TX to RX (channel FREQUENCY unchanged)		20		uS
$t_{RXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX		0		uS
$t_{TXCHAIN}$	TX chain delay		0.6		uS
$t_{RXCHAIN}$	RX chain delay		9.4		uS
$t_{RXCHAIN,2M}$	RX chain delay in 2Msps mode		5		uS

6.9. Received Signal Strength Indicator (RSSI) specifications

Symbol	Description	Min.	Typ.	Max.	Units
$RSSI_{ACC}$	RSSI Accuracy Valid range -90 to -20 dBm		±2		dB
$RSSI_{RESOLUTION}$	RSSI resolution		1		dB
$RSSI_{PERIOD}$	Sample period		0.25		uS

6.10. Jitter

Symbol	Description	Min.	Typ.	Max.	Units
$t_{DISABLEDJITTER}$	Jitter on DISABLED event relative to END event when shortcut between END and DISABLE is enabled.		0.25		uS
$t_{READYJITTER}$	Jitter on READY event relative to TXEN and RXEN task.		0.25		uS

6.11. Delay when disabling the RADIO

Symbol	Description	Min.	Typ.	Max.	Units
$t_{TXDISABLE,1M}$	Disable delay from TX. Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit		6		uS
$t_{RXDISABLE,1M}$	Disable delay from RX. Delay between DISABLE and DISABLED for MODE = Nrf_1Mbit and MODE = Ble_1Mbit		0		uS

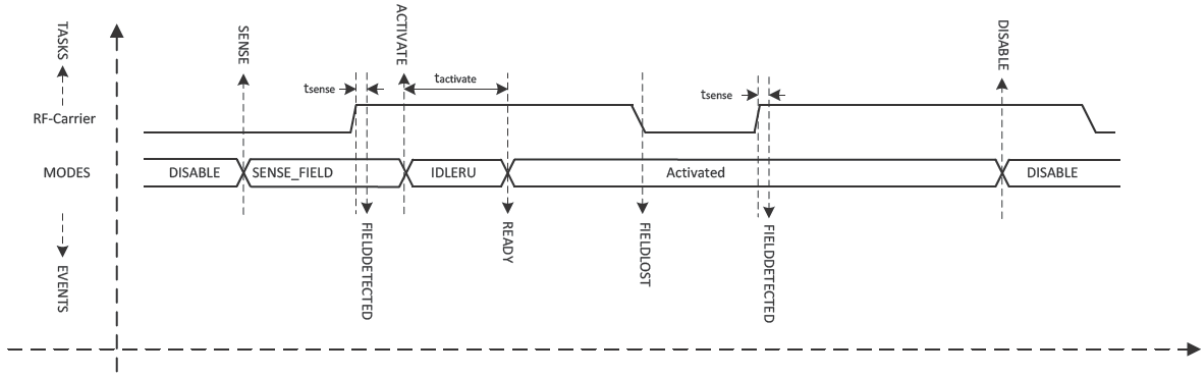
7. NFCT – Near field communication tag

7.1. NFCT Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Units
f_c	Frequency of operation		13.56		MHz
C_{MI}	Carrier modulation index	95			%
DR	Data Rate		106		Kbps
f_s	Modulation sub-carrier frequency		fc/16		MHz
V_{swing}	Peak differential Input voltage swing on NFC1 and NFC2			VCC	Vp
V_{sense}	Peak differential Field detect threshold level on NFC1-NFC2[35]		1.0		Vp
I_{sense}	Current in SENSE STATE		100		nA
$I_{activated}$	Current in ACTIVATED STATE		480		uA
R_{in_min}	Minimum input resistance when regulating voltage swing			40	Ω
R_{in_max}	Maximum input resistance when regulating voltage swing	1.0			kΩ
$R_{in\_loadmod}$	Input resistance when load modulating	8		22	Ω
I_{max}	Maximum input current on NFC pins			80	mA

7.2. NFCT Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Units
$t_{activate}$	Time from task_ACTIVATE in SENSE or DISABLE state to ACTIVATE_A or IDLE state[36]			500	uS
t_{sense}	Time from remote field is present in SENSE mode to FIELDDETECTED event is asserted			20	uS



NFCT timing parameters (Shortcuts for FIELDDETECTED and FIELDLOST are disabled)

**35 Input is high impedance in sense mode

**36 Does not account for voltage supply and oscillator startup times

8. SAADC – Successive approximation analog-todigital converter

8.1. Reference

The ADC can use two different references, controlled in the REFSEL field of the CH[n].CONFIG register. These are:

- Internal reference
- VCC as reference

The internal reference results in an input range of ±0.6 V on the ADC core. VCC as reference results in an input range of ±VCC/4 on the ADC core. The gain block can be used to change the effective input range of the ADC.

Input range = (+/- 0.6 V or +/-VDD/4)/Gain

For example, choosing VCC as reference, single ended input (grounded negative input), and a gain of 1/4 the input range will be:

Input range = (VCC/4)/(1/4) = VCC

With internal reference, single ended input (grounded negative input), and a gain of 1/6 the input range will be:

Input range = (0.6 V)/(1/6) = 3.6 V

The AIN0-AIN7 inputs cannot exceed VCC, or be lower than GND.

8.2. Acquisition time

To sample the input voltage, the ADC connects a capacitor to the input.

For illustration, see Figure 103: Simplified ADC sample network on page. The acquisition time indicates how long the capacitor is connected, see TACQ field in CH[n].CONFIG register. The required acquisition time depends on the source (Rsource) resistance. For high source resistance the acquisition time should be increased, see Table 89: Acquisition time on page.

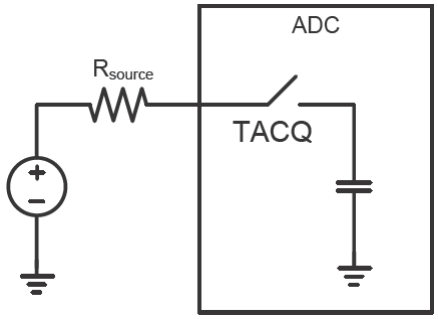


Figure 103: Simplified ADC sample network

Table 89: Acquisition time

TACQ [μs]	Maximum source resistance [kOhm]
3	10
5	40
10	100
15	200
20	400
40	800

8.3. Limits event monitoring

A channel can be event monitored by configuring limit register CH[n].LIMIT.

If the conversion result is higher than the defined high limit, or lower than the defined low limit, the appropriate event will get fired.

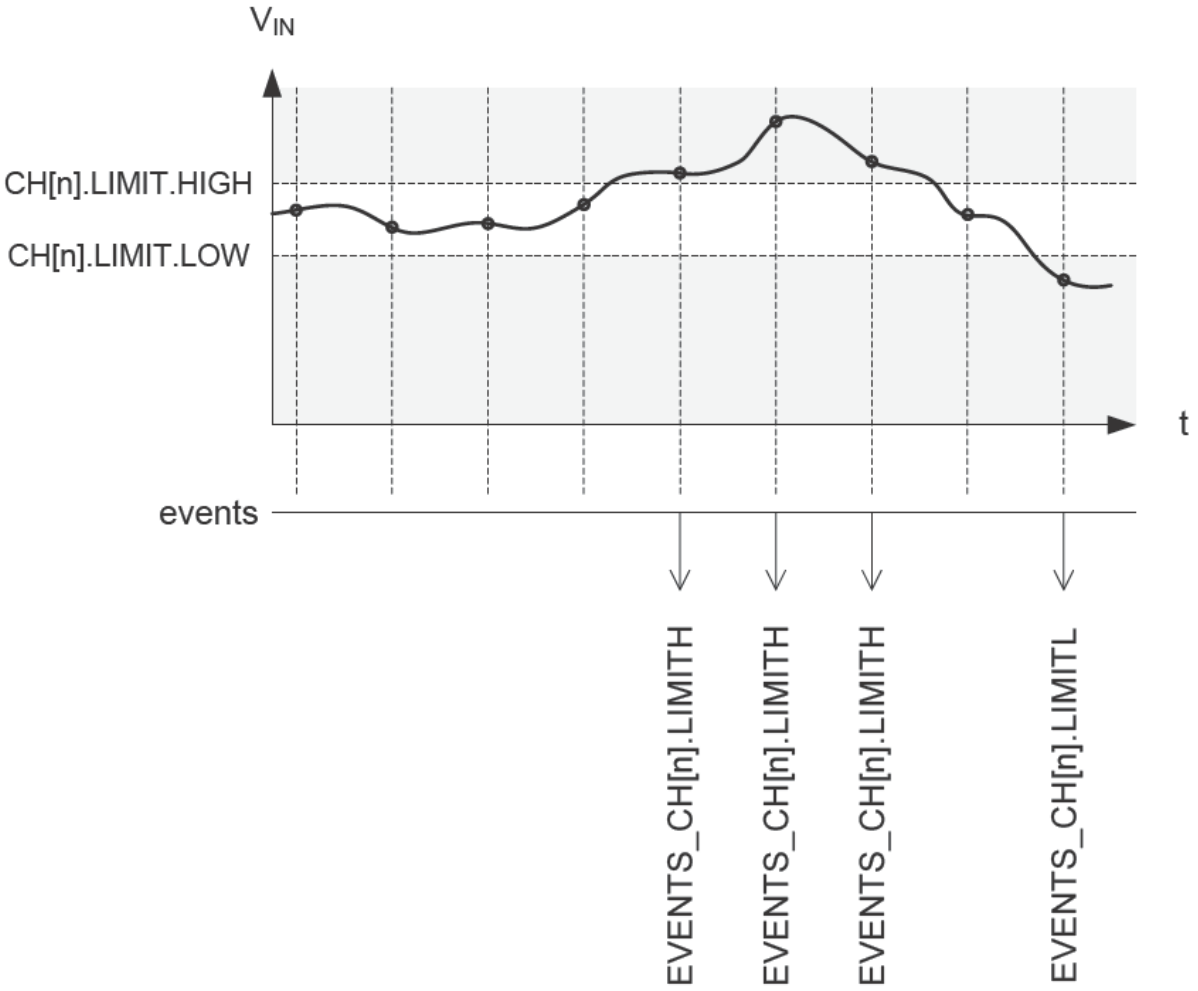


Figure 104: Example of limits monitoring on channel 'n'

Note that when setting the limits, CH[n].LIMIT.HIGH shall always be higher than or equal to CH[n].LIMIT.LOW . In other words, an event can be fired only when the input signal has been sampled outside of the defined limits. It is not possible to fire an event when the input signal is inside a defined range by swapping high and low limits.

The comparison to limits always takes place, there is no need to enable it. If comparison is not required on a channel, the software shall simply ignore the related events. In that situation, the value of the limits registers is irrelevant, so it does not matter if CH[n].LIMIT.LOW is lower than CH[n].LIMIT.HIGH or not.

8.4. SAADC Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
DNL	Differential non-linearity, 10-bit resolution	-0.95	<1		LSB
INL	Integral non-linearity, 10-bit resolution		1		LSB
V_{OS}	Differential offset error (calibrated), 10-bit resolution[a]		±2		LSB
C_{EG}	Gain error temperature coefficient		0.02		% / ℃
f_{SAMPLE}	Maximum sampling rate			200	kHz
$t_{ACQ,10k}$	Acquisition time (configurable), source Resistance <= 10kOhm		3		uS
$t_{ACQ,40k}$	Acquisition time (configurable), source Resistance <= 40kOhm		5		uS
$t_{ACQ,100k}$	Acquisition time (configurable), source Resistance <= 100kOhm		10		uS
$t_{ACQ,200k}$	Acquisition time (configurable), source Resistance <= 200kOhm		15		uS
$t_{ACQ,400k}$	Acquisition time (configurable), source Resistance <= 400kOhm		20		uS
$t_{ACQ,800k}$	Acquisition time (configurable), source Resistance <= 800kOhm		40		uS
t_{CONV}	Conversion time		<2		uS
$I_{ADC,CONV}$	ADC current during ACQuisition and CONVersion		700		uA

$I_{ADC, IDLE}$	Idle current, when not sampling, excluding clock sources and regulator base currents33		<5		uA
$E_{G1/6}$	Errorb for Gain = 1/6	-3		3	%
$E_{G1/4}$	Errorb for Gain = 1/4	-3		3	%
$E_{G1/2}$	Errorb for Gain = 1/2	-3		4	%
E_{G1}	Errorb for Gain = 1	-3		4	%
C_{SAMPLE}	Sample and hold capacitance at maximum gain[34]		2.5		pF
R_{INPUT}	Input resistance		>1		MΩ
E_{NOB}	Effective number of bits, differential mode, 12-bit resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200 ksps		9		Bit
S_{NDR}	Peak signal to noise and distortion ratio, differential mode, 12-bit resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200ksps		56		dB
S_{FDR}	Spurious free dynamic range, differential mode, 12-bit resolution, 1/1 gain, 3 μs acquisition time, crystal HFCLK, 200 ksps		70		dBc
R_{LADDER}	Ladder resistance		160		kΩ

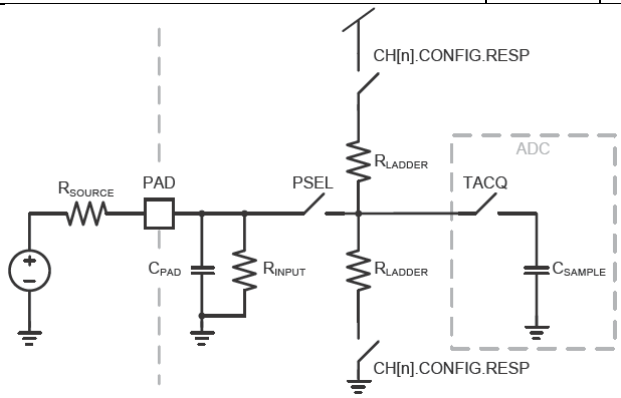


Figure 105: Model of SAADC input (one channel)

Note: SAADC average current calculation for a given application is based on the sample period, conversion and acquisition time (t_{conv} and t_{ACQ}) and conversion and idle current ($I_{ADC, CONV}$ and $I_{ADC, IDLE}$). For example, sampling at 4kHz gives a sample period of 250 μs. The average current consumption would then be:

$$I_{AVERAGE} = \left(\frac{(t_{CONV} + t_{ACQ})}{250}\right)(I_{ADC,CONV}) + \left(\frac{250 - (t_{CONV} + t_{ACQ})}{250}\right)(I_{ADC,IDLE})$$

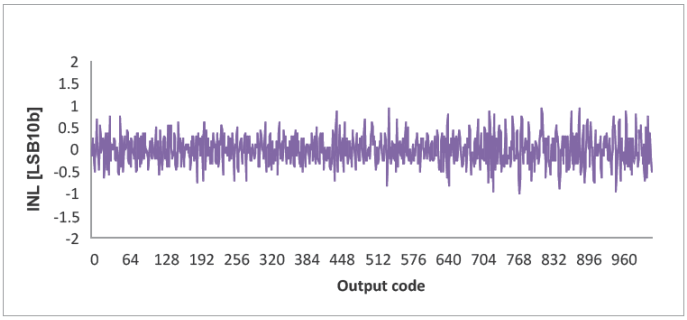


Figure 106: ADC INL vs Output Code

**a Digital output code at zero volt differential input.

**33 When tACQ is 10us or longer, and if DC/DC is active, it will be allowed to work in refresh mode if no other resource is requiring a high quality power supply from 1V3. If tACQ is smaller than 10us and DC/DC is active, refresh mode will not be allowed, and it will remain in normal mode from the START task to the STOPPED event. So depending on tACQ and other resources' needs, the appropriate base current needs to be taken into account.

**b Does not include temperature drift

**34 Maximum gain corresponds to highest capacitance.

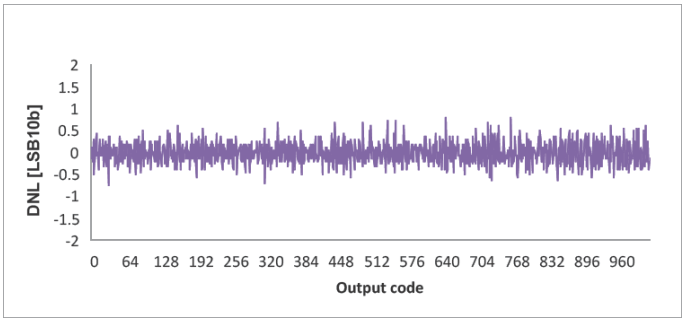


Figure 107: ADC DNL vs Output Code

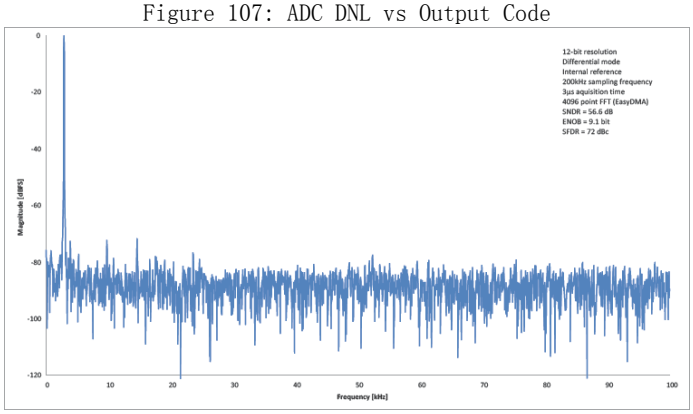
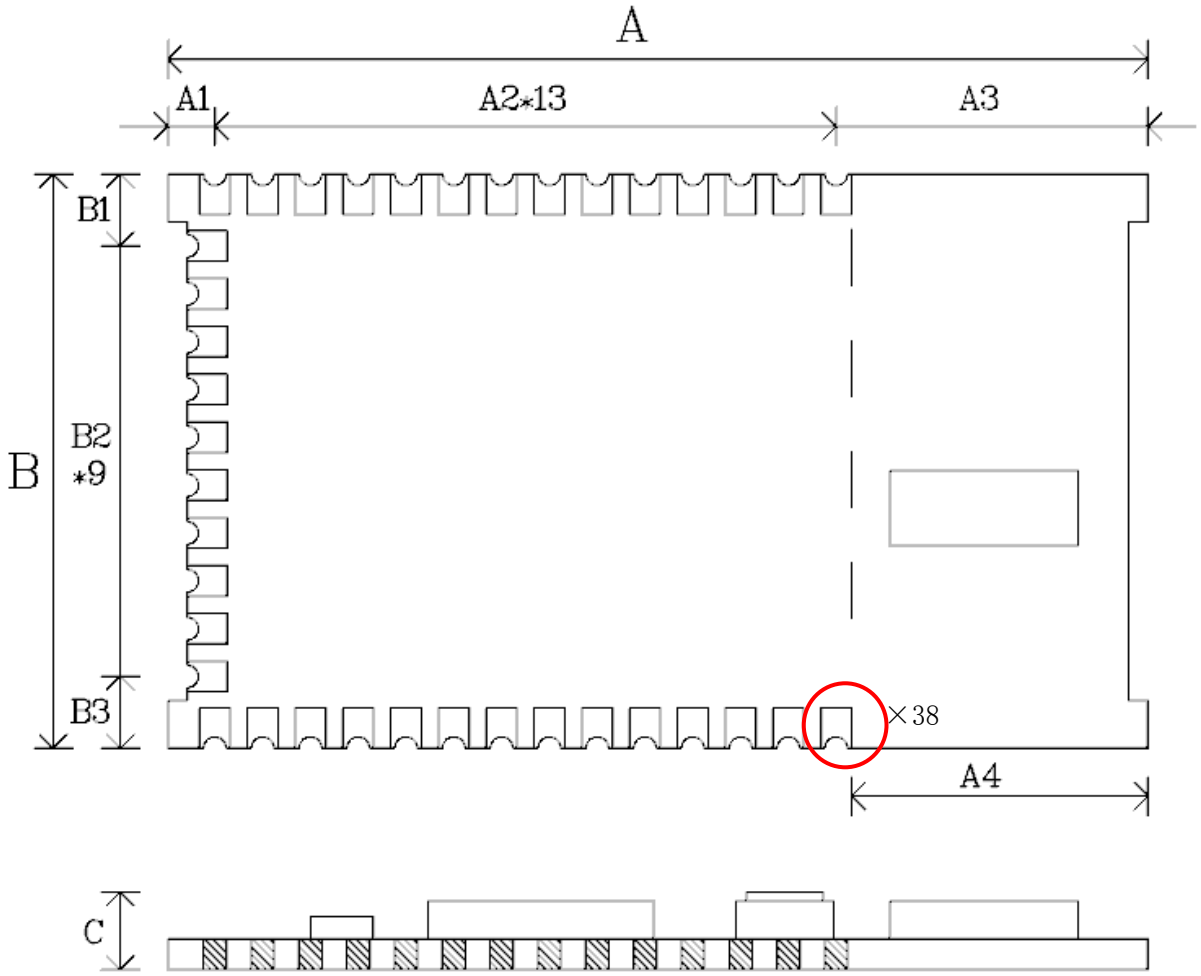
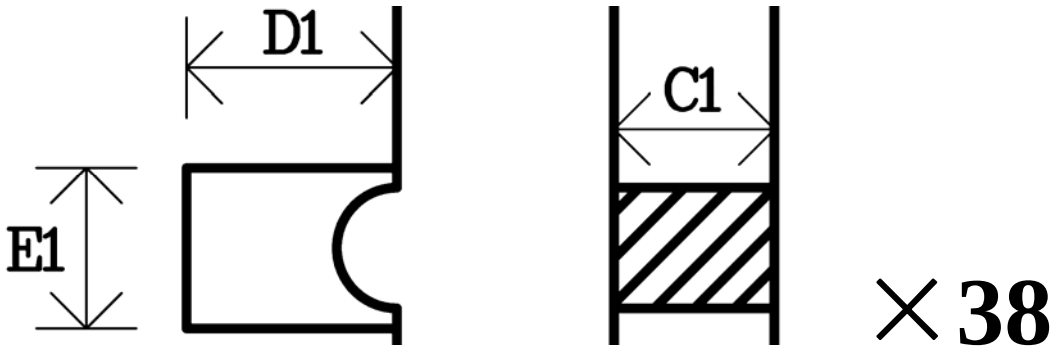


Figure 108: FFT of a 2.8 kHz sine at 200 ksps ()

9. Physical Dimensions



A	A1	A2	A3	A4	B	B1	B2	B3	C	Unit
1025	50	50	325	310	600	75	50	75	80	mil
26.035	1.27	1.27	8.255	7.874	15.24	1.905	1.27	1.905	2.286	mm



C1	D1	E1								Unit
32	42	32								mil
0.8128	1.0668	0.8128								mm

10. Solder Profiles

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow. There are four zones:

1. Preheat Zone - This zone raises the temperature at a controlled rate, typically 1-2.5° C/s.

2. Equilibrium Zone - This zone brings the board to a uniform temperature and also activates the flux.

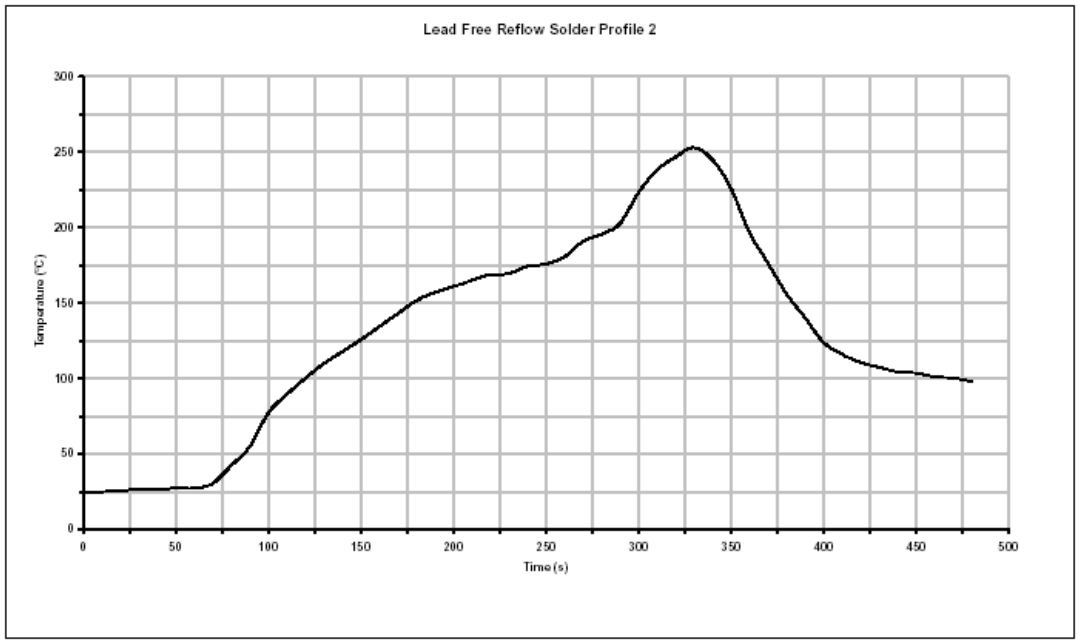
The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.

3. Reflow Zone - The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.

4. Cooling Zone - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5° C/s.

10.1. Solder Re-Flow Profile for Devices with Lead-Free Solder Balls

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%



Typical Lead-Free Re-flow Solder Profile

Key features of the profile:

- Initial Ramp = 1-2.5° C/sec to 175° C±25° C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250° C) = 3° C/sec max.
- Time above liquidus temperature (217° C): 45-90 seconds
- Device absolute maximum reflow temperature: 260° C

Devices will withstand the specified profile. Lead-free devices will withstand up to three reflows to a maximum temperature of 260° C.

Notes：They need to be baked prior to mounting。

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Modular Approval:
The BLE0305C2P module is designed to comply with the FCC statement. FCC ID is SI8-BLE0305C2P. The host system using BLE0305C2P, should have label indicated it contain modular' s FCC ID SI8-BLE0305C2P.

RF warning for Mobile device:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

15.19 Labelling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

15.21 Information to user.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by Chongqing JINOU Science and Technology Development Co., Ltd.

turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed
IMPORTANT NOTE: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.