UHF Narrow band multi channel transceiver
LMD-400-R 458-462.5 MHz

Operation Guide

Version 0.9 (Sept.2009)

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GENERAL DESCRIPTION & FEATURES

General Description

The LMD-400-R (458-462.5MHz) is a synthesized multi channel transceiver module for use under the FCC Part 90 Private Land Mobile Radio (PLMR) services. This simple, compact   and low power transceiver is designed for embedding in user equipment and suitable for various low power industrial telecontrol and telemetry applications requiring high performance and reliability.

All high frequency circuits are enclosed inside a robust housing to provide superior resistance against shock and vibration. Using a TCXO as the reference oscillator circuit of the radio component ensures high frequency stability in the temperature range from –20 to +60 °C.

Features

- ➢ Programmable RF channel with 12.5 kHz channel space
- ➢ 10 mW, GFSK, 4800 bps
- ➢ Low power operation 3- 5.5V, 50mA/TX, 32mA/RX
- ➢ Small size 50 x 30 x 9 mm
- ➢ Excellent mechanical durability, high vibration & shock resistance
- ➢ Wide operation range – 20 to +60 degree C
- ➢ FCC part 90 certified

Applications

- ➢ Industrial remote control / Telemetry
- ➢ Remote monitoring / Security

CIRCUIT DESIGN, INC.

SPECIFICATIONS

LMD-400-R 458-462.5 MHz

All ratings at 25 +/-10 °C unless otherwise noted

General characteristics

Item	Units	MIN	TYP	MAX	Remarks
Applicable standard		FCC Part 90.267			
Communication method		Simplex, Half-duplex			
Emission class		F1D			
Operating frequency range	MHz	458.000		462.500	
Operation temperature range	°C	-20		60	No dew condensation
Storage temperature range	°C	-30		75	No dew condensation
Aging rate	ppm	-1		1	TX freq., RX Lo freq.
Initial frequency tolerance	ppm	-1.5		1.5	TX freq., RX Lo freq.
Dimensions	mm	30 x 50 x 9 mm			Not including antenna
Weight	g	25 g			

Electrical specification <Common>

Item		MIN	TYP	MAX	Remarks
Oscillation type		PLL controlled VCO			
Frequency stability (-20 to 60°C)	ppm	-2.5		2.5	Reference frequency at 25 °C
TX/RX switching time	ms		15	20	DI/DO
Channel step	kHz		12.5		
Data rate	bps	2400		4800	DO/DI
Max. pulse width	ms		15	20	DO/DI
Min. pulse width	us	200			DO/DI
Data polarity		Positive			DO/DI
PLL reference frequency	MHz		21.25		TCXO
PLL response	ms		30	60	from PLL setting to LD out
Antenna impedance	Ω		50		Nominal
Operating voltage	V	3.0		5.5	
TX consumption current	mA		52		Vcc = 3.0 V
RX consumption current	mA		42		Vcc = 3.0 V

Transmitter part

Item		MIN	TYP	MAX	Remarks
RF output power	mW	7.2	10	14	Conducted 50 Ω
Deviation	kHz	+/-2.0	+/-2.4	+/-2.8	PN9 4800 bps
DI input level	V	0		5.5	L= GND, H = 3 V- Vcc
Residual FM noise	kHz		0.08		DI=L, LPF=20 kHz
Spurious emission	dBm			-37	< 1000 MHz, conducted 50 Ω
				-31	> 1000 MHz, conducted 50 Ω
Adjacent CH power	nW			200	PN9 4800

Receiver part

Item		MIN	TYP	MAX	Remarks
Receiver type			Double superheterodyne		
1st IF frequency	MHz		21.7		
2nd IF frequency	kHz		450		
Maximum input level	dBm			10	
BER (0 error/2556 bits) [1]	dBm		-113		PN 9 4800bps
BER (1 % error) [2]	dBm		-116		PN 9 4800bps
Sensitivity 12dB/ SINAD	dBm		-116		fm1 k/ dev 2.4 kHz CCITT
Co-channel rejection	dB		-7		D/U ratio
Spurious response rejection [3]	dB		70		1 st Mix, 2 signal method, 1 % error
			70		2 nd Mix, 2 signal method, 1 % error
Adjacent CH selectivity [3]	dB		65		25 kHz ch, 2 signal method, 1 % error
			55		12.5 kHz ch, 2 signal method, 1 % error
Blocking	dB		840		Unwanted signal +/-1M, 2 signal method, 1 % error
DO output level	V			2.8	L = GND H = 2.8 V
RSSI rising time	ms		30	50	CH shift of 25 kHz (from PLL setup)
			50	70	When power ON (from PLL setup)
Time until valid Data-out [4]	ms		50	100	CH shift of 25 kHz (from PLL setup)
			70	120	When power ON (from PLL setup)
Spurious radiation (1st Lo)	dBm		-60	-57	Conducted 50 Ω
RSSI	mV	240	290	340	With −100 dBm
		170	220	270	Wih −110 dBm

Specifications are subject to change without prior notice

Notice
- The time required until a stable DO is established may get longer due to the possible frequency drift caused by operation environment changes, especially when switching from TX to RX, from RX to TX and changing channels. Please make sure to optimize the timing. The recommended preamble is more than 20 ms.
- Antenna connection is designed as pin connection.
- RF output power, sensitivity, spurious emission and spurious radiation levels may vary with the pattern used between the RF pin and the coaxial connection. Please make sure to verify those parameters before use.
- The feet of the shield case should be soldered to the wide GND pattern to avoid any change in characteristics.
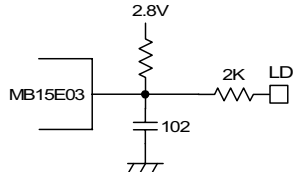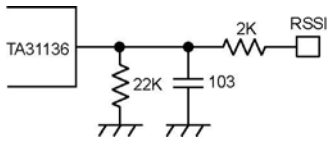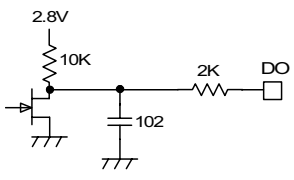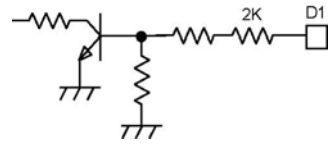
Notes about the specification values
*1 BER: RF level where no error per 2556 bits is confirmed with the signal of PN9 and 4800 bps.
*2 BER (1 % error) : RF level where 1% error per 2556 bits is confirmed with the signal of PN9 and 4800 bps.
*3 Spurious response, CH selectivity: The deviation of the unwanted signal is 12% of the channel separation (=1.5kHz). Modulation frequency is 400Hz.
*4 Time until valid Data-out : Valid DO is determined at the point where Bit Error Rate meter starts detecting the signal of 4800 bps, 1010repeated signal.

All specifications are specified based on the data measured in a shield room using the PLL setting controller board prepared by Circuit Design.

PIN DESCRIPTION

Pin name	I/O	Description	Equivalent circuit
RF	I/O	RF input terminal Antenna impedance nominal 50 Ω	
GND	I	GROUND terminal The GND pins and the feet of the shield case shoud be connected to the wide GND pattern.	
VCC	I	Power supply terminal DC 3.0 to 5.5 V	
TXSEL	I	TX select terminal GND = TXSEL active To enable the transmitter circuits, connect TXSEL to GND and RXSEL to OPEN or 2.8 V.	
RXSEL	I	RX select terminal GND= RXSEL active To enable the receiver circuits, connect RXSEL to GND and TXSEL to OPEN or 2.8 V.	
AF	O	Analogue output terminal There is DC offset of approx. 1 V. Refer to the specification table for amplitude level.	
CLK	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	
DATA	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	
LE	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	

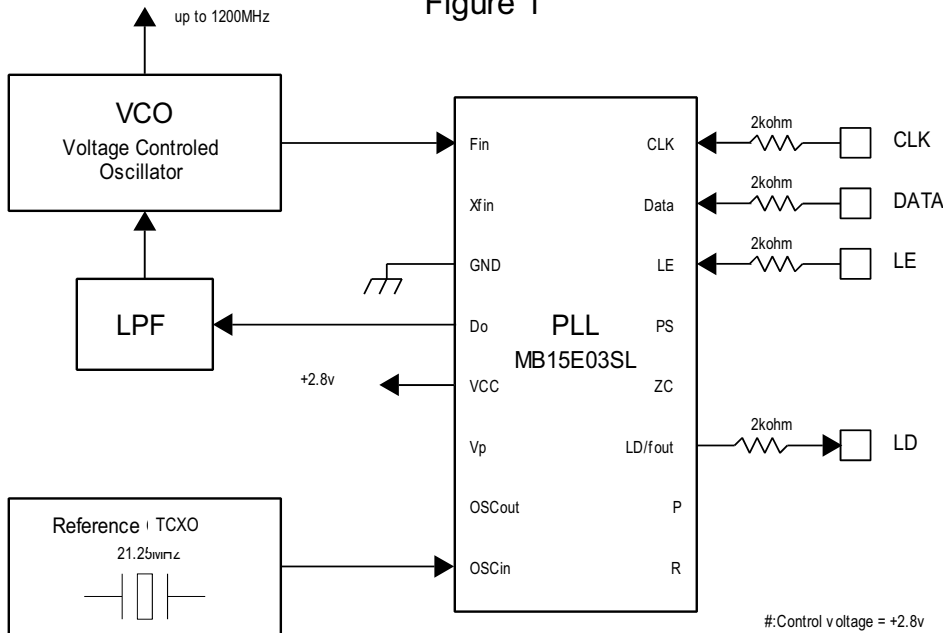| LD	O	PLL lock/unlock monitor terminal Lock = H (2.8 V), Unlock = L (0 V)	
RSSI	O	Received Signal Strength Indicator terminal	
DO	O	Data output terminal Interface voltage: H=2.8V, L=0V	
DI	I	Data input terminal Interface voltage: H=2.8V to Vcc, L=0V Input data pulse width Min.100 µs Max. 15 ms	

DIMENSIONS
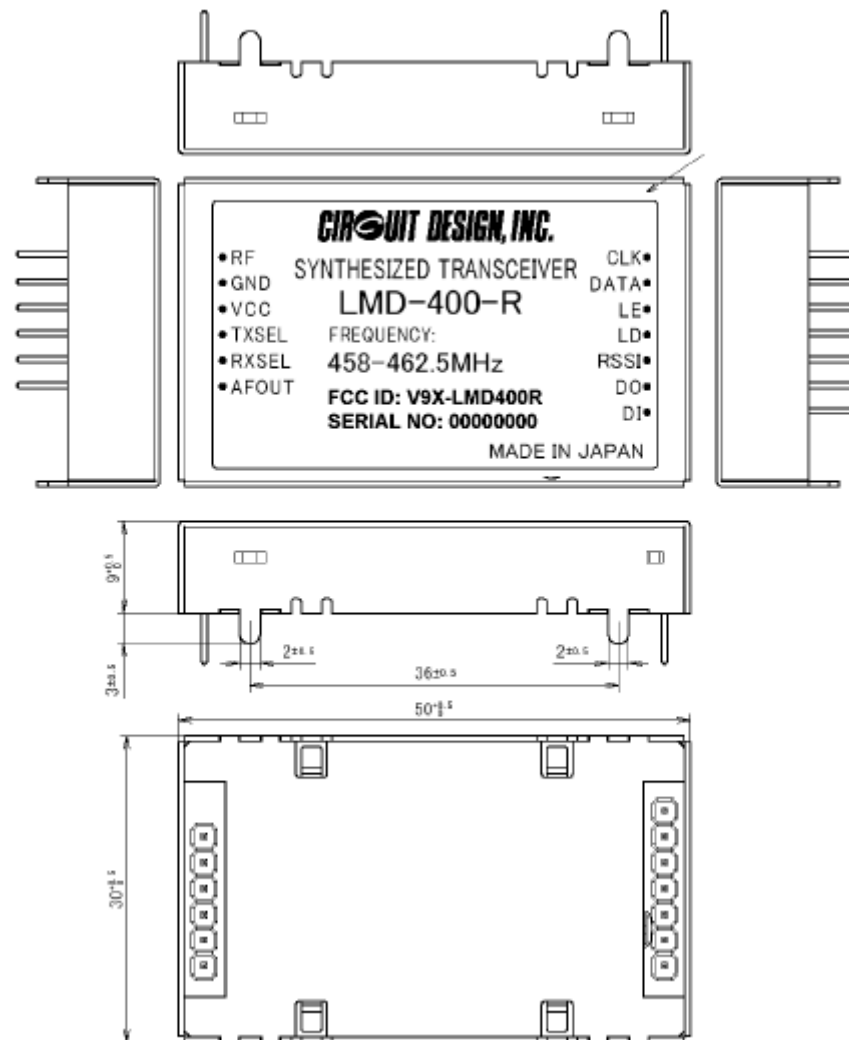
PLL IC CONTROL

● **PLL IC control**

Figure 1

LMD-400-R is equipped with an internal PLL frequency synthesizer as shown in Figure 1. The operation of the PLL circuit enables the VCO to oscillate at a stable frequency. Transmission frequency is set externally by the controlling IC. LMD-400-R has control terminals (CLK, LE, DATA) for the PLL IC and the setting data is sent to the internal register serially via the data line. Also LMD-400-R has a Lock Detect (LD) terminal that shows the lock status of the frequency. These signal lines are connected directly to the PLL IC through a 2 kΩ resistor.

The interface voltage of LMD-400-R is 2.8 V, so the control voltage must be the same.
LMD-400-R comes equipped with a Fujitsu MB15E03SL PLL IC. Please refer to the manual of the PLL IC.

The following is a supplementary description related to operation with LMD-400-R. In this description, the same names and terminology as in the PLL IC manual are used, so please read the manual beforehand.

● **How to calculate the setting values for the PLL register**

The PLL IC manual shows that the PLL frequency setting value is obtained with the following equation.
f_{vco} = [(M x N)+A] x f_{osc} / R   -- Equation 1
f_{vco} : Output frequency of external VCO
M: Preset divide ratio of the prescaler (64 or 128)
N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter (0 ≤ A ≤ 127 A<N))
f_{osc}: Output frequency of the reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

With LMD-400-R, there is an offset frequency (f_{offset}) 21.7 MHz for the transmission RF channel frequency f_{ch}. Therefore the expected value of the frequency generated at VCO (f_{expect}) is as below.
$f_{vco} = f_{expect} = f_{ch} - f_{offset}$ ---- Equation 2

The PLL internal circuit compares the phase to the oscillation frequency f_{vco}. This phase comparison frequency (f_{comp}) must be decided. f_{comp} is made by dividing the frequency input to the PLL from the reference frequency oscillator by reference counter R. LMD-400-R uses 21.25 MHz for the reference clock f_{osc}. f_{comp} is one of 6.25 kHz, 12.5 kHz or 25 kHz.

The above equation 1 results in the following with n = M x N + A, where "n" is the number for division.
$f_{vco}=n*f_{comp}$ ---- Equation 3   n = f_{vco}/f_{comp} ---- Equation 4   note: $f_{comp} = f_{osc}/R$

Also, this PLL IC operates with the following R, N, A and M relational expressions.
R=f_{osc}/f_{comp} ---- Equation 5   N = INT (n / M) ---- Equation 6   A = n - (M x N) ---- Equation 7
                                        INT: integer portion of a division.

As an example, the setting value of RF channel frequency f_{ch} 461.0375 MHz can be calculated as below.
The constant values depend on the electronic circuits of LMD-400-R.
        Conditions: Channel center frequency: f_{ch} = 460.525 MHz
                          Constant: Offset frequency: f_{offset}=21.7 MHz
                          Constant: Reference frequency: f_{osc}=21.25 MHz
                          Set 25 kHz for Phase comparison frequency and 64 for Prescaler value M

The frequency of VCO will be
$f_{vco} = f_{expect} = f_{ch} - f_{offset}$ = 460.525 –21.7 = 438.825 MHz
Dividing value "n" is derived from Equation 4
n = f_{vco} / f_{comp} = 438.825 MHz/25 kHz = 17553
Value "R" of the reference counter is derived from Equation 5.
R = f_{osc}/f_{comp} = 21.25 MHz/25 kHz = 850
Value "N" of the programmable counter is derived from Equation 6.
N = INT (n/M) = INT(17553/64) = 274
Value "A" of the swallow counter is derived from Equation 7.
A = n – (M x N) =17553 – 64 x 274 = 17

The frequency of LMD-400-R is locked at a center frequency f_{ch} by inputting the PLL setting values N, A and R obtained with the above equations as serial data. The above calculations are the same for the other frequencies.
Excel sheets that contain automatic calculations for the above equations can be found on our web site (www.cdt21.com/).

The result of the calculations is arranged as a table in the CPU ROM. The table is read by the channel change routine each time the channel is changed, and the data is sent to the PLL.
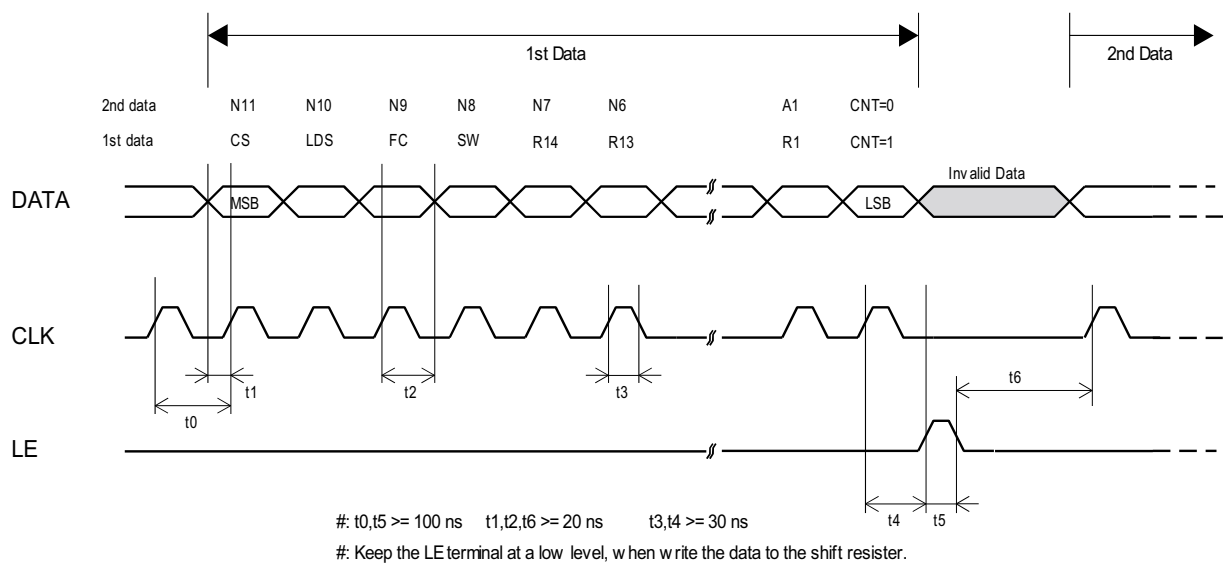
● **Method of serial data input to the PLL**

After the RF channel table plan is decided, the data needs to be allocated to the ROM table and read from there or calculated with the software.
Together with this setting data, operation bits that decide operation of the PLL must be sent to the PLL.
The operation bits for setting the PLL are as follows. These values are placed at the head of the reference counter value and are sent to the PLL.

1. CS: Charge pump current select bit
   CS = 0   +/-1.5 mA select   VCO is optimized to +/-1.5 mA
2. LDS: LD/fout output setting bit
   LDS = 0   LD select   Hardware is set to LD output
3. FC: Phase control bit for the phase comparator
   FC = 1   Hardware operates at this phase

Figure 2

#: t0,t5 >= 100 ns   t1,t2,t6 >= 20 ns   t3,t4 >= 30 ns
#: Keep the LE terminal at a low level, when write the data to the shift resister.

The PLL IC, which operates as shown in the block diagram in the manual, shifts the data to the 19-bit shift register and then transfers it to the respective latch (counter, register) by judging the CNT control bit value input at the end.

1. CLK [Clock]: Data is shifted into the shift register on the rising edge of this clock.
2. LE [Load Enable]: Data in the 19-bit shift register is transferred to respective latches on the rising edge of the clock. The data is transferred to a latch according to the control bit CNT value.
3. Data [Serial Data]: You can perform either reference counter setup or programmable counter setup first.

TIMING CHART

Control timing in a typical application is shown in Figure 3.
Initial setting of the port connected to the radio module is performed when power is supplied by the CPU and reset is completed. MOS-FET for supply voltage control of the radio module, RXSEL and TXSEL are set to inactive to avoid unwanted emissions. The power supply of the radio module is then turned on. When the radio module is turned on, the PLL internal resistor is not yet set and the peripheral VCO circuit is unstable. Therefore data transmission and reception is possible 40 ms after the setting data is sent to the PLL at the first change of channel, however from the second change of channel, the circuit stabilizes within 20 ms and is able to handle the data.
Changing channels must be carried out in the receive mode. If switching is performed in transmission mode, unwanted emission occurs.

If the module is switched to the receive mode when operating in the same channel, (a new PLL setting is not necessary) it can receive data within 5 ms of switching[1]. For data transmission, if the RF channel to be used for transmission is set while still in receiving mode, data can be sent at 5 ms after the radio module is switched from reception to transmission[2].
Check that the Lock Detect signal is "high" 20 ms after the channel is changed. In some cases the Lock Detect signal becomes unstable before the lock is correctly detected, so it is necessary to note if processing of the signal is interrupted. It is recommended to observe the actual waveform before writing the process program.

[1] DC offset may occur due to frequency drift caused by ambient temperature change. Under conditions below -10 °C, 10 to 20 ms delay of DO output is estimated. The customer is urged to verify operation at low temperature and optimize the timing.

[2] Sending '10101…..' preamble just after switching to transmission mode enables smoother operation of the binarization circuit of the receiver. Preamble length: -20 °C - +60 °C: 15 ms (Typical)

Figure 3: Timing diagram for LMD-400
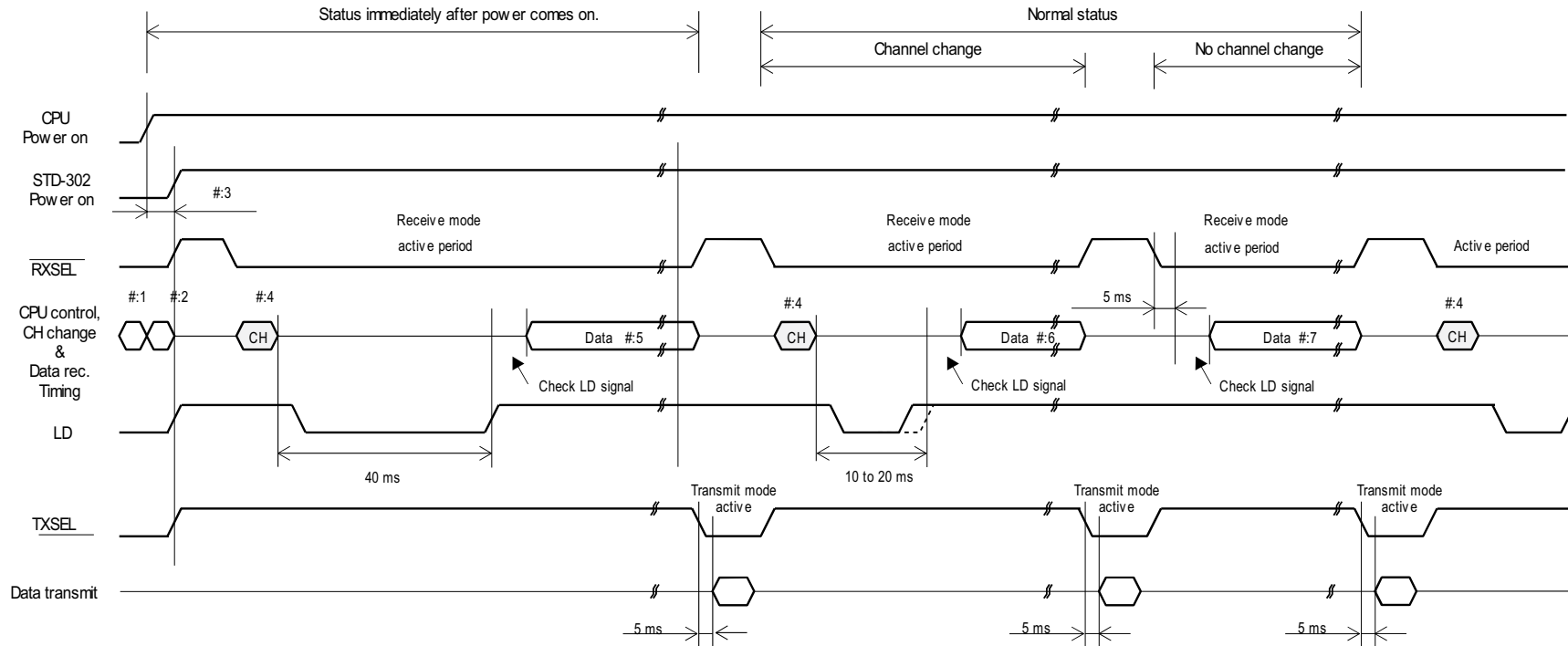
#:1 Reset control CPU

#:2 Initialize the port connected to the module.

#:3 Supply power to the module after initializing CPU.

#:4 RFchannel change must be performed in receiving mode.

#:5 40 ms later, the receiver can receive the data after changing the channel..

#:6 10 to 20 ms later, the receiver can receive the data after changing the channel.

#:7 5 ms later, the data can be received if the RF channel is not changed.

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PLL FREQUENCY SETTING DATA REFERENCE

Example : Setting from 458.000 MHz to 458.6125 MHz

Parameter name	Value
Phase Comparing Frequency F_{comp} [kHz]	25
Start Channel Frequency F_{ch} [MHz]	458.000
Channel Step Frequency [kHz]	12.5
Number of Channel	50
Prescaler M	64

■ : For data input
■ : Result of calculation
■ : Fixed value

Parameter name	Value
Reference Counter R	850
Programmable Counter N Min. Value	272
Programmable Counter N Max. Value	273
Swallow Counter A Min. Value	0
Swallow Counter A Max. Value	63

Parameter name	Value
Reference Frequency F_{osc} [MHz]	21.25
Offset Frequency F_{offset} [MHz]	21.7

Channel Frequency FCH (MHz)	Expect Frequency FEXPECT (MHz)	Lock Frequency FVCO (MHz)	Number of Division n	Programable Counter N	Swallow Counter A
458.0000	436.3000	436.3000	17452	272	44
458.0125	436.3125	436.3000	17452	272	44
458.0250	436.3250	436.3250	17453	272	45
458.0375	436.3375	436.3250	17453	272	45
458.0500	436.3500	436.3500	17454	272	46
458.0625	436.3625	436.3500	17454	272	46
458.0750	436.3750	436.3750	17455	272	47
458.0875	436.3875	436.3750	17455	272	47
458.1000	436.4000	436.4000	17456	272	48
458.1125	436.4125	436.4000	17456	272	48
458.1250	436.4250	436.4250	17457	272	49
458.1375	436.4375	436.4250	17457	272	49
458.1500	436.4500	436.4500	17458	272	50
458.1625	436.4625	436.4500	17458	272	50
458.1750	436.4750	436.4750	17459	272	51
458.1875	436.4875	436.4750	17459	272	51
458.2000	436.5000	436.5000	17460	272	52
458.2125	436.5125	436.5000	17460	272	52
458.2250	436.5250	436.5250	17461	272	53
458.2375	436.5375	436.5250	17461	272	53
458.2500	436.5500	436.5500	17462	272	54
458.2625	436.5625	436.5500	17462	272	54
458.2750	436.5750	436.5750	17463	272	55
458.2875	436.5875	436.5750	17463	272	55
458.3000	436.6000	436.6000	17464	272	56
458.3125	436.6125	436.6000	17464	272	56
458.3250	436.6250	436.6250	17465	272	57
458.3375	436.6375	436.6250	17465	272	57
458.3500	436.6500	436.6500	17466	272	58
458.3625	436.6625	436.6500	17466	272	58
458.3750	436.6750	436.6750	17467	272	59

458.3875	436.6875	436.6750	17467	272	59
458.4000	436.7000	436.7000	17468	272	60
458.4125	436.7125	436.7000	17468	272	60
458.4250	436.7250	436.7250	17469	272	61
458.4375	436.7375	436.7250	17469	272	61
458.4500	436.7500	436.7500	17470	272	62
458.4625	436.7625	436.7500	17470	272	62
458.4750	436.7750	436.7750	17471	272	63
458.4875	436.7875	436.7750	17471	272	63
458.5000	436.8000	436.8000	17472	273	0
458.5125	436.8125	436.8000	17472	273	0
458.5250	436.8250	436.8250	17473	273	1
458.5375	436.8375	436.8250	17473	273	1
458.5500	436.8500	436.8500	17474	273	2
458.5625	436.8625	436.8500	17474	273	2
458.5750	436.8750	436.8750	17475	273	3
458.5875	436.8875	436.8750	17475	273	3
458.6000	436.9000	436.9000	17476	273	4
458.6125	436.9125	436.9000	17476	273	4

For the all frequency table of the LMD-400-R, refer to "Data transceiver for use in the USA under FCC Part 90 License".

Regulatory compliance information

The LMD-400-R complies with the FCC Part 90.

Labelling:
The LMD-400-R 458 MHz-462.5 MHz is labeled as below.

FCC ID: V9X-LMD400R

The proposed FCC ID label format is to be placed on the module. If FCC ID is not visible when the module is installed into the system, "Contains FCC ID: V9X-LMD400R" shall be placed on the outside of final host system.

Exposure to radio frequency radiation:
To comply with FCC RF exposure compliance requirements, a separation distance of at least 20 cm must be maintained between the antenna of this device and all persons. This device must not be co-located or operating in conjunction with any other antenna or transmitter.
The maximum allowable MPE value of 0.305 mW/cm^2 will be reached in a distance of 20 cm in case that an antenna gain less than 22 dBi will be used.
The LMD-400-R complies with Part 15 Subpart B of the FCC Rules. Operation is subject to the condition that this device does not cause harmful interference.

NOTE: The LMD-400-R has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a commercial installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
· Reorient or relocate the receiving antenna.
· Keep water and moisture out of all antenna and radio fittings.
· Check all antenna connections – any imbalance in coax cable can cause
radio interference and receive / transmit problems.

Caution:
Changes or modifications not expressly approved by the party responsible for compliance could avoid the user's authority to operate the equipment.

Licensing of end-use products

LMD-400-R 458 MHz-462.5 MHz holds equipment authorization for transmitting equipment under Title 47 of the Code of Federal Regulations Part 90. (FCC Identifier: V9X-LMD400R)
This shall be the only guarantee of Circuit Design Inc for compliance with FCC regulations. Those who integrate LMD-400-R 458 MHz-462.5 MHz in a system and operate the radio system in the United States are required to apply for a user station license before the equipment can be operated. Application for the station license in Part 90 may be required to be submitted to a certified frequency coordinator for frequency coordination, then the FCC licensing bureau issues a license for equipment users/stations. As local frequency management issues are involved in licensing, Circuit Design Inc shall not be held liable for failure in obtaining the station license. Circuit Design Inc recommends users to contact a certified frequency coordinator in the region in advance to confirm whether or not a license can be granted.
For more details, please refer to "Data transceiver for use in the USA under FCC Part 90 License".

Important notice

- Customers are advised to consult with Circuit Design sales representatives before ordering.
  Circuit Design believes the provided information is accurate and reliable. However, Circuit Design reserves the right to make changes to this product without notice.
- Circuit Design products are neither designed nor intended for use in life support applications where malfunction can reasonably be expected to result in significant personal injury to the user. Any use of Circuit Design products in such safety-critical applications is understood to be fully at the risk of the customer and the customer must fully indemnify Circuit Design, Inc for any damages resulting from any improper use.
- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.

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Cautions

- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- Do not use the equipment within the vicinity of devices that may malfunction as a result of electronic radio waves from the radio module.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.
- Communication performance will be affected by the surrounding environment, so communication tests should be carried out before actual use.
- Ensure that the power supply for the radio module is within the specified rating. Short circuits and reverse connections may result in overheating and damage and must be avoided at all costs.
- Ensure that the power supply has been switched off before attempting any wiring work.
- The case is connected to the GND terminal of the internal circuit, so do not make contact between the '+' side of the power supply terminal and the case.
- When batteries are used as the power source, avoid short circuits, recharging, dismantling, and pressure. Failure to observe this caution may result in the outbreak of fire, overheating and damage to the equipment. Remove the batteries when the equipment is not to be used for a long period of time. Failure to observe this caution may result in battery leaks and damage to the equipment.
- Do not use this equipment in vehicles with the windows closed, in locations where it is subject to direct sunlight, or in locations with extremely high humidity.
- The radio module is neither waterproof nor splash proof. Ensure that it is not splashed with soot or water. Do not use the equipment if water or other foreign matter has entered the case.
- Do not drop the radio module or otherwise subject it to strong shocks.
- Do not subject the equipment to condensation (including moving it from cold locations to locations with a significant increase in temperature.)
- Do not use the equipment in locations where it is likely to be affected by acid, alkalis, organic agents or corrosive gas.
- Do not bend or break the antenna. Metallic objects placed in the vicinity of the antenna will have a great effect on communication performance. As far as possible, ensure that the equipment is placed well away from metallic objects.
- The GND for the radio module will also affect communication performance. If possible, ensure that the case GND and the circuit GND are connected to a large GND pattern.

Warnings

- Do not take a part or modify the equipment.
- Do not remove the product label (the label attached to the upper surface of the module.) Using a module from which the label has been removed is prohibited.

REVISION HISTORY

Version	Date	Description	Remark
0.9	Sept. 2009	Preliminary	