The **8051 CPU** core used in the CC253x device family is a single-cycle 8051-compatible core.
It has three different memory-access buses (SFR, DATA and CODE/XDATA) with single-cycle access to SFR, DATA, and the main SRAM.
It also includes a debug interface and an 18-input extended interrupt unit.
The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities.
Any interrupt service request is serviced also when the device is in idle mode by going back to active mode.
Some interrupts can also wake up the device from sleep mode (power modes 1–3).
The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus.
The memory arbiter has four memory access points, access of which can map to one of three physical memories: an 8-KB SRAM, flash memory, and XREG/SFR registers.
It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.
The **8-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces.
The 8-KB SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power modes 2 and 3).
This is an important feature for low-power applications.
The **32/64/128/256 KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.
In addition to holding program code and constants, the non-volatile memory allows the application to save data that must be preserved such that it is available after restarting the device.
Using this feature one can, e.g., use saved network-specific data to avoid the need for a full start-up and network find-and-join process .
The digital core and peripherals are powered by a 1.8-V low-dropout **voltage regulator**. It provides **power management** functionality that enables low power operation for long battery life using different power modes.
Five different **reset** sources exist to reset the device.
The CC2530 includes many different peripherals that allow the application designer to develop advanced applications.
The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging.
Through this debug interface, it is possible to perform an erasure of the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute supplied instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code.
Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The device contains flash memory for storage of program code.
The flash memory is programmable from the user software and through the debug interface.
The **flash controller** handles writing and erasing the embedded flash memory.
The flash controller allows page-wise erasure and 4-bytewise programming.
The **I/O controller** is responsible for all general-purpose I/O pins.
The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. CPU interrupts can be enabled on each pin individually.
Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.
A versatile five-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories.
Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors anywhere in memory.
Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface) achieve highly efficient operation by using the DMA controller for data transfers between SFR or XREG addresses and flash/SRAM.
Timer 1 is a 16-bit timer with timer/counter/PWM functionality.
It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value.
Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals.
It can also be configured in **IR Generation Mode** where it counts Timer 3 periods and the output is ANDed with the output of Timer 3 to generate modulated consumer IR signals with minimal CPU interaction.
The **MAC timer (Timer 2)** is specially designed for supporting an IEEE 802.15.4 MAC or other time-slotted protocol in software.
The timer has a configurable timer period and an 8-bit overflow counter that can be used to keep track of the number of periods that have transpired.
A 16-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends, as well as a 16-bit output compare register that can produce various command strobes (start RX, start TX, etc.) at specific times to the radio modules.
Timer 3 and Timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value.
Each of the counter channels can be used as a PWM output.
The **sleep timer** is an ultralow-power timer that counts 32-kHz crystal oscillator or 32-kHz RC oscillator

periods.
The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power mode 1 or 2.
The **ADC** supports 7 to 12 bits of resolution in a 30 kHz to 4 kHz bandwidth, respectively.
DC and audio conversions with up to eight input channels (Port 0) are possible.
The inputs can be selected as single-ended or differential.
The reference voltage can be internal, AVDD, or a single-ended or differential external signal.
The ADC also has a temperature-sensor input channel.
The ADC can automate the process of periodic sampling or conversion over a sequence of channels.
The **random-number generator** uses a 16-bit LFSR to generate pseudorandom numbers, which can be read by the CPU or used directly by the command strobe processor.
The random numbers can, e.g., be used to generate random keys used for security.
The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys.
The core is able to support the AES operations required by IEEE 802.15.4 MAC security, the ZigBee network layer, and the application layer.
A built-in **watchdog timer** allows the CC2530 to reset itself in case the firmware hangs.
When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.
It can alternatively be configured for use as a general 32-kHz timer.
USART 0 and USART 1 are each configurable as either a SPI master/slave or a UART.
They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications.
Each has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses.
The CC2530 features an IEEE 802.15.4-compliant radio transceiver.
The RF core controls the analog radio modules. In addition, it provides an interface between the MCU and the radio which makes it possible to issue commands, read status, and automate and sequence radio events.
The radio also includes a packet-filtering and address-recognition module.

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
. Reorient or relocate the receiving antenna.
. Increase the separation between the equipment and receiver.
. Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
. Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: To assure continued compliance, any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. (Example - use only shielded interface cables when connecting to computer or peripheral devices).

End Product Labeling

This transmitter module is authorized only for use in devices where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in visible area with the following: “Contains FCC ID: GX9ZBH-SA ”
”

End Product Manual Information

The user manual for end users must include the following information in a prominent location “IMPORTANT NOTE: To comply with FCC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be colocated or operating in conjunction with any other antenna or transmitter.” This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions (1) This device may not cause harmful interference and (2) This device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the

FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization. This device is intended only for OEM integrators under the following conditions: The antenna must be installed such that 20 cm is maintained between the antenna and users. As long as a condition above is met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).