DANIELS™
ELECTRONICS LTD.

MT-3 RADIO SYSTEMS

PAGING MODULATOR INSTRUCTION MANUAL
CI-PM-3

Covers models: CI-PM-3-00

Issue:	1	Previous Issue:	-
Issue Date:	October 1998	Previous Issue Date:	-
Printing Date:	Month Year		
Part No.:	IM55-CIPM3		

Daniels Electronics Ltd.
Victoria, BC.
PRINTED IN CANADA

FCC ID: H4JVT-3-150-SW08

Reviewed By:

Quality Assurance:

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Name	Signature	Date

NOTE:

The user's authority to operate this equipment could be revoked through any changes or modifications not expressly approved by Daniels Electronics Ltd.

The design of this equipment is subject to change due to continuous development. This equipment may incorporate minor changes in detail from the information contained in this manual.

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1. GENERAL

1.1 Introduction

The CI-PM-3 Paging Modulator module is an optional plug-in component of the MT-3 Radio Repeater System. This module provides digital and/or analog paging capability for Daniels MT-3 transmitters in all supported frequency bands.

The CI-PM-3 is designed for low power consumption, typically drawing less than 250 mA in steady state. In its standard configuration, the CI-PM-3 uses an on-board frequency reference source consisting of a 10 MHz OCXO with a standard stability of 0.03 PPM. For high stability applications (such as Simulcast), the CI-PM-3 Paging Modulator may be configured to use an external high stability reference source (i.e. rubidium, GPS or WWV) with a standard stability greater than or equal to 0.002 PPM, to discipline the on-board phase-locked loop OCXO oscillator. To ensure that paging signals are the same relative to each transmitter, the CI-PM-3 also incorporates a limited delay compensation for the different link propagation paths between transmitters.

The CI-PM-3 Paging Modulator supports both analog and digital paging formats, and can transmit POCSAG and other 2-level modulation schemes at data transfer rates of 512, 1200, and 2400 Baud. It can also be configured for use as a data repeater, whereby 2-level paging data is recovered, re-shaped and then re-transmitted to an additional repeater/paging transmitter. The CI-PM-3 supports 4-level modulation formats in non-repeater mode (i.e. in a base station paging transmitter application only) at data transfer rates up to 1600 BPS. Each of the four modulation deviation levels can be independently set, making the CI-PM-3 suitable for use in such pager signaling schemes as Motorola's FLEX™ Paging Protocol.

Setup conditions are established via front panel switch settings, while internal jumper settings and setup adjustments are easily accessible using the EC-96, 96 Pin Extender Card.

The CI-PM-3 Paging Modulator includes the following standard features:

- low power analog and CMOS control circuitry.
- extended operating temperature range;
- jumper selectable Repeater/paging transmitter configuration;
- on-board +/-0.03 PPM 10 MHz OCXO;
- front panel selection of PLL OCXO using external high stability frequency reference;
- jumper and line selectable analog / digital paging configuration;
- connection for optional CTCSS encoder / decoder;
- balanced 600 Ω / single-ended microphone input;
- selectable digital delay for Simulcast operation

1.2 Construction

The CI-PM-3 Paging Modulator is packaged in a compact Eurostandard shell module housing of nickel/steel with an anodized aluminum front panel. Corrosion resistant fasteners are used throughout the assembly.

1.3 Printed Circuit Board Numbering Convention

To ease troubleshooting and maintenance procedures, Daniels Electronics Limited has adopted a printed circuit board (PCB) numbering convention in which the last two digits of the Circuit Board number represent the Circuit Board version. For example:

- PCB number 43-912010 indicates Circuit Board version 1.0;
- PCB number 50002-02 indicates Circuit Board version 2.0.

All PCB's manufactured by Daniels Electronics are identified by one of the above conventions.

1.4 SPECIFICATIONS

1.4.1 General Specifications

Model Number:	CI-PM-3
Type:	MT-3 Series Paging Modulator
Compatibility:	MT-3 Series Radio Systems
Frequency Range:	29-50 MHz, 132-174 MHz, 406-430 MHz, 450-512 MHz, 806-824 MHz, 851-869 MHz, 896-902 MHz, 928-935 MHz and 935-960 MHz
Modulation: 16K0F3D 14K4F1D	~~11/16K0F3E (FM Analog), and 11/16K0F1D (FM Data Transmission).~~
Audio Input:	Balanced 600 Ω (tone or voice)
Digital Input:	Bipolar: RS-232 compatible
Reference Input:	10 MHz, 0.5 to 2.5 V rms, 50 Ω Front Panel SMA
Reference Output:	10 MHz (Modulated), 2.5 V rms, 50 Ω Front Panel SMA
Frequency Stability:	Standard: ±0.03ppm -40°C to +60°C Optional: External High Stability Reference ±0.002ppm -40°C to +60°C (requires WWV or GPS reference source).

Duty Cycle:	Continuous, 100% from -40°C to +60°C
Audio Response:	0 Hz to 3.4 kHz
Maximum Deviation:	+/- 50 PPM
Front Panel Control:	FREQ REF (INT / EXT), MODE (NORM / SETUP), SET MOD (2 LEVEL / 4 LEVEL) SET DEV
Analog / Digital PTT Activation:	Front panel connector / rear motherboard connection
Current Consumption:	+13.8 VDC supply: 600 mA power up 200 mA steady state +9.5 VDC supply: 100 mA
Operating Temperature Range:	-40°C to +60°C
4 Level Paging:	Local.Base Station paging only
2 Level Paging:	Multiple Transmitter paging
Simulcast	Supported through the use of WWV/GPS.
IC Type Approval:	TBA
FCC Type Acceptance:	TBA

1.4.2 CTCSS Decoder/Encoder (Option)

Manufacturer:	Communication Specialties
Model Number:	TS-64
Number of Tones:	64
Frequency Range of Tones:	33.0 to 254.1 Hz
Signal to Noise:	Better than 4 dB SINAD
Decode Time:	150 ms. nominal
Fade Time:	350 ms. nominal
Squelch Tail Elimination::	160 ms. reverse phase burst
Current Consumption:	9 mA

1.4.3 Physical Specifications

Physical Dimensions:	Width:	Height:	Depth:
	3.5 cm (1.38")	12.8 cm (5.05")	19 cm (7.5")
Module Weight:	0.4 kg (1 lb.)		
Corrosion Prevention:	Anodized aluminum construction with Stainless steel hardware. Selectively applied Conformal coated glass epoxy 4 layer printed circuit boards. Gold plated module connectors.		
Module Design:	Compact Eurostandard modular design. Plug-in module mates with Daniels standard 19" M3 repeater subrack. Interchange able for test and repair.		
External Connections:	REF Input and Output SMA connectors located on the module's front panel. Motherboard Connections (Audio, Modulation, Power, and Control) are made through a 96 pin, gold plated type C connector on the rear of the module. User connections (Audio, Modulation, and Control) are made through a front panel DB-15 connector as well as through the 96 pin connector on the rear of the module.		

2. THEORY OF OPERATION

The CI-PM-3 Paging Module circuitry can be divided into three main functional blocks: Paging Signal Path, OCXO/PLL, and Configuration Options. The Paging Signal Path includes signal conditioning circuitry which is used to level and edge-condition the incoming data signal, then band-limit it for transmission. The OCXO/PLL circuitry develops a high stability 10 MHz reference signal for the transmitter. The Configuration Options circuitry allows the CI-PM-3 to be configured for paging/repeater operation, and includes compensation for propagation path delays in multiple transmitter systems.

2.1 Paging Signal Path

The CI-PM-3 can process both analog and digital paging signals. Paging control and data signals are accessed via the DB-15 front panel DATA/CTRL PORT J1 or through the 14 pin Control 2 IO Connectors on the rear of the M-3 motherboard. Bi-level, RS-232 compatible 2-level digital paging data is input through J1 Pin 1 (ALARM 8 control line). 4-level digital paging data is input through J1 Pin 1 and J1 Pin 2 (ALARM 8 and ALARM 6 control lines). A clock input line is available through J1 Pin 3 (ALARM 4 control line) for optional high-stability synchronization of 4-level paging data.

Analog paging information is input through the balanced audio inputs, J1 Pin 9 and J1 Pin 10 (ALARM 7 and ALARM 5 control lines). The paging mode, either analog or digital, is controlled by J1 Pin 5 (ALARM 2 control line). For applications which utilize both analog and digital paging modes, J1 Pin 5 must be switched high for analog paging and switched low for digital paging. In digital-only paging configurations, Analog/Digital Override shunt jumper JU41-B must be installed. Analog and/or digital TX PTT is input via J1 Pin 7 (ALARM 1 control line) for base paging transmitter applications, and is generated internally from RX A or RX B COR for paging/repeater applications.

2.1.1 2-Level Digital Paging

For 2-level data, front panel switch SW2 must in the NORM position, Level Select jumper JU23 must be in the 2/4-LVL (A) position and J1 Pin 4 (ALARM 3 control line) must be held low. Alternately, if the paging system will be processing 2-level data only, 2-Lvl/4-Lvl Mode Override jumper JU42 can be in the 2-Lvl (B) position and the control line left unconnected. Data is input on J1 Pin 1 (ALARM 8 control line), routed through Data Input jumper JU8-A to RS-232 Driver/Receiver U3, then through the normally made contacts of Digital Switch U11b to Data Delay / Bypass jumper JU36. The data signal is then routed through U9a to U12 where it is reshaped (edge-conditioned). If the binary polarity of the data signal is to be inverted (i.e. a logic '1' processed as negative deviation, and a logic '0' as positive deviation), it is routed through U12d and 2-Lvl Polarity Select jumper JU1-B (inverted). Otherwise it is routed through U12c and 2-Lvl Polarity Select JU1-A (normal). The data from U12 controls digital switch U9c which switches between the

positive and negative deviation limits of the modulated signal as set by R5/U13c and R6/U13d, respectively. The output of U9c passes through U10a which is normally closed for 2-level signals, and through U7b which is normally closed for digital signals, to input buffer U14a of the 6-pole Butterworth Filter comprised of U14b, U14c and U14d. The output of the Butterworth Filter is low-pass limited to 3400 Hz, and is sent to TX A and/or TX B DIR MOD (band pass) inputs via U15a and U15b. R23 adjusts the band pass signal level. The output of the Butterworth Filter is also normally routed via XO Polarity Select jumper JU5-A (normal polarity) to U15C and then through U10b which is normally closed for digital signals, to the XO SELECT jumper JU6. The XO SELECT jumper is normally installed in the normal (A) position, selecting the on-board ±0.03 PPM OCXO. The signal is then buffered (if no external REF IN signal is used) or summed with the PLL correction signal (if an external high stability REF IN signal is used) by U16c and then input to the MOD I/P of the on-board OCXO.

Note: Position B of the XO SELECT jumper selects the MT-3 transmitter's +/-1.0 PPM 9.6 MHz VCXO in lieu of the on-board 10 MHz OCXO. Use of this option requires reconfiguration of the MT-3 Synthesizer and may require that the XO Polarity Select jumper JU5 be installed in the B (inverted) position, if the VCXO has a negative slope. An external +/-0.002 PPM high stability reference signal cannot be used in this configuration.

2.1.1.1 Self Test Circuitry

With front panel switch SW2 in the SETUP position, 8 VDC is switched to the control input of switch U11a andU11d. U11a applies 8 VDC to the square wave symmetry adjustment R70. U11d enables the square wave generator U17c. Switch SW2 also places a GND potential on the control input of square wave frequency selector, U7c, disabling it and switching R72 out of the feedback circuit of U17c. Switch SW4 controls the output of oscillator U17c such that with switch SW4 in the Data "1" position, a binary "1" is output from U17c and with switch SW4 in the Data "0" position, a binary "0" is output. With switch SW4 in the "centre" position, R41 is placed in the feedback circuit of U17c through U11d, causing U17c to oscillate at approximately 600 Hz. The symmetry of the square wave signal produced (i.e. the width of the positive going pulses as compared to the width of the negative going pulses) is adjustable by R70. The three signals, binary "0", binary "1" and the 600 Hz square wave, are switched through front panel switch SW3 to set up the 2 and 4-Level positive and negative deviation levels (R3, R4, R5 and R6) as well as the band pass gain (R23).

2.1.1.2 Data Indicator Circuitry

With front panel switch SW2 in the NORM position, voltage follower U17b buffers the data signal at the output of U11b and prior to the input of U9a. When an alternating binary signal is present on J1 Pin 1, the detector circuitry comprised of C46, R49, D8, R71 and C47 develops a DC voltage on the control input (Pin 1) of switch U11a. Conversely, zero voltage will be developed at this point for a constant binary "0" or constant binary "1". This control signal causes U11a to switch 8 VDC

to the square wave generator U17c and the square wave frequency selector U7c. Switch U7c places R72 in parallel with R41 in the feedback circuit of U17c through U11d, causing U17c to oscillate at approximately 10 Hz. This signal causes the front panel DATA indicator, LED2, to flash at a rate discernible to the naked eye.

2.1.2 4-Level Digital Paging

For 4-level data operation, front panel SW2 must be in the NORM position, 2-Lvl/4-Lvl Mode Override jumper JU42 must be in the A position, and Level Select jumper JU23 must be in the 2/4-LVL position with J1 Pin 4 held high or left unconnected. 4-level paging data is represented using two data bits; input on pins 1 and 2 of front panel DATA/CTRL PORT J1. Each of the four possible bit combinations corresponds to a deviation level setting (refer to Table 4-6). An optional clock input line is provided through J1 Pin 3 for 4-level signal synchronization. 4-level data is input on J1 Pin 1 (ALARM 8 control line) and J1 Pin 2 (ALARM 6 control line). The 2 and 4-level input is then routed through driver/receiver U3, through the normally made contacts of digital switch U11b and U11c to the inputs of digital switches U9a (through Data Delay/Bypass jumper JU36) and U9b. Data is also routed to the inputs of D Flip-Flop U18. If a synchronizing clock signal is used, Clock Enable jumper JU46-A is installed and the clocked outputs of U18 are switched through U9a and U9b. Data is then input from U9a and U9b to U12c and U12e. U12c and U12e reshape the data signals and the outputs are then routed through 2-Lvl Polarity Select jumper jumpers JU1-A (normal polarity) and 4-Lvl Polarity Select jumper JU2-A (normal polarity), or through U12d and U12f and then jumpers JU1-B (inverted polarity) and JU2-B (inverted polarity). The data signal from U12c/U12d, representing Bit 0 of the 4-level data signal, is used to control digital switches U9c and U9d, which switch between positive and negative deviation settings of the modulated signal as set by R5/U13c, R6U13d, R3/U13a and R4U13b. The output of U9c or U9d is selected by U10a based on Bit 1 of the 4-level data signal from U12e/U12f through U7a. The output of U10a is passed through U7b and follows the same path to the VCXO and OCXO inputs as the 2-level data, explained in section 2.1.1 above.

2.1.3 Analog Paging

During an analog page, A/D Mode select control line (J1 Pin 5 or ALARM 2) must be switched high, disabling the digital path and causing U10b to switch in the 2.5 VDC reference voltage set by R24/U15d. The reference voltage is applied to the OCXO Modulation I/P through XO Select jumper JU6 to maintain the XO centre frequency for the duration of the analog page. The analog paging signal is input through Pins 9 and 10 of J1 (ALARM 7 and ALARM 5 control lines), and routed to TX A and/or TX B BAL I/P 1 and 2 audio connections via JU26/JU27, JU15/JU16 and JU24/JU25. Analog deviation settings are made on the MT-3 Transmitter Audio Processor Board.

2.2 OCXO/PLL

The main component of the OCXO/PLL circuitry is the 10 MHz Ovenized Crystal Oscillator (OCXO), which provides the (standard) +/-0.03 PPM stability reference signal to the front panel REFERENCE INPUT of the MT-3 Transmitter. This circuit may also be configured to phase-lock to a GPS or WWV referenced high stability 10 MHz signal via the front panel REF IN SMA connector to generate a higher stability reference signal of +/-0.002 PPM.

2.2.1 Standard Frequency Reference

When the on-board OCXO is used as a stand-alone +/-0.03 PPM frequency reference, front panel FREQ REF switch SW1 is set to the INT position. The centre frequency of 10 MHz is factory-adjusted via R82 which sets the output of voltage follower U16c. It is HIGHLY recommended that this adjustment NOT be altered. U16c also buffers the modulating digital paging signal routed through XO Select jumper JU6-A. The output of the OCXO is buffered by 50 Ω gain block U19, to the front panel REF OUT SMA connector, where it is then connected via 50 Ω coax cable to the REFERENCE INPUT SMA connector on the front panel of the MT-3 transmitter.

2.2.2 High Stability Frequency Reference

When a higher stability paging signal is required (i.e. for Simulcast operation), an external GPS or WWV referenced signal is input via the front panel REF IN SMA connector. To enable the on-board PLL circuitry, PLL Power Enable jumpers JU37 and JU39 must be installed and front panel FREQ REF switch SW1 must be set to the EXT position. The input reference signal is buffered by 50 Ω gain block U20, is level and edge-conditioned by U21b and U25a, then input as the reference to Ultrahigh Speed Phase/Frequency Discriminator U4. The second input to U4 is the on-board OCXO output which has been level and edge-conditioned by U21a and U25b. The output of U4 is a pulse train of digital error signals with a duty cycle proportional to the phase difference between the reference and OCXO signals. This pulse train is filtered by the second-order passive RC low-pass filter comprised of R85, R84 and C36 for analog paging signals (short time constant), or R42, R28 and C36 for digital paging signals (long time constant). The selection of long or short time constant filter is made through digital switches U10c and U10d based on the condition of DATA/VOICE mode selection line J1 Pin 5 (ALARM 2 control line). The output of the low-pass loop filter is buffered by U16a, level-adjusted by U16b, summed with the modulating digital signal in U16c, and connected to the modulating input of the OCXO. The output of the OCXO is buffered by 50 Ω gain block U19 to the front panel REF OUT SMA connector, where it is then connected via 50 Ω coax cable to the REFERENCE INPUT SMA connector on the front panel of the transmitter.

The CI-PM-3 has been designed for use in stand-alone base paging transmitter applications as well as multiple-transmitter systems. A multiple-transmitter system normally consists of a local base station paging transmitter and one or more remote paging transmitters which regenerate the paging signal and extend the paging coverage area. Optionally, one or more paging link repeaters may be installed in the system to further extend the range and overcome such obstacles as extended distance and/or mountainous terrain.

Due to the complexity of 4-level signal regeneration, only 2-level paging formats are supported in multiple-transmitter configurations. In any multiple-transmitter system, 2-Lvl/4-Lvl Mode Override jumper JU42-B should be installed in the B position to select 2-level paging only.

2.3.1 Simultaneous Broadcasting (2 Level Paging Only)

When a paging system contains multiple transmitters, it is possible that the signal from one transmitter may interfere with the signal from another, resulting in distortion that will degrade paging reliability and intelligibility. A Simulcast system addresses this problem by ensuring that all paging signals are of the same frequency and phase and that they are all transmitted at the same time. To obtain identical frequency and phase at each transmitter, the on-board 10 MHz OCXO of each CI-PM-3 can be phase-locked to an external reference signal (typically GPS or WWV disciplined) via the front panel REF IN SMA connector (see Section 2.2.2, High Stability Frequency Reference). To ensure that each transmitter in the system transmits at exactly the same time, the link paging signals are delayed by a value which is proportional to the distance to the furthest transmitter in the system. In this way, the propagation path delay for each link is accounted for, such that the transmitter located the furthest from the base station has no delay applied to its paging signal, while those located closer in have increasing amounts of delay.

The CI-PM-3 incorporates selectable digital delay compensation, thereby eliminating the necessity for an external signal delay unit in most applications. To enable data delay, Data Delay Power Enable jumpers JU38 and JU40 must be installed and the two jumpers of Data Delay/Bypass jumper JU36 must be oriented in the DELAY position. The 2-level data output from U11b is routed through JU36 to the input of the positive and negative-edge integrator circuitry and also to the data input of U23. The positive-edge integrator is comprised of C60/51 and R99, U24a, U8d, and D11. The negative-edge integrator is comprised of C52, U24b, U8e, U8c and D12. U8f buffers and shapes the combined edge pulses, which are then used to synchronize Programmable Counter U22 to the data signal. The fundamental 2 MHz output frequency of U22 is set by resonator X1 and is fine-tuned by tuning capacitor C55. The output of U22 is a square wave which is a variable of the fundamental frequency determined by jumper settings Data Delay Selection jumpers JU31, JU32 and JU33. This square wave is used as the OSC input to Contact Debouncer U23, which generates a corresponding delay on both the positive and negative going edges of the data signal. The jumper settings of JU35, JU31, JU32 and JU33 will determine the total amount of delay applied to the data signal to compensate for the propagation path distance (refer to Table 4-3).

At the remote repeater/paging transmitter, Rx Discr O/P Enable jumpers JU29 and/or JU43 are closed and Data Regeneration jumper JU7 is in the B (Enabled) position, allowing the discriminated data signal to be routed from B10/C28 to U16d where it is amplified to TTL levels. The regenerated data is converted to RS-232 levels through driver/receiver U3, is routed through Data Select Jumper JU8-B (RPTR DATA I/P) and then follows the normal data path through U3 to U11b. The regenerated data is also available to the user at J1 pin 11 (DATA OUT) through jumper RS-232 Data Out Enable jumper JU50. RX A or RX B COR signal is routed through JU19 and/or JU45 to U8a and Q3 to generate the repeater PTT signal, which is routed through JU22 and JU20 and/or JU21to TX A and/or TX B. Power enable jumper JU40 must be installed to provide power to the PTT regeneration circuit.

If the system is configured for digital paging only, all CI-PM-3 units (i.e. base station, repeater and remote paging transmitter) must have Analog/Digital Override shunt jumper JU41-B and Repeater Digital Only PTT Enable jumper JU51 installed.

If the multiple-transmitter system is configured for both analog and digital paging, the CI-PM-3 units at both the base station and the remote repeater/paging transmitter must have a TS-64 CTCSS module installed. The TS-64 must be configured with POLARITY jumper JP7 installed. CI-PM-3 CTCSS PTT Bypass jumper JU34 must be removed. CTCSS configuration jumpers JU52 and JU53 (normally open) are used in conjunction with TS-64 jumper JP11 to select the HANG UP/BUSY INPUT functions of the CTCSS module.

During an analog page, the DATA/VOICE SELECT line J1 Pin 5 (ALARM 2 control line) of the base station CI-PM-3 is held high, and the PTT signal from J1 Pin 7 (ALARM 1 control line) enables the TS-64 CTCSS Module. The TS-64 immediately keys TX A and/or TX B through JU51 and JU20 and/or JU21 and generates a CTCSS sub-audible tone. The CTCSS tone is routed through Repeater CTCSS Enable jumper JU10-B, buffered by U15d and switched by digital switch U10b through XO Select jumper JU6-A to the OCXO Modulation I/P. In the remote paging transmitter, CTCSS RX A Mute Bypass jumper JU28, Analog/Digital Mode Override jumper JU41-A and RX Discr O/P Enable jumpers JU29 and/or JU43 must be installed, while CTCSS PTT Bypass jumper JU34 and Repeater Digital Only PTT Enable jumper JU51 must be removed. Normally, the CTCSS module holds the RX MUTE line low. This line is routed through CTCSS RX A Mute Bypass jumper JU28 to the DATA/VOICE SELECT line input to transistor switch Q1, placing the CI-PM-3 in digital mode. The PTT signal is generated by the RX A or RX B COR signal through D6, U8a and Q3. An analog page is indicated by a sub-audible tone, detected by the CTCSS module via RX A or RX B DISCR O/P. On receipt of an analog page, the TS-64 sets the RX MUTE line high, causing transistor switch Q1 to switch the remote repeater/paging transmitter into analog paging mode.

3. ALIGNMENT PROCEDURE AND INSTALLATION

3.1 General

The CI-PM-3 Paging Modulator is by default configured for stand-alone base station paging, using 2-Level paging data with a binary polarity of 1, and using the on-board +/-0.03 PPM 10 MHz OCXO. Table 4-4 contains a complete list of CI-PM-3 default jumper settings. The CI-PM-3 can also be configured for 4-level signal (base transmitter only) paging, remote paging, link repeater or higher stability operation. Each of these configurations is covered separately in the following sections.

3.2 Repair Notes

Removal and replacement of surface mount components should be performed only in specifically designed surface mount rework and repair stations complete with electrostatic discharge (ESD) protection.

To help prevent damage to the circuit board pads when removing Surface Mount Solder Jumpers, it is recommended that solder braid be used in place of manual vacuum de-soldering tools.

3.3 Recommended Equipment List

Alignment of the CI-PM-3 requires the following test and radio equipment, or its equivalent:

• Power Supply:	Regulated +13.8 VDC at 2 A
• Oscilloscope / Multi-meter:	Fluke 97 Scopemeter
• Current Meter:	Fluke 75 Multi-meter
• Radio Communications Test Set:	Marconi Instruments 2955R (W/External Reference)
• Sub-rack:	Daniels SR-3 Series 19" Sub-rack
• System Monitor:	Daniels SM-3 Series System Monitor
• Transmitter Module:	Daniels Enhanced Performance VT-3 / UT-3 Series
• Extender Card and Cable:	Daniels EC-96K, 96 Pin Extender Card and Cable
• Alignment Tool:	Johanson 8766

Note: It is highly recommended that the Radio Communications Test Set be frequency locked to an external 10 MHz reference (WWV or GPS), ***especially*** if the factory-adjusted frequency settings are to be altered in any way.

3.4 Installation

1. Install the Daniels EC-96 Extender Card in either the far left-hand or the far right-hand slot of the subrack (as viewed from the front). Remove the side covers of the CI-PM-3 Paging Modulator and attach the 96-Pin Extender Cable between it and the Extender Card.

2. Apply +13.8 VDC power to the Subrack. Allow approximately 5 minutes for warm-up.

3.5 Alignment

Refer to Figure 5-1 for the location of the CI-PM-3 module front panel controls.

1. Ensure the CI-PM-3 circuit board jumpers are initialized to their default settings (refer to Table 4-4). Note any differences so that the jumpers can be returned to their former positions.

2. For alignment procedures in this section, set the front panel switches to the following settings, unless otherwise noted:
   a) SW1 (FREQ REF) set to INT
   b) SW2 (MODE) set to SETUP
   c) SW3 (SET MOD) set to 2 LEVEL
   d) SW4 (SET DEV) set to Data "1" (Top Position)

3. Ensure the Transmitter Audio Processor circuit board jumpers are initialized to their default settings (refer to Tables 4-7 or 4-8).

4. Connect the CI-PM-3 REF OUT connector to the transmitter REFERENCE INPUT connector via a SMA to SMA RF cable.

Do not connect any other input signal/control lines to the CI-PM-3 at this time.

3.6 Frequency (Digital Paging) Adjustment

CI-PM-3 frequency adjustments are factory set. It is strongly recommended that they not be altered. The following procedure applies **only** if field adjustment is required:

1. Set front panel SW1 (FREQ REF) INT and remove shunt jumper JU6-A.

2. Set front panel DB-15 connector J1 Pin 4 and J1 Pin 5 to J1 ground (J1 Pin 8).

3. Set the transmitter front panel NORM/KEY TX switch to KEY TX.

4. Monitor the Communications Test Set and adjust FREQ ADJ potentiometer R82 for the transmitter operating frequency +/-1 Hz.

5. Set the transmitter front panel NORM/KEY TX switch to NORM and replace JU6-A.

3.7 Reference (Analog Paging) Adjustment

CI-PM-3 Reference frequency adjustment is factory set. It is strongly recommended that they not be altered. The following procedure applies **only** if field adjustment is required.

1. Ensure shunt jumper JU6-A is installed. Set front panel DB-15 connector J1 Pin 4 to ground (J1 Pin 8) and J1 Pin 5 to open (no connection).
2. Monitor the Communications Test Set and adjust REF ADJ potentiometer R24 for the transmitter operating frequency +/-1 Hz.
3. Set the transmitter front panel NORM/KEY TX switch to NORM.

3.8 Test Data Symmetry Adjustment

2. Set the oscilloscope for 1.0 V/Div (vertical) and 0.5 ms/Div (horizontal). Monitor TP10.
3. Set front panel DB-15 connector J1 Pin 4 and J1 Pin 5 to ground (J1 Pin 8).
4. Set SW3 (SET MOD) to 2 LEVEL and SW4 (SET DEV) to the centre or "Continuous Bit Stream" position.
5. Adjust R70 (Test Data Symmetry Adjust) for symmetrical positive and negative pulses (i.e. of equal width) as measured at TP10.

3.9 2 And 4 Level Deviation Adjustment

1. Monitor the transmitter frequency and deviation on the Communications Test Set and set the transmitter front panel NORM/KEY TX switch to KEY TX.
2. Set front panel DB-15 connector J1 Pin 4 and J1 Pin 5 to J1 ground (J1 Pin 8).
3. Set SW3 (SET MOD) to 2 LEVEL, and SW4 (SET DEV) to the Data "1" (top) position. Adjust R5 (2-LVL +Dev) for +4.8 kHz deviation (4.8 kHz above centre frequency).
4. Change SW4 (SET DEV) to the Data "0" (bottom) position. Adjust R6 (2-LVL -Dev) for -4.8 kHz deviation (4.8 kHz below centre frequency).
5. Change SW3 (SET MOD) to 4 LEVEL. Adjust R4 (4-LVL -Dev) for -1.6 kHz deviation.
6. Change SW4 (SET DEV) to the Data "1" (top) position. Adjust R3 (4-LVL +Dev) for +1.6 kHz deviation.

7. Set SW3 (SET MOD) to 2 LEVEL. Set SW4 (SET DEV) to the centre position. Adjust R23 (BP DEV ADJ) for maximum deviation of +/-4.8 kHz.

3.10 PLL Setup

CI-PM-3 PLL adjustments are factory set. It is **strongly** recommended that they not be altered. The following procedure applies **only** if field adjustment is required:

1. Install Power Enable surface-mount jumpers JU37 and JU39.

2. Ensure front panel SW1 (FREQ REF) is set to EXT, and shunt jumper JU6-A is removed. Set front panel DB-15 connector J1 Pin 4 to ground (J1 Pin 8) and J1 Pin 5 to J1 to open (no connection).

3. Connect the 50 Ω output of a high stability, 10 MHz reference to front panel REF IN SMA connector J3. Ensure the output level of the external reference is between 0.5 to 2.5 V rms.

4. Measure and record the voltage at TP13 with the DMM.

5. Measure the voltage at TP12 with the DMM.

6. Adjust PLL CAL potentiometer R101 until the voltage measured at TP12 matches the voltage measured in step (a) above within ± 0.2 Vdc. Note that when the PLL locks in, the voltage at TP12 will also lock in to within ±0.2 Vdc of the voltage at TP13. At this point further adjustment of R101 will not change the value unless it is brought out of lock.

7. Replace shunt jumper JU6-A.

3.11 Data Delay Setup

1. Enable the DATA DELAY option by installing Power Enable surface-mount jumpers JU38 and JU40. And moving the two DATA DELAY shunt jumpers of JU36 to the DELAY (vertical) position.

2. Set front panel switches SW2 (MODE) to SETUP, SW3 (SET MOD) to 2 LEVEL, and SW4 (SET DEV) to "Continuous Bit Stream" (refer to SW4 DETAIL in Figure 6-1).

<u>To calibrate the positive and negative edge delay:</u>

3. Set the oscilloscope for 1.0 V/Div (vertical) and 0.5 µs/Div (horizontal). Select channel 1 as trigger input and set Trigger Slope to positive.

4. Monitor the data signal at TP9 on channel 1 of the oscilloscope.

5. Monitor and record the period of the data delay pulse at TP7 on channel 2 of the oscilloscope.

6. Set Trigger Slope to negative.

7. Continue monitoring the data signal at TP9 on channel 1 of the oscilloscope while monitoring the period of the data delay pulse at TP7 on channel 2.

8. Adjust R95, DELAY SYNC, until the period of the data delay pulse measured at TP7 is identical to that measured in step (b) above.

To set the delay resolution (output frequency of Programmable Counter U22):

9. With shunt jumpers JU31A, JU32A and JU33A installed, monitor the frequency of the signal at TP8.

10. Adjust tuning capacitor C55 for a frequency of 1.0 MHz (+/- 10 Hz) at TP8.

3.12 Simulcast Delay Setup

A typical Simulcast system is depicted in Figure 5-2. To correctly determine the differing propagation path delays to each transmitter in a Simulcast system and compensate for them, signal delays in both the transmission medium and the equipment must be known. For the purposes of this manual, it is assumed that only Daniels MT-3 radio equipment will be utilized at each paging site, and that each radio subrack will be identically configured with CI-PM-3 Paging Modulator modules.

Signal delays from the base transmitter to any paging transmitter are calculated as follows:

$$Delay = t_{(Link)} + t_{(Eqpt)}$$

Where:

$t_{(Link)}$ = *Propagation delay from Base TX to Paging TX*

$t_{(Eqpt)} = t_{(RX)} + t_{(PM)} + t_{(TX)}$

$t_{(RX)}$ = *Delay through Receiver*

$t_{(PM)}$ = *Delay through Paging Modulator*

$t_{(TX)}$ = *Delay through Transmitter*

d = *Distance*

The delay through the equipment at each paging transmitter site, $t_{(Eqpt)}$, will be identical for each link, and can therefore be eliminated from our calculations. As such, the only delay variable(s) of interest will be the distance from the base transmitter to each paging transmitter. Since radio waves propagate at or near the speed of light (3×10^8 m/sec), the delay calculation becomes:

$$\begin{aligned} Delay &= t_{(Link)} \\ &= d\,(km) \times 3.33\mu sec \\ &\qquad or \\ &= d\,(mi) \times 5.37\mu sec \end{aligned}$$

For the Simulcast system depicted in Figure 5-2, the signal transmitted by PAGING TX #1 will not be delayed, as this is the furthest site from the BASE TX. However, to ensure identical signal processing characteristics at each site, the DATA DELAY circuitry of the CI-PM-3 at PAGING TX #1 will be enabled, but with zero delay selected. PAGING TX #2 will have its paging signal delayed by a value proportional to the difference in distance between PAGING TX #1 and PAGING TX #2 to the BASE TX. The delay for PAGING TX #2 is therefore calculated as:

$$Delay_{(Link\ B)} = (d_{(Link\ A)}\ (km) - d_{(Link\ B)}\ (km)) \times 3.33\mu sec$$
$$or$$
$$= (d_{(Link\ A)}\ (mi) - d_{(Link\ B)}\ (mi)) \times 5.37\mu sec$$

The delay calculations for any paging transmitter site in a multiple-transmitter system, with distances measured from the site of interest back to the BASE TX, becomes:

$$Delay_{(Site\ of\ Interest)} = (d_{(Furthest\ Site)}\ (km) - d_{(Site\ of\ Interest)}\ (km)) \times 3.33\mu see$$
$$or$$
$$= (d_{(Furthest\ Site)}\ (mi) - d_{(Site\ of\ Interest)}\ (mi)) \times 5.37\mu sec$$

To set the delay value: Once the required delay has been calculated for a particular paging site, refer to Table 4-3 delay settings:

1. Locate the DELAY (µsec) value which is closest to the calculated value.

2. Set shunt jumpers JU31, JU32, JU33, and JU35 according to the JUMPER SETTINGS.

Data Delay Adjust: To set delay values other than those listed in Table 4-3:

1. Set the oscilloscope for 1.0 V/Div (vertical) and 0.5 µs/Div (horizontal). Select channel 1 as trigger input and set Trigger Slope to positive.

2. Monitor the test data signal at TP9 on channel 1 of the oscilloscope and the output signal at TP5 on channel 2.

3. Adjust the oscilloscope for maximum horizontal display of the distance between the signals' leading edges. Adjust tuning capacitor C55 until the output signal's leading edge on channel 2 is delayed from the input signal's leading edge on channel 1 by the desired delay amount.

Example: To set a delay of 44 µsec:

1. Set oscilloscope horizontal resolution to 5 µsec/div.

2. Install shunt jumpers JU31B, JU32A, JU33A and JU35E (refer to Table 4-3).

3. Monitor TP9 on channel 1 of the oscilloscope. Monitor TP5 on channel 2 of the oscilloscope. Adjust C55 for 8.8 horizontal divisions between the signals' leading edges (8.8×5 µsec = 44 µsec delay).

3.13 Repeater Configuration

The CI-PM-3 modules at both the base transmitter and paging/repeater must be configured individually. Individual setup procedures must also be followed for analog/digital paging and for digital-only paging.

Note: The CI-PM-3 modules must be set for 2-level signal operation only when configured for use in a paging repeater system.

3.13.1 Base Transmitter Site CI-PM-3 Configuration

The setup instructions of sections 3.5 through 3.12 must be completed prior to commencing setup of the remote paging/repeater site CI-PM-3.

3.13.1.1 Digital-Only Paging

1. Install shunt jumpers JU41-B and JU42-B.
2. Install surface-mount jumpers JU34, JU51, JU20 and/or JU21

3.13.1.2 Analog/Digital Paging

Ensure the TS-64 CTCSS Module, MOD1, is installed. Refer to section 3.13.3 for TS-64 CTCSS Module Configuration.

1. Install shunt jumpers JU8-A, JU10-B, JU41-A and JU42-B.
2. Install surface-mount jumpers JU51, JU20 and/or JU21.
3. Remove surface-mount jumpers JU28, JU30/JU44 and JU34.

3.13.2 Repeater Site CI-PM-3 Configuration

At the remote paging/repeater site, the digital paging signal is received and discriminated by the receiver, regenerated (reshaped) by the CI-PM-3, and re-transmitted through the normal CI-PM-3 data signal path. Analog paging signals are routed from the receiver, through the CI-PM-3, then directly to the transmitter.

The setup instructions of sections 3.5 through 3.12 must be completed prior to commencing setup of the remote paging/repeater site CI-PM-3.

3.13.2.1 Digital-Only Paging and/or Repeater

1. Install shunt jumpers JU7-B, JU8-B, JU41-B and JU42-B.

2. Install surface-mount jumpers JU19/JU45, JU20/JU21, JU22, JU29/JU43, JU34, JU40 and JU51.

3.13.2.2 Analog/Digital Paging

Ensure the TS-64 CTCSS Module, MOD1, is installed. Refer to section 3.13.3 for TS-64 CTCSS Module Configuration.

1. Install shunt jumpers JU7-B, JU8-B, JU10-B, JU41-A and JU42-B.

2. Install surface-mount jumpers JU19/JU45, JU20/JU21, JU22, JU28, JU29/JU43, JU40 and JU51.

3. Remove surface-mount jumper JU34.

3.13.2.3 Analog/Digital Repeater

Ensure the TS-64 CTCSS Module, MOD1, is installed. Refer to section 3.13.3 for TS-64 CTCSS Module Configuration.

1. Install shunt jumpers JU7-B, JU8-B, JU10-B, JU41-A and JU42-B.

2. Install surface-mount jumpers JU19/JU45, JU20/JU21, JU28, JU29/JU43, JU40, JU51 and JU55.

3. Remove surface-mount jumpers JU22 and JU34.

3.13.3 TS-64 Configuration

1. Ensure POLARITY jumper JP7 is installed.

2. For normal operation (i.e. receiver audio is muted until a CTCSS coded transmission is received):

   a) Ensure TS-64 jumper JP11 is removed.

   b) Ground the TS-64 Hang-up Input:

      i) Install jumper JU52, or

ii) Remove jumper JU52, install jumper JU53 and ground CTCSS HU/BUSY input J1 Pin 11.

3. To place the TS-64 in monitor mode (i.e. over-ride the decoder and un-mute the receiver audio for channel monitoring):

   a) Ensure TS-64 jumper JP11 is removed.

   b) Ensure the TS-64 Hang-up Input is floating or above ground potential:

      i) Remove jumpers JU52 and JU53, or

      ii) Remove jumper JU52, install jumper JU53, and leave CTCSS HU/BUSY input J1 Pin 11 floating.

4. To disable paging transmission while the channel is busy:

   a) Install TS-64 jumper JP11.

   b) Remove jumper JU52, install jumpers JU53 and JU54.

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4. Connector Pin Functions And Jumper Functions

4.1 Data / Control Port (Connector J1) Pin Functions

Table 4-1 Data / Control Port (Connector J1) Pin Functions

PIN	NAME	FUNCTION
1	2-Lvl Data	2 Level RS-232 Data input.
2	4-Lvl Data	4 Level RS-232 Data input.
3	Ext Clock	External Clock for 4 Level signal synchronization.
4	2-Lvl/4-Lvl Select	2 Level / 4 Level select. Low = 2 Level, High = 4 Level.
5	A/D Mode Select	Analog / Digital Mode select. Low = Digital, High = Analog.
6	Discr O/P	Discriminator Output from Receiver.
7	PTT	Push To Talk.
8	Ground	Ground.
9	Balanced Audio I/P 1	Balanced Audio Input 1. Routed directly to Transmitter.
10	Balanced Audio I/P 2	Balanced Audio Input 2. Routed directly to Transmitter.
11	Data Out	Regenerated digital data from receiver.
12	HU/Busy	CTCSS Hang Up / Busy signal from optional CTCSS module.
13	No Connection	-
14	No Connection	-
15	No Connection	-

4.2 Motherboard Interface (Connector P1) Pin Functions

Table 4-2 Motherboard Interface Connector P1 Pin Functions

Note: **Bolded** entries are utilized by CI-PM-3

PIN	NAME	FUNCTION
C1	IMC1	Inter-module Communications Line No. 1
B1	5W RX AUDIO	5W RX A/RX B Audio From System Monitor
A1	5W RX AUDIO	5W RX A/RX B Audio From System Monitor
C2	**TX A AUDIO CNTL**	**TX A Audio Control**
B2	**13.8V**	**13.8V from M3 Motherboard J8 (Unregulated)**
A2	**13.8V**	**13.8V from M3 Motherboard J8 (Unregulated)**
C3	IMC2	Inter-module Communications Line No. 2
B3	RX A AMPD AUDIO	RX A Amplified Audio Output
A3	RX B AMPD AUDIO	RX B Amplified Audio Output
C4	**TX B AUDIO CNTL**	**TX B Audio Control**
B4	**9.5V**	**Regulated +9.5V from System Monitor**
A4	**9.5V**	**Regulated +9.5V from System Monitor**
C5	IMC3	Inter-module Communications Line No. 3
B5	RX A 9.5V	RX A Current Sense Output Line (Supply)
A5	RX B 9.5V	RX B Current Sense Output Line (Supply)
C6	**ALARM 1**	**Inter-module Alarm Line No. 1.**
B6	**TX A PTT**	**Transmitter A Press To Talk input.**
A6	**TX B PTT**	**Transmitter B Press To Talk input.**
C7	**ALARM 2**	**Inter-module Alarm Line No. 2.**
B7	RX A 9.5V MON	RX A Current Sense Output Line (Module)
A7	RX B 9.5V MON	RX B Current Sense Output Line (Module)
C8	**ALARM 3**	**Inter-module Alarm Line No. 3**
B8	**RX A COR**	**RX A Carrier Operated Relay Output**

PIN	NAME	FUNCTION
A8	RX B COR	RX B Carrier Operated Relay Output
C9	ALARM 4	Inter-module Alarm Line No. 4
B9	TX A STANDBY	TX A Audio Standby
A9	TX B STANDBY	TX B Audio Standby
C10	RX A SQL OVERRIDE	RX A Squelch Disable Input
B10	RX A DISC O/P	RX A Discriminator Output
A10	TX A PTT OUT	TX A Microphone Press To Talk Output
C11	ALARM 5	Inter-module Alarm Line No. 5
B11	SPARE 5	Inter-module Spare Line No. 5
A11	SPARE 6	Inter-module Spare Line No. 6
C12	RX A SQL FLAT	RX A Squelched, Flat Audio Output
B12	RX A ISO COR A	RX A Isolated Carrier Operated Relay, Side A O/P
A12	RX A ISO COR K	RX A Isolated Carrier Operated Relay, Side K O/P
C13	ALARM 6	Inter-module Alarm Line No. 6
B13	RX A DISC L/P O/P	RX A Discriminator Low-Pass Audio Output
A13	RX B DISC L/P O/P	RX B Discriminator Low-Pass Audio Output
C14	RX B SQL DE-EMP	RX B Squelched, De-Emphasized Audio Output
B14	SPARE 3	Inter-module Spare Line No. 3
A14	SPARE 4	Inter-module Spare Line No. 4
C15	ALARM 7	Inter-module Alarm Line No. 7
B15	RX A SIG STREN	RX A Signal Strength Indicator Output
A15	RX B SIG STREN	RX B Signal Strength Indicator Output
C16	TX B BAL I/P 1	TX B Balanced Audio Input, Side 1
B16	TX B SUBT I/P 1	TX B Subtone Audio Input No. 1
A16	TX B PTT OUT	TX B Microphone Press To Talk Output
C17	ALARM 8	Inter-module Alarm Line No. 8
B17	TX A VSWR FWD	TX A VSWR Forward Level Indicator Output
A17	TX B VSWR FWD	TX B VSWR Forward Level Indicator Output
C18	TX A BAL I/P 1	TX B Balanced Audio Input, Side 1
B18	TX A BAL I/P 2	TX B Balanced Audio Input, Side 2
A18	TX B BAL I/P 2	TX B Balanced Audio Input, Side 2
C19	SPARE 1	Inter-module Spare Line No. 1
B19	TX A VSWR REV	TX A VSWR Reverse Level Indicator Output
A19	TX B VSWR REV	TX B VSWR Reverse Level Indicator Output
C20	SPARE 2	Inter-module Spare Line No. 2
B20	TX A DIR MOD	TX A Direct Modulation Input
A20	TX B DIR MOD	TX B Direct Modulation Input
C21	TX A CSEL D0	TX A Channel Select Line No. D0
B21	TX A CSEL D1	TX A Channel Select Line No. D1
A21	TX A CSEL D2	TX A Channel Select Line No. D2
C22	TX A SUBT I/P 1	TX A Subtone Audio Input No. 1
B22	RX A MUTE	RX A Mute Input
A22	RX A SQL DE-EMP	RX A Squelched, De-Emphasized Audio Output
C23	TX A CSEL D3	TX A Channel Select Line No. D3
B23	RX A CSEL D0	RX A Channel Select Line No. D0
A23	RX A CSEL D1	RX A Channel Select Line No. D1
C24	TX A SUBT I/P 2	TX A Subtone Audio Input No. 2
B24	RX A BAL O/P 1	RX A Balanced Audio Output, Side 1
A24	RX A BAL O/P 2	RX A Balanced Audio Output, Side 2
C25	RX A CSEL D2	RX A Channel Select Line No. D2
B25	RX A CSEL D3	RX A Channel Select Line No. D3
A25	TX B CSEL D0	TX B Channel Select Line No. D0
C26	TX B SUBT I/P 2	TX B Subtone Audio Input No. 2
B26	RX B SQL OVERRIDE	RX B Squelch Disable Input

PIN	NAME	FUNCTION
A26	RX B MUTE	RX B Mute Input
C27	TX B CSEL D1	TX B Channel Select Line No. D1
B27	TX B CSEL D2	TX B Channel Select Line No. D2
A27	TX B CSEL D3	TX B Channel Select Line No. D3
C28	RX B DISC O/P	RX B Discriminator Audio Output
B28	RX B ISO COR K	RX B Isolated Carrier Operated Relay, Side K O/P
A28	RX B ISO COR A	RX B Isolated Carrier Operated Relay, Side A O/P
C29	RX B CSEL D0	RX B Channel Select Line No. D0
B29	RX B CSEL D1	RX B Channel Select Line No. D1
A29	RX B CSEL D2	RX B Channel Select Line No. D2
C30	RX B BAL O/P 1	RX B Balanced Audio Output, Side 1
B30	RX B BAL O/P 2	RX B Balanced Audio Output, Side 2
A30	RX B SQL FLAT	RX B Squelched, Flat Audio Output
C31	RX B CSEL D3	RX B Channel Select Line No. D3
B31	RX A PRIORITY COR	RX A Priority COR (not affected by Mute)

4.3 CI-PM-3 Data Delay Jumper Settings

Table 4-3 Delay Settings

JUMPER SETTINGS				DELAY	DISTANCE	DISTANCE
JU33	JU32	JU31	JU35	(μSec)	(km)	(mi)
A	A	A	A	4	1.20	0.75
A	A	B	A	8	2.40	1.49
A	A	A	C	12	3.60	2.24
A	B	A	A	16	4.80	2.98
A	A	A	E	20	6.00	3.73
A	B	B	C	24	7.20	4.47
A	B	B	A	32	9.60	5.97
A	A	B	E	40	12.00	7.46
A	B	A	C	48	14.40	8.95
B	A	A	A	64	19.20	11.93
A	B	A	E	80	24.00	14.91
A	B	B	C	96	28.80	17.90
B	A	B	A	128	38.40	23.86
A	B	B	E	160	48.00	29.83
B	A	A	C	192	57.60	35.79
B	B	A	A	256	76.80	47.72
B	A	A	E	320	96.00	59.65
B	A	B	C	384	115.20	71.59
B	B	A	B	512	153.60	95.45
B	A	B	E	640	192.00	119.31
B	B	A	C	768	230.40	143.17
B	B	A	D	1024	307.20	190.89
B	B	A	E	1280	384.00	238.62
B	B	A	F	1536	460.80	286.34

4.4 CI-PM-3 Circuit Board Jumpers

Table 4-4 CI-PM-3 Default Jumper Settings

REF. DESIG.	DESCRIPTION	JUMPER TYPE	DEFAULT POSITION
JU1	2-LVL Polarity Select (A = Normal; B = Inverted)	Shunt	A
JU2	4-LVL Polarity Select (A = Normal; B = Inverted)	Shunt	A
JU3	RX A Balanced O/P 1 Enable	SM Solder	Not Installed
JU4	RX A Balanced O/P 2 Enable	SM Solder	Not Installed
JU5	XO Polarity Select (A = Normal; B = Inverted)	Shunt	B
JU6	XO Select (A=OCXO; B=VCXO)	Shunt	A
JU7	Data Regeneration (A = Disable; B = Enable)	SM Solder	A
JU8	Data Input (A = Data/Ctrl Port; B=RX A Regenerated Data)	SM Solder	A
JU9	Discriminator O/P To Front Panel J1 Enable	SM Solder	Not Installed
JU10	Repeater CTCSS Enable (A = Disable; B = Enable)	SM Solder	A
JU11	TX A Direct Modulation Enable	SM Solder	Installed
JU12	TX B Direct Modulation Enable	SM Solder	Not Installed
JU13	TX A Subtone I/P 2 Enable	SM Solder	Installed
JU14	TX B Subtone I/P 2 Enable	SM Solder	Not Installed
JU15	TX A Balanced I/P 1 Enable	SM Solder	Installed
JU16	TX B Balanced I/P 1 Enable	SM Solder	Not Installed
JU17	TX A Audio Control Enable	SM Solder	Installed
JU18	TX B Audio Control Enable	SM Solder	Not Installed
JU19	RX A COR Enable	SM Solder	Not Installed
JU20	TX A PTT Enable	SM Solder	Installed
JU21	TX B PTT Enable	SM Solder	Not Installed
JU22	Repeater PTT Enable	SM Solder	Not Installed
JU23	Level Select (A=2/4-LVL; B=4-LVL)	Shunt	A
JU24	TX A Balanced I/P 2 Enable	SM Solder	Installed
JU25	TX B Balanced I/P 2 Enable	SM Solder	Not Installed
JU26	Alarm 7 To TX A and B Balanced O/P 1 Enable	SM Solder	Installed
JU27	Alarm 5 To TX A and B Balanced O/P 2 Enable	SM Solder	Installed
JU28	CTCSS RX A Mute Bypass	SM Solder	Not Installed
JU29	RX A Discriminator Output Enable	SM Solder	Not Installed
JU30	RX A Mute Enable	SM Solder	Not Installed
JU31	Data Delay Selection (Refer to Table 4-3)	Shunt	A
JU32	Data Delay Selection (Refer to Table 4-3)	Shunt	A
JU33	Data Delay Selection (Refer to Table 4-3)	Shunt	A
JU34	CTCSS PTT Bypass	SM Solder	Installed
JU35	Data Delay Selection (A - F, Refer to Table 4-3)	Shunt	A
JU36	Data Delay/By-Pass	Shunt	Bypass
JU37	Switched 8.0 Volts For PLL I/O Circuitry	SM Solder	Not Installed
JU38	Switched 8.0 Volts For Data Delay Circuitry	SM Solder	Not Installed
JU39	Switched 5.0 Volts For PLL I/O Circuitry	SM Solder	Not Installed
JU40	Switched 5.0 Volts For Regenerated PTT and Data Delay Circuitry	SM Solder	Not Installed
JU41	Analog/Digital Mode Over-ride	SM Solder	A
JU42	2-LVL / 4-LVL Mode Over-ride	SM Solder	A
JU43	RX B Discriminator O/P Enable	SM Solder	Not Installed
JU44	RX B Mute Enable	SM Solder	Not Installed
JU45	RX B COR Enable	SM Solder	Not Installed
JU46	RX B Balanced O/P 1 Enable	SM Solder	Not Installed
JU47	RX B Balanced O/P 2 Enable	SM Solder	Not Installed
JU48	External Clock Enable (A = Disable; B = Enable)	Shunt	A
JU49	Switched 5.0 Volts For 2-LVL / 4-LVL Switching Circuitry	SM Solder	Installed

REF. DESIG.	DESCRIPTION	JUMPER TYPE	DEFAULT POSITION
JU50	RS-232 Data Out Enable	SM Solder	Not Installed
JU51	Repeater Digital-Only PTT Enable	SM Solder	Not Installed
JU52	TS-64 Hang-up RX Mute	SM Solder	Not Installed
JU53	TS-64 Busy Input Enable	SM Solder	Not Installed
JU54	TS-64 Busy Input Connect to COR	SM Solder	Not Installed
JU55	TS-64 Repeater PTT Enable (Analog/Digital only)	SM Solder	Not Installed

4.5 TS-64 MOD1 Jumper Settings - (If installed)

Table 4-5 CTCSS Jumper Settings

REF. DESIG.	DESCRIPTION	DEFAULT POSITION
JP1-JP6	CTCSS Tone Frequency Select	*
JP7	RX Audio Mute Polarity (Installed: Mute = Open, Not Installed: Mute = Ground)	Installed
JP8-JP10	TX Time-Out-Timer Interval Select	*
JP11	Hang-Up/Busy-Input Configure (Installed = Busy-Input, Not Installed = Hang-Up Input)	Not Installed

Note: Refer to TS-64 Instruction Sheet for configuration details.

4.6 4-Level Modulation Bit Pattern

Table 4-6 4-Level Modulation Bit Pattern

J1-PIN1 (BIT 0)	J1-PIN2 (BIT 1)	DEVIATION SETTING
0	0	- 4800 Hz
0	1	- 1600 Hz
1	1	+ 1600 Hz
1	0	+ 4800 Hz

4.7 Transmitter Audio Processor Jumper Settings

Table 4-7 Transmitter Audio Processor V1.6 Settings

JUMPER	POSITION
JU1	Y
JU6	Replaced with 33nF
JU8	Short
JU9	Open
JU11	Short
JU15	Short
JU27	Y
JU28	Y
JU34	Y
JU35	Y
JU38	Y

Note: All other jumper settings as per the factory defaults.

Table 4-8 Transmitter Audio Processor V1.8 Settings

JUMPER	POSITION
JU1	X
JU5	Y
JU6	Replaced with 33nF
JU8	Short
JU9	Open
JU11	Y
JU15	Short
JU27	Y
JU28	Y
JU34	Y
JU35	Y
JU37	Short
JU38	Y

Note: All other jumper settings as per the factory defaults.

4.8 Receiver IF / Audio PCB Jumper Settings

Table 4-9 Receiver IF / Audio PCB Jumper Settings

JUMPER	POSITION
JU5	Short
JU25	Short

Note: All other jumper settings as per the factory defaults.

4.9 CI-PM-3 Test Points

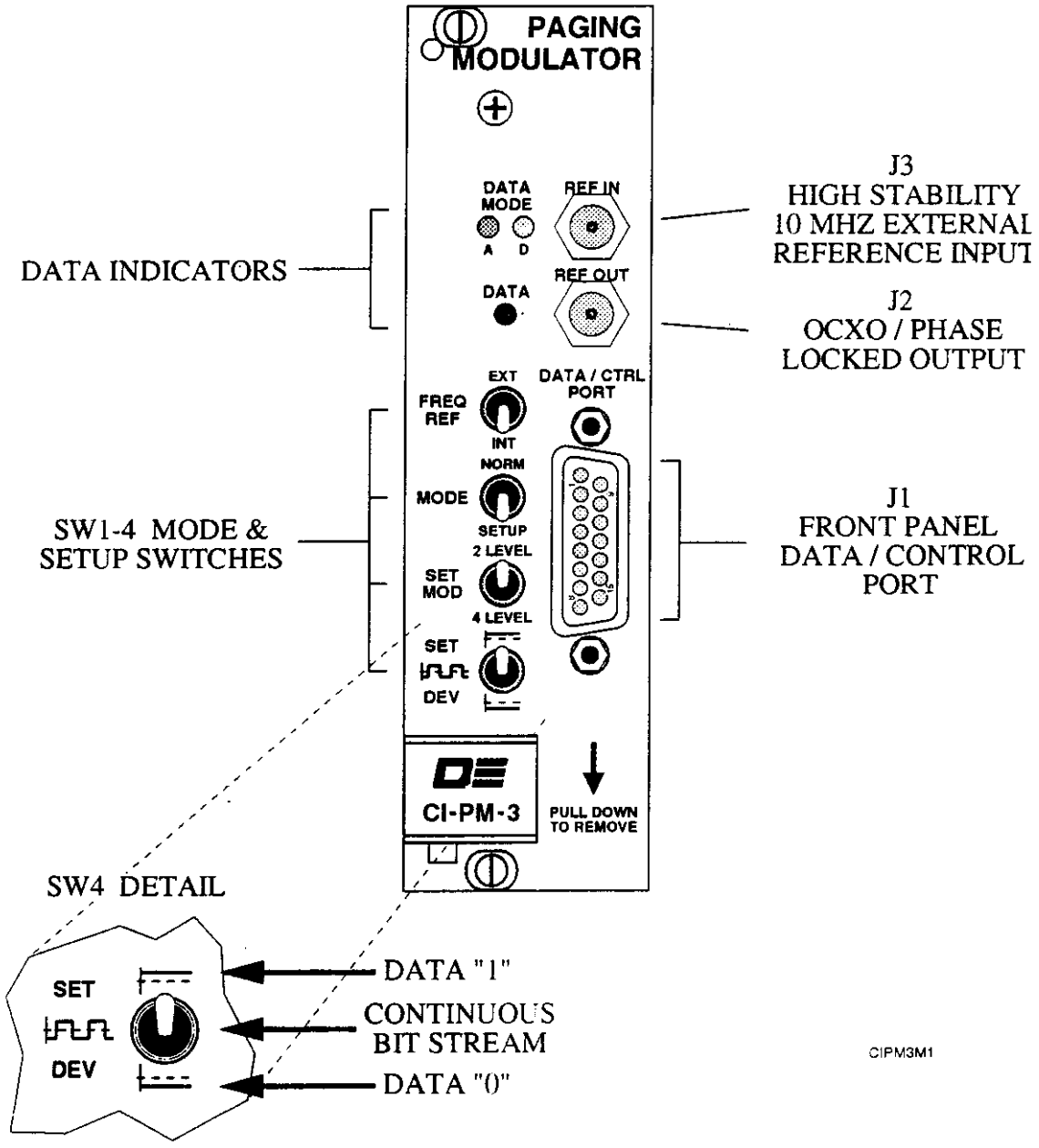
Table 4-10 CI-PM-3 Test Points

TEST POINT	DESCRIPTION
TP1	+8 Vdc Supply
TP2	+4 Vdc Supply
TP3	+5 Vdc Supply
TP4	Analog / Digital Mode (High = Digital, Low = Analog)
TP5	2 Level Data (TTL)
TP6	OCXO 9.5 Vdc Supply
TP7	Positive and Negative Edge Integrator Output
TP8	Data Delay Programmable Counter Output.
TP9	Input to Data Delay Circuitry
TP10	2 Level Data
TP11	Level Adjusted Paging Signal
TP12	OCXO Reference Adjust (nominally 2.5 Vdc)
TP13	PLL Correction Voltage

5. ILLUSTRATIONS AND SCHEMATIC DIAGRAMS

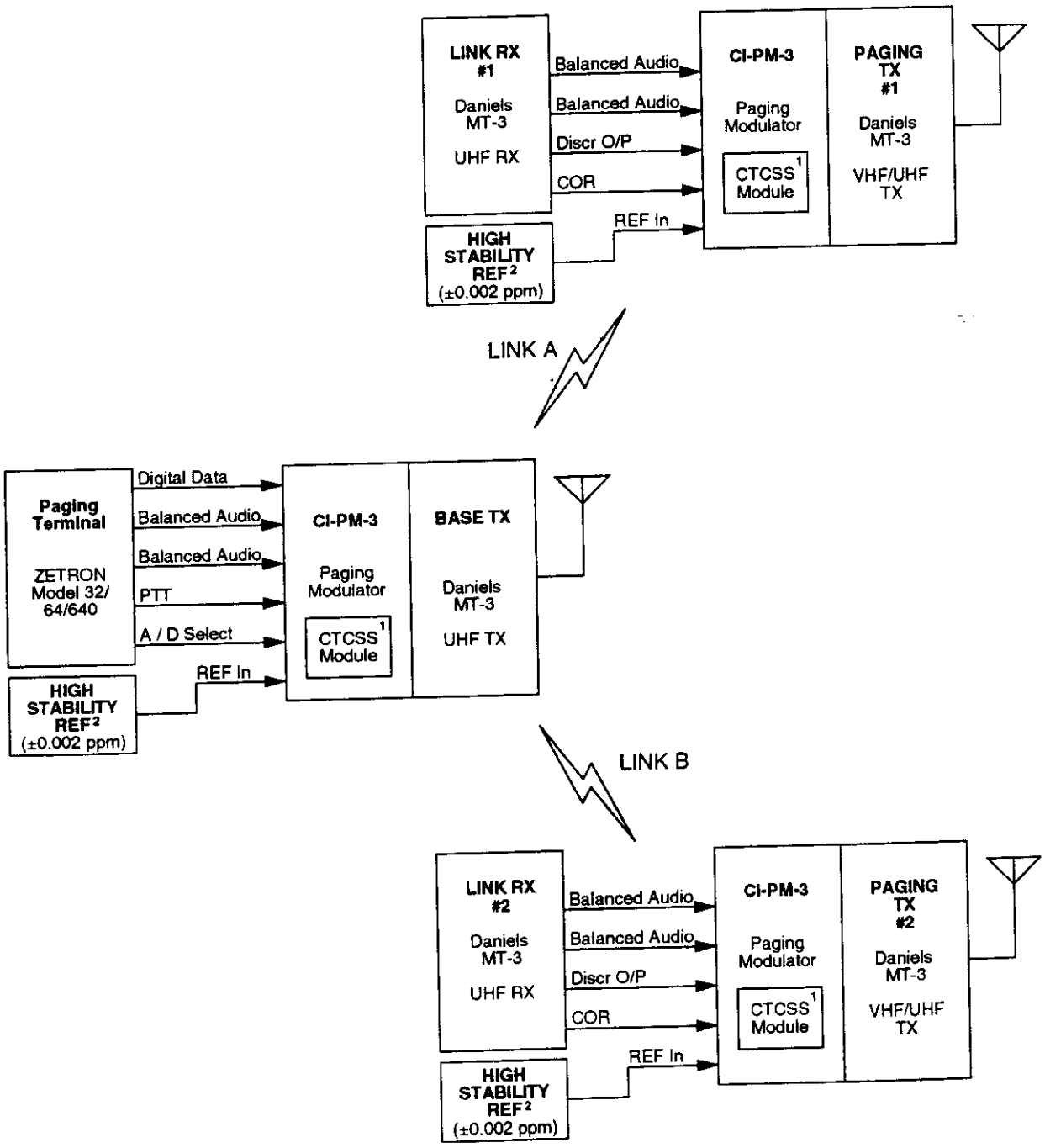
5.1 CI-PM-3 Front Panel Controls

Figure 5-1 CI-PM-3 Front Panel Controls



5.2 Simulcast Paging Example

Figure 5-2 Simulcast Paging Example



Notes:

1. CTCSS selects Analog / Digital Paging Mode.
2. High stability oscillators are referenced to a common GPS, WWV or other signal.

CIPM3M2