NAT4882®
Programmer Reference Manual

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About This Manual

The NAT4882 is an application-specific integrated circuit developed by National Instruments. The NAT4882 is an IEEE 488.2 Controller chip designed to perform all the interface functions defined in the IEEE 488.1-1987 standard and the additional requirements of the IEEE 488.2-1987 standard. The NAT4882 performs complete IEEE 488 Talker, Listener, and Controller functions and is software compatible with the NEC μPD7210 and TI TMS9914A GPIB controller chips. The NAT4882 provides the core of a complete, high-speed IEEE 488.2 interface.

This manual describes the programmable features of the NAT4882 and contains information suitable for programmers and engineers who wish to write software for the NAT4882.

Organization of This Manual

This manual is divided into the following sections and appendixes:

- Chapter 1, *Introduction and General Description*, contains a list of NAT4882 features, a functional description of the NAT4882, a list of GPIB and interrupt capabilities, and a discussion of the addressing scheme used by the NAT4882.
- Chapter 2, *NAT4882 Interface Registers*, contains information on the use of the NAT4882 internal program registers. It also contains NAT4882 address maps and detailed descriptions of the NAT4882 interface registers.
- Chapter 3, *NAT4882 Programming Considerations*, explains important considerations for programming the NAT4882 in 7210 mode.
- Appendix A, *Multiline Interface Command Messages*, lists the multiline interface messages and describes the mnemonics and messages that correspond to the interface functions. These functions include initializing the bus, addressing and unaddressing devices, and setting device modes for local or remote programming. The multiline interface messages are IEEE 488-defined commands that are sent and received with ATN TRUE.
- Appendix B, *Mnemonics Key*, is an easy reference table that defines the mnemonics (abbreviations) used throughout this manual for functions, remote messages, local messages, states, bits, registers, integrated circuits, and system functions.
- Appendix C, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products and manuals.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including acronyms, abbreviations, metric prefixes, mnemonics, and symbols.
- The *Index* contains an alphabetical list of key terms and topics used in this manual, including the page number where you can find each one.

Conventions Used in This Manual

The following conventions are used to distinguish elements of text throughout this manual:

italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.
7210 mode	7210 mode is used throughout this manual to refer to the NEC μPD7210 software compatibility mode.
9914 mode	9914 mode is used throughout this manual to refer to the TI TMS9914A software compatibility mode.
IEEE 488 and IEEE 488.2	IEEE 488 and IEEE 488.2 are used throughout this manual to refer to the ANSI/IEEE Standard 488.1-1987 and the ANSI/IEEE Standard 488.2-1987, respectively, which define the GPIB.

Abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms are listed in the *Glossary*.

Related Documents

The following documents contain information that may be helpful as you read this manual:

- ANSI/IEEE Standard 488.1-1987, *IEEE Standard Digital Interface for Programmable Instrumentation*.
- ANSI/IEEE Standard 488.2-1987, *IEEE Standard Codes, Formats, Protocols, and Common Commands*.
- *NAT4882BPL IEEE 488.2 Controller Chip data sheet*, National Instruments Corporation (part number 340495-01).

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National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix C, *Customer Communication*, at the end of this manual.

Chapter 1
Introduction and General Description

This chapter contains a list of NAT4882 features, a functional description of the NAT4882, a list of GPIB and interrupt capabilities, and a discussion of the addressing scheme used by the NAT4882.

The NAT4882 is an IEEE 488.2 Controller chip designed to perform all the interface functions defined in the IEEE 488.1-1987 specification and the additional requirements and recommendations of the IEEE 488.2-1987 specification. The NAT4882 manages the IEEE 488 interface functions with a set of control and status registers that increase the throughput of driver software and simplify hardware and software design. The NAT4882 performs complete IEEE 488 Talker, Listener, and Controller functions and is software-compatible with the NEC μPD7210 and TI TMS9914A chips. The compatibility mode can be determined by either hardware or software. The NAT4882 is a surface-mountable 68-pin Plastic Leaded Chip Carrier (PLCC) part.

NAT4882 Features

The National Instruments NAT4882 has all the features necessary to provide a high-performance IEEE 488 interface. These features include the following:

- Can use all IEEE 488.1 interface functions and IEEE 488.2 requirements
    - Source Handshake (SH1)
    - Acceptor Handshake (AH1)
    - Talker or Extended Talker (T5 or TE5)
    - Listener or Extended Listener (L3 or LE3)
    - Service Request (SR1)
    - Remote/Local (RL1)
    - Parallel Poll
      remote configuration (PP1)
      local configuration (PP2)
    - Device Clear (DC1)
    - Device Trigger (DT1)
    - Controller, all capabilities (C1-C5)
    - Busline Monitoring
    - Preferred Implementation of requesting service

- Can use six addressing modes

  - Automatic single or dual primary addressing detection
  - Automatic single primary with single secondary address detection
  - Single or dual primary with multiple secondary addressing
  - Multiple primary addressing

- Software-compatible with NEC μPD7210 and TI TMS9914A Controller chips

- Automatic EOS and/or NL message detection
- DMA support with automatic END message generation or automatic holdoff on terminal count

- Ability to detect bus synchronization

- Programmable T1 delay (2 μsec, 500 nsec, or 350 nsec)

- Automatic IEEE 488 command processing and undefined command read capability

- Programmable bus transceiver support (Texas Instruments, National Semiconductor, Motorola, Intel)

NAT4882 Functional Description

The NAT4882 can be characterized as a bus translator, converting messages and signals from the CPU into appropriate GPIB messages and signals. In GPIB terminology, the NAT4882 implements GPIB board and device functions to communicate with the central processor and memory. For the computer, the NAT4882 is an interface to the outside world.

Figure 1-1 shows a block diagram of a typical application using the NAT4882 to implement an IEEE 488.2 interface.

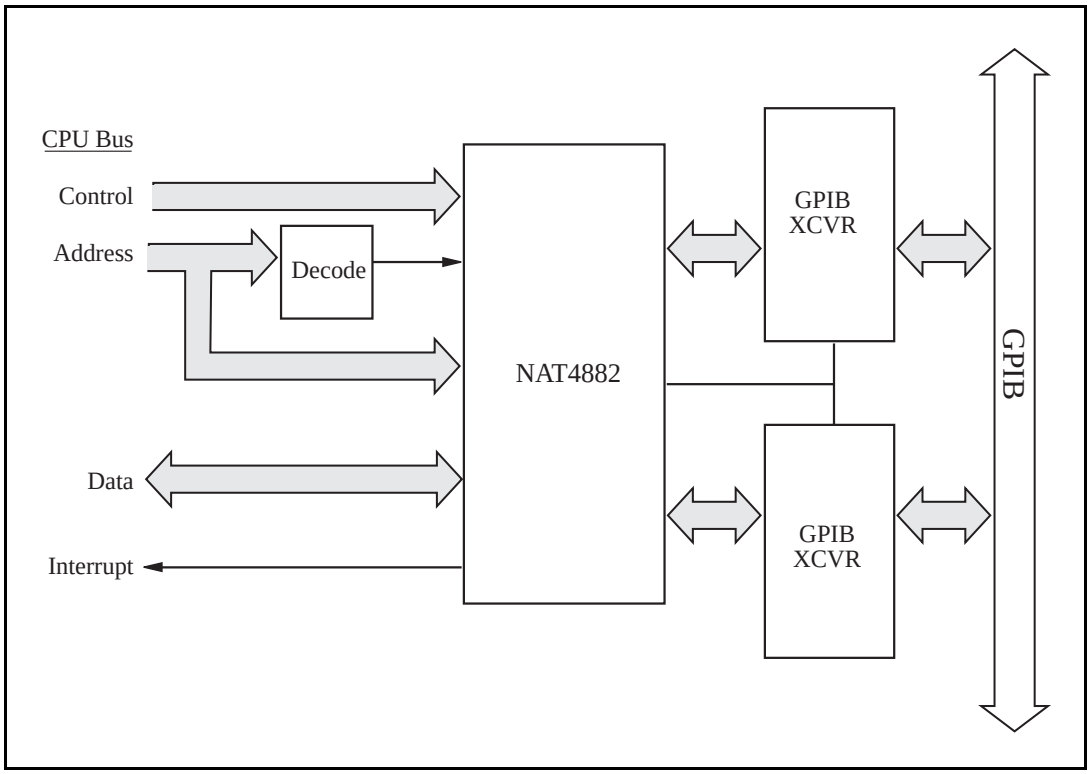


Figure 1-1. NAT4882 Implementation Block Diagram

In all applications, the NAT4882 must be connected to the GPIB via special transceivers. The NAT4882 supplies the control signals necessary to interface to the IEEE 488 bus using several different types of transceivers, such as the 75160 and 75162 from National Semiconductor or Texas Instruments.

The NAT4882 interfaces to a CPU or local bus. Data is transferred to and from the registers of NAT4882 from the local bus to perform configuration, check status, or transfer data across the IEEE 488 bus. The NAT4882 can interrupt the CPU on many conditions. The NAT4882 also can use a Direct Memory Access (DMA) Controller for enhanced transfer speed.

Figure 1-2 shows a block diagram of the NAT4882.

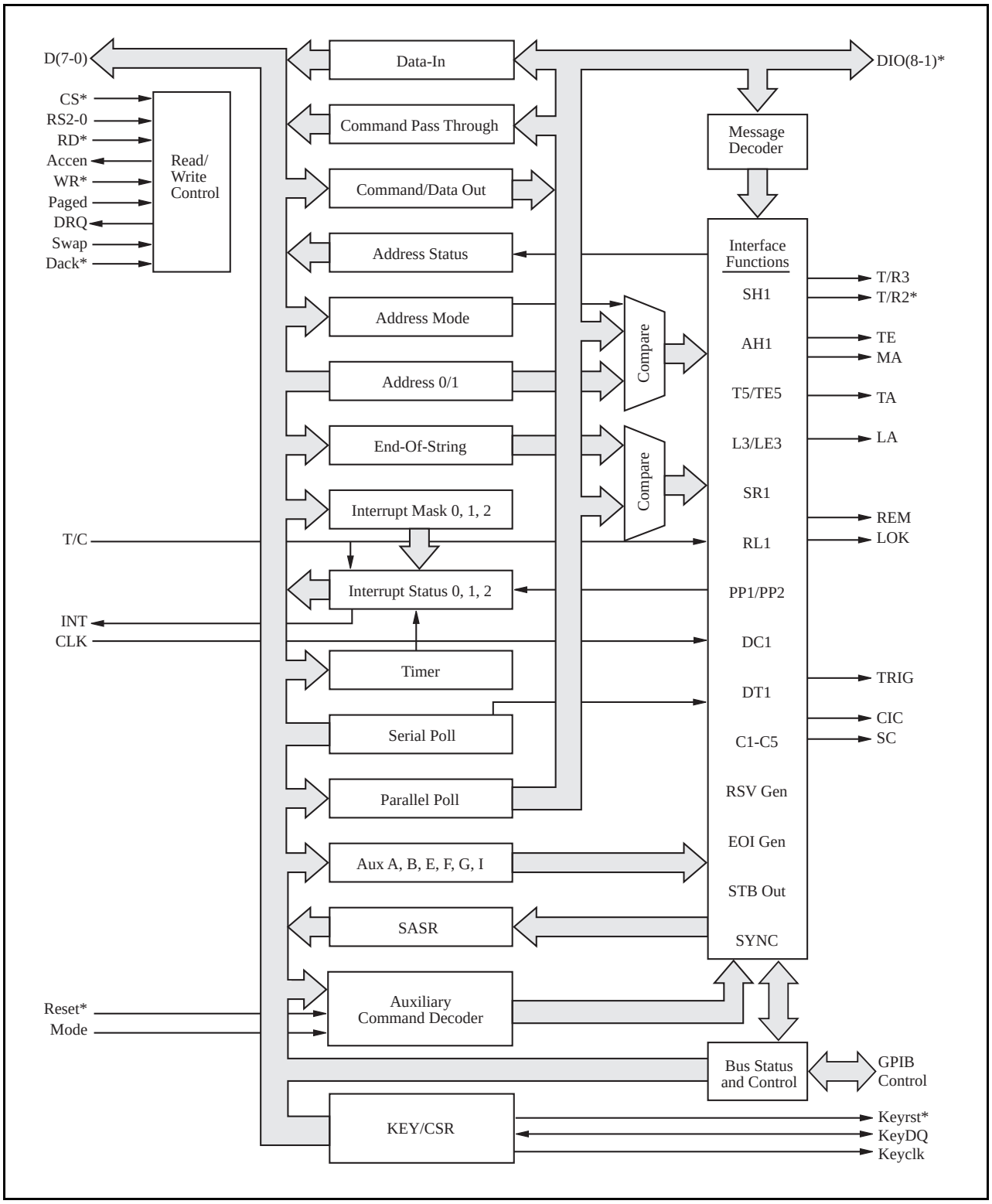


Figure 1-2. NAT4882 Block Diagram

The interface includes the following major components:

- *Read/Write Control* converts the CPU signals presented to the NAT4882 to read and write signals for each internal register.
- *Internal NAT4882 Registers* configure and control the operation of the NAT4882. They transfer data between the NAT4882 and the GPIB bus, report status information, and set the operating modes. Each register is described in detail in Chapter 2, *NAT4882 Interface Registers*.
- *Interface Functions* implement the interface functions described in the IEEE 488.1-1978 specification. The interface functions are controlled by some of the internal registers, and you can use other internal registers to monitor their status. The interface functions drive and receive the GPIB control signals and generate the signals to control the GPIB transceivers.
- *Message Decoding* receives the GPIB data lines and decodes the GPIB commands that affect the operation of the interface functions.

GPIB Capabilities

Table 1-1 lists the capabilities of the NAT4882 in terms of the IEEE 488 standard codes.

Table 1-1. NAT4882 IEEE 488 Interface Capabilities

Capability Code	Description
SH1	Complete Source Handshake capability
AH1	Complete Acceptor Handshake capability, DAC and RFD Holdoff on certain events
T5	Complete Talker capability Basic Talker Serial Poll Talk Only mode Unaddressed on MLA Send END or EOS Dual primary addressing
TE5	Complete Extended Talker capability Basic Extended Talker Serial Poll Talk Only mode Unaddressed on MSA*LPAS Send END or EOS Dual extended addressing with software assist

(continues)

Table 1-1. NAT4882 IEEE 488 Interface Capabilities (continued)

Capability Code	Description
L3	Complete Listener capability Basic Listener Listen Only mode Unaddressed on MTA Detect END or EOS Dual primary addressing
LE3	Complete Extended Listener capability Basic Extended Listener Listen Only mode Unaddressed on MSA*TPAS Detect END or EOS Dual extended addressing with software assist
SR1	Complete Service Request capability
RL1	Complete Remote/Local capability with software interpretation
PP1	Remote Parallel Poll configuration
PP2	Local Parallel Poll configuration with software assist
DC1	Complete Device Clear capability with software interpretation
DT1	Complete Device Trigger capability with software interpretation
C1 through C5	Complete Controller capability System Controller Send IFC and take charge Send REN Respond to SRQ Send interface messages Received control Parallel Poll Take control synchronously or asynchronously
E1, E2	Provides an output signal (T/R3) that can be used to switch the GPIB transceivers from Three-state drivers to open Collector drivers during Parallel Polls

The NAT4882 has complete Source and Acceptor Handshake capability. It can operate as a basic Talker or Extended Talker and can respond to a Serial Poll. If you place it in a talk-only mode, it is unaddressed to talk when it receives its listen address. The NAT4882 GPIB interface can also operate as a basic Listener or Extended Listener. If you place it in a listen-only mode, it is unaddressed to listen when it receives its talk address. The NAT4882 can request service from another Controller. The ability to place the NAT4882 in local mode is software-dependent. The interface can conduct a Parallel Poll, although local configuration requires software assistance.

Device Clear and Trigger capability is included in the interface, but the interpretation is software-dependent.

The NAT4882 includes all Controller functions, as specified by the IEEE 488 standard. These functions include the capability to do the following:

- Act as System Controller
- Initialize the interface
- Send Remote Enable
- Respond to Service Request
- Send multiline command messages
- Receive control
- Pass control
- Conduct a Parallel Poll
- Take control synchronously or asynchronously

Interrupt Capabilities

You can enable and disable NAT4882 interrupt sources individually by using the three Interrupt Mask Registers (IMR0, IMR1, and IMR2). All unmasked interrupt conditions in the NAT4882 are logically combined (ORed) before being driven on the NAT4882 IRQ line.

7210 Mode Interrupts

The interrupt conditions in 7210 mode are as follows:

- GPIB Data In (DI)
- GPIB Data Out (DO)
- END received (END RX)
- GPIB Command Out (CO)
- Remote Mode Change (REMC)
- GPIB Handshake Errors (ERR)
- Lockout Change (LOKC)

- Address Status Change (ADSC)
- Secondary Address received (APT)
- Service Request received (SRQI)
- Trigger command received (DET)
- Device Clear received (DEC)
- Unrecognized command received (CPT)
- Status Byte Out (STBO)
- Interface Clear (IFC)
- Attention (ATN)
- Time Out (TO)
- GPIB Synchronized (SYNC)

For more information on the 7210 mode interrupt conditions, refer to *Interrupt Status Register 0, 1,* and *2* in the *7210 Mode Registers* section of Chapter 2, *NAT4882 Interface Registers*.

9914 Mode Interrupts

The interrupt conditions in 9914 mode are as follows:

- GPIB Byte In (BI)
- GPIB Byte Out (BO)
- END message received (END)
- Serial Poll Active State (SPAS)
- Remote/Local Change (RLC)
- My Address Change (MAC)
- Group Execute Trigger (GET)
- Transmit Error (ERR)
- Unrecognized Command (UNC)
- Secondary Address received (APT)
- Device Clear Active State (DCAS)

- My Address (MA)
- Service Request received (SRQ)
- Interface Clear (IFC)
- Status Byte Out (STBO)
- Local Lockout Change (LLOC)
- Attention (ATN)
- Time Out (TO)
- Controller-in-Charge (CIC)

For more information on the 9914 mode interrupt conditions, refer to *Interrupt Status Register 0*, *1*, and *2* in the *9914 Mode Registers* section of Chapter 2, *NAT4882 Interface Registers*.

Addressing Schemes

Because the NAT4882 was designed to be completely compatible with the NEC μPD7210 or TI TMS9914A, only three register select lines are available, providing access to eight register locations. To include the additional features of the NAT4882, there are two methods of accessing additional registers: the hidden registers method and the paged registers method. The NAT4882 comes out of reset with a completely compatible register map so that existing software for either chip can run with no modification. By accessing these additional registers, features can be invoked under software control.

Hidden registers have always been a part of the μPD7210 chip, but their number has increased in the NAT4882, and their use has been expanded to the TMS9914A chip. Hidden registers provide additional write-only registers by using part of the data byte being written as an address. The upper three or four bits of a write to the Auxiliary Mode Register (AUXMR) in 7210 mode or the Accessory Register (ACCR) in 9914 mode select the register to be written. The lower four or five bits contain the data written to the register.

You can add additional readable and writeable registers to the 7210 mode by using one of two methods to page them into the locations of existing registers. If you issue the page-in auxiliary command, the additional registers are paged in until after the next CPU access to the NAT4882. If you use this method, you must issue the page-in command before every access to a paged register. Alternately, you can page in the registers by asserting the Page-In pin during an access. If you use this method, you can connect the Page-In pin to an additional address line, so that the paged registers appear at a different offset, and the NAT4882 occupies sixteen register locations. This method is the more efficient of the two, and is recommended unless it is necessary that the NAT4882 only occupy eight register locations.

The TMS9914A chip has two unused readable locations and one unused writeable location that are used to add additional registers. Four additional write-only registers, located at the same offset, are added to the 9914 mode, and are made available by issuing a page-in command. Each register has its own page-in command, and unlike in the 7210 mode, a CPU access does not page out a register. You can only page out a register by issuing the page-in command of another register or by issuing the clear page-in command. The two unused readable locations are used for two new read-only registers after any page-in command has been issued. If no page-in command is issued, the NAT4882 does not drive the data bus when an unused location is accessed. The ACCEN pin indicates when registers have been paged in.

Chapter 2
NAT4882 Interface Registers

This chapter contains information on the use of the NAT4882 internal program registers. It also contains NAT4882 address maps and detailed descriptions of the NAT4882 interface registers.

Software written for the NAT4882 controls the GPIB interface through a set of hardware registers. The internal registers of the NAT4882 IEEE 488.2 Controller are mapped between offsets 0 and 7 hex. Many of the registers are read-only or write-only. Some registers are not storage registers at all, but buffers through which status signals can be read or through which control signals can be sent. Two special register types are also located in the NAT4882: multiple *hidden* registers are accessed through a single register space by using the upper data bits to distinguish the registers; *Paged* registers are made accessible by writing a command to the NAT4882 before accessing the register.

The NAT4882 operates in two different compatibility modes: NEC μPD7210 mode and TI 9914A mode. The registers are mapped differently for the two modes and some registers exist in only one of the modes.

Note: Throughout this manual, *7210 mode* is used to refer to the NEC μPD7210 software compatibility mode, and *9914 mode* is used to refer to the TI TMS9914A software compatibility mode.

Register Description Format

The remainder of this chapter describes each register in the 7210 and 9914 compatibility modes. Each register description gives the address, type, word size, and bit map of the register, followed by a detailed description of each bit.

The bit map of each register shows a diagram of the register with the most significant bit (bit 7 for an 8-bit register) shown on the left, and the least significant bit (bit 0) shown on the right. A square is used to represent each bit. Each bit is labeled with a name inside its square. An asterisk (*) after the bit name indicates that the signal is active low. An asterisk is equivalent to an overbar.

In many of the registers, several bits are labeled with an X, indicating *don't care* bits. When one of these registers is read, the don't care bits may appear set or cleared but should be ignored, as they have no significance. When a register is written to, these bits should be written as zeros.

The terms *set*, *set true*, and *set to one* are synonymous. The terms *clear*, *set false*, *set to zero*, and *clear to zero* are synonymous. The meanings of *preset* and *reset* are determined by the context in which they are used. Bit signatures are written in uppercase letters.

The term *addressed* indicates that the interface has been configured to perform a function from the GPIB side, while the term *programmed* means that it has been configured from the CPU interface side. This distinction is important to make, because many functions, such as making the interface a Talker or Listener, can be activated from either side.

Where it is necessary to specify a particular bit of a register, the bit position appears as a decimal number in square brackets after the mnemonic. For example, ISR1[1] indicates the DI bit of Interrupt Status Register 1.

A minus sign (-) indicates logical negation. An ampersand (&) represents AND, and a plus sign (+) represents OR in logical expressions.

All numbers, except register offsets, are decimal unless specified otherwise. Register offsets are given in hexadecimal notation.

Uppercase mnemonics are used for control, status, data registers, register contents, and interface functions, as well as GPIB remote messages, commands, and logic states as defined in the IEEE 488 standard.

After a mnemonic of a name is defined, the mnemonic is used thereafter. Appendix B, *Mnemonics Key*, contains a list of all mnemonics used in this manual, along with their type and name. Mnemonics are assigned to messages, states, registers, bits, functions, and integrated circuits. Most mnemonics contain some clue to their meaning. Table 2-1 contains a list of clues to look for.

Table 2-1. Clues to Understanding Mnemonics

Clue	Mnemonic Probably Stands For:
Ends in IE	Interrupt enable bit
Ends in EN	Enable bit
4 letters, ends in S	Interface function as defined in the IEEE 488 standard
Ends in R, R0, R1, R2	GPIB program register
3 letters, uppercase	Remote GPIB message
3 letters, lowercase	Local GPIB message

7210 Mode Registers

The 7210 mode register group consists of 31 registers.

Figure 2-1 shows the register map for the 7210 mode registers, and Figure 2-2 shows the 7210 mode hidden registers. The 7210 hidden registers are accessed by writing to the auxiliary mode register (AUXMR). The upper three or four bits written to the AUXMR determine which hidden register will be accessed, and the lower four or five bits are written to that hidden register as shown in Figure 2-2. The non-shaded registers in Figure 2-1 are normally available in 7210 mode.

The paged registers in 7210 mode, which are shaded in Figure 2-1, can be accessed using two methods. You can issue the Page-In auxiliary command, which makes the paged registers available during the next CPU access to the NAT4882. After this paged access, the registers are paged out. Alternately, you can assert the Page-In pin of the NAT4882 during the access to make the paged registers available. The Page-In pin would commonly be connected as an additional address line so that the paged registers would appear at an address different from the standard 7210 registers, unless address space was limited.

The sections following Figures 2-1 and 2-2 contain detailed function descriptions of all 31 7210 mode registers.

Key

= 7210 Mode Paged Registers
R = Read Register
W = Write Register

		7	6	5	4	3	2	1	0	
DIR	+0	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	R
CDOR		CDO7	CDO6	CDO5	CDO4	CDO3	CDO2	CDO1	CDO0	W
ISR1	+1	CPT	APT	DET	END RX	DEC	ERR	DO	DI	R
IMR1		CPT IE	APT IE	DET IE	END IE	DEC IE	ERR IE	DO IE	DI IE	W
ISR2	+2	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC	R
IMR2		0	SRQI IE	DMAO	DMAI	CO IE	LOKC IE	REMC IE	ADSC IE	W
SPSR	+3	S8	PEND	S6	S5	S4	S3	S2	S1	R
KSR		V3	V2	V1	V0	KEYDQ	MODE	0	0	R
KCR		0	SWAP	MSTD	NO T1	KEYCLK	KEYDATEN	KEYDATA	KEYRST*	W
SPMR		S8	rsv/RQS	S6	S5	S4	S3	S2	S1	W
ADSR	+4	CIC	ATN*	SPMS	LPAS	TPAS	LA	TA	MJMN	R
ADMR		ton	lon	TRM1	TRM0	0	0	ADM1	ADM0	W
CPTR	+5	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0	R
SASR		cdba	AEHS	ANHS1	ANHS2	ADHS	ACRDY	SH1A	SH1B	R
AUXMR		CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0	W
ADR0	+6	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0	R
ISR0		cdba	STBO	NL	EOS	IFCI	ATNI	TO	SYNC	R
IMR0		GLINT	STBO IE	NLEE	BTO	IFCI IE	ATNI IE	TO IE	SYNC IE	W
ADR		ARS	DT	DL	AD5	AD4	AD3	AD2	AD1	W
ADR1	+7	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1	R
BSR		ATN_S	DAV_S	NDAC_S	NRFD_S	EOI_S	SRQ_S	IFC_S	REN_S	R
BCR		ATN_C	DAV_C	NDAC_C	NRFD_C	EOI_C	SRQ_C	IFC_C	REN_C	W
EOSR		EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0	W

Figure 2-1. 7210 Mode Register Map

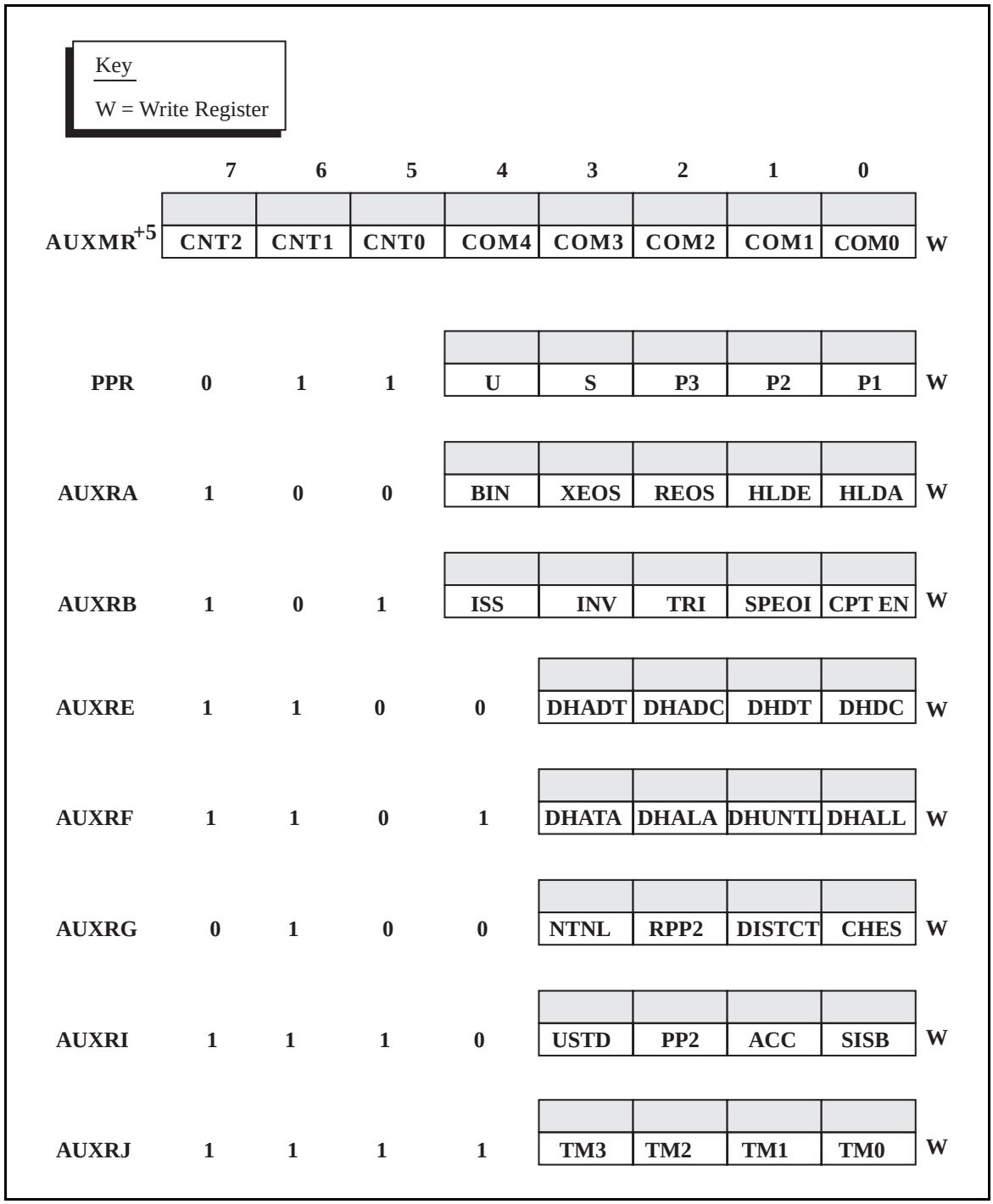


Figure 2-2. 7210 Mode Hidden Registers

Data In Register (DIR)

Access: location 0 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Attributes: Read-Only

7	6	5	4	3	2	1	0	R
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	

The Data In Register (DIR) moves data from the GPIB to the computer when the interface is a Listener. Incoming information is separately latched by this register when a write to the Command/Data Out Register (CDOR) takes place, and is not destroyed. If the TLC is not in continuous mode, GPIB data is latched in this register when ACDS1 & ~ATN and the DI bit in ISR1 is set . The Not Ready For Data (NRFD) message is asserted until the byte is read from the DIR. The Acceptor Handshake (AH) completes automatically after the byte is read unless the TLC is in Ready For Data (RFD) Holdoff mode. In that case, the GPIB Handshake is not finished until the Finish Handshake (FH) auxiliary command is issued telling the NAT4882 to release the Holdoff. By using the RFD Holdoff mode, the same byte may be read several times or a GPIB Talker may be held off until the program is ready to proceed. This register can also be read by asserting the DACK* and RD* pins. For more information on the RFD Holdoff mode, refer to the *Auxiliary Register A* description later in this chapter.

DI1 is the least significant bit of the data byte and corresponds to GPIB data line DIO1. DI8 is the most significant bit of the data byte and corresponds to GPIB DIO8.

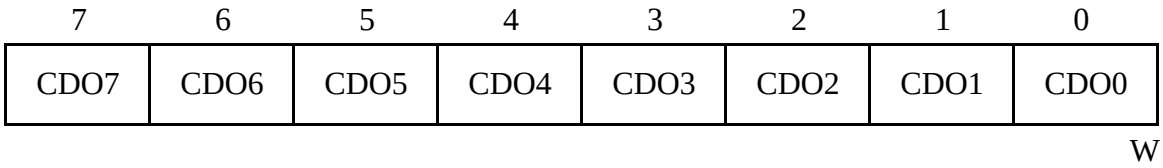
Bit	**Mnemonic**	**Description**
7-0r	DIR[7-0]	GPIB Data lines DIO[8-1]

Command/Data Out Register (CDOR)

Access: location 0 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Attributes: Write-Only



The Command/Data Out Register (CDOR) moves data from the computer to the GPIB when the interface is the GPIB Talker or the Active Controller. Outgoing data is separately latched by this register and is not destroyed by a read from the DIR. When a byte is written to the CDOR, the NAT4882 GPIB Source Handshake (SH) function is initiated (that is, the local message nba is true) and the byte is transferred to the GPIB. This register is also written on the assertion of the WR* signal when DACK* is asserted. The CDOR is a transparent latch; therefore, changes on the CPU data bus (D(7:0)) during write cycles to the CDOR are reflected on the GPIB data bus (DIO(8:1)).

Bit	Mnemonic	Description
7-0w	CDO[7-0]	GPIB Data lines DIO[8-1]

Interrupt Status Register 1 (ISR1)

Access: location 1 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Attributes: Read-Only
Bits are cleared when read and SISB=0

Interrupt Mask Register 1 (IMR1)

Access: location 1 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Attributes: Write-Only

7	6	5	4	3	2	1	0	R
CPT	APT	DET	END RX	DEC	ERR	DO	DI	
CPT IE	APT IE	DET IE	END IE	DEC IE	ERR IE	DO IE	DI IE	
								W

The Interrupt Status Register 1 (ISR1) is made up of eight Interrupt Status bits. The Interrupt Mask Register 1 (IMR1) is made up of eight Interrupt Enable bits that directly correspond to the Interrupt Status bits in ISR1. As a result, ISR1 and IMR1 service eight possible interrupt conditions, where each condition has an Interrupt Status bit and an Interrupt Enable bit associated with it. If the Interrupt Enable bit and the GLINT bit (in ISR0) is true when the corresponding status condition or event occurs, a hardware interrupt request is generated. Bits in ISR1 are set and cleared by the NAT4882 regardless of the status of the Interrupt bits in IMR1. If an interrupt condition occurs at the same time ISR1 is being read, the NAT4882 holds off setting the corresponding Status bit until the read has finished. All bits in IMR1 are cleared by a hardware reset.

Bit	Mnemonic	Description
7r	CPT	Command Pass Through bit
7w	CPT IE	Command Pass Through Interrupt Enable bit
		The CPT bit flags the occurrence of any GPIB command not recognized by the NAT4882, and all following GPIB secondary commands when the Command Pass Through feature is enabled by the CPT ENAB bit, AUXRB[0]w. Any GPIB command message not decoded by the NAT4882 is treated as an undefined command (see Table 2-3 for a list of commands recognized in 7210 mode). However, any addressed command is automatically ignored when the NAT4882 is not addressed. The CPT can also flag the occurrence of a GPIB command or group of commands specified by the AUXRE[3-2]w or AUXRF[3-0]w bits.

Bit **Mnemonic** **Description**

Undefined commands are read using the Command Pass Through Register (CPTR). The NAT4882 holds off the GPIB Acceptor Handshake in the Accept Data State (ACDS) until the program writes the Valid or Non-Valid auxiliary command function code to the AUXMR. If CPT ENAB is cleared, undefined commands are simply ignored. However, commands specified by the AUXRE[3-2]w and AUXRF[3-0]w are still flagged.

CPT is set by:

[UCG + ACG & (TADS + LADS)] & undefined & ACDS & CPT ENAB
+ UDPCF & SCG & ACDS1 & CPT ENAB
+ DHADT & GET & ACDS
+ DHADC & (SDC + DCL) & ACDS
+ DHATA & TAG & ~UNT & ACDS
+ DHALA & LAG & ~UNL & ACDS
+ DHUNTL & (UNT + UNL) & ACDS
+ DHALL & (UCG + ACG + SCG) & ACDS

CPT is cleared by:

pon + (read ISR1) & ~SISB + (read CPT) & SISB

Notes

UCG:	GPIB Universal Command Group message
ACG:	GPIB Addressed Command Group message
GET:	GPIB Group Execute Trigger message
SDC:	GPIB Selected Device Clear message
DCL:	GPIB Device Clear message
UNT:	GPIB Untalk message
UNL:	GPIB Unlisten message
TADS:	GPIB Talker Addressed State
LADS:	GPIB Listener Addressed State
defined:	GPIB command automatically recognized and executed by NAT4882
undefined:	GPIB command not automatically recognized and executed by NAT4882
ACDS:	GPIB Accept Data State
CPT ENAB:	AUXRB[0]w
SISB:	AUXRI[0]w
DHADT:	AUXRE[3]w
DHADC:	AUXRE[2]w
DHATA:	AUXRF[3]w
DHALA:	AUXRF[2]w
DHUNTL:	AUXRF[1]w
DHALL:	AUXRF[0]w
UDPCF:	Undefined Primary Command Function
SCG:	GPIB Secondary Command Group message
pon:	Power On Reset

Bit	Mnemonic	Description

TAG: GPIB Talk Address Group message
LAG: GPIB Listen Address Group message
read ISR1: Read the Interrupt Status Register 1
read CPTR: Read of the Command Pass Through Register

UDPCF is set by:

[UCG + ACG & (TADS + LADS)] & undefined & ACDS & CPT ENAB

UDPCF is cleared by:

[(UCG + ACG) & defined + TAG + LAG] & ACDS + -(CPT ENAB) + pon

6r APT Address Pass Through
6w APT IE Address Pass Through Interrupt Enable

The APT bit indicates that a secondary GPIB address has been received and is available in the CPTR for inspection.

Note: The application program must check this bit when using NAT4882 address mode 3.

When APT is set, the Data Accepted (DAC) message is held and the GPIB Handshake stops until either the Valid or Non-Valid auxiliary command is issued.

APT is set by:

ADM1 & ADM0 & (TPAS + LPAS) & SCG & ACDS

APT is cleared by:

pon + (read ISR1) & ~SISB + (Valid + Non-Valid) & SISB

Notes

ADM1: Address Mode Register bit 1, ADMR[1]w
ADM0: Address Mode Register bit 0, ADMR[0]w
SISB: Static Interrupt Status bits, AUXRI[0]w
Valid: Valid Auxiliary Command issued
Non-Valid: Non-Valid Auxiliary Command issued
TPAS: GPIB Talker Primary Addressed State
LPAS: GPIB Listener Primary Addressed State
SCG: GPIB Secondary Command Group
ACDS: GPIB Accept Data State
pon: Power On Reset
read ISR1: Read the Interrupt Status Register 1

Bit	Mnemonic	Description
5r	DET	Device Execute Trigger bit
5w	DET IE	Device Execute Trigger Interrupt Enable bit

The DET bit indicates that the GPIB Group Execute Trigger (GET) command was received while the NAT4882 was a GPIB Listener–that is, while the NAT4882 was in DTAS.

DET is set by:

DTAS = GET & LADS & ACDS

DET is cleared by:

pon + (read ISR1) & ~SISB + clearDET

Notes

DTAS:	GPIB Device Trigger Active State
pon:	Power On Reset
read ISR1:	Read the Interrupt Status Register 1
SISB:	Static Interrupt Status Bits, AUXRI[0]w
clearDET:	clearDET Auxiliary Command issued

4r	END RX	End Received bit
4w	END IE	End Received Interrupt Enable bit

The END RX bit is set when the NAT4882 is a Listener and the GPIB uniline message, END, is received with a data byte from the GPIB Talker, when the data byte in the DIR matches the contents of the End Of String Register (EOSR) and REOS is set, or when the data byte in the DIR matches the ASCII newline character (hex 0A) and NLEE is set. The END bit is always set before the DI bit when a byte that sets END is received.

END RX is set by:

LACS & (EOI + EOS & REOS + NL & NLEE) & ACDS

END RX is cleared by:

pon + (read ISR1) & ~SISB + clearEND

Notes

LACS:	GPIB Listener Active State
EOI:	GPIB End Or Identify Signal
EOS:	GPIB End Of String message
NL:	ASCII 'Newline' message (hex 0A)
ACDS:	GPIB Accept Data State

Bit	Mnemonic	Description

pon:	Power On Reset
read ISR1:	Read the Interrupt Status Register 1
REOS:	END on EOS Received bit, AUXRA[2]w
SISB:	Static Interrupt Status Bits, AUXRI[0]w
NLEE:	New Line End Enable, IMR0[5]w
clearEND:	clearEND Auxiliary Command issued

3r DEC Device Clear bit
3w DEC IE Device Clear Interrupt Enable bit

The DEC bit indicates that either the NAT4882 received the GPIB Device Clear (DCL) command or that the NAT4882 received the GPIB Selected Device Clear (SDC) command while it was a GPIB Listener. The NAT4882 is in DCAS.

DEC is set by:

DCAS = (SDC & LADS + DCL) & ACDS

DEC is cleared by:

pon + (read ISR1) & ~SISB + clearDEC

Notes

DCAS:	GPIB Device Clear Active State
pon:	Power On Reset
read ISR1:	Read the Interrupt Status Register 1
SISB:	Static Interrupt Status Bits, AUXRI[0]w
clearDEC:	clearDEC Auxiliary Command issued

2r ERR Error bit
2w ERR IE Error Interrupt Enable bit

The definition of the ERR bit depends on the status of the NTNL bit. If NTNL=0, the ERR bit indicates that the contents of the CDOR have been lost. ERR is set when data is sent over the GPIB without a specified Listener, when a byte is written to the CDOR during SIDS, or when a transition from SDYS to SIDS has occurred. If NTNL=1, the ERR bit indicates that the Source Handshake is attempting to send data or commands across the bus and finds that there are no Listeners–that is, that NDAC and NRFD are unasserted. Data is not lost, because the Source Handshake will attempt to source the data or command as soon as a Listener appears.

Bit	Mnemonic	Description

ERR is set by:

~NTNL & TACS & SDYS & DAC & RFD
+ ~NTNL & SIDS & (write CDOR)
+ ~NTNL & (SDYS to SIDS)
+ NTNL & SDYS & EXTDAC & RFD

ERR is cleared by:

pon + (read ISR1) & ~SISB + clearERR

Notes

TACS:	GPIB Talker Active State
SDYS:	GPIB Source Delay State
DAC:	GPIB Data Accepted message
EXTDAC:	GPIB Data Accepted message asserted by a device other than the NAT4882 Acceptor Handshake
RFD:	GPIB Ready For Data message
SIDS:	GPIB Source Idle State
write CDOR:	Writing to the Command/Data Out Register
SDYS to SIDS:	Transition from GPIB Source Delay State to Source Idle State
pon:	Power On Reset
SISB:	Static Interrupt Status Bits, AUXRI[0]w
NTNL:	No Talking when No Listener bit, AUXRG[3]w
clearERR:	clearERR Auxiliary Command issued
read ISR1:	Read the Interrupt Status Register 1

1r	DO	Data Out bit
1w	DO IE	Data Out Interrupt Enable bit

The DO bit indicates that the NAT4882, as GPIB Talker, is ready to accept another data byte from the CPU for transmission to the GPIB. The DO bit is cleared when a byte is written to the CDOR or when the NAT4882 ceases to be the Active Talker.

DO is set by:

(TACS & SGNS & ~nba)

DO is cleared by:

~(TACS) + ~(SGNS) + nba + (read ISR1) & ~SISB

Notes

TACS:	GPIB Talker Active State
SGNS:	GPIB Source Generate State
nba:	New Byte Available Local Message
SISB:	Static Interrupt Status Bits, AUXRI[0]w
read ISR1:	Read the Interrupt Status Register 1

Bit	Mnemonic	Description
0r	DI	Data In bit
0w	DI IE	Data In Interrupt Enable bit

The DI bit indicates that the NAT4882, as a GPIB Listener, has accepted a data byte from the GPIB Talker.

DI is set by:

LACS & ACDS & ~(continuous mode)

DI is cleared by:

pon + (read ISR1) & ~SISB + (Finish Handshake) & (Holdoff mode) + (read DIR)

Notes

LACS:	GPIB Listener Active State
ACDS:	GPIB Accept Data State
continuous mode:	Listen in Continuous Mode auxiliary command in effect
SISB:	Static Interrupt Status Bits, AUXRI[0]w
pon:	Power On Reset
read ISR1:	Read the Interrupt Status Register 1
finish Handshake:	Finish Handshake auxiliary command issued
Holdoff mode:	RFD Holdoff state
read DIR:	Read Data In Register

Interrupt Status Register 2 (ISR2)

Access: location 2 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Attributes: Read-Only
Bits clear when read if SISB=0

Interrupt Mask Register 2 (IMR2)

Access: location 2 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Attributes: Write-Only

7	6	5	4	3	2	1	0	R
INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC	
0	SRQI IE	DMAO	DMAI	CO IE	LOKC IE	REMC IE	ADSC IE	
								W

The Interrupt Status Register 2 (ISR2) consists of six Interrupt Status bits and two Internal Status bits. The Interrupt Mask Register 2 (IMR2) consists of five Interrupt Enable bits and two Internal Control bits. If the Interrupt Enable and GLINT bits (in ISR0) are true when the corresponding status condition or event occurs, an interrupt request is generated. Bits in ISR2 are set and cleared regardless of the status of the bits in IMR2. If the NAT4882 must set or clear a bit or bits in ISR2 while ISR2 is being read, the NAT4882 holds off setting or clearing the bit or bits until the read is finished. All bits in IMR2 are cleared on a hardware reset.

Bit **Mnemonic** **Description**

7r INT Interrupt bit

This bit is the logical OR of all the Enabled Interrupt Status bits in ISR0, ISR1 and ISR2, each one ANDed with its Interrupt Enable bit.

INT is set by:

Global IE & [(CPT & CPT IE) + (APT & APT IE) + (DET & DET IE) + (ERR & ERR IE) + (END RX & END IE) + (DEC & DEC IE) + (DO & DO IE) + (DI & DI IE) + (SRQI & SRQI IE) + (REMC & REMC IE) + (CO & CO IE) + (LOKC & LOKC IE) + (ADSC & ADSC IE) + (STBO IE & STBO) + (IFCI IE & IFCI) + (ATNI IE & ATNI) + (TO IE & TO) + (SYNC IE & SYNC)]

Bit	Mnemonic	Description
		Notes
		Global IE: Enable Interrupt on Command Pass Through bit CPT: Command Pass Through bit CPT IE: Enable Interrupt on Command Pass Through bit APT: Address Pass Through bit APT IE: Enable Interrupt on Address Pass Through bit DET: Device Execute Trigger bit DET IE: Enable Interrupt on Device Execute Trigger bit ERR: Error bit ERR IE: Enable Interrupt on Error bit END RX: End Received bit END IE: Enable Interrupt on End Received bit DEC: Device Clear bit DEC IE: Enable Interrupt on Device Clear bit DO: Data Out bit DO IE: Enable Interrupt on Data Out bit DI: Data In bit DI IE: Enable Interrupt on Data In bit SRQI: Service Request Input bit SRQI IE: Enable Interrupt on Service Request Input bit REMC: Remote Change bit REMC IE: Enable Interrupt on Remote Change bit CO: Command Output bit CO IE: Enable Interrupt on Command Output bit LOKC: Lockout Change bit LOKC IE: Enable Interrupt on Lockout Change bit ADSC: Address Status Change bit ADSC IE: Enable Interrupt on Address Status Change bit STBO: Status Byte Out bit STBO IE: Enable Interrupt on Status Byte Out bit IFCI: IFC Assertion bit IFCI IE: Enable Interrupt on IFC Assertion bit ATNI: ATN Assertion bit ATNI IE: Enable Interrupt ATN Assertion bit TO: Time Out bit TO IE: Enable Interrupt on Time Out bit SYNC: Synchronize bit SYNC IE: Enable Interrupt on Synchronize bit
7w	0	Unused bit Write zero to this bit.
6r 6w	SRQI SRQI IE	Service Request Input bit Service Request Input Interrupt Enable bit The SRQI bit indicates that a GPIB Service Request (SRQ) message has been received while the NAT4882 was Controller-In-Charge (CIC). The term ~(RQS & DAV) ensures

Bit	Mnemonic	Description

that if SRQ remains asserted while serial polling a device in APRS, the SRQI bit will be set again, indicating that another device is also requesting service. In version 2 of the NAT4882 (NAT4882B), if the clear SRQI auxiliary command is issued and SRQ is still asserted, the SRQI bit clears for one clock pulse and is set again. In version 1 (NAT4882A), the command clears the SRQI bit, and it is not reset. Refer to the Key Status Register (KSR) to determine the version number of your NAT4882 chip.

SRQI is set when:

(CIC & SRQ & -(RQS & DAV)) becomes true
where RQS = DIO7 & ~ATN & SPMS

SRQI is cleared by:

pon + (read ISR2) & ~SISB + clearSRQI

Notes

CIC:	GPIB Controller-In-Charge
SRQ:	GPIB Service Request message
RQS:	GPIB Request Service message
SISB:	Static Interrupt Status Bits, AUXRI[0]w
clearSRQI:	clearSRQI Auxiliary Command Issued
DAV:	GPIB Data Valid message
pon:	Power On Reset
read ISR2:	Read Interrupt Status Register 2

5r LOK Lockout bit

LOK is used, along with the REM bit, to indicate the status of the NAT4882 GPIB Remote/Local (RL) function. If set, the LOK bit indicates that the NAT4882 is in Local With Lockout State (LWLS) or Remote With Lockout State (RWLS). LOK is a Non-Interrupt bit.

5w DMAO DMA Out Enable bit

Setting DMAO enables the NAT4882 to assert the DRQ line when the set DO condition occurs. Once asserted the NAT4882 will keep the DRQ pin asserted until the set DO condition is false.

4r REM Remote bit

This bit is set when the NAT4882 GPIB RL function is in either Remote State (REMS) or Remote With Lockout State (RWLS). The NAT4882 RL function transfers to one of these states when the System Controller has asserted the Remote Enable line (REN), and the CIC addresses the NAT4882 as a Listener.

Bit	Mnemonic	Description
4w	DMAI	DMA Input Enable bit

Setting DMAI enables the NAT4882 to assert the DRQ line when the set DI condition occurs. Once asserted, the NAT4882 keeps the DRQ pin asserted until any of the clear DI conditions (except read ISR1) occurs.

3r	CO	Command Out bit
3w	CO IE	Command Out Interrupt Enable bit

CO = 1 indicates that the CDOR is empty and that another command can be written to it for transmission over the GPIB without overwriting a previous command.

CO is set by:

(CACS & SGNS & ~nba)

CO is cleared by:

(read ISR2) & ~SISB + ~CACS + ~SGNS + cdba

Notes

CACS:	GPIB Controller Active State
SGNS:	GPIB Source Generate State
SISB:	Static Interrupt Status Bits, AUXRI[0]w
nba:	New Byte Available local message
read ISR2:	Read the Interrupt Status Register 2

2r	LOKC	Lockout Change bit
2w	LOKC IE	Lockout Change Interrupt Enable bit

LOKC is set if there is a change in the LOK bit, ISR2[5]r, (LOCS<–>LWLS or REMS<–>RWLS).

LOKC is set by any change in LOK.

LOKC is cleared by:

pon + (read ISR2) & ~SISB + clearLOKC

Notes

LOK:	ISR2[5]r
pon:	Power On Reset
SISB:	Static Interrupt Status Bits, AUXRI[0]w
clearLOKC:	clearLOKC auxiliary command issued
read ISR2:	Read the Interrupt Status Register 2

Bit	Mnemonic	Description
1r	REMC	Remote Change bit
1w	REMC IE	Remote Change Interrupt Enable bit

REMC is set when there is a change in the REM bit, ISR2[4]r, (LOCS<–>REMS or LWLS<–>RWLS).

REMC is set by any change in REM.

REMC is cleared by:

pon + (read ISR2) & ~SISB + clearREMC

Notes

REM:	ISR2[4]r
pon:	Power On Reset
SISB:	Static Interrupt Status Bits, AUXRI[0]w
clearREMC:	clearREMC auxiliary command issued
read ISR2:	Read the Interrupt Status Register 2

0r	ADSC	Addressed Status Change bit
0w	ADSC IE	Addressed Status Change Interrupt Enable bit

ADSC is set when there is a change in one of the four bits TA, LA, CIC, MJMN of the Address Status Register (ADSR).

ADSC is set by:

[(any change in TA) + (any change in LA) + (any change in CIC) + (any change in MJMN)] & -(lon + ton)

ADSC is cleared by:

pon + (read ISR2) & ~SISB + clearADSC + lon + ton

Notes

TA:	Talker Active bit, ADSR[1]r
LA:	Listener Active bit, ADSR[2]r
CIC:	Controller-In-Charge bit, ADSR[7]r
MJMN:	Major/Minor bit, ADSR[0]r
lon:	Listen Only bit, ADMR[6]w
ton:	Talk Only bit, ADMR[7]w
pon:	Power On Reset
SISB:	Static Interrupt Status Bits, AUXRI[0]w
clearADSC:	clearADSC auxiliary command issued
read ISR2:	Read the Interrupt Status Register 2
ADSR:	Address Status Register
ADMR:	Address Mode Register

Serial Poll Status Register (SPSR)

Access: location 3 (except immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Read-Only

Serial Poll Mode Register (SPMR)

Access: location 3 (except immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Write-Only

7	6	5	4	3	2	1	0	R
S8	PEND	S6	S5	S4	S3	S2	S1	
S8	rsv/RQS	S6	S5	S4	S3	S2	S1	
								W

Bit	Mnemonic	Description
7r	S8	Serial Poll Status bit 8
7w, 5-0r, 5-0w	S[6-1]	Serial Poll Status bits 6 through 1 Cleared by issuing the Chip Reset auxiliary command. These bits send device- or system-dependent status information over the GPIB when the NAT4882 is serial polled. When STBO IE = 0 and the NAT4882, as the GPIB Talker, receives the GPIB multiline Serial Poll Enable (SPE) command message, the NAT4882 transmits a byte of status information, SPMR[7- 0], to the Controller-In-Charge after the Controller Goes to Standby and becomes an Active Listener. In this mode, the SPMR bits S[8,6-1] are double-buffered and if the register is written to while the device is addressed during a serial poll (serial poll active state, SPAS), the value written is saved. These bits are updated when SPAS is terminated. When STBO IE = 1, the device STB should be written to these bits in response to an STBO interrupt and the value written will be sourced as the STB during that particular serial poll.

Bit	Mnemonic	Description
6r	PEND	Pending bit PEND is set when rsv=1. PEND is cleared when the NAT4882 is in Negative Poll Response State [NPRS] and the local Request Service message [rsv] is false. Reading the PEND status bit can confirm that a request was accepted and that the Status Byte (STB) was transmitted (PEND=0).
6w	rsv/RQS	Request Service/ RQS bit When STBO IE = 0, bit 6 is the rsv bit. The rsv bit generates the GPIB local rsv message. When rsv is set and the GPIB Active Controller is not serial polling the NAT4882, the NAT4882 enters the Service Request State (SRQS) and asserts the GPIB SRQ signal. When the Active Controller reads the STB during the poll, the NAT4882 clears rsv at the Affirmative Poll Response State (APRS). The rsv bit is also cleared by pon, by issuing the Chip Reset auxiliary command, or by writing a zero (0) to it. When STBO IE = 1, bit 6 is the RQS bit. The RQS bit should be written in response to an STBO interrupt along with the STB. The value written to the RQS bit is sourced on GPIB DIO7 (RQS) along with the STB during that particular serial poll.

Key Status Register (KSR)

Access: location 3 (immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Read-Only

7	6	5	4	3	2	1	0 R
V3	V2	V1	V0	KEYDQ	MODE	0	0

The Key Status Register contains a value unique to each version of the NAT4882 and can be used to distinguish itself from a standard µPD7210. It is also used to read data from an electronic key, if attached.

Bit	Mnemonic	Description
7-4r	V[3-0]	The version number of the NAT4882. NAT4882A reads 0001. NAT4882B reads 0010.
3r	KEYDQ	Key Data bit KEYDQ returns the logic value of the KEYDQ pin. If you are using an electronic key, the KEYDATEN bit in the KEY Register must be cleared to read data from the key. Key data bits are read from the key memory on the rising edge of KEYCLK.
2r	MODE	MODE bit MODE returns the logic value of the MODE pin. The MODE pin determines which mode the NAT4882 functions in following a hardware reset. If MODE = 0, the NAT4882 functions in the 9914 mode following a hardware reset. If MODE = 1, the NAT4882 functions in the 7210 mode following a hardware reset.
1-0r	0	Reserved. These bits always read back zero.

Key Control Register (KCR)

Access: location 3 (immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Write-Only

7	6	5	4	3	2	1	0
0	SWAP	MSTD	NO T1	KEY CLK	KEY DATEN	KEY DATA	KEY RST*
							W

The Key Register is a write-only register that can be used to control a hardware key.

Bit	Mnemonic	Description
7w	0	Unused bit Write zero to this bit.
6w	SWAP	Swap bit The SWAP* pin of the NAT4882 is sampled during a hard reset to set the power on value of the SWAP bit. The bit is set if SWAP* is low when RESET* unasserts. The SWAP bit rearranges the order of the 9914 mode registers for use by the Turbo488 ASIC.
5w	MSTD	Maximum Speed T1 Delay bit When set, this bit reduces the T1 delay to 200 nsec (four clocks at 20 MHz). This setting provides the maximum Source Handshake speed for interfaces that have the necessary 150 nsec of setup on the D7-0 bus (for example, the Turbo488 ASIC) before unasserting WR*.
4w	NO T1	No T1 Delay bit When set, the NAT4882 has a very short T1 delay, between 1 and 2 clock periods. It should be used for test purposes only.
3w	KEYCLK	Key Clock bit This bit controls the KEYCLK output pin. Setting KEYCLK drives the KEYCLK pin low. Clearing KEYCLK drives the KEYCLK pin high. This bit must be toggled to read or write data to an electronic key using the KEYDATA bit. If KEYDATEN is set to one, the data in KEYDATA is written to the key on the falling edge of KEYCLK . If KEYDATEN is cleared, data is read from the key and placed at the KEYDQ bit in the KSR on the rising edge of KEYCLK.

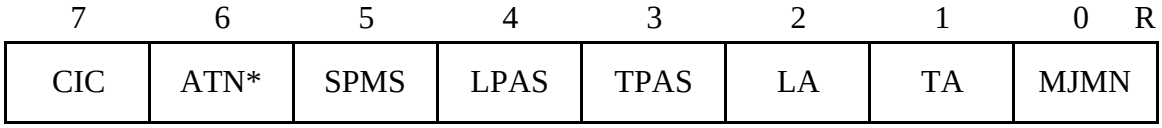
Bit	Mnemonic	Description
		Note: The active edges of KEYCLK contradict the DS1204 data sheet because the KEYCLK bit is inverted before being presented to the hardware keys.
2w	KEYDATEN	Key Data Enable bit This bit must be set to one to write data into the key. If it is cleared, data can be read from the key.
1w	KEYDATA	Key Data bit This bit holds the data to be written into the key memory. The data bit is written into the key memory on the rising edge of the KEYCLK signal.
0w	KEYRST*	Key Reset bit This bit must be set to one to initiate a key data transfer, and must remain set to one throughout the entire data transfer. Clearing this bit terminates a key data transfer.

Address Status Register (ADSR)

Access: location 4 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Attributes: Read-Only



7	6	5	4	3	2	1	0 R
CIC	ATN*	SPMS	LPAS	TPAS	LA	TA	MJMN

The Address Status Register (ADSR) contains information that can be used to monitor the TLC GPIB address status.

Bit	Mnemonic	Description
7r	CIC	Controller-In-Charge bit CIC = ~(CIDS + CADS) CIC indicates that the NAT4882 GPIB Controller function is in an active or standby state, with ATN* on or off, respectively. The Controller function is in an idle state (CIDS) or addressed state (CADS) if CIC = 0.
6r	ATN*	Attention* bit ATN* is a Status bit that indicates the current level of the GPIB ATN* signal. If ATN* = 0, the GPIB ATN* signal is asserted.
5r	SPMS	Serial Poll Mode State bit If SPMS = 1, the NAT4882 GPIB Talker (T) or Talker Extended (TE) function is enabled to participate in a serial poll. SPMS is set when the GPIB Active Controller has issued the GPIB Serial Poll Enable (SPE) command message. SPMS is cleared when the GPIB SPD (Serial Poll Disable) command is received, either by pon or by the assertion of the GPIB IFC signal.
4r	LPAS	Listener Primary Addressed State bit The LPAS bit is used when the NAT4882 is configured for extended GPIB addressing and, when set, indicates that the NAT4882 has received its primary listen address. In mode 3 addressing (see *Address Mode Register* in this chapter), LPAS = 1 indicates that the secondary address received on the next GPIB command may represent the NAT4882 extended (secondary) GPIB listen address. LPAS is cleared by a primary command that is not the TLCs primary listen address, by pon, or by the Chip Reset auxiliary command.

Bit	Mnemonic	Description
3r	TPAS	Talker Primary Addressed State bit TPAS is used when the NAT4882 is configured for extended GPIB addressing, and, when set, indicates that the NAT4882 has received its primary GPIB talk address. In extended mode addressing (mode 3 addressing), TPAS = 1 indicates that the secondary address being received as the next GPIB command may represent the NAT4882 extended (secondary) GPIB talk address. TPAS is cleared by a primary command that is not the TLCs primary talk address, by pon, or by the Chip Reset auxiliary command.
2r	LA	Listener Active bit LA is set when the NAT4882 has been addressed or programmed as a GPIB Listener–that is, the NAT4882 is in the Listener Active State (LACS) or the Listener Addressed State (LADS). The NAT4882 can be addressed to listen either by sending its own listen or extended listen address while it is CIC or by receiving its listen address from another CIC. It can also be programmed to listen using the Listen Only (lon) bit in the Address Mode Register (ADMR). If the NAT4882 is addressed to listen, it is automatically unaddressed to talk. LA is cleared by the UNL GPIB command, by the assertion of the GPIB IFC signal, by pon, by issuing the Chip Reset auxiliary command, by issuing the local unlisten auxiliary command (lun) while in CACS, or by issuing the unlisten auxiliary command (lul).
1r	TA	Talker Active bit TA is set when the NAT4882 has been addressed or programmed as the GPIB Talker–that is, when the NAT4882 is in the Talker Active State (TACS), the Talker Addressed State (TADS), or the Serial Poll Active State (SPAS). The NAT4882 can be addressed to talk either by sending its own talk or extended talk address while it is CIC or by receiving its talk address from another CIC. It can also be programmed to talk using the Talk Only (ton) bit in the ADMR. If the NAT4882 is addressed to talk, it is automatically unaddressed to listen. TA is cleared upon receiving an Other Talk Address (OTA), the assertion of the GPIB IFC signal, by pon, by issuing the Chip Reset auxiliary command, or by issuing the untalk auxiliary command (lut).

Bit	Mnemonic	Description
0r	MJMN	Major-Minor bit

The MJMN bit indicates whether the information in the other ADSR bits applies to the NAT4882 major or minor Talker and Listener functions. MJMN is set to one when the NAT4882 GPIB minor talk address or minor listen address is received. MJMN is cleared on receipt of the NAT4882 major talk or major listen address.

Note: Only one Talker or Listener can be active at any one time; thus, the MJMN bit indicates which, if either, of the NAT4882 Talker and Listener functions is addressed or active.

MJMN is always zero unless a dual primary addressing mode (mode 1 or mode 3) is enabled (see *Address Mode Register* in this chapter). The MJMN bit is cleared by pon or by issuing the Chip Reset auxiliary command.

Address Mode Register (ADMR)

Access: location 4 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Attributes: Write-Only

7	6	5	4	3	2	1	0
ton	lon	TRM1	TRM0	0	0	ADM1	ADM0
							W

Bit	Mnemonic	Description
7w	ton	Talk-Only bit Setting ton programs the NAT4882 to become a GPIB Talker. If ton is set, the lon, ADM1, and ADM0 bits should be cleared. Use this method in place of the addressing method when the NAT4882 will be only a Talker. **Note:** Clearing ton does not, by itself, take the NAT4882 out of GPIB Talker Active State (TACS). You must also execute the Chip Reset or Immediate Execute pon auxiliary commands, receive another Talk Address, send the local untalk auxiliary command, or detect the assertion of the GPIB IFC signal to get the NAT4882 to exit TACS.
6w	lon	Listen-Only bit Setting lon programs the NAT4882 to become a GPIB Listener. If lon is set, ton, ADM1, and ADM0 should be cleared. **Note:** Clearing lon does not, by itself, take the NAT4882 out of GPIB Listener Active State (LACS). You must also execute the Chip Reset or Immediate Execute pon auxiliary commands, receive an Unlisten command, send the local unlisten auxiliary command while in CACS, send the unlisten auxiliary command, or detect the assertion of the GPIB IFC signal to get the NAT4882 to exit LACS.

Bit	Mnemonic	Description

5-4w TRM[1-0] Transmit/Receive Mode bit

TRM1 and TRM0 control the function of the NAT4882 T/R2* and T/R3 output pins in the following manner:

TRM1	TRM0	T/R2*	T/R3
0	0	EOIOE*	TRIG
0	1	CIC*	TRIG
1	0	CIC*	EOI OE
1	1	CIC*	PE

Key

EOIOE* = Not GPIB EOI signal output enable ~(TACS + SPAS + CIC & ~(CSBS + CSHS))
CIC* = Not Controller-In-Charge (CIDS + CADS)
TRIG = Trigger (pulses when DTAS = 1 or a trigger auxiliary command is issued)
PE = Pull-up Enable (CIC + -(PPAS))

3-2w 0 Reserved bits

Write zeros to these bits.

1-0w ADM[1-0] Address Mode bits 1 through 0

These bits specify the addressing mode that is in effect–that is, the manner in which the information in ADR0 and ADR1 is interpreted (see *Address Register 0* and *Address Register 1* later in this chapter). If both bits are zero, the NAT4882 does not respond to GPIB address commands; instead, the ton and lon bits are used to program the Talker and Listener functions, respectively. The ton and lon bits must be cleared if mode 1, 2, or 3 addressing is selected, and the ADM[1-0] bits must be cleared if either of the bits ton or lon are set.

Mode	ADM1	ADM0	Title
0	0	0	Talk-Only (ton)/Listen-Only (lon)
1	0	1	Normal dual addressing
2	1	0	Extended single addressing
3	1	1	Extended dual addressing

In mode 1, ADR0 and ADR1 contain the major and minor addresses, respectively, for dual primary GPIB address applications–that is, the NAT4882 responds to two GPIB addresses, a major one and a minor one. The MJMN bit in the ADSR indicates which address was received. In applications that

Bit	Mnemonic	Description
		only require that the NAT4882 respond to one address, the major Talker and Listener function is used and the minor Talker and Listener functions should be disabled. The minor Talker and Listener functions can be disabled by setting the Disable Talker (DT) and Disable Listener (DL) bits in ADR1 (see *ADR* and *ADR1* later in this chapter). In mode 2 (ADM1 = 1, ADM0 = 0), the NAT4882 recognizes primary and secondary GPIB address bytes. Both GPIB address bytes must be received to enable the NAT4882 to talk or listen. Thus, mode 2 addressing implements the Extended Talker and Extended Listener functions as defined in IEEE 488, without requiring computer program intervention. In mode 2, ADR0 and ADR1 contain the NAT4882 primary and secondary GPIB addresses, respectively. In mode 3 (ADM1 = 1 and ADM0 = 1), the NAT4882 handles addressing just as it does in mode 1, except that each major or minor GPIB primary address must be followed by a secondary address. All secondary GPIB addresses must be verified by computer program when mode 3 is used. When the NAT4882 is in Talker Primary Addressed State (TPAS) or Listener Primary Addressed State (LPAS) and a secondary address byte is received on the GPIB DIO lines, the APT bit of ISR2 is set and the secondary GPIB address may be inspected in the CPTR. The NAT4882 Acceptor Handshake is held up in the Accept Data State (ACDS) until the Valid or Non-Valid auxiliary command is written to the AUXMR, signaling a valid or invalid secondary address, respectively, to the NAT4882. ADM0 and ADM1 should both be cleared when either of the two programmable bits ton or lon is set.

Command Pass Through Register (CPTR)

Access: location 5 (except immediately after the page-in auxiliary command or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Read-Only

7	6	5	4	3	2	1	0 R
CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

Bit **Mnemonic** **Description**

7-0r CPT[7-0] Command Pass Through bits 7 through 0

These bits transfer undefined multiline GPIB command messages from the GPIB DIO lines to the computer. When the CPT feature is enabled (CPT ENAB = 1, AUXRB[0]w), any GPIB Primary Command Group (PCG) message not decoded by the NAT4882 is treated as an undefined command. Table 2-2 lists the multiline GPIB commands recognized by the µPD7210 chip. All GPIB Secondary Command Group (SCG) messages following an undefined GPIB PCG message are also treated as undefined. In such a case, when an undefined GPIB message is encountered, it is held in the CPTR and the NAT4882 Acceptor Handshake function is held off in ACDS until a Valid or Not Valid auxiliary command is written to the AUXMR. The CPTR is also used to inspect secondary addresses when addressing mode 3 is used. The NAT4882 Acceptor Handshake function is held off in ACDS until the Valid or Non-Valid auxiliary command is written to the AUXMR. Recognized commands that the NAT4882 has been programmed to Holdoff on via AUXRE[3-0] or AUXRF[3-0] may be inspected in the CPTR.

Table 2-2. Multiline GPIB Commands Recognized by the GPIB Chip in µPD7210 Mode

Hex Number	Message	Description
01	GTL	Go To Local
04	SDC	Selected Device Clear
05	PPC*	Parallel Poll Configure
08	GET	Group Execute Trigger

(continues)

Bit Mnemonic Description

Table 2-2. Multiline GPIB Commands Recognized by the GPIB Chip in µPD7210 Mode (continued)

Hex Number	Message	Description
09	TCT†	Take Control
11	LLO	Local Lockout
14	DCL	Device Clear
15	PPU*	Parallel Poll Unconfigure
18	SPE	Serial Poll Enable
19	SPD	Serial Poll Disable
20-3E	MLA	My Listen Address
3F	UNL	Unlisten
40-5E	MTA	My Talk Address
5F	UNT	Untalk
60-6F	MSA, PPE	My Secondary Address or Parallel Poll Enable
70-7F	MSA, PPD	My Secondary Address or Parallel Poll Disable

† TCT is treated as an undefined command if DISTCT is set.

* PPC and PPU are treated as undefined commands if PP2 is set.

The CPTR is read during a NAT4882-initiated Parallel Poll operation to fetch the Parallel Poll response. When using the local rpp1 message, the PPR message is latched into the CPTR when CPPS is set, and is held valid until either CIDS is set or a command byte is sent over the GPIB. When using the local rpp2 message the PPR message is not latched into the CPTR and must be read before rpp2 is cleared.

Source/Acceptor Status Register (SASR)

Access: location 5 (immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Read-Only

7	6	5	4	3	2	1	0 R
cdba	AEHS	ANHS1	ANHS2	ADHS	ACRDY	SH1A	SH1B

The Source/Acceptor Status Register contains status bits that indicate the state of the Source and Acceptor Functions.

Bit	Mnemonic	Description
7r	cdba	Command/Data byte available local message
6r	AEHS	Acceptor End Holdoff State bit
5r	ANHS1	Acceptor Not Ready Holdoff State bit
4r	ANHS2	Acceptor Not Ready Holdoff Immediately State bit
3r	ADHS	Acceptor Data Holdoff State bit
2r	ACRDY	Acceptor Ready State bit

This bit can be used to determine the state of the Acceptor Handshake. By monitoring the LA and ATN bits in ADSR, the DAV bit in the BSR, and the ADHS and ACRDY bits, you can determine the state of the Acceptor Handshake function as described below:

```
AIDS  = ~ATN + ~LA
ANRS  = ~AIDS & ~ACRDY & ~DAV
ACRS  = ~AIDS &  ACRDY & ~DAV
ACDS  = ~AIDS &  ACRDY &  DAV
          + ~AIDS & ~ACRDY &  DAV &ATN & ADHS
AWNS  = ~AIDS & ~ACRDY &  DAV & ~(ATN & ADHS)
```

Bit	Mnemonic	Description
1-0r	SH1A	Source Handshake State bits
	SH1B	These bits can be used to determine the state of the source handshake. By monitoring the TA, SPMS, and ATN bits in the ADSR, and the SH1A and SH1B bits, you can determine the state of the source handshake function as described below: SIDS = ~(TACS & ~ATN + CIC & ATN) SGNS = ~SIDS & ~SH1A & ~SH1B SDYS = ~SIDS & SH1A STRS = ~SIDS & ~SH1A & SH1B

Auxiliary Mode Register (AUXMR)

Access: location 5 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Attributes: Write-Only,
Permits Access to Hidden Registers

7	6	5	4	3	2	1	0
CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

W

The AUXMR is used to issue auxiliary commands. It is also used to write the eight hidden registers:

- Parallel Poll Register (PPR)
- Auxiliary Register A (AUXRA)
- Auxiliary Register B (AUXRB)
- Auxiliary Register E (AUXRE)
- Auxiliary Register F (AUXRF)
- Auxiliary Register G (AUXRG)
- Auxiliary Register I (AUXRI)
- Auxiliary Register J (AUXRJ)

Table 2-4 shows the implementation of the control and command codes.

Note: Commands should be issued at intervals of at least 200 nsec (four clock cycles at 20 MHz).

Bit	**Mnemonic**	**Description**
7-5w	CNT[2-0]	Control Code bits 2 through 0 These bits specify the control code–that is, the manner in which the information in bits COM[4-0] is to be used. If CNT[2-0] are equal to 000 or 010, the special function selected by COM[4-0] is executed. Otherwise, the hidden register selected by CNT[2-0] and COM[4] is loaded with the data from COM[4-0].
4-0w	COM[4-0]	Command Code bits 4 through 0 These bits specify the command code of the special function if the control code is 000 or 010. Table 2-3 summarizes the implemented special functions. The special functions can either enable/disable a feature or initiate an action within the NAT4882.

Bit Mnemonic Description

Table 2-4 explains the details of each special function. If the control code is not 000 or 010, these bits are written to one of the hidden registers, as indicated by the control code in CNT[2-0].

Table 2-3. Auxiliary Command Summary

Control (CNT2-0) 2 1 0	Function Code* (COM4-COM0) 4 3 2 1 0	Hex Code**	Auxiliary Command
0 0 0	0 0 0 0 0	00	Immediate Execute power-on (pon)
0 0 0	0 0 0 1 0	02	Chip Reset (chip reset)
0 0 0	0 0 0 1 1	03	Finish Handshake (rhdf)
0 0 0	0 0 1 0 0	04	Trigger (trig)
0 0 0 0 0 0	0 0 1 0 1 0 1 1 0 1	05 OD	clear or pulse Return to Local set Return to Local (rtl)
0 0 0	0 0 1 1 0	06	Send EOI (seoi)
0 0 0	0 0 1 1 1	07	Non-Valid Secondary Command or Address (non valid)
0 0 0	0 1 1 1 1	0F	Valid Secondary Command or Address (valid)
0 0 0	0 1 0 0 0	08†	Request Control Command (rqc)
0 0 0 0 0 0	0 0 0 0 1 0 1 0 0 1	01 09	Clear Parallel Poll Flag (~ist) Set Parallel Poll Flag (ist)
0 0 0	0 1 0 1 0	0A†	Release Control Command (rlc)
0 0 0	0 1 0 1 1	0B†	Untalk Command (lut)
0 0 0	0 1 1 0 0	0C†	Unlisten Command (lul)
0 0 0	0 1 1 1 0	0E†	New Byte Available False (nbaf)
0 0 0	1 0 0 0 0	10	Go To Standby (gts)
0 0 0 0 0 0 0 0 0	1 0 0 0 1 1 0 0 1 0 1 1 0 1 0	11 12 1A	Take Control Asynchronously (tca) Take Control Synchronously (tcs) Take Control Synchronously on End (tcse)
0 0 0 0 0 0 0 0 0	1 0 0 1 1 1 1 0 1 1 1 1 1 0 0	13 1B 1C	Listen (ltn) Listen in Continuous Mode (ltn and cont) Local Unlisten (lun)

(continues)

Table 2-3. Auxiliary Command Summary (continued)

Control (CNT2-0) 2 1 0	**Function Code* (COM4-COM0) 4 3 2 1 0**	**Hex Code****	**Auxiliary Command**
0 0 0	1 0 1 0 0	14	Disable System Control (~rsc)
0 0 0	1 0 1 0 1	15†	Switch to 9914A Mode Command
0 0 0 0 0 0	1 1 1 1 0 1 0 1 1 0	1E 16	Set IFC (sic & rsc) Clear IFC (~sic & rsc)
0 0 0 0 0 0	1 1 1 1 1 1 0 1 1 1	1F 17	Set REN (sre & rsc) Clear REN (~sre & rsc)
0 0 0 0 0 0	1 1 0 0 0 1 1 0 0 1	18† 19†	Request rsv True (reqt) Request rsv False (reqf)
0 0 0	1 1 1 0 1	1D	Execute Parallel Poll (rppl)
0 1 0	1 0 0 0 0	50†	Page-In Additional Registers
0 1 0	1 0 0 0 1	51†	Holdoff Handshake Immediately (hldi)
0 1 0 0 1 0	1 0 0 1 0 1 0 0 1 1	52† 53†	Reserved Reserved
0 1 0	1 0 1 0 0	54†	Clear DET (ISR1[5]r) Command
0 1 0	1 0 1 0 1	55†	Clear END (ISR1[4]r) Command
0 1 0	1 0 1 1 0	56†	Clear DEC (ISR1[3]r) Command
0 1 0	1 0 1 1 1	57†	Clear ERR (ISR1[2]r) Command
0 1 0	1 1 0 0 0	58†	Clear SRQI (ISR2[6]r) Command
0 1 0	1 1 0 0 1	59†	Clear LOKC (ISR2[2]r) Command
0 1 0	1 1 0 1 0	5A†	Clear REMC (ISR2[1]r) Command
0 1 0	1 1 0 1 1	5B†	Clear ADSC (ISR2[0]r) Command
0 1 0	1 1 1 0 0	5C†	Clear IFCI (ISR0[3]r) Command
0 1 0	1 1 1 0 1	5D†	Clear ATNI (ISR0[2]r) Command
0 1 0 0 1 0	1 1 1 1 0 1 1 1 1 1	5E† 5F†	Clear SYNC (ISR0[0]r) Command Set SYNC (ISR0[0]r) Command

* CNT[2-0] set to 000 or 010 binary
**Represents all eight bits of the Auxiliary Mode Register
† Denotes an auxiliary command not available in a standard µPD7210

Table 2-4 shows the functions that are executed when the AUXMR Control Code (CNT[2-0]) is loaded with 000 or 010 (binary) and the Command Code (COM[4-0]) is loaded.

Table 2-4. Auxiliary Command Description

Data Pattern (Hex)	Description
00	Immediate Execute Power-On (pon) This command generates the local message, pon, that places the following GPIB interface function into their idle states: AIDS Acceptor Idle State CIDS Controller Idle State LIDS Listener Idle State LOCS Local State LPIS Listener Primary Idle State NPRS Negative Poll Response State PPIS Parallel Poll Idle State PUCS Parallel Poll to Unaddressed to Configure State SIDS Source Idle State SIIS System Control Interface Clear Idle State SPIS Serial Poll Idle State SRIS System Control Remote Enable Idle State TIDS Talker Idle State TPIS Talker Primary Idle State If the command is sent while a pon message is already active (by either an external rest pulse or the Chip Reset auxiliary command, the pon local message becomes false.
02	Chip Reset The Chip Reset command resets the NAT4882. The NAT 4882 is reset via the chip reset to the following conditions: • The local pon message is set and the interface functions are placed in their idle states. • All bits of the SPMR are cleared. • The EOI bit is cleared. • All bits of the AUXRA, AUXRB, AUXRE, AUXRF, AUXRG, AUXRI, and AUXRJ are cleared. • The Parallel Poll Flag and RSC local message are cleared. • The TRM0 bit and the TRM1 bit are cleared. The interface functions are held in their idle states until released by an Immediate Execute pon command. Between these commands, the NAT4882 writeable bits can be programmed to their desired states.
03	Finish Handshake (rhdf) The Finish Handshake command finishes a GPIB Handshake that was stopped because of a Holdoff on RFD condition.

(continues)

Table 2-4. Auxiliary Command Description (continued)

Data Pattern (Hex)	Description
04	Trigger (trig) Trigger command generates a high pulse on the TRIG pin and the T/R3 pin when TRM1 = 0. The Trigger command performs the same function as if the DET (Device Trigger) bit (ISR1[5]r) were set. The DET bit is not set by issuing the Trigger command.
05 0D	Return To Local (rtl) Return to Local (rtl) The two Return to Local commands implement the rtl message as defined by IEEE 488. When COM3 is zero, the message is generated in the form of a pulse. If rtl is already set, this command clears it. When COM3 is set, the rtl command is set and remains set until the rtl command is issued with COM3 cleared or a chip reset auxiliary command is issued.
06	Send EOI (seoi) The Send EOI command causes the GPIB End Or Identify (EOI) line to go true with the next data byte transmitted. The EOI line is cleared upon completion of the Handshake for that byte. The NAT4882 recognizes the Send EOI command only if TACS = 1 (that is, the NAT4882 is the Talker Active State) when NTNL = 0.
07	Non-Valid Secondary Command or Address (non-valid) The Non-Valid command releases the GPIB DAC message held off by the Address Pass Through (APT) bit. The NAT4882 operates as if an Other Secondary Address (OSA) message has been received. This command also releases a DAC holdoff due to the Command Pass Through (CPT) bit being set.
0F	Valid Secondary Command or Address (valid) The Valid command releases the GPIB DAC message held off by APT and allows the NAT4882 to function as if a My Secondary Address (MSA) message had been received. The Valid command release the DAC holdoff (ADHS) when enabled because of CPT conditions or DCAS or DTAS is in holdoff state.
01 09	Clear Parallel Poll Flag (ist) Set Parallel Poll Flag These commands set the Parallel Poll Flag equal to the value of COM3. The value of the Parallel Poll Flag is used as the local message ist when AUXRB[4]w = 0. The value of SRQS is used as the ist when ISS = 1. ist is cleared by a chip or hardware reset.

(continues)

Table 2-4. Auxiliary Command Description (continued)

Data Pattern (Hex)	Description
10	Go To Standby (gts) The Go To Standby command sets the local message gts if the NAT4882 is in Controller Active State (CACS). If gts is true, the ATN line is set to false and the Controller enters CSBS. If the NAT4882 leaves CACS, gts is cleared.
11	Take Control Asynchronously (tca) The Take Control Asynchronously command pulses the local message tca. When this command is issued, the Controller regains control and asserts the ATN line.
12	Take Control Synchronously (tcs) The Take Control Synchronously command sets the local message tcs. The local message tcs should be issued when the NAT4882 is in Controller Standby State (CSBS). The local message tcs is cleared when the NAT4882 enters CAWS, CIDS or CADS.
1A	Take Control Synchronously on END (tsce) The Take Control Synchronously on END command sets the local message tcs when the data block transfer End message (END bit equal to one) is generated at CSBS. The tcs message is cleared when the NAT4882 enters CAWS, CIDS, or CADS.
13	Listen (ltn) The listen command generates the local message ltn in the form of a pulse. It should be issued when the Controller is in CACS.
1B	Listen in Continuous Mode (ltn & cont) The Listen in Continuous Mode command generates the local message ltn in the form of a pulse and places the NAT4882 in continuous mode. In continuous mode, the local message rdy is issued when the Acceptor Not Ready State (ANRS) is initiated unless data block transfer end is detected (END RX bit equals one). When END is detected, the NAT4882 is placed in the RFD Holdoff state, preventing generation of the rdy message. In continuous mode, the DI bit is not set when a data byte is received. The continuous mode caused by the Listen in Continuous Mode command is released when the Listen auxiliary command is issued or the NAT4882 enters the Listener Idle State (LIDS).
1C	Local Unlisten (lun) The Local Unlisten command generates the local message lun in the form of a pulse. It should be issued when the Controller is in CACS.

(continues)

Table 2-4. Auxiliary Command Description (continued)

Data Pattern (Hex)	Description
1D	Execute Parallel Poll (rppl) The Execute Parallel Poll command sets the local message Request Parallel Poll (rpp1). The rpp message is cleared when the NAT4882 enters either Controller Parallel Poll State (CPPS), Controller Idle State (CIDS), or Controller Addressed State (CADS). The transition of the Controller interface function is not guaranteed if the local messages rpp and Go To Standby (gts) are issued simultaneously when the NAT4882 is in Controller Active State (CACS) and Source Generate State (SGNS).
1E 16	Set IFC (sic & rsc) Clear IFC (~sic & rsc) These commands generate the local message Request System Control (rsc) and set the local message Send Interface Clear (sic) equal to the value of COM3. These commands should only be issued if the interface is System Controller. To meet the IEEE 488 requirements, you must not issue the Clear IFC command until IFC has been held true for at least 100 µsec.
1F 17	Set REN (sre & rsc) Clear REN (~sre & rsc) These commands generate the local message Request System Control (rsc) and set the local message Send Remote Enable (sre) to the value in COM3. These commands should only be issued if the interface is System Controller. To meet IEEE 488 requirements, you must not issue the Set REN command until REN has been held false for at least 100 µsec.
14	Disable System Control (~rsc) The Disable System Control command clears the local message rsc.
50†	Page-In Additional Registers The Page-In Additional Registers replaces some of the standard µPD7210 registers with new registers. By using this method, you can implement more read/write registers while staying within the eight byte address space of the µPD7210. Issuing the Page-In Additional Registers auxiliary command replaces the SPSR with the Key Status Register (KSR) and the SPMR with the Key Control Register (KCR) at offset 3, the CPTR with the Source/Acceptor Status Register (SASR) at offset 5, the ACR0/ADR with the ISR0/IMR0 at offset 6, and ADR1/EOSR with the BSR/BCR at offset 7. The new registers remain paged-in until any non-DMA register access is made, after which the standard µPD7210 registers are paged back.

(continues)

Table 2-4. Auxiliary Command Description (continued)

Data Pattern (Hex)	Description
51†	Immediate Holdoff This command forces the acceptor handshake function to immediately perform an RFD Holdoff when Listener. Issuing this command forces a transition into ANHS where the handshake is held off until a release handshake holdoff is issued.
52† 53†	Reserved Reserved These commands are reserved for future use and should not be issued by the control program.
54†	Clear DET This command clears the DET bit (ISR1[5]r). Use this command to clear the DET bit when SISB is set.
55†	Clear END This command clears the END bit (ISR1[4]r). Use this command to clear the END bit when SISB is set.
56†	Clear DEC This command clears the DEC bit (ISR1[3]r). Use this command to clear the DEC bit when SISB is set.
57†	Clear ERR This command clears the ERR bit (ISR1[2]r). Use this command to clear the ER bit when SISB is set.
58†	Clear SRQI This command clears the SRQI bit (ISR2[6]r). Use this command to clear the SRQI bit when SISB is set. If SRQ is still asserted when this command is issued, SRQI clears and then sets after one clock cycle. SRQI continues to be set until SRQ is unasserted and the command is issued. The NAT4882A did not have this feature, and SRQI would remain cleared after issuing the command.
59†	Clear LOKC This command clears the LOKC bit (ISR2[2]r). Use this command to clear the LOKC bit when SISB is set.
5A†	Clear REMC This command clears the REMC bit (ISR2[1]r). Use this command to clear the REMC bit when SISB is set.

(continues)

Table 2-4. Auxiliary Command Description (continued)

Data Pattern (Hex)	Description
5B†	Clear ADSC This command clears the ADSC bit (ISR2[0]r). Use this command to clear the ADCS bit when SISB is set.
5C†	Clear IFCI This command clears the IFCI bit (ISR0[3]r). Use this command to clear the IFCI bit when SISB is set.
5D†	Clear ATNI This command clears the ATNI bit (ISR0[2]r). Use this command to clear the ATNI bit when SISB is set.
5E† 5F†	Clear SYNC Set SYNC These commands are used to control the SYNC function by resetting or starting the function. For more information on the SYNC function, refer to *Synchronization Detection* in Chapter 3.
15†	Switch to 9914A Mode This command puts the interface chip in 9914A compatibility mode.
08†	Request Control (rqc) This command forces the Controller function to enter CADs, where it will wait for ATN to unassert and then enter CACS
0A†	Release Control (rlc) This command forces the Controller function to unassert ATN and enter CIDS.
0B†	Untalk (lut) This command issues the local unt message forcing the Talker function to enter TIDS.
0C†	Unlisten (lul) This command issues the local unl message forcing the Listener function to enter LIDS.
0E†	New Byte Available False (nbaf) If a Talker is interrupted before the byte just stored in the CDOR is sent over the interface, this byte is transmitted as soon as the ATN line returns to the unasserted state when NTNL is set. If, as a result of the interrupt, this byte is no longer required, you can use the nbaf command to suppress transmission.

(continues)

Table 2-4. Auxiliary Command Description (continued)

Data Pattern (Hex)	Description
18† 19†	Request rsv True (reqt) Request rsv False (reqf) These commands are inputs to the IEEE 488.2 Service Request Synchronization circuitry. These commands are used to set and clear the local message rsv. If STBO IE = 0, the commands reqt and reqf are not issued immediately, but are issued on the write of the SPMR following the issuing of the reqt or reqf auxiliary command. If STBO = IE, the commands reqt and reqf are issued immediately.

Hidden Registers

The hidden registers are loaded through the Auxiliary Mode Register (AUXMR). AUXMR[7-5] or AUXMR[7-4] is loaded with the hidden register number, and AUXMR[4-0] or AUXMR[3-0] is loaded with the data to be transferred to the hidden register. The hidden registers cannot be read. Figure 2-2 shows the five hidden registers and illustrates how they are loaded with data from the AUXMR. All hidden registers are cleared by a Chip Reset auxiliary command or a hardware reset.

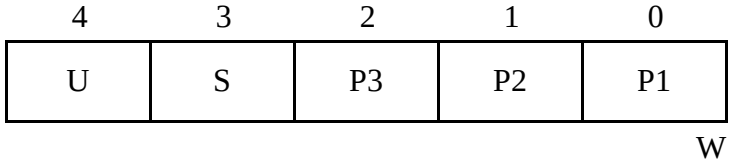
Parallel Poll Register (PPR)

Access: 2-location 5 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Control Code: 011 (Binary, bits 7 - 5)

Attributes: Write-Only
Accessed through AUXMR



Writing to the Parallel Poll Register (PPR) is done via the AUXMR. Writing the binary value 011 into the Control Code (CNT[2-0]) and writing a bit pattern into the command code portion (COM[4-0]) of the AUXMR causes the command code to be written to the PPR. When COM[4-0] is written to the PPR, the bits are named as shown in the PPR. This 5-bit command code determines the manner in which the NAT4882 responds to a Parallel Poll.

When using the remote Parallel Poll Configure (IEEE 488 capability code PP1), do not write to the PPR. The NAT4882 implements remote configuration fully and automatically without software assistance. The hardware recognizes, interprets, and responds to Parallel Poll Configure (PPC), Parallel Poll Unconfigure (PPU), Parallel Poll Enable (PPE), Parallel Poll Disable (PPD), and Identify (IDY) messages. You need only set or clear the individual status (ist) message (using Set/Clear Parallel Poll Flag auxiliary commands) according to pre-established system protocol convention. Writing to the PPR after it is remotely configured corrupts the configuration.

When using the local PPC (capability code PP2), use a valid PPE or PPD message to write to the PPR in advance of the poll. If PP2 (AUXRI[2]w) is clear, the contents written to the PPR will be overwritten if the Controller sends a Parallel Poll command (such as, PPE or PPD while in PACS or PPU), causing the remote configuration to override the local configuration. If PP2 is set, the reception of Parallel Poll commands does not affect the contents of the PPR and the local configuration determines the response during Parallel Polls.

Bit	Mnemonic	Description
4w	U	Unconfigure bit The U bit determines whether or not the NAT4882 participates in a Parallel Poll. If U = 0, the NAT4882 participates in Parallel Polls and responds in the manner defined by PPR[3] through PPR[0] and by ist. If U = 1, the NAT4882 does not participate in a Parallel Poll. The U bit is equivalent to the local message lpe* (Local Poll Enable, active low). When U = 0, S and P[3-1] are the same as the bit of the same name in the PPE message, and the I/O write operation to the PPR is the same as the receipt of the PPE message from the GPIB Controller. When U = 1, S and P[3-1] do not carry any meaning, but they should be cleared.
3w	S	Status Bit Polarity (Sense) bit The S bit indicates the polarity, or sense, of the NAT4882 local ist message. If S = 1, the status is *in phase*, meaning that if, during a Parallel Poll response, S = ist, and U = 0, the NAT4882 responds to the Parallel Poll by driving one of the eight GPIB DIO lines low, thus asserting it to a logic one. If S = 1 and ist = 0, the NAT4882 does not assert the DIO line. If S = 0, the status is *in reverse phase*, meaning that if, during a Parallel Poll, ist = 0, and U = 0, the NAT4882 responds to the Parallel Poll by driving one of the eight GPIB DIO lines low. If S = 0 and ist = 1, the NAT4882 does not assert the DIO line. Refer to the description of *Auxiliary Register B* and *Clear Parallel Poll Flags/Set Parallel Poll Flags* later in this chapter for more information.
2-0w	P[3-1]	Parallel Poll Response bits 3 through 1 PPR bits 3 through 1, designated P[3-1], contain an encoded version of the Parallel Poll response. P[3-1] indicate which of the eight DIO lines is asserted during a Parallel Poll (equal to N-1). For example, if P[3-1] = 010 (binary), GPIB DIO line DIO3* is driven low (asserted) if the GPIB chip is parallel polled and S = ist.

Some examples of configuring the Parallel Poll Register are as follows:

Written to the AUXMR 7 6 5 4 3 2 1 0	Result
0 1 1 1 0 0 0 0	Unconfigures PPR.
0 1 1 0 0 0 0 0	0 0 0 0 0 is written to the PPR. If ist = 0, the GPIB chip participates in a Parallel Poll asserting the DIO1 line. Otherwise, it does not participate.
0 1 1 0 1 0 0 1	0 1 0 0 1 is written to the PPR. If ist = 1, the GPIB chip participates in a Parallel Poll asserting the DIO2 line. Otherwise, it does not participate.

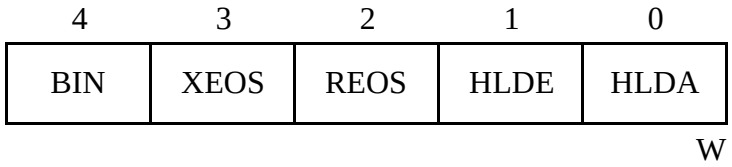
Auxiliary Register A (AUXRA)

Access: location 5 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Control Code: 100 (Binary, bits 7 - 5)

Attributes: Write-Only
Accessed through AUXMR



Writing to Auxiliary Register A (AUXRA) is done via the AUXMR. Writing the binary value 100 into the Control Code (CNT[2-0]) and a bit pattern into the Command Code (COM[4-0]) portion of the AUXMR causes the Command Code to be written to Auxiliary Register A. When the data is written to AUXRA, the bits are denoted by the mnemonics shown in the figure above. This 5-bit code controls the data transfer messages Holdoff and EOS/END. The AUXRA is cleared by a chip reset or a hardware reset.

Bit	Mnemonic	Description
4w	BIN	Binary bit The BIN bit selects the length of the EOS message. If BIN = 1, the End Of String Register (EOSR) is treated as a full 8-bit byte when the NAT4882 checks the GPIB data for End Of String. If BIN = 0, the EOSR is treated as a 7-bit register (for ASCII characters) and only a 7-bit comparison is done with the data on the GPIB.
3w	XEOS	Transmit END with EOS bit The XEOS bit permits or prohibits automatic transmission of the GPIB END message at the same time as the EOS message when the NAT4882 is in Talker Active State (TACS). If XEOS = 1 and the byte in the CDOR matches the contents of the EOSR, the EOI line is sent true along with the data.
2w	REOS	END on EOS Received bit The REOS bit permits or prohibits setting the END bit (ISR1[4]r) upon receiving the EOS message when the NAT4882 is in Listener Active State (LACS). If REOS = 1 and the byte in the DIR matches the byte in the EOSR, the END bit (ISR1[4]r) is set and the acceptor function treats the EOS character just as if it were received with EOI asserted.

Bit	Mnemonic	Description
1-0w	HLDE HLDA	Holdoff on End bit Holdoff on All bit

HLDE and HLDA together determine the GPIB data receiving mode. The four possible modes are as follows:

HLDE	HLDA	Data Receiving Mode
0	0	Normal Handshake mode
0	1	RFD Holdoff on All Data mode
1	0	RFD Holdoff on END mode
1	1	Continuous mode

In Normal Handshake mode, the local message rdy is generated when data is received from the GPIB. When the received data is read from the DIR, rdy is generated in Acceptor Not Ready State (ANRS), the RFD message is transmitted, and the GPIB Handshake continues.

In RFD Holdoff on All Data (HLDA) mode, RFD is not sent true after data is received until the Finish Handshake auxiliary command is issued. Unlike normal Handshake mode, the RFD HLDA mode does not generate the rdy message even if the received data is read through the DIR–that is, the GPIB RFD message is not generated.

In RFD Holdoff on End mode, operation is the same as the RFD HLDA mode, but only when the end of the data block (EOS or END message) is detected–that is, when the END message is received, or if REOS is set and the EOS character is received, or when NLEE is set and the NL character is received. The Finish Handshake auxiliary command releases Handshake Holdoff.

In continuous mode, the rdy message is generated when in ANRS until the end of the data block is detected. A Holdoff is generated at the end of a data block. The Finish Handshake auxiliary command must be issued to release the Holdoff. The continuous mode is useful for monitoring the data block transfer without actually participating in the transfer (no data reception). In Continuous mode, the DI bit (ISR1[0]r) is not set by receiving a data byte.

Auxiliary Register B (AUXRB)

Access: location 5 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Control Code: 101 (Binary, bits 7 - 5)

Attributes: Write-Only
Accessed through AUXMR

4	3	2	1	0
ISS	INV	TRI	SPEOI	CPT ENABLE
				W

Writing to Auxiliary Register B (AUXRB) is done via the AUXMR. Writing the value 101 into the Control Code (CNT[2-0]) and a bit pattern into the Command Code portion (COM[4-0]) of the AUXMR causes the Command Code to be written to AUXRB. When the data is written to AUXRB, the bits are denoted as shown in the figure above. This 5-bit code affects several interface functions, as described in the following paragraphs. The AUXRB is cleared by a chip reset or a hardware reset.

Bit	Mnemonic	Description
4w	ISS	Individual Status Select bit The ISS bit determines the value of the NAT4882 ist. If ISS = 1, ist takes on the value of the NAT4882 Service Request State (SRQS). (The NAT4882 is asserting the GPIB SRQ message when it is in SRQS.) If ISS = 0, ist takes on the value of the NAT4882 Parallel Poll Flag. The Parallel Poll Flag is set and cleared using the Set Parallel Poll Flag and Clear Parallel Poll Flag auxiliary commands.
3w	INV	Invert bit The INV bit affects the polarity of the NAT4882 INT pin. If INV = 1, the polarity of the Interrupt (INT) pin on the NAT4882 is active low.
2w	TRI	Three-State Timing bit The TRI bit determines the NAT4882 GPIB Source Handshake Timing, T1. TRI can be set to enable high-speed data transfers (T1 ≥ 500 nsec) when tri-state GPIB drivers are used. Setting TRI enables high-speed timing as T1 of the GPIB Source Handshake after transmission of the first data byte. Clearing TRI sets the low-speed timing (T1 ≥ 2 µsec). The T1 delay can be reduced further by setting the USTD bit (AUXRI[3]w) or MSTD bit .

Bit	Mnemonic	Description
1w	SPEOI	Send Serial Poll EOI bit The SPEOI bit permits or prohibits the transmission of the END message in Serial Poll Active State (SPAS). If SPEOI = 1, EOI is sent true when the NAT4882 is in SPAS and is sourcing an STB. Otherwise, EOI is sent false in SPAS.
0w	CPT ENABLE	Command Pass Through Enable bit The CPT ENABLE bit permits or prohibits the detection of undefined GPIB commands and permits or prohibits the setting of the CPT bit (ISR1[7]r) on receipt of an undefined command. If CPT ENABLE = 1 and an undefined command has been received, the DAC message is held and the Handshake stops until the Valid or Non-valid auxiliary command is issued. The undefined command can be read from the CPTR and processed by the software.

Auxiliary Register E (AUXRE)

Access: location 5 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Control Code: 1100 (Binary, bits 7 - 4)

Attributes: Write-Only
Accessed through AUXMR

3	2	1	0
DHADT	DHADC	DHDT	DHDC
			W

Writing to Auxiliary Register E (AUXRE) is done via the AUXMR. Writing the binary value 1100 into the Data Lines 7 through 4 and a bit pattern into the lower four bits of the AUXMR (COM[3-0]) causes the four lowest order bits to be written to AUXRE. The 4-bit code determines how the NAT4882 uses DAC Holdoff. The AUXRE is cleared by a chip reset or a hardware reset.

Bit	Mnemonic	Description
3w	DHADT	DAC Holdoff on GET bit Setting DHADT enables DAC Holdoff when the acceptor handshake function receives the GET command. When this occurs, the CPT bit in ISR1 is set. Clearing DHADT disables DAC Holdoff on GET. Issuing the Valid or the Non-valid auxiliary command releases the Holdoff. With this feature, you are notified via a CPT interrupt that GET was sent regardless of the status of the Listener function.
2w	DHADC	DAC Holdoff on DCL or SDC bit Setting DHADC enables DAC Holdoff when the acceptor handshake function receives the DCL or SDC command. When this occurs the CPT bit in ISR1 is set. Clearing DHADC disables DAC Holdoff on DCL or SDC. Issuing the Valid or the Non-valid auxiliary command releases the Holdoff. With this feature, you are notified via a CPT interrupt that DCL or SDC was sent regardless of the status of the Listener function.
1w	DHDT	DAC Holdoff on DTAS bit Setting DHDT enables DAC Holdoff when the NAT4882 enters Device Trigger Active State (DTAS). Clearing DHDT disables DAC Holdoff on DTAS. Issuing the Valid or the Non-valid auxiliary command releases the Holdoff.

Bit	Mnemonic	Description
0w	DHDC	DAC Holdoff on DCAS bit Setting DHDC enables DAC Holdoff when the NAT4882 enters Device Clear Active State (DCAS). Clearing DHDC disables DAC Holdoff on DCAS. Issuing the Valid or the Non-valid auxiliary command releases the Holdoff.

Auxiliary Register F (AUXRF)

Access: location 5 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Control Code: 1101 (Binary, bits 7 - 4)

Attributes: Write-Only
Accessed through AUXMR

3	2	1	0
DHATA	DHALA	DHUNTL	DHALL
			W

Writing to Auxiliary Register F (AUXRF) is done via the AUXMR. Writing the binary value 1101 into the Data Lines 7 through 4 and a bit pattern into the lower four bits of the AUXMR (COM[3-0]) causes the four lowest order bits to be written to AUXRF. The 4-bit code determines how the NAT4882 uses DAC Holdoff. The AUXRF is cleared by a chip reset or a hardware reset.

Bit	Mnemonic	Description
3w	DHATA	DAC Holdoff on All Talker Addresses bit Setting DHATA enables DAC Holdoff when the Acceptor Handshake function receives any primary Talker Address. When this occurs the CPT bit in ISR1 is set. Clearing DHATA disables DAC Holdoff on primary Talker Addresses. Issuing the Valid or the Non-valid auxiliary command releases the Holdoff. With this feature, you are notified via a CPT interrupt that a primary Talker Address was issued.
2w	DHALA	DAC Holdoff on All Listener Addresses bit Setting DHALA enables DAC Holdoff when the Acceptor Handshake function receives any primary Listener Address. When this occurs the CPT bit in ISR1 is set. Clearing DHALA disables DAC Holdoff on primary Listener Addresses. Issuing the Valid or the Non-valid auxiliary command releases the Holdoff. With this feature you are notified via a CPT interrupt that a primary Listener Address was issued.
1w	DHUNTL	DAC Holdoff on the UNT or UNL Command bit Setting DHUNTL enables DAC Holdoff when the Acceptor Handshake function receives the UNT or UNL command. When this occurs the CPT bit in ISR1 is set. Clearing DHUNTL disables

Bit	Mnemonic	Description
		DAC Holdoff on UNT and UNL. Issuing the Valid or the Non-valid auxiliary command releases the Holdoff. With this feature, you are notified via a CPT interrupt that UNT or UNL was issued.
0w	DHALL	DAC Holdoff on All UCG, ACG, and SCG Commands bit Setting DHALL enables DAC Holdoff when the Acceptor Handshake function receives any UCG, ACG, or SCG command. When this occurs the CPT bit in ISR1 is set. Clearing DHALL disables DAC Holdoff on any UCG, ACG, or SCG command. Issuing the Valid or the Non-valid auxiliary command releases the Holdoff. With this feature, you are notified via a CPT interrupt that a UCG, ACG, or SCG command was issued.

Auxiliary Register G (AUXRG)

Access: location 5 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Control Code: 0100 (Binary, bits 7 - 4)

Attributes: Write-Only
Accessed through AUXMR

3	2	1	0
NTNL	RPP2	DISTCT	CHES

W

Writing to Auxiliary Register G (AUXRG) is done via the AUXMR. Writing the binary value 0100 into the Data Lines 7 through 4 and a bit pattern into the lower four bits of the AUXMR (COM[3-0]) causes the four lowest order bits to be written to AUXRG. The AUXRG is cleared by a chip reset or a hardware reset.

Bit	Mnemonic	Description
3w	NTNL	No Talking When No Listener bit Setting this bit prevents the chip from sourcing data (talking) when there is no external Listener, modifies the setting of the ERR bit, modifies the way the nba local message is cleared, and changes the EOI generation function. If NTNL is cleared, the NAT4882 Source Handshake State machine performs the following: the Source NRFD is unasserted; the ERR bit is set on TACS&SDYS&DAC&RFD + SIDS&(write CDOR) + (the transition from SDYS to SIDS if the local message nba is cleared upon entering SIDS or STRS); and the send EOI auxiliary command is ignored or forgotten upon exiting TACS. If NTNL = 1, the Source Handshake function will not make the transition from SDYS to STRS unless there is an external Listener (that is, a device on the GPIB is asserting NDAC); the ERR bit is set when the T1 delay has elapsed and TACS&SDYS&EXTDAC&RFD (where EXTDAC refers to some device on the GPIB asserting NDAC); the local nba is cleared upon entering STRS and ~SPAS; and the send EOI auxiliary command is cleared upon entering SDYS or STRS.
2w	RPP2	Request Parallel Poll 2 bit During the execution of a Parallel Poll via the Execute Parallel Poll auxiliary command, the NAT4882 asserts the GPIB lines ATN and EOI (Controller state CPWS) for approximately 2 µsecs (T6) and then latches the state of the DIO lines into the Command Pass

Bit	Mnemonic	Description
		Through Register. In some situations, such as with bus extenders, it is desirable to extend the amount of time that ATN and EOI are asserted by extending the time value of T6. Setting the RPP2 bit causes a Parallel Poll to execute which does not terminate until the RPP2 bit is cleared via software. Using this method, the amount of time that ATN and EOI are asserted is controlled by software and can be any value. The result of the Parallel Poll must be read in the CPTR before RPP2 is cleared.
1w	DISTCT	Disable Automatic Take Control bit If DISTCT = 0 and control is passed to the NAT4882 by the Take Control GPIB command (TCT), the NAT4882 automatically becomes Controller-In-Charge. In some applications (such as Talker/Listener only configurations) this feature is undesirable. Setting the DISTCT bit disables the NAT4882's ability to automatically take control when another GPIB Controller-In-Charge passes control. However, even if DISTCT is set, the interface chip can still take control by issuing the Request Control auxiliary command. When DISTCT is set the TCT command is considered undefined.
0w	CHES	Clear Holdoff on End Select bit CHES determines how long the NAT4882 remembers that it detected an END condition. IF CHES = 0, the NAT4882 remembers the detection of the END condition until the Release Handshake Holdoff auxiliary command is issued. This command causes the NAT4882 holdoff circuitry to treat every data byte as if it was the END message until the Release Handshake auxiliary command is issued. If CHES is set, the NAT4882 remembers the detection of the END condition until the Release Handshake Holdoff auxiliary command is issued or the DIR is read when in the normal Handshake Holdoff mode (that is, HLDE and HLDA cleared). This setting causes the NAT4882 holdoff circuitry to treat every data byte as it appears, with or without END.

Auxiliary Register I (AUXRI)

Access: location 5 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Control Code: 1110 (Binary, bits 7 - 4)

Attributes: Write-Only
Accessed through AUXMR

3	2	1	0
USTD	PP2	ACC	SISB
			W

Writing to Auxiliary Register I (AUXRI) is done via the AUXMR. Writing the binary value 1110 into the Data Lines 7 through 4 and a bit pattern into the lower four bits of the AUXMR (COM[3-0]) causes the four lowest order bits to be written to AUXRI. The AUXRI is cleared by a chip reset or a hardware reset.

Bit **Mnemonic** **Description**

3w USTD Ultra Short T1 Delay bit

USTD sets the value of the T1 delay used by the Source Handshake function for data setup to 350 nsec for the second and subsequent data bytes sent after ATN unasserts. If this bit is cleared, the value of T1 is determined by the TRI bit (AUXRB[2]w). The bit is overridden by the MSTD in the KCR.

TRI Bit	UST D Bit	T1 for first data & all commands	T1 for the second and remaining data
0	0	2 µsec	2 µsec
0	1	1.1 µsec	1.1 µsec
1	0	2 µsec	500 nsec
1	1	1.1 µsec	350 nsec

2w PP2 Parallel Poll 2 bit

If PP2 = 0, the NAT4882 responds to Parallel Polls in the same manner as the µPD7210–that is, by supporting Parallel Poll functions PP1 and PP2 at the same time. However, a contradiction arises because PP1 requires the interface to be configured by remote GPIB commands and PP2 requires the interface to be

Bit	Mnemonic	Description
		configured locally and ignore remote GPIB commands. When PP2 is set, the chip ignores remote GPIB commands (that is, PPC & PPU are treated as undefined commands), thus allowing a true implementation of PP2. Also, by setting PP2 and U (PPR[4]w), the chip supports PP0 (no Parallel Poll response).
1w	ACC	Automatic Carry Cycle bit Setting ACC enables automatic carry cycles on GPIB DMA transfers. When this bit is set during GPIB DMA reads, the Acceptor Handshake function performs an RFD Holdoff on the last byte read by the DMA Controller–that is, on the byte in which the T/C signal is pulsed during the read. Issuing the Finish Handshake auxiliary command releases the holdoff. If this bit is set during GPIB DMA writes, the source handshake function issues EOI with the last byte written to the CDOR by the DMA Controller–that is, the byte in which the T/C signal is pulsed when written. **Note:** When you use the NAT4882 with the Turbo488, do not set this bit, because the Turbo488 handles Carry Cycles automatically and the T/C pin is normally grounded.
0w	SISB	Static Interrupt Status Bits bit Setting SISB changes the ISR0, ISR1, and ISR2 bits (in µPD7210 mode) from being automatically cleared by reads of the corresponding Interrupt Status register to being static bits that remain set until a certain condition is met. Table 2-5 lists the condition for clearing each interrupt status bit when SISB = 1.

Table 2-5. Clear Conditions for SISB Bit

Bit	Clear Condition when SISB = 1
CPT	pon + read CPTR
APT	pon + Valid + Non-Valid
DET	pon + clearDET
END	pon + clearEND
DEC	pon +clearDEC
ERR	pon + clearERR
DO	pon + ~TACS +~SGNS +nba
DI	pon + (finish handshake) * (Holdoff mode) + read DIR
SRQI	pon + clearSRQI

(continues)

Table 2-5. Clear Conditions for SISB Bit (continued)

Bit	Clear Condition when SISB = 1
CO	pon + ~CACS + ~SGNS + nba
LOKC	pon + clear LOKC
REMC	pon + clearREMC
ADSC	pon + clearADSC + ton +lon
IFCI	pon + clearIFCI
ATNI	pon + clearATNI

Note: Interrupt Status bits STBO, SYNC, and TO are not affected by the SISB bit.

Auxiliary Register J (AUXRJ)

Access: location 5 (not affected by the page-in auxiliary command or the Page-In pin)

Mode: µPD7210

Control Code: 1111 (Binary, bits 7 - 4)

Attributes: Write-Only
Accessed through AUXMR

3	2	1	0
TM3	TM2	TM1	TM0
			W

Writing to Auxiliary Register J (AUXRJ) is done via the AUXMR. Writing the binary value 1111 into the Data Lines 7 through 4 and a bit pattern into the lower four bits of the AUXMR (COM[3-0]) causes the four lowest order bits to be written to AUXRJ.

Auxiliary Register J is a four-bit register that sets the timeout value of the Timer interrupt. The timeout value can be set between the range of 10 µsec and 134 sec when the NAT4882 clock is 20 MHz. The Timer starts when the Timer Register is written with a nonzero value and sets the TO bit in ISR0 when the timeout value expires. The Timer is cleared when a zero is written to the Timer Register. For more information on the Timer interrupt capability see *Interrupt Status Register 0* later in this chapter. The AUXRJ is reset by a hardware or chip reset.

Bit	Mnemonic	Description
3-0w	TM[3-0]	Timer bits 3 through 0

Table 2-6 lists the approximate timeout values supported by Auxiliary Register J at 20 MHz. If the NAT4882 uses another clock frequency, the timeout value can be computed with the following formula: time = $(2^{factor} * 5)$/frequency

Table 2-6. Timeout Values in µPD7210 Mode

TM3-0	Timeout Value (> or =)	Factor
0000	Disable	-
0001	16 µsec	6
0010	32 µsec	7
0011	128 µsec	9
0100	256 µsec	10

(continues)

Bit **Mnemonic** **Description**

Table 2-6. Timeout Values in µPD7210 Mode (continued)

TM3-0	Timeout Value (> or =)	Factor
0101	1 msec	12
0110	4 msec	14
0111	16 msec	16
1000	33 msec	17
1001	131 msec	19
1010	262 msec	20
1011	1 sec	22
1100	4 sec	24
1101	17 sec	26
1110	34 sec	27
1111	134 sec	29

The Timer supports two different types of timeouts depending on the value of the BTO bit. If BTO is cleared, the Timer operates in global mode. In this mode, the Timer starts upon writing a non-zero value to the Timer Register and continues counting until it reaches the timeout value and sets the TO bit.

If BTO is set, the Timer operates in Byte Timeout mode. In this mode, the Timer starts upon writing a non-zero value to the Timer Register and continues counting until it reaches the timeout value. However, reads of the DIR or writes of the CDOR clear the Timer and force it to start counting over. In Byte Timeout mode, if TO is set, it remains set until the Timer Register is written. Further reads of DIR or writes of CDOR have no effect on TO until the Timer Register is written.

Address Register 0 (ADR0)

Access: location 6 (except immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Read-Only

7	6	5	4	3	2	1	0 R
X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0

Address Register 0 (ADR0) reflects the internal GPIB address status of the NAT4882 as configured using the ADMR. In addressing mode 2, ADR0 indicates the address and enable bits for the primary GPIB address of the NAT4882. In dual primary addressing (Modes 1 and 3) ADR0 indicates the NAT4882 major primary GPIB address. Refer to the description of the *Address Mode Register* earlier in this chapter for information on addressing modes.

Bit	Mnemonic	Description
7r	X	Don't care bit
6r	DT0	Disable Talker 0 bit If DT0 is set, the mode 2 primary (or mode 1 and 3 major) Talker is not enabled, and this register will not be compared with GPIB Talker addresses. If DT0 = 0, the NAT4882 responds to a GPIB talk address matching bits AD[5-0 through 1-0].
5r	DL0	Disable Listener 0 bit If DL0 is set, the mode 2 primary (or mode 1 and 3 major) Listener is not enabled, and this register will not be compared with GPIB Listener addresses. If DL0=0, the NAT4882 responds to a GPIB listen address matching bits AD[5-0 through 1-0].
4-0r	AD[5-0 – 1-0]	NAT4882 GPIB Address bits 5-0 through 1-0 These are the lower 5 bits of the NAT4882 GPIB primary (or major) address. The primary talk address is formed by adding hex 40 to AD[5-0 through 1-0], while the listen address is formed by adding hex 20.

Address Register (ADR)

Access: location 6 (except immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Write-Only

7	6	5	4	3	2	1	0
ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
							W

The Address Register (ADR) loads the internal registers ADR0 and ADR1. Both ADR0 and ADR1 must be loaded for all addressing modes.

Bit	Mnemonic	Description
7w	ARS	Address Register Select bit If ARS = 1, the seven low-order bits of ADR are loaded into internal register ADR1. If ARS = 0, they are loaded into ADR0.
6w	DT	Disable Talker bit DT = 1 disables recognition of the GPIB talk address formed from AD5 through AD1 (ADR[4-0]w).
5w	DL	Disable Listener bit DL = 1 disables recognition of the GPIB listen address formed from AD5 through AD1 (ADR[4-0]w).
4-0w	AD[5-1]	NAT4882 GPIB Address bits 5 through 1 These bits specify the five low-order bits of the GPIB address that is to be recognized by the NAT4882. The corresponding GPIB talk address is formed by adding hex 40 to AD[5-1], while the corresponding GPIB listen address is formed by adding hex 20. The value written to AD[5-1] should not be all ones because the corresponding talk and listen addresses would conflict with the GPIB Untalk (UNT) and GPIB Unlisten (UNL) commands.

Interrupt Status Register 0 (ISR0)

Access: location 6 (immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Read-Only

Interrupt Mask Register 0 (IMR0)

Access: location 6 (except immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Write-Only

7	6	5	4	3	2	1	0	R
cdba	STBO	NL	EOS	IFCI	ATNI	TO	SYNC	
GLINT	STBO IE	NLEE	BTO	IFCI IE	ATNI IE	TO IE	SYNC IE	W

The Interrupt Status Register 0 (ISR0) consists of five Interrupt Status bits and three Internal Status bits. The Interrupt Mask Register 0 (IMR0) consists of six Interrupt Enable bits and two Internal Control bits. If the Interrupt Enable bit is true when the corresponding status condition or event occurs, an interrupt request is generated. Bits in ISR0 are set and cleared regardless of the status of the bits in IMR2. If a condition occurs that requires the NAT4882 to set or clear an Interrupt Status bit in the ISR0 at the same time the ISR2 is being read, the NAT4882 holds off setting or clearing the bit or bits until the read is finished. A hardware reset clears all bits in IMR0 except GLINT, which is set.

Bit	Mnemonic	Description
7r	cdba	Command/Data Byte Available local message bit This bit reflects the status of the local message Command/Data Byte Available. cdba is set on writes to the CDOR and cleared on entrance to STRS, pon, nbaf or the entrance into SIDS when NTNL = 0.
7w	GLINT	Global Interrupt Enable bit GLINT provides a Global Interrupt Enable. If this bit is cleared, the NAT4882 does not generate an Interrupt request regardless of the state of the ISR bits and IMR bits. If this bit is set, the NAT4882 can generate interrupts. A hardware reset sets this bit.

Bit	Mnemonic	Description
6r	STBO	Status Byte Out bit
6w	STBO IE	Status Byte Out Interrupt Enable bit

STBO is set if it enters SPAS when STBO IE is set, thus causing an interrupt. The control program writes the current STB to the SPMR which will be transmitted to the GPIB as the STB. Writing the SPMR, clears STBO, which is then set upon entering SPAS during the next serial poll. When STBO IE is set, the rsv bit in the SPMR has no effect on the SR function and rsv must be generated via the reqt auxiliary command.

STBO is set by:

STBO IE & SPAS

STBO is cleared by:

pon + (write SPMR) + ~SPAS

Notes

SPAS: GPIB Serial Poll Active State
pon: Power On Reset
write SPMR: Write the Serial Poll Mode Register

5r NL — New Line Receive bit

NL is set when the NAT4882 accepts the ASCII new line character from the GPIB data bus.

NL is set by:

LACS & NL & ACDS

NL is cleared by:

pon + (LACS & ~NL & ACDS)

Notes

LACS: GPIB Listener Active State
NL: seven bit ASCII 'new line' character (hex 0A)
ACDS: GPIB Accept Data State
pon: Power On Reset

5w NLEE — New Line End Enable bit

If NLEE = 1, the NAT4882 treats the seven-bit ASCII new line character (0A hex) as an EOS character. The Acceptor Handshake function responds to the acceptance of a new line character as if EOI was sent.

Bit	Mnemonic	Description
4r	EOS	End-Of-String Character bit The EOS bit indicates that the END bit in ISR1 was set by the acceptance of the End-Of-String character. EOS is set by: LACS & EOS & REOS & ACDS EOS is cleared by: pon + (LACS & ~EOS & ACDS) + ~REOS **Notes** LACS: GPIB Listener Active State EOS: GPIB End-Of-String message REOS: End on EOS Received bit, AUXRA[2]w ACDS: GPIB Accept Data State pon: Power On Reset
4w	BTO	Byte Timeout bit Setting BTO enables Byte Timeouts. For more information on the function of Byte Timeouts, see *Auxiliary Register J* earlier in this chapter.
3r 3w	IFCI IFCI IE	IFC Interrupt bit IFC Interrupt Enable bit IFCI is set on the assertion of the GPIB IFC* line. IFCI is set by: (IFC & ~SACS) becomes true IFCI is cleared by: pon + (read ISR0) & ~SISB + clearIFCI **Notes** IFC: GPIB Interface Clear Signal SACS: GPIB System Control Active State read ISR0: Read the Interrupt Status Register 0 SISB: Static Interrupt Status Bit, AUXRI[0]w pon: Power On Reset clearIFCI: clearIFCI Auxiliary Command issued

Bit	Mnemonic	Description
2r 2w	ATNI ATNI IE	ATN Interrupt bit ATN Interrupt Enable bit

ATNI is set on the assertion of the GPIB ATN* line.

ATNI is set by:

(ATN) becomes true

ATNI is cleared by:

pon + (read ISR0) & ~SISB + clearATNI

Notes

ATN:	GPIB Attention Signal
read ISR0:	Read the Interrupt Status Register 0
SISB:	Static Interrupt Status Bit, AUXRI[0]w
pon:	Power On Reset
clearATNI:	clearATNI Auxiliary Command issued

1r 1w	TO TO IE	Time-Out bit Time-Out Interrupt Enable bit

TO reflects the status of the Timer. Once started, the Timer sets the timeout status bit after the amount of time specified in the Timer Register has elapsed (see Auxiliary Register J). An interrupt is generated when TO IE and TO are set. TO is cleared when the Timer Register is written.

0r 0w	SYNC SYNC IE	GPIB Synchronization bit GPIB Synchronization Interrupt Enable bit

This bit reflects the status of a GPIB handshake line after a transfer. It is set at the completion of a transfer when the GPIB handshake is complete. An interrupt is generated when SYNC IE and SYNC are set. For more information, refer to the *Synchronization Detection* section in Chapter 3, *NAT4882 Programming Considerations*.

Address Register 1 (ADR1)

Access: location 7 (except immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Read-Only

7	6	5	4	3	2	1	0	R
EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1	

Address Register 1 (ADR1) indicates the status of the GPIB address and enable bits for the secondary address of the NAT4882 if mode 2 addressing is used, or the minor primary address of the NAT4882 if dual primary addressing is used (modes 1 and 3). If mode 1 addressing is used and only a single primary address is needed, both the talk and listen addresses must disable in this register. If mode 2 addressing is used, the talk and listen disable bits in this register must match those in ADR0.

Bit	Mnemonic	Description
7r	EOI	End Or Identify bit EOI indicates the value of the GPIB EOI line latched when a data byte is received by the NAT4882 GPIB Acceptor Handshake (AH) function. If EOI = 1, the EOI line was asserted with the received byte. EOI is cleared by issuing the Chip Reset auxiliary command. EOI is updated after each byte is received.
6r	DT1	Disable Talker 1 bit If DT1 is set, the mode 2 secondary (or mode 1 and 3 minor) Talker function is not enabled–that is, the GPIB secondary address (or minor primary talk address) is not compared with this register. If DT1 is cleared, and the NAT4882 received its primary talk address (that is, in TPAS), the secondary address is checked when in mode 2. In mode 1 or 3, the minor talk address is checked.
5r	DL1	Disable Listener 1 bit If DL1 is set, the mode 2 secondary (or mode 1 and 3 minor) Listener function is not enabled–that is, the GPIB secondary address (or minor primary listen address) is not compared with this register. If DL1 is cleared, and the NAT4882 received its primary listen address (that is, in LPAS), the secondary address is checked when in mode 2. In mode 1 or 3, the minor listen address is checked.

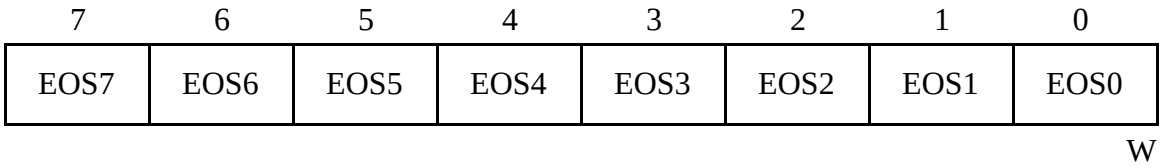
Bit	Mnemonic	Description
4-0r	AD[5-1 – 1-1]	NAT4882 GPIB Address bits 5-1 through 1-1 These are the lower five bits of the NAT4882 secondary or minor address. The secondary address is formed by adding hex 60 to bits AD[5-1 through 1-1]. The minor talk address is formed by adding hex 40 to AD[5-1 through 1-1], while the listen address is formed by adding hex 20.

End Of String Register (EOSR)

Access: location 7 (except immediately after the page-in auxiliary command is issued or if the Page-In pin is asserted)

Mode: µPD7210

Attributes: Write-Only



The End Of String Register (EOSR) holds the byte that the NAT4882 uses to detect the end of a GPIB data block transfer. You can place a seven- or eight-bit byte (ASCII or binary) in the EOSR to be used in detecting the end of a block of data. The length of the EOS byte to be used in the comparison is selected by the BIN bit in Auxiliary Register A, AUXRA[4]w.

If the NAT4882 is a Listener and bit REOS of AUXRA is set, the END bit is set in ISR1 whenever the byte in the DIR matches the EOSR. If the NAT4882 is a Talker and bit XEOS of AUXRA is set, the END message (GPIB EOI* line asserted low) is sent along with the data byte whenever the contents of the CDOR matches the EOSR.

Bit	**Mnemonic**	**Description**
7-0w	EOS[7-0]	End of String bits 7 through 0

Bus Status Register (BSR)

Access: location 7 (immediately after the page-in auxiliary command is issued or if the Page-In Pin is asserted)
Mode: µPD7210

Attributes: Read-Only

Bus Control Register (BCR)

Access: location 7 (immediately after the page-in auxiliary command is issued or if the Page-In Pin is asserted)
Mode: µPD7210

Attributes: Write-Only

Reads of the Bus Status Register (BSR) return the status of the GPIB control lines at the time of the read. Writing a one to a bit in the Bus Control Register (BCR) asserts the corresponding GPIB control lines. The order of bits in the BCR and BSR are shown below:

7	6	5	4	3	2	1	0 R
ATN_S	DAV_S	NDAC_S	NRFD_S	EOI_S	SRQ_S	IFC_S	REN_S
ATN_C	DAV_C	NDAC_C	NRFD_C	EOI_C	SRQ_C	IFC_C	REN_C
							W

Because the chip is either transmitting or receiving a GPIB control line at any particular time, and not doing both simultaneously, setting a bit in the BCR may not automatically assert the corresponding line on the GPIB. If the chip is transmitting a GPIB line when the corresponding bit in the BCR is set, the chip asserts the GPIB line. If the chip is receiving a GPIB line when the corresponding bit in the BCR is set, the GPIB line is not asserted. However, in both these cases, the GPIB signal internal to the interface chip is logically ORed with the value of the BCR bit. Figure 2-3 illustrates the GPIB input/output hardware configuration.

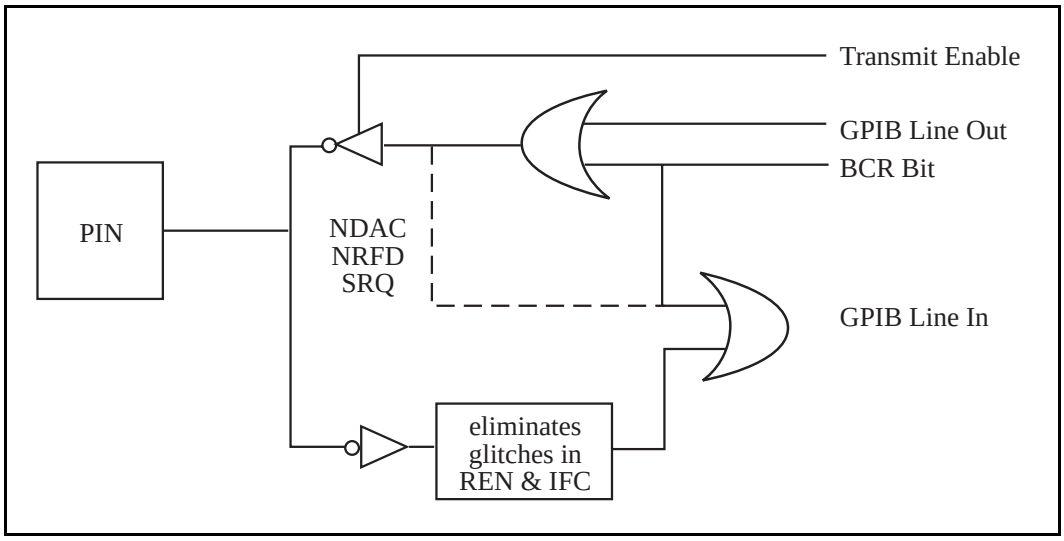


Figure 2-3. GPIB I/O Hardware Configuration for µPD7210 Mode

Transmit Enable represents the internal signal that is true when the chip is driving a particular GPIB control line. *GPIB Line Out* represents the internal signal that is true when an interface function within the chip is attempting to assert a GPIB control signal. *BCR bit* corresponds to the bit in the Bus Control register. *GPIB Line In* represents the internal GPIB lines that are inputs to the GPIB interface functions and the Bus Status register. The internal signals *SRQ*, *NDAC*, and *NRFD* are monitored by the interface functions even when they are not driven onto the pin. For this reason, the internal value of these signals is ORed with the external value.

Bit	**Mnemonic**	**Description**
7r	ATN_S	GPIB Attention Status bit
7w	ATN_C	GPIB Attention Control bit
6r	DAV_S	GPIB Data Valid Status bit
6w	DAV_C	GPIB Data Valid Control bit
5r	NDAC_S	GPIB Not Data Accepted Status bit
5w	NDAC_C	GPIB Not Data Accepted Control bit
4r	NRFD_S	GPIB Not Ready For Data Status bit
4w	NRFD_C	GPIB Not Ready For Data Control bit
3r	EOI_S	GPIB End or Identify Status bit
3w	EOI_C	GPIB End or Identify Control bit
2r	SRQ_S	GPIB Service Request Status bit
2w	SRQ_C	GPIB Service Request Control bit
1r	IFC_S	GPIB Interface Clear Status bit
1w	IFC_C	GPIB Interface Clear Control bit
0r	REN_S	GPIB Remote Enable Status bit
0w	REN_C	GPIB Remote Enable Control bit

Because the BSR samples the GPIB control lines from the GPIB transceiver and not the actual GPIB bus, the validity of each bit is determined by the direction of each line. Generally, when a signal is an input, its true bus status is reflected in the BSR, while an output signal only reflects the NAT4882 value of that particular line. Under normal GPIB operation, this function should not be too limiting, because the lines that are typically monitored are valid when they are monitored. For example, the SRQ line is valid in the BSR when the NAT4882 is CIC, which is also when the SRQ line will be monitored.

9914 Mode Registers

The 9914 mode register group consists of 26 registers available when the NAT4882 is in 9914A mode. This set of registers is a compatible superset of those found in the Texas Instruments TMS9914A.

Figure 2-4 shows the register map for the NAT4882 in 9914 mode, and Figure 2-5 shows the 9914 hidden registers. The leftmost column of each register map gives the name of each register in mnemonic form. Following the register names is the register offset, and then a block showing the bits of all of the registers at that offset. On the rightmost column of each register, the map tells whether that register is a read-only or a write-only register. In the cases where there is more than one register at the same offset, the register with the white bitmap normally responds at that offset, and the shaded register responds only after it has been paged-in. In the 9914A mode, all of the shaded registers are at the same offset and there is a separate page-in command for each one. The registers remain paged in until another page-in command is issued or a chip reset occurs.

Key

= 9914 Mode Paged Registers
R = Read Register
W = Write Register

		7	6	5	4	3	2	1	0	
ISR0	+0	INT0	INT1	BI	BO	END	SPAS	RLC	MAC	R
IMR0		DMAO	DMAI	BI IE	BO IE	END IE	SPAS IE	RLC IE	MAC IE	W
ISR1	+1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	R
IMR1		GET IE	ERR IE	UNC IE	APT IE	DCAS IE	MA IE	SRQ IE	IFC IE	W
ADSR	+2	REM	LLO	ATN	LPAS	TPAS	LA	TA	ulpa	R
IMR2		GLINT	STBO IE	NLEE	BTO	LLOC IE	ATNI IE	TO IE	CIC IE	W
EOSR		EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0	W
BCR		ATN_C	DAV_C	NDAC_C	NRFD_C	EOI_C	SRQ_C	IFC_C	REN_C	W
ACCR		CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0	W
BSR	+3	ATN_S	DAV_S	NDAC_S	NRFD_S	EOI_S	SRQ_S	IFC_S	REN_S	R
AUXCR		CS	0	0	F4	F3	F2	F1	F0	W
ISR2	+4	cdba	STBO	NL	EOS	LLOC	ATNI	TO	CIC	R
ADR		edpa	dal	dat	A5	A4	A3	A2	A1	W
SPSR	+5	S8	PEND	S6	S5	S4	S3	S2	S1	R
SPMR		S8	rsv/RQS	S6	S5	S4	S3	S2	S1	W
CPTR	+6	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0	R
PPR		PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	W
DIR	+7	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	R
DOR		DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	W

Figure 2-4. 9914 Mode Interface Registers

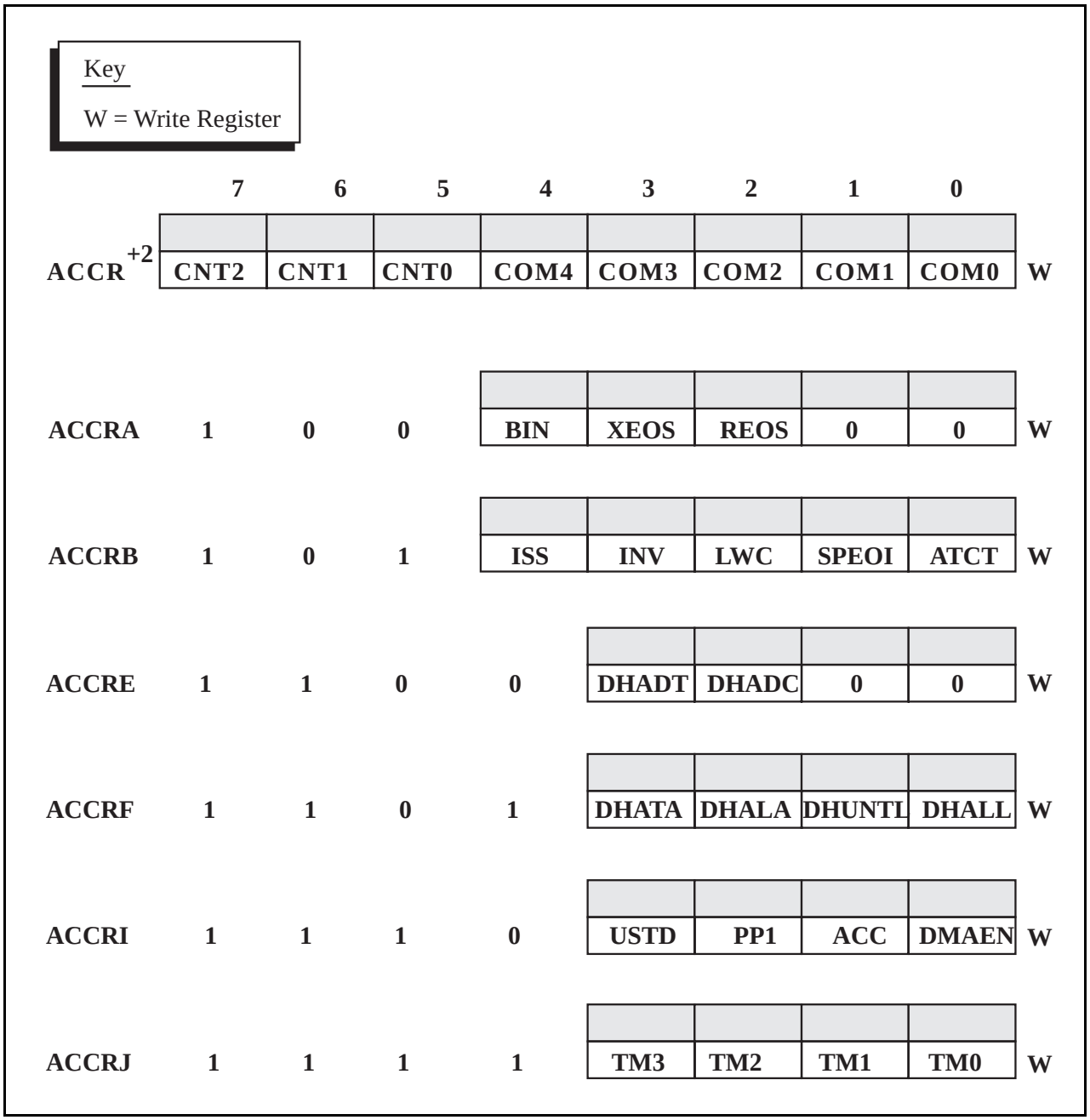


Figure 2-5. 9914 Mode Hidden Registers

Interrupt Status Register 0 (ISR0)

Access: location 0 (if Swap* is unasserted) or location 6 (if Swap* is asserted)
(not affected by a page-in auxiliary command)

Mode: TMS9914A

Attributes: Read-Only
Bits are cleared when read

Interrupt Mask Register 0 (IMR0)

Access: location 0 (if Swap* is unasserted) or location 6 (if Swap* is asserted)
(not affected by a page-in auxiliary command)

Mode: TMS9914A

Attributes: Write-Only

7	6	5	4	3	2	1	0	R
INT0	INT1	BI	BO	END	SPAS	RLC	MAC	
DMAO	DMAI	BI IE	BO IE	END IE	SPAS IE	RLC IE	MAC IE	
								W

The Interrupt Status Register 1 (ISR1) is composed of eight Interrupt Status bits. The Interrupt Mask Register 1 (IMR1) is composed of six Interrupt Enable bits that directly correspond to the Interrupt Status bits in ISR1. As a result, ISR1 and IMR1 service six possible interrupt conditions, where each condition has an Interrupt Status bit and an Interrupt Enable bit associated with it. If the Interrupt Enable bit is true when the corresponding status condition or event occurs, a hardware interrupt request is generated. Bits in ISR1 are set and cleared by the NAT4882 regardless of the status of the Interrupt bits in IMR1. If an interrupt condition occurs at the same time ISR1 is being read, the NAT4882 holds off setting the corresponding Status bit until the read has finished.

Bit	Mnemonic	Description
7r	INT0	Interrupt Register 0 Interrupt bit INT0 is set when an unmasked status bit in Interrupt Status Register 0 is set to a 1.
7w	DMAO	DMA Output Enable bit If DMAEN = 0, this bit has no meaning. If DMAEN = 1, setting DMAO enables the NAT4882 to assert the DRQ line when TACS & SGNS & ~cdba. Once asserted, the NAT4882 keeps the DRQ pin asserted until ~[TACS & SGNS & ~cdba].

Bit	Mnemonic	Description
6r	INT1	Interrupt Register 1 Interrupt bit INT1 is set when an unmasked status bit in Interrupt Status Register 1 is set.
6w	DMAI	DMA Input Enable bit If DMAEN = 0, this bit has no meaning. If DMAEN = 1, setting DMAI enables the NAT4882 to assert the DRQ line when LACS & ACDS & ~shadow handshaking. Once asserted, the NAT4882 keeps the DRQ pin asserted until the DIR is read.
5r	BI	Byte In bit
5w	BI IE	Byte In Interrupt Enable bit The BI bit indicates that a data byte has been received in the Data In Register. An RFD Holdoff must occur before the next data byte can be accepted. BI is cleared by reading the DIR or reading ISR0. BI is not set if shadow handshaking is on. BI is set by: LACS & ACDS & ~shadow handshaking BI is cleared by: swrst + (read ISR0) + (read DIR) **Notes** swrst: software reset Auxiliary Command issued LACS: GPIB Listener Active State ACDS: GPIB Accept Data State shadow handshaking: Shadow Handshaking enabled read ISR0: Read the Interrupt Status Register 0 read DIR: Read the Data In Register
4r	BO	Byte Out bit
4w	BO IE	Byte Out Interrupt Enable bit The BO bit indicates that the Data Out Register is available to send a byte over the GPIB. This byte can be either a command if the device is a Controller or data if the device is a Talker. It is set when the device becomes Active Talker or Controller, but will not occur if the DOR has been loaded with a byte that has not been sent (that is, cdba is true). BO sets again after each byte has been sent and the source handshake returns to SGNS. BO is cleared by writing the DOR or reading ISR0.

Bit	Mnemonic	Description

BO is set by:

CACS & SGNS & ~cdba + TACS & SGNS & ~cdba

BO is cleared by:

swrst + (read ISR0) + (write DOR)

Notes

swrst:	software reset Auxiliary Command issued
TACS:	GPIB Talker Active State
CACS:	GPIB Controller Active State
SGNS:	GPIB Source Generate State
cdba:	Command/Data Byte Available local message
read ISR0:	Read the Interrupt Status Register 0
write DOR:	Write the Data Out Register

3r	END	End Received bit
3w	END IE	End Received Interrupt Enable bit

The END bit is set either when the NAT4882 is a Listener and the GPIB uniline message, END, is received with a data byte from the GPIB Talker, when the data byte in the DIR matches the contents of the End Of String Register (EOSR) and REOS is set, or when the data byte in the DIR matches the ASCII new line character (hex 0A) and NLEE is set. END is always set before the BI bit is set to indicate that the data byte with END was received.

END is set by:

LACS & (EOI + EOS & REOS + NL & NLEE) & ACDS

END is cleared by:

swrst + (read ISR0)

Notes

swrst:	software reset Auxiliary Command issued
LACS:	GPIB Listener Active State
EOI:	GPIB End Of Identify Signal
EOS:	GPIB END Of String message
NL:	ASCII 'new line' message (hex 0A)
ACDS:	GPIB Accept Data State
read ISR0:	Read the Interrupt Status Register 0
REOS:	END on EOS Received bit, AUXRA[2]w
NLEE:	New Line End Enable, IMR0[5]w

Bit	Mnemonic	Description
2r	SPAS	Serial Poll Active State bit
2w	SPAS IE	Serial Poll Active State Interrupt Enable bit

The SPAS bit indicates that the NAT4882 has requested service and has been serial polled. It is set on the false transition of STRS when the serial poll status byte is sent.

SPAS is set by:

[STRS & SPAS & APRS] becoming false

SPAS is cleared by:

swrst + (read ISR0)

Notes

swrst:	software reset Auxiliary Command issued
STRS:	GPIB Source Transfer State
SPAS:	GPIB Serial Poll Active State
APRS:	GPIB Affirmative Poll Response State
read ISR0:	Read the Interrupt Status Register 0

1r	RLC	Remote/Local Change bit
1w	RLC IE	Remote/Local Change Interrupt Enable bit

RLC is set on any change in the REM bit, ADSR[7]r.

RLC is set by:

LOCS -> REMS + REMS -> LOCS +
LWLS -> RWLS + RWLS -> LWLS

RLC is cleared by:

swrst + (read ISR0)

Notes

swrst:	software reset Auxiliary Command issued
LOCS:	GPIB Local State
REMS:	GPIB Remote State
LWLS:	GPIB Local with Lockout State
RWLS:	GPIB Remote with Lockout State
read ISR0:	Read the Interrupt Status Register 0

Bit	Mnemonic	Description
0r	MAC	My Address Change bit
0w	MAC IE	My Address Change Interrupt Enable bit

The MAC bit indicates that a command has been received from the GPIB that has changed the addressed state of the NAT4882. It does not occur if secondary addressing is being used, nor does it indicate that the NAT4882 has been readdressed on its other primary address.

MAC is set by:

ACDS & (MTA & ~TADS & ~APTIE+ OTA & TADS
+ MLA & ~LADS & ~APTIE + UNL & LADS)

MAC is cleared by:

swrst + (read ISR0)

Notes

swrst:	software reset Auxiliary Command issued
ACDS:	GPIB Accept Data State
MTA:	GPIB My Talk Address
TADS:	GPIB Talker Active State
OTA:	GPIB Other Talk Address
MLA:	GPIB My Listen Address
LADS:	GPIB Listen Active State
UNL:	GPIB Unlisten Message
read ISR0:	Read the Interrupt Status Register 0

Interrupt Status Register 1 (ISR1)

Access: location 1 (if Swap* is unasserted) or location 7 (if Swap* is asserted)
(not affected by a page-in auxiliary command)

Mode: TMS9914A

Attributes: Read-Only
Bits are cleared when read

Interrupt Mask Register 1 (IMR1)

Access: location 1 (if Swap* is unasserted) or location 7 (if Swap* is asserted)
(not affected by a page-in auxiliary command)

Mode: TMS9914A

Attributes: Write-Only

7	6	5	4	3	2	1	0	R
GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	
GET IE	ERR IE	UNC IE	APT IE	DCAS IE	MA IE	SRQ IE	IFC IE	
								W

The Interrupt Status Register 1 (ISR1) consists of eight Interrupt Status bits. The Interrupt Mask Register 1 (IMR1) consists of eight Interrupt Enable bits. If the Interrupt Enable bit is true when the corresponding status condition or event occurs, an interrupt request is generated. Bits in ISR1 are set and cleared regardless of the status of the bits in IMR1. If a condition occurs that requires the NAT4882 to set or clear a bit or bits in ISR1 while ISR1 is being read, the NAT4882 holds off setting or clearing the bit or bits until the read is finished. The interrupts GET, UNC, APT, DCAS, and MA are all set in response to commands received over the bus and if unmasked, a Data Accepted (DAC) Holdoff occurs when the interrupt is set.

Bit	Mnemonic	Description
7r	GET	Group Execute Trigger bit
7w	GET IE	Group Execute Trigger Interrupt Enable bit

The GET bit indicates that the GPIB Group Execute Trigger (GET) command was received while the NAT4882 was a GPIB Listener (the NAT4882 has been in DTAS). A DAC Holdoff occurs if the interrupt is unmasked when the interrupt condition occurs. The TRIG pin goes high when this command is received and remains high until the DAC Holdoff is released. If the interrupt is masked, the TRIG pin asserts for one clock pulse.

Bit	Mnemonic	Description

GET is set by:

GET & LADS & ACDS

GET is cleared by:

swrst + (read ISR1)

Notes

GET:	GPIB Group Execute Trigger Message
LADS:	GPIB Listener Active State
ACDS:	GPIB Acceptor Ready State
swrst:	software reset Auxiliary Command issued
read ISR1:	Read the Interrupt Status Register 1

6r ERR Error bit
6w ERR IE Error Interrupt Enable bit

The ERR bit is set when the Source Handshake becomes active (enters SDYS) and finds that NDAC and NRFD lines are both unasserted on the GPIB. This indicates that there are no acceptors on the GPIB.

ERR is set by:

SDYS & EXTDAC & RFD

ERR is cleared by:

swrst + (read ISR1)

Notes

swrst:	software reset Auxiliary Command issued
TACS:	GPIB Talker Active State
SDYS:	GPIB Source Delay State
EXTDAC:	GPIB Data Accepted message asserted by a device other than the NAT4882 Acceptor Handshake
RFD:	GPIB Ready For Data message
read ISR1:	Read the Interrupt Status Register 1

5r UNC Unrecognized Command bit
5w UNC IE Unrecognized Command Interrupt Enable bit

The UNC bit flags the occurrence of a GPIB command not recognized by the NAT4882 and all GPIB secondary commands following the Pass Through Next Secondary auxiliary command. Any GPIB command message not decoded by the NAT4882 is treated as an undefined command. However, any addressed command is automatically ignored when the NAT4882 is not addressed. The UNC can also flag the occurrence of a GPIB

Bit **Mnemonic** **Description**

command (or group of commands) specified by the AUXRE[3-2]w or AUXRF[3-0]w bits.

If UNC IE is set, a DAC Holdoff occurs when an unrecognized command is received. You can then read undefined commands using the Command Pass Through Register (CPTR). The DAC Holdoff is released when the Release DAC Holdoff auxiliary command is issued.

UNC is set by:

ACDS & UCG & ~(LLO + SPE + SPD + DCL + PPU & PP1)
+ ACDS & ACG & ~(GET + GTL + SDC + TCT + PPC & PP1) & LADS
+ TCT & TADS & ACDS & ~ATCT
+ SCG & PTS & ACDS
+ DHADT & GET & ACDS
+ DHADC & (SDC + DCL) & ACDS
+ DHATA & TAG & ~UNT & ACDS
+ DHALA & LAG & ~UNL & ACDS
+ DHUNTL & (UNT + UNL) & ACDS
+ DHALL & (UCG + ACG + SCG) & ACDS

UNC is cleared by:

swsrt + (read ISR1)

Notes

UCG:	GPIB Universal Command Group message
ACG:	GPIB Addressed Command Group message
LLO:	GPIB Local Lock Out message
SPE:	GPIB Serial Poll Enable message
SPD:	GPIB Serial Poll Disable message
DCL:	GPIB Device Clear message
GET:	GPIB Group Execute Trigger message
GTL:	GPIB Go To Local message
SDC:	GPIB Selected Device Clear message
TCT:	GPIB Take Control message
PTS:	Pass Through Next Secondary local message
UNT:	GPIB Untalk message
UNL:	GPIB Unlisten message
TADS:	GPIB Talker Addressed State
LADS:	GPIB Listener Addressed State
ACDS:	GPIB Accept Data State
DHADT:	AUXRE[3]w
DHADC:	AUXRE[2]w
DHATA:	AUXRF[3]w
DHALA:	AUXRF[2]w
DHUNTL:	AUXRF[1]w
DHALL:	AUXRF[0]w
SCG:	GPIB Secondary Command Group message

Bit	Mnemonic	Description
		swrst: software reset Auxiliary Command issued TAG: GPIB Talk Address Group message LAG: GPIB Listen Address Group message read ISR1: Read the Interrupt Status Register 1
4r	APT	Address Pass Through
4w	APT IE	Address Pass Through Interrupt Enable

Unmasking APT enables secondary addressing. The APT bit is set when a secondary command is received if the last primary command received was a primary talk or listen address of the NAT4882, indicating that a secondary GPIB address has been received and is available in the CPTR for inspection.

Note: The application program must check this bit when using secondary addressing.

When APT and APT IE are set, the Data Accepted (DAC) message is held and the GPIB Handshake stops until either the Valid or Non-Valid auxiliary command is issued. The secondary address can be read from the CPTR.

APT is set by:

(TPAS + LPAS) & SCG & ACDS

APT is cleared by:

swrst + (read ISR1)

Notes

TPAS: GPIB Talker Primary Addressed State
LPAS: GPIB Listener Primary Addressed State
SCG: GPIB Secondary Command Group
ACDS: GPIB Accept Data State
swrst: software reset Auxiliary Command issued
read ISR1: Read the Interrupt Status Register 1

3r	DCAS	Device Clear Active State bit
3w	DCAS IE	Device Clear Active State Interrupt Enable bit

The DCAS bit indicates that the GPIB Device Clear (DCL) command has been received or that the GPIB Selected Device Clear (SDC) command has been received while the NAT4882 was a GPIB Listener (the NAT4882 is in DCAS). A DAC Holdoff occurs if the interrupt is unmasked when the interrupt condition occurs.

Bit	Mnemonic	Description

DCAS is set by:

ACDS & (DCL + SDC & LADS)

DEC is cleared by:

swrst + (read ISR1)

Notes

LADS:	GPIB Listener Primary Addressed State
DCL:	GPIB Device Clear Message
SDC:	GPIB Selected Device Clear Message
ACDS:	GPIB Accept Data State
swrst:	software reset Auxiliary Command issued
read ISR1:	Read the Interrupt Status Register 1

2r MA — My Address bit
2w MA IE — My Address Interrupt Enable bit

MA is set when the NAT4882 recognizes its primary talk or listen address. A DAC Holdoff occurs, if MA IE is set.

MA is set by:

(MLA + MTA) & ACDS & ~SPMS & ~APT IE

MA is cleared by:

swrst + (read ISR1)

Notes

SPMS:	GPIB Serial Poll Mode State
MLA:	GPIB My Listen Address Message
MTA:	GPIB My Talk Address Message
ACDS:	GPIB Accept Data State
APT IE:	Address Pass Through Interrupt Enable, IMR1[4]w
swrst:	software reset Auxiliary Command issued
read ISR1:	Read the Interrupt Status Register 1

1r SRQI — Service Request Input bit
1w SRQI IE — Service Request Input Interrupt Enable bit

The SRQI bit indicates that a GPIB Service Request (SRQ) message has been received while the NAT4882 Controller function is active (CIC). The Controller should execute a serial poll in response to this interrupt.

Bit	Mnemonic	Description
		SRQI is set by: SRQ & ~(CIDS + CADS). SRQI is cleared by: swrst + (read ISR1) **Notes** CIDS: GPIB Controller Idle State CADS: GPIB Controller Addressed State SRQ: GPIB Service Request message swrst: software reset Auxiliary Command issued read ISR1: Read Interrupt Status Register 1
0r	IFC	Interface Clear bit
0w	IFC IE	Interface Clear Interrupt Enable bit IFC is set on the assertion of IFC when the interface is not in SACS (that is, not System Controller). IFC is set by: (IFC & ~SACS) becoming true IFC is cleared by: swrst + (read ISR1) **Notes** IFC: GPIB Interface Clear Signal SACS: GPIB System Control Active State swrst: software reset Auxiliary Command issued read ISR1: Read Interrupt Status Register 1

Address Status Register (ADSR)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(not affected by a page-in auxiliary command)

Mode: TMS9914A

Attributes: Read-Only

7	6	5	4	3	2	1	0 R
REM	LLO	ATN	LPAS	TPAS	LA	TA	ulpa

The Address Status Register (ADSR) contains information that can be used to monitor the NAT4882 GPIB address status.

Bit	Mnemonic	Description
7r	REM	Remote bit This bit is true when the NAT4882 GPIB RL function is in either Remote State (REMS) or Remote With Lockout State (RWLS). The NAT4882 RL function transfers to one of these states when the System Controller has asserted the Remote Enable line (REN), and the CIC addresses the NAT4882 as a Listener.
6r	LLO	Local Lockout bit LLO is used, along with the REM bit, to indicate the status of the NAT4882 GPIB Remote/Local (RL) function. If set, the LLO bit indicates that the NAT4882 is in Local With Lockout State (LWLS) or Remote With Lockout State (RWLS).
5r	ATN	Attention bit ATN is a Status bit that indicates the current level of the GPIB ATN signal. If ATN = 1, the GPIB ATN signal is asserted.
4r	LPAS	Listener Primary Addressed State bit LPAS is used when the NAT4882 is configured for secondary addressing (APT IE is set) and when set, indicates that the NAT4882 has received its primary GPIB listen address. In secondary addressing mode, LPAS = 1 indicates that the secondary address being received on the next GPIB command may represent the NAT4882 secondary GPIB listen address. LPAS is cleared upon receiving a primary command that is not the TLC primary listen address, by pon, or by issuing the Chip Reset auxiliary command.

Bit	Mnemonic	Description
3r	TPAS	Talker Primary Addressed State bit TPAS is used when the NAT4882 is configured for secondary addressing (APT IE is set) and when set, indicates that the NAT4882 has received its primary GPIB talk address. In secondary addressing mode, TPAS = 1 indicates that the secondary address being received on the next GPIB command may represent the NAT4882 secondary GPIB talk address. TPAS is cleared upon receiving a Primary Command other than its primary talk address, by pon, or by issuing the Chip Reset auxiliary command.
2r	LA	Listener Active bit LA is set when the NAT4882 has been addressed or programmed as a GPIB Listener–that is, when the NAT4882 is in the Listener Active State (LACS) or the Listener Addressed State (LADS). The NAT4882 can be addressed to listen either by sending its own listen or extended listen address while it is CIC and the LWC bit is set or by receiving its listen address from another CIC. It can also be programmed to listen using the Listen Only auxiliary command. If the NAT4882 is addressed to listen, it is automatically unaddressed to talk. LA is cleared by pon, issuing the Chip Reset auxiliary command, issuing the Unlisten Auxiliary command, receiving the GPIB UNL message, being addressed to Talk, or the asserting of the GPIB IFC signal.
1r	TA	Talker Active bit TA is set when the NAT4882 has been addressed or programmed as the GPIB Talker–that is, when the NAT4882 is in the Talker Active State (TACS), the Talker Addressed State (TADS), or the Serial Poll Active State (SPAS). The NAT4882 can be addressed to talk either by sending its own talk or extended talk address while it is CIC and the LWC bit is set or by receiving its talk address from another CIC. It can also be programmed to talk using the Talk Only auxiliary command. If the NAT4882 is addressed to talk, it is automatically unaddressed to listen. TA is cleared by pon, by issuing the Chip Reset auxiliary command, issuing the Untalk Auxiliary command, receiving a GPIB OTA message, being addressed to Listen, or the assertion of the GPIB IFC signal.

Bit	Mnemonic	Description
0r	ulpa	Upper/ Lower Primary Address bit The ulpa bit indicates to which primary address the information in the ADSR bits applies. The ulpa bit shows the LSB of the last primary address recognized by the NAT4882. **Note:** Only one Talker or Listener may be active at any one time; thus, the ulpa bit indicates which, if either, of the NAT4882 Talker and Listener functions is addressed or active. The ulpa bit is cleared by issuing the Chip Reset auxiliary command.

Interrupt Mask Register 2 (IMR2)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(after the page-in Interrupt Mask 2 auxiliary command)

Mode: TMS9914A

Attributes: Write-Only

7	6	5	4	3	2	1	0
GLINT	STBO IE	NLEE	BTO	LLOC IE	ATNI IE	TO IE	CIC IE
							W

The Interrupt Mask Register 2 (IMR2) consists of six Interrupt Enable bits and two Internal Control bits. If the Interrupt Enable bit is true when the corresponding status condition or event occurs, an interrupt request is generated. Bits in ISR2 are set and cleared regardless of the status of the bits in IMR2. A hardware reset clears all bits in IMR2 except GLINT, which a hardware reset sets.

Bit	Mnemonic	Description
7w	GLINT	Global Interrupt Enable This bit supplies a Global Interrupt Enable. If this bit is cleared, the TLC does not generate an interrupt regardless of the state of the ISR bits and IMR bits. If this bit is set, the TLC can generate interrupts. A hardware reset sets this bit.
6w	STBO IE	Status Byte Out Interrupt Enable bit When STBO IE is set, STBO (in ISR2) is set upon entering SPAS and causes an interrupt. The control program should write the current STB to the SPMR, which will be transmitted to the GPIB as the STB. Writing the SPMR clears STBO, which is set when it enters SPAS during the next serial poll. When STBO IE is set, the rsv bit in the SPMR has no effect on the SR function. rsv must be generated via the reqt auxiliary command.
5w	NLEE	New Line End Enable bit If NLEE = 1, the NAT4882 treats the 7-bit ASCII new line character (0A hex) as an EOS character. The Acceptor Handshake function responds to the acceptance of a new line character as if EOI was sent.
4w	BTO	Byte Timeout bit Setting BTO enables byte timeouts. For more information on the function of Byte Timeouts, see *Auxiliary Register J (AUXRJ)* later in this chapter.

Bit	Mnemonic	Description
3w	LLOC IE	Local Lockout Change Interrupt Enable bit By setting LLOC IE, the NAT4882 can generate an interrupt when the LLOC bit in ISR2 is set. For more information on the setting of LLOC, refer to the *Interrupt Status Register 2 (ISR2)* description earlier in this chapter.
2w	ATNI IE	ATN Interrupt Enable bit By setting ATNI IE, the NAT4882 can generate an interrupt when ATN is asserted.
1w	TO IE	Timeout Interrupt Enable bit TO reflects the status of the timer. Once started, the timer sets the timeout status bit after the amount of time specified in the Timer Register has elapsed (see *Auxiliary Register J* later in this chapter). An interrupt is generated when TO IE and TO are set. TO is cleared when the Timer Register is written.
0w	CIC IE	Controller-In-Charge Interrupt Enable bit Setting CIC IE enables the NAT4882 to generate an interrupt when the interface is CIC. This bit is used along with the ATCT bit (in ACCRB) to indicate when control has been passed to the NAT4882.

End of String Register (EOSR)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(after the page-in EOSR auxiliary command)

Mode: TMS9914A

Attributes: Write-Only

7	6	5	4	3	2	1	0
EOS7	EOS6	EOS5	EOS4	EOS3	EOS2	EOS1	EOS0
							W

The End Of String Register (EOSR) holds the byte that the NAT4882 uses to detect the end of a GPIB data block transfer. A 7- or 8-bit byte (ASCII or binary) can be placed in the EOSR to be used in detecting the end of a block of data. The length of the EOS byte to be used in the comparison is selected by the BIN bit in Auxiliary Register A, ACCRA[4]w.

If the NAT4882 is a Listener and bit REOS of ACCRA is set, the END bit is set in ISR0 whenever the byte in the DIR matches the EOSR. If the NAT4882 is a Talker and the data is being transmitted, and bit XEOS of ACCRA is set, the END message (GPIB EOI* line asserted low) is sent along with the data byte whenever the contents of the DOR matches the EOSR.

Bit	Mnemonic	Description
7-0w	EOS[7-0]	End of String bits 7 through 0

Bus Control Register (BCR)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(after the page-in BCS auxiliary command)

Mode: TMS9914A

Attributes: Write-Only

Writing ones to bits in the Bus Control Register (BCR) asserts the corresponding GPIB control lines. The order of the bits in the BCR are shown below:

7	6	5	4	3	2	1	0
ATN_C	DAV_C	NDAC_C	NRFD_C	EOI_C	SRQ_C	IFC_C	REN_C

W

Because the chip is either transmitting or receiving a GPIB control line at any particular time, and not doing both simultaneously setting a bit in the BCR may not automatically assert the corresponding line on the GPIB. If the chip is transmitting a GPIB line when the corresponding bit in the BCR is set, the chip asserts the GPIB line. If the chip is receiving a GPIB line when the corresponding bit in the BCR is set, the GPIB line is not asserted. However, in both these cases, the GPIB signal internal to the interface chip is logically ORed with the value of the BCR bit. Figure 2-6 illustrates the GPIB input/output hardware configuration.

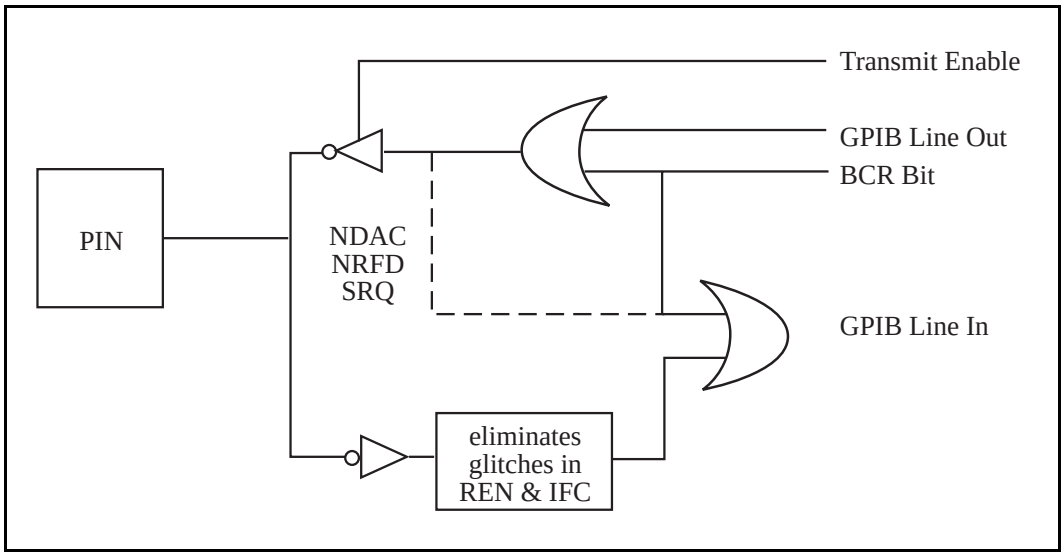


Figure 2-6. GPIB I/O Hardware Configuration for TMS9914A Mode

Transmit Enable represents the internal signal that is true when the chip is driving a particular GPIB control line. *GPIB Line Out* represents the internal signal that is true when an interface function within the chip is attempting to assert a GPIB control signal. *BCR bit* corresponds to the bit in the Bus Control Register. *GPIB Line In* represents the internal GPIB lines that are inputs to

the GPIB interface functions and the Bus Status Register. The internal signals *SRQ*, *NDAC*, and *NRFD* are monitored by the interface functions even when they are not driven onto the pin. For this reason, the internal value of these signals is ORed with the external value.

Bit	Mnemonic	Description
7w	ATN_C	GPIB Attention Control bit
6w	DAV_C	GPIB Data Valid Control bit
5w	NDAC_C	GPIB Not Data Accepted Control bit
4w	NRFD_C	GPIB Not Ready For Data Control bit
3w	EOI_C	GPIB End Or Identify Control bit
2w	SRQ_C	GPIB Service Request Control bit
1w	IFC_C	GPIB Interface Clear Control bit
0w	REN_C	GPIB Remote Enable Control bit

Hidden Registers

The hidden registers are loaded through the Accessory Register (ACCR). ACCR[7-5] or ACCR[7-4] is loaded with the hidden register number, and ACCR[4-0] or ACCR[3-0] is loaded with the data to be transferred to the hidden register. The hidden registers cannot be read. All hidden registers are cleared by a Chip Reset auxiliary command or a hard reset.

Accessory Register A (ACCRA)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(after the page-in Accessory Register auxiliary command)

Mode: TMS9914A

Control Code: 100 (Binary, bits 7-5)

Attributes: Write-Only
Accessed through the ACCR

4	3	2	1	0
BIN	XEOS	REOS	0	0
				W

Writing to Accessory Register A (ACCRA) is done via the ACCR. Writing the binary value 100 into the Control Code (CNT[2-0]) and a bit pattern into the Command Code (COM[4-0]) portion of the ACCR causes the Command Code to be written to Accessory Register A. When the data is written to ACCRA, the bits are denoted by the mnemonics shown in the above register. This 5-bit code controls the transmission and reception of EOS/END. ACCRA is cleared by a chip reset or a hardware reset.

Bit	Mnemonic	Description
4w	BIN	Binary bit The BIN bit selects the length of the EOS message. If BIN = 1, the End Of String Register (EOSR) is treated as a full 8-bit byte. If BIN = 0, the EOSR is treated as a 7-bit register (for ASCII characters) and only a 7-bit comparison is done with the data on the GPIB.
3w	XEOS	Transmit END with EOS bit The XEOS bit permits or prohibits automatic transmission of the GPIB END message at the same time as the EOS message when the TLC is in Talker Active State (TACS). If XEOS is set and the byte in the CDOR matches the contents of the EOSR, the EOI line is sent true along with the data.

Bit	Mnemonic	Description
2w	REOS	END on EOS Received bit The REOS bit permits or prohibits setting the END bit (ISR0[3]r) upon receiving the EOS message when the TLC is in Listener Active State (LACS). If REOS is set and the byte in the DIR matches the byte in the EOSR, the END bit (ISR1[4]r) is set and the EOS character is treated by the Acceptor Handshake function just as if it were received with EOI asserted.
1-0w	0	Reserved bits Must be written with zeros.

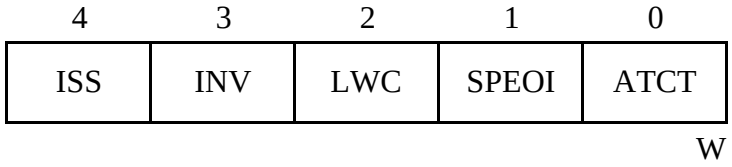
Accessory Register B (ACCRB)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(after the page-in Accessory Register auxiliary command)

Mode: TMS9914A

Control Code: 101 (Binary, bits 7-5)

Attributes: Write-Only
Accessed through the ACCR



Writing to Accessory Register B (ACCRB) is done via the ACCR. Writing the value 101 into the Control Code (CNT[2-0]) and a bit pattern into the Command Code portion (COM[4-0]) of the ACCR causes the Command Code to be written to ACCRB. When the data is written to ACCRB, the bits are denoted as shown in the figure above. This 5-bit code affects several interface functions, as described in the following paragraphs. ACCRB is cleared by a chip reset or a hardware reset.

Bit	Mnemonic	Description
4w	ISS	Individual Status Select bit The ISS bit determines the value of the NAT4882 ist local message. When ISS = 1, ist takes on the value as the NAT4882 Service Request State (SRQS). (The NAT4882 is asserting the GPIB SRQ message when it is in SRQS.) When ISS = 0, ist takes on the value of the NAT4882 Parallel Poll Flag. The Parallel Poll Flag is set and cleared using the Set Parallel Poll Flag and Clear Parallel Poll Flag auxiliary commands.
3w	INV	Invert bit The INV bit affects the polarity of the NAT4882 INT pin. Setting INV causes the polarity of the Interrupt (INT) pin on the NAT4882 to be active low. INV = 0 : INT pin is active high INV = 1 : INT pin is active low
2w	LWC	Listen When Controller bit If LWC is clear, the NAT4882 does not accept command bytes that it sources when Controller-In-Charge. However, if LWC is set, the NAT4882 automatically accepts commands that it sources when

Bit	Mnemonic	Description
		Controller-In-Charge. This setting allows the NAT4882 to respond to GPIB commands that it sources, such as primary addresses, when it is in 9914A mode.
1w	SPEOI	Send Serial Poll EOI bit The SPEOI bit permits or prohibits the transmission of the END message in Serial Poll Active State (SPAS). If SPEOI = 1, EOI is sent true when the NAT4882 is in SPAS and is sourcing an STB. Otherwise, EOI is sent false in SPAS.
0w	ATCT	Automatic Take Control bit By setting ATCT, the interface can automatically take control when passed by another Controller. The Acceptor Handshake function does not perform a DAC Holdoff upon receiving a TCT command. Use the CIC bit in ISR2 to determine when the interface has received control. The CIC IE bit of IMR2 can be used to generate an interrupt upon accepting control.

Accessory Register E (ACCRE)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(after the page-in Accessory Register auxiliary command)

Mode: TMS9914A

Control Code: 1100 (Binary, bits 7-4)

Attributes: Write-Only
Accessed through the ACCR

3	2	1	0
DHADT	DHADC	0	0
			W

Writing to Accessory Register E (ACCRE) is done via the ACCR. Writing the binary value 1100 into the Data Lines 7 through 4 and a bit pattern into the lower four bits of the ACCR (COM[3-0]) causes the four lowest order bits to be written to ACCRE. The 4-bit code determines how the NAT4882 uses DAC Holdoff. ACCRE is cleared by a chip reset or a hardware reset.

Bit	Mnemonic	Description
3w	DHADT	DAC Holdoff on GET bit Setting DHADT enables DAC Holdoff when the Acceptor Handshake function receives the GET command. When this occurs, the CPT bit in ISR1 is set. Clearing DHADT disables DAC Holdoff on GET. Issuing the Valid or the Nonvalid auxiliary command releases the Holdoff. With this feature, you can be notified via a CPT interrupt that GET was sent regardless of the status of the Listener function.
2w	DHADC	DAC Holdoff on DCL or SDC bit Setting DHADC enables DAC Holdoff when the Acceptor Handshake function receives the DCL or SDC command. When this occurs the CPT bit in ISR1 is set. Clearing DHADC disables DAC Holdoff on DCL or SDC. Issuing the Valid or the Nonvalid auxiliary command releases the Holdoff. With this feature, you can be notified via a CPT interrupt that DCL or SDC was sent regardless of the status of the Listener function.
1-0w	0	Reserved bits These bits must be written with zeros.

Accessory Register F (ACCRF)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(after the page-in Accessory Register auxiliary command)

Mode: TMS9914A

Control Code: 1101 (Binary, bits 7-4)

Attributes: Write-Only
Accessed through the ACCR

3	2	1	0
DHATA	DHALA	DHUNTL	DHALL
			W

Writing to Accessory Register F (ACCRF) is done via the ACCR. Writing the binary value 1101 into the Data Lines 7 through 4 and a bit pattern into the lower four bits of the ACCR (COM[3-0]) causes the four lowest order bits to be written to ACCRF. The four-bit code determines how the NAT4882 uses DAC Holdoff. ACCRF is cleared by a chip reset or a hardware reset.

Bit	**Mnemonic**	**Description**
3w	DHATA	Setting DHATA enables DAC Holdoff when the Acceptor Handshake function receives any primary Talker Address. When this occurs, the CPT bit in ISR1 is set. Clearing DHATA disables DAC Holdoff on primary Talker Addresses. Issuing the Valid or the Nonvalid auxiliary command releases the Holdoff. With this feature, you can be notified via a CPT interrupt that a primary Talker Address was issued.
2w	DHALA	DAC Holdoff on All Listener Addresses Setting DHALA enables DAC Holdoff when the Acceptor Handshake function receives any primary Listener Address. When this occurs, the CPT bit in ISR1 is set. Clearing DHALA disables DAC Holdoff on primary Listener Addresses. Issuing the Valid or the Nonvalid auxiliary command releases the Holdoff. With this feature you can be notified via a CPT interrupt that a primary Listener Address was issued.
1w	DHUNTL	DAC Holdoff on the UNT or UNL Command Setting DHUNTL enables DAC Holdoff when the Acceptor Handshake function receives the UNT or UNL command. When this occurs, the CPT bit in ISR1 is set. Clearing DHUNTL disables DAC Holdoff on UNT and UNL. Issuing the Valid or the Nonvalid auxiliary command releases the Holdoff. With this feature, you can be notified via a CPT interrupt that UNT or UNL was issued.

Bit	Mnemonic	Description
0w	DHALL	DAC Holdoff on All UCG, ACG, and SCG Commands Setting DHALL enables DAC Holdoff when the Acceptor Handshake function receives any UCG, ACG, or SCG command. When this occurs, the CPT bit in ISR1 is set. Clearing DHALL disables DAC Holdoff on any UCG, ACG, or SCG command. Issuing the Valid or the Nonvalid auxiliary command releases the Holdoff. With this feature, you can be notified via a CPT interrupt that a UCG, ACG, or SCG command was issued.

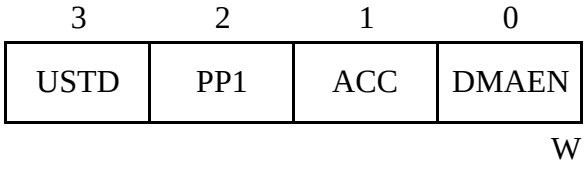
Accessory Register I (ACCRI)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(after the page-in Accessory Register auxiliary command)

Mode: TMS9914A

Control Code: 1110 (Binary, bits 7-4)

Attributes: Write-Only
Accessed through the ACCR



Writing to Accessory Register I (ACCRI) is done via the ACCR. Writing the binary value 1110 into the Data Lines 7 through 4 and a bit pattern into the lower four bits of the ACCR (COM[3-0]) causes the four lowest order bits to be written to ACCRI. ACCRI is cleared by a chip reset or a hardware reset.

Bit	Mnemonic	Description
3w	USTD	Ultra Short T1 Delay Setting this bit sets the T1 delay that the Source Handshake function uses for data bytes subsequent to the first data byte after ATN is unasserted to 350 nsec. If this bit is cleared, the value of T1 is determined by stdl and vstdl.
2w	PP1	Parallel Poll 1 The PP1 bit permits or prohibits the ability to respond to remote Parallel Poll configuration automatically. If PP1 is set, the interface may be configured remotely for Parallel Polls. The Acceptor Handshake does not perform a DAC Holdoff and set the UNC bit upon receiving a Parallel Poll Command (PPC or PPU). If PP1 is cleared, Parallel Polls must be configured via the PPR and Parallel Poll Commands must be monitored by the UNC bit.
1w	ACC	Automatic Carry Cycle Setting ACC enables automatic carry cycles on GPIB DMA transfers. When this bit is set during GPIB DMA reads, the Acceptor Handshake function performs an RFD Holdoff on the lastbyte read by the DMA Controller (that is, on the byte in which the T/C signal is pulsed during the read). Issuing the Finish Handshake auxiliary command releases the Holdoff. If this bit is set during GPIB DMA writes, the Source Handshake function

Bit	Mnemonic	Description
		issues EOI with the last byte written to the CDOR by the DMA Controller (that is, the byte in which the T/C signal is pulsed when written). **Note:** When you use the NAT4882 with the Turbo488, do not set this bit, because the Turbo488 handles Carry Cycles automatically and the T/C pin is normally grounded.
0w	DMAEN	DMA Enable bit The DMAEN bit changes the way the DRQ pin is asserted in 9914 mode. If DMAEN is cleared, the DRQ pin asserts if the interface receives a data byte or TACS & SGNS & ~cdba. The DRQ pin unasserts if either the DIR is read or DOR is written. If DMAEN is set, the DMAI and DMAO bits in the ISR0 become active. The DRQ pin asserts on the set BI condition and unasserts upon reading DIR or pon. The DRQ pin asserts if DMAO = 1 and (TACS & SGNS & ~cdba).

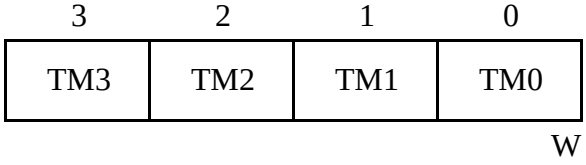
Accessory Register J (ACCRJ)

Access: location 2 (if Swap* is unasserted) or location 4 (if Swap* is asserted)
(after the page-in Accessory Register auxiliary command)

Mode: TMS9914A

Control Code: 1111 (Binary, bits 7-4)

Attributes: Write-Only
Accessed through the ACCR



Writing to Accessory Register J (ACCRJ) is done via the ACCR. Writing the binary value 1111 into the Data Lines 7 through 4 and a bit pattern into the lower four bits of the ACCR (COM[3-0]) causes the four lowest order bits to be written to ACCRJ.

Accessory Register J is a 4-bit register used to set the timeout value of the timer interrupt. The timeout value can be set between the range of 16 µsec to 134 sec when the NAT4882 clock is 20 MHz. The timer is started when the Timer Register is written with a nonzero value and sets the TO bit in ISR2 when the timeout value has expired. The timer is cleared when a zero is written to the Timer Register. For more information on the timer interrupt capability, see *Interrupt Status Register 2* earlier in this chapter.

Bit	Mnemonic	Description
3-0w	TM[3-0]	Timer bits 3 through 0 Table 2-7 lists the approximate timeout values supported by Accessory Register J at 20 MHz. If the NAT4882 uses another clock frequency, the timeout value can be computed with the formula: time = $(2^{factor} * 5)$/frequency.

Table 2-7. Timeout Values in TMS9914A Mode

TM3-0	Timeout Value (> or =)	Factor
0000	Disabled	-
0001	16 µsec	6
0010	32 µsec	7
0011	128 µsec	9
0100	256 µsec	10

(continues)

Bit **Mnemonic** **Description**

Table 2-7. Timeout Values in TMS9914 Mode (continued)

TM3-0	Timeout Value (> or =)	Factor
0101	1 msec	12
0110	4 msec	14
0111	16 msec	16
1000	33 msec	17
1001	131 msec	19
1010	262 msec	20
1011	1 sec	22
1100	4 sec	24
1101	17 sec	26
1110	34 sec	27
1111	134 sec	29

The timer supports two different types of timeouts depending on the value of the BTO bit. If BTO is cleared, the timer operates in global mode. In this mode, the timer starts upon writing a non-zero value to the Timer Register and continues counting until it reaches the timeout value and sets the TO bit.

If BTO is set, the timer operates in Byte Timeout mode. In this mode, the timer starts upon writing a non-zero value to the Timer Register and continues counting until it reaches the timeout value. However, reads of the DIR or writes of the CDOR clear the timer and force it to start counting over. In Byte Timeout mode, if TO is set, it remains set until the Timer Register is written. Further, reads of DIR or writes of CDOR have no effect on TO until the Timer Register is written.

Bus Status Register (BSR)

Access: location 3 (if Swap* is unasserted) or location 5 (if Swap* is asserted)
(not affected by the page-in auxiliary commands)

Mode: TMS9914A

Attributes: Read-Only

7	6	5	4	3	2	1	0 R
ATN_S	DAV_S	NDAC_S	NRFD_S	EOI_S	SRQ_S	IFC_S	REN_S

Reads of the Bus Status Register (BSR) return the status of the GPIB control lines at the time of the read. The IFC_S bit of this register does not indicate the true value if the interface is a System Controller using the *sic* auxiliary command.

Bit	**Mnemonic**	**Description**
7r	ATN_S	GPIB Attention Status bit
6r	DAV_S	GPIB Data Valid Status bit
5r	NDAC_S	GPIB Not Data Accepted Status bit
4r	NRFD_S	GPIB Not Ready For Data Status bit
3r	EOI_S	GPIB End or Identify Status bit
2r	SRQ_S	GPIB Service Request Status bit
1r	IFC_S	GPIB Interface Clear Status bit
0r	REN_S	GPIB Remote Enable Status bit

Because the BSR samples the GPIB control lines from the GPIB transceiver and not the actual GPIB bus, the validity of each bit is determined by the direction of each line. Generally, when a signal is an input, its true bus status is reflected in the BSR, while an output signal only reflects the NAT4882 value of that particular line. Under normal GPIB operation, this function should not be too limiting, because the lines that are typically monitored are valid when they are monitored. For example, the SRQ line is valid in the BSR when the NAT4882 is CIC, which is also when the SRQ line will be monitored.

Auxiliary Command Register (AUXCR)

Access: location 3 (if Swap* is unasserted) or location 5 (if Swap* is asserted)
(not affected by the page-in auxiliary commands)

Mode: TMS9914A

Attributes: Write-Only

7	6	5	4	3	2	1	0
CS	0	0	F4	F3	F2	F1	F0
							W

The AUXCR is used to issue auxiliary commands. There are two basic types of commands implemented in the Auxiliary Command Register: pulsed and static. Static commands are used to enable (set) or disable (clear) the various features of the NAT4882. The particular feature is selected by the code on F[4-0] and it is set or cleared according to the value of the CS bit. The pulsed commands stay active for one clock pulse after the Auxiliary Command Register has been written to.

Note: Writes to the auxiliary Command Register must be spaced at least 200 nsec apart.

Bit	Mnemonic	Description
7w	CS	Clear or Set bit CS is used in most cases when the feature selected by F4 through F0 is of the clear/set type. The feature is enabled if CS is set and disabled if CS is cleared. In other cases, the CS bit is unused and ignored by these commands. All clear/set auxiliary commands are cleared by the hardware reset pin or the Chip Reset auxiliary command, except for swrst, which is set true by reset.
6-5w	0	Reserved bits Write zeros to these bits.
4-0w	F[4-0]	Feature Code bits 4 through 0 These bits specify the feature code of each special function. Table 2-8 is a summary of the implemented special functions. Table 2-9 explains the details of each special function.

Table 2-8. Auxiliary Command Summary

CS Bit	Function Code (F4-F0) 4 3 2 1 0	Mnemonic	Auxiliary Command
0 1	0 0 0 0 0	swrst	Clear Software Reset Set Software Reset
0 1	0 0 0 0 1	dacr	Non-Valid Release DAC Holdoff Valid Release DAC Holdoff
X	0 0 0 1 0	rhdf	Release RFD Holdoff
0 1	0 0 0 1 1	hdfa	Clear Holdoff on All Data Set Holdoff on All Data
0 1	0 0 1 0 0	hdfe	Clear Holdoff on END Only Set Holdoff on END Only
X	0 0 1 0 1	nbaf	New Byte Available False
0 1	0 0 1 1 0	fget	Clear Force Group Execute Trigger Set Force Group Execute Trigger
0 1	0 0 1 1 1	rtl	Clear Return to Local Set Return to Local
X	0 1 0 0 0	feoi	Send EOI with the next byte
0 1	0 1 0 0 1	lon	Clear Listen Only Set Listen Only
0 1	0 1 0 1 0	ton	Clear Talk Only Set Talk Only
X	0 1 0 1 1	gts	Go To Standby
X	0 1 1 0 0	tca	Take Control Asynchronously
X	0 1 1 0 1	tcs	Take Control Synchronously
0 1	0 1 1 1 0	rpp	Clear Request Parallel Poll Set Request Parallel Poll
0 1	0 1 1 1 1	sic	Clear Send Interface Clear Set Send Interface Clear
0 1	1 0 0 0 0	sre	Clear Send Remote Enable Set Send Remote Enable
X	1 0 0 0 1	rqc	Request Control
X	1 0 0 1 0	rlc	Release Control

(continues)

Table 2-8. Auxiliary Command Summary (continued)

CS Bit	Function Code (F4-F0) 4 3 2 1 0	Mnemonic	Auxiliary Command
0 1	1 0 0 1 1	dai	Clear Disable All Interrupts Set Disable All Interrupts
X	1 0 1 0 0	pts	Pass Through Next Secondary
0 1	1 0 1 0 1	stdl	Clear Short T1 Settling Time Set Short T1 Settling Time
0 1	1 0 1 1 0	shdw	Clear Shadow Handshake Set Shadow Handshake
0 1	1 0 1 1 1	vstdl	Clear Very Short T1 Delay Set Very Short T1 Delay
0 1	1 1 0 0 0	rsv2	Clear Request Service bit 2 Set Request Service bit 2
0	1 1 0 0 1	rsvd	Reserved
1	1 1 0 0 1	sw7210†	Switch to µPD7210 Mode
0 1	1 1 0 1 0	reqf† reqt†	Request rsv False (Reqf) Request rsv True (Reqt)
X	1 1 0 1 1	rsvd	Reserved
0	1 1 1 0 0	ch_rst†	Issue a Chip Reset
0 1	1 1 1 0 1	ist†	Clear Parallel Poll Flag Set Parallel Poll Flag
0	1 1 1 1 0	piimr2†	Page-In Interrupt Mask Register 2
1	1 1 1 1 0	pieosr†	Page-In End-Of-String Register
0	1 1 1 1 1	pibcr†	Page-In Bus Control Register
1	1 1 1 1 1	piaccr†	Page-In Accessory Register
1	1 1 1 0 0	clrpi†	Clear Page-In Registers
† Denotes an auxiliary command not available in a standard TMS9914A			

Table 2-9. Auxiliary Command Description

Mnemonic	Description
swrst	Software Reset (0xx00000/1xx00000) This command generates a local swrst message that places the following GPIB interface functions into these idle states: AIDS Acceptor Idle State CIDS Controller Idle State LIDS Listener Idle State LOCS Local State LPIS Listener Primary Idle State NPRS Negative Poll Response State PPIS Parallel Poll Idle State PPSS Parallel Poll Standby State PUCS Parallel Poll to Unaddressed to Configure State SIDS Source Idle State SPIS Serial Poll Idle State TIDS Talker Idle State TPIS Talker Primary Idle State swrst is set by a power-on reset or the chip reset auxiliary command. You should configure the NAT4882 while swrst is set. Configuration includes writing the address of the device into the Address Register, writing mask values into the Interrupt Mask Registers, and selecting the desired features in the Auxiliary Command, Accessory, and Address Registers. When swrst is cleared, the device becomes logically existent on the GPIB.
dacr	Release DAC Holdoff (0xx00001/1xx00001) The Data Accept (DAC) Holdoff allows time for the control program to respond to unrecognized commands, secondary addresses, and device clear commands. The holdoff should be released after any required action has been taken. Normally the command is issued with the CS bit cleared; however, when used with the address pass-through feature, CS is set to indicate that the secondary address was valid or cleared if invalid (see APT interrupt, IMR1[4]w).
rhdf	Release RFD Holdoff (xxx00010) Releases any Ready for Data (RFD) Holdoff caused by *hdfa* or *hlde*.
hdfa	Holdoff on All Data (0xx00011/1xx00011) A Ready For Data (RFD) Holdoff is caused on every data byte until the command is loaded with CS cleared. You must complete the handshake after each byte has been received by issuing the rhdf command.

(continues)

Table 2-9. Auxiliary Command Description (continued)

Mnemonic	Description
hdfe	Holdoff on END Only (0xx00100/1xx00100) A Ready For Data (RFD) Holdoff is caused upon receiving END when hdfe is true. The handshake must be released by issuing the rhdf command.
nbaf	New Byte Available False (xxx00101) If a Talker is interrupted before the byte just stored in the CDOR is sent over the interface, this byte is transmitted as soon as the ATN line returns to the unasserted state. If, as a result of the interrupt, this byte is no longer required, you can suppress transmitting the byte by using the nbaf command.
fget	Force Group Execute Trigger (0xx00110/1xx00110) The Force Group Execute Trigger command generates a high pulse on the TRIG pin. If CS is cleared when fget is issued, the TRIG pin is pulsed high for one clock cycle. If CS is set when fget is issued, the TRIG pin is driven high and remains high until fget is issued with CS cleared. The Trigger command performs the same function as if the GET (Group Execute Trigger) bit (ISR1[5]r) were set. The GET bit is not set by issuing fget.
rtl	Return to Local (0xx00111/1xx00111) The Return to Local command implements the rtl message as defined by IEEE 488. When CS is zero, the message is generated in the form of a pulse. If rtl is already set, this command clears it. When CS is one, the rtl is set and remains set until the rtl command is issued with CS cleared, or chip reset.
feoi	Send EOI with the Next Byte (xxx01000) The Send EOI command causes the GPIB End Or Identify (EOI) line to go true with the next data byte transmitted.
lon	Listen Only (0xx01001/1xx01001) Issuing the lon command with CS set forces the Listener function into the Listener Active state where it remains until the lon command is issued with the CS bit cleared or a GPIB UNL is received.
ton	Talk Only (0xx01010/1xx01010) Issuing the ton command with CS set forces the Talker function into the Talker Active state where it remains until the ton command is issued with the CS bit cleared or a GPIB OTA is received.

(continues)

Table 2-9. Auxiliary Command Description (continued)

Mnemonic	Description
gts	Go To Standby (xxx01011) The Go To Standby command sets the local message gts. When gts is true and the Source Handshake function is in SGNS, the ATN line is set to false, and the Controller enters CSBS.
tcs	Take Control Synchronously (xxx01101) The Take Control Synchronously command sets the local message tcs. This causes control to be taken by the Controller-In-Charge and ATN to be asserted when the AH1 is in ANRS. If the Controller is not a true Listener, the shadow handshaking command must be used to monitor the handshake lines so that the interface is synchronous with the Talker/Listener and only asserts ATN at the end of a byte transfer. This ensures that no data is lost or corrupted.
rpp	Request Parallel Poll (0xx01110/1xx01110) Issuing rpp with CS set, sets the local message Request Parallel Poll (rpp). If this is executed when the Controller-In-Charge is in CACS & SGNS (that is, ATN is asserted), the Controller sends the Parallel Poll command across the GPIB (ATN and EOI asserted). The poll is completed by reading the CPTR to obtain the status bits and sending rpp with CS cleared.
tca	Take Control Asynchronously (xxx01100) The Take Control Asynchronously command pulses the local message tca. When this command is issued, the Controller regains control and asserts the ATN line. The command is executed immediately and can result in data corruption or loss of data if a Talker/Listener is in the process of transferring a byte.
sic	Send Interface Clear (0xx01111/1xx01111) This command sets the local message send interface clear (sic) equal to the value of CS. This command must only be issued if the interface is System Controller. To meet the IEEE 488 requirements, do not set sic equal to zero until IFC has been held true for at least 100 µsec.
sre	Send Remote Enable (0xx10000/1xx10000) This command sets the local message send remote enable (sre) equal to the value in CS. These commands must only be issued if the interface is System Controller. To meet the IEEE 488 requirements, do not set sre equal to one until REN has been held false for at least 100 µsec.

(continues)

Table 2-9. Auxiliary Command Description (continued)

Mnemonic	Description
dai	Disable All Interrupts (0xx10011/1xx10011) Issuing dai disables the interrupt pin (always unasserted). The Interrupt Status Registers and any holdoffs selected in the Interrupt Mask Register are not affected.
pts	Pass Through Next Secondary (xxx10100) This feature can be used to carry out a remote configuration of a Parallel Poll. The Parallel Poll configure command (PPC) is passed through the interface as an unrecognized command when PP1 is cleared. The pts command causes the next byte received by the interface to be passed through the CPTR which sets the UNC bit. The byte in the CPTR is the Parallel Poll Enable (PPE) command, which can be read by the control program and used to determine the Parallel Poll response that should be written to the PPR.
stdl	Set T1 Delay (0xx10101/1xx10101) Issuing stdl with CS set sets stdl, which makes the T1 delay time 1.1 µsec. The T1 delay time is 2 µsec following a power-on reset, chip reset auxiliary command, or the issuing of stdl with CS cleared. The T1 delay can be reduced to less that 1.1 µsec for the second and subsequent data bytes after ATN becomes false by setting vstd1 or the USTD bit.
shdw	Shadow Handshaking (0xx10110/1xx10110) Issuing shdw with CS set enables the Controller-In-Charge to carry out the Listener handshake without participating in a data transfer. The acceptor handshake participates in the data handshake, but does not set BI nor hold off the handshake. The shadow handshake feature allows the tcs command to be synchronized with the Acceptor Not Ready State (ANRS) so that ATN can be re-asserted without causing a loss or corruption of data bytes. The END interrupt can also be received and causes an RFD holdoff to be generated if hlde is set.
vstdl	Very Short T1 Delay (0xx10111/1xx10111) Issuing vstdl with CS set sets vstdl, which reduces the T1 delay time to 500 nsec on the second and subsequent data bytes after ATN is unasserted. Otherwise, the GPIB settling time is determined by stdl. Issuing vstdl with CS = 0 clears vstdl. The T1 delay can be reduced to less than 500 nsec by setting the USTD bit.

(continues)

Table 2-9. Auxiliary Command Description (continued)

Mnemonic	Description
rqc	Request Control (xxx10001) This command forces the Controller function to enter CADS where it waits for ATN to unassert before entering.
rlc	Release Control (xxx10010) This command forces the Controller function to unassert ATN and enter CIDS.
rsv2	Request Service bit 2 (0xx11000/1xx11000) The rsv2 bit performs the same function as the rsv1 bit in the SPMR, but also provides a means of requesting service that is independent of the SPMR. With rsv2, you can make minor updates to the SPMR without affecting the state of service request. rsv2 is cleared when the serial poll status byte is sent to the Controller during a serial poll (that is, SPAS & APRS & STRS).
sw7210	Switch to NEC µPD7210 Mode (1xx11001) Issuing sw7210 switches the NAT4882 into NEC µPD7210 compatibility mode.
reqt reqf	Request rsv True (1xx11010) Request rsv False (0xx11010) These commands are inputs to the IEEE 488.2 Service Request Synchronization circuit. These commands are used to set and clear the local message rsv. If STBO IE = 0, the commands reqt and reqf are not issued immediately, but are issued on the write of the SPMR following the issuing of the reqt or reqf auxiliary command. If STBO IE = 1, the commands are issued immediately.
ch_rst	Chip Reset (0xx11100) The Chip Reset command resets the NAT4882 in the same way as an external reset pulse. The NAT4882 is reset to the following conditions: • The local swrst message is set and the interface functions are placed in their idle states. • All bits of the SPMR are cleared. • The EOS and NL bits are cleared. • All bits of the ACCRA, ACCRB, ACCRE, ACCRF, ACCRI, and ACCRJ are cleared. • The Parallel Poll Flag and RSC local message are cleared. • The ulpa bit is cleared.

(continues)

Table 2-9. Auxiliary Command Description (continued)

Mnemonic	Description
ist	Parallel Poll Flag (0xx11101/1xx11101) This command sets the Parallel Poll Flag to the value of CS. The value of the Parallel Poll Flag is used as the local message ist when bit four of Accessory Register B (ISS) is zero. The value of SRQS is used as the ist local message when ISS = 1. The ist local message is cleared by a chip reset or hardware reset.
piimr2	Page-In Interrupt Mask Register 2 (0xx11110) Issuing piimr2 maps the Interrupt Mask Register 2 to address offset 2. After this command is issued, the IMR2 can be accessed at address offset 2 until a hardware reset, the chip reset auxiliary command is issued, another register is paged into the address offset 2, or the clear page-in auxiliary command is issued.
pieosr	Page-In End-Of-String Register (1xx11110) Issuing pieosr maps the End-Of-String Register to address offset 2. After this command is issued, the EOSR can be accessed at address offset 2 until a hardware reset, the chip reset auxiliary command is issued, another register is paged into the address offset 2, or the clear page-in auxiliary command is issued.
pibcr	Page-In Bus Control Register (0xx11111) Issuing pibcr maps the Bus Control Register to address offset 2. After this command is issued, the BCR can be accessed at address offset 2 until a hardware reset, the chip reset auxiliary command is issued, another register is paged into the address offset 2, or the clear page-in auxiliary command is issued.
piaccr	Page-In Accessory Register (1xx11111) Issuing piaccr maps the Accessory Register to address offset 2. After this command is issued, the ACCR can be accessed at address offset 2 until a hardware reset, the chip reset auxiliary command is issued, another register is paged into the address offset 2, or the clear page-in auxiliary command is issued.
clrpi	Clear Page-In Registers (1xx11100) Issuing clrpi removes the previously paged in Accessory Register from address offset 2. After this command is issued, writes to offset 2 will have no effect until a page-in auxiliary command is issued.

Interrupt Status Register 2 (ISR2)

Access: location 4 (if Swap* is unasserted) or location 3 (if Swap* is asserted)
(after any page-in auxiliary command is issued)

Mode: TMS9914A

Attributes: Read-Only

7	6	5	4	3	2	1	0 R
cdba	STBO	NL	EOS	LLOC	ATNI	TO	CIC

The Interrupt Status Register 2 (ISR2) consists of five Interrupt Status bits and three Internal Status bits. If the Interrupt Enable bit is true when the corresponding status condition or event occurs, an interrupt request is generated. Bits in ISR2 are set and cleared regardless of the status of the bits in IMR2. If a condition occurs that requires the NAT4882 to set or clear an Interrupt Status bit in the ISR2 at the same time the ISR2 is being read, the NAT4882 holds off setting or clearing the bit until the read is finished.

Bit	Mnemonic	Description
7r	cdba	Command/Data Byte Available local message This bit is true when the local variable cdba is true. cdba is set on writes to the CDOR and cleared on entrance to STRS, pon or nbaf.
6r	STBO	Status Byte Out bit STBO is set upon entering SPAS when STBO IE is set, thus causing an interrupt. The control program should write the current STB to the SPMR, which will be transmitted to the GPIB as the STB. Writing the SPMR clears STBO, which is set again when it enters SPAS during the next serial poll. STBO is set by: STBO IE & SPAS STBO is cleared by: swrst + (write SPMR) + ~SPAS **Notes** SPAS: GPIB Serial Poll Active State swrst: Software Reset write SPMR: Write the Serial Poll Mode Register

Bit	Mnemonic	Description
5r	NL	New Line Receive bit NL is set by: LACS & NL & ACDS NL is cleared by: swrst + (LACS & ~NL & ACDS) **Notes** LACS: GPIB Listener Active State NL: seven bit ASCII 'new line' character (hex 0A) ACDS: GPIB Accept Data State swrst: Software Reset
4r	EOS	End-Of-String Character bit EOS is set by: LACS & EOS & REOS & ACDS EOS is cleared by: swrst + (LACS & ~EOS & ACDS) + ~REOS **Notes** LACS: GPIB Listener Active State EOS: GPIB End-Of-String message REOS: End on EOS Received bit, AUXRA[2]w ACDS: GPIB Accept Data State swrst: Software Reset
3r	LLOC	Local Lockout Change Interrupt bit LLOC is set by: any change in LOK LLOC is cleared by: chip_reset + (read ISR0) **Notes** LOK: ADSR[6]r read ISR0: Read the Interrupt Status Register 0 chip_reset: Chip Reset

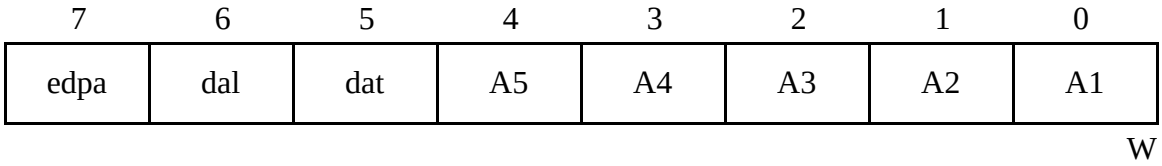
Bit	Mnemonic	Description
2r	ATNI	ATN Interrupt bit ATNI is set by: (ATN) becomes true ATNI is cleared by: chip_reset + read ISR0 **Notes** ATN: GPIB Attention Signal read ISR0: Read the Interrupt Status Register 0 chip_reset: Chip Reset
1r	TO	Time-Out bit TO reflects the status of the timer. Once started, the timer will set the timeout status bit after the amount of time specified in Timer Register has elapsed (see Auxiliary Register J). An interrupt is generated when TO IE and TO are set. TO is cleared when the Timer Register is written.
0r	CIC	Controller-In-Charge Interrupt bit This bit is set if the Controller function is not in CIDS or CADS. If the Controller-In-Charge Interrupt Mask bit is set and CIC = 1, the GPIB chip asserts its interrupt pin. If ATCT=1, this bit may be used to determine when control has been passed to the NAT4882.

Address Register (ADR)

Access: location 4 (if Swap* is unasserted) or location 3 (if Swap* is asserted)
(not affected by the page-in auxiliary commands)

Mode: TMS9914A

Attributes: Write-Only



The Address Register (ADR) is used to load the primary GPIB address of the interface.

Bit	Mnemonic	Description
7w	edpa	Enable Dual Primary Addressing mode bit Setting this bit enables the dual primary addressing mode of the NAT4882. It causes the LSB of the address to be ignored by the address comparator giving two consecutive primary addresses for the device. The address by which the NAT4882 was selected is indicated by the ulpa bit in the ADSR.
6w	dal	Disable Listener bit Setting this bit returns the Listener function to LIDS. The Listener function remains in LIDS even if the chip receives its GPIB listen address or a lon auxiliary command.
5w	dat	Disable Talker bit Setting this bit returns the Talker function to TIDS. The Talker function remains in TIDS even if the chip receives its GPIB talk address or a ton auxiliary command.
4-0w	A[5-1]	TLC GPIB Address bits 5 through 1 These bits specify the five low-order bits of the primary GPIB address that is to be recognized by the TLC. The corresponding GPIB talk address is formed by adding hex 40 to AD[5-1], while the corresponding GPIB listen address is formed by adding hex 20. The value written to AD[5-1] should not be all ones, because the corresponding talk and listen addresses then conflicts with the GPIB Untalk (UNT) and GPIB Unlisten (UNL) commands.

Serial Poll Status Register (SPSR)

Access: location 5 (if Swap* is unasserted) or location 2 (if Swap* is asserted)
(after any page-in auxiliary command is issued)

Mode: TMS9914A

Attributes: Read-Only

Serial Poll Mode Register (SPMR)

Access: location 5 (if Swap* is unasserted) or location 2 (if Swap* is asserted)
(not affected by the page-in auxiliary commands)

Mode: TMS9914A

Attributes: Write-Only

7	6	5	4	3	2	1	0	R
S8	PEND	S6	S5	S4	S3	S2	S1	
S8	rsv/RQS	S6	S5	S4	S3	S2	S1	
								W

Bit	Mnemonic	Description
7r	S8	Serial Poll Status bit 8
7w, 5-0r, 5-0w	S[6-1]	Serial Poll Status bits 6 through 1 Cleared by a hardware reset or by issuing the Chip Reset auxiliary command. These bits send device- or system-dependent status information over the GPIB when the NAT4882 is serial polled. If STBO IE = 0, the NAT4882 is addressed as the GPIB Talker, and the NAT4882 receives the GPIB multiline Serial Poll Enable (SPE) command message, it transmits a byte of status information, SPMR[7-0], to the Controller-In-Charge after the Controller goes to standby and becomes an Active Listener. If STBO IE = 1, the Status byte is not automatically sourced when the Controller goes to standby. Instead, the SPMR must be written with the STB to be sourced in response to an STBO interrupt. The STB written to the SPMR is sourced at the end of the write cycle. These bits are double-buffered and if a write to the register takes place while the device is addressed during a serial poll (SPAS), the value written is saved and these bits are updated when SPAS is terminated.

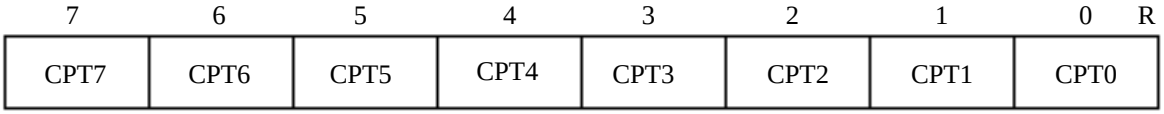
Bit	Mnemonic	Description
6r	PEND	Pending bit PEND is set when rsv is true and cleared when NPRS & ~rsv. It can be used to determine if the interface was polled.
6w	rsv/ RQS	Request Service bit The definition of the rsv1/RQS bit is determined by the STBO IE. If STBO IE = 0, the rsv1/RQS bit is used to generate the GPIB local rsv message. When rsv is set and the GPIB Active Controller is not serial polling the NAT4882, the NAT4882 enters the Service Request State (SRQS) and asserts the GPIB SRQ signal. After the Active Controller reads the STB during the poll, the rsv1 bit must be cleared and set true again to request service a second time. The rsv bit is cleared by a hardware reset, by issuing the Chip Reset auxiliary command, or by writing a zero (0) to it. If STBO IE = 1, the rsv1/RQS bit should be written with the value of the RQS that should be sent along with the STB in response to an STBO IE interrupt.

Command Pass Through Register (CPTR)

Access: location 6 (if Swap* is unasserted) or location 1 (if Swap* is asserted)
(not affected by the page-in auxiliary commands)

Mode: TMS9914A

Attributes: Read-Only



Bit	Mnemonic	Description
7-0r	CPT[7-0]	Command Pass Through bits 7 through 0

With this register, you can inspect the GPIB data lines (DIO(8-1)) directly. It has no storage and should be used when the data lines are known to be in a steady state, such as during a DAC Holdoff or during a Parallel Poll in CPWS. It is used to read unrecognized commands and secondaries, recognized commands that have been programmed following a UNC interrupt, or secondary addresses following an APT interrupt. In addition, an Active Controller uses this register to read the results of a Parallel Poll at least 2 µsec after setting the rpp auxiliary command. Table 2-10 lists the GPIB commands recognized by the NAT4882.

Table 2-10. Multiline GPIB Commands Recognized by the NAT4882 in 9914A Mode

Hex Number	Message	Description
01	GTL	Go To Local
04	SDC*	Selected Device Clear
05	PPC †	Parallel Poll Configure
08	GET*	Group Execute Trigger
09	TCT††	Take Control
11	LLO	Local Lockout
14	DCL	Device Clear
15	PPU†	Parallel Poll Unconfigure
18	SPE	Serial Poll Enable

(continues)

Table 2-10. Multiline GPIB Commands Recognized by the NAT4882 in 9914A Mode (continued)

Hex Number	Message	Description
19	SPD	Serial Poll Disable
20-3E	MLA	My Listen Address
3F	UNL	Unlisten
40-5E	MTA	My Talk Address
5F	UNT	Untalk
60-6F	MSA, PPE	My Secondary Address or Parallel Poll Enable
70-7E	MSA, PPD	My Secondary Address or Parallel Poll Disable

† Parallel Poll commands are treated as defined commands if PP1 is set.

* Defined while in LADS

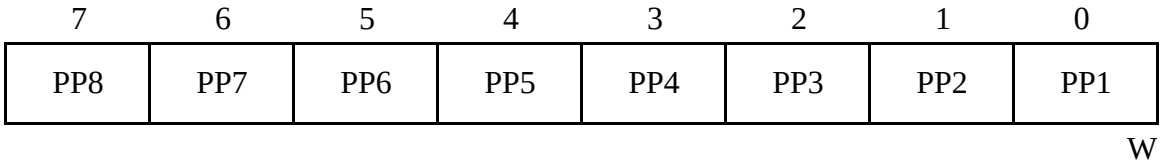
†† Defined if ATCT bit is set

Parallel Poll Register (PPR)

Access: location 6 if Swap* is unasserted or location 1 if Swap* is asserted
(not affected by the page-in auxiliary commands)

Mode: TMS9914A

Attributes: Write-Only



Bit	Mnemonic	Description
7-0w	PP[8-1]	When a Controller initiates a Parallel Poll, the contents of this register are presented to the GPIB data lines. If all bits of the register are cleared, none of the lines (DIO(8-1)) will be asserted during a Parallel Poll that corresponds to the Parallel Poll Idle State (PPIS) of the IEEE 488. If the device is to participate, the bit corresponding to the desired Parallel Poll response should be set. The PPR is double-buffered. If it is written during a Parallel Poll, the new value is held until the Parallel Poll ends, at which point the register is updated. This permits the control program to update the Parallel Poll response completely asynchronously to the GPIB. This register is cleared by a hardware reset and the Chip Reset auxiliary command. It can be loaded while the chip is being configured with swrst set.

Data In Register (DIR)

Access: location 7 (if Swap* is unasserted) or location 0 (if Swap* is asserted)
(not affected by the page-in auxiliary commands)

Mode: TMS9914A

Attributes: Read-Only

7	6	5	4	3	2	1	0 R
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

The Data In Register (DIR) moves data from the GPIB to the computer when the interface is a Listener. Incoming information is latched by this register when (ACDS & ~ATN) which sets the BI bit if shadow handshaking is not enabled. The Not Ready For Data (NRFD) message is asserted until the byte is read from the DIR. The Acceptor Handshake (AH) completes automatically after the byte has been read unless the handshake is in RFD Holdoff because hlda or hlde is set. In that case, the GPIB Handshake is not finished until the Finish Handshake (FH) auxiliary command is issued informing the NAT4882 to release the Holdoff. By using one of the RFD Holdoff modes, the same byte can be read several times or a GPIB Talker can be held off until the program is ready to proceed. The DIR can also be read by asserting the DACK* and RD* pins.

DIO1 is the least significant bit of the data byte and corresponds to GPIB DIO1. DIO8 is the most significant bit of the data byte and corresponds to GPIB DIO8.

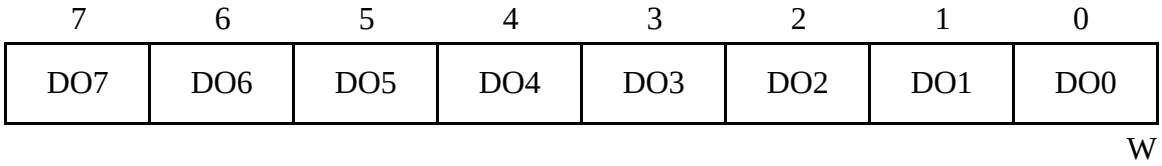
Bit	Mnemonic	Description
7-0r	DIR[7-0]	GPIB Data Lines DIO[8-1]

Data Out Register (DOR)

Access: location 7 (if Swap* is unasserted) or location 0 (if Swap* is asserted)
(not affected by the page-in auxiliary commands)

Mode: TMS9914A

Attributes: Write-Only



The Data Out Register (DOR) moves data from the computer to the GPIB when the interface is the GPIB Talker or the Active Controller. Outgoing data is separately latched by this register and is not destroyed by a read from the DIR. When the interface enters TACS, CACS, or CTRS, the contents of the Data Out Register are presented to the GPIB data lines (DIO(8-1)). The byte is sent over the bus under the control of the Source Handshake. Each time a byte is written to the DOR, the local message cdba is set, allowing the Source Handshake to send the byte. If the handshake is interrupted before the byte can be sent, it will be sent the next time the Source Handshake becomes active unless a new byte available false (nbaf) auxiliary command is issued. This command has the effect of clearing the unsent byte from the DOR, although the register itself is not cleared, and the interface behaves as if it had not been loaded. Each time the Source Handshake becomes active (SGNS) and there is no unsent byte in the Data Out Register (cdba is cleared), the BO bit is set to inform the control program that the DOR is available for use. The DOR is not double-buffered. Its contents are output directly to the data lines of the GPIB. The DOR also latches in data on the rising edge of the WR* signal when DACK* is asserted.

Bit	Mnemonic	Description
7-0w	DO[7-0]	GPIB Data Lines DIO[8-1]

Chapter 3
NAT4882 Programming Considerations

This chapter explains important considerations for programming the NAT4882 in 7210 mode.

The NAT4882 can be programmed in either 7210 mode or 9914 mode, and the programming steps are similar for each mode. This chapter assumes that the NAT4882 is operating in 7210 mode, but the programming considerations can be easily applied to 9914 mode with some modification. For differences between the 7210 and 9914 modes, refer to Chapter 2, *NAT4882 Interface Registers* earlier in this manual.

Initialization

Asserting the RESET* input initializes the NAT4882.

RESET* causes the NAT4882 to do the following:

- Set the local Power On (pon) message and place the interface functions in their idle states (SIDS, AIDS, TIDS, SPIS, TPIS, LIDS, LPIS, NPRS, LOCS, PPIS, PUCS, CIDS, SRIS, SIIS).
- Clear all the bits in the Serial Poll Mode Register (SPMR).
- Clear the End Or Identify (EOI) bit in Address Register 1 (ADR1).
- Clear all the bits of Auxiliary Register A (AUXRA), Auxiliary Register B (AUXRB), Auxiliary Register E (AUXRE), Auxiliary Register F (AUXRF), Auxiliary Register G (AUXRG), Auxiliary Register I (AUXRI), and Auxiliary Register J (AUXRJ).
- Clear the Parallel Poll Flag and Request System Control (rsc) local message.
- Clear the Transmit/Receive Mode 0 (TRM0) and Transmit/Receive Mode 1 (TRM1) bits in the Address Mode Register (ADMR).

All other register contents should be considered undefined while the RESET* line is asserted and after the RESET* line has been deasserted. All NAT4882 registers can be programmed while the NAT4882 internal signal pon is set. When you release or clear pon by issuing an immediate execute pon auxiliary command to the NAT4882, the interface functions are released from the pon state and auxiliary commands can be executed.

A typical programming initialization sequence for the NAT4882 might include the following steps:

1. Place the NAT4882 in a known quiescent state by writing the Chip Reset command to the AUXMR.

2. Set or clear the appropriate Interrupt Enable bits in the Interrupt Mask Register 0 (IMR0), Interrupt Mask Register 1 (IMR1), and the Interrupt Mask Register 2 (IMR2).

3. Load the NAT4882 GPIB address information in the Address Register 0 (ADR0) and the Address Register 1 (ADR1).

4. Enable or disable the GPIB Talker and Listener functions and addressing mode as well as the TRM0 and TRM1 bits using the ADMR.

5. Program the bits in the Auxiliary Mode Register to their desired values. The following are some preferred settings:

   - Set B2 and USTD to enable the very high-speed T1 delay of 350 nsec.

   - Set CHES to enable the clearing of the END detection circuitry on the reception of a data byte without END.

   - Set NTNL to prevent the NAT4882 from sourcing data or commands when there are no Listeners on the GPIB.

   - Set SISB to prevent the interrupt status bits from clearing when they are read.

6. Load the Serial Poll Response in the SPMR.

7. If you use local configuration, load the Parallel Poll response in the Parallel Poll Register (PPR). If you use remote configuration, clear the PPR.

8. Issue the Holdoff Handshake Immediately auxiliary command to cause the NAT4882 to perform an RFD Holdoff if it is addressed to Listen.

9. Clear pon by issuing the Immediate Execute pon auxiliary command.

10. Execute the desired auxiliary commands.

The NAT4882 as GPIB Controller

The NAT4882 Controller function is generally in one of two modes: idle or in charge. When in charge, the Controller function is either active (asserting Attention (ATN)) or standby (not asserting ATN). The following sections discuss the various transitions between these two modes.

System Controller

The NAT4882 can be the GPIB System Controller and perform all System Controller functions. It can control the GPIB IFC and REN lines via the Set and Clear IFC and REN auxiliary commands. Issuing any of these auxiliary commands sets the SC pin of the NAT4882 and enables the interface to drive IFC and REN. Remember that it is the responsibility of the control program to meet the IEEE 488 specification requirements of keeping the IFC line asserted for a minimum of 100 µsec and never unasserting the REN line for less than 100 µsec. The SC pin can be cleared by issuing the Disable System and Control auxiliary command. If the SC pin is unasserted, the NAT4882 receives the IFC and REN lines.

Becoming Controller-In-Charge (CIC) and Active Controller

The NAT4882 can become CIC either by issuing the Set IFC auxiliary command while System Controller, by being passed control of the GPIB from the current active Controller, or by issuing the request control auxiliary command.

To take control, issue the Set IFC auxiliary command, wait for a minimum of 100 µsec, and issue the Clear IFC auxiliary command. The ensuing GPIB IFC message initializes the GPIB interface functions of all devices on the bus. As soon as any existing CIC goes to idle, unasserting ATN if it was active, the NAT4882 becomes CIC and Active Controller and asserts the GPIB ATN line. The SC pin can be cleared by issuing the Disable System Control auxiliary command.

Another Active Controller can pass control to the NAT4882 by sending the NAT4882 GPIB talk address (My Talk Address (MTA)) followed by the GPIB Take Control (TCT) message. The NAT4882, upon receiving these two messages, automatically becomes CIC when ATN is unasserted. The following events take place:

1. The NAT4882 receives MTA, causing a transition to Talker Addressed State (TADS). This operation can be transparent to a program. The Talker Active (TA) bit in the Address Status Register (ADSR) is set when the NAT4882 receives its GPIB talk address.
2. The NAT4882 receives the GPIB TCT.
3. The current Active Controller sees the completed Handshake, goes to idle and unasserts ATN.
4. As soon as the ATN line on the GPIB is unasserted, the NAT4882 automatically becomes CIC and asserts ATN.

As soon as the NAT4882 becomes CIC, the CIC bit in the ADSR and the Command Output (CO) bit in Interrupt Status Register 2 (ISR2) are set. Using these two bits, the program can unambiguously determine that the NAT4882 is the GPIB Active Controller and can send remote messages.

The NAT4882 can also take control by issuing the request control auxiliary command (rqc). This command causes the NAT4882 to take control as soon as the ATN line on the GPIB is unasserted. Notice that this method allows the NAT4882 to become the GPIB Active Controller without any GPIB activity.

Sending Remote Multiline Messages (Commands)

When the NAT4882 is Active Controller, you can send commands (interface messages) by writing to the Control/Data Out Register (CDOR) in response to the CO status bit in ISR2. To send commands, wait until the NAT4882 has been passed control, or has been programmed to be Active Controller, and the CDOR is empty. When this condition occurs, the CO bit in the ISR2 is set, indicating that it is safe to write a command byte to the CDOR. When you write a byte to the CDOR, the NAT4882 sends that byte as a command across the GPIB. The CO bit is set again once the byte has been received by all GPIB devices.

To determine when the CDOR is empty, either poll the ISR2 until the CO status appears, or allow a program interrupt to occur on the event. Remember, however, that if the SISB is cleared when the ISR2 is read, the status bits and interrupt signals are cleared, so the absence of a true CO status does not indicate that the CDOR is still full. If the SISB bit is set, the CO status remains set as long as the NAT4882 is Active Controller and the CDOR is empty, even if the ISR2 is read.

The NAT4882 can address itself to be both Talker and Listener in address mode 1 or 2–that is, the NAT4882 recognizes its address when it sends or receives it.

Going from Active to Standby Controller

If the NAT4882 is GPIB Active Controller, the Controller Standby State (CSBS) is entered upon reception of the Go To Standby auxiliary command. The ATN line is unasserted as soon as the NAT4882 enters CSBS. Even though the NAT4882 GPIB Controller state machine is in standby, the CIC bit in the ADSR is still set. Do not issue the Go To Standby auxiliary command unless the CO bit in ISR2 is set.

Use one of the following methods to send the NAT4882 to standby, depending on what state you want the NAT4882 to function in when ATN is unasserted:

- If you want the NAT4882 to become the GPIB Talker when ATN is unasserted, wait for CO to be set, send My Talk Address (MTA), wait for CO to be set again, and then issue the Go To Standby (gts) auxiliary command.
- If you want the NAT4882 to become a GPIB Listener when ATN is unasserted, wait for CO to be set, either issue the Listen auxiliary command or send the My Listen Address (MLA) and wait for CO to be set again, and then issue gts.
- If you want the NAT4882 to be neither GPIB Talker nor Listener, either issue the Listen in Continuous Mode auxiliary command or set the Holdoff on End (HLDE) and Holdoff on All (HLDA) bits in AUXRA before going to standby. This step puts the NAT4882 in the continuous mode, in which the NAT4882 participates in the GPIB Handshake without setting the Data In (DI) bit. Next, issue gts. When Holdoff occurs, the NAT4882 can take control

synchronously. This means that the Talker must finish its transmission with the END or EOS message. It can then take control synchronously when necessary by issuing the take control synchronously (tcs) auxiliary command.

Note: The Take Control Synchronously on End (tcse) auxiliary command can be issued after gts, thereby causing the NAT4882 to automatically take control synchronously after the END message is transmitted.

Going from Standby to Active Controller

The NAT4882 resumes GPIB Active Control in one of the following ways, depending on how it went to standby:

- As a Talker, the NAT4882 takes control upon receiving the Take Control Asynchronously (tca) auxiliary command. Do not issue tca until there are no more bytes to send and the GPIB is synchronized (that is, the DO bit is set in ISR1 or the DONE bit is set in ISR3.)
- As a Listener, the NAT4882 takes control upon receiving the Take Control Synchronously (tcs) auxiliary command. If Programmed I/O is used, issue the tcs command between seeing a DI status bit and reading the last byte from the Data In Register (DIR).
- As neither Talker nor Listener, the NAT4882 takes control synchronously with the tcs auxiliary command after detecting the End Received (END RX) bit set in Interrupt Status Register 1 (ISR1). This bit indicates that a Holdoff is in progress.

Note: The tcse auxiliary command can be issued after gts, thereby causing the NAT4882 to automatically take control on Holdoff.

When the tcs auxiliary command is used, the NAT4882 takes control of the GPIB only at the end of a data transfer. Therefore, one transfer must follow or be in progress when the tcs auxiliary command is issued. If this is not the case, you must use the tca auxiliary command. Of course, you can use the tca auxiliary command in place of the tcs auxiliary command when the possibility of disrupting an in-progress GPIB Handshake (before all GPIB Listeners have accepted the data byte) is acceptable.

If the NAT4882 does not take control as a Talker, the Enable Interrupt on End Received (END IE) bit in IMR1 can also be set to indicate to the program that the NAT4882 (functioning as a GPIB Listener) has received its last byte.

In all cases, a CO status indicates that the NAT4882 is now Active Controller.

Going from Active to Idle Controller

To go from Active to Idle GPIB Controller, or to *pass control*, the NAT4882 must initially be the Active Controller so it can send the necessary GPIB command messages. After the NAT4882 becomes the GPIB Active Controller, the sequence of events required to pass control is as follows:

1. Write the GPIB talk address of the device being passed control to the CDOR.

2. In response to the next CO status, write the TCT message to the CDOR.

As soon as the TCT command message is accepted by all devices on the GPIB, the NAT4882 automatically unasserts ATN and the new Controller asserts ATN.

The NAT4882 can also go to idle by issuing the release control auxiliary command (rlc) which causes the NAT4882 to return to the Controller Idle State (CIDS). Notice that this method allows the NAT4882 to return to CIDS without any GPIB activity.

The NAT4882 as GPIB Talker and Listener

The NAT4882 can be either GPIB Talker or Listener, but not both simultaneously. Either function is deactivated automatically if the other is activated. The Talker Active (TA), Listener Active (LA), and ATN* bits in the ADSR together indicate the specific state of the NAT4882, as follows:

ATN*	TA	LA	
0	1	0	Addressed Talker – cannot send data
1	1	0	Active Talker – can send data
0	0	1	Addressed Listener – cannot receive data
1	0	1	Active Listener – can receive data

The Addressed Status Change (ADSC), Command Output (CO), Address Pass Through (APT), Data Out (DO), and Data In (DI) status bits prompt the program (with an interrupt request if enabled) when a change of state occurs. The following sections discuss several aspects of addressing the NAT4882 as a GPIB device.

Programmed Implementation of Talker and Listener

When there is no Controller in the GPIB system, the ton and lon address modes are used to activate the NAT4882 GPIB Talker and Listener functions. For more information on ton and lon, refer to the *Address Mode Register (ADMR)* description in Chapter 2. If ton or lon are used, Talker Only (ton) or Listener Only (lon) should be set during NAT4882 initialization.

The Talker Only (ton) or Listener Only (lon) bits can also be used to temporarily place the NAT4882 in the Talker or Listener state. Setting the ton or lon bit places the NAT4882 in the Talker or Listener state respectively. To return to the Talker Idle State (TIDS) or Listener Idle State (LIDS), clear the ton or lon bit and issue the Untalk or Unlisten auxiliary command.

When the NAT4882 is GPIB Active Controller, you can use the Listen and Local Unlisten programmed auxiliary commands to activate and deactivate the NAT4882 GPIB Listener function.

Addressed Implementation of Talker and Listener

When the NAT4882 is the GPIB Active Controller, it can address itself to talk or listen by sending its own MTA or MLA using the CO bit and the CDOR. When there is another device on the GPIB acting as Controller, GPIB command messages address the NAT4882 to become a Talker or Listener. The NAT4882 also handles unaddressing automatically. If the NAT4882 is

Talker, it automatically becomes unaddressed to talk (TIDS) if it receives an Other Talk Address (OTA) message. If the NAT4882 is Listener, it automatically becomes unaddressed to listen (LIDS) if it receives the Unlisten (UNL) message.

Address Mode 1

If the NAT4882 ADMR has been configured for address mode 1, the NAT4882 responds to receiving two primary GPIB addresses: major and minor. Write the major primary address to Address Register 0 (ADR0) and the minor primary address to Address Register 1 (ADR1). Upon receiving its major or minor MTA or its major or minor MLA from the GPIB Active Controller, the NAT4882 is addressed as Talker or Listener. If the NAT4882 has received its GPIB Talk address, the TA bit in the ADSR is set, the ADSC bit in ISR2 is set, and the DO bit in ISR1 is set when ATN is unasserted. If the NAT4882 has received its GPIB listen address, the LA bit in the ADSR is set, the ADSC bit in ISR2 is set, and the DI bit in ISR1 is set when the first GPIB data byte is received. The Major-Minor (MJMN) bit in the ADSR indicates whether the address status refers to the major or minor address.

Address Mode 2

Address mode 2 is used when Talker Extended (TE) or Listener Extended (LE) functions are to be used. TE and LE functions must receive two addresses (primary and secondary) before the TA or the LA bits are set. The NAT4882 GPIB primary address is specified by the byte written to ADR0. The secondary address is specified by the byte written to ADR1. If it receives both the primary and secondary GPIB addresses, the NAT4882 becomes an addressed Talker or Listener. If the NAT4882 has received its primary GPIB talk address, the Talker Primary Addressed State (TPAS) bit in the ADSR is set. If the NAT4882 receives its secondary GPIB talk address before receiving another GPIB Primary Command Group (PCG) message that is not its MTA, the TA bit in the ADSR and the ADSC bit in the ISR2 are set and the DO bit in the ISR1 will set when ATN is unasserted. If the NAT4882 has received its primary GPIB listen address, the Listener Primary Addressed State (LPAS) bit in the ADSR is set. If the NAT4882 receives its secondary GPIB listen address before receiving another GPIB Primary Command Group (PCG) message that is not its MLA, the LA bit in the ADSR and the ADSC bit in ISR2 are set, and the DI bit in ISR1 is set when the first GPIB data byte is received.

Address Mode 3

Address mode 3, like address mode 2, is used to implement extended GPIB talk and listen address recognition. However, unlike address mode 2, address mode 3 uses both major and minor primary addresses, and your program must identify the secondary address by reading the Command Pass Through Register (CPTR). Complete the following steps to use address mode 3:

1. During initialization of the NAT4882, enable address mode 3 and, optionally, set the Enable Interrupt on Address Pass Through (APT IE) bit in IMR1 to enable an interrupt request on receipt of a secondary GPIB address.

2. Write the major GPIB primary address of the NAT4882 to Address Register 0 (ADR0) and the minor GPIB primary address of the NAT4882 to Address Register 1 (ADR1).

   Receipt of the major or minor primary MTA, or major or minor primary MLA, of the NAT4882 sets TPAS or LPAS, indicating that the primary address has been received.

3. If the next GPIB command following the primary address is a secondary address, the APT bit is set and a Data Accepted (DAC) Handshake Holdoff is activated (the GPIB DAC message is held false).

4. When APT is set, the program must perform the following steps:

   a. Determine whether the command just received is a listen, talk, major, or minor address by reading the LPAS, TPAS, and MJMN bits of the ADSR.

   b. Read the secondary address in the CPTR and determine whether it is the address of the NAT4882.

      • If the secondary address is the NAT4882 address, issue the Valid auxiliary command. The NAT4882 assumes that the My Secondary Address (MSA) message has been received, and causes the following actions to occur:

        - If LPAS was set, the LA bit is set and the TA bit is cleared, as follows:

          Listener Addressed State (LADS) = Talker Idle State (TIDS) = 1

          If TPAS was set, the TA bit is set and the LA bit is cleared, as follows:

          Talker Addressed State (TADS) = Listener Idle State (LIDS) = 1

        - The GPIB DAC message is sent true and the GPIB Handshake finishes.

      • If the secondary address is not the NAT4882 address, issue the Non-Valid auxiliary command. The NAT4882 assumes that the Other Secondary Address (OSA) message has been received, and causes the following actions to occur:

        - If TPAS was set, the NAT4882 Talker function goes to its idle state (TIDS=1).

        - The GPIB DAC message is sent true and the GPIB Handshake finishes.

Until the NAT4882 receives a PCG message (that is, as long as the subsequent messages are secondary addresses), the APT bit is set and a DAC Holdoff is in effect each time the NAT4882 receives a GPIB secondary address. Thus, the GPIB CIC can address several devices that have the same primary address each time. If the NAT4882 receives a PCG message before it receives a secondary address, the TPAS and LPAS bits are cleared.

Sending and Receiving Messages

If the NAT4882 is a GPIB Talker or Listener, you can send or receive data (device-dependent messages) by directly monitoring NAT4882 registers.

To send data, wait until the NAT4882 has been programmed or addressed to talk and the CDOR is empty. When this condition occurs, the DO bit in the ISR1 is set, indicating that it is safe to write a byte to the CDOR. When a byte is written to the CDOR, the NAT4882 sends it as a data byte on the GPIB. The DO bit is set again when all GPIB Listeners receive the byte.

To receive data, wait until the NAT4882 has been programmed or addressed to listen. When this condition occurs, the DI bit in the ISR1 is set when the GPIB Talker has sent a byte across the

GPIB and the NAT4882 has received the byte in the DIR. The NAT4882 performs an RFD Holdoff on the data byte until the byte is read from the DIR. Once that byte has been read, the RFD Holdoff is released and the DI bit is cleared until the GPIB Talker receives a new byte.

To determine when the CDOR is empty or the DIR is full, either poll the ISR1 until the DO or DI status first appears, or wait for a program interrupt to occur on the respective event. Remember, however, that if the SISB bit is cleared, the status bits and interrupt signals are cleared when the ISR1 is read, so the absence of a true DO or DI status does not indicate that the CDOR is still full or that the DIR is still empty. If SISB is set, the absence of DO indicates that the CDOR is full, and the absence of DI indicates that the DIR is empty.

A DMA Controller can also transfer data to and from the NAT4882. If you set the DMAO bit, the DMAREQ line of the NAT4882 is asserted when the CDOR is empty. The DMA Controller responds to the request by asserting DACK* and WR* to place the data byte into the CDOR. In a similar fashion, setting the DMAI bit causes the DMAREQ line to assert when a data byte is accepted into the DIR. Asserting DACK* and RD* causes the DIR to read the byte.

Sending and Receiving END or EOS

To send the GPIB END message along with a data byte, issue the Send EOI auxiliary command just before writing the data byte to the CDOR. To send the GPIB EOS message, simply make the last byte written to the CDOR the End-Of-String (EOS) code. If you use a DMA Controller to transfer data, you can use the automatic carry cycle feature to send the GPIB END message with the last byte of the transfer. The ACC bit should be set, and the TC pin of the NAT4882 should be asserted when the last byte is written to the CDOR.

The END status bit or interrupt (see the *Interrupt Status Register 1 (ISR1)* and *Interrupt Mask Register 1 (IMR1)* descriptions in Chapter 2) informs the control program that the NAT4882 has received an END or EOS message. The EOS message can be either the new line character (0A hex), if the NLEE bit is set in the Interrupt Status Register 0, or the value written to the End-Of-String Register (EOSR), if the REOS bit is set in Auxiliary Mode Register A, or both. The value in the EOSR can be compared to the byte in the DIR as an eight-bit value (BIN set) or a seven-bit value (BIN cleared). The new line character is always compared to the data byte in the DIR as a seven-bit character.

Once the END bit is set, the control program can determine which terminating event caused it to set by monitoring certain status bits. The EOI bit in ADR1 sets if END set because the GPIB EOI line was asserted with the last byte. The NL or EOS bits set in the ISR0 if the END bit was set upon receiving the new line character or a data byte matching the value of the EOSR, respectively.

Performing an RFD Holdoff on the Last Data Byte

You will usually want to perform an RFD Holdoff on the last byte of a string of data read in from the GPIB during a GPIB read operation. If the last byte of data read in was sent with EOI asserted or was the EOS character, an RFD Holdoff will be performed automatically if the NAT4882 has been programmed for the RFD Holdoff on END Mode (AUXRA(1-0) = 10 (bin)). If you do not know if the last byte sent by the Talker will be transmitted with EOI or match the EOS character, program the NAT4882 to RFD Holdoff on all data Mode (AUXRA(1-0) = 01 (bin)). This causes

the NAT4882 to perform an RFD Holdoff on the next byte of data received in the DIR until a Release Handshake Holdoff auxiliary command is issued. If a DMA Controller is used to transfer data, you can use the automatic carry cycle feature to perform an RFD Holdoff with the last byte of the transfer. Set the ACC bit and assert the TC pin of the NAT4882 when the last byte is read from the DIR.

Aborting a Data Transmission

When sourcing data on the GPIB as a Talker, you sometimes must abort a transfer before it is complete. The most common method of aborting a transfer is to have the Controller take control synchronously (assert ATN) and unaddress the NAT4882 before it completes its transfer. If this occurs and the NTNL is cleared, a data byte that was written to the CDOR, but not yet sourced, is flushed from the CDOR. If the NTNL bit is set, a data byte written to the CDOR, but not yet sourced, is retained. If the NAT4882 is readdressed to talk, the NAT4882 proceeds where it left off sourcing the data byte in the CDOR. If the control program does not need to transfer the byte in the CDOR when it is readdressed to talk, you can flush the CDOR by issuing the new byte available false auxiliary command (nbaf).

Serial Polls

By using Serial Polls, the GPIB Controller-in-Charge (CIC) can obtain detailed status information on each device that has been configured for responding.

Conducting Serial Polls

The NAT4882, as CIC, can serial poll other devices as described in the IEEE Standard 488.1-1987, *IEEE Standard Digital Interface for Programmable Instrumentation*. From the programming perspective, the NAT4882 must first become Active Controller to send the addressing and enabling commands to the device being polled, make itself a GPIB Listener by either issuing the Listen auxiliary command or sending its listen address, and then go to standby with the Go To Standby auxiliary command to read the status byte from the addressed GPIB device. The NAT4882 can detect when a device is requesting service while it is CIC through the SRQI interrupt status bit in ISR2.

Requesting Service

The NAT4882 supports two means of requesting service: the rsv bit in SPMS and the reqt and reqf auxiliary commands. Use only one method in an application program.

If you use the rsv bit in SPMR before you request service, you must check the Pending (PEND) bit of the SPSR to ensure that the NAT4882 is not presently in the middle of a Serial Poll (SP) (SPAS = 0). If PEND = 0, write the desired Status Byte (STB) to the SPMR with the rsv bit set. At that time, PEND sets and the NAT4882 asserts the SRQ line. The PEND bit remains set until the SP completes.

If you use the reqt and reqf auxiliary commands to request service, issue the reqt auxiliary command and write the desired Status Byte (STB) to the SPMR with the rsv bit cleared. The reqt auxiliary command sets the local message rsv according to the Set rsv state machine described in

the IEEE 488.2 specification. That is, the local rsv message becomes true when the NAT4882 Request Service function is not in Affirmative Poll Response State (APRS). The local message rsv goes false when the NAT4882 enters APRS. If, after issuing the reqt auxiliary command, there is no longer a reason to request service, you can clear the local message rsv by issuing the reqf auxiliary message and writing the desired Status Byte (STB) to the SPMR with the rsv bit cleared.

Note: If you use the reqt and reqf auxiliary commands to control the local message rsv, the rsv bit in the SPMR must always be cleared.

Responding to Serial Polls

The Controller-in-Charge can conduct Serial Polls to determine which device is asserting the GPIB SRQ signal to request service and to obtain status from the requesting device.

Once Request Service (rsv) is set, the NAT4882 waits until any current SP is complete and asserts the GPIB SRQ signal. In response to that signal, the CIC starts the SP by addressing the NAT4882 to talk and sending the Serial Poll Enable (SPE) command. When the CIC unasserts ATN, the NAT4882 unasserts Service Request (SRQ) and transfers the STB message on to the GPIB data bus with DIO7 (the RSQ signal) asserted.

The NAT4882 supports two different manners of transmitting its STB. If the STBO IE bit is cleared, the NAT4882 automatically transmits the STB in the SPMR when serial polled, and sets the RQS field with the value of the local message rsv. If the STBO IE bit is set, the NAT4882 sets the STBO status bit in ISR0 when it is serial polled, causing the NAT4882 interrupt line to be asserted. The NAT4882 does not source its STB until the SPMR is written with the current STB. Writing the SPMR also clears the STBO status bit and the interrupt condition. When the STB is sourced in this manner, the RQS field is still equal to the value of the local message rsv.

While the SP is in progress (SPAS = 1), the CIC normally reads the STB only once, but can read it any number of times if it asserts ATN between each 1-byte read. However, RSQ is set only during the first read. After the first read, rsv is cleared as well. PEND is cleared when the CIC asserts ATN to terminate the SP.

The GPIB EOI line is asserted along with the status byte (that is, the END message is sent) during the SP if the Send Serial Poll End Or Identify bit (SPEOI) of AUXRB is set.

Parallel Polls

The GPIB Active Controller uses Parallel Polls to check the status of several devices simultaneously. The meaning of the status returned by the devices being polled is device-dependent, but there are two general ways in which Parallel Polls are useful.

- When the GPIB Controller recognizes SRQ asserted in a system with eight or less devices, it can determine quickly, usually using only one Parallel Poll (PP), which one needs to be serial polled.

- In systems in which the Controller requires little response time to service a device is low and the number of devices is low, PPs can replace SPs entirely, if the Controller polls frequently.

Although the Controller can obtain a Parallel Poll Response (PPR) quickly and at any time, there can be considerable front-end overhead during initialization to configure the devices to respond appropriately. This situation is contrasted with SP, whose overhead, in the form of addressing and enabling command messages, occurs with each SP.

Conducting a Parallel Poll

The NAT4882 as Active Controller can conduct a Parallel Poll either by using the Execute Parallel Poll auxiliary command and the RPP2 bit in AUXRG.

When you issue the Execute Parallel Poll auxiliary command, the NAT4882 internal local message rpp is set and a Parallel Poll is executed (that is, the GPIB message IDY is sent true) as soon as the NAT4882 Controller interface function is placed in the proper state (CAWS or CACS). The NAT4882 automatically reads the response from the GPIB DIO line into the CPTR and clears the rpp local message after a 2 μsec interval. To determine whether the PP operation is complete, the program must determine the condition of CO (that is, CO = 1 when the poll is complete) and read the contents of the CPTR to obtain the PPR. The response is held in the CPTR until a GPIB command is transmitted or the NAT4882 Controller function becomes inactive.

Setting the RPP2 bit in AUXRG also sets the NAT4882 internal local message rpp and causes a PP to execute. The NAT4882 remains in the PP state (ATN and EOI asserted) until the RPP2 is cleared, allowing the control program to extend the length of the PP for either applications that use GPIB extenders or instruments that take longer than 2 μsecs to respond to a PP. To end the PP, the control program must read the contents of the CPTR to obtain the results of the PP, and then clear the RPP2 bit.

In response to IDY, each device participating in the PP drives only one GPIB DIO line (its PPR) active true or passive false, while it drives the other GPIB DIO lines passive false.

Because there are eight data lines, each line can have two responses (true or false), there are 16 possible responses. Which line a device uses and how that device drives the line depend on how the device is configured and whether its local individual status message (ist) is one or zero. Thus, each device on the GPIB can be configured to drive its assigned DIO line true if ist = 1 or to drive the DIO line false if ist = 0. Alternately, each device can also be configured to do the opposite, and to drive the DIO line true if ist = 0 or false if ist = 1. The meaning of the value of ist, whether one or zero, is system- or device-dependent.

Because the data lines are driven with an Open Collector driver during Parallel Polls, more than one device can respond on each line. The device or devices asserting the line true override any device asserting the line false. The Controller must know in advance whether a true response means that the local ist message of the device is one or zero. To do this, the device must be configured to respond in one of the following ways:

- *Local configuration* (Parallel Poll function subset PP2) involves assigning a response line and a sense (polarity) from the device side, in a similar manner to assigning the device GPIB address. Thus, one device might be assigned to respond with remote message PPR1 (driving DIO1), while a second device might be assigned to respond with remote message PPR3 (driving DIO3), both positive (that is, a true response if ist = 1). Local configuration is static, in that it does not change after the system is installed and configured.

- *Remote configuration* (Parallel Poll function subset PP1) involves dynamically assigning response line and assigning sense to devices on the GPIB. These steps are accomplished using Parallel Poll Enable (PPE) and Parallel Poll Disable (PPD) commands, which are issued by the Active Controller. Complete the following steps to remotely configure devices:

  1. Place the NAT4882 in the Active Controller state.

  2. Send the GPIB UNL (Unlisten) message to unaddress all GPIB Listeners.

  3. Send the listen address of the first device to be configured.

  4. Send the GPIB PPC message, followed by the PPE message for that device.

  5. Repeat this procedure from step 2 for each additional device.

  Use this procedure to disable polling as well, substituting the PPD message for the PPE message.

Responding to a Parallel Poll

Before the NAT4882 can be polled by the CIC, the NAT4882 must be configured either locally by the user program at initialization time or remotely by the CIC. Configuration involves the following steps:

- Enabling the NAT4882 to participate in polls

- Selecting the sense or polarity of the response

- Selecting the GPIB data line on which the response is asserted when the CIC issues the Identify (IDY) message

Using remote configuration (PP1), the NAT4882 interprets the configuration commands received from the CIC without any software assistance or interpretation from the user program. Using local configuration (PP2), the three steps listed above must be explicitly handled in the software by writing the appropriate values to the U, S, and P3 through P1 bits of the PPR. Refer to the *Parallel Poll Register* description in Chapter 2 for more information.

Note: If you use local configuration (PP2), the values written to the PPR are overwritten if the NAT4882 is also configured remotely, causing the NAT4882 to respond as requested by the remote configuration. To avoid this problem, set the PP2 bit in AUXRI. This bit causes the NAT4882 to ignore remote Parallel Poll configure commands, and to respond to Parallel Polls in the manner configured locally.

When the PPR is configured, all that remains for the user program is to determine the source and value of the local individual status (ist) message. If the Individual Status Select (ISS) bit in the AUXRB is zero, ist is set and cleared using the Set Parallel Poll and Clear Parallel Poll auxiliary commands. If ISS is set to 1, ist is set if the Service Request function of the NAT4882 is in the Service Request State (SRQS), and the NAT4882 is asserting the GPIB SRQ signal line. Otherwise, ist is cleared. Consequently, setting ISS ties the PP function to the Service Request function, as well as to the Serial Poll function.

The particular response sent by the NAT4882 during a PP is determined by the value of ist and the configuration of the NAT4882. The value of ist and the actual configuration must be decided by the GPIB system integrator. The response can be changed dynamically during program execution by changing the value of ist and, when remote configuration is used, by reconfiguration.

You can completely disable responding to Parallel Polls by setting the PP2 bit in AUXRI and setting the U bit in the PPR, thus supporting PP0 (no Parallel Poll capability).

Interrupts

The NAT4882 can generate interrupts on any of the 18 conditions specified by the ISR0, ISR1, and ISR2 bits. For one of these conditions to drive the NAT4882 interrupt signal, the following must be true:

- The interrupt condition must be true.
- The interrupt condition must be enabled.

After the NAT4882 asserts the interrupt request line, it remains asserted until the bit causing the interrupt condition is cleared. If the interrupt is caused by a condition in the ISR0, ISR1, or ISR2 and the SISB is cleared, the interrupt can be cleared by reading the ISR0, ISR1, or ISR2 or by taking action to clear the condition. If the SISB bit is set, the interrupt is cleared when action is taken to clear the condition.

If the SISB bit is cleared, the status bits in ISR0, ISR1, and ISR2 are all automatically cleared when the register is read, even if the conditions are still true. If two conditions are true at the same time (that is, more than one bit in the ISR1 or ISR2 is set) and the SISB bit is cleared, you should maintain a software copy of the register if the program is going to analyze the conditions one at a time.

Direct Memory Access (DMA)

The NAT4882 supplies a DMA request and DMA acknowledge signal to be used when interfacing to a DMA Controller. DMA is enabled for GPIB writes or GPIB reads by setting the DMAO or DMAI bits, respectively. Additionally, the T/C (terminal count) pin may be interfaced to indicate the last byte of a transfer between the NAT4882 and the DMA Controller. The Automatic Carry Cycle (see the ACC bit description in AUXRI) and Synchronization Detection (see the SYNC bit description in ISR0) features use the T/C input.

Synchronization Detection

When a transfer completes, you usually want the Controller to detect when all the bytes have been accepted by all Listeners. This action is called *bus synchronization*. When the bus is synchronized, the Controller can take control with the tca auxiliary command without disrupting bus activity. The NAT4882 uses a sychronization detection circuit for this purpose.

The detection circuit operates in either a programmed I/O or DMA mode, depending on the setting of the DMAO and DMAI bits in IMR2. If both bits are clear, programmed I/O mode is enabled. When performing GPIB writes in this mode, issue the Clear SYNC auxiliary command before you write the last byte to the CDOR. When performing programmed I/O reads, issue the Set SYNC auxiliary command before you read the last byte from the DIR.

DMA mode is enabled by setting either DMAI or DMAO. If a DMA controller is used and the T/C pin is asserted during the last byte of either a read or write transfer, the programming is simplified. You only need to issue the Clear SYNC auxiliary command after programming the IMR2 and before starting the DMA controller. In both modes, the bus is synchronized when the SYNC bit in ISR0 is set. You can interrupt off this condition by setting the SYNC IE bit in IMR0.

Timeouts

The NAT4882 contains a built-in timer that can generate interrupts or terminate GPIB subroutine calls that may not return. The timer is controlled and monitored via the AUXRJ, BTO and TO bits in ISR0. The timeout value can be set between the range of 16 μsec to 134 sec. Refer to the *Auxiliary Register J* description in Chapter 2 for more information on programming the timeout values. The timer starts when a nonzero value is written to the AUXRJ. The timer operates in either Global or Byte mode.

Global Timeouts

If the BTO bit is cleared, the timer operates in Global mode. Once the timer starts, it continues to count until the timeout value is reached, which sets the TO bit in ISR0. The TO bit remains set until a value is written to the AUXRJ. The TO bit can generate an interrupt if the TO IE bit is set in IMR0.

Byte Timeouts

If the BTO bit is set, the timer operates in Byte mode. Once the timer starts, it continues to count until the timeout value is reached. However, reads of the DIR or writes of the CDOR clear the timer and force it to start counting over. When the timer reaches the time-out value, the TO bit is set and remains set until the AUXRJ is written. Further reads of DIR or writes of CDOR have no effect on TO until the AUXRJ is written again. Byte timeouts can generate interrupts when long delays exist between data or command bytes transferred across the GPIB. The TO bit can generate an interrupt if the TO IE bit is set in IMR0.

Appendix A
Multiline Interface Command Messages

This appendix lists the multiline interface messages and describes the mnemonics and messages that correspond to the interface functions. These functions include initializing the bus, addressing and unaddressing devices, and setting device modes for local or remote programming. The multiline interface messages are IEEE 488-defined commands that are sent and received with ATN TRUE.

Multiline Interface Messages

Hex	Oct	Dec	ASCII	Msg	Hex	Oct	Dec	ASCII	Msg
00	000	0	NUL		20	040	32	SP	MLA0
01	001	1	SOH	GTL	21	041	33	!	MLA1
02	002	2	STX		22	042	34	"	MLA2
03	003	3	ETX		23	043	35	#	MLA3
04	004	4	EOT	SDC	24	044	36	$	MLA4
05	005	5	ENQ	PPC	25	045	37	%	MLA5
06	006	6	ACK		26	046	38	&	MLA6
07	007	7	BEL		27	047	39	'	MLA7
08	010	8	BS	GET	28	050	40	(	MLA8
09	011	9	HT	TCT	29	051	41	)	MLA9
0A	012	10	LF		2A	052	42	*	MLA10
0B	013	11	VT		2B	053	43	+	MLA11
0C	014	12	FF		2C	054	44	,	MLA12
0D	015	13	CR		2D	055	45	-	MLA13
0E	016	14	SO		2E	056	46	.	MLA14
0F	017	15	SI		2F	057	47	/	MLA15
10	020	16	DLE		30	060	48	0	MLA16
11	021	17	DC1	LLO	31	061	49	1	MLA17
12	022	18	DC2		32	062	50	2	MLA18
13	023	19	DC3		33	063	51	3	MLA19
14	024	20	DC4	DCL	34	064	52	4	MLA20
15	025	21	NAK	PPU	35	065	53	5	MLA21
16	026	22	SYN		36	066	54	6	MLA22
17	027	23	ETB		37	067	55	7	MLA23
18	030	24	CAN	SPE	38	070	56	8	MLA24
19	031	25	EM	SPD	39	071	57	9	MLA25
1A	032	26	SUB		3A	072	58	:	MLA26
1B	033	27	ESC		3B	073	59	;	MLA27
1C	034	28	FS		3C	074	60	<	MLA28
1D	035	29	GS		3D	075	61	=	MLA29
1E	036	30	RS		3E	076	62	>	MLA30
1F	037	31	US		3F	077	63	?	UNL

Message Definitions

DCL Device Clear
GET Group Execute Trigger
GTL Go To Local
LLO Local Lockout
MLA My Listen Address
MSA My Secondary Address
MTA My Talk Address
PPC Parallel Poll Configure
PPD Parallel Poll Disable

Multiline Interface Messages

Hex	Oct	Dec	ASCII	Msg	Hex	Oct	Dec	ASCII	Msg
40	100	64	@	MTA0	60	140	96	`	MSA0,PPE
41	101	65	A	MTA1	61	141	97	a	MSA1,PPE
42	102	66	B	MTA2	62	142	98	b	MSA2,PPE
43	103	67	C	MTA3	63	143	99	c	MSA3,PPE
44	104	68	D	MTA4	64	144	100	d	MSA4,PPE
45	105	69	E	MTA5	65	145	101	e	MSA5,PPE
46	106	70	F	MTA6	66	146	102	f	MSA6,PPE
47	107	71	G	MTA7	67	147	103	g	MSA7,PPE
48	110	72	H	MTA8	68	150	104	h	MSA8,PPE
49	111	73	I	MTA9	69	151	105	i	MSA9,PPE
4A	112	74	J	MTA10	6A	152	106	j	MSA10,PPE
4B	113	75	K	MTA11	6B	153	107	k	MSA11,PPE
4C	114	76	L	MTA12	6C	154	108	l	MSA12,PPE
4D	115	77	M	MTA13	6D	155	109	m	MSA13,PPE
4E	116	78	N	MTA14	6E	156	110	n	MSA14,PPE
4F	117	79	O	MTA15	6F	157	111	o	MSA15,PPE
50	120	80	P	MTA16	70	160	112	p	MSA16,PPD
51	121	81	Q	MTA17	71	161	113	q	MSA17,PPD
52	122	82	R	MTA18	72	162	114	r	MSA18,PPD
53	123	83	S	MTA19	73	163	115	s	MSA19,PPD
54	124	84	T	MTA20	74	164	116	t	MSA20,PPD
55	125	85	U	MTA21	75	165	117	u	MSA21,PPD
56	126	86	V	MTA22	76	166	118	v	MSA22,PPD
57	127	87	W	MTA23	77	167	119	w	MSA23,PPD
58	130	88	X	MTA24	78	170	120	x	MSA24,PPD
59	131	89	Y	MTA25	79	171	121	y	MSA25,PPD
5A	132	90	Z	MTA26	7A	172	122	z	MSA26,PPD
5B	133	91	[	MTA27	7B	173	123	{	MSA27,PPD
5C	134	92	\	MTA28	7C	174	124	|	MSA28,PPD
5D	135	93	]	MTA29	7D	175	125	}	MSA29,PPD
5E	136	94	^	MTA30	7E	176	126	~	MSA30,PPD
5F	137	95	_	UNT	7F	177	127	DEL	

PPE	Parallel Poll Enable	SPE	Serial Poll Enable
PPU	Parallel Poll Unconfigure	TCT	Take Control
SDC	Selected Device Clear	UNL	Unlisten
SPD	Serial Poll Disable	UNT	Untalk

Appendix B
Mnemonics Key

This appendix is an easy reference table that defines the mnemonics (abbreviations) used throughout this manual for functions, remote messages, local messages, states, bits, registers, integrated circuits, and system functions.

The mnemonic types in the key that follows are abbreviated to mean the following:

B	Bit
F	Function
IC	Integrated Circuit
LM	Local Message
R	Register
RM	Remote Message
SF	System Function
ST	State

Mnemonic	Type	Definition
A		
ACDS	ST	Acceptor Data State (AH function)
ACG	RM	Addressed Command Group
ACRS	ST	Acceptor Ready State
AD[5-1]	B	Talker/Listener/Controller (TLC) GPIB Address Bits 5 through 1
AD[5-0 – 1-0]	B	Mode 2 Primary TLC GPIB Address Bits 5 through 1
AD[5-1 – 1-1]	B	Mode 2 Secondary TLC GPIB Address Bits 5 through 1
ADCS	B	Addressed Status Change Bit
ADCS IE	B	Enable Interrupt on Addressed Status Change Bit
ADM[1-0]	B	Address Mode Bits 1 through 0
ADMR	R	Address Mode Register
ADR	R	Address Register
ADR0	R	Address Register 0
ADR1	R	Address Register 1
ADSC	B	Address Status Change Bit
ADSC IE	B	Enable Interrupt on Address Status Change Bit
ADSR	R	Address Status Register
AH	ST	Acceptor Handshake
AIDS	ST	Acceptor Idle State
ANRS	ST	Acceptor Not Ready State
APRS	ST	Affirmative Poll Response State
APT	B	Address Pass Through Bit
APT IE	B	Enable Interrupt on Address Pass Through Bit
ARS	B	Address Register Select Bit
ATN	SL	Attention
ATN*	B	Attention Bit
ATN IE	B	Enable Interrupt on Attention Bit
AUXMR	R	Auxiliary Mode Register
AUXRA	R	Auxiliary Register A
AUXRB	R	Auxiliary Register B
AUXRE	R	Auxiliary Register E
AWNS	ST	Acceptor Wait for New Cycle State
B		
BIN	B	Binary Bit
C		
C	F	Controller
CACS	ST	Controller Active State (C function)
CADS	ST	Controller Addressed State
CAWS	ST	Controller Active Wait State
CDOR	R	Control/Data Out Register
CDO[7-0]	B	Control/Data Out Bits 7 through 0
CIC	B	Controller-In-Charge Bit

Mnemonic	Type	Definition
CIDS	ST	Controller Idle State
CNT[2-0]	B	Control Code Bits 2 through 0
CO	B	Command Output Bit
CO IE	B	Enable Interrupt on Command Output Bit
COM[4-0]	B	Command Code Bits 4 through 0
CPPS	ST	Controller Parallel Poll State
CPT	B	Command Pass Through Bit
CPT ENAB	B	Command Pass Through Enable Bit
CPT IE	B	Enable Interrupt on Command Pass Through Bit
CPTR	R	Command Pass Through Register
CPT[7-0]	B	Command Pass Through Bits 7 through 0
CPWS	ST	Controller Parallel Poll Wait State
CSBS	ST	Controller Standby State
CSHS	ST	Controller Standby Hold State
CSNS	ST	Controller Service Not Requested State
CSRS	ST	Controller Service Requested State
CSWS	ST	Controller Synchronous Wait State
CTRS	ST	Controller Transfer State (C function)

D

DAB	RM	Data Byte
DAC	RM	Data Accepted
DACK	R	Direct Memory Access (DMA) Acknowledge Register
DAV	B	GPIB Data Valid Signal Bit
DAV	RM	Data Valid
DC	F	Device Clear
DCAS	ST	Device Clear Active State
DCIS	ST	Device Clear Idle State
DCL	RM	Device Clear
DEC	B	Device Clear Bit
DEC IE	B	Enable Interrupt on Device Clear Bit
DET	B	Device Execute Trigger Bit
DET IE	B	Enable Interrupt on Device Execute Trigger Bit
DHDC	B	Data Accepted Holdoff on Device Clear Active State Bit
DHDT	B	Data Accepted Holdoff on Device Trigger Active State Bit
DI	B	Data In Bit
DI[7-0]	B	Data In Bits 7 through 0
DI IE	B	Enable Interrupt on Data In Bit
DIO[8-1]	B	GPIB Data Drive and Read Register Bits 8 through 1
DIR	R	Data In Register
DL	B	Disable Listener Bit
DL0	B	Disable Listener 0 Bit
DL1	B	Disable Listener 1 Bit
DMA	SF	Direct Memory Access
DMAEN	B	Direct Memory Access Enable Bit
DMAI	B	Direct Memory Access Input Enable Bit
DMAO	B	Direct Memory Access Output Enable Bit
DO	B	Data Out Bit

Mnemonic	Type	Definition
DO IE	B	Enable Interrupt on Data Out Bit
DT	F	Device Trigger
DT	B	Disable Talker Bit
DT0	B	Disable Talker 0 Bit
DT1	B	Disable Talker 1 Bit
DTAS	ST	Device Trigger Active State
DTIS	ST	Device Trigger Idle State

E

END	RM	End
END IE	B	Enable Interrupt on End Received Bit
END RX	B	End Received Bit
EOI	B	End or Identify Bit
EOI	RM	End or Identify
EOS	RM	End of String
EOS[7-0]	B	End of String Bits 7 through 0
EOSR	R	End of String Register
ERR	B	Error Bit
ERR	RM	Error
ERR IE	B	Enable Interrupt on Error Bit

G

GET	RM	Group Execute Trigger
GTL	RM	Go To Local
gts	LM	Go to Standby

H

HLDA	B	Holdoff on All Bit
HLDE	B	Holdoff on End Bit

I

IDY	RM	Identify
IFC	RM	Interface Clear
IMR1	R	Interrupt Mask Register 1
IMR2	R	Interrupt Mask Register 2
INT	B	Interrupt Bit
INV	B	Invert Bit
ISR1	R	Interrupt Status Register 1
ISR2	R	Interrupt Status Register 2
ISS	B	Individual Status Select Bit
ist	LM	Individual Status

Mnemonic	Type	Definition

K

KEYCLK	B	Key Clock Bit
KEYDATA	B	Data input from an electronic key Bit
KEYDATEN	B	Key Data Enable Bit
KEYRST*	B	Key Reset Bit

L

L	F	Listener
LA	B	Listener Active Bit
LACS	ST	Listener Active State (L function)
LADS	ST	Listener Addressed State (L function)
LAG	RM	Listener Address Group
LE	F	Listener Extended
LIDS	ST	Listener Idle State
LLO	RM	Local Lockout
LOCS	ST	Local State
LOK	B	Lockout Bit
LOKC	B	Lockout Change Bit
LOKC IE	B	Enable Interrupt on Lockout Change Bit
lon	B	Listen Only Bit
lon	LM	Listen Only
LPAS	B	Listener Primary Addressed State Bit
LPAS	ST	Listener Primary Addressed State
lpe	LM	Local Poll Enabled
LPIS	ST	Listener Primary Idle State
ltn	LM	Listen
lun	LM	Local Unlisten
LWLS	ST	Local With Lockout State

M

MJMN	B	Major-Minor Bit
MLA	RM	My Listen Address
MSA	RM	My Secondary Address
MTA	RM	My Talk Address

N

nba	LM	New Byte Available
NDAC*	B	GPIB Not Data Accepted Bit
NPRS	ST	Negative Poll Response State
NRFD*	B	GPIB Not Ready For Data Bit
NUL	RM	Null byte

Mnemonic	Type	Definition
O		
OSA	RM	Other Secondary Address
OTA	RM	Other Talk Address
P		
P[3-1]	B	Parallel Poll Response Bits 3 through 1
PACS	ST	Parallel Poll Addressed to Configure State
PCG	RM	Primary Command Group
PEND	B	Pending Bit
pon	LM	Power On
PP	F	Parallel Poll (scan all status flags)
PPAS	ST	Parallel Poll Active State
PPC	RM	Parallel Poll Configure
PPD	RM	Parallel Poll Disable
PPE	RM	Parallel Poll Enable
PPIS	ST	Parallel Poll Idle State
PPR	RM	Parallel Poll Response
PPR	R	Parallel Poll Register
PPSS	ST	Parallel Poll Standby Active
PPU	RM	Parallel Poll Unconfigure
PUCS	ST	Parallel Poll Unaddressed to Configure State
R		
rdy	LM	Ready for next message
REM	B	Remote Bit
REMC	B	Remote Change Bit
REMC IE	B	Enable Interrupt on Remote Change Bit
REMS	ST	Remote State
REN	RM	Remote Enable
REOS	B	End on End Of String Received Bit
RFD	RM	Ready For Data
RL	F	Remote/Local
rpp	LM	Request Parallel Poll
RQS	RM	Request Service
rsc	LM	Request System Control
rsv	B	Request Service Bit
rsv	LM	Request Service
rtl	LM	Return To Local
RWLS	ST	Remote With Lockout State
S		
S	B	Status Bit Polarity (Sense) Bit
S[6-1]	B	Serial Poll Status Bits 6 through 1
S8	B	Serial Poll Status Byte Bit

Mnemonic	Type	Definition
SACS	ST	System Control Active State
SCG	RM	Secondary Command Group
SDC	RM	Selected Device Clear
SDYS	ST	Source Delay State
SGNS	ST	Source Generate State
SH	F	Source Handshake
SIAS	ST	System Control Interface Clear Active State
sic	LM	Send Interface Clear
SIDS	ST	Source Idle State
SIIS	ST	System Control Interface Clear Idle State
SINS	ST	System Control Interface Clear Not Active State
SIWS	ST	Source Idle Wait State
SNAS	ST	System Control Not Active State
SP	F	Serial Poll (scanning flags)
SPAS	ST	Serial Poll Active State (T function)
SPD	RM	Serial Poll Disable
SPE	RM	Serial Poll Enable
SPEOI	B	Send Serial Poll End Or Identify Bit
SPIS	ST	Serial Poll Idle State
SPMR	R	Serial Poll Mode Register
SPMS	B	Serial Poll Mode State Bit
SPMS	ST	Serial Poll Mode State
SPSR	R	Serial Poll Status Register
SR	F	Service Request
SRAS	ST	System Control Remote Enable Active State
sre	LM	Send Remote Enable
SRIS	ST	System Control Remote Enable Idle State
SRNS	ST	System Control Remote Enable Not Active State
SRQ	RM	Service Request
SRQI	B	Service Request Input Bit
SRQI IE	B	Enable Interrupt on Service Request Input Bit
SRQS	ST	Service Request State
STB	RM	Status Byte
STRS	ST	Source Transfer State
SWNS	ST	Source Wait for New Cycle State

T

T	F	Talker
TA	B	Talker Active Bit
TACS	ST	Talker Active State (T function)
TADS	ST	Talker Addressed State
TAG	RM	Talk Address Group
tca	LM	Talk Control Asynchronously
tcs	LM	Take Control Synchronously
tcse	LM	Take Control Synchronously on End
TCT	TM	Take Control
TE	F	Extended Talk
TIDS	ST	Talker Idle State

Mnemonic	Type	Definition
TLC	IC	Talker/Listener/Controller (GPIB Adapter)
ton	B	Talker Only Bit
ton	LM	Talker Only
TPAS	B	Talker Primary Addressed State Bit
TPAS	ST	Talker Primary Addressed State
TPIS	ST	Talker Primary Idle State
TRI	B	Three-State Timing Bit
TRM[1-0]	B	Transmit/Receive Mode Bits 1 through 0

U

U	B	Unconfigure Bit
UCG	RM	Universal Command Group
UNL	RM	Unlisten command
UNT	RM	Untalk command

X

X	B	Don't Care Bit
XEOS	B	Transmit End with End Of String Bit

Appendix C
Customer Communication

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve technical problems you might have as well as a form you can use to comment on the product documentation. Filling out a copy of the *Technical Support Form* before contacting National Instruments helps us help you better and faster.

National Instruments provides comprehensive technical assistance around the world. In the U.S. and Canada, applications engineers are available Monday through Friday from 8:00 a.m. to 6:00 p.m. (central time). In other countries, contact the nearest branch office. You may fax questions to us at any time.

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Technical Support Form

Photocopy this form and update it each time you make changes to your software or hardware, and use the completed copy of this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name _____

Company _____

Address _____

_____

Fax (___)_____ Phone (___)_____

Computer brand _____ Model _____ Processor _____

Operating system _____

Speed _____MHz RAM _____M Display adapter _____

Mouse _____yes _____no Other adapters installed _____

Hard disk capacity _____M Brand _____

Instruments used _____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is _____

_____

_____

_____

_____

List any error messages _____

_____

_____

_____

_____

The following steps will reproduce the problem _____

_____

_____

Documentation Comment Form

National Instruments encourages you to comment on the documentation supplied with our products. This information helps us provide quality products to meet your needs.

Title: **NAT4882® Programmer Reference Manual**

Edition Date: **October 1993**

Part Number: **320383-01**

Please comment on the completeness, clarity, and organization of the manual.

If you find errors in the manual, please record the page numbers and describe the errors.

Thank you for your help.

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Glossary

Prefix	Meaning	Value
n- μ- M-	nano- micro- mega-	10^{-9} 10^{-6} 10^{6}

ANSI	American National Standards Institute
ASCII	American Standard Code for Information Interchange
ASIC	application-specific integrated circuit
CIC	Controller-In-Charge
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DMA	direct memory access
EOI	End or Identify bit
EOS	end of string
FIFO	first-in-first-out
GPIB	General Purpose Interface Bus
hex	hexadecimal
Hz	hertz
I/O	input/output
IEEE	Institute of Electrical and Electronic Engineers
M	megabytes of memory
PLCC	Plastic Leaded Chip Carrier
sec	second
TLC	Talker/Listener/Controller

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Symbols/Numbers

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