SPECIFICATIONS

PXIe-6674

Timing and Synchronization Module for PXI Express

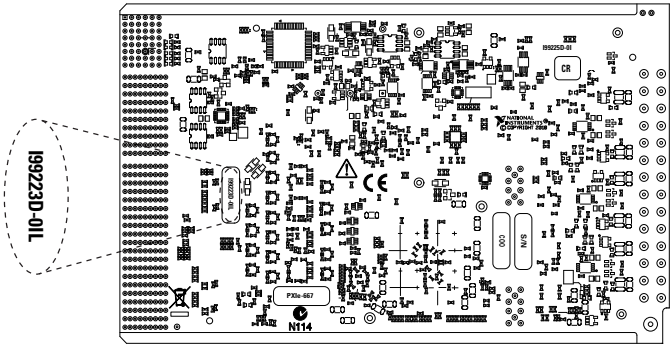
This section lists the system specifications for PXIe-6674 modules. These specifications are typical at 25 °C, unless otherwise stated.

Caution Specifications are subject to change without notice.

Note Some specifications are specific to earlier revisions of the PXIe-6674 module. A label with revision information can be found on the module board as shown in the PXIe-6674 Revision Label figure below.

x denotes all letter revisions of the assembly. Ensure the specifications of interest match the revision that is printed on the label.

Figure 1. PXIe-6674 Revision Label



Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

The following characteristic specifications describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are *Typical* unless otherwise noted.

PXIe-6674 Conditions

Specifications are valid at 25 °C unless otherwise noted.

CLKIN Characteristics

Input coupling	AC
Input impedance	50 Ω, nominal

Table 1. Minimum and Maximum Input Levels

Setting	Attenuation Setting On	Attenuation Setting Off
Attenuation Setting	On (default)	Off
Attenuation Behavior	5:1	1:1
Minimum Input Swing with 50% Duty Cycle*	750 mV_{pp}	150 mV_{pp}
Maximum Input Swing with 50% Duty Cycle†	5.0 V_{pp}	1.2 V_{pp}
Absolute Maximum Input Powered On‡	5.6 V_{pp}	2.8 V_{pp}

Table 1. Minimum and Maximum Input Levels (Continued)

Setting	Attenuation Setting On	Attenuation Setting Off
Absolute Maximum Input Powered Off**	1.5 V_{pp}	

* A duty cycle other than 50% will increase the minimum input swing. Refer to Figure A-2 for more information.

† A duty cycle other than 50% will increase the minimum input swing. Refer to Figure A-3 for more information.

‡ Operation above the Absolute Maximum Input Powered On may cause damage to the device.

** Absolute Maximum Input Powered Off is the maximum input signal amplitude that the device can tolerate before damage might occur while in an unpowered state.

Note Input can be either square wave or sinusoidal.

Figure 2. Maximum and Minimum Input Swing with Attenuation On

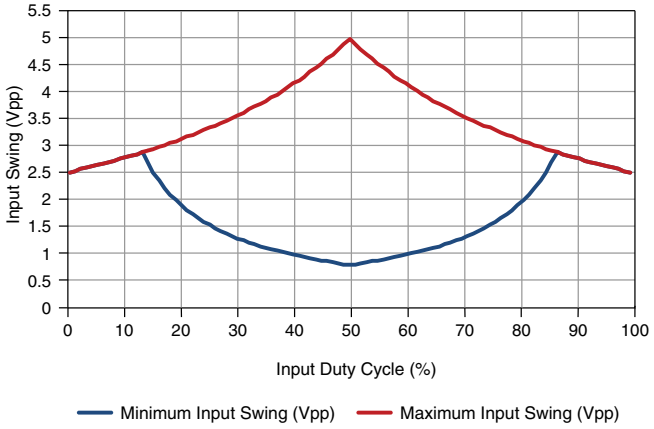
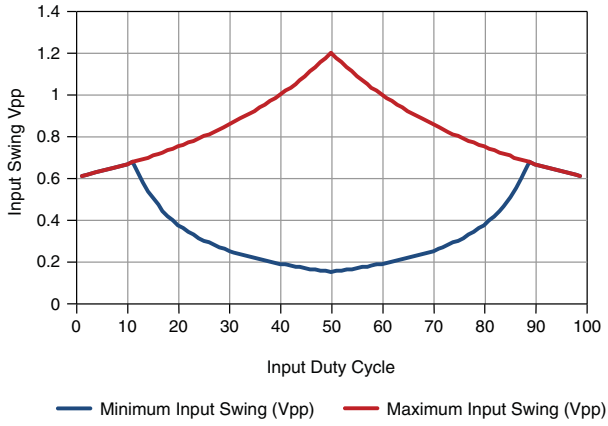


Figure 3. Maximum and Minimum Input Swing with Attenuation Off



Minimum Frequency	1 MHz[1]
Maximum Frequency	
To Clk10PLL	100 MHz
To FPGA	200 MHz
To PXIe-DStarA	1 GHz
ClkIn to PXI_Clk10_In Delay (PLL not used)	
Typical at 25 °C	6.75 ns
Maximum over temperature	14.8 ns

ClkOut

	Low Speed ClkOut	High Speed ClkOut
Coupling	AC Coupled	AC Coupled
Expected Termination	50 Ω or high impedance	50 Ω
Frequency Range	1 MHz to 50 MHz*	1 MHz to 1 GHz†
Typical Amplitude	2.57 V_{pp} into 50 Ω, 5 V_{pp} into high Z	800 mV_{pp}

[1] The minimum frequency is limited by AC coupling.

	Low Speed ClkOut	High Speed ClkOut
Rising/Falling Edge (20%, 80%)	270 ps, typical	180 ps typical
Duty Cycle of output with Clock Generation as source	45% to 55%	45% to 55%
Available Sources	PXI_CLK10, Clock Generation up to 50 MHz	Clock Generation, PXIe-DStarA
* Operation of low speed ClkOut above 50 MHz is possible, however, NI does not guarantee performance. Use ClkOutLS as the destination terminal to force NI-Sync to use the low speed driver above 50 MHz. † Operation above 1 GHz is possible but NI does not guarantee performance.		

PXI_CLK10 to ClkOut Delay

Typical at 25 °C	20.2 nbs
Maximum over temperature	47.75 ns

Figure 4. Typical Low Speed ClkOut Amplitude Performance (Sample Size: 19 Modules)

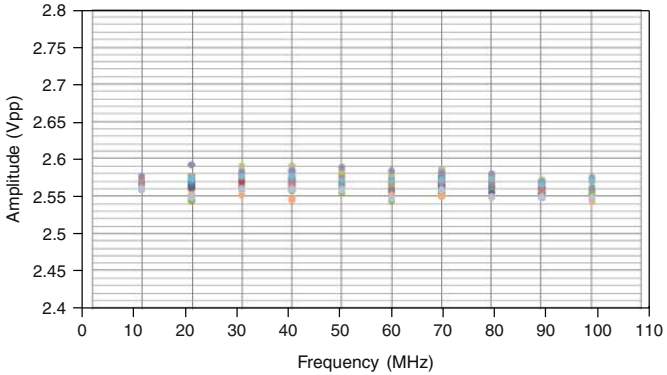
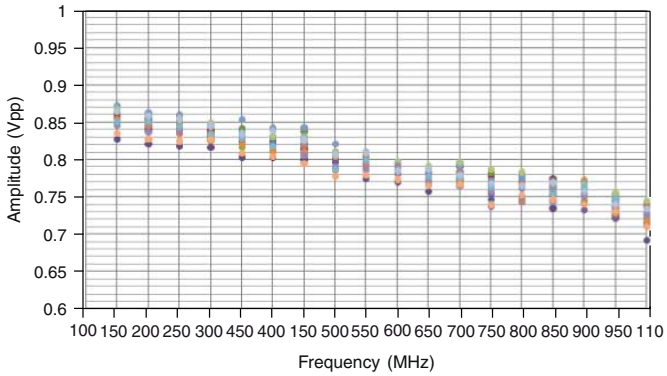


Figure 5. Typical High Speed ClkOut Amplitude Performance (Sample Size: 19 Modules)



Clock Generation

Reference Frequency Source[2]	PXIe_Clk100
Base Frequency Resolution (150 MHz to 300 MHz)	2.84217 μHz[3]
Minimum Generated Frequency[4]	
With FPGA divider	0.2794 Hz
Without FPGA divider	4.6785 MHz
Maximum Generated Frequency	1 GHz[5]

Clock Generation Phase Noise Performance

Note All Phase Noise Measurements were made on a Representative Module of various Clock Generation frequencies routed to ClkOut. All measurements made in a

[2] Frequency Accuracy is inherited from PXIe_Clk100/PXI_Clk10. Use OCXO for PXIe_Clk100/PXI_Clk10 replacement for improved frequency accuracy and phase noise.

[3] This is the frequency resolution of the DDS used in the Clock Generation circuitry. For Clock Generation frequencies below 150 MHz, this resolution is divided down and for frequencies above 300 MHz, this resolution is multiplied up.

[4] When routed to ClkOut Low Speed or used as a trigger synchronization clock, Clock Generation can be further divided by the FPGA by factors of two up to 24. This extends the Clock Generation range down to 4.6875 MHz/2^{24}=0.2794 Hz. When routed to ClkOut High Speed the minimum frequency is 4.6875 MHz. Use ClkOutHS as the destination terminal to force NI-Sync to use the low speed driver below 50 MHz. Note that AC coupling on ClkOut limits the minimum frequency which can be used.

[5] Clock Generation can be operated beyond the upper limit; however, NI does not guarantee performance beyond 1 GHz. 2 GHz is the maximum output frequency by design.

PXIe-1062 chassis with low fan speed and an OCXO connected to PXI_Clk10_IN using a PXIe-6674T.

The phase noise performance of the clock generation circuitry varies depending on what elements are used to generate the requested frequency. To generate frequencies above 300 MHz, a PLL is used to multiply the DDS frequency up which results in increased phase noise versus when the DDS is used directly (all frequencies below 300 MHz).

Figure 6. Phase Noise Performance

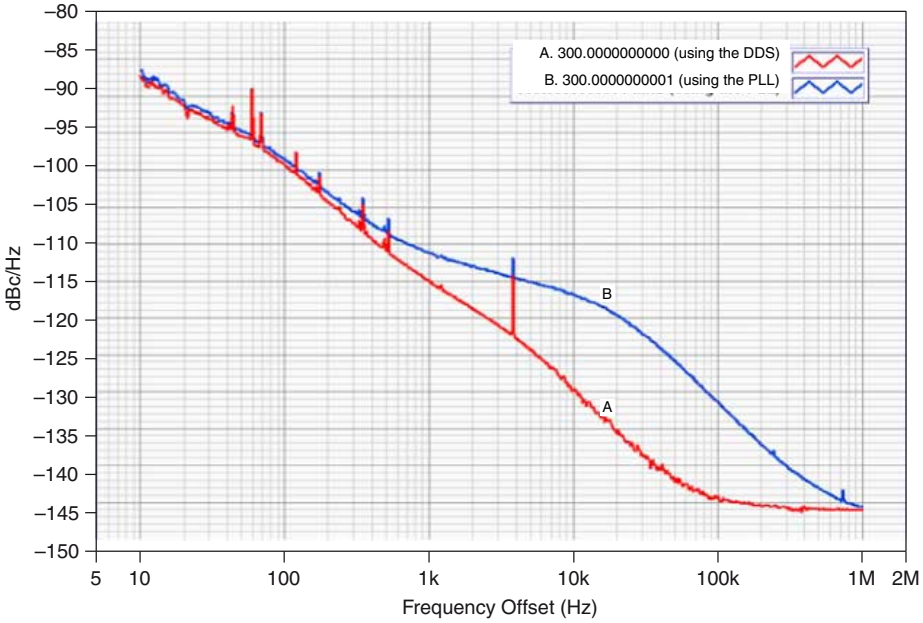
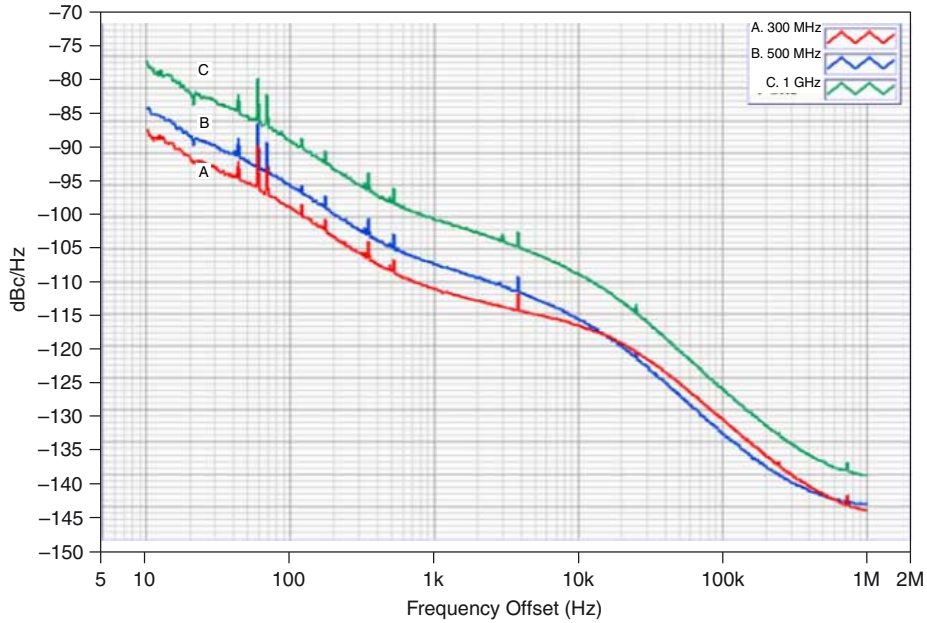


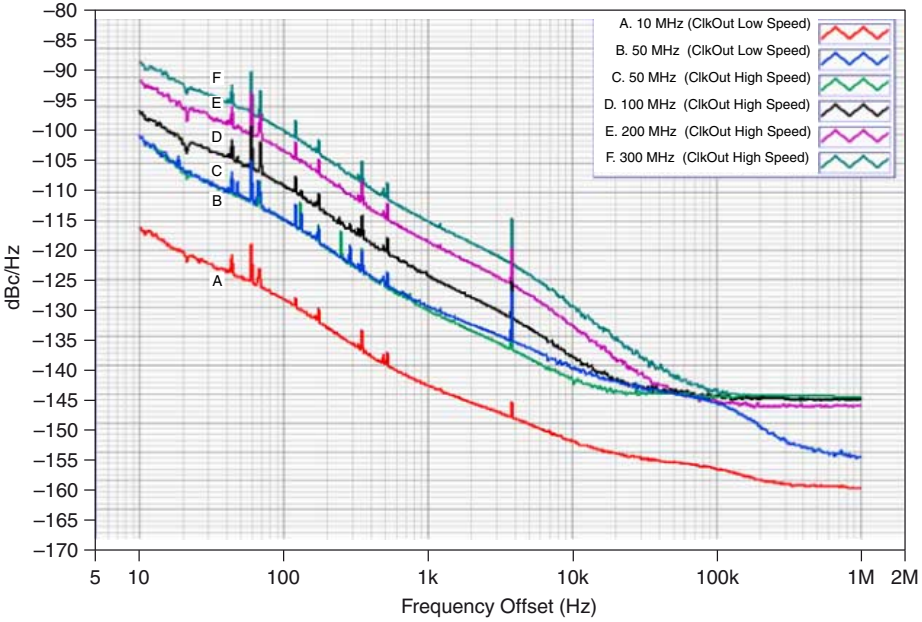
Figure 7. Phase Noise of Frequencies from the Multiplying PLL



At 50 MHz, NI-Sync software will automatically switch between the high speed and low speed ClkOut drivers[6]. The phase noise performance of these two drivers differs, as shown in the following figure:

[6] Use ClkOutHS as the destination terminal to force NI-Sync to use the high speed driver below 50 MHz.

Figure 8. Phase Noise Performance Between High Speed and Low Speed ClkOut Drivers



Triggers

PFI Single Ended

Table 2. Input Characteristics

Termination Setting	High Impedance	50 Ω
Input Impedance	10 kΩ, ±20%	50 Ω, ±5%
Input Coupling	DC	DC
Hysteresis	50 mV typical	58 mV typical (Revision D)‡‡ 53 mV typical (Revision E and later)‡‡
Adjustable Threshold Range	15 mV to 3.975 V	16.8 mV to 4.25 V (Revision D) ‡‡15.975 mV (Revision E and later) ‡‡

Table 2. Input Characteristics (Continued)

Adjustable Threshold Resolution	15 mV	16.8 mV (Revision D)‡‡15.975 mV (Revision E and later)‡‡
Adjustable Threshold Error*	±5 mV	±5 mV
Default Threshold Setting	1.005 V	1.008 V (Revision D)‡‡ 1.006 V (Revision E and later)‡‡
Minimum Input Voltage Swing†	400 mV_{pp}	450 mV_{pp}
Frequency Range ‡	DC to 150 MHz	DC to 150 MHz
Recommended Maximum Input Voltage Range	0.0 V to 5.0 V	0.0 V to 5.5 V
Maximum Input Voltage Range**	-0.5 V to 5.5 V	-0.5 V to 5.5 V
PFI Open Circuit Voltage††	0.45 V, typical	N/A

* PFI Input switching behavior is a function of both the threshold setting and hysteresis.

† Input Voltage Swing below 400 mV may be possible but performance is not guaranteed.

‡ Operation beyond 150 MHz frequency may be possible but performance is not guaranteed.

** Voltages beyond the maximum range may cause damage to the device.

†† PFI line will float to 0.45 V when configured in high impedance mode with no external signal connected as input.

‡‡ Ensure that the specifications of interest match the revision label on your board.

Table 3. Output Characteristics

Output Impedance	50 Ω, nominal
Output Coupling	DC
Output Voltage Range into 50 Ω load	0 V to 1.63 V, typical
Output Voltage Range into open load	0 V to 3.22 V, typical
Output Rising/Falling Edge into 50 Ω load	450 ps to 500 ps, 20% to 80%, typical
Maximum Output Frequency*	DC to 150 MHz
* Operation beyond 150 MHz frequency may be possible but performance is not guaranteed.	

Table 4. Input Characteristics

Minimum Differential Input Voltage	100 mV_{pp}
Recommended Maximum Differential Input Voltage*	1 V
Maximum Input Voltage Range†	0 V to 4 V
Differential Input Resistance	100 Ω, ±10%
Maximum Input Frequency‡	200 MHz

* Operation with greater voltage swing will not damage the device but performance characteristics are not guaranteed.

† Maximum Input Voltage Range is any combination of input voltage swing and common mode voltage. For example, a 200 mV differential swing with common mode voltage of 100 mV is acceptable as the lowest applied voltage to the input would be 0 V. A 200 mV differential swing with common mode less than 100 mV would cause the applied voltage to fall below 0V and therefore would not be acceptable.

‡ Operation beyond 200 MHz is possible but performance is not guaranteed. THis limitation comes from the FPGA, not the LVDS receiver.

Table 5. Output Characteristics

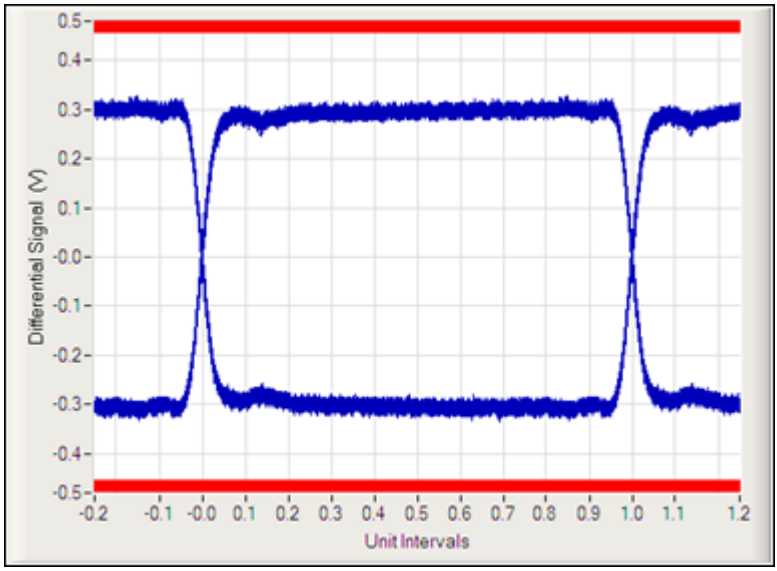
Differential Output Voltage into 100 Ω differential load (at DC)	600 mV_{pp} typical
Output Common Mode Voltage	1.125 V to 1.375 V
Maximum Output Frequency—Sourced from Clock Generation and PXIe_DSTARA*	1 GHz
Maximum Output Frequency—Sourced from FPGA†	200 MHz
Differential Rise and Fall Time	180 ps, typical

* Operation beyond 1 GHz is possible but performance is not guaranteed.

† Operation beyond 200 MHz is possible but performance is not guaranteed. This limitation comes from the FPGA, not the LVDS driver.

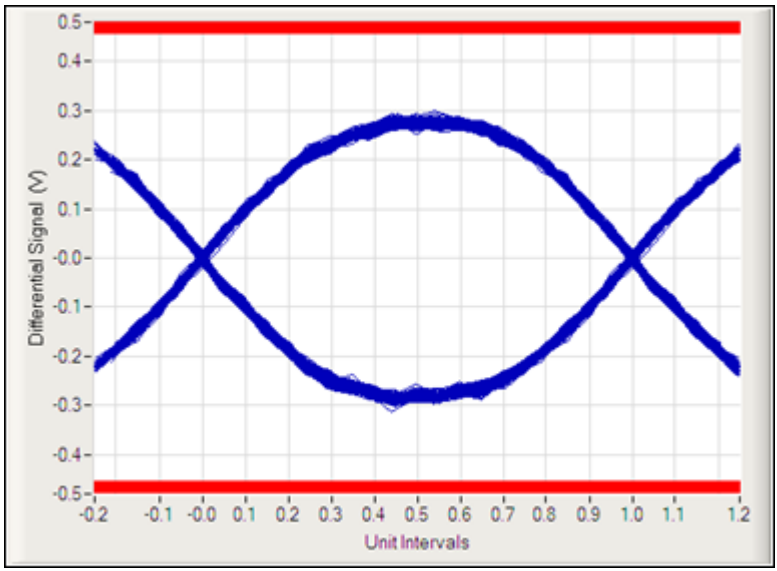
The following figure shows the representative LVDS output operating at 100 MHz. 1 unit interval in this figure equals 5 ns.

Figure 9. Representative LVDS Output at 100 MHz



The following figure shows the representative LVDS output operating at 1 GHz. 1 unit interval in the figure equals 500 ps.

Figure 10. Representative LVDS Output at 1 GHz



PXI-Triggers

I/O Voltage Level	3.3 V CMOS, 5 V input tolerant

PXI-Star

I/O Voltage Level	3.3 V CMOS, 5 V input tolerant

PXIe-DStarB

The PXIe-DStarB signals are LVDS signals that allow the PXIe-6674 to receive high speed trigger signals from the system timing slot module. Each PXI Express slot in a chassis has its own PXIe-DStarB connection with the System Timing Slot.

Maximum operating frequency	200 MHz

PXIe-DStarC

The PXIe-DStarC signals are LVDS signals that come from peripheral PXI Express slots in a chassis. Each PXI Express slot in a chassis has a PXIe-DStarC connection with the System Timing Slot. The PXIe-6674 can route signals to PXIe-DStarC.

Maximum operating frequency	200 MHz

Trigger Timing

Asynchronous Trigger Delays and Skew

Table 6. Asynchronous Trigger Delays and Skew Values

Trigger Source	Trigger Destination	Typical Delay*	Typical Skew†
Single Ended PFI	Single Ended PFI	18.9 ns	<0.5 ns
Single Ended PFI	LVDS PFI	17.7 ns	<0.5 ns
Single Ended PFI	PXI-Trigger	34.6 ns	<1.5 ns
Single Ended PFI	PXI-Star	23.0 ns	N/A
Single Ended PFI	PXIe-DStarC	11.8 ns	N/A
LVDS PFI	Single Ended PFI	12.2 ns	<0.5 ns
LVDS PFI	LVDS PFI	10.3 ns	<0.5 ns
LVDS PFI	PXI-Trigger	27.4 ns	<1.5 ns
LVDS PFI	PXI-Star	15.9 ns	N/A
LVDS PFI	PXIe-DStarC	11.8 ns	N/A

Table 6. Asynchronous Trigger Delays and Skew Values (Continued)

Trigger Source	Trigger Destination	Typical Delay*	Typical Skew†
PXI-Trigger	Single Ended PFI	16.9 ns	<0.5 ns
PXI-Trigger	LVDS PFI	15.7 ns	<0.5 ns
PXI-Trigger	PXI-Trigger	31.1 ns	<1.5 ns
PXI-Trigger	PXI-Star	19.4 ns	N/A
PXI-Trigger	PXIe-DStarC	14.5 ns	N/A
PXI-Star	Single Ended PFI	15.1 ns	<0.5 ns
PXI-Star	LVDS PFI	13.9 ns	<0.5 ns
PXI-Star	PXI-Trigger	28.9 ns	<1.5 ns
PXI-Star	PXIe-DStarC	13.6 ns	N/A
PXIe-DStarB	Single Ended PFI	11.8 ns	<0.5 ns
PXIe-DStarB	LVDS PFI	10.5ns	<0.5 ns
PXIe-DStarB	PXI-Trigger	25.7 ns	<1.5 ns
PXIe-DStarB	PXI-Star	14.0 ns	N/A

* Typical Delay is measured from the input to the NI PXIe-6674 at the connector to the output at the connector. For example, Single Ended PFI to PXI-Star is the delay from the Single Ended PFI SMA connector to the PXI-Star at the backplane connector.

† Typical Skew is defined as the difference in arrival time of a rising edge on a common source to two or more outputs with in a trigger destination, as seen as the connector. For example, if Single Ended PFI(0) is asynchronously routed to all PXI-Trigger lines, the typical skew would be less than 1.5 ns.

Synchronized Trigger PXI_Clk10 to Out

Table 7. Synchronized Trigger PXI_Clk10 to Out

Trigger Destination	Clock to Out Time*
Single Ended PFI	10.1 ns Typical, 19.9 ns Max
LVDS PFI	8.9 ns Typical, 14.8 ns Max
PXI-Trigger	23.4 ns Typical, 28.2 ns Max

Table 7. Synchronized Trigger PXI_Clk10 to Out (Continued)

Trigger Destination	Clock to Out Time*
PXI-Star	11.9 ns Typical, 22.5 ns Max
PXIe-DStarC	8.9 ns Typical, 14.0 ns Max
*Clock to Out Time is the amount of time it takes for a logic change on a synchronous trigger to appear (at the connector) with respect to the rising edge of PXI-Clk10 (at the backplane connector) that it is synchronized to.	

Synchronized Trigger Setup and Hold Timing with Respect to PXI-Clk10

Table 8. Synchronized Trigger Setup and Hold Timing with Respect to PXI_Clk10

Trigger Source	Trigger Destination	Setup Time*	Hold Time†
Single Ended PFI	Single Ended PFI	7.9 ns Typical, 14 ns Max	-6.3 ns Typical, 0.6 ns Max
Single Ended PFI	LVDS PFI	8.2 ns Typical, 14.3 ns Max	-5.9 ns Typical, 0.2 ns Max
Single Ended PFI	PXI-Trigger	9.3 Typical, 14.4 ns Max	-7.9 ns Typical, 0.3 ns Max
Single Ended PFI	PXI-Star	8.4 ns Typical, 14 ns Max	-7.7 ns Typical, 0.6 ns Max
Single Ended PFI	PXIe-StarC	9.6 ns Typical, 15.6 ns Max	-8.7 ns Typical, -.05 ns Max
LVDS PFI	Single Ended PFI	0.8 ns Typical, 3.6 ns Max	0 ns Typical, 4.2 ns Max
LVDS PFI	LVDS PFI	0.5 ns Typical, 3.4 ns Max	-.01 ns Typical, 4.1 ns Max
LVDS PFI	PXI-Trigger	1.6 ns Typical, 4.7 ns Max	-0.8 ns Typical, 4 ns Max
LVDS PFI	PXI-Star	1.1 ns Typical, 3.9 ns Max	-0.8 ns Typical, 4 ns Max
LVDS PFI	PXIe-DStarC	2.7 ns Typical, 6.1 ns Max	-1.5 ns typical, 2.3 ns Max

Table 8. Synchronized Trigger Setup and Hold Timing with Respect to PXI_Clk10 (Continued)

Trigger Source	Trigger Destination	Setup Time*	Hold Time†
PXI-Trigger	Single Ended PFI	9.8 ns Typical, 17.8 ns Max	-7.8 ns Typical, -5 ns Max
PXI-Trigger	LVDS PFI	9.7 ns Typical, 18.6 ns Max	-8.5 ns Typical, -5.7 ns Max
PXI-Trigger	PXI-Trigger	9.1 ns Typical, 17.4 ns Max	-7.3 ns Typical, -4.7 ns Max
PXI-Trigger	PXI-Star	8.8 ns Typical, 17.1 ns Max	-8 ns Typical, -4.5 ns Max
PXI-Trigger	PXIe-DStarC	8.5 ns Typical, 17 ns Max	-7.3 ns Typical, -4.6 ns Max
PXI-Star	Single Ended PFI	3.9 ns Typical, 10.5 ns Max	-.3 ns Typical, -0.2 ns Max
PXI-Star	LVDS PFI	4.3 ns Typical, 11.6 ns Max	-3.9 ns Typical, -1.2 ns Max
PXI-Star	PXI-Trigger	3.5 ns Typical, 10.9 ns Max	-2.3 ns Typical, -0.5 ns Max
PXI-Star	PXIe_DStarC	3.9 ns Typical, 10.7 ns Max	-3.6 ns Typical, -0.5 ns Max
PXIe-DStarB	Single Ended PFI	0.8 ns Typical, 3.2 ns Max	0 ns Typical, 4.2 ns Max
PXIe-DStarB	LVDS PFI	0.9 ns Typical, 4.2 ns Max	-0.3 ns Typical, 3.2 ns Max
PXIe-DStarB	PXI-Trigger	0.7 ns Typical, 3.5 ns Max	-0.2 ns Typical, 3.9 ns Max
PXIe-DStarB	PXI-Star	1.3 ns Typical, 3.3 ns Max	-1.1 ns Typical, 4 ns Max

Table 8. Synchronized Trigger Setup and Hold Timing with Respect to PXI_Clk10 (Continued)

Trigger Source	Trigger Destination	Setup Time*	Hold Time†
PXIe-DStarB	PXIe-DStarC	0.5 ns Typical, 3.3 ns Max	-0.3 ns Typical, 3.9 ns Max

* Setup Time is the amount of time before a rising edge of PXI-Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update.

† Hold Time is the amount of time after a rising edge of PXI-Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update.

FPGA Functionality

Trigger Routing

The following table shows the signal routes that can be made.

Figure 11. Sources and Destinations for NI PXIe-6674 Signal Routing Descriptions

			Destinations					
			Front Panel			Backplane		
			CLKOUT	PFI <0..5>	PFI_LVDS <0..2>	PXI_STAR Peripheral	PXI_TRIG <0..7>	DSTARC Peripheral
Sources	Front Panel	CLKIN	✓	✓†	✓†	✓†	✓†	✓†
		PFI<0..5>		✓	✓	✓	✓	✓
		PFI_LVDS <0..2>		✓	✓	✓	✓	✓
	Backplane	PXI_ CLK10	✓	✓†	✓†	✓†	✓†	✓†
		PXI_ CLK100		✓†	✓†	✓†	✓†	✓†
		PXI_STAR Peripheral		✓	✓	✓	✓	✓
		PXI_TRIG <0..7>		✓	✓	✓	✓	✓
		DSTARA Peripheral	✓		✓			
		DSTARB Peripheral		✓	✓	✓	✓	✓
	Onboard	Clk Gen	✓	✓†	✓	✓†	✓†	✓†
		Global Software		✓	✓	✓	✓	✓

† Routing PXI_CLK10, PXIe_CLK100, or ClkGen is accomplished by setting the synchronization clock (NI-Sync Property Node) to the desired clock source and then routing the synchronization clock as the source.

	Route made through the FPGA.
	Route to PFI_LVDS can be made through the FPGA when used as a trigger, or through the PXIe-DTARA network when used as a clock.

Frequency Measurement

Maximum Measurable Frequency[7]	200 MHz
Reference Counter Source[8]	PXIe-Clk100
Frequency Counter Sources	All Trigger inputs plus Clock In

[7] Operation beyond 200 MHz is possible but performance is not guaranteed.

[8] Accuracy of frequency measurement is relative to the frequency accuracy of the reference counter source. The Measure Frequency function in NI-Sync does not account for error from the reference source.

Trigger Sync Clock

Two independent synchronization clock zones:

- Front Synchronization Clock for PFI Single Ended and PFI LVDS
- Rear Synchronization Clock for PXI-Star, PXI-Trigger, and PXIe-DStarB

Synchronization Clock Sources	PXI_Clk10, PXIe_Clk100, Clock In, and Clock Generation

Two division ratios can be specified in powers of 2 from 2 to 512. These ratios are used in all synchronization clock zones to divide down the selected full speed synchronization clock.

Physical

Chassis requirement	One 3U PXI Express slot
Dimensions (not including connectors)	16 cm × 10 cm (6.3 in. × 3.9 in.)
Front panel connectors	Eight SMA female, 50 Ω
Front panel indicators	Two tricolor LEDs (green, red, and amber)
Weight	315 g (11.1 oz)

Power Requirements

+3.3 V	2.54 A, max
+12 V	2.25 A, max
+5 V_{AUX}	0 A, max

Environmental

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 to 55 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Storage Environment

Ambient temperature range	-40 to 71 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Shock and Vibration

Operating Shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
Random Vibration	
Operating	5 to 500 Hz, 0.3 g_{rms}
Nonoperating	5 to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Caution Clean the PXIe-6674 module with a soft, nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Note Specifications are subject to change without notice.

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Note For EMC declarations and certifications, and additional information, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit *ni.com/certification*, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at *ni.com/environment*. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers This symbol indicates that waste products should be disposed of separately from municipal household waste according to WEEE Directive 2002/96/EC of the European Parliament and the Council on waste electrical and electronic equipment (WEEE). All products at the end of their life cycle must be sent to a WEEE collection and recycling center. Proper WEEE disposal reduces environmental impact and the risk to human health due to potentially hazardous substances used in such equipment. Your cooperation in proper WEEE disposal will contribute to the effective usage of natural resources. For information about the available collection and recycling scheme in a particular country, go to *ni.com/environment/weee*.

电子信息产品污染控制管理办法（中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

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