PRELIMINARY

TECHNICAL MANUAL

OPERATION AND MAINTENANCE INSTRUCTIONS

OPERATIONAL LEVEL

VHF TRANSCEIVER

ATC-100

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PRELIMINARY

RECORD OF CHANGES

CHANGE	DATE	TITLE OF BRIEF DESCRIPTIONS	ENTERED BY

PRELIMINARY

FOREWORD

SCOPE

This manual contains information to obtain best performance from the ATC-100 transceiver. The information includes: a general description of the equipment, preparation for use and installation instructions, operating instructions, general theory of operation, maintenance instructions, preparation for reshipment, storage, and parts list.

PROPRIETARY DATA

CORRECTION NOTICE

Information contained in this document is believed to be correct as of the publication date. If a variation is noted between the information in this manual and the equipment in your possession, contact the factory for clarification. Future issues will be updated if necessary.

RIGHTS RESERVED

TABLE OF CONTENTS

TABLE OF CONTENTS - Cont.

LIST OF ILLUSTRATIONS

LIST OF TABLES

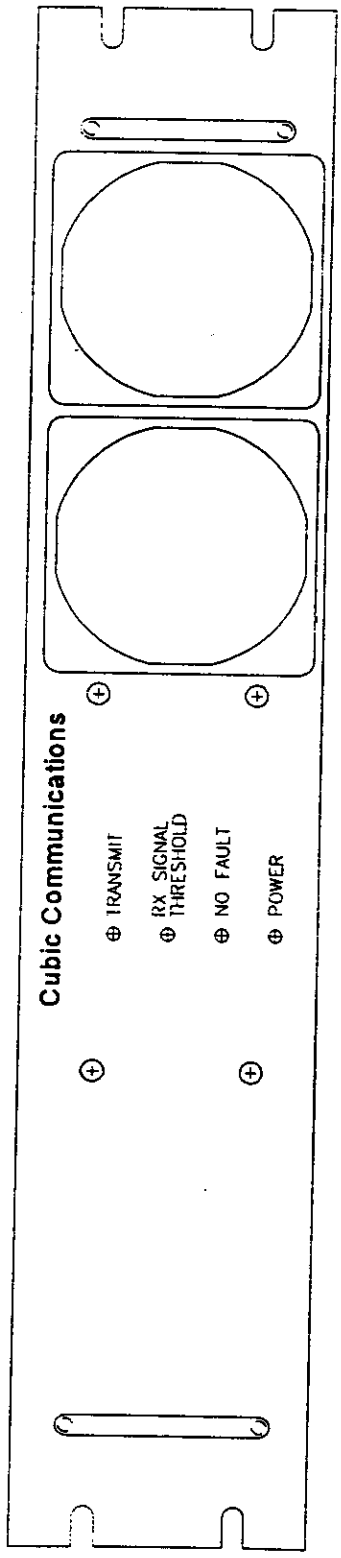


Figure 1-1 ATC-100 Front View.

CHAPTER 1
GENERAL DESCRIPTION

1-1 INTRODUCTION.

This chapter contains an equipment description, equipment supplied and required, storage data, tools and test equipment, and a summary of safety precautions.

1-2 EQUIPMENT DESCRIPTION.

The ATC-100 Transceiver (figure 1-1) is a superheterodyne design using digital signal processing (DSP) in the final IF and direct I&Q digital modulation in transmit. The DSP gives superior accuracy and flexibility for both modulation and demodulation. The ATC 100 has a frequency range from 118 MHz to 136.975 MHz with 25 kHz channel spacing. The Transceiver is fully interoperable with the present AM voice mode used in the ATC services. The transceiver can also be upgraded to Modes 1 - 4.

The transceiver contains circuit card assemblies and modules mounted in a 19 by 3½ by 16-inch rack-mount chassis.

The transceiver is controlled through a remote interface by any suitable bus controller using either an RS-232, or RS-485 serial interface bus, using specific command messages to request status or change conditions of the transceiver. There are four LED indicators on the front panel which provide transmit, breaking squelch, fault, and power status.

The audio output and input is available on the 600-ohm balanced line, through the rear Audio 15 pin sub D connector.

Either an internal or external reference frequency may be used. The external reference frequency is automatically sensed and used when connected to the rear panel.

1-3 SPECIFICATIONS.

Refer to table 1-1 for specifications of the equipment.

1-4 EQUIPMENT FURNISHED.

Table 1-2 lists the items furnished, items required but not furnished, and optional items.

1-5 STORAGE DATA.

Refer to Chapter 7 for storage data.

1-6 TOOLS AND TEST EQUIPMENT.

Table 1-3 lists recommended tools and test equipment for operational level maintenance. There are no special tools or test equipment required.

1-7 SAFETY PRECAUTIONS.

Safety precautions are presented in this manual preceded by the word WARNING or CAUTION just prior to the point where the hazard is likely to be encountered. Warnings and cautions are defined as follows:

WARNING

Refers to a procedure or practice that, if not correctly followed, could result in injury, death, or long term health hazard.

CAUTION

Refers to a procedure or practice that, if not correctly followed, could result in equipment damage or destruction.

Table 1-1 ATC-100 Specifications.

Item	Specification
FREQUENCY	
Tuning Range	118 MHz - 136.975 MHz
Tuning Time	Can tune to any of the 25 kHz channels within 100 ms
Channel Spacing	25 kHz
Frequency Stability	2 ppm (-20°C to 50°C) after a 4 minute warmup
External Reference Frequency	10 MHz (Automatically switches to external reference when external reference signal is applied)
DETECTION MODES	Mode 0: 300 Hz to 3.4 kHz (Data with external modem) Mode 1, 2, 3, & 4 upgradable
RF SECTION	
Antenna Impedance	50 ohms nominal
Antenna VSWR	1.5:1 (typical) 2.0:1 (maximum)
Sensitivity	-97 dBm (Mod 0, 30% AM)
Protection	Will not suffer permanent damage when subject to a signal of +21 dBm in-band, or +27 dBm out-of-band.
Preselection	4 Selectable bandpass filters with an additional FM Reject filter.
RECEIVER FUNCTION (Mode 0)	
Channel Spacing	25 kHz
Control	Remote RS232/485
Type of Modulation	AM (A3E) for voice
Sensitivity: For (S+N)/N = 10 dB, weighted to Psophometric filter, 1 kHz, Mod = 30% DSP IF bandwidth/selectivity with 25 kHz channel spacing: 6 dB/80 dB	-97 dBm typical ≥15 kHz/≤ 50 kHz
AF Outputs: Impedance Frequency Range: 25 kHz spacing Frequency response pass band Frequency response stop band	600 Ohms 300 to 3400 Hz + 1 dB/-2 dB referred to 1 kHz -10 dB at 100 Hz /6000 Hz referred to 1 kHz

Table 1-1 ATC-100 Specifications-Cont.

Item	Specification
AF Control: RF AGC; for input voltages -107 dBm to -7 dBm, 30% mod, 1 kHz	+ 1 dB/-3 dB referred to -47 dBm input
Harmonic distortion: For 90% AM, 1 kHz, -87 dBm to -7 dBm EMF Ultimate S/N ratio, 60% AM, 1 kHz (Weighted to Psophometric filter)	≤ 5% ≥ 50 dB
Squelch:	Programmable C/N = 0-99 dB, Level -103 dBm to 0 dBm
Squelch Response Time	≤ 10 msec
TRANSMIT FUNCTION (MODE 0)	
Channel Spacing	25 kHz
Control	Remote RS-232/485
TX Channel Characteristics	Frequency offset, power (high/low)
Load VSWR Capacity	Operates into any passive load
Transmitter Distortion	Distortion at 90% AM does not exceed 10% over the frequency range 600 Hz to 6 kHz
Spurious Emissions	When the transmitter is modulated and terminated in a resistive load equal to the nominal output impedance, the power of any spurious emission at the output of the transmitter does not exceed: 80 dB below carrier for 25 kHz <|f| < 500 kHz 90 dB below carrier for |f| > 500 kHz (non-harmonic) 80 dB below carrier, harmonically related
Wide Band Noise	Noise power measured on an unmodulated Carrier shall be less than -135 dBc/Hz at f = ± 500 kHz from center frequency and decreases at the rate of not less than 5 dB per octave to at least -150 dBc/Hz
Modulation	AM (A3E) (up to 90%)
RF Carrier Power	Unmodulated carrier 25W
P_{high} and P_{low}	Set in 1 watt increments
Operation	Continuous with single fan (auto temperature sense)
Backdoor Intermodulation	>15 dB below interfering signal at -20 dBc
Frequency Response	@ 25 kHz 300 to 3400 Hz: ≤ 4 dB (+1, -3 dB/ref 1 kHz) ≤ -19 dB at 100 Hz: ≤ -20 dB at 5000 Hz

Table 1-1 ATC-100 Specifications-Cont.

Item	Specification
Harmonic Distortion (@ 90%mod)	Line <10%
Audio Level Control (ALC)	Automatic ALC holds level modulation within 1 dB over 30 dB input range.
Ultimate SNR (weighed to Psophometric filter)	≥ 45 dB (mod = 90% at f_m = 1 kHz)
Test Generator	Built-in 1 kHz tone for test remotely controllable
GENERAL DATA	
Power Requirements	90 - 260 VAC, 47 -63 Hz, 225 W
Dimensions	19" (48.26 cm) wide, 3.5" (8.89 cm) high, 16" (40.64 cm) deep
Weight	16.7 lbs. (6.2 kg) (Unpackaged)
Temperature Range	-20 to +50°C Operating, -20 to +70°C Storage.
BITE	Internal diagnostics provide 95% of fault detection. Fault detectors continuously monitor voltage levels and phase lock. Serial BUS messages regarding BITE control and status are available by using the Radio Command and Status Message listed in Chapter 3. *Remote BITE Test provides Forward Power, Reflected Power, VSWR, Modulation Percentage & Sensitivity Measurements.*
Reliability	50,000 hours MTBF
OPTIONS	
DC Power	20V to 32V negative pole to ground

Table 1-2 Items Furnished.

Part No.	Nomenclature	Furn./Optl.
3003-1000?-XX	ATC-100 VHF Transceiver	Furn.
696-012	AC power cord	Furn.
3003-1021-1	Technical manual	Furn.
222-026	Bracket Slide (adj pair)	Optl. Not furnished
222-023	Slide (Non-tilt pair)	Optl. Not furnished
[1]XX indicates model number and factory installed options. Refer to identification plate on equipment.		

Table 1-3 Recommended Tools and Test Equipment (Or Equivalent).

Part No.	Nomenclature	Manufacturer
-	Screwdriver, Phillips 6 inch, No. 1	Any
-	Screwdriver, Phillips 6 inch, No. 2	Any
-	Driver, nut, 1/4 inch	Any
-	Wrench, open end, 5/16 inch	Any
-	Wrench, open end, 9/16 inch	Any
-	Engage/Disengage OSMT Cable Tool	Any
HP8642B	RF signal generator	Hewlett Packard
465B	Oscilloscope	Tektronix
8050A	Digital multimeter (true RMS)	Fluke
HP5381A	Frequency counter[1]	Hewlett Packard
HP8568B	Spectrum analyzer[1]	Hewlett Packard
HP8903	Audio analyzer[1]	Hewlett Packard
[1]Optional		

CHAPTER 2
PREPARATION FOR USE AND INSTALLATION INSTRUCTIONS

2-1 INTRODUCTION.

This chapter contains unpacking, inspection, installation, connections, and initial alignment procedures.

2-2 UNPACKING AND INSPECTION.

To unpack and inspect the transceiver for damage, perform the following procedures:

WARNING

Do not drop the equipment when lifting or carrying. Personnel injury or equipment damage may occur.

1. Inspect the shipping carton for damage before unpacking the transceiver.

NOTE
If the carton is damaged, open the carton in the presence of a shipping carrier agent if possible. If damage is found after the transceiver is unpacked, retain the carton and packing materials for inspection.

2. Open the carton and remove the foam packing material on top of the transceiver.

3. Lift the transceiver from the carton.

NOTE
Save carton for possible reshipment.

4. Inspect the transceiver for external damage including dents and scratches.

CAUTION

Do not attempt to operate the transceiver if major damage is found.

2-3 INSTALLATION.

The transceiver is designed for 19-inch rack mount operation in a relatively dust free environment with an ambient temperature range between -20 and +50°C. Optional slides may be provided for the ATC-100. Follow the instructions provided with the slides for installation.. No special tools or additional materials are required for installation.

NOTE
See figure FO-1 for clearance requirements and mounting details.

2-4 CONNECTIONS.

Refer to table 2-1 for a description of the rear panel connections, (see figure 2-1.)

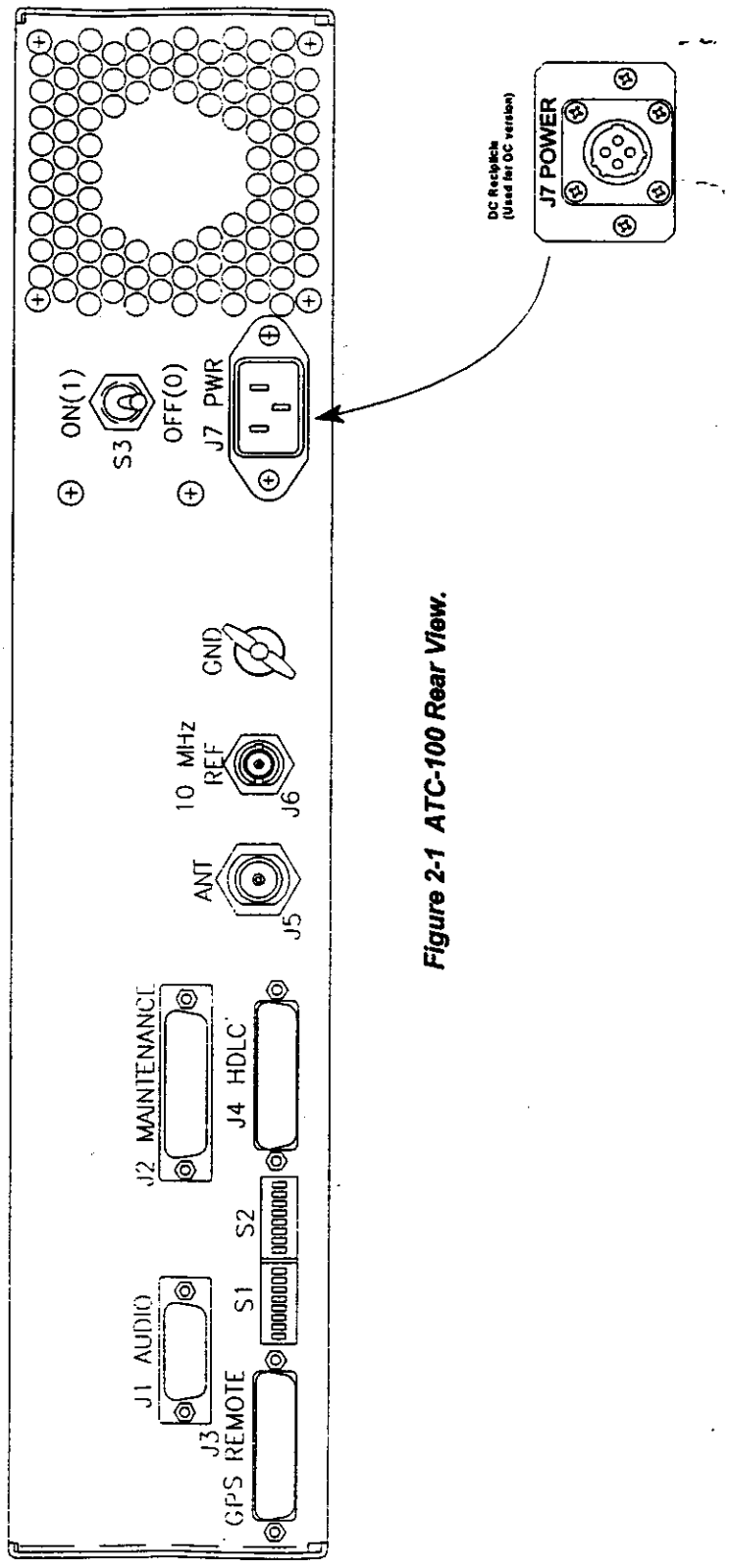


Figure 2-1 ATC-100 Rear View.

Table 2-1 Rear Panel Connections.

Name	Connector On Unit	Recommended Mating Type	Description
AUDIO (J1)	15-pin "D" subminiature male (324-009)	15-pin "D" subminiature female (324-070)	Used to connect audio to remote controller or other equipment. Table 2-2 lists the pin descriptions. For units that have the optional Audio Daughter Board, the Audio Interface is transformer coupled with center tap available. The pin descriptions for the optional Audio Interface are describe in Table 2-2a.
MAINTENANCE (J2)	25-pin male D subminiature connector.	25-pin female D sub-miniature connector	Table 2-3 lists the pin descriptions.
GPS REMOTE (J3)	25-pin female D sub-miniature connector.	25-pin male D subminiature connector.	For external RS-232C or RS-485 remote control bus operation. Table 2-4 lists the pin descriptions. Refer to chapter 3 to set the serial bus configuration.
HDLC (J4)	25-pin female D sub-miniature connector.	25-pin male D subminiature connector.	Table 2-5 lists the pin descriptions.
ANTENNA (J5)	BNC Jack (344-246)	BNC Plug (Customer Option)	Coaxial antenna connection. Impedance is approximately 50 ohms with a VSWR less than 3 to 1 at the receiver tuned frequency.
REF (J6)	BNC Jack (344-246)	BNC Plug (Customer Option)	Reference frequency in. Used to connect 10 MHz external frequency standard. 50 ohms, 0 dBm ±3dB
AC POWER (J7)	IEC 320-C-13 (343-002)	NEMA 5-15P (696-012, Power Cord)	90 to 260 VAC, 47 to 63 Hz, single phase 250 watts max. Figure 2-2a shows the pin descriptions.
DC POWER (J7) (Optional)	AMP, INC. 206061-1 with 66361-4 contacts	AMP, INV 206060-1 with 66360-4 contacts (qty 4) & 206358-1 backshell	20V to 32V negative pole to ground. Table 2-6 lists the pin descriptions. Figure 2-2b shows the pin configuration
ON/OFF (S3)			Power Switch. ATC-100 power on/off.
DIP Switches (S1)			Used to set the bus address. Refer to figure 3-1 for proper switch settings.
DIP Switches (S2)			Used to set the Boot Normal, Bus Share & Type, BITS/Parity/Stop and Baud Rate. Refer to figure 3-1 for proper switch settings.
NOTE: Part numbers in parenthesis (000-000) indicate CCI part number if applicable.			

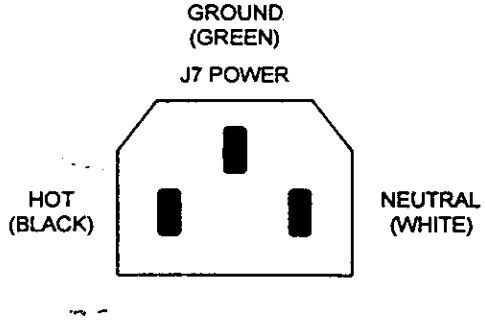


Figure 2-2a AC Power Connector (J7) Pin Descriptions. (Standard)

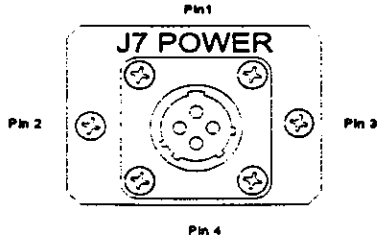


Figure 2-2b DC Power Connector (J7) Pin Descriptions. (Option)

Table 2-2 AUDIO Connector (J1) Pin Descriptions.

Pin	Signal	Remarks
1	AUDIO IN	
2	AUDIO IN RTN	
3	KEY	Ground for TX
4	AUDIO OUT	RSSI Analog Meter
5	AUDIO OUT RTN	RSSI Analog Meter
6	SIGNAL STRENGTH	
7- 9	NC	
10 & 11	GND	
12	NC	
13	GND	
14	NC	
15	GND	

Table 2-2a Optional AUDIO Interface Connector (J1) Pin Descriptions.

Pin	Signal	Remarks
1	AUDIO IN	
2	AUDIO IN RTN	
3	KEY	
4	AUDIO OUT	
5	AUDIO OUT RTN	
6	SIGNAL STR	
7	NC	
8	GND	
9	AUDIO IN CENTER	
10 & 11	GND	
12	AUDIO OUT CTR	
13	GND	
14	SIGNAL STR RTN	
15	GND	

Table 2-3 MAINTENANCE Connector (J2) Pin Descriptions.

Pin	Signal	Remarks
1	NC	
2	TXD	RS-232 Transmit Data
3	RXD	RS-232 Receive Data
4	RTS	RS-232 Request To Send
5	CTS	RS-232 Clear To Send
6	NC	
7	GND	Digital Ground
8-13	NC	
14	DO_RI	RS-485 Bus Input/Output +
15	DO_RI-	RS-485 Bus Input/Output -
16-25	NC	

NOTE: The pinout for the RS-232 interface follows the recommendations of the EIA standard. Since the EIA standard for RS-485 does not call out recommended pin assignments, these circuits are assigned to unused pins on the same connector as the RS-232 circuits.

Only one set of signals (RS-232 or RS-485) is active at any given time. The name "Transmitted Data" for RS-232 is synonymous with "Send Data" for RS-485. All circuits for the RS-485 interface consist of a differential pair of signal lines labeled A and B. Both lines must be connected to the circuit at the other end, A to A and B to B.

A receiver configured with the serial interface will operate as Data Terminal Equipment (DTE). This means that the circuits named Transmitted Data and Request to Send are outputs from the receiver and the circuits named Received Data and Clear to Send are inputs to the receiver. The electrical characteristics of the interface will conform to either EIA standard RS-232-C or EIA standard RS-485-A with the following exceptions.

When so configured from the rear panel DIP switches, the line drivers associated with the Transmitted Data and Request to Send circuits for the unit will be in a high impedance state except when that unit has been commanded by the system controller to transmit. When done transmitting, the line drivers will return to the high impedance state. This feature, referred to as bus sharing or party line operation, allows multiple receivers to share a single circuit for the Transmitted Data signal to the system controller. In systems where only one receiver is connected to the external controlling device, this feature may be disabled from the receiver rear panel switches.

The Request to Send (RTS) and Clear to Send (CTS) handshake circuits are generally not used when the line drivers are configured for bus sharing operation. When the line drivers are not configured for bus sharing, the operation of the CTS and RTS lines is as follows: When a receiver is ready to accept remote control commands it will set the RTS circuit true. When it has received a message and is processing the commands, it will set the RTS circuit false until it is ready to receive another command. The receiver will only transmit messages to an external device when its CTS circuit is held true by the external device. The external device may stop the transmitted output of the receiver (to prevent buffer overflow for example) by taking the CTS circuit false. When the CTS circuit is again taken true, the receiver will begin transmitting where it left off. NOTE: When bus sharing is enabled from the receiver rear panel switches, the state of the CTS circuit is ignored.

(CONTINUED)

NOTE (CONTINUED)

The number of ATC-100 transceivers that may be connected to a single controller is dependent on the serial bus type and the line driver characteristics of the controller, but in general is at least 10 transreceivers for RS-232 operation and at least 30 transceivers for RS-485 operation. The input resistance of the RS-232 line is approximately 5000 Ohms. The ATC-100 transceiver contains no termination resistors for the RS-485 bus.

If connected directly to a computer interface also configured as DTE, a reversal of transmit and receive data (TXD and RXD or SD and RD) and request to send and clear to send (RTS and CTS or RS and CS) lines may be necessary. The Request to Send and Clear to Send lines may be jumpered together on the mating connector if required by the system. These reversals or jumpers are normally not required if units are connected through a modem. If an ATC-100 transreceiver is to be connected to another DTE device as its controller, the circuits must be swapped for proper operation as follows:

ATC-100 Transeceiver		*Other DTE Device*
Transmitted Data	——>	*Received Data*
Received Data	<——	*Transmitted Data*
Request to Send	——>	*Clear to Send*
Clear to Send	<——	*Request to Send*
Signal Ground	——	*Signal Ground*

Table 2-4 GPS Remote Control Bus Connector (J3) Pin Descriptions.

Pin	Signal	Remarks
1	NC	
2	SD+	RS-485 Send Data Differential Output+
3	RD+	RS-485 Receive Data Differential Input +
4-6	NC	
7	GND	Digital Ground
8-13	NC	
14	SD-	RS-485 Send Data Differential Output -
15	NC	
16	RD-	RS-485 Receive Data Differential Input -
17 & 18	NC	
19	EXT_AGC0	External TTL AGC Reporting
20	NC	
21	EXT_AGC1	External TTL AGC Reporting
22	NC	
23	GPS_IPPS-	GPS 1 Pulse Per Sec. -
24	NC	
25	GPS_IPPS+	GPS 1 Pulse Per Sec. +

Note: This connector is reserved for future MODE 3 option.

Table 2-5 HDLC Connector (J4) Pin Descriptions.

Pin	Signal	Remarks
1	NC	
2	HDLC_TXD-	RS-485 Transmit Data Differential Output
3	HDLC_RXD-	RS-485 Receivet Data Differential Output -
4	HDLC_CTS-	RS-485 Request To Send Differential Input -
5	HDLC_RTS-	RS-485 Clear To Send Differential Output-
6	NC	
7	GND	Digital Ground
8	HDLC_DCD-	RS-485 Digital Carrier Detected Differential Output-
9 & 12	HDLC_RCLK-	RS-485 Receive Data Differential Clock Input-
10	HDLC_DCD+	RS-485 Digital Carrier Detected Differential Output+
11	HDLC_TLCK-	RS-485 Transmit Data Differential Clock Output.-
13	HDLC_RTS+	RS-485 Clear To Send Differential Output +
14	HDLC_TXD+	RS-485 Transmit Data Differential Output
15 & 17	HDLC_RCLK+	RS-485 Receive Data Differential Clock Input +
16	HDLC_RXD+	RS-485 Receive Data Differential Output+
18	NC	
19	HDLC_CTS+	RS-485 Request To Send Differential Input
20-23	NC	
24	HDLC_TCLK+	RS-485 Transmit Data Differential Clock Output +
25	NC	

Note: This connector is reserved for future MODE 2 and MODE 3 option.

Table 2-6 Optional DC Power Connector Pin Descriptions.

Pin	Signal	Remarks
1,2	+ DC Power In	20 - 32 VDC
3,4	-DC Power In	Chassis Ground

CHAPTER 3
OPERATING INSTRUCTIONS

The ATC-100 transceiver is remotely controlled via a serial interface on the Maintenance Port. The serial interface standards available for the ATC-100 transceiver are the unbalanced (RS-232) and balanced (RS-485) line interfaces.

Parameters associated with the remote control interface can be checked and changed from the rear panel of the transceiver. The bus address, bus type (RS-232 or RS-485), baud rate, bus sharing option, and line parameters may be set. (Line parameters include number of data bits, number of stop bits and parity options).

Each type of interface is described below.

3-1 REMOTE OPERATION USING SERIAL BUS.

The transceiver is operated under remote control using a serial bus and a suitable controller. Ensure that the communications parameters are set in accordance with the system requirements. The bus address, bus type (RS-232 or RS-485), baud rate, number of data bits, type of parity used, and number of stop bits must match the requirements of the system controller.

3-1.1 *ATC-100 Set Up.*

Before operating the equipment, set the DIP switches, on the rear panel, for correct remote operation (refer to figure 3-1). The factory default settings provide a starting point; where all DIP switches are OFF except for S-2(5) and S-2(7), which are ON to establish the baud rate at 38,400.

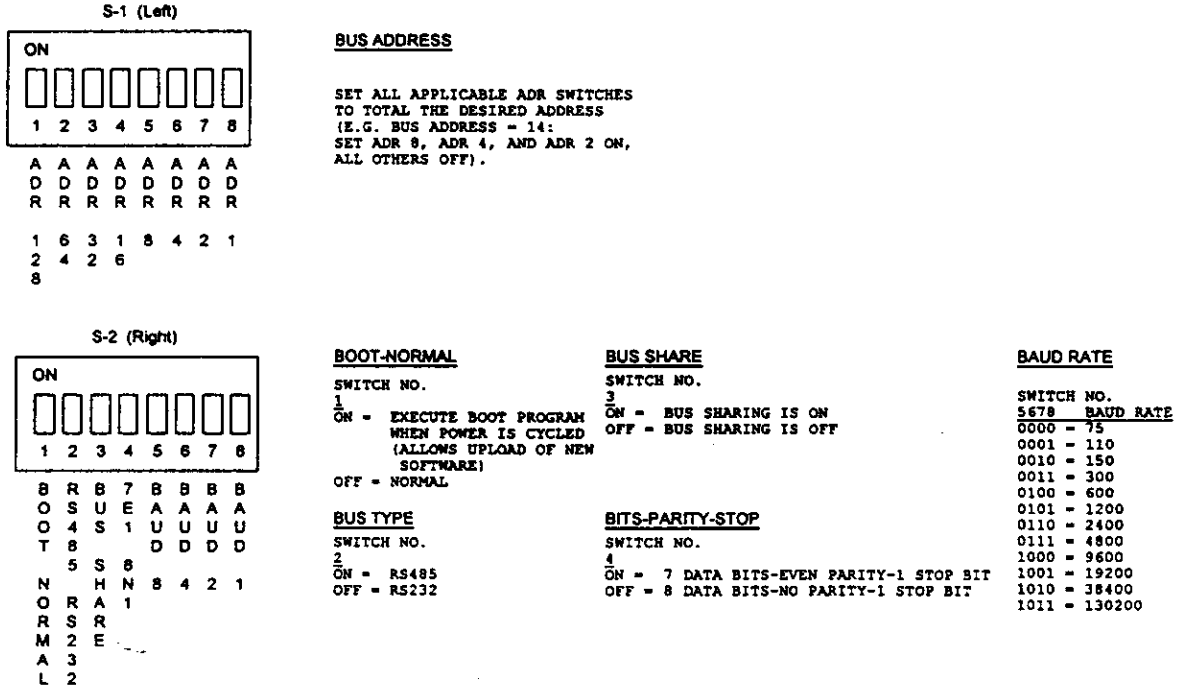


Figure 3-1 DIP Circuits - Switch Settings.

PRELIMINARY

3-1.2 *Software Installation Up Grade Procedures.* If it becomes necessary, the internal software may be upgraded by connecting the Maintenance Port to an IBM compatible PC running DOS or a DOS window under Windows™. Use the Cubic-furnished program RCOMM, and connect the computer serial port to the Maintenance Port with a suitable cable. In most cases a "Null Modem" cable or adapter is required. In some cases, a gender adapter is also required.

1. Verify that the DIP switches reflect the desired settings. In most cases the Factory Default settings will suffice, refer to paragraph 3-1.1.

2. Enter RCOMM and verify the settings. Select the Serial Interface: COM port 1 or 2 (Alt-I, 1 or 2). Then examine the serial line parameters at the bottom of the screen or window. If using the recommended Factory Default settings on the transceiver, use the following RCOMM settings:
   a. Baud Rate = 38,400
   b. Data Bits = 8
   c. No Parity
   d. Address = 0
   e. F/C (flow control) = OFF
   f. Terminator = <CR>
   g. Preamble = 1STX, 3ADR.

   If any parameters need to be changed, access the Configuration/Serial menu (Alt-C, S) and the parameter to be changed.

3. Verify communications with the transceiver by typing ID? and Return. You should see an ASCII message identifying the unit as an ATC-100 with a certain control software version and date.

4. Turn power to the ATC-100 transceiver OFF.

5. Set DIP switch S2-1 to ON (Boot Program)

6. Set the address on DIP switch S1 to 3 if uploading the Control program or 1 if uploading the DSP program.
   a. Address 3: S1-7 & S1-8 ON, others OFF
   b. Address 1: S1-8, all others (on S1) OFF.

7. Still in RCOMM, select the File Upload function (Alt-F, U) and enter the Path and Filename in the space provided. Conclude with *Enter*.

8. Turn the transceiver power ON. Upload should proceed with progress indications in the RCOMM screen. Press *Enter* after the display indicates the file has been transferred.

9. Repeat steps 4 to 8 for each program to be uploaded.

10. Turn off power to the transceiver.

11. Reset the address switch (S1) to the operational address.

12. Set DIP switch S2-1 to OFF (Normal).

13. Power on the unit. Set RCOMM to the transceiver's operational address. Verify the uploads using the ID? query for control software or IDD? for the DSP software.

3-1.3 *Serial Bus Description.* The serial interface includes both unbalanced (RS-232) and balanced (RS-485) line interfaces. The interface type must be set by the operator prior to power up via the DIP switches.

3-1.4 *Serial Bus Message Format.* All transmissions, in either direction, conform to the message format shown in figure 3-2. All transmitted and received characters will be encoded and interpreted as conforming to the ASCII character code.

Each character in the message is passed in an asynchronous serial format as shown in figure 3-3. The number of data bits, number of stop bits, parity options and baud rate are all selectable from the rear panel of the. These selections are stored in non-volatile memory. All characters are in ASCII code.

3-1.5 *Serial Bus Message Types.* All messages are divided into two major categories: command messages and status messages. Each category is discussed in the following paragraphs:

3-1.5.1 *Serial Bus Command Messages.* Command messages are sent from the controller to the transceiver and are subdivided into two classes as follows:

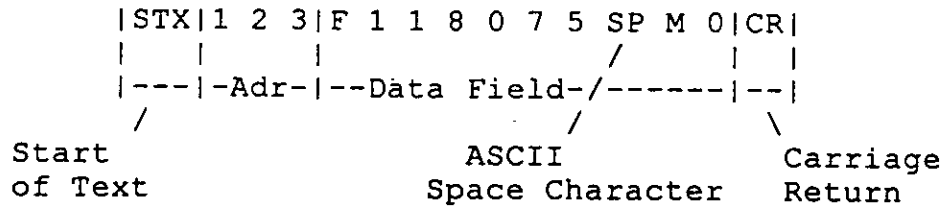
3-1.5.1.1 *Serial Bus Radio Command Messages.* Radio command messages contain commands that are passed to the transceiver. They may command the transceiver to change operational parameters or to report back operational status.

3-1.5.1.2 *Serial Bus Interface Command Messages.* Interface command messages contain commands that are acted upon by the communications interface in the transceiver. These commands cause the interface to change modes or report status.

3-1.5.2 *Serial Bus Status Messages.* Status messages are sent from the transceiver to the controller and are subdivided into two classes as follows:

3-1.5.2.1 *Serial Bus Radio Status Messages.* Radio status messages contain information about the operational status of the transceiver. These messages are sent as a reply to radio command messages that request a status report.

3-1.5.2.2 *Serial Bus Interface Status Messages.* Interface status messages contain error status information caused by a previous command message or other source. When the transceiver is in the acknowledge mode, it will respond to all command messages with an interface status message unless the command explicitly requested a status message.



NOTES:

The first character of a transmission will always be STX (start of text, ASCII code 02).

The second, third, and fourth characters will contain the address in decimal, with the most significant digit first, of the transceiver sending the transmission or to which it is being sent by the controller. The address code for any transceiver may be any number from 000 to 254 provided that it is not used by any other unit connected to the bus. Address 255 is reserved for "broadcasting" to all transceivers on the bus (refer to paragraph 3.1.8). The controller has no address. All three digits must be transmitted. Addresses less than 100 must be filled with '0' digits on the left. The address is set from the front panel with the soft key sequence CONFIG- REMOTE- ADDRS.

The fifth character of the transmission is the beginning of the data field. This field may contain as few as one or as many as 250 characters. The data field may contain one or more messages. If more than one message is contained in the data field, each message must be separated from the next by one or more blank (space) characters.

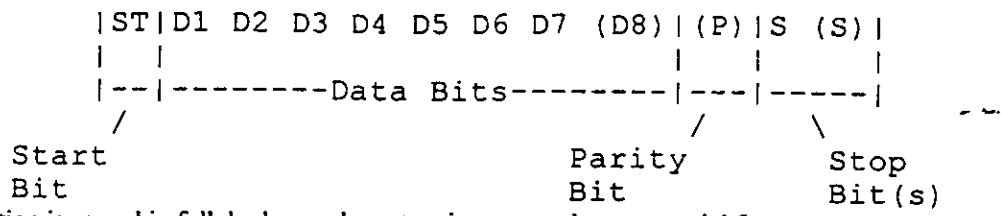
Any number of messages may be included in the data field provided that the maximum number of characters is not exceeded. There are, however, certain request for status commands that may not be mixed with any other request for status commands in the same transmission. These messages will be noted as such in table 3-3.

The final character of the transmission will be a CR (carriage return). This character will follow the last character of the data field.

This transmission above from the controller is addressed to the transceiver with address 123 and contains two messages: "F118075" and "M0".

When sending messages to the transceiver that require numeric values as arguments, it is not necessary to include leading zeros. For example, to send a message to change the manual gain reduction to 66 dB, the command message "G66" may be given in place of "G066". When a request for a status message is made, the reply will always include any leading zeros so that the value may be extracted by counting characters in the message.

Figure 3-2 Serial Bus Message Format.



NOTES: Information is passed in full duplex as characters in an asynchronous serial format. Each character consists of a start bit, 7 or 8 data bits with the least significant bit sent first, an optional parity bit which may provide odd or even parity, and one or two stop bits. The serial transmission rate may be set to each of the following standard rates: 75, 110, 150, 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, and 130200 bits per second. Number of data bits, number of stop bits, parity options and baud rate are all selectable from the front panel of the transceiver through the keypad from the CONFIG - REMOTE menu. The selected values take effect immediately when changed and are stored in non-volatile memory.

Figure 3-3 Serial Bus Character Format.

3-1.6 *Serial Bus Message Protocol.* The interface system operates in one of two modes: normal or acknowledge. These modes are selected by sending the transceiver the appropriate interface command message. Both modes are discussed in the following paragraphs:

3-1.6.1 *Serial Bus Normal Mode.* In Normal Mode the transceiver unit will process messages that are addressed to it but no response will be sent back unless the Command Message was a request for Status Message (Radio or Interface). The controller can verify that its Command Message(s) was received without error by sending a Command Message requesting a reply Status Message either immediately after sending the original Command Message, or after having sent Command Messages to other transceiver units. This mode allows the fastest throughput of commands to a large group of transceivers because the controller does not have to wait for each transceiver unit to process the message(s) before moving on to the next transceiver unit.

3-1.6.2 *Serial Bus Acknowledge Mode.* In Acknowledge Mode a transceiver unit will always respond to Command Messages with a Status Message after it has processed the Command Message. If the Command Message was for a reply Radio Status Message, and no errors or faults have been detected, the reply will be the requested Status Message. In all other cases, the transceiver unit will respond with an Interface Status Message. This mode reduces maximum throughput because the controller must wait for the reply Status Message before issuing another command, but it simplifies the controller's job when it wants to verify the reception of its Command Messages and maximum throughput is not needed.

3-1.7 *Line Driver Operation.* When Bus Sharing is enabled through the transceiver's front panel, that transceiver's Transmitted Data and Request to Send line drivers are maintained in a high impedance state at all times except when it is required for that unit to transmit. In Normal Mode operation, this only occurs when the unit has received a Command Message that requests a reply Status Message. In Acknowledge Mode, all commands will caused the addressed unit to transmit.

The line drivers will be turned on and placed into the mark state for at least one full character time before the first character (the STX) is transmitted.

3-1.8 *Broadcast Address.* All transceivers will respond to address 255 the same as its actual configured address. This is referred to as the broadcast address. If a single transmission is sent to this address, each transceiver on the bus will respond to the commands in the transmission as if they were sent to it individually. This feature may be used to cause a group of transceivers to act in unison, or to reduce the time it takes to initialize a group of transceivers to a set of common parameters.

The broadcast address must not be used to request status from a group of transceivers or when the transceivers are operating in the acknowledge mode, since this would cause bus contention as all transceivers would reply at the same time. With only one transceiver on the bus it is possible for the controller to determine the unit's address by sending a status request to the broadcast address and examining the address field in the reply, since the reply message contains the unit's configured address. This can be used during system integration as a troubleshooting aid.

3-1.9 *Serial Bus Message Definition.* All messages are ASCII encoded and inserted into the data field of transmissions as defined in paragraph 3-8.2. Messages from the controller may use lower or upper case for all alphabetic characters. The transceiver always uses upper case.

Each message that can be sent using the bus controller is listed in the following tables:

- o Table 3-1. Serial Bus Interface Command Messages.
- o Table 3-2. Serial Bus Interface Status Messages.
- o Table 3-3. Radio Command and Status Messages

Most Radio Status Messages use the same format as the Radio Command Message for that parameter. For example, the reply to the Radio Command Message "F?" (request current frequency setting) is "F123456" in the same format as the Radio Command Message to change the Frequency.

All Radio Status Messages are made up of fixed length strings so that values may be parsed by counting the characters of the Status Message. Messages which return a numeric value will be padded with zeros on the left to give the same number of characters as the same message with the maximum value. When more than one parameter is being reported, the individual parameters are separated by a blank (space) character.

Table 3-1 Serial Bus Interface Command Messages.

Message	Definition
:NORM	Set NORMAL interface mode
:ACKN	Set ACKNOWLEDGE interface mode
:?	Request Interface Status Message

Table 3-2 Serial Bus Interface Status Messages.

Message	Definition
OK:NORM	No errors, NORMAL Mode
OK:ACKN	No errors, ACKNOWLEDGE Mode
TE:EEPR	Testing error - EEPROM corrupted
TE:POST	Testing error - power on self test error
IE:OVFL	Interface error - buffer overflow
IE:IVAL	Interface error - illegal value
IE:UNKN	Interface error - unrecognized message
RE:FALT	Radio error - fault has been detected

Table 3-3 Radio Command and Status Messages.

Syntax	Reply	Description
An		Enable or disable Automatic Gain Control (AGC) operation. Replace the n with 1 to enable AGC operation or 0 to disable AGC operation. When AGC operation is disabled, the current Manual Gain setting is in effect. (Default is on.)
A?	An	Request current status of AGC (on or off). The n character is replaced with a 1 if AGC is enabled, or a 0 if AGC is disabled.
BI		Perform the built-in-test-equipment (BITE) test sequence. This command may take several seconds to complete. To see the results of the BITE test, send the BI? command.
BI?	Binnnn	Request the results of the last executed BITE test sequence. Each of the n characters represents one of the tests performed when the BITE sequence is performed and is replaced with a 1 to indicate that the test failed or a 0 to indicate that the test passed. Starting with the first (left most) n character, the definition of each test bit is as follows: Receive 120 MHz, Receive 125 MHz, Receive 130 MHz, Receive 135 MHz.
BG		Turns on BITE comb generator. The RSSI output must be disabled before giving this command after `RSSI0`. (Refer to `RSSI` commands.) The BITE generator will be turned off with any of several other commands, including the change frequency command, `Fnnnnnn`.
BR?	`PFnnn PRnnn VSWRnnn AMnnn MARnnn`	Runs and immediately returns the results of the Remote BITE test sequence. PF is the forward power in units of 0.1 watt, PR is the reflected power in units of 0.1 watt, VSWR is the voltage standing wave ratio in units of 0.1 (e.g. VSWR013 represents a VSWR of 1.3:1). AM is the modulation percentage in whole percent, and MAR is the noise margin expressed as the difference in whole dB from the predicted value. This command takes approximately 1 second to complete.
C?		Request report of all parameters that are now different from those reported in the last Radio Status Message for each parameter.
CFC		Clear current faults. All bits of the `FC?` reply are cleared to 0.
CFA		Clear accumulated faults. All bits of the `FA?` reply are cleared to 0.
DACn		Turns on or off the DAC (digital-to-analog converter) test. This test produces a 1 kHz audio tone from the receiver audio port. Replace n with 1 to enable the DAC test, or 0 to disable the DAC test. While the DAC test is enabled, the transceiver's normal operation is suspended and the response to other commands (except `DAC?`) is unpredictable.

Table 3-3 Radio Command and Status Messages.

Syntax	Reply	Description
DAC?	DACn	Requests the condition of the DAC test. 0 indicates the DAC test is on and 0 indicates the DAC test is off.
F123456		Change the transceiver operating frequency. Digits 1 through 6 represent the six digits of the transceiver operating frequency with 1 representing the 100 MHz digit and 6 representing the 1 kHz digit. The requested frequency must be a multiple of 25 kHz. Range: 118000 kHz to 136975 kHz. (Default is 121500 kHz.)
F?	Fnnnnnn	Request the current frequency. The reply format is the same as for the change frequency command above.
FA?	FAnnnnnnnnnnnnnnnn	Request a report of all accumulated faults. Once a fault condition has occurred, it will be reported as 1 even though the fault condition may no longer exist. The meaning of the 16 n characters is the same as for the FC? command above. All bits may be cleared to 0 with the CFA command.
FC?	FCnnnnnnnnnnnnnnnn	Request a report of all current faults. The 16 n characters represent the current status of the fault conditions with each n replaced with a 1 to indicate a fault conditions exists, or a 0 to indicate a fault condition does not exist. Starting with the first (left most) n character, the definition of each fault bit is as follows: 1. Software error interrupt has occurred 2. Not currently used 3. 1st or 2nd LO PLL out of lock 4. DSP clock synthesizer PLL out of lock 5. Transmit synthesizer PLL out of lock 6. DSP processor not responding to requests 7. EEPROM does not accept programming 8. One of the serial ports has timed out while transmitting 9. Not currently used 10. Not currently used 11. Serial port overrun error 12. Serial port parity error 13. Serial port framing error 14. Not currently used 15. Not currently used 16. Not currently used All bits except bit 1 will be cleared to 0 whenever the associated fault condition goes away. Serial port faults are cleared when subsequent serial data is received without the error condition. All bits of this message may be cleared with the CFC command.

Table 3-3 Radio Command and Status Messages.

Syntax	Reply	Description
FS?	FSn	Fault Summary. This is an abbreviated version of the FC? command. If any of the FC? bits are set true, this request returns FS1. Otherwise it returns FS0.
G123		Change manual gain. Digits 1 through 3 represent the significant figures of the IF gain reduction from full gain. This number is in units of 1/2 dB and is implicitly negative. To convert the desired actual manual gain reduction in dB, multiply it by 2. For example, to set a gain of -123.5 dB, send G247. (Range: 0 through 255 corresponding to 0 to 127.5 dB of gain reduction).
G?	Gnnn	Request the current manual gain setting. The format of the reply is the same as for the Gnnn command above
GB		Go to the boot program. This command is used in preparation for uploading new control and DSP firmware. The unit immediately switches to the Boot program and will accept Xmodem formatted uploads from the asynchronous serial ports or the HDLC port. For asynchronous serial uploads, the desired program to upload and serial line parameters must still be selected with the rear panel DIP switches *Note: Primarily for factory use.*
ID?	Cubic Communications VHF Transceiver Ver n.nn mm-dd-yy Copyright "YEAR" CCI	Request identification information for the control processor firmware. Information returned includes the manufacturer, version number, date, and the copyright notice of the program.
IDD?	DSP firmware: Ver nn.nn mm-dd-yy	Request identification information for the DSP processor firmware. Information returned included the version number and the date.
ISn		Set the audio input source. n is replaced as follows: 0 = reserved, 1 = line input, 2 = internal tone, 3 = internal noise source, and 4 = CW
IS?	ISn	Request the audio input source. The reply format is the same as for the ISn command.
L123		Change the amplitude based squelch level. Digits 1 through 3 represent the signal level in dBm that must be present to open the squelch with the 1 representing the hundreds of dBm, and the 3 representing the units of dBm. This number is implicitly negative. If it is set to 113, the squelch will open without regard to signal amplitude. Note that the squelch may also be opened by the carrier-to-noise ratio independently of this setting.
L?	Lnnn Nnn	Request current squelch level settings - both level and noise. The reply format is the same as for the L123 and N12 commands.

Table 3-3 Radio Command and Status Messages.

Syntax	Reply	Description
Mn		Change receiver operating mode. Replace the n with a number from 0 to 3 that represents the desired mode. Mode 0 is analog AM modulation, mode 1 is AM-MSK digital modulation, and mode 2 is D8PSK digital modulation. Presently only Mode 0 is valid
M?	Mn	Request the current mode. The reply format is the same as in the Mn command.
N12		Set the carrier-to-noise ratio based squelch. Digits 1 and 2 represent the carrier-to-noise level in dB, range 0-99 dB, that must be present for the squelch to open. Note that the squelch may also be opened by the signal amplitude independently of this setting. Settings > 40 dB may not operate reliably.
N?	Lnnn Nnn	Same as L?.
PF?	PFnnn	Report current transmitter forward power in watts.
PO		Run the power-on-self-test (POST) sequence. This test is run automatically at power-on, but may be repeated at any time with this command.
PO?	POnnnnnn	Request the results of the most recent power-on-self-test (POST) sequence. The POST sequence includes the BITE test. Each of the n characters represents one of the tests performed when the POST sequence is run and is replaced with a 1 to indicate that the test failed or a 0 to indicate that the test passed. Starting with the first (left most) n character, the definition of each test bit is as follows: Control processor program ROM test failure Cntrol processor RAM test failure DSP processor self test failure BITE test failure Power Supply Test
PR?	PRnnn	Report current transmitter reflected power in watts.

Table 3-3 Radio Command and Status Messages.

Syntax	Reply	Description
PS?	PSnnnnnnnn	Request status of power supply voltage. The 8 n characters represent the status of the power supply voltages. Each n is replaced with a 1 to indicate a fault condition exists, or a 0 to indicate a fault condition does not exist. Starting with the first (left most) n character, the definition of each fault bit is as follows. 1. -17 too low 2. -17 too high 3. +8 too low 4. +8 too high 5. +17 too low 6. +17 too high 7. +28 too low 8. +28 too high All bits will be cleared to 0 whenever the associated fault condition goes away. *Note: For negative voltages, "too low" means "too close to zero volts".*
PWRnn		Set the transmitter power output to nn watts. Range: 1 – 25 watts (Default value is 25 watts.)
PWR?	PWRnn	Report the current transmit power setting. The reply format is the same as for the PWRnn command
RSSIn		Enable or disable updating Received Signal Strength Indication (RSSI) output. Replace the n with 1 to enable RSSI operation or 0 to disable RSSI output. When RSSI output is disabled, updating ceases. (Default is on.)
RSSI?	RSSIn	Request current status of the updating RSSI output (on or off). The n character is replaced with a 1 if RSSI is enabled, or a 0 if RSSI is disabled.
R?	F123456 Mn Lnnn Nnnn An Gnnn Isn FSn	Request receiver operating parameters. Each of the reported parameters is formatted the same as for the individual requests.
SA?	SA±123	Request the current audio output level in dBm. The ± character represents the sign of the value and will be either + or -. The 1 digit represents the tens of dBm, and the 3 represents the tenths of dBm. Range –50.1 to +12 dBm.
SS?	SS±123	Request signal strength in Mode 0. The ± character represents the sign of the value and will be either + or -. Digits 1 through 3 represent the significant digits of the signal strength in dB relative to one milliwatt where 1 represents the hundreds of dBm and the 3 represents the units of dBm. Range: -115 to +12.

Table 3-3 Radio Command and Status Messages.

Syntax	Reply	Description
SSH?	SSH±123	Same as the SS? command except that the returned value is in units of ½ dB. This gives more resolution for making certain measurements.
SN?	SN123	Request the current carrier-to-noise measurement. The returned value is expressed in dB with the 1 representing the 100s of dB (always 0) and the 3 representing the units of dB. Range: 0 to 50 dB.
Tn		Transmit/receive switch for Mode 0. To switch to transmit replace the n with 1, to switch to receive replace the n with 0.
TNnnnnn		Set the frequency of the tone generator (or frequency shift in FSK mode) to nnnn Hz. Range = 50 to 6000 Hz. (Default is 1 kHz.)
TOn		Sets the transmitter offset. TO0 is no offset, TO1 is -4kHz, and TO2 is +4 kHz. (Default is TO0.)
TTnnnn		Set the Mode 0 transmit timer value. The nnnn characters represent the maximum time in seconds that the transmitter may stay on. Range: 1 through 1020 seconds. A setting of 0 disables the timer. The default is timer disabled.
T?	Tn	Request the transmit/receive status. If the unit is in the receive state the reply will be T0, if in transmit, the reply will be T1.
TN?	TNnnnnn	Request the current frequency of the tone generator. The reply format is the same as for the TNnnnnn command.
TO?	TOn	Request the current transmitter offset frequency. The reply format is the same for the TOn command above
TT?	TTnnnn	Request the mode 0 transmit timer value. The reply format is the same as for the TTnnnn command.
VFn		Turn on or off vector feedback. Replace the n with 1 to turn on vector feedback, or a 0 to turn off vector feedback. Vector feedback is on by default at power on.
VFCAL		Perform the vector feedback calibration and store the constants in a table in the EEPROM. Before executing this command, a dummy load must be connected to the antenna connector. The calibration may take over 30 seconds to complete, and activity is signaled by a click for every frequency stored in the table. The command is complete when the clicking stops. Vector feedback is turned on at the completion of this command.
VF?	VFn	Requests status of vector feedback. The reply is the same as for the VFn command.

Table 3-3 Radio Command and Status Messages.

Syntax	Reply	Description
VFC?	VFC I=±nnnnn Q=±nnnnn	Requests the vector feedback values for the current frequency. The reply is the same format as the VFI±nnnnn and VFQ±nnnnn commands.
VFCLR		Sets the values in the vector feedback constant table in EEPROM to zero. This prevents the use of vector feedback. The VFCAL command will rebuild the table.
VFI±nnnnn		Store the value ±nnnnn as the I vector feedback value for the current frequency in the table. The value must be in the range of -32768 to 32767.
VFONE		Run the vector feedback calibration routine on the current frequency only. The result is stored in the vector feedback calibration table.
VFQ±nnnnn		Store the value ±nnnnn as the Q vector feedback value for the current frequency in the table. The value must be in the range of -32768 to 32767
VPS?	VPSsnnn snnn snnn snnn	Where snnn represents the sign and digits of the power supply voltage in units of 1/10 volt, nominal values are: VPS +280 +170 +080 -170

3-2 POWER UP AND TESTING CONSIDERATIONS.

Whenever power is applied to the transceiver it will execute a Power On Self Test sequence. This sequence tests several functions inside the transceiver including memory tests, a confidence test of the configuration options stored in non-volatile memory, and a BITE (built in test equipment) test of transceiver functions. Since it is often required that the transceiver not send any unsolicited bus messages, the transceivers will not announce a wait condition over the bus. During the wait condition, the transceiver will only respond to a limited subset of commands from the bus. These are:

`:?`	Request interface status message
`PO?`	Request results of Power On Self Test
`!`	Clear wait condition and proceed with startup

While in the wait condition, if the `:?` command is sent, the transceiver will respond with:

`TE:EEPR` or `TE:POST`

This indicates that the transceiver is waiting. This condition can only be cleared by sending the `!` command. To determine the reason for POST failure, the user should then request POST results (`PO?`) and if this shows BITE failure, also request the BITE results (`BI?`) after clearing the Power on Wait condition with the ! command.

NOTE:
In the event of a POST failure, the radio will emit a sequence of failure codes in morse code. These codes should be relayed to CCI in order to assist in troubleshooting.

The proper way to structure a remote control program to handle this condition is to query each transceiver for interface status (`:?`) before sending any other commands at power up and wait for the reply. A reply will not be sent until a wait condition has been entered or normal operation has been entered. If the wait condition is indicated, send the ! command and test again. This process should be repeated until the transceiver responds with an interface status other than `TE:` (serial interface.)

3-3 EEPROM FAILURE.

If a POST failure was caused by a corrupted EEPROM, send the VFCLR command to reset the vector feedback constant table values in EEPROM to zero. Next, connect the transceiver to a 25 watt, 50Ω dummy load. Then send the VFCAL command to rebuild the table.

CHAPTER 4
GENERAL THEORY OF OPERATION

4-1 INTRODUCTION.

This chapter contains a block diagram description of the ATC-100. Each of the boards/modules are discussed in the paragraphs below: (See figure FO-2.)

NOTE:
AC input is standard, DC input is optional.

4-2 BLOCK DIAGRAM DISCUSSION.

4-2.1 *Receptacle/RFI Filter.* The Receptacle/RFI Filter keeps internally generated power supply switching noise off the input line. When the rear panel power switch (S3) is set on, power is applied to the power supply module through the Receptacle/RFI Filter, through the circuit breaker (CB1) and the Line Filter.

4-2.2 *Line Filter.* The Line Filter board keeps internally generated power supply switching noise off the input line. When the front panel power switch is set ON, input power is applied to the power supply module through the Line Filter board.

4-2.3 *Power Supply Module.* The power supply module is a switching regulated type that provides +28, +8, +17, and -17 VDC to the RF Analog Board, Digital Board, PA Module and the TX Synthesizer Module using 90 to 260 VAC input power (automatically sensed). Fault detector circuits send a fault signal to the Command Input Latch in the Digital module if any of the voltages fall below a preset level.

4-2.4 *RF Analog Module.* The RF Analog Module contains the RF Section, 1st IF, 2nd IF, Mode 2/3 fast AGC Detector, Mode 0/1 AGC Filter, AGC Shaping Network, Mode 0/1 Transmit Audio Input, Mode 0/1 Receive Audio Driver, Receiver Signal Strength Indicator (RSSI) Driver, LED Drivers, DSP Clock, 10 MHz Reference, RF Bite Circuits. Refer to the RF Analog Module schematics in the back of this manual for each of the circuits described below.

4.2.4.1 *RF Section.* The RF Section contains the directional coupler, transmit/receive switch, highpass filter, limiter, highpass filter/FM broadcast notch, 1st RF preselector, RF AGC attenuator, RF amplifier, 2nd RF preselector, fixed attenuator, 1st mixer, and the 1st local oscillator. Each of these circuits are described below.

4-2.4.1.1 *Directional Coupler.* The first section on the antenna port of the RF/Analog board is a directional coupler etched onto the printed circuit board. The directional coupler allows a very low path loss for both transmitted RF as well as received RF signals. The circuit couples a small BITE signal into the receiver front end for functional testing while keeping the signal radiating out the antenna to a very low level.

4-2.4.1.2 *Transmit/Receive Switch.* The transmit/receive switch is used to route the transmit signal to the antenna when in transmit mode and to route the signal received from the antenna to the receiver when in receive mode. Two PIN diodes (CR1 and CR2) are used for this function. When in transmit mode, both diodes are biased on, the transmit signal goes through the series diode (CR1), while the shunt diode (CR2) provides a high impedance at the C1/CR1 node through the 90 degree phase shift network (C130 - C56). In receive mode, both diodes are off, presenting a high impedance which allows a low loss path from C1 to C7.

4-2.4.1.3 *Highpass Filter.* The highpass filter (C7 - C14) rejects frequencies at the 1st IF frequency (45 MHz) from entering the rest of the RF circuitry. It also attenuates signals which could create harmonics in the RF passband (118 - 137 MHz) from reaching the 1st mixer.

4-2.4.1.4 *Limiter.* The RF limiter is used to keep very high level signals below levels which could cause damage to active components downstream. Diodes CR18 and CR45 provide a fast responding clamp to limit the voltage. CR44 is a PIN diode which provides a shunt impedance which decreases with increased RF level to provide additional protection. Printed inductors ML1 and ML2 along with shunt capacitance from C46, PCB traces and diodes form a lowpass filter.

4-2.4.1.5 *Highpass Filter FM Broadcast Notch.* The circuit of C20 - C26 is an elliptical highpass filter specifically designed to attenuate signals in the FM broadcast band (88 - 108 MHz), while providing a low path loss to signals in the desired band (118 - 137 MHz).

4-2.4.1.6 *1st RF Preselector.* The 1st RF preselector is to break the aircraft band (118 - 137 MHz) into 4 ranges to provide low loss in each of the ranges and good selectivity outside the range. The 4 ranges are achieved by using PIN diodes (CR9 - CR12) to switch in or out variable capacitors (CR32, 33, 42 and 43) which resonate with L11 and L14.

4-2.4.1.7 *RF AGC Attenuator.* The RF AGC attenuator is used to provide a voltage controlled attenuation of the RF signal to prevent circuits downstream from functioning in a non-linear fashion. As bias current increases through PIN diodes CR25 and CR26, their RF resistance decreases and the signal is attenuated. The RF resistance of CR26 connects the RF node of L32 and C101 directly to RF ground (C100). The RF resistance of CR25 connects the RF node of L31 and C97 directly to RF ground (C99) through a 47 ohm termination (R165). This circuit provides a low VSWR at the input (C96 side) at all attenuator settings with the 90 degree phase shift network formed by C97 - C101. This circuit has a range of approximately 20 dB.

4-2.4.1.8 *RF Amplifier.* The RF amplifier is used to boost the input signal to overcome losses downstream as well as beginning to establish system noise figure. The resistor network between U8 and C48 serve to provide an RF pad to the amplifier, which helps input VSWR and stability (to oscillation). The resistors also provide the DC bias to U8.

4-2.4.1.9 *2nd RF Preselector* The 2nd RF preselector is nearly identical to the 1st RF preselector. Its main difference is it has more selectivity than the 1st preselector at the expense of slightly more insertion loss. The better selectivity and higher loss are appropriate here because it follows the RF amplifier. The 1st and 2nd RF preselectors produce a smooth cascade with the RF amplifier (and bias pad) acting as an impedance buffer.

4-2.4.1.10 *Fixed Attenuator.* The three resistor pad (R147, 149 and 150) provide the 2nd RF preselector with a stable impedance while also lowering the level to the first mixer (Z1).The three resistor pad (R147, 149 and 150) provide the 2nd RF preselector with a stable impedance while also lowering the level to the first mixer (Z1).

4-2.4.1.11 *1st Mixer.* The 1st mixer (Z1) translates the RF signals to the 1st IF frequency (45 MHz). The drive signal from the 1st LO is filtered through a lowpass filter (C83 - C88). The LO port sees a broadband termination with the bandpass network (L30/R152 - C89/R155).

4-2.4.1.12 *1st Local Oscillator.* The 1st LO is used to convert the incoming signal to the I.F. frequency of 45 MHz. The frequency of the 1st LO can be found by adding 45 MHz to the tuned channel frequency. The output level of the 1st LO is +17 dBm that is fed to the 1st mixer, Z1.

The Voltage Controlled Oscillator generates the 1st LO frequency in 2 bands. Q34 and associated circuitry operates from 163 to 171.975 MHz while Q37 and associated circuitry operates from 172 to 181.975 MHz. 5 VDC on the FLTSEL1 line connected to R553 switches to the 172 to 181.975 MHz VCO. The VCO signal is amplified by Q57 and Q51 to buffer the VCO and increase the level to +17 dBm.

The frequency of the 1st LO is determined by a digital phase lock loop. The 10 MHz reference circuit provides a highly accurate signal that is divided by 100 to provide 100 KHz as a comparison frequency for the digital phase detector contained in PLL integrated circuit, U53. The signal is amplified and buffered by Q42 and input to Pin 8 of U53. An internal programmable divider in U53 is set to divide by 100. The VCO signal is amplified by Q57 and input to the RF IN pin of U53. This signal is divided by a programmable divider contained in U53 and used as the second input to the digital phase detector contained in U53. The phase detector generates an error voltage on the PHP pin of U53. This voltage is integrated by Q26 and inverted by U56 to provide a DC tune voltage (TP13) to set the VCO on the desired frequency.

Programming of the Phase Lock Loop is accomplished by 3 line serial interface consisting of Data, Clock, and 1STLOEN. A data word consisting of 24 bits is clocked into registers contained in U53 and latched on the rising edge of the 1STLOEN line on the STROBE input to U53. 4 data words are required to program U53, providing initialization and frequency setting. Once initialized, the frequency is changed by a 32 bit word.

4-2.4.2 *1st IF (45 MHz).* The 1st IF contains the 1st mixer termination, 1st 45 MHz IF amplifier, IF AGC attenuator, fixed attenuator, crystal filter, 2nd 45 MHz IF amplifier, 2nd mixer, and the 2nd local oscillator. Each of these circuits are described below.

4-2.4.2.1 *1st Mixer Termination.* The IF port of the 1st mixer is attached to a highpass filter and broadband termination circuit (between C110 and L40). At 45 MHz, this circuit provides a low loss path between the mixer and IF amplifier (U15). Out of band, signals are terminated into R187 and R189 for a low VSWR over a very broad frequency range.

4-2.4.2.2 *1st 45 MHz IF Amplifier.* After the losses of the 2nd preselector, pad and mixer, the signal needs to be boosted again, U15 serves this purpose. L40, 41 and C128 lower the VSWR of U15 at 45 MHz. L42, 43 and C129 serve as a DC bias path and parallel resonant circuit at the output of U15.

4-2.4.2.3 *IF AGC Attenuator.* The IF AGC attenuator (C121 - C170) is very similar to the RF AGC attenuator. The main differences are the frequency range (45 MHz instead of the aircraft band (118 - 137 MHz)), and two sections instead of one. The IF AGC network also contains three 90 degree phase shift networks (C121 - C170). The two IF AGC networks are also placed in a mirror image fashion to produce low VSWR to both the input (C121) and output (C170) at all attenuation settings. The IF AGC attenuator has a range of approximately 40 dB.

4-2.4.2.4 *Fixed Attenuator.* The resistor network of R19, 2, 20, 21, and 121 helps to stabilize the input impedance of the crystal filter network with varying attenuation from the IF attenuator circuit.

4-2.4.2.5 *Crystal Filter.* The crystal filter (FL1) provides selectivity to keep components downstream within their linear range. The inductors and capacitors (C141 - C142) match 50 ohms up to the crystal impedance of approximately 800 ohms. The adjustments in this circuit are critical to provide a repeatable group delay from unit to unit for proper response to D8PSK signals.

4-2.4.2.6 *2nd 45 MHz IF Amplifier.* The 2nd 45 MHz IF amplifier (U19) boosts the signal level prior to the 2nd mixer.

4-2.4.2.7 *2nd Mixer.* The 2nd mixer (Z2) translates the 1st IF frequency (45 MHz) to the 2nd IF frequency (456 KHz). The drive signal from the 2nd LO is filtered through a lowpass filter (C185 - C188). The LO port sees a broadband termination with the bandpass network (L52/R273 - C190/R276).

4-2.4.2.8 *2nd Local Oscillator.* The 2nd LO is used to convert the 45 MHz IF to 456 KHz and operates at 44.544 MHz. The output level of +17 dBm is fed to the second mixer, Z2.

The Voltage Controlled Oscillator (VCO) consists of Q40 and associated circuitry. The output is amplified by Q58 and Q54 to provide the +17 dBm output to the 2nd mixer Z2. C329 is adjusted to center the VCO range to 45 MHz ±3 MHz.

The frequency of the 2nd LO is set by a Digital Phase Lock Loop. U54 contains the reference divider, VCO divider and Phase Detector required. Frequency accuracy is determined by a 10 MHz reference signal that is buffered by Q43 and input to the OSCIN pin of U54. The reference divider contained in U54 divides this signal by a programmed value of 625 to provide a reference of 16 KHz to the Phase Detector. The VCO frequency is input to the FIN pin of U54 and divided by the value of 2784 programmed into the VCO divider. This frequency is compared to the 16KHz reference by the Phase Detector to generate an error voltage on the PD pin if U54. The error voltage is integrated by Q32 to provide a DC Tune Voltage (TP23) which sets the VCO to the desired frequency.

Programming the PLL integrated circuit is done with a 3 line serial interface. Data is clocked into U54 while the 2NDLOEN line is held low. An 8 bit data word initializes U54, a 15 bit data word programs the reference value and a 16 bit data word programs the frequency.

4-2.4.3 *2nd IF (456 kHz).* The 2st IF contains the 2nd mixer termination, 2nd IF amplifier, ceramic filter, and variable gain 2nd IF amplifier. Each of these circuits are described below.

4-2.4.3.1 *2nd Mixer Termination.* The IF port of the 2nd mixer is attached to a bandpass filter and broadband termination circuit (between J28 and L56). At 456 KHz, this circuit provides a low loss path between the mixer and IF amplifiers (Q6 and U23). Out of band, signals are terminated into R299 and R301 for a low VSWR over a very broad frequency range. The circuit containing L56 through C202 is a broadband termination working down to DC.

4-2.4.3.2 *2nd IF Amplifier.* Q6 and its surrounding components provide a gain stage prior to the ceramic filter (FL2). Resistors on the source of Q6 maintain a constant current bias. L57 and C204 are a parallel resonant tank at the output of Q6, L57 also provides DC power to Q6.

4-2.4.3.3 *Ceramic Filter.* The ceramic filter (FL2) provides additional selectivity prior to the analog to digital conversion. Resistor networks at the filter input and output provide the proper termination impedance to the ceramic filter.

4-2.4.3.4 *Variable Gain 2nd IF Amplifier.* U22 is the final gain stage prior to the analog to digital conversion. R328 is adjusted to a set value of translation gain of the analog circuitry.

4-2.4.4 *Mode 2, 3 Fast AGC Detector.* The Mode 2,3 fast AGC detector contains variable gain 2nd IF amplifier (analog AGC threshold set) and the detector. Each of these circuits are described below.

4-2.4.4.1 *Variable Gain 2nd IF Amplifier (analog threshold set).* The 456 KHz level is boosted with U23 and U24 to provide adequate levels to the detector diodes. R22 is used to set the threshold level of the detector.

4-2.4.4.2 *Detector.* The IF signal into detector diodes CR6 and CR7 produce a ½ wave rectified voltage for the AGC circuitry. Temperature compensation is accomplished by measuring the differential voltage of the detector diodes relative to a set of diodes with a fixed bias. A fast attack/slow decay integrator is used to quickly adjust the analog output level to allow capture of a D8PSK signal. CR3, R52 form the path to charge the integrator capacitor C111, R69 sets the slow decay discharge path for C111. A signal from the digital board is used to discharge the integrator capacitor (C111) with Q50. R72, 73 and CR19 clamp the integrator output to approximately 3 VDC.

4-2.4.5 *Mode 0,1 AGC Filter.* The circuit from R453 to C434 forms a lowpass filter for anti-aliasing from the digital to analog converter on the digital board. The AGC voltage comes from the digital board when the receiver is in mode 0 or mode 1. U26 switches the AGC voltage between the digital board (mode 0,1 or voice) or from the fast AGC circuit (C60 - R74) when in mode 2 or 3.

4-2.4.6 *AGC Shaping Network.* The AGC shaping network (R87 - U4) serves to provide a reasonably linear voltage to (analog) attenuation level (in dB) transfer function. The RF and IF AGC attenuators have a very non-linear transfer curve. It is important to have a linear transfer characteristic for two reasons, AGC loop stability and RSSI reporting accuracy. The shaping network uses two multiplier IC's (U27 and U28) to form a third order polynomial transfer network. U4 serves as a buffer to drive the AGC circuits.

4-2.4.7 *(Mode 0,1) Transmit Audio Input.* The transmit audio input circuit (E7/E8 through C405) serves two purposes. The first is to convert the balanced audio input to unbalanced, and second to buffer and filter the signal. U32A, 32B and 33A convert the balanced signal to unbalanced. R158 to C405 filters out high frequency noise components before going to the analog to digital converter on the digital board.

4-2.4.8 *(Mode 0,1) Receive Audio Driver.* The circuitry from R127/R12 through C289/C290 is a receive audio balanced input to balanced output for mode 0, 1 or voice. When in mode 0, 1 or voice, analog balanced inputs from the digital board travel through U3A and are filtered in U3B. U26 opens the audio path to U30 and U31 when transmitting to avoid noise getting to the audio output and into a modem, speaker or headphones. U31 converts the signal from unbalanced to balanced and serves as a driver for a modem or other audio output device. The circuitry from C35/C37 to R44 is a detector which provides a digital output to J2 when audio is present at U31. U16B converts the balanced audio signal to unbalanced. U16A, CR38 and C73 form a ½ wave rectifier and integrator which produces a DC level proportional to the AC input. U17A and its surrounding resistors form a comparator with hysteresis which generates a high DC level when an audio threshold level is achieved. Q45 and R44 produce an active low output.

4-2.4.9 *Receive Signal Strength Indicator (RSSI) Driver.* The RSSI (Receive Signal Strength Indicator) is a DC level used to drive an external analog meter which is proportional to received signal level. refer to table 4-1. U35 is a digital to analog converter which takes in serial data and outputs a DC voltage. U39A is a buffer and gain amplifier to drive the meter.

Table 4-1 RSSI Input Signal Voltages

RF Input -μV	AGC-VDC
0.10	5.87
0.35	5.47
0.88	5.0
3.25	4.45
19.00	4.02
275.00	3.50
5,000.00	2.96
15,000.00	2.74
70,000.00	2.40
360,000.00	2.00

4-2.4.10 *LED Drivers* Four front panel LEDs are circuit driven. The POWER LED line is driven directly from the +8 VDC line from the power supply. The other three lines are controlled through logic levels from the digital board.

4-2.4.11 *DSP Clock* The DSP clock circuit generates a 49.152 MHz signal used as the timing signal for the DSP. A crystal oscillator is employed to achieve frequency accuracy during start up conditions. The oscillator is locked to the 10 MHz system reference frequency for precise accuracy.

The Voltage Controlled Crystal Oscillator (VCXO) consists of Q9, Y2 and associated components. C183 sets the center frequency of the oscillator such that the oscillator will tune above and below 49.152 MHz by 2.5 kHz. The oscillator output is amplitude limited by Q20 and buffered by Q39. A low pass filter and resistive attenuator reduce harmonics and set the output level to 7 dBm.

The DSP Clock is locked to the 10 MHz system reference using a Digital Phase Lock Loop. The reference divider, VCO divider and Phase detector are contained in Integrated Circuit U65. The 10MHz REF signal is amplified by Q44 and input to the OSCIN pin of U65. This signal is divided by the reference divider to provide a 16 KHz reference to the Phase Detector. The output from the crystal oscillator is input to the FIN pin of U65 where it is divided by the programmed value of 3072 to provide the second input to the Phase detector. The phase detector generates an error voltage on the PD pin of U65. This voltage is integrated by Q19 to provide a DC Tune Voltage (TP24) to set the oscillator on frequency.

4-2.4.12 *10 MHz System Reference* The 10 MHz reference circuit provides a 10 MHz signal to synchronize the 1st LO, 2nd LO, DSP Clock, Bite Generator and Transmit Synthesizer. A TCXO is employed for frequency accuracy over temperature variations and an input for an external 10 MHz reference is provided.

Y1 is the Temperature Compensated Crystal Oscillator. (TCXO) This provides a 10 MHz signal accurate within 2 parts per million. (ppm) This signal is fed through solid state switch U47, amplified by Q46 and low pass filtered, then connected to the 1st LO, 2nd LO, DSP Clock, and Bite generator. Amplifier Q48 provides a 50 Ohm output for the reference coax to the Transmit Synthesizer.

An external 10 MHz reference can be connected to the ATC-100 and switching from internal to external is done automatically by detecting the presence of an external 10 MHz signal. The EXT 10MHz is input to the RF Analog board on J8. The signal is limited by CR40 and CR41, then amplified and bandpass filtered by Q15 and associated circuitry. CR43 and U46 detect the EXT 10MHz signal and switch U47 from the internal path to the external 10 MHz path. Simultaneously the 5 VDC power is removed from Y1 to prevent interference.

4-2.4.13 *RF BITE Circuit* The RF BITE circuit (C368 through R599) is used to produce RF levels in the aircraft band. Q47 boosts the 10 MHz reference signal into U45A which divides the frequency of the signal by two to output a 5 MHz square wave. U45B takes the 5 MHz square wave and outputs a very narrow pulse at a 5 MHz rate. The spectrum of this waveform is a "comb" of frequencies at 5 MHz intervals whose amplitudes are reasonably flat through the aircraft band. The frequencies of this comb generator which can be used for aircraft band testing are 120, 125, 130, and 135 MHz. R597 - R599 provide attenuation of the signals as well as an impedance buffer.

4-2.5 *TX Synthesizer Module.* The Transmit Synthesizer provides the on channel carrier for the ATC-100 transmitter. During receive mode the synthesizer output is switched off to prevent interference with the receiver.

The Voltage Controlled Oscillator generates the transmit frequency in 2 bands. Q9 and associated circuitry operates from 118 to 126.975 MHz while Q12 and associated circuitry operates from 127 to 136.975 MHz. 5 VDC on the FLTSEL1 line connected to R57 switches to the 127 to 136.975 MHz VCO. The VCO signal is buffered by U10, Q13, U11, and U15. A 0 Volt low signal on the TXSYN ON/OFF line causes U13 and U14 to shut off the signal path during receive. U16 amplifies the signal to the +17 dBm level.

The frequency of the Transmit Synthesizer is determined by a digital phase lock loop. The 10 MHz reference circuit provides a highly accurate signal that is divided by 100 to provide 100 KHz as a comparison frequency for the digital phase detector contained in PLL integrated circuit, U5. The signal is input to Pin 8 of U5. An internal programmable divider in U5 is set to divide by 100. The VCO signal is amplified by U10 and input to the RF IN pin of U5. This signal is divided by a programmable divider contained in U5 and used as the second input to the digital phase detector contained in U5. The phase detector generates an error voltage on the PHP pin of U5. This voltage is integrated by Q6 and inverted by U7 to provide a DC tune voltage to set the VCO on the desired frequency.

Programming of the Phase Lock Loop is accomplished by 3 line serial interface consisting of Data, Clock, and TXSYN EN. A data word consisting of 24 bits is clocked into registers contained in U53 and latched on the rising edge of the TXSYN EN line on the STROBE input to U5. 4 data words are required to program U5, providing initialization and frequency setting. Once initialized, the frequency is changed by a 32 bit word.

4-2.6 *Digital Module.* The Digital module contains two major sections: the Control Section and the DSP Section. Each of these sections is described below

4-2.6.1 *Control Section.* As shown in figure 4-1, the Control Section governs all aspects of the transceivers operation. The Control Section receives commands and transmits status via a RS232/485 interface. All receiver operating parameters, such as frequency and bandwidth are controlled by the Control Section. In addition, the Control Section stores calibration parameters in non-volatile memory which are retained when power is removed.

The Control Section contains a microprocessor which has a 16 bit data bus. The clock frequency of the microprocessor is 50 MHz. The program is stored in a 128K x 16 bit flash memory and the data memory consists of a 32K x 16 bit static RAM. Non-volatile storage requirements are provided by a 8K x 8 bit EEPROM.

A CPLD is use to generate the address decoding logic circuitry for the various Control Section peripherals. An additional I/O port in the CPLD is used by the microprocessor for control of the RS-485 interface, the RS-232 interface and other off-board circuitry.

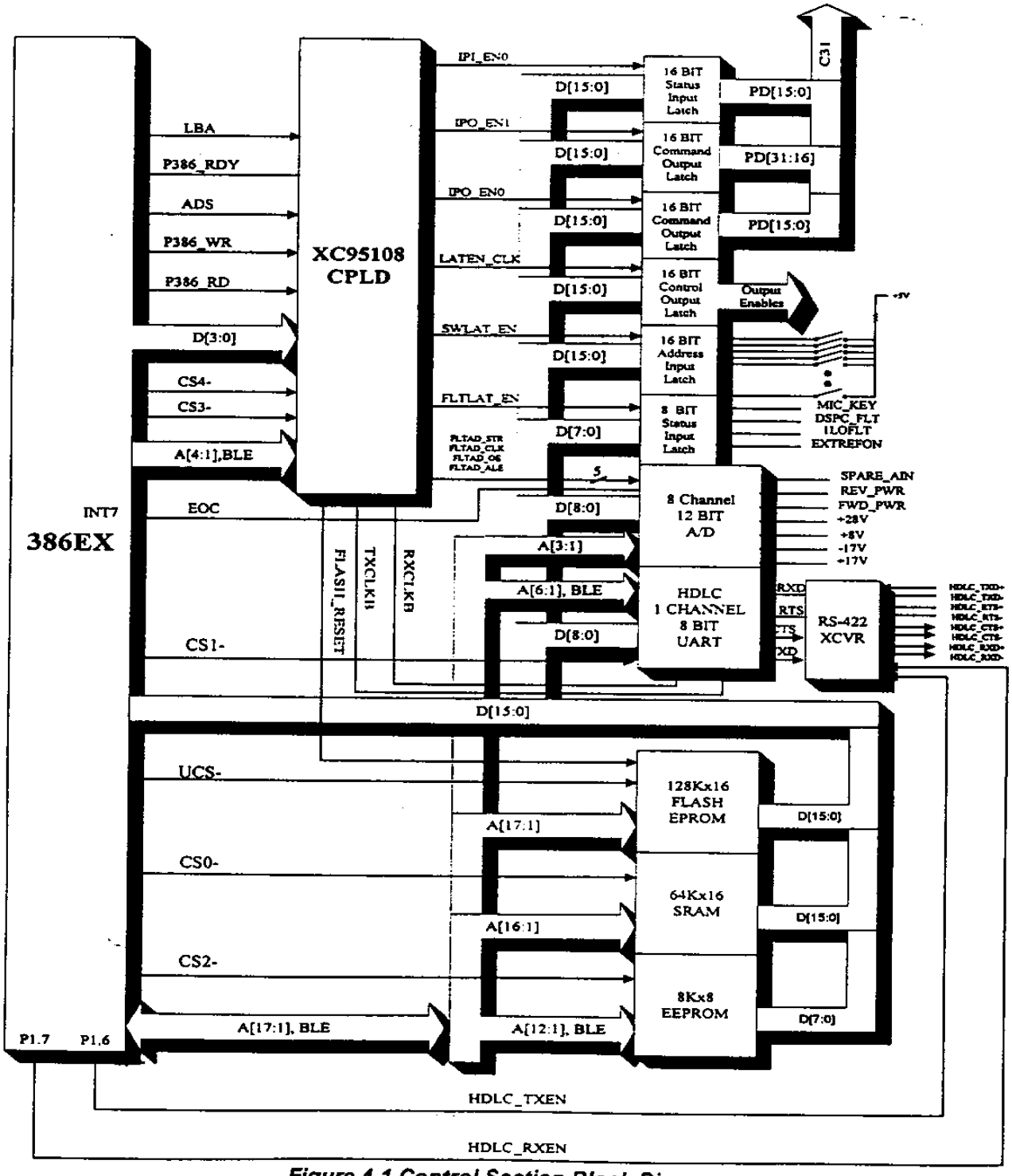


Figure 4-1 Control Section Block Diagram.

The microprocessor uses a 12 bit A/D to monitor the power supply voltages (-17V, +17V, +8V, +28V) as well as the Forward and Reflected power levels.

I/O ports provide processor output to the analog and DSP sections of the transceiver. D-latches are clocked by decoded addresses gated with a processor write signal. Some of these latched output lines are grouped together as enable, clock, and data lines and are operated by the processor as synchronous serial ports. Other latched output lines are used as control signals directly.

I/O signals include:

MIC_KEY	Indicates that the microphone key has been controlled on the rear panel or programmed on the serial port.
EXT_REF	Indicates that the external reference is on.
LO_FLT	Indicates that the 1st LO section has detected an out of lock condition.
DSPC_FLT	Indicates that the DSP Clock has detected an out of lock condition.
TXSYN_FLT	Indicates that the TX synthesizer has detected an out of lock condition.
1ST_LO_EN	Enables serial data to be written to the 1st Local Oscillator section.
2ND_LO_EN	Enables serial data to be written to the 2nd Local Oscillator section.
BITE_EN	Enables the BITE Test.
TXSYN_EN	Enables serial data to be written to the Transmit Synthesizer.
DSPC_EN	Enables serial data to be written to the DSP Clock.
RSSI_EN	Enables Data to be clocked into RSSI DAC.
PA_ENABLE	Enables the Power Amplifier.
FLTSEL0 FLTSEL1	Select one of four preselector filters.
TX_SYN_ON_OFF	Enables the transmit synthesizer output.
SRLCLK	Clocks out the control data to all modules.
SRLDATA	Control Data to all modules.

Furthermore, an RS-485 and an RS-232 serial interface is available as a directly communication link to the Control Section via the microprocessor as shown in figure 4-2. The microprocessor may use either of these two ports for maintenance or other predefined purpose.

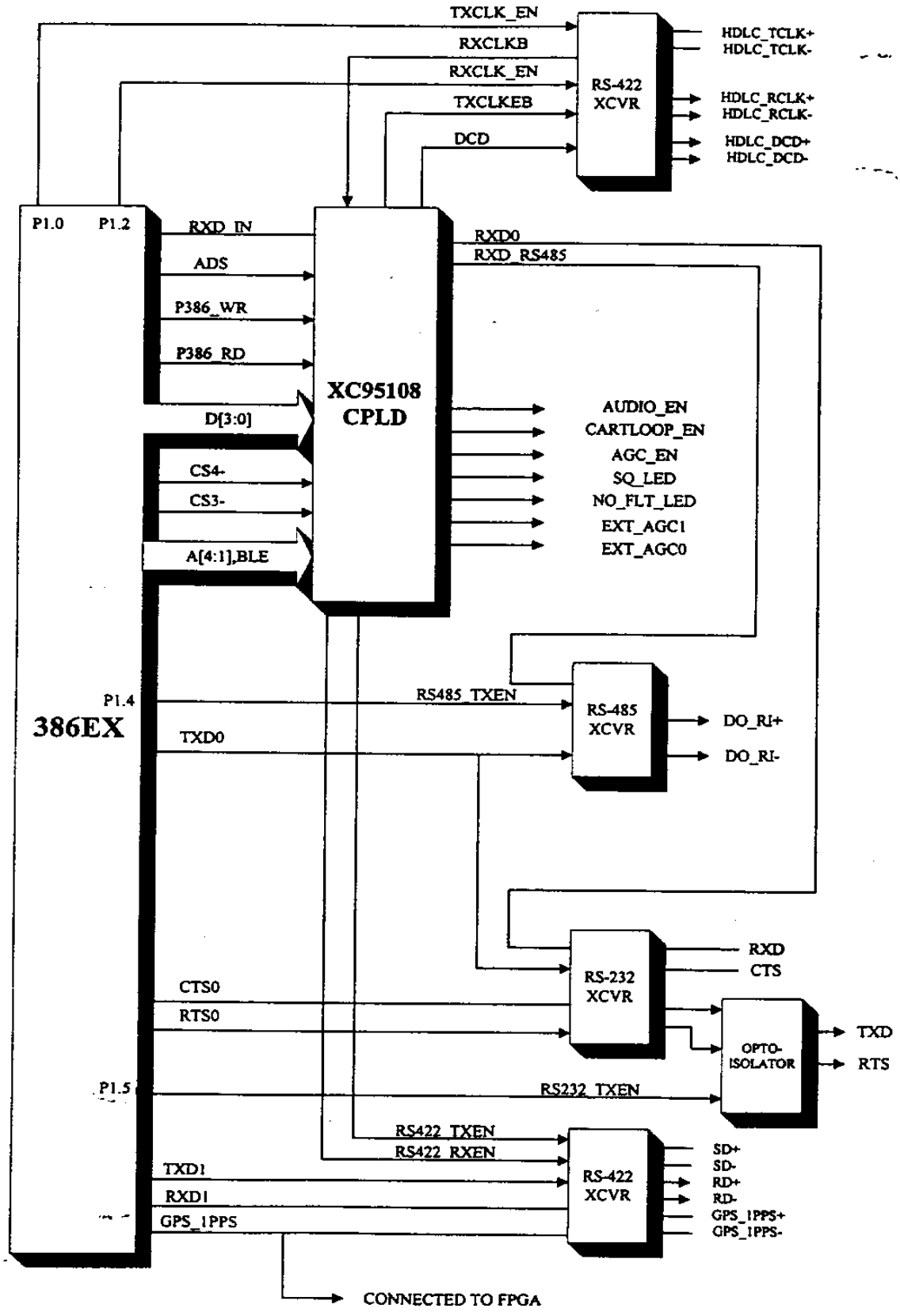


Figure 4-2 Control Section Communication Block Diagram.

4-2.6.2 *DSP Section.* The Digital Signal Processing (DSP) section contains a 4:1 Analog Multiplexer, a 14 bit A/D converter, a digital signal processor, 256K x 8 bit Flash EPROM, 32K x 32 bit Static RAM and a 12 bit D/A converter.

The DSP Section operates semi-independently from the Control Section. All communication between the Control Section and the DSP Section is through the I/O ports shown in figure 4-3. When the transceivers operating parameters are changed, the Control Section sends one or more commands to the DSP Section which makes the necessary changes to its operation, and the continues processing.

The processor controls the input to the 14 bit A/D converter via a 4:1 analog multiplexer. This allows the processor to select either the Received IF, the Transmitted Audio, the I Channel Feedback, or the Q Channel Feedback. This selection is based on the configuration of the transceiver (i.e. Receive mode, Transmit mode, or Calibration mode). The A/D converter samples that selected signal at a 96 KHz rate.

Once the analog signal is digitized, the processor will implement the modulation, demodulation, or calibration algorithms again depending on the mode of the transceiver.

Additionally, the processor will implement automatic gain control (AGC) through the use of a 12 bit D/A converter. The D/A converter output voltage controls the attenuators on the RF Analog Board.

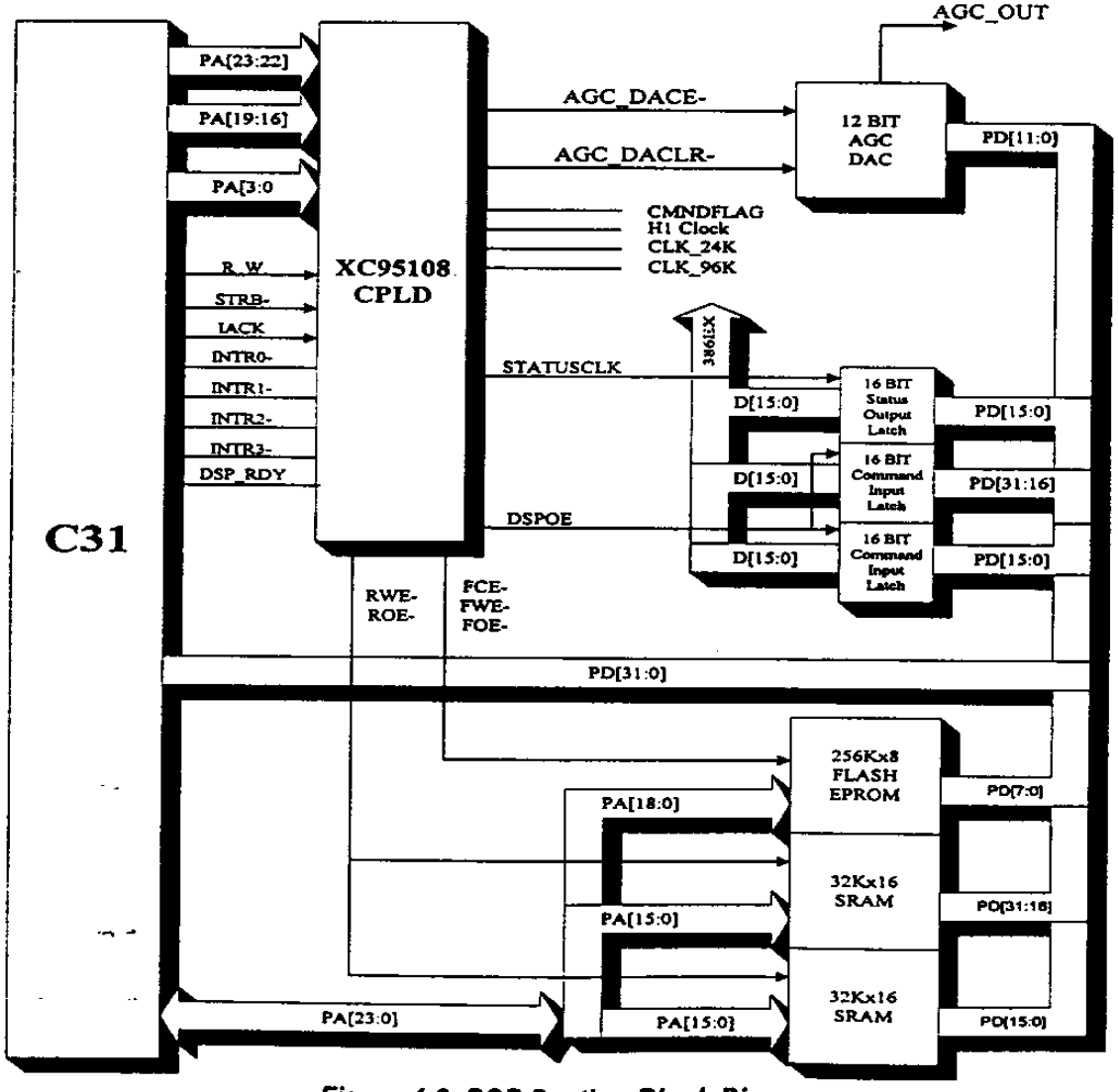


Figure 4-3 DSP Section Block Diagram.

4-2.7 *PA Module.* The power amplifier board is mounted on the aluminum heat sink and performs modulation and amplification of the transmit carrier. The modulator incorporates vector feedback to reduce the distortion of the transmitted signal and control output power. Additional functions include Temperature Sensing/Fan switch and FWD and REFL power detection.

The transmit carrier is modulated using an IQ Modulator. The I DATA and Q DATA modulating signals are filtered using 3 pole active filters and applied to modulators Z1 and Z2 through summing amplifiers U14 and U15. The I and Q modulations are combined by PS2 and applied to the three stage power amplifier consisting of Q3, Q5, and Q6. The output of Q6 allows a peak power of 100 Watts which is filtered by a 7 pole low pass filter. The output of the low pass filter is sampled by the directional couplers and connected by coax to the T/R switch located on the RF/Analog board.

The 2-way directional coupler provides a forward power signal for the vector feedback and forward and reflected power signals for generation of the REF PWR by CR3 and U4 and FWD PWR by CR4 and U4 sense voltages.

U3 is a temperature sensing integrated circuit which provides a logic level for switching on a fan. Q7 provides the high current switch for the fan connected to J3. The on and off switch points are programmed by a three line serial data interface at power up.

Vector Feedback reduces distortion of the modulated signal and controls power output. The forward power sample from the directional coupler is input to the IQ demodulator, U6. The unmodulated carrier is input to U6 to demodulate the I and Q modulation signals. Proper phase of the carrier is established by the I CAL and Q CAL signals from the DSP controlling the Phase shifter U10. The I and Q demodulated signals are amplified by U7 and U9 then input to summing amplifiers U15 and U14. The summing amplifiers compare the input I DATA and Q DATA signals with the demodulated I and Q signals and adjusts the modulation drive to compensate for distortion caused by the modulators, summer, and power amplifier.

4-2.8 *Front Panel.* The Front Panel contains a four indicator LED's(i.e. Transmit, RX Signal Threshold, No Fault, and Power). and two replaceable air filters..

The Transmit indicator lights red when the unit is transmitting in any Mode. The RX Signal Threshold indicators lights amber when an incoming signal breaks the squelch threshold thereby indicating an incoming signal is being received. The No Fault indicator remains lighted, green, as long as no faults are detected in the unit. When a fault is detected the No Fault indicator will extinguish. The Power indicator remains lighted, green, as long as power is applied to the unit.

CHAPTER 5
MAINTENANCE INSTRUCTIONS

Section I. PREVENTIVE MAINTENANCE

5-1 INTRODUCTION.

This chapter contains both preventive and corrective operational level maintenance instructions. The information includes cleaning and lubrication, inspection, performance verification, troubleshooting, and subassembly removal and replacement.

5-2 CLEANING AND LUBRICATION.

Clean the external surfaces, front panel and the air inlet filter pads on the front panel every 2 weeks using a vacuum cleaner or small soft brush to remove any dirt or dust. The filter pads can be reused by rinsing with water, see section 5-6 for removal procedures. Do not use any cleaning agents. There are no lubrication requirements.

5-3 INSPECTION.

If the unit is faulty or suspected to be faulty perform a visual inspection as follows:

5-3.1 *External Inspection.*

1. Check front panel for physical damage.
2. Check external case for physical damage.
3. Check rear panel for physical damage.
4. Check rear panel connectors for corrosion and loose connectors.
5. Check rear panel cables for frayed or broken wires.

5-3.2 *Internal Inspection.*

WARNING

With the rear panel power switch set OFF and the power cord plugged into the power source, high voltage shock danger is present internally at the rear panel POWER receptacle/RFI filter, AC Line Filter board, and the rear panel circuit breaker.

CAUTION

When working on the receiver with covers removed and power applied, do not allow tools or metal objects to come in contact with receiver components. Equipment damage may occur.

CAUTION

Unit contains parts and assemblies sensitive to damage by electrostatic discharge (ESD). Use ESD precautionary procedures when touching removing or inserting parts.

1. Turn the unit off, and remove the power cord from the power source.
2. Using a no. 2 Phillips screwdriver, push down and turn all captive fasteners on the cover 1/4 turn counter-clockwise, and remove the covers.
3. Check for loose modules and circuit boards.
4. Check for loose connectors, corrosion, or burn marks.
5. Check for frayed or broken wires and cable ribbons.

5-4 PERFORMANCE VERIFICATION.

Because of the extensive built-in test equipment (BITE), the basic performance can be verified to a high degree of confidence with minimal external equipment. The following sections describe in detail the procedures to run the ATC-100 self verification tests.

5-4.1 *External Connections.*

1. Connect the power input to a suitable power source. Leave the power switched off at this time.

2. Connect a 50-ohm dummy load capable of dissipating 25 watts continuously and 100 watts peak to the Antenna jack.

3. Connect a serial COM1 or COM2 port of a DOS-based computer or a Windows™-based computer running a DOS window to the Maintenance port. In most instances a "Null Modem" cable or adapter is required. In many instances a gender adapter is required. Set the transceiver's rear panel DIP switches for the desired communications parameters as described in Chapter 3.

4. Power on the transceiver.

5. On the computer, run the Cubic-furnished program, RCOMM, and verify the settings. RCOMM remembers the settings the last time it was run. If running it for the first time, be sure to select the Serial interface: COM port 1 or 2 (Alt-I, 1 or 2). Then examine the serial line parameters at the bottom of the screen or window. If using the recommended Factory Default settings on the transceiver, the RCOMM settings should include
   a. Baud Rate = 38,400
   b. Data Bits = 8, no Parity
   c. Address = 0
   d. F/C (flow control) = OFF
   e. Terminator = <CR>
   f. Preamble = 1STX, 3ADR.

   If any parameters need to be changed, access the Configuration/Serial menu (Alt-C, S) and the parameter to be changed.

6. Verify communications with the transceiver by typing ID? and Return. You should see an ASCII message identifying the unit as an ATC-100 with a control software version and date. If so, proceed to transceiver performance verification.

5-4.2 *Transceiver Performance Verification*

1. Use the `PO?` query to obtain the results of the Power On Self Test. All zeros indicates no failures. Refer to Table 3-3 for the meaning of the individual result bits. If desired, use the `PO` command to repeat the tests.

2. Use the `BI?` query to obtain the results of the last BITE test sequence. All zeros indicates no failure. Refer to Table 3-3 for the test frequencies of the individual tests. If desired, use the `BI` command to repeat the test sequence. The BITE sequence conducts a receiver functional test at one frequency in each preselector band.

3. Use the `BR?` query to run the Remote BITE test and receive the results. Refer to Table 3-3 for details on the forward power, reflected power, VSWR, modulation percentage, MAR (receiver sensitivity margin).

If the BITE test reveals no failures and the Remote BITE indicates adequate forward power, low VSWR, adequate modulation percentage and MAR values, the unit is fully operational.

Section II. CORRECTIVE MAINTENANCE

5-5 TROUBLESHOOTING.

5-5.1 Troubleshooting Philosophy.
Certain assumptions are made concerning the troubleshooting approach as applied to the receiver as follows:

1. All point-to-point wiring is correct. Therefore, no malfunction is the result of a wiring (or cable connector) fault.

   NOTE
   Suspected failure of cables or connectors require visual inspection and continuity tests using the appropriate diagram. See FO-3 for interconnecting, schematic.

2. Malfunctions are non-interactive. Each symptom of a problem is caused by a single malfunction and no additional failures occurred during the troubleshooting process.
3. Multiple faults can be isolated if they are non-interactive.
4. Preventive maintenance has been performed (Section I).

5-5.2 *Built-In Tests.* The ATC-100 provides three types of testing: power-on self test (POST), built-in test equipment (BITE), and built-in test (BIT). Each is discussed below.

5-5.2.1 *POST.* The POST is performed automatically each time the receiver is powered on. Under firmware control, the POST sequences through a series of tests that checks the Control and DSP section of the Digital module, then activates the BITE check. If a failure is detected, the unit generates an audio tone in morse code describing error. Record the failure data. Depending on the failure, receiver functions may or may not be possible. If a BIT fault is detected after the POST, the unit will also generate an audio tone in morse code describing error. POST results are also reported over the remote control bus.

5-5.2.2 *BITE.* The BITE check is controlled by the firmware and is a sequence that checks the signal path with the BITE Generator. This test exercises the entire receiver signal path. Different frequencies are used to check each preselector filter. The BITE check is automatically performed during the POST, or may be selected manually at any time by the remote control bus. The audio output is disabled during the POST BITE check, but is enabled during the manual BITE check.

(See figure FO-2). During the BITE check, the Control section in the Digital module activates the BITE circuits through the shift register in the Preselector section of the RF Analog module.

5-5.2.3 *BIT.* During normal receiver operation, fault detectors are operating in the background. Table 5-1 lists the fault detectors, their locations and the fault signal sent to the Control section in the Digital module. If a fault is detected, the Control section stores the information in memory, causes the fault indication to be shown on the display, and sends the fault information over the remote control bus. The operator can view the current or cumulative faults (since power up) using the UTILITY FAULTS soft key menu.

Table 5-1 Fault Detectors.

Detector	Module Location	Fault Signal
$\overline{\text{LO FLT}}$	RF Analog	1st or 2nd LO out of lock
$\overline{\text{DSPC FLT}}$	RF Analog	DSP Clock out of lock
$\overline{\text{TX SYNTH FLD}}$	Transmit Synthesizer	TX Synthesizer out of lock
SELF TEST ADC	Digital Board	Power Supply Monitor
AUDIO DET	RF Analog	Detects audio output

5-5.3 *Troubleshooting Procedure.* Equipment troubleshooting should be performed in the following order:

1. Initial checks..
2. Fault identification
3. Front panel display interpretation.
4. Signal tracing (If required).
5. Subassembly replacement.

5-5.3.1 *Initial Checks.* If a problem is suspected conduct the following::

1. Check that the power switch is on and the Power and No Fault LED's on the front panel are lighted. If the Power and No Fault LED's are off, and the power switch is set to on, ensure that input power is correct.
2. Check for air flow into the unit from the front panel. The fan on the rear panel draws air through the filter on the front panel.
3. If an external reference frequency is used, try disconnecting it, and recheck the transceiver. Check for correct external reference frequency.

5-5.3.2 *Fault Identification.* Should the transceiver identify a fault, the "No Fault" LED on the front panel of the transceiver will extinguish.. Since the transceiver is designed to be operated remotely verification of the "No Fault" LED may not be a viable option. If a malfunction is suspected Several Radio Command Messages are available to help localize and determine the cause of the problem. These command messages are:

:? Request Interface Status Messages.
A? Request AGC status (on or off).
BI? Request BITE status.
BR? Request results of Remote BITE test.
C? Request a report of Radio Status Messages.
DACn Initiate DAC test.
DAC? Request condition of the DAC.
FA? Request a report of all accumulated faults.
FC? Request a report of all current faults.
FS? Request a fault summary report.
G? Request manual gain status setting.
IS? Request the audio input source.
PO? Request results of the most recent POST.
PS? Request status of the power supply voltages.
PWR? Request the transmitter power output.
R? Request receiver operating parameter status.
SS? Request signal strength in Mode 0.
SSH? Same as SS? except return value is in units of ½ dB.
SA? Request the audio output level in dBm.
SN? Request the carrier-to- noise measurement.
T? Request the Transmit/receive status.
TN? Request the frequency of the tone generator.
TO? Request the current transmitter offset frequency.
TT? Request the mode 0 transmit timer value.
VF? Request the vector feedback status.
VPC? Request the vector feedback values for the current frequency.
VFONE Runs the vector feedback calibration routine on the current frequency.
VPS? Displays the current power supply voltages.

A more detailed description of these commands is provided in chapter 3.

NOTE

When using the FA? or FC? Radio Commands the operator can determine the fault from table 3-3. To determine the meaning and the maintenance action to take in response to these fault messages, refer to table 5-2.

5-5.3.3 *Signal Tracing.* If the failed subassembly cannot be isolated using the initial check or fault identification interpretation, isolate the failed subassembly using conventional signal tracing techniques. Refer to chapter 4 for signal flow descriptions.

Signals are checked at various locations in the equipment using an RF signal generator and oscilloscope (see figures FO-3 and FO-4). Refer to SECTION 5-4 to pass a signal through the transceiver for signal tracing. Tables 2-1 through 2-5 lists signals at the rear panel connectors.

Table 5-2 Fault Messages.

Message	Meaning	Action To Take
Software error interrupt has occurred	Divide by zero or other software error has occurred. Normally innocuous and very rare.	If condition recurs, report to CCI factory engineers. Use R? query to identify all operation conditions at time of error.
1st or 2nd LO PLL out of lock	Phase Lock Loop (PLL) malfunctioning.	1. Recycle power. 2. If problem persists or recurs, replace RF Analog board.
DSP clock synthesizer PLL out of lock	Phase Lock Loop (PLL) malfunctioning.	1. Recycle power. 2. If problem persists or recurs, replace RF Analog board.
Transmit synthesizer PLL out of lock	Phase Lock Loop (PLL) malfunctioning.	1. Recycle power. 2. If problem persists or recurs, replace RF Analog board.
DSP processor not responding to requests	Digital Signal Processor or DSP Clock malfunctioning.	1. Recycle Power. 2. If problem persists or recurs, check 49.152 MHz DSP clock: a. If bad, replace RF Analog board. b. If good, replace Digital board.
EEPROM does not accept programming	EEPROM faulty.	Replace Digital board.
One of the serial ports has timed out while transmitting	Hardware handshake has presented timely transmission of a message from the transceiver.	1. Check handshake lines. 2. Check host software. 3. Try different baud rate.
Serial port overrun error	Character receive to fast for transceiver to process.	Verify that host respects RTS handshake.
Serial port parity error	Character received with incorrect parity.	1. Check line parameter settings. 2. Chose host line settings. 3. Choose no-parity mode of transmission.
Serial port framing error	Character received without required stop bit.	1. Check transceiver line parameter settings. 2. Check host line parameter settings for match.

5-6 SUBASSEMBLY REMOVAL AND REPLACEMENT.

The following procedures describe removal and replacement procedures for subassemblies at the maintenance operational level:

No internal adjustments (except audio line output) or component level maintenance should be performed at the operational level. These functions should be performed at the factory or an authorized repair depot.

WARNING

Turn off power and remove power cord before replacing subassemblies. Personnel injury or equipment damage may occur.

To remove the top cover, do the following: (Refer to figure FO-4 for locations.

Using a no. 2 Phillips screwdriver, push down and turn all captive fasteners on the cover 1/4 turn counter-clockwise, and remove the cover.

CAUTION

In the following procedures, to prevent damage to screw holes in the chassis, ensure screws are completely retracted before pulling the module or board from the chassis..

CAUTION

Module connectors may be difficult to separate. Pry gently on both sides of the connector to assist module removal.

NOTE

When removing subassemblies, save attaching hardware for subassembly replacement.

5-6.1 *RF Analog Board.*

1. Remove top cover.
2. Disconnect the 4 ribbon cable connectors J2, J3, J5, & J7 and the single column wire connector J1 from the board.
3. Using an Engage/Disengage OSMT Cable Tool, disconnect coax cables from J8, J9, J11, & J12.
4. Disconnect the two coax cable connectors:
   a. Disconnect the antenna coax connector (J4) from the board.
   b. Disconnect J10 coax connector from the board.
5. Using a no. 1 Phillips screw driver remove the 7 screws from the top of the board.
6. Lift the board out of the chassis and turn over.
7. Using a 5/16 in. wrench, disconnect the 2 coax cable SMA connectors from the TX Synthesizer Module.
8. Using a no. 1 Phillips screw driver remove 7 screws that attach the metal plate to the RF Analog board.
9. Lift the board from the plate.
10. To replace, reverse removal procedures.

5-6.2 *TX Synthesizer Module.*

1. Remove the top cover.
2. Remove the RF Analog Board:
   a. Using a no. 1 Phillips screw driver remove the 7 screws from the board.
   b. Lift the board out of the chassis and turn over
   c. Using a 5/16 in. wrench, disconnect the 2 coax cable SMA connectors from the TX Synthesizer Module.
   d. Using a no. 1 Phillips screw driver remove 7 screws that attach the metal plate to the RF Analog board.
   e. Lift the board from the plate.
3. Using a no. 1 Phillips screw driver, remove 4 screws from the metal plate that are connected to the TX Synthesizer Module.
4. To replace, reverse removal procedures.

5-6.3 *Digital Board.*

1. Remove the top cover.
2. Remove the RF Analog Board:
   a. Using a no. 1 Phillips screw driver remove the 7 screws from the board.
   b. Lift the board out of the chassis.

2. Disconnect 4 ribbon cables connectors J1, J2, J5, J6 and the dual column wire connector J9 from the Digital Board.
3. Using an Engage/Disengage OSMT Cable Tool, disconnect the coax cable from J7 & J8.
4. Using a 5 mm socket driver, unscrew the 2 lugs from each of the rear panel's 25 pin female connectors J3 & J4.

CAUTION

When removing board from chassis ensure that the connectors J3 & J4 do not hang up on the rear panel chassis.

5. Using a no. 1 Phillips screw driver, remove the screws from the underneath portion of the chassis that screws to the Digital Board.
6. To replace, reverse removal procedures.

5-6.4 *Power Amplifier Module.*

1. Remove the top cover.
2. Disconnect the 3 cables GND (J4), +28 VDC (J1), & J3.
3. Disconnect the ribbon cable J2.
4. Disconnect the coax cable E3 from the RF Analog board.
5. Remove the RF Analog Board:
   a. Using a no. 1 Phillips screw driver remove the 7 screws from the board.
   b. Lift the board out of the chassis and turn over.
6. On the Power Amplifier Module, locate the coax cable E4.
7. Using a 5/16 in. wrench, disconnect the coax cable, E4, SMA connector from the TX Synthesizer Module.
8. Turn the transceiver on its side. Using a no. 1 Phillips screw driver, remove the 8 screws from the bottom of the chassis that secure the PA Module.
9. Lift the Module out (heat sink & board).
10. To replace, reverse removal procedures.

5-6.5 *Power Supply.*

1. Remove the top cover.
2. Disconnect single column connectors J1 & J2.
3. Turn the transceiver on its side. Using a no. 1 Phillips screw driver, remove the 4 screws from the bottom of the chassis that secure the power supply.
4. Lift the power supply up at an angle from the bracket side.
5. To replace, reverse removal procedures.

5-6.6 *AC Line Filter Board.*

1. Remove top.
2. Disconnect wire connections J1 thru J4 from the AC Line Filter Board.
3. Turn the transceiver on it side. Using a no. 1 Phillips screw driver, remove the 4 screw from the bottom of the chassis that secure the AC Line Filter Board.
5. Lift board from unit.
6. To replace, reverse removal procedures.

5-6.7 *Receptacle/RFI Filter.*

1. Remove top cover.
2. Using no. 1 Phillips screwdriver remove the 2 screw from the rear panel that secure the power receptacle to the rear panel.
3. Pull the Receptacle out from inside the transceiver and disconnect the 3 wire connectors from the rear of the receptacle.
4. To replace, reverse removal procedures.

5-6.8 *Power Switch/Circuit Breaker.*

1. Remove top cover.
2. Using a 9/16 in. wrench, remove the nut that secures the power switch to the outside rear panel.
3. Pull switch out through the inside of the chassis.
4. Using a no. 2 Phillips screw driver, remove the 2 wires from the rear of the power switch.
5. To replace, reverse removal procedures.

5-6.9 *Fan Assembly.*

1. Remove top cover.
2. Disconnect the fan cable from the PA Module J3.
3. Using a no. 1 Phillips screw driver and 3/16 in. wrench, remove 4 screws and attaching hardware from the fan assembly.
4. Lift fan from chassis.
5. To replace, reverse removal procedures.

5-6.10 *Air Inlet Filter Pads.*

1. Starting at the top of the filter pad cover, gently lift and pry back.
2. Work the sides and bottom and gently pull cover off.

CAUTION

The cover is held on by plastic clips. Excessive pulling may damage the cover.

3. Lift out filter pad.
4. To replace, reverse removal procedures.

5-6.11 *Support Handles*

1. Remove top cover.
2. Using no. 2 Phillips screwdriver, remove 2 screws securing handles to front panel.

NOTE:
To remove the handle near the RF Analog Board an offset screw driver is required. If an offset screw driver is not available then perform step 3 & 4.

3. Remove the RF Analog Board.
   a. Using a no. 1 Phillips screw driver remove the 7 screws from the board.
   b. Lift the board out of the chassis.
4. Using a no. 2 Phillips screw driver, remove the lower screw.
5. To replace, reverse removal procedures.

5-7 SOFTWARE UPLOADING.

The transceiver's control and DSP software may be replaced using the Maintenance connector J2 on the rear of the unit to gain access to the unit's flash memory. The upload may be done using a DOS-based personal computer with a serial bus null-modem cable and one of the COMM ports on the PC.

To upload software to the transceiver control and DSP processors, refer to section 3-1 of the manual.

CHAPTER 6
PREPARATION FOR RESHIPMENT

6-1 INTRODUCTION.

This chapter contains information to prepare the unit for reshipment including disassembly and removal from the rack mount, packaging, and shipping.

6-2 DISASSEMBLY AND REMOVAL.

To disassemble and remove the unit from the rack mount, perform the following procedures:

1. Ensure the power is set to off.
2. Disconnect the input power cable.
3. Disconnect all cables from the rear panel.
4. Remove the unit from the rack mount if used.

6-3 PACKAGING.

NOTE
The unit should be packed in the original shipping container if available.

To package the unit for reshipment perform the following steps:

1. Ensure that there is sufficient foam packing material in the shipping container to protect the unit from any hard impact.
2. Cover the unit with foam or bubble-type packing material.
3. Place the unit in the center of the shipping container.
4. If using a cardboard packing carton, securely tape the seams of the carton's top cover, bottom cover, and side flaps with reinforced packing tape.
5. Attach labels or stamp in indelible ink the word FRAGILE on the top, bottom, and all sides of the container.

6-4 SHIPPING.

CAUTION

Unit contains parts and assemblies sensitive to damage by electrostatic discharge (ESD). Do not ship or store near strong electrostatic, electromagnetic, magnetic or radioactive fields.

There are no special shipping requirements for the unit. Commercial or military surface or air shipping services may be used.

CHAPTER 7
STORAGE

7-1 INTRODUCTION.

This chapter contains information for storage of the equipment including environmental conditions and any special preservation requirements.

7-2 STORAGE ENVIRONMENT.

The receiver should be stored indoors in the original shipping container (or similar container) as described in chapter 6. The humidity should be between 40 and 90% (non-condensing) with a temperature range of -20 to +70°C.

CAUTION

Unit contains parts and assemblies sensitive to damage by electrostatic discharge (ESD). Do not ship or store near strong electrostatic, electromagnetic, magnetic or radioactive fields.

7-3 PRESERVATION.

There are no special coverings or preservation materials required to store the receiver.

CHAPTER 8
PARTS LIST

8-1 INTRODUCTION.

This chapter contains the parts list for replaceable modules and chassis-mounted components at the operational maintenance level.

8-2 REPLACEABLE PARTS LISTING.

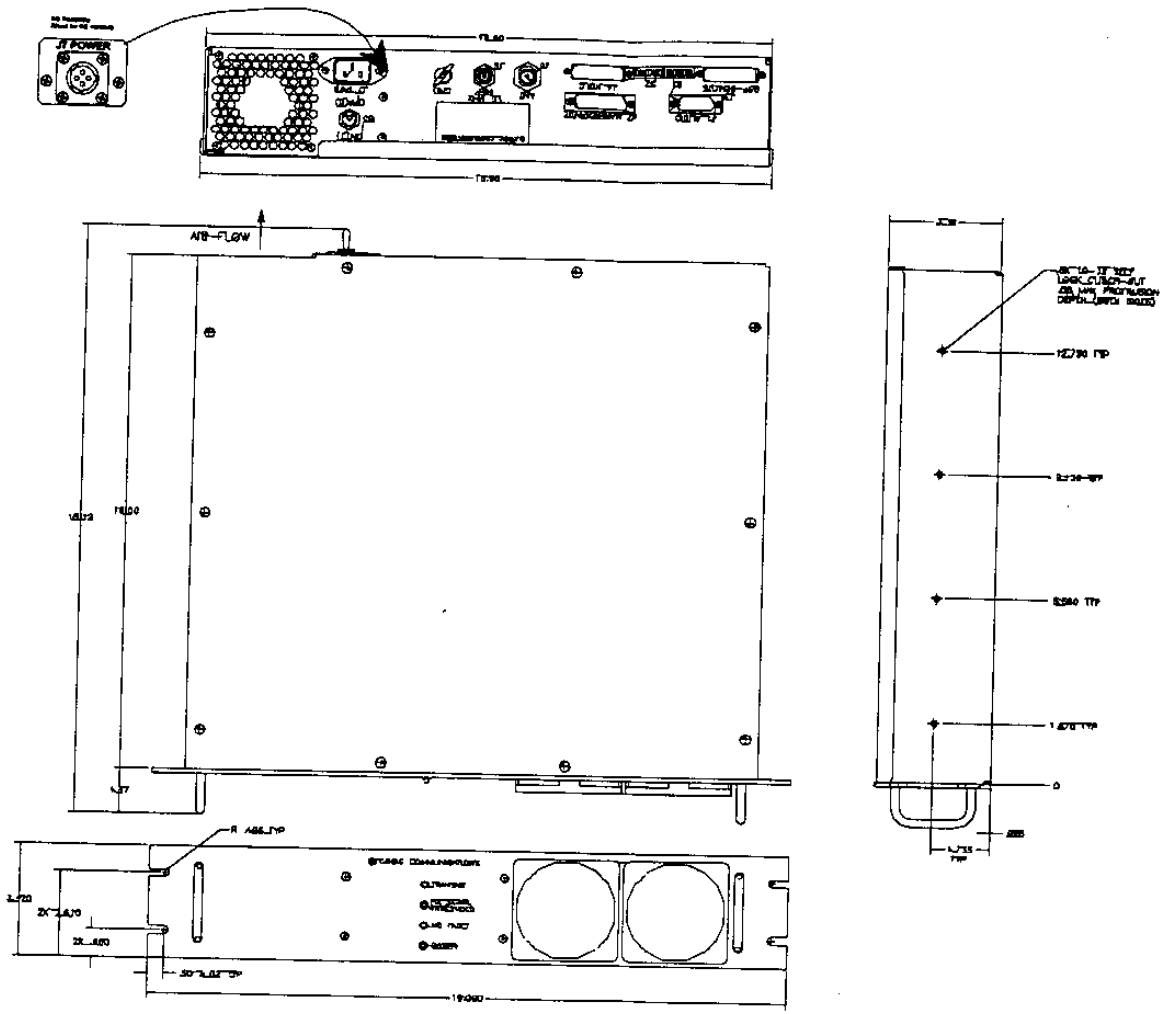
Table 8-1 lists replaceable modules and chassis-mounted components for the unit. (See figure FO-4 for locations.)

Table 8-1 Replaceable Parts.

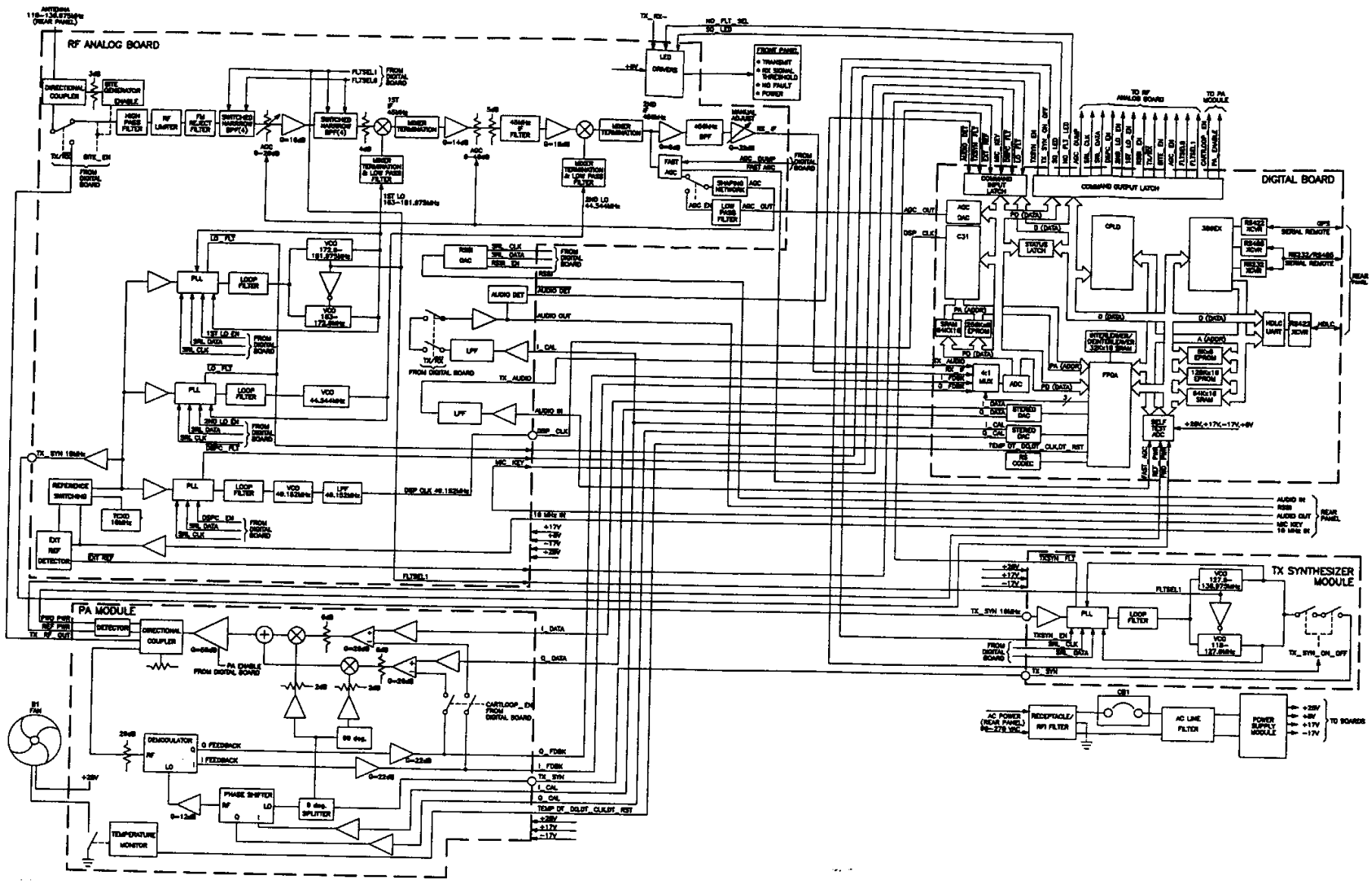
Qty	Description	Part Number	Remarks	Mfr
1	Board, AC Line Filter	260340-2		CCI[1]
1	Board, DC Line Filter	2608-2015-2	Optional, DC version only	CCI
1	Board, Digital	3003-2003-1		CCI
1	Board, RF Analog	3003-2002-1		CCI
1	Cable Assy, Fan	115-030	Includes fan	CCI
2	Handle, Support	222-086		CCI
1	Module, Power Amplifier	3003-1104-1		CCI
1	Module, Transceiver Synthesizer	3003-1108-1		CCI
1.	Power Cord, AC	696-012	Not Shown	
1	Power Supply, AC	275-015		CCI
1	Power Supply, DC	275-017	Optional, DC version only	CCI
1	Power Switch/Circuit Breaker, AC	482-088		CCI
1	Power Switch/Circuit Breaker, DC	482-091	Optional, DC version only	CCI
1	Receptacle/RFI Filter, AC	343-007	DC receptacle is not a replaceable part	CCI

[1]Cubic Communications, Inc. (FSCM 59532)

PRELIMINARY



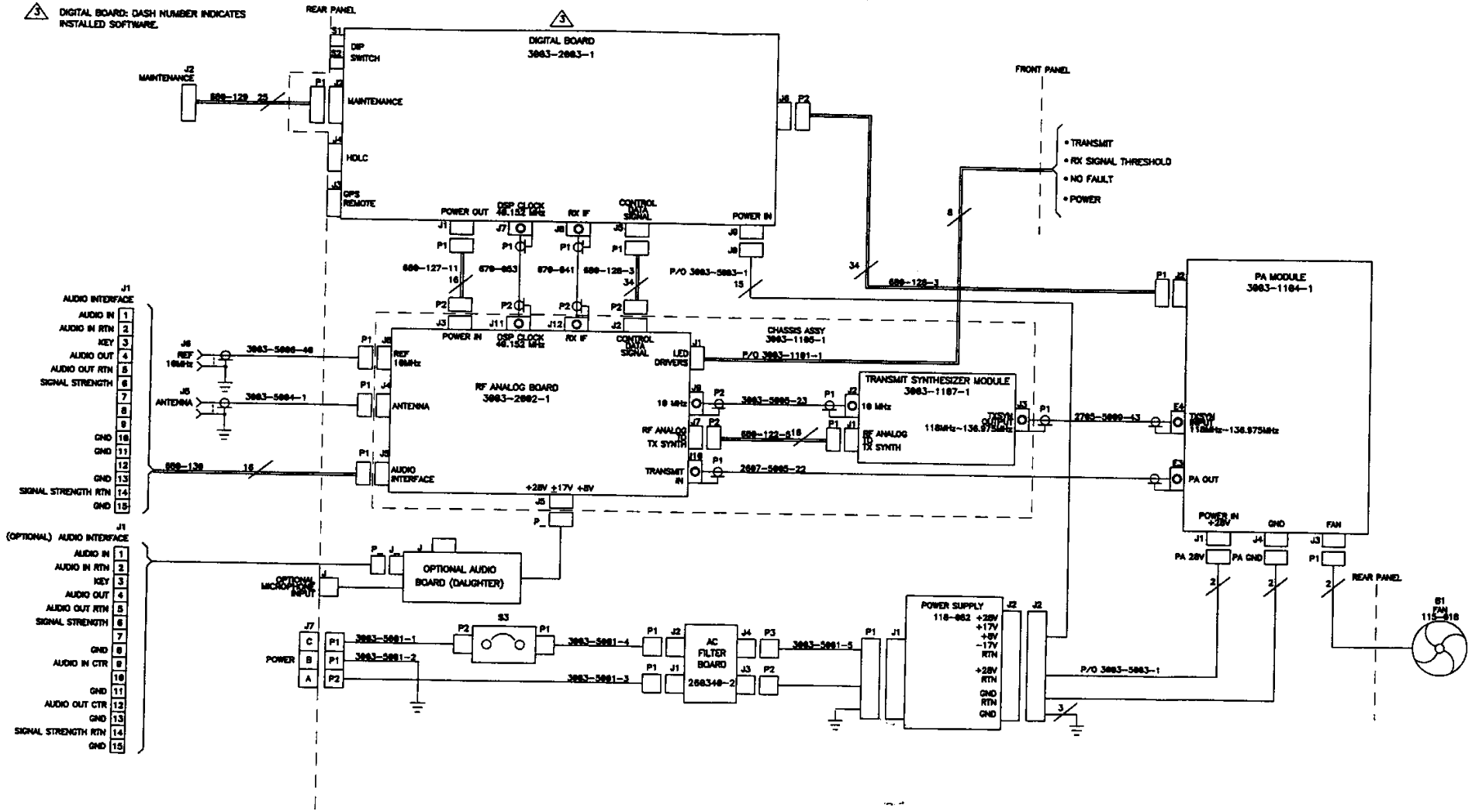
FO-1. ATC-100 Outline and Mounting Drawing.



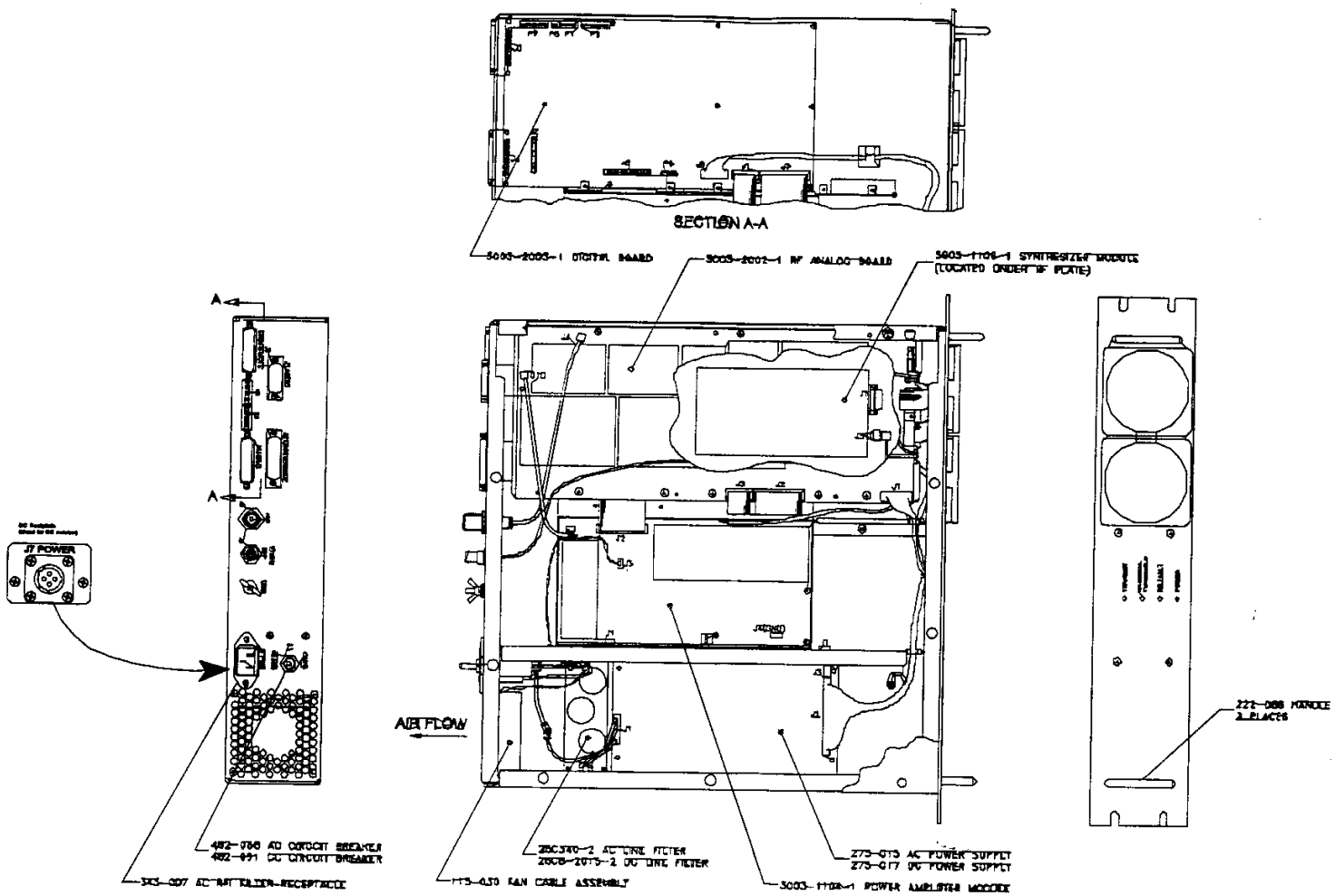
FO-2. ATC-100 Block Diagram.

NOTES: UNLESS OTHERWISE SPECIFIED

1. XX / INDICATES NUMBER OF CONDUCTORS IN CABLE.
2. ═══ INDICATES RIBBON CABLE.
3. DIGITAL BOARD: DASH NUMBER INDICATES INSTALLED SOFTWARE.

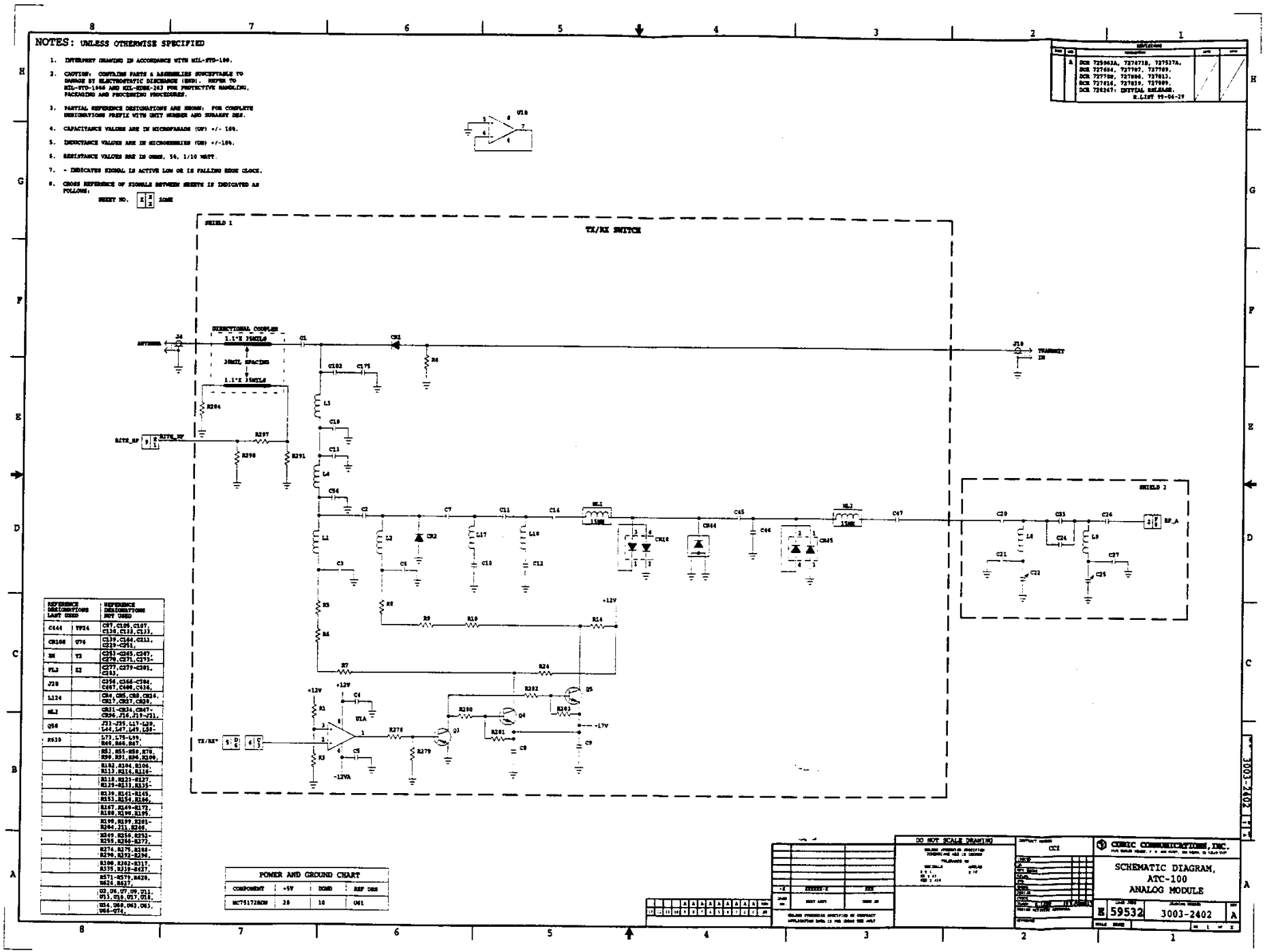


FO-3. *ATC-100 Interconnect Diagram.*

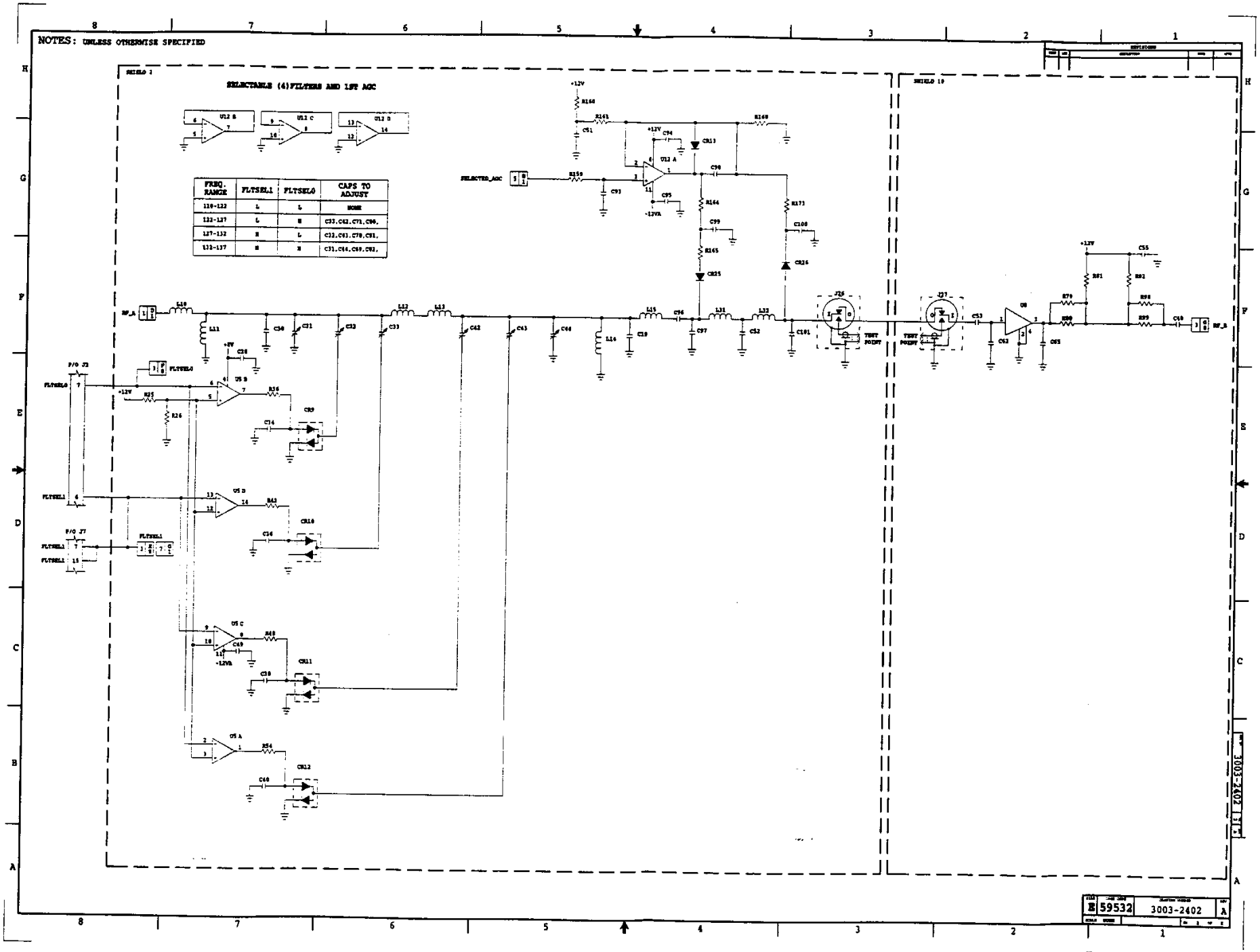


3003-1022

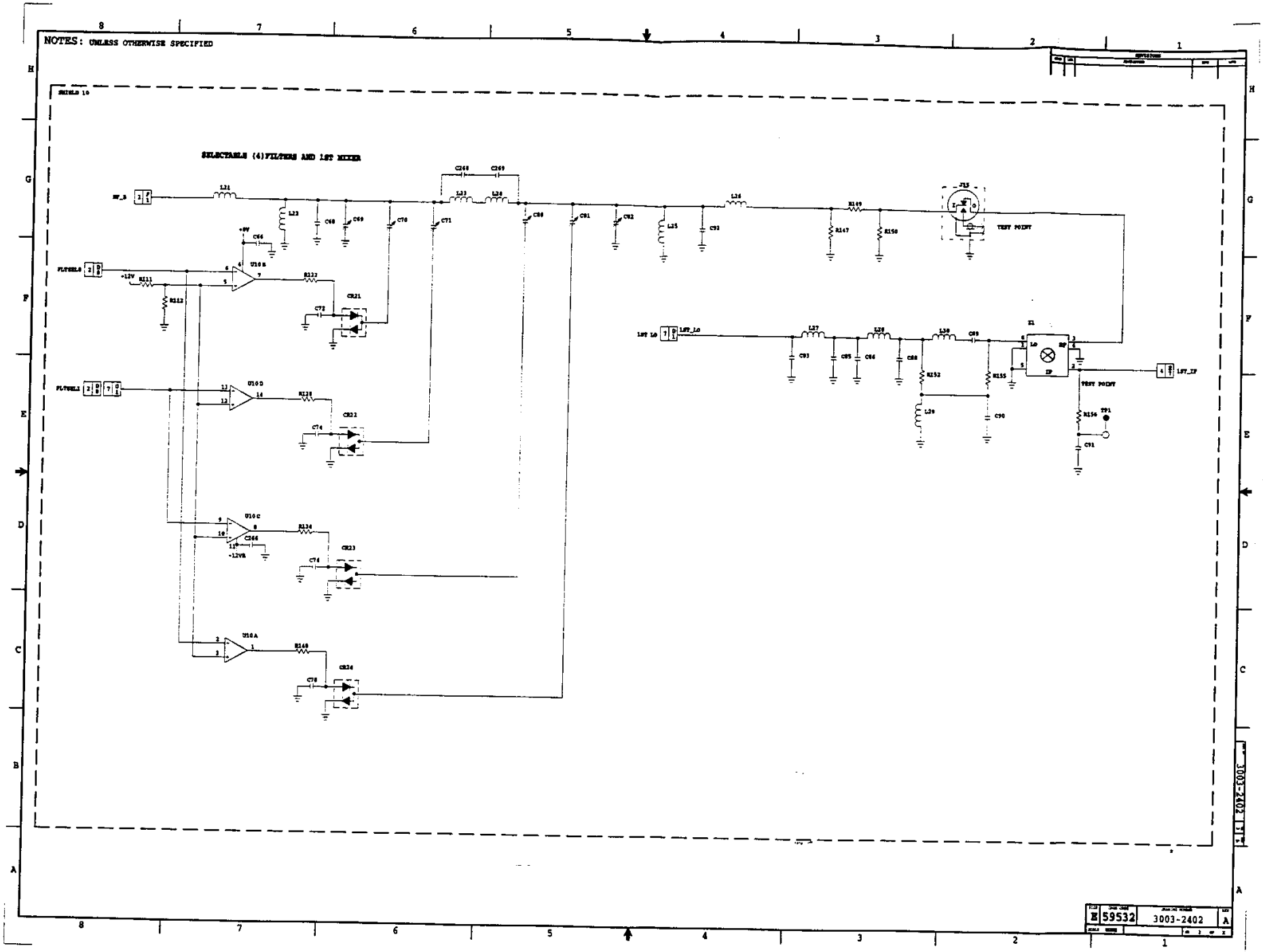
FO-4. ATC-100 Replaceable Parts Locator Diagram.



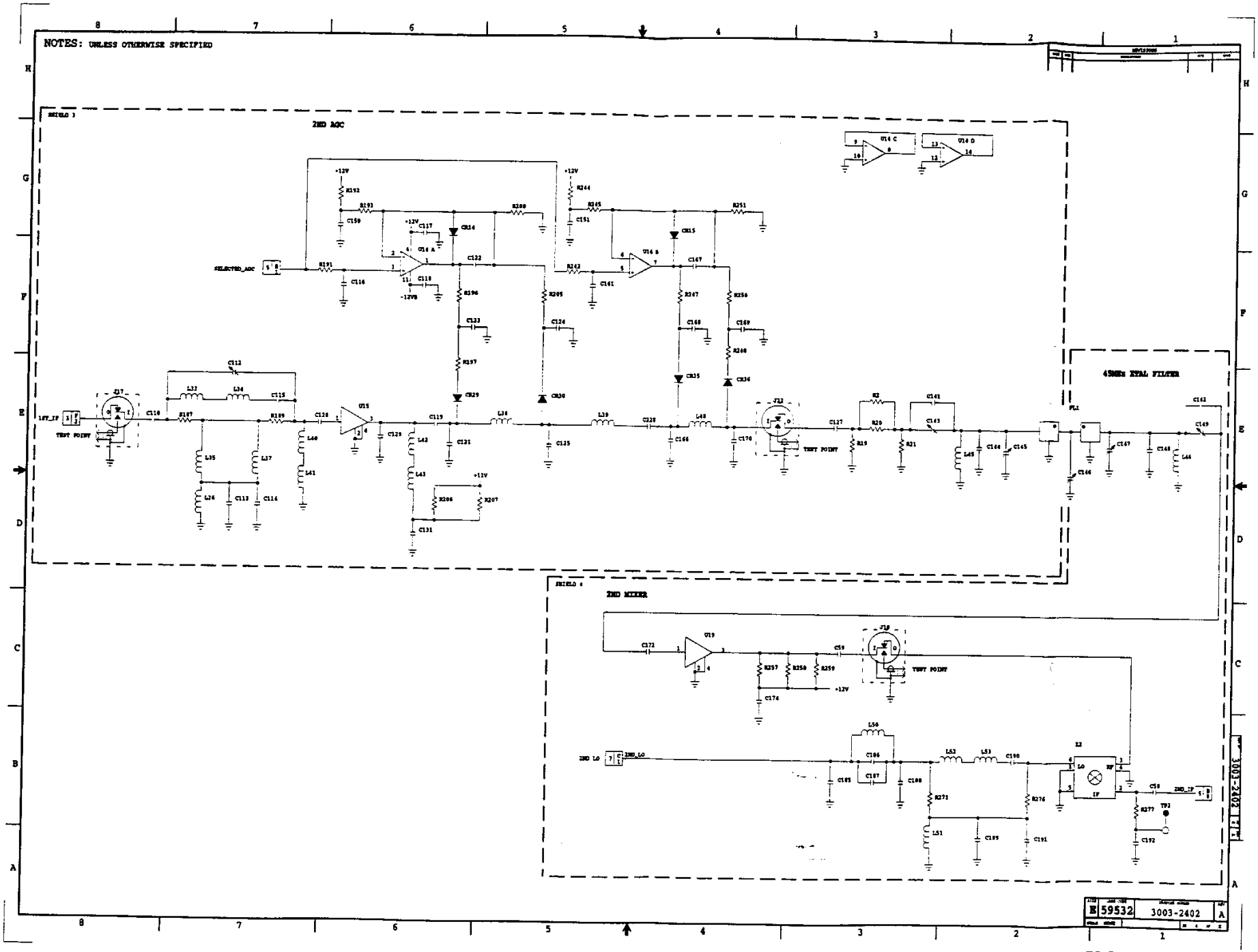
FO-5. ATC-100 Schematic Diagram, Analog Modu
FP-9/(FP-10 blan



FO-5. ATC-100 Schematic Diagram, Analog Modul
FP-11/FP-12 blan

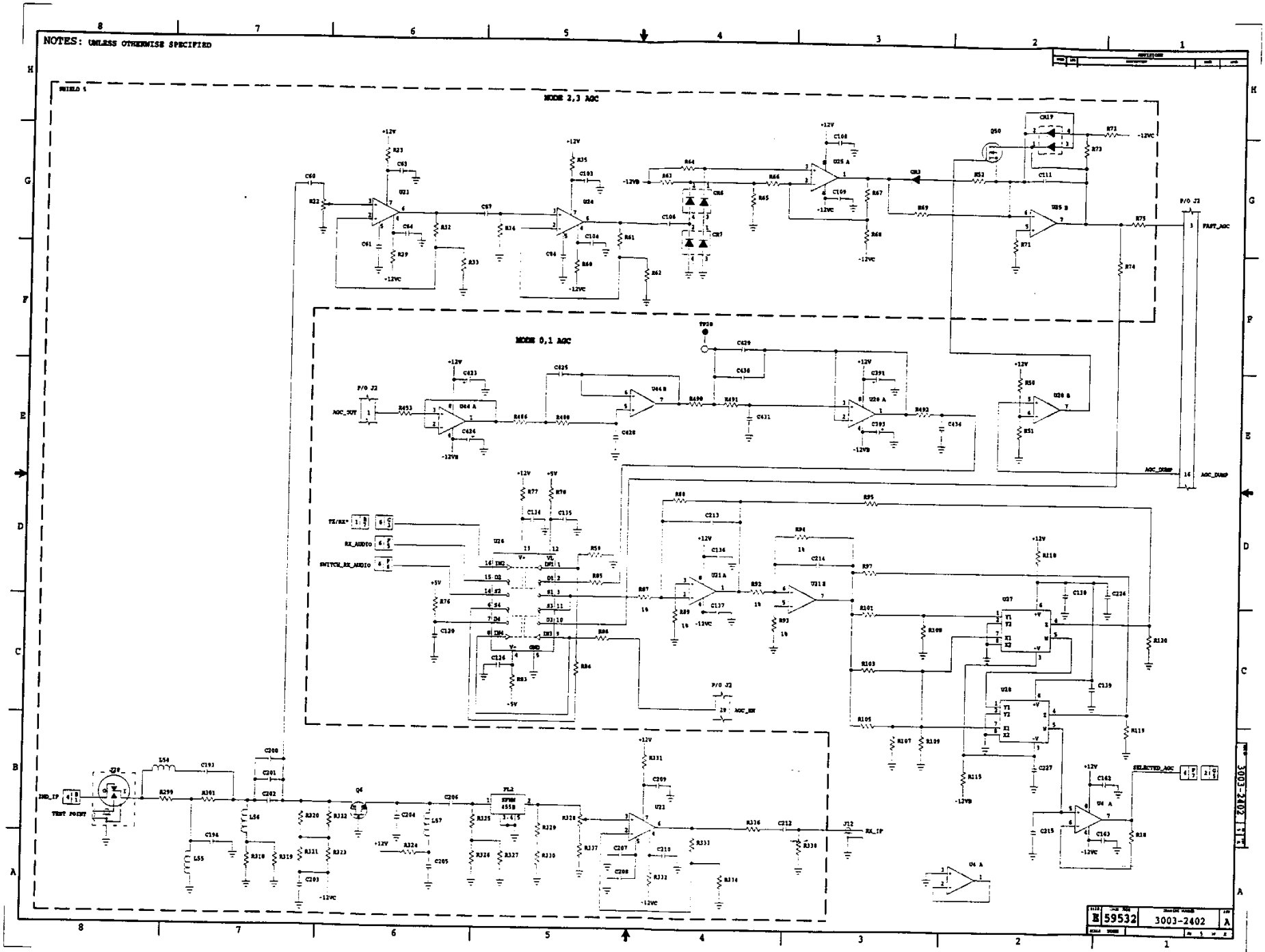


FO-5. ATC-100 Schematic Diagram, Analog Modu
FP-13/(FP-14 blar

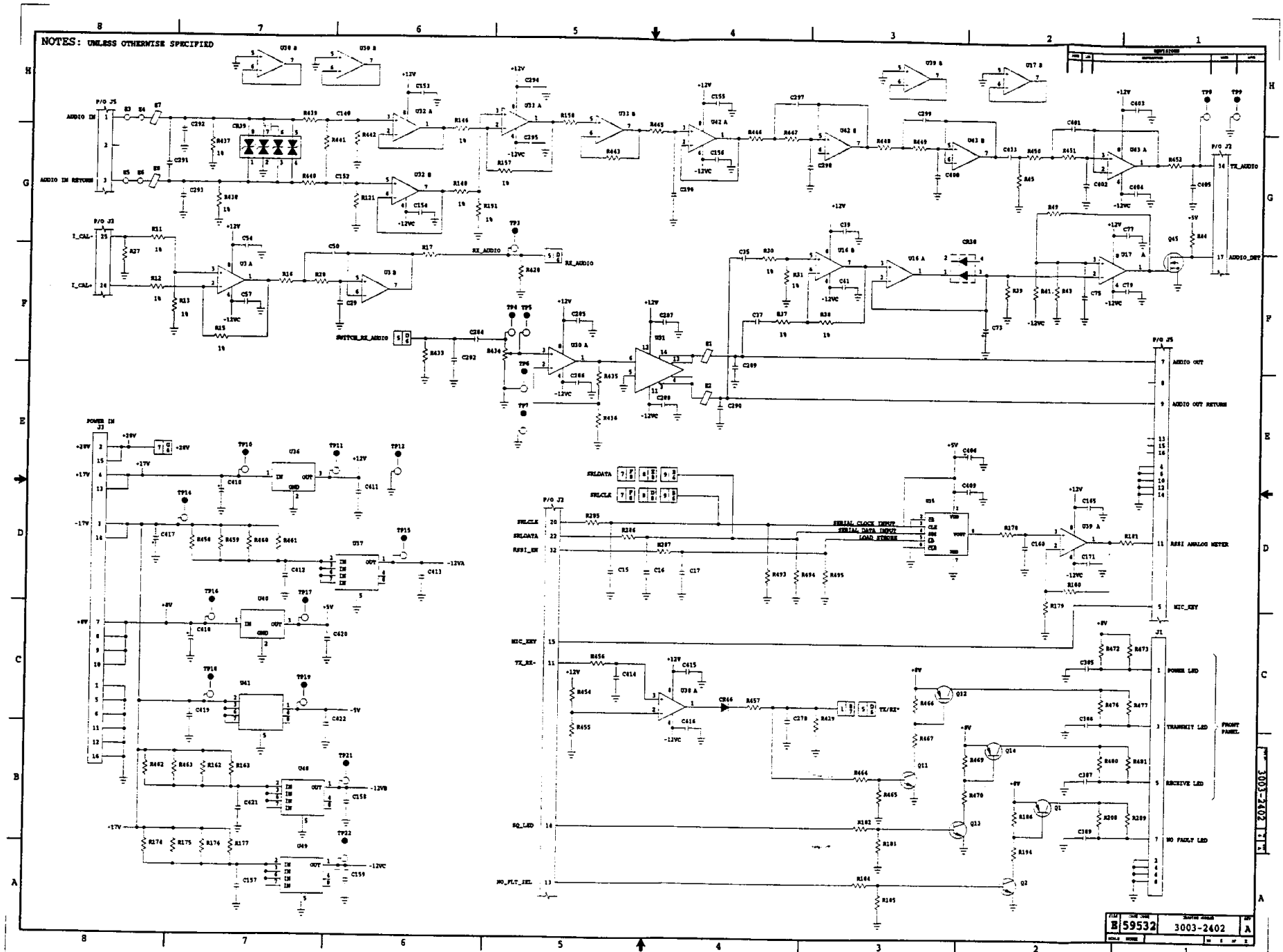


FO-5. ATC-100 Schematic Diagram, Analog Modu

FP-15/(FP-16 bla

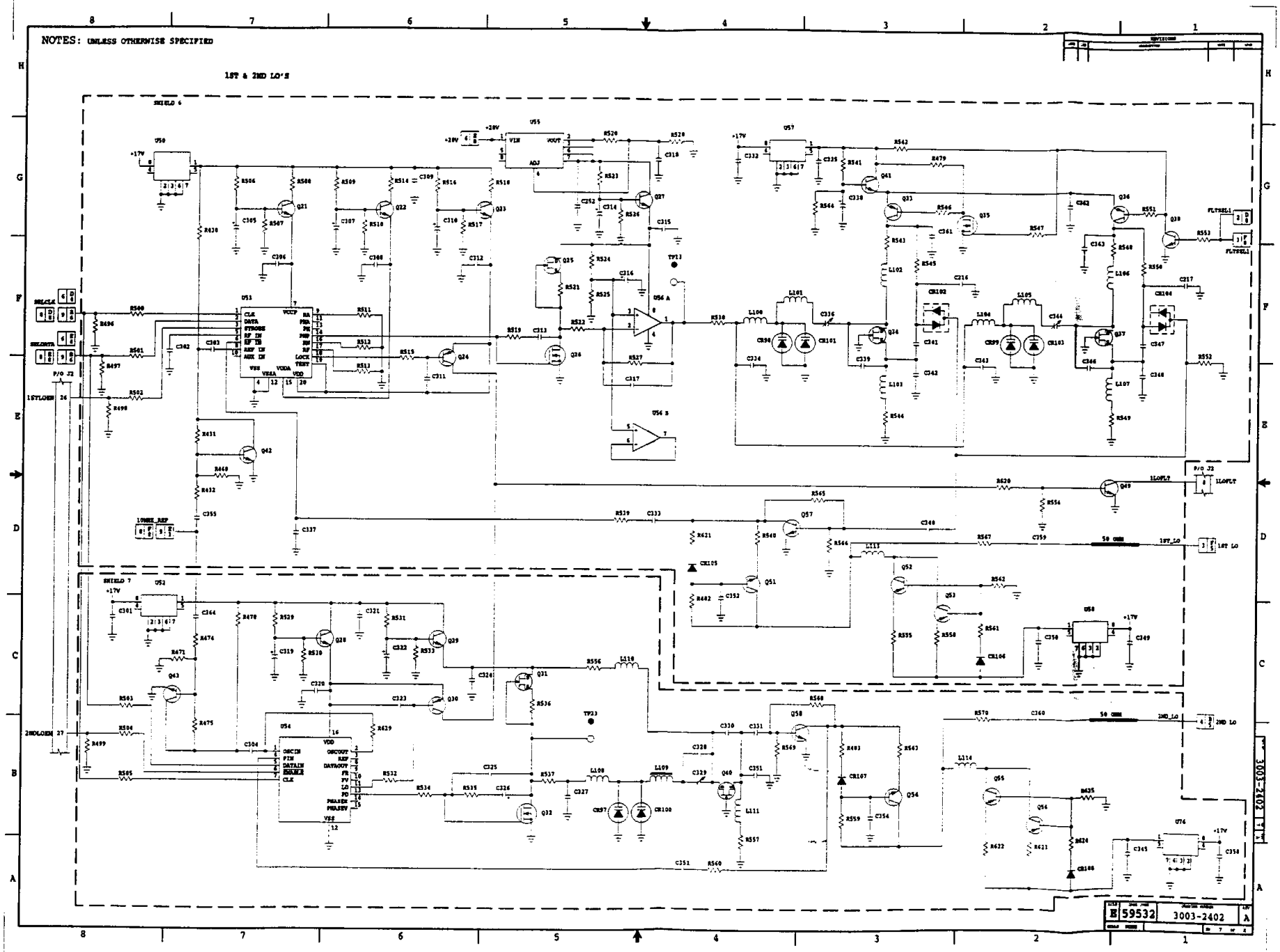


FO-5. ATC-100 Schematic Diagram, Analog Modu
FP-17/IFP-18 blar

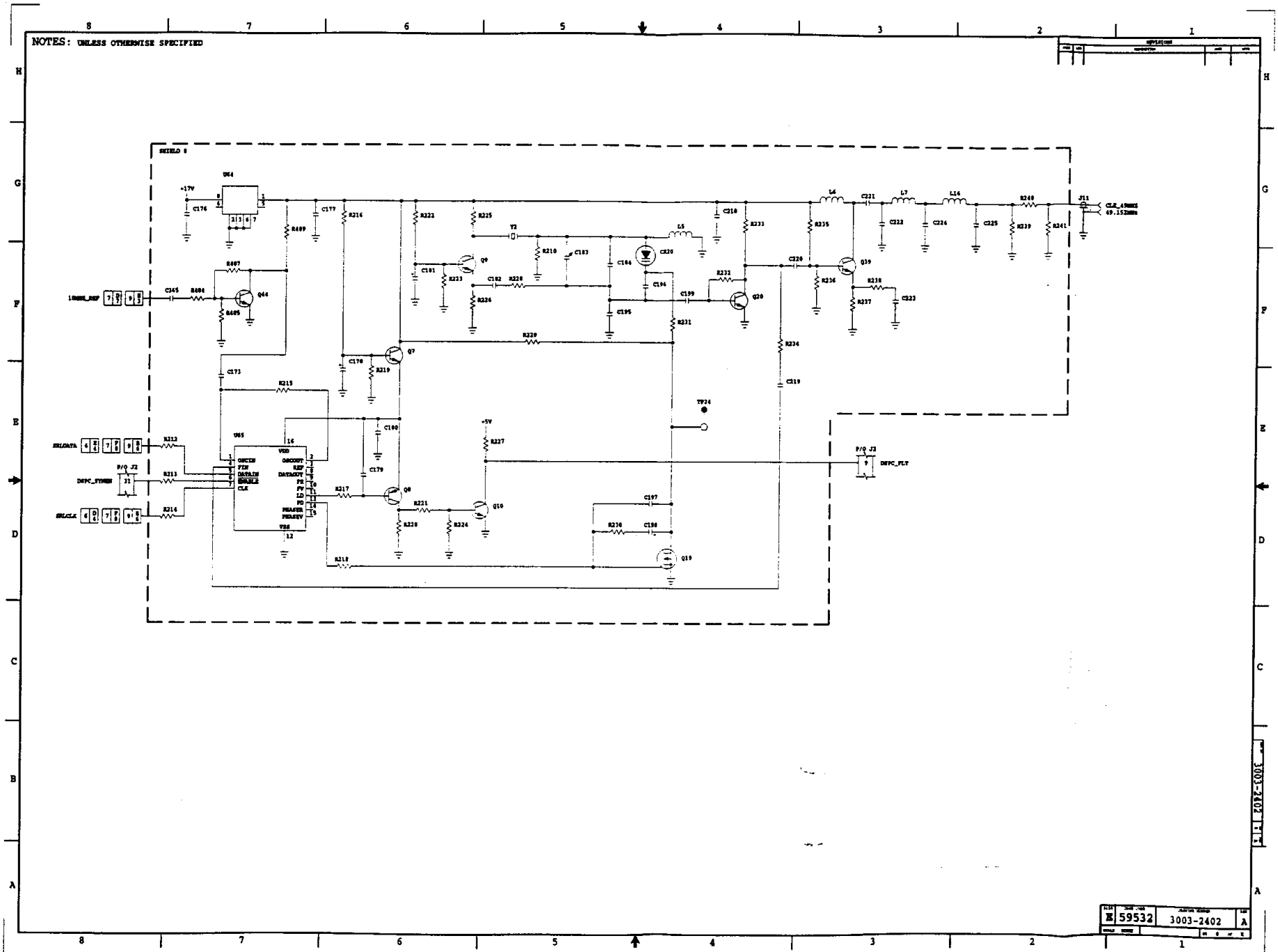


FO-5. ATC-100 Schematic Diagram, Analog Modul

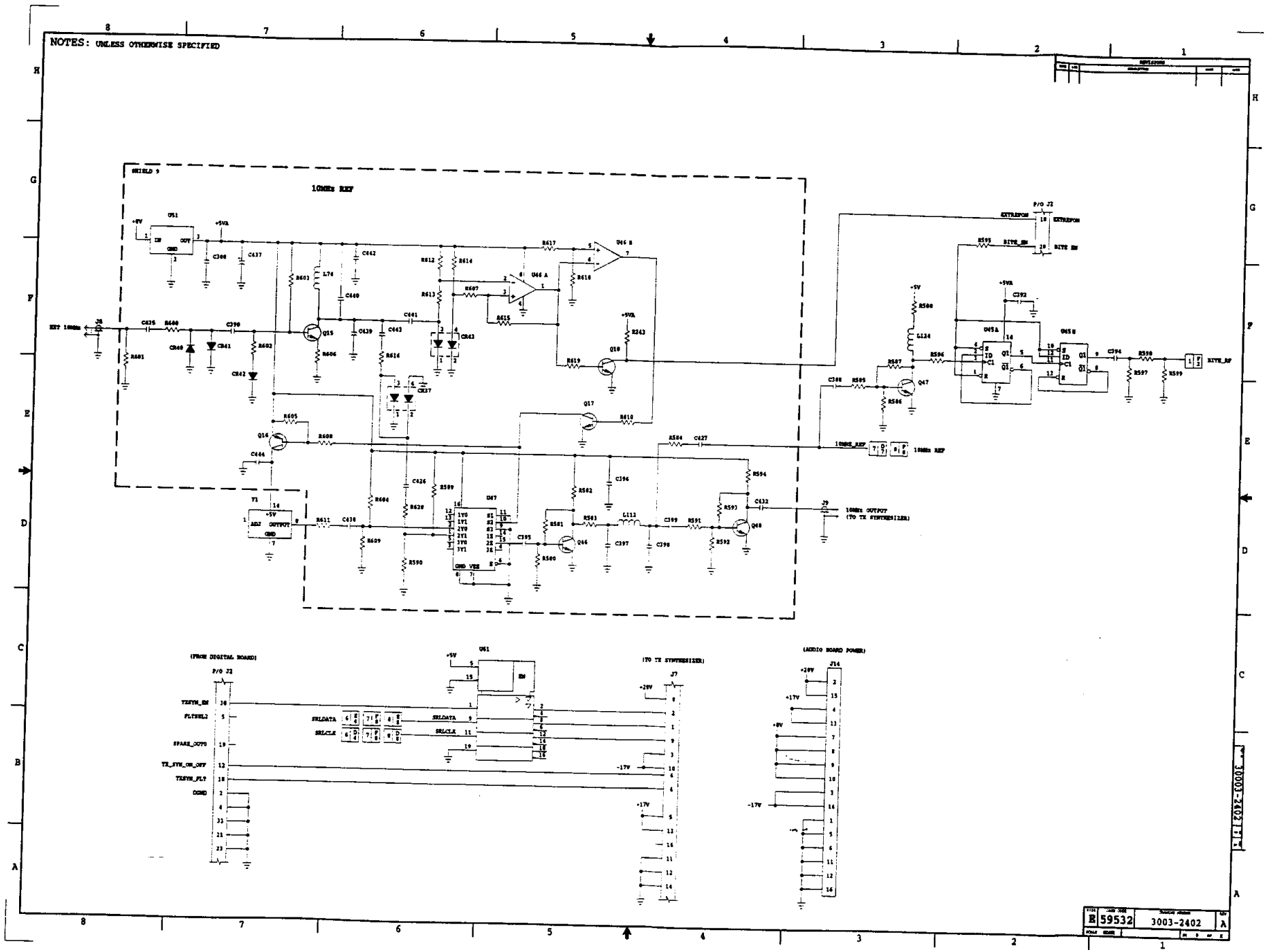
ED-19I/ED-20 blan



FO-5. ATC-100 Schematic Diagram, Analog Modul
FP-21/FP-22 blan



FO-5. ATC-100 Schematic Diagram, Analog Modu
FP-23/(FP-24 bla



FO-5. ATC-100 Schematic Diagram, Analog Modul
FP-25/FP-26 blan