CYW20732S

Bluetooth Low Energy SiP Module

Doc. # 002-15222 Rev. *G

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Preface

This document provides descriptions of the interfaces, pin assignments, and specifications of Cypress CYW20732S Bluetooth Low Energy (BLE) System-in-Package (SiP) module. It is intended for designers who are responsible for adding the CYW20732S module to wireless input devices including heart-rate monitors, blood pressure monitors, proximity sensors, temperature sensors, and battery monitors.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 2-1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20732	CYW20732
BCM20732S	CYW20732S

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to http://www.cypress.com/glossary.

Document Conventions

The following conventions may be used in this document:

Convention	Description
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
Monospace	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

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1. Introduction

1.1 Overview

The CYW20732S is a compact, highly-integrated Bluetooth low-energy (BLE) system-in-package (SiP) module. The CYW20732S SiP includes an embedded BLE antenna, 24 MHz clock, and 512 Kb EEPROM, so only a minimal set of external components is needed to create a standalone BLE device.

The CYW20732S is designed to accelerate time-to-market. The Bluetooth stack and several application profiles are built into the module, allowing customers to focus on their core applications. To further reduce application development time, the CYW20732S includes integrated software support, with one-click installation of the complete environment and a one-click compile/build/link/load cycle. All this, coupled with an ultra-small form factor and support for a wide voltage range, makes the CYW20732S well suited for virtually any Bluetooth Smart application.

1.1.1 Features

- ARM Cortex-M3 microcontroller unit (MCU)
- Embedded 512 Kb EEPROM
- Broadcom Serial Control (BSC), SPI, and UART interfaces
- FCC and CE compliant
- RoHS compliant, certified lead- and halogen-free
- Moisture Sensitivity Level (MSL) 3 compliant
- 6.5 mm × 6.5 mm × 1.2 mm Land Grid Array (LGA) 48-pin package

1.1.2 Application Profiles

The following profiles are supported in CYW20732S ROM:

- Battery status
- Blood pressure monitor
- Find me
- Heart rate monitor
- Proximity
- Thermometer
- Weight scale
- Time
- Blood glucose monitor

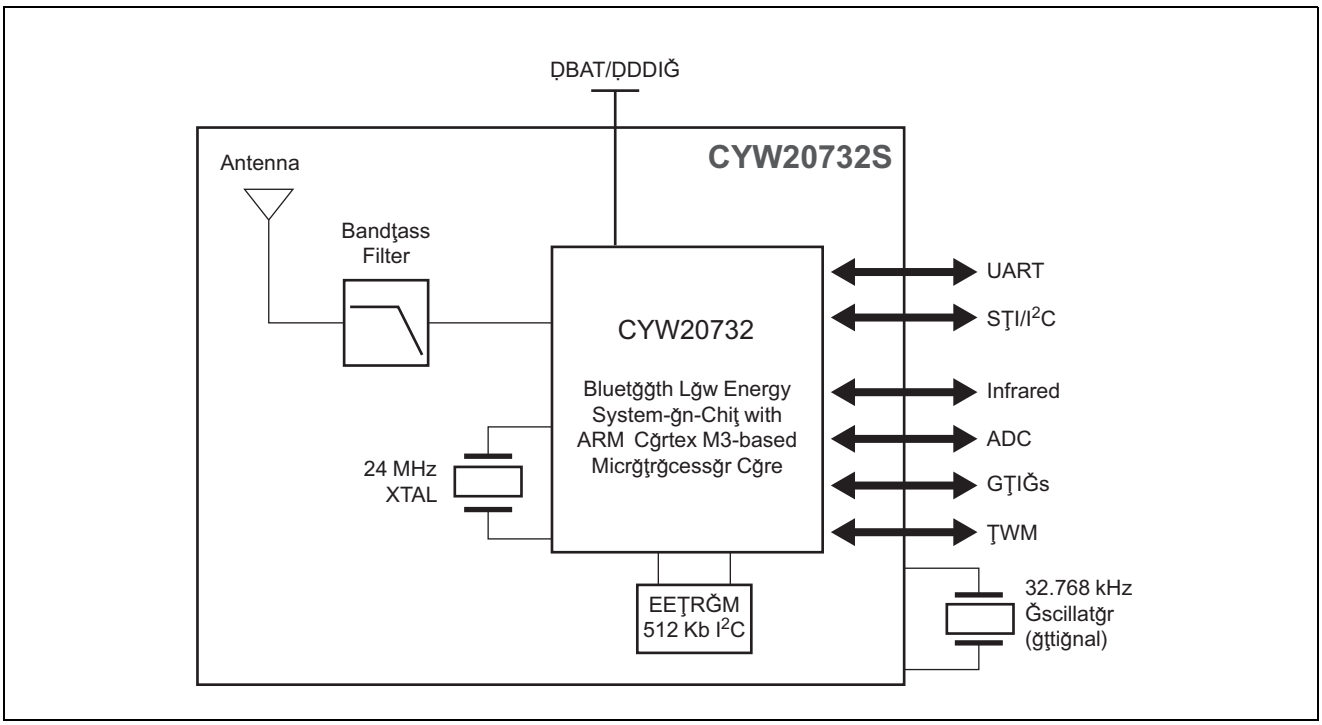
Additional profiles that can be supported in CYW20732S RAM include:

- Blood glucose monitor
- Temperature alarm
- Location
- Other custom profiles

1.1.3 Block Diagram

A block diagram of the CYW20732S BLE SiP is shown in Figure 1-1.

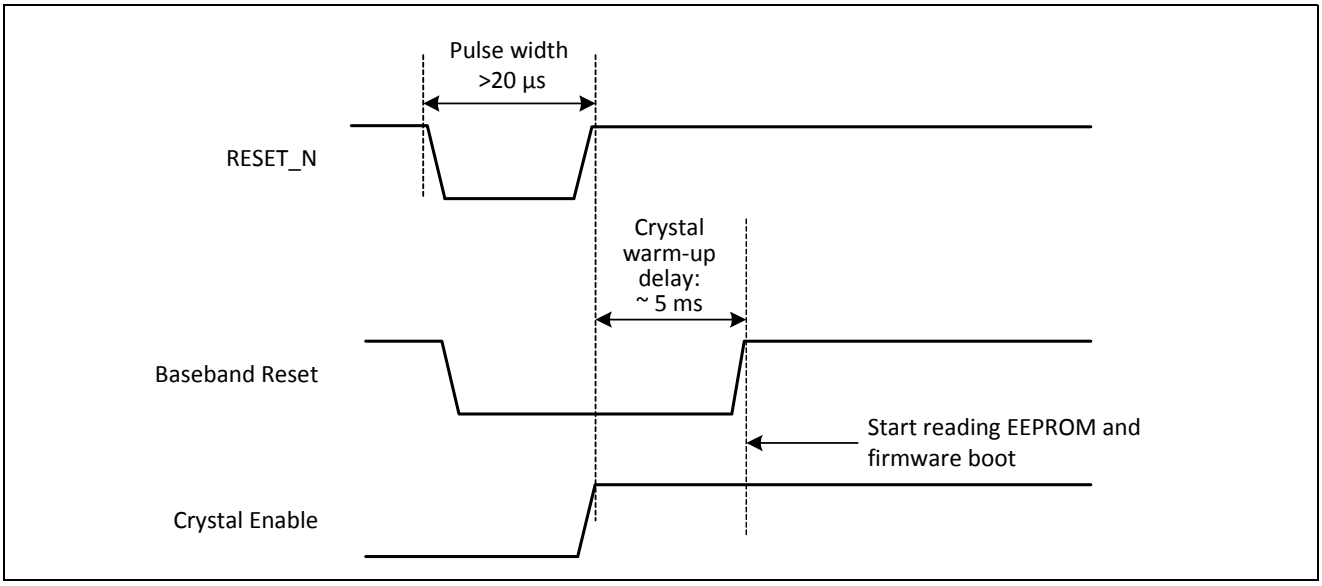
Figure 1-1. CYW20732S BLE SiP Block Diagram



1.1.4 External Reset

External reset timing for the CYW20732S is illustrated in Figure 1-2.

Figure 1-2. External Reset Timing



1.1.5 32.768 kHz Oscillator

The CYW20732S includes a standard Pierce oscillator. The oscillator circuit includes a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis eliminates chatter when the input is near the comparator threshold (~100 mV). The oscillator circuit can is designed for a 32 kHz or 32.768 kHz crystal oscillator, and can also be driven by an external clock input with a similar frequency. Characteristics for a 32 kHz oscillator are defined in Table 1-1.

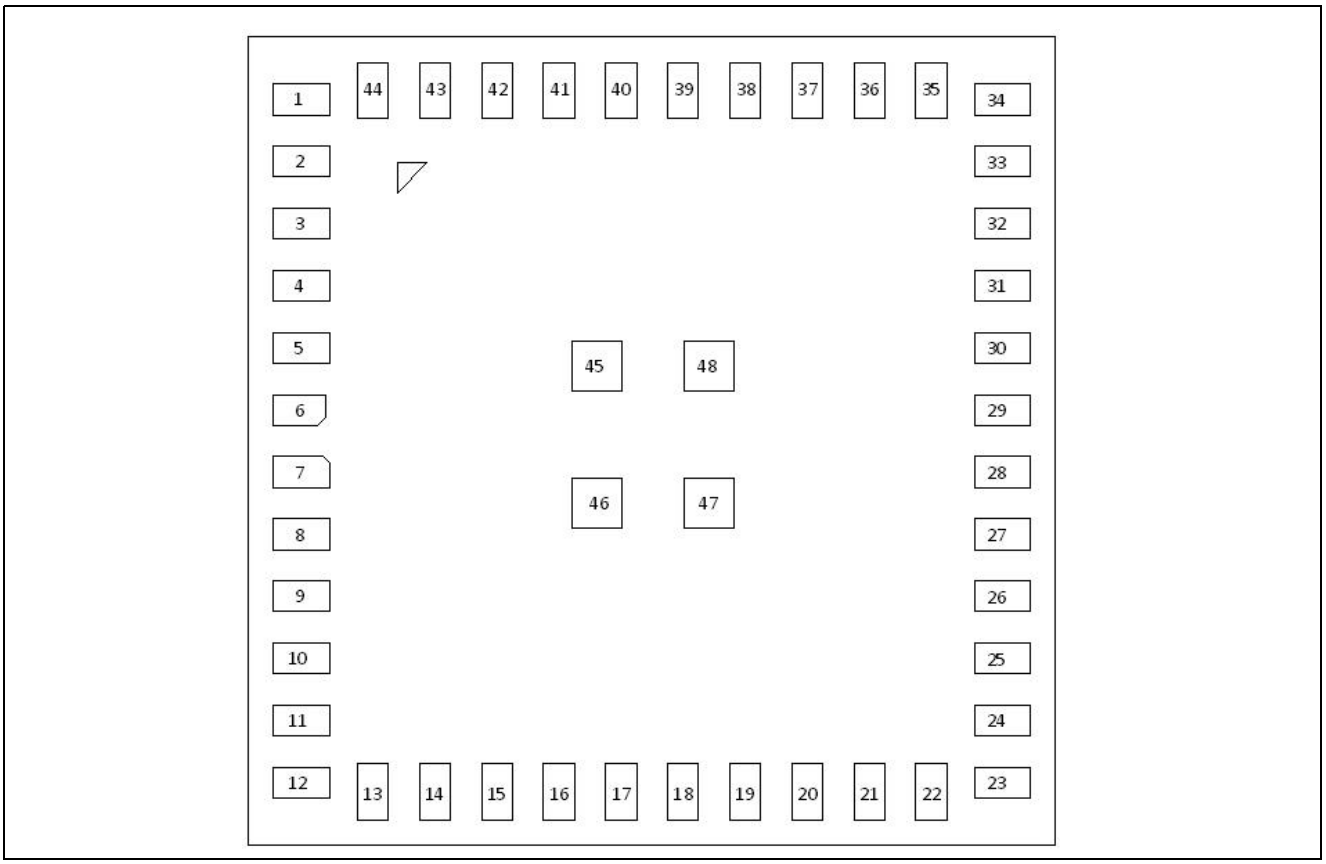
Table 1-1. 32 kHz Crystal Oscillator Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	F_{tol}	Crystal-dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	–	500	µs
Crystal drive level	P_{drv}	For crystal selection	0.5	–	–	µW
Crystal series resistance	R_{series}	For crystal selection	–	–	70	kΩ
Crystal shunt capacitance	C_{shunt}	For crystal selection	–	–	1.3	pF

1.2 Pin Map and Signal Descriptions

The CYW20732S pin map is shown in Figure 1-3.

Figure 1-3. CYW20732S (TOP View)



The signal name, type, and description of each pin in the CYW20732S is listed in Table 1-2. The symbols shown under I/O Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 1-2. Pin Descriptions

Pin	Name	I/O Type	Description
1	GPIO: P27 PWM1	I	Default direction: Input. After POR state: Input floating. Drain current: 16 mA Alternate function: MOSI (master and slave) for SPI_2
2	GND	GND	GND
3	VBAT	I	Battery supply input.
4	GND	GND	GND
5	GND	GND	GND
6	GND	GND	GND
7	GND	GND	GND
8	GND	GND	GND

Table 1-2. Pin Descriptions *(continued)*

Pin	Name	I/O Type	Description
9	GND	GND	GND
10	Reserved	–	Leave floating
11	GND	GND	GND
12	GND	GND	GND
13	GND	GND	GND
14	GND	GND	GND
15	GND	GND	GND
16	GND	GND	GND
17	GND	GND	GND
18	UART_RX	I	UART_RX. This pin is pulled low through an internal 10 kΩ resistor.
19	UART_TX	O, PU	UART_TX
20	GND	GND	GND
21	SCL	I/O, PU	SCL I/O, PU clock signal for an external I^2C device
22	SDA	I/O, PU	SDA I/O, PU data signal for an external I^2C device
23	GND	GND	GND
24	GND	GND	GND
25	GPIO: P1	I	Default direction: Input. After POR state: Input floating. This pin is tied to the WP pin of the embedded EEPROM. Requires an external 10K pull-up
26	TMC	I	Test mode control. Pull this pin high to invoke test mode; leave it floating if not used. This pin is connected to GND through an internal 10 kΩ resistor.
27	RESET_N	I/O PU	Active-low system reset with open-drain output
28	GPIO: P0	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ Peripheral UART TX (PUART_TX) ■ MOSI (master and slave) for SPI_2 ■ IR_RX ■ 60Hz_main
29	GND	GND	GND
30	GPIO: P3	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ Peripheral UART CTS (PUART_CTS) ■ SPI_CLK (master and slave) for SPI_2
31	GPIO: P2	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ Peripheral UART RX (PUART_RX) ■ SPI_CS (slave only) for SPI_2 ■ SPI_MOSI (master only) for SPI_2

Table 1-2. Pin Descriptions *(continued)*

Pin	Name	I/O Type	Description
32	GPIO: P4	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ Peripheral UART RX (PUART_RX) ■ MOSI (master and slave) for SPI_2. ■ IR_TX
33	GPIO: P8	I	Default direction: Input. After POR state: Input floating. Alternate functions: A/D converter input
34	GPIO: P33	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ MOSI (slave only) for SPI_2 ■ Auxiliary clock output (ACLK1) ■ Peripheral UART RX (PUART_RX)
35	GPIO: P32	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ SPI_CS (slave only) for SPI_2. ■ Auxiliary clock output (ACLK0) ■ Peripheral UART TX (PUART_TX)
36	GPIO: P25	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ MISO (master and slave) for SPI_2 ■ Peripheral UART RX (PUART_RX)
37	GPIO: P24	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ SPI_CLK (master and slave) for SPI_2 ■ Peripheral UART TX (PUART_TX)
38	N/C	N/C	N/C
39	GPIO: P13 PWM3	I	Default Direction: Input After POR State: Input Floating Drain current: 16 mA Alternate function: A/D converter input
	GPIO: P28 PWM2	I	Default direction: Input. After POR state: Input floating. Drain current: 16 mA Alternate functions: ■ A/D converter input ■ LED1 ■ IR_TX
40	GPIO: P14 PWM2	I	Default direction: Input. After POR state: Input floating. Alternate function: A/D converter input
	GPIO: P38	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ MOSI (master and slave) for SPI_2 ■ IR_TX

Table 1-2. Pin Descriptions *(continued)*

Pin	Name	I/O Type	Description
41	GPIO: P15	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ IR_RX ■ 60 Hz_main
42	GPIO: P26 PWM0	I	Default direction: Input. After POR state: Input floating. Drain current: 16 mA Alternate function: SPI_CS (slave only) for SPI_2
43[a]	GPIO: P12	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ XTALO32K
	XTALO32K	O	Low-power oscillator (LPO) output. Alternate functions: P12 P26
44[b]	GPIO: P11	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ XTALI32K
	XTALI32K	I	Low-power oscillator (LPO) input. Alternate functions: ■ P11 ■ P27
45	GND	GND	GND
46	GND	GND	GND
47	GND	GND	GND
48	GND	GND	GND

a. When pin 43 (XTALO32K) is used, ADC/GPIO:P12 is unavailable. P26 may still be available.
b. When pin 44 (XTALI32K) is used, ADC/GPIO:P11 is unavailable. P27 may still be available.

1.3 Electrical Specifications

Absolute maximum ratings are defined in Table 1-3.

Table 1-3. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply power	NA	3.63	V
Storage temperature	–40	125	°C
Voltage ripple	0	±2	%
Power supply (VBAT absolute maximum rating)	1.62	3.63	V

Power for the CYW20732S module is provided by the host through the power pins.

Table 1-4. Voltage

Symbol	Parameter	Min.	Typ.	Max.	Unit
VBAT	Battery voltage	1.62	–	3.63	V

Table 1-5. Current Consumption

Operating Mode	Condition	Nominal	Maximum	Unit
Receive	Receiver and baseband are both operating, 100%	24.0	28.0	mA
Transmit	Transmitter and baseband are both operating, 100%	24.0	28.0	mA
Sleep	Wake in < 5 ms	55.0	60.0	µA
Deep Sleep	Wake on interrupt	2.0	2.5	µA
Note: All measurements taken at 25°C				

Based on the current measurements in Table 1-5 , CYW20732S peak power values are:

- RX: 101.6 mW
- TX: 101.6 mW
- Sleep mode: 217.8 µW
- Deep Sleep mode: 9.1 µW

1.4 RF Specifications

CYW20732S receiver specifications are defined in Table 1-6.

Table 1-6. Receiver Specifications

Parameter	Mode and Conditions	Min.	Typ.	Max.	Unit
Frequency range	–	2402	–	2480	MHz
RX sensitivity (standard)	Packets: 200 Payload: PRBS 9 Length: 37 Bytes Dirty Transmitter: off. PER: 30.8%	–	–94	–	dBm
Maximum input	–	–10	–	–	dBm
Note: All measurements taken at 3.0V (default voltage)					

RF transmitter specifications are defined in Table 1-7.

Table 1-7. Transmitter Specifications

Parameter	Min.	Typ.	Max.	Unit
Transmitter				
Frequency range[a]	2402	–	2480	MHz
Output power adjustment range	–20	–	4	dBm
Output power	–	2	–	dBm
Output power variation	–	2.5	–	dB
LO Performance				
Initial carrier frequency tolerance	–	–	±150	kHz
Frequency Drift				
Frequency drift	–	–	±50	kHz
Drift rate	–	–	20	kHz/50 µs
Frequency Deviation				
Average deviation in payload (sequence: 00001111)	225	–	275	kHz
Average deviation in payload (sequence: 10101010)	185	–	–	kHz
Channel spacing	–	2	–	MHz

a. This parameter is taken from the Bluetooth 4.0 specification.

1.5 ADC Specifications

CYW20732S ADC specifications are defined in Table 1-8.

Table 1-8. ADC Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Number of input channels	–	–	–	9	–	-
Channel switching rate	f_{ch}	–	–	–	133.33	Kch/s
Input signal range	V_{inp}	–	0	–	3.63	V
Reference settling time	–	Charging refsel	7.5	–	–	µs
Input resistance	R_{inp}	Effective, single-ended	–	500	–	kΩ
Input capacitance	C_{inp}	–	–	–	5	pF
Conversion rate	F_c	–	5.859	–	187	kHz
Conversion time	T_c	–	5.35	–	170.7	µs
Resolution	R	–		16		Bits
Absolute voltage measurement error	–	Using on–chip ADC firmware driver	–	±2	–	%
Current	I	$I_{avdd1p2} + I_{avdd3p3}$	–	–	1	mA
Power	P	–	–	1.5	–	mW
Leakage Current	$I_{leakage}$	T = 25°C	–	–	100	nA
Power-up time	$T_{powerup}$	–	–	–	200	µs
Integral nonlinearity	I_{NL}	In the guaranteed performance range	–1	–	1	LSB[a]
Differential nonlinearity	D_{NL}	In the guaranteed performance range	–1	–	1	LSB<Superscript>a

a. LSBs are expressed at the 10-bit level.

1.6 Timing and AC Characteristics

1.6.1 SPI Timing

SPI interface timing is illustrated in Figure 1-4 and Figure 1-5 and are defined in Table 1-9 .

Figure 1-4. SPI Timing—Modes 0 and 2

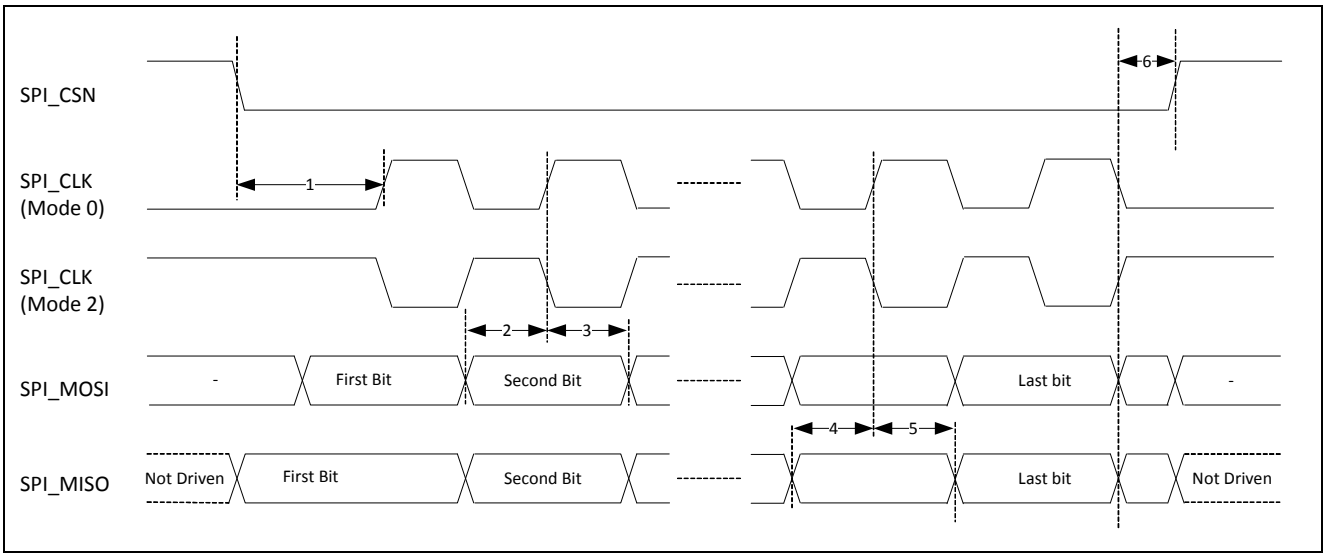


Figure 1-5. SPI Timing—Modes 1 and 3

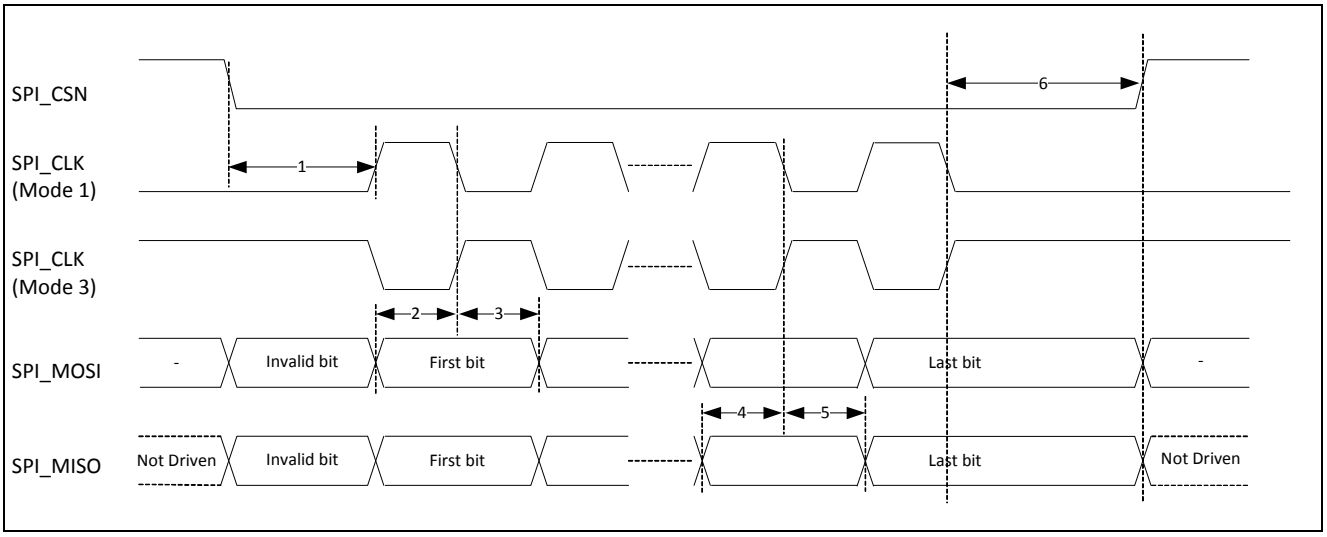


Table 1-9. SPI Interface Timing Specifications

Reference	Characteristics	Min.	Typ.	Max.
1	Time from CSN asserted to first clock edge	1 SCK	100	∞
2	Master setup time	–	1/2SCK	–
3	Master hold time	1/2SCK	-	–
4	Slave setup time	–	1/2 SCK	–
5	Slave hold time	1/2 SCK	–	–
6	Time from last clock edge to CSN deasserted	SCK	10 SCK	100

1.6.2 BSC Interface Timing

BSC interface timing is illustrated in Figure 1-6 and is defined in Table 1-10.

Figure 1-6. BSC Interface Timing

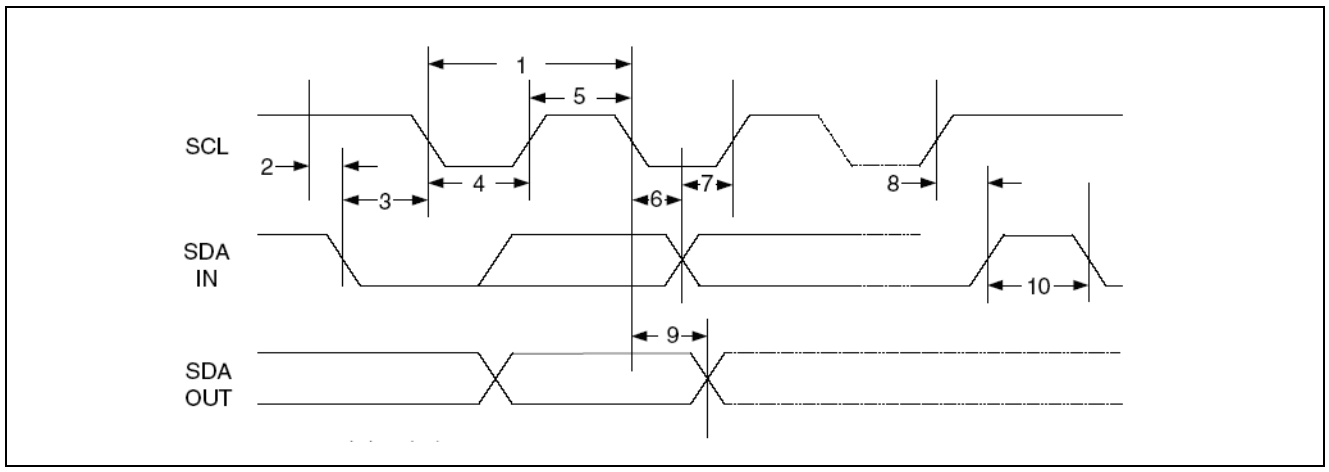


Table 1-10. BSC Interface Timing Specifications

Reference	Characteristics	Min.	Max.	Unit
1	Clock frequency	–	100, 400, 800, 1000	kHz
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time	650	–	ns

1.6.3 UART Timing

UART timing is illustrated in Figure 1-7 and defined in Table 1-11.

Figure 1-7. UART Timing

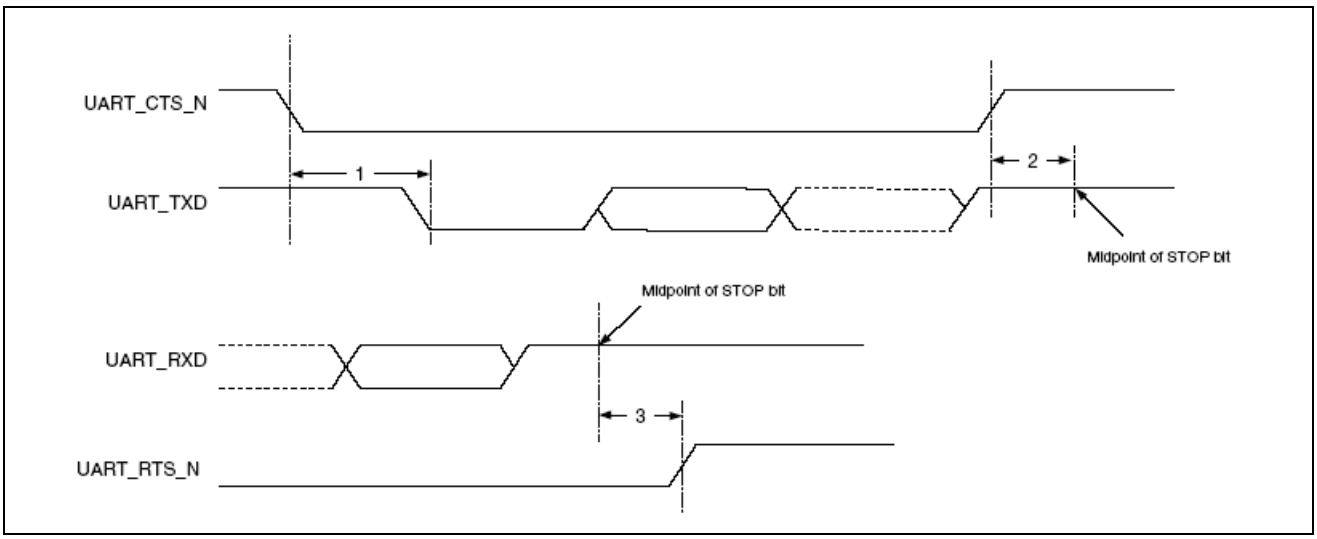


Table 1-11. UART Timing Specifications

Reference	Characteristics	Min.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baudout cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baudout cycles

1.7 PCB Design and Manufacturing Recommendations

1.7.1 Pad and Solder Mask Opening Dimensions

CYW20732S pad and solder mask opening dimensions are defined in Table 1-12.

Table 1-12. Pad and Solder Mask Dimensions

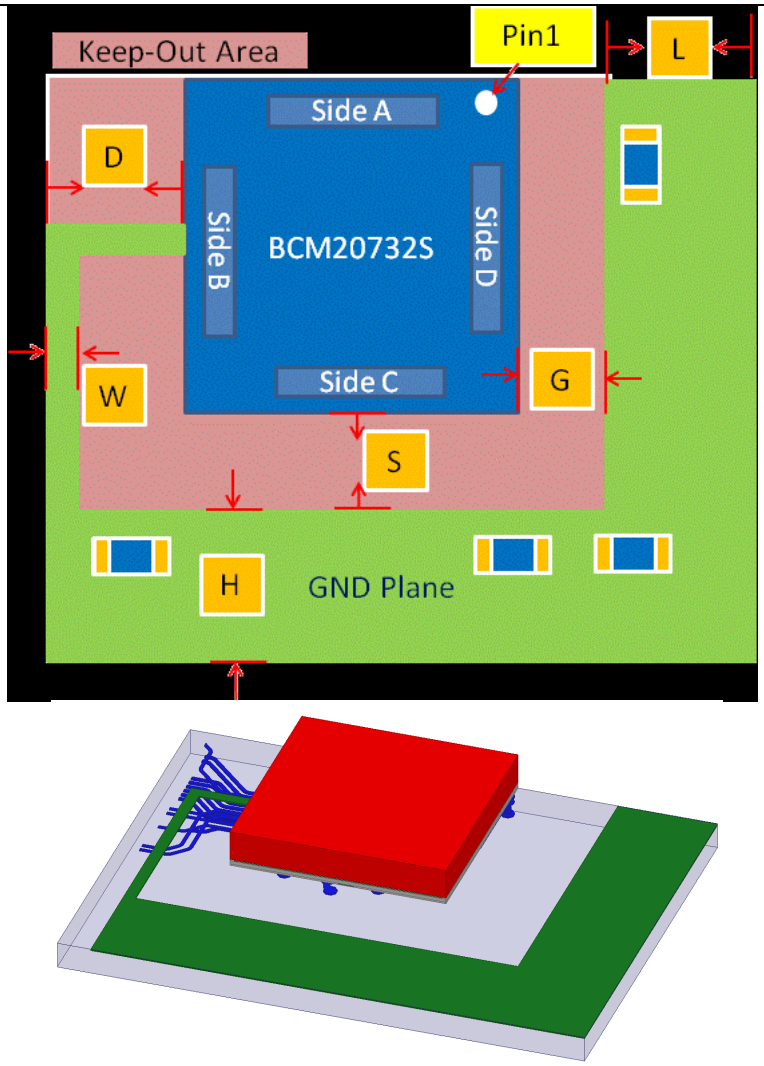
Pad Type	Pad Dimensions	Solder Mask Opening Dimensions	Unit
Type A	0.6 × 0.25	0.7 × 0.35	mm
Type B	0.55 × 0.3	0.65 × 0.4	
Type C	0.4 × 0.4	0.5 × 0.5	

1.7.2 PCB Layout Recommendations for Configuration A

The following layout recommendations are referenced to Figure 1-8:

- Connect to system ground from side B of the module (pins 13–22).
- An L-shaped ground plane is required for the embedded BLE antenna. Keep the GND continuous. Do not cut off the GND shape to accommodate trace routes.
- If the L-shaped GND plane is located on the top layer of the PCB, do not place components on the ground plane. If this cannot be avoided, move the L-shaped ground plane to another layer.
- Antenna efficiency of 31–41% can be achieved based on the layout in Figure 1-8 and the dimensions listed below. Following these layout recommendations is expected to yield 50+ meters of usable range; deviating from these recommendations may reduce the range of the antenna.
  - D: 4.5 mm (typical)
  - G, H, S: 3 mm (typical)
  - L: 3 mm (minimum)
  - W: 0.4 mm (typical)
- Route signal traces out of the module from side C (between pins 27 and 30) or side B (between pins 16 and 19) of the module. Traces can be overlapped to avoid routing through the keep-out area.
- Do not route traces from side A or sideD.

Figure 1-8. PCB Layout Example, Configuration A



Notes:

- Side A indicates the side of Pin #1 - Pin #12 of the CYW20732S.
- Side B indicates the side of Pin #13 - Pin #22 of the CYW20732S.
- Side C indicates the side of Pin #23 - Pin #34 of the CYW20732S.
- Side D indicates the side of Pin #35 - Pin #44 of the CYW20732S.

1.7.2.1 Example of an L-Shaped Ground Plane

Figure 1-9 shows an L-shaped ground arrangement in the 2nd layer (purple color) and the top-side component placement and trace routing (blue color). We can see that some components and routings are placing in the L-shaped area on the top layer and the “L -shaped” ground is connected to system ground in the 2nd layer.

Figure 1-9 also indicates the clearance area (marked in yellow) and L-shaped GND area (marked in green).

Figure 1-9. L-Shaped Ground Plane

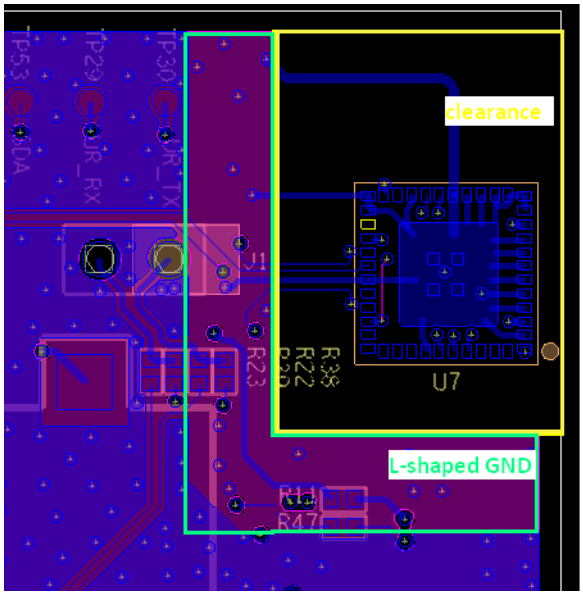
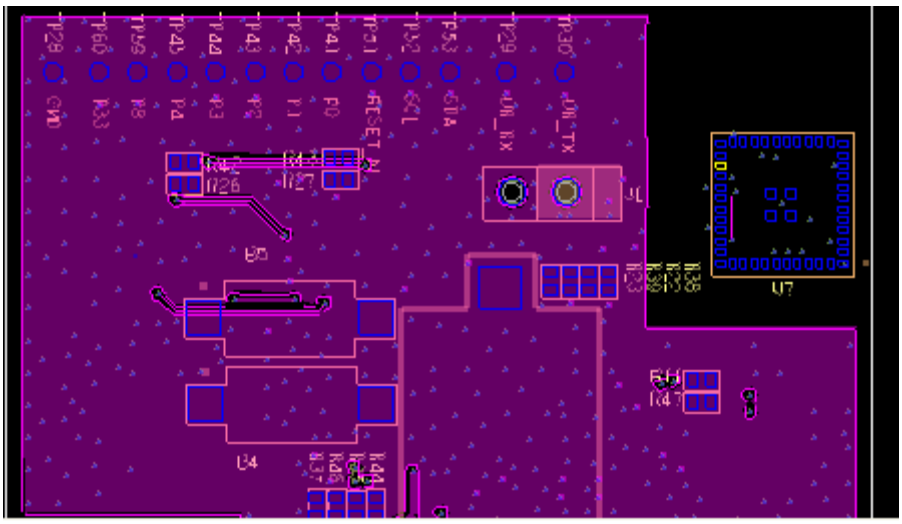


Figure 1-10 shows an L -shaped ground (arranged in the 2nd layer) only.

Figure 1-10. L-Shaped Ground Plane, 2nd Layer

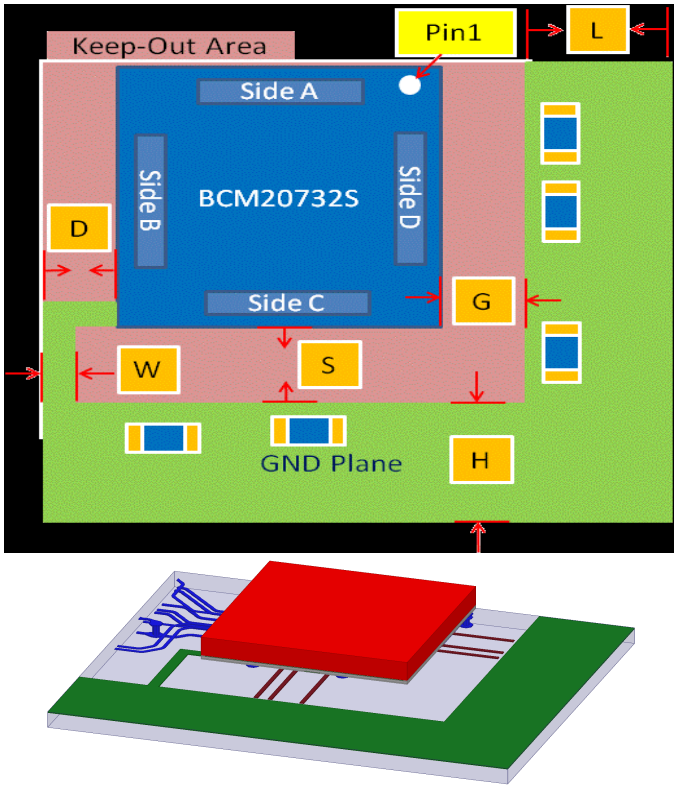


1.7.3 PCB Layout Recommendations for Configuration B

The following layout recommendations are referenced to Figure 1-11:

- Connect to system ground from side B of the module (pins 13–22).
- An L-shaped ground plane is required for the embedded BLE antenna. Keep the GND continuous. Do not cut off the GND shape to accommodate trace routes.
- If the L-shaped GND plane is located on the top layer of the PCB, do not place components on the ground plane. If this cannot be avoided, move the L-shaped ground plane to another layer.
- Antenna efficiency of 31–41% can be achieved based on the layout in Figure 1-11 and the dimensions listed below. Following these layout recommendations is expected to yield 50+ meters of usable range; deviating from these recommendations may reduce the range of the antenna.
  - D: 4.5 mm (typical)
  - G, H, S: 3 mm (typical)
  - L: 3 mm (minimum)
  - W: 0.4 mm (typical)
- Route signal traces out of the module from side C (between pins 27 and 30) or side B (between pins 16 and 19) of the module. Traces can be overlapped to avoid routing through the keep-out area.
- Do not route traces from side A or sideD.

Figure 1-11. PCB Layout Example, Configuration B



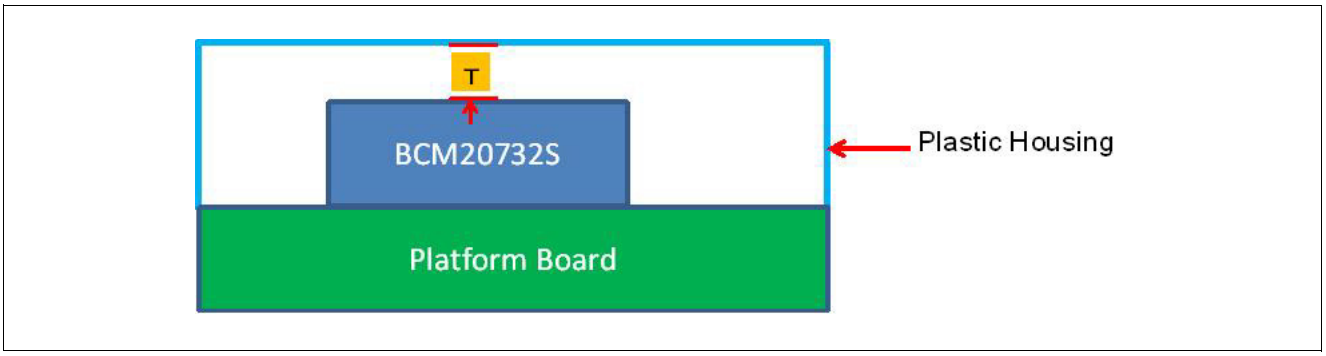
Notes:

- Side A indicates the side of Pin #1 - Pin #12 of the CYW20732S.
- Side B indicates the side of Pin #13 - Pin #22 of the CYW20732S.
- Side C indicates the side of Pin #23 - Pin #34 of the CYW20732S.
- Side D indicates the side of Pin #35 - Pin #44 of the CYW20732S.

1.7.4 Common Guidelines for CYW20732S

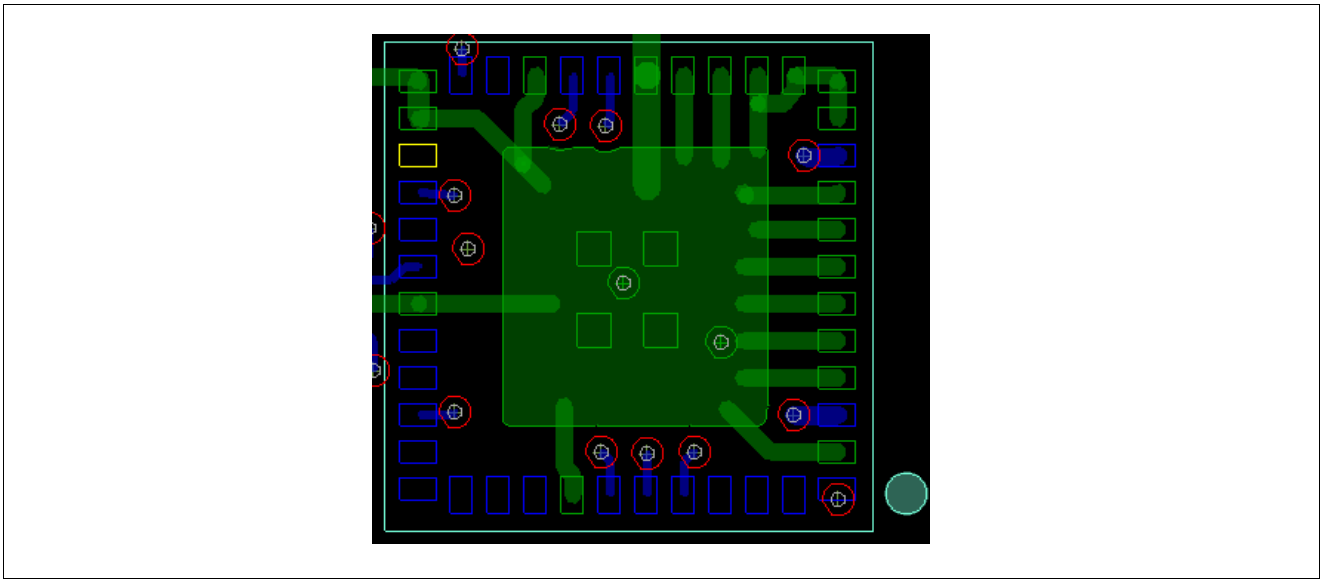
It is recommended to have a 0.4 mm gap between the chip's upper surface and the plastic housing (Figure 1-12).

Figure 1-12. Gap Between Chip’s Upper Surface and Plastic Housing



Arrange the GND plane under the module and connect the GND pins of the module to the GND plane as shown in Figure 1-14.

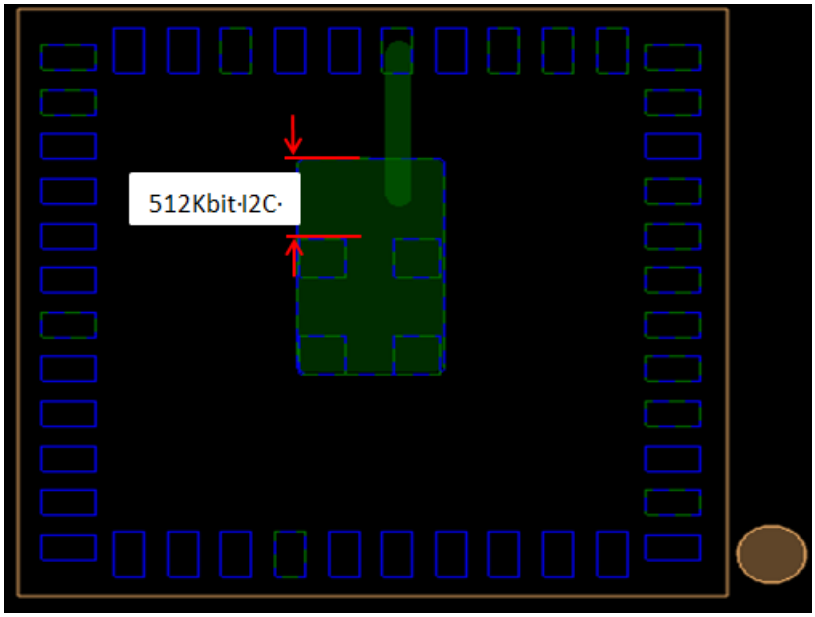
Figure 1-13. Example of Ground Plane Under the Module



Note: Do not route the GND plane under the RF pin.

If you are unable to reserve such a large GND plane, then use the minimal required area as shown in Figure 1-14.

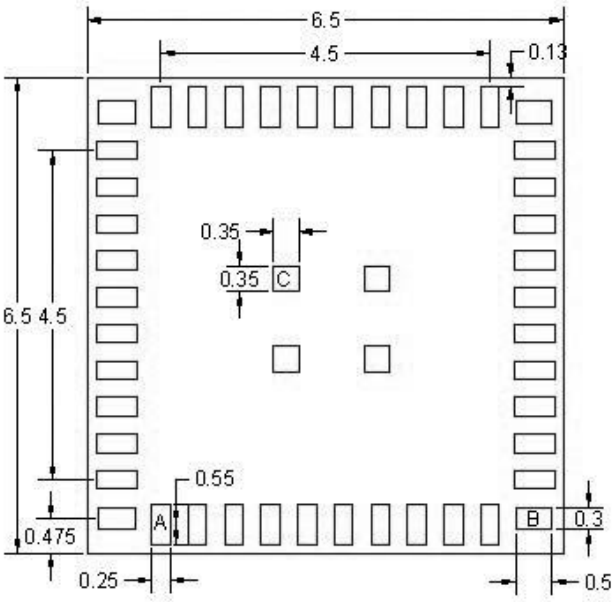
Figure 1-14. Minimum Required Ground Plane



1.7.5 PCB Stencil

The recommended PCB stencil is shown in Figure 1-15 (all measurements in mm). Use an unsolder mask to set the module footprint.

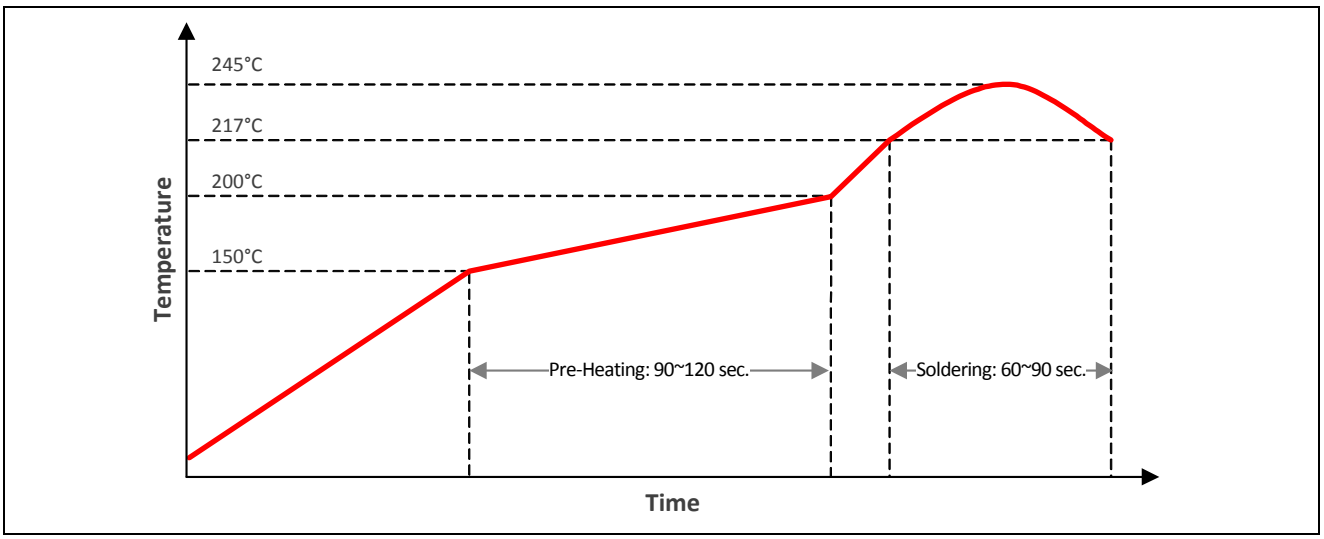
Figure 1-15. CYW20732S Stencil (Bottom View)



1.7.6 Solder Reflow

The recommended solder reflow profile for the CYW20732S is defined in Figure 1-16.

Figure 1-16. Solder Reflow Profile



1.8 Packaging and Storage Information

The CYW20732S is available in a tape and reel package and is shipped in an ESD-protected moisture-resistant (MSL-3) bag as shown in Figure 1-17. The storage temperature range is –40°C to +125°C.

Figure 1-17. CYW20732S ESD/Moisture Packaging

The moisture sensitivity label on the CYW20732S shipping bag is shown in Figure 1-18.

Figure 1-18. CYW20732S Moisture Sensitivity Label

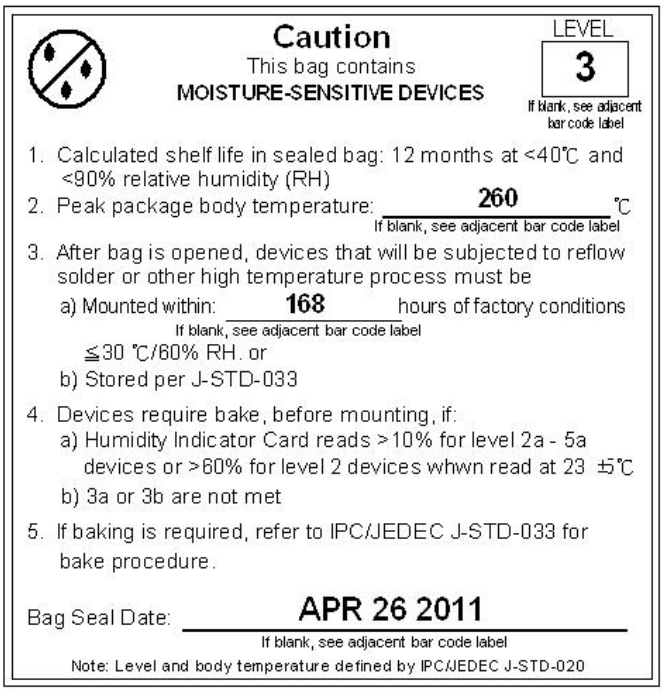
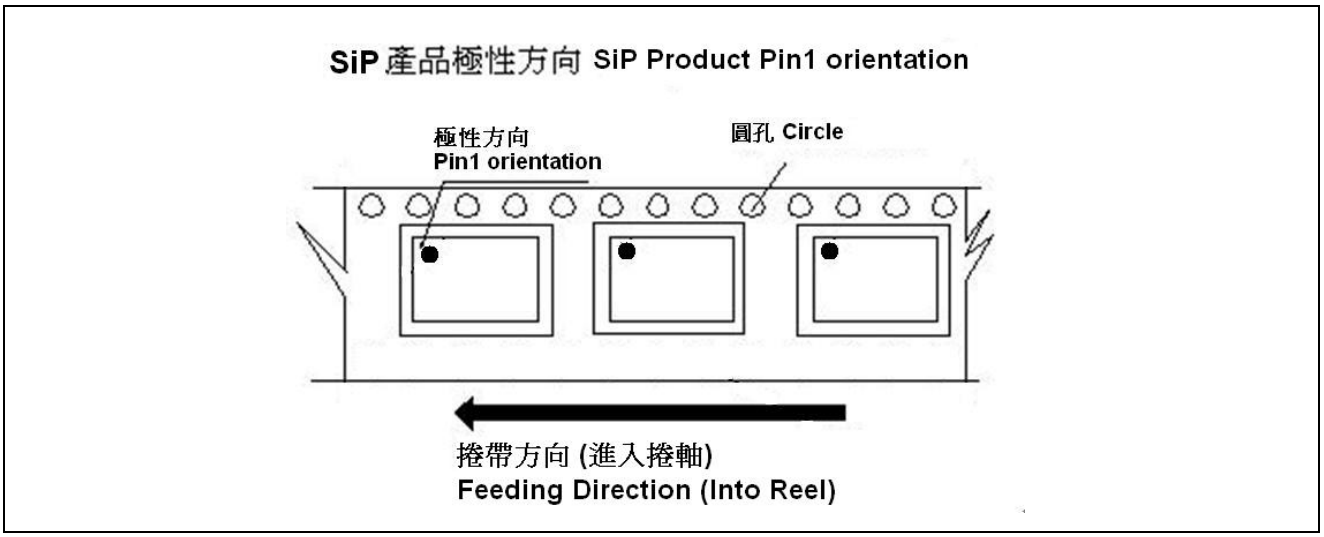


Figure 1-19 shows the location of pin 1 on the CYW20732S relative to its orientation on the tape packaging.

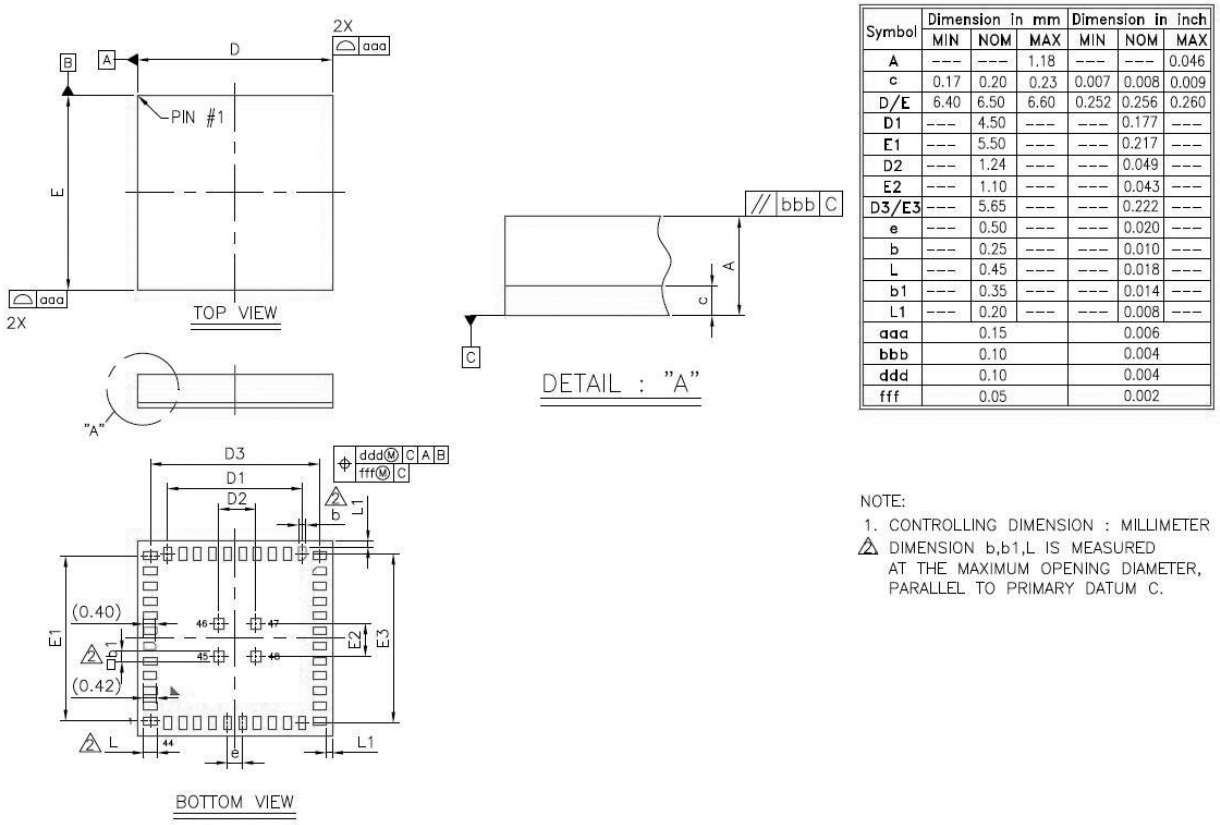
Figure 1-19. CYW20732S Tape and Reel Pin 1 Location



1.9 Mechanical Information

Package dimensions for the CYW20732S are shown in Figure 1-20.

Figure 1-20. CYW20732S Package Dimensions

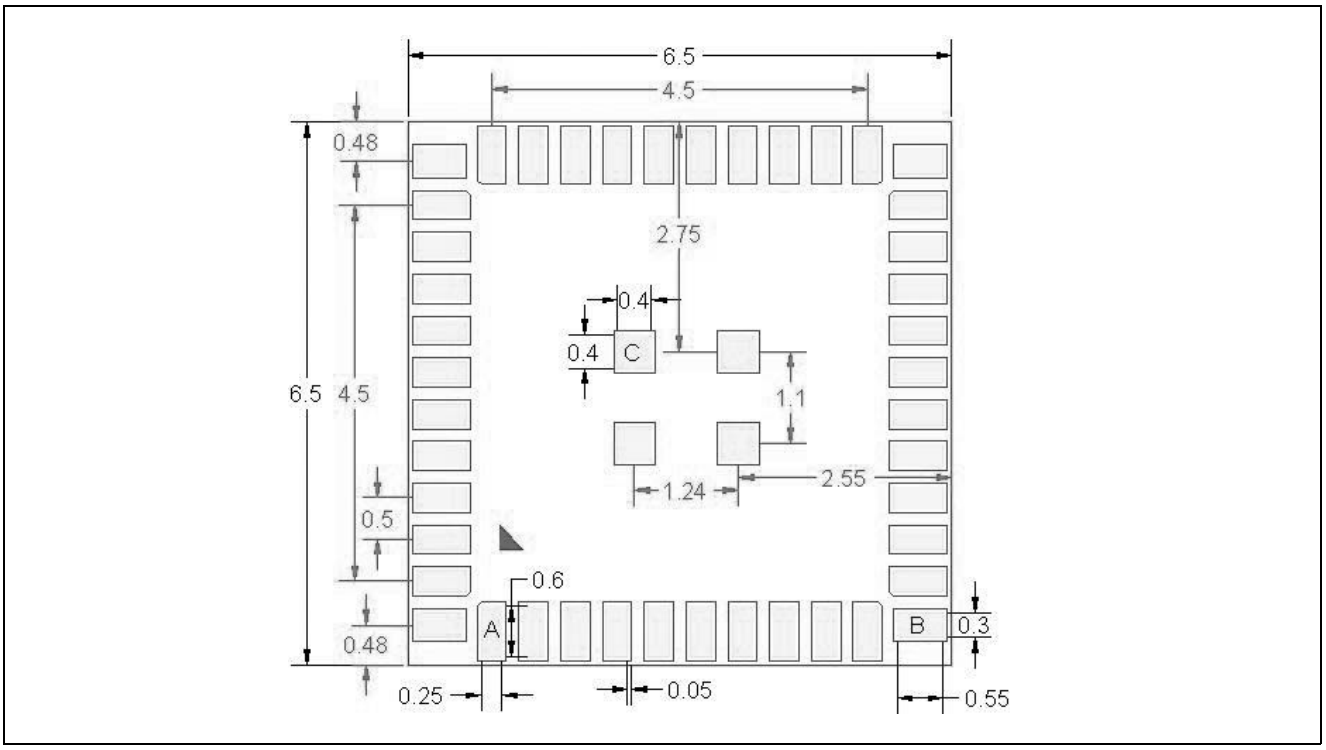


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.18	---	---	0.046
c	0.17	0.20	0.23	0.007	0.008	0.009
D/E	6.40	6.50	6.60	0.252	0.256	0.260
D1	---	4.50	---	---	0.177	---
E1	---	5.50	---	---	0.217	---
D2	---	1.24	---	---	0.049	---
E2	---	1.10	---	---	0.043	---
D3/E3	---	5.65	---	---	0.222	---
e	---	0.50	---	---	0.020	---
b	---	0.25	---	---	0.010	---
L	---	0.45	---	---	0.018	---
b1	---	0.35	---	---	0.014	---
L1	---	0.20	---	---	0.008	---
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
fff		0.05			0.002	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. DIMENSION b,b1,L IS MEASURED AT THE MAXIMUM OPENING DIAMETER, PARALLEL TO PRIMARY DATUM C.

Additional CYW20732Spackage dimensions are shown in Figure 1-21.

Figure 1-21. CYW20732S Pin Dimensions (Bottom View)



1.10 Ordering Information

Table 1-13. Ordering Information

Part Number	Package	Operating Temperature	Humidity
CYW20732S	48-pin LGA	–40°C to +85°C	95% max., noncondensing

Regulatory Information

FCC

FCC NOTICE:

The device complies with part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions,ê may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP-0737

In any case the end product must be labeled exterior with "Contains FCC ID: WAP-0737".

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antennas listed below. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas in Table 5 on page 10, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of the device with the PCB antenna (FCC ID: WAP-0737) is far below the FCC radio frequency exposure limits. Nevertheless, use the device such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

ISED Certification

The device is licensed to meet the regulatory requirements of Industry Canada (IC),

License: IC: 7922A-0737

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in Table 5 on page 10, having a maximum gain of -1.5dBi, antennas not included in this list or having a gain greater than -1.5dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

IC NOTICE:

The device including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

IC RADIATION EXPOSURE STATEMENT FOR CANADA

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device. (3) No SAR evaluation is required since maximum transmitter Pout is below IC threshold

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.
(3) Aucune évaluation SAR n'est requise étant donné que la puissance maximale de l'émetteur est inférieure au seuil IC.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that IC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the IC Notice above. The IC identifier is 7922A-0737 . In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-0737 ".

European R&TTE Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module complies with the essential requirements and other relevant provisions of Directive 1999/5/EC. As a result of the conformity assessment procedure described in Annex III of the Directive 1999/5/EC, the end-customer equipment should be labeled as follows:

CE

All versions of the device in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

Revision History

Document Revision History

Document Title: CYW20732S Bluetooth Low Energy SiP Module Document Number: 002-15222				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	-	10/02/2013	-	MMP20732S-TRM100-R: Initial Release
*A	-	01/15/2014	-	MMP20732S-TRM101-R Update document template
*B	-	03/04/2014	-	MMP20732S-TRM102-R **Updated:** ■ Table 2: “Pin Descriptions”. ■ “Technical Support” (added link to the WICED support community). ■ Section: Electrical Specifications, Table 4: “Voltage”
*C	-	05/13/2014	-	MMP20732S-TRM103-R **Added:** ■ Footnotes for pins 43 and 44 of Table 2: “Pin Descriptions” ■ “PCB Layout Recommendations for Configuration A” ■ “PCB Layout Recommendations for Configuration B” ■ “Common Guidelines for CYW20732S”
*D	-	08/22/2014	-	MMP20732S-TRM104-R **Updated:** Table 2: “Pin Descriptions,” (pins 33 and 38).
*E	-	09/11/2014	-	MMP20732S-TRM105-R **Updated:** ■ Table 2: “Pin Descriptions”, pin 37 alternate functions. ■ “PCB Layout Recommendations for Configuration A”. ■ “PCB Layout Recommendations for Configuration B”. **Removed:** Appendix A: “Acronyms and Abbreviations”.
*F	-	03/24/2016	-	MMP20732S-TRM106-R **Updated:** Table 5, “Current Consumption”
*G	5560143	01/27/2017	UTSV	Updated to Cypress Template.