PRELIMINARY

CYBT-353027-02

EZ-BT™ WICED Module

General Description

The CYBT-353027-02 is a fully integrated Bluetooth® Smart Ready wireless module. The CYBT-353027-02 includes an onboard crystal oscillator, passive components, flash memory, and the Cypress CYW2070x silicon device.

The CYBT-353027-02 supports peripheral functions (ADC, timers), UART, I2C, and SPI communication, and a Bluetooth audio interface. The CYBT-353027-02 includes a royalty-free BLE stack compatible with Bluetooth 5.0 in a 9.0 × 9.0 × 1.75 mm SMT package.

The CYBT-353027-02 includes 512 KB of onboard serial flash memory and is designed for standalone operation. The CYBT-353027-02 uses an integrated power amplifier to achieve Class I or Class II output power capability.

The CYBT-353027-02 is fully qualified by Bluetooth SIG and is targeted at space constrained applications.

Module Description

- Module size: 9.00 mm × 9.00 mm × 1.75 mm
- Bluetooth 5.0 Qualified Smart Ready module
  - QDID: TBD
  - Declaration ID: TBD
- Certified to FCC, ISED, MIC, and CE regulations
- Castelated solder pad connections for ease-of-use
- 512-KB on-module serial flash memory
- Up to 8 GPIOs
- Temperature range: -30 °C to +85 °C
- Cortex-M3 32-bit processor
- Maximum TX output power:
  - +12 dbm for Bluetooth Classic
  - +9 dBm for Bluetooth Low Energy
- RX Receive Sensitivity:
  - –93.5 dBm for Bluetooth Classic
  - –96.5 dBm for Bluetooth Low Energy

Power Consumption[1]

- TX average current consumption: 52.5 mA (EDR) at 8 dBm
- RX average current consumption: 26.4 mA (EDR)
- Low power mode support
  - Deep Sleep: 2.69 uA

Functional Capabilities

- Σ-Δ ADC for audio (12 bits) and DC measurement (10 bits)
- Serial Communications interface compatible with I^2C slaves
- Master Serial Peripheral Interface (SPI) support
- HCI interface through UART
- PCM/I2S Audio interface
- Two-wire Global Coexistence Interface (GCI)
- Programmable output power control
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Bluetooth wideband speech support

Benefits

CYBT-353027-02 provides all necessary components required to operate BLE and/or BR/EDR communication standards.

- Proven hardware design ready to use
- Dual-mode operation eliminates the need for multiple modules
- Cost optimized for applications without space constraints
- Nonvolatile memory for self-sufficient operation and Over-the-air updates
- Bluetooth SIG Listed with QDID and Declaration ID
- Fully certified module eliminates the time needed for design, development and certification processes
- WICED™ STUDIO provides an easy-to-use integrated design environment (IDE) to configure, develop, and program a Bluetooth application

Note

1. The values in this section were calculated for a 90% efficient DC-DC at 3V in HCI mode, and based on a Class I configuration bench-marked at Class II. Lower values are expected for a class II configuration using an external LPO and corresponding PA configuration.

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

References

- Overview: EZ-BLE/BT Module Portfolio, Module Roadmap
- Development Kits:
  - CYBT-353027-EVAL, CYBT-353027-02 Evaluation Board
- Test and Debug Tools:
  - CYSmart, Bluetooth® LE Test and Debug Tool (Windows)
  - CYSmart Mobile, Bluetooth® LE Test and Debug Tool (Android/iOS Mobile App)
- Knowledge Base Article
  - KBA97095 - EZ-BLE™ Module Placement
  - KBA213976 - FAQ for BLE and Regulatory Certifications with EZ-BLE modules
  - KBA210802 - Queries on BLE Qualification and Declaration Processes
  - KBA218122 - 3D Model Fils for EZ-BLE/EZ-BT Modules

Development Environments

Wireless Connectivity for Embedded Devices (WICED) Studio Software Development Kit (SDK)

Cypress' WICED® (Wireless Connectivity for Embedded Devices) is a full-featured platform with proven Software Development Kits (SDKs) and turnkey hardware solutions from partners to readily enable Wi-Fi and Bluetooth® connectivity in system design.

WICED Studio is the only SDK for the Internet of Things (ioT) that combines Wi-Fi and Bluetooth into a single integrated development environment. In addition to providing WICED APIs and an application framework designed to abstract complexity, WICED Studio also leverages many common industry standards.

Technical Support

- Cypress Community: Whether you're a customer, partner or a developer interested in the latest Cypress innovations, the Cypress Developer Community offers you a place to learn, share and engage with both Cypress experts and other embedded engineers around the world.
- Frequently Asked Questions (FAQs): Learn more about our Bluetooth ECO System.
- Visit our support page and create a technical support case or contact a local sales representatives. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

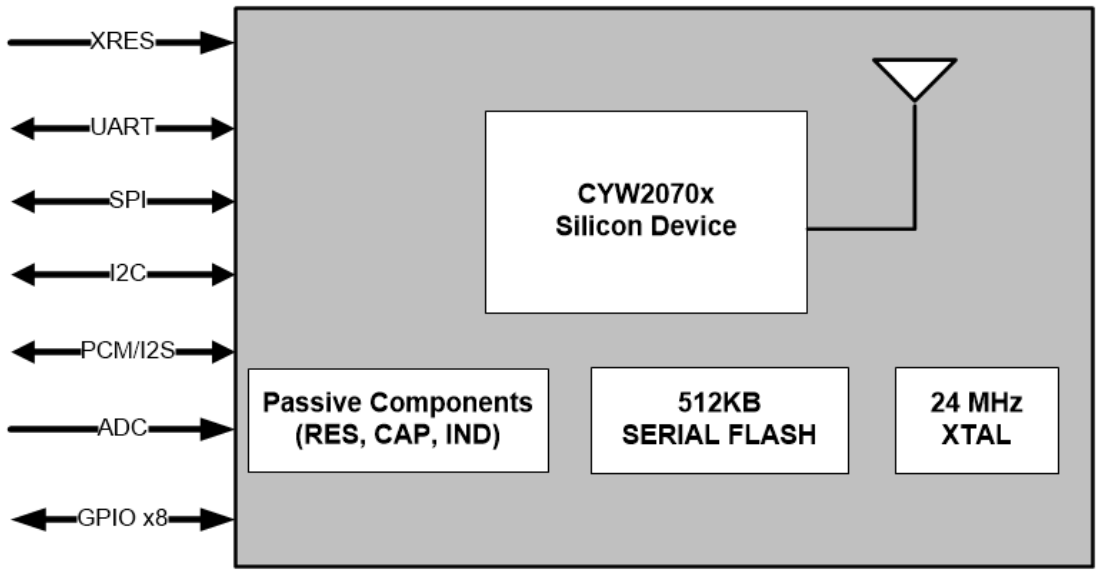
Contents

Overview

Functional Block Diagram

Figure 1 illustrates the CYBT-353027-02 functional block diagram.

Figure 1. Functional Block Diagram



Module Description

The CYBT-353027-02 module is a complete module designed to be soldered to the application's main board.

Module Dimensions and Drawing

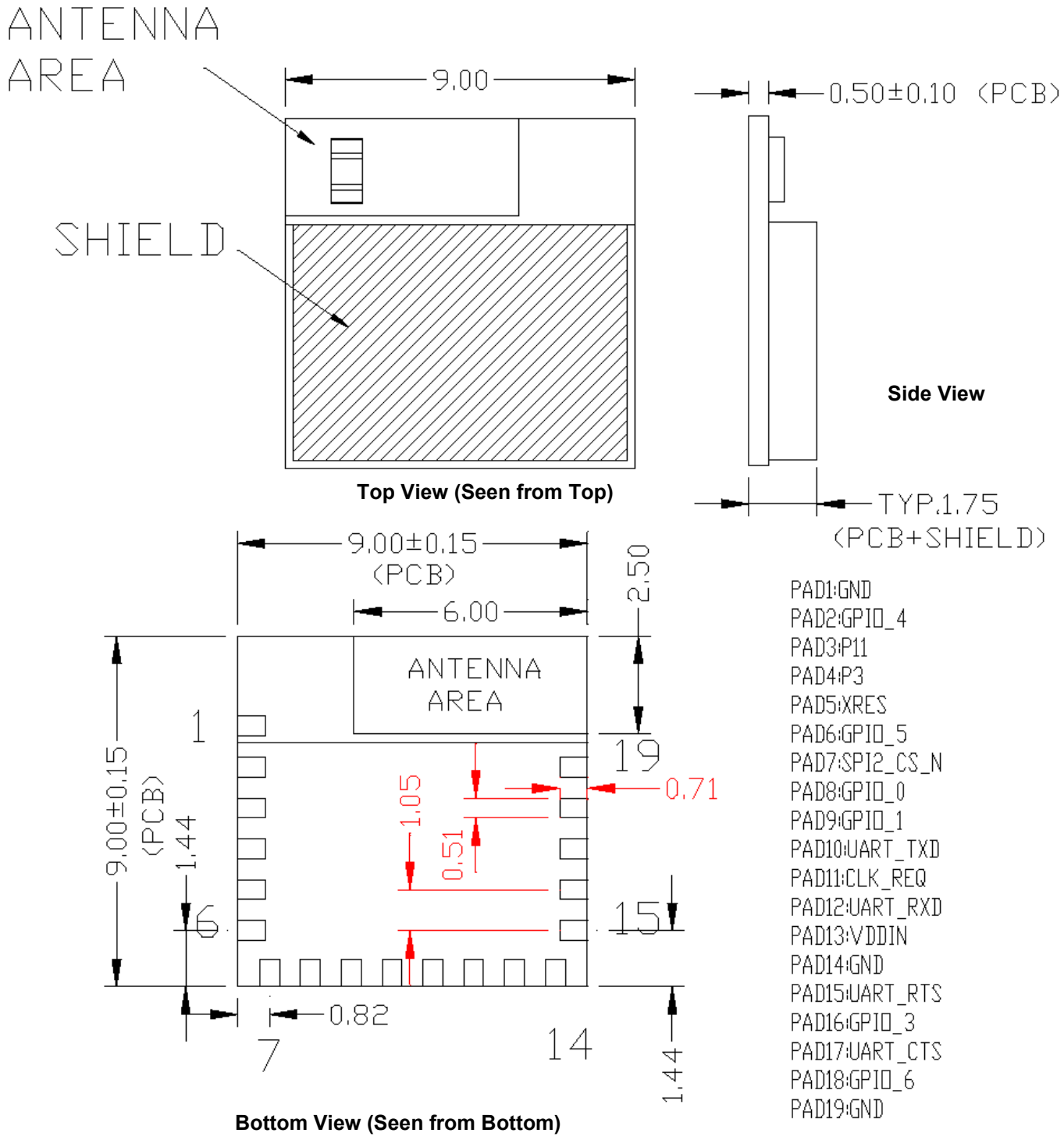
Cypress reserves the right to select components from various vendors to achieve the Bluetooth module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in Figure 2 on page 5. All dimensions are in millimeters (mm).

Table 1. Module Design Dimensions

Dimension Item		Specification
Module dimensions	Length (X)	9.00 ± 0.15 mm
	Width (Y)	9.00 ± 0.15 mm
Antenna area dimensions	Length (X)	6.00 mm
	Width (Y)	2.50 mm
PCB thickness	Height (H)	0.50 ± 0.10 mm
Shield height	Height (H)	1.25 mm typical
Maximum component height	Height (H)	1.25 mm typical
Total module thickness (bottom of module to highest component)	Height (H)	1.75 mm typical

See Figure 2 for the mechanical reference drawing for CYBT-353027-02.

Figure 2. Module Mechanical Drawing



Notes

2. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see "Recommended Host PCB Layout" on page 7.

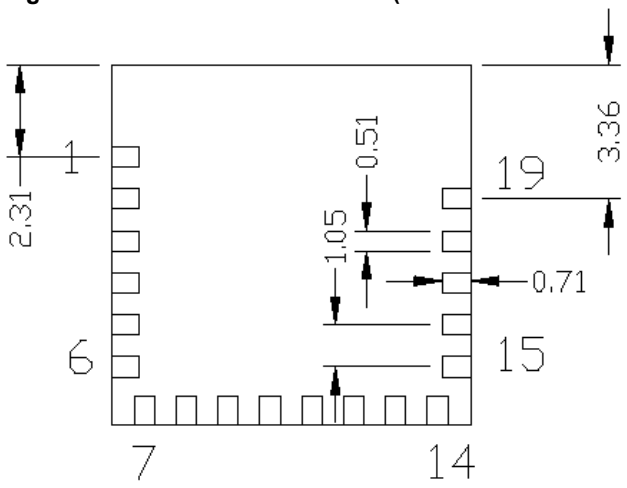
Pad Connection Interface

As shown in the bottom view of Figure 2 on page 5, the CYBT-353027-02 connects to the host board via solder pads on the backside of the module. Table 2 and Figure 3 detail the solder pad length, width, and pitch dimensions of the CYBT-353027-02 module.

Table 2. Connection Description

Name	Connections	Connection Type	Pad Length Dimension	Pad Width Dimension	Pad Pitch
SP	24	Solder Pads	0.71 mm	0.51 mm	1.05 mm

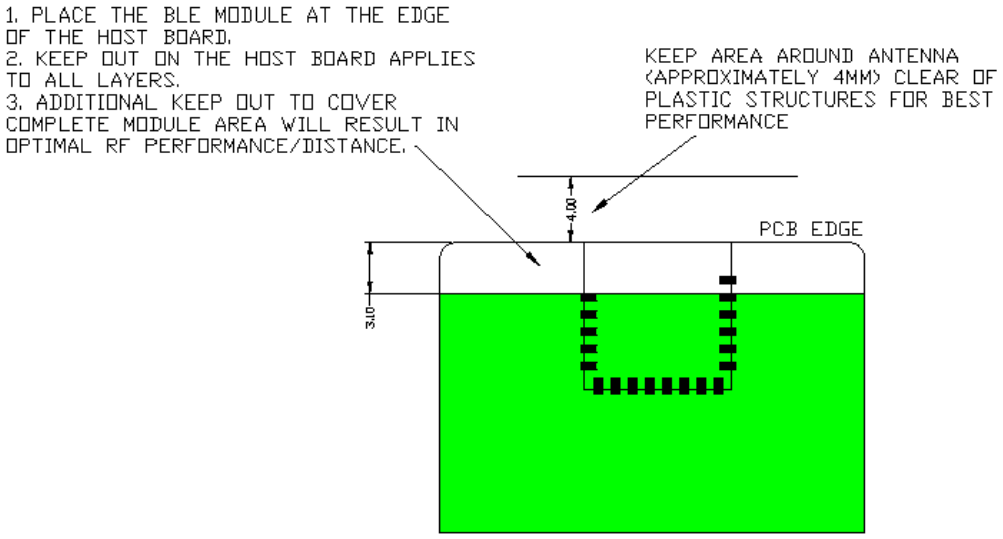
Figure 3. Solder Pad Dimensions (Seen from Bottom



To maximize RF performance, the host layout should follow these recommendations:

1. Antenna Area Keepout: The host board directly below the antenna area of the Cypress module (see Figure 2 on page 5) must contain no ground or signal traces. This keep out area requirement applies to all layers of the host board.
2. Module Placement: The ideal placement of the Cypress Bluetooth module is in a corner of the host board with the PCB trace antenna located at the far corner. This placement minimizes the additional recommended keep out area stated in item 2. Refer to AN96841 for module placement best practices.

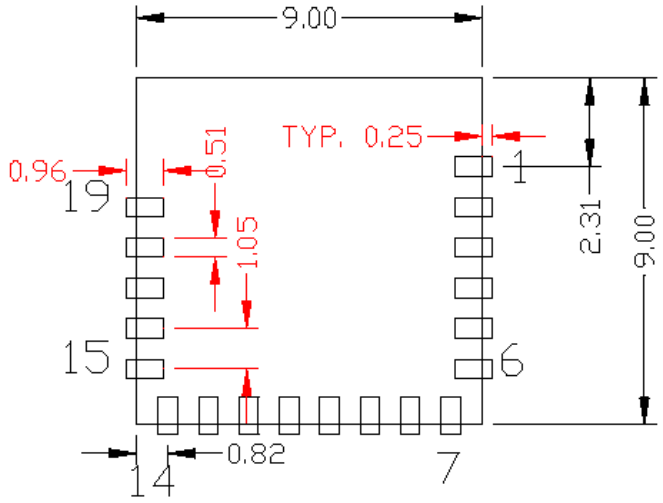
Figure 4. Recommended Host PCB Keep Out Area Around the CYBT-353027-02 Antenna



Recommended Host PCB Layout

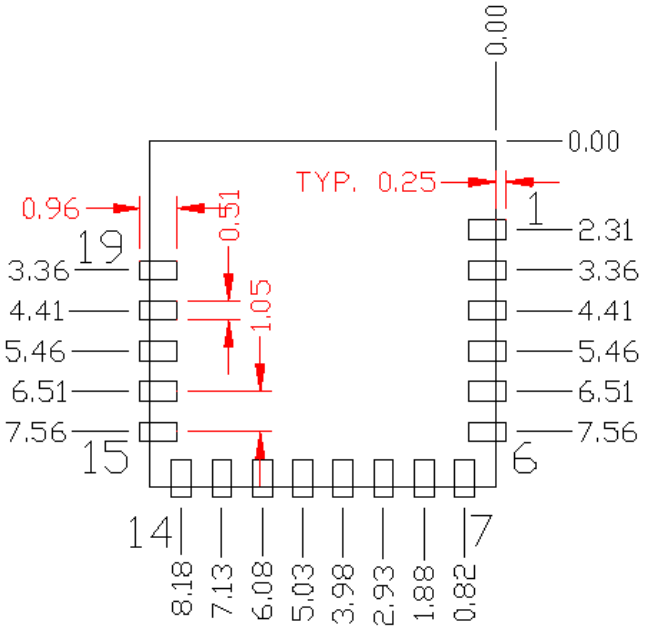
Figure 5, Figure 6, Figure 7, and Table 3 provide details that can be used for the recommended host PCB layout pattern for the CYBT-353027-02. Dimensions are in millimeters unless otherwise noted. Pad length of 0.96 mm (0.48 mm from center of the pad on either side) shown in Figure 7 is the minimum recommended host pad length. The host PCB layout pattern can be completed using either Figure 5, Figure 6, or Figure 7. It is not necessary to use all figures to complete the host PCB layout pattern.

Figure 5. CYBT-353027-02 Host Layout (Dimensioned)



Top View (Seen on Host PCB)

Figure 6. CYBT-353027-02 Host Layout (Relative to Origin)



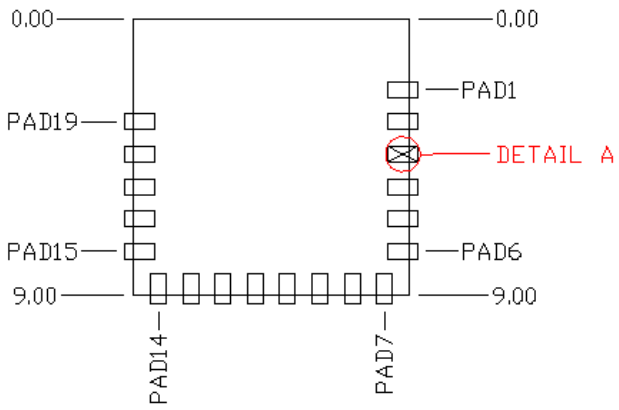
Top View (Seen on Host PCB)

Table 3 provides the center location for each solder pad on the CYBT-353027-02. All dimensions are referenced to the center of the solder pad. Refer to Figure 7 for the location of each module solder pad.

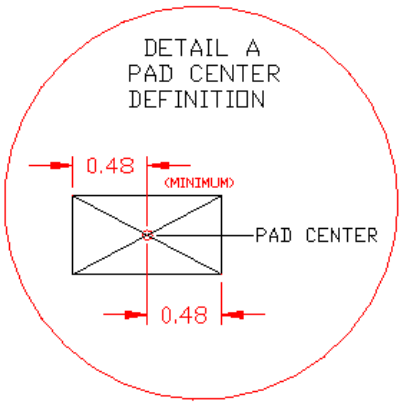
Table 3. Module Solder Pad Location

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Dimension from Origin (mils)
1	(0.23, 2.31)	(9.06, 119.29)
2	(0.23, 3.36)	(9.06, 132.28)
3	(0.23, 4.41)	(9.06, 201.97)
4	(0.23, 5.46)	(9.06, 243.31)
5	(0.23, 6.51)	(9.06, 284.65)
6	(0.23, 7.56)	(9.06, 297.64)
7	(0.82,8.77)	(32.28, 345.27)
8	(1.88,8.77)	(74.02, 345.27)
9	(2.93,8.77)	(115.35, 345.27)
10	(3.98,8.77)	(156.69, 345.27)
11	(5.03,8.77)	(198.03, 345.27)
12	(6.08,8.77)	(239.37, 345.27)
13	(7.13,8.77)	(280.71, 345.27)
14	(8.18,8.77)	(322.05, 345.27)
15	(8.77,7.56)	(345.27, 297.64)
16	(8.77,6.51)	(345.27,256.30)
17	(8.77,5.46)	(345.27, 214.96)
18	(8.77,4.41)	(345.27, 173.62)
19	(8.77,3.36)	(345.27, 132.28)

Figure 7. Solder Pad Reference Location



Top View (Seen on Host PCB)



Module Connections

Table 4 details the solder pad connection definitions and available functions for the pad connections for the CYBT-353027-02 module. Table 4 lists the solder pads on the CYBT-353027-02 module, the silicon device pin, and denotes what functions are available for each solder pad.

Table 4. CYBT-353027-02 Solder Pad Connection Definitions

Pad	Pad Name	Silicon Port Pin Name(s)	UART	SPI[3]	I2C	ADC	COEX	CLK/XTAL	GPIO	Other
1	GND	GND	Ground							
2	GPIO_4	GPIO_4/P1/I2S_CLK/PCM_CLK		SPI1_MISO/P1 (master)		IN28/P1			✓	PCM_CLK I2S_CLK
3	P11	P11/I2S_WS/PCM_SYNC				IN24			✓	PCM_Sync I2S_WS
4	P3	P3/I2S_DI/PCM_IN		SPI1_CLK (master)	SDA				✓	PCM_DI I2S_DI
5	XRES	RST_N	External Reset (Active Low)							
6	GPIO_5	BT_GPIO_5/P8/P33	PUART_RX/P33			IN27/P8 IN6/P33	✓ (GCI_SECI_OUT)	ACK1/P33	✓	
7	SPI2_CS_N	SPI2_CSN[4]		SPI2_CS_N						
8	GPIO_0	BT_GPIO_0							✓ (Dev Wake)	
9	GPIO_1	BT_GPIO_1							✓ (Host Wake)	
10	UART_TXD	BT_UART_TXD	HCI UART Transmit Data							
11	CLK_REQ	BT_CLK_REQ	Used for shared-clock applications							
12	UART_RXD	BT_UART_RXD	HCI UART Receive Data							
13	VDDIN	VDDO	VDDIN (2.3V ~ 3.6V)							
14	GND	GND	Ground							
15	UART_RTS	BT_UART_RTS_N	HCI UART Request To Send Output							
16	GPIO_3	BT_GPIO_3/P0	PUART_TX/P0	SPI1_MOSI/P0 (master)		IN29/P0			✓	
17	UART_CTS	BT_UART_CTS_N	HCI UART Clear To Send Input							
18	GPIO_6	BT_GPIO_6/P9/I2S_DO/PCM_OUT			SCL	IN26/P9	✓ (GCI_SECI_IN)		✓	I2S_DO PCM_Out
19	GND	GND	Ground							

Note
3. The CYBT-353027-02 contains a single SPI (SPI1) peripheral supporting master configuration. SPI2 is used for on-module serial memory interface.
4. SPI2_CS_N is internally routed on the module to on-board serical flash memory. SPI2_CS_N is made available on module pad 7 to be used for Recover Mode operation only.

Connections and Optional External Components

Power Connections (VDDIN)

The CYBT-353027-02 contains one power supply connection, VDDIN. VDDIN accepts a supply input range of 2.3 V to 3.6 V for CYBT-353027-02. Table 11 provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in Table 11.

It is not required to place any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included, but is not necessary. If used, the ferrite bead should be positioned as close as possible to the module pin connection and the recommended ferrite bead value is 330 Ω, 100 MHz.

Considerations and Optional Components for Brown Out (BO) Conditions

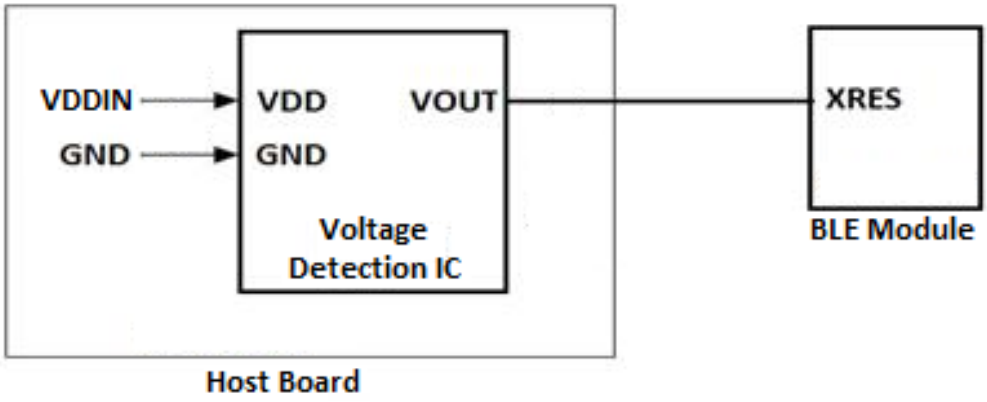
Power supply design must be completed to ensure that the CYBT-353027-02 module does not encounter a Brown Out condition, which can lead to unexpected functionality, or module lock up. A Brown Out condition may be met if power supply provided to the module during power up or reset is in the following range:

$$V_{IL} \leq VDDIN \leq V_{IH}$$

Refer to Table 12 for the V_{IL} and V_{IH} specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (that is, battery installation, high-value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brown Out voltage range from occurring during power removal. Refer to Figure 8 for the recommended circuit design when using an external voltage detection IC.

Figure 8. Reference Circuit Block Diagram for External Voltage Detection IC



In the event that the module does encounter a Brown Out condition, and is operating erratically or not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brown Out conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brown Out condition.

External Reset (XRES)

The CYBT-353027-02 has an integrated power-on reset circuit, which completely resets all circuits to a known power-on state. This action can also be evoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYBT-353027-02 module (solder pad 5). The CYBT-353027-02 module does not require an external pull-up resistor on the XRES input

During power-on operation, the XRES connection to the CYBT-353027-02 is required to be held low 50 ms after the VDD power supply input to the module is stable. This can be accomplished in the following ways:

- The host device should connect a GPIO to the XRES of the Cypress CYBT-353027-02 module and pull XRES low until VDD is stable. XRES is recommended to be released 50 ms after VDDIN is stable.
- If the XRES connection of the CYBT-353027-02 module is not used in the application, a 10-µF capacitor may be connected to the XRES solder pad of the CYBT-353027-02 in order to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the VDDIN power supply ramp time of the system. The capacitor value should result in an XRES release timing of 50 ms after VDDIN stability.
- The XRES release timing may be controlled by a external voltage detection IC. XRES should be released 50 ms after VDD is stable.

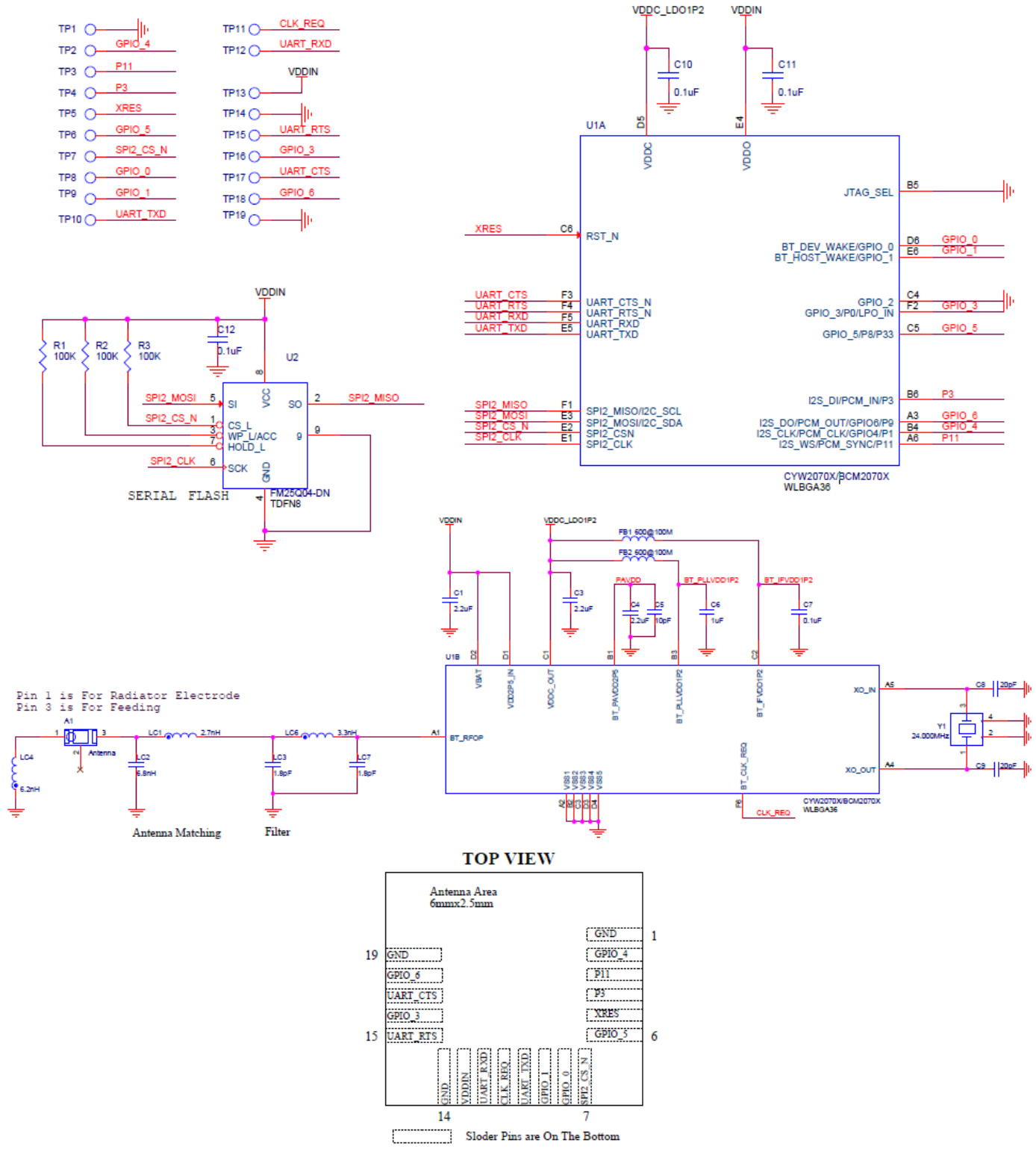
Refer to Figure 11 on page 17 for XRES operating and timing requirements during power-on events.

Multiple-Bonded GPIO Connections

The CYBT-353027-02 contains GPIOs, which are multiple-bonded at the silicon level. If any of these dual-bonded GPIOs are used, only the functionality and features for one of these port pins may be used. The desired port pin should be configured in the WICED Studio SDK. For details on the port pins that are multiple-bonded, refer to the GPIO Port section of this document.

Figure 9 illustrates the CYBT-353027-02 schematic.

Figure 9. CYBT-353027-02 Schematic Diagram



Critical Components List

Table 5 details the critical components used in the CYBT-353027-02 module.

Table 5. Critical Component List

Component	Reference Designator	Description
Silicon	U1	36-pin FBGA BT/BLE Silicon Device - CYW2070X
Silicon	U2	8-pin TDF8N, 512K Serial Flash
Crystal	Y1	24.000 MHz, 12PF

Antenna Design

Table 6 details trace antenna used in the CYBT-353027-02 module. For more information, see Table 6.

Table 6. Chip Antenna Specifications

Item	Description
Frequency Range	2400–2500 MHz
Peak Gain	-1.0 dBi typical
Return Loss	10 dB minimum

Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL and TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types. The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Bluetooth Features

CYBT-353027-02 is qualified to the Bluetooth 5.0 specification. CYBT-353027-02 supports all Bluetooth 4.2 and legacy features, with the following benefits.

- Dual-mode Bluetooth (BT Classic and BLE) operation
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption pause resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link supervision time out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link timeout supervision.
- Quality of service (QoS) enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.
- Secure connections (BR/EDR)
- Fast advertising interval
- Piconet clock adjust
- Connectionless broadcast
- LE privacy v1.1
- Low duty cycle directed advertising
- LE dual mode topology

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state in the LCU.

- States:
  - Standby
  - Connection
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff
  - Advertising
  - Scanning

Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth clock, and device address.

Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4-GHz transceiver, which then processes the power-down functions accordingly.

Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in deep sleep (HIDOFF) mode.

BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the CYBT-353027-02 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYBT-353027-02 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF (Deep Sleep) mode

The CYBT-353027-02 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

In HIDOFF (Deep Sleep) mode, the CYBT-353027-02 baseband and core are powered off by disabling power to LDOOUT. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

Microcontroller Unit

The microcontroller unit in CYBT-353027-02 runs software from the link control (LC) layer up to the host controller interface (HCI). The microcontroller is based on the Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The microcontroller also includes 848 KB of ROM memory for program storage and boot ROM, 352 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

NVRAM Configuration Data and Storage

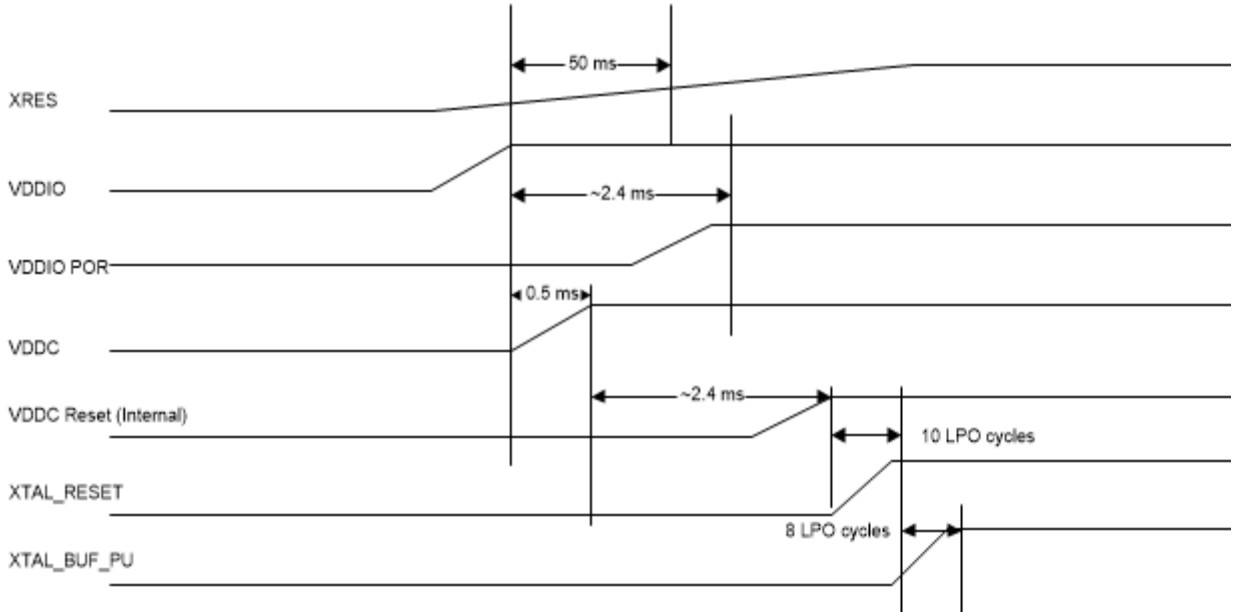
NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The CYBT-353027-02 uses SPI Serial Flash for NVRAM storage.

External Reset (XRES)

The CYBT-353027-02 has an integrated power-on reset circuit that completely resets all circuits to a known power-on state. An external active low reset signal, XRES, can be used to put the CYBT-353027-02 in the reset state. The XRES pin has an internal pull-up resistor and, in most applications, it does not require anything to be connected to it.

Figure 10. External Reset Internal Timing

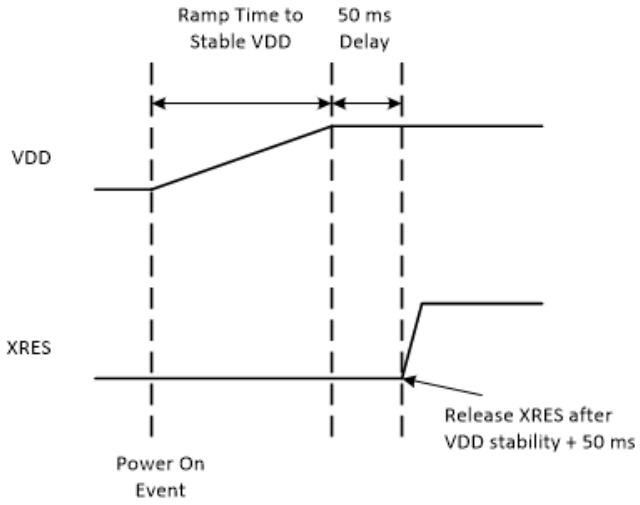


External Reset (XRES) Recommended External Components and Proper Operation

During a power-on event, the XRES line of the CYBT-353027-02 is required to be held low 50 ms after the VDD power supply input to the module is stable. Refer to Figure 11 for the Power-On XRES timing operation. This power-on operation can be accomplished in the following ways:

- A host device should connect a GPIO to the XRES of the Cypress CYBT-353027-02 module and pull XRES low until VDD is stable. XRES can be released after VDD is stable.
- If the XRES connection of the CYBT-353027-02 module is not used in the application, a 10-µF capacitor may be connected to the XRES solder pad of the CYBT-353027-02.
- The XRES release timing can also be controlled via an external voltage detection circuit.

Figure 11. Power-On External Reset (XRES) Operation



Integrated Radio Transceiver

The CYBT-353027-02 has an integrated radio transceiver that has been optimized for use in 2.4-GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. The CYBT-353027-02 is fully compliant with the Bluetooth Radio Specification and enhanced data rate (EDR) specification and meets or exceeds the requirements to provide the highest communication link quality of service.

Transmitter Path

The CYBT-353027-02 a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4-GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible with the BLE specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, π4-DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

Receiver Path

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYBT-353027-02 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the CYBT-353027-02 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

Local Oscillator Generation

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation sub-block employs an architecture for high immunity to LO pulling during PA operation. The CYBT-353027-02 uses an internal loop filter.

Calibration

The CYBT-353027-02 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration tunes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops, and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Internal LDO

The microcontroller in CYBT-353027-02 uses two LDOs – one for 1.2 V and the other for 2.5 V. The 1.2-V LDO provides power to the baseband and radio and the 2.5-V LDO powers the PA.

Collaborative Coexistence

The CYBT-353027-02 provides extensions and collaborative coexistence to the standard Bluetooth AFH for direct communication with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously in a single device. The device supports industry-standard coexistence signaling, including 802.15.2, and supports Cypress and third-party WLAN solutions.

Global Coexistence Interface

The CYBT-353027-02 supports the proprietary Cypress Global Coexistence Interface (GCI) which is a 2-wire interface.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over GCI_SECI_IN and GCI_SECI_OUT a two-wire interface, one serial input (GCI_SECI_IN), and one serial output (GCI_SECI_OUT). The pad configuration registers must be programmed to choose the digital I/O pins that serve the GCI_SECI_IN and GCI_SECI_OUT function.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronization upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

SECI I/O

The microcontroller in CYBT-353027-02 has dedicated GCI_SECI_IN (PAD18/GPIO_6) and GCI_SECI_OUT (PAD 6/GPIO_5) pins. Refer to Table 4, which detail the module solder pad number used for SECI I/O.

Peripheral and Communication Interfaces

Cypress Serial Communications Interface

The CYBT-353027-02 provides a 2-pin master BSC interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I^2C slave devices. The BSC does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by the BSC:

- 100 kHz
- 400 kHz
- 800 kHz (not a standard I^2C-compatible speed.)
- 1 MHz (Compatibility with high-speed I^2C-compatible devices is not guaranteed.)
- The following transfer types are supported by the BSC:
- Read (Up to 127 bytes can be read)
- Write (Up to 127 bytes can be written)
- Read-then-Write (Up to 127 bytes can be read and up to 127 bytes can be written)
- Write-then-Read (Up to127 bytes can be written and up to 127 bytes can be read)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pad (I2C_SCL) and data pad 2 (I2C_SDA) are both open-drain I/O pins. Pull-up resistors, external to the CYBT-353027-02, are required on both the SCL and SDA pad for proper operation.

HCI UART Interface

The UART physical interface is a standard, 2-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 38400 bps to 6 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYBT-353027-02 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 6 Mbps. The baud rate of the CYBT-353027-02UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Table 7 contains example values to generate common baud rates with a 24 MHz UART clock.

Table 7. Common Baud Rate Examples, 24 MHz Clock

Baud Rate (bps)	Baud Rate Adjustment		Mode	Error (%)
	High Nibble	Low Nibble		
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16
38400	0x01	0x00	Normal	0.00

Table 8 contains example values to generate common baud rates with a 48 MHz UART clock.

Table 8. Common Baud Rate Examples, 48 MHz Clock

Baud Rate (bps)	High Rate	Low Rate	Mode	Error (%)
6M	0xFF	0xF8	High rate	0
4M	0xFF	0xF4	High rate	0
3M	0x0	0xFF	Normal	0
2M	0x44	0xFF	Normal	0
1.5M	0x0	0xFE	Normal	0
1M	0x0	0xFD	Normal	0
921600	0x22	0xFD	Normal	0.16
230400	0x0	0xF3	Normal	0.16
115200	0x1	0xE6	Normal	–0.08
57600	0x1	0xCC	Normal	0.04
38400	0x11	0xB2	Normal	0

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYBT-353027-02 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Peripheral UART Interface

The CYBT-353027-02 has a second UART that may be used to interface to other peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each signal as shown in Table 9 The CYBT-353027-02 supports a two wire UART interface. Flow Control is not supported on this module.

Table 9. CYBT-353027-02 Peripheral UART

Signal Name	PUART_TX	PUART_RX	PUART_CTS_N	PUART_RTS_N
Configured port name	P0	P33	-	-

Serial Peripheral Interface

The CYBT-353027-02 has two independent SPI interfaces. One is a master-only interface (SPI2) and is used for on-module SFLASH interface. The other (SPI1) can be used as a master interface. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYBT-353027-02 has optional I/O ports that can be configured individually and separately for each functional pin. The CYBT-353027-02 acts as an SPI master device that supports 2.3 V or 3.3 V SPI slaves. The CYBT-353027-02 can also act as an SPI slave device that supports a 2.3 V or 3.3 V SPI master.

SPI voltage depends on VDD; therefore, it defines the type of devices that can be supported

PCM Interface

The CYBT-353027-02 includes a PCM interface that shares pins with the I^2S interface. The PCM Interface on the CYBT-353027-02 can connect to linear PCM codec devices in master or slave mode. In master mode, the CYBT-353027-02 generates the PCM_CLK and PCM_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the CYBT-353027-02.

Slot Mapping

The CYBT-353027-02 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The CYBT-353027-02 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The CYBT-353027-02 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the CYBT-353027-02 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

Clock Frequencies

The CYBT-353027-02 has an integrated 24 MHz crystal on the module. There is no need to add an additional crystal oscillator.

ADC Port

The ADC is a Σ-Δ ADC core designed for audio (12 bits) and DC (10 bits) measurement. There are 5 solder pad connections that can act as input channels on the CYBT-353027-02 module.

The following CYBT-353027-02 module solder pads can be used as ADC inputs:

- Pad 2: P1, ADC Input Channel 28
- Pad 3: P11, ADC Input Channel 24
- Pad 6: P8/P33, ADC Input Channels 27/6 respectively; NOTE: only one ADC input on this solder pad can be active at a given time.
- Pad 16: P0, ADC Input Channel 29
- Pad 18: P9, ADC Input Channel 26

GPIO Port

The CYBT-353027-02 has eight GPIOs besides two I^2C pads. All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3 V or 4 mA at 1.8 V,.

The following GPIOs are available on the module pads:

- PAD 2 GPIO_4: GPIO_4/P1/I^2S_CLK_PCM_CLK (triple bonded; only one of three is available)
- PAD 3 P11: P11/I^2S_WS_PCM_SYNC (Dual bonded; only one of two is available)
- PAD 4 P3: P3/I^2S_DI_PCM_IN (dual bonded; only one of two is available)
- PAD 6 GPIO_5: GPIO_5/P8/P33 (triple bonded; only one of three is available)
- PAD 8 GPIO_0
- PAD 9 GPIO_1
- PAD 16 GPIO_3: GPIO_3/P0/LPO_IN (triple bonded; only one of three is available)
- PAD 18 GPIO_6: GPIO_6/P9/I^2S_DO_PCM_OUT (triple bonded; only one of three is available)

Pads 2, 3, 6, 16, and 18 can be programmed as ADC inputs.

NOTE: SPI2_CS_N is internally routed on the module to on-board serial flash memory. SPI2_CS_N is made available on module pad 7 to be used for Recover Mode operation only. No other functionality should be used with this connection.

Electrical Characteristics

Table 10 shows the maximum electrical rating for voltages referenced to VDD pin.

Table 10. Maximum Electrical Rating

Rating	Symbol	Value	Unit
V_{DDIN}	–	3.795	V
Voltage on input or output pin	–	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating ambient temperature range	Topr	-30 to +85	°C
Storage temperature range	Tstg	–40 to +85	°C

Table 11 shows the power supply characteristics for the range T_J = 0 to 125 °C.

Table 11. Power Supply

Parameter	Description	Minimum[5]	Typical	Maximum[5]	Unit
V_{DDIN}	Power Supply Input (CYBT-353027-02)	2.3	–	3.6	V

Table 12 shows the specifications for the digital voltage levels.

Table 12. Digital Levels

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.8	V
Input high voltage	V_{IH}	2.0	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	V_{DD} – 0.4	–	–	V
Input capacitance (V_{DDMEM} domain)	C_{IN}	–	–	0.4	pF

Table 13 shows the current consumption measurements

Table 13. Bluetooth, BLE, BR and EDR Chipset Current Consumption, Class 1

Mode	Remarks	Typ	Unit
3DH5/3DH5	–	37.10	mA
BLE			
■ BLE	Connected 600-ms interval	211	µA
■ BLE ADV	Unconnectable 1.00 sec	176	µA
■ BLE Scan	No devices present. A 1.28 second interval with a scan window of 11.25 ms	355	µA
DMx/DHx			
■ DM1/DH1	–	32.15	mA
■ DM3/DH3	–	38.14	mA
■ DM5/DH5	–	38.46	mA
HIDOFF	Deep sleep	2.69	µA
Page scan	Periodic scan rate is 1.28 sec	0.486	mA
Receive			
■ 1 Mbps	Peak current level during reception of a basic-rate packet.	26.373	mA
■ EDR	Peak current level during the reception of a 2 or 3 Mbps rate packet.	26.373	mA

Note
5. Overall performance degrades beyond minimum and maximum supply voltages.The voltage range specified is determined by the minimum and maximum operating voltage of the SPI Serial Flash included on the module.

Table 13. Bluetooth, BLE, BR and EDR Chipset Current Consumption, Class 1

Mode	Remarks	Typ	Unit
Sniff Slave			
■ 11.25 ms	–	4.95	mA
■ 22.5 ms	–	2.6	mA
■ 495.00 ms	Based on one attempt and no timeout.	254	µA
Transmit			
■ 1 Mbps	Peak current level during the transmission of a basic-rate packet: GFSK output power = 10 dBm.	60.289	mA
■ EDR	Peak current level during the transmission of a 2 or 3 Mbps rate packet. EDR output power = 8 dBm.	52.485	mA

Table 14. Bluetooth and BLE Chipset Current Consumption, Class 2 (0 dBm)

Mode	Remarks	Typ.	Unit
3DH5/3DH5	–	31.57	mA
BLE			
■ BLE ADV	Unconnectable 1.00 sec	174	µA
■ BLE Scan	No devices present. A 1.28 second interval with a scan window of 11.25 ms	368	µA
DMx/DHx			
■ DM1/DH1	–	27.5	mA
■ DM3/DH3	–	31.34	mA
■ DM5/DH5	–	32.36	mA

Chipset RF Specifications

All specifications in Table 15 are for industrial temperatures and are single-ended. Unused inputs are left open.

Table 15. Chipset Receiver RF Specifications

Parameter	Conditions	Minimum	Typical[6]	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity[7]	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	LE GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Maximum input	π/4-DQPSK, 8-DPSK, 2/3 Mbps	–	–	–20	dBm
Interference Performance					
C/I cochannel	GFSK, 0.1% BER	–	9.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–5	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–49	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–27	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–37	–20.0	dB
C/I cochannel	π/4-DQPSK, 0.1% BER	–	11	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–8	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–40	–30.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–50	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–27	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–40	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	17	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–5	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–40	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–47	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–20	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–35	–13.0	dB
Out-of-Band Blocking Performance (CW)[8]					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm

Notes
6. Typical operating conditions are 1.22-V operating voltage and 25°C ambient temperature.
7. The receiver sensitivity is measured at BER of 0.1% on the device interface.
8. Meets this specification using front-end band pass filter.

Table 15. Chipset Receiver RF Specifications (continued)

Parameter	Conditions	Minimum	Typical[6]	Maximum	Unit
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-Band Blocking Performance, Modulated Interferer					
776–764 MHz	CDMA	–	–10[9]	–	dBm
824–849 MHz	CDMA	–	–10[9]	–	dBm
1850–1910 MHz	CDMA	–	–23[9]	–	dBm
824–849 MHz	EDGE/GSM	–	–10[9]	–	dBm
880–915 MHz	EDGE/GSM	–	–10[9]	–	dBm
1710–1785 MHz	EDGE/GSM	–	–23[9]	–	dBm
1850–1910 MHz	EDGE/GSM	–	–23[9]	–	dBm
1850–1910 MHz	WCDMA	–	–23[9]	–	dBm
1920–1980 MHz	WCDMA	–	–23[9]	–	dBm
Intermodulation Performance[10]					
BT, Df = 5 MHz	–	–39.0	–	–	dBm
Spurious Emissions[11]					
30 MHz to 1 GHz	–	–	–	–62	dBm
1 GHz to 12.75 GHz	–	–	–	–47	dBm
65 MHz to 108 MHz	FM Rx	–	–147	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–147	–	dBm/Hz
851–894 MHz	CDMA	–	–147	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1930–1990 MHz	PCS	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–147	–	dBm/Hz

Notes
9. Numbers are referred to the pin output with an external BPF filter.
10. f0 = -64 dBm Bluetooth-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.
11. Includes baseband radiated emissions.

Table 16. Chipset Transmitter RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class1: GFSK Tx power[12]	–	–	12	–	dBm
Class1: EDR Tx power[13]	–	–	9	–	dBm
Class 2: GFSK Tx power	–	–	2	–	dBm
Power control step	–	2	4	8	dB
Modulation Accuracy					
π/4-DQPSK Frequency Stability	–	–10	–	10	kHz
π/4-DQPSK RMS DEVM	–	–	–	20	%
π/4-QPSK Peak DEVM	–	–	–	35	%
π/4-DQPSK 99% DEVM	–	–	–	30	%
8-DPSK frequency stability	–	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	–	13	%
8-DPSK Peak DEVM	–	–	–	25	%
8-DPSK 99% DEVM	–	–	–	20	%
In-Band Spurious Emissions					
1.0 MHz < |M – N| < 1.5 MHz	–	–	–	–26	dBc
1.5 MHz < |M – N| < 2.5 MHz	–	–	–	–20	dBm
|M – N| ≥ 2.5 MHz	–	–	–	–40	dBm
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0[14]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[14, 15]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm

Table 17. Chipset BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	N/A	2402	–	2480	MHz
Rx sense[16]	GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
Tx power[17]	N/A	–	9	–	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[18]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

12. TBD dBm output for GFSK measured with PAVDD = 2.5 V.
13. TBD dBm output for EDR measured with PAVDD = 2.5 V.
14. Maximum value is the value required for Bluetooth qualification.
15. Meets this spec using a front-end band-pass filter.
16. Dirty Tx is Off.
17. The BLE Tx power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc. The output is capped at 12 dBm out. The BLE Tx power at the antenna port cannot exceed the 10 dBm EIRP specification limit.
18. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

Timing and AC Characteristics

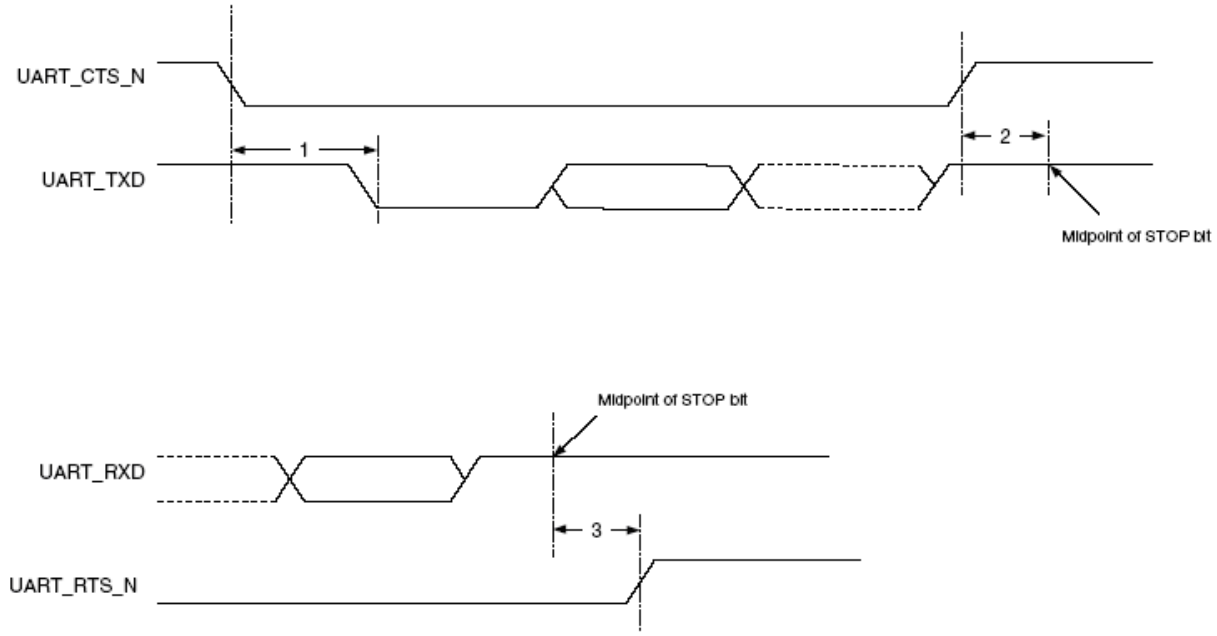
In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

UART Timing

Table 18. UART Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baud out cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baud out cycles

Figure 12. UART Timing



SPI Timing

The SPI interface supports clock speeds up to 12 MHz

Table 19 and Figure 13 show the timing requirements when operating in SPI Mode 0 and 2, and SPI Mode 1 and 3, respectively.

Table 19. SPI Mode 0 and 2

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	∞	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	∞	ns
3	Time from master assert SPI_CSN to first clock edge	20	∞	ns
4	Setup time for MOSI data lines	8	½ SCK	ns
5	Hold time for MOSI data lines	8	½ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	∞	ns
8	Idle time between subsequent SPI transactions	1 SCK	∞	ns

Figure 13. SPI Timing – Mode 0 and 2

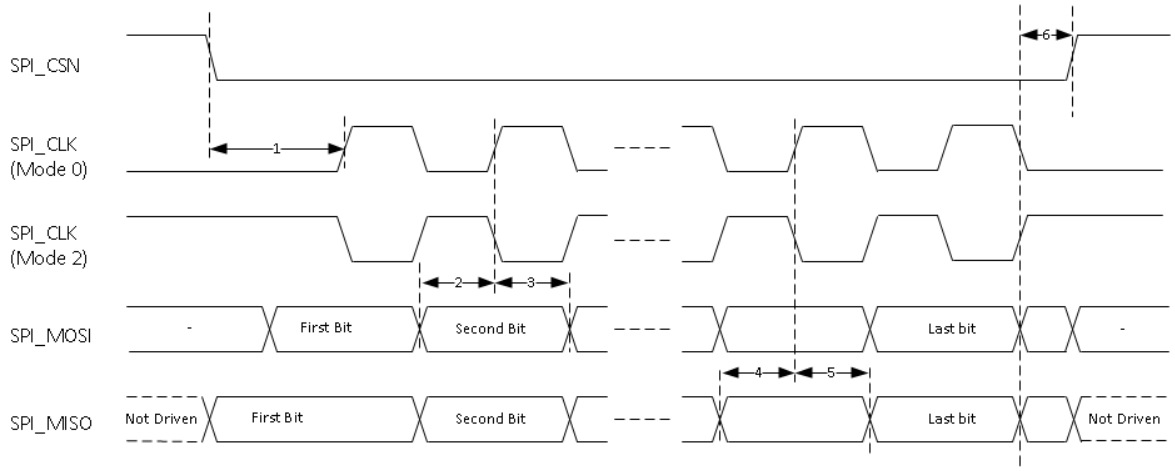
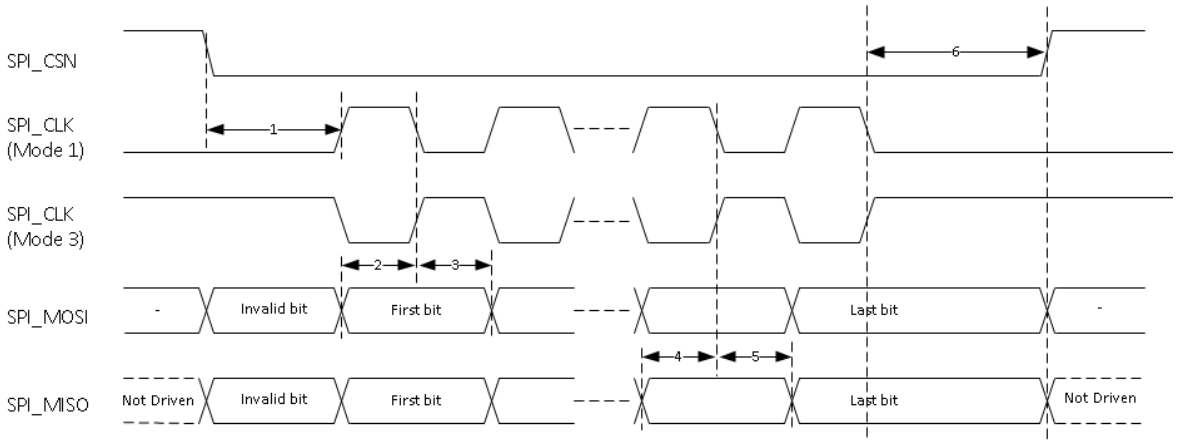


Table 20 and Figure 14 show the timing requirements when operating in SPI Mode 1 and 3.

Table 20. SPI Mode 1 and 3

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	∞	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	∞	ns
3	Time from master assert SPI_CSN to first clock edge	20	∞	ns
4	Setup time for MOSI data lines	8	½ SCK	ns
5	Hold time for MOSI data lines	8	½ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	∞	ns
8	Idle time between subsequent SPI transactions	1 SCK	∞	ns

Figure 14. SPI Timing – Mode 1 and 3

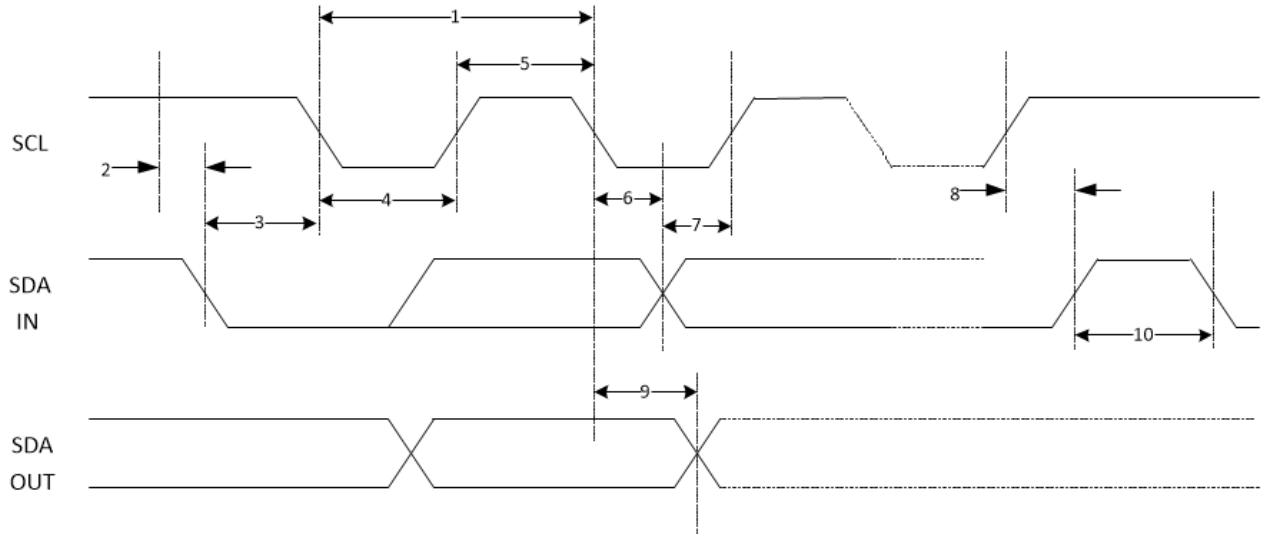


BSC Interface Timing

Table 21. BSC Interface Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[19]	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[20]	650	–	ns

Figure 15. BSC Interface Timing Diagram



Notes
19. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
20. Time that the cbus must be free before a new transaction can start.

PCM Interface Timing

Short Frame Sync, Master Mode

Figure 16. PCM Timing Diagram (Short Frame Sync, Master Mode)

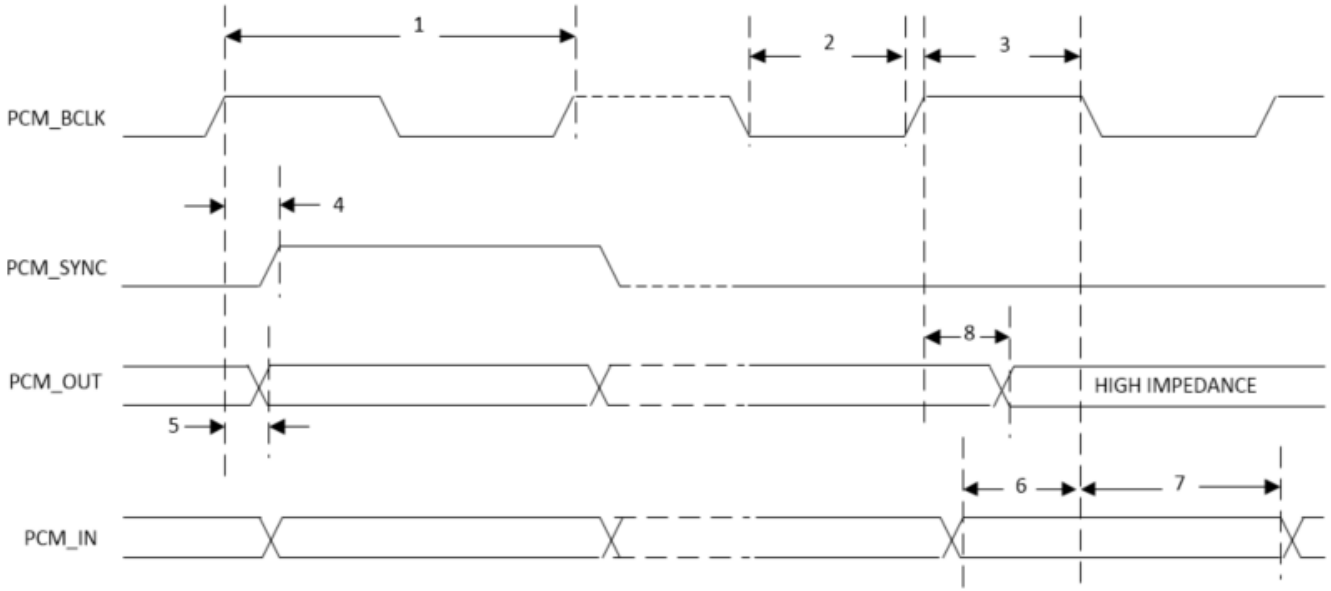


Table 22. PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	20.0	MHz
2	PCM bit clock LOW	20.0	–	–	ns
3	PCM bit clock HIGH	20.0	–	–	ns
4	PCM_SYNC delay	0	–	5.7	ns
5	PCM_OUT delay	–0.4	–	5.6	ns
6	PCM_IN setup	16.9	–	–	ns
7	PCM_IN hold	25.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	–0.4	–	5.6	ns

Short Frame Sync, Slave Mode

Figure 17. PCM Timing Diagram (Short Frame Sync, Slave Mode)

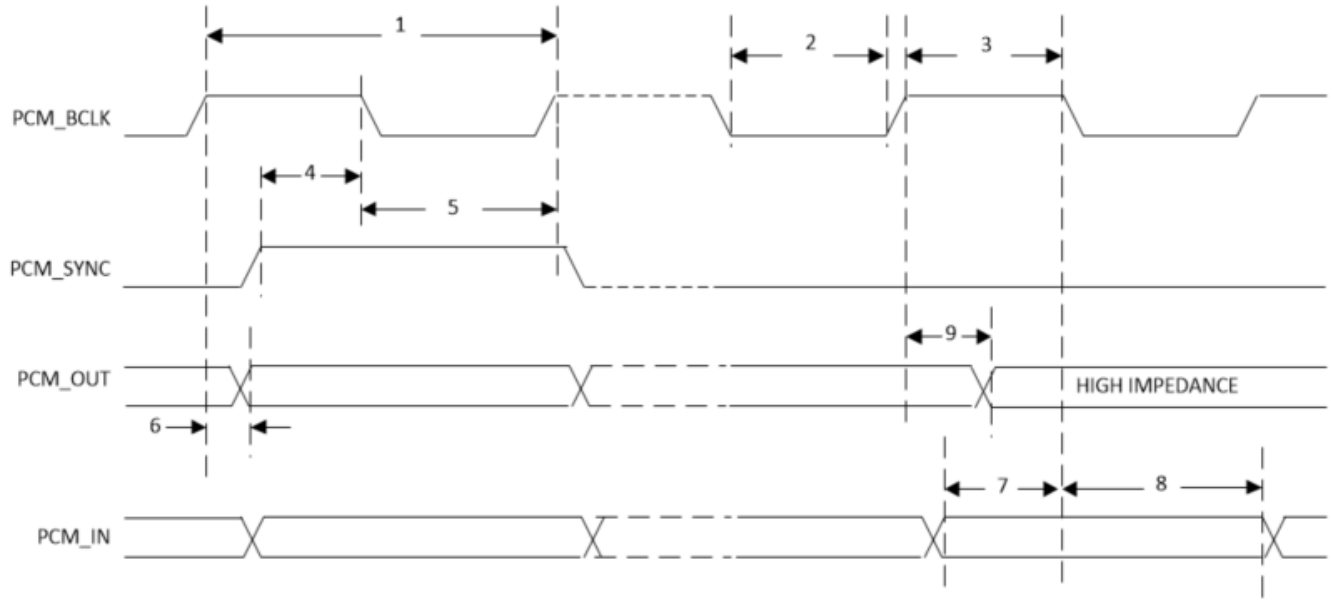


Table 23. PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	TBD	MHz
2	PCM bit clock LOW	TBD	–	–	ns
3	PCM bit clock HIGH	TBD	–	–	ns
4	PCM_SYNC setup	TBD	–	–	ns
5	PCM_SYNC hold	TBD	–	–	ns
6	PCM_OUT delay	TBD	–	TBD	ns
7	PCM_IN setup	TBD	–	–	ns
8	PCM_IN hold	TBD	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	TBD	–	TBD	ns

Long Frame Sync, Master Mode

Figure 18. PCM Timing Diagram (Long Frame Sync, Master Mode)

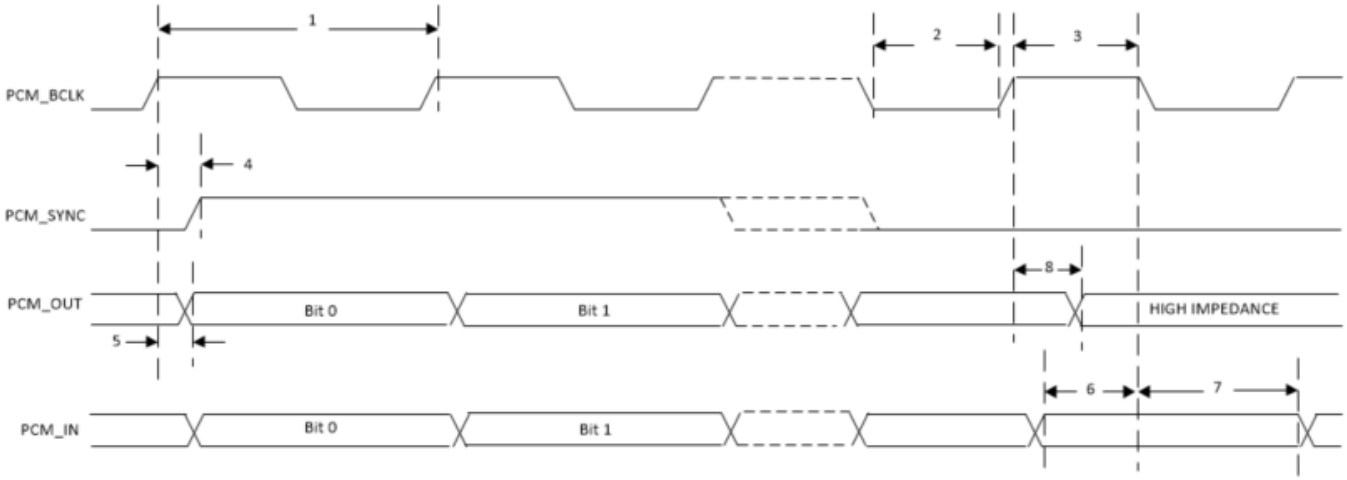


Table 24. PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	TBD	MHz
2	PCM bit clock LOW	TBD	–	–	ns
3	PCM bit clock HIGH	TBD	–	–	ns
4	PCM_SYNC delay	TBD	–	TBD	ns
5	PCM_OUT delay	TBD	–	TBD	ns
6	PCM_IN setup	TBD	–	–	ns
7	PCM_IN hold	TBD	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	TBD	–	TBD	ns

Long Frame Sync, Slave Mode

Figure 19. PCM Timing Diagram (Long Frame Sync, Slave Mode)

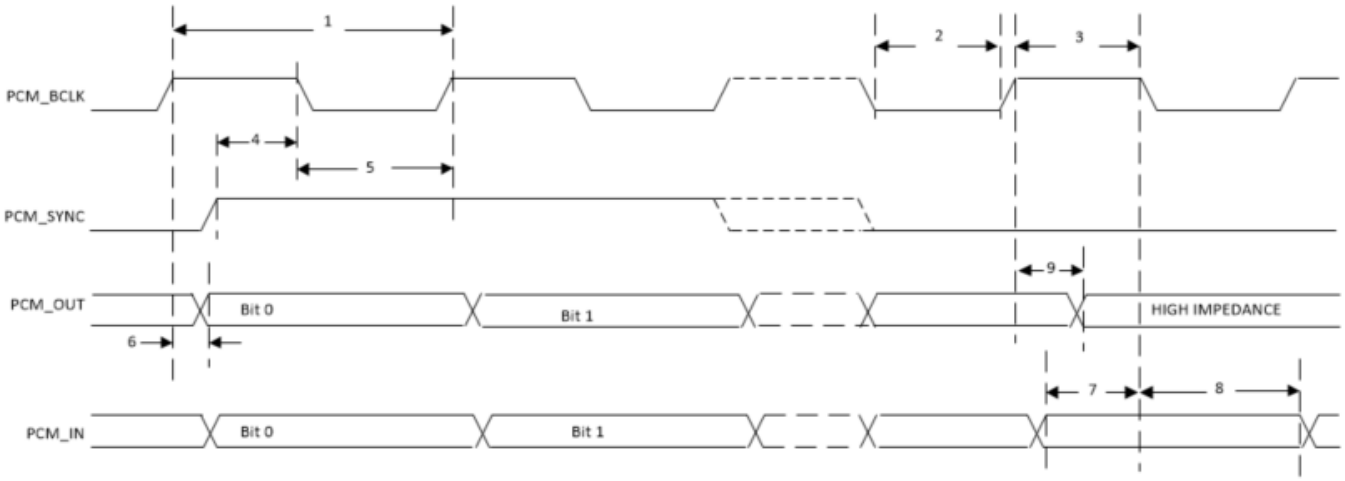


Table 25. PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	TBD	MHz
2	PCM bit clock LOW	TBD	–	–	ns
3	PCM bit clock HIGH	TBD	–	–	ns
4	PCM_SYNC setup	TBD	–	–	ns
5	PCM_SYNC hold	TBD	–	–	ns
6	PCM_OUT delay	TBD	–	TBD	ns
7	PCM_IN setup	TBD	–	–	ns
8	PCM_IN hold	TBD	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	TBD	–	TBD	ns

I²S Interface Timing

The I²S interface supports both master and slave modes. The I²S signals are:

- I²S clock: I²S SCK
- I²S Word Select: I²S WS
- I²S Data Out: I²S SDO
- I²S Data In: I²S SDI

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYBT-013033-01 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider. In the slave mode, any clock rate is supported to a maximum of 3.072 MHz. Timing values specified in Table 26 are relative to high and low threshold levels.

Table 26. Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	Notes
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	Note 21
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	Note 22
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	Note 22
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	Note 23
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	Note 23
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	Note 24
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	Note 25
Hold time t_{htr}	0	–	–	–	–	–	–	–	Note 25
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	Note 26
Hold time t_{hr}	–	–	–	–	–	0	–	–	Note 26

Notes

21. The system clock period T must be greater than Ttr and Tr because both the transmitter and receiver have to be able to handle the data transfer rate.
22. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, tHC and tLC are specified with respect to T.
23. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35Tr, any clock that meets the requirements can be used.
24. Because the delay (tdtr) and the maximum transmitter speed (defined by Ttr) are related, a fast transmitter driven by a slow clock edge can result in tdtr not exceeding tRC which means thtr becomes zero or negative. Therefore, the transmitter has to guarantee that thtr is greater than or equal to zero, so long as the clock rise-time tRC is not more than tRCmax, where tRCmax is not less than 0.15Ttr.
25. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
26. The data setup and hold time must not be less than the specified receiver setup and hold time.

Environmental Specifications

Environmental Compliance

This CYBT-353027-02 BLE module is produced in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen-Free (HF) directives. The Cypress module and components used to produce this module are RoHS and HF compliant.

RF Certification

The CYBT-353027-02 module will be certified under the following RF certification standards at production release.

- FCC: WAP3027
- CE
- IC: 7922A-3027
- MIC: TBD

Safety Certification

The CYBT-353027-02 module complies with the following safety regulations:

- Underwriters Laboratories, Inc. (UL): Filing E331901
- CSA
- TUV

Environmental Conditions

Table 27 describes the operating and storage conditions for the Cypress BLE module.

Table 27. Environmental Conditions for CYBT-353027-02

Description	Minimum Specification	Maximum Specification
Operating temperature	-30 °C	85 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	3 °C/minute
Storage temperature	–40 °C	85 °C
Storage temperature and humidity	–	85 °C at 85%
ESD: Module integrated into end system Components[27]	–	15 kV Air 2.0 kV Contact

ESD and EMI Protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device Handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

Note
27. This does not apply to the RF pins (ANT).

Regulatory Information

FCC

FCC NOTICE:

The device CYBT-353027-02 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: WAP3027.

In any case the end product must be labeled exterior with "Contains FCC ID: 7922A-3027"

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antenna listed in Table 6 on page 13. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antenna in Table 6 on page 13, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBT-353027-02 with the trace antenna is far below the FCC radio frequency exposure limits. Nevertheless, use CYBT-353027-02 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

ISED

Innovation, Science and Economic Development Canada (ISED) Certification

CYBT-353027-02 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development Canada (ISED),

License: IC: 7922A-3027

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

This device has been designed to operate with the antennas listed in Table 6 on page 13, having a maximum gain of -0.5 dBi. Antennas not included in this list or having a gain greater than -0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED NOTICE:

The device CYBT-353027-02 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYBT-353027-02, y compris l'antenne intégrée, est conforme aux Règles RSS-GEN de Canada. L'appareil répond aux exigences d'approbation de l'émetteur modulaire tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant entraîner un fonctionnement indésirable.

ISED INTERFERENCE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device. (3) SAR is not required for this module as long as the distance is higher than 15mm away from user since the maximum output power is below IC threshold.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement. (3) Le SAR n'est pas requis pour ce module tant que la distance est supérieure à 15 mm par rapport à l'utilisateur, car la puissance de sortie maximale est inférieure au seuil IC.

ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the ISED Notices above. The IC identifier is TBD. In any case, the end product must be labeled in its exterior with "Contains IC: 7922A-3027"

European Declaration of Conformity

Hereby, Cypress Semiconductor declares that the Bluetooth module CYBT-353027-02 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:

All versions of the CYBT-353027-02 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

MIC Japan

CYBT-353027-02 is certified as a module with certification number TBD. End products that integrate CYBT-353027-02 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

Packaging

Table 28. Solder Reflow Peak Temperature

Module Part Number	Package	Maximum Peak Temperature	Maximum Time at Peak Temperature	No. of Cycles
CYBT-353027-02	19-pad SMT	260 °C	30 seconds	2

Table 29. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Module Part Number	Package	MSL
CYBT-353027-02	19-pad SMT	MSL 3

The CYBT-353027-02 is offered in tape and reel packaging. Figure 20 details the tape dimensions used for the CYBT-353027-02.

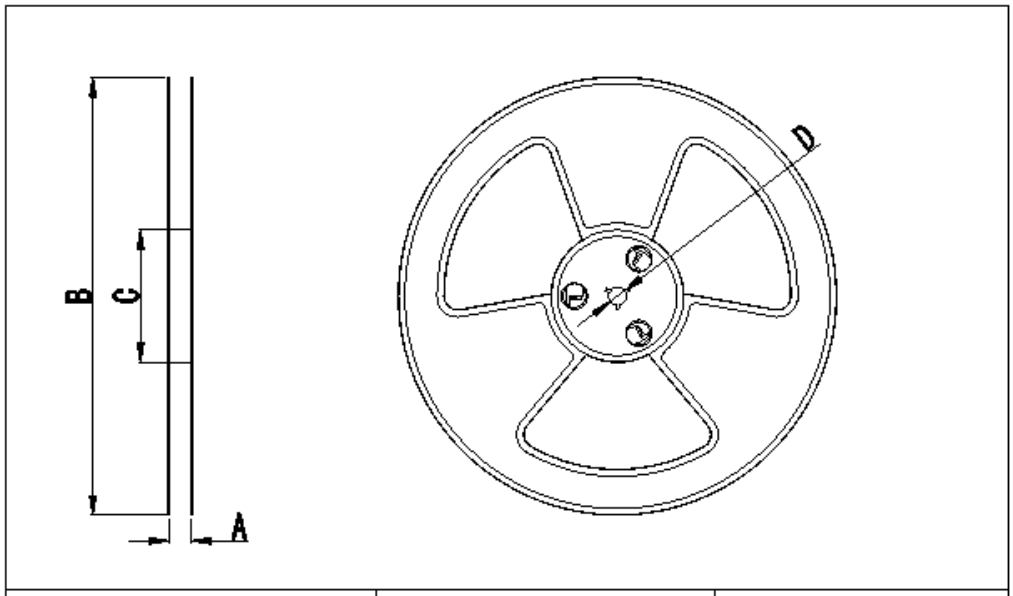
Figure 20. CYBT-353027-02 Tape Dimensions (TBD)

Figure 21 details the orientation of the CYBT-353027-02 in the tape as well as the direction for unreeling.

Figure 21. Component Orientation in Tape and Unreeling Direction (TBD)

Figure 22 details reel dimensions used for the CYBT-353027-02.

Figure 22. Reel Dimensions



Index	NOTE	Dimension	Tolerance	
A	Inside Width	24.4	+2.0mm	-0.0mm
B	Reel Diameter	254.00	+2.0mm	-2.0mm
C	Outer Axis Diameter	100.00	+2.0mm	-2.0mm
D	Inner Axis Diameter	13.20	+0.3mm	-0.2mm

The CYBT-353027-02 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBT-353027-02 is detailed in Figure 23.

Figure 23. CYBT-353027-02 Center of Mass (TBD)

Ordering Information

Table 30 lists the CYBT-353027-02 part number and features. Table 31 lists the reel shipment quantities for the CYBT-353027-02.

Table 30. Ordering Information

Ordering Part Number	Max CPU Speed (MHz)	SFlash Size (KB)	RAM Size (KB)	UART	I^2C	SPI	I^2S	PCM	PWM	ADC Inputs	GPIOs	Package	Packaging
CYBT-353027-02	24	512	352	Yes	Yes	Yes	Yes	Yes	-	5	8	19-SMT	Tape and Reel

Table 31. Tape and Reel Package Quantity and Minimum Order Amount

Description	Minimum Reel Quantity	Maximum Reel Quantity	Comments
Reel Quantity	500	500	Ships in 500 unit reel quantities.
Minimum Order Quantity (MOQ)	500	–	–
Order Increment (OI)	500	–	–

The CYBT-353027-02 is offered in tape and reel packaging. The CYBT-353027-02 ships in a reel size of 500.

For additional information and a complete list of Cypress Semiconductor Wireless products, contact your local Cypress sales representative. To locate the nearest Cypress office, visit our website.

U.S. Cypress Headquarters Address	198 Champion Court, San Jose, CA 95134
U.S. Cypress Headquarter Contact Info	(408) 943-2600
Cypress website address	http://www.cypress.com

Acronyms

Table 32. Acronyms Used in this Document

Acronym	Description	Acronym	Description
ADC	analog-to-digital converter	IDE	integrated development environment
ALU	arithmetic logic unit	I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
AMUXBUS	analog multiplexer bus	IC	Industry Canada
API	application programming interface	IIR	infinite impulse response, see also FIR
ARM®	advanced RISC machine, a CPU architecture	ILO	internal low-speed oscillator, see also IMO
BLE	Bluetooth Low Energy	IMO	internal main oscillator, see also ILO
Bluetooth SIG	Bluetooth Special Interest Group	INL	integral nonlinearity, see also DNL
BW	bandwidth	I/O	input/output, see also GPIO, DIO, SIO, USBIO
CAN	Controller Area Network, a communications protocol	IPOR	initial power-on reset
CE	European Conformity	IPSR	interrupt program status register
CSA	Canadian Standards Association	IRQ	interrupt request
CMRR	common-mode rejection ratio	ITM	instrumentation trace macrocell
CPU	central processing unit	KC	Korea Certification
CRC	cyclic redundancy check, an error-checking protocol	LCD	liquid crystal display
ECC	error correcting code	LIN	Local Interconnect Network, a communications protocol.
ECO	external crystal oscillator	LNA	low noise amplifier
EEPROM	electrically erasable programmable read-only memory	LR	link register
EMI	electromagnetic interference	LUT	lookup table
EMIF	external memory interface	LVD	low-voltage detect, see also LVI
EOC	end of conversion	LVI	low-voltage interrupt, see also HVI
EOF	end of frame	LVTTL	low-voltage transistor-transistor logic
ESD	electrostatic discharge	MAC	multiply-accumulate
FCC	Federal Communications Commission	MCU	microcontroller unit
FET	field-effect transistor	MIC	Ministry of Internal Affairs and Communications (Japan)
FIR	finite impulse response, see also IIR	MISO	master-in slave-out
FPB	flash patch and breakpoint	NC	no connect
FS	full-speed	NMI	nonmaskable interrupt
GPIO	general-purpose input/output, applies to a PSoC pin	NRZ	non-return-to-zero
HCI	host controller interface	NVIC	nested vectored interrupt controller
HVI	high-voltage interrupt, see also LVI, LVD	NVL	nonvolatile latch, see also WOL
IC	integrated circuit	Opamp	operational amplifier
IDAC	current DAC, see also DAC, VDAC	PA	power amplifier

Table 32. Acronyms Used in this Document (continued)

Acronym	Description	Acronym	Description
PAL	programmable array logic, see also PLD	SOF	start of frame
PC	program counter	S/H	sample and hold
PCB	printed circuit board	SINAD	signal to noise and distortion ratio
PGA	programmable gain amplifier	SIO	special input/output, GPIO with advanced features. See GPIO.
PHUB	peripheral hub	SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
PHY	physical layer	SPI	Serial Peripheral Interface, a communications protocol
PICU	port interrupt control unit	SR	slew rate
PLA	programmable logic array	SRAM	static random access memory
PLD	programmable logic device, see also PAL	SRES	software reset
PLL	phase-locked loop	STN	super twisted nematic
PMDD	package material declaration data sheet	SWD	serial wire debug, a test protocol
POR	power-on reset	SWV	single-wire viewer
PRES	precise power-on reset	TD	transaction descriptor, see also DMA
PRS	pseudo random sequence	THD	total harmonic distortion
PS	port read data register	TIA	transimpedance amplifier
PSoC®	Programmable System-on-Chip™	TN	twisted nematic
PSRR	power supply rejection ratio	TRM	technical reference manual
PWM	pulse-width modulator	TTL	transistor-transistor logic
QDID	qualification design ID	TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
RAM	random-access memory	TX	transmit
RISC	reduced-instruction-set computing	UART	Universal Asynchronous Transmitter Receiver, a communications protocol
RMS	root-mean-square	UDB	universal digital block
RTC	real-time clock	USB	Universal Serial Bus
RTL	register transfer language	USBIO	USB input/output, PSoC pins used to connect to a USB port
RTR	remote transmission request	VDAC	voltage DAC, see also DAC, IDAC
RX	receive	WDT	watchdog timer
SAR	successive approximation register	WOL	write once latch, see also NVL
SC/CT	switched capacitor/continuous time	WRES	watchdog timer reset
SCL	I^2C serial clock	XRES	external reset I/O pin
SDA	I^2C serial data	XTAL	crystal
SOC	start of conversion		

Document Conventions

Units of Measure

Table 33. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
dBm	decibel-milliwatts
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Document History Page

Document Title: CYBT-353027-02 EZ-BT™ WICED Module Document Number: 002-23132				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**		DSO	03/13/2018	Preliminary datasheet for CYBT-353027-02 module.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support