

M3000

MOTOR AND MOTION CONTROLLER SUMMARY

SYSTEM^{SS}
SEMICONDUCTOR

M3000 Motor and Motion Controller Summary Change Log

[illegible]

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

System Semiconductor, reserves the right to make changes without further notice to any products herein to improve reliability, function or design. System Semiconductor does not assume any liability arising out of the application or use of any product or circuit described herein in accordance with System Semiconductor's standard warranty; neither does it convey any license under its patent rights of others. System Semiconductor, SYSTEM^{SS}™ and SSI are trademarks of System Semiconductor.



System Semiconductor's general policy does not recommend the use of its products in life support or aircraft applications wherein a failure or malfunction of the product may directly threaten life or injury. Per System Semiconductor's terms and conditions of sales, the user of System Semiconductor, products in life support or aircraft applications assumes all risks of such use and indemnifies System Semiconductor, against all damages.

Table of Contents

Feature Overview.....	1
Description	2
Package Specifications.....	2
SS-M3000-F (160 QFP) Top View.....	2
SS-M3000-S (128 QFP) Top View.....	2
SS-M3001-B (128 BGA) Bottom View.....	2
Block Diagram	3
Absolute Maximum Ratings.....	4
Thermal Characteristics	4
Analog Characteristics.....	4
DC Characteristics	5
Feature Summary by Package	6
Pin Configuration by Package Type	7
Processor Control.....	7
Communications	7
Memory (Code/Program Space) M3000 128 and 160 QFP Only.....	8
Memory (Code/Program Space) M3001 128 TFBGA	9
External Timer	10
Indexer Logic.....	10
Analog.....	10
I/O Ports/Memory.....	11
Motor Bridge Drive Stage	12
Power and Ground	13
Register Summary	14
Motor and Motion Control Registers	14
Interrupt Registers.....	15
Instruction Memory Programming Registers	15
CAN Controller Registers.....	16
ADC Registers	17
DAC Registers	17
Analog Switch Registers.....	17
Microcontroller Status Register.....	17
External Timer/Counter Registers	17
Internal Timer/Counter Registers.....	18
Watchdog Timer Control Register	18
UART Registers.....	18
Master SPI Registers.....	18
User SPI Registers.....	19
Instruction Set Summary	19
Arithmetic and Logic Instructions.....	19
MCU Control Instructions	20
Branch Instructions	20
Data Transfer Instructions	21
Bit and Bit Test Instructions.....	22
Conditional Branch Summary	22

Feature Overview

Available Packages

- SS-M3000-F: 160 QFP
- SS-M3000-S: 128 QFP
- SS-M3001-B: 128 BGA

Power

- 3.3 V with 5 V tolerant Inputs

CPU Block

- A high-speed RISC based Atmel AVR core running at 20 MHz
- 4K x 8 of data RAM
- 64K x 16 program memory embedded ²
- Boot code for system initialization and in-circuit FLASH programming
- JTAG port for system debug
- Watchdog timer
- Interrupt controller with 2 external interrupts
- Internal and external counter timers
- 20 general purpose I/O lines ¹
- External 4K x 8 data interface ²

Communication Block

- 2 SPI ports
- General purpose UART
- CAN controller (3 TX buffers, 7 RX masks)

General Purpose Analog Block

- 10-bit A to D converter
- 10-bit D to A converter
- Analog mux
- Operational amplifier

Motor Phase Current Control Block

- Sine/cosine generator capable of 20 different microstep resolutions
- 10-bit sine/cosine D to A converters
- 8-bit reference D to A converter
- Advanced dual H-bridge control
- Advanced phase current control with low and mid range resonance reduction

Motion Control Block

- Advanced acceleration/deceleration velocity generator capable of up to a 5MHz step clock rate
- 32-bit position and encoder counters
- 32-bit position compare register
- 32-bit high-speed position capture register
- External clock interface for following (with ratio) or providing an external clock and direction that accepts/outputs step and direction, quadrature or step up/down signals

¹ 12 I/O lines on 128 QFP package;
20 I/O lines on 160 QFP and 128 BGA packages.

² Not available in all packages.

³ 200 step/revolution motor.

Description

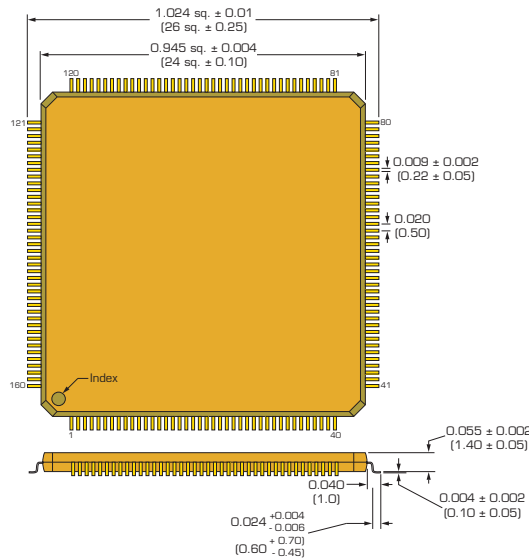
The System Semiconductor M3000 Motion Controller is a highly integrated, mixed signal system-on-a-chip. The M3000 combines all the major building blocks necessary to control and position multi-phase step motors while also working as a high-speed general purpose microcontroller incorporating extensive communication, analog and system functions.

Integration of System Semiconductor's patent-pending phase current control circuits enables motor performance to reach new limits of increased speed and smoothness while lowering audible noise and vibration. And with System Semiconductor's advanced acceleration, velocity and position control circuits virtually eliminating corresponding time critical tasks, the CPU is freed to perform other system control functions allowing system throughput rivaling high-end DSP's costing far more.

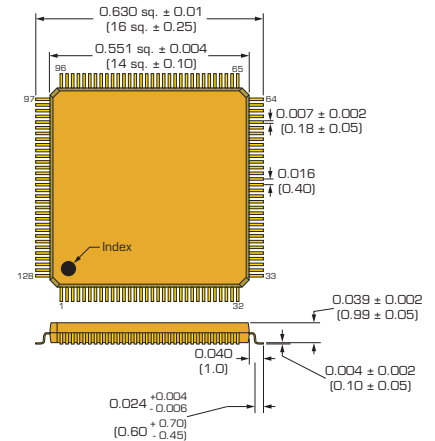
Incorporation of the M3000's extensive communication and general analog functions provides the user the capability to control a large variety of systems without additional circuits. By integrating all major system's functions into one system-on-a-chip, performance and reliability are greatly enhanced while cost and time to market are reduced. A large temperature range also makes the M3000 ideal for commercial, industrial and automotive applications.

Package Specifications SS-M3000-F (160 QFP) Top View

Dimensions in Inches (mm)



SS-M3000-S (128 QFP) Top View



SS-M3001-B (128 BGA) Bottom View

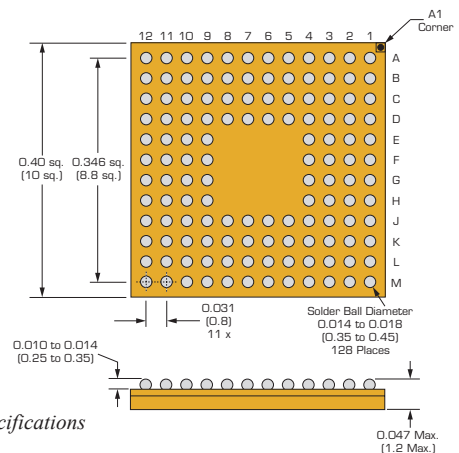


Figure 1: M3000 Mechanical Specifications

Block Diagram

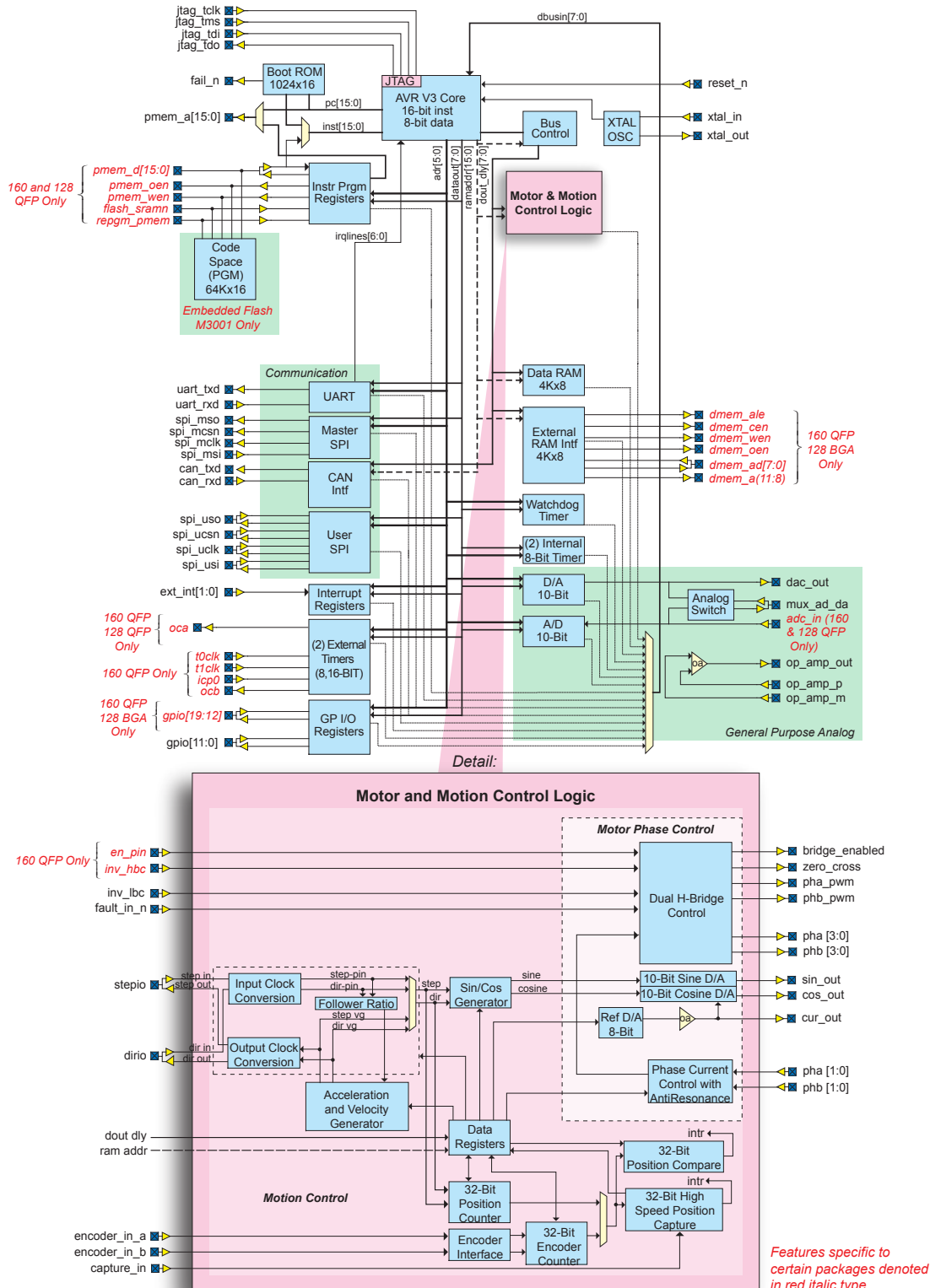


Figure 2: M3000 Block Diagram

Absolute Maximum Ratings

Absolute Maximum Ratings	
Parameter	Value
Operating Junction Temperature	-55°C to 125°C
Storage Temperature	-65°C to 150°C
Operating Ambient	
SS-M3000-F (160 QFP)	+85°C
SS-M3000-S (128 QFP)	+85°C
SS-M3001-B (128 BGA)	+85°C
Digital Input Voltage	+5.5 VDC
Analog Input Voltage	3.6 VDC
Operating Voltage (V_{dd} , AV_{dd})	+3.6 VDC

Table 1: Absolute Maximum Ratings

Thermal Characteristics

Thermal Ratings	
Package	Value
SS-M3000-F (160 QFP)	39.0 °C/W
SS-M3000-S (128 QFP)	29.0 °C/W
SS-M3001-B (128 BGA)	27.5 °C/W

Table 2: Absolute Maximum Ratings

Analog Characteristics

Analog Characteristics					
Device	Parameter	Minimum	Typical	Maximum	Unit
Motor Drive DAC	Resolution		10		bit
	Integral Linearity			±2.5	LSb
	Differential Linearity			±1.0	LSb
	Zero Offset			±2.0	LSb
	Reference Voltage	0	$V_{dd} - 0.1$		V
Motor Drive Reference DAC	Resolution		8		bit
	Integral Linearity			±2.5	LSb
	Differential Linearity			±1.0	LSb
	Zero Offset			±2.0	LSb
	Reference Voltage		V_{dd}		V
General Purpose DAC	Resolution		10		bit
	Integral Linearity			±2.5	LSb
	Differential Linearity			±1.0	LSb
	Zero Offset			±2.0	LSb
	Reference Voltage		V_{dd}		V
General Purpose ADC	Resolution		10		bit
	Integral Linearity			±2.5	LSb
	Differential Linearity			±1.0	LSb
	Zero Offset			±2.0	LSb
	Reference Voltage		V_{dd}		V

Table 3: Analog Characteristics

DC Characteristics

M3000 DC Electrical Characteristics								
Buffer	Used For	Symbol	Parameter	Test Condition	Min.	Typ.	Max	Unit
Power (PVSS, PVDD)	Power Supply	Vdd	Supply Voltage		3.0	3.3	3.6	VDC
Supply Current (Max)	M3000	Idd	Supply Current (Max)				119	mA
	M3001	Idd	Supply Current (Max)				131	mA
Input, CMOS, Schmidt, 5V Tolerant (PICSV)	All Inputs and I/O except Program Memory Data I/O	Iih	High-Level Input Current	Vin=Vdd Vdd=Vdd (Max)			10	μA
		Iil	Low-Level Input Current	Vin=Vss Vdd=Vdd (Max)	-10			μA
		Vhys	Schmidt Hysteresis			0.6		V
		Vih	High-Level Input Voltage		2.0			V
		Vil	Low-Level Input Voltage				1.2	V
Input, CMOS, 5V Tolerant (PICV)	Program Memory Data I/O	Iih	High-Level Input Current	Vin=Vdd Vdd=Vdd (Max)			10	μA
		Iil	Low-Level Input Current	Vin=Vss Vdd=Vdd (Max)	-10			μA
		Vih	High-Level Input Voltage		2.0			V
		Vil	Low-Level Input Voltage				1.2	V
Output, CMOS, 2 mA, 5V Tolerant (PO11V)	All Outputs and I/O except CANTX Output	Voh	High-Level Output Voltage	Ioh=1.7 mA Vdd=Vdd (Min)	0.7 Vdd			V
		Vol	Low-Level Output Voltage	Ioh=8mA			0.5	V
		Ios	Output Short Circuit Current	Vout=Vdd Vdd=Vdd (Max)		15		mA
				Vout=Vss Vdd=Vdd (Max)		-11		mA
Output, CMOS, 8 mA, 5V Tolerant (PO44V)	CANTX Output	Voh	High-Level Output Voltage	Ioh=8 mA Vdd=Vdd (Min)				V
		Vol	Low-Level Output Voltage	Ioh=1.4 mA			0.5	V
		Ios	Output Short Circuit Current	Vout=Vdd Vdd=Vdd (Max)		15		mA
				Vout=Vss Vdd=Vdd (Max)		-11		mA
Output	All Tri-stateable Outputs	Ioz	High Impedance State Output Current	Vin=Vdd or Vss Vdd=Vdd (Max) No Pull-Up	-10		10	μA
Oscillator (PX4L)	Oscillator Output	Ios	Output Short Circuit Current	Vout=Vdd Vdd=Vdd (Max)		45		mA
				Vout=Vss Vdd=Vdd (Max)		-42		mA
	Oscillator	Gm	Transconductance				20	mA/V
		Vb	Self Bias Voltage				1.6	V
Pull-Up (PRU1, PRUP1)	Fixed and Programmable Pull-Up and Pull-Down Resistors	Rpu	Pull-Up				20k	Ω
Pull-Down (PRD1, PRDP1)		Rpd	Pull-Down				20k	Ω
Input, Analog (PFIAMUX)	Opamp, ADC_in, MUX_AD_DA Inputs	Iih	High-Level Input Current	Vin=Vdd=			10	μA
		Iil	Low-Level Input Current	Vin=Vdd=	10			μA
		Vih	High-Level Input Voltage			Vdd		V
		Vil	Low-Level Input Voltage			0		V
Output, Analog (PFOAMUX)	DAC_out, MUX_AD_DA, SIN_OUT, COS_OUT Outputs	Voh	High-Level Output Voltage	Ioh=0		Vdd		V
		Vol	Low-Level Output Voltage	Ioh=0		0		V
		Ios	Output Short Circuit Current	Vout=Vdd		44		mA
				Vout=Vss		33		mA
Output, Analog (ascop039a)	Opamp, Cur_Out Outputs	Voh	High-Level Output Voltage				Vdd-0.1	V
		Vol	Low-Level Output Voltage		0.1			V
		Io	Output Current			3		mA

Table 4: M3000 DC Electrical Characteristics

Feature Summary by Package

Feature Summary By Package Style				
	FUNCTION	M3000F 160 QFP	M3000S 128 QFP	M3001 128 BGA
Processor Control				
	JTAG	Y	Y	Y
	IBOOT_N, RePgm_Pmem	Y	Y	Y
	FLASH vs RAM Speed	Y	Y	Y
	ResetN, XTAL, TEST	Y	Y	Y
	Fail_n	Y	Y	N
Memory (Code Space)				
	Pmem..Addr lines, Data lines, we, oe	Y	Y	N
	Memory is Embedded	N	N	Y
	Note: if N, requires external memory			
Communications				
	SPI_USER (configurable as Master or Slave)	Y	Y	Y
	SPI_Master only	Y	Y	Y
	CAN	Y	Y	Y
	UART	Y	Y	Y
Timers				
	Timer (Internal: 8bit timer0, 16bit timer1)	Y	Y	Y
	Timer (External: 8bit timer0, 16bit timer1)	Y	Y	Y
	T0clk, T1clk, Ipc0 (timer1 only)	Y	N	N
	ocA " "	Y	Y	N
	ocB " "	Y	N	N
Indexer Logic				
	Encoder_In	Y	Y	Y
	STEP_IO, DIR_IO	Y	Y	Y
	CAPTURE_IN, TRIP_Out	Y	Y	Y
	External Interrupts [0..1]	Y	Y	Y
IO Ports / Memory (Extra Data Space)				
	8 GPIO[0..7]	Y	Y	Y
	4 GPIO[8..11] / DataMem_A[8..11]	Y	Y	Y
	8 GPIO[12..19] / DataMem_AD[0..7]	Y	N	Y
	DataMem_[CEN, ALE, WEN, OEN]	Y	N	Y
Analog				
	Op_Amp [_Out, _M, _P]	Y	Y	Y
	adc_in	Y	Y	N
	Mux_ad_da	Y	Y	Y
	dac_out	Y	Y	N
Motor Bridge Driver Stage				
	PhA [LH, LL, _RH, _RL, _Fwd, _Rev]	Y	Y	Y
	PhB [LH, LL, _RH, _RL, _Fwd, _Rev]	Y	Y	Y
	BridgeEnabled	Y	Y	Y
	PhA_Pwm, PhB_Pwm	Y	Y	N
	Pwm_Osc, Mask, Sin_Sign	Y	N	N
	Zero_Cross out	Y	Y	Y
	Sin_Out, Cos_Out	Y	Y	Y
	Cur_Out	Y	Y	Y
	Pwm_Current Reference Output	Y	N	N
	dac_SDA, dac_CS_N	Y	N	N
	En_Pin	Y	N	N
	Inv_HBC	Y	N	N
	Fault_IN_N	Y	Y	Y
	Inv_LBC	Y	Y	Y

Table 5: Features by Package Style

The following tables illustrate the Motor and Motion Control Pin Assignments for the M3000 in its three different packages:

- SS-M3000-F (160 QFP - Not a stock item. Contact factory for availability.)
- SS-M3000-S (128 QFP)
- SS-M3001-B (128 BGA)

The pins are grouped by function. Table cells marked "X" indicate a feature not available on that particular package.

Pin Configuration by Package Type

Processor Control

All Packages

Processor Control Pin Functions and Assignment						
	Function	Pin Name	M3000 160 QFP Pin#	M3000 128 QFP Pin#	M3001 128 BGA Pin#	Pull-Up (PU) Pull-Down (PD) Program (PGM)
JTAG	JTAG Emulator Clock Input	JTAG_TCLK	141	113	B7	PD
	JTAG Emulator Mode Select Input	JTAG_TMS	146	117	B6	PU
	JTAG Emulator Data Input	JTAG_TDI	147	118	A6	PU
	JTAG Emulator Data Output	JTAG_TDO	142	114	A7	
	JTAG Reset Input	JTAG_TRST_N	2	2	B1	PU
XTAL	Crystal Input	XTAL_IN	99	79	G12	
	Crystal Output	XTAL_OUT	100	80	G11	
MISC	Internal Boot Input	IBOOT_N	21	17	F3	PD
	Reprogram Flash Memory Input	REPGM_PMEM	28	23	H1	PD
	Program Memory Type Input: Flash=1/SRAM=0	FLASH_SRAM_N	27	22	G4	PU
	Master Reset Input	RESET_N	31	25	H3	PU
	Test Control Input	TEST	24	20	G2	PD
	Fail Boot Test Output and Serial DAC Clock Output	FAIL_N/DAC_CLK	23	19	X	

Table 6: Processor Control Pin Functions and Assignment

Communications

All Packages

Communications Pin Functions and Assignment						
	Function	Pin Name	M3000 160 QFP Pin#	M3000 128 QFP Pin#	M3001 128 BGA Pin#	Pull-Up (PU) Pull-Down (PD) Program (PGM)
USER SPI	SPI User Clock Output I/O (Master or Slave)	SPI_UCLK	103	83	F12	PU
	SPI User Chip Select Output I/O (Master or Slave)	SPI_UCSN	102	82	G9	PU
	SPI User Serial In I/O (Master or Slave) (MOSI)	SPI_USI	94	75	H12	PU
	SPI User Serial Out I/O (Master or Slave) (MISO)	SPI_USO	95	76	H11	PU
MASTER SPI	SPI Master Clock Output	SPI_MCLK	98	78	H9	
	SPI Master Chip Select Output	SPI_MCSN	90	72	J12	
	SPI Master Serial Input	SPI_MSI	91	73	J11	PU
	SPI Master Serial Output	SPI_MSO	93	74	J10	
CAN	CAN Transmit Data Output	CAN_TXD	107	86	F9	
	CAN Receive Data Input	CAN_RXD	112	90	E9	PU
UART	UART Transmit Data Output	UART_TXD	104	84	F11	
	UART Receive Data Output	UART_RXD	106	85	F10	PU

Table 7: Communications Pin Functions and Assignment

Pin Configuration by Package Type

Memory (Code/Program Space)

M3000 128 and 160 QFP

Memory (Code/Program Space) Pin Functions and Assignment				
	Function	Pin Name	M3000 160 QFP Pin#	M3000 128 QFP Pin#
PROGRAM MEMORY ADDRESS LINES	Program Memory SRAM/FLASH Address Bus A0 Output	PMEM_A0	86	69
	Program Memory SRAM/FLASH Address Bus A1 Output	PMEM_A1	76	61
	Program Memory SRAM/FLASH Address Bus A2 Output	PMEM_A2	71	57
	Program Memory SRAM/FLASH Address Bus A3 Output	PMEM_A3	85	68
	Program Memory SRAM/FLASH Address Bus A4 Output	PMEM_A4	83	67
	Program Memory SRAM/FLASH Address Bus A5 Output	PMEM_A5	78	62
	Program Memory SRAM/FLASH Address Bus A6 Output	PMEM_A6	72	58
	Program Memory SRAM/FLASH Address Bus A7 Output	PMEM_A7	67	54
	Program Memory SRAM/FLASH Address Bus A8 Output	PMEM_A8	62	50
	Program Memory SRAM/FLASH Address Bus A9 Output	PMEM_A9	58	46
	Program Memory SRAM/FLASH Address Bus A10 Output	PMEM_A10	53	42
	Program Memory SRAM/FLASH Address Bus A11 Output	PMEM_A11	49	39
	Program Memory SRAM/FLASH Address Bus A12 Output	PMEM_A12	46	37
	Program Memory SRAM/FLASH Address Bus A13 Output	PMEM_A13	45	36
	Program Memory SRAM/FLASH Address Bus A14 Output	PMEM_A14	47	38
	Program Memory SRAM/FLASH Address Bus A15 Output	PMEM_A15	43	35
PROGRAM MEMORY DATA LINES	Program Memory SRAM/FLASH Data Bus D0 I/O	PMEM_D0	87	70
	Program Memory SRAM/FLASH Data Bus D1 I/O	PMEM_D1	89	71
	Program Memory SRAM/FLASH Data Bus D2 I/O	PMEM_D2	79	63
	Program Memory SRAM/FLASH Data Bus D3 I/O	PMEM_D3	75	60
	Program Memory SRAM/FLASH Data Bus D4 I/O	PMEM_D4	66	53
	Program Memory SRAM/FLASH Data Bus D5 I/O	PMEM_D5	70	56
	Program Memory SRAM/FLASH Data Bus D6 I/O	PMEM_D6	74	59
	Program Memory SRAM/FLASH Data Bus D7 I/O	PMEM_D7	68	55
	Program Memory SRAM/FLASH Data Bus D8 I/O	PMEM_D8	63	51
	Program Memory SRAM/FLASH Data Bus D9 I/O	PMEM_D9	59	47
	Program Memory SRAM/FLASH Data Bus D10 I/O	PMEM_D10	54	43
	Program Memory SRAM/FLASH Data Bus D11 I/O	PMEM_D11	64	52
	Program Memory SRAM/FLASH Data Bus D12 I/O	PMEM_D12	60	48
	Program Memory SRAM/FLASH Data Bus D13 I/O	PMEM_D13	55	44
	Program Memory SRAM/FLASH Data Bus D14 I/O	PMEM_D14	50	40
	Program Memory SRAM/FLASH Data Bus D15 I/O	PMEM_D15	51	41
CTRL	Program Memory SRAM/FLASH Write Enable Output	PMEM_WEN	42	34
	Program Memory SRAM/FLASH Output Enable Output	PMEM_OEN	82	66

Table 8: Memory (Code/Program Space) Pin Functions and Assignment - M3000 160 and 128 QFP

Memory (Code/Program Space)

M3001 128 BGA

Pin Configuration by Package Type

Memory (Code/Program Space) Pin Functions and Assignment		
Function	Pin Name	M3001 128 BGA Pin #
Program Memory SRAM/FLASH Chip Enable	PMEM_CEN	L11
FACTORY USE ONLY!	TA0	L12
	TA1	L9
	TA2	L8
	TA3	M12
	TA4	M11
	TA5	M9
	TA6	M8
	TA7	M7
	TA8	M6
	TA9	M5
	TA10	M4
	TD0	K12
	TD1	K11
	TD2	K10
	TD3	K9
	TD4	L7
	TD5	K8
	TD6	J9
	TD7	J8
	TD8	J7
	TD9	J6
	TD10	J5
	TD11	K7
	TD12	K6
	TD13	K5
	TD14	K4
	TD15	L4



WARNING!
Ball L11 - Chip Enable **MUST** be connected to Ground for the M3001 to function.

Table 9: Memory (Code/Program Space) Pin Functions and Assignment - M3001

Pin Configuration by Package Type

External Timer

All Packages

External Timer Pin Functions and Assignment						
	Function	Pin Name	M3000 160 QFP Pin#	M3000 128 QFP Pin#	M3001 128 BGA Pin#	Pull-Up (PU) Pull-Down (PD) Program (PGM)
TIMER	Timer T/C0 Clock Input	T0CLK	105	X	X	PU
	Timer T/C 1 Clock Input	T1CLK	109	X	X	PU
	Timer 0 Capture Input	ICP0	113	X	X	PU
	Timer A Compare Output	OCA	26	21	X	
	Timer B Compare Output	OCB	117	X	X	

Indexer Logic

All Packages

Indexer Logic Pin Functions and Assignment						
	Function	Pin Name	M3000 160 QFP Pin#	M3000 128 QFP Pin#	M3001 128 BGA Pin#	Pull-Up (PU) Pull-Down (PD) Program (PGM)
ENCODER	Encoder Channel A Input	ENC_IN_A	134	107	D8	PU
	Encoder Channel B Input	ENC_IN_B	139	111	D7	PU
	Encoder Index Input	ENC_IN_IDX	143	115	D6	PU
LOGIC I/O	Capture Input	CAPTURE_IN	131	105	B9	PU
	Trip Output	TRIP_OUT	133	106	A9	
	Step Clock I/O (or Step-up, or CH A)	STEP_IO	137	109	B8	PU
	Direction I/O (or Step-down, or CH B)	DIR_IO	138	110	A8	PU
INT	External Interrupt Input 0 (Programmable Polarity)	EXT_INT0	39	31	K1	PU
	External Interrupt Input 1 (Programmable Polarity)	EXT_INT1	38	30	J4	PU

Table 11: Indexer Logic Pin Functions and Assignment

Analog

All Packages

Analog Pin Functions and Assignment						
	Function	Pin Name	M3000 160 QFP Pin#	M3000 128 QFP Pin#	M3001 128 BGA Pin#	Pull-Up (PU) Pull-Down (PD) Program (PGM)
OP-AMP 0...7	General Purpose Op-Amp Output	OP_AMP_OUT	5	4	C1	
	General Purpose Op-Amp Minus Input	OP_AMP_M	8	6	C3	
	General Purpose Op-Amp Plus Input	OP_AMP_P	9	7	D1	
MISC	General Purpose ADC Input	ADC_IN	10	8	X	
	ADC Input or DAC Output	MUX_AD_DA	11	9	D3	
	General Purpose DAC Output	DAC_OUT	14	12	X	

Table 11: Analog Pin Functions and Assignment

I/O Ports/Memory

All Packages

Pin Configuration by
Package Type

97I/O Ports/Memory (Extra Data Space) Pin Functions and Assignment						
	Function	Pin Name	M3000 160 QFP Pin#	M3000 128 QFP Pin#	M3001 128 BGA Pin#	Pull-Up (PU) Pull-Down (PD) Program (PGM)
8 GPIO 0...7	Gen. Purpose I/O 0	GPIO0	36	29	J3	PU, PGM
	Gen. Purpose I/O 1	GPIO1	35	28	J2	PU, PGM
	Gen. Purpose I/O 2	GPIO2	34	27	J1	PU, PGM
	Gen. Purpose I/O 3	GPIO3	32	26	H4	PU, PGM
	Gen. Purpose I/O 4	GPIO4	119	95	C12	PU, PGM
	Gen. Purpose I/O 5	GPIO5	118	94	D9	PU, PGM
	Gen. Purpose I/O 6	GPIO6	116	93	D10	PU, PGM
	Gen. Purpose I/O 7	GPIO7	115	92	D11	PU, PGM
GPIO/DATA MEM 8...11	Gen. Purpose I/O 8/Data Memory Address 8	GPIO8/DMEM_A8	114	91	D12	PU, PGM
	Gen. Purpose I/O 9/Data Memory Address 9	GPIO9/DMEM_A9	111	89	E10	PU, PGM
	Gen. Purpose I/O 10/Data Memory Address 10	GPIO10/DMEM_A10	110	88	E11	PU, PGM
	Gen. Purpose I/O 11/Data Memory Address 11	GPIO11/DMEM_A11	108	87	E12	PU, PGM
GPIO 12...19/ DATA MEM 0...8	Gen. Purpose I/O 12/Data Memory Address 0	GPIO12/DMEM_A0	44	X	L1	PU, PGM
	Gen. Purpose I/O 13/Data Memory Address 1	GPIO13/DMEM_A1	48	X	L2	PU, PGM
	Gen. Purpose I/O 14/Data Memory Address 2	GPIO14/DMEM_A2	52	X	M1	PU, PGM
	Gen. Purpose I/O 15/Data Memory Address 3	GPIO15/DMEM_A3	56	X	M2	PU, PGM
	Gen. Purpose I/O 16/Data Memory Address 4	GPIO16/DMEM_A4	65	X	L3	PU, PGM
	Gen. Purpose I/O 17/Data Memory Address 5	GPIO17/DMEM_A5	69	X	M3	PU, PGM
	Gen. Purpose I/O 18/Data Memory Address 6	GPIO18/DMEM_A6	73	X	G3	PU, PGM
	Gen. Purpose I/O 19/Data Memory Address 7	GPIO19/DMEM_A7	77	X	G1	PU, PGM
DATA MEM CTRL	Data Memory Chip Enable	DMEM_CEN	37	X	A5	
	Data Memory Address Latch Enable Output	DMEM_ALE	84	X	E2	
	Data Memory Write Enable Output	DMEM_WEN	88	X	D2	
	Data Memory Output Enable Output	DMEM_OEN	92	X	A10	

Table 12: I/O Ports/Memory (Extra Data Space) Pin Functions and Assignment

Pin Configuration by Package Type

Motor Bridge Drive Stage

All Packages

Motor Bridge Drive Stage Pin Functions and Assignment						
	Function	Pin Name	M3000 160 QFP Pin #	M3000 128 QFP Pin #	M3001 128 BGA Pin #	Pull-Up (PU) Pull-Down (PD) Program (PGM)
PHASE A CONTROL	Bridge Control Phase A Left High Output	PHA_LH	122	98	B12	
	Bridge Control Phase A Left Low Output	PHA_LL	123	99	B11	
	Bridge Control Phase A Right High Output	PHA_RH	126	101	A11	
	Bridge Control Phase A Right Low Output	PHA_RL	125	100	A12	
	Bridge Control Phase A Reverse Input	PHA_REV	135	108	C8	PU
	Bridge Control Phase A Forward Input	PHA_FWD	130	104	C9	PU
PHASE B CONTROL	Bridge Control Phase B Left High Output	PHB_LH	156	125	A4	
	Bridge Control Phase B Left Low Output	PHB_LL	159	127	A3	
	Bridge Control Phase B Right High Output	PHB_RH	158	126	B3	
	Bridge Control Phase B Right Low Output	PHB_RL	155	124	B4	
	Bridge Control Phase B Reverse Input	PHB_REV	150	120	C5	PU
	Bridge Control Phase B Forward Input	PHB_FWD	154	123	C4	PU
BRIDGE CONTROL	Bridge Enable Output	BRDG_EN	151	121	B5	
	Bridge Enable Input	EN_PIN	136	X	X	PU
	Invert High Bridge Control Input	INV_HBC	128	X	X	PD
	Invert Low Bridge Control Input	INV_LBC	127	102	B10	PD
PWM	Bridge Control Phase A PWM Output	PHA_PWM	129	103	X	
	Bridge Control Phase B PWM Output	PHB_PWM	152	122	X	
	PWM Oscillator Output	PWM_OSC	29	X	X	
	PWM Current Reference Output	PWM_CUR	132	X	X	
MISC	Zero Crossing Output	ZERO_CROSS	148	119	D5	
	Mask Output	MASK	25	X	X	
	Fault Input	FAULT_IN_N	30	24	H2	PU
	Sine Sign Output	SIN_SIGN	33	X	X	
DAC	Serial DAC Chip Select Output	DAC_CS_N	18	X	X	
	Serial DAC Data Output	DAC_SDA	19	X	X	
	DAC Sine Output	SIN_OUT	17	15	F1	
	DAC Cosine Output	COS_OUT	16	14	E4	
	Current Reference (Reference DAC Output)	CUR_OUT	7	5	C2	

Table 13: Motor Bridge Driver Stage Pin Functions and Assignment

Power and Ground

All Packages

Pin Configuration by Package Type

Power and Ground Pin Functions and Assignment					
	Function	Pin Name	M3000 160 QFP Pin#	M3000 128 QFP Pin#	M3001 128 BGA Pin#
DIGITAL POWER	Digital Power	VDD	22	18	F4
			41	33	K3
			61	49	L6
			81	65	M10
			101	81	G10
			121	97	C10
			144	116	C6
			145	X	X
ANALOG POWER	Analog Power	AVDD	3	3	B2
			15	13	E3
DIGITAL GROUND	Digital Ground	GND	96	77	C7
			140	112	H10
			20	16	F2
			40	32	K2
			57	45	L5
			80	64	L10
			120	96	C11
			160	128	A2
ANALOG GROUND	Analog Ground	AGND	97	X	X
			1	1	A1
			12	10	D4
			13	11	E1

Table 14: Power and Ground Pin Functions and Assignment

Register Summary

General Purpose I/O Registers

The General Purpose I/O consists of 9 registers that drive the 12 + 8* GPI/O pins. The registers consist of three sets of the following registers: a data-direction register, a data (output) register, and a pin (input) register. Each set of three registers provides programmability for the corresponding 4 or 2x8 GPI/O pins.

General Purpose I/O Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x1F (0x3F)	AGPPORT	General Purpose I/O Data Register A	1	R/W	6-1
0x1E (0x3E)	AGPDDR	General Purpose I/O Data Direction Register A	1	R/W	6-1
0x1D (0x3D)	AGPPIN	General Purpose I/O Input Pins Register A	1	R	6-1
0x1C (0x3C)	BGPPORT	General Purpose I/O Data Register B	1	R/W	6-2
0x1B (0x3B)	BGPDDR	General Purpose I/O Data Direction Register B	1	R/W	6-2
0x1A (0x3A)	BGPPIN	General Purpose I/O Input Pins Register B	1	R/W	6-3
0x32 (0x52)	CGPPORT	General Purpose I/O Data Register C	1	R/W	6-3
0x31 (0x51)	CGPDDR	General Purpose I/O Data Direction Register C	1	R/W	6-3
0x30 (0x50)	CGPPIN	General Purpose I/O Input Pins Register C	1	R	6-3

Table 15: General Purpose I/O Registers

Motor and Motion Control Registers

The motor and motion control registers control the M3000 Motion block including PWM, Run/Hold current, Velocity, Index and DAC and clock functions.

Motor and Motion Control Registers					
RAM Address	Name	Function	Bytes	Read/Write	Page
PWM Registers					
0x0200	PWMSK	PWM Mask	1	R/W	7-18
0x0201	PWMPER	PWM Percent	1	R/W	7-18
0x0202	PWMSFRQ	PWM Frequency	1	R/W	7-18
0x0203	PWMCTL	PWM Control	1	R/W	7-19
Current Registers					
0x0204	CURIRUN	Run Current	1	R/W	7-19
0x0205	CURIRED	Current Reduction	1	R/W	7-20
0x0206 - 0x0207	CURRDLY	Current Reduction Delay	2	R/W	7-20
Velocity Registers					
0x0208 - 0x020A	VELLOW	Initial Low Velocity	3	R/W	7-20
0x020B - 0x020D	VELHI	Terminal High Velocity	3	R/W	7-21
0x020E - 0x0210	VELDEC	Velocity Deceleration	3	R/W	7-21
0x0211 - 0x0213	VELACC	Velocity Acceleration	3	R/W	7-21
0x0214 - 0x0216	VELCVEL	Current Velocity	3	R	7-22
0x0217 - 0x0219	VELTVEL	Trip Velocity	3	R/W	7-22
0x021A	VELVGCTL	Velocity Generator Control	1	R/W	7-23
0x021B	VELSTB	Velocity Strobe	1	W	7-23
0x021C	VELIFLG	Velocity Interrupt Flag	1	R/W	7-24
0x021D	VELIMSK	Velocity Interrupt Mask	1	R/W	7-24
Index Registers					
0x021E - 0x0221	IDXTRT	Index Trip Target	4	R/W	7-25
0x0222 - 0x0225	IDXENT	Index End Target	4	R/W	7-25
0x0226 - 0x0227	IDXMSDT	Index Motor Settling Delay Time	2	R/W	7-26
0x0228 - 0x022B	IDXPOT	Index Position Target	4	R/W	7-26
0x022C - 0x022F	IDXPOS	Index Position Count	4	R/W	7-27

Table 16: Motor and Motion Control Registers I

Register Summary

Motor and Motion Control Registers					
RAM Address	Name	Function	Bytes	Read/Write	Page
Index Registers cont'd					
0x0230 - 0x0233	IDXENC	Index Encoder Count	4	R/W	7-27
0x0234	IDXCTRL	Index Control	1	R/W	7-28
0x0235	IDXSTRB	Index Strobe	1	W	7-29
0x0236 - 0x0239	IDXCPTP	Index Capture Position	4	R	7-30
0x023A	IDXIFLG	Index Interrupt Flag	1	R/W	7-30
0x023B	IDXIMSK	Index Interrupt Mask	1	R/W	7-31
Step Clock Registers					
0x23C	SCIO	Step Clock I/O	1	R/W	7-32
0x23D	SCSW	Step Clock Step Width	1	R/W	7-33
0x23E - 0x241	SCRFB	Step Clock Ratio Factor	4	R/W	7-33
Miscellaneous Registers					
0x242	IOF	Input/Output Filter	1	R/W	7-34
0x243	MSELR	Microstep/Step Select Register	1	R/W	7-35
0x244	STAT	Status	1	R	7-36
0x245	SPWMCTL	Safety, PWM Control	1	R	7-36
Motor Phase Control					
0x285	DACCTRL	D/A Converter Control	1	R/W	7-38
0x280	SINDACL	Sine D/A Converter Low Bits	1	R/W	7-38
0x281	SINDACH	Sine D/A Converter High Bits	1	R/W	7-38
0x282	COSDACL	Cosine D/A Converter Low Bits	1	R/W	7-39
0x283	COSDACH	Cosine D/A Converter High Bits	1	R/W	7-39
0x284	GAINDAC	D/A Converter Gain	1	R/W	7-39

Table 17: Motor and Motion Control Registers II

Interrupt Registers

Several of the peripherals use interrupts to inform the AVR of completion of an operation and the System Semiconductor Motion Controller has two pins for external interrupt generation.

Interrupt Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x17 (0x37)	GIMSK	General Interrupt Mask	1	R/W	8-3
0x16 (0x36)	GIFR	General Interrupt Flag	1	R/W	8-4
0x2B (0x4B)	EXTIMSK	External Timer/Counter Interrupt Mask	1	R/W	8-5
0x2A (0x4A)	EXTIFR	External Timer/Counter Interrupt Flag	1	R/W	8-5
0x80B	INTIMSK	Internal Timer/Counter Interrupt Mask	1	R/W	8-6
0x80A	INTIFR	Internal Timer/Counter Interrupt Flag	1	R/W	8-6

Table 18: Interrupt Registers

Instruction Memory Programming Registers

The following registers control the instruction program memory and data bus.

Instruction Memory Programming Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x04 (0x24)	IPCR	Instruction Program Control	1	R/W	9-14
0x03-0x02 (0x23-0x22)	IPAH/L	Instruction Program Address High/Low	2	R/W	9-14
0x01-0x00 (0x21-0x20)	IPDH/L	Instruction Program Data High/Low	2	R/W	9-15

Table 19: Instruction Memory Programming Registers

Register Summary

CAN Controller Registers

All CAN Registers are mapped into the AVR processors Data Space and are accessible via ordinary memory access instructions.

CAN Controller Registers					
RAM Address	Name	Function	Bytes	Read/Write	Page
BAUD Rate					
0x0100	CDIVCAN	CAN Enable and Clock Prescale	1	R/W	10-9
0x0101-0x0103	CBTR	CAN Bus Timing Register 0, 1, 2	3	R/W	10-9, 10
Control and Enable					
0x0104	CMCR	Can Module Control Register	1	R/W	10-11
0x0105	CRAFEN	CAN Receiver Acceptance Filter Enable	1	R/W	10-12
0x0106	CTARR	CAN Transmit Abort Request Register	1	R/W	10-12
Interrupt, Flag and Status					
0x0107	CIER	CAN Interrupt Enable Register	1	R/W	10-13
0x0108	CCFLG	CAN Communications Flag Register	1	R/W	10-14
0x0109	CCISR	CAN Communications Interrupt Status Register	1	R	10-15
0x010A	CIDAH0	CAN Identifier Acceptance Hit 0 Register	1	R/W	10-16
0x010B	CIDAH1	CAN Identifier Acceptance Hit 1 Register	1	R/W	10-16
Error Specific and Version					
0x010C	CEFR	CAN Error Flag Register	1	R	10-17
0x010D	CRXERR	CAN Receive Error Counter	1	R	10-19
0x010E	CTXERR	CAN Transmit Error Counter	1	R	10-19
0x010F	CVER	CAN Hardware Version	1	R	10-19
RX (7 Code and Mask Registers)					
0x0110-0x0113	CIDAC0R	CAN Identifier Acceptance Code 0 Register	4	R/W	10-20
0x0114-0x0117	CIDM0R	CAN Identifier Mask 0 Register	4	R/W	10-20
0x0118-0x011B	CIDAC1R	CAN Identifier Acceptance Code 1 Register	4	R/W	10-20
0x011C-0x011F	CIDM1R	CAN Identifier Mask 1 Register	4	R/W	10-20
0x0120-0x0123	CIDAC2R	CAN Identifier Acceptance Code 2 Register	4	R/W	10-20
0x0124-0x0127	CIDM2R	CAN Identifier Mask 2 Register	4	R/W	10-20
0x0128-0x012B	CIDAC3R	CAN Identifier Acceptance Code 3 Register	4	R/W	10-20
0x012C-0x012F	CIDM3R	CAN Identifier Mask 3 Register	4	R/W	10-20
0x0130-0x0133	CIDAC4R	CAN Identifier Acceptance Code 4 Register	4	R/W	10-20
0x0134-0x0137	CIDM4R	CAN Identifier Mask 4 Register	4	R/W	10-20
0x0138-0x013B	CIDAC5R	CAN Identifier Acceptance Code 5 Register	4	R/W	10-20
0x013C-0x013F	CIDM5R	CAN Identifier Mask 5 Register	4	R/W	10-20
0x0140-0x0143	CIDAC6R	CAN Identifier Acceptance Code 6 Register	4	R/W	10-20
0x0144-0x0147	CIDM6R	CAN Identifier Mask 6 Register	4	R/W	10-20
3 TX and 2 RX Buffers					
0x0150-0x015F	CTXB0	CAN Transmit Buffer 0	16	R/W	10-22
0x0160-0x016F	CTXB1	CAN Transmit Buffer 2	16	R/W	10-22
0x0170-0x017F	CTXB2	CAN Transmit Buffer 2	16	R/W	10-22
0x0180-0x018F	CRXB0	CAN Receive Buffer 0	16	R/W	10-22
0x0190-0x019F	CRXB1	CAN Receive Buffer 1	16	R/W	10-22

Table 20: CAN Controller Registers

ADC Registers

The ADC registers control the general purpose 10-bit analog to digital conversion.

Register Summary

ADC Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x07 (0x27)	ADCSR	ADC Control and Status	1	R-R/W	11-2
0x06 (0x26)-0x05 (0x25)	ADRS1THI/LO	ADC Result High/Low	2	R	11-2

Table 21: ADC Registers

DAC Registers

The following registers control the General Purpose D/A interface, a 10-bit Cascaded Potentiometric Digital to Analog Converter.

DAC Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x19 (0x39)-0x18 (0x38)	DACVALHI/LO	DAC Conversion High Byte/Low Byte	2	R-R/W	12-1

Table 22: DAC Registers

Analog Switch Registers

An analog switch is provided to switch a single pin on the M3000 between being an analog input for the General Purpose A/D converter and being an output from the General Purpose D/A converter under the control of an I/O register.

Analog Switch Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x0B (0x2B)	AMUXCTL	Analog MUX Control	1	R/W	13-1

Table 23: Analog Switch Registers

Microcontroller Status Register

The Micro Controller Status Register monitors several fault and reset conditions on the M3000.

Microcontroller Status Register					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x33 (0x53)	MCSR	Microcontroller Status Register	1	R-R/W	16-1

Table 24: Microcontroller Status Register

External Timer/Counter Registers

These registers control the external Timer/Counters are supplied with the M3000.

External Timer/Counter Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x2D (0x4D)	EXTCCR0	External Timer/Counter 0 Control Register	1	R/W	17-5
0x2C (0x4C)	EXTCNT	External Timer/Counter 0	1	R/W	17-5
0x20 (0x40)-0x21 (0x41)	EXTCCR1A/B	External Timer/Counter 1 Control Register A/B	2	R/W	17-6
0x23 (0x43)-0x22 (0x42)	EXTCNT1H/L	External Timer/Counter 1 Register High Byte/Low Byte	2	R/W	17-8
0x25 (0x45)-0x24 (0x44)	EXOCR1AH/L	External Timer/Counter 1 Output Compare Register A High Byte/Low Byte	2	R/W	17-8
0x27 (0x47)-0x26 (0x46)	EXOCR1BH/L	External Timer/Counter 1 Output Compare Register B High Byte/Low Byte	2	R/W	17-9

Table 25: External Timer/Counter Registers

Register Summary

Internal Timer/Counter Registers

These registers control the internal Timer/Counters supplied with the M3000.

Internal Timer/Counter Registers					
RAM Address	Name	Function	Bytes	Read/Write	Page
0x809	INTCCR0	Internal Timer/Counter 0 Control Register	1	R/W	17-10
0x808	INTCNT	Internal Timer/Counter 0	1	R/W	17-10
0x800-0x801	INTCCR1A/B	Internal Timer/Counter 1 Control Register A/B	2	R/W	17-11
0x803-0x802	INTCNT1H/L	Internal Timer/Counter 1 Register High Byte/Low Byte	2	R/W	17-13
0x805-0x804	INOCR1AH/L	Internal Timer/Counter 1 Output Compare Register A High Byte/Low Byte	2	R/W	17-13
0x808-0x807	INOCR1BH/L	Internal Timer/Counter 1 Output Compare Register B High Byte/Low Byte	2	R/W	17-14

Table 26: Internal Timer/Counter Registers

Watchdog Timer Control Register

The Watchdog Timer generates a time-out signal if it has not been reset after a certain number of clock cycles.

Watchdog Timer Control Register					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x0F (0x2F)	WDTCR	Watchdog Timer Control Register	1	R/W	18-3

Table 27: Watchdog Timer Control Register

UART Registers

The following registers control the Universal Asynchronous serial Receiver and Transmitter (UART)

UART Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x15 (0x35)-0x14 (0x34)	UBRRHI/LO	UART BAUD Rate High/Low	2	R/W	19-14
0x13 (0x33)-0x12 (0x32)	UCRB/A	UART Control Register B/A	2	R/W	19-15
0x11 (0x31)	USR	UART Status Register	1	R	19-17

Table 28: UART Registers

Master SPI Registers

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the M3000 and peripheral devices, or between several M3000 devices.

Master SPI Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x0E (0x2E)	MSPDR	Master SPI Data Register	1	R/W	20-5
0x0D (0x2D)	MSPSR	Master SPI Status Register	1	R	20-5
0x0C (0x2C)	MSPCR	Master SPI Control Register	1	R/W	20-6

Table 29: Master SPI Registers

User SPI Registers

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the M3000 and peripheral devices, or between several M3000 devices.

Register Summary

User SPI Registers					
I/O (SRAM) Address	Name	Function	Bytes	Read/Write	Page
0x0E (0x2E)	USPDR	User SPI Data Register	1	R/W	20-7
0x0D (0x2D)	USPSR	User SPI Status Register	1	R	20-7
0x0C (0x2C)	USPCR	User SPI Control Register	1	R/W	20-7

Table 30: User SPI Registers

Arithmetic and Logic Instructions

Instruction Set Summary

Arithmetic and Logic Instructions						
	Mnemonics	Operands	Description	Operation	Flags	# Clock Note
ADD	ADD	Rd, Rr	Add without Carry	$Rd \leftarrow Rd + Rr$	Z,C,N,V,S,H	1
	ADC	Rd, Rr	Add With Carry	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,S,H	1
	ADIW	Rd, K	Add Immediate to Word	$Rd + 1:Rd \leftarrow Rd + 1:Rd + K$	Z,C,N,V,S	2
SUBTRACT	SUB	Rd, Rr	Subtract without Carry	$Rd \leftarrow Rd - Rr$	Z,C,N,V,S,H	1
	SUBI	Rd, K	Subtract Immediate	$Rd \leftarrow Rd - K$	Z,C,N,V,S,H	1
	SBC	Rd, Rr	Subtract with Carry	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,S,H	1
	SBCI	Rd, K	Subtract Immediate with Carry	$Rd \leftarrow Rd - K - C$	Z,C,N,V,S,H	1
	SBIW	Rd, K	Subtract Immediate from Word	$Rd + 1:Rd \leftarrow Rd + 1:Rd - K$	Z,C,N,V,S	2
AND	AND	Rd, Rr	Logical AND	$Rd \leftarrow Rd \cdot Rr$	Z,N,V,S	1
	ANDI	Rd, K	Logical AND with Immediate	$Rd \leftarrow Rd \cdot K$	Z,N,V,S	1
OR	OR	Rd, Rr	Logical OR	$Rd \leftarrow Rd \vee Rr$	Z,N,V,S	1
	ORI	Rd, K	Logical OR with Immediate	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
	EOR	Rd, Rr	Exclusive OR	$Rd \leftarrow Rd \oplus Rr$	Z,N,V,S	1
MISCELLANEOUS	COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V,S	1
	NEG	Rd	Two's Complement	$Rd \leftarrow 0x00 - Rd$	Z,C,N,V,S,H	1
	SBR	Rd, K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V,S	1
	CBR	Rd, K	Clear Bit(s) in Register	$Rd \leftarrow Rd \cdot [0xFF - K]$	Z,N,V,S	1
	INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V,S	1
	DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V,S	1
	TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \cdot Rd$	Z,N,V,S	1
	CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V,S	1
	SER	Rd	Set Register	$Rd \leftarrow 0xFF$	None	1
MULTIPLY	MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr [UU]$	Z,C	2
	MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr [SS]$	Z,C	2
	MULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr [SU]$	Z,C	2
	FMUL	Rd, Rr	Fractional Multiply Unsigned	$R1:R0 \leftarrow [Rd \times Rr] < 1 [UU]$	Z,C	2
	FMULS	Rd, Rr	Fractional Multiply Signed	$R1:R0 \leftarrow Rd \times Rr < 1 [SS]$	Z,C	2
	FMULSU	Rd, Rr	Multiply Signed with Unsigned	$R1:R0 \leftarrow Rd \times Rr < 1 [SU]$	Z,C	2

Table 31: Arithmetic and Logic Instructions

Instruction Set Summary

MCU Control Instructions

MCU Control Instructions					
Mnemonics	Operands	Description	Operation	Flags	# Clock Note
BREAK	—	Break	(See Specific Description for BREAK)	None	1
NOP	—	No Operation		None	1
SLEEP	—	Sleep	(See Specific Description for SLEEP)	None	1
WDR	—	Watchdog Reset	(See Specific Description for WDR)	None	1

Table 32: MCU Control Instructions

Branch Instructions

Branch Instructions						
	Mnemonics	Operands	Description	Operation	Flags	# Clock Note
JUMP	RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
	IJMP		Indirect Jump to (Z)	$PC(15:0) \leftarrow Z, PC(21:16) \leftarrow 0$	None	2
	EIJMP		Extended Indirect Jump to (Z)	$PC(15:0) \leftarrow Z, PC(21:16) \leftarrow \text{FIND}$	None	2
	JMP	k	Jump	$PC \leftarrow k$	None	2
CALL	RCALL	k	Relative Call Subroutine	$PC \leftarrow PC + k + 1$	None	3/4 ⁽¹⁾
	ICALL		Indirect Call to (Z)	$PC(15:0) \leftarrow Z, PC(21:16) \leftarrow 0$	None	3/4 ⁽¹⁾
	EICALL		Extended Indirect Call to (Z)	$PC(15:0) \leftarrow Z, PC(21:16) \leftarrow \text{FIND}$	None	4 ⁽¹⁾
	CALL	k	Call Subroutine	$PC \leftarrow k$	None	4/5 ⁽¹⁾
	RET		Subroutine Return	$PC \leftarrow \text{STACK}$	None	4/5 ⁽¹⁾
	RETI		Interrupt Return	$PC \leftarrow \text{STACK}$	I	4/5 ⁽¹⁾
COMPARE	CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1/2/3
	CP	Rd,Rr	Compare	$Rd - Rr$	Z,C,N,V,S,H	1
	CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z,C,N,V,S,H	1
	CPI	Rd,k	Compare with Immediate	$Rd - K$	Z,C,N,V,S,H	1
SKIP	SBRC	Rd,b	Skip if Bit in Register Cleared	if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
	SBRs	Rd,b	Skip if Bit in Register Set	if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
	SBIC	A, b	Skip if Bit in I/O Register Cleared	if(I/O(A,b)=0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
	SBIS	A, b	Skip if Bit in I/O Register Set	if(I/O(A,b)=1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRANCH	BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
	BREQ	k	Branch if Equal	if (Z = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1/2
	BRCS	k	Branch if Carry Set	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRCC	k	Branch if Carry Cleared	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
	BRSH	k	Branch if Same or Higher	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
	BRLO	k	Branch if Lower	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRMI	k	Branch if Minus	if (N = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRPL	k	Branch if Plus	if (N = 0) then $PC \leftarrow PC + k + 1$	None	1/2
	BRGE	k	Branch if Greater or Equal, Signed	if (N ∨ V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
	BRLT	k	Branch if Less Than, Signed	if (N ∨ V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then $PC \leftarrow PC + k + 1$	None	1/2
	BRTS	k	Branch if T Flag Set	if (T = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRTC	k	Branch if T Flag Cleared	if (T = 0) then $PC \leftarrow PC + k + 1$	None	1/2
	BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
	BRIE	k	Branch if Interrupt Enabled	if (I = 1) then $PC \leftarrow PC + k + 1$	None	1/2
	BRID	k	Branch if Interrupt Disabled	if (I = 0) then $PC \leftarrow PC + k + 1$	None	1/2

Table 33: Branch Instructions

Data Transfer Instructions

Instruction Set Summary

Data Transfer Instructions						
	Mnemonics	Operands	Description	Operation	Flags	# Clock Note
COPY	MOV	Rd, Rr	Copy Register	$Rd \leftarrow Rr$	None	1
	MOVW	Rd, Rr	Copy Register Pair	$Rd+1:Rd \leftarrow Rr+1:Rr$	None	1
LOAD DATA	LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
	LDS	Rd, k	Load Direct from data space	$Rd \leftarrow (k)$	None	2 ⁽¹⁾
	LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2 ⁽¹⁾
	LD	Rd, X+	Load Indirect and Post-Increment	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2 ⁽¹⁾
	LD	Rd, -X	Load Indirect and Pre-Decrement	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2 ⁽¹⁾
	LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2 ⁽¹⁾
	LD	Rd, Y+	Load Indirect and Post-Increment	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2 ⁽¹⁾
	LD	Rd, -Y	Load Indirect and Pre-Decrement	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2 ⁽¹⁾
	LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2 ⁽¹⁾
	LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2 ⁽¹⁾
	LD	Rd, Z+	Load Indirect and Post-Increment	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	2 ⁽¹⁾
	LD	Rd, -Z	Load Indirect and Pre-Decrement	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2 ⁽¹⁾
	LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2 ⁽¹⁾
STORE	STS	k, Rr	Store Direct to data space	$(k) \leftarrow Rr$	None	2 ⁽¹⁾
	ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2 ⁽¹⁾
	ST	X+, Rr	Store Indirect and Post-Increment	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2 ⁽¹⁾
	ST	-X, Rr	Store Indirect and Pre-Decrement	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2 ⁽¹⁾
	ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2 ⁽¹⁾
	ST	Y+, Rr	Store Indirect and Post-Increment	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2 ⁽¹⁾
	ST	-Y, Rr	Store Indirect and Pre-Decrement	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2 ⁽¹⁾
	STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2 ⁽¹⁾
	ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2 ⁽¹⁾
	ST	Z+, Rr	Store Indirect and Post-Increment	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2 ⁽¹⁾
	ST	-Z, Rr	Store Indirect and Pre-Decrement	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2 ⁽¹⁾
	STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2 ⁽¹⁾
LOAD PGM	LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
	LPM	Rd, Z	Load Program Memory	$Rd \leftarrow (Z)$	None	3
	LPM	Rd, Z+	Load Program Memory and Post Increment	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	3
	ELPM		Increment	$R0 \leftarrow (RAMPZ:Z)$	None	3
	ELPM	Rd, Z	Extended Load Program Memory	$Rd \leftarrow (RAMPZ:Z) \leftarrow Z + 1$	None	3
	ELPM	Rd, Z+	Extended Load Program Memory and Post Increment	$Rd \leftarrow (RAMPZ:Z)$	None	3
MISC.	SPM		Store Program Memory	$(Z) \leftarrow R1:R0$	None	—
	IN	Rd, A	In From I/O Location	$Rd \leftarrow I/O(A)$	None	1
	OUT	A, Rr	Out To I/O Location	$I/O(A) \leftarrow Rr$	None	1
	PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
	POP	Rd	Pop Register From Stack	$Rd \leftarrow STACK$	None	2

Table 34: Data Transfer Instructions

Instruction Set Summary

Bit and Bit-Test Instructions

Bit and Bit-Test Instructions					
Mnemonics	Operands	Description	Operation	Flags	# Clock Note
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0, C \leftarrow Rd(7)$	Z, C, N, V, H	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0, C \leftarrow Rd(0)$	Z, C, N, V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z, C, N, V, H	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z, C, N, V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z, C, N, V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftrightarrow Rd(7..4)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	$I/O(A, b) \leftarrow 1$	None	2
CBI	A, b	Clear Bit in I/O Register	$I/O(A, b) \leftarrow 0$	None	2
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Two's Complement Overflow	$V \leftarrow 1$	V	1
CLV		Clear Two's Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1

Table 35: Bit and Bit-Test Instructions

Conditional Branch Summary

Conditional Branch Summary						
Test	Boolean	Mnemonic	Complementary	Boolean	Mnemonic	Comment
$Rd > Rr$	$Z \cdot (N \oplus V) = 0$	BRLT(1)	$Rd \leq Rr$	$Z + (N \oplus V) = 1$	BRGE*	Signed
$Rd \geq Rr$	$(N \oplus V) = 0$	BRGE	$Rd < Rr$	$(N \oplus V) = 1$	BRLT	Signed
$Rd = Rr$	$Z = 1$	BREQ	$Rd \neq Rr$	$Z = 0$	BRNE	Signed
$Rd \leq Rr$	$Z + (N \oplus V) = 1$	BRGE(1)	$Rd > Rr$	$Z \cdot (N \oplus V) = 0$	BRLT*	Signed
$Rd < Rr$	$(N \oplus V) = 1$	BRLT	$Rd \geq Rr$	$(N \oplus V) = 0$	BRGE	Signed
$Rd > Rr$	$C + Z = 0$	BRLO(1)	$Rd \leq Rr$	$C + Z = 1$	BRLO/BRCS	Unsigned
$Rd \geq Rr$	$C = 0$	BRSH/BRCC	$Rd < Rr$	$C = 1$	BRCS	Unsigned
$Rd = Rr$	$Z = 1$	BREQ	$Rd \neq Rr$	$Z = 0$	BRNE	Unsigned
$Rd \leq Rr$	$C + Z = 1$	BRSH(1)	$Rd > Rr$	$C + Z = 0$	BRLO*	Unsigned
$Rd < Rr$	$C = 1$	BRLO/BRCS	$Rd \geq Rr$	$C = 0$	BRSH/BRCC	Unsigned
Carry	$C = 1$	BRCS	No carry	$C = 0$	BRCC	Simple
Negative	$N = 1$	BRMI	Positive	$N = 0$	BRPL	Simple
Overflow	$V = 1$	BRVS	No overflow	$V = 0$	BRVC	Simple
Zero	$Z = 1$	BREQ	Not zero	$Z = 0$	BRNE	Simple

Table 36: Conditional Branch Summary

WARRANTY

System Semiconductor (“SSI”), warrants only to the purchaser of the Product from SSI (the “Customer”) that the product purchased from SSI (the “Product”) will be free from defects and meets the applicable specifications at the time of sale. Customer’s exclusive remedy under this Limited Warranty shall be the repair or replacement, at Company’s sole option, of the Product, or any part of the Product, determined by SSI to be defective.

This Limited Warranty does not extend to any Product damaged by reason of alteration, accident, abuse, neglect or misuse or improper or inadequate handling; improper or inadequate wiring utilized or installed in connection with the Product; installation, operation or use of the Product not made in strict accordance with the specifications and written instructions provided by SSI; use of the Product for any purpose other than those for which it was designed; ordinary wear and tear; disasters or Acts of God; unauthorized attachments, alterations or modifications to the Product; the misuse or failure of any item or equipment connected to the Product not supplied by SSI; improper maintenance or repair of the Product; or any other reason or event not caused by SSI.

SSI HEREBY DISCLAIMS ALL OTHER WARRANTIES, WHETHER WRITTEN OR ORAL, EXPRESS OR IMPLIED BY LAW OR OTHERWISE, INCLUDING WITHOUT LIMITATION, **ANY WARRANTIES OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE**. CUSTOMER’S SOLE REMEDY FOR ANY DEFECTIVE PRODUCT WILL BE AS STATED ABOVE, AND IN NO EVENT WILL THE SSI BE LIABLE FOR INCIDENTAL, CONSEQUENTIAL, SPECIAL OR INDIRECT DAMAGES IN CONNECTION WITH THE PRODUCT.

This Limited Warranty shall be void if the Customer fails to comply with all of the terms set forth in this Limited Warranty. This Limited Warranty is the sole warranty offered by SSI with respect to the Product. SSI does not assume any other liability in connection with the sale of the Product. No representative of SSI is authorized to extend this Limited Warranty or to change it in any manner whatsoever. No warranty applies to any party other than the original Customer.

SSI and its directors, officers, employees, subsidiaries and affiliates shall not be liable for any damages arising from any loss of equipment, loss or distortion of data, loss of time, loss or destruction of software or other property, loss of production or profits, overhead costs, claims of third parties, labor or materials, penalties or liquidated damages or punitive damages, whatsoever, whether based upon breach of warranty, breach of contract, negligence, strict liability or any other legal theory, or other losses or expenses incurred by the Customer or any third party.

System Semiconductor’s general policy does not recommend the use of its products in life support or aircraft applications wherein a failure or malfunction of the product may directly threaten life or injury. Per System Semiconductor’s terms and conditions of sales, the user of System Semiconductor, products in life support or aircraft applications assumes all risks of such use and indemnifies System Semiconductor, against all damages.

