NEC

AGC AMPLIFIER | UPC3211GR

FEATURES

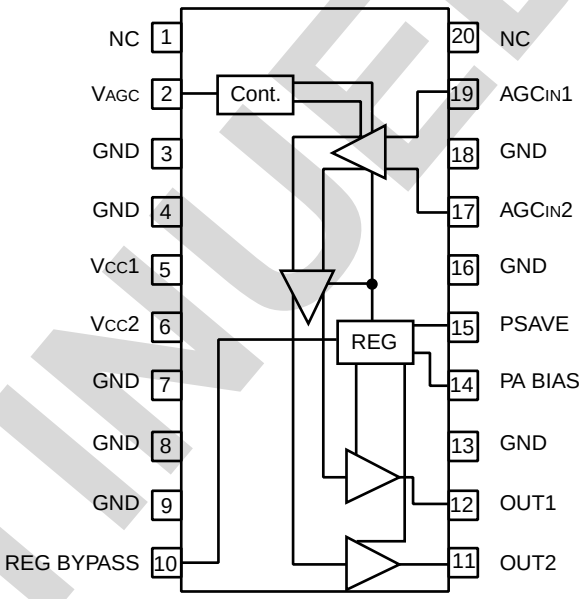
- **WIDE GAIN CONTROL RANGE:** 55 dB (TYP)
- **LOW DISTORTION:**
  IM_3 = 57 dBc (TYP) at P_{OUT} = -10 dBm
  IM_2 = 44 dBc (TYP) at P_{OUT} = -10 dBm
- **SUPPLY VOLTAGE:** 9 V
- **PACKAGED IN 20 PIN SSOP SUITABLE FOR HIGH-DENSITY SURFACE MOUNT**

DESCRIPTION

The UPC3211GR is a Silicon RFIC designed as an AGC amplifier for digital CATV return path applications. This IC consists of an AGC amplifier with 55 dB gain control range which is packaged in a 20 pin SSOP.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

INTERNAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 9 V, V_{AGC} = 0 V, V_{PS} = 9 V, unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPC3211GR S20		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{CC}	Circuit Current (no input signal), V_{AGC} = 0 V V_{AGC} = 3 V	mA mA	29	38 43	51
$I_{CC(PS)}$	Circuit Current in Power Save Mode (no input signal), V_{PS} = 0 V[1]	mA		3	
G_{MAX}	Maximum Gain[2]	dB	14	16	18
GCR	Gain Control Range[2], V_{AGC} = 0 to 3 V	dB	47	55	
G_{FLAT}	Gain Flatness, f_{IN} = 5 to 100 MHz, 6 MHz Bandwidth	dB		±0.1	
P_{SAT}	Saturated Output Power, P_{IN} = -5 dBm	dBm		+5	
I_{SOL}	Isolation in Sleep Mode, V_{PS} = 0 V[1]	dB	60	65	
IM_2	2nd Order Intermodulation Level, f_{IN1} = 65 MHz, f_{IN2} = 66.8 MHz, P_{OUT} = -10 dBm	dBc		44	40
IM_3	3rd Order Intermodulation Level, f_{IN1} = 65 MHz, f_{IN2} = 66.8 MHz, P_{OUT} = -10 dBm	dBc		57	50
NF	Noise Figure, f_{IN} = 65 MHz	dB		10	
OIP_3	Output 3rd Order Intercept Point, f_{IN1} = 65 MHz, f_{IN2} = 66.8 MHz	dBm		+16	
$T_{PS\ (RISE)}$	Power Save Rise Time, $V_{PS(OFF)} \rightarrow V_{PS(ON)}$	µs		200	
$T_{PS\ (FALL)}$	Power Save Fall Time, $V_{PS(ON)} \rightarrow V_{PS(OFF)}$	mS		1.7	

Notes:
1. Bias V_{PS} through a 5 kΩ Resistor.
2. f_{IN} = 65 MHz, P_{IN} = -20 dBm.

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	11.0
V_{PS}	Power Save Voltage[3]	V	11.0
V_{AGC}	AGC Control Voltage	V	3.6
P_D	Power Dissipation[2]	mW	500
T_A	Operating Ambient Temp.	°C	-40 to +75
T_{STG}	Storage Temp. Range	°C	-55 to +150
$P_{IN(MAX)}$	Maximum Input Level	dBm	+5

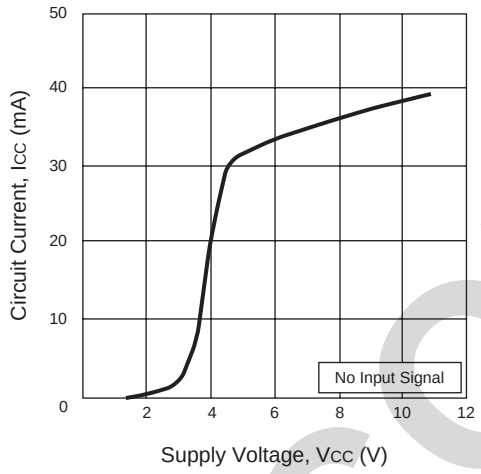
Notes:
1. Operation in excess of any one of these conditions may result in permanent damage.
2. T_A = 75°C Mounted on a 50x50x1.6 mm double epoxy glass board.
3. Bias V_{PS} through 5 k Ω resistor.

RECOMMENDED OPERATING CONDITIONS

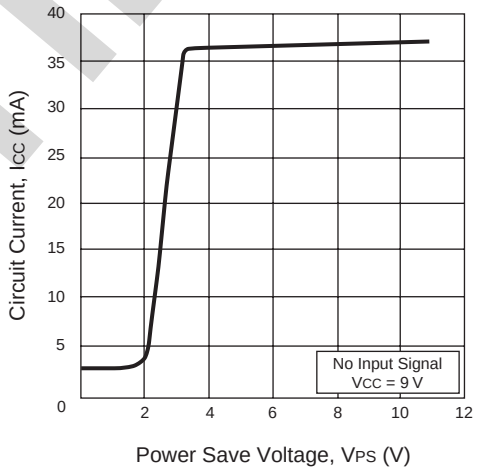
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	8.0	9.0	10.0
V_{PS}	Power Save Voltage	V	0	–	10.0
V_{AGC}	AGC Control Voltage	V	0	–	3.3
T_A	Operating Ambient Temp.	°C	-40	+25	+75
f_{IN}	Input Frequency	MHz	5	–	100
$P_{IN(MAX)}$	Maximum Input Level	dBm	–	–	0

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

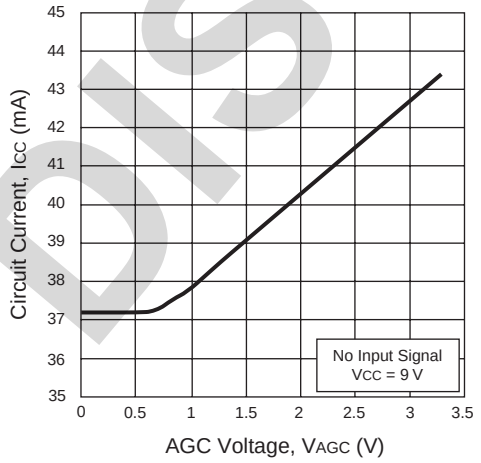
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



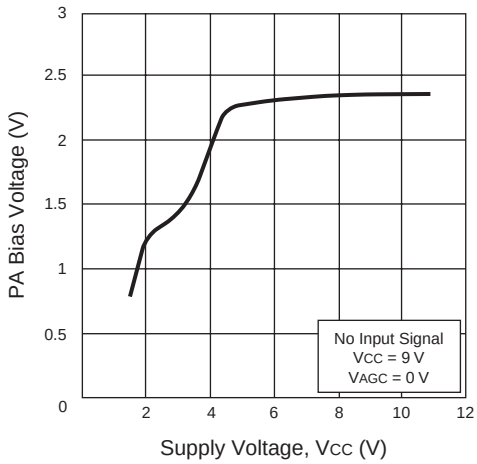
CIRCUIT CURRENT vs. POWER SAVE VOLTAGE



CIRCUIT CURRENT vs. AGC VOLTAGE

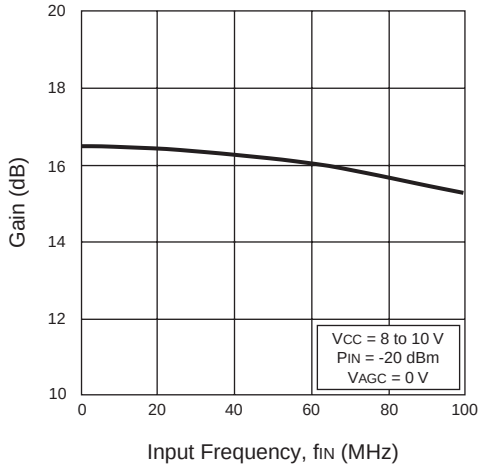


PA BIAS VOLTAGE vs. SUPPLY VOLTAGE

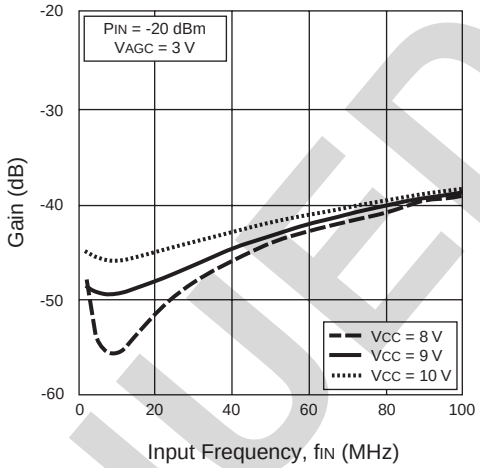


TYPICAL PERFORMANCE CURVES (T_A = 25°C)

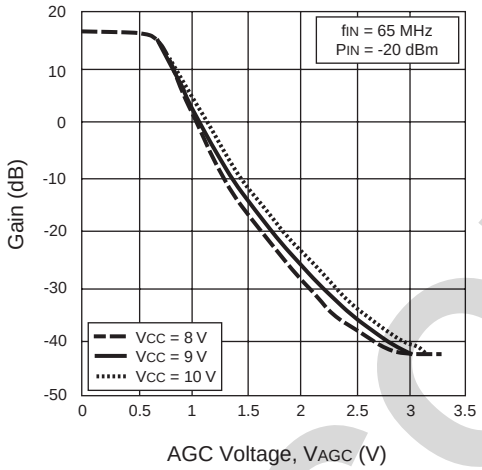
GAIN vs. INPUT FREQUENCY



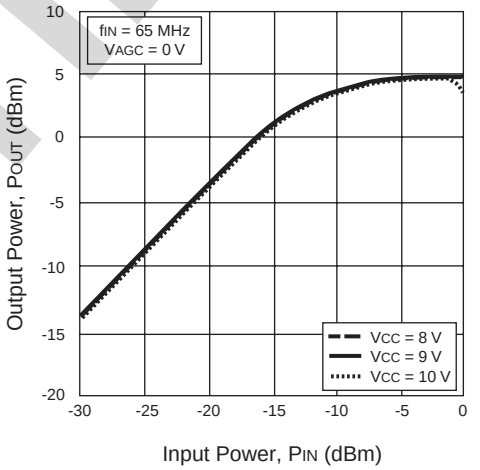
GAIN vs. INPUT FREQUENCY AND SUPPLY VOLTAGE



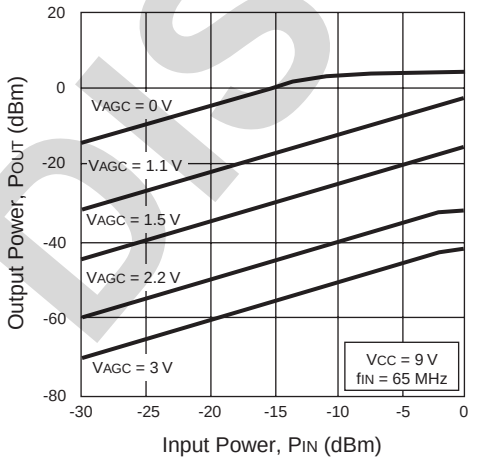
GAIN vs. AGC VOLTAGE AND SUPPLY VOLTAGE



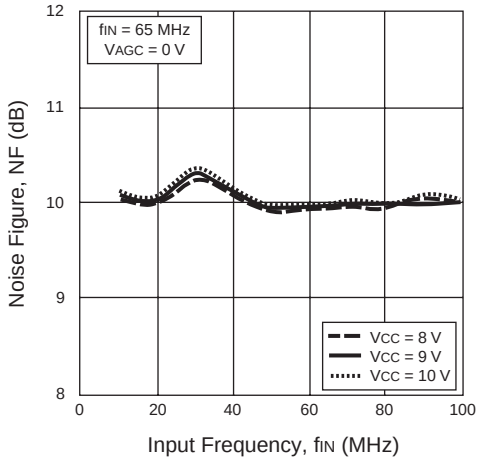
OUTPUT POWER vs. INPUT POWER AND SUPPLY VOLTAGE



OUTPUT POWER vs. INPUT POWER AND AGC VOLTAGE

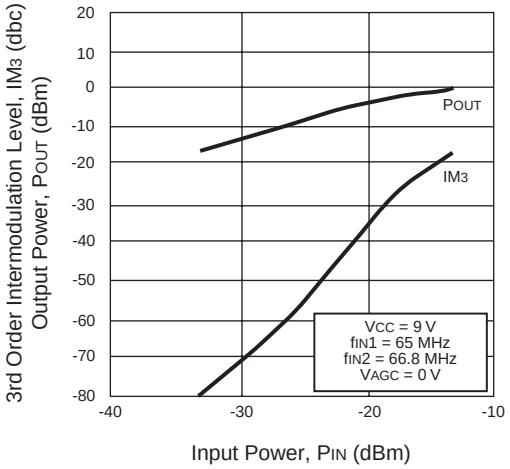


NOISE FIGURE vs. INPUT FREQUENCY AND SUPPLY VOLTAGE

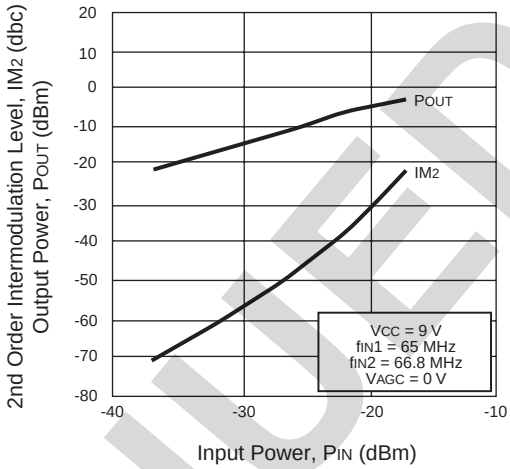


STANDARD PERFORMANCE CURVES (T_A = 25°C)

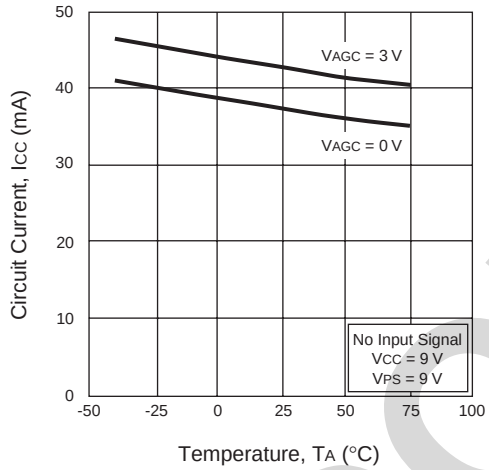
3RD ORDER INTERMODULATION LEVEL AND OUTPUT POWER vs. INPUT POWER



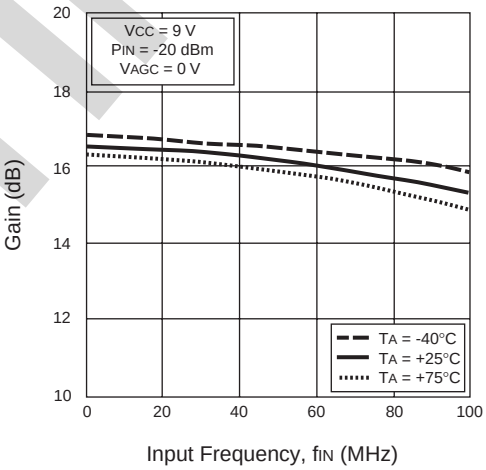
2ND ORDER INTERMODULATION LEVEL AND OUTPUT POWER vs. INPUT POWER



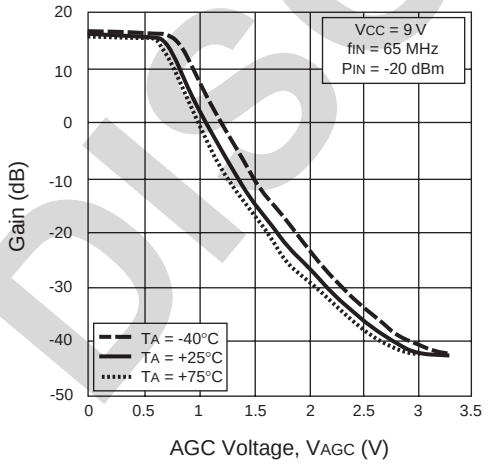
CIRCUIT CURRENT vs. TEMPERATURE



GAIN vs. INPUT FREQUENCY AND TEMPERATURE

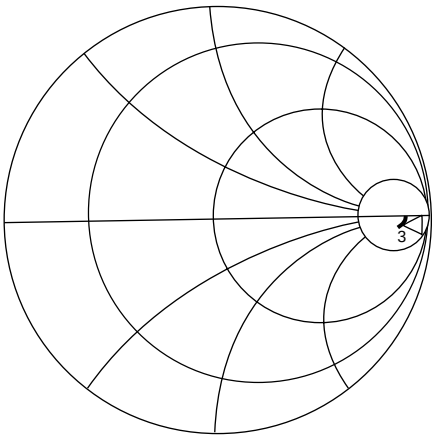


GAIN vs. AGC VOLTAGE AND TEMPERATURE



STANDARD PERFORMANCE CURVES (T_A = 25°C)

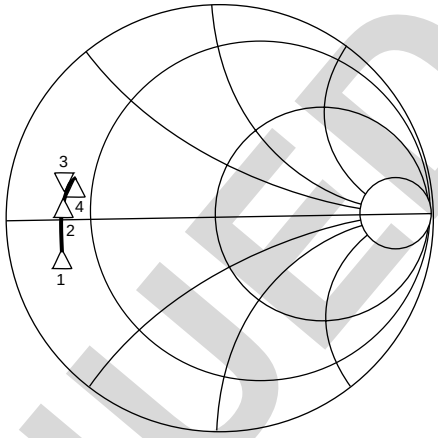
INPUT IMPEDANCE (PIN 19)



Start 0.1 MHz	Stop 100 MHz	
Δ 1: 5 MHz	533.6 Ω	-16.4 Ω
Δ 2: 40 MHz	515.2 Ω	-81.4 Ω
Δ 3: 65 MHz	493.7 Ω	-123.3 Ω
Δ 4: 100 MHz	455.9 Ω	-190.3 Ω

T_A = 25°C
V_{CC} = 9 V
P_{IN} = -20 dBm

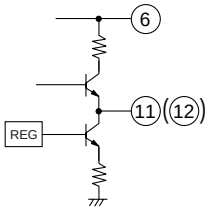
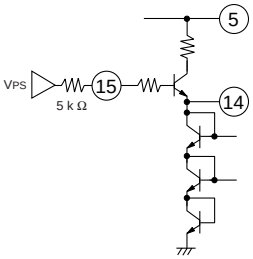
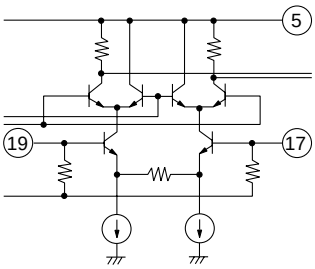
OUTPUT IMPEDANCE (PIN 11)



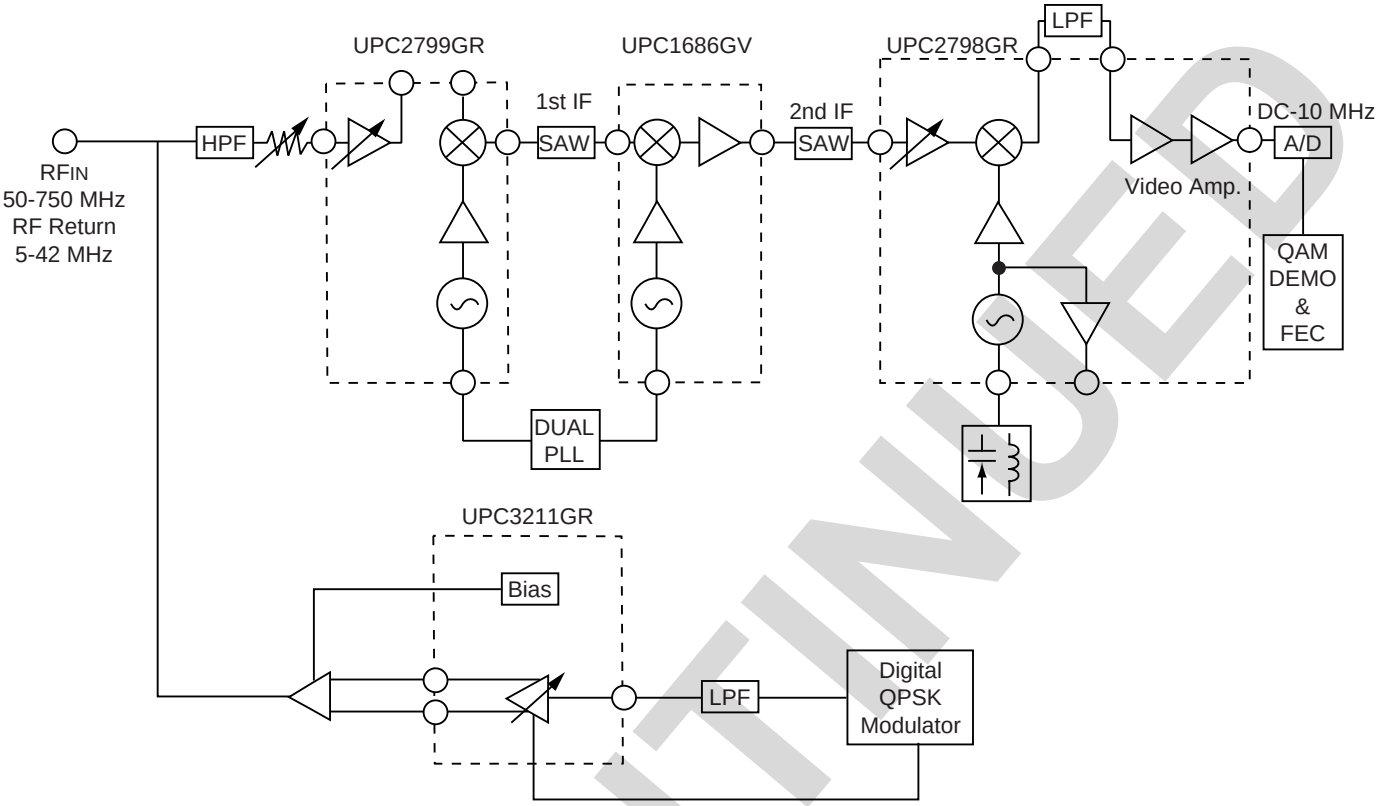
Start 5 MHz	Stop 100 MHz	
Δ 1: 5 MHz	9.779 Ω	-2.306 Ω
Δ 2: 40 MHz	10.066 Ω	3.033 Ω
Δ 3: 65 MHz	10.574 Ω	5.237 Ω
Δ 4: 100 MHz	11.88 Ω	7.805 Ω

T_A = 25°C
V_{CC} = 9 V
P_{IN} = -20 dBm

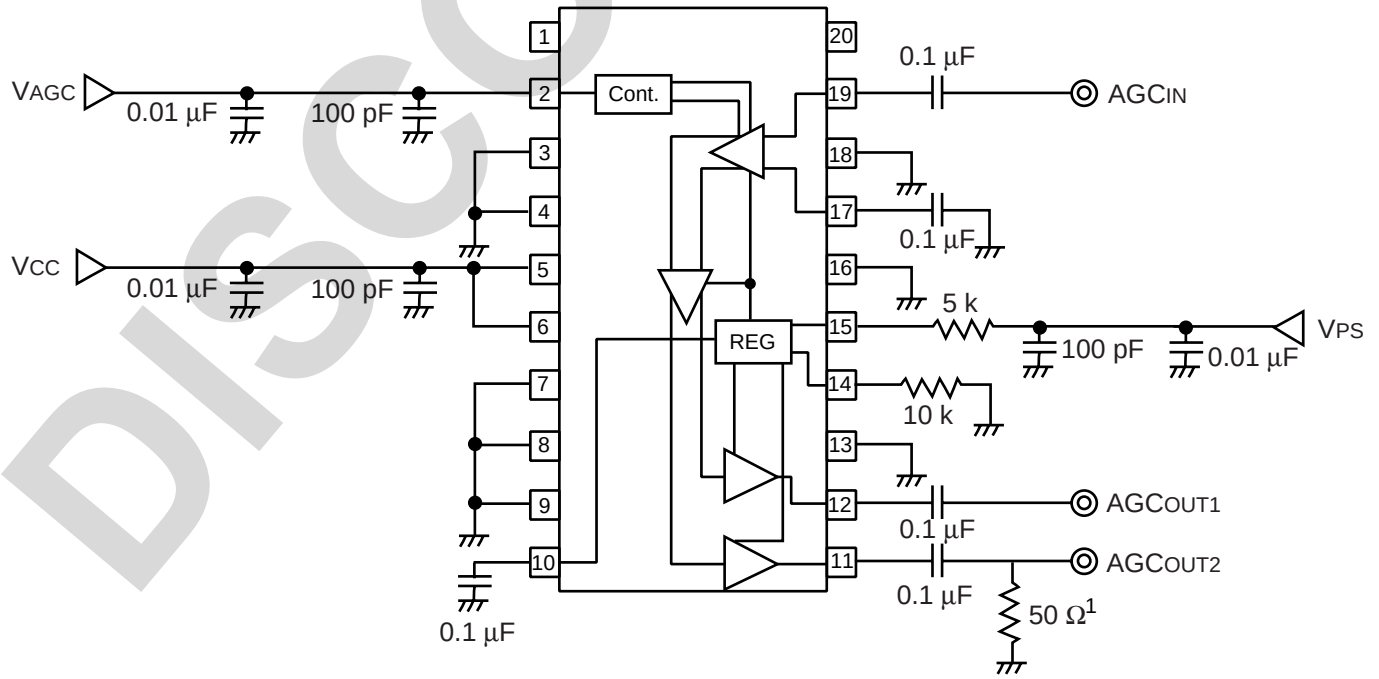
PIN FUNCTIONS

Pin No.	Symbol	Pin Voltage (V)	Description	Equivalent Circuit
1	NC	–	No connection. This pin should be left open.	
2	V_{AGC}	0 to 3	Automatic gain control pin. V_{AGC} Up = Gain Down.	
3 4	GND	0	Differential amp ground pins. These pins must be connected to system ground. Form ground pattern as wide as possible to minimize ground impedance.	
5	$V_{CC}1$	9.0	Supply voltage pin for the AGC amp. This pin should be connected with a bypass capacitor to minimize ground impedance.	
6	$V_{CC}2$	9.0	Supply voltage pin for the differential amp and output block. This pin should be connected with a bypass capacitor to minimize ground impedance.	
7 8 9	GND	0	Differential amp ground pins. These pins must be connected to system ground. Form ground pattern as wide as possible to minimize ground impedance.	
10	REG BYPASS	1.64	Bypass pin of regulator block. This pin should be bypassed to ground through a capacitor.	
11	OUT2	6.9	Signal output pins. These are emitter-follower outputs, which feature low impedance. In case of single-ended output, the unused pin should be connected to ground through a load resistor.	
12	OUT1	6.9		
13	GND	0	Output block ground pin. This pin must be connected to system ground. Form ground pattern as wide as possible to minimize ground impedance.	
14	PA_BIAS	2.45	This pin provides the base bias voltage to transistors configured as a power amplifier.	
15	V_{PS}	9.0	Power save control pin can control the On/Sleep state with bias as follows: V_{PS} (V) / STATE: 3-9 / ON; 0-2 / SLEEP It is recommended to use a 5 kΩ in series with this pin.	
16 18	GND	0	AGC amp ground pin. This pin must be connected to system ground. Form ground pattern as wide as possible to minimize ground impedance.	
17	AGC_{IN2}	2.43	Signal input pins. In the case of single-ended input, bypass the unused pin to ground through a capacitor.	
19	AGC_{IN1}	2.43		
20	NC	—	No connection. This pin should be left open.	

TYPICAL APPLICATION



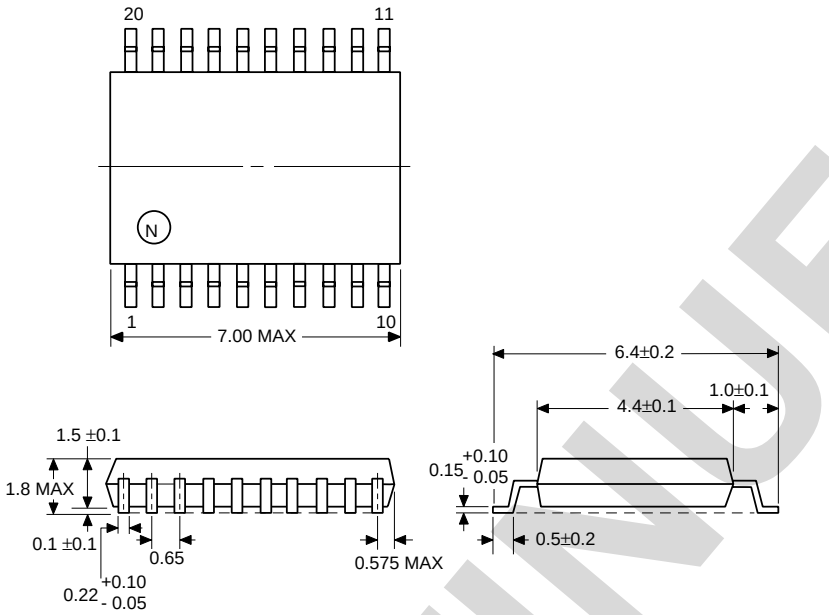
MEASUREMENT CIRCUIT



Note:
1. The pin that is not connected to the 50 Ω test system should be grounded through a 50 Ω resistor.

PACKAGE DIMENSIONS (Units in mm)

PACKAGE OUTLINE S20



Note:
1. All dimensions are typical unless otherwise specified.

ORDERING INFORMATION

PART NUMBER	QUANTITY
UPC3211GR-E1	2.5 k/Reel

Notes:
Embossed tape, 12 mm wide. Pin 1 indicates pull-out direction of tape.