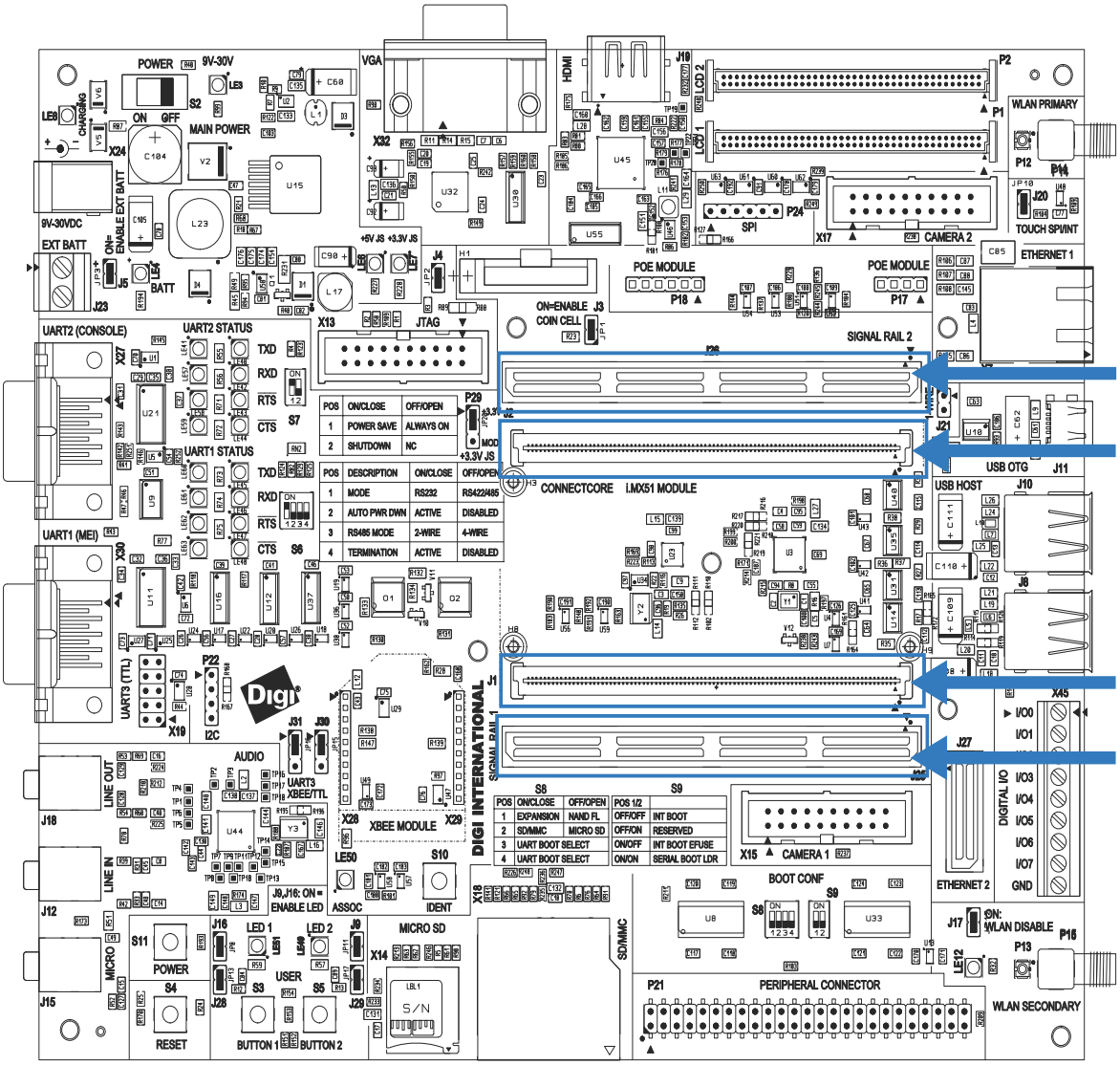
Module Connectors and Signal Rails



Module Connectors

See the "Module Pinout" chapter on page 14 for related information.

Signal Rails, J25 and J26

The development board provides two 2x80 pin signal rails, J25 and J26. These connectors provide most of the signals available on the module connectors and can be used for measurement or development purposes.

- J25 corresponds to module connector J1
- J26 corresponds to module connector J2

J25 Pinout

Pin	Signal	Pin	Signal
1	CSI1_D8	2	CSI1_D9
3	CSI1_D10	4	CSI1_D11
5	CSI1_D12	6	CSI1_D13
7	CSI1_D14	8	CSI1_D15
9	CSI1_D16	10	CSI1_D17
11	CSI1_D18	12	CSI1_D19
13	CSI1_VSYNC/GPIO3_14	14	CSI1_HSYNC/GPIO3_15
15	CSI1_PIXCLK	16	CSI1_MCLK
17	WLAN_TDO	18	WLAN_TCK
19	WLAN_TDI	20	WLAN_TMS
21	WLAN_LED	22	RS_BT_PRIORITY
23	RS_WLAN_ACTIVE	24	RS_BT_ACTIVE
25	+2.775V	26	WLAN_DISABLE#
27	+2.775V	28	+2.775V
29	MC13892_GPO1	30	+2.775V
31	PMIC_PWRON1	32	PMIC_STDBY_REQ
33	PMIC_INT_REQ	34	PWRGTDRV1
35	CHRGLED	36	PWRGTDRV2
37	CHRGSE1#	38	VCC_COINCELL
39	VLIO	40	+5V_IN

Pin	Signal	Pin	Signal
41	VLIO	42	+5V_IN
43	VLIO	44	+5V_IN
45	DISP2_SER_DIN/GPIO3_5	46	DISPB2_SER_DIO/GPIO3_6
47	DISPB2_SER_RS/GPIO3_8	48	DISPB2_SER_CLK/GPIO3_7
49	DISP2_DATA0/MII_RXD3/USBH3_CLK	50	DISP2_DATA1/MII_RX_ER/USBH3_DIR
51	DISP2_DATA2	52	DISP2_DATA3
53	DISP2_DATA4	54	DISP2_DATA5
55	DISP2_DATA6/MII_TXD1/USBH3_STP	56	DISP2_DATA7/MII_TXD2/USBH3_NXT
57	DISP2_DATA8/MII_TXD3/USBH3_DATA0	58	DISP2_DATA9/MII_TXEN/USBH3_DATA1
59	DISP2_DATA10/MII_COL/USBH3_DATA2	60	DISP2_DATA11/MII_RX_CLK/USBH3_DATA3
61	DISP2_DATA12/MII_RX_DV/USBH3_DATA4	62	DISP2_DATA13/MII_TX_CLK/USBH3_DATA5
63	DISP2_DATA14/MII_RXD0/USBH3_DATA6	64	DISP2_DATA15/MII_TXD0/USBH3_DATA7
65	D12_PIN2/MII_MDC	66	D12_DISP_CLK/MII_RXD1
67	D12_PIN4/MII_CRS	68	D12_PIN3/MII_MDIO
69	IOR	70	IOG
71	IOR_BACK	72	IOG_BACK
73	IOB	74	JTAG_TRST#
75	IOB_BACK	76	JTAG_MOD#
77	JTAG_TCK	78	JTAG_DE#
79	JTAG_TMS	80	RESET_IN#
81	JTAG_TDI	82	+1.8V
83	JTAG_TDO	84	EIM_CS1/GPIO2_26
85	POR#	86	EIM_CS3/GPIO2_28
87	EIM_CS0/GPIO2_25	88	EIM_CS5_LAN9221_CS#/GPIO2_30
89	EIM_CS2/GPIO2_27	90	EIM_LBA/GPIO3_1
91	EIM_CS4/GPIO2_29	92	EIM_DA1/TRACE17
93	EIM_DTACK/GPIO2_31	94	EIM_DA3/TRACE19
95	EIM_DA0/TRACE16	96	EIM_DA5/TRACE21
97	EIM_DA2/TRACE18	98	EIM_DA7/TRACE23
99	EIM_DA4/TRACE20	100	EIM_DA9/TRACE25
101	EIM_DA6/TRACE22	102	EIM_DA11/TRACE27
103	EIM_DA8/TRACE 24	104	EIM_DA13/TRACE29
105	EIM_DA10/TRACE26	106	EIM_DA15/TRACE31

Pin	Signal	Pin	Signal
107	EIM_DA12/TRACE28	108	EIM_DA17/TRACE1
109	EIM_DA14/TRACE30	110	EIM_DA19/TRACE3
111	EIM_DA16/TRACE0	112	EIM_DA21/TRACE5
113	EIM_DA18/TRACE2	114	EIM_DA23/TRACE7
115	+3.15V	116	EIM_DA25/TRACE9
117	EIM_DA20/TRACE4	118	EIM_DA27/TRACE11
119	EIM_DA22/TRACE6	120	EIM_DA29/TRACE13
121	EIM_DA24/TRACE8	122	EIM_DA31/TRACE15
123	EIM_DA26/TRACE10	124	EIM_A17/GPIO2_11
125	EIM_DA28/TRACE12	126	EIM_A19/GPIO2_13
127	EIM_DA30/TRACE14	128	EIM_A21/GPIO2_15
129	EIM_A16/GPIO2_10	130	EIM_A23/GPIO2_17
131	EIM_A18/GPIO2_12	132	EIM_A25/GPIO2_19
133	EIM_A20/GPIO2_14	134	EIM_A27/GPIO2_21
135	EIM_A22/GPIO2_16	136	EIM_OE#/GPIO2_24
137	EIM_A24/GPIO2_18	138	EIM_RW#
139	EIM_A26.GPIO2_20	140	EIM_CRE/GPIO3_2
141	EIM_EB0	142	EIM_WAIT
143	EIM_EB1	144	GND
145	EIM_EB2/GPIO2_22/TRCTL	146	EIM_BCLK
147	EIM_EB3/GPIO2_23/TRCLK	148	GND
149	NANDF_ALE/GPIO3_5	150	NAND_RE#/SD3_DATA1/GPIO3_4
151	NANDF_WP#/SD3_DATA2/GPIO3_7	152	NANDF_CLE/GPIO3_6
153	NANDF_RB1_SP12_RDY/GPIO3_9	154	NANDF_RB0/SD3_DATA3/GPIO3_8
155	NANDF_RB3/SP12_MISO/GPIO3_11	156	NANDF_R2/SP12_SCLK/GPIO3_10
157	-	158	-
159	-	160	-

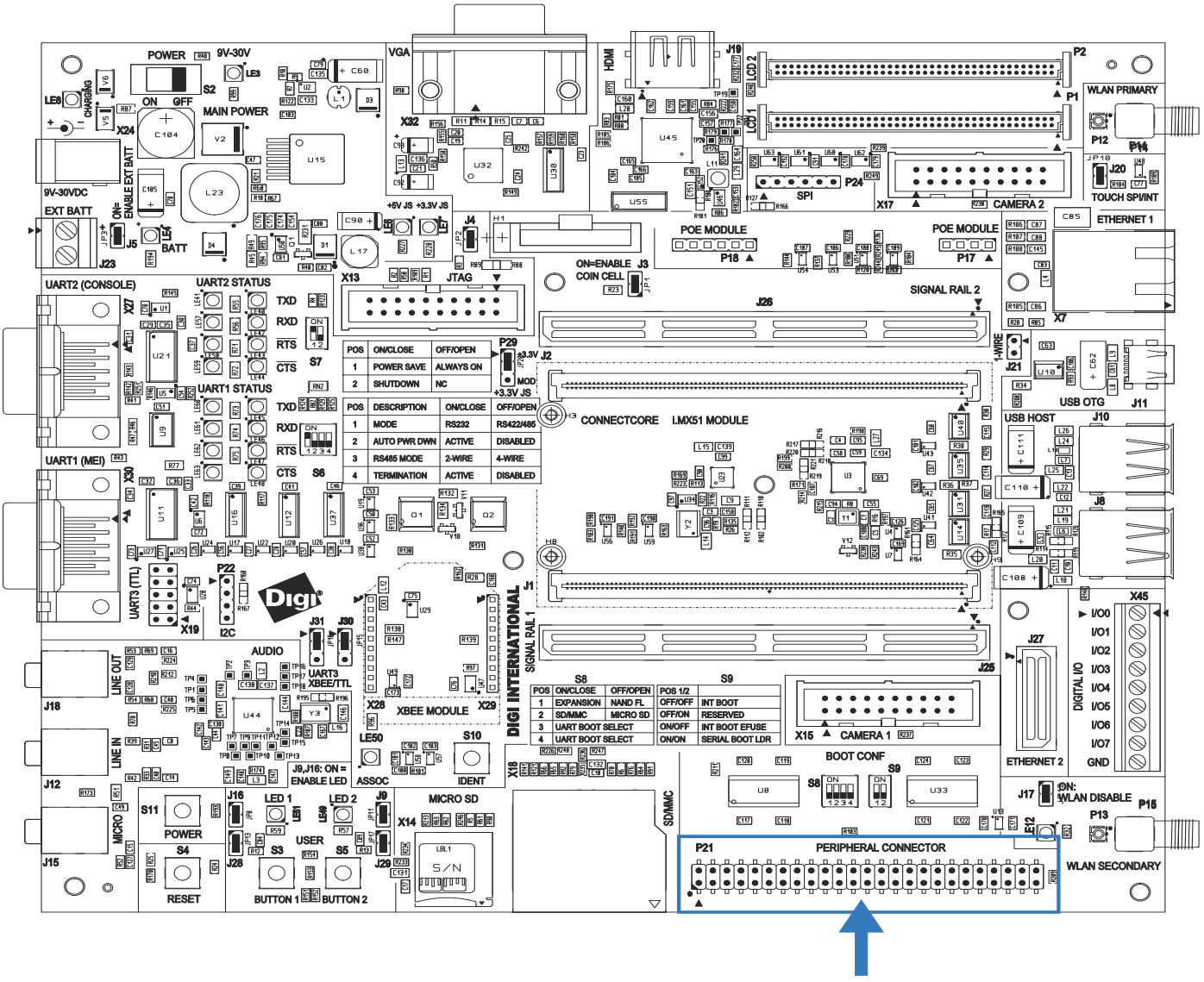
J26 Pinout

Pin	Signal	Pin	Signal
1	DISP1_DAT0	2	DISP1_DAT1
3	DISP1_DAT2	4	DISP1_DAT3
5	DISP1_DAT4	6	DISP1_DAT5
7	DISP1_DAT6	8	DISP1_DAT7
9	DISP1_DAT8	10	DISP1_DAT9
11	DISP1_DAT10	12	DISP1_DAT11
13	DISP1_DAT12	14	DISP1_DAT13
15	DISP1_DAT14	16	DISP1_DAT15
17	DISP1_DAT16	18	DISP1_DAT17
19	DISP1_DAT18	20	DISP1_DAT19
21	DISP1_DAT20	22	DISP1_DAT21
23	DISP1_DAT22	24	DISP1_DAT23
25	DI1_PIN2	26	DI1_DISP_CLK
27	DI1_PIN11/GPIO3_0	28	DI1_PIN3
29	DI1_PIN13/GPIO3_2	30	DI1_PIN12/GPIO3_1
31	DI1_PIN15	32	DI_GP1
33	DI_GP2	34	DI_GP3/MII_TX_ER
35	DI_GP4/MII_RXD2	36	DI1_D0_CS/GPIO3_3
37	DI1_D1_CS/GPIO3_4	38	ADIN5
39	TOUCH_X1	40	ADIN6
41	TOUCH_X2	42	ADIN7
43	TOUCH_Y1	44	ADC_GND
45	TOUCH_Y2	46	ADTRIG
47	SWBST	48	-
49	LEDR	50	-
51	LEDG	52	-
53	LEDB	54	-
55	CSI2_D12/GPIO4_9	56	CSI2_D13/GPIO4_10
57	CSI2_D14	58	CSI2_D15
59	CSI2_D16	60	CSI2_D17

Pin	Signal	Pin	Signal
61	CSI2_D18/GPIO4_11	62	CSI2_D19/GPIO4_12
63	CSI2_VSYNC/GPIO4_13	64	CSI2_HSYNC/GPIO4_14
65	CSI2_PIXCLK/GPIO4_15	66	GPIO1_8/USB_PWR
67	GPIO1_7/MMA7455LR_INT1	68	GPIO1_2/PWM1/I2C2_SCL
69	GPIO1_6/MMA7455LR_INT2	70	GPIO1_3/PWM2/I2C2_SDA
71	CKIH1	72	CLK32K_PER
73	SD2_DATA0/SD1_DATA4/SPI_MOSI	74	CKIH2
75	SD2_DATA1/SD1_DATA5	76	SD2_CLK/I2C1_SDA/SPI_SCLK
77	SD2_DATA2/SD1/DATA6	78	SD2_CMD/I2C1_SCL/SPI_MOSI
79	SD2_DATA3/SD1_DATA7/SPI_SS2	80	KEY_COL0
81	ROW0	82	KEY_COL1
83	ROW1	84	KEY_COL2
85	ROW2	86	KEY_COL3
87	ROW3	88	KEY_COL5/UART3_CTS#/I2C2_SDA
89	KEY_COL4/UART3_RTS#/I2C2_SCL	90	GPIO1_0/SD1_CD#/SPI_SS2
91	OWIRE_LINE/GPIO1_24	92	GPIO1_1/SD1_WP#/SPI_MISO
93	SC1_CMD/AUD5_RXFS/SPI_MOSI	94	SD1_DAT0/AUD5_TXD/SPI_MOSI
95	SD1_CLK/AUD5_RXC/SPI_SCLK	96	SD1_DATA1/AUD5_RXD
97	WDOG1#/GPIO1_4	98	SD1_DATA2/AUD5_TXC
99	CSPI1_MOSI/I2C1_SDA/GPIO4_22	100	SD1_DATA3/AUD5_TXFS/SPI_SS1
101	CSPI1_MISO/AUD4_RXD/GPIO4_23	102	CSPI1_SS0_PMIC/AUD4_TXC/GPIO4_24
103	CSPI1_SCLK/I2C1_SDA/GPIO4_27	104	CSPI1_SS1/AUD4_TXD/GPIO4_25
105	UART1_RXD/GPIO4_28	106	CSPI1_RDY/AUD4_TXFS/GPIO4_26
107	UART1_TXD/PWM2/GPIO4_29	108	UART1_RTS#/GPIO4_30
109	UART2_RXD/GPIO1_20	110	UART1_CTS#/GPIO4_31
111	UART2_TXD/GPIO1_21	112	UART3_RXD/UART1_DTR#/GPIO1_22
113	USBH1_DATA2/UART2_TXD/GPIO1_13	114	UART3_TXD/UART1_DSR#/GPIO_23
115	USBH1_DATA4/SPI_SS0/GPIO1_15	116	USBH1_DATA0/UART2_CTS#/GPIO1_11
117	USBH1_DATA6/SPI_SS2/GPIO1_17	118	USBH1_DATA1/UART2_RXD/GPIO1_12
119	USBH1_DIR/SPI_MOSI/GPIO1_26/ I2C2_SDA	120	USBH1_DATA3/UART2_RTS#/GPIO1_14
121	USBH1_STP/SPI_RDY/GPIO1_27	122	USBH1_DATA5/SPI_SS1/GPIO1_16

Pin	Signal	Pin	Signal
123	USBH1_NXT/SPI_MISO/GPIO1_28	124	USBH1_DATA7/SPI_SS3/SPI2_SS3/ GPIO1_18
125	AUD3_BB_TXD/GPIO4_18	126	USBH1_CLK/SPI_SCLK/GPIO1_25/ I2C2_SCL
127	AUD3_BB_RXD/UART3_RXD/ GPIO4_19	128	HS_I2C_SCL/GPIO4_16
129	AUD3_BB_CK/GPIO4_20	130	HS_I2C_SDA/GPIO4_17
131	+3.3V MOD	132	AUD3_BB_FS/UART3_TXD/GPIO4_21
133	NANDF_D0/PATA_D0/SD4_DATA7/ GPIO4_8	134	+3.3V
135	NANDF_D2/PATA_D2/SD4_DATA5/ GPIO4_6	136	NANDF_D1/PATA_D1/SD4_DATA6/ GPIO4_7
137	NANDF_D4/PATA_D4/SD4_CD/ GPIO4_4	138	NANDF_D3/PATA_D3/SD4_DATA4/ GPIO4_5
139	NANDF_D6/PATA_D6/SD4_LCTL/ GPIO4_2	140	NANDF_D5/PATA_D5/SD4_WP#/GPIO4_3
141	NANDF_D8/PATA_D8/GPIO4_0/ SD3_DATA0	142	NANDF_D7/PATA_D7/GPIO4_1
143	NANDF_D10/PATA_D10/GPIO3_30/ SD3_D2	144	NANDF_D9/PATA_D9/GPIO3_31/SD3_D1
145	NANDF_D12/PATA_D12/GPIO3_28/ SD3_D4	146	NANDF_D11/PATA_D11/GPIO3_29/ SD3_D3
147	NANDF_D14/PATA_D14/GPIO3_26/ SD3_D6	148	NANDF_D13/PATA_D13/GPIO3_27/ SD3_D5
149	NANDF_CS0#/GPIO3_16	150	NANDF_D15/PATA_D15/GPIO3_25/ SD3_D7
151	NANDF_CS2#/PATA_CS0#/GPIO3_18	152	NANDF_CS1#/GPIO3_17
153	NANDF_CS4#/PATA_DA0/GPIO3_20	154	NANDF_CS3#/PATA_CS1#/GPIO3_19
155	NANDF_CS6#/PATA_DA2/GPIO3_22	156	NANDF_CS5#/PATA_DA1/GPIO3_21
157	NANDF_RDY_INT/GPIO3_24	158	NANDF_CS7#/GPIO3_23
159	NANDF_WE#/PATA_DIOW/GPIO3_3	160	GPIO_NAND/PATA_INTRQ/GPIO3_12

Peripheral Application Header



The development board provides one, 2x25-pin, 2.54mm pitch header for applications-specific daughter cards/expansion boards:

- P21, Peripheral application header. Provides access to a 16-bit data bus, 10-bit address bus and control signals (such as CS#, OE#, WE#), as well as I^2C and power (+3.3V). Using these signals you can connect Digi-specific extension modules or your own custom daughter card to the module's address/data bus and other interfaces.

Peripheral Application Header, P21

Pin	Signal	Pin	Signal
1	GND	2	D0
3	D1	4	D2
5	D3	6	GND
7	D4	8	D5
9	D6	10	D7
11	GND	12	D8
13	D9	14	D10
15	D11	16	GND
17	D12	18	D13
19	D14	20	D15
21	GND	22	8-bit / 16-bit (default)
23	GND	24	+3.3V
25	+3.3V	26	A0
27	A1	28	A2
29	A3	30	GND
31	A4	32	A5
33	A6	34	A7
35	GND	36	A8
37	A9	38	GND
39	CS0#	40	I^2C^2_SDA/GPIO1_3
41	WE#	42	OE#
43	I^2C^2_SCL/GPIO1_2	44	GPIO3_2
45	+3.3V	46	+3.3V
47	BE2#	48	BE3#
49	BCLK	50	GND

The voltage level of the data, address and control signals provided by the module is +1.8V. A level shifter is provided on the development board to buffer and change the voltage level of most peripheral application signals on this header to +3.3V.

The Data bus signals D0 - D15 are connected to the i.MX51 data bus signals D16 - D31.

The Address bus signals A0 - A9 are connected to the i.MX51 data/address bus signals DA0 - DA9.

The BE2# signal is connected to the i.MX51 byte enable 2 (D16 - D23).

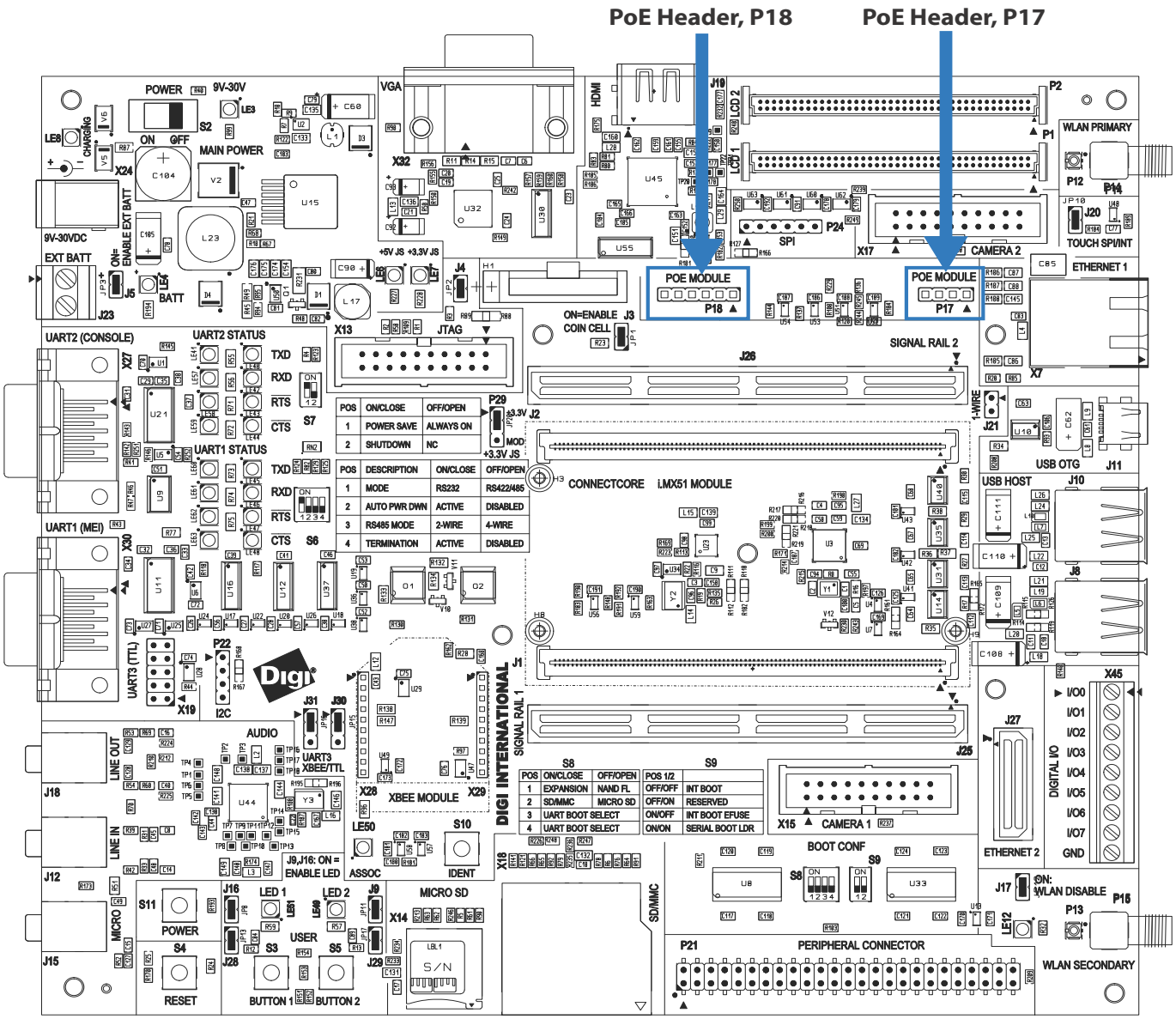
The BE3# signal is connected to the i.MX51 byte enable 3 (D24 - D31).

The BCLK signal corresponds to the i.MX51 burst clock signal. This clock signal is not buffered, and its voltage level is +1.8V. This signal is connected to the peripheral connector through a 0R resister. By default, this resistor is not populated.

The I^2C interface corresponds to i.MX51 I^2C port 2. For more information, refer to the I^2C chapter in this document.

The signal GPIO3_2 can only be used as an input signal to the i.MX51. This signal is intended to be used as interrupt line in the peripheral boards.

Power-Over-Ethernet (PoE) - IEEE802.3af



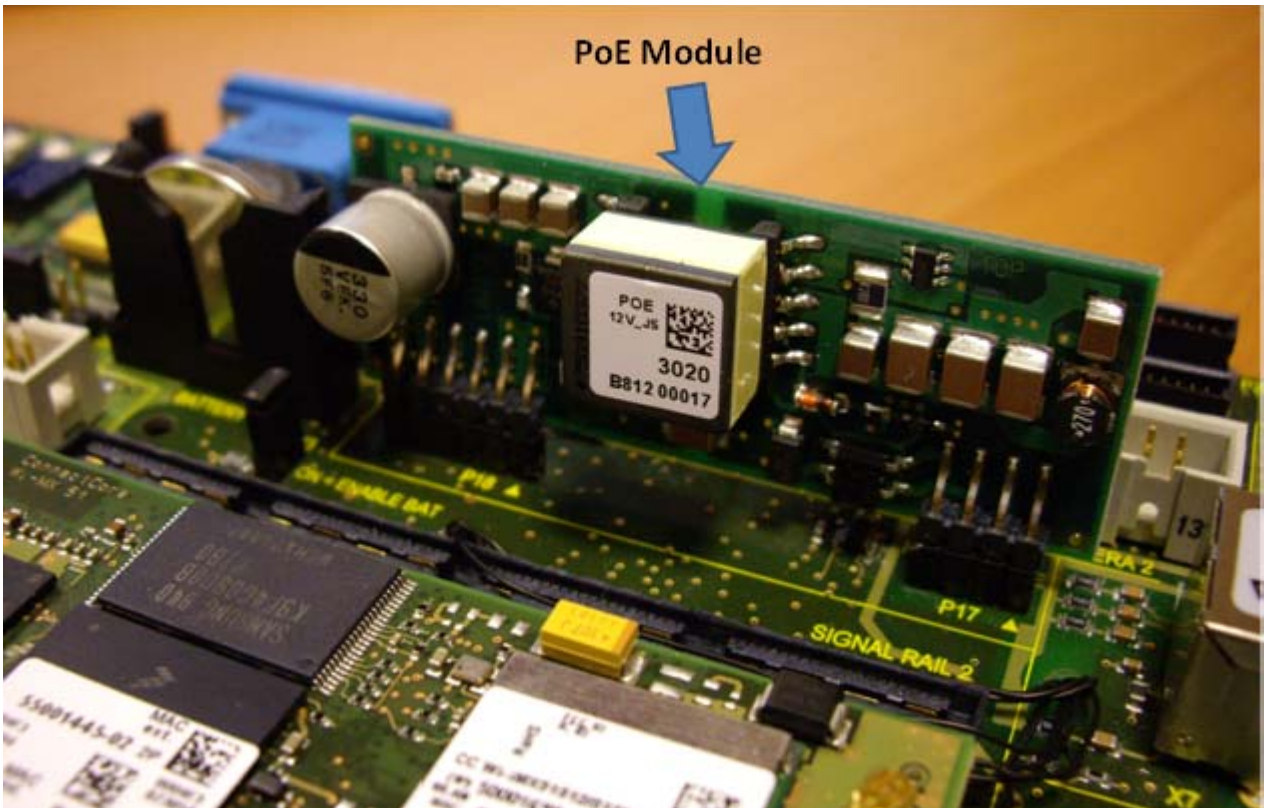
The development board provides two PoE module connectors, P17 and P18, to plug a Digi PoE module (DG-ACC-POE). The PoE module is an optional accessory item that can be plugged on the development board through the two connectors.

- P17, input connector: provides access to the PoE signals from the Ethernet connector
- P18, output connector: provides the output power supply from the PoE module

The PoE Module

Plug in the PoE module at a right angle to the development board, as shown in the picture below.

Note: the PoE module is part of the optional Digi 802.3af application kit (sold separately, Digi P/N DG-ACC-POE).



PoE Connector (power in), P17

The table below provides the pinout of the PoE input connector:

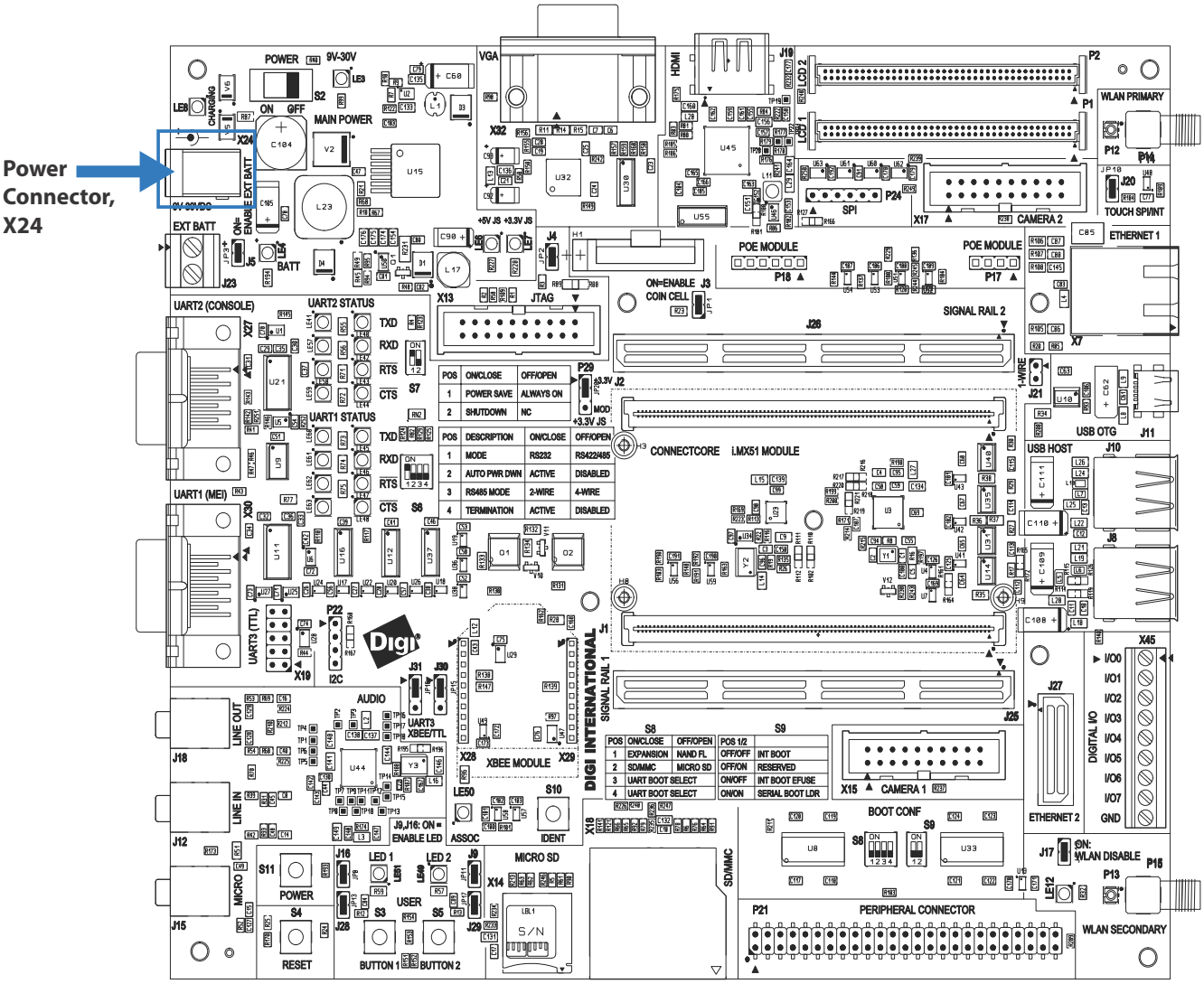
Pin	Signal
1	POE_TX_CT
2	POE_RX_CT
3	POE_RJ45_4/5
4	POE_RJ45_7/8

PoE Connector (power out), P18

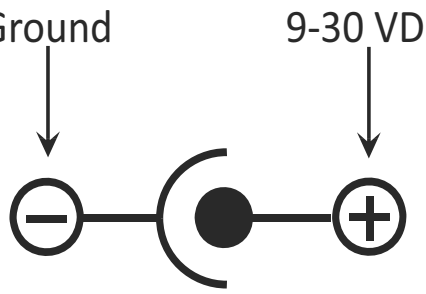
The table below provides the pinout of the PoE output connector:

Pin	Signal
1	+12V_PoE
2	+12V_PoE
3	GND
4	GND
5	PoE_GND
6	PoE_GND

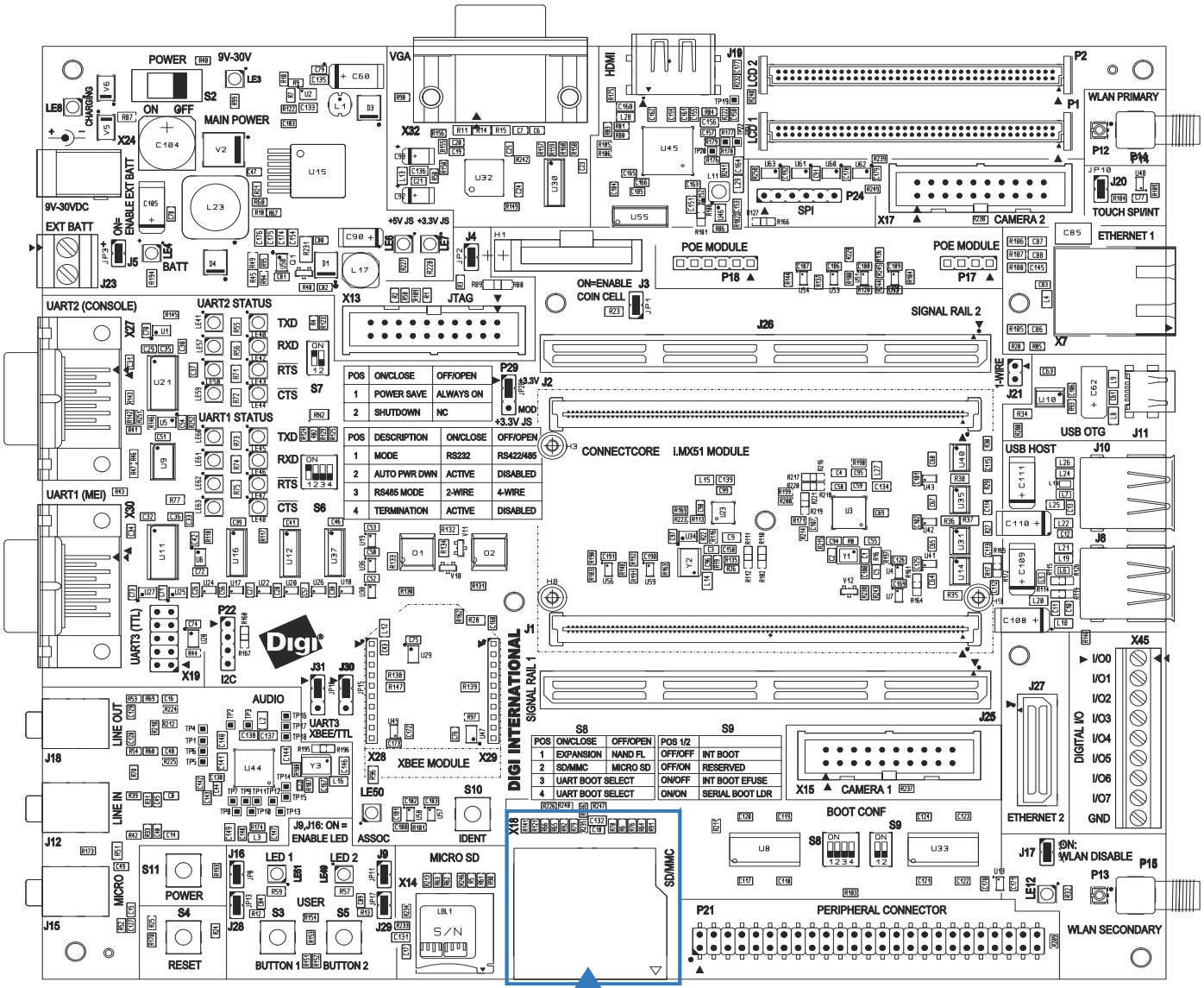
Main Power Connector



The main power connector (X24) is a barrel connector for the development board's 9-30VDC power supply. The figure below shows the polarity.



SD-Card Interface



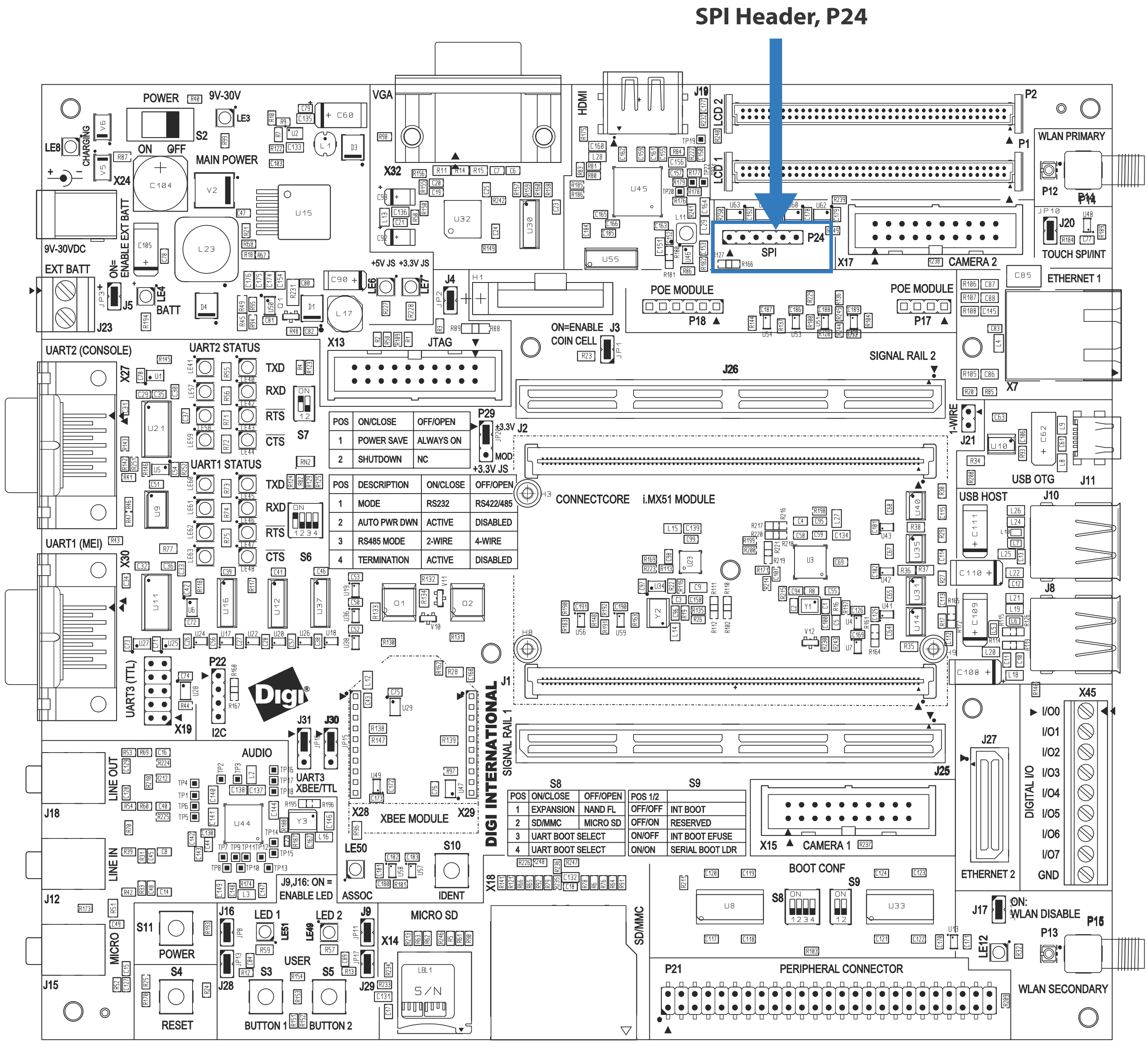
SD/MMC Connector, X18

The development board provides one SD/MMC card connector, X18. This interface is connected to the enhanced Secured Digital Host controller 3 (eSDHC3) of the i.MX51 CPU.

The following table provides the pinout of the SD/MMC connector:

Pin	Function
1	SD_DATA3
2	SD_CMD#
3	GND
4	+3.3V
5	SD_CLK
6	GND
7	SD_DATA0
8	SD_DATA1
9	SD_DATA2
10	SD_DATA4
11	SD_DATA5
12	SD_DATA6
13	SD_DATA7
14	SD_CD#
15	SD_WP#

SPI Interface



SPI Header, P24

The development board provides access to the SPI interface on the module using the SPI header, P24. This interface is connected to i.MX51 ECSPI1 port.

The SPI bus is connected to the following interfaces on the development board:

Interface	Chip Select
SPI Header	CSPI1_SS1/GPIO4_25
LCD1	GPIO4_26 (*)
LCD2	GPIO4_26 (*)

(*) the SPI chip select signal for the two LCD interfaces is generated with a logic combination of GPIO4_26 and the touch selection jumper (J20).

The SPI bus is connected to the following interfaces of the ConnectCore for i.MX51 module.

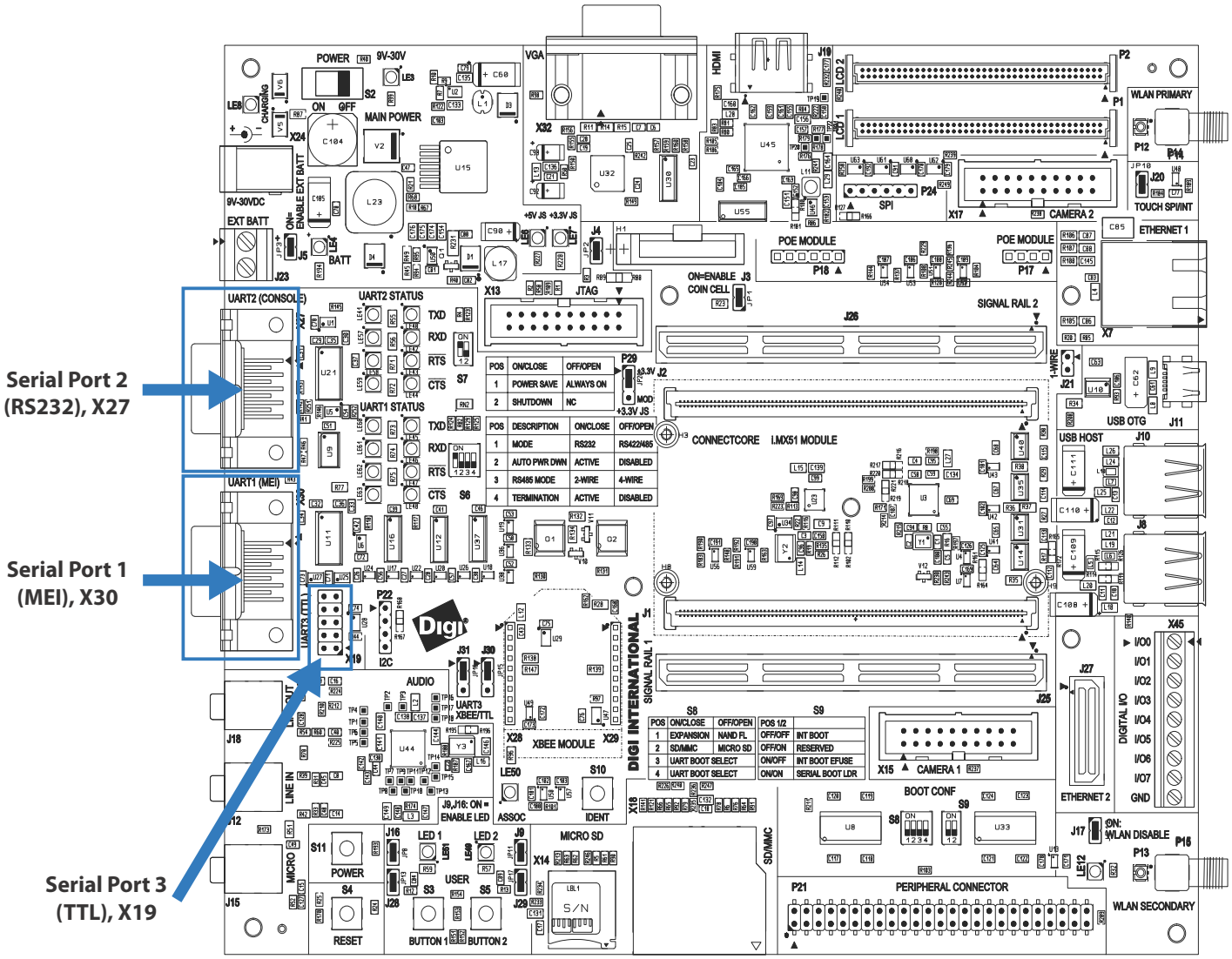
Interface	Chip Select
MC13892 Power Management	CSPI1_SS0/GPIO4_24

The table below provides the pinout of the SPI header:

Pin	Function	Defaults to
1	+2.775V	
2	SPI_MOSI/GPIO4_22	GPIO4_22
3	SPI_MISO/GPIO4_23	GPIO4_23
4	SPI_SCLK/GPIO4_27	GPIO4_27
5	SPI_SS1/GPIO4_25	GPIO4_25
6	GND	

By default, SPI pins are configured as GPIO signals.

UART Interface



Serial Port 2, RS232, X27

The serial (UART) port 2 connector, X27, is a DB-9 male connector, which is also used as the standard console port. This asynchronous serial port is operating in DTE mode and requires a null-modem cable to connect to a computer serial port.

The serial port 2 interface is connected to i.MX51 UART port 2. The corresponding line driver on the development board can be enabled or disabled using switch S7. Refer to paragraph "Switches and Push-buttons" in this document for more information.

Serial port 2 pins are allocated as shown:

Pin	Function	Defaults to
1	NC	-
2	RXD	GPIO1_20
3	TXD	GPIO1_21
4	NC	-
5	GND	-
6	NC	-
7	RTS#	GPIO1_14
8	CTS#	GPIO1_11
9	NC	-

By default, serial port 2 signals are configured as GPIO signals.

Serial Port 1, MEI Interface, X30

The serial (UART) port 1 connector, X30, is a DB-9 male connector. This asynchronous serial port is operating in DTE mode and requires a null-modem cable to connect to a computer serial port.

The serial port 1 MEI (multiple electrical interface) interface corresponds to i.MX51 UART port 1. The line drivers are configured using the switch S6. Refer to the "Switches and Push-buttons" section of this document for more information.

Serial port 1 pins are allocated as shown:

Pin	RS232 Function	RS232 Default	RS485 Function	RS485 Default
1	-	-	CTS-	-
2	RXD	GPIO4_28	RX+	GPIO4_28
3	TXD	GPIO4_29	TX+	GPIO4_29
4	-	-	RTS-	-
5	GND	-	GND	-
6	-	-	RX-	-
7	RTS#	GPIO4_30	RTS+	GPIO4_30
8	CTS#	GPIO4_31	CTS+	GPIO4_31
9	-	-	TX-	-