ConnectCore™ for i.MX53™ Hardware Reference

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Using this Guide

This guide provides information about the Digi ConnectCore for i.MX53 embedded core module family.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This convention	Is used for
italic type	Emphasis, new terms, variables, and document titles.
monospaced type	Filenames, pathnames, and code examples.

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Additional Resources

Please also refer to the most recent Freescale i.MX53 Application Processor Reference Manual (IMX53RM) and related documentation for additional information.

About the Module

CHAPTER 1

The network-enabled ConnectCore for i.MX53 is a highly integrated and future-proof System-on-Module (SOM) solution based on the new Freescale® i.MX535/i.MX536 application processor with a high-performance ARM® Cortex-A8® core, powerful multimedia options, and a complete set of peripherals.

The module combines the fast integration, reliability and design flexibility of an off-the-shelf SOM with complete out-of-the-box software development support for platforms such as Microsoft® Windows® Embedded CE 7.0, Digi® Embedded Linux ®, Timesys® LinuxLink®, and Android™.

With industry-leading performance and key features like a dual-display interface and a hardware encryption engine, the module is the ideal choice for a broad range of target markets including medical, digital signage, security/access control, retail, industrial/ building automation, transportation and more.

Complete and cost-efficient Digi JumpStart Kits™ for Microsoft Windows Embedded Compact 7.0, Linux and Android allow immediate and professional embedded product development with dramatically reduced design risk and time-to-market.

Features and Functionality

The ConnectCore for i.MX53 module is based on the i.MX53 processor from Freescale. This processor offers a high number of interfaces. Most of these interfaces are multiplexed and are not available simultaneously. The module has the following features:

- High-end, low-power 32-bit System-on-Module
- Freescale i.MX535/i.MX536 processor
  - Cortex-A8 at 1GHz/800 MHz
  - 32Kbyte L1 instruction and 32Kbyte L1 data cache
  - 256Kbyte L2 cache
  - NEON coprocessor
  - Vector Floating Point (VFP) unit
- SLC and MLC NAND flash support on module
- Up to 2GB 32-bit/200 MHz DDR2-800 memory
- Dialog DA9053 Power Manager IC
  - Programmable battery charger
  - 4 buck converters and 10 LDO's to supply processor and peripherals
  - RTC counter with Coin Cell input
  - White LED driver boost for three LED strings
  - ADC and touch screen interface
- Debug interfaces
  - Standard JTAG controller IEEE 1149.1
  - ETM/ETB
- SAHARA Security co-processor that includes
  - Encryption (AES, DES and 3DES)
  - Hashing algorithms (MD5, SHA-1, SHA-224 and SHA-256)
  - Cipher algorithm (ARC4)
  - Hardware random number generator
- RTC
- Timer
- Two watchdog timers
- Up to 5 UART ports, up to 4Mbps each
- Up to 3 SPIs, (two of them up to 54Mbps each)
- Up to 3 I^2Cs (up to 400Kbps)
- SATA controller
- 2 controller area network (FLEXCAN), 1Mbps each

- 8/16-bit external memory interface
- 4 memory card interfaces (3 for the wireless version of the module)
  - SD/SDIO - 1 and 4-bits (up to 200Mbps)
  - MMC - 1, 4 and 8-bits (up to 416Mbps)
- USB
  - Up tp 3x USB 2.0 high-speed USB Host ports
  - 1 USB Host with integrated high-speed PHY
  - 1 high-speed USB 2.0 on-the-go USB port with integrated PHY
- 2 parallel camera ports
- Display
  - 5 interfaces available. Total rate of all interfaces is up to 180Mpixels/sec, 24 bits per pixel. Up to 2 interfaces may be active at once.
  - 2x parallel 24-bit display ports up to 165Mpixels/sec (UXGA@60Hz)
  - 2x LVDS serial ports. 1 port up to 165Mpixels/sec or 2 ports (WXGA@60Hz) each
  - 1 TV-out/VGA port up to 150Mpixels/sec (1080p at 60Hz)
- 4-wire resistive touch screen with pen pressure measurement
- SPDIF output
- 3 I^2S/AC97/SSI, up to 1.4Mbps each connected to Audio Multiplexer providing 4 external ports
- 1-wire interface
- Keypad port
- Up to 4 independent PWM interfaces
- GPIO with interrupt capabilities
- Up to 3x 10-bit ADC channels
- On-module three axis accelerometer (optional)
- On-module 10/100 Ethernet controller (optional)
- Second on-module 10/100Mbit Ethernet interface (optional)
- 2.4GHz & 5GHz IEEE 802.11a/b/g/n wireless LAN interface (optional)
  - Future 802.11abgn + Bluetooth 4.0 option
- Complete Microsoft Windows Embedded Compact 7, Linux and Android platform support with BSP source code

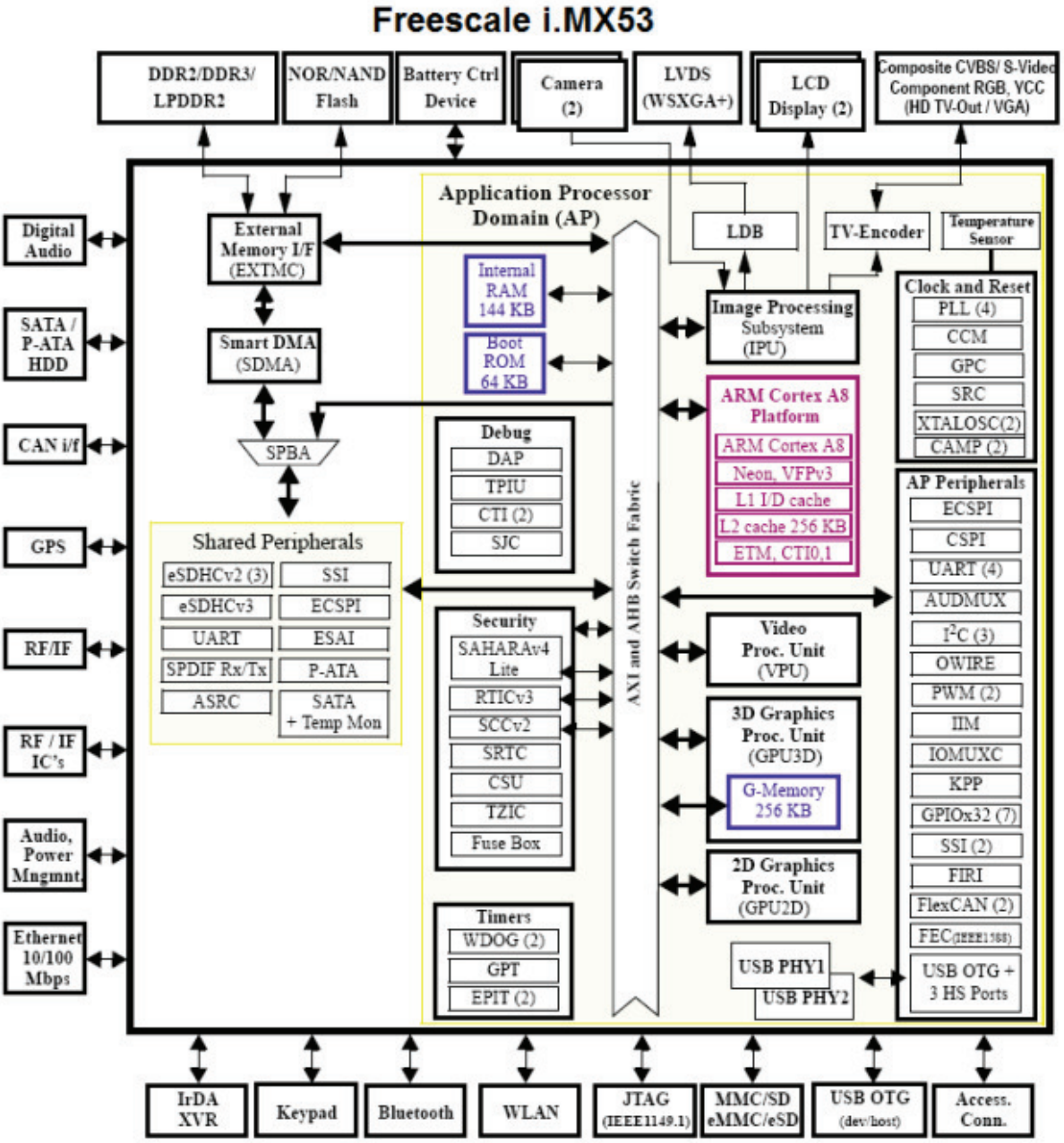
Module Variant

The ConnectCore for i.MX53 module is available with various population options such as network interfaces (Ethernet, WLAN), memory (flash, RAM), processor (speed grade/ operating temperature) and others.

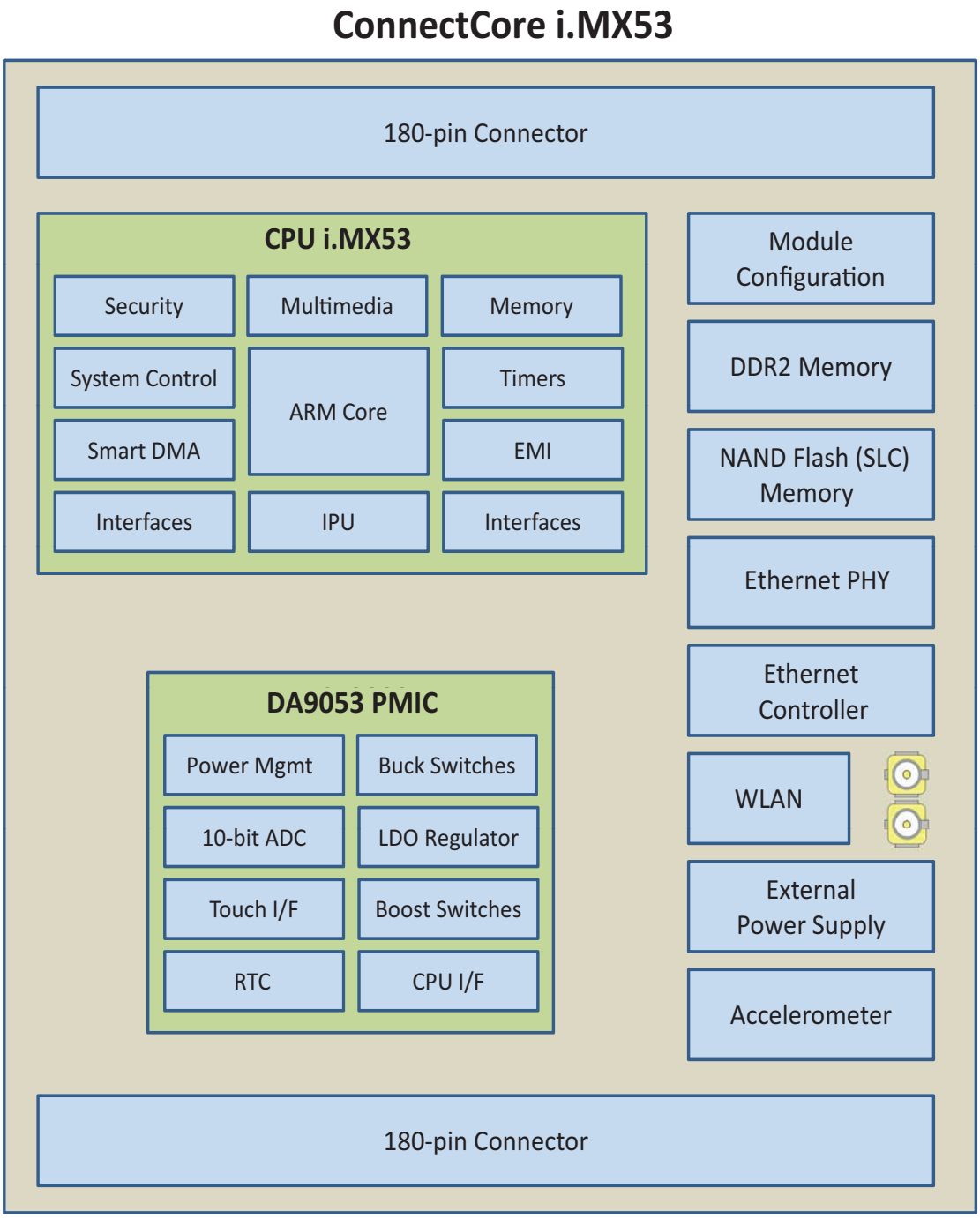
Block Diagram

The following figures show the block diagram of the Freescale i.MX535 CPU and the block diagram of the ConnectCore for i.MX53 module.

CPU



Module



Module Pinout

The module has two 180-pin connectors, J1 and J2. The following tables describe each pin, its properties, and its use on the module and development board. The DC parameters for each I/O type are defined in the "I/O DC Parameters" section of Appendix A - Module Specifications.

The ‘Use on module’ column shows the connection of the signals on the module. The format of this column is *component: pad_name*, where ‘component’ indicates the connected component on the module, and ‘pad_name’ indicates the corresponding component signal (per datasheet).

Pinout Legend

#	Low level active signal
NC	Pin not connected on module

Pinout Definitions

GPIO - General Purpose IO

UHVIO - Ultra High Voltage IO

HSGPIO - High Speed GPIO

LVIO - Low Voltage IO (meaning 1.8V)

I/O Type descriptions can be read as follows:

- 18 - 1.8V logic level switching (for example, GPIO18)
- 27 - 2.775V logic level switching (for example, GPIO27)
- 31 - 3.15V logic level switching (for example, UHVIO31)
- 33 - 3.3V logic level switching (for example, UHVIO33)

J1 Pinout

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
1	UHVIO27	KEY_COL7/GPIO5_26	i.MX53: CSI0_D8	Camera 2 reset (default) / Keypad column 7	Repeated pin (J2-96)
2	UHVIO27	KEY_ROW7/GPIO5_27	i.MX53: CSI0_D9	Camera 1 reset (default) / Keypad row 7	Repeated pin (J2-99)
3	UHVIO27	GPIO5_28	i.MX53: CSI0_D10	PEN_IRQ#	
4	UHVIO27	GPIO5_29	i.MX53: CSI0_D11	USB_HUB_RESET#	
5	UHVIO27	CSI0_D12	i.MX53: CSI0_D12	Camera 1 data	
6	UHVIO27	CSI0_D13	i.MX53: CSI0_D13	Camera 1 data	
7	UHVIO27	CSI0_D14	i.MX53: CSI0_D14	Camera 1 data	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
8	UHVIO27	CSI0_D15	i.MX53: CSI0_D15	Camera 1 data	
9	UHVIO27	CSI0_D16	i.MX53: CSI0_D16	Camera 1 data	
10	UHVIO27	CSI0_D17	i.MX53: CSI0_D17	Camera 1 data	
11	UHVIO27	CSI0_D18	i.MX53: CSI0_D18	Camera 1 data	
12	UHVIO27	CSI0_D19	i.MX53: CSI0_D19	Camera 1 data	
13	UHVIO27	CSI0_VSYNC	i.MX53: CSI0_VSYNC	Camera 1 vertical sync	
14	UHVIO27	CSI0_HSYNC	i.MX53: CSI0_MCLK	Camera 1 horizontal sync	
15	UHVIO27	CSI0_PIXCLK	i.MX53: CSI0_PIXCLK	Camera 1 pixel clock	
16	UHVIO27	CSI0_MCLK	i.MX53: GPIO1_0	Camera 1 & 2 master clock	SSI1_EXT_CLK used as master clock for both cameras Repeated pin (J2-136)
17	GROUND	GND	-	-	
18	GROUND	GND	-	-	
19	WLAN	WLAN_TDO	WLAN: TDO	Not used	
20	WLAN	WLAN_TCK	WLAN: TCK	Not used	
21	WLAN	WLAN_TDI	WLAN: TDI	Not used	
22	WLAN	WLAN_TMS	WLAN: TMS	Not used	
23	WLAN	WLAN_LED	WLAN: LED_ON	WLAN_LED	
24	WLAN	RS_BT_PRIORITY	WLAN: BT_PRIORITY	Not used	
25	WLAN	RS_WLAN_ACTIVE	WLAN: WLAN_ACTIVE	Not used	
26	WLAN	RS_BT_ACTIVE	WLAN: BT_ACTIVE	Not used	
27	LVIO	BOOT_MDE0	i.MX53: BOOT_MODE0	Boot mode selection	10K pull-down on module
28	WLAN	WLAN_DISABLE#	WLAN power supply switch	WLAN disable jumper (J17)	This signal switches ON/OFF the power supply of WLAN
29	LVIO	BOOT_MODE1	i.MX53: BOOT_MODE1	Boot mode selection	10K pull-down on module
30	POWER	VBAT	PMIC: VBAT	Battery supply	
31	POWER	VBAT	PMIC: VBAT	Battery supply	
32	POWER	VCHRG	PMIC: DCIN	Charger supply	
33	POWER	+2.775V	PMIC: VLDO9	-	
34	POWER	VCHRG	PMIC: DCIN	Charger supply	
35	POWER	+2.775V	PMIC: VLDO9	-	
36	POWER	+2.775V	PMIC: VLDO9	-	
37	PMIC_IO1 PMIC_IO2	PMIC_GPIO8	PMIC: GPIO8	Not used	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
38	POWER	+2.775V	PMIC: VLDO9	-	
39	VDDCORE PMIC_IO2	PMIC_ONKEY#	PMIC: ONKEY#	Power ON button (S13)	10K pull-up on module to VDDCORE
40	PMIC_IO1 PMIC_IO2	PMIC_GPIO13	PMIC: GPIO13	Not used	
41	PMIC_IO1 PMIC_IO2	PMIC_IRQ#/JTAG_DE#	PMIC: IRQ# i.MX53: GPIO7_11	Not used	10K pull-up on module to +2.775V
42	PMIC_IO1 PMIC_IO2	PMIC_GPIO9	PMIC: GPIO9 +3.3V_EXT: Enable	Power enable	GPIO used to enable external power supplies
43	-	NC	-	-	
44	PMIC_IO1 PMIC_IO2	PMIC_PWR_UP	PMIC: PWR_UP	Not used	
45	-	NC	-	-	
46	POWER	VCC_COINCELL	PMIC: VBBAT	Coincell	
47	POWER	VBAT	PMIC: VBAT	Battery supply	
48	POWER	VCHRG	PMIC: DCIN	Charger supply	
49	POWER	VBAT	PMIC: VBAT	Battery supply	
50	POWER	VCHRG	PMIC: DCIN	Charger supply	
51	POWER	VBAT	PMIC: VBAT	Battery supply	
52	POWER	VCHRG	PMIC: DCIN	Charger supply	
53	ETH	ETH1_TX+	ETH_PHY: TXP	Ethernet 1	
54	ETH	ETH1_RX+	ETH_PHY: RXP	Ethernet 1	
55	ETH	ETH1_TX-	ETH_PHY: TXN	Ethernet 1	
56	ETH	ETH1_RX-	ETH_PHY: RXN	Ethernet 1	
57	GROUND	GND	-	-	
58	UHVIO27	ETH1_LINK	EHT_PHY: LED1	Ethernet 1 Link LED	
59	-	NC	-	-	
60	UHVIO27	ETH1_ACTIVITY	ETH_PHY: LED2	Ethernet 1 Activity LED	
61	-	NC	-	-	
62	GPIO	GPIO4_O	i.MX53: GPIO4_0	User Key 1	
63	LVDS	LVDS0_CLK_N	i.MX53: LVDS0_CLK_N	LVDS 0 clock	
64	UHVIO27	KEY_COL7/GPIO5_26	i.MX53: CSI0_D8	Camera 2 reset (default) / Keypad column 7	Repeated pin (J1-1)
65	LVDS	LVDS0_CLK_P	i.MX53: LVDS0_CLK_P	LVDS 0 clock	
66	LVDS	LVDS1_CLK_N	i.MX53: LVDS1_CLK_N	Not used	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
67	LVDS	LVDS0_TXD0_N	i.MX53: LVDS0_TXD0_N	LVDS 0 data	
68	LVDS	LVDS1_CLK_P	i.MX53: LVDS1_CLK_P	Not used	
69	LVDS	LVDS0_TXD0_P	i.MX53: LVDS0_TXD0_P	LVDS 0 data	
70	LVDS	LVDS1_TXD0_N	i.MX53: LVDS1_TXD0_N	Not used	
71	LVDS	LVDS0_TXD1_N	i.MX53: LVDS0_TXD1_N	LVDS 0 data	
72	LVDS	LVDS1_TXD0_P	i.MX53: LVDS1_TXD0_P	Not used	
73	LVDS	LVDS0_TXD1_P	i.MX53: LVDS0_TXD1_P	LVDS 0 data	
74	LVDS	LVDS1_TXD1_N	i.MX53: LVDS1_TXD1_N	Not used	
75	LVDS	LVDS0_TXD2_N	i.MX53: LVDS0_TXD2_N	LVDS 0 data	
76	LVDS	LVDS1_TXD1_P	i.MX53: LVDS1_TXD1_P	Not used	
77	LVDS	LVDS0_TXD2_P	i.MX53: LVDS0_TXD2_P	LVDS 0 data	
78	LVDS	LVDS1_TXD2_N	i.MX53: LVDS1_TXD2_N	Not used	
79	LVDS	LVDS0_TXD3_N	i.MX53: LVDS0_TXD3_N	LVDS 0 data	
80	LVDS	LVDS1_TXD2_P	i.MX53: LVDS1_TXD2_P	Not used	
81	LVDS	LVDS0_TXD3_P	i.MX53: LVDS0_TXD3_P	LVDS 0 data	
82	GROUND	GND	-	-	
83	RGB	IOR	i.MX53: IOR	VGA	
84	LVDS	LVDS1_TXD3_N	i.MX53: LVDS1_TXD3_N	Not used	
85	RGB	IOR_BACK	i.MX53: IOR_BACK	VGA	
86	LVDS	LVDS1_TXD3_P	i.MX53: LVDS1_TXD3_P	Not used	
87	RGB	IOB	i.MX53: IOB	VGA	
88	RGB	IOG	i.MX53: IOG	VGA	
89	RGB	IOB_BACK	i.MX53: IOB_BACK	VGA	
90	RGB	IOG_BACK	i.MX53: IOG_BACK	VGA	
91	GPIO18	JTAG_TCK	i.MX53: JTAG_TCK	JTAG	10K pull-up on module
92	GPIO18	JTAG_TRST#	i.MX53: JTAG_TRSTB	JTAG	10K pull-up on module
93	GPIO18	JTAG_TMS	i.MX53: JTAG_TMS	JTAG	10K pull-up on module
94	GPIO18	JTAG_MOD#	i.MX53: JTAG_MOD	Jumper J4	
95	GPIO18	JTAG_TDI	i.MX53: JTAG_TDI	JTAG	10K pull-up on module
96	GPIO27	PMIC_IRQ#/JTAG_DE#	PMIC: IRQ# i.MX53: GPIO7_11	Not used	Repeated pin (J1-41)
97	GPIO18	JTAG_TDO	i.MX53: JTAG_TDO	JTAG	
98	LVIO	RESET_IN#	i.MX53: RESET_IN_B	Not used	10K pull-up on module

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
99	LVIO	POR#	i.MX53: POR_B PMIC: RESET_OUT#	Parallel LCD, JTAG, Reset button (S12)	10K pull-up on module
100	POWER	+1.8V	PMIC: VLDO8 PMIC: VDD_IO2	-	
101	GROUND	GND	-	-	
102	GROUND	GND	-	-	
103	ETH	ETH2_TX+	ETH_CTRL: TPO+	Ethernet 2	
104	ETH	ETH2_RX+	ETH_CTRL: TPI+	Ethernet 2	
105	ETH	ETH2_TX-	ETH_CTRL: TPO-	Ethernet 2	
106	ETH	ETH2_RX-	ETH_CTRL: TPI-	Ethernet 2	
107	-	NC	-	-	
108	-	NC	-	-	
109	-	NC	-	-	
110	-	NC	-	-	
111	GPIO18	ETH2_ACTIVITY#	ETH_CTRL: LED2#	Ethernet 2 Activity LED	
112	GPIO18	ETH2_LINK#	ETH_CTRL: LED1#	Ethernet 2 Link LED	
113	UHVIO18	EIM_CS0	i.MX53: EIM_CS0	Peripheral connector (EIM_CS0)	
114	UHVIO18	LAN9221_CS#	i.MX53: EIM_CS1 ETH_CTRL: CS#	Not used	
115	-	NC	-	-	
116	-	NC	-	-	
117	-	NC	-	-	
118	-	NC	-	-	
119	-	NC	-	-	
120	UHVIO18	EIM_LBA/GPIO2_27	i.MX53: EIM_LBA	Not used	10K pull-up on module
121	UHVIO18	EIM_DA0	i.MX53: EIM_DA0 ETH_CTRL: A1	Peripheral connector (EIM_DA0)	10K pull-down on module
122	UHVIO18	EIM_DA1	i.MX53: EIM_DA1 ETH_CTRL: A2	Peripheral connector (EIM_DA1)	10K pull-down on module
123	UHVIO18	EIM_DA2	i.MX53: EIM_DA2 ETH_CTRL: A3	Peripheral connector (EIM_DA2)	10K pull-up on module
124	UHVIO18	EIM_DA3	i.MX53: EIM_DA3 ETH_CTRL: A4	Peripheral connector (EIM_DA3)	10K pull-up on module
125	GROUND	GND	-	-	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
126	UHVIO18	EIM_DA5	i.MX53: EIM_DA5 ETH_CTRL: A6	Peripheral connector (EIM_DA5)	10K pull-down on module
127	UHVIO18	EIM_DA4	i.MX53: EIM_DA4 ETH_CTRL: A5	Peripheral connector (EIM_DA4)	10K pull-up on module
128	UHVIO18	EIM_DA7	i.MX53: EIM_DA7 ETH_CTRL: FIFO_SEL	Peripheral connector (EIM_DA7)	10K pull-down on module
129	UHVIO18	EIM_DA6	i.MX53: EIM_DA6 ETH_CTRL: A7	Peripheral connector (EIM_DA6)	10K pull-up on module
130	GROUND	GND	-	-	
131	UHVIO18	EIM_DA8	i.MX53: EIM_DA8	Peripheral connector (EIM_DA8)	10K pull-down on module
132	UHVIO18	EIM_DA9	i.MX53: EIM_DA9	Peripheral connector (EIM_DA9)	10K pull-down on module
133	UHVIO18	EIM_DA10/GPIO3_10	i.MX53: EIM_DA10	Not used	10K pull-up on module
134	UHVIO18	EIM_DA11/CSI1_HSYNC	i.MX53: EIM_DA11	VGA horizontal sync (default) Camera 2 horizontal sync	
135	GROUND	GND	-	-	
136	UHVIO18	EIM_DA13/GPIO3_13	i.MX53: EIM_DA13	Not used	
137	UHVIO18	EIM_DA12/CSI1_VSYNC	i.MX53: EIM_DA12	VGA vertical sync (default) Camera 2 vertical sync	
138	UHVIO18	EIM_DA15/GPIO3_15	i.MX53: EIM_DA15	Not used	
139	UHVIO18	EIM_DA14/GPIO3_14	i.MX53: EIM_DA14	Not used	
140	-	GND	-	-	
141	UHVIO18	EIM_D16	i.MX53: EIM_D16 ETH_CTRL: D0	Peripheral connector (EIM_D16)	
142	UHVIO18	EIM_D17	i.MX53: EIM_D17 ETH_CTRL: D1	Peripheral connector (EIM_D17)	
143	UHVIO18	EIM_D18	i.MX53: EIM_D18 ETH_CTRL: D2	Peripheral connector (EIM_D18)	
144	UHVIO18	EIM_D19	i.MX53: EIM_D19 ETH_CTRL: D3	Peripheral connector (EIM_D19)	
145	POWER	+3.15V	-	-	
146	UVHIO18	EIM_D21	i.MX53: EIM_D21 ETH_CTRL: D5	Peripheral connector (EIM_D21)	
147	UHVIO18	EIM_D20	i.MX53: EIM_D20 ETH_CTRL: D4	Peripheral connector (EIM_D20)	
148	UHVIO18	EIM_D23	i.MX53: EIM_D23 ETH_CTRL: D7	Peripheral connector (EIM_D23)	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
149	UHVIO18	EIM_D22	i.MX53: EIM_D22 ETH_CTRL: D6	Peripheral connector (EIM_D22)	
150	GROUND	GND	-	-	
151	UHVIO18	EIM_D24	i.MX53: EIM_D24 ETH_CTRL: D8	Peripheral connector (EIM_D24)	
152	UHVIO18	EIM_D25	i.MX53: EIM_D25 ETH_CTRL: D9	Peripheral connector (EIM_D25)	
153	UHVIO18	EIM_D26	i.MX53: EIM_D26 ETH_CTRL: D10	Peripheral connector (EIM_D26)	
154	UHVIO18	EIM_D27	i.MX53: EIM_D27 ETH_CTRL: D11	Peripheral connector (EIM_D27)	
155	GROUND	GND	-	-	
156	UHVIO18	EIM_D29	i.MX53: EIM_D29 ETH_CTRL: D13	Peripheral connector (EIM_D29)	
157	UHVIO18	EIM_D28	i.MX53: EIM_D28 ETH_CTRL: D12	Peripheral connector (EIM_D28)	
158	UHVIO18	EIM_D31	i.MX53: EIM_D31 ETH_CTRL: D15	Peripheral connector (EIM_D31)	
159	UHVIO18	EIM_D30	i.MX53: EIM_D30 ETH_CTRL: D14	Peripheral connector (EIM_D30)	
160	UHVIO18	EIM_A17/CSI1_D12	i.MX53: EIM_A17	Camera 2 data	10K pull-down on module
161	UHVIO18	EIM_A16/CSI1_PIXCLK	i.MX53: EIM_A16	Camera 2 pixel clock	10K pull-down on module
162	UHVIO18	EIM_A19/CSI1_D14	i.MX53: EIM_A19	Camera 2 data	10K pull-down on module
163	UHVIO18	EIM_A18/CSI1_D13	i.MX53: EIM_A18	Camera 2 data	10K pull-up on module
164	UHVIO18	EIM_A21/CSI1_D16	i.MX53: EIM_A21	Camera 2 data	10K pull-down on module
165	UHVIO18	EIM_A20/CSI1_D15	i.MX53: EIM_A20	Camera 2 data	10K pull-down on module
166	UHVIO18	EIM_A23/CSI1_D18	i.MX53: EIM_A23	Camera 2 data	
167	UHVIO18	EIM_A22/CSI1_D17	i.MX53: EIM_A22	Camera 2 data	10K pull-up on module
168	UHVIO18	EIM_A25/GPIO5_2	i.MX53: EIM_A25	HDMI_INT#	
169	UHVIO18	EIM_A24/CSI1_D19	i.MX53: EIM_A24	Camera 2 data	
170	-	NC	-	-	
171	-	NC	-	-	
172	UHVIO18	EIM_OE#	i.MX53: EIM_OE ETH_CTRL: RD#	Peripheral connector (EIM_OE#)	
173	UHVIO18	EIM_EB0/GPIO2_28	i.MX53: EIM_EB0	Not used	10K pull-down on module

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
174	UHVIO18	EIM_RW#	i.MX53: EIM_RW ETH_CTRL: WR#	Peripheral connector (EIM_RW#)	
175	UHVIO18	EIM_EB1/GPIO2_29	i.MX53: EIM_EB1	Not used	10K pull-up on module
176	-	NC	-	-	
177	UHVIO18	EIM_EB2	i.MX53: EIM_EB2	Peripheral connector (EIM_EB2)	
178	UHVIO18	EIM_WAIT/GPIO5_0	i.MX53: EIM_WAIT	Peripheral connector (EIM_IRQ)	
179	UHVIO18	EIM_EB3	i.MX53: EIM_EB3	Peripheral connector (EIM_EB3)	
180	UHVIO18	EIM_BCLK	i.MX53: EIM_BCLK	Peripheral connector (EIM_BCLK)	By default, not connected on development board

J2 Pinout

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
1	GPIO27	DISP0_DAT0	i.MX53: DISP0_DAT0	Parallel LCD, HDMI	
2	GPIO27	DISP0_DAT1	i.MX53: DISP0_DAT1	Parallel LCD, HDMI	
3	GPIO27	DISP0_DAT2	i.MX53: DISP0_DAT2	Parallel LCD, HDMI	
4	GPIO27	DISP0_DAT3	i.MX53: DISP0_DAT3	Parallel LCD, HDMI	
5	GPIO27	DISP0_DAT4	i.MX53: DISP0_DAT4	Parallel LCD, HDMI	
6	GPIO27	DISP0_DAT5	i.MX53: DISP0_DAT5	Parallel LCD, HDMI	
7	GPIO27	DISP0_DAT6	i.MX53: DISP0_DAT6	Parallel LCD, HDMI	
8	GPIO27	DISP0_DAT7	i.MX53: DISP0_DAT7	Parallel LCD, HDMI	
9	GPIO27	DISP0_DAT8	i.MX53: DISP0_DAT8	Parallel LCD, HDMI	
10	GPIO27	DISP0_DAT9	i.MX53: DISP0_DAT9	Parallel LCD, HDMI	
11	GPIO27	DISP0_DAT10	i.MX53: DISP0_DAT10	Parallel LCD, HDMI	
12	GPIO27	DISP0_DAT11	i.MX53: DISP0_DAT11	Parallel LCD, HDMI	
13	GPIO27	DISP0_DAT12	i.MX53: DISP0_DAT12	Parallel LCD, HDMI	
14	GPIO27	DISP0_DAT13	i.MX53: DISP0_DAT13	Parallel LCD, HDMI	
15	GPIO27	DISP0_DAT14	i.MX53: DISP0_DAT14	Parallel LCD, HDMI	
16	GPIO27	DISP0_DAT15	i.MX53: DISP0_DAT15	Parallel LCD, HDMI	
17	GPIO27	DISP0_DAT16	i.MX53: DISP0_DAT16	Parallel LCD, HDMI	
18	GPIO27	DISP0_DAT17	i.MX53: DISP0_DAT17	Parallel LCD, HDMI	
19	GPIO27	DISP0_DAT18	i.MX53: DISP0_DAT18	Parallel LCD, HDMI	
20	GPIO27	DISP0_DAT19	i.MX53: DISP0_DAT19	Parallel LCD, HDMI	
21	GPIO27	DISP0_DAT20	i.MX53: DISP0_DAT20	Parallel LCD, HDMI	
22	GPIO27	DISP0_DAT21	i.MX53: DISP0_DAT21	Parallel LCD, HDMI	
23	GPIO27	DISP0_DAT22	i.MX53: DISP0_DAT22	Parallel LCD, HDMI	
24	GPIO27	DISP0_DAT23	i.MX53: DISP0_DAT23	Parallel LCD, HDMI	
25	GPIO27	DISP0_PIN2	i.MX53: DI0_PIN2	Parallel LCD, HDMI, VGA	Display 0 HSYNC
26	GROUND	GND	-	-	
27	PMIC_IO1 PMIC_IO2	PMIC_GPIO14/PMW1	PMIC: GPIO14	Parallel LCD, PWM connector	
28	GPIO27	DI0_DISP_CLK	i.MX53: DI0_DISP_CLK	Parallel LCD, HDMI	
29	GPIO27	GPIO4_20	i.MX53: DI0_PIN4	Parallel LCD	
30	GPIO27	DISP0_PIN3	i.MX53: DI0_PIN3	Parallel LCD, HDMI, VGA	Display 0 VSYNC

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
31	GPIO27	DISP0_PIN15	i.MX53: DI0_PIN15	Parallel LCD, HDMI	Display 0 DRDY
32	PMIC_IO1 PMIC_IO2	PMIC_GPIO15/PMW2	PMIC: GPIO15	LVDS, PWM connector	
33	-	SATA_TXM	i.MX53: SATA_TXM	SATA	
34	-	SATA_TXP	i.MX53: SATA_TXP	SATA	
35	-	SATA_RXM	i.MX53: SATA_RXM	SATA	
36	-	SATA_RXP	i.MX53: SATA_RXP	SATA	
37	-	NC	-	-	
38	-	NC	-	-	
39	PMIC_TOUCH	TOUCH_X1	PMIC: TSIXN	Parallel LCD, LVDS	
40	PMIC_ADC	ADIN4	PMIC: ADCIN4	Not used	10K pull-up on module to VDDCORE
41	PMIC_TOUCH	TOUCH_X2	PMIC: TSIXP	Parallel LCD, LVDS	
42	PMIC_ADC	ADIN5	PMIC: ADCIN5	Not used	10K pull-up on module to VDDCORE
43	PMIC_TOUCH	TOUCH_Y1	PMIC: TSIYN	Parallel LCD, LVDS	
44	PMIC_ADC	ADIN6	PMIC: ADCIN6	Not used	
45	PMIC_TOUCH	TOUCH_Y2	PMIC: TSIYP	Parallel LCD, LVDS	
46	-	NC	-	-	
47	GROUND	GND	-	-	
48	-	NC	-	-	
49	-	NC	-	-	
50	GROUND	LED1_IN	PMIC: LED1_IN	Parallel LCD	Current sink inputs
51	-	NC	-	-	
52	GROUND	LED2_IN	PMIC: LED2_IN	Not used	Current sink inputs
53	-	NC	-	-	
54	GROUND	LED3_IN	PMIC: LED3_IN	Not used	Current sink inputs
55	-	NC	-	-	
56	POWER	VSWLED	PMIC: SW_BOOST	Parallel LCD	LED driver
57	-	NC	-	-	
58	-	NC	-	-	
59	-	NC	-	-	
60	-	NC	-	-	
61	-	NC	-	-	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
62	-	NC	-	-	
63	-	NC	-	-	
64	-	NC	-	-	
65	-	NC	-	-	
66	-	NC	-	-	
67	-	NC	-	-	
68	GROUND	GND	-	-	
69	GROUND	GND	-	-	
70	-	USB_OTG_ID	i.MX53: USB_OTG_ID	USB OTG	
71	-	USB_OTG_DP	i.MX53: USB_OTG_DP	USB OTG	
72	-	USB_OTG_VBUS	i.MX53: USB_OTG_VBUS	USB OTG	
73	-	USB_OTG_DN	i.MX53: USB_OTG_DN	USB OTG	
74	UHVIO27	GPIO7_12	i.MX53: GPIO7_12	Not used	Repeated pin (J2-177)
75	GROUND	GND	-	-	
76	GPIO27	I2C3_SCL	iMX53: GPIO1_5 Accelerometer, PMIC	Peripheral connector, I^2C connector, parallel LCD, HDMI, Camera 1 & 2	2K2 pull-up on module to +2.775V
77	GPIO27	MMA7455_IRQ1/GPIO4_4	iMX53: GPIO4_4 Accelerometer	Not used	
78	GPIO27	I2C3_SDA	iMX53: GPIO1_6 Accelerometer, PMIC	Peripheral connector, I^2C connector, parallel LCD, HDMI, Camera 1 & 2	2K2 pull-up on module to +2.775V
79	GPIO27	MMA7455_IRQ2/GPIO4_3	iMX53: GPIO4_3	Audio headphone detection	
80	PMIC_IO1 PMIC_IO2	PMIC_OUT_32K	PMIC: OUT_32K	Not used	
81	GROUND	GND	-	-	
82	GROUND	GND	-	-	
83	-	CKIH1	i.MX53: CKIH1	Not used	
84	-	CKIH2	i.MX53: CKIH2	Not used	
85	UHVIO31	SDI_DATA0	i.MX53: SD1_DATA0 WLAN: SD_DATA0	Not used	
86	UHVIO31	SDI_CLK	i.MX53: SD1_CLK WLAN: SD_CLK	Not used	
87	UHVIO31	SDI_DATA1	i.MX53: SD1_DATA1 WLAN: SD_DATA1	Not used	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
88	UHVIO31	SDI_CMD	i.MX53: SD1_CMD WLAN: SD_CMD	Not used	
89	UHVIO31	SDI_DATA2	i.MX53: SD1_DATA2 WLAN: SD_DATA2	Not used	
90	UHVIO27	KEY_COL2	i.MX53: KEY_COL2	Keypad	
91	UHVIO31	SDI_DATA3	i.MX53: SD1_DATA3 WLAN: SD_DATA3	Not used	
92	UHVIO27	KEY_COL3	i.MX53: KEY_COL3	Keypad	
93	UHVIO27	KEY_ROW2	i.MX53: KEY_ROW2	Keypad	
94	UHVIO27	KEY_COL6/WDOG1#	i.MX53: GPIO1_9	Keypad	Repeated pin (J2-109)
95	UHVIO27	KEY_ROW3	i.MX53: KEY_ROW3	Keypad	
96	UHVIO27	KEY_COL7/GPIO5_26	i.MX53: CSI0_D8	Not used	Repeated pin (J1-1)
97	UHVIO27	KEY_ROW5	i.MX53: GPIO1_1	Keypad	
98	UHVIO27	UART3_CTS	i.MX53: PATA_DA_1	UART 3 connector, XBee	
99	UHVIO27	KEY_ROW7/GPIO5_27	i.MX53: CSI0_D9	Not used	Repeated pin (J1-2)
100	-	NC	-	-	
101	UHVIO31	UART3_RTS	i.MX53: PATA_DA_2	UART 3 connector, XBee	
102	GPIO27	GPIO4_1	i.MX53: GPIO4_1	User key 2	
103	UHVIO27	OWIRE_LINE	i.MX53: GPIO7_13	OWIRE EEPROM, OWIRE connector, iButton retainer	
104	UHVIO31	SD2_DATA0	i.MX53: SD2_DATA0	SD-card connector	
105	UHVIO31	SD2_CDM	i.MX53: SD2_CMD	SD-card connector	
106	UHVIO31	SD2_DATA1	i.MX53: SD2_DATA1	SD-card connector	
107	UHVIO31	SD2_CLK	i.MX53: SD2_CLK	SD-card connector	
108	UHVIO31	SD2_DATA2	i.MX53: SD2_DATA2	SD-card connector	
109	UHVIO27	KEY_COL6/WDOG1#	i.MX53: GPIO1_9	Not used	Repeated pin (J2-94)
110	UHVIO31	SD2_DATA3	i.MX53: SD2_DATA3	SD-card connector	
111	UHVIO27	CSPI1_MOSI	iMX53: CSI0_DAT5	Parallel LCD, LVDS, SPI conn	
112	UHVIO27	CSPI1_SS0	iMX53: CSI0_DAT7	Touch selection	
113	UHVIO27	CSPI1_MISO	iMX53: CSI0_DAT6	Parallel LCD, LVDS, SPI conn	
114	GPIO27	CSPI1_SS1	iMX53: DI0_PIN4	SPI connector	
115	UHVIO27	CSPI1_MCLK	iMX53: CSI0_DAT4	Parallel LCD, LVDS, SPI conn	
116	GPIO27	CSPI1_RDY	iMX53: GPIO4_5	Not used	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
117	UHVIO31	UART2_RXD	iMX53: PATA_BUFF_EN WLAN: UART	UART_MEI	By default disconnected from WLAN UART
118	UHVIO31	UART2_RTS#	iMX53: PATA_DIOR WLAN: UART	UART_MEI	By default disconnected from WLAN UART
119	UHVIO31	UART2_TXD	iMX53: PATA_DMARQ WLAN: UART	UART_MEI	By default disconnected from WLAN UART
120	UHVIO31	UART2_CTS#	iMX53: PATA_INTRQ WLAN: UART	UART_MEI	By default disconnected from WLAN UART
121	UHVIO31	UART1_RXD	iMX53: PATA_DMACK	UART 1, Status LED	
122	UHVIO31	UART3_RXD	iMX53: PATA_CS_1	UART 3, connector, XBee	
123	UHVIO31	UART1_TXD	iMX53: PATA_DIOW	UART 1, Status LED	
124	UHVIO31	UART3_TXD	iMX53: PATA_CS_0	UART 3, connector, XBee	
125	-	USB_H1_VBUS	iMX53: USB_H1_VBUS	USB Host	
126	GROUND	GND	-	-	
127	GROUND	GND	-	-	
128	UHVIO31	SD3_CMD/UART1_CTS	iMX53: PATA_RESET#	Console port	By default disconnected from console port. Repeated pin (J2-169).
129	-	USB_H1_DP	iMX53: USB_H1_DP	USB Host	
130	UHVIO27	CAN1_TXD	iMX53: GPIO1_7	CAN 1	
131	-	USB_H1_DN	iMX53: USB_H1_DN	USB Host	
132	UHVIO31	SD3_CLK/UART1_RTS	iMX53: PATA_IORDY	Console port	By default disconnected from console port. Repeated pin (J2-170).
133	GROUND	GND	-	-	
134	UHVIO27	CAN1_RXD	iMX53: GPIO1_8	CAN 1	
135	UHVIO27	MX53_ONKEY#/GPIO1_3	iMX53: GPIO1_3	Not used	
136	UHVIO27	CSI_MCLK	iMX53: CSI0_MCLK	Not used	Repeated pin (J1-16)
137	UHVIO27	AUD5-TXD	iMX53: KEY_ROW0	Audio CODEC, HDMI	
138	-	NC	-	-	
139	UHVIO27	AUD_5_RXD	iMX53: KEY_ROW1	Audio CODEC	
140	UHVIO27	CAN2_RXD	iMX53: KEY_ROW4	CAN 2	
141	UHVIO27	AUD5_TCK	iMX53: KEY_COL0	Audio CODEC, HDMI	22R serial resistor on module
142	UHVIO27	CAN2_TXD	iMX53: KEY_COL4	CAN 2	
143	POWER	+3.3V_MOD	-	-	

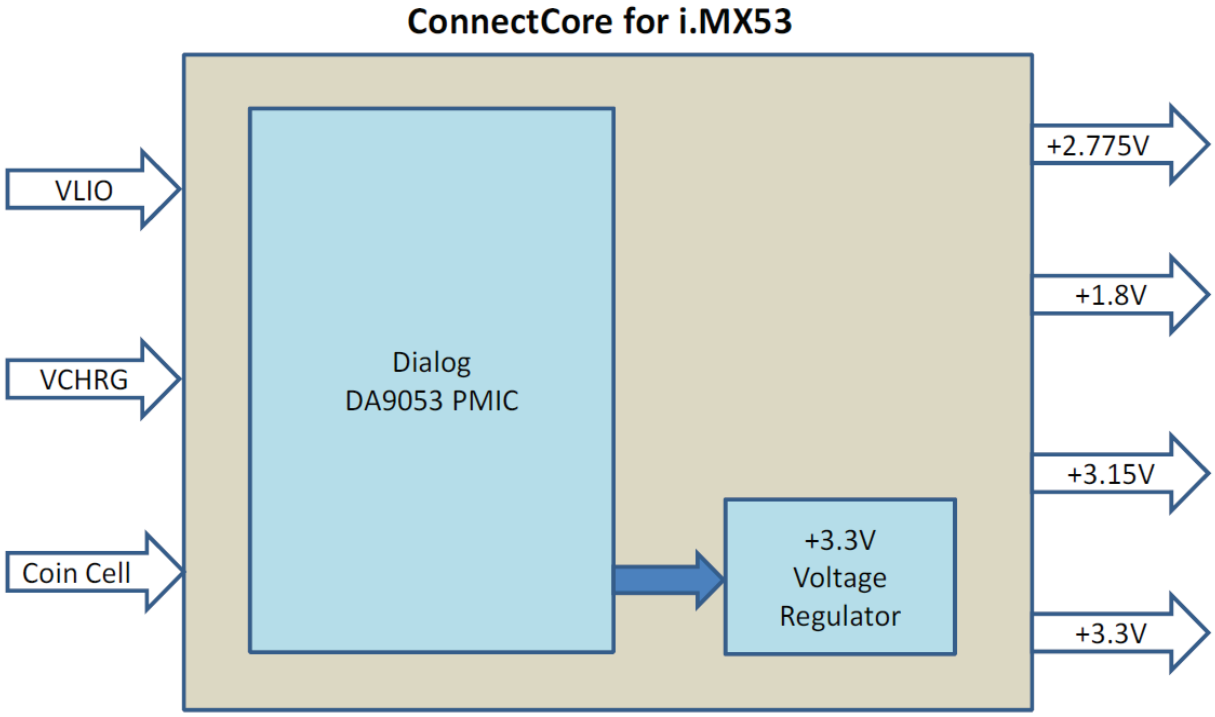
Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
144	UHVIO27	AUD5_TXFS	iMX53: KEY_COL1	Audio CODEC, HDMI	
145	UHVIO31	NANDF_D0	iMX53: PATA_DATA0 NAND flash: Data	Not used	
146	POWER	+3.3V_MOD	-	-	
147	UHVIO31	NANDF_D2	iMX53: PATA_DATA2 NAND flash: Data	Not used	
148	UHVIO31	NANDF_D1	iMX53: PATA_DATA1 NAND flash: Data	Not used	
149	UHVIO31	NANDF_D4	iMX53: PATA_DATA4 NAND flash: Data	Not used	
150	UHVIO31	NANDF_D3	iMX53: PATA_DATA3 NAND flash: Data	Not used	
151	UHVIO31	NANDF_D6	iMX53: PATA_DATA6 NAND flash: Data	Not used	
152	UHVIO31	NANDF_D5	iMX53: PATA_DATA5 NAND flash: Data	Not used	
153	UHVIO31	SD3_DATA0	iMX53: PATA_DATA8	micro SD card	
154	UHVIO31	NANDF_D7	iMX53: PATA_DATA7 NAND flash: Data	Not used	
155	UHVIO31	SD3_DATA2	iMX53: PATA_DATA10	micro SD card	
156	UHVIO31	SD3_DATA1	iMX53: PATA_DATA9	micro SD card	
157	UHVIO31	SD2_DATA4	iMX53: PATA_DATA12	SD card	
158	UHVIO31	SD3_DATA3	iMX53: PATA_DATA11	micro SD card	
159	UHVIO31	SD2_DATA6	iMX53: PATA_DATA14	SD card	
160	UHVIO31	SD2_DATA5	iMX53: PATA_DATA13	SD card	
161	UHVIO31	NANDF_CS0#	iMX53: NANDF_CS0 NAND flash: CS#	Not used	
162	UHVIO31	SD2_DATA7	iMX53: PATA_DATA15	SD card	
163	UHVIO31	GPIO6_15	iMX53: PATA_CS2 WLAN: GPIO Nand flash: NC	Dig IO connector, XBEE_RESET#	10K pull-up on module to +3.15V. By default, disconnected from WLAN.
164	GPIO27	GPIO1_2/SD2_WP#	iMX53: GPIO1_2	SD card WP#	
165	UHVIO31	GOIO7_6	iMX53: PATA_DA_0	Dig IO connector, XBEE_SLEEP_RQ	
166	-	NC	-	-	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
167	UHVIO31	GPIO6_14	iMX53: PATA_CS1 WLAN: GPIO Nand flash: NC	Dig IO connector	By default, disconnected from WLAN
168	UHVIO31	GPIO6_16	iMX53: PATA_CS3 Nand flash: NC	Dig IO connector, XBEE_ON/SLEEP	10K pull-up on module to +3.15V
169	UHVIO31	SD3_CMD/UART1_CTS	iMX53: PATA_RESET#	micro SD Card	Repeated pin (J2-128)
170	UHVIO31	SD3_CLK/UART1_RTS	iMX53: PATA_IORDY	micro SD Card	Repeated pin (J2-132)
171	UHVIO31	NANDF_WE#	iMX53: NANDF_WE# NAND flash: WE#	Not used	Level shifter on module
172	GPIO27	GPIO1_4/SD2_CD#	iMX53: GPIO1_4	SD Card CD#	
173	UHVIO31	NANDF_ALE	iMX53: NANDF_ALE NAND flash: ALE	Not used	
174	UHVIO31	NANDF_RE#	iMX53: NANDF_RE# NAND flash: RE#	Not used	Level shifter on module
175	UHVIO31	NANDF_WP#	iMX53: NANDF_WP# NAND flash: WP#	Not used	
176	UHVIO31	NANDF_CLE	iMX53: NANDF_CLE# NAND flash: CLE#	Not used	
177	UHVIO27	GPIO7_12	iMX53: GPIO7_12	User LED2	Repeated pin (J2-74)
178	UHVIO31	NANDF_RB0	iMX53: NANDF_RB0# Nand flash: R/B#	Not used	
179	-	NC	-	-	
180	UHVIO27	GPIO5_20	iMX53: CSI0_DATA_EN	User LED1	

Power

Module Power Supplies

The following figure shows the power supply scheme of the ConnectCore for i.MX53 module.



Supply Inputs

The ConnectCore for i.MX53 module has the following supply inputs:

- Battery input (VLIO)
- Charger input (VCHRG)
- Coin Cell input (VCC_COINCELL)

Battery input (VLIO)

The VLIO supply is used to generate all the voltage supplies needed by the ConnectCore for i.MX53. The minimum voltage of VLIO (allowing the module to power up) is +3.4V. The maximum voltage of VLIO is +4.8V.

This input is the recommended when only one of the two main power inputs (VLIO, VCHRG) is used. The benefit of using this as the Main input is that power restrictions are relaxed and a higher overall current may be drawn through this input. If this is used as the Main power input, the other input VCHRG can be left disconnected. If this is the only power input used, the supply must be rated to maintain the voltage on this input during times of peak demand by the module.

Charger input (VCHRG)

The battery charger supply is used to charge rechargeable batteries, as well as to power up the module when the battery is discharged or not connected. The minimum voltage of the battery charger is +3.4V. The maximum voltage of the battery charger is +5.5V.

Whether this input is used depends on the Host Circuit. If a Lithium Ion secondary cell is connected to VLIO this input is necessary, but the minimum voltage to allow the Lithium Ion cell to charge means that the effective minimum input voltage rises to +4.5V. Note that the i.MX53 module will still work when VCHRG is lower, but the battery will not charge. When there is a Lithium Ion cell connected to VLIO and power is also applied to VCHRG, the current needed by the i.MX53 module and anything that the module powers can be shared between the two inputs. This allows a measurement of the average current to be taken and after allowing a margin for variation and also for the charging of the battery, this figure can be used as the amount needed at the VCHRG input. In this circumstance the peaks drawn by the module are taken from the battery, thus allowing for a smaller power supply to power VCHRG.

If there is no Lithium Ion secondary cell on VLIO, it is still allowed to use the VCHRG power input as the Main input, in which case the VLIO input can be left disconnected. The benefit of using this input as the Main input is that it has a wider input voltage range than VLIO. There are some limitations on the amount of current that can be drawn (especially during power-up), this may mean that Carrier boards for the module that use this power input alone may need to have software controlled power features to prevent the load exceeding the current capabilities. If this is the only power input used, the supply must be rated to maintain the voltage on this input during times of peak demand by the module.

Coin Cell input (VCC_COINCELL)

A connection for a coin cell or supercap is provided at VCC_COINCELL. This power pin can provide power to the RTC even without a connected main battery. If higher voltage is present on the main battery or charger inputs, the main battery/charger will be used as a power source instead.

There are three types of components that can be connected to this pin: Lithium coin cells (Primary cell: non-rechargeable), Lithium coin cells (Secondary cell: rechargeable), and Supercaps. When a Primary Lithium coin cell is connected, the charger must be turned off and this pin is used strictly as an input. It is hazardous to attempt to charge Primary Lithium cells as they may vent or explode. Secondary Lithium coin cells are only made available directly to manufacturers of equipment that could use them, in that case they are normally required to design their product to prevent the user gaining access to this part since there is a danger to the user if by replacing it, they fit a primary type (the only sort that they are likely to be able to source) into the charging circuit. When a Secondary Lithium coin cell is used, both the charging current and the termination voltage are programmable. When a Supercap is used, both the charge current and termination voltage should be set to the maximum values.

The advantage of using a Primary Lithium coin cell is that the energy density usually allows years of service since the self discharge rate is low. The advantage of using a Secondary Lithium coin cell is that the self discharge rate is usually sufficient to allow a few months of support for the RTC before it will need recharging. The advantage of the Supercap is that it is intrinsically safe and can out-last the Primary Lithium coin cell option, however the self discharge rate is high meaning that a 1F capacitor at 25° C is likely to support the RTC for approximately 5 to 10 days.

A programmable constant charge current charger with a programmable top-off charging voltage is provided for charging of Secondary Lithium-Manganese coin cell batteries and super capacitors. Charging current is programmable from 100uA to 6mA. Termination voltage is programmable from +1.1 to +3.1V.

The minimum voltage of the coin cell supply is +2V. The maximum voltage of the coin cell supply is +3.6V.

Supply Outputs

The ConnectCore for i.MX53 module provides the following supply outputs:

- +3.3V
- +2.775V
- +1.8V
- +3.15V

+3.3V

The ConnectCore for i.MX53 module has a DC/DC converter to generate a +3.3V supply. This supply is used on the module to power the WLAN interface, the Ethernet PHY and the Ethernet Controller.

This power regulator can be enabled/disabled by software to save power when the module is in the low power modes. The maximum current provided by this regulator is 1A.

The current available to supply off-module components is 400mA for the wireless variants of the ConnectCore for i.MX53, and 800mA for the wired-only variant of the ConnectCore for i.MX53. If the module is powered from the charger, the maximum charger current limit (1800mA) may limit the current available to supply off-module components.

+2.775V

This supply is generated by LDO4 of the DA9053 PMIC. This supply is used on the module to power the CPU peripherals, the Ethernet PHY, the accelerometer and the CPU image processing unit. The maximum current provided by this supply is 150mA.

The current available to supply off-module components is 80mA.

+1.8V

This supply is generated by LDO8 of the DA9053 PMIC. This supply is used on the module to power the External Interface Module (EIM), the JTAG interface, the touch screen controller and the Ethernet controller. The maximum current provided by this supply is 200mA.

The current available to supply off-module components is 100mA.

+3.15V

This supply is generated by LDO6 of the DA9053 PMIC. This supply is used in the module to power the NAND flash interface, the SD interfaces and the PATA controller. The maximum current provided by this supply is 150mA.

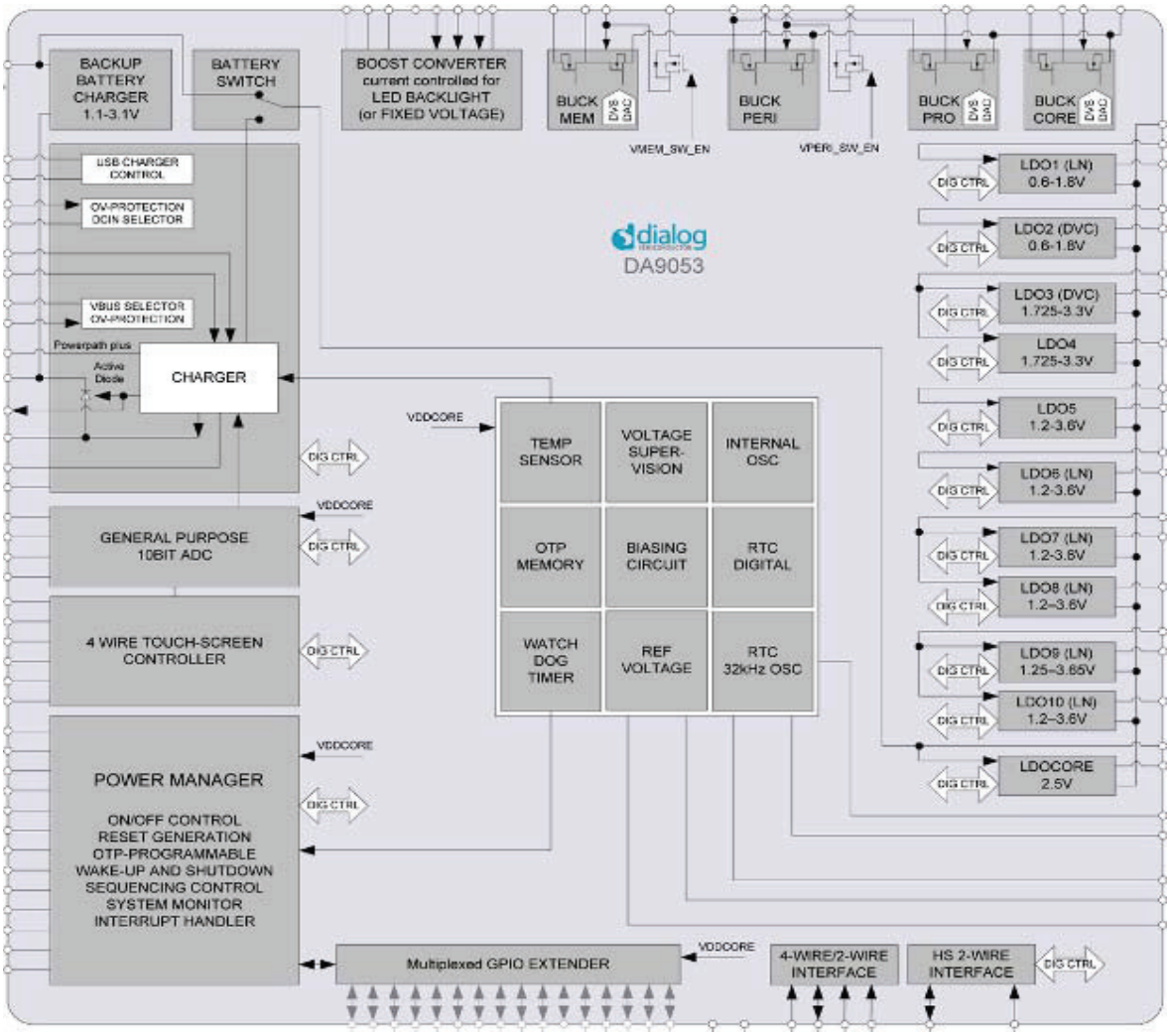
The current available to supply off-module components is 100mA.

DA9053 Power Management

The ConnectCore for i.MX53 module integrates a Dialog DA9053 Power Management chip. This chip provides reference and supply voltages for the ConnectCore for i.MX53 processor as well as for the peripheral devices.

The DA9053 provides four buck switchers and ten low dropout regulators. The start-up of DA9053 supplies is performed with a configurable sequencer. The DA9053 also provides a battery charger that supports current/voltage charging at currents up to 1.25A. Other interfaces as touch screen, general purpose 10bit ADC and PWM are also included on the DA9053.

The following figure shows a block diagram of the DA9053.



Memory

Overview

The i.MX53 processor has an External Memory Controller (EXTMC) that services all the external memory access requests. The EXTMC provides the arbitration interface and different external memory controllers in order to support several memory devices:

- M4IF – Multi Master Multi Memory Interface
- ESDRAMC – Enhanced DDR memory controller
- NFC – NAND flash memory controller
- EIM – SRAM/PSRAM/NOR/NOR flash memory controller

DDR2 SDRAM Memory

The ConnectCore for i.MX53 module provides up to 2GB of DDR2-800 SDRAM memory. On the module in the development kits four 16-bit, 128Mbit, DDR2-800 chips, configured as two banks of 32-bits of 128Mbits DDR2-800 memory are used.

NAND Flash Memory

The ConnectCore for i.MX53 module provides 8GB of NAND flash memory. On the module in the development kits a 512MByte, 2Kbyte page, NAND flash chip is used. This NAND flash device is connected to NAND flash Chip Select 0.

The NAND flash controller signals are available on the module connectors.

External Interface Module (EIM)

The External Interface Module (EIM) is used on the ConnectCore for i.MX53 module to control the Ethernet Controller. This device is connected to EIM Chip Select 1.

The EIM signals are available on the module connectors.

System Boot

The ConnectCore for i.MX53 boot process begins at Power On Reset when the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. Boot ROM code uses the state of the internal register BOOT_MODE[1:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behavior of the module.

The ConnectCore for i.MX53 supports the following boot modes:

- Internal boot
  - The module boots from the internal ROM
  - Program Image loaded from the chosen boot device
  - Boot flow controlled by GPIO and eFUSE (GPIO overrides eFUSE settings)
  - Supports a secure boot using HAB

- Boot from fuses
  - Same as internal boot but GPIO boot override pins are ignored
- Serial Downloader
  - Supports UART and USB

The ConnectCore for i.MX53 supports the following boot devices:

- NOR flash with External Interface Module (EIM), located on CS0, 16-bits bus width
- One NAND flash with EIM, located on CS0, 16-bits bus width
- NAND flash
- SD/MMC
- Parallel ATA (PATA)/Serial ATA (SATA) HDD
- Serial ROM devices (SPI and I^2C EEPROM)

Audio Subsystem

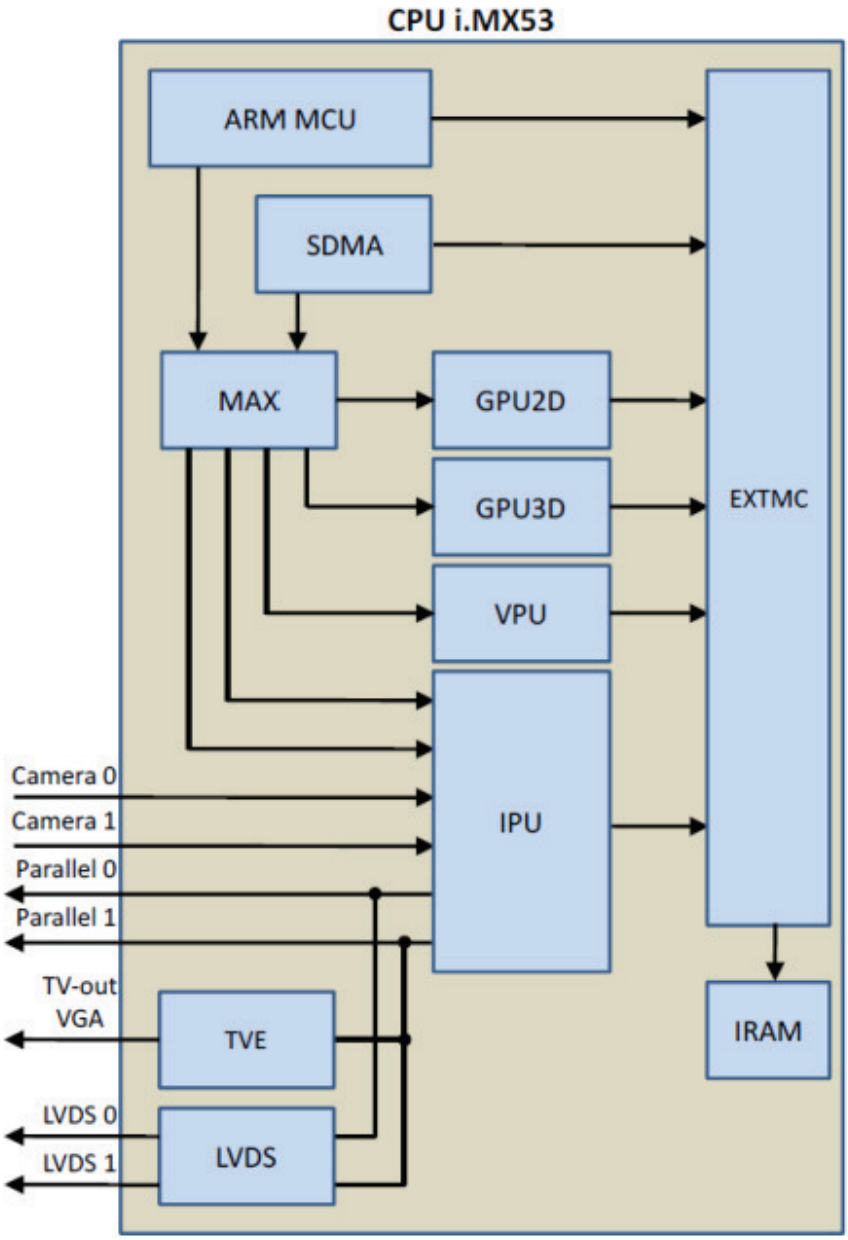
The audio subsystem provided by the ConnectCore for i.MX53 consists of the SSI, SPDIF and the AUDMUX blocs. In addition, the IOMUXC must be configured for appropriate signal directions.

Video Subsystem

The ConnectCore for i.MX53 has a video subsystem that includes the following modules:

- Video Processing Unit (VPU): a multi-standard video/image codec
- Two Graphics Processing Units (GPUs): one for accelerating 3D graphics (OpenGL/ES), and one for accelerating vector graphics (OpenVG and 2D graphics BitBLT)
- Image Processing Unit (IPU): providing connectivity to cameras and displays, related processing, synchronization and control
- Display interface bridge: providing optional translation from the digital display interface supported by the IPU to other interfaces:
  - TV encoder (TVE) bride: composite, S-video, component and VGA interfaces
  - LVDS bridge: up to two LVDS interfaces

The following figure on the next page shows the block diagram of the Video Subsystem:


CPU i.MX53
ARM MCU
SDMA
MAX
GPU2D
GPU3D
VPU
IPU
EXTMC
IRAM
TVE
LVDS
Camera 0
Camera 1
Parallel 0
Parallel 1
TV-out
VGA
LVDS 0
LVDS 1

Multiplexed GPIO

GPIO Multiplexing Table

The ConnectCore for i.MX53 has seven GPIO banks. Each bank provides up to 32 bidirectional general purpose input and output signals.

The GPIO pins are multiplexed with other functions on the module. The IOMUX controller allows the configuration of the pin functions (ALT Mode) and other options (pull-up, keeper, etc).

The table below shows the default configuration of the GPIO pins, the name of the Pad and the default use on the ConnectCore for i.MX53 module. For a detailed description of all the muxing options for each pin, please refer to the Freescale i.MX53 Reference Manual (IMX53RM).

GPIO	Mode	Pad	On module defaults used as
GPIO1_0	ALT3	GPIO_0	Camera MCLK
GPIO1_1	ALT2	GPIO_1	Keypad ROW[5]
GPIO1_2	ALT6	GPIO_2	SD2 WP
GPIO1_3	ALT1	GPIO_3	MX53 ONKEY# input
GPIO1_4	ALT6	GPIO_4	SD2 CD#
GPIO1_5	ALT6	GPIO_5	I2C3_SCL
GPIO1_6	ALT2	GPIO_6	I2SC3_SDA
GPIO1_7	ALT3	GPIO_7	CAN1 TXCAN
GPIO1_8	ALT3	GPIO_8	CAN1 RXCAN
GPIO1_9	ALT2	GPIO_9	Keypad COL[6]
GPIO1_10	ALT0	SD2_CLK	SD2 CLK
GPIO1_11	ALT0	SD2_CMD	SD2 CMD
GPIO1_12	ALT0	SD2_DATA3	SD2 DAT3
GPIO1_13	ALT0	SD2_DATA2	SD2 DAT2
GPIO1_14	ALT0	SD2_DATA1	SD2 DAT1
GPIO1_15	ALT0	SD2_DATA0	SD2 DAT0
GPIO1_16	ALT0	SD1_DATA0	SD1 DAT0
GPIO1_17	ALT0	SD1_DATA1	SD1 DAT1
GPIO1_18	ALT0	SD1_CMD	SD1 CMD
GPIO1_19	ALT0	SD1_DATA2	SD1 DAT2
GPIO1_20	ALT0	SD1_CLK	SD1 CLK
GPIO1_21	ALT0	SD1_DATA3	SD1 DAT3
GPIO1_22	ALT0	FEC_MDIO	FEC MDIO

GPIO	Mode	Pad	On module defaults used as
GPIO1_23	ALT0	FEC_REF_CLK	FEC TX_CLK
GPIO1_24	ALT0	FEC_RX_ER	FEC RX_ER
GPIO1_25	ALT0	FEC_CRS_DV	FEC CRS_DV
GPIO1_26	ALT0	FEC_RXD1	FEC RXD1
GPIO1_27	ALT0	FEC_RXD0	FEC RXD0
GPIO1_28	ALT0	FEC_TX_EN	FEC TX_EN
GPIO1_29	ALT0	FEC_TXD1	FEC TXD1
GPIO1_30	ALT0	FEC_TXD0	FEC TXD0
GPIO1_31	ALT0	FEC_MDC	FEC MDC
GPIO2_0	ALT3	PATA_DATA0	EIM NANDF_D[0]
GPIO2_1	ALT3	PATA_DATA1	EIM NANDF_D[1]
GPIO2_2	ALT3	PATA_DATA2	EIM NANDF_D[2]
GPIO2_3	ALT3	PATA_DATA3	EIM NANDF_D[3]
GPIO2_4	ALT3	PATA_DATA4	EIM NANDF_D[4]
GPIO2_5	ALT3	PATA_DATA5	EIM NANDF_D[5]
GPIO2_6	ALT3	PATA_DATA6	EIM NANDF_D[6]
GPIO2_7	ALT3	PATA_DATA7	EIM NANDF_D[7]
GPIO2_8	ALT4	PATA_DATA8	SD3 DAT0
GPIO2_9	ALT4	PATA_DATA9	SD3 DAT1
GPIO2_10	ALT4	PATA_DATA10	SD3 DAT2
GPIO2_11	ALT4	PATA_DATA11	SD3 DAT3
GPIO2_12	ALT2	PATA_DATA12	SD3 DAT4
GPIO2_13	ALT2	PATA_DATA13	SD3 DAT5
GPIO2_14	ALT2	PATA_DATA14	SD2 DAT6
GPIO2_15	ALT2	PATA_DATA15	SD2 DAT7
GPIO2_16	ALT3	EIM_A22	Camera 2 D[17]
GPIO2_17	ALT3	EIM_A21	Camera 2 D[16]
GPIO2_18	ALT3	EIM_A20	Camera 2 D[15]
GPIO2_19	ALT3	EIM_A19	Camera 2 D[14]
GPIO2_20	ALT3	EIM_A18	Camera 2 D[13]
GPIO2_21	ALT3	EIM_A17	Camera 2 D[12]
GPIO2_22	ALT3	EIM_A16	Camera 2 PIXCLK
GPIO2_23	ALT0	EIM_CS0	EIM CS[0]

GPIO	Mode	Pad	On module defaults used as
GPIO2_24	ALT0	EIM_CS1	EIM CS[1]
GPIO2_25	ALT0	EIM_OE	EIM OE
GPIO2_26	ALT0	EIM_RW	EIM RW
GPIO2_27	ALT0	EIM_LBA	EIM LBA
GPIO2_28	ALT0	EIM_EB0	EIM EB[0]
GPIO2_29	ALT0	EIM_EB1	EIM EB[1]
GPIO2_30	ALT0	EIM_EB2	EIM EB[2]
GPIO2_31	ALT0	EIM_EB3	EIM EB[3]
GPIO3_0	ALT0	EIM_DA0	EIM DA[0]
GPIO3_1	ALT0	EIM_DA1	EIM DA[1]
GPIO3_2	ALT0	EIM_DA2	EIM DA[2]
GPIO3_3	ALT0	EIM_DA3	EIM DA[3]
GPIO3_4	ALT0	EIM_DA4	EIM DA[4]
GPIO3_5	ALT0	EIM_DA5	EIM DA[5]
GPIO3_6	ALT0	EIM_DA6	EIM DA[6]
GPIO3_7	ALT0	EIM_DA7	EIM DA[7]
GPIO3_8	ALT0	EIM_DA8	EIM DA[8]
GPIO3_9	ALT0	EIM_DA9	EIM DA[9]
GPIO3_10	ALT0	EIM_DA10	EIM DA[10]
GPIO3_11	ALT4	EIM_DA11	Camera 2 HSYNC
GPIO3_12	ALT4	EIM_DA12	Camera 2 VSYNC
GPIO3_13	ALT1	EIM_DA13	GPIO[13]
GPIO3_14	ALT1	EIM_DA14	GPIO[14]
GPIO3_15	ALT1	EIM_DA15	GPIO[15]
GPIO3_16	ALT0	EIM_D16	EIM D[16]
GPIO3_17	ALT0	EIM_D17	EIM D[17]
GPIO3_18	ALT0	EIM_D18	EIM D[18]
GPIO3_19	ALT0	EIM_D19	EIM D[19]
GPIO3_20	ALT0	EIM_D20	EIM D[20]
GPIO3_21	ALT0	EIM_D21	EIM D[21]
GPIO3_22	ALT0	EIM_D22	EIM D[22]
GPIO3_23	ALT0	EIM_D23	EIM D[23]
GPIO3_24	ALT0	EIM_D24	EIM D[24]

GPIO	Mode	Pad	On module defaults used as
GPIO3_25	ALT0	EIM_D25	EIM D[25]
GPIO3_26	ALT0	EIM_D26	EIM D[26]
GPIO3_27	ALT0	EIM_D27	EIM D[27]
GPIO3_28	ALT0	EIM_D28	EIM D[28]
GPIO3_29	ALT0	EIM_D29	EIM D[29]
GPIO3_30	ALT0	EIM_D30	EIM D[30]
GPIO3_31	ALT0	EIM_D31	EIM D[31]
GPIO4_0	ALT0	GPIO_10	User key 1
GPIO4_1	ALT0	GPIO_11	User key 2
GPIO4_2	ALT0	GPIO_12	Ethernet controller IRQ
GPIO4_3	ALT0	GPIO_13	Headphone detection
GPIO4_4	ALT0	GPIO_14	Accelerometer IRQ
GPIO4_5	ALT5	GPIO_19	SPI1 RDY
GPIO4_6	ALT2	KEY_COL0	AUD5_TXC
GPIO4_7	ALT2	KEY_ROW0	AUD5_TXD
GPIO4_8	ALT2	KEY_COL1	AUD5_TXFS
GPIO4_9	ALT2	KEY_ROW1	AUD5_RXD
GPIO4_10	ALT0	KEY_COL2	Keypad COL[2]
GPIO4_11	ALT0	KEY_ROW2	Keypad ROW[2]
GPIO4_12	ALT0	KEY_COL3	Keypad COL[3]
GPIO4_13	ALT0	KEY_ROW3	Keypad ROW[3]
GPIO4_14	ALT2	KEY_COL4	CAN2 TXCAN
GPIO4_15	ALT2	KEY_ROW4	CAN2 RXCAN
GPIO4_16	ALT0	DI0_DISP_CLK	DISP0_CLK
GPIO4_17	ALT0	DI0_PIN15	DISP0_PIN15
GPIO4_18	ALT0	DIO_PIN2	DISP0_PIN2
GPIO4_19	ALT0	DIO_PIN3	DISP0_PIN3
GPIO4_20	ALT1	DIO_PIN4	DISP0 GPIO
GPIO4_21	ALT0	DISP0_DAT0	DISP0 DAT[0]
GPIO4_22	ALT0	DISP0_DAT1	DISP0 DAT[1]
GPIO4_23	ALT0	DISP0_DAT2	DISP0 DAT[2]
GPIO4_24	ALT0	DISP0_DAT3	DISP0 DAT[3]
GPIO4_25	ALT0	DISP0_DAT4	DISP0 DAT[4]

GPIO	Mode	Pad	On module defaults used as
GPIO4_26	ALT0	DISP0_DAT5	DISP0 DAT[5]
GPIO4_27	ALT0	DISP0_DAT6	DISP0 DAT[6]
GPIO4_28	ALT0	DISP0_DAT7	DISP0 DAT[7]
GPIO4_29	ALT0	DISP0_DAT8	DISP0 DAT[8]
GPIO4_30	ALT0	DISP0_DAT9	DISP0 DAT[9]
GPIO4_31	ALT0	DISP0_DAT10	DISP0 DAT[10]
GPIO5_0	ALT1	EIM_WAIT	EIM IRQ
GPIO5_2	ALT1	EIM_A25	HDMI IRQ
GPIO5_4	ALT3	EIM_A24	Camera 1 D[9]
GPIO5_5	ALT0	DISP0_DAT11	DISP0 DAT[11]
GPIO5_6	ALT0	DISP0_DAT12	DISP0 DAT[12]
GPIO5_7	ALT0	DISP0_DAT13	DISP0 DAT[13]
GPIO5_8	ALT0	DISP0_DAT14	DISP0 DAT[14]
GPIO5_9	ALT0	DISP0_DAT15	DISP0 DAT[15]
GPIO5_10	ALT0	DISP0_DAT16	DISP0 DAT[16]
GPIO5_11	ALT0	DISP0_DAT17	DISP0 DAT[17]
GPIO5_12	ALT0	DISP0_DAT18	DISP0 DAT[18]
GPIO5_13	ALT0	DISP0_DAT19	DISP0 DAT[19]
GPIO5_14	ALT0	DISP0_DAT20	DISP0 DAT[20]
GPIO5_15	ALT0	DISP0_DAT21	DISP0 DAT[21]
GPIO5_16	ALT0	DISP0_DAT22	DISP0 DAT[22]
GPIO5_17	ALT0	DISP0_DAT23	DISP0 DAT[23]
GPIO5_18	ALT0	CSI0_PIXCLK	Camera 0 PIXCLK
GPIO5_19	ALT0	CSI0_MCLK	Camera 0 HSYNC
GPIO5_20	ALT1	CSI0_DATA_EN	User LED 1
GPIO5_21	ALT0	CSIO_VSYNC	Camera 1 VSYNC
GPIO5_22	ALT3	CSI0_DAT4	SPI1 SCLK
GPIO5_23	ALT3	CSI0_DAT5	SPI1 MOSI
GPIO5_24	ALT3	CSI0_DAT6	SPI1 MISO
GPIO5_25	ALT3	CSI0_DAT7	SPI0 SS0
GPIO5_26	ALT1	CSI0_DAT8	Camera 2 reset
GPIO5_27	ALT1	CSI0_DAT9	Camera 1 reset
GPIO5_28	ALT1	CSI0_DAT10	Touch pen IRQ#

GPIO	Mode	Pad	On module defaults used as
GPIO5_29	ALT1	CSI0_DAT11	USB HUB reset
GPIO5_30	ALT0	CSI0_DAT12	Camera 1 D[12]
GPIO5_31	ALT0	CSIO_DAT13	Camera 1 D[13]
GPIO6_0	ALT0	CSI0_DAT14	Camera 1 D[14]
GPIO6_1	ALT0	CSI0_DAT15	Camera 1 D[15]
GPIO6_2	ALT0	CSI0_DAT16	Camera 1 D[16]
GPIO6_3	ALT0	CSI0_DAT17	Camera 1 D[17]
GPIO6_4	ALT0	CSI0_DAT18	Camera 1 D[18]
GPIO6_5	ALT0	CSI0_DAT19	Camera 1 D[19]
GPIO6_6	ALT3	EIM_A23	Camera 2 D[18]
GPIO6_7	ALT0	NANDF_CLE	NANDF CLE
GPIO6_8	ALT0	NANDF_ALE	NANDF ALE
GPIO6_9	ALT0	NANDF_WP_B	NANDF WP_B
GPIO6_10	ALT0	NANDF_RB0	NANDF RB[0]
GPIO6_11	ALT0	NANDF_CS0	NANDF CS[0]
GPIO6_12	ALT0	NANDF_WE_B	NANDF WE_B
GPIO6_13	ALT0	NANDF_RE_B	NANDF RE_B
GPIO6_14	ALT1	NANDF_CS1	DIGIO 3
GPIO6_15	ALT1	NANDF_CS2	DIGIO 0
GPIO6_16	ALT1	NANDF_CS3	DIGIO 2
GPIO6_17	ALT3	PATA_DIOW	UART1 TXD
GPIO6_18	ALT3	PATA_DMACK	UART1 RXD
GPIO6_22	ALT1	LVDS1_TX3_P	LVDS1 TX3_P
GPIO6_23	ALT1	LVDS1_TX3_N	LVDS1 TX3_N
GPIO6_24	ALT1	LVDS1_TX2_P	LVDS1 TX2_P
GPIO6_25	ALT1	LVDS1_TX2_N	LVDS1 TX2_N
GPIO6_26	ALT1	LVDS1_CLK_P	LVDS1 CLK_P
GPIO6_27	ALT1	LVDS1_CLK_N	LVDS1 CLK_N
GPIO6_28	ALT1	LVDS1_TX1_P	LVDS1 TX1_P
GPIO6_29	ALT1	LVDS1_TX1_N	LVDS1 TX1_N
GPIO6_30	ALT1	LVDS1_TX0_P	LVDS1 TX0_P
GPIO6_31	ALT1	LVDS1_TX0_N	LVDS1 TX0_N
GPIO7_0	ALT3	PATA_DMARQ	UART2 TXD

GPIO	Mode	Pad	On module defaults used as
GPIO7_1	ALT3	PATA_BUFFER_EN	UART2 RXD
GPIO7_2	ALT3	PATA_INTRQ	UART2 CTS
GPIO7_3	ALT3	PATA_DIOR	UART2 RTS
GPIO7_4	ALT2	PATA_RESET_B	SD3 CMD
GPIO7_5	ALT2	PATA_IORDY	SD3 CLK
GPIO7_6	ALT1	PATA_DA_0	DIGIO 1
GPIO7_7	ALT4	PATA_DA_1	UART3 CTS
GPIO7_8	ALT4	PATA_DA_2	UART3 RTS
GPIO7_9	ALT4	PATA_CS_0	UART3 TXD
GPIO7_10	ALT4	PATA_CS_1	UART3 RXD
GPIO7_11	ALT1	GPIO_16	PMIC IRQ
GPIO7_12	ALT1	GPIO_17	USER LED 2
GPIO7_13	ALT3	GPIO_18	OWIRE LINE
GPIO7_22	ALT1	LVDS0_TX3_P	LVDS0 TX3_P
GPIO7_23	ALT1	LVDS0_TX3_N	LVDS0 TX3_N
GPIO7_24	ALT1	LVDS0_CLK_P	LVDS0 CLK_P
GPIO7_25	ALT1	LVDSO_CLK_N	LVDS0 CLK_N
GPIO7_26	ALT1	LVDS0_TX2_P	LVDS0 TX2_P
GPIO7_27	ALT1	LVDS0_TX2_N	LVDS0 TX2_N
GPIO7_28	ALT1	LVDS0_TX1_P	LVDS0 TX1_P
GPIO7_29	ALT1	LVDS0_TX1_N	LVDS0 TX1_N
GPIO7_30	ALT1	LVDS0_TX0_P	LVDS0 TX0_P
GPIO7_31	ALT1	LVDS0_TX0_N	LVDS0 TX0_N

Interfaces

1-Wire

The ConnectCore for i.MX53 provides a 1-Wire interface to communicate with 1-Wire devices such as EEPROMs, secure memory and sensors. The required protocol for accessing the generic 1-Wire device is defined by Maxim.

The 1-Wire interfaces offer the following capabilities:

- Performs the 1-Wire bus protocol to communicate with an external 1-Wire device.
- Provides a clock divider to generate a 1-Wire bus reference clock.
- Supports byte transfers with optional interrupts for more efficient programming.
- Provides a search ROM accelerator mode to speed the search ROM protocol.

Accelerometer

The module provides a three axis digital output accelerometer. This device is connected to the CPU through the I^2C bus.

Interface	I^2C Address (7 bits)
Accelerometer (Freescale MMA7455L)	0 x 1D

The accelerometer offers the following:

- User assigned registers for offset calibration
- Programmable threshold interrupt output
- Level detection for motion recognition (shock, vibration, freefall)
- Pulse detection for single or double pulse recognition
- Selectable sensitivity (±2g, ±4g, ±8g) for 8-bit mode

ADC and Touch Screen

The module provides an Analogue to Digital Converter (ADC) and Touch Screen Interface. The ADC/Touch interface is part of the integrated DA9053 PMIC.

The ADC has a 10 bit resolution and a track and hold circuitry combined with an analog input multiplexer. The analog multiplexer allows conversion of up to 10 different inputs.

The track and hold circuit ensures stable input voltages at the input of the ADC during the conversion.

The following table shows the ADC channel assignments:

Channel	Name	Description
0	VDDOUT	Measurement of the system voltage
1	ICH	Measurement of internal battery charger current
2	TBAT	Output of the battery NTC
3	VBAT	Measurement of the battery voltage
4	ADC_IN4	High impedance input (0-2.5V)
5	ADC_IN5	High impedance input (0-2.5V)
6	ADC_IN6	High impedance input (input divider, 0-2.5V)
7	XY	Touch screen interface to measure the X and Y voltage of the touch screen resistive potentiometers
8	TJUNC	Measurement of internal temperature sensor
9	VBBAT	Measurement of the back battery voltage (Coin Cell)

CAN

The ConnectCore for i.MX53 provides two FlexCAN controllers implementing the CAN protocol according to the CAN 2.0B protocol specification. The CAN block includes two embedded memories, one for storing Message Buffers and another one for storing Rx Individual Mask Registers.

The FlexCAN controllers include these distinctive features:

- Full Implementation of the CAN protocol specification
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mb/sec
  - Content-related addressing
- Deterministic behavior and increased reliability of FlexCAN
- Flexible Message Buffers of zero to eight bytes data length
- Each Message Buffer configurable as Rx or Tx, all supporting standard and extended messages

- Individual Rx Mask Registers per Message Buffer
- Includes 1056 bytes (64 Mbytes) of RAM used for Message Buffer storage
- Includes 256 bytes (64 Mbytes) of RAM used for individual Rx Mask Registers
- Full featured Rx FIFO with storage capacity for 6 frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous CAN version
- Programmable clock source to the CAN Protocol Interface, either bus clock or crystal oscillator
- Unused message buffer and Rx Mask Register space can be used as general purpose RAM space
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power modes, with programmable wake up on bus activity
- Configurable Glitch filter width to filter the noise on CAN bus when waking up

Clock Amplifier (CAMP)

The ConnectCore for i.MX53 provides two inputs connected to a clock amplifier. The clock amplifier converts a square wave/sinusoidal input of frequency range 8-40 MHz, into a +1.8V rail to rail square wave.

The input to the CAMP is internally AC coupled. No external coupling is required.

The outputs of the CAMP are connected to the Clock Control Module (CCM) of the ConnectCore for i.MX53.

Configurable SPI (CSPI)

The ConnectCore for i.MX53 module provides one Configurable SPI (CSPI) interface that can be configured in either master or slave mode. The CSPI contains an 8 x 32 receive buffer (RXFIFO) and an 8 x 32 transmit buffer (TXFIFO).

Key features of the CSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 8-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Max operation frequency up to one quarter of the reference clock frequency

Digital Audio MUX (AUDMUX)

The Digital Audio Multiplexer (AUDMUX) provides a programmable interconnect device for voice, audio, and synchronous data routing between host serial interfaces, such as SSI, and peripheral serial interfaces-that is, audio and voice codecs.

The AUDMUX includes two types of interfaces. Host ports connect to the processor serial interfaces, and peripheral ports connect to off-chip audio devices. A desired connectivity is achieved by configuring the appropriate host and peripheral ports.

The AUDMUX provides flexible, programmable routing of the on-chip serial interfaces to and from off-chip audio devices. The AUDMUX routes audio data but does not decode or process audio data itself.

Enhanced Configurable SPI (ECSPI)

The ConnectCore for i.MX53 module provides two Enhanced Configurable SPI (ECSPI) interfaces that can be configured in either master or slave mode. The ECSPI contains a 64 x 32 receive buffer (RXFIFO) and a 64 x 32 transmit buffer (TXFIFO).

Key features of the ECSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four Chip Select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable

- Direct Memory Access (DMA) support
- Max operation frequency up to the reference clock frequency

Ethernet 1

The ConnectCore for i.MX53 provides a Fast Ethernet Controller (FEC) designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. A low-power 10/100 Ethernet PHY (SMSC LAN8710A) is integrated on the module.

The module does not provide a transformer and Ethernet connector.

The PHY address on the MII bus is 0x7 (0b00111).

The module also provides two status signals for activity and link LEDs.

Ethernet 2

The ConnectCore for i.MX53 module can provide an optional high-performance 10/100Mbit Ethernet controller (SMSC LAN9221) with integrated MAC and PHY as a second Ethernet port.

Key features of the second Ethernet controller:

- Embedded 16 Kbyte FIFO for packet buffers
- Support burst-mode read for highest performance applications
- Configurable interrupt pin with programmable hold-off timer
- Compatible with IEEE 802.3, 802.3u standards
- Integrate Fast Ethernet MAC/PHY transceiver in one chip
- 10Mbps and 100Mbps data rate
- Full and half duplex operations
- 10/100Mbps Auto-negotiation operation
- Twisted pair crossover detection and auto-correction (HP Auto-MDIX)
- EEE 802.3x flow control for full-duplex operation
- Wake-on-LAN capabilities:
- LED pins for various network activity indications

The Ethernet controller is connected to EIM_CS1#. Its programmable polarity interrupt output is connected to the signal GPIO4_2.

The module does not have a transformer and Ethernet connector.

The module provides two status signals for activity and link LEDs.

External Interface Module (EIM)

The ConnectCore for i.MX53 module provides access to the External Interface Module (EIM) of the i.MX53 processor. The EIM allows interfacing devices external to the ConnectCore for i.MX53, including generation of chip selects, clock and control for external peripherals and memory. It provides asynchronous access to devices with SRAM-like interface and synchronous access to devices with NOR-flash-like or PSRAM-like interface.

Key features of the External Interface Module:

- Support for multiplexed address/data bus operations x16 and x32
- Programmable data port size of each Chip select (x8, x16 and x32)
- Up to 6 Chip select with selectable Write Protection for each Chip Select
- Read and write control lines
- 26-bit address bus
- 2x byte enable signals
- Asynchronous accesses with programmable setup and hold times for control signals
- Support for Asynchronous page mode accesses (x16 and x32 port size)
- Independent synchronous Memory Burst Mode support for Nor-flash and PSRAM memories (x16 and x32 port size)
- Support for Big Endian and Little Endian operation modes per access

General Purpose Input/Output (GPIO)

The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce CORE interrupts.

Each GPIO input has a dedicated edge-detect circuit which can be configured through software to detect rising edges, falling edges, logic low-levels or logic high-levels on the input signals. The outputs of the edge detect circuits are optionally masked by setting the corresponding bit in the interrupt mask register.

The GPIO includes the following features:

- General purpose input/output logic capabilities:
  - Drives specific data to output using the data register (GPIO_DR)
  - Controls the direction of the signal using the GPIO direction register (GPIO_GDR)
  - Enables the core to sample the status of the corresponding inputs by reading the pad sample register (GPIO_PSR).

- GPIO interrupt capabilities:
  - Supports up to 32 interrupts
  - Identifies interrupt edges
  - Generates three active-high interrupts to the ConnectCore for i.MX53 interrupt controller

Graphics Processing Unit 2D (GPU2D)

The 2D graphics processing unit is an embedded 2D and vector graphics accelerator. The GPU2D is divided into two segments. The first accelerates 2D bitmap graphics operations. The second one accelerates vector graphics rendering with anti-aliasing polygon rasterizer.

Key features of the GPU2D:

- Frame buffer size support up to 2048x2048
- Linear and block-based (4x4 pixels) frame buffer modes
- Fast buffer clears
- Support for OpenVG render to Image

Main features of the 2D bitmap graphics unit:

- BitBlt (surface-to-surface copy)
- Block fill
- Internal 32-bit color precision
- Supports three source bitmaps for separate mask/pattern/alpha bitmap support plus reading destination for ROP, blend and color key operations
- Supports masking source coordinates for wrapping patterns
- Supports inverting mask and alpha values from source
- Supports destination rotation by 0/90/180/270 degrees
- Supports programmable blending with optional alpha un-premultiply
- Supports color keying by source and destination colors, with optional ignoring of alpha channel
- Supports one scissor rectangle for destination coordinates
- Dithering (ordered)
- Color component masking
- sRGB reads and writes
- BitBlt with scaling, bilinear filtering with texture lookups, programmable filter kernels possible with the programmable Pixel processor

Key features of the vector graphics unit:

- Rasterization of convex and concave polygons with anti-aliasing
- Efficient native polygon rendering (no tessellation to triangles)
- Non-zero and odd-even fill rules
- Primitives supported:
  - Polygons
  - OpenVG path primitives
  - Curve types supported: cubic and quadratic Bézier
  - Strokes with thickness, joints and end caps, unlimited stroke thickness
  - Supports paths with a maximum of 256 crossings along a horizontal or a vertical line
- Input coordinates:
  - Absolute and relative coordinate input in floating point
  - Fixed-point and floating-point coordinate input - 0.8, 0.16, 16.16 formats
- Geometry:
  - User to surface transform for vertices and stroke shape
  - Hardware curve tessellation
  - Adjustable accuracy for curve and round cap splitting
  - OpenVG/SVG join types: Miter (with miter limit), round, bevel
  - OpenVG/SVG cap types: Butt, round, square
- Pixel processing:
  - Programmable gradient and texturing processor
  - Linear and radial gradients (with focal point)
  - Perspective texture mapping with filtering
  - Two textures supported
  - sRGB and pre-multiply support for textures
  - 16-sample anti-aliasing
  - Per-pixel alpha-masking
  - Maximum texture size: 1024x1024 pixels
- Vector graphics rendering system ARM platform load:
  - Display list generation during path creation - commands and vertices are stored to an internal format/buffer, no format conversion is performed
  - Filling or stroking a path only requires a few register writes to start the operation in hardware
  - Display lists are transferred to the vector graphics rasterizer using DMA without ARM platform interaction

Graphics Processing Unit 3D (GPU3D)

The 3D Graphics Processing Unit (GPU3D) is an embedded engine capable of DirectX9 Shader Model 3.0+ program execution. The unit is focused on accelerating user level graphics APIs.

Main features of the GPU3D:

- Built to accelerate OpenGL ES 2.0
- Uses shading architecture to share resources between vertex and pixel shaders
- Advanced packet based command processor for efficient host-GPU transfers
- Integrated Power Management
- Customer configurable on-chip memory used to accelerate 3D rendering

I^2C

The ConnectCore for i.MX53 module provides up to three I^2C interfaces. The I^2C interfaces operate up to 400Kbps, depending on pad loading and timing characteristics. The I^2C system is a true multiple master bus including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously.

The I^2C port 3 interface is used on the module to communicate to the accelerometer and to the DA9053 PMIC. Two 2K2 pull-up resistors connected to +2.775V are provided on the module. This bus is available at the module connector J2.

The I^2C interfaces provide the following capabilities:

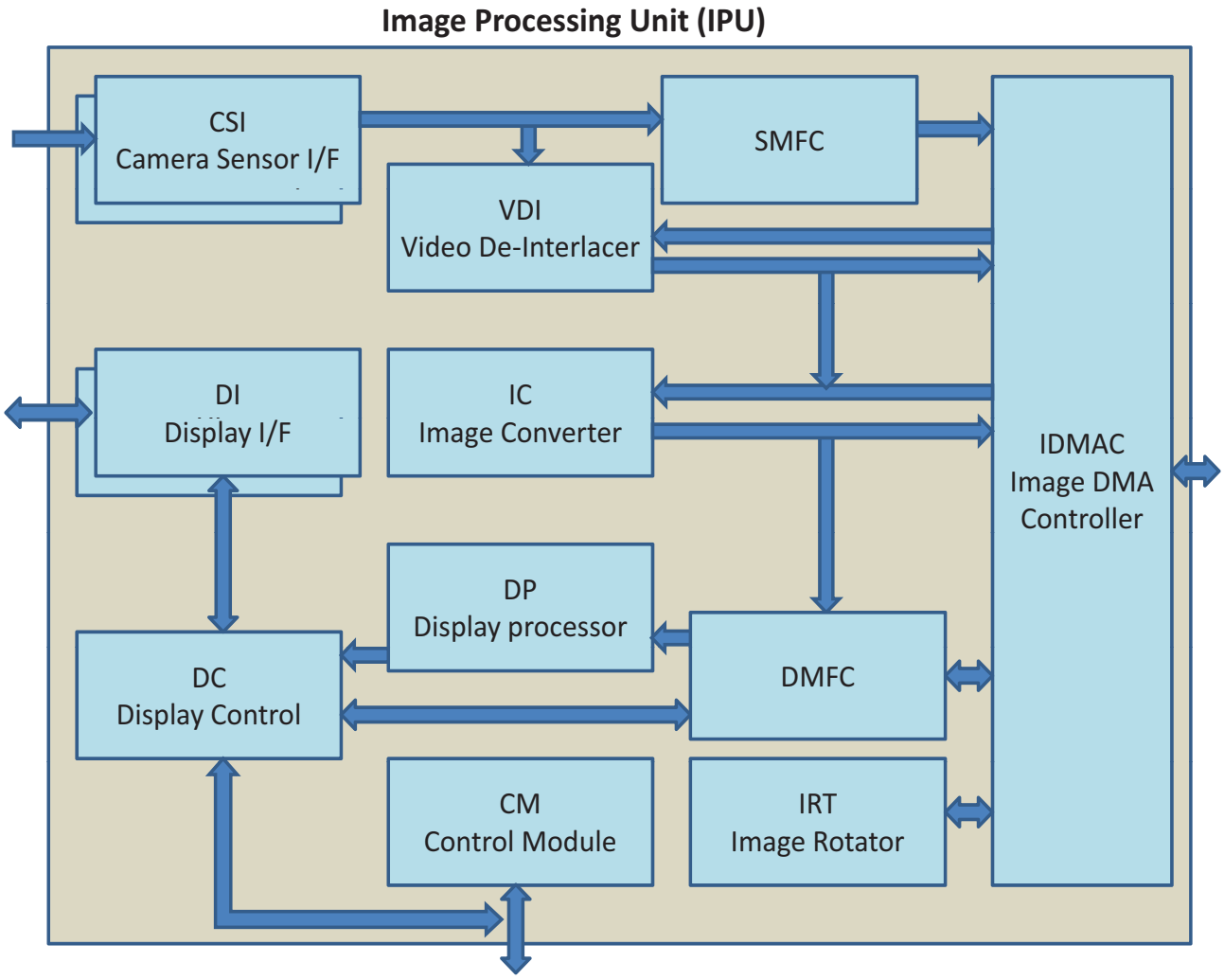
- Compatibility with I^2C bus standard
- Multiple-master operation
- Software programmable for one of 64 different serial clock frequencies
- Software selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

Image Processing Unit (IPU)

The Image Processing Unit (IPU) provides comprehensive support for the flow of data from an image sensor and/or display device:

- Connect relevant devices - cameras, displays, graphics accelerators, TV encoders and decoders
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, etc.
- Synchronization and control capabilities (for example, to avoid tearing artifacts)

The following figure shows the simplified block diagram of the IPU:



The image processing unit has the following blocks:

- 2x Camera Sensor Interface - CSI
  - Controls a camera port; provides interface to an image sensor or a related device.
- 2x Display Interface - DI
  - Provides interface to displays, display controllers and related devices.
- Display Controller - DC
  - Controls the display ports
- Display Processor - DP
  - Performs the processing required for data sent to display
- Image Converter - IC
  - Performs resizing, color conversion/correction, combining with graphics, and horizontal inversion
- Video De Interlacer - VDI
  - Performs video de interlacing (interlaced -> progressive)
- Image Rotator - IRT
  - Performs rotation (90 or 180 degrees) and inversion (vertical/horizontal)
- Image DMA Controller - IDMAC
  - Controls the memory port; transfers data to/from system memory
- Sensor Multi FIFO Controller - SMFC
  - Controls FIFOs for output from the CSIs to system memory
- Display Multi FIFO Controller - DMFC
  - Controls FIFOs for IDMAC channels related to the display system
- Control Module - CM
  - Provides control and synchronization

For more in-depth information regarding the blocks of the IPU please refer to the Freescale i.MX53 Applications Processor Reference Manual (IMX53RM).

Keypad

The ConnectCore for i.MX53 module provides a keypad port that can be used as a keypad matrix interface or as general purpose input/output.

The Keypad port interface to a keypad matrix with 2-point contact or 3-point contact keys. The Keypad port is designed to simplify the software task of scanning a keypad matrix. With appropriate software support, the Keypad port is capable of detecting, debouncing, and decoding one or multiple keys pressed simultaneously on the keypad.

The Keypad Port includes these features:

- Supports up to an 8 x 8 external keypad matrix
- Port pins can be used as general purpose I/O
- Open drain design
- Glitch suppression circuit design
- Multiple-key detection
- Long key-press detection
- Standby key-press detection
- Synchronizer chain clear
- Supports a 2-point and 3-point contact key matrix

LVDS Display Bridge (LDB)

The LVDS Display Bridge (LDB) is used to connect the Image Processing Unit (IPU) to an external LVDS display interface.

The LDB provides following ports:

- Two parallel display port inputs
- Two LVDS channel outputs – each channel consisting of 4 data pairs, and 1 clock pair
- Control signals – to configure LDB parameters and operations
- Clocks from SoC DPLLs

The RGB input data interface contains RGB data (18 or 24 bits), pixel clock and control signals (HSYNC, VSYNC and DE). The rates supported are:

- For single-channel output: Up to 170 MHz pixel clock (for example, UXGA -1600x1200 @ 60 Hz + 35% blanking)
- For dual-channel output: Up to 85 MHz per interface (for example, WXGA -1366x768 @ 60 Hz + 35% blanking)

The two LVDS ports may be used as follows:

- One single-channel output
- One dual channel output: single input, split to two output channels

- Two identical outputs: single input sent to both output channels
- Two independent outputs: two inputs sent, each to a different output channel

Memory Cards (MMCI/eMMC/SD/SDIO)

The ConnectCore for i.MX53 module provides up to four Enhanced Secured Digital Host Controllers (ESDHC) to interface between the i.MX53 CPU and MMC/eMMC/SD/SDIO devices. The ESDHC acts as a bridge, passing host bus transactions to the cards by sending commands and performing data accesses to/from the cards. It handles the MMC/eMMC/SD/SDIO protocols at the transmission levels.

The types of cards supported by the ESDHC are described briefly as follows:

- MultiMediaCard (MMC)

  This is a universal low-cost data storage and communication media that is designed to cover a wide area of applications including mobile video and gaming, WLAN or other wireless networks. Old MMC cards are based on 7-pin serial bus with a single data pin, while the newer high-speed MMC communication is based on an advanced 11-pin serial bus designed to operate at lower voltage.

- Embedded Multimedia Card (eMMC)

  The eMMC describes an architecture consisting of an embedded storage solution with MMC interface, flash memory and controller, all in a small ball grid array (BGA) package.

- Secure Digital (SD) card

  This is an evolution of earlier MMC technology. It is specifically designed to meet the security, capacity, performance, and environment requirements inherent in newly emerging audio and video consumer electronic devices. The physical form factor, pin assignment and data transfer protocol are forward compatible with MMC, with some additions. Under the SD protocol, an SD card can be categorized as memory card, I/O card, or combo card (having both memory and I/O functions).

The main features of the ESDHC are the following:

- Designed to work with MMC, MMC plus, MMC RS, SD memory, miniSD memory, SDIO, and SD Combo. Compatible with the following specifications:
  - MMC System Specification versions 4.2/4.3/4.4
  - SD Host Controller Standard Specification version 2.0
  - SD Memory Card Specification version 2.0 and supports High-Capacity SD Memory Cards
  - SDIO Card Specification version 2.0
- Supports 1, 4, or 8 bit MMC modes and 1bit or 4 bit SD and SDIO modes
  - Card bus clock frequency up to 52 MHz
  - Up to 832 Mbps of data transfer for MMC cards in 8-bit Dual Data Rate mode
  - Up to 416 Mbps of data transfer for MMC cards in 8-bit Single Data Rate mode
  - Up to 200 Mbps of data transfer for SD/SDIO cards in 4-bit mode

- Supports Single Block, Multi Block read and write
- Supports block sizes of 1 ~ 4096 bytes
- Supports the write protection switch for write operations
- Supports both synchronous and asynchronous abort
- Supports pause during the data transfer at block gap
- Supports SDIO read wait and suspend resume operations
- Supports auto CMD12 for multi-block transfer
- Host can initiate non-data transfer command while data transfer is in progress
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes
- Embodies a fully configurable 128x32-bit FIFO for read/write data
- Supports internal and external DMA capabilities
- Supports advanced DMA to perform linked memory access

PWM

The ConnectCore for i.MX53 module provides four PWM interfaces. Two of these PWM interfaces are available on the i.MX53 CPU and the other two PWM interfaces are provided by the DA9053 PMIC.

ConnectCore for i.MX53 PWM

The two PWM interfaces of the i.MX53 have a 16-bit counter, and are optimized to generate sound from stored sample audio images and they can also generate tones.

Main features of these PWM interfaces:

- 16-bit up-counter with clock source selection
- 4 × 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low power and debug modes
- Interrupts at compare and rollover

DA9053 PWM

The DA9053 PMIC has two GPIO signals including PWM control. The generated PWM signals have a frequency of 21 kHz. The duty cycle can be controlled with 95 steps (using a 2MHz clock for each step).

The PWM signals can be configured to use an internal 100Kohm pull-up to +3.3V, or an external pull-up.

RTC

The ConnectCore for i.MX53 provides a Real Time Clock and a Secure Real Time clock.

The real time clock function is provided including time and day counters as well as an alarm function. The RTC utilizes a 32.768 KHz crystal oscillator for the time base and is powered by the coin cell backup supply when main supply has dropped below operational range. The accuracy of the 32.768 KHz crystal used for the Real-Time Clock is ±20ppm.

- RTC accuracy ±20ppm
- 6-bit year counter. Year 0 corresponds to 2000.
- Alarm registers containing min, hrs, day, month, and year.

The secure real time clock helps to comply with issues arising out of different applications requiring secure and certifiable time, for example Digital Rights Management (DRM) schemes.

Main features of the secure RTC interface are the following:

- Secure 47-bit time counter
- Non-secure 47-bit time counter
- Use-mode protection. The SRTC cannot be configured by non-secured SW.
- Re-programming protection. The SRTC cannot be altered or disabled after SRTC locked.
- Clock source protection
- Programmable secure and non-secure alarms with interrupt

Known Issue with the RTC

Symptom:

Loss of Time and Date from the RTC registers.

Occurrence:

When the VCHRG power supply is used, the VLIO power supply is disconnected, a coin-cell is connected to VBBAT and the temperature is below +40 Celsius. At the time when VCHRG is disconnected, the PMIC should cause the power to switch over from VCHRG (charger power input) to VBBAT (the coin-cell power input). However, there is a fault which results in the registers being reset. At +20 Celsius and below, this happens every time the power change-over takes place. At temperatures between +20 and +40 Celsius the fault may occur. For temperatures over +40 Celsius the switch-over works satisfactorily.

Note: There may be some variation in the temperature trip points.

Possible Workarounds:

1. Use the VLIO and VBBAT inputs only, leave VCHRG disconnected.
2. Use VLIO, VBBAT and VCHRG.
3. Use an RTC on the board that hosts this module.

SATA

The integrated Serial Advanced Technology Attachment (SATA) Controller is compatible with the Advanced Host Controller Interface (AHCI) specification. The SATA Controller along with integrated physical link hardware (SATA PHY) provides one SATA port for the attachment of external SATA compliant storage devices.

The ConnectCore for i.MX53 module provides connection to the SATA port on system module connectors (J1 and J2).

The SATA port provides the following features:

- Compliant with Serial ATA Specification 2.6, and AHCI Revision 1.3 specifications (except FIS-based switching) at 1.5 Gb/s port speed
- Rx Data Buffer for recovered clock systems
- Data alignment circuitry
- OOB signaling detection and generation
- Asynchronous Signal Recovery, including retry polling
- Digitally supports device hot-plugging
- 8b/10b encoding/decoding
- Supports power management features including automatic partial to slumber transition
- Supports BIST loopback data checking on a per FIS basis
- Supports one SATA device (Port 0)
- AMBA AHB interface (one master and one slave)
- Internal DMA engine for reading command lists and transferring data
- Supports hardware-assisted native command queuing for up to 32 entries
- Supports port multiplier with command-based switching
- Activity LED support
- Supports disabling Rx and Tx data clocks during power down modes
- Supports eSATA (when external analog logic also supports eSATA)

SPDIF

The ConnectCore for i.MX53 provides a Sony/Philips Digital Interface Transmitter (SPDIF Tx) audio module enabling the processor to transmit stereo digital audio. The SPDIF transceiver allows handling of both SPDIF channel status (CS) and User (U), data including a frequency measurement for the precise measurement of an incoming sampling frequency.

As the SPDIF internal data width is 24-bit, the eight most-significant bits of all registers return zeros.

The SPDIF is composed of two parts: SPDIF Receiver and SPDIF Transmitter. The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs. The Channel Status and User Bits are also extracted from each frame and placed in the corresponding registers. The SPDIF receiver also provides a bypass option for direct transfer of the SPDIF input signal to the SPDIF transmitter.

For the SPDIF transmitter, the audio data is provided by the processor. The Channel Status bits are also provided via the corresponding registers. The SPDIF transmitter generates a SPDIF output bitstream in the biphase mark format (IEC60958), which consists of audio data, channel status and user bits.

In the SPDIF transmitter, the IEC60958 biphase bit stream is generated on both edges of the SPDIF Transmit clock. The SPDIF Transmit clock is generated by the SPDIF internal clock generate block and the sources are from outside of the SPDIF block. For the SPDIF receiver, it can recover the SPDIF Rx clock. Both the Rx clock and Tx clock are be sent to the ASRC.

Synchronous Serial Interface (SSI)

The ConnectCore for i.MX53 module provides up to three synchronous serial interfaces (SSI). The SSI is a full-duplex serial port that allows communication with external audio devices using a variety of serial protocols (SSI normal, SSI network, I2S and AC-97), bit depths and clock/frame sync options.

SSI is typically used to transfer samples in a periodic manner. The SSI consists of independent transmitter and receiver sections with independent clock generation and frame synchronization.

Main features of the SSI interface:

- Independent (asynchronous) or shared (synchronous) transmit and receive sections operating in Master or Slave mode
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as 32 time slots
- Two sets of four 15 x 32 bits Transmit and Receive FIFOs
- Programmable data interface mode such like I2S, LSB, MSB aligned
- Programmable word length 8, 10, 12, 16, 18, 20, 22 or 24 bits
- Program options for frame sync and clock generation
- Programmable I^2S modes (Master, Slave or Normal)
- AC97 support
- Completely separate clock and frame sync selections for the receive and transmit sections
- External network clock input for use in I^2S Master mode
- SSI power-down

Television Encoder (TVE)

The Television Encoder (TVE) provides a direct connection between the ConnectCore for i.MX53 and a TV set via analog interface. The TV Encoder supports Standard Definition (SD) and High Definition (HD) television standards.

The TVE can operate in two modes:

- Encoding the video data according to the selected TV standard
- Generating RGB analog signals according to the VGA specification

Key features of the TVE in TV encoding mode:

- SD mode features
  - Supported TV standards: NTSC, 480i, 576i and PAL B,D,G,H, I/M/N
  - Supported output formats: CVBS, S-Video (Y/C), YPrPb and RGB
  - Wide-Screen Signaling (WSS) support
  - Macrovision™ 7.1 copy protection
  - Output oversampling up to x16 for elimination of external analog filters
- HD mode features
  - Supported TV standards: 720p@60Hz, 720p@50Hz, 720p@30Hz, 720p@25Hz, 1080i@60Hz, 1080i@50Hz, 1035i@60Hz, 1080p@30Hz, 1080p@50Hz, 1080p@60Hz
  - Supported output formats: YPrPb and RGB
  - Output oversampling up to x4 for elimination of external analog filters
- Common SD/HD mode features
  - Flexible timing and gain control mechanism allowing non-standard parameters
  - Programmable Chroma digital filters
  - Programmable adaptive Luma digital filters
  - Programmable YCrCb to RGB color matrix
  - Output resolution - 10 bits

UART

The ConnectCore for i.MX53 module provides up to five UART ports. UART 1 is a full-modem UART port with all handshake signals available. The other UART ports are 4-wire UART ports with data lines RXD/TXD and the handshake lines RTS#/CTS#.

The UART ports supports NRZ encoding and IrDA-compatible infrared slow data rate (SIR) format.

Main features of these UART ports:

- High-speed TIA/EIA-232-F compatible, up to 4.0 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 7 or 8 data bits

- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS#) and clear to send (CTS#) signals (signal direction according to DCE mode).
- Maskable Interrupts
- Two DMA Requests (TxFIFO FMA Request and RxFIFO DMA Request)
- Escape character sequence detection
- Voting logic for improved noise immunity (16x oversampling)
- DCE/DTE capability
- Auto baud rate detection (up to 115.2 Kbps)
- Programmable baud rate (up to 4Mbps)
- Two independent 32-byte FIFOs for receive and transmit
- Receiver, transmitter and UART internal clocks enable/disable for power saving

USB Host and USB OTG

The ConnectCore for i.MX53 provides three USB 2.0 high speed Host controllers and one USB 2.0 On-The-Go (OTG) high speed controller. These interfaces conform to the USB 2.0 specification, the OTG supplement.

Each controller can support ULPI, Serial, UTMI, IC-USB or HSIC interfaces according to its feature. All four controllers are single-port. For the OTG, there is only one port. It is used as both a downstream and upstream port. For the Host-only core, there is also one port which is used as a downstream port.

Key USB features:

- High-speed/full-speed/low-speed host only (Host1)
  - HS/FS/LS UTMI compliant interface
  - HS USB PHY included
- High-speed/full-speed/low-speed host only (Host2)
  - HS/FS/LS ULPI compliant interface
  - Software configurable for full speed/low speed interface for Serial transceiver
  - Full Speed Inter-Chip USB compliant interface (IC-USB)
- High-speed/full-speed/low-speed host only (Host3)
  - HS/FS/LS ULPI compliant interface
  - Software configurable for full speed/low speed interface for Serial transceiver
- High-speed/full-speed/low-speed OTG
  - HS/FS/LS UTMI compliant interface
  - HS USB PHY included

  - High Speed, Full Speed and Low Speed operation in Host mode (with UTMI transceiver)
  - High Speed, and Full Speed operation in Peripheral mode (with UTMI transceiver)
  - Hardware support for OTG signaling, session request protocol, and host negotiation protocol
  - Up to 8 bidirectional endpoints
- Low-power mode with local and remote wake-up capability
- Serial PHY interfaces configurable for bidirectional/unidirectional and differential/ single ended
- Embedded DMA controller

Video Processing Unit (VPU)

The video processing unit is a multi-standard video processing codec capable of handling multiple streams simultaneously through time multiplexing. This VPU covers many standards and high definition video decoders and decoders as a multi-standard video codec engine, as well as several important video processes such as rotation, mirroring and deringing.

The VPU has its own DMA driven AXI masters that allow it to retrieve data directly from system memory (DDR and iRAM).

The following table lists the VPU's encoding/decoding capabilities:

Dec/Enc	Standard	Profile	Resolution	Bitrate
HW Decoder	MPEG-2	Main-High	1080 i/p	40Mbps
	MPEG4/XviD	SP/ASP	1080 i/p	40Mbps
	H.263	P0/P3	16CIF	20Mbps
	Sorenson H.263	N/A	16CIF	20Mbps
	H.264	BP/MP/HP	1080 i/p	40Mbps
	VC1	SP/MP/AP	1080 i/p	40Mbps
	Real Video	8/9/10	1080 i/p	40Mbps
	DivX	2/4/5/6	1080 i/p	40Mbps
	MJPEG	Baseline	8192x8192	40Mpixel/sec (YUV444)
HW Encoder	MPEG2	Main-Main	D1	15Mbps
	MPEG4	Simple	720p	20Mbps
	H.263	P0/P3	4CIF	20Mbps
	H.264	Baseline	720p	20Mbps
	MJPEG	Baseline	8192x8192	80Mpixel/sec (YUV422)

Watchdog Timer

The Watchdog Timer (WDOG-1) protects against system failures by providing a method of recovering from unexpected events or programming errors. Once the watchdog is activated, it must be serviced by software on a periodic basis. If servicing does not take place, the watchdog asserts the internal system reset signal after the corresponding timeout occurs.

The Watchdog Timer features are as follows:

- A time-out counter with time-out periods from 0.5 to 128 seconds
- Time resolution of 0.5 seconds
- Configurable time-out counter that can be programmed to run or stop during low power and debug modes
- Programmable interrupt generation prior to time-out

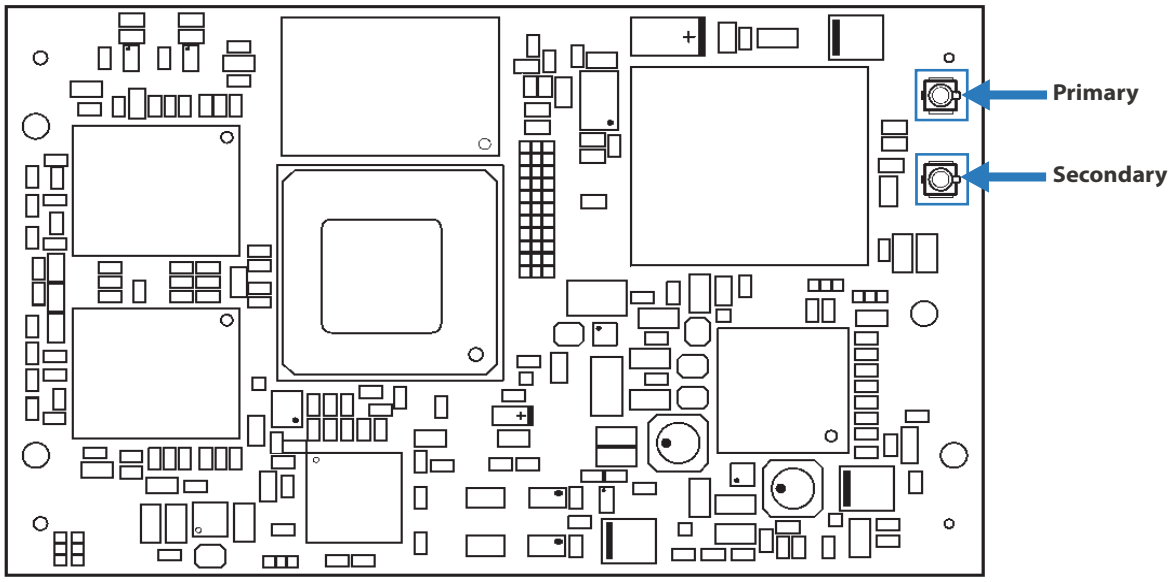
- Programmable time duration between interrupt and timeout events, from 0 to 128 seconds in steps of 0.5 seconds
- Power down counter with fixed time-out period of 16 seconds

WLAN

WLAN

In addition to the on-module Ethernet interface, the ConnectCore for i.MX53 module can also provide an optional dual-diversity 802.11a/b/g/n WLAN interface with data rates up to 54 Mbps 802.11a/b/g mode and up to 65 Mbps in 802.11n mode.

Two U.FL antenna connectors are provided on the module.



On the ConnectCore for i.MX53 module variant, attach the antennas with the U.FL-RP-SMA female cable to the primary connector and secondary connector on the module.

Note: When disconnecting U.FL connectors, the use of a U.FL plug extraction tool (Hirose P/N U.FL-LP-N-2 or U.FL-LP(V)-N-2) is strongly recommended to avoid damage to the U.FL connectors on the module.

To mate U.FL connectors, the mating axes of both connectors must be aligned. The "click" will confirm mated connection. Do not attempt insertion at an extreme angle.

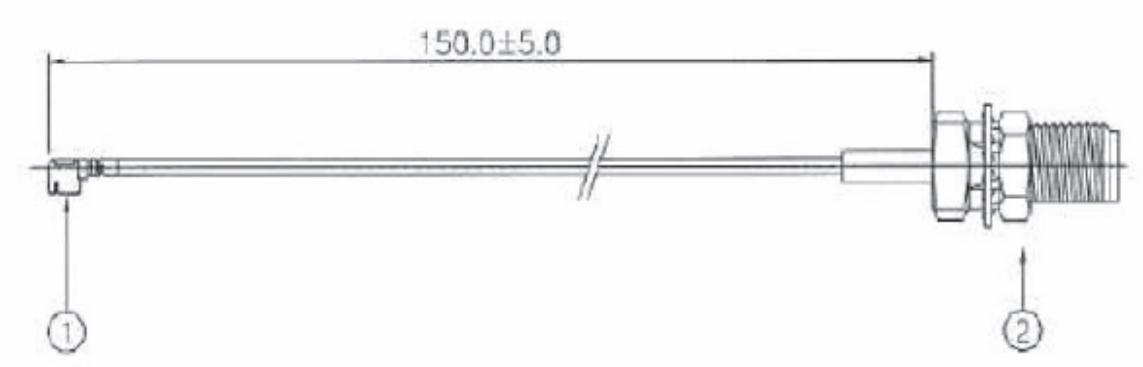
Cable Specification: U.FL/W.FL to RP-SMA

Attributes

Attribute	Property
Impedance	50 Ohm
Frequency Range	0 to 6 GHz
Length	150 mm
Temperature Range	-40° to +90° C
Loss	3.8dB/m (3 GHz) 5.6dB/m (6 GHz)

Dimensions

Note: Dimensions are provided for reference purposes only. The actual antenna might vary.



1 = U.FL

2 = RP-SMA

Note: This module obtained its complete certification by using the cable described here. End users in North America should use a cable that matches these specifications to maintain the module's certification.

Antenna Specification: RP-SMA

Attributes

Attribute	Property
Frequency Range	2.4 to 2.4835 GHz / 5.15 to 5.35 GHz / 5.725 to 5.85 GHz
Impedance	50 Ohm
VSWR	2.0 max
Return Loss	-10dB max
Gain	5 dBi (Typ.)
Polarization	Linear
Radiation Pattern	Near omni-directional in the horizontal plane
Admitted Power	1W
Electrical	1/2 λ Dipole

Note: This module obtained its complete certification by using the antenna described here. End users in North America should use an antenna that matches these specifications to maintain the module's certification. Antennas of the same type but operating with a lower gain may be used.

SAR Requirements

This module and its associated antennas should be installed at a distance of at least 20cm from personnel.

Labelling Requirements

Products in which this module is fitted must be labelled with the following text "contains FCC ID: MCQ-50M1699".

About the Development Board

CHAPTER 2

The development board supports the ConnectCore for i.MX53 module. This chapter describes the interfaces of the development board and explains how to configure the board for your requirements.

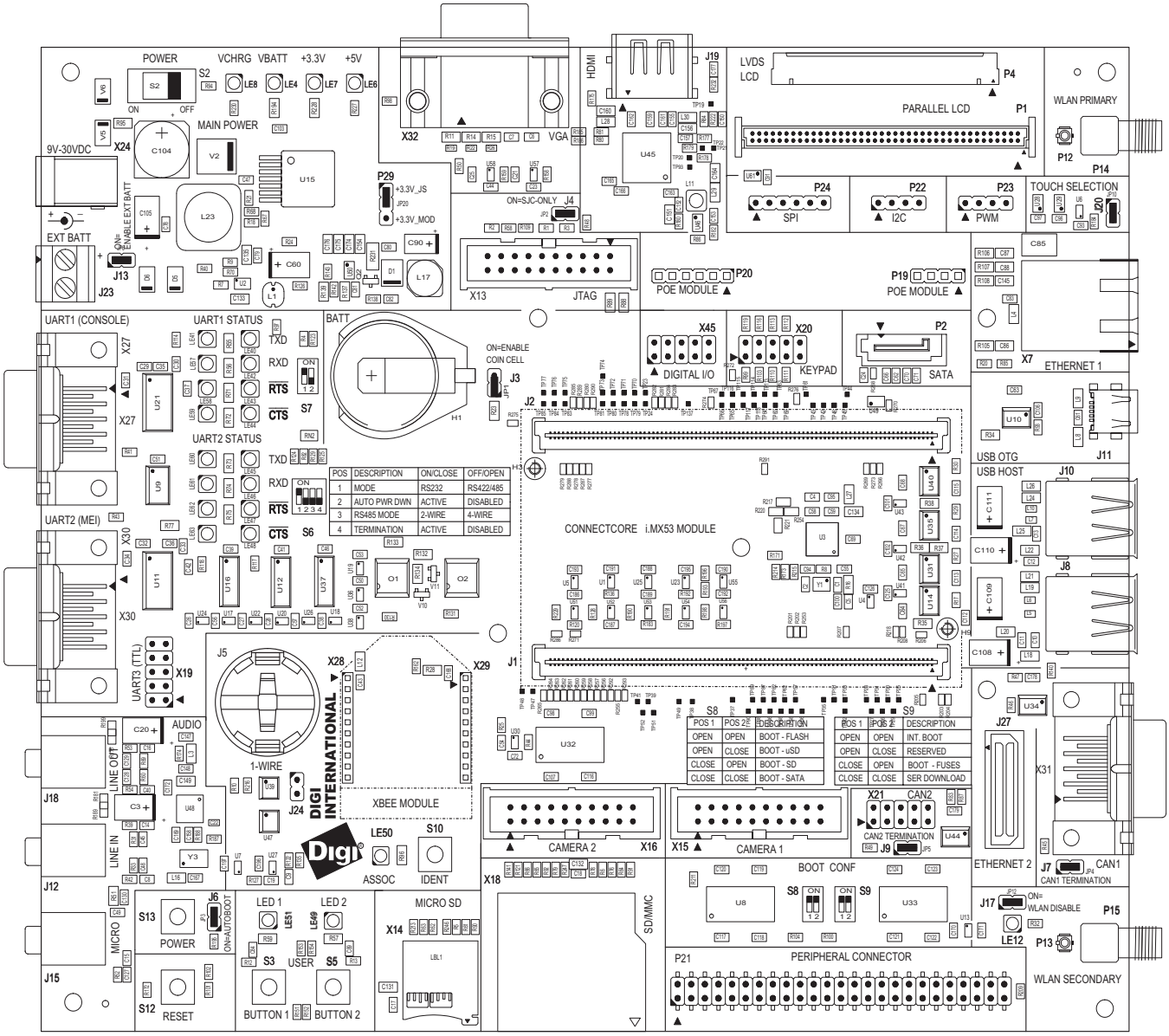
The development board has two 180-pin connectors that mate with the module connectors.

What's on the Development Board?

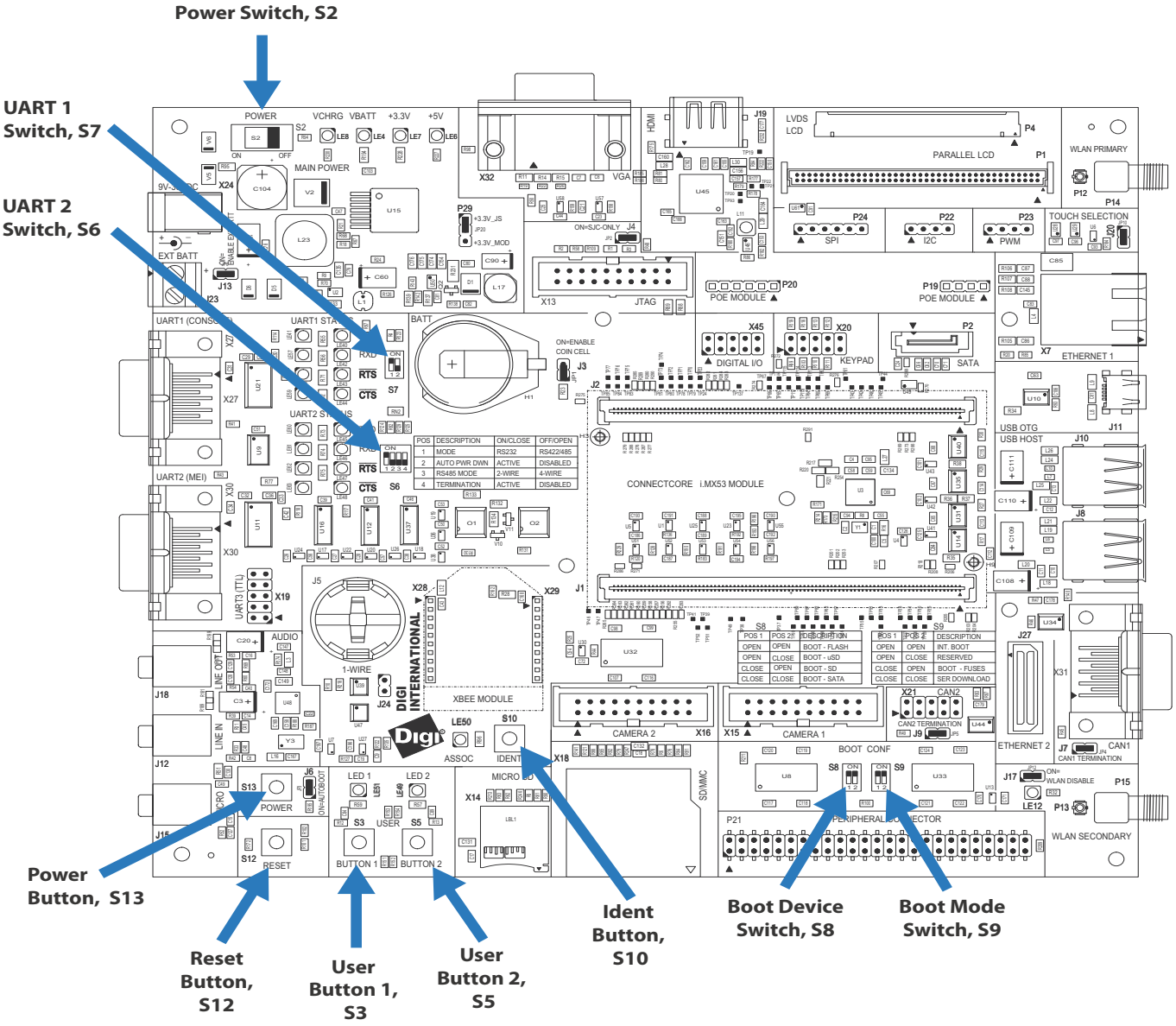
- Flexible 9-30VDC charger power supply with power-on switch
- Screw-flange Battery header with enable jumper
- 3V coin cell battery
- +3.3V selection jumper. The +3.3V supply can be selected from the module or from the development board.
- Connectors for Digi 802.3af PoE Application board (sold separately)
- 1 x UART RS232 with status LEDs and SUB-D 9-pin connector
- 1 x UART MEI (RS232/RS4xx) with status LEDs and SUB-D 9-pin connector
- 1 x UART with TTL levels
- 1 x CAN bus with termination resistor selection and SUB-D 9-pin connector
- 1 x CAN bus with termination resistor selection and pin header
- 1 x USB OTG connector
- 4 x USB Host connectors
- 1 x SD/MMC card holder
- 1 x MicroSD card holder
- 1 x SATA connector
- SPI and I^2C headers
- PWM header
- Audio interface with Line-out, Line-In and Mic-In jacks
- VGA interface

- HDMI interface
- Parallel LCD connector with Touch Screen interface
- LVDS LCD connector with Touch Screen interface
- Touch Screen selection circuit
- 2 x Camera connectors
- RJ-45 Ethernet connector
- Connector for a Digi 100M_ETHADPT (sold separately)
- 2 x RP-SMA WLAN antenna connectors
- Digital I/O header
- XBee socket with Association LED and Ident Button (XBee module sold separately)
- 1-Wire interface with 2-pin header
- 1-Wire EEPROM
- 1-Wire iButton retainer
- Peripheral application header
- Keypad header
- JTAG interface
- 2 x User LEDs (green)
- 2 x User Push-buttons
- Boot mode switch
- Boot device switch
- 1 x Power Push-button
- 1 x Reset Push-button

The Development Board



Switches and Push-buttons



Power Switch, S2

The development board has an ON/OFF switch, S2. The power switch S2 can switch both 9V-30VDC input power supply and 12VDC coming out of the optional PoE module (Digi P/N DG-ACC-POE). However, if a power plug is present on the DC power jack, PoE is disabled.

Reset Button, S12

The reset push-button S12, resets the module and the peripherals on the development board. A push-button allows manual reset by connecting POR# or optionally RSTIN# to ground.

Power Button, S13

The power button S12 generates a power event for the i.MX53 and the DA9053 PMIC.

When the module is in Off mode, a Power event will power on the module.

When the module is in On mode, a long press (>2sec) of the power button will turn off the module.

When the module is in On mode, a short press of the power button will put the module in suspend mode (low power).

When the module is in Suspend mode, a short press of the power button will resume the module.

User Buttons, S3 and S5

Use the user push-buttons to interact with the applications running on the ConnectCore for i.MX53 module. Use these module signals to implement the push-buttons:

Signal Name	Button	GPIO Used
USER_KEY1	S3	GPIO4_0
USER_KEY2	S5	GPIO4_1

Ident Button, S10

The Ident push-button S10 is associated to the commissioning input of the Digi XBee modules. This input provides a variety of simple functions to aid in deploying devices in a network. For a deeply description of this functionality please refer to the Digi XBee modules documentation.

Legend for Multi-Position Switches

Switches S6, S7, S8 and S9 are multi-pin switches. In the description tables for these switches, the position is designated as *S[switch number].[pin number]*. For example, position 1 on switch S6 is specified as S6.1.

UART 1 Switch, S7

Use S7 to configure the line interface for serial port 1 (console):

Switch Pin	Function	Comments
S7.1	On = Power save Off = Normal Operation	If there is a valid RS232 signal at receiver inputs the UART will be in normal operation mode. If there is not a valid RS232 signal at receiver inputs the UART will be in shutdown mode.
S7.2	On = Shutdown Off = Normal Operation	Shutdown is the highest priority functionality. If switch S7.2 = ON, the UART 2 will be in shutdown mode independently of the position of S7.1.

UART 2 Switch, S6

Use S6 to configure the line interface for serial port 2 MEI:

Switch Pin	Function	Comments
S6.1	On = RS232 transceiver enabled RS4xx transceiver disabled Off = RS232 transceiver disabled RS4xx transceiver enabled	
S6.2	On = Auto Power Down enabled Off = Auto Power Down disabled	Auto Power Down is not supported on this board. This signal is only accessible to permit the user to completely disable the MEI interface for using the signals for other purposes. To disable the MEI interface, go into RS232 mode (S6.1 = ON) and activate the Auto Power Down feature (S1.2 = ON) - be sure that no cable is connected to connector X30.
S6.3	On = 2-wire interface (RS4xx) Off = 4-wire interface (RS422)	
S6.4	On = Termination ON Off = No termination	

Boot Device Switch, S8

Use S8 to configure the source of the boot code when S9 is configured in internal boot mode.

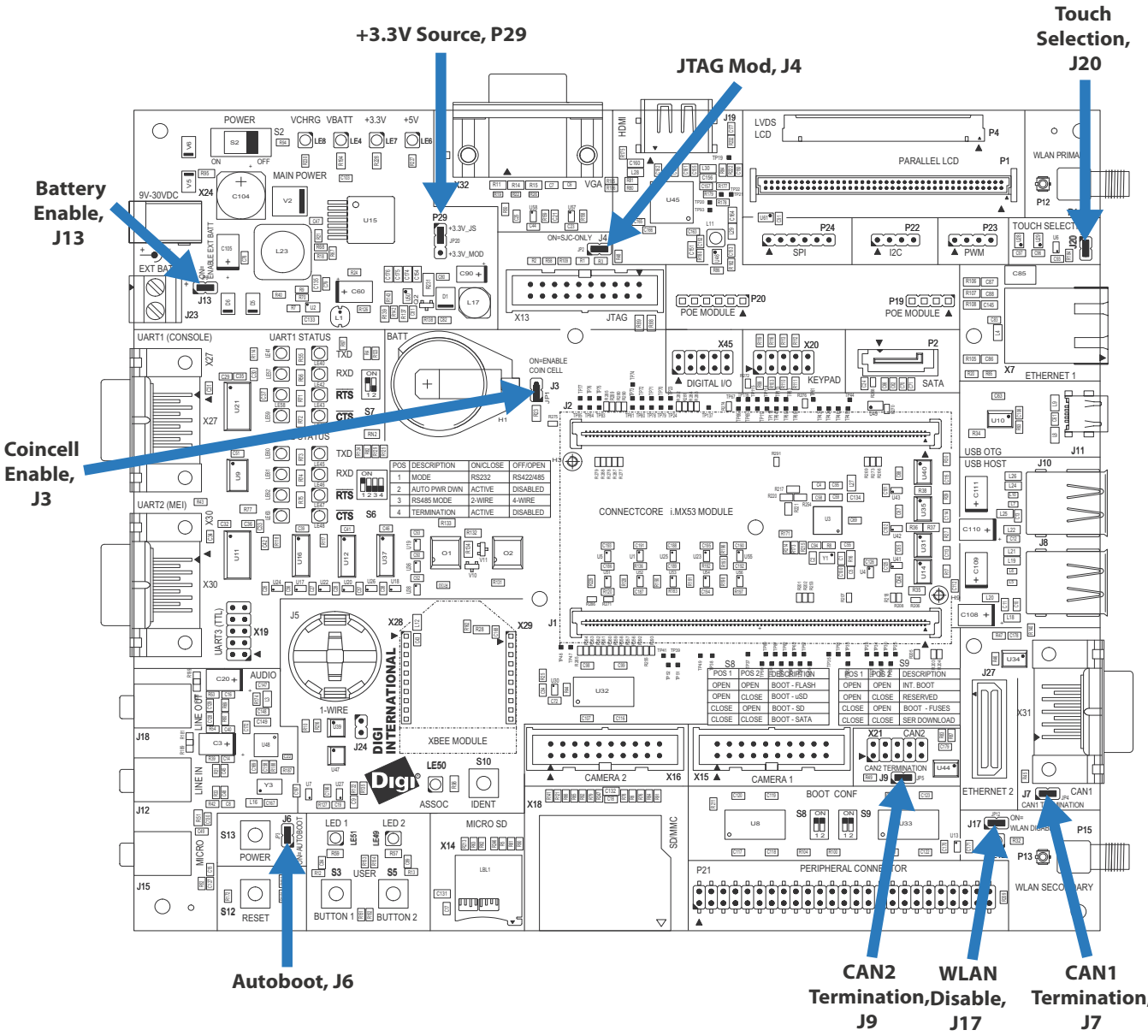
Switch Pin	Function	Comments
S8.1 / S8.2	Off / Off	Boot from NAND flash
S8.1 / S8.2	Off / On	Boot from microSD
S8.1 / S8.2	On / Off	Boot from SD
S8.1 / S8.2	On / On	Boot from SATA

Boot Mode Switch, S9

Use S9 to configure the module boot mode:

Switch Pin	Function	Comments
S9.1 / S9.2	Off / Off	Internal Boot
S9.1 / S9.2	Off / On	Reserved
S9.1 / S9.2	On / Off	Internal Boot configured by fuse block
S9.1 / S9.2	On / On	Serial downloader

Jumpers



Battery Enable, J13

When J13 is set, the development board can be powered by an external battery connected to J23.

+3.3V Source, P29

When set on positions 1-2, the +3.3V supply of the development board is generated in a voltage regulator provided on the development board.

When set on positions 2-3, the +3.3V supply of the development board is generated on the module.

WLAN Disable, J17

When J17 is set, the WLAN interface is disabled.

Touch Selection, J20

When J20 is set, an external SPI touch screen controller is configured for the Parallel LCD interface, and the internal analog touch screen controller (on module) is configured for the LVDS interface.

When J20 is removed, an external SPI touch screen controller is configured for the LVDS interface, and the internal analog touch screen controller (on module) is configured for the parallel LCD interface.

Coincell Enable, J3

When J3 is set, +3V from the lithium coin cell battery is supplied to the RTC, even if the board is switched off.

JTAG Mod, J4

When J4 is set, the Standard JTAG interface is the only debug capability enabled for the ConnectCore for i.MX53.

When J4 is removed, the Trace port is also enabled for debugging.

Autoboot, J6

When J6 is set, the module boots as soon as the power supplies are present.

When J6 is removed, a power on event is needed to turn on the module.

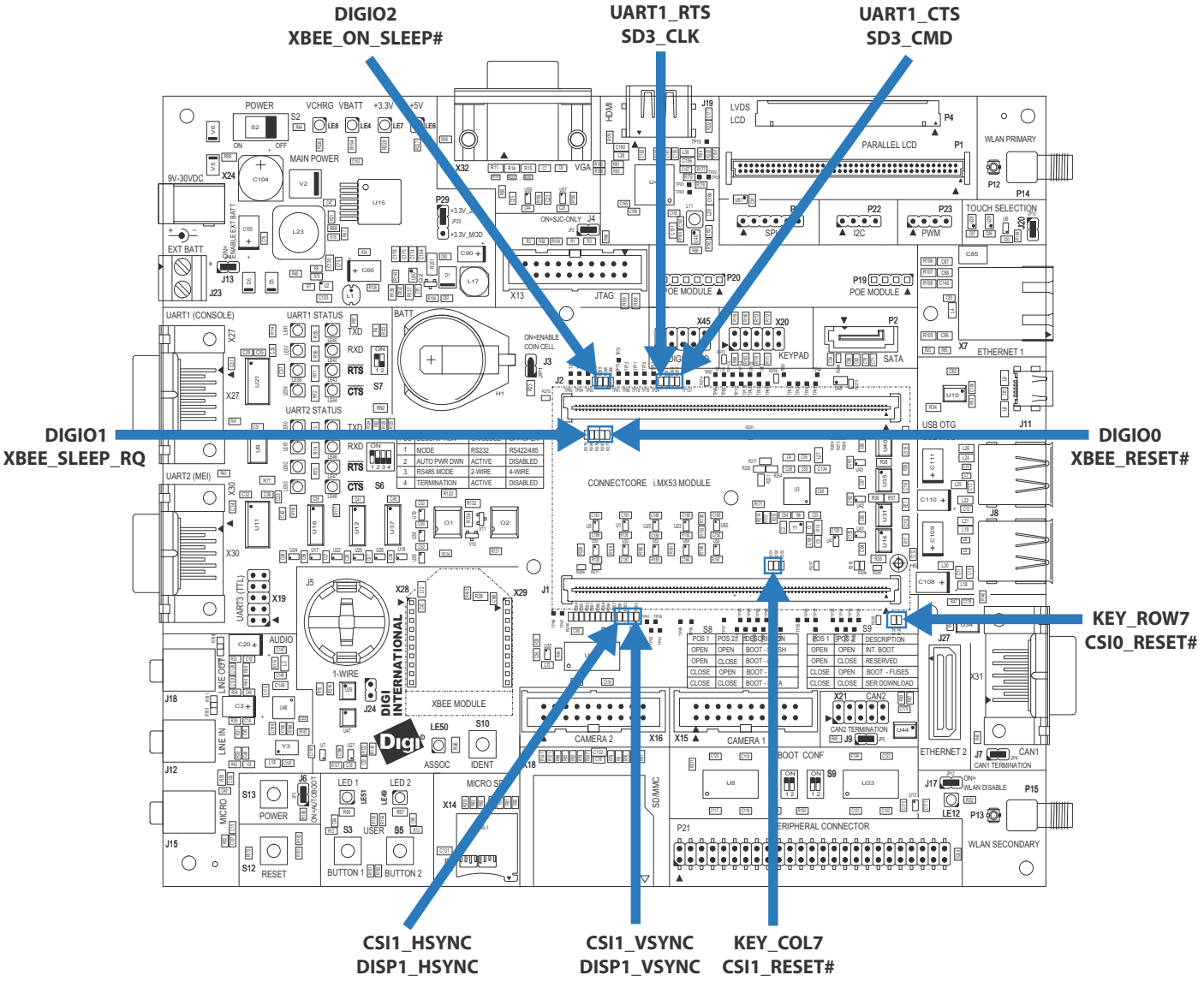
CAN1 Termination resistor, J7

When J7 is set, a 120 Ohm termination resistor is connected to the CAN 1 lines.

CAN2 Termination resistor, J9

When J9 is set, a 120 Ohm termination resistor is connected to the CAN 2 lines.

Configuration Resistors



CSI0_RESET#/KEY_ROW7, R203/R204

The development board provides two 0Ω resistors, R203 and R204 to select the interface where the KEY_ROW7/GPIO5_27 signal is connected. These two resistors should not be populated at the same time.

The following table shows the configuration of these two resistors:

Resistor	Signal Configuration	Note
R203	GPIO5_27	Populated by default
R204	KEY_ROW7	Non-populated by default

CSI1_RESET#/KEY_COL7, R201/R202

The development board provides two 0Ω resistors, R201 and R202 to select the interface where the KEY_COL7/GPIO5_26 signal is connected. These two resistors should not be populated at the same time.

The following table shows the configuration of these two resistors:

Resistor	Signal Configuration	Note
R201	GPIO5_26	Populated by default GPIO connected to Camera 2 reset
R202	KEY_COL7	Non-populated by default

CSI1_HSYNC#/DISP1_HSYNC, R256/R292

The development board provides two 0Ω resistors, R256 and R292 to select the interface where the EIM_DA11/CSI1_HSYNC signal is connected. These two resistors should not be populated at the same time.

The following table shows the configuration of these two resistors:

Resistor	Signal Configuration	Note
R256	CSI1_HSYNC	Non-populated by default Connected to Camera 2 HSYNC input
R292	DI1_PIN2	Populated by default Connected to VGA HSYNC output

CSI1_VSYNC#/DISP1_VSYNC, R255/R293

The development board provides two 0Ω resistors, R255 and R293 to select the interface where the EIM_DA12/CSI1_VSYNC signal is connected. These two resistors should not be populated at the same time.

The following table shows the configuration of these two resistors:

Resistor	Signal Configuration	Note
R255	CSI1_VSYNC	Non-populated by default Connected to Camera 2 VSYNC input
R293	DI1_PIN3	Populated by default Connected to VGA VSYNC output

UART1_CTS/SD3_CMD, R283/R284

The development board provides two 0Ω resistors, R283 and R284 to select the interface where the SD3_CMD/UART1_CTS signal is connected. These two resistors should not be populated at the same time.

The following table shows the configuration of these two resistors:

Resistor	Signal Configuration	Note
R283	UART1_CTS	Non-populated by default Connected to UART1
R284	SD3_CMD	Populated by default Connected to microSD connector

UART1_RTS/SD3_CLK, R281/R282

The development board provides two 0Ω resistors, R281 and R282 to select the interface where the SD3_CLK/UART1_RTS signal is connected. These two resistors should not be populated at the same time.

The following table shows the configuration of these two resistors:

Resistor	Signal Configuration	Note
R281	UART1_RTS	Non-populated by default Connected to UART1
R282	SD3_CLK	Populated by default Connected to microSD connector

DIGIO0/XBEE_RESET#, R277/R287

The development board provides two 0Ω resistors, R277 and R287 to select the interface where the GPIO6_15 signal is connected.

The following table shows the configuration of these two resistors:

Resistor	Signal Configuration	Note
R277	GPIO6_15	Populated by default Connected to DIGIO connector
R287	GPIO6_15	Populated by default Connected to XBee connector as XBee reset

DIGIO1/XBEE_SLEEP_RQ, R278/R288

The development board provides two 0Ω resistors, R278 and R288 to select the interface where the GPIO7_6 signal is connected.

The following table shows the configuration of these two resistors:

Resistor	Signal Configuration	Note
R278	GPIO7_6	Populated by default Connected to DIGIO connector
R288	GPIO7_6	Populated by default Connected to XBee connector as XBee sleep request

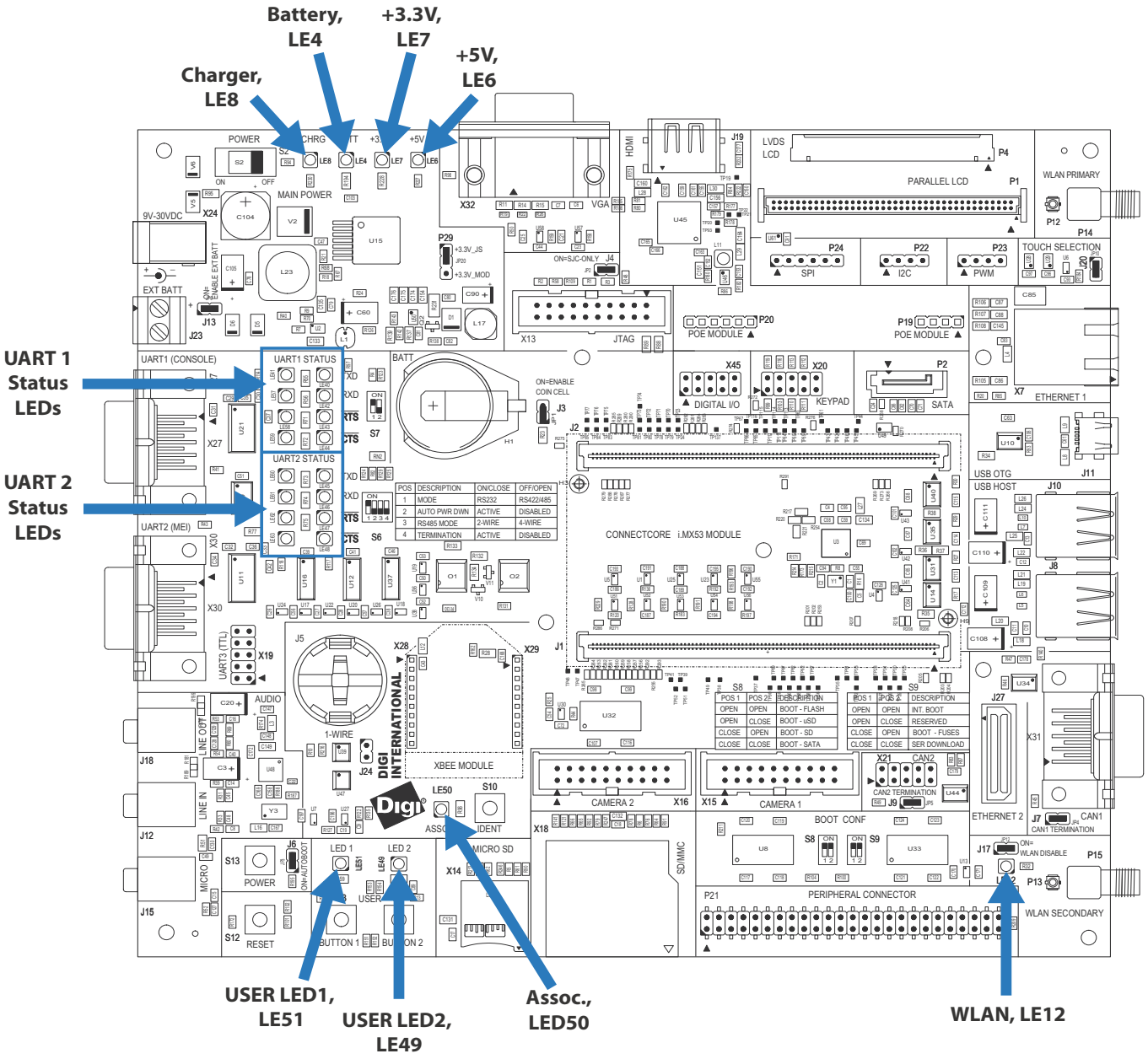
DIGIO2/XBEE_ON_SLEEP#, R280/R289

The development board provides two 0Ω resistors, R280 and R289 to select the interface where the GPIO6_16 signal is connected.

The following table shows the configuration of these two resistors:

Resistor	Signal Configuration	Note
R280	GPIO6_16	Populated by default Connected to DIGIO connector
R289	GPIO6_16	Populated by default Connected to XBee connector as XBee on/sleep status

LEDs



WLAN, LE12

Green LED indicating WLAN operational status.

Power LEDs LE4, LE6, LE7 and LE8

The power LEDs show the status of their power supplies. All power LEDs are red.

- LE4 ON indicates that battery power is present or that the DA9053 PMIC is charging the battery. The intensity of the LED will change depending on the battery voltage and depending on the charging voltage.
- LE6 ON indicates that +5VDC power for the development board is present
- LE7 ON indicates that +3.3VDC power for the development board is present
- LE8 ON indicates that charger power is present

User LEDs, LE49 and LE51

The user LEDs are controlled through applications running on the ConnectCore for i.MX53 module. You may use these module signals to implement the LEDs:

Signal Name	Button	GPIO Used
USER_LED1	LE51	GPIO5_20
USER_LED2	LE49	GPIO7_12

Serial Status LEDs

The development board has two sets of serial port LEDs - four for serial port 1 and four for serial port 2. The LEDs are connected to the TTL side of the RS232 or RS4xx transceivers.

- Green means corresponding signal high
- Red means corresponding signal low
- The intensity and color of the LED will change when the voltage is switching

UART 1 Status LEDs

LED Reference		Function
RED	GREEN	
LE41	LE40	TXD
LE57	LE42	RXD
LE58	LE43	RTS#
LE59	LE44	CTS#

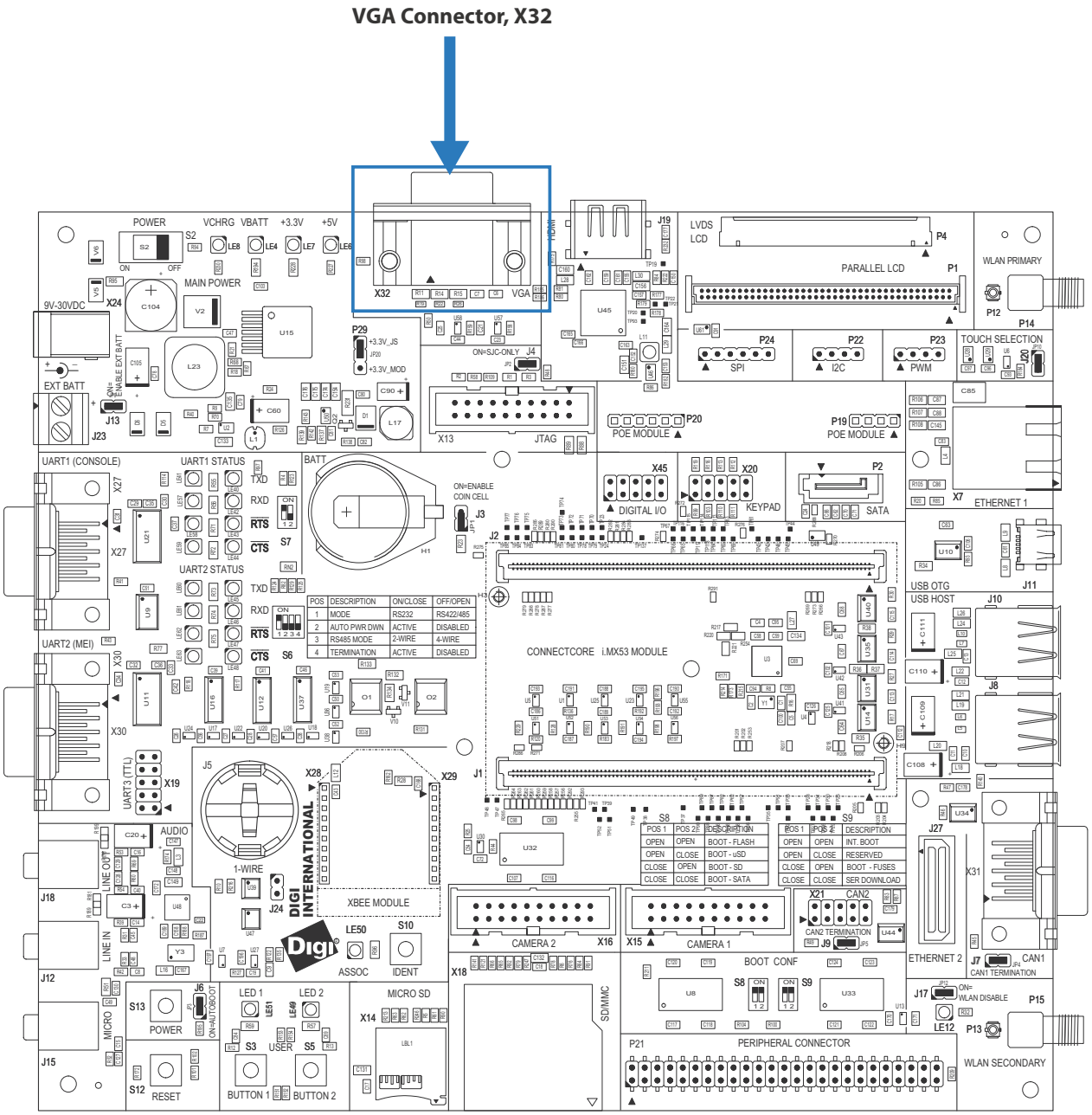
UART 2 Status LEDs

LED Reference		Function
RED	GREEN	
LE60	LE45	TXD
LE61	LE46	RXD
LE62	LE47	RTS#
LE63	LE48	CTS#

XBee Assoc., LE50

This LED is connected to the Associate output of the Digi XBee module. This LED provides information of the device's network status and diagnostics information. For a more in-depth description of this LED please refer to the Digi XBee module documentation available on the Digi website.

Analog Video Interface (VGA)



Analog Video Connector, X32

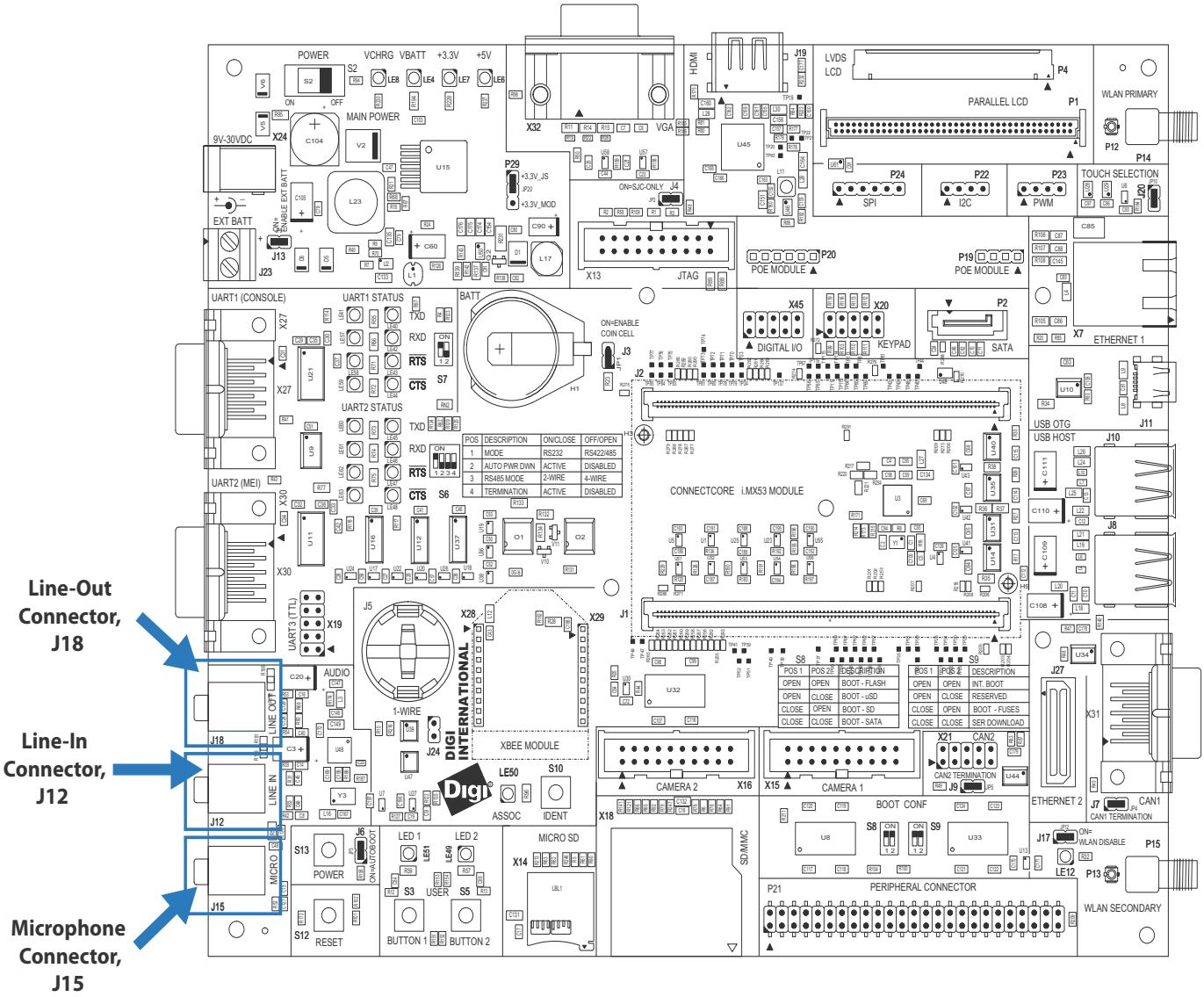
connector. The Analog Video interface is connected to the television encoder interface (TVE) and to the display 2 synchronization interface (DISP1) of the i.MX53 CPU.

The VGA interface shares share the functionality in the development board with the bootstrap interface and with the camera 2 interface. To avoid conflict between the camera 2/VGA signals and the bootstrap interface, a delay circuit is provided in the board to disable the camera 2 and the VGA interfaces while the bootstrap configuration is being reading by the i.MX53 CPU. Once the bootstrap configuration has been read the camera 2 and the VGA interfaces are enabled. To avoid conflicts between the camera 2 and the VGA interface 0Ω resistors are used to select the interface to be used. Please refer to the "Configuration Resistors" section on page 79 for detailed information.

The table below shows the pinout of the Analog Video connector.

Pin	Signal
1	VGA_RED
2	VGA_GREEN
3	VGA_BLUE
4	-
5	GND
6	RED_RETURN
7	GREEN_RETURN
8	BLUE_RETURN
9	-
10	GND
11	-
12	-
13	DISP1_HSYNC#
14	DISP1_VSYNC#
15	-

Audio Interface



The development board provides an audio interface with line in, line out, and microphone in. The Freescale SGTL5000 audio CODEC on the development board is controlled through I^2C port 3 of the ConnectCore for i.MX53 module. Digital audio data is sent/receive between the audio CODEC and the module through the I^2S interface (AUD5 channel of the i.MX53 AUDMUX).

Interface	I^2C Address (7 bits)
Audio CODEC (SGTL5000)	0 x 1A

Three stereo audio jacks are provided on the development board:

- J18 connector for LINE-OUT
- J12 connector for LINE-IN
- J15 connector for microphone

Line-out Connector Pinout, J18

Pin	Signal
1	GND
2	LINE-OUT-RIGHT
3	LINE-OUT-LEFT
4	-
5	HEADPHONE-DETECT

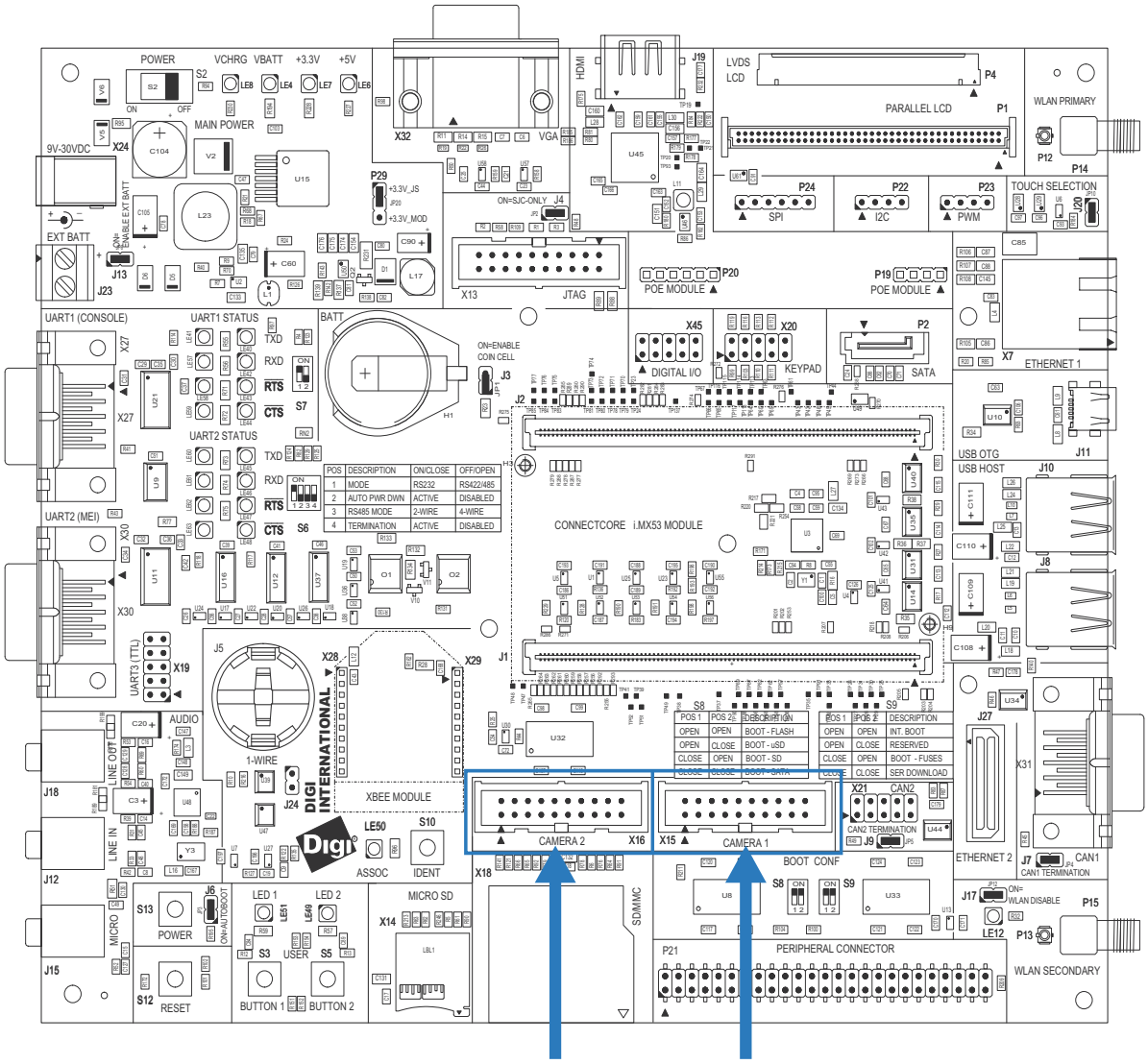
Line-in Connector Pinout, J12

Pin	Signal
1	GND
2	LINE-IN-RIGHT
3	LINE-IN-LEFT
4	GND
5	GND

Microphone Connector Pinou, J15

Pin	Signal
1	GND
2	MIC-IN
3	MICBIAS
4	GND
5	GND

Camera Interfaces



The development board provides two camera interfaces connected to the camera sensor interfaces (CSI) of the i.MX53 CPU. The I^2C bus 3 of the ConnectCore for i.MX53 module is used to configure and control connected cameras.

Two 2x10 pin headers, X15 and X16, are provided on the development board for optional Digi camera application kits or customer specific camera hardware.

- X15 connector for camera 1
- X16 connector for camera 2

The camera 2 signals share the functionality in the development board with the bootstrap interface and with the VGA interface. To avoid conflict between the camera 2/VGA signals and the bootstrap interface, a delay circuit is provided in the board to disable the camera 2 and the VGA interfaces while the bootstrap configuration is being reading by the i.MX53 CPU. Once the bootstrap configuration has been read the camera 2 and the VGA interfaces are enabled. To avoid conflicts between the camera 2 and the VGA interface 0Ù resistors are used to select the interface to be used. Please refer to the "Configuration Resistors" section on page 79 for detailed information.

The following table shows the I^2C device addresses of the Digi camera application kits:

Interface	I^2C Address (7 bits)
Camera 1	0 x 5C
Camera 2	0 x 48

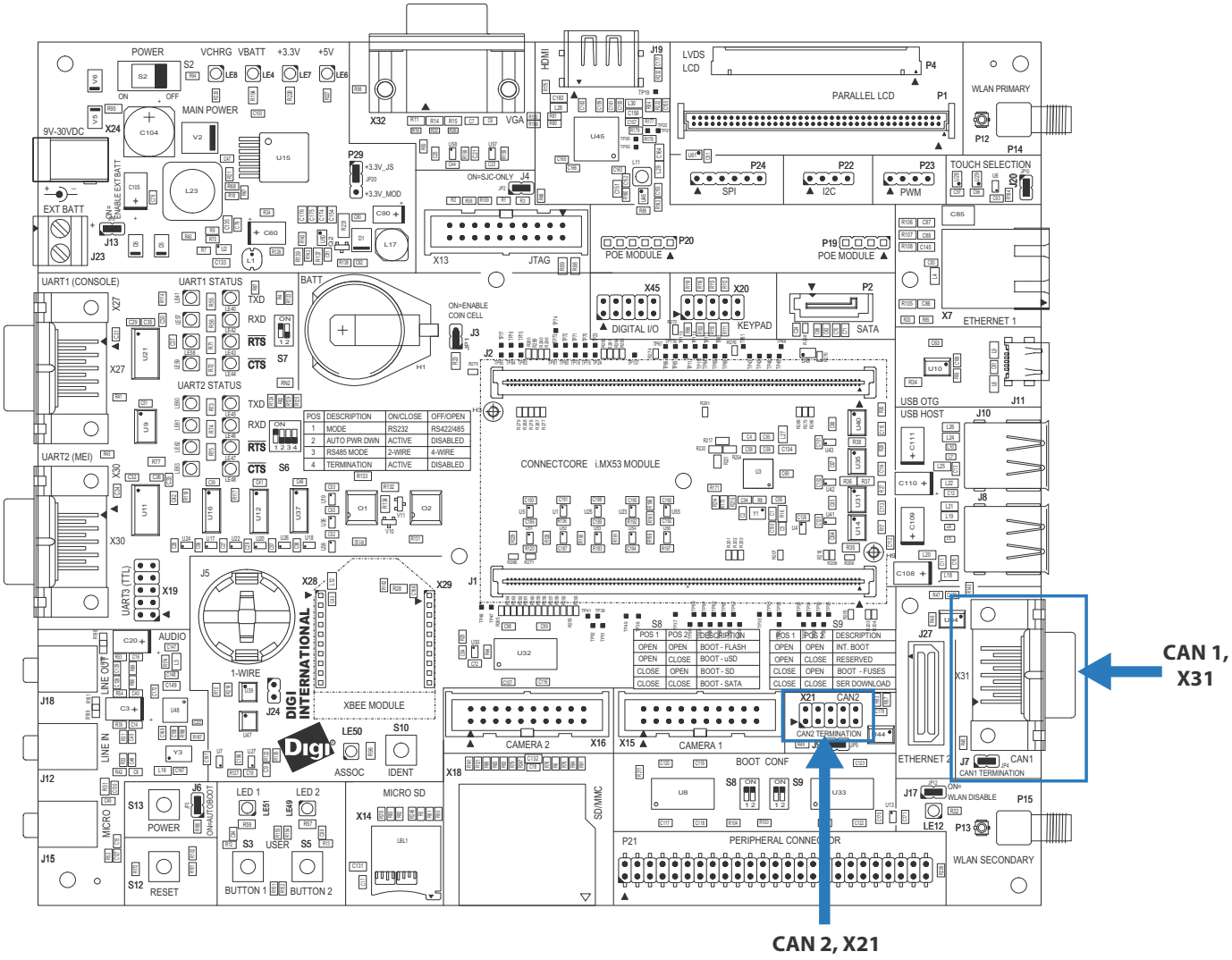
X15 Pinout

Pin	Signal	Pin	Signal
1	+2.775V	2	GND
3	CSI0_D12	4	CSI0_D13
5	CSIO_D14	6	CSI0_D15
7	CSI0_D16	8	CSI0_D17
9	CSI0_D18	10	CSI0_D19
11	CSI_MCLK	12	CSI0_PIXCLK
13	CSI0_HSYNC	14	CSI0_VSYNC
15	I2C3_SCL	16	I2C3_SDA
17	-	18	GPIO5_29/CSI0_RESET#
19	GND	20	-

X16 Pinout

Pin	Signal	Pin	Signal
1	+2.775V	2	GND
3	CSI1_D12	4	CSI1_D13
5	CSI1_D14	6	CSI1_D15
7	CSI1_D16	8	CSI1_D17
9	CSI1_D18	10	CSI1_D19
11	CSI_MCLK	12	CSI1_PIXCLK
13	CSI1_HSYNC	14	CSI1_VSYNC
15	I2C3_SCL	16	I2C3_SDA
17	-	18	GPIO5_26/CSI1_RESET#
19	GND	20	-

CAN Interface



CAN 1, X31

The CAN 1 connector X31, is a DB-9 male connector. One 120 ohm termination resistor can be connected to the output lines of the CAN 1 bus. The termination resistor can be connected or disconnected using the jumper J7. Refer to the "Jumpers" section on page 77 for more information.

CAN 1 pins are allocated as shown:

Pin	Function
1	-
2	CAN1L
3	GND
4	-
5	-
6	GND
7	CAN1H
8	-
9	-
10	-

CAN 2, X21

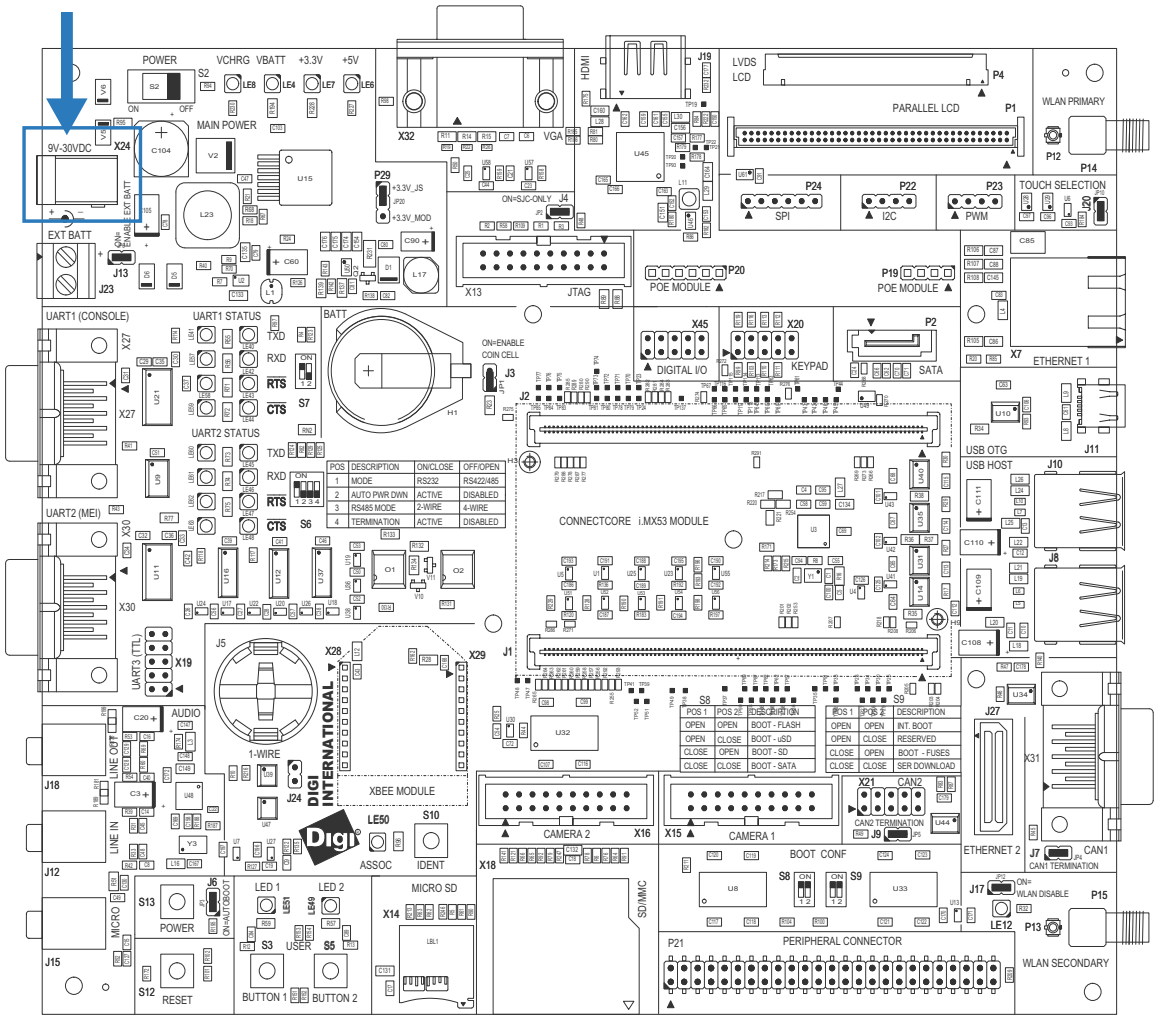
The CAN 2 connector X21, is a 2x5 pin header. One 120 ohm termination resistor can be connected to the output lines of the CAN 2 bus. The termination resistor can be connected or disconnected using the jumper J9. Refer to the "Jumpers" section on page 77 for more information.

CAN 2 pins are allocated as shown:

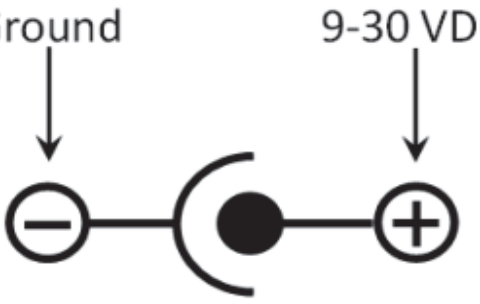
Pin	Function
1	-
2	CAN2L
3	GND
4	-
5	-
6	GND
7	CAN2H
8	-
9	-

Charger Power Connector

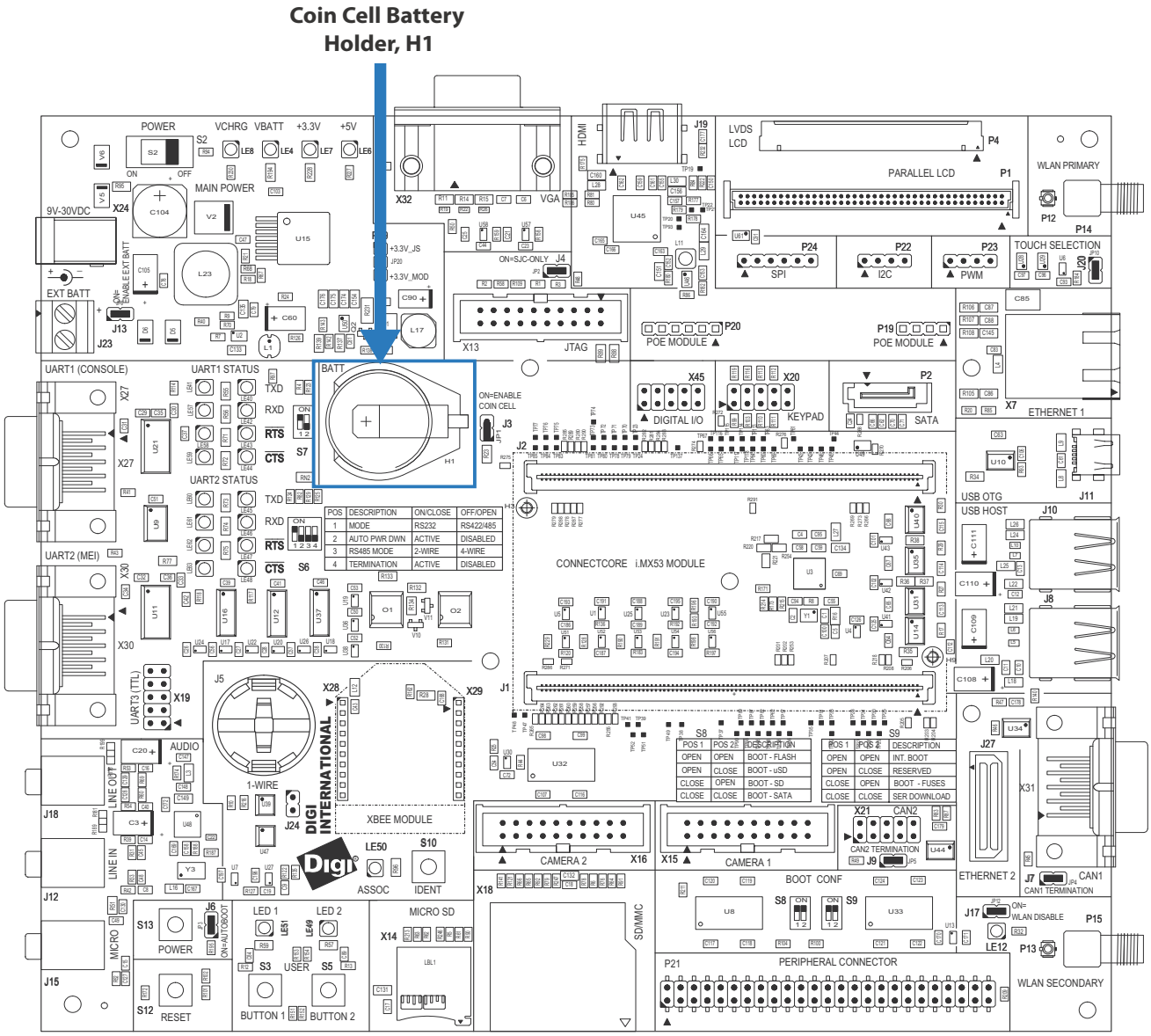
Charger Power Connector, X24



The charger power connector (X24) is a barrel connector for the development board's 9-30VDC power supply. The figure below shows the polarity.

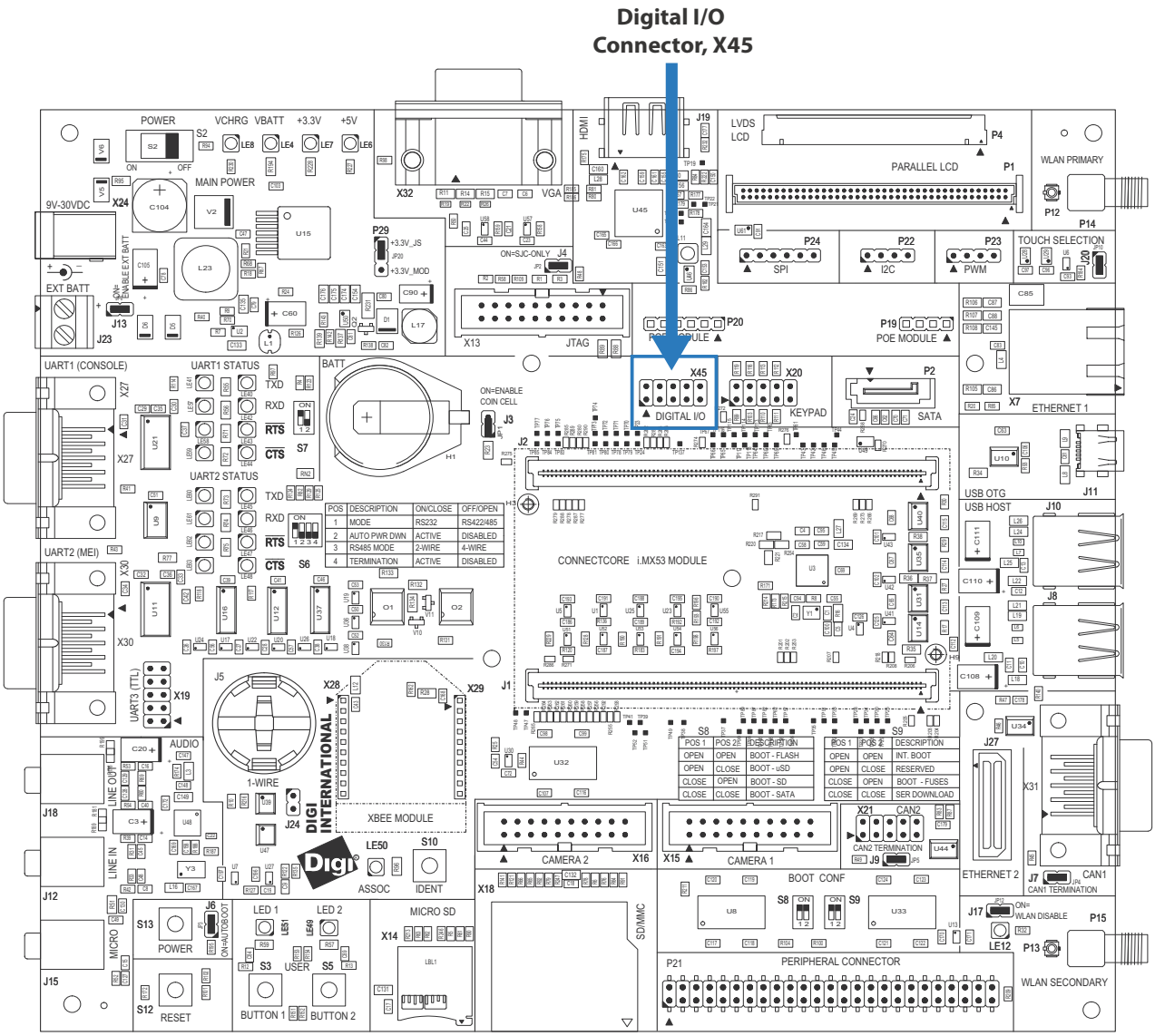


Coin Cell Battery



The development board provides a coin cell battery to back up the module's integrated RTC while main power is disconnected. Jumper J3 connects/disconnects the coin cell power source.

Digital IO Interface



Digital I/O Connector, X45

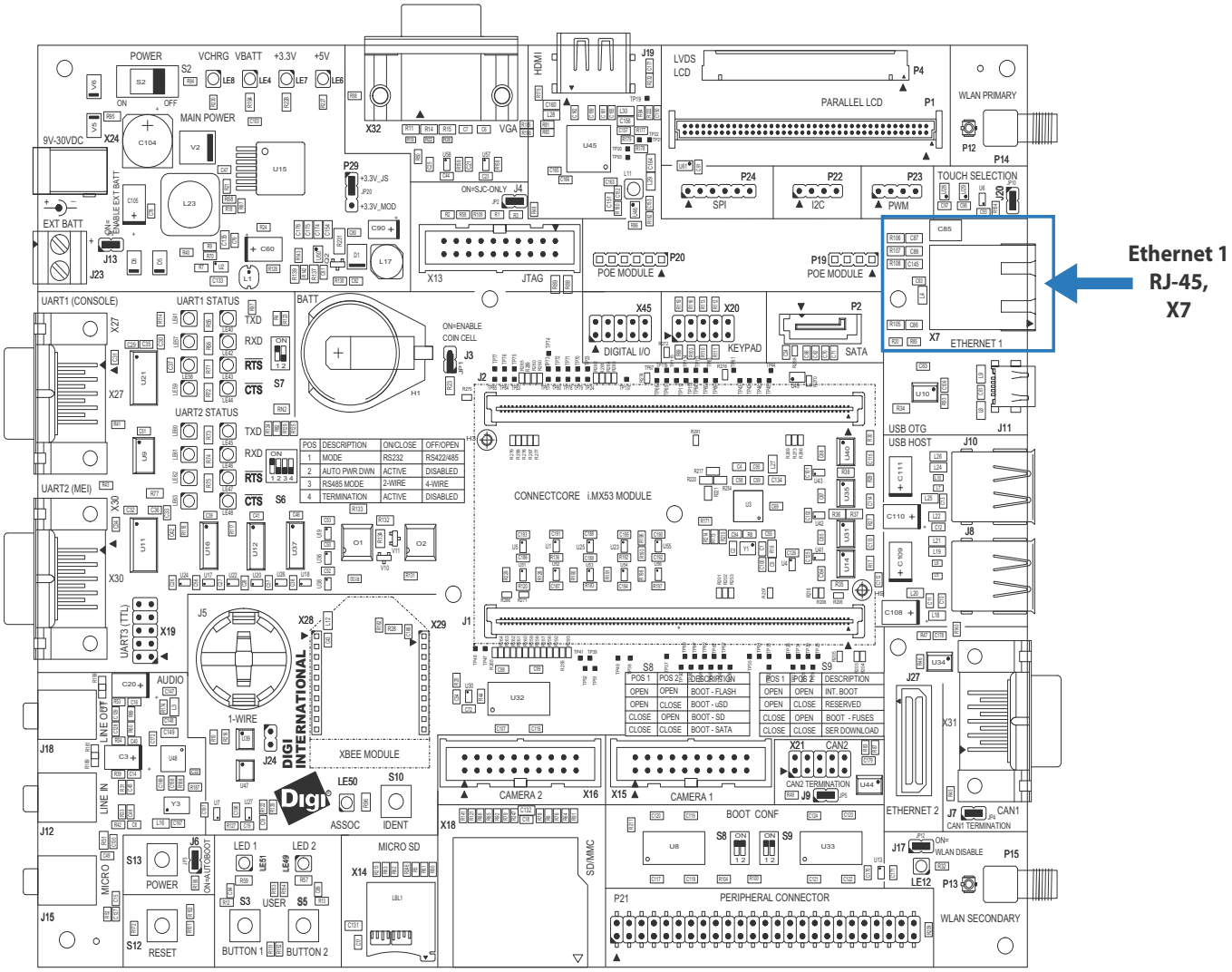
The development board provides a 2x5 position pin header, X45, to access four on-chip digital GPIOs of the i.MX53 CPU.

Pin	Signal	GPIO	Voltage Level
1	DIGIO0	GPIO6_15	+3.15V
2	NC		
3	DIGIO1	GPIO7_6	+3.15V
4	NC		
5	DIGIO2	GPIO6_16	+3.15V
6	NC		
7	DIGIO3	GPIO6_14	+3.15V
8	GND	GND	0V
9	GND	GND	0V

On the development board, GPIO6_15, GPIO6_16 and GPIO7_6 are connected to the XBee interface. When using these signals as digital I/O, the XBee interface should not be used.

Note: The digital I/O interface is not-protected against ESD, over-voltage or inverse polarity. Care must be taken when using these signals.

Ethernet 1 Interface



The development board provides one 8-wire RJ-45 jack with integrated 1:1 transformers and link/activity LEDs for the Ethernet 1 interface. This interface is attached to the Fast Ethernet controller (FEC) of the i.MX53. The ConnectCore for Wi-i.MX53 module provides a 10/100 Ethernet PHY chip for this interface.

The Ethernet 1 RJ-45 connector also supports 802.3af (PoE) operation (optional Digi PoE application kit required).

Ethernet 1, RJ-45 Connector X7

The table below shows the pinout of the Ethernet 1 RJ-45 connector.

Pin	Signal	802.3af End-Span (mode A)	802.3ad Mid-Span (mode B)	Description
1	TXD+	Negative V_{Port}		Transmit data+
2	TXD-	Negative V_{Port}		Transmit data-
3	RXD+	Positive V_{Port}		Receive data+
4	EPWR+		Positive V_{Port}	Power from switch+
5	EPWR+		Positive V_{Port}	Power from switch+
6	RXD-	Positive V_{Port}		Receive data-
7	EPWR-		Negative V_{Port}	Power from switch-
8	EPWR-		Negative V_{Port}	Power from switch-

The table below shows the description of the Ethernet 1 LEDs.

LED	Description
Yellow	Network activity (speed): - Flashing - indicates network traffic - Off - no network traffic
Green	Network link: - On - indicates an active network link - Off - no network link present