3000/4000 SERIES SYNCHRONOUS WRITE TAPE TRANSPORT

Peripheral Equipment Corporation

PEC

J201	Reel Servo	100129-01
J202	Capstan Drive Synch.	100475-03
J203	Function Control, Syn. B	100443-02
J204	Transmitters, DTL	100339-01
J205	Receivers, DTL	100334-01
J206	Double Buffer, 9-Channel W/A	100239-01
J208	CRC	100265-01
J209	Function Control, Syn. A	100359-01

MODEL NO. 4800-9

SERIAL NO. 380094

3000/4000 SERIES SYNCHRONOUS WRITE TAPE TRANSPORT

OPERATING AND SERVICE MANUAL

Peripheral Equipment Corporation

CHATSWORTH, CALIF. 91311
TELEPHONE (213) 882-0030 TWX: (910) 494-2093

MANUAL NO. 100605

PEC

FOREWORD

This manual provides operating and servicing instructions for the Synchronous Write Tape Transport, 3000 and 4000 Series, manufactured by PERIPHERAL EQUIPMENT CORPORATION, Chatsworth, California.

The content includes a detailed description, specifications, installation instructions and checkout of the tape transport. Also included is the theory of operation and preventive maintenance instructions. Section VII contains the schematics, parts lists, and wiring diagrams necessary to provide an understanding of the transport and to perform troubleshooting when required. The Glossary contains definitions of abbreviations referred to in this manual.

All graphic symbols used in logic diagrams conform to the requirements of MIL-STD-806 and all symbols used in schematic diagrams are as specified in MIL-STD-15.

The models of tape transports covered by this manual are listed in the following tabulation.

3000 Series	4000 Series	Bit Packing Density (bpi)	Character Rate at 25 ips (KHz)	Number of Channels
3800-9	4800-9	800	20	9
3800-7	4800-7	800	20	7
3500	4500	556	13.9	7
3200	4200	200	5	7

SERVICE AND WARRANTY

This tape unit has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected from manufacturers "off the shelf" stock. Should a component fail, it may be readily replaced from PEC or your local supplier. The tape unit has been designed for "plug-in" replacement of circuit boards or major components which will ensure a minimum of equipment down time.

PEC warrants its equipment and materials to be free from defects in material and workmanship under normal use and service for a period of 12 months from the original date of shipment. Under the warranty period, the company's obligation being limited to repairing or replacing any defective part or parts of such products that are returned to PEC. All repairs and replacements made under this warranty are F. O. B. company's factory shipping point or company designated service depot.

Please read the instruction manual thoroughly as to operation, maintenance and component reference list. Should you require additional assistance in servicing this equipment, please contact the following regional Service Centers. A trained service representative will be pleased to assist you.

FIELD SERVICE OFFICES

Chatsworth, California	(213) 882-0030	Brussels, Belgium	02-358065
Houston, Texas	(713) 622-3620	Munich, Germany	5133056
Waltham, Massachusetts	(617) 899-0126	Stockholm, Sweden	(08) 870240
Ottawa, Canada	(613) 725-3354	Geneva, Switzerland	358-415

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SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1-1. INTRODUCTION

This section provides a functional description, physical description, and specifications for the Synchronous Write Tape Transport, 3000 and 4000 Series, manufactured by PERIPHERAL EQUIPMENT CORPORATION, Chatsworth, California.

1-2. PURPOSE OF EQUIPMENT

The Synchronous Write Tape Transport can record digital data on 7- (or 9-) track magnetic tape in IBM-compatible format, at speeds up to 25 ips. This transport accepts data at the corresponding rate up to a maximum of 20,000 characters per second.

The transport operates directly from 117- or 230-volts ac single-phase 48 to 400 Hz power.

1-3. PHYSICAL DESCRIPTION OF EQUIPMENT

The 3000 Series Transport is shown in Figure 1-1 and utilizes an 8-1/2 inch tape reel. All electrical and mechanical components that are necessary to operate the transport are contained within a single unit designed to mount on the standard 19-inch retma rack.

The transport mechanism is mounted on the front plate, which is hinged to provide easy access to the electrical components and the printed circuit boards. The dust cover, which is also hinged, affords protection to the magnetic tape, magnetic head, capstan, and other tape components from dust and other contaminants.

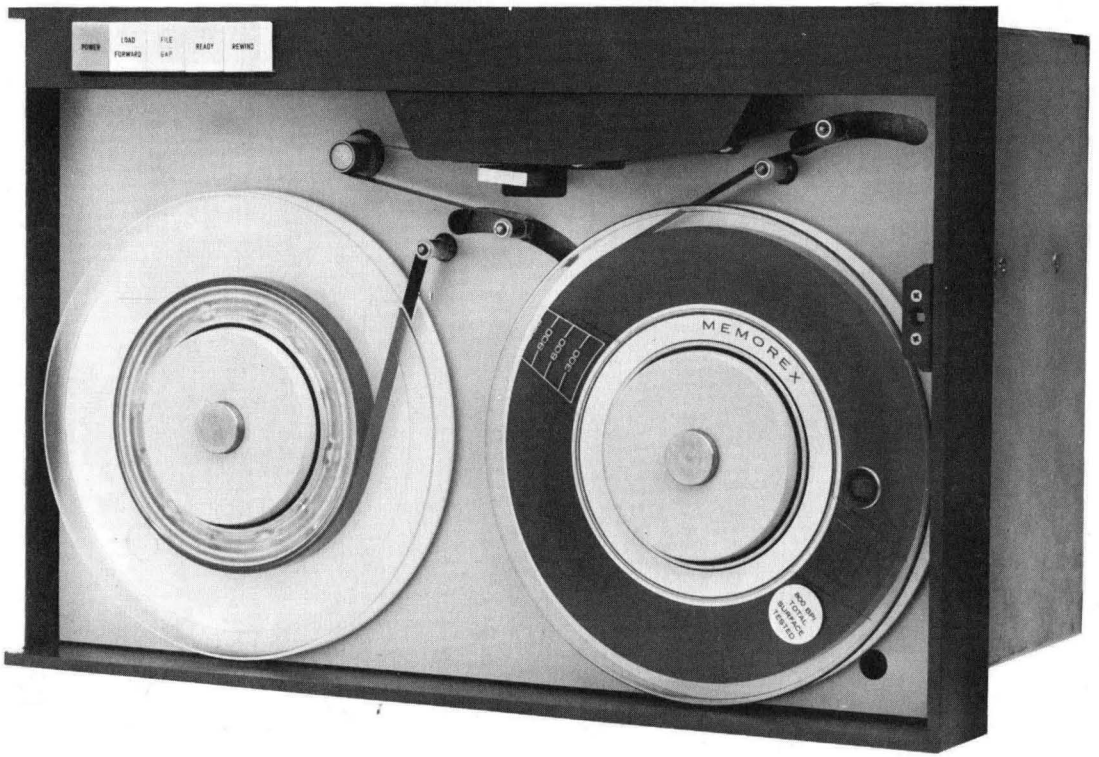

Figure 1-1. Tape Transport (8-1/2 Inch Reel)

The operational controls, which illuminate when the relevant function is being performed, are mounted on the front plate and are accessible with the dust cover door closed. Two connectors, one for power and one for interface lines, are mounted on the rear panel.

The 4000 Series Transport, shown in Figure 1-2, utilizes a 10-1/2 inch tape reel and also mounts in the standard 19-inch retma rack. Except for the physical size, the 4000 Series Transport is almost identical to the 3000 Series Transport.

1-4. FUNCTIONAL DESCRIPTION

Figure 1-3 shows a block diagram of the system. The transport utilizes a single capstan drive for controlling tape motion during the normal recording and rewind modes. This provides several operating advantages. It minimizes the number of mechanical components required to handle magnetic tape and completely eliminates troublesome parts such as pinch rollers (a major skew-producing component). The tape is always under a constant tension of 8 ounces, thus eliminating the possibility of tape "cinch" when the tape reel is placed on a computer transport.

The capstan is controlled by a velocity servo. The velocity information is generated using a dc tachometer that is directly coupled to the capstan motor shaft and produces a voltage that is directly proportional to the rotational velocity of the capstan. This voltage is compared to a reference voltage from the ramp generators using operational amplifier techniques and the difference is used to control the capstan motor. This capstan control technique gives precise control of tape accelerations and tape velocities, thus minimizing tape tension transients.

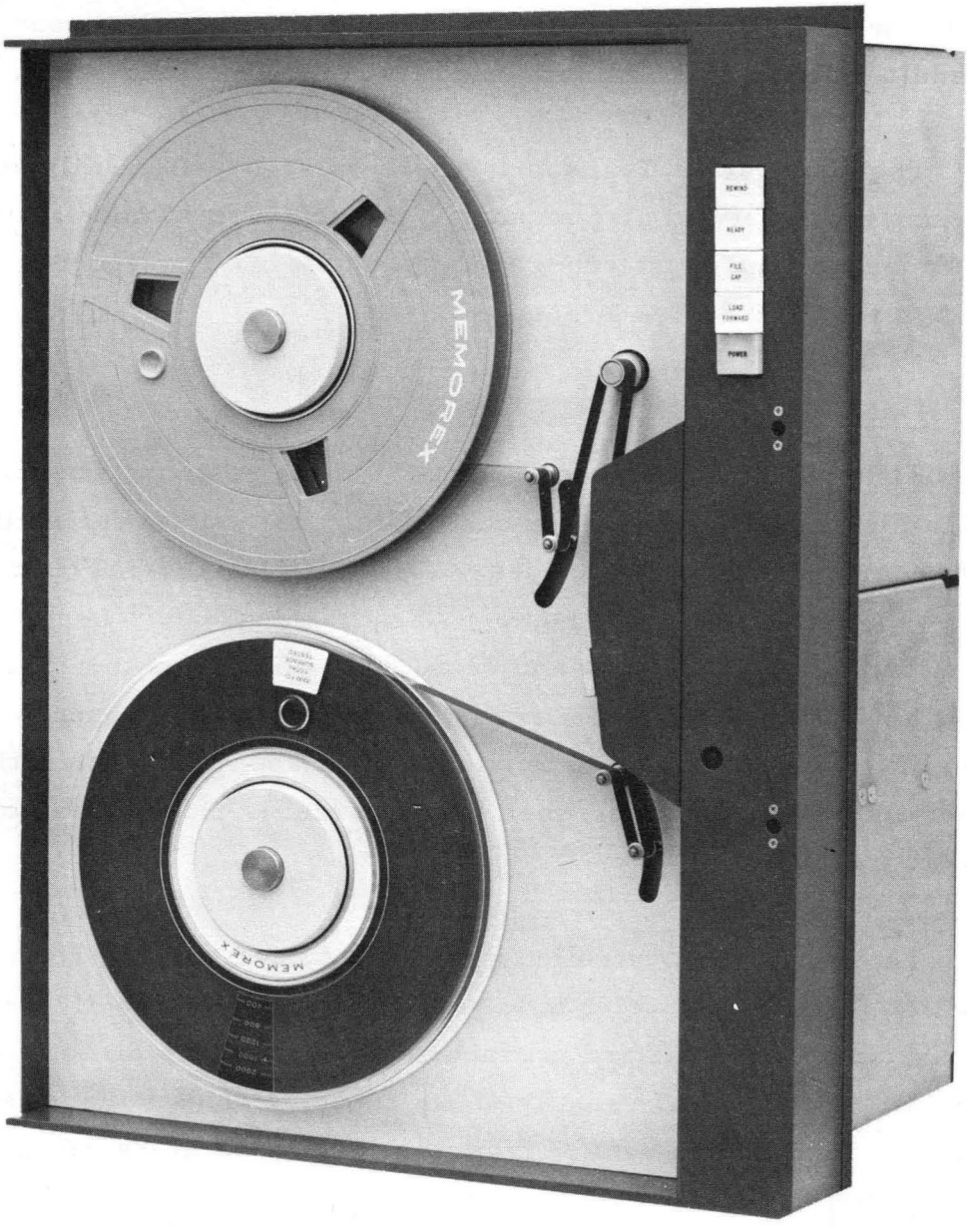

Figure 1-2. Tape Transport (10-1/2 Inch Reel)

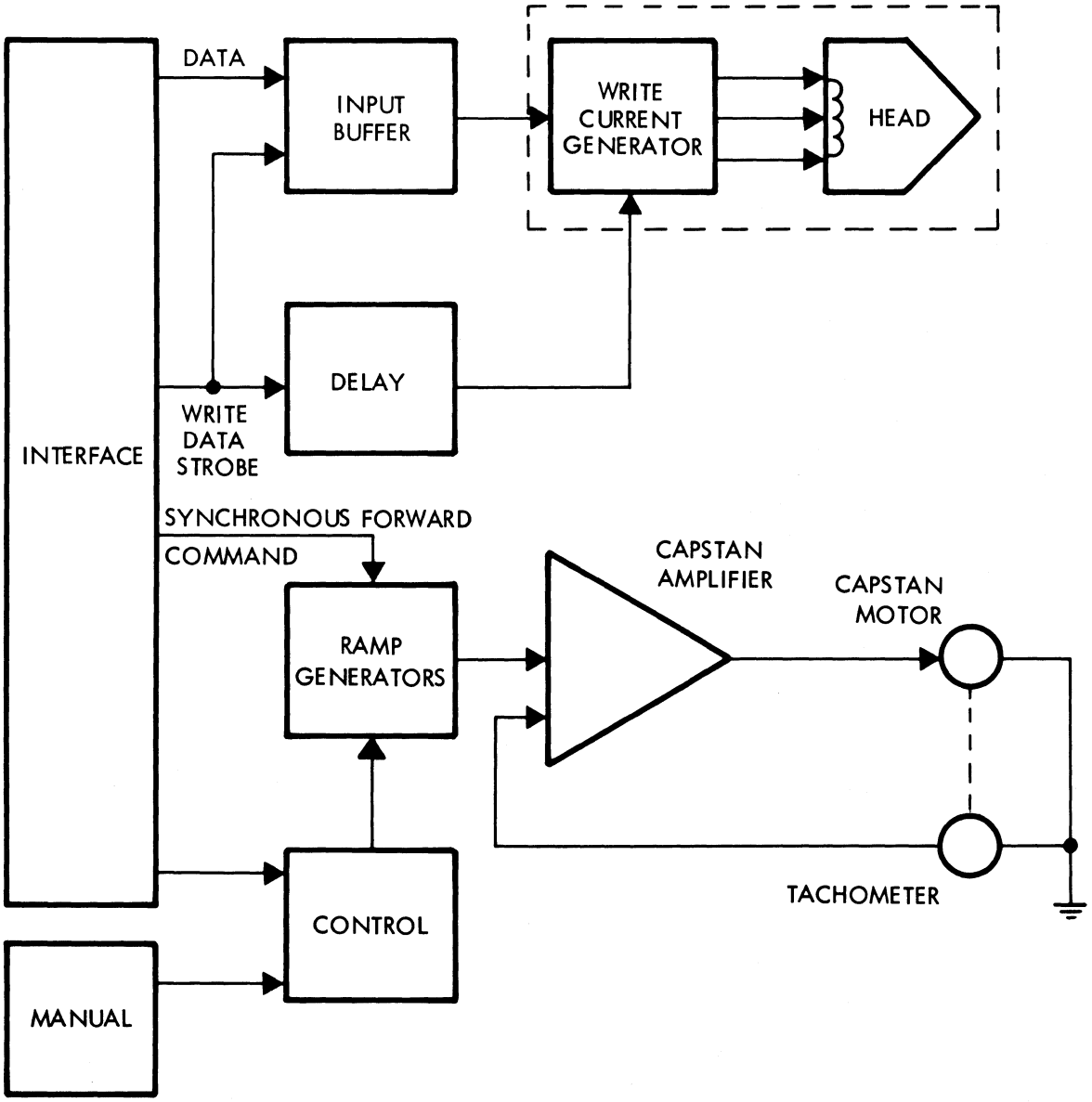

Figure 1-3. Block Diagram of
Synchronous Write Tape Transport, 3000/4000 Series

During a Writing operation, the tape is accelerated in a controlled manner to the required velocity. This velocity is maintained constant and data characters are written on the tape at a constant rate such that:

$$\text{Bit density} = \frac{\text{Character Rate}}{\text{Tape Velocity}}$$

When data recording is complete, the tape is decelerated to zero velocity in a controlled manner.

Since the writing operation relies on a constant tape velocity, Inter-Record Gaps (IRGs) (containing no data), must be provided to allow for the tape acceleration and deceleration periods. Control of tape motion to produce a defined IRG is provided in conjunction with the tape acceleration and deceleration characteristics defined within the transport.

In addition to the capstan control system, the transport consists of a mechanical tape storage system, supply and take-up reel servo systems, write head and its associated electronics, and the control logic.

The mechanical storage system buffers the relatively fast starts and stops of the capstan from the high inertia of the supply and take-up reels. As tape is taken from or supplied to the storage system, a long-life potentiometer measures the displacement of the storage arm and feeds an error signal to the reel motor amplifier. This signal is amplified and used to control the reel motor such that the reel will either supply or take up tape to maintain the storage arm in its nominal operating position. The storage arm system is designed to give a constant tape tension as long as the arm is within its operating

region. This tape path design minimizes tape wear because there is only relative motion of the tape oxide at the magnetic head and the head guides.

The magnetic head writes the flux transitions on the tape under control of the data electronics.

The control logic operates on manual or remote commands and controls tape motion for synchronously writing IBM-compatible tapes.

The transport is also supplied with a photoelectric sensor for detection of the Beginning-of-Tape (BOT) tab and End-of-Tape (EOT) tab. The BOT signal is used internally in the transport for control purposes and both BOT and EOT signals are sent as levels to the customer.

The transport is designed with an interlock control to protect the tape from damage due to component or power failure.

1-5. SPECIFICATIONS

1-6. MECHANICAL AND ELECTRICAL SPECIFICATIONS

The mechanical and electrical specifications for the tape transport are shown in Table 1-1.

1-7. INTERFACE SPECIFICATIONS

One interface is available with the Synchronous Write Tape Transport. This is the DTL interface that is described in the following paragraphs.

The interface circuits are designed so that a disconnected wire results in a false signal being interpreted at the receiver end of the wire. The customer must have specified which interface alternative is required (see Figure 1-4).

Table 1-1

Mechanical and Electrical Specifications

	3000 Series	4000 Series
Tape (computer grade)		
Width (inches)	0.5	0.5
Thickness (mil)	1.5	1.5
Tape Tension (ounces)	8.0	8.0
Reel Diameter (inches)	8.5	10.5
Recording Mode (IBM compatible)	NRZ1	NRZ1
Tape Speed (ips) Standard	25.0	25.0
Instantaneous Speed Variation (%)	±3	±3
Long-Term Speed Variation (%)	±1	±1
Rewind Speed (ips)	75 nominal	75 nominal
Interchannel Displacement Error* (static and dynamic)		
800 bpi (microinches)	150 maximum	150 maximum
556 bpi (microinches)	200 maximum	200 maximum
Start/Stop Time (milliseconds)**	$\frac{431.25 \pm 18.75 \text{ ms}}{\text{Tape Velocity (ips)}}$	$\frac{431.25 \pm 18.75 \text{ ms}}{\text{Tape Velocity (ips)}}$
Start/Stop Displacement (inch)**	0.21 ±0.02	0.21 ±0.02
Beginning of Tape (BOT) and End of Tape (EOT) Detectors	Photoelectric*** IBM compatible	Photoelectric*** IBM compatible
Weight (pounds)	60.0	85.0
Dimensions		
Height (inches)	12.25	24.5
Width (inches)	19.0	19.0
Depth (inches) (from mounting surface)	11.7	11.7
Depth (inches) (total)	14.0	15.0
Operating Temperature (°F)	35 to 122	35 to 122
Altitude (feet)	0 to 20,000	0 to 20,000
Power		
(volts ac)	117 or 230	117 or 230
(watts)	120	250
(Hz)	48 to 400	48 to 400
Mounting	Standard 19-inch retma rack	Standard 19-inch retma rack
Electronics	All silicon DTL Logic	All silicon DTL Logic

*This is defined as the maximum displacement between any two bits of a character when the tape is written with all "ones".

**Start time and distance are related to actual tape motion and do not include start delays.

***Approximate distance from detection area to head gap equals 1.2 inches.

1-8. DTL Interface

Levels: Consistent with circuit configurations shown in Figure 1-4.

Noise margins are as shown in Table 1-2.

Pulses: Minimum pulse width of 2 μseconds.

Maximum width of 10 milliseconds, except WRITE DATA STROBE (see Paragraph 3-10).

Edge transmission delay not greater than 200 nanoseconds.

It is assumed that interconnection of PERIPHERAL EQUIPMENT CORPORATION and Customer equipment uses a harness of individual twisted pairs, each with the following characteristics.

(1) Maximum length of 20 feet.

(2) Not less than 1 twist per inch.

(3) 22 gauge or 24 gauge conductor with minimum insulation thickness of 0.01 inch.

It is important that the ground side of each twisted pair is grounded within a few inches of the customer's interface card to which it is connected.

Figure 1-4 shows the configuration for which the PERIPHERAL EQUIPMENT CORPORATION transmitters and receivers have been designed. Noise margins will depend on the circuit configuration, ambient temperature, and whether the interface line is in a high or low state.

In the high state, the relative movement of the transmitter +5-volt line and receiver ground is important. In the low state, transmitter-ground-to-receiver-ground relative movement is important.

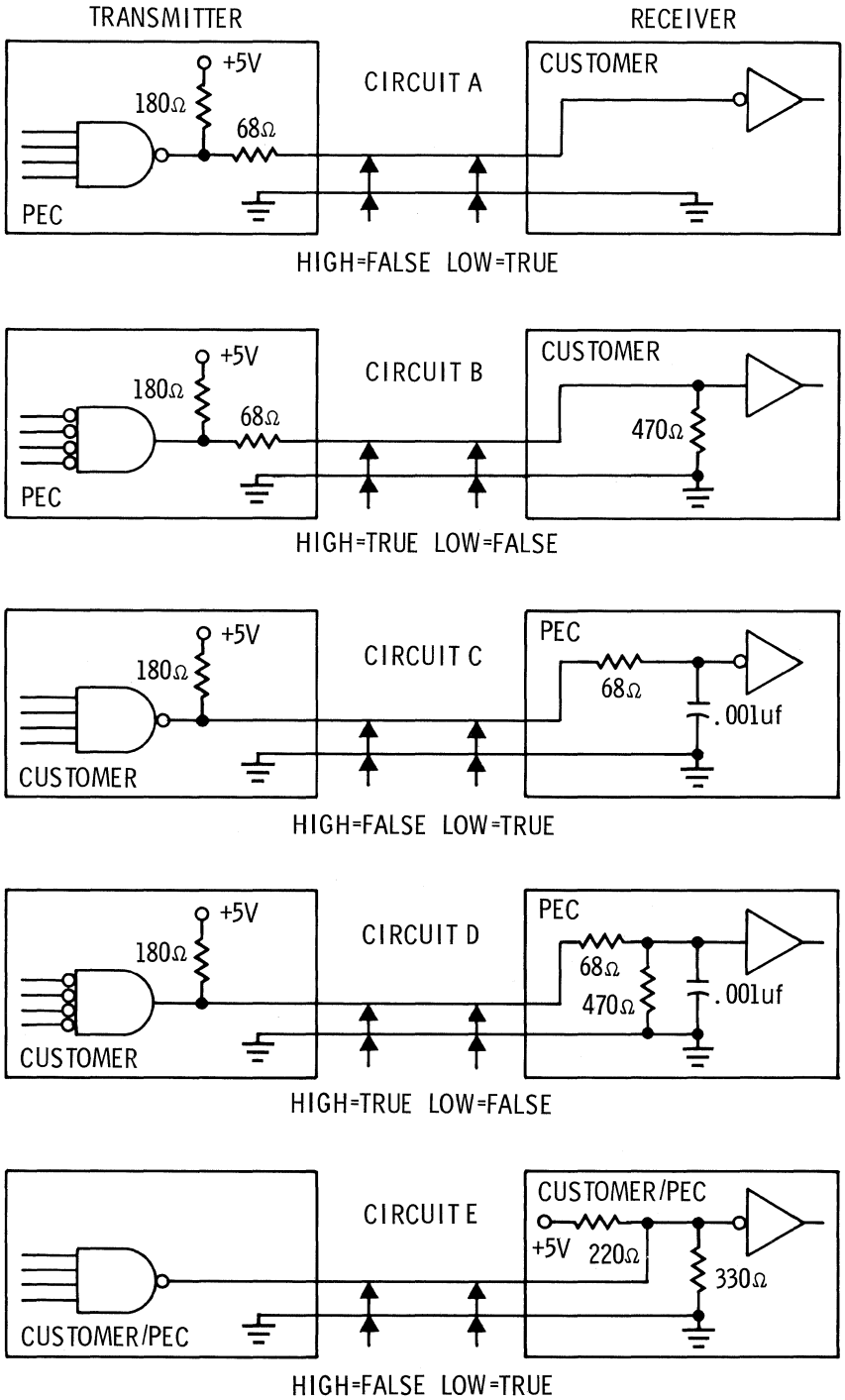

Figure 1-4. DTL Interface Circuit

Table 1-2

Noise Margins*

Circuit State	0°C	25°C	50°C
A&C low	500 mv	400 mv	200 mv
A&C high	2.0 v	2.1 v	2.25 v
B&D low	650 mv	550 mv	350 mv
B&D high	600 mv	700 mv	850 mv
E low	450 mv	250 mv	200 mv
E high	300 mv	450 mv	550 mv

*These margins are in excess of maximum crosstalk on a 20-foot long continuous cable without shielding.

1-9. DTL Interface Receivers and Transmitters

The design of the interface is based on the limited temperature range (0 to 75°C) series of Diode Transistor Logic (DTL) dual in-line modules. DTL 944 power gates are used as transmitters and DTL 936 inverters or DTL 946 dual-input gates are used as receivers. The system is also suitable for using equivalent Transistor Transistor Logic (TTL) modules.

The interface is designed so that all signal inputs can be included in one harness and all signal outputs can be included in a second harness. The maximum transmission distance is 20 feet. The two harnesses can be run in close proximity. The signals are transmitted via individual twisted pairs to reduce crosstalk.

The high edge speeds involved result in considerable distortion of the signal. Matching techniques must be employed to avoid spurious signals due to distortion. The interface circuits are designed so that a disconnected wire results in a false signal.

To give maximum flexibility, the interface transmitters and receivers used by PERIPHERAL EQUIPMENT CORPORATION transports incorporate the matching that is necessary to interface satisfactorily with unmatched transmitters and receivers in the customer's equipment.

SECTION II
INSTALLATION AND INITIAL CHECKOUT

2-1. INTRODUCTION

This section contains a summary of interface lines, information for uncrating the transport, as well as the procedure for electrically connecting and initially checking out the transport.

2-2. UNCRATING THE TRANSPORT

The transport is shipped in a protective container to minimize the possibility of damage during shipping.

Place the shipping container in the position indicated on the container.

Open the shipping container and remove the packing material so that the transport and its metal mounting frame can be lifted from the container.

Lift the transport out of the container using the metal shipping frame.

This metal shipping frame may be used during checkout of the transport if desired; however, it should be operated with the tape deck closed during checkout.

Check the contents of the shipping container against the packing slip and investigate for possible damage. If there is any damage, notify the carrier.

Open the tape deck and check that all cards are secured in their respective card slots. Also check for any visible mechanical damage.

CAUTION

THE TAPE DECK MAY BE OPENED, BUT PRECAUTION SHOULD BE TAKEN TO PREVENT THE TRANSPORT FROM TIPPING FORWARD AND POSSIBLY SUSTAINING DAMAGE.

The tape deck is opened by releasing the screw that secures it to the sheet metal electronic chassis. This may be accomplished by using a large flat-head screwdriver and turning the screw counterclockwise. This locking screw is located on the right-hand side of the transport under the dust cover door.

2-3. POWER CONNECTIONS

A power cord is supplied for plugging into a polarized 117-volt outlet. The power requirement is 120 watts, nominal, for the 3000 series and 250 watts for the 4000 series. Figure 2-1 shows the pin allotment for the power connector.

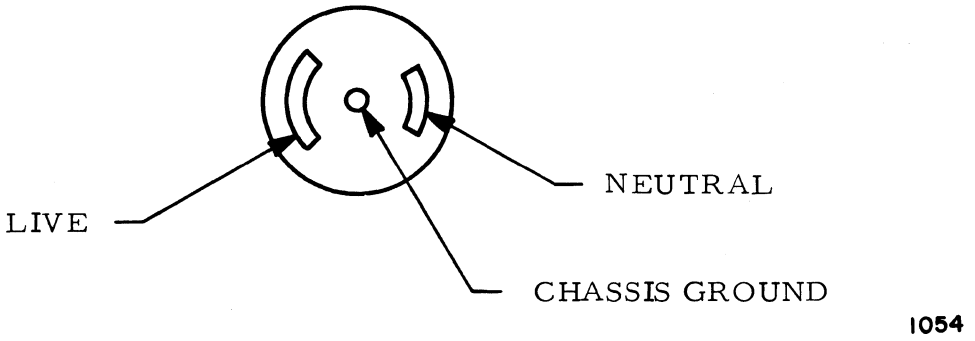

Figure 2-1. Power Connector

2-4. INTERFACE CONNECTIONS

Table 2-1 shows the Input/Output lines required. Details relating to the interface are contained in Section III.

2-5. INITIAL CHECKOUT PROCEDURE

Section III contains a detailed description of all controls. To check the proper operation of the transport before placing it in the system, follow the specified procedure.

(1) Connect the power cord.

(2) Place tape on the transport as described in Paragraph 3-29.

(3) Turn the transport power ON.

(4) Depress the LOAD FORWARD control momentarily to apply capstan-motor and reel-motor power.

Table 2-1

DTL Interface Signals

Transport Connector Mating Connector		Winchester MRAC 104S-J6 Winchester MRAC 104P-JTC6H
LIVE PIN	GROUND PIN	SIGNAL
A	E	→ LOAD FORWARD Command
K	P	→ READY Command
U	Y	→ REWIND Command
c	h	→ REMOTE RESET
m	r	→ DISABLE MANUAL CONTROLS
v	z	→ INTER-RECORD GAP Command
AD	AJ	→ FILE GAP Command
AY	BC	→ WRITE DATA STROBE
AX	BB	→ WRITE DATA 0
BF	BL	→ WRITE DATA 1
BR	BV	→ WRITE DATA 2
BZ	CD	→ WRITE DATA 3
CJ	CN	→ WRITE DATA 4
B	F	→ WRITE DATA 5
L	R	→ WRITE DATA 6 ┐ 9-track only
V	Z	→ WRITE DATA 7 ┘
d	i	→ WRITE DATA PARITY
n	s	→ ECHO CHECK RESET
D	J	← END OF TAPE Marker
N	T	← BEGINNING OF TAPE Marker
X	b	← TAPE NOT TENSIONED
g	k	← TRANSPORT READY
p	t	← DATA BUSY
AH	AM	← ECHO CHECK PARITY ERROR (optional)
w	AA	→ SYNCHRONOUS FORWARD Command
CP		← CHASSIS GROUND
CE		← 0 Volt Logic
CA		← +5 Volts ┐
BW		← -5 Volts ├ For monitoring only;
CR		← +10 Volts ├ not for customer use.
CL		← -10 Volts ┘
y	AC	← GAP IN PROCESS
AS	AW	← SPARE

(5) Depress the LOAD FORWARD control a second time and hold it in until tape reaches the BOT tab and stops. Then release the LOAD FORWARD control. The READY indicator will be illuminated.

(6) The transport is now ready to receive remote or local commands.

(7) FORWARD can be checked by depressing the control and checking that tape runs at the specified speed.

(8) Run several feet of tape onto the take-up reel by using the FORWARD control.

(9) Depress the REWIND control momentarily to initiate the rewind mode and illuminate the REWIND indicator. The tape will rewind to the BOT tab.

(10) When at BOT, depress the REWIND control and hold it down until all of the tape rewinds onto the supply reel. The reel is then removed as described in Paragraph 3-34.

2-6. RACK MOUNTING THE 3000 SERIES TRANSPORT

The physical dimensions of the transport are such that it may be mounted in a standard retma rack. A 12-1/4 inch panel space is required. It requires a depth behind the mounting surface of at least 12 inches.

To rack mount the transport, follow the specified procedure. (Figure 2-2 shows the relevant mounting dimensions.)

(1) Place the transport in the normal operating position with the reels facing the operator.

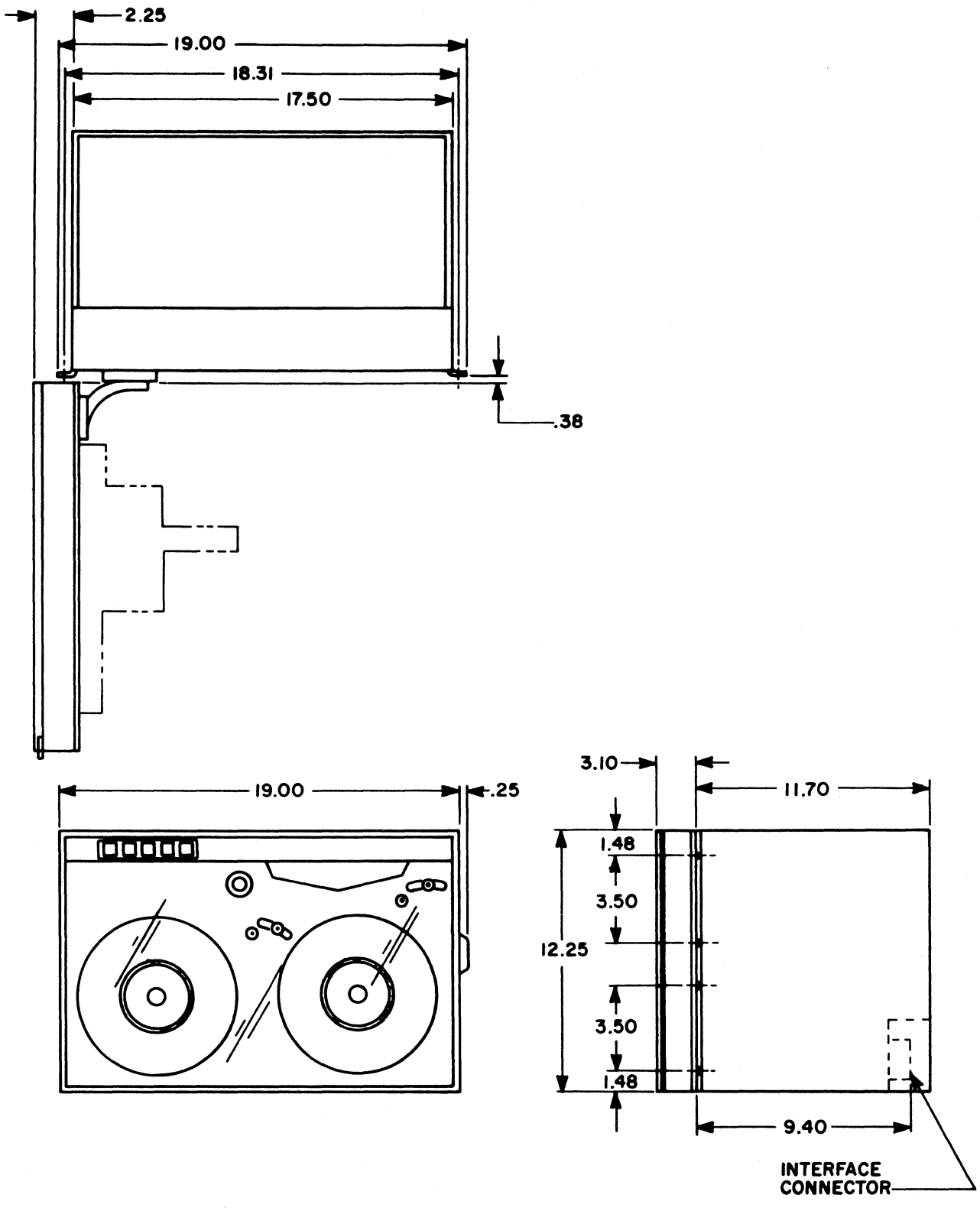

Figure 2-2. Mounting Dimensions (8-1/2 Inch Transport)

(2) Open the dust cover door and remove the capstan using the spline drive wrench supplied (note the position of the capstan for replacement). Unlock the tape deck as described in Paragraph 2-2. Close dust cover door.

(3) Open the tape deck, taking care that the transport does not tip forward.

(4) Remove the dust cover door and rim by removing 5 flat-head screws that are located at the perimeter on the back of the tape deck. Lift off the cover door and rim.

CAUTION

WHEN REMOVING TRIM FROM THE DECK, CARE MUST BE TAKEN TO AVOID CONTACT BETWEEN THE HEAD AND GUIDES AND THE OVERLAY PLATE.

(5) Close the tape deck and lock in place.

(6) Place the transport on its back so that the reels are facing up.

(7) Remove the screws that mount the transport to the metal shipping frame.

(8) Lift the transport out of the shipping frame and place it in the new cabinet.

(9) Line up the mounting holes of the transport and cabinet and bolt the transport to the cabinet.

NOTE

Transport mounting holes are for standard retma rack mounting.

(10) Open the tape deck and replace the dust cover door, rim, and capstan.

(11) Clean the tape deck as described in the maintenance procedure, Paragraph 6-38.

(12) Close the dust cover door.

2-7. RACK MOUNTING THE 4000 SERIES TRANSPORT

The physical dimensions of the transport are such that it may be mounted in a standard retma rack. A 24-1/2 inch panel space is required. It requires a depth behind the mounting surface of at least 12 inches.

To rack mount the transport, follow the specified procedure. (Figure 2-3 shows the relevant mounting dimensions.)

(1) Place the transport, still in its shipping frame, in the normal operating position with the reels facing the operator.

(2) Open the dust cover door and unlatch the tape deck by rotating the fastener.

(3) From the inside of the deck plate, disconnect the interchassis connector and the head cable connector bracket. Disconnect the deck retaining linkage.

(4) Remove the two hinge retainers located at the bottom of the hinge blocks. Lift the deck plate assembly until the painted arm of the hinge (attached to the deck plate) clears the hinge pins and the deck is free from the chassis.

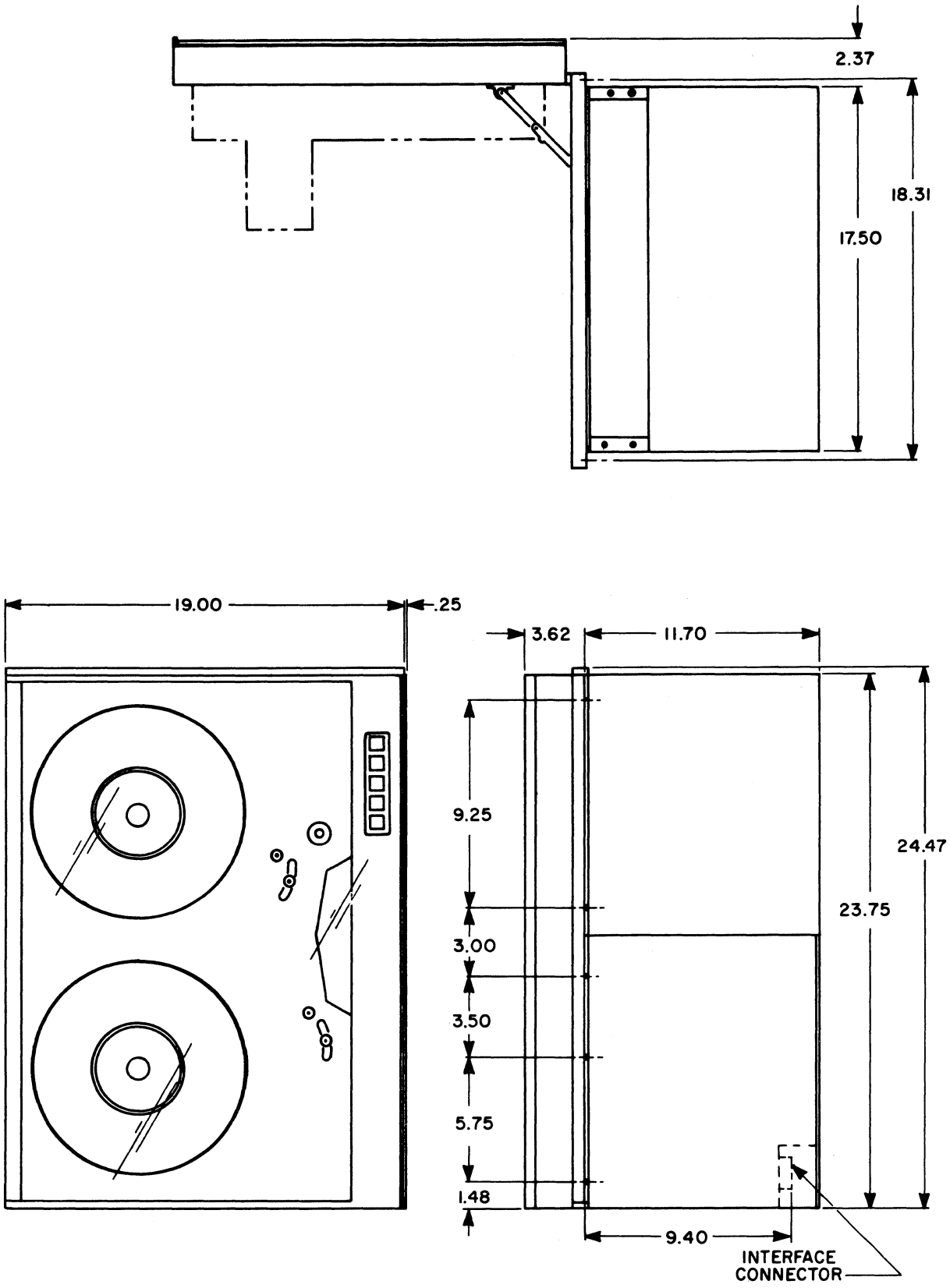

Figure 2-3. Mounting Dimensions (10-1/2 Inch Transport)

(5) Separate the electronic chassis from the hinge frame and the shipping supports.

(6) Mount the electronic chassis in the rack with four screws positioned opposite the relief holes in the hinge frame.

(7) Mount the hinge frame over the chassis utilizing the remaining mounting holes.

(8) Hang the deck on its hinges. Replace the hinge retainer, deck retaining linkage, the interchassis connector, and the head connector.

(9) Clean the tape deck as described in the maintenance procedure, Paragraph 6-38.

(10) Close dust cover door.

SECTION III
OPERATION

3-1. INTRODUCTION

This section contains information to manually operate the tape transport and specifications related to the interface input and output signal lines.

3-2. MANUAL CONTROLS

A power switch and four operational controls, are located on the front of the tape transport (see Figures 3-1 and 3-2). These controls are used to apply ac power to the transport, bring the tape to Beginning of Tape (BOT), rewind the tape to BOT and bring the transport to the Ready state.

3-3. POWER

The POWER control supplies ac power to the transformer. Both sides of the power line are switched. When power is turned on:

(1) All power supplies are established

(2) The ground returns of all the motors are open-circuited.

(3) A GENERAL RESET signal is applied to all the relevant control flip-flops.

3-4. LOAD FORWARD

The LOAD FORWARD control is a momentary switch. After power has been applied to the transport and tape has been loaded, momentarily depressing the LOAD FORWARD switch closes the interlock relay, applies ground returns to the capstan motor and reel

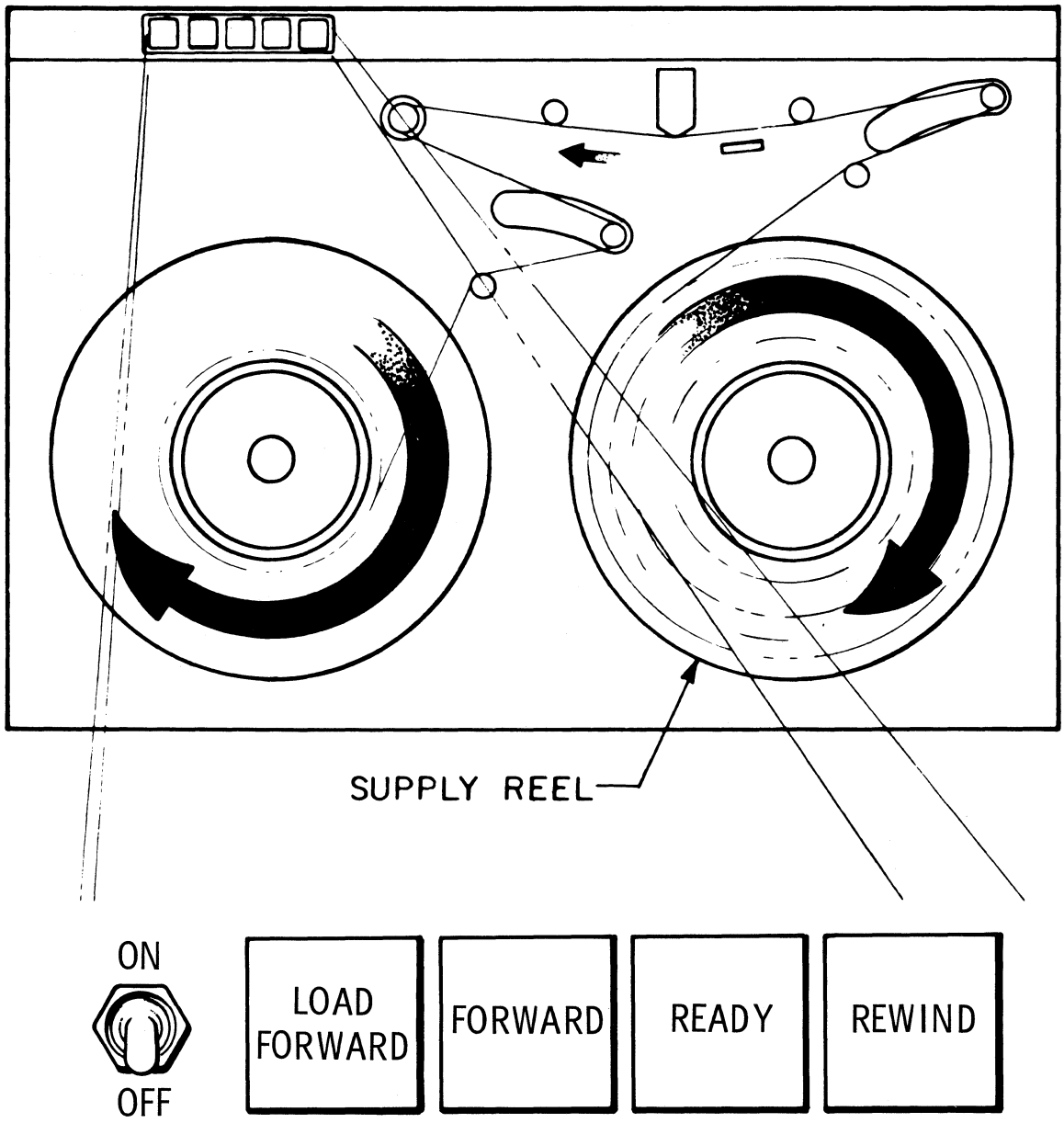

Figure 3-1. Tape Path and Controls (3000 Series)

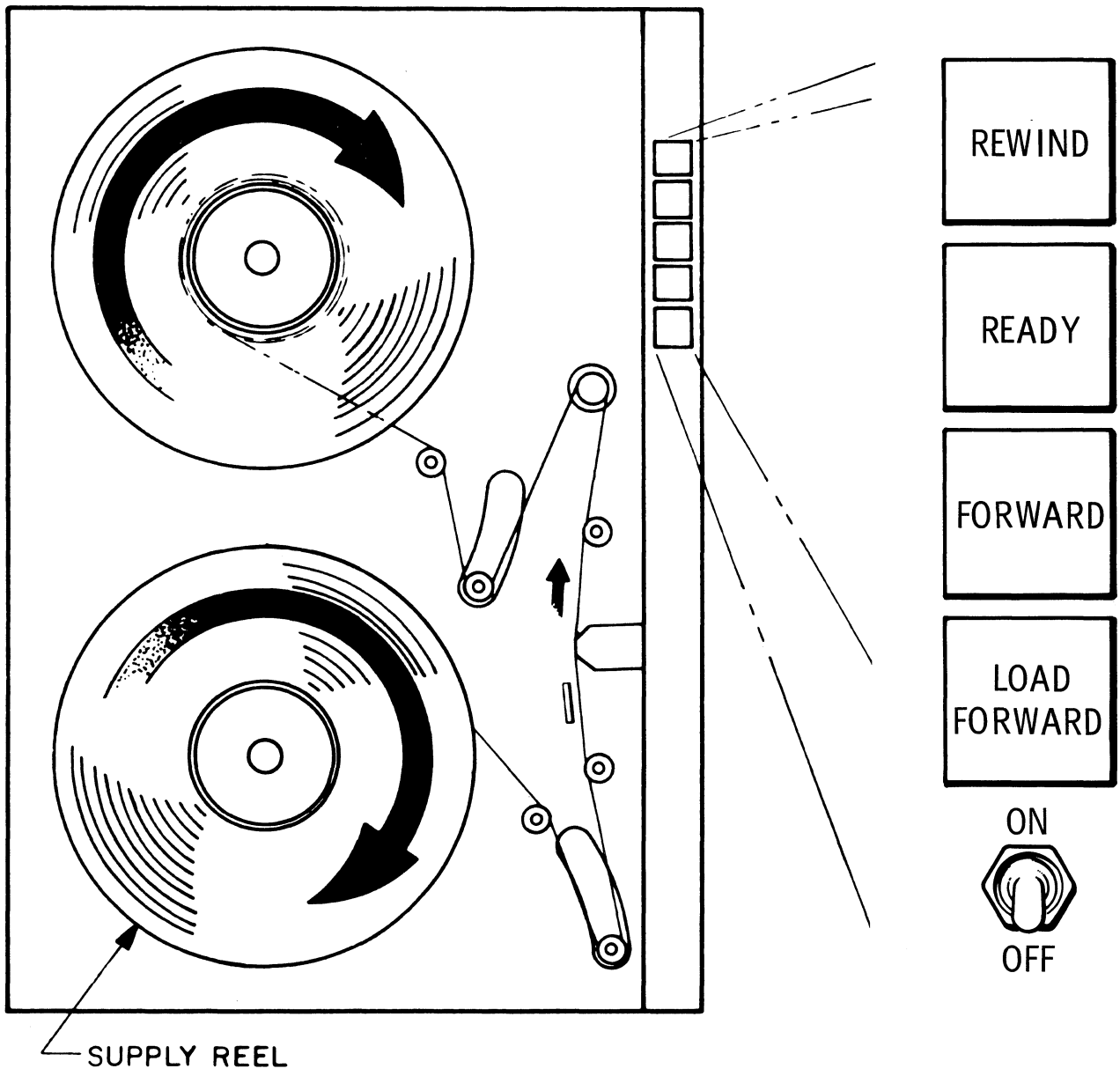

Figure 3-2. Tape Path and Controls (4000 Series)

motors, and removes the GENERAL RESET signal. When tape is loaded on a transport, but has not been tensioned, the limit switch on the take-up storage arm is still open; momentary depression of the LOAD FORWARD control bypasses the switch and allows the reel motors to bring the storage arms to their nominal operating position.

After the tape has been loaded and power has been applied to the capstan motor and reel motors, each reel servo will maintain its respective storage arm in the nominal operating position.

To bring the tape to BOT, the LOAD FORWARD control must again be depressed and held depressed until the BOT tab has passed the phototab detector. After the BOT tab has been detected, the tape will be brought to a controlled stop with the BOT tab displaced the proper distance from the magnetic head, even though the LOAD FORWARD control is still depressed. Detecting the BOT tab also places the transport in the READY condition and illuminates the READY indicator. When the tape has come to a stop, the LOAD FORWARD control may be released.

After the tape has been brought to BOT, when the LOAD FORWARD control is again depressed, the tape will move at the specified speed until the control is released.

3-5. FORWARD

The FORWARD control is a momentary switch which, when held depressed, enables tape to move forward at the normal synchronous forward speed.

3-6. READY

The READY control is a momentary switch that is illuminated when the transport is in the READY state. READY state indicates that the transport is ready to receive remote commands.

The transport can be placed in the READY state by any of the following procedures.

(1) Load the tape on the transport and bring the tape to BOT by using the LOAD FORWARD control.

(2) Apply power to the transport, momentarily depress the LOAD FORWARD control and then the READY control. This is useful when bringing the transport to READY without tape movement.

Remove the READY state by using one of the following.

(1) Turn power to OFF.

(2) Apply REMOTE RESET.

(3) Place the transport in the Rewind mode.

All of the manual controls except POWER may be inhibited remotely using the DISABLE MANUAL CONTROLS interface input.

3-7. REWIND

The REWIND control is a switch which, when momentarily depressed, causes the tape to move in reverse at a nominal speed of 75 ips. Upon reaching the BOT tab, the rewind operation ceases and the tape comes to a controlled stop. If already at Load Point when the REWIND control is depressed, tape will run in reverse at 75 ips until the control is released. The REWIND indicator is illuminated while the tape is rewinding.

3-8. INTERFACE INPUTS

3-9. SYNCHRONOUS FORWARD COMMAND

This is a level which, when true, causes tape to move forward at the specified speed. When the level goes false, tape motion ceases. The velocity profile is trapezoidal with nominally equal rise and fall times.

3-10. WRITE DATA STROBE

This is an input pulse for each character to be written. It is assumed that the data lines change before or coincident with the leading edge of the WRITE DATA STROBE pulse. The recording density is determined by the frequency of the pulse train. Frequency stability of the pulse train should be better than 0.25 percent. WRITE DATA STROBEs should be not less than 2 μseconds wide and the leading edge of a subsequent WRITE DATA STROBE must be separated from the trailing edge of the preceding WRITE DATA STROBE by a minimum duration of 20 μseconds. WRITE DATA STROBEs should never be issued if the transport is not ready.

3-11. REWIND COMMAND

This is a pulse which causes tape to move in reverse at a nominal speed of 75 ips. Upon detecting the

BOT tab, the rewind operation will cease and the tape will decelerate to a controlled stop. The velocity profile is trapezoidal with rise and fall times of less than 1.0 second.

3-12. REMOTE RESET

This is a level which, when true, resets all relevant flip-flops in the control logic. It must be true for a minimum of 2 milliseconds.

3-13. LOAD FORWARD COMMAND

This is a level which, when true, causes tape to move forward at the specified tape speed. When the BOT tab reaches the photosensor, the tape stops after completing the initial gap sequence. If the level is returned to the false state and then back to the true state, motion is again initiated. Tape motion stops when the LOAD FORWARD command becomes false.

3-14. READY COMMAND

This is a pulse which, if tape is tensioned, can be used to place the transport in the READY state and illuminate the READY indicator. READY state indicates that the transport is ready to receive remote commands. This line will normally be used when a BOT tab is not present on the tape and a LOAD FORWARD command is given.

3-15. DISABLE MANUAL CONTROLS

This is a level which, when true, causes the Manual Controls to be inoperative, except the power switch.

3-16. WRITE DATA PARITY

This is a level which, when true, will cause the writing of a bit in the parity channel, provided the selector switch on the Receiver

PCBA is in the external (X) position. With the switch in the "odd" (O) or "even" (E) positions, the selected parity is internally generated and the WRITE DATA PARITY interface line is ineffective. It must adhere to the timing requirements established for the WRITE DATA lines.

3-17. FILE GAP COMMAND

This is a pulse which, when true, will initiate the generation of a 3.8-inch gap where the File Mark character and its associated LRC character is written.

In a 7-track transport, the File Mark character and its associated LRC character consists of bits recorded on tape in data bit positions WD0, WD1, WD2, and WD3. In a 9-track transport, these characters are recorded on tape in data bit positions WD3, WD6, and WD7. In the 9-track transport, the CRC character is omitted in the File Mark.

The leading edge of the FILE GAP command can occur coincident with, or at any time after, the termination of the SYNCHRONOUS FORWARD command.

3-18. ECHO CHECK RESET (Optional)

This is a level which, when true, will reset the Echo Check Error flip-flop. Note that this flip-flop is also reset by internal logic at the end of each record.

3-19. WRITE DATA LINES (WD0 through WD5 or WD7)

A true level on a data line occurring coincident with the WRITE DATA STROBE line transition will cause a "one" bit to be recorded in its corresponding track. The level on the WRITE DATA line must be maintained for a duration of 10 μseconds after the leading edge transition of the WRITE DATA STROBE.

3-20. INTER-RECORD GAP COMMAND

Normally, the writing of check characters at the end of a record is initiated by the termination of the SYNCHRONOUS FORWARD command. If it is required to generate an Inter-Record gap (IRG) "on the fly" (i.e., at a constant tape speed), the SYNCHRONOUS FORWARD command remains enabled and a pulse on the IRG line initiates the check character generation. The IRG signal must be coincident with the leading edge of the last WRITE DATA STROBE for the record.

3-21. INTERFACE OUTPUTS

3-22. DATA BUSY

This is a signal which goes false at a specified time related to tape speed, after the receipt of a SYNCHRONOUS FORWARD command. The false condition of this signal is used by the controller to release WRITE DATA STROBEs to the transport.

3-23. GAP IN PROCESS

This is a level which, when true, indicates that a File Gap or initial BOT gap sequence is in process.

3-24. END OF TAPE (EOT)

This line is true when the EOT tab is being detected. Circuitry using this output should not assume that the transitions to and from the true state are clean.

3-25. ECHO CHECK ERROR (optional)

This is a line which, when true, indicates that an Echo Check Parity Error has been detected. This line remains true until receipt of an ECHO CHECK RESET command, or until reset by internal logic at the end of each record.

3-26. BEGINNING OF TAPE (BOT)

This line is true when the BOT tab is being detected. Circuitry using this output should not assume the transitions to and from the true state are clean.

3-27. TAPE NOT TENSIONED

This line is true when the tape storage arms are not in the nominal operating position.

3-28. TRANSPORT READY

This line is true when the tape transport is in a condition to receive remote commands.

3-29. LOADING TAPE ON TRANSPORT

The 3000 Series transport, in the position shown in Figure 3-1, has the take-up reel on the left side (facing the transport) and is located below the manual controls. The supply reel (reel to be recorded) is located on the right-hand side.

The 4000 Series transport, in the position shown in Figure 3-2, has the take-up reel on the top (facing the transport) and is located below.

CAUTION

BE SURE THE SUPPLY REEL IS SUCH THAT TAPE WILL UNWIND FROM THE REEL WHEN THE REEL IS TURNED CLOCKWISE WHILE FACING THE TRANSPORT. THIS IS SHOWN IN FIGURE 3-1.

3-30. REEL LOADING

To load the supply reel, position the reel over the reel retainer hub and then depress the center plunger. This will allow the reel to slip over the rubber ring on the reel retainer. Press the reel evenly and firmly against the back of the reel retainer hub while the center plunger is depressed. While holding the reel in this position, release the center plunger. The reel is now properly aligned in the tape path and ready for tape threading.

3-31. TAPE THREADING

Thread the tape through the transport as shown in Figure 3-1. Wrap the tape leader on the take-up reel so that the tape will be wound on the reel when the reel is rotated clockwise. Wind several turns on the take-up reel and then turn the supply reel counterclockwise until the slack tape has been taken up.

CAUTION

IF SLACK IS LEFT IN THE TAPE, TAPE DAMAGE MAY RESULT WHEN POWER IS APPLIED.

AFTER THE TAPE HAS BEEN MANUALLY TENSIONED, CHECK TO BE SURE THE TAPE IS PROPERLY LOCATED ON ALL GUIDES OR TAPE DAMAGE MAY RESULT.

CLOSE THE DUST COVER DOOR AND KEEP IT CLOSED EXCEPT WHEN CHANGING TAPE REELS. DATA RELIABILITY DUE TO TAPE CONTAMINATION WILL BE IMPAIRED IF THE DOOR IS LEFT OPEN.

3-32. BRING TAPE TO BOT

After the tape has been loaded on the transport, the following steps will bring the tape to BOT.

(1) Turn the power on with the power switch on the Manual Control Panel.

(2) Momentarily depress the LOAD FORWARD control. This will apply power to the capstan motor and reel motors and allows the reel servos to operate, bringing the tape storage arms to the nominal operating position.

CAUTION

CHECK TO SEE THAT THE TAPE IS POSITIONED PROPERLY ON ALL GUIDES OR TAPE DAMAGE MAY RESULT.

(3) Depress the LOAD FORWARD control and hold depressed. This will move the tape forward at the specified velocity. When the BOT tab is detected, the tape will come to a controlled stop with an IBM-compatible displacement between the tab and the record head.

The LOAD FORWARD control may now be released.

When the above sequence has been followed, the READY indicator will be illuminated when the BOT tab is detected.

The transport is now ready to receive remote commands.

CAUTION

CLOSE THE DUST COVER DOOR AND KEEP IT CLOSED EXCEPT WHEN EXCHANGING TAPE REELS. DATA RELIABILITY WILL BE IMPAIRED DUE TO TAPE CONTAMINATION IF THE DOOR IS LEFT OPEN.

3-33. BRING TAPE TO THE READY STATE

If the power is turned off, complete the following procedure to bring the transport to the Ready State.

(1) Turn power on with the POWER control.

(2) Momentarily depress the LOAD FORWARD control.

(3) Depress the READY control.

The transport is now in a Ready State.

3-34. UNLOADING THE TAPE

To unload a tape, complete the following procedure if the power has been switched off (if power has not been switched off and the READY indicator is illuminated, start the procedure at Step (3)).

(1) Turn the transport power on.

(2) Momentarily depress the LOAD FORWARD control to apply capstan-motor and reel-motor power.

(3) Momentarily depress the REWIND control. When the tape has rewound to BOT, the tape will come to a controlled stop.

NOTE

When rewind has been initiated, the tape cannot be stopped until it reaches BOT (unless transport power is turned off). After detecting BOT, the last few feet of tape can be unwound by using the REWIND control. When the REWIND control is released, the tape will stop. Depress the REWIND control and allow the tape leader to wind onto the supply reel. When the tape leader has emptied from the take-up reel, tape tension will be lost which allows the tension arms to move to the unload position. When the storage arms move to this position, an interlock switch is activated which removes power from the capstan motor and reel motors.

(4) Open the dust cover door, depress the reel hub retainer plunger and remove the supply reel. Close the dust cover door.

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION

This section provides a general theory of operation of the Synchronous Write Tape Transport.

4-2. GENERAL THEORY

The transport consists of the mechanical and electronic components necessary to record data on magnetic tape which can be reproduced on an IBM digital tape transport or its equivalent. The systems that comprise the transport are:

(1) Power supplies

(2) Capstan drive system

(3) Tape storage systems and associated reel servos

(4) Magnetic recording head and associated tape guides

(5) General reset logic

(6) Data recording electronics

(7) Control logic required to bring the transport to operational status and the logic necessary to allow forward and rewind operations.

4-3. POWER SUPPLIES

Figure 4-1 is a block diagram of the power supplies. The ac power lines, both live and neutral, are controlled by the power switch. A series 20-ohm resistor in the neutral line limits the surge of current into the power supply capacitors. This resistor is shorted when the interlock relay contacts are closed. Unregulated dc (at a nominal ±16

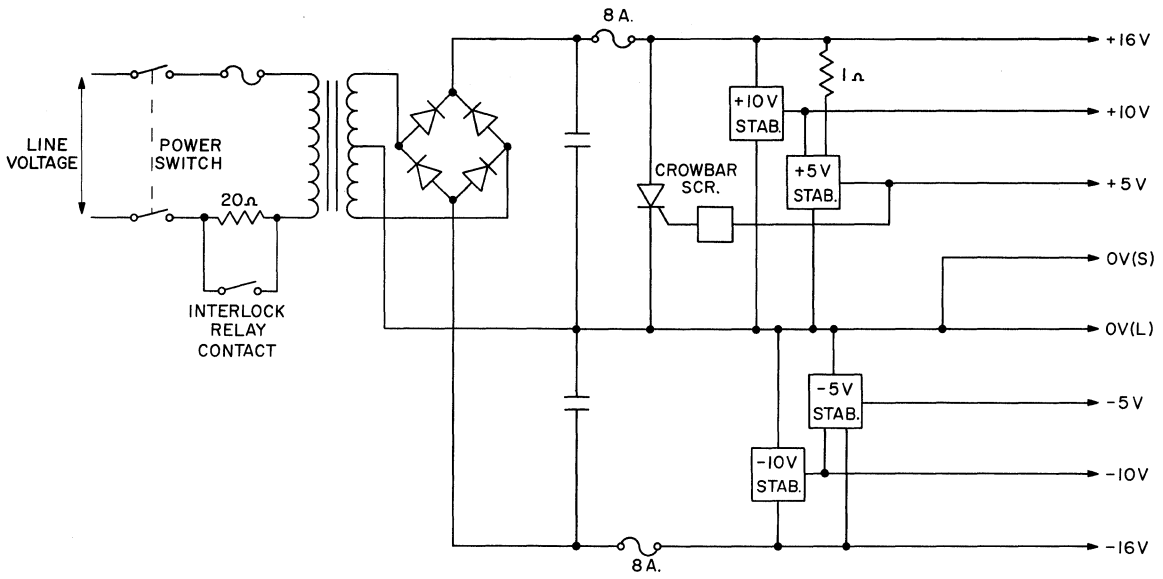

Figure 4-1. Block Diagram of Power Supplies

volts) is used to drive the motors and the regulated supplies. Four regulated supplies are generated. The +10- and -10-volt lines are regulated to ±7 percent and can supply 300 milliamps each. The reference diodes in the +5- and -5-volt regulators are driven from their respective 10-volt line. The 5-volt lines are adjusted and regulated to within ±1 percent and can supply 3.0 amps. (Note that certain of these voltages are brought out to the interface connector; however, this is for monitoring only. These voltages should not be utilized by the customer.)

Since DTL integrated circuits are widely used, it is necessary to employ a silicon controlled rectifier (SCR) for "crowbar" protection against over-voltages on the +5-volt line. The circuits used can withstand up to 12 volts for 1 second. When the +5-volt line rises above 8 volts, the SCR connected between the +16 volts and 0 volt is turned on.

This holds the voltage across the integrated circuits down until the fuse opens (a few milliseconds later). A separate 0-volt line is used for the high-current servo circuitry and is called 0V(S) (S represents servo). The logic circuitry 0-volt line is called 0V(L) (L represents logic). They are connected together at the power-distribution terminal block (TB201).

4-4. CAPSTAN DRIVE SYSTEM

Figure 4-2 is a block diagram of the capstan drive. The capstan drive mechanism is a direct-coupled system that consists of a dc motor, capstan, and dc tachometer. The dc tachometer indicates the angular velocity of the capstan.

The motor and tachometer are used in a conventional velocity servo that is controlled by the output of one of two ramp generators, depending upon the mode of operation (forward or rewind). Resistors R1 and R2 determine the output of the ramp generators which, in conjunction with the dc tachometer via R3, controls the capstan speed. When the transport is in the standby condition, none of the ramp generators is enabled. In this case, the capstan position is maintained by the motor friction.

Tape is held on the capstan by friction and is in contact with the capstan through an angle of 180 degrees. A tape tension of approximately 8 ounces assures no possibility of slippage.

4-5. Record Mode

The receipt of a SYNCHRONOUS FORWARD command enables the Forward 1 ramp generator and the tape is accelerated to a prescribed velocity, depending on the speed selected by the customer. This velocity is maintained until the ramp generator is disabled and the tape is decelerated. Figure 4-3 shows the relevant waveforms.

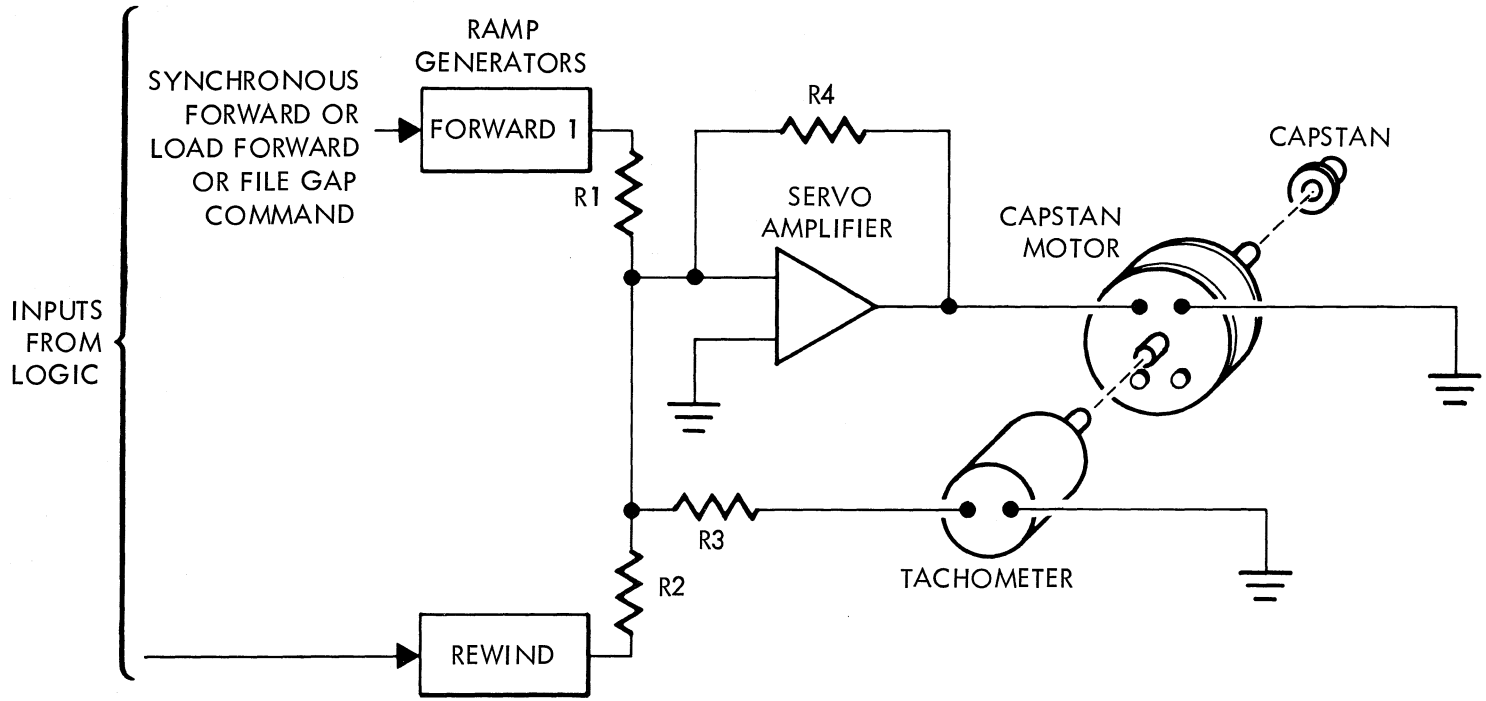

Figure 4-2. Capstan Drive Block Diagram

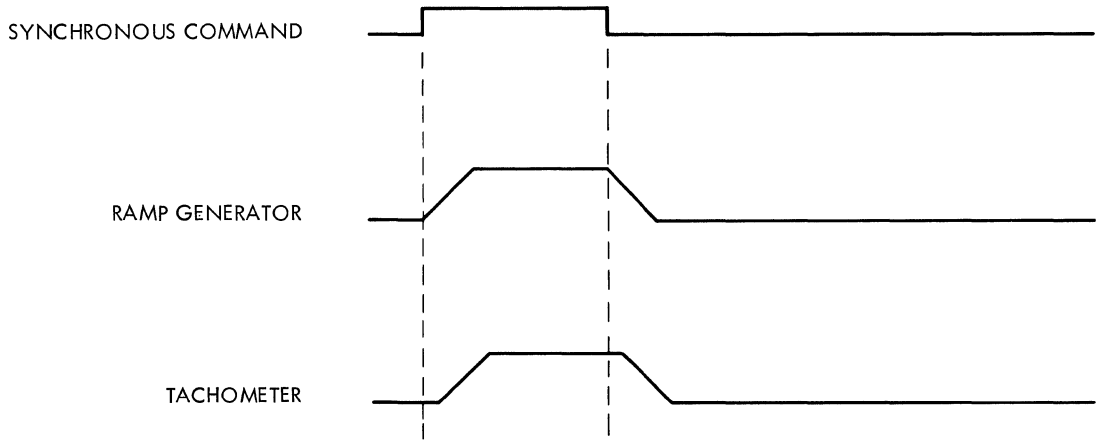

Figure 4-3. Capstan Drive Waveforms

The Forward 1 ramp generator is activated by the SYNCHRONOUS FORWARD or FILE GAP commands, or the FORWARD or LOAD FORWARD controls. This ramp generator is designed to allow the tape velocity to reach the specified value before a distance equal to one-half of an IBM IRG distance has been traversed. In Figure 4-3 a typical forward, stop sequence is shown. Also shown are the ramps and the tachometer output that are directly related to the actual tape movement. Note that this tachometer output is delayed slightly behind the Ramp Generator waveform. This is inherent in this type of direct-drive capstan servo system because of the system bandwidth.

4-6. Rewind Mode

The Rewind ramp generator rises and falls in less than 1.0 second to generate a high-speed reverse velocity. The long rise and fall times of the Rewind ramp generator are required to prevent the tape storage arms from moving outside their operating region during tape acceleration and deceleration.

Tape speed is controlled in the Rewind mode by the capstan. The tape is in contact with the capstan through an angle of 180 degrees and the tape tension of 8 ounces assures proper packing of the tape on the supply reel.

4-7. REEL SERVO SYSTEM

Figure 4-4 is a diagram of a reel servo. Identical linear position servos control the supply and takeup of tape by the reels. The storage arms isolate the inertia of the reels from the capstan. Low-friction ball-bearing guides are used to minimize tape tension variations. The position of the storage arm is sensed by a long-life potentiometer. The potentiometer output, after amplification, drives the reel motor in the direction to center the arm. The geometry of the storage arm and spring ensure that only negligible changes in tape tension occur as the storage arm moves through its approximately 30-degree arc.

With the tape stationary, the storage arms take up a position such that the amplified potentiometer output, when applied to the reel motor, produces enough torque to balance the spring torque. Initially, the potentiometers have been set by rotating the body of the potentiometers so that the tension arms operate in the center of their range. The position of the storage arm changes slightly for different steady-state capstan velocities. This occurs because the amplifier output varies with the back-emf of the motor, requiring corresponding input voltages from the potentiometer.

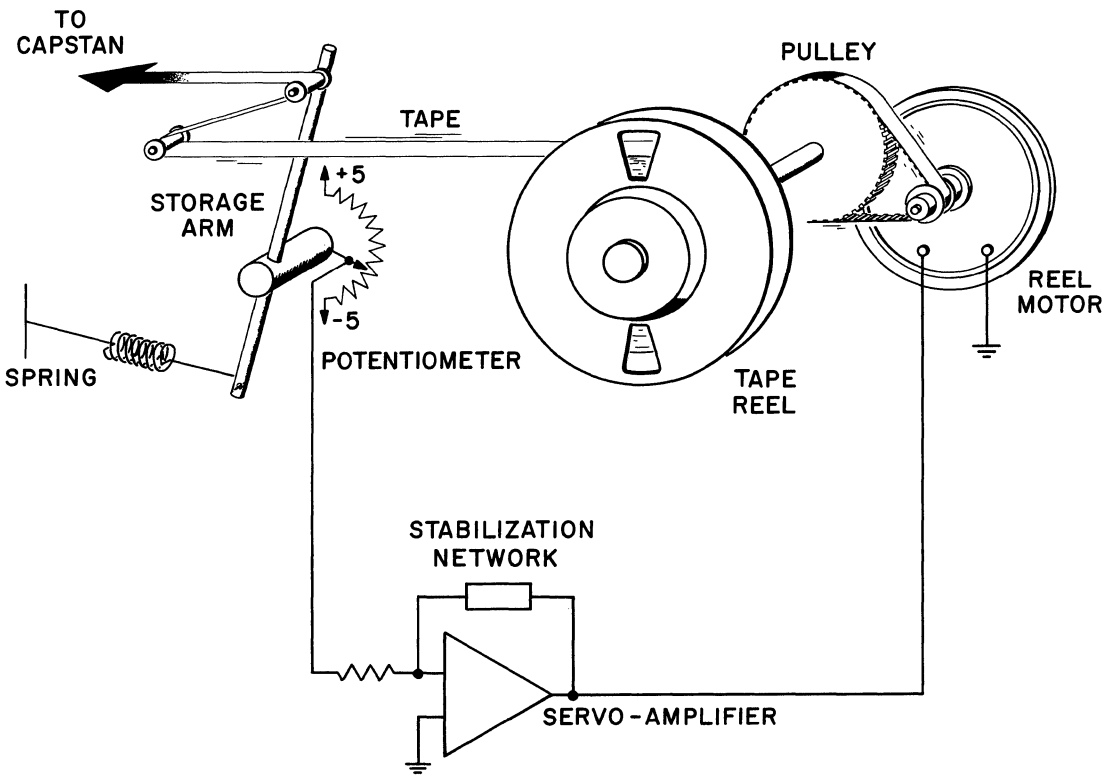

Figure 4-4. Reel Servo Diagram

When the capstan applies a tape velocity transient in either direction, the arm moves and the potentiometer output changes, driving the reel motor in the direction to recenter the arm.

Without tape, the arms rest against the stops and the tension-arm limit switch is open, causing the interlock relay to be de-energized, removing power to all motors.

Each reel motor is driven by a linear amplifier with transitional lead servo stabilization. The low frequency gain of the amplifier is 11 volts per volt. The zero of the stabilization network is at 1.5 Hz, and the pole is 15 Hz.

When the transport operates in the Rewind mode, the gain of the amplifier is approximately doubled to accommodate the higher velocity.

4-8. BRINGING THE TRANSPORT TO OPERATIONAL STATUS

Operation is best understood by considering the sequence required to achieve operational status. Figure 4-5 is a basic logic diagram illustrating the necessary components and interconnections. When the tape transport is located some distance from the associated equipment, it is desirable (after bringing the machine to operational status) to ensure that the manual controls cannot be inadvertently operated. When the DISABLE MANUAL CONTROLS signal (which is generated externally) is true, operation of any of the manual controls (except the power switch) cannot generate the signal required to set the associated flip-flops.

4-9. Switch Power Control

This applies ac power to the power supply via the 20-ohm resistor. The value of this resistor is chosen to limit the input surge caused by the capacitor-input filter network, but it is not sufficient to disturb the regulation of the stabilized power supplies. The following conditions now exist.

(1) All power supplies are established; i.e., ±16, ±10, and ±5 volts.

(2) The interlock relay is de-energized and contacts KA, KB, KC, KD, and KE are open.

(3) The return lines for the two reel motors and the capstan motor are open-circuited via contacts KC, KD, and KE.

(4) A GENERAL RESET signal is applied to all relevant flip-flops (it can also be initiated externally).

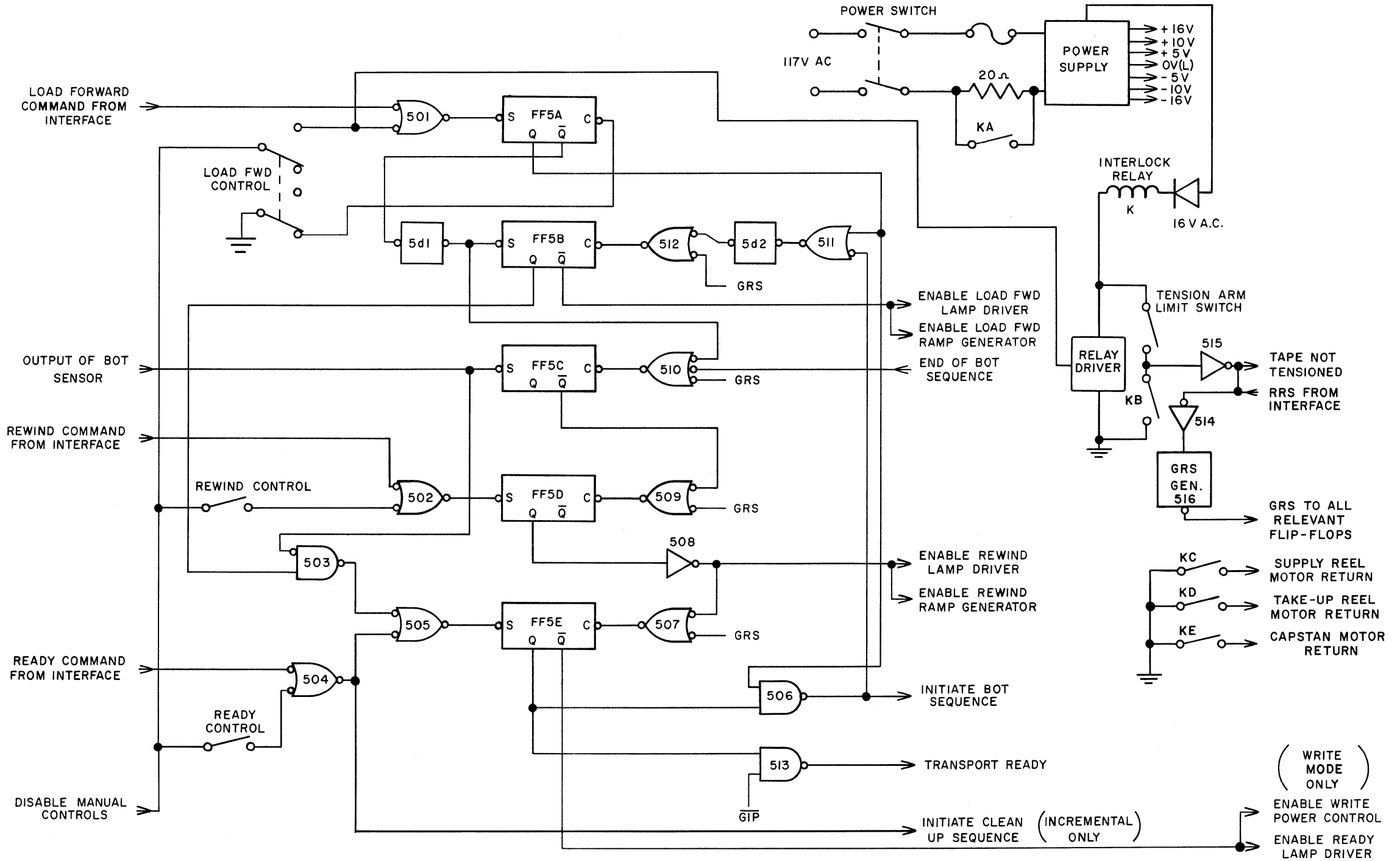

Figure 4-5. Control Logic to Bring Transport to Operational Status

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(5) The TRANSPORT READY line is false.

(6) The TAPE NOT TENSIONED line is true.

Tape can be loaded and threaded while in this condition, since power is not applied to the motors.

4-10. Press LOAD FORWARD Control (First Time)

This bypasses the tension-arm limit switch and relay-latching contact KB, energizing the interlock relay. Provided that the tape is correctly loaded, power is now applied to the reel motors. The motors move the reels in a direction to establish tape tension. The tension arms move into their operational region and the tension-arm limit switch closes, allowing the interlock relay to latch. The LOAD FORWARD control may now be released. At this time the GENERAL RESET signal is removed and the TAPE NOT TENSIONED signal becomes false.

If at any time the tension arms move outside their operating region, the interlock relay de-energizes, power is disconnected from the motors, and the GENERAL RESET signal is applied. The tension-arm limit switch opens at both extremes of the arm travel. This provides protection against over-tension as well as under-tension conditions.

4-11. Press LOAD FORWARD Control (Second Time)

If the LOAD FORWARD control is depressed and held, the following sequence occurs.

(1) Flip-flop 5A is set via OR gate 501 and the $\overline{Q}$ output is differentiated by 5d1. The output pulse sets flip-flop 5B. Flip-flop 5A is used in conjunction with the LOAD FORWARD switch to eliminate the effects of contact bounce.

(2) The $\overline{Q}$ output of flip-flop 5B enables the Load Forward lamp driver and the Load Forward (Forward 1) ramp generator, causing the tape to accelerate to the specified speed. One input of AND gate 503 is enabled by the Q output of flip-flop 5B.

(3) Tape motion will continue as long as the LOAD FORWARD switch is held depressed, until the BOT tab reaches the BOT sensor, at which time the second input of AND gate 503 is enabled.

(4) The output of AND gate 503 sets flip-flop 5E via OR gate 505.

(5) Since the LOAD FORWARD control is still depressed, the BOT sequence is initiated via AND gate 506 and flip-flop 5B is reset via OR gates 511 and 512, disabling the Forward 1 ramp generator and lamp driver.

(6) Prior to the time that the BOT is initiated, the magnetic head is adjacent to the tape just forward of the BOT tab. The tape advances so that the trailing edge of the BOT marker is less than 0.5 inch forward of the head gap which establishes IBM compatibility.

(7) While the BOT sequence is in process, the NOT GAP IN PROCESS signal will be false. When flip-flop 5E is set, one input to AND gate 513 is true. After completion of the BOT sequence, the NOT GAP IN PROCESS signal is true and enables AND gate 513 which indicates TRANSPORT READY. Since the TRANSPORT READY signal is true, the transport is now ready to receive remote commands.

If at any time before the BOT tab arrives the LOAD FORWARD control is released, flip-flop 5A resets flip-flop 5B via OR gate 511, differentiator 5d2 and OR gate 512. When flip-flop 5B is reset, the Load Forward (Forward 1) ramp generator is disabled. Depressing the LOAD FORWARD control again will restart tape motion.

4-12. Special Case When a BOT Tab is Not Attached

Sometimes a BOT tab is not attached to the tape. It is then possible to bring the transport to operational status by the following sequence.

(1) After the operations described in Paragraphs 4-9 and 4-10 are performed, tape motion will be initiated as described in the first two steps of Paragraph 4-11.

(2) The READY control is depressed, flip-flop 5E is set via OR gates 504 and 505 and results in the conditions described in Steps (5) through (7) of Paragraph 4-11.

In essence, depressing the READY control simulates the occurrence of the BOT tab.

4-13. Special Case When Operational Status is Required Without Tape Motion

Provision has been made to cover the situation described in the following paragraphs.

After recording data, it may be required to turn power off and, at a later time, turn power on and re-establish operational status without tape motion.

It is noted that due to the possibility of tape motion during off/on switching, a spike may be written onto the tape. Therefore, with this type of operation, data errors may occur in the off/on switching sequence.

Operational status is re-established by the following procedure.

(1) When the power control is on and the LOAD FORWARD control is momentarily depressed, tape tension is established and the GENERAL RESET signal is removed from all flip-flops.

(2) Depressing the READY control sets flip-flop 5E via OR gates 504 and 505, enabling the Ready lamp driver. However, since the LOAD FORWARD control is not depressed, AND gate 506 is not enabled and the BOT sequence is omitted.

4-14. REWINDING TAPE

The necessary logic and interconnections are shown in Figure 4-5.

4-15. Press REWIND Control

When the REWIND control is momentarily depressed, the following sequence occurs.

(1) Flip-flop 5D is set via OR gate 502.

(2) The Rewind ramp generator is enabled and the tape accelerates to the rewind speed.

(3) Flip-flop 5E is reset, disabling WRITE POWER CONTROL and the Ready lamp driver. The TRANSPORT READY signal becomes false.

Once initiated in this manner, rewind cannot be stopped until a BOT tab is detected, power is switched off, or a REMOTE RESET signal is applied via the interface.

When the BOT tab is detected, flip-flop 5C is set and flip-flop 5D is reset. The Rewind ramp generator is disabled and the tape comes to a halt. Since flip-flop 5B is not set, AND gate 503 is not enabled. The output of inverter 508 is used instead of the $\overline{Q}$ output of flip-flop 5D because the permanent clear input clamps $\overline{Q}$ and only Q can respond to the set signal from OR gate 502.

Since flip-flop 5C is set, the Rewind flip-flop 5D has a permanent clear input and further rewind operation is now under the control of the REWIND control. Thus, if the control is depressed, tape moves in reverse until it is released. This mode of operation assists in unloading tape from the take-up reel.

Flip-flop 5C is reset when the LOAD FORWARD control is depressed via flip-flop 5A, differentiator 5d1, and OR gate 510. The other input to OR gate 510 is used to reset flip-flop 5C after the BOT tab has been detected when bringing the transport to operational status (as described in Paragraph 4-8).

4-16. GENERAL RESET GENERATION

Because of the complexity of the GENERAL RESET wiring, the generation of this signal and its path through the system is discussed. Figure 4-5 in conjunction with Table 4-1 will assist in understanding the system.

Table 4-1
Cross Reference Chart

Component (Shown in Figure 4-5)	Circuit Location		
	Input Pin	Circuit Board	Output Pin
Inverter 515		Function Control J203	17
Inverter 514	Y	Receiver, DTL Interface J205	25
General Reset Signal Generator 516	L	Capstan Drive J202	M

On examination of Figure 4-5, note that a GENERAL RESET signal can be generated by either one of two methods: when the interlock relay is open or by a REMOTE RESET signal from the customer via the interface.

Since the input of inverter 515 is floating when the interlock relay is open, the output of inverter 515 is low, providing a true TAPE NOT TENSIONED signal. The output of inverter 515 is also fed to inverter 514 whose output becomes high and in turn is fed to GENERAL RESET signal generator 516. The output of generator 516 being low provides a GENERAL RESET signal to all relevant flip-flops in the system. Actually the output of the generator 516 is at -0.7 volt; however, this voltage is compensated for by the diodes at the GENERAL RESET signal inputs of each flip-flop.

When the customer initiates a REMOTE RESET signal, the signal (which is collector OR'd to the TAPE NOT TENSIONED signal at Receiver circuit board J205) is true at the input of inverter 514. The GENERAL RESET signal is then generated as explained in the previous paragraph.

4-17. RECORDING INFORMATION

4-18. Digit Representation

Information is recorded in the NRZI mode; (i.e., a "1" on the information line causes a change of direction of magnetization between positive and negative saturation levels). Two tape formats are in general use. They are the IBM 727/729 7-track format which can operate at 200, 556 and 800 bpi, and the IBM 2400 9-track format which operates at 800 bpi only. Figure 4-6 illustrates the relevant 7- and 9-track allocations and spacing. In the 9-track system consecutive data channels are not allocated to consecutive tracks. This organization

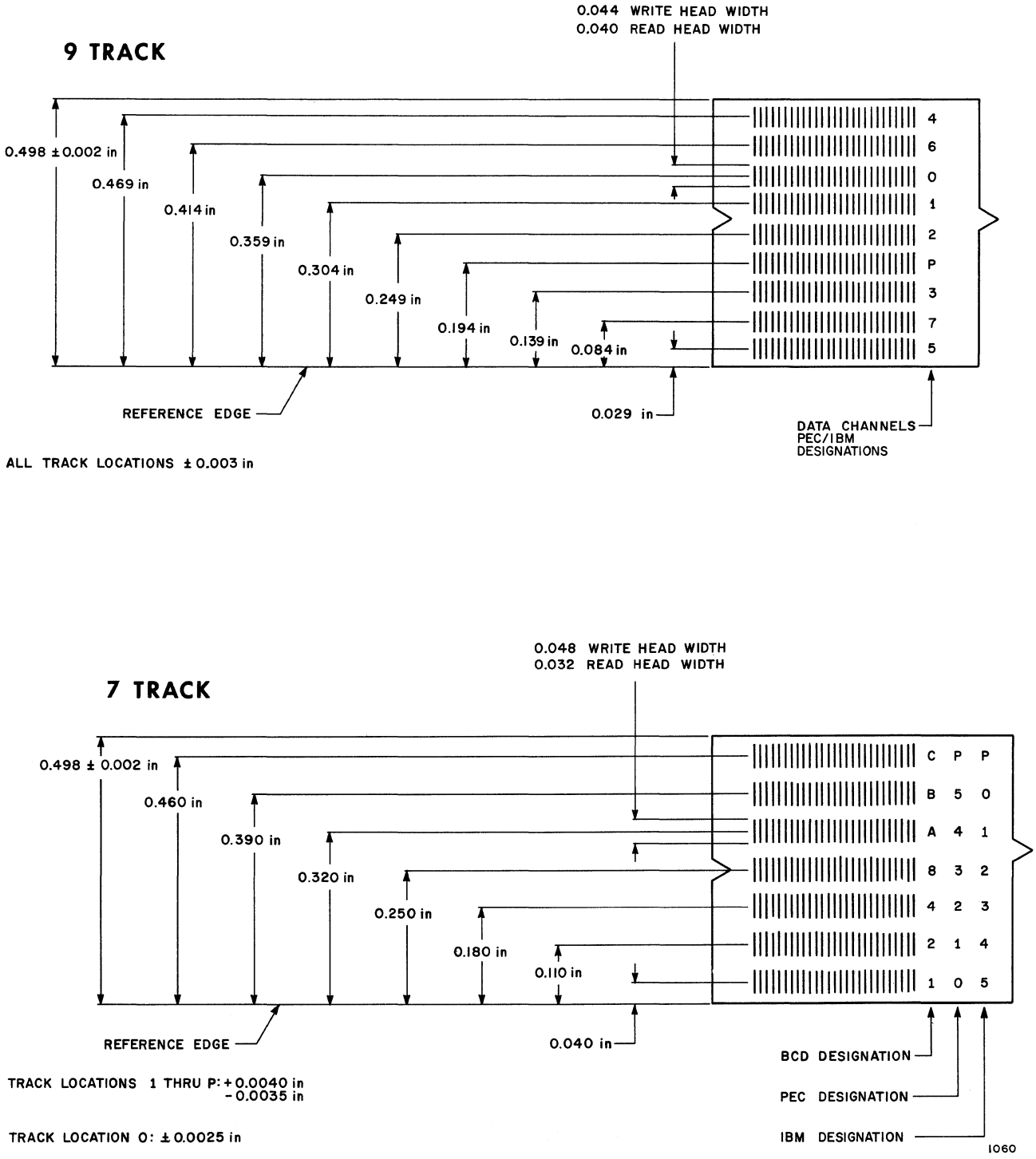

Figure 4-6. Allocation and Spacing for 9- and 7-Track Tape

increases tape system reliability since the most used data channels are located near the center of the tape; consequently, they are least subject to errors caused by contamination of the tape.

Figure 4-7 shows typical waveforms which occurred during a write operation and, for reference, the associated readback waveforms which can be obtained by reading at a constant speed. It is shown that the the magnetization transitions recorded on the tape are not perfectly sharp. This is due to the limited resolution of the magnetic reproducing process.

During reading, the amplified readback voltage is full-wave rectified (since no significance is attributable to the sign of the read-back voltage) and clipped to remove base line noise. This is necessary because there is no read signal output for a recorded zero. The output of the rectifier is peak sensed and a pulse generated for each "1" recorded.

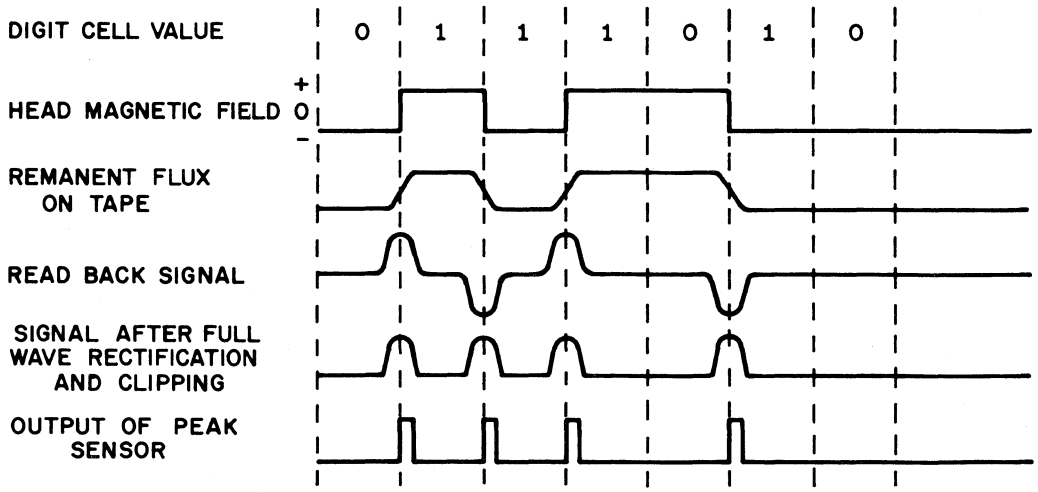

Figure 4-7. Write and Read Waveforms

4-19. Data Recording

Figure 4-8 shows a logic diagram of one channel of data electronics together with the necessary control.

Included in the transport is a parity generation circuit (not shown in Figure 4-8) which can generate odd or even parity, depending on the setting of a switch and a special circuit to provide Binary Zero to BCD10 conversion. This may be required because zero in some systems is represented by all "zeros" on the data lines. If BCD recording with even parity is being used, an invalid character will result. Therefore, the special circuit is arranged to detect the all-zero input condition and force the "1" and "3" channels to a "1" state so that BCD10 is recorded. The circuits are detailed in Section V. This system is capable of accepting and recording data at a rate between 300 and 20,000 characters per second.

Flip-flops 8A and 8B (see Figure 4-8) comprise the two-stage input buffer and flip-flop 8C is the Write current generator. This generator, in conjunction with the center-tapped head, maintains the magnetization on the tape in the appropriate direction between change-overs as required by the NRZI format. In a 7-track system, data bit N is routed directly to gate 806. In a 9-track system, data bit N is routed to the CRC generator. During data recording, gate 802 is enabled and the data bit transferred to gate 806 via AND gate 802 and OR gate 804. It is also used to generate the CRCC.

During a Gapping sequence, gate 802 is disabled and gate 803 is enabled so that CRCC bit N is transferred to gate 806. The lines marked PRIME for LRCC and PRIME for FM are also required by the Gapping sequence. Details of this Gapping sequence are discussed in Paragraphs 4-27 through 4-32. Flip-flops 8D and 8E together with gate 811 and the 4-μsecond delay comprise the control loop.

Operation of the system can be understood by considering what happens during a recording operation. It is assumed that the transport has been brought to operational status so that WRITE POWER CONTROL is enabled and current is flowing in the heads. Initially, all flip-flops are reset so that their outputs are false. On receipt of a SYNCHRONOUS FORWARD command, the transport accelerates under the control of the Forward 1 ramp generator. Throughout the acceleration period, a DATA BUSY signal generated on the Function Control A (see Schematic 100358) circuit board indicates that the transport is unable to accept data. At the end of the acceleration period, the DATA BUSY signal goes false; therefore, data and WRITE DATA STROBEs can be accepted. Figure 4-9 shows typical waveforms.

On receipt of a WRITE DATA STROBE, the data level on the input wire is strobed into the Buffer 2 flip-flop for each channel via AND gate 806. In the transport, a "1" on the data line causes Buffer 2 to toggle (a "0" leaves it unchanged).

Flip-flop 8D is set and the Q output transmitted via AND gate 811 (since flip-flop 8E is reset) to the 4-μsecond delay. The output of the delay resets flip-flop 8D and sets flip-flop 8E. The output of the delay is therefore a pulse delayed approximately 9 μseconds from the leading edge of the WRITE DATA STROBE. This output also enables AND gates 807 and 808, which transfers the status of Buffer 2 to Buffer 1. Approximately 15 μseconds after the WRITE DATA STROBE, a pulse (WRITE PULSE) is generated (from the Function Control A circuit board) which copies the status of Buffer 1 into flip-flop 8C via AND gates 809 and 810 and resets flip-flop 8E. Flip-flop 8C is the Write current generator. The magnetization direction is changed on the tape whenever a "1" is to be recorded.

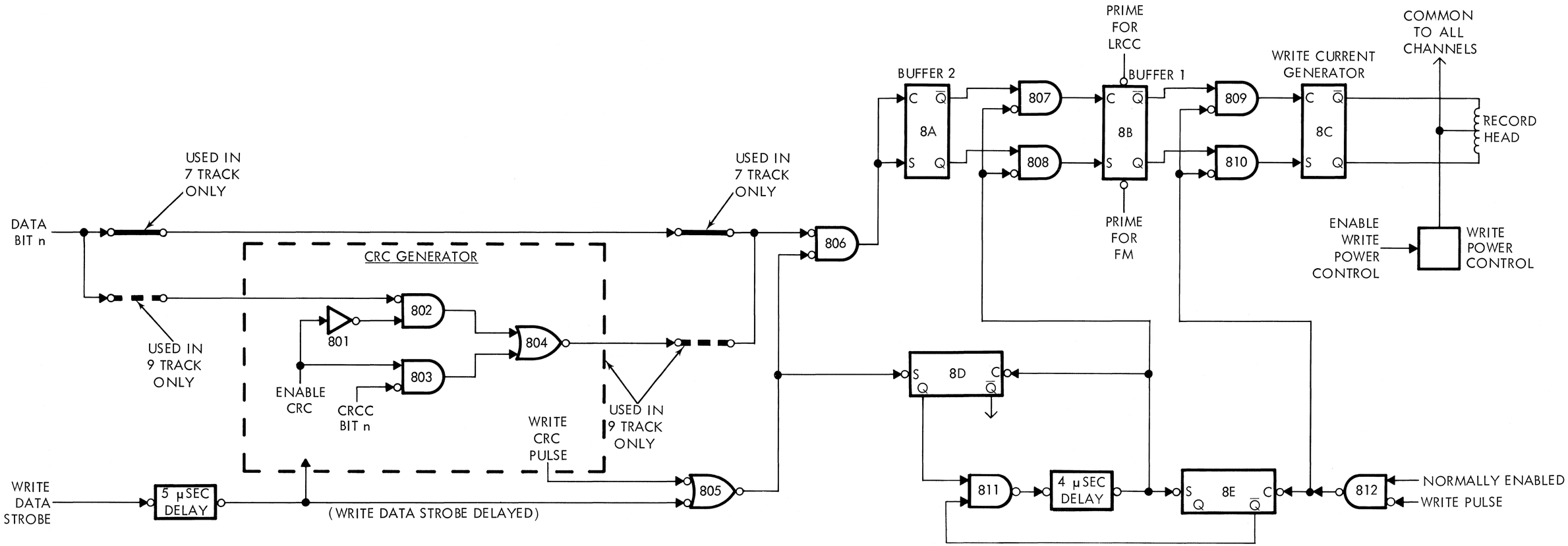

Figure 4-8. One Channel of Data Electronics and Controls

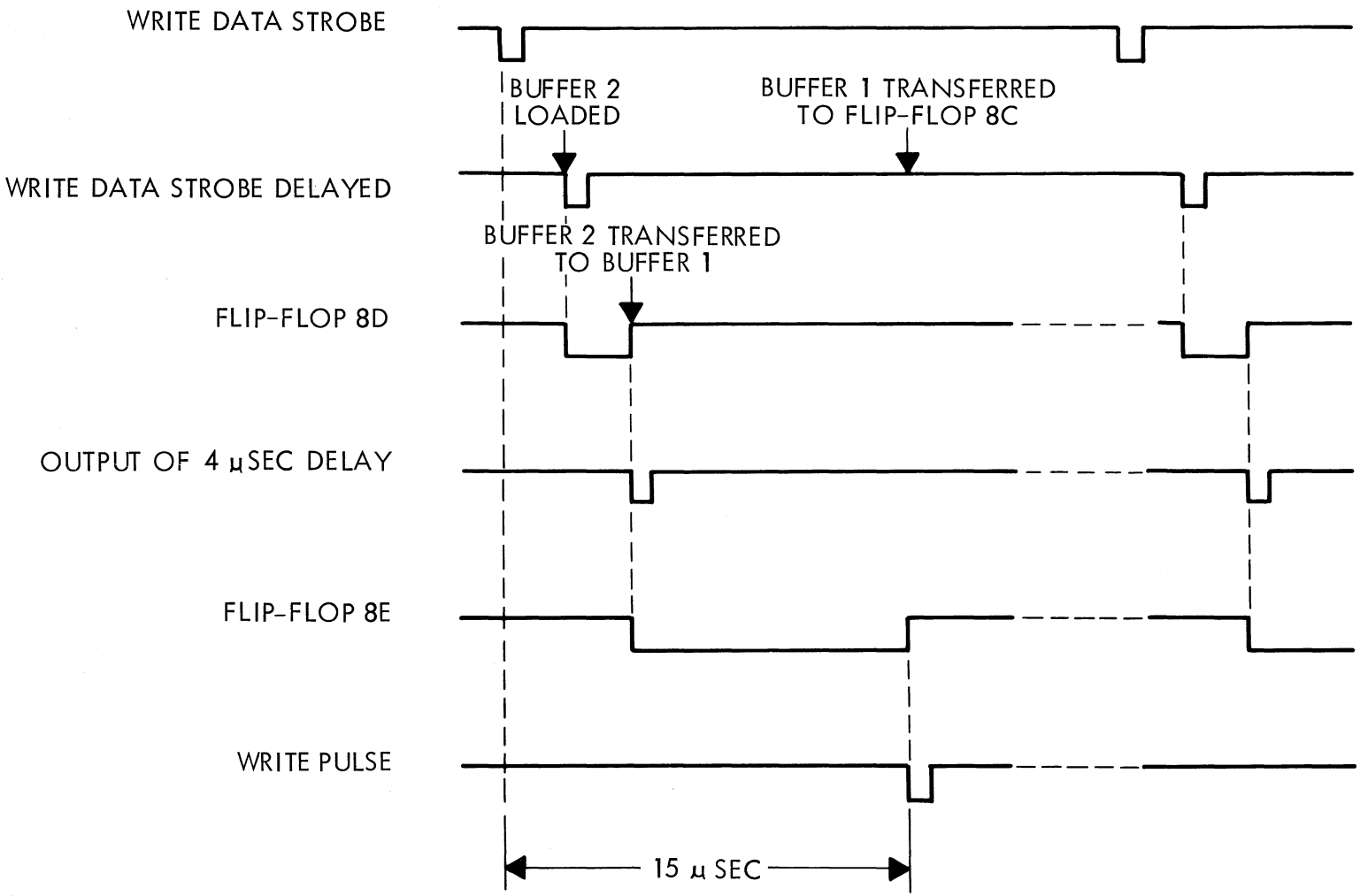

Figure 4-9. Control Waveforms

4-20. Error Checking Systems

4-21. General

In any information recording system, it is desirable to provide safeguards against loss of information during the recording process and also to provide error detection and correction during the subsequent reproducing process.

The most satisfactory way to check the recording process is to read back the recorded information and check it against the data source before discarding the original data. Alternatively, the parity of the readback information can be checked.

These techniques require a read facility and particularly a read-after-write system for efficient operation. In the absence of read-after-write facilities, an Echo Check system can be used and this is offered as an option with PEC tape transport systems.

To provide facilities for error detection and correction during the reproducing process, a parity bit is recorded with each data character and at the end of a record, Cyclic Redundancy Check characters (CRCC) and/or Longitudinal Redundancy Check characters (LRCC) are recorded. Parity, LRCC, and, where appropriate, CRCC generation facilities are provided in all PEC Synchronous Write Tape Transports.

These error checking systems are briefly described in the following paragraphs.

4-22. Echo Check System

Information is recorded in the NRZI mode; i.e., reversal of magnetization on the tape occurs for each "1" recorded. This is accomplished by feeding current into either one or the other half

of a center-tapped head. Whenever current is switched off in one half of the head (and switched on in the other half) the voltage at the end of that half swings below the return voltage of the center tap due to the inductive nature of the recording head. The negative swings from each half of the head associated with a particular channel are used to generate pulses. These pulses trigger a flip-flop associated with that channel. The outputs of these flip-flops are fed to a parity-tree check system whose output is interrogated at the appropriate time. If the parity is incorrect, a flip-flop is set and the output, ECHO CHECK ERROR, is fed to the interface. This flip-flop will remain set until reset by the customer or at the end of a record by internal logic. The occurrence of an ECHO CHECK ERROR signal does not cause any internal action in the transport. The circuitry and control logic associated with the Echo Check system is described in Paragraph 5-32.

4-23. Error Correction Characters

In addition to the usual parity bit associated with each character, additional error detection and correction characters are provided. In a 7-track system, one LRCC is written at the end of a record. This character is used to give a Longitudinal Parity Check on each track and is such that the total number of "1s" (i.e., transitions) in any one track including the LRCC bit is even.

In a 9-track system, two check characters are written at the end of each record. The first character is the CRCC; the second character is an LRCC similar to the one used in 7-track operation. The use of a CRCC is the basis for an error correction technique which employs a modified cyclic code in conjunction with the character parity to correct error bursts of unlimited length in any one of the 9 tracks. Errors involving more than one track within the same record are detected but cannot be corrected.

The CRCC is generated in the CRC Register (CRCR) (see Paragraph 5-33) according to the following rules.

(1) All data characters in the record are added to the contents of the CRCR without carry. Each data bit is exclusive OR'd to the corresponding bit of the CRCR.

(2) Between additions, the CRCR is shifted one position (CRCP to CRCO, etc., and CRC7 to CRCP).

(3) If shifting will cause CRCP to become a "1", the bits being shifted into positions CRC2, CRC3, CRC4, and CRC5 are inverted.

(4) After the last data character has been added, the CRCR is shifted once more in accordance with the first two steps.

(5) The contents of all the CRCR positions except CRC2 and CRC4 are inverted and the resultant character written on the tape.

4-24. Insertion of IBM-Compatible Gaps and Special Characters

Two types of gaps are used when writing IBM-compatible tapes. These are the Inter-Record gap and the File gap.

4-25. Inter-Record Gap

An Inter-Record Gap (IRG) is used to separate groups of characters which comprise a record of information. Records may be of variable length.

In a 7-track system, the IRG control generates a standard 0.75-inch IBM-compatible IRG (see Figure 4-10). When an IRG is inserted, an LRCC is written four character spaces after the last data character of the record as shown in Figure 4-10. This Longitudinal Parity Check character is such that the total number of "1s" (i.e., transitions) in any one track is even.

In a 9-track system, the IRG control generates a standard 0.6-inch IBM-compatible IRG. When an IRG is inserted, a CRCC is written four character spaces after the last data character of the record. This is followed after four character spaces (i.e., a total of 8) by the LRCC (see Figure 4-11).

4-26. File Gap

A File Gap is used to separate files of information and is identified by a special character on the tape. In general, the number of different files on a single reel of tape will be small and the File Gap time is not critical. The File Gap control is designed to generate a standard IBM-compatible File Gap with appropriate identification.

In a 7-track system, the sequence is writing an LRCC for the last record, moving approximately 3.8 inches, writing the File Mark character (binary 15), and then inserting an IRG. This IRG contains the LRCC associated with the File Mark character (see Figure 4-12).

In a 9-track system, the sequence is writing the CRCC and the LRCC for the last record, moving approximately 3.8 inches, writing the File Mark character (a "1" digit in data channels 3, 6, and 7) and then inserting an IRG. This IRG contains the LRCC associated with the File Mark character, but no CRCC is written (see Figure 4-13).

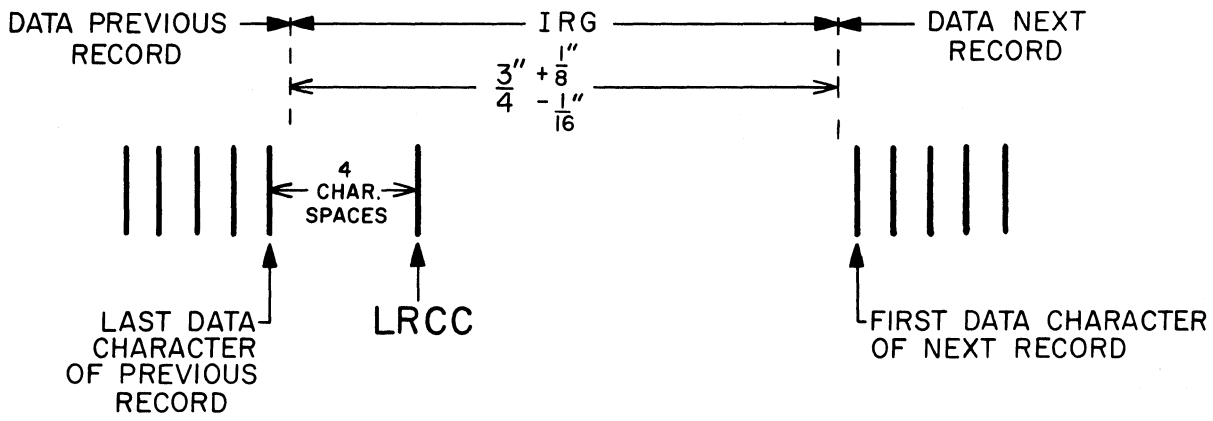

Figure 4-10. IRG Format — 7-Track

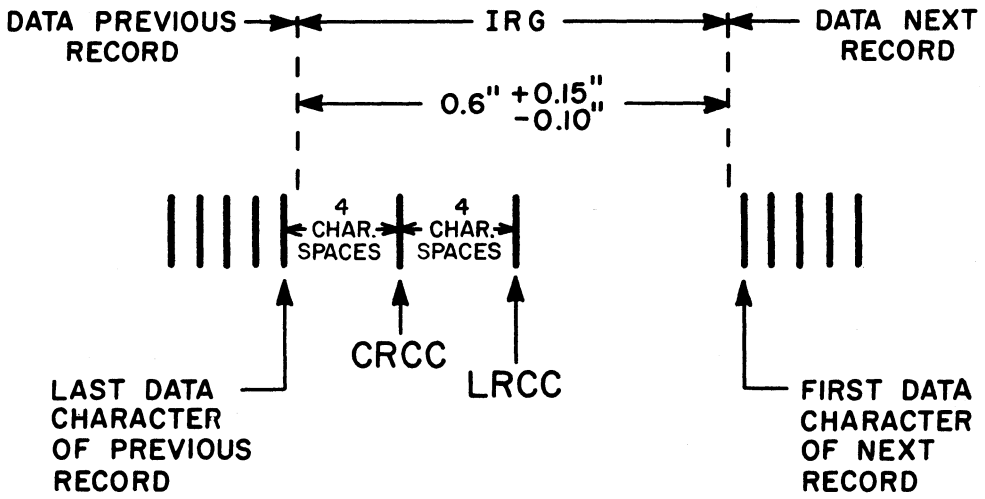

Figure 4-11. IRG Format — 9-Track

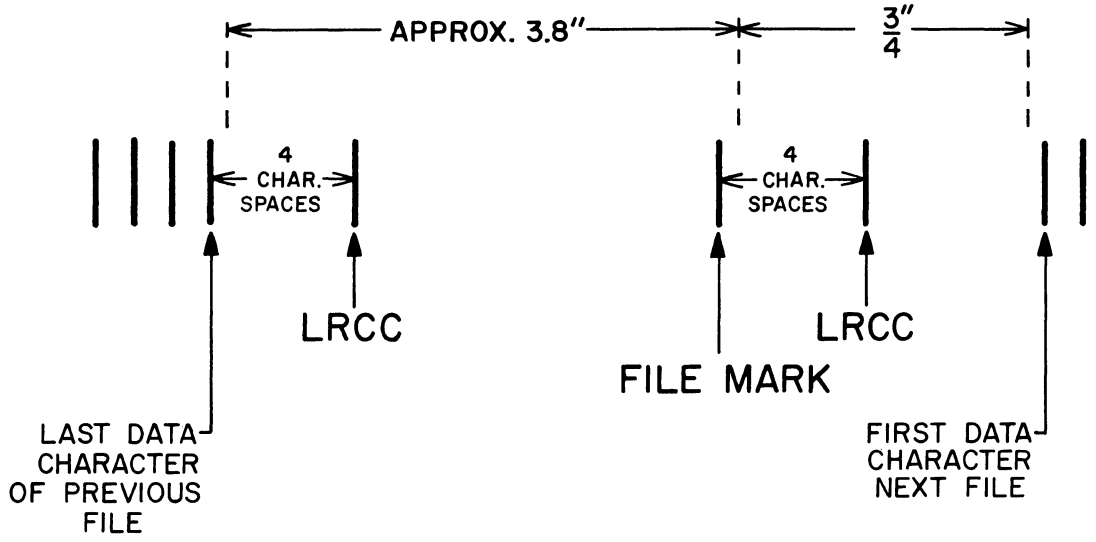

Figure 4-12. File Gap Format — 7-Track

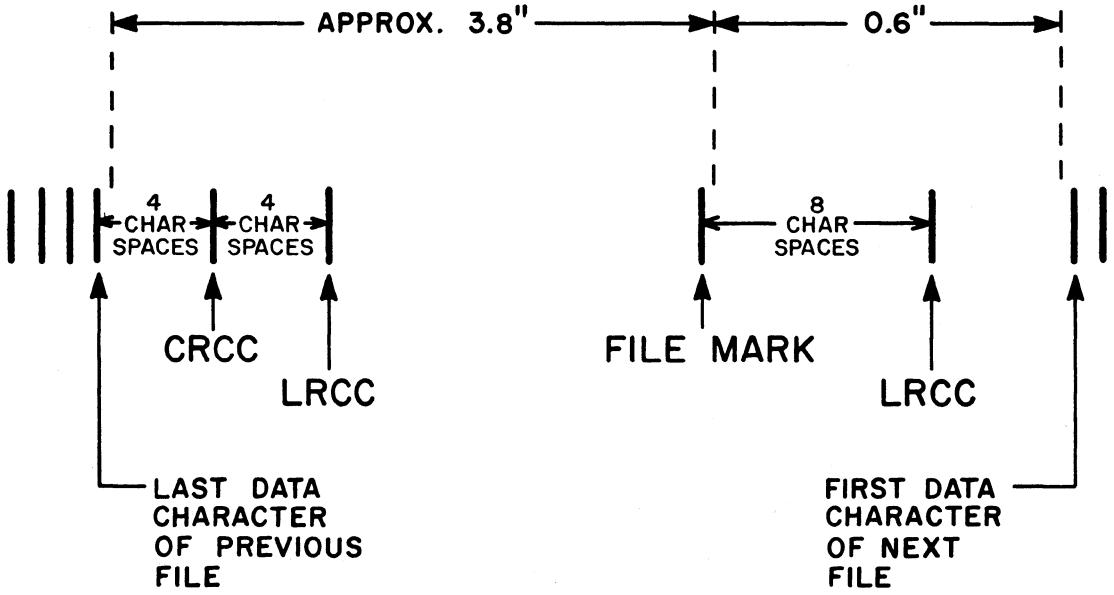

Figure 4-13. File Gap Format — 9-Track

4-27. Generation of Inter-Record Gaps

There are two methods for generating an IRG with this system. They are detailed in the following paragraphs.

(1) Case (a). Whenever the SYNCHRONOUS FORWARD command is terminated, an IRG is inserted together with the appropriate check characters. The distance during deceleration of the tape is approximately one-half of the IRG; the second half of the IRG distance occurs after the next SYNCHRONOUS FORWARD command is issued. It is assumed that the termination of the SYNCHRONOUS FORWARD command occurs coincident with the last WRITE DATA STROBE in the record, otherwise incorrect placement of the check characters might result.

(2) Case (b). When an IRG command is given while the SYNCHRONOUS FORWARD command is true, an IRG will be inserted "on the fly". This is used to generate IRGs between records, and to write the appropriate check characters at a constant tape velocity; i.e., when tape stopping is not desired. It is assumed that the IRG command is issued coincident with the last WRITE DATA STROBE in the record, otherwise incorrect placement of the check characters might result.

4-28. Case (a) IRG Generation — 7-Track Mode

Refer to Figure 4-14, a block diagram of the control logic, and Figure 4-15, the relevant timing diagrams, for this discussion. During data recording, the SYNCHRONOUS FORWARD command is true and the Forward 1 ramp generator is enabled, causing tape to move. WRITE DATA STROBEs (Plot 7) are received via the interface and trigger the 15-μsecond single-shot 14SS5 via gate 1413. The output (WRITE PULSE) from the single-shot is therefore a train of pulses.

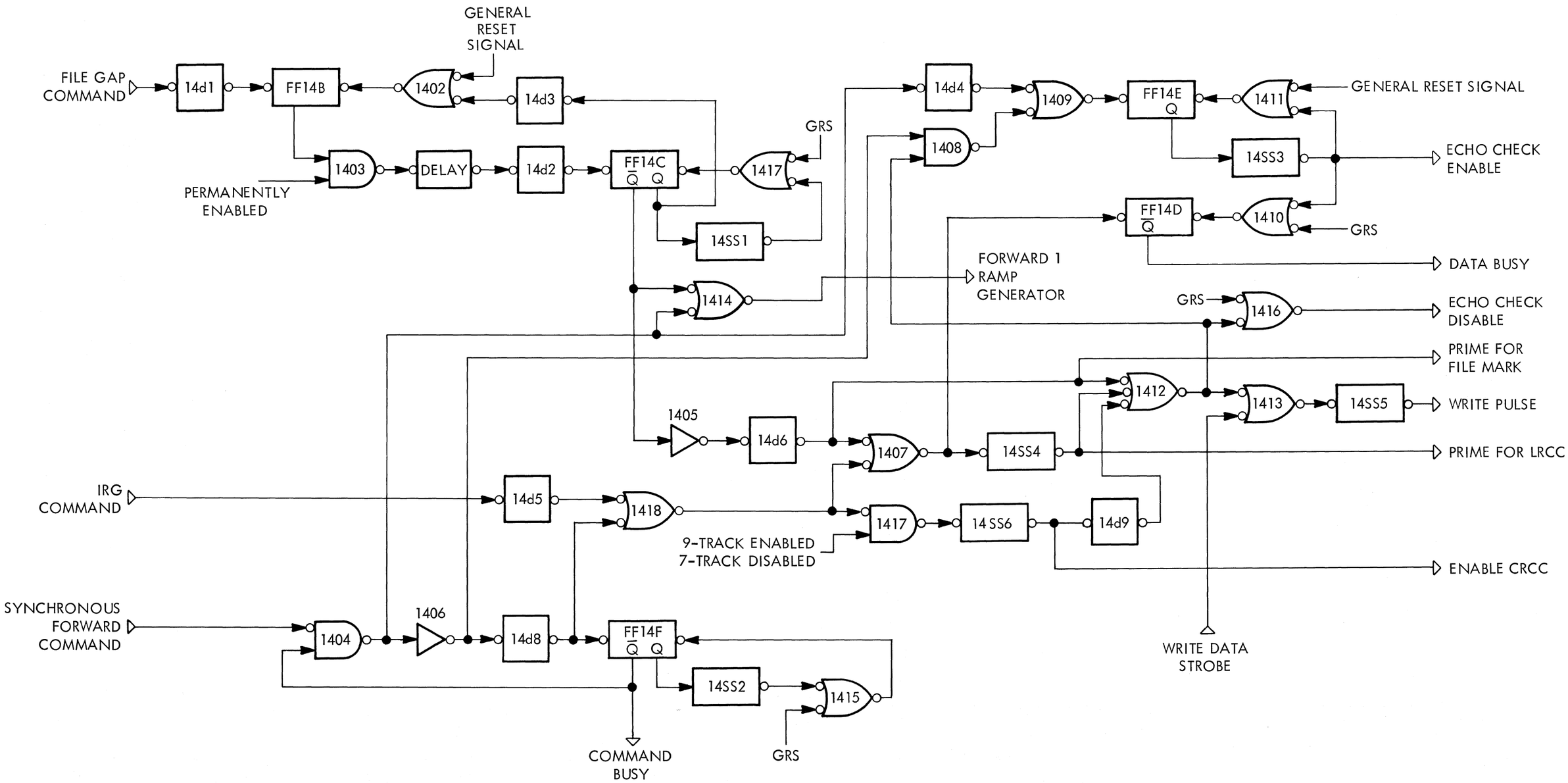

Figure 4-14. Gapping Control Logic

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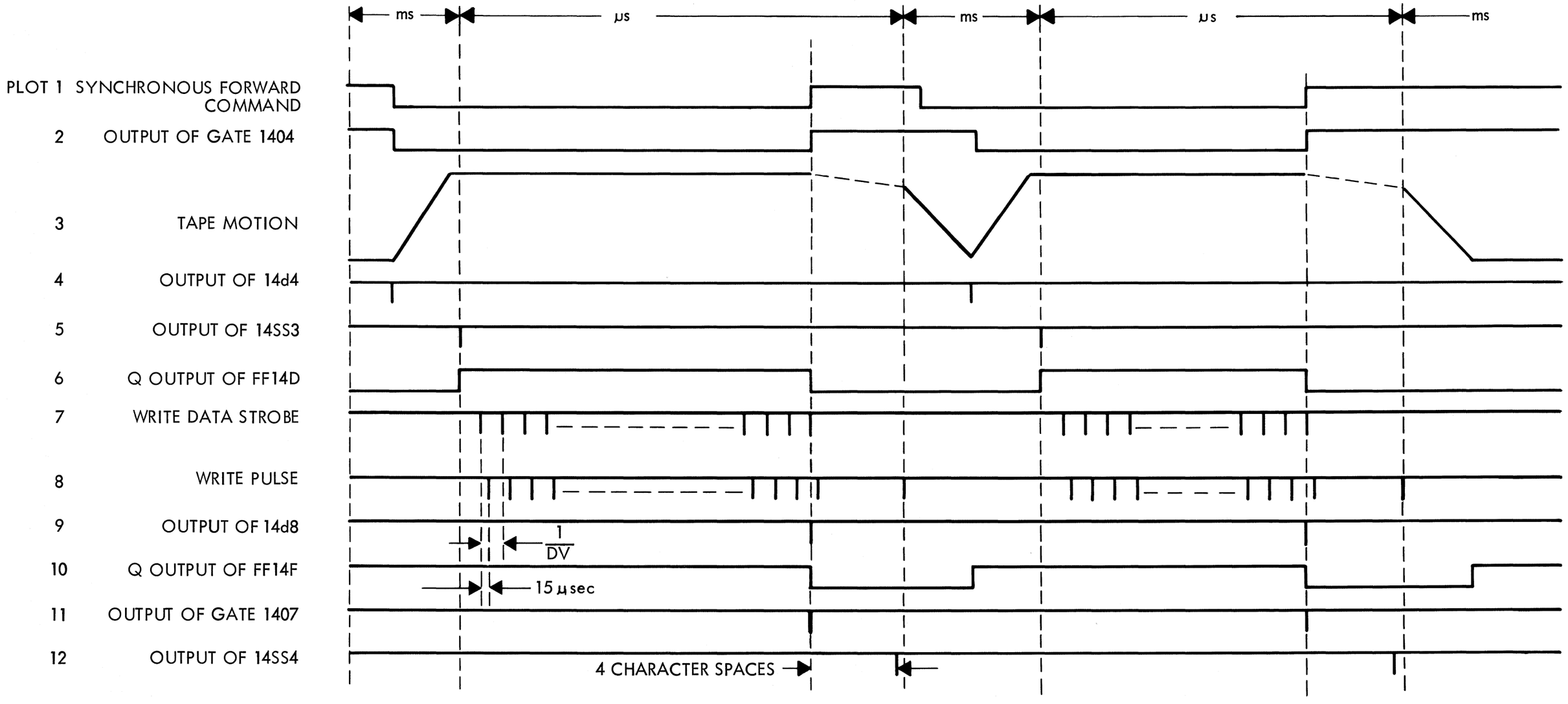


D = DENSITY (bpi)
V = VELOCITY (ips)

Figure 4-15. IRG Sequence for Case (a) Timing Diagram — 7-Track

(Plot 8) delayed 15 μseconds from the WRITE DATA STROBE. The WRITE DATA STROBEs are used in the data recording electronics as described in Paragraph 4-19. When the SYNCHRONOUS FORWARD command goes false (Plot 1) the Forward 1 ramp generator is disabled and the tape decelerates. In addition, the output of inverter 1406 goes true and a pulse is generated by differentiator 14d8 (Plot 9). This pulse does the following.

(1) Sets flip-flop 14D (Plot 6) generating a DATA BUSY signal.

(2) Sets flip-flop 14F (Plot 10) generating a COMMAND BUSY delay. (This COMMAND BUSY delay is used internally to ensure that tape motion has stopped before the transport will act upon the next motion command.)

(3) Triggers single-shot 14SS4 via gate 1407. The single-shot time is the duration of four character spaces and at the end of this time a pulse is generated (Plot 12). This output (PRIME for LRCC) is used to reset all the Buffer 1 flip-flops in the recording electronics (see Figure 4-8) using the leading edge. It is also used to trigger the 15-μsecond single-shot 14SS5 via gates 1412 and 1413. An additional WRITE PULSE is generated (Plot 8) in this way and is used to write the LRCC on the tape.

The process described occurs during the deceleration of the tape; however, the deceleration time is several milliseconds so that the change of velocity over the four character spaces involved is negligible.

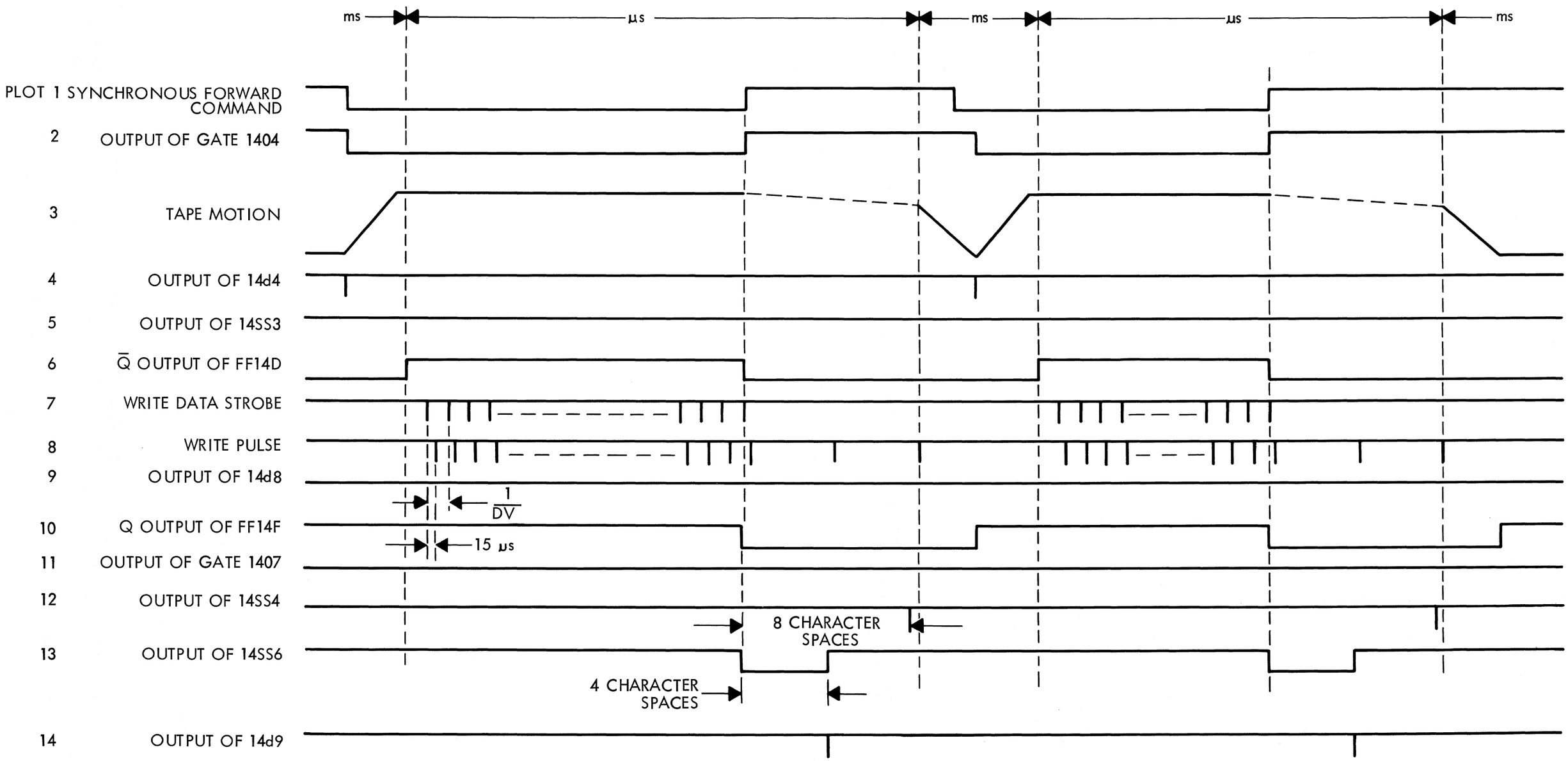
The deceleration time from the synchronous tape velocity results in a tape motion of less than one-half of an IRG distance from the last character until motion ceases. When the SYNCHRONOUS FORWARD command goes true, one input of gate 1404 is enabled. If

sufficient time has elapsed since the termination of the previous SYNCHRONOUS FORWARD command, the $\overline{Q}$ output of flip-flop 14F will be true and the SYNCHRONOUS FORWARD command will be transmitted to differentiator 14d4 and to the Forward 1 ramp generator via gate 1414. If insufficient time has elapsed, gate 1404 will be inhibited by the $\overline{Q}$ output of flip-flop 14F (Plot 10) until the COMMAND BUSY delay is complete.

The SYNCHRONOUS FORWARD command then re-enables the Forward 1 ramp generator and the tape accelerates to the specified velocity. A pulse is generated by differentiator 14d4 (Plot 4) which triggers flip-flop 14E, enabling single-shot 14SS3. After an appropriate delay, a pulse is generated by the single-shot (Plot 5) which resets flip-flops 14E and 14D, causing the DATA BUSY signal (Plot 6) to go false. This indicates to the customer controller that data may be transmitted to the transport. It has already been stated that the tape moves somewhat less than one-half of an IRG distance during the deceleration time. Similarly, during the acceleration period the tape also moves somewhat less than one-half of an IRG distance. The single-shot (14SS3) delay is designed so that after the acceleration phase, the tape moves at synchronous velocity for some distance before the first data are recorded. The magnitude of the delay is chosen so that the sum of the distance moved during the deceleration phase plus the distance moved during the acceleration phase and the extra distance discussed is equal to the required displacement.

4-29. Case (a) IRG Generation — 9-Track Mode

Refer to Figure 4-14, a block diagram of the control logic, and to Figure 4-16, the relevant timing diagrams, for this discussion. Data recording proceeds as described in Paragraph 4-28 until the SYNCHRONOUS FORWARD command goes false (Plot 1), and the



D = DENSITY (bpi)
V = VELOCITY (ips)

Figure 4-16. IRG Sequence for Case (a) Timing Diagram — 9-Track

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Forward 1 ramp generator is disabled and the tape decelerates. The output of inverter 1406 goes true and a pulse is generated by differentiator 14d8 (Plot 9). This pulse does the following.

(1) Sets flip-flop 14D (Plot 6) generating a DATA BUSY signal.

(2) Sets flip-flop 14F (Plot 10) generating a COMMAND BUSY delay. (This COMMAND BUSY delay is used internally to ensure that tape motion has stopped before the transport will act upon the next motion command.)

(3) Triggers single-shots 14SS4 and 14SS6 via gates 1407 and 1417, respectively.

The output of single-shot 14SS6 (ENABLE CRCC) is a gate (Plot 13) of duration equivalent to four character spaces at synchronous forward velocity. It is used by the CRC generator to complete the generation of the CRCC (see Paragraph 5-33) and transfers it to the Buffer 2 and then Buffer 1 flip-flops in the recording electronics.

A pulse (Plot 14) is generated from the back edge of the gate by differentiator 14d9, which triggers the 15-μsecond single-shot 14SS5 via gate 1412. An additional WRITE PULSE is thus generated (Plot 8) and is used to write CRCC on the tape.

The output of single-shot 14SS4 is a pulse (Plot 12) delayed the equivalent of eight character spaces at synchronous forward velocity. This pulse is used to reset all the Buffer 1 flip-flops in the recording electronics, using the leading edge. It also triggers the 15-μsecond single-shot 14SS5 via gates 1412 and 1413. A second additional WRITE PULSE is thus generated (Plot 8) and used to write the LRCC on tape. The remainder of the IRG sequence is identical with that described in Paragraph 4-28.

4-30. Case (b) IRG Generation "On the Fly" — 7-Track Mode

Refer to Figures 4-14 and 4-17 for this discussion. If an IRG command is given while the SYNCHRONOUS FORWARD command is still true, the following sequence occurs. Figure 4-17 shows the relevant timing diagram.

Data recording proceeds as previously described. When the IRG command is given (Plot 9), a pulse is generated by differentiator 14d5. This pulse does the following.

(1) Sets flip-flop 14D (Plot 6) via gates 1418 and 1407, informing the controller that data is busy.

(2) Triggers single-shot 14SS4 via gates 1418 and 1407. The single-shot time is the duration of four character spaces and at the end of this time a pulse is generated (Plot 12). This output (PRIME for LRCC) is used to reset all the Buffer 1 flip-flops in the recording electronics (Figure 4-8), using the leading edge. It is also used to trigger the 15-μsecond single-shot 14SS5 via gates 1412 and 1413. Thus, an additional WRITE PULSE is generated (Plot 8) to write the LRCC on the tape.

The pulse output of 14SS4 is also transmitted to gate 1408, via gate 1412. Since SYNCHRONOUS FORWARD command is still enabled, the output of gate 1406 is true and flip-flop 14E is set via gate 1409. After an appropriate time which allows the IRG distance to be traversed at a constant tape speed, single-shot 14SS3 generates the reset pulse (Plot 5) for flip-flops 14D and 14E.

DATA BUSY goes false, signaling that further data recording should begin. The distance traversed between the last WRITE DATA STROBE of the previous record and the first WRITE DATA STROBE of the next record is nominally 0.75 inch.

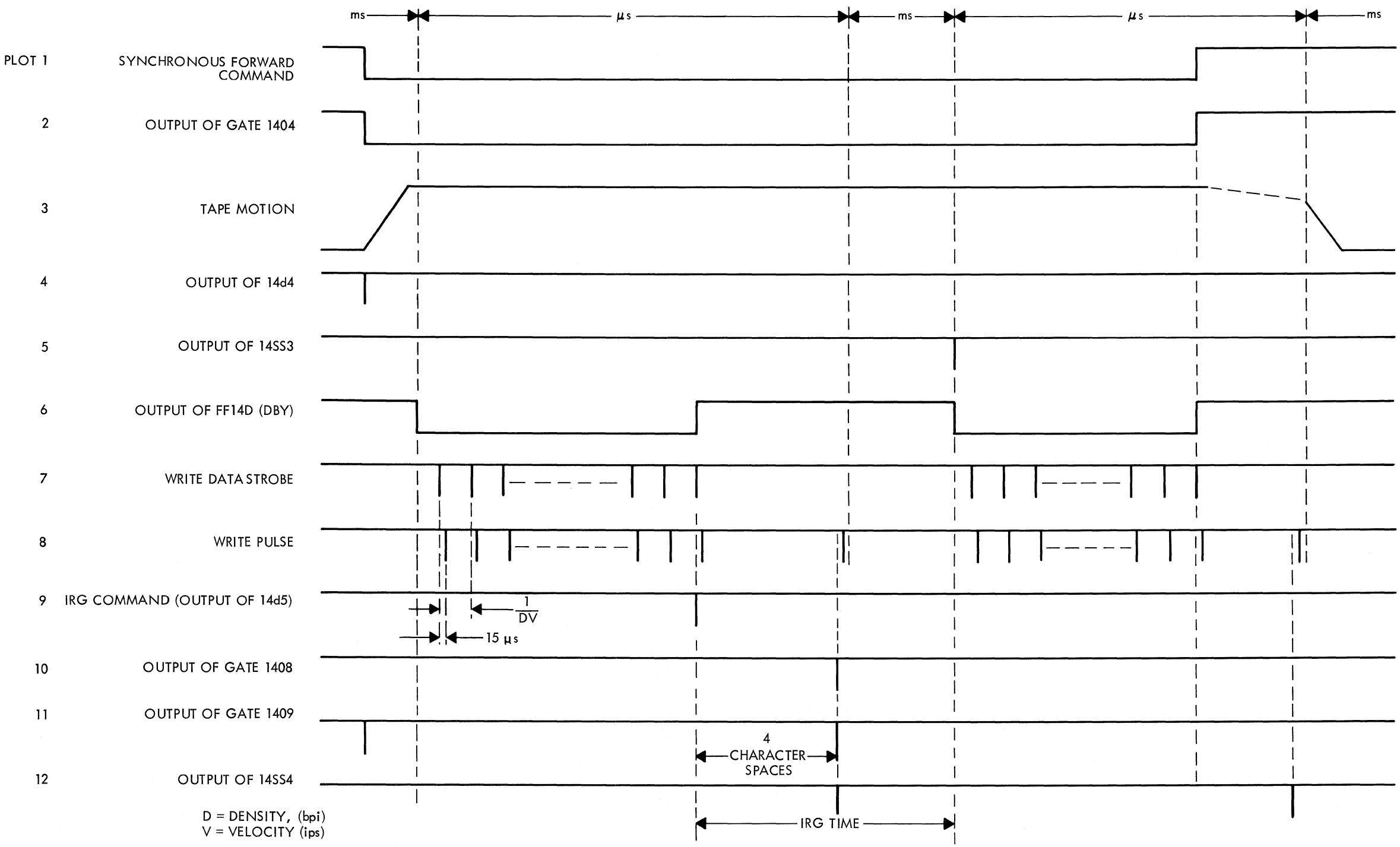

Figure 4-17. IRG Sequence On the Fly Timing Diagram — 7-Track

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When the SYNCHRONOUS FORWARD command goes false, an LRCC character is inserted and the tape decelerates to rest in approximately one-half of an IRG as described in Paragraph 4-28.

4-31. Case (b) IRG Generation "On the Fly" — 9-Track Mode

Refer to Figures 4-14 and 4-18 for the block diagram and the relevant timing diagrams for this 9-track mode. The discussion of the IRG generation is similar to Paragraph 4-30. The exception is writing the CRCC via 14SS6 as described in Paragraph 4-29.

4-32. File Gap Generation

This discussion assumes that data recording is proceeding and a FILE GAP command is issued coincident with the termination of the SYNCHRONOUS FORWARD command. Figure 4-14 is a block diagram of the control logic and Figures 4-19 and 4-20 represent the timing diagrams relevant to 7-track and 9-track operation, respectively.

The FILE GAP command (Plot 12) is applied to differentiator 14d1. The output pulse sets flip-flop 14B which then sets flip-flop 14C via differentiator 14d2, thus enabling single-shot 14SS1. The $\overline{Q}$ output of flip-flop 14C is transmitted to the Forward 1 ramp generator via OR gate 1414. Therefore, the Forward 1 ramp generator continues to be enabled after the termination of the SYNCHRONOUS FORWARD command for a time defined by single-shot 14SS1. At the end of this time flip-flop 14C is reset, disabling the Forward 1 ramp generator and the tape decelerates (Plot 3).

In addition, the termination of the SYNCHRONOUS FORWARD command (coincident with the FILE GAP command), generates a pulse via inverter 1406 and differentiator 14d8, which is fed to OR gate 1407 and AND gate 1417. The output of gate 1407 sets flip-flop 14D

(Plot 6) generating a DATA BUSY signal, and also triggers single-shot 14SS4 in both 7-track and 9-track systems. However, in a 9-track system, single-shot 14SS6 is also triggered via AND gate 1417.

In a 7-track system, the output of single-shot 14SS4 (Plot 10) resets the Buffer 1 flip-flops in the recording electronics (as discussed in Paragraph 4-28) and generates an additional WRITE PULSE (Plot 8) which writes the LRCC four character spaces after the last data character. In a 9-track system, the output of single-shot 14SS6 initiates the completion of the CRCC generation and causes the CRCC to be loaded into the Buffer 2 and then Buffer 1 in the recording electronics (as discussed in Paragraph 4-29). It also generates an additional WRITE PULSE (Plot 8) which writes the CRCC four character spaces after the last data character. The output of single-shot 14SS4 causes the LRCC to be written eight character spaces after the last data character (as discussed in Paragraph 4-29).

At the end of the File Gap time, flip-flop 14C is reset and the $\overline{Q}$ output goes high. This edge is transmitted by inverter 1405 and differentiator 14d6, which generates a pulse (Plot 14). This pulse (PRIME for FM) is used to set the relevant flip-flops (depending on whether the 7-track or 9-track modes are operational) in the recording electronics (Figure 4-8), using the leading edge. It also triggers single-shot 14SS5 via gates 1412 and 1413, generating a WRITE PULSE which is used to write the File Mark on the tape.

The pulse output of differentiator 14d6 also triggers single-shot 14SS4 via gate 1407. The output of the single-shot (Plot 10) resets the Buffer 1 flip-flops in the recording electronics and generates a corresponding WRITE PULSE via single-shot 14SS5 (Plot 8). This writes the LRCC character for the File Mark four character spaces after the File Mark for 7-track, or eight character spaces after the File Mark for 9-track systems. The distance traversed in the deceleration phase is less

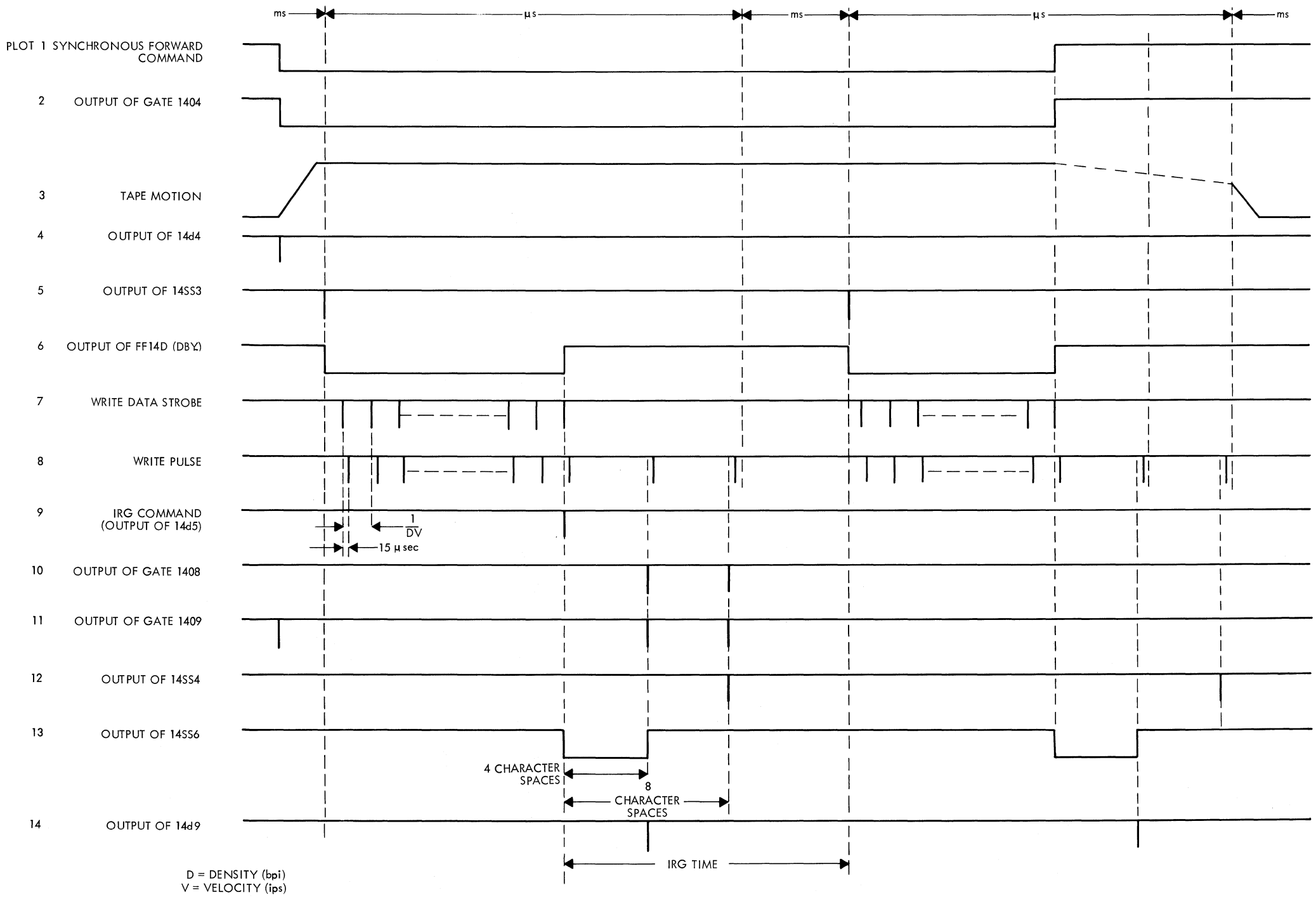

Figure 4-18. IRG Sequence On the Fly Timing Diagram — 9-Track

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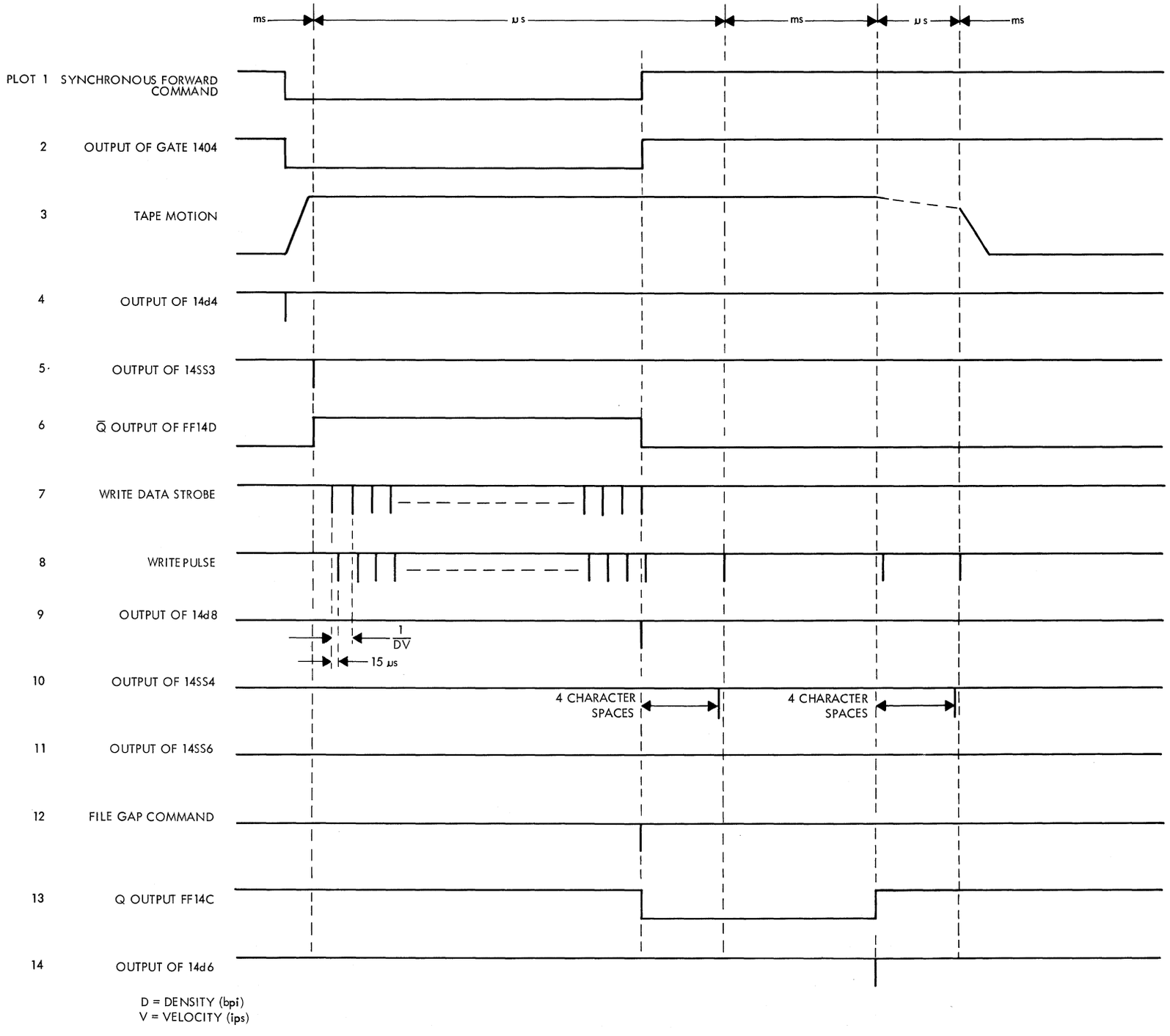

Figure 4-19. File Gap Sequence Timing Diagram — 7-Track

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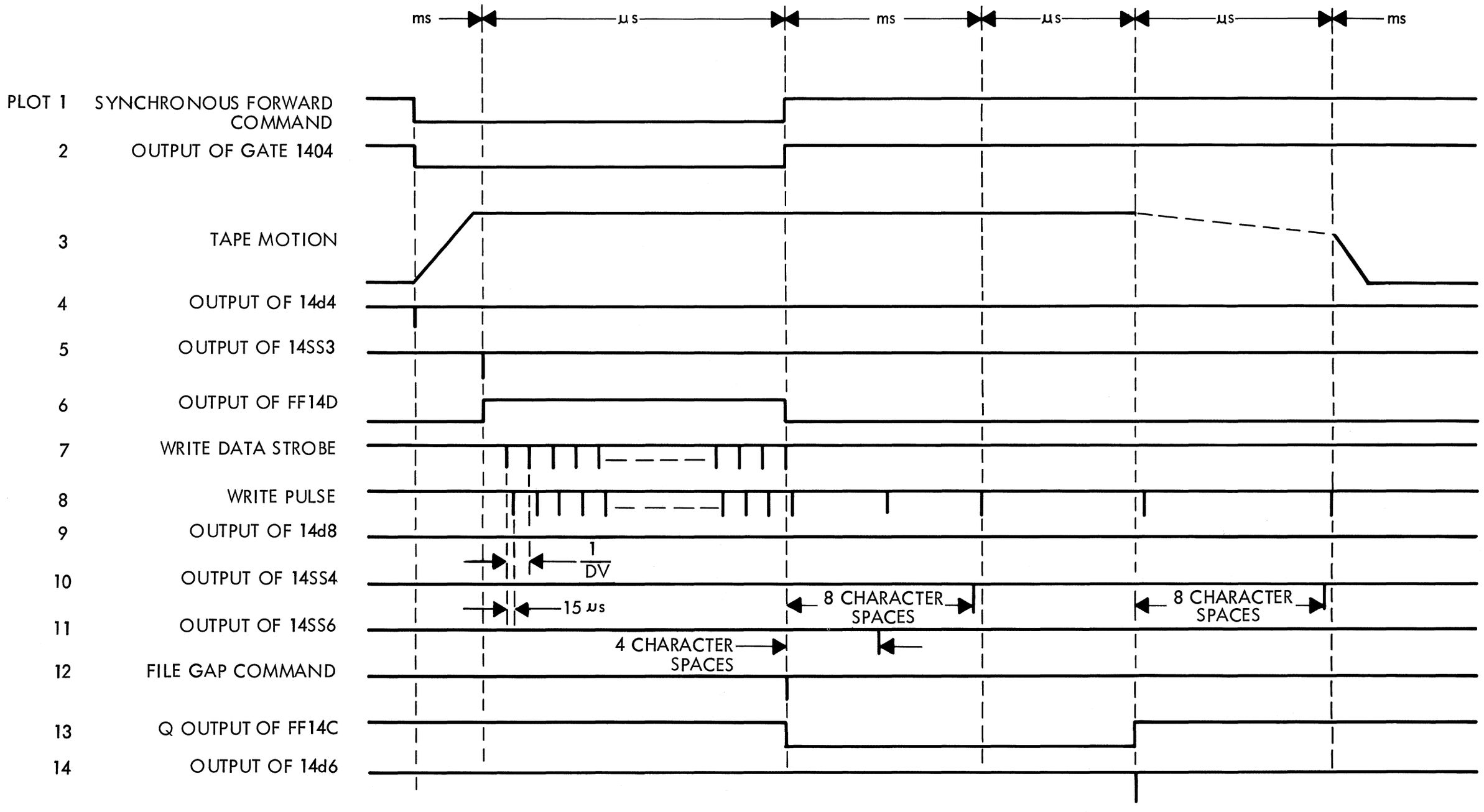

D = DENSITY (bpi)
V = VELOCITY (ips)

Figure 4-20. File Gap Sequence Timing Diagram — 9-Track

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than the IRG distance required at the end of a File Gap. The remainder of the IRG distance is covered in the acceleration phase prior to the next data recording period.

4-33. Echo Check Control

During the gapping process, File Mark and LRCC characters are written (Figure 4-14). The parity of the File Mark is even in a 7-track system and odd in a 9-track system. The LRCC character parity depends on the number of characters in the record. Since the Echo Check system operates on the assumption that the parity will be the same as that of the data, it is necessary to inhibit the Echo Check system during gapping. In a 7-track system, the output of single-shot 14SS4 is used to disable the Echo Check system via gates 1412 and 1416. Note that this occurs 15 μseconds before the LRCC character is written on the tape.

In a 9-track system, the output of single-shot 14SS6 is used to disable the Echo Check system via gates 1412 and 1416. Note that this occurs 15 μseconds before the CRCC is written on the tape.

The pulse output of single-shot 14SS3 that causes the DATA BUSY signal to go false is also used to enable the Echo Check system.

SECTION V
PRINTED CIRCUIT BOARDS THEORY OF OPERATION

5-1. INTRODUCTION

This section contains the theory of operation of the printed circuit boards used in the Synchronous Write Tape Transport. All standard boards are included. The specific boards and the relevant versions used in a typical transport are discussed in Paragraph 5-34. The schematic and assembly drawing for each board and the system wiring diagrams are contained in Section VII.

A better understanding of the logic utilized in the tape transport can be gained when the operation of the J-K flip-flop is fully understood. The following paragraphs provide a brief summary of the operation of the 852 J-K flip-flop, which is the type most commonly used in the system.

This flip-flop operates on a "Master-Slave" principle. A logic diagram of the flip-flop is shown in Figure 5-1. The flip-flop is designed so that the threshold voltage of AND gates 101 and 102 is higher than that of AND gates 103 and 104. Since operation depends exclusively on voltage levels, any waveform of the proper voltage levels can trigger the J-K flip-flop.

Assume that the trigger voltage is initially low. When the trigger voltage goes high, AND gates 103 and 104 are disabled. Subsequently, AND gates 101 and 102 are enabled by the trigger pulse, the J and K inputs, and the information previously stored at the output of the "slave" unit. The J and K input information at this time is transferred to the input of the "master" unit. When the trigger voltage goes

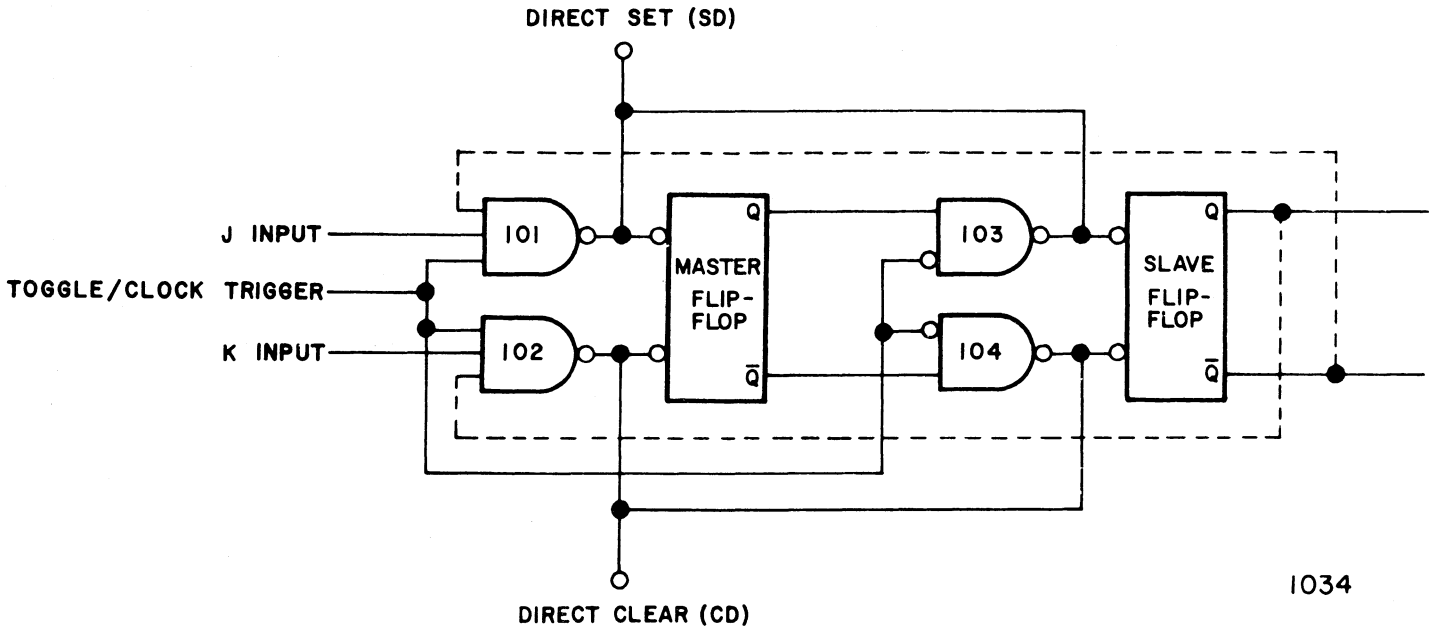


Figure 5-1. Simplified Logic Diagram, "Master-Slave" Flip-Flop

low, AND gates 101 and 102 are disabled. AND gates 103 and 104 are then enabled and the information stored in the "master" unit is transferred to the output of the "slave" unit.

5-2. THEORY OF OPERATION

5-3. REEL SERVO AND VOLTAGE REGULATOR – B

Refer to Schematic 100912 for this description. This circuit board contains reel servo amplifiers and four voltage regulators (+10, +5, -10, and -5 volts) that operate in conjunction with several externally mounted power transistors (shown in Schematic 100388 and referenced in Schematic 100912).

5-4. Reel Servo Amplifiers

Identical dc linear-position servo amplifiers are used for both the take-up and supply reel storage systems. The amplifiers are the conventional dc, Class B type.

In normal operation, the feedback network (R19, R20, R45, C7, C8, and R21 for the supply reel or R4, R5, R52, C2, C3, and R6 for the take-up reel) defines a gain of approximately 11 at frequencies below 1.5 Hz and a gain of approximately 100 above 15 Hz.

When the Rewind ramp is enabled, Q22 is turned on. Current through CR12 turns on Q23, establishing a ground return for resistor R51. This increases the dc gain of the take-up reel servo by a factor of approximately two when in the Rewind mode, to accommodate the higher velocity.

The gain of the supply reel servo is also increased in the Rewind mode. The ground return for resistor R46 is established through CR11.

Two external heatsink-mounted output transistors are associated with each amplifier (see Schematic 100388). Q201 and Q202 are used in the take-up amplifier and Q203 and Q204 in the supply amplifier. The input resistors, R1 and R16 (Schematic 100912), are driven by the 1000-ohm tension-arm potentiometers, R101 and R102 (Schematic 100388), which are connected between the +5- and -5-volt lines.

5-5. Voltage Regulators

(1) +10 Volts. A 10-volt zener diode (CR1) in series with diode CR2, supplied with current from a 100-ohm resistor (R31), connected to the +16-volt unregulated line is the voltage reference for the +10-volt supply. A power transistor (Q210) connected as an emitter-follower with the voltage reference on the base, completes the circuit. The +10-volt line is taken from the emitter of Q210 to the circuit board under discussion, where it drives the 6.8-volt zener diode (CR5) for the +5-volt regulator.

(2) +5 Volts. The +5-volt regulator supplies the bulk of the power to the circuit boards and is stablized within ±1 percent. A 500-ohm potentiometer (R36) is connected across the 6.8-volt reference diode (CR5) and an emitter-coupled comparator (Q16 and Q17) compares the +5-volt line with the voltage on the potentiometer wiper. The difference is amplified by transistor Q20 and again by power transistor Q207. Test Point 1 is connected to the +5-volt line. The +5-volt regulator can supply 3.0 amps.

(3) -10 Volts. Except for the additional inverting PNP transistor (Q15), operation of the -10-volt regulator is similar to the +10-volt regulator. The -10-volt line is returned from the collector of Q208 to the voltage regulator circuit board where it drives the 6.8-volt zener diode (CR6) for the -5-volt regulator.

(4) -5 Volts. Operation of the -5-volt regulator is identical in principle to that of the +5-volt regulator. Q209 is the power transistor associated with the -5-volt regulator. Test Point 2 is connected to the -5-volt line and Test Point 3 is connected to OV(L).

5-6. Overvoltage Protection

The anode of zener diode CR9 is connected to the gate of the "crowbar" SCR (Q211 on Schematic 100388) for the overvoltage protection. R44 and C15 keep the SCR from triggering due to transients during the power-on cycle.

5-7. CAPSTAN DRIVE, SYNCHRONOUS

Refer to Schematic 100474 for this description. This board comprises the capstan servo amplifier and stabilization networks, ramp generators, lamp drivers, general reset circuit, and the interlock relay driver.

5-8. Capstan Servo Amplifier

This consists of an integrated circuit input stage (U3-A) and a discrete component output stage with externally mounted power transistors Q205 and Q206 (see Schematic 100388). The low frequency gain from the tachometer to the amplifier output is defined by the ratio of R34 to R62 and R63, (i.e., K = 36). The dead-band of the amplifier is large enough that, with no input, the input offset voltage is not large enough to produce any output voltage. Test Point 1 is connected to the amplifier output. Test Point 5 is connected to the filtered tachometer output.

A 1-ohm power resistor (R203) is placed in series with the -16-volt line to the output stage to reduce power dissipation in Q206. Filter L1, C16 stabilizes the servo.

5-9. Ramp Generators

5-10. Forward 1 (Synchronous Forward and Load Forward)

This circuit is used to generate the command voltage for moving tape at the specified speed. Test Point 4 can be brought to approximately 1.5 volts by applying a 0-volt level to the appropriate input. (0 volt on pin 23 or pin 24 takes the voltage at TP4 to 1.5 volts for forward operation.) The rate at which the voltage on TP4 changes is controlled by the integrator, which consists of U2-B, C3, or C17, C18, or C19, C20, R13, R14, R16, and R17. The resulting tape velocity is determined by R21 and R22.

5-11. Rewind

This circuit generates the command voltage which results in a tape speed of 75 ips in the reverse direction. Rise and fall times are approximately 0.5 second, determined by R58, R64, and C15. When 0 volt is applied to pin 20, the emitter of Q13 reaches -5 volts.

5-12. Lamp Drivers

The four lamp drivers connect the lamps between +5 and -16 volts when the relevant input H, K, 8, or 5 is taken to 0 volt. The circuit is designed to supply 60 milliamps.

5-13. General Reset Circuit

When input L is high or open, a GENERAL RESET signal is applied to the appropriate control flip-flops by turning on Q18 so that the output, pin M, is taken to -0.8 volt.

5-14. FUNCTION CONTROL, SYNCHRONOUS B

Refer to Schematic 100442 for this description. This circuit board contains the logic required to bring the transport to operational status in conjunction with the manual and remote controls and photosensors.

Operation of the logic is described in detail in Paragraph 4-8 through 4-15, using Figure 4-5. The Cross Reference Chart, Table 5-1, will assist in identifying the major components in the system; however, 100 percent correspondence is not possible since Figure 4-5 is a logic diagram, while the schematic shows every component.

In addition to the integrated circuit logic, the circuit board contains the following discrete component circuits: switch-contact filter, differentiator, photosensors, and a single-shot.

Table 5-1

Function Control B
Cross Reference Chart

Figure 4-5 Reference Designations	Schematic 100442 Reference Designations
Flip-Flop 5A	U1-A, U1-B
Flip-Flop 5B	U1-C, U1-D
Flip-Flop 5C	U4-A, U4-B
Flip-Flop 5D	U4-C, U4-D
Flip-Flop 5E	U2-B, U2-A
Inverter 515	Q2 and Associated Components

5-15. Switch Contact Filter Circuit

The combination of resistor R7, capacitor C4, and resistor R6 is a typical switch-contact filter circuit. The main purpose of the circuit is to filter out noise caused by capacitive crosstalk between the switch lines that are cabled together in the same harness. R7 and C4 form the filter, while R6 ensures that the input to pin 1 of U1 is at +5 volts when the switch contact is open. Since the threshold of the IC is approximately 1.8 volts, considerable noise rejection is available.

5-16. Differentiators

A typical differentiator is designated 5d1 in Figure 4-5 and consists of components C5, R12, R10, and R11 (in Schematic 100442). Resistors R10 and R12 set the static level at the output of the differentiator at +3 volts, giving a noise immunity of 1.2 volts (typically). C5 is the differentiating input capacitor and resistor R11 limits the current that flows when the IC input is driven below 0 volt by capacitor C5, causing the substrate diode to conduct.

5-17. Photosensor Circuits

Two photosensor circuits are provided: one to detect the BOT tab and one to detect the EOT tab.

Two photo transistors and a lamp make up the Photosensor Assembly that is located on the head plate. Two collector loads for the two transistors are potentiometers R15 and R30, which allow the sensitivity of the circuit to be adjusted. The photo transistor output drive emitter followers Q1, Q10, and Q3; capacitors C7, C10, and C21 filter out any spurious signals picked up in the harness. Resistors R14, R64, and R31 limit the charging current that flows on positive-going edges.

5-18. Single-Shot

This circuit provides a delay for timing the distance between detecting the BOT tab and stopping tape. C11 and C12 are timing capacitors and R37 is the timing resistor. The gap time is adjusted by varying the potential (with R35) from which the capacitors start discharging. To generate the BOT gap, flip-flop U11-B, U11-A is set; therefore, Q4 is cut off.

When the potential at C11, C12 discharges to approximately 0 volt, transistor Q5 turns on, Q6 turns off, causing Q7 to turn on. The voltage at the collector of Q7 goes low, resetting flip-flop U11-B, U11-A; Q4 is then saturated and the circuit is returned to its initial state.

5-19. Write Power Control

In this circuit, the Ready status causes R44 to be taken to 0 volt, which turns on Q8 and Q9. The turning on of Q9 is slowed by C14 to avoid head current transients. The center taps of all of the head windings are connected to the collector of Q9. This point is connected to TP3.

5-20. TRANSMITTER – DTL

Refer to Schematic 100338 for this description. This circuit board is designed to convert the transport's internal logic levels to levels suitable for transmission over an interface cable that consists of twisted pairs of up to 20 feet in length. It operates with the Receiver-DTL circuit board or equivalent.

The input is compatible with DTL integrated circuits (0 volt true and 5 volts false). Two configurations are available resulting in high-true or low-true outputs. The high level as measured at the test

points is between +3 or +5 volts, depending on the receiver configuration. The low level is between 0 and +0.4 volt.

Inverters U1, U2, U3, and U7 are used only in the low-true configuration when the "dotted" jumper wire is inserted. In the high-true configuration, inverters U1, U2, U3, and U7 are omitted and the solid jumper wires are inserted. The 180-ohm pull-up resistors are connected to +5 volts externally, except where a pull-up resistor is used at the receiver end of the cable; in this case, they are omitted. The series 68-ohm resistor is included in certain versions to provide a partial source termination for negative-going edges. The output stage uses the DTL power gate type 844, or equivalent.

5-21. RECEIVER – DTL

Refer to Schematic 100333 for this description. This circuit board is designed to convert interface signals to standard logic levels. It terminates an interface cable that consists of multiple twisted pairs of up to 20 feet in length. It operates with the Transmitter – DTL circuit board or its equivalent. The board is also used to generate the parity bit for 6- or 8-bit characters in certain versions. Three configurations are used in different versions and are discussed in the following paragraphs.

5-22. Configuration A

Configuration A is used for high-true logic where a 180-ohm pull-up resistor is used at the transmitter output. The 68-ohm resistor (R1) and capacitor C1 reduce the reflections due to imperfect termination. The 470-ohm resistor (R2) causes the input to go low-false on removal of the cable.

5-23. Configuration B

Configuration B is used for low-true logic where a 180-ohm pull-up resistor is used at the transmitter output. The 68-ohm resistor (R1) and capacitor C1 reduce the reflections due to imperfect termination. The 470-ohm resistor (R2) of configuration A is removed so that the input goes high-false on removal of the cable. However, note that the removal of power at the transmitter results in a low-true condition if the 180-ohm resistor on the transmitter is allowed to "turn off" the input inverter of the receiver.

5-24. Configuration C

Configuration C is used for low-true logic and circumvents the possibility of interpreting the removal of power at the transmitter as a low-true signal. The pull-up for the input inverter of the receiver is located at the received end of the cable and a high resistance at the transmitter output ensures that loss of transmitter power or interruption of the interface cable cannot be interpreted as anything except a high-false signal. The parallel combination of resistors R1 and R2 results in the termination with close to the characteristic impedance of the line.

5-25. Parity Generator

The parity generation circuit used in certain configurations of the transport consists of cascaded "half-adders" which produce the parity bit at pins 8 and 11 of U7. If the total number of "1s" in the 6- or 8-bit character is odd, a low level results at this point; by switching S1 to the E position (for even parity), a "1" is written in the check bit track. If the total number of "1s" in the 6- or 8-bit character is even, a low level appears at pin 3 of U7; by switching S1 to the O position (for odd parity), a "1" is written in the check bit track. The third switch position, X, is used when the parity bit is included with the data

character and internal generation is not required. The externally generated parity bit must be brought into circuit 100.

5-26. Binary Zero to BCD10 Conversion

Inverters U4-F, U4-E, U1-A, U1-B, U1-D, and U1-F form an AND gate which produces a high output at pin $\overline{E}$ when the data character consists of six "0s". Unless pin $\overline{E}$ is tied to 0 volt externally, bits 2^1 and 2^3 will be forced to the "1" state by inverters U4-C and U1-F to produce the BCD1010 character. Unless otherwise specified, pin $\overline{E}$ is connected externally to 0 volt on J205, removing this facility.

5-27. DOUBLE BUFFER — WRITE AMPLIFIER

Refer to Schematic 100233 for this description. This circuit board is comprised of seven write amplifiers, two buffer registers for temporary storage of the write data, and control circuits.

The two buffer registers consist of seven J-K flip-flops; each is comprised of a master and a slave flip-flop. These correspond to flip-flops 8A and 8B of Figure 4-8. The master flip-flop toggles on receipt of a "1" and the output is copied successively into the slave flip-flops and then to Write amplifiers Q4 through Q17 (see flip-flop 8C of Figure 4-8). The Write amplifier is a resistor-transistor flip-flop which defines the write current by means of resistors (R26, etc.) in series with the head windings. The head-winding center tap is taken to -5 volts when the write current is enabled. Test points 1 through 7 are connected to the write amplifier outputs.

At the Write Data inputs (WD0 through WDP) 0 volt represents a "1". The WRITE PULSE that toggles the master flip-flop in response to write data "1s" is generated from the WRITE DATA STROBE. The 2-μsecond pulse at TP8 is generated from the trailing edge of the output

of single-shot Q1, Q2. After being delayed 4 μseconds by U12-A, U12-B, R20, C8 and R21, C9, this pulse sets the control flip-flop, U13-D, U13-C (see flip-flop 7E of Figure 4-8). This delayed pulse also copies the content of the master flip-flops into the slave flip-flop register. This pulse is visible at TP9.

When power is switched on and before write current is turned on, the buffer slave flip-flops are reset and gates U7, U8, U9, and U10 are held enabled to force the state of the write amplifier flip-flops when the write current enable waveform takes the head center taps to -5 volts. After write current is turned on, the U18-A, U18-B flip-flop is reset via pin $\overline{A}$ when DATA BUSY goes false, by the output of single-shot 14SS3 (see Figure 4-14), thus returning control of these gates to the WRITE PULSE.

Data is copied into the write amplifiers by enabling gates U7, U8, U9, and U10 for 2 μseconds. This copy pulse appears on TP10 and is generated on both the positive- and negative-going edges of the WRITE PULSE waveform by gates and discrete capacitors and resistors.

The negative-going ENABLE CHECK CHARACTER (ECC) pulse resets all buffer slave flip-flops when an LRCC is required. The presence of an ENABLE FILE MARK signal and an ECC pulse sets the first four (WD0 to WD3) buffer slave flip-flops to write a File Mark character at the receipt of the following WRITE PULSE.

Note that certain nomenclature is not directly applicable to this transport. For example, EAO (pin $\overline{E}$) is actually the WRITE PULSE (WRP). This is due to the utilization of this circuit board in other PEC tape transports.

5-28. DOUBLE BUFFER, 9-CHANNEL WRITE AMPLIFIER

Refer to Schematic 100238 for this description. The Double Buffer, 9-Channel Write Amplifier has 9 channels of write electronics. Each channel is comprised of the following.

(1) Two buffer registers for temporary storage of the write data (these correspond to flip-flops 8A and 8B of Figure 4-8).

(2) A write waveform generator and a write amplifier circuit (these are combined into flip-flop 8C of Figure 4-8).

(3) Control circuits

The two data buffer registers consist of the master and slave sections of J-K flip-flops U4-A, U4-B, U5-A, U5-B, U6-A, U6-B, U7-A, U7-B. The write waveform generator is comprised of J-K flip-flops U9 through U17. The outputs of these flip-flops drive the write current amplifier transistors (Q4 through Q21). Test points 1 through 9 are connected to the write amplifier outputs.

In operation, the WRITE DATA STROBE at pin 13 triggers the 5-μsecond single-shot Q1, Q2. A 2-μsecond pulse is generated from the back edge of the single-shot and fed to power gate U21-B via inverters U25-C and U25-D. The output of U21-B is used to strobe the low-true data inputs WD0 through WDP into the master section of the buffer J-K flip-flops via AND gates U1-B, U1-C; U1-D, U1-A through U3-F, U3-E. This pulse is visible at TP10. If the data input is a "1", the corresponding master section of the flip-flop toggles.

The pulse also triggers the control loop consisting of flip-flops U20-A, U20-B and U20-D, U20-C (see flip-flops 8A and 8B in Figure 4-8), gate U24-A and R20, U19-B, R21, and U19-A, which comprise the 4-μsecond delay. A 2-μsecond shift pulse is generated by this control loop and is fed to power gate U21-A. The output of U21-A, which is visible at TP11, copies the content of the master section of the buffer flip-flops into the slave section. The WRITE PULSE from Function Control A is fed to pin $\overline{F}$. This results in a positive-going pulse ENCODER PULSE WIDE (EPW) at pin 24 and a 2-μsecond positive-going pulse ENCODER PULSE NARROW POWERFUL (EPNP) at pin 22 (visible at TP12). (Note that certain nomenclature is not directly applicable because the circuit board is utilized in other PEC tape transports.)

The EPNP pulse copies the output of the buffer flip-flops into the master sections of the write waveform generator flip-flops. EPNP is also fed to the toggle inputs (pins C, 3, 7, 10, 15, 16, 21, Y, $\overline{C}$) of these flip-flops so that at the trailing edge of EPNP, the content of the master sections of the J-K flip-flops is transferred to the slave sections. The slave outputs feed the write amplifiers. EPNP also resets flip-flop U20-D, U20-C.

The ENABLE FILE MARK and ENABLE CHECK CHARACTER waveforms are combined to produce signals at the outputs of U23-B and U24-B that correspond to PRIME for LRCC and PRIME for FM (described in Paragraph 4-27). These signals are used to reset the second stage of the buffer flip-flops for LRCC generation and those stages relevant for File Mark generation.

The WRITE CRC (WCRC) pulse on pin 28 is OR'd into the WRITE DATA STROBE channel and is used to copy CRCC into the buffer during a 9-track gapping sequence.

Flip-flops U18-A, U18-B, gates U18-C and U27-C, and inverters U19-D and U19-E are not used in Synchronous Write Tape Transports.

Two versions of the Double Buffer, 9-Channel Write Amplifier circuit board are available which are suitable for 7- and 9-track operation. The appropriate File Mark generation is selected by jumpers W1 and W2. The components within the dotted box are omitted in the 7-track version.

5-29. FUNCTION CONTROL, SYNCHRONOUS A

Refer to Schematic 100358 for this description. This circuit board provides the logic required to generate IBM-compatible gaps and special characters; also, the delays required for the COMMAND BUSY delay and the DATA BUSY signal.

Operation of the logic has already been described in Paragraph 4-27 (see Figure 4-14). The Cross Reference Chart, Table 5-2, will assist in identifying the major components in the system; however, 100 percent correspondence is not possible since Figure 4-14 is a logic diagram while the schematic shows every component.

5-30. Differentiators

A typical differentiator is designated 14d4 in Figure 4-14 and consists of components C5, R17, R18, and R19 (in Schematic 100358). R17 and R18 set the static level at the output of the differentiator at +3 volts, giving a noise immunity of 1.2 volts (typically). C5 is the differentiating input capacitor and R19 limits the current which flows when the IC input is driven below 0 volt by C5, causing the substrate diode to conduct.

Table 5-2

Function Control A
Cross Reference Chart

Figure 4-14 Reference Designations	Schematic 100358 Reference Designations
Flip-Flop 14D	U2-A, U2-B
Flip-Flop 14E	U2-C, U2-D
Flip-Flop 14F	U6-A, U6-B
Single-Shot 14SS2	Q5, Q6, Q7, Q8
Single-Shot 14SS3	Q1, Q2, Q3, Q4
Single-Shot 14SS4	Q12, Q13, Q14
Single-Shot 14SS5	Q9, Q10, Q11
Single-Shot 14SS6	Q15, Q16, Q17

5-31. Single-Shots

Single-shots 14SS4, 14SS5, and 14SS6 are conventional single-shots and are not described.

Single-shot 14SS2 (and 14SS3) operates as follows. C10 and C24 are the timing capacitors and R40 is the timing resistor. The gap time is adjusted by varying the potential (with R38) from which the capacitors start discharging. Flip-flop U6A, U6B is reset and Q5 is turned on, charging the timing capacitors to a potential defined by the resistor chain R37, R38, and R39.

When flip-flop U6-A, U6-B is set, Q5 is turned off and CR6 cut off. The capacitors discharge on an exponential toward -5 volts with time constant (C10 + C24) x (R40). Q6, Q7, and Q8 comprise a comparator whose threshold is approximately 0 volt.

Normally, Q6 and CR7 are cut off, Q7 is on, and Q8 off, so that the collector of Q8 is high. When the potential of the capacitors is approximately -0.7 volt, Q6 starts to conduct and begins to turn off Q7. Positive feedback is provided by C11 and R45 and the comparator latches. The collector of Q8 goes low, resetting flip-flop U6-A, U6-B. As a result, Q5 is turned on and the capacitors are charged to their starting potential through the 220-ohm resistor (R37). After a time which is determined by R42, R45, and C11, the comparator switches back to the quiescent state.

5-32. ECHO CHECK PARITY

Refer to Schematic 100363 for this description. This circuit board has the facilities for detecting an error during the recording process.

Information is recorded in the NRZI mode; i.e., reversal of magnetization on the tape occurs for each "1" recorded. This is accomplished by feeding current into one-half of a center-tapped recording head. The center-tap of the head is returned to -5 volts and current is supplied to the relevant half-winding from a PNP transistor connected to +5 volts through a current-defining resistor. Both the PNP transistor and current-defining resistor are located on the Double Buffer Write Amplifier circuit board.

Whenever current is switched off in one-half of the magnetic head (and switched on in the other half), the voltage at one end swings negative, relative to -5 volts, due to the inductive nature of the

recording head. The negative swings from each half of the head windings are fed to diodes CR1 and CR2, cutting off transistor Q1. A positive-going pulse is thus generated at the junction of resistors R3 and R4 for each "1" bit recorded. The typical circuits, designated 100 through 900, provide this function for each of the seven or nine heads. In a 7-track system, circuits 100 through 600 and circuit 900 are used. The positive pulses are inverted by U1-B, U1-A, etc., and fed to flip-flops U2-C, U2-D, etc., and in turn are fed to a parity-tree check system where the appropriate output of gate U13-B (even parity) or gate U17-D (odd parity) is selected by parity switch S1. If the parity is incorrect, pin 12 of AND gate U13-D is enabled.

Input ENCODER PULSE WIDE is an 8-μsecond positive-going pulse whose leading edge is used to trigger the flip-flops, located on the Double Buffer Write Amplifier circuit board, and whose negative-going edge is used to generate a positive pulse at transistor Q2. This, in turn, is fed to the interface transmitter via U13-D as the ECHO CHECK ERROR signal.

The negative-going edge of ENCODER PULSE WIDE also triggers the single-shot circuit consisting of transistors Q3 and Q4. The output of this single-shot is inverted by U9-D where the trailing edge is differentiated by capacitor C7 and inverted by transistor Q5. This pulse resets flip-flops U2-D, U2-C, etc., via inverter U9-E, OR gate U10-D and inverters U11-E and U11-C. The Echo Check Error flip-flop U13-C, U12-B is reset externally via pin $\overline{F}$ (ECR).

It is necessary to disable the Echo Check system under two circumstances. The first condition occurs when write current is switched on during the time that the transport is being brought to operational status. This could cause spurious signals to inputs 1 and 2, which could set the flip-flops prematurely. Flip-flop U12-D, U12-C prevents this situation as follows. The flip-flop is reset initially by the

GENERAL RESET signal, which disables the system by holding flip-flop U13-C, U12-B reset. When the DATA BUSY signal goes false just prior to the start of recording, the ENABLE ECHO CHECK signal (from the Function Control Synchronous A circuit board) goes true and sets flip-flop U12-D, U12-C enabling the Echo Check system.

At the end of each record, an ECHO CHECK DISABLE signal is generated which resets flip-flop U12-C, U12-D, disabling the Echo Check system until the DATA BUSY signal goes false at the beginning of the next record. This also pertains to the situation that occurs during a gapping sequence. The parity of the check characters (LRCC and CRCC) and the File Mark depends on the number of characters in the record and whether 7- or 9-track recording is being used. Therefore, it is not always the same as the data; thus, the Echo Check system must be disabled during gapping.

5-33. CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

Refer to Schematic 100264 for this description. The CRC Generator circuit board comprises the CRC register (CRCR), 22 exclusive OR gates, and two single-shots. The CRC Generator circuit board is used only in 9-channel systems. The operating procedures for generating the CRC characters (CRCC) are discussed in Paragraph 4-23. The actual mechanization of the system is as follows.

Each bit of the 9-bit character (8 plus parity) is presented to one input of each of the nine low-true AND gates (U8-B, U8-E; U8-A, U8-F; etc.). During data recording, one input of each of these gates is enabled and the output of each gate is fed to one input of each of the nine AND gates: U9-B, U9-C, U7-B, U7-C, U5-B, U5-C, U4-B, U4-C, and U2-B. The other inputs of each of these gates are enabled at this time and the outputs of these gates feed the Double Buffer Write Amplifier circuit board.

The output of gates U8-B, U8-E; U8-A, U8-F; etc., are inverted by U20-A, U20-F, etc., and the two phases of each bit of the character are fed to the first level of Exclusive OR circuits. For bits P, 0, 1, 6, and 7, the other input is from the adjacent position in the CRCR. Thus, for example, data bit P is exclusively OR'd with CRCC bit 7 by U29-C, U29-D, and U20-B, etc. For bits 2, 3, 4, and 5, two other inputs are OR'd with each data input using three-way Exclusive OR circuits. Therefore, data bit 2 is exclusively OR'd with CRCC bit 7 and with CRCC bit 1, using U31-A, U31-B, and U19-F and U26-C, U26-D, and U19-E.

The second level of Exclusive OR circuits U29-A, U29-B, and U20-C; U28-A, U28-B, and U20-D, are similar for all nine positions. The first level Exclusive OR circuit outputs form one input; the other input is from the same bit position of the CRCR. The outputs of the second level Exclusive OR circuits are each fed to one of the nine J-K flip-flops U15-A, U15-B, U14-A, U14-B, etc., which comprise the CRCR.

The WRITE DATA STROBE corresponding to each data character, is fed via OR gate U16-C, U16-A, U16-B to the single-shot, Q4, Q5, Q6, which delays the WRITE DATA STROBE 5 μseconds before it is fed to the clock input of each J-K flip-flop. This pulse can be observed at TP2. If the output of the second level Exclusive OR circuit for a particular bit is true, the J-K flip-flop for that bit is toggled by the delayed WRITE DATA STROBE. The status of each bit of the CRCR can be observed at Test Points 11, 12, 10, 8, 9, 5, 7, 3, and 4.

After the termination of data recording, the IRG or FILE GAP command is given, causing the ENABLE CRC waveform to go low. This negative-going edge is delayed approximately 10 μseconds via R1, C2, U33-A and U33-C, and used to trigger the 10-μsecond single-shot (Q1

and Q2). As a result, a 10-μsecond positive-going pulse is generated at the outputs of inverters U32-A and U33-F. This pulse disables the low-true AND gates U8-B, U8-E; U8-A, U8-F; etc., so that the nine data inputs in the first level Exclusive OR circuits are guaranteed false (i.e., "0"). The positive-going edge of the 10-μsecond pulse is OR'd into the WSC (nomenclature is not applicable to this transport — other PEC transports only) line and triggers single-shot Q4, Q5, and Q6 generating an artificial WRITE DATA STROBE, 5 μseconds later. This generates an extra shift.

The delayed ENABLE CRC waveform, which is inverted by power gate U1-B and can be observed at TP6, enables one input of each of the nine AND gates U9-A, U9-D, U7-A, U7-D, U5-A, U5-D, U4-A, U4-D, and U2-A. The other input to these gates is from the J-K flip-flops that comprise the CRCR. In this manner, the output of the CRCR is routed to the Double Buffer Write Amplifier circuit board. Note that the $\overline{Q}$ outputs of the J-K flip-flops are used, except CRC2 and CRC4 which use the Q outputs.

The negative-going edge of the 10-μsecond positive-going pulse is differentiated by R9, C5, R10, and Q3, generating a negative-going WRITE CRC pulse at the output of inverter U33-B. This pulse, observed at TP13, is used to copy the content of the CRCR into the Double Buffer (Write Amplifier) circuit board, where it is held until the appropriate WRITE PULSE causes the CRCC to be written. This pulse is generated four character spaces after the last WRITE DATA STROBE of the record by a delay circuit on the Function Control Synchronous A circuit board.

Four character spaces after the CRCC has been written, the LRCC is written. This is accomplished in the Double Buffer (Write Amplifier) circuit board by the Enable Check Character waveform which is generated on the Function Control Synchronous A circuit board. This

This information is also fed to pin 6 of the CRC Generator circuit board and inverted by U2-D. The output of U2-D is fed to power gate U10-A. The output of gate U10-A, which can be observed at TP14, resets the CRCR and is ready for CRC generation during the next record.

5-34. CIRCUIT BOARD LOCATIONS

Table 5-3 shows locations of the printed circuit boards for a standard tape transport.

5-35. SIGNAL LIST

The Glossary lists the signal abbreviations referenced in this manual and on the Schematics contained in Section VII. Unless otherwise specified, the signal description defines the status of each line in its true ("1") state.

Table 5-3

Circuit Board Locations

Circuit Board		Location
Reel Servo	100913	J201
Capstan Drive	100475	J202
Function Control — Synchronous B	100443	J203
Transmitter	100339	J204
Receiver	100334	J205
Double Buffer Write Amplifier	100234	J206
or		
Double Buffer — 9-Channel Write Amplifier *	100239	
Echo Check Parity**	100364	J207
CRC Generator *	100265	J208
Function Control — Synchronous A	100359	J209

* This circuit board is used only with 9-track transports.

** Optional

SECTION VI
MAINTENANCE AND TROUBLESHOOTING

6-1. INTRODUCTION

This section provides the information necessary to perform electrical adjustments, mechanical adjustments, maintenance, parts replacement and troubleshooting.

Section VII contains the schematic diagrams required for reference when electrical adjustments or troubleshooting are necessary.

6-2. FUSE REPLACEMENT

Line Fuse: 100- to 125-volts ac line; 3.0 amps, 3AG, slow-blow
200- to 250-volts ac line; 2.0 amps, 3AG, slow-blow

XF201: 8 amps, 3AG

XF202: 8 amps, 3AG

6-3. ELECTRICAL ADJUSTMENTS

6-4. POWER SUPPLY

6-5. Required Test Equipment

VTVM

6-6. Adjustment Procedure

NOTE

Make certain that the transport does not contain any circuit board other than J201.

(1) Depress the POWER control.

(2) Connect the VTVM to TP1 (ground on TP3) of J201, Reel Servo-B circuit board, see Schematic 100912.

(3) Adjust trimpot R36 (top) for +5 ±0.05 volts.

(4) Connect the VTVM to TP2 (ground on TP3) of J201.

(5) Adjust trimpot R37 (second from top) for -5 ±0.05 volts.

6-7. CAPSTAN SERVO

6-8. RAMP GENERATORS

Only the Synchronous Forward ramp generator is adjustable. Adjustment is only necessary if the capstan drive circuit board or one of the generator components has been replaced.

6-9. Ramp Rise and Fall Time

With a 5-Hz square wave applied to the SYNCHRONOUS FORWARD command input, set the upper trimpot so that the rise and fall times appearing on TP4 of the Capstan Drive (J202) are as specified. This single adjustment sets both the rise and fall times.

6-10. Synchronous Forward Speed

With the SYNCHRONOUS FORWARD command in the true state, set the lower trimpot on the capstan drive (J202) for the specified speed. The correct speed can be determined by reading a standard tape or examining the capstan with a stroboscope.

6-11. REEL SERVO POTENTIOMETERS

The adjustment procedures are applicable to both the take-up and supply servo potentiometers. The potentiometers are located directly behind the shaft of the respective tension arm.

6-12. Reel Servo Potentiometer Adjustment Procedure

Complete the following procedure.

(1) Using a 3/32 Allen wrench, loosen Allen screws that secure clamps to the potentiometer housing.

(2) Bring the transport to READY status.

(3) Depress the FORWARD control and keep depressed.

(4) Turn the housing of the potentiometer in the appropriate direction until the tension arm is operating in the approximate center of the slotted area of the overlay plate.

(5) Release the FORWARD control.

(6) Apply a SYNCHRONOUS FORWARD command from a pulse generator to the appropriate interface pin (refer to Paragraph 1-7 for the required pulse specification and to Table 2-1 for the appropriate SYNCHRONOUS FORWARD command interface pin).

(7) Set the pulse generator to approximately 5 Hz.

(8) With a full supply reel, ensure that the transport operates satisfactorily.

(9) Run forward until the take-up reel is nearly full.

(10) With a full take-up reel, ensure that the transport operates satisfactorily when a SYNCHRONOUS FORWARD command is applied at approximately 5 Hz.

(11) Momentarily depress the REWIND control.

(12) If the transport operates in the Rewind mode, switch the POWER switch off and tighten the Allen screws that secure the clamps to the potentiometer housing. If the transport does not operate in the Rewind mode, continue to step (13).

(13) Turn the housing of the take-up potentiometer 1 or 2 degrees in the counterclockwise direction.

(14) Bring the transport to READY status.

(15) Repeat steps (12) through (15) until the transport operates in the Rewind mode.

6-13. BOT PHOTOSENSOR AMPLIFIER

6-14. Required Test Equipment

Multimeter.

6-15. Adjustment Procedure

Complete the following procedure.

(1) Apply power to the transport.

(2) Making certain the BOT tab is not over the photosensor, connect the multimeter to TP1 of J203 (Function Control B circuit board, see Schematic 100442).

(3) Adjust trimpot R15 (top) for +3 volts.

(4) Bring the BOT tab over the photosensor.

(5) Voltage should drop to less than +0.4 volt.

6-16. EOT PHOTOSENSOR AMPLIFIER

Adjustment of the EOT Photosensor Amplifier is identical to the BOT adjustment, except that voltage is measured at TP2 and adjusted by trimpot R30 (second from top).

6-17. MOTION COMMAND AND CHECK CHARACTER DELAY ADJUSTMENTS

These delays are provided by single-shot circuits contained on the Function Control Synchronous A circuit board (see Schematic 100358).

The SYNCHRONOUS FORWARD command is applied to the appropriate interface pin (refer to Paragraph 1-7 for the required pulse specification and to Table 2-1 for the SYNCHRONOUS FORWARD command interface pin).

6-18. Required Test Equipment

Pulse Generator (100 Hz).

Oscilloscope.

6-19. Command Busy Delay

Complete the following procedure.

(1) Apply SYNCHRONOUS FORWARD commands at a rate of approximately 100 Hz.

(2) Synchronize the oscilloscope on the trailing edge of the SYNCHRONOUS FORWARD command.

(3) Monitor TP8.

(4) Adjust trimpot R38 (fifth from the top) so that the positive pulse width is:

Stop Time + (5 to 10) milliseconds.

(See Paragraph 6-9 for stop time.)

6-20. Write Pulse Delay

Complete the following procedure.

(1) Apply SYNCHRONOUS FORWARD commands at a rate of approximately 100 Hz.

(2) Apply WRITE DATA STROBES at a rate of:

$$D \times V \text{ Hz}$$

where

D is bit density in bpi

V is tape speed in ips

(3) Synchronize the oscilloscope on the leading edge of the WRITE DATA STROBE.

(4) Monitor TP6.

(5) Adjust trimpot R48 (third from top) so that the leading edge of the negative-going WRITE PULSE is delayed in the range of 15 to 20 μseconds from the WRITE DATA STROBE.

6-21. LRCC Delay

Complete the following procedure.

(1) Apply SYNCHRONOUS FORWARD commands at a rate of approximately 100 Hz.

(2) Synchronize the oscilloscope on the trailing edge of the SYNCHRONOUS FORWARD command.

(3) Monitor TP4.

(4) Adjust trimpot R61 (second from top) so that the negative-going ENABLE CHECK CHARACTER pulse is delayed four character spaces for a 7-track system or eight character spaces for a 9-track system, after the termination of the SYNCHRONOUS FORWARD command. A character space is:

$$\frac{1}{DV}$$

where

D is bit density in bpi

V is tape speed in ips

For example, one character space equals 50 μseconds for an 800 bpi, 25 ips system.

6-22. CRC Delay (9-track systems only)

Complete the following procedure.

(1) Apply SYNCHRONOUS FORWARD commands at a rate of approximately 100 Hz.

(2) Synchronize the oscilloscope on the trailing edge of the SYNCHRONOUS FORWARD command.

(3) Monitor TP3.

(4) Adjust trimpot R72 (top) so that the negative-going ENABLE CRC pulse is delayed four character spaces after the termination of the SYNCHRONOUS FORWARD command. A character space is defined in Paragraph 6-21.

6-23. Data Busy Delay

Complete the following procedure.

(1) Apply SYNCHRONOUS FORWARD commands at a rate of approximately 100 Hz.

(2) Synchronize the oscilloscope on the leading edge of the SYNCHRONOUS FORWARD command.

(3) Monitor TP7.

(4) Adjust trimpot R28 (fourth from the top) so that the positive pulse width (in milliseconds) is:

$$\frac{IRG}{V}$$

where

IRG = 0.75 inch for a 7-track system, or

IRG = 0.60 inch for a 9-track system

V is tape speed in ips

For example, 24 milliseconds for 9-track, 25 ips systems.

6-24. MECHANICAL ADJUSTMENTS

6-25. REEL SERVO BELT TENSION

The belts should not be over-tightened, since low motor bearing life and over-heating might result. Tension is applied by loosening the four screws that retain the reel motor, moving the motor until the belt is at the required tension, and tightening the screws. The proper tension will be applied when the following is established. With a steel scale placed on the belt, extending across the two pulleys, the belt deflection should be 3/8 ±1/8 inch when a 1/2-pound force is applied midway between the pulleys.

6-26. TAPE PATH GUIDE ALIGNMENT

All tape guiding elements in the tape path are referenced to the outer edge of the head guides. It is assumed that the tension-arm spring tension has been set up as described in Paragraph 6-32.

6-27. Fixed Guides

With the trim removed, measure the distance to the outer tape-guiding edge of each head guide from the tape deck. These measurements will normally be within 0.001 inch of each other. Measure the distance from tape deck to the outer tape-guiding edge of the supply and take-up fixed guides. Shim the guides between the guide post and roller to within 0.002 inch of the head guide dimensions. This places the outer edge of all fixed guides the same distance from the tape deck.

6-28. Tension Arm Guides

With the trim removed from the deck, the tension arms should be rotated so that the tape guides are as nearly as possible perpendicular to the tape deck and secured. The reel retainer hubs should be positioned so that the reel locating edge is located 0.625 ±0.005 inch from the tape deck. Secure the reel retainer hubs with the two set screws on the shaft flats.

6-29. Supply Tension Arm Guide

Remove the head retaining screws and move the head from between the head guides. Place a 6-inch steel scale across the head guides as shown in Figure 6-1. The scale should preferably be narrower than 1/2 inch so that it can easily be held against the outer edges of the guides at A and B. The tension-arm guide-shaft set screw is loosened and the guide positioned so that the outer edge lines up with the scale. Secure the guide-shaft set screw and replace the head.

6-30. Take-up Tension Arm Guide

Place a 6-inch steel scale across the fixed guides as shown in Figure 6-2. The scale should be held against the outer edge of the guides. Rotate the take-up tension arm counterclockwise until the roller contacts the guide. Move the guide so that the outer edge lines up with the scale. Secure the guide-shaft set screw.

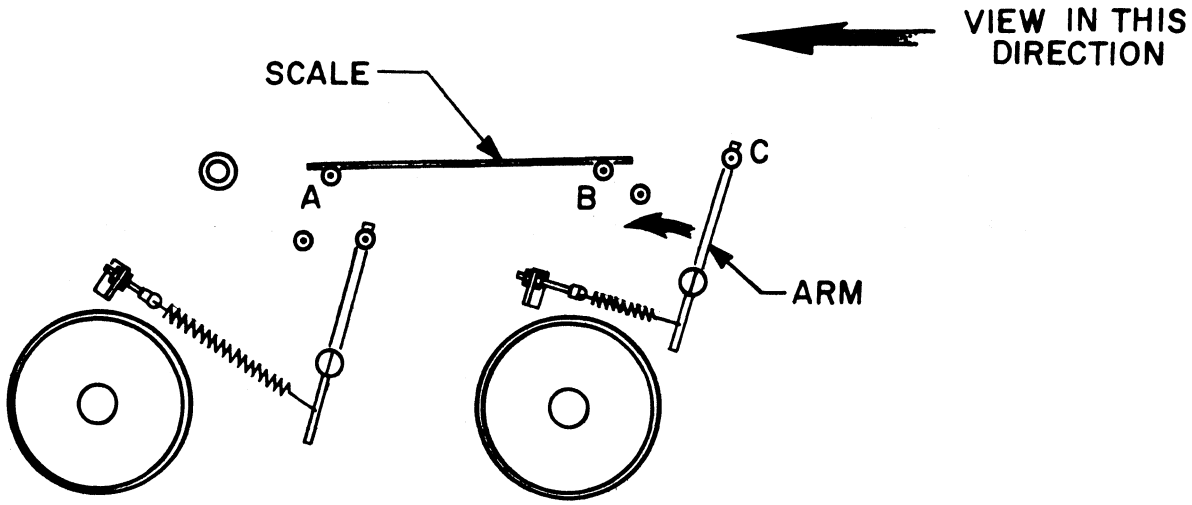


Figure 6-1. Supply Tension Arm Guide Adjustment

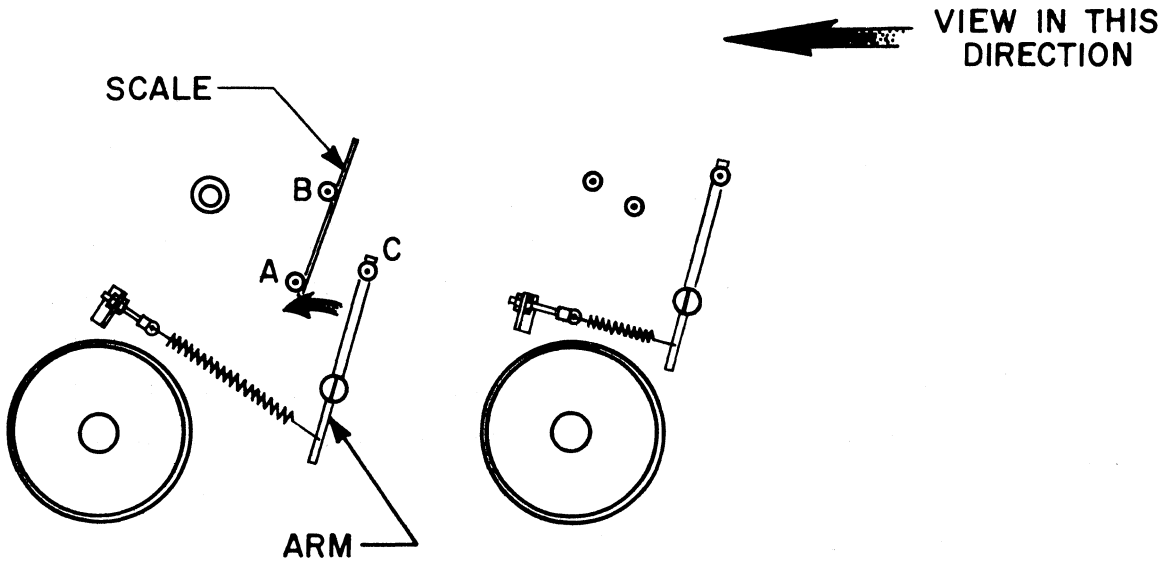


Figure 6-2. Take-up Tension Arm Guide Adjustment

6-31. Guide Perpendicularity

The head is replaced and the tape threaded in the normal tape path. Power is turned on and the final adjustment is made to the tension arm guide perpendicularity by running the tape and noting the tension arm rollers. When the guides are perpendicular, the tape has an even tension across the guide with no buckling at the flanges. After adjustment, secure tension arm securely to ensure that there is no rotation during operation.

CAUTION

USE EXTREME CARE TO AVOID CONTACT WITH THE HEAD AND GUIDES WHEN REPLACING THE TRIM.

6-32. TAPE TENSION

6-33. Supply Tension Arm

With the trim removed from the deck, thread a loop of tape as shown in Figure 6-3. Using a force gauge, measure the force required to pull the tension arm off its backstop and slowly through its stroke. The force required should not vary by more than a total of 0.3 ounce as the motion of the arm is slowly reversed at any part of the stroke. Adjust the spring tension screw (A) until the average force (as measured) is 8 ounces. Tighten the lock nuts.

6-34. Take-Up Tension Arm

Thread the tape as shown in Figure 6-4. Using a force gauge, measure the force required to pull the tension arm off the backstop and slowly through its stroke. The force required should not vary by more than a total of 0.3 ounce as the motion of the arm is slowly reversed at any point of the stroke. Adjust the spring tension screw (A) until the

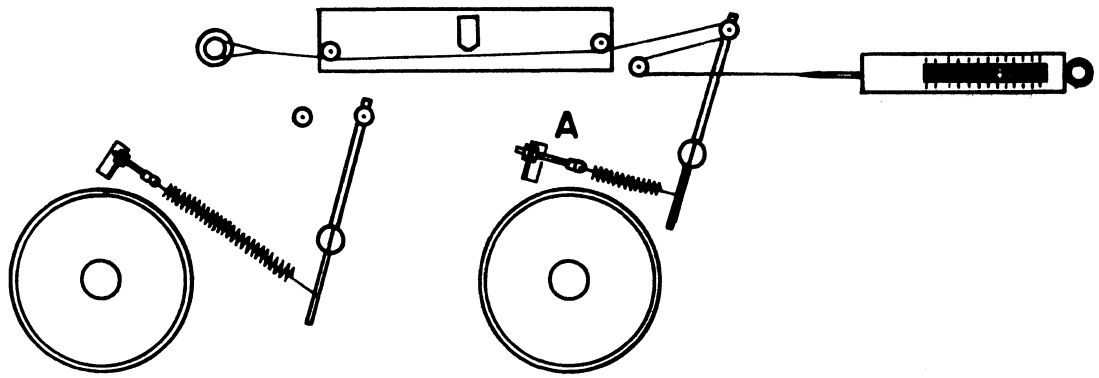


Figure 6-3. Supply Tension Spring Measurement

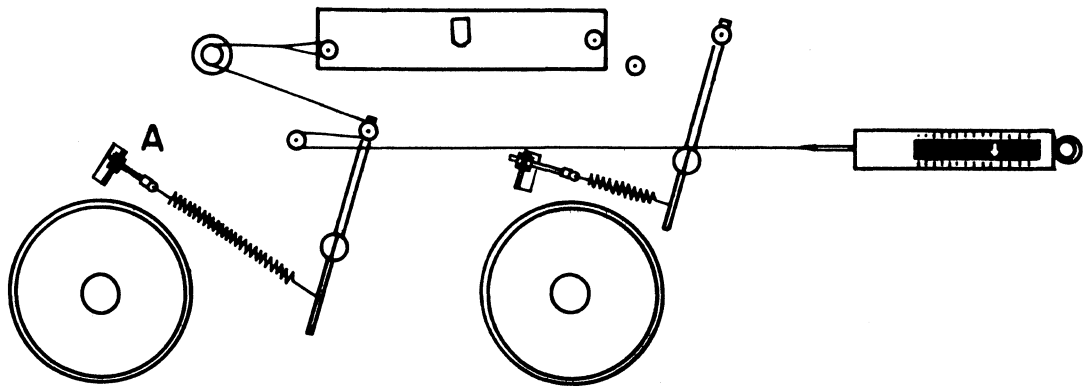


Figure 6-4. Take-up Tension Spring Measurement

average force as measured above is 8 ounces. Tighten the lock nuts. Tension should be adjusted with the transport oriented in the direction of intended use.

6-35. Limit Switch (Take-Up Tension Arm)

In normal operation this switch is closed, shorting the inputs, When the take-up tension arm is resting on its backstop or at the other end of its stroke, the switch should be open, which indicates that the tension arm is out of the normal operating region. The cam on the tension arm shaft should be positioned so that the switch roller has moved enough to open the switch just before the tension arm contacts the backstop. A pin prevents the switch roller from contacting the cam surface when the tension arm is in the normal operating area. The oversize mounting holes for the switch are used to position the switch so that it is positively closed in the normal operating region and is opened before the arm reaches the limits of its stroke. Care should be taken to see that the cam does not contact the roller in a line drawn along the lever and through the center of the roller.

6-36. MECHANICAL MAINTENANCE

The tape transport is designed to operate with a minimum of maintenance and adjustments. Replacement of parts is designed to be as simple as possible. Repair equipment needed is kept to a minimum and only simple tools are required in most cases. Paragraph 6-39 lists the tools required to maintain the tape transport.

6-37. PREVENTIVE MAINTENANCE SCHEDULE

To assume that the transport operates at its optimum design potential and to assure long life, a program of planned preventive maintenance is recommended. A suitable schedule is shown in Table 6-1.

Table 6-1

Preventive Maintenance Schedule

Maintenance Operation	Frequency (hours)	Quantity to Maintain	Time Required (minutes)	Manual Paragraph Reference
Clean Transport	16 (or end of operating day)	–	5	6-38
Check Roller Guides	While cleaning	4	3	6-38
Check Capstan Surface	While cleaning	1	2	6-38
Check Tape Tracking	200		5	6-36
Check Tape Tension	500		15	6-32
Replace Reel Motor	15,000	2	10	–
Replace Capstan Drive Assembly	20,000	1	10	–
Check Head Wear	5,000	1	3	–

6-38. CLEANING THE TRANSPORT

The transport requires cleaning in three major areas: head and associated guides, capstan, and Delrin roller guides.

To clean the head and associated guides, use a lint-free cloth or cotton swab moistened in isopropyl alcohol. Wipe the head carefully to remove all accumulated oxide and dirt.

CAUTION

ROUGH OR ABRASIVE CLOTHS SHOULD NOT BE USED TO CLEAN THE HEAD AND HEAD GUIDES. USE ONLY ISOPROPYL ALCOHOL. OTHER SOLVENTS, SUCH AS CARBON TETRACHLORIDE, MAY RESULT IN DAMAGE TO THE HEAD LAMINATION ADHESIVE.

To clean the capstan, use only a cotton swab moistened with isopropyl alcohol to remove accumulated oxide and dirt.

To clean the Delrin roller guides, use a lint-free cloth or cotton swab moistened in isopropyl alcohol. Wipe the guide surfaces carefully to remove all accumulated oxide and dirt.

CAUTION

DO NOT SOAK THE GUIDES WITH EXCESSIVE SOLVENT. EXCESSIVE SOLVENT MAY SEEP INTO THE PRECISION GUIDE BEARINGS, CAUSING CONTAMINATION AND A BREAKDOWN OF THE BEARING LUBRICANT.

6-39. MAINTENANCE TOOLS

The following list of tools is required to maintain the tape transport.

(1) Socket wrench set for 4-40, 10-32 cap screws.

(2) Socket wrench set for 4-40, 6-32, 10-32 set screws.

(3) Splined socket wrenches for 4-40, 6-40, set screws

(4) Open end wrenches for 3/16-, 1/4-, 5/16-, and 3/8-inch bolts.

(5) Long-nose pliers.

(6) Phillips screwdriver set.

(7) Standard screwdriver set.

(8) Soldering aid.

(9) Soldering iron.

(10) One-pound force gauge.

(11) Lint-free cloth.

(12) Cotton swabs.

(13) Isopropyl alcohol.

6-40. TROUBLESHOOTING

Table 6-2, System Troubleshooting chart, provides a means of isolating faults, the possible causes, and the remedies. Table 6-2 is used in conjunction with the schematic, assembly drawings, and wiring diagrams listed in Section VII.

Table 6-2

System Troubleshooting

Symptom	Probable Cause	Remedy	Reference
Tape does not tension and capstan shaft rotates freely when LOAD FORWARD is depressed for the first time.	Interlock relay K201 does not close.	Check operation of relay. Replace if necessary.	Schematic 100388
	LOAD FORWARD switch S103 not operative.	Check operation of switch. Replace if necessary.	Schematic 100388
	Relay Driver defective.	With power on, check for a maximum of 0.5 volt at pin E. If greater, replace defective delay driver component.	Schematic 100474
Tape tension is present when LOAD FORWARD control is depressed, but is removed when control is released.	Limit switch S101 not operative.	Replace switch if defective.	Schematic 100388
	Limit switch S101 not adjusted properly.	Adjust switch.	Paragraph 6-35
Tape runs away when LOAD FORWARD control is depressed or tape speed is excessive.	Fuse XF202 blown.	Replace fuse.	Paragraph 6-2
	No tachometer feedback.	Check resistance between pins 7 and 8 of TB301 for approximately 150 ohms. Replace entire capstan assembly if tachometer is defective.	Schematic 100388
		Check ramp generator for proper output. Replace defective component.	Schematic 100474

Table 6-2 (continued)

Symptom	Probable Cause	Remedy	Reference
Tape unwinds or tension arm hits stops when LOAD FORWARD control is depressed.	Tape improperly threaded.	Rethread tape.	Paragraph 3-29
	No +5 volts at pin 4 of J201.	Repair or replace Reel Servo circuit board.	Schematic 100912
Tape continues to run when BOT tab reaches photosensor.	BOT tab dirty or tarnished.	Replace tab or increase sensitivity of photo tab amplifier.	Paragraph 6-15
	Photosensor not properly adjusted.	Adjust photosensor.	Paragraph 6-15
	Photosensor or amplifier defective.	Check for +3 volts at pin D of J203 with tab not over photosensor. Repair or replace defective parts.	Schematic 100442 Paragraph 6-15
Transport does not move in response to SYNCHRONOUS FORWARD commands.	Interface cable fault or receiver fault.	Check relevant receiver test point.	
	Fault on Capstan Drive card.	Check TP4, J202.	Schematic 100474

Table 6-2 (continued)

Symptom	Probable Cause	Remedy	Reference
Parity is written incorrectly.	Parity generator switch set incorrectly on Receiver circuit board.	Set switch to correct position.	Schematic 100333 Paragraph 5-25.
CRC and/or LRC check characters spacing incorrect.	Single-shot timings maladjusted.	Adjust trimpot R61 and/or R72 on Function Control Synchronous A circuit board.	Schematic 100358 Paragraphs 6-21 and 6-22
IRG distance too short or too long.	Data Busy single-shot maladjusted.	Adjust trimpot R28 on Function Control Synchronous A circuit board.	Schematic 100358 Paragraph 6-23
	Last WDS of record not coincident with termination of SFC.	Correct interface timing.	Paragraph 3-10

SECTION VII

SCHEMATICS, PART LISTS, AND WIRING DIAGRAMS

7-1. INTRODUCTION

Printed circuit board schematics, assembly drawings, and wiring diagrams are included in this section and are collated in the same order shown in Table 7-1.

Table 7-2, Part Number Cross Reference, provides a cross reference to the manufacturer's part numbers from PEC part numbers.

Table 7-1

List of Schematics

Description	Schematic Number	Assembly Number
Reel Servo and Voltage Regulator	100912	100913
Capstan Drive	100474	100475
Function Control, Synchronous B	100442	100443
Function Control, Synchronous A	100358	100359
Transmitter, DTL	100338	100339
Receiver, DTL	100333	100334
Double Buffer Write Amplifier	100233	100234
Double Buffer - 9 Channel Write Amplifier	100238	100239
Echo Check Parity	100363	100364
CRC Generator	100264	100265
Wiring Diagram — 9-Track	101200	
Wiring Diagram — 7-Track	101201	
Power and Harness Wiring Diagram	100388	

Table 7-2

Part Number Cross Reference

PEC Part Number	Manufacturer (or equivalent)	Description or Part Number*
Carbon Comp. Resistors		
101 - 1525	Allen Bradley, Stancor	RC20 (1500 ohms, 5%, 1/2 watt)
102 - 1525		RC32 (1500 ohms, 5%, 1 watt)
107 - 1525		RC42 (1500 ohms, 5%, 2 watts)
Precision Resistor		
104 - 2612	Corning, IRC	RL20C, (26,100 ohms, 1%, 1/4 watt)
Variable Resistors		
121 - 1010	Beckman Helipot	79PR100, (100 ohms, 10%, 3/4 watt)
121 - 1020		79PR1K, (1000 ohms, 10%, 3/4 watt)
Dipped Mica Capacitors		
130 - 1515	El Menco	CM05CJ03 (150 picofarads, 500 volts, 5%)
Mylar Capacitors		
131 - 1540	Cornell - Dubilier	WMF1P15 (0.15 μfarads, 100 volts, 10%)
Solid Tantalum Capacitors		
132 - 2752	Kemet	TK2R7W35 (2.7 μfarads, 35 volts, 20%)
Aluminum Electrolytic Capacitors		
133 - 7060	Mallory	MTA70E20 (70 μfarads, 20 volts -10 +100%)

*For resistors and capacitors typical part numbers only are shown.

Table 7-2

Part Number Cross Reference (Continued)

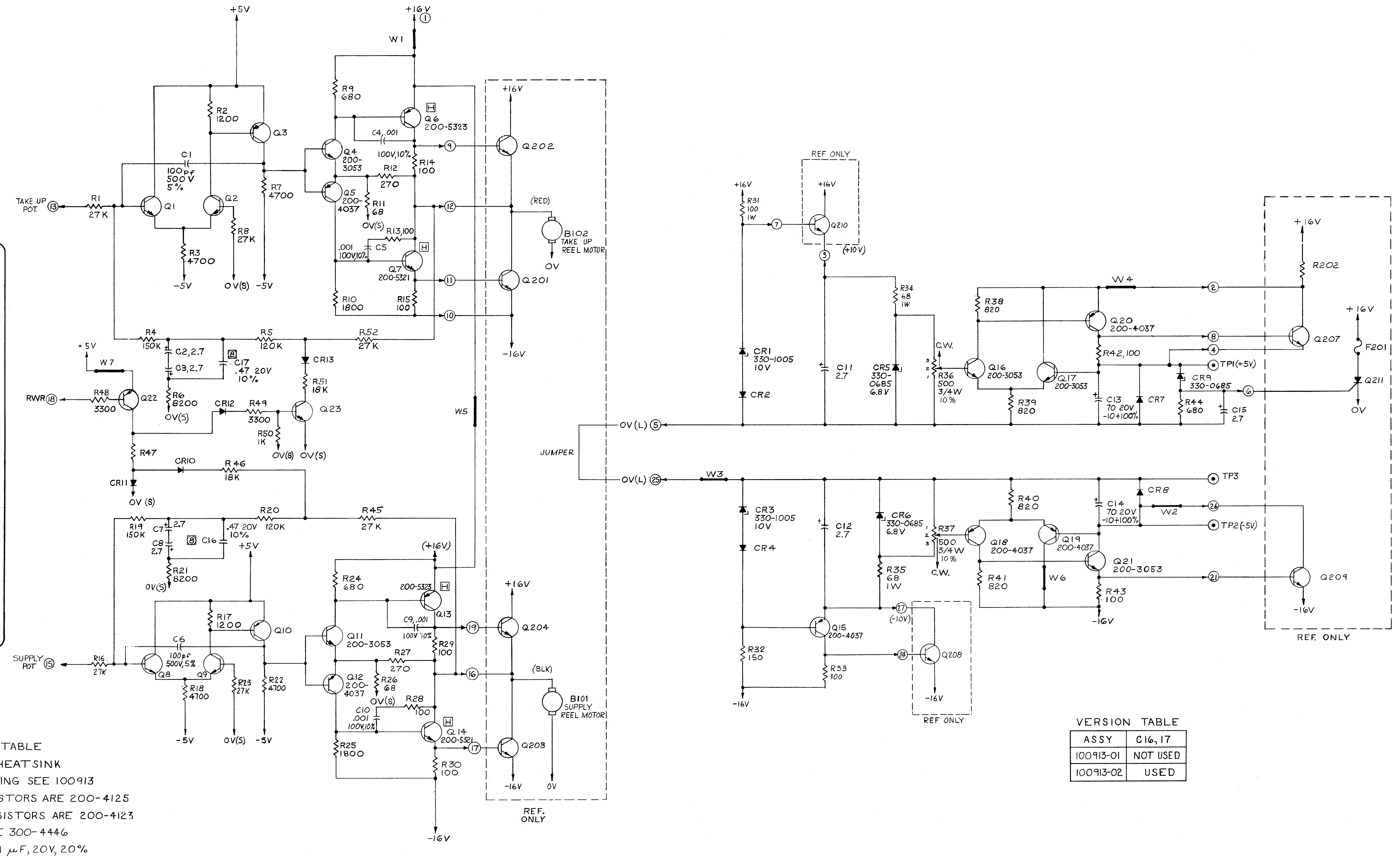
PEC Part Number	Manufacturer (or equivalent)	Description or Part Number
Transistors		
200 - 4123	Motorola	2N4123 (NPN switching)
200 - 4125	Motorola	2N4125 (PNP switching)
200 - 3053	RCA	2N3053 (NPN, T05, medium power)
200 - 5321	RCA	2N5321 (NPN, T05, medium power)
200 - 4037	RCA	2N4037 (PNP, T05, medium power)
200 - 5323	RCA	2N5323 (PNP, T05, medium power)
200 - 3771	RCA	2N3771 (NPN, T03, power)
200 - 3055	RCA	2N3055 (NPN, T03, power)
Diodes		
300 - 4446	TI	1N4446 (logic diode)
Rectifier Bridge		
320 - 9622	Motorola	MDA 962-2 (100 volts, 10 amps)
Zener Diodes		
330 - 0685	Motorola	1N4736A (6.8 volts, 5%)
330 - 1005	Motorola	1N4740A (10 volts, 5%)
OP Amplifier		
400 - 1435	Motorola	MC1435P

Table 7-2

Part Number Cross Reference (Continued)

PEC Part Number	Manufacturer (or equivalent)	Description or Part Number
Digital IC		
700 - 8360	Fairchild	U6A993659
700 - 8440	Fairchild	U6A994459
700 - 8450	Fairchild	U6A994559
700 - 8460	Fairchild	U6A994659
700 - 8520	Fairchild	U6A909959

REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ECN 633 (REDRAWN)				



Pin		Signal
A	1	+16V
B	2	PWR. SUP. COL. (+5)
C	3	+10V
D	4	+5V
E	5	OV (L)
F	6	O/V OUTPUT
H	7	PWR. SUP. BASE (+10)
J	8	PWR. SUP. BASE (+5)
K	9	T. U. BASE (POS.)
L	10	T. U. EMIT. (NEG.)
M	11	T. U. BASE (NEG)
N	12	T.U. OUTPUT
P	13	T.U. POT.
R	14	OV (S)
S	15	SUP. POT.
T	16	SUP. OUTPUT
U	17	SUP. BASE (NEG.)
V	18	RWR
W	19	SUP. BASE (POS.)
X	20	
Y	21	PWR. SUP. BASE (-5)
Z	22	
Ā	23	
B̄	24	PWR. SUP. BASE (-10)
C̄	25	OV (L)
D̄	26	-5V
Ē	27	-10V
F̄	28	-16V

VERSION TABLE

ASSY	C16, 17
100913-01	NOT USED
100913-02	USED

8. SEE VERSION TABLE
7. H INDICATES HEATSINK
6. FOR ASSY DRAWING SEE 100913
5. ALL PNP TRANSISTORS ARE 200-4125
4. ALL NPN TRANSISTORS ARE 200-4123
3. ALL DIODES ARE 300-4446
2. ALL CAPACITORS IN μF, 20V, 20%
1. ALL RESISTORS IN OHMS, ±5%, 1/2 WATT.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010, ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS

DR J. CITINO

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC: REEL SERVO 'B'

NEXT ASSY	USED ON
100913	TOP ASSY

APPLICATION

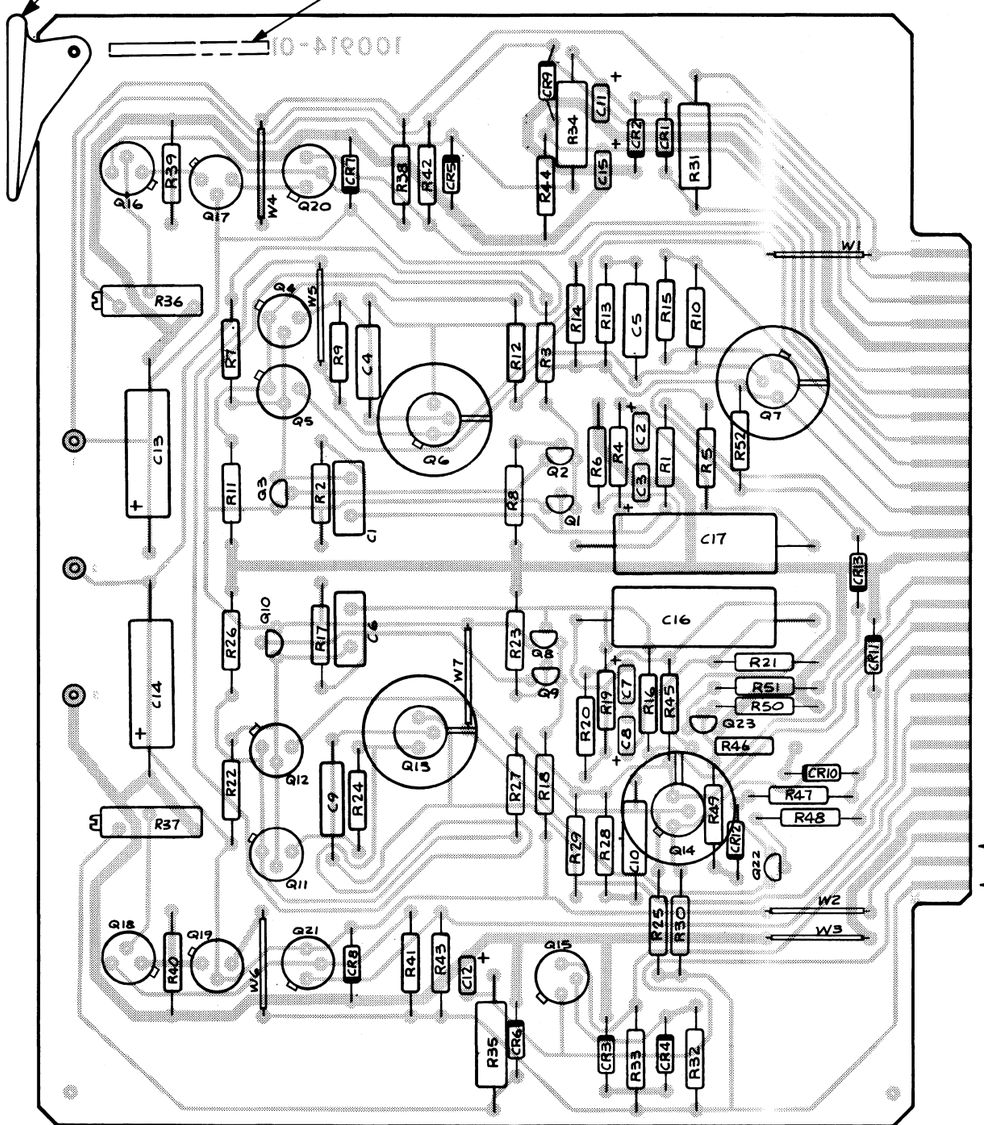
SIZE D | DWG NO. 100912 | REV B

SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN-1-WD				
B	ECN 628				
C	ECN 770, REVISED & REDRAWN				

651-6100

3



100914-01

4 TABLE I

PART NO.	REF DESIGNATION
200-4123	Q1,2,8,9,23
200-4125	Q3,10,22
200-3053	Q4,11,21,16,17
200-4037	Q5,12,15,18,19,20
200-5321	Q7,14
200-5323	Q6,13
300-4446	CR2,4,7,8,10,11,12,13
330-0685	CR5,6,9
330-1005	CR1,3
130-1015	C1,6
131-1020	C4,5,9,10
132-2752	C2,3,7,8,11,12,15
133-7060	C13,14
101-6805	R11,26
101-1015	R13,14,15,28,29,30,33,42,43
101-1516	R32
101-2715	R12,27
101-6815	R9,24,44
101-8215	R38,39,40,41
101-1025	R50
101-1225	R2,17
101-1825	R10,25
101-3325	R47,48,49
101-4725	R3,7,18,22
101-8225	R6,21
101-1835	R46,51
101-2735	R1,8,16,23,45,52
101-1245	R5,20
101-1545	R4,19
102-6805	R34,35
102-1015	R31
121-5010	R36,37
100373-01	W1-7
650-2230	Q6,7,13,14
668-7717	Q4,5,6,7,11,12,13,14,15,16,17, 18,19,20,21

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09
C16,17	—	131-4140							

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO SEE TABLE II.

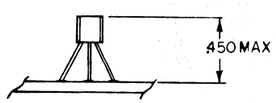
4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100912
SPECIFICATION-100916

NOTES: UNLESS OTHERWISE SPECIFIED



VIEW A-A

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± ½°
.XXX ± .005
X ± 1/32
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES	DATE
DR G. FICKEN	4/3/69
CHK W. KORP	4/4/69
DES	
ENGR TCP	4/17/69
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA
REEL SERVO AND
VOLTAGE REGULATOR-B

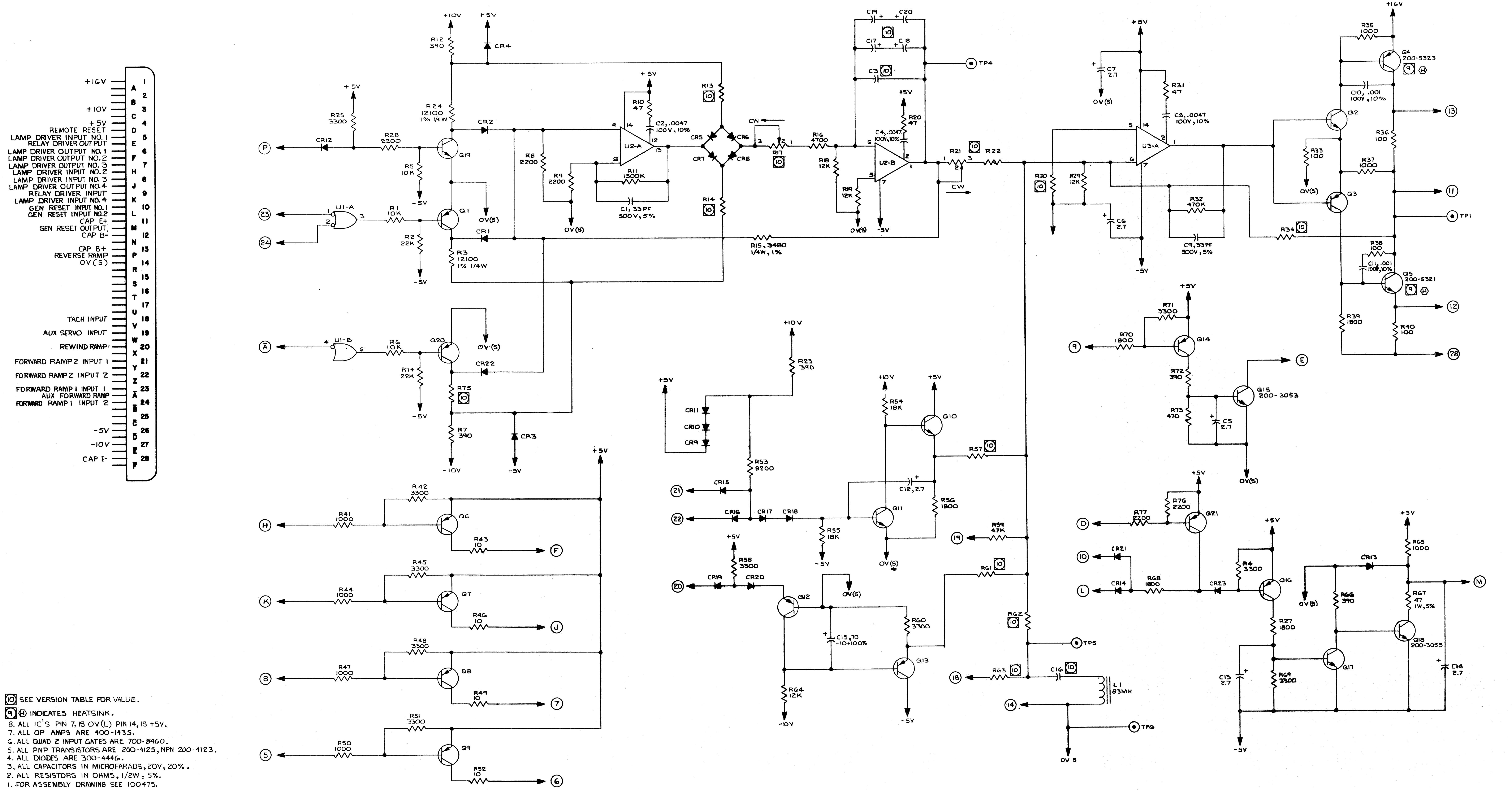
TOP ASSY	
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:

MATL:

SIZE D | CODE IDENT. NO. | DWG NO. 100913 | REV C

SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1



(10) SEE VERSION TABLE FOR VALUE.

(9) (H) INDICATES HEATSINK.

8. ALL IC'S PIN 7, IS OV(L) PIN 14, IS +5V.
7. ALL OP AMPS ARE 400-1435.
6. ALL QUAD 2 INPUT GATES ARE 700-8460.
5. ALL PNP TRANSISTORS ARE 200-4125, NPN 200-4123.
4. ALL DIODES ARE 300-4446.
3. ALL CAPACITORS IN MICROFARADS, 20V, 20%.
2. ALL RESISTORS IN OHMS, 1/2W, 5%.
1. FOR ASSEMBLY DRAWING SEE 100475.

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPD
L	REVISED AND REDRAWN ECN 527	[illegible]	J.T.	[illegible]	[illegible]
M	ECN 587	[illegible]	[illegible]	WK	[illegible]
N	ECN 630	[illegible]	JV	WK	[illegible]
P	ECN 667	5/9/[illegible]	J.C.	WK	[illegible]
R	ECN 735	5/24/[illegible]	J.G.	WK	[illegible]
S	ECN 954	[illegible]	J.C	WK	[illegible]

REFERENCE DESIGNATORS

LAST USED	DELETED
R77	R26
C20	
CR23	
Q21	
U3	
L1	
TPG	TP2,3

VERSION TABLE

MACHINE TYPE	CAPSTAN DIA	SPEED IPS	ASS'Y 100475	R13	R14	R17 3/4W,10%	R21 3/4W,10%	R22 1/4W 1%	R30	R34	R57	R61	R75 1/4W 1%	C3 100V,10%	C16 100V,10%	C17 & C18 20%	C19 & C20 20%	R62 1/4W 1%	R63 1/4W 1%
READ ONLY OR WRITE ONLY	.56	1.5	-01	56K		50K	10K	26100	1800	220K	12K	1800	NOT USED	.33	.033	NOT USED	NOT USED	3480	3160
READ ONLY OR WRITE ONLY	.80	20	-02	150K		↑	1K	2610	1800	220K	18K	2700	↑	↑	.033	↑	↑	↑	↑
READ AND WRITE	1.60	25	-03	180K			5K	4220	2200	220K	33K	5600		↓	.033				
READ ONLY OR WRITE ONLY	.80	25	-04	180K			1K	2150	2200	82K	18K	2700	↓	.33	.047				
READ ONLY OR WRITE ONLY	.80	25 & 11	-05	100K			1K	2150	2200	82K	18K	2700	26100	.15	.047	↓			
READ ONLY OR WRITE ONLY	.40	.55	-06	56K			50K	38300	1800	220K	10K	1800	↑	.33	.033	NOT USED			
READ AND WRITE	.80	10	-07	82K			5K	4220	↑	220K	18K	2700		NOT USED	↑	2.7uf 35V			
READ ONLY OR WRITE ONLY	.80	5	-08	180K			10K	8250		↑	↑	↑		.33		NOT USED			
READ ONLY OR WRITE ONLY	.80	15	-09	180K			10K	2150	↓	↓	↓	↓	↓	.33		NOT USED			
READ AND WRITE	.80	12.5	-10	56K		↓	5K	4220	1800	220K	18K	2700	NOT USED	NOT USED		2.7uf 35V			
READ ONLY OR WRITE ONLY	1.60	25 & 11	-11	121K 1/4W 1%		50K	1K	4220	2200	120K	33K	5600	26100	.15		NOT USED	↓		
READ AND WRITE	.80	15	-12	68100 1/4W 1%		20K	5K	3160	1800	220K	18K	2700	NOT USED	NOT USED		2.7uf 35V	NOT USED		
READ AND WRITE	.80	5	-13	90900 1/4W 1%		50K	5K	10K	↑	↑	18K	2700	↑	↑		↑	2.7uf 35V		
READ AND WRITE	.56	4	-14	110K 1/4W 1%		50K	5K	8250	↓	↓	12K	1800	↓	↓	↓	↓	↕	↓	↓
READ ONLY OR WRITE ONLY	.56	<4-1.5	-15	12100 1/4W 1%		20K	20K	8250	1800	220K	12K	1800	NOT USED	NOT USED	.033	2.7uf 35V	2.7uf 35V	3480	3160
READ ONLY OR WRITE ONLY	.56	25 & 2.5	-16	196K 1/4W 1%	2.87K 1/4W 1%	50K	1K	2870	2200	220K	22K	3900	121K	.47	.033	NOT USED	NOT USED	6810	6190
READ ONLY OR WRITE ONLY	.80	25	-17	68100 1/4W 1%		20K	1K	1960	1800	150K	18K	2700	NOT USED	NOT USED	.033	2.7uf 35V	NOT USED	3480	3160

100475	TOP ASSY
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

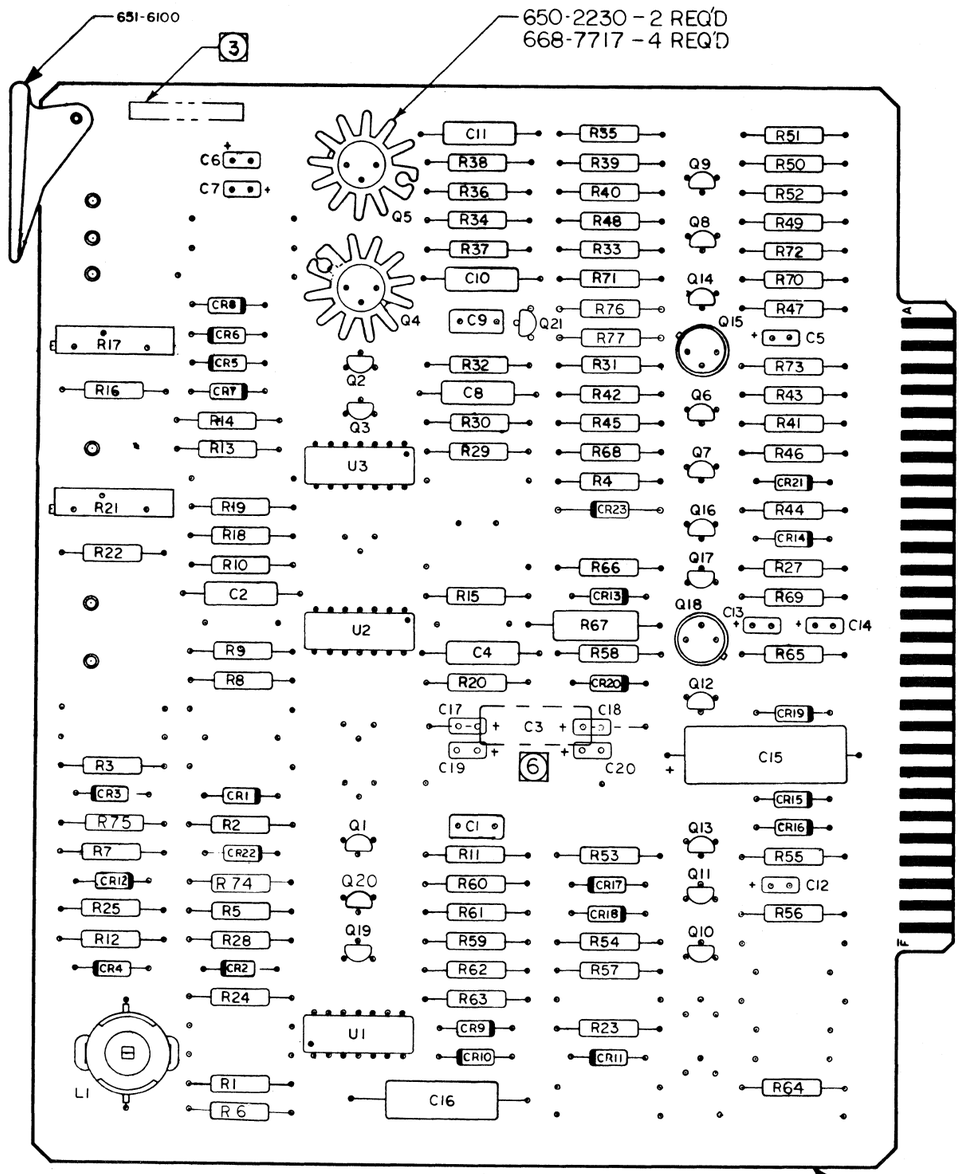
MATL:

SIGNATURES	DATE
DR J.R. THOMPSON	[illegible]
CHK	
DES	
ENGR [illegible]	[illegible]
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE
SCHEMATIC-CAPSTAN DRIVE SYNCHRONOUS

SIZE H | DWG NO. 100474 | REV S
SCALE — DO NOT SCALE DWG | SHEET OF



5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

3 RUBBER STAMP PART NO., INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100474
SPEC-100476

6 FOR APPLICABLE CAPACITORS SEE VERSION TABLE II

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
S	ECN 954	8/26/69	JC		

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
L	ECN 523	3/5/69	J.T.		TCL
M	ECN 587	3/28/69	J.T.		
N	ECN 630	4/14/69	SWm	WK	
P	ECN667	5/9/69	J.C.	WK	
R	ECN 735	5/26/69	J.C.		

4 TABLE I

PART NO.	REF. DESIGNATION
200-4123	Q2,10,11,17, 19
200-4125	Q3,6,7,8,9,12,13,14,16,1,20,21
200-3053	Q15,18
200-5323	Q4
300-4446	CR1-23
130-3305	C1,9
131-1020	C10,11
131-4720	C2,4,8
132-2752	C6,7,12,5,13,14
133-7060	C15
200-5321	Q5
101-1005	R43,46,49,52
101-4705	R20,31,10
101-1015	R33,36,38, 40
101-3915	R7, 12,23,72,66
101-4715	R73
101-1025	R35,37,41,44,47, 50,65
101-1825	R39,56,70,68,27
101-2225	R8,9,28,76, 77
101-3325	R42,45,48,51,58,60,25, 71,4,69
101-4725	R16
101-8225	R53
101-1035	R1,5,6
101-1235	R18,19,29,64
101-1835	R54,55
101-2235	R2,74
101-4735	R59
104-3481	R15
104-1212	R3,24
101-1555	R11
102-4705	R67
400-1435	U2,3
101-4745	R32
700-8460	U1
100212-01	L1

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
TYPE	WRITE OR READ ONLY	WRITE OR READ ONLY	WRITE AND READ	WRITE OR READ ONLY	WRITE OR READ ONLY	WRITE OR READ ONLY	WRITE AND READ	WRITE OR READ ONLY	WRITE OR READ ONLY
CAPSTAN DIA.	.56	.80	1.60	.80	.80	.40	.80	.80	.80
IPS	1.5	20	25	25	11	.55	10	5	15
VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09
R13	101-5635	101-1545	101-1545	101-1545	101-1045	101-5635	101-8235	101-1545	101-1545
R21	121-1030	121-1020	121-5020	121-1020	121-1020	121-5030	121-5020	121-1030	121-1030
R22	104-2612	104-2611	104-4221	104-2151	104-2151	104-3832	104-4221	104-8251	104-2151
R30	101-1825	101-1825	101-2225	101-2225	101-2225	101-1825	101-1825	101 1825	101-1825
R57	101-1235	101-1835	101-3335	101-1835	101-1835	101-1035	101-1835	101-1835	101-1835
R61	101-1825	101-2725	101-5625	101-2725	101-2725	101-1825	101-2725	101-2725	101-2725
R75					104-2612				
R34	101-2245	101-2245	101-2245	101-8235	101-8235	101-2245	101-2245	101-2245	101-2245
C3	131-3340	131-3340	131-3340	131-3340	131-1540	131-3340		131-3340	131-3340
C16	131-3330	131-3330	131-3330	131-4730	131-4730	131-3330	131-3330	131-3330	131-3330
C17, 18							132-2752		
C19, 20									
R17	121-5030	121-5030	121-5030	121-5030	121-5030	121-5030	121-5030	121-5030	121-5030
R14	101-5635	101-1545	101-1545	101-1545	101-1045	101-5635	101-8235	101-1545	101-1545
R62	104-3481	104-3481	104-3481	104-3481	104-3481	104-3481	104-3481	104-3481	104-3481
R63	104-3161	104-3161	104-3161	104-3161	104-3161	104-3161	104-3161	104-3161	104-3161

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
TYPE	WRITE AND READ	WRITE OR READ ONLY	WRITE AND READ	WRITE AND READ	WRITE AND READ	WRITE OR READ ONLY	WRITE OR READ ONLY	WRITE OR READ ONLY	
CAPSTAN DIA.	.80	1.60	.80	.80	.56	.56	.56	.80	
IPS	12.5	25&11	15	5	4	<4-1.5	25&2.5	25	
VER.	-10	-11	-12	-13	-14	-15	-16	-17	-
R13	101-5635	104-1213	104-6812	104-9092	104-1103	104-1212	104-1963	104-6812	
R21	121-5020	121-1020	121-5020	121-5020	121-5020	121-2030	121-1020	121-1020	
R22	104-4221	104-4221	104-3161	104-1002	104-8251	104-8251	104-2871	104-1961	
R30	101-1825	101-2225	101-1825	101-1825	101-1825	101-1825	101-2225	101-1825	
R57	101-1835	101-3335	101-1835	101-1835	101-1235	101-1235	101-2235	101-1835	
R61	101-2725	101-5625	101-2725	101-2725	101-1825	101-1825	101-3925	101-2725	
R75		104-2612					104-1213		
R34	101-2245	101-1245	101-2245	101-2245	101-2245	101-2245	101-2245	101-1545	
C3		131-1540					131-4740		
C16	131-3330	131-3330	131-3330	131-3330	131-3330	131-3330	131-3330	131-3330	
C17, 18	132-2752		132-2752	132-2752	132-2752	132-2752		132-2752	
C19, 20				132-2752	132-2752	132-2752			
R17	121-5030	121-5030	121-2030	121-5030	121-5030	121-2030	121-5030	121-2030	
R14	101-5635	104-1213	104-6812	104-9092	104-1103	104-1212	104-2873	101-6812	
R62	104-3481	104-3481	104-3481	104-3481	104-3481	104-3481	104-6811	104-3481	
R63	104-3161	104-3161	104-3161	104-3161	104-3161	104-3161	104-6191	104-3161	

FINAL ASSY	
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± ½°
.XXX ± .005
X/X ± 1/32
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES	DATE
DR J.R.THOMPSON	7/31/69
CHK	
DES	
ENGR TCL	7/7/69
ENGR	

FINISH:

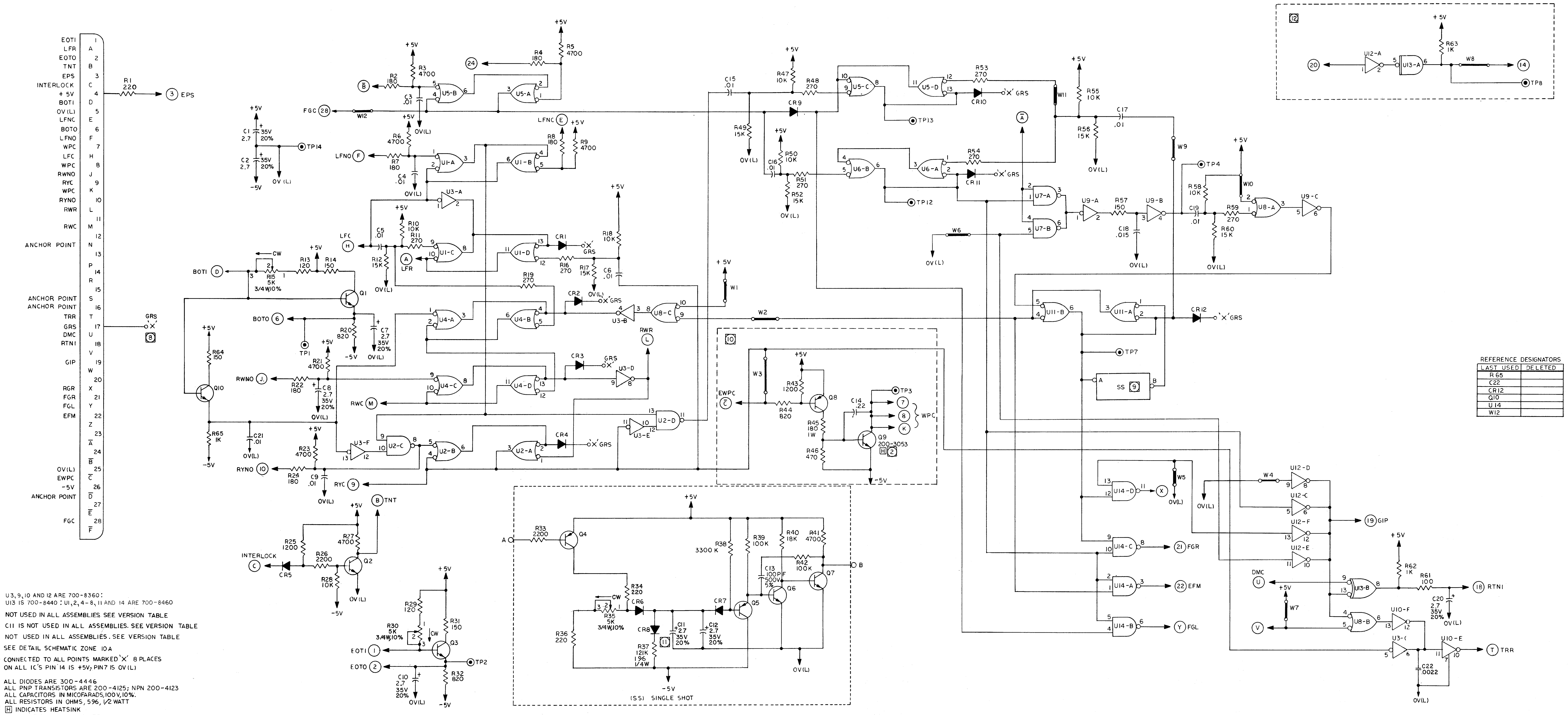
MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA
CAPSTAN DRIVE-
SYNCHRONOUS

SIZE	CODE IDENT. NO.	DWG NO.	REV
D		100475	S

SCALE 2/1 DO NOT SCALE DWG SHEET 1 OF 1



DATE	SYM	REVISION RECORD	AUTH	DR	CH
24 JUNE 68	A	ERN 1-CL	[illegible]	JE	
10/18/68	B	ECN 301	[illegible]	[illegible]	WK
2/26/69	C	ECN 510	[illegible]	WK	[illegible]
7/26/69	D	ECN 867	[illegible]	[illegible]	WK

VERSION TABLE

ASSEMBLY	MODEL	(10)	C11	(12)
100443-01	SYNC READ	NOT USED	NOT USED	NOT USED
100443-02	SYNC WRITE	USED	USED	USED

REFERENCE DESIGNATORS

LAST USED	DELETED
R 65	
C22	
CR12	
Q10	
U 14	
W12	

(13) U3, 9, 10 AND 12 ARE 700-8360:
U13 IS 700-8440: U1, 2, 4-8, 11 AND 14 ARE 700-8460

(12) NOT USED IN ALL ASSEMBLIES. SEE VERSION TABLE

(11) C11 IS NOT USED IN ALL ASSEMBLIES. SEE VERSION TABLE

(10) NOT USED IN ALL ASSEMBLIES. SEE VERSION TABLE

(9) SEE DETAIL SCHEMATIC ZONE 10A

(8) CONNECTED TO ALL POINTS MARKED 'X' 8 PLACES

7. ON ALL IC'S PIN 14 IS +5V; PIN 7 IS OV(L)

6. ALL DIODES ARE 300-4446

5. ALL PNP TRANSISTORS ARE 200-4125; NPN 200-4123

4. ALL CAPACITORS IN MICOFARADS, 100V, 10%.

3. ALL RESISTORS IN OHMS, 5%, 1/2 WATT

(2) [H] INDICATES HEATSINK

1. FOR ASSEMBLY DRAWING SEE 100443.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR
.XXX ± .005 ± 1/2°
X/X ± 1/32
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES	DATE
DR J.E.	5/10/8
CHK	
DES	
ENGR	
ENGR S. MABON	5/10/8

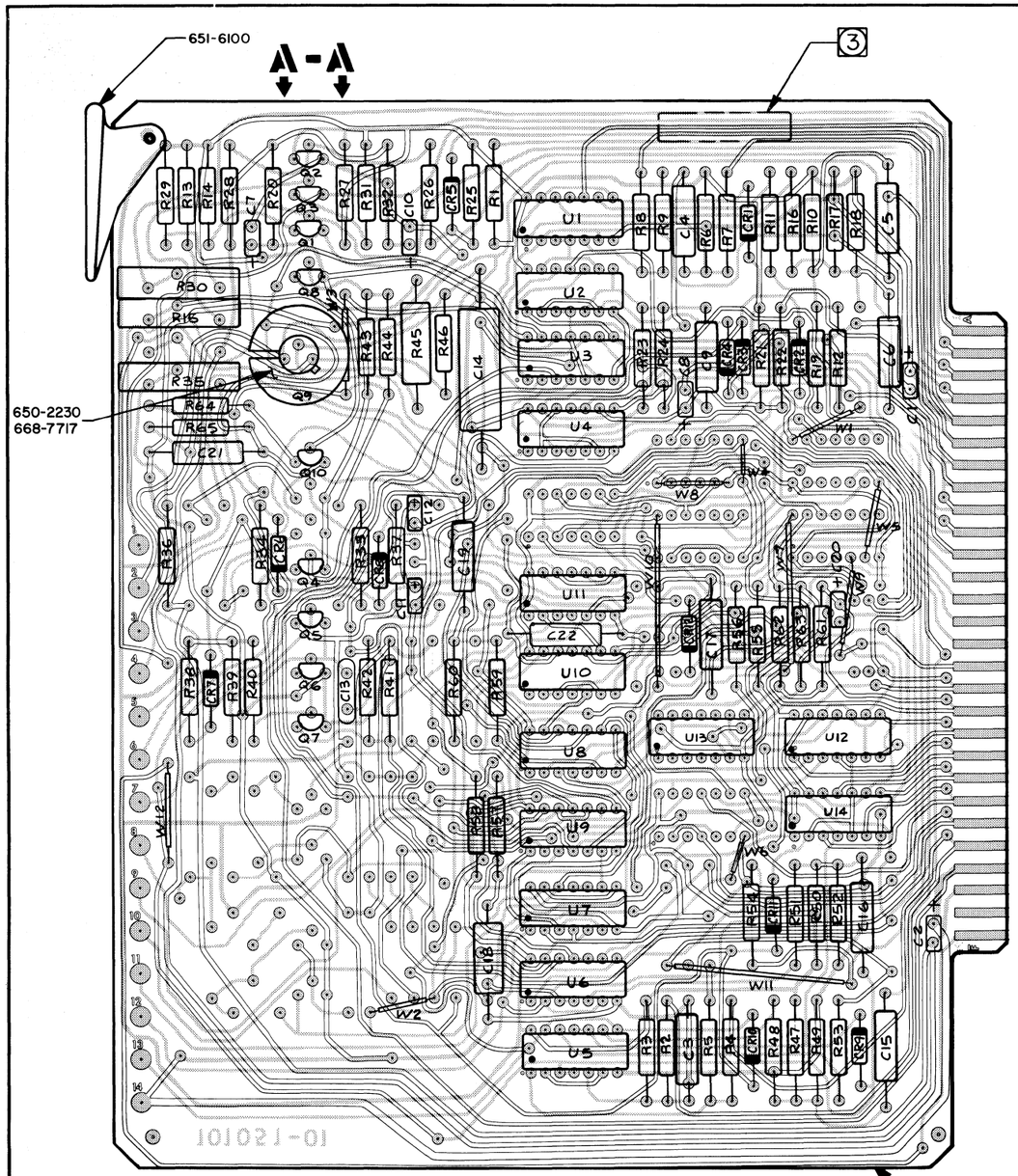
NEXT ASSY | 1ST USED ON
APPLICATION
FINISH:
MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC— FUNCTION CONTROL, SYNCHRONOUS, TYPE B

SIZE D | CODE IDENT. NO. | DWG NO. 100442 | REV D
SCALE | DO NOT SCALE DWG | SHEET | OF

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 1-DN				
B	ECN 206				
C	ECN 868, REVISED & REDRAWN	6/27/9	MK	WK	MK
D	ECN 916; INCORPORATED 511	8/4/9	WK	JDF	MK



4 TABLE I

PART NO.	REF DESIGNATION
101-1015	R61
101-1515	R14,31,57,64
101-1815	R2,4,7,8,22,24
101-2715	R11,16,19,48,51,53,54,59
101-2215	R1,34,36
101-8215	R20,32
101-1025	R62,65
101-1225	R25
101-2225	R26,33
101-4725	R3,5,6,21,23,27,41,9
101-1035	R10,18,28,47,50,55,58
101-1535	R12,17,49,52,56,60
101-1835	R40
101-1045	R39,42
101-3355	R38
121-5020	R15,30,35
104-1213	R37
130-1015	C13
131-1030	C3,4,5,6,9,15,16,17,19,21
131-1530	C18
132-2752	C1,2,7,8,10,12,20
300-4446	CR1-12
200-4123	Q1,2,3,6,7,10
200-4125	Q4,5
700-8360	U3,9,10,12
700-8440	U13
700-8460	U1,2,4,5,6,7,8,11,14
691-0022	W1,2,4,5,6,7,9,10,11
131-2220	C22
101-1215	R13,29
100373-01	W12

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL / VER. -01	SYNC WRITE -02	SYNC READ -03	SYNC WRITE -04	-05	-06	-07	-08	-09
R46	NO	101-4715							
R44	ADDITIONS	101-8215							
R63		101-1025							
R43		101-1225							
R45		102-1815							
C14		131-2240							
Q9		200-3053							
Q8		200-4125							
W8		691-0022							
W3		100373-01							
C11		132-2752							

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO, SEE TABLE II.

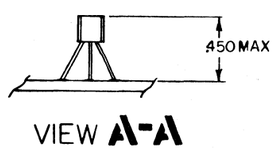
4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC 100442
SPECIFICATION 100446

NOTES: UNLESS OTHERWISE SPECIFIED



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± ½°
.XXX ± .005
X/X ± 1/32
BREAK ALL SHARP CORNERS
APPROX. 010

SIGNATURES	DATE
DR G. FICKEN	7/10/6
CHK	
DES	
ENGR E.M.D	7/10/68
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA- FUNCTION CONTROL SYNCHRONOUS "B"

NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:

MATL:

SIZE	CODE IDENT. NO.	DWG NO.	REV
D		100443	D
SCALE 2/1		DO NOT SCALE DWG	SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPD
A	ERN 1-SH		J.T.		
B	ECN 593	9/2/69			

REFERENCE DESIGNATORS

LAST USED	DELETED
R81	
C24	
CR17	
Q17	
U10	
TP9	

VERSION TABLE

SPEED IPS	NUMBER OF TRACKS	DENSITY BPI	ASSEMBLY NUMBER 100359	R30,40 1/2W 5%	R62 1/2W 5%	R73 1/2W 5%	C16 100V 10%	C19 100V 10%	C23,24 20V 20%
FOR REFERENCE ONLY			-01						
			-02						
			-03						
25-16	9	800	-04	27K	27K	33K	.015	.0068	NOT USED
	7	800	-05	33K	33K	NOT USED	.0068	NOT USED	↑
	7	556	-06	33K	18K	NOT USED	.015	NOT USED	
	7	200	-07	33K	27K	NOT USED	.033	NOT USED	
∠16-10	9	800	-08	47K	18K	22K	.033	.015	
	7	800	-09	56K	22K	NOT USED	.015	NOT USED	
	7	556	-10	56K	18K	NOT USED	.022	NOT USED	↓
	7	200	-11	56K	27K	NOT USED	.047	NOT USED	NOT USED
∠10-6	9	800	-12	39K	18K	22K	.047	.022	2.7
	7	800	-13	47K	22K	NOT USED	.022	NOT USED	↑
	7	556	-14	47K	22K	NOT USED	.033	NOT USED	
	7	200	-15	47K	22K	NOT USED	.10	NOT USED	
∠6-4	9	800	-16	56K	39K	47K	.047	.022	
	7	800	-17	68K	47K	NOT USED	.022	NOT USED	
	7	556	-18	68K	27K	NOT USED	.047	NOT USED	↓
	7	200	-19	68K	39K	NOT USED	.10	NOT USED	2.7

12. (PX) DESIGNATIONS BY POTENTIOMETERS ARE REFERENCE FROM TOP OF CARD.
11. ON 7 AND 9 TRK PIN C IS CONNECTED TO PIN L ON CARD CAGE WIRING.
10. ON 9 TRK PIN W IS CONNECTED TO PIN Y ON CARD CAGE WIRING AND PIN U IS CONNECTED TO PIN S ON CARD CAGE WIRING.
9. ON 7 TRK PIN W IS CONNECTED TO PIN Y ON CARD CAGE WIRING.
8. SEE VERSION TABLE FOR COMPONENT VALUE.
7. ALL QUAD-2 INPUT GATES ARE 700-8460.
6. ALL HEX-INVERTORS 700-8360.
5. ALL PNP TRANSISTORS ARE 200-4125, NPN 200-4123.
4. ALL DIODES ARE 300-4446.
3. ALL CAPACITORS IN MICROFARADS, 100 VOLTS, 10%.
2. ALL RESISTORS IN OHMS, 1/2 WATT, 5%.
1. FOR ASSEMBLY DRAWING SEE 100359.

NOTES: UNLESS OTHERWISE SPECIFIED

100359	—
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010, .XXX ± .005, X/X ± 1/32; ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

SIGNATURES	DATE
DR J.R. THOMPSON	2/3/69
CHK	2/3/69
DES	
ENGR E.M. Dunstan	
ENGR	

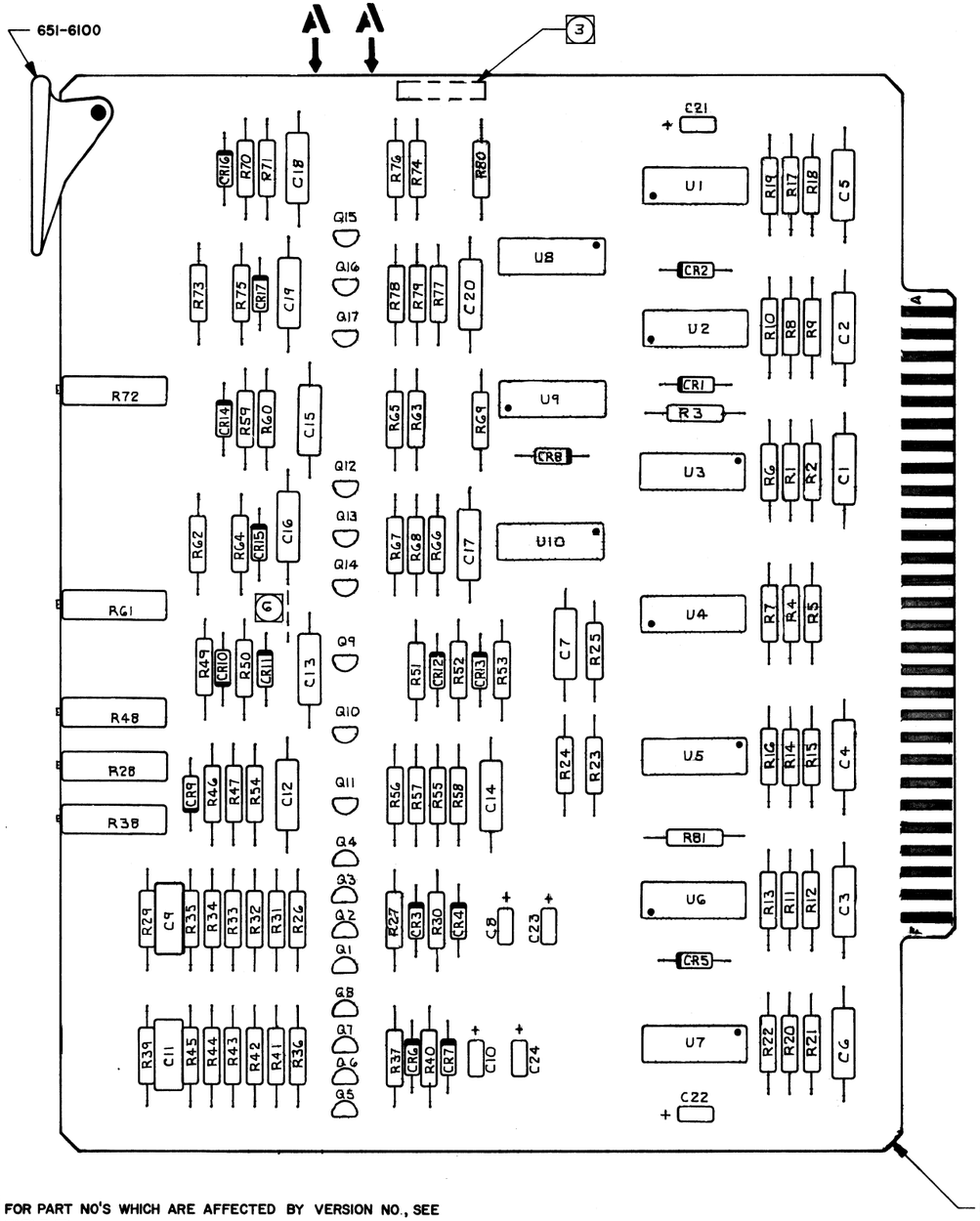
MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC FUNCTION CONTROL SYNCHRONOUS 'A'

SIZE	CODE IDENT. NO.	DWG NO.	REV
H		100358	B
SCALE NONE		DO NOT SCALE DWG	SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
C	ERN 1-ST	9/4/69	J.T.	WK	MCT
D	ECN 533	9/11/69	J.T.	WK	MCT



4 TABLE I

PART NO	REF. DESIGNATION
700-8360	U3,5,7,8,10
700-8460	U1,2,4,6,9
300-4446	CR1-17
200-4123	Q3,4,7-17
200-4125	Q1,2,5,6
132-2752	C8,10,21,22
131-1020	C7,12,15,18
131-4720	C14,17,20
131-1030	C1,3-6
131-3320	C13
131-2220	C2
130-1015	C9,11
121-1030	R48
121-5030	R61,72
121-5020	R28,38
104-8251	R49
101-2215	R27,29,37,39
101-2715	R3,6,7,10,13,16,19,22, 25,81
101-1025	R54,55,58,66,69, 77,80
101-2225	R26,36,47,60,71
101-2725	R56,67,78
101-3325	R46,57,59,68,70,79
101-4725	R34,44,63,65,74,76
101-1035	R1,4,8,11,14,17,20, 23,51,52,53
101-1535	R2,5,9,12,15,18, 21,24
101-1835	R33,43
101-2235	R64,75
101-3935	R50
101-1045	R32,35,42,45
101-3355	R31,41

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VERSION	-01	-02	-03	-04	-05	-06	-07	-08	-09
R30,40				101-2735	101-3335	101-3335	101-3335	101-4735	101-5635
R62				101-2735	101-3335	101-1835	101-2735	101-1835	101-2235
R73				101-3335				101-2235	
C16				131-1530	131-6820	131-1530	131-3330	131-3330	131-1530
C19				131-6820				131-1530	
C23,24									

TABLE II CONTINUED

REFERENCE DESIGNATION	PART NUMBERS									
MODEL / VERSION	-10	-11	-12	-13	-14	-15	-16	-17	-18	-19
R30,40	101-5635	101-5635	101-3935	101-4735	101-4735	101-4735	101-5635	101-6835	101-6835	101-6835
R62	101-1835	101-2735	101-1835	101-2235	101-2235	101-2235	101-3935	101-4735	101-2735	101-3935
R73			101-2235				101-4735			
C16	131-2230	131-4730	131-4730	131-2230	131-3330	131-1040	131-4730	131-2230	131-4730	131-1040
C19			131-2230				131-2230			
C23,24			132-2752	132-2752	132-2752	132-2752	132-2752	132-2752	132-2752	132-2752

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO., SEE TABLE II.

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO., SEE TABLE I.

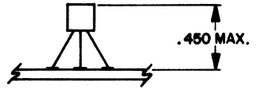
3 RUBBER STAMP PART NO., INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REFERENCE DRAWINGS: SCHEMATIC-100358
SPECIFICATION-

NOTES: UNLESS OTHERWISE SPECIFIED

6 LARGER SPACING REQUIRED VERSIONS -16 AND -19.



VIEW A-A

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
XX ± .010 ANGULAR
XXX ± .005 ± 1/2°
X/X ± 1/32
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES	DATE
DR J.R. THOMPSON	8/4/69
CHK Walt Konp	9 sept 69
DES	
ENGR MCT	8/5/69
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA
FUNCTION CONTROL
SYNCHRONOUS 'A'

TOP ASSY	
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:

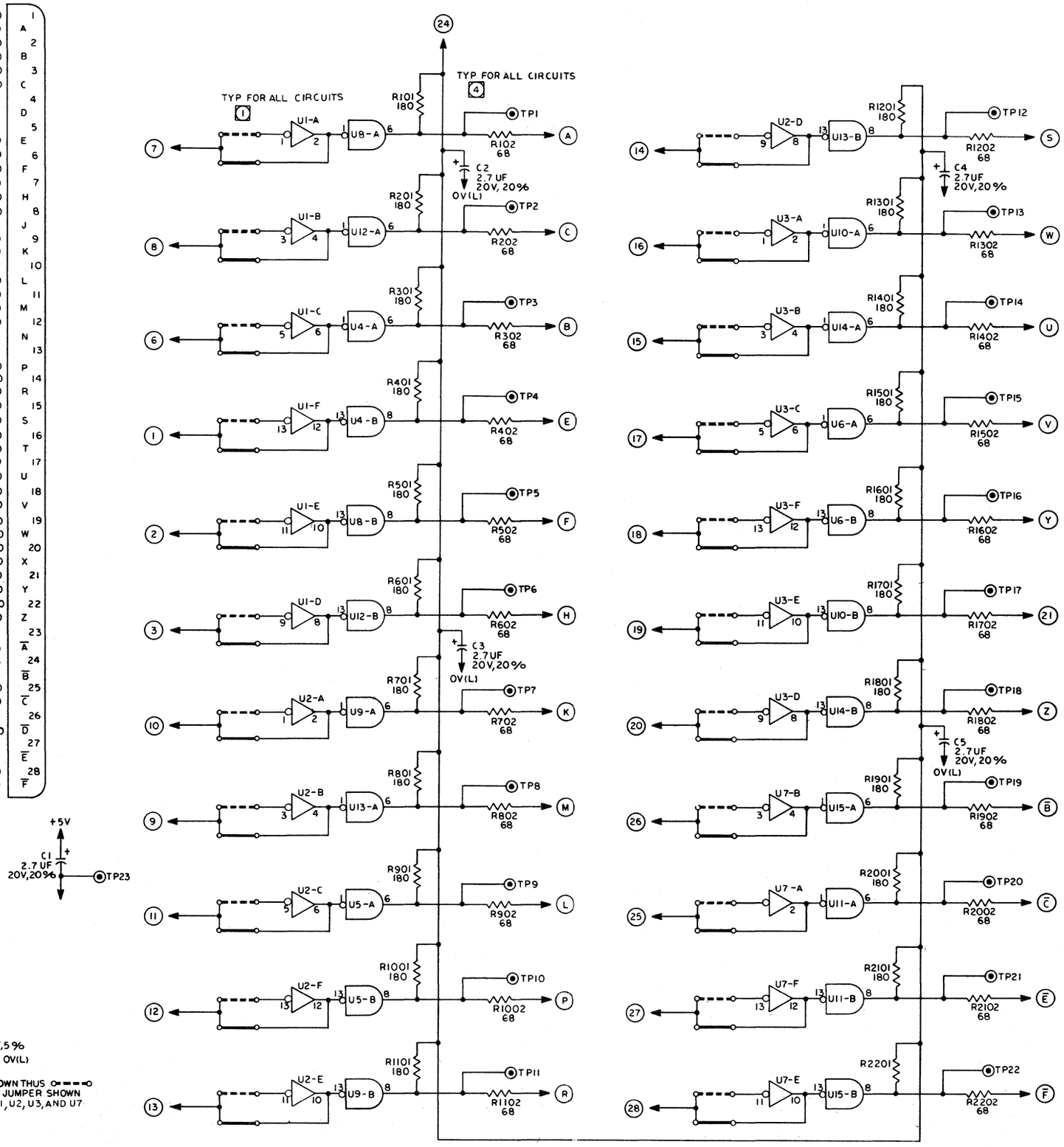
MATL:

SIZE D | CODE IDENT NO. | DWG NO. 100359 | REV D

SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

DATE	SYM	REVISION RECORD	AUTH	DR	CH
4/11/68	A	ERN 1-AN	JAW	JS	JAW
3 MAY 68	B	ECN 023	JAW	JCT	JAW

INPUT CIRCUIT 400	1
OUTPUT CIRCUIT 100	A
INPUT CIRCUIT 500	2
OUTPUT CIRCUIT 300	B
INPUT CIRCUIT 600	3
OUTPUT CIRCUIT 200	C
+5V	4
GROUND RETURN CIRCUITS 100,200,300	D
OV(L)	5
OUTPUT CIRCUIT 400	E
INPUT CIRCUIT 300	6
OUTPUT CIRCUIT 500	F
INPUT CIRCUIT 100	7
OUTPUT CIRCUIT 600	H
INPUT CIRCUIT 200	8
GROUND RETURN CIRCUITS 400,500,600	J
INPUT CIRCUIT 800	9
OUTPUT CIRCUIT 700	K
INPUT CIRCUIT 700	10
OUTPUT CIRCUIT 900	L
INPUT CIRCUIT 900	11
OUTPUT CIRCUIT 800	M
INPUT CIRCUIT 1000	12
GROUND RETURN CIRCUITS 700,800,900	N
INPUT CIRCUIT 1100	13
OUTPUT CIRCUIT 1000	P
INPUT CIRCUIT 1200	14
OUTPUT CIRCUIT 1100	R
INPUT CIRCUIT 1400	15
OUTPUT CIRCUIT 1200	S
INPUT CIRCUIT 1300	16
GROUND RETURN CIRCUITS 1000,1100,1200	T
INPUT CIRCUIT 1500	17
OUTPUT CIRCUIT 1400	U
INPUT CIRCUIT 1600	18
OUTPUT CIRCUIT 1500	V
INPUT CIRCUIT 1700	19
OUTPUT CIRCUIT 1300	W
INPUT CIRCUIT 1800	20
GROUND RETURN CIRCUITS 1300,1400,1500	X
OUTPUT CIRCUIT 1700	21
OUTPUT CIRCUIT 1600	Y
GROUND RETURN CIRCUIT 2200	22
OUTPUT CIRCUIT 1800	Z
	23
GROUND RETURN CIRCUITS 1600,1700,1800	$\overline{A}$
PULL-UP RESISTORS	24
OUTPUT CIRCUIT 1900	$\overline{B}$
INPUT CIRCUIT 2000	25
OUTPUT CIRCUIT 2000	$\overline{C}$
INPUT CIRCUIT 1900	26
GROUND RETURN CIRCUITS 1900,2000,2100	$\overline{D}$
INPUT CIRCUIT 2100	27
OUTPUT CIRCUIT 2100	$\overline{E}$
INPUT CIRCUIT 2200	28
OUTPUT CIRCUIT 2200	$\overline{F}$



VERSION TABLE

MODEL	ASSEMBY	CIRCUITS USED	R1	R2	C2THRU C5
HIGH TRUE	100339-01	100 THRU 1200	USED	USED	USED
HIGH TRUE	100339-02	100 THRU 2200	USED	USED	USED
LOW TRUE	100339-03	100 THRU 1200	USED	USED	USED
LOW TRUE	100339-04	100 THRU 2200	USED	USED	USED
LOW TRUE	100339-05	100 THRU 2200	NOT USED	NOT USED, SUBSTITUTED WITH JUMPER	NOT USED
LOW TRUE	100339-06	100 THRU 1200	NOT USED	NOT USED, SUBSTITUTED WITH JUMPER	NOT USED

REFERENCE DESIGNATOR

LAST USED	DELETED
R2	
C5	
U15	
TP23	

[4] SEE VERSION TABLE

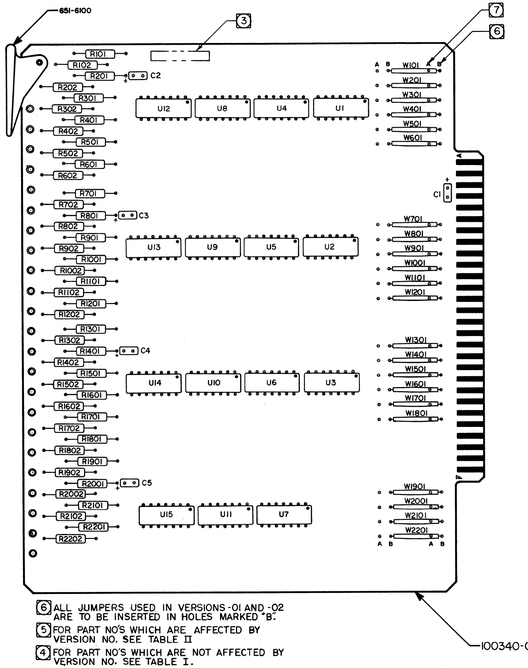
3. ALL RESISTORS IN OHMS, 1/2 WATT, 5%
2. ON ALL IC'S PIN14 IS +5V; PIN 7 IS OV(L)

[1] FOR LOW-TRUE LOGIC, JUMPER SHOWN THUS o----o IS USED. FOR HIGH-TRUE LOGIC, JUMPER SHOWN THUS o——o IS USED AND IC U1, U2, U3, AND U7 ARE OMITTED

NOTES. UNLESS OTHERWISE SPECIFIED

TOLERANCES UNLESS OTHERWISE SPECIFIED	PERIPHERAL EQUIPMENT CORPORATION	
DECIMAL ±	SCALE	DRAWN BY J.E. RINGLER
FRACTIONAL ±	TITLE SCHEMATIC-TRANSMITTER DTL	
ANGULAR ±	DATE 23 FEB 68	DRAWING NUMBER 100338 ISSUE B

SHEET	ZONE	REVISION RECORD	APPD	DATE
01	A	ERN 1-EC	WC	8/77



INFORMATION IN TABLES ON SH 1 APPLIES TO VERSIONS 01,02,03 AND 04

4 TABLE I

PART NO.	REF DESIGNATION
700-8440	U4,5,8,9,12,13
132-2752	C1,2,3
101-1815	R1101-1201
101-6805	R1102-1202
100373-01	W101-1201

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL / HI-TRUE VER.	-01	HI-TRUE -02	LOW-TRUE -03	LOW-TRUE -04	-05	-06	-07	-08	-09
U6,10,11,14,15	NO ADDITIONS		700-8440		700-8440					
U1,2				700-8360	700-8360					
U3,7					700-8360					
C4,5			132-2752		132-2752					
R1301-2201			101-1815		101-1815					
R1302-2202			101-6805		101-6805					
W1301-2201			100373-01		100373-01					

6 ALL JUMPERS USED IN VERSIONS -01 AND -02 ARE TO BE INSERTED IN HOLES MARKED "B".

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II

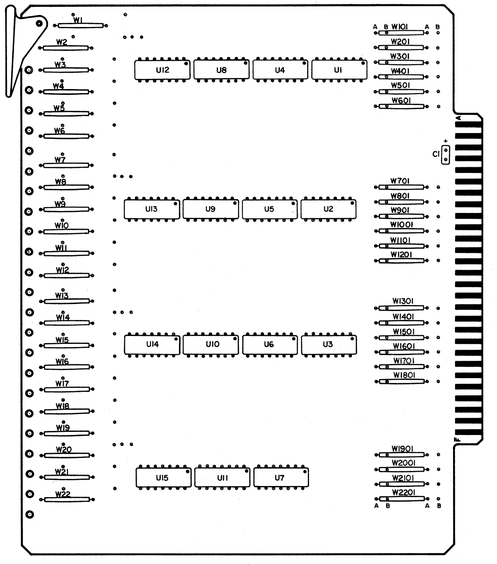
4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.
2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.
1. REF DWGS: SCHEMATIC-100338
SPEC-100342

7 ALL JUMPERS USED IN VERSIONS -03,04,05 AND -06. ARE TO BE INSERTED IN HOLES MARKED "A".

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES UNLESS OTHERWISE NOTED	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL .X ± .XX ±		SIZE 2:1	APPROVED
FRACTIONAL ±	TITLE PCBA TRANSMITTER, DTL		SHEET 1 OF 2
ANGULAR ±	DATE 1-28-78	DRAWING NUMBER 100339	ISSUE A



INFORMATION IN TABLES ON SH 2 APPLIES TO VERSIONS 05 AND 06.

TABLE I

PART NO.	REF DESIGNATION
700-8360	U1,2
700-8440	U4,5,8,9,12,13
132-2752	C1
100373-01	W1-12, 101-1201

TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL / LOW TRUE VER.	-01	-02	-03	-04	LOW TRUE -05	LOW TRUE -06	-07	-08	-09
U3,7						700-8360	NO			
U6,10,11,14,15						700-8440	ADDITIONS			
W13-22, 1301-2201						100373-01				

TOLERANCES UNLESS OTHERWISE NOTED	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL .X ± .XX ±		SIZE 2:1	APPROVED
FRACTIONAL ±	TITLE PCBA TRANSMITTER DTL		SHEET 2 OF 2
ANGULAR ±	DATE 5-26-78	DRAWING NUMBER 100339	ISSUE A

DATE	SYM	REVISION RECORD	AUTH	D	CH
11-14	A	ECN 1-AN			
4 MAY	B	ECN-067			
6 MAY	C	ECN-078			
8-2	D	ECN-167			

5 CONNECTIONS

CIRCUIT	100	200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000	2100
IC	U14	U14	U14	U13	U13	U13	U12	U12	U12	U11	U11	U11	U10	U10	U10	U9	U9	U8	U8		
A	13	11	9	13	11	9	13	11	9	13	11	9	13	11	9	13	11	9	13	9	11
B	12	10	8	12	10	8	12	10	8	12	10	8	12	10	8	12	10	8	12	8	10
C	1	3	5	1	3	5	1	3	5	1	3	5	1	3	5	1	3	5	1	5	3
D	2	4	6	2	4	6	2	4	6	2	4	6	2	4	6	2	4	6	2	6	4
W	1	2	3	4	5	6	7	8	9	10	11	12,13	14	15,16	17,18	19	20,21	22	23	24,25	26,27

VERSION TABLE

MODEL	ASSEMBLY	CIRCUITS USED CONFIG A	CONFIG B	CONFIG C	7	6
HIGH-TRUE WRITE	100334-01	100 THRU 1700,1900 THRU 2100	1800	NONE	USED	NOT USED
LOW-TRUE WRITE	100334-02	NONE	ALL	NONE	USED	NOT USED
HIGH-TRUE READ	100334-03	200 THRU 900,1300 1600	1800	NONE	NOT USED	NOT USED
LOW-TRUE READ	100334-04	NONE	200 THRU 900,1300 1600,1800	NONE	NOT USED	NOT USED
LOW-TRUE READ	100334-05	NONE	1800	200 THRU 900,1300 1600	NOT USED	USED
LOW-TRUE WRITE	100334-06	NONE	1800	100 THRU 1700,1900 THRU 2100	USED	USED

REFERENCE DESIGNATORS

LAST USED	DELETED
R3	
C9	
U14	
TP23	
S1	
W27	

9 SEE DWG 100334 FOR ASSEMBLY

8. ALL CAPACITORS IN MICOFARADS, 20V, 20%

7 THIS PORTION OF CIRCUIT (ENCLOSED IN BROKEN LINE) IS OMITTED IN SOME ASSEMBLIES. SEE VERSION TABLE ZONE 2E

6 C3 THRU C8 ARE NOT USED IN ALL ASSEMBLIES. SEE VERSION TABLE

5 SEE CONNECTION CHART FOR PIN NUMBERS AND WIRE NUMBERS

4. REFERENCE DESIGNATORS ARE NOT COMPLETE. FOR COMPLETE DES. ADD PREFIX OF CIRCUIT TO DESIGNATOR. FOR EXAMPLE: R1 OF CIRCUIT 500 IS R501; C1 OF CIRCUIT 2100 IS C2101

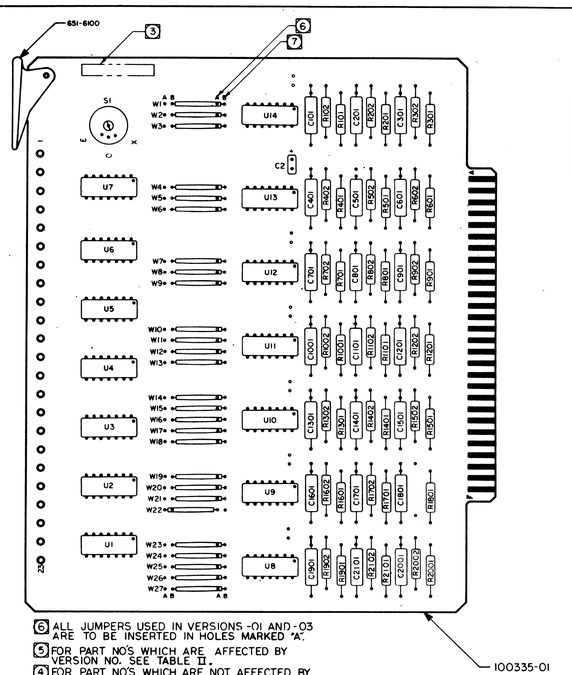
3 O = ODD PARITY, E = EVEN PARITY, X = EXTERNAL PARITY

2 TYPICAL OF CIRCUITS 200,300,400,500,600,700,800,900,1300,1600 AND 1900. SEE CONNECTOR FOR PINS USED FOR EACH CIRCUIT. TEST POINTS ARE IDENTIFIED BY CIRCUIT NO. FOR EXAMPLE: TEST POINT OF CIRCUIT 200 IS TP2, CIRCUIT 1600 IS TP16

1 WHEN CONFIGURATION 'A' IS USED, THE REQUIRED JUMPER CONNECTIONS ARE REPRESENTED THUS: o——o; CONFIGURATION 'B' OR 'C': o - - - - o. SEE VERSION TABLE FOR CONNECTIONS USED.

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE	DRAWN BY D. DELUCA
FRACTIONAL ±	TITLE SCHEMATIC - RECEIVER, DTL		APPROVED BY
ANGULAR ±	DATE 19 Feb 66	DRAWING NUMBER 100333	ISSUE D



INFORMATION ON SHEET 1 APPLIES TO VERSIONS -01,02,03,04.

4 TABLE I

PART NO.	REF DESIGNATION
700-8360	U9,10,12,13,14
132-2752	C2
131-1020	C201-901,1301,1401,1801
101-6805	R201-901, 1301, 1601, 1801
100373-01	W2-9, 14, 19, 22

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL / VER	LOW TRUE WRITE	HIGH TRUE READ	LOW TRUE READ	LOW TRUE READ	LOW TRUE WRITE	-07	-08	-09
	-01	-02	-03	-04	-05	-06			
U1,4,5,8,11		700-8360	700-8360		NO	SEE			
U2,3,6,7		700-8460	700-8460		ADDITIONS	SHT 2	SHT 2		
S1		514-8711	514-8711						
C101,1001,1101,1201,1401		131-1020	131-1020						
C1501,1701,1901-2101									
R101,1001,1101,1201 1401		101-6805	101-6805						
R1501,1701,1901-2101									
R202-902,1302,1602		101-4715		101-4715					
R102,1002,1102,1202, R1402,1502,1702, R1902-2102		101-4715							
W1,10-13,15-18,20,21, W23-27		100373-01	100373-01						

6 ALL JUMPERS USED IN VERSIONS -01 AND -03 ARE TO BE INSERTED IN HOLES MARKED "A".

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

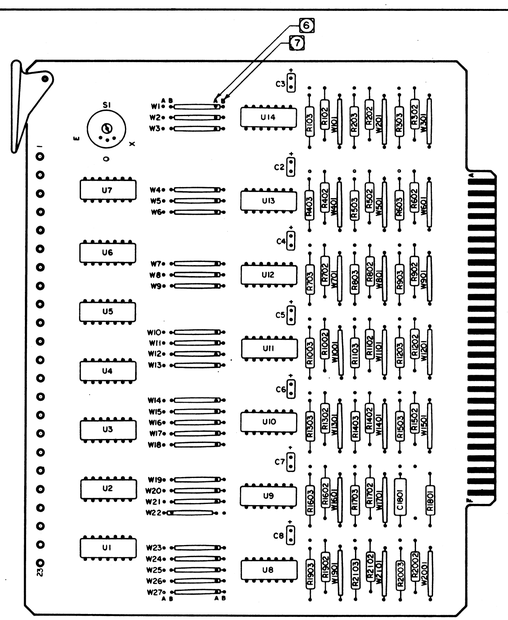
2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100333
SPEC-100337

NOTES: UNLESS OTHERWISE SPECIFIED

7 ALL JUMPERS USED IN VERSIONS -02,-04,-05, AND -06, EXCEPT W22, ARE TO BE INSERTED IN HOLES MARKED "B".

TOLERANCES	PERIPHERAL EQUIPMENT CORPORATION		
.X		SCALE 2/1	
.XX	TITLE PCBA RECEIVER DTL		SHEET 1 OF 2
.XXX	DATE 10-16-68	DRAWING NUMBER 100334	ISSUE C



INFORMATION ON SHEET 2 APPLIES TO VERSIONS 05,06.

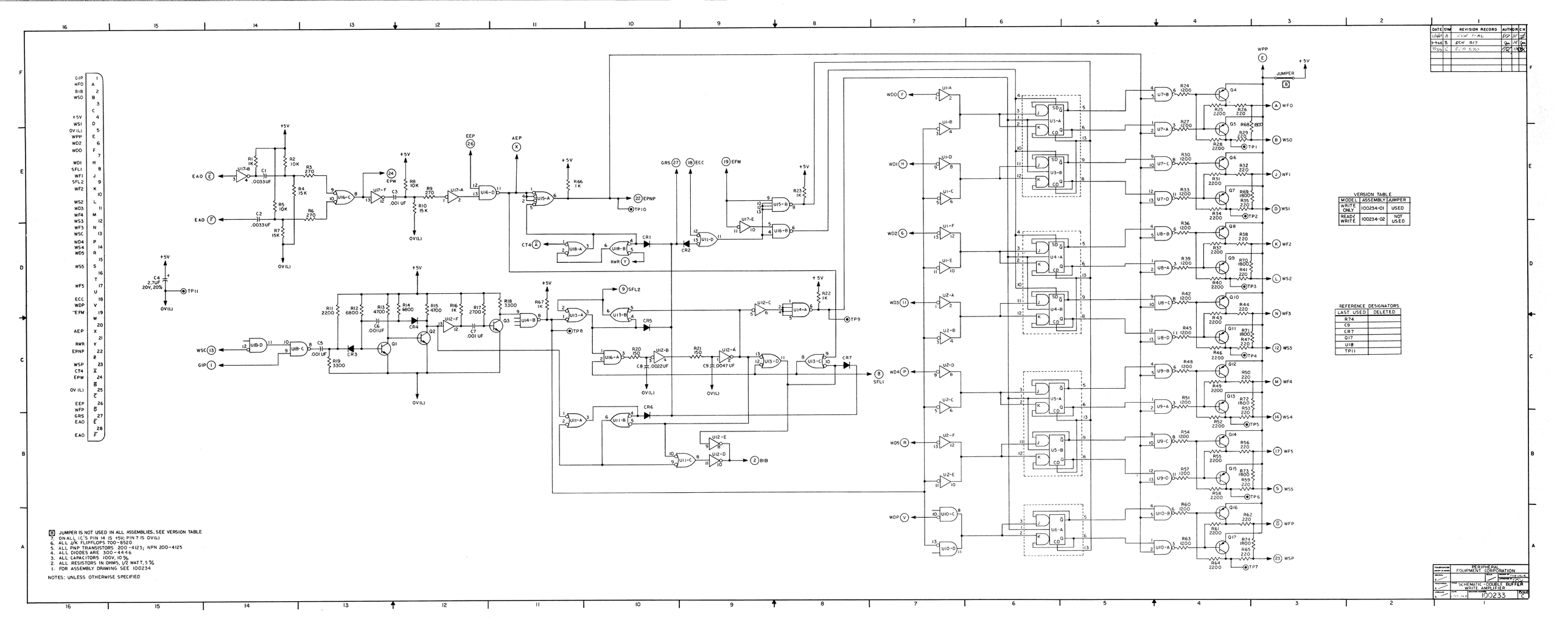
4 TABLE I

PART NO.	REF DESIGNATION
700-8360	U9,10,12,13,14
132-2752	C2-8
131-1020	C1801
101-6805	R1801
101-2215	R203-903,1303,1603
101-3315	R202-902,1302,1602
100373-01	W2-9,14,19,22, W201-901,1301,1601

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL / VER				LOW TRUE READ	LOW TRUE WRITE			
	-01	-02	-03	-04	-05	-06	-07	-08	-09
U1,4,5,8,11					NO	700-8360			
U2,3,6,7					ADDITIONS	700-8460			
S1						514-8711			
R102,1002-1202,1402						101 3315			
R1502,1702,1902-2102									
R103,1003-1203,1403, R1503,1703,1903-2103						101 2215			
W1,10,11,12,15,16,17,18, W20,21,23-27,						100373-01			
W101,1001-1201,1401, W1501,1701,1901-2101									

TOLERANCES	PERIPHERAL EQUIPMENT CORPORATION		
.X		SCALE 2/1	
.XX	TITLE PCBA RECEIVER DTL		SHEET 2 OF 2
.XXX	DATE 10-16-68	DRAWING NUMBER 100334	ISSUE C



DATE	SYM	REVISION RECORD	AUTHOR	CH
1/1/69	A	[illegible]	[illegible]	[illegible]
3-7-69	B	ECN 017	[illegible]	[illegible]
[illegible]	C	[illegible]	[illegible]	[illegible]

VERSION TABLE

MODEL	ASSEMBLY	JUMPER
WRITE ONLY	100234-01	USED
READ/ WRITE	100234-02	NOT USED

REFERENCE DESIGNATORS

LAST USED	DELETED
R74	
C9	
CR7	
Q17	
U18	
TP11	

(8) JUMPER IS NOT USED IN ALL ASSEMBLIES. SEE VERSION TABLE

7. ON ALL I.C.'S PIN 14 IS +5V; PIN 7 IS OV(L)
6. ALL U/A FLIPFLOPS 700-8520
5. ALL PNP TRANSISTORS 200-4123; NPN 200-4125
4. ALL DIODES ARE 300-4446
3. ALL CAPACITORS 100V, 10%
2. ALL RESISTORS IN OHMS, 1/2 WATT, 5%
1. FOR ASSEMBLY DRAWING SEE 100234

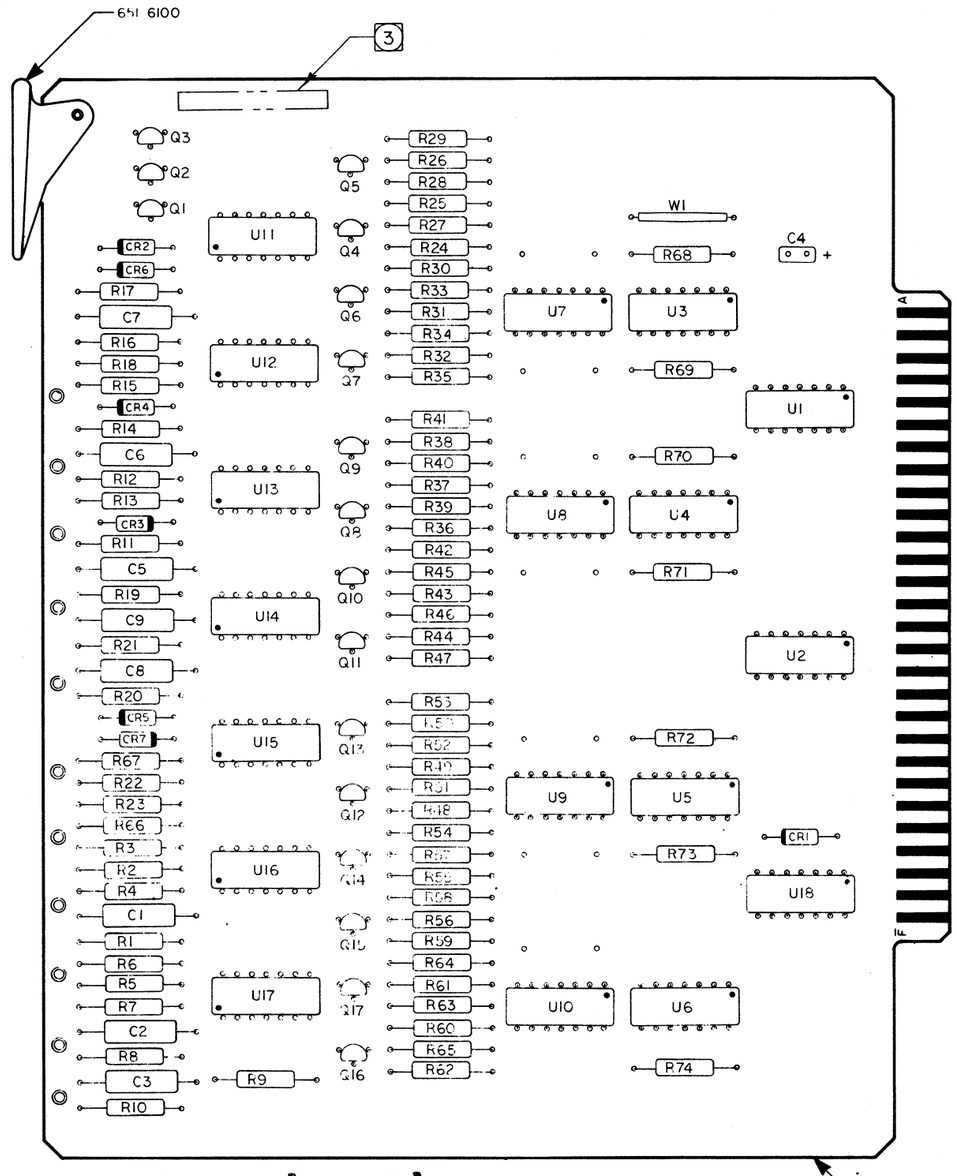
NOTES: UNLESS OTHERWISE SPECIFIED

PERIPHERAL EQUIPMENT CORPORATION

SCHEMATIC - DOUBLE BUFFER WRITE AMPLIFIER

10233 C

DATE	BYM	REVISION RECORD	AUTH	DR	CK



100235-01

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I

3 RUBBER STAMP PART NO., INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC, 100233
SPEC, 100237

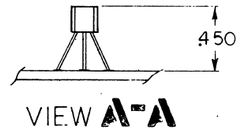
NOTES: UNLESS OTHERWISE SPECIFIED

4 TABLE I

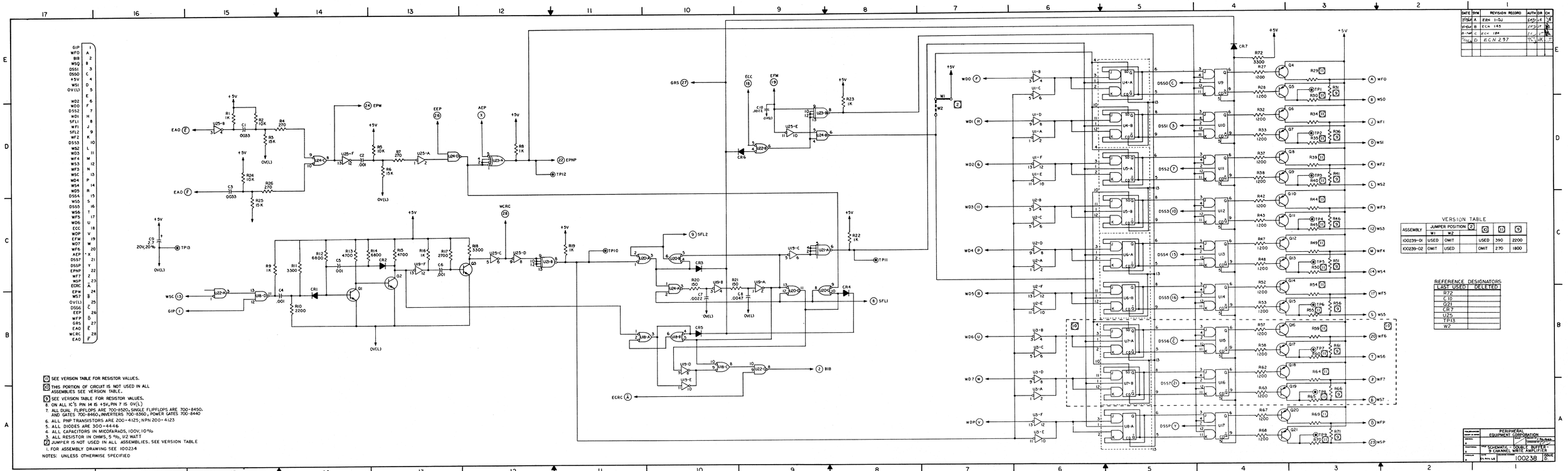
PART NO.	REF DESIGNATION
200-4123	Q1,2,3
200-4125	Q4,5,6,7,8,9,10,11,12,13,14, 15,16,17
700-8360	U1,2,12,17
700-8440	U14,15
700-8460	U7,8,9,10,11,13,16,18
700-8520	U3,4,5,6
300-4446	CR1,2,3,4,5,6,7
101-1515	R20,21
101-2215	R26,29,32,35,38,41,44, 47,50,53,56,59,62,65
101-2715	R3,6,9
101-1025	R1,16,22,23,66,67
101-1225	R24,27,30,33,36,39,42, 45,48,51,54,57,60,63
101-2225	R11,25,28,31,34,37,40,43, 46,49,52,55,58,61,64
101-2725	R17
101-3325	R18,19
101-4725	R13,15
101-6825	R12,14
101-1035	R2,8,5
101-1535	R4,7,10
101-1825	R68,69,70,71,72,73,74
131-1020	C3,5,6,7
131-2220	C8
131-3320	C1,2
131-4720	C9
131-2752	C4
100373-01	W1

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
	MODEL / VER. -01	-02	-03	-04	-05	-06	-07	-08	-09



TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE 5:1	DRAWN BY M.K.S.
			APPROVED BY
FRACTIONAL ±	TITLE PCBA DOUBLE BUFFER W AMP		SHEET 1 OF 1
ANGULAR ±	DATE	DRAWING NUMBER 100234	ISSUE C



DATE	SYM	REVISION RECORD	AUTH	DR	CK
2/76	A	ECN 145			
4/76	B	ECN 145			
8/76	C	ECN 184			
10/76	D	ECN 297			

VERSION TABLE

ASSEMBLY	JUMPER POSITION [2] W1	W2	[10]	[11]	[9]
100239-01	USED	OMIT	USED	390	2200
100239-02	OMIT	USED	OMIT	270	1800

REFERENCE DESIGNATORS

LIST USED	DELETED
R72	
C10	
Q21	
CR7	
U25	
TP13	
W2	

[11] SEE VERSION TABLE FOR RESISTOR VALUES.

[10] THIS PORTION OF CIRCUIT IS NOT USED IN ALL ASSEMBLIES SEE VERSION TABLE.

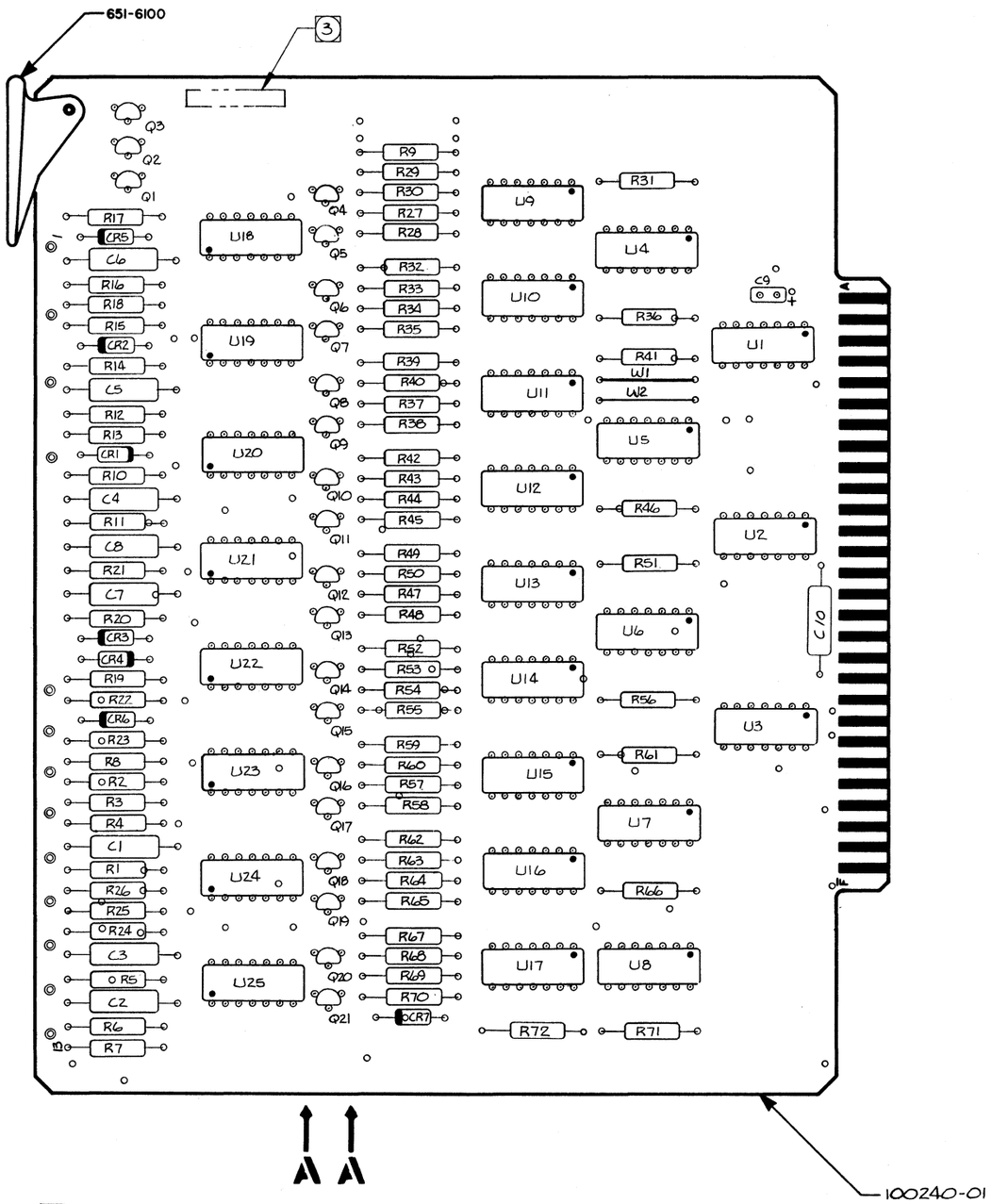
[9] SEE VERSION TABLE FOR RESISTOR VALUES.

8. ON ALL IC'S PIN 14 IS +5V, PIN 7 IS OV(L)
7. ALL DUAL FLIPFLOPS ARE 700-8520, SINGLE FLIPFLOPS ARE 700-8450, AND GATES 700-8460, INVERTERS 700-8360, POWER GATES 700-8440
6. ALL PNP TRANSISTORS ARE 200-4125, NPN 200-4123
5. ALL DIODES ARE 300-4446
4. ALL CAPACITORS IN MICOFARADS, 100V, 10%
3. ALL RESISTOR IN OHMS, 5 %, 1/2 WATT
[2] JUMPER IS NOT USED IN ALL ASSEMBLIES, SEE VERSION TABLE
1. FOR ASSEMBLY DRAWING SEE 100234

NOTES: UNLESS OTHERWISE SPECIFIED

PERIPHERAL EQUIPMENT CORPORATION
SCHEMATIC - DOUBLE BUFFER - 9 CHANNEL WRITE AMPLIFIER
100238 D

DATE	BY	REVISION RECORD	AUTH.	QA	CK.
7-29	A	ERN 1-EC	ERD	MK	MK
8-8	B	ECN 120	ERD	MK	MK
9/66	C	ECN 297	ERD	MK	STD



3 RUBBER STAMP PART NO, INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100238.
SPEC-100242.

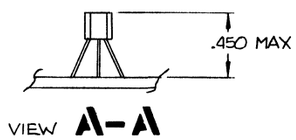
NOTES: UNLESS OTHERWISE SPECIFIED

4 TABLE I

PART NO.	REF. DESIGNATION
101-1515	R20, 21
101-2715	R4, 7, 26
101-1025	R1, 8, 9, 16, 19, 22, 23
101-1225	R27, 28, 32, 33, 37, 38, 42, 43, 47, 48, 52, 53, 68, 67
101-2225	R10
101-2725	R17
101-3325	R11, R18, R72
101-4725	R13, R15
101-6825	R12, 14
101-1085	R2, 5, 24
101-1535	R3, 6, 25
131-1020	C2, 4, 5, 6
131-2220	C7, 10
131-3320	C1, 3
131-4720	C8
132-2752	C9
200-4123	Q1, 2, 3
200-4125	Q4-Q15, 20, 21
200-4446	CR1-CR7
700-8360	U1, 2, 3, 19, 25
700-8440	U21, 23
700-8450	U9-U14, 17
700-8460	U18, 20, 22, 24
700-8520	U4-U6, 8

5 TABLE II

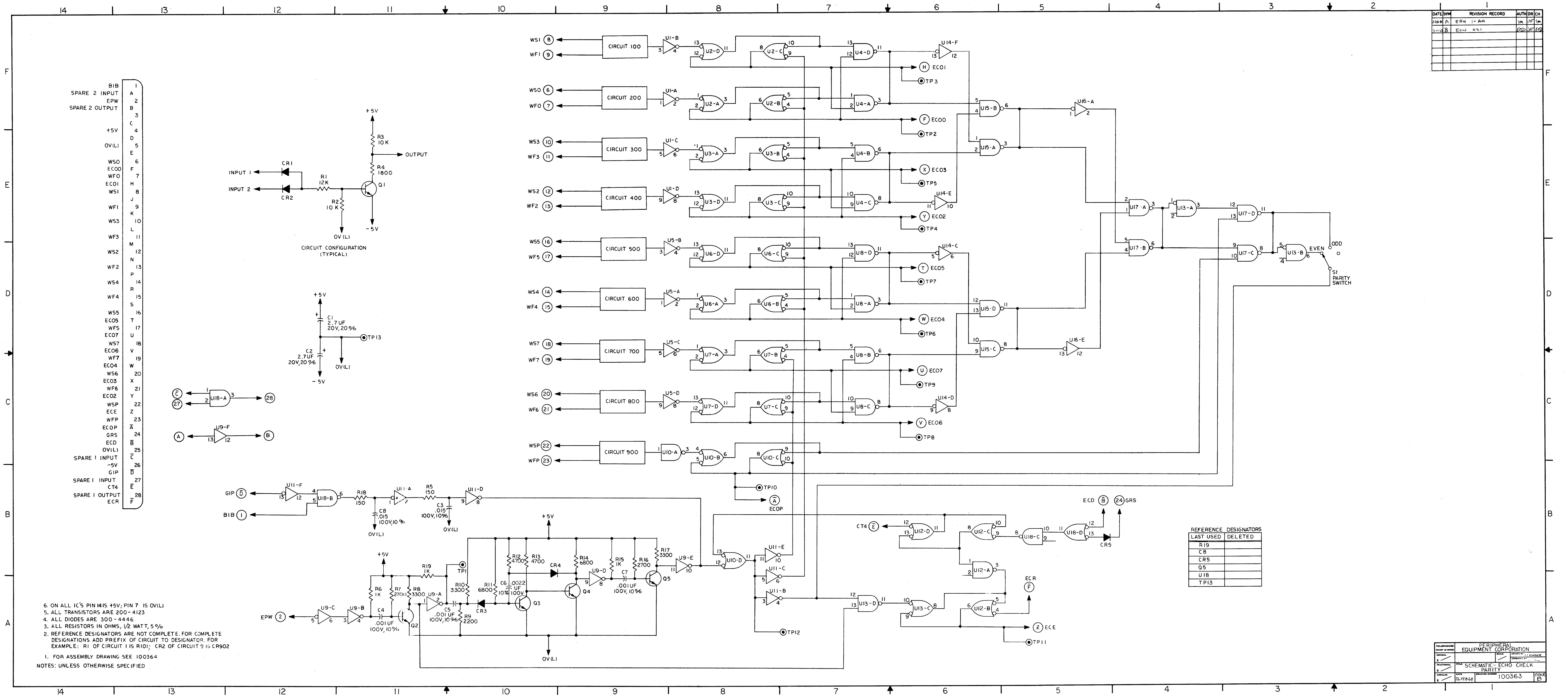
REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	9TK -01	7 TRACK -02	-03	-04	-05	-06	-07	-08	-09
R29,30,34,35,39,40,44,45, 49,50,54,55,69,70	101-3915	101-2715							
R59,60,64,65	101-3915								
R31,36,41,46,51,56,71	101-2225	101-1825							
R61,66	101-2225								
R57,58,62,63	101-1225								
W1	100373-01								
W2		100373-01							
Q16-19	200-4125								
U15,16	700-8450								
U7	700-8520								



5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.

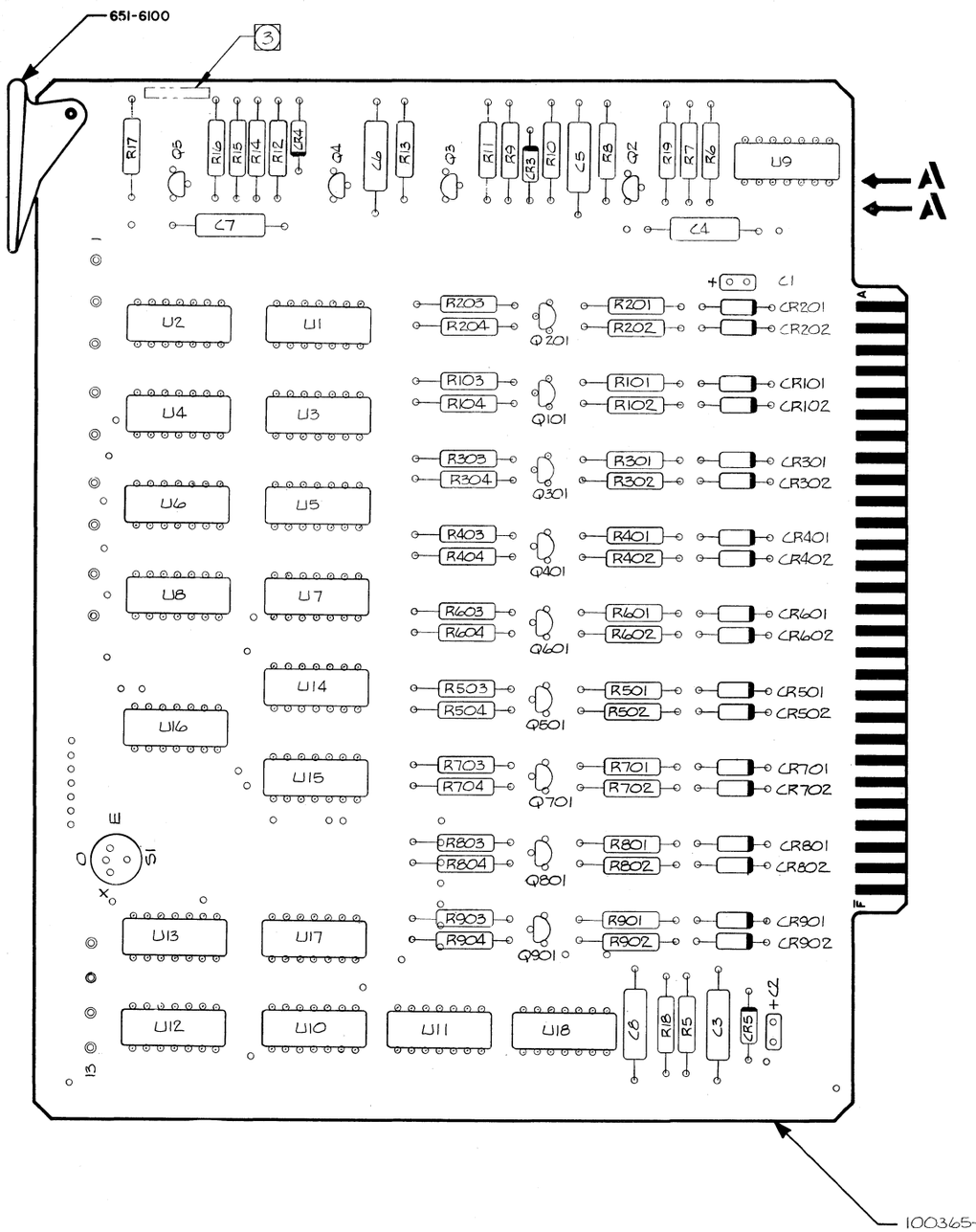
4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION	
DECIMAL ±	SCALE 2/1	DRAWN BY S. FICKEN
FRACTIONAL ±	TITLE PCBA-DOUBLE BUFFER 9 CHANNEL WRITE AMP.	APPROVED BY ERD
ANGULAR ±	DATE 7/10/68	DRAWING NUMBER 100239
		SHEET 1 OF 1
		ISSUE C



CIRCUIT 100
CIRCUIT 200
CIRCUIT 300
CIRCUIT 400
CIRCUIT 500
CIRCUIT 600
CIRCUIT 700
CIRCUIT 800
CIRCUIT 900
CIRCUIT CONFIGURATION (TYPICAL)
INPUT 1
INPUT 2
OUTPUT
S1 PARITY SWITCH
EVEN
ODD
REFERENCE DESIGNATORS
LAST USED | DELETED
R19
C8
CR5
Q5
U18
TP13
6. ON ALL IC'S PIN 14 IS +5V; PIN 7 IS OV(L)
5. ALL TRANSISTORS ARE 200-4123
4. ALL DIODES ARE 300-4446
3. ALL RESISTORS IN OHMS, 1/2 WATT, 5%
2. REFERENCE DESIGNATORS ARE NOT COMPLETE. FOR COMPLETE DESIGNATIONS ADD PREFIX OF CIRCUIT TO DESIGNATOR. FOR EXAMPLE: R1 OF CIRCUIT 1 IS R101; CR2 OF CIRCUIT 9 IS CR902
1. FOR ASSEMBLY DRAWING SEE 100364
NOTES: UNLESS OTHERWISE SPECIFIED
PERIPHERAL EQUIPMENT CORPORATION
SCHEMATIC - ECHO CHECK PARITY
DATE 26 FEB 68
DRAWING NUMBER 100363
ISSUE B

DATE	SYM	REVISION RECORD	AUTH.	DR.	CK.
8/68	A	ERN 1-EN	GJN		

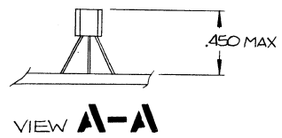


4 TABLE I

PART NO.	REF. DESIGNATION
101-1515	R5,18
101-1025	R6,15,19
101-1825	R104-904
101-2225	R9
101-2725	R7,16
101-3325	R8,17,10
101-4725	R12,13
101-6825	R11,14
101-1035	R102-R902,R103-R903
101-1235	R101-R901
131-1030	C4,5,7
131-2220	C6
131-1530	C3,8
132-2752	C1,2
200-4123	Q101-Q901, Q2-Q5
300-4446	CR101-901,102-902,3,4,5
574-8711	S1
700-8360	U1,5,9,11,14,16
700-8460	U2-4,6-8,10,12,13,15,17,18

TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VER.	-01	-02	-03	-04	-05	-06	-07	-08	-09



3 RUBBER STAMP PART NO, INCLUDING VERSION NO, AND LATEST ISSUE.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REF DWGS: SCHEMATIC-100363
SPEC-100367

NOTES: UNLESS OTHERWISE SPECIFIED

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSIONS, SEE TABLE I.

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL		SCALE 2/1	DRAWN BY G. FICKEN
FRACTIONAL	TITLE PCBA ECHO CHECK PARITY		SHEET 1 OF 1
ANGULAR	DATE 7/11/68	DRAWING NUMBER 100364	ISSUE A

REFERENCE DESIGNATORS	
LAST USED	DELETED
R27	
C11	
CR5	
Q6	
U33	
TP15	

VERSION TABLE [10]

ASSEMBLY	JUMPER
100265-01	W1
100265-02	W2

[10] SEE VERSION TABLE FOR APPLICABLE JUMPER.
9. ON ALL IC'S PIN 14 IS +5V, PIN 7 OV(L)
8. ALL INVERTERS 700-8360
7. ALL GATES 700-8460
6. ALL J/K FLIPFLOPS 700-8520
5. ALL PNP TRANSISTORS 200-412 , NPN 200-412
4. ALL DIODES ARE 300-4446
3. ALL CAPACITORS 100V, 10%
2. ALL RESISTORS IN OHMS, 1/2 WATT 5%
1. FOR ASSEMBLY DRAWING SEE 100265

NOTES: UNLESS OTHERWISE SPECIFIED

100265	TOP ASSY
NEXT ASSY	1ST USED ON
APPLICATION	

DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 X/X ± 1/32 ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. 010
FINISH:

SIGNATURES	DATE
DR GARY FICKEN	1/27/69
CHK J. THOMPSON	[illegible]
DES	
ENGR [illegible]	[illegible]
ENGR	

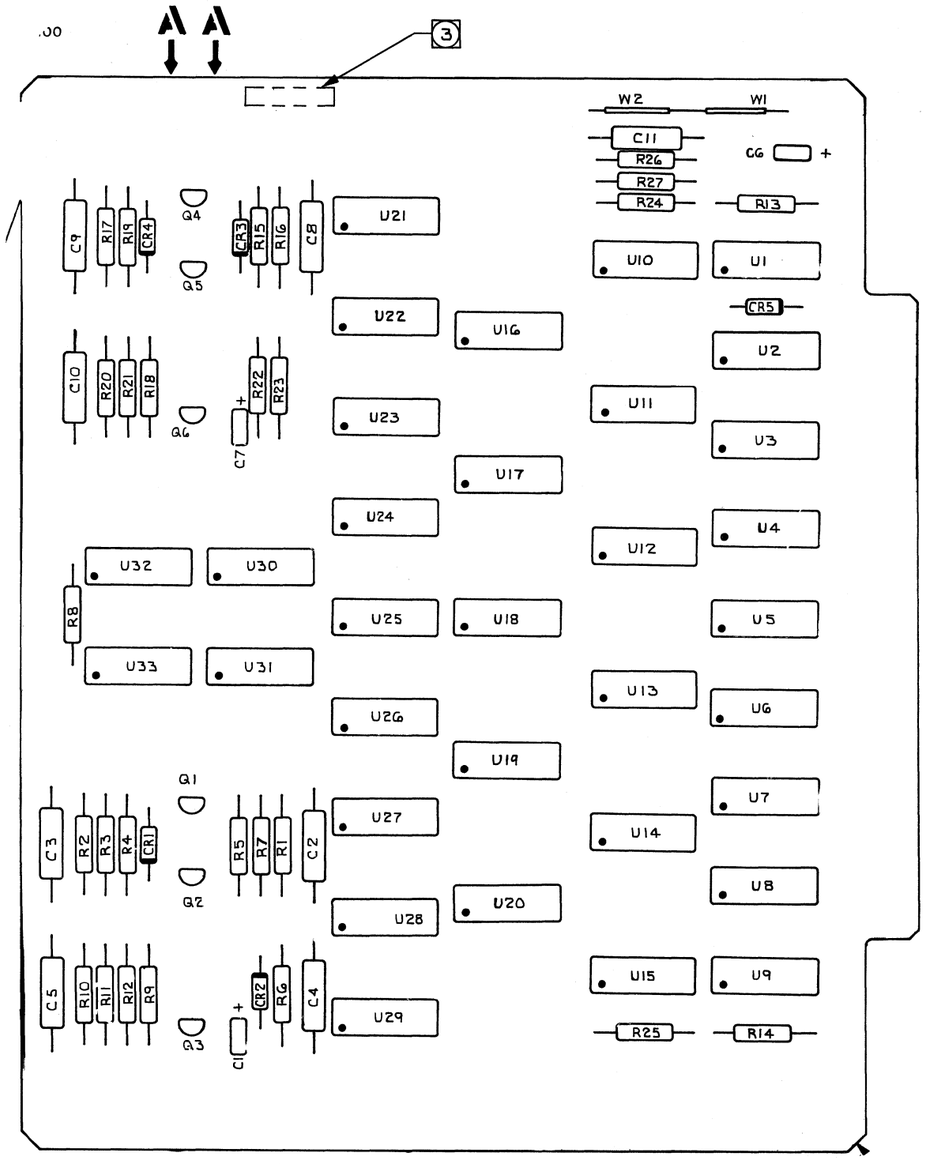
MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE
SCHEMATIC - CRC GENERATOR

SIZE H | CODE IDENT. NO. | DWG NO. 100264 | REV D
SCALE ~ | DO NOT SCALE DWG | SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
D	ECN 627	4-9-9	SV		



4 TABLE I

PART NO	REF. DESIGNATION
200-4123	Q1-6
300-4446	CR1-5
131-1020	C5,8,9,10,11
131-2220	C4
131-3320	C3
131-1530	C2
132-2752	C1,6,7
101-1515	R1
101-1025	R8,9,12,13,14,21,24,25
101-2225	R3,16
101-2725	R10,22
101-3325	R2,11,15,23,27
101-4725	R5,7,18,20
101-5625	R26
101-6825	R4,6,17,19
700-8360	U3,6,8,16-20,32,33
700-8440	U1,10
700-8460	U2,4,5,7,9,21-31
700-8520	U11-15

5 TABLE II

REFERENCE DESIGNATION	PART NUMBERS								
MODEL / VERSION	-01	-02	-03	-04	-05	-06	-07	-08	-09
W1	100373-01								
W2		100373-01							

5 FOR PART NO'S WHICH ARE AFFECTED BY VERSION NO, SEE TABLE II.

4 FOR PART NO'S WHICH ARE NOT AFFECTED BY VERSION NO., SEE TABLE I.

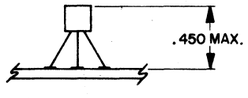
3 RUBBER STAMP PART NO., INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

1. REFERENCE DRAWINGS SCHEMATIC-100264
SPECIFICATION-100268

NOTES: UNLESS OTHERWISE SPECIFIED

100266-01



VIEW A-A

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
XX ± .010 ANGULAR ± ½°
XXX ± .005
X/X ± 1/32
BREAK ALL SHARP CORNERS
APPROX .010

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE

SIGNATURES	DATE
DR J.R. THOMPSON	3/6/69
CHK	
DES	
ENGR	3/6/69
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE PCBA
CRC GENERATOR

TOP ASSY	
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:

MATL:

SIZE	CODE IDENT NO	DWG NO.	REV
D		100265	D

SCALE 4/1 DO NOT SCALE DWG SHEET 1 OF 1

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 2-EK	[illegible]	[illegible]	WK	[illegible]
B	ECN 994	9/3/9	WK	[illegible]	[illegible]

5. REF DWGS: WL 100379, 100466, 100470.

(4) WIRING TO J207 IS ONLY INCLUDED ON TRANSPORTS WITH ECHO CHECK PARITY OPTION.

3. INTER-CAGE, INTERFACE, AND HEAD WIRING ONLY ARE SHOWN. FOR POWER AND CONTROLS WIRING SEE HARNESS WIRING DIAGRAM 100388.

2. ADJACENT CONNECTIONS ONLY ARE SHOWN.

1. ALL CONNECTORS ARE NOT USED IN SOME ASSEMBLIES.

NOTES: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	1ST USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES.
XX ± .010 ANGULAR ± 1/2°
XXX ± .005
X/X ± 1/32
BREAK ALL SHARP CORNERS APPROX .010

FINISH:

SIGNATURES		DATE
DR	[illegible]	[illegible]
CHK	W. Korp	[illegible]
DES		
ENGR	[illegible]	[illegible]
ENGR		

MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE WIRING DIAGRAM- SYNCHRONOUS WRITE DTL 9 TRACK

SIZE D | CODE IDENT NO | DWG NO. 101200 | REV B

SCALE | DO NOT SCALE DWG | SHEET 1 OF 1

5. REF DWGS: 100385, 100466, 100470.
④ WIRING TO J207 IS ONLY INCLUDED ON TRANSPORTS WITH ECHO CHECK PARITY OPTION.
3. INTER-CAGE, INTERFACE, AND HEAD WIRING ONLY ARE SHOWN. FOR POWER AND CONTROLS WIRING SEE HARNESS WIRING DIAGRAM 100388.
2. ADJACENT CONNECTORS ONLY ARE SHOWN.
1. ALL CONNECTORS ARE NOT USED IN SOME ASSEMBLIES.

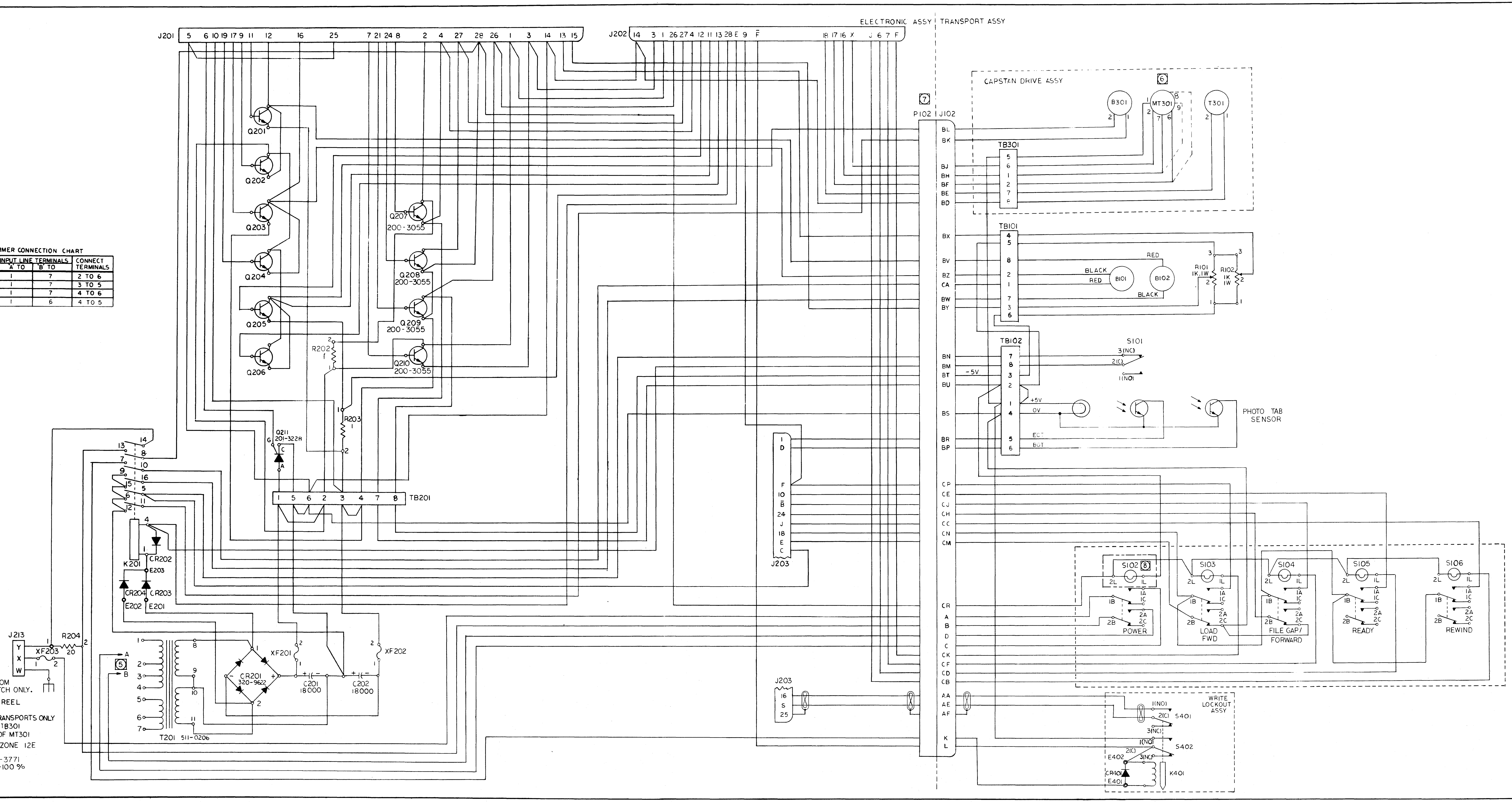
NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED	DIMENSIONS ARE IN INCHES; TOLERANCES XX ± .010, XXX ± .005, X/X ± 1/32; ANGULAR ± 1/2°; BREAK ALL SHARP CORNERS APPROX .010
COMPANY	PEC PERIPHERAL EQUIPMENT CORPORATION
TITLE	WIRING DIAGRAM- SYNCHRONOUS WRITE DTL 7 TRACK
SIZE	D
DWG NO.	101201
REV	A
SHEET	1 OF 1

DATE	SYM	REVISION RECORD	AUTH	DR	CH
2/13	A	ERN 1-AK	SM	JE	SM
3/19	B	ECN 020	SM	JE	SM
6/19	C	REVISED & REDRAWN ECN 116	SM	JE	WK
10-23	D	ECN 311	RL	JT	WK
31 Jan 69	E	ECN455 DELETED R201	RL	WK	RL
8/28/69	F	ECN509	RL	ML	JDP

TRANSFORMER CONNECTION CHART

LINE VOLTAGE	INPUT LINE TERMINALS 'A' TO	INPUT LINE TERMINALS 'B' TO	CONNECT TERMINALS
115 V	1	7	2 TO 6
200 V	1	7	3 TO 5
220 V	1	7	4 TO 6
240 V	1	6	4 TO 5



8. PORTION OF S102 ENCLOSED BY PHANTOM LINE USED WITH ALTERNATE ACTION SWITCH ONLY.
7. P102 & J102 IS SUPPLIED WITH 10-1/2 IN. REEL TRANSPORTS ONLY.
6. MT301 IS SUPPLIED WITH INCREMENTAL TRANSPORTS ONLY UNIT WILL BE SHIPPED WITH PINS 1&2 OF TB301 CONNECTED TO EITHER PINS 6&7 OR 8&9 OF MT301
5. SEE TRANSFORMER CONNECTION CHART, ZONE 12E
4. ALL DIODES ARE 300-4446
3. TRANSISTORS Q201 THRU Q206 ARE 200-3771
2. ALL CAPACITORS IN MICOFARADS, 26V, -10, +100 %
1. ALL RESISTORS IN OHMS, 20 WATT, 10 %

NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCES (EXCEPT AS NOTED)	PERIPHERAL EQUIPMENT CORPORATION		
DECIMAL ±		SCALE	DRAWN BY J ERINGER / APPROVED BY STU MABON
FRACTIONAL ±	TITLE SCHEMATIC - POWER AND HARNESS WIRING		
ANGULAR ±	DATE 12 FEB68	DRAWING NUMBER 100388	ISSUE E

APPENDIX A

GLOSSARY

GLOSSARY

Symbol	Description	Symbol	Description
BCD10	Binary Coded Decimal	DBY	Data Busy
BOTO	Beginning of Tape Output	DMC	Disable Manual Controls
CBY	Command Busy	ECC	Enable Check Character
CCS	Check Character Strobe	ECD	Echo Check Disable
CRC0	Cyclic Redundancy Check 0	ECE	Echo Check Error
CRC1	Cyclic Redundancy Check 1	ECR	Echo Check Reset
CRC2	Cyclic Redundancy Check 2	ECRC	Enable CRC
CRC3	Cyclic Redundancy Check 3	EEC	Enable Echo Check
CRC4	Cyclic Redundancy Check 4	EF	Erase Winding Finish
CRC5	Cyclic Redundancy Check 5	EFM	Enable File Mark
CRC6	Cyclic Redundancy Check 6	EOTO	End of Tape Output
CRC7	Cyclic Redundancy Check 7	EPNP	Encoder Pulse Narrow Powerful
CRCP	Cyclic Redundancy Check Parity	EPW	Encoder Pulse Wide
CT0	Center Tap 0	ES	Erase Winding Start
CT1	Center Tap 1	FGC	File Gap Command
CT2	Center Tap 2	FGL	File Gap Lamp
CT3	Center Tap 3	FGR	File Gap Ramp
CT4	Center Tap 4	GIP	Gap In Process
CT5	Center Tap 5	GRS	General Reset
CT6	Center Tap 6	IRGC	Inter-record Gap Command
CT7	Center Tap 7	LD	Lamp Driver
CTP	Center Tap Parity		

GLOSSARY (continued)

Symbol	Description	Symbol	Description
LFC	Load Forward Command	WDS	Write Data Strobe
LFR	Load Forward Ramp	WDSN	Write Data Strobe Narrow
RD	Relay Driver	WF0	Write Finish 0
RRS	Remote Reset	WF1	Write Finish 1
RWC	Rewind Command	WF2	Write Finish 2
RWR	Rewind Ramp	WF3	Write Finish 3
RYC	Ready Command	WF4	Write Finish 4
SFC	Synchronous Forward Command	WF5	Write Finish 5
SFCD	Synchronous Forward Command Delayed	WF6	Write Finish 6
TNT	Tape Not Tensioned	WF7	Write Finish 7
TRR	Transport Ready	WFP	Write Finish Parity
WCRC	Write CRC	WPC	Write Power Control
WD0	Write Data 0	WRP	Write Pulse
WD1	Write Data 1	WS0	Write Start 0
WD2	Write Data 2	WS1	Write Start 1
WD3	Write Data 3	WS2	Write Start 2
WD4	Write Data 4	WS3	Write Start 3
WD5	Write Data 5	WS4	Write Start 4
WD6	Write Data 6	WS5	Write Start 5
WD7	Write Data 7	WS6	Write Start 6
WDP	Write Data Parity	WS7	Write Start 7
		WSP	Write Start Parity

PEC