Service Manual

DV4100/A1B, /N1B, /S1G, /U1B

DVD Player

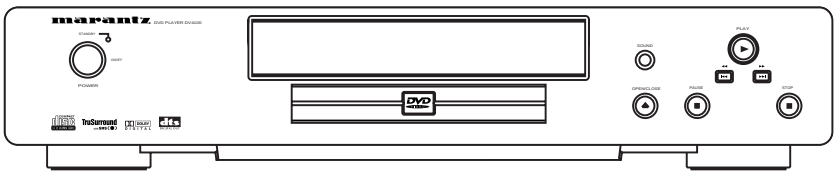


TABLE OF CONTENTS

Please use this service manual with referring to the user guide (D.F.U) without fail.

marantz®

DV4100

302W855010 AO
3120 785 22440
First Issue:2000.11

Printed in Japan

MARANTZ DESIGN AND SERVICE

Using superior design and selected high grade components, **MARANTZ** company has created the ultimate in stereo sound. Only original **MARANTZ** parts can insure that your **MARANTZ** product will continue to perform to the specifications for which it is famous.

Parts for your **MARANTZ** equipment are generally available to our National Marantz Subsidiary or Agent.

ORDERING PARTS :

Parts can be ordered either by mail or by Fax.. In both cases, the correct part number has to be specified.

The following information must be supplied to eliminate delays in processing your order :

1. Complete address
2. Complete part numbers and quantities required
3. Description of parts
4. Model number for which part is required
5. Way of shipment
6. Signature : any order form or Fax. must be signed, otherwise such part order will be considered as null and void.

USA

MARANTZ AMERICA, INC.
440 MEDINAH ROAD
ROSELLE, ILLINOIS 60172
USA
PHONE : 630 - 307 - 3100
FAX : 630 - 307 - 2687

EUROPE / TRADING

MARANTZ EUROPE B.V.
P.O.BOX 80002, BUILDING SFF2
5600 JB EINDHOVEN
THE NETHERLANDS
PHONE : +31 - 40 - 2732241
FAX : +31 - 40 - 2735578

BRAZIL

PHILIPS DA AMAZONIA IND. ELET. ITDA
CENTRO DE INFORMACOES AO
CEP 04698-970
SAO PAULO, SP, BRAZIL
PHONE : 0800 - 123123(Discagem Direta Gratuita)
FAX : +55 11 534. 8988

PROFESSIONAL **AMERICAS**

SUPERSCOPE TECHNOLOGIES, INC.
MARANTZ PROFESSIONAL PRODUCTS
2640 WHITE OAK CIRCLE, SUITE A
AURORA, ILLINOIS 60504 USA
PHONE : 630 - 820 - 4800
FAX : 630 - 820 - 8103

PROFESSIONAL **AUSTRALIA**

TECHNICAL AUDIO GROUP PTY, LTD
558 DARLING STREET,
BALMAIN, NSW 2041,
AUSTRALIA
PHONE : 61 - 2 - 9810 - 5300
FAX : 61 - 2 - 9810 - 5355

CANADA

LENBROOK INDUSTRIES LIMITED
633 GRANITE COURT,
PICKERING, ONTARIO L1W 3K1
CANADA
PHONE : 905 - 831 - 6333
FAX : 905 - 831 - 6936

AUSTRALIA

QualiFi Pty Ltd,
24 LIONEL ROAD,
MT. WAVERLEY VIC 3149
AUSTRALIA
PHONE : +61 - (0)3 - 9543 - 1522
FAX : +61 - (0)3 - 9543 - 3677

THAILAND

MRZ STANDARD CO.,LTD
746 - 754 MAHACHAI ROAD.,
WANGBURAPAPIROM, PHRANAKORN,
BANGKOK, 10200 THAILAND
PHONE : +66 - 2 - 222 9181
FAX : +66 - 2 - 224 6795

SINGAPORE

WO KEE HONG DISTRIBUTION PTE LTD
130 JOO SENG ROAD
#03-02 OLIVINE BUILDING
SINGAPORE 368357
PHONE : +65 858 5535 / +65 381 8621
FAX : +65 858 6078

NEW ZEALAND

WILDASH AUDIO SYSTEMS NZ
14 MALVERN ROAD MT ALBERT
AUCKLAND NEW ZEALAND
PHONE : +64 - 9 - 8451958
FAX : +64 - 9 - 8463554

TAIWAN

PAI- YUING CO., LTD.
6 TH FL NO, 148 SUNG KIANG ROAD,
TAIPEI, 10429, TAIWAN R.O.C.
PHONE : +886 - 2 - 25221304
FAX : +886 - 2 - 25630415

MALAYSIA

WO KEE HONG ELECTRONICS SDN. BHD.
SUITE 8.1, LEVEL 8, MENARA GENESIS,
NO. 33, JALAN SULTAN ISMAIL,
50250 KUALA LUMPUR, MALAYSIA
PHONE : +60 3 - 2457677
FAX : +60 3 - 2458180

JAPAN *Technical*

MARANTZ JAPAN, INC.
35- 1, 7- CHOME, SAGAMIONO
SAGAMIHARA - SHI, KANAGAWA
JAPAN 228-8505
PHONE : +81 42 748 1013
FAX : +81 42 741 9190

日本マランツ株式会社

本　社　〒228-8505
神奈川県相模原市相模大野7-35-1
営業本部　〒150-0022
東京都渋谷区恵比寿南1-11-9

KOREA

MK ENTERPRISES LTD.
ROOM 604/605, ELECTRO-OFFICETEL, 16-58,
3GA, HANGANG-RO, YONGSAN-KU, SEOUL
KOREA
PHONE : +822 - 3232 - 155
FAX : +822 - 3232 - 154

SHOCK, FIRE HAZARD SERVICE TEST :

CAUTION : After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom.

Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before it is return to the user/customer.

Ref. UL Standard No. 1492.

In case of difficulties, do not hesitate to contact the Technical Department at above mentioned address.

1. TECHHNICAL SPECIFICATIONS (/N1B)

PLAYBACK SYSTEM

DVD-Video
Video CD
CD (CD-R and CD-RW)

OPTICAL READOUT SYSTEM

Lasertype	Semiconductor AlGaAs
Numerical Aperture	0.60 (DVD) 0.45 (VCD/CD)
Wavelength	650 nm (DVD) 780 nm (VCD/CD)

DVD DISC FORMAT

Medium	Optical Disc	
Diameter	12cm (8cm)	
Playing time	One layer	2.15 h*
(12cm)	Dual layer	4 h*
	Two side Single layer	4.30 h*
	Two side Dual layer	8 h*

TV STANDARD	**EUROPE**	**USA**
	(PAL/50Hz)	(NTSC/60Hz)
Number of lines	625	525
Playback	Multistandard	(PAL/NTSC)

VIDEO FORMAT

DA Converter	10 bits
Signal handling	Components
Digital Compression	MPEG2 for DVD, MPEG1 for VCD

DVD

Horiz. Resolutio	720 pixels**	720 pixels**
Vertical Resolution	576 lines	480 lines

VCD

Horiz. Resolution	352 pixels	352 pixels
Vertical Resolution	288 lines	240 lines

VIDEO PERFORMANCE

Video output	1 Vpp into 75 ohm
S-Video output	Y: 1 Vpp into 75 ohm C: 0.3 Vpp into 75 ohm
RGB output	1 Vpp into 75 ohm
Black Level Shift	On/Off
Video Shift	Left/Right

AUDIO FORMAT

Digital	MPEG DTS/AC-3	Compressed Digital
	PCM	16, 20, 24 bits fs, 44.1, 48, 96 kHz

Analog Sound Stereo
Dolby Pro Logic downmix from AC-3 multi-channel sound
3D Sound for virtual 5.1 channel sound on 2 speakers

AUDIO PERFORMANCE

DA Converter	24 bits	
DVD	fs 96 kHz	4 Hz - 22kHz
	fs 48 kHz	4 Hz - 22 kHz
Video CD	fs 48 kHz	4 Hz - 22 kHz
CD	fs 44.1 kHz	4 Hz - 20 kHz
Signal-Noise (1kHz)		95 dB
Dynamic Range (1kHz)		90 dB
Crosstalk (1kHz)		110 dB
Distortion and Noise (1kHz)		85 dB

CONNECTIONS

SCART	Euroconnector 2x
S-Video Output	Mini DIN, 4 pins
Video Output	Cinch (yellow)
Audio L+R output	Cinch (white/red)
Digital Output	1 coaxial, 1 optical IEC958 for CDDA / LPCM IEC1937 for MPEG1/2, AC-3 and DTS

CABINET

Dimensions(w x h x d)	440 x 92 x 305 mm
Weight	Approx. 3.8 Kg

PACKAGE CONTENTS

DVD-Video Player
Remote Control & Batteries
AC Power cable
User Manual
SCART cable (Euroconnector)
Audio/Video cable

GENERAL FUNCTIONALITY

Stop / Play / Pause
Fast Forward / Backward
Time search
Step Forward / Backward
Slow
Title / Chapter / Track Select
Skip Next / Skip Previous
Repeat (Chapter / Title / All) or (Track / All)
A-B Repeat
Shuffle
Enhanced ease of use graphical interface
Perfect Still with digital multi-tap filter
Zoom (x1.33, x2, x4) with picture enhancement
3D Sound
Virtual jog shuttle
Audio and video bit rate indicator *(only available in certain countries)*

DVD FUNCTIONALITY

Multi-angle Selection
Audio Selection (1 out of max. 8 languages)
Subtitles Selection (1 out of max. 32 languages)
Aspect Ratio conversion (16:9, 4:3 Letterbox, 4:3 Pan Scan)
Parental Control and Disk Lock
Disc Menu support (Title Menu and Root Menu)
Resume (5 discs) after stop / standby
Screen Saver (Dim 75% after 15 min.)
Programming Titles/chapters with Favorite Selection

VIDEO CD FUNCTIONALITY

Playback Control for VCD 2.0 discs
Parental Control and Disc lock
Resume (5 discs) after stop / standby
Screen Saver (Dim 75% after 15 min.)
Programming Tracks with Favorite Selection

AUDIO CD FUNCTIONALITY

Time Display (Total / Track)
Full audio functionality with remote control
Programming with Favorite Track Selection

** typical playing time for movie with 2 spoken languages and 3 subtitle languages.*

*** equivalent to 500 lines on your TV*

Specifications subject to change without prior notice

(/A1B, /S1G, /U1B)

PLAYBACK SYSTEM
DVD-Video
Video CD
CD (CD-R and CD-RW)

OPTICAL READOUT SYSTEM

Lasertype	Semiconductor AlGaAs
Numerical Aperture	0.60 (DVD) 0.45 (VCD/CD)
Wavelength	650 nm (DVD) 780 nm (VCD/CD)

DVD DISC FORMAT

Medium	Optical Disc	
Diameter	12cm (8cm)	
Playing time	One layer	2.15 h*
(12cm)	Dual layer	4 h*
	Two side Single layer	4.30 h*
	Two side Dual layer	8 h*

TV STANDARD	EUROPE	USA
	(PAL/50Hz)	(NTSC/60Hz)
Number of lines	625	525
Playback	Multistandard	(PAL/NTSC)

VIDEO FORMAT

DA Converter	10 bits
Signal handling	Components
Digital Compression	MPEG2 for DVD, MPEG1 for VCD

DVD

Horiz. Resolution	720 pixels*	720 pixels**
Vertical Resolution	576 line	480 lines

VCD

Horiz. Resolution	352 pixel	352 pixels
Vertical Resolution	288 line	240 lines

VIDEO PERFORMANCE

Video output	1 Vpp into 75 ohm
S-Video output	Y: 1 Vpp into 75 ohm C: 0.3 Vpp into 75 ohm
Y	1 Vpp into 75 ohm
C_R	0.7 Vpp into 75 ohm
C_B	0.7 Vpp into 75 ohm
Black Level Shift	On/Off
Video Shift	Left/Right

AUDIO FORMAT

Digital	MPEG	Compressed
	DTS/AC-3	
	PCM	16, 20, 24 bits fs, 48, 96 kHz

Analog Sound Stereo
Dolby Pro Logic downmix from AC-3 multi-channel sound
3D Sound for virtual 5.1 channel sound on 2 speakers

AUDIO PERFORMANCE

DA Converter	24 bits	
DVD	fs 96 kHz	4 Hz - 44 kHz
	fs 48 kHz	4 Hz - 22 kHz
Video CD	fs 48 kHz	4 Hz - 22 kHz
CD	fs 44.1 kHz	4 Hz - 20 kHz
Signal-Noise (1kHz)		95 dB
Dynamic Range (1kHz)		90 dB
Crosstalk (1kHz)		110 dB
Distortion and Noise (1kHz)		85 dB

CONNECTIONS

S-Video Output	Mini DIN, 4 pins
Component Video	Y Cinch (green) U (C_R) Cinch (blue) V (C_B) Cinch (red)
Video Output	Cinch (yellow) 2x
Audio L+R output	Cinch (white/red) 2x
Digital Output	1 coaxial, 1 optical IEC958 for CDDA / LPCM IEC1937 for MPEG1/2, AC-3 and DTS

CABINET

Dimensions (w x h x d)	440 x 92 x 305mm
Weight	Approx. 3.8 Kg

PACKAGE CONTENTS
DVD-Video Player
Remote Control & Batteries
AC power cord
User Manual
Audio/Video cord

GENERAL FUNCTIONALITY
Stop / Play / Pause
Fast Forward / Backward
Time search
Step Forward / Backward
Title / Chapter / Track Select
Skip Next / Skip Previous
Repeat (Chapter / Title / All) or (Track / All)
A-B Repeat
Shuffle
Enhanced ease of use graphical interface
Perfect Still with digital multi-tap filter
Zoom (x1.33 x2. x4) with picture enhancement
3D Sound
Virtual Jog Shuttle
Audio and video bit rate indicator (only available in certain countries)

DVD FUNCTIONALITY
Multi-angle Selection
Audio Selection (1 out of max. 8 languages)
Subtitles Selection (1 out of max. 32 languages)
Aspect Ratio conversion (16:9, 4:3 Letterbox, 4:3 Pan Scan)
Parental Control and Disk Lock
Disc Menu support (Title Menu and Root Menu)
Resume (5 discs) after stop / standby
Screen Saver (Dim 75% after 15 min.)
Programming Titles/chapters with Favorite Selection

VIDEO CD FUNCTIONALITY
Playback Control for VCD 2.0 discs
Parental Control and Disc lock
Resume (5 discs) after stop / standby
Screen Saver (Dim 75% after 15 min.)
Programming Tracks with Favorite Selection

AUDIO CD FUNCTIONALITY
Time Display (Total / Track)
Full audio functionality with remote control
Programming with Favorite Track Selection

* typical playing time for movie with 2 spoken languages and 3 subtitle languages.
** equivalent to 500 lines on your TV

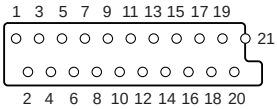
Specifications subject to change without prior notice

2. CONNECTION FACILITIES

SCART (/N1B versions only)

Full according PQR3 IMS
Connector implementation according EN50049-1; color = black; dual SCART
Fully according to prEN1057-2-1
Signal switching is P50 controlled; supported features of mode 3 see survey of applicable standards.

2-1 Video performance (/N1B only)



2-1-1 SCART II (connected to TV)

Pin signals:

1	Output	Audio R	1.8V RMS
2	Input	Audio R	
3	Output	Audio L	1.8V RMS
4		Audio GND	
5		Blue/Chroma GND	
6	Input	Audio L	
7	Bi-dir	Blue out/Chroma in	0.7pp +/-0.1V into 75 Ohm (*)
8	Output	Function switch	<2V = TV >4.5V / <7V = asp. ratio 16:9 DVD >9.5V / <12V = asp. ratio 4:3 DVD
9		Green GND	
10		Bi-dir P50 control	
11	Output	Green	0.7Vpp +/-0.1V into 75 Ohm (*)
12		not connected	
13		Red/Chroma GND	
14		fast switch GND	
15	Output	Red out/Chroma out	0.7Vpp +/-0.1V into 75 Ohm (*) +/-3dB 0.3Vpp in case of Chroma
16	Output	fast switch RGB /CVBS or Y	>1V / <3V into 75 Ohm = RGB 0.4V into 75 Ohm = CVBS
17		Y/CVBS GND	
18		fast switching GND	
19	Output	CVBS/Y/RGB sync	1Vpp +/-0.1V into 75 Ohm (*)
20	Input	CVBS/Y	
21		Shield	

SCART I (connected to AUX)

Pin signals:

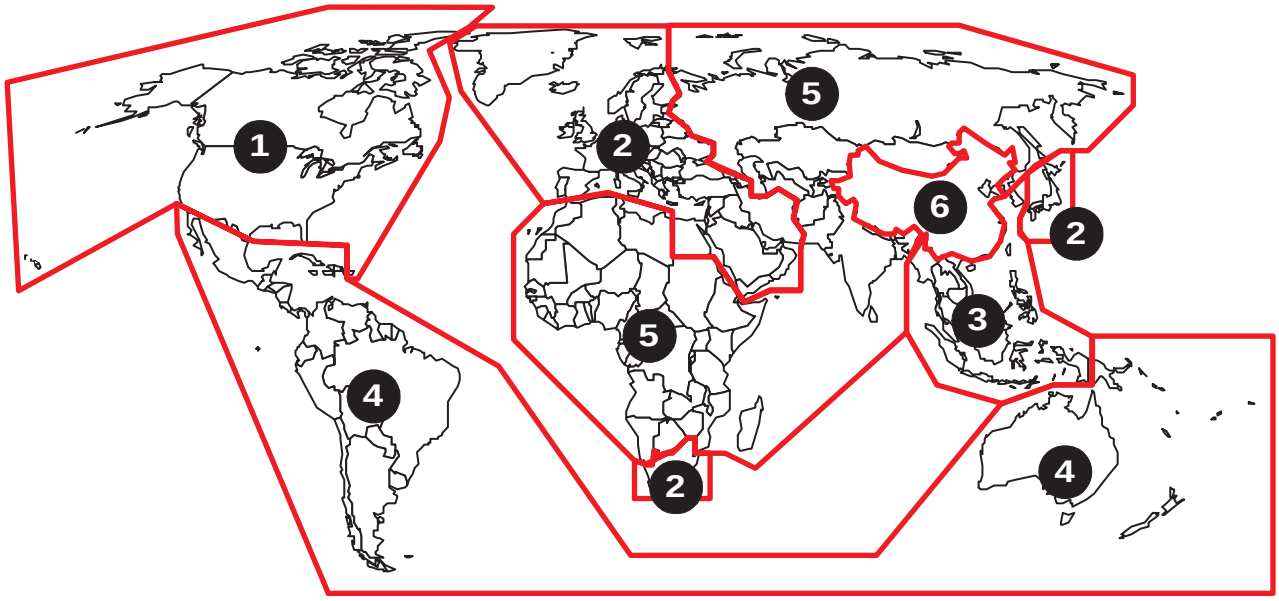
1	Output	Audio R	1.8V RMS
2	Input	Audio R	
3	Output	Audio L	1.8V RMS
4		Audio GND	
5		Blue/Chroma GND	
6	Input	Audio L	
7	Bi-dir	Blue in/Chroma out	+/-3dB 0.3Vpp Chroma
8	Input	Function switch	
9		Green GND	
10	Bi-dir	P50 control	
11	Input	Green	
12		not connected	
13		Red/Chroma GND	
14		fast switch GND	
15	Input	Red in/Chroma in	
16	Input	fast switch RGB/CVBS or Y	
17		CVBS GND	
18		fast switching GND	
19			
20	Input	CVBS/Y	
21		Shield	

(*) for 100% white

What are "regional codes"?

Motion picture studios want to control the home release of movies in different countries because theater releases arenít simultaneous (a movie may come out on DVD in the US when itís just hitting screens in Europe). Therefore they have required that the DVD standard include codes which can be used to lock out the playback of certain discs in certain geographical regions. Players sold in each region will have that regionís code built into the player. The player will refuse to play these "region coded" discs which are not allowed in the region. However, regional codes are entirely optional. Discs without codes will play on any player in any country. Some studios have already announced that only their new releases will have regional codes. There are six regions:

1. United States and Canada
2. Europe and Japan
3. Far East (except Japan & China)
4. South America and Oceania
5. Africa and the Middle East
6. China (except Hong Kong)



Map of DVD Regions

3. INFORMATIONS

REGION CODE

VERSION	REGION CODE	COUNTRY
/N1B	2	EUROPE
/S1G	3	ASIAN PACIFIC
/U1B	1	USA/CANADA
/A1B	4	AUSTRALIA

THE DISCS THAT THE DV4100 CAN HANDLE

The following discs can be played back with a DV4100.

disc	mark	playback capability	size	side
DVD	DVD VIDEO	Audio/Video	12 cm 8 cm	single/double
CD	COMPACT disc DIGITAL AUDIO	Audio	12 cm 8 cm	single
VCD	COMPACT disc DIGITAL VIDEO VIDEO CD	Audio/Video	12 cm 8 cm	single

Note: The regional code of the discs must meet to the regional code of the DV4100.

DVD INFORMATION

Below is a glossary of the new terms related to DVD.

Title:

A disc may have more than one story/movie on it, so each story/movie is called a “title”.
For example, if there are 2 movies on the disc, they are separated into Title 1 and Title 2.

Chapter:

A title may also be separated into chapters.
For example, a movie (title) may be separated into 3 scenes (chapters).

Title 1			Title 2		
Chapter 1	Chapter 2	Chapter 3	Chapter 1	Chapter 2	Chapter 3

Subtitles:

DVDs are recorded with up to 32 different subtitle languages. If a disc has more than one subtitle language, you can select the subtitle language that you want to read.

Soundtrack language:

DVDs are recorded with up to 8 different soundtrack languages. If a disc has more than one language, you can select the soundtrack language that you want to listen to.

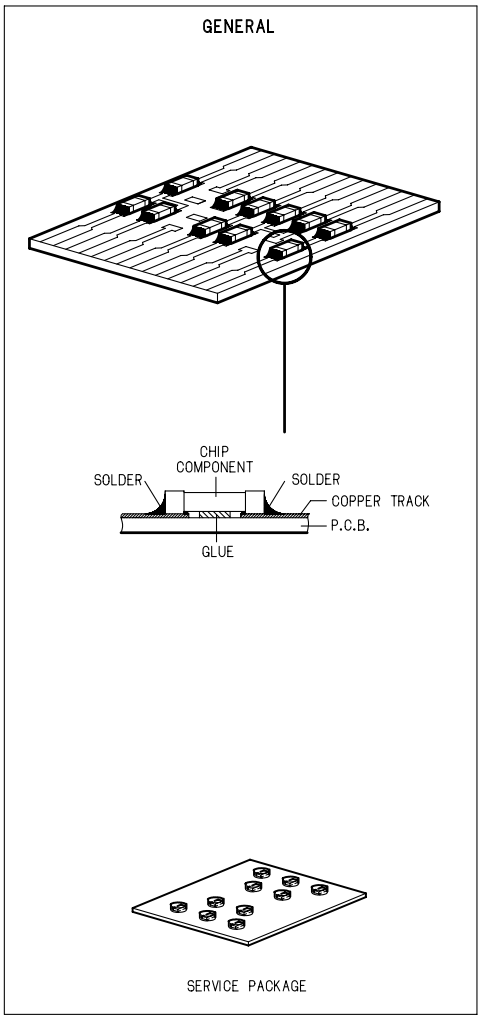
Multi-angles:

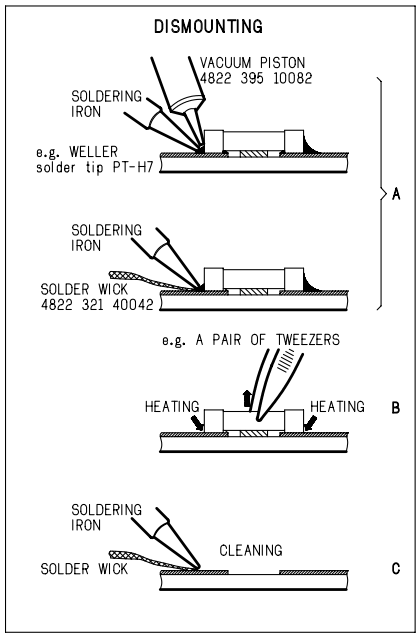
On some DVDs, scenes have been filmed from different angles (up to a maximum of 9). On these discs, you can select the angle that you want to watch. Please refer to the DVD’s manual to see which scenes have multi-angles.

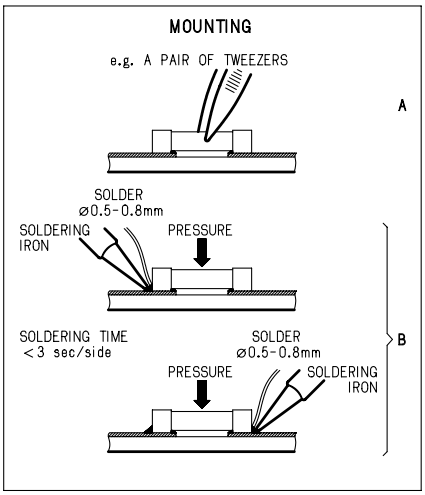
∗ It is important to note that CD-R, CD-RW discs must be FINALIZED before they can be played on this player. The disc types which run on the player feature one or more of these logos on the disc packaging.

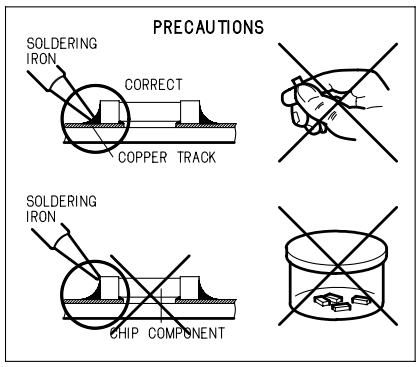
4. SERVICING HINT

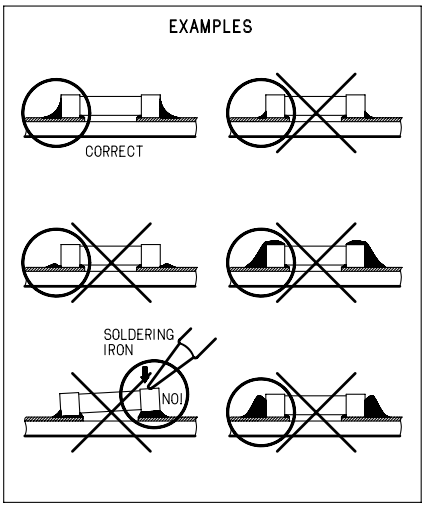
SERVICE HINTS











SERVICE TOOLS

Audio signals disc	4822 397 30184
Disc without errors (SBC444)+	
Disc with DO errors, black spots and fingerprints (SBC444A)	4822 397 30245
Disc (65 min 1kHz) without no pause	4822 397 30155
Max. diameter disc (58.0 mm)	4822 397 60141
Torx screwdrivers	
Set (straight)	4822 395 50145
Set (square)	4822 395 50132
13th order filter	4822 395 30204
DVD test disc	4822 397 10131
TEST software for PC : ComPair V1. 2	4822 727 21634
ComPair V1. 3	4822 727 21637
Connection Cable	3122 785 90017

5. WARNING AND LASER SAFETY INSTRUCTIONS

GB **WARNING**

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD).
Careless handling during repair can reduce life drastically.
When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.
Keep components and tools also at this potential.

NL **WAARSCHUWING**

Alle IC's en vele andere halfgeleiders zijn gevoelig voor elektrostatische ontladingen (ESD).
Onzorgvuldig behandelen tijdens reparatie kan de levensduur drastisch doen verminderen.
Zorg ervoor dat u tijdens reparatie via een polsband met weerstand verbonden bent met hetzelfde potentiaal als de massa van het apparaat.
Houd componenten en hulpmiddelen ook op ditzelfde potentiaal.

F **ATTENTION**

Tous les IC et beaucoup d'autres semi-conducteurs sont sensibles aux décharges statiques (ESD).
Leur longévité pourrait être considérablement écourtée par le fait qu'aucune précaution n'est prise a leur manipulation.
Lors de réparations, s'assurer de bien être relié au même potentiel que la masse de l'appareil et enfiler le bracelet serti d'une résistance de sécurité.
Veiller a ce que les composants ainsi que les outils que l'on utilise soient également a ce potentiel.

D **WARNUNG**

Alle IC und viele andere Halbleiter sind empfindlich gegen elektrostatische Entladungen (ESD).
Unsorgfältige Behandlung bei der Reparatur kann die Lebensdauer drastisch vermindern.
Sorgen sie dafür, das Sie im Reparaturfall über ein Pulsarmband mit Widerstand mit dem Massepotential des Gerätes verbunden sind.
Halten Sie Bauteile und Hilfsmittel ebenfalls auf diesem Potential.

I **AVVERTIMENTO**

Tutti IC e parecchi semi-conduttori sono sensibili alle scariche statiche (ESD).
La loro longevita potrebbe essere fortemente ridatta in caso di non osservazione della piu grande cauzione alla loro manipolazione.
Durante le riparazioni occorre quindi essere collegato allo stesso potenziale che quello della massa dell'apparecchio tramite un braccialetto a resistenza.
Assicurarsi che i componenti e anche gli utensili con quali si lavora siano anche a questo potenziale.

GB

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

NL

Veiligheidsbepalingen vereisen, dat het apparaat in zijn oorspronkelijke toestand wordt terug gebracht en dat onderdelen, identiek aan de gespecifieerde worden toegepast.

D

Bei jeder Reparatur sind die geltenden Sicherheitsvorschriften zu beachten.
Der Originalzustand des Gerats darf nicht verandert werden.
Fur Reparaturen sind Original-Ersatzteile zu verwenden.

I

Le norme di sicurezza esigono che l'apparecchio venga rimesso nelle condizioni originali e che siano utilizzati pezzi di ricambiago idetici a quelli specificati.

F

Les normes de sécurité exigent que l'appareil soit remis a l'état d'origine et que soient utilisées les pièces de rechange identiques à celles spécifiées.

SHOCK, FIRE HAZARD SERVICE TEST:

CAUTION: After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom,
Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before return to user/customer.
Ref.UL Standard NO.1492.

NOTE ON SAFETY:

Symbol ⚠ : Fire or electrical shock hazard. Only original parts should be used to replace any part with symbol ⚠
Any other component substitution(other than original type), may increase risk or fire or electrical shock hazard.

LASER SAFETY

This unit employs a laser. Only a qualified service person should remove the cover or attempt to service this device, due to possible eye injury.

LASER DEVICE UNIT

Type:	SemiconductorlaserGaAlAs
Wave length:	650 nm (DVD)
	780 nm (VCD/CD)
Output Power:	7 mW (DVD)
	10 mW (VCD/CD)
Beam divergence:	60 degree

USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURE OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.

AVOID DIRECT EXPOSURE TO BEAM

WARNING

The use of optical instruments with this product will increase eye hazard.
Repair handling should take place as much as possible with a disc loaded inside the player

WARNING LOCATION: INSIDE ON LASER COVERSHIELD

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN
VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN
VARO! AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN
VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETSEN
DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

Warning forpowersupply on position1005

The primary side of the powersupplyincluding the heatsink carries live mains voltage when the player is connected to the mains even when the player is swiched off !
This primary area is not shielded so it is possible to touch copper tracks and/or components when servicingthe player. Service personel have to take precautions to prevent touchingthis area or components in this area .
The primary side of the powersupply has been indicated with a lightning stroke and a stripe-marked printed onthe printedwiring board

Note:
The screws on the basic Engine (position 218 in on the exploded view drawing) may never be touched removed or re-adjusted.
Handle the Basic engine with care when the unit has to be exchanged!
The mechanism of the basic engine is very sensative for droping or shocks

6. SERVICE HINTS

6.1 DVD-Module 218

The DVD mechanism has to be exchanged completely in case of failure. A new or repaired mechanism can be ordered with codenumber 9305 023 61001.
Return the defective unit complete assembled in original package to Philips Consumer Service in Eindhoven.

The monoboard has to be repaired on component level.

6.2 Diagnostic software

In chapter “Diagnostic software” some tests are refering to the SCART functionality.
These tests are for sets with RGB-output.

For sets without RGB-output no SCART connector is mounted.
In these sets the SCART tests will automatically be skipped

6.3 Power Supply options

3122 427 21750		**3122 427 21370**		**3122 427 21760**	
110V USA		220V Europe China		Multi voltage A/P	
2261	CAP 330pF	2121	ELCO 100uF 385V	2261	CAP 330pF
2121	ELCO 150uF 250V			2121	ELCO 150uF 400V
3133	Resistor 10M				

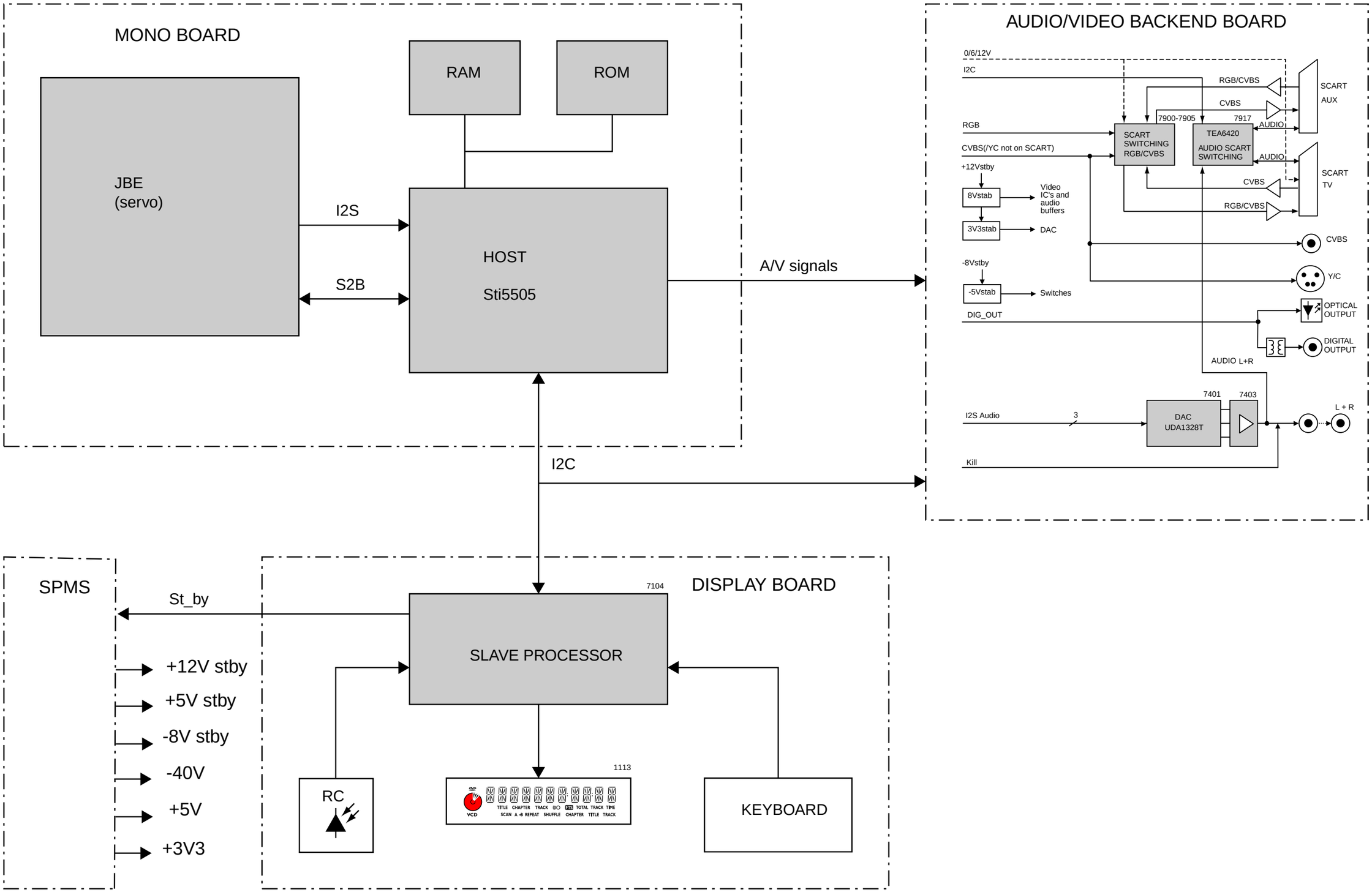
6.4 Compair

For assistance with the repair process of the monoboard an electronic Fault finding guidance has been developed , this program is called COMPAIR.
This COMPAIR program is available on CDROM.
The Version of the CDROM for repair of the monoboard is V1.3 and can be ordered with codenumber : 4822 727 21637.
This is an update CDROM , so when the COMPAIR CDROM is used for the first time , one has to install the COMPAIR ENGINE CDROM V1.2 first.
The V1.2 CDROM can be ordered with codenumber 4822 727 634 and has to registered after installation , the procedure for registration is explained in the help file of the program and in the booklet from the CDROM.
The cable to connect the monoboard with a PC can be ordered with codenumber 3122 785 90017.
All the hardware and software requirements of the systems necessary for working with COMPAIR is described on the CDROM.

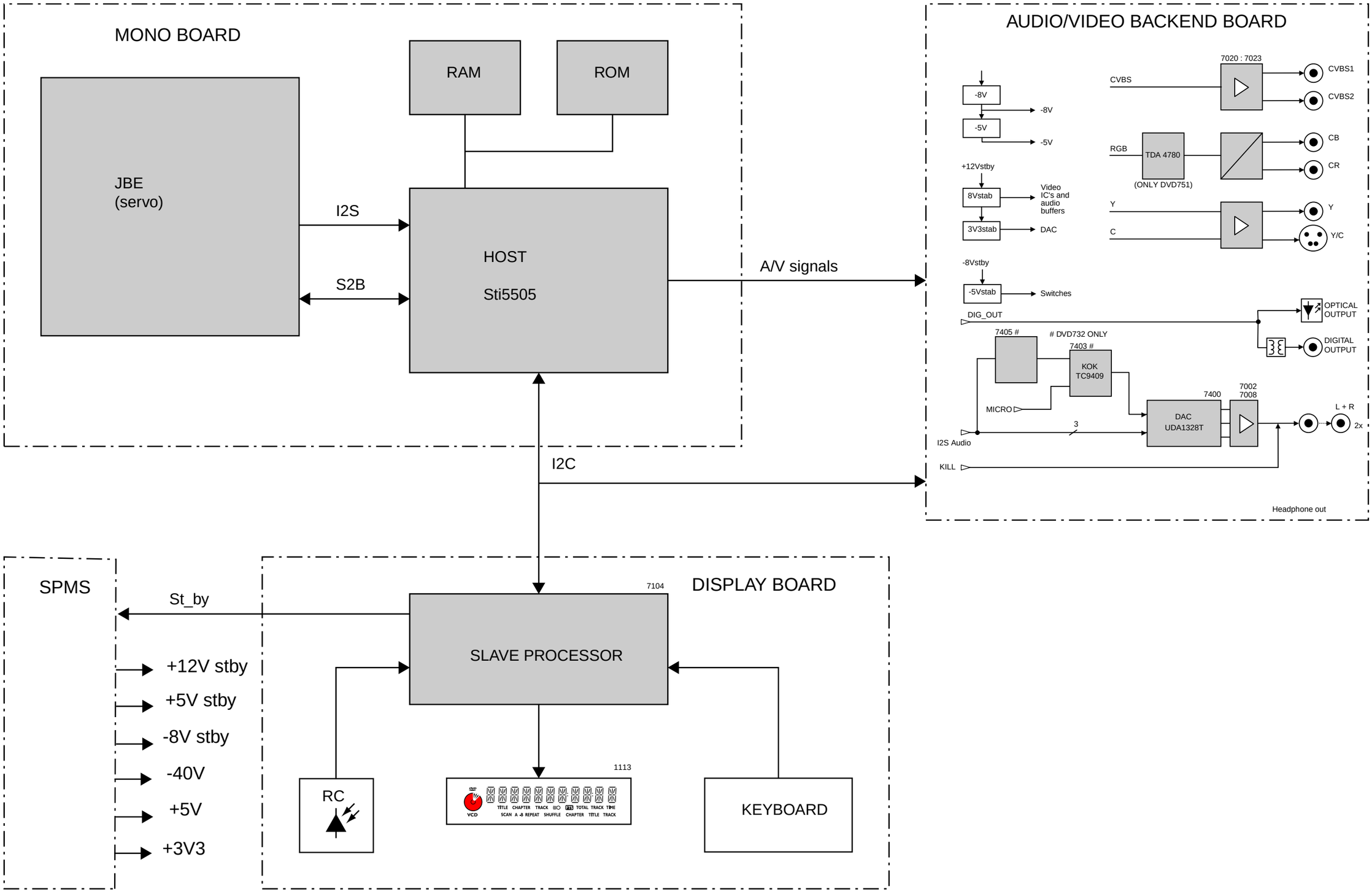
6.5 Monoboard repair

For repair of the monoboard the service manual 3122 785 10045 must be used.

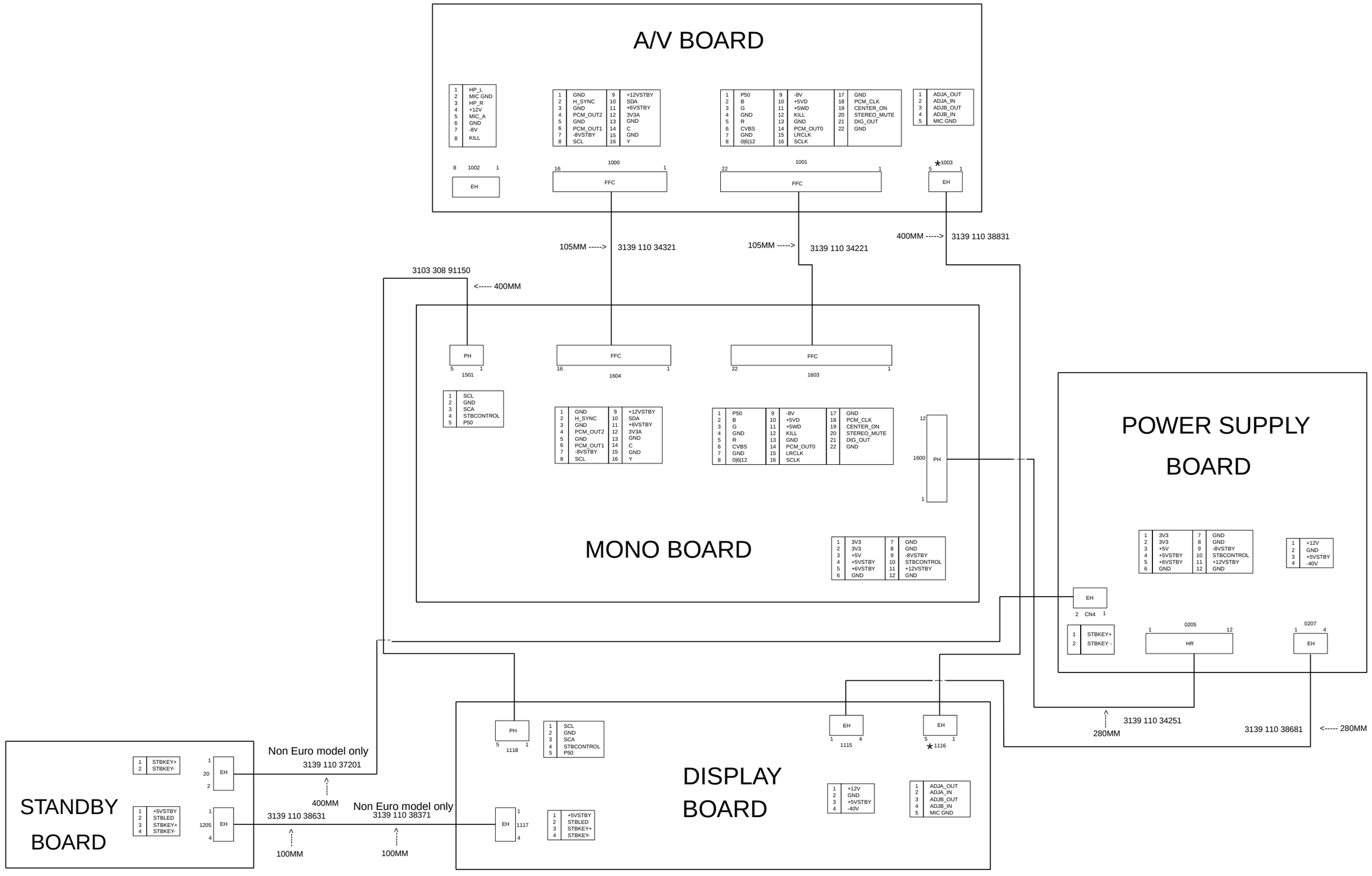
7. BLOCK DIAGRAM (/N1B)



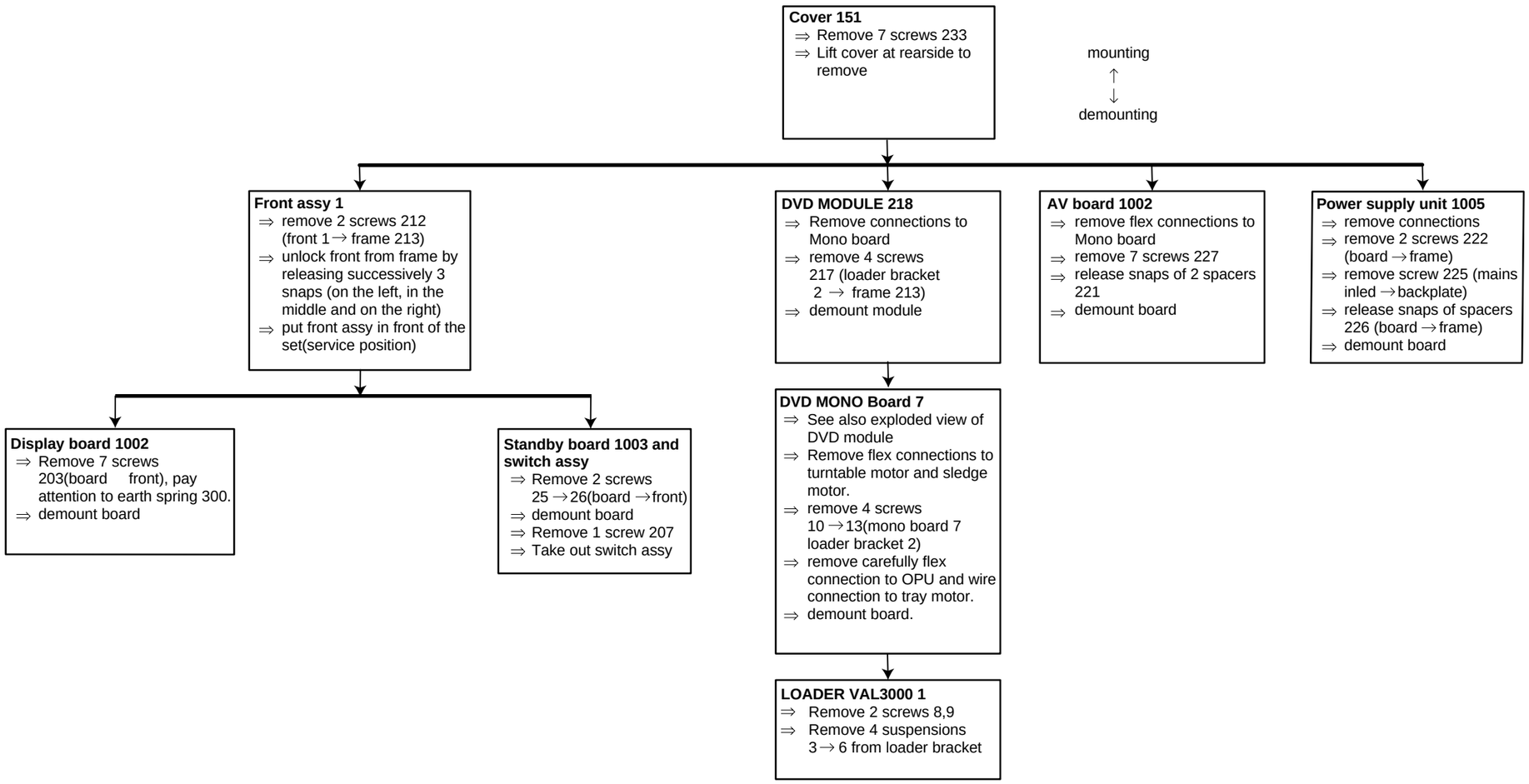
(/A1B, /S1G, /U1B)


MONO BOARD
RAM
ROM
JBE
(servo)
I2S
S2B
HOST
Sti5505
A/V signals
I2C
AUDIO/VIDEO BACKEND BOARD
-8V
-8V
-5V
-5V
+12Vstby
8Vstab
Video IC's and audio buffers
3V3stab
DAC
-8Vstby
-5Vstab
Switches
DIG_OUT
OPTICAL OUTPUT
DIGITAL OUTPUT
7405 #
DVD732 ONLY
7403 #
KOK TC9409
MICRO
I2S Audio
3
DAC UDA1328T
7400
7002
7008
L + R
2x
KILL
Headphone out
7020 : 7023
CVBS
CVBS1
CVBS2
RGB
TDA 4780
(ONLY DVD751)
CB
CR
Y
C
Y
Y/C
SPMS
St_by
+12V stby
+5V stby
-8V stby
-40V
+5V
+3V3
DISPLAY BOARD
7104
SLAVE PROCESSOR
RC
1113
KEYBOARD

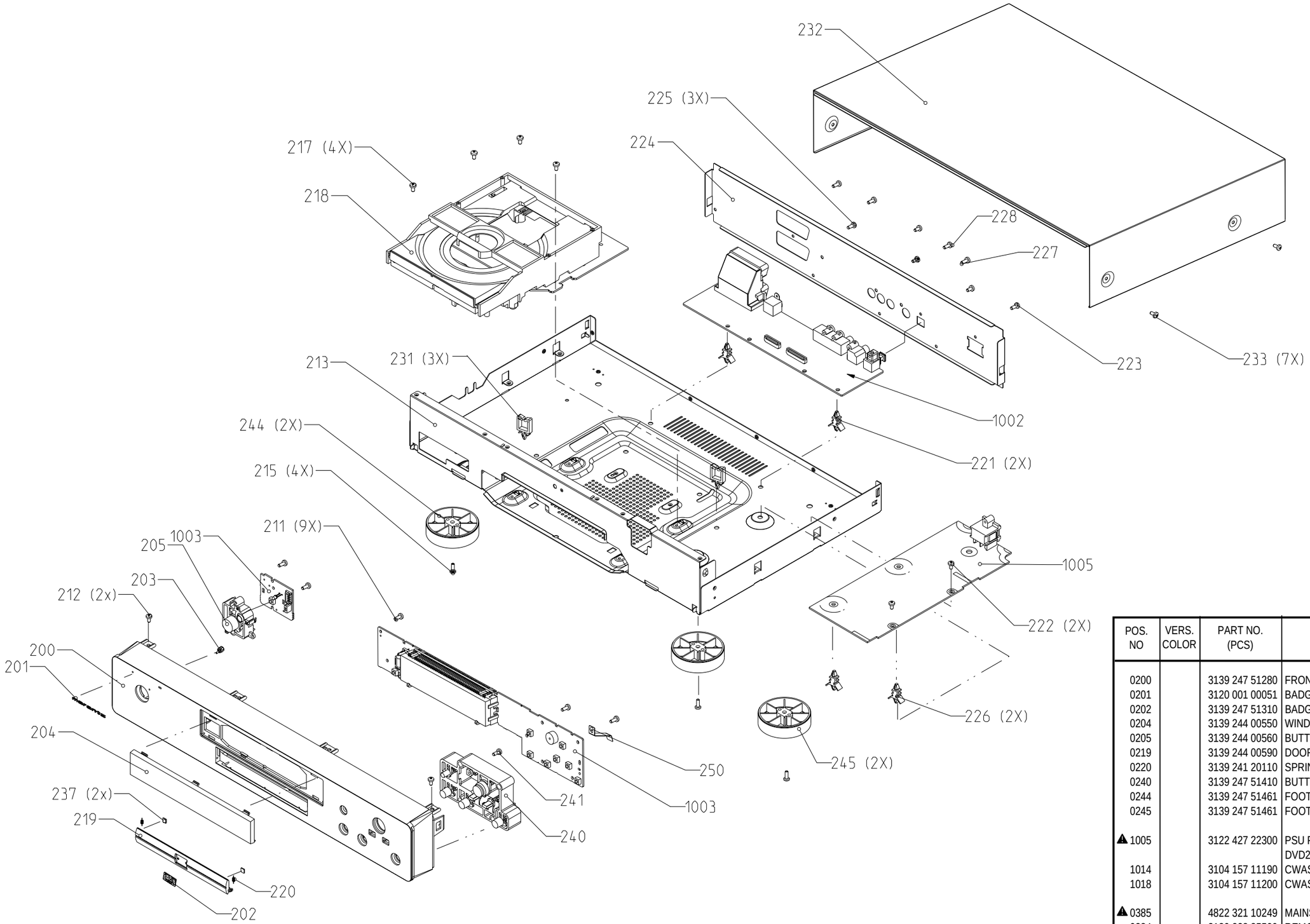
8. WIRING DIAGRAM



9. DISMANTLING INSTRUCTIONS

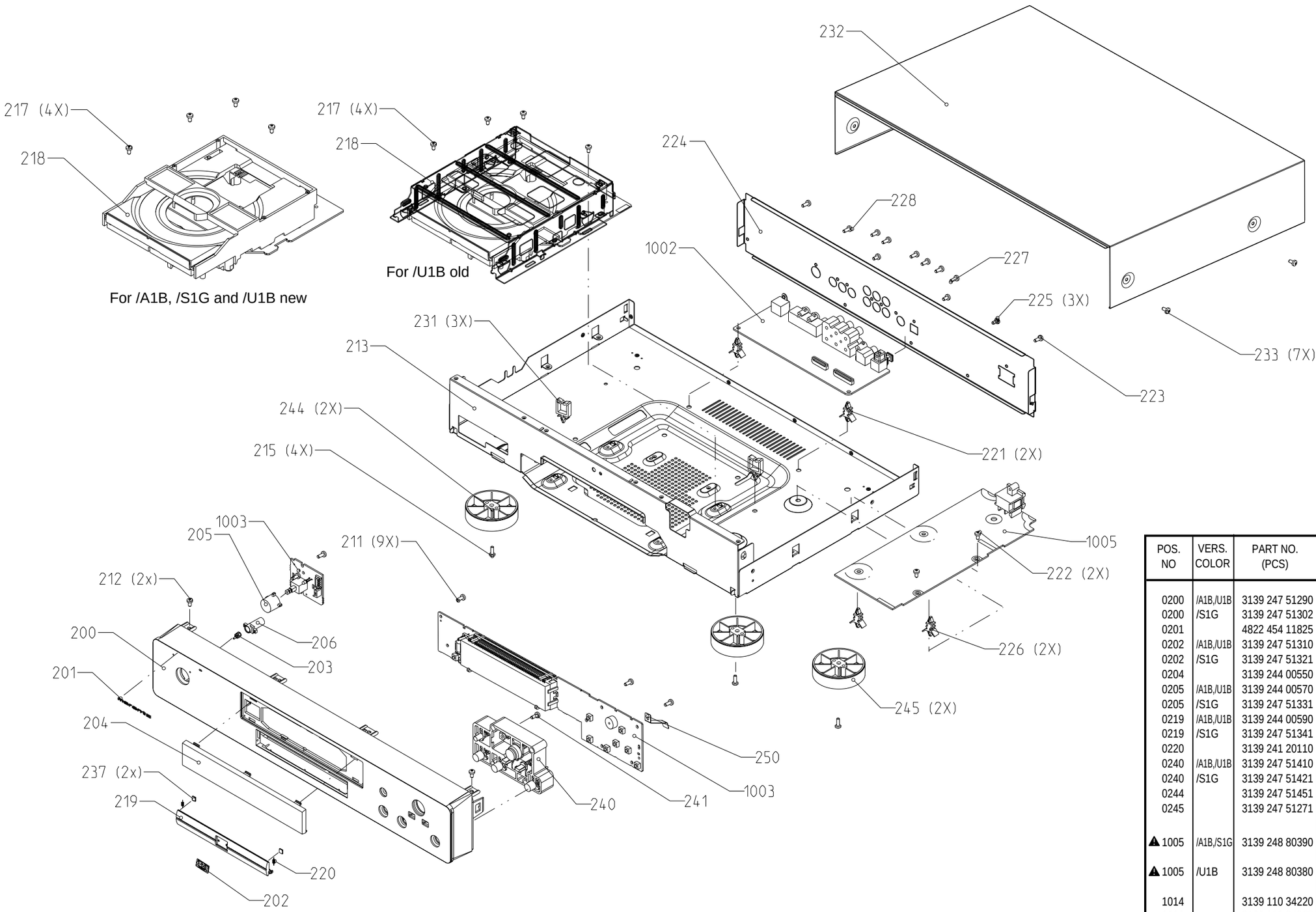


10. EXPLODED VIEW AND PARTS LIST (/N1B)



POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
0200		3139 247 51280	FRONT PANEL (BLACK)	QT24751280
0201		3120 001 00051	BADGE MARANTZ	QZ00100051
0202		3139 247 51310	BADGE DVD	QT24751310
0204		3139 244 00550	WINDOW	QT24400550
0205		3139 244 00560	BUTTON STANDBY	QT24400560
0219		3139 244 00590	DOOR	QT24400590
0220		3139 241 20110	SPRING DOOR	QT24120110
0240		3139 247 51410	BUTTON CONTROL	QT24751410
0244		3139 247 51461	FOOT	QT24751461
0245		3139 247 51461	FOOT	QT24751461
⚠ 1005		3122 427 22300	PSU PCB ASSY DVD2B+ 20PS223	
1014		3104 157 11190	CWAS FLEX DVD 22 130 32S	QW15711190
1018		3104 157 11200	CWAS FLEX DVD 16 130 32S	QW15711200
⚠ 0385		4822 321 10249	MAINS CORD	QP32110249
0384		3139 228 85500	REMOTE CONTROL	QT22885500
0387		3139 246 10340	USER GUIDE (/N1B)	QT24610340

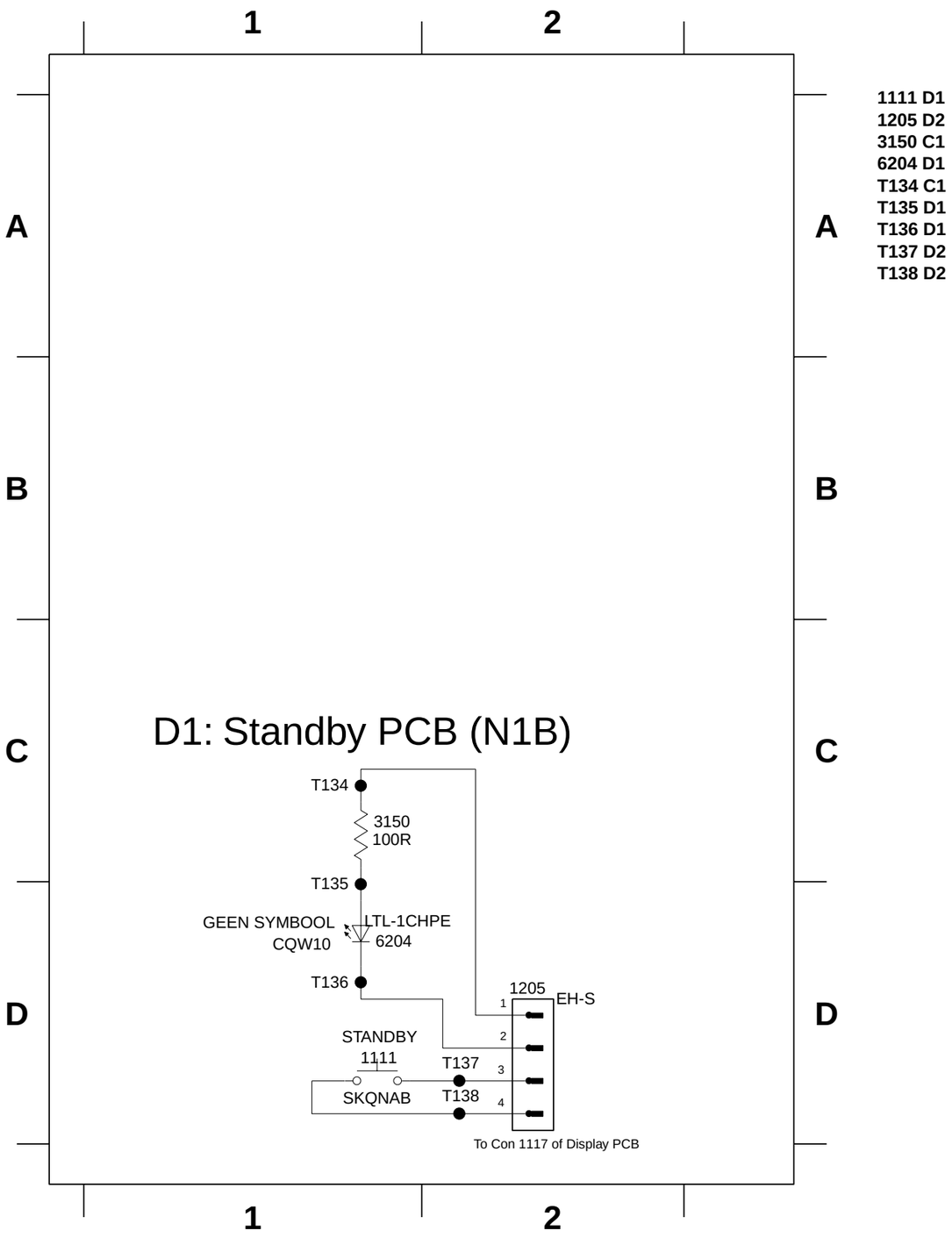
(/A1B, /S1G, /U1B)

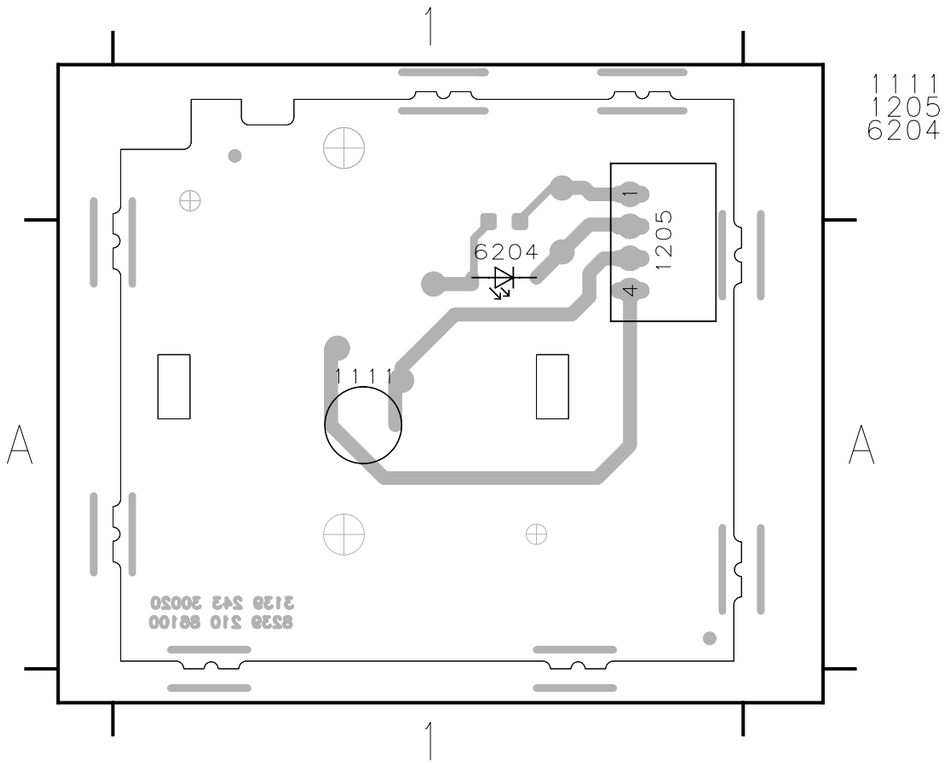


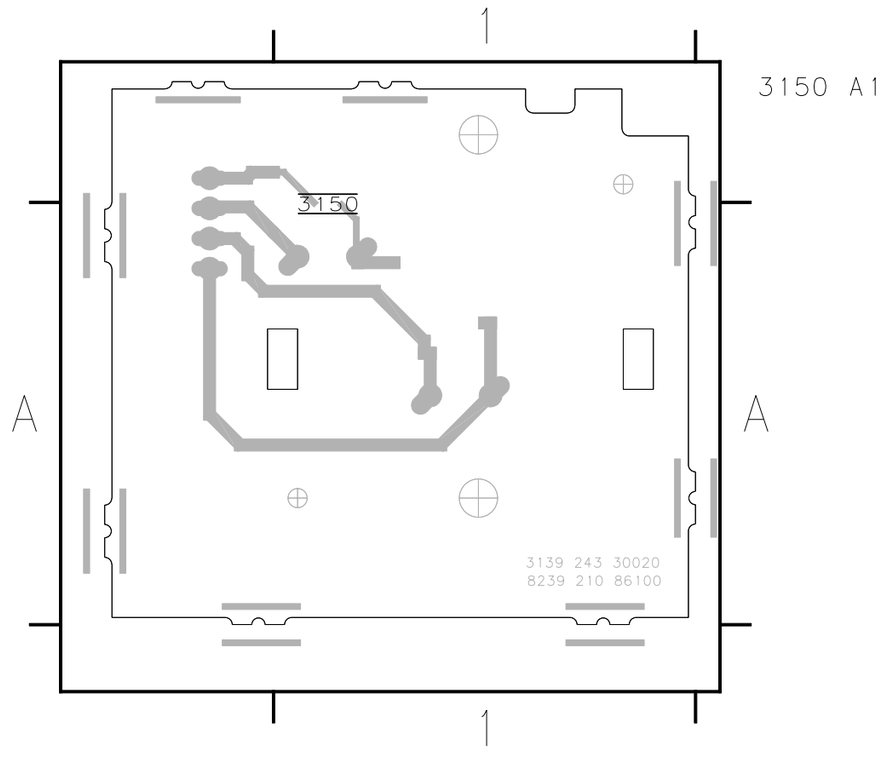
POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
0200	/A1B,/U1B	3139 247 51290	FRONT PANEL (BLACK)	QT24751290
0200	/S1G	3139 247 51302	FRONT PANEL (GOLD)	QT24751302
0201		4822 454 11825	BADGE MARANTZ	QP45411825
0202	/A1B,/U1B	3139 247 51310	BADGE DVD (BLACK)	QT24751310
0202	/S1G	3139 247 51321	BADGE DVD (GOLD)	QT24751321
0204		3139 244 00550	WINDOW	QT24400550
0205	/A1B,/U1B	3139 244 00570	BUTTON POWER (BLACK)	QT24400570
0205	/S1G	3139 247 51331	BUTTON POWER (GOLD)	QT24751331
0219	/A1B,/U1B	3139 244 00590	DOOR (BLACK)	QT24400590
0219	/S1G	3139 247 51341	DOOR (GOLD)	QT24751341
0220		3139 241 20110	SPRING DOOR	QT24120110
0240	/A1B,/U1B	3139 247 51410	BUTTON CONTROL (BLACK)	QT24751410
0240	/S1G	3139 247 51421	BUTTON CONTROL (GOLD)	QT24751421
0244		3139 247 51451	FOOT	QT24751451
0245		3139 247 51271	FOOT	QT24751271
⚠ 1005	/A1B,/S1G	3139 248 80390	PSU PCB ASSY DVD2000 (OVS)	QT24880390
⚠ 1005	/U1B	3139 248 80380	PSU PCB ASSY DVD2000 (USS)	QT24880380
1014		3139 110 34220	FFC FOIL 22P/105/22P BD B	QT11034220
1018		3139 110 34230	FFC FOIL 16P/105/16P BD B	QT11034230
0384		3139 228 85500	REMOTE CONTROL	QT22885500
⚠ 0385	/A1B	3139 118 73040	MAINS CORD (/A1B)	QT11873040
⚠ 0385	/S1G	4822 321 10249	MAINS CORD (/S1G)	QP32110249
⚠ 0385	/U1B	4822 321 11466	MAINS CORD (/U1B)	QP32111466
0387	/U1B	3139 246 10350	USER GUIDE (/U1B)	QT24610350
0387	/A1B,/U1B	3139 246 10521	USER GUIDE (/A1B,/S1G)	QT24610521

12. SCHEMATIC DIAGRAM AND PARTS LOCATION

Volume / Standby PWB







A1 : FRONT DISPLAY PCB

For models with P50 only

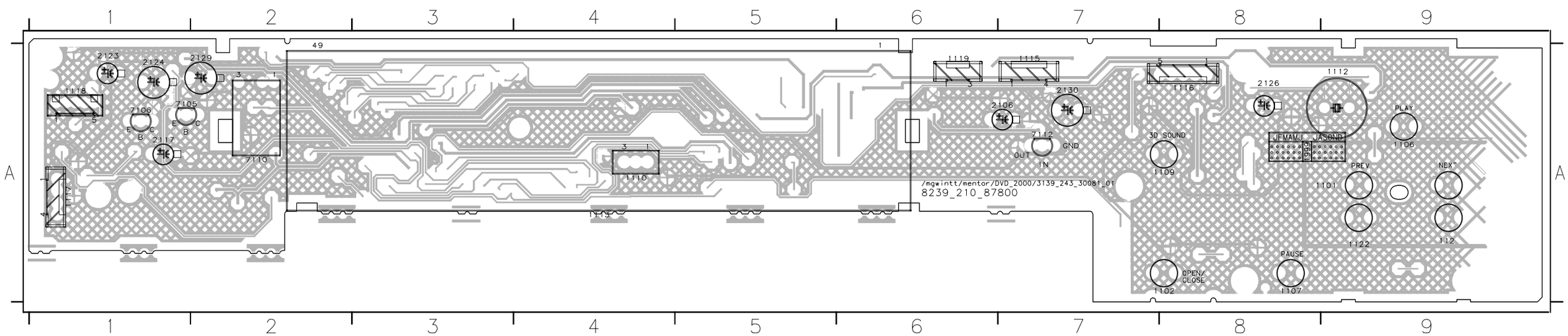
For DVD732 only

OPTION

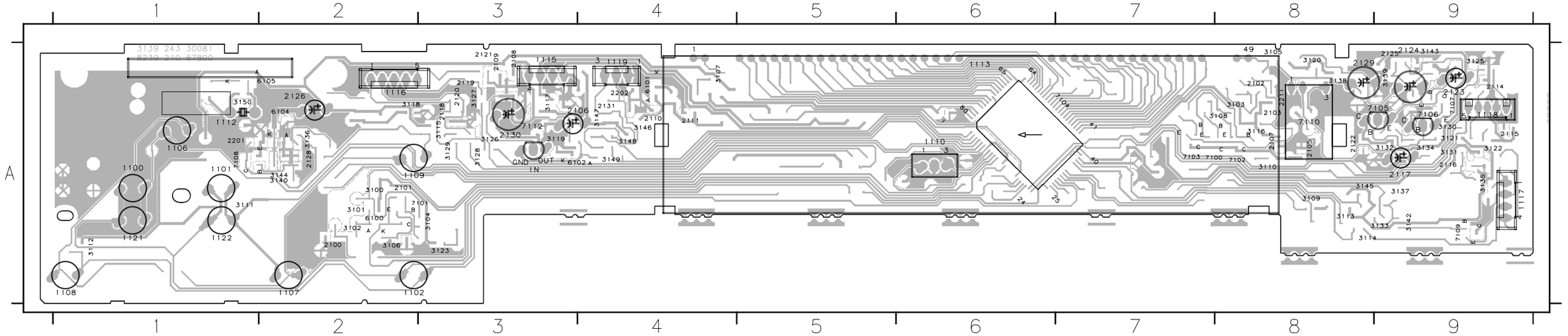
INFO : FIL2-FIL1=4.8Vac-RMS

Display PWB

1100 A91101 A91102 A81106 A91107 A81108 A91109 A81110 A41112 A91113 A41115 A71116 A81117 A11118 A11119 A61121 A91122 A21106 A72117 A12123 A12124 A12126 A82129 A22130 A77105 A77106 A77110 A27112 A7

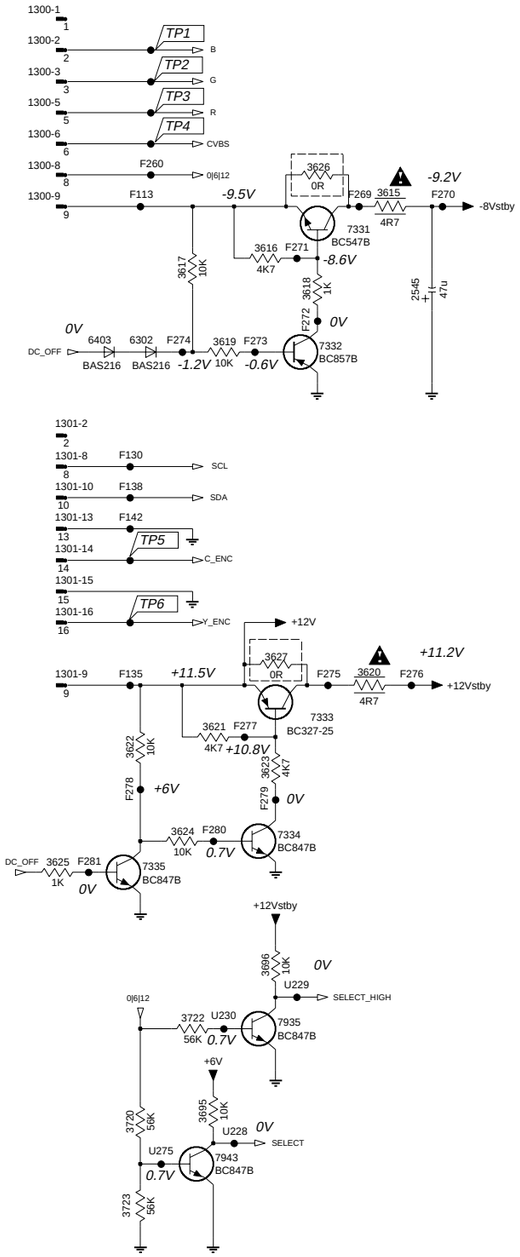


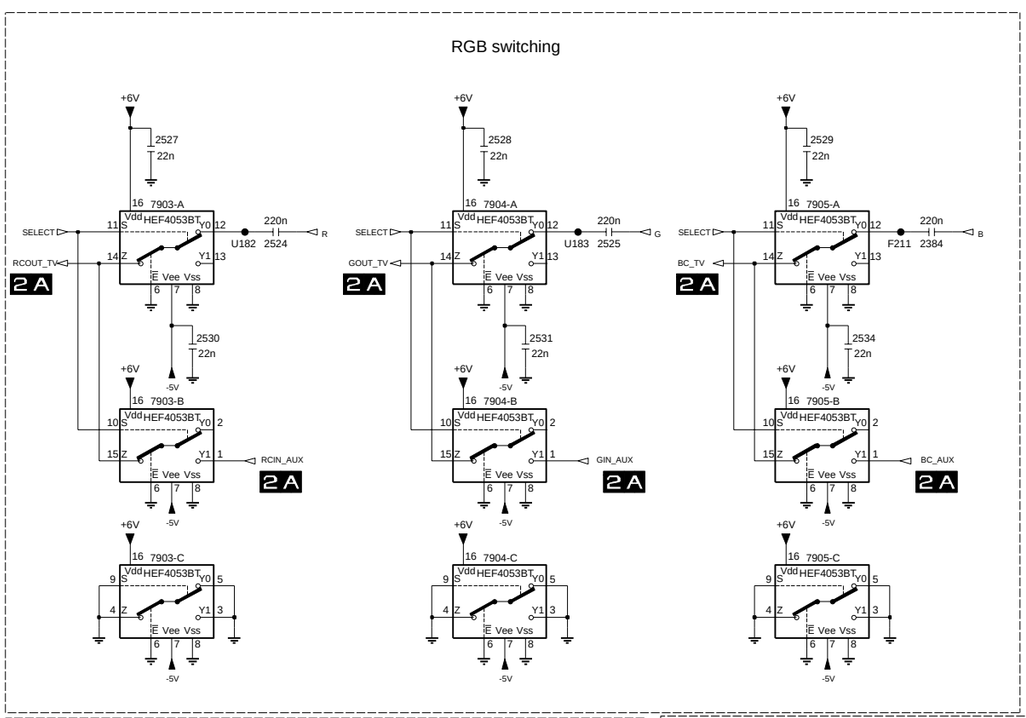
2100 A22103 A82108 A32111 A42116 A92120 A32125 A92201 A13100 A23103 A83106 A23109 A83112 A13115 A33118 A23121 A96125 A93128 A33131 A96134 A96137 A96140 A23144 A23147 A43150 A16102 A37100 A77103 A77108 A1
2101 A22105 A82109 A32114 A96118 A32121 A32128 A22202 A43101 A23104 A35107 A85110 A83113 A83116 A85119 A35122 A96126 A35129 A35132 A96135 A96138 A86142 A95145 A85148 A46100 A26104 A27101 A27104 A67109 A9
2102 A82107 A82110 A42115 A92119 A32122 A82131 A42211 A83102 A23105 A83108 A83111 A13114 A83117 A33120 A83123 A33127 A33130 A95133 A95136 A23139 A96143 A95146 A43149 A46101 A46105 A17102 A87107 A9

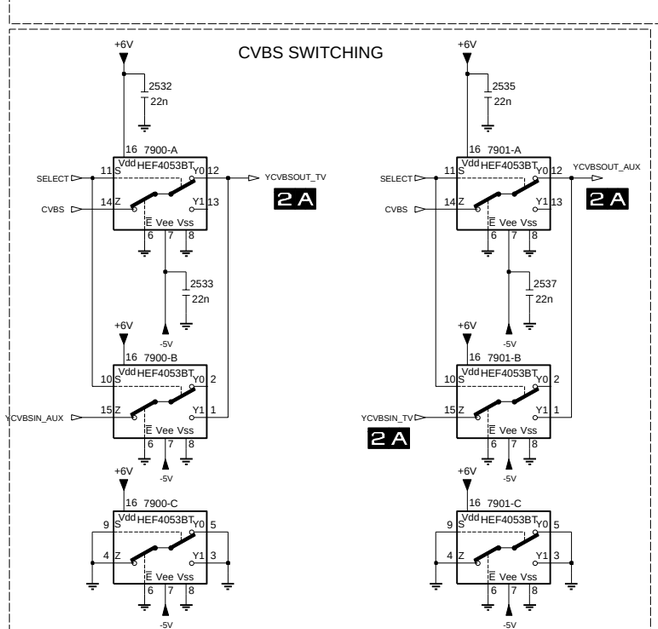


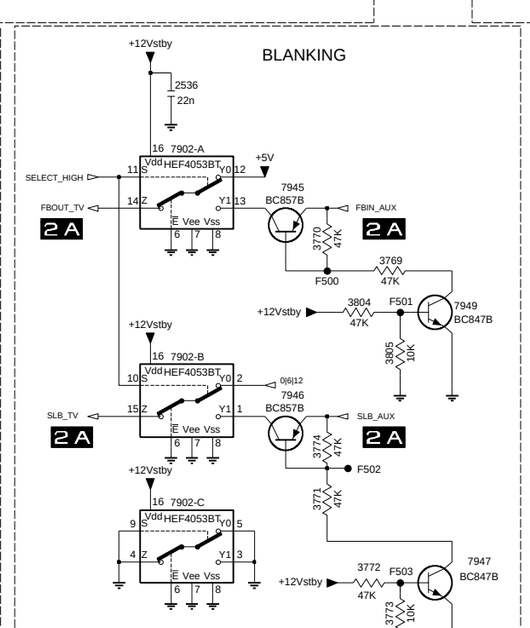
Supply and video switching (/N1B)

1 A SUPPLY & VIDEO SWITCHING









SELECT:
0V DURING PLAYER SCRIPT: "SCART DVD"
6V DURING PLAYER SCRIPT: "SCART LOOP"

SELECT HIGH:
0V DURING PLAYER SCRIPT: "SCART DVD"
12V DURING PLAYER SCRIPT: "SCART LOOP"

ALL DC VOLTAGES MEASURED IN STOP MODE.

1300-1 A1
1300-2 A1
1300-3 A1
1300-5 A1
1300-6 B1
1300-8 B1
1300-9 B1
1301-10 D1
1301-13 D1
1301-14 D1
1301-15 E1
1301-16 E1
1301-2 D1
1301-8 D1
1301-9 E1
2354 B13
2384 B11
2412 B14
2452 C13
2453 C14
2524 B6
2525 B9
2527 A6
2528 A8
2529 A10
2530 C6
2531 C8
2532 F6
2533 G6
2534 C10
2535 F8
2536 F10
2537 G8
2541 B14
2545 C4
3433 B14
3615 B3
3616 B3
3617 C2
3618 C3
3619 C2
3620 E3
3621 F2
3622 F2
3623 F3
3624 F2
3625 G1
3626 B3
3627 E3
3695 H2
3696 G3
3720 H2
3722 H2
3723 I2
3762 D13
3769 G12
3770 G11
3771 H11
3772 I11
3773 I12
3774 H11
3804 G11
3805 G12
6302 C2
6403 C1
6404 D13
7304 B13
7331 B3
7332 C3
7333 F3
7334 F3
7335 G2
7400 C13
7900-A F6
7900-B G6
7900-C H6
7901-A F8
7901-B G8
7901-C H8
7902-A F10
7902-B G10
7902-C H10
7903-A B6
7903-B C6
7903-C D6
7904-A B8
7904-B C8
7904-C D8
7905-A B10
7905-B C10
7905-C D10
7935 H3
7943 I2
7945 F11
7946 H11
7947 I12
7949 G12
F106 A2
F109 A2
F110 A2
F112 B2
F113 B2
F120 B13
F121 B14
F130 D2
F135 E2
F138 D2
F142 D2
F144 D2
F150 E2
F211 B11
F260 B2
F269 B3
F270 B4
F271 B3
F272 C3
F273 C2
F274 C2
F275 E3
F276 E4
F277 F2
F278 F2
F279 F3
F280 F2
F281 G1
F401 C14
F500 G11
F501 G12
F502 H11
F503 I12
U182 B6
U183 B8
U185 D13
U228 H2
U229 G3
U230 H2
U275 I2

Audio A/V MUX (/N1B)

1 B AUDIO

KILL:
-8V DURING PLAY
+4.8V DURING STOP, NEXT, PREVIOUS

Option L/R

AUDIO SCART SWITCHING

1300-10 G1
1300-11 G1
1300-12 G1
1300-13 G1
1300-14 G1
1300-15 H1
1300-16 H1
1300-17 H1
1300-18 H1
1300-19 I1
1300-20 I1
1300-21 I1
1300-22 I1
1300-4 F1
1300-7 F1
1301-1 D1
1301-11 E1
1301-12 F1
1301-3 D1
1301-4 D1
1301-5 E1
1301-6 E1
1301-7 E1
1402-B D10
1402-C C10
1405 I14
1410 D14
2360 C14
2361 C13
2372 D12
2373 A12
2450 C6
2455 D4
2456 D6
2457 D9
2458 D6
2459 A5
2460 A2
2461 E6
2462 B6
2463 B9
2464 C6
2469 D2
2471 D3
2472 D3
2488 H14
2495 I13
2496 C11
2497 C11
2498 C11
2519 I13
2542 H7
2543 H10
2544 H11
3321 C14
3322 C14
3338 E13
3339 E12
3340 A12
3341 A13
3442 D8
3444 D4
3445 D9
3446 D7
3447 E7
3448 D5
3451 E5
3453 E6
3454 A5
3455 B5
3456 B7
3457 B8
3459 B5
3461 B9
3462 B7
3463 C8
3464 B6
3505 H10
3507 H10
3508 H12
3511 C1
3512 C2
3517 C7
3519 A3
3610 F8
3611 G7
3612 H7
3613 G7
3614 H8
3631 D7
3632 C6
3634 A4
3635 B11
3764 H6
3765 H6
3766 C3
3767 C4
3768 G7
3802 E1
3803 G2
5400 H11
6400 H14
6401 C11
7329 G8
7330 H8
7401 B2
7402 A4
7403-A B6
7403-B D6
7403-C A9
7403-D E9
7404 D8
7405 E8
7406 C8
7407 B8
7917 B12
7944 G7
7948 C4
F139 C12
F141 C13
F176 D12
F177 B12
F180 A12
F181 D12
F265 G8
F266 H7
F267 H8
F268 G7
F400 A9
F403 B5
F404 B6
F405 B8
F406 B8
F408 B5
F410 B7
F411 C8
F412 A4
F413 E9
F414 A2
F415 D5
F416 D8
F417 D8
F418 D5
F419 B1
F421 D6
F422 B1
F423 D7
F424 E8
F425 B1
F432 C1
F437 D3
F448 G1
F455 G1
F478 I1
F486 H11
F487 H11
F488 H12
F489 H13
F490 H12
F497 E1
F504 E1
F505 G2
U186 C12
U187 B7
U188 C3
U189 C3
U190 E3
U191 E3
U226 C12
U227 D7

Scart panel (N1B)

2A SCART

AUX-SCART 1304-2

TV-SCART 1304-1

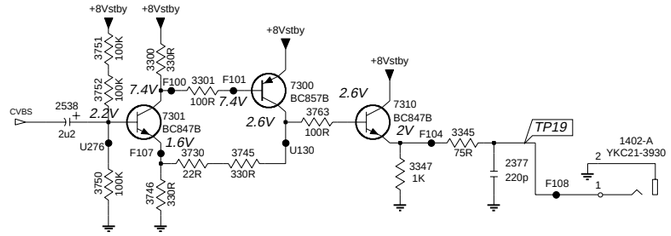
1304-3 0350808190

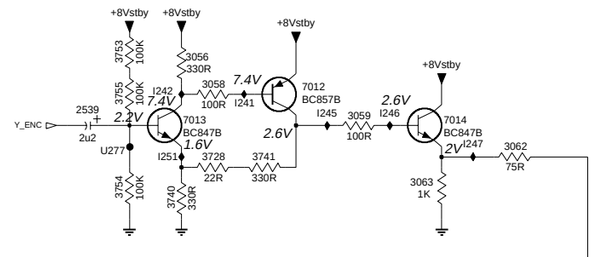
{ROUT_AUX,RIN_AUX,LOUT_AUX,LIN_AUX,BC_AUX,SLB_AUX,GIN_AUX,RCIN_AUX,FBIN_AUX,YCVBSOUT_AUX,YCVBSIN_AUX}

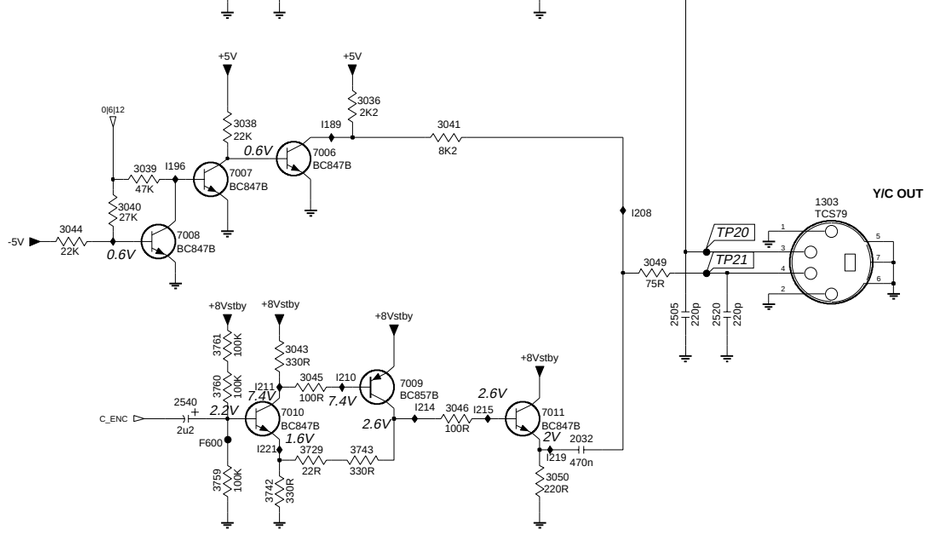
1304-1 C13
1304-2 C6
1304-3 G13
2353 A10
2355 A10
2357 B10
2358 A12
2359 B10
2371 I11
2378 A3
2382 A3
2383 B3
2385 C3
2395 C5
2402 F5
2404 E5
2408 F5
2409 I5
2499 G5
2500 E12
2501 F11
2502 C11
2503 G11
2504 H11
2506 G2
2507 D9
2508 F8
2509 C8
2511 H8
2521 B12
2522 A5
2523 B5
3313 D12
3314 A11
3315 A11
3316 A12
3318 B11
3319 B11
3320 B12
3323 B11
3325 B11
3343 I11
3348 A4
3349 A5
3351 B4
3359 B5
3363 B4
3366 B5
3394 C4
3397 C5
3407 E5
3408 F4
3409 D4
3413 D4
3425 F5
3432 I4
3629 C5
3636 G2
3637 G2
3638 D9
3639 E9
3640 E8
3641 F8
3642 C8
3643 D8
3646 H8
3647 I8
3648 G2
3649 D9
3650 E8
3651 C8
3653 H9
3672 G5
3673 E11
3674 F11
3675 C11
3676 G10
3677 H11
3678 G3
3679 G3
3680 D10
3681 D10
3682 F9
3683 F10
3684 C9
3685 C10
3687 G9
3688 H9
3689 H10
3690 I11
3691 C4
3692 D4
3693 E4
3694 I4
3697 G4
3698 E11
3699 F10
3700 C10
3701 G10
3702 I10
3703 I10
3704 D3
3705 E3
3706 F3
3707 I3
3721 G10
3724 H9
3725 F9
3726 E9
3727 G3
3731 C9
3732 I9
3733 H9
3734 F8
3735 F9
3736 E9
3737 E10
3738 H2
3739 G3
3744 D8
3747 C9
3748 C8
3749 G2
3756 D9
3757 F8
3758 H8
3800 G9
3801 G10
7918 I10
7919 C3
7920 D3
7921 E3
7922 I3
7923 G4
7924 G2
7925 D11
7926 D9
7927 F10
7928 F9
7929 C10
7930 C8
7931 G9
7933 H10
7934 H9
7936 G3
7937 D10
7938 F10
7939 C9
7941 H9
7942 G10
U103 F10
U114 A11
U115 A11
U127 B11
U133 B11
U134 C13
U140 C13
U145 D13
U148 D12
U149 D13
U154 F13
U155 A4
U156 F13
U157 C10
U158 C10
U159 C9
U160 C9
U161 C8
U162 G10
U163 G9
U167 H11
U168 H10
U169 H9
U170 H9
U184 H8
U193 A2
U194 B2
U195 B2
U196 C2
U197 C2
U198 D2
U199 D4
U200 C4
U201 E4
U202 E2
U203 F2
U204 E6
U205 G2
U206 I4
U207 I2
U208 I8
U209 I10
U210 H8
U211 H8
U212 G10
U213 F8
U214 F8
U215 D9
U216 D8
U217 C8
U218 C8
U219 B8
U220 B8
U221 A8
U222 G2
U223 A8
U225 D6
U278 G8
U279 G9

CVBS / YC panel (/N1B)

2B CVBS & YC



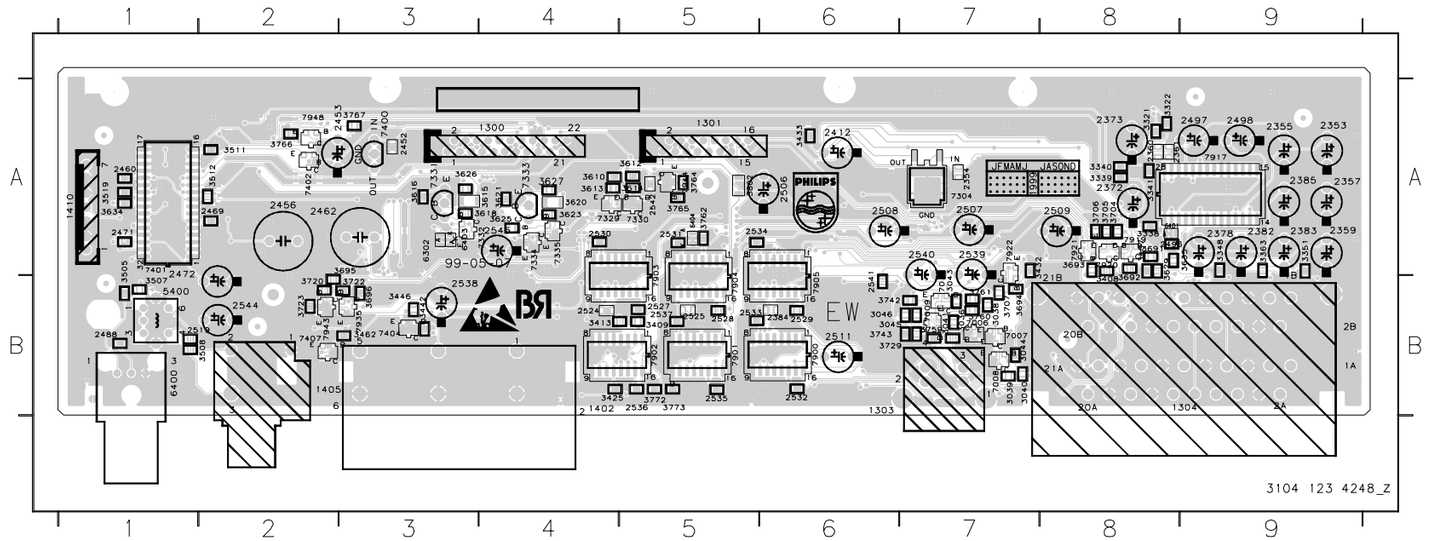




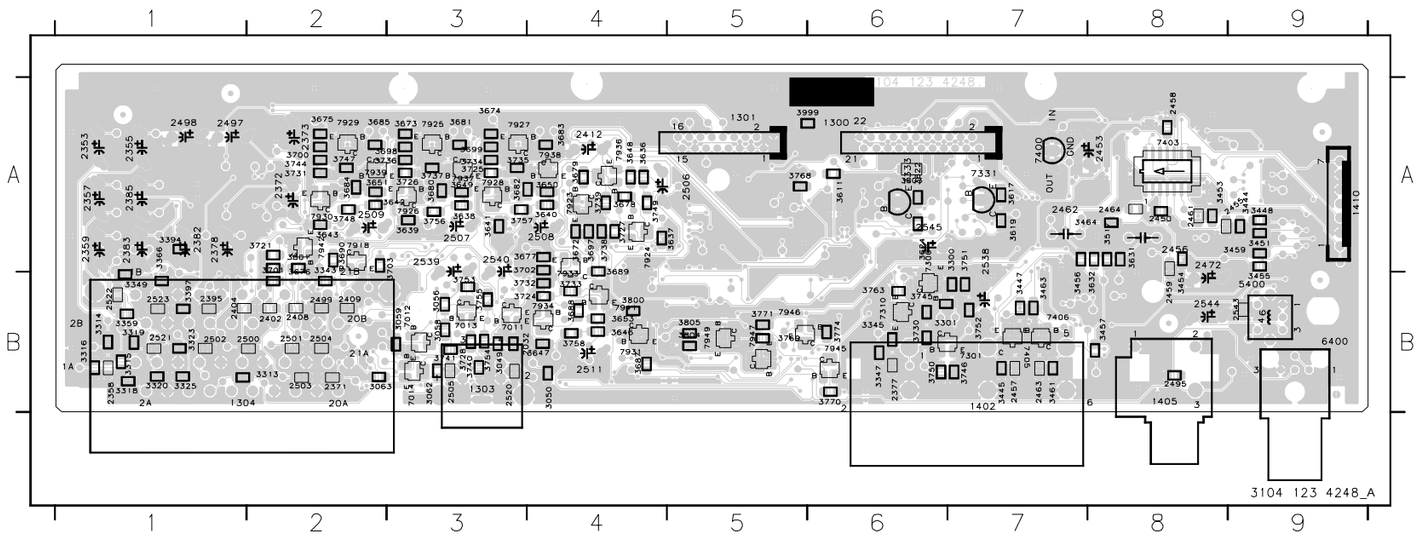
1303 F10
1402-A B9
2032 H8
2377 B9
2505 G9
2520 G9
2538 B5
2539 D6
2540 H6
3036 F7
3038 F6
3039 F5
3040 F5
3041 F7
3043 G6
3044 F5
3045 G6
3046 H7
3049 G9
3050 H8
3056 D6
3058 D6
3059 D7
3062 D9
3063 E8
3300 B6
3301 B6
3345 B8
3347 B8
3728 D6
3729 H6
3730 B6
3740 E6
3741 D7
3742 H6
3743 H7
3745 B7
3746 B6
3750 B6
3751 A6
3752 B6
3753 D6
3754 E6
3755 D6
3759 H6
3760 G6
3761 G6
3763 B7
3999 I1
7006 F6
7007 F6
7008 F6
7009 G7
7010 H6
7011 H8
7012 D7
7013 D6
7014 D8
7300 B7
7301 B6
7310 B8
F100 B6
F101 B7
F104 B8
F107 B6
F108 B9
F600 H6
I189 F7
I191 F6
I196 F6
I200 G5
I208 F9
I210 G7
I211 G6
I214 H7
I215 H8
I219 H8
I221 H6
I241 D7
I242 D6
I245 D7
I246 D8
I247 D8
I251 D6
U130 B7
U192 G9
U224 G9
U276 B6
U277 D6

A/V Mux panel (/N1B)

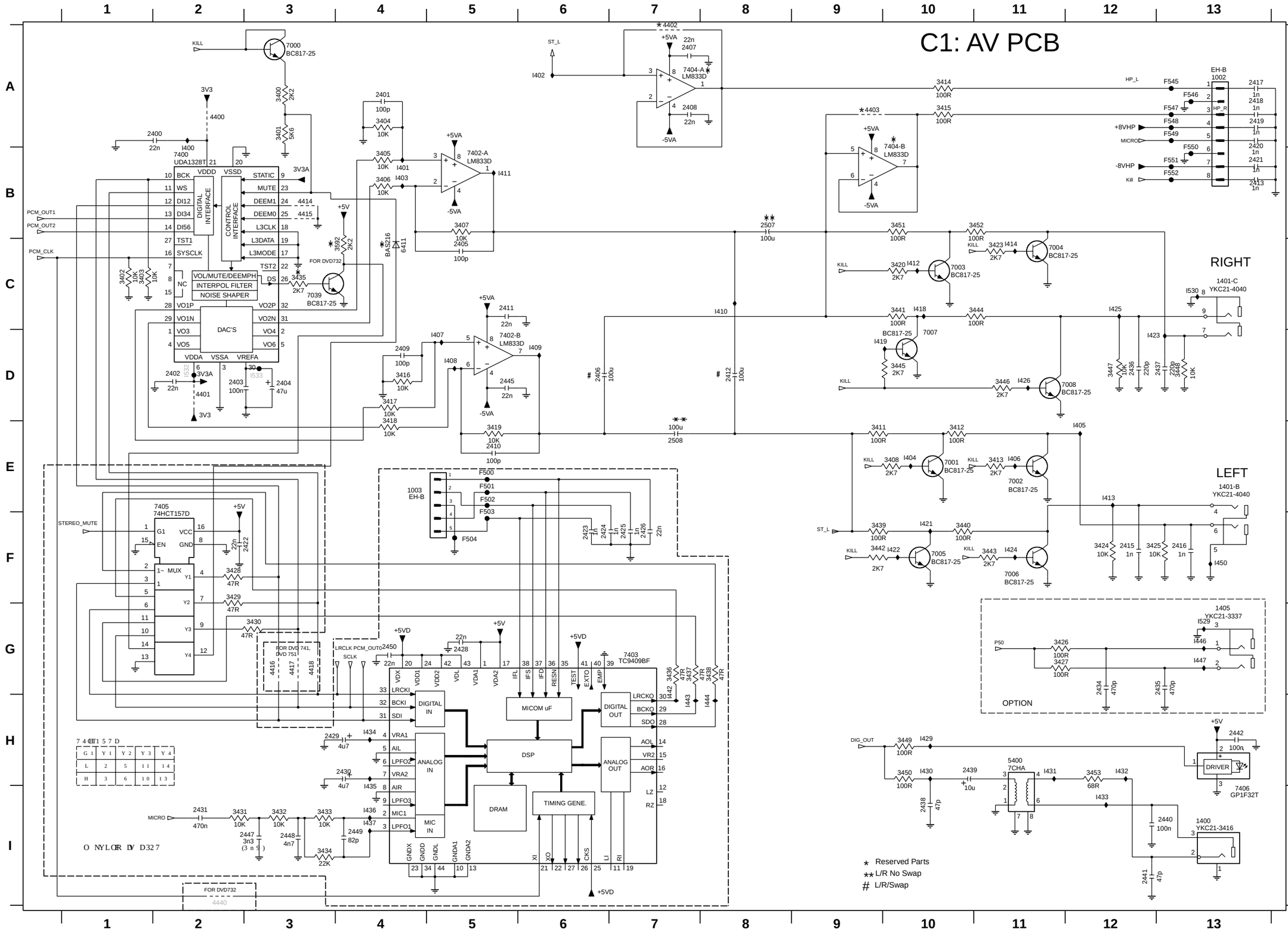
1300 A4 2357 A9 2385 A9 2488 B1 2524 B4 2535 B5 3036 B7 3322 A8 3409 B5 3508 B1 3618 A3 3691 A8 3720 B2 3764 A5 6401 A8 7330 A5 7407 B2 7921 A8
1301 A5 2359 A9 2412 A6 2496 A8 2525 B5 2536 B5 3038 B7 3338 A8 3413 B5 3511 A2 3620 A4 3692 A8 3722 B3 3765 A5 6403 A3 7331 A3 7900 B6 7922 A7
1303 B7 2360 A8 2452 A3 2497 A9 2527 B5 2537 B5 3039 B7 3339 A8 3425 B4 3512 A2 3621 A4 3693 A8 3723 B2 3766 A2 6404 A5 7332 A3 7901 B5 7935 B3
1304 B9 2361 A8 2453 A2 2498 A9 2528 B5 2538 B3 3040 B7 3340 A8 3432 A7 3519 A1 3623 A4 3694 B7 3729 B7 3767 A3 7006 B7 7333 A4 7902 B4 7943 B2
1402 B3 2372 A8 2456 A2 2506 A6 2529 B6 2539 A7 3041 B7 3341 A8 3433 A6 3610 A4 3625 A4 3695 B2 3742 B7 3772 B5 7007 B7 7334 A4 7903 B4 7944 A5
1405 B2 2373 A8 2460 A1 2507 A7 2530 A4 2540 A7 3043 B7 3348 A9 3442 B3 3612 A5 3626 A3 3696 B3 3743 B7 3773 B5 7008 B7 7335 A4 7904 B5 7948 A2
1410 A1 2378 A9 2462 A3 2508 A6 2531 A5 2541 B6 3044 B7 3351 A9 3446 B3 3613 A4 3627 A4 3704 A8 3759 B7 3802 A5 7009 B7 7400 A3 7905 B6
2353 A9 2382 A9 2469 A2 2509 A8 2532 B6 2542 A5 3045 B7 3363 A9 3462 B3 3614 A5 3629 A8 3705 A8 3760 B7 5400 B1 7010 B7 7401 A1 7917 A9
2354 A7 2383 A9 2471 A1 2511 B6 2533 B5 2544 B2 3046 B7 3407 A8 3505 B1 3615 A3 3634 A1 3706 A8 3761 B7 6302 A3 7304 A7 7402 A2 7919 A8
2355 A9 2384 B6 2472 B2 2519 B1 2534 A5 2545 A4 3321 A8 3408 A8 3507 B1 3616 A3 3635 A8 3707 B7 3762 A5 6400 B1 7329 A4 7404 B3 7920 A8



2032 B3 2504 B2 3323 B1 3464 A8 3653 B4 3701 B2 3746 B7 3805 B5 7934 B4
2358 B1 2505 B3 3325 B1 3517 A8 3672 A4 3702 A4 3747 A2 3999 A6 7936 A4
2371 B2 2520 B3 3343 B2 3611 A6 3673 A3 3703 A2 3748 A2 7011 B3 7937 A3
2377 B6 2521 B1 3345 B6 3617 A7 3674 A3 3721 A2 3749 A4 7012 B3 7938 A4
2395 B1 2522 B1 3347 B6 3619 A7 3675 A2 3724 B4 3750 B6 7013 B3 7939 A2
2402 B2 2523 B1 3349 B1 3622 A6 3676 A2 3725 A3 3751 B7 7014 B3 7941 B4
2404 B1 2543 B9 3359 B1 3624 A6 3677 A4 3726 A3 3752 B7 7300 B6 7942 A2
2408 B2 3049 B3 3366 B1 3631 A8 3678 A4 3727 A4 3753 B3 7301 B6 7945 B6
2409 B2 3050 B4 3394 A1 3632 A8 3679 A4 3728 B3 3754 B3 7310 B6 7946 B5
2450 A8 3056 B3 3397 B1 3636 A4 3680 A3 3730 B6 3755 B3 7403 A8 7947 B5
2455 A8 3058 B3 3444 A9 3637 A4 3681 A3 3731 A2 3756 A3 7405 B7 7949 B5
2457 B7 3059 B3 3445 B7 3638 A3 3682 A4 3732 B4 3757 A3 7406 B7
2458 A8 3062 B3 3447 B7 3639 A3 3683 A4 3733 B4 3758 B4 7918 A2
2459 A8 3063 B2 3448 A9 3640 A4 3684 A2 3734 A3 3763 B6 7923 A4
2461 A8 3300 B7 3451 A9 3641 A3 3685 A2 3735 A3 3768 A5 7924 A4
2463 B7 3301 B6 3453 A8 3642 A2 3687 B4 3736 A3 3769 B5 7925 A3
2464 A8 3313 B1 3454 A8 3643 A2 3688 B4 3737 A3 3770 B6 7926 A3
2495 B8 3314 B1 3455 A9 3646 B4 3689 A4 3738 A4 3771 B5 7927 A3
2499 B2 3315 B1 3456 A7 3647 B4 3690 A2 3739 A4 3774 B6 7928 A3
2500 B2 3316 B1 3457 B8 3648 A4 3697 A4 3740 B3 3800 B4 7929 A2
2501 B2 3318 B1 3459 A9 3649 A3 3698 A3 3741 B3 3801 A2 7930 A2
2502 B1 3319 B1 3461 B7 3650 A4 3699 A3 3744 A2 3803 A6 7931 B4
2503 B2 3320 B1 3463 B7 3651 A2 3700 A2 3745 B6 3804 B5 7933 A4



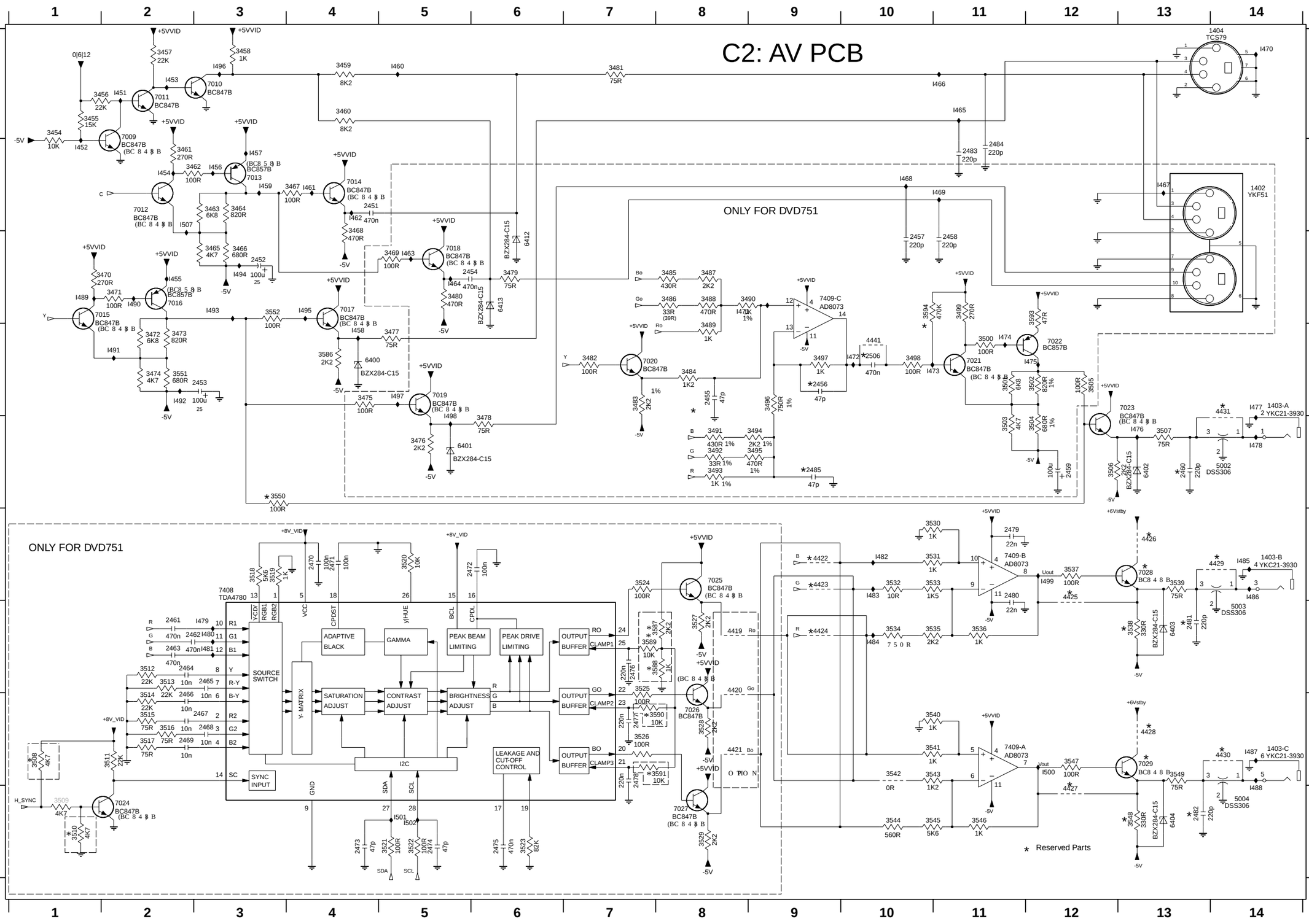
A/V board (A1B, /S1G, /U1B)



1002 A13	7001 B7	2409 D4	7402-A B5
1003 E4	7002 B8	2410 E5	7402-B D5
1400 I13	7003 F10	2411 C5	7403 G7
1401-B B13	7004 F11	2412 D6	7404-A A7
1401-C F13	7005 D8	2413 B13	7404-B C9
1405 D13	7006 E9	2415 C12	7405 E2
2400 A2	7007 G10	2416 C13	7406 H13
2401 A4	7008 G12	2417 A13	F500 E5
2402 D2	7039 C3	2418 A13	F501 E5
2403 D2	7400 B2	2419 A13	F502 E5
2404 D3	7402-A B5	2420 B13	F503 F5
2405 C5	7402-B D5	2421 B13	F504 F5
2406 B6	7403 G7	2422 F2	F545 A13
2407 A7	7404-A A7	2423 F6	F546 A13
2408 A7	7404-B C9	2424 F6	F547 A13
2409 D4	7405 E2	2425 F7	F548 A13
2410 E5	7406 H13	2426 F7	F549 A13
2411 C5	F500 E5	2428 G5	F550 B13
2412 D6	F501 E5	2429 H3	F551 B13
2413 B13	F502 E5	2430 H4	F552 B13
2415 C12	F503 F5	2431 I2	I400 B2
2416 C13	F504 F5	2434 D12	I401 B4
2417 A13	F545 A13	2435 D13	I402 A6
2418 A13	F546 A13	2436 G12	I403 B4
2419 A13	F547 A13	2437 G13	I404 B6
2420 B13	F548 A13	2438 I10	I405 B12
2421 B13	F549 A13	2439 H10	I406 B8
2422 F2	F550 B13	2440 I13	I407 D5
2423 F6	F551 B13	2441 I12	I408 D5
2424 F6	F552 B13	2442 H13	I409 D6
2425 F7	I400 B2	2445 D5	I410 C6
2426 F7	I401 B4	2447 I3	I411 B5
2428 G5	I402 A6	2448 I3	I412 F10
2429 H3	I403 B4	2449 I4	I413 B12
2430 H4	I404 B6	2450 G4	I414 E11
2431 I2	I405 B12	2507 C5	I418 F10
2434 D12	I406 B8	2508 C6	I419 G10
2435 D13	I407 D5	3400 A3	I421 D8
2436 G12	I408 D5	3401 A3	I422 D8
2437 G13	I409 D6	3402 C1	I423 F13
2438 I10	I410 C6	3403 C1	I424 D9
2439 H10	I411 B5	3404 A4	I425 F12
2440 I13	I412 F10	3405 B4	I426 G11
2441 I12	I413 B12	3406 B4	I429 H10
2442 H13	I414 E11	3407 B5	I430 H10
2445 D5	I418 F10	3408 B6	I431 H11
2447 I3	I419 G10	3411 B6	I432 H12
2448 I3	I421 D8	3412 B7	I433 I12
2449 I4	I422 D8	3413 B7	I434 H4
2450 G4	I423 F13	3414 A10	I435 I4
2507 C5	I424 D9	3415 A10	I436 I4
2508 C6	I425 F12	3416 D4	I437 I4
3400 A3	I426 G11	3417 D4	I442 G7
3401 A3	I429 H10	3418 E4	I443 H7
3402 C1	I430 H10	3419 E5	I444 H8
3403 C1	I431 H11	3420 F10	I446 D13
3404 A4	I432 H12	3423 F11	I447 D13
3405 B4	I433 I12	3424 C12	I450 C13
3406 B4	I434 H4	3425 C12	I529 D13
3407 B5	I435 I4	3426 D12	I530 F13
3408 B6	I436 I4	3427 D12	I532 D2
3411 B6	I437 I4	3428 F2	I533 D3
3412 B7	I442 G7	3429 F2	
3413 B7	I443 H7	3430 G3	
3414 A10	I444 H8	3431 I2	
3415 A10	I446 D13	3432 I3	
3416 D4	I447 D13	3433 I3	
3417 D4	I450 C13	3434 I3	
3418 E4	I529 D13	3435 C3	
3419 E5	I530 F13	3436 G7	
3420 F10	I532 D2	3437 G7	
3423 F11	I533 D3	3438 G8	
3424 C12		3439 D7	
3425 C12		3440 D9	
3426 D12		3441 F10	
3427 D12		3442 D7	
3428 F2		3443 D9	
3429 F2		3444 F11	
3430 G3		3445 G10	
3431 I2		3446 G11	
3432 I3		3447 G12	
3433 I3		3448 G13	
3434 I3		3449 H10	
3435 C3		3450 H10	
3436 G7		3451 E10	
3437 G7		3452 E11	
3438 G8		3453 H12	
3439 D7		3592 C4	
3440 D9		4400 A2	
3441 F10		4401 D2	
3442 D7		4402 A7	
3443 D9		4403 B8	
3444 F11		4414 B3	
3445 G10		4415 B3	
3446 G11		4416 G3	
3447 G12		4417 G3	
3448 G13		4418 G3	
3449 H10		4440 I2	
3450 H10		5400 H11	
3451 E10		6411 C4	
3452 E11		7000 A3	
3453 H12			
3592 C4			
4400 A2			
4401 D2			
4402 A7			
4403 B8			
4414 B3			
4415 B3			
4416 G3			
4417 G3			
4418 G3			
4440 I2			
5400 H11			
6411 C4			
7000 A3			

A/V board (A1B, /S1G, /U1B)

C2: AV PCB



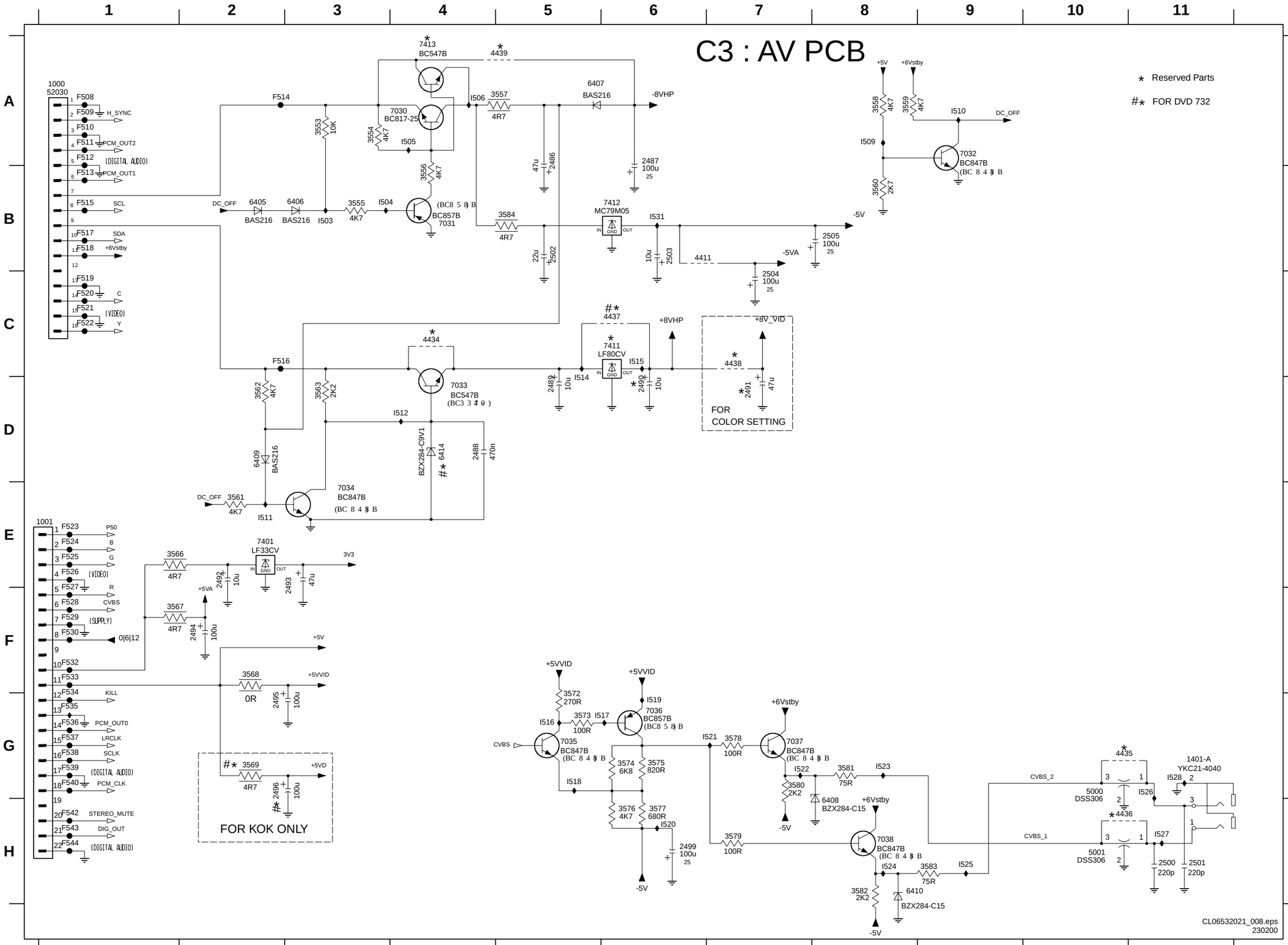
1402 B14
1403-A D14
1403-B F14
1403-C H14
1404 A14
2451 B4
2452 C3
2453 D3
2454 C5
2455 D8
2456 D9
2457 C10
2458 C11
2459 E12
2460 E13
2461 G2
2462 G2
2463 G2
2464 G2
2465 G3
2466 H2
2467 H3
2468 H3
2469 H2
2470 F4
2471 F4
2472 F6
2473 I4
2474 I5
2475 I6
2476 G7
2477 H7
2478 H7
2479 F11
2480 F11
2481 G13
2482 I13
2483 B11
2484 B11
2485 E9
2506 D10
3454 A1
3455 A1
3456 A1
3457 A2
3458 A3
3459 A4
3460 A4
3461 B2
3462 B2
3463 B3
3464 B3
3465 C3
3466 C3
3467 B4
3468 C4
3469 C5
3470 C2
3471 C2
3472 D2
3473 D2
3474 D2
3475 D4
3476 E5
3477 D5
3478 E6
3479 C6
3480 C5
3481 A7
3482 D7
3483 D7
3484 D8
3485 C8
3486 C8
3487 C8
3488 C8
3489 D8
3490 C8
3491 E8
3492 E8
3493 E8
3494 E9
3495 E9
3496 D9
3497 D9
3498 D10
3499 C11
3500 D11
3501 D11
3502 D12
3503 E11
3504 E12
3505 D12
3506 E12
3507 E13
3508 H1
3509 I1
3510 I1
3511 H2
3512 G2
3513 G2
3514 H2
3515 H2
3516 H2
3517 H2
3518 F3
3519 F3
3520 F5
3521 I5
3522 I5
3523 I6
3524 F7
3525 G7
3526 H7
3527 G8
3528 H8
3529 I8
3530 F10
3531 F10
3532 F10
3533 F10
3534 G10
3535 G10
3536 G11
3537 F12
3538 G13
3539 F13
3540 H10
3541 H10
3542 H10
3543 H10
3544 I10
3545 I10
3546 I11
3547 H12
3548 I13
3549 H13
3550 E3
3551 D2
3552 C3
3586 D4
3587 G8
3588 G8
3589 G7
3590 H8
3591 H8
3593 C12
3594 C10
4419 G8
4420 G8
4421 H8
4422 F9
4423 F9
4424 G9
4425 F12
4426 F13
4427 I12
4428 H13
4429 F14
4430 H14
4431 D14
5002 E14
5003 G14
5004 I14
6400 D4
6401 E5
6402 E13
6403 G13
6404 I13
6412 C6
6413 C6
7009 B2
7010 A3
7011 A2
7012 B2
7013 B3
7014 B4
7015 C1
7016 C2
7017 C4
7018 C5
7019 D5
7020 D7
7021 D11
7022 D12
7023 D13
7024 I2
7025 F8
7026 H8
7027 I8
7028 F13
7029 H13
7408 F3
7409-A H11
7409-B F11
7409-C C9
I451 A2
I452 B1
I453 A2
I454 B2
I455 C2
I456 B3
I457 B3
I458 D4
I459 B3
I460 A5
I461 B4
I462 B4
I463 C5
I464 C5
I465 A11
I466 A11
I467 B13
I468 B10
I469 B11
I470 A14
I471 C8
I472 D10
I473 D10
I474 D11
I475 D12
I476 E13
I477 D14
I478 E14
I480 G3
I481 G3
I482 F10
I483 F10
I484 G10
I485 F14
I486 F14
I487 H14
I488 I14
I489 C1
I490 C2
I491 D2
I492 D2
I493 C3
I494 C3
I495 C4
I496 A3
I497 D5
I498 E5
I499 F12
I500 H12
I501 I5
I502 I5
I507 B2
4441 D10

A/V board (A1B, /S1G, /U1B)

C3 : AV PCB

* Reserved Parts

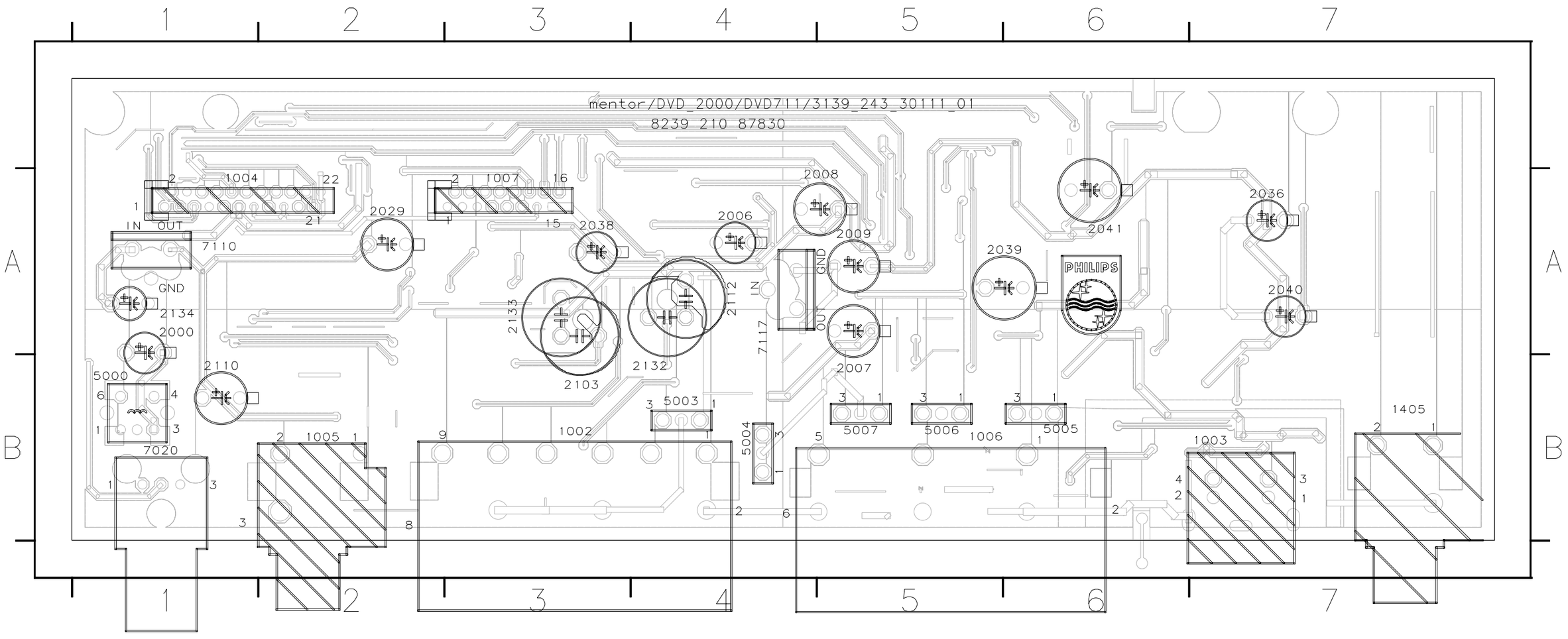
#* FOR DVD 732



1000 A1	F534 G1	
1001 E1	F535 G1	
1401-A G11	F536 G1	
2486 A5	F537 G1	
2487 A6	F538 G1	
2488 D4	F539 G1	
2489 D5	F540 G1	
2490 D6	F542 H1	
2491 D7	F543 H1	
2492 E2	F544 H1	
2493 E3	I503 B3	
2494 F2	I504 B3	
2495 G2	I505 A4	
2496 G2	I506 A4	
2499 H6	I509 A8	
2500 H11	I510 A9	
2501 H11	I511 E2	
2502 B5	I512 D4	
2503 B6	I514 D5	
2504 C7	I515 C6	
2505 B8	I516 G5	
3553 A3	I517 G6	
3554 A3	I518 G5	
3555 B3	I519 G6	
3556 B4	I520 H6	
3557 A5	I521 G7	
3558 A8	I522 G7	
3559 A8	I523 G8	
3560 B8	I524 H8	
3561 E2	I525 H9	
3562 D2	I526 G11	
3563 D3	I527 H11	
3566 E1	I528 G11	
3567 F1	I531 B6	
3568 F2		
3569 G2		
3572 G5		
3573 G5		
3574 G6		
3575 G6		
3576 H6		
3577 H6		
3578 G7		
3579 H7		
3580 G7		
3581 G8		
3582 H8		
3583 H9		
3584 B5		
4411 B6		
4434 C4		
4435 G10		
4436 H10		
4437 C6		
4438 C7		
4439 A5		
5000 G10		
5001 H10		
6405 B2		
6406 B3		
6407 A5		
6408 H8		
6409 D2		
6410 H8		
6414 D4		
7030 A4		
7031 B4		
7032 A9		
7033 D4		
7034 E3		
7035 G5		
7036 G6		
7037 G7		
7038 H8		
7401 E2		
7411 C6		
7412 B6		
7413 A4		
F508 A1		
F509 A1		
F510 A1		
F511 A1		
F512 A1		
F513 B1		
F514 A2		
F515 B1		
F516 C2		
F517 B1		
F518 B1		
F519 C1		
F520 C1		
F521 C1		
F522 C1		
F523 E1		
F524 E1		
F525 E1		
F526 E1		
F527 F1		
F528 F1		
F529 F1		
F530 F1		
F532 F1		
F533 F1		

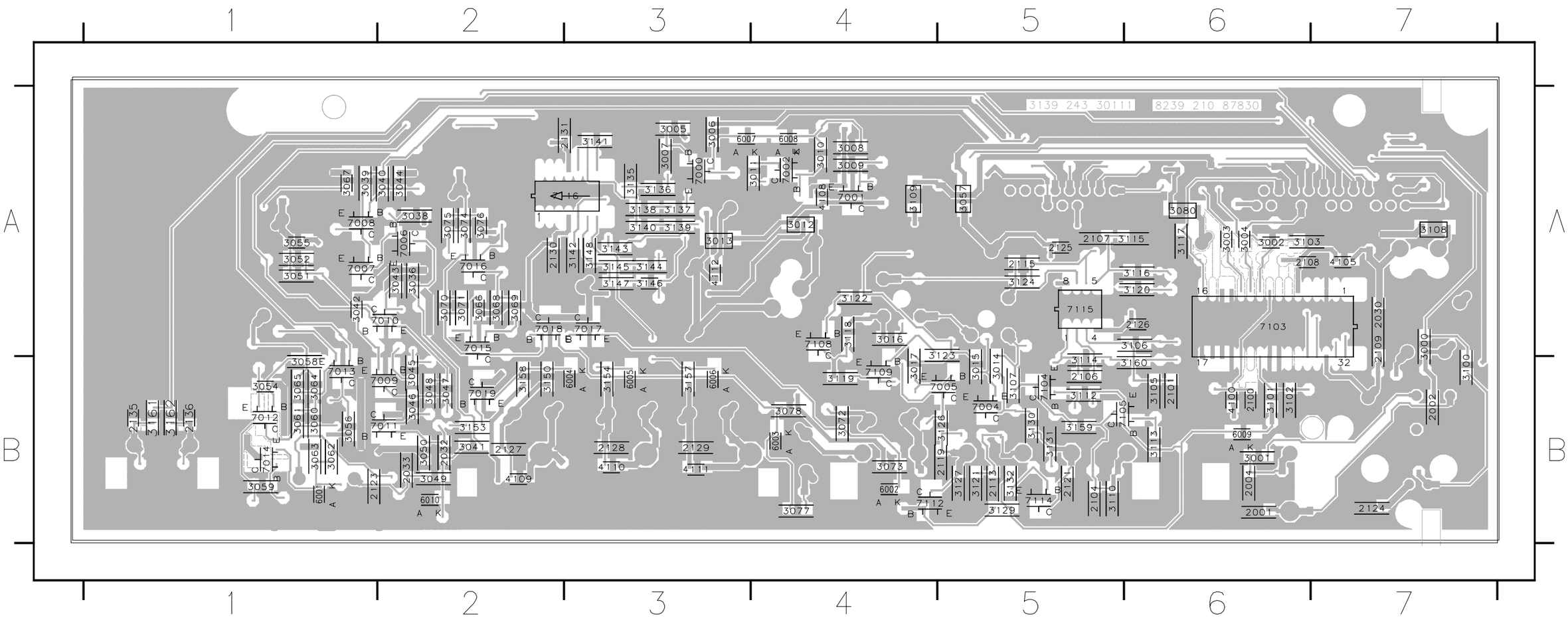
A/V Pwb (A1B, /S1G, /U1B)

1002 B3	1005 B2	1405 B7	2007 B5	2029 A2	2039 A6	2103 B3	2132 B4	5000 B1	5005 B6	7020 B1
1003 B7	1006 B5	2000 A1	2008 A5	2036 A7	2040 A7	2110 B1	2133 A3	5003 B4	5006 B5	7110 A1
1004 A1	1007 A3	2006 A4	2009 A5	2038 A3	2041 A6	2112 A4	2134 A1	5004 B4	5007 B5	7117 A4



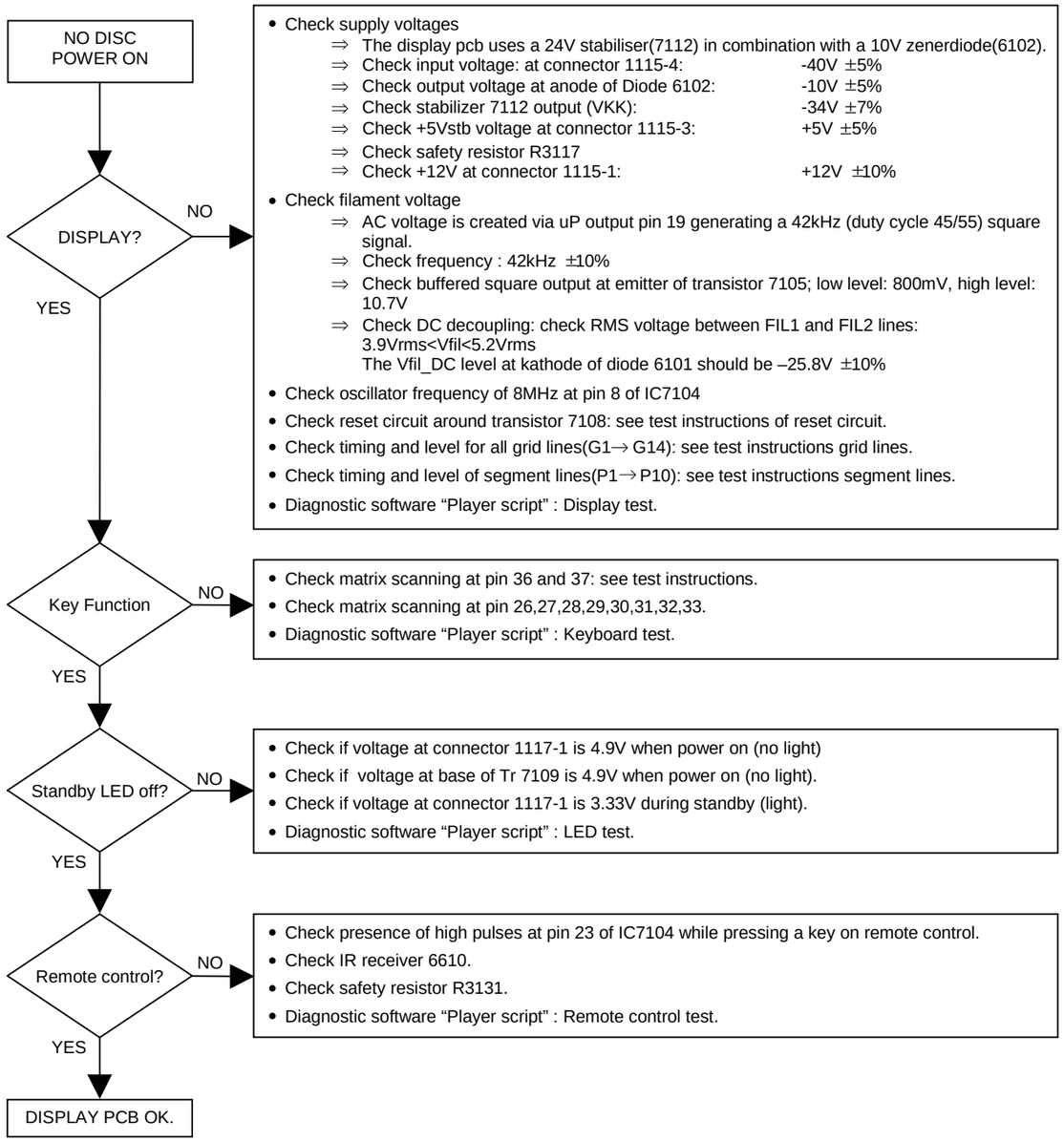
A/V Pwb (A1B, /S1G, /U1B)

2001	B6	2113	B5	2135	B1	3011	A4	3043	A2	3057	A5	3070	A2	3103	A6	3118	A4	3135	A3	3148	A3	4109	B2	6010	B2	7013	B1	7114	B5
2002	B7	2115	A5	2136	B1	3012	A4	3044	A2	3058	B1	3071	A2	3105	B6	3119	B4	3136	A3	3150	B2	4110	B3	7000	A3	7014	B1	7115	A5
2004	B6	2119	B5	3000	A7	3013	A3	3045	B2	3059	B1	3072	B4	3106	A6	3120	A6	3137	A3	3153	B2	4111	B3	7001	A4	7015	A2	7116	A3
2030	A7	2121	B5	3001	B6	3014	B5	3046	B2	3060	B1	3073	B4	3107	B5	3121	B5	3138	A3	3154	B3	4112	A3	7002	A4	7016	A2		
2032	B2	2123	B1	3002	A6	3015	B5	3047	B2	3061	B1	3074	A2	3108	A7	3122	A4	3139	A3	3157	B3	6001	B1	7004	B5	7017	A3		
2033	B2	2124	B7	3003	A6	3016	A4	3048	B2	3062	B1	3075	A2	3109	A4	3123	A5	3140	A3	3158	B2	6002	B4	7005	B5	7018	A2		
2100	B6	2125	A5	3004	A6	3017	B4	3049	B2	3063	B1	3076	A2	3110	B5	3124	A5	3141	A3	3159	B5	6003	B4	7006	A2	7019	B2		
2101	B6	2126	A6	3005	A3	3036	A2	3050	B2	3064	B1	3077	B4	3112	B5	3126	B5	3142	A3	3160	B6	6004	B3	7007	A1	7103	A6		
2104	B5	2127	B2	3006	A3	3038	A2	3051	A1	3065	B1	3078	B4	3113	B6	3127	B5	3143	A3	3161	B1	6005	B3	7008	A1	7104	B5		
2106	B5	2128	B3	3007	A3	3039	A1	3052	A1	3066	A2	3080	A6	3114	B5	3129	B5	3144	A3	3162	B1	6006	B3	7009	B2	7105	B5		
2107	A5	2129	B3	3008	A4	3040	A2	3054	B1	3067	A1	3100	B7	3115	A6	3130	B5	3145	A3	4100	B6	6007	A3	7010	A2	7108	A4		
2108	A6	2130	A2	3009	A4	3041	B2	3055	A1	3068	A2	3101	B6	3116	A6	3131	B5	3146	A3	4105	A7	6008	A4	7011	B2	7109	B4		
2109	A7	2131	A3	3010	A4	3042	A1	3056	B1	3069	A2	3102	B6	3117	A6	3132	B5	3147	A3	4108	A4	6009	B6	7012	B1	7112	B4		



12. TROUBLESHOOTING

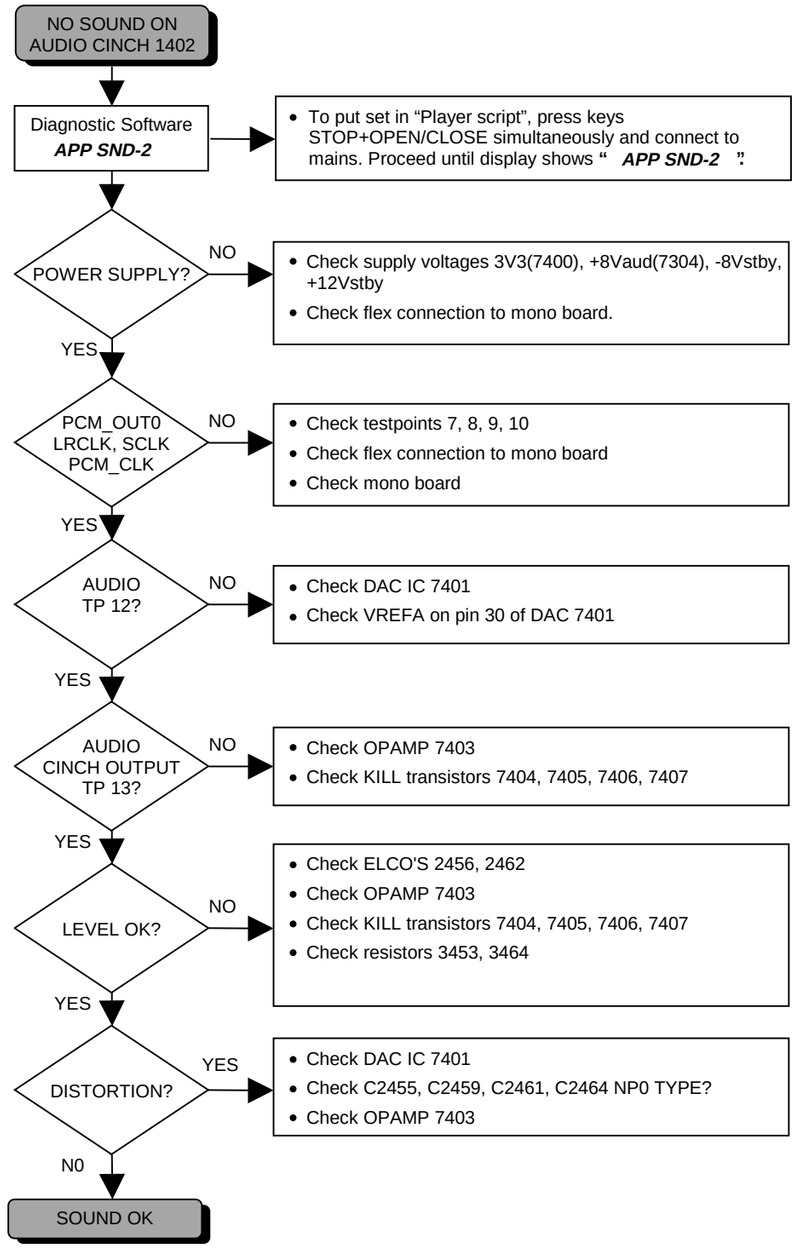
TROUBLESHOOTING DISPLAY BOARD

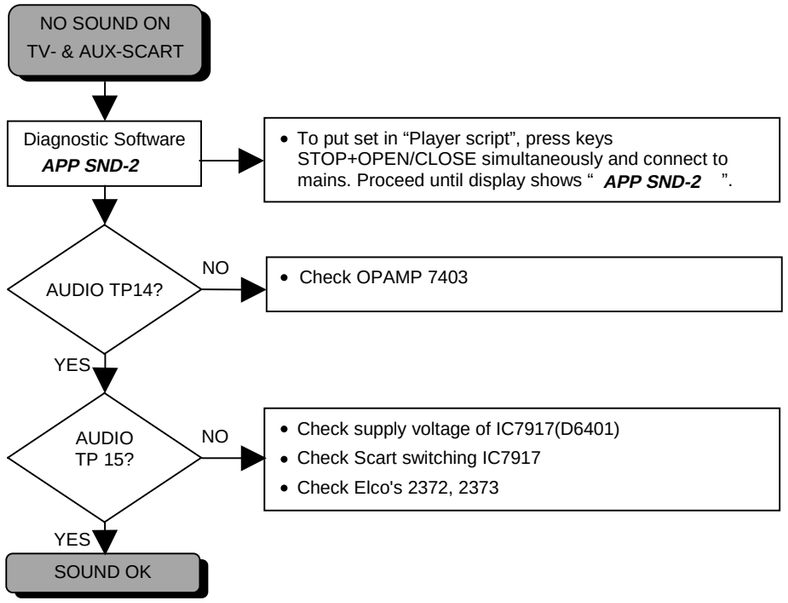


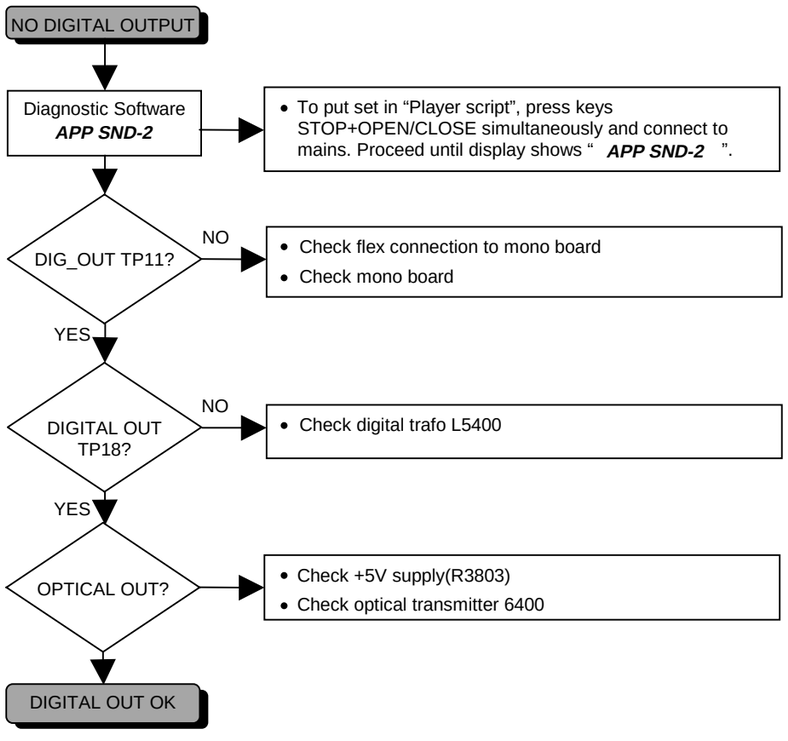
TROUBLESHOOTING A/V BOARD

Testing of A/V board can be done using diagnostic software “Player script”.
Mono board is used to generate a sinus with the soundtest SND-2 or a VIDEO signal with the picture test PIC-1.
See description in chapter “Diagnostic Software : Script Interfaces”

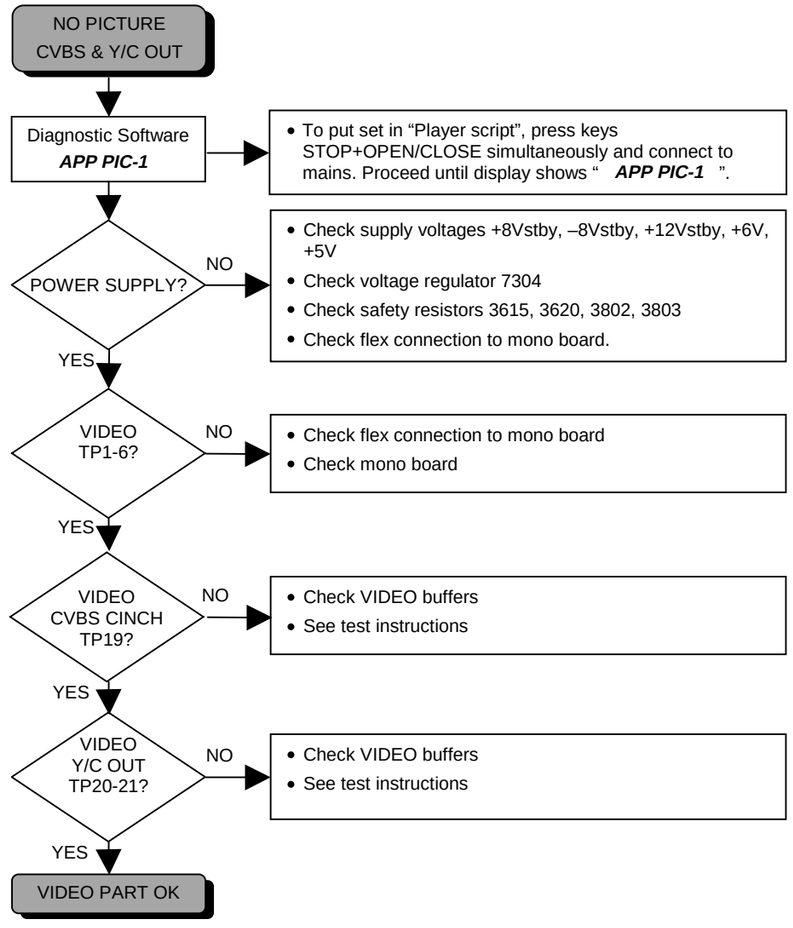
AUDIO PART

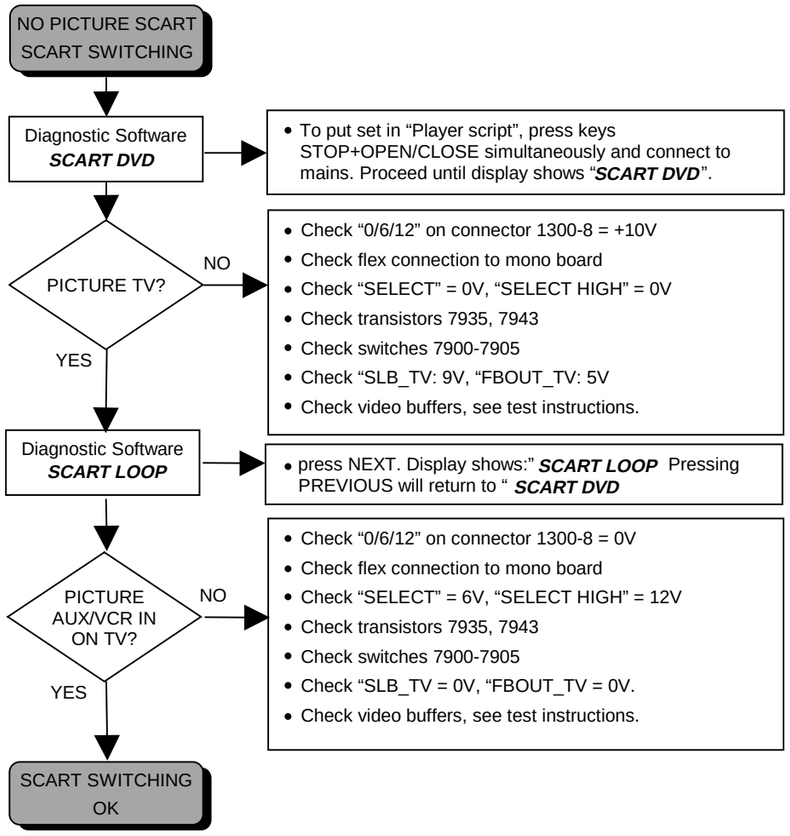


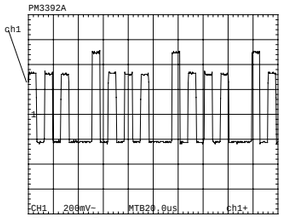

NO SOUND ON
TV- & AUX-SCART
Diagnostic Software
APP SND-2
To put set in “Player script”, press keys STOP+OPEN/CLOSE simultaneously and connect to mains. Proceed until display shows “ APP SND-2 ”.
AUDIO TP14?
NO
Check OPAMP 7403
YES
AUDIO TP 15?
NO
Check supply voltage of IC7917(D6401)
Check Scart switching IC7917
Check Elco's 2372, 2373
YES
SOUND OK


NO DIGITAL OUTPUT
Diagnostic Software
APP SND-2
To put set in “Player script”, press keys STOP+OPEN/CLOSE simultaneously and connect to mains. Proceed until display shows “ APP SND-2 ”.
DIG_OUT TP11?
NO
Check flex connection to mono board
Check mono board
YES
DIGITAL OUT TP18?
NO
Check digital trafo L5400
YES
OPTICAL OUT?
Check +5V supply(R3803)
Check optical transmitter 6400
DIGITAL OUT OK

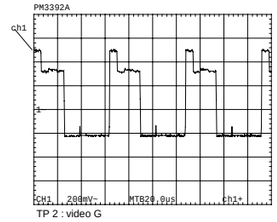
VIDEO PART


NO PICTURE
CVBS & Y/C OUT
Diagnostic Software
APP PIC-1
To put set in “Player script”, press keys STOP+OPEN/CLOSE simultaneously and connect to mains. Proceed until display shows “ APP PIC-1 ”.
POWER SUPPLY?
NO
Check supply voltages +8Vstby, –8Vstby, +12Vstby, +6V, +5V
Check voltage regulator 7304
Check safety resistors 3615, 3620, 3802, 3803
Check flex connection to mono board.
YES
VIDEO TP1-6?
NO
Check flex connection to mono board
Check mono board
YES
VIDEO CVBS CINCH TP19?
NO
Check VIDEO buffers
See test instructions
YES
VIDEO Y/C OUT TP20-21?
NO
Check VIDEO buffers
See test instructions
YES
VIDEO PART OK

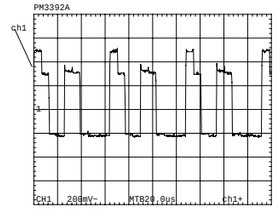




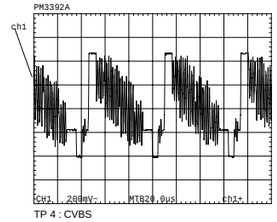
TP 1 : video B



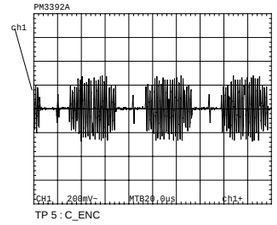
TP 2 : video G



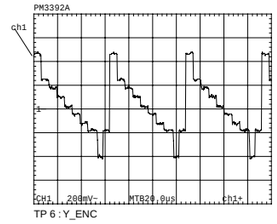
TP 3 : video R



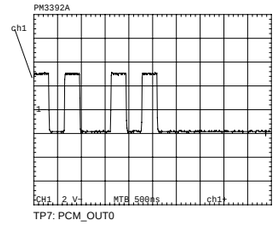
TP 4 : CVBS



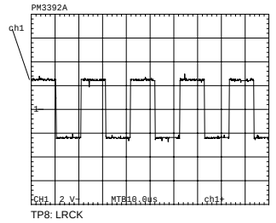
TP 5 : C_ENC



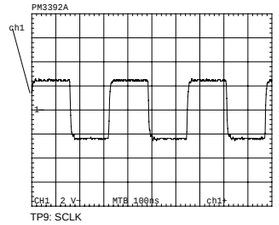
TP 6 : Y_ENC



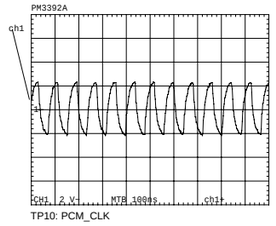
TP7: PCM_OUT0



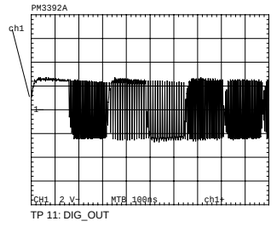
TP8: LRCK



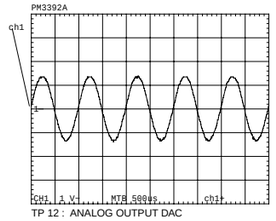
TP9: SCLK



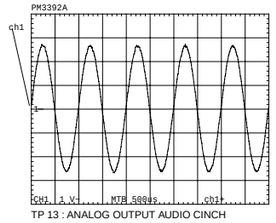
TP10: PCM_CLK



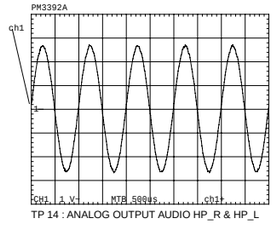
TP 11: DIG_OUT



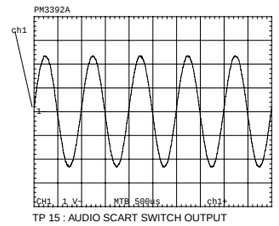
TP 12 : ANALOG OUTPUT DAC



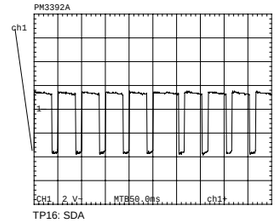
TP 13 : ANALOG OUTPUT AUDIO CINCH



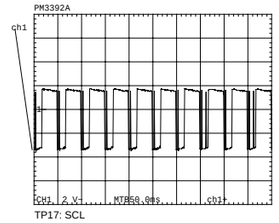
TP 14 : ANALOG OUTPUT AUDIO HP_R & HP_L



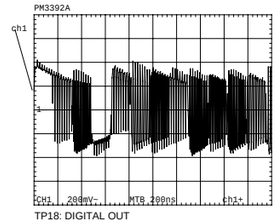
TP 15 : AUDIO SCART SWITCH OUTPUT



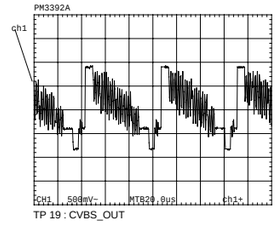
TP16: SDA



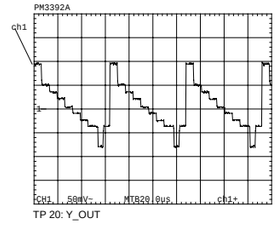
TP17: SCL



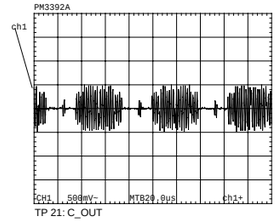
TP18: DIGITAL OUT



TP 19 : CVBS_OUT



TP 20: Y_OUT



TP 21: C_OUT

13. DIAGNOSTIC SOFTWARE : SCRIPT INTERFACES

13.1 DEALER SCRIPT

13.1.1 Purpose of Dealer Script

The dealer script can give a diagnosis on a standalone DVD player; no other equipment is needed to perform a number of hardware tests to check if the DVD player is faulty. The diagnosis is simply a "error" or "pass" message; no indication is given of faulty hardware modules. Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

13.1.2 Contents of Dealer Script

The dealer script executes all diagnostic nuclei that do not need any user interaction and are meaningful on a standalone DVD player.
The nuclei called in the dealer script are the following (the number after each nucleus name corresponds with the number being on the local display when the nucleus is executed during the dealer script):

Nucleus		Description
VideoColSetupComm		Checks the I2C interface with the RGB video processor on the Audio/Video board (only for DVD players with RGB video processor).
VideoScartSwComm		Checks the I2C interface with the scart switch on the Audio/Video board
PapChksFl		Calculate and verify checksum of FLASH memory.
PapDramWrR		Pattern test of all locations in the DRAM(s).
PapI2cDisp		Checks the I2C interface with the slave processor on the display PCB.
PapS2bEcho		Checks the I2C interface to the basic engine.
PapI2cNvram		Checks the I2C interface with the NVRAM.
PapNvramWrR		Pattern test of all locations in the NVRAM
CompSdramWrR		Pattern test of all locations in the SDRAM(s).

Figure 13-1

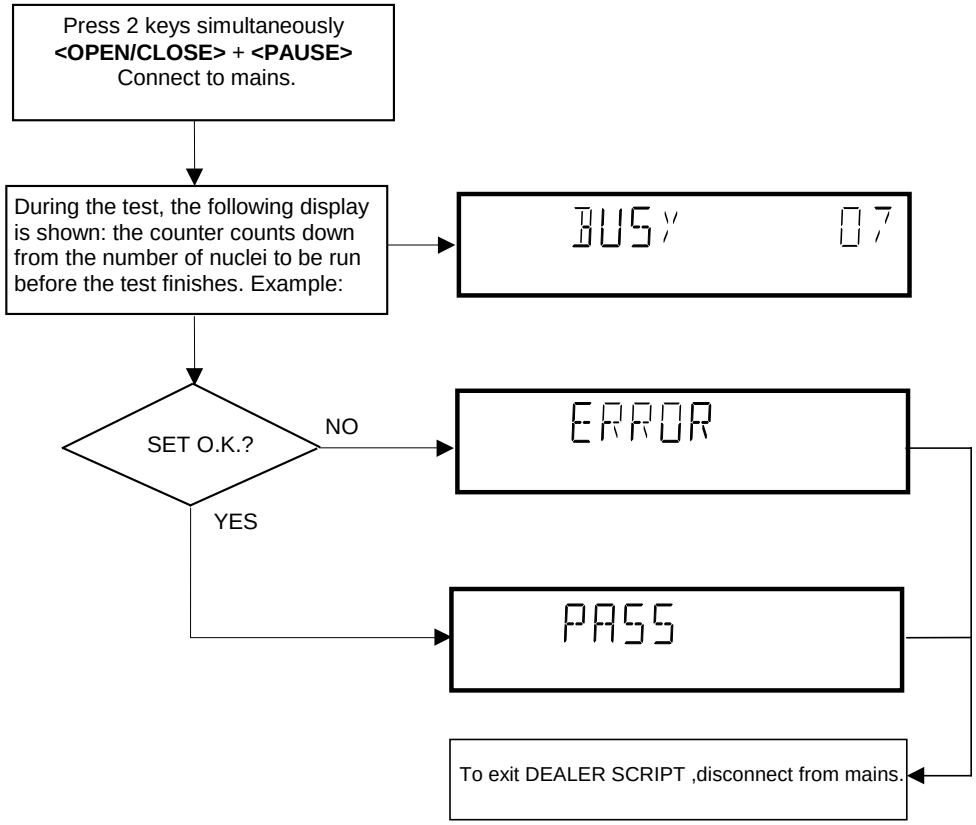


Figure 13-2

13.2 PLAYER SCRIPT

13.2.1 Purpose of Player Script

The Player script will give the opportunity to perform a test that will determine which of the DVD player's modules are faulty, to read the error log and error bits and to perform an endurance loop test. To successfully perform the tests, the DVD player must be connected to a tv set to check the output of a number of nuclei. For DVDv2b a multi-channel amplifier, a set of 6 boxes and an external video source are necessary to test. To be able to check results of certain nuclei, the player script expects some interaction of the user (i.e. to approve a test picture or a test sound). Some nuclei (e.g. nuclei that test functionality of the Basic Engine module) require that the DVD player itself is opened, to enable the user to observe moving parts and approve their movement visually. Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

13.2.2 Contents of Player Script

The player script contains all nuclei that are useful on a DVD player that is connected to a tv-set and help to determine which module of the DVD player is faulty, as well as to read out the contents of the error logs.

13.2.3 Structure of Player Script

The player script consists of a set of nuclei testing the three hardware modules in the DVD player: the Display PWB, the Digital PWB and the Basic Engine.
Nuclei run by the player test need some user interaction; in the next paragraph this interaction is described. The player test is done in two phases:

1. Interactive tests: this part of the player test depends strongly on user interaction and input to determine nucleus results and to progress through the full test. Reading the error log and error bits information can be useful to determine any errors that occurred recently during normal operation of the DVD player.
2. The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely.

13.2.4 Survey

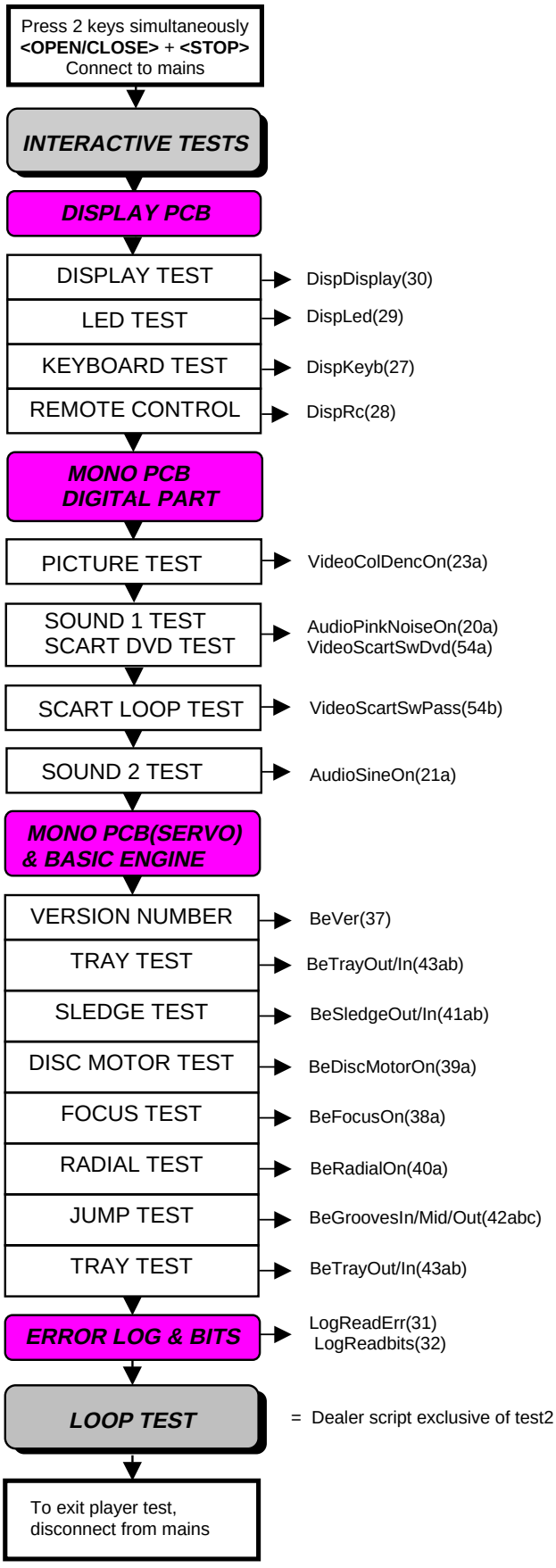


Figure 13-3

14. INTERACTIVE TESTS

14.1 DISPLAY PCB

14.1.1 DISPLAY TEST

The display test is performed by nucleus DispDisplay. By putting a series of test patterns on the local display, the local display is tested. To step through all different patterns, the user must either press PLAY (pattern is ok) or PAUSE (pattern was incorrect) to proceed to the next pattern. The display of patterns is continued in a cyclic manner until the user presses NEXT. If the user presses NEXT before all display patterns are tested, the DispDisplay nucleus will return TRUE (display test successful).

14.1.2 LED TEST

The LED(s) on the DVD player is (are) tested by nucleus DispLed. The user must check if the LED(s) is (are) lighted; if it is, press PLAY, if it is not, press PAUSE. By pressing NEXT the script will proceed to the next test. If the user presses NEXT before PLAY or PAUSE, the DispLed nucleus will return TRUE (LED test successful).

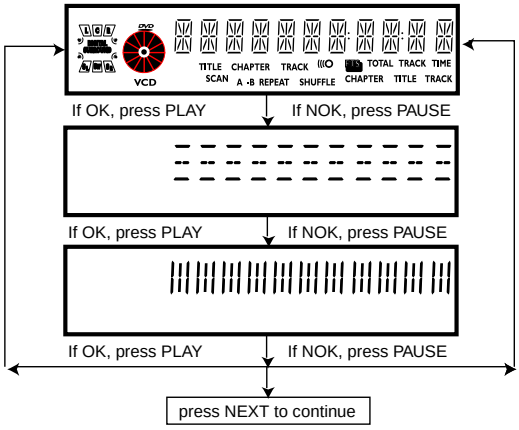


Figure 14-1

14.1.3 KEYBOARD TEST

The keyboard of the DVD player is tested by nucleus DispKeyb. The user is expected to press all keys on the local keyboard once. The code of the key pressed is shown on the local display (1 hexadecimal digit) immediately followed by a (hexadecimal) number indicating how many times that key has been pressed. Example of the local display during this test:

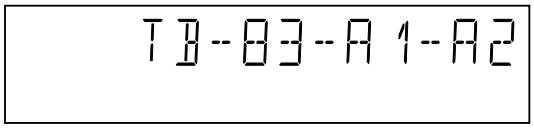


Figure 14-2

The key-codes displayed on the local display will scroll from right to left when the display gets full, the text "tb-" will remain on display.

key id.	key
0	PLAY
1	NEXT
2	PREVIOUS
3	PAUSE
4	STOP
5	OPEN / CLOSE
6	SOUND

Figure14-3

If any keys are detected more than once (due to hardware error), the key-code is displayed twice (or more), with the second digit increased by 1.
If the user does not press all keys minimally once (in any order), the DispKeys nucleus will return FALSE and cause an error in the overall result of the player script.
The user can leave the keyboard test by pressing the NEXT key on the local display of the DVD player for at least one full second.
The result of the keyboard test is shown on local display as follows:

Figure 14-4

Or

Figure 14-5

Pressing NEXT on the local keyboard again will proceed to the next text.

14.1.4 REMOTE CONTROL TEST

The remote control of the DVD player is tested by nucleus DispRc. The user must press any key on the remote control just once. The codes of the key pressed will be shown on the local display in hexadecimal format. Example:

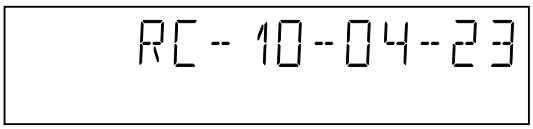


Figure 14-6

In this example 23 is the hexidecimal code of the pressed RC key. The user can leave the remote-control test by pressing NEXT on the local keyboard of the DVD player. The remote control test is successful if a code was received before the user pressed the NEXT key; pressing the NEXT key before pressing a key on the remote control gives an error in the remote control test (note that the remote control test will also fail if a key on the remote control was pressed but no code was received). The remote control test does not check upon the contents of the received code, that is it will not be checked if the received code matches the key pressed. If desired, the user can manually check this code by using a code-table for the remote control key-codes.

RC Key id	Hexadecimal code
STANDBY	**C**
STOP	**31**
PLAY	**2C**
PAUSE	**30**
NEXT	**20**
PREVIOUS	**21**
CURSOR UP	**58**
CURSOR DOWN	**59**
CURSOR LEFT	**5A**
CURSOR RIGHT	**5B**
OK	**5C**
0	**0**
1	**1**
2	**2**
3	**3**
4	**4**
5	**5**
6	**6**
7	**7**
8	**8**
9	**9**
ANGLE	**85**
AUDIO	**4E**
SUBTITLES	**4B**
ROOT MENU	**54**
OSD ON/OFF	**F**
RETURN	**83**
SHUFFLE	**1C**
REPEAT	**1D**
A/B REPEAT	**3D**

Figure 14-7

After pressing NEXT, the result of the remote control test is displayed on the local display of the DVD player as follows:

Figure 14-8

Or

Figure 14-9

Pressing NEXT on the local keyboard again will proceed to the next test.

14.2 MONO PCB DIGITAL PART

14.2.1 PICTURE TEST

The picture test is performed by putting a predefined picture (colour bar) on the display (nucleus VideoColDencOn) and asking the user for confirmation. The display will show the following message:

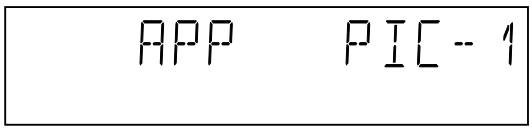


Figure 14-10

By pressing PLAY the user confirms the test, pressing PAUSE will indicate the picture was invisible or incorrect. Pressing NEXT will proceed to the next test

14.2.2 SOUND 1 & SCART DVD TEST

The first soundtest is performed by starting a pink noise sound that needs confirmation from the user (nucleus AudioPinkNoiseOn); the display will show the following message very shortly:

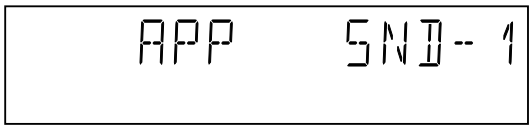


Figure 14-11

This sound will only be audible from version cut3.1 of Sti5505(item7503 on mono board) onwards. After starting up sound 1, SCART loop-trough will be simultaneously active during this test. SCART loop-trough will be measured with the aid of an external video source.
When entering the SCART loop-trough, the local display indicates:

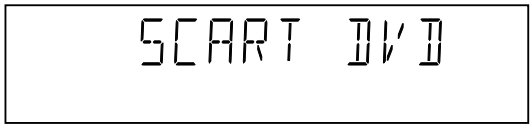


Figure 14-12

On the TV screen a colour bar (generated by nucleus VideoColDencOn) is visual and the internally generated pinknoise is audible. By pressing PLAY the user confirms the test, pressing PAUSE will indicate the sound was inaudible or incorrect. Pressing NEXT will proceed to the next test; if the user presses NEXT without pressing PLAY or PAUSE first, the result of this test will be TRUE (sound ok). By pressing the NEXT button there will be switched over to the external source, this must become now visible on the TV screen (using the SCART). The local display indicates:

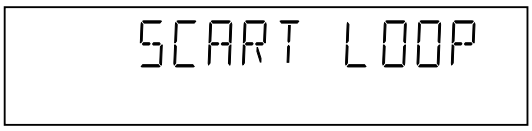


Figure 14-13

The internally generated colour bar is still available on the CVBS and Y/C outputs. And the pinknoise-signal is still available on the cinch audio outputs. By pressing the PREV button, the internal generated colour bar becomes visual again. The test can be left by pressing the NEXT key for more than one second.

14.2.3 SOUND 2 TEST

The second soundtest is performed by producing a sine sound (nucleus AudioSineOn). The signal can be stopped by pressing the STOP-key. The display will show the following message:

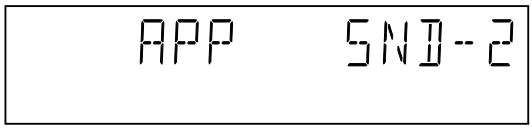


Figure 14-14

By pressing PLAY the user confirms the test, pressing PAUSE will indicate that something went wrong. Pressing NEXT will proceed to the next; if the user presses NEXT without pressing PLAY or PAUSE first, the result of this test will be TRUE (sound ok).

14.3 BASIC ENGINE

14.3.1 VERSION NUMBER

In the basic engine tests, the version number of the Basic Engine will be shown first, as the following example:

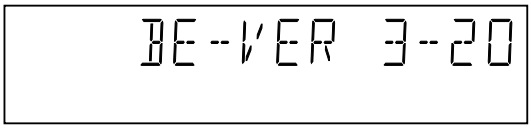


Figure 14-15

By pressing the NEXT key, the Basic Engine tests are started.

14.3.2 TRAY TEST

First, the tray is tested. The purpose of this test is also to give the user the opportunity to put a disc in the tray of the DVD player. Some tests on the Basic Engine require that a disc(e.g. DVD MPTD test disc) is present in the player. At the end of the Basic Engine tests this tray test will be repeated solely to enable the user to remove the disc in the tray. The local display will look as follows:

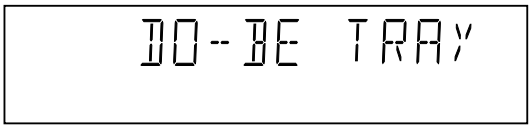


Figure 14-16

By pressing PLAY or PAUSE the user can toggle the position of the tray. Note that this test will not contribute to the test result of the Basic Engine. Pressing NEXT will proceed to the next test, after the tray has been closed (by the software) if it was open.

14.3.3 SLEDGE TEST(visual test)

The second Basic Engine test tests the sledge; the user can move the sledge as many times as desired by using PLAY (nucleus BeSledgeOut) and PAUSE (nucleus BeSledgeIn). Pressing NEXT on the local keyboard proceeds to the next test. Note that this test will not contribute to the test result of the Basic Engine. The local display will look as follows during the sledge test:

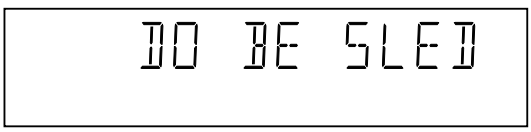


Figure 14-17

14.3.4 DISC MOTOR TEST(visual test)

The third Basic Engine test tests the disc motor (nucleus BeDiscMotorOn); the local display looks as follows:

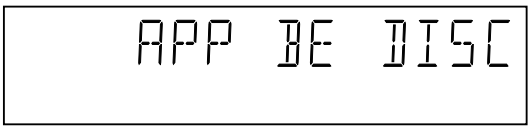


Figure 14-18

By pressing PLAY the user confirms that the disc motor is running; pressing PAUSE indicates the disc motor does not work. Pressing NEXT proceeds to the next test, after a reset of the disc motor (nucleus BeDiscMotorOff). If the user presses NEXT before pressing PLAY or PAUSE, the result of this test will be TRUE (disc motor is running).

14.3.5 FOCUS TEST(visual test)

The fourth Basic Engine test tests the focussing; first focussing is turned on by calling nucleus BeFocusOn. The display will look as follows:

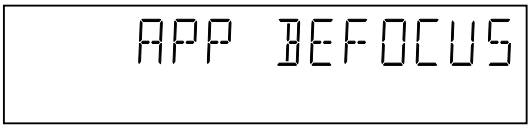


Figure 14-19

By pressing PLAY the user confirms that the focussing was succesful; pressing PAUSE indicates a focussing failure. Pressing NEXT proceeds to the next test after a reset of the focussing (nucleus BeFocusOff); if NEXT is pressed before PLAY or PAUSE, the result of this test will be TRUE (focus successful).

14.3.6 RADIAL TEST(visual & listening test)

The fifth Basic Engine test tests the radial functionality (nucleus BeRadialOn); the local display looks as follows:

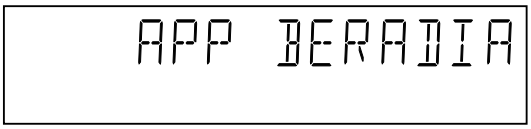


Figure 14-20

By pressing PLAY the user confirms that the radial function worked; pressing PAUSE indicates the function does not work. Pressing NEXT proceeds to the next test, after a reset of the radial (nucleus BeRadialOff). If the user presses NEXT before pressing PLAY or PAUSE, the result of this test will be TRUE (radial successful).

14.3.7 JUMP TEST(listening test)

The sixth and last Basic Engine test tests the jumping by calling nuclei BeGroovesIn, BeGroovesMid and BeGroovesOut. During this test, the local display looks as follows:

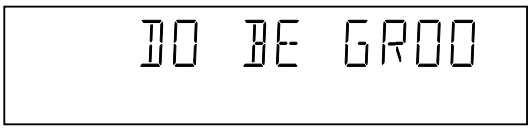


Figure 14-21

The user can switch between the three different types of groove settings by pressing PLAY (forward to next nucleus in the list In-Mid-Out) or PAUSE (backward in the list In-Mid-Out). This is done in a cyclic manner; note that this test will not contribute to the test result of the Basic Engine. Pressing NEXT proceeds to the next test, after the disc motor has been shut off with a call to nucleus BeDiscMotorOff.

14.3.8 TRAY TEST

As a last action for the Basic Engine tests, the tray test is repeated. The local display will look as follows:

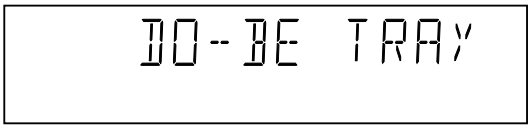


Figure 14-22

This test is meant to give the user the opportunity to remove the disc in the tray. The tray position can be toggled using the PLAY and PAUSE key. The tray will be closed (by the software, if it is open) before proceeding to the next test when the user presses the NEXT key.

14.3.9 ERROR LOG

Reading the error log and error bits information can be useful to determine any errors that occurred recently during normal operation of the DVD player. Reading the error log is done by nucleus LogReadErr. The display during the errorlog readout looks as follows :

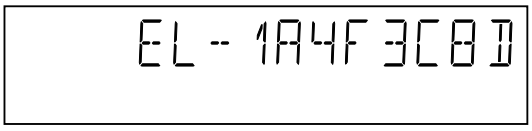


Figure 14-23

By pressing PLAY or PAUSE the user can move forward or backward (respectively) through the logged error codes. The highlighted number indicates which errorcode is currently on display (in the example above, errorcode number 4 is displayed). If "0000" is displayed at all positions, the error log is empty. Display of the logged errors is done in a cyclic manner. The errorcode with the lowest highlighted number is the most recent. By pressing NEXT on the local keyboard, the user can proceed to the next test.

14.3.10 ERROR BITS

Reading the error bits is done by nucleus LogReadBits. The display during the errorbits readout looks as follows:

Figure 14-24

Only the set errorbits will be shown by their (decimal) number. Refer to the appropriate documentation for the explanation of each bit number. If the display only shows "EB-0", no error bits were set. By pressing NEXT the user can continue to the next test.
See table below:

Error log / bits table	Read ERROR LOG in player script	Read ERROR BITS in player script
Basic engine errors	Value:	Value:
Command to the Basic Engine not allowed in this state or unknown command	150101	8
Parameter(s) from the command to the Basic Engine is not valid	150102	7
Sledge could not be moved to the inner home position	150103	6
Focus failure	150104	5
Turntable motor speed could not be reached within timeout	150105	4
Radial servo could not get on track on the disc	150106	3
PLL could not lock in the accessing or tracking state	150107	2
Subcode or sector information could not be read	150108	1
requested subcode could not be found	150109	16
Tray could not be closed or opened completely	15010A	15
TOC could not be read within timeout	15010B	14
The requested seek on the disc could not be executed	15010C	13
A requested lead-in is not on the disc	15010D	12
A non existing burst cutting area is requested	15010E	11
S2b communication error	1501F0	10
S2b communication error	1501F1	9
S2b communication error	1501F3	24
S2b communication error	1501F4	23
S2b communication error	1501F5	22
Digital PWB errors		
Communication error with the Sti 5505	90000	32
Communication error with the Sti 5505	90001	31
Disply processor errors		
Communication error with the display processor	190000	40

14.4 LOOP TEST

At the start of the loop test, the display will show the result of the interactive player test:

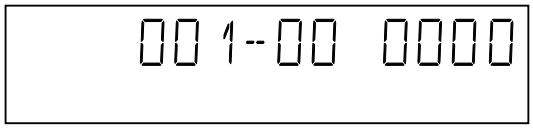


Figure 14-25

The left side of the display contains a 3-digit code, which can have a value between 000 and 111. These values are to be interpreted as follows:

Displayed Value	Indication for each module		
	Basic Engine	Mono PCB	Display PCB
000	ok	ok	ok
001	ok	ok	faulty
010	ok	faulty	ok
011	ok	faulty	faulty
100	faulty	ok	ok
101	faulty	ok	faulty
110	faulty	faulty	ok
111	faulty	faulty	faulty

Figure 14-26

The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely. The display of the DVD player will display not only the three digits indicating correct/faulty modules and the last found error code (as mentioned, faults are detected as far as they can be within the scope of the diagnostic software), but also a loop counter indicating how many times the loop has been gone through. Example:

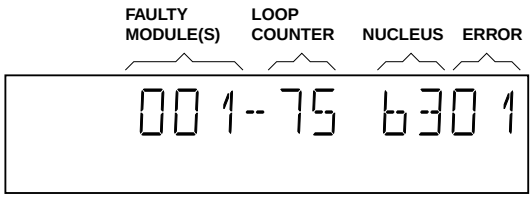


Figure 14-27

The number after the hyphen indicates the number of times the loop test has been performed; the 4 digits at the right side of the display show the last error that was found when running the loop test: the leftmost two digits of this code indicate which nucleus resulted in a fault; the rightmost two digits refer to the faultcode within that nucleus. For further explanation of this error code, see list of error codes below.

ERROR CODES LOOP TEST

ERROR CODE	NUCLEUS NUMBER	ERROR DESCRIPTION
0601	6	Calculated checksum of FLASH is not correct
0901	9	The DVD DRAM is faulty
1104	11	I2C bus busy before start
1102		NVRAM access time-out
1103		No NVRAM Acknowledge
1104		NVRAM reply time-out
1201	12	I2C bus busy
1202		I2C bus not working
1203		Slave controller not responding
1204		Slave response is not correct
1301	13	Parity error from basic engine to serial
1302		Parity error from serial to basic engine
1303		No communication between serial and basic engine
1304		Communication time-out error
1601	16	The SDRAM is faulty

Figure 14-28

14.5 Servicing DVD module and MONO board

For /U1B with old DVD module "VAE3000". (Production WEEK36 or earlier)

The DVD module(Basic Engine and the mono board) has to be exchanged completely in case of failure. A new module for DV4100 can be ordered with codenumber 3104 129 51980.

For other DV4100

Please refer the DVD Module ADS-1 Service Manual (3122 785 10840) attached with this Service Manual.
For servicing DVD Module ADS-1, the service application softwear "ComPair" is necessary.

14.5.1 Reprogramming of new mono boards.

Caution

This information is confidential and may not be distributed. Only a qualified service person should reprogram the mono board.

After replacement of the mono board, all the customer settings and also the region code will be lost.
Reprogramming of the mono board will put the player back in the state in which it has left the factory, i.e. with the default settings and the allowed region code.
Reprogramming is limited to 25 times
When the counter reaches 25, reprogramming is not possible anymore
Reprogramming will be done by way of the remote control.
Put the player in stop mode, no disc loaded.
Press the following keys on the remote control:
<***PLAY***> followed by numerical keys ***<2> <7> <4>***
The display shows: "***- - - - - - - - - - -***"
Press now successively the following keys :

for DV4100/A1B : ***<0><1><5> <0><0><0><0><0><0><0><0><0> PAL / NTSC***
for DV4100/N1B : ***<0><1><2> <0><0><0><0><0><0><0><0><0> PAL / NTSC***
for DV4100/S1G : ***<0><1><3> <0><0><0><0><0><0><0><0><0> PAL / NTSC***
for DV4100/U1B : ***<0><1><0> <0><0><0><0><0><0><0><0><0> PAL / NTSC***

Press <***PLAY***> again.
The TV screen will become BLUE during a short time to confirm that the mono board has been reprogrammed, then the set goes to standby mode.

Figure 14-29

14.5.2 Reset of Virgin Mode

After the player has been powered up for test by the dealer, it would have gone through the Virgin Mode. It is possible to reset the settings made during that mode before the delivery of player to the customer. This can be done as shown in the following diagram:

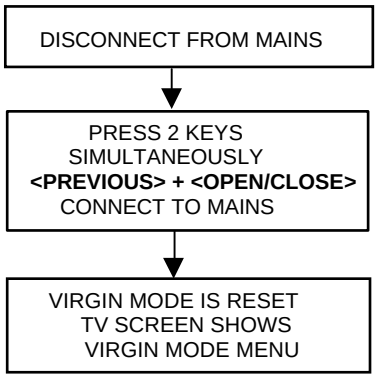


Figure 14-30

TRADE MODE

When the player is in Trade Mode, the player cannot be controlled by means of the front key buttons, but only by means of the remote control.

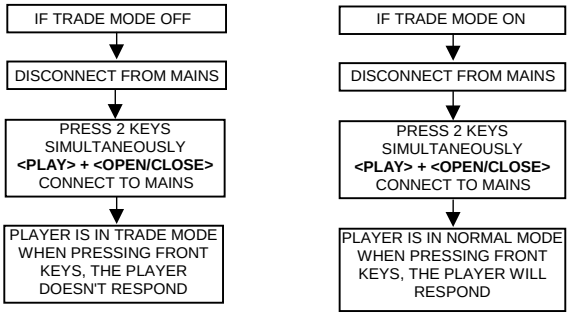


Figure 14-31

15. TEST INSTRUCTIONS DISPLAY BOARD

15.1 Display board

15.1.1 Introduction

These test instructions are written for all versions of the display PCB 3104 123 42230.
The contents of the PCB can be split up into next blocks:

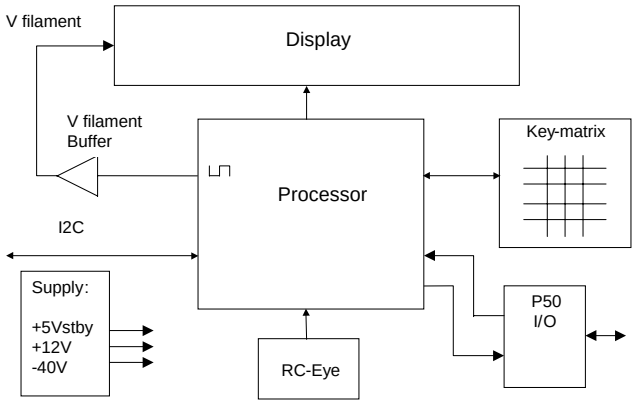


Figure 15-1

15.1.2 Functionality description:

The essential component of the display PCB is the µP (slave). This slave works on an 8MHz resonator and has a reset circuit that is triggered by the +5Vstby. After the reset pulse, the standby control line will release the reset of the host µP. This host µP will then initialise the slave. In addition, when going to stand-by, the slave will put the host µP in reset. When the slave receives the right IR or key code to leave the standby mode, the reset of the host µP will be released.
Other slave functions are:

- Square signal generator to generate the filament voltage, which is required for an AC FTD.
- Generates the grid and segment scanning for the FTD.
- Generates a scanning grid for the keys (separated from display scanning).
- Has inputs for RC (RC5 and RC6) and P50 (P50 controller is built in).

15.1.3 General

- Oscilloscope measurements have been carried out using a Philips PM3392A.
- Impedance of measuring-equipment should be > 1MΩ.
- To do correct measurements we recommend to use supply 3122 427 21370, which is used in all "second generation B" DVD-players. Make sure that the main 3.3V has a 0.7A load.

15.1.4 Reset

Check next reset timing with an oscilloscope at pin 10 of the microprocessor.

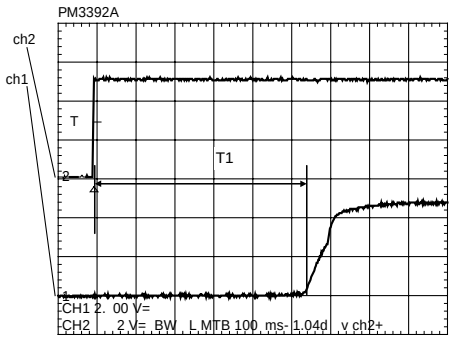


Figure 15-2

Timing: 400msec < T1 > 700msec.
CH1: +5Vstby voltage at power on.
CH2: Voltage at pin 10.

15.1.5 Display steerign

Check next timing and level for all grid-lines (G1 r G14).

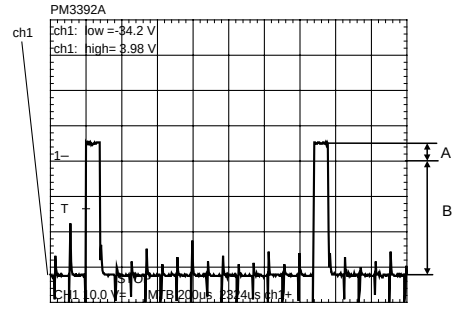


Figure 15-3

1. Check level A: +4V5 +/-10% for grid lines 1 => 11
2. Check level A: +4V0 +/-10% for grid lines 12 => 14
3. Check level B: -33V +/-10%
4. Check timing and levels of segment-lines P1 => P10:

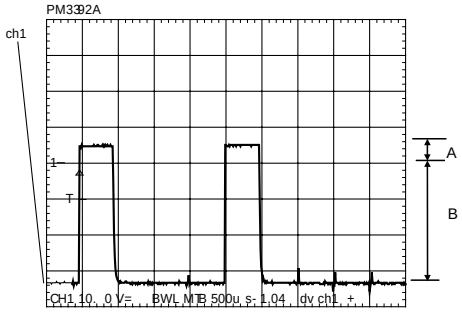


Figure 15-4

Level A:+4V5 +/-10%
Level B:-33V +/-10%
The data on these segment lines depend on the characters that are displayed.
The characters can be set by sending I2C commands to the display.
See the Slave URS how to send a display command.

15.1.6 Key-matrix

Connect a extra 10k pull-up to pin 36 en 37 of the P and check next matrix scanning at these pins.

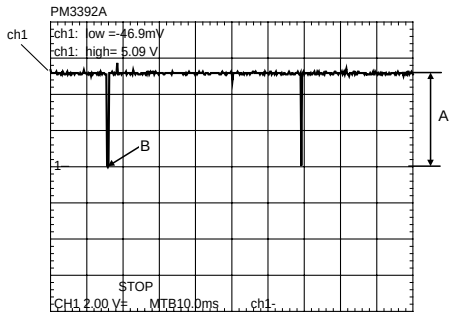


Figure 15-5

Level A: 5.0V +/-7%
Level B: 0V +/-200mV
Check matrix scanning from pin 26 until 33 of the μP.
The results should be the same as the diagram above.

15.1.7 I.R. receiver

Check at pin 23 of the μP if this line switches from low (< 0.3V) to high (> 4.5V), while pressing a key on a Philips RC5 or RC6 remote control.

15.1.8 P50 interface

P50 is a bi-directional serial interface, which is used for communication between video equipment. For European sets, this communication goes via pin 10 of the scart-bus. In other regions, it can be a cinch bus at the back of the set.

1. Keep the P in reset by short-circuiting emitter and collector of transistor 7108, via resistor 3100 and 3104 transistor 7101 is switched on.
2. Check the voltage at the P50 output connector 1118-5: < 200mV.

When the reset is released the P output-pin becomes low and transistor 7101 is switched off.

1. Check the voltage at the P50 output connector 1118-5: 4V9 +/-5%.
2. Check also the μP P50 input (μP pin 20): 5V +/-5%.
3. Connect the P50 line (connector 1118-5) to ground.
4. Check again the μP P50 input (μP pin 20): <0V3.

16. CURRENT MODE POWER SUPPLY 20PS203

16.1 Blockdiagram

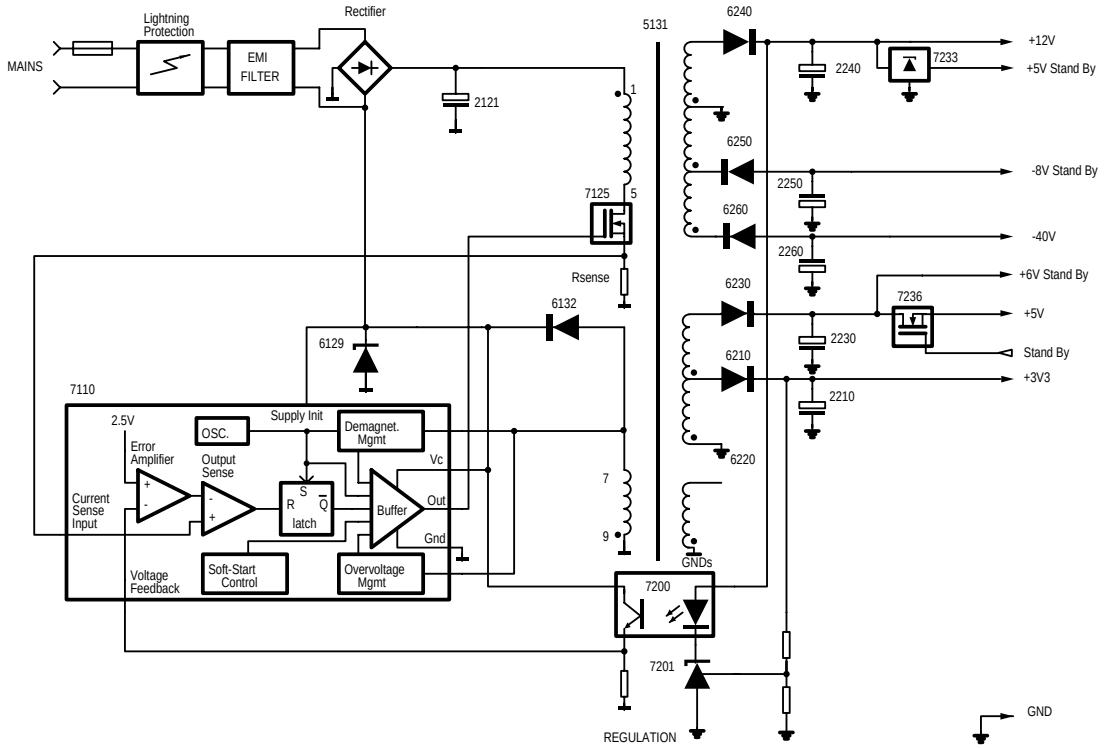


Figure 16-1

16.1.1 Function description of the current mode power supply

MOSFET 7125 is used as a power switch controlled by the controller IC 7110. When the switch is closed, energy is transferred from the mains into the transformer. This energy is then supplied to the load when the switch is opened. By control of the switched-on time, the energy transferred in each cycle is regulated so that the output voltages are independent of load or input voltage variations. The controlling device MC44603P is an integrated pulse width modulator. A clock signal initiates power pulses at a fixed frequency. The termination of each output pulse occurs when an analogue of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls the peak inductor current on cycle-by-cycle basis.

16.2 General description of MC44603

The MC44603 is an enhanced high performance controller that is specifically designed for Off-line and dc-to dc converter applications. This device has the unique ability of automatically changing operating modes if the converter output is overloaded., unloaded, or shorted. The MC44603 has several distinguishing features when compared to conventional SMPS controllers. These features consist of a foldback facility for overload protection, a standby mode when the converter output is slightly loaded, a demagnetisation detection for reduced switching stresses on transistor and diodes, and a high current totem pole output ideally suited for driving a power MOSFET. It can also be used for driving a bipolar transistor in low power converters. It is optimised to operate in discontinuous mode but can also operate in continuous mode. Its advanced design allows use in current mode or voltage mode control applications.

16.3 Pin connections

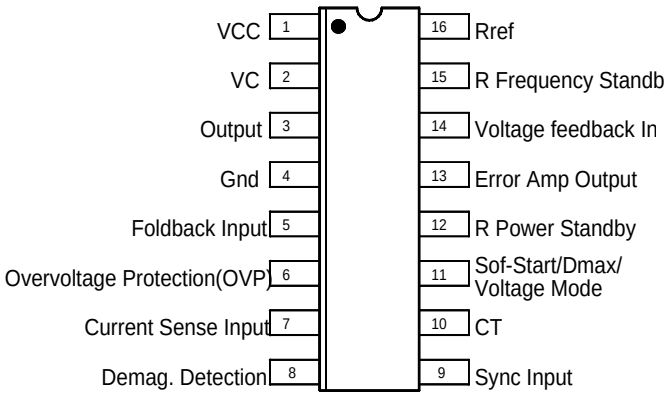


Figure 16-2

16.4 Blockdiagram of MC44603

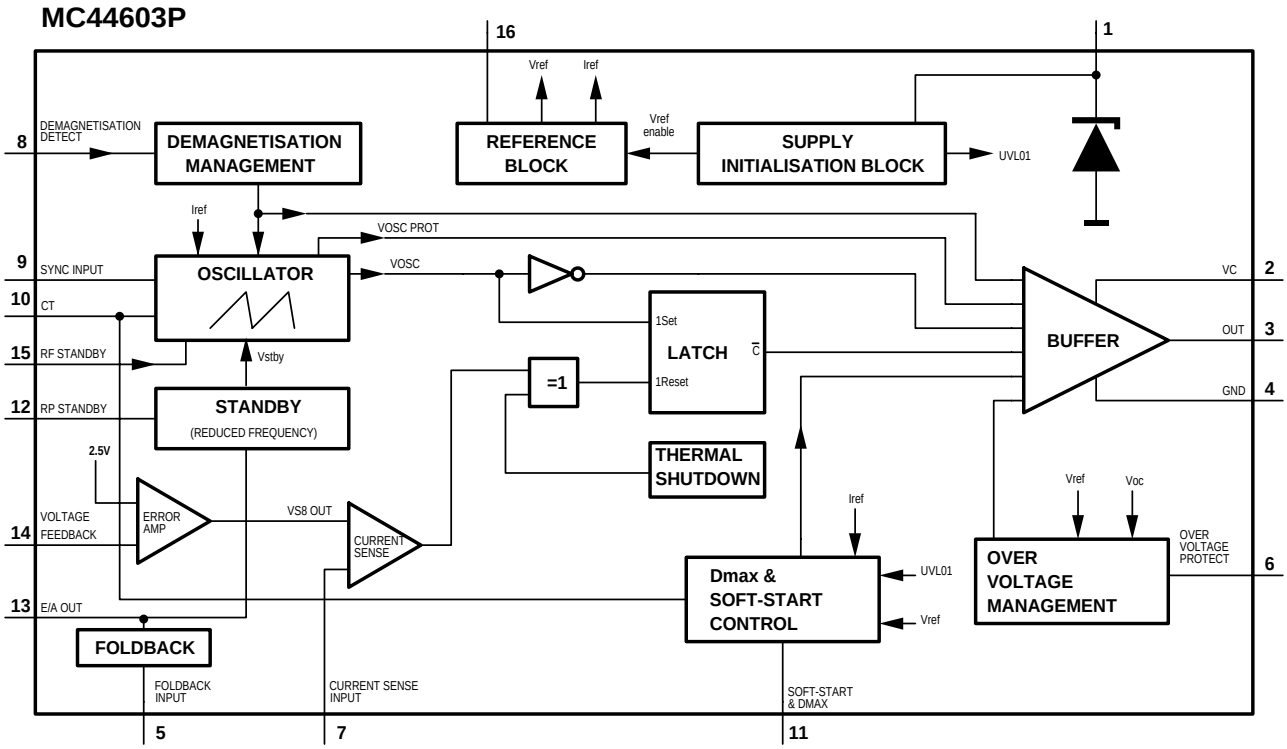


Figure 16-3

16.5 Pin function description

Pin function description

Pin	Name	Description
1	VCC	This pin is the positive supply of the IC. The operating voltage range after start-up is 9.0 to 14.5 V.
2	VC	The output high state (VOH) is set by the voltage applied to this pin.
3	Output	Peak currents up to 750 mA can be sourced or sunk, suitable for driving either MOSFET or Bipolar transistors.
4	Gnd	The groundpin is a single return, typically connected back to the power source.
5	Foldback Input	The foldback function provides overload protection.
6	Overvoltage Protection	When the overvoltage protection pin receives a voltage greater than 2.5V, the device is disabled and requires a complete restart sequence.
7	Current Sense Input	A voltage proportional to the current flowing into the power switch is connected to this input.
8	Demagnetisation Detection	A voltage delivered by an auxiliary transformer winding provides to the demagnetisation pin an indication of the magnetisation state of the flyback transformer. A zero voltage detection corresponds to complete core saturation.
9	Synchronisation Input	The synchronisation input pin can be activated with either a negative pulse going from a level between 0.7V and 3.7V to Gnd or a positive pulse going from a level between 0.7V and 3.7V up to a level higher than 3.7V. The oscillator runs free when Pin 9 is connected to Gnd.
10	C_T	The normal mode oscillator frequency is programmed by the capacitor CT choice together with the Rref resistance value. CT, connected between Pin 10 and Gnd, generates the oscillator sawtooth.
11	Soft-Start/Dmax/Voltage-Mode	A capacitor, resistor or a voltage source connected to this pin limits the switching duty-cycle. This pin can be used as a voltage mode control input. By connecting Pin 11 to Ground, the MC44603 can be shut down.
12	RP Standby	A voltage level applied to the RP Standby pin determines the output power level at which the oscillator will turn into the reduced frequency mode of operation(i.e. standby mode). An internal hysteresis comparator allows to return in the normal mode at a higher output power level.
13	E/A Out	The error amplifier output is made available for loop compensation.
14	Voltage Feedback	This is the inverting input of the Error Amplifier. It can be connected to the switching power supply output through an optical (or other) feedback loop.
15	RF Standby	The reduced frequency or standby frequency programming is made by the RF Standby resistance choice.
16	Rref	Rref sets the internal reference current. The internal reference current ranges from 100μA to 500μA. This requires that 5.0kΩ $\leq$Rref $\leq$25kΩ.

Figure 16-4

16.6 Operating description

The input voltage Vcc(pin 1) is monitored by a comparator with hysteresis, enabling the circuit at 14.5V and disabling the circuit below 7.5V. The error amplifier compares a voltage Vfb(pin 14) related to the output voltage of the power supply, with an internal 2.5V reference. The current sense comparator compares the output of the error amplifier with the switch current Isense(pin 7) of the power supply. The output of the current sense comparator resets a latch, which is set every cycle by the oscillator. The output stage is a totem pole, capable of driving a MOSFET directly.

16.6.1 Start-up sequence

t1: Charging the capacitor at Vcc
C2129 will be charged via R3123 and R3134, C2133 and C2111 via R3129. The output is switched off during t1.

t2: Charging of output capacitors
When the input voltage of the IC exceeds 14.5V, the circuit is enabled and starts to produce output pulses. The current consumption of the circuit increases to about 17mA, depending on the external loads of the IC. At first, the capacitor at the Vcc pin will discharge because the primary auxiliary voltage, coming from winding 7-9 is below the Vcc voltage. At some moment during t2, the primary auxiliary voltage reaches the same level as Vcc. The Vcc voltage is now determinated by this primary auxiliary voltage.

t3: regulation
The output voltage of the power supply is in regulation

t4: overload
When the output is shortened, the supply voltage of the circuit will decrease and after some time drop below the lower threshold voltage. At that moment, the output will be disabled and the process of charging the Vcc capacitor starts again. If the output is still shorted at the next t2 phase, the complete start-and stop sequence will repeat. The power supply comes in a hiccup mode

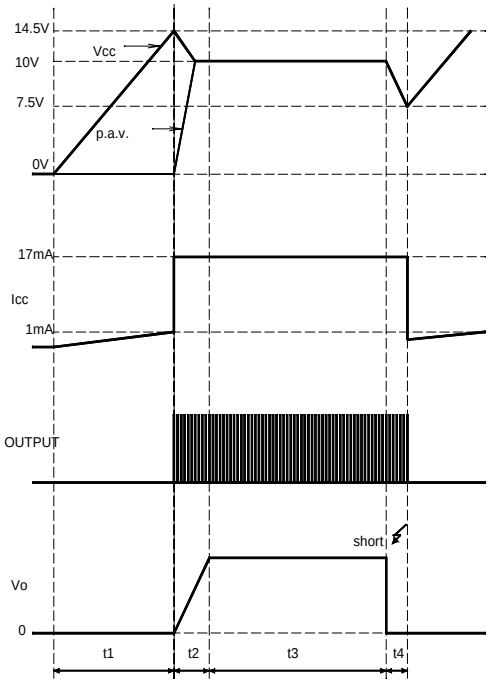


Figure 16-5 Start-up sequence

16.7 Regulation

Figure 16-6 shows the most relevant signals during the regulation phase of the power supply.
The oscillator voltage ramps up and down between V1 and V2. The voltage at the current sense terminal is compared every cycle with the output of the error amplifier Vcomp. The output is switched off when the current sense level exceeds the level at the output of the error amplifier.

1. TimeON phase : A drain current will flow from the positive supply at pin 1 of the transformer through the transformer's primary winding, the MOSFET and Rsense to ground. As the positive voltage at pin 1 of the transformer is constant, the current will increase linearly and create a ramp dependent on the mains voltage and the inductance of the primary winding. A certain amount of energy is stored in the transformer in the form of a magnetic field. The polarity of the voltages at the secundary windings is such that the diodes are non-conducting.
2. TimeDIODE phase : When the MOSFET is switched off, energy is no longer supplied to the tranformer. The inductance of the tranformer now tries to maintain the current which has been flowing through it at a constant level. The polarity of the voltage from the transformer therefore becomes reversed. This results in a current flow through the tranformer's secondary winding via the diodes, electrolytic capacitors and the load. This current is also ramp shaped but decreasing.
3. TimeDEAD phase : when the stored energy has been supplied to the load, the current in the secondary windings stops flowing. At this point the drain voltage of the MOSFET will drop to the voltage of C2121 with a ringing caused by the Drain-Source capacitance with the primary inductance.

The oscillator will start a next cyclus which consists of the described three phases. The time of the different phases depends on the mains voltage and the load.
TimeDEAD is maximum at an input of 400VDC and minimum load, it will be zero at an input of 100VDC and overload.

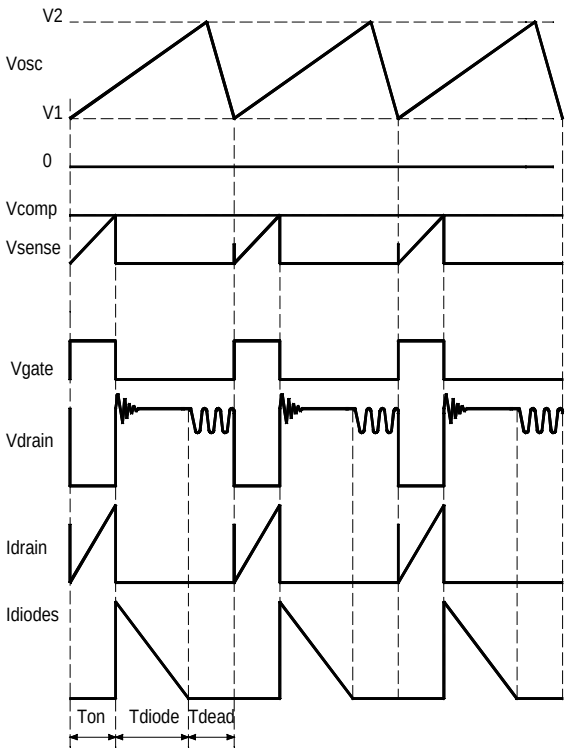
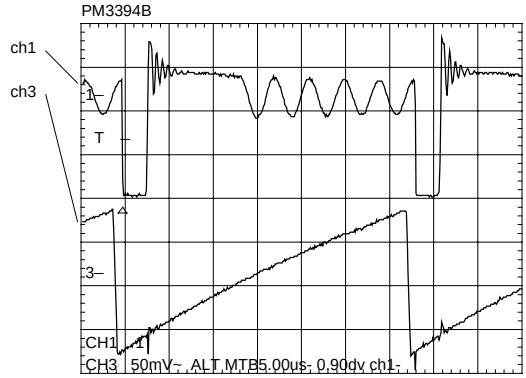


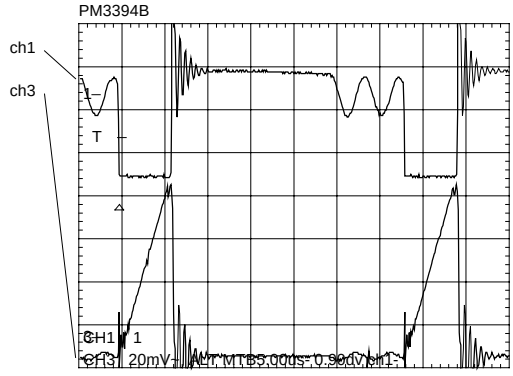
Figure 16-6 Regulation

16.8 Oscillograms

ch1 : Drain voltage
ch2 : Drain current
ch3 : Gate voltage



ch1 : Drain voltage
ch2 : Oscillator voltage



ch1 : Drain voltage
ch3 : Sense voltage

Figure 16-7

17. CIRCUIT DESCRIPTIONS AND ABBREVIATIONS

17.1 Input circuit

The input circuit consists of a lightning protection circuit and an EMI filter.
The lightning protection comprises R3120, gasarrestor 1125 and R3124. The EMI filter is formed by C2120, L5120, C2125 and C2126. It prevents inflow of noises into the mains.

17.2 Primary rectifier/smoothing circuit

The AC input is rectified by rectifier bridge 6120 and smoothed into C2121. The voltage over C2121 is approximately 300V. It can vary from 100V to 390V.

17.3 Start circuit and Vcc supply

This circuit is formed by R3123, R3134, C2129, D6129, R3129, R3111, C2133 and C2111.
When the power plug is connected to the mains voltage, the stabilised voltage over D6129(24V) will charge C2133 via R3129. When the voltage reaches 14.5V across C2111, the control circuit of IC7110 is turned on and the regulation starts. During regulation, Vcc of IC7110 will be supplied by the rectified voltage from winding 7-9 via R3135, D6132 and C2133.

17.4 Control circuit

The control circuit exists of IC7110, C2102, 2104, 2107, 2109, 2110, R3102, 3103, 3104, 3107, 3108, 3109 and 3110. The frequency of the oscillator is defined by C2102 and R3110.
Power switch circuit
This circuit comprises MOSFET 7125, Rsense 3126, 3127 and 3128, R3125 , C2127, L5125, R3112 and R3113. R3125 is a pull-down resistor to remove static charges from the gate of the MOSFET.

17.5 Regulation circuit

The regulation circuit comprises opto-coupler 7200 which isolates the error signal from the control IC on the primary side and a reference component 7201. The TL431(7201) can be represented by two components:

- a very stable and accurate reference diode
- a high gain amplifier

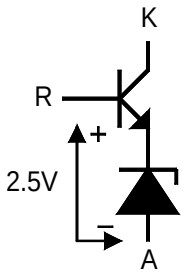


Figure 17-1

TL431 will conduct from cathode to anode when the reference is higher than the internal reference voltage of about 2.5V. If the reference voltage is lower, the cathode current is almost zero. The cathode current flows through the LED of the opto-coupler. The collector current of the opto-coupler flows through R3106, producing an error voltage, connected to voltage feedback pin 14 of IC7110.

17.6 Demagnetisation

The auxiliary winding (7-9) voltage is used to detect magnetic saturation of the transformer core and connected via R3101 to pin 8 of IC7110. During the demagnetisation phase, the output will be disabled.

17.7 Overvoltage protection circuit

This circuit consist of D6114, C2114, R3115 and R3116.
When the regulation circuit is interrupted due to an error in the control loop, the regulated output voltage will increase (overvoltage). This overvoltage is sensed on the primary winding 7-9.
When an overvoltage longer than 2.0 (s is detected, the output is disabled until VCC is removed and then re-applied. The power supply will come in a hiccup mode as long as the error in the control loop is present.

17.8 Secondary rectifier/smoothing circuit

There are 5 rectifier/smoothing circuits on the secondary side. Each voltage depends on the number of windings of the transformer.
The +5Vstby power supply is derived from the +12Vstby by voltage regulator 7233, C2233 and L5233.
The -5V voltage is regulated by voltage regulator 7259 and will be switched off via D6256, T7256 and T7255 during standby (control signal STAND BY is high). When jumper 4250 is mounted instead of this circuit, a supply voltage -8Vstby will be present at pin 9 of connector 0205. -5V is used in DVD730 MK II, DVD 930 MK II and DVD710. -8Vstby is used in DVD750 and DVD950.
The +5V power supply is derived from +6Vstby by the loader-up circuit formed by MOSFET 7236, reference component 7237, R3236, R3237 and C2239. This voltage will be switched off during STAND BY via T7235.
The 3V3 power supply is regulated by the control loop (7201, 7200, 7110) of the switched mode PSU.

17.9 List of abbreviations

B	Buffered Video input Blue from DVD monoboard
BC_AUX	Blue or Chroma input from AUX-scart
BC_TV	Blue or Chroma output to TV-scart
C_ENC	Buffered Chroma input from DVD monoboard
CVBS	Buffered Composite video input from DVD monoboard
DC_OFF	Control signal to switch off −8Vstby and +12Vstby during standby
DIG_OUT	Digital out
FBIN_AUX	Fast blanking input from AUX-scart
FBOUT_TV	Fast blanking output to TV-scart
G	Buffered Video input Green from DVD monoboard
GIN_AUX	Video input Green from AUX-scart
GOUT_TV	Video output Green to TV-scart
HP_L	Audio output left to headphone and audio scart switch TEA6420
HP_R	Audio output right to headphone and audio scart switch TEA6420
KILL	Kill control signal for audio outputs and for soft mute of DAC
LIN_AUX	Audio input left from AUX-scart
LIN_TV	Audio input left from TV-scart
LOUT_AUX	Audio output left to AUX-scart
LOUT_TV	Audio output left to TV-scart
LRCLK	Left/Right clock
PCM_CLK	Audio system clock for DAC
PCM_OUT0	Audio serial output data
R	Buffered Video input Red from DVD monoboard
RCIN_TV	Red or Chroma input from TV-scart
RCOUT_TV	Red or Chroma output to TV-scart
RIN_AUX	Audio input right from AUX-scart
RIN_TV	Audio input right from TV-scart
ROUT_AUX	Audio output right to AUX-scart
ROUT_TV	Audio output right to TV-scart
SCL	I2C bus clock
SCLK	Audio serial bit clock
SDA	I2C bus data
SELECT	Control signal for video scart switches; high = TV ,low = AUX
SELECT_HIGH	Control signal for switching fast blanking and slow blanking signals; high = TV,.low = AUX
SLB_AUX	Slow blanking control signal from AUX-scart
SLB_TV	Slow blanking control signal to TV-scart
STANDBY	Control signal from STI5505 used to swith off −8Vstby and +12Vstby during standby.
STEREO_L	Audio cinch output left
STEREO_R	Audio cinch output right
Y_ENC	Buffered Luma input from DVD monoboard
YCVBSIN_AUX	Luma or CVBS input from AUX-scart
YCVBSIN_TV	Luma or CVBS input from TV-scart
YCVBSOUT_AUX	Luma or CVBS output to AUX-scart
YCVBSOUT_TV	Luma or CVBS output to TV-scart
0/6/12	Scart switch control signal A/V board. 0V : loop through (AUX to TV), 6V : play 16:9 format, 12V : play 4:3 format

18. ELECTRICAL PARTS LIST

ASSIGNMENT OF COMMON PARTS CODES.

RESISTORS

R＊＊＊ : 1) GD05 x x x 140, Carbon film fixed resistor,±5% 1/4W
R＊＊＊ : 2) GD05 x x x 160, Carbon film fixed resistor,±5% 1/6W
① Resistance value

Examples
① Resistance value

0.1Ω	001	10Ω	100	1kΩ	102	100kΩ	104
0.5Ω	005	18Ω	180	2.7kΩ	272	680kΩ	684
1Ω	010	100Ω	101	10kΩ	103	1MΩ	105
6.8Ω	068	390Ω	391	22kΩ	223	4.7MΩ	475

Note : Please distinguish 1/4W from 1/6W by the shape of parts used actually.

CAPACITORS

C＊＊＊ : CERAMIC CAP.
3) DD1 x x x x 370, Ceramic capacitor
Disc type
Temp.coeff. P350~N1000, 50V
③ Capacity value
② Tolerance

Examples
② Tolerance (Capacity deviation)
±0.25 pF 0
±0.5 pF 1
±5 % 5
Tolerance of COMMON PARTS handled here are as follows :
0.5 pF - 5 pF ..... ± 0.25 pF
6 pF - 10 pF ..... ± 0.5 pF
12 pF - 560 pF ... ± 5 %
③ Capacity value

0.5 pF	005	3 pF	030	100 pF	101
1 pF	010	10 pF	100	220 pF	221
1.5 pF	015	47 pF	470	560 pF	561

C＊＊＊ : CERAMIC CAP.
4) DK16 x x x 300, High dielectric constant ceramic capacitor
Disc type
Temp.chara. 2B4, 50V
④ Capacity value

Examples
④ Capacity value

100 pF	101	1000 pF	102	10000 pF	103
470 pF	471	2200 pF	222		

C＊＊＊ : 5) ELECTROLY CAP.( ), 6)FILM CAP ( )
5) EA x x x x x x 10, Electrolytic capacitor
One-way lead type,Tolerance ±20%
⑥ Working voltage
⑤ Capacity value

Examples
⑤ Capacity value

0.1μF	104	4.7μF	475	100μF	107
0.33μF	334	10μF	106	330μF	337
1μF	105	22μF	226	1100μF	118
2200μF	228				

⑥ Working voltage

6.3 V	006	25 V	025
10 V	010	35 V	035
16 V	016	50 V	050

6) DF15 x x x 350 → Plastic film capacitor
DF15 x x x 310 → One-way type, Mylar ±5% 50V
DF16 x x x 310 → Plastic film capacitor
One-way type, Mylar ±10% 50V
⑦ Capacity value

Examples
⑦ Capacity value

0.001μF (1000 pF)	102	0.1μF	104
0.0018μF	182	0.56μF	564
0.01μF	103	1μF	105
0.015μF	153		

NOTE 1) The above CODES(R＊＊＊ ,R＊＊＊ ,C＊＊＊ ,C＊＊＊ and C＊＊＊) are omitted on the schematic diagram in some case.
2) On the occasion, be confirmed the common parts on the parts list.
3) Refer to “Common Parts List” for the other common parts**(RI05, DD4, DK4)**.

NOTE ON SAFETY FOR FUSIBLE RESIST OR :

The suppliers and their type numbers of fusible resistors are as follows ;
1 . KOA Corporation

Part No.(MJI)	Type No.(KOA)	Description
NH05 x x x 140	RF25S x x x x Ω	J ±5% (1/4W)
NH05 x x x 120	RF50S x x x x Ω	J ±5% (1/2W)
NH85 x x x 110	RF73B2A x x x x Ω	J ±5% (1/10W)
NH95 x x x 140	RF73B2E x x x x Ω	J ±5% (1/4W)

＊ Resistance value　　Resistance value(0.1Ω - 10k Ω)

2. Matsushita Electronic Components Co., Ltd

Part No.(MJI)	Type No.(MEC)	Description
NF05 x x x 140	ERD-2FCJ x x x	(±5% 1/4W)
RF05 x x x 140		
NF02 x x x 140	ERD-2FCG x x x	(±2% 1/4W)
RF02 x x x 140		

＊Resistance value

Examples
＊Resistance value

0.1Ω	001	10Ω	100	1kΩ	102	100kΩ	104
0.5Ω	005	18Ω	180	2.7kΩ	272	680kΩ	684
1Ω	010	100Ω	101	10kΩ	103	1MΩ	105
6.8Ω	068	390Ω	391	22kΩ	223	4.7MΩ	475

ABBREVIATION AND MARKS

ANT.	: ANTENNA	BATT.	: BATTERY
CAP.	: CAPACITOR	CER.	: CERAMIC
CONN.	: CONNECTING	DIG.	: DIGITAL
HP	: HEADPHONE	MIC.	: MICROPHONE
μ-PRO	: MICROPROCESSOR	REC.	: RECORDING
RES.	: RESISTOR	SPK	: SPEAKER
SW	: SWITCH	TRANSF.	: TRANSFORMER
TRIM.	: TRIMMING	TRS.	: TRANSISTOR
VAR.	: VARIABLE	X’ TAL	: CRYSTAL

NOTE ON SAFETY:

Symbol ⚠ Fire or electrical shock hazard. Only original parts should be used to replaced any part marked with symbol ⚠ Any other component substitution (other than original type), may increase risk of fire or electrical shock hazard.

安全上の注意：

⚠ がついている部品は、安全上重要な部品です。必ず指定されている部品番号の部品を使用して下さい。

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
			AV CIRCUIT BOARD (/A1B,/S1G,/U1B)	
			CAPACITORS	
2000		3198 028 41090	ELECT 10µF 20% 35V	QT02841090
2001		4822 126 13838	CER. 100NF 50V	QP12613838
2002		4822 126 13692	CER. 47pF 1% 63V	QP12613692
2004		4822 126 13692	CER. 47pF 1% 63V	QP12613692
2006		4822 124 41796	ELECT 22µF 20% 16V	QP12441796
2007		4822 124 23432	ELECT 100µF 20% 10V	QP12423432
2029		4822 124 81286	ELECT 47µF 20% 16V	QP12481286
2030		4822 126 13482	CER. 470NF +80 -20% 16V	QP12613482
2032		4822 126 13482	CER. 470NF +80 -20% 16V	QP12613482
2033		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2036		4822 124 41643	ELECT 100µF 20% 16V	QP12441643
2038		4822 124 41584	ELECT 100µF 20% 10V	QP12441584
2039		4822 124 40181	ELECT 220µF 20% 10V	QP12440181
2040		4822 124 41643	ELECT 100µF 20% 16V	QP12441643
2041		4822 124 41643	ELECT 100µF 20% 16V	QP12441643
2100		5322 122 32654	CER. 22N 63V	QQ12232654
2101		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2104		5322 122 31647	CER. 1NF 10% 63V	QQ12231647
2106		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2107		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2108		5322 122 32654	CER. 22N 63V	QQ12232654
2109		4822 126 13838	CER. 100NF 50V	QP12613838
2110		4822 124 81286	ELECT 47µF 20% 16V	QP12481286
2113		5322 122 31647	CER. 1NF 10% 63V	QQ12231647
2115		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2119		5322 122 31647	CER. 1NF 10% 63V	QQ12231647
2121		5322 122 31647	CER. 1NF 10% 63V	QQ12231647
2123		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2124		4822 126 14585	CER. 100NF 10% 50V	QP12614585
2125		5322 122 32654	CER. 22N 3V	QQ12232654
2126		5322 122 32654	CER. 22N 63V	QQ12232654
2130		5322 122 32654	CER. 22N 63V	QQ12232654
2131		5322 122 32654	CER. 22N 63V	QQ12232654
2132		4822 124 22339	ELECT 100µE 16V	QP12422339
2133		4822 124 22339	ELECT 100µE 16V	QP12422339
2134		4822 124 11947	ELECT 10µF 20% 16V	QP12411947
			DIODES	
6001				
∫		4822 130 11087	DIODE BZX284-C15	QP13011087
6006				
6007		4822 130 83757	DIODE BAS216	QP13083757
6008		4822 130 83757	DIODE BAS216	QP13083757
6009		4822 130 83757	DIODE BAS216	QP13083757
6010		4822 130 11087	DIODE BZX284-C15	QP13011087
			SEMICONDUCTORS	
7103		4822 209 17423	IC ANA UAD1328T	QP20917423
7110		4822 209 16978	IC ANA LF33CV	QP20916978
7115		4822 209 30095	IC ANA LM833D	QP20930095
7116		9322 141 80668	IC ANA AD8073	
7117		4822 209 72684	IC ANA L7905CV	QP20972684
7000		5322 130 60159	TRS. BC846B	QQ13060159
7001		4822 130 42804	TRS. BC817-25	QP13042804
7002		4822 130 60373	TRS. BC856B	QP13060373
7004		4822 130 42804	TRS. BC817-25	QP13042804
7005		4822 130 42804	TRS. BC817-25	QP13042804
7006		5322 130 60159	TRS. BC846B	QQ13060159
7007		5322 130 60159	TRS. BC846B	QQ13060159
7008		5322 130 60159	TRS. BC846B	QQ13060159
7009		4822 130 60373	TRS. BC856B	QP13060373
7010		5322 130 60159	TRS. BC846B	QQ13060159
7011		5322 130 60159	TRS. BC846B	QQ13060159
7012		4822 130 60373	TRS. BC856B	QP13060373

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
7013		5322 130 60159	TRS. BC846B	QQ13060159
7014		5322 130 60159	TRS. BC846B	QQ13060159
7015		4822 130 60373	TRS. BC856B	QP13060373
7016		5322 130 60159	TRS. BC846B	QQ13060159
7017		5322 130 60159	TRS. BC846B	QQ13060159
7018		5322 130 60159	TRS. BC846B	QQ13060159
7019		5322 130 60159	TRS. BC846B	QQ13060159
7104		4822 130 42804	TRS. BC817-25	QP13042804
7105		4822 130 42804	TRS. BC817-25	QP13042804
7108		4822 130 42804	TRS. BC817-25	QP13042804
7109		4822 130 42804	TRS. BC817-25	QP13042804
7112		4822 130 42804	TRS. BC817-25	QP13042804
7114		4822 130 42804	TRS. BC817-25	QP13042804
			RESISTORS	
3000		4822 051 20101	100R00 5% 0.1W	QP05120101
3001		4822 117 12521	68R 1% 0.1W	QP11712521
3005		4822 051 20472	4K70 5% 0.1W	QP05120472
3006		4822 051 20472	4K70 5% 0.1W	QP05120472
3007		4822 117 12955	2K7 1% 0.1W	QP11712955
3008		4822 117 10833	10k 1% 0.1W	QP11710833
3009		4822 051 20472	4K70 5% 0.1W	QP05120472
3010		4822 051 20472	4K70 5% 0.1W	QP05120472
3011		4822 051 20472	4K70 5% 0.1W	QP05120472
3012		4822 117 11152	4R7 5%	QP11711152
3014		4822 051 20101	100R00 5% 0.1W	QP05120101
3015		4822 117 12955	2K7 1% 0.1W	QP11712955
3016		4822 051 20101	100R00 5% 0.1W	QP05120101
3017		4822 117 12955	2K7 1% 0.1W	QP11712955
3036		4822 117 11449	2K2 5% 0.1W	QP11711449
3038		4822 051 20223	22K00 5% 0.1W	QP05120223
3039		4822 051 20223	22K00 5% 0.1W	QP05120223
3040		4822 116 83933	15K 1% 0.1W	QP11683933
3041		4822 051 20822	8K20 5% 0.1W	QP05120822
3043		4822 117 11504	270R 1% 0.1W	QP11711504
3044		4822 117 10833	10k 1% 0.1W	QP11710833
3045		4822 051 20101	100R00 5% 0.1W	QP05120101
3046		4822 051 20101	100R00 5% 0.1W	QP05120101
3047		4822 117 11507	6K8 1% 0.1W	QP11711507
3048		4822 117 11454	820R 1% 0.1W	QP11711454
3049		4822 117 11927	75R 1% 0.1W	QP11711927
3050		4822 051 20471	470R00 5% 0.1W	QP05120471
3051		4822 051 20472	4K70 5% 0.1W	QP05120472
3052		4822 117 10361	680R 1% 0.1W	QP11710361
3056		4822 117 11504	270R 1% 0.1W	QP11711504
3057		4822 117 11152	4R7 5%	QP11711152
3058		4822 051 20101	100R00 5% 0.1W	QP05120101
3059		4822 051 20101	100R00 5% 0.1W	QP05120101
3060		4822 117 11507	6K8 1% 0.1W	QP11711507
3061		4822 117 11454	820R 1% 0.1W	QP11711454
3062		4822 117 11927	75R 1% 0.1W	QP11711927
3063		4822 117 11449	2K2 5% 0.1W	QP11711449
3064		4822 051 20472	4K70 5% 0.1W	QP05120472
3065		4822 117 10361	680R 1% 0.1W	QP11710361
3068		4822 117 11504	270R 1% 0.1W	QP11711504
3069		4822 051 20101	100R00 5% 0.1W	QP05120101
3070		4822 117 11507	6K8 1% 0.1W	QP11711507
3071		4822 117 11454	820R 1% 0.1W	QP11711454
3072		4822 117 11927	75R 1% 0.1W	QP11711927
3073		4822 117 11449	2K2 5% 0.1W	QP11711449
3074		4822 051 20472	4K70 5% 0.1W	QP05120472
3075		4822 117 10361	680R 1% 0.1W	QP11710361
3077		4822 117 11927	75R 1% 0.1W	QP11711927
3078		4822 117 11449	2K2 5% 0.1W	QP11711449
3100		4822 051 20101	100R00 5% 0.1W	QP05120101
3101		4822 051 20472	4K70 5% 0.1W	QP05120472
3102		4822 117 10833	10k 1% 0.1W	QP11710833

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
3103		4822 117 10833	10k 1% 0.1W	QP11710833
3105		4822 117 10833	10k 1% 0.1W	QP11710833
3106		4822 117 10833	10k 1% 0.1W	QP11710833
3107		4822 051 20101	100R00 5% 0.1W	QP05120101
3108		4822 117 11152	4R7 5%	QP11711152
3109		4822 117 11152	4R7 5%	QP11711152
3110		4822 117 10833	10k 1% 0.1W	QP11710833
3112		4822 117 12955	2K7 1% 0.1W	QP11712955
3113		4822 117 12955	2K7 1% 0.1W	QP11712955
3114				
∫		4822 117 10833	10k 1% 0.1W	QP11710833
3117				
3118		4822 051 20101	100R00 5% 0.1W	QP05120101
3119		4822 051 20101	100R00 5% 0.1W	QP05120101
3120		4822 117 10833	10k 1% 0.1W	QP11710833
3121		4822 117 10833	10k 1% 0.1W	QP11710833
3122		4822 117 12955	2K7 1% 0.1W	QP11712955
3123		4822 117 12955	2K7 1% 0.1W	QP11712955
3124		4822 117 10833	10k 1% 0.1W	QP11710833
3126		4822 051 20101	100R00 5% 0.1W	QP05120101
3127		4822 117 10833	10k 1% 0.1W	QP11710833
3129		4822 117 12955	2K7 1% 0.1W	QP11712955
3130		4822 051 20101	100R00 5% 0.1W	QP05120101
3131		4822 117 10833	10k 1% 0.1W	QP11710833
3132		4822 117 12955	2K7 1% 0.1W	QP11712955
3135		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487
3136		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487
3137		4822 117 12635	10R 1% 0.125W	QP11712635
3138		4822 117 11139	1k5 1% 0.1W	QP11711139
3139		4822 117 11931	750R 1% 0.1W	QP11711931
3140		2120 108 92619	SM ERJ6EN 2K2PM1	
3141		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487
3142		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487
3143		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487
3144		4822 117 11953	560R 1% 0.1W	QP11711953
3145		2120 108 92625	SM ERJ6EN 5K6PM1	
3147		2120 108 92616	SM ERJ6EN 1k2 PM1	
3148		5322 117 12487	1k 1% 0.125W RC12G	QQ11712487
3150		4822 117 11927	75R 1% 0.1W	QP11711927
3153		4822 051 20101	100R00 5% 0.1W	QP05120101
3154		4822 117 11927	75R 1% 0.1W	QP11711927
3157		4822 117 11927	75R 1% 0.1W	QP11711927
3158		4822 117 11449	2K2 5% 0.1W	QP11711449
3159		4822 051 20101	100R00 5% 0.1W	QP05120101
3160		4822 117 10833	10k 1% 0.1W	QP11710833
			MISCELLANEOUS	
1002		2422 026 05047	CONNECTOR CINCH H 6P F RDWHYE B	QU02605047
1003		4822 267 10994	CONNECTOR 4P MDIN	QP26710994
1004		2422 025 16526	CONNECTOR 22P F 1.00 FFC 0.3 R	QU02516526
1005		4822 267 31729	CONNECTOR	QP26731729
1006		2422 026 05049	CON BM CINCH H 3P F	QU02605049
1007		2422 025 16525	CONNECTOR 16P F 1.00 FFC 0.3 R	QU02516525
5000		4822 157 70601	COIL 100UH (920927085A)	QP15770601
5003				
∫		4822 242 10756	FILTER L/C	QP24210756
5007			DSS306-92Y5S221M100	
7020		9322 155 28667	CONNECTOR GP1FA550TZ (SRPJ)L	

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
			AV CIRCUIT BOARD (/N1B)	
			CAPACITORS	
2032		4822 126 13482	CER. 470NF +80 -20% 16V	QP12613482
2353		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2354		4822 126 14076	CER. 220N 25V	QP12614076
2355		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2357		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2358		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2359		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2360		4822 126 13692	CER. 47pF 1% 63V	QP12613692
2361		4822 126 13692	CER. 47pF 1% 63V	QP12613692
2371		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2372		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2373		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2377		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2378		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2382		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2383		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2385		4822 124 40769	ELECT 4.7µF 20% 100V	QP12440769
2395		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2402		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2404		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2408		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2409		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2412		4822 124 40433	ELECT 47µF 20% 25V	QP12440433
2450		5322 122 32654	CER. 22N 63V	QQ12232654
2452		4822 126 14076	CER. 220N 25V	QP12614076
2453		4822 124 40433	ELECT 47µF 20% 25V	QP12440433
2455		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2456		4822 124 22339	ELECT 100µE 16V	QP12422339
2457		5322 126 10511	CER. 1NF 5% 50V	QQ12610511
2458		5322 122 32654	CER. 22N 63V	QQ12232654
2459		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2460		5322 122 32654	CER. 22N 63V	QQ12232654
2461		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2462		4822 124 22339	ELECT 100µE 16V	QP12422339
2463		5322 126 10511	CER. 1NF 5% 50V	QQ12610511
2464		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2469		5322 122 32654	CER. 22N 63V	QQ12232654
2471		4822 126 14585	CER. 100NF 10% 50V	QP12614585
2472		4822 124 40433	ELECT 47µF 20% 25V	QP12440433
2488		4822 126 14585	CER. 100NF 10% 50V	QP12614585
2495		4822 126 14585	CER. 100NF 10% 50V	QP12614585
2496		5322 122 32654	CER. 22N 63V	QQ12232654
2497		4822 124 81151	ELECT 22µF 50V	QP12481151
2498		4822 124 41584	ELECT 100µF 20% 10V	QP12441584
2499				
∫		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2505				
2506				
∫		4822 124 40763	ELECT 2.2µF 100V	QP12440763
2509				
2511		4822 124 40763	ELECT 2.2µF 100V	QP12440763
2520				
∫		4822 122 33575	CER. 220pF 5% 63V	QP12233575
2523				
2527				
∫		5322 122 32654	CER. 22N 63V	QQ12232654
2537				
2538		4822 124 40763	ELECT 2.2µF 100V	QP12440763
2539		4822 124 40763	ELECT 2.2µF 100V	QP12440763
2540		4822 124 40763	ELECT 2.2µF 100V	QP12440763
2541		4822 126 14585	CER. 100NF 10% 50V	QP12614585
2542		4822 126 14491	CER. 2.2µF 10V	QP12614491
2543		4822 126 13692	CER. 47pF 1% 63V	QP12613692
2544		4822 124 40248	ELECT 10µF 20% 63V	QP12440248
2545		4822 124 40433	ELECT 47µF 20% 25V	QP12440433

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
			DIODES	
6302		4822 130 83757	DIODE BAS216	QP13083757
6401		4822 130 11047	DIODE BZX284-C9V1	QP13011047
6403		4822 130 83757	DIODE BAS216	QP13083757
6404		4822 130 11383	DIODE BZX284-C5V1	QP13011383
			SEMICONDUCTORS	
7400		9322 134 92676	IC ANA L78L33	
7401		4822 209 17423	IC ANA UAD1328T	QP20917423
7403		4822 209 32071	IC ANA MC33079D	QP20932071
7900				
⟆		5322 209 14481	IC DIG HEF4053BT	QQ20914481
7905				
7917		4822 209 17512	IC ANA TEA6420D	QP20917512
7006		5322 130 60159	TRS. BC846B	QQ13060159
7007		5322 130 60159	TRS. BC846B	QQ13060159
7008		5322 130 60159	TRS. BC846B	QQ13060159
7009		4822 130 60373	TRS. BC856B	QP13060373
7010				
⟆		5322 130 60159	TRS. BC846B	QQ13060159
7014				
7300		4822 130 60373	TRS. BC856B	QP13060373
7301		5322 130 60159	TRS. BC846B	QQ13060159
7304		9322 134 86668	TRS. LF80C	
7310		5322 130 60159	TRS. BC846B	QQ13060159
7329		5322 130 60159	TRS. BC846B	QQ13060159
7330		5322 130 60159	TRS. BC846B	QQ13060159
7331		4822 130 40959	TRS. BC547B	QP13040959
7332		4822 130 60373	TRS. BC856B	QP13060373
7333		4822 130 41246	TRS. BC327-25	QP13041246
7334		5322 130 60159	TRS. BC846B	QQ13060159
7335		5322 130 60159	TRS. BC846B	QQ13060159
7402		4822 130 42804	TRS. BC817-25	QP13042804
7404				
⟆		4822 130 42615	TRS. BC817-40	QP13042615
7407				
7918				
⟆		5322 130 60159	TRS. BC846B	QQ13060159
7935				
7936				
⟆		4822 130 60373	TRS. BC856B	QP13060373
7939				
7941		4822 130 60373	TRS. BC856B	QP13060373
7942		4822 130 60373	TRS. BC856B	QP13060373
7943		5322 130 60159	TRS. BC846B	QQ13060159
7944		5322 130 60159	TRS. BC846B	QQ13060159
7945		4822 130 60373	TRS. BC856B	QP13060373
7946		4822 130 60373	TRS. BC856B	QP13060373
7947		5322 130 60159	TRS. BC846B	QQ13060159
7949		5322 130 60159	TRS. BC846B	QQ13060159
			RESISTORS	
3036		4822 117 11449	2K2 5% 0.1W	QP11711449
3038		4822 051 20223	22K00 5% 0.1W	QP05120223
3039		4822 117 10834	47k 1% 0.1W	QP11710834
3040		4822 051 20273	27K00 5% 0.1W	QP05120273
3041		4822 051 20822	8K20 5% 0.1W	QP05120822
3043		4822 117 13577	330R 1% 1.25W	QP11713577
3044		4822 051 20223	22K00 5% 0.1W	QP05120223
3045		4822 051 20101	100R00 5% 0.1W	QP05120101
3046		4822 051 20101	100R00 5% 0.1W	QP05120101
3049		4822 117 11927	75R 1% 0.1W	QP11711927
3050		4822 117 11503	220R 1% 0.1W	QP11711503
3056		4822 117 13577	330R 1% 1.25W	QP11713577
3058		4822 051 20101	100R00 5% 0.1W	QP05120101
3059		4822 051 20101	100R00 5% 0.1W	QP05120101
3062		4822 117 11927	75R 1% 0.1W	QP11711927
3063		4822 051 10102	1K00 2% 0.25W	QP05110102

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
3300		4822 117 13577	330R 1% 1.25W	QP11713577
3301		4822 051 20101	100R00 5% 0.1W	QP05120101
3313		4822 117 11503	220R 1% 0.1W	QP11711503
3314		4822 051 10102	1K00 2% 0.25W	QP05110102
3315		4822 051 20471	470R00 5% 0.1W	QP05120471
3316		4822 117 10834	47k 1% 0.1W	QP11710834
3318		4822 117 10834	47k 1% 0.1W	QP11710834
3319		4822 051 10102	1K00 2% 0.25W	QP05110102
3320		4822 117 10834	47k 1% 0.1W	QP11710834
3321		4822 051 20101	100R00 5% 0.1W	QP05120101
3322		4822 051 20101	100R00 5% 0.1W	QP05120101
3323		4822 051 20471	470R00 5% 0.1W	QP05120471
3325		4822 117 10834	47k 1% 0.1W	QP11710834
3339		4822 051 10102	1K00 2% 0.25W	QP05110102
3340		4822 051 10102	1K00 2% 0.25W	QP05110102
3343		4822 117 11927	75R 1% 0.1W	QP11711927
3345		4822 117 11927	75R 1% 0.1W	QP11711927
3347		4822 051 10102	1K00 2% 0.25W	QP05110102
3348		4822 051 10102	1K00 2% 0.25W	QP05110102
3349		4822 117 10834	47k 1% 0.1W	QP11710834
3351		4822 051 20471	470R00 5% 0.1W	QP05120471
3359		4822 117 10834	47k 1% 0.1W	QP11710834
3363		4822 051 10102	1K00 2% 0.25W	QP05110102
3366		4822 117 10834	47k 1% 0.1W	QP11710834
3394		4822 051 20471	470R00 5% 0.1W	QP05120471
3397		4822 117 10834	47k 1% 0.1W	QP11710834
3407		4822 117 11927	75R 1% 0.1W	QP11711927
3408		4822 117 11927	75R 1% 0.1W	QP11711927
3409		4822 117 11503	220R 1% 0.1W	QP11711503
3413		4822 117 10834	47k 1% 0.1W	QP11710834
3425		4822 117 11927	75R 1% 0.1W	QP11711927
3432		4822 117 11927	75R 1% 0.1W	QP11711927
3442		4822 051 20101	100R00 5% 0.1W	QP05120101
3444		4822 117 10833	10k 1% 0.1W	QP11710833
3445		4822 117 10833	10k 1% 0.1W	QP11710833
3446		4822 117 12955	2K7 1% 0.1W	QP11712955
3447		4822 117 12955	2K7 1% 0.1W	QP11712955
3448		4822 117 10833	10k 1% 0.1W	QP11710833
3451		4822 117 10833	10k 1% 0.1W	QP11710833
3453		4822 117 10833	10k 1% 0.1W	QP11710833
3454		4822 117 10833	10k 1% 0.1W	QP11710833
3455		4822 117 10833	10k 1% 0.1W	QP11710833
3457		4822 051 20101	100R00 5% 0.1W	QP05120101
3459		4822 117 10833	10k 1% 0.1W	QP11710833
3461		4822 117 10833	10k 1% 0.1W	QP11710833
3462		4822 117 12955	2K7 1% 0.1W	QP11712955
3463		4822 117 12955	2K7 1% 0.1W	QP11712955
3464		4822 117 10833	10k 1% 0.1W	QP11710833
3505		4822 051 20101	100R00 5% 0.1W	QP05120101
3507		4822 051 20101	100R00 5% 0.1W	QP05120101
3508		4822 117 12521	68R 1% 0.1W	QP11712521
3511		4822 117 10833	10k 1% 0.1W	QP11710833
3512		4822 117 10833	10k 1% 0.1W	QP11710833
3517		4822 051 20101	100R00 5% 0.1W	QP05120101
3519		4822 051 20562	5K6 5% 0.1W	QP05120562
3610		4822 051 20472	4K70 5% 0.1W	QP05120472
3611		4822 051 20472	4K70 5% 0.1W	QP05120472
3612		4822 117 10834	47k 1% 0.1W	QP11710834
3613		4822 117 12955	2K7 1% 0.1W	QP11712955
3614		4822 051 20223	22K00 5% 0.1W	QP05120223
3615		4822 117 11152	4R7 5%	QP11711152
3616		4822 051 20472	4K70 5% 0.1W	QP05120472
3617		4822 117 10833	10k 1% 0.1W	QP11710833
3618		4822 051 10102	1K00 2% 0.25W	QP05110102
3619		4822 117 10833	10k 1% 0.1W	QP11710833
3620		4822 051 10008	0R00 5% 0.25W	QP05110008
3621		4822 051 20472	4K70 5% 0.1W	QP05120472

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
3622		4822 117 10833	10k 1% 0.1W	QP11710833
3623		4822 051 20472	4K70 5% 0.1W	QP05120472
3624		4822 117 10833	10k 1% 0.1W	QP11710833
3625		4822 051 10102	1K00 2% 0.25W	QP05110102
3629		4822 117 11927	75R 1% 0.1W	QP11711927
3632		4822 051 20101	100R00 5% 0.1W	QP05120101
3634		4822 117 11449	2K2 5% 0.1W	QP11711449
3635		4822 117 11503	220R 1% 0.1W	QP11711503
3636				
∫		4822 117 10837	100k 1% 0.1W	QP11710837
3643				
3646		4822 117 10837	100k 1% 0.1W	QP11710837
3647		4822 117 10837	100k 1% 0.1W	QP11710837
3648				
∫		4822 117 13577	330R 1% 1.25W	QP11713577
3651				
3653		4822 117 13577	330R 1% 1.25W	QP11713577
3672				
∫		4822 117 11927	75R 1% 0.1W	QP11711927
3675				
3676		4822 117 10353	150R 1% 0.1W	QP11710353
3677		4822 117 11927	75R 1% 0.1W	QP11711927
3678				
∫		4822 051 20101	100R00 5% 0.1W	QP05120101
3685				
3687		4822 051 20472	4K70 5% 0.1W	QP05120472
3688		4822 051 20101	100R00 5% 0.1W	QP05120101
3689		4822 051 20101	100R00 5% 0.1W	QP05120101
3690				
∫		4822 051 10102	1K00 2% 0.25W	QP05110102
3694				
3695		4822 117 10833	10k 1% 0.1W	QP11710833
3696		4822 117 10833	10k 1% 0.1W	QP11710833
3697				
∫		4822 051 10102	1K00 2% 0.25W	QP05110102
3700				
3701		4822 051 20471	470R00 5% 0.1W	QP05120471
3702		4822 051 10102	1K00 2% 0.25W	QP05110102
3703				
∫		4822 117 11507	6K8 1% 0.1W	QP11711507
3707				
3720		4822 117 11148	56K 1% 0.1W	QP11711148
3721		4822 117 10353	150R 1% 0.1W	QP11710353
3722		4822 117 11148	56K 1% 0.1W	QP11711148
3723		4822 117 11148	56K 1% 0.1W	QP11711148
3724				
∫		4822 051 20229	22R00 5% 0.1W	QP05120229
3731				
3732				
∫		4822 117 13577	330R 1% 1.25W	QP11713577
3747				
3748				
∫		4822 117 10837	100k 1% 0.1W	QP11710837
3761				
3762		4822 117 11504	270R 1% 0.1W	QP11711504
3763		4822 051 20101	100R00 5% 0.1W	QP05120101
3764		4822 117 10833	10k 1% 0.1W	QP11710833
3765		4822 117 10833	10k 1% 0.1W	QP11710833
3768				
∫		4822 117 10834	47k 1% 0.1W	QP11710834
3772				
3773		4822 117 10833	10k 1% 0.1W	QP11710833
3774		4822 117 10834	47k 1% 0.1W	QP11710834
3800		4822 051 20472	4K70 5% 0.1W	QP05120472
3801		4822 051 20472	4K70 5% 0.1W	QP05120472
!3802		4822 117 11152	4R7 5%	QP11711152
!3803		4822 117 11152	4R7 5%	QP11711152
3804		4822 117 10834	47k 1% 0.1W	QP11710834
3805		4822 117 10833	10k 1% 0.1W	QP11710833

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
3999		4822 117 12842		QP11712842
			MISCELLANEOUS	
1300		4822 265 11154	CONNECTOR 52030-2210 (22P)	QP26511154
1301		4822 265 11103	CONNECTOR 52030-1610 (16P)	QP26511103
1303		4822 267 10994	CONNECTOR 4P MDIN	QP26710994
1304		2422 033 00334	CON BM EURO H 42P F BK GRND-L	QU03300334
1402		4822 265 11566	CONNECTOR 3P YKC21-3930	QP26511566
1405		4822 267 31729	CONNECTOR	QP26731729
1410		4822 265 41392	CONNECTOR B7B-EH-A	QP26541392
5400		4822 157 70601	COIL 100µH (920927085A)	QP15770601
6400		4822 130 10845	CONNECTOR GP1F32T	QP13010845
			FRONT CIRCUIT BOARD	
			CAPACITORS	
2100	/N1B	4822 122 33575	CER. 220pF 5% 63V	QP12233575
2101	/N1B	4822 122 33575	CER. 220pF 5% 63V	QP12233575
2102		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2103		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
2105		4822 126 12105	CER. 33NF 50V	QP12612105
2106		4822 124 40248	ELECT 10µF 20% 63V	QP12440248
2107				
∫		4822 126 12105	CER. 33NF 50V	QP12612105
2111				
2114		5322 122 32658	CER. 22pF 5% 50V	QQ12232658
2115		5322 122 32658	CER. 22pF 5% 50V	QQ12232658
2116		4822 126 12105	CER. 33NF 50V	QP12612105
2117		4822 124 40248	ELECT 10µF 20% 63V	QP12440248
2122		4822 126 12105	CER. 33NF 50V	QP12612105
2123		4822 124 11947	ELECT 10µF 20% 16V	QP12411947
2124		3198 028 42290	ELECT 22µF 35V	
2125		5322 122 32658	CER. 22pF 5% 50V	QQ12232658
2126		4822 124 40248	ELECT 10µF 20% 63V	QP12440248
2128		5322 122 31647	CER. 1NF 10% 63V	QQ12231647
2129		3198 028 42290	ELECT 22µF 35V	
2130		3198 028 42290	ELECT 22µF 35V	
2201		4822 126 12105	CER. 33NF 50V	QP12612105
2211		5322 122 32531	CER. 100pF 5% 50V	QQ12232531
			DIODES	
6100	/N1B	4822 130 83757	DIODE BAS216	QP13083757
6101		4822 130 11666	DIODE BZX284-C8V2	QP13011666
6102		4822 130 10794	DIODE BZX284-C10	QP13010794
6104		4822 130 83757	DIODE BAS216	QP13083757
6200		4822 130 82978	LED LTL-16KPE-P	QP13082978
			SEMICONDUCTORS	
7104	/N1B	3104 123 94532	IC DIG TMP87CH74F-1E29-V2.18-DVDSLAVE	QW12394532
7104	/A1B, /S1G,/U1B	3104 123 94761	IC DIG ROM TMP87CH74	QW12394761
7112		4822 209 31257	IC ANA MC79L24ACP	QP20931257
7100		5322 130 60159	TRS. BC846B	QQ13060159
7101	/N1B	5322 130 60159	TRS. BC846B	QQ13060159
7102		5322 130 60159	TRS. BC846B	QQ13060159
7103		5322 130 60159	TRS. BC846B	QQ13060159
7105		4822 130 40855	TRS. BC337	QP13040855
7106		4822 130 40854	TRS. BC327	QP13040854
7107		5322 130 60159	TRS. BC846B	QQ13060159
7108		5322 130 60159	TRS. BC846B	QQ13060159
7109		4822 130 60373	TRS. BC856B	QP13060373
7110		4822 212 30842	REMOTE RECEIVER TSOP1736SB1	QP21230842

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)
			RESISTORS	
3100	/N1B	4822 051 20223	22K00 5% 0.1W	QP05120223
3101	/N1B	4822 051 20273	27K00 5% 0.1W	QP05120273
3102	/N1B	4822 117 10834	47k 1% 0.1W	QP11710834
3103		4822 117 11149	82k 1% 0.1W	QP11711149
3104	/N1B	4822 117 10837	100k 1% 0.1W	QP11710837
3106	/N1B	4822 117 11503	220R 1% 0.1W	QP11711503
3108		4822 117 11149	82k 1% 0.1W	QP11711149
3109				
∫		4822 051 20472	4K70 5% 0.1W	QP05120472
3113				
3114		4822 051 20109	10R00 5% 0.1W	QP05120109
3115		4822 051 20472	4K70 5% 0.1W	QP05120472
3116		4822 117 11149	82k 1% 0.1W	QP11711149
3117		4822 117 11152	4R7 5%	QP11711152
3118		4822 117 10833	10k 1% 0.1W	QP11710833
3119		4822 117 10833	10k 1% 0.1W	QP11710833
3120		4822 051 20471	470R00 5% 0.1W	QP05120471
3121		4822 051 20472	4K70 5% 0.1W	QP05120472
3122		4822 051 20109	10R00 5% 0.1W	QP05120109
3123		4822 117 10833	10k 1% 0.1W	QP11710833
3125		4822 051 20109	10R00 5% 0.1W	QP05120109
3130		4822 051 20109	10R00 5% 0.1W	QP05120109
3131		4822 117 11152	4R7 5%	QP11711152
3132		4822 117 13577	330R 1% 1.25W	QP11713577
3133		4822 051 20109	10R00 5% 0.1W	QP05120109
3134		4822 117 13577	330R 1% 1.25W	QP11713577
3135		4822 117 11503	220R 1% 0.1W	QP11711503
3136		4822 051 10102	1K00 2% 0.25W	QP05110102
3137		4822 117 10833	10k 1% 0.1W	QP11710833
3138		4822 051 20471	470R00 5% 0.1W	QP05120471
3139		4822 051 20472	4K70 5% 0.1W	QP05120472
3140		4822 117 10833	10k 1% 0.1W	QP11710833
3142		4822 117 13577	330R 1% 1.25W	QP11713577
3143		4822 117 10833	10k 1% 0.1W	QP11710833
3144		4822 117 10837	100k 1% 0.1W	QP11710837
3145		4822 117 10833	10k 1% 0.1W	QP11710833
3151		4822 051 20101	100R00 5% 0.1W	QP05120101
			MISCELLANEOUS	
0002		3139 244 00440	FTD HOLDER DVD711	QT24400440
0020	/A1B, /S1G,/U1B	2422 025 04849	CONNECTOR,BMT 2P	QU02504849
1100		4822 276 13775	SWITCH PUSH BUTTON	QP27613775
1101		4822 276 13775	SWITCH PUSH BUTTON	QP27613775
1102		4822 276 13775	SWITCH PUSH BUTTON	QP27613775
1106				
∫		4822 276 13775	SWITCH PUSH BUTTON	QP27613775
1109				
1110		2422 540 98423	RES CER 8MHZ CSTS*MG03	QU54098423
1111	/N1B	4822 276 13775	SWITCH PUSH BUTTON	QP27613775
1113		2722 171 07172	VIDEO DECODER UNIT 14-MT-27GNK	
1115		4822 267 10565	CONNECTOR PRINTED CIRCUIT 4P	QP26710565
1117	/N1B	4822 267 10565	CONNECTOR PRINTED CIRCUIT 4P	QP26710565
1117	/A1B, /S1G,/U1B	2412 020 00724	CONNECTOR 2P	
1118		4822 267 10637	CONNECTOR 5P	QP26710637
1205	/N1B	4822 267 10567	CONNECTOR 4P	QP26710567
1205	/A1B, /S1G,/U1B	2422 025 12488	CONNECTOR 2P	QU02512488

POS. NO	VERS. COLOR	PART NO. (PCS)	DESCRIPTION	PART NO. (MJI)

– CAUTION –

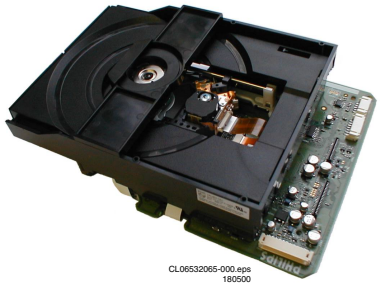
For repairing the DVD Module ADS-1, the serice application software "ComPair" is needed. The application CD-ROM "ComPair" is available via MARANTZ orgauization or PCS. <Refer the page 5> A "service Bulletin" will oublish the latest "ComPair" information.

DVD-Video Player

DVD Module ASD-1

(Euro) 3104 129 21910
(Non euro) 3104 129 21920

Service
Service
Service



Service Manual

DVD VIDEO COMPACT disc DIGITAL VIDEO COMPACT disc DIGITAL AUDIO

Contents **Page**

Published by MT0065 Service DPS Hasselt Printed in the Netherlands Subject to modification GB 3122 785 10840

PHILIPS

1. Technical Specifications

1.1 Connections

1.1.1 Connector 1600: Supply input connector.

1. +3V3stby
2. +3V3stby
3. +5V
4. +5Vstby
5. Vreserved
6. GND
7. GND
8. GND
9. -8Vstby
10. Standby control line
11. +12Vstby
12. GND

1.1.2 Connector 1603: A/V 1 connector.

1. P50
2. Blue Video
3. Green Video
4. GND
5. Red Video
6. CVBS
7. GND
8. Slow blanking scart
9. -8Vstby
10. +5V
11. +5V
12. Audio mute
13. GND
14. I2S data0 out
15. I2S wordselect
16. I2S bitclock
17. GND
18. I2S systemclock
19. Center_on
20. Kar_bypass
21. Kar_bypass
22. GND

1.1.3 Connector 1604: A/V 2 connector.

1. GND
2. Hor. sync.
3. GND
4. I2S data 2 out
5. GND
6. I2S data 1 out
7. -8Vstby
8. I2C clock
9. +12Vstby
10. I2C data
11. Vreserved
12. +3V3
13. GND
14. C video
15. GND
16. Y video

1.1.4 Connector 1501: I2C interface connector.

1. I2C clock
2. GND
3. I2C data
4. Standby control line
5. P50

1.1.5 Connector 1602: Service connector.

1. TXD
2. Service activation
3. RXD
4. Reserved for RTS
5. 5: GND
6. Reserved for CTS
7. +5V

1.2 Signal specifications

This the specification of all signals as described under “Connections”
H = +5V ±0.5V
h = 3V3 ±0.3V
L = 0V ±0.5V
l = 0V ±0.3V

Stby	:	If the set supports a “standby” function, all supply voltages marked with “stby” have to stay on during standby.
Standby control line	:	HStandby mode
	:	LOn mode.
P50	:	Connection between front and A/V board, and can be used as P50 signal line. The signal is not connected to the module electronics.
Slow blanking scart	:	This signal switches between
	:	0V (220Ωoutput impedance)
	:	12Vstby/2 (455Ω output impedance)
	:	12vstby (690Ω output impedance)
Audio mute	:	Can be used for audio mute transistors during stop or power on/off.
	:	Mute on : +5Vstby
	:	Mute off: -8Vstby via a 10kΩ resistor.
I2S data0 out	:	I2S front data output.
	:	Level h/l
I2S wordselect / I2S bitclock	:	I2S timing signals
	:	Level h/l
I2S systemclock	:	256xFS audio systemclock.
	:	Level H/L
Kar_bypass	:	Bypasses the karaoke chip on the A/V board.
	:	Bypass activeH
	:	Bypass offL
Center_on	:	Switches the center audio to the scart output.
	:	Center to scarth
	:	L/R to scartl
SPDIF out	:	Digital audio output
	:	Level H/L

Hor. Sync	:	Video Horizontal synchronisation
	:	Level h/l
I2S data1 out	:	I2S surround data output.
	:	Level: h/l.
I2S data2 out	:	I2S center/sub data output.
	:	Level h/l.
I2C clock / I2C data	:	I2C databus
	:	Level: H/L
TXD / RXD / RTS / CTS	:	Service UART to be connected direct to PC serial input.
	:	Output levelsH/L
	:	Input levelsRS232 compliant
Service activation	:	Signal openNormal module start-up
	:	Signal tied to GND Module start-up in service mode.
Vreserved	:	Reserved in case the A/V board requires an extra supply voltage.
	:	This supply is limited by a positive polarised 47uF/16V elco + 100nF/16V.

1.3 Performance:

1.3.1 Digital output

CDDA/LPCM	:	according IEC958
MPEG1 is converted to LPCM	:	
MPEG2, AC3 audio.	:	according IEC1937
DTS.	:	according IEC61937 amendment 1.
	:	Digital output level is 0V / 5V with GND as reference. To meet the standards a decouple circuit is necesary.

1.3.2 I2S output

Accuracy	:	Up to 24bit.
Sample rate	:	44.1kHz / 48kHz.
Standard	:	Philips I2S output
Number of I2S outputs	:	3 (6 channel: Front / Surround / Center-Bass)
Deemphasis	:	Already processed in module.
Audio source streams	:	CDDA / MPEG1 / LPCM / MPEG2 / AC3
	:	No DTS decoding.
Audio trick modes	:	Dolby Pro Logic (multichannel downmix on front output)
	:	3D sound.

1.3.3 Analog output

The module has no analog audio ouput.	:	The analog audio specification will be determined by the external DAC circuit.

1.3.4 Video.

Standards	:	The video output standard will follow the source material.
	:	The OSD standard is switchable between PAL or NTSC.
Outputs	:	The module has 6 analog outputs (3 formats): Y/C CVBS RGB.
Specification.	:	The output is fully according PQR3 IMS except
	:	Output load>1kΩ to GND / Cap. load <47pF.
	:	Level0.5Vpp with 100% white
	:	DC-levelSync bottom = -0.65V ±10%
	:	Some specification points are significantly better then PQR3
	:	SNR on all video outputs is better then 60dB.
	:	Video bandwidth >5MHz (±3dB)

2. Warnings and Laser safety instructions

GB **WARNING**

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD).
Careless handling during repair can reduce life drastically.
When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.
Keep components and tools also at this potential.

ESD

NL **WAARSCHUWING**

Alle IC's en vele andere halfgeleiders zijn gevoelig voor elektrostatische ontladingen (ESD).
Onzorgvuldig behandelen tijdens reparatie kan de levensduur drastisch doen verminderen.
Zorg ervoor dat u tijdens reparatie via een polsband met weerstand verbonden bent met hetzelfde potentiaal als de massa van het apparaat.
Houd componenten en hulpmiddelen ook op ditzelfde potentiaal.

F **ATTENTION**

Tous les IC et beaucoup d'autres semi-conducteurs sont sensibles aux décharges statiques (ESD).
Leur longévité pourrait être considérablement écourtée par le fait qu'aucune précaution n'est prise a leur manipulation.
Lors de réparations, s'assurer de bien être relié au même potentiel que la masse de l'appareil et enfiler le bracelet serti d'une résistance de sécurité.
Veiller a ce que les composants ainsi que les outils que l'on utilise soient également a ce potentiel.

D **WARNUNG**

Alle IC und viele andere Halbleiter sind empfindlich gegen elektrostatische Entladungen (ESD).
Unsorgfältige Behandlung bei der Reparatur kann die Lebensdauer drastisch vermindern.
Sorgen sie dafür, das Sie im Reparaturfall über ein Pulsarmband mit Widerstand mit dem Massepotential des Gerätes verbunden sind.
Halten Sie Bauteile und Hilfsmittel ebenfalls auf diesem Potential.

I **AVVERTIMENTO**

Tutti IC e parecchi semi-conduttori sono sensibili alle scariche statiche (ESD).
La loro longevita potrebbe essere fortemente ridatta in caso di non osservazione della piu grande cauzione alla loro manipolazione.
Durante le riparazioni occorre quindi essere collegato allo stesso potenziale che quello della massa dell'apparecchio tramite un braccialetto a resistenza.
Assicurarsi che i componenti e anche gli utensili con quali si lavora siano anche a questo potenziale.

GB

Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.

NL

Veiligheidsbepalingen vereisen, dat het apparaat in zijn oorspronkelijke toestand wordt terug gebracht en dat onderdelen, identiek aan de gespecifieerde worden toegepast.

D

Bei jeder Reparatur sind die geltenden Sicherheitsvorschriften zu beachten.
Der Originalzustand des Gerats darf nicht verandert werden.
Fur Reparaturen sind Original-Ersatzteile zu verwenden.

I

Le norme di sicurezza esigono che l'apparecchio venga rimesso nelle condizioni originali e che siano utilizzati pezzi di ricambiago idetici a quelli specificati.

F

Les normes de sécurité exigent que l'appareil soit remis a l'état d'origine et que soient utilisées les pièces de rechange identiques à celles spécifiées.

SHOCK, FIRE HAZARD SERVICE TEST:

CAUTION: After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom,
Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before return to user/customer.
Ref.UL Standard NO.1492.

NOTE ON SAFETY:

Symbol ⚠ : Fire or electrical shock hazard. Only original parts should be used to replace any part with symbol ⚠
Any other component substitution(other than original type), may increase risk or fire or electrical shock hazard.

"Pour votre sécurité, ces documents doivent être utilisés par des spécialistes agrées, seuls habilités à réparer votre appareil en panne."

LASER SAFETY

This unit employs a laser. Only a qualified service person should remove the cover or attempt to service this device, due to possible eye injury.

LASER DEVICE UNIT

Type:	SemiconductorlaserGaAlAs
Wave length:	650 nm (DVD)
	780 nm (VCD/CD)
Output Power:	7 mW (DVD)
	10 mW (VCD/CD)
Beam divergence:	60 degree

USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURE OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.

AVOID DIRECT EXPOSURE TO BEAM

WARNING

The use of optical instruments with this product will increase eye hazard.
Repair handling should take place as much as possible with a disc loaded inside the player

WARNING LOCATION: INSIDE ON LASER COVERSHIELD

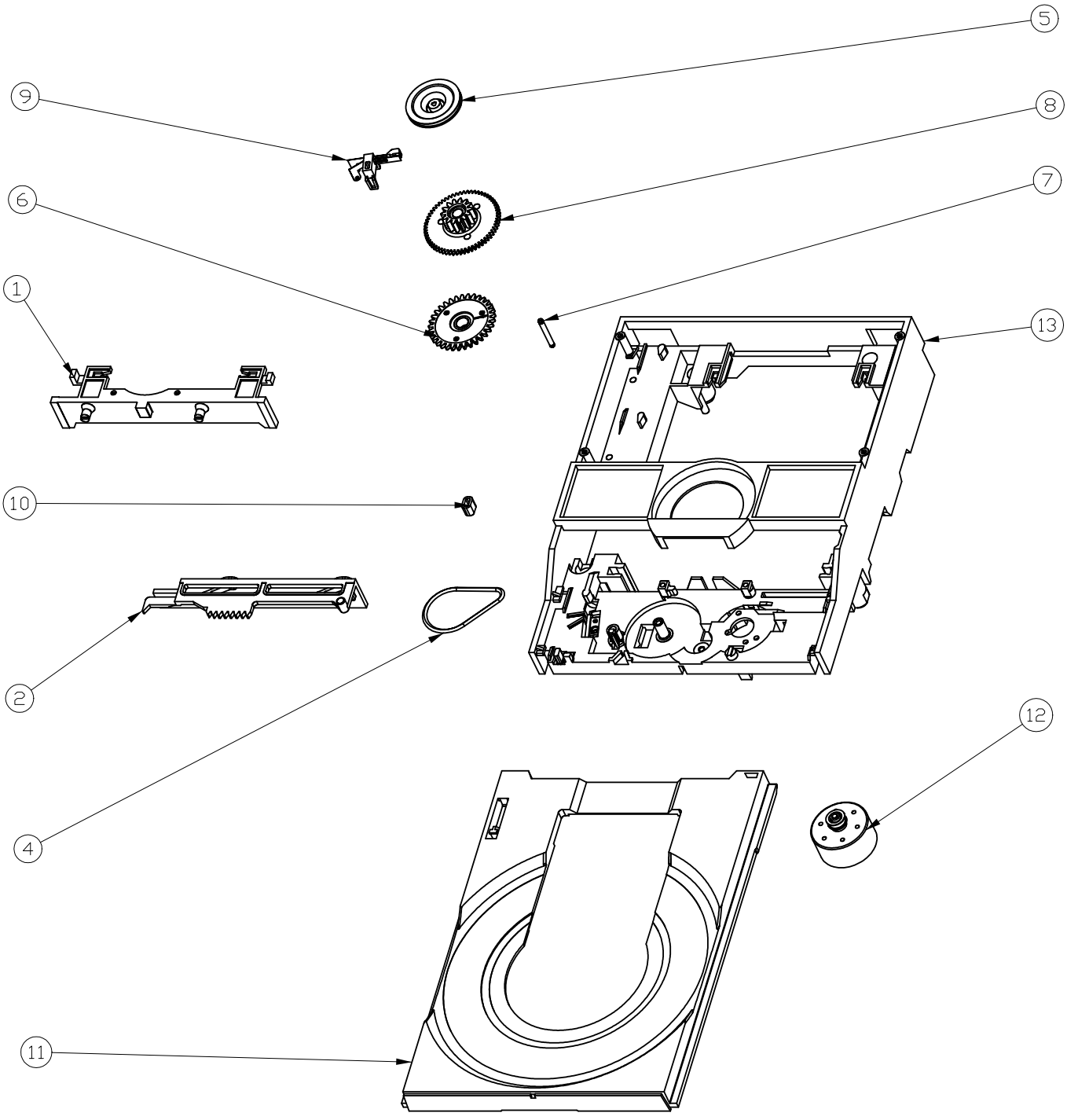
CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING
ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN
VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN
VARO! AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN
VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETSEN
DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

CL 06532065_051.eps
230500

3. Directions for use

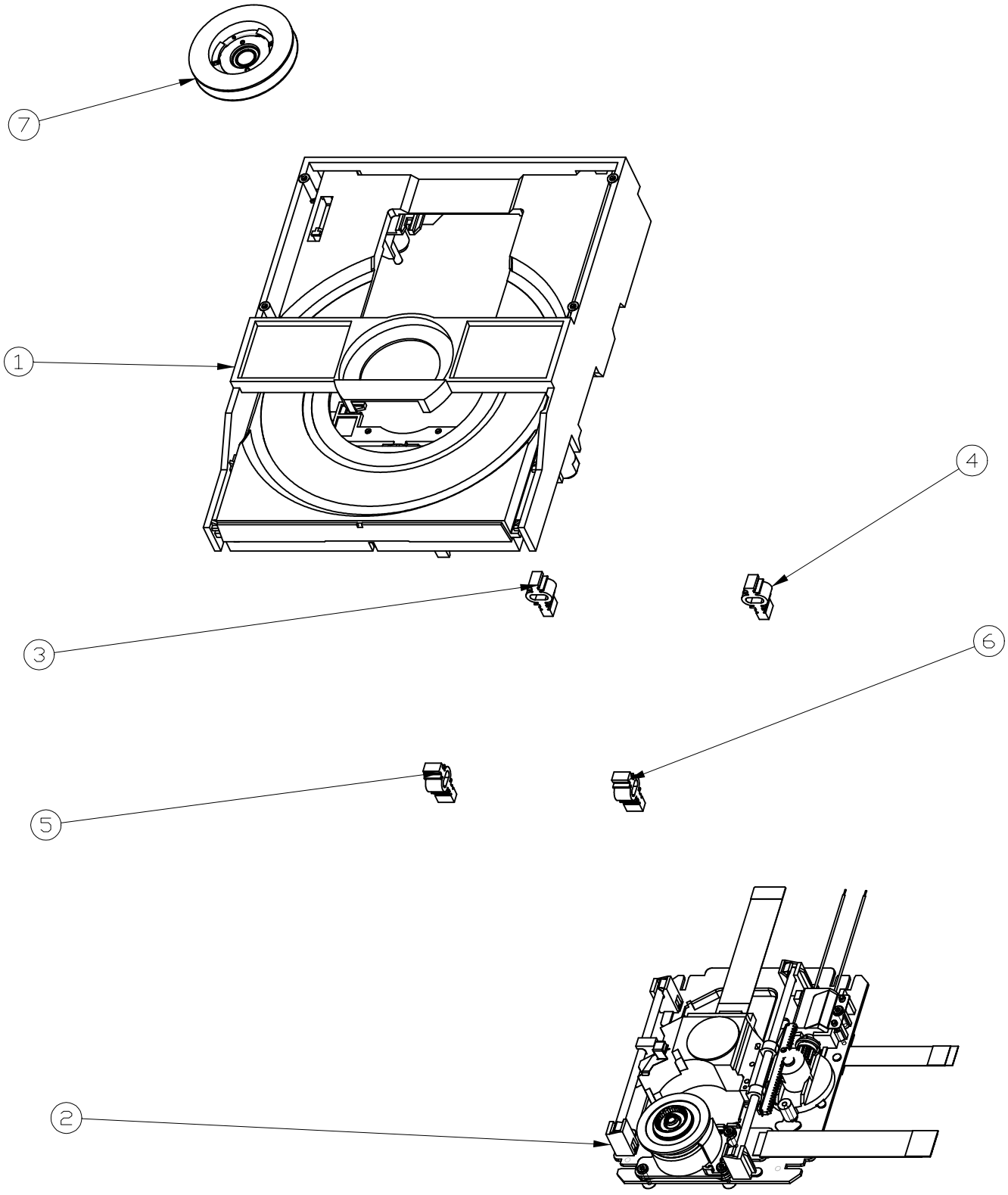
There is no DFU available

4. Mechanical instructions



4	4822 358 10266	BELT
9	3139 198 80010	SWITCH
10	4822 532 13097	TULE
11	3139194 00270	TRAY
12	3139 197 50060	TRAY MOTOR ASSY

CL06532065-001.eps
180500



	9305 023 61101	VAL6011/01 LOADER COMPLETE
1	3139 197 60090	GENEVA LP LOADER ASSY
2	9305 022 60101	VAM6001/01
3+4	3139 194 00710	SUSPENSION (YELLOW)
5+6	3139 194 00620	SUSPENSION (BLUE)
7	3139 197 60060	CLAMPER ASSY

CL06532065-002.eps
180500

5. Test instructions mono board DVD-ASD1

5.1 General

- Impedance of measuring-equipment should be > 1MΩ.
- Most tests have to be done by software commands. Together with the software command you will find a Ref.# nbr. This is the number of the diagnostic nulceus used for this test. More detailed information can be find in the chapter “Diagnostic Nuclei”.
- Levels: Most measurements are digital measurements. The high and low levels in this document got to have next specification:
  low : < 0.3V
  high : > 3.0V
  LOW : < 0.4V
  HIGH : > 4.5V
- All voltages marked with “stby” have to stay on during standby.

5.2 General start-up measurements

5.2.1 Supply check:

Pin nbr.	Supply
1600-1	3V3
1600-2	3V3
1600-3	+5V0V during STAND BY
1600-4	+5Vstby
1600-5	+6V
1600-6	0V
1600-7	0V
1600-8	0V
1600-9	-8V
1600-10	0V5V during STAND BY
1600-11	+12Vstby

0V

Check the supply currents to be sure there are no large failures on the board. Before measuring the currents, make sure that no A/V board, display board or Mercury 1 loader is connected to the mono board and that the PC interface cable is connected to the board.
Also check if the servo part gets its power.
Testpoint F608: +3V3 ±5%
Testpoint F101: +9V ±5%
The supply currents can be measured using a Tektronix AM503B current probe.

Supply	power consumption	
3V3	400mA ±10%	
5V	370mA ±10%	
5Vstby	< 5mA	
-8V	55mA ±10%	fluctuation: ±20mA
12Vstby	30mA ±20%	fluctuation: ±150mA

5.2.2 Reset check:

The reset circuit is triggered by the stand-by line. First make sure that the STB_CONT line is HIGH by connecting 5V to testpoint F505.
Then switch STB_CONT over to LOW and check next timing at the STI5505 reset input (testpoint F503):

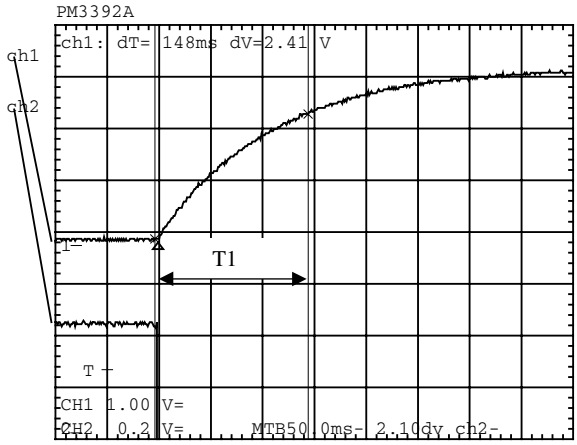


Figure 5-1

T 1 = 150msec ±25% (From 0V to 3V3 -3db)
If the reset input doesn’t go high then check the circuit around transistor 7501.

5.2.3 Clock check

To check the correct functioning of the STI5505, we first have to check the presence of all clocks.
All clocks to be measured with 0.02% tolerance.

Clock-name	Testpoint	Frequency
27M_CLK	F051	27MHz
PCM_CLK	F566	11.2896MHz

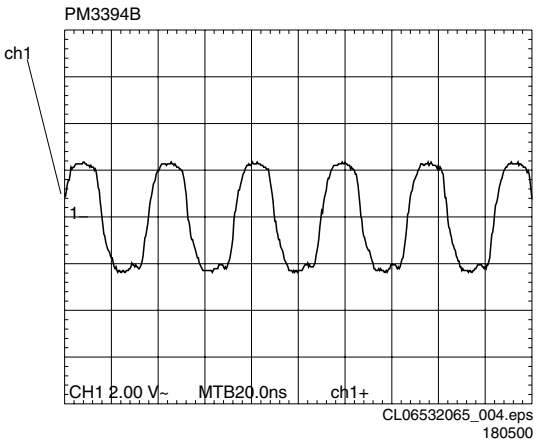


Figure 5-2

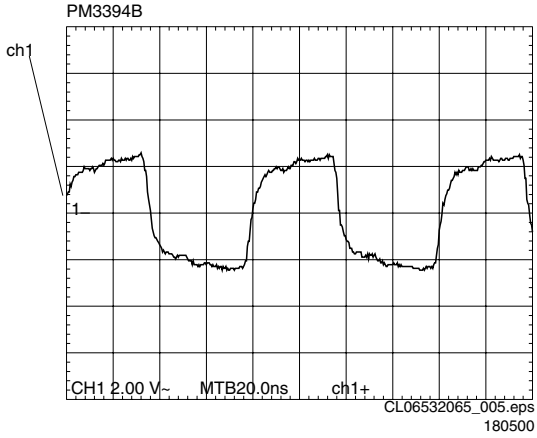


Figure 5-3

5.3 µP environment:

5.3.1 General:

All the tests are carried out by software tests. To start the software tests, connect a PC to the serial bus of the STI5505. Use connector 1602 for this connection:

Connector pin	Signal
1602-1	TXD (STI5505 out)
1602-2	Service-mode select
1602-3	RXD (STI5505 in)
1602-4	RTS (STI5505 out)
1602-5	GND
1602-6	CTS (STI5505 in)
1602-7	+5V

Now start the terminal program. Make sure that the service-pin of the µP is pulled low
(pin 1602-2) and then reset the µP (make the STB_CONT line low). The terminal program of your PC should now display: "DVD2 Diagnostic software version ...". This message already means that the µP is running. The first 5 commands from the diagnostic software will be carried out automaticly during diagnostic start-up. The other commands can be carried out by selecting the "command input". Just type the reference nbr. to do the test.
To be sure that the µP is able to run the diagnostic software, serial port will be checked during start-up.

Ref. #	Reference Name	Remark
(1)	BasicSpAcc	Serial port Access test/initialisation
(2)	BasicDramWrR	DRAM Write Read

5.3.2 Memory check:

The µP has a data bus that is connected to a DRAM (not present!!) and a Flash.
The µP has also an internal link to the MPEG SDRAM interface.
Next databus checks will be done at start-up to check this data-bus and SDRAM bus.

Ref. #	Command Name	Remark
(2b)	BasicInterconSDRAM	Data and address bus Interconnection
(2c)	BasicInterconFlash	Data and address bus Interconnection

There are 2 memory checks left that can be done by hand command

Ref. #	Command Name	Remark
6	PapChksFl	Checksum FLASH
16	CompSdramWrR	SDRAM Write Read

5.4 General I/O port & peripherals check

5.4.1 I2C bus / EEprom check

To access the EEprom, the I2C bus is used. So by writing and reading to the EEprom the chip and the bus is checked. With next commands a certain byte is written to the EEprom. The original information will always be written back into the EEprom.

Ref. #	Command Name	Remark
11	PapI2cNvram	I2C NVRAM access

The complete Eeprom can also be checked on failures by writing to all addresses and reading back. This test takes a long time (110 sec).

Ref. #	Command Name	Remark
15	PapNvramWrR	NVRAM Write Read

5.4.2 Audio clock switch check

For a DVD disc the audio clock has to be switched from 44.1KHz sampling to 48KHz sampling.
To do so IO-port 1 / 4 has to be switched. Send next commands and check the audio-clock

Ref. #	Remark	Testpoint	Frequency
7a	(Clock A_CLK in 44.1kHz mode)	F566	11.2896MHz ± 0.02%
7b	(Clock A_CLK in 48kHz mode)	F566	12.288MHz ± 0.02%

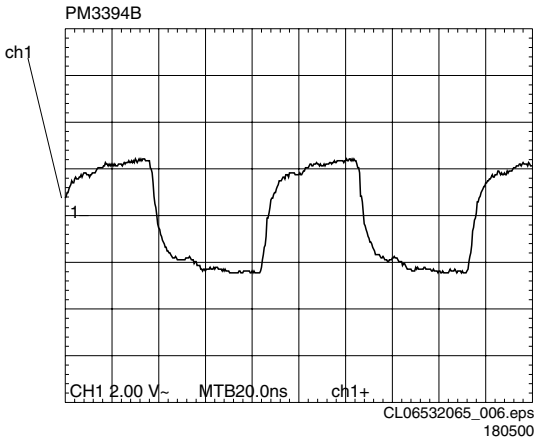


Figure 5-4

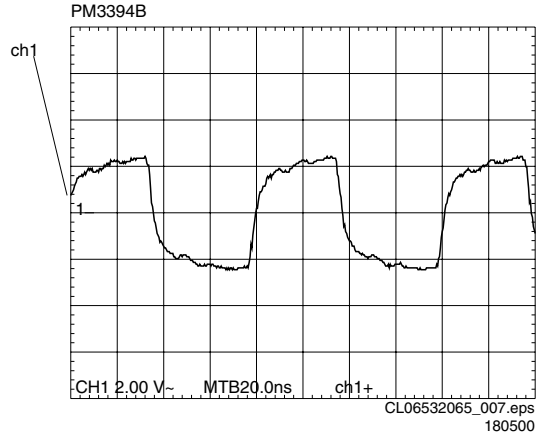


Figure 5-5

5.4.3 Audio deemphasise check

The STI5505 output pins PIO 4-0 and PIO 4-1 were used to switch deemphasis on a previous type of DAC. This function is not used anymore, because deemphasis is done internally in STI5505, but the name still remains. The lines are now used for a series of functions such as centre_on_stereo or karaoke_bypass. The PIO 4-0 has got a pull-up to +5V and the PIO 4-1 has not. To check these pins these commands can be used.

Ref. #	Command Name	Remark	Testpoint	Value
18e	AudioDeemp0TristateOn	PIO 4-0 Tristate On	------	
56a	AudioDeemp0On	PIO 4-0 On	F630	HIGH
56b	AudioDeemp0Off	PIO 4-0 0 Off	F630	low
18f	AudioDeemp0TristateOff	PIO 4-0 Tristate Off	------	
56c	AudioDeemp1On	PIO 4-1 On	F633	high
56d	AudioDeemp1Off	PIO 4-1 Off	F633	low

5.4.4 Audio mute check

Switch on the Mute circuit by sending next command:

Ref. #	Command Name	Remark
19a	AudioMuteOn	AudioMuteOn

Check the Mute output again at testpoint F625: 4.7V ±10%
Switch off the Mute circuit by sending next command

Ref. #	Command Name	Remark
19a	AudioMuteOff	AudioMuteOff

Check the Mute output at testpoint F625: -8V ±10%

5.4.5 Audio I2S check

To check the audio output, connect a audio DAC to the I2S output (DVD950 A/V board) and start-up the audio test. Look at the audio outputs from the A/V board for both sine and pink noise.

Ref. #	Command Name	Remark	Audio outputs
21a	AudioSineOn	Audio Sine signal Off	Audio Sine signal On Sine, 1kHz on stereo Press stop button
20a	AudioPinkNoiseOn	Audio Pinknoise On	Pink Noise on 6 channels
20b	AudioPinkNoiseOff	Audio Pinknoise Off	

The audio signal (sine or pink noise) will also be present on the digital ouput (SPDif). This can be checked by connecting an amplifier with digital input.
Check the I2S output.
LRCLK at testpoint F641

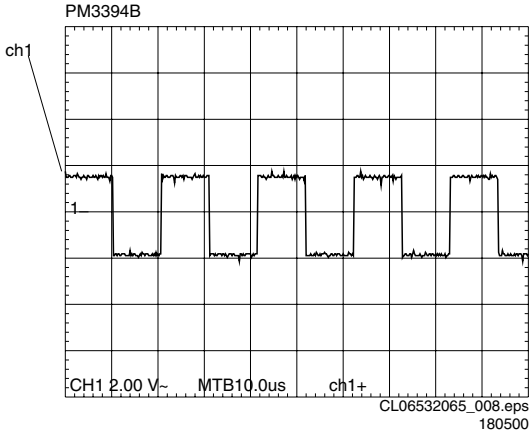


Figure 5-6

SCLK at testpoint F637

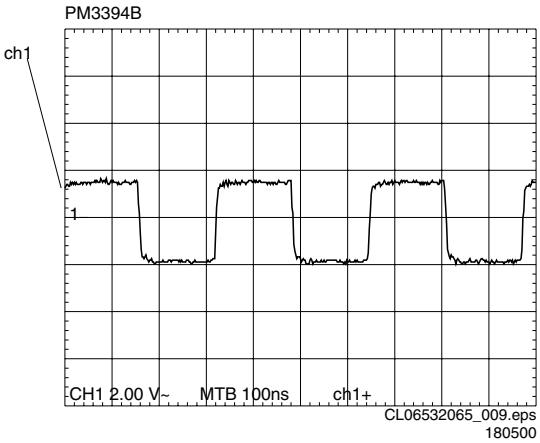


Figure 5-7

PCM_OUT0 at testpoint F638
PCM_OUT1 at testpoint F659
PCM_OUT2 at testpoint F658

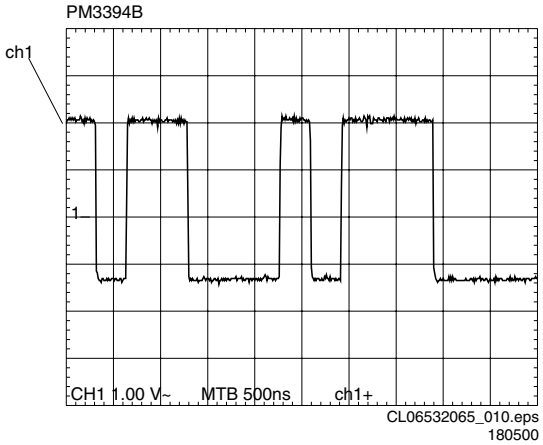


Figure 5-8

PCM_CLK at testpoint F640

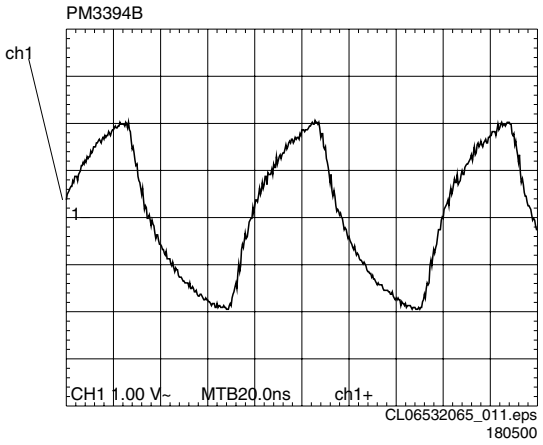


Figure 5-9

SPDIF at testpoint F644

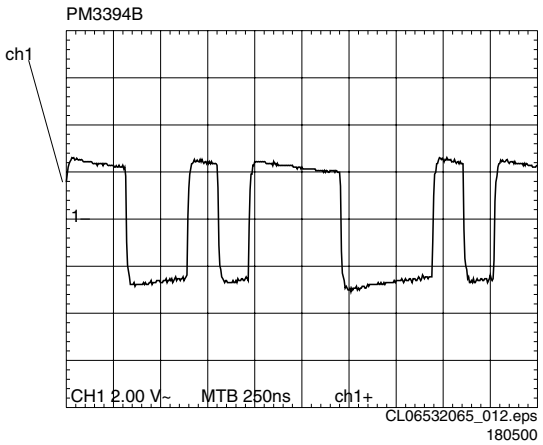


Figure 5-10

To switch the audio signal off, press the STOP button on the front.
Without A/V board all levels should be switching between low and high except:

– PCM_OUT1 and PCM_OUT2 only between low and high for pink noise. For sine, this is low.
– PCM_CLK and SPDIF switches between LOW and HIGH

Alternatively, there is a check that can be done without A/V board.
First, let the decoder generate pink noise on the audio outputs.

Ref. #	Command Name	Remark
20a	AudioPinkNoiseOn	Audio Pinknoise On

Measure then these signals on level and frequency.

Signal	Level between	Frequency
LRCLK	low/high	48kHz ± 0.02%
SCLK	low/high	3.072MHz ± 0.02%
PCM_CLK	LOW/HIGH	12.288 MHz ± 0.02%
PCM_OUT0, 1, 2	low/high	N/A
SPDIF	LOW/HIGH	N/A

Put the pink noise off:

Ref. #	Command Name	Remark
20b	AudioPinkNoiseOff	Audio Pinknoise Off

5.5 VIDEO

5.5.1 Video output check

Check DC output-level at all video-outputs at conn 1603-2,3,5,6 and conn 1604-16: -0.65V ± 10%
Generate a color-bar via next software commands:

Ref. #	Command Name	Remark
23a	VideoColDencOn	Colourbar DENC On
23b	VideoColDencOff	Colourbar DENC Off

Check video output at the next testpoints:
F646: R_VID

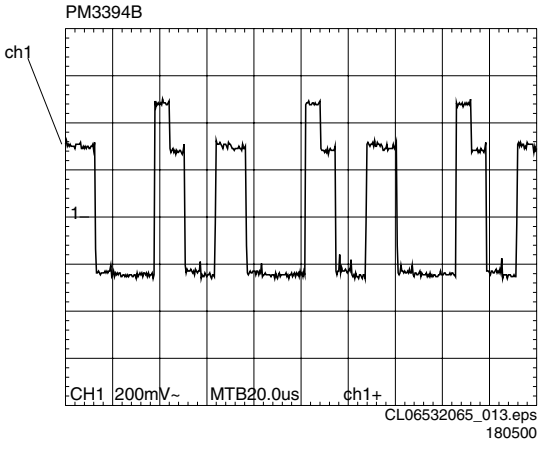


Figure 5-11

F649: G_VID

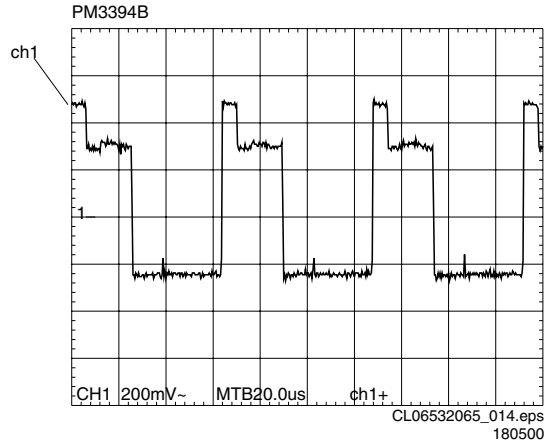


Figure 5-12

F653: B_VID

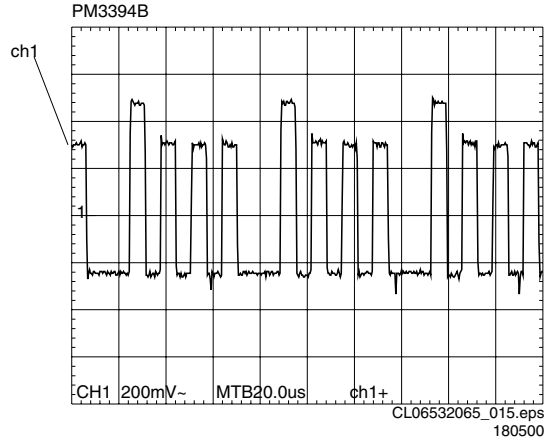


Figure 5-13

F657: CVBS

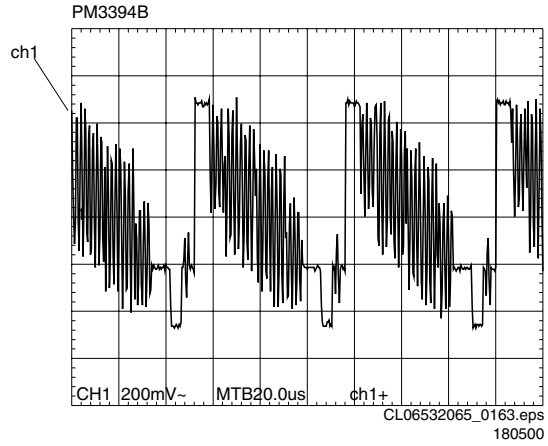


Figure 5-14

F665: C_VID

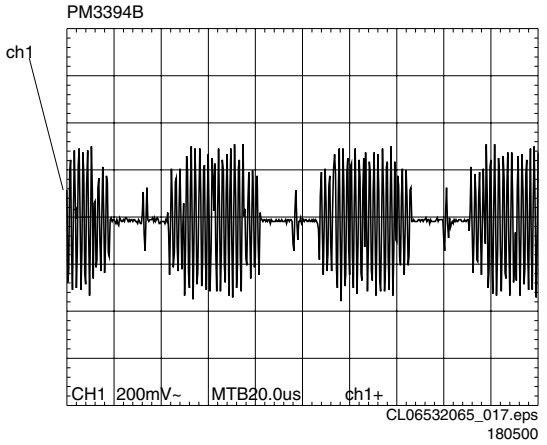


Figure 5-15

F666: Y_VID

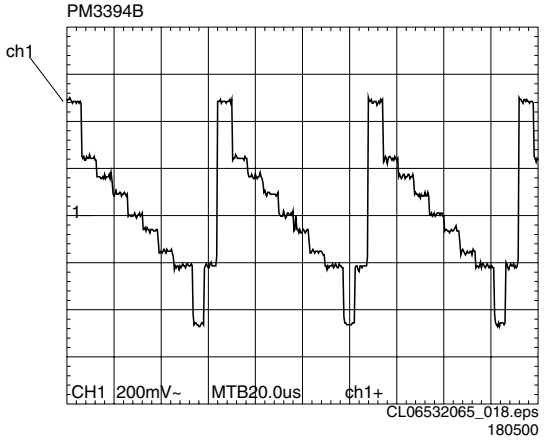


Figure 5-16

5.5.2 Scart-switching voltage

An aditional part of the video-path is the scart-switching voltage.
This voltage can be 0V, 6V, 12V.
Check at testpoint F620 the output-voltage while using next commands:

Ref. #	Command Name	Remark
25a	VideoScartLo	Sends out 0V ± 0.5V
25b	VideoScartMi	Sends out 6V ± 10%
25c	VideoScartHi	Sends out 12V ± 10%

5.5.3 Video Hsync check.

To measure the correctness of this output, F656 should be checked.

Ref. #	Command Name	Remark	Value
23a	VideoColDencOn	Colourbar	DENC on15.625 kHz ± 0.02% Vpeak-peak > 3V
23b	VideoColDencOff	Colourbar	DENC off No measurements needed

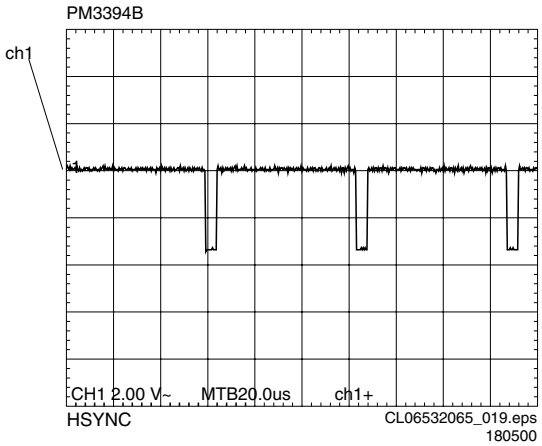


Figure 5-17

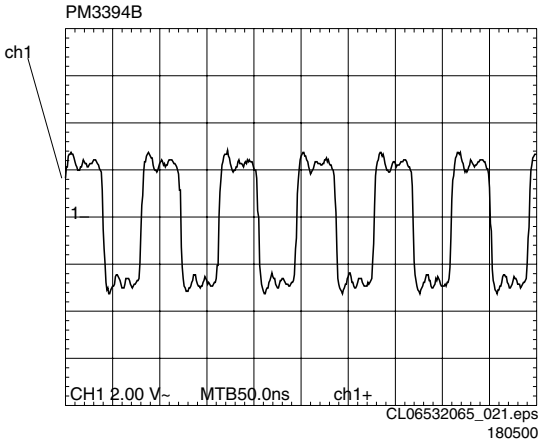


Figure 5-19

5.6 Servo

5.6.1 General start-up measurements:

Reset the Basic Engine part

Ref. #	Command Name	Remark
44	BeReset	Basic Engin

Check Vref

Name	Testpoint	Value
Vref	F188	2.5V+/-0.3

Check I2S interface

Name	Testpoint	Value
B_BCLK	F347	6.0MHz +/-0.1

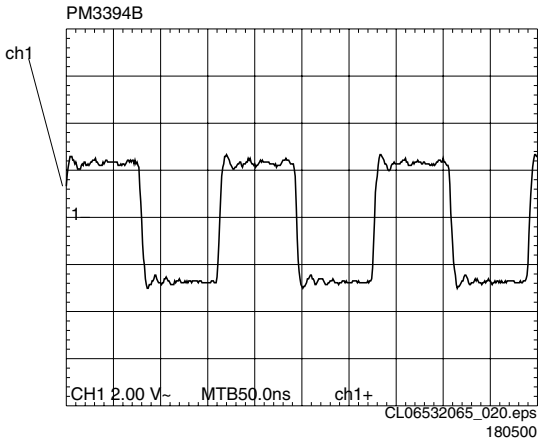


Figure 5-18

CL1F33712.0MHz +/-0.2

B_WCLKF343HIGH
StopclkF338HIGH
B_SyncF344HIGH
B_V4F348HIGH

5.6.2 Spindle Motor:

Before switching on the discmotor, check the following testpoints:

Name	Testpoint	Value
Stby	F357	high
Stby-out	F355	LOW
Moto1	F361	3V±0.3

Switch the Discmotor on/off with next commands:

Ref. #	Command Name	Remark
39a	BeDiscmotorOn	Discmotor on
39b	BeDiscmotorOff	Discmotor off

Check the following signals when discmotor has been switched on::

Name	Pin nr.	Frequency
Stby	F357	low
Stby-out	F355	HIGH
Moto1	F361	3V±0.5V
A3	F350	see oscillogram
A2	F352	see oscillogram
A1	F353	see oscillogram

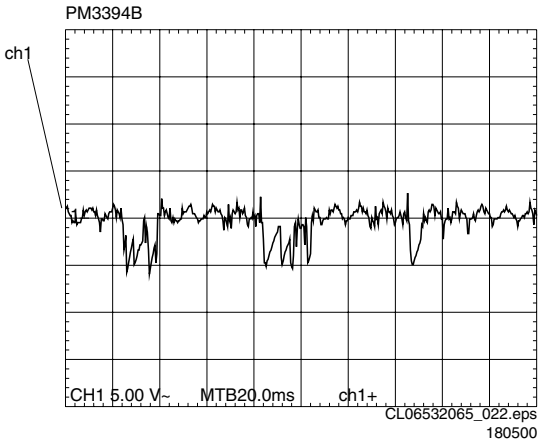


Figure 5-20

T1	F280	see oscillogram
T2	F368	see oscillogram
T3	F371	see oscillogram

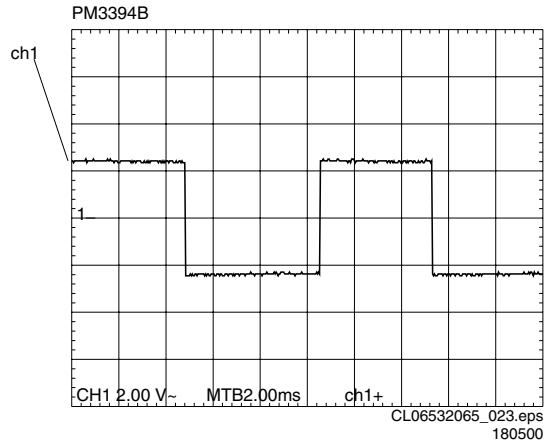


Figure 5-21

VH	F365	3V±0.5V
H1+	F354	see oscillogram
H1-	F359	see oscillogram
H2+	F364	see oscillogram
H2-	F366	see oscillogram
H3+	F367	see oscillogram
H3-	F370	see oscillogram

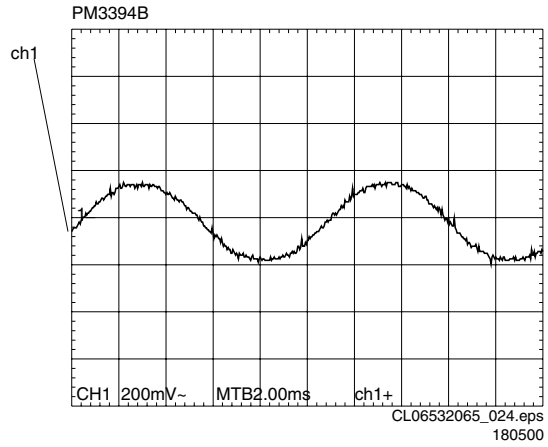


Figure 5-22

Switch the discmotor off.

5.6.3 Radial

Swith the radial control on/off with the following commands:

Ref. #	Command Name	Remark
40a	BeRadialOn	Radial control on
40b	BeRadialOff	Radial control off

Check the following signals:

Name	Testpoint	Value
Rad -	F128	4.3V±0.5V
Rad +	F121	4.3V±0.5V

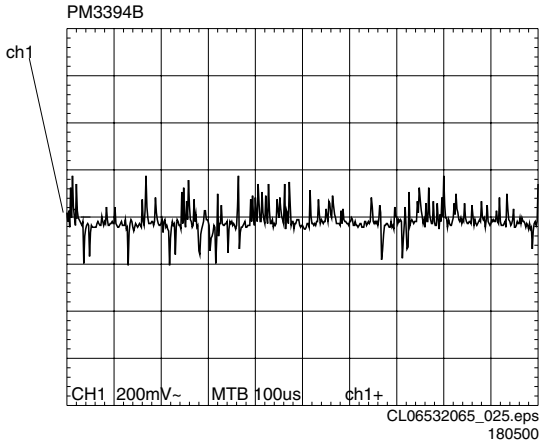


Figure 5-23

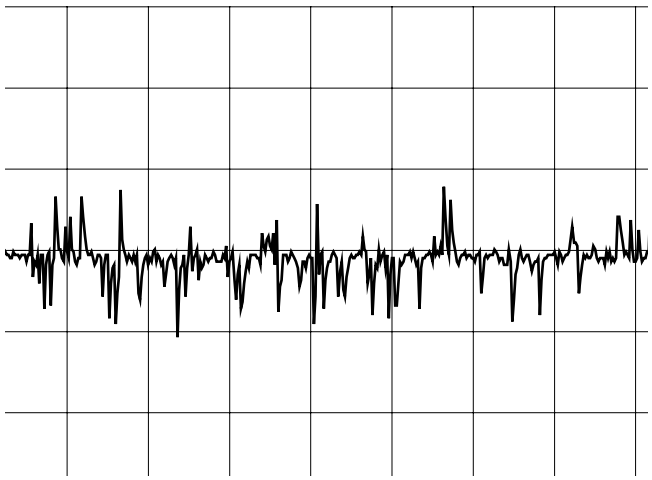


Figure 5-24

Check for pulse density signal RA at testpoint F227

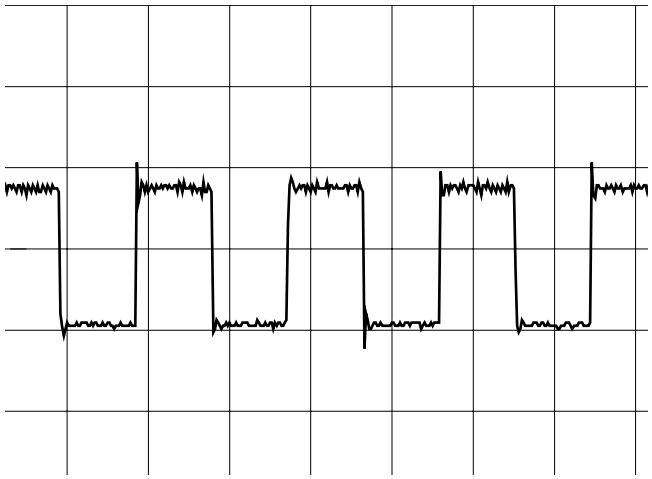


Figure 5-25

Check if laser is switched on (visual check of laserlight).
Switch the radial control off.

5.6.4 Sledge

Use the following commands to move the sledge:

Ref. #	Command Name	Remark
41a	BeSledgeIn	Sledge inwards
41b	BeSledgeOut	Sledge outwards

Check pulse density signal SL at testpoint F221

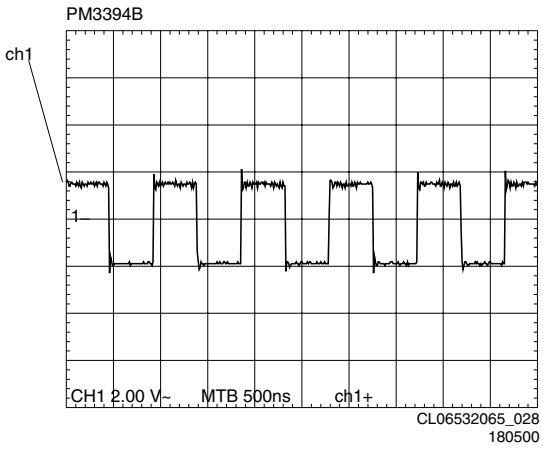


Figure 5-26

Name	Testpoint	Value
Sl -	F012	4.5V±0.5V
Sl +	F011	4.5V±0.5V

Measure peak to peak signal on SL- and SL+ while moving sledge outwards.

Name	Testpoint	Value
Sl -	F012	10Vptp +/-0.5
Sl +	F011	10Vptp +/-0.5

Measure input sledge control (sledge in home position)

Name	Testpoint	Value
Sinph	F182	2.2V±0.5V
Cosph	F192	2.2V±0.5V

5.6.5 Tray:

To open and close the tray use the following commands:

Ref. #	Command Name	Remark
43a	BeTrayIn	Tray in
43b	BeTrayOut	Tray out

Measure the driver outputs of the BA5938FM for the tray closed.

Name	Testpoint	Value
Vo2 -	F116	4.3V±2.0V
Vo2 +	F111	4.3V±2.0V

Measure again the driver outputs while the tray is opening.

Name	Testpoint	Value
Vo2 -	F116	2.0V±1.0V
Vo2 +	F111	6.0V±1.0V

5.6.6 Focus

To switch the Focus motor on/off, use the following commands:

Ref. #	Command Name	Remark
38a	BeFocusOn	Focus on
38b	BefocusOff	Focus off

Measure the driver outputs of the BA5938FM for the Focus off.

Name	Testpoint	Value
foc -	F124	4.3V±0.5V
foc +	F127	4.3V±0.5V

Switch the focus on
Measure again the driver outputs

Name	Testpoint	Value
Foc - (sawtooth)	F124	1V±0.2V
Foc + (sawtooth)	F127	1V±0.2V

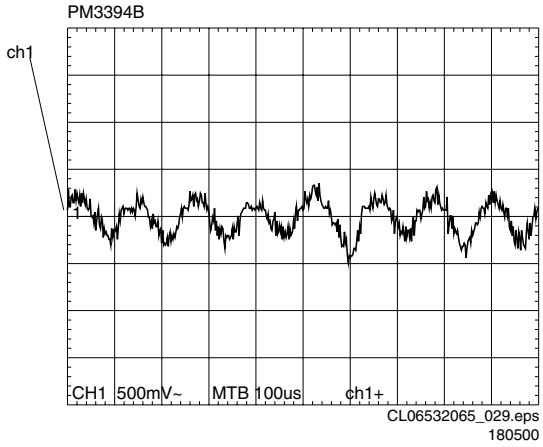


Figure 5-27

Check for pulse density signal FO at testpoint F234

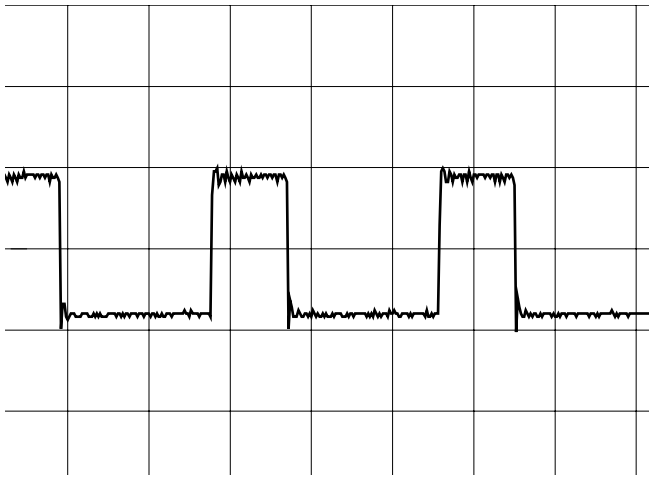


Figure 5-28

Check for laserlight.
Switch the focus off

5.6.7 Hf path

Play DVD test disc.
Measure outputs of diodes A, B, C, D, E, F.

Name	Testpoint	Value
A	F140	2.6V±0.2V
B	F141	2.6V±0.2V
C	F143	2.6V±0.2V
D	F144	2.6V±0.2V
E	F147	2.6V±0.2V
F	F148	2.6V±0.2V

At outputs of diodes A, B, C, D the following oscillogram can be measured:

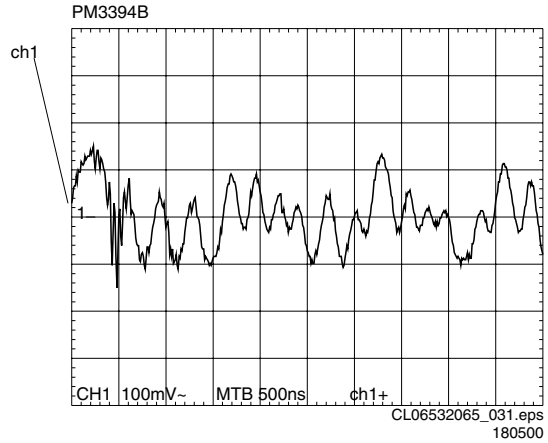


Figure 5-29 cl06532065-031

Measure DVDALAS outputs

Name	Testpoint	Value
RFO DC	F146	2.5V ±0.2V
O1	F156	25mV±10mV
O2	F159	25mV±10mV
O3	F169	25mV±10mV
O4	F166	25mV±10mV
S1	F174	25mV±10mV
S2	F175	25mV±10Mv

At output RFO, the following oscillogram can be measured:

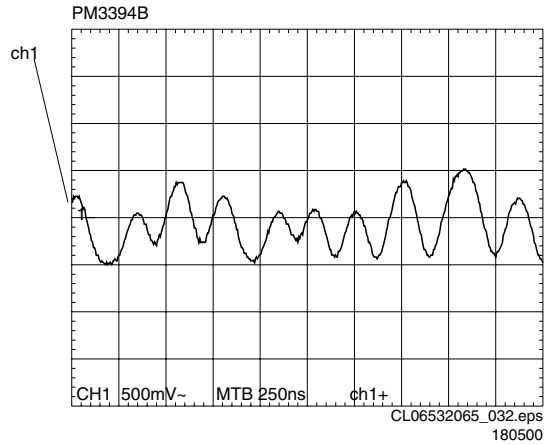


Figure 5-30

5.7 Diagnostic software description Introduction

5.7.1 Introduction

Purpose

This document describes all interfaces from the outside world to the diagnostic software, what is needed to use these interfaces and how to access them.
Changes for DVDv2b are marked.

Scope

This document has been realised within the framework of the product development of the second generation DVD video player. This player forms the basis for future DVD developments as described in the DVDv2 Overall Project Management Plan.

5.7.2 Definitions and abbreviations

Definitions

Control PC	Automatic test equipment, part of the production control system in the factory, to control the execution of Diagnostic Nuclei in the DVD player.
Diagnostic Nucleus	Part of the Diagnostic Software. Each nucleus contains an atomic and software independent diagnostic test, testing a functional part of the DVD player hardware on component level.
Script	Part of the Diagnostic Software. Each script contains a sequence of Diagnostic Nuclei to be executed.
Service PC	PC used by a service- or repair-person to communicate with the Diagnostic Software in the DVD player.

Abbreviations

FDS	Full Diagnostic Software

5.8 Overview of Interfaces

The table below shows an overview of the user interfaces of the Diagnostic Software. The table is based on logical interface, interfaces as seen from user perspective. A logical interface can use one or more physical interface components. The DVD has only a single RS232 port, implying that all interfaces using this port are mutually exclusive.

Logical Interface	Description	Physical interface components
Menu Interface	Menu-driven activation of individual nuclei, used for Level 2/ Second Line diagnostic mode. Users are service or repair people	Service PC running a terminal emulation program, connected to the RS232 port of the DVD player Test pin
Command Line Interface	Used during Level 1 diagnostic mode. Used to send commands from the Control PC into the DVD hardware.	Control PC, running a control program (e.g. Asterix), connected to RS232 port of the DVD player Test pin
Script Interface	Used to execute Player Test Script (including reading the error log) and Dealer Test Script.	Local keyboard Local display
S2B interface	Used for S2B communication with the Basic Engine	Service PC, running a S2B monitor program, connected to the RS232 port of DVD player Test pin
Download Interface	Used to download diagnostic software into the DVD player	Service PC running a terminal emulation program, connected to the RS232 port of the DVD player Test pin

In the next chapters the logical user interfaces are described in more detail including the exact use of the physical interface components.

5.9 Description Of Interfaces

5.9.1 Menu Interface

The menu interface is part of the Level 2 / Second Line diagnostic mode. Via the menu interface it is possible to control the execution of the Diagnostic Nuclei.

Set-up physical interface components
Hardware required:
- Service PC
- one free COM port on the Service PC
- special cable to connect DVD player to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD player. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

5.9.2 Code nr. PC interface cable: 3122 785 90017

Activation
Switch the player on and the following text will appear on the screen of the terminal (program):

```
DVDv2 Diagnostic Software version 1.0


SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK


(M)enu, (C)ommand (S)2B-interface or (D)ownload? [M]:@M <-
<main menu>
Select>
```

CL06532065-033.eps
180500

The first line indicates that the Diagnostic software has been activated and contains the version number of the diagnostic; this is also an indication that the first basic nucleus (nucleus number 1) has been executed succesfully. The next three lines are the succesful result of the subsequent basic tests (nuclei 2, 3, 4 and initialisation of Karaoke chip respectively). If not all these messages appear on the terminal screen, then the related nucleus found an error. The last line is the prompt asking to choose for an interface form. If a choice for Menu Interface has been made, the main menu will appear. For the layout of the menus, see page 25.
To switch between interfaces, the DVD player needs to be switched off and on again.
Note1 : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.
Note2 : The Dram tests are no longer executed because the player has no DRAM .
Note3 : When the stack is located in the internal memory, the test with the SRAM doesn't work and will be left out.
Note4 : The karaoke initialisation will also take place if there is no karaoke-chip in the player.

Usage
A selection can be given by the user by typing the number of the menu-item chosen at the prompt. Each entry must be terminated with a . Invalid selections will cause an error message by the Menu Handler. Example:

```
Select > 60
0001 Invalid menu selection ER @
Press RETURN to continue…@
```

CL96532111_021.eps
071099

Result and output of an activated (and terminated) nucleus will be sent back to the service terminal. Example:

```
Select > 16
1601 Data line X is not connected to the SDRAM ER @
Press RETURN to continue…@
```

CL96532111_022.eps
071099

After the user presses a key, the current menu is rebuilt on screen.
Pressing < return > at the prompt without any further input at the terminal will always rebuild the main menu.

Termination
The menu interface is terminated by switching off the DVD player.

5.9.3 Command Line Interface

The command line interface is part of level 1 diagnostic mode. Via a command line interface the execution of Diagnostic Nuclei can be controlled.

Set-up physical interface components
Hardware required:
- Control PC
- one free COM port on the Control PC
- special cable to connect DVD player to the Control PC

The control PC must use the following port settings for the used COM port: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The control PC is connected with a special cable to the RS232 port of the DVD player. Via the same connection the test pin will be connected to ground.

Activation
After power on the next text will sent to the control PC

```
DVDv2 Diagnostic Software version 1.0
SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK

(M)enu, (C)ommand (S)2B-interface or (D)ownload? [M]:@ C <-
DD>
```

CL06532065_034.eps
180500

The first line indicates that the Diagnostic software has been activated and contains the version number; this is also an indication that the first basic nucleus (nucleus number 1) has been executed succesfully. The next three lines are the succesful result of two subsequent basic tests (nuclei 2, 3, 4and karaoke initialisation respectively). If not all these messages appear on the terminal screen, then the related nucleus found an error. The fifth line lets the user choose between the two possible interface forms. The last line is the prompt ("DD>"). The diagnostic software is now ready to receive commands.
Note1 : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.
Note2 : When it is a player without DRAM, the DRAM tests are left out.

Usage
The commands that can be given are the names or the numbers of the nuclei. A command must be terminated with a < return > character from the control PC. When typing commands, the backspace key can be used to make corrections.
In case of typing errors in the command, an error message is returned. Example:

```
DD >CompSdarmWrR
0001 Unknown command ER @
DD>
```

CL96532111_024.eps
071099

If the command (the nucleus name or number) is recognised, the nucleus is executed. Result and output of an activated (and terminated) nucleus will be sent back to the control PC according to the standard layout as defined in Appendix C.

Example in case the command is correct:

```
DD >CompSdarmWrR
1600 OK @
DD>
```

CL96532111_025.eps
071099

Example in case the result is an error:

```
DD >CompSdarmWrR
1601 Address line X not connected to the SDRAM @
DD>
```

CL96532111_026.eps
071099

Termination
The command line interface is terminated by switching off the DVD player.

5.9.4 S2B Interface (not for service)

Set-up physical interface components
Hardware needed:
- Control PC
- one free COM port on the Control PC
- special cable to connect DVD player to Control PC
- S2B monitor tool running on the Control PC

Activation
To start the S2B interface, connect the RS232 cable to the Control PC in the correct manner. Then start the PC, start the monitor tool and start the DVD player; turn off the monitor tool, turn on S2B monitor tool. The S2B monitor tool now takes all communication.
The S2B interface is activated by sending the bit pattern 110x xxxx with the first character to the DVD player, when the user is asked to choose an interface type. The command handler will then activate the S2B pass-through nucleus. The character sent will be passed to this nucleus without loss.
Note: The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.

Termination
To terminate S2B pass-through mode, switch off the DVD player.

5.10 Script Interfaces

This interface is used during execution of the Player Script and the Dealer Script to display output and error messages.
The local display will be used to display the output and the error messages.

5.10.1 Dealer Script

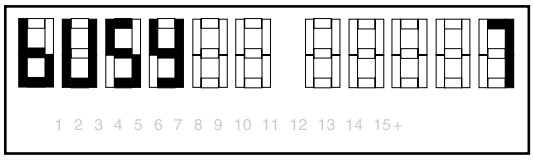
Set-up physical interface components
Hardware required:
- DVD player

The DVD player is tested stand-alone: no other equipment than the DVD player is needed.

Activation
The dealer script is activated by pressing OPEN/CLOSE and PAUSE on the local keyboard of the DVD player simultaneously during power-on.

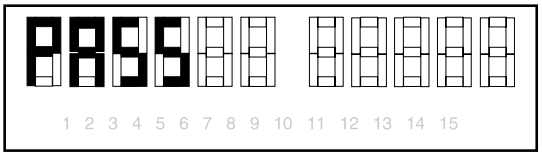
Note : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.

Usage
The test requires no user interaction. A number of nuclei will be run before a message is returned indicating if there is a failure in the DVD player.
During the execution of a script, a progress indicator is displayed on the local display of the DVD player.

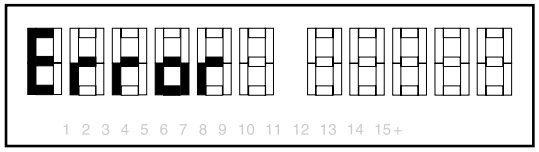


CL96532111_017.eps
071099

The counter at the right side of the display counts down from the number of nuclei to be run to zero. At zero all nuclei from the script have been run and the result (PASS/Error) is displayed on the local display of the DVD player.
When the dealer script has been completed, the results are displayed in the following manner:



CL96532111_018.eps
071099



CL96532111_019.eps
071099

Termination
To turn off the dealer test, the DVD player must be powered down.

5.10.2 Player Script

Set-up physical interface components
Hardware needed:
- DVD player
- television set, connected to the DVD player
- 6 audio speakers
- an external video source

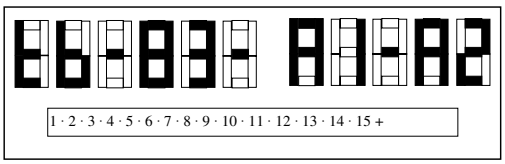
Activation
To activate the player script, press OPEN, CLOSE and STOP keys on the local keyboard of the DVD player simultaneously during power-on.

Usage
The player test requires human interaction to decide whether nuclei give correct output, e.g. the user needs to confirm the results of the display test. This needs to be given through the local keyboard on the DVD player. Which keys can be used for this purpose is described with each test.
Module test (with user interaction)
During the first phase of the dealer test, the three main modules (Digital PWB, Display PWB and Basic Engine) are tested; some interaction from the user is required.
1. Testing the Display PWB
This involves testing the local display and keyboard, but also testing the remote control and the leds.

The Display Test
During the display test, different patterns will be shown on the local display of the DVD player. The user needs to step through these patterns using the PLAY key on the local keyboard. If any of the displayed patterns is incorrect, the display test has failed, and also the player test has failed.
The test patterns on display will be repeated in a loop (stepped through using PLAY) until the user presses NEXT on the local keyboard to proceed to the next test.

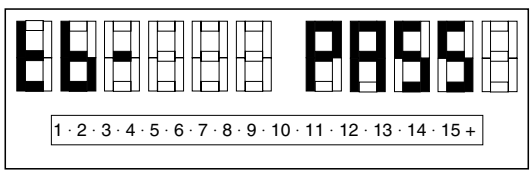
The LED Test
Next is the LED test; the LEDs on the DVD player are lit. Pressing PLAY will indicate that all LEDs are operational. To indicate that a LED did not light up, the user must press the PAUSE key. Pressing PLAY or PAUSE will proceed the user into the next test.

The Keyboard Test
During the keyboard test, the user needs to press all the keys on the local keyboard one by one. On the local display each key is represented by its scancode (a hexadecimal 2-digit code identifying the key to the DVD player).
Pressing a key will show its representing code on the local display of the DVD player: the first hexadecimal digit identifies the key pressed, the second indicates how many times this particular key was detected. In case the key is pressed more than once, the scancode is displayed as many times, with the second digit of its code increased each time. The display of scancodes scrolls from right to left, with the most recent scancode at the right. The following example gives a possible layout of the local display during the display/remote control test:



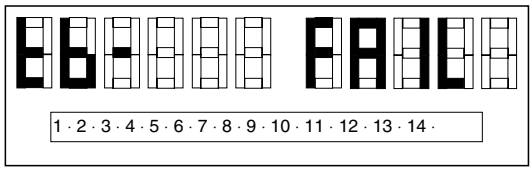
CL 96532097_004.eps
130999

To terminate the keyboard test, press the NEXT key on the local keyboard of the DVD player and keep it pressed for 1 (one) full second. The keyboard test will terminate with a message on the local display. In case the keyboard test was successful, the message is:



CL 96532097_007.eps
130999

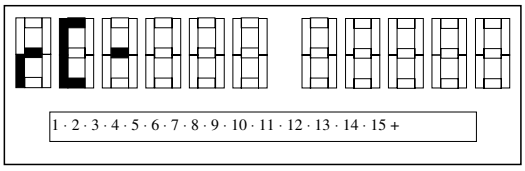
In case the keyboard test was not successful, the message will be:



CL 96532097_008.eps
130999

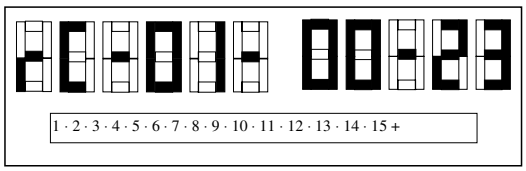
If the "tbFAIL"-message is displayed, the player test has failed. This is the end of the player test: turn off the DVD player, or press NEXT on the local keyboard of the DVD player to proceed to the next test.

The remote control test
For the remote control test, the user must press a key (any key) on the DVD's remote control. The display at the start of the test looks as follows:



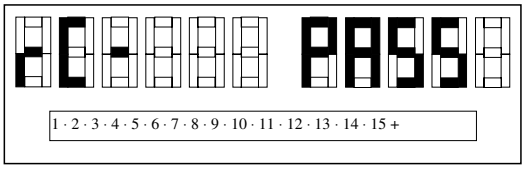
CL 96532111_032.eps
071099

When a remote control code has been received, its scancode is displayed as follows:



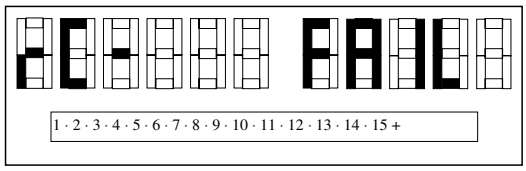
CL 96532097_009.eps
130999

The NEXT key can be pressed to exit this test.
However, if the user requires to test all keys on the remote control, (s)he can continue to press keys and these will all be displayed on the local display. With a code-table at hand this test can be used to test the full functionality of the DVD's remote control.
When the user has pressed NEXT on the local keyboard (NOT on the remote control!), the result of the remote control test is shown on the local display as follows:



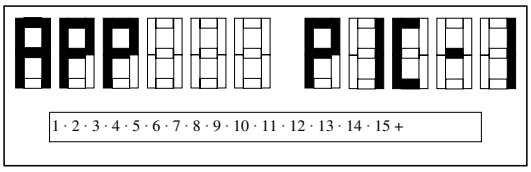
CL 96532097_011.eps
130999

in case of succes;



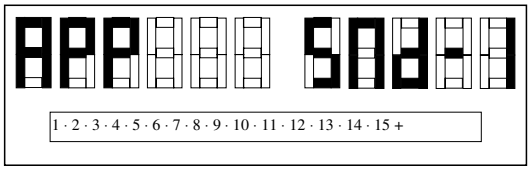
CL 96532097_012.eps
130999

if the test fails.
Pressing NEXT on the local keyboard again will proceed to the next test.
2. Testing the Monoboard
The picture tests involve putting a predefined picture on the connected television set, and asking the user for confirmation. When the picture has been put on screen, the local display asks for confirmation by the user as follows:



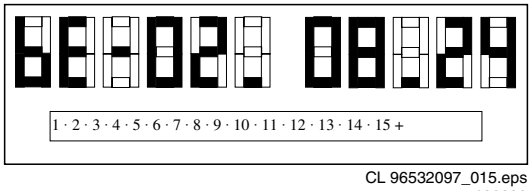
CL 96532097_013.eps
130999

If the user presses PLAY, he confirms the test; pressing PAUSE will indicate a fault in the test. At this time, the player test had failed and the DVD player can be switched off, or the user can proceed to the next test by pressing NEXT on the local keyboard of the DVD player.
Pressing the NEXT key on the local keyboard will start the next picture test (Colour set-up functional test).
When the picture tests are finished, the sound tests are run. A predefined sound will be generated, and again the user is asked to confirm this. The local display looks as follows:



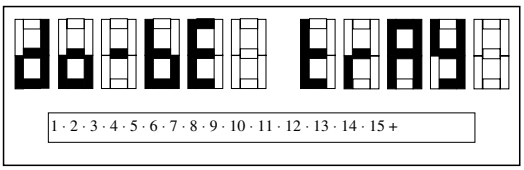
CL 96532097_014.eps
130999

Pressing PLAY confirms the test, PAUSE indicates test failure. If the test is faulty, the player test failed and the DVD player can be shut off. Subsequent sound tests will be numbered in ascending order.
Pressing NEXT on the local keyboard of the DVD player will take the user into the next test.
3. Testing the Basic Engine
Most tests on the basic engine require user interaction.
When the basic engine tests are started, the version of the basic engine which is present in the DVD player is shown on the local display, as follows:



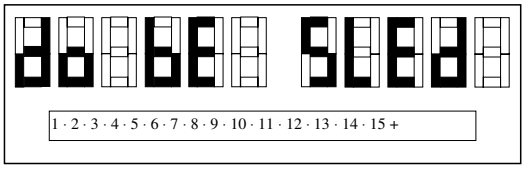
CL 96532097_015.eps
130999

The version number is displayed in decimal representation (the underscore replacing the dot). When the user presses NEXT on the local keyboard, the tests on the basic engine are started. First, the tray operation is tested. The user can move the tray in and out by pressing the PLAY or PAUSE key on the local keyboard (both keys have essentially the same function). The results need to be checked visually by the user, the software cannot detect any faults. The local display looks as follows:



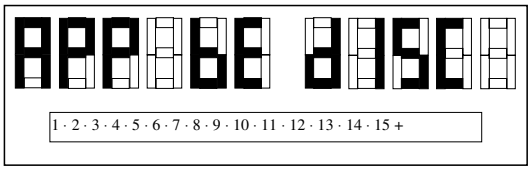
CL 96532097_016.eps
130999

To indicate this is a test of which the result is to be checked by the user, the first word on the local display is "do".
Except for testing the tray, this test is also meant to give the user the opportunity to put a disc into the DVD player for subsequent basic engine tests. Some of the following tests need a disc in the DVD player to operate properly. Always put a disc into the DVD player during this test! At the end of the basic engine tests there is opportunity to remove it (before the looptests start). Pressing the NEXT key on the local keyboard proceeds to the next test.
Second test is the sledge test; the user is asked to move the sledge by using the keys PLAY and PAUSE on the local keyboard (both keys have essentially the same function). This test needs to be checked visually by the user; the software cannot detect any faults. The local display during this test looks as follows:



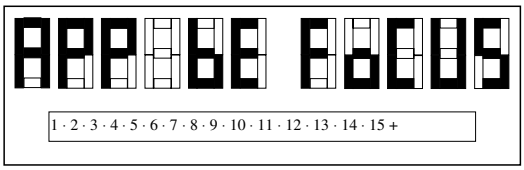
CL96532097_017.eps
130999

After pressing NEXT on the local keyboard the discmotor is tested; the local display looks as follows:



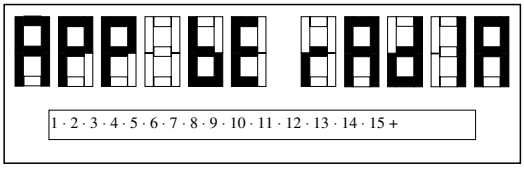
CL 96532097_018.eps
130999

The user is required to listen if the disc motor is running; this must be confirmed by pressing PLAY on the local keyboard. The PAUSE key is used to indicate the discmotor does not run. Pressing NEXT on the local keyboard starts the focus test. The local display looks as follows during this test:



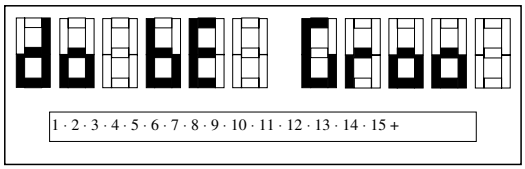
CL 96532097_019.eps
130999

By pressing PLAY the user confirms successful focussing by the basic engine; pressing PAUSE indicates a fault in the focus function.
Pressing NEXT on the local keyboard starts the radial function; the local display looks as follows:



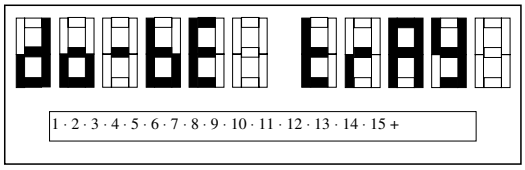
CL 96532097_020.eps
130999

Again, PLAY confirms the result, PAUSE indicates an error. After pressing NEXT on the local keyboard, the grooves/jump test is started. As this is also a test that cannot be checked by the software, the user needs to perform a visual test. The local display looks as follows:



CL 96532097_021.eps
130999

By pressing PLAY the next grooves/jump position is taken; pressing PAUSE will go to the previous grooves/jump position. Switching through the different positions is done in a cyclic manner.
Press the NEXT key on the local keyboard to proceed to the last basic engine test: again, the tray is tested. This has been done at the beginning of the basic engine test already, the repeat is only meant to enable the user to remove the disc in the tray before proceeding. The local display will look as follows:

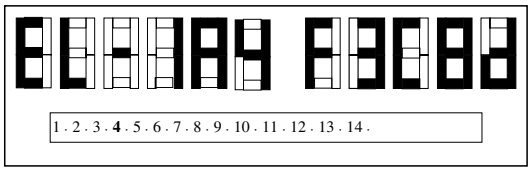


CL 96532097_016.eps
130999

Press PLAY or PAUSE to operate the tray; remove the disc in the tray.
The tray will be closed automatically (if needed) before proceeding to the next tests (by pressing NEXT on the local keyboard).
Read Error Log

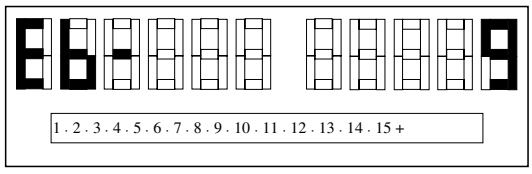
The contents of the error log will be displayed on the local display, as follows :

Note: This is an example only; no actual errorcode is intended



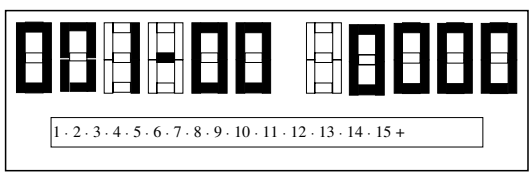
CL 96532097_022.eps
130999

The first two characters on the local display ("EL") indicate that the read-out mode of the error log is activated. After the hyphen 8 hexadecimal digits (one faultcode) are displayed. Below the row of 7-segment displays the highlighted number indicates the number of the faultcode being displayed. (Not for DVDv2B) The highest number indicates the oldest faultcode.
If, in the future, more than 15 faultcodes need to be displayed, the "+" character can be used to indicate the display of a faultcode in the range 16 - 30.
To step through the different fault codes, the PLAY (next) and PAUSE (previous) key on the local keyboard can be used. The display of faultcodes is cyclic. If the error log does not contain any fault codes, all displayed error codes will be "000 00000".
To switch off the display of the error log, the NEXT key must be pressed on the local keyboard.
Read Error Bits
The error bits are used to indicate that an error occurred once or more times; if that is the case the bit representing the error is set. To read out this field of error bits, the local display is used. Only the numbers of the errors where the bit is set will be displayed on the local display. The layout of the local display is (globally) as follows2:



CL 96532097_023.eps
130999

The number of the set bits is displayed in a cyclic manner. Scrolling through the set error bits can be done with the PLAY key for 'next' and PAUSE key for 'previous'. Pressing the PLAY key at the last bit number will display the first bit number again, pressing the PAUSE button at the first bit number will display the last bit number in the list. The representation of bit numbers is decimal.
If no error bits are set, the number on the right side of the display will be "00"
Module Looptest
The module looptest is an infinite loop in which a number of nuclei are executed over and over again. The nuclei run are the same as in the dealer test; user interaction is not required.
During this looptest, the display looks as follows3:



CL 96532097_025.eps
130999

The leftmost three digits indicate which of the DVD player's modules is faulty; the explanation is in the following table:

Displayed Value	Indication for each module		
	Loader	Mono-board	Display PCB
000	ok	ok	ok
001	ok	ok	faulty
010	ok	faulty	ok
011	ok	faulty	faulty
100	faulty	ok	ok
101	faulty	ok	faulty
110	faulty	faulty	ok
111	faulty	faulty	faulty

CL 06532065_052.eps
230500

After the hyphen the (decimal) number indicates the number of times the looptest was performed.
The right side of the display shows an error code DNER (in decimal representation), which is built from a nucleus number (DN) and an error number (ER). This code indicates the last nucleus that returned an error code. For explanation of this DNER code, see document [SDD_DN].
Pressing NEXT on the local keyboard of the DVD player will exit this loop and show the end result of the player test.
End result of the player test is equal to the last display shown above: it shows which module is faulty and which nucleus caused the last error, as well as how many loops were performed.

Termination
To terminate the player test, switch off the DVD player.

5.11 Download Interfaces (not for service)

The download interface enables the user to download another version of diagnostic software into the RAM of the DVD player. The downloaded software will overrule the software which is placed in the DVD player's ROM; running the original diagnostic software is disabled until the DVD player is switched off and on again.
For download of diagnostic software, the RS232 port may be used.

5.11.1 Set-up physical interface components

Hardware required:
- Service PC
- one free COM port on the Service PC
- special cable to connect DVD player to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm in Windows95) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control.
The free COM port must be connected via a special cable to the RS232 port of the DVD player. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

5.11.2 Activation

Switch the DVD player on and the following text will appear on the screen of the terminal (emulation program):

```
DVDv2 Diagnostic Software version 1.0
SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK

(M)enu, (C)ommand (S)2B-interface or (D)ownload? [M]:@ D <-
DVD diagnostic software awaiting download...@
```

CL06532065_035.eps
180500

The DVD player is now in a wait-mode, awaiting the download of a file in Motorola S3-format.
Enter the download command (which will be an "upload" from the terminal!) at the terminal:

```
upload <file>
```

CL96532111_028.eps
071099

Progress seen by the diagnostic software is indicated by displaying the character "*" on screen repeatedly; if the download software encounters an error, the end of the downloaded file will be awaited and instead of the "*"-character, the "+"- character will be used to indicate (erroneous) progress.
When download is finished, the following message will come from the DVD player:

```
Download succesful
Press return to start downloaded program...
```

CL96532111_029.eps
071099

When the user then presses a key, the DVD player will report

```
DVD Diagnostic Software version X.X
```

CL96532111_030.eps
071099

and start to run the downloaded software.
Note1 : The DVDv2B player has no power-ON key, but should be turned on by connecting the power-cable.
Note2 : For players without DRAM, the DRAM-tests will be scipped.

5.11.3 Usage

The usage of the downloaded software depends on the contents of that software and cannot be described here.

5.11.4 Termination (not for service)

To exit the download-interface and remove the downloaded software from the DVD player, switch off the DVD player.

External Scripts
A script is a sequence of nucleus calls. Internal scripts (e.g. scripts built into the diagnostic software itself) are in the form of a C-language module. However it cannot be expected from a customer to write C-modules in order to create new scripts.

The scripts that can be made externally are therefor in one of the following two forms:

1. A Procomm or Telex script Procomm or Telex can be used to write diagnostic scripts. The script language of both communication packages contains possibilities for construction of loops and branches in the scripts. Commands then going over the line will be exactly the same as described in the chapter "Command Interface". The diagnostic software (the engine) will receive normal RS232 commands and processes these as defined, sending results of these nuclei back over the RS232 line. In the Terminal the Procomm or Telex script determines which command sequence is followed
2. An Asterix-script Asterix-scripts are C-programs in which commands are sent to the diagnostic software (the engine). The construction of branches and loops is again located in the remote machine, i.e. the Asterix machine. Commands going over the line will be exactly the same as described in the chapter "Command Interface". The diagnostic software (the engine) will receive normal RS232 commands and processes these as defined, sending results of the called nuclei back over the RS232 line. In the Asterix PC the C-program determines which command sequence is followed.

Layout of menus and submenus for the Service Terminal
NOTE: a symbol "-->" in the next menu layouts indicates that that specific menu choice will invoke the display of a submenu. This symbol will also be used in the implementation of the menus (i.e. the "-->" will also appear in the user interface).

Main Menu

MAIN MENU
1. Audio -->
2. Basic Engine -->
3. Display PWB -->
4. Processor & Peripherals -->
5. Karaoke -->
6. Log -->
7. Miscellaneous -->
8. Video -->

First Level Submenus

AUDIO MENU
1. Deemphasis -->
2. Mute -->
3. PinkNoise -->
4. SineWave -->

BASIC ENGINE MENU
1. Disc Motor -->
2. Focus -->
3. Grooves -->
4. Radial -->
5. Reset [44]
6. Sledge -->
7. Tray -->
8. Version [37]

DISPLAY PWB MENU
1. Display [30]
2. Keyboard [27]
3. LEDs [29]
4. Remote control [28]
5. Version [28]

LOG MENU
1. Read last errors [31]
2. Read error bits [32]

3. Reset [33]

PROCESSOR AND PERIPHERALS MENU
1. Clock -->
2. DRAM Write/Read [9]
3. Flash -->
4. I2C -->
5. S2B -->
6. SDRAM Write/Read [16]

MISCELLANEOUS MENU
1. NVRam Utils -->
2. PalNtsc Line --> (Not for DVDv2B)
3. 2B Utils -->
4. Statistics Info -->
5. Read Application Version [46]

VIDEO MENU
1. Colourbar -->
2. Scart -->

KARAOKE MENU
1. Karaoke Mode Off [48a]
2. Karaoke Mode On [48b]
3. KaraokeMicInput [49]
4. KaraokeKey On [50a]
5. KaraokeKey Off [50b]
6. Karaoke Echo On [51a]
7. Karaoke Echo Off [51b]

Second level submenus

DEEMPHASIS MENU
1. Deemphasis 0 On [18a]
2. Deemphasis 0 Off [18b]
3. Deemphasis 1 On [18c]
4. Deemphasis 1 Off [18d]

for DVDv2B:
1. Deemphasis On [18a]
2. Deemphasis Off [18b]
3. Deemp 0 Tristate On [18e]
4. Deemp 0 Tristate Off [18f]
5. Deemp 1 Tristate On [18g]
6. Deemp 1 Tristate Off [18h]

MUTE MENU
1. Mute On [19a]
2. Mute Off [19b]

PINKNOISE MENU
1. Pinknoise On [20a]
2. Pinknoise Off [20b]

SINEWAVE MENU
1. Audio Sine On [21a]
2. Audio Burst On [21b]

DISC MOTOR MENU
1. Disc Motor On [39a]
2. Disc Motor Off [39b]

FOCUS MENU
1. Focus On [38a]
2. Focus Off [38b]

GROOVES MENU
1. Jump Grooves to Inside [42a]
2. Jump Grooves to Middle [42b]
3. Jump Grooves to Outside [42c]

RADIAL MENU
1. Radial Control On [40a]
2. Radial Control Off [40b]

SLEDGE MENU
1. Sledge Inwards [41a]
2. Sledge Outwards [41b]

TRAY MENU
1. Open Tray [43b]
2. Close Tray [43a]

LASER MENU
1. Laser Cd On[58a]
2. Laser Cd Off[58b]
3. Laser DVD On[58c]
4. Laser DVD Off[58d]

UCLOCK MENU
1. µClock A_CLK in CDDA Mode [7a]
2. µClock A_CLK in DVD Mode [7b]

FLASH MENU
1. Checksum FLASH [6]
2. Flash write access [10]

I2C MENU
1. I2C NVRAM Access [11]
2. I2C Display PWB [12]

S2B MENU
1. S2B Echo [13]
2. S2B Pass-through [14]

NVRAM MENU
1. NVRAM Config [34]
2. NVRAM reset [35]
3. NVRAM Mod [36]
4. NVRAM write/read [15]

PAL/NTSC MENU (Not for DVDv2B)
1. PalNtscHi [45a]
2. PalNtscLo [45b]

2B UTILS MENU
1. I2C Scart Check [54]
2. Scart to DVD [55a]
3. Scart Pass through [55b]
4. VideoColSetupI2C [52]
5. VideoColSetupHi [53a]
6. VideoColSetupLo [53b]

VIDEO COLOURBAR MENU
1. Colourbar DENC On [23a]
2. Colourbar DENC Off [23b]

SCART MENU
1. Scart Low [25a]
2. Scart Medium [25b]
3. Scart High [25c]

STATISTICS INFO MENU
1. Total Nr of Times Tray Open [47a]
2. Toat Time Power On [47b]
3. Total Play-time CDDA & VCD [47c]
4. Total Play-time DVD [47d]

Screen layout with menus

When menus are used, no specific screen layout can be given: menu information will not be in a special format, except for the layout as mentioned in the previous paragraphs.
A typical menu session can look as follows:

```
----------< top of screen >----------
DVDv2 Diagnostic Software version 1.0
SDRAM Interconnection test passed
Basic SDRAM test passed
Karaoke init OK
(M)enu, (C)ommand, (S)2B-interface or (D)ownload? [M]:@
M <--
```

MAIN MENU

```
1. Audio -->
2. Basic Engine -->
3. Display PWB -->
4. Processor & Peripherals -->
5. Karaoke -->
6. Log -->
7. Miscellaneous -->
8. Video -->
Select> 4 <--
```

PROCESSOR AND PERIPHERALS MENU

```
1. Clock -->
2. DRAM Write/Read [9]
3. Flash -->
4. I2C -->
5. S2B -->
6. SDRAM Write/Read [16]
Select> 6 <--
----------< bottom of screen >----------
```

Depending on the height of the screen, the text will start scrolling off the top of the screen.

Layout of Results diagnostic nuclei on control/service PC

Results returned from a Diagnostic Nucleus to the control/ service PC will have a maximum length of 300 characters and are terminated by a CR character (included in the string length)
The result has the following layout
< number >< string > [OK I ER] @< CR >
The use of the "@" enables the Asterix system on the Control PC to parse the output string of each nucleus into a database.
< number > is a 4-digit decimal number padded with leading zeros if its value is less than 4 digits. The first two digits identify the generating nucleus (or goup of nuclei), the latter two digits indicate the error number.
< string > is a text string containing information about the result of the Diagnostic Nucleus.
< number > and < string > are defined in [SDD_DN] in the output sections of each Nucleus.
Examples:

```
1. 0001 Unknown command ER @
2. 3100 OK @
3. 0901 Data line X is not connected to the DRAM ER @
```

CL96532111_031.eps
071099

5.12 Diagnostic Nuclei

Each nucleus contains an atomic and independent diagnostic test, testing a functional part of the DVD player hardware on component level. Each Nucleus returns a result message to its caller. Some tests (e.g. generating a colour bar) can only return an "OK" result. Internal communication will be done via a uniform interface between the diagnostic Engine, Scripts and the Diagnostic Nuclei.
The diagnostic Engine can only operate if a certain (minimal) set of hardware is functioning properly. To test this set of hardware, a set of basic diagnostic nuclei is embedded in the DVD player. Each basic diagnostic nucleus will only test that part of the hardware which is required for execution of the diagnostic Engine, e.g. a RAM test will only test that part of RAM that is used by the diagnostic engine. After the Diagnostic Engine is operational it is possible to do a full RAM diagnostic. All basic diagnostic nuclei start with prefix 'Basic'.
In the overview each Diagnostic Nucleus consists of a reference number, a reference name and remarks. Reference number and name are coupled and one of them is enough for unique identification. The reference number can be used to find the description of the Diagnostic Nucleus in paragraph Error! Reference source not found..# where # is the reference number.

5.12.1 Basic Diagnostic Nuclei

Ref.	Reference Name	Remark
1	BasicSpAcc	Serial port Access test/ initialisation
2a	BasicInterconDram	Data and address bus Interconnection (only for DVDv2A)
2b	BasicInterconSdram	Data and address bus interconnection
3	BasicDramWrR	DRAM Write Read (only for DVDv2A)
4	BasicSdramWrR	SDRAM Write Read
5	BasicSramWrR	SRAM Write Read

5.12.2 Processor and Peripherals

Ref.	Reference Name	Remark
6	PapChksFl	Checksum FLASH
7a	PapUclkAclkCdda	uClock A_CLK in CD-DA mode
7b	PapUclkAclkDvd	uClock A_CLK in DVD mode
9	PapDramWrR	DRAM Write Read (only for DVDv2A)
10	PapFlashWrAcc	FLASH Write Access
11	PapI2cNvram	I2C NVRAM access
12	PapI2cDisp	I2C Display PWB
13	PapS2bEcho	S2B Echo
14	PapS2bPass	S2B Pass-through
15	PapNvramWrR	NVRAM Write Read

5.12.3 Components

Ref. #	Reference Name	Remark
16	CompSdramWrR	SDRAM Write Read

5.12.4 Audio

Ref.	Reference Name	Remark
17	AudioSig	Audio Signature (Optional)
18a	AudioDeemp0On	Audio De-emphasis 0 On
	AudioDeempOn (DVD2B)	Audio De-emphasis On (DVDv2B)
18b	AudioDeemp0Off	Audio De-emphasis 0 Off
	AudioDeempOff (DVD2B)	Audio De-emphasis Off (DVDv2B)
18c	AudioDeemp1On	Audio De-emphasis 1 On (Not for DVDv2B)
18d	AudioDeemp1Off	Audio De-emphasis 1 Off (Not for DVDv2B)
18e	AudioDeemp0TristateOn	Audio De-emphasis 0 in tristate/bidirectional mode (DVDv2B)
18f	AudioDeemp0TristateOff	Audio De-emphasis 0 back in output mode (Off) (DVDv2B)
18g	AudioDeemp1TristateOn	Audio De-emphasis 1 in tristate/bidirectional mode (DVDv2B)
18h	AudioDeemp1TristateOff	Audio De-emphasis 1 back in output mode (Off) (DVDv2B)
19a	AudioMuteOn	Audio Mute On
19b	AudioMuteOff	Audio Mute Off
20a	AudioPinkNoiseOn	Audio Pinknoise On
20b	AudioPinkNoiseOff	Audio Pinknoise Off
21a	AudioSineOn	Audio Sine signal On/Off
21b	AudioSineBurst	Audio Sine signal Burst
56a	AudioDeemp0On	PIO-pins as used in 2A for Deemphasis
56b	AudioDeemp0Off	PIO-pins as used in 2A for Deemphasis
56c	AudioDeemp1On	PIO-pins as used in 2A for Deemphasis
56d	AudioDeemp1Off	PIO-pins as used in 2A for Deemphasis

5.12.5 Video

Ref.	Reference Name	Remark
23a	VideoColDencOn	Colourbar DENC On
23b	VideoColDencOff	Colourbar DENC Off
25a	VideoScartLo	Scart Low
25b	VideoScartMi	Scart Medium
25c	VideoScartHi	Scart High
52	VideoColSetupCom	Colour Setup Communication
53a	VideoColSetupHi	Colour Setup High
53b	VideoColSetupLo	Colour Setup Low
54	VideoScartSwComm	Scart Switch communication
55a	VideoScartSwDvd	Scart Switch Dvd
55b	VideoScartSwPass	Scart Switch Pass-through

Ref.	Reference Name	Remark
57a	VideoScartPinLo	PIO-pins as used in 2A for Scart-switching
57b	VideoScartPinMi	PIO-pins as used in 2A for Scart-switching
57c	VideoScartPinHi	PIO-pins as used in 2A for Scart-switching

5.12.6 DisplayPWB (slave processor)

Ref.	Reference Name	Remark
26	DispVer	Version number
27	DispKeyb	Keyboard
28	DispRc	Remote Control
29	DispLed	LEDs
30	DispDisplay	Display

5.12.7 Log (error logging in NVRAM)

Ref.	Reference Name	Remark
31	LogReadErr	Read last Errors
32	LogReadBits	Read errors Bits
33	LogReset	Reset

5.12.8 Miscellaneous

Ref.	Reference Name	Remark
34	MiscReadConfig	Read Configuration area from NVRAM
35	MiscNvramReset	NVRAM Reset
36	MiscNvramMod	Modify NVRAM contents
45a	MiscPalNtscHi	Check if PAL/NTSC line is high (Not for DVDv2B)
45b	MiscPalNtscLo	Check if PAL/NTSC line is low (Not for DVDv2B)
46	MiscApplVer	Read version of application software
47a	MiscTrayOpenNr	Read the number of times the tray opened
47b	MiscPowerOnTime	Read the total time the player's power has been on
47c	MiscPlayTimeCddaVcd	Read the Playtime of CDDA and VCD discs
47d	MiscPlayTimeDvd	Read the Playtime of DVD discs

5.12.9 Basic Engine

Ref.	Reference Name	Remark
37	BeVer	Version number
38a	BeFocusOn	Focus On
38b	BeFocusOff	Focus Off
39a	BeDiscmotorOn	Discmotor On
39b	BeDiscmotorOff	Discmotor Off
40a	BeRadialOn	Radial control On
40b	BeRadialOff	Radial control Off
41a	BeSledgeIn	Sledge Inwards
41b	BeSledgeOut	Sledge Outwards
42a	BeGroovesIn	jump Grooves to Inside
42b	BeGroovesMid	jump Grooves to Middle
42c	BeGroovesOut	jump Grooves to Outside
43a	BeTrayIn	Tray In
43b	BeTrayOut	Tray Out
44	BeReset	Reset Basic Engine
58a	LaserCdOn	CD Laser on
58b	LaserCdOff	CD Laser off
58c	LaserDvdOn	DVD Laser on
58d	LaserDvdOff	DVD Laser off

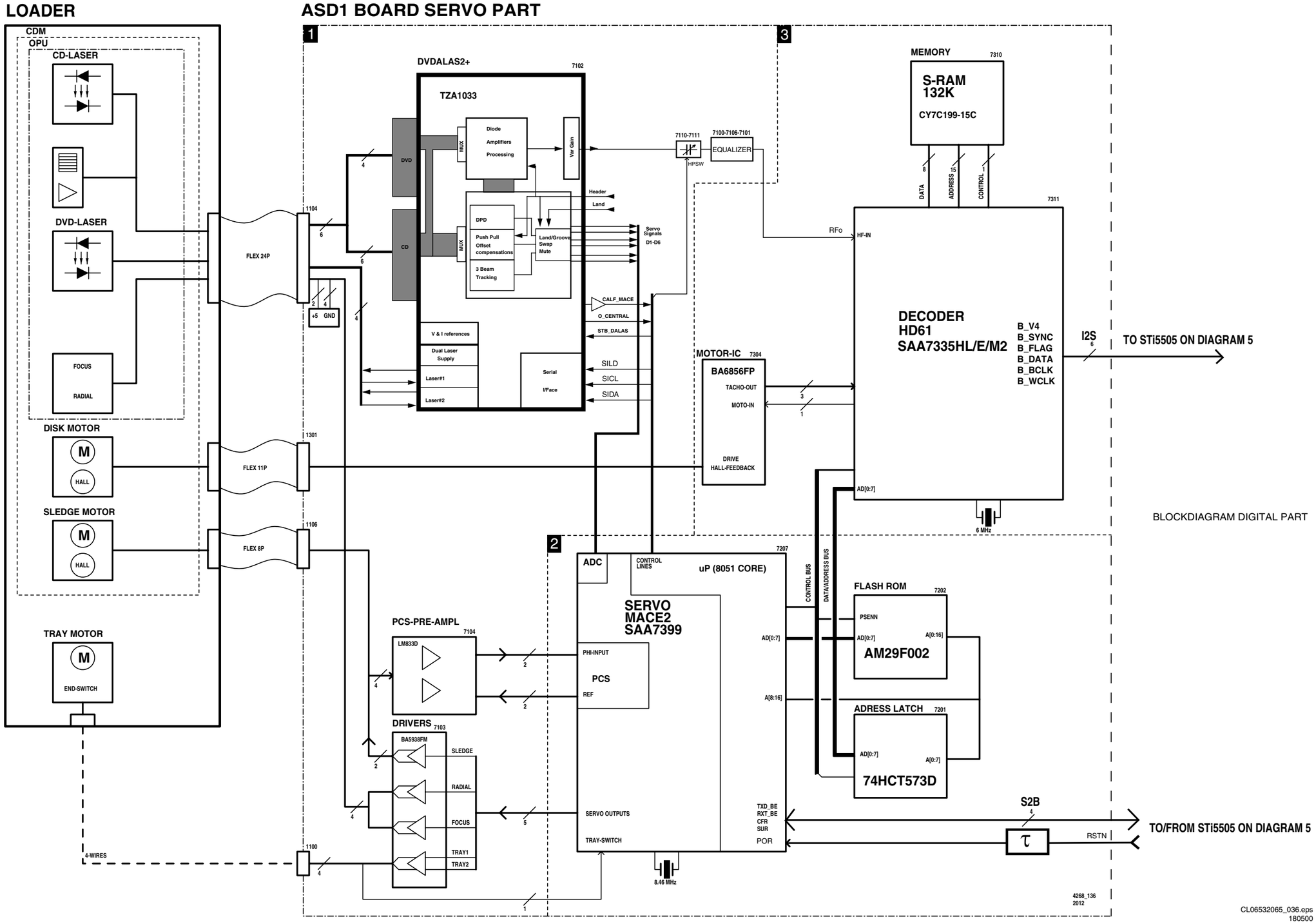
5.12.10 Karaoke

Ref.	Reference Name	Remark
48a	KaraokeModeOff	Switch Karaoke mode off
48b	KaraokeModeOn	Switch Karaoke mode on
49	KaraokeMicInput	Check path from the microphone input to audio output
50a	KaraokeKeyOn	Set Karaoke Key to the maximum level (1200 cent)
50b	KaraokeKeyOff	Set Karaoke Key to flat octave (0 cent)
51a	KaraokeEchoOn	Set Echo Control fuction on
51b	KaraokeEchoOff	Set Echo Control function off

Note: A new Compair version for repair of the MONO boards will be developed.

6. Block diagrams

Servo

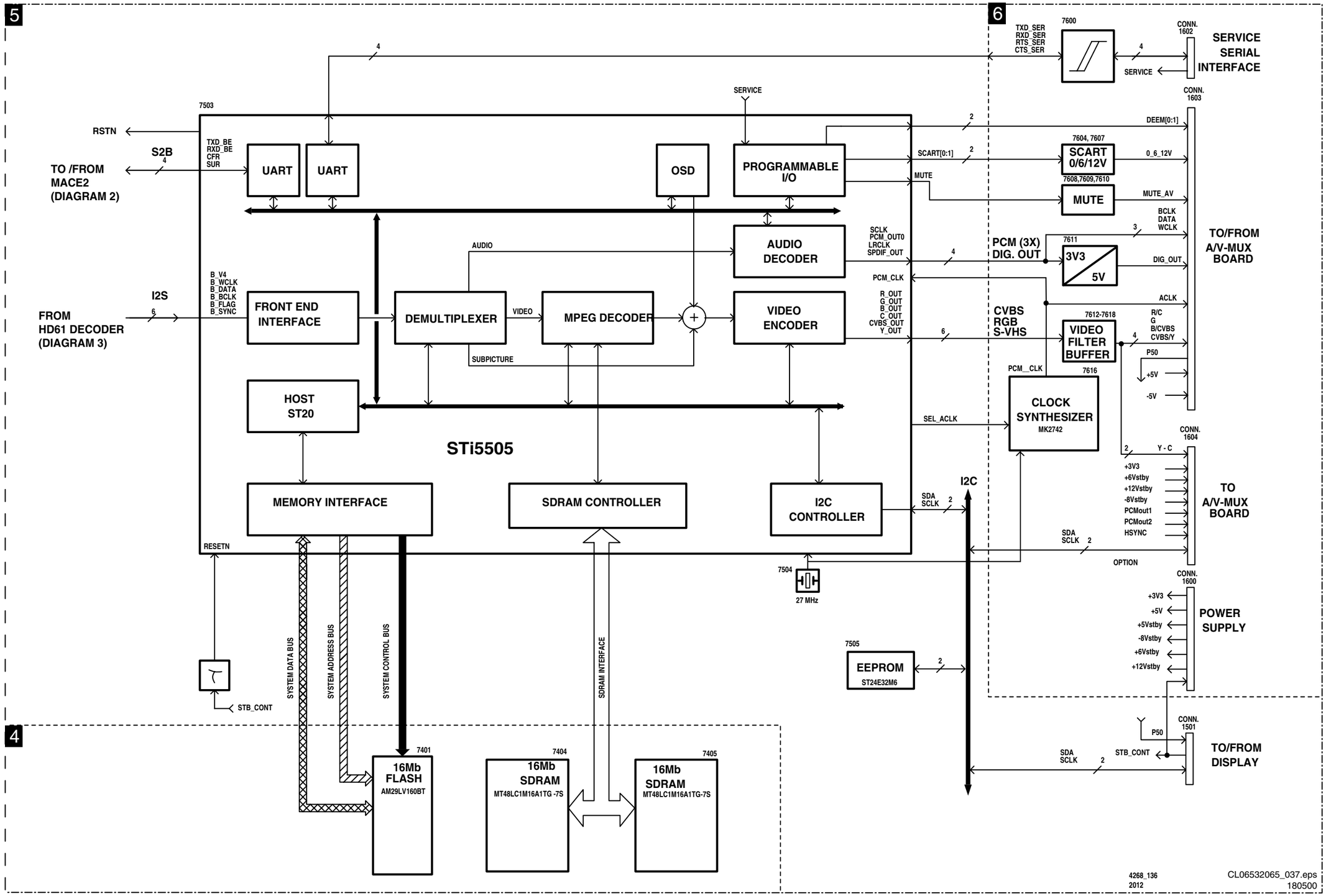


BLOCKDIAGRAM DIGITAL PART

CL06532065_036.eps
180500

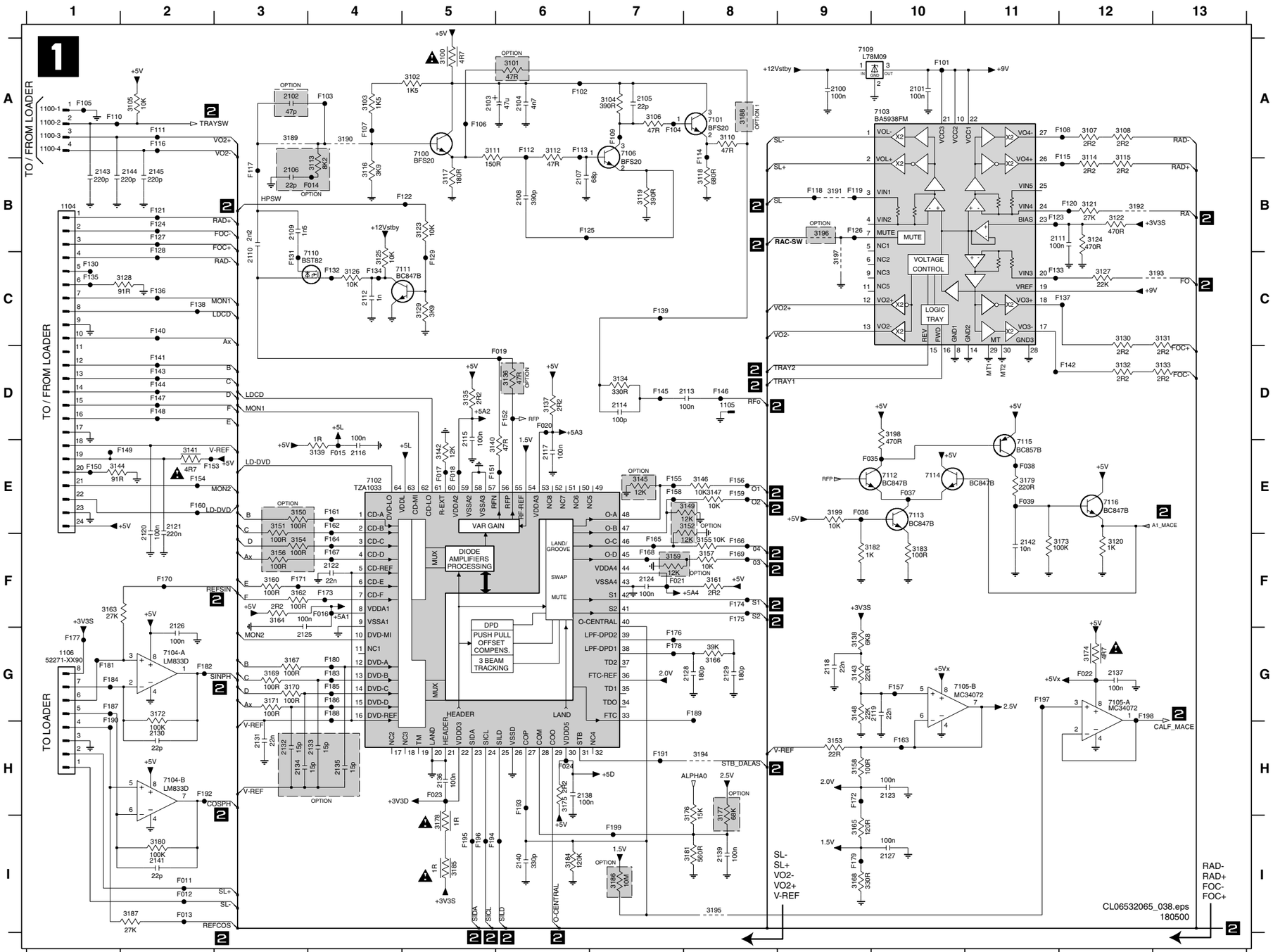
Didital

ASD1 BOARD DIGITAL PART



7. Electrical diagrams and PWB's

SERVO DALAS



1100-1 A1	3165 I9	F147 D2
1100-2 A1	3166 G8	F148 D2
1100-3 A1	3167 G3	F149 E2
1100-4 A1	3168 I9	F150 E1
1104 B1	3169 G3	F151 E5
1105 D8	3170 G3	F152 D6
1106 G1	3171 G3	F153 E2
2100 A9	3172 G2	F154 E2
2101 A10	3173 F12	F155 E7
2102 A3	3174 G12	F156 E8
2103 A5	3175 H6	F157 G10
2104 A6	3176 H8	F158 E7
2105 A7	3177 H8	F159 E8
2106 B3	3178 I5	F160 E2
2107 B6	3179 E11	F161 E4
2108 B6	3180 I2	F162 E4
2109 B3	3181 I8	F163 H10
2110 B3	3182 F10	F164 F4
2111 B11	3183 F10	F165 F7
2112 C4	3184 I6	F166 F8
2113 D8	3185 I5	F167 F4
2114 D7	3186 I7	F168 F7
2115 D5	3187 I2	F169 F8
2116 E4	3188 A8	F170 F2
2117 E6	3189 A3	F171 F3
2118 G9	3190 A4	F172 H9
2119 G10	3191 B9	F173 F4
2120 E2	3192 B12	F174 F8
2121 E2	3193 C13	F175 F8
2122 F4	3194 H8	F176 G7
2123 H10	3195 I8	F177 G1
2124 F7	3196 B9	F178 G7
2125 G3	3197 C9	F179 I9
2126 G2	3198 D10	F180 G4
2127 I10	3199 E9	F181 G1
2128 G8	7100 A5	F182 G2
2129 G8	7101 A8	F183 G4
2130 H2	7102 E4	F184 G1
2131 H3	7103 A10	F185 G4
2132 H3	7104-A G2	F186 G4
2133 H4	7104-B H2	F187 G1
2134 H3	7105-A G12	F188 G4
2135 H4	7105-B G10	F189 G8
2136 H5	7106 A7	F190 H1
2137 G12	7109 A9	F191 H7
2138 H6	7110 C4	F192 H2
2139 I8	7111 C5	F193 H6
2140 I6	7112 E10	F194 I5
2141 I2	7113 E10	F195 I5
2142 F11	7114 E10	F196 I5
2143 B1	7115 D11	F197 G11
2144 B2	7116 E12	F198 G12
2145 B2	F011 I2	F199 I7
3100 A5	F012 I2	
3101 A6	F013 I2	
3102 A5	F014 B4	
3103 A4	F015 E4	
3104 A7	F016 F4	
3105 A2	F017 E5	
3106 A7	F018 E5	
3107 A12	F019 D6	
3108 A12	F020 D6	
3110 A8	F021 F7	
3111 A5	F022 G12	
3112 A6	F023 H5	
3113 B4	F024 H6	
3114 B12	F035 E9	
3115 B12	F036 E9	
3116 B4	F037 E10	
3117 B5	F038 E11	
3118 B8	F039 E11	
3119 B7	F101 A10	
3120 F12	F102 A6	
3121 B12	F103 A4	
3122 B12	F104 A7	
3123 B5	F105 A1	
3124 B12	F106 A5	
3125 C4	F107 A4	
3126 C4	F108 A12	
3127 C12	F109 A7	
3128 C2	F110 A1	
3129 C5	F111 A2	
3130 C12	F112 A6	
3131 C13	F113 A6	
3132 D12	F114 A8	
3133 D13	F115 B12	
3134 D7	F116 A2	
3135 D5	F117 B3	
3136 D6	F118 B9	
3137 D6	F119 B9	
3138 G9	F120 B12	
3139 E4	F121 B2	
3140 E5	F122 B5	
3141 E2	F123 B11	
3142 E5	F124 B2	
3143 G9	F125 B6	
3144 E1	F126 B9	
3145 E7	F127 B2	
3146 E8	F128 C2	
3147 E8	F129 C5	
3148 G9	F130 C1	
3149 E8	F131 C3	
3150 E3	F132 C4	
3151 E3	F133 C11	
3152 E8	F134 C4	
3153 H9	F135 C1	
3154 F3	F136 C2	
3155 F8	F137 C12	
3156 F3	F138 C2	
3157 F8	F139 C7	
3158 H9	F140 C2	
3159 F7	F141 D2	
3160 F3	F142 D12	
3161 F8	F143 D2	
3162 F3	F144 D2	
3163 F1	F145 D7	
3164 F3	F146 D8	

PB 4268 ASD1
MONO-BOARD
3104 123 4268.4

SERVO MACE

PB 4268 ASD1
MONO-BOARD
3104 123 4268.4

PCS
Sledge control
Radial control
Focus control
Defect detector
Track counter
Signal cond.
OPC
Laser control
ADC/ AGC ref.
CLOCK GEN.
TEST
DEBUG
8051 core
ROM
RAM
SFR
Port 5
Port 3
Port 1
Port 4
Port 2
Port 0
System interface
ADRESS BUS
ADRESS_DATA BUS
CONTROL BUS
BE INTERFACE

{CFR,SUR,RXD_BE,TXD_BE}
{ALE,PSENn,RDI,WRI,CSI,WE,OTD-HD61,POR,PORN,RSTN,INT,MOTO1,RFo,T1,T2,T3}

CL06532065_039.eps
180500

1201 I13 F228 C11
1205 A4 F229 D11
2203 A10 F230 D2
2204 B2 F231 D11
2205 B2 F232 D11
2206 C1 F233 D1
2207 D1 F234 D2
2208 D13 F235 D11
2209 D14 F236 D2
2210 D1 F237 D10
2212 H3 F238 D13
2213 H4 F239 D10
2214 H13 F240 D13
2215 H11 F241 E10
2216 H12 F242 E13
2226 A4 F243 E10
2227 A6 F244 E13
2228 A7 F245 E10
3200 A4 F246 E13
3201 A6 F247 E10
3202 A7 F248 E13
3203 A4 F249 E10
3204 A4 F250 E2
3205 B2 F251 E13
3206 B2 F252 E10
3208 C2 F253 E13
3209 C2 F254 F10
3210 C2 F255 F10
3211 D2 F256 F10
3212 D13 F257 F11
3213 D14 F258 F2
3214 D2 F259 F11
3215 D2 F260 F14
3219 F2 F261 F2
3220 F10 F262 F10
3221 F2 F263 G2
3222 F1 F264 H4
3223 F2 F265 H3
3224 H3 F266 H9
3225 H5 F267 H8
3226 H4 F268 H8
3227 H13 F269 H7
3228 I8 F270 H9
3229 H13 F271 H8
3230 H8 F272 H9
3231 H6 F273 H5
3232 H12 F274 H5
3234 I11 F275 H5
3235 I12 F276 H6
3236 H9 F277 H6
3237 H2 F278 H4
3238 I8 F279 H4
3239 F10 F280 H6
3240 B10 F281 H14
3241 B1 F282 H7
3242 C1 F283 H7
3243 C2 F284 H8
3244 C2 F285 H13
3245 A5 F286 H12
3246 C2 F287 I11
3247 F10 F288 I12
3248 G2 F289 I7
3249 G2 F290 I7
3250 G2 F291 I6
3251 H8 F292 I6
3252 H8 F293 I8
3253 H5 F294 I12
3254 H8 F295 I7
3255 I7 F296 I7
3256 I7 F297 A4
3257 I8 F298 A10
3258 I12 F299 B2
3259 A6
3260 A7
5200 A9
6200 H12
7201 D12
7202 D13
7203 H12
7207 A3
F025 G2
F026 G2
F027 G2
F028 H4
F029 H5
F030 I8
F031 I8
F032 H8
F033 D13
F034 D13
F200 A5
F201 A5
F202 A9
F203 A6
F204 A4
F205 A7
F206 A5
F207 A6
F208 A5
F209 A6
F210 A5
F211 A4
F212 B10
F213 B2
F214 B10
F215 B2
F216 B10
F217 B2
F218 C10
F219 C10
F220 C2
F221 C2
F222 C11
F223 C11
F224 C2
F225 C11
F226 C1
F227 C2

Decoder

PB 4268 ASD1
MONO-BOARD
3104 123 4268.4

CL06532065_040.eps
180500

1300 A6 F353 G12
1301 G13 F354 H12
2300 A11 F355 H9
2301 A8 F356 H13
2302 A5 F357 H6
2303 A5 F358 H7
2304 B5 F359 H12
2305 C5 F360 H8
2306 C2 F361 H9
2307 C3 F362 H8
2309 F7 F363 H9
2310 G11 F364 H12
2311 H12 F365 I13
2312 H12 F366 I12
2313 H12 F367 I12
2314 H8 F368 I9
2315 I9 F369 I13
2318 B3 F370 I12
2319 C4 F371 I9
3300 A11 F372 I12
3301 A6 F373 I12
3302 A7
3304 B3
3305 C3
3309 C5
3310 E5
3311 F7
3312 F6
3313 F6
3316 G9
3317 G9
3318 H7
3319 H13
3320 H6
3321 H12
3322 H8
3323 H8
3324 I9
3325 I12
3326 I13
3327 I12
3328 I12
3329 I13
3330 B5
3331 B4
3332 C4
3333 F8
3334 F8
3335 F8
3336 F8
3337 F9
3338 F9
3339 C5
3340 H9
5300 A8
5301 A5
6301 G8
6302 G9
6303 G8
7304 G11
7310 A10
7311 A6
7312 I13
7315 H7
F300 A11
F301 A8
F302 A7
F303 A5
F304 A6
F305 B10
F306 B5
F307 B10
F308 B10
F309 B4
F310 B10
F311 B10
F312 B4
F313 B10
F314 B5
F315 C10
F316 C5
F317 C10
F318 C10
F319 C5
F320 C10
F321 C10
F322 C5
F323 C10
F324 D10
F325 D10
F326 D10
F327 D10
F328 D10
F329 D10
F330 D10
F331 E10
F332 E10
F333 E10
F334 E10
F335 E10
F336 F7
F337 F7
F338 F8
F339 F6
F340 F6
F341 F7
F342 F9
F343 F9
F344 F8
F345 F8
F346 F8
F347 F9
F348 F8
F349 G9
F350 G12
F351 G9
F352 G12

Memory

4 MEMORY PART

PB 4268 ASD1
MONO-BOARD
3104 123 4268.4

OPTION = NOT USED FOR FUTURE APPLICATION: I²C FROM MASTER TO SLAVE FOR SYSTEMS / COMBI'S

SYSTEM DATA Bus 5
SYSTEM ADDRESS Bus 5
RAM/ROM Interface 5
SDRAM Interface 5

OPTION

+5Vstby, 5400 100MHZ, F421, +5V_DS, 2400 100n
7406 PCF8584T
RESET_I2C, CE1, DTACKn, IRQ_I2C, CLK_8MHz, SDA_EXE, SCL_EXE
F422, F423, F424, F425, 3400 100R, 3401 100R
RESET_|STROBE_, CS_, A0, WR_, RD_, INT_|SCL-OUT, IACK_|SDA-IN, CLK, SDA|SDA-OUT, SCL|SCL-IN, VSS
DB7..DB0 → D7..D0
RWN, A1

OPTION

+5V_DS, 2415 100n, 3402 10K, DTACKn, 7400-A 74HCT00D, F406, 7400-D 74HCT00D, 3418, WAIT 5
+5V_DS, 7400-B 74HCT00D, CE1 5

OPTION

+5VOSC, 2416 100n, 2417 100n
7402 74HCT1G79, F430, 7403 74HCT1G04
AUXCLK 5, F431, 3407 22R, NC, CLK_8MHz

7401 Am29LV160BT
VDD_MEM, 2405 100n, VCC
A0..A20, DQ0..DQ15|A-1
3412, F434, 3413 OPTION, RWN, CE_ROMn, FLASH_OEN
F435, 3405 10K, 3414_, 3415 OPTION, F432, 3416_
VDD_MEM
CE_, OE_, WE_, RESET_, BYTE_, VSS1, VSS2

7404 MT48LC1M16A1TG — BOTTOM
7405 MT48LC1M16A1TG — TOP
VDD_MEM2
2401 100n, 2402 100n, 2403 100n, 2404 100n, 2406 100n, 2407 100n, 2408 100n, 2409 100n, 2410 100n, 2411 100n, 2412 100n, 2413 100n
VDD, VDDQ, 1, 25, 7, 13, 38, 44
AD11, AD0..AD10, CLK, VDD_MEM2 3403 10K F415, CSN1, RASN, CASN, WEN, DQMU, DQML
3404 10K F416, CSN2
BA, BANK SELECT
ADDRESS REGISTER
DATA INPUT REGISTER
I/O CONTROL
LWE, LDQM
ROW BUFFER REFRESH COUNTER
ROW DECODER
512Kx16 × 2
SENSE AMP
OUTPUT BUFFER
COLUMN DECODER
LATENCY & BURST LENGTH
PROGRAMMING REGISTER
TIMING REGISTER
LCKE, LRAS, LCBR, LCAS, LWE, LWCBR, LQDM
DQ0..DQ15 → D0..D15
NC 33 37
VSS 26 50, VSSQ 4 10 41 47

OPTION

3409, +5V_DS, 27M_CLK1 5, 7400-C 74HCT00D, 2414 100n, 3406 100R, F428, 27M_CLKOUT 5
3410

+3V3, 5402 100MHZ, F419, VDD_MEM, 2418 100u
+3V3, 5403 100MHZ, F420, VDD_MEM2, 2419 47u, 2420 47u

CL06532065_041.eps
290500

2400 B3
2401 C9
2402 C10
2403 C12
2404 C13
2405 B6
2406 C9
2407 C10
2408 C12
2409 C13
2410 C9
2411 C10
2412 C12
2413 C13
2414 H7
2415 E1
2416 H2
2417 H3
2418 I10
2419 I13
2420 I13
3400 C1
3401 C2
3402 E1
3403 F8
3404 F11
3405 F5
3406 I7
3407 I3
3409 H7
3410 I6
3412 E5
3413 F5
3414 F5
3415 F5
3416 G5
3418 E4
5400 A3
5402 I9
5403 I12
7400-A E2
7400-B F2
7400-C I6
7400-D E3
7401 C6
7402 H2
7403 H3
7404 D9
7405 D12
7406 B3
F406 E2
F415 G8
F416 G11
F419 I10
F420 I13
F421 A3
F422 C2
F423 C2
F424 C2
F425 C2
F428 I8
F430 H2
F431 H1
F432 G5
F434 F5
F435 F5

STI 5505

BASIC ENGINE INTERFACE Bus

I2C Bus

SYSTEM ADDRESS Bus

SYSTEM DATA Bus

RAM/ROM Interface

SDRAM Interface

MEMORY interface

SYSTEM USE

PORT 0 I/O

PORT 1 I/O

PORT 2 I/O

PORT 3 I/O

PORT 4 I/O

JTAG

TEST

IRQ

uP ST20cpu

FRONT-END Interface

A/V/Sub demultiplexer

MPEG DECODER

SDRAM CONTROLLER

ADDRESS

DATA

Audio

Video

Subpicture

Subpicture decoder

AC3 LPCM MPEG1/2 AUDIO DECODER

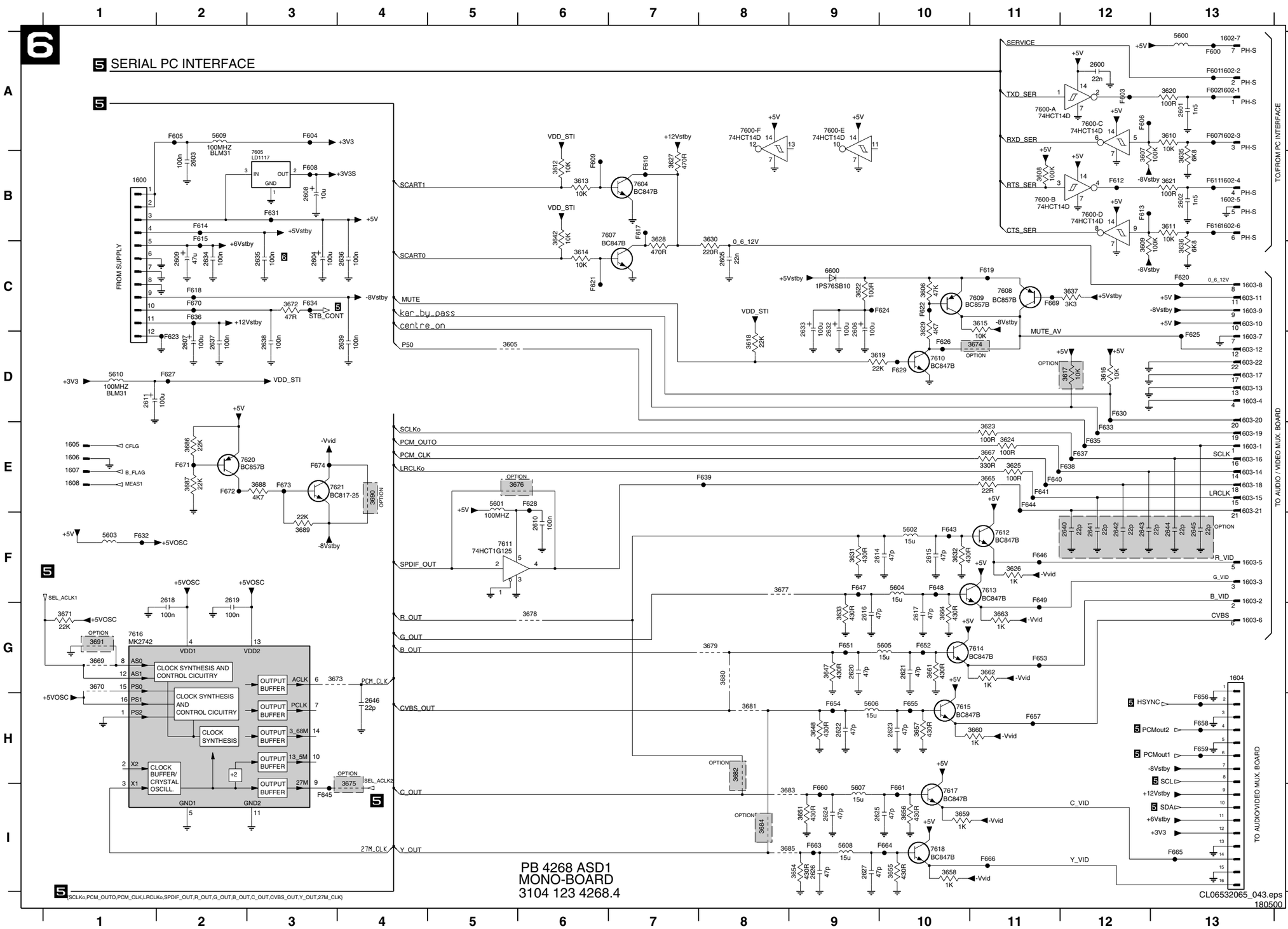
VIDEO ENCODER

PB 4268 ASD1
MONO-BOARD
3104 123 4268.4

CL06532065_042.eps
180500

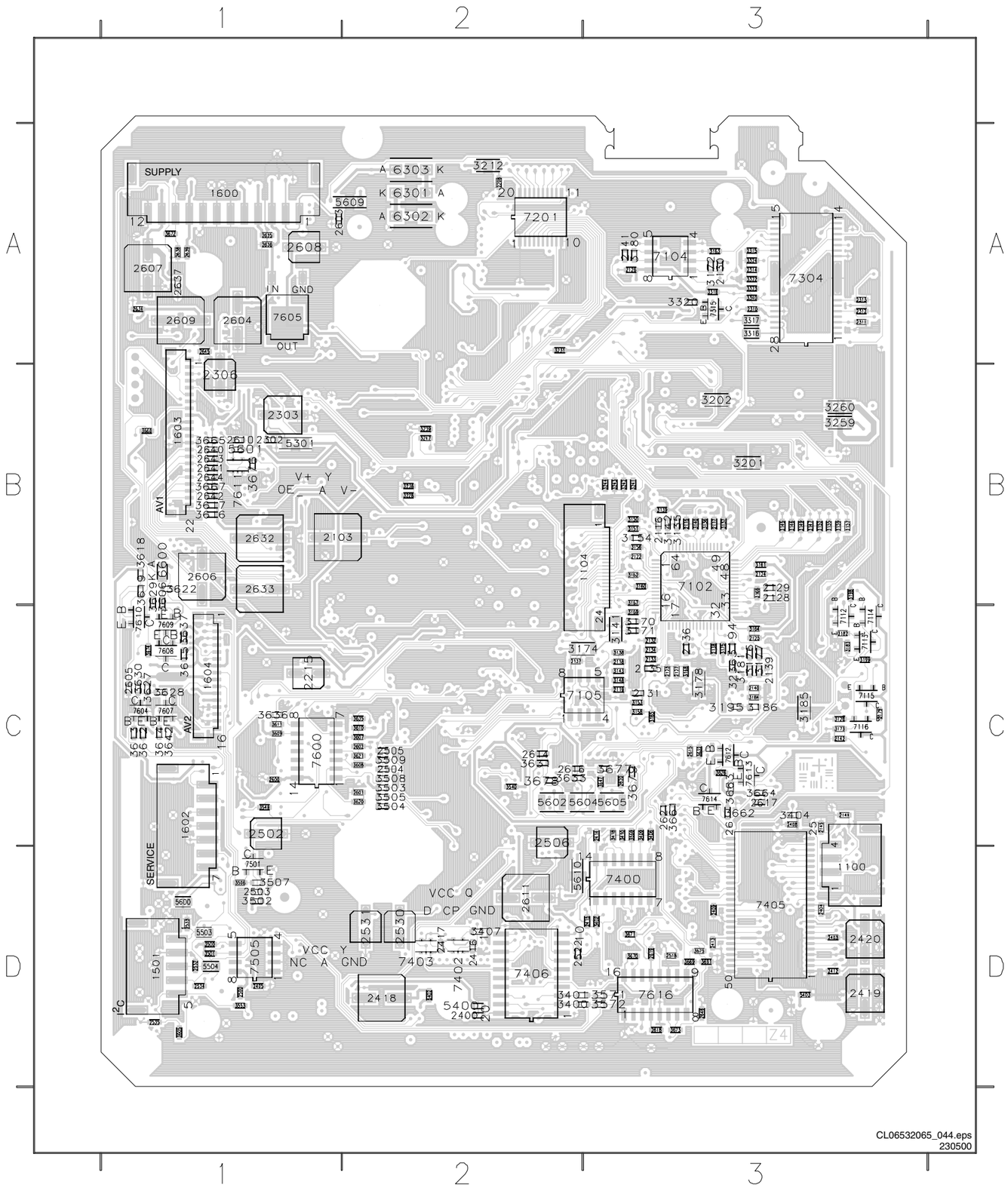
1501-1 A1
1501-2 B1
1501-3 B1
1501-4 B1
1501-5 B1
1506-1 A14
1506-10 B14
1506-11 B14
1506-12 B14
1506-13 B14
1506-14 B14
1506-15 B14
1506-16 C14
1506-17 C14
1506-18 C14
1506-19 C14
1506-2 A14
1506-20 C14
1506-21 C14
1506-22 C14
1506-23 D14
1506-24 D14
1506-3 A14
1506-4 A14
1506-5 A14
1506-6 A14
1506-7 A14
1506-8 A14
1506-9 B14
2500 A3
2502 B5
2504 C11
2505 B11
2506 D14
2507 D14
2508 E14
2509 E13
2510 I3
2511 I3
2512 I4
2513 I4
2514 I4
2515 I4
2516 I5
2517 I5
2518 I5
2519 I9
2520 I9
2521 I9
2522 I10
2523 I10
2524 I10
2525 I10
2526 I11
2527 H13
2528 I11
2529 I11
2530 I11
2531 I11
2532 B1
2533 A1
2534 B1
2535 B1
3500 B3
3501 B3
3502 B5
3503 B11
3504 B11
3505 B11
3506 B4
3507 B5
3508 B11
3509 B11
3511 C6
3512 C6
3513 A10
3515 C6
3516 C6
3517 C13
3519 C9
3520 C11
3521 C12
3522 C12
3523 D13
3524 D14
3525 E14
3526 F2
3534 I12
3535 I13
3536 I14
3537 I12
3538 I13
3540 C9
3541 B7
3542 B8
3545 D14
3546 C7
3547 B6
3548 A10
3549 B10
3550 B10
3551 B10
3552 B10
3553 B11
3554 B10
3555 B9
3556 B9
3557 B9
3558 B9
3559 B9
3560 B9
3561 B9
3562 C7
3563 C7
3564 C7
3565 C8
3566 C7
3567 C7
3568 C8
3569 I12
3570 F14
3571 A2
3572 B2
3573 I12
5501 H11
5502 I11
5503 A1
5504 B1
5505 B5
7501 B5
7503 D2
7504 I13
7505 A2
F050 I14
F051 I14
F052 C7
F053 C7
F054 C12
F055 D14
F056 F14
F058 C7
F059 C8
F500 A13
F501 A11
F502 B5
F503 A6
F504 B9
F505 B9
F506 B9
F507 B9
F508 B9
F509 B9
F510 B9
F511 A1
F512 B1
F513 B11
F514 B6
F515 B1
F516 B1
F517 B11
F518 B6
F519 C9
F520 C7
F521 C10
F522 C11
F523 C13
F524 C10
F525 C11
F526 C7
F527 C7
F528 C11
F529 D7
F530 C10
F531 C10
F532 C10
F533 C10
F534 C10
F535 C5
F536 C6
F537 C11
F538 C6
F539 C6
F540 C6
F541 C12
F542 C9
F543 C7
F544 C9
F545 C9
F546 C9
F547 C9
F548 C9
F549 C9
F552 C7
F553 C8
F554 D8
F555 D6
F556 D12
F557 D12
F558 D14
F559 E14
F560 E14
F562 E14
F564 F14
F566 F14
F567 F14
F568 F2
F569 F14
F573 G14
F574 G14
F576 G14
F578 G2
F579 G2
F580 G2
F581 G2
F582 G2
F583 G2
F590 H13
F592 I8
F593 I8
F594 I8
F595 I8
F596 I8
F597 I8
F598 I8
F599 I8
[SCLKo,PCM_OUTO,PCM_CLK,LRCLKo,SPDIF_OUT,R_OUT,G_OUT,B_OUT,C_OUT,CVBS_OUT,Y_OUT,27M_CLK]

Service interface and Back-end



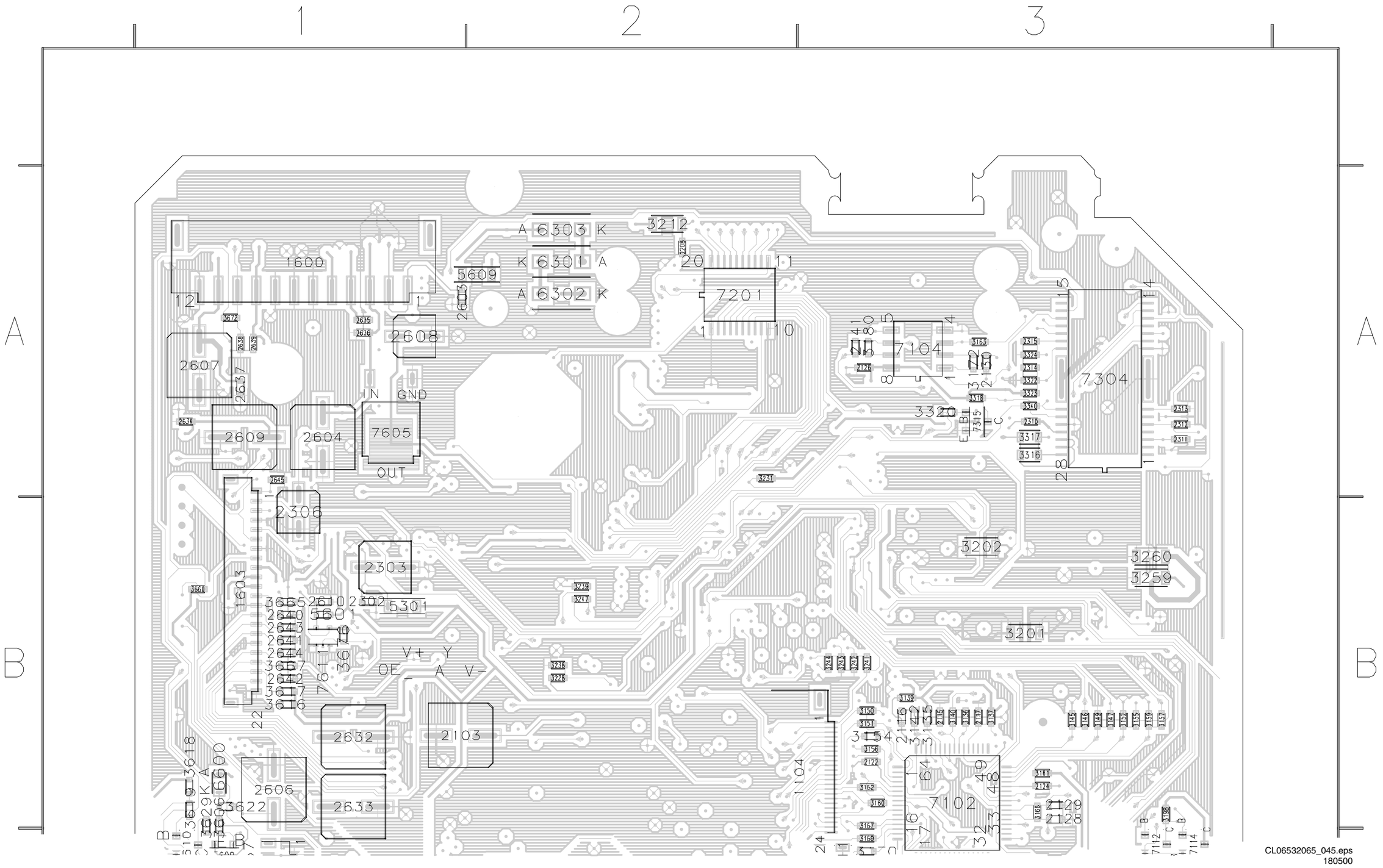
1600 B1	3658 I10	F652 G10	
1602-1 A13	3659 I10	F653 G11	
1602-2 A13	3660 H11	F654 H9	
1602-3 A13	3661 G10	F655 H10	
1602-4 B13	3662 G11	F656 H13	
1602-5 B13	3663 G11	F657 H11	
1602-6 B13	3664 G10	F658 H13	
1602-7 A13	3665 E11	F659 H13	
1603-1 E13	3667 E11	F660 I9	
1603-10 C13	3669 G1	F661 I10	
1603-11 C13	3670 G1	F663 I9	
1603-12 D13	3671 G1	F664 I10	
1603-13 D13	3672 C3	F665 I13	
1603-14 E13	3673 G3	F666 I11	
1603-15 E13	3674 D11	F669 C11	
1603-16 E13	3675 I4	F670 C2	
1603-17 D13	3676 E5	F671 E2	
1603-18 E13	3677 F8	F672 E2	
1603-19 E13	3678 G6	F673 E3	
1603-2 G13	3679 G8	F674 E3	
1603-20 E13	3680 G8		
1603-21 F13	3681 H8		
1603-22 D13	3682 H8		
1603-3 F13	3683 I8		
1603-4 D13	3684 I8		
1603-5 F13	3685 I8		
1603-6 G13	3686 E2		
1603-7 D13	3687 E2		
1603-8 C13	3688 E3		
1603-9 C13	3689 F3		
1604 G13	3690 E4		
1605 E1	3691 G1		
1606 E1	5600 A13		
1607 E1	5601 E5		
1608 E1	5602 F10		
2600 A12	5603 F1		
2601 A13	5604 F10		
2602 B13	5605 G10		
2603 B2	5606 H9		
2604 C3	5607 I9		
2605 C8	5608 I9		
2606 C9	5609 A2		
2607 D2	5610 D1		
2608 B3	6600 C9		
2609 C2	7600-A A11		
2610 F6	7600-B B11		
2611 D1	7600-C A12		
2614 F9	7600-D B12		
2615 F10	7600-E A9		
2616 G9	7600-F A8		
2617 G10	7604 B7		
2618 F2	7605 B3		
2619 F2	7607 B6		
2620 G9	7608 C11		
2621 G10	7609 C10		
2622 H9	7610 D10		
2623 H10	7611 F5		
2624 I9	7612 F11		
2625 I9	7613 F11		
2626 I9	7614 G10		
2627 I9	7615 H10		
2632 C9	7616 G1		
2633 C9	7617 I10		
2634 C2	7618 I10		
2635 C3	7620 E2		
2636 C4	7621 E3		
2637 D2	F600 A13		
2638 D3	F601 A13		
2639 D4	F602 A13		
2640 F12	F603 A12		
2641 F12	F604 A3		
2642 F12	F605 A2		
2643 F12	F606 A12		
2644 F13	F607 A13		
2645 F13	F608 B3		
2646 H4	F609 B6		
3605 D5	F610 B7		
3606 C10	F611 B13		
3607 B12	F612 B12		
3608 B11	F613 B12		
3609 C12	F614 B2		
3610 A13	F615 B2		
3611 B13	F616 B13		
3612 B6	F617 B7		
3613 B6	F618 C2		
3614 C6	F619 C11		
3615 C11	F620 C13		
3616 D12	F621 C6		
3617 D12	F622 C10		
3618 D8	F623 D2		
3619 D9	F624 C10		
3620 A13	F625 D13		
3621 B13	F626 D10		
3622 C9	F627 D2		
3623 E11	F628 E6		
3624 E11	F629 D10		
3625 E11	F630 D12		
3626 F11	F631 B3		
3627 B7	F632 F1		
3628 C7	F633 E12		
3629 C10	F634 C3		
3630 C8	F635 E12		
3631 F9	F636 C2		
3632 F10	F637 E12		
3633 G9	F638 E12		
3635 B13	F639 E8		
3636 C13	F640 E11		
3637 C12	F641 E11		
3642 B6	F643 F10		
3647 G9	F644 E11		
3648 H9	F645 I3		
3651 I9	F646 F11		
3654 I9	F647 F9		
3655 I10	F648 F10		
3656 I10	F649 F11		
3657 H10	F651 G9		

Top view



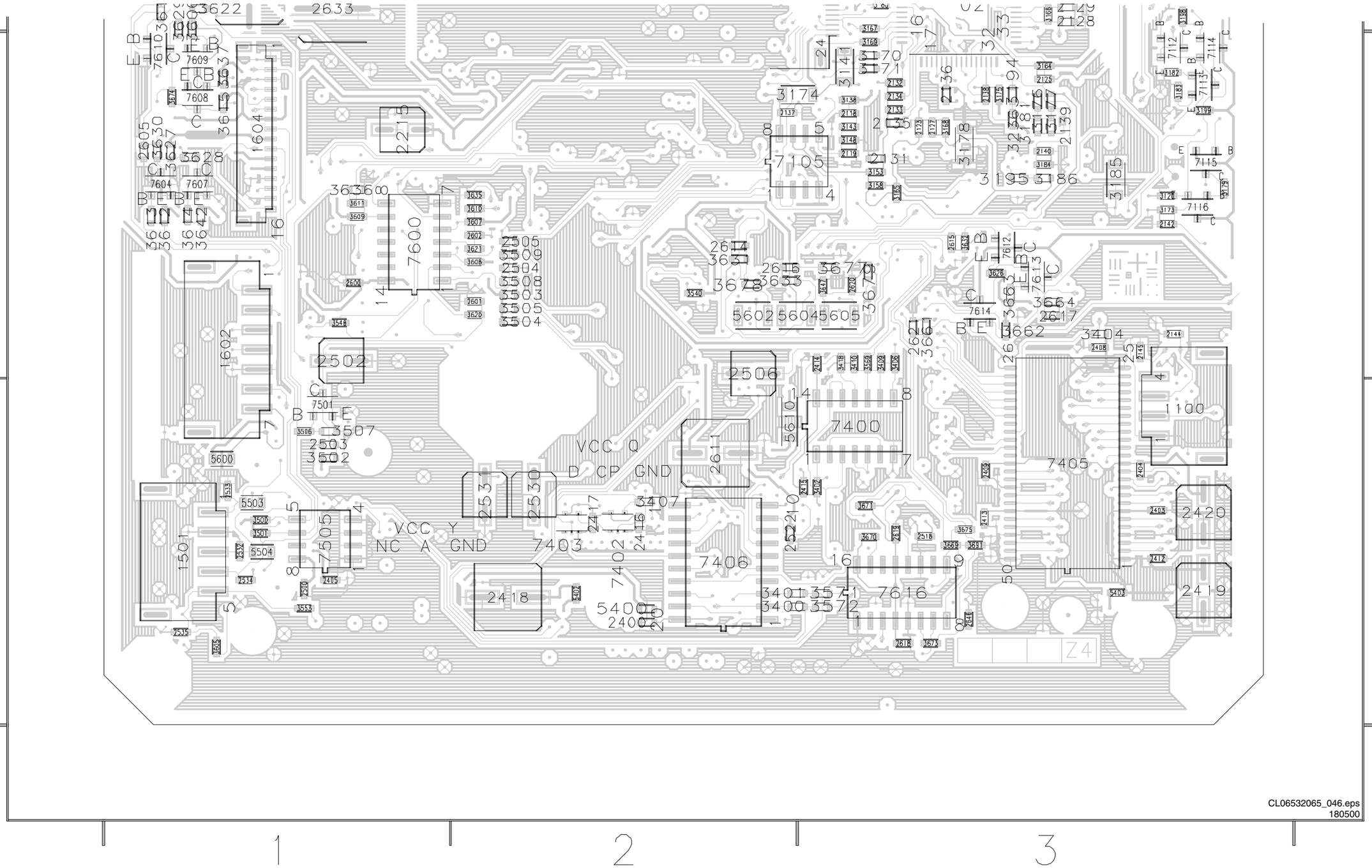
1100	D3	2618	D3	3318	A3	5609	A2
1104	B3	2619	D3	3320	A3	5610	D2
1501	D1	2620	C3	3322	A3	6301	A2
1600	A1	2621	C3	3323	A3	6302	A2
1602	C1	2632	B1	3324	A3	6303	A2
1603	B1	2633	B1	3340	A3	6600	B1
1604	C1	2634	A1	3400	D2	7102	B3
2103	B1	2635	A1	3401	D2	7104	A3
2115	B3	2636	A1	3402	D3	7105	C3
2116	B3	2637	A1	3404	C3	7112	C3
2117	B3	2638	A1	3406	C3	7113	C3
2118	C3	2639	A1	3407	D2	7114	C3
2119	C3	2640	B1	3409	C3	7115	C3
2122	B3	2641	B1	3410	C3	7116	C3
2123	C3	2642	B1	3418	C3	7201	A2
2124	B3	2643	B1	3500	D1	7304	A3
2125	C3	2644	B1	3501	D1	7315	A3
2126	A3	2645	A1	3502	D1	7400	D3
2127	C3	2646	D3	3503	C2	7402	D2
2128	B3	3120	C3	3504	C2	7403	D2
2129	B3	3135	B3	3505	C2	7405	D3
2130	A3	3136	B3	3506	D1	7406	D2
2131	C3	3137	B3	3507	D1	7501	D1
2132	C3	3138	C3	3508	C2	7505	D1
2133	C3	3139	B3	3509	C2	7600	C1
2134	C3	3140	B3	3540	C2	7604	C1
2135	C3	3141	C3	3548	C1	7605	A1
2136	C3	3142	B3	3553	D1	7607	C1
2137	C3	3143	C3	3569	C3	7608	C1
2138	C3	3145	B3	3571	D3	7609	C1
2139	C3	3146	B3	3572	D3	7610	C1
2140	C3	3147	B3	3605	D1	7611	B1
2141	A3	3148	C3	3606	B1	7612	C3
2142	C3	3149	B3	3607	C2	7613	C3
2144	C3	3150	B3	3608	C2	7614	C3
2145	C3	3151	B3	3609	C1	7616	D3
2208	A2	3152	B3	3610	C2		
2215	C1	3153	C3	3611	C1		
2302	B1	3154	B3	3612	C1		
2303	B1	3155	B3	3613	C1		
2306	B1	3156	B3	3614	C1		
2310	A3	3157	B3	3615	C1		
2311	A3	3158	C3	3616	B1		
2312	A3	3159	B3	3617	B1		
2313	A3	3160	B3	3618	B1		
2314	A3	3161	B3	3619	B1		
2315	A3	3162	B3	3620	C2		
2400	D2	3163	A3	3621	C2		
2403	D3	3164	C3	3622	B1		
2404	D3	3165	C3	3626	C3		
2405	D1	3166	B3	3627	C1		
2408	C3	3167	B3	3628	C1		
2409	D3	3168	C3	3629	B1		
2412	D3	3169	C3	3630	C1		
2413	D3	3170	C3	3631	C2		
2414	C3	3171	C3	3632	C3		
2415	D3	3172	A3	3633	C2		
2416	D2	3173	C3	3635	C2		
2417	D2	3174	C3	3636	C1		
2418	D2	3175	C3	3637	C1		
2419	D3	3176	C3	3642	C1		
2420	D3	3177	C3	3647	C3		
2500	D1	3178	C3	3660	B1		
2502	C1	3179	C3	3661	C3		
2503	D1	3180	A3	3662	C3		
2504	C2	3181	C3	3663	C3		
2505	C2	3182	C3	3664	C3		
2506	C2	3183	C3	3665	B1		
2518	D3	3184	C3	3667	B1		
2522	D2	3185	C3	3669	D3		
2530	D2	3186	C3	3670	D3		
2531	D2	3194	C3	3671	D3		
2532	D1	3195	C3	3672	A1		
2533	D1	3198	B3	3673	D3		
2534	D1	3199	C3	3674	C1		
2535	D1	3201	B3	3675	D3		
2600	C1	3202	B3	3676	B1		
2601	C2	3212	A2	3677	C3		
2602	C2	3228	B2	3678	C2		
2603	A1	3231	A2	3679	C3		
2604	A1	3236	C3	3691	D3		
2605	C1	3238	B2	5301	B1		
2606	B1	3239	B2	5400	D2		
2607	A1	3241	B3	5402	D2		
2608	A1	3242	B3	5403	D3		
2609	A1	3243	B3	5503	D1		
2610	B1	3244	B3	5504	D1		
2611	D2	3247	B2	5600	D1		
2614	C2	3259	B3	5601	B1		
2615	C3	3260	B3	5602	C2		
2616	C2	3316	A3	5604	C3		
2617	C3	3317	A3	5605	C3		

Detailed Top view 1

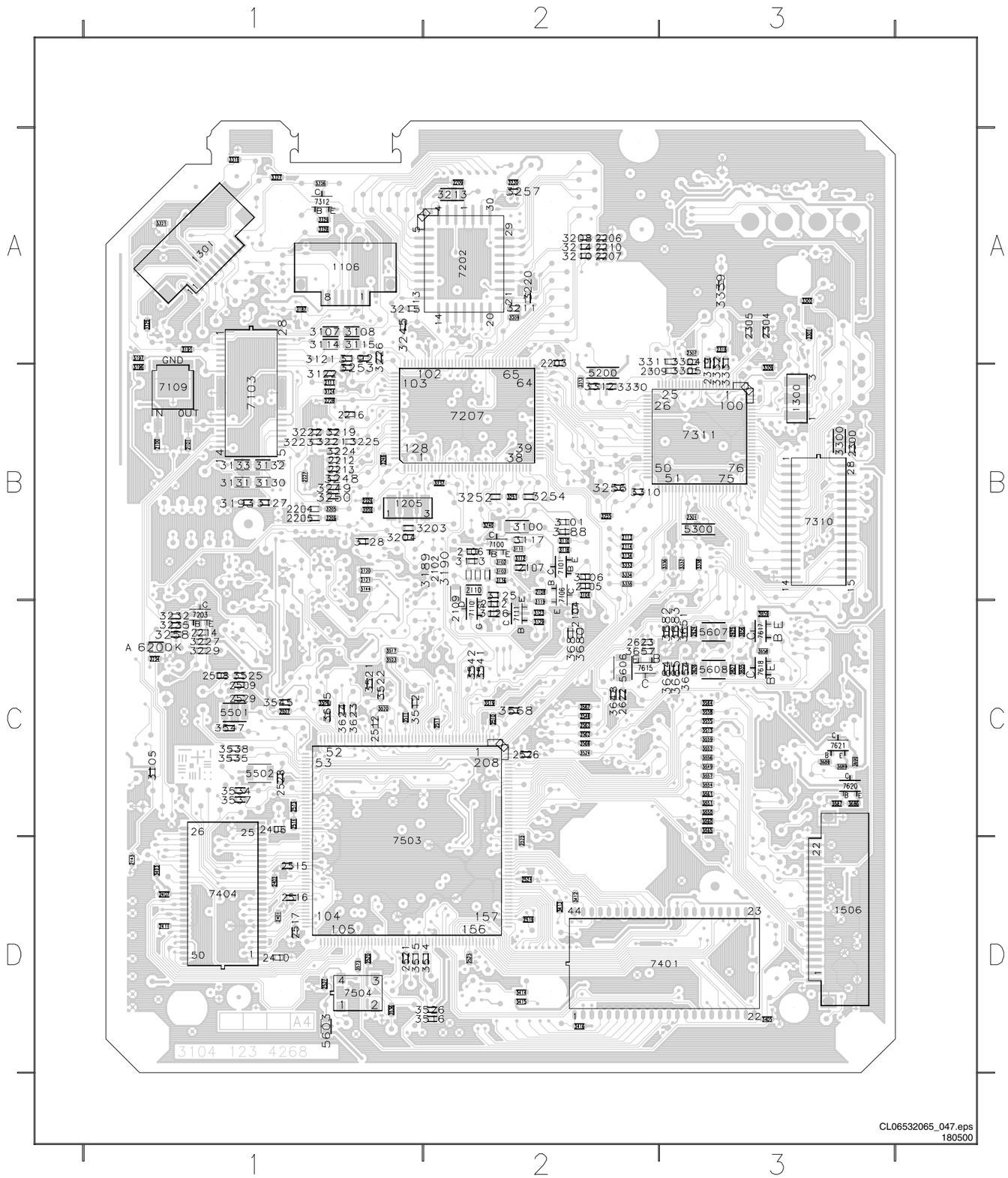


CL06532065_045.eps
180500

Detailed Top view 2

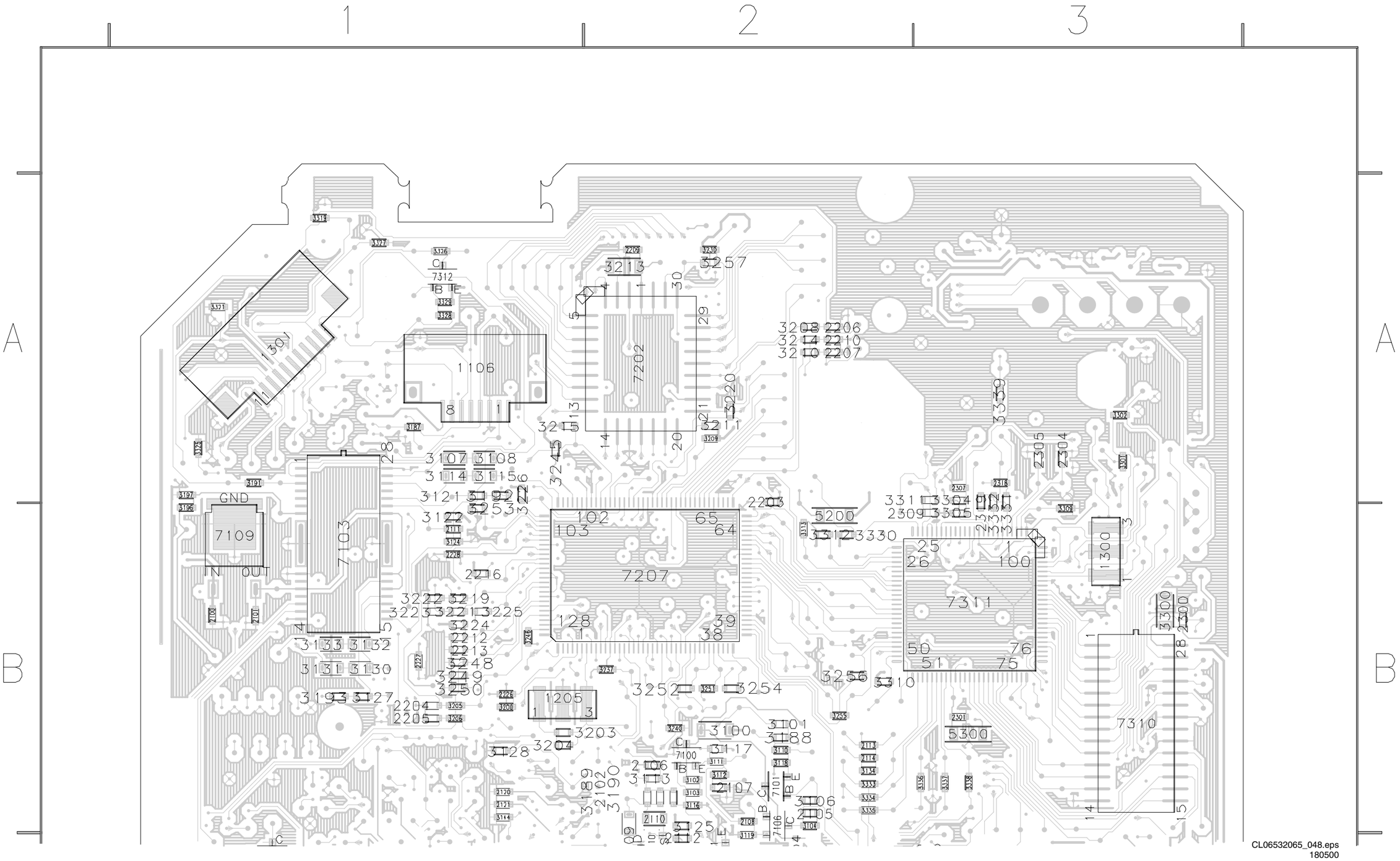


Bottom view

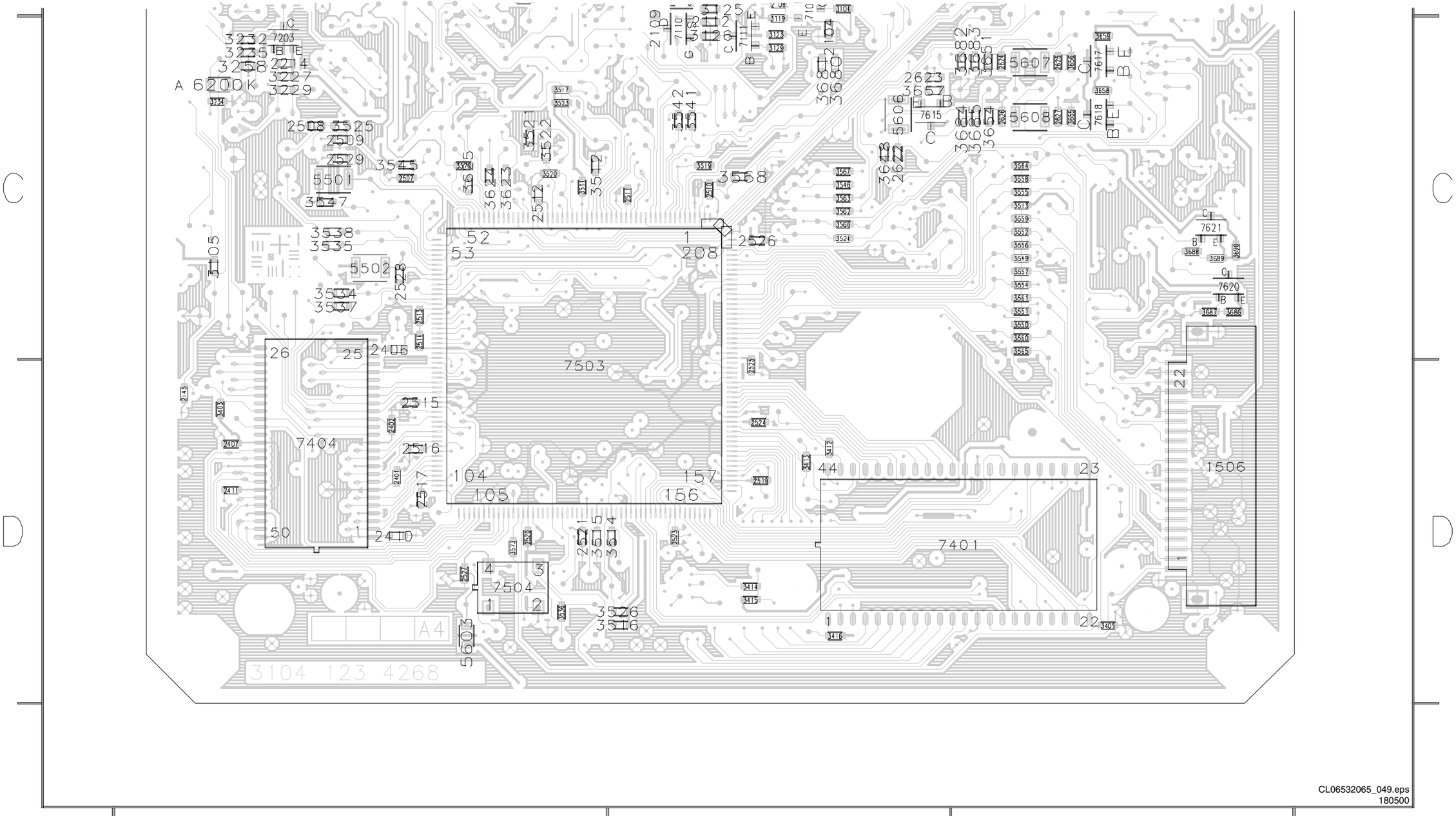


1106	A1	3117	B2	3338	B3	7202	A2
1205	B1	3118	B2	3339	A3	7203	C1
1300	B3	3119	C2	3403	D1	7207	B2
1301	A1	3121	A1	3405	D3	7310	B3
1506	D3	3122	B1	3412	D2	7311	B3
2100	B1	3123	C2	3413	D2	7312	A1
2101	B1	3124	B1	3414	D2	7401	D3
2102	B2	3125	B2	3415	D2	7404	D1
2104	C2	3126	C2	3416	D2	7503	D1
2105	B2	3127	B1	3511	C1	7504	D1
2106	B2	3128	B1	3512	C1	7615	C2
2107	B2	3129	C2	3513	C3	7617	C3
2108	B2	3130	B1	3514	D2	7618	C3
2109	C2	3131	B1	3515	D1	7620	C3
2110	B2	3132	B1	3516	D2	7621	C3
2111	B1	3133	B1	3517	C1		
2112	C2	3134	B2	3519	C2		
2113	B2	3144	B1	3520	C1		
2114	B2	3187	A1	3521	C1		
2120	B1	3188	B2	3522	C1		
2121	B1	3189	B2	3523	C1		
2143	D1	3190	B2	3524	C2		
2203	A2	3191	A1	3525	C1		
2204	B1	3192	A1	3526	D2		
2205	B1	3193	B1	3534	C1		
2206	A2	3196	B1	3535	C1		
2207	A2	3197	A1	3536	D1		
2209	A2	3200	B1	3537	C1		
2210	A2	3203	B2	3538	C1		
2212	B1	3204	B1	3541	C2		
2213	B1	3205	B1	3542	C2		
2214	C1	3206	B1	3545	C1		
2216	B1	3208	A2	3546	C2		
2226	B1	3209	A2	3547	C1		
2227	B1	3210	A2	3549	C3		
2228	B1	3211	A2	3550	C3		
2300	B3	3213	A2	3551	C3		
2301	B3	3214	A2	3552	C3		
2304	A3	3215	A1	3554	C3		
2305	A3	3219	B1	3555	C3		
2307	A3	3220	A2	3556	C3		
2309	B2	3221	B1	3557	C3		
2318	A3	3222	B1	3558	C3		
2319	B3	3223	B1	3559	C3		
2401	D1	3224	B1	3560	C3		
2402	D1	3225	B1	3561	C3		
2406	C1	3226	A1	3562	C2		
2407	D1	3227	C1	3563	C2		
2410	D1	3229	C1	3564	C3		
2411	D1	3230	A2	3565	C3		
2507	C1	3232	C1	3566	C2		
2508	C1	3234	C1	3567	C2		
2509	C1	3235	C1	3568	C2		
2510	C2	3237	B2	3570	C1		
2511	C2	3240	B2	3573	D1		
2512	C1	3245	A1	3623	C1		
2513	C1	3246	B1	3624	C1		
2514	C1	3248	B1	3625	C1		
2515	D1	3249	B1	3648	C2		
2516	D1	3250	B1	3651	C3		
2517	D1	3251	B2	3654	C3		
2519	D2	3252	B2	3655	C3		
2520	D1	3253	B1	3656	C3		
2521	D1	3254	B2	3657	C2		
2523	D2	3255	B2	3658	C3		
2524	D2	3256	B2	3659	C3		
2525	D2	3257	A2	3680	C2		
2526	C2	3258	C1	3681	C3		
2527	D1	3300	B3	3682	C3		
2528	C1	3301	A3	3683	C3		
2529	C1	3302	A3	3684	C3		
2622	C2	3304	A3	3685	C3		
2623	C2	3305	B3	3686	C3		
2624	C3	3309	B3	3687	C3		
2625	C3	3310	B2	3688	C3		
2626	C3	3311	A2	3689	C3		
2627	C3	3312	B2	3690	C3		
3100	B2	3313	B2	5200	B2		
3101	B2	3319	A1	5300	B3		
3102	B2	3321	A1	5501	C1		
3103	B2	3325	A1	5502	C1		
3104	B2	3326	A1	5603	D1		
3105	C1	3327	A1	5606	C2		
3106	B2	3328	A1	5607	C3		
3107	A1	3329	A1	5608	C3		
3108	A1	3330	B2	6200	C1		
3110	B2	3331	B3	7100	B2		
3111	B2	3332	B3	7101	B2		
3112	B2	3333	B2	7103	B1		
3113	B2	3334	B2	7106	B2		
3114	A1	3335	B2	7109	B1		
3115	A1	3336	B3	7110	C2		
3116	B2	3337	B3	7111	C2		

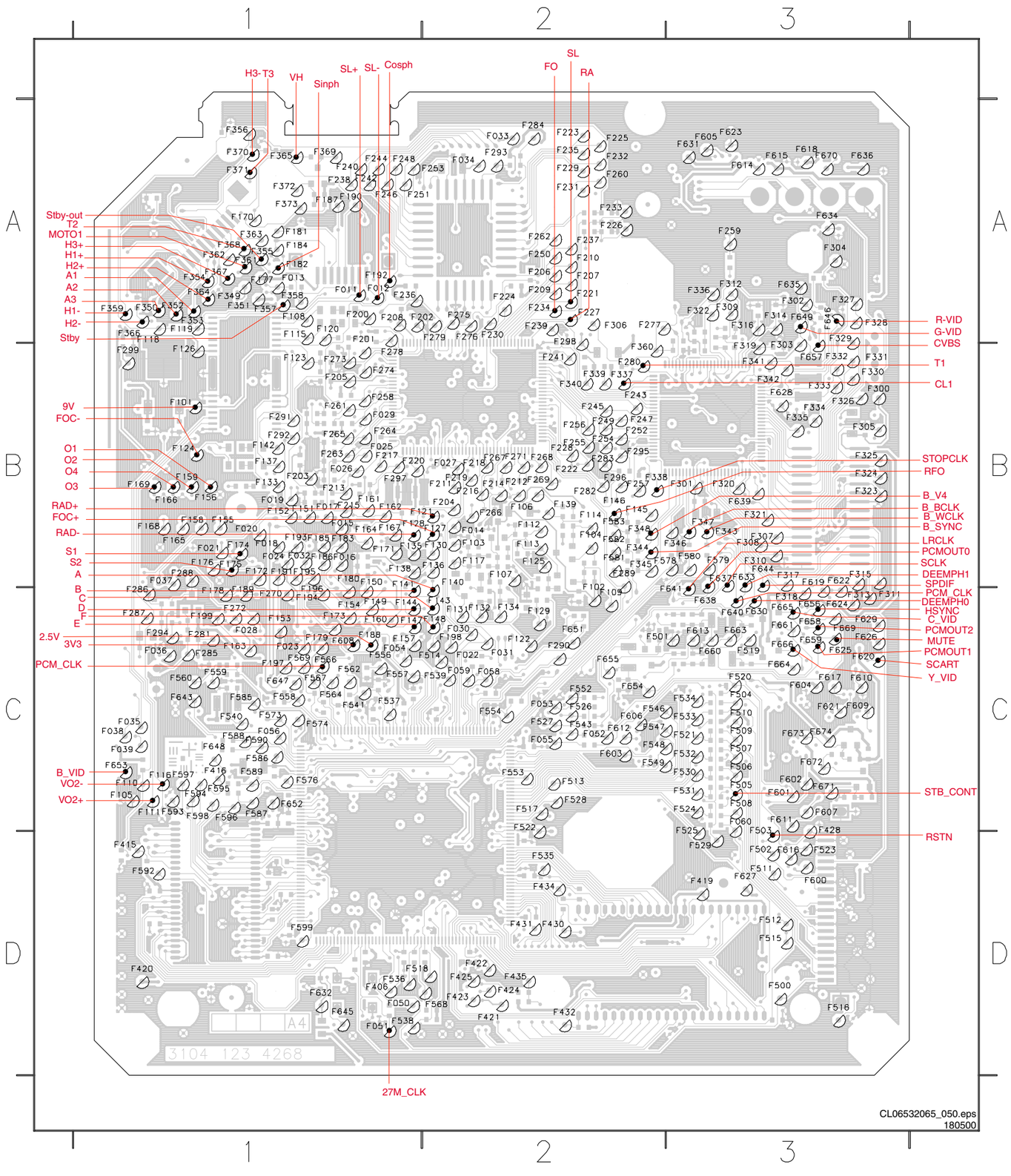
Detailed Bottom view 1



Detailed Bottom view 2



Testpoint overview



F011	A1	F151	B1	F240	A1	F329	A3	F528	C2	F633	B3
F012	A1	F152	B1	F241	B2	F330	B3	F529	D3	F634	A3
F013	A1	F153	C1	F242	A1	F331	B3	F530	C3	F635	A3
F014	B2	F154	C1	F243	B2	F332	B3	F531	C3	F636	A3
F015	B1	F155	B1	F244	A1	F333	B3	F532	C3	F637	B3
F016	B1	F156	B1	F245	B2	F334	B3	F533	C3	F638	C3
F017	B1	F157	C1	F246	A1	F335	B3	F534	C3	F639	B3
F018	B1	F158	B1	F247	B2	F336	A3	F535	D2	F640	C3
F019	B1	F159	B1	F248	A1	F337	B2	F536	D1	F641	C3
F020	B1	F160	C1	F249	B2	F338	B2	F537	C1	F643	C1
F021	B1	F161	B1	F250	A2	F339	B2	F538	D1	F644	B3
F022	C2	F162	B1	F251	A1	F340	B2	F539	C2	F645	D1
F023	C1	F163	C1	F252	B2	F341	B3	F540	C1	F646	A3
F024	B1	F164	B1	F253	A2	F342	B3	F541	C1	F647	C1
F025	B1	F165	B1	F254	B2	F343	B3	F543	C2	F648	C1
F026	B1	F166	B1	F255	B2	F344	B2	F546	C2	F649	A3
F027	B2	F167	B1	F256	B2	F345	B2	F547	C2	F651	C2
F028	C1	F168	B1	F257	B2	F346	B3	F548	C2	F652	C1
F029	B1	F169	B1	F258	B1	F347	B3	F549	C2	F653	C1
F030	C2	F170	A1	F259	A3	F348	B2	F552	C2	F654	C2
F031	C2	F171	B1	F260	A2	F349	A1	F553	C2	F655	C2
F032	B1	F172	B1	F261	B1	F350	A1	F554	C2	F656	C3
F033	A2	F173	C1	F262	A2	F351	A1	F556	C1	F657	B3
F034	A2	F174	B1	F263	B1	F352	A1	F557	C1	F658	C3
F035	C1	F175	B1	F264	B1	F353	A1	F558	C1	F659	C3
F036	C1	F176	B1	F265	B1	F354	A1	F559	C1	F660	C3
F037	B1	F177	A1	F266	B2	F355	A1	F560	C1	F661	C3
F038	C1	F178	C1	F267	B2	F356	A1	F562	C1	F663	C3
F039	C1	F179	C1	F268	B2	F357	A1	F564	C1	F664	C3
F050	D1	F180	B1	F269	B2	F358	A1	F566	C1	F665	C3
F051	D1	F181	A1	F270	C1	F359	A1	F567	C1	F666	C3
F052	C2	F182	A1	F271	B2	F360	B2	F568	D2	F669	C3
F053	C2	F183	B1	F272	C1	F361	A1	F569	C1	F670	A3
F054	C1	F184	A1	F273	B1	F362	A1	F573	C1	F671	C3
F055	C2	F185	B1	F274	B1	F363	A1	F574	C1	F672	C3
F056	C1	F186	B1	F275	A2	F364	A1	F576	C1	F673	C3
F058	C2	F187	A1	F276	A2	F365	A1	F578	B2	F674	C3
F059	C2	F188	C1	F277	A2	F366	A1	F579	B3		
F060	C3	F189	C1	F278	B1	F367	A1	F580	B3		
F101	B1	F190	A1	F279	A2	F368	A1	F581	B2		
F102	B2	F191	B1	F280	B2	F369	A1	F582	B2		
F103	B2	F192	A1	F281	C1	F370	A1	F583	B2		
F104	B2	F193	B1	F282	B2	F371	A1	F585	C1		
F105	C1	F194	C1	F283	B2	F372	A1	F586	C1		
F106	B2	F195	B1	F284	A2	F373	A1	F587	C1		
F107	B2	F196	B1	F285	C1	F406	D1	F588	C1		
F108	A1	F197	C1	F286	C1	F415	D1	F589	C1		
F109	C2	F198	C2	F287	C1	F416	C1	F590	C1		
F110	C1	F199	C1	F288	B1	F419	D3	F592	D1		
F111	C1	F200	A1	F289	B2	F420	D1	F593	C1		
F112	B2	F201	A1	F290	C2	F421	D2	F594	C1		
F113	B2	F202	A2	F291	B1	F422	D2	F595	C1		
F114	B2	F203	B1	F292	B1	F423	D2	F596	C1		
F115	A1	F204	B2	F293	A2	F424	D2	F597	C1		
F116	C1	F205	B1	F294	C1	F425	D2	F598	C1		
F117	B2	F206	A2	F295	B2	F428	C3	F599	D1		
F118	A1	F207	A2	F296	B2	F430	D2	F600	D3		
F119	A1	F208	A1	F297	B1	F431	D2	F601	C3		
F120	A1	F209	A2	F298	A2	F432	D2	F602	C3		
F121	B1	F210	A2	F299	B1	F434	D2	F603	C2		
F122	C2	F211	B2	F300	B3	F435	D2	F604	C3		
F123	B1	F212	B2	F301	B3	F500	D3	F605	A3		
F124	B1	F213	B1	F302	A3	F501	C2	F606	C2		
F125	B2	F214	B2	F303	B3	F502	D3	F607	C3		
F126	B1	F215	B1	F304	A3	F503	C3	F608	C1		
F127	B2	F216	B2	F305	B3	F504	C3	F609	C3		
F128	B1	F217	B1	F306	A2	F505	C3	F610	C3		
F129	C2	F218	B2	F307	B3	F506	C3	F611	C3		
F130	B2	F219	B2	F308	B3	F507	C3	F612	C2		
F131	C2	F220	B1	F309	A3	F508	C3	F613	C3		
F132	C2	F221	A2	F310	B3	F509	C3	F614	A3		
F133	B1	F222	B2	F311	C3	F510	C3	F615	A3		
F134	C2	F223	A2	F312	A3	F511	D3	F616	D3		
F135	B1	F224	A2	F313	C3	F512	D3	F617	C3		
F136	B2	F225	A2	F314	A3	F513	C2	F618	A3		
F137	B1	F226	A2	F315	B3	F514	C2	F619	B3		
F138	B1	F227	A2	F316	A3	F515	D3	F620	C3		
F139	B2	F228	B2	F317	B3	F516	D3	F621	C3		
F140	B2	F229	A2	F318	C3	F517	C2	F622	B3		
F141	B1	F230	A2	F319	B3	F518	D1	F623	A3		
F142	B1	F231	A2	F320	B3	F519	C3	F624	C3		
F143	C2	F232	A2	F321	B3	F520	C3	F625	C3		
F144	C1	F233	A2	F322	A3	F521	C3	F626	C3		
F145	B2	F234	A2	F323	B3	F522	C2	F627	D3		
F146	B2	F235	A2	F324	B3	F523	D3	F628	B3		
F147	C1	F236	A1	F325	B3	F524	C3	F629	C3		
F148	C2	F237	A2	F326	B3	F525	C3	F630	C3		
F149	C1	F238	A1	F327	A3	F526	C2	F631	A3		
F150	B1	F239	A2	F328	A3	F527	C2	F632	D1		

Personal notes:

Personal notes:

8. Alignments

No alignments available

9. IC Descriptions.

9.1 SAA7399 (MACE2) General.

Mace2 is a name used for the successor of the ACE1 IC. The term MACE (mini-ACE) is used because MACE2 does not have a decoder on board. Application area's: Mainly CD-R(W) and prototyping of DVD(-ROM) or high speed CD-ROM.
Functions implemented on-board of MACE2:
A further improved digital servo module. Derived from the ACE1 servo module, but with improvements (make the input switchable between diode signal and error signal processing, improved brake).
The 80C51 micro-controller with external ROM.
The OPC. Optimum Power calibration, used for CDR.
The PCS. Position Control Sledge. A way to speed up sledge movement using hall sensors.

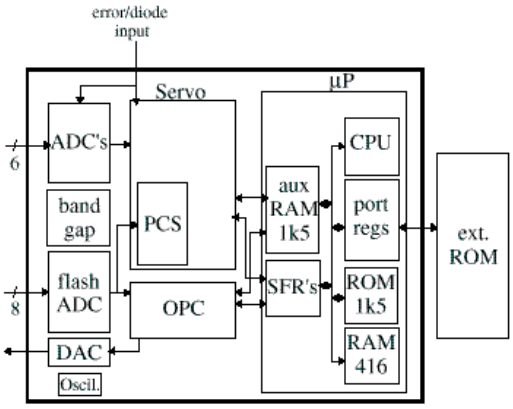


Figure 9-1 Overall block diagram MACE2.

9.2 Features

- Focus and Radial servo loop.
- Built-in access procedure.
- Selectable servo error or servo diode inputs.
- Focus noise performance equivalent to DSICS
- Automatic closed loop gain control available for focus and radial loops
- High speed track crossing velocity measurement > 350 kHz.
- Fast Radial Brake circuitry.
- Sledge motor servo loop, with pulsed sledge support and PCS
- Incorporated micro-controller equivalent to 80C51 --> 66MHz.
- Programmable wait state controller.
- Two embedded RAM's of 416 bytes and 1.5 kB res.
- Optimum Power Calibration Hardware support up to write at N=8.
- Debug facilities.
- Memory mapped interface to sub-modules.
- Programmable clock multiplier.
- 8 Multipurpose I/O lines.
- 5 external interrupt lines.
- External Flash ROM support.
- Sledge stepper motor support.

9.3 The Digital Servo block.

In a CD system, there are some 12 control loops active. About six of them are needed to adjust the servo error signals, that is once per disc rotation offsets, signal amplitudes and loop gains (AGC's) are adjusted to enlarge system robustness and to avoid expensive potentiometer adjustments in production. The other six loops determine the laser spot position on the disc in the radial, axial (focus) and tangential directions. The servo in MACE2 takes care of these controls.
The servo inside Mace2 also has to take care that the spot accesses a required position as fast as possible. This access system consists of two parts, namely the actuator and the sled, which are within a certain range, mechanically and electrically independent. So during an access the servo has to control as well the actuator as the sled.

9.4 Functional description servo

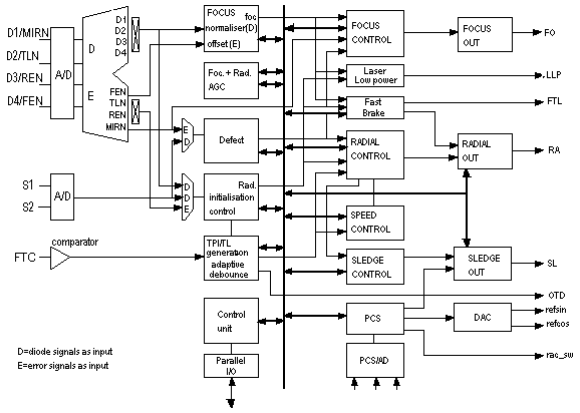


Figure 9-2 Mace2 servo block diagram.

The following functions can be distinguished:
– A to D conversion: a direct AD-conversion of the diode/ error currents.
– Pulse density D to A conversion: Noise shaper output stages.
– Control unit: Provides mainly the communication and on/ off functions.
– Focus normaliser: A partial division of focus and sum signal. Special saturating provisions are included when dividing through very small numbers.
– Initialisation control: Includes the radial normaliser, automatic radial offset compensation and level initialisation for the Track Position Indicator (TPI) for both diode and error input signals.
– TPI/TL generation and adaptive debounce: Generates Track loss (TL) which is protected against disc defects. The TL is made out of the unprotected TPI signal. The debouncer (with improved debounce times) minimises the disturbing effect of HF on the TL and Rp crossovers for the track count circuitry.

- Defect detector: Holds the focus and/or radial control signal on disc dropouts.
- Speed control: Used during access. With radial actuator feed forward.
- Focus control: PID controller with wide range adjustable characteristics.
- Radial control: PID controller with wide range adjustable characteristics.
- Sledge control: PID controller with wide range adjustable characteristics and a pulsed sledge controller.
- Laser Low Power: Switches the laser from write back to read power whenever the device tends to go off-track.

9.5 Input circuits servo

Five out of six of the MACE2 servo inputs can be switched between diode current inputs (for audio and data application) and error signal inputs (for recordable applications).
The analogue signals from the diode pre processor are converted into a digital representation using A/D converters.

9.6 Focus control.

9.6.1 Focus start-up.

To bring the actuator in focus position a triangular shaped voltage is applied to the actuator to perform a search movement. When the lens moves from or to the disc, CA (central aperture) is monitored to reach a certain programmable absolute level. When this value is CA level is reached, the FOK signal becomes true and FEn is passed to the FEn level detector.
At the moment this FEn level is reached the wait for the focus mode is entered and the focus control loop is enabled to detect a sign inversion in the FEn signal.
When this zero crossing in this FEn signal is detected, the loop is closed to function as PID controlled loop and is switched to the PID mode.
During focus start-up a dither signal is added to the output signal of the integrator. It prevents the actuator from hitting its natural resonance. With this technique quantisation, effects are compensated for during start-up.

9.6.2 Focus Position Control loop.

The focus control loop contains a digital PID controller that has 5 parameters available to the user. These coefficients influence the integrating, proportional and differential action of this PID and a digital low pass filter following the PID. The fifth coefficient influences the loop gain.

9.6.3 Dropout detection.

This detector can be influenced by one parameter. The FOK signal will become false and the integrator of the PID will hold if the CA signal drops below this programmable absolute CA level. When the FOK signal becomes false, it is assumed as caused by a black dot in the first place.

9.6.4 Focus Loss detection and Fast restart.

Whenever FOK is false longer than about 2 ms, it is assumed that the focus point is lost. A fast restart procedure is initiated which is capable of restarting the focus loop within 200 to 300 ms depending on the uP-programmed coefficients.

9.6.5 Focus Automatic Gain Control loop.

The loop gain of the focus control loop can be corrected automatically to eliminate tolerances in the focus loop. This gain control injects a signal into the loop that is used to correct the loop gain. Since this decreases the optimal performance, the gain control should only activated shortly (for instance when starting a new disc).

9.7 Radial control.

The MACE2 digital controller includes the following radial servo functions:

9.7.1 Level initialisation:

During start-up an automatic adjustment procedure is activated to set the values of the radial error gain, offset and satellite sum/MIRN signal gain for TPI level generation. The initialisation procedure runs in a radial open loop situation and is < 200 ms. This start-up time period may coincide with the last part of the turntable motor start-up time period.

9.7.2 Automatic gain adjustment:

Because of this initialisation the amplitude of the RE signal is adjusted within _10% around the nominal RE amplitude. Offset adjustment: The additional offset in RE due to the limited accuracy of the start-up procedure is less than +/- 50nm.

9.7.3 TPI level generation:

The accuracy of the initialisation procedure is such that the duty cycle range of TPI becomes 0.4 < duty cycle < 0.6.

Sledge home:
Sledge moves to reference position at the inner side of the disc with user defined voltage.

Tracking control:
The actuator is controlled using a PID loop filter with user defined coefficients.

Access:
In Mace2 there are two fundamentally different ways to perform an access:

Using the PCS
A more detailed description of this access method is given in an other section.

Using the servo controlled access:
The way it was done in the predecessors of Mace2.This access procedure is divided into 3 different modes, depending on the requested jump size:
access type size access speed
Actuator jump decreasing velocity
Sledge jump maximum power to sledge 1
Controlled sl. jump controlled brake power
The access procedure makes use of a track counting mechanism, a velocity signal based upon the number of tracks passed within a fixed time interval, a velocity setpoint calculated from the number of tracks to go and a user programmable parameter indicating the maximum sledge performance.
If the number of tracks to jump is too large, then the Sledge jump mode is activated, else the actuator jump is performed. The requested jump size together with the required sledge braking distance at maximum access speed defines the value of the maximum numbers of tracks.
During the actuator jump mode, velocity control with a PI controller is used for the actuator. The sledge is then continuously controlled using the filtered value of the integrator contents of the actuator. All filter parameters (for actuator and sledge) are user programmable.

In the sledge jump mode maximum power (user programmable) is applied to the sledge in the correct direction, while the actuator becomes idle.

Radial Automatic Gain Control loop:
The loop gain of the radial control loop can be corrected automatically to eliminate tolerances in the radial loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimal performance the gain control should only be activated shortly (for instance when starting a new disc). This gain control differs from the earlier mentioned level initialisation. This level initialisation should be done first. The level initialisation without the gain control reduces tolerances from the front-end only.

9.8 The radial PID.

Since we are dealing with a big variety of applications and drives, the servo controllers in MACE2 should be adjustable within a large frequency range.
In order to read out the track properly -a track consists of sequential ordered data pit's which hold audio, video or ROM data - the focus and radial position controls must follow the moving track within some tenths of a micrometer, despite of disc imperfections and external disturbances.
For instance, a rotating disc causes, due to track eccentricity, track unroundness, or disc skew, track movements up to some millimetres. The control loop reduces this to about one tenth of a micrometer.

9.9 Initialisation control.

Due to optical, electrical and mechanical tolerances in CD players, properties of the servo signals such as offset and gain can vary. In general, without proper signal processing, a simple PID controller function cannot cope with this relatively large offset and gain spreads. Therefore, gain and offset adjustments during manufacture or active control, to compensate for these signal imperfections, become inevitable.
Adjustment procedures in the factory are expensive. So, automatic adjustment procedures have been implemented in order to avoid most of the potentiometer adjustments. In the MACE2 servo automatic adjustments are applied to the radial error signal only.

9.10 The AGC.

The Automatic Gain Control is used in the MACE2 digital servo to adjust the radial and focus bandwidths to a nominal value. Injecting a signal in the loop and measuring the phase of its resulting signal (wobble method) does this.
Principle of the Automatic Gain Control.
The principle of the Automatic Gain Control (AGC) circuit, as used in MACE2, is drawn in the next figure.

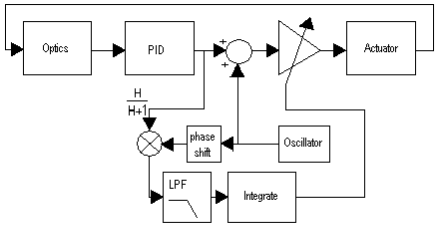


Figure 9-3 Principle of the automatic gain control.

A sine wave signal with a certain frequency is injected in the control loop at the summation point. The resulting signal is measured before the injection point. The injected signal is shaped by H/1+H . This measured signal is multiplied by a phase shifted version of the injected signal. The result of the multiplication is low pass filtered and integrated. (The integrator is started at the nominal gain of the control loop). The result of the integration is fed to the adjustable loop gain. This principle, synchronous detection, is also known as 'wobble method'.

9.11 The Fast brake.

The fast brake is an aid to speed up radial capture after a high-speed jump. It is a separate radial control with a much higher bandwidth. The radial control output can be switched between fast brake mode and original radial control mode. The fast brake helps the radial actuator at the end of a jump to "stick" to the right track. In fast brake mode, the actuator starts to follow the track movements. It's a bit like jumping on a moving train. If you run as fast as the train, you can just step in. After a radial open loop jump the tracks are moving (as a result of eccentricity) at a very high speed underneath the radial actuator. This speed is too high for a normal radial control loop to do radial capture. When the radial control is switched over to fast brake mode for a short term, this moving of the tracks underneath the actuator becomes much slower, (because the actuator follows the track movement), so when you switch back to original radial control, it's much easier to do radial capture.

9.12 The Defect Detector.

Because of the possible earlier mentioned defects (fingerprints, etc) a defect detection circuit is incorporated into the MACE2 servo. If a defect is detected, the radial and focus error signals may be zeroed, resulting in better playability.

9.12.1 Operation:

The defect detector prevents the light spot from going out of focus and going off track due to disc dropout excitations. The defect detector can be switched on and off under software control and can be applied to the focus control only, or both to the focus and radial control.
Whenever this circuit detects a defect, it will hold all radial and focus controls.
The hold signal is generated whenever the reflected light intensity drops rapidly (< 1:5 ms) down to roughly 75% of the actual intensity level. In that case the output of the comparator becomes active and controls the focus and radial signal switch.
This circuit improves the playability of the application (black dot performance, etc) and is programmable to optimise it for specific disc defects. The actions of this circuit can be monitored on the DEFO pin (active high).
An external defect detection circuit can be added by removing the connection between DEFO and DEFI (normal operation) and inserting the external circuitry.
These signals are afflicted with some uncertainties caused by:

- Disc defects like scratches and fingerprints
- The HF information on the disc, which is considered as noise by the detector signals.

9.13 Laser Drive On.

The LDON pin is used to switch the laser drive off and on. It is an open drain output. In case the laser is on, the output has a high impedance. The pin will be automatically driven if the focus control loop is switched on.

9.14 Laser Low Power (LLP).

The LLP output can be used by write-able systems to switch the laser back to read power when the light spot goes off-track while writing discs. To prevent that the neighbour tracks are damaged when the spot goes off-track the laser has to be switched very fast to the safe read power. The laser is not switched off (like LDON does), so the system can carry on reading.
The tracking (radial) and focus error signals are used to disable the laser write power. This is done through the LLPn, active low Laser Low Power, signal. Note that LLPn is a servo output, which is inverted before it is output via the LLP pin, so the LLP pin is active high.
So, if any of the following conditions is true, the laser write power is disabled by the MACE2 servo.

- Off Track, more than a quarter off a track away from the correct one
- ORD, radial error signal too large. Larger than the given setpoint, which should be chosen at a critical write failure level. An adjustable band pass filter first processes the radial error signal.
- OFD, focus error signal too large. Larger than the given setpoint, which should also be chosen with care. An adjustable band pass filter also first processes the focus error signal. All settings of the focus and radial part are independent.
- OTR, prot stat flag which becomes active if ORD becomes active during an actual laser write (LWR) action. This flag is reset only by a status read (RSTAT) command. So until then LLPN stays active.
- OFO, prot stat flag that becomes active if OFD becomes active during an actual laser write action. Same idea as OTR.

This error detection circuit can be switched off (apart from the Off Track detection) by raising the setpoint levels to its maximum value.

9.15 The OPC.

The OPC block in Mace2 is used for the following functions:

- During write actions, it stores Pw samples, which can be evaluated by the microprocessor.
- During OPC read actions, it stores A1, A2 and CALF samples, which are used for calculating the asymmetry and the modulation index.
- The OPC block is used for EFM detection.
- During reading of a disc, it stores A1 and CALF samples, which can be monitored.

Although the OPC block is used for multiple functions, it got it's name from the OPC procedure, which is it's main task.
The OPC (Optimum Power Calibration) procedure is used in CD-R/CD-RW/DVD-RAM applications. It is used to "calibrate" the laser write power in writable systems.
It reads in 3 analogue signals from an analogue pre-processor like AEGER-2 (A1, A2, and CALF) and the actual write power (Pw) from the laser controller and feeds an analogue output signal Alpha0 back to AEGER-2. A1, A2 and CALF represent the max, min and average value of the EFM signal respectively. Alpha0 controls the laser write power. All analogue signals are converted to an 8 bit digital signal. Conversion frequency at 16.9MHz base clock is 88kHz (each channel).

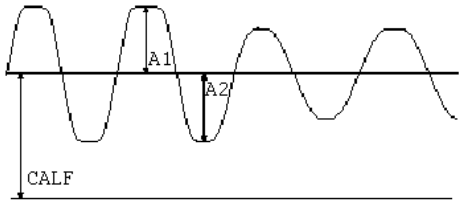


Figure 9-4 Definition of the A1, A2 and CALF signals.

9.16 Definition of terms.

The asymmetry (and modulation index m of the EFM signal are calculated from the analogue inputs:

$$\beta = \frac{A1 - A2}{A1 + A2}$$

$$m = \frac{A1 + A2}{A1 + CALF}$$

9.17 Rough description of the OPC procedure

Basically the OPC procedure tries to find out the optimum laser power to be used on a specific disc. The OPC procedure uses about 15 ATIP frames. These frames are located in the "PCA" area. This is a special part of the disc used only for power calibration. The drive first checks whether there are 15 frames "empty" in the PCA. Next the OPC is performed in these 15 frames.
The OPC operation consists of two stages: A "write" and a "read" stage. First 15 ATIP frames are written (during which the OPC block stores Pw samples), and then the same 15 ATIP frames are read back again, (during which the OPC block stores A1, A2 and CALF samples). During the write stage, random EFMis written in a test area located on the inner side of the disc. During this recording the write power is increased stepwise from a low to a high power level.

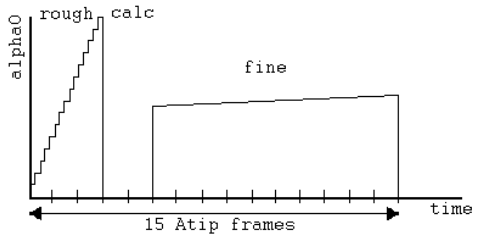


Figure 9-5 Figure 5: OPC write profile.

First during 3 ATIP frames the power is increased in rather big steps (rough OPC). During this action Pw samples are stored into memory. During the rough OPC, the OPC makes 7 steps per ATIP frame. This gives 21 samples into the OPC memory. From these samples, the microprocessor can calculate what's roughly the best alpha0 setting for this typical disc.
After 2 frames of calculations, another 10 ATIP frames are written using smaller steps (fine OPC) around the alpha0 setting, which gave the best result during the rough OPC.
The second stage of the OPC procedure is the "read" phase

in which the pattern recorded in the previous stage is read back.
During this read phase the OPC block stores A1, A2 and CALF samples from exact the same location where during the OPC write phase the Pw samples where stored. The samples for A1, A2, CALF and Pw are listed side by side into memory. After the read back phase the processor calculates at which setting of alpha0 the least jitter is encountered. This setting will be used to write the disc with.

9.18 The OPC top level.

The OPC block as a whole has 5 possible modes:
- Recording mode: This can be either OPC writing (writing EFM test patterns to disc and Alpha0 stepping) or standard write mode (i.e. alpha0 is constant).
- OPC reading: Reading back OPC test patterns from disc.
- Normal read mode: detects the presence of EFM.
- DVD read mode: used for DVD-RAM experiments.
- EFMD only mode: no data being written to the AUX RAM, but the EFM detector and the PW monitor still running. Contents of the QUX RAM remain unchanged.

All actions in the OPC hardware are synchronised to the ATIP frame sync, which can be either generated internally or received from the encoder/decoder during writing. The microprocessor writes data asynchronously to the OPC hardware. The OPC block synchronises this data to the sync either internally generated, or obtained from CDR60.

9.19 The Analogue to Digital converter.

The analogue to digital converter of the OPC is shared with the ADC required by the PCS.

9.20 The digital input filters.

The combined ADC for the OPC and the PCS delivers a multiplexed stream of 8 bit words. A sequential low-pass filter filters this multiplexed stream. The 4 analogue multiplexed input signals from the OPC (A1, A2, CALF and Pw) are filtered by 4 identical LPF's. (One for each channel). This filters can be adapted to various speeds by changing the subsampling factor (i.e. the sample rate of the filter), the cut off frequency scales with the sample frequency. The sample frequency of the filter is equivalent to the OPC timebase frequency, which is the output of the pre-scaler.

9.21 OPC demux.

The OPC demux block demultiplexes the stream supplied by the LPF. This same block also changes the format of the digital data from signed (representation inside the filter) to unsigned (representation in the rest of the OPC). The demultiplexing process introduces one baseclock delay.

9.22 The sequencer.

The OPC sequencer controls the timing of all the hardware actions in the OPC hardware. It generates the OPC timebase and locks it to the ATIP pulse. A programmable pre-scaler generates the OPC timebase.
Dividing the ADC sample clock by 8 derives the input clock of this pre-scaler. (= Identical to the sample rate per channel). The pre-scaler can divide this clock by a number in the range from 1-16. The division factor can be programmed via the OPC ctrl register. The OPC timebase is locked to the selected ATIP source, which can be either an external ATI P sync or an internally generated sync. (Programmable). The OPC timebase clock supplies the sample frequency for the input LPF's, the OPC pre-processor and the EFM detector.
The sequencer controls the timing of all the hardware actions in the OPC hardware. The sequencer is started either by an external ATIP sync or an internally generated sync (programmable).
All data acquisition and alpha0 settings change synchronised to this sync signal (rising edge of the ATIP sync). An exception on this is the switching of the ATIP input itself, which is immediately changed whenever the bit in the OPC ctrl register is changed. When this was latched on the ATIP source itself, it would create a deadlock when there was no ATIPin from CDR-60.

9.23 The Pw monitor

The Pw monitor is used during the "OPC write" and normal write mode. The comparator compares the incoming Pw with two programmable thresholds PW MAX and PW MIN. Both these thresholds can be programmed via the OPC PW register, which contains 4 bits for each threshold.
Internally both 4-bit thresholds PW MAX and PW MIN are extended to 8 bit values. The compare function performs an unsigned compare.
The first threshold is used to detect fingerprints. The second is used to check the correct operation of the laser driver.

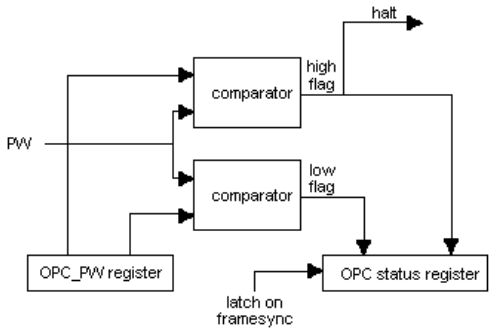


Figure 9-6 OPC PW monitor.

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply

TZA1033

FEATURES

- Operates with DVD-ROM,DVD-RAM, DVD+RW, DVD-RW, CD-ROM and CD-RW media
- Operates up to 64x CD-ROM and 8x DVD-ROM
- Support for Dual Light pen DVD systems (DVD/CDRW)
- DVD-RAM (C) playback capability
- DVD-RAM Land-Groove servo polarity switching
- 3 different tracking servo strategies:
  Conventional 3 beam tracking for CD
  Differential Phase Detection (DPD) for DVD-ROM (including option to emulate traditional drop out detection; drop out concealment)
  Advanced Push Pull with dynamic offset compensation for DVD-RAM (recorded and unrecorded areas)
- Radial error signal for fast track counting (FTC)
- 2 different strategies to read header data:
  - Full bandwidth Push Pull signal
  - Left and Right side signal
- Universal photo diode IC interface using internal conversion resistors and offset cancelation
- Flexible adaption to different light pen configurations
- Input buffer amplifiers with low-pass filtering
- RF data amplifier with wide (programmable) bandwidth equivalent to 64xCD / 8x DVD when using equaliser function
- Built-in equalisers cover CAV inner-outer disc range at highest speed.
- Programmable RF gain for DVD-ROM / DVD-RAM / CD-RW / CDROM applications(approx 50dB range)
- Balanced RF-Data signal transfer (single ended still supported)
- Fully automatic laser control including stabilization and an ON/OFF switch, plus a separate supplypin for power efficiency
- Automatic monitor diode polarity selection.
- 3 and 5 V compatible digital interface
- Enhanced signal conditioning in DPD circuit for optimal tracking performance under noisy conditions.

GENERAL DESCRIPTION

The DVDALAS2 is an analogue preprocessor and laser supply circuit for DVD / CD read only players. The device contains data amplifiers, several options for radial tracking and focus control. The preamplifier forms a versatile, programmable interface between dual, voltage output CD/DVD mechanisms to Philips' digital signal processor family for CD and DVD (Gecko, HDR65, Iguano, etc..)

The device contains serval options for radial tracking:
Conventional 3 beam tracking for CD;
Differential Phase Detector (DPD) for DVD;
Push Pull for DVD-RAM with flexible L/R weighing to compensate dynamic offsets e.g. beamlanding offset.
A radial error signal is generated to allow fast track count (FTC) during track jumps.

The dynamic range of this preamp/processor combination can be optimized for the LF servo and RF data paths. The gain in both channels can be programmed separately. This will guarantee an optimal playability for all kind of discs.

Several functions are included to allow playback of DVD-RAM(C) discs:

- The header information can be read via the data output path (RF)
- DC offset compensation techniques provide a fast settling after disc errors.
- Radial servo Polarity switch for land/groove
- two settings for focus offset correction for land and groove

The device can accommodate astigmatic, single foucault and double foucault detectors and can be used with P-type lasers with N- or P-sub monitor diodes. After an initial adjustment, the circuit will maintain control over the laser diode current. With an on-chip reference voltage generator, a constant and stabilized output power is ensured independent of ageing. A separate power supply connection allows the internal power dissipation to be reduced by connecting a low voltage supply.

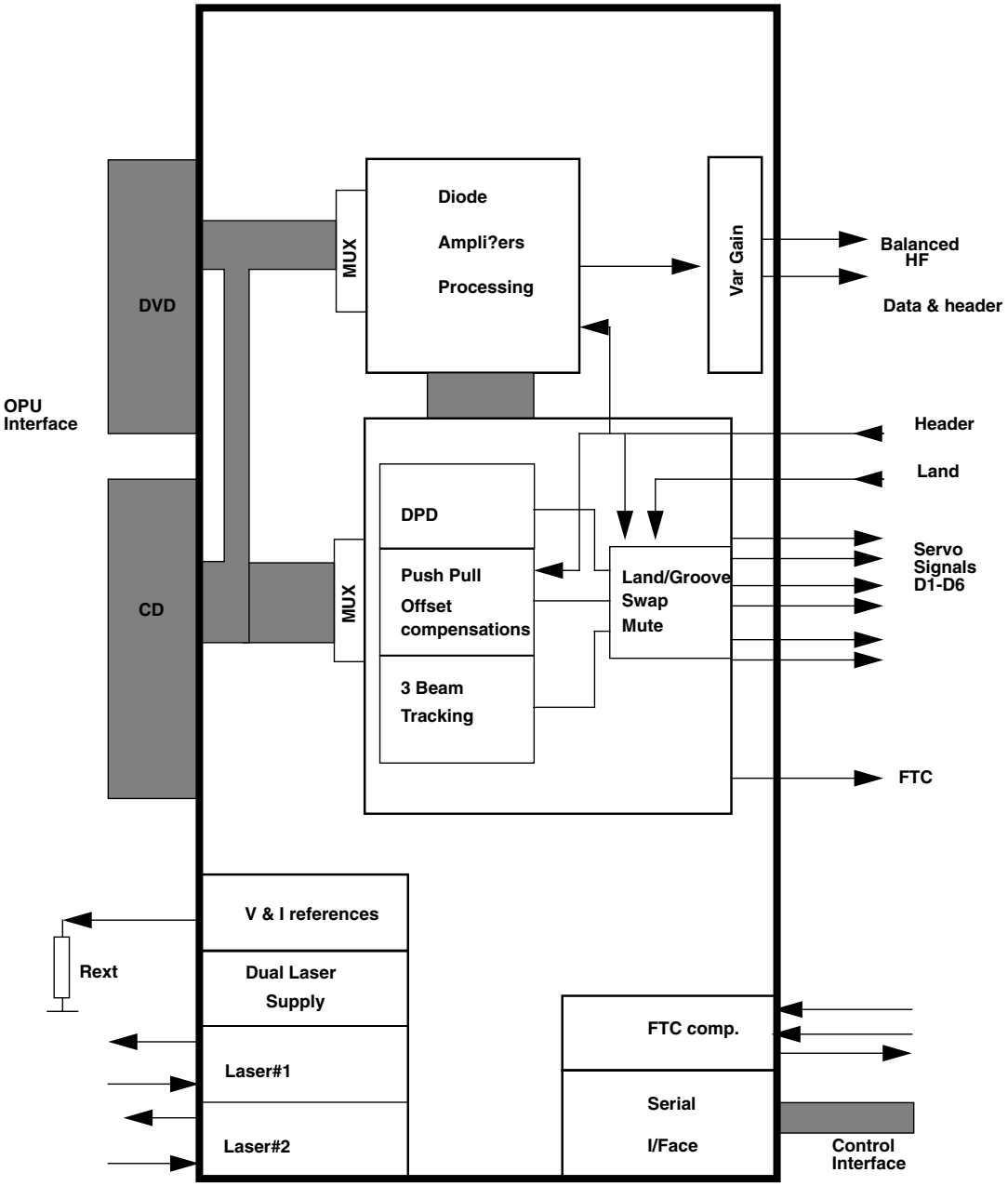
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA1023	LQFP64	Plastic low pro?le QFP64; body 10 x 10 x 1.4 mm	SOT314-2

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply

TZA1033

DEVICE BLOCK DIAGRAM



DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply — TZA1033

PINNING

Name	Pin	Description
CD-A	1	CD pick up input A
CD-B	2	CD pick up input B
CD-C	3	CD pick up input C
CD-D	4	CD pick up input D
CD-REF	5	CD pick up reference voltage
CD-E	6	CD pick up input E
CD-F	7	CD pick up input F
DVD-A	12	DVD pick up input A
DVD-B	13	DVD pick up input B
DVD-C	14	DVD pick up input C
DVD-D	15	DVD pick up input D
DVD-ref	16	DVD pick up reference voltage
O-A	48	Servo current output for Focus-A
O-B	47	Servo current output for Focus-B
O-C	46	Servo current output for Focus-C
O-D	45	Servo current output for Focus-D
O-central	40	Testpin for offset cancelation
TD2	37	Internally connected
FTC-ref	36	Servo output voltage reference input
S1	42	Servo current output for radial tracking
S2	41	Servo current output for radial tracking
TD1	35	Internally connected
FTC	33	Fast track count voltage output
RFP	55	pos. RF output signal
RFN	56	neg. RF output signal
RF-REF	54	DC Reference signal input RF
LPF-DPD1	38	DPD Low pass bandwidth capacitor, channel pos
LPF-DPD2	39	DPD Low passbandwidth capacitor, channel neg
Land	20	Land/groove toggle input
HEADER	21	Header detector window input
CD-MI	62	CD laser monitor input
DVD-MI	10	DVD laser monitor input
CD-LO	61	CD laser output
DVD-LO	64	DVD laser output
COP	27	Positive inputFTC comparator
COM	28	Inverting inputFTC comparator
COO	29	FTC comparator output

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply — TZA1033

Name	Pin	Description
SIDA	23	Serial host interface data input
SICL	24	Serial host interface clock input
SILD	25	Serial host interface load
VDDA1	8	Analog Supply voltage 1 (RF input)
VDDA2	59	Analog Supply voltage 2 (RF internal)
VDDA3	53	Analog Supply voltage 3 (RF output stage)
VDDA4	44	Analog Supply voltage 4 (Servo)
VDDD5	30	Digital Supply voltage (5V dig core)
VDDD3	22	Digital Supply voltage (3V I/O pads and FTC comp.)
VDDL	63	Supply voltage for laser
VSSA1	9	Analog Ground 1
VSSA2	58	Analog Ground 2
VSSA3	57	Analog Ground 3
VSSA4	43	Analog Ground 4
VSSD	26	Digital ground
Rext	60	Reference current input (Connect 12k1 to VSSA4)
STB	31	Standby input
TM	19	Testmode input
TDO	34	test data out

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply

TZA1033

PINNING

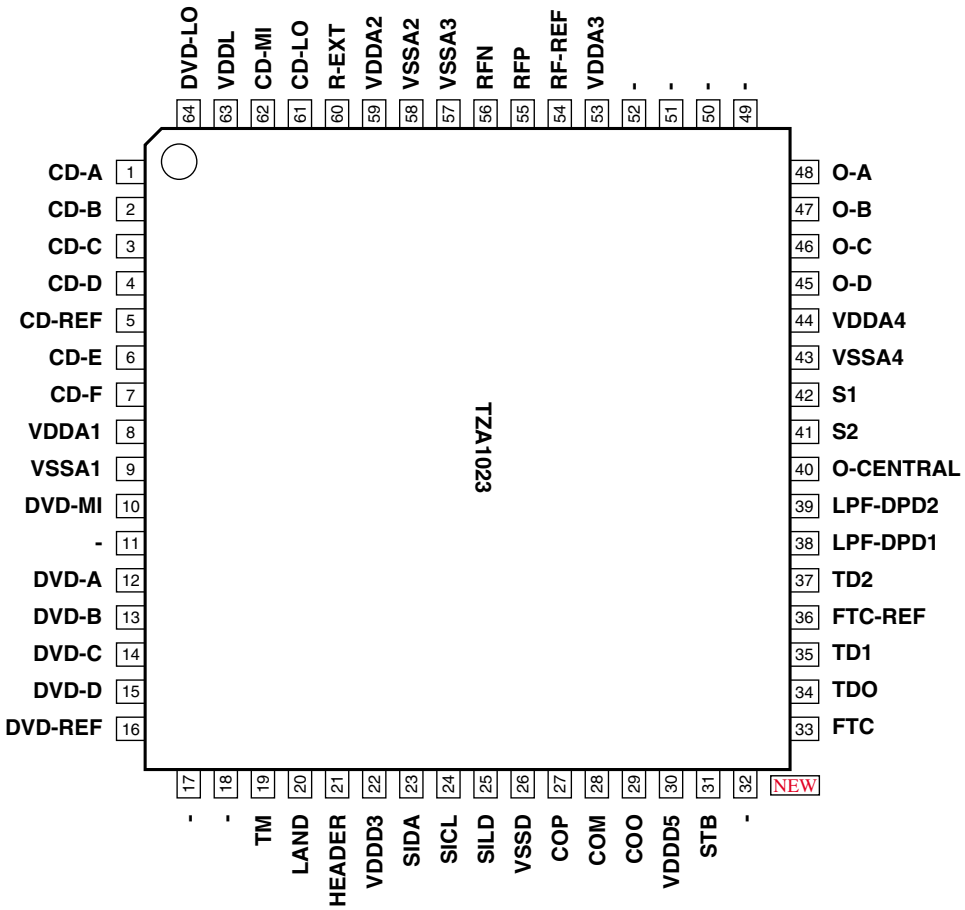


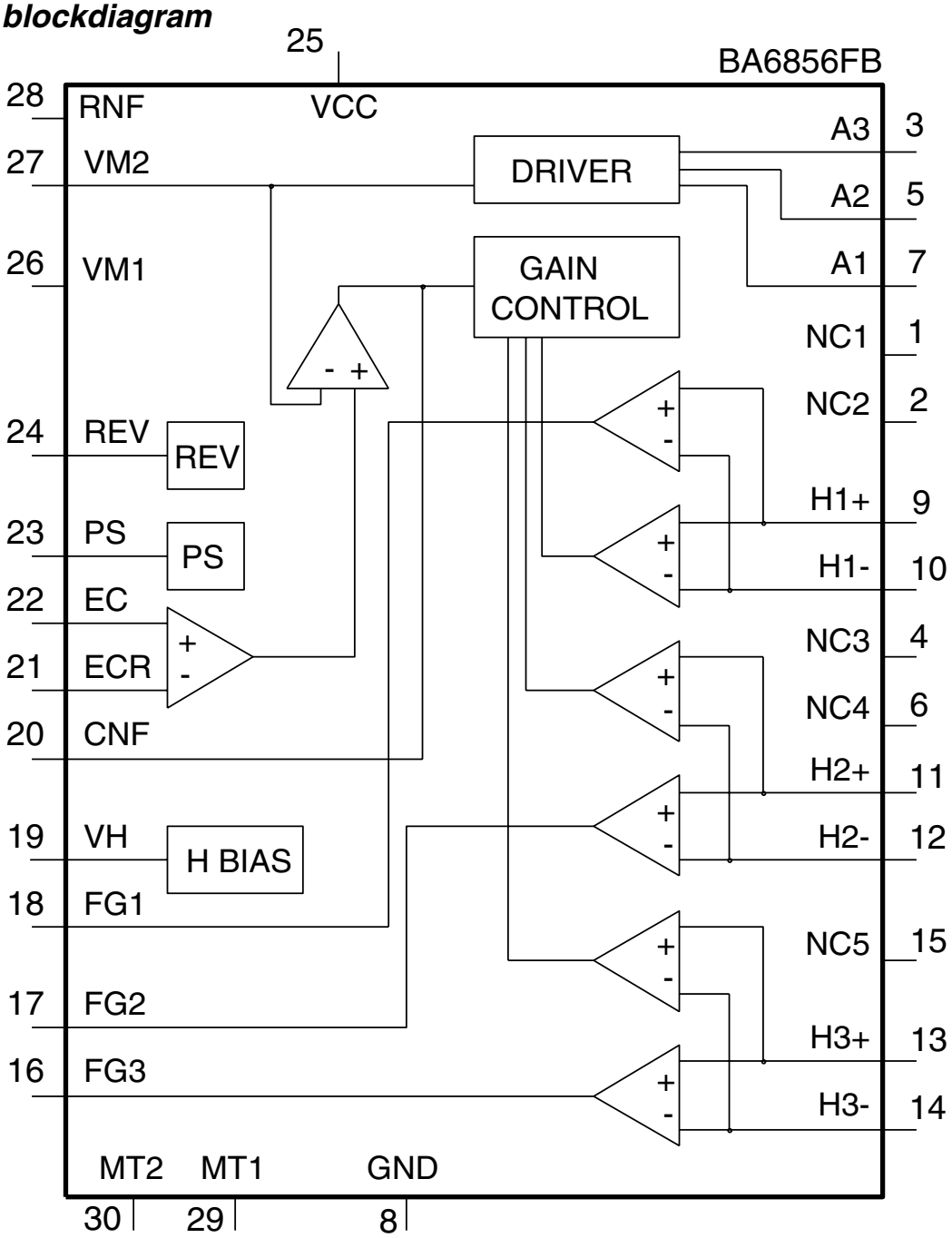
Fig.2 Pin configuration.

BA6856FP: 3 PHASE MOTOR DRIVER FOR DVD PLAYERS

Features

- /3-phase, full-wave pseudo linear driving system
- built-in power save
- built-in therma shut down circuit
- built-in current limit circuit
- built in Hall bias circuit
- built in FG-output (3-phase parallel output)
- with switching function of regular/ reverse rotations

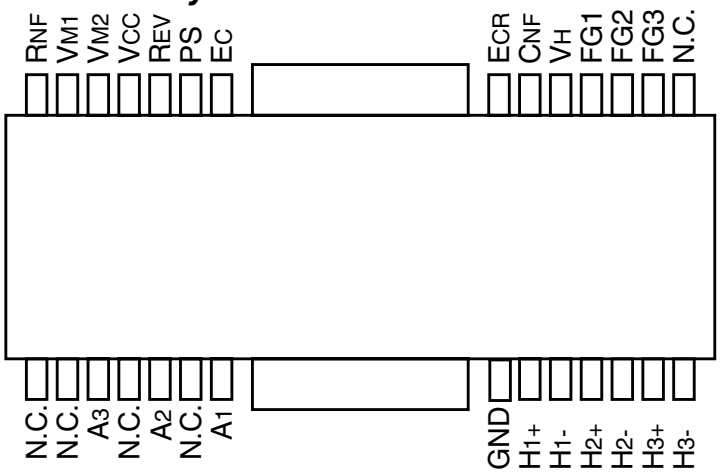
blockdiagram



pin description

PIN No	PIN NAME	DESCRIPTION
1	N.C.	Not connected
2	N.C.	Not connected
3	A_3	Output 3 for motor
4	N.C.	Not connected
5	A_2	Output 2 for motor
6	N.C.	Not connected
7	A_1	Output 1 for motor
8	GND	Ground
9	H_1^+	Hall input Amp1. positive input
10	H_1^-	Hall input Amp1. negative input
11	H_2^+	Hall input Amp2. positive input
12	H_2^-	Hall input Amp2. negative input
13	H_3^+	Hall input Amp3. positive input
14	H_3^-	Hall input Amp3. negative input
15	N.C.	Not connected
16	FG3	FG3 signal output terminal
17	FG2	FG2 signal output terminal
18	FG1	FG1 signal output terminal
19	V_H	Hall Bias
20	C_{NF}	Capacitor connection pin for phase compensation
21	E_{CR}	Torque control standard voltage input terminal
22	E_C	Torque control voltage input terminal
23	PS	POWER SAVE switch
24	R_{EV}	Reverse terminal
25	V_{CC}	Power supply for sinal division
26	V_{M2}	Power supply 2 for driver
27	V_{M1}	Power supply 2 for driver
28	R_{NF}	Power supply for driver division
FIN	FIN	GND

Terminal lay-out



DSP for CD and DVD-ROM systems SAA7335

FEATURES

- Compatibility with CD-I, CD-ROM, MPEG-video DVD-ROM and DVD-video applications
- Designed for very high playback speeds
- Typical CD-ROM operation up to n = 12, DVD-ROM to n = 1.9, maximum rates (tbf)
- Matched filtering, quad-pass error correction (C1-C2-C1-C2), overspeed audio playback function included (up to 3 kbytes buffer)
- Lock-to-disc playback, Constant Angular Velocity (CAV), pseudo-Constant Linear Velocity (CLV) and CLV motor control loops
- Interface to 32 kbytes SRAM for DVD error correction and de-interleave
- Sub-code/ header processing for DVD and CD formats
- Programmable HF equalizer
- In DVD mode it is still compatible with Philips block decoders
- Sub-CPU interface can be parallel or fast I²C-bus
- On-chip clock multiplier.

GENERAL DESCRIPTION

This device is a high-end combined Compact Disc (CD) and Digital Versatile Disc (DVD) compatible decoding device. The device operates with an external 32 kbytes S-RAM memory for de-interleaving operations. The device provides quad-pass error correction for CD-ROM applications (C1-C2-C1-C2) and operates in lock-to-disk, CAV, pseudo CLV and CLV modes.

In DVD modes double-pass C1-C2 error correction is used which is capable of correcting up to 5 C1 frame errors and 16 C2 frame errors.

The SAA7335 contains all the functions required to decode an EFM or EFM+ HF signal directly from the laser pre-amplifier, including analog front-end, PLL data recovery, demodulation and error correction. The spindle motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the motor unit.

The SAA7335 has two independent microcontroller interfaces. The first is a serial I²C-bus and the second is a standard 8-bit multiplexed parallel interface. Both of these interfaces provide access to a total of 32 × 8-bit registers for control and status.

This data sheet contains an descriptive overview of the device together with electrical and timing characteristics. For a detailed description of the device refer to the user guide *"SAU/UM96018"*.

Supply of this CD/DVD IC does not convey an implied license under any patent right to use this IC in any CD or DVD application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDD}	digital supply current	–	70	300	mA
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	70	300	mA
f_{xtal}	crystal input frequency	4	25	tbf	MHz
T_{amb}	operating ambient temperature	−20	–	+70	°C
T_{stg}	storage temperature	−55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7335GP	LQFP100	plastic low pro?le quad ?at package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

BLOCK DIAGRAM

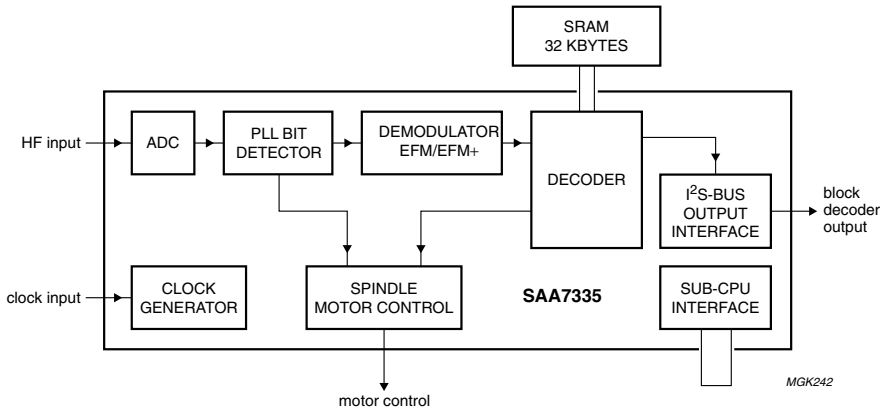


Fig.1 Simplified block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SSA1}	1	supply	analog ground 1
I_{ref}	2	I	analog current reference input for ADC
REFLo	3	I	analog low reference input for ADC
REFHi	4	I	analog high reference input for ADC
VREF	5	I	analog negative input
HFIN	6	I	analog positive input
V_{SSA2}	7	supply	analog ground 2
AGCOUT	8	O	analog test pin output
V_{DDA2}	9	supply	analog supply voltage 2
V_{DDD1}	10	supply	digital supply voltage 1
V_{SSD1}	11	supply	digital ground 1
OTD	12	I	off track detect input
MOTO1	13	O	3-state motor control output
n.c.	14	–	not connected, reserved
MOTO2/T3	15	I/O	motor control output/tachometer 3 input
n.c.	16	–	not connected, reserved
T1	17	I	tachometer 1 input
T2	18	I	tachometer 2 input
V_{DDD2}	19	supply	digital supply voltage 2
V_{SSD2}	20	supply	digital ground 2
TEST1	21	I	test input 1
TEST2	22	I	test input 2
POR	23	I	power-on reset input
MUXSWICH	24	I	use clock multiplier input
n.c.	25	–	not connected, reserved
CL1	26	O	divided clock output
BCAIN	27	I	BCA input
SDA	28	I/O	sub-CPU I^2C-bus serial data input/output
SCL	29	I	sub-CPU I^2C-bus serial clock input
INT	30	O	sub-CPU interrupt output (open-drain)
V_{DDD3}	31	supply	digital supply voltage 3
V_{SSD3}	32	supply	digital ground 3
da7	33	I/O	sub-CPU data bus bit 7 input/output (parallel)
da6	34	I/O	sub-CPU data bus bit 6 input/output (parallel)
da5	35	I/O	sub-CPU data bus bit 5 input/output (parallel)
n.c.	36	–	not connected, reserved
da4	37	I/O	sub-CPU data bus bit 4 input/output (parallel)
n.c.	38	–	not connected, reserved
da3	39	I/O	sub-CPU data bus bit 3 input/output (parallel)
da2	40	I/O	sub-CPU data bus bit 2 input/output (parallel)

SYMBOL	PIN	TYPE	DESCRIPTION
da1	41	I/O	sub-CPU data bus bit 1 input/output (parallel)
n.c.	42	–	not connected, reserved
da0	43	I/O	sub-CPU data bus bit 0 input/output (parallel)
V_{DDD4}	44	supply	digital supply voltage 4
V_{SSD4}	45	supply	digital ground 4
$\overline{WRi}$	46	I	sub-CPU write enable input (active LOW)
$\overline{RDi}$	47	I	sub-CPU read enable input (active LOW)
ALE	48	I	sub-CPU address latch enable input
CSi	49	I	sub-CPU chip select input (active HIGH)
STOPCLOCK	50	O	stop clock output
n.c.	51	–	not connected, reserved
V4	52	O	serial subcode output (for CD)
EBUOUT	53	O	digital audio output
SYNC	54	O	I^2S-bus sector sync output
FLAG	55	O	I^2S-bus correction ?ag output
DATA	56	O	I^2S-bus serial data output
BCLK	57	I/O	I^2S-bus bit serial clock input/output
WCLK	58	I/O	I^2S-bus word clock input/output
V_{DDD5}	59	supply	digital supply voltage 5
V_{SSD5}	60	supply	digital ground 5
RAMRW	61	O	RAM read/write control output
n.c.	62	–	not connected, reserved
RAMDA7	63	I/O	RAM data bus bit 7 input/output
RAMDA6	64	I/O	RAM data bus bit 6 input/output
RAMDA5	65	I/O	RAM data bus bit 5 input/output
RAMDA4	66	I/O	RAM data bus bit 4 input/output
RAMDA3	67	I/O	RAM data bus bit 3 input/output
RAMDA2	68	I/O	RAM data bus bit 2 input/output
n.c.	69	–	not connected, reserved
RAMDA1	70	I/O	RAM data bus bit 1 input/output
RAMDA0	71	I/O	RAM data bus bit 0 input/output
V_{DDD6}	72	supply	digital supply voltage 6
V_{SSD6}	73	supply	digital ground 6
RAMAD0	74	O	RAM address bit 0 output
RAMAD1	75	O	RAM address bit 1 output
RAMAD2	76	O	RAM address bit 2 output
RAMAD3	77	O	RAM address bit 3 output
RAMAD4	78	O	RAM address bit 4 output
RAMAD5	79	O	RAM address bit 5 output
RAMAD6	80	O	RAM address bit 6 output
V_{DDD7}	81	supply	digital supply voltage 7

SYMBOL	PIN	TYPE	DESCRIPTION
V_{SSD7}	82	supply	digital ground 7
RAMAD7	83	O	RAM address bit 7 output
RAMAD8	84	O	RAM address bit 8 output
RAMAD9	85	O	RAM address bit 9 output
n.c.	86	–	not connected, reserved
RAMAD10	87	O	RAM address bit 10 output
RAMAD11	88	O	RAM address bit 11 output
RAMAD12	89	O	RAM address bit 12 output
RAMAD13	90	O	RAM address bit 13 output
RAMAD14	91	O	RAM address bit 14 output
V_{DDD8}	92	supply	digital supply voltage 8
V_{SSD8}	93	supply	digital ground 8
CRIN	94	I	analog crystal input
CROUT	95	O	analog crystal output
CFLG	96	O	correction statistics output
MEAS1	97	O	front-end telemetry output
V_{DDD9}	98	supply	digital supply voltage 9
V_{SSD9}	99	supply	digital ground 9
V_{DDA1}	100	supply	analog supply voltage 1

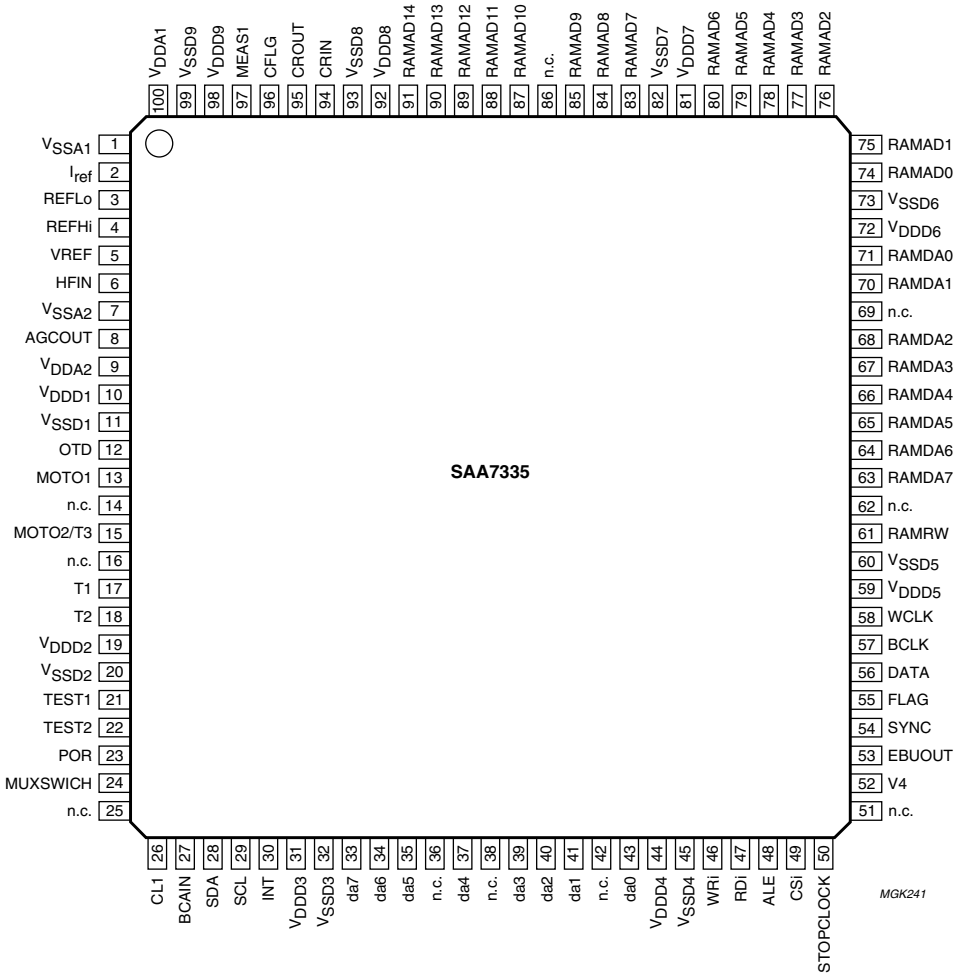


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Analog front-end

This block converts the HF input to the digital domain using an 8-bit ADC proceeded by an AGC circuit to obtain the optimum performance from the convertor. This block is clocked by ADCCLK which is set by the external crystal frequency plus a flexible clock multiplier and divider block.

PLL and bit detector

This subsystem recovers the data from the channel stream. The block corrects asymmetry, performs noise filtering and equalisation and finally recovers the bit clock and data from the channel using a digital PLL.

The equalizer and the data slicer are programmable.

Digital logic

All the digital system logic is clocked from the master ADC clock (ADCCLK) described above.

Advanced bit detector

The advanced bit detector offers improved data recovery for multi-layer discs and contains two extra detection circuits to increase the margins in the bit recovery block:

1. Adaptive slicer: adds a second stage slicer with higher bandwidth
2. Run length 2 push-back: all T2 run lengths are pushed back to T3, thereby automatically determining the erroneous edge and shifting the transitions on that edge.

Demodulator

FRAME SYNC PROTECTION CD MODE

This circuit detects the frame synchronization signals. Two synchronization counters are used in the SAA7335:

1. The coincidence counter: this is used to detect the coincidence of successive syncs. It generates a sync coincidence signal if 2 syncs are 588 ±1 EFM clocks apart.
2. The main counter: this is used to partition the EFM signal into 17-bit words. This counter is reset when:
   a) A sync coincidence is generated
   b) A sync is found within ±6 EFM clocks of its expected position.

The sync coincidence signal is also used to generate the lock signal which will go active HIGH when 1 sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no sync coincidence is found.

FRAME SYNC PROTECTION DVD MODE

This circuit detects the frame synchronization signals. Two synchronization counters are used in the SAA7335:

1. The coincidence counter: this is used to detect the coincidence of successive syncs. It generates a sync coincidence signal if 2 syncs are 1488 ±3 EFM+ clocks apart.
2. The main counter: this is used to partition the EFM+ signal into 16-bit words. This counter is reset when:
   a) A sync coincidence is generated
   b) A sync is found within ±10 EFM+ clocks of its expected position.

The sync coincidence signal is also used to generate the lock signal which will go active HIGH when 1 sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no sync coincidence is found.

EFM/EFM+ demodulation

The 14-bit EFM (16-bit EFM+) data and subcode words are decoded into 8-bit symbols.

Microcontroller interface

The SAA7335 has two microcontroller interfaces, one serial I²C-bus and one parallel (8051 microcontroller compatible).

The two communication modes may be operated at the same time, the modes are described below:

1. Parallel mode: protocol compatible with 8052 multiplexed bus:
   a) da0 to da7 = address/data bus
   b) ALE = Address Latch Enable, latches the address information on the bus
   c) $\overline{WRi}$ = active LOW write signal for write to SAA7335
   d) $\overline{RDi}$ = active LOW read signal for read from SAA7335
   e) CSi = active HIGH Chip Select signal (this signal gates the $\overline{RDi}$ and $\overline{WRi}$ signals).
2. I²C-bus mode: I²C-bus protocol where SAA7335 behaves as slave device where:
   a) SDA = I²C-bus data
   b) SCL = I²C-bus clock
   c) I²C-bus slave address (write mode) = 3EH
   d) I²C-bus slave address (read mode) = 3FH
   e) Maximum data transfer rate = 400 kbits/s.

MICROCONTROLLER INTERFACE (I²C-BUS MODE)

Bytes are transferred over the interface in single bytes of which there are two types; write data commands and read data commands.

The sequence for a write data command (1 data byte) is as follows:

- Send START condition
- Send address 3EH (write)
- Write command address byte
- Write data byte
- Send STOP condition.

The sequence for a read data command (that reads 1 data byte) is as follows:

- Send START condition
- Send address 3EH (write)
- Write status address byte
- Send STOP condition
- Send START condition
- Send address 3FH (read)
- Read data byte
- Send STOP condition.

READING AND WRITING DATA TO THE SAA7335

The SAA7335 has 32 × 8-bit configuration and status registers as shown in Table 1. Not all locations are currently defined and some remain reserved for future upgrades. These can be written to or read from via the microcontroller interface using either the serial or parallel control bus.

Am29LV160BT/Am29LV160BB

16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 3.0 Volt-only Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.35 μm process technology**
- **Supports Common Flash Memory Interface (CFI)**
- **High performance**
  - — Full voltage range: access times as fast as 90 ns
  - — Regulated voltage range: access times as fast as 80 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 10 mA read current
  - — 20 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 100,000 write cycle guarantee per sector**
- **Package option**
  - — 48-ball FBGA
  - — 48-ball μBGA
  - — 48-pin TSOP
  - — 44-pin SO
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion (not available on 44-pin SO)
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

GENERAL DESCRIPTION

The Am29LV160B is a 16 Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in 48-ball FBGA, 48-ball µBGA, 44-pin SO, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. A 12.0 V V_{PP} or 5.0 V_{CC} are not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 80, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Am29LV160B is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

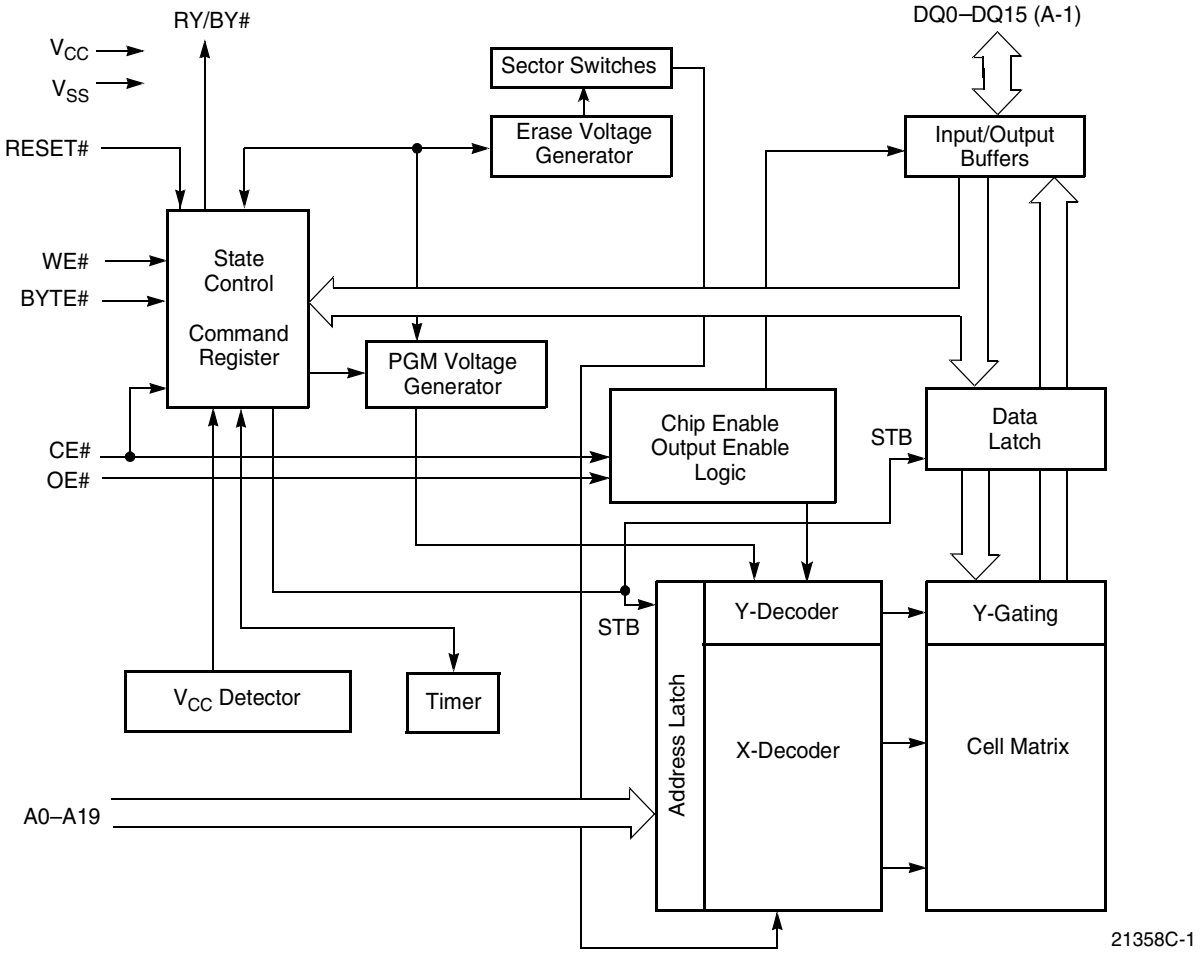
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

PRODUCT SELECTOR GUIDE

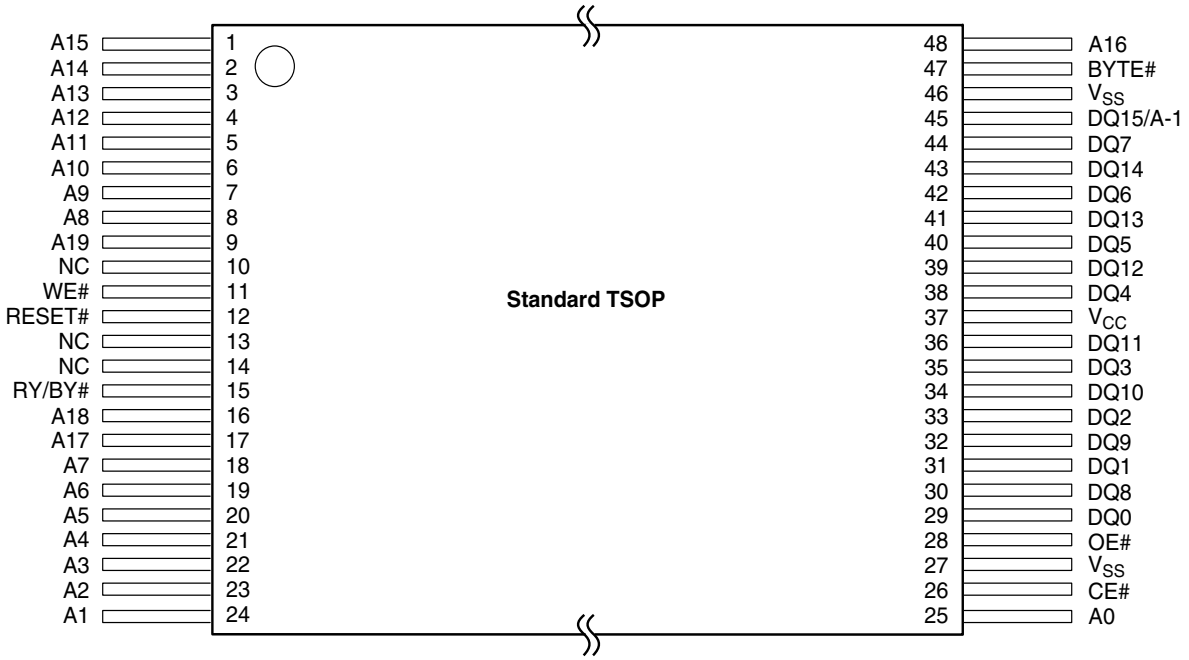
Family Part Number	Am29LV160B		
Ordering Part Number: V_{CC} =3.0–3.6 V	**80R**		
V_{CC} = 2.7–3.6 V		**90**	**120**
Max access time, ns (t_{ACC})	80	90	120
Max CE# access time, ns (t_{CE})	80	90	120
Max OE# access time, ns (t_{OE})	30	35	50

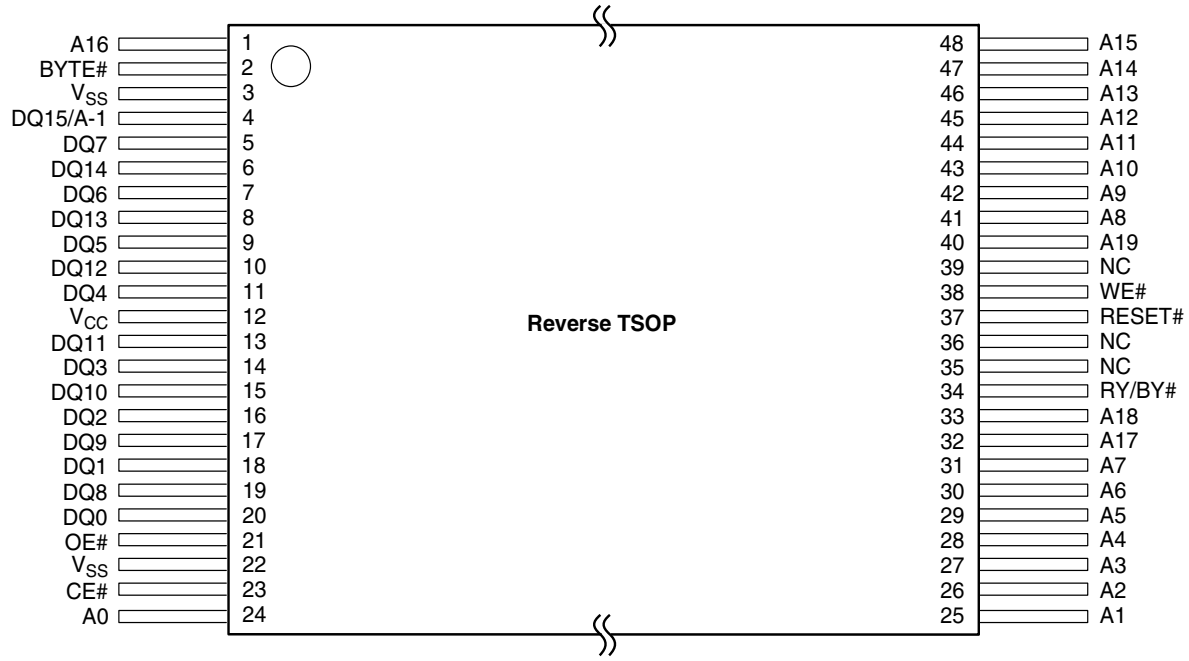
Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



CONNECTION DIAGRAMS





21358C-2

SYNCHRONOUS DRAM

MT48LC1M16A1 S - 512K x 16 x 2 banks

FEATURES

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
  1 Meg x 16 - 512K x 16 x 2 banks architecture with 11 row, 8 column addresses per bank
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge Mode, includes CONCURRENT AUTO PRECHARGE
- Self Refresh and Adaptable Auto Refresh Modes
  - 32ms, 2,048-cycle refresh or
  - 64ms, 2,048-cycle refresh or
  - 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Supports CAS latency of 1, 2 and 3

OPTIONS — MARKING

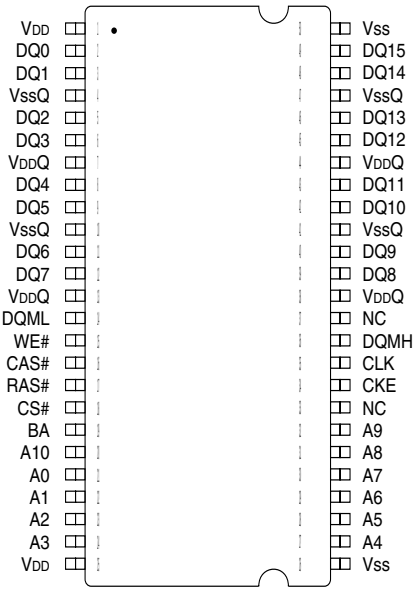
- Configuration
  1 Meg x 16 (512K x 16 x 2 banks) — 1M16A1
- Plastic Package - OCPL*
  50-pin TSOP (400 mil) — TG
- Timing (Cycle Time)
  6ns (166 MHz) — -6
  7ns (143 MHz) — -7
  8ns (125 MHz) — -8A
- Refresh
  2K or 4K with Self Refresh Mode at 64ms — S
- Part Number Example: MT48LC1M16A1TG-7S

KEY TIMING PARAMETERS

-6	166 MHz	5.5ns	2ns	1ns
-7	143 MHz	5.5ns	2ns	1ns
-8A	125 MHz	6ns	2ns	1ns

*Off-center parting line
**CL = CAS (READ) latency

PIN ASSIGNMENT (Top View)
50-Pin TSOP



Note: The # symbol indicates signal is active LOW.

16Mb (x16) SDRAM PART NUMBER

MT48LC1M16A1TG S	1 Meg x 16

GENERAL DESCRIPTION

The 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual 512K x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16-bit banks is organized as 2,048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed

16Mb: x16 SDRAM

sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

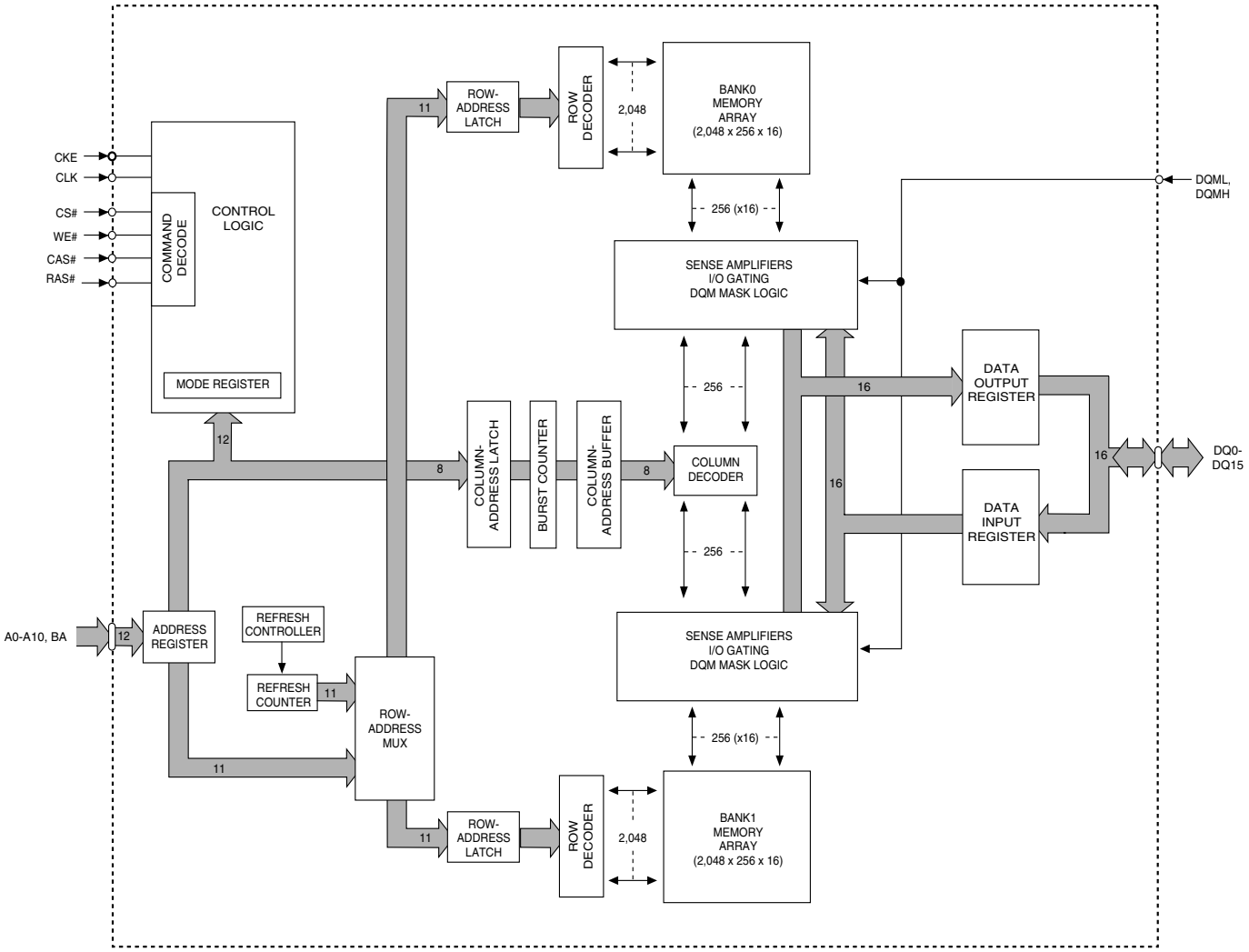
The 1 Meg x 16 SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2 rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 1 Meg x 16 SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

16Mb: x16 SDRAM

FUNCTIONAL BLOCK DIAGRAM
1 Meg x 16 SDRAM



PIN DESCRIPTIONS

Pin Number(s)	Symbol	Type	Description
35	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
34	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), ACTIVE POWER-DOWN (row ACTIVE in either bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
18	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
15, 16, 17	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
14, 36	DQML, DQMH	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ0-DQ7; DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
19	BA	Input	Bank Address Inputs: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the twelfth bit of the Mode Register.
21-24, 27-32, 20	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7, with A10 defining AUTO PRECHARGE) to select one location out of the 512K available in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0-DQ15	Input/ Output	Data I/Os: Data bus.
33, 37	NC	–	No Connect: These pins should be left unconnected.
7, 13, 38, 44	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
4, 10, 41, 47	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 25	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
26, 50	V_{SS}	Supply	Ground.

STi5505 (Rev. Ax)

DVD BACKEND DECODER WITH INTEGRATED HOST PROCESSOR

PRODUCT PREVIEW

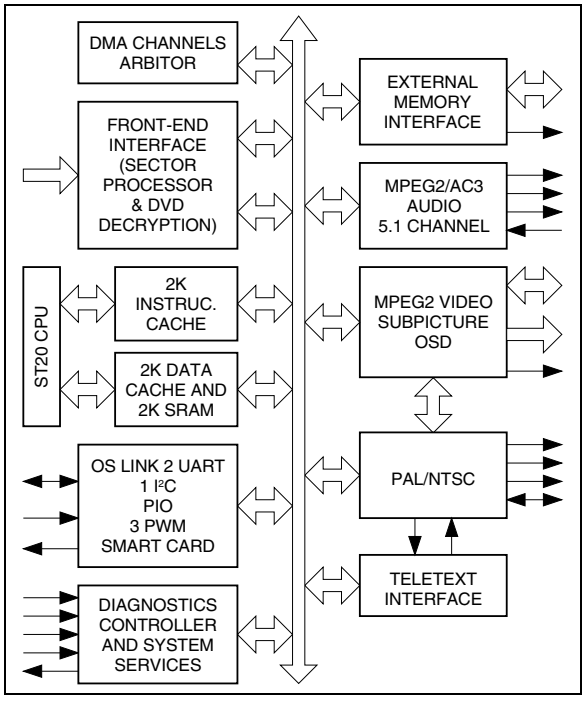
- INTEGRATED 32-BIT RISC HOST CPU
  - 2KBYTES INSTRUCTION CACHE, 2KBYTES DATA CACHE/SRAM
  - 50K DHRYSTONES/SEC (2.1) - 50MHz
- VIDEO DECODER
  - FULLY SUPPORTS MPEG-2 MP@ML
  - MEMORY REDUCTION - PAL IN 12MBITS
- SUBPICTURE DECODER
- HIGH PERFORMANCE ON-SCREEN DISPLAY
- AUDIO DECODER
  - 5.1 CHANNEL DOLBY AC-3® / MULTI CHANNEL MPEG-2 DECODING
  - DOWNMIX TO STEREO OR TO DOLBY PRO-LOGIC COMPATIBLE OUTPUTS FOR MPEG-2 AND AC-3
  - IEC6958 - IEC61937 COMPATIBLE OUTPUT
  - LPCM (DVD) MODE SUPPORTED
  - 6 CHANNELS OUTPUT
- PAL/NTSC ENCODER
  - MACROVISION™ 7.01/6.1 COMPATIBLE
  - TELETEXT, AND CLOSED CAPTION
- HIGH PERFORMANCE SDRAM INTERFACE
- PROGRAMMABLE MEMORY INTERFACE FOR DRAM, ROM, PERIPHERALS ETC.
- FRONT-END CHANNEL IC INTERFACE
  - DVD, VCD AND CD-DA COMPATIBLE
  - DSS - DVB BISTREAMS
  - SERIAL AND PARALLEL INTERFACES
  - HARDWARE SECTOR FILTERING
  - INTEGRATED CSS DECRYPTION AND TRACK BUFFER
- INTEGRATED PERIPHERALS
  - 2 UARTS, 1 I^2C CONTROLLER, 3 PWM OUTPUTS, 3 TIMERS, 3 CAPTURE TIMERS, SMART CARD
  - 34 BITS OF PROGRAMMABLE I/O
  - OS LINK
- PROFESSIONAL TOOLSET SUPPORT
  - ANSI C COMPILER AND LIBRARIES
  - OPERATING SYSTEMS SUPPORT
  - ADVANCED DEBUGGING TOOLS
- 208 PIN PQFP PACKAGE

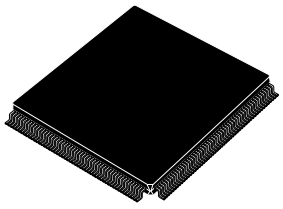
DESCRIPTION

The STi5505 provides a very highly integrated back-end solution for DVD and combo DVD-DVB (Set Top Box) applications. The STi5505 incorporates a host CPU which handles both general application (DVD navigation, CD-DA, VCD, DVB) and drivers of the different embedded periphals (audio/video, subpicture decoders, OSD, PAL/NTSC encoder...).

The STi5505 offers one of the best cost-effective (memory savings, internal peripherals availability) solution to DVD-DVB applications with rapid time to market (Reference design, DVD-DVB Software Toolkit).

Figure 1 : General Block Diagram





PQFP208 (Plastic Quad Flat Pack)
ORDER CODE : STi5505ACV

I - GENERAL DESCRIPTION

The performance offered by the ST20 CPU and its associated hardware (decoders, encoder, peripherals...) allows an integrated and unified DVD or DVD-DVB software solution.

All the following operations are performed inside the STi5505 :

- application management (DVD Navigation, VCD, CD-DA, DVB-Program Guide ...),
- device data retrieval drivers (demultiplex, stream buffer management ...),
- device presentation drivers (video decoder, subpicture decoder, on-screen display, audio decoder, PAL/NTSC encoder ...),
- embedded peripherals drivers (UART, I^2C, Programmable I/O, Smart Card ...).

I.1 - ST20 32-bit CPU

The ST20 micro-core family has been developped by SGS-THOMSON Microelectronics to provide the tools and building blocks to enable the development of highly integrated application-specific 32-bits device at the lowest cost and fastest time to market.

The STi5505 integrates a ST20 C2 core with the following characteristics :

- 50K Dhrystones/s at 50MHz,
- 8/16 bits instructions (32 most common instructions in 8 bits),
- instruction cache 2Kbytes - write back replacement policy,
- internal SRAM 2Kbytes to ensure fast access to critical code, data, interrupt handler ...
- data cache 2 Kbytes - write back replacement policy,

The STi5505's ST20 is provided with advanced debugging tools :

- on-chip real-time emulation,
- debugging with minimal impact on software and performance,
- non intrusive attachment to the host via JTAG (IEEE1149.1),
- no intrusion into the performance of the CPU core,
- no intrusion into user code space by a debug kernel,
- only 40bytes used for breakpoint handler.

I.2 - Video Decoder

The video decoder implemented in the STi5505 uses a patented memory reduction/bandwith reduction scheme to offer the user the best bandwidth/memory size compromise.
The algorithm is lossless and uses "on-the-fly" decoding to reduce the memory requirements to two frame buffers in memory reduction mode.

In this mode, PAL decoding is contained in 12Mbits. When used in bandwith reduction mode, the memory usage is the normal three buffers but the bandwith required by the decoder is significantly reduced compared to a classical implementation.

In summary, the features of the decoder are :

- MPEG-2 Main Profile/Main Level (MP@ML) support,
- MPEG-2 program streams, Packet Elementary streams and MPEG-1 system streams support,
- memory reduction architecture allowing sharing of single 16 Mbits SDRAM between MPEG decoding, micro and transport functions - memory expandable to 32 Mbits of SDRAM,
- letter box (16:9) filter,
- pan-scan, horizontal and vertical image resizing,
- automatic error concealment.

I.3 - Subpicture Decoder

The STi5505 has a hardware DVD compliant subpicture decoder. Subpicture units are copied by DMA into subpicture bit buffer.

The subpicture decoder can decode complete subpicture units without any interaction from the ST20.

The main subpicture decoder features are :

- up to 720x480 or 720x576 subpicture area,
- internal LUTs for Sub Picture, Highlight and PCI (4 bits color and contrast outputs),
- internal color LUT (4 bits from SP, HL, PCI to 24 Y,Cr,Cb bits) for SP color inputs to MPEG, OSD, SP mixer.

I.4 - Audio Decoder

The audio decoder cell is a fully compatible Dolby AC-3™ / MPEG-1/MPEG-2 decoder capable of decoding both 5.1 and 2 channel streams compatible with the DVD standard.

Downmix from 5.1 channels is supported for both Dolby and MPEG-2 streams. The output can be sent directly to external DACs or formatted for transmission in accordance with the IE6958 standard.

The decoder can also handle linear PCM in accordance with the DVD standard. An integrated downsampler is provided for conversion from 96 kHz to 48kHz.

STi5505 (Rev. Ax)

I - GENERAL DESCRIPTION (continued)

The main features of the decoder core are :

- Decodes 5.1 Dolby AC-3 Digital surround,
- Output to 6 channels. Downmix modes : 1, 2, 3 or 4 channels for MPEG and AC-3 streams,
- Karaoke mode for DVD. MPEG-2 capable, AC-3 capable,
- MPEG-1, 2-channel audio decoder layers 1 and 2,
- MPEG-2, 6-channel audio decoder layer 2,
- PCM : transparent. downsampling 96 to 48 kHz,
- Accepts MPEG-2 PES stream format for : MPEG-2, MPEG-1, Dolby AC-3 and Linear PCM,
- IEC6958 Output Interface,
- CD-DA PCM format (subcode output in IEC6958 user data),
- Downmix for Dolby Pro Logic compatible outputs for AC-3 and MPEG-2 (Pro Logic encoder),
- Pro Logic decoder,
- PLL for Internal 44.1 and 48kHz PCM clock generation,
- On chip pink noise generator.

I.5 - High Performance On-Screen Display

The graphics performance of the STi5505 supports the new requirements for intelligent program guides and interactive applications.

The display interface supports up to 256 colors for each OSD region and a transparency feature allows mixing of video with the OSD. Fast access graphics and many other additional features are available and are supported by a graphics library.

Very high system performance is obtained by closely coupling the ST20 RISC processor and cache with the MPEG audio/video core and display memory.

Low latency RISC access and DMA engines allow rapid construction of bit maps.

I.6 - PAL/NTSC Encoder

The STi5505 integrates a PAL/NTSC encoder. It converts the digital MPEG/Sub Picture/OSD stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. Six analog output pins are available on which it is possible to output CVBS, S-VHS (Y/C) and RGB formats.

The encoder handles interlaced and non-interlaced mode.

It can perform Closed Captions, CGMS or Teletext encoding and allows Macrovision 7.01/6.1 copy protection.

The encoder supports both master and slave modes for synchronization.

I.7 - Memory Interfaces

The STi5505 has been designed to minimize system costs by enabling various memory savings. Two kinds of memory interfaces are used on the STi5505 : a programmable External Memory Interface (EMI) and a high performance SDRAM interface.

The External Memory Interface supports several address ranges (memory banks). In each bank, a set of signals are entirely programmable and can be used to map 8/16 bits peripherals such as Front End channel ICs in DVD applications.

The EMI contains a zero glue logic DRAM and a low-cost EPROM interface.

This interface can be programmed to interface very easily peripherals.

The SDRAM memory interface supports gluelessly 125 MHz SDRAMs providing the adequate bandwiths to achieve MPEG decoding and display, OSD drawing and display, and general system use.

Memory savings can be realized on ROM requirements too : the ST20 VL-RISC micro-core has the highest code density of any 32 bit CPU, leading to the lowest cost program ROM.

I.8 - Front-End Interface

The STi5505 's front end interface accepts :

- DVD, VCD and CD-DA sectors,
- DVB-DSS transport stream.

In DVD mode, DVD, VCD and CD-DA information can be input into STi5505 through a serial interface or a generic parallel interface.

In serial mode, data are captured and filtered from I2S and V4 interfaces by an internal sector processor. V4 interface is used to capture VCD and CD-DA subcode information. In parallel mode, sector processor is bypassed.

I - GENERAL DESCRIPTION (continued)

The main features of the DVD interface are :

- DVD, VCD and CD-DA compatible,
- hardware sector filtering,
- subcode error correction for CD-DA,
- integrated CSS decryption,
- integrated track buffer support,
- DMA engine to ST20 memory.

In DVB-DSS mode, DVB-DSS transport stream is input through a serial interface. The STi5505 extracts and descrambles Packet Elementary Streams belonging to one user selected program to be decoded and presented.

The main features of the DVB-DSS interface are :

- descrambling (transport packet and packet elementary streams in DVB mode, transport packet in DSS mode ; up to 32 streams descrambling),
- PID and section filtering,
- clock recovery,
- DMA engine.

In DVB-DSS mode, a high speed digital interface allows to transfer packets between the Set Top Box and external units, either for recording or playback purposes. This interface provides also full support for an external IEEE1394 connection.

I.9 - Integrated Peripherals

Several peripherals generally used in DVD players or DVD-DVB combos have been integrated into the STi5505.

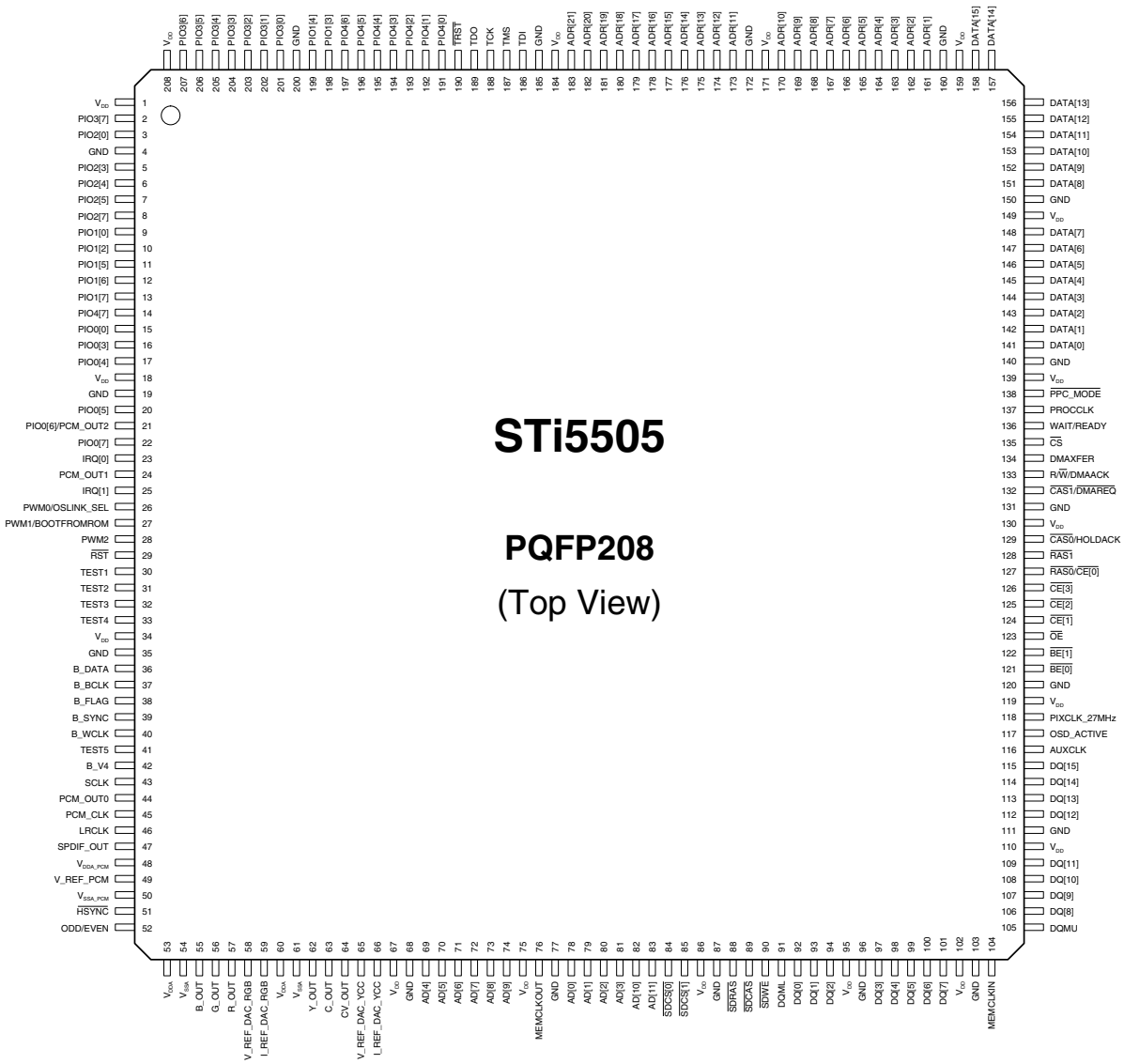
They are :

- two UARTs to interface remote control receivers, DVD front end, modem ...,
- one I^2C controller to interface serial memories, remote control receivers, microcontrollers...,
- 2 SmartCard interfaces (ISO7816-3) for DVB-DSS conditionnal access, pay per view ...,
- PWM/timer module for control of system clock,
- 34 programmable I/O pins,
- OS Link interface,
- JTAG with boundary scan for debug.

STi5505 (Rev. Ax)

II - PIN DESCRIPTION

II.1 - Pin Connections



II - PIN DESCRIPTION (continued)

II.2 - Pin List

Pin	Name	Type	Function
SUPPLIES			
1, 18, 34, 67, 75, 86, 95, 102, 110, 119, 130, 139, 149, 159, 171, 184, 208	V_{DD}		Power Supply
4, 19, 35, 68, 77, 87, 96, 103, 111, 120, 131, 140, 150, 160, 172, 185, 200	GND		Ground
53, 60	V_{DDA}		Analog Power Supply for DENC D/A Converters
54, 61	V_{SSA}		Analog Ground for DENC D/A Converters
48	V_{DDA_PCM}		Analog Power Supply for PLL PCM
49	V_REF_PCM		Analog Reference for PLL PCM
50	V_{SSA_PCM}		Analog Ground for PLL PCM
FRONT-END INTERFACE			
36	B_DATA	I	I^2S Data (DVD) or PARA_DATA[2] (DVD//) or Link Data (DVB/DSS)
40	B_WCLK	I/O	I^2S Word Clock or PARA_DATA[6] (DVD//) or NRSS_CLK (DVB/DSS)
37	B_BCLK	I	I^2S Bit Clock (DVD) or PARA_DATA[3] (DVD//) or Link Bit Clock (DVB/DSS)
38	B_FLAG	I	Error Flag (DVD) or PARA_DATA [4] (DVD//) or Link Sync (DVB/DSS)
39	B_SYNC	I	Sector / Abs Time Sync (DVD) or PARA_DATA[5] (DVD//) or Link Not Valid (DVB/DSS)
42	B_V4	I	Versatile Input Pin (Subcode Input) or PARA_DATA[7] (DVD//) or NRSS_IN (DVB/DSS)
VIDEO OUTPUT INTERFACE			
57	R_OUT	O	Red Output
56	G_OUT	O	Green Output
55	B_OUT	O	Blue Output
63	C_OUT	O	Chroma Output
64	CV_OUT	O	Composite Video Output
62	Y_OUT	O	Luma Output
59	I_REF_DAC_RGB	I	DAC Current Reference
66	I_REF_DAC_YCC	I	DAC Current Reference
58	V_REF_DAC_RGB	I	DAC Voltage Reference
65	V_REF_DAC_YCC	I	DAC Voltage Reference
117	OSD_ACTIVE	I/O	OSD Active
118	PIXCLK_27MHz	I	System Clock Input
51	$\overline{\text{HSYNC}}$	I/O	Horizontal Sync
52	ODD/EVEN	I/O	Vertical Sync
AC-3/MPEG1-2 AUDIO OUTPUT INTERFACE			
43	SCLK	O	Serial Bit Clock
44	PCM_OUT0	O	Audio Serial Output Data 0
24	PCM_OUT1	O	Audio Serial Output Data 1
21	PCM_OUT2	O	Audio Serial Output Data 2
45	PCM_CLK	I/O	PCM Clock In or Out
46	LRCLK	O	Left/Right Clock
47	SPDIF_OUT	O	SPDIF Output

STi5505 (Rev. Ax)

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Type	Function
EXTERNAL INTERRUPTS			
23, 25	IRQ[0:1]	I	External Interrupts
PROGRAMMABLE I/O AND ALTERNATE FUNCTION (see Device Configuration Chapter)			
15	PIO0 [0]	I/O	General Purpose I/O or PARA_SYNC (DVD//Front End) or Sc1Data (Smart Card 1 Data I/O)
16	PIO0 [3]	I/O	General Purpose I/O or PARA_REQ (DVD//Front End) or Sc1Clk (Smart Card 1 Clock)
17	PIO0 [4]	I/O	General Purpose I/O or PARA_STR (DVD//Front End) or Sc1RST (Smart Card 1 Reset)
20	PIO0 [5]	I/O	General Purpose I/O or PARA_DATA[0] (DVD//Front End) or Sc1Cmd V_{CC} (Smart Card 1 Voltage Enable)
21	PIO0 [6]	I/O	General Purpose IO or Sc1DataDir (Smart Card 1 Dir)
22	PIO0 [7]	I/O	General Purpose I/O or PARA_DATA[1] (DVD//Front End) or Sc1Detect(Smart Card 1 Detect)
9	PIO1 [0]	I/O	General Purpose I/O or I^2C Data
10	PIO1 [2]	I/O	General Purpose I/O or I^2C Clock
198, 199	PIO1 [3:4]	I/O	General Purpose IO
11	PIO1 [5]	I/O	General Purpose IO or ASC1 TXD
12	PIO1 [6]	I/O	General Purpose IO or ASC1 RXD
13	PIO1 [7]	I/O	General Purpose IO or ASC3 TXD
3	PIO2 [0]	I/O	General Purpose I/O or Sc0Data (Smart Card 0 Data I/O)
5	PIO2 [3]	I/O	General Purpose I/O or Sc0Clk (Smart Card 0 Clock)
6	PIO2 [4]	I/O	General Purpose I/O or Sc0RST (Smart Card 0 Reset)
7	PIO2 [5]	I/O	General Purpose I/O or Sc0CmdV_{CC} (Smart Card 0 Voltage Enable)
8	PIO2 [7]	I/O	General Purpose I/O or Sc0Detect (Smart Card 0 Detect)
201	PIO3 [0]	I/O	General Purpose IO or OSLink In
202	PIO3 [1]	I/O	General Purpose IO or OSLink Out
203	PIO3 [2]	I/O	General Purpose IO or CPUReset
204	PIO3 [3]	I/O	General Purpose IO or CPU Analyse
205	PIO3 [4]	I/O	General Purpose IO or ErrorOut
206, 207, 2	PIO3 [5:7]	I/O	General Purpose IO
191-197	PIO4 [0:6]	I/O	General Purpose IO
14	PIO4 [7]	I/O	General Purpose IO or ASC3 RXD
JTAG INTERFACE			
188	TCK	I	Test Clock
186	TDI	I	Test Data Input
189	TDO	O	Test Data Input
187	TMS	I	Test Mode Select
190	$\overline{\text{TRST}}$	I	Test Reset
SYSTEM USE			
28	PWM2	O	PWM2 Output
27	PWM1/BOOTFROMROM	O/I	PWM1 Output or Configuration Oslink Pins
26	PWM0/OSLINK_SEL	O/I	PWM0 Output or Boot from ROM during Reset
29	$\overline{\text{RST}}$	I	Reset
116	AUXCLK	O	Auxilary Clock for Any Purpose

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Type	Function
SDRAM INTERFACE			
78-81, 69, 70-74, 82, 83	AD[0:11]	O	SDRAM Address Bus
92-94, 97-101, 106-109, 112-115	DQ[0:15]	I/O	SDRAM Data (Lower Byte)
84, 85	$\overline{\text{SDCS}}$[0:1]	O	SDRAM Chip Selects
89	$\overline{\text{SDCAS}}$	O	SDRAM CAS
88	$\overline{\text{SDRAS}}$	O	SDRAM RAS
90	$\overline{\text{SDWE}}$	O	SDRAM Write Enable
104	MEMCLKIN	I	SDRAM Memory Clock Input
76	MEMCLKOUT	O	SDRAM Memory Clock Output
91	DQML	O	DQ Mask Enable (Lower)
105	DQMU	O	DQ Mask Enable (Upper)
EXTERNAL MEMORY INTERFACE			
161-170, 173-183	ADR[1:21]	I/O	External Memory Address Bus
141-148, 151-158	DATA[0:15]	I/O	External Memory Data Bus
128	$\overline{\text{RAS1}}$/HOLDREQ	O	DRAM RAS or reserved
136	WAIT/READY	I/O	External Wait States or Reserved
133	R/$\overline{\text{W}}$/DMAACK	I/O	DRAM R/$\overline{\text{W}}$ Strobe or Reserved
121, 122	$\overline{\text{BE}}$[0:1]	O	Byte enable
129	$\overline{\text{CAS0}}$/HOLDACK	O/I	DRAM CAS or Reserved
132	$\overline{\text{CAS1}}$/DMAREQ	O	DRAM CAS or Reserved
124-126	$\overline{\text{CE}}$[1:3]	O	Chip Select for Banks 1 - 3
135	$\overline{\text{CS}}$	I	Reserved
137	PROCCLK	I/O	ST20 Clock or Reserved
127	$\overline{\text{RAS0}}$/$\overline{\text{CE0}}$	O	DRAM RAS or Chip Select for Bank 0
134	DMAXFER	I	Reserved
138	$\overline{\text{PPC\_MODE}}$	I	Reserved
123	$\overline{\text{OE}}$	I/O	Output Enable or Reserved
SDAV/P1394 INTERFACE			
30	TEST1	I/O	DATA_RX/STROBE_TX (SDAV Mode) or SDAV_CLK (P1394 Mode)
31	TEST2	I/O	STROBE_RX/DATA_TX (SDAV Mode) or DATA_IN/DATA_OUT (P1394 Mode)
32	TEST3	I/O	Direction (SDAV Mode) or DATA_VALID In/Out (P1394 Mode)
MISCELLANEOUS			
41	TEST5	O	NRSS_OUT (DVB/DSS)

STi5505 (Rev. Ax)

III - FUNCTIONAL DESCRIPTION

III.1 - Functional Modules

Figure 1 shows the subsystem modules that make up the STi5505. These modules are outlined below.

III.1 - CPU

The Central Processing Unit (CPU) on the STi5505 is the ST20-C2 32-bit processor core. It contains instruction processing logic, instruction and data pointers and an operand register. It directly accesses the high speed on-chip SRAM memory, which can store data or programs, and uses the Caches to reduce access time to off chip program and data memory.

The processor can access memory via the general purpose External Memory Interface (EMI) or via the SDRAM EMI which is shared with the MPEG decoder.

III.2 - Memory Subsystem

The STi5505 on-chip SRAM memory system provides 160 Mbytes/s internal data bandwidth, supporting pipelined 2 cycles internal memory access at 25ns cycle times. The STi5505 memory system consists of 2 Kbytes of SRAM, 2Kbytes of instruction cache, a 2Kbytes data cache that can be programmed to be SRAM, and an external memory interface (EMI).

The STi5505 product has 2 Kbytes of on-chip SRAM. The advantage of this is the ability to store time critical code on chip, for instance interrupt routines, software kernels or device drivers, and even frequently used data without these being flushed from the caches.

The instruction and data caches are direct mapped with a write-back system for the data cache and support burst accesses to the external memories for refill and write-back which are effective for increasing performance with page-mode and SDRAM memories.

The STi5505 EMI controls access to the external memory and peripherals while the SDRAM EMI provides access to the SDRAM buffer for the MPEG decoders, ST20 and DMA peripherals.

The STi5505 EMI can access a 16 Mbytes (or greater if DRAM is used) physical address space in each of the four general purpose memory banks, and provides sustained transfer rates of up to 80 Mbytes/s. Peripherals that support an asynchronous data acknowledge are supported as is an external Power PC which can share the bus with the STi5505 and access the SDRAM buffer through the device.

High memory bandwidths up to 200 Mbytes/s can be supported by the SDRAM EMI.

The STi5505 internal memory interconnect provides buffering and arbitration of memory access requests to sustain very high throughput of memory accesses.

III.3 - System Services Module

The STi5505 system services module includes :

- Phase locked loop (PLL) - accepts 27MHz input and generates all the internal high frequency clocks needed for the CPU and the OS-Link.
- test access port - JTAG compatible.
- Diagnostics controller accessed via the JTAG port providing :
- Bootstrapping during development
- Hardware breakpoint and watchpoint
- Real time trace
- External LSA triggering support.

III.4 - Serial Communications

To facilitate the connection of this system the front end device and other peripherals, two UARTs (ASCs) are included in the device. The UARTs provide an asynchronous serial interface.

The UART can be programmed to support a range of baud rates and data formats, for example, data size, stop bits and parity. Two synchronous serial communications (SSC) interfaces are provided on the device. These can be used for a remote control device for example via an I^2C or SPI bus.

III.5 - Interrupt Subsystem

The STi5505 interrupt subsystem supports eight prioritized interrupt levels. Two external interrupt pins are provided. Level assignment logic allows any of the internal or external interrupts to be assigned and, if necessary, share any interrupt level.

III.6 - Front End Interface & DVD Decryption

The front end interface accepts sectors in the case of DVD, MPEG-1 system stream in the case of VCD and PCM data for CD-DA applications on an I2S interface. In the case of VCD and CD-DA disks the subcode information is input via a simple asynchronous serial interface similar to a UART.

The bitstream and subcode stream then pass through a "sector processor" block which handles sector filtering in the case of DVD and sectorizing using the subcode stream for VCD and CD-DA systems.

III - FUNCTIONAL DESCRIPTION (continued)

The block also handles overspeed processing for all systems. The capturing of CD-DA sectors is based on a flywheel tiner to improve robusters by concealing erros in the subcode stream. For DVD the data, having had sector headers removed, then passes through a DVD conformant de-cryption stage and is written into any of the system memories using a programmable DMA engine. When a subcode stream is present it is locally buffered, by subcode block and can be read by the CPU for subsequent processing, if required.

III.7- PWM and counter module

This unit includes three separate pulse width modulator (PWM) generators using a shared counter, and three timer compare and capture channels sharing a second counter.

The counters can be clocked from a pre-scaled internal clock or from a pre-scaled external clock via the capture clock input and the event on which the timer value is captured is also programmable.

The PWM counters are 8-bit with 8-bit registers to set the output high time. The capture/compare counter and the compare and capture registers are 32-bit.

III.8 - Parallel Programmable IO module

40 bits of parallel I/O are provided. 34 of then are connected to actual PIO pins. Each bit is programmable as an output or an input. The output can be configured as a totem pole or open drain driver. Input compare logic is provided which can generate an interrupt on any change on any input bit.

Many pins of the STi5505 device are multi-function and can either be configured as PIO or connected to an internal peripheral signal.

III.9 - MPEG Video decoder

The video decoder is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60 Hz and 720 x 576 x 50 Hz. Picture format conversion for display is performed by vertical and horizontal filters. User-defined bitmaps may be superimposed on the display picture through use of the on-screen display function.

III.10 - PAL/NTSC encoder

The digital encoder which is integrated in the STi5505 converts a multiplexed 4:2:2 YUV stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. The encoder can also perform closed-caption, CGMS or teletext encoding and allows Macrovision^{TM} 7.01/6.1 copy protection.

III.11 - MPEG-2 Audio / Dolby AC-3 Decoder

The audio decoder is a Dolby AC-3 decoder capable of decoding both 5.1 and 2 channel DVD comformant bitstreams. The decoder also handles MPEG-1 (layers 1 & 2) and MPEG-2 layer 2 (6 channels). Downmix to 2 channels is possible for Dolby and MPEG standards with optional pro-logic encoding.

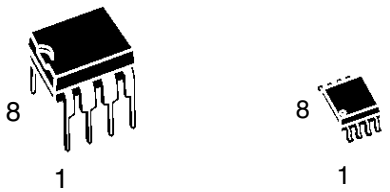
The decoder directly accepts MPEG-2 PES streams as input. The decoder is capable of supporting IEC6958-IEC61937 formatted outputs for AC-3 and MPEG audio, linear PCM (left & right,16, 18, 20 & 24 bits), zero output (Mute mode) and PCM audio.

ST24E32
ST25E32

32K SERIAL I²C EEPROM with EXTENDED ADDRESSING

NOT FOR NEW DESIGN

- COMPATIBLE with I²C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES, OVER the FULL SUPPLY VOLTAGE RANGE
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - ± 4.5V to 5.5V for ST24E32 version
  - ± 2.5V to 5.5V for ST25E32 version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 32 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES
- ***ST24E32 and ST25E32 are replaced by the M24C32***



PSDIP8 (B)
0.25mm Frame

SO8 (M)
200mil Width

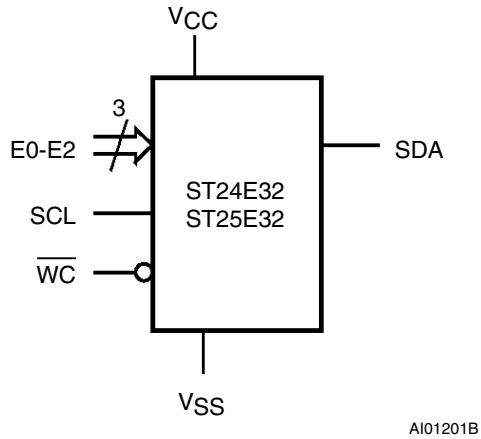
DESCRIPTION

The ST24/25E32 are 32K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 512 x 8 bits. The ST25E32 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



ST24E32, ST25E32

Figure 2A. DIP Pin Connections

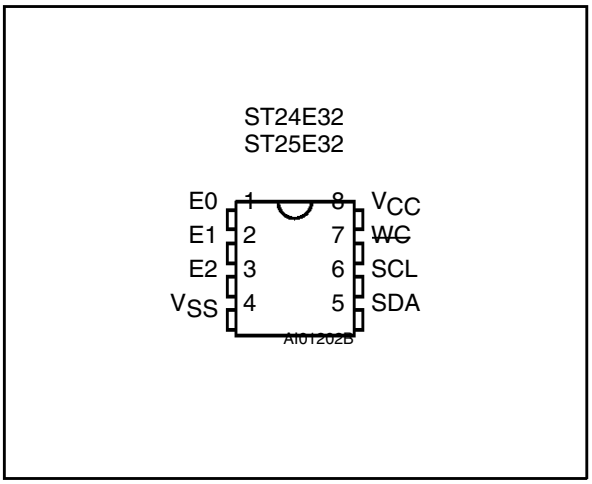


Figure 2B. SO Pin Connections

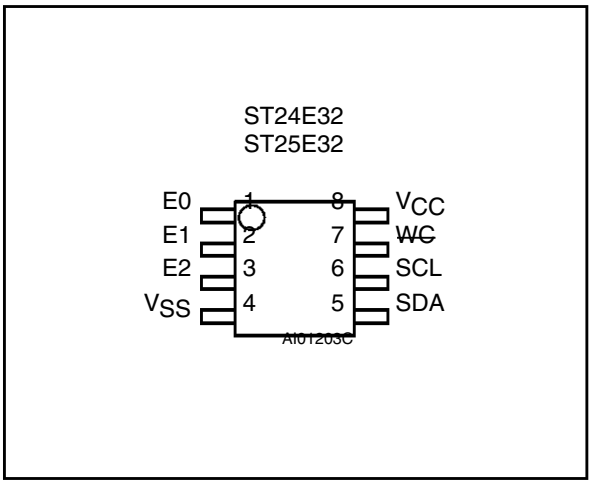


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			±40 to 125	°C
T_{STG}	Storage Temperature			±65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			±0.6 to 6.5	V
V_{CC}	Supply Voltage			±0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E32 carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E32 behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

10. Spare parts list

VAL6011

Various

0001	3139 197 60090	GENEVA LP LOADER ASSY
0002	9305 022 60101	VAM6001/01
0003	3139 194 00710	SUSPENSION
0004	3139 194 00710	SUSPENSION
0005	3139 194 00620	SUSPENSION
0006	3139 194 00620	SUSPENSION
0007	3139 197 60060	CLAMPER ASSEMBLY

Loader

Various

0004	4822 358 10266	
0009	3139 198 80010	
0010	4822 532 13097	TULE
0011	3139 194 00270	
0012	3139 197 50060	

Monoboard

Various

1104	2422 025 15963	CON BM H 24P F 0.50 FFC SMD R
1106	2422 025 16158	CON BM H 8P F 1.00 FFC 0.3 R
1205	2422 540 98428	RES CER SM 8M467 CSTCC8.46MHz R
1300	2422 540 98426	RES CER SM 6MHz CSTCC6.00MHz R
1301	4822 267 51454	CONN. 11P FEMALE
1603	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1604	2422 025 16388	CON BM V 16P F 1.00 FFC 0.3 R

⊣⊢

2100	4822 126 14305	100nF 10% 16V 0603
2101	4822 126 14305	100nF 10% 16V 0603
2103	4822 124 80151	47µF 16V
2104	4822 126 13193	4.7nF 10% 63V
2105	4822 122 33761	22pF 5% 50V
2107	4822 126 13956	68pF 5% 63V CASE 0603
2108	4822 126 14315	390pF 5% 50V 0603
2109	2020 552 95697	
2110	2222 861 15222	50V 2N2 PM5
2111	4822 126 14305	100nF 10% 16V 0603
2112	5322 126 11578	1nF 10% 50V 0603
2113	4822 126 14305	100nF 10% 16V 0603
2114	4822 122 31765	100pF 2% 63V
2115	4822 126 14305	100nF 10% 16V 0603
2116	4822 126 14305	100nF 10% 16V 0603
2117	4822 126 14305	100nF 10% 16V 0603
2120	4822 126 14305	100nF 10% 16V 0603
2121	4822 126 13879	220nF 20% 16V
2123	4822 126 14305	100nF 10% 16V 0603
2124	4822 126 14305	100nF 10% 16V 0603
2125	4822 126 14305	100nF 10% 16V 0603
2126	4822 126 14305	100nF 10% 16V 0603
2127	4822 126 14305	100nF 10% 16V 0603
2128	4822 126 14508	180pF 5% 50V 0603
2129	4822 126 14508	180pF 5% 50V 0603
2130	4822 122 33761	22pF 5% 50V
2131	4822 126 14494	22nF 10% 25V 0603
2136	4822 126 14305	100nF 10% 16V 0603
2137	4822 126 14305	100nF 10% 16V 0603
2138	4822 126 14305	100nF 10% 16V 0603
2139	4822 126 14305	100nF 10% 16V 0603
2140	4822 126 14241	0603 50V 330P COL R
2141	4822 122 33761	22pF 5% 50V
2142	5322 126 11583	10nF 10% 50V 0603
2143	4822 126 13883	220pF 5% 50V
2144	4822 126 13883	220pF 5% 50V
2145	4822 126 13883	220pF 5% 50V
2203	4822 126 14305	100nF 10% 16V 0603
2204	4822 126 14305	100nF 10% 16V 0603
2205	4822 126 14305	100nF 10% 16V 0603
2206	4822 126 14549	33nF 16V O6O3
2207	5322 126 11578	1nF 10% 50V 0603
2208	4822 126 14305	100nF 10% 16V 0603
2209	4822 126 14305	100nF 10% 16V 0603
2210	5322 126 11578	1nF 10% 50V 0603
2212	4822 126 14305	100nF 10% 16V 0603
2213	4822 126 14305	100nF 10% 16V 0603
2215	4822 124 23237	22µF 6.3V
2216	5322 126 11578	1nF 10% 50V 0603
2226	4822 126 14305	100nF 10% 16V 0603
2227	4822 126 14305	100nF 10% 16V 0603
2228	4822 126 14305	100nF 10% 16V 0603
2300	4822 126 14305	100nF 10% 16V 0603
2301	4822 126 14305	100nF 10% 16V 0603
2302	4822 126 14305	100nF 10% 16V 0603
2303	4822 124 80349	47µF 20% 6.3V
2306	4822 124 23002	10µF 16V
2309	4822 126 14305	100nF 10% 16V 0603
2310	4822 126 14305	100nF 10% 16V 0603
2314	4822 126 14305	100nF 10% 16V 0603
2315	4822 126 14305	100nF 10% 16V 0603
2318	5322 122 33861	120pF 10% 50V
2319	4822 126 11669	27pF
2401	4822 126 14305	100nF 10% 16V 0603
2402	4822 126 14305	100nF 10% 16V 0603
2403	4822 126 14305	100nF 10% 16V 0603
2404	4822 126 14305	100nF 10% 16V 0603
2405	4822 126 14305	100nF 10% 16V 0603
2406	4822 126 14305	100nF 10% 16V 0603
2407	4822 126 14305	100nF 10% 16V 0603
2408	4822 126 14305	100nF 10% 16V 0603
2409	4822 126 14305	100nF 10% 16V 0603
2410	4822 126 14305	100nF 10% 16V 0603
2411	4822 126 14305	100nF 10% 16V 0603
2412	4822 126 14305	100nF 10% 16V 0603
2413	4822 126 14305	100nF 10% 16V 0603
2418	4822 124 12095	100µF 20% 16V
2419	4822 124 80349	47µF 20% 6.3V
2420	4822 124 80349	47µF 20% 6.3V
2500	4822 126 14305	100nF 10% 16V 0603
2502	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2503	4822 126 14305	100nF 10% 16V 0603
2504	4822 122 31765	100pF 2% 63V
2505	4822 126 14494	22nF 10% 25V 0603
2506	4822 124 23002	10µF 16V
2507	4822 126 14305	100nF 10% 16V 0603
2508	5322 126 11579	3.3nF 10% 63V
2509	4822 126 14241	0603 50V 330P COL R
2510	4822 126 14305	100nF 10% 16V 0603
2511	4822 126 14305	100nF 10% 16V 0603
2512	4822 126 14305	100nF 10% 16V 0603
2513	4822 126 14305	100nF 10% 16V 0603
2514	4822 126 14305	100nF 10% 16V 0603
2515	4822 126 14305	100nF 10% 16V 0603
2516	4822 126 14305	100nF 10% 16V 0603
2517	4822 126 14305	100nF 10% 16V 0603
2518	4822 126 14305	100nF 10% 16V 0603
2519	4822 126 14305	100nF 10% 16V 0603
2520	4822 126 14305	100nF 10% 16V 0603
2521	4822 126 14305	100nF 10% 16V 0603
2522	4822 126 14305	100nF 10% 16V 0603
2523	4822 126 14305	100nF 10% 16V 0603
2524	4822 126 14305	100nF 10% 16V 0603
2525	4822 126 14305	100nF 10% 16V 0603
2526	4822 126 14305	100nF 10% 16V 0603
2527	4822 126 14305	100nF 10% 16V 0603
2528	4822 126 14305	100nF 10% 16V 0603
2529	4822 126 14305	100nF 10% 16V 0603
2530	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2531	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2532	4822 122 33777	47pF 5% 63V
2533	4822 122 33777	47pF 5% 63V
2534	5322 126 11578	1nF 10% 50V 0603
2535	5322 126 11578	1nF 10% 50V 0603
2600	4822 126 14494	22nF 10% 25V 0603
2601	4822 126 14247	0603 50V 1N5 COL R
2602	4822 126 14247	0603 50V 1N5 COL R
2603	4822 126 14305	100nF 10% 16V 0603
2604	4822 124 12095	100µF 20% 16V
2605	4822 126 14494	22nF 10% 25V 0603
2606	4822 124 12095	100µF 20% 16V
2607	4822 124 12095	100µF 20% 16V
2608	4822 124 23002	10µF 16V
2609	4822 124 80151	47µF 16V
2610	4822 126 14305	100nF 10% 16V 0603
2611	4822 124 12095	100µF 20% 16V
2614	4822 122 33777	47pF 5% 63V
2615	4822 122 33777	47pF 5% 63V
2616	4822 122 33777	47pF 5% 63V
2617	4822 122 33777	47pF 5% 63V
2618	4822 126 14305	100nF 10% 16V 0603
2619	4822 126 14305	100nF 10% 16V 0603
2620	4822 122 33777	47pF 5% 63V
2621	4822 122 33777	47pF 5% 63V
2622	4822 122 33777	47pF 5% 63V
2623	4822 122 33777	47pF 5% 63V
2624	4822 122 33777	47pF 5% 63V
2625	4822 122 33777	47pF 5% 63V
2626	4822 122 33777	47pF 5% 63V
2627	4822 122 33777	47pF 5% 63V
2632	4822 124 12095	100µF 20% 16V
2633	4822 124 12095	100µF 20% 16V
2634	4822 126 14305	100nF 10% 16V 0603
2635	4822 126 14305	100nF 10% 16V 0603
2636	4822 126 14305	100nF 10% 16V 0603
2637	4822 126 14305	100nF 10% 16V 0603
2638	4822 126 14305	100nF 10% 16V 0603
2639	4822 126 14305	100nF 10% 16V 0603

⊣▭⊢

3100	4822 117 11152	4Ω7 5%
3102	5322 117 13034	1k5 1% 0.063W 0603 RC22H
3103	5322 117 13034	1k5 1% 0.063W 0603 RC22H
3104	5322 117 13062	390Ω 1% 0.063W 0603 RC22H
3105	4822 051 30103	10k 5% 0.062W
3106	4822 051 30479	47Ω 5% 0.062W
3107	4822 051 20228	2Ω2 5% 0.1W
3108	4822 051 20228	2Ω2 5% 0.1W
3110	4822 051 30479	47Ω 5% 0.062W
3111	5322 117 13058	150Ω 1% 0.063W 0603 RC22H
3112	5322 117 13021	47Ω 1% 0.063W 0603 RC22H
3114	4822 051 20228	2Ω2 5% 0.1W
3115	4822 051 20228	2Ω2 5% 0.1W
3116	5322 117 13042	3k9 1% 0.063W 0603 RC22H
3117	4822 051 30181	180Ω 5% 0.062W
3118	4822 051 30681	680Ω 5% 0.062W
3119	5322 117 13062	390Ω 1% 0.063W 0603 RC22H
3120	4822 051 30102	1k 5% 0.062W
3121	4822 051 30273	27k 5% 0.062W
3122	4822 051 30471	470Ω 5% 0.062W
3123	4822 051 30103	10k 5% 0.062W
3124	4822 051 30471	470Ω 5% 0.062W
3125	4822 051 30103	10k 5% 0.062W
3126	4822 051 30103	10k 5% 0.062W
3127	4822 051 30223	22k 5% 0.062W
3128	2322 704 69109	
3129	4822 051 30392	3k9 5% 0.063W 0603
3130	4822 051 20228	2Ω2 5% 0.1W
3131	4822 051 20228	2Ω2 5% 0.1W
3132	4822 051 20228	2Ω2 5% 0.1W
3133	4822 051 20228	2Ω2 5% 0.1W
3134	5322 117 13047	330Ω 1% 0.063W 0603 RC22H
3135	4822 117 13613	2Ω2 5% 0603
3137	4822 117 13613	2Ω2 5% 0603
3138	5322 117 13053	6k8 1% 0.063W 0603 RC22H
3139	4822 117 12917	1Ω 5% 0.062W CASE0603
3140	4822 051 30479	47Ω 5% 0.062W
3141	4822 117 11152	4Ω7 5%
3142	5322 117 13028	12k 1% 0.063W 0603 RC22H
3143	5322 117 13043	220Ω 1% 0.063W 0603 RC22H
3144	2322 704 69109	
3146	4822 051 30103	10k 5% 0.062W
3147	4822 051 30103	10k 5% 0.062W
3148	5322 117 13022	22k 1% 0.063W 0603 RC22H
3153	4822 117 12139	22Ω 5% 0.062W
3155	4822 051 30103	10k 5% 0.062W
3157	4822 051 30103	10k 5% 0.062W
3158	5322 117 13017	100Ω 1% 0.063W 0603 RC22H
3160	4822 051 30101	100Ω 5% 0.062W
3161	4822 117 13613	2Ω2 5% 0603
3162	4822 051 30101	100Ω 5% 0.062W
3163	4822 051 30273	27k 5% 0.062W
3164	4822 117 13613	2Ω2 5% 0603

3165	5322 117 13063	120Ω 1% 0.063W 0603 RC22H
3166	4822 051 30393	39k 5% 0.062W
3167	4822 051 30101	100Ω 5% 0.062W
3168	5322 117 13047	330Ω 1% 0.063W 0603 RC22H
3169	4822 051 30101	100Ω 5% 0.062W
3170	4822 051 30101	100Ω 5% 0.062W
3171	4822 051 30101	100Ω 5% 0.062W
3172	4822 117 13632	100k 1% 0603 0.62W
3173	4822 117 13632	100k 1% 0603 0.62W
3174	4822 117 11152	4Ω7 5%
3175	4822 117 13613	2Ω2 5% 0603
3176	4822 051 30153	15k 5% 0.062W
3178	4822 117 11151	1Ω 5%
3179	4822 051 30221	220Ω 5% 0.062W
3180	4822 117 13632	100k 1% 0603 0.62W
3181	4822 051 30561	560Ω 5% 0.062W
3182	5322 117 13018	1k0 1% 0.063W 0603 RC22H
3183	5322 117 13017	100Ω 1% 0.063W 0603 RC22H
3184	2322 704 61204	
3185	4822 117 11151	1Ω 5%
3187	4822 051 30273	27k 5% 0.062W
3189	4822 051 30008	0Ω jumper
3190	4822 051 30008	0Ω jumper
3191	4822 051 30008	0Ω jumper
3192	4822 051 30008	0Ω jumper
3193	4822 051 30008	0Ω jumper
3194	4822 051 30008	0Ω jumper
3195	4822 051 30008	0Ω jumper
3197	4822 051 30008	0Ω jumper
3198	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3199	5322 117 13042	3k9 1% 0.063W 0603 RC22H
3200	4822 051 30103	10k 5% 0.062W
3201	4822 117 11151	1Ω 5%
3202	4822 117 11151	1Ω 5%
3203	4822 051 30105	1M 5% 0.062W
3204	4822 051 30331	330Ω 5% 0.062W
3205	4822 051 30103	10k 5% 0.062W
3206	4822 051 30103	10k 5% 0.062W
3208	4822 051 30272	2k7 5% 0.062W
3209	4822 051 30472	4k7 5% 0.062W
3210	4822 051 30392	3k9 5% 0.063W 0603
3211	4822 051 30472	4k7 5% 0.062W
3212	4822 117 11152	4Ω7 5%
3213	4822 117 11152	4Ω7 5%
3214	4822 051 30392	3k9 5% 0.063W 0603
3215	4822 051 30103	10k 5% 0.062W
3219	4822 051 30103	10k 5% 0.062W
3220	4822 051 30103	10k 5% 0.062W
3221	4822 051 30103	10k 5% 0.062W
3224	4822 051 30151	150Ω 5% 0.062W
3225	2322 704 62004	
3226	4822 051 30103	10k 5% 0.062W
3227	4822 051 30472	4k7 5% 0.062W
3229	4822 051 30123	12k 5% 0.062W
3230	4822 051 30103	10k 5% 0.062W
3231	4822 051 30103	10k 5% 0.062W
3232	4822 117 13613	2Ω2 5% 0603
3234	4822 117 12902	8k2 1% 0.063W 0603
3235	4822 117 13632	100k 1% 0603 0.62W
3236	4822 051 30472	4k7 5% 0.062W
3237	4822 051 30103	10k 5% 0.062W
3238	4822 051 30103	10k 5% 0.062W
3239	4822 051 30103	10k 5% 0.062W
3240	4822 051 30103	10k 5% 0.062W
3242	4822 051 30008	0Ω jumper
3243	4822 051 30008	0Ω jumper
3246	4822 051 30008	0Ω jumper
3247	4822 051 30008	0Ω jumper
3249	4822 051 30008	0Ω jumper
3250	4822 051 30008	0Ω jumper
3251	4822 051 30008	0Ω jumper
3252	4822 051 30008	0Ω jumper
3253	4822 051 30008	0Ω jumper
3254	4822 051 30008	0Ω jumper
3255	4822 051 30008	0Ω jumper
3256	4822 051 30008	0Ω jumper
3257	4822 051 30008	0Ω jumper
3258	4822 051 30008	0Ω jumper
3259	4822 117 11151	1Ω 5%
3260	4822 117 11151	1Ω 5%
3300	4822 117 11152	4Ω7 5%
3301	4822 051 30105	1M 5% 0.062W
3302	4822 051 30221	220Ω 5% 0.062W
3304	4822 051 30272	2k7 5% 0.062W
3305	4822 051 30272	2k7 5% 0.062W
3309	4822 051 30103	10k 5% 0.062W
3310	4822 051 30223	22k 5% 0.062W
3311	4822 051 30223	22k 5% 0.062W
3312	4822 051 30472	4k7 5% 0.062W
3313	4822 051 30472	4k7 5% 0.062W
3316	4822 051 20108	1Ω 5% 0.1W
3317	4822 051 20108	1Ω 5% 0.1W
3318	4822 051 30472	4k7 5% 0.062W
3319	4822 051 30479	47Ω 5% 0.062W
3320	4822 051 30472	4k7 5% 0.062W
3321	4822 051 30682	6k8 5% 0.062W
3322	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3323	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3324	4822 117 13632	100k 1% 0603 0.62W
3325	4822 051 30682	6k8 5% 0.062W
3326	4822 051 30479	47Ω 5% 0.062W
3327	4822 051 30682	6k8 5% 0.062W
3328	4822 051 30223	22k 5% 0.062W
3329	4822 051 30223	22k 5% 0.062W
3330	4822 051 30223	22k 5% 0.062W
3331	4822 051 30332	3k3 5% 0.062W
3332	4822 051 30332	3k3 5% 0.062W
3333	4822 051 30101	100Ω 5% 0.062W
3334	4822 051 30101	100Ω 5% 0.062W
3335	4822 051 30101	100Ω 5% 0.062W
3336	4822 051 30101	100Ω 5% 0.062W
3337	4822 051 30101	100Ω 5% 0.062W
3338	4822 051 30101	100Ω 5% 0.062W
3339	4822 051 30008	0Ω jumper
3340	4822 051 30008	0Ω jumper
3403	4822 051 30103	10k 5% 0.062W
3404	4822 051 30103	10k 5% 0.062W
3405	4822 051 30103	10k 5% 0.062W
3412	4822 051 30008	0Ω jumper
3414	4822 051 30008	0Ω jumper
3416	4822 051 30008	0Ω jumper
3500	4822 051 30332	3k3 5% 0.062W
3501	4822 051 30332	3k3 5% 0.062W
3502	4822 051 30223	22k 5% 0.062W
3503	4822 051 30103	10k 5% 0.062W
3504	4822 051 30103	10k 5% 0.062W
3505	4822 051 30103	10k 5% 0.062W
3506	4822 051 30103	10k 5% 0.062W
3507	4822 051 30472	4k7 5% 0.062W
3508	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3509	4822 051 30103	10k 5% 0.062W
3511	4822 051 30332	3k3 5% 0.062W
3512	4822 051 30332	3k3 5% 0.062W
3513	4822 051 30103	10k 5% 0.062W
3514	4822 051 30103	10k 5% 0.062W
3515	4822 051 30103	10k 5% 0.062W
3516	4822 051 30103	10k 5% 0.062W
3517	4822 051 30332	3k3 5% 0.062W
3519	4822 051 30103	10k 5% 0.062W
3520	4822 051 30103	10k 5% 0.062W
3521	4822 051 30103	10k 5% 0.062W
3522	4822 051 30103	10k 5% 0.062W
3523	4822 051 30332	3k3 5% 0.062W
3524	4822 051 30101	100Ω 5% 0.062W
3525	4822 051 30103	10k 5% 0.062W
3526	4822 051 30103	10k 5% 0.062W
3534	4822 051 30103	10k 5% 0.062W
3535	4822 051 30153	15k 5% 0.062W
3536	4822 051 30101	100Ω 5% 0.062W
3537	4822 051 30331	330Ω 5% 0.062W
3538	4822 051 30681	680Ω 5% 0.062W
3541	4822 051 30479	47Ω 5% 0.062W
3542	4822 051 30479	47Ω 5% 0.062W
3545	4822 051 30221	220Ω 5% 0.062W
3546	4822 051 30101	100Ω 5% 0.062W
3548	4822 051 30008	0Ω jumper
3549	4822 051 30008	0Ω jumper
3550	4822 051 30101	100Ω 5% 0.062W
3551	4822 051 30101	100Ω 5% 0.062W
3552	4822 051 30008	0Ω jumper
3554	4822 051 30008	0Ω jumper
3564	4822 051 30008	0Ω jumper
3566	4822 051 30008	0Ω jumper
3570	4822 051 30101	100Ω 5% 0.062W
3571	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3572	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3605	4822 051 30008	0Ω jumper
3606	4822 117 12925	47k 1% 0.063W 0603
3607	4822 117 13632	100k 1% 0603 0.62W
3608	4822 117 13632	100k 1% 0603 0.62W
3609	4822 117 13632	100k 1% 0603 0.62W
3610	4822 051 30103	10k 5% 0.062W
3611	4822 051 30103	10k 5% 0.062W
3612	4822 051 30103	10k 5% 0.062W
3613	4822 051 30103	10k 5% 0.062W
3614	4822 051 30103	10k 5% 0.062W
3615	4822 051 30103	10k 5% 0.062W
3616	4822 051 30103	10k 5% 0.062W
3618	4822 051 30223	22k 5% 0.062W
3619	4822 051 30223	22k 5% 0.062W
3620	4822 051 30101	100Ω 5% 0.062W
3621	4822 051 30101	100Ω 5% 0.062W
3622	4822 051 30101	100Ω 5% 0.062W
3623	4822 051 30101	100Ω 5% 0.062W
3624	4822 051 30101	100Ω 5% 0.062W
3625	4822 051 30101	100Ω 5% 0.062W
3626	4822 051 30102	1k 5% 0.062W
3627	4822 051 30471	470Ω 5% 0.062W
3628	4822 051 30471	470Ω 5% 0.062W
3629	4822 051 30472	4k7 5% 0.062W
3630	4822 051 30221	220Ω 5% 0.062W
3631	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3632	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3633	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3635	4822 051 30682	6k8 5% 0.062W
3636	4822 051 30682	6k8 5% 0.062W
3637	4822 051 30332	3k3 5% 0.062W
3642	4822 051 30103	10k 5% 0.062W
3647	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3648	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3651	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3654	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3655	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3656	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3657	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3658	4822 051 30102	1k 5% 0.062W
3659	4822 051 30102	1k 5% 0.062W
3660	4822 051 30102	1k 5% 0.062W
3661	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3662	4822 051 30102	1k 5% 0.062W
3663	4822 051 30102	1k 5% 0.062W
3664	2322 704 64301	RST SM 0603 RC22H 430Ω PM1 R
3665	4822 117 12139	22Ω 5% 0.062W
3667	4822 051 30331	330Ω 5% 0.062W
3669	4822 051 30008	0Ω jumper
3670	4822 051 30008	0Ω jumper
3671	4822 051 30223	22k 5% 0.062W
3672	4822 051 30479	47Ω 5% 0.062W
3673	4822 051 30101	100Ω 5% 0.062W
3677	4822 051 30008	0Ω jumper
3678	4822 051 30008	0Ω jumper
3679	4822 051 30008	0Ω jumper
3681	4822 051 30008	0Ω jumper
3683	4822 051 30008	0Ω jumper
3685	4822 051 30008	0Ω jumper
3686	4822 051 30223	22k 5% 0.062W
3687	4822 051 30223	22k 5% 0.062W
3688	4822 051 30472	4k7 5% 0.062W
3689	4822 051 30223	22k 5% 0.062W

⏦

5200	4822 157 11717	BLM31P500SPT
5300	4822 157 11717	BLM31P500SPT
5301	4822 157 11717	BLM31P500SPT
5402	4822 157 11499	BLM11P600SPT
5403	4822 157 11499	BLM11P600SPT
5501	4822 157 70299	2.2µH (NL322522T-2R2J)
5502	4822 157 70299	2.2µH (NL322522T-2R2J)
5503	4822 157 71206	BLM21A601SPT
5504	4822 157 71206	BLM21A601SPT
5600	4822 157 71206	BLM21A601SPT
5601	4822 157 11499	BLM11P600SPT
5602	4822 157 10547	15µH 5%
5603	4822 157 71206	BLM21A601SPT
5604	4822 157 10547	15µH 5%
5605	4822 157 10547	15µH 5%
5606	4822 157 10547	15µH 5%
5607	4822 157 10547	15µH 5%
5608	4822 157 10547	15µH 5%
5609	4822 157 11717	BLM31P500SPT
5610	4822 157 11717	BLM31P500SPT

⏩

6200	4822 130 11397	BAS316
6301	9322 128 69685	S1D

6302	9322 128 69685	S1D
6303	9322 128 69685	S1D
6600	4822 130 11528	1PS76SB10

7100	5322 130 42718	BFS20
7101	5322 130 42718	BFS20
7102	9352 637 37518	
7103	4822 209 17229	BA5938FM
7104	4822 209 30095	LM833D
7105	4822 209 32073	MC34072D
7106	5322 130 42718	BFS20
7109	4822 209 15083	AN78M09
7110	5322 130 60803	BST72A
7111	5322 130 60159	BC846B
7112	5322 130 60159	BC846B
7113	5322 130 60159	BC846B
7114	5322 130 60159	BC846B
7115	4822 130 60373	BC856B
7116	5322 130 60159	BC846B
7201	9351 869 80118	
7202	3104 123 95660	
7203	4822 130 60373	BC856B
7207	9352 636 60557	SAA7399HL/M2A
7304	4822 209 16877	BA6856FP
7310	4822 209 15899	CY7C199-15C
7311	9352 622 13557	SAA7335HL
7312	4822 130 60373	BC856B
7315	5322 130 60159	BC846B
7401	9322 132 01668	AM29LV160B
7404	9322 144 59668	IC SM MT48LC1M16A1TG-7S (MRN)R
7405	9322 144 59668	IC SM MT48LC1M16A1TG-7S (MRN)R
7501	5322 130 60159	BC846B
7503	9322 151 16671	IC SM STI5505AVC (ST00) Y
7504	4822 242 10838	27MHZ 120P FX0-31FT
7505	8204 056 05580	IC SM M24C32-WMN6TNKSA
7600	5322 209 71568	PC74HCT14T
7604	5322 130 60159	BC846B
7605	4822 209 17398	LD1117DT33
7607	5322 130 60159	BC846B
7608	4822 130 60373	BC856B
7609	4822 130 60373	BC856B
7610	5322 130 60159	BC846B
7611	9352 456 80115	
7612	5322 130 60159	BC846B
7613	5322 130 60159	BC846B
7614	5322 130 60159	BC846B
7615	5322 130 60159	BC846B
7616	4822 209 16062	MK2742-03S
7617	5322 130 60159	BC846B
7618	5322 130 60159	BC846B
7620	4822 130 60373	BC856B
7621	4822 130 42804	BC817-25