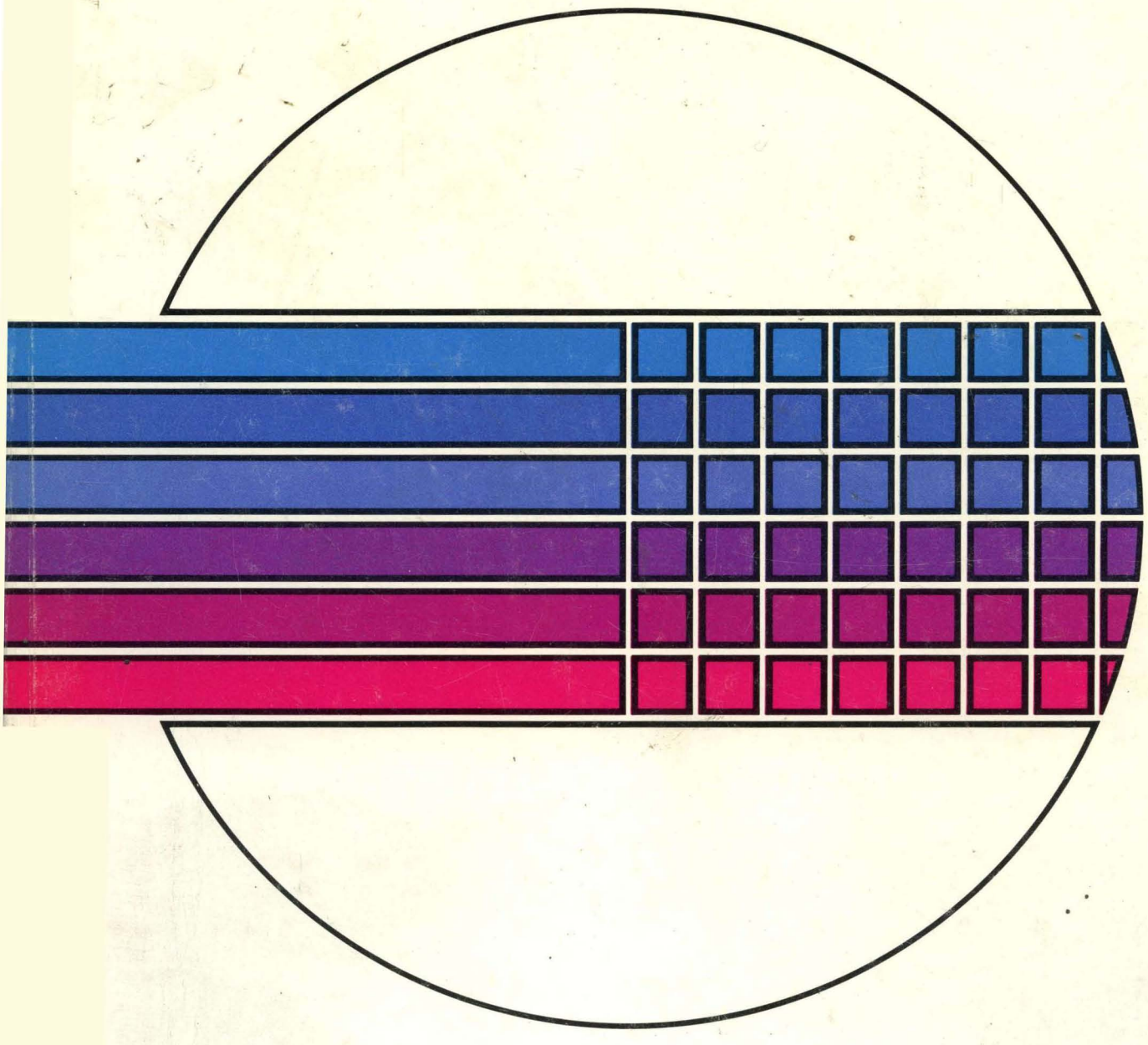
SIGNETICS BIPOLAR & MOS MEMORY

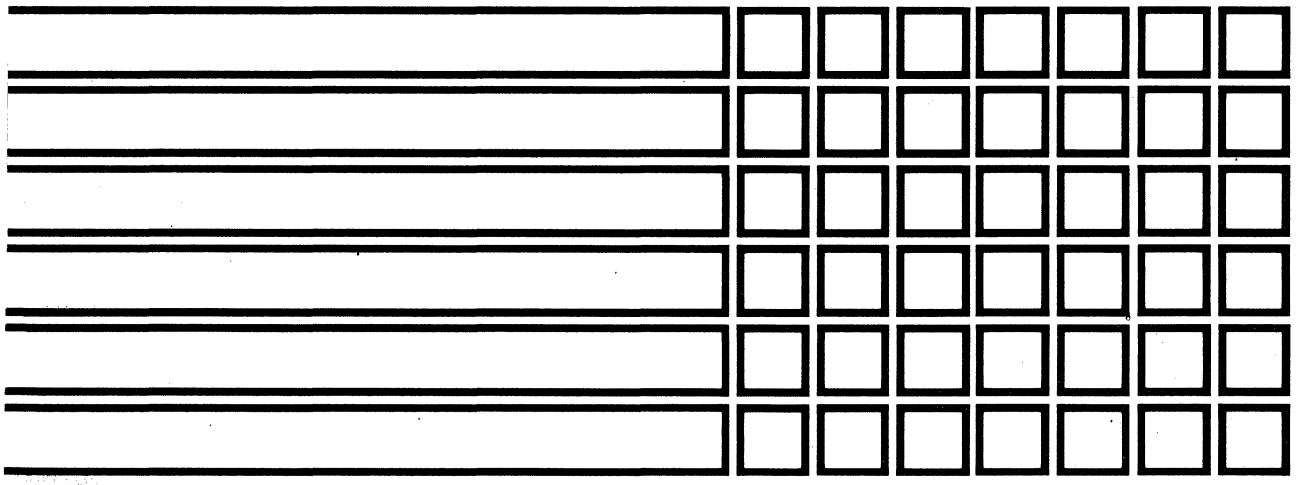
DATA MANUAL

$3.50



SIGNETICS BIPOLAR & MOS MEMORY

DATA MANUAL



Rapid improvement in both the cost and performance of semiconductor memories has led to a dramatic increase in their usage in today's highly sophisticated electronic systems. Signetics has worked diligently over the the last 10 years to develop the various technologies necessary to satisfy the broad range of users' semiconductor memory requirements. As a result, in 1977, Signetics is able to offer the broadest bipolar and MOS memory product lines available in the industry.

Signetics offers a complete line of bipolar Schottky RAMs, PROMs and other special memory products for high speed applications. These products are available with organizations ranging from 64 to 1024 bits for the RAM family and 256 to 8K bits for the PROM family. All Signetics' bipolar products are fabricated with double level metalization for maximum packaging density and low cost. PROM fuses are constructed with nichrome links for the highest reliability and programming yield in the industry. Signetics will continue to advance bipolar memory "state of the art" in 1977 with the introduction of our new 16K PROM, 4K RAM and programmable array logic products.

The MOS memory standard product line spans the many diverse memory application requirements of today's industry. Signetics' dynamic RAMs offer high bit density coupled with low standby power, while our static RAM family offers speed and ease of use. Ultra-violet (UV) eraseable EPROMs are available for use in development programs, with their ROM counterparts, in 8K and 16K densities in volume production. All Signetics' MOS 2600 series ROMs have a single +5V power supply and all industry standard pinouts are available. The MOS memory division also offers a complete shift register and character generator line.

The 1977 Signetics Memory Data Manual contains all necessary data on currently available products and those products which will be available in the future. In addition, the following pages provide product selection guides to aid the user in quickly selecting the optimum product for his particular system application.

Signetics reserves the right to make changes in the products contained in this book in order to improve design or performance and to supply the best possible products. Signetics also assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

TABLE OF CONTENTS

INTRODUCTION

BIPOLAR MEMORY CROSS REFERENCE

AMD	SIGNETICS
2700/27LS00	82S16
2701/27LS01	82S17
27S08/27LS08	82S23
27S09/27LS09	82S123
27S10	82S126
27S11	82S129
3101	82S25
3101A/27S02	3101A
93415	82S10
93415A	82S10
93425	82S11
93425A	82S11

FAIRCHILD	SIGNETICS
10149	10149
10144	10144
10410	10144
10415	10146
93403	82S25
93406	82S226
93411	82S17
93411A	82S117
93415	82S10
93415A	82S10
93417	82S126
93419	82S09
93421	82S16
93421A	82S116
93425A	82S11
93427	82S129
93431	82S130
93436	82S130
93438	82S140
93441	82S131
93442	82S240
93446	82S131
93448	82S141
93452	82S136
93453	82S137
93454	82S280
93457	82S126
93464	82S281
93467	82S129

HARRIS	SIGNETICS
0064	82S25
HM7602	82S23
HM7603	82S123
HM7608	82S2708
HM7610	82S126
HM7611	82S129
7615	10149
HM7620	82S130
HM7621	82S131
HM7640	82S140
HM7641	82S141
HM7642	82S136
HM7643	82S137
HM7647	82S115
HM7680	82S180
HM7681	82S181
HM7684	82S184
HM7685	82S185

INTEL	SIGNETICS
2708	82S2708
2716	82S2716
3101	82S25
3101A	3101A
3106/A	82S16
3107/A	82S17
3301A	82S226
3302	82S230
3322	82S231
3601	82S126
3602	82S130
3604	82S140
3605	82S136
3608	82S180
3622	82S131
3624	82S141
3625	82S137
3628	82S181

INTERSIL	SIGNETICS
5501	82S25
5508	82S10
5508A	82S10
5518	82S11
5518A	82S11
5523	74S201
5523A	82S16
5533	74S301
5533A	82S17
5600	82S23
5603A	82S126
5604	82S130
5605	82S140
5610	82S123
5623A	82S129
5624	82S131
5625	82S141
56506	82S136
56526	82S137

MOTOROLA	SIGNETICS
4004A	82S226
4064	82S25
4256	82S16
5005	82S126
10139	10139
10144	10144
10149	10149

MMI	SIGNETICS
6200	82S226
6201	82S229
6205	82S230
6206	82S231
6246	8204
6247	8205
6300-1	82S126
6301-1	82S129
6305-1	82S130
6306-1	82S131
6330	82S23
6331	82S123

MMI	SIGNETICS
6340-1	82S140
6341	82S141
6348	82S146
6349	82S147
6352	82S136
6353	82S137
6380	82S180
6381	82S181
6385	82S2708
6530	82S17
6531	82S16
H6555	82S09
6560	82S25/3101A

NATIONAL	SIGNETICS
74187	82S226
74S188	82S23
74S287	82S129
74S288	82S123
74S387	82S126
74S570	82S130
74S571	82S131
74S572	82S136
74S573	82S137
8582	82S17
86L99	82S25
87S295	82S140
87S296	82S141

T.I.	SIGNETICS
2708	82S2708
74187	82S226
74S188	82S23
74S189	74S189
74S200	74S200
74S201	74S201
74S209	82S11
74S270	82S230
74S287	82S129
74S288	82S123
74S289	3101A
74S301	74S301
74S309	82S10
74S370	82S231
74S387	82S126
74S472	82S147
74S473	82S146
74S474	82S141
74S475	82S140
74S476	82S137
74S477	82S136

Parts are pin for pin functional replacements except where noted. Signetics supplies most devices in both commercial and military temperature ranges.

BIPOLAR MEMORY SELECTION GUIDE

DEVICE	ORGANI-ZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME [ns][4]	TEMPERATURE RANGE[3]	PACKAGE	NO. OF PINS	MAX. I_{CC} [mA][4]
CAMS								
10155	8X2	OE	—	13	C	F,N	18	140
SAMS								
82S12	8X4	OC	T	40	C	F,N	24	160
82S112	8X4	TS	T	40	C	F,N	24	160
RAMS								
82S25	16X4	OC	B	50	M,C	F,N	16	105
3101A	16X4	OC	B	35	M,C	F,N	16	105
54/74S89	16X4	OC	T	50	M,C	F,N	16	105
54/74S189	16X4	TS	B	35	M,C	F,N	16	110
82S21	32X2	OC	T	50	C	F,N	16	130
82S16	256X1	TS	T	50	M,C	F,N	16	115
82S116	256X1	TS	T	40	C	F,N	16	115
82S17	256X1	OC	T	50	M,C	F,N	16	115
82S117	256X1	OC	T	40	C	F,N	16	115
54/74S200	256X1	TS	B	50	M,C	F,N	16	130
54/74S201	256X1	TS	B	50	M,C	F,N	16	130
54/74S301	256X1	OC	B	50	M,C	F,N	16	130
82S09	64X9	OC	T	45	M,C	I,N	28	190
82S10	1024X1	OC	B	45	M,C	F,N	16	170
82S110	1024X1	OC	B	35	C	F,N	16	170
82S11	1024X1	TS	B	45	M,C	F,N	16	170
82S111	1024X1	TS	B	35	C	F,N	16	170
93415A	1024X1	OC	B	45	M,C	F,N	16	170
93425A	1024X1	TS	B	45	M,C	F,N	16	170
82S208*	256X8	TS	B	60	C	F	22	185
82S210*	256X9	TS	B	60	C	F,N	24	185
82S400*	4096X1	OC	B	70	C	I	18	155
82S401*	4096X1	TS	B	70	C	I	18	155
ROMS								
82S226	256X4	OC	—	50	M,C	F,N	16	120
82S229	256X4	TS	—	50	M,C	F,N	16	120
82S214	256X8	TS	—	60	M,C	F,N	24	175
82S230	512X4	OC	—	50	M,C	F,N	16	140
82S231	512X4	TS	—	50	M,C	F,N	16	140
82S215	512X8	TS	—	60	M,C	F,N	24	175
82S240	512X8	OC	—	60	M,C	F,N	24	175
82S241	512X8	TS	—	60	M,C	F,N	24	175
8228	1024X4	TTL	—	50	C	F	16	170
82S280	1024X8	OC	—	70	M,C	F,N	24	140
82S281	1024X8	TS	—	70	M,C	F,N	24	140
82S290	2048X8	OC	—	80	M,C	F,N	24	170
82S291	2048X8	TS	—	80	M,C	F,N	24	170

*To be announced

NOTES

1. Output circuit:
   OE = Open emitter
   OC = Open collector
   TS = Tri-state
2. Output logic:
   T = Transparent—input data appears on output during Write
   B = Blanked—output is blanked during Write
3. Temperature range:
   C = Commercial (0° C to +75° C)
   M = Military (-55° C to +125° C)
   All ECL 10,000 series (-30° C to +85° C)
4. Commercial (0°C to +75°C)

BIPOLAR MEMORY SELECTION GUIDE (Cont'd)

DEVICE	ORGANI-ZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME (ns)	TEMPERATURE RANGE[3]	PACKAGE	NO. OF PINS	MAX. I_{CC} (mA)	EQUIVA-LENT ROM
PROMS									
82S23	32X8	OC	—	50	M,C	F,N	16	77	—
82S123	32X8	TS	—	50	M,C	F,N	16	77	—
10139	32X8	OE	—	15	C	F,N	16	145	—
82S27	256X4	OC	—	40	C	F	16	140	—
82S126	256X4	OC	—	50	M,C	F,N	16	120	82S226
82S129	256X4	TS	—	50	M,C	F,N	16	120	82S229
10149	256X4	OE	—	20	C	F	16	150	—
82S114	256X8	TS	—	60	M,C	F,N	24	175	82S214
82S130	512X4	OC	—	50	M,C	F,N	16	140	82S230
82S131	512X4	TS	—	50	M,C	F,N	16	140	82S231
82S115	512X8	TS	—	60	M,C	F,N	24	175	82S215
82S140	512X8	OC	—	60	M,C	F,N	24	175	82S240
82S141	512X8	TS	—	60	M,C	F,N	24	175	82S241
82S136	1024X4	OC	—	60	M,C	F,N	18	140	—
82S137	1024X4	TS	—	60	M,C	F,N	18	140	—
82S180	1024X8	OC	—	70	M,C	F,N	24	175	82S280
82S181	1024X8	TS	—	70	M,C	F,N	24	175	82S281
82S2708	1024X8	TS	—	70	M,C	F,N	24	175	—
82S184	2048X4	OC	—	100	M,C	I	18	120	—
82S185	2048X4	TS	—	100	M,C	I	18	120	—
82S190	2048X8	OC	—	70	M,C	I	24	175	82S290
82S191	2048X8	TS	—	70	M,C	I	24	175	82S291
FPLAS									
82S100	16X48X8	TS	—	50	M,C	I,N	28	170	—
82S101	16X48X8	OC	—	50	M,C	I,N	28	170	—
PLAS									
82S200	16X48X8	TS	—	50	M,C	I,N	28	170	—
82S201	16X48X8	OC	—	50	M,C	I,N	28	170	—
FPGAS									
82S102	16X9	OC	—	30	M,C	I,N	28	170	—
82S103	16X9	TS	—	30	M,C	I,N	28	170	—

*To be announced

NOTES

1. Output circuit:
   OE = Open emitter
   OC = Open collector
   TS = Tri-state
2. Output logic:
   T = Transparent—input data appears on output during Write
   B = Blanked—output is blanked during Write
3. Temperature range:
   C = Commercial (0° C to +75° C)
   M = Military (-55° C to +125° C)
   All ECL 10,000 series (-30° C to +85° C)
4. Commercial (0° C to +75° C)

MOS MEMORY CROSS REFERENCE

	SIGNETICS				
	RAMs	ROMs	CHARACTER GENERATORS	E PROMs	SHIFT REGISTERS
AMD					
AM2101/9101	2101				
AM2111/9111	2111				
AM2112/9112	2112				
AM2102/9102	2102/2102A				
AM9060	2680				
AM9216		2617			
AM9208		2608			
AM1402					2502
AM1403					2503
AM1404					2504
AM1405					2505
AM1506					2506
AM1507					2507/2517
AM2806					2512
AM2807					2524
AM2808					2525
AM2809					2521
AM2833					2533
AMI					
6830		2608			
EA					
2308/8308		2608			
4600		2600			
FAIRCHILD					
35L38	2101				
2102	2102				
4096	2660				
3343					2521
3343					2522
3347					2532
3349					2518
3533					2533
GI					
2513			2513		
2516			2516		
2530		2530			
2580		2580			
9316A/B		2616			
2509					2509
2510					2510
2511					2511
2533					2533
INTERSIL					
IM7552	2102				
IM7712					2512
IM7722					2525
IM7780					2532

MOS MEMORY CROSS REFERENCE (Cont'd)

	SIGNETICS				
	RAMs	ROMs	CHARACTER GENERATORS	E PROMs	SHIFT REGISTERS
INTEL					
2101	2101				
2111	2111				
2112	2112				
2102/2102A	2102/2102A				
1103	1103				
2107B	2680				
2104	2660				
2115	2115*				
2125	2125*				
2114	2614*				
2308		2607			
2316E		2616			
2704				2704	
2708				2708	
1402A					2502
1403A					2503
1404A					2504
1405A					2505
MOSTEK					
MK4007	2501				
MK4102	2102				
MK4096	2660				
MK4027	2627*				
MK30000		2607			
MK34000		2316			
MK3708				2708	
MK1007					2532
MOTOROLA					
2102/A	2102/2102A				
6604	2660				
6830		2608			
6570			2609		
NATIONAL					
MM2101	2101				
MM2111	2111				
MM2112	2112				
MM2102	2102				
MM5280	2680				
MM506					2506
MM507					2507/2517
MM1402A					2502
MM1403A					2503
MM1404A					2504
MM2521					2521
MM2522					2522
MM5058					2533

MOS MEMORY CROSS REFERENCE (Cont'd)

	SIGNETICS				
	RAMs	ROMs	CHARACTER GENERATORS	E PROMs	SHIFT REGISTERS
TI					
TMS4039	2101				
TMS4042	2111				
TMS4043	2112				
TMS4033-35	2102/2102A				
TMS1103	1103				
TMS4060	2680				
TMS4700		2607			
TMS3112					2518
TMS3120					2532
TMS3128					2521
TMS3129					2522
TMS3133					2533

MOS MEMORY SELECTION GUIDE

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	ACCESS/CYCLE TIME (ns)	TEMPERATURE RANGE[2]	PACKAGE	NO. OF PINS	CLOCK/CE/TTL COMPATABILITY	POWER SUPPLIES (V)
RAMS								
Static								
2501	256X1	TTL	1000/1000	C	I, N	16	Yes	+5, -9
25L01	256X1	TTL	1000/1000	C	I, N	16	Yes	±5, -12
2101	256X4	TS	1000/1000	C	F, N	22	Yes	+5, Gnd
2101-1	256X4	TS	500/500	C	F, N	22	Yes	+5, Gnd
2101-2	256X4	TS	650/650	C	F, N	22	Yes	+5, Gnd
2111	256X4	TS	1000/1000	C	I, N	18	Yes	+5, Gnd
2111-1	256X4	TS	500/500	C	I, N	18	Yes	+5, Gnd
2111-2	256X4	TS	650/650	C	I, N	18	Yes	+5, Gnd
2112	256X4	TS	1000/1000	C	F, N	16	Yes	+5, Gnd
2112-1	256X4	TS	500/500	C	F, N	16	Yes	+5, Gnd
2112-2	256X4	TS	650/650	C	F, N	16	Yes	+5, Gnd
2606	256X4	TS	750/750	C	F, I, N	16	Yes	+5, Gnd
2606-1	256X4	TS	500/500	C	F, I, N	16	Yes	+5, Gnd
2102	1024X1	TS	1000/1000	C	F, I, N	16	Yes	+5, Gnd
2102-1	1024X1	TS	500/500	C	F, I, N	16	Yes	+5, Gnd
2102-2	1024X1	TS	650/650	C	F, I, N	16	Yes	+5, Gnd
2102A	1024X1	TS	350/350	C	F, I, N	16	Yes	+5, Gnd
2102AL	1024X1	TS	350/350	C	F, I, N	16	Yes	+5, Gnd
2102A-2	1024X1	TS	250/250	C	F, I, N	16	Yes	+5, Gnd
2102AL-2	1024X1	TS	250/250	C	F, I, N	16	Yes	+5, Gnd
2102A-4	1024X1	TS	450/450	C	F, I, N	16	Yes	+5, Gnd
2102AL-4	1024X1	TS	450/450	C	F, I, N	16	Yes	+5, Gnd
2102A-6	1024X1	TS	650/650	C	F, I, N	16	Yes	+5, Gnd
21F02	1024X1	TS	350/350	C	F, I, N	16	Yes	+5, Gnd
210F02-2	1024X1	TS	250/250	C	F, I, N	16	Yes	+5, Gnd
21F02-4	1024X1	TS	450/450	C	F, I, N	16	Yes	+5, Gnd
21L02	1024X1	TS	1000/1000	C	F, I, N	16	Yes	+5, Gnd
21L02-1	1024X1	TS	500/500	C	F, I, N	16	Yes	+5, Gnd
21L02-2	1024X1	TS	650/650	C	F, I, N	16	Yes	+5, Gnd
21L02-3	1024X1	TS	400/400	C	F, I, N	16	Yes	+5, Gnd
2115*	1024X1	OD	45/45	C	F, I, N	16	Yes	+5, Gnd
2115L*	1024X1	OD	45/45	C	F, I, N	16	Yes	+5, Gnd
2125*	1024X1	TS	45/45	C	F, I, N	16	Yes	+5, Gnd
2125L*	1024X1	TS	45/45	C	F, I, N	16	Yes	+5, Gnd
2614*	1024X4	TS	200/200	C	F, I, N	18	—	+5, Gnd
2613*	4096X1	TS	200/200	C	F, I, N	18	—	+5, Gnd
Dynamic								
1103	1024X1	OD	300/480	C	I, N	18	No	+20, +16, Gnd
2660	4096X1	TS	250/375	C	F, I, N	16	Yes	+12, ±5, Gnd
2660-1	4096X1	TS	300/425	C	F, I, N	16	Yes	+12, ±5, Gnd
2660-2	4096X1	TS	350/500	C	F, I, N	16	Yes	+12, ±5, Gnd
2660-3	4096X1	TS	140/375	C	F, I, N	16	Yes	+12, ±5, Gnd
2680	4096X1	TS	200/400	C	F, I, N	22	No	+12, ±5, Gnd
2680-1	4096X1	TS	270/470	C	F, I, N	22	No	+12, ±5, Gnd
2680-2	4096X1	TS	350/800	C	F, I, N	22	No	+12, ±5, Gnd
2627*	4096X1	—	150/320	C	F	16	—	+12, ±5, Gnd
2627-1*	4096X1	—	200/200	C	F	16	—	+12, ±5, Gnd
2627-2*	4096X1	—	250/250	C	F	16	—	+12, ±5, Gnd
2690*	16,384X1	—	150/375	C	—	16	—	+12, ±5, Gnd

*To be announced

NOTES

1. Output circuit:
   TS = Tri-state
   OD = Open drain
   BD = Bare drain
   PD = Pull down
   PP = Push-pull
2. Temperature range:
   C = Commercial (0 °C to +75 °C)
   M = Military (-55 ° C to +125 °C)

MOS MEMORY SELECTION GUIDE (Cont'd)

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	ACCESS/CYCLE TIME (ns)	TEMPERATURE RANGE[2]	PACKAGE	NO. OF PINS	CLOCK/CE/TTL COMPATABILITY	POWER SUPPLIES (V)
ROMS								
Static								
2530	512X8	TS	700/700	C	I, N	24	Yes	±5, -12
2609	128X9X7	TS	500/500	C	F, I, N	24	Yes	+5, Gnd
2607	1024X8	TS	500/500	C	F, I, N	24	Yes	+5, Gnd
2608	1024X8	TS	550/550	C	F, I, N	24	Yes	+5, Gnd
2608-1	1024X8	TS	450/450	C	F, I, N	24	Yes	+5, Gnd
2580	2048X4	TS	950/950	C	I, N	24	Yes	+5, -12
2600	2048X8	TS	500/500	C	F, I, N	24	Yes	+5, Gnd
2600-1	2048X8	TS	300/300	C	F, I, N	24	Yes	+5, Gnd
2616	2048X8	TS	450	C	F, I, N	24	Yes	+5, Gnd
2616-1	2048X8	TS	350	C	F, I, N	24	Yes	+5, Gnd
2617	2048X8	TS	450	C	F, I, N	24	Yes	+5, Gnd
2617-1	2048X8	TS	350	C	F, I, N	24	Yes	+5, Gnd
2632*	4096X8	—	500/500	C	I, N	24	—	+5, Gnd
2633*	4096X8	—	450/450	C	I, N	24	—	+5, Gnd
CHARACTER GENERATORS								
2513	64X8X5	TS	600/600	C	I, N	24	Yes	±5, -12
2516	64X6X8	TS	600/600	C	I, N	24	Yes	±5, -12
2526	64X9X9	TS	700/700	C	I, N	24	Yes	+5, -12
UV EPROMS								
1702A	256X8	TS	1000/1000	C	I	24	Yes	+5, -9
2704	512X8	TS	450/450	C	I	24	Yes	+12, ±5, Gnd
2708	1024X8	TS	450/450	C	I	24	Yes	+12, ±5, Gnd

STANDARD ROM CODE

DEVICE	CODE NO.	DESCRIPTION
STATIC ROM		
2530	CM3530	Code Converter, ASCH to EBCDIC and EBCDIC to ASCII
2608	CN0000	10X7 Upper and Lower Case ASCII Character Generator
2609	CN6571	128 ASCII Characters in 7X9 Matrix Count Down
	CN6571A	128 ASCII Characters in 7X9 Matrix Count Up
	CN6575	128 ASCII Characters in 7X9 Matrix Count Up with Special Characters
2580	CMXXXX	Random code pattern for evaluation purposes
CHARACTER GENERATOR		
2513	CM2140	New ASCII Character Generator, Upper Case, 7X5, Horizontal Scan
	CM2170	ASCII Character Generator, Upper Case with Yen Sign, 7X5, Horizontal Scan
	CM3021	ASCII Character Generator, Lower Case, 7X5, Horizontal Scan
	CM3030	Old ASCII Character Generator, Upper Case, 7X5, Horizontal Scan
	CM4800	Katakana Character Generator, 7X5, Horizontal Scan
2516	CM2150	ASCII Character Generator, Upper Case, 5X7, Vertical Scan
	CM3001/3010	ASCII Character Generator, Upper Case, 10X7, Vertical Scan (2 chips)
	CM3041	ASCII Character Generator, Lower Case, 10X7, Vertical Scan
	CM3970/3980	ASCII Character Generator, Upper Case, 12X8, Vertical Scan (2 chips)
2526	CM3400	ASCII Character Generator with EBCDIC and BAUDOT code translations, Upper Case, 7X9, Vertical Scan
	CM3940	ASCII Character Generator, Upper Case, 7X9, Horizontal Scan
	CM6760	Katakana Character Generator, 7X9, Horizontal Scan

*To be announced

NOTES

1. Output circuit:
   TS = Tri-state
   OD = Open drain
   BD = Bare drain
   PD = Pull down
   PP = Push-pull
2. Temperature range:
   C = Commercial (0° C to +75° C)
   M = Military (-55 °C to +125 °C)

MOS MEMORY SELECTION GUIDE (Cont'd)

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	ON CHIP RECIRCULATE	TEMPERATURE RANGE[2]	PACKAGE	NO. OF PINS	NO. OF CLOCKS	TYPICAL SPEED (MHz)	CLOCK/CE/TTL COMPATABILITY	POWER SUPPLIES (V)
SHIFT REGISTERS										
Static										
2518	32X6	BD	Yes	C	N	16	1	3.0	Yes	+5, -12
2519	40X6	BD	Yes	C	N	16	1	3.0	Yes	+5, -12
2509	50X2	TS	Yes	C	N, K	14/10	1	3.0	Yes	+5, -5, -12
2532	80X4	PP	Yes	C	N	16	1	3.0	Yes	+5, -12
2510	100X2	TS	Yes	C	N, K	14/10	1	3.0	Yes	+5, -5, -12
2521	128X2	PP	Yes	C	N	8	1	3.0	Yes	+5, -12
2522	132X2	PP	Yes	C	N	8	1	3.0	Yes	+5, -12
2511	200X2	TS	Yes	C	N, K	14/10	1	3.0	Yes	+5, -5, -12
2527	240X2	PP	Yes	C	N	8	1	2.5	Yes	+5, -12
2528	250X2	PP	Yes	C	N	8	1	2.5	Yes	+5, -12
2529	256X2	PP	Yes	C	N	8	1	3.0	Yes	+5, -12
2533	1024X1	PP	Jumper	C	N	8	1	2.0	Yes	+5, -12
Dynamic										
2506	100X2	BD	No	C	T, N	8	2	4.0	No	+5, -5
2507	100X2	7.5KPD	No	C	T, N	8	2	4.0	No	+5, -5
2517	100X2	20KPD	No	C	T, N	8	2	4.0	No	+5, -5
2505	512X1	BD	Yes	C	K	10	2	3.0	No	+5, -5
2524	512X1	BD	Yes	C	N	8	2	5.0	No	+5, -5
2502	256X4	BD	No	C	N	16	2	10.0	No	+5, -5
2503	512X2	BD	No	C	TA, N	8	2	10.0	No	+5, -5
2504	1024X1	BD	No	C	TA, N	8	2	10.0	No	+5, -5
2512	1024X1	BD	Yes	C	K	10	2	5.0	No	+5, -5
2525	1024X1	BD	Yes	C	N	8	2	3.0	No	+5, -5

*To be announced

NOTES

1. Output circuit:
   TS = Tri-state
   OD = Open drain
   BD = Bare drain
   PD = Pull down
   PP = Push-pull
2. Temperature range:
   C = Commercial (0 °C to +75 °C)
   M = Military (-55 °C to +125 °C)

BIPOLAR MEMORY DATA SPECIFICATIONS

DESCRIPTION

The 10155 is a 16-bit ECL Content Addressable Memory (CAM) organized as an array of 8 words by 2 bits. Each cell of the array consists of a D-type latch and an exclusive-OR comparator, along with control logic for reading, writing and masking.

The modes of operation possible with the 10155 are associate, masked associate, read, write, and hybrid. Lines Y_0-Y_7 are used for linear word select in the read/write mode, and are used as outputs for match/mismatch information in the associate mode.

In associate operation, I_0 and I_1contain information to be compared. If the latches at a particular Y location are in a state matching the input data, that Y line goes low.

The Y outputs are open emitters, allowing expansion in multiples of 2 bits by tying additional 10155's to the Y bus lines. To inhibit comparison of a particular bit, the corresponding A_0 or A_1 line is held low.

In the read mode, the state of the selected cells appears on outputs D_0 and D_1. In the write mode, these outputs are transparent, following the state of I_0 and I_1.

In Hybrid mode, one of the I_0 or I_1 data inputs may be associated with the Q_{n0} or Q_{n1} cells respectively. If a match exists, the corresponding Y_n line(s) will go low, and can be used to address the other half of the memory for writing new data. Thus, it is possible to write I_1 in Q_{n1} where I_0 matches Q_{n0} or vice versa.

FEATURES

- **12ns associate time (max.)**
- **Linear address select**
- **Single bit masking**
- **50 Ω output drive**
- **ECL 10K compatible**
- **Open emitter match lines for easy bit expansion**
- **50k Ω input pulldown resistors (except on Y lines)**

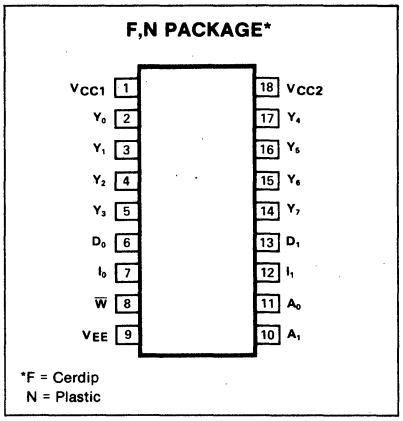
APPLICATION

- **Content addressable memory systems**

RECOMMENDED OPERATING VOLTAGES

- $V_{CC1} = V_{CC2} = 0V$
- $V_{EE} = -5.2V \pm 5\%$

PIN CONFIGURATION



*F = Cerdip
N = Plastic

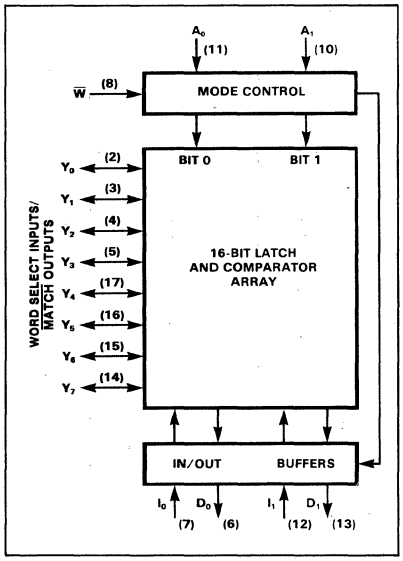
TRUTH TABLE (POSITIVE LOGIC)

MODE	A_0	A_1	I_0	I_1	$\overline{W}$	D_0	D_1	Q_{n0}	Q_{n1}	Y_n
Associate[1]	1	1	1/0	1/0	X	0	0	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0 + Q_{n1} \oplus I_1$
Associate[1,2] (masked)	1	0	1/0	X	1	0	D_1	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0$
Associate[1,2] (masked)	0	1	X	1/0	1	D_0	0	Q_{n0}	Q_{n1}	$Q_{n1} \oplus I_1$
Read[3]	0	0	X	X	1	D_0[2]	D_1[2]	Q_{n0}	Q_{n1}	0 (Selected address)
Write[3,4]	0	0	1/0	1/0	0	I_0	I_1	I_0	I_1	0 (Selected address)
Hybrid[5]	1	0	1/0	1/0	0	0	I_1	Q_{n0}	$I_1 \cdot \overline{Y_n}$	$Q_{n0} \oplus I_0$
Hybrid[5]	0	1	1/0	1/0	0	I_1	0	$I_0 \cdot \overline{Y_n}$	Q_{n1}	$Q_{n1} \oplus I_1$

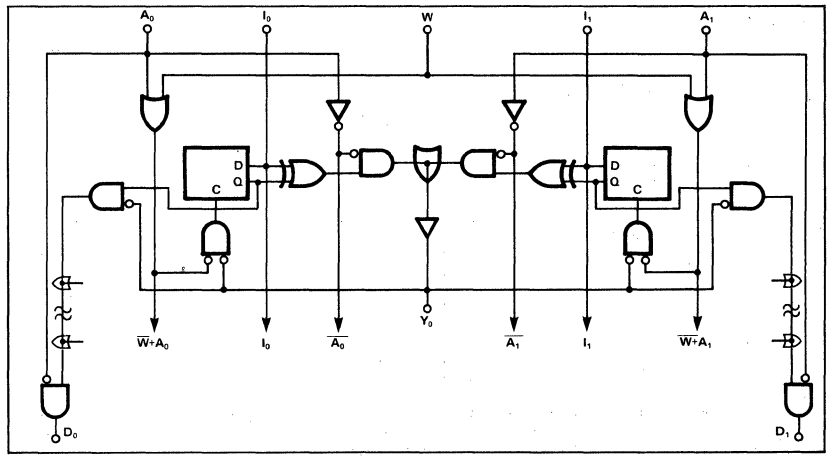
X = Don't care
Q_{n0} = Contents of address n, Bit 0 (n = 0 to 7)
Q_{n1} = Contents of address n, Bit 1

NOTES
1. 1 (high) = Mismatch, 0 (low) = Match
2. Read mode: $D_0 = Q_{00} \bullet \overline{Y_0} + Q_{10} \bullet \overline{Y_1} + \bullet\bullet\bullet + Q_{70} \bullet \overline{Y_7}$
   $D_1 = Q_{01} \bullet \overline{Y_0} + Q_{11} \bullet \overline{Y_1} \bullet\bullet\bullet + Q_{71} \bullet \overline{Y_7}$
3. In normal operation a single Y address is selected for read or write
4. Write is transparent
5. Simultaneous Associate and Write at all "Match" addresses.

BLOCK DIAGRAM



LOGIC DIAGRAM (TYPICAL BIT)



ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2} = 0V$

PARAMETER		RATING	UNIT
V_{EE}	Supply voltage	-8	Vdc
V_{IN}	Input voltage	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
	Temperature Range		°C
T_A	Operating	-30 to +85	
T_J	Operating junction	125	
T_{STG}	Storage	-55 to +125	

DC ELECTRICAL CHARACTERISTICS[1] $V_{CC1} = V_{CC2} = 0V$, $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2V$

PARAMETER		TEST CONDITIONS	-30 °C			+25 °C			+85 °C			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Input voltage											V
V_{IL}	Low		-1.890			-1.850			-1.825			
V_{IH}	High				-0.890			-0.810			-0.700	
V_{ILA}	Low threshold				-1.500			-1.475			-1.440	
V_{IHA}	High threshold		-1.205			-1.105			-1.035			
	Output voltage											V
V_{OL}	Low	V_{IH} = Max, V_{IL} = Min	-1.89		-1.675	-1.65	-1.70	-1.85	-1.825		-1.615	
V_{OH}	High		-1.06		-0.89	-0.96	-0.89	-0.81	-0.89		-0.70	
V_{OLA}	Low threshold				-1.655			-1.63			-1.595	
V_{OHA}	High threshold	V_{IHA} = Min, V_{ILA} = Max	-1.08			-0.98			-0.91			
	Input current											μA
I_{IL}	Low	Y,A,I,W = V_{IL} Min				0.5						
I_{IH}	High	A = V_{IH} Max						220				
		I,W = V_{IH} Max						200				
		Y = V_{IH} Max						50				
I_{EE}	Supply current	V_{IH} Max					115	140				mA

AC ELECTRICAL CHARACTERISTICS[2] $-30°C \le T_A \le +85°C$, $V_{CC1} = V_{CC2} = +2V$, $V_{EE} = -3.2V$, $R_L = 50\Omega$ to ground

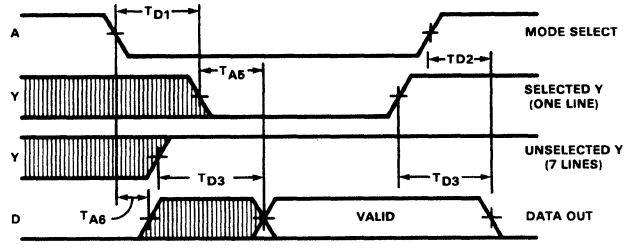
PARAMETER		FROM	TO	TEST CONDITIONS	LIMITS			UNIT
					Min[3]	Typ[4]	Max	
	Associate time							ns
T_{A1}		I±	Y±			8	12	
T_{A2}		A+	Y+			9	12	
	Disable time							ns
T_{D1}		A-	Y-			8	12	
T_{D2}		A+	D-			4	7	
T_{D3}		Y+	D-			9	13	
	Setup and hold time							ns
T_{H1}	Hold time	$\overline{W}$+	A+		1	0		
T_{S2}	Setup time	A-	Y-		15	11		
T_{H2}	Hold time	$\overline{W}$+	Y±		3	1		
T_{S3}	Setup time	Y+	$\overline{W}$-		3	2		
T_{H3}	Hold time	$\overline{W}$+	I±		3	1		
T_{S4}	Setup time	I±	$\overline{W}$+		5	3		
T_W	Write pulse width				10	5		ns
	Access time							ns
T_{A3}	Write	$\overline{W}$-	D±	$T_{S4} \ge T_W$		13	17	
T_{A4}	Write	I+,-	D+,-			9	13	
T_{A5}	Read	Y-	D+			6	10	
T_{A6}	Read	A-	D+			4		

NOTES

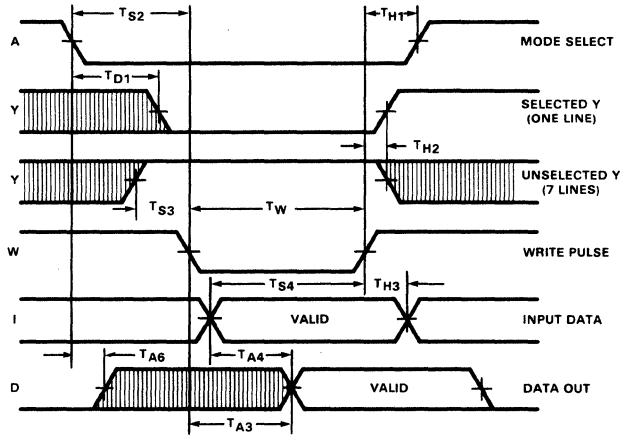
1. Each ECL 10K series device has been designed to meet the dc and ac specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
2. Refer to dc characteristics.
3. Minimum allowed.
4. All typical values are at $T_A = +25°C$.

VOLTAGE WAVEFORMS

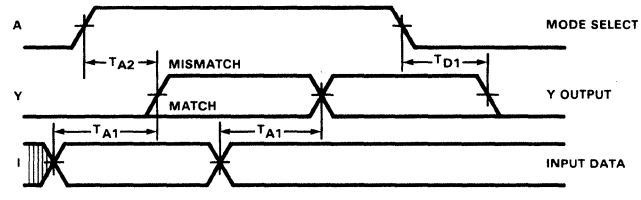
READ CYCLE



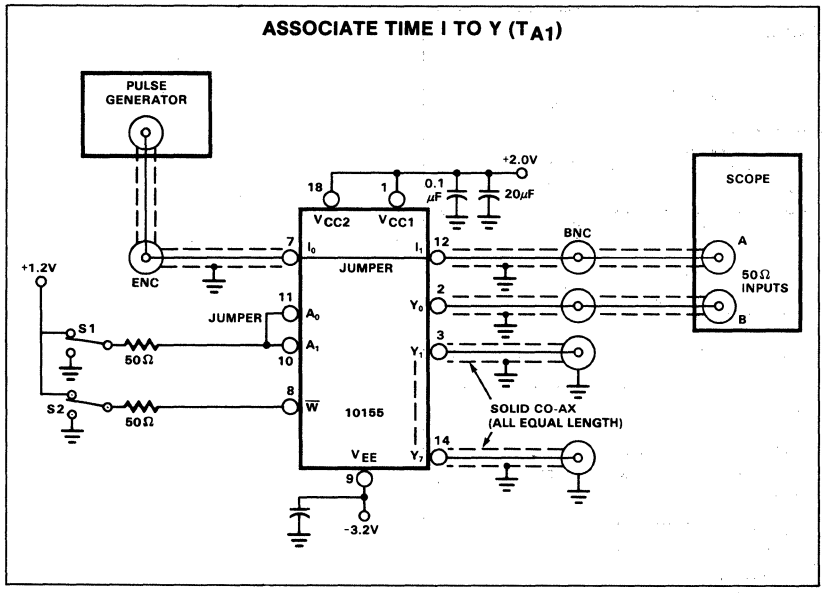
WRITE CYCLE



ASSOCIATE CYCLE



MEASUREMENT CIRCUIT



82S12-F,N • 82S112-F,N

DESCRIPTION

Data is stored in a single storage matrix which is addressed via 2 independent sets of address inputs, designated respectively as Port A and Port B.

Data can be read from memory via either Port A or B, through their respective output sets. However, input data (latched on the leading edge of write enable in the input data latches) is written only in memory locations specified by the address on Port A, regardless of Port B.

When both Port addresses are equal, data from the same location can be read in either or both Port output sets by means of output select lines S_A and S_B. During Write, new data stored in memory is immediately transferred on both Port output sets.

When both Port addresses are different, 2 different locations can be simultaneously read from memory. It is also possible to simultaneously read through Port B while writing new input data through Port A by utilizing the "A_N" address to specify the location of the word to be written, and the "B_N" address to specify the word to be read.

Both devices are ideally suited for high speed accumulator and buffer memories, and can be readily expanded to form larger arrays by means of their output select and write enable lines.

Both the 82S12 and 82S112 are available over the limited temperature range of +10°C to +75°C. Over this temperature range, specify N82S12/82S112F,N.

FEATURES

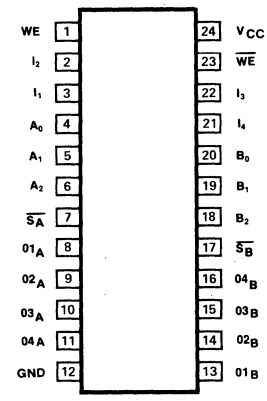
- **Address access time: 40ns max**
- **Write cycle time: 65ns max**
- **Power dissipation: 8.5mW/bit typ**
- **Input loading: −250μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S12 Open collector**
  - **82S112 Tri-state**
- **Non-inverting outputs**
- **Input data latches**
- **Two write enable lines**
- **Separate output enable lines**
- **Output follows data input during write**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Accumulator register**
- **Data routing/shifting**
- **ALU control**
- **Multiprocessor memory management**
- **Bandwidth increase by multi-operand fetch**
- **Communication controllers**
- **I/O data packing/unpacking**
- **Large FIFO memories**

PIN CONFIGURATION

F,N PACKAGE*



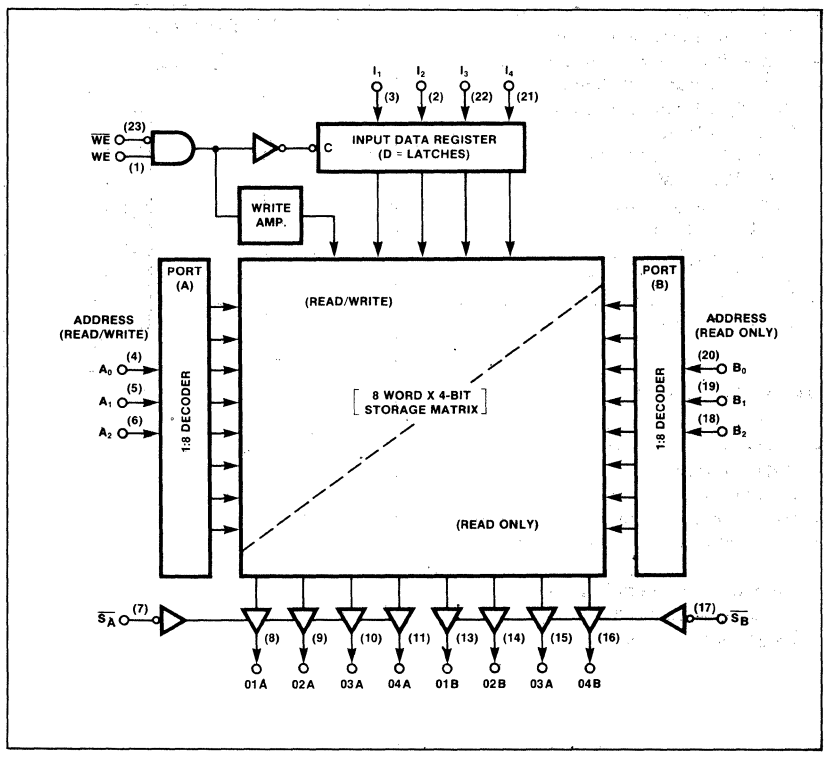
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	WE	$\overline{WE}$	I_N	$\overline{S_A}$	$\overline{S_B}$	PORT ADDRESS	82S12 $(O_N)A$	82S12 $(O_N)B$	82S112 $(O_N)A$	82S112 $(O_N)B$
Disabled				1	1	X	1	1	Hi-Z	Hi-Z
Read	0 or X	X or 1	X	0	1	A = B	Stored Data	1	Stored Data	Hi-Z
				1	0		1	Stored Data	Hi-Z	Stored Data
				0	0		Stored Data	Stored Data	Stored Data	Stored Data
				0	1	A ≠ B	[A_N]	1	[A_N]	Hi-Z
				1	0		1	[B_N]	Hi-Z	[B_N]
				0	0		[A_N]	[B_N]	[A_N]	[B_N]
Write	1	0	1/0	1	1	A = B	1	1	Hi-Z	Hi-Z
				0	1		I_N	1	I_N	Hi-Z
				1	0		1	I_N	Hi-Z	I_N
				0	0		I_N	I_N	I_N	I_N
				1	1	A ≠ B	1	1	Hi-Z	Hi-Z
				0	1		I_N	1	I_N	Hi-Z
				1	0		1	[B_N]	Hi-Z	[B_N]
				0	0		I_N	[B_N]	I_N	[B_N]

X = Don't care
[ ] = Contents of

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S12)	+5.5	
V_O	Off-state (82S112)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $+10°C \le T_A \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER[1]		TEST CONDITIONS	82S12			82S112			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IH}	High[1]	V_{CC} = 5.25V	2			2			
V_{IL}	Low[1]	V_{CC} = 4.75V			0.85			0.85	
V_{IC}	Clamp[1,3]	V_{CC} = 4.75V, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = 4.75V							V
V_{OH}	High[1,4]	I_{OH} = -2mA				2.4			
V_{OL}	Low[1,5]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.45	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		-10	-250		-10	-250	
	Output current	V_{CC} = 5.25V							
I_{OLK}	Leakage[6]	V_{OUT} = 5.25V		1	40				μA
$I_{O(OFF)}$	Hi-Z state[6]	V_{OUT} = 5.25V					1	40	μA
		V_{OUT} = 0.45V					-1	-40	
I_{OS}	Short circuit[3,7]	V_{OUT} = 0V				-20		-70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = 5.25V		110	160		110	160	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
V_{OUT}	Output	V_{OUT} = 2.0V		8			8		

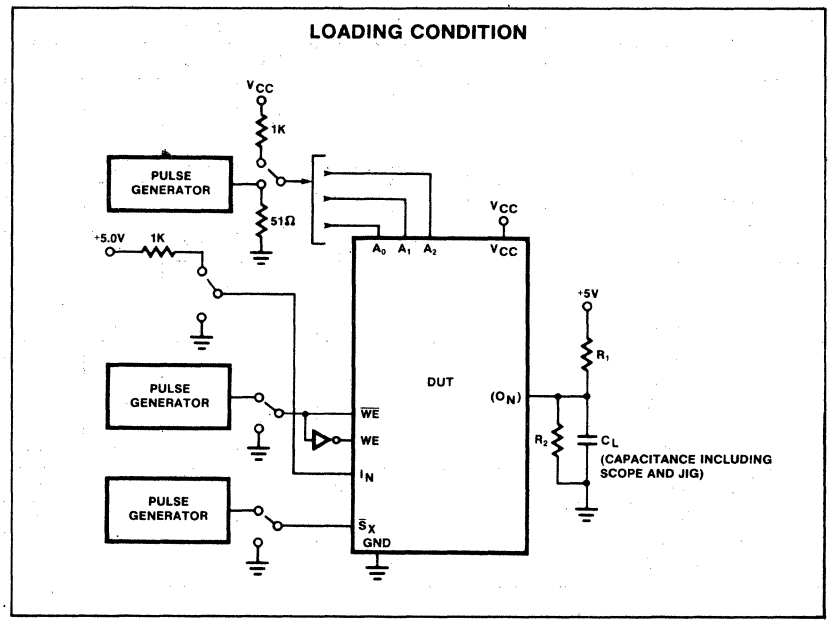
AC ELECTRICAL CHARACTERISTICS $+10°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
	Access time						ns
T_{AA}	Address	Output	Address			40	
T_{SE}	Port select	Output	Output enable			30	
	Disable time						ns
T_{SD}	Port deselect	Output	Output enable			30	
T_{WD}	Valid time	Output	Write enable			40	ns
	Setup and hold time						ns
T_{WSA}	Setup time	Write enable	Address	15	10		
T_{WHA}	Hold time			5	0		
T_{WSD}	Setup time	Write enable	Data in	15			
T_{WHD}	Hold time			10			
	Pulse width						ns
T_{WP}	Write enable			45			

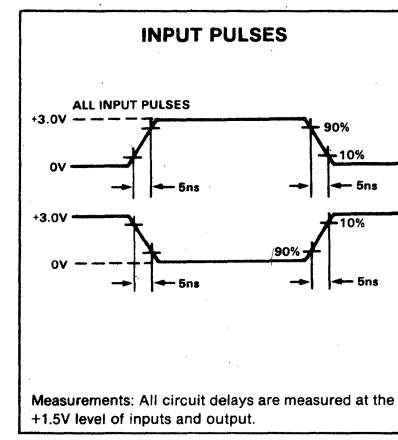
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test one at the time.
4. Measured with V_{IL} applied to $\overline{Sx}$ and a logic high stored.
5. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{Sx}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with all inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

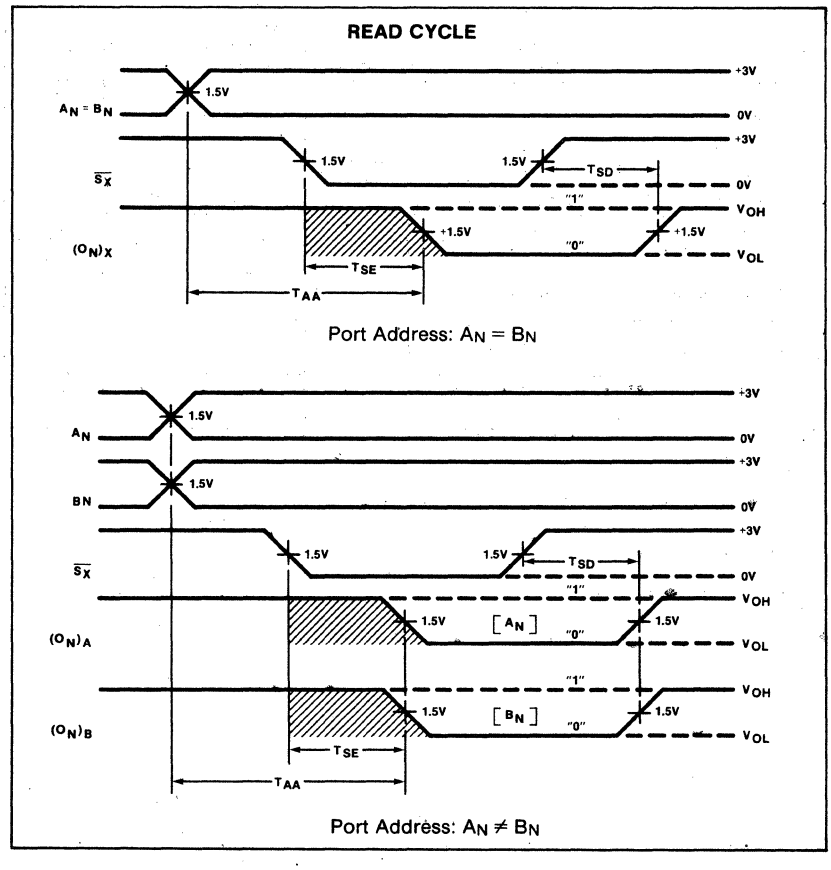


VOLTAGE WAVEFORM



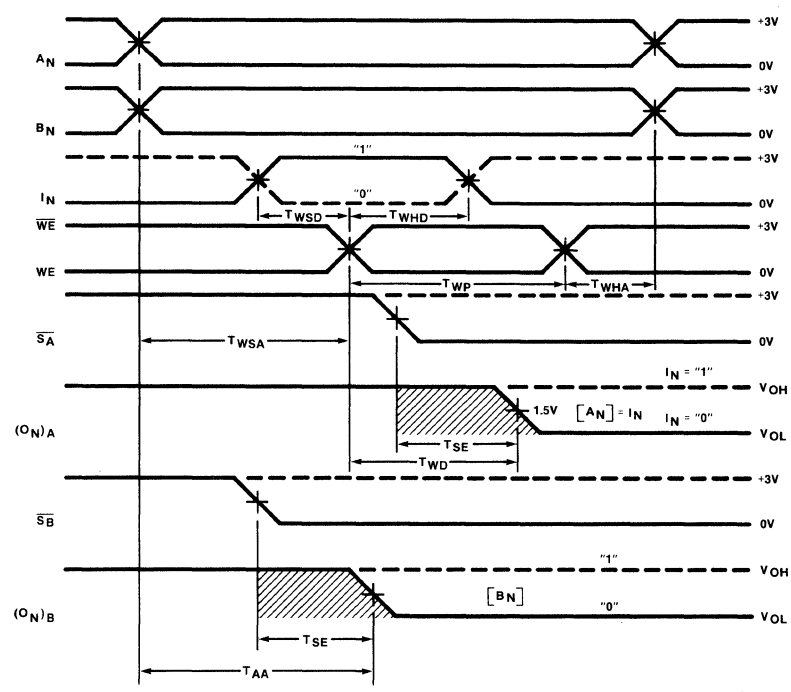
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS



TIMING DIAGRAMS (Cont'd)

SIMULTANEOUS READ/WRITE CYCLE

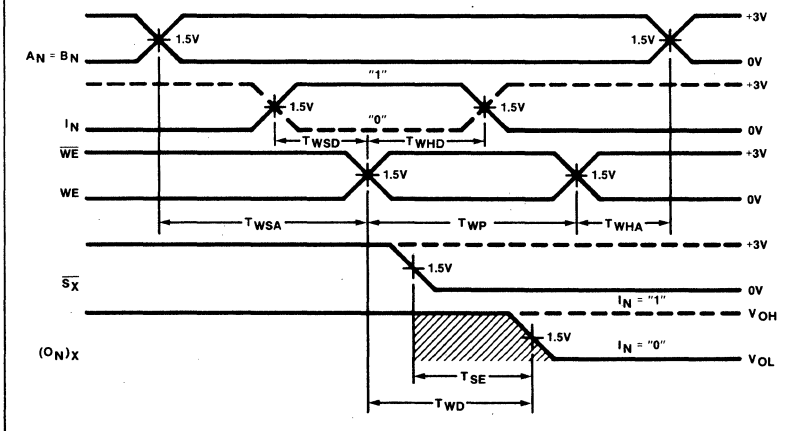


Port Address: $A_N \neq B_N$

A_N = Write

B_N = Read

PORT A WRITE CYCLE



Port Address: $A_N = B_N$

MEMORY TIMING DEFINITIONS

T_{SE}	Delay between beginning of Output Enable low (with Address valid) and when Data Output becomes valid.
T_{SD}	Delay between when Output Enable becomes high and Data Output is in Hi-Z or high state.
T_{AA}	Delay between beginning of valid Address (with Output Enable low) and when Data Output becomes valid.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects the Data Input.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature pnp inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume a logic state by the output access time and the truth table.

The family is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify the N prefix, and for the military temperature range (-55°C to +125°C) specify the S prefix. The 54/74S89/189 military temperature range product is ordered as S54S89/189. The S grade product is supplied in the F package only.

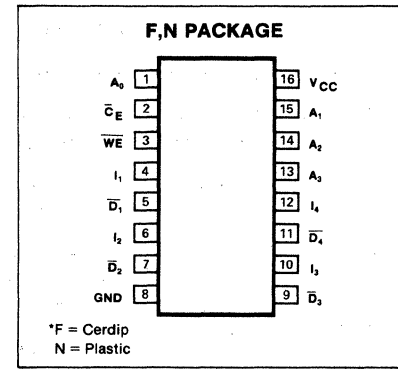
FEATURES

- **Output access time:**
  - **N82S25: 50ns**
  - **N3101A: 35ns**
  - **N54/74S89: 50ns**
  - **N54/74S189: 35ns**
- **Power dissipation: 6.25mW/bit, typ**
- **Input loading:**
  - **N grade: -100μA max**
  - **S grade: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S25: Open collector**
  - **3101A: Open collector**
  - **54/74S89: Open collector**
  - **54/74S189: Tri-state**
- **Schottky processed**
- **TTL compatible**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

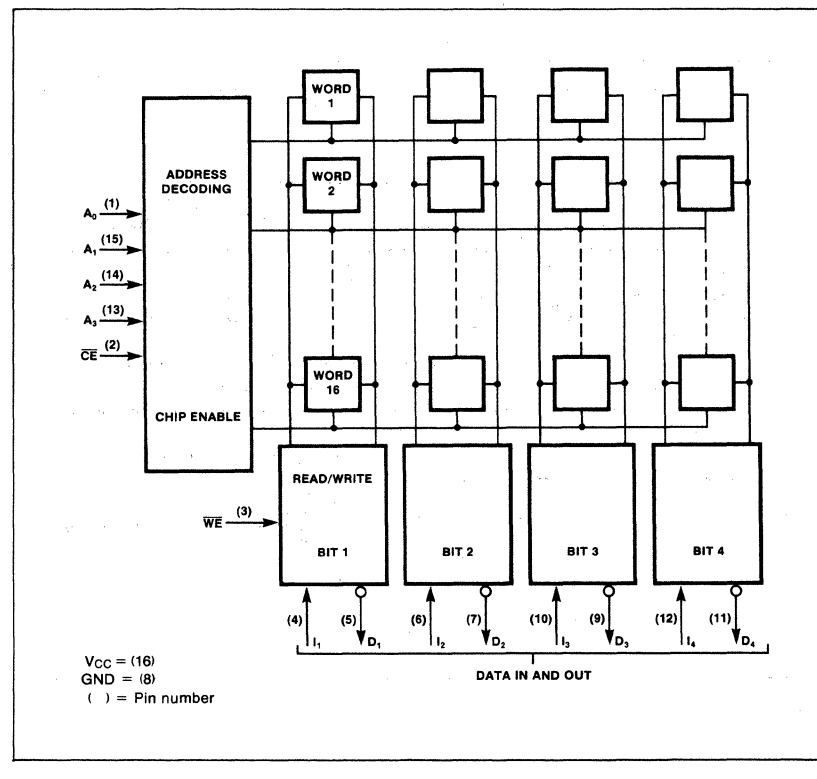
PIN CONFIGURATION



TRUTH TABLE

	$\overline{CE}$	$\overline{WE}$	D_{IN}	82S25	3101A	54/74S89	54/74S189
				DATA OUT			
Read	0	1	X	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$	$\overline{\text{Stored data}}$
Write "0"	0	0	0	1	1	1	Hi-Z
Write "1"	0	0	1	1	1	0	Hi-Z
Disable	1	X	X	1	1	1	Hi-Z

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_{OH}	Output voltage High	+5.5	Vdc
T_A	Temperature range Operating		°C
	N grade	0 to +75	
	S grade	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N GRADE			S GRADE			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp	I_{IN} = -12mA, V_{CC} = Min		-1.0	-1.5		-1.0	-1.5	
	Output voltage								V
V_{OL}	Low[3,4]	I_{OUT} = 16mA, V_{CC} = Min		0.35	0.45		0.35	0.5	
V_{OH}	High (54/74S189)	I_{OUT} = 2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V			10			25	
	Output current								
I_{OLK}	Leakage	CE = high, V_{OUT} = 5.5V, V_{CC} = Min		<1	100		<1	100	μA
I_{OS}	Short circuit (54/74S189)	V_{OUT} = 0V		-30	-100	-30		-100	mA
$I_{O(OFF)}$	Hi-Z (54/74S189)	$2.4 \ge V_{OUT} \ge 0.4V$			±50			±50	μA
I_{CC}	Supply current[4]								mA
	82S25, 54/74S89			80	105		80	120	
	3101A			80	105		80	120	
	54/74S189			80	110		80	110	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IH} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V, CE = high		8			8		

AC ELECTRICAL CHARACTERISTICS

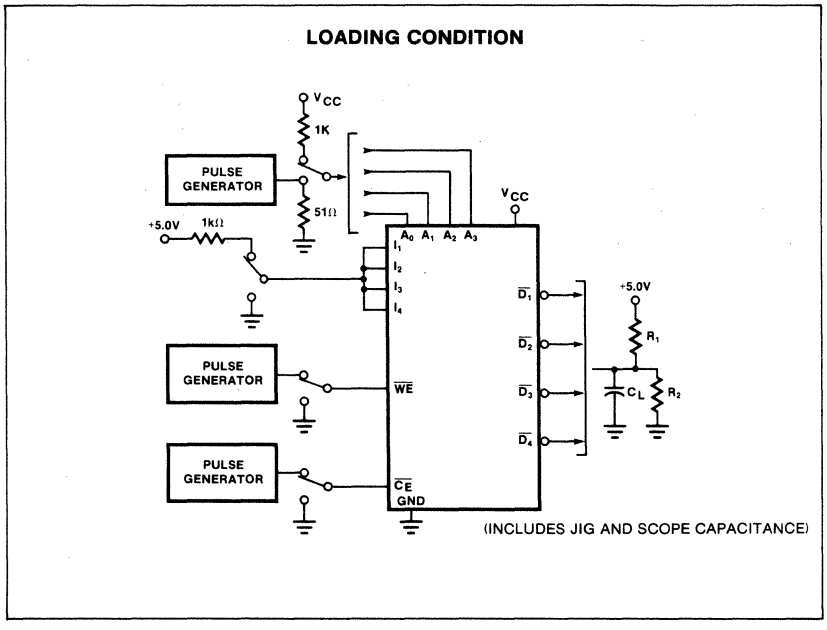
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, See ac test load
N grade: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S grade: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S25, N74S89			S82S25, S54S89			N3101A, N74S189			S3101A, S54S189			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time															ns
T_{AA}	Address				35	50		35	60		25	35		25	50	
T_{CE}	Chip enable				20	35		20	35		12	17		12	25	
T_{CD}	Disable time	Output	Chip enable		20	35		20	35		12	17		12	25	ns
T_{WD}	Response time	Output	Write enable		20	25		20	30		15	25		15	30	ns
T_{WR}	Write recovery time				35	50		35	60		22	35		22	40	ns
	Setup and hold time															ns
T_{WSA}	Setup time	Write	Address	5	-8		10	-8		0			0			
T_{WHA}	Hold time	enable		5	0		10	0		0			10			
T_{WSD}	Setup time	Write	Data in	30	15		30	15		25			30			
T_{WHD}	Hold time	enable		5	-3		10	-3		0			10			
T_{WSC}	Setup time	Write	$\overline{CE}$	0	-5		0	-5		0			0			
T_{WHC}	Hold time	enable		5	0		5	0		0			0			
	Pulse width															ns
T_{WP}	Write enable[5]			30	18		30	18		25			30	1		

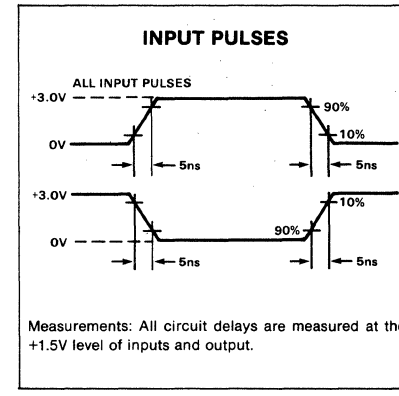
NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25°C$.
3. Output sink current is supplied through a resistor to V_{CC}.
4. All sense outputs in low state.
5. To guarantee a Write into the slowest bit.
6. Positive current is defined as into the terminal referenced.
7. Positive logic definition: high ≈ +5.0V, low ≈ GND.
8. Test each input one at a time.

TEST LOAD CIRCUIT



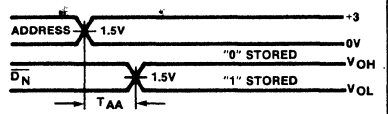
VOLTAGE WAVEFORM



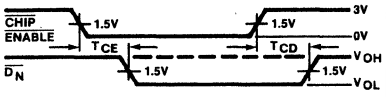
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS

READ CYCLE

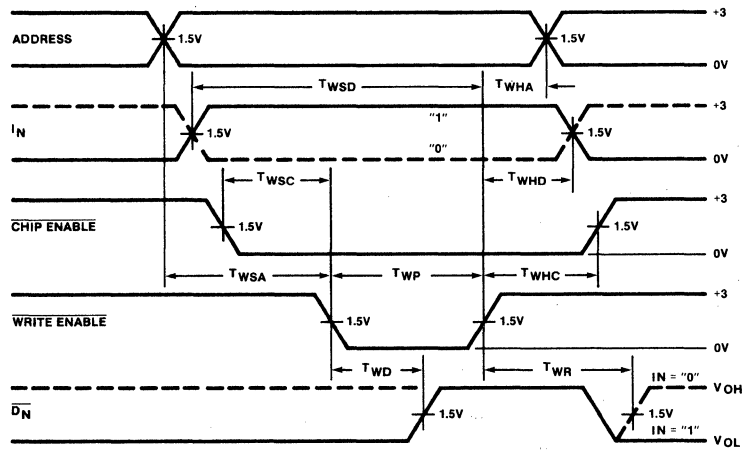


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



BIPOLAR MEMORY

82S21-F,N

DESCRIPTION

The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5-input decoder when the chip enable input, CE is at logic high. $\overline{WS_0}$ and $\overline{WS_1}$ are the write select inputs for the bit 0 and bit 1 of the word selected. $\overline{WE}$ is the write control input. When $\overline{WS_N}$ and $\overline{WE}$ are both at logic low data on the DI_0 and DI_1 data lines are written into the addressed word. The read function is enabled when either $\overline{WS_N}$ or $\overline{WE}$ is at logic high.

An internal latch provides the Write-While-Read capability. When the latch control line (strobe) is logic high and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When strobe goes from a logic high to logic low, the outputs are latched and will remain latched regardless of the state of any other address or control line. When strobe goes from low to high, the outputs unlatch and will assume the contents of the present address word.

FEATURES

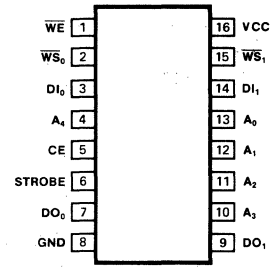
- **Address access time: 50ns max**
- **Write cycle time:**
  Transparent mode: 45ns max
  Latched mode: 60ns max
- **Power dissipation: 7.5mW/bit typ**
- **32mA output sink capability**
- **On-chip output latches**
- **Bit masking control lines**
- **Write-While-Read function**
- **Non-inverting open collector outputs**
- **TTL compatible**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Accumulator register**
- **Control store**

PIN CONFIGURATION

F,N PACKAGE



*F = Cerdip
N = Plastic

TRUTH TABLE

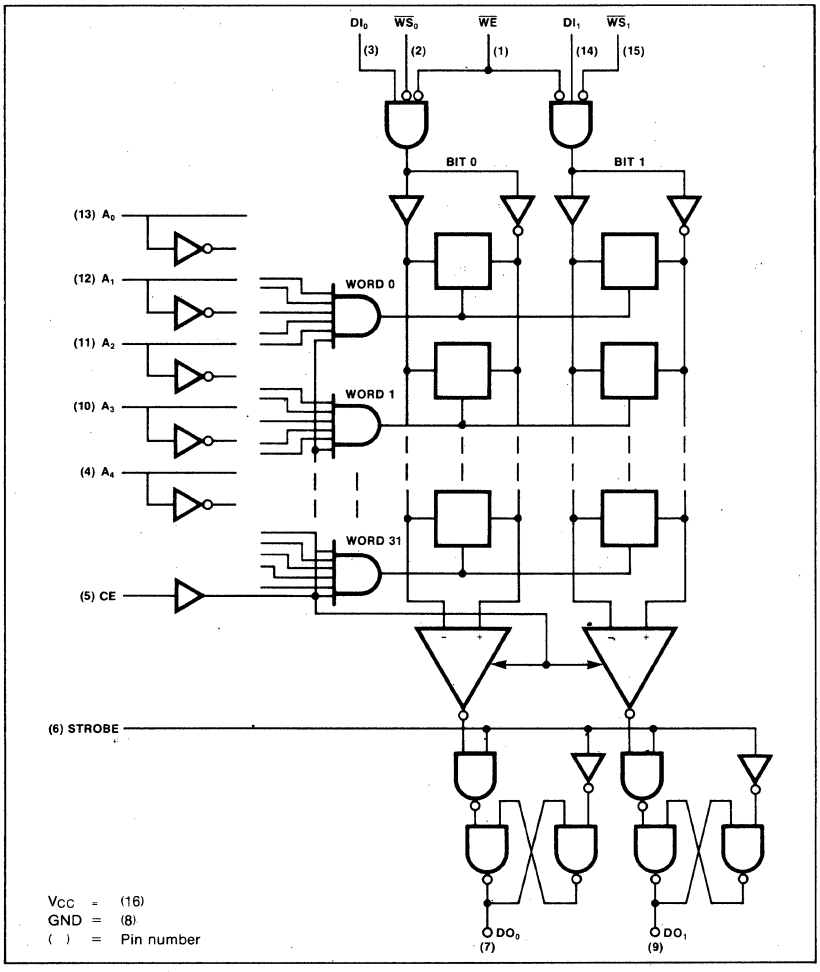
CE	$\overline{WE}$	$\overline{WS_0}$	$\overline{WS_1}$	STROBE	MODE	OUTPUTS
X	X	X	X	0	Output hold	$DO_N = (A_M)$ at last CE = high
0	X	X	X	0	Disabled	DO_N = high
1	1	X	X	1 or ↓	Read (transparent/latched)	$DO_N = (A_M)$
1	0	1	1	1 or ↓	Read (transparent/latched)	
1	0	0	0	0	Write data	$DO_N = (A_M)$ at last strobe = ↓
1	0	0	0	1	Write data	$DO_N = DI_N$
1	0	0	1	X	Write data into bit 0 only	If strobe = low: $DO_N = (A_M)$ at last strobe = ↓ If strobe = high: $DO_N = DI_N$ or (A_M) as per $\overline{WS_N}$
1	0	1	0	X	Write data into bit 1 only	

( ) = Contents of
↓ = High → low transition

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_{OH}	Output voltage	+5.5	Vdc
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER[1]		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low[1]	V_{CC} = 4.75V			0.85	
V_{IH}	High[1]	V_{CC} =5.25V	2			
V_{IC}	Clamp[1,3]	V_{CC} = 4.75V, I_{IN} = -18mA		-0.8	-1.2	
	Output voltage					V
V_{OL}	Low[1,4]	V_{CC} = 4.75V, I_{OL} = 32mA		0.35	0.45	
	Input current					
I_{IL}	Low	V_{IN} = 0.45V			-1.6	mA
I_{IH}	High	V_{IN} = 5.5V		<1	25	μA
	Output current	V_{CC} = 5.25V				μA
I_{OLK}	Leakage[5]	V_{OUT} = 5.25V		1	40	
I_{CC}	V_{CC} supply current[6]	V_{CC} = 5.25V		100	130	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 150\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ[2]	Max	
Access time							ns
T_{AA} Address	Output	Address	Latched or transparent read		40	50	
T_{CE} Chip enable	Output	Chip enable			40	50	
Disable time							ns
T_{CD} Chip enable	Output	Chip enable	Latched or transparent read		40	50	
Setup and hold time							ns
T_{WSA} Setup time	Write	Address	Latched or transparent write	15	10		
T_{WHA} Hold time				5	0		
T_{WSD} Setup time	Write	Data in	Latched or transparent write	25			
T_{WHD} Hold time				5	0		
T_{WSC} Setup time	Write	CE	Latched or transparent write	15	10		
T_{WHC} Hold time				5	0		
T_{CES} Setup time	Strobe	Chip enable	Latched read	50	40		
T_{CEH} Hold time				5	0		
T_{ADH} Hold time	Output	Address	Latched read	5	0		
Pulse width							ns
T_{SW} Strobe			Latched read	30			
T_{WP} Write inputs			Latched or transparent write	25			
Latch time							ns
T_{SLR} Read strobe	Strobe	Address	Latched read	50	40		
T_{SLW} Write strobe	Strobe	Write	Latched write	40	30		
T_{LRW} WWR strobe	Write	Strobe	Write while read	10	5		
Delatch time							ns
T_{DL} Strobe	Output	Strobe	Latched read		20	25	
T_{WD} Valid time	Output	Write	Latched or transparent write		30	40	ns

NOTES
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. Test each input one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to CE, and V_{IH} to strobe.
6. I_{CC} is measured with all inputs at 4.5V, and the outputs open.

MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable high (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes low and Data Output is in high state.

T_{AA} Delay between beginning of valid Address (with Chip Enable high) and when Data Output becomes valid.

T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.

T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.

T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.

T_{WSD} Required delay between beginning of valid Data Input and end of Write Enable pulse.

T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.

T_{WP} Width of Write Enable pulse.

T_{WD} Delay between beginning of Write Enable pulse and when Data Output reflects the contents of the Data Input.

T_{CES} Minimum delay between leading edge of Chip Enable and trailing edge of Strobe, for latching valid output data.

T_{CEH} Required delay between trailing edge of Strobe and end of Chip Enable, for latching valid output data.

T_{SLR} Minimum delay between Address valid time and trailing edge of Strobe, for latching valid output data.

T_{SW} Minimum width of Strobe pulse required to update contents of output data latches.

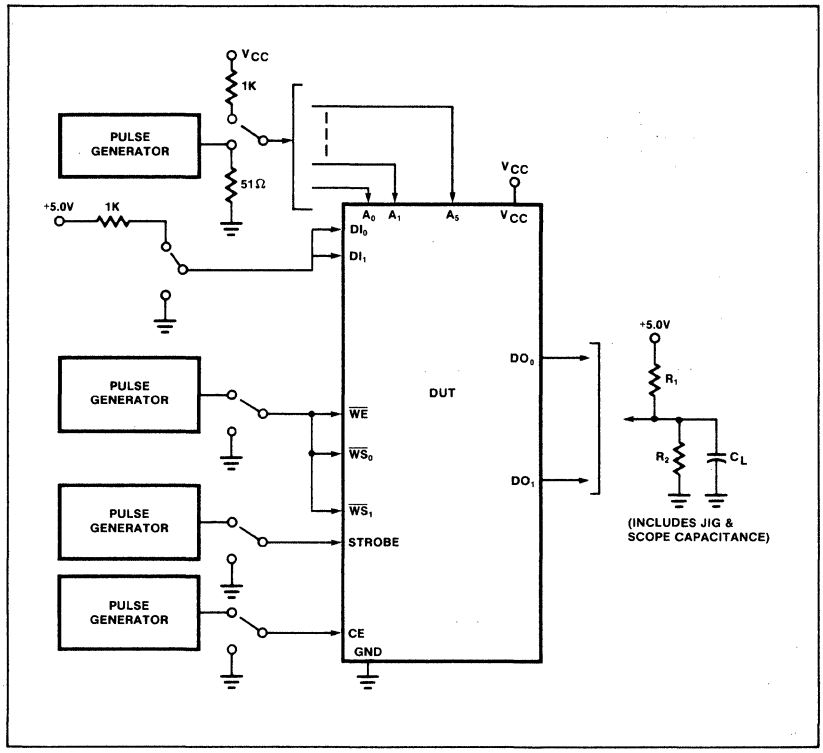
T_{ADH} Required delay between trailing edge of Strobe and end of valid Address.

T_{DL} Delay between leading edge of Strobe and when output data latches are released.

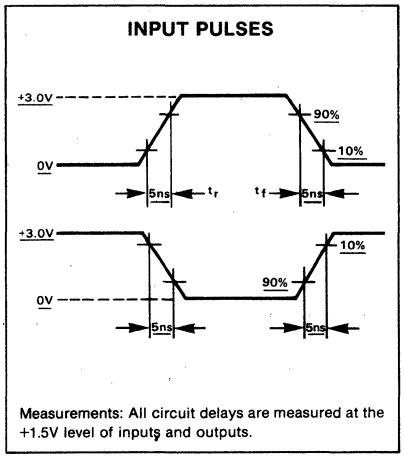
T_{LRW} Minimum delay required between trailing edge of Strobe and leading edges of Write Enable or Write Select for latching old output data (being read) while new data is being written (at the same address).

T_{SLW} Minimum delay between leading edge of Write Enable or Write Select and trailing edge of Strobe for latching data being written in output data latches.

TEST LOAD CIRCUIT

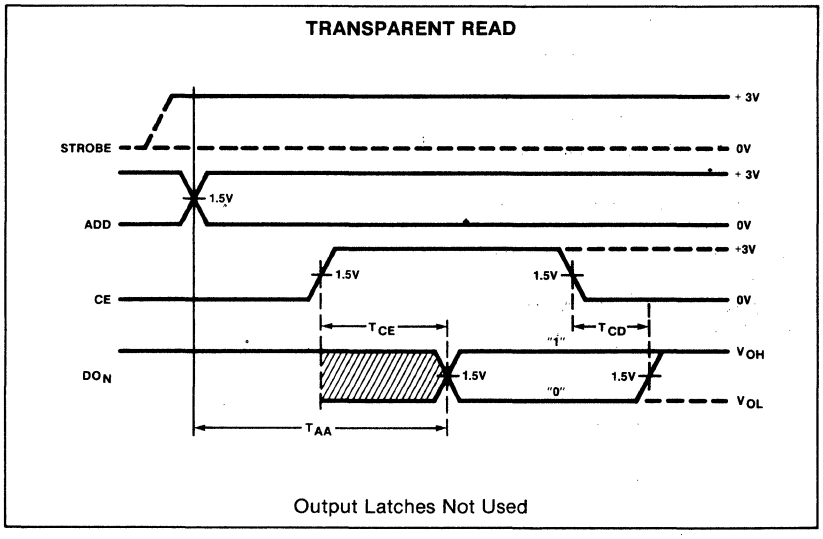


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

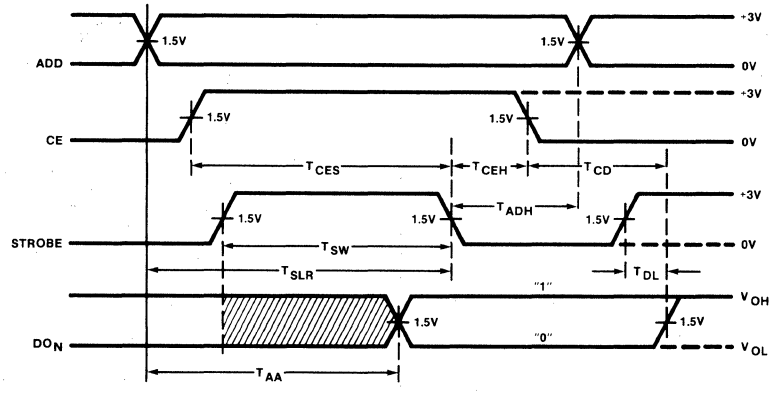
TIMING DIAGRAMS



Output Latches Not Used

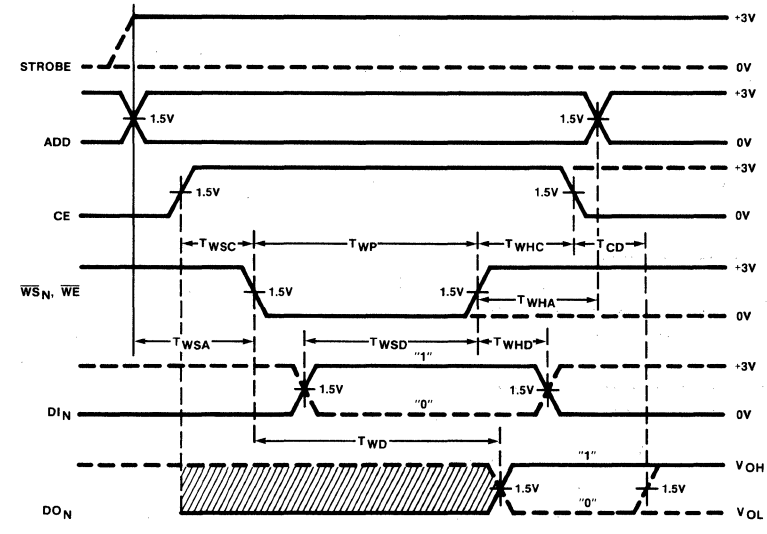
TIMING DIAGRAMS (Cont'd)

LATCHED READ



Output Latches Used

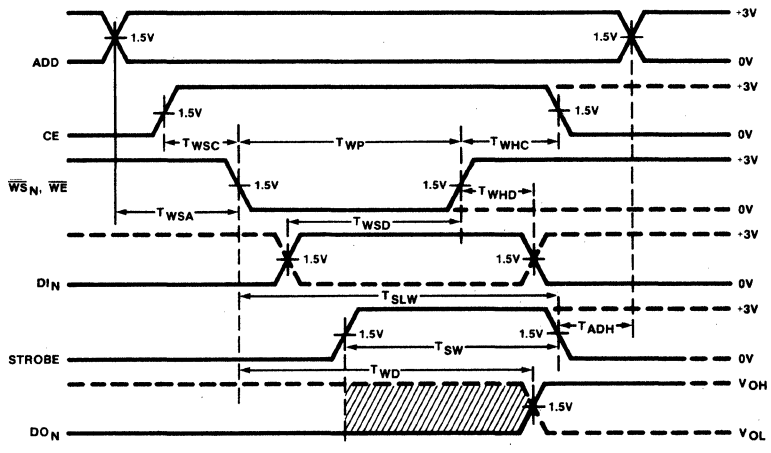
TRANSPARENT WRITE



Output Latches Not Used

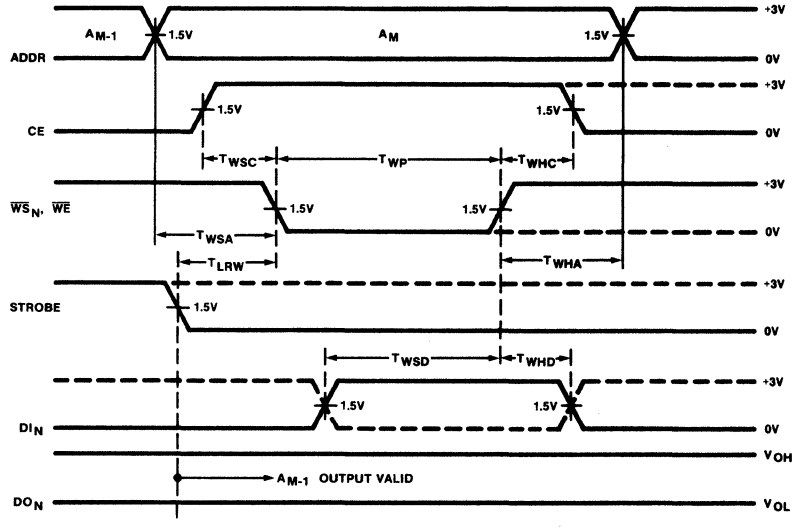
TIMING DIAGRAMS (Cont'd)

LATCHED WRITE



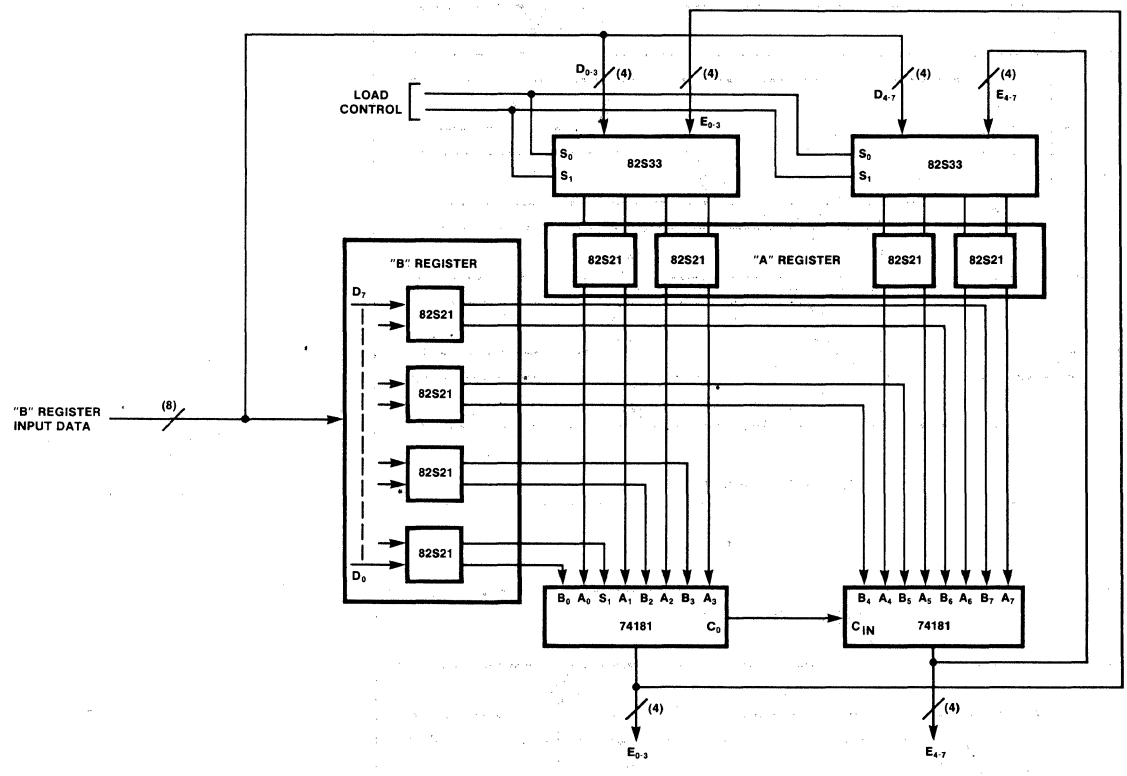
Output Latches Used

WRITE-WHILE-READ



TYPICAL APPLICATION

BASIC 8-BIT FULLY BUFFERED ACCUMULATOR



By use of the control lines S_0 and S_1 data is loaded into the "A" register through inputs D_X or from the outputs of the 74181's (E_X) to the 82S33's and stored in the 82S21's organized as a 32X8 RAM register. Data is loaded directly into the "B" register. With this arrangement, the function A+B → A (A plus B into A) can be performed in 70ns, typically, starting from data stored in the 82S21's.

DESCRIPTION

The 82S16/116 and 82S17/117 are read/write memory arrays which feature either open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors which reduce input loading to 25μA for a high level, and –100μA for a low level.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write-Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

Both devices have fast read access and write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

All devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82S16/116/17/117, F or N. The 82S16 and 82S17 are also available in the military temperature range (–55°C to +125°C) and are specified as S82S16/17.

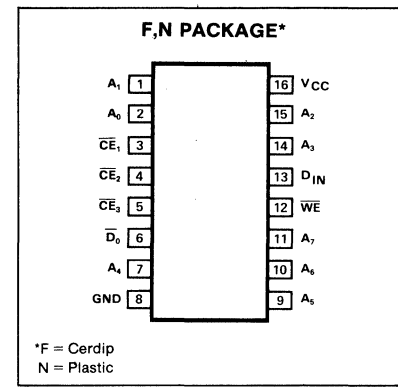
FEATURES

- **Address access time:**
  82S116/117: 40ns max
- **Write cycle time:**
  82S116/117: 25ns max
- **Power dissipation: 1.5mW/bit typ**
- **Input loading:**
  N82S116/117: –100μA
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Output option:**
  82S16/116: Tri-state
  82S17/117: Open collector
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION



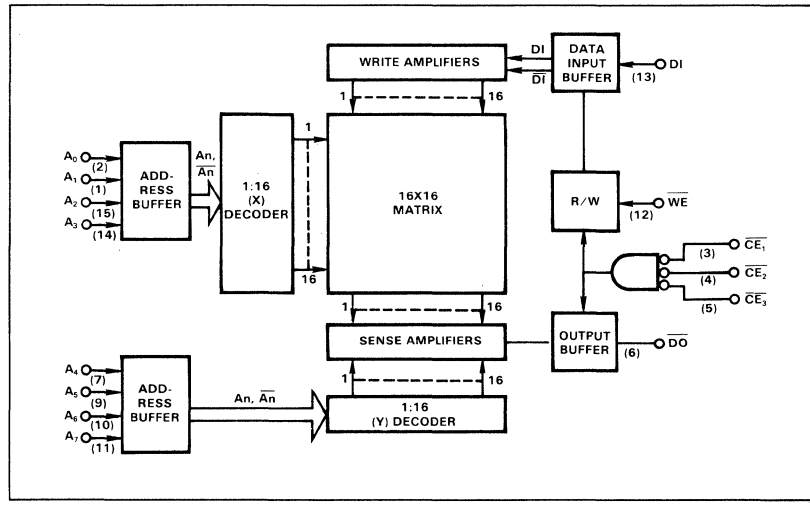
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	
				82S16/116	82S17/117
Read	0	1	X	Stored $\overline{data}$	Stored $\overline{data}$
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	0
Diasabled	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage	+5.5	Vdc
V_{OUT}	High (82S17)		
V_O	Off-state (82S16)		
	Temperature range		°C
T_A	Operating		
	S82S16/17	-55 to + 125	
	N82S16/17, N82S116/117	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S116/117, N82S16/17: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S16/17: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS	N82S16/17/116/117			S82S16/17			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage[2]								V
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage[2]	V_{CC}= Min							V
V_{OH}	High (82S16/116)[4]	I_{OH} = -3.2mA	2.6			2.4			
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45		0.35	0.5	
	Input current[3]	V_{CC} = Max							mA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-250	
	Output current								
I_{OLK}	Leakage (82S17/117)[6]	V_{OUT} = 5.5V		1	40		1	40	μA
$I_{O(OFF)}$	Hi-Z state (82S16/116)[6]	V_{OUT} = 5.5V		1	40		1	50	μA
		V_{OUT} = 0.45V		-1	-40		-1	-50	
I_{OS}	Short-circuit (82S16/116)[7]	V_{CC} = Max, V_O = 0V	-20		-70	-20		-70	μA
I_{CC}	V_{CC} supply current	V_{CC} = Max		80	115		80	120	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S116/117, N82S16/17: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S16/17: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

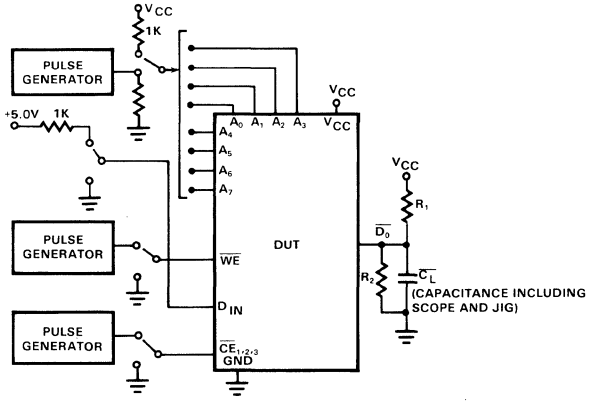
PARAMETER		TO	FROM	N82S16/17			N82S116/117			S82S16/17			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time												ns
T_{AA}	Address				40	50		30	40		40	70	
T_{CE}	Chip enable				30	40		15	25		30	40	
T_{CD}	Disable time	Output	Chip enable		30	40		15	25		30	40	ns
T_{WD}	Valid time	Output	Write enable		30	40		30	40		30	55	ns
	Setup and hold time												ns
T_{WSA}	Setup time	Write enable	Address	20	5		0	-5		20	5		
T_{WHA}	Hold time			5	0		0	-5		10	0		
T_{WSD}	Setup time	Write enable	Data in	40	30		25	15		50	40		
T_{WHD}	Hold time			5	0		0	-5		10	0		
T_{WSC}	Setup time	Write enable	$\overline{CE}$	10	0		0	-5		10	0		
T_{WHC}	Hold time			5	0		0	-5		10	0		
	Pulse width												ns
T_{WP}	Write enable[8]			30	15		25	15		40	20		

NOTES

1. All typical values are at $V_{CC} = 5V$, T_A +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at the time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.

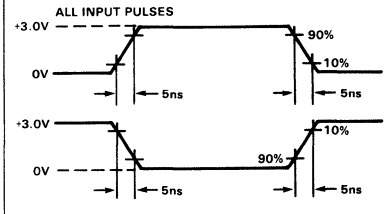
TEST LOAD CIRCUIT

LOADING CONDITION



VOLTAGE WAVEFORM

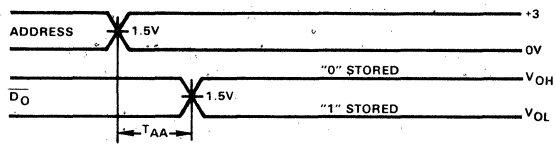
INPUT PULSES



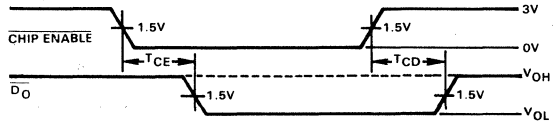
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS

READ CYCLE

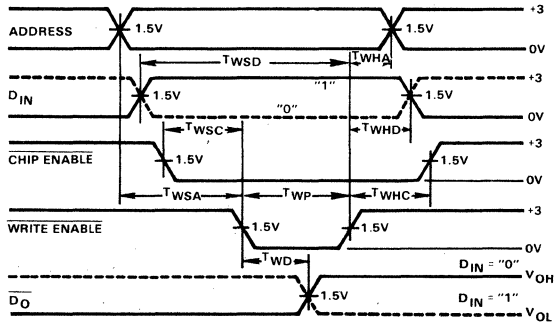


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The 54/74S200/201 and 54/74S301 are read/write memory arrays which feature either open collector or tri-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and pnp input transistors, which reduces input loading to 25μA for a high level and -250μA (S54S200/201/301) or -100μA (N74S200/201/301) for a low level.

The additional feature of output blanking during Write ($\overline{D}_O$ terminal "H" or "Hi-Z" state) permits $\overline{D}_O$ and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast read access and write cycle times, and thus are ideally suited in high speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

They are available in both the commercial and military temperature ranges. The commercial temperature range (0°C to +75°C) is specified as N74S200/201/301, F or N, and the military temperature range (-55°C to +125°C) is specified as S54S200/201/301, F only.

FEATURES

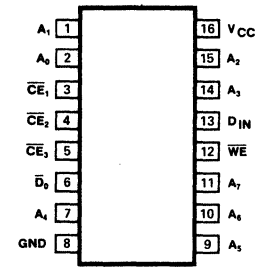
- **Address access time:**
  N74S200/201/301: 50ns max
  S54S200/201/301: 70ns max
- **Write cycle time:**
  N74S200/201/301: 50ns max
  S54S200/201/301: 60ns max
- **Power dissipation : 1.5mW/bit typ**
- **Input loading:**
  N74S200/201/301: -100μA max
  S54S200/201/301: -250μA max
- **Output blanking during Write**
- **On-chip address decoding**
- **Output option:**
  54/74S200/201: Tri-state
  54/74S301: Open collector
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION

F,N PACKAGE*



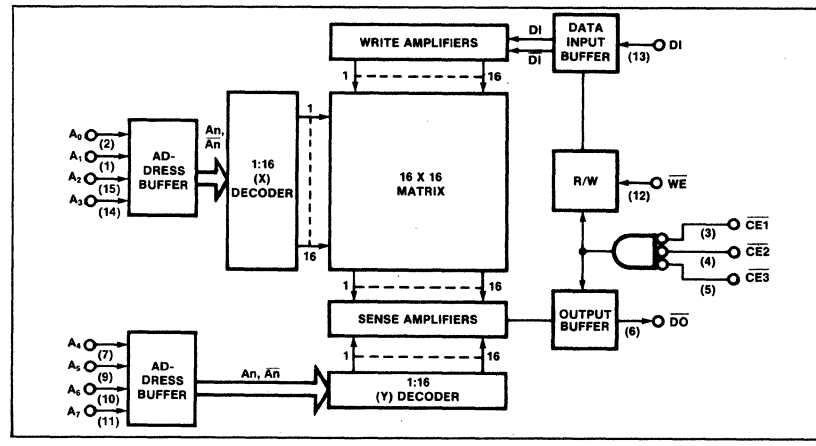
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D}_{OUT}$	
				54/74S301	54/74S200/201
Read	0	1	X	Stored $\overline{Data}$	Stored $\overline{Data}$
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

*"0" = All $\overline{CE}$ inputs low; "1" = One or more $\overline{CE}$ inputs high.
X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OUT}	High (54/74S301)	+5.5	
V_O	Off-state (54/74S200/201)	+5.5	
	Temperature range		°C
T_A	Operating		
	N74S200/201/301	0 to +70	
	S54S200/201/301	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N74S200/201/301: $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$

S54S200/201/301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N74S200/201/301			S54S200/201/301			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low[2]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[2]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp [2,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[2,4]	I_{OL} = 16mA		0.35	0.45		0.30	0.50	
V_{OH}	High (N74S200/201)[2,5]	I_{OH} = 10.3mA	2.4						
V_{OH}	High (S54200/201)[2,5]	I_{OH} = -5.2mA				2.4			
	Input current[3]	V_{CC} = Max							
I_I	At V_{IN} Max	V_{IN} = 5.5V			1			1	mA
I_{IL}	Low	V_{IL} = 0.45V		-10	-100		-10	-250	μA
I_{IH}	High	V_{IH} = 2.7V		1	25		1	25	μA
	Output current								
I_{OLK}	Leakage (54/74S301)[6]	V_{IH} = 2V, V_O = 5.5V		1	40		1	50	μA
$I_{O(OFF)}$	Hi-Z state (54/74S200/201)[6]	V_{CC} = Max, V_O = 5.5V		1	40		1	100	μA
		V_{IH} = 2V, V_O = 0.4V		-1	-40		-1	-100	
I_{OS}	Short circuit (54/74S200/201)[7]	V_{CC} = Max, V_O = 0V	-30		-100	-30		-100	mA
I_{CC}	V_{CC} supply current[8]	V_{CC}= Max		80	130		80	130	mA
		V_{CC} = Max, T_A = +125°C						99	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_L = 270\Omega$, $C_L = 15pF$, See ac test load

N74S200/201/301: $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$

S54S200/201/301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[9]		TO	FROM	TEST CONDITIONS	N74S200/201			S54S200/201			UNIT
					Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time [B,D,E]										ns
t_{PLH}	Low to high		Address			40	50		40	70	
t_{PHL}	High to low										
t_{PLH}	Low to high		Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
	Enable time										ns
t_{ZL}	Low [C,D,F,G]	Output	Chip enable				35			45	
t_{ZH}	High [C,D,F,G]										
t_{PHL}	High to low [C,D,E]	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
	Disable time										ns
t_{LZ}	Low [C,D,F,G]	Output	Chip enable	$C_L=5pF$			20			30	
t_{HZ}	High [C,D,F,G]										
t_{PLH}	Low to high [C,D,E]	Output	Chip enable Write enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
t_{PHL}	High to low [C,D,E]										
t_{LZ}	Low [D,G]	Output	Write enable	$C_L=5pF$			30			40	
t_{HZ}	High [D,G]										
	Sense recovery time										ns
t_{ZL}	Low [D,F]						40			50	
t_{ZH}	High [D,F]										
t_{SR}	Sense [D]										
	Pulse width [H]										ns
t_W	Write enable			$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			
	Setup and hold time [D]										ns
t_S	Setup time	Write enable	Address		0			0			
t_H	Hold time	Address	Write enable		10			10			
t_S	Setup time	Write enable	Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
t_H	Hold time	Address	Write enable								
t_S	Setup time	Write enable	Data		40			50			
t_H	Hold time	Data	Write enable		10			10			
t_S	Setup time	Write enable	Data	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
t_H	Hold time	Data	Write enable								
t_S	Setup time	Write enable	Chip enable		0			0			
t_H	Hold time	Chip enable	Write enable		0			0			
t_S	Setup time	Write enable	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$							
t_H	Hold time	Chip enable	Write enable								

AC ELECTRICAL CHARACTERISTICS

(Cont'd) $R_L = 270\Omega$, $C_L = 15pF$, See ac test load
N74S200/201/301: $0°C \le T_A \le +70°C$, $4.75V \le V_{CC} \le 5.25V$
S54S200/201/301: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

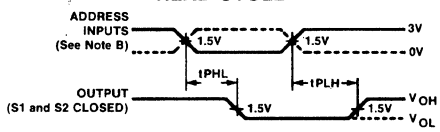
PARAMETER[9]		TO	FROM	TEST CONDITIONS	N74S301			S54S301			UNIT
					Min	Typ[1]	Max	Min	Typ	Max	
	Access time [B,D,E]										ns
t_{PLH}	Low to high		Address								
t_{PHL}	High to low										
t_{PLH}	Low to high		Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$		40	50		40	70	
	Enable time										ns
t_{ZL}	Low [C,D,F,G]	Output	Chip enable								
t_{ZH}	High [C,D,F,G]										
t_{PHL}	High to low [C,D,E]	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$			35			45	
	Disable time										ns
t_{LZ}	Low [C,D,F,G]	Output	Chip enable	$C_L=5pF$							
t_{HZ}	High [C,D,F,G]										
t_{PLH}	Low to high [C,D,E]	Output	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$			20			30	
t_{PHL}	High to low [C,D,E]		Write enable				30			40	
t_{LZ}	Low [D,G]	Output	Write enable	$C_L=5pF$							
t_{HZ}	High [D,G]										
	Sense recovery time										ns
t_{ZL}	Low [D,F]										
t_{ZH}	High [D,F]										
t_{SR}	Sense [D]						40			50	
	Pulse width [H]										ns
t_W	Write enable			$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			
	Setup and hold time [D]										ns
t_S	Setup time	Write enable	Address								
t_H	Hold time	Address	Write enable								
t_S	Setup time	Write enable	Address	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	0			0			
t_H	Hold time	Address	Write enable		10			10			
t_S	Setup time	Write enable	Data								
t_H	Hold time	Data	Write enable								
t_S	Setup time	Write enable	Data	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	40			50			
t_H	Hold time	Data	Write enable		10			10			
t_S	Setup time	Write enable	Chip enable								
t_H	Hold time	Chip enable	Write enable								
t_S	Setup time	Write enable	Chip enable	$R_{L1}=270\Omega$, $R_{L2}=1k\Omega$	0			0			
t_H	Hold time	Chip enable	Write enable		0			0			

NOTES

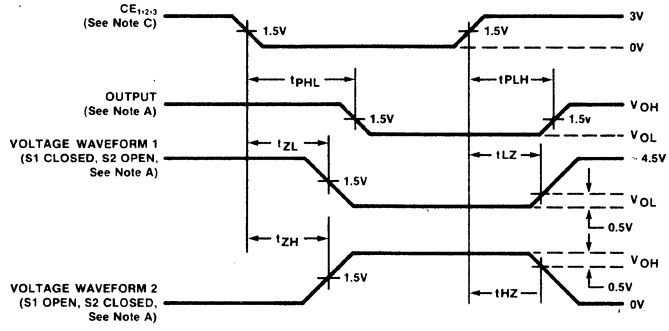
1. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with logic stored, and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. See timing diagram notes.

TIMING DIAGRAMS

READ CYCLE

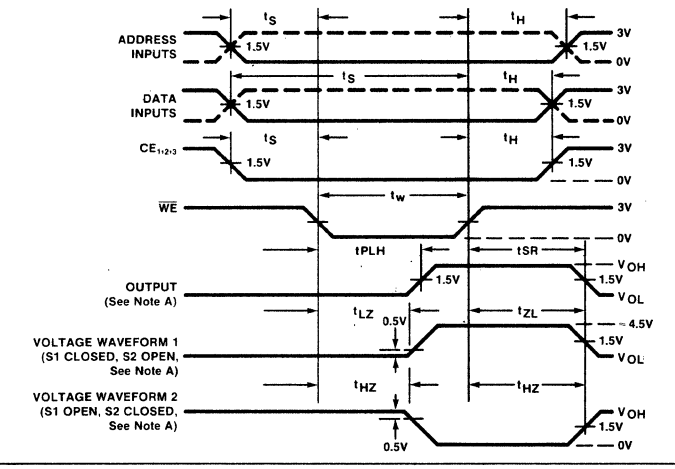


Address Time From Address



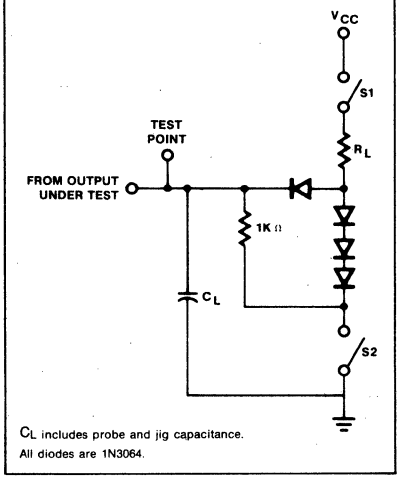
Chip Enable and Disable Time

WRITE CYCLE



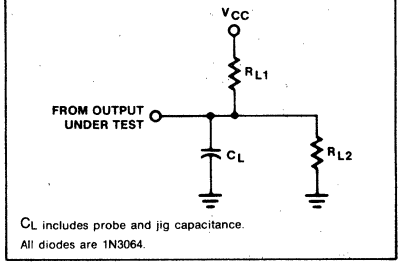
TEST LOAD CIRCUITS

54/74S200/201



CL includes probe and jig capacitance.
All diodes are 1N3064.

54/74S301



CL includes probe and jig capacitance.
All diodes are 1N3064.

NOTES

A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ns, $t_f \leq 2.5$ns, PRR ≤ 1MHz, and $Z_{OUT} \approx 50\Omega$.
E. t_{PLH} propagation delay time, low-to-high level output, t_{PHL} propagation delay time, high-to-low level output.
F. t_{ZH} propagation delay time, Hi-Z to high level output, t_{ZL} propagation delay time, Hi-Z to low level output.
G. T_{HZ} propagation delay time, high level to Hi-Z output, t_{LZ} propagation delay time, low level to Hi-Z output.
H. Minimum required to guarantee a Write into the slowest bit.

82S09-I,N

DESCRIPTION

The organization of this device allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09 features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the logic state of the device output follows the complement of the data input being written. This feature allows faster execution of Write-Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

The 82S09 is available in the commercial and military temperature ranges. For the commercial temperature ranges. (0°C to +75°C) specify N82S09, and for the military temperature range (-55°C to +125°C) specify S82S09.

FEATURES

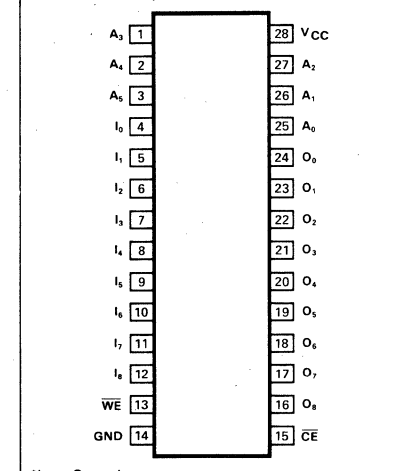
- **Address access time:**
  N82S09: 45ns max
  S82S09: 80ns max
- **Write cycle time:**
  N82S09: 45ns max
  S82S09: 75ns max
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  N82S09: -100μA max
  S82S09: -150μA max
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

PIN CONFIGURATION

I,N PACKAGE*



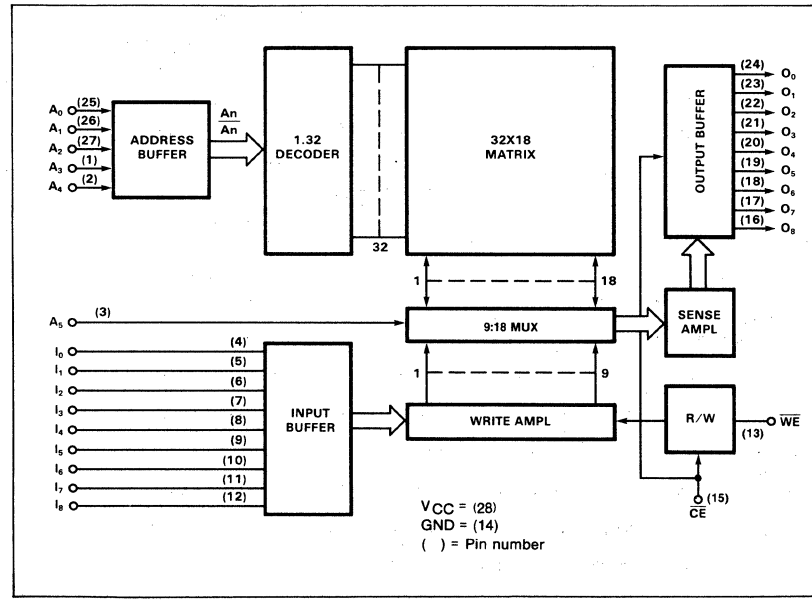
*I = Ceramic
N = Plastic

TRUTH TABLE

MODE	CE	WE	I_N	O_N
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	1

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S10)	+5.5	
T_A	Temperature range		°C
	Operating		
	N82S09	0 to +75	
	S82S09	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS[1]

N82S09: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82S09: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER[1]		TEST CONDITONS	N82S09			S82S09			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.2			
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5		-1.0	-1.5	
	Output voltage								V
V_{OL}	Low[4]	V_{CC} = Min, I_{OL} = 6.4mA		0.35	0.5		0.35	0.5	
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		1	25		1	40	
	Output current								μA
I_{OLK}	Leakage[5]	V_{CC} = Max, V_{OUT} = 5.5V		1	40		1	60	
I_{CC}	V_{CC} supply current[6]	V_{CC} = Max		150	190		150	200	mA
	Capacitance	V_{CC} =5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

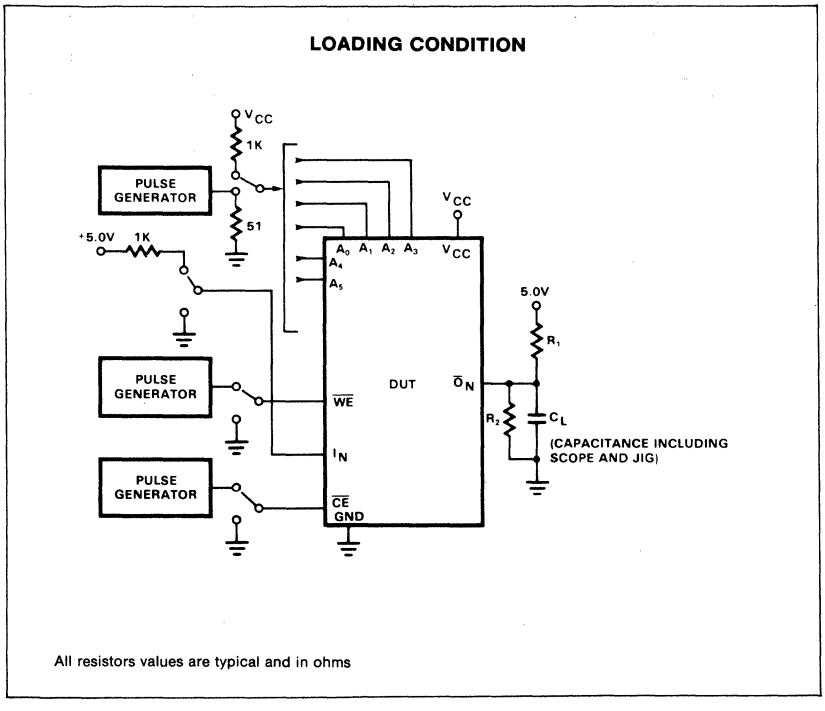
$R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30pF$, See ac test load
N82S09: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S09: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TO	FROM	N82S09			S82S09			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}	Address				30	45		30	80	
T_{CE}	Chip enable				15	30		15	50	
T_{CD}	Disable time	Output	Chip enable		15	30		15	50	ns
T_{WD}	Valid time	Output	Write enable		25	50		25	80	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	5	0		10	0		
T_{WHA}	Hold time									
T_{WSD}	Setup time	Write enable	Data in	35	25		50	25		
T_{WHD}	Hold time			5	0		5	0		
T_{WSC}	Setup time	Write enable	CE	5	0		10	0		
T_{WHC}	Hold time									
	Pulse width									ns
T_{WP}	Write enable			35	25		50	25		

NOTES

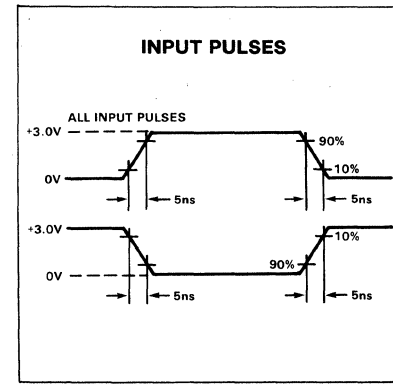
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Test each input one at a time.
4. Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IH} applied to $\overline{CE}$.
6. I_{CC} is measured with the write enable and memory enable input grounded, all other inputs at 4.5V, and the outputs open.
7. Minimum required to guarantee a Write into the slowest bit.
8. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TEST LOAD CIRCUIT



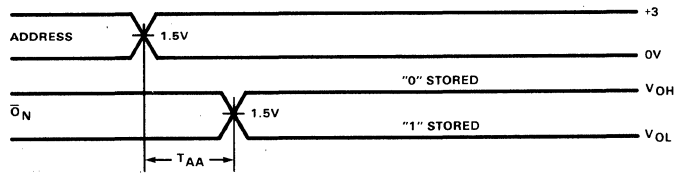
All resistors values are typical and in ohms

VOLTAGE WAVEFORM

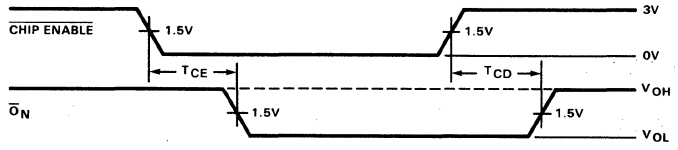


TIMING DIAGRAMS

READ CYCLE

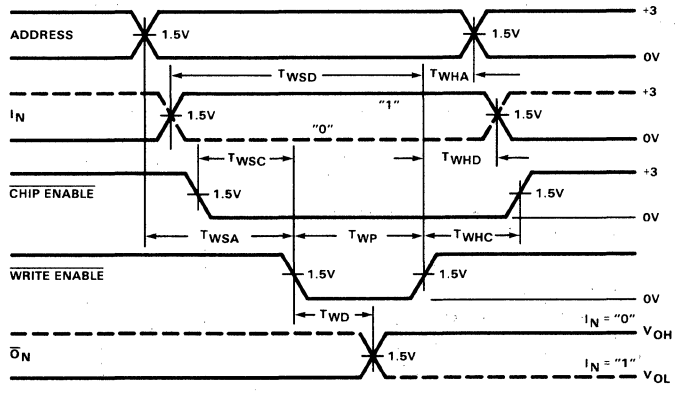


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output reflects complement of Data Input.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The 82S10/11, with a typical access time of 30ns, is ideal for cache buffer applications and for systems requiring very high speed main memory.

The 82S10/11 family requires single +5V power supply and features very low current pnp input structures. They include on-chip decoding and a chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

All devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82S10/110/11/111. The 82S10 and 82S11 are also available in the military temperature range (-55°C to +125°C) and are specified as S82S10/11.

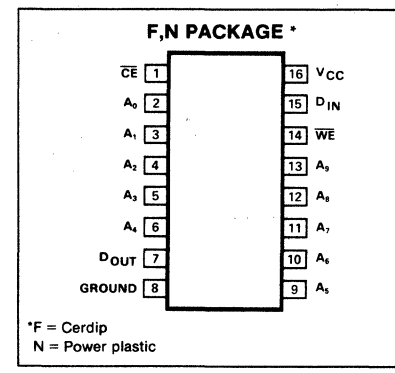
FEATURES

- **Address access time:**
  N82S10/11: 45ns max
  S82S10/11: 70ns max
  N82S110/111: 35ns max
- **Write cycle time:**
  N82S10/11: 45ns max
  S82S10/11: 75ns max
  N82S110/111: 40ns max
- **Power dissipation: 0.5W/bit typ**
- **Input loading:**
  N82S10/11: -250μA max
  S82S10/11: -250μA max
  N82S110/111: -250μA max
- **Output options:**
  82S10/110: Open collector
  82S11/111: Tri-state
- **On-chip address decoding**
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

APPLICATIONS

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION



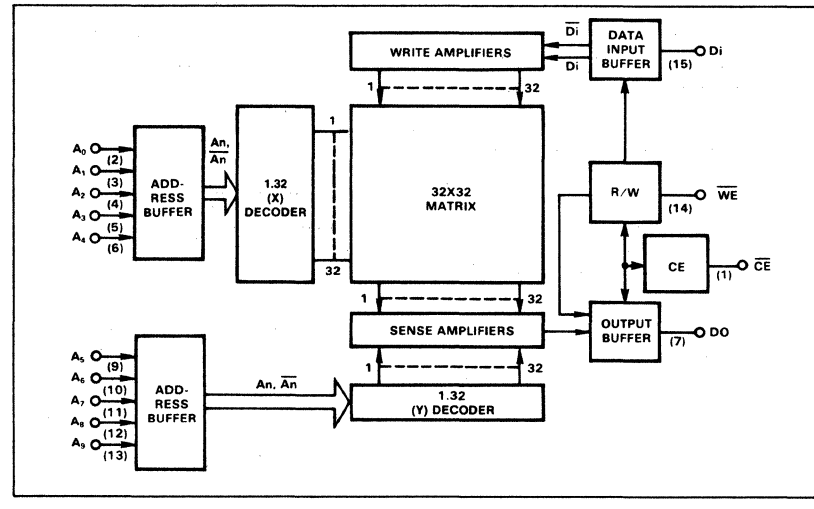
*F = Cerdip
N = Power plastic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D	D_{OUT}	
				82S10/110	82S11/111
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S10/110)	+5.5	
V_O	Off-state (82S11/111)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S10/11/110/111	0 to +75	
	S82S10/11	−55 to +125	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS[2]

N82S10/110/11/111: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S10/11: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S10/11/110/111			S82S10/11			UNIT
			Min	Typ[3]	Max	Min	Typ[3]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			.85			.80	
V_{IH}	High[1]	V_{CC} = Max	2.1			2.1			
V_{IC}	Clamp[1,4]	V_{CC} = Min, I_{IN} = −12mA		−1.0	−1.5		−1.0	−1.5	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,5]	I_{OL} = 16mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S11/111)[1,6]	I_{OH} = −2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−250		−10	−250	
I_{IH}	High	V_{IN} = 5.5V		1	25		1	40	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S10/110)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S11/111)	V_{OUT} = 5.5V		1	60		1	100	μA
		V_{OUT} = 0.45V[7]		−1	−60		−1	−100	
I_{OS}	Short circuit (82S11/111)[8]	V_{OUT} = 0V	−20		−100	−20		−100	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max							mA
		$0 < T_A < 25°C$		120	155		120	155	
		$T_A \ge 25°C$		95	130		95	130	
		$T_A \le 0°C$			170			170	
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		7			4		
C_{OUT}	Output	V_{OUT} = 2.0V							

AC ELECTRICAL CHARACTERISTICS[2]

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

N82S10/110/11/111: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

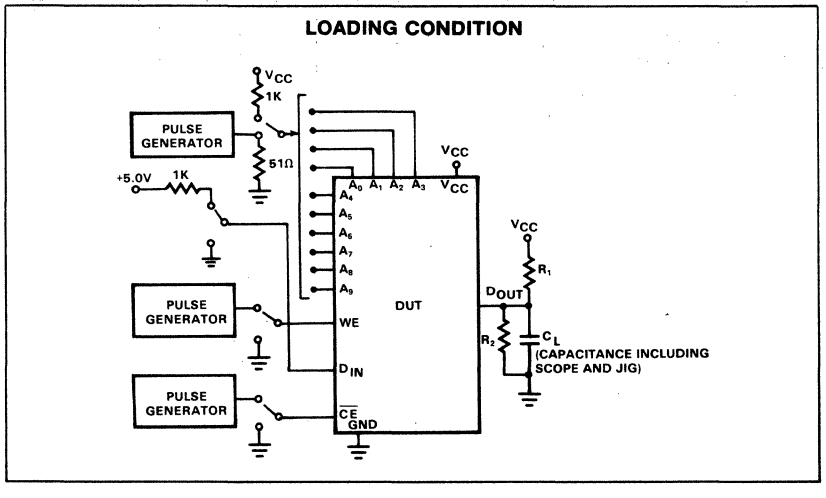
S82S10/11: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S10/11			N82S110/111			S82S10/11			UNIT
			Min	Typ[3]	Max	Min	Typ	Max	Min	Typ[3]	Max	
Access time												ns
T_{AA} Address				30	45			35		30	70	
T_{CE} Chip enable				15	30			25		15	45	
Disable time												ns
T_{CD}	Output	Chip enable		15	30			25		15	45	
T_{WD}	Output	Write enable		20	30			25		20	45	
T_{WR} Write recovery time				20	30			25		20	45	ns
Setup and hold time												ns
T_{WSA} Setup time	Write enable	Address	5	0		5			15	0		
T_{WHA} Hold time			5	0		10			10	0		
T_{WSD} Setup time	Write enable	Data in	40	30		30			55	35		
T_{WHD} Hold time			5	0		5			5	0		
T_{WSC} Setup time	Write enable	$\overline{CE}$	5	0		5			5	0		
T_{WHC} Hold time												
Pulse width												ns
T_{WP} Write enable[10]			35	25		25			50	25		

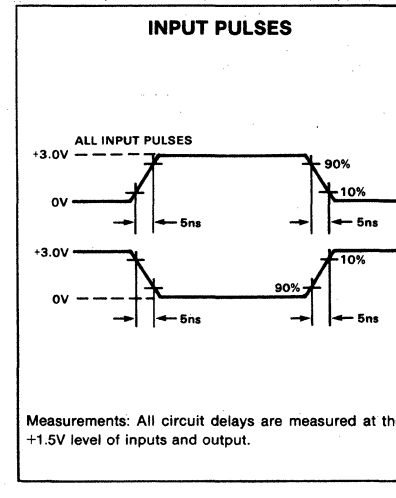
NOTES

1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
   Typical thermal resistance values of the package at maximum temperature are:
   Θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
   Θ_{JA} junction to ambient - still air - 90°C/watt
   Θ_{JA} junction to case - 20°C/watt
3. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
4. Test each input one at a time.
5. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
7. Measured with V_{IH} applied to $\overline{CE}$.
8. Duration of the short circuit should not exceed 1 second.
9. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
10. Minimum required to guarantee a Write into the slowest bit.

TEST LOAD CIRCUIT

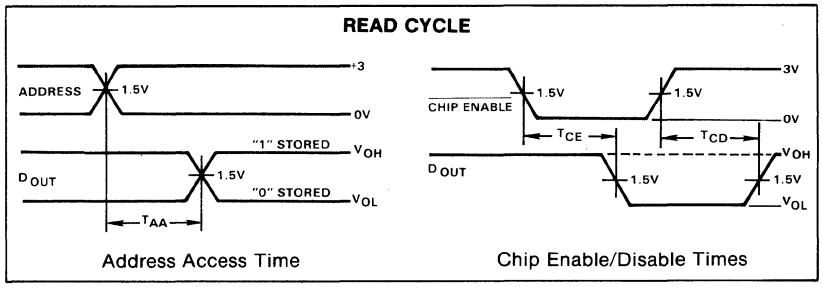


VOLTAGE WAVEFORM



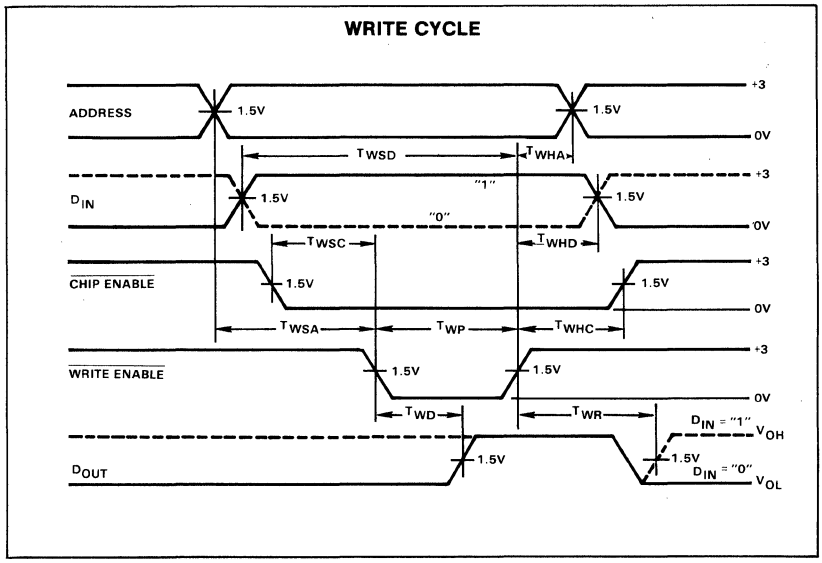
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS



Address Access Time

Chip Enable/Disable Times



MEMORY TIMING DEFINITIONS

T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid—not as shown.)
T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output is in off state.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The 93415A and 93425A, with a typical access time of 30ns, are ideal for cache buffer applications and for systems requiring very high speed main memory.

Both the 93415A and 93425A require a single +5V power supply and feature very low current pnp input structures. They include on-chip decoding and a chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both devices are available in the commercial temperature range (0°C to +75°C).

FEATURES

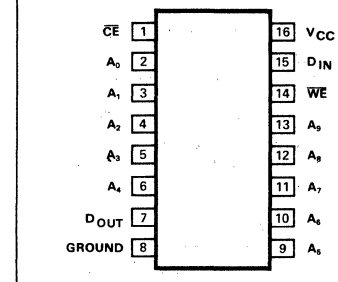
- **Address access time: 45ns max**
- **Write cycle time: 45ns max**
- **Power dissipation: 0.5mW/bit typ**
- **Input loading: -250μA max**
- **On-chip address decoding**
- **Output options:**
  - **93415A: Open collector**
  - **93425A: Tri-state**
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

APPLICATIONS

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION

F,N PACKAGE*



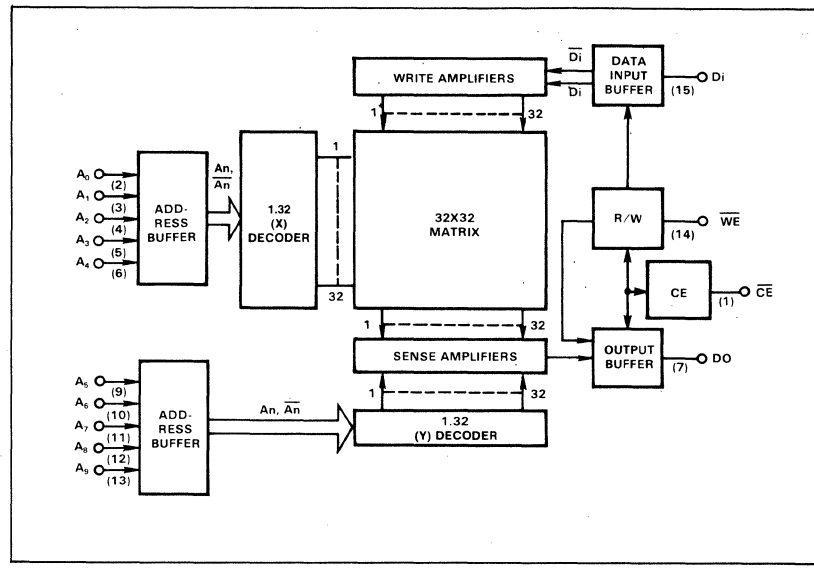
*F = Cerdip
N = Power plastic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				93415A	93425A
Read	0	1	X	Stored data	Stored data
Write low	0	0	0	1	High-Z
Write high	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (93415A)	+5.5	
V_O	Off-state (93425A)	+5.5	
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

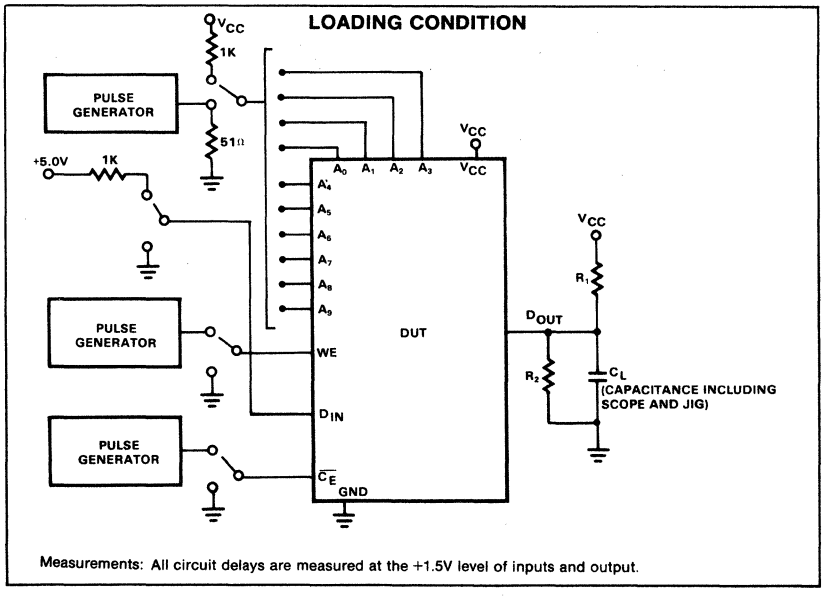
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low[1]	V_{CC} = Min			.85	
V_{IH}	High[1]	V_{CC} = Max	2.1			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5	
	Output voltage	V_{CC} = Min				V
V_{OL}	Low[1,4]	I_{OL} = 16mA		0.35	0.45	
V_{OH}	High (93425A)[1,5]	I_{OH} = -2mA	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-250	
I_{IH}	High	V_{IN}= 5.5V		1	25	
	Output current	V_{CC} = Max				
I_{OLK}	Leakage (93415A)[6]	V_{OUT} = 5.5V		1	40	μA
$I_{O(OFF)}$	Hi-Z state (93425A)	V_{OUT} = 5.5V		1	60	μA
		V_{OUT} = 0.45[6]		-1	-60	
I_{OS}	Short circuit (93425A)[7]	V_{OUT} = 0V	-20		-100	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max				mA
		$0 < T_A < 25°C$		120	155	
		$T_A \ge 25°C$		95	130	
		$T_A \le 0°C$			170	
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		4		
C_{OUT}	Output	V_{OUT} = 2.0V		7		

AC ELECTRICAL CHARACTERISTICS[9] $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
	Access time						ns
T_{AA}	Address				30	45	
T_{CE}	Chip enable				15	30	
	Disable time						ns
T_{CD}		Output	Chip enable		15	30	
T_{WD}		Output	Write enable		20	30	
T_{WR}	Write recovery time				20	30	ns
	Setup and hold time						ns
T_{WSA}	Setup time	Write enable	Address	5	0		
T_{WHA}	Hold time						
T_{WSD}	Setup time[10]	Write enable	Data in	40	35		
T_{WHD}	Hold time			5	0		
T_{WSC}	Setup time	Write enable	$\overline{CE}$	5	0		
T_{WHC}	Hold time						
	Pulse width						ns
T_{WP}	Write enable[11]			35	25		

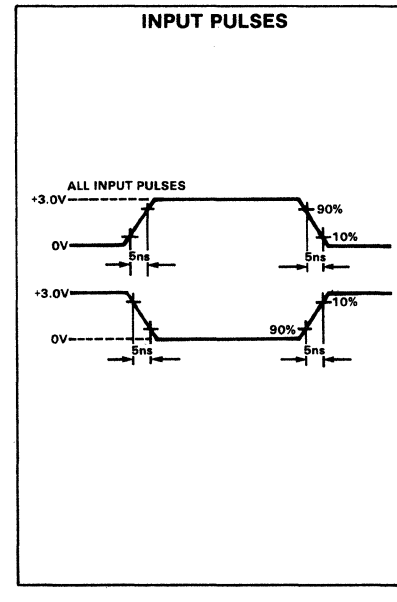
NOTES
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Test each input one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} junction to ambient at 400fpm air flow-50°C/watt
   θ_{JA} junction to ambient-still air-90°C/watt
   θ_{JA} junction to case-20°C/watt
10. For minimum Write pulse width.
11. Minimum required to guarantee a Write into the slowest bit.

TEST LOAD CIRCUIT



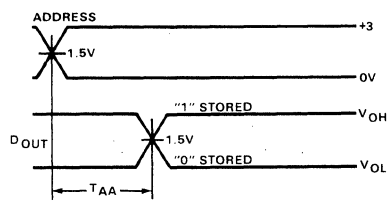
Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

VOLTAGE WAVEFORM

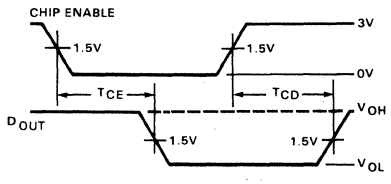


TIMING DIAGRAMS

READ CYCLE

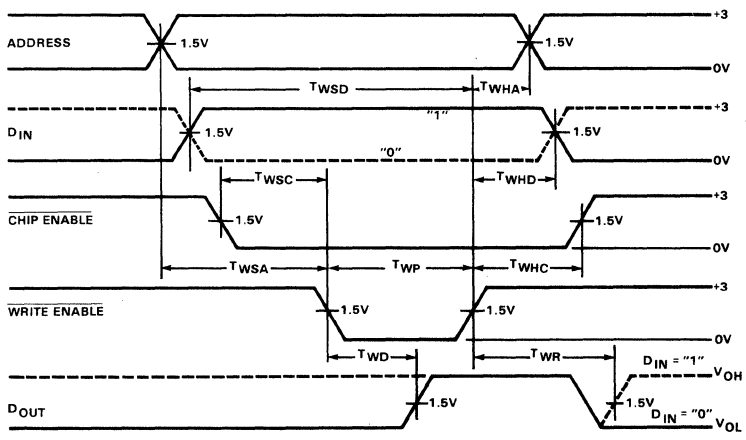


Address Access Time



Chip Enable/Disable Times

WRITE CYCLE



MEMORY TIMING DEFINITIONS

T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming Address still valid—not as shown.)
T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output is in off state.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The 82S208 and 82S210 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

The address inputs have a latch feature controlled by a latch control pin ($\overline{L}$). In the Transparent mode, the $\overline{L}$ pin is held high and the read or write location is accessed directly from the address inputs. In the Latched mode, a negative transition on the $\overline{L}$ line causes the present address state to be held in the address latches, independent of any other control signals. A positive pulse on the $\overline{L}$ line will cause a new address state to be strobed into the latches.

FEATURES

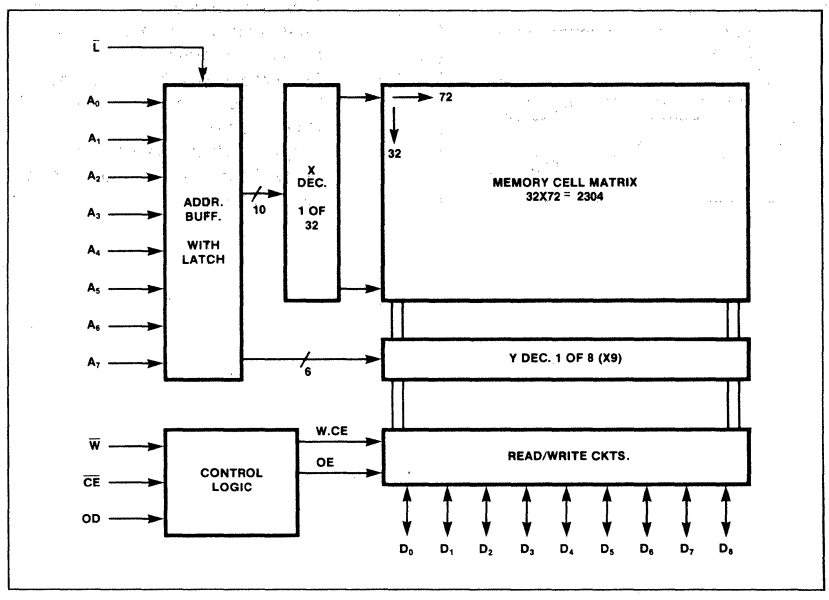
- **Access time:**
  Address: 60ns max
  Strobe: 70ns max
- **On-chip address latches**
- **Tri-state outputs**
- **Schottky clamped TTL**

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	OD	$\overline{L}$	D_N IN/OUT
Disable output	X	X	1	X	High Z
Disable R/W	X	1	X	X	High Z
Write	0	0	1	X	Data in
Read	1	0	0	X	Data out
Transparent address	X	X	X	1	—
Hold address	X	X	X	0	—

X = Don't care

BLOCK DIAGRAM

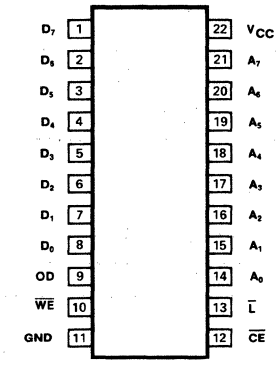


ABSOLUTE MAXIMUM RATINGS

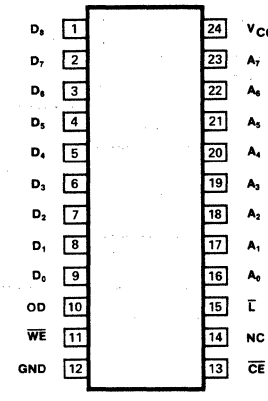
	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

PIN CONFIGURATION

82S208
F PACKAGE*

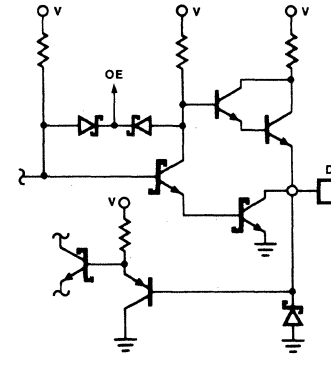


82S210
F,N PACKAGE*



*F = Cerdip
N = Plastic

TYPICAL I/O STRUCTURE



DC ELECTRICAL CHARACTERISTICS $0°C \le T_A +75°C$, $4.75V \le V_{CC}$ 5.25V[1]

PARAMETER		TEST CONDITIONS	LIMITS[2]			UNIT
			Min	Typ[3]	Max	
	Input voltage					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp[4]	I_{IN} = -18mA		-0.8	-1.2	
	Output voltage	CE = Low, OD = Low				V
V_{OL}	Low	I_{OUT} = 9.6mA			0.5	
V_{OH}	High	I_{OUT} = -2mA, High stored	2.4	3.3		
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			-100	
I_{IH}	High	V_{IN} + 5.5V			25	
	Output current					
$I_{O(OFF)}$	Hi-Z state	CE = Low, OD = High, V_{OUT} = 5.5V			40	μA
		CE = High, V_{OUT} = 0.5V			-100	
I_{OS}	Short circuit[4,5]	V_{OUT} = 0V	-20		-70	mA
I_{CC}	Supply current			135	185	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V, CE = High, OD = High		8		

AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Access time						ns
T_{AA}	Address	Output	Address			60	
T_{AL}	Strobe	Output	Latch			70	
	Enable time						ns
T_{OE}	Output	Output	OD			35	
T_{CE}	Output	Output	Chip enable			35	
	Disable time						ns
T_{OD}	Output	Output	OD			35	
T_{CD}	Output	Output	Chip enable				
	Pulse width						ns
T_{WL}	Strobe			20			
T_W	Write			40			
	Setup and hold time						ns
T_{SL}	Setup time	Latch	Address	5			
T_{HL}	Hold time	Address	Latch	10			
T_{SSA}	Setup time (strobe)	Latch	Address	0			
T_{SC}	Setup time	Write	Chip enable	5			
T_{HC}	Hold time	Chip enable	Write				
T_{SD}	Setup time	Write	Data	35			
T_{HD}	Hold time	Data	Write	10			
T_{SA}	Setup time	Write	Address	10			
T_{HA}	Hold time	Address	Write				
T_{SLW}	Setup time	Write	Latch	15			
T_{HLW}	Hold time	Latch	Write	10			
T_{S01}	Setup time (from disabled state)	Chip enable	OD	5			
T_{S02}	Setup time (from enabled state)	Data in	OD	35			
T_{HO}	Hold time	OD	Chip enable	5			

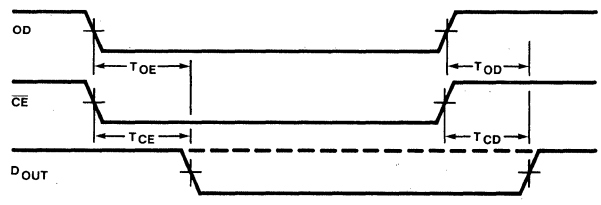
NOTES on following page.

NOTES

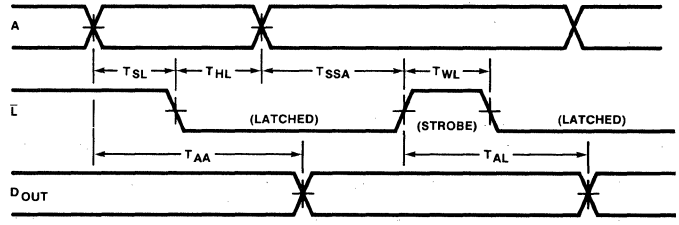
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at V_{CC} = 5V, T_A = 25°C.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.

TIMING DIAGRAMS

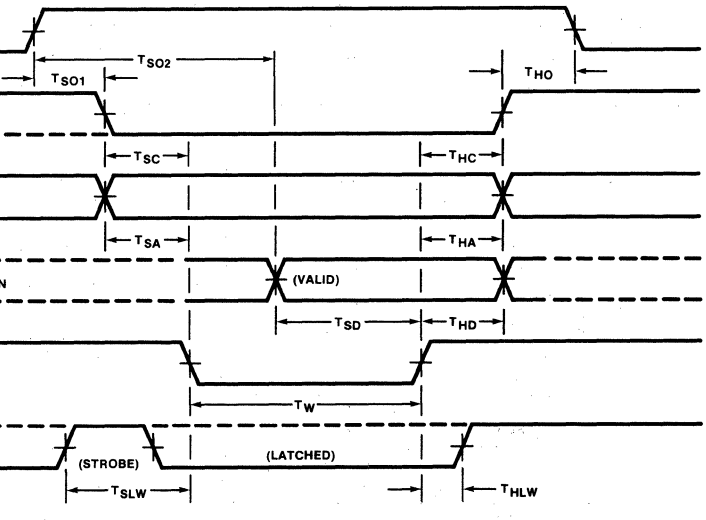
ENABLE/DISABLE



READ MODE



WRITE MODE



OBJECTIVE SPECIFICATION

82S400/400A - I • 82S401/401A - I

DESCRIPTION

The 82S400 and 82S401, with typical access time of 45ns, are ideal for cache buffer applications and for systems requiring very high speed main memory. The 82S400A and 82S401A are devices selected for speed compatibility with industry standard 1024-bit RAMs having 45ns access time.

Both devices require a single +5V power supply, feature very low current pnp input structures, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

APPLICATIONS

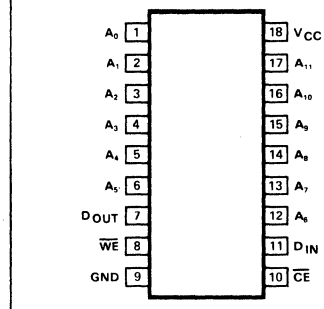
- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

FEATURES

- **Address access time:**
  82S400/401: 70ns max
  82S400A/401A: 45ns max
- **Write cycle time: 70ns max**
- **Power dissipation: 0.12mW/bit typ**
- **Input loading: -150μA max**
- **On-chip address decoding**
- **Output options:**
  82S400: Open collector
  82S401: Tri-state
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

PIN CONFIGURATION

I PACKAGE*



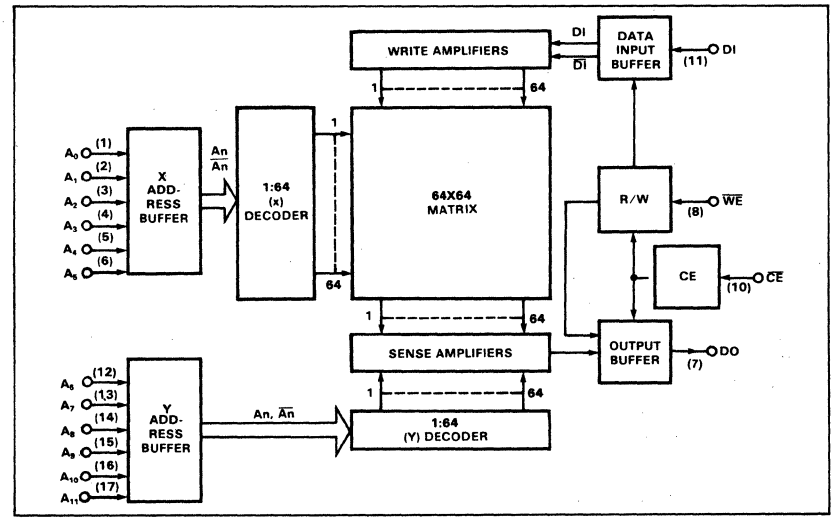
*I = Ceramic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82S400	82S401
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S400)	+5.5	
V_O	Off-state (82S401)	+5.5	
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low[1]	V_{CC} = Min			.85	
V_{IH}	High[1]	V_{CC} = Max	2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5	
	Output voltage	V_{CC} = Min				V
V_{OL}	Low[1,4]	I_{OL} = 16mA		0.35	0.45	
V_{OH}	High (82S401)[1,5]	I_{OH} = -2mA	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V		-25	-150	
I_{IH}	High	V_{IN} = 5.5V		1	25	
	Output current	V_{CC} = Max				
I_{OLK}	Leakage (82S400)[6]	V_{OUT} = 5.5V		1	40	μA
$I_{O(OFF)}$	Hi-Z state (82S401)[6]	V_{OUT} = 5.5V		1	60	μA
		V_{OUT} = 0.45V		-1	-60	
I_{OS}	Short circuit (82S401)[7]	V_{OUT} = 0V	-20		-100	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max				mA
		$0 < T_A < 25°C$		120	155	
		$T_A \ge 25°C$		105	130	
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		4		
C_{OUT}	Output	V_{OUT} = 2.0V		7		

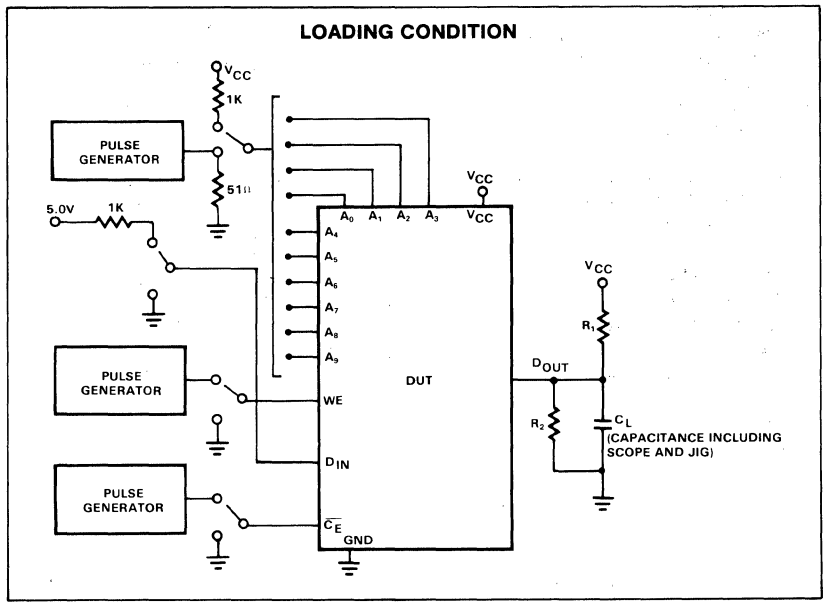
AC ELECTRICAL CHARACTERISTICS $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

PARAMETER		TO	FROM	N82S400A/401A			N82S400/401			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}		Output	Address			45		45	70	
T_{CE}		Output	Chip enable			30		30	45	
	Disable time									ns
T_{CD}		Output	Chip enable			30		30	45	
T_{WD}		Output	Write enable			30		30	45	
T_{WR}	Recovery time	Output	Write enable			30		30	45	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	5			10	5		
T_{WHA}	Hold time									
T_{WSD}	Setup time	Write enable	Data in	35			50	35		
T_{WHD}	Hold time			5			10	5		
T_{WSC}	Setup time	Write enable	CE	5			10	5		
T_{WHC}	Hold time									
	Pulse width[9]									ns
T_{WP}	Write enable			35			50	35		

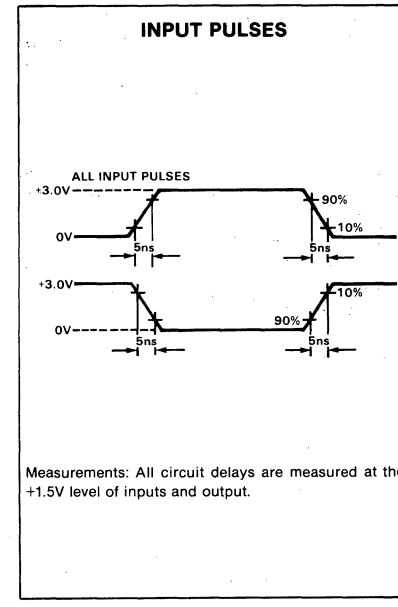
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A 25°C.
3. Test each input one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
    Θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
    Θ_{JA} junction to ambient - still air - 90°C/watt
    Θ_{JA} junction to case - 20°C/watt

TEST LOAD CIRCUIT

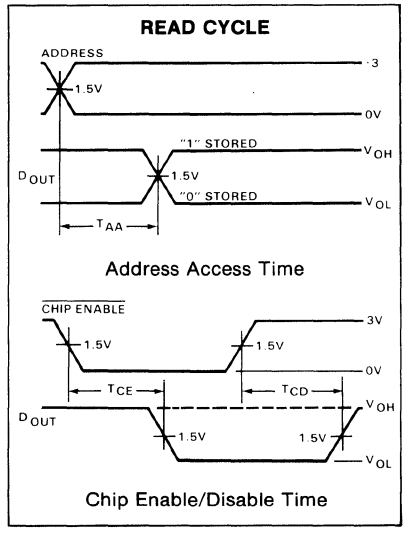


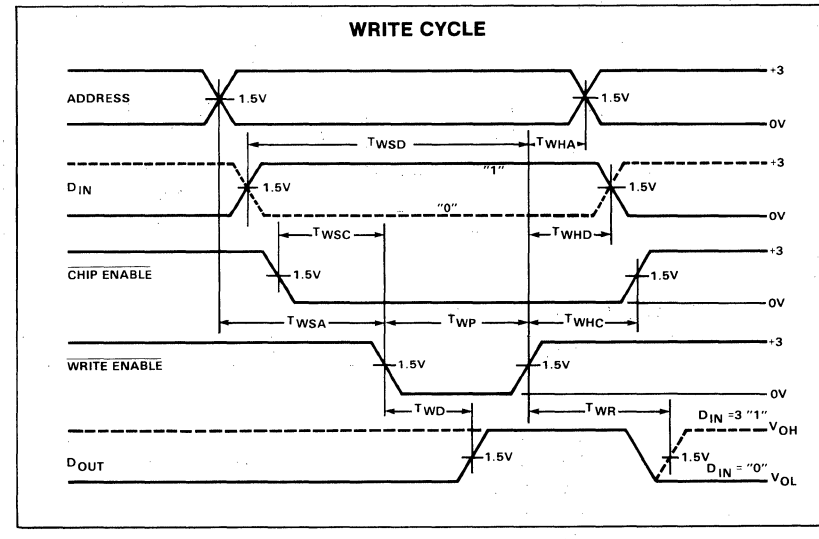
VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS





TIMING DEFINITIONS

T_{WR} Delay between end of Write Enable pulse and when Data Output becomes valid (assuming Address still valid—not as shown).

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state.

T_{AA} Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.

T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.

T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.

T_{WP} Width of Write Enable pulse.

T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WSD} Required delay between beginning of valid Data Input and end of Write Enable pulse.

T_{WD} Delay between beginning of Write Enable pulse and when Data Output is in off state.

T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.

T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.

DESCRIPTION

The 82S226 and 82S229 include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S226 and 82S229 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S226/229, F or N, and for the military temperature range (-55°C to +125°C specify S82S226/229, F only.

FEATURES

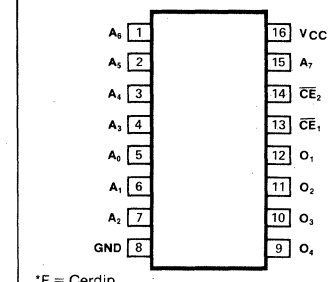
- **Address access time:**
  N82S226/229: 50ns max
  S82S226/229 70ns max
- **Power dissipation: 0.5mW/bit typ**
- **Input loading:**
  N82S226/229: -100μA max
  S82S226/229: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S226: Open collector
  82S229: Tri-state
- **Fully compatible with Signetics 82S126/129 1024-bit PROMs**
- **Fully TTL compatible**

APPLICATIONS

- **Volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

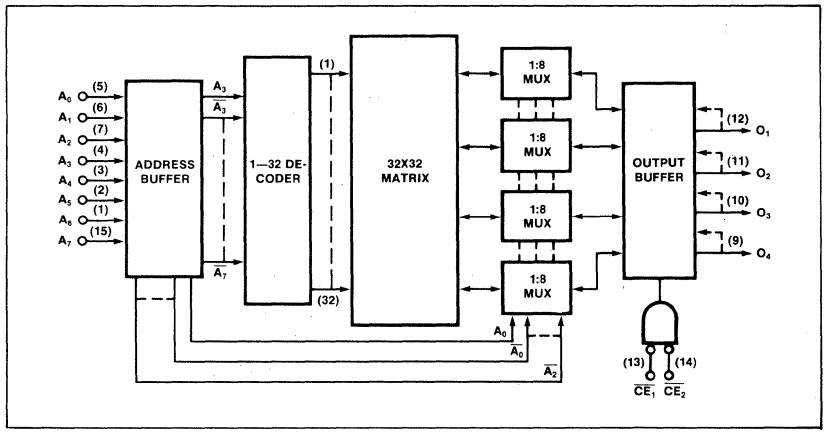
PIN CONFIGURATION

F,N PACKAGE*



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S226)	+5.5	
V_O	Off-state (82S229)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S226/229	0 to +75	
	S82S226/229	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S226/229: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S226/229: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S226/229			S82S226/229			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S229)	$\overline{CE}_1 = \overline{CE}_2$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S226)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S229)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 0.5V			-40			-60	
I_{OS}	Short circuit (82S229)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			105	120		105	125	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

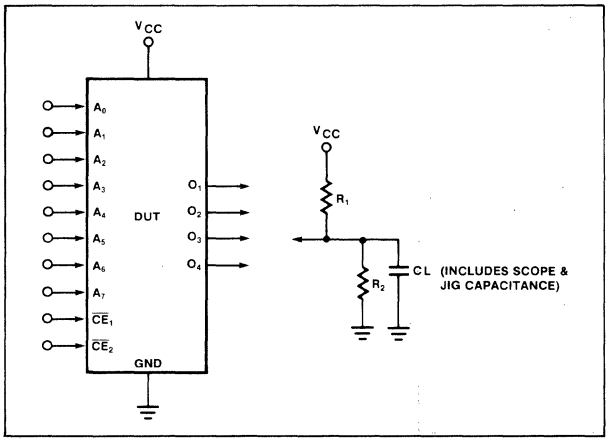
$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF
N82S226/229: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S226/229: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S226/229			S82S226/229			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		35	50		35	70	
T_{CE}	Output	Chip enable		15	25		15	35	
Disable time									ns
T_{CD}	Output	Chip disable		15	25		15	35	

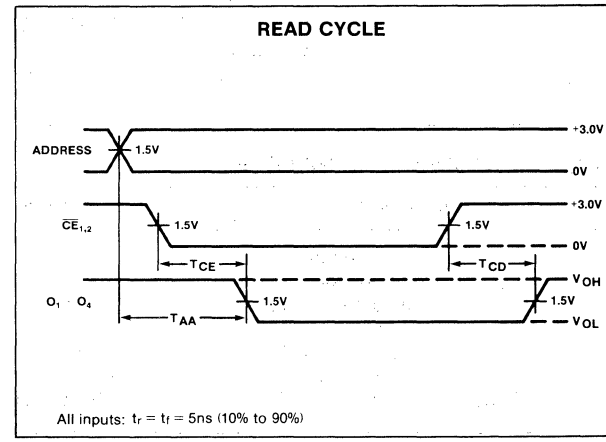
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



DESCRIPTION

The 82S214 and 82S215 include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

Both 82S214 and 82S215 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S214/215, F or N, and for the military temperature range (-55°C to +125°C) specify S82S214/215, F.

FEATURES

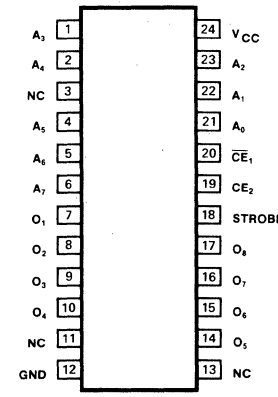
- **Address access time:**
  N82S214/215: 60ns max
  S82S214/215: 90ns max
- **Power dissipation: 165μW/bit typ**
- **Input loading:**
  N82S214/215: -100μA max
  S82S214/215: -150μA max
- **On-chip data output registers**
- **On-chip storage latches**
- **Schottky clamped**
- **Fully compatible with Signetics 82S114/115 PROMs**
- **Fully TTL compatible**

APPLICATIONS

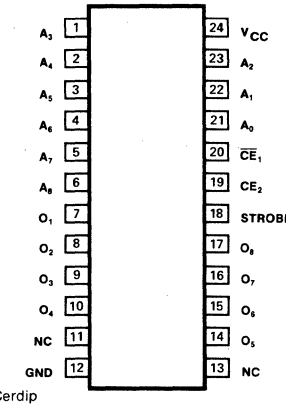
- **Microprogramming**
- **Hardwire algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATIONS

F,N PACKAGE*
82S214

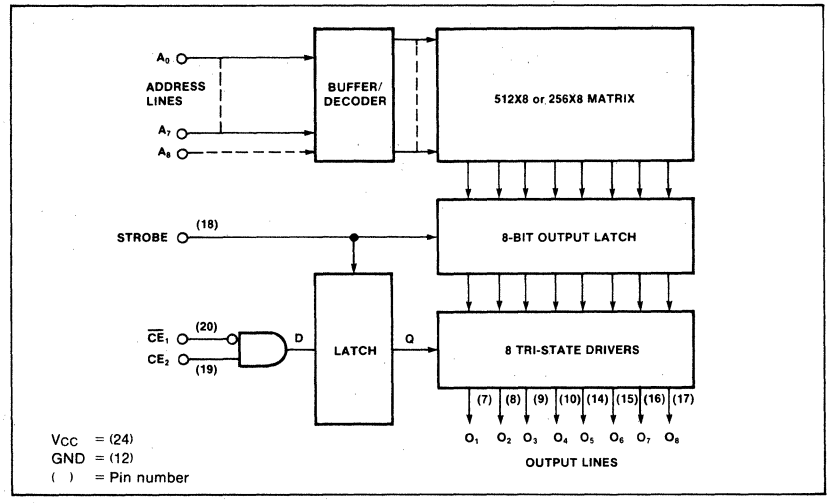


F,N PACKAGE*
82S215



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating		
	N82S214/215	0 to +75	
	S82S214/215	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S214/215: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S214/215: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S214/215			S82S214/215			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA			0.5			0.5	
V_{OH}	High	CE_1 = Low, CE_2 = High, I_{OUT} = -2mA, High stored	2.7	3.3		2.4	3.3		
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			25			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	CE_1 = High or CE_2 = Low, V_{OUT} = 5.5V			40			100	μA
		CE_1 = High or CE_2 = Low, V_{OUT} = 0.5V			-40			-100	
I_{OS}	Short circuit[3]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175		130	815	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V, CE_1 = High or CE_2 = Low		8			8		

AC ELECTRICAL CHARACTERISTICS

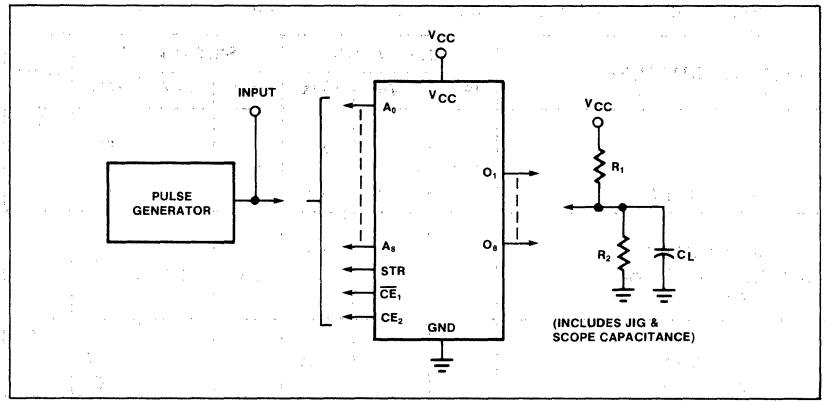
R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S214/215: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S214/215: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TO	FROM	TEST CONDITIONS	N82S214/215			S82S214/215			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time[4]			Latched or transparent read							ns
T_{AA}		Output	Address			35	60		35	90	
T_{CE}		Output	Chip enable			20	40		20	50	
	Disable time[4]			Latched or transparent read							ns
T_{CD}		Output	Chip disable			20	40		20	50	
	Setup and hold time[5]			Latched read only							ns
T_{ADH}	Hold time	Output	Address		0	-10		5	-10		
T_{CDS}	Setup time	Output	Chip enable		40			50			
T_{CDH}	Hold time				10	0		10	0		
	Pulse width[5]			Latched read only							ns
T_{SW}	Strobe				30	20		40	20		
	Latch time[5]			Latched read only							ns
T_{SL}	Strobe				60	35		90	35		
	Delatch time[5]			Latched read only							ns
T_{DL}	Strobe						30			35	

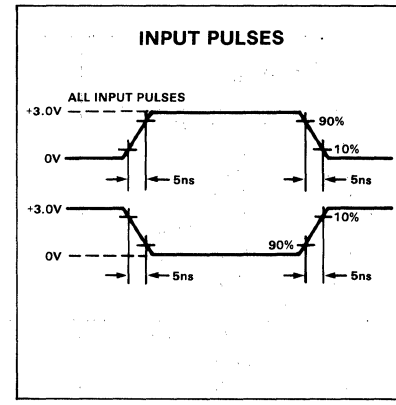
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
3. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
4. If the strobe is high, the device functions in a manner idential to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed and T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an "off" or high impedance state after it has been enabled.
5. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.

TEST LOAD CIRCUIT

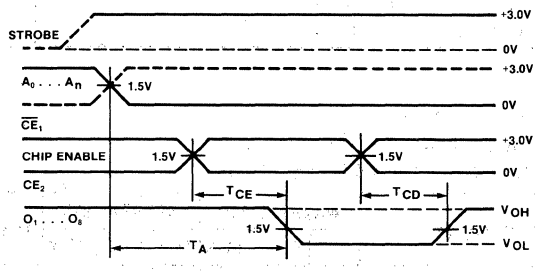


VOLTAGE WAVEFORM



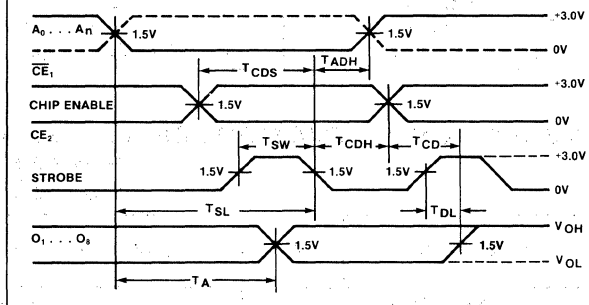
TIMING DIAGRAMS

TRANSPARENT READ



Output Latches Not Used

LATCHED READ



Output Latches Used

82S230-F,N • 82S231-F,N

DESCRIPTION

The 82S230 and 82S231 include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S230 and 82S231 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S230/231, F or N, and for the military temperature range (-55°C to +125°C) specify S82S230/231, F.

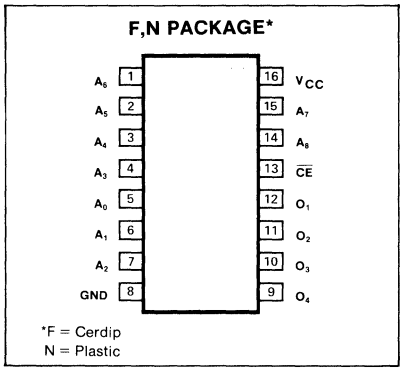
FEATURES

- **Address access time:**
  N82S230/231: 50ns max
  S82S230/231: 70ns max
- **Power dissipation: 0.3mW/bit typ**
- **Input loading:**
  N82S230/231: -100μA max
  S82S230/231: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S230: Open collector
  82S231: Tri-state
- **Fully compatible with Signetics 82S130/131 PROMs**
- **Fully TTL compatible**

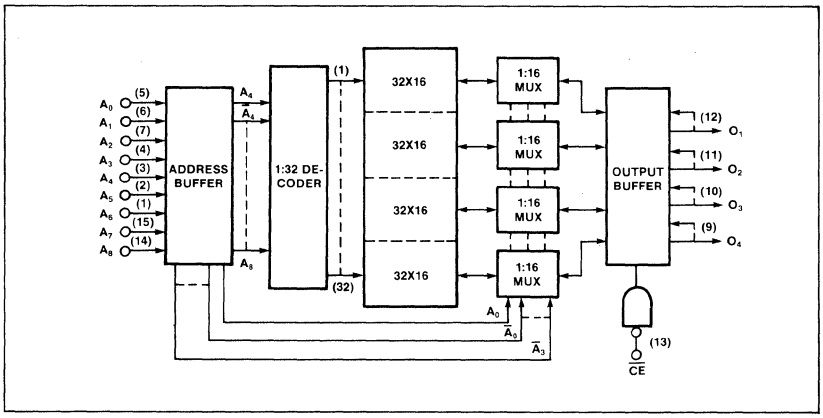
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S230)	+5.5	
V_O	Off-state (82S231)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S230/231	0 to +75	
	S82S230/231	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S230/231: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S230/231: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S230/231			S82S230/231			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S231)	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100		-150		
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S230)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S231)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit (82S231)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			120	140		120	140	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN}= 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

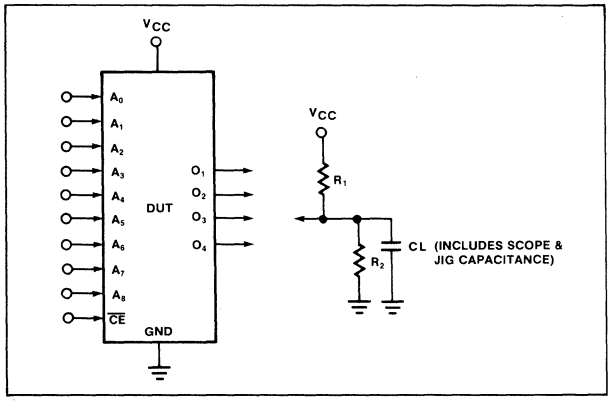
R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF[1]
N82S230/231: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S230/231: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S230/231			S82S230/231			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		40	50		40	70	
T_{CE}	Output	Chip enable		20	30		20	35	
Disable time									ns
T_{CD}	Output	Chip disable		20	30		20	35	

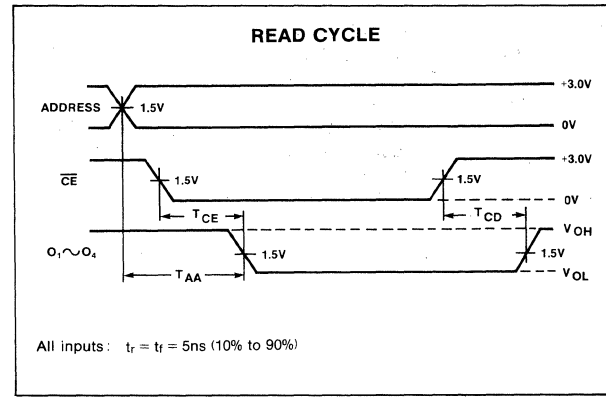
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



DESCRIPTION

The 82S240 and 82S241 are mask programmable, and include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S240 and 82S241 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S240/241, F or N, and for the military temperature range (-55°C to +125°C) specify S82S240/241, F.

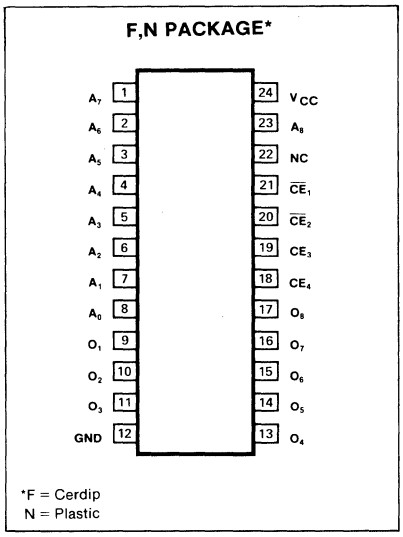
FEATURES

- **Address access time:**
  N82S240/241: 60ns max
  S82S240/241: 90ns max
- **Power dissipation: .17mW/bit typ**
- **Input loading:**
  N82S240/241: -100μA max
  S82S240/241: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S240: Open collector
  S82S241: Tri-state
- **Fully TTL compatible**

APPLICATIONS

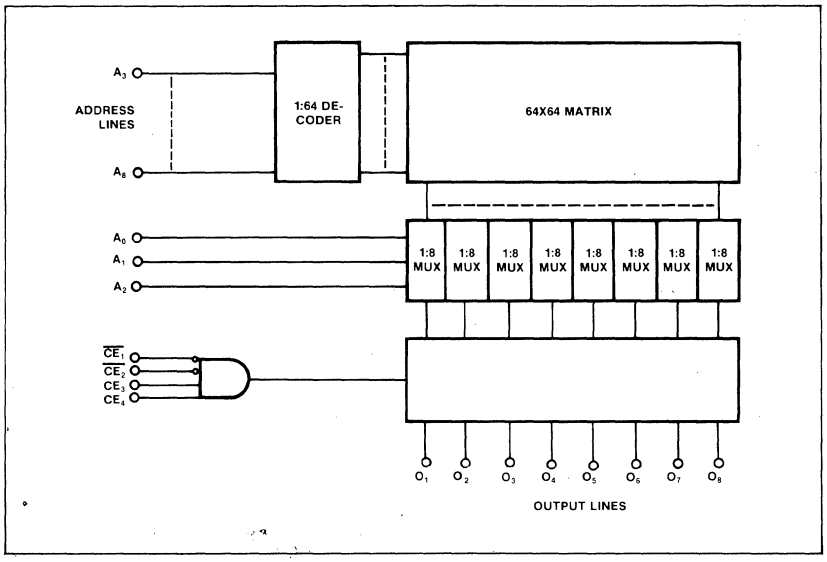
- **Volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S240)	+5.5	
V_O	Off-state (82S241)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S240/241	0 to +75	
	S82S240/241	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S240/241: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S240/241: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S240/241			S82S240/241			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45			0.5	
V_{OH}	High (82S241)	CE_1 = Low, $I_{OUT} = -2mA$, CE_2 = Low, CE_3 = High, CE_4 = High, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
I_{OLK}	Leakage (82S240)	CE_1 = High, $V_{OUT} = 5.5V$, CE_2 = High, CE_3 = Low, CE_4 = Low			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S241)	CE_1 = High, $V_{OUT} = 0.5V$, CE_2 = High, CE_3 = Low, CE_4 = Low			-40			-60	μA
		CE_1 = High, $V_{OUT} = 5.5V$, CE_2 = High, CE_3 = Low, CE_4 = Low			40			60	
I_{OS}	Short circuit (82S241)	$V_{OUT} = 0V$	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			140	175		140	185	mA
	Capacitance	$V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

AC ELECTRICAL CHARACTERISTICS

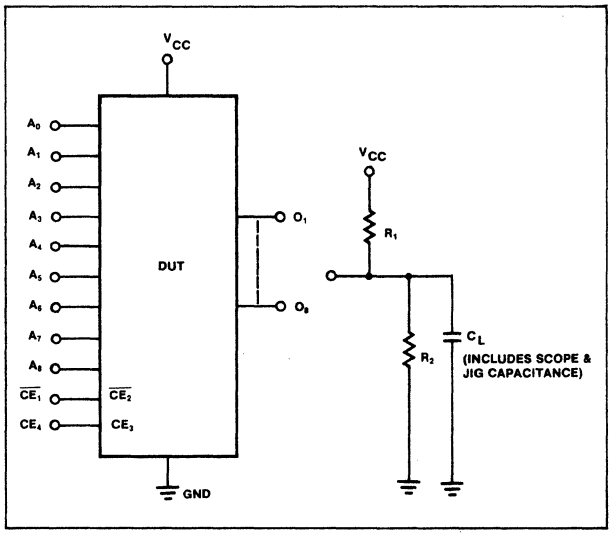
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S240/241: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S240/241: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S240/241			S82S240/241			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		40	60		40	90	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

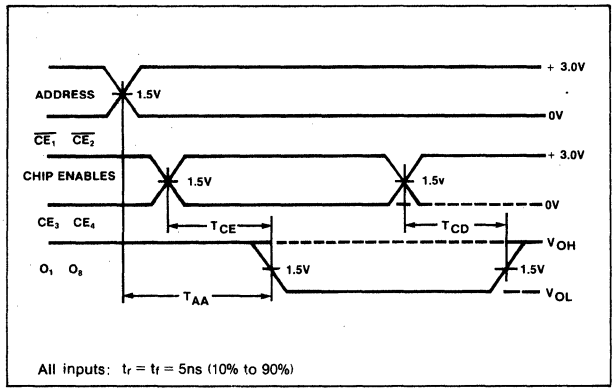
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



8228-F

DESCRIPTION

The 8228, available in a 16-pin dual-in-line package, can provide very high bit packing density by replacing 4 standard 256X4 ROMs.

This device includes on-chip decoding, and has a typical access time of 50ns with a power consumption of only .125mW per bit.

The standard 8228 ROM pattern is the USASCII Row Character Generator code; however, custom patterns are also available. The standard pattern is specified as the N8228I-CB162, while custom circuits are identified as N8228I-CXXX.

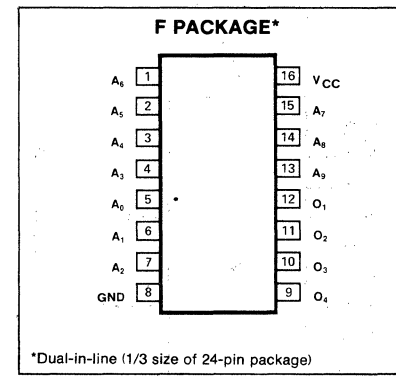
FEATURES

- **Buffered address lines**
- **Totem pole outputs**
- **Diode protected inputs**
- **Fully TTL compatible**

APPLICATIONS

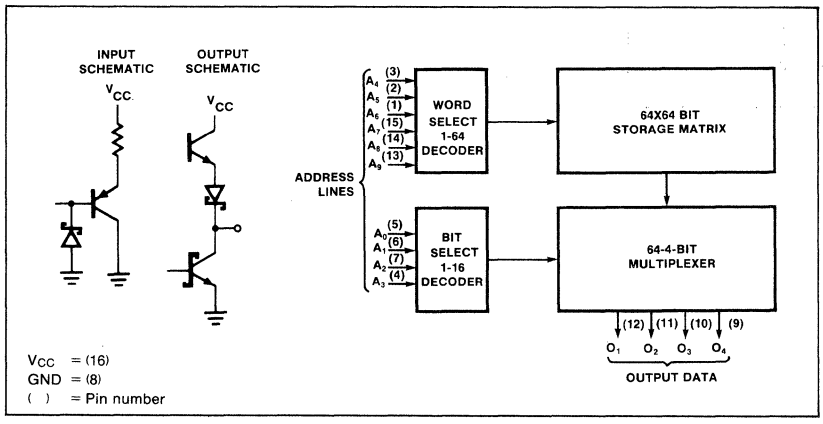
- **Microprogramming**
- **Hardwired algorithms**
- **Character recognition**
- **Character generation**
- **Control store**

PIN CONFIGURATION



*Dual-in-line (1/3 size of 24-pin package)

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low				.85	
V_{IL}	High		2.0			
V_{IC}	Clamp	I_{IN} = -18mA	-1.2			
	Output voltage					V
V_{OL}	Low	I_{OUT} = 11.2mA			0.5	
V_{OH}	High	I_{OUT} = -1.0mA	2.7			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-400	
I_{IH}	High	V_{IN} = 5.5V		1	25	
	Output current					mA
I_{OS}	Short circuit	V_{OUT} = 0V	-20		-70	
I_{CC}	Power consumption	O_1 to O_3 = Low		140	170	mA

8228-F

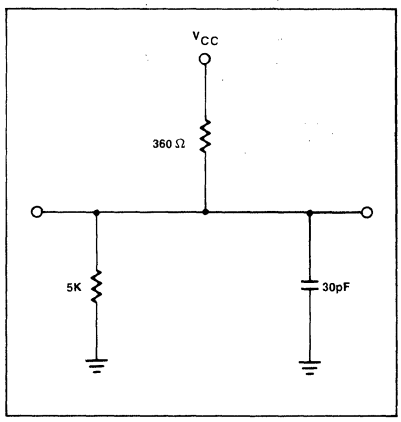
AC ELECTRICAL CHARACTERISTICS $0 \leq T_A \leq 75°C$, $4.75 \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time[1] T_{AA}	Output	Address		50	70	ns

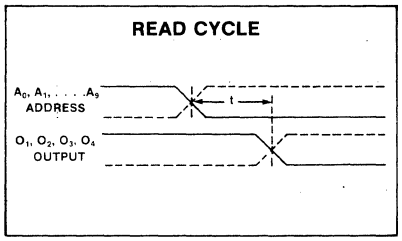
NOTES

1. Rise and fall time for this test must be less than 5ns. Input amplitudes are 3.0V and all measurements are made at 1.5V.
2. Positive current is defined as into the terminal referenced.
3. No more than 1 output should be grounded at the same time.
4. Manufacturer reserves the right to make design and process changes and improvements.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



82S280-F,N • 82S281-F,N

DESCRIPTION

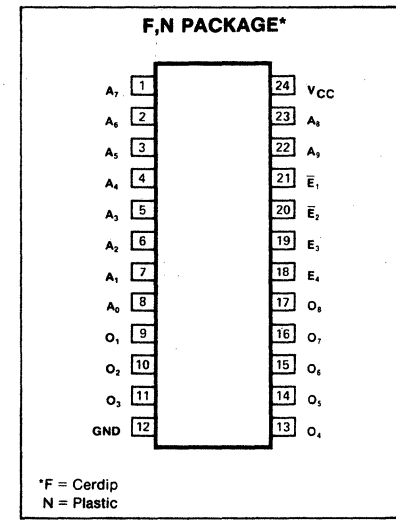
The 82S280 and 82S281 include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S280 and 82S281 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S280/281, F or N, and for the military temperature range (-55°C to +125°C) specify S82S280/281, F only.

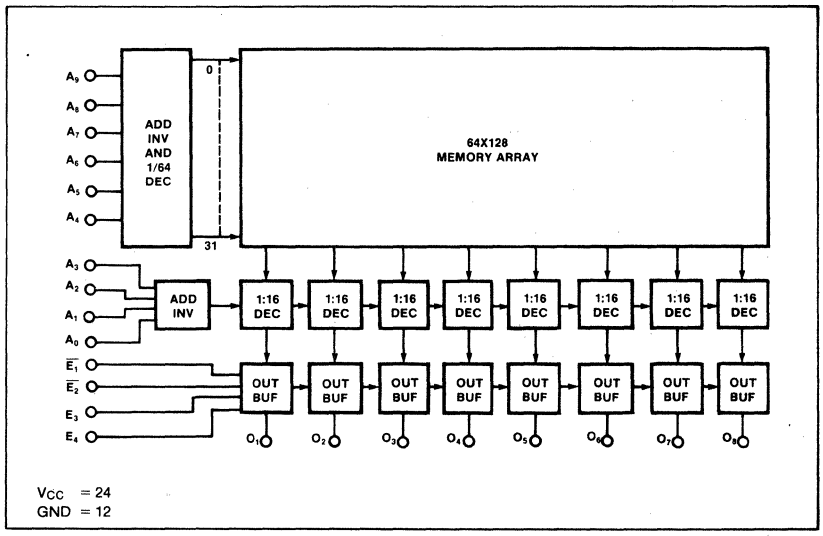
FEATURES

- **Address access time:**
  N82S280/281: 70ns max
  S82S280/281: 100ns max
- **Power dissipation: 60μW/bit typ**
- **Input loading:**
  N82S280/281: -100μA max
  S82S280/281: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S280: Open collector
  82S281: Tri-state
- **Enable = $\overline{E1}$ • $\overline{E2}$ • E3 • E4**
- **Fully TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S280/281	0 to +75	
	S82S280/281	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S280/281: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S280/281: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S280/281[1]			S82S280/281[1]			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45			0.5	
V_{OH}	High	CE_1 = Low, CE_2 = High, $I_{OUT} = -2mA$, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			25			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	CE_1 = High or CE_2 = Low, $V_{OUT} = 5.5V$			40			100	μA
		CE_1 = High or CE_2 = Low, $V_{OUT} = 0.5V$			-40			-100	
I_{OS}	Short circuit[3]	$V_{OUT} = 0V$	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			100	140		100	150	mA
	Capacitance	$V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

AC ELECTRICAL CHARACTERISTICS

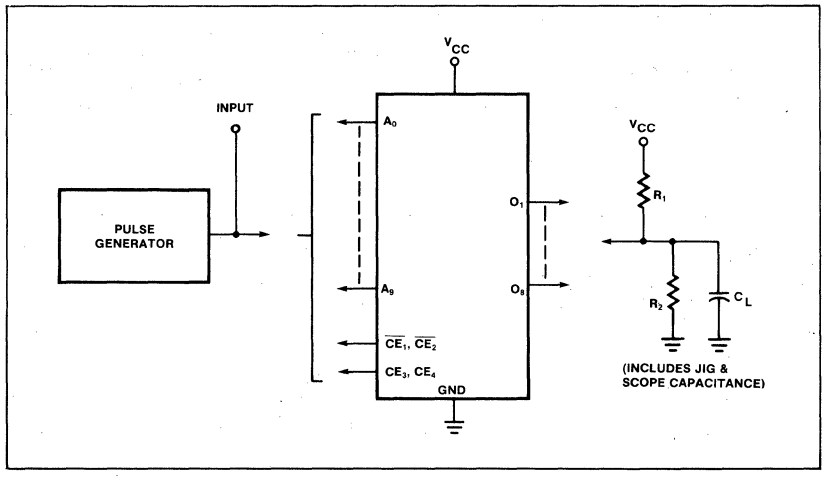
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S280/281: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S280/281: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S280/281			S82S280/281			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		40	70		40	100	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

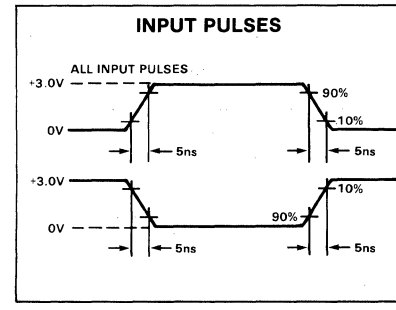
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = +5.0V$ and $T_A = +25°C$.
3. No more than one output should be grounded at the same time.

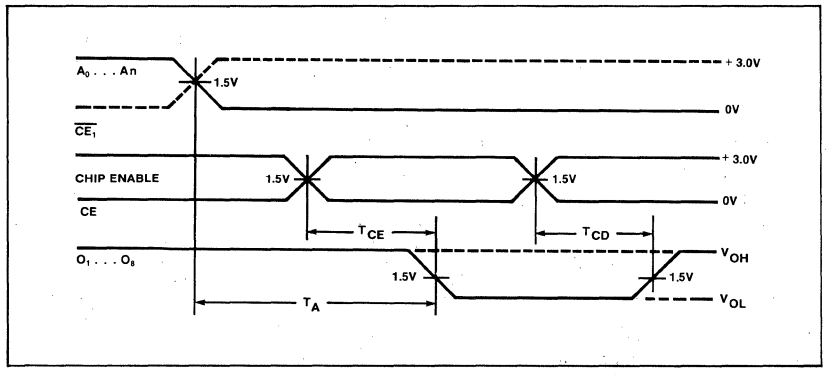
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAM



OBJECTIVE SPECIFICATION

82S290-F,N • 82S291-F,N

DESCRIPTION

The 82S290 and 82S291 include on-chip decoding and 3 programmable chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S290 and 82S291 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S290/291, F or N, and for the military temperature range (-55°C to +125°C) specify S82S290/291, F.

FEATURES

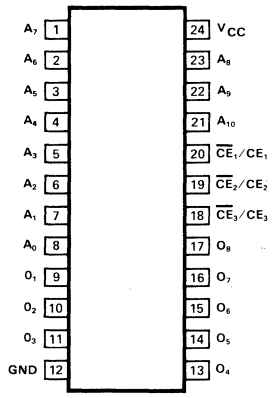
- **Address access time:**
  N82S290/291: 80ns max
  S82S290/291: 100ns max
- **Power dissipation: 40μW/bit typ**
- **Input loading:**
  N82S290/291: -100μA max
  S82S290/291: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S290: Open collector
  82S291: Tri-state
- **Fully compatible with Signetics 82S190/191 PROMs**
- **Fully TTL compatible**

APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

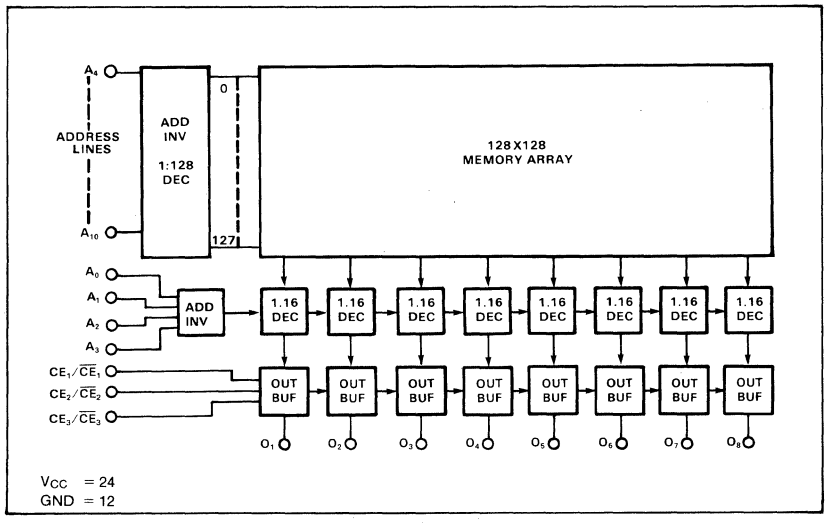
PIN CONFIGURATION

F,N PACKACE*



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S290)	+5.5	
V_O	Off-state (82S291)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S290/291	0 to +75	
	S82S290/291	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S290/291: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S290/291: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S290/291			S82S290/291			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High (82S291)	$\overline{CE}$ = Low, I_{OUT} = -2.4mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S290)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S291)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit (82S291)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	170		130	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

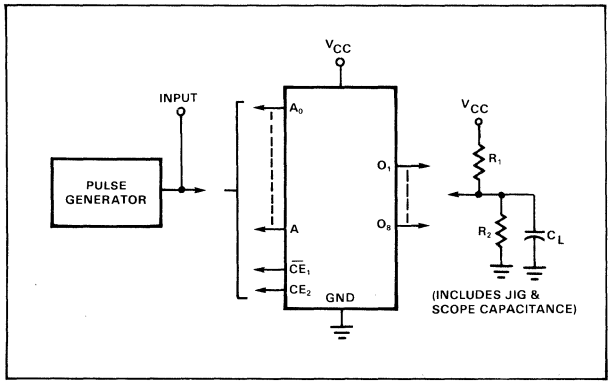
$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF[1]
N82S290/291: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S290/291: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S290/291			S82S290/291			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		50	80		50	100	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

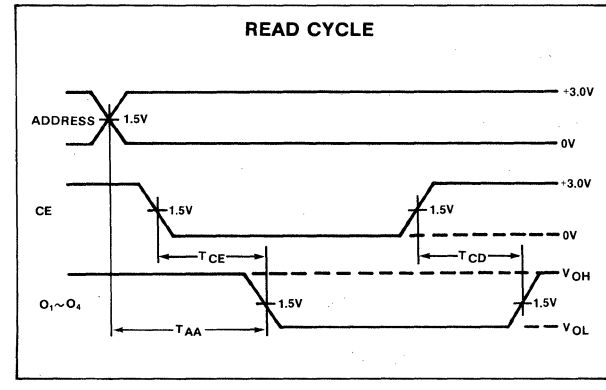
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING INFORMATION

Programming Equipment for Signetics PROMs

Programming equipment is available from several manufacturers, including Curtis Enterprises, Data I/O, and Pro-Log. Choice of equipment varies from manual duplicators to fully automatic programmers which read paper tape coded in a variety of formats.

For more information, contact Signetics Memory Marketing or any of the following programmer manufacturers:

Curtis Enterprises
P.O. Box 4090
Mountain View, Calif. 94040
(415) 964-3136

Data I/O Corporation
P.O. Box 308
Issaquah, Washington 98027

Pro-Log Corporation
2411A Garden Road
Monterey, Calif. 93940
(408) 372-4593

CURTIS ENTERPRISES REFERENCE

PROM TYPE	ORGANIZATION	OUTPUTS	MANUAL PROGRAMMER	DUPLICATOR
8223	32X8	OC	PR-23B or PR-1369A	PR-2300
82S23	32X8	OC	PR-1369A	PR-2300S
82S123	32X8	TS	PR-1369A	PR-2300S
82S27	256X4	OC	PR-27	PR-2700S
82S126	256X4	OC	PR-1369A or PR-1269	PR
82S129	256X4	TS	PR-1369A or PR-1269	PR-2600SA
82S114	256X8	TS	PR-145	PR-1145
82S115	512X8	TS	PR-145	PR-1145
82S130	512X4	OC	PR-1369A	PR-2600SA
82S131	512X4	TS	PR-1369A	PR-2600SA
10139	32X8	(ECL)	PR-10139	—

PRO-LOG REFERENCE

PROM TYPE	ORGANIZATION	OUTPUTS	MANUAL PROGRAMMER
82S23	32X8		PM9010
82S123	32X8		PM9010
82S126	256X4		PM9008
82S129	256X4		PM9008
82S130	512X4		PM9008
82S131	512X4		PM9008
82S114	256X8		PM9021
82S115	512X8		PM9021
10149	256X4	(ECL)	N/A*
82S136	1024X4		N/A*
82S137	1024X4		N/A*
82S184	2048X4		N/A*
82S185	2048X4		N/A*
82S180	1024X8		N/A*
82S181	1024X8		N/A*

*Contact Signetics or Pro-Log

DATA I/O
MODEL V UNIVERSAL PROGRAMMER
MODEL IX PORTABLE PROGRAMMER
MODEL X FPLA PROGRAMMER

CONFIGURATION	MANUFACTURERS' PART NO.	DATA I/O PROGRAM CARD SET	PROGRAM SOCKET ADAPTER	PRO-GRAMMED LOGIC LEVEL	READ-ONLY OPTIONS	
					READ-ONLY CARD	READ-ONLY SOCKET ADAPTER
32X8 (FL)	8223	1051-1	1034	VOH	1142	1037
32X8 (FL)	10139 ECL	1051-2	1034	VOH	1142	1037
32X8(FL)	82S23, 82S123	1051-7	1034	VOH	1142	1037
256X8 (FL)	82S114	1226-2*	1096	VOH	1142	1096
512X8 (FL)	82S115	1226-2*	1097	VOH	1142	1097
256X4 (FL)	10149 ECL	1144-1	1003-4	VOH	1187-13	1003-4
256X4 (FL)	82S126, 82S129	1226-2*	1035-1	VOH	1142	1035
512X4 (FL)	82S130, 82S131	1226-2*	1035-2	VOH	1142	1035
512X8 (FL)	82S140, 82S141	1226-2*	1033-2	VOH	1142	1033
1024X4 (FL)	82S136, 82S137	1226-2*	1039-3	VOH	1142	1039
1024X8 (FL)	82S180, 82S181, 82S2708	1226-2*	1033-3	VOH	1142	1033
2048X4 (FL)	82S184, 82S185	1226-2*	1039	VOH	1142	1039
2048X8 (FL)	82S190, 82S191	1226-2*	1033	VOH	1142	1033

*Generic Program Cards

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S23 and 82S123 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

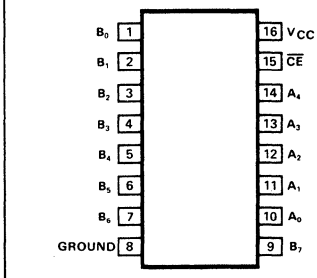
Both 82S23 and 82S123 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23/123, N or F, and for the military temperature range (-55°C to +125°C) specify S82S23/123, F only.

FEATURES

- **Address access time:**
  N82S23/123: 50ns max
  S82S23/123: 65ns max
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  N82S23/123: -100μA max
  S82S23/123: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S23: Open collector
  82S123: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION

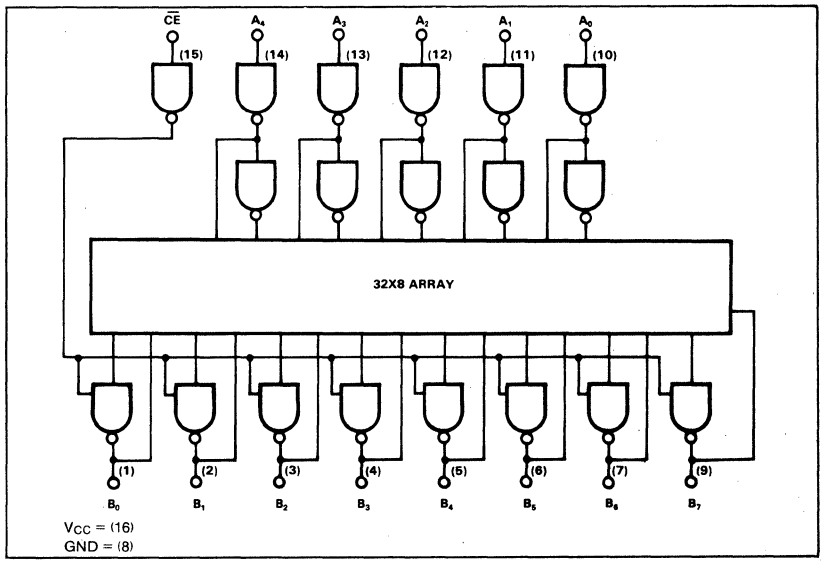
F,N PACKAGE



APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S23)	+5.5	
V_O	Off-state (82S123)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S23/123	0 to +75	
	S82S23/123	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S23/123: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S23/123: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S23/123			S82S23/123			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.85			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	$I_{OUT} = 16mA$			0.45			0.5	
V_{OH}	High	$\overline{CE}$ = Low, $I_{OUT} = -2mA$, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			50			50	
	Output current								
I_{OLK}	Leakage (82S23)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40			50	μA
$I_{O(OFF)}$	Hi-Z state (82S123)	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40			50	μA
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			-40			-50	
I_{OS}	Short circuit (82S123)	$V_{OUT} = 0V$	-20		-90	-20		-100	mA
I_{CC}	V_{CC} supply current			65	77		65	85	mA
	Capacitance	$V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

AC ELECTRICAL CHARACTERISTICS

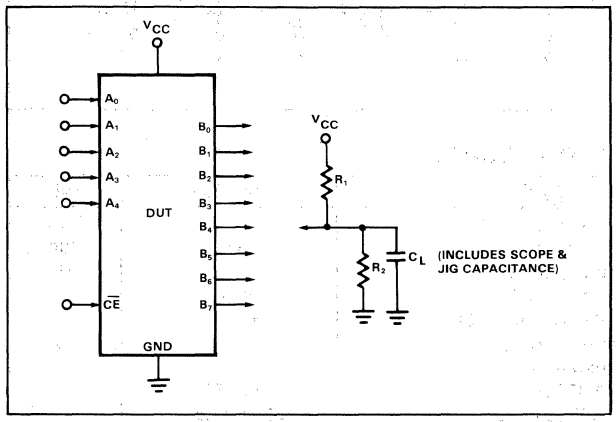
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$[1]
N82S23/123: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S23/123: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S23/123			S82S23/123			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time								ns
T_{AA}	Output	Address		35	50		35	65	
T_{CE}	Output	Chip enable		25	35		25	40	
	Disable time								ns
T_{CD}	Output	Chip disable		25	35		25	40	

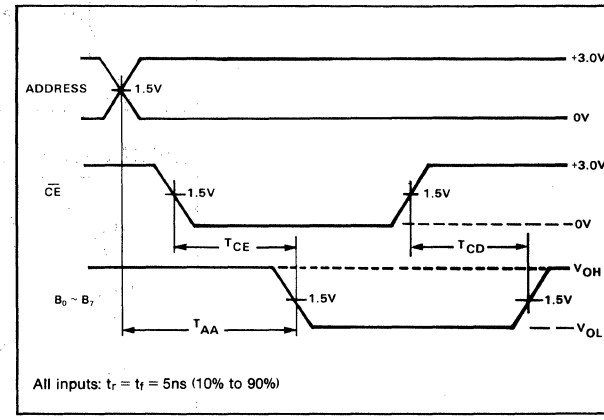
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	$I_{CCP} = 250 \pm 50mA$, Transient or steady state	9.5	10.0	10.5	
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		0.9	1.0	1.1	V
I_{CCP}	Programming supply current	$V_{CCP} = +10.0 \pm 0.5V$	200	250	300	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	$V_{IH} = +5.5V$			50	
I_{IL}	Low	$V_{IL} = +0.4V$			-500	
V_{OUT}	Output programming voltage[3]	$I_{OUT} = 65 \pm 3mA$, Transient or steady state	15.0	15.5	16.0	V
I_{OUT}	Output programming current	$V_{OUT} = +15.5 \pm 0.5V$	60			mA
T_R	Output pulse rise time		10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_V	Verify delay		50			μs
t_D	Pulse sequence delay		10			
T_{PRI}	Initial programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS}	Programming pause	$V_{CC} = 0V$	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%

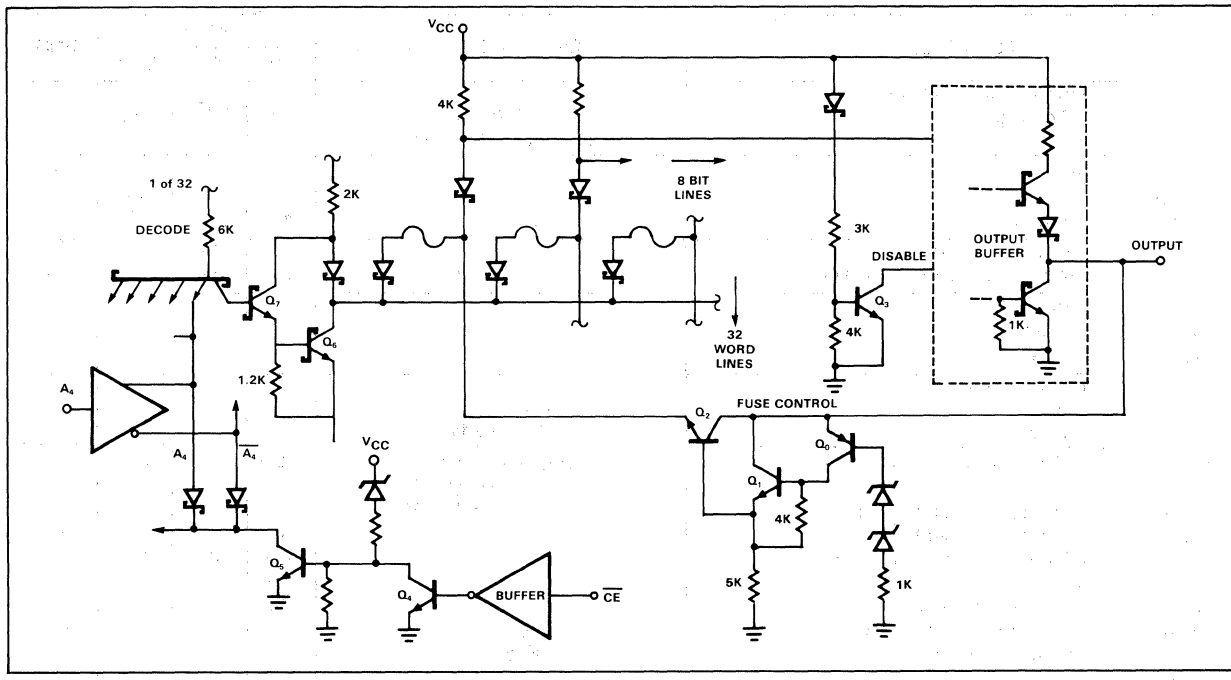
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure that $+15.5 \pm 0.5V$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. Continuous fusing for an unlimited time is also allowed, provided that a 50% duty cycle is maintained. This may be accomplished by using a programming time and pauses of 6μs each.

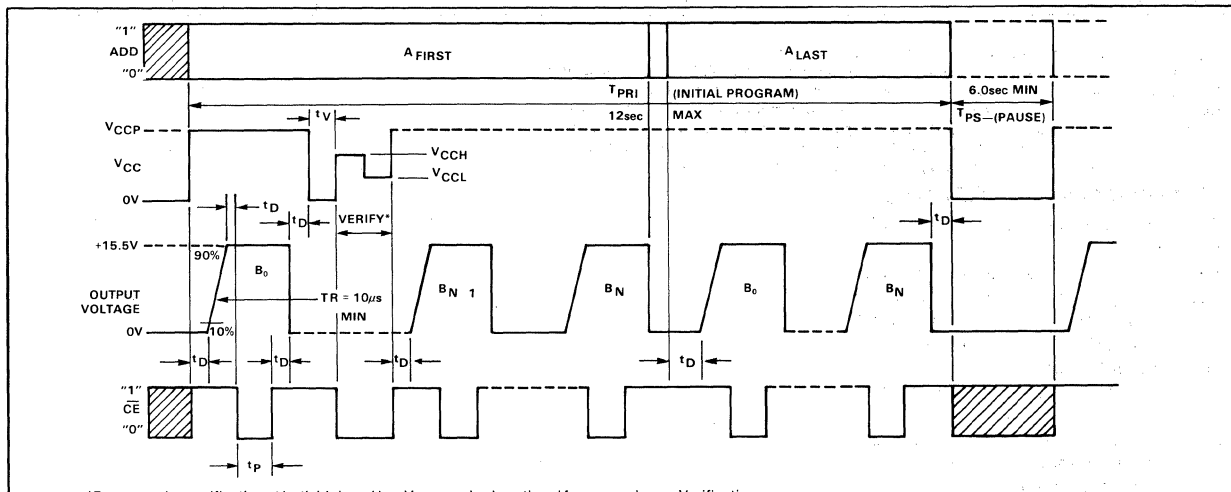
PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the address to be programmed, and raise V_{CC} to $V_{CCP} = +10 \pm 0.5V$.
3. After 10μs delay, apply $I_{OUT} = 65 \pm 3mA$ to the output to be programmed. Program one output at a time.
4. After 10μs delay, pulse the CE input to logic low for 0.3 to 0.5μs.
5. After 10μs delay, remove I_{OUT} from the programmed output.
6. After 10μs delay, return V_{CC} to 0V.
7. To verify programming, after 50μs delay, raise V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic low level to the CE input. The programmed output should remain in the high state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2V$, and verify that the programmed output remains in the high state.
8. Raise V_{CC} to $V_{CCP} = +10 \pm 0.5V$ and repeat steps 3 through 7 to program other bits at the same address.
9. After 10μs delay, repeat steps 2 through 8 to program all other address locations.

TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional for convenience. Verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

10139-F,N

DESCRIPTION

The 10139 is organized as an array of 32 words and 8 bits. The initial unprogrammed state is 0 (low). The user may program 1's to obtain any desired pattern. Outputs go to the 0 (low) state when the chip enable input is high, allowing wired-OR output connections. A 50Ω output drive capability makes the part suitable for use in high performance ECL systems.

FEATURES

- **Access time: 15ns typ**
- **Power dissipation: 580mW typ**
- **Field programmable (Ni-Cr link)**
- **Fully decoded**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50Ω drive)**
- **Fully compatible with Signetics ECL 10K products**

APPLICATIONS

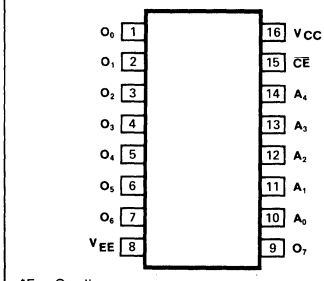
- **Programmable logic**
- **Control stores**
- **Microprogramming**
- **Hardwired algorithms**

RECOMMENDED OPERATING VOLTAGE

- **V_{CC} = GND, V_{EE} = -5.2V ± 5%**

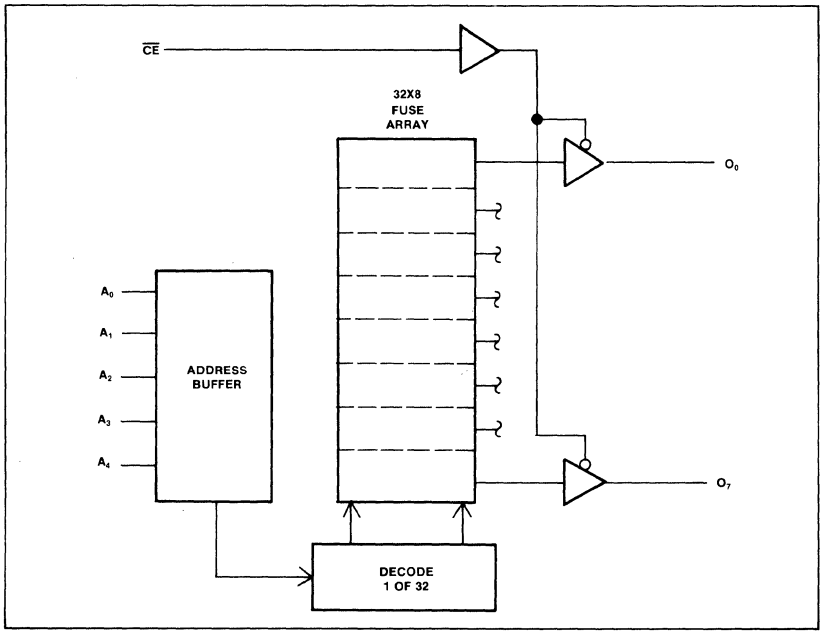
PIN CONFIGURATION

F,N PACKAGE*



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
T_A	Temperature range Operating	-30 to +85	°C

10139-F,N

DC ELECTRICAL CHARACTERISTICS V_{CC} = 0V, V_{EE} = -5.2V, R_L = 50Ω to -2V, Vdc ± 1%

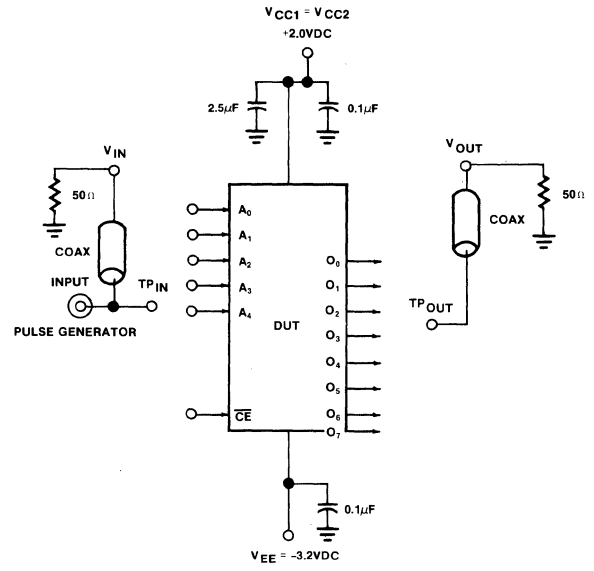
PARAMETER	TEST CONDITIONS	-30°C			+25°C			+85°C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input voltage											V
V_{IL} Low		-1.890			-1.850			-1.825			
V_{IH} High				-0.890			-0.810			-0.700	
V_{ILA} Low threshold				-1.500			-1.475			-1.440	
V_{IHA} High threshold		-1.205			-1.105			-1.035			
Output voltage											V
V_{OL} Low	V_{IH} = Max, V_{IL} = Min	-1.89		-1.675	-1.85	-1.70	-1.65	-1.825		-1.615	
V_{OH} High		-1.06		-0.89	-0.96	-0.89	-0.81	-0.89		-0.70	
V_{OLA} Low threshold	V_{IHA} = Min, V_{ILA} = Max			-1.655			-1.63			-1.595	
V_{OHA} High threshold		-1.08			-0.98			-0.91			
Input current											μA
I_{IL} Low	V_{IL} = Min				0.5						
I_{IH} High	V_{IH} = Max						265				
I_{EE} Power supply drain current						110	145				mA

AC ELECTRICAL CHARACTERISTICS V_{CC} = 2V, R_L = 50Ω to ground, -30°C ≤ T_A ≤ 85°C, V_{EE} = -3.2V

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time						ns
T_{AA}	Output	Address		15	22	
T_{CE}	Output	Chip enable		10	17	
Disable time						ns
T_{CD}	Output	Chip disable		10	17	
Rise and fall time						ns
t_+ Rise time (20-80%)				4.0		
t_- Fall time (20-80%)				4.0		

10139-F,N

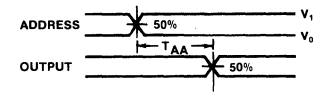
TEST LOAD CIRCUIT



Input pulse: $t_+ = t_- = 2.0 - 0.2$ns (20 to 80%)

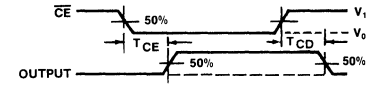
VOLTAGE WAVEFORMS

ADDRESS ACCESS TIME



Input pulse conditions: $V_0 = 0.31V$, $V_1 = 1.11V$, $t_r = 2$ns (20 to 80%), $t_f = 2$ns (20 to 80%)

CHIP ENABLE/DISABLE TIMES



Input pulse conditions: $V_0 = 0.31V$, $V_1 = 1.11V$, $t_r = 2$ns (20 to 80%), $t_f = 2$ns (20 to 80%)

NOTES

1. Dc and ac specifications apply after thermal equilibrium has been established, with transverse air flow greater than 500 linear ft/min.
2. For ac tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
3. Test procedures are shown for only 1 input or set of input conditions. Other inputs are tested in the same manner.

PROGRAMMING SYSTEMS SPECIFICATIONS

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program		11.5	12.0	12.5	
V_{CCV}	To verify		5.0	5.2	5.4	
I_{CCP}	Programming supply current	$V_{CC} = 12.0V$			250	mA
	Address voltage					V
V_{IH}	High		4.0		4.6	
V_{IL}	Low		0		1.0	
	Max time at $V_{CC} = V_{CCP}$				1.0	sec
I_{OP}	Output programming current		3.75	4.25	4.75	mA
t_p	Output program pulse width		0.5		1.0	ms
	Output pulse rise time				10	μs
	Programming pulse delay*					ms
t_d	Following V_{CC} change		0.1		1.0	
t_{d1}	Between output pulses		0.01		1.0	

*Maximum is specified to minimize the amount of time V_{CC} is at 12V.

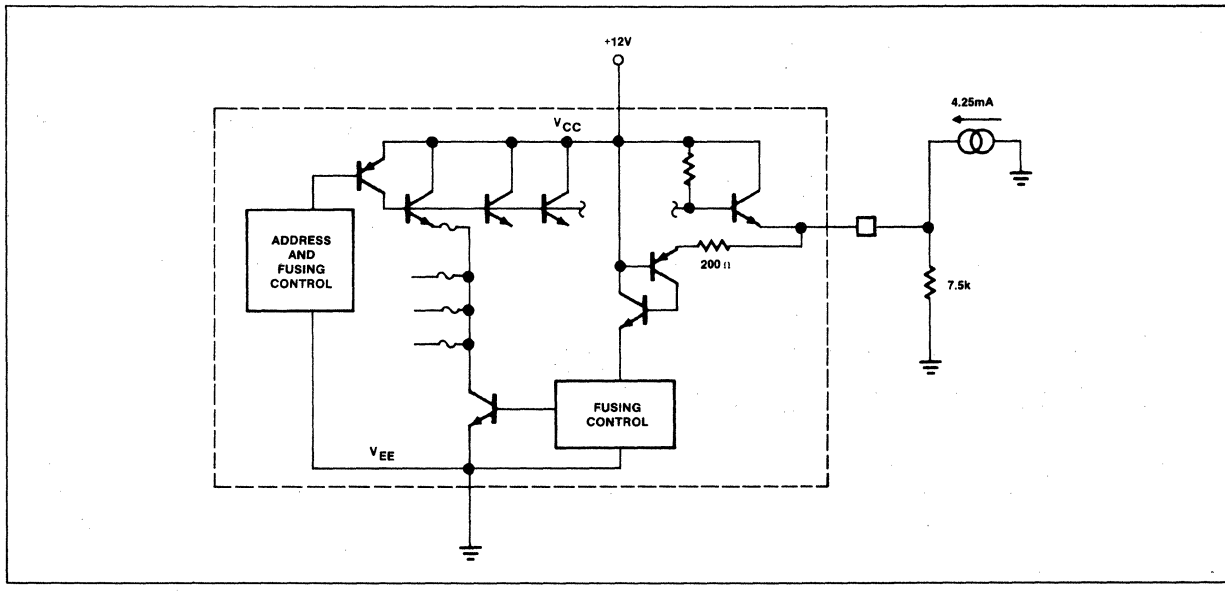
10139-F,N

PROGRAMMING PROCEDURE

The 10139 is shipped with all bits at logical low. To program logical high's, proceed as follows:

1. Connect a 7.5kΩ resistor from each output to ground. This prevents crosstalk into unselected outputs during programming.
2. Connect pin 8 (V_{EE}) to ground and pin 16 (V_{CC}) to +5.2V.
3. Address the desired word location using 0 to 1.0V for a logic low and 4.0 to 4.6V for a logic high.
4. Raise V_{CC} to 12V. Wait 100μs (min) for settling. Maximum time at 12V is 1.0 sec.
5. Apply a +4.25mA current pulse to the first output to be programmed. Output pin voltage will be approximately 1.2V above V_{CC}, and the 7.5kΩ resistor will take 1.75mA. Pulse duration is 0.5 to 1.0ms. Other outputs may be programmed sequentially using a delay of .01 to 1.0ms between current pulses.
6. Return V_{CC} to 5.2V and verify the word. Repeat step 5 once only if any bit failed to program.
7. Repeat steps 3, 4, 5 and 6 for all address locations to be programmed.
8. Verify complete truth table.

TYPICAL FUSING PATH



82S27-F

DESCRIPTION

The 82S27 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S27 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The device includes on-chip decoding, 2 chip enable inputs, and open collector outputs for ease of memory expansion.

The 82S27 is available in the commercial temperature range (0°C to +75°C) and is specified as N82S27, F.

FEATURES

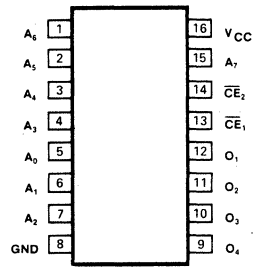
- **Address access time: 40ns max**
- **Power dissipation: 0.6mW/bit typ**
- **Input loading: 1.6mA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

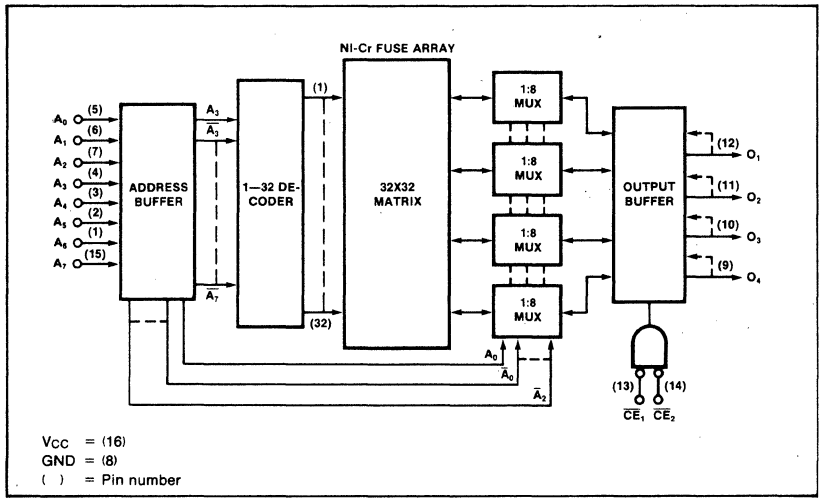
PIN CONFIGURATION

F PACKAGE*



*F = Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low				.80	
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		-1.0	-1.5	
	Output voltage					V
V_{OL}	Low	$I_{OUT} = 32mA$		0.45	0.50	
	Input current					
I_{IL}	Low	$V_{IN} = 0.50V$			-1.6	mA
I_{IH}	High	$V_{IN} = 2.4V$			40	μA
		$V_{IN} = 5.5V$			1	mA
	Output current					μA
I_{OLK}	Leakage	$\overline{CE_1}$ or $\overline{CE_2}$ = High, $V_{OUT} = 5.5V$			100	
	Capacitance	$V_{CC} = 5.0V$				pF
C_{IN}	Input	$V_{IN} = 2.0V$		5		
C_{OUT}	Output	$V_{OUT} = 2.0V$, $\overline{CE_1}$ or $\overline{CE_2}$ = High		8		

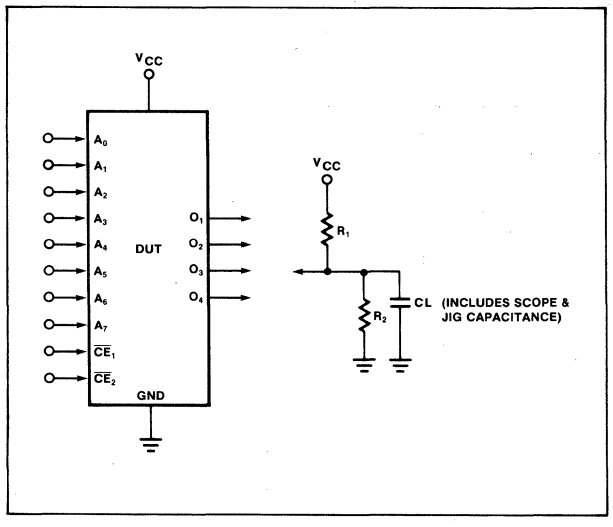
AC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
	Access time						ns
T_{AA}		Output	Address		30	40	
T_{CE}		Output	Chip enable		15	20	
	Disable time						ns
T_{CD}		Output	Chip disable		15	20	

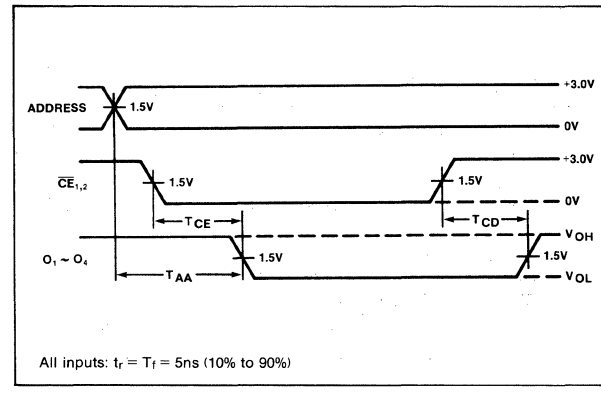
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	I_{CCP} = 300 ± 50mA, Transient or steady state	5.0		5.25	
	Verify limit					V
V_{CCH}	Upper		5.0	5.25	5.5	
V_{CCL}	Lower		4.5	4.75	5.0	
V_S	Verify threshold[2]		0.9	1.0	1.1	V
	Input voltage					V
V_{IH}	High (except $\overline{CE}_1$)		3.0		5.0	
V_{IL}	Low		0	0.4	0.5	
V_{IN}	Program level ($\overline{CE}_1$ only)		14.0	14.5	15.0	
	Input current					
I_{IH}	High	V_{IH} = +3.0V			100	μA
I_{IL}	Low	V_{IL} = +0.5V			-1.6	mA
I_{IN}	Program level ($\overline{CE}_1$ only)	V_{IN} = +15.0V			15	mA
V_{OUT}	Output programming voltage[3]	I_{OUT} = 115 ± 10mA, Transient or steady state	16.5	17.0	17.5	V
I_{OUT}	Output programming current	V_{OUT} = +17.0 ± 0.5V	105	115	125	mA
T_R	Output pulse rise time[4]		0.2		0.5	μs
t_p	Programming pulse width		0.25		0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS}	Programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR} + T_{PS}}$	Programming duty cycle[5]			50		%

NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 0.5V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. Measured with a 1K dummy load connected across the fusing source.
5. Continuous fusing for an unlimited time is also allowed, provided that a 50% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a rest period (V_{CC} = 0V) of 0.5ms.

PROGRAMMING PROCEDURE

The 82S27 is shipped with all bits at logical low. To write logical high, proceed as follows:

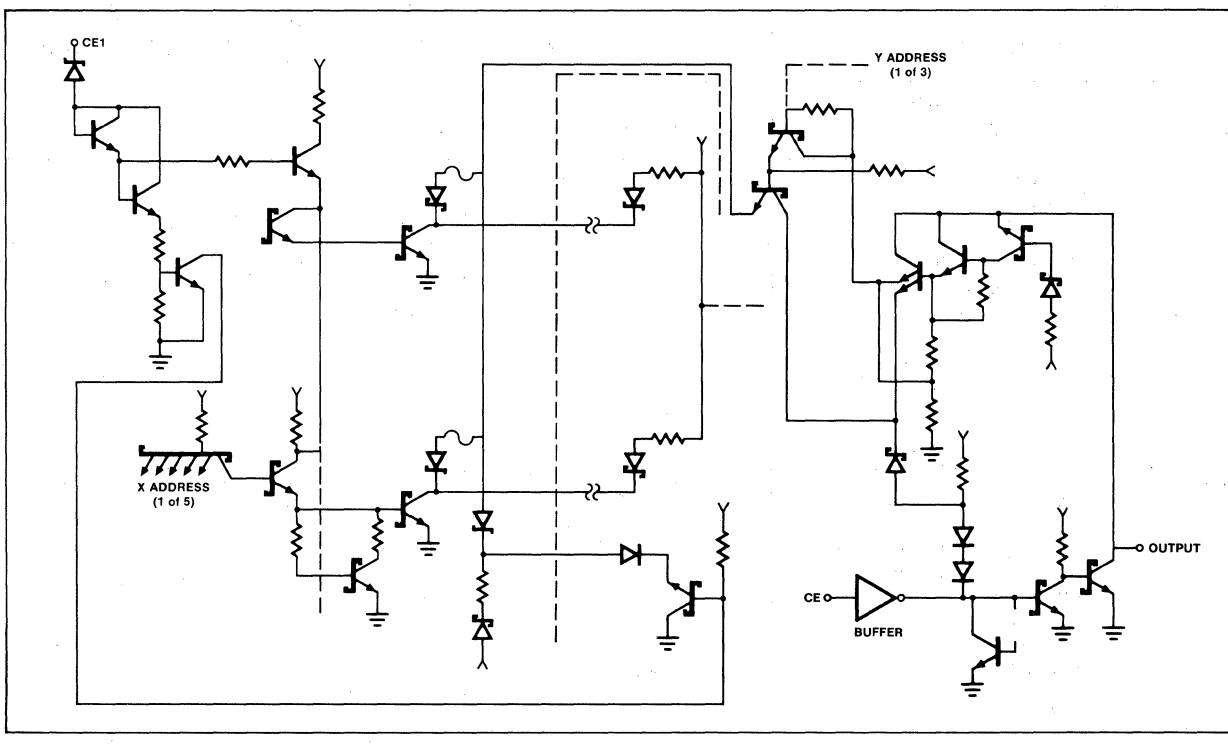
Set-up

1. Apply GND to pin 12.
2. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
3. Set $\overline{CE}_2$ to logic low.

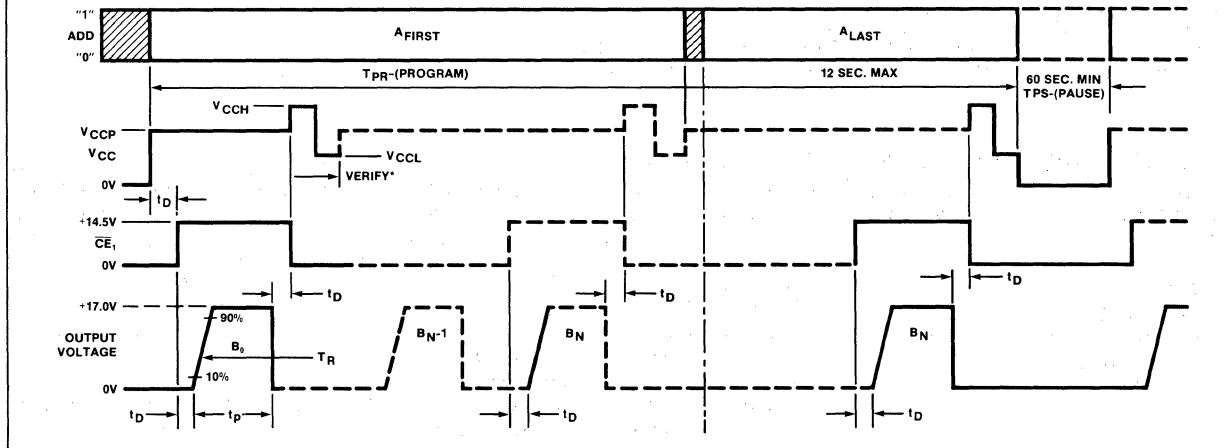
Program-Verify Sequence

1. Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL high and low logic levels to the device address inputs.
2. After 10μs delay, apply to $\overline{CE}_1$ (pin 13) a voltage source of 14.5 ± 0.5V, with 15mA sourcing current capability.
3. After 10μs delay, apply a voltage source of +17.0 ± 0.5V to the output to be programmed. The source must have a current limit of 115mA. Prgram one output at the time.
4. After 10μs delay, remove +17.0V supply from programmed output.
5. To verify programming, after 10μs delay, return $\overline{CE}_1$ to 0V. Raise V_{CC} to V_{CCH} = +5.25 ± .25V. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.75 ± .25V, and verify that the programmed output remains in the high state.
6. Raise V_{CC} to V_{CCP}, and repeat steps 2 through 5 to program other bits at the same address.
7. Repeat steps 1 through 6 to program all other address locations.

TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S126 and 82S129 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, F or N, and for the military temperature range (-55°C to +125°C) specify S82S126/129, F only.

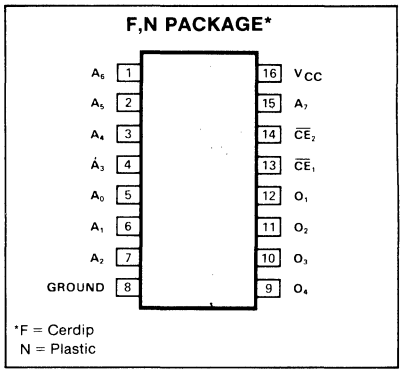
FEATURES

- **Address access time:**
  N82S126/129: 50ns max
  S82S126/129: 70ns max
- **Power dissipation: 0.5mW/bit typ**
- **Input loading:**
  N82S126/129: -100μA max
  S82S126/129: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S126: Open collector
  82S129: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

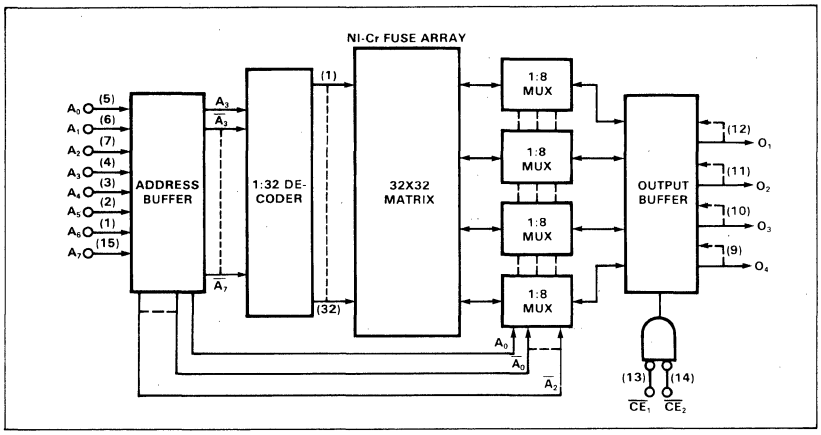
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S126)	+5.5	
V_O	Off-state (82S129)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S126/129	0 to +75	
	S82S126/129	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S126/129: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S126/129: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S126/129			S82S126/129			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S129)	$\overline{CE_1} = \overline{CE_2}$ = Low, I_{OUT} = -2.0mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S126)	$\overline{CE_1}$ or $\overline{CE_2}$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S129)	$\overline{CE_1}$ or $\overline{CE_2}$ = High, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE_1}$ or $\overline{CE_2}$ = High, V_{OUT} = 0.5V			-40			-60	
I_{OS}	Short circuit (82S129)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			105	120		105	125	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

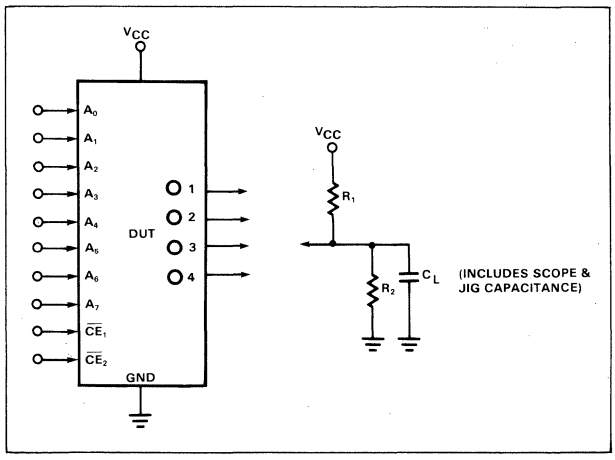
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF
N82S126/129: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S126/129: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

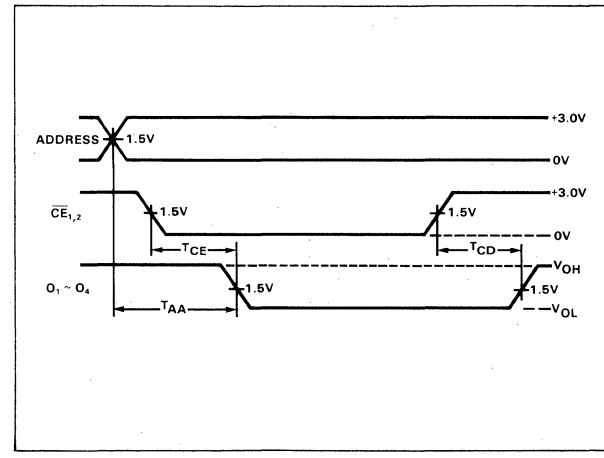
PARAMETER	TO	FROM	N82S126/129			S82S126/129			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time								ns
T_{AA}	Output	Address		35	50		35	70	
T_{CE}	Output	Chip enable		15	25		15	35	
	Disable time								ns
T_{CD}	Output	Chip disable		15	25		15	35	

NOTES
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEM SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	$I_{CCP} = 375 \pm 75mA$, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	$V_{CCP} = +8.75 \pm .25V$	300		450	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	$V_{IH} = +5.5V$			50	
I_{IL}	Low	$V_{IL} = +0.4V$			-500	
V_{OUT}	Output programming voltage[3]	$I_{OUT} = 200 \pm 20mA$, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_p	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PSI}	Initial programming pause	$V_{CC} = 0V$	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

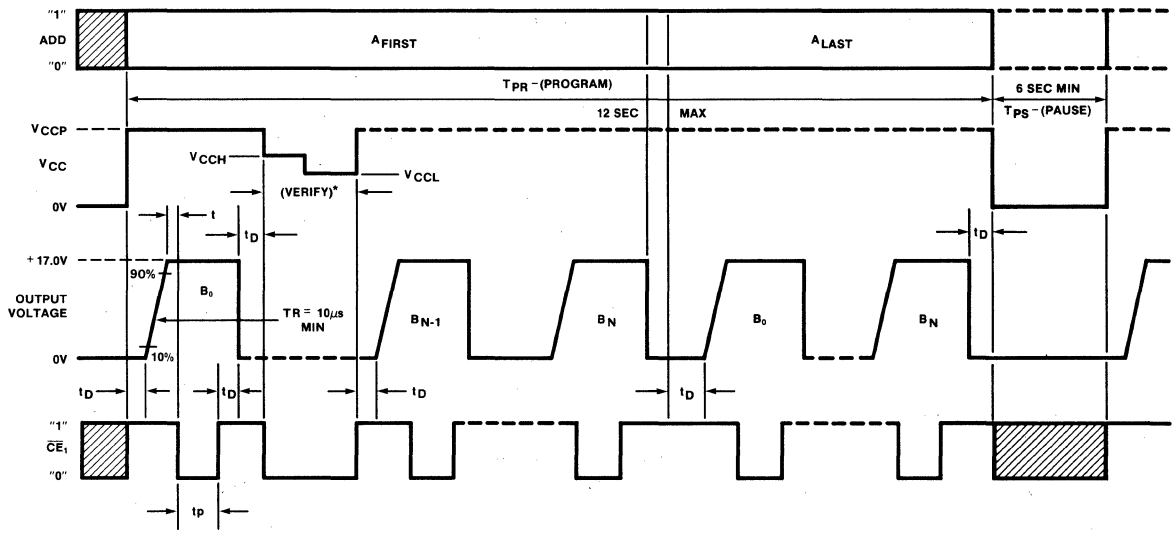
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the $17 \pm 1V$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = High, $\overline{CE}_2$ = Low.
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$.
3. After 10μs delay, apply $V_{OUT} = +17 \pm 1V$ to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2V$, and apply a logic low level to the CE input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25V$, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

10149-F

DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard device is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 10149 is suitable for use in high performance ECL systems. The outputs are capable of driving 500Ω loads.

A chip enable input is provided for ease of memory expansion.

FEATURES

- **Address access time: 20ns max**
- **Power dissipation: 0.66mW/bit typ**
- **High impedance inputs (50kΩ pulldown)**
- **Open emitter outputs (50kΩ drive)**
- **On-chip address decoding**
- **No separate fusing pins**
- **Fully compatible with ECL 10K series**

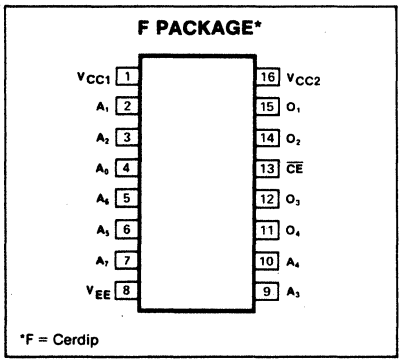
APPLICATIONS

- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

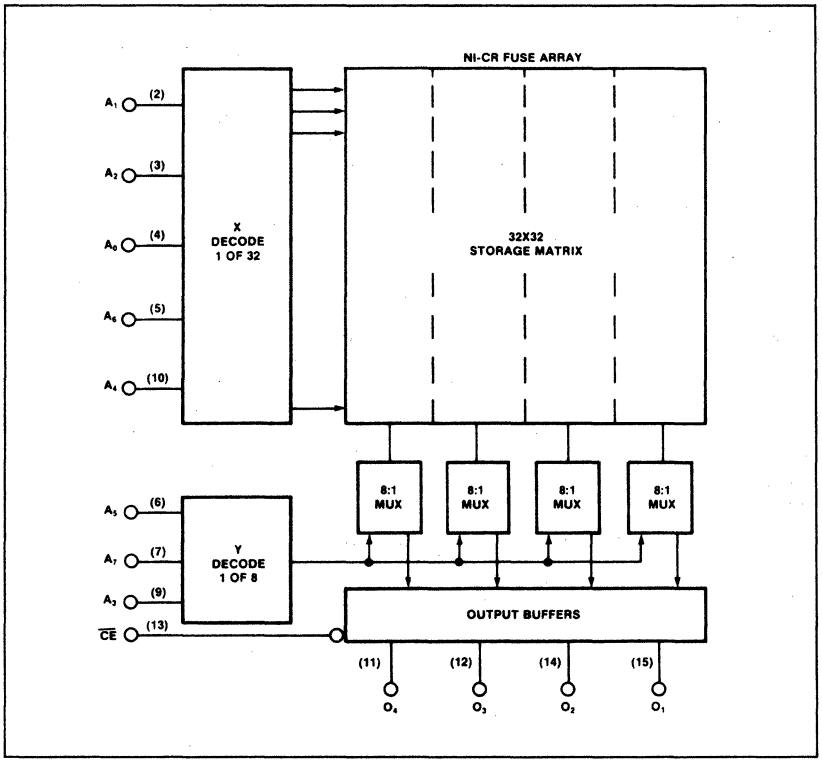
RECOMMENDED OPERATING RANGES

- **$V_{CC1} = V_{CC2} = GND$**
- **$V_{EE} = -5.2V \pm 5\%$**
- **$T_A = -30°C$ to $+85°C$ ambient**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER[1]	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	8	Vdc
V_{IN}	Input voltage (V_{CC} = 0)	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
	Temperature range		°C
T_A	Operating	-30 to +85	
T_J	Operating junction	125	
T_{STG}	Storage	-55 to +125	

10149-F

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 0V$, $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2V$

PARAMETER[1]	TEST CONDITIONS	-30°C			+25°C			+85°C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input voltage[2,3]											V
V_{IL} Low		-1.890			-1.850			-1.825			
V_{IH} High				-0.890			-0.810			-0.700	
V_{ILA} Low threshold				-1.500			-1.475			-1.440	
V_{IHA} High threshold		-1.205			-1.105			-1.035			
Output voltage											V
V_{OL} Low	V_{IH} = max	-1.89		-1.675	-1.85	-1.70	-1.65	-1.825		-1.615	
V_{OH} High	V_{IL} = min	-1.06		-0.89	-0.96	-0.89	-0.81	-0.89		-0.70	
V_{OLA} Low threshold	V_{IHA} = min, V_{ILA} = max			-1.655			-1.63			-1.595	
V_{OHA} High threshold		-1.08			-0.98			-0.91			
Input current											μA
I_{IL} Low	V_{IH} = max				0.5						
I_{IH} High	V_{IL} = min						265				
I_{EE} Supply drain current						130	150				mA

AC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{EE} = -3.2V$, $V_{CC1} = V_{CC2} = 2V$, $R_L = 50\Omega$ to ground

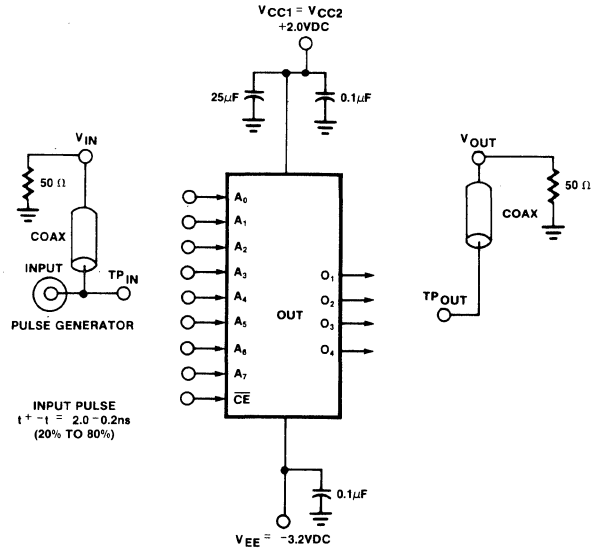
PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
Access time						ns
T_{AA}	Output	Address		12	20	
T_{CE}	Output	Chip enable		5.5	8	
T_{CD} Disable time	Output	Chip disable		5.5	8	ns
Rise and fall time						ns
t+ Rise time (20-80%)				4.0		
t- Fall time (20-80%)				4.0		

NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Vdc ± 1%.
3. Each ECL 10K series device has been designed to meet the dc specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to -2V.

10149-F

TEST LOAD CIRCUIT



NOTES

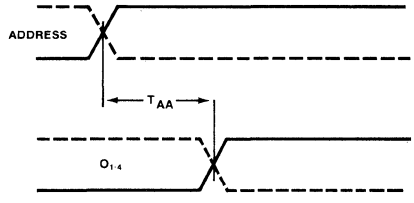
A. For ac tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.

B. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.

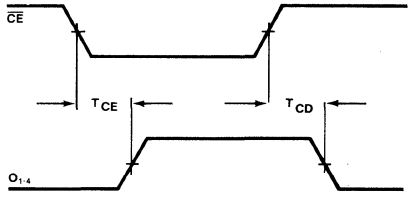
C. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as possible. A 10μF capacitor between V_{CC1} and V_{CC} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS

ADDRESS ACCESS TIME



CHIP ENABLE/DISABLE PROPAGATION DELAYS

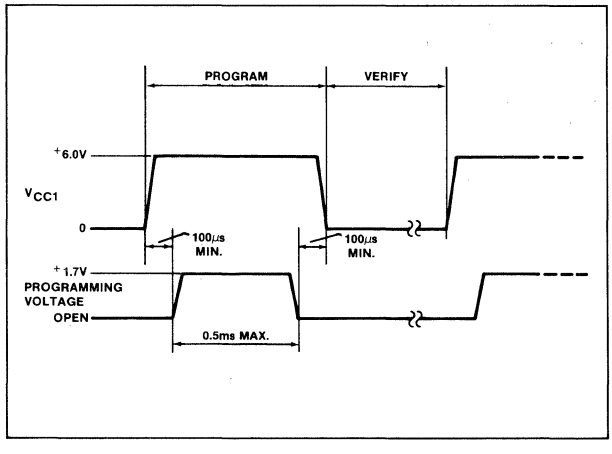


10149-F

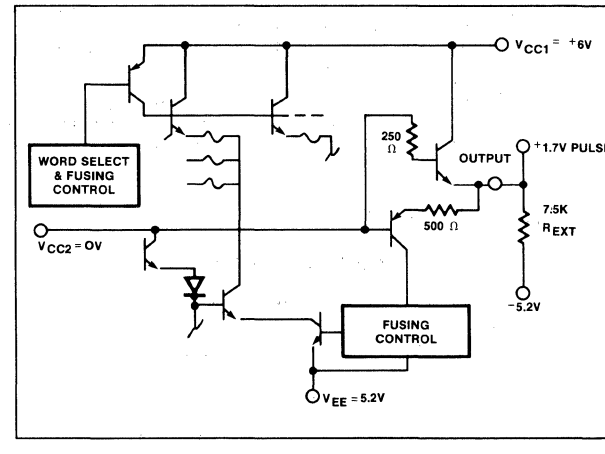
PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{EE}	Program/verify		-5.46	-5.2	-4.94	
V_{CC1p}	To program	See steps 4 and 8 in Programming Procedure	5.7	6.0	6.3	
V_{CC1v}	To verify			0		
	Programming supply current					mA
I_{EEP}		$V_{EE} = -5.2V$	300			
I_{CC1p}		$V_{CC1} = 6.0V$	150			
	Input voltage					V
V_{IH}	High		-0.90	-.75	-0.60	
V_{IL}	Low		-2.0	-1.80	-1.60	
	Output voltage					V
V_{OUT}	Programming	$I_{OUT} = 4.0mA$	1.50	1.70	1.90	
V_{VOUT}	Verify 1		-1.0		-1.50	
	Verify 0					
t_P	Output programming pulse width		.25		.5	ms
t_D	Pulse sequence delay		100			μs
T_{PR}	Programming time	$V_{CC1} = +6V$			6	sec
T_{PS}	Programming pause	$V_{CC1} = V_{CC2} = V_{EE} = 0V$	6			sec

TYPICAL PROGRAMMING SEQUENCE



TYPICAL FUSING PATH



PROGRAMMING PROCEDURE

The 10149 is shipped with all bits at logical low. To write logical high, proceed as follows:

1. Terminate all device outputs with 7.5kΩ to -5.2V.
2. Connect V_{EE} (pin 8) to -5.2V ± 5% and V_{CC2} (pin 16) to GND (0V).
3. Address the desired location by applying a voltage of -.75 ± .15V for a high and a voltage of -1.80 ± .20V for a low at the address inputs.
4. Apply +6.0V ± 5% to V_{CC1} (pin 1).
5. Allow a minimum delay of 100μs and apply a voltage of +1.7V ± 0.2V to the output to be programmed. Program one output at a time.
6. Hold the output programming voltage for 0.25 to 0.5ms, and then disconnect the voltage source from the programmed output.
7. Allow a minimum delay of 100μs and then reduce V_{CC1} to GND (0V) to verify programmed output.
8. Repeat steps 4 through 7 to program other bits of the word.
9. Change the address and repeat steps 4 through 8 until the entire bit pattern is programmed into your custom 10149.
10. Verify complete truth table.

DESCRIPTION

The 82S114 and 82S115 are field programmable and include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by CE1 and CE2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

Both 82S114 and 82S115 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S114/115, F or N, and for the military temperature range (-55°C to +125°C) specify S82S114/115, F.

FEATURES

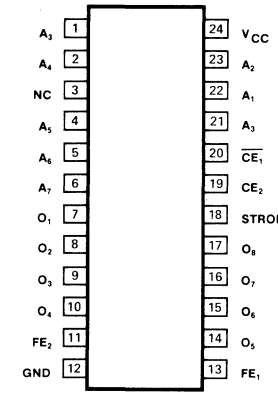
- **Address access time:**
  N82S114/115: 60ns max
  S82S114/115: 90ns max
- **Power dissipation: 165μW/bit typ**
- **Input loading:**
  N82S114/115: -100μA max
  S82S114/115: -150μA max
- **On-chip storage latches**
- **Schottky clamped**
- **Fully compatible with Signetics 82S214 and 82S215 ROMs**
- **Fully TTL compatible**

APPLICATIONS

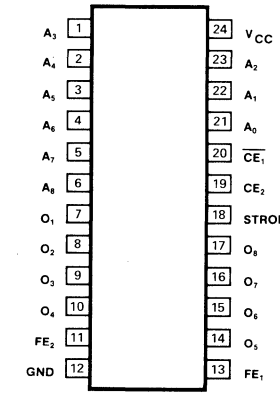
- **Microprogramming**
- **Hardwire algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATIONS

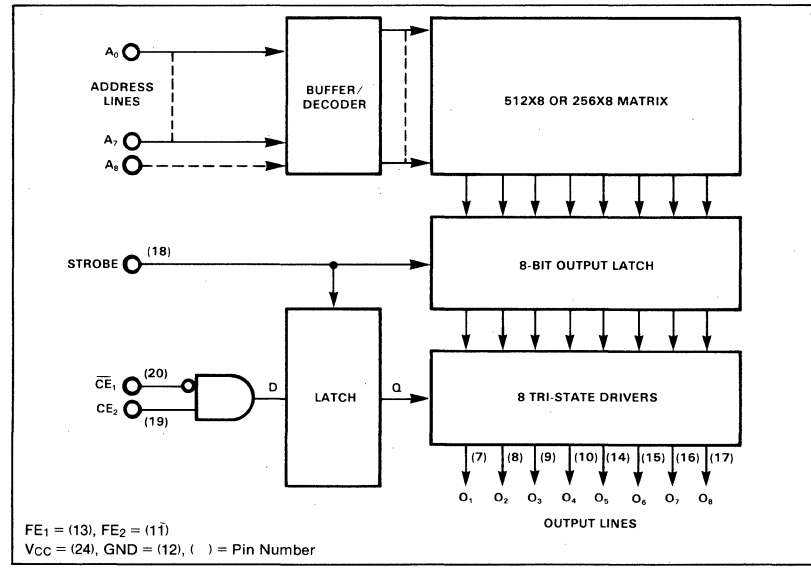
F,N PACKAGE
82S114



F,N PACKAGE
82S115



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating		
	N82S114/115	0 to +75	
	S82S114/115	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S114/115: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S114/115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S114/115			S82S114/115			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low				.85			.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	$I_{OUT} = 9.6mA$		0.4	0.45		0.4	0.5	
V_{OH}	High	$\overline{CE_1}$ = Low, CE_2 = High, $I_{OUT} = -2mA$, High stored	2.7	3.3		2.4	3.3		
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			25			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE_1}$ = High or CE_2 = O, $V_{OUT} = 5.5V$			40			100	μA
		$\overline{CE_1}$ = High or CE_2 = O, $V_{OUT} = 0.5V$			-40			-100	
I_{OS}	Short circuit[2]	V_{OUT} = OV	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175		130	185	mA
	Capacitance	$V_{CC} = 5.0V$, $V_{IN} = 2.0V$							pF
C_{IN}	Input	$V_{CC} = 5.0V$, $V_{OUT} = 2.0V$		5			5		
C_{OUT}	Output	$\overline{CE_1}$ = High or CE_2 = 0		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S114/115: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S114/115: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

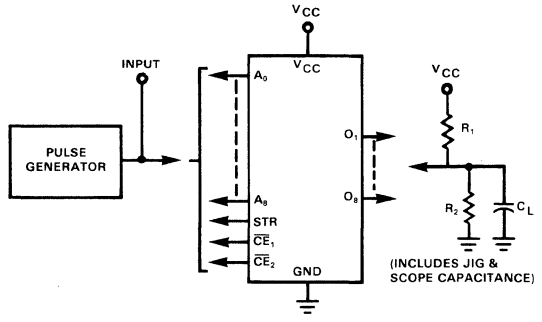
PARAMETER		TO	FROM	TEST CONDITIONS	N82S114/115			S82S114/115			UNIT
					Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time[3]			Latched or transparent read							ns
T_{AA}		Output	Address			35	60		35	90	
T_{CE}		Output	Chip enable			20	40		20	50	
	Disable time[3]			Latched or transparent read							ns
T_{CD}		Output	Chip disable			20	40		20	50	
	Setup and hold time[4]			Latched read only							ns
T_{CDS}	Setup time	Output	Chip enable		40			50			
T_{CDH}	Hold time				10	0		10	0		
T_{ADH}	Hold time	Output	Address		0	-10		5	-10		
	Pulse width[4]			Latched read only							ns
T_{SW}	Strobe				30	20		40	20		
	Latch time[4]			Latched read only							ns
T_{SL}	Strobe				60	35		90	35		
	Delatch time[4]			Latched read only							ns
T_{DL}	Strobe						30			35	

NOTES on following page.

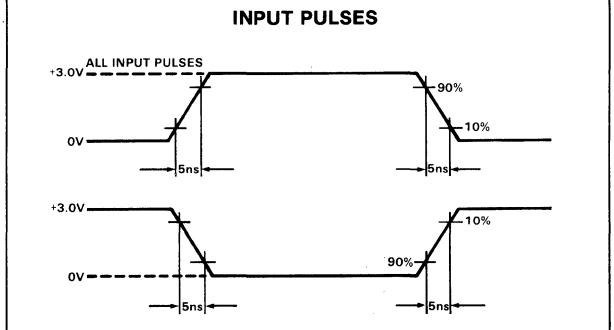
NOTES

1. Typical values are at V_{CC} = +5.0V and T_A = +25°C.
2. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
3. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_A nanoseconds after the address has changed the T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.
4. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
5. During operation the fusing pins FE1 and FE2 may be grounded or left floating.
6. Positive current is defined as into the terminal referenced.

TEST LOAD CIRCUIT

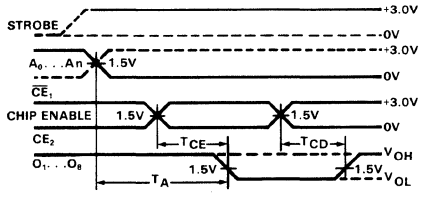


VOLTAGE WAVEFORM



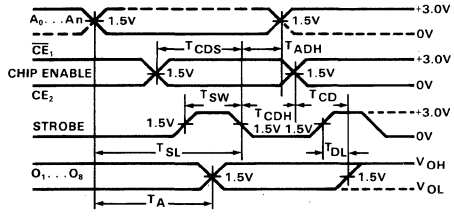
TIMING DIAGRAMS

TRANSPARENT READ[4]



Output Latches Not Used

LATCHED READ[5]



Output Latches Used

PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Power supply voltage					V
V_{CCP}	To program[1]	I_{CCP} = 200 ± 25mA, Transient or steady state	4.75	5.0	5.25	
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		0.9	1.0	1.1	V
I_{CCP}	Programming supply current	V_{CCP} = +5.0 ± .25V	175	200	225	mA
	Input voltage					V
V_{IL}	Low		0	0.4	0.8	
V_{IH}	High		2.4		5.5	
	Input current (FE_1 & FE_2 only)					
I_{IL}	Low	V_{IL} = +0.45V			-100	μA
I_{IH}	High	V_{IH} = +5.5V			10	mA
	Input current (except FE_1 & FE_2)					μA
I_{IL}	Low	V_{IL} = +0.45V			-100	
I_{IH}	High	V_{IH} = +5.5V			25	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_P	FE_2 programming pulse width		0.3	0.4	0.5	ms
T_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS}	Programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%

NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period (V_{CC} = 0V) of 3ms.

RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical low. To write logical high, proceed as follows:

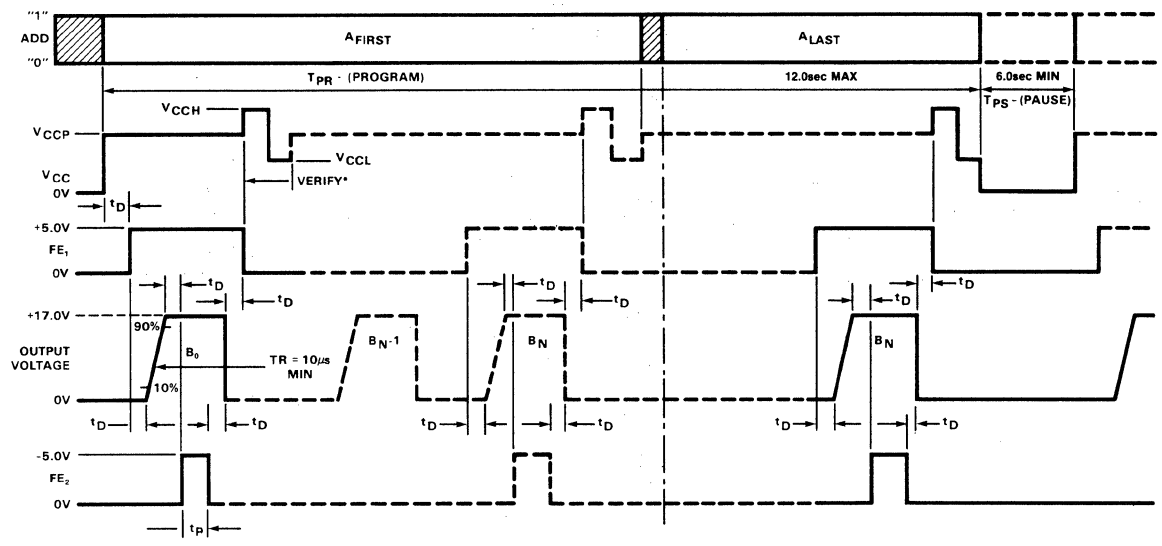
SET-UP

1. Apply GND to pin 12.
2. Terminate all device outputs with a 10kΩ resistor to V_{CC}.
3. Set $\overline{CE}_1$ to logic low, and CE_2 to logic high (TTL levels).
4. Set Strobe to logic high level.

Program-Verify Sequence

1. Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL high and low logic levels to the device address inputs.
2. After 10μs delay, apply to FE_1 (pin 13) a voltage source of +5.0 ± 0.5V, with 10mA sourcing current capability.
3. After 10μs delay, apply a voltage source of +17.0 ± 1.0V to the output to be programmed. The source must have a current limit 200mA. Program on output at the time.
4. After 10μs delay, raise FE_2 (pin 11) from 0V to +5.0 ± 0.5V for a period of 1ms, and then return to 0V. Pulse source must have a 10mA sourcing current capability.
5. After 10μs delay, remove +17.0V supply from programmed output.
6. To verify programming, after 10μs delay, return FE_1 to 0V. Raise V_{CC} to V_{CCH} = +5.5 ± .2V. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} and repeat steps 2 through 6 to program other bits at the same address.
8. Repeat steps 1 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S130-F,N • 82S131-F,N

DESCRIPTION

The 82S130 and 82S131 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S130 and 82S131 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S130 and 82S131 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0° to +75°C) specify N82S130/131, F or N, and for the military temperature range (-55°C to +125°C) specify S82S130/131, F.

FEATURES

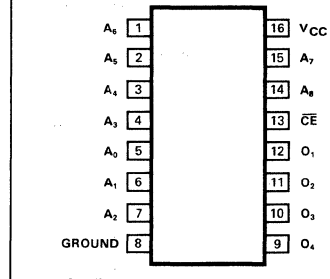
- **Address access time:**
  N82S130/131: 50ns max
  S82S130/131: 70ns max
- **Power dissipation: 0.3mW/bit typ**
- **Input loading:**
  N82S130/131: -100μA max
  S82S130/131: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S130: Open collector
  82S131: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

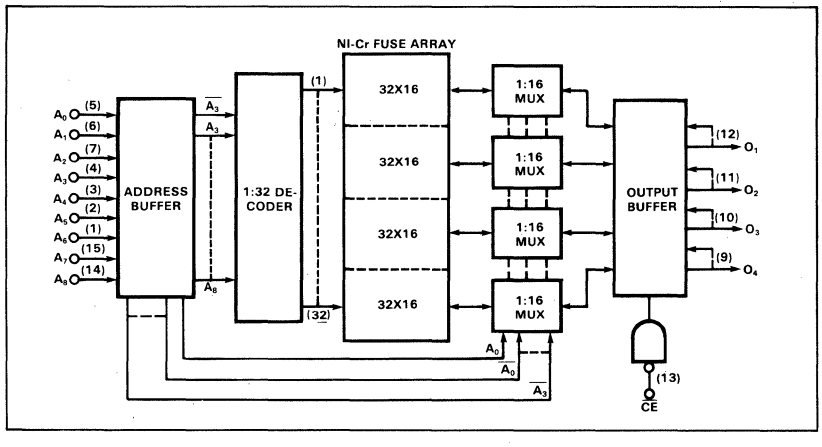
PIN CONFIGURATION

F,N PACKAGE*



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S130)	+5.5	
V_O	Off-state (82S131)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S130/131	0 to +75	
	S82S130/131	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S130/131: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S130/131: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S130/131			S82S130/131			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S131)	$\overline{CE}$ = low, I_{OUT} = -2mA high stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		40				-150	
I_{IH}	High	V_{IN} = 5.5V		.85				50	
	Output current								
I_{OLK}	Leakage (82S130)	$\overline{CE}$ = high, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S131)	$\overline{CE}$ = high, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE}$ = high, V_{OUT} = 0.5V			-40			-60	
I_{OS}	Short circuit (82S131)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			120	140		120	140	mA
	Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V							pF
C_{IN}	Input			5			5		
C_{OUT}	Output			8			8		

AC ELECTRICAL CHARACTERISTICS

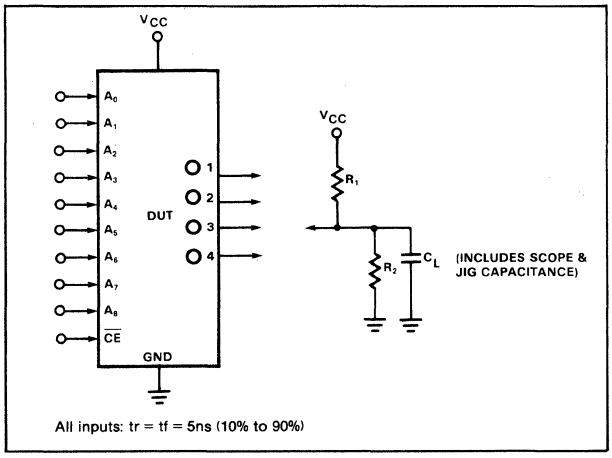
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$[2]
N82S130/131: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S130/131: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S130/131			S82S130/131			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time								ns
T_{AA}	Output	Address		40	50		40	70	
T_{CE}	Output	Chip enable		20	30		20	40	
	Disable time								ns
T_{CD}	Output	Chip disable		20	30		20	40	

NOTES

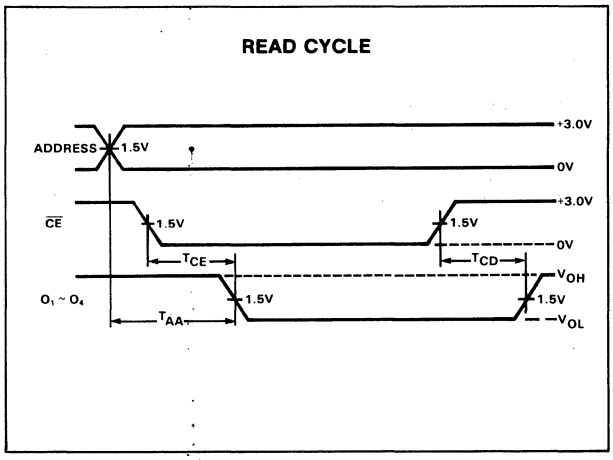
1. Typical values are at V_{CC} = 5.0V, T_A = +25°C.
2. Positive current is defined as into the terminal referenced.

TEST LOAD CIRCUIT



All inputs: tr = tf = 5ns (10% to 90%)

VOLTAGE WAVEFORM



PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 375 ± 75mA, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	300		450	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CCP} = V_{CCP}$			12	sec
T_{PSI}	Initial programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

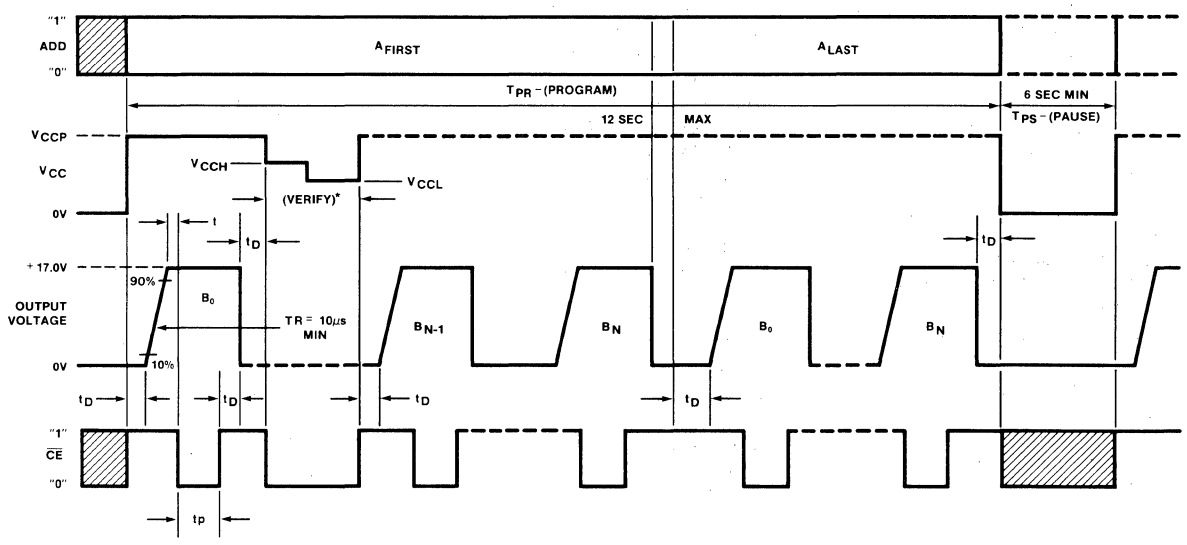
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. VS is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10K resistor to V_{CC}. Apply $\overline{CE}_1$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the CE input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S140-F,N • 82S141-F,N

DESCRIPTION

The 82S140 and 82S141 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S140 and 82S141 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S140 and 82S141 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S140/141, F, and for the military temperature range (-55°C to +125°C) specify S82S140/141, F.

FEATURES

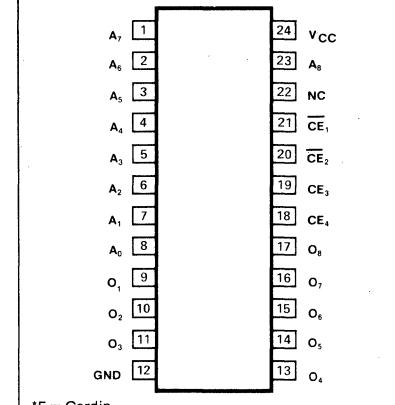
- **Address access time:**
  N82S140/141: 60ns max
  S82S140/141: 90ns max
- **Power dissipation: .17mW/bit typ**
- **Input loading:**
  N82S140/141: -100μA max
  S82S140/141: -150μA max
- **On-chip address decoding**
- **Output options:**
  S82S140: Open collector
  S82S141: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

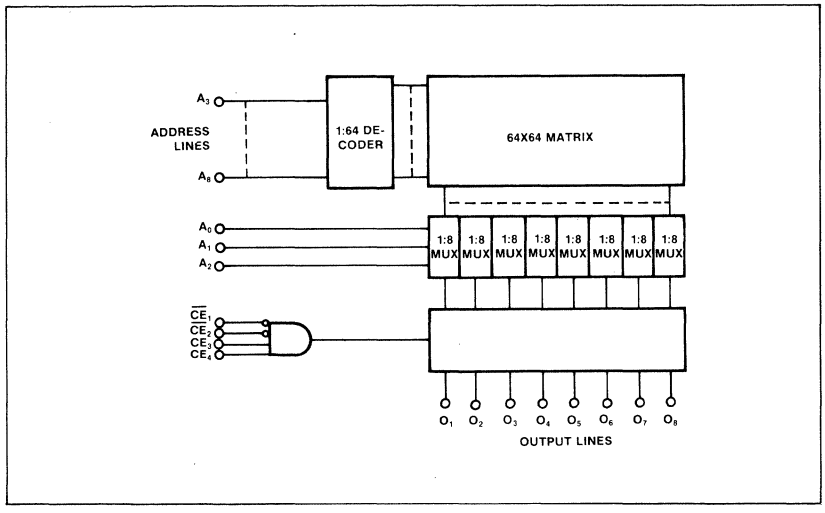
PIN CONFIGURATION

F,N PACKAGE *



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S140)	+5.5	
V_O	Off-state (82S141)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S140/141	0 to +75	
	S82S140/141	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S140/141: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S140/141: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS[1]	N82S140/141			S82S140/141			UNIT
		Min	Typ[2]	Max	Min	Typ[2]	Max	
Input voltage								V
V_{IL} Low				.85			.80	
V_{IH} High		2.0			2.0			
V_{IC} Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
Output voltage								V
V_{OL} Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH} High (82S141)	$\overline{CE_1}$ = Low, I_{OUT} = -2mA, $\overline{CE_2}$ = Low, CE_3 = High, CE_4 = High, High stored	2.4			2.4			
Input current								μA
I_{IL} Low	V_{IN} =0.45V			-100			-150	
I_{IH} High	V_{IN} = 5.5V			40			50	
Output current								
I_{OLK} Leakage (82S140)	$\overline{CE_1}$ = High, V_{OUT} = 5.5V, $\overline{CE_2}$ = High, CE_3 = Low, CE_4 = Low			40			60	μA
$I_{O(OFF)}$ Hi-Z state (82S141)	$\overline{CE_1}$ = High, V_{OUT} = 0.5V, $\overline{CE_2}$ = High, CE_3 = Low, CE_4 = Low			-40			-60	μA
	$\overline{CE_1}$ = High, V_{OUT} = 5.5V, $\overline{CE_2}$ = High, CE_3 = Low, CE_4 = Low			40			60	
I_{OS} Short circuit (82S141)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC} V_{CC} supply current			140	175		140	185	mA
Capacitance	V_{CC} = 5.0V							pF
C_{IN} Input	V_{IN} = 2.0V		5			5		
C_{OUT} Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

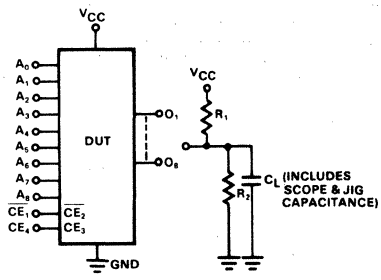
R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S140/141: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S140/141: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S140/141			S82S140/141			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		40	60		40	90	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

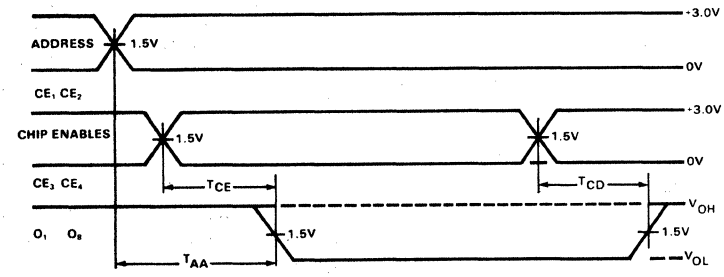
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



tr = tf = 5ns (10% to 90%)

PROGRAMMING SYSTEMS SPECIFICATIONS

(Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 375 ± 75mA, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	300		450	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_P	CE programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	V_{CC} = V_{CCP}			12	sec
T_{PSI}	Initial programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

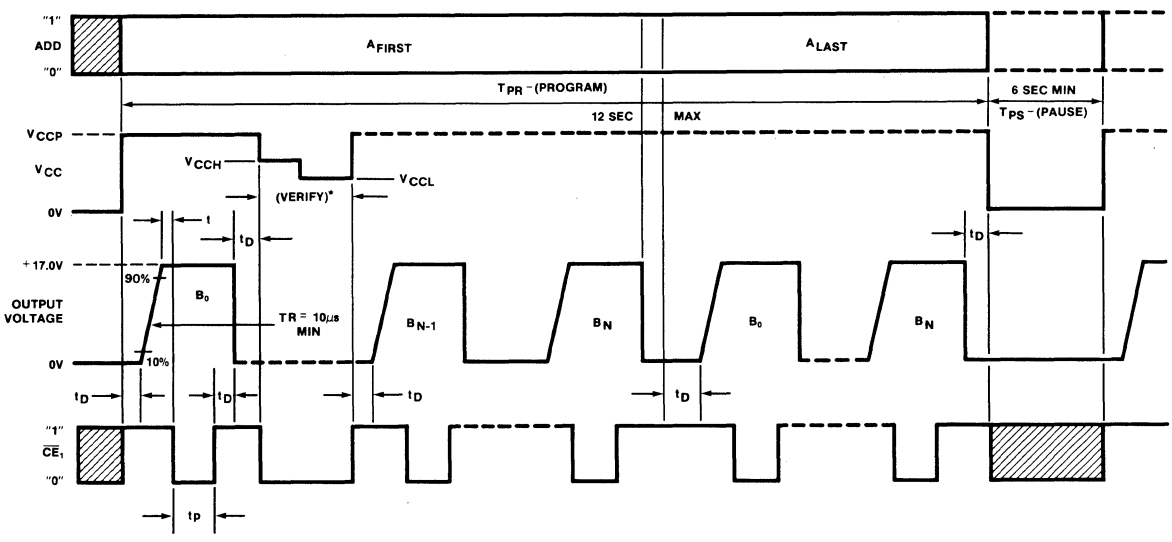
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = High, $\overline{CE}_2$ = Low, CE_3 = High and CE_4 = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the CE input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

DESCRIPTION

The 82S136 and 82S137 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S136 and 82S137 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

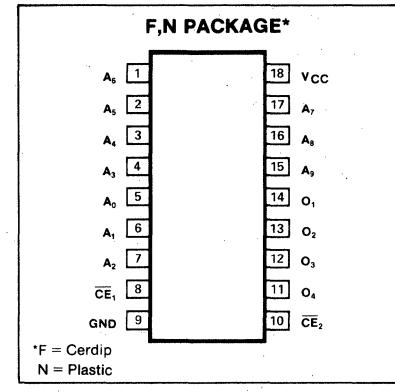
These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S136 and 82S137 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S136/137, F or N, and for the military temperature range (-55°C to +125°C) specify S82S136/137, F.

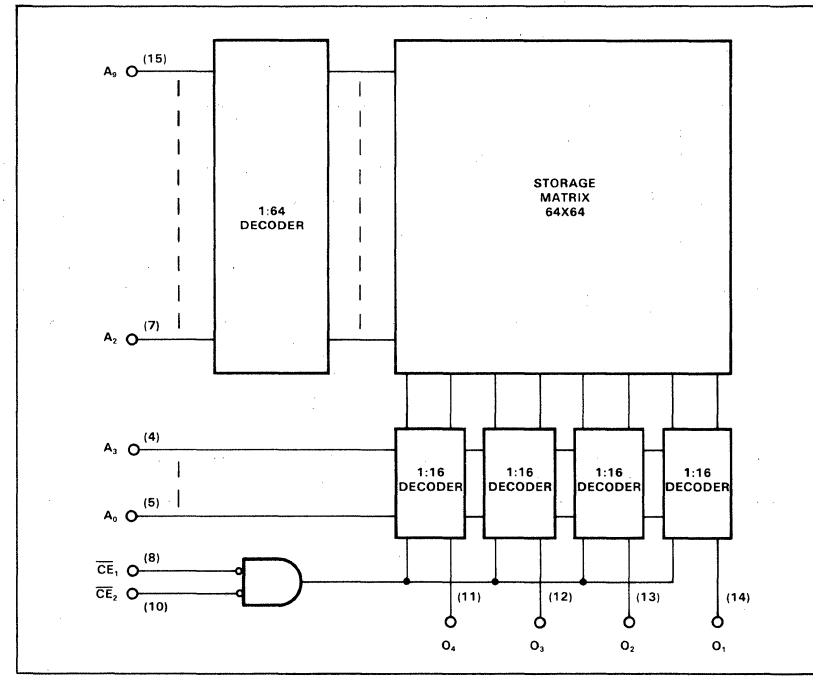
FEATURES

- **Address access time:**
  - **N82S136/137: 60ns max**
  - **S82S136/137: 80ns max**
- **Power dissipation: .13mW/bit typ**
- **Input loading:**
  - **N82S136/137: -100μA max**
  - **S82S136/137: -150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S136: Open collector**
  - **82S137: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S136)	+5.5	
V_O	Off-state (82S137)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S136/137	0 to +75	
	S82S136/137	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S136/137: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S136/137: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S136/137			S82S136/137			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S137)	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S136)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Off-state (82S137)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit (82S137)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			105	140		105	140	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

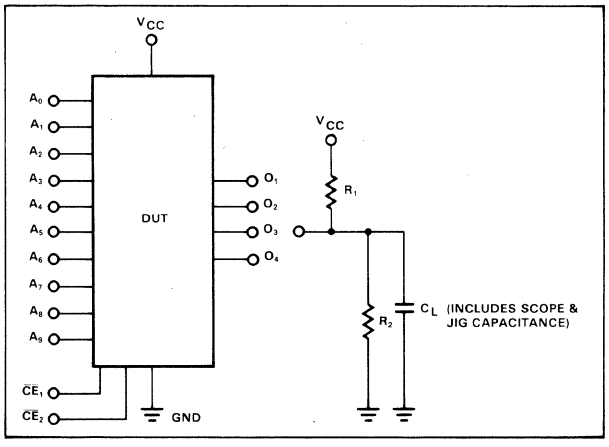
$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF[1]
N82S136/137: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S136/137: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S136/137			S82S136/137			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		40	60		40	80	
T_{CE}	Output	Chip enable		20	30		20	40	
Disable time									ns
T_{CD}	Output	Chip disable		20	30		20	40	

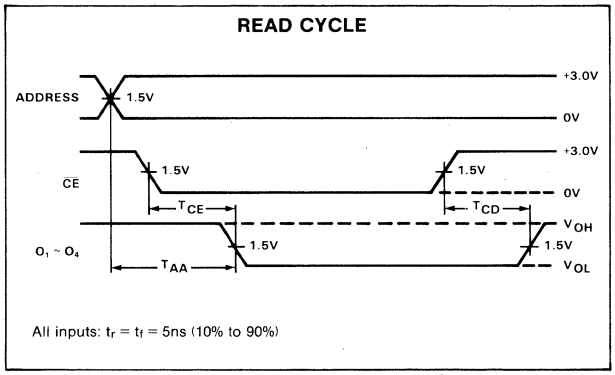
NOTES

1. Positive current is defined as into the terminal referenced.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 375 ± 75mA, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	300		450	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_P	CE programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	V_{CC} = V_{CCP}			12	sec
T_{PSI}	Initial programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

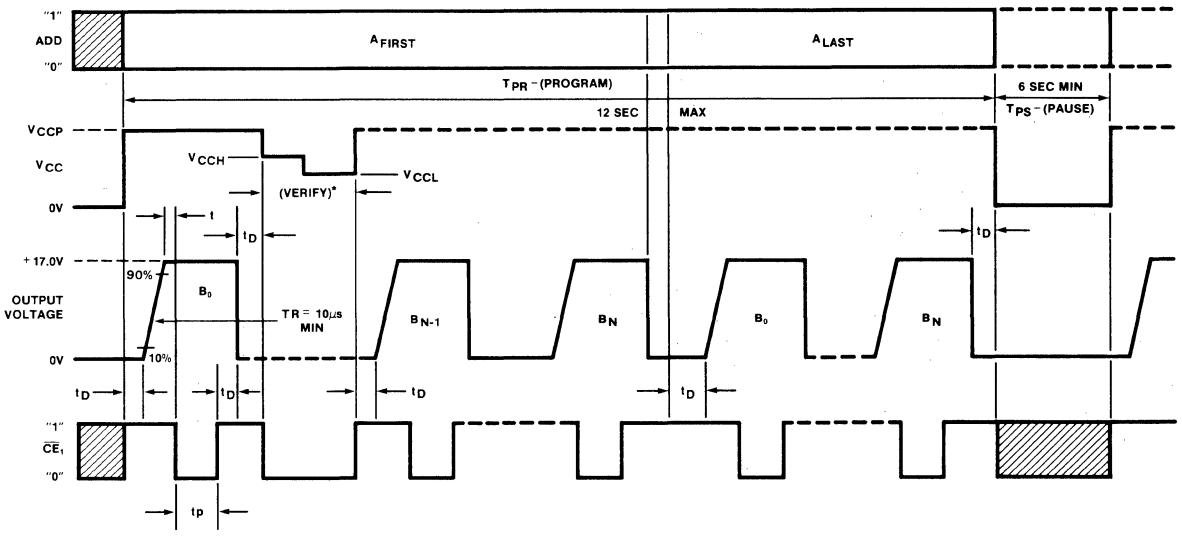
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10KΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = High $\overline{CE}_2$ = Low.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} V_{CCH} = +5.5 ± .2V, and apply a logic low level to the CE input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S180-F,N • 82S181-F,N

DESCRIPTION

The 82S180 and 82S181 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S180 and 82S181 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

The 82S180 and 82S181 are available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S180/181, F or N, and for the military temperature range (-55°C to +125°C) specify S82S180/181, F.

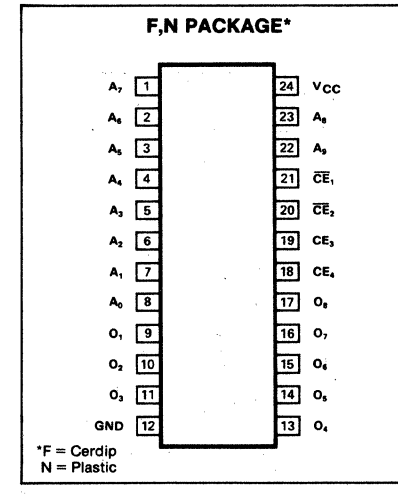
FEATURES

- **Address access time:**
  N82S180/181: 70ns max
  S82S180/181: 90ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
  N82S180/181: -100μA max
  S82S180/181: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S180: Open collector
  82S181: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

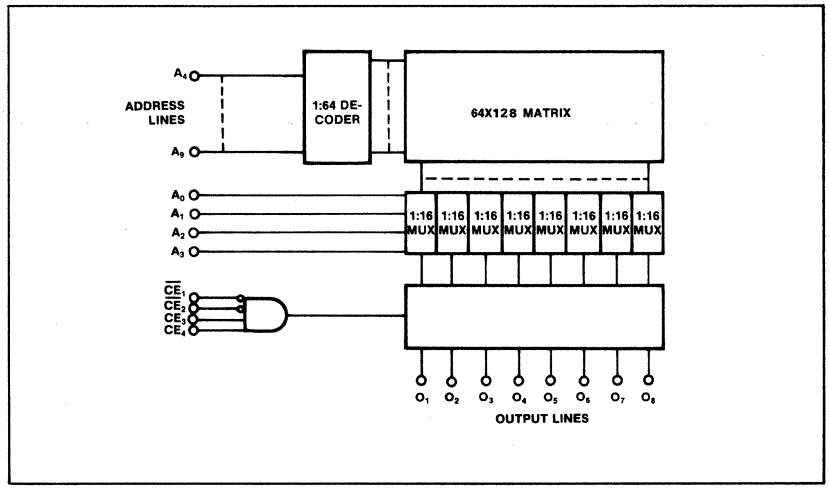
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S180)	+5.5	
V_O	Off-state (82S181)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S180/181	0 to +75	
	S82S180/181	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S180/181: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S180/181: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S180/181			S82S180/181			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High (82S181)	$\overline{CE_1}$ = low, I_{OUT} = -2mA, $\overline{CE_2}$ = low, CE_2 = high, CE_4 = high, high stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S180)	$\overline{CE_1}$ = high, V_{OUT} = 5.5V, $\overline{CE_2}$ = high, CE_3 = low, CE_4 = low			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S181)	$\overline{CE_1}$ = high, V_{OUT} = 0.5V, $\overline{CE_2}$ = high, CE_3 = low, CE_4 = low			-40			-60	μA
		$\overline{CE_1}$ = high, V_{OUT} = 5.5V, $\overline{CE_2}$ = high, CE_3 = low, CE_4 = low			40			60	μA
I_{OS}	Short circuit (82S181)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			140	175		140	185	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

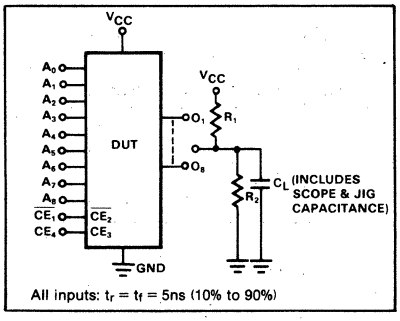
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S180/181: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S180/181: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC}$ 5.5V

PARAMETER	TO	FROM	N82S180/181			S82S180/181			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		50	70		50	90	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

NOTES

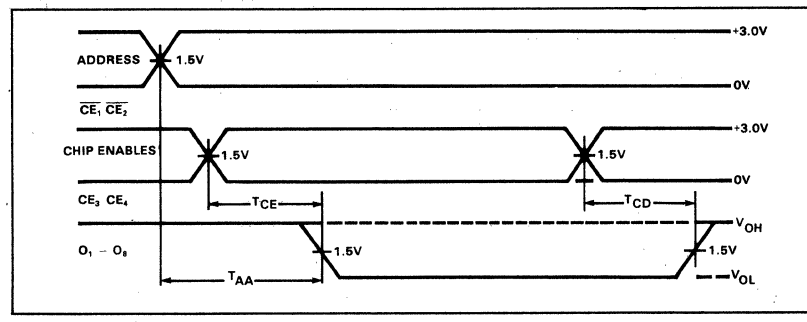
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

VOLTAGE WAVEFORM



PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	$I_{CCP} = 375 \pm 75mA$, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	$V_{CCP} = +8.75 \pm .25V$	300		450	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	$V_{IH} = +5.5V$			50	
I_{IL}	Low	$V_{IL} = +0.4V$			-500	
V_{OUT}	Output programming voltage[3]	$I_{OUT} = 200 \pm 20mA$, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	$V_{OUT} = +17 \pm 1V$	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_p	CE programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PSI}	Initial programming pause	$V_{CC} = 0V$	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

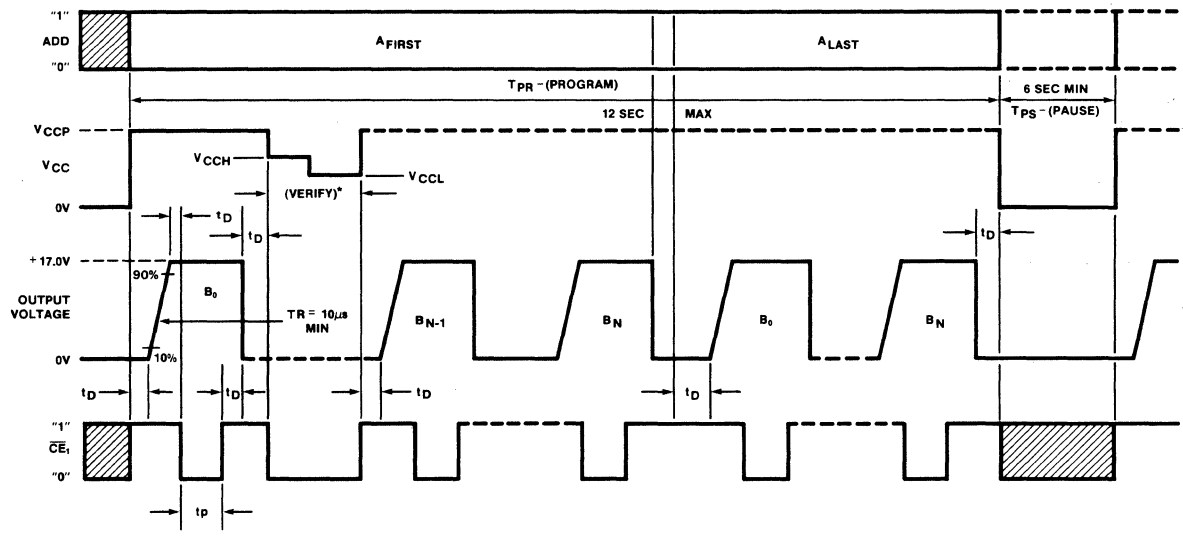
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the $17 \pm 1V$ output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = High, $\overline{CE}_2$ = Low, CE_3 = High and CE_4 = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the $\overline{CE}_1$ input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

82S2708-F,N

DESCRIPTION

The 82S2708 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S2708 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S2708 is available in both the commercial and military temperature ranges. For the commercial temperature range (0° to +75°C) specify N82S2708, and for the military temperature range (-55°C to +125°C) specify S82S2708.

APPLICATIONS

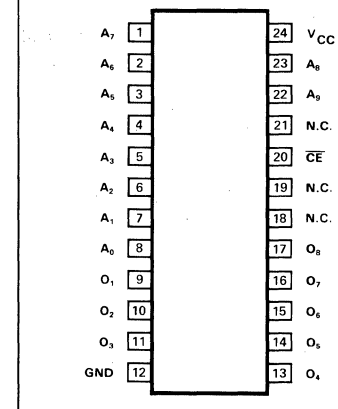
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

FEATURES

- **Address access time:**
  N82S2708: 70ns max
  S82S2708: 90ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
  N82S2708: -100μA max
  S82S2708: -150μA max
- **Chip enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Pin for pin replacement for 2708 EROM**
- **Fully TTL compatible**

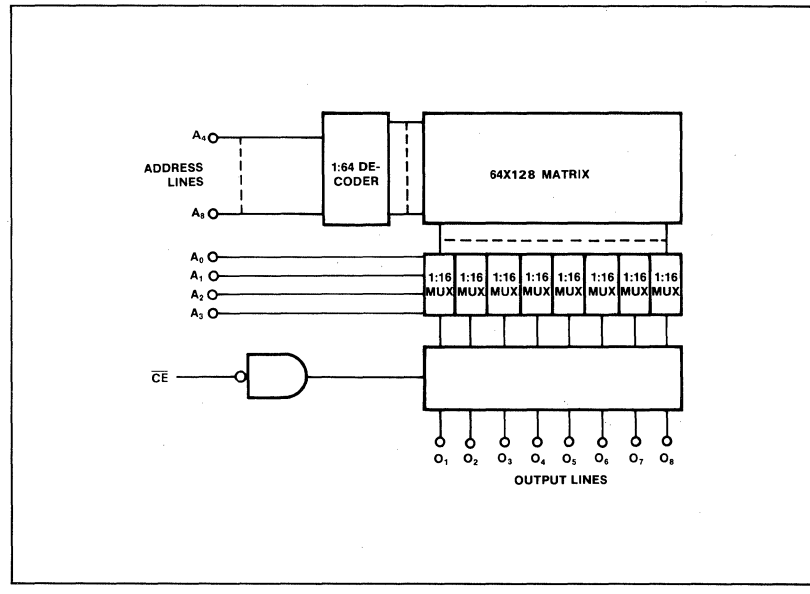
PIN CONFIGURATION

F,N PACKAGE*



*F = Cerdip
N = Plastic
NC = No connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S2708	0 to +75	
	S82S2708	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S2708: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S2708: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S2708			S82S2708			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45			0.5	
V_{OH}	High	$I_{OUT} = -2.0mA$, $\overline{CE}$ = Low, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High, $V_{OUT} = 0.5V$			-40			-60	μA
		$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40			60	
I_{OS}	Short circuit	$V_{OUT} = 0V$	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			140	175		140	185	mA
	Capacitance	$V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

AC ELECTRICAL CHARACTERISTICS

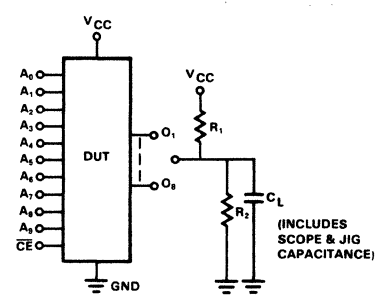
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S2708: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S2708: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S2708			S82S2708			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}		Output	Address		50	70		50	90	
T_{CE}		Output	Chip enable		20	40		20	50	
	Disable time									ns
T_{CD}		Output	Chip disable		20	40		20	50	

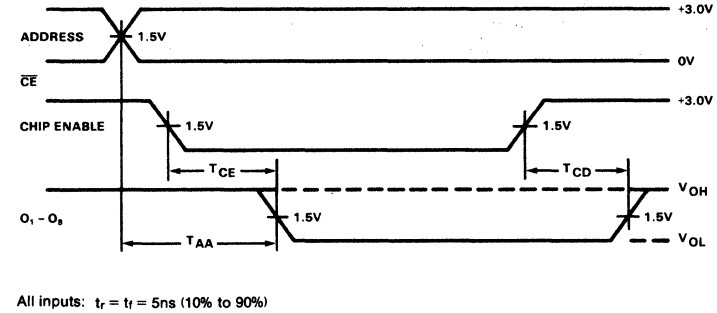
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are $V_{CC} = 5.0V$, $T_A = +25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 375 ± 75mA, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	300		450	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_p	CE programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	V_{CC} = V_{CCP}			12	sec
T_{PSI}	Initial programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

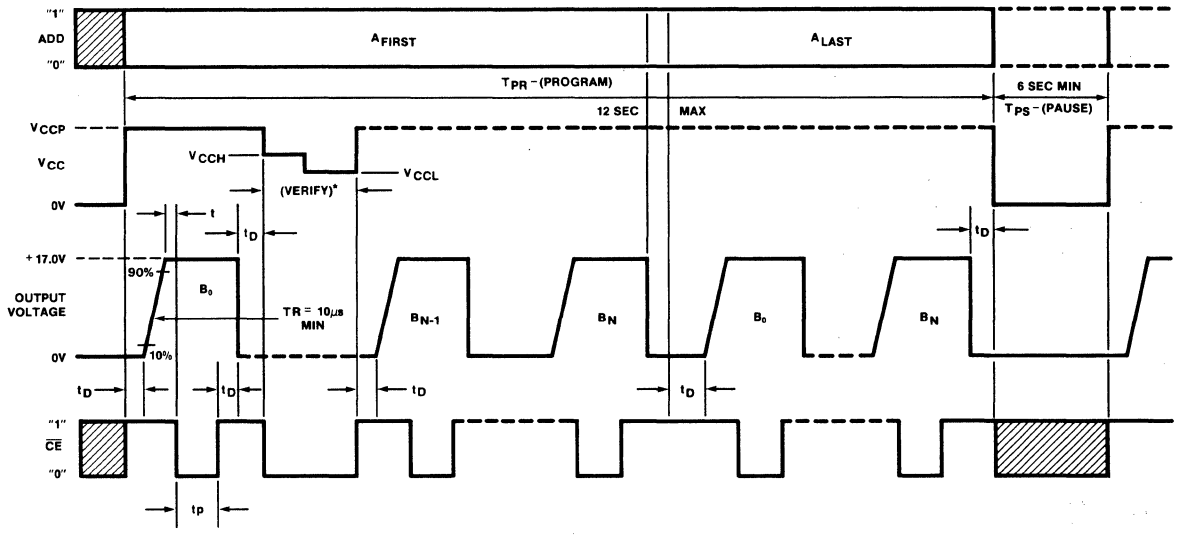
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the $\overline{CE}$ input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

DESCRIPTION

The 82S184 and 82S185 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S184 and 82S185 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

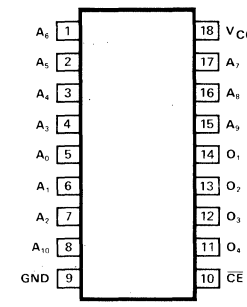
These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S184 and 82S185 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C specify N82S184/185, I, and for the military temperature range (-55°C to +125°C) specify S82S184/185, I.

FEATURES

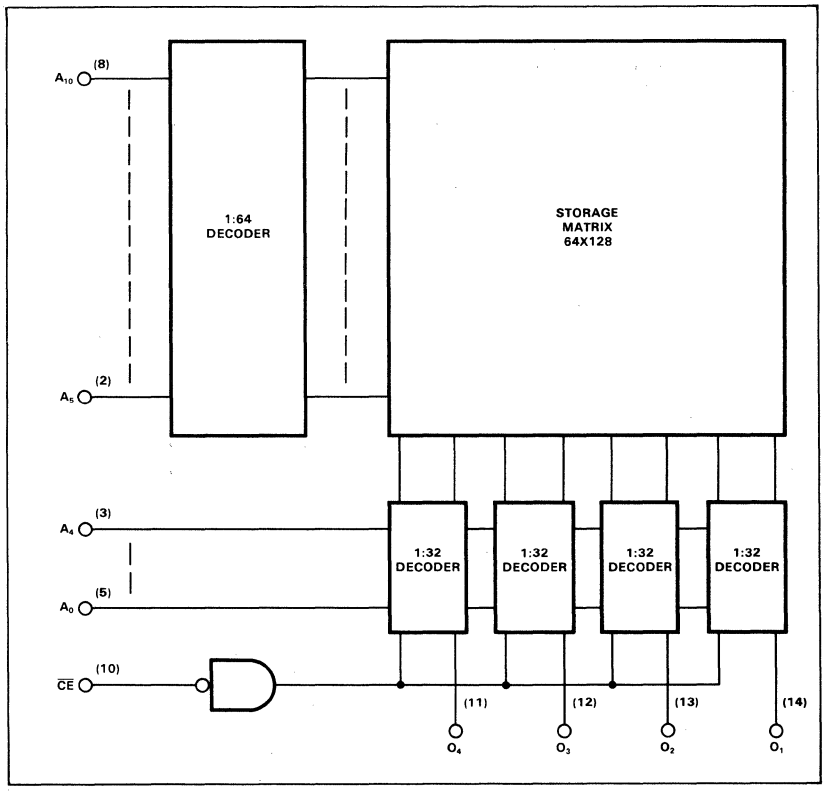
- **Low power dissipation: 50μW/bit typ**
- **Address access time:**
  N82S184/185: 100ns max
  S82S184/185: 150ns max
- **Input loading:**
  N82S184/185: -100μA max
  S82S184/185: -150μA max
- **On-chip address decoding**
- **Output options:**
  82S184: Open collector
  82S185: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

I PACKAGE*



*I = Cerdip

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S184)	+5.5	
V_O	Off-state (82S185)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S184/185	0 to +75	
	S82S184/185	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S184/185: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S184/185: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	N82S184/185			S82S184/185			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S185)	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN}= 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S184)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	μA
I_O (OFF)	Hi-Z state (82S185)	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit (82S185)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			80	120		80	130	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

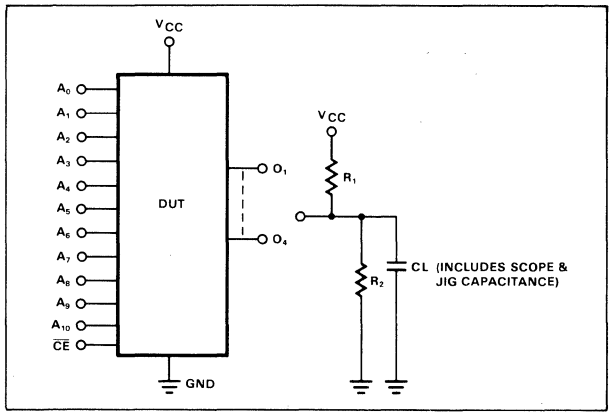
$R_1 = 270\Omega$, $R_2 = 600\Omega$, C_L = 30pF[3]
N82S184/185: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S184/185: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S184/185			S82S184/185			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		70	100		70	125	
T_{CE}	Output	Chip enable		30	40		30	60	
Disable time									ns
T_{CD}	Output	Chip disable		30	40		30	60	

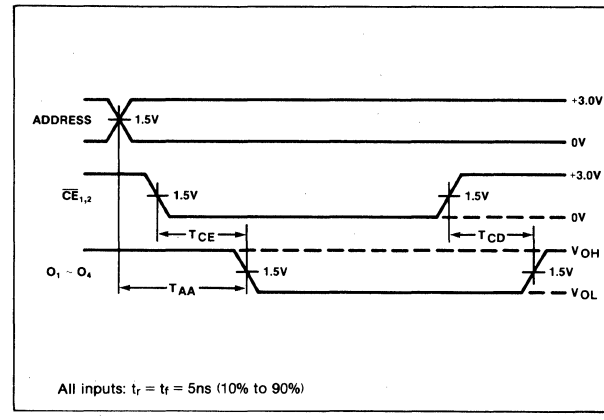
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Positive current is defined as into the terminal referenced.
4. Duration of the short circuit should not exceed 1 second.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



PROGRAMMING SYSTEMS SPECIFICATIONS

(Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 375 ± 75mA, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	300		450	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_p	CE programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	V_{CC} = V_{CCP}			12	sec
T_{PSI}	Initial programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

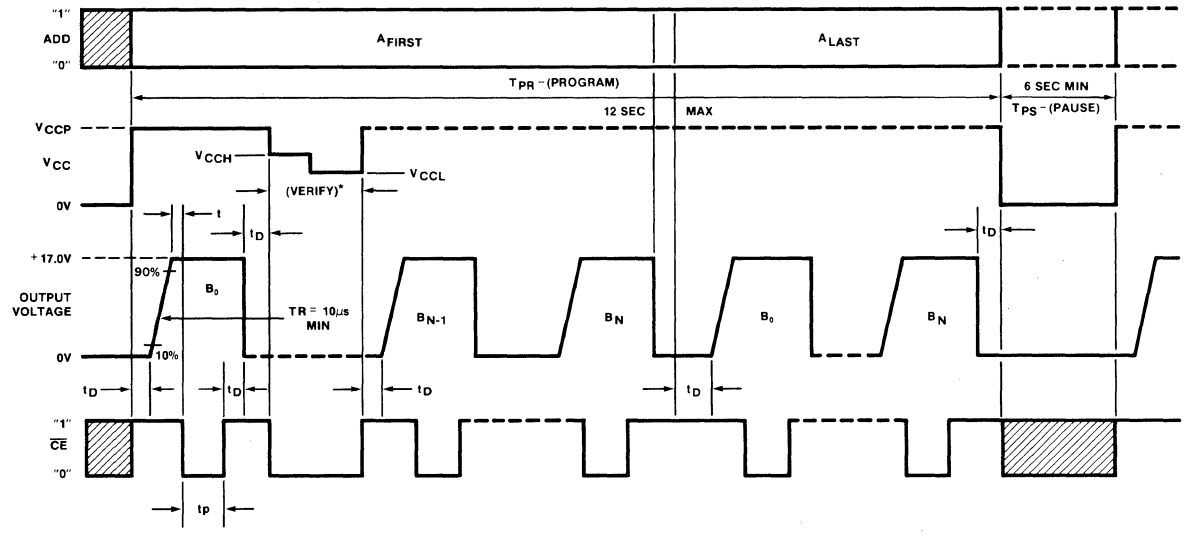
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}$ = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse the $\overline{CE}$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the $\overline{CE}$ input. The programmed output should remain in the high state. Again, low V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

DESCRIPTION

The 82S190 and 82S191 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S190 and 82S191 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 3 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S190 and 82S191 devices are available in the commercial and military ranges. For the commercial temperature range (0°C to +75°C) specify N82S190/191, I, and for the military temperature range (-55°C to +125°C) specify S82S190/191, I.

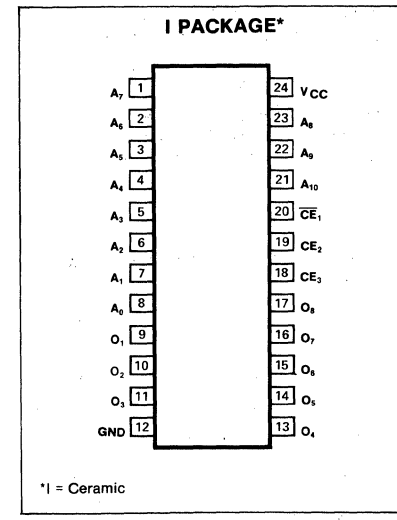
FEATURES

- **Address access time:**
  N82S190/191: 80ns max
  S82S190/: 100ns max
- **Power dissipation : 40μW/bit typ**
- **Input loading:**
  N82S190/191: -100μA max
  S82S190/191: -150μA max
- **3 chip enable inputs**
- **On-chip address decoding**
- **Output options:**
  82S190: Open collector
  82S191: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

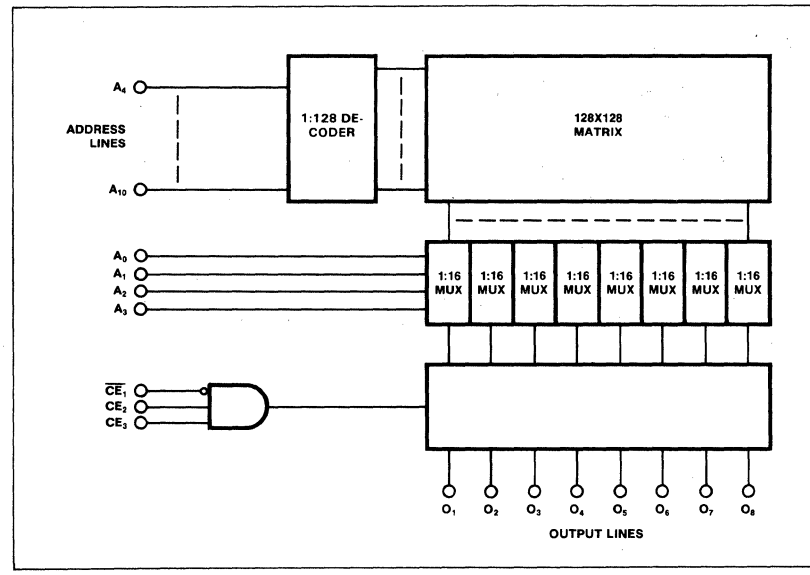
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



*I = Ceramic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S140)	+5.5	
V_O	Off-state (82S141)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S190/191	0 to +75	
	S82S190/191	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S190/191: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S190/191: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1]	N82S190/191			S82S190/191			UNIT
			Min	Typ2	Max	Min	Typ2	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage								V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High (82S191)	I_{OUT} = -2mA, $\overline{CE_1}$ = Low, CE_2 = High, CE_3 = High, High stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S190)	V_{OUT} = 5.5V, $\overline{CE_1}$ = High, CE_2 = Low, $\overline{CE_3}$ = Low			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S191)	V_{OUT} = 0.5V, $\overline{CE_1}$ = High, CE_2 = Low, $\overline{CE_3}$ = Low			-40			-60	μA
		V_{OUT} = 5.5V, $\overline{CE_1}$ = High, CE_2 = Low, CE_3 = Low			40			60	
I_{OS}	Short circuit (82S191)	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175		130	185	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

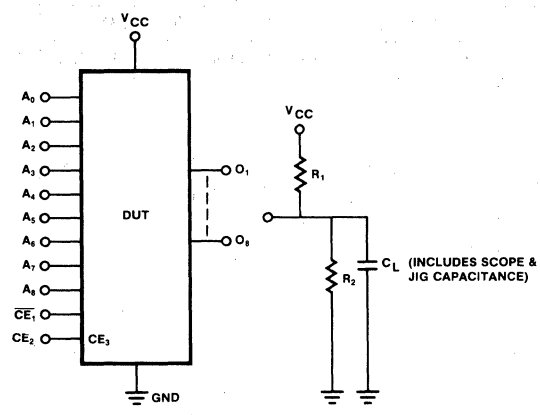
R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S190/191: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S190/191: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S190/191			S82S190/191			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
Access time									ns
T_{AA}	Output	Address		50	80		50	100	
T_{CE}	Output	Chip enable		20	40		20	50	
Disable time									ns
T_{CD}	Output	Chip disable		20	40		20	50	

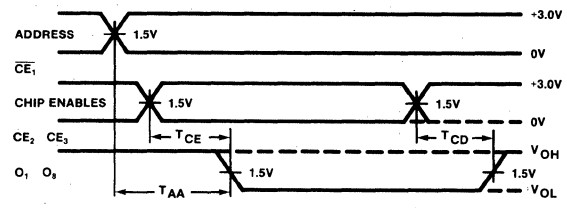
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

PROGRAMMING SYSTEMS SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCP}	Power supply voltage To program[1]	I_{CCP} = 375 ± 75mA, Transient or steady state	8.5	8.75	9.0	V
	Verify limit					V
V_{CCH}	Upper		5.3	5.5	5.7	
V_{CCL}	Lower		4.3	4.5	4.7	
V_S	Verify threshold[2]		1.4	1.5	1.6	V
I_{CCP}	Programming supply current	V_{CCP} = +8.75 ± .25V	300		450	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = +0.4V			-500	
V_{OUT}	Output programming voltage[3]	I_{OUT} = 200 ± 20mA, Transient or steady state	16.0	17.0	18.0	V
I_{OUT}	Output programming current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output pulse rise time		10		50	μs
t_P	CE programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PSI}	Initial programming pause	V_{CC} = 0V	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle[4]				50	%
F_L	Fusing attempts per link				2	cycle

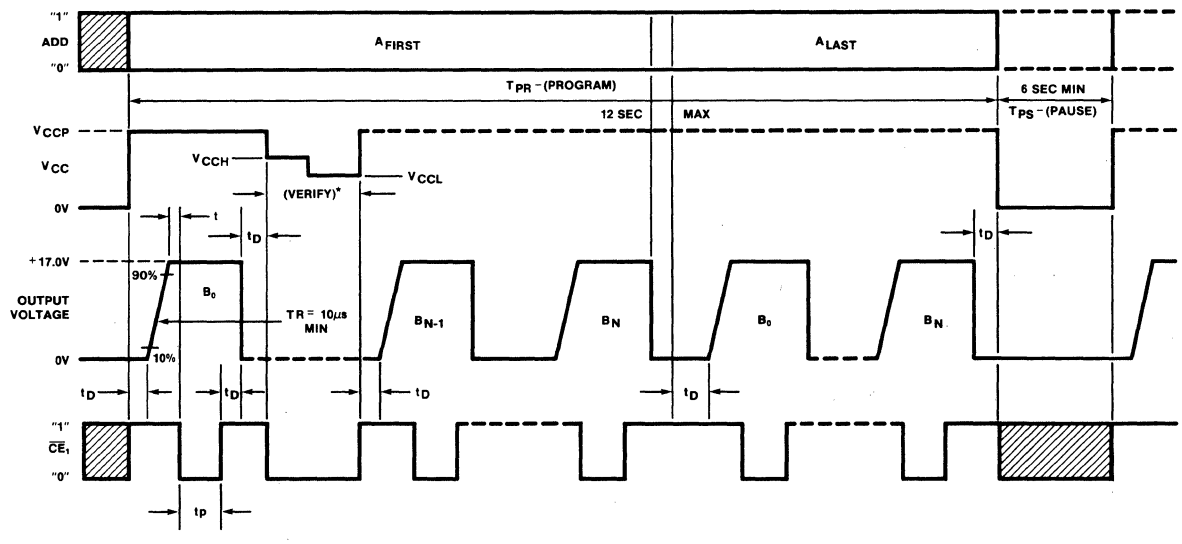
NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle.
4. Programming duty cycle is 50% after continuous programming at 100% duty cycle.
5. This is an updated method of programming and does not obsolete any programming systems presently being used.

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = High, CE_2 = High and CE_3 = High.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Progam one output at the time.
4. After 10μs delay, pulse the $\overline{CE}_1$ input to logic low for 0.3 to 0.5ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic low level to the $\overline{CE}_1$ input. The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

TYPICAL PROGRAMMING SEQUENCE



*Programming verification at both high and low V_{CC} margins is optional. For convenience, verification can also be executed at the operating V_{CC} limits specified in the dc characteristics.

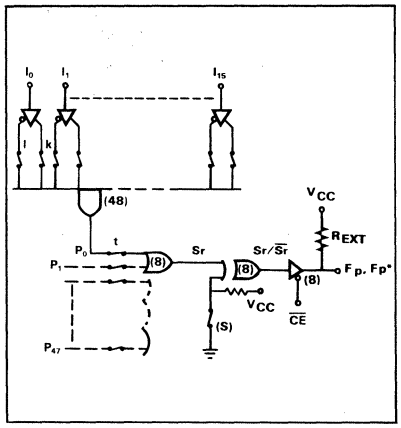
DESCRIPTION

The 82S100 (tri-state outputs) and the 82S101 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-high (Fp), or true active-low ($F\dot{p}$). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are field programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S100/101,I or N, and for the military temperature range (-55°C to +125°C) specify S82S100/101,I.

FPLA EQUIVALENT LOGIC PATH



LOGIC FUNCTION

Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions:
$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2)$ @ S = Closed
$F_0^* = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ S = Open

NOTE

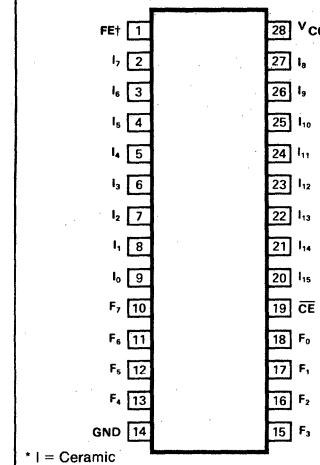
For each of the 8 outputs, either the function Fp (active-high) or $F\dot{p}$ (active low) is available, but not both. The required function polarity is programmed via link (S).

APPLICATIONS

- **CRT display systems**
- **Random logic**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Sequential controllers**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**

PIN CONFIGURATION

I,N PACKAGE*



* I = Ceramic
N = Plastic
†Open during normal operation

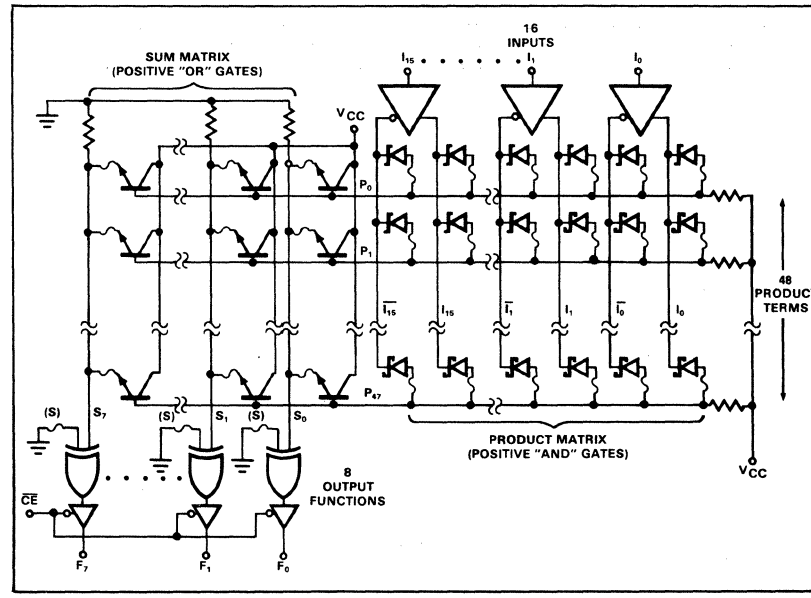
TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	$F\dot{p}$
Disabled (82S101)	X	1	X	1	1
Disabled (82S100)				Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S100/101	0	+75	
	S82S100/101	-55	+125	
T_{STG}	Storage	-65	+150	

DC ELECTRICAL CHARACTERISTICS

N82S100/101: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S100/101 Min	N82S100/101 Typ	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ	S82S100/101 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-12	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S100)[3,6]	I_{OL} = 9.6mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OH} = -2mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S100)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S100)[4,8]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V		8			8		pF
C_{IN}	Input	V_{IN} = 2.0V		17			17		
C_{OUT}	Output	V_{OUT} = 2.0V							

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S100/101: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

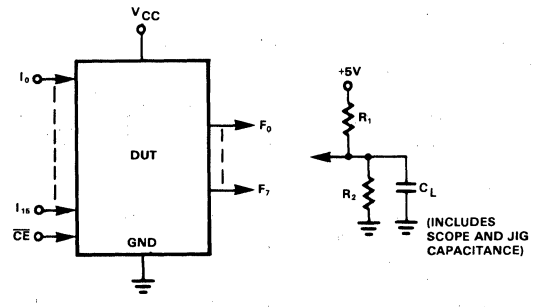
PARAMETER		TO	FROM	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Access time									ns
T_{IA}	Input	Output	Input		35	50		35	80	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	40	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	40	

NOTES on following page.

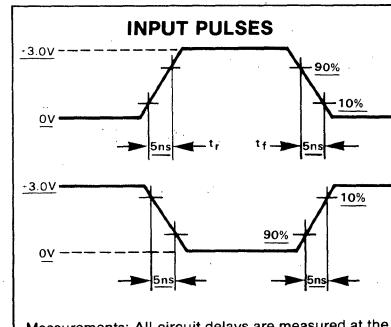
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied thru a resistor to V_{CC}.
7. Measured with: V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

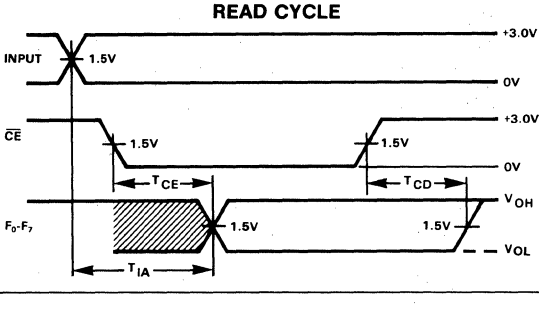


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAM



TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).

T_{IA} Delay between beginning of valid Input (with Chip Enable low) and when Data Output becomes valid.

VIRGIN DEVICE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "false").
3. The "OR" Matrix contains all 48-P-terms.
4. The polarity of each output is set to active high (Fp function).
5. All outputs are at a low logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the "AND" matrix, "OR" matrix, and output polarity outlined below. To maximize recovery from programming errors, leave all links in unused device areas intact.

SET-UP

Terminate all device outputs with a 10K resistor to +5V. Set GND (pin 14) to 0V.

Output Polarity

PROGRAM ACTIVE LOW ($\overline{F_P}$ FUNCTION)

Program output polarity before programming "AND" matrix and "OR" matrix. Program 1 output at the time. (S) links of unused outputs are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Set V_{CC} (pin 28) to V_{CCL}.
3. Set $\overline{CE}$ (pin 19), and I_0 through I_{15} to V_{IH}.
4. Apply V_{OPH} to the appropriate output, and remove after a period t_p.
5. Repeat step 4 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCS}.
2. Enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Address a non-existent P-term by applying V_{IH} to all inputs I_0 through I_{15}.
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a high logic level are programmed active low (F_p function), while all outputs at a low logic level are programmed active high (F_p function).
5. Return V_{CC} to V_{CCP} or V_{CCL}.

"AND" Matrix

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set FE (pin 1) to V_{FEL}, and V_{CC} (pin 28) to V_{CCP}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels V_{OHF} and V_{OLF}.

5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.

5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step 6.

5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step 6.

6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.

6c. After t_D delay, return FE input to V_{FEL}.

7. Disable programmed input by returning I_0 to V_{IX}.
8. Repeat steps 5 through 7 for all other input variables.
9. Repeat steps 4 through 8 for all other P-terms.
10. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

1. Set FE (pin 1) to V_{FEL}; set V_{CC} (pin 28) to V_{CCP}.
2. Enable F_7 output by setting $\overline{CE}$ to V_{IX}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.
4. Address the P-term to be verified (No. 0 through 47) by forcing the corresponding binary code on outputs F_0 through F_5.
5. Interrogate input variable I_0 as follows:
   A. Lower the input voltage at I_0 from V_{IX} to V_{IH}, and sense the logic state of output F_7.
   B. Lower the input voltage at I_0 from V_{IH} to V_{IL}, and sense the logic state output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	INPUT VARIABLE STATE CONTAINED IN P-TERM
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Don't Care
0 1	0 0	(I_0), $(\overline{I_0})$

Note that 2 tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Disable verified input by returning I_0 to V_{IX}.
7. Repeat steps 5 and 6 for all other input variables.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{IX} from all input variables.

"OR" MATRIX

PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links in the "OR" matrix corresponding to unused outputs and unused P-terms are not required to be fused.

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_6 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB.

5a. If the P-term is contained in output function F_0 ($F_0 = 1$ or $F_0^* = 0$), got to step 6, (fusing cycle not required).

5b. If the P-term is **not** contained in output function F_0 ($F_0 = 0$ or $F_0^* = 1$), set to fuse the P_n link by forcing output F_0 to V_{OPF}.

6a. After t_D delay, raise FE (pin 1) from V_{FEL} to V_{FEH}.

6b. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.

6c. After t_D delay, return FE input to V_{FEL}.

6d. After t_D delay, remove V_{OPF} from output F_0.

7. Repeat steps 5 and 6 for all other output functions.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove V_{CCS} from V_{CC}.

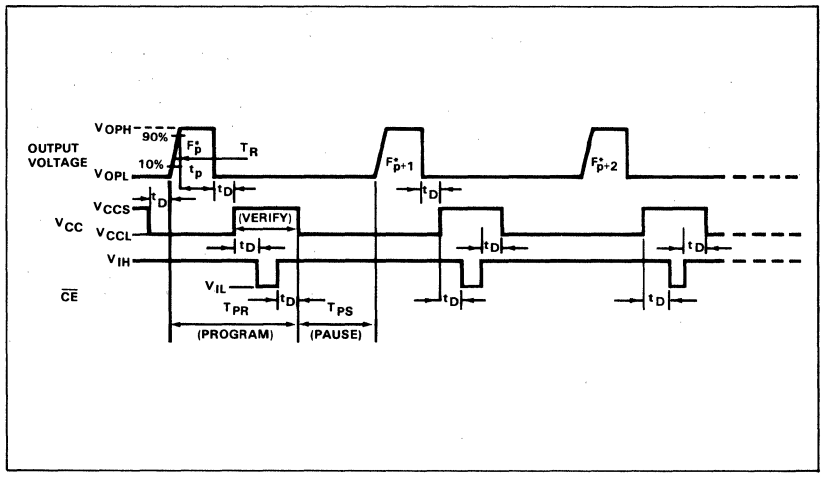
VERIFY PRODUCT TERM

1. Set FE (pin 1) to V_{FEL}.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. After t_D delay, set V_{CC} (pin 28) to V_{CCS}, and inputs I_0 through I_{15} to V_{IH}, V_{IL}, or V_{IX}.
4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5.
5. After t_D delay, enable the chip by setting $\overline{CE}$ (pin 19) to V_{IL}.
6. To determine the status of the P_n link in the "OR" matrix for each output function F_p or F_p^*, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

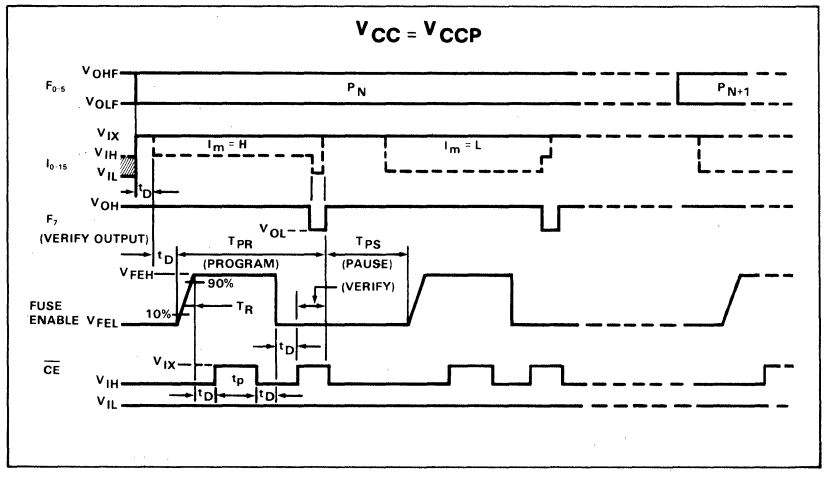
OUTPUT		P-TERM LINK
Active High (F_p)	Active Low (F_p^*)	
0 1	1 0	**Fused** **Present**

7. Repeat steps 4 through 6 for all other P-terms.
8. Remove V_{CCS} from V_{CC}.

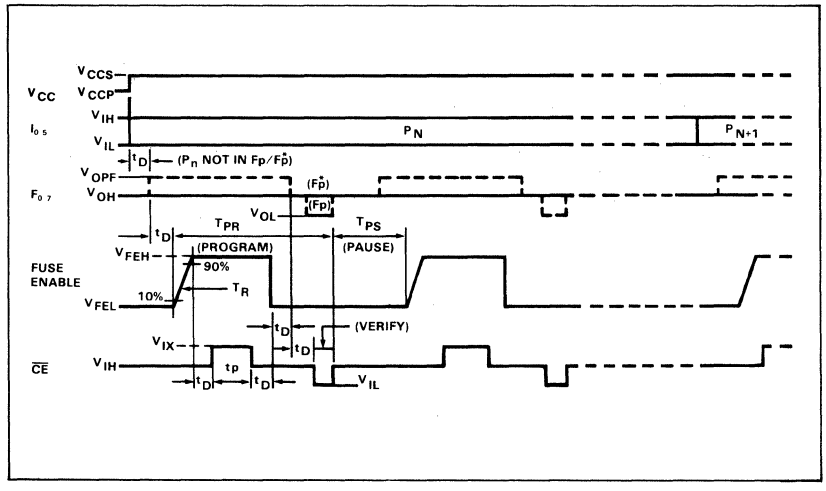
OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



"AND" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



"OR" MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



PROGRAMMING SYSTEM SPECIFICATIONS[1] (T_A = +25°C)

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CCS}	V_{CC} supply (program/verify "OR", verify output polarity)[2]	I_{CCS} = 550mA, min, Transient or steady state	8.5	8.75	9.0	V
V_{CCL}	V_{CC} supply (program output polarity)		0	0.4	0.8	V
I_{CCS}	I_{CC} limit (program "OR")	V_{CCS} = +8.75 ± .25V	550		1,000	mA
	Output voltage					V
V_{OPH}	Program output polarity[3]	I_{OPH} = 300 ± 25mA	16.0	17.0	18.0	
V_{OPL}	Idle		0	0.4	0.8	
I_{OPH}	Output current limit (Program output polarity)	V_{OPH} = +17 ± 1V	275	300	325	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					µA
I_{IH}	High	V_{IH} = +5.5V			50	
I_{IL}	Low	V_{IL} = 0V			-500	
	Forced output voltage					V
V_{OHF}	High		2.4		5.5	
V_{OLF}	Low		0	0.4	0.8	
	Output current					
I_{OHF}	High	V_{OHF} = +5.5V			100	µA
I_{OLF}	Low	V_{OLF} = 0V			-1	mA
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	V_{IX} = +10V			2.5	mA
I_{IX2}	$\overline{CE}$ input current	V_{IX} = +10V			5.0	mA
V_{FEH}	FE supply (program)[3]	I_{FEH} = 300 ± 25mA, Transient or steady state	16.0	17.0	18.0	V
V_{FEL}	FE supply (idle)	I_{FEL} = -1mA, max	1.25	1.5	1.75	V
I_{FEH}	FE supply current limit	V_{FEH} = +17 ± 1V	275	300	325	mA
V_{CCP}	V_{CC} supply (program/verify "AND")	I_{CCP} = 550mA, min, Transient or steady state	4.75	5.0	5.25	V
I_{CCP}	I_{CC} limit (program "AND")	V_{CCP} = +5.0 ± .25V	550		1,000	mA
V_{OPF}	Forced output (program)		9.5	10	10.5	V
I_{OPF}	Output current (program)				10	mA
T_R	Output pulse rise time		10		50	µs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms[5]
t_D	Pulse sequence delay		10			µs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle				50	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

1. These are specifications which a Programming System must satisy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01µf capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of the FPLA output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
5. These are new limits resulting from device improvements, and which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment.

82S100-I,N • 82S101-I,N

16X48X8 FPLA PROGRAM TABLE

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) ______

CUSTOMER SYMBOLIZED PART # ______

DATE RECEIVED ______

COMMENTS ______

CUSTOMER NAME ______

PURCHASE ORDER # ______

SIGNETICS DEVICE # ______

TOTAL NUMBER OF PARTS ______

PROGRAM TABLE # ______

REV ______ DATE ______

PROGRAM TABLE ENTRIES						
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	$\overline{Im}$	Don't Care	Prod. Term Present in Fp	Prod. Term Not Present in Fp	Active High	Active Low
H	L	— (dash)	A	• (period)	H	L
NOTE Enter (—) for unused inputs of used P-terms.			NOTES 1. Entries independent of output polarity. 2. Enter (A) for unused outputs of used P-terms.		NOTES 1. Polarity programmed once only. 2. Enter (H) for all unused outputs.	

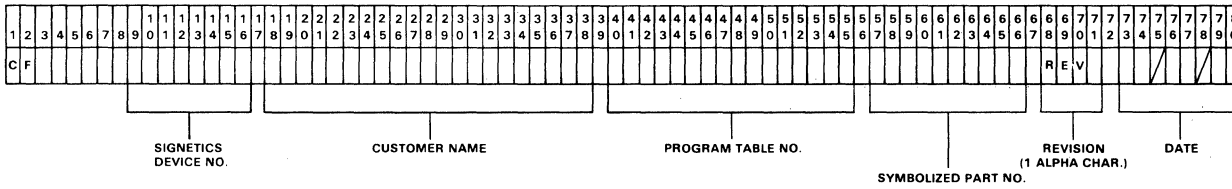
	PRODUCT TERM* / INPUT VARIABLE*																ACTIVE LEVEL* / OUTPUT FUNCTION*							
NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																								
1																								
2																								
3																								
4																								
5																								
6																								
7																								
8																								
9																								
10																								
11																								
12																								
13																								
14																								
15																								
16																								
17																								
18																								
19																								
20																								
21																								
22																								
23																								
24																								
25																								
26																								
27																								
28																								
29																								
30																								
31																								
32																								
33																								
34																								
35																								
36																								
37																								
38																								
39																								
40																								
41																								
42																								
43																								
44																								
45																								
46																								
47																								

* Input and Output fields of unused P-terms can be left blank. Unused inputs and outputs are FPLA terminals left floating.

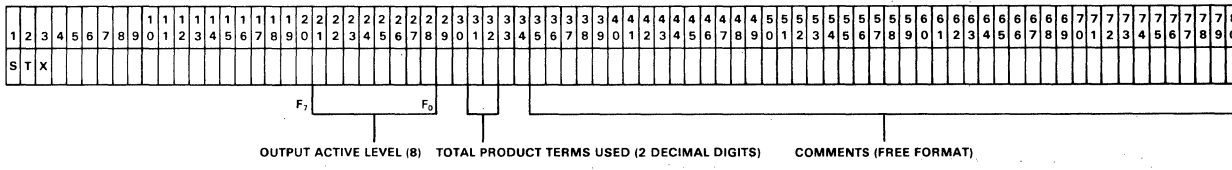
PUNCHED CARD CODING FORMAT

The FPLA Program Table can be supplied directly to Signetics in punched card form, using standard 80-column IBM cards. For each FPLA Program Table, the customer should prepare in input card deck in accordance with the following format. Product Term cards 3 through 50 can be in any order. Not all 48 Product Terms need to be present. Unused Product Terms require no entry cards, and will be skipped during the actual programming sequence:

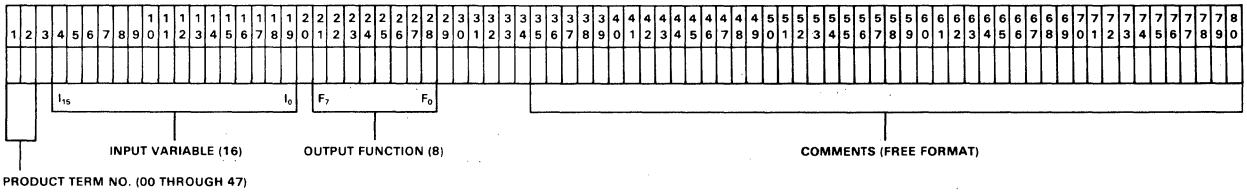
CARD NO.1—Free format within designated fields.



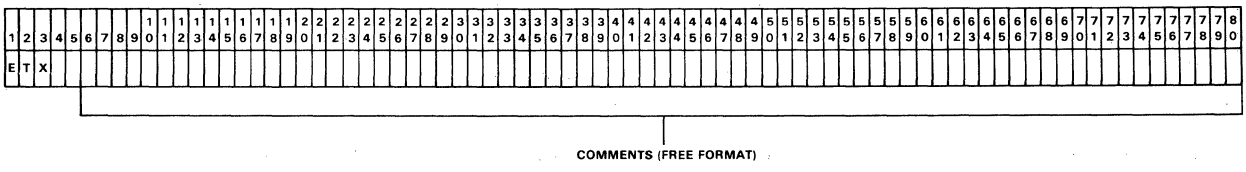
CARD NO. 2—



CARD NO. 3 through NO. 50



CARD NO. 51



Output Active Level entries are determined in accordance with the following table:

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES
1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

Input Variable entries are determined in accordance with the following table:

INPUT VARIABLE		
Im H	$\overline{\text{Im}}$ L	Don't care — (dash)

NOTE
Enter (—) for unused inputs of used P-terms.

Output Function entries are determined in accordance with the following table:

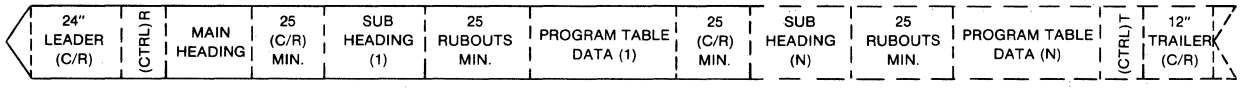
OUTPUT FUNCTION	
Product term present in FP A	Product term *not* present in FP • (period)

NOTES
1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

TWX TAPE CODING FORMAT

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



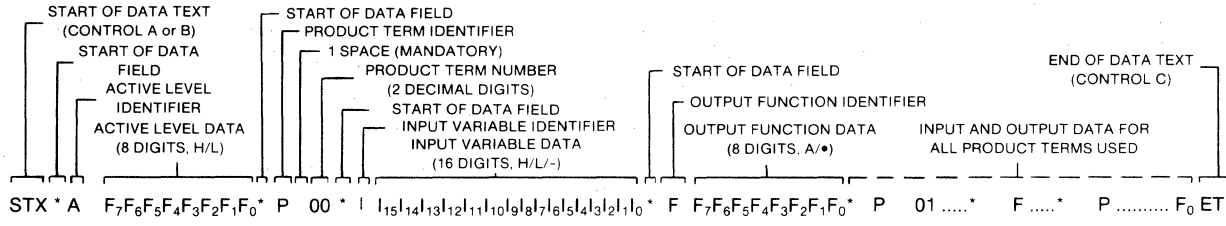
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following format:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE		
I_m H	$\overline{I_m}$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

OUTPUT FUNCTION	
Product term present in Fp A	Product term not present in Fp • (period)

NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

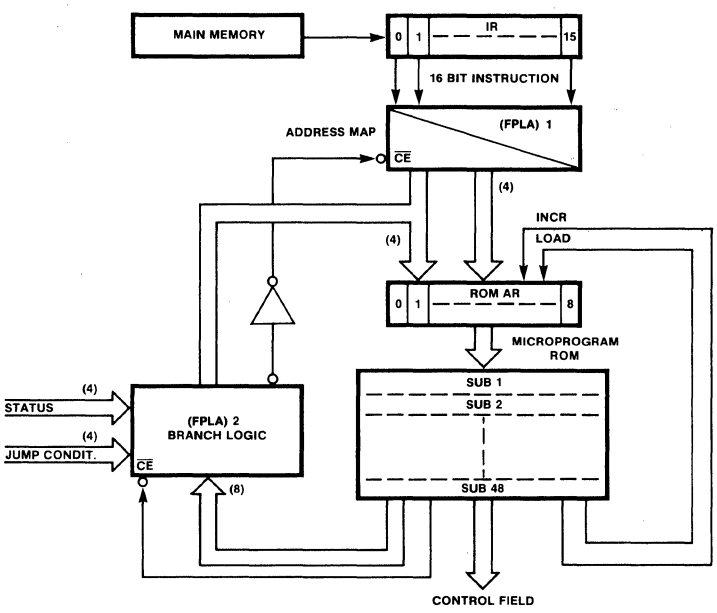
Although the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

NOTES

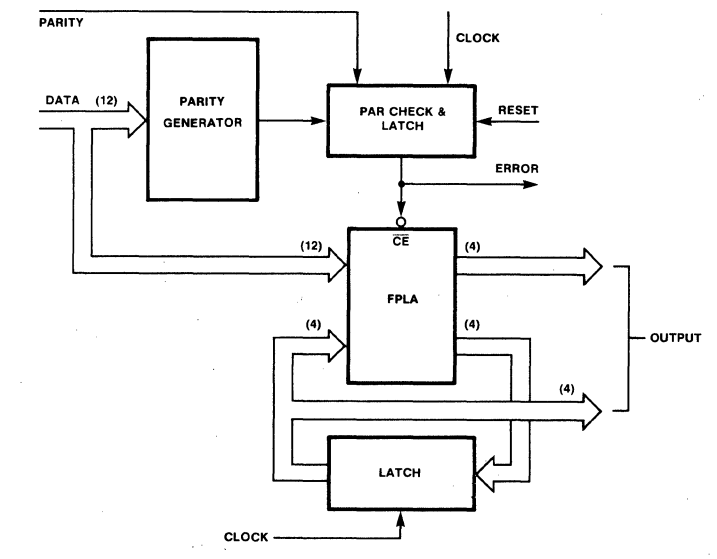
1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. P-Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. Any P-Term can be deleted entirely by inserting the character (E) immediately following the P-Term number to be deleted, i.e., *P 25E deletes P-Term 25.
4. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups, but only preceding an asterisk (*).
5. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

TYPICAL APPLICATIONS

SUBROUTINE ADDRESS MAP



SEQUENTIAL CONTROLLER



DESCRIPTION

The 82S200 (tri-state outputs) and the 82S201 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR tems). Each OR term controls an output function which can be programmed either true active-high (F_P), or true active-low (F_P*). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are mask programmable by supplying to Signetics Program Table data in one of the formats specified in this data sheet.

The 82S200 and 82S201 are fully TTL compatible, and include chip enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

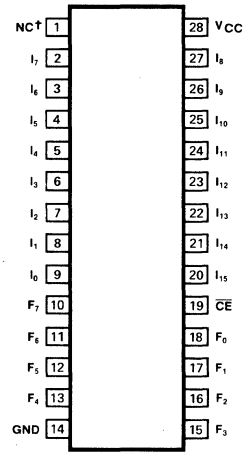
Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S200/201, I or N, and for the military temperature range (-55°C to +125°C) specify S82S200/201, I.

APPLICATIONS

- **CRT display systems**
- **Random logic**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Sequential controllers**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**

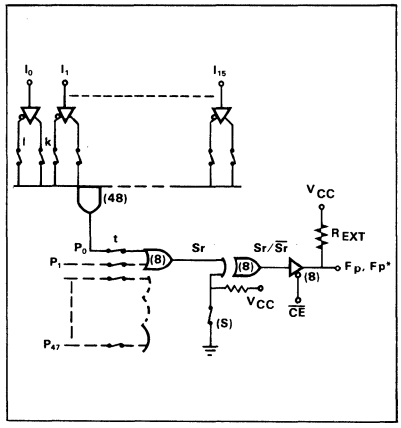
PIN CONFIGURATION

I,N PACKAGE*



*I = Ceramic
N = Plastic
†Open during normal operation

PLA EQUIVALENT LOGIC PATH



LOGIC FUNCTION

Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions:
$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2)$ @ S = Closed
$F_0^* = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ S = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or $F\dot{p}$ (active low) is available, but not both. The required function polarity is programmed via link (S).

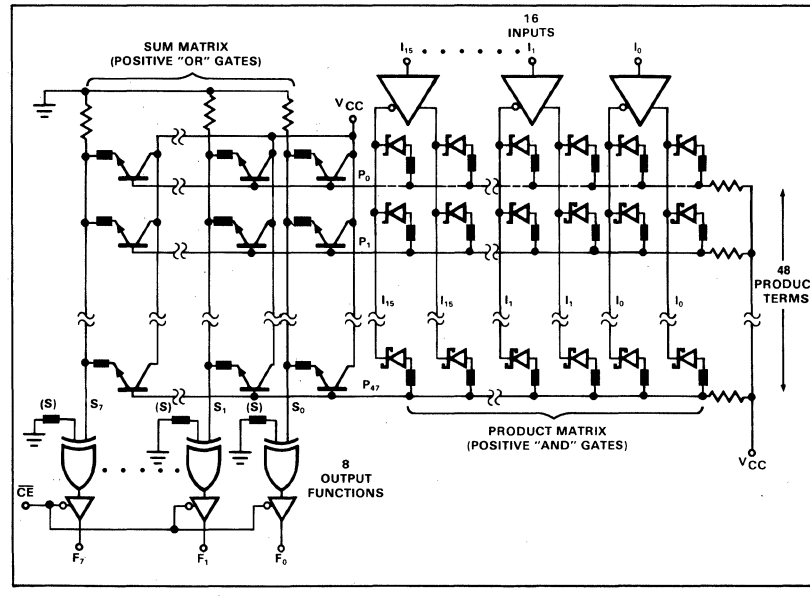
TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	$F\dot{p}$
Disabled (82S201)	X	1	X	1	1
Disabled (82S200)				Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING		UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S200/201	0	+75	
	S82S200/201	-55	+125	
T_{STG}	Storage	-65	+150	

DC ELECTRICAL CHARACTERISTICS

N82S200/201: $0° \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S200/201: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	N82S200/201			S82S200/201			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} 7 -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S200)[3,5]	I_{OH} = -2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S200)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S200)[4,8]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

N82S200/201: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

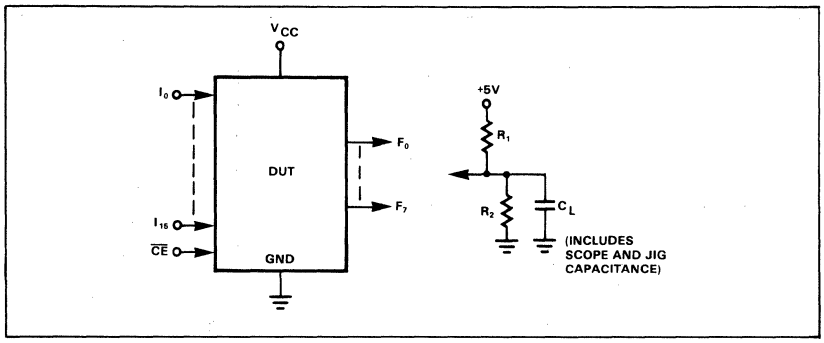
S82S200/201: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S200/201			S82S200/201			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{IA}	Input	Output	Input		35	50		35	80	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	50	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	50	

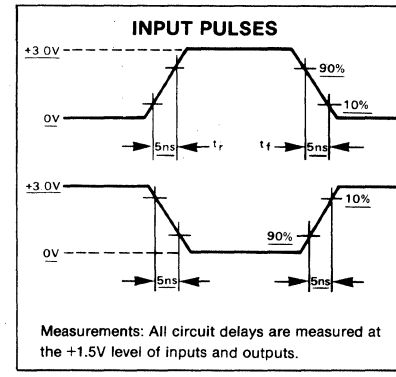
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied thru a resistor to V_{CC}.
7. Measured with: V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

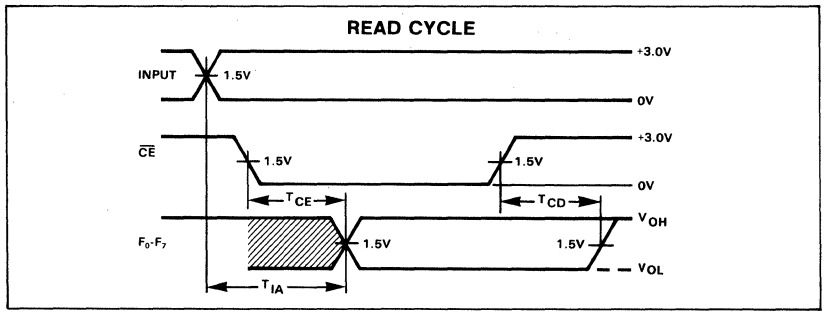


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAM



TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).

T_{IA} Delay between beginning of valid Input (with Chip Enable low) and when Data Output becomes valid.

16X48X8 PLA PROGRAM TABLE

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____

REV _____ DATE _____

PROGRAM TABLE ENTRIES						
INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
Im	$\overline{Im}$	Don't Care	Prod. Term Present in F_P	Prod. Term Not Present in F_P	Active High	Active Low
H	L	— (dash)	A	• (period)	H	L
NOTE: Enter (—) for unused inputs of used P-terms.			NOTES: 1. Entries independent of output polarity. 2. Enter (A) for unused outputs of used P-terms.		NOTES: 1. Polarity programmed once only. 2. Enter (H) for all unused outputs.	

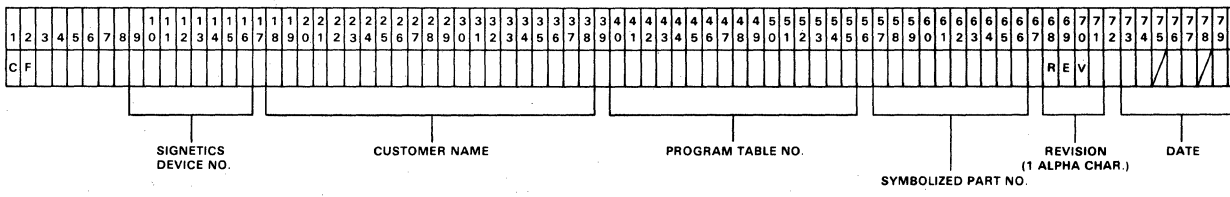
NO.	PRODUCT TERM* INPUT VARIABLE*																ACTIVE LEVEL* OUTPUT FUNCTION*							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																								
1																								
2																								
3																								
4																								
5																								
6																								
7																								
8																								
9																								
10																								
11																								
12																								
13																								
14																								
15																								
16																								
17																								
18																								
19																								
20																								
21																								
22																								
23																								
24																								
25																								
26																								
27																								
28																								
29																								
30																								
31																								
32																								
33																								
34																								
35																								
36																								
37																								
38																								
39																								
40																								
41																								
42																								
43																								
44																								
45																								
46																								
47																								

*Input and Output fields of unused P-terms can be left blank. Unused inputs and outputs are PLA terminals left floating.

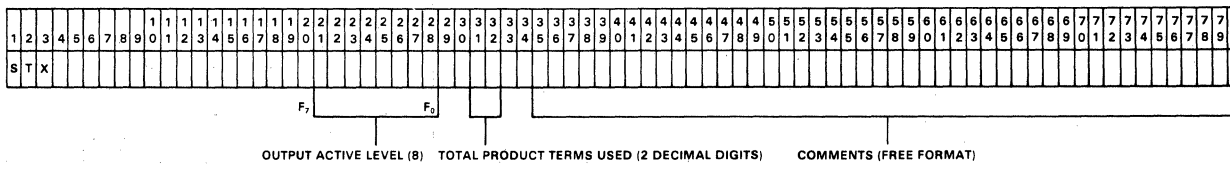
PUNCHED CARD CODING FORMAT

The PLA Program Table can be supplied directly to Signetics in punched card form, using standard 80-column IBM cards. For each PLA Program Table, the customer should prepare an input card deck in accordance with the following format. Product Term cards 3 through 50 can be in any order. Not all 48 Product Terms need to be present. Unused Product Terms require no entry cards, and will be skipped during the actual programming sequence:

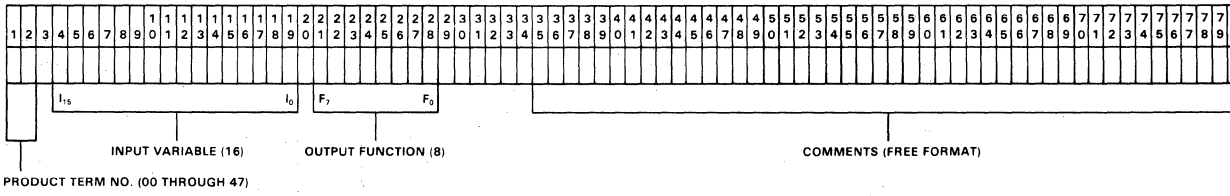
CARD NO.1—Free format within designated fields.



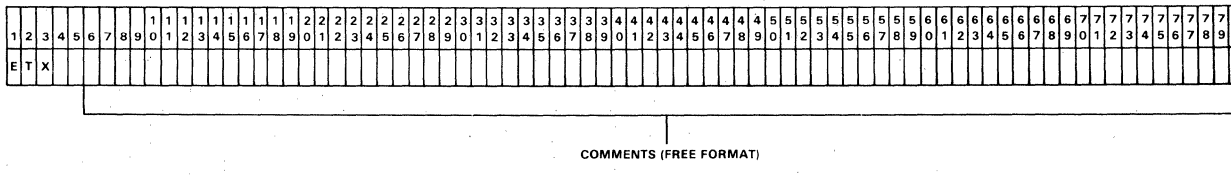
CARD NO. 2—



CARD NO. 3 through NO. 50



CARD NO. 51



Output Active Level entries are determined in accordance with the following table:

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

Input Variable entries are determined in accordance with the following table:

INPUT VARIABLE		
Im H	$\overline{Im}$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

Output Function entries are determined in accordance with the following table:

OUTPUT FUNCTION	
Product term present in Fp A	Product term not present in Fp • (period)

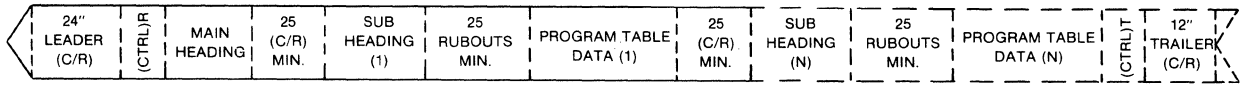
NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

TWX TAPE CODING FORMAT

The PLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter:



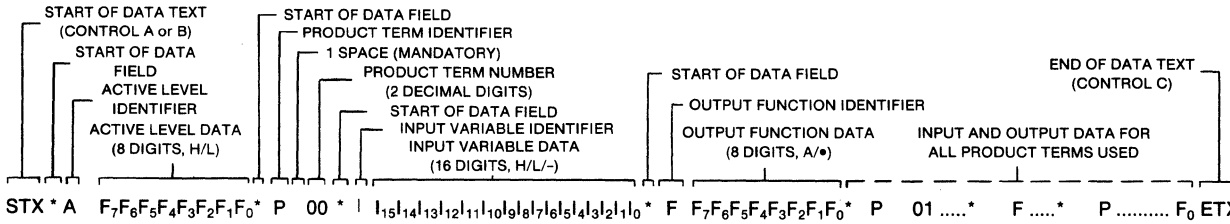
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. Customer Name _____
2. Customer TWX No. _____
3. Date _____
4. Purchase Order No. _____
5. Number of Program Tables _____
6. Total Number of Parts _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. Signetics Device No. _____
2. Program Table No. _____
3. Revision _____
4. Date _____
5. Customer Symbolized Part No. _____
6. Number of Parts _____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information separated by appropriate identifiers in accordance with the following format:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE		
I_m H	$\overline{I}_m$ L	Don't care — (dash)

NOTE

Enter (—) for unused inputs of used P-terms.

OUTPUT FUNCTION	
Product term present in Fp A	Product term not present in Fp • (period)

NOTES

1. Entries independent of output polarity.
2. Enter (A) for unused outputs of used P-terms.

OUTPUT ACTIVE LEVEL	
Active high H	**Active low** L

NOTES

1. Polarity programmed once only.
2. Enter (H) for all unused outputs.

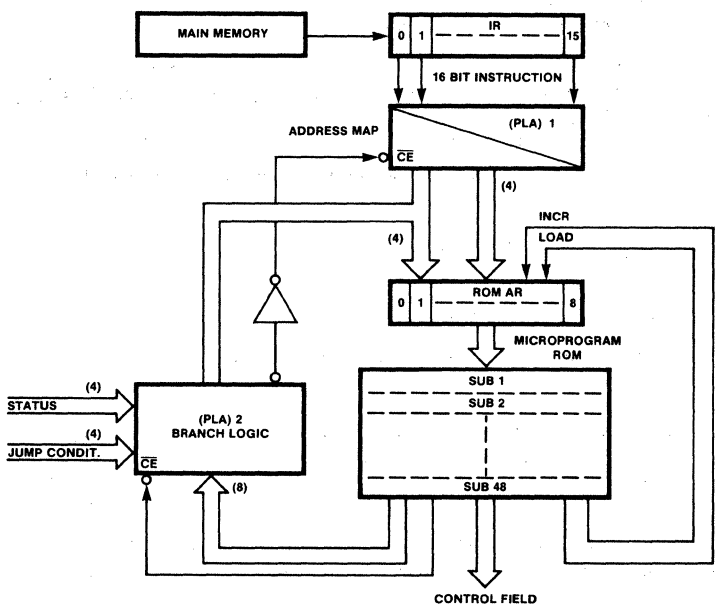
Although the Product Term data are shown entered in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

NOTES

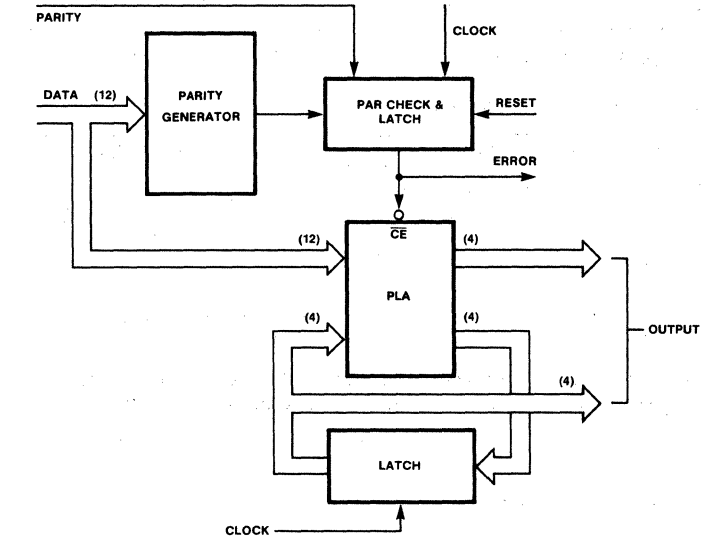
1. Corrections to any entry can be made by backspace and rubout. However, limit consecutive rubouts to less than 25.
2. P-Terms can be re-entered any number of times. The last entry for a particular P-Term will be interpreted as valid data.
3. Any P-Term can be deleted entirely by inserting the character (E) immediately following the P-Term number to be deleted, i.e., *P 25E deletes P-Term 25.
4. To facilitate an orderly Teletype print out, carriage returns, line feeds, spaces, rubouts etc. may be interspersed between data groups, but only preceding an asterisk (*).
5. Comments are allowed between data fields, provided that an asterisk (*) is not used in any Heading or Comment entry.

TYPICAL APPLICATIONS

SUBROUTINE ADDRESS MAP



SEQUENTIAL CONTROLLER



DESCRIPTION

The 82S102 and 82S103 are Bipolar programmable AND/NAND gate arrays, containing 9 gates sharing 16 common inputs. On-chip input buffers enable the user to individually program for each gate either the True (I_m), Complement ($\overline{I_m}$), or Don't Care (X) logic state of each input. In addition, the polarity of each gate output is individually programmable to implement either AND or NAND logic functions.

Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its input variables, and output (DeMorgan theorem).

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S102 and 82S103 include chip-enable control for output strobing and inhibit. They feature either open collector or tri-state outputs for ease of expansion of input variables and application in bus-organized systems.

Both devices are available in the commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S102/103, I or N, and for the military range (−55°C to +125°C) specify S82S102/103, I.

FEATURES

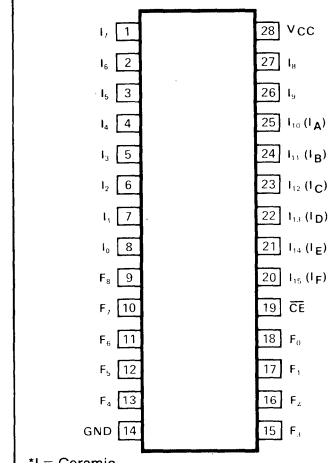
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay:**
  N82S102/103: 30ns max
  S82S102/103: 50ns max
- **Power dissipation: 600mW typ**
- **Input loading:**
  N82S102/103: −100μA max
  S82S102/103: −150μA max
- **Output options:**
  82S102: Open collector
  82S103: Tri-state
- **Output disable function:**
  82S102: Hi
  82S103: Hi-Z
- **Fully TTL compatible**

APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

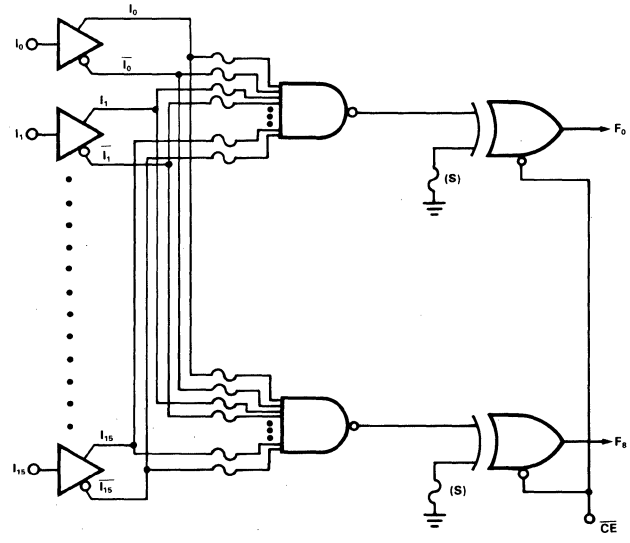
PIN CONFIGURATION

I,N PACKAGE*



*I = Ceramic
N = Plastic

LOGIC DIAGRAM

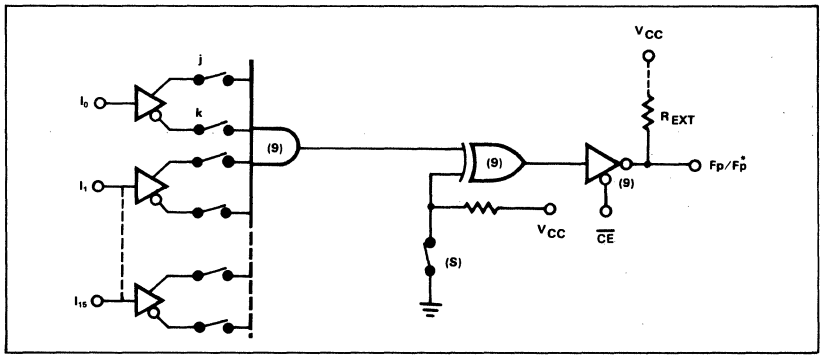


For each of the 9 outputs, either the function Fp (active high) or Fp (active low) is available, but not both. The required function polarity is user programmable via fuse (S).

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S102)	+5.5	
V_O	Off-state (82S103)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating		
	N82S102/103	0 to +75	
	S82S102/103	-55 to +125	
T_{STG}	Storage	-65 to +150	

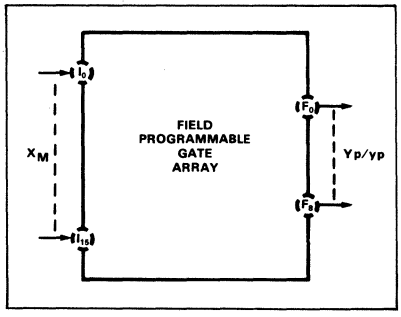
EQUIVALENT LOGIC PATH



The Field Programmable Gate Array consists of 9 gates with individually programmable inputs and outputs.

The inputs to each gate can be programmed either True (I_m), Complement ($\overline{I_m}$), or Don't Care via corresponding links (j) and (k). The outputs of each gate can be programmed active-high (F_p) or active-low (F_p^*) via corresponding links (S). Thus, each gate provides either of 2 output logic functions in terms of *external* input logic variables X_m as defined below (positive logic):

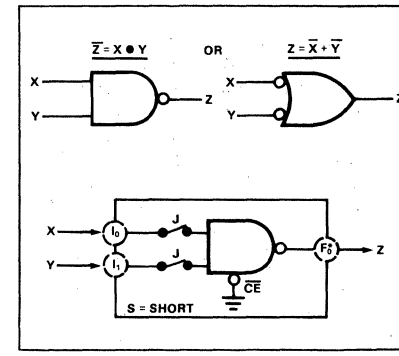
At S = Open:
$F_p = \overline{CE} + (X_0 \bullet X_1 \bullet X_2 \bullet \ldots . Xm) = Yp$
At S = Closed:
$F_p^* = \overline{CE} + (\overline{X}_0 + \overline{X}_1 + \overline{X}_2 + \ldots . X_m) = yp$
m = 0, 1, 2, ... 15
p = 0, 1, 2, ... 8
and where $X_m = I_m, \overline{I_m}$, Don't Care, as assigned by programming polarity of inputs I_0- I_{15}.

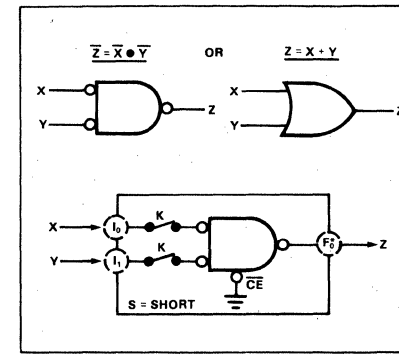


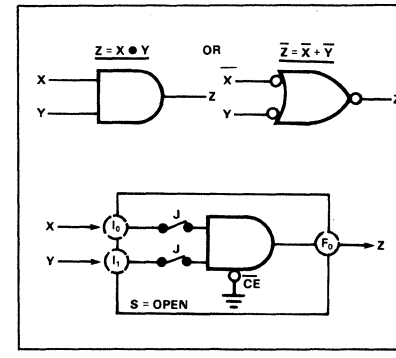
When $\overline{CE}$ = low, all gates are enabled, and $F_p^* = \overline{F}_p$ giving $y_p = \overline{Y}_p$.

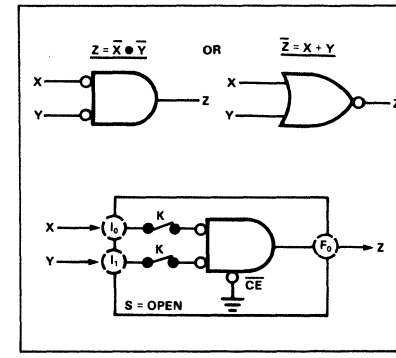
PROGRAMMABLE LOGIC FUNCTIONS

All internal links of virgin FPGAs are intact. Therefore, as shown in the Equivalent Logic Path, all symbolic switches are initially closed. Selective programming (opening) of links (J), (K), and (S) enables the user to assign input and output polarities to each gate for implementing NAND, NOR, AND, OR logic functions without changing the routing of input and output wires. This is shown in the following diagrams for a typical gate in terms of 2 input variables, which can be readily extended up to 16.









DC ELECTRICAL CHARACTERISTICS

N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[1]		TEST CONDITIONS	N82S102/103			S82S102/103			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S103)[1,5]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S102)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S103)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S103)[3,7]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170		120	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15			15		

AC ELECTRICAL CHARACTERISTICS

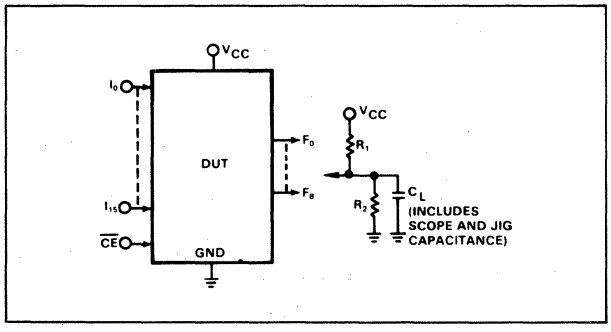
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S102/103			S82S103/103			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{IA}	Input	Output	Input		20	30		20	50	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	40	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	40	

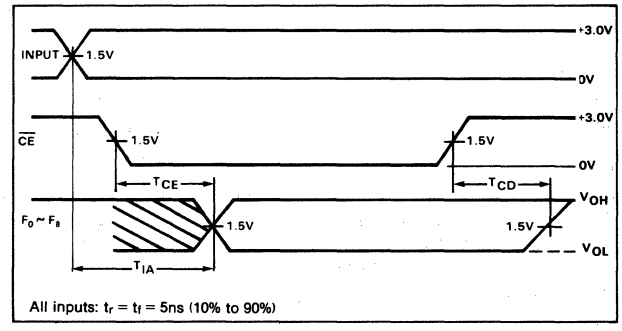
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test each output one at a time.
4. Measured with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

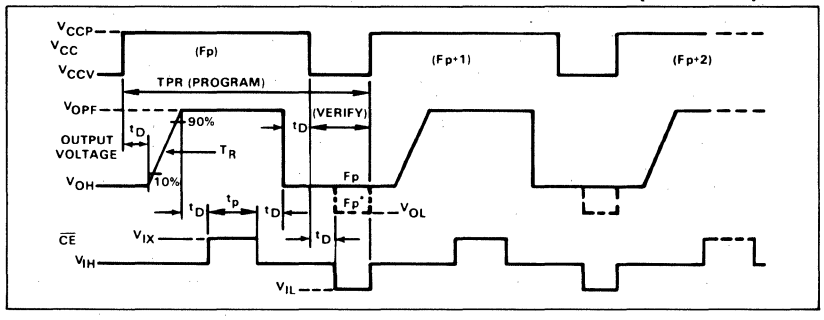
TEST LOAD CIRCUIT



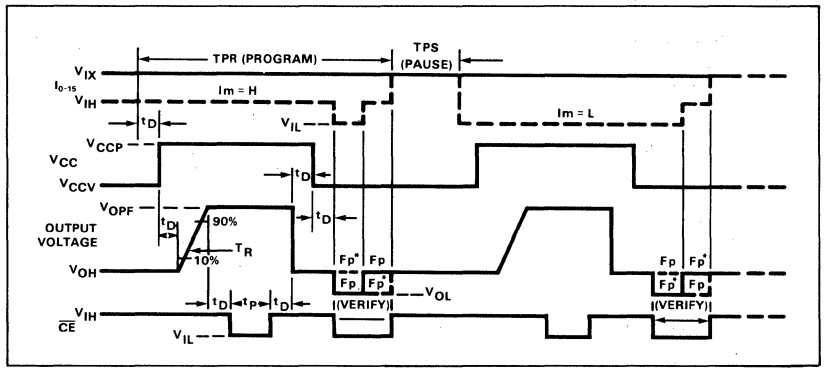
VOLTAGE WAVEFORM



OUTPUT POLARITY PROGRAM-VERIFY SEQUENCE (TYPICAL)



INPUT MATRIX PROGRAM-VERIFY SEQUENCE (TYPICAL)



VIRGIN DEVICE

The 82S102/103 are shipped in an unprogrammed state, characterized by:

1. All internal Ni-Cr links are intact.
2. Each gate contains both true and complement values of every input variable I_m (logic Null state).
3. The polarity of each output is set to active low (F_p^* function).
4. All outputs are at a high logic level.

RECOMMENDED PROGRAMMING PROCEDURE

To program each of 9 Boolean logic functions of 16 True, Complement, or Don't Care input variables follow the program/verify procedures for the Input Matrix and Output Polarity outlined below. To maximize recovery from programming errors, leave all links of unused gates intact.

SET-UP

Terminate all device outputs with a 10KΩ resistor to +5V.

Output Polarity

PROGRAM ACTIVE HIGH (Fp FUNCTION)

Program output polarity before programming inputs (for convenience). Program one output at a time. (S) links of unused outputs are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Raise V_{CC} (pin 28) from V_{CCV} to V_{CCP}.
B. After t_D delay, force output to be programmed to V_{OPF}.
C. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IX} for a period t_p.
D. After t_D delay, remove V_{OPF} voltage source from output being programmed.
E. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
F. Repeat steps A through E for any other output.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. After t_D delay, set the $\overline{CE}$ input to V_{IL}.
B. Verify output polarity by sensing the logic state of outputs F_0 through F_8. All outputs at a low logic level are programmed active low (F_p^* function), while all outputs at a high logic level are programmed active high (F_p function).

Input Matrix

PROGRAM INPUT VARIABLE

Program one input at a time for one gate at a time. Input variable links of unused gates are not required to be fused. However, unused input variables must be programmed at Don't Care for all used gates.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Disable all device outputs by setting $\overline{CE}$ (pin 19) to V_{IH}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A-1. If a gate contains nether I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both j and k links by executing both steps A-2 and A-3, before continuing with step C.
A-2. If a gate contains I_0, set to fuse the k link by lowering the input voltage at I_0 from V_{IX} to V_{IH}. Execute step B.
A-3. If a gate contains $\overline{I_0}$, set to fuse the j link by lowering the input voltage at I_0 from V_{IX} to V_{IL}. Execute step B.
B-1. After t_D delay, raise V_{CC} from V_{CCV} to V_{CCP}.
B-2. After t_D delay, force output of gate to be programmed to V_{OPF}.
B-3. After t_D delay, pulse the $\overline{CE}$ input from V_{IH} to V_{IL} for a period t_p.
B-4. After t_D delay, remove V_{OPF} voltage source from output of gate being programmed.
B-5. After t_D delay, return V_{CC} (pin 28) to V_{CCV}, and verify.
C. Disable programmed input by returning I_0 to V_{IX}.
D. Repeat steps A through C for all other input variables.
E. Repeat steps A through D for all other gates to be programmed.
F. Remove V_{IX} from all input variables.

VERIFY INPUT VARIABLE

Unambiguous verification of the logic state programmed for the inputs of each gate requires prior knowledge of its programmed output polarity. Therefore, the output polarity verify procedure must precede input variable verify.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to V_{CCV}.
2. Enable all outputs by setting $\overline{CE}$ (pin 19) to V_{IL}.
3. Disable all input variables by applying V_{IX} to inputs I_0 through I_{15}.

A. Interrogate input variable I_0 as follows:
Lower the input voltage to I_0 from V_{IX} to V_{IL}, and sense the logic state of outputs F_{0-8}.

Raise the input voltage to I_0 from V_{IL} to V_{IH} and sense the logic state of outputs F_{0-8}.

The state of I_0 contained in each gate is determined in accordance with the given truth table. Note that 2 tests are required to uniquely determine the state of the input variable contained in each gate.

B. Disable verified input by returning I_0 to V_{IX}.

C. Repeat steps A and B for all other input variables.

D. Remove V_{IX} from all input variables.

TRUTH TABLE FOR INPUT VERIFICATION

I_0	Fp	$F\dot{p}$	INPUT VARIABLE STATE	LINK FUSED
0	1	0	$\overline{I_0}$	j
1	0	1		
0	0	1	I_0	k
1	1	0		
0	1	0	Don't care	Both
1	1	0		
0	0	1	(I_0), $(\overline{I_0})$	Neither
1	0	1		

PROGRAMMING SYSTEMS SPECIFICATIONS[1] $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	V_{CC} supply					V
V_{CCP}	Program[2]	$I_{CCP} = 350 \pm 50mA$, Transient or steady state	8.5	8.75	9.0	
V_{CCV}	Verify		4.75	5.0	5.25	
I_{CCP}	I_{CC} limit (program)	$V_{CCP} = +8.75 \pm .25V$, Transient or steady state	400	450	500	mA
V_{OPF}	Forced output voltage[3] (program)	$I_{OP} = 150 \pm 25mA$, Transient or steady state	16.0	17.0	18.0	V
I_{OPF}	Output current limit (program)	$V_{OP} = +17 \pm 1V$, Transient or steady state	125	150	175	mA
	Input voltage					V
V_{IH}	High		2.4		5.5	
V_{IL}	Low		0	0.4	0.8	
	Input current					μA
I_{IH}	High	$V_{IH} = +5.5V$			50	
I_{IL}	Low	$V_{IL} = 0V$			-500	
V_{IX}	$\overline{CE}$ program enable level		9.5	10	10.5	V
I_{IX1}	Input variables current	$V_{IX} = +10V$			5.0	mA
I_{IX2}	$\overline{CE}$ input current	$V_{IX} = +10V$			10.0	mA
T_R	Output pulse rise time		10		50	μs
t_P	$\overline{CE}$ programming pulse width		0.3	0.4	0.5	ms
t_D	Pulse sequence delay		10			μs
T_{PR}	Programming time			0.6		ms
$\frac{T_{PR}}{T_{PR}+T_{PS}}$	Programming duty cycle				100	%
F_L	Fusing attempts per link				2	cycle
V_S	Verify threshold[4]		1.4	1.5	1.6	V

NOTES

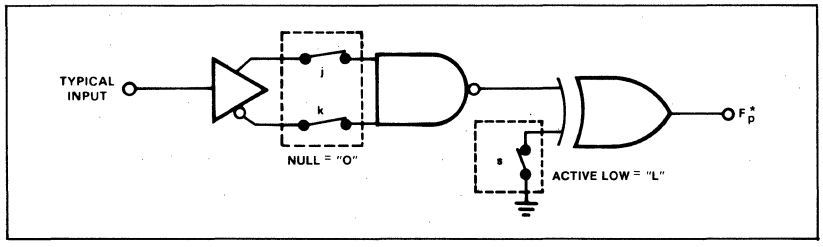
1. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
2. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
3. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
4. V_S is the sensing threshold of a gate output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

PROGRAMMING

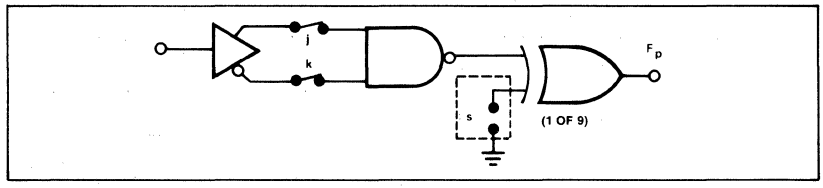
In a virgin device all Ni-Cr links are intact. The initial programmed state of each gate is shown in the Typical Gate illustration.

To program inputs and outputs of each gate for implementing the desired logic function, fuse Ni-Cr links as indicated in the fuse link diagrams.

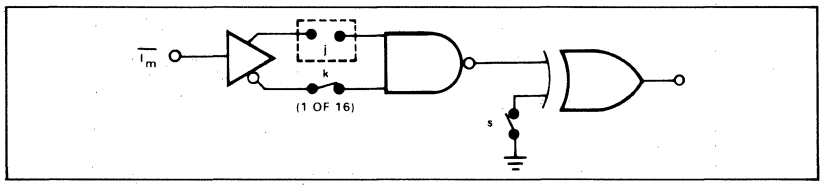
TYPICAL GATE



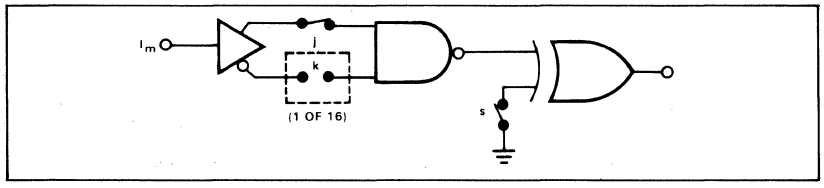
OUTPUT ACTIVE HIGH = FUSE LINK S



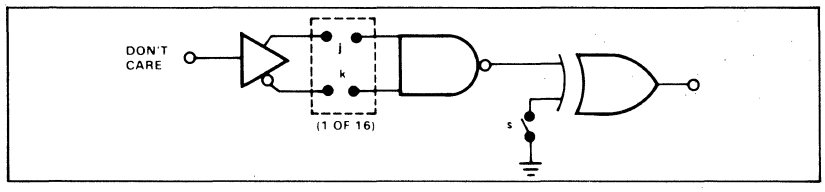
INPUT $\overline{I}m$ = FUSE LINK J



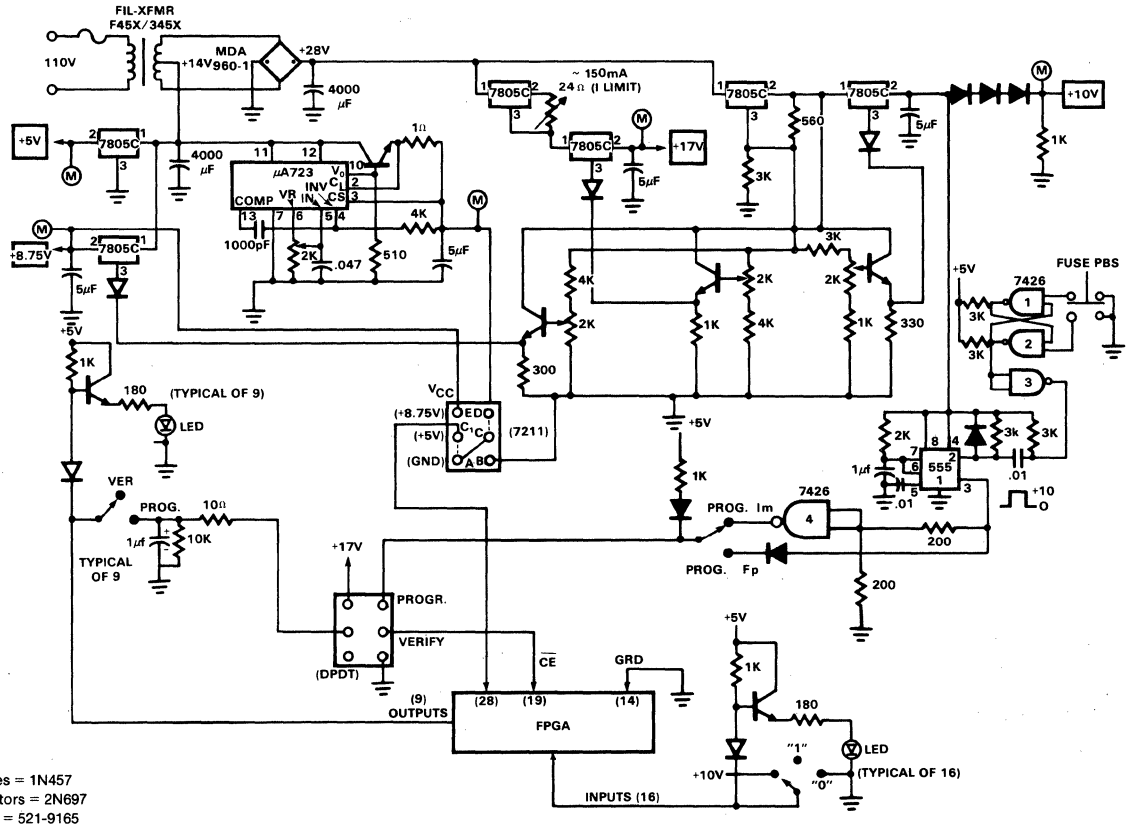
INPUT Im = FUSE LINK K



INPUT DON'T CARE = FUSE BOTH LINKS J, K



FPGA MANUAL FUSER



Diodes = 1N457
Resistors = 2N697
LEDs = 521-9165

16X9 FPGA PROGRAM TABLE

CUSTOMER NAME _____	*THIS PORTION TO BE COMPLETED BY SIGNETICS*
PURCHASE ORDER # _____	*CF (XXXX)* _____
SIGNETICS DEVICE # _____	*CUSTOMER SYMBOLIZED PART #* _____
TOTAL NUMBER OF PARTS _____	*DATE RECEIVED* _____
PROGRAM TABLE # _____	*COMMENTS* _____

F_0 = _____

F_1 = _____

F_2 = _____

F_3 = _____

F_4 = _____

F_5 = _____

F_6 = _____

F_7 = _____

F_8 = _____

OUTPUT POLARITY		INPUT VARIABLE															
		I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_A	I_B	I_C	I_D	I_E	I_F
F_0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
F_1	16	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
F_2	32	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
F_3	48	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
F_4	64	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
F_5	80	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
F_6	96	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
F_7	112	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
F_8	128	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
Active-high = H Active-low = L		I_m = H $\overline{I_m}$ = L Don't Care = —															

The number in each cell in the table denotes its address for programmers with a decimal address display.

MOS MEMORY DATA SPECIFICATIONS

2501-I,N

DESCRIPTION

The 2501 employs enhancement mode p-channel MOS devices integrated on a single monolithic chip.

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics unique silicon gate MOS process technology. Unlike the standard metal gate MOS process, the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide-substrate structure provides an ion barrier. In addition, Signetics' proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

The use of Signetics' unique silicon gate low threshold process allows the design and production of higher performance MOS circuits and provides higher functional density on a chip than other MOS technologies.

All inputs of the 2501 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA which is sufficient to drive one standard TTL load.

The maximum power dissipation of 1.6mW/bit is required only during read or write. For standby operation, 150μW/bit is obtained by removing V_D and reducing V_{DD} to -4.0V. Removal of V_D alone will cut power dissipation by a factor of 1.5.

The outputs of the 2501 are effectively open circuited when the device is not selected (logic high on chip select). This feature allows OR-tying for memory expansion.

FEATURES

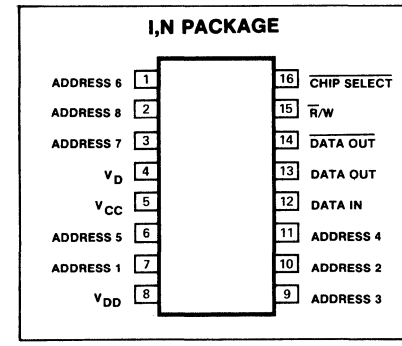
- **Fully decoded addresses**
- **Access time: 1.0μs guaranteed**
- **Power dissipation: 1.6mW/bit max**
- **Standby power dissipation: 150μW/bit**
- **DTL and TTL compatible**
- **Chip select and output wired-OR capability**
- **Standard 16-pin DIP**
- **P-MOS silicon gate technology**
- **Completely static**
- **Requires no clocking**

APPLICATIONS

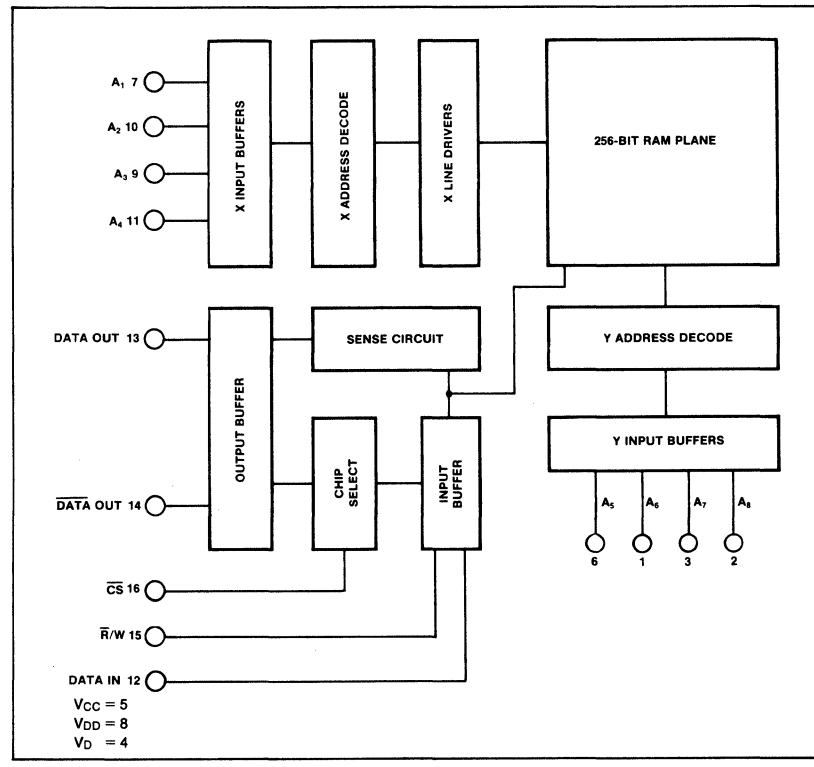
- **Small buffer stores**
- **Small core memory replacement**
- **Bipolar compatible data storage**

PIN CONFIGURATION

I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	-65 to +150	
P_D	Power dissipation		mW
	I package	800	
	N package	640	
	All input or output voltages with respect to the most positive supply voltage, V_{CC}	+0.3 to -20	V
	Supply voltages V_{DD} and V_D with respect to V_{CC}	-18	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V[2], V_{DD} = V_D = -9V ± 5% unless otherwise specified.[3,4,5,6,7,8,9]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low		-5.0		V_{CC}-4.5	
V_{IH}	High		V_{CC}-2.0		V_{CC}+0.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 3.0mA		-0.7	0.45	
V_{OH}	High	I_{OH} = -100μA	3.5	4.5		
	Input current	V_{IN} = 0V, T_A = +25°C				nA
I_{LI}	Load (All input pins)			<1.0	500	
	Output current					
I_{LO}	Leakage	V_{OUT} = 0V, Chip select input = 3.3V, T_A = 25°C		<1.0	1000	nA
	Sink					mA
I_{OL1}		V_{OUT} = 0.45V, T_A = +25°C	3.0	6		
I_{OL2}		V_{OUT} = 0.45V, T_A = +70°C	2.0	5		
I_{OL3}		V_{OUT} = -0.7V		6	13	
	Source	V_{OUT} = 0V				mA
I_{OH1}		T_A = +25°C	-3.0	4		
I_{OH2}		T_A = +70°C	-2.0	3		
	Supply current	T_A = +25°C, V_{DD} = V_D = -9V				mA
I_{DD}	V_{DD}			13.0	18	
I_D	V_D	I_{OL} = 0mA		8.5	12	
	Capacitance	f = 1MHz				pF
C_{IN}	Input (All pins)	V_{IN} = 5V		7	10	
C_{OUT}	Output	V_{OUT} = 5V		7	10	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V[2], V_{DD} = V_D = -9V ± 5%, Input pulse amplitudes = 0 to 5V, Input pulse rise and fall times = <10ns, Speed measurements referenced to 1.5V levels, Output load = 1 TTL gate, Measurements made at output of TTL gate (t_{pd} ≤ 10ns), unless otherwise specified.

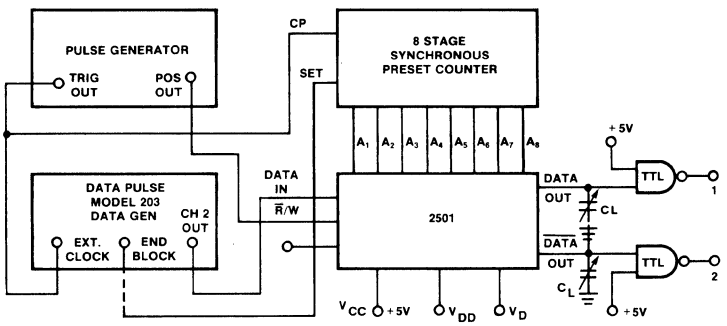
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
READ CYCLE							
t_A	Access time	Output	Address			1000	ns
WRITE CYCLE							
t_W	Write time	Write	Address	300			ns
t_{WD}	Delay time			300			ns
t_{WP}	Write pulse width			400			ns
t_{DO}	Data-write pulse overlap			100			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5V.
3. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient for the I package or 150°C/W for the N package.
4. All inputs are protected against static charge.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.
9. Special device are available for operation at V_{DD} = -7V, V_D = -10V. Contact your Signetics Representative for details.

TEST LOAD CIRCUIT

SPEED MEASUREMENT

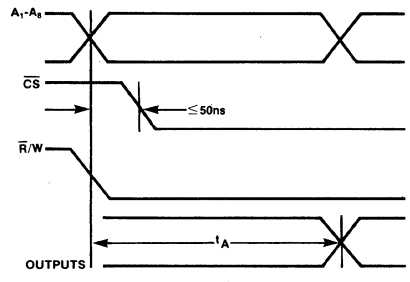


NOTES

A. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the delay and width controls of the pulse generator.
B. Data generator produces a 256-bit block of data, 32 bits repeated 8 times. PCM mode used so data can be changed in 32 bits of the 2501 from one cycle to the next.
C. All inputs to the 2501 are standard TTL outputs with V_{CC} = 5V ± 5%.
D. Access time is measured between A1 (least significant address input) and points 1 and 2.

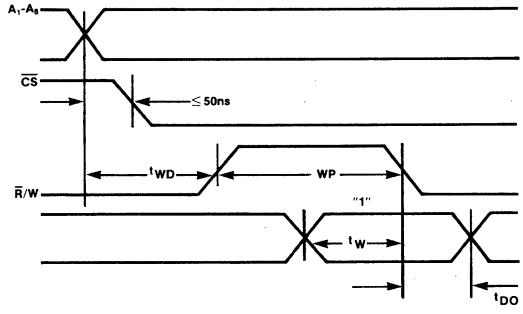
VOLTAGE WAVEFORMS

READ CYCLE



For Measurement Purpose Only

WRITE CYCLE



For Measurement Purpose Only

25L01-I,N

DESCRIPTION

The 25L01 employs enhancement mode p-channel MOS devices integrated on a single monolithic chip.

Low cost silicone DIP packaging is implemented and reliability is assured by the use of Signetics' unique silicon gate MOS process technology. Unlike the standard metal gate MOS process the silicon material over the gate oxide passivates the MOS transistors, and the deposited dielectric material over the silicon gate-oxide substrate structure provides an ion barrier. In addition, Signetics' proprietary surface passivation and silicone packaging techniques result in an MOS circuit with inherent high reliability and demonstrating superior moisture resistance, mechanical shock and ionic contamination barriers.

All inputs of the 25L01 can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA, sufficient to drive one standard TTL load.

The maximum power dissipation of 1.7mW/bit is required only during read or write. For standby operation 100μW/bit is obtained by removing V_D and reducing V_{DD} to -8.0V. Removal of V_D alone wll cut power dissipation by a factor of almost 3.

The outputs of the 25L01 are effectively open circuited when the device is not selected (logic high on chip select). This feature allows OR-tying for memory expansion.

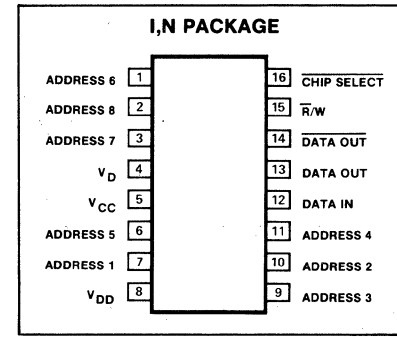
FEATURES

- **Fully decoded addresses**
- **Access time: 1.0μs guaranteed**
- **Power dissipation: 1.7mW/bit max**
- **Standby power dissipation: 100μW/bit**
- **DTL and TTL compatible**
- **Chip select and output wired-OR capability**
- **Standard 16-pin DIP**
- **P-MOS silicon gate technology**
- **Fully static**
- **Requires no clocking**
- **Optimized with +5 and -12V supplies**

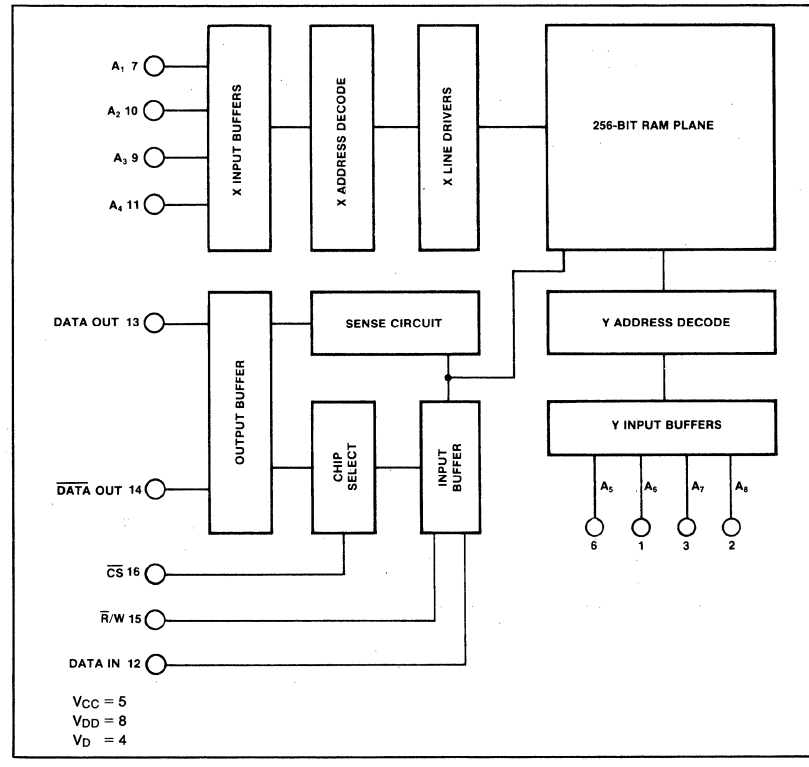
APPLICATIONS

- **Small buffer stores**
- **Small core memory replacement**
- **Bipolar compatible data storage**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	-65 to +150	
P_D	Power dissipation		mW
	I package	800	
	N package	640	
	All input or output voltages with respect to the most positive supply voltage, V_{CC}	+0.3 to -20	V
	Supply voltages V_{DD} and V_D with respect to V_{CC}	-18	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{DD} = V_D = -12V ± 5% unless otherwise specified.[2,3,4,5,6,7]

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage					V
V_{IL}	Low		-12		V_{CC}-4.5	
V_{IH}	High		V_{CC}-2.0		V_{CC}+0.3	
	Output voltage					V
V_{OL}	Low	I_{OL} 3.0mA		-0.7	0.45	
V_{OH}	High	I_{OH} = -100μA	3.5	4.5		
	Input current	V_{IN} = 0V, T_A = +25°C				nA
I_{LI}	Load (All input pins)			<1.0	500	
	Output current					
I_{LO}	Leakage	V_{OUT} = 0V, Chip select input = 3.3V, T_A = 25°C		<1.0	1000	nA
	Sink					
I_{OL1}		V_{OUT} = 0.45V, T_A = +25°C	3.0	6		
I_{OL2}		V_{OUT} = 0.45V, T_A = +70°C	2.0	5		
I_{OL3}		V_{OUT} = -0.7V		6	13	
	Source	V_{OUT} = 0V				mA
I_{OH1}		T_A = +25°C	-3.0	4		
I_{OH2}		T_A = +70°C	-2.0	3		
	Supply current	T_A = +25°C				mA
I_{DD}	V_{DD}			5	9	
I_D	V_D	I_{OL} = 0mA		11	16	
	Capacitance	f = 1MHz				pF
C_{IN}	Input (All pins)	V_{IH} = 5V		7	10	
C_{OUT}	Output	V_{OUT} = 5V		7	10	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, V_{DD} = V_D = -12V ± 5%, Input pulse amplitudes = 0 to 5V, Input pulse rise and fall times = <10ns, Speed measurements referenced to 1.5V levels, Output load = 1 TTL gate, Measurements made at output of TTL gate (t_{pd} ≤ 10ns), unless otherwise specified.

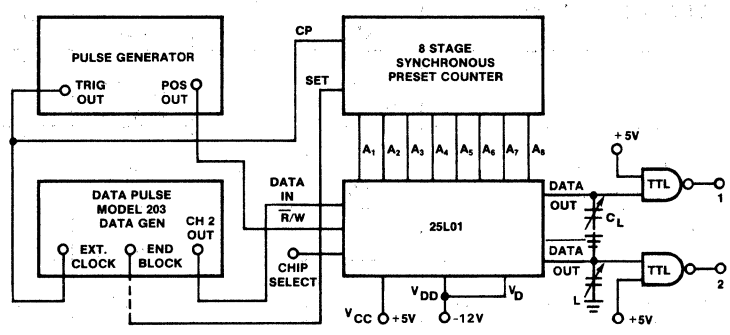
	PARAMETER	TO	FROM	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
READ CYCLE							
t_A	Access time	Output	Address			1000	ns
WRITE CYCLE							
t_W	Write time	Write	Address	300			ns
t_{WD}	Delay time			300			ns
t_{WP}	Write pulse width			400			ns
t_{DO}	Data-write pulse overlap			100			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient for the I package or 150°C/W for the N package.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.

TEST LOAD CIRCUIT

SPEED MEASUREMENT

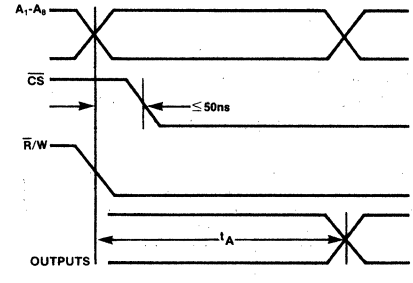


NOTES

A. Each clock time is split into a Read followed by a Write. Read and Write times can be varied by adjustment of the delay and width controls of the pulse generator.
B. Data generator produces a 256-bit block of data, 32 bits repeated 8 times. PCM mode used so data can be changed in 32 bits of the 2501 from one cycle to the next.
C. All inputs to the 25L01 are standard TTL outputs with V_{CC} = 5V ± 5%.
D. Access time is measured between A1 (least significant address input) and points 1 and 2.

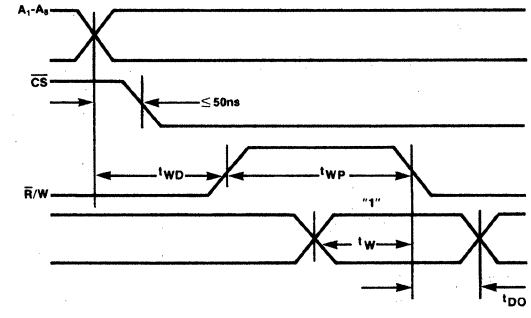
VOLTAGE WAVEFORMS

READ CYCLE



For Measurement Purpose Only

WRITE CYCLE



For Measurement Purpose Only

2101-F,N • 2101-1-F,N • 2101-2-F,N

DESCRIPTION

The 2101 series is high performance, low power static read/write RAM's.

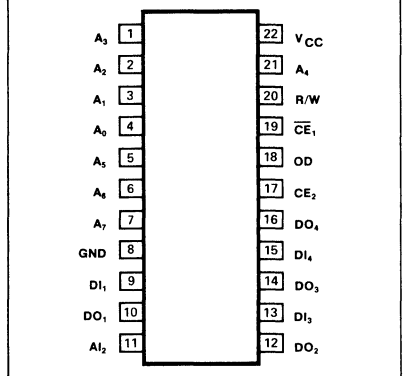
The 2101 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

FEATURES

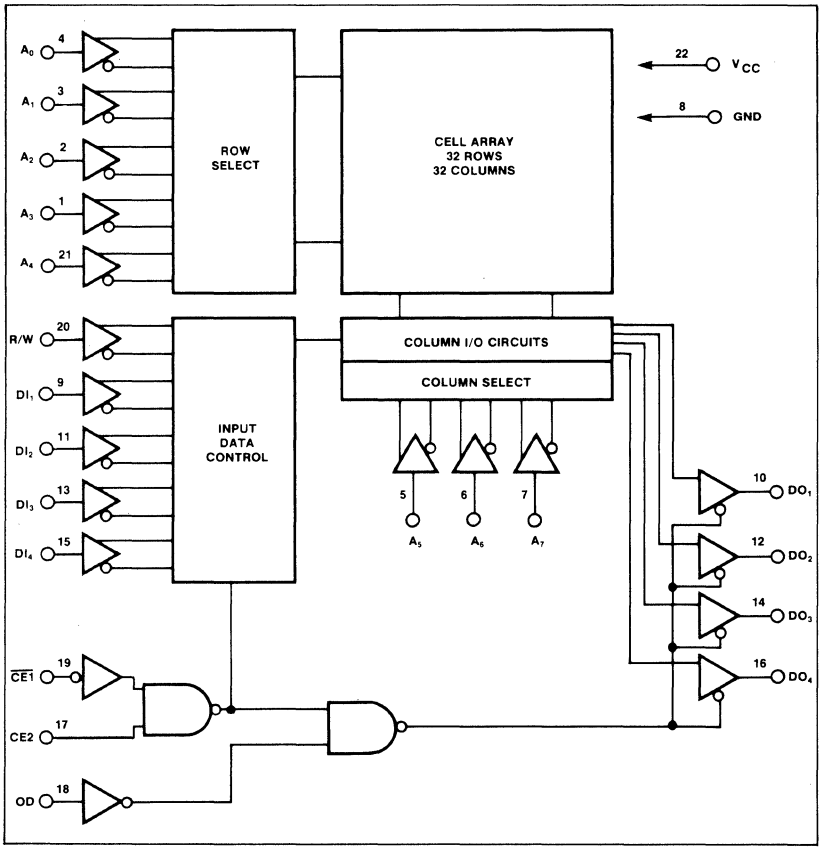
- **Fully static**
- **No refresh operations, sense amps or clocks required**
- **All inputs and outputs are TTL compatible**
- **One 5V power supply required**

PIN CONFIGURATION

F,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA			0.45	
V_{OH}	High	I_{OH} = 150μA	2.2			
I_{LI}	Input current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current[3]	$\overline{CE}_1$ = 2.2V				μA
I_{LOH}		V_{OUT} = 4.0V			15	
I_{LOL}		V_{OUT} = 0.45V			-50	
	Supply current	V_{IN} = 5.25V, I_O = OmA				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]					pF
C_{IN}	Input (All pins)	V_{IN} = 0V		4	8	
C_{OUT}	Output	V_{OUT} = 0V		8	12	

AC ELECTRICAL CHARACTERISTICS

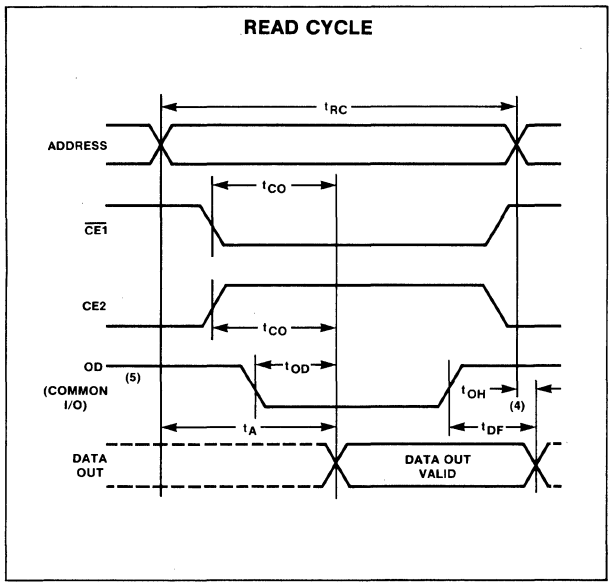
T_A =0°C to 70°C, V_{CC} = 5V ± 5%, Input pulse levels = +0.65V to 2.2V, Input pulse rise and fall times = 20ns, Timing measurement reference level = 1.5V, Output load = 1 TTL gate and C_L = 100pF, unless otherwise specified.

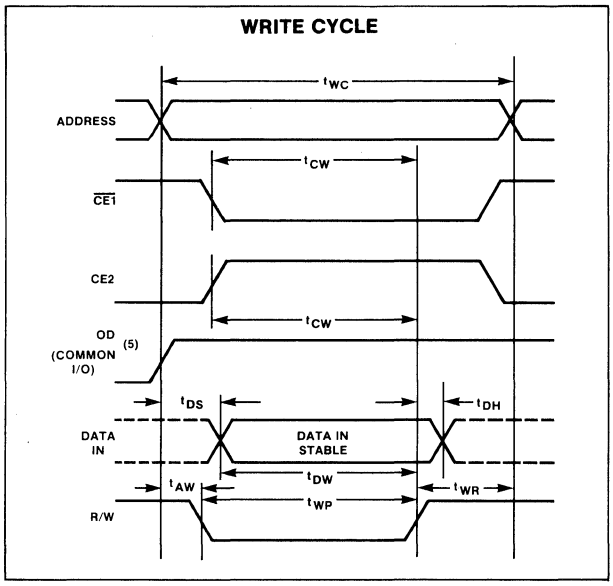
PARAMETER		TO	FROM	2101			2101-1			2101-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE												
t_{RC}	Read cycle			1,000			500			650			ns
t_A	Access time					1,000			500			650	ns
t_{CO}		Output	Chip enable			800			350			400	ns
t_{OD}		Output	Output disable			700			300			350	ns
t_{DF}[4]		High Z state	Data output	0		200	0		150	0		150	ns
t_{OH}	Previous read data valid after change of address			40			40			40			ns
	WRITE CYCLE												
t_{WC}	Write cycle			1,000			500			650			ns
t_{AW}	Write delay			150			100			150			ns
t_{CW}		Write	Chip enable	900			400			550			ns
	Setup and hold time												ns
t_{DW}	Setup time	Rise of R/W	Data in	700			280			400			
t_{DH}	Hold time	Change of data in	Rise of R/W	100			100			100			
t_{DS}	Setup time	Output	Output disable	200			150			150			
t_{WP}	Write pulse			750			300			400			ns
t_{WR}	Write recovery			50			50			50			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2 or OD, whichever occurs first.
5. CD should be tied low for separate I/O operation.

TIMING DIAGRAMS





2111-I,N • 2111-1-I,N • 2111-2-I,N

DESCRIPTION

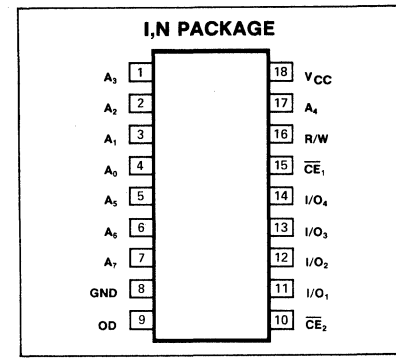
The 2111 series is a high-performance, low-power static read/write RAM.

The 2111 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

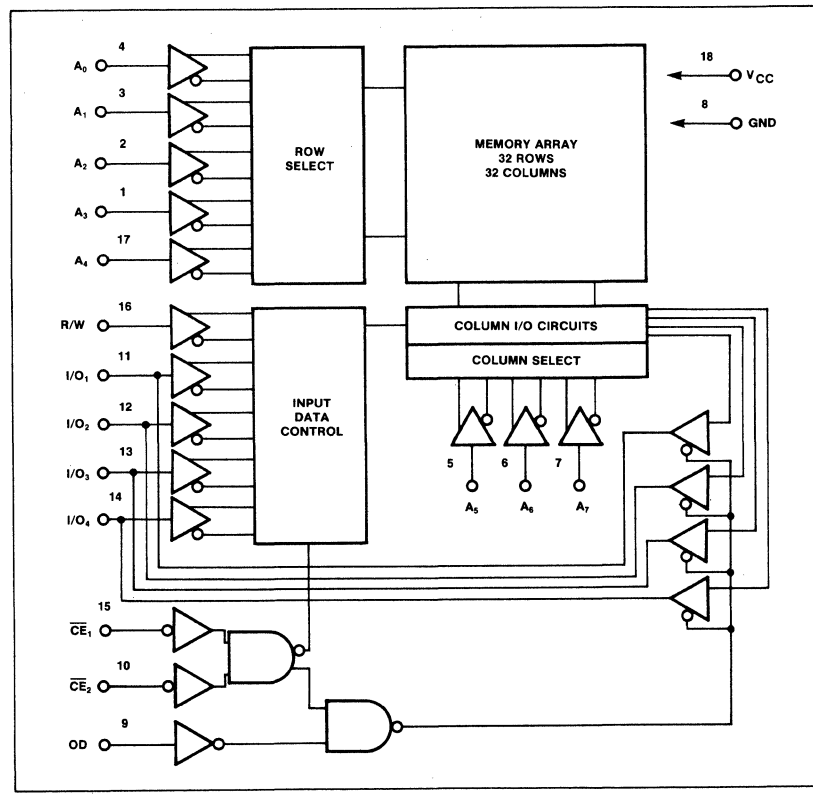
FEATURES

- **Fully static**
- **Requires no refresh operations, sense amps or clocks**
- **Completely TTL compatible**
- **Only one 5V power supply required**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA			0.45	
V_{OH}	High	I_{OH} = -150μA	2.2			
I_{LI}	Input load current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current	$\overline{CE_1}$ = $\overline{CE_2}$ = 2.2V				μA
I_{LOH}		$V_{1/0}$ = 4.0V			15	
I_{LOL}		$V_{1/0}$ = 0.45V			-50	
	Supply current	V_{IN} = 5.25V, $I_{1/0}$ = OmA				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	
	Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN}	Input	V_{IN} = OV		4	8	
$C_{I/O}$	I/O	$V_{I/O}$ = OV		10	15	

AC ELECTRICAL CHARACTERISTICS

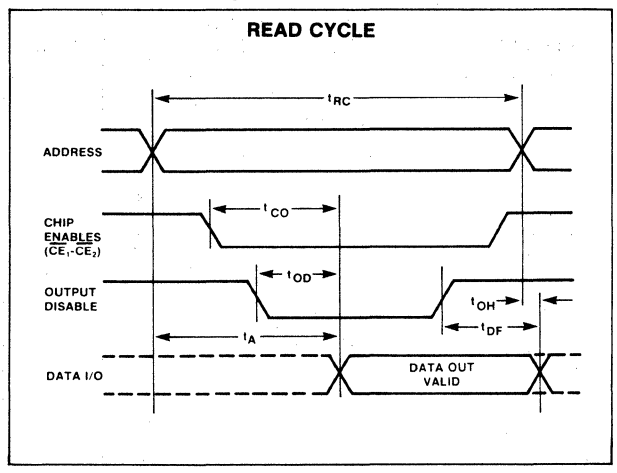
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified,
Input pulse levels = 0.65V to 2.2V, Input pulse rise and fall times = 20ns,
Timing measurement reference level = 1.5V,
Output load = 1 TTL gate and C_L = 100pF

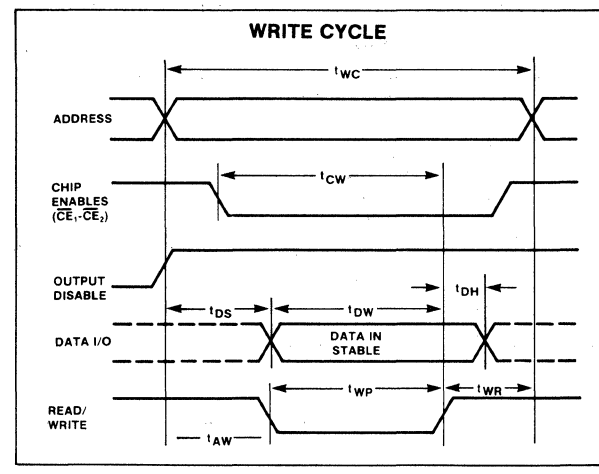
PARAMETER		TO	FROM	2111			2111-1			2111-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ CYCLE												
t_{RC}	Read cycle			1,000			500			650			ns
t_A	Access time					1,000			500			650	ns
t_{CC}		Output	Chip enable			800			350			400	ns
t_{OD}		Output	Output disable			700			300			350	ns
t_{DF}[3]		High Z state	Data output	0		200	0		150	0		150	ns
t_{OH}	Previous read data valid after change of address			40			40			40			ns
	WRITE CYCLE												
t_{WC}	Write cycle			1,000			500			650			ns
t_{AW}	Write delay			150			100			150			ns
t_{CW}		Write	Chip enable	900			400			550			ns
	Setup and hold time												ns
t_{DW}	Setup time	R/W	Data	700			280			400			
t_{DH}	Hold time	Data	R/W	100			100			100			
t_{DS}	Setup time	Output	Output disable	200			150			150			
t_{WP}	Write pulse			750			300			400			ns
t_{WR}	Write recovery			50			50			50			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values for T_A = 25°C and supply voltage.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS





2112-F,N • 2112-1-F,N • 2112-2-F,N

DESCRIPTION

The 2112 series is high performance, low power static read/write RAMs.

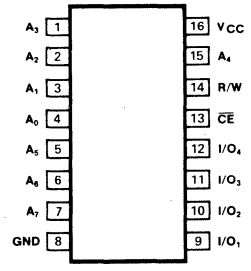
The 2112 series is fabricated with n-channel silicon gate technology which allows the design of high performance easy to use MOS circuits and provides a high functional density on a given monolithic chip.

FEATURES

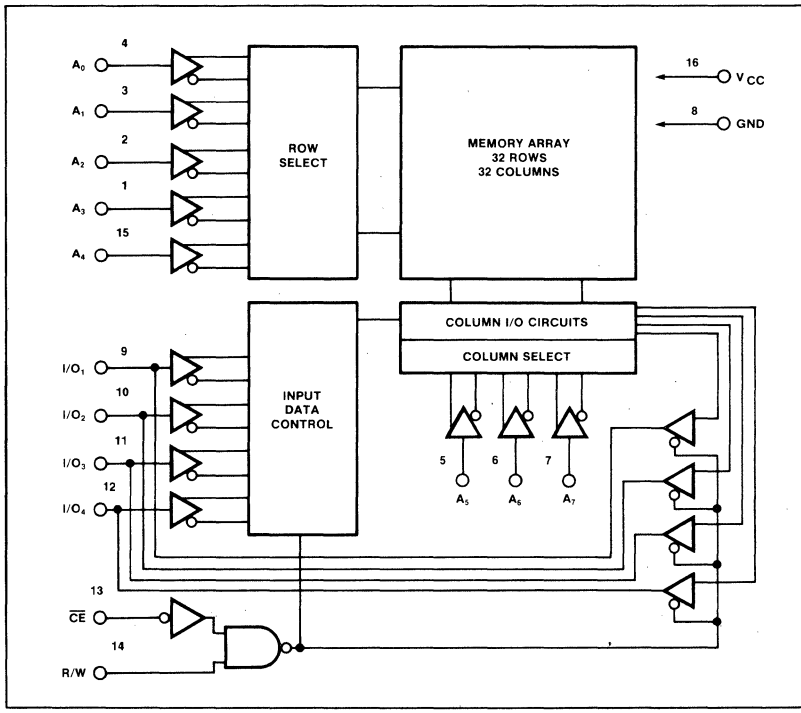
- **Fully static**
- **No refresh operations, sense amps or clocks required**
- **Directly TTL compatible**
- **One 5V power supply**

PIN CONFIGURATION

F,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
	Voltage on any pin with respect to ground	-0.5 to 7	V
P_D	Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ[2]	Max	
Input voltage					V
V_{IL} Low		-0.5		0.65	
V_{IH} High		2.2		V_{CC}	
Output voltage					V
V_{OL} Low	I_{OL} = 2mA			0.45	
V_{OH} High	I_{OH} = -150μA	2.2			
I_{LI} Input current	V_{IN} = 0 to 5.25V			10	μA
I/O leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}	$V_{I/O}$ = 4.0V			15	
I_{LOL}	$V_{I/O}$ = 0.45V			-50	
Supply current	V_{IN} = 5.25V, $I_{I/O}$ = 0mA				mA
I_{CC1}	T_A = 25°C		30	60	
I_{CC2}	T_A = 0°C			70	
Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN} Input (All pins)	V_{IN} = 0V		4	8	
$C_{I/O}$ I/O	$V_{I/O}$ = 0V		10	15	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
t_R and t_F = 20ns, V_{IN} = 0.65V to 2.2V, Timing reference = 1.5V,
Load = 1 TTL gate and C_L = 100pF

PARAMETER	TO	FROM	2112			2112-1			2112-2			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
READ CYCLE												
t_{RC} Read cycle			1000			500			650			ns
t_A Access time					1000			500			650	ns
t_{CO}	Output	Chip enable			800			150			500	ns
t_{CD}	Output disable	Chip enable	0		200	0		100	0		150	ns
t_{OH} Previous read data valid after change of address			40			40			40			ns
WRITE CYCLE #1												
t_{WC1} Write cycle			850			500			500			ns
Setup and hold time												ns
t_{AW1} Setup time	Write	Address	150			100			100			
t_{DW1} Setup time	R/W high	Data	650			250			280			
t_{CS1} Setup time	$\overline{CE}$ low	R/W low	0			0			0			
t_{CH1} Hold time	$\overline{CE}$ high	R/W high	0			0			0			
t_{DH1} Hold time	Data	R/W high	100			50			50			
t_{CW1} Setup time	R/W high	$\overline{CE}$ low	650			250			350			
t_{WP1} Write pulse width			650			250			350			ns
t_{WR1} Write recovery time			50			50			50			ns
WRITE CYCLE #2												
t_{WC2} Write cycle			1050			500			650			ns
Setup and hold time												ns
t_{AW2} Setup time	Write	Address	150			100			100			
t_{DW2} Setup time	R/W high	Data	650			250			280			
t_{CS2} Setup time	$\overline{CE}$ low	R/W low	0			0			0			
t_{CH2} Hold time	$\overline{CE}$ high	R/W high	0			0			0			
t_{DH2} Hold time	Data	R/W high	100			50			50			
t_{WD2} Disable time	R/W high	Data	200			200			200			ns
t_{WR2} Write recovery time			50			50			50			ns

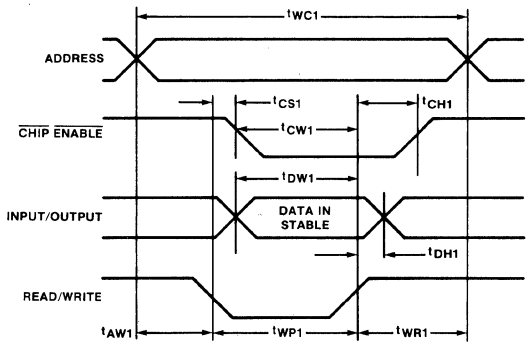
NOTES on following page.

NOTES

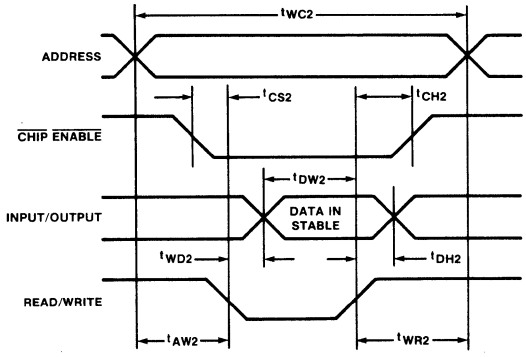
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for $T_A = 25°C$ and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. Output is enabled and t_{CO} commences only with both CE low and WE high.
5. Output is disabled and t_{DF} combined from either the rising edge of CE or the falling edge of WE.
6. Minimum t_{WP} is valid when CE has been high at least t_{DF} before WE goes low. Oherwise $t_{WP(min)} = t_{DW(min)} + t_{DF(max)}$.
7. When WE goes high at the end of the write cycle, it will be possible to turn on the output buffers if CE is still low. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.

VOLTAGE WAVEFORMS

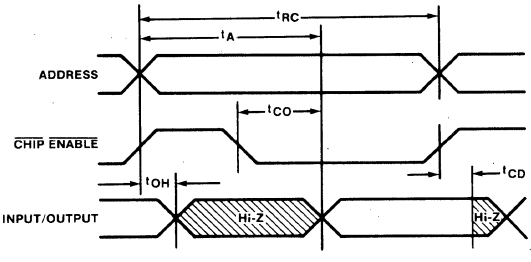
WRITE CYCLE #1



WRITE CYCLE #2



READ CYCLE



2606-F,I,N • 2606-1-F,I,N

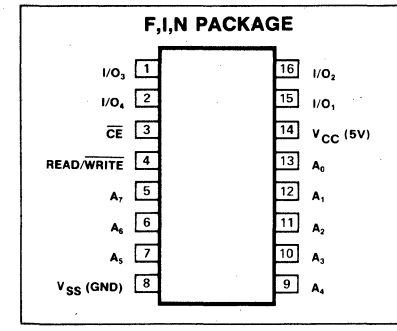
DESCRIPTION

The 2606 is fabricated with n-channel silicon gate MOS technology and achieves an access time of less than 750ns.

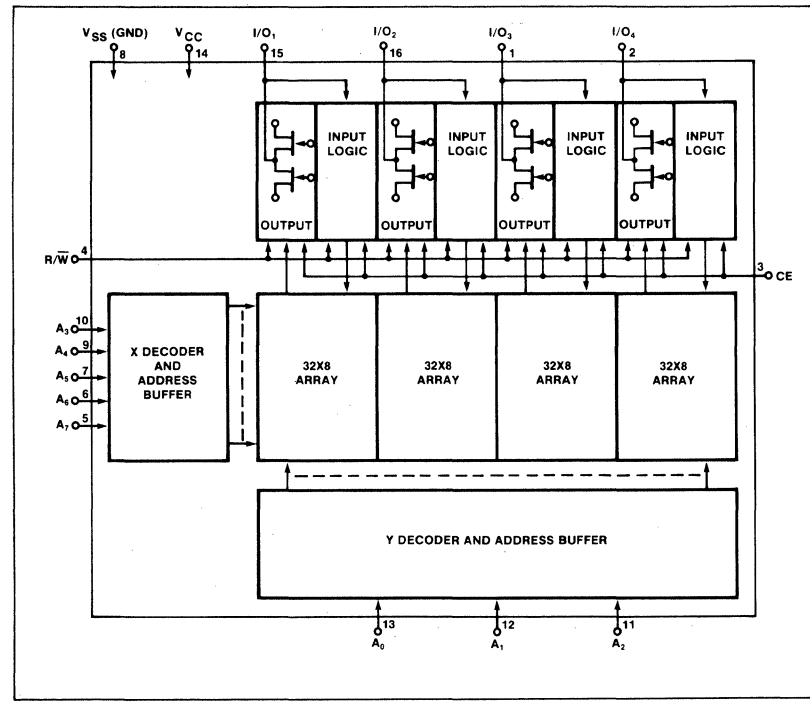
FEATURES

- **Fully decoded**
- **No clocks required**
- **All interface signals, including power supply directly TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.9mA			0.45	
V_{OH}	High	I_{OH} = -100μA	2.4			
I_{LI}	Input current	V_{IN} = 0 to 5.25V			10	μA
	I/O leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}		$V_{I/O}$ = 4.0V			10	
I_{LOL}		$V_{I/O}$ = 0.45V			-100	
	Supply current	V_{IN} = 5.25V, $I_{I/O}$ = OmA				mA
I_{CC1}		T_A = 25°C			70	
I_{CC2}		T_A = 0°C			80	
	Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN}	Input (All pins)	V_{IN} = OV		4	7	
$C_{I/O}$	I/O	V_{OUT} =OV		7	10	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C, V_{CC} = 5V ± 5% unless other specified.[4,5,6,7]

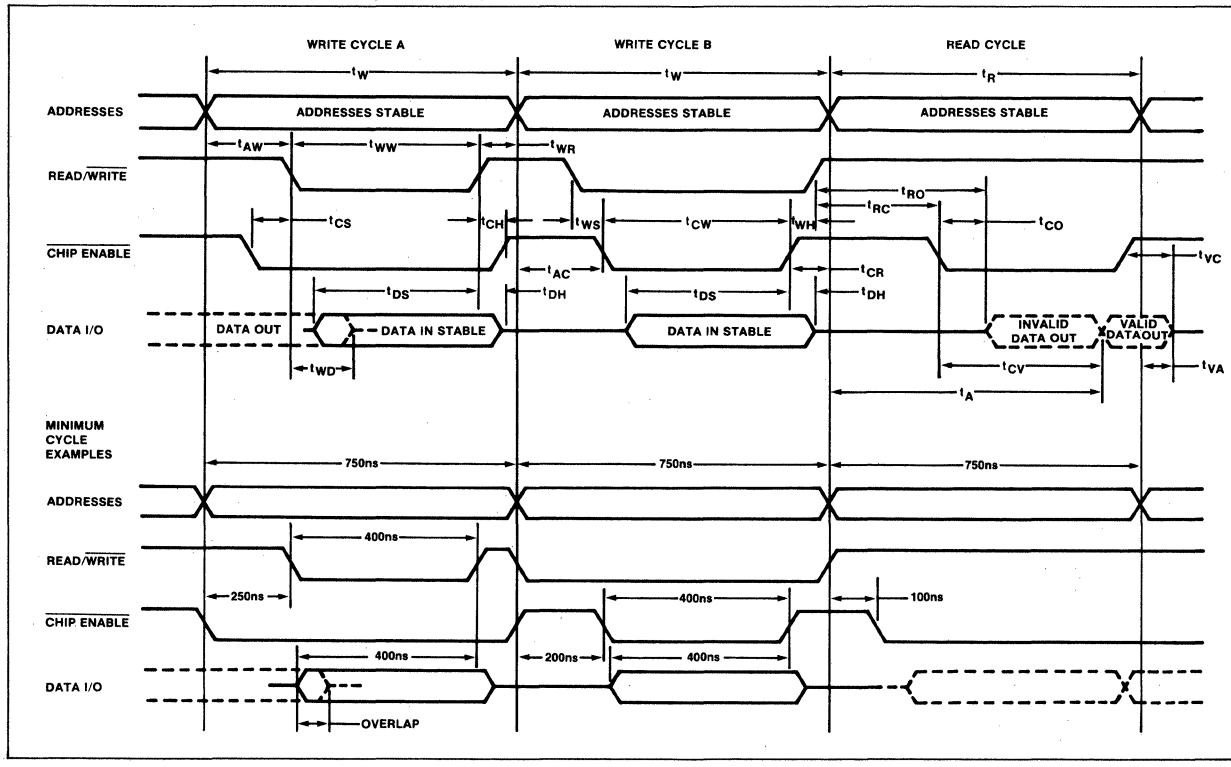
PARAMETER		TO	FROM	2606			2606-1			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ CYCLE									
t_R	Read cycle time			750			500			ns
t_A	Access time					750			500	ns
T_{RO}[8]		Output enable	Read	100			75			ns
t_{CO}[8]		Output enable	Chip enable	0			0			ns
	Previous data valid with respect to									ns
t_{VC}	Chip disable			0		150	0		100	
t_{VA}	Address change			50			50			
t_{CV}	Delay time	Data valid	Chip enable			400			300	ns
t_{RC}		Chip enable	Read	100			50			ns
	WRITE CYCLE A									
t_W	Write cycle time			750			500			ns
t_{AW}		Write	Address	250			150			ns
t_{WW}	Write pulse width			400			300			ns
t_{WR}	Write recovery time			100			50			ns
	Setup and hold time									ns
t_{CS}	Setup time	R/W	Chip enable	0			0			
t_{CH}	Hold time	Chip enable	R/W							
t_{DS}	Setup time	R/W	Data	380			280			
t_{DH}	Hold time[9]	Data	R/W	0			0			
t_{WD}	Disable delay[10]	Data out	Write			125			100	ns
	WRITE CYCLE B									
t_W	Write cycle time			750			500			ns
t_{AC}		Chip enable	Address	250			150			ns
t_{CW}	Chip enable pulse width			400			300			ns
t_{CR}	Chip enable recovery time			100			50			ns
	Setup and hold time[11]									ns
t_{WS}	Setup time	Chip enable	R/W	200			100			
t_{WH}	Hold time	R/W	Chip enable	0			0			
t_{DS}	Setup time	Chip enable	Data	380			280			
t_{DH}	Hold time[8]	Data	Chip enable	0			0			

NOTES on following page.

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25° C and typical supply voltage.
3. This parameter is periodically sampled and is not 100% tested.
4. Input levels swing between 0.65V and 2.2V.
5. Input signal transition times are 20ns.
6. Timing reference level is 1.5V.
7. Bus load is 100pF, 1 TTL tri-state output.
8. R/$\overline{W}$ must be high and CE must be low in order for output buffers to turn on.
9. Maximum t_{DH} governed by potential conflict with data out during next cycle.
10. The output buffers will turn off within the specified time after write mode is selected.
11. Write setup required to prevent data overlap. For write cycle B the R/$\overline{W}$ line will typically change with the addresses.

TIMING DIAGRAM



2102-F,I,N • 2102-1-F,I,N • 2102-2-F,I,N

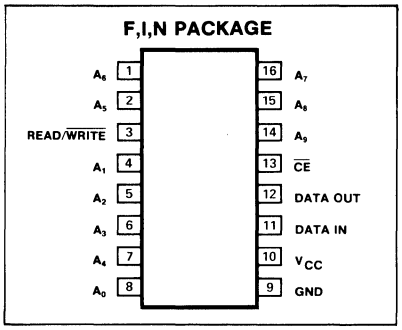
DESCRIPTION

The 2102, 2102-1 and 2102-2 are static random access read/write memories fabricated with low threshold n-channel silicon gate technology.

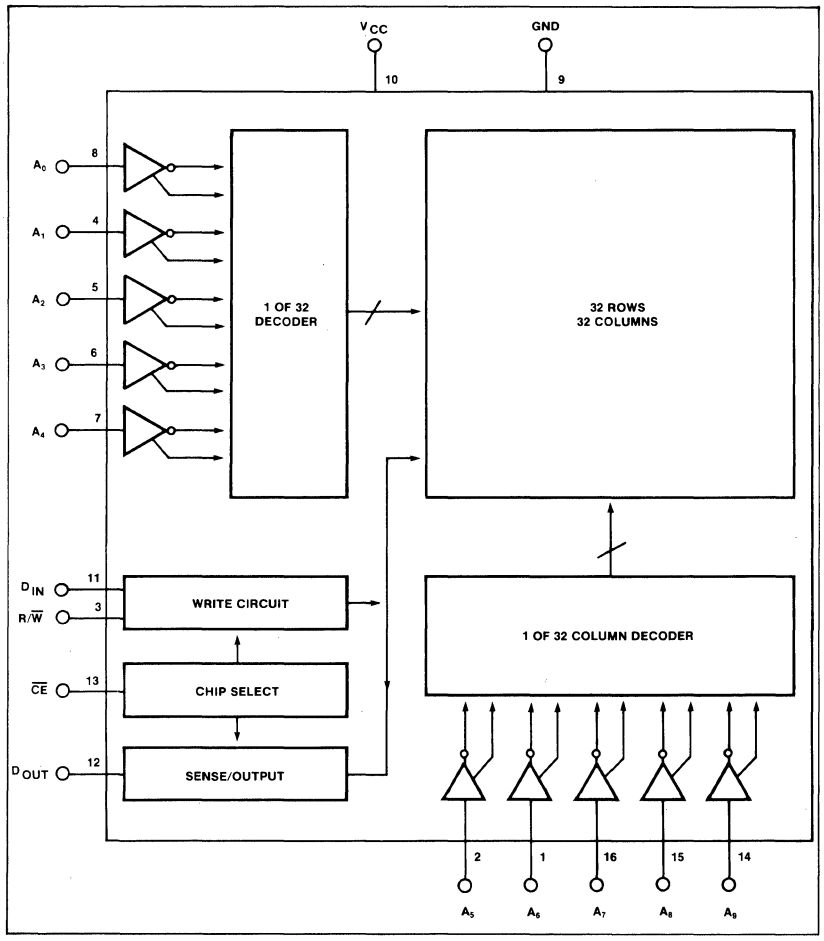
FEATURES

- **Fully static**
- **Require no clocks**
- **Completely DTL/TTL compatible**
- **Single 5V power supply**
- **Three-state output for OR-tie capability**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation[2]		
	N package	640	mW
	F package	1	W
	I package	1	W
	All input, output and supply voltages with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ[1]	Max	
Input voltage					V
V_{IL} Low		-0.5		0.65	
V_{IH} High		2.2		V_{CC}	
Output voltage					V
V_{OL} Low	I_{OL} = 1.9mA			0.45	
V_{OH} High	I_{OH} = -100μA	2.2			
I_{LI} Input load current (All input pins)	V_{IN} = 0 to 5.25V			10	μA
Leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}	V_{OUT} = 4.0V			10	
I_{LOL}	V_{OUT} = 0.45V			-100	
Supply current	All inputs = 5.25V, Data out open				mA
I_{CC1}	T_A = 25°C		30	60	
I_{CC2}	T_A = 0°C			70	

AC ELECTRICAL CHARACTERISTICS

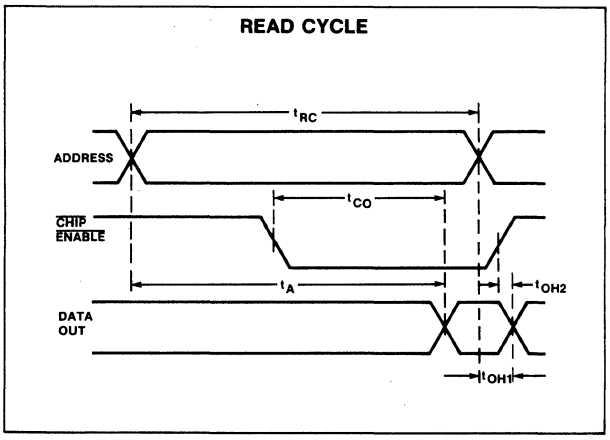
T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

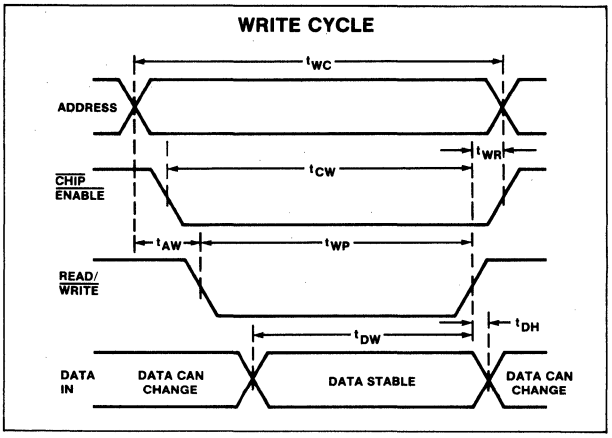
PARAMETER	TO	FROM	2102			2102-1			2102-2			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
READ CYCLE												
t_{RC} Read cycle			1,000			500			650			ns
t_A Access time					1,000			500			650	ns
t_{CO}	Output	Chip enable			500			350			400	ns
Previous data valid with respect to												ns
t_{OH1} Address			50			50			50			
t_{OH2} Chip enable			0			0			0			
WRITE CYCLE												
t_{WC} Write cycle			1,000			500			650			ns
t_{WP} Write pulse width			750			300			400			ns
t_{WR} Write recovery time			50			50			50			ns
Setup and hold time												ns
t_{AW} Setup time	Write	Address	200			150			200			
t_{DW} Setup time	Rise of R/$\overline{W}$	Data in	800			330			450			
t_{DH} Hold time	Change of data in	Rise of R/$\overline{W}$	100			100			100			
t_{CW} Setup time	Write	Chip enable	900			400			550			

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient ("B" package).
3. All inputs protected against static charge.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.

TIMING DIAGRAMS





DESCRIPTION

The 2102A is a high speed static random access memory element using n-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. A low standby power version (2102AL) is also available, and has all the same operating characteristics of the 2102A with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.

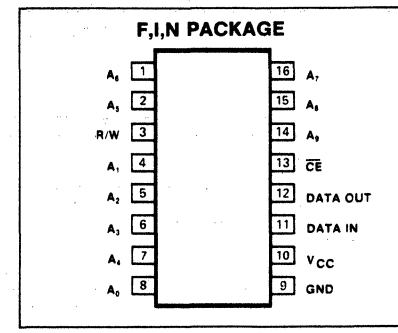
A separate chip enable ($\overline{CE}$) lead allows easy selction of an individual package when outputs are OR-tied.

The 2102A is fabricated with n-channel silicon gate technology, which allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or p-channel silicon gate technology.

FEATURES

- **Single 5V supply voltage**
- **Fully TTL compatible**
- **Standby power mode (2102AL)**
- **Tri-state output**
- **OR-tie capability**
- **All inputs protected against static charge**
- **Low cost packaging**

PIN CONFIGURATION



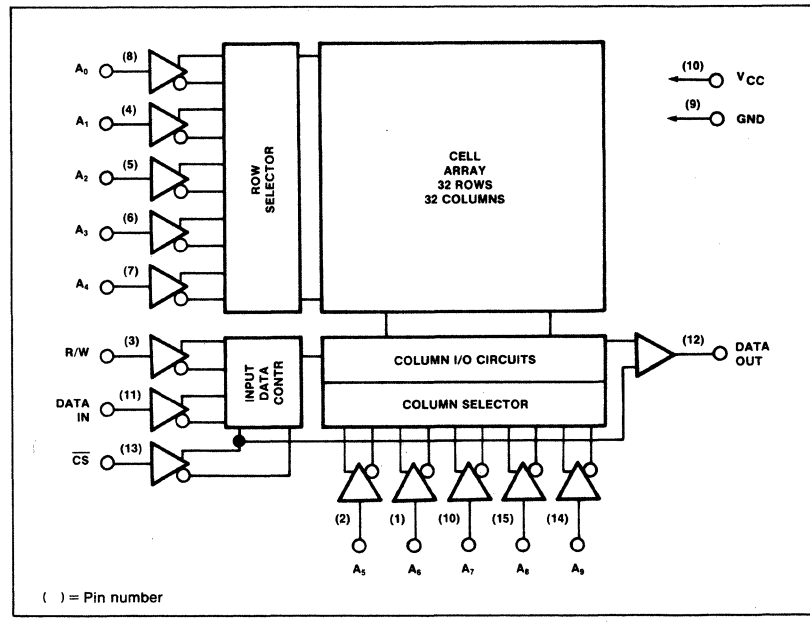
PIN DESIGNATION

PIN NO.	SYMBOL	FUNCTION	TYPE
11	D_{IN}	Data input	
1,2,4-8,14,16	A_0-A_9	Address inputs	
3	R/W	Read/write input	
13	$\overline{CE}$	Chip enable	
12	D_{OUT}	Data output	
10	V_{CC}	Power (5V)	
9	GND	Ground	

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	High Z	Not selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	-10 to 80	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	Voltage on any pin with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	2102A/2102A-4/ 2102AL/2102AL-4			2102A-2/ 2102AL-2			2102A-6			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage											V
V_{IL}	Low		-0.5		0.8	-0.5		0.8	-0.5		0.65	
V_{IH}	High		2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	
	Output voltage											V
V_{OL}	Low	$I_{OL} = 2.1mA$			0.4			0.4			0.45	
V_{OH}	High	$I_{OH} = -100\mu A$	2.4			2.4			2.2			
I_{LI}	Input load current	$V_{IN} = 0$ to 5.25V		1	10		1	10		1	10	μA
	Output leakage current	$\overline{CE} = 2.0V$										μA
I_{LOH}		$V_{OUT} = V_{OH}$		1	5		1	5		1	5	
I_{LOL}		$V_{OUT} = 0.4V$		-1	-10		-1	-10		-1	-10	
I_{CC}	Supply current[3]	Data out open, $T_A = 0°C$		33			45	65		33	55	mA
	Capacitance[4]											pF
C_{IN}	Input (All pins)	$V_{IN} = 0V$		3	5		3	5		3	5	
C_{OUT}	Output	$V_{OUT} = 0V$		7	10		7	10		7	10	

STANDBY CHARACTERISTICS $T_A = 0°C$ to $70°C$

PARAMETER		TEST CONDITIONS	2102AL, 2102AL-4			2102AL-2			UNIT
			Min	Typ[5]	Max	Min	Typ[5]	Max	
V_{PD}	V_{CC} in standby		1.5			1.5			V
V_{CES}	$\overline{CE}$ bias in standby[6]	$2.0V \le V_{PD} \le V_{CC}$ max	2.0			2.0			V
		$1.5V \le V_{PD} < 2.0V$	V_{PD}			V_{PD}			
	Standby current								mA
I_{PD1}		All inputs = $V_{PD1} = 1.5V$		15	23		20	28	
I_{PD2}		All inputs = $V_{PD2} = 2.0V$		20	30		25	38	
t_{CP}	Chip deselect to standby time		0			0			ns
t_R	Standby recovery time[7]		t_{RC}			t_{RC}			ns

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise noted,
Input pulse levels = 0.8V to 2.0V, Input rise and fall times = 10ns,
Timing measurement reference level inputs = 1.5V
Output = 0.8V and 2.0V, Output load = 1 TTL gate and C_L = 100pF

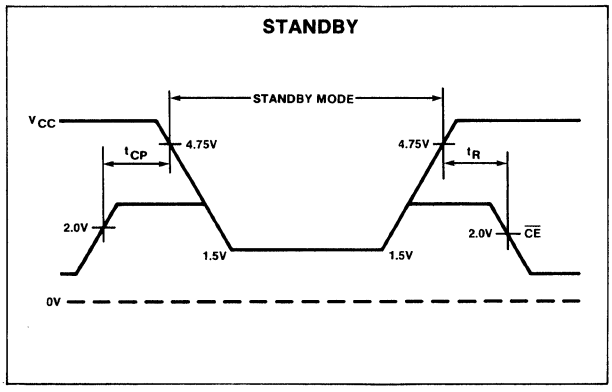
	PARAMETER	TO	FROM	2102A-2, 2102AL-2			2102A, 2102AL			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ CYCLE									
t_{RC}	Read cycle			250			350			ns
t_A	Access time					250			350	ns
t_{CO}		Output time	Chip enable			130			180	ns
	Previous read data valid with respect to									ns
t_{OH1}	Address			40			40			
t_{OH2}	Chip enable			0			0			
	WRITE CYCLE									
t_{WC}	Write cycle			250			350			ns
t_{WP}	Write pulse width			180			250			ns
t_{WR}	Write recovery time			0			0			ns
	Setup and hold time									ns
t_{AW}	Setup time	Write	Address	20			20			
t_{DW}	Setup time	R/W	Data	180			250			
t_{DH}	Hold time	Output	Data	0			0			
t_{CW}	Setup time	Data	R/W	180			250			

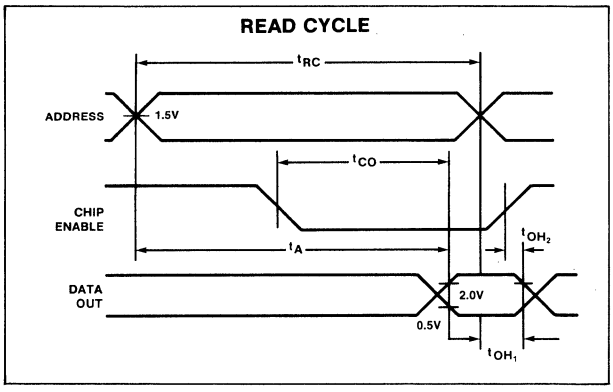
	PARAMETER	TO	FROM	2102A-4, 2102AL-4			2102A-6			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ CYCLE									
t_{RC}	Read cycle			450			650			ns
t_A	Access time					450			650	ns
t_{CO}		Output time	Chip enable			230			400	ns
	Previous read data valid with respect to									ns
t_{OH1}	Address			40			50			
t_{OH2}	Chip enable			0			0			
	WRITE CYCLE									
t_{WC}	Write cycle			450			650			ns
t_{WP}	Write pulse width			300			400			ns
t_{WR}	Write recovery time			0			50			ns
	Setup and hold time									ns
t_{AW}	Setup time	Write	Address	20			200			
t_{DW}	Setup time	R/W	Data	300			450			
t_{DH}	Hold time	Output	Data	0			20			
t_{CW}	Setup time	Data	R/W	300			550			

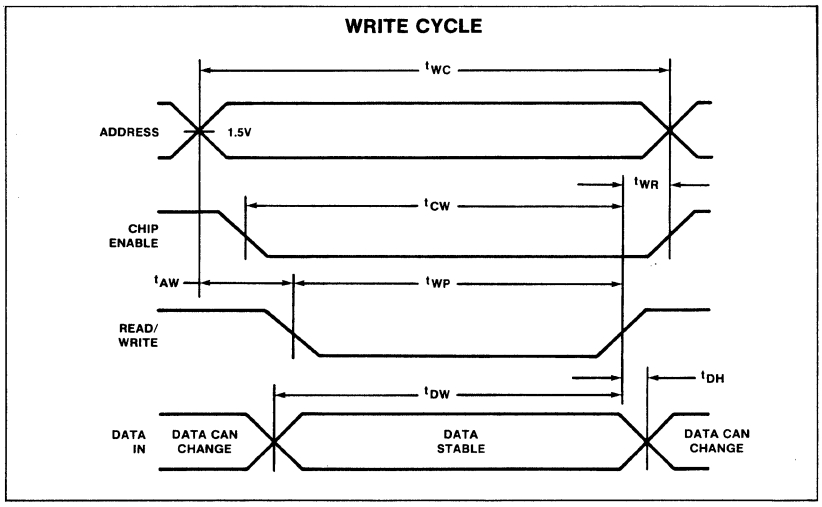
NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltage.
3. The maximum I_{CC} value is 55mA for the 2102A and 2102A-4, and 33mA for the 2102AL and 2102AL-4.
4. This parameter is periodically sampled and is not 100% tested.
5. Typical values are for T_A = 25°C.
6. Consider the test conditions as shown: if the standby voltage (V_{PD}) is between 5.25V (V_{CC} max) and 2.0V, then $\overline{CE}$ must be held at 2.0V min (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the 2.
7. $t_R = t_{RC}$ (read cycle time).

VOLTAGE WAVEFORMS







21F02-F,I,N • 21F02-2 - F,I,N • 21F02-4 - F,I,N

DESCRIPTION

The 21F02 is a high speed static random access memory element using n-channel MOS devices integrated on a monolithic array. It uses fully dc stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

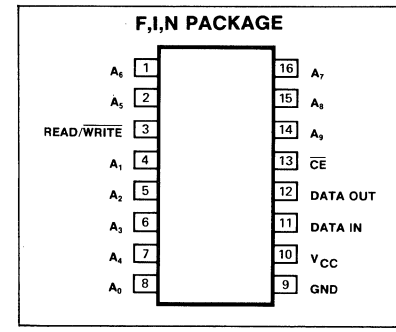
The 21F02 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. A separate chip enable (CE) lead allows easy selection of an individual package when outputs are OR-tied.

The Signetics 21F02 is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or p-channel silicon gate technology.

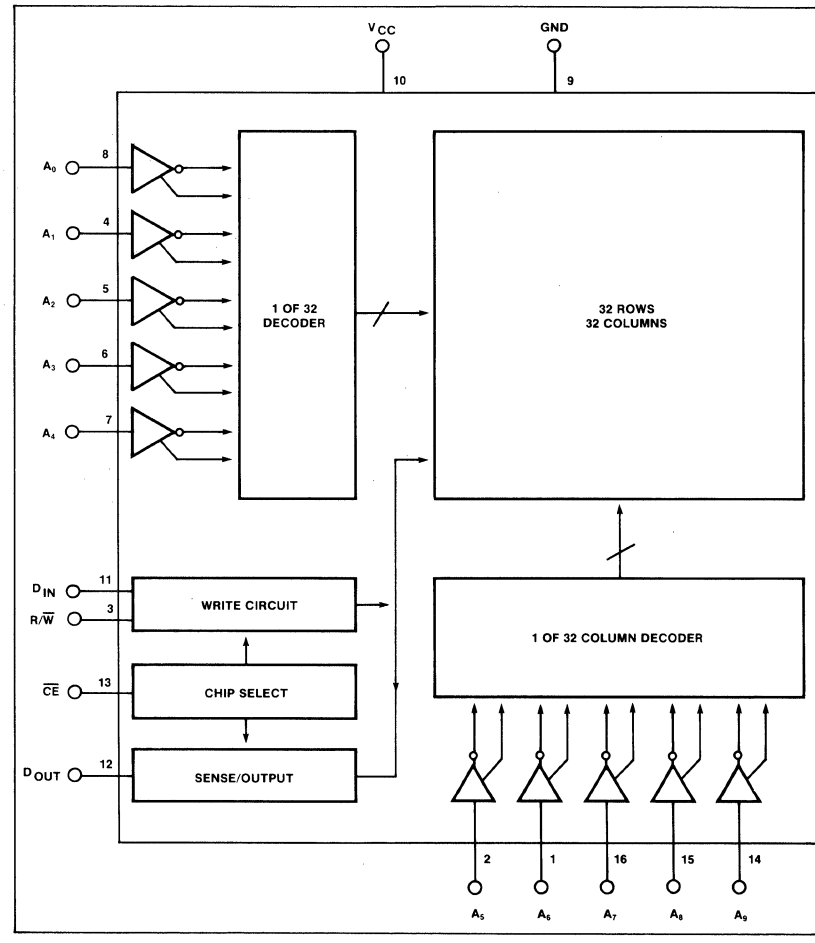
FEATURES

- **Fully TTL compatible**
- **Single 5V supply**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation[2]		
	N package	640	mW
	F package	1	W
	I package	1	W
	All input, output and supply voltages with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.0		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.1mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4			
I_{LI}	Input load current (All input pins)	V_{IN} = 0 to 5.25V			10	μA
	Output leakage current	$\overline{CE}$ = 2.0V				μA
I_{LOH}		V_{OUT} = 2.4 to V_{CC}			5	
I_{LOL}		V_{OUT} = 0.4V			-10	
	Supply current	All inputs = 5.25V, Data out open				mA
I_{CC1}		T_A = 25°C		30	60	
I_{CC2}		T_A = 0°C			70	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
Input pulse levels = 0.65 to 2.2V, Input pulse rise and fall times = 20ns,
Timing measurement reference level = 1.5V,
Output load = 1 TTL gate and C_L = 100pF

	PARAMETER	TO	FROM	21F02			21F02-2			21F02-4			UNIT
				Min	Typ[3]	Max	Min	Typ[3]	Max	Min	Typ[3]	Max	
	READ CYCLE												
t_{RC}	Read cycle			350			250			450			ns
t_A	Access time					350			250			450	ns
t_{CO}		Output time	Chip enable			180			130			230	ns
	Previous read data valid with respect to												ns
t_{OH1}	Address			40			40			40			
t_{OH2}	Chip enable			0			0			0			
	WRITE CYCLE												
t_{WC}	Write cycle			350			250			450			ns
t_{WP}	Write pulse width			250			180			300			ns
t_{WR}	Write recovery time			20			20			20			ns
	Setup and hold time												ns
t_{AW}	Setup time	Write	Address	20			20			20			
t_{DW}	Setup time	Output	Data	250			180			300			
t_{DH}	Hold time	Output	Data	0			0			0			
t_{CW}	Setup time	Write	Chip enable	250			180			300			

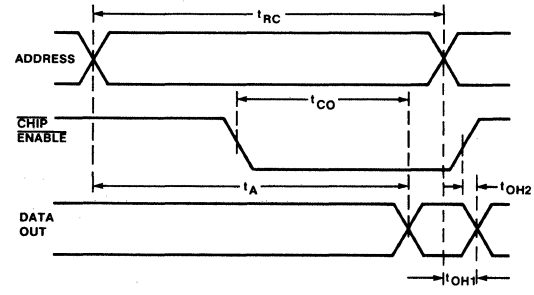
NOTES on following page.

NOTES

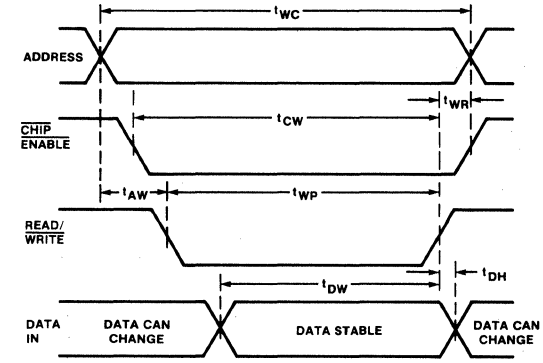
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient (B package).
3. Typical values are at +25°C and typical supply voltages.
4. All inputs protected against static charge.
5. Parameter valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE



21L02-F,I,N • 21L02-1-F,I,N • 21L02-2-F,I,N • 21L02-3-F,I,N

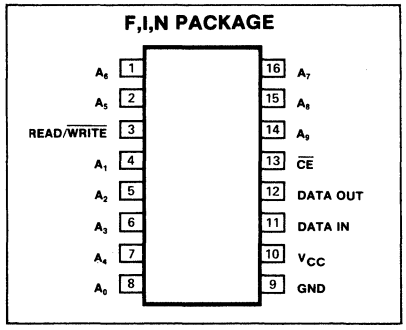
DESCRIPTION

The 21L02, 21L02-1, 21L02-2, and 21L02-3 are low power static random access read/write memories fabricated with low threshold n-channel silicon gate technology.

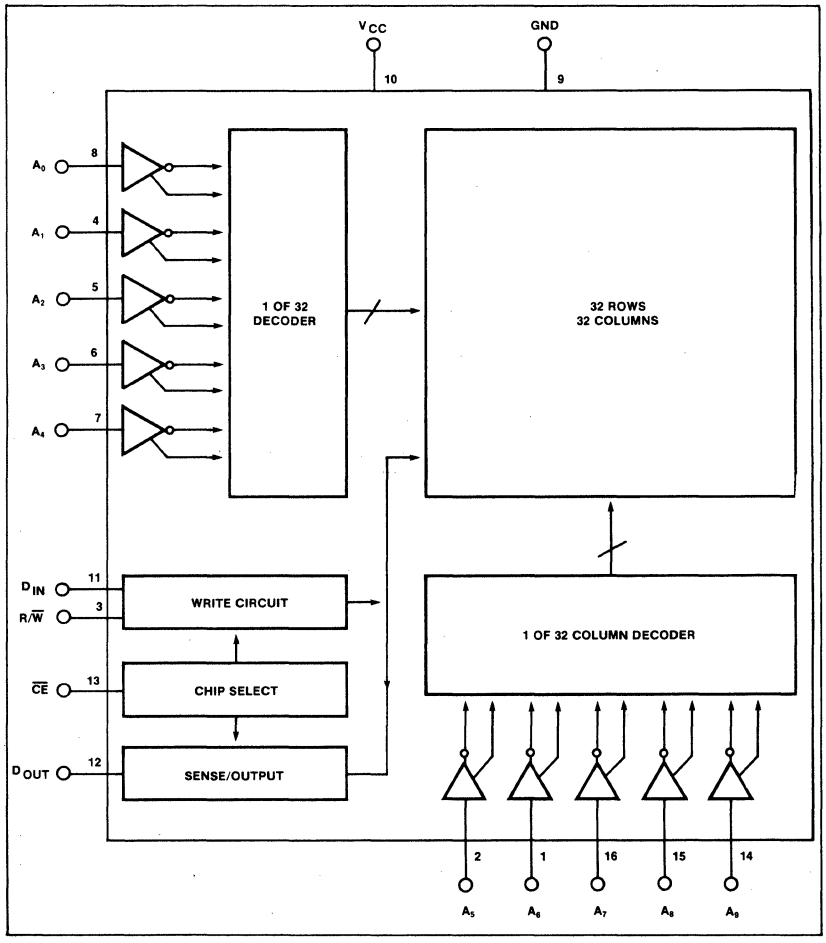
FEATURES

- **Fully static**
- **Requires no clocks**
- **Completely DTL/TTL compatible**
- **Single 5V power supply**
- **Three-state output for OR-tie capability**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation[2]		
	N package	640	mW
	F package	1	W
	I package	1	W
	All input, output and supply voltages with respect to ground	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ[3]	Max	
Input voltage					V
V_{IL} Low		-0.5		0.65	
V_{IH} High		2.2		V_{CC}	
Output voltage					V
V_{OL} Low	I_{OL} = 1.9mA			0.45	
V_{OH} High	I_{OH} = -100μA	2.2			
I_{LI} Input load current (All input pins)	V_{IN} = 0 to 5.25V			10	μA
Output leakage current	$\overline{CE}$ = 2.2V				μA
I_{LOH}	V_{OUT} = 4.0V			10	
I_{LOL}	V_{OUT} = 0.45V			-100	
Supply current	All inputs = 5.25V, Data out open				mA
I_{CC1}	T_A = 25°C		30	40	
I_{CC2}	T_A = 0°C			40	

AC ELECTRICAL CHARACTERISTICS

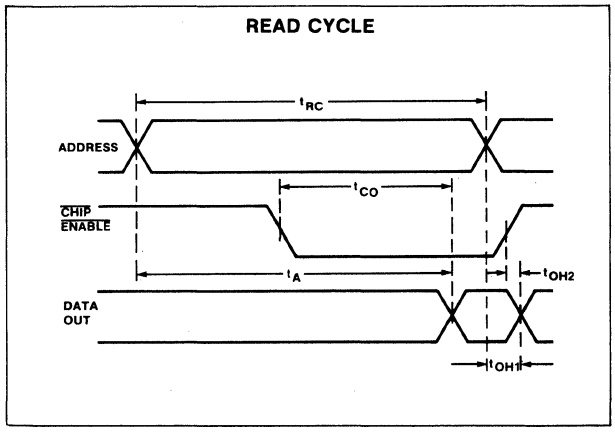
T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
Input pulse levels = 0.65V to 2.2V, Input pulse rise and fall times = 20ns,
Timing measurement reference level = 1.5V, Output load = 1 TTL gate
and C_L = 100pF

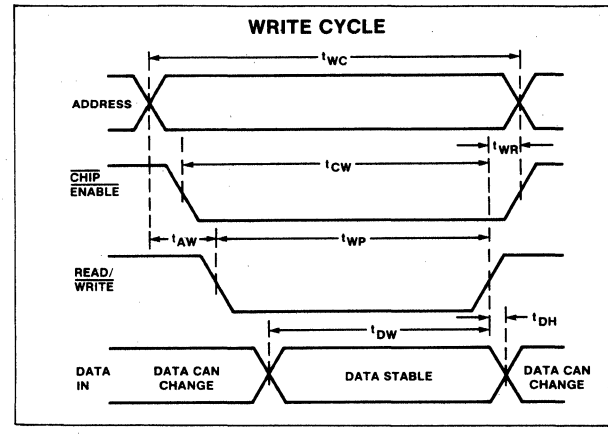
PARAMETER	TO	FROM	21L02			21L02-1			21L02-2			21L02-3			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
READ CYCLE															
t_{RC} Read cycle			1,000			500			650			400			ns
t_A Access time					1,000			500			650		400		ns
t_{CO}	Output time	Chip enable			500			350			400		300		ns
Previous read data valid with respect to															ns
t_{OH1} Address			50			50			50			50			
t_{OH2} Chip enable			0			0			0			0			
WRITE CYCLE															
t_{WC} Write cycle			1,000			500			650			400			ns
t_{WP} Write pulse width			750			300			400			250			ns
T_{WR} Write recovery time			50			50			50			50			ns
Setup and hold time															ns
t_{AW} Setup time	Write	Address	200			150			200			100			
t_{DW} Setup time	Rise of R/$\overline{W}$	Data in	800			330			450			300			
t_{DH} Hold time	Change of data in	Rise of R/$\overline{W}$	100			100			100			50			
t_{CW} Setup time	Write	Chip enable	900			400			550			300			

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of these or any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient (B package).
3. Typical values are at +25°C and typical supply voltages.
4. All inputs protected against static charge.
5. Parameter valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.

TIMING DIAGRAMS





OBJECTIVE SPECIFICATION

2115/2115L-F,I,N • 2125/2125L-F,I,N

DESCRIPTION

The 2115 and 2125 family are read/write RAMs which are designed for buffer control storage and high performance main memory applications.

These devices offer the advantages of high performance, low power dissipation, and system cost savings, making them ideal where cost is a prime factor. N-channel technology allows the design and production of high speed MOS RAMs which are compatible to the performance of Bipolar RAMs.

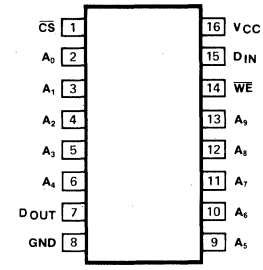
FEATURES

- **Power dissipation: 0.2mW/bit typ (2115L, 2125L)**
- **Output options:**
  2115: Uncommitted collector*
  2125: Three-state
- **Non-inverting data output**
- **Dual-in-line package**
- **N-channel MOS silicon gate technology**
- **Fully pin compatible to 93415 (2115) and 93425 (2125)**
- **Fully compatible with TTL logic families including inputs, output and single 5V supply**

* The 2115 is an MOS device and the output is actually an uncommitted drain.

PIN CONFIGURATION

F,I,N PACKAGE



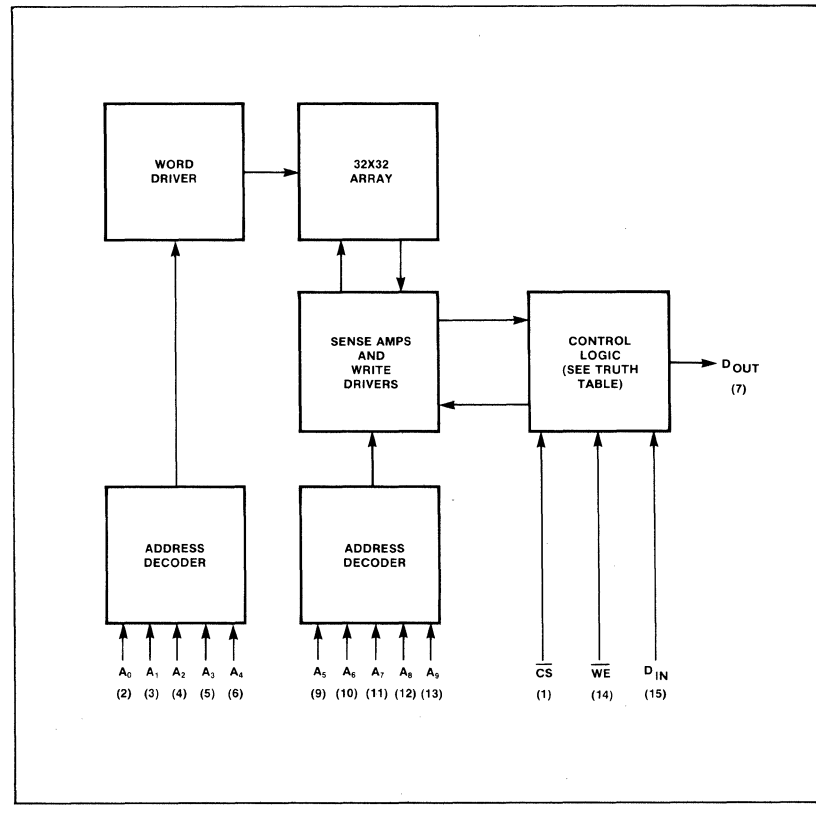
TRUTH TABLE

INPUTS			OUTPUT 2115 FAMILY	OUTPUT 2125 FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	High Z	Not selected
L	L	L	H	High Z	Write "0"
L	L	H	H	High Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

PIN DESIGNATION

PIN NO.	SYMBOL	FUNCTION
1	$\overline{CS}$	Chip select
2-6, 9-13	A_{0-9}	Address inputs
7	D_{OUT}	Data output
8	GND	Ground
14	$\overline{WE}$	Write enable
15	D_{IN}	Data input

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	-10 to 85	
T_{STG}	Storage	-65 to 150	
	All output or supply voltages	-0.5 to 7	V
	All input voltages	-0.5 to 5.5	V
	Dc output current	20	mA

DC ELECTRICAL CHARACTERISTICS[2] $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $75°C$

PARAMETER		TEST CONDITIONS	2115/2115L			2125/2125L			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.1			2.1			
	Output voltage								V
V_{OL}	Low	I_{OL} = 16mA			0.45			0.45	
V_{OH}	High	I_{OH} = -3.2mA	2.4			2.4			
	Input current	V_{CC} = Max							μA
I_{IL}	Low	V_{IN} = 0.4V		-1	-40		-1	-40	
I_{IH}	High	V_{IN} = 4.5V		1	40		1	40	
	Output current	V_{CC} = Max							
I_{CEX}	Leakage	V_{OUT} = 4.5V		10	100				μA
I_{OFF}	High Z	V_{OUT} = 0.5V/2.4V					10	50	μA
I_{OS}[3]	Short circuit	V_{CC} = 4.5V						-100	mA
	Supply current	All inputs grounded, output open							mA
I_{CCL}	2115L, 2125L			50	65		50	65	
I_{CC1}	2115, 2125			75	100		75	100	
	Capacitance	All inputs = OV, Output open							pF
C_{IN}	Input			4	8		4	8	
C_{OUT}	Output	$\overline{CS}$ = 5V		5	8		5	8	

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to $75°C$

PARAMETER		TO	FROM	2115/2125			2115L/2125L			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ CYCLE									
t_{ACS}	Chip select time			5		45	5		50	ns
t_{RCS}	Chip select recovery time					40			40	ns
t_{AA}	Access time	Output	Address		75	95		75	95	ns
t_{OH}	Previous read data valid after change of address			10			10			ns
	WRITE CYCLE									
	Enable time									ns
t_{WS}		Write enable	Data out							
t_{ZWS}	(2125, 2125L)	High Z	Write enable			40			40	
t_{WR}	Write recovery time			5		45	5		50	ns
t_W	Write pulse width			50			50			ns
	Setup and hold time									ns
t_{WSD}	Setup time prior to write	$\overline{WE}$	Data							
t_{WHD}	Hold time after write	Data	$\overline{WE}$	5			15			
t_{WSA}	Setup time	$\overline{WE}$	Address	30			30			
t_{WHA}	Hold time	Address	$\overline{WE}$	5			15			
t_{WSCS}	Setup time	$\overline{WE}$	Chip select							
t_{WHCS}	Hold time	Chip select	$\overline{WE}$	5			15			

NOTES on following page.

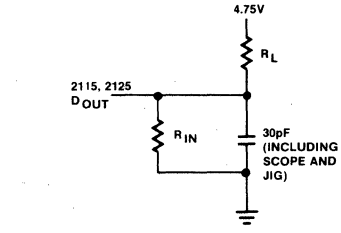
NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2 minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (@ 400fpm air flow) = 45°C/W
   θ_{JA} (still air) = 60°C/W
   θ_{JC} = 25°C/W.
3. Duration of short circuit current should not exceed 1sec.

TEST LOAD CIRCUITS

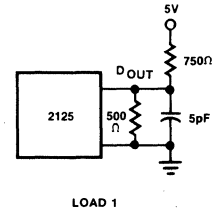
2115/2125

AC AND DC LOADING CONDITIONS



	2115	2125
R_L	330Ω	330Ω
R_{IN}	600Ω	300Ω

2125

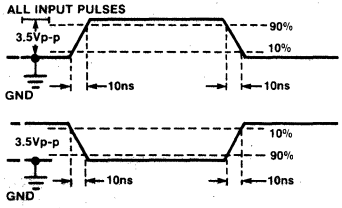


LOAD 1

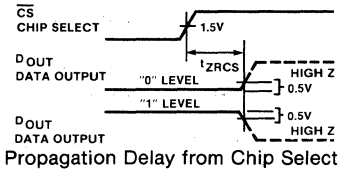
Write Enable to High Z Delay

VOLTAGE WAVEFORMS

2115/2125



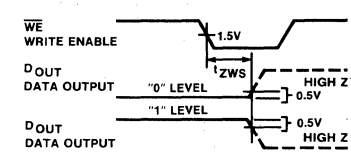
2125



Propagation Delay from Chip Select to High Z

All tzxxx parameters are measured at a delta of 0.5V from the logic level and using Load 1.

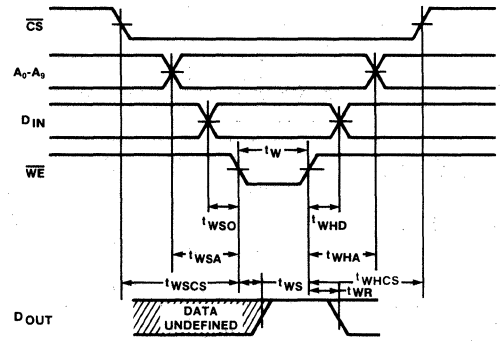
2125



Write Enable to High Z Delay

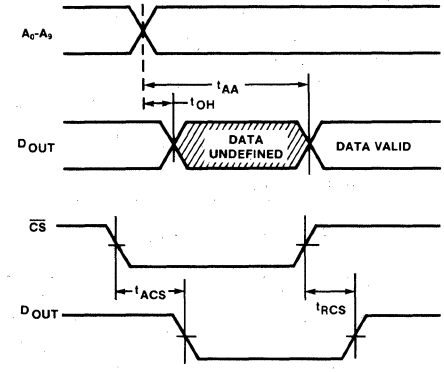
TIMING DIAGRAMS

2115 WRITE CYCLE



All measurements referenced to 1.5V

2115 READ CYCLE

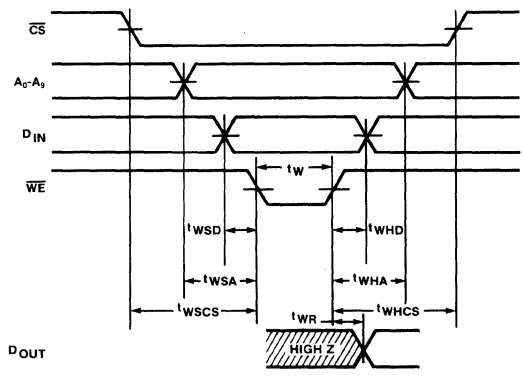


Propagation Delay from Chip Select

All measurements referenced to 1.5V

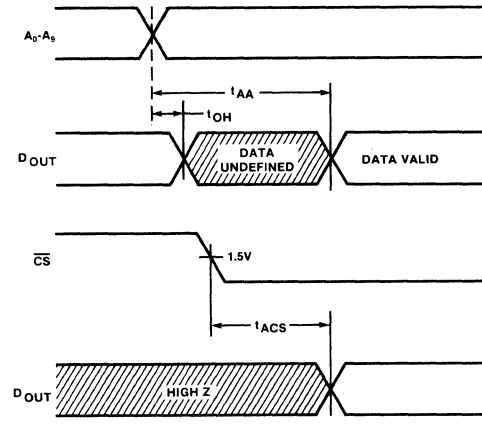
TIMING DIAGRAMS (Cont'd)

2125 WRITE CYCLE



All measurements referenced to 1.5V

2125 READ CYCLE

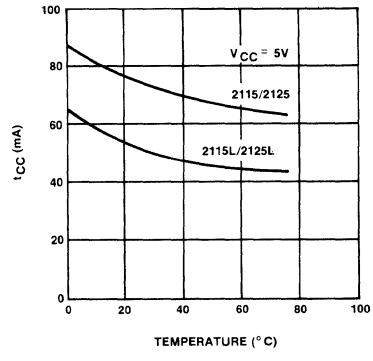


Propagation Delay from Chip Select

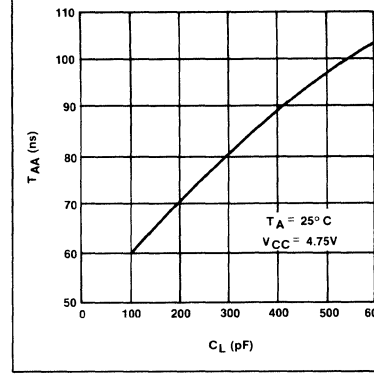
All measurements referenced to 1.5V

TYPICAL PERFORMANCE CHARACTERISTICS

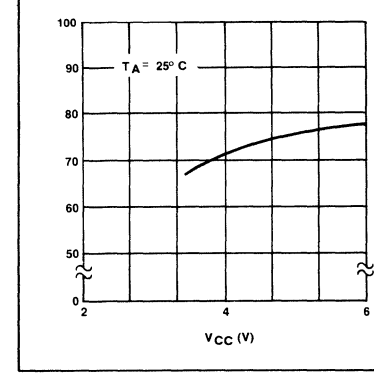
ICC vs TEMPERATURE



ACCESS TIME vs CAPACITANCE



ICC vs VCC

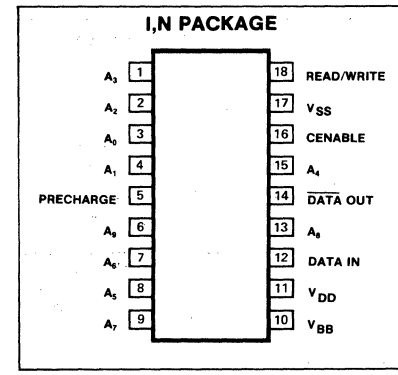


DESCRIPTION

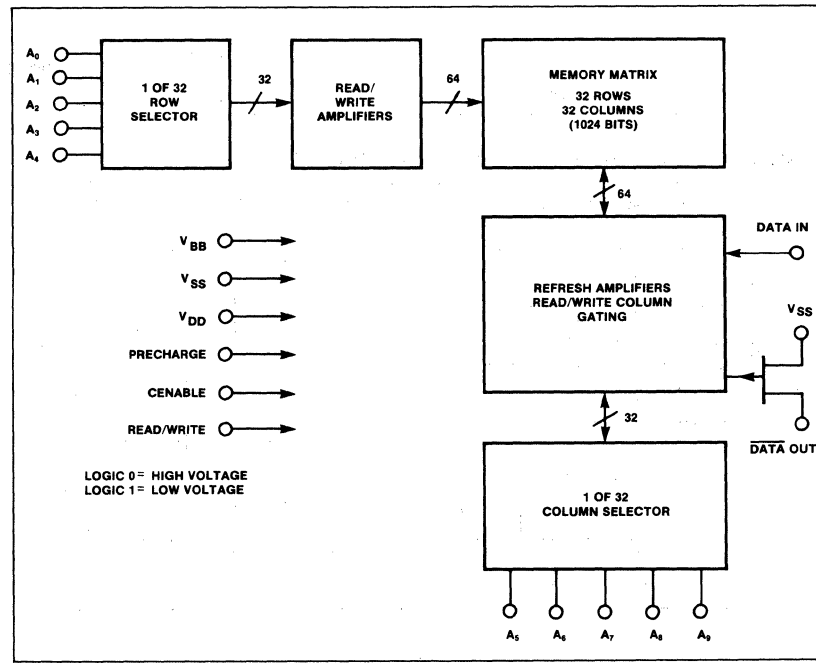
The 1103 is designed for main memory applications where high performance, low cost and large bit storage are important design objectives. It is a random access memory element using enhancement mode p-channel MOS devices integrated on a monolithic array. It is fully decoded, permitting the use of an 18-pin dual in-line package. The dynamic circuitry dissipates significant power only during precharge. Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every 2ms. A separate cenable (chip enable) lead allows easy selection of an individual package when outputs are OR-tied. Use Signetics 8T25 sense amp, and 3207 clock driver.

PIN CONFIGURATION

I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1	W
	All input or output voltages with respect to the most positive supply voltage, V_{BB}	-25 to 0.3	V
	Supply voltages V_{DD} and V_{SS} with respect to V_{BB}	-25 to 0.3	V

1103-I,N

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS}[2] = 16V ± 5%, (V_{BB} - V_{SS})[3] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
	Low					
V_{IL1}[4]	All address and data in lines	T_A = 0°C	V_{SS} - 17		V_{SS} - 14.2	
V_{IL2}[4]	All address and data in lines	T_A = 70°C	V_{SS} - 17		V_{SS} - 14.5	
V_{IL3}[4,5]	Precharge, Cenable, Read/write inputs	T_A = 0°C	V_{SS} - 17		V_{SS} - 14.7	
V_{IL4}[4,5]	Precharge, Cenable, Read/write inputs	T_A = 70°C	V_{SS} - 17		V_{SS} - 15.0	
	High[4]					
V_{IH1}	All inputs	T_A = 0°C	V_{SS} - 1		V_{SS} + 1	
V_{IH2}	All inputs	T_A = 70°C	V_{SS} - 0.7		V_{SS} + 1	
	Output voltage	R_{LOAD} = 100Ω[6]				mV
V_{OL}	Low[7]					
	High					
V_{OH1}		T_A = 25°C	60	90	400	
V_{OH2}		T_A = 70°C	50	80	400	
	Supply current	T_A = 25°C, All addresses = 0V, Precharge = 0V				mA
I_{DD1}	During T_{PC}[8]	Cenable = V_{SS}		37	56	
I_{DD2}	During T_{OV}[8]	Cenable = 0V		38	59	
I_{DD3}	During T_{POV}[8]	Cenable = 0V		5.5	11	
I_{DD4}	During T_{CP}[8]	Cenable = V_{SS}		3	4	
I_{DDAV}	Average[9]	Cycle time = 580ns, Precharge width = 190ns		17	25	
I_{BB}	V_{BB} supply current				100	μA
	Output current	R_{LOAD} = 100Ω[6]				μA
	High					
I_{OH1}		T_A = 25°C	600	900	4000	
I_{OH2}		T_A = 70°C	500	800	4000	
	Capacitance[10]	f = 1MHz, All unused pins are at ac ground, V_{IN} = V_{SS}				pF
C_{AD}	Address				7	
C_{PR}	Precharge				18	
C_{CE}	Cenable				18	
C_{RW}	Read/write				15	
	Data input					
C_{IN1}		Cenable = 0V			5	
C_{IN2}		Cenable = V_{SS}			4	
	Data output					
C_{OUT}		V_{OUT} = 0V			3	

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{SS} = 16 \pm 5\%$, $(V_{BB} - V_{SS}) = 3.0V$ to $4.0V$, $V_{DD} = 0V$

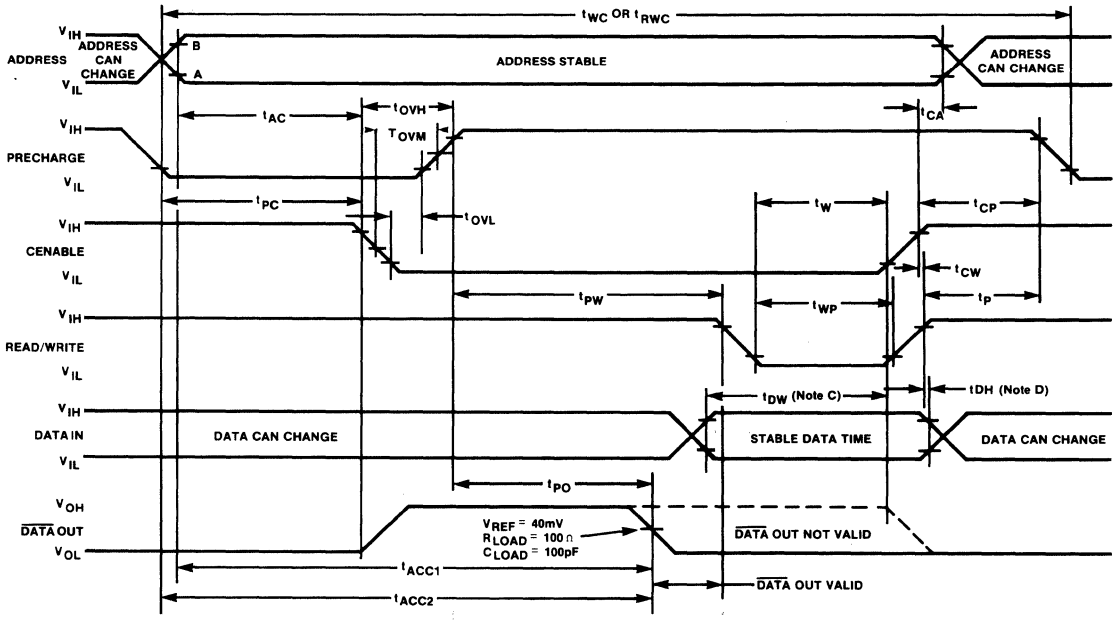
PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
READ, WRITE AND READ/WRITE CYCLE								
T_{REF}	Time between refresh						2	ms
	Setup and hold time							ns
t_{AC}	Setup time[11]	Cenable	Address		115			
t_{CA}	Hold time	Address	Cenable		20			
	Delay time							ns
t_{PC}[11]		Cenable	Precharge		125			
t_{CP}		Precharge	Cenable		85			
	Precharge and cenable overlap			t = 20ns				ns
t_{OVL}	Low				25		75	
t_{OVH}	High						140	
t_{OVM}	50% points				45		95	
	READ CYCLE			$t_{AC(min)} + t_{OVL(min} + t_{PO(max)} =$ $2t, t_{PC(min)} + t_{OVL(min)} + t_{PO(max)}$ $+ 2t$, t = 20ns, C_{LOAD} = 100pF, R_{LOAD} = 100, V_{REF} = 40mV				
t_{RC}	Read cycle[11]				480			ns
	Delay time							ns
t_{POV}		End of cenable	Precharge		165		500	
t_{PO}		Output	End of precharge				120	
	Access time[11]							ns
t_{ACC1}		Output	Address		300			
t_{ACC2}		Output	Precharge		310			
WRITE OR READ/WRITE CYCLE				$C_{LOAD} = 100pF$, $R_{LOAD} = 100$, $V_{REF} = 40mW$				
t_{WC}	Write cycle[11]			t = 20ns	580			ns
t_{RWC}	Read/write cycle[11]			t = 20ns	580			ns
	Delay time							ns
t_{PW}		Read/write	Precharge		165		500	
t_{PO}		Output	End of precharge				120	
	Setup and hold time							ns
t_W	Setup time	Chip enable high	Read/write		80			
t_{DW}	Setup time	Chip enable high	Data		105			
t_{DH}	Hold time	Data	R/W high		10			
t_{CW}	Hold time	R/W high	Chip enable high				10	
t_{WP}	Read/write pulse width				50			ns
t_P	Time to next precharge				0			ns

NOTES

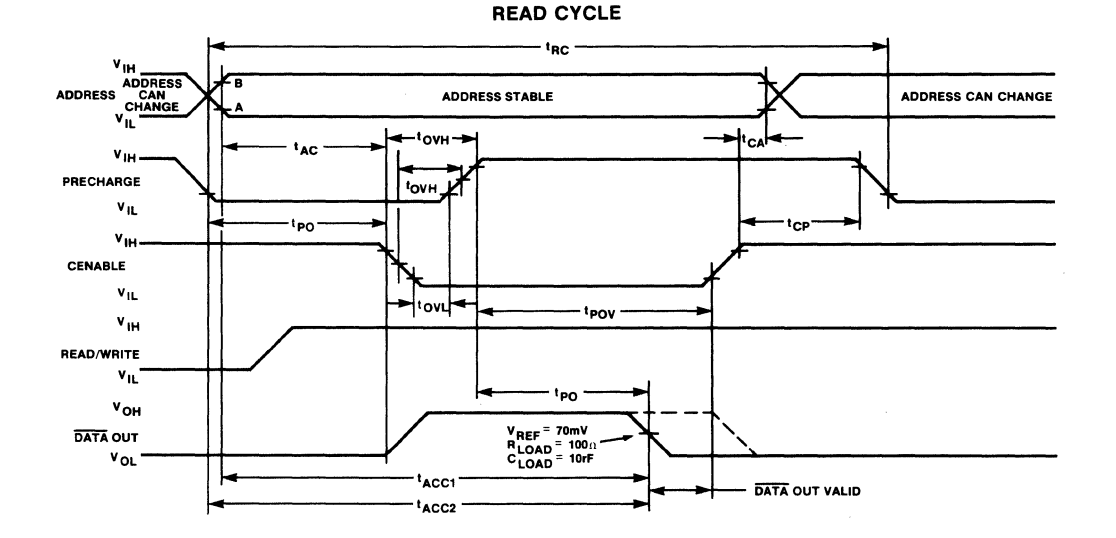
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$.
3. $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.
4. The maximum values for V_{IL} and the minimum values for V_{IH} are linearly related to temperature between 0°C and 70°C. Thus any value in between 0°C and 70°C can be calculated by using a straight-line relationship.
5. The maximum values for V_{IL} (for precharge, cenable and read/write) may be increased to V_{SS} - 14.2 at 0°C and V_{SS} - 14.5 at 70°C (same values as those specified for the address and data-in lines) with a 40ns degradation (worst case) in t_{AC}, t_{PC}, t_{RC}, t_{WC}, t_{RWC}, t_{ACC1} and t_{ACC2}.
6. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1kΩ.
7. The output current when reading a low output is the leakage current of the 1103 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
8. See Supply Current vs Temperature for guaranteed current at the temperature extremes. These values are taken from a single pulse measurement.
9. This parameter is periodically sampled and is not 100% tested.
10. This parameter is periodically sampled and is not 100% tested. It is measured at worst case operating conditions. Capacitance measurements for plastic package only.
11. These times will degrade by 40ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS} - 14.2V at 0°C and V_{SS} - 14.5V at 70°C.

TIMING DIAGRAMS

WRITE CYCLE OF READ/WRITE CYCLE



READ CYCLE



NOTES

A. V_{DD} + 2V
B. V_{SS} - 2V
t_T is defined as the transitions between these two points.
C. t_{DW} is referenced to point 1 of the rising edge of cenable of read/write whichever occurs first.
D. t_{DH} is referenced to point 2 of the rising edge of cenable or read/write whichever occurs first.

2660-F,I,N • 2660-1 - F,I,N • 2660-2 - F,I,N • 2660-3 - F,I,N

DESCRIPTION

The 2660 is fabricated with n-channel silicon gate technology for high performance and high functional density, and uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2660 allows it to be packaged in the industry standard 16-pin in-line package, which provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16-pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2660 on 6 address input pins. The two 6-bit address words are latched into the device by the 2 TTL clocks, Row Address Strobe (RAS) and Column Address Strobe (CAS). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

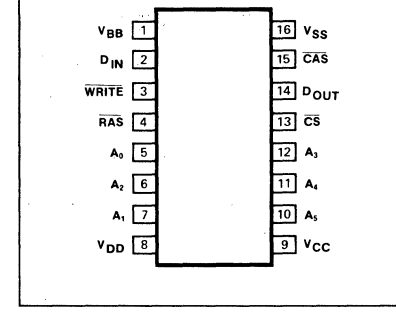
The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention, and this is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2ms.

FEATURES

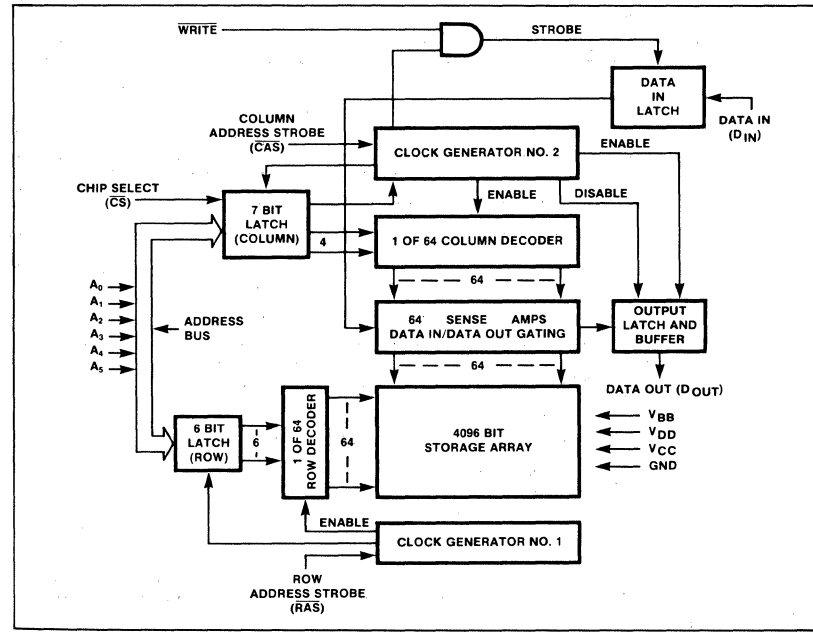
- **Standard 16-pin DIP**
- **All inputs including clocks TTL compatible**
- **On chip latches for address, chip select and data in**
- **Tri-state TTL compatible output**
- **Output data is latched and valid into next cycle**
- **Read and write cycle time:**
  - **2660: 375ns**
  - **2660-1: 425ns**
  - **2660-2: 500ns**
  - **2660-3: 375ns**
- **Access time:**
  - **2660: 250ns**
  - **2660-1: 300ns**
  - **2660-2: 350ns**
  - **2660-3: 250ns**
- **Low power:**
  - **Operating: <380mW**
  - **Standby: <24mW**
- **RAS only refresh (no dummy cycles required)**
- **Page mode addressing: 2660-3**
- **±10% power supply margins: 2660-3**
- **TRPW = $\overline{RAS}$ pulse width of 32μs: 2660-3**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_{STG}	Storage	-55 to 150	
	All input or output voltages with respect to the most negative supply voltage V_{BB}	+25 to -.5	V
	Supply voltages V_{DD}, V_{CC} and V_{SS} with respect to V_{BB}	+20 to -.5	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD}[2] = 12V ± 5% (10%), V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = OV unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[3]	Any input				V
V_{IL}	Low		-1.0		0.8	
V_{IH}	High		2.4		7.0	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA	0.0		0.4	
V_{OH}	High	I_{OH} = -5.0mA	2.4		V_{CC}	
	Leakage current	Any input				μA
I_{IL}	Input[4]				5	
I_{OL}	Output[5]				10	
	V_{DD} current					mA
I_{DD1}	Average[6]				35	
I_{DD2}	Supply	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}		1	1.5	
I_{CC}	V_{CC} supply current[7]	Deselected			10	μA
I_{BB}	Average V_{BB} current				75	μA
	Capacitance					pF
C_{AD}	Address				10	
C_C	$\overline{CAS}$,$\overline{RAS}$,$\overline{CS}$,DIN,$\overline{WRITE}$				7	
C_{OUT}	Output				8	

AC ELECTRICAL CHARACTERISTICS[8]

T_A = 0°C to 70°C, V_{DD}[2] = 12V ± 5% (10%), V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise specified.

	PARAMETER	TO	FROM	2660			2660-1			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ, WRITE AND READ MODIFY WRITE CYCLES									
t_{REF}	Time between refresh					2			2	ms
t_{RP}	$\overline{RAS}$ precharge time			115			125			ns
t_{CP}	Column precharge time									ns
	Lead time									ns
t_{RCL}	Leading edge[9]	$\overline{CAS}$	$\overline{RAS}$	60		110	80		135	
t_{CRL}	Trailing edge[10]			-40		40	-50		50	
	Access time									ns
t_{CAC}[11]		Output	$\overline{CAS}$			140			165	
t_{RAC}[12]		Output	$\overline{RAS}$			250			300	
t_T	Rise and fall time[13]			3		50	3		50	ns
t_{OFF}	Output buffer turnoff delay			0		65	0		80	ns
	Setup and hold time									ns
t_{AS}	Setup time	$\overline{CAS}$	Address or $\overline{CS}$	0			0			
t_{AH}	Hold time	Address or $\overline{CS}$	$\overline{CAS}$	60			80			
	READ CYCLE									
t_{RC}	Random read cycle time[12,14]			375			425			ns
	Pulse width									ns
t_{CPW}	$\overline{CAS}$			140		10000	165		10000	
t_{RPW}	$\overline{RAS}$			250		10000	300		10000	
	Setup and hold time									ns
t_{RCS}	Setup time	$\overline{CAS}$ low	$\overline{WE}$ high	0			0			
t_{RCH}	Hold time	$\overline{WE}$ low	$\overline{CAS}$ high							
t_{RSH}	Hold time	$\overline{RAS}$ high	$\overline{CAS}$ low	140			165			
t_{CSH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	210			250			
	WRITE CYCLE									
t_{RC}	Random write cycle time[12,14]			375			425			ns
	Pulse width									ns
t_{CPW}	$\overline{CAS}$			140		10000	165		10000	
t_{RPW}	$\overline{RAS}$			250		10000	300		10000	
t_{WP}	Write command			110			130			
	Setup and hold time									ns
t_{DS}	Setup time[15]	$\overline{CAS}$	Data in	0			0			
t_{DH}	Hold time[15]	Data in	$\overline{CAS}$	110			130			
t_{RSH}	Hold time	$\overline{RAS}$ high	$\overline{CAS}$ low	140			165			
t_{CSH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	210			250			
t_{WCH}	Hold time[16]	$\overline{WE}$ high	$\overline{CAS}$ low	110			130			
t_{CWL}	Lead time	$\overline{CAS}$ high	$\overline{WE}$ low	110			130			ns
	READ MODIFY WRITE CYCLE									
t_{RMW}	Read modify write cycle time[12,14]			475		10000	555	10000		ns
	Cycle width									ns
t_{CRW}	$\overline{CAS}$			250		10000	295	10000		
t_{RRW}	$\overline{RAS}$			360		10000	430	10000		
	Pulse width									ns
t_{WP}	Write command			110			130			
	Setup and hold time									ns
t_{DS}	Setup time	$\overline{CAS}$	Data in	0			0			
t_{DH}	Hold time	Data in	$\overline{CAS}$	110			130			
t_{RCS}	Setup time	$\overline{CAS}$ low	$\overline{WE}$ high	0			0			
t_{RWH}	Hold time	$\overline{RAS}$ high	$\overline{WE}$ low	110			130			
t_{CWH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	360			430			
t_{CWL}	Lead time	$\overline{CAS}$ high	$\overline{WE}$ low	110			130			ns
t_{MOD}	Modify time	$\overline{WE}$ low	Data out	0			0			ns

AC ELECTRICAL CHARACTERISTICS[8]

(Cont'd) $T_A = 0°C$ to $70°C$, V_{DD}[2] = 12V ± 5% (10%), V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise specified.

PARAMETER		TO	FROM	2660-2			2660-3			UNIT
				Min	Typ	Max	Min	Typ	Max	
	READ, WRITE AND READ MODIFY WRITE CYCLES									
t_{REF}	Time between refresh					2			2	ms
t_{RP}	$\overline{RAS}$ precharge time			150			115			ns
t_{CP}	Column precharge time						110			ns
	Lead time									ns
t_{RCL}	Leading edge[9]	$\overline{CAS}$	$\overline{RAS}$	110		150	60		110	
t_{CRL}	Trailing edge[10]			-50		50	-40		40	
	Access time									ns
t_{CAC}[11]		Output	$\overline{CAS}$			200			140	
t_{RAC}[12]		Output	$\overline{RAS}$			350			250	
t_T	Rise and fall time[13]			3		50	3		50	ns
t_{OFF}	Output buffer turnoff delay			0		100	0		65	ns
	Setup and hold time									ns
t_{AS}	Setup time	$\overline{CAS}$	$\overline{Address}$ or $\overline{CS}$	0			0			
t_{AH}	Hold time	Address or $\overline{CS}$	CAS	100			60			
	READ CYCLE									
t_{RC}	Random read cycle time[12,14]			500			375			ns
	Pulse width									ns
t_{CPW}	$\overline{CAS}$			200		10000	140		32000	
t_{RPW}	$\overline{RAS}$			350		10000	250		32000	
	Setup and hold time									ns
t_{RCS}	Setup time	$\overline{CAS}$ low	$\overline{WE}$ high	0			0			
t_{RCH}	Hold time	$\overline{WE}$ low	$\overline{CAS}$ high							
t_{RSH}	Hold time	$\overline{RAS}$ high	$\overline{CAS}$ low	200			140			
t_{CSH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	350			210			
	WRITE CYCLE									
t_{RC}	Random write cycle time[12,14]			500			375			ns
	Pulse width									ns
t_{CPW}	$\overline{CAS}$			200		10000	140		32000	
t_{RPW}	$\overline{RAS}$			350		10000	250		32000	
t_{WP}	Write command			150			110			
	Setup and hold time									ns
t_{DS}	Setup time[15]	$\overline{CAS}$	Data in	0			0			
t_{DH}	Hold time[15]	Data in	$\overline{CAS}$	150			110			
t_{RSH}	Hold time	$\overline{RAS}$ high	$\overline{CAS}$ low	200			140			
t_{CSH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	300			210			
t_{WCH}	Hold time[16]	$\overline{WE}$ high	$\overline{CAS}$ low	150			110			
t_{CWL}	Lead time	CAS high	$\overline{WE}$ low	150			110			ns
	READ MODIFY WRITE CYCLE									
t_{RMW}	Read modify write cycle time[12,14]			650		10000	475		32000	ns
	Cycle width									ns
t_{CRW}	$\overline{CAS}$			350		10000	250		32000	
t_{RRW}	$\overline{RAS}$			500		10000	360		32000	
	Pulse width									ns
t_{WP}	Write command			150			110			
	Setup and hold time									ns
t_{DS}	Setup time	$\overline{CAS}$	Data in	0			0			
t_{DH}	Hold time	Data in	$\overline{CAS}$	150			110			
t_{RCS}	Setup time	$\overline{CAS}$ low	$\overline{WE}$ high	0			0			
t_{RWH}	Hold time	$\overline{RAS}$ high	$\overline{WE}$ low	150			110			
t_{CWH}	Hold time	$\overline{CAS}$ high	$\overline{RAS}$ low	500			360			
t_{CWL}	Lead time	$\overline{CAS}$ high	$\overline{WE}$ low	150			110			ns
t_{MOD}	Modify time	$\overline{WE}$ low	Data out	0			0			ns

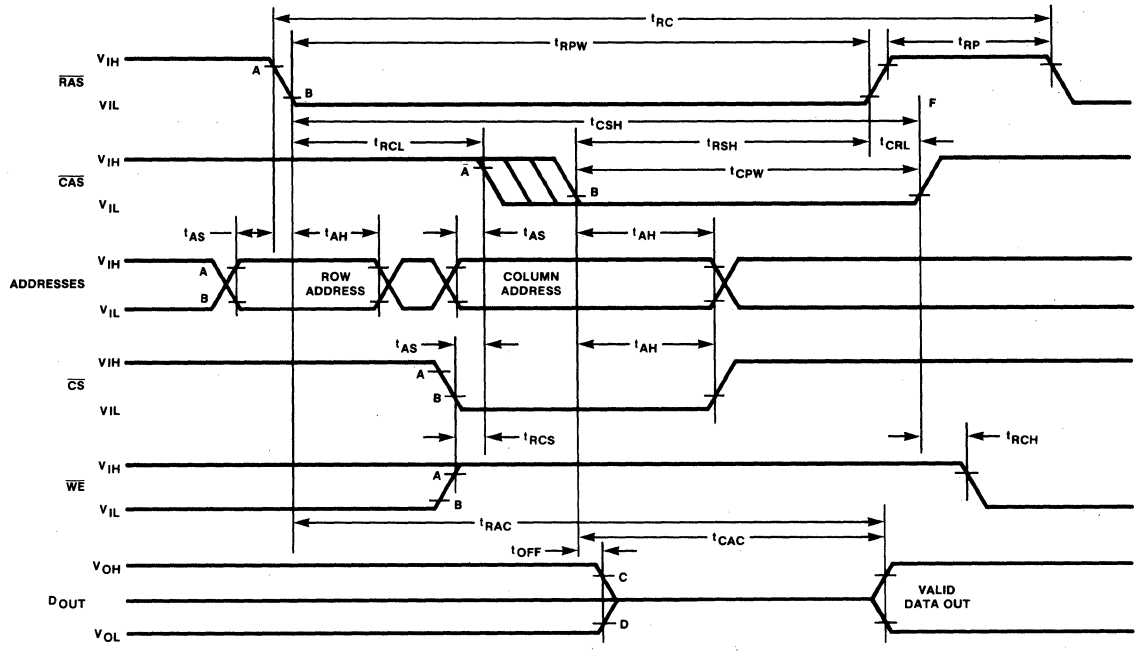
NOTES on following page.

NOTES

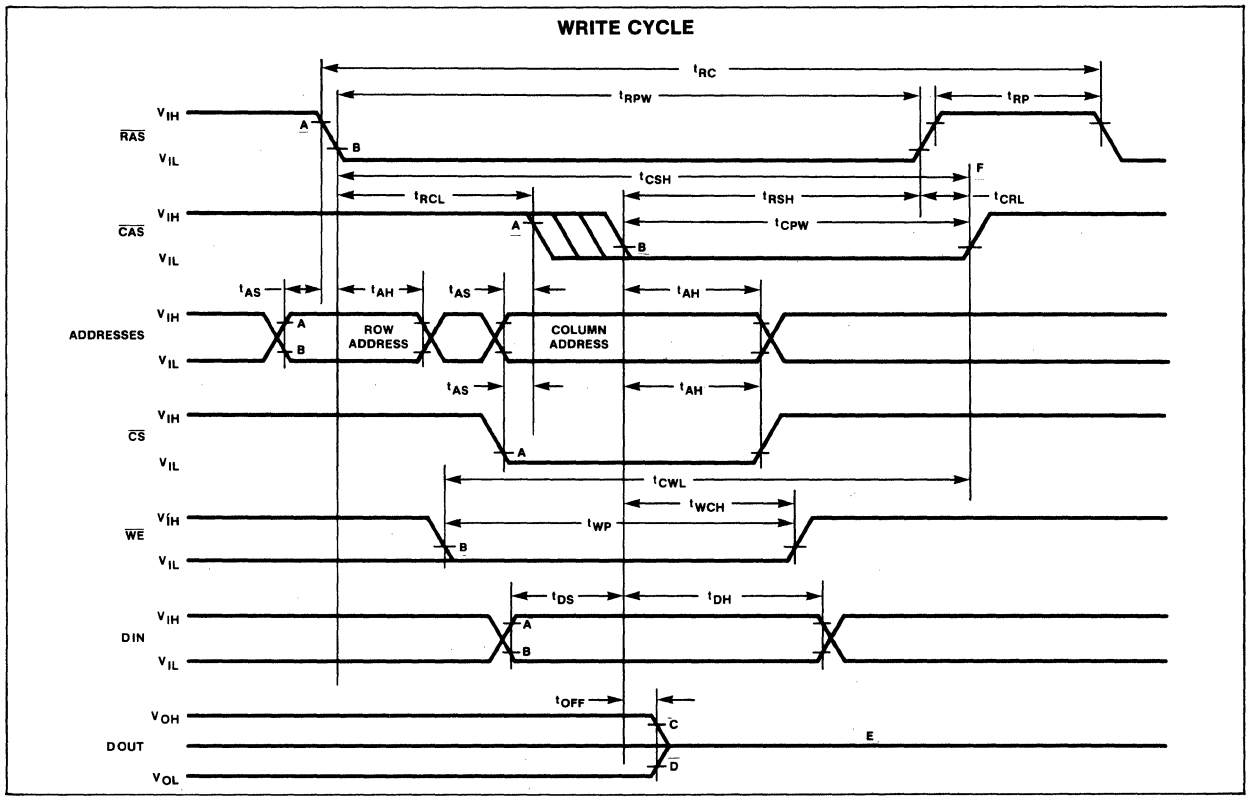
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. V_{DD} = 12 ± 10% for the 2660-3.
3. Input voltages greater than TTL levels (0 to 5V) require device operation at reduced speed.
4. All device pins at 0V except V_{BB} at -5V and pin under test which is at +10V.
5. Output disabled by chip select input.
6. Current is proportional to clock speed with maximum current measured at fastest cycle rate.
7. Depends upon output loading. The V_{CC} supply is connected to the output buffer only.
8. Assumes t_T = 5ns.
9. For minimum cycle, t_{RCL} has a maximum value of 110ns.
10. Implies $|t_{CRL}| \leq 40ns$ only for minimum cycle time; otherwise $|t_{CRL}| \gg 40ns$ is legal for other than minimum cycle time.
11. Assumes $t_{RCL} + t_T > t_{RCL}$ (max). If not, the access time is controlled by t_{RAC}.
12. Assumes that $t_{RCL} + t_T < t_{RCL}$ (max). If $t_{RCL} + t_T > t_{RCL}$ (max), then t_{RC} and t_{RAC} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).
13. Rise and fall times measured between V_{IH} and V_{IL}.
14. The minimum cycle time is achieved by compensating for RAS rise and fall times with t_{CRL}. The minimum cycle time is then constrained by t_{RCL} (max) + t_{CPW} + t_{RP}.
15. These parameters are referenced to the CAS leading edge in random write cycle operation and to the Write leading edge in read-write or read-modify-write cycle.
16. Write command hold time is important only when performing normal random write cycles. During read-write or read-modify-write cycles, the write command pulse width is the limiting parameter.
17. All voltages reference to V_{SS}.
18. Output voltage will swing from V_{SS} to V_{CC} independent of differential between V_{SS} and V_{CC}.

TIMING DIAGRAMS

READ CYCLE

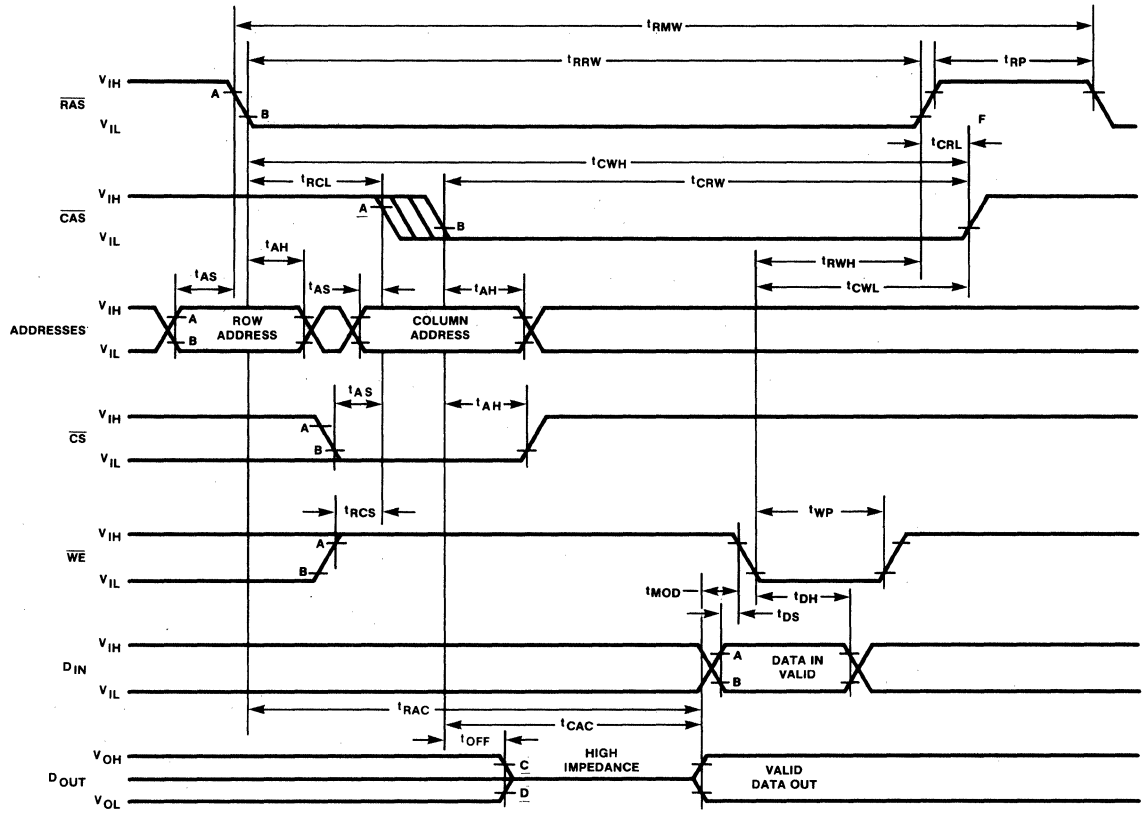


TIMING DIAGRAMS (Cont'd)



TIMING DIAGRAMS (Cont'd)

READ MODIFY WRITE CYCLE



NOTES

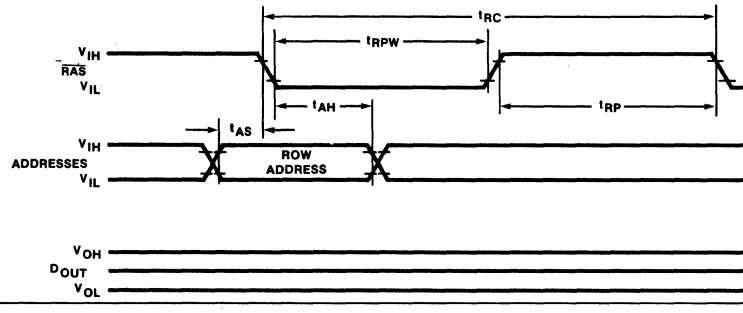
A,B. V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.

C,D. V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT} with 100pf load.

E. If $\overline{WE}$ goes low while $\overline{CAS}$ is low, D_{OUT} could go either V_{OL} or V_{OH} after t_{CAC}. D_{OUT} will be in open circuit state (write cycle waveforms), if $\overline{WE}$ goes Low before $\overline{CAS}$ goes low. In a read-modify-write cycle D_{OUT} is data read and does not change during modify-write portion of the cycle.

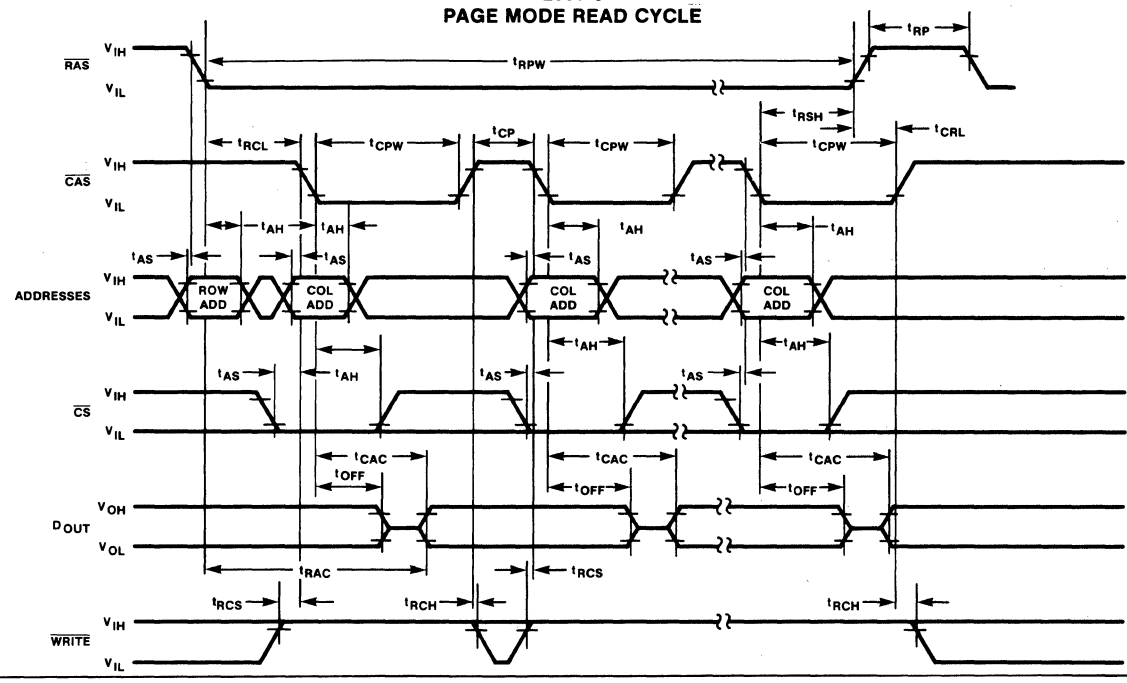
F. For minimum cycle timing, t_{CRL} must be 0 to 40ns for the 2660 and 2660-3; 0 to 50ns for the 2660-1 and 2660-2.

RAS ONLY REFRESH CYCLE

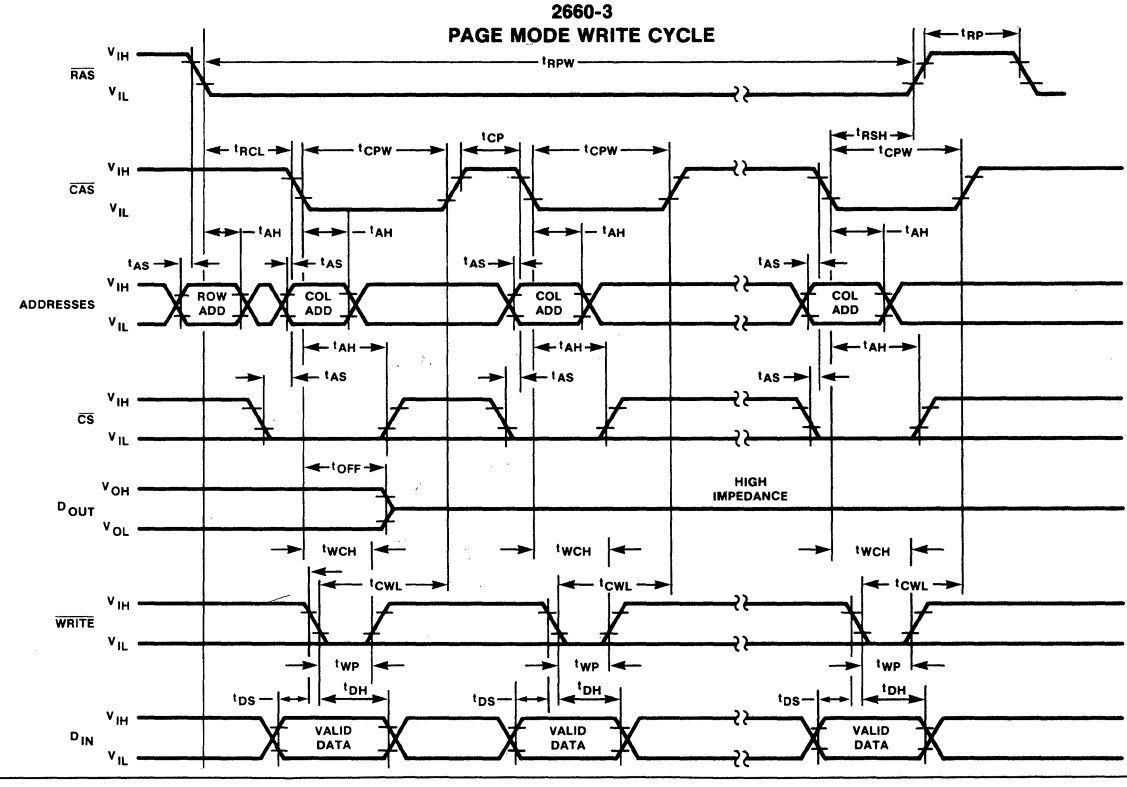


TIMING DIAGRAMS (Cont'd)

2660-3
PAGE MODE READ CYCLE



2660-3
PAGE MODE WRITE CYCLE



2680-F,I,N • 2680-1-F,I,N • 2680-2-F,I,N

DESCRIPTION

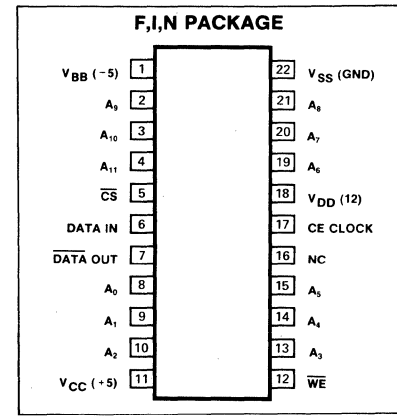
The 2680 incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The 2680 must be refreshed every 2ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A_0-A_5). The chip select input can be either high or low for refresh.

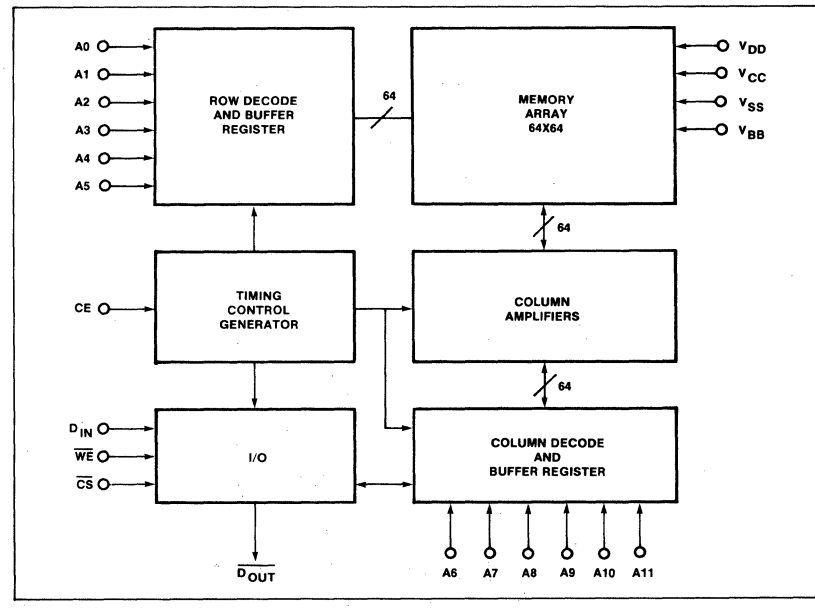
The 2680 has been designed with minimum production costs as a prime criterion. It is fabricated using n-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The 2680 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance and low cost memory device.

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating under bias	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation	1.25	W
	All input or output voltages with respect to the most negative supply voltage, V_{BB}	20 to -0.3	V
	Supply voltages V_{DD}, V_{CC}, and V_{SS} with respect to V_{BB}	20 to -0.3	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	LIMITS			UNIT
	Min	Typ	Max	
Supply voltage				V
V_{CC}	4.75	5	5.25	
V_{DD}	11.4	12	12.6	
V_{SS}		0		
V_{BB}	-4.5	-5	-5.5	

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		-1.0		0.6	
V_{IH}	High		2.4		V_{CC} +1	
V_{ILC}	CE low		-1.0		1.0	
V_{IHC}	CE high		V_{DD} -1		V_{DD} +1	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.0mA	0.0		0.45	
V_{OH}	High	I_{OH} = -2.0mA	2.4		V_{CC}	
	Input load current					μA
I_{LC}	CE	V_{IN} = 0 min to V_{IHC} max		.01	2	
I_{LI}	All inputs except CE	V_{IN} = 0 min to V_{IH} max, CE = V_{ILC} or V_{IHC}		.01	10	
$\|I_{LO}\|$	Output leakage current high impedance state	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = OV to 5.25V		.01	10	μA
	Supply current (V_{DD})					
I_{DD1}	During CE off[3]	CE = - 1V to 6V		50	200	μA
I_{DD2}	During CE on	CE = V_{IHC}, $\overline{CS}$ = V_{IL}			60	mA
I_{DDAV1}	Average V_{DD} current	Cycle time = 400ns, $\overline{CS}$ = V_{IL}, t_{CE} = 230ns, T_A = 25°C		35	54	mA
	Supply current					μA
I_{CC1}	V_{CC}[4]	CE = V_{ILC} or $\overline{CS}$ = V_{IH}		.01	10	
I_{BB}	V_{BB}			5	100	
	Capacitance[5]					pF
C_{AD}	Address, CS	V_{IN} = V_{SS}		4	6	
C_{CE}	CE	V_{IN} = V_{SS}		13	25	
C_{IN}	Input and $\overline{WE}$	V_{IN} = V_{SS}		5	10	
C_{OUT}	Output	V_{OUT} = OV		4	7	

AC ELECTRICAL CHARACTERISTICS

Over recommended supply voltage range, T_A = 0°C to 70°C, t_T = 20ns, C_L = 50pF, Load = 1 TTL gate, $t_{ACC} = t_{AC} + t_{CO} + 1t_T$

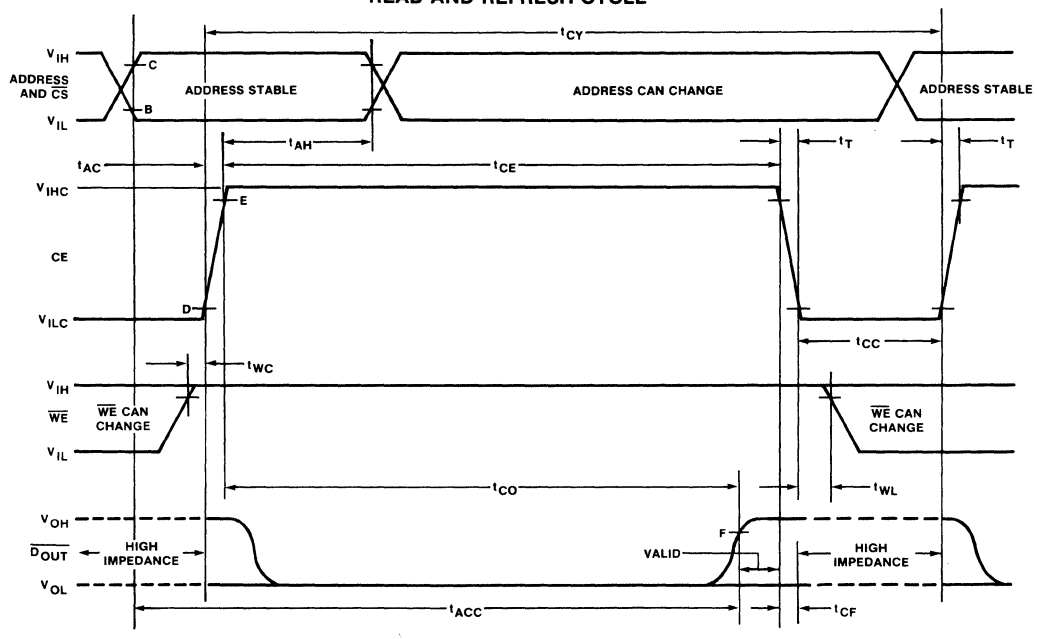
	PARAMETER	TO	FROM	2680			2680-1			2680-2			UNIT
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	READ, WRITE, AND READ MODIFY/ WRITE CYCLE												
t_{REF}	Time between refresh					2			2			1	ms
	Setup and hold time												ns
t_{AC}	Setup time	CE	Address	0			0			10			
t_{AH}	Hold time	Address	CE	100			100			100			
t_{CC}	CE off time			130			130			380			ns
t_T	CE transition time			10		40	10		40	10		40	ns
t_{CF}	CE high impedance state	Output	CE off	0			0			0			ns
	READ CYCLE												
t_{CY}	Cycle time			400			470			800			ns
t_{CE}	CE on time			230		4000	300		4000	380		4000	ns
t_{CO}	CE output delay time					180			250			320	ns
t_{ACC}	Access time	Output	Address			200			270			350	ns
t_{WL}		$\overline{WE}$	$\overline{CE}$	0			0			0			ns
t_{WC}		CE on	$\overline{WE}$	0			0			0			ns
	WRITE CYCLE												
t_{CY}	Cycle time			400			470			800			ns
t_{CE}	CE on time			230		4000	300		4000	380		4000	ns
t_W		CE off	$\overline{WE}$	150			150			200			ns
t_{CW}		$\overline{WE}$	CE	150			150			150			ns
	Setup and hold time												ns
t_{DW}	Setup time[6]	$\overline{WE}$	D_{IN}	0			0			0			
t_{DH}	Hold time	D_{IN}	CE	0			0			0			
	Pulse width												ns
t_{WP}	$\overline{WE}$			50			50			100			
	READ, MODIFY, WRITE CYCLE												
t_{RWC}	Cycle time			520			590			960			ns
t_{CRW}	CE width during cycle			350		4000	420		4000	540		4000	ns
t_W		CE off	$\overline{WE}$	150			150			200			ns
t_{WC}		CE on	$\overline{WE}$	0			0			0			ns
	Setup and hold time												ns
t_{DW}	Setup time	$\overline{WE}$	D_{IN}	0			0			0			
t_{DH}	Hold time	D_{IN}	CE	0			0			0			
	Pulse width												ns
t_{WP}	$\overline{WE}$			50			50			100			
t_{CO}	Delay time	Output	CE			180			250			320	ns
t_{ACC}	Access time					200			270			350	ns

NOTES

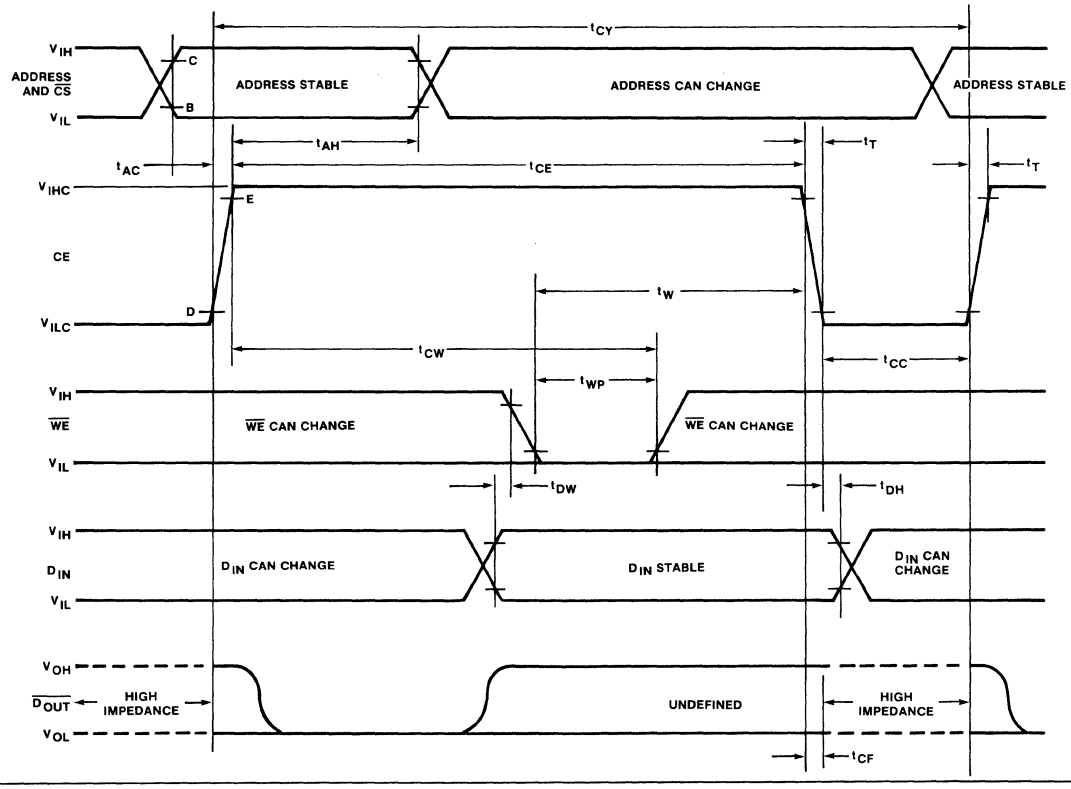
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading V_{CC} is connected to output buffer only.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation with the current equal to a constant 20mA.
6. If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.
7. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V more negative than V_{BB}.

TIMING DIAGRAMS

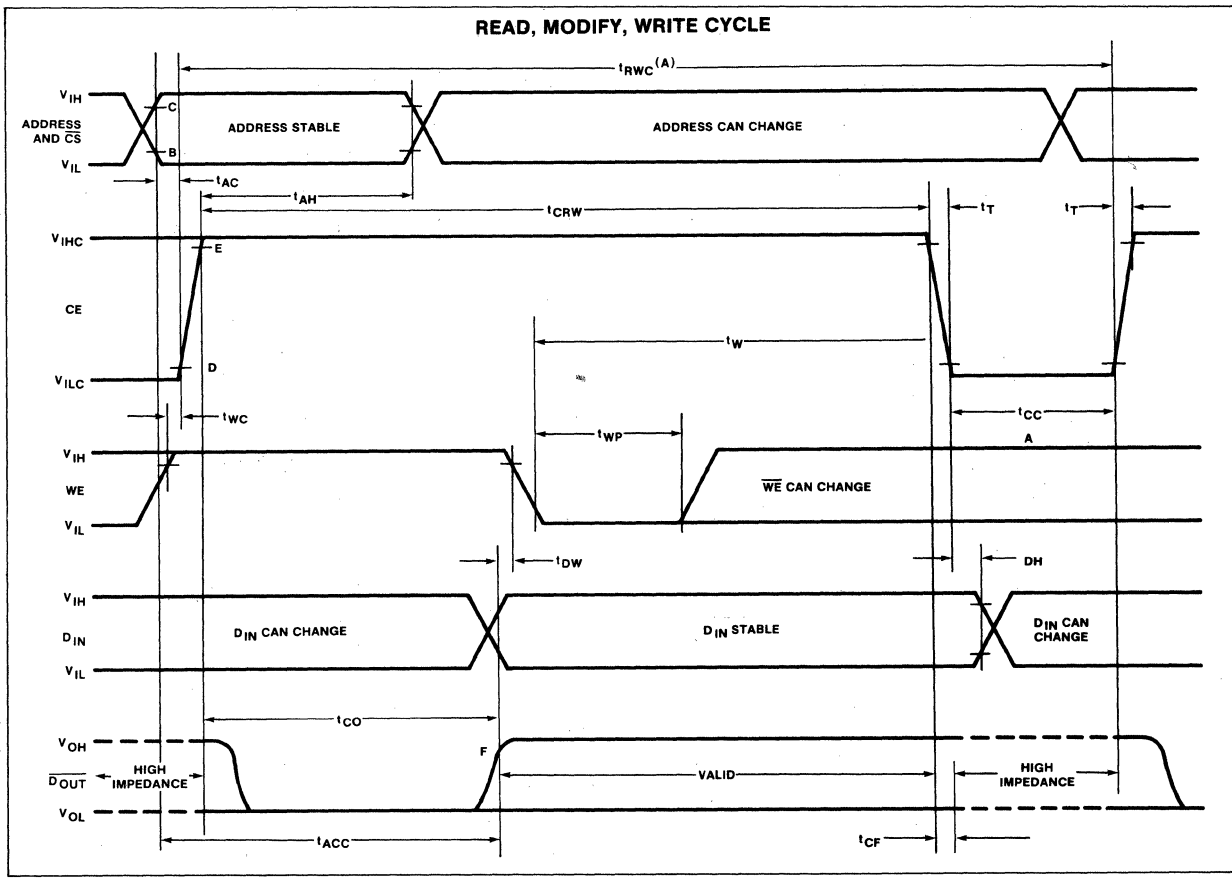
READ AND REFRESH CYCLE[A]



WRITE CYCLE



TIMING DIAGRAMS (Cont'd)



NOTES

A. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
B V_{IL} max is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
C. V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
D. V_{SS} +2.0V is the reference level for measuring timing of CE.
E. V_{DD} -2V is the reference level for measuring timing of CE.
F. V_{SS} +2.4V is the reference level for measuring the timing of D_{OUT}.

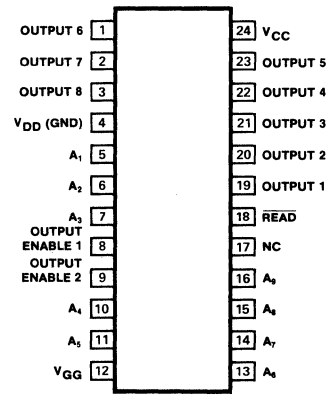
2530-I,N

DESCRIPTION

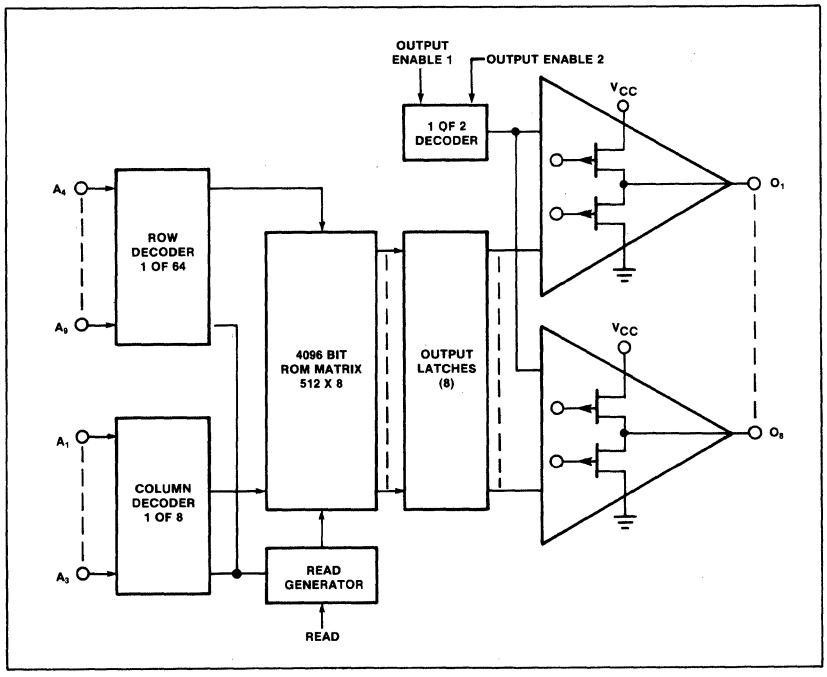
The 2530 has a read input which controls the entry of data from the ROM into output latches. Three-state outputs allow OR-tying for implementing larger memories. Two mask programmable output enables control the 8 output devices without affecting address circuitry.

PIN CONFIGURATION

I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to +150	
P_D	Power dissipation at 70°C[2]	730	mW
	Input and supply voltages with respect to V_{CC}[3]	+0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = 0V, V_{GG} = -12V ± 5%, unless otherwise specified.[4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[8]					V
V_{IL}	Low		-5		0.6	
V_{IH}	High		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.5	
V_{OH}	High	I_{OH} = 100μA	3.8			
I_{LI}	Input load current	V_{IN} = -5.5V, T_A = 25°C		10	500	nA
I_{LO}	Output leakage current	V_{OUT} = OV, T_A = 25°C		10	1000	nA
	Supply current[9]					mA
I_{CC}	V_{CC}			30	45	
I_{GG}	V_{GG}			30	45	
C_{IN}	Address input capacitance	V_{IN} = V_{CC}, V_{AC} = 25m p-p, f=1MHz			10	pF

AC ELECTRICAL CHARACTERISTICS

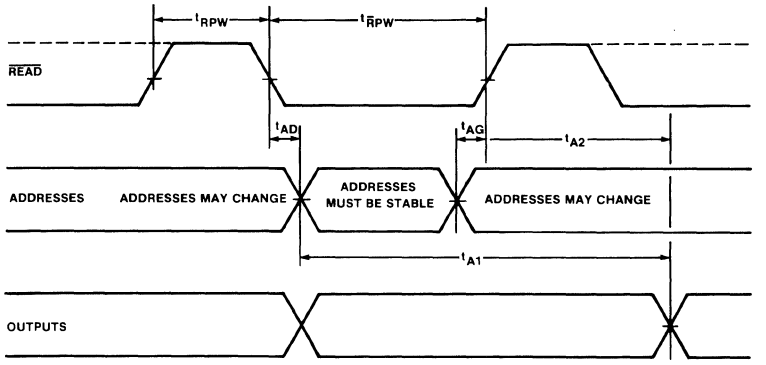
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = 0V, V_{GG} = -12V ± 5%, unless otherwise specified.

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Pulse width						ns
t_{RPW}	$\overline{\text{Read}}$[10]			250	200		
$t_{\overline{R}PW}$	Read[11]			500	400		
	Address time[12]						ns
t_{AD}	Delay	Address	$\overline{\text{Read}}$ low			50	
t_{AG}	Read	$\overline{\text{Read}}$ high	Address			50	
	Delay time						ns
t_{A1}[13]		Output	Address		625	700	
t_{A2}[13]		Output	End of read pulse		200	250	
t_{OE}		Output	Output enable		100	250	

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to 70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} -1.85V and V_{IL} = V_{CC} -4.15V.
9. Outputs open, t_{RPW} = 250ns, $t_{\overline{R}PW}$ = 500ns.
10. During $t_{\overline{R}PW1}$ addresses are decoded and sent to the memory matrix and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (rising edge) of the $\overline{\text{read}}$ pulse. After t_{A2} data appears at the output terminals.
11. During t_{RPW1} data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
12. Addresses must be stable within 50ns after the $\overline{\text{read}}$ line falls and must remain stable until at least 50ns before the $\overline{\text{read}}$ line goes high.
13. t_A = 0°C to +70°C.

TIMING DIAGRAM



All times measured from 50% points, for all input waveforms $t_r = t_f = 10ns$.

CUSTOM CODING INFORMATION

Data Card Format

HEADER CARD

Card No. 1

Columns	
1-5	2530N or 25301
6-14	Blank
15-19	CODED
20	Blank
21	Logic state of Output Enable #2, (CS2)-Most Significant Bit
22	Logic state of Output Enable #1
23	Blank
24-71	Customer company name
72	Blank
73-80	Date

I.D./ COMMENT CARDS

Card No. 1

Columns	
1	C
2	Blank
3-80	Person responsible for reviewing Signetics truth table and company name

Card No. 2

Columns	
1	C
2	Blank
3-80	Customer city, state, zip

DATA CARDS

Card No. 1

Columns	
1-3	Decimal address (blank, blank, 0)
4	Blank
5-12	8-digit binary output (MSB-left)*
13-20	Blank
21-33	Decimal address (blank, blank, 1)
24	Blank
25-32	8-digit binary output (MSB-left)*
33-40	Blank
41-43	Decimal address (blank, blank, 2)
44	Blank
45-52	8-digit binary output (MSB-left)*
53-60	Blank
61-63	Decimal address (blank, blank, 3)
64	Blank
65-72	8-digit binary output (MSB-left)*
73-80	Blank

Card No. 2

Same format as Card No. 1

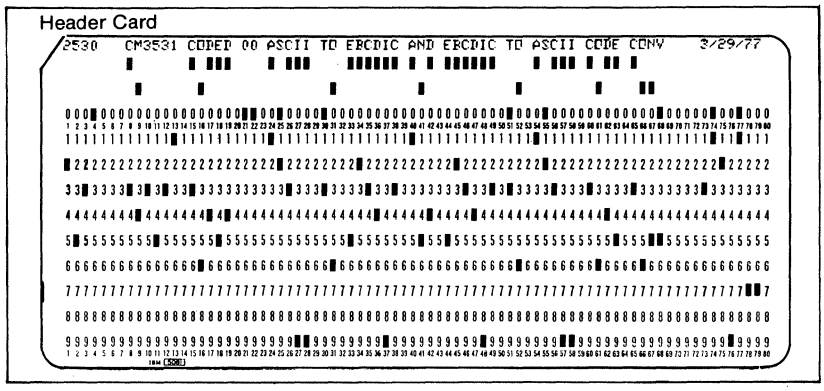
Card No. 128

128 Same format as Card No. 1

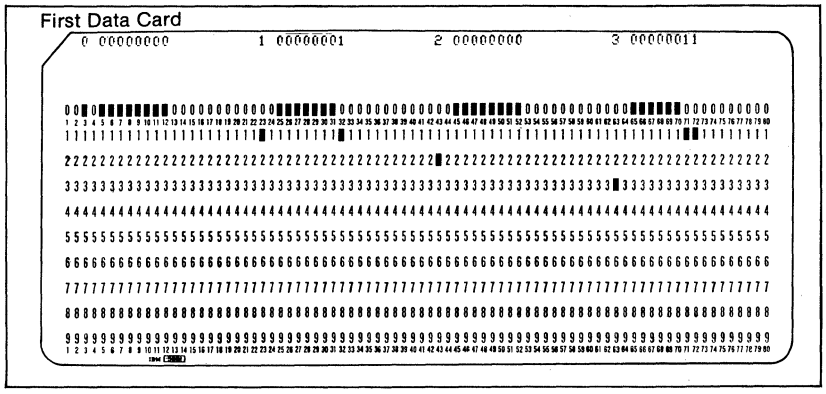
*MSB = O_9

EXAMPLES

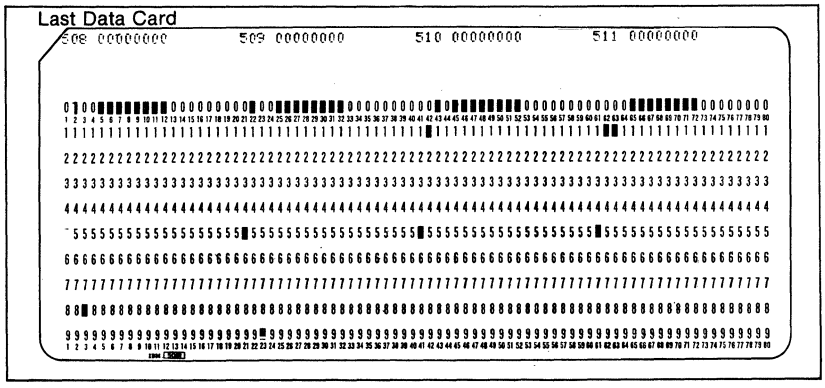
Header Card



First Data Card



Last Data Card



OBJECTIVE SPECIFICATION 2609-F,I,N

DESCRIPTION

The 2609 is a mask-programmable 8192-bit row select character generator. It contains 128 characters in a 7X9 matrix, and has the capability of shifting certain characters that normally extend below the baseline, such as j, y, g, p and q. Circuitry is supplied internally to effectively lower the whole matrix for this type of character, a feature previously requiring external circuitry.

A 7-bit address code is used to select 1 of the 128 available characters. Each character is defined as a specific combination of logic "1"s and "0"s stored in a 7X9 matrix. When a specific 4-bit binary row select code is applied, a word of 7 parallel bits appears at the output. The rows can be sequentially selected, providing a 9-word sequence of 7 parallel bits per word for each character selected by the address inputs. As the row select inputs are sequentially addressed, the devices will automatically place the 7X9 character in 1 of 2 pre-programmed positions on the 16-row matrix, with the positions defined by the 4 row select inputs.

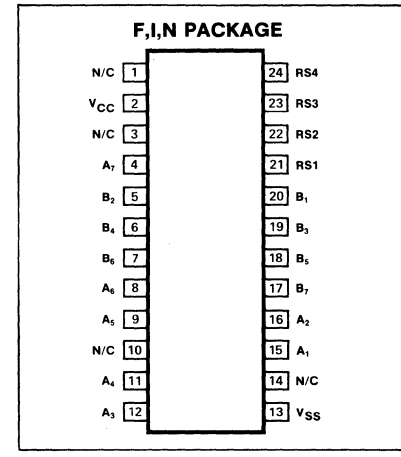
Complete TTL compatibility is provided, as well as direct interfacing with other NMOS devices, and with CMOS when using a +5V power supply. Maximum access time is 500ns; however, if a device is programmed without shifted characters, the access time is reduced.

FEATURES

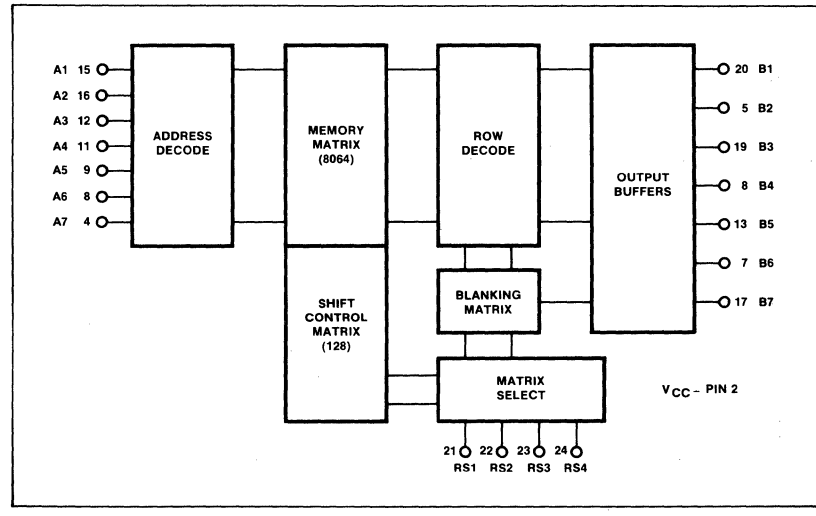
- **Static operation—no clocks**
- **Access time: 500ns max**
- **Single 5V power supply**
- **TTL compatible inputs and outputs**
- **Power dissipation: 525mW**
- **N-channel silicon gate technology**
- **Standard 24-pin package**
- **All inputs are capacitive and do not sink or source current**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to +150	
	All input, output and supply voltages with respect to ground pin	-0.5 to +7	V

OBJECTIVE SPECIFICATION 2609-F,I,N

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low		0		0.65	
V_{IH}	High[1]	Driven by TTL	2.2		V_{CC}	
	Output voltage					V
V_{OB}	Low (Blank)	I_{OL} = 1.6mA	0	0.4		
V_{OD}	High (Dot)	I_{OH} = -40μA	2.4			
I_{IH}	Leakage current	V_{IH} = 5.25V, V_{CC} = 4.75V			10	μA
I_{CC}	Supply current			80	100	mA
	Capacitance[2]	f = 1.0MHz, T_A = 25°C				pF
C_{IN}	Input				7.5	
C_{OUT}	Output			4.0	15	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified,
V_{IN} levels = 0.65V and 2.2V or driven by TTL, Input t_r and t_f < 20ns,
Measurement reference level = 1.5V, Output loading = 1 TTL gate +130pF

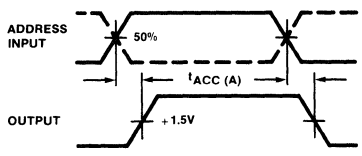
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Access time						ns
$t_{ACC(A)}$		Output	Address		350	500	
$t_{ACC(RS)}$		Output	Row select		300	500	
P_D	Power dissipation				400	525	mW

NOTES

1. No pullup resistors are required.
2. Capacitances are periodically sampled rather than 100% tested.
3. This is advance information and specifications are subject to change without notice.

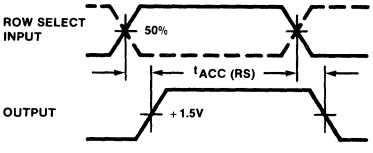
TIMING DIAGRAMS

ADDRESS ACCESS



Address inputs are set in a dc state

ROW SELECT ACCESS



Row select inputs are set in a dc state

MEMORY OPERATION USING POSITIVE LOGIC

(Most positive level = 1, most negative level = 0)

Address

To select 1 of the 128 characters, apply the appropriate binary code to the address inputs (A1-A7).

Row Select

To select 1 of the rows of the addressed character to appear at the 7 output lines, apply the appropriate binary code to the row select inputs (RS1-RS4).

Shifted Characters

These devices have the capability of displaying characters that descend below the bottom line (such as lower case letters j, y, g, p and q). Internal circuitry effectively drops the whole matrix for this type of character. Any character can be programmed to occupy either of the 2 positions in a 7X16 matrix.

Output

For these devices, an output dot is defined as a logic "1" level, and an output blank is defined as a logic "0" level.

MEMORY TIMING DEFINITIONS

$t_{ACC(A)}$ Address Access Time:
The time delay between a change in the address inputs and a corresponding change at the output lines with all other inputs held stable, and with the recommended load.

$t_{ACC(RS)}$ Row Select Access Time:
The time delay between a change in the row select inputs and the appearance of valid information at the output lines, with all other inputs held stable.

DISPLAY FORMAT

Figure 1 shows the relationship between the logic levels at the row select inputs and the character row at the outputs. The 2609 allows the user to locate the basic 7X9 font anywhere in 7X16 array. In addition, a shift-

ed font can be placed anywhere in the same 7X16 array. For example, the basic CN6571 font is established in rows R14-R6. All other rows are automatically blanked. The shifted font is established in rows R11-R3. Thus, while any one character is contained in a 7X9 array, the CN6571 requires a 7X12 array on the CRT screen to contain both normal and descending characters. Other uses of the shift option may require as much as the full 7X16 array, or as little as the basic 7X9 array.

The 2609 can be programmed to be scanned either from bottom to top or from top to bottom. This is achieved through the option of assigning row numbers in ascending or descending count, as long as both the basic font and the shifted font are the same. For example, an up counter will scan the CN6571 from bottom to top.

CUSTOM PROGRAMMING FOR 2609

By programming of a single photomask, the customer may specify the content of this memory. Encoding of the photomask is done with the aid of a computer. Use of the computer provides a quick and efficient way to implement a custom bit pattern, while reducing the cost of implementation.

Information on the general options of the 2609 should be submitted on an Organizational Data Form.

Programming of the memory content should be transmitted to Signetics as completed data encoding sheets. The Data Encoding Sheet Format illustration details the requirements for proper completion of the data encoding sheets.

Three examples are shown to indicate proper character encoding. The following rules apply:

1. Enter the character number in the space provided above each dot matrix. Address 0000000 is used for character number 1, with other character numbers following in the normal binary progression.
2. Indicate the rows to be used in the space provided to the left of each dot matrix. Note that characters may be positioned in either of two 7X9 locations on a 7X16 matrix; however, only 2 positions are allowed per mask option. The character for a given address may occupy only 1 of these positions
3. Column zero is added to the dot matrix on the format sheet for use in indicating shifted characters. If a character is to be shifted, a dot should be entered into the first row of the first (zero) column (see the third example, j).
4. The desired character should be entered in the matrix, using only columns B1-B7.

FORMAT FOR PROGRAMMING GENERAL OPTIONS

ORGANIZATIONAL DATA
SIGNETICS 2609 MOS ROM

Customer _____

Customer part no. _____ Rev. _____

Row number for top row of non-shifted characters _____

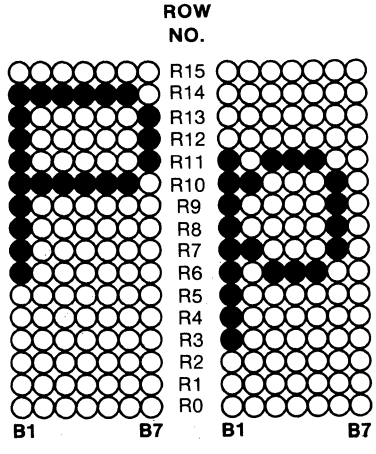
Row number for top row of shifted characters _____

Count down Count up

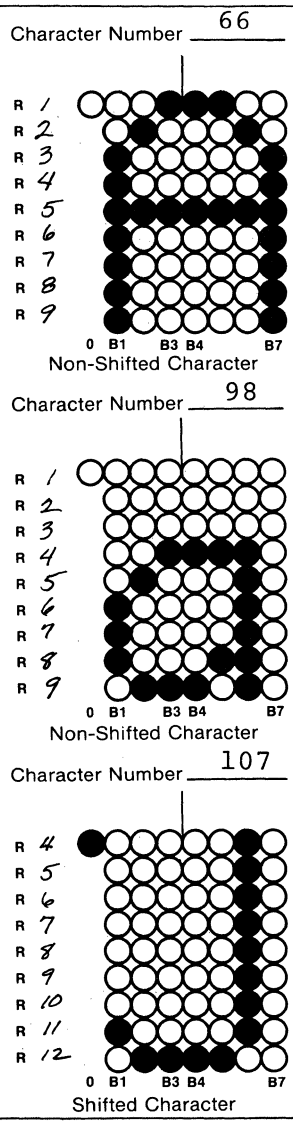
ROW SELECT INPUT CODE AND SAMPLE CHARACTERS FOR CN6571

TRUTH TABLE

RS4	RS3	RS2	RS1	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15



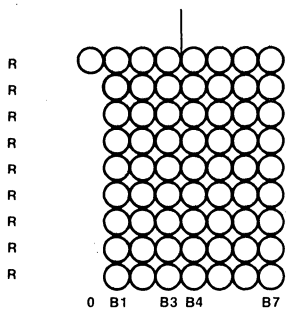
DATA ENCODING SHEET FORMAT



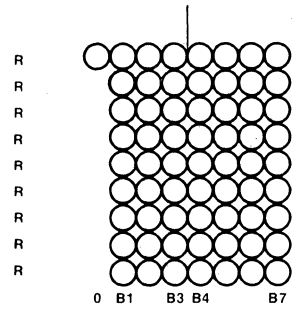
DATA ENCODING SHEET FOR 2609

Customer ____________ Customer Part No. ____________ Rev. ______ Page ______ of ______ Pages

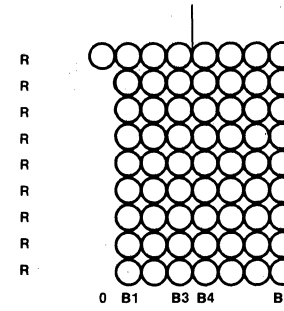
Character Number ________



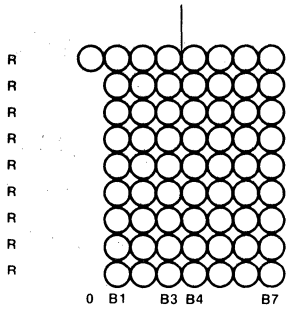
Character Number ________



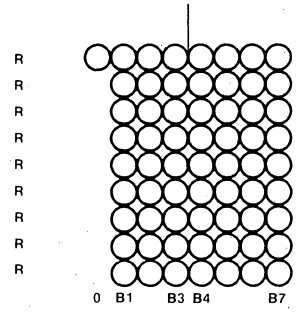
Character Number ________



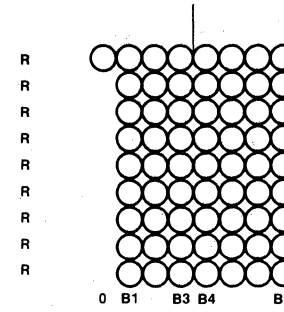
Character Number ________



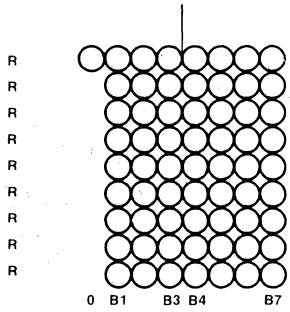
Character Number ________



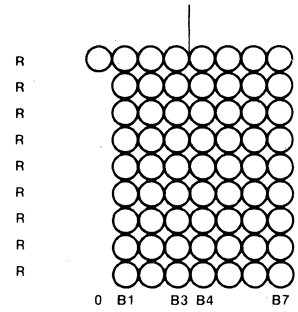
Character Number ________



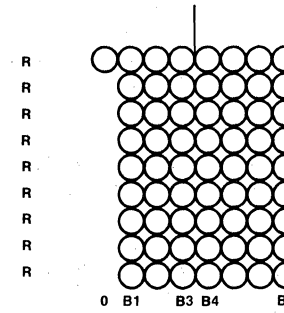
Character Number ________



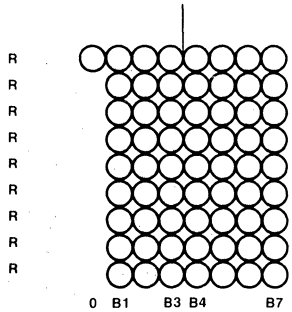
Character Number ________



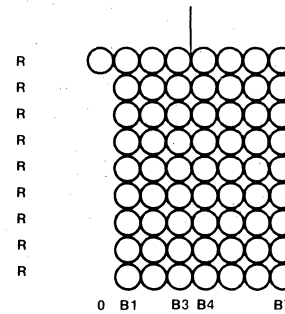
Character Number ________



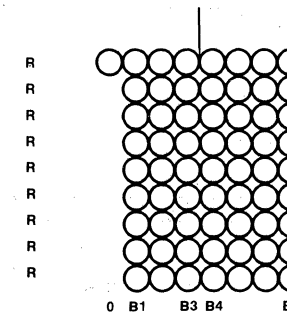
Character Number ________



Character Number ________



Character Number ________



USASCII CHARACTER GENERATOR CODE

The CN6571 has been programmed with the characters shown. No attempt has been made on this figure to indicate columns and rows actually used on the display for each character.

ADDRESS (A)							DISPLAYED CHARACTER	SHIFTED
7	6	5	4	3	2	1		
0	0	0	0	0	0	0	α	
0	0	0	0	0	0	1	β	yes
0	0	0	0	0	1	0	γ	yes
0	0	0	0	0	1	1	δ	
0	0	0	0	1	0	0	ε	
0	0	0	0	1	0	1	ζ	
0	0	0	0	1	1	0	η	yes
0	0	0	0	1	1	1	θ	
0	0	0	1	0	0	0	ι	
0	0	0	1	0	0	1	κ	
0	0	0	1	0	1	0	λ	
0	0	0	1	0	1	1	μ	yes
0	0	0	1	1	0	0	ν	
0	0	0	1	1	0	1	ξ	
0	0	0	1	1	1	0	ο	
0	0	0	1	1	1	1	π	
0	0	1	0	0	0	0	ρ	yes
0	0	1	0	0	0	1	σ	
0	0	1	0	0	1	0	τ	
0	0	1	0	0	1	1	υ	
0	0	1	0	1	0	0	φ	
0	0	1	0	1	0	1	χ	
0	0	1	0	1	1	0	ψ	yes
0	0	1	0	1	1	1	ω	
0	0	1	1	0	0	0	Ω	
0	0	1	1	0	0	1	√	
0	0	1	1	0	1	0	→	
0	0	1	1	0	1	1	←	
0	0	1	1	1	0	0	↑	
0	0	1	1	1	0	1	÷	
0	0	1	1	1	1	0	Σ	
0	0	1	1	1	1	1	≈	
0	1	0	0	0	0	0	Blank	
0	1	0	0	0	0	1	!	
0	1	0	0	0	1	0	"	
0	1	0	0	0	1	1	#	
0	1	0	0	1	0	0	$	
0	1	0	0	1	0	1	%	
0	1	0	0	1	1	0	&	
0	1	0	0	1	1	1	'	
0	1	0	1	0	0	0	(	
0	1	0	1	0	0	1	)	
0	1	0	1	0	1	0	*	
0	1	0	1	0	1	1	+	
0	1	0	1	1	0	0	,	yes
0	1	0	1	1	0	1	—	
0	1	0	1	1	1	0	.	
0	1	0	1	1	1	1	/	
0	1	1	0	0	0	0	0	
0	1	1	0	0	0	1	1	
0	1	1	0	0	1	0	2	
0	1	1	0	0	1	1	3	
0	1	1	0	1	0	0	4	
0	1	1	0	1	0	1	5	
0	1	1	0	1	1	0	6	
0	1	1	0	1	1	1	7	
0	1	1	1	0	0	0	8	
0	1	1	1	0	0	1	9	
0	1	1	1	0	1	0	:	
0	1	1	1	0	1	1	;	
0	1	1	1	1	0	0	<	
0	1	1	1	1	0	1	=	
0	1	1	1	1	1	0	>	
0	1	1	1	1	1	1	?	

ADDRESS (A)							DISPLAYED CHARACTER	SHIFTED
7	6	5	4	3	2	1		
1	0	0	0	0	0	0	@	
1	0	0	0	0	0	1	A	
1	0	0	0	0	1	0	B	
1	0	0	0	0	1	1	C	
1	0	0	0	1	0	0	D	
1	0	0	0	1	0	1	E	
1	0	0	0	1	1	0	F	
1	0	0	0	1	1	1	G	
1	0	0	1	0	0	0	H	
1	0	0	1	0	0	1	I	
1	0	0	1	0	1	0	J	
1	0	0	1	0	1	1	K	
1	0	0	1	1	0	0	L	
1	0	0	1	1	0	1	M	
1	0	0	1	1	1	0	N	
1	0	0	1	1	1	1	O	
1	0	1	0	0	0	0	P	
1	0	1	0	0	0	1	Q	
1	0	1	0	0	1	0	R	
1	0	1	0	0	1	1	S	
1	0	1	0	1	0	0	T	
1	0	1	0	1	0	1	U	
1	0	1	0	1	1	0	V	
1	0	1	0	1	1	1	W	
1	0	1	1	0	0	0	X	
1	0	1	1	0	0	1	Y	
1	0	1	1	0	1	0	Z	
1	0	1	1	0	1	1		
1	0	1	1	1	0	0	—	
1	0	1	1	1	0	1	⌋	
1	0	1	1	1	1	0	⌐	
1	0	1	1	1	1	1	—	
1	1	0	0	0	0	0	`	
1	1	0	0	0	0	1	a	
1	1	0	0	0	1	0	b	
1	1	0	0	0	1	1	c	
1	1	0	0	1	0	0	d	
1	1	0	0	1	0	1	e	
1	1	0	0	1	1	0	f	
1	1	0	0	1	1	1	g	yes
1	1	0	1	0	0	0	h	
1	1	0	1	0	0	1	i	
1	1	0	1	0	1	0	j	yes
1	1	0	1	0	1	1	k	
1	1	0	1	1	0	0	l	
1	1	0	1	1	0	1	m	
1	1	0	1	1	1	0	n	
1	1	0	1	1	1	1	o	
1	1	1	0	0	0	0	p	yes
1	1	1	0	0	0	1	q	yes
1	1	1	0	0	1	0	r	
1	1	1	0	0	1	1	s	
1	1	1	0	1	0	0	t	
1	1	1	0	1	0	1	u	
1	1	1	0	1	1	0	v	
1	1	1	0	1	1	1	w	
1	1	1	1	0	0	0	x	
1	1	1	1	0	0	1	y	yes
1	1	1	1	0	1	0	z	
1	1	1	1	0	1	1	{	
1	1	1	1	1	0	0	¦	
1	1	1	1	1	0	1	}	
1	1	1	1	1	1	0	~	
1	1	1	1	1	1	1	Solid	

CARD FORMAT HEADER CARDS

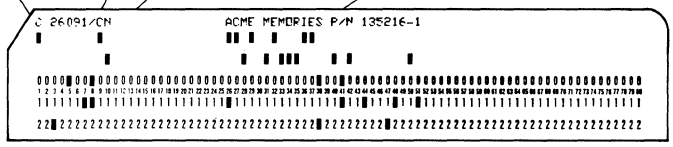
IDENTIFICATION CARDS

Column 8, 9
Custom designation "CN"

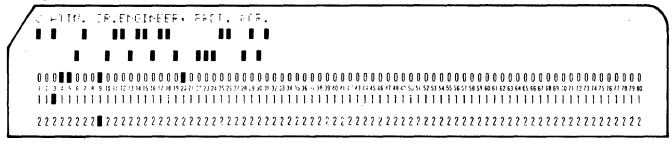
Column 10, 11, 12, 13,
Custom number (assigned by Signetics)

Column 2-6
Basic part type

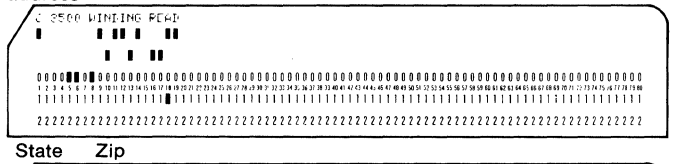
Column 26-80
Customer identification



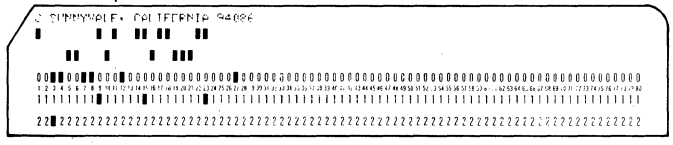
Person responsible for reviewing Signetics computer generated truth table



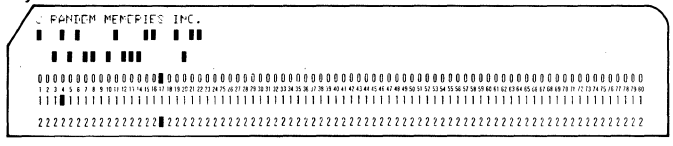
Street address



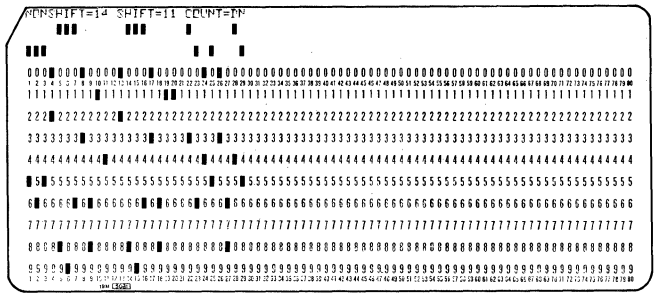
City State Zip



Company name



CHARACTER SET UP CARD



CHARACTER SET UP CARD

Card #6

Columns	
1	Type in —, NONSHIFT =
10 & 11	Enter decimal number that corresponds to TOP row of the nonshifted characters
13-18	Type in —, SHIFT =
19 & 20	Enter decimal number that corresponds to TOP row of shifted characters
22-27	Type in —, COUNT =
28 & 29	These columns are used to identify the direction of the numerical count for the subsequent row numbers. When "DN" is punched this adds -1 to the number of top row of character to get the second row; third row is -2; etc.
30-78	Leave blank
79 & 80	Enter truth table number

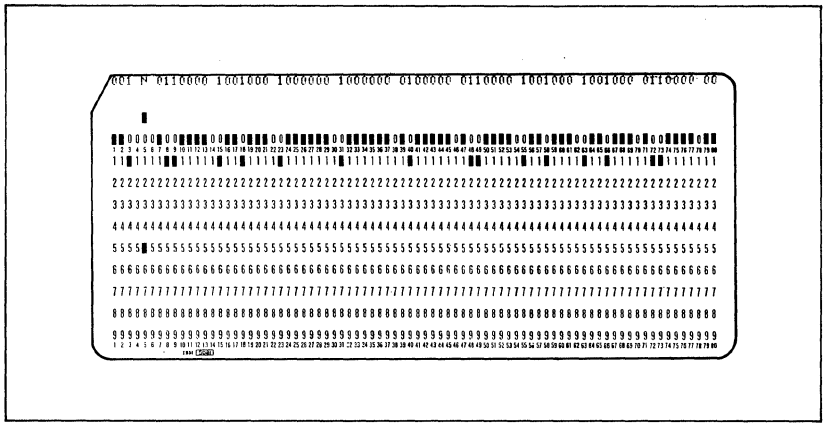
CHARACTER CARDS

This format identifies characters by numerical sequence beginning with 001 (the first character of the set) and ending with 128 (the last character of the set). Address 0000000 is used for character #1, with other characters following in normal binary progression with A_1 the LSB and A_7 the MSB.

Columns	
1-3	Enter decimal character number
4	Leave blank
5	Enter character position: S for shifted, N for nonshifted
6	Leave blank
7-13	Enter contents of the top row of character beginning with the least significant bit (B_1) and ending with the most significant bit (B_7)[A,B]
14	Leave blank
15-21	Enter contents of second row of character (LSB to MSB)
22	Leave blank
23-29	Enter third row
30	Leave blank
31-77	Continue until contents of all 9 rows have been entered
78	Leave blank
79 & 80	Enter truth table number

OBJECTIVE SPECIFICATION 2609-F,I,N

CHARACTER CARD



NOTES

A. An entered dot corresponds to a high voltage output
B. A complete card deck consists of 5 header cards, 1 set up card and 128 character cards

2607-F,I,N

FEATURES

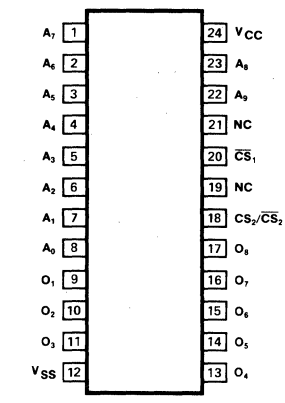
- Static operation—no clocks
- Access time: 450ns max
- Single 5V power supply
- TTL compatible inputs and outputs
- Power dissipation: 525mW
- Tri-state outputs
- Mask programmable chip select for easy word expansion
- N-channel silicon gate technology
- Standard 24-pin package
- Designed for system applications requiring high performance, large bit storage and simple interfacing
- 2 chip selects ($\overline{CS}1$, negative true; $CS2/\overline{CS}2$, either negative true or positive true at mask level)
- Pin for pin compatible with Intel 2708 electrically programmed erasable ROM and Intel 2308/8308 ROM, except only requiring +5V supply
- All inputs capacitive and do not sink or source current

PIN DESIGNATION

PIN NO.	FUNCTION
A_0-A_9	Address inputs
O_1-O_8	Data outputs
CS_1, CS_2	Chip select inputs
NC	No connect

PIN CONFIGURATION

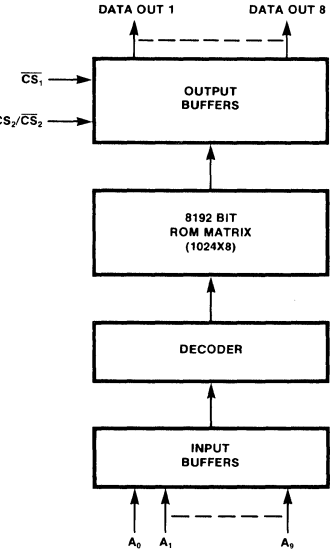
F,I,N PACKAGE



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to +150	
	All input, output, and supply voltages with respect to ground pin	-0.5 to +7	V

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = OV unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low				0.65	
V_{IH}	High		2.2		V_{CC}+1.0	
	Output voltage					V
V_{OL}	Low	I_{OL} = 2mA			0.45	
V_{OH1}	High	I_{OH} = 1mA	2.4			
I_{LI}	Input load current	V_{IN} = 0 to 5.25V			10	μA
I_{LO}	Output leakage current	Chip deselected			10	μA
I_{CC}	Supply current			80	100	mA
P_D	Power dissipation			400	525	mW
	Capacitance	T_A = 25°C, f = 1MHz, V_{CC} and all other pins tied to V_{SS}				pF
C_{IN}	Input				7.5	
C_{OUT}	Output				15	

AC ELECTRICAL CHARACTERISTICS

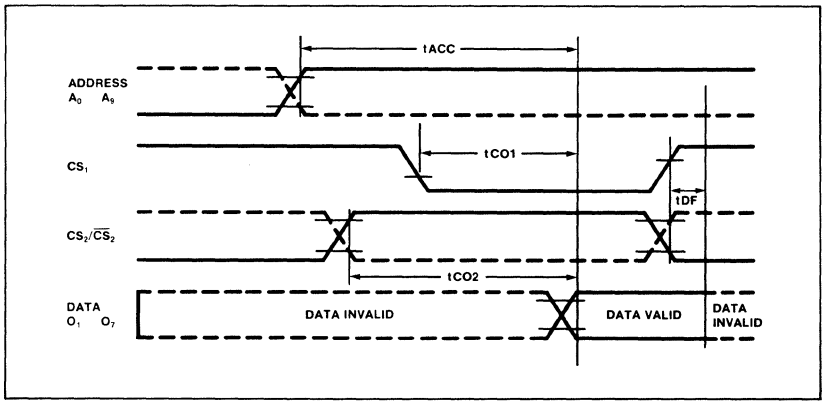
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = OV unless otherwise specified, Output load = 1 TTL gate, Input pulse levels = .65V to 2.2V, Input pulse rise and fall times = 20ns, Timing measurement reference level: V_{IH} = 2.0V, V_{OH} = 0.8V, V_{IL} = V_{OL}

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Delay time						ns
t_{ACC}		Output	Address		200	450	
t_{CO1}		Output	Chip select 1		85	160	
t_{CO2}		Output	Chip select 2		85	160	
t_{DF}	Float time	Output data	Chip deselect		70	160	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values for T_A = 25°C and typical supply voltages.

TIMING DIAGRAM



CARD FORMAT

IDENTIFICATION CARDS

Column 8, 9
Custom designation "CN"

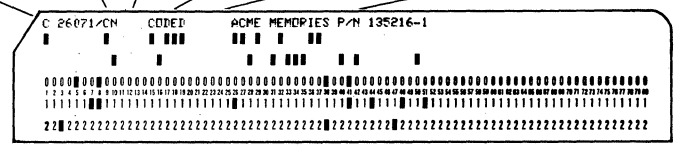
Column 10, 11, 12, 13,
Custom number (assigned
by Signetics)

Column 15, 16, 17, 18, 19
"Coded"

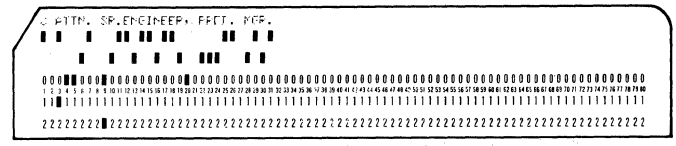
Column 22
Chip select code
(CS2)

Column 26-80
Customer identificaton

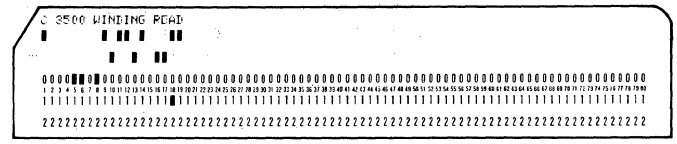
Basic part type



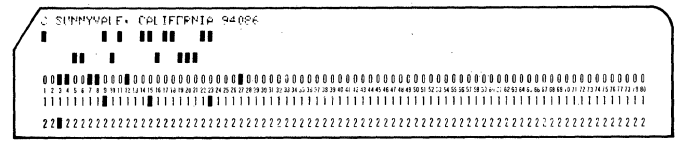
Person responsible for reviewing Signetics computer generated truth table



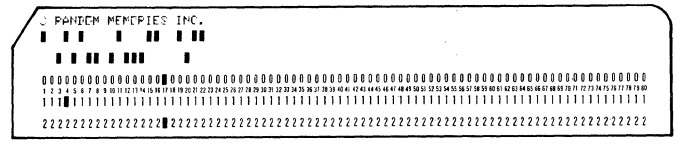
Street address



City State Zip



Company name



INPUT FORMAT

A. For a N words X 8-bit organization only, cards 2 and the following cards should be punched as shown. Each card specifies the 8-bit output of 8 words.

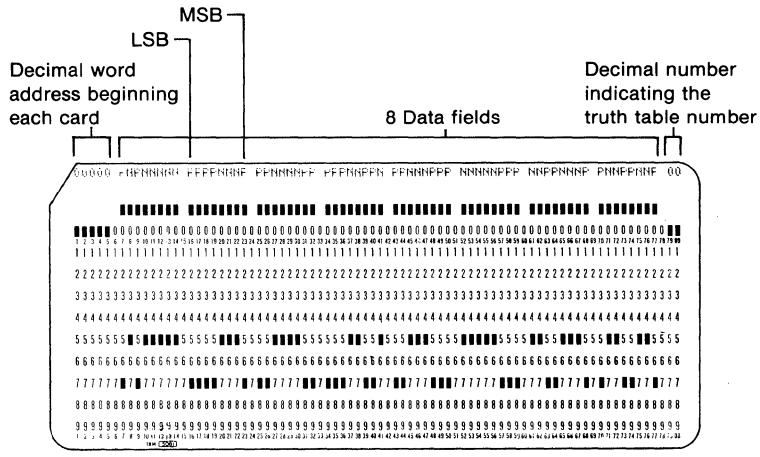
B. Paper Tape Format
The paper tapes which should be used are the:

1. 1" wide paper tape using 7 or 8-bit ASCII code, such as a model 33 ASR teletype produces:

The format requirements are as follows:

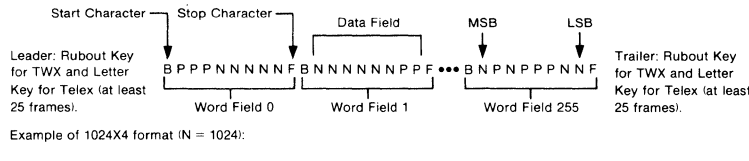
1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the NX8 organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for the NX8 organization.

   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORLD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes).
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every 4 word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every 4 word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

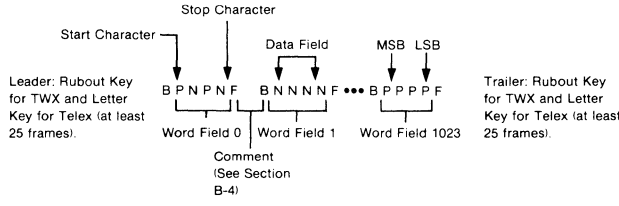


COLUMN	DATA
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., 00000, 00008, 00016, etc.
6	Blank
7-14	Data field
15	Blank
16-23	Data field
24	Blank
25-32	Data field
33	Blank
34-41	Data field
42	Blank
43-50	Data field
51	Blank
52-59	Data field
60	Blank
61-68	Data field
69	Blank
70-77	Data field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

EXAMPLE OF 256X8 FORMAT (N = 256)



Example of 1024X4 format (N = 1024):

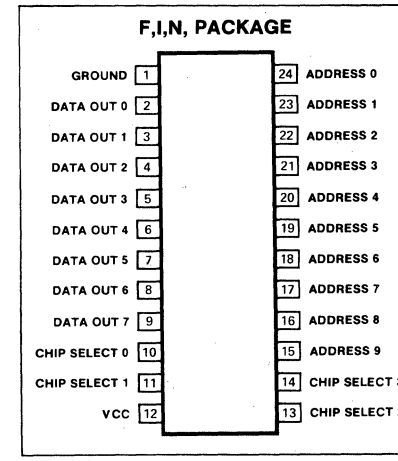


2608-F,I,N • 2608-1-F,I,N

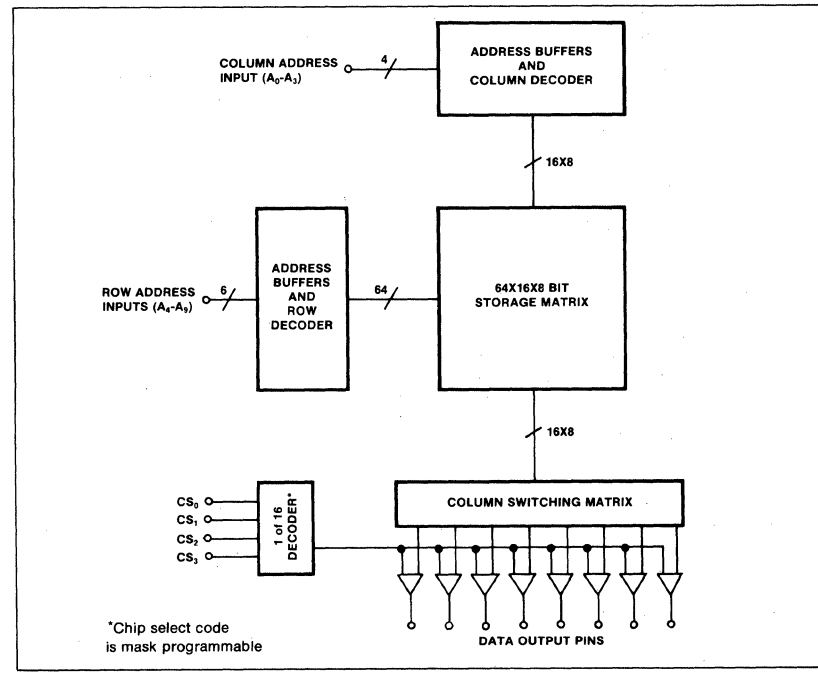
FEATURES

- Static operation—no clocks
- Access time:
  - 2608: 550ns
  - 2608-1: 450ns
- Single 5V power supply and ground power connections
- TTL compatible inputs and outputs
- Power dissipation: 400mW max
- Tri-state outputs
- 4 mask programmable chip selects for easy word expansion
- Low threshold n-channel silicon gate technology which allows ease of use with low voltage logic families such as transistor-transistor logic
- Standard 24-pin package
- Fully decoded

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
	All input, output and supply voltages with respect to ground pin	-0.5 to 7	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ (unless otherwise noted)[3,4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low		-0.5		0.65	
V_{IH}	High		2.2			
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.45	
V_{OH}	High	$I_{OH} = 100\mu A$	2.4			
I_{IN}	Input load current	$0 \leq V_{IN} \leq 5.25V$			10	μA
	Output leakage current	Device deselected				μA
I_{LOH}		$V_O = 2.4V$			10	
I_{LOL}		$V_O = 0.4V$			10	
I_{CC}	Supply current	$V_{CC} = 5.25V$, $T_A = 0°C$			80	mA
	Capacitance					pF
C_{IN}	Input	$V_{IN} = OV$			7.5	
C_{OUT}	Output	$V_{OUT} = OV$			15	

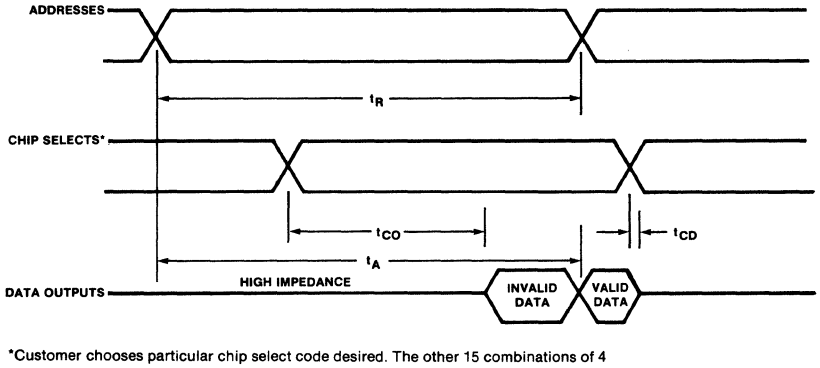
AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$[8,9,10]

PARAMETER		TO	FROM	2608			2608-1			UNIT
				Min	Typ	Max	Min	Typ	Max	
t_R	Read cycle time			550			450			ns
t_{CO}	Enable time[11]	Output	Chip select			300			300	ns
t_{CD}	Disable time[11]	Output	Chip select	10		150	10		150	ns
t_A	Access time[11]	Output	Address	100		550	100		450	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 50° C/W junction to ambient.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameter valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process improvements.
7. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
8. Input levels swing between 0.65V and 2.2V.
9. Input signal transition times are 20ns.
10. Timing reference level is 1.5V.
11. Output load is one standard TTL load plus 130pF.

TIMING DIAGRAM



*Customer chooses particular chip select code desired. The other 15 combinations of 4 chip select inputs disable the outputs.

PIN DESCRIPTION

Addresses

These 10 TTL-compatible inputs are decoded on-chip to select one of 1024 8-bit bytes. Since the 2608 utilizes static logic throughout, a change in addresses results in a change in data as long as the chip is selected. Access time is measured from the point where the last address input became stable. Cycle time and access time are equal in a static ROM design.

Chip Selects

There are 4 TTL-compatible chip select inputs for the 2608. Only 1 combination of these 4 signals enables the chip. The other 15 disable the chip. The particular enabling combination is chosen by the customer and specified on the first punched card of the customer card deck. A positive logic convention is assumed.

Data Outputs

The 8 data outputs are push-pull buffers capable of driving one standard TTL load plus a 130pF load capacitance. These outputs are placed in the high impedance state when any one of the disabling combinations of the chip select inputs is present.

CODING FORMAT

Coding data for the 2608 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer Aided Design (CAD) facility. The truth table will then be sent to the customer for final approval. On receipt of final approval, Signetics will produce masks and proceed with manufacturing.

DATA CARDS

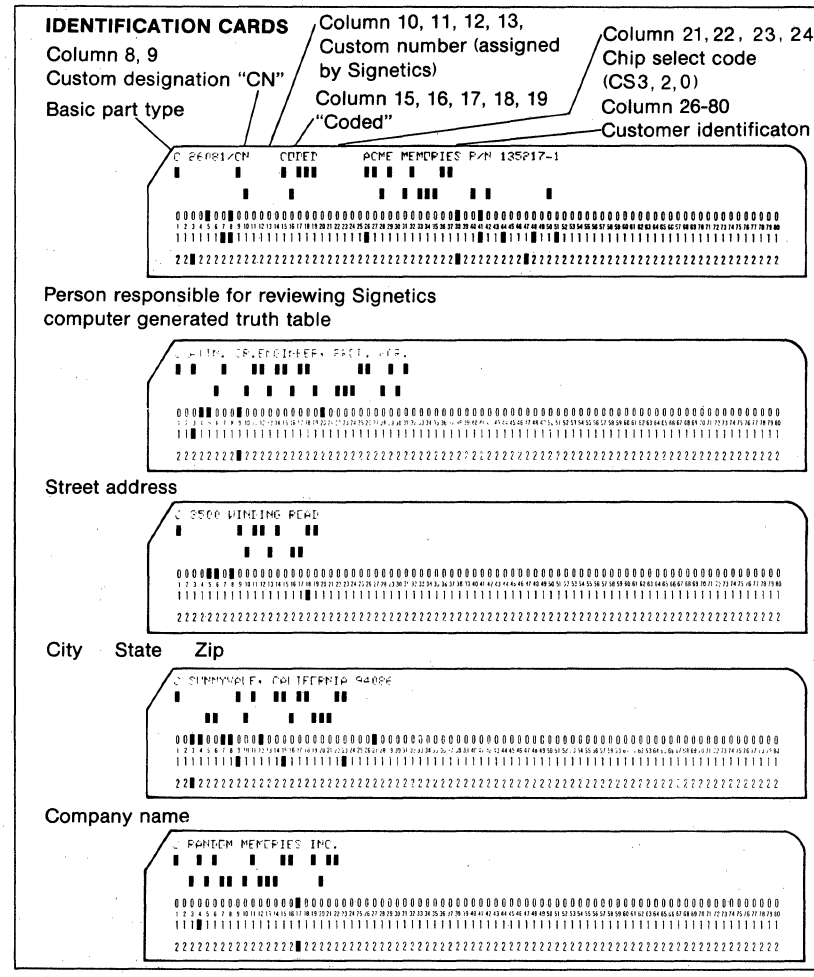
Columns

12—75	Hexadecimal data coding
77—78	Card number (starting 01)
79—80	Total number of cards (32)

Column 12 on the first card contains the hexadecimal equivalent of bits D7 thru D4 of byte 0, while column 13 contains the hexadecimal equivalent of bits D3 thru D0. Columns 14 and 15 contain byte 1, columns 16 and 17 byte 2, and so on.

The first card contains the first 32 bytes. Columns 12 and 13 on the second card will contain byte 32 (the 33rd byte). A total of 32 cards will contain 1024 bytes of 8 bit.

CARD FORMAT



BINARY TO HEXADECIMAL CONVERSION

BINARY COMBINATION D0-D3 or Dr-D7				HEXA-DECIMAL CHARACTER
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	F

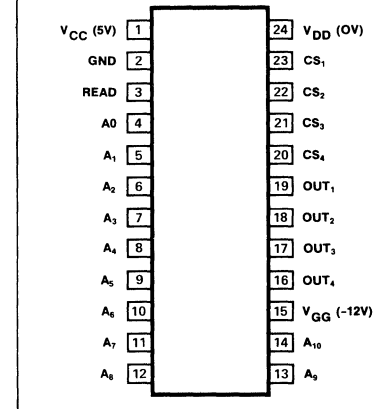
2580-I,N

DESCRIPTION

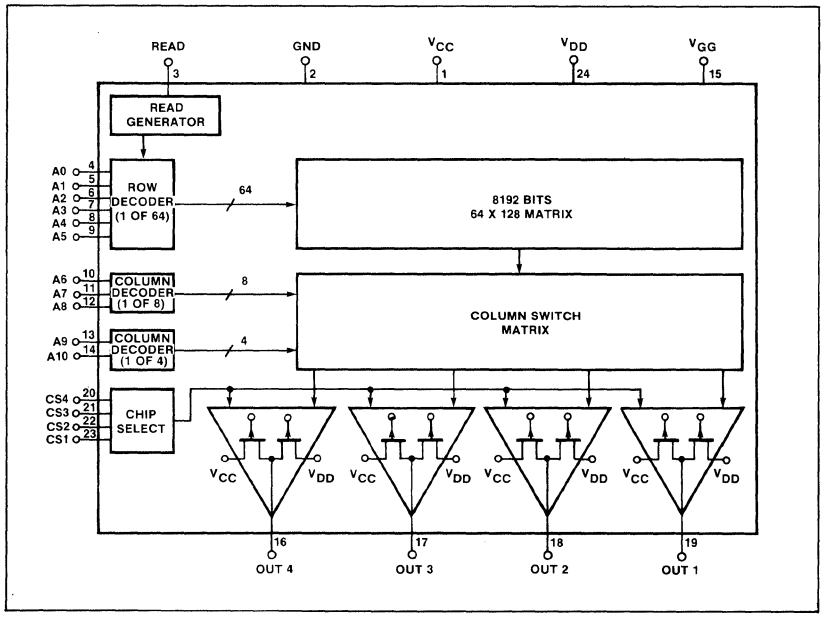
The 2580 has a Read input which controls the entry of data from the ROM into output latches. Three-state outputs allow OR-tying for implementing larger memories. The outputs are enabled by a programmable 4-bit select code applied to 4 binary chip select terminals.

PIN CONFIGURATION

I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at 70°C[2]	730	mW
	Input and supply voltages with respect to V_{CC}[3]	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = OV, V_{GG} = -12V ± 5% unless otherwise noted.[4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[8]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.5	
V_{OH}	High	I_{OH} = 100μA	3.8			
I_{LI}	Input load current	V_{IN} = -5.5V, T_A = 25°C		10	500	nA
I_{LO}	Output leakage current	V_{OUT} = OV, T_A = 25°C		10	1000	nA
	Supply current[9]					mA
I_{CC}	V_{CC}			23	35	
I_{GG}	V_{GG}			23	35	
C_{IN}	Input capacitance	f = 1MHz, V_{AC} = 25m p-p, V_{IN} = V_{CC}			10	pF

AC ELECTRICAL CHARACTERISTICS

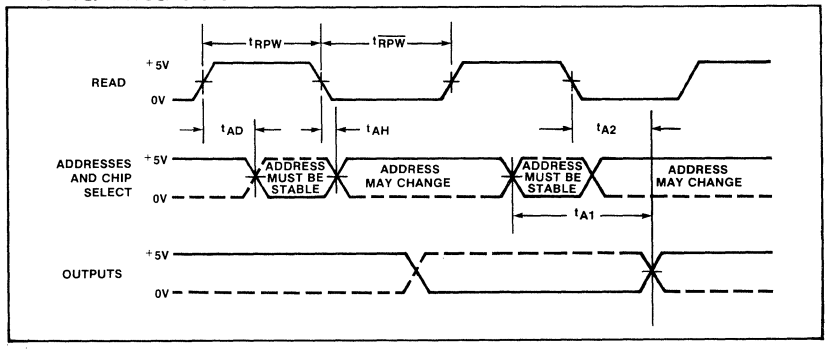
T_A = 25°C, V_{CC} = 5V ± 5%, V_{DD} = OV, V_{GG} = -12V ± 5% unless otherwise specified.

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Pulse width						ns
t_{RPW}	Read[10]			650	500		
$t_{\overline{RPW}}$	$\overline{\text{Read}}$[11]			500	400		
	Address time						ns
t_{AD}	Delay[12]					50	
t_{AH}	Hold			0			
	Delay time						ns
t_{A1}		Output	Address		625	950	
t_{A2}		Output	End of read pulse		250	350	

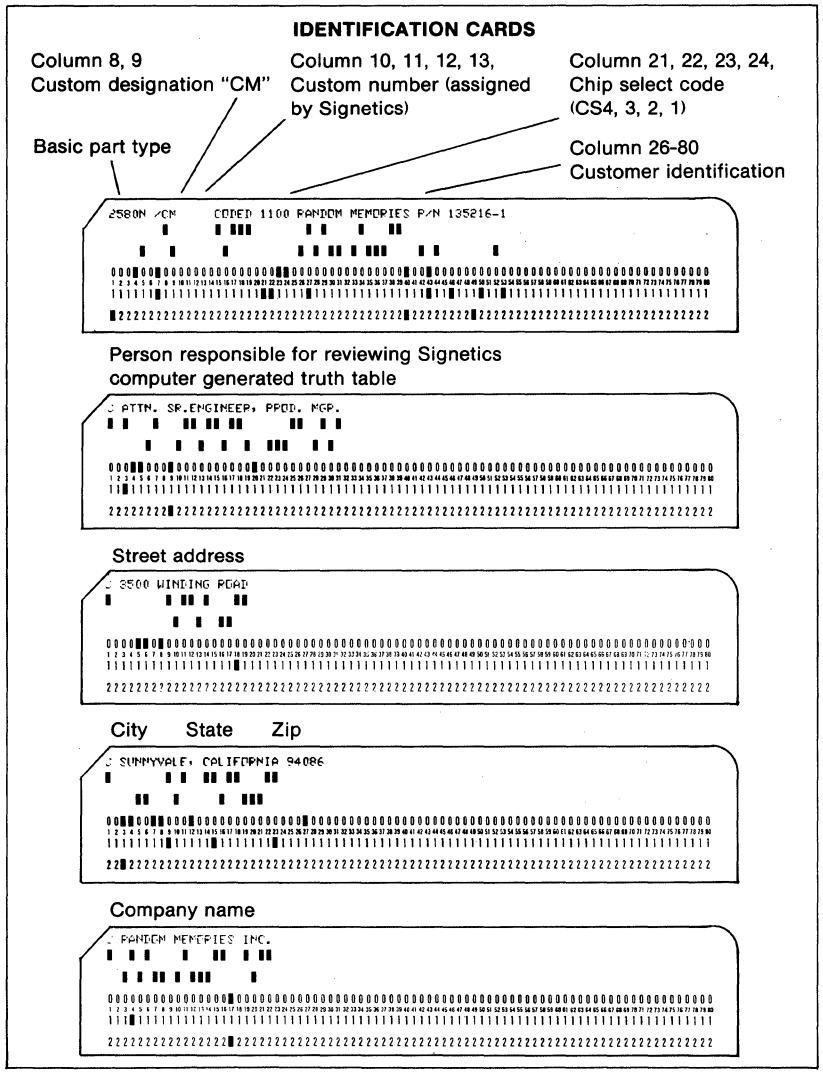
NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to 70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} -1.85 and V_{IL} = V_{CC} -4.15V.
9. Outputs open, t_{RPW} = 500ns, $t_{\overline{RPW}}$ = 500ns.
10. During t_{RPW} addresses are decoded and sent to the memory matrix, and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (falling edge) of the read pulse. After t_{A2}, data appears at the output terminals.
11. During $t_{\overline{RPW}}$ data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
12. Addresses must be stable within 50ns after the read line rises and must remain stable until the read line falls.

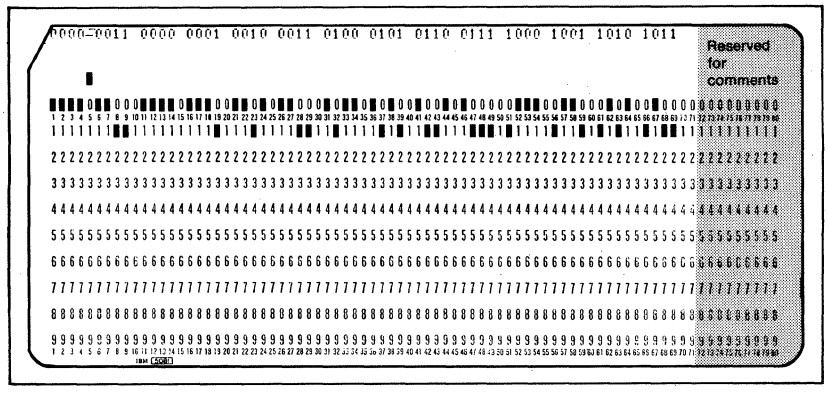
TIMING DIAGRAM



CARD FORMAT



EXAMPLE



CODING FORMAT

Coding data for the 2580 may be sent to Signetics via punched cards or via a written truth table. Cards are preferred since errors are essentially eliminated.

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer Aided Design (CAD) facility. The truth table will then be sent to the customer requesting engineer for final approval. On receipt of final approval, Signetics will cut the rubylith mask and proceed with manufacture.

DATA CARD FORMAT

Columns	
1-4	Decimal equivalent of first data word location Example: 0124 Note: Leading zeros must be used for addresses from 0000 to 0999
5	Dash (—) to separate numbers
6-9	Address of last word on card
10	Blank
11-14	First data word (O_4, O_3, O_2, O_1)
15	Blank
16-19	Second data word
Etc. thru 71	
72-80	Reserved for comments (these columns are ignored by the computer)

Up to twelve (12) data words can be coded on one card. Less than 12 may be used as long as the first and last addresses are given in columns 1-9.

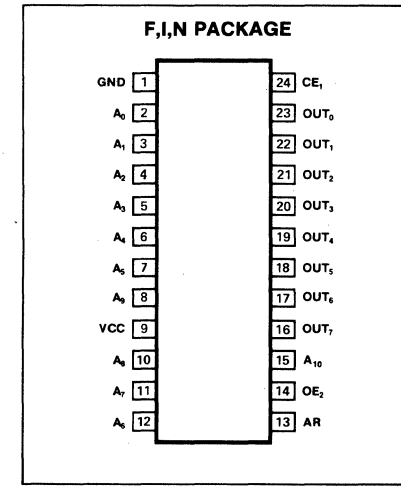
DESCRIPTION

The 2600 outputs appear and remain in a steady state condition until a new address is read. The 16,384 bits are organized as 2048 addresses with 8 output lines. Full address decoding is performed on chip. The 2600's size enhances its usage in any high density, fixed memory application such as logic function generation or microprogramming. Programming of the device is accomplished via the use of one custom mask during device fabrication.

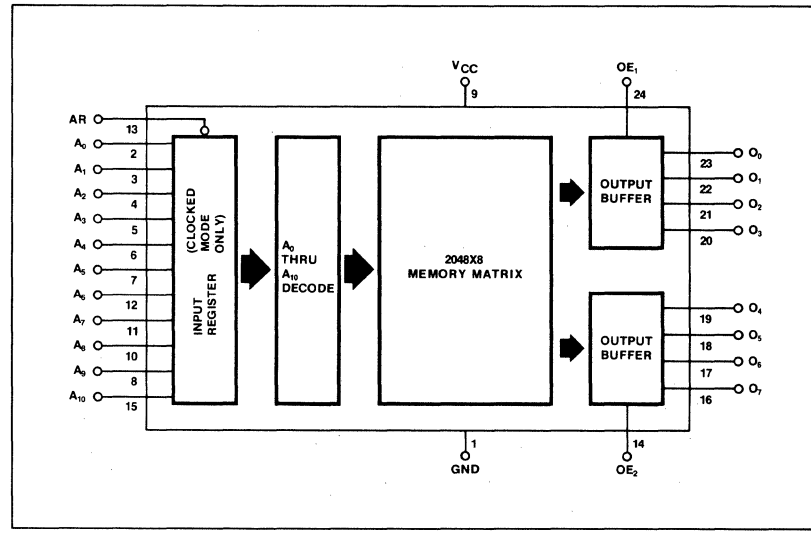
FEATURES

- **Completely static**
- **Utilizes MOS n-channel si-gate technology**
- **Clocked or unclocked operation**
- **Access time: 300/550ns max**
- **Single +5V power supply**
- **2 output enable controls allow:**
  Wire OR'D three-state outputs for expanded memories
  2048X8 or 4096X4 organization
- **All inputs and outputs directly TTL compatible**
- **Pin compatible with EA4600 and EA4900**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to +150	
P_D	Power dissipation	Hermetic 1.25	W
	Voltages on all inputs and supply pins	-0.5 to +7.0	V

ELECTRICAL DRIVE REQUIREMENTS $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[2,3]	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage	Address read, address input and output enable				V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage	TTL interface				V
V_{OL}	Low data	I_O = 1.6mA		0.2	0.4	
V_{OH}	High data	I_O = -100μA	2.4	3.5	V_{CC}	
I_{LI}	Input leakage current	Test pin at V = V_{CC} max, Other pins at ground			10	μA
I_{CC}	Supply current	V_{CC} = V_{CC} max 25°C		80	115	mA
	Capacitance	0V bias, f = 1MHz				pF
C_{IN}	Address input			5	7.5	
C_{AR}	AR input			5	7.5	
C_{OUT}	Output			7	10	

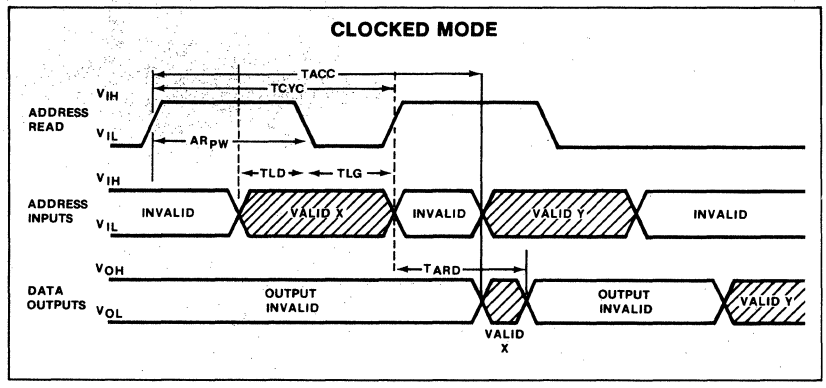
TIMING SPECIFICATIONS $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$

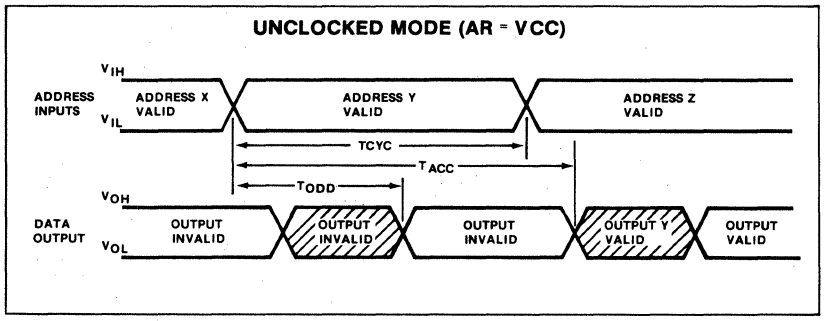
PARAMETER		TO	FROM	TEST CONDITIONS[2,3]	2600			2600-1			UNIT
					Min	Typ	Max	Min	Typ	Max	
CLOCKED MODE											
T_{CYC}	Cycle time				500			300			ns
	Pulse width										ns
AR_{PW}	Address read				300	150		100	50		
	Delay time										ns
T_{ACC}		Output	Address			450	550		200	300	
T_{ARD}		Output disturb	Address read		75	140		0	30		
T_{LD}	Address lead time				100	30		50	0		ns
T_{LG}	Address lag time				150	70		100	50		ns
UNCLOCKED MODE											
T_{CYC}	Cycle time			Standard	500			300			ns
	Delay time										ns
t_{ACC}		Output	Address			450	500		200	300	
T_{ODD}		Output disturb			0	50		0	30		
OUTPUT ENABLE (CLOCKED OR UNCLOCKED MODE)											
	Delay time										ns
T_{CO}		Output on	Output enable			100	300		(50)	150	
T_{DO}		Output off	Output enable			150	400		100	200	

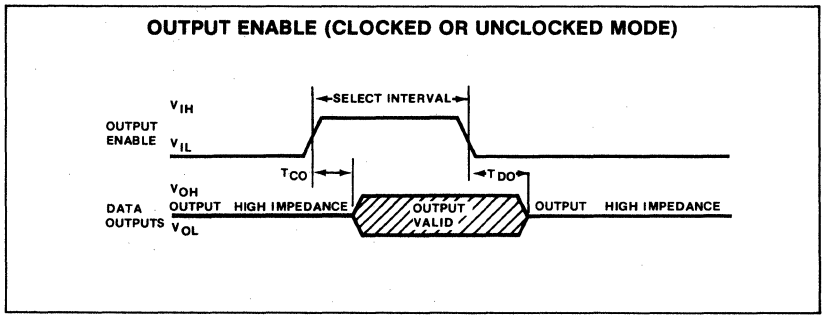
NOTES

1. Stresses more severe than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and operation of the device at any condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are referenced to V_{SS}. Positive current flows into the referenced pin.
3. Output load = 50pF plus 1 standard TTL input.

TIMING DIAGRAMS







DEFINITIONS

Clocked Mode

1. T_{CYC}, Cycle Time is the time between successive address read pulses.
2. T_{LD}, Address Lead Time is the minimum time required for the address to be valid prior to the falling edge of the AR pulse.
3. T_{LG}, Address Lag Time is the minimum amount of the time required for the address to remain valid after the falling edge of the AR pulse.
4. T_{ARD}, Address Read to Output Disturb Delay is the minimum time between the AR pulse and the first output transition when a new address is present.

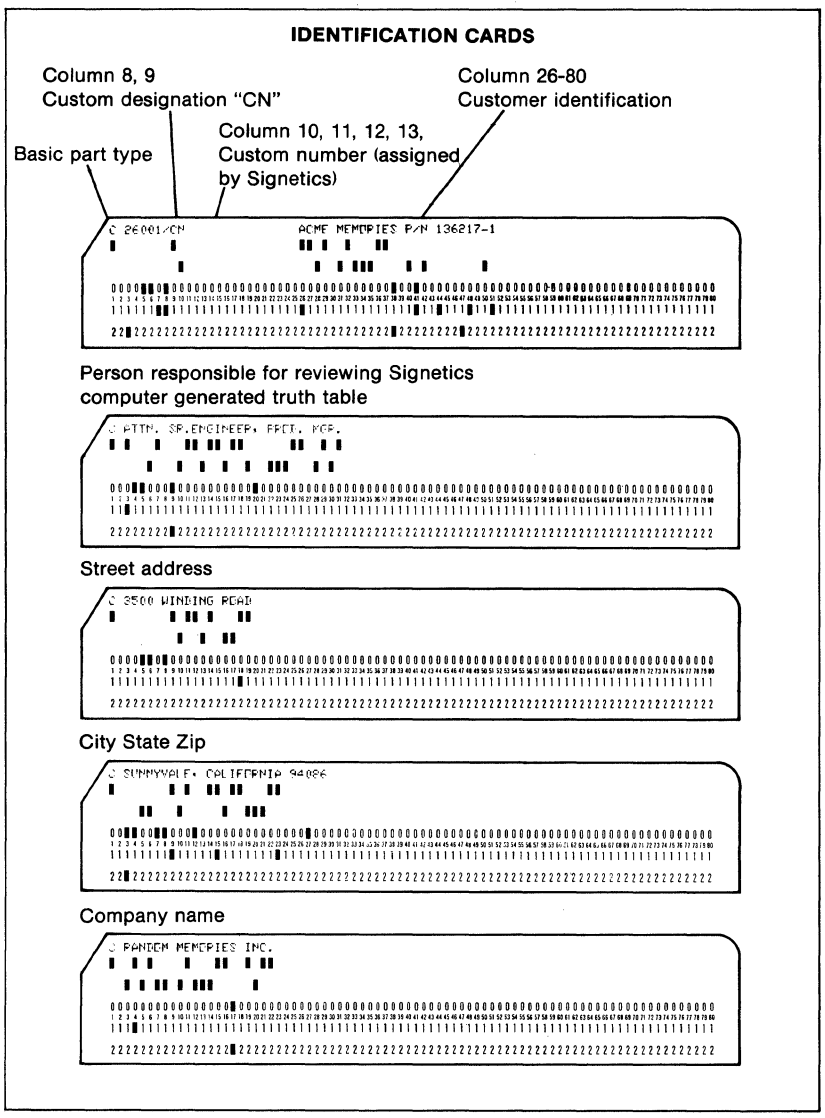
Unclocked Mode

1. T_{CYC}, Cycle Time is the time between application of successive addresses.
2. T_{ACC}, Address to Output Delay Time is the maximum time between a new valid address and the corresponding valid output.
3. T_{ODD}, Output Disturb Delay is the minimum time between the address change and the first output transition.

Output Enable

1. T_{CO}, Output Enable to Output ON Delay Time is the minimum time required for the output, in high impedance state, to become valid after rising edge of the output enable pulse.
2. T_{DO}, Output Enable to Output ON Delay Time is the minimum time required for the output to become high impedance after the falling edge of the output enable pulse.

CARD FORMAT



CUSTOM PATTERN PROGRAMMING INSTRUCTIONS

For the very large MOS ROM now produced by Signetics, a computer aided technique utilizing punched computer cards is employed. This technique requires that the customer supply Signetics with a deck of standard 80 column computer cards describing the data to be stored in the ROM array.

The required punching format is described below. All addresses must be included with their outputs defined. That is, no assumptions are made regarding the bit configuration of undefined outputs. Therefore the customer must submit cards defining the entire ROM contents, even though part or portions of the ROM may be unused (zeros).

Data Card Format for Custom ROMs

Each card is to be punched as follows. Note that for the Signetics 2600, a 3-digit octal number is used for representing the 8 ROM outputs.

Column	
1-4	Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card. (This is the initial address)
5-7	Punch a 3-digit octal number representing the outputs for the initial input address.
8-10	Punch a 3-digit octal number representing the outputs for the initial input address +1.
11-13	Punch a 3-digit octal number representing the outputs for the initial input address +2.
50-52	Punch a 3-digit octal number representing the outputs for the initial input address +15.
69-80	The unique number assigned to this ROM pattern by Signetics must be punched in this field enclosed by blank spaces. This number can be obtained by contacting your local Signetics salesman, representative, or the marketing department at the factory directly.

Each card, therefore, carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the unique ROM number. The card must be provided for all possible sequential address locations (in blocks of 16). A 2048 word ROM, therefore, requires 128 cards, with all 16 output words defined on each card.

GENERAL

The Signetics 2600-1 is a high speed 16K MOS ROM that utilizes the n-channel silicon gate technology. The maximum access and cycle time is 300ns. The memory is organized in a 2048X8 configuration at the outputs, however, two separate output enable signals allow the memory to also operate as a 4096X4 organization, where required.

The TTL compatibility of all inputs and outputs including the power requirements of only a single +5V supply, coupled with Signetics' process and design, results in a denser, more economical and more reliable part at the system level, where it counts.

Figure 1 illustrates the 2600-1 block diagram, while Figure 2 illustrates the pin configuration.

The 2600-1 is pin compatible to the EA 4600, but outperforms it by nearly a 2:1 margin in access/cycle times. The Signetics 2600-1 also offers many other advantages over EA's part which will be discussed in the following paragraphs.

2600-1 BLOCK DIAGRAM

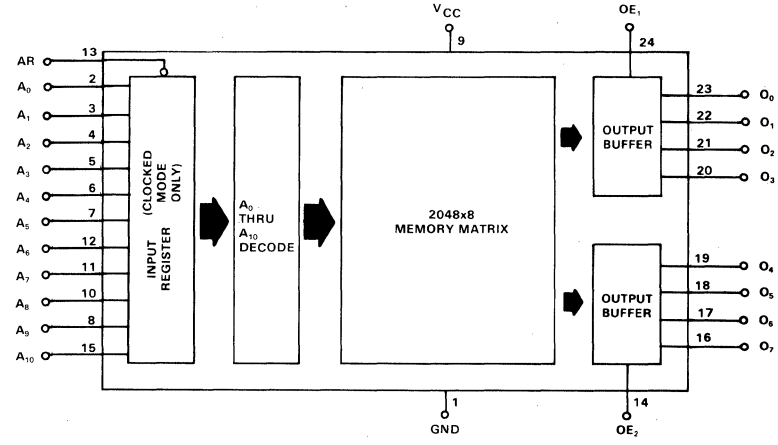


Figure 1

TECHNOLOGY ADVANTAGE

The 2600-1 is fabricated using the MOS n-channel silicon gate process in favor of metal gate to produce a smaller die size and a more reliable part. The Signetics proprietary version of the n-channel was developed to achieve the speed goal of 300ns access as the major speed distribution under worst case temperature, supply voltage and input/output voltage levels. Figure 3 is an illustration of the Signetics manufacturing process advantages.

PERFORMANCE ADVANTAGE

The Signetics 2600-1 is specified at 300ns maximum access/cycle compared with competition's 550ns access/500ns cycle. This means a 45 percent improvement in performance over the EA 4600 equivalent device, at the same maximum power consumption. What this means to the system designer is this:

1. More system timing margins for system currently designed to the EA 4600 ROM. Eliminates critical timing problems and "soft" errors due to worst case data settling times, crosstalk, and coincident timings where several timing pulse edges often line up during the access time to latch the data at the earliest possible time in order to meet system timings.
2. Upgrade current systems using the EA 4600 with the 2600-1 where the ROM is the gating item for performance. The instruction fetch time, for example, can be sped up by 45 percent for program store applications.
3. Anticipate future requirements for faster ROMs. Microprocessors, for example, are going to single +5V supply and becoming progressively faster. A ROM which covers this spectrum means fewer changes at the system level which ultimately translates into valuable development and design time savings and less dollars spent on qualification, documentation, design, etc.

2600-1 PIN CONFIGURATION

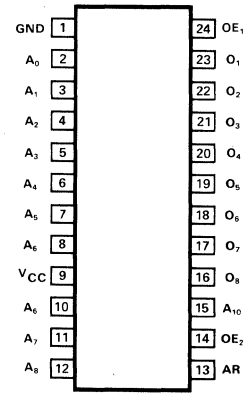
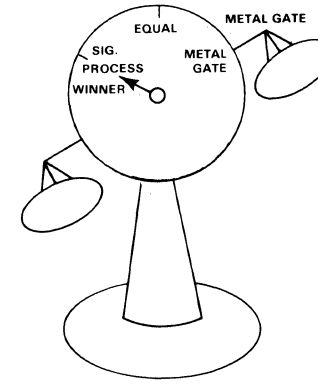


Figure 2

N-CHANNEL SILICON GATE TECHNOLOGY



ADVANTAGES

Smaller Die
Higher Yield
Lower Production Cost/Die
Better Reliability
Gate Oxide Protection
Self Aligning Gates
Lower Internal Capacitance

Figure 3

SPECIFICATION ADVANTAGE

Power Supply Requirements

The Signetics 2600-1, like the EA 4600, operates from a single +5V supply and both

specify the supply current I_{CC} = 115mA maximum. The big difference is the speed/power ratio. Table 1 shows this difference.

Normalized, this ratio becomes 1 for the Signetics 2600-1 and 1.8 for the EA 4600. The 2600-1 is, therefore, nearly two times more efficient with the same maximum power consumption of 603mW (115mA X 5.25V). To the system designer this means:

1. No change in power supply ratings is required when replacing or upgrading systems currently using EA 4600's with Signetics 2600-1's, although the most performance improvement is almost double that over EA's part.
2. Cost savings in implementing noise suppression techniques (additional bypass capacitors, bigger ground/power PC traces, and bus bars) where multiple ROM chips are employed for a given speed of operation.

Signetics 2600-1	$\frac{300ns}{115mA}$ = 2.6 = 1 normalized
EA 4600	$\frac{550ns}{115mA}$ = 4.78 = 1.8 normalized

Table 1 COMPARISON OF POWER SUPPLY REQUIREMENTS

	PARAMETER	SIGNETICS 2600-1	EA 4600	COMMENTS
AR_{PW}	Address read pulse width	100ns min.	300ns min.	Signetics 2600-1 is twice the speed.
T_{CYC}	Cycle time	300ns min.	500ns min.	Signetics 2600-1 is twice the speed.
T_{ACC}	Address to output delay	300ns max.	550ns max.	Signetics 2600-1 is 250ns faster.
T_{LD}	Address lead time	50ns min.	100ns min.	Signetics 2600-1 has 100ns margin over EA 4600.
T_{LG}	Address lag time	100ns min.	150ns min.	Signetics 2600-1 has 100ns margin over EA 4600.
T_{ARD}	Address read to output disturb	0ns min.	75ns min.	No timing skews

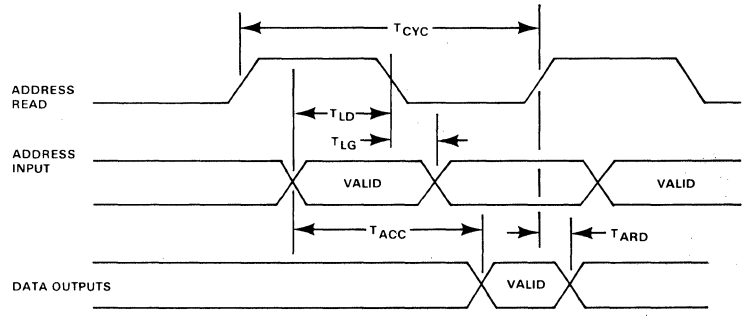
Table 2 CLOCKED MODE TIMING COMPARISON

Timing Requirements

The 2600-1 is capable of operation in the fully static unclocked mode or the clocked mode. The difference is that in clocked mode, the input address to the ROM is latched internally, controlled by the Address Read (AR) input signal, thereby holding the output data valid until the AR signal allows the next address to be propagated. If it is desired that the output data changes with the input addresses, the Address Read signal is not used and is tied to V_{CC}. It is also possible to operate in the clocked mode during other times by controlling the AR input signal.

1. *Clocked Mode*
   In the clocked mode of operation, the Address Read (AR) input signal controls the input address latches similar to a clock controlling a D-latch where the contents of this set of latches (the address) selects the corresponding eight bits of data which become out 0 through out 7. As long as AR is held high, the input addresses are allowed to propagate through the latches. If the addresses change, the address latches will reflect this change and the selection of the corresponding data bits begins. However, when AR is brought to the low level, the addresses are latched to the state of the address lines prior to the negative transition of AR. There are minimum set-up and hold time requirements indicated by TLD (address lead time) and TLG (address lag time). They are the minimum times the address must be valid before and after the falling edge of the AR signal. The 2600-1 requires TLD of 50ns and TLG of 100ns compared to EA's 100ns and 150ns, respectively. This means that for the address to be latched (thereby the output data is effectively latched) it need only be present in a given cycle for 150ns compared to EA's requirement of 250ns. This frees up the address bus for an extra 100ns where other operations may take advantage of the bus. A timing diagram for the clocked mode is shown in Figure 4, while Table 2 is a competitive comparison.

CLOCKED MODE TIMING



DEFINITIONS

1. T_{CYC} Cycle Time—The time between successive address read pulses.
2. T_{LD} Address Lead Time—The minimum time required for the address to be valid prior to the falling edge of the AR pulse.
3. T_{LG} Address Lag Time—The minimum amount of the time required for address to remain valid after the falling edge of the AR pulse.
4. T_{ARD} Address Read to Output Disturb Delay—The minimum time between the AR pulse and the first output transition when a new address is present.

Figure 4

The clocked mode is useful when cycle time is greater than the minimum cycle where, for example, in common bussed lines it is desirable to free the bus up as quickly as possible so that it may be used to initiate another device between memory accesses. Using the ROM in the clocked mode therefore eliminates the need for a set of input address latches.

2. *Unclocked Mode*
   The 2600-1 is fully static allowing it to be operated in the unclocked mode. That is, the output data always reflects the stored data at the address location of the input address delayed by the access time when the address is valid for the minimum specified time. The AR input is held high when it is desired to operate in the unclocked mode.

   The Signetics 2600-1 output will become valid 300ns from address valid. There is no timing skew between the minimum cycle and the maximum access times. Figure 5 shows the unclocked mode timing diagram and Table 3 presents a competitive comparison.

Output Flexibility

The 2600-1 is configured as a 2048X8 bits memory, however because there are separate output enable control signals for the lower and upper 4 bits of data out, the corresponding output lines may be OR-tied to achieve a 4096X4-bit organization. The output enable signals (OE_1 and OE_2) are then used as A_{11} and $\overline{A}_{11}$. Figure 6 illustrates the 4096X4 organization.

For applications that require the 8 bits of output data to be multiplexed onto a 4-bit bus, the Output Enable signal (OE_1 and OE_2) must be timed serially so as not to garble the output data. Figure 7 illustrates the 2048X8 organization.

Figure 8 shows the turn-on and turn-off timing diagrams. The turn-on and the turn-off delay times dictate the minimum time required to strobe data onto the bus.

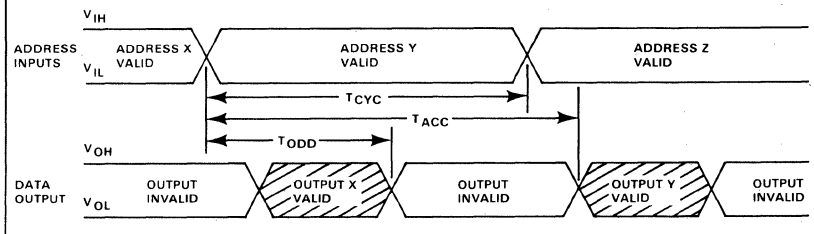
It is desirable to have as quick a response as possible in order to minimize these overhead delays.

The 2600-1 has 550ns (TCO + 2 TDO) of overhead while the EA 4600 has 100ns of overhead. The bus is in an indeterminable state during this time period and cannot be used to transmit information.

	PARAMETER	SIGNETICS 2600-1	EA 4600	COMMENTS
T_{ACC}	Address to output delay	300ns max.	500ns max.	Signetics 2600-1 is 200ns faster.
T_{CYC}	Cycle time	300ns min.	500ns min.	Signetics 2600-1 is twice the speed.
T_{ODD}	Output disturb delay	0ns min.	75ns min.	

Table 3 UNCLOCKED MODE TIMING COMPARISON

UNCLOCKED MODE TIMING DIAGRAM (AR TIED TO V_{CC})



DEFINITIONS

1. T_{CYC} Cycle Time—The time between application of successive addresses.
2. T_{ACC} Address to Output Delay Time—The maximum time between a new valid address and the corresponding valid output.
3. T_{ODD} Output Disturb Delay—The minimum time between the address change and the first output transition.

Figure 5

4096X4 CONNECTION DIAGRAM

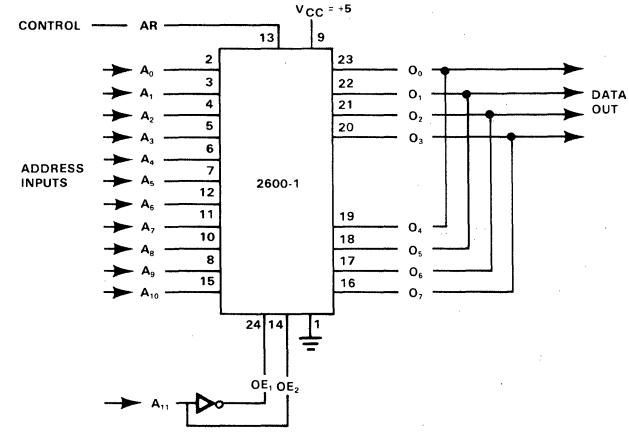


Figure 6

2048 X 8 MULTIPLEXED ONTO A 4-BIT BUS

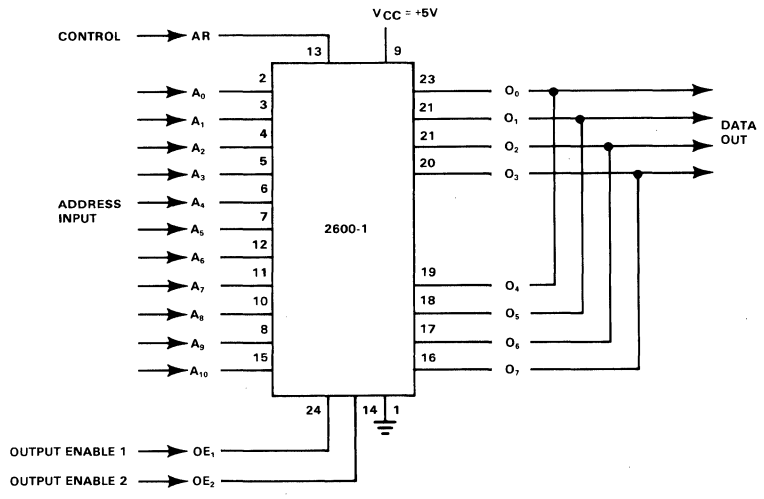


Figure 7

TURN-ON/TURN-OFF TIMING DIAGRAMS

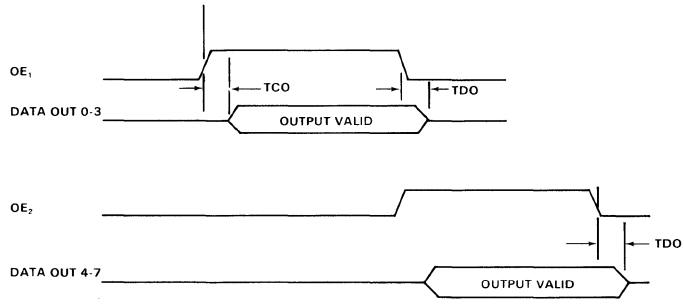


Figure 8

PARAMETER	SIGNETICS 2600-1	EA 4600	COMMENTS
Technology	N-channel, silicon gate	N-channel, metal	Smaller, more reliable die with Signetics process
Performance Access	300ns	550ns	Signetics 2600-1 is nearly two times faster than EA's 4600.
Cycle	300ns	500ns	
Power Supply	+5V	+5V	Both are fully TTL compatible
Power Consumption	603mW max.	603mW max.	Signetics' 2600-1 has the same power consumption with twice the performance.
Output Delay			
TCO	150ns max.	300ns max.	Signetic's 2600-1 has less overhead time.
TDO	200ns max.	400ns max.	Faster throughout for OR-tied multiple 8-bit output

Table 4 SIGNETICS 2600-1 VERSUS EA 4600—SUMMARY

DESCRIPTION

The Signetics 2616 is a 16,384-bit static MOS read-only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single 5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

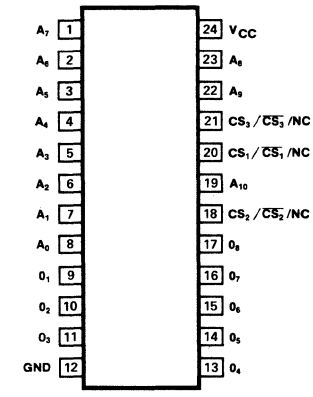
The 2616 read-only memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single 5V power supply is needed and all devices are directly TTL compatible.

FEATURES

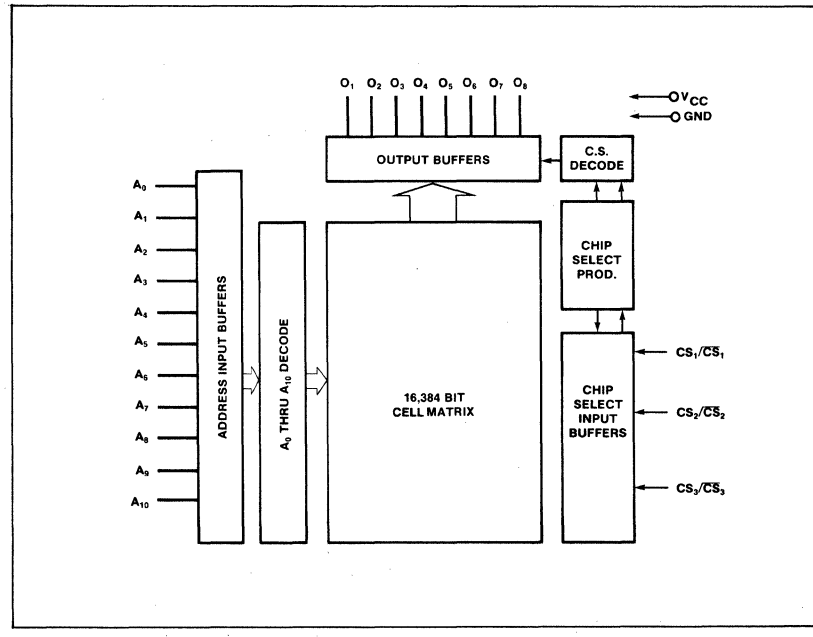
- **Single 5V power supply**
- **Guaranteed 350/450ns access time**
- **Directly TTL compatible—all inputs and outputs**
- **Three programmable chip select inputs for easy memory expansion or no connection option**
- **Three-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
	Supply voltage to ground potential	-0.5 to 7	V
	Applied voltage		V
	Input	-0.5 to 7	
	Output	-0.5 to 7	
P_D	Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[2]					V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage	V_{CC} = 4.75V				V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4		V_{CC}	
I_{LI}	Input load current	V_{CC} = 5.25V, OV ≤ V_{IN} ≤ 5.25V			10	μA
I_{LO}	Output leakage current	Chip deselected, V_{OUT} = 0.4V to V_{CC}			10	μA
I_{CC}	Supply current	Output unloaded, T_A = 25°C, V_{CC} = 5.25V, V_{IN} = V_{CC}			115	mA
	Capacitance[3]	T_A = 25°C, f = 1.0MHz, all pins except pin under test tied to ac ground				pF
C_{IN}	Input				7	
C_O	Output				10	

AC ELECTRICAL CHARACTERISTICS

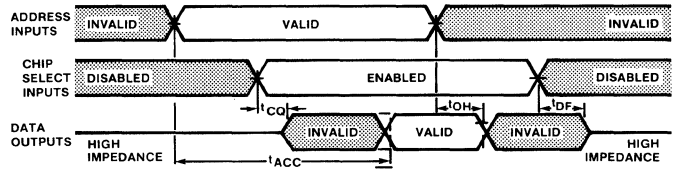
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

PARAMETER		2616			2616-1			UNIT
		Min	Typ	Max	Min	Typ	Max	
t_{ACC}	Address access time			450			350	ns
t_{CO}	Chip select delay			200			150	ns
t_{DF}	Chip deselect delay			200			150	ns
t_{OH}	Previous data valid after address change delay	20			20			ns

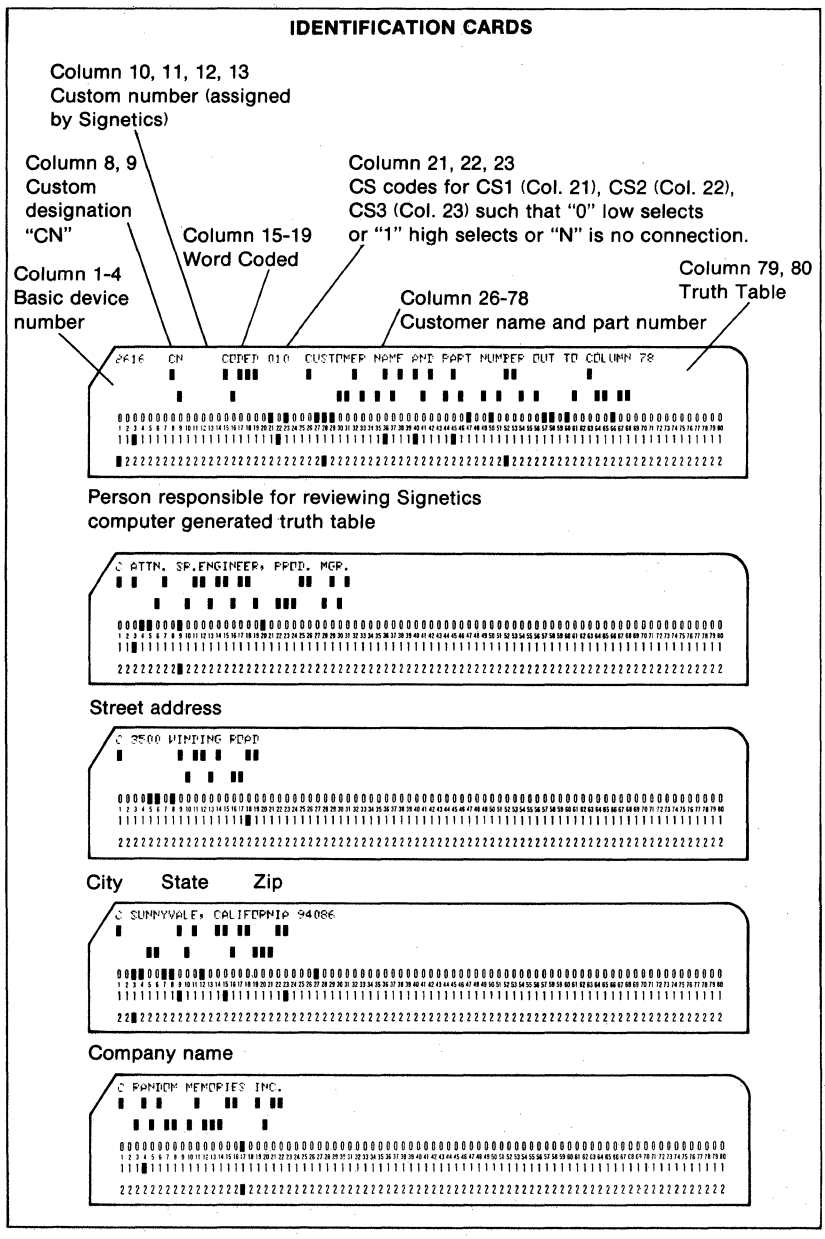
NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



CARD FORMAT



PROGRAMMING INSTRUCTIONS

2616

All Signetics Read Only Memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern is supplied on standard 80 column computer cards in the format described below.

All address and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of:

A. Title card
B. Comment cards
C. Data cards

For the user's convenience the data cards consisting of address and bit patterns can be specified in any one of three formats:

1. The hexadecimal format, where each data card carries (in hexadecimal) the initial input address for the 32 output words contained on that card, the 32 output words themselves (in hexadecimal) and the ROM truth table number. An N word ROM, therefore, requires n/32 cards, with all 32 output words defined on each card.
2. The octal format, where each data card carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the ROM truth table number. An N word ROM, therefore, requires N/16 cards, with all 16 output words defined on each card.
3. The binary format, where each data card carries (in decimal) the initial input address for the 8 output words contained on that card, the 8 output words themselves (in binary) and the ROM truth table number. An N word ROM, therefore, requires N/8 cards, with all 8 output words defined on each card.

Positive logic is used on all input cards; a logic "1" is the most positive voltage level and a logic "0" is the most negative level.

Title Card

COLUMN	INFORMATION
1-4	Signetics Part Number, that is, 2600, 2616, 2620, etc.
7-13	Leave blank _____ Pattern Number to be assigned by Signetics.
15-19	Punch the letters "CODED"
21	CS1/$\overline{CS1}$/NC Chip Select Logic Level (If low selects chip, punch "0"; if high selects chip, punch "1"; if no connection, punch "N".)

PROGRAMMING INSTRUCTIONS

2616 (Cont'd)

22	CS2/$\overline{CS2}$/NC Chip Select Logic Level
23	CS3/$\overline{CS3}$/NC Chip Select Logic Level
26-78	Customer Identification
79-80	ROM Truth Table Number (may be left blank)

Comment Cards

Any number of comment cards may be used for specifying the user's name, telephone number, address, any special instructions, etc. On these cards the letter "C" must be punched in column 1 and comments can be punched in columns 2-80.

Hexadecimal Format Data Cards

COLUMN	INFORMATION
1-5	Hexadecimal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 00000, 00020, 00040, etc.
7-8	Hexadecimal equivalent of the binary output data (O_0 = LSB) for initial input address. EXAMPLE: Column 7 is upper 4 bits.

```
0      0
7----0

10100101

  A    5
  ↑    ↑
Col. 7  Col. 8
```

9-10	Output data for initial input address +1.
11-12	Output data for initial input address +2.
⋮	⋮
67-68	Output data for initial input address +30.
69-70	Output data for initial input address +31.
79-80	ROM truth table number (may be left blank)

Octal Format Data Cards

COLUMN	INFORMATION
1-4	Octal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 0000, 0020, 0040, etc.
5-7	Octal equivalent of the binary output data (O_0 = LSB) for initial input address. EXAMPLE:

```
0      0
7----0

10100101

  2  4  5

Col. 5 ↑     ↑ Col. 7
       ↑
    Col. 6
```

8-10	Output data for initial input address +1.
11-13	Output data for initial input address +2.
⋮	⋮
47-49	Output data for initial input address +14.
50-52	Output data for initial input address +15.
79-80	ROM truth table number (may be left blank).

Binary Format Data Cards

COLUMN	INFORMATION
1-5	Decimal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 00000, 00008, 00016, etc.
7-14	Binary output data (O_0 = LSB) for initial input address. Output data can also be punched with a "P" or an "N" instead of a "1" or a "0," respectively.

```
0      0
7------0

10100101

Col. 7 ↑     ↑ Col. 14
```

16-23	Output data for initial input address +1.
25-32	Output data for initial input address +2.
34-41	Output data for initial input address +3.
43-50	Output data for initial input address +4.
52-59	Output data for initial input address +5.
61-68	Output data for initial input address +6.
70-77	Output data for initial input address +7.
79-80	ROM truth table number (may be left blank).

DESCRIPTION

The Signetics 2617 is a 16,384-bit static MOS read-only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single 5V power supply. The two chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These two programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitate easy memory expansion.

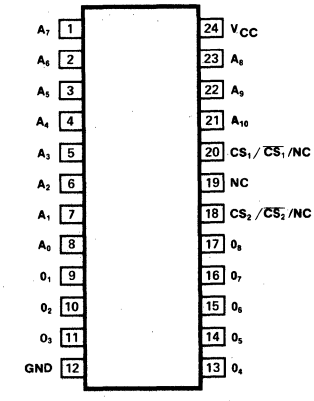
The 2617 read-only memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single 5V power supply is needed and all devices are directly TTL compatible.

FEATURES

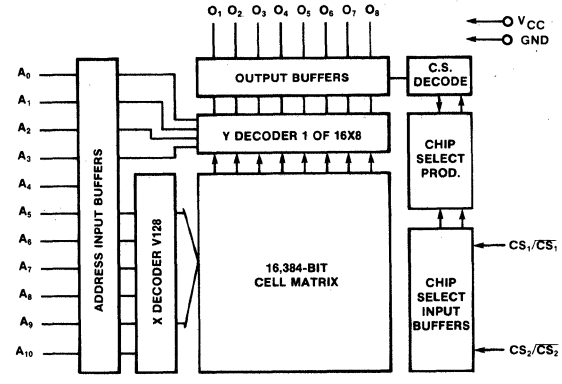
- **Single 5V power supply**
- **Guaranteed 350/450ns access time**
- **Directly TTL compatible—all inputs and outputs**
- **Two programmable chip select inputs for easy memory expansion or no connection option**
- **Three-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
	Supply voltage to ground potential	-0.5 to 7	V
	Applied voltage		V
	Input	-0.5 to 7	
	Output	-0.5 to 7	
P_D	Power dissipation	1	W

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[2]					V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage	V_{CC} = 4.75V				V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4		V_{CC}	
I_{LI}	Input load current	V_{CC} = 5.25V, OV ≤ V_{IN} ≤ 5.25V			10	μA
I_{LO}	Output leakage current	Chip deselected, V_{OUT} = 0.4V to V_{CC}			10	μA
I_{CC}	Supply current	Output unloaded, T_A = 25°C, V_{CC} = 5.25V, V_{IN} = V_{CC}			115	mA
	Capacitance[3]	T_A = 25°C, f = 1.0MHz, all pins except pin under test tied to ac ground				pF
C_{IN}	Input				7	
C_O	Output				10	

AC ELECTRICAL CHARACTERISTICS

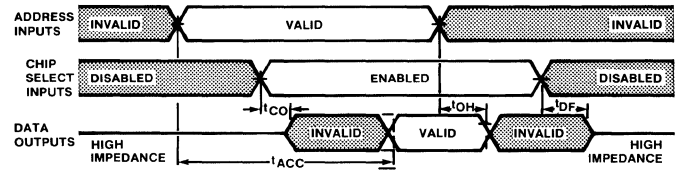
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

PARAMETER		2617			2617-1			UNIT
		Min	Typ	Max	Min	Typ	Max	
t_{ACC}	Address access time			450			350	ns
t_{CO}	Chip select delay			200			150	ns
t_{DF}	Chip deselect delay			200			150	ns
t_{OH}	Previous data valid after address change delay	20			20			ns

NOTES

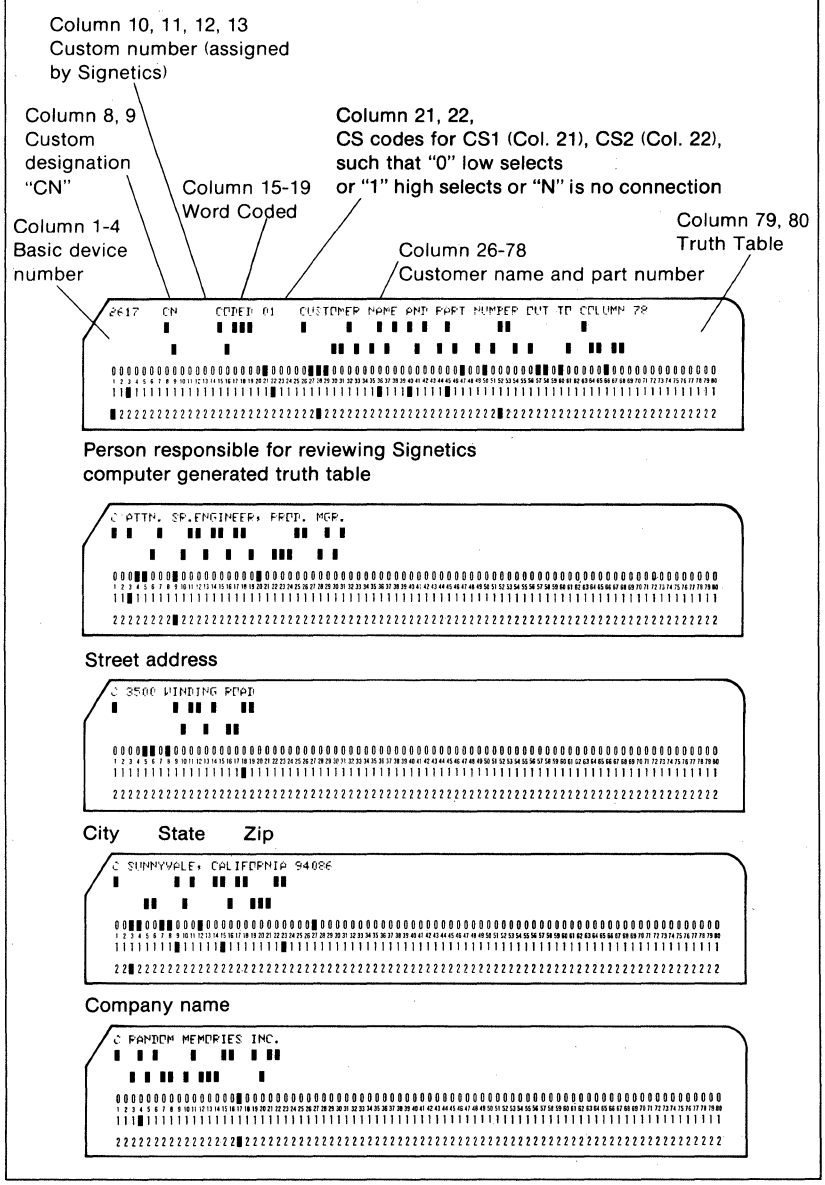
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



CARD FORMAT

IDENTIFICATION CARDS



PROGRAMMING INSTRUCTIONS

2617

All Signetics Read Only Memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern is supplied on standard 80 column computer cards in the format described below.

All address and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of:

A. Title card
B. Comment cards
C. Data cards

For the user's convenience the data cards consisting of address and bit patterns can be specified in any one of three formats:

1. The hexadecimal format, where each data card carries (in hexadecimal) the initial input address for the 32 output words contained on that card, the 32 output words themselves (in hexadecimal) and the ROM truth table number. An N word ROM, therefore, requires N/32 cards, with all 32 output words defined on each card.
2. The octal format, where each data card carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the ROM truth table number. An N word ROM, therefore, requires N/16 cards, with all 16 output words defined on each card.
3. The binary format, where each data card carries (in decimal) the initial input address for the 8 output words contained on that card, the 8 output words themselves (in binary) and the ROM truth table number. An N word ROM, therefore, requires N/8 cards, with all 8 output words defined on each card.

Positive logic is used on all input cards; a logic "1" is the most positive voltage level and a logic "0" is the most negative level.

Title Card

COLUMN	INFORMATION
1-4	Signetics Part Number, that is, 2600, 2616, 2620, etc.
7-13	Leave blank ____ Pattern Number to be assigned by Signetics.
15-19	Punch the letters "CODED"
21	CS1/$\overline{CS1}$/NC Chip Select Logic Level (If low selects chip, punch "0"; if high selects chip, punch "1"; if no connection, punch "N".)

PROGRAMMING INSTRUCTIONS

2617 (Cont'd)

22	CS2/$\overline{CS2}$/NC Chip Select Logic Level
26-78	Customer Identification
79-80	ROM Truth Table Number (may be left bank)

Comment Cards

Any number of comment cards may be used for specifying the user's name, telephone number, address, any special instructions, etc. On these cards the letter "C" must be punched in column 1 and comments can be punched in columns 2-80.

Hexadecimal Format Data Cards

COLUMN	INFORMATION
1-5	Hexadecimal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 00000, 00020, 00040, etc.
7-8	Hexadecimal equivalent of the binary output data (O_0 = LSB) for initial input address. EXAMPLE: Column 7 is upper 4 bits.

```
0      0
7------0

10100101
 ‾‾ ‾‾
 A  5
 ↑  ↑
Col. 7  Col. 8
```

9-10	Output data for initial input address +1.
11-12	Output data for initial input address +2.
⋮	⋮
67-68	Output data for initial input address +30.
69-70	Output data for initial input address +31.
79-80	ROM truth table number (may be left blank)

Octal Format Data Cards

COLUMN	INFORMATION
1-4	Octal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 0000, 0020, 0040, etc.
5-7	Octal equivalent of the binary output data (O_0 = LSB) for initial input address. EXAMPLE:

```
0      0
7------0

10100101
 ‾‾‾ ‾‾‾
 2 4 5

Col. 5 ↑      ↑ Col. 7
       ↑
    Col. 6
```

8-10	Output data for initial input address +1.
11-13	Output data for initial input address +2.
⋮	⋮
47-49	Output data for initial input address +14.
50-52	Output data for initial input address +15.
79-80	ROM truth table number (may be left blank).

Binary Format Data Cards

COLUMN	INFORMATION
1-5	Decimal equivalent of the binary input address (A_0 = LSB). This is the initial input address and is punched right justified, that is, 00000, 00008, 00016, etc.
7-14	Binary output data (O_0 = LSB) for initial input address. Output data can also be punched with a "P" or an "N" instead of a "1" or a "0", respectively.

```
0      0
7------0

10100101

Col. 7 ↑      ↑ Col. 14
```

16-23	Output data for initial input address +1.
25-32	Output data for initial input uddress +2.
34-41	Output data for initial input address +3.
43-50	Output data for initial input address +4.
52-59	Output data for initial input address +5.
61-68	Output data for initial input address +6.
70-77	Output data for initial input address +7.
79-80	ROM truth table number (may be left blank).

2513-I,N

FEATURES

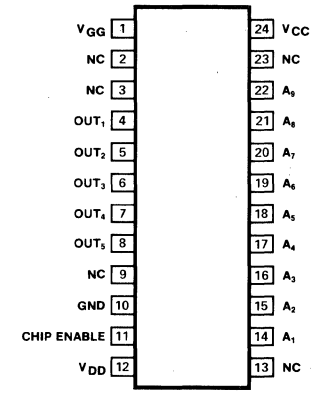
- **Standard 7X5 dot matrix fits well**
- **TTL level interface signals**
- **Tri-state outputs**
- **Direct, low cost interfacing with TTL, DTL, CMOS and Signetics MOS 2500 series**

TRUTH TABLE

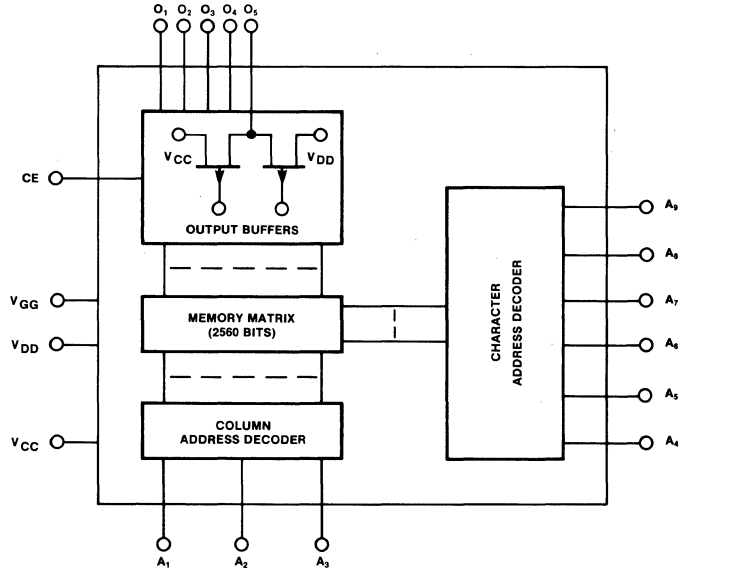
CE	OUTPUT
0	Data
1	Open

PIN CONFIGURATION

I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C[2]	730	mW
	Input[3] and supply voltages with respect to V_{CC}	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$ unless otherwise specified.[4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[8]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
	Output voltage	One TTL load				V
V_{OL}	Low		-5		0.4	
V_{OH}	High		3.0			
I_{LI}	Input load current	$V_{IN} = -5.5V$, $T_A = 25°C$		10	500	nA
I_{LO}	Output leakage current	$V_{OUT} = -5.5V$, $T_A = 25°C$, $V_{CE} = V_{CC}$		10	1000	nA
	Supply current	Outputs open				mA
I_{DD}	V_{DD}			12	15	
I_{GG}	V_{GG}	$V_{CE} = V_{CC}$		10	25	
	Capacitance					pF
C_{IN}	Address input	f = 1MHz, $V_{IH} = V_{CC}$, 25mV p-p			10	

AC ELECTRICAL CHARACTERISTICS

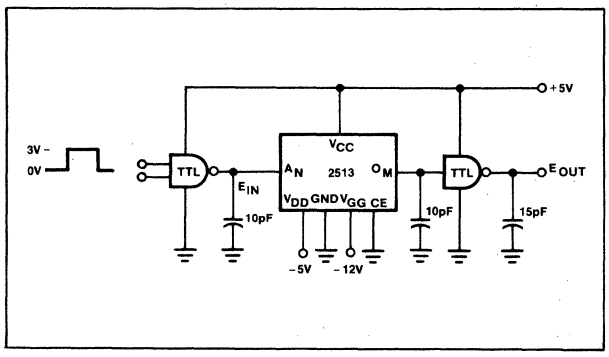
$T_A = 0°C$, to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Access time			See ac test setup				ns
t_{CA}	Character (CM2140)					500	600	
t_{RA}	Row (A_1-A_3)					450	500	
t_{CE}		Output	Chip enable			150		

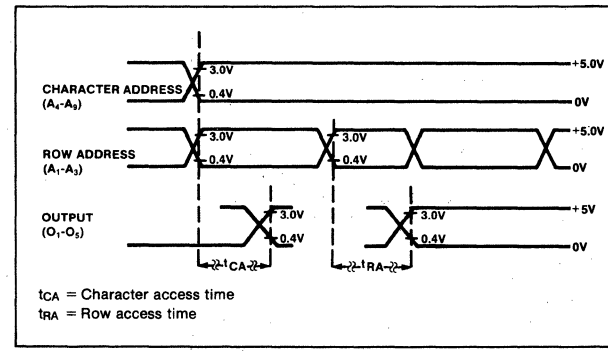
NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values at +25°C and typical supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC}$ -1.85V and $V_{IL} = V_{CC}$ -4.15V.

TEST LOAD CIRCUIT



TIMING DIAGRAM



t_{CA} = Character access time
t_{RA} = Row access time

MOS MEMORY

CHARACTER FORMAT

ROW ADDRESS

ROW ADDRESS			OUTPUTS				
A_3	A_2	A_1	O_5	O_4	O_3	O_2	O_1
0	0	0	0	0	0	0	0
0	0	1	0	1	1	1	0
0	1	0	1	0	0	0	1
0	1	1	1	0	0	0	0
1	0	0	0	1	1	1	0
1	0	1	0	0	0	0	1
1	1	0	1	0	0	0	1
1	1	1	0	1	1	1	0

EXAMPLE 'S'

CHARACTER ADDRESS

	COLUMN ADDRESS					
	A_4	A_5	A_6	A_7	A_8	A_9
ASCII CHARACTER	1	1	0	0	1	0

ORGANIZATION AS CHARACTER GENERATOR

A 6-bit binary address (A_4-A_9) selects 1-of-64 matrix characters arranged 5 dots horizontally and 8 dots vertically. A 3-bit binary address code (A_1-A_3) selects 1 of 8 rows. Five outputs display a complete row of the character matrix (see Row Address Character Format). The devices may also be used in pairs to provide 9X7 and 10X8 vertical scan formats.

ORGANIZATION AS ROM

For a straight 512X5 ROM, the 5 outputs will display any one of 512 5-bit stored words corresponding to a 9-bit address applied to A_1-A_9.

CUSTOM DEVICES

For unique custom memory patterns, this form should be used to transmit coding instructions. The nomenclature for a custom device will consist of the basic product type followed by a unique CM number assigned by Signetics, i.e, 2513N/CM2141.

- Programming with punched cards:
  For maximum accuracy and minimum cost and turn-around time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.

VERIFICATION

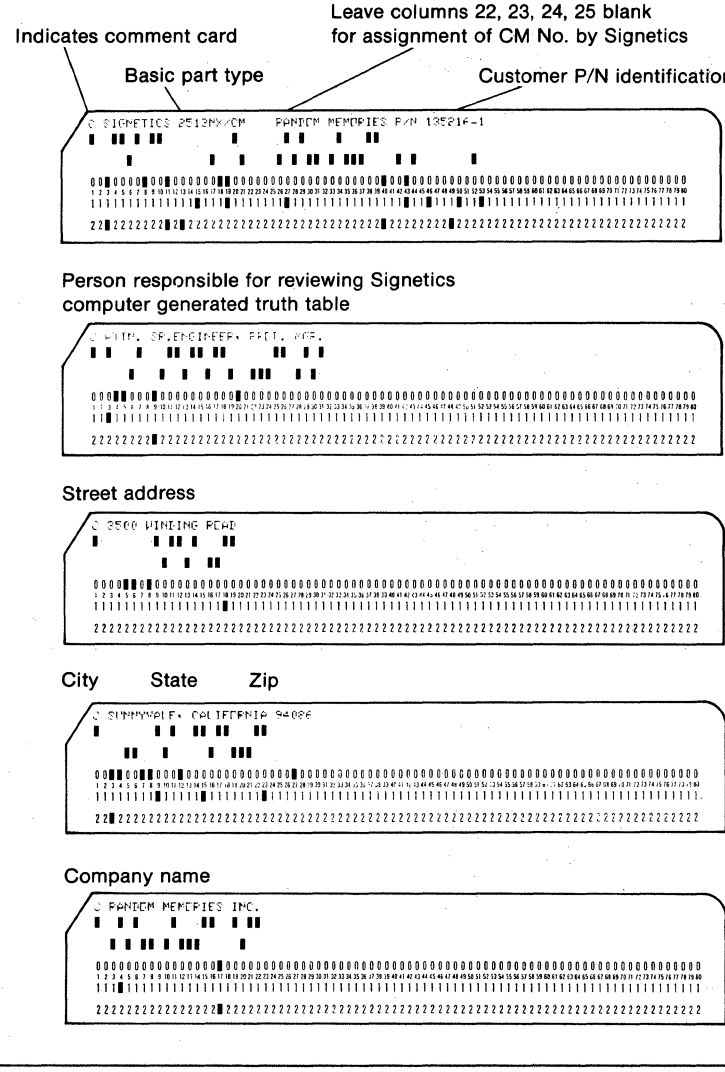
Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

Logic "1"s or blackened squares in the truth table will result in high output from the indicated output terminal, i.e., 3.2V minimum. Similarly, a "1" address input level is interpreted as 3.2V minimum.

CARD FORMAT

IDENTIFICATION CARDS

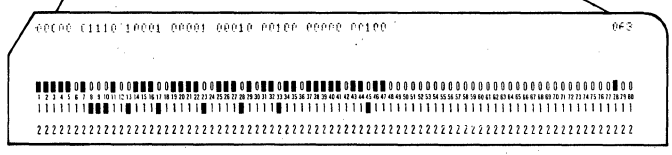


CARD FORMAT (Cont'd)

DATA CARDS

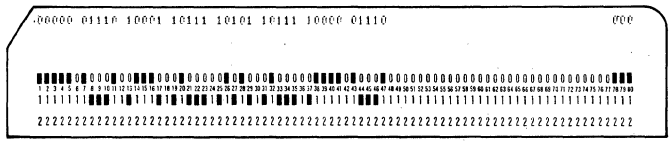
Outputs O_5 — O_1 respectively

Character number
(Data card number)



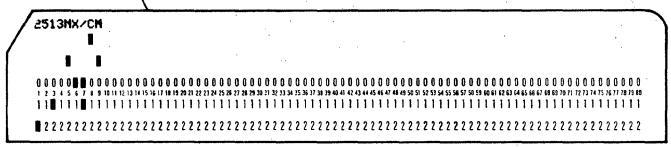
Row address

000 001 010 011 100 101 110 111



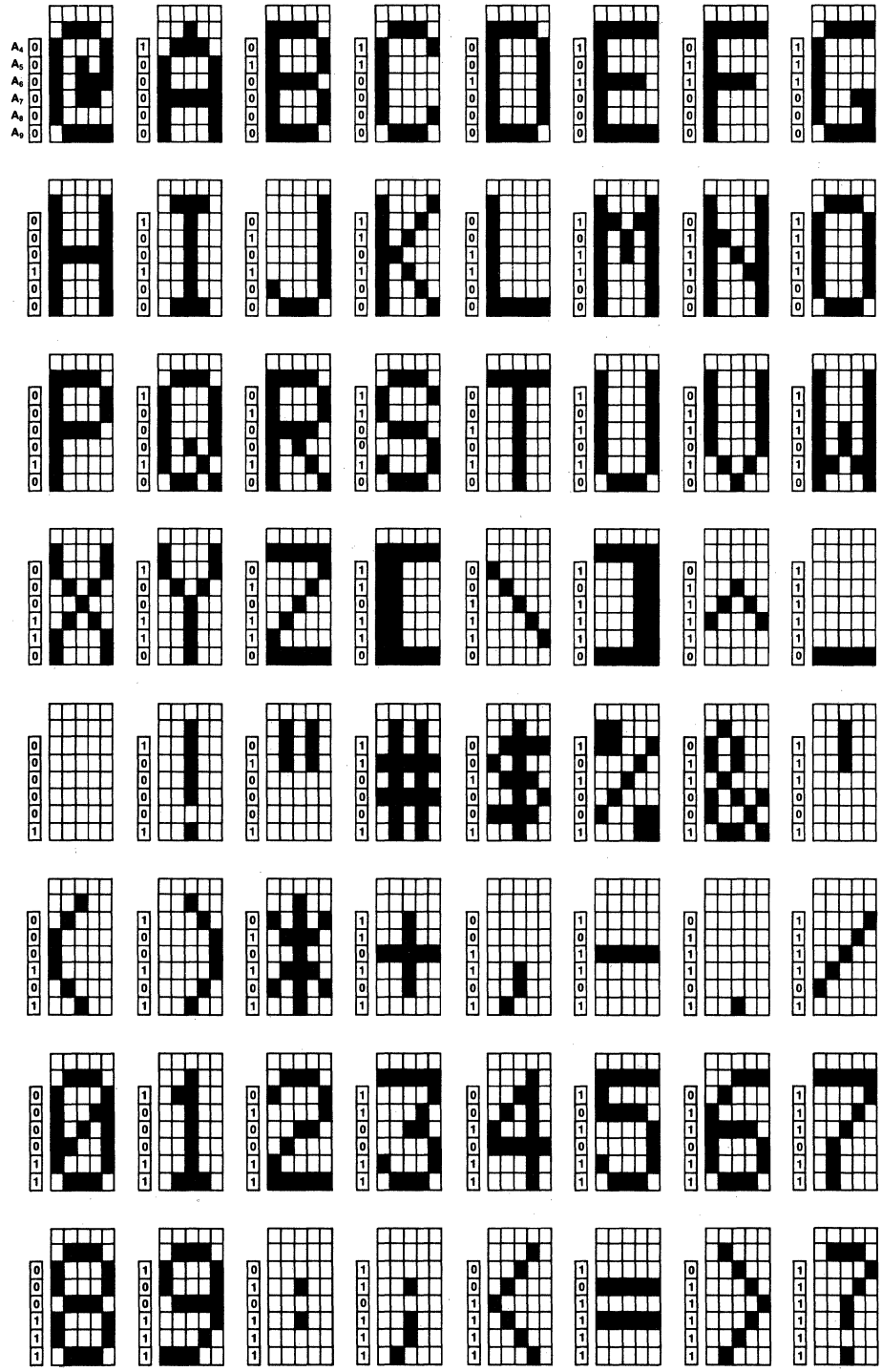
Basic device type

Leave columns 10, 11, 12, 13 blank for assignment of CM No. by Signetics



Character number is in columns 78, 79 and 80. Note that each group of 5-bit words is treated as a character for convenience of coding.

ASCII CHARACTER FONT



For upper case order CM2140; For lower case order CM3021.

2516-I,N

FEATURES

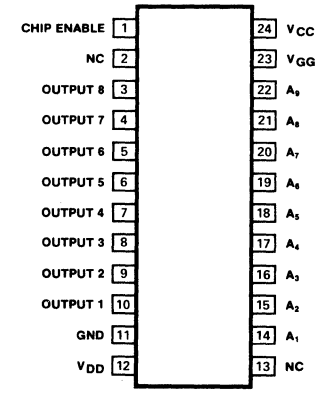
- **5V TTL level input signals**
- **Tri-state outputs**
- **Direct, low cost interfacing with TTL, DTL and Signetics MOS 2500 series**

TRUTH TABLE

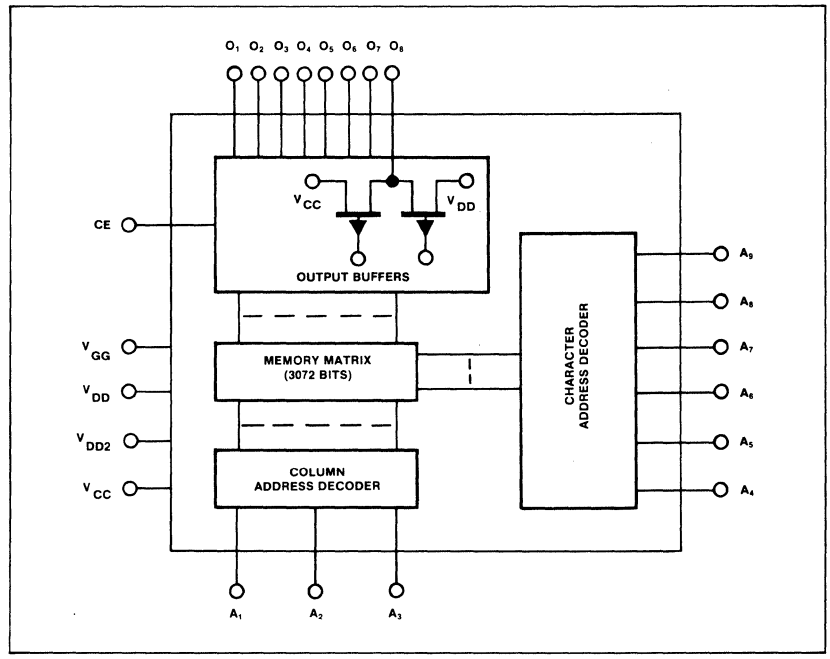
CE	OUTPUT
0	Data
1	Open

PIN CONFIGURATION

I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at 70°C[2]	730	mW
	Input[3] and supply voltages with respect to V_{CC}	0.3 to -20	V

MOS MEMORY

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = -5V ± 5%, V_{GG} = -12V ± 5% unless other noted.[4,5,6,7]

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage[8]					V
V_{IL}	Low		-5		0.6	
V_{IH}	High		3.4		5.3	
	Output voltage[9]					V
V_{OL}	Low	I_{OL} = 1.6mA	-5		0.5	
V_{OH}	High	I_{OH} = 100μA	3.8			
I_{LI}	Input load current	V_{IN} = -5.5V, T_A = 25°C		10	500	nA
I_{LO}	Output leakage current	V_{OUT} = -5.5V, T_A = 25°C, V_{CE} = V_{CC}		10	1000	nA
	Supply current	Outputs open				mA
I_{DD}	V_{DD}			14	21	
I_{GG}	V_{GG}			8	12	
	Capacitance					pF
C_{IN}	Address input	f = 1MHz, V_{IH} = V_{CC}, 25mV p-p			10	

AC ELECTRICAL CHARACTERISTICS

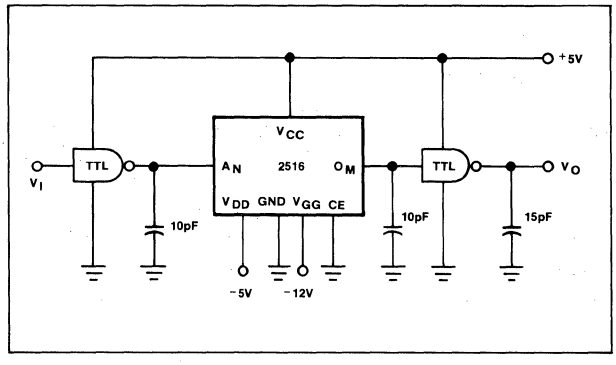
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = -5V ± 5%, V_{GG} = -12V ± 5%, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Access time	See test load circuit				ns
t_{CA}	Character			500	600	
t_{CLA}	Column (A_1-A_3)			400	500	

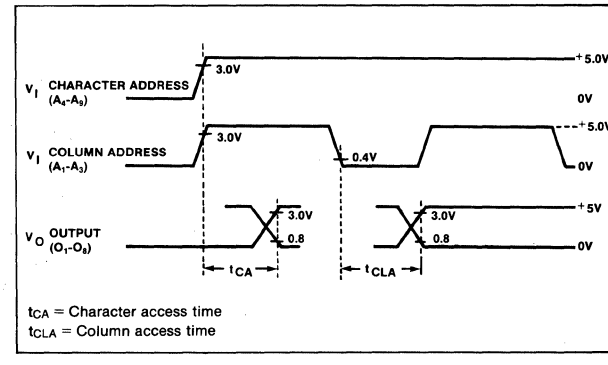
NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} -1.85V and V_{IL} = V_{CC} -4.15V.
9. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH}, which are stated for a V_{CC} of exactly 5V.

TEST LOAD CIRCUIT

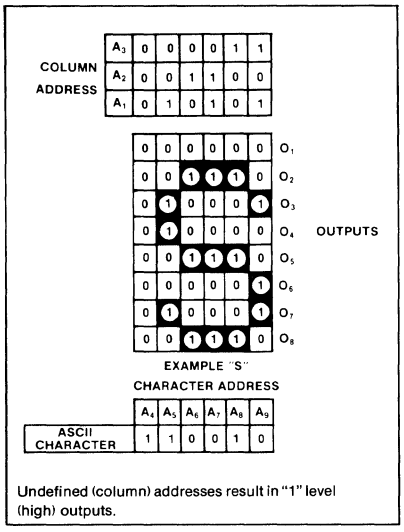


TIMING DIAGRAM



t_{CA} = Character access time
t_{CLA} = Column access time

CHARACTER FORMAT



Undefined (column) addresses result in "1" level (high) outputs.

APPLICATIONS DATA

Output Interfacing Notes

The tri-state outputs on this device exhibit 3 states:

1. "1" = Low impedance to +5V
2. "0" = Low impedance to -5V
3. Off = High impedance, 10m

The off state is controlled by the chip enable control input.

Custom ROM Organizations

The 2516 is a static ROM with a total 64X6X8-bit capacity. This allows a standard 5X7 font to be encoded in the ROM, e.g., the 2516/CM2150 ASCII font standard product. A custom coding configuration may make use of the full 6X8 dot matrix if desired.

ORGANIZATION AS CHARACTER GENERATOR

A 6-bit binary address (A_4-A_9) selects 1-of-64 matrix characters arranged 6 dots horizontally and 8 dots vertically. A 3-bit binary address code (A_1-A_3) selects 1 of 6 columns. Eight outputs display a complete column of the character matrix.

STANDARD PATTERN

A standard ASCII Character Font is available for the 2516. This device (2516N/CM2150) may be used for ASCII character generation or for device evaluation.

CUSTOM DEVICES

For unique custom memory patterns, the following formats should be used to transmit coding instructions. The nomenclature for each custom device will consist of the basic product type followed by a unique CM number assigned by Signetics, i.e., 2516N/CM2151.

- Programming with punched cards:
  For maximum accuracy and minimum cost and turn-around time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.
- Programming with written truth table:
  When punched data cards cannot be supplied, the truth table may be transmitted in written form using the attached blank truth table.

VERIFICATION

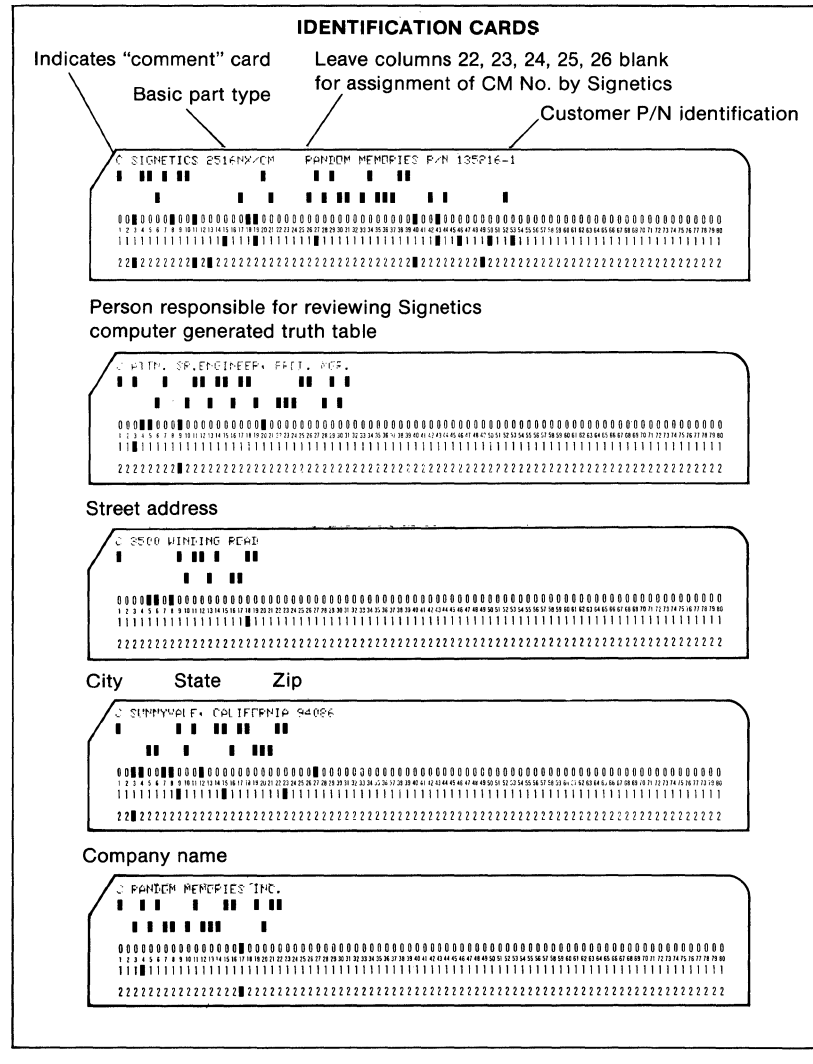
Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

Logic "1"s of blackened squares in the truth table will result in high output from the indicated output terminal, i.e., +3.6V minimum. Similarly, a "1" address input level is interpreted as +3.2V minimum.

Undefined addresses result in "1" level outputs.

CARD FORMAT

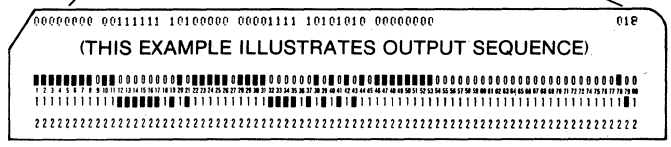


CARD FORMAT (Cont'd)

DATA CARDS

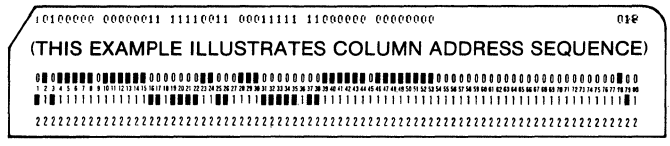
Outputs O_8 — O_1 respectively

Decimal character address
(Data card number 001 — 064)



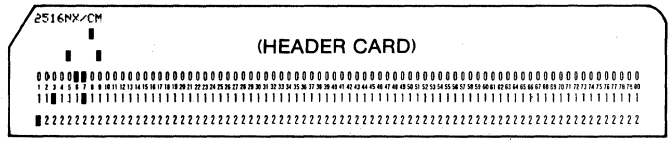
Column address (A_3,A_2,A_1)

000 001 010 011 100 101



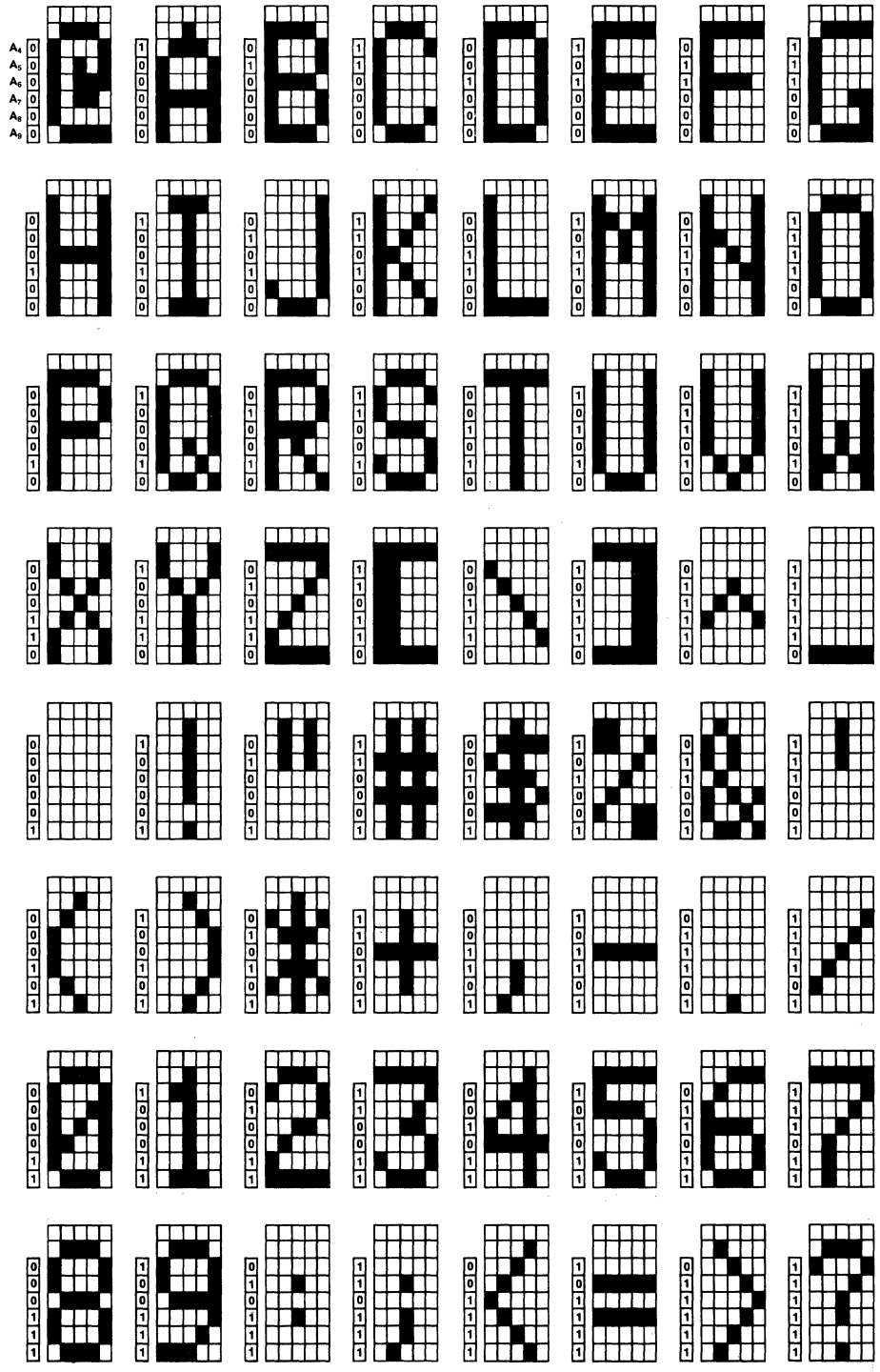
Basic device type

Leave columns 10, 11, 12, 13 blank for assignment of CM No. by Signetics



Character number is in columns 78, 79 and 80.

ASCII CHARACTER FONT



Excess addresses yield logic "1" outputs.

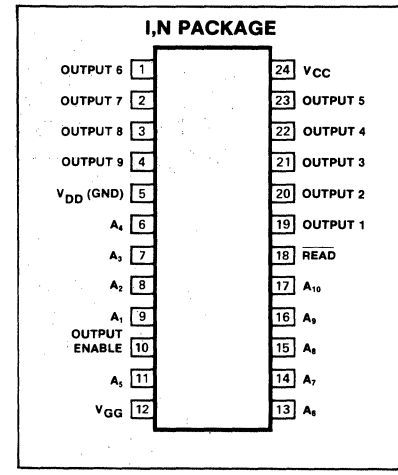
2526-I,N

DESCRIPTION

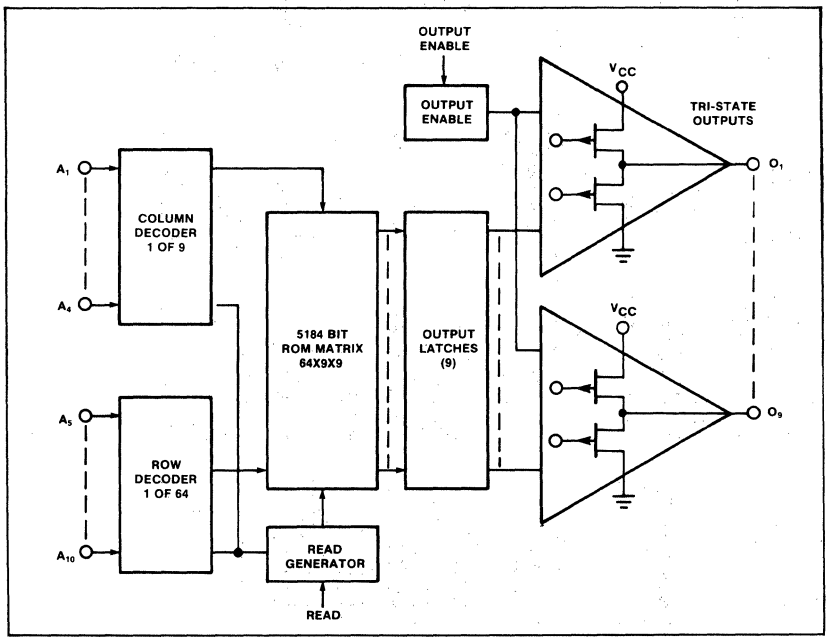
The 2526 high speed ROM may be organized as 64X9X9 for use as a character generator, or as a 512X9 ROM for general purpose use. A read input controls the entry of data from the ROM into output latches. Three-state outputs allow OR-tying for implementing large memories. Output enable controls the 9 output devices without affecting address circuitry.

PIN CONFIGURATION

I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
	Power dissipation at 70°C[2]	730	mW
	Input and supply voltages with respect to V_{CC}[3]	0.3 to -20	V

2526-I,N

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{GG} = -12V ± 5%, unless otherwise specified[4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[8]					V
V_{IL}	Low		-5		0.6	
V_{IH}	High		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.5	
V_{OH}	High	I_{OH} = 100μA	3.8			
I_{LI}	Input load current	V_{IN} = -5.5V, T_A = 25°C		10	500	nA
I_{LO}	Output leakage current	V_{OUT} = OV, T_A = 25°C, V_{CE} = V_{CC}		10	1000	nA
	Supply current[9]					mA
I_{CC}	V_{CC}			30	55	
I_{GG}	V_{GG}			30	55	
C_{IN}	Address input capacitance	f = 1MHz, V_{AC} = 25mV p-p, V_{IN} = V_{CC}			10	pF

AC ELECTRICAL CHARACTERISTICS

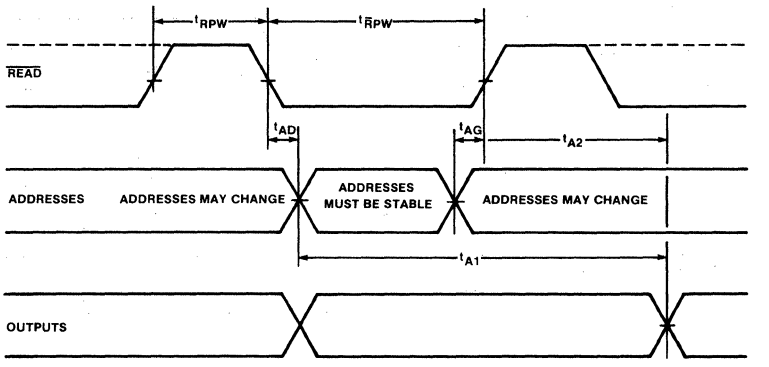
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{GG} = -12V ± 5% unless otherwise specified.

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Pulse width						ns
t_{RPW}	Read[10]			250	200		
$t_{\overline{R}PW}$	$\overline{\text{Read}}$[11]			500	400		
	Address time[12]						ns
t_{AD}	Delay	Address	$\overline{\text{Read}}$ low			50	
t_{AG}	Pulse gap	$\overline{\text{Read}}$ high	Address			50	
	Delay time						ns
t_{A1}[13]		Output	Address		625	700	
t_{A2}[13]		Output	End of read pulse		200	250	
t_{OE}		Output	Output enable		100	250	

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to 70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} - 1.85V and V_{IL} = V_{CC} - 4.15V.
9. Outputs open, t_{RPW} = 250ns, $t_{\overline{R}PW}$ = 500ns.
10. During t_{RPW1} addresses are decoded and sent to the memory matrix and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (rising edge) of the $\overline{\text{read}}$ pulse. After t_{A2}, data appears at the output terminals.
11. During t_{RPW1} data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
12. Addresses must be stable within 50ns after the $\overline{\text{read}}$ line falls and must remain stable until at least 50ns before the $\overline{\text{read}}$ line goes high.
13. t_A = 0°C to +70°C.

TIMING DIAGRAM



All times measured from 50% points.
tr = tf = 10ns or less

CUSTOM CODING INFORMATION

Data Card Format

I.D./COMMENT CARDS

Card No. 1

Columns	
1	C
2	Blank
3-17	SIGNETICS 2526N/CM
18-26	Blank
27-71	Customer I.D. (company, project, part no., etc.)
72	Blank
73-80	Date

Card No. 2

Columns	
1	C
2	Blank
3-80	Person responsible for reviewing Signetics truth table

Card No. 3

Columns	
1	C
2	Blank
3-80	Customer street address

Card No. 4

Columns	
1	C
2	Blank
3-80	Customer city, state, zip

Card No. 5

Columns	
1	C
2	Blank
3-80	Name

DATA CARDS

Card No. 1

Columns	
1-9	Binary outputs of rows 9 through 1 (MSB at 9), first column, first character (first character is 000), logic high is high output (3.2V min)
10	Blank
11-19	Binary outputs of second column, first character
20	Blank
21-29	Third column
30	Blank
31-39	Fourth column
40	Blank
41-49	Fifth column
50	Blank
51-59	Sixth column
60	Blank
61-69	Seventh column
70-71	Blank
72	Data card number of first character (1)
73	Blank
74-76	Anything—customer option
77	Blank
78-80	Decimal character number (000)

Card No. 2

Columns	
1-9	Eighth column
10	Blank
11-19	Ninth column
20-70	Anything—customer option
71	Blank
72	Data card number of first character (2)
73	Blank
74-76	Customer option
77	Blank
78-80	Decimal character number (000)

Card No. 3

Columns	
1-9	First column, second character, rows 9 through 1
(etc., as Card 1)	MSB at (9). Second character is 001.

Card No. 4

Columns	
(etc., as Card 2)	

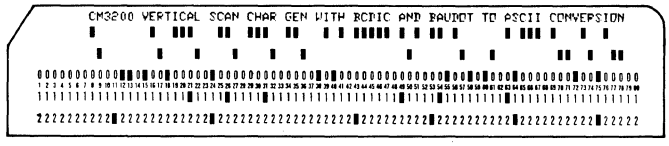
Card No. 128

Columns	
78-80	Decimal character number (063)

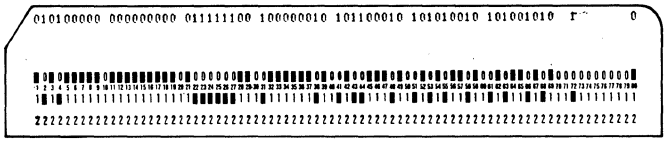
2526-I,N

EXAMPLES

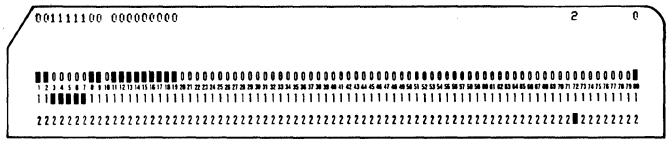
I.D. Card



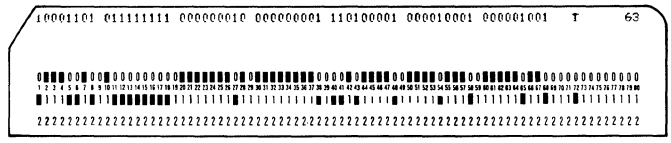
First Data Card—First Character



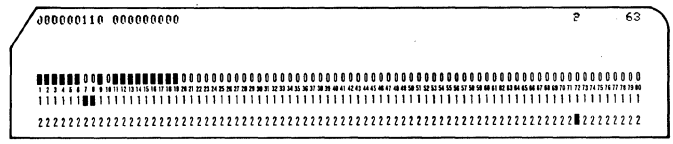
Second Data Card—First Character



First Data Card—Last Character



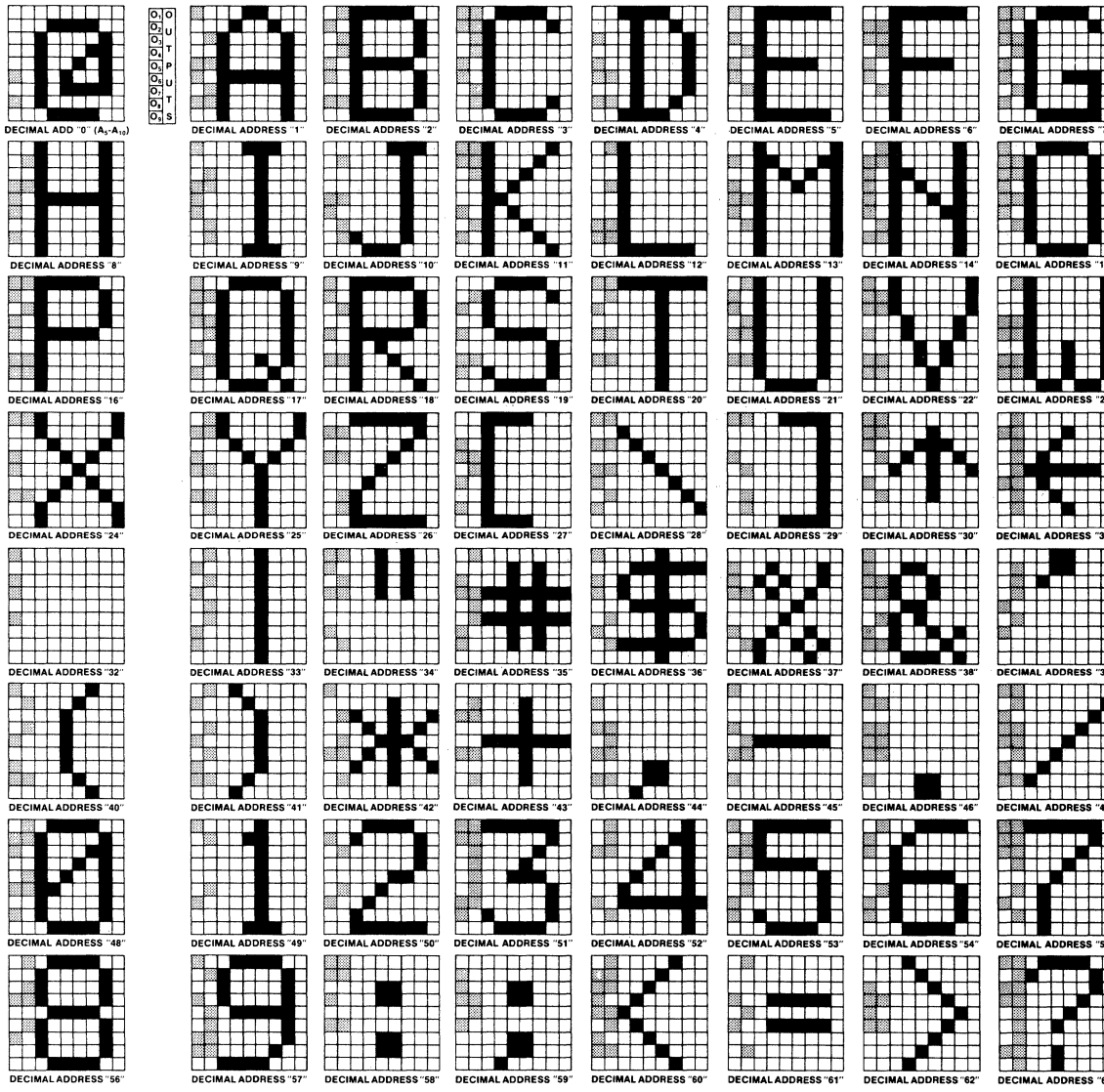
Second Data Card—Last Character



STANDARD CHARACTER FONTS

CM 3400
ASCII SET, VERTICAL SCAN 7X9 WITH CODE CONVERSION

COLUMN ADDRESSES									
A_1	0	1	0	1	0	1	0	1	0
A_2	0	0	1	1	0	0	1	1	0
A_3	0	0	0	0	1	1	1	1	0
A_4	0	0	0	0	0	0	0	0	1

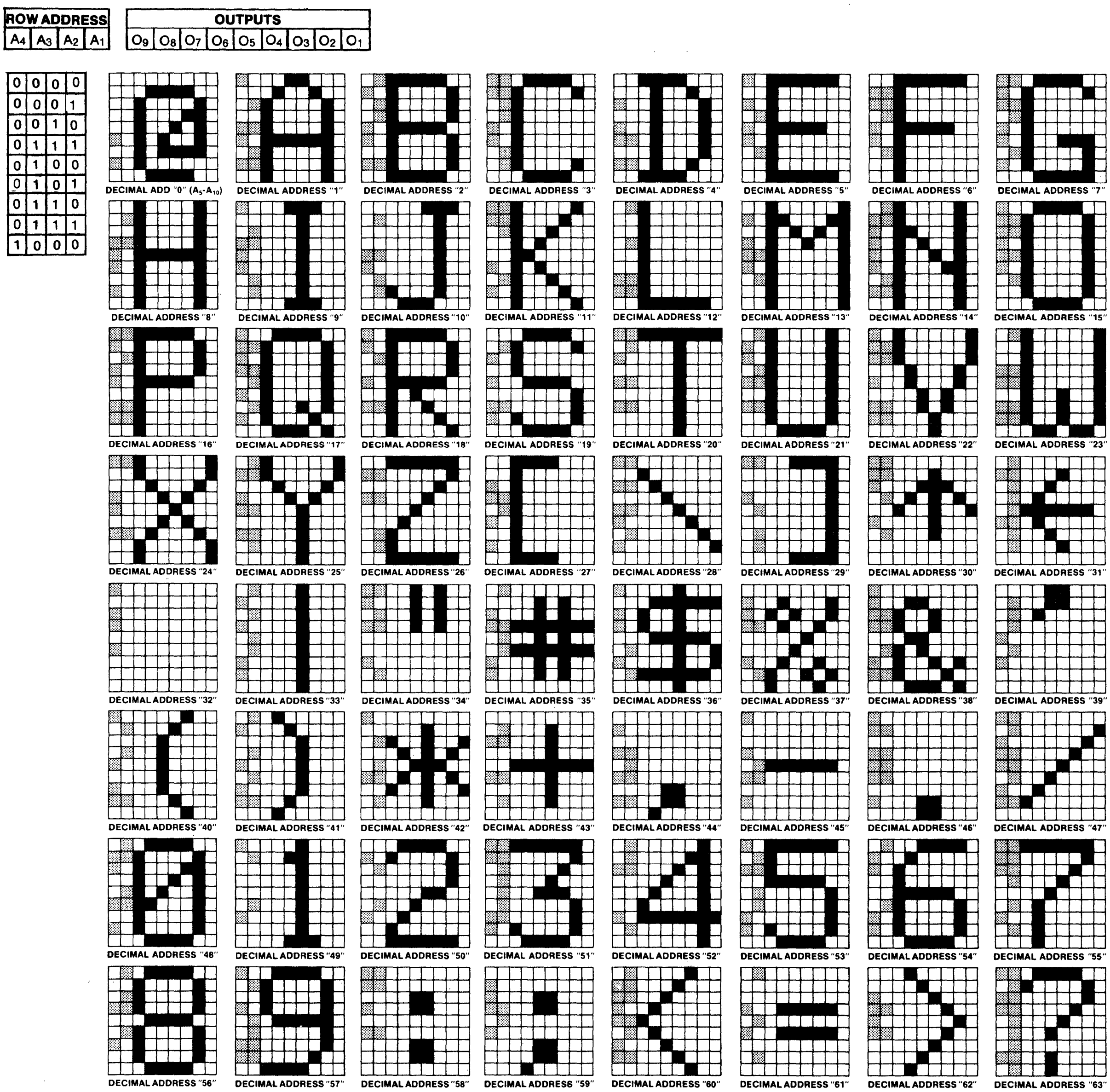


NOTES

A. BCDIC to ASCII in leftmost column, Baudot to ASCII in next column to right.
B. Undefined addresses result in all outputs going low (TTL "0").
C. Black squares in character font are high (TTL "1").

STANDARD CHARACTER FONTS (Cont'd)

CM 3941
ASCII SET, RASTER SCAN 7X9 WITH CODE CONVERSION



NOTES

A. BCDIC to ASCII in leftmost column, Baudot to ASCII in next column to right.
B. Undefined addresses result in all outputs going low (TTL "0").
C. Black squares in characer font are high (TTL "1").

1702A-I

DESCRIPTION

The 1702A is ideally suited for uses where fast turn-around and pattern experimentation are important. The device undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.[1]

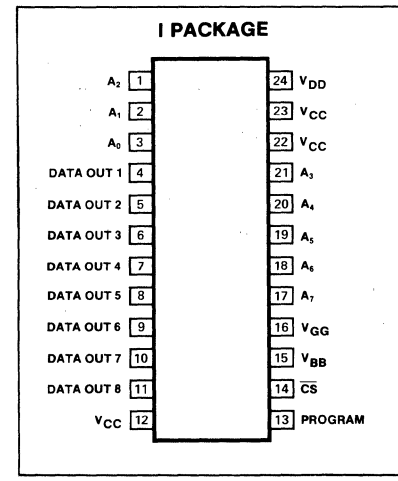
The 1702A is packaged in a 24-pin dual in-line package with a UV transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

The 1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of high performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

FEATURES

- **Fast programming for all 2048 bits: 2 minutes**
- **All 2048 bits guaranteed programmable**
- **100% factory tested**
- **Fully decoded**
- **Static MOS: No clocks required**
- **Inputs and outputs DTL and TTL compatible**
- **Tri-state output: OR-tie capability**
- **Simple memory expansion**
- **Chip select input lead**

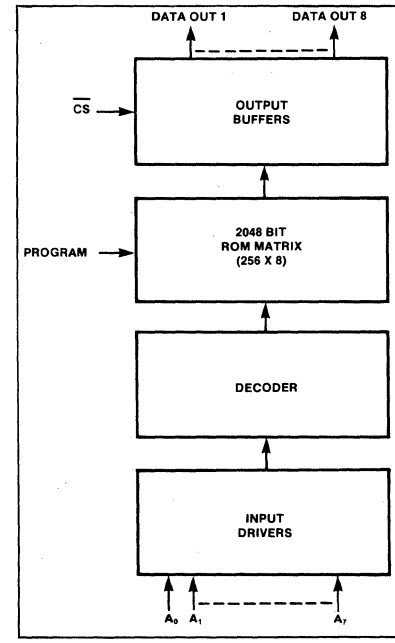
PIN CONFIGURATION



PIN DESIGNATION[2]

PIN NO.	SYMBOL	NAME & FUNCTION
		Read mode
12	V_{CC}	V_{CC}
13	Program	V_{CC}
14	$\overline{CS}$	GND
15	V_{BB}	V_{CC}
16	V_{GG}	V_{GG}
22	V_{CC}	V_{CC}
23	V_{CC}	V_{CC}
		Programming mode
12	V_{CC}	GND
13	Program	Program pulse
14	$\overline{CS}$	GND
15	V_{BB}	V_{BB}
16	V_{GG}	Pulsed V_{GG} (V_{IL4P})
22	V_{CC}	GND
23	V_{CC}	GND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[3]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	-65 to +125	
P_D	Power dissipation	2	W
	Soldering of leads (10sec)	300	°C
	Input voltages and supply voltages with respect to V_{CC}		V
	Read operation	0.5 to -20	
	Program operation	-48	

1702A-I

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = -9V ± 5%, V_{GG}[3] = -9V ± 5% unless otherwise specified.[4]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL1}	Low for TTL interface		-1.0		0.65	
V_{IL2}	Low for MOS interface		V_{DD}		V_{CC}-6	
V_{IH}	Address and chip select high		V_{CC}-2		V_{CC}+0.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA		-.7	0.45	
V_{OH}	High	I_{OH} = -100μA	3.5	4.5		
I_{LI}	Address and chip select input load current	V_{IN} = 0.0V			1	μA
I_{LO}	Output leakage current	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} -2			1	μA
	Supply current	I_{OL} = 0.0mA				mA
I_{DD1}		$\overline{CS}$ = V_{CC} -2, T_A = 25°C		35	50	
I_{DD2}		$\overline{CS}$ = 0.0, T_A = 25°C		32	46	
I_{DD3}		$\overline{CS}$ = V_{CC} -2, T_A = 0°C		38.5	60	
I_{GG}	Gate				1	
	Output current					mA
	Clamp	V_{OUT} = -1.0V				
I_{CF1}		T_A = 0°C		8	14	
I_{CF2}		T_A = 25°C			13	
I_{OL}	Sink	V_{OUT} = 0.45V	1.6	4		
I_{OH}	Source	V_{OUT} = 0.0V	-2.0			
	Capacitance[5]	All unused pins are at ac ground				pF
C_{IN}	Input	V_{IN} = V_{CC}, $\overline{CS}$ = V_{CC}		8	15	
C_{OUT}	Output	V_{OUT} = V_{CC}, V_{GG} = V_{CC}		10	15	

AC ELECTRICAL CHARACTERISTICS

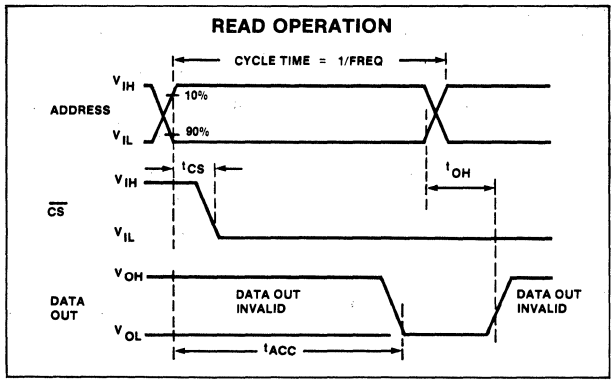
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = -9V ± 5% unless otherwise specified, Input pulse amplitudes = 0 to 4V, t_R, $t_F \leq$ 50ns, Output load is 1 TTL gate, Measurements made at output of TTL gate ($t_{PD} \leq$ 15ns), C_L = 15pF

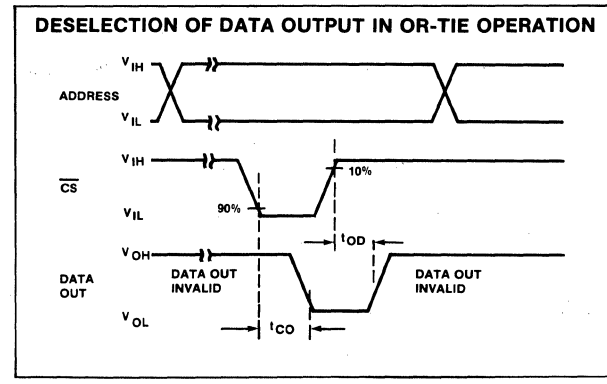
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Freq	Repetition Rate					1	MHz
t_{OH}	Previous read data valid					100	ns
	Delay time						
t_{ACC}[1]		Output	Address		0.7	1	μs
t_{CS}		Output	Chip select			100	ns
t_{CO}		Output	$\overline{CS}$			900	ns
t_{OD}	Output deselect					300	ns

NOTES

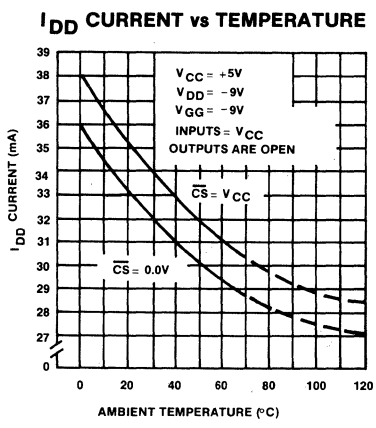
1. Signetics liability shall be limited to replacing any unit which fails to program as desired.
2. The external lead connections to the 1702A differ depending on whether the device is being programmed or used in read mode. In the programming mode, the data inputs 1-8 are pins 4-11 respectively.
3. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
4. Typical values are T_A = 25°C and at typical supply voltages.
5. This parameter is perdiodically sampled and is not 100° tested.

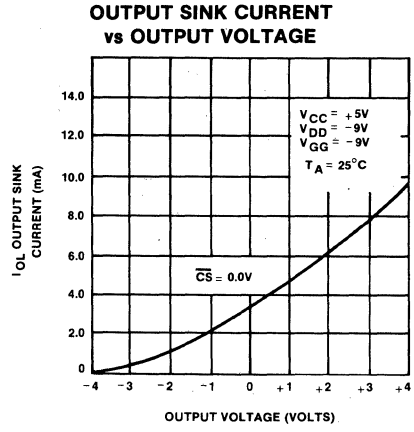
TIMING DIAGRAMS

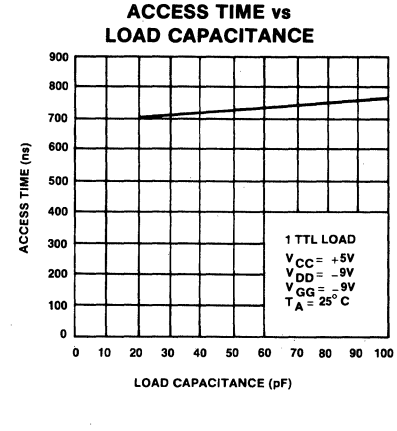


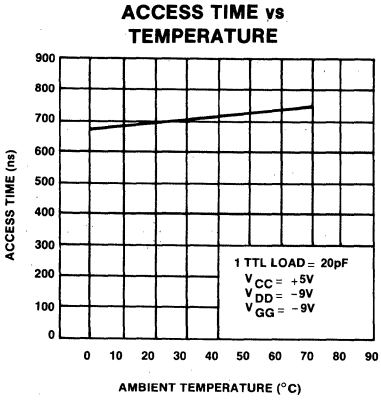


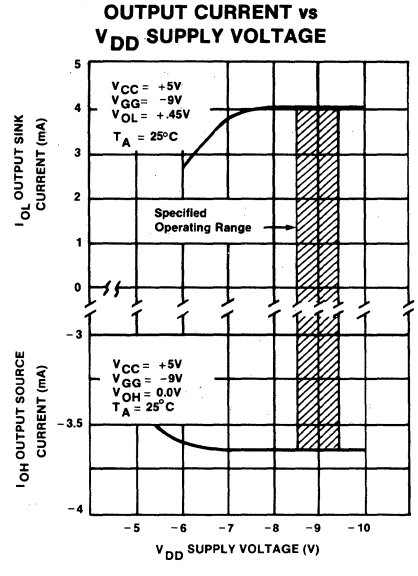
TYPICAL PERFORMANCE CHARACTERISTICS

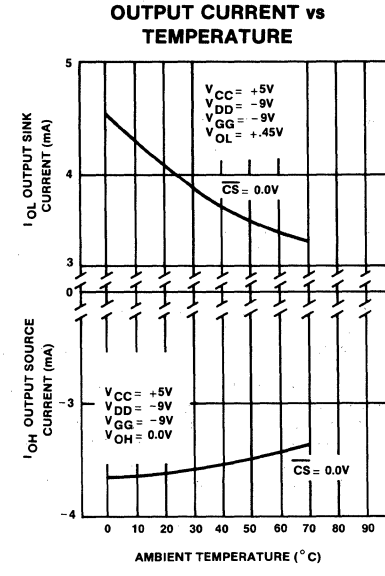












DC AND OPERATING PROGRAMMING CHARACTERISTICS

T_A = 25°C, V_{CC} = 0V, V_{BB} = +12V ± 10%, $\overline{CS}$ = 0V unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IHP}	High			0.3		
V_{IL1P}	Pulsed data low		-46	-48		
V_{IL2P}	Address low		-40	-48		
V_{IL3P}	Pulsed low V_{DD} and program		-46	-48		
V_{IL4P}	Pulsed low V_{GG}		-35	-40		
	Load current					mA
I_{LI1P}	Address and data input	V_{IN} = -48V		10		
I_{LI2P}	Program and V_{GG}	V_{IN} = -48V		10		
I_{BB}	V_{BB} supply[1]		10	100		
I_{DDP}	Peak I_{DD} supply[2]	$V_{DD} = V_{prog}$ = -48V, V_{GG} = -35V	200	300		

AC PROGRAMMING CHARACTERISTICS

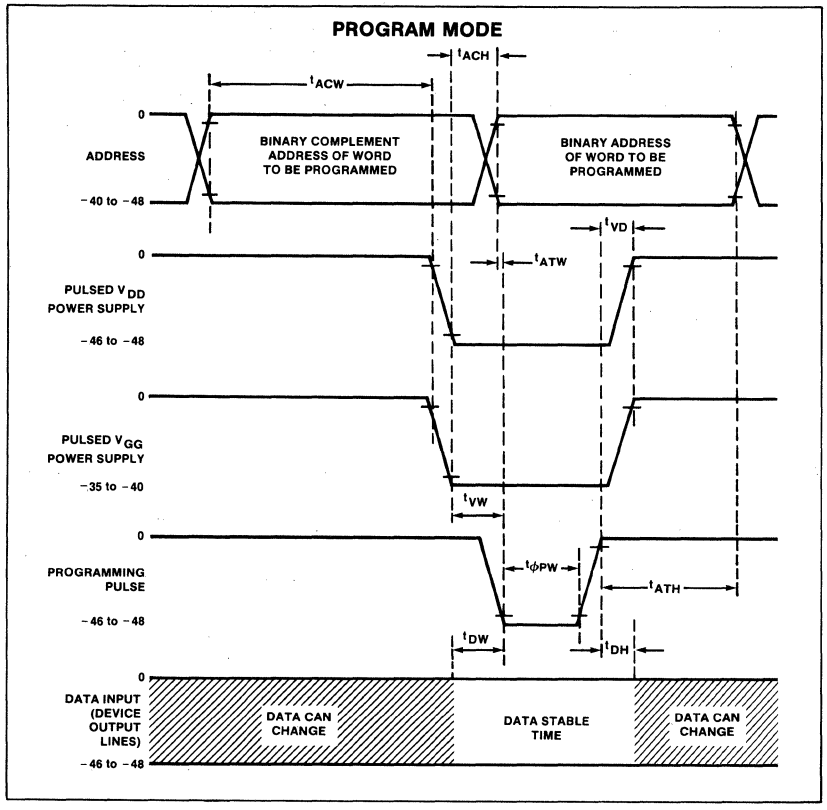
T_A = 25°C, V_{CC} = 0V, V_{BB} = +12V ± 10%, $\overline{CS}$ = 0V, unless otherwise specified, Input rise and fall times = < 1μs unless otherwise specified.

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Duty cycle (V_{DD}, V_{GG})						20	%
$t_{\phi PW}$	Program pulse width			$V_{DD} = V_{prog}$ = -48V, V_{GG} = -35V			3	ms
	Setup and hold time							μs
t_{DW}	Setup time	Programming pulse	Data		25			
t_{DH}	Hold time	Data	Programming pulse		10			
t_{VW}	Setup time	Programming pulse	Pulsed power supply		100			
t_{VD}	Hold time	Pulsed power supply	Programming pulse		10		100	
t_{ACW}	Setup time[3]	Pulsed V_{DD} power supply	Address		25			
t_{ACH}	Hold time[3]	Address	Pulsed V_{DD} power supply		25			
t_{ATW}	Setup time	Programming pulse	Address		10			
t_{ATH}	Hold time	Address	Programming pulse		10			

NOTES

1. The V_{BB} supply must be limited to 100mA current to prevent damage to the device.
2. I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μs. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.
3. All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0-255) must be programmed as shown in the timing diagram.

TIMING DIAGRAM



OPERATION IN PROGRAM MODE

Initially, all 2048 bits of the ROM are in the low state. Information is introduced by selectively programming high's in the proper bit locations.

Word Address selection is done by the same decoding circuitry used in the Read mode (see dc Electrical Characteristics table). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state of a minimum of 25μs after V_{DD} and V_{GG} have moved to the negative levels. The addresses must then make the transition to their true state a minimum of 10μs before the program pulse is applied.

The 8 output terminals are used as data inputs to determine the information pattern in the 8 bits of each word. A low data input level (-48V) will then program a "1" and a high data input level (ground) will leave a "0" (see dc and Operating Programming Characteristics table). All 8 bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the progamming, V_{GG}, V_{DD} and the program pulse are pulsed signals. We recommend the P+4P smart programming routine where P = the number of programming pulses for data to read true; P max = 256; and 4P = the number of over programming pulses applied.

ERASING PROCEDURE

The 1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537A°. The recommended integrated dose (i.e., UV intensity x exposure time) is 6W-sec/cm^2. Examples of ultraviolet sources which can erase the 1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc., 5114 Walnut Grove Avenue, San Gabriel, Ca. The lamps should be used without short-wave filters, and the 1702A to be erased should be placed about one inch away from the lamp tubes.

4096-BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE MOS ROM (512X8) 2704
8192-BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE MOS ROM (1024X8) 2708

DESCRIPTION

The 2708/2704 are high speed Erasable and Electrically Reprogrammable ROMs (EPROM) ideally suited where fast turn around and pattern experimentation are important requirements.

The 2708/2704 are packaged in a 24 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

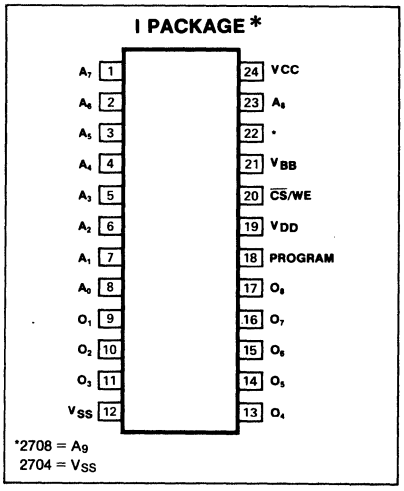
A pin for pin mask programmed ROM, the Signetics 2607, is available for large volume production runs of systems initially using the 2708.

The 2708/2704 is fabricated with the time proven n-channel silicon gate technology.

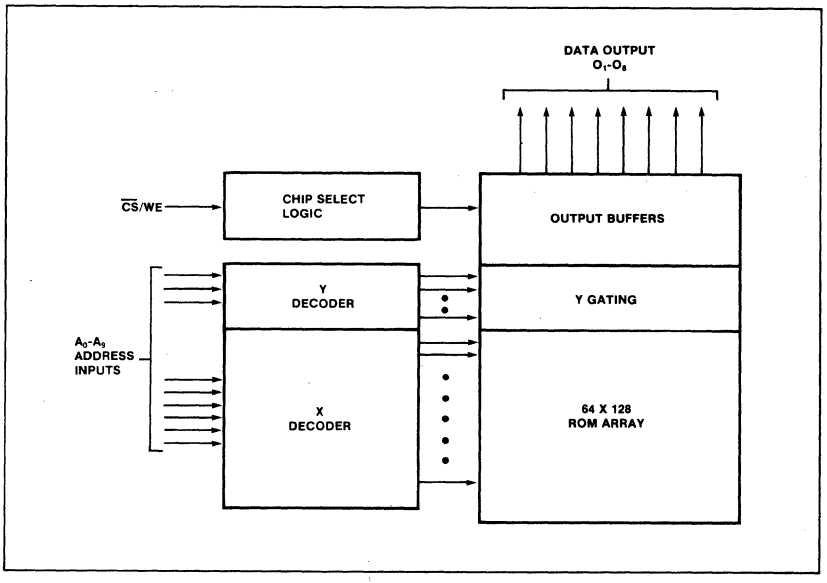
FEATURES

- **Organization:**
  2708: 1024X8
  2704: 512X8
- **Fast programming-100 sec. typ for all 8K bits**
- **Low power during programming**
- **Access time: 450ns**
- **Standard power supplies 12V, ±5V**
- **Static—no clocks required**
- **Inputs and outputs TTL compatible during both read and program modes**
- **Three-state output—OR-tie capability**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 125	
P_D	Power dissipation	1.5	W
	All input or output voltage with respect to V_{BB} (except program)	15 to -0.3	V
	Program input to V_{BB}	35 to -0.3	V
	Supply voltages V_{CC} and V_{SS} with respect to V_{BB}	15 to -0.3	V
	V_{DD} with respect to V_{BB}	20 to -0.3	V

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ± .25V, V_{BB} = -5V ± .25V, V_{DD} = 12V ± .6V, V_{SS} = 0V,
T_A = 0°C to 70°C, Output load = 100pF plus 1TTL input.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low		V_{SS}		0.65	
V_{IH}	High		3.0		V_{CC} + 1	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.45	
V_{OH1}	High	I_{OH} = -100μA	3.7			
V_{OH2}	High	I_{OH} = -1mA	2.4			
I_{LI}	Input load current	V_{IH} = 5.25V				μA
	Address and chip select				10	
I_{LO}	Output leakage current	V_{OUT} = 5.25V, CS/WE = 5V			10	μA
	Supply current	Worst case supply currents, All inputs high				mA
I_{DD}	V_{DD}			50	65	
I_{CC}	V_{CC}			6	10	
I_{BB}	V_{BB}	$\overline{CS}$/WE = 5V; T_A = 0°C		30	45	
P_D	Power dissipation	T_A = 70°C			800	mW
	Capacitance[3]	T_A = 25°C, f = 1MHz				pF
C_{IN}	Input	V_{IN} = 0V		4	6	
C_{OUT}	Output	V_{OUT} = 0V		8	12	

AC ELECTRICAL CHARACTERISTICS

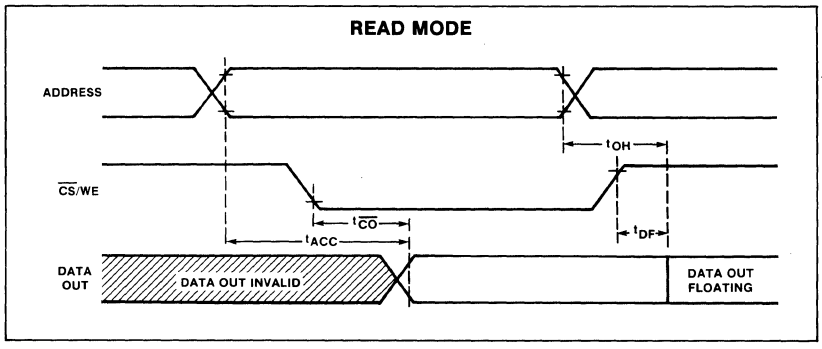
Output load = 1 TTL gate and CL = 100pF,
Input rise and fall times = 20ns,
Timing measurement reference levels = 0.8V and 2.8V for inputs,
0.8V and 2.4V for outputs. Input pulse levels = 0.65V to 3.0V

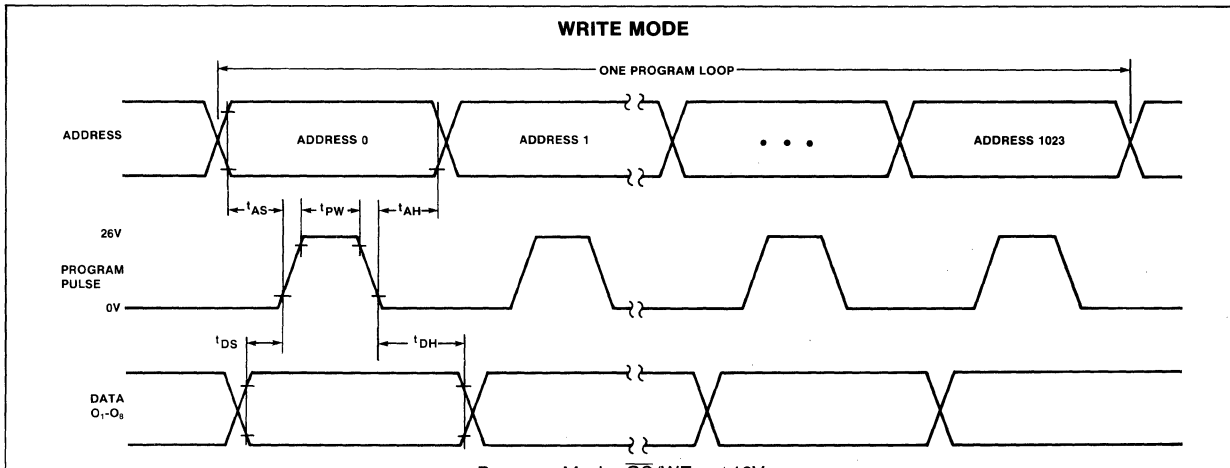
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Delay time						ns
t_{ACC}		Output	Address		280	450	
$t_{\overline{CO}}$		Output	Chip select			120	
t_{DF}	Float time	Output	Chip deselect	0		120	ns
t_{OH}	Hold time	Output	Address	0			ns

NOTES

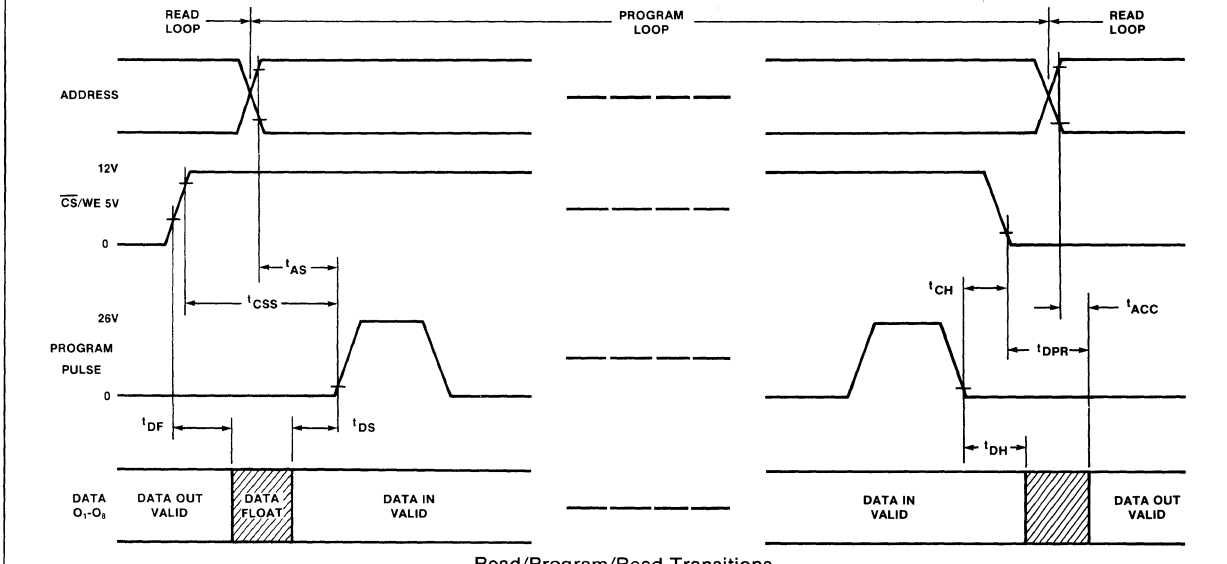
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Typical values are for T_A = 25°C and typical supply voltages.
3. This parameter is periodically sampled and not 100% tested.
4. The program input (pin 18) may be tied to V_{SS} during the read mode.
5. Signetics reserves the right to make changes in specification at any time and without notice. The information furnished by Signetics in this publication is believed to be accurate and reliable. However, no responsibility is assumed by Signetics for its use; nor any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of Signetics.

TIMING DIAGRAMS





Program Mode: $\overline{CS}$/WE = +12V



Read/Program/Read Transitions

Logic levels and timing reference levels same as in the Read Mode unless noted otherwise.

PROGRAMMING SPECIFICATIONS $T_A = 25°C$

	PARAMETER	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Setup and hold time				μs
t_{AS}	Address setup	10			
t_{AH}	Address hold	1			
t_{CSS}	$\overline{CS}$/WE setup	10			
t_{CH}	$\overline{CS}$/WE hold	.5			
t_{DS}	Data setup	10			
t_{DH}	Data hold	1			
t_{DF}	Chip deselect to output float delay	0		120	ns
t_{DPR}	Program to read delay			10	μs
t_{PW}	Program pulse width	.1		1.0	ms
t_{PR}	Program pulse rise time	.5		2.0	μs
t_{PF}	Program pulse fall time	.5		2.0	μA
I_P	Programming current		10	20	mA
V_P	Program pulse amplitude	25		27	V

PROGRAMMING PROCEDURE

At shipment and after each erasure, all bits of the 2708/2704 are in the logic high state (output high). The device is put into the program mode by raising the $\overline{CS}$/WE input (pin 20) to +12V. While in the program mode, data to be stored is presented on lines O_1-O_8, forming an 8-bit word. Word addresses are selected in the same manner as in the Read mode. After each address and data word is set up, one program pulse (V_P) is applied to the program input (pin 18). Refer to the Program Mode timing diagram. A program loop is defined as one pass through all device addresses. The number of loops (N) required is dependent upon the program pulse width (t_{PW}) according to $N^* t_{PW} \geq 100ms$.

Program and read loops may be alternated as shown in the Read/Program/Read Transitions timing diagram.

ERASING PROCEDURE

The 2708/2704 may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of $2537A_2°$. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W-sec/cm². Examples of ultraviolet sources which can erase the 2708/2704 in 30 to 60 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc., 5114 Walnut Grove Avenue, San Gabriel, California. The lamps should be used without short-wave filters, and the 2708/2704 to be erased should be placed about 1 inch away from the lamp tubes. Both Cervue and UV glass lids are available.

2518-N • 2519-N

DESCRIPTION

The 2518 32-bit and the 2519 40-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices intergrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing ease.

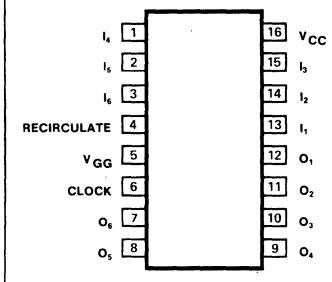
TRUTH TABLE

RECIR-CULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is written
0	1	"1" is written

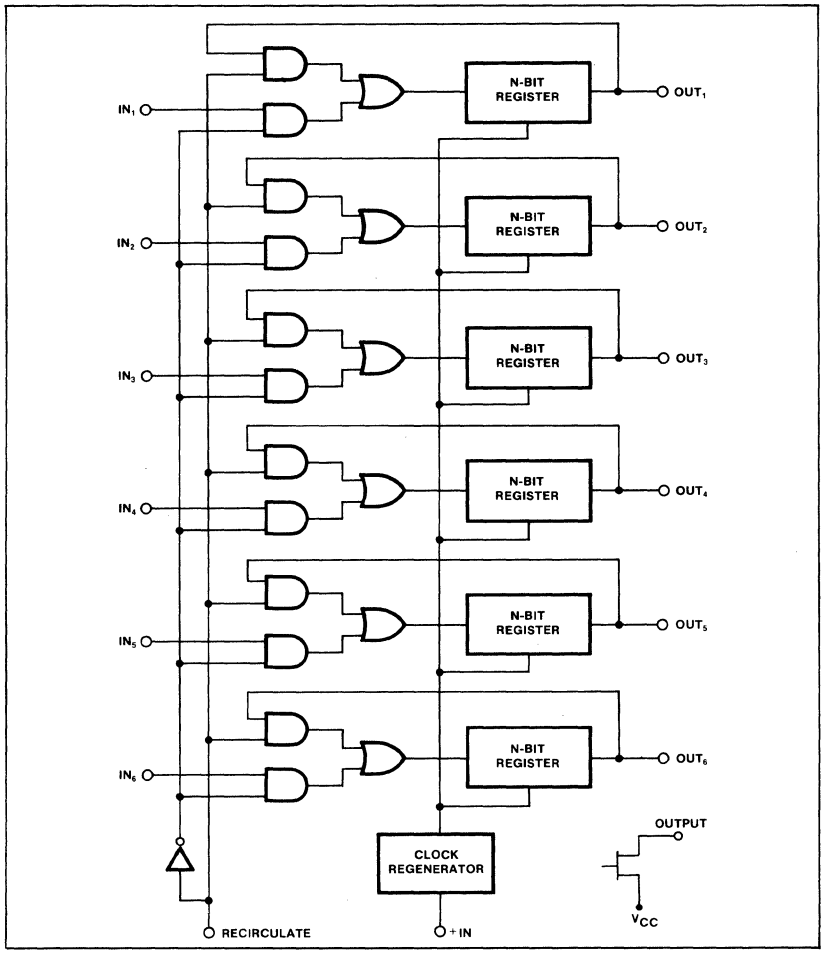
Data is read out when output enable is low. Output is tri-stated when output enable is high.

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating[2]	0 to +70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at $T_A = 70°C$	640	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{GG} = -12V ± 5% unless otherwise specified.[3,4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[8]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA		0.5		
V_{OH}	High	I_{OH} = 100μA	3.8			
	Leakage current	T_A = 25°C				nA
I_{LO}	Output			10	1000	
I_{LC}	Clock	V_{ILC} = GND		10	500	
I_{LI}	Input load current	V_{IN} = -5.5V, T_A = 25°C		10	500	nA
I_{GG}	Supply current	Continuous operation, T_A = 25°C, f = 1.5MHz		16	25	mA
	Capacitance	At 1MHz, V_{AC} = 25mV p-p				pF
C_{IN}	Input	V_{IN} = V_{CC}		5	7	
C_ϕ	Clock	V_ϕ = V_{CC}		6	7	

AC ELECTRICAL CHARACTERISTICS

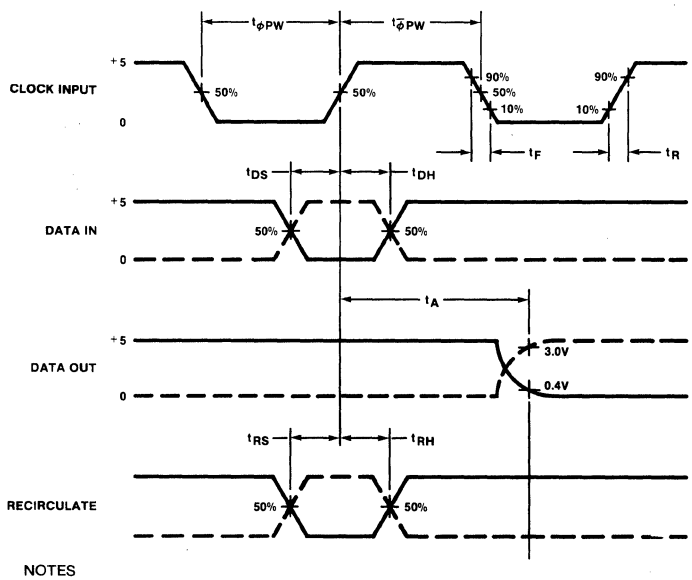
T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{GG} = -12V ± 5%, V_{ILC} = 0.4V to 4.0V

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
Freq.	Clock rep rate			dc	3	2	MHz
	Pulse width						μs
$t_{\phi PW}$	Clock[10]			.300		100	
$t_{\overline{\phi}PW}$	$\overline{\text{Clock}}$			.200		dc	
	Setup and hold time						ns
t_{DS}	Setup time	Clock in	Data in	100			
t_{DH}	Hold time	Data in	Clock in	70			
t_{RS}	Setup time	Clock	Recirculate	150			
t_{RH}	Hold time	Recirculate	Clock	50			
t_R,t_F	Clock pulse transition					5	μs
t_A	Clock to data out delay	Data	Clock		300	350	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C C/W, junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} -1.85V and V_{IL} = V_{CC} - 4.15V.
9. V_{OL} is dependent on R_L and input characteristics of driven gate.
10. Input rise and fall times = 10ns. Output load is 1 TTL gate.
11. For static operation, clock must be stopped in TTL high state in order to retain data (see clock pulse width specification).

TIMING DIAGRAM



NOTES

A. Input rise and fall times = 10ns. Output load is 1 TTL gate.
B. For static operation, clock must be stopped in TTL high state in order to retain data

DUAL 50-BIT STATIC SHIFT REGISTER (50X2) 2509
DUAL 100-BIT STATIC SHIFT REGISTER (100X2) 2510
DUAL 200-BIT STATIC SHIFT REGISTER (200X2) 2511

2509-N,K • 2510-N,K • 2511-N,K

DESCRIPTION

The 2509 50-bit, 2510 100-bit, and the 2511 200-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals plus tri-state outputs are provided for maximum interfacing ease.

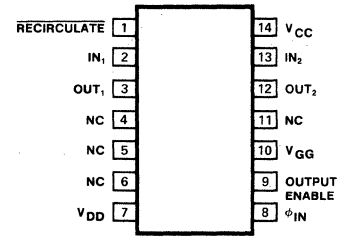
TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

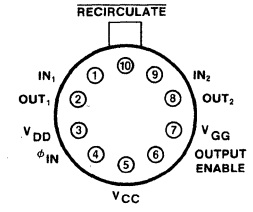
"0" = OV; "1" = +5V.

PIN CONFIGURATIONS

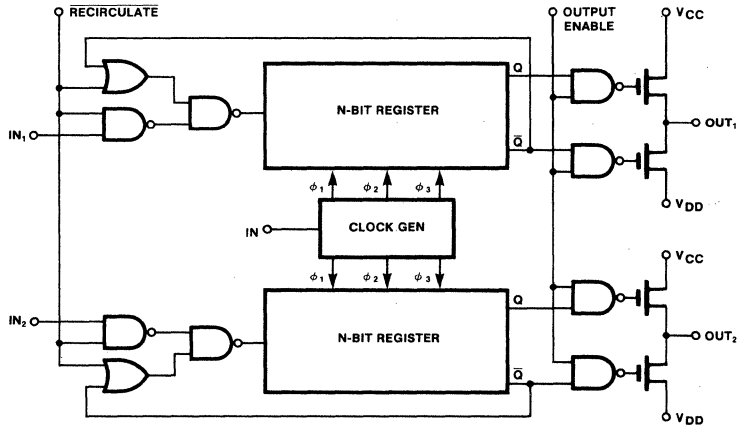
N PACKAGE



K PACKAGE



BLOCK DIAGRAM



NOTES

A. N = 50 for 2509, N = 100 for 2510, N = 200 for 2511.
B. If output enable = low, output is off.
C. If output enable = high, see Truth Table.

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating[2]	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C[2]	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}[3]	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V$[4], $V_{DD} = -5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$ unless otherwise specified[5,6,7,8]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[4]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low		-5		0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.5	
V_{OH}	High	$I_{OH} = 100\mu A$	3.8	3.5		
	Driving MOS		3.6			
	Leakage current	$T_A = 25°C$				nA
I_{LO}	Output	$V_{CE} = 1.05V$, $V_{OUT} = -5V$		10	1000	
I_{LC}	Clock	$V_{ILC} = GND$		10	500	
I_{DD}	Supply current	Continuous operation, $T_A = 25°C$, f = 1.5MHz				mA
	Dual 50			6.5	15	
	Dual 100			12	30	
	Dual 200			20	40	
I_{GG}				4.5	7.5	
I_{LI}	Input load current	$V_{IN} = -5.5V$, $T_A = 25°C$		10	500	nA
	Capacitance	At 1MHz; $V_{AC} = 25mV$ p-p				pF
C_{IN}	Input	$V_{IN} = V_{CC}$			5	
C_{OUT}	Output	$V_{OUT} = V_{CC}$			5	
C_{ϕ}	Clock	$V_{\phi} = V_{CC}$			5	

AC ELECTRICAL CHARACTERISTICS

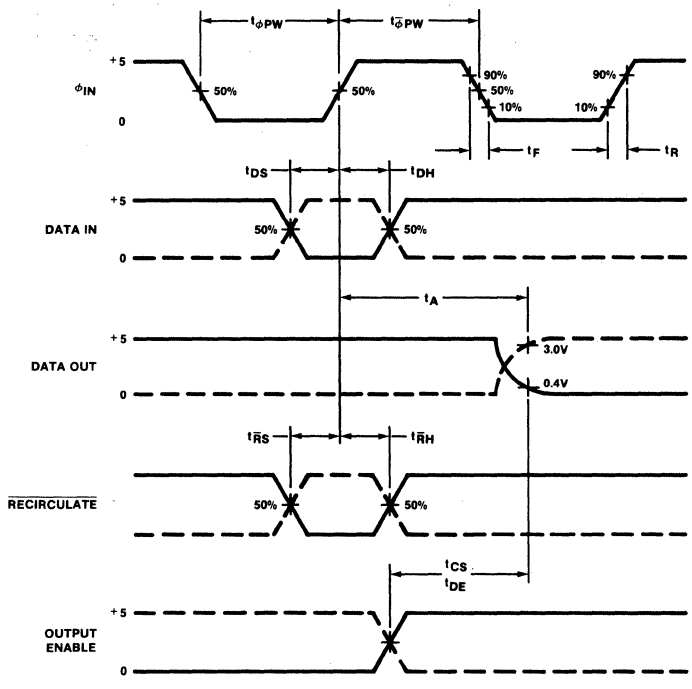
$V_{CC} = 5V$[4], $V_{DD} = -5V \pm 5\%$, $V_{ILC} = 0.4V$ to $4V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $70°C$.

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate				dc	3	1.5	MHz
	Pulse width							μs
$t_{\phi}PW$	Clock				.290	150	100	
$t_{\overline{\phi}}PW$	$\overline{\text{Clock}}$				.210		dc	
	Setup and hold time							ns
t_{DS}	Setup time	ϕin	Data in		50			
t_{DH}	Hold time	Data in	ϕin		70			
	Propagation delay							ns
t_A		Data out	Clock			200	350	
t_A				$I_{OL} = 1.6mA$			500	
T_{CS}	Select time	Data out	Output enable				300	ns
T_{DE}	Deselect time						300	ns
t_R, t_F	Clock pulse transition						1	μs

NOTES

1. Stresses above those listed under absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 150°C/W.
3. All inputs are protected against static charge accumulation.
4. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to 70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
5. Parameters are valid over operating temperature range unless otherwise specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at 25°C and typical supply voltages.

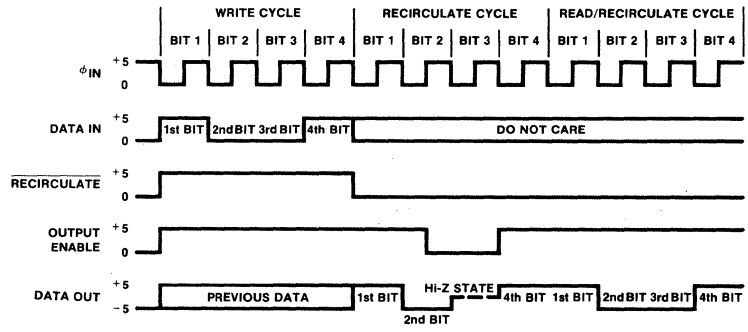
TIMING DIAGRAM



$t_R = t_F < 10ns$ for all inputs

TYPICAL APPLICATION

EXAMPLE FOR 4-BIT SHIFT REGISTER



NOTES

A. Write Cycle: The positive going edge of the recirculate control is coincident with the negative-going clock edge. The output enable control may be either high or low. If it is high, previous data will be read, and the 1st bit will be read after the fourth rising clock edge.

B. Recirculate Cycle: Data Recirculates while the recirculate control is low. Output enable may be either high or low. If it is low, the output is in the high impedance state.

C. Read/Recirculate Cycle: Data is read out while the output enable is high. Data is also recirculated as long as the recirculate control is low.

DESCRIPTION

The 2532 static shift register consists of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip. Each of the four 80-bit registers is provided with an independent input, push-pull output and recirculation control. The single phase clock is common to all 4 registers. All inputs and outputs including the clock interface directly with TTL or DTL circuits without external components.

Data is entered when the clock is at a logic high. Data is shifted when the clock goes low. When the recirculate control is at a logic high, data recirculates and is continuously available at the output, data input is inhibited. When the recirculate control is at a logic low, data is entered.

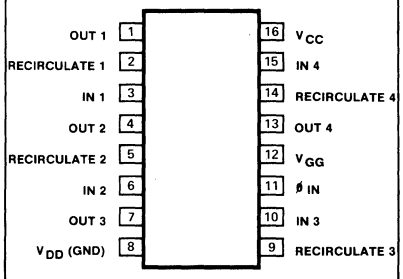
TRUTH TABLE

RECIRCULATE	FUNCTION	INPUT
0	"0" is written	0
0	"1" is written	1
1	Recirculate	0
1	Recirculate	1

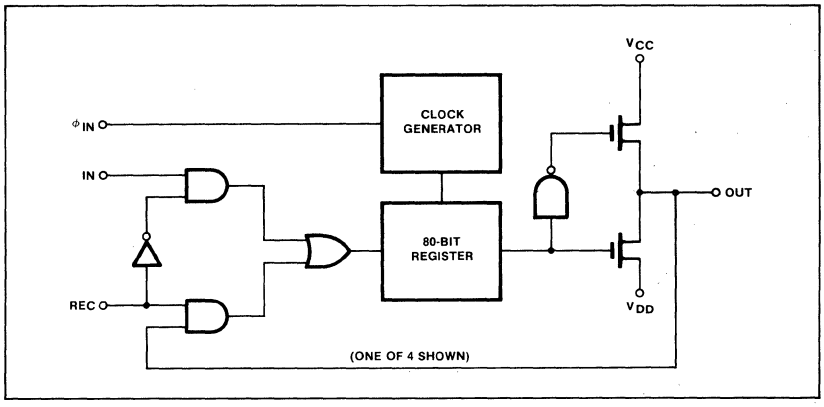
"0" = OV, "1" = +5V

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating[2]	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at $T_A = 70°C$	640	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	+0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{GG} = -12V ± 5% unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[3]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.5	
V_{OH}	High	I_{OH} = 100μA	3.8			
	Supply current					mA
I_{GG}		Continous operation, f = 1.5MHz, T_A = 25°C, Outputs open		6	10	
I_{CC}				12	20	
I_{LI}	Input load current	V_{IN} - 5.5V, T_A -25°C		10	500	nA
I_{LC}	Clock leakage current	V_{ILC} = OV, T_A = 25°C		10	500	nA
	Capacitance	At 1MHz, V_{AC} = 25mV p-p				pF
C_{IN}	Input	V_{IN} = V_{CC}			5	
C_ϕ	Clock	V_ϕ = V_{CC}			5	

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{GG} = -12V ± 5%,
Input rise and fall times = 10ns, Output load = 1TTL gate

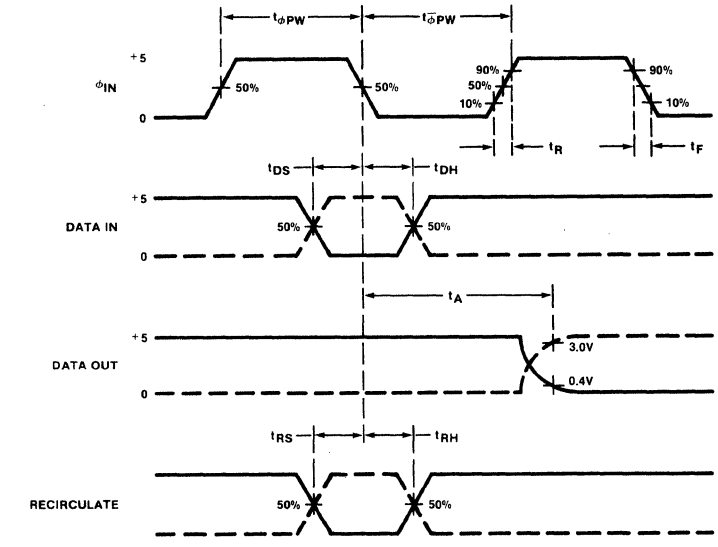
PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate			See timing diagram	dc	3.0	1.5	MHz
	Pulse width							μs
$t_{\phi PW}$	Clock				0.33		100	
$t_{\overline{\phi}PW}$	$\overline{\text{Clock}}$				0.33		dc	
t_R,t_F	Clock pulse transition						5	μs
	Setup and hold time							ns
t_{DS}	Setup time	ϕin	Data in		120			
t_{DH}	Hold time	Data in	ϕin		70			
t_{RS}	Setup time	ϕin	Recirculate		150			
t_{RH}	Hold time	Recirculate	ϕin		70			
t_A	Delay time	Data out	Clock	I_{OL} = 1.6mA			400	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} -1.85V and V_{IL} = V_{CC} -4.15V.
4. All inputs are protected against static charge.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.

2532-N

TIMING DIAGRAM



NOTES

A. $t_R = t_F$ 10ns for all inputs.
B. Clock must be stopped in the TTL low state to retain data during static operation.

2521-N • 2522-N

DESCRIPTION

The 2521 128-bit and the 2522 132-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip.

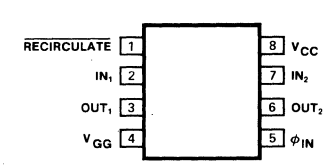
TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

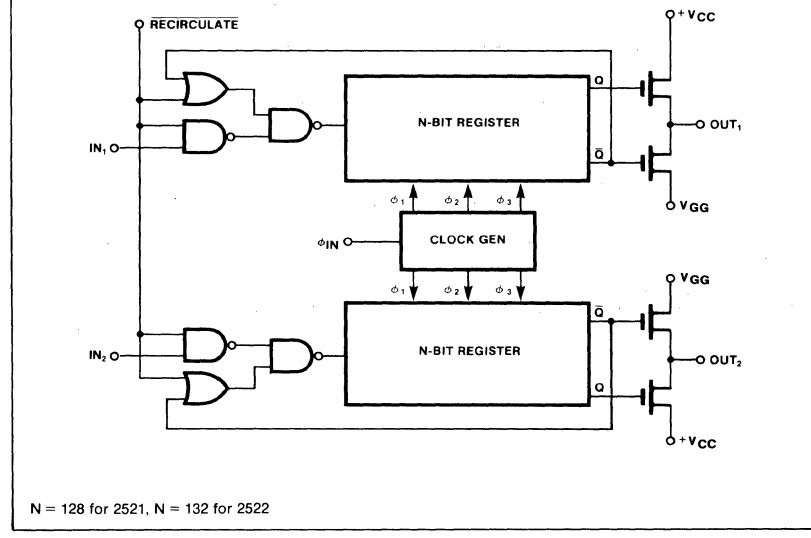
"0" = 0V, "1" = +5V.

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



N = 128 for 2521, N = 132 for 2522

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5V ± 5%, V_{GG} = −12V ± 5% unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[3]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.5	
V_{OH}	High	I_{OH} = 100μA	3.8			
I_{LI}	Input load current	V_{IN} = 5.5V, T_A = 25°C		10	500	nA
I_{LC}	Clock leakage current	V_{ILC} = GND, T_A = 25°C		10	500	nA
I_{GG}	Supply current	Continuous operation, T_A = 25°C, f = 1.5MHz		28	32	mA
	Capacitance	At 1MHz, V_{AC} = 25mV p-p				pF
C_{IN}	Input	V_{IN} = V_{CC}			5	
C_ϕ	Clock	V_ϕ = V_{CC}			5	

AC ELECTRICAL CHARACTERISTICS

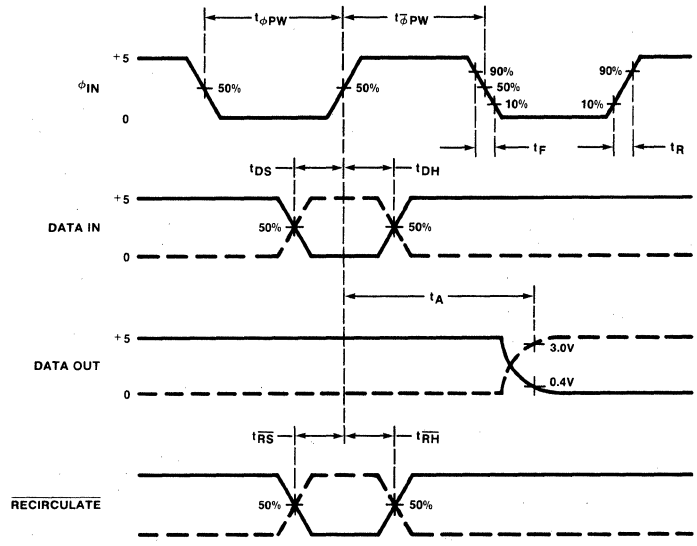
V_{CC} = 5V + 5V ± 5%, V_{GG} = −12V ± 5%, T_A = 0°C to 70°C

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate				dc		1.5	MHz
	Pulse width			See timing diagram note				
$t_{\phi PW}$	Clock				.350	.100	100	μs
$t_{\overline{\phi} PW}$	$\overline{\text{Clock}}$				.200		dc	μs
t_R,t_F	Clock pulse transition[2]						1	μs
	Setup and hold time							ns
t_{DS}	Setup time	Write	Data		75			
t_{DH}	Hold time	Clock	Data		70			
$t_{\overline{RS}}$	Setup[2]	ϕ in high	$\overline{\text{Recirculate}}$		50			
$t_{\overline{RH}}$	Hold[2]	$\overline{\text{Recirculate}}$	ϕ in high					
t_A	Delay time[2]	Data	ϕ in high			250	350	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} − 1.85V and V_{IL} = V_{CC} − 4.15V.
4. All inputs are protected against static charge.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserving the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.

TIMING DIAGRAM



NOTES

A. $t_R = t_F < 10ns$ for all inputs.
B. For static operation, clock must be stopped in TTL high state in order to retain data (see clock pulse width specification).

DUAL 240-BIT STATIC SHIFT REGISTER (240X2) 2527
DUAL 250-BIT STATIC SHIFT REGISTER (250X2) 2528
DUAL 256-BIT STATIC SHIFT REGISTER (256X2) 2529

2527-N • 2528-N • 2529-N

DESCRIPTION

The 2527 240-bit, 2528 250-bit, and the 2529 256-bit recirculating static shift registers consist of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip.

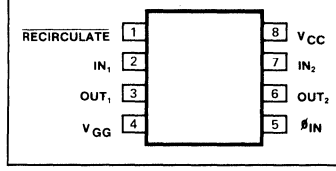
TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is written
1	1	"1" is written

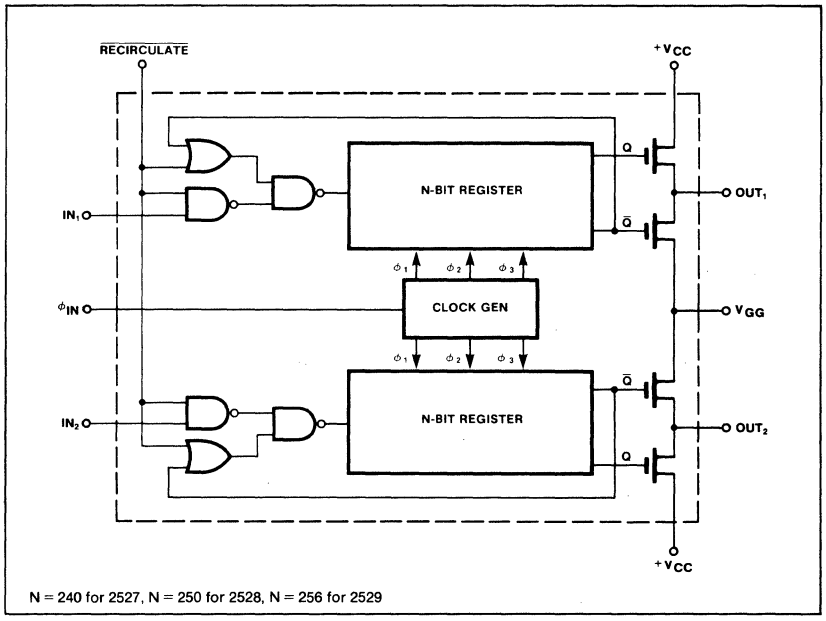
"0" = 0V; "1" = +5V

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



N = 240 for 2527, N = 250 for 2528, N = 256 for 2529

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

MOS MEMORY

2527-N • 2528-N • 2529-N

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[3]					V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.5	
V_{OH}	High	$I_{OH} = 100\mu A$	3.8			
I_{LI}	Input load current	$V_{IN} = 5.5V$, $T_A = 25°C$		10	500	nA
I_{LC}	Clock leakage current	$V_{ILC} = OV$, $T_A = 25°C$		10	500	nA
I_{GG}	Supply current	Continuous operation, $T_A = 25°C$, f = 1.5MHz, Outputs open		28	35	mA
	Capacitance	At 1MHz, $V_{AC} = 25mV$ p-p				pF
C_{IN}	Input	$V_{IN} = V_{CC}$			5	
C_ϕ	Clock	$V_\phi = V_{CC}$			5	

AC ELECTRICAL CHARACTERISTICS

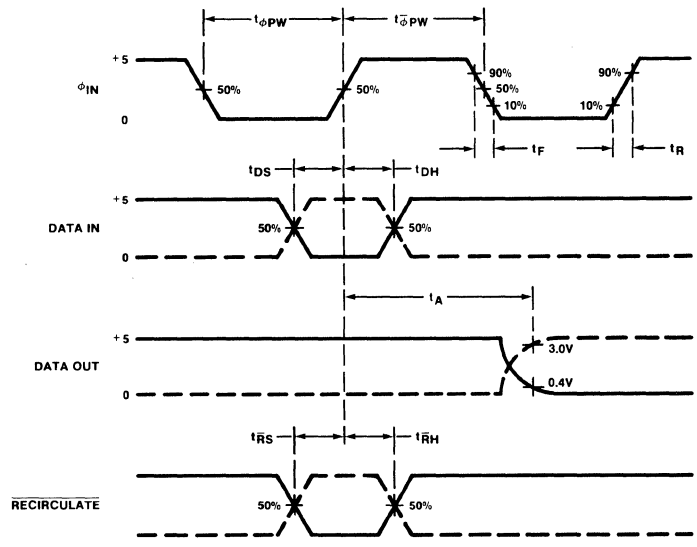
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{GG} = -12V +5\%$,
Input rise and fall times = 10ns, Output load = 1TTL gate.

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate			See timing diagram note	dc	2.5	1.5	MHz
	Pulse width							μs
$t_{\phi PW}$	Clock				0.2	0.1	100	
$t_{\overline{\phi} PW}$	$\overline{\text{Clock}}$				0.2		dc	
$t_{R,tF}$	Clock pulse transition						1	μs
	Setup and hold time							ns
t_{DS}	Setup time	ϕin	Data in		50			
t_{DH}	Hold time	Data in	ϕin		70			
$t_{\overline{RS}}$	Setup time	ϕin	$\overline{\text{Recirculate}}$		50			
t_{RH}	Hold time	$\overline{\text{Recirculate}}$	ϕin					
t_A	Delay time	Data out	Clock	$I_{OL} = 1.6mA$		330	450	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
4. All inputs are protected against static charge.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.

TIMING DIAGRAM



NOTES

A. $t_R = t_F < 10$ns for all inputs.
B. For static operation, the input clock must be stopped in the TTL high state in order to retain data (see clock pulse width specification).

2533-N

DESCRIPTION

The 2533 static shift register consists of enhancement mode p-channel silicon gate MOS devices integrated on a single monolithic chip.

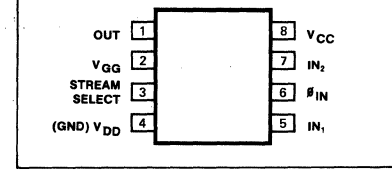
The 1024-bit register is equipped with 2 data inputs together with a stream select control to facilitate external recirculation.

The single phase clock input, data input, data output, and stream select control will interface directly with TTL/DTL circuits without external components.

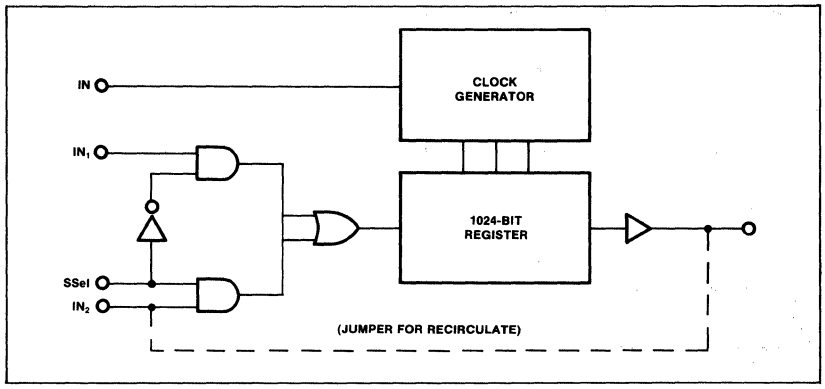
Data is entered when the clock is at a logic high. Data is shifted when the clock goes low.

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



TRUTH TABLE

STREAM SELECT	FUNCTION
0	IN 1 selected
1	IN 2 selected

"0" = 0V, "1" = +5V

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at $T_A > 25°C$[2]	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to 70°, $V_{CC} = 5V \pm 5\%$, $V_{GG} = -12V + 5\%$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage[3]	$V_{CC} = 5V$				V
V_{IL}	Low				0.6	
V_{IH}	High		3.4		5.3	
V_{ILC}	Clock low				0.6	
V_{IHC}	Clock high		3.4		5.3	
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.5	
V_{OH}	High	$I_{OH} = 100\mu A$	3.8			
I_{LI}	Input load current	$V_{IN} = 0$, $T_A = 25°C$		10	500	nA
I_{LC}	Clock leakage current	$V_{ILC} = GND$, $T_A = 25°C$		10	500	nA
	Supply current	Continuous operation, f = 1.5MHz				mA
I_{CC}				16	30	
I_{GG}				5.0	7.5	
	Capacitance	At 1MHz; $V_{AC} = 25mV$ p-p				pF
C_{IN}	Input	$V_{IN} = V_{CC}$			5	
C_{OUT}	Output	$V_{OUT} = V_{CC}$			5	
C_ϕ	Clock	$V_\phi = V_{CC}$			5	

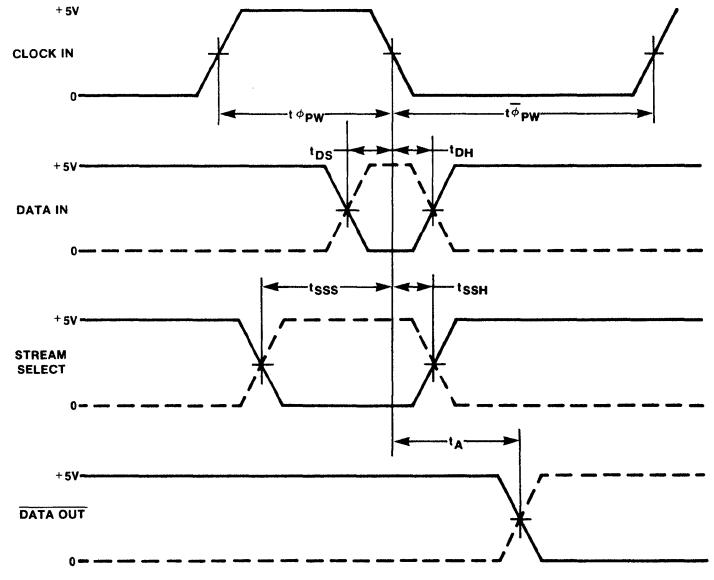
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Clock and data rep rate			See timing diagram		2	1.5	MHz
	Pulse width							
$t_\phi PW$	Clock				.350		100	μs
$t_{\overline{\phi}} PW$	Clock				250		dc	ns
t_R, t_F	Clock pulse transition						1	μs
	Setup and hold time							ns
t_{DW}	Setup time	Write	Data		50			
t_{DH}	Hold time	Clock	Data		70			
t_{SSS}	Setup time	Clock in	Stream select		80			
t_{SSH}	Hold time	Stream select	Clock in		50			
t_A	Delay time	Data out	Clock			200	300	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated corresponding to a thermal resistance of 150°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
4. All inputs are protected against static charge.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.

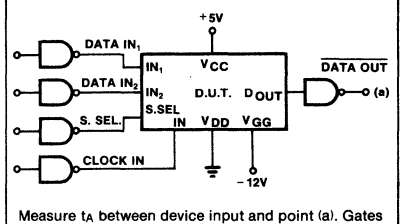
TIMING DIAGRAM



NOTES

A. Times measured at 50% points with input t_R $t_F \leq 10ns$.
B. Clock must be stopped in TTL low state to retain data during static mode operation.

TEST LOAD CIRCUIT



Measure t_A between device input and point (a). Gates are standard 7400.

MOS MEMORY

2506-T,N • 2507-T,N • 2517-T,N

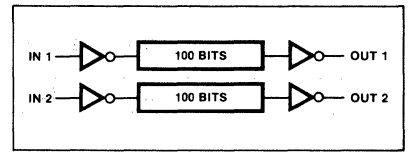
DESCRIPTION

These Signetics 2500 Series dual 100-bit Dynamic Shift Registers consist of enhancement mode p-channel MOS devices integrated on a single monolithic chip. They use 2 clock phases.

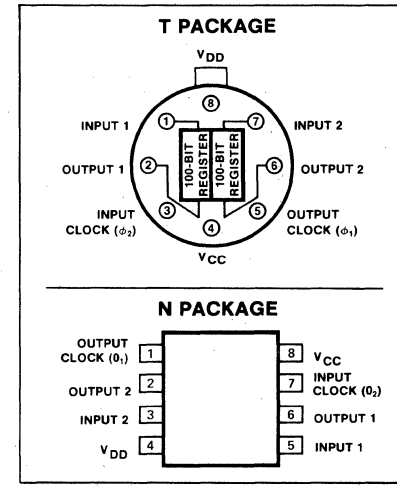
FEATURES

- **2506: Bare drain**
- **2507: 7.5K Pull down**
- **2517: 20K Pull down**

BLOCK DIAGRAM



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C[2]		mW
	T package	535	
	N package	455	
	Clock input voltages with respect to V_{CC}[3]	0.3 to -20	V
	Supply and data input voltages with respect to V_{CC}[3]	0.3 to -12	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = -5V ± 5%, V_{CC} = 5V[4], unless otherwise specified.[5,6,7,8]

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage[9]					V
V_{IL}	Low		-5		1.05	
V_{IH}	High		3.2		5.3	
V_{ILC}	Clock low		-12		-10	
V_{IHC}	Clock high		4		5.3	
	Output voltage[9]					V
V_{OH1}	High (driving MOS)	R_{INT} = 7.5k typ, C_L = 10pF, 2507 only	3.4	4.0		
		R_{INT} = 20k typ, 2517 only				
V_{OH2}	High (driving TTL)	R_L = 3.3k, V_{DD} = -5V, 2506 only	3.0	3.5		
I_{LI}	Load current	T_A = 25°C				nA
	Input 1	OUT 1, ϕ1, ϕ2 and V_{CC} = 5V, IN 2, OUT 2 and IN 1 = -5.5V, V_{DD} = -4.5V		10	500	
	Input 2	OUT 2, ϕ1, ϕ2 and V_{CC} = 5V, IN 1, OUT 1 and IN 2 = -5.5V, V_{DD} = -4.5V		10	500	
I_{LO}	Leakage current[10]	T_A= 25°C				nA
	Out 1	IN 1, V_{CC}, OUT 2 and ϕ2 = 5V, IN 2, V_{DD} and OUT 1 = -5.5V, ϕ1 = -5V		10	1000	
	Out 2	IN 1, OUT 1, V_{CC} and ϕ2 = 5V, IN 2, V_{DD} and OUT 2 = -5.5V, ϕ = -5V		10	1000	
I_{LC}	Clock leakage current	T_A = 25°C, V_{DD} = -4.5V, All other pins 5V				nA
	ϕ1	Vϕ1 = -12V		10	1000	
	ϕ2	Vϕ2 = -12V		10	1000	
I_{DD}	V_{DD} supply current	Outputs at logic low or high 3MHz, ϕ_1 = 150ns, ϕ_2 = 100ns		12	26	mA
	Capacitance	1MHz, 25mV p-p				pF
C_{IN}	Input (1 and 2)	V_{IN} = V_{CC}		2.5	5	
$C\phi$	Clock input (ϕ1,ϕ2)	Vϕ = V_{CC}		25	40	

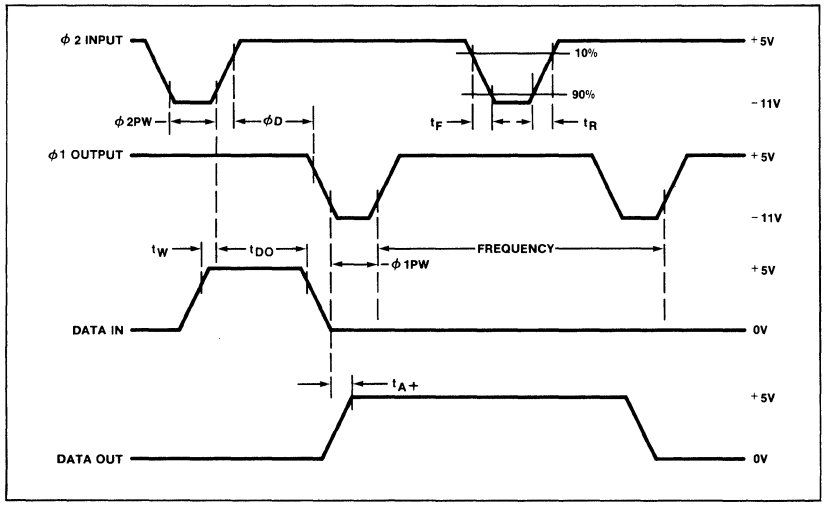
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{DD} = -5V \pm 5\%$, $V_{CC} = 5V^4$, $V_{ILC} = -11V$

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate				.0006	4	3	MHz
	Pulse width			At 3MHz				ns
ϕ1PW	Clock ϕ1				150			
ϕ2PW	Clock ϕ2				100			
ϕ_d	Clock pulse delay			At 3MHz	10			ns
t_R,t_F	Clock pulse transition			At 3MHz	10		1000	ns
tw	Setup time	ϕ2	Data in		75			ns
t_{DO}	Data in overlap			$t_{R02} = t_{R01} = 10ns$	10			ns
t_{A+}	Delay time	Data out	ϕ1	$V\phi = V_{CC}$ -16V, Data out = 2.5V		90	150	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (T package) or 175°C/W (V package).
3. All inputs are protected against static charge.
4. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
5. Parameters are valid over operating temperature range unless otherwise specified.
6. All voltage meuurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.
9. Logic Convention: Data Lines - Positive; Clocks -Negative.
10. V_{OL} (for this bare drain device) is a function only of the driven gate characteristics together with the external pull-down resistor. (R_{PD}).

TIMING DIAGRAM



2505-K • 2512-K

DESCRIPTION

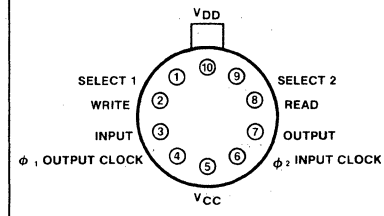
The 2505 512-bit and the 2512 1024-bit recirculating dynamic shift registers consist of enhancement mode p-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls, together with 2 chip select controls are included on the chip.

TRUTH TABLE

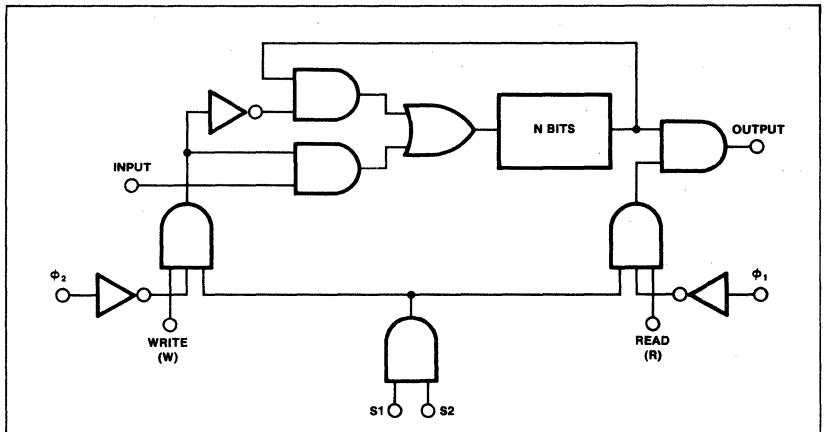
WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is data
1	0	Write mode, Output is '0'
1	1	Read/write, Output is data

PIN CONFIGURATION

K PACKAGE



BLOCK DIAGRAM



NOTES

A. N = 512 or 1024, Low = 0V, High = +5V.
B. When S1 or S2 is low, data recirculates.
C. When S1 and S2 are high, see Truth Table.

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at $T_A > 70°C$[2]	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

2505-K • 2512-K

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	2505			2512			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage[3]								V
V_{IL}	Low		-5.0		0.6	-5.0		0.6	
V_{IH}	High		3.4		5.3	3.4		5.3	
V_{ILC}	Clock low		-12.0		-10.0	-12.0		-10.0	
V_{IHC}	Clock high		4.0		5.3	4.0		5.3	
	Output voltage								V
V_{OL}	Low	$R_L = 3.0K$, 1 TTL load ($I_L = 1.6mA$)[4]		-1.0			-1.0		
V_{OH1}	High, driving 1 TTL load	$R_L = 3.0K$, 1 TTL load ($I_L = 100\mu A$)	2.4	3.5		2.4	3.5		
V_{OH2}	High, driving MOS	$R_L = 5.6K$, $C_L = 10pF$	3.6	4.0		3.6	4.0		
I_{LI}	Input load current	$V_{IN} = 5.5V$, $T_A = 25°C$		10	500		10	500	nA
	Leakage current	$T_A = 25°C$							nA
I_{LO}	Output	$V_{\phi1} = V_{\phi2} = -12V$, $V_{DD} = -5V$, $V_{OUT} = -5.5V$		10	1000		10	1000	
I_{LC}	Clock	$V_{ILC} = -12V$		10	1000		10	1000	
I_{DD}	Supply current	Continuous operation, $\phi pW = 150ns$, 1MHz, $V_{ILC} = -12V$, $T_A = 25°C$, $V_{DD} = -5.5V$		15	25		25	35	mA
	Capacitance	1 MHz, $V_{AC} = 25mV$ p-p							pF
C_{IN}	Input	$V_I = V_{CC}$			5			5	
C_{OUT}	Output	$V_O = V_{CC}$			5			5	
C_ϕ	Clock	$V_\phi = V_{CC}$			50			100	

AC ELECTRICAL CHARACTERISTICS

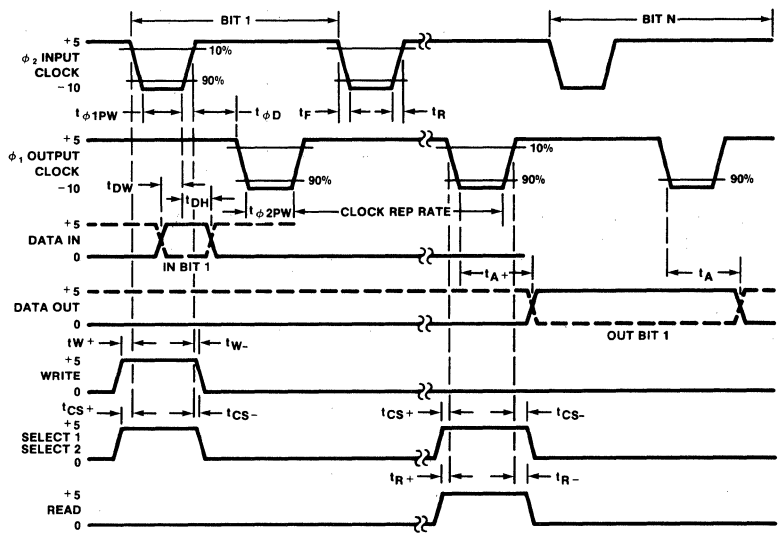
$T_A = 25°C$, $V_{CC} = 5V$[3], $V_{DD} = -5V \pm 5\%$, $V_{ILC} = -11V$

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock data rep rate			W = R = V_{CC}	.0005	3	2.5	MHz
$t_{\phi PW}$	Clock pulse width				180			ns
$t_{\phi D}$	Clock pulse delay				10			ns
t_r, t_F	Clock pulse transition						1	μs
	Setup and hold time							ns
t_{DW}	Setup time	Input clock	Data in		150			
t_{DH}	Hold time	Data in	Input clock		10			
t_{A+}, t_{A-}	Delay time	Data out	Clock				100	ns
	Clock to read or chip select or write timing							ns
t_{R-}, t_{CS-}, t_{W-}					0			
t_{R-}, t_{CS+}, T_{W+}					0			

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
4. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_O, and V_{CLAMP} and the value of the pull-down resistor (R_L).
5. All inputs are protected against static charge.
6. Parameters are valid over operating temperature range unless otherwise specified.
7. All voltage measurements are referenced to ground.
8. Manufacturer reserves the right to make design and process changes and improvements.
9. Typical values are at +25°C and typical supply voltage.

TIMING DIAGRAM



NOTES

A. N = 512 for the 2505, N = 1024 for the 2512.
B. Note that the read input is AND'ed with ϕ_1; therefore this function is not valid until ϕ_1 occurs.

512-BIT RECIRCULATING DYNAMIC SHIFT REGISTER (512X1) 2524
1024-BIT RECIRCULATING DYNAMIC SHIFT REGISTER (1024X1) 2525

2524-N • 2525-N

DESCRIPTION

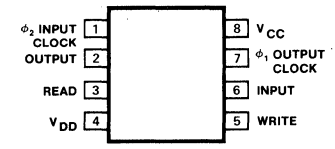
The 2525 1024-bit recirculating dynamic shift register consists of enhancement mode p-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls are included on the chip.

TRUTH TABLE

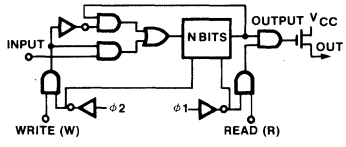
WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is data
1	0	Write mode, Output is '0'
1	1	Read mode, Output is data

PIN CONFIGURATION

N PACKAGE



BLOCK DIAGRAM



N = 512 or 1024, Low = 0V, High = +5V

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at $T_A > 70°C$[2]	535	mW
	Data and clock input voltages and supply voltages with respect to V_{CC}	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	2524			2525			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Input voltage[3]								V
V_{IL}	Low		-5.0		0.6	-5.0		0.6	
V_{IH}	High		3.4		5.3	3.4		5.3	
V_{ILC}	Clock low		-12.0		-10.0	-12.0		-10.0	
V_{IHC}	Clock high		4.0		5.3	4.0		5.3	
	Output voltage								V
V_{OL}	Low, driving 1 TTL load	$R_L = 3.0K$, 1 TTL load ($I_L = 1.6mA$)[4]		-1.0			-1.0		
V_{OH1}	High, driving 1 TTL load	$R_L = 3.0K$, 1 TTL load ($I_L = 100\mu A$)	2.4	3.5		2.4	3.5		
V_{OH2}	High, driving MOS	$R_L = 5.6K$, $C_L = 10pF$	3.6	4.0		3.6	4.0		
I_{LI}	Input load current	$V_{IN} = -5.5V$, $T_A = 25°C$		10	500		10	500	nA
	Leakage current	$T_A = 25°C$							nA
I_{LO}	Output	$V_{\phi 2} = V_{\phi 1} = -12V$, $V_{DD} = -5$, $V_{OUT} = -5.5V$		10	1000		10	1000	
I_{LC}	Clock	$V_{ILC} = -12V$		10	1000		10	1000	
I_{DD}	Supply current	Continuous operation, $\phi pW = 150ns$, $f = 1MHz$, $V_{ILC} = -12V$, $T_A = 25°C$, $V_{DD} = -5.5V$		15	35		25	35	mA
	Capacitance	1MHz, $V_{AC} = 25mV$ p-p							pF
C_{IN}	Input	$V_I = V_{CC}$			5			5	
C_{OUT}	Output	$V_O = V_{CC}$			5			5	
C_ϕ	Clock	$V = V_{CC}$			80			160	

AC ELECTRICAL CHARACTERISTICS

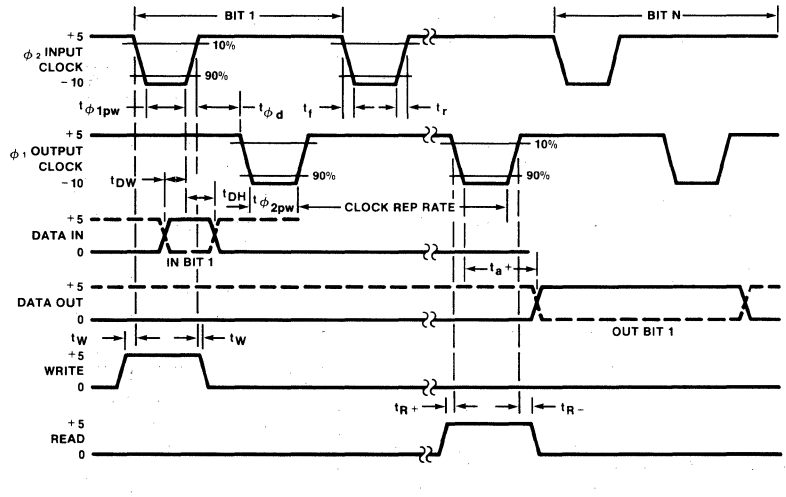
T_A = 25°C, V_{CC} = 5V ± 5%, V_{DD} = -5V ± 5%, V_{ILC} = -11V,
Input rise and fall times = 10ns, Output load = 1 TTL gate

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock data rep rate[5]			W = R = V_{CC}	.0005	5	3	MHz
$t_{\phi}PW$	Clock pulse width				135	85		ns
$t_{\phi D}$	Clock pulse delay				10			ns
t_R,t_F	Clock pulse transition				10		1000	ns
	Setup and hold time							ns
t_{DW}	Setup time	Clock	Data in		70			
t_{DH}	Hold time	Data in	Clock		20			
t_{A+}	Delay time	Data out	Clock				100	ns
t_{R-},t_{W-}	Clock to read or write timing				0			ns
t_{R-},t_{W+}	Clock to read or write timing				0			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.
4. V_{OL} is a function of the input characteristics of the driven TTL/DTL gate I_{OI} and V_{CLAMP} and the value of the pull-down resistor (R_L).
5. See Minimum Operating Frequency graph for low limits on data rep. rate.
6. All inputs are protected against static charge.
7. All voltage measurements are referenced to ground.
8. Manufacturer reserving the right to make design and process changes and improvements.
9. Typical values are at +25°C and typical supply voltages.
10. Parameters are valid over operating temperature range unless otherwise specified.

TIMING DIAGRAM



NOTES

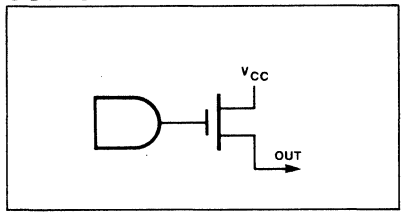
A. N = 512 for 2524, N = 1024 for 2525.
B. Note that the read input is AND'ed with $\overline{\phi_1}$; therefore this function is not valid until ϕ_1 occurs.

2502-N • 2503-TA,N • 2504-TA,N

DESCRIPTION

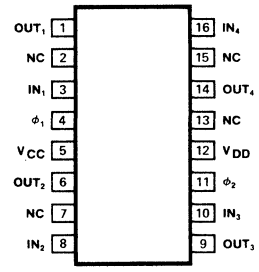
These 2500 Series 1024-bit multiplexed dynamic shift registers consist of enhancement mode p-channel MOS devices integrated on a single monolithic chip. Due to on-chip multiplexing, the data rate is twice the clock rate.

OUTPUT BUFFER

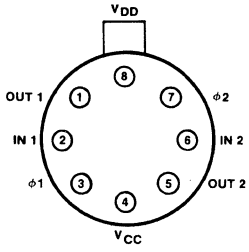


PIN CONFIGURATIONS

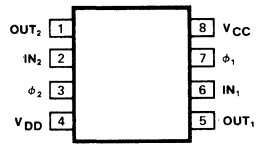
2502 N PACKAGE



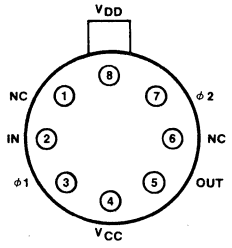
2503 TA PACKAGE



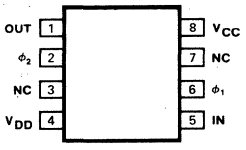
2503 N PACKAGE



2504 TA PACKAGE



2504 N PACKAGE



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range[2]		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation $T_A = 70°C$[2]		mW
	TA and N (8-pin) package	535	
	N (16-pin) package	640	
	Data and clock input voltages and supply voltages with respect to V_{CC}[3]	0.3 to -20	V

2502-N • 2503-TA,N • 2504-TA,N

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = -5V ± 5%, V_{CC} = 5V[4] unless otherwise specified[5,6,7,8]

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Input voltage					V
V_{IL}	Low				1.05	
V_{IH}	High		3.2		5.3	
V_{ILC}	Clock low		-10		-12	
V_{IHC}	Clock high		4.0		5.3	
	Output voltage					V
V_{OL}	Low	R_L = 3K, depends on R_L and TTL gate		-0.3		
V_{OH1}	High, driving MOS	R_L = 5.6K	3.6	4.0		
V_{OH2}	High, driving TTL	R_L = 3K	3.0	3.5		
I_{LI}	Input load current	V_{IN} = V_{CC} to V_{DD}, T_A = 25°C			500	nA
	Leakage current	T_A = 25°C				nA
I_{LO}	Output	$V_{\phi1}$ = $V_{\phi2}$ = -10V, V_{OUT} = 0.0V		10	1000	
I_{LC}	Clock	V_{ILC} = -10V		10	1000	
I_{DD}	Supply current	Outputs at logic low, 4MHz data rate, $\phi1$ = $\phi2$ = 85ns continuous operation, V_{ILC} = -12V, T_A = 25°C		15	25	mA
	Capacitance	At 1MHz, 25mV p-p, T_A = 25°C				pF
C_{IN}	Input		2.5		5	
C_{OUT}	Output		2.5		5	
C_ϕ	Clock		110		150	

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = -5V ± 5%, V_{CC} = 5V[3], V_{ILC} = -11V[4,5,6,7]

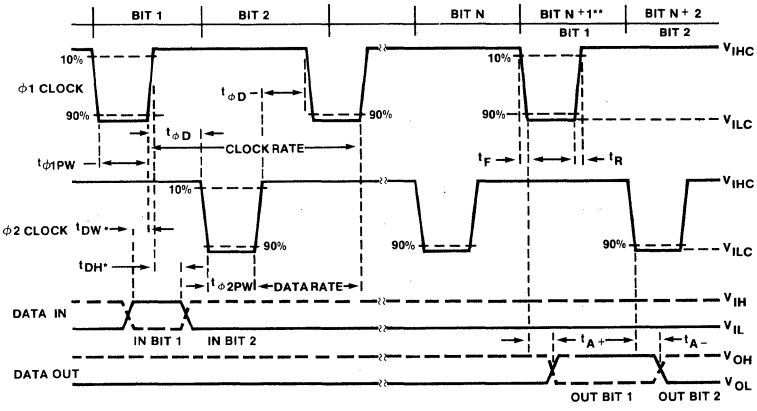
PARAMETER		LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Freq.	Rep rate				MHz
	Clock	0.0005		4	
	Data	0.001		8	
ϕ_{PW}	Clock pulse width	85			ns
ϕ_D	Clock pulse delay	10			ns
t_R,t_F	Clock pulse transition	10		1000	ns
t_W	Data write time (setup)	50			ns
t_{DO}	Data in overlap	10			ns
t_{A+},t_{A-}	Data out			90	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (TA and V package) or 125°C/W (B package).
3. All inputs are protected against static charge.
4. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
5. Parameters are valid over operating temperature range unless specified.
6. All voltage measurements are referenced to ground.
7. Manufacturer reserving the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.

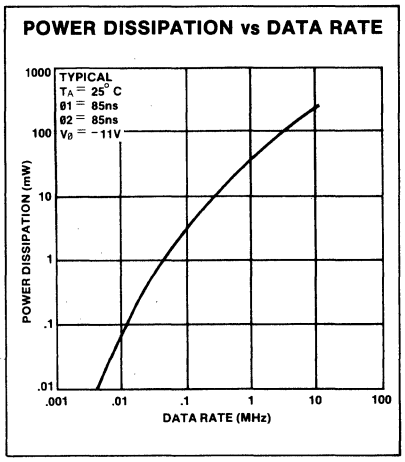
2502-N • 2503-TA,N • 2504-TA.N

TIMING DIAGRAM



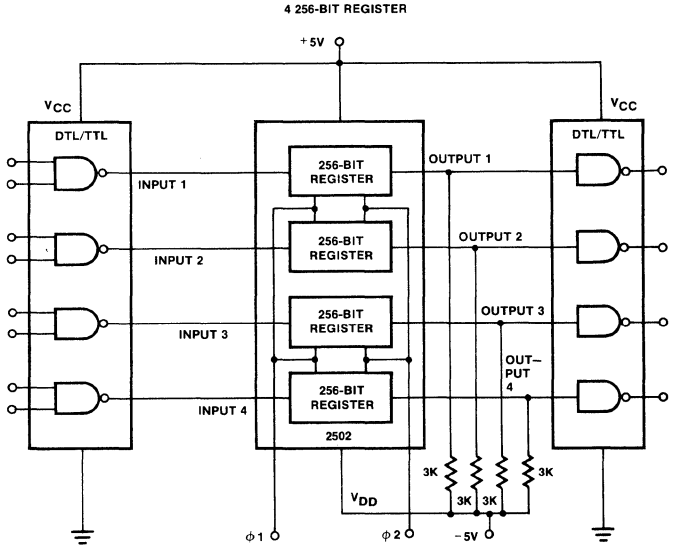
*t_{DW} and t_{DH} same for $t_{\phi 2}$
**N = 256 for 2502, N = 512 for 2503, N = 1024 for 2504

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATIONS

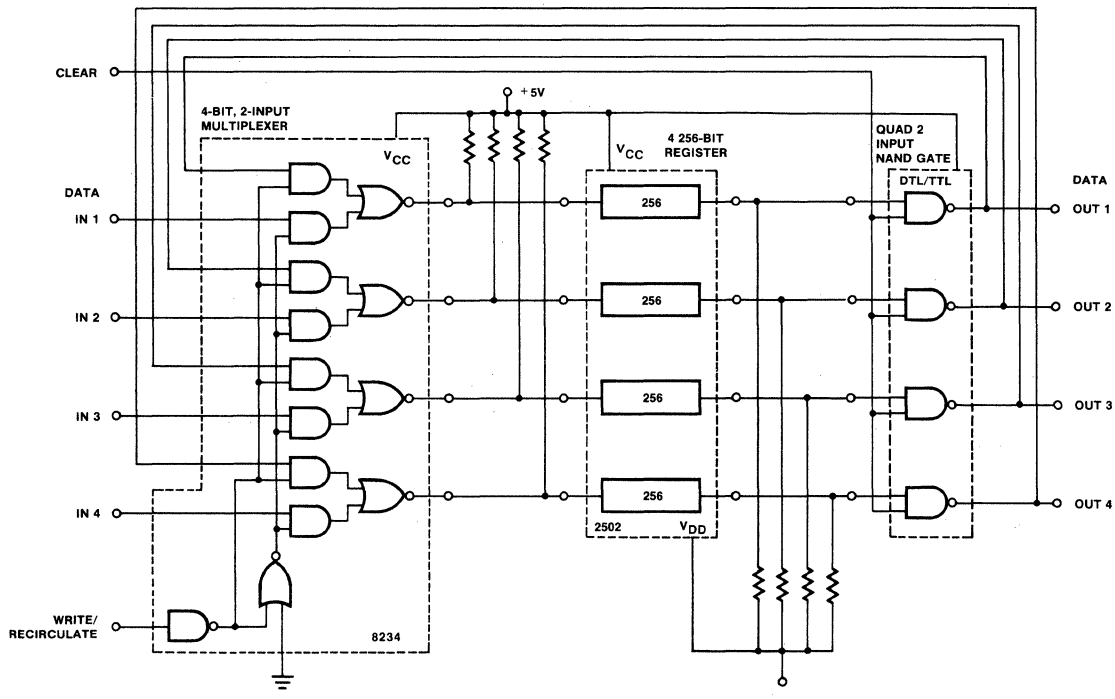
DTL/TTL/MOS INTERFACES



When interfacing MOS to MOS output resistors should be 4.7K min.

TYPICAL APPLICATIONS (Cont'd)

WRITE/RECIRCULATE LOGIC



All resistors 3kΩ 5%

MILITARY

The Signetics Mil 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customers to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 1 and 2.

	JB	JBX	RBX	RB	S
	JAN Qualified	JAN Processed	JAN Rel	/883	Mil Temp
54/54H	X	X	X	X	X
54LS	X	X	X	X	X
54S	X	X	X	X	X
82/8T	X	X	X	X	X
93XX	X	X	X	X	X
96XX	—	—	X	X	X
Linear	Planned	X	X	X	X
Bipolar Memory	Planned	—	X	X	X
Microprocessor	—	—	X	X	X

Table 1 MILITARY SUMMARY

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES				
			Dual-In-Line		
	8-Pin	10-Pin	14-Pin	16-Pin	24-Pin
CB	—	—	F	—	—
EB	—	—	—	F	—
JB	—	—	—	—	I/F*
DB	—	—	W	—	—
FB	—	—	—	W	—
ZC	—	—	—	—	Q
GC	T	—	—	—	—
IC	—	K	—	—	—

*The gold plated versions of these packages will be available for a limited time.
All products listed in the Military section are also available in Die form.

Table 2 MILITARY PACKAGE AVAILABILITY

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

JAN PROCESSING (JBX)

This option is extremely useful when the reliability and screening of a JAN device is required, however, Signetics is not listed on the QPL for the product needed. Processing is performed to Mil-Std-883 Method 5004, and product is 100% electrically tested to the appropriate JAN slash sheet.

Group B, C and D data for JAN processed and the other military processing levels which follow, consist of Group B, C and D testing performed per Mil-Std-883 Method 5005, in accordance with the Signetics Military Data Program.

JAN REL (RBX)

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets.

/883B (RB)

This is a lower priced version of the JAN Rel option described above. Processing is identical with the only exceptions being the dc electrical testing over the temperature range and ac electrical testing at room temperature are performed as a part of Group A instead of 100%.

MIL TEMP/883C (S/RC)

If you need a Military temp. range device, but do not require all the high reliability screening performed in the other processing options, our Mil-Temp. product is ideal. Mil-Temp. parts are the standard full Mil-Temperature range product guaranteed to a 1% AQL to the Signetics data sheet parameters.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 3.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A	Electrical Test	See NOTE 1	See NOTE 1
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied.	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE
1. Group A is performed on each lot or sublot of Signetics devices.

Table 3 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS					
			CLASS A	JAN Qualified (JB)	JAN Processed (JBX)	JAN Rel (RBX)	/883B (RB)	/883C (RC)
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program Plan B. Manufacturer's Certification	The manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A	N/A	N/A
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A	N/A	N/A
Screening Per Method 5004 of Mil-Std-883								
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X	X	X
8. Temperature Cycling* *For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)	1010, Cond. C; (10 cycles, -65°C to +150°C)	100%	X	X	X	X	X	X
9. Constant Acceleration	2001, Cond. E; (30_{kg} in YI Plane)	100%	X	X	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X	X	X
11. Seal (Hermeticity)	1014							
A. Fine	Cond. A or B (5.0 X 10^{-8}CC/Sec)	100%	X	X	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Slash Sheet	Data Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Slash Sheet	Data Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	X	N/A	N/A
C. Static Tests @ -55°C	Sub Group 3		X	X	X	X	N/A	N/A

Table 4 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS					
			CLASS A	JAN Qualified (JB)	JAN Processed (JBX)	JAN Rel (RBX)	/883B (RB)	/883C (RC)
D. Dynamic Test @ 25°C	Sub Group 4 for (Linear Product Mainly)		X	X	X	X	X	X
E. Functional Test @ 25°C	Sub Group 7		X	X	X	X	X	X
F. Switching Test @ 25°C	Sub Group 9		X	X	X	X	N/A	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @ 25°C (A-1). This is controlled by the slash sheets for JB & JBX products. For RBX & RB 10% is standard.	10%	5%	X	X	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/ XXXX Slash Sheet #	M38510/ XXXX Slash Sheet #	M38510/ SXXXX Sig. Basic #	SXXXX/ 883B Sig. Basic #	SXXXX/ 883C Sig. Basic #
17. X-Ray	2012		100%	N/A	N/A	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std-883								
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per microcircuit group	X	X	Generic Data Available			
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constant acceleration.	Every 3 months per package type	X	X	Generic Data Available			
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available			

Table 4 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS (Cont'd)

BIPOLAR MEMORIES CROSS REFERENCE

DEVICE	ORGANIZATION	PACKAGE*		FAIRCHILD	HARRIS	MMI	INTERSIL	AMD	TI
PROMs									
82S23	32X8	F	R	—	7602-2	5330	5600	27S08	54S188
82S115	512X8	I	R	—	7644-2	—	—	—	
82S123	32X8	F	R	—	7603-2	5331	5610	27S09	54S288
82S126	256X4	F	R	93416	7610-2	5300	5603	27S10	54S387
82S129	256X4	F	R	93426	7611-2	5301	5623	27S11	54S287
82S130	512X4	F	R	93436	7620-2	5305	5604	—	—
82S131	512X4	F	R	93446	7621-2	5306	5624	—	—
82S136	1024X4	F,I	R	93443	7642-2	5352	5606	—	—
82S137	1024X4	F,I	R	93453	7643-2	5353	5626	—	—
82S140	512X8	I	R	93438	7640-2	5340	5606	—	—
82S141	512X8	I	R	93448	7641-2	5341	5625	—	—
82S180	1024X8	I	R	—	—	5380	—	—	—
82S181	1024X8	I	R	—	—	5381	—	—	—
82S184	2048X4	I	R	—	—	—	—	—	—
82S185	2048X4	I	R	—	—	—	—	—	—
FPLAs									
82S100	16X48X8	I	R	93459	—	82S100	—	27S100	—
82S101	16X48X8	I	R	93458	—	82S101	—	27S101	—
PLAs									
82S200	16X48X8	I	R	—	—	—	—	—	—
82S201	16X48X8	I	R	—	—	—	—	—	—
RAMs									
54S89	16X4	F	R	—	—	—	—	—	5489
54S189	16X4	F	R	—	—	—	—	—	54189
54S200	256X1	F	R	—	—	—	—	—	54S200
54S201	256X1	F	R	—	—	—	—	—	54S201
54S301	256X1	F	R	—	—	—	—	—	54S301
82S09	64X9	I	R	93419	—	—	—	—	—
82S10	1024X1	F,I	R	93415	—	—	55S08	2952	—
82S11	1024X1	F,I	R	93425	—	—	55S18	2953	—
82S16	256X1	F	R	93421	—	5531	5523	2700	—
82S17	256X1	F	R	93411	—	5530	5533	2701	—
82S25	16X4	F	R	93403	0064	5560	5501	3101	—
ROMs									
82S15	512X8								
82S223	32X8								
82S224	32X8								
82S226	256X4								
82S229	256X4								
82S230	512X4								
82S231	512X4								
82S280	1024X8								
82S281	1024X8								

*NOTE

R = BeO Flat Pack
F = Cerdip
I = Ceramic DIP

LOGIC—5400 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL*		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
5400	Quad 2-Input NAND Gate	/00104	1	1	F	W	F	W
5401	Quad 2-Input NAND Gate with o/c	/00107	1	1	F	W	F	W
5402	Quad 2-Input NOR Gate	/00401	1	1	F	W	F	W
5403	Quad 2-Input NAND Gate with o/c	/00109	1	1	F	*	F	—
5404	Hex Inverter	/00105	1	1	F	W	F	W
5405	Hex Inverter with o/c	/00108	1	1	F	W	F	W
5406	Hex Inverter w/Buffer/Driver with o/c	/00801	—	—	F	W	F	W
5407	Hex Buffer/Driver with o/c	/00803	—	—	F	W	F	W
5408	Quad 2-Input AND Gate	/01601	1	1	F	W	F	W
5409	Quad 2-Input AND Gate with o/c	/01602	1	1	F	W	F	W
5410	Triple 3-Input NAND Gate	/00103	1	1	F	W	F	W
5411	Triple 3-Input NAND Gate	—	—	—	—	—	F	W
5412	Triple 3-Input NAND Gate wih o/c	/00106	—	—	—	—	F	W
5413	Dual NAND Schmitt Trigger	/15101	*	*	F	W	F	W
5414	Hex Schmitt Trigger	/15102	*	*	F	W	F	W
5416	Hex Inverter Buffer/Driver with o/c	/00802	—	—	F	W	F	W
5417	Hex Buffer/Driver with o/c	/00804	—	—	F	W	F	W
5420	Dual 4-Input NAND Gate	/00102	1	1	F	W	F	W
5421	Dual 4-Input AND Gate	—	—	—	—	—	F	W
5426	Quad 2-Input NAND Gate with o/c	/00805	1	—	F	—	F	—
5427	Triple 3-Input NOR Gate	/00404	*	*	F	W	F	W
5428	Quad 2-Input NOR Buffer	/16201	—	—	—	—	F	W
5430	8-Input NAND Gate	/00101	1	1	F	W	F	W
5432	Quad 2-Input OR Gate	/16101	*	*	—	—	F	W
5433	Quad 2-Input NOR Buffer with o/c	—	—	—	—	—	F	W
5437	Quad 2-Input NAND Buffer	/00302	1	1	F	W	F	W
5438	Quad 2-Input NAND Buffer with o/c	/00303	1	1	F	W	F	W
5439	Quad 2-Input NAND Buffer	—	—	—	—	—	F	W
5440	Dual 4-Input NAND Buffer	/00301	1	1	F	W	F	W
5442	BCD-to-Decimal Decoder	/01001	1	1	F	W	F	W
5443	Excess 3-to-Decimal Decoder	/01002	1	1	F	W	F	W
5444	Excess 3-Gray-to-Decimal Decoder	/01003	1	1	F	W	F	W
5445	BCD-to-Decimal Decoder/Driver with o/c	/01004	—	—	F	W	F	W
5446A	BCD-to-7 Segment Decoder/ Driver	/01006	—	—	F	W	F	W
5447A	BCD-to-7 Segment Decoder/ Driver	/01007	—	—	F	W	F	W
5448	BCD-to-7 Segment Decoder/ Driver	/01008	—	—	F	W	F	W
5450	Expandable Dual 2-Wide 2-Input A01	/00501	1	1	F	W	F	W
5451	Dual 2-Wide 2-Input A01 Gate	/00502	1	1	F	W	F	W
5453	4-Wide 2-Input A01 Gate (Expandable)	/00503	1	1	F	W	F	W
5454	4-Wide 2-Input A01 Gate	/00504	1	1	F	W	F	W
5455	2-Wide 4-Input A01 Gate	/04005	—	—	—	—	—	—

NOTE

Per QPL 38510-28 dated 1 Apr. 1977
1 = Level 1 Qualification
2 = Level 2 Qualification
* = In process

LOGIC—5400 SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL*		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
5460	Dual 4-Input Expander	—	—	—	—	—	F	W
5470	J-K Flip-Flop	/00206	1	1	F	W	F	W
5472	J-K Master-Slave Flip-Flop	/00201	1	1	F	W	F	W
5473	Dual J-K Master-Slave Flip-Flop	/00202	1	1	F	W	F	W
5474	Dual D-Type Edge-Triggered Flip-Flop	/00205	1	1	F	W	F	W
5475	Quad Bistable Latch	/01501	1	1	F	W	F	W
5476	Dual J-K Master-Slave Flip-Flop	/00204	1	1	F	W	F	W
5477	Quad Bistable Latch	/01502	—	1	—	W	—	W
5480	Gated Full Adder	—	—	—	—	—	F	W
5483	4-Bit Binary Full Adder	/00602	1	1	F	W	F	W
5485	4-Bit Magnitude Comparator	/15001	1	1	F	W	F	W
5486	Quad 2-Input Exclusive-OR Gate	/00701	1	1	F	W	F	W
5490	Decade Counter	/01307	*	*	F	W	F	W
5491	8-Bit Shift Register	—	—	—	—	—	F	W
5492	Divide-by-Twelve Counter	/01301	1	1	F	W	F	W
5493	4-Bit Binary Counter	/01302	1	1	F	W	F	W
5494	4-Bit Shift Register (PISO)	—	—	—	—	—	F	W
5495	4-Bit Left-Right Shift Register	/00901	1	—	F	—	F	W
5496	5-Bit Shift Register	/00902	1	1	F	W	F	W
54100	4-Bit Bistable Latch (Dual)	—	—	—	—	—	F	W
54107	Dual J-K Master-Slave Flip-Flop	/00203	1	—	F	—	F	—
54109	Dual J-K Positive Edge-Triggered Flip-Flop	—	—	—	—	—	F	W
54116	Dual 4-Bit Latch with Clear	/01503	2	—	I	—	I	—
54121	Monostable Multivibrator	/01201	1	1	F	W	F	W
54122	Retriggerable Monostable Multivibrator	/01202	—	—	—	—	—	—
54123	Retriggerable Monostable Multivibrator	/01203	1	1	F	W	F	W
54125	Quad Bus Buffer Gate w/Tri-State Outputs	/15301	2	2	F	W	F	W
54126	Quad Bus Buffer Gate w/Tri-State Outputs	/15302	2	2	F	W	F	W
54128	Quad 2-Input NOR Buffer	—	—	—	—	—	F	W
54132	Quad Schmitt Trigger	/15103	*	*	F	W	F	W
54145	BCD-to-Decimal Decoder/Driver with o/c	/01005	—	—	F	W	F	W
54147	10-Line to 4-Line Priority Encoder	/15601	*	*	F	W	F	W
54148	8-Line to 3-Line Priority Encoder	/15602	*	*	F	W	F	W
54150	16-Line to 1-Line Mux	/01401	2	—	I	—	I	—
54151	8-Line to 1-Line Mux	/01406	2	2	F	W	F	W
54152	8-Line to 1-Line Mux	—	—	—	—	—	F	W
54153	Dual 4-Line to 1-Line Mux	/01403	2	2	F	W	F	W
54154	4-Line to 16-Line Decoder/ Demux	/15201	*	—	I	—	I	Q
54155	Dual 2-Line to 4-Line Decoder/Demux	/15202	2	2	F	W	F	W
54156	Dual 2-Line to 4-Line Decoder/Demux	/15203	2	2	F	W	F	W
54157	Quad 2-Input Data Selector (non-inv.)	/01405	1	1	F	W	F	W
54158	Quad 2-Input Data Selector (inv.)	—	—	—	—	—	F	W
54160	Synchronous 4-Bit Decade Counter	/01303	1	1	F	W	F	W

NOTE

Per QPL 38510-28 dated 1 Apr. 1977
1 = Level 1 Qualification
2 = Level 2 Qualification
* = In process

LOGIC—5400 SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54161	Synchronous 4-Bit Binary Counter	/01306	1	1	F	W	F	W
54162	Synchronous 4-Bit Decade Counter	/01305	1	1	F	W	F	W
54163	Synchronous 4-Bit Binary Counter	/01304	1	1	F	W	F	W
54164	8-Bit Parallel-Out Serial Shift Register	/00903	1	—	F	—	F	—
54165	Parallel-Load 8-Bit Shift Register	/00904	*	*	F	W	F	W
			—	—	—	—	F	W
54166	8-Bit Shift Register	—	—	—	—	—	F	—
54170	4X4 Register File	/01801						
54174	Hex D-Type Flip-Flop with Clear	/01701	1	1	F	W	F	W
54175	Quad D-Type Edge-Triggered Flip-Flop	/01702	1	1	F	W	F	W
54180	8-Bit Odd/Even Parity Checker	/01901	—	2	F	W	F	W
54181	4-Bit Arithmetic Logic Unit	/01101	1	—	I	—	I	—
54182	Look-Ahead Carry Generator	/01102	1	1	F	W	F	W
54190	Synchronous Up/Down Counter (BCD)	—	—	—	—	—	*	*
54191	Synchronous Up/Down Counter (Binary)	—	—	—	—	—	*	*
54192	Synchronous Decade Up/Down Counter	/01308	*	*	F	W	F	W
54193	Synchronous 4-Bit Binary Up/Down Counter	/01309	*	*	F	W	F	W
54194	4-Bit Bidirectional Universal Shift Register	/00905	*	*	F	W	F	W
54195	4-Bit Parallel-Access Shift Register	/00906	*	*	F	W	F	W
54198	8-Bit Shift Register	—	—	—	—	—	I	Q
54199	8-Bit Shift Register	—	—	—	—	—	—	—
54221	Dual Monostable Multivibrator	—	—	—	—	—	F	W
54279	Quad S-R Latch	—	—	—	—	—	F	W
54298	Quad 2-Input Mux with Storage	—	—	—	—	—	F	W
54365	Hex Buffer w/Common Enable (3-State)	/16301	*	*	*	*	*	*
54366	Hex Buffer w/Common Enable (3-State)	/16302	*	*	*	*	F	W
54367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16303	*	*	*	*	F	W
54368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16304	*	*	*	*	F	W

NOTE

Per QPL 38510-28 dated 1 Apr. 1977
1 = Level 1 Qualification
2 = Level 2 Qualification
* = In process

LOGIC—54H SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54H00	Quad 2-Input NAND Gate	/02304	1	1	F	W	F	W
54H01	Quad 2-Input NAND Gate with o/c	/02306	1	1	F	W	F	W
54H04	Hex Inverter	/02305	1	1	F	W	F	W
54H05	Hex Inverter with o/c	—	—	—	—	—	F	W
54H08	Quad 2-Input AND Gate	/15501	2	—	F	—	F	W
54H10	Triple 3-Input NAND Gate	/02303	1	1	F	W	F	W
54H11	Triple 3-Input NAND Gate	/15502	2	—	F	—	F	W
54H20	Dual 4-Input NAND Gate	/02302	1	1	F	W	F	W
54H21	Dual 4-Input AND Gate	/15503	2	—	F	—	F	W
54H22	Dual 4-Input NAND Gate with o/c	/02307	1	—	F	W	F	W
54H30	8-Input NAND Gate	/02301	1	1	F	W	F	W
54H40	Dual 4-Input NAND Buffer	/02401	1	1	F	W	F	W
54H50	Expandable Dual 2-Wide 2-Input A01	/04001	1	1	F	W	F	W
54H51	Dual 2-Wide 2-Input A01 Gate	/04002	1	1	F	W	F	W
54H52	Expandable 4-Wide 2-2-2-3 Input AND-OR Gate	—	—	—	—	—	F	W
54H53	4-Wide 2-Input A01 Gate (Expandable)	/04003	1	1	F	W	F	W
54H54	4-Wide 2-Input A01 Gate	/04004	1	1	F	W	F	W
54H55	2-Wide 2-Input A01 Gate	/04005	1	1	F	W	F	W
54H60	Dual 4-Input Expander	—	—	—	—	—	F	W
54H61	Triple 3-Input Expander	—	—	—	—	—	F	W
54H62	3-2-2-3 Input AND-OR Expander	—	—	—	—	—	F	W
54H71	J-K Master-Slave Flip-Flop with AND-OR Inputs	—	—	—	—	—	F	W
54H72	J-K Master-Slave Flip-Flop	/02201	1	1	F	W	F	W
54H73	Dual J-K Master-Slave Flip-Flop	/02202	1	1	F	W	F	W
54H74	Dual D-Type Edge-Triggered Flip-Flop	/02203	1	1	F	W	F	W
54H76	Dual J-K Master-Slave Flip-Flop	/02204	1	1	F	W	F	W
54H101	J-K Negative Edge-Triggered Flip-Flop	/02205	1	1	F	W	F	W
54H102	J-K Negative Edge-Triggered Flip-Flop	—	—	—	—	—	F	W
54H103	Dual J-K Negative Edge-Triggered Flip-Flop	/02206	1	1	F	W	F	W
54H106	Dual J-K Negative Edge-Triggered Flip-Flop	—	—	—	—	—	F	W
54H108	Dual J-K Negative Edge-Triggered Flip-Flop	—	—	—	—	—	F	—

NOTE

Per QPL 38510-28 dated 1 April 1977.
1 = Level 1 Qualification
2 = Level 2 Qualification

LOGIC—54LS SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54LS00	Quad 2-Input NAND Gate	/30001	2	2	F	W	F	W
54LS01	Quad 2-Input NAND Gate with o/c	—	—	—	F	W	F	W
54LS02	Quad 2-Input NOR Gate	/30301	2	2	F	W	F	W
54LS03	Quad 2-Input NAND Gate with o/c	/30002	1	1	F	W	F	W
54LS04	Hex Inverter	/30003	1	1	F	W	F	W
54LS05	Hex Inverter with o/c	/30004	1	1	F	W	F	W
54LS08	Quad 2-Input AND Gate	/31004	2	2	F	W	F	W
54LS09	Quad 2-Input AND Gate with o/c	—	—	—	—	—	F	W
54LS10	Triple 3-Input NAND Gate	/30005	1	1	F	W	F	W
54LS11	Triple 3-Input NAND Gate	/31001	2	2	F	W	F	W
54LS12	Triple 3-Input NAND Gate with o/c	/30006	1	1	F	W	F	W
54LS13	Dual NAND Schmitt Trigger	/31301	*	*	F	W	F	W
54LS14	Hex Schmitt Trigger	/31302	*	*	F	W	F	W
54LS15	Triple 3-Input AND Gate with o/c	/31002	2	2	F	W	F	W
54LS20	Dual 4-Input NAND Gate	/30007	1	1	F	W	F	W
54LS21	Dual 4-Input AND Gate	/31003	2	2	F	W	F	W
54LS22	Dual 4-Input NAND Gate with o/c	/30008	1	1	F	W	F	W
54LS26	Quad 2-Input NAND Gate with o/c	/32101	*	*	F	W	F	W
54LS27	Triple 3-Input NOR Gate	/30302	2	2	F	W	F	W
54LS28	Quad 2-Input NOR Buffer	/30204	*	*	F	W	F	W
54LS30	8-Input NAND Gate	/30009	2	2	F	W	F	W
54LS32	Quad 2-Input OR Gate	/30501	2	2	F	W	F	W
54LS33	Quad 2-Input NOR Buffer with o/c	—	—	—	—	—	F	W
54LS37	Quad 2-Input NAND Buffer	/30202	2	2	F	W	F	W
54LS38	Quad 2-Input NAND Buffer with o/c	/30203	*	*	F	W	F	W
54LS40	Dual 4-Input NAND Buffer	/30201	2	2	F	W	F	W
54LS42	BCD-to-Decimal Decoder	/30703	*	*	*	*	F	W
54LS51	Dual 2-Wide 2-Input A01 Gate	/03401	2	2	F	W	F	W
54LS54	4-Wide 2-Input A01 Gate	/30402	2	2	F	W	F	W
54LS55	2-Wide 4-Input A01 Gate	—	—	—	—	—	F	W
54LS73	Dual J-K Master-Slave Flip-Flop	/30101	—	—	—	—	F	W
54LS74	Dual D-Type Edge-Triggered Flip-Flop	/30102	*	*	F	W	F	W
54LS75	Quad Bistable Latch	—	—	—	F	W	F	W
54LS76	Dual J-K Master-Slave Flip-Flop	/30110	*	*	F	W	F	W
54LS78	Quad Bistable Latch	—	—	—	—	—	F	W
54LS83A	4-Bit Binary Full Adder	/31201	*	*	F	W	F	W
54LS85	4-Bit Magnitude Comparator	/31101	*	*	F	W	F	W
54LS86	Quad 2-Input Exclusive-OR Gate	/30502	*	*	F	W	F	W
54LS90	Decade Counter	/31501	*	*	F	W	F	W
54LS92	Divide-by-Twelve Counter	/31510	*	*	F	W	F	W
54LS93	4-Bit Binary Counter	/31502	*	*	F	W	F	W
54LS95	4-Bit Left-Right Shift Register	/30603	*	*	F	W	F	W
54LS96	5-Bit Shift Register	/30604	*	*	F	W	F	W

NOTE

Per QPL 38510-28 dated 1 April 1977.
1 = Level 1 Qualification
2 = Level 2 Qualification

LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54LS107	Dual J-K Master-Slave Flip-Flop	/30108	*	*	F	W	F	W
54LS109	Dual J-K Positive Edge-Triggered Flip-Flop	/30109	*	*	F	W	F	W
54LS112	Dual J-K Negative Edge-Triggered Flip-Flop	/30103	*	*	F	W	F	W
54LS113	Dual J-K Negative Edge-Triggered Flip-Flop	/30104	*	*	F	W	F	W
54LS114	Dual J-K Negative Edge-Triggered Flip-Flop	/30105	*	*	F	W	F	W
54LS122	Retriggerable Monostable Multivibrator	/31403	—	—	—	—	—	—
54LS125	Quad Bus Buffer Gate w/Tri-State Outputs	/32301	*	*	*	*	F	W
54LS126	Quad Bus Buffer Gate w/Tri-State Outputs	/32302	*	*	*	*	F	W
54LS132	Quad Schmitt Trigger	/31303	*	*	F	W	F	W
54LS136	Quad Exclusive-OR with o/c	—	—	—			F	W
54LS138	3-to-8 Line Decoder/Demux	/30701	*	*	*	*	F	W
54LS139	Dual 2-to-4 Line Decoder/ Demux	/30702	*	*	*	*	F	W
54LS145	BCD to Decimal Decoder/Dye	—	—	—	—	—	F	W
54LS151	8-Line to 1-Line Mux	/30901	*	*	*	*	*	*
54LS153	Dual 4-Line to 1-Line Mux	/30902	*	*	F	W	F	W
54LS154	4-Line to 16-Line Decoder/ Demux	—	—	—	—	—	I	Q
54LS155	Dual 2-Line to 4-Line Decoder/Demux	—	—	—	—	—	F	W
54LS157	Quad 2-Input Data Selector (non-inv.)	/30903	*	*	F	W	F	W
54LS158	Quad 2-Input Data Selector (inv.)	/30904	*	*	F	W	F	W
54LS160	Synchronous 4-Bit Decade Counter	/31503	*	*	*	*	F	W
54LS161	Synchronous 4-Bit Binary Counter	/31504	*	*	F	W	F	W
54LS162	Synchronous 4-Bit Decade Counter	/31511	*	*	*	*	F	W
54LS163	Synchronous 4-Bit Binary Counter	/31512	*	*	*	*	F	W
54LS164	8-Bit Parallel-Out Serial Shift Register	/30605	*	*	F	W	F	W
54LS170	4X4 Register File	—	—	—	—	—	F	W
54LS173	Quad D-Type Flip-Flop (Tri-State) (8T10)	—	—	—	—	—	F	W
54LS174	Hex D-Type Flip-Flop with Clear	/30106	*	*	F	W	F	W
54LS175	Quad D-Type Edge-Triggered Flip-Flop	/30107	*	*	F	W	F	W
54LS181	4-Bit Arithmetic Logic Unit	/03801	2	—	I	—	I	Q
54LS190	Synchronous Up/Down Counter (BCD)	/31513	*	*	F	W	F	W
54LS191	Synchronous Up/Down Counter (Binary)	/31509	*	*	F	W	F	W

NOTE

Per QPL 38510-28 dated 1 April 1977.
1 = Level 1 Qualification
2 = Level 2 Qualification

LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54LS192	Synchronous Decade Up/Down Counter	/31507	*	*	F	W	F	W
54LS193	Synchronous 4-Bit Binary Up/Down Counter	/31508	*	*	F	W	F	W
54LS194	4-Bit Bidirectional Universal Shift Register	/30601	*	*	*	*	*	*
54LS195	4-Bit Parallel-Access Shift Register	/30602	*	*	*	*	*	*
54LS196	Presettable Decade Counter/ Latch (8290)	/31601	*	*	*	*	*	*
54LS197	Presettable Binary Counter/ Latch (8291)	/31602	*	*	*	*	*	*
54LS221	Dual Monostable Multivibrator	/31402	*	*	*	*	*	*
54LS251	Data Selector/Mux with 3-State Outputs	/30905	*	*	*	*	*	*
54LS253	Dual 4-Line to 1-Line Data Selector/Mux	/30908	*	*	F	W	F	W
54LS257	Quad 2-Line to 1-Line Data Selector/Mux	/30906	*	*	F	W	F	W
54LS258	Quad 2-Line to 1-Line Data Selector/Mux	/30907	*	*	*	*	F	W
54LS260	Dual 5-Input NOR Gate	—	—	—	—	—	F	W
54LS261	2X4 Parallel Binary Multiplier	—	—	—	—	—	F	W
54LS266	Quad Exclusive-NOR Gate	/30303	2	2	F	W	F	W
54LS279	Quad S-R Latch	—	—	—	—	—	F	W
54LS280	9-Bit Odd/Even Parity Generator/Checker	—	—	—	—	—	*	*
54LS283	4-Bit Adder	/31202	*	*	*	*	F	W
54LS290	Decade Counter	/32003	*	*	F	W	F	W
54LS293	4-Bit Binary Counter	/32004	*	*	F	W	F	W
54LS295A	4-Bit Right-Shift Left-Shift Register	/30606	*	*	*	*	F	W
54LS298	Quad 2-Input Mux with Storage	—	—	—	—	—	F	W
54LS365	Hex Buffer w/Common Enable (3-State)	/32201	*	*	*	*	F	W
54LS366	Hex Buffer w/Common Enable (3-State)	/32202	*	*	*	*	F	W
54LS367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32203	*	*	*	*	F	W
54LS368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32204	*	*	*	*	F	W
54LS375	Quad Latch	—	—	—	—	—	F	W
54LS386	Exclusive-OR Gate	—	—	—	—	—	F	W
54LS395	4-Bit Cascadeable Shift Register (3-State)	/30607	*	*	*	*	F	W
54LS445	BCD to Decimal Decoder/Dye	—	—	—	—	—	F	W
54LS670	4X4 Register File (Tri-State)	—	—	—	—	—	F	W

NOTE

Per QPL 38510-28 dated 1 April 1977.
1 = Level 1 Qualification
2 = Level 2 Qualification

LOGIC—54S SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54S00	Quad 2-Input NAND Gate	/07001	1	1	F	W	F	W
54S02	Quad 2-Input NOR Gate	/07301	2	2	F	W	F	W
54S03	Quad 2-Input NAND Gate with o/c	/07002	2	2	F	W	F	W
54S04	Hex Inverter	/07003	1	1	F	W	F	W
54S05	Hex Inverter with o/c	/07004	1	1	F	W	F	W
54S08	Quad 2-Input AND Gate	/08003	*	*	F	W	F	W
54S09	Quad 2-Input AND Gate with o/c	/08004	—	—	—	—	F	W
54S10	Triple 3-Input NAND Gate	/07005	2	2	F	W	F	W
54S11	Triple 3-Input NAND Gate	/08001	2	2	F	W	F	W
54S15	Triple 3-Input AND Gate with o/c	/08002	2	2	F	W	F	W
54S20	Dual 4-Input NAND Gate	/07006	2	2	F	W	F	W
54S22	Dual 4-Input NAND Gate with o/c	/07007	1	1	F	W	F	W
54S30	8-Input NAND Gate	/07008	—	—	—	—	—	—
54S32	Quad 2-Input OR Gate	—	—	—	—	—	F	W
54S40	Dual 4-Input NAND Buffer	/07201	2	2	F	W	F	W
54S51	Dual 2-Wide 2-Input A01 Gate	/07401	2	2	F	W	F	W
54S64	4-2-3-2 Input A01 Gate	/07402	2	2	F	W	F	W
54S65	4-2-3-2 Input A01 Gate	/07403	2	2	F	W	F	W
54S74	Dual D-Type Edge-Triggered Flip-Flop	/07101	2	2	F	W	F	W
54S85	4-Bit Magnitude Comparator	/08201	*	—	F	—	F	—
54S86	Quad 2-Input Exclusive-OR Gate	/07501	2	2	F	W	F	W
54S112	Dual J-K Negative Edge-Triggered Flip-Flop	/07102	—	—	—	—	F	W
54S113	Dual J-K Negative Edge-Triggered Flip-Flop	/07103	—	—	—	—	F	W
54S114	Dual J-K Negative Edge-Triggered Flip-Flop	/07104	—	—	—	—	F	W
54S133	13-Input NAND Gate	/07009	2	2	F	W	F	W
54S134	12-Input NAND Gate w/Tri-State Outputs	/07010	2	2	F	W	F	W
54S135	Quad Exclusive-OR/NOR Gate	/07502	—	—	—	—	—	—
54S138	3-to-8 Line Decoder/Demux	/07701	—	—	—	—	—	—
54S139	Dual 2-to-4 Line Decoder/ Demux	/07702	—	—	—	—	F	W
54S140	Dual 4-Input NAND Line Driver	/08101	2	2	F	W	F	W
54S151	8-Line to 1-Line Mux	/07901	2	2	F	W	F	W
54S153	Dual 4-Line to 1-Line Mux	/07902	2	2	F	W	F	W
54S157	Quad 2-Input Data Selector (non.inv.)	/07903	2	2	F	W	F	W
54S158	Quad 2-Input Data Selector (inv.)	/07904	*	*	F	W	F	W
54S174	Hex D-Type Flip-Flop with Clear	/07106	—	—	—	—	*	*
54S175	Quad D-Type Edge-Triggered Flip-Flop	/07105	—	—	—	—	*	*
54S181	4-Bit Arithmetic Logic Unit	/07801	*	—	I	—	I	*
54S182	Look-Ahead Carry Generator	/07802	—	—	—	—	*	*
54S194	4-Bit Bidirectional Universal Shift Register	/07601	—	—	—	—	—	—
54S195	4-Bit Parallel-Access Shift Register	/07602	—	—	—	—	—	—

NOTE

Per QPL 38510-28 dated 1 April 1977.
1 = Level 1 Qualification
2 = Level 2 Qualification

LOGIC—54S SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUAL		JAN PROC-ESSED		MIL REL/883	
			DIP	FLATPACK	DIP	FLATPACK	DIP	FLATPACK
54S251	Data Selector/Mux with 3-State Outputs	/08905	—	—	—	—	—	—
54S253	Dual 4-Line to 1-Line Data Selector/Mux	—	—	—	—	—	F	W
54S257	Quad 2-Line to 1-Line Data Selector/Mux	/07906	—	—	—	—	—	—
54S258	Quad 2-Lint to 1-Line Data Selector/Mux	/07907	—	—	—	—	—	—
54S260	Dual 5-Input NOR Gate	—	—	—	—	—	F	W
54S280	9-Bit Odd/Even Parity Generator/Checker	/07703	—	—	—	—	—	—
54S350	4/6 Bit Shifter-Tri-State	—	—	—	—	—	F	—

NOTE

Per QPL 38510-28 dated 1 Apr. 1977
1 = Level 1 Qualification
2 = Level 2 Qualification

LOGIC—8200/9300/9600 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED*		JAN PROCESSED		MIL REL/883 MIL TEMP	
			Dip	Flat Pack	Dip	Flat Pack	Dip	Flat Pack
8200	Dual 5-Bit Buffer Register	—	—	—	—	—	I	Q
8201	Dual 5-Bit Buffer Register with D Inputs	—		—	—	—	I	Q
8202	10-Bit Buffer Register	—	—	—	—	—	I	Q
8203	10-Bit Buffer Register with D Inputs	—	—	—	—	—	I	Q
8230	8-Input Digital Multiplexer	/01402	*	*	F	W	F	W
8231	8-Input Digital Multiplexer	—	—	—	—	—	F	W
8232	8-Input Digital Multiplexer	—	—	—	—	—	F	W
8233	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8234	2-Input 4-Bit Digital Multiplexer		—	—	—	—	F	W
8235	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8241	Quad Exclusive-OR Gate	—	—	—	—	—	F	W
8242	Quad Exclusive-NOR Gate	—	—	—	—	—	F	W
8243	8-Bit Position Scaler	—	—	—	—	—	I	Q
8250	Binary-to-Octal Decoder	/15204	2	2	F	W	F	W
8251	BCD-to-Decimal Decoder	/15205	2	2	F	W	F	W
8252	BCD-to-Decimal Decoder	/15206	2	2	F	W	F	W
8260	Arithmetic Logic Unit	—	—	—	—	—	I	Q
8261	Fast Carry Extender	—	—	—	—	—	F	W
8262	9-Bit Parity Generator and Checker	—	—	—	—	—	F	W
8263	3-Input 4-Bit Digital Multiplexer	—	—	—	—	—	I	Q
8264	3-Input 4-Bit Digital Multiplexer		—	—	—	—	I	Q
8266	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8267	2-Input 4-Bit Digital Multiplexer	—	—	—	—	—	F	W
8268	Gated Full Adder	—	—	—	—	—	F	Q
8269	4-Bit Comparator	—	—	—	—	—	F	W
8270	4-Bit Shift Register	—	—	—	—	—	F	W
8271	4-Bit Shift Register	—	—	—	—	—	F	W
8273	10-Bit Serial-In, Parallel-Out Shift Register	—	—	—	—	—	F	W
8274	10-Bit Parallel-In, Serial-Out Shift Register	—	—	—	—	—	F	W
8275	Quad Bistable Latch	—	—	—	—	—	F	W
8276	8-Bit Serial Shift Register	—	—	—	—	—	F	—
8277	Dual 8-Bit Shift Register	—	—	—	—	—	F	—
8280	Presettable Decade Counter	—	—	—	—	—	F	W
8281	Presettable Binary Counter	—	—	—	—	—	F	W
8284	Binary Up/Down Counter	—	—	—	—	—	F	W
8285	Decade Up/Down Counter	—	—	—	—	—	F	W
8288	Divide-by-Twelve Counter	—	—	—	—	—	F	W
8290	Presettable High Speed Decade Counter	—	—	—	—	—	F	W
8291	Presettable High Speed Binary Counter	—	—	—	—	—	F	W
8292	Presettable Low Power Decade Counter	—	—	—	—	—	F	W
8293	Presettable Low Power Binary Counter	—	—	—	—	—	F	W
9300	4-Bit Shift Register	/15901	*	*	F	W	F	W
9301	BCD to Decimal Decoder	/15206	2	2	F	W	F	W
9308	Dual 4-Bit Latch w/Clear	—	—	—	—	—	I	Q
9309	Dual 4-Input Multiplexer	/01404	I	I	F	W	F	W
9310	4-Bit Decade Counter	—	—	—	—	—	F	W
9312	8-Input Digital Multiplexer	/01402	*	*	F	W	F	W
9316	4-Bit Binary Counter	—	—	—	—	—	F	W
9322	Data Selector-Multiplexer	—	—	—	—	—	F	W
9324	5-Bit Comparator	/15002	*	*	F	WF	W	—
9334	8-Bit Addressable Latch	/16001	—	—	—	—	F	W
9602	Dual Monostable Multivibrator	—	*	*	F	W	F	W

NOTE

Per QPL 38510-28 dated 1 Apr. 1977
1 = Level 1 Qualification
2 = Level 2 Qualification

LOGIC—8T INTERFACE SERIES

DEVICE	DESCRIPTION	JAN M38510 SHEET	MIL REL/883 MIL TEMP	
			Dip	Flat Pack
8T04	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T05	7-Segment Decoder Display Driver (Active-Hi Outputs)	—	F	W
8T06	7-Segment Decoder Display Driver (Active-Low Outputs)	—	F	W
8T09	Quad Bus Driver with Tri-State Outputs	—	F	W
8T10	Quad D-Type Bus Latch (Tri-State)	—	F	W
8T13	Dual Line Driver	—	F	W
8T14	Triple Line Receiver/Schmitt Trigger	—	F	W
8T18	Dual 2-Input NAND (High Voltage to TTL Interface)	—	F	W
8T20	Bidirectional Monostable Multivibrator (Diff. Input)	—	*	*
8T22	Retriggerable Monostable Multivibrator (54122/9601)	—	F	W
8T26A	Quad Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T28	Quad Non-Inverting Bus Driver/Receiver (Tri-State Outputs)	—	F	W
8T31	8-Bit Bidirectional I/O Port	—	*	*
8T32	Programmable 8-Bit, I/O Port (3-State)	—	I	*
8T33	Programmable 8-Bit, I/O Port (Open Collector)	—	I	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	—	I	*
8T37	Hex Bus Receiver with Hysteresis—Schmitt Trigger (DM8837)		F	W
8T38	Quad Bus Transceiver (Open Collector) (DM8838)	—	F	W
8T80	Quad 2-Input NAND Gate (High Voltage)	—	F	W
8T90	Hex Inverter (High Voltage)	—	F	W
8T95	High Speed Hex Buffers/Inverters (74365/DM8095)	—	F	W
8T96	High Speed Hex Buffers/Inverters (74366/DM8096)	—	F	W
8T97	High Speed Hex Buffers/Inverters (74367/DM8097)		F	W
8T98	High Speed Hex Buffers/Inverters (74368/DM8098)		F	W

* = Qualification planned

LINEAR INDUSTRY CROSS REFERENCE

DEVICE	DESCRIPTION	PACKAGE	
	COMPARATORS		
SE521	Dual Comparator	F	
SE526	Analog Voltage Comparator	F	K
SE527	Analog Voltage Comparator	F	K
SE529	Analog Voltage Comparator	F	K
LH2111	Dual Comparator	F	
LM111	Comparator	F	T
LM119	Dual Comparator	F	K
LM139	Quad Comparator	F	
LM193/193A	Dual Comparator		T
μA710	Differential Voltage Comparator	F	T
μA711	Comparator	F	K
	DIFFERENTIAL AMPLIFIERS		
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
SE515	Differential Amplifier	F	K
μA733	Video Amplifier	F	K
	OPERATIONAL AMPLIFIERS		
LF155/156	FET Op Amp	T	
LH2101A	Dual Op Amp	F	
LH2108A	Dual Op Amp	F	
LM101	High Perf. Op Amp	F	T
LM101A	High Perf. Op Amp	F	T
LM107	General Purpose Op Amp	F	F
LM108	Precision Op Amp	F	T
LM108A	Precision Op Amp	F	T
LM124	Quad Op Amp	F	
LM158	Dual Op Amp		T
MC1556	Op Amp	F	T
MC1558	Dual Op Amp	F	T
SE532	Dual Op Amp	—	T
SE535	Hi Slew Rate Op Amp	T	
SE538	Hi Slew Rate Op Amp	T	
μA709	Op Amp	F	T
μA709A	Op Amp	F	T
μA741	General Purpose Op Amp	F	T
μA747	Dual Op Amp	F	K
μA748	General Purpose Op Amp	F	T

DEVICE	DESCRIPTION	PACKAGE	
	PHASE LOCKED LOOPS		
SE567	Tone Decoder P11	F	T
	LINE RECEIVERS		
DM7820	Dual Differential Line Receiver	F	
DM7830	Dual Differential Line Receiver	F	
	TIMERS		
SE555	Timer	F	T
SE556	Dual Timer	F	
SE558/9	Quad Timer	F	
	VOLTAGE REGULATORS		
LM109	5 Volt Regulator	DA	
SE5554	Dual Track Reg	F	
78XX (7)	Positive Reg	DA	
79XX (7)	Negative Reg	DA	
79MXX (7)	Med Power Reg	DB	
μA723	Precision Voltage Regulator	F	L
	DRIVERS		
DS1611-1614	Peripheral Drivers		T
	D/A		
MC1508-8	8-Bit D/A	F	
SE5008	8-Bit D/A	F	
SE5009	8-Bit D/A	F	

PACKAGES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across VCC and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Alloy 42 or equivalent, solder dipped.
6. Body material: Plastic
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

9. Lead material
   a. Alloy 52—gold plated, or solder dipped.
   b. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
   c. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated.
   d. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
   e. ASTM alloy F-15 (KOVAR) or equivalent—tin plated.
10. Body Material
   a. 1010 Steel—nickel plated or tin plate over nickel.
   b. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated.
   c. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
   d. Ceramic with glass seal at leads.
   e. BeO ceramic with glass seal at leads.
   f. Ceramic with ASTM alloy F-15 or equivalent.
11. Lid Material
   a. 1010 steel, nickel plated, or tin-plate over nickel, weld seal.
   b. Nickel or tin plated nickel, weld seal.
   c. Ceramic, glass seal.
   d. ASTM alloy F-15 or equivalent, gold plated.
   e. BeO Ceramic with glass seal.
   f. Translucent $A1_2O_3$, glass seal.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	Θ_{ja}/Θ_{jc} (°C/W)	DESCRIPTION[1]	PAGE
Standard Dual-in-Line				
8	NE	162/65		3
14	NH	150/65	TO-116/MO-001	3
16	NJ	137/53	MO-001	3
18	NK	135/53		3
20	NL	135/53		3
22	NM	120/53		3
24	NN	116/53	MO-015	4
28	NQ	116/53	MO-015	4
40	NW[3]	110/50	MO-015	4
Power Dual-in-Line				
14	NHA[2]	95/33	Butterfly	3
16	NJA[2]	95/33	Butterfly	3
18	NKA[2,3]	90/26	Butterfly	3
20	NLA[2,3]	90/26	Butterfly	3
24	NNA[2]	60/23	Butterfly	4
28	NQA[2]	56/21	Butterfly	4
Power				
3	S	200/70	TO-92	5
3	U	75/3	TO-220	5
3 + GND	GB[3]	95/15	Single-in-Line (SIL)	5
4 + GND	GC[3]	95/15	Single-in-Line (SIL)	5
12 + GND	PH/PHA[3]	95/15	Batwing	5

12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb .010 inches.
15. Maximum glass climb or lid skew is .010 inches.
16. Typical four places.
17. Dimension also applies to seating plane.

HERMETIC PACKAGES

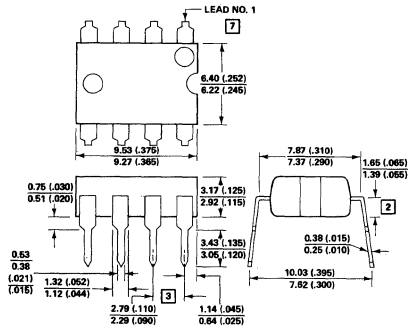
NO. OF LEADS	PACKAGE CODE	Θ_{ja}/Θ_{jc} (°C/W)	DESCRIPTION[1]	PAGE
Metal Headers				
2	DA	TBD	TO-3 Solid Header	6
3	DB	TBD	TO-39 Solid Header, Short Can	6
4	DC	TBD	TO-72 Solid Header	6
4	DE	TBD	TO-72 Glass Filled Header	6
8	T	150/25	TO-99 Header (.200 Dia.)	7
10	K	150/25	TO-100 Header, Short Can	7
10	L	150/25	TO-100 Header, Tall Can	7
Flat Packs				
10	WF	240/50	Flat Ceramic	8
14	WH	205/50	Flat Ceramic	8
16	WJ	200/50	Flat Ceramic	8
24	WN	155/40	Flat Ceramic	8
16	RJ/RJA	133/30	Flat Ceramic, BeO	8
18	RKA[3]	TBD	Flat Ceramic, BeO	—
24	RNA	TBD	Flat Ceramic, BeO	8
28	RQA	TBD	Flat Ceramic, BeO	9
40	RWA	TBD	Flat Ceramic, BeO	9
10	QF	230/55	Flat Ceramic	9
14	QH	185/45	Flat Ceramic	9
16	QJ	170/45	Flat Ceramic	9
24	QN	155/44	Flat Ceramic	9
10	QFA	230/55	Flat Ceramic Laminate	10
14	QHA	185/45	Flat Ceramic Laminate	10
16	QJA	170/45	Flat Ceramic Laminate	10
24	QNA	155/44	Flat Ceramic Laminate	10
Cerdip Family				
14	FH	110/30	Dual in-Line Ceramic	11
16	FJ	100/30	Dual-in-Line Ceramic	11
18	FK	93/27	Dual-in-Line Ceramic	11
22	FM	75/27	Dual-in-Line Ceramic	11
24	FN	60/26	Dual-in-Line Ceramic	11
Laminated Ceramic, Side Brazed Lead				
8	IEA	100/30	Dip Laminate	12
14	IHA	95/25	Dip Laminate	12
16	IJA	90/25	Dip Laminate	12
18	IKA	88/25	Dip Laminate	12
22	IMA	80/25	Dip Laminate	12
24	INC/IND	65/25	Dip Laminate	12
28	IQA	60/25	Dip Laminate	13
40	IWA	55/25	Dip Laminate	13
50	IZA	TBD	Dip Laminate	13

NOTES

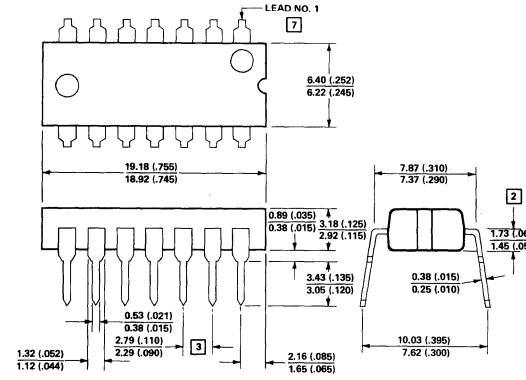
1. Dual-in-Line packages unless otherwise described
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads
3. Package not yet available, scheduled for 1977 release

PLASTIC: Standard and Power Dual-In-Line

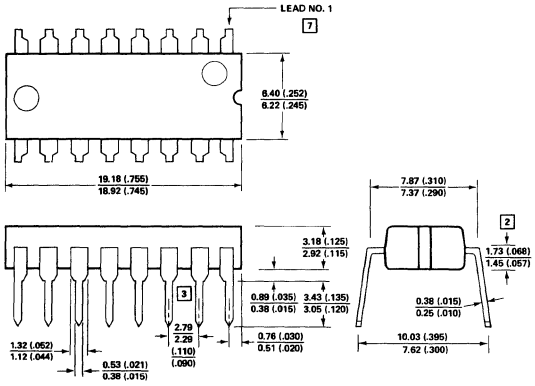
NE Package



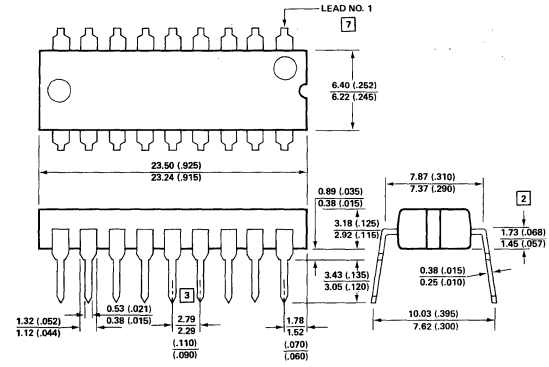
NH Package and NHA Package



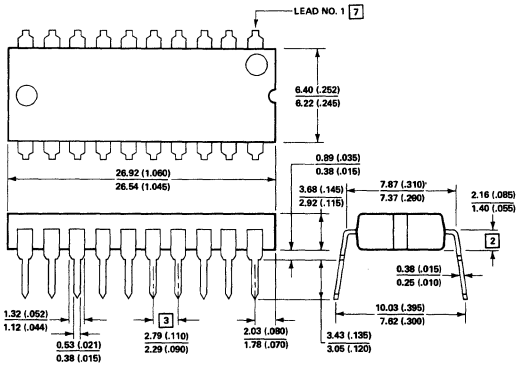
NJ Package and NJA Package



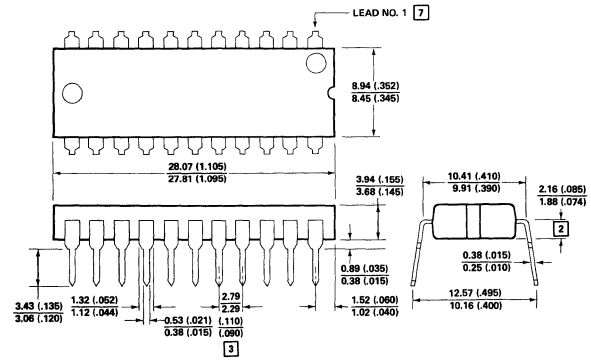
NK Package and NKA Package



NL Package and NLA Package

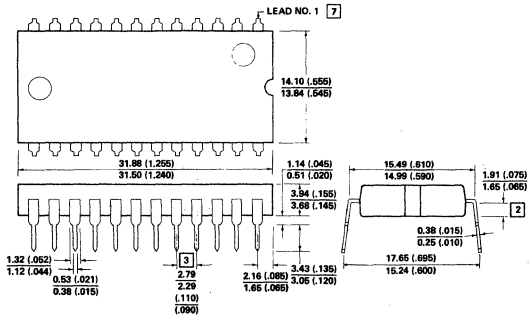


NM Package

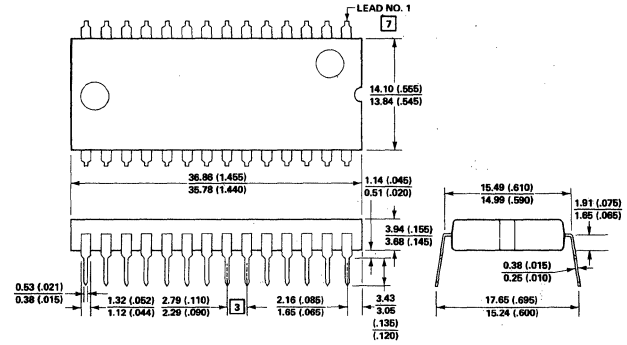


PLASTIC: Standard and Power Dual-In-Line (cont'd.)

NN Package and NNA Package



NQ Package and NQA Package

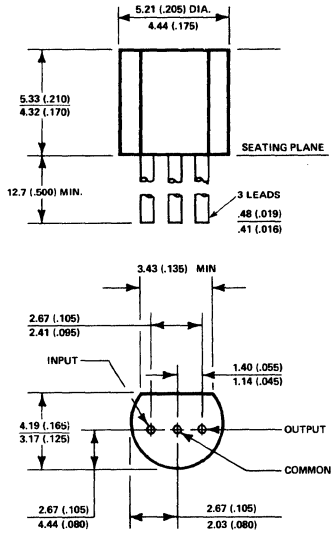


NW Package

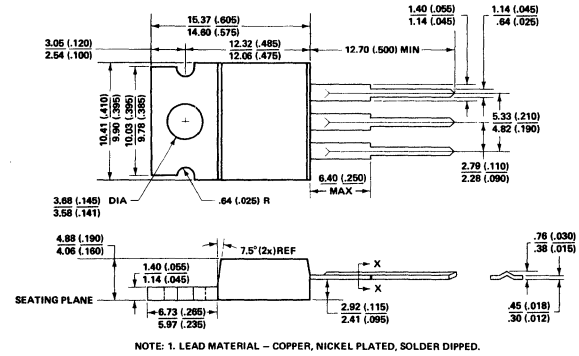
Package not yet available
Scheduled for 1977 release

PLASTIC: Power (Not Dual-In-Line)

S Package



U Package



NOTE: 1. LEAD MATERIAL – COPPER, NICKEL PLATED, SOLDER DIPPED.

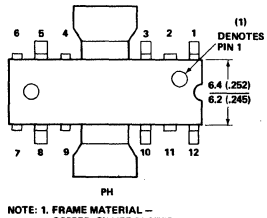
GB Package

Package not yet available
Scheduled for 1977 release

GC Package

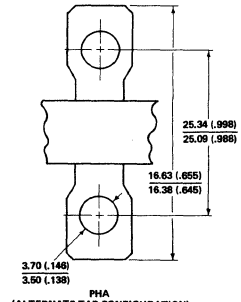
Package not yet available
Scheduled for 1977 release

PH/PHA Package

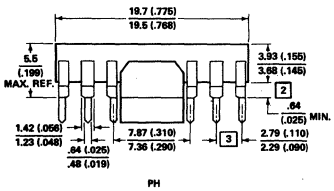


PH

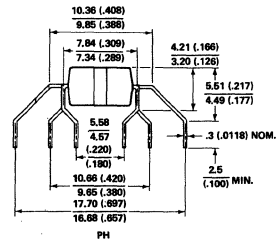
NOTE: 1. FRAME MATERIAL – COPPER, SILVER PLATED.



PHA
(ALTERNATE TAB CONFIGURATION)



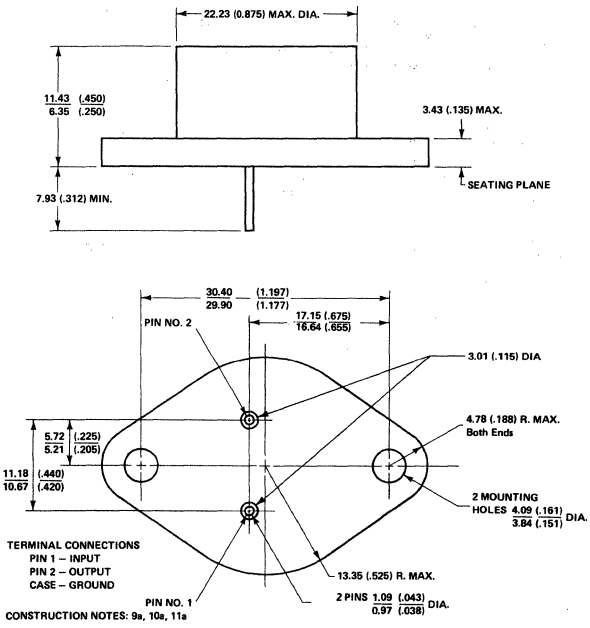
PH



PH

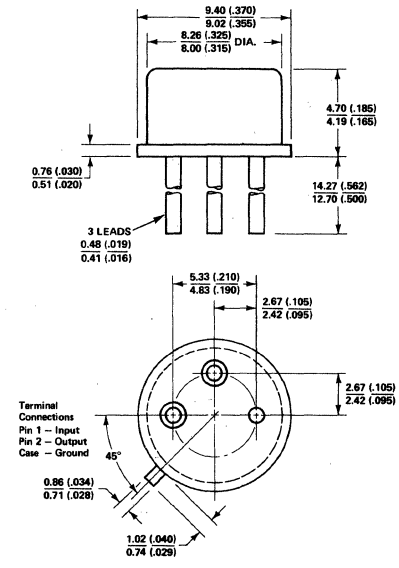
HERMETIC: Metal Headers

DA Package



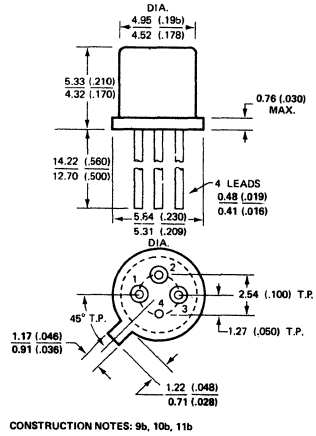
CONSTRUCTION NOTES: 9a, 10a, 11a

DB Package



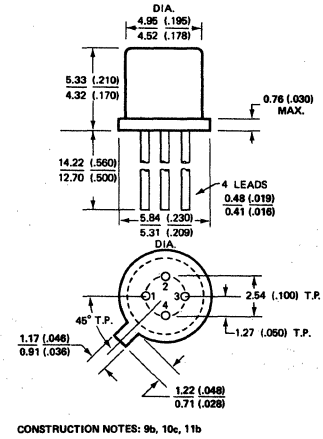
CONSTRUCTION NOTES: 9b, 10b, 11b

DC Package



CONSTRUCTION NOTES: 9b, 10b, 11b

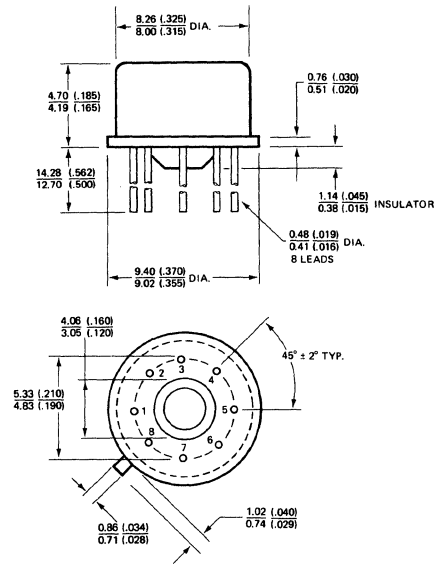
DE Package



CONSTRUCTION NOTES: 9b, 10c, 11b

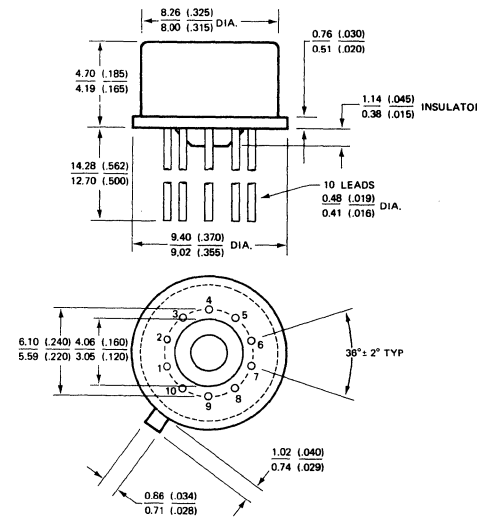
HERMETIC: Metal Headers (cont'd.)

T Package



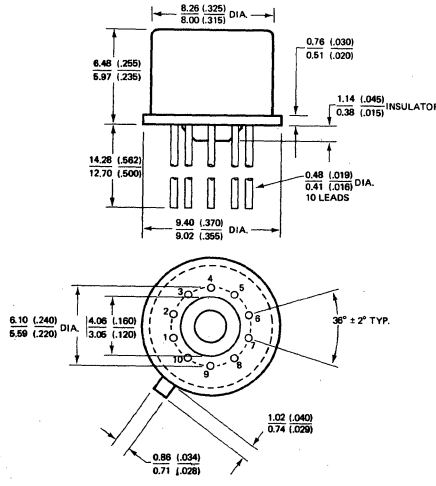
CONSTRUCTION NOTES: 9b, 10c, 11b

K Package



CONSTRUCTION NOTES: 9b, 10c, 11b

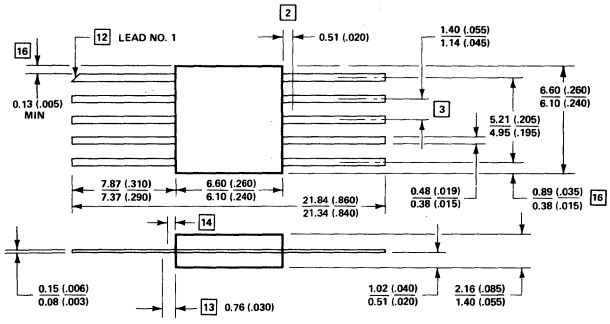
L Package



CONSTRUCTION NOTES: 9b, 10c, 11b

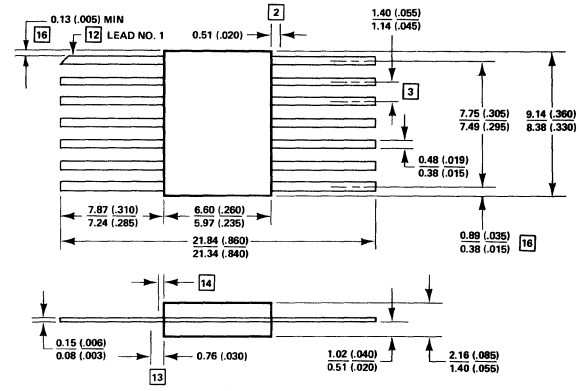
HERMETIC: Flat Packs

WF Package



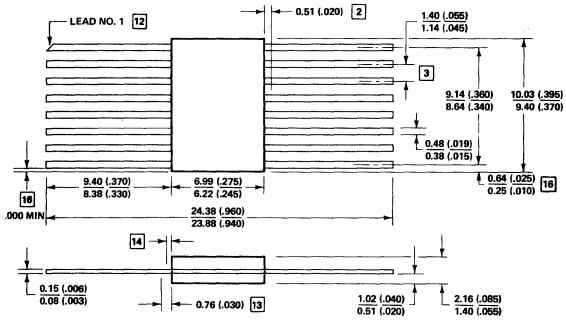
CONSTRUCTION NOTES: 9c, 10d, 11c

WH Package



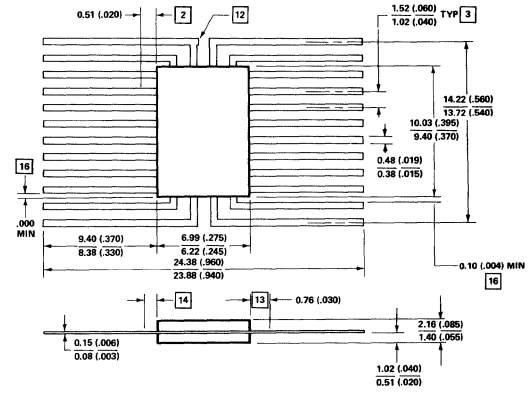
CONSTRUCTION NOTES: 9c, 10d, 11c

WJ Package



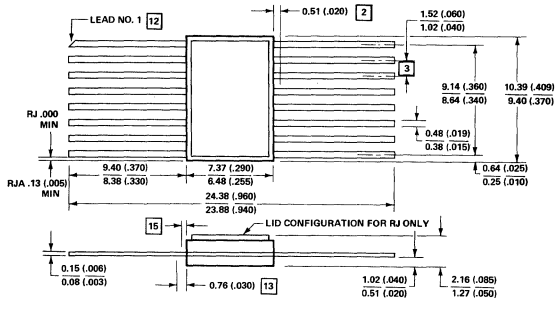
CONSTRUCTION NOTES: 9c, 10d, 11c

WN Package



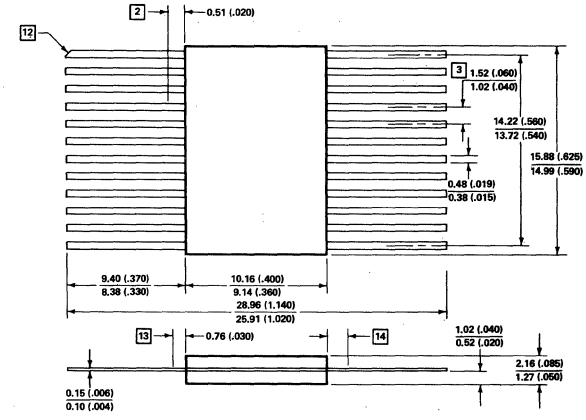
CONSTRUCTION NOTES: 9c, 10d, 11c

RJ and RJA Package



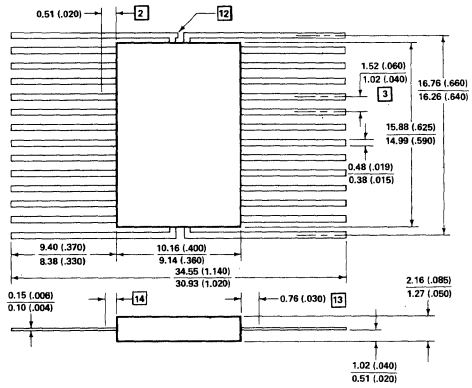
RJA CONSTRUCTION NOTES: 9c, 10e, 11e
RJ CONSTRUCTION NOTES: 9d, 10e, 11d

RNA Package



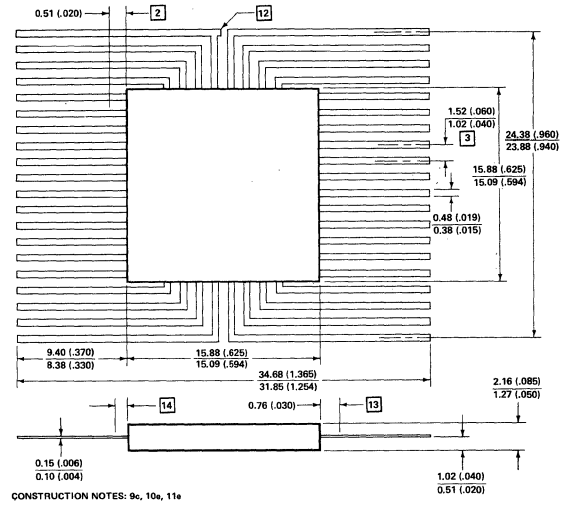
HERMETIC: Flat Packs (cont'd.)

RQA Package



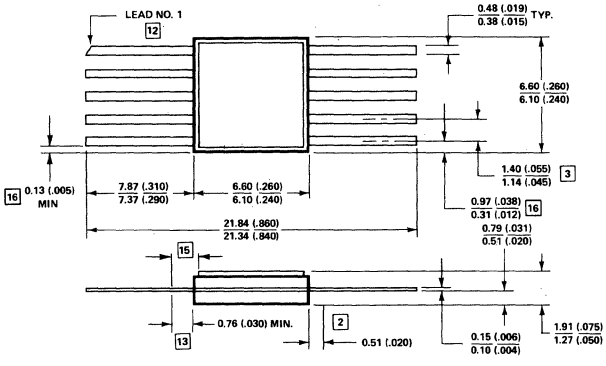
CONSTRUCTION NOTES: 9c, 10e, 11e

RWA Package



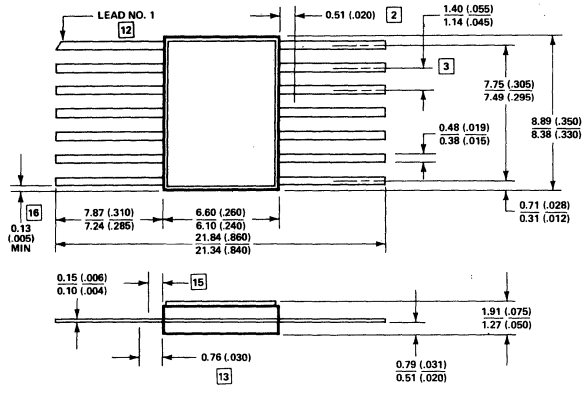
CONSTRUCTION NOTES: 9c, 10e, 11e

QF Package



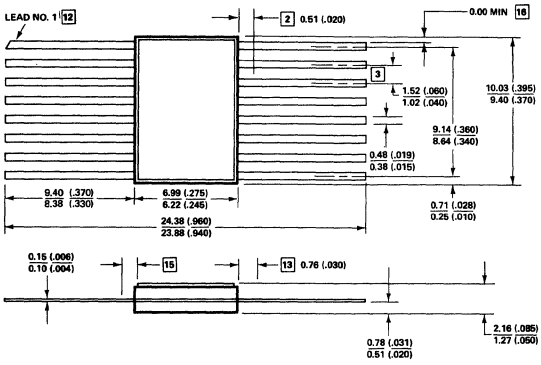
CONSTRUCTION NOTES: 9d, 10d, 11c

QH Package



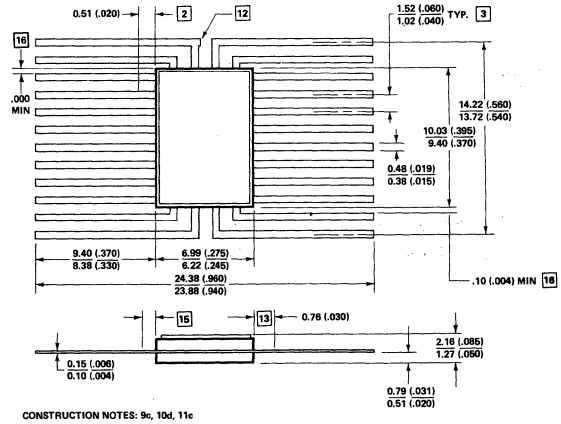
CONSTRUCTION NOTES: 9d, 10d, 11c

QJ Package



CONSTRUCTION NOTES: 9d, 10d, 11c

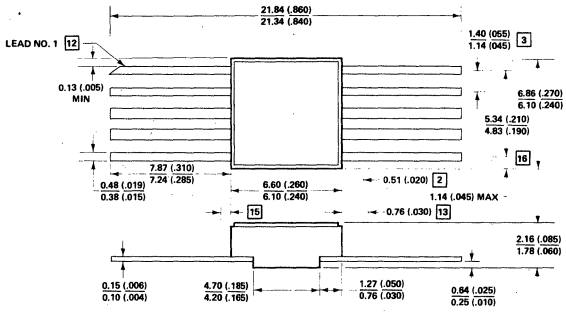
QN Package



CONSTRUCTION NOTES: 9c, 10d, 11c

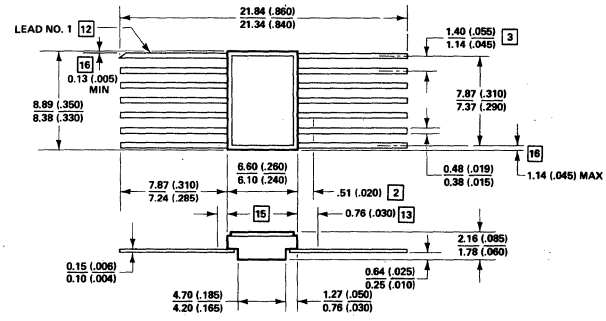
HERMETIC: Flat Packs (cont'd.)

QFA Package



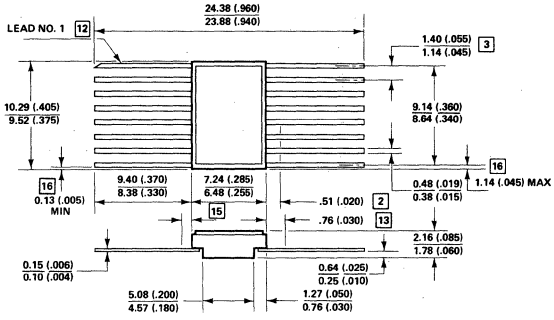
CONSTRUCTION NOTES: 9d, 10f, 11c

QHA Package



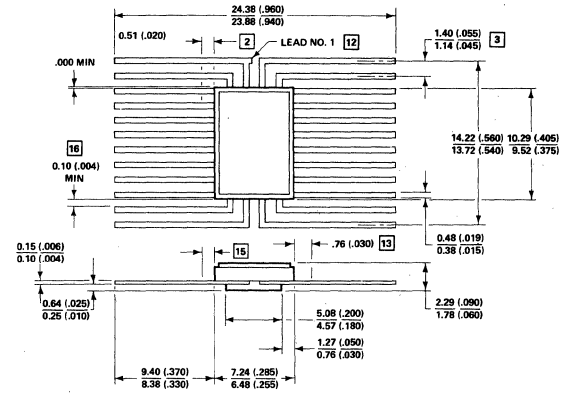
CONSTRUCTION NOTES: 9d, 10f, 11c

QJA Package



CONSTRUCTION NOTES: 9d, 10f, 11c

QNA Package



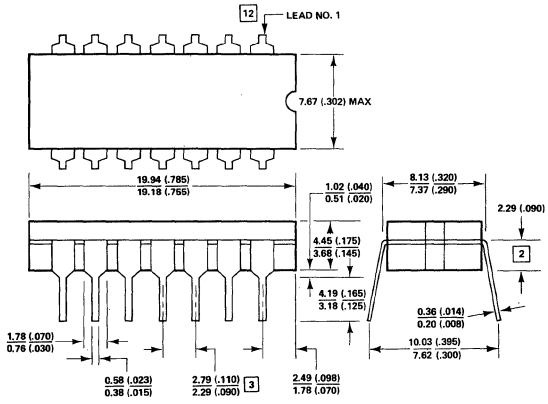
CONSTRUCTION NOTES: 9d, 10f, 11c

RKA Package

Package not yet available
Scheduled for 1977 release

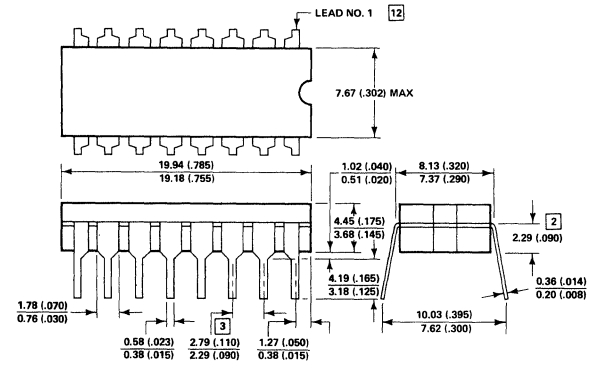
HERMETIC: Cerdip

FH Package



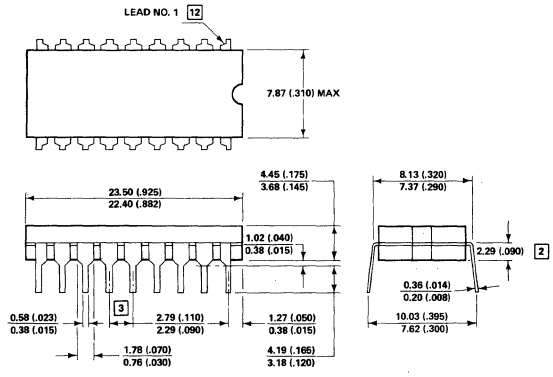
CONSTRUCTION NOTES: 9c, 10d, 11c

FJ Package



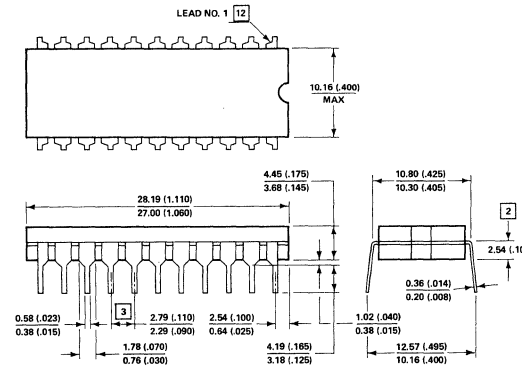
CONSTRUCTION NOTES: 9c, 10d, 11c

FK Package



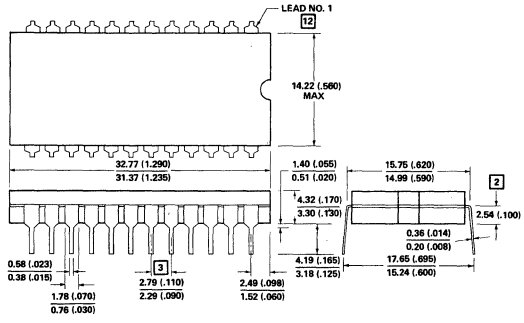
CONSTRUCTION NOTES: 9c, 10d, 11c

FM Package



CONSTRUCTION NOTES: 9c, 10d, 11c

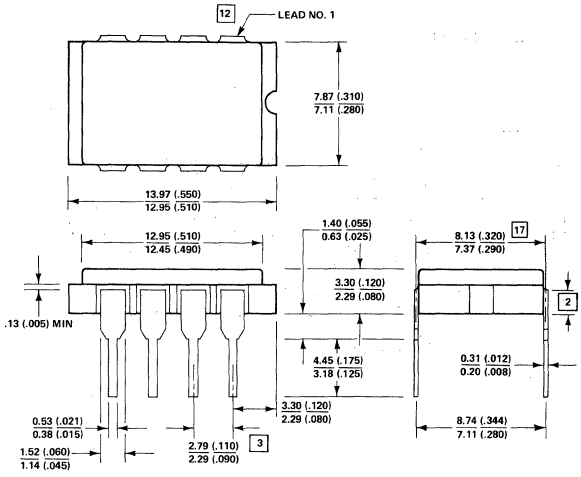
FN Package



CONSTRUCTION NOTES: 9c, 10d, 11c

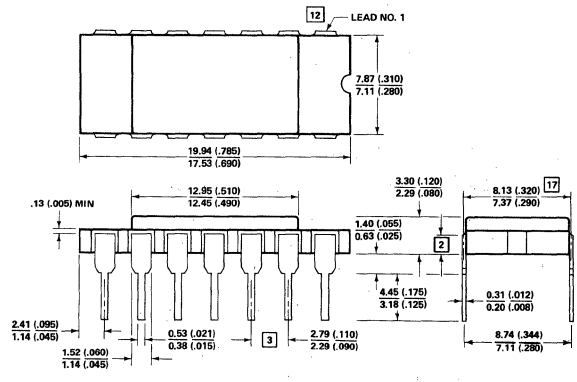
HERMETIC: Laminated Ceramic, Side Brazed Lead

IEA Package



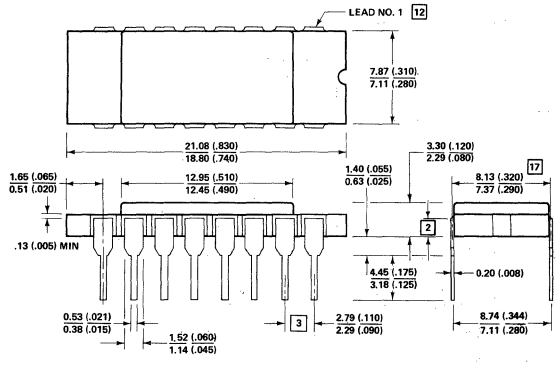
CONSTRUCTION NOTES: 9e, 10f, 11c

IHA Package



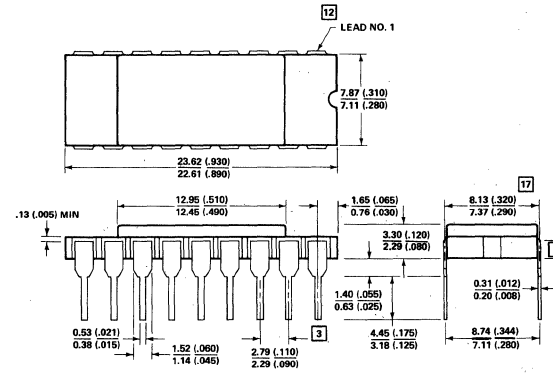
CONSTRUCTION NOTES: 9e, 10f, 11c

IJA Package



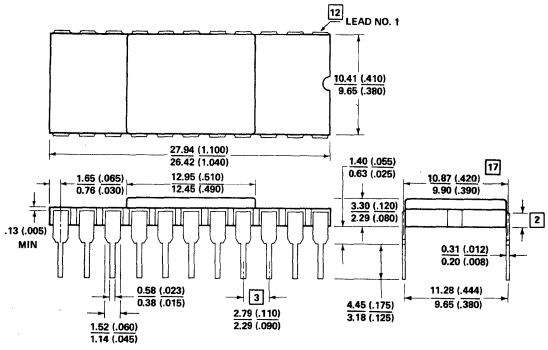
CONSTRUCTION NOTES: 9e, 10f, 11c

IKA Package



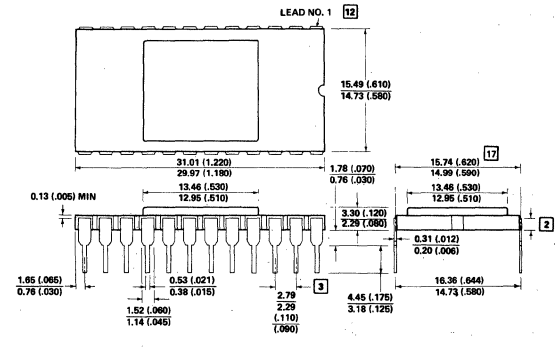
CONSTRUCTION NOTES: 9e, 10f, 11c

IMA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

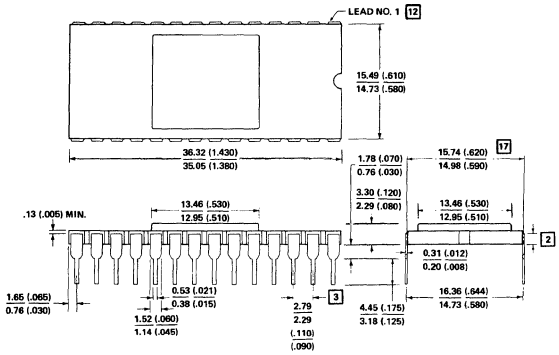
INC Package and IND Package



CONSTRUCTION NOTES: 9e, 10f, 11c, 11f (IND)

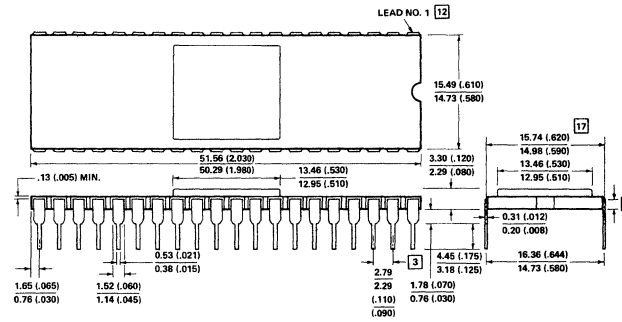
HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IQA Package



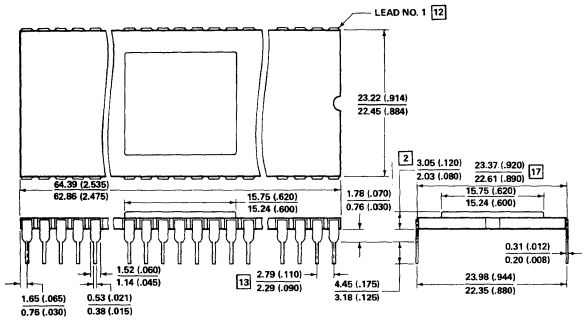
CONSTRUCTION NOTES: 9e, 10f, 11c

IWA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

IZA Package



CONSTRUCTION NOTES: 9e, 10f, 11c

SALES OFFICES

SIGNETICS

HEADQUARTERS

811 East Arques Avenue
Sunnyvale, California 94086
Phone: (408) 739-7700

ALABAMA

Huntsville
Phone: (205) 534-5671

ARIZONA

Phoenix
Phone: (602) 971-2517

CALIFORNIA

Inglewood
Phone: (213) 670-1101
Irvine
Phone: (714) 833-8980
(213) 924-1668
San Diego
Phone: (714) 560-0242
Sunnyvale
Phone: (408) 736-7565

COLORADO

Parker
Phone: (303) 841-3274

FLORIDA

Pompano Beach
Phone: (305) 782-8225

ILLINOIS

Rolling Meadows
Phone: (312) 259-8300

INDIANA

Noblesville
Phone (317) 773-6770

KANSAS

Wichita
Phone: (316) 683-5652

MARYLAND

Columbia
Phone: (301) 730-8100

MASSACHUSETTS

Woburn
Phone: (617) 933-8450

MINNESOTA

Edina
Phone: (612) 835-7455

NEW JERSEY

Cherry Hill
Phone: (609) 665-5071
Piscataway
Phone: (201) 981-0123

NEW YORK

Wappingers Falls
Phone: (914) 297-4074
Woodbury, L.I.
Phone: (516) 364-9100

OHIO

Worthington
Phone: (614) 888-7143

TEXAS

Dallas
Phone: (214) 661-1296

REPRESENTATIVES

CALIFORNIA

San Diego
Mesa Engineering
Phone: (714) 278-8021

Sherman Oaks
Astralonics
Phone: (213) 990-5903

CANADA

Calgary, Alberta
Philips Electronics Industries Ltd.
Phone: (403) 243-2710

Montreal, Quebec
Philips Electronics Industries Ltd.
Phone: (514) 342-9180

Ottawa, Ontario
Phillips Electronics Industries Ltd.
Phone: (613) 237-3131

Scarborough, Ontario
Philips Electronics Industries Ltd.
Phone: (416) 292-5161

Vancouver, B.C.
Philips Electronics Industries Ltd.
Phone: (604) 435-4411

COLORADO

Denver
Barnhill Five, Inc.
Phone: (303) 426-0222

CONNECTICUT

Newtown
Kanan Associates
Phone: (203) 426-8157

FLORIDA

Altamonte Springs
Semtronic Associates
Phone: (305) 831-8233

Largo
Semtronic Associates
Phone: (813) 586-1404

ILLINOIS

Chicago
L-Tec Inc.
Phone: (312) 286-1500

INDIANA

Indianapolis
Enco Marketing
Phone: (317) 546-5511

MARYLAND

Glen Burni
Microcomp, Inc.
Phone: (301) 761-4600

MASSACHUSETTS

Reading
Kanan Associates
Phone: (617) 944-8484

MICHIGAN

Bloomfield Hills
Enco Marketing
Phone: (313) 642-0203

MINNESOTA

Edina
Mel Foster Tech. Assoc.
Phone: (612) 835-2254

NEW JERSEY

Haddonfield
Thomas Assoc. Inc.
Phone: (609) 854-3011

NEW MEXICO

Albuquerque
The Staley Company, Inc.
Phone: (505) 821-4310/11

NEW YORK

Ithaca
Bob Dean, Inc.
Phone: (607) 272-2187

NORTH CAROLINA

Cary
Montgomery Marketing
Phone: (919) 467-6319

OHIO

Centerville
Norm Case Associates
Phone: (513) 433-0966

Fairview Park
Norm Case Associates
Phone: (216) 333-4120

OREGON

Portland
Western Technical Sales
Phone: (503) 297-1711

TEXAS

Austin
Cunningham Co.
Phone: (512) 459-8947

Dallas
Cunningham Co.
Phone: (214) 233-4303

Houston
Cunningham Company
Phone: (713) 461-4197

UTAH

West Bountiful
Barnhill Five, Inc.
Phone: (801) 292-8991

WASHINGTON

Bellevue
Western Technical Sales
Phone: (206) 641-3900

WISCONSIN

Greenfield
L-Tec, Inc.
Phone: (414) 545-8900

DISTRIBUTORS

ALABAMA

Huntsville
Hamilton/Avnet Electronics
Phone: (205) 533-1170

ARIZONA

Phoenix
Hamilton/Avnet Electronics
Phone: (602) 275-7851

Liberty Electronics
Phone: (602) 257-1272

CALIFORNIA

Costa Mesa
Avnet Electronics
Phone: (714) 754-6111

Schweber Electronics
Phone: (213) 537-4320

Culver City
Hamilton Electro Sales
Phone: (213) 558-2173

El Segundo
Liberty Electronics
Phone: (213) 322-8100

Mountain View
Elmar Electronics
Phone: (415) 961-3611

Hamilton/Avnet Electronics
Phone: (415) 961-7000

San Diego
Hamilton/Avnet Electronics
Phone: (714) 279-2421

Liberty Electronics
Phone: (714) 565-9171

Sunnyvale
Intermark Electronics
Phone: (408) 738-1111

CANADA

Downsview, Ontario
Cesco Electronics
Phone: (416) 661-0220

Mississauga, Ontario
Hamilton/Avnet Electronics
Phone: (416) 677-7432

Montreal, Quebec
Cesco Electronics
Phone: (514) 735-5511

Zentronics Ltd.
Phone: (514) 735-5361

Ottawa, Ontario
Cesco Electronics
Phone: (613) 729-5118

Hamilton/Avnet Electronics
Phone: (613) 226-1700

Zentronics Ltd.
Phone: (613) 238-6411

Toronto, Ontario
Zentronics Ltd.
Phone: (416) 789-5111

Vancouver, B.C.
Bowtek Electronics Co., Ltd.
Phone: (604) 736-1141

Ville St. Laurent, Quebec
Hamilton/Avnet Electronics
Phone: (514) 331-6443

COLORADO

Commerce City
Elmar Electronics
Phone: (303) 287-9611

Denver
Hamilton/Avnet Electronics
Phone: (303) 534-1212

Lakewood Acacia Sales
Phone: (303) 232-2882

CONNECTICUT

Danbury
Schweber Electronics
Phone: (203) 792-3500

Georgetown
Hamilton/Avnet Electronics
Phone: (203) 762-0361

Hamden
Arrow Electronics
Phone: (203) 248-3801

FLORIDA

Ft. Lauderdale
Arrow Electronics
Phone: (305) 776-7790

Hamilton/Avnet Electronics
Phone: (305) 971-2900

Hollywood
Schweber Electronics
Phone: (305) 922-4506

Orlando
Hammond Electronics
Phone: (305) 241-6601

GEORGIA

Atlanta
Schweber Electronics
Phone: (404) 449-9170

Norcross
Hamilton/Avnet Electronics
Phone: (404) 448-0800

ILLINOIS

Elk Grove
Schweber Electronics
Phone: (312) 593-2740

Elmhurst
Semiconductor Specialists
Phone: (312) 279-1000

Schiller Park
Hamilton/Avnet Electronics
Phone: (312) 671-6082

INDIANA

Indianapolis
Semiconductor Specialists
Phone: (317) 243-8271

KANSAS

Lenexa
Hamilton/Avnet Electronics
Phone: (913) 888-8900

MARYLAND

Baltimore
Arrow Electronics
Phone: (301) 247-5200

Gaithersburg
Pioneer Washington Electronics
Phone: (301) 948-0710

Hanover
Hamilton/Avnet Electronics
Phone: (301) 796-5000

Rockville
Schweber Electronics
Phone: (301) 881-2970

MASSACHUSETTS

Waltham
Schweber Electronics
Phone: (617) 890-8484

Woburn
Arrow Electronics
Phone: (617) 933-8130

Hamilton/Avnet Electronics
Phone: (617) 933-8000

MICHIGAN

Livonia
Hamilton/Avnet Electronics
Phone: (313) 522-4700

Troy
Schweber Electronics
Phone: (313) 583-9242

MINNESOTA

Eden Prairie
Schweber Electronics
Phone: (612) 941-5280

Edina
Hamilton/Avnet Electronics
Phone: (612) 941-3801

Minneapolis
Semiconductor Specialists
Phone: (612) 854-8841

MISSOURI

Hazelwood
Hamilton/Avnet Electronics
Phone: (314) 731-1144

NEW MEXICO

Albuquerque
Hamilton/Avnet Electronics
Phone: (505) 765-1500

NEW YORK

Buffalo
Summit Distributors
Phone: (716) 884-3450

East Syracuse
Hamilton/Avnet Electronics
Phone: (315) 437-2642

Farmingdale, L.I.
Arrow Electronics
Phone: (516) 694-6800

Rochester
Hamilton/Avnet Electronics
Phone: (716) 442-7820

Schweber Electronics
Phone: (716) 461-4000

Westbury, L.I.
Hamilton/Avnet Electronics
Phone: (516) 333-5800

Schweber Electronics
Phone: (516) 334-7474

NORTHERN NEW JERSEY

Cedar Grove
Hamilton/Avnet Electronics
Phone: (201) 239-0800

Saddlebrook
Arrow Electronics
Phone: (201) 797-5800

SOUTHERN NEW JERSEY AND PENNSYLVANIA

Cherry Hill, N.J.
Milgray-Delaware Valley
Phone: (609) 424-1300

Moorestown, N.J.
Arrow/Angus Electronics
Phone: (609) 235-1900

Mt. Laurel, N.J.
Hamilton/Avnet Electronics
Phone: (609) 234-2133

CENTRAL NEW JERSEY AND PENNSYLVANIA

Somerset, N.J.
Schweber Electronics
Phone: (201) 469-6008

Horsham, PA
Schweber Electronics
Phone: (215) 441-0600

NORTH CAROLINA

Greensboro
Hammond Electronics
Phone: (919) 275-6391

OHIO

Beechwood
Schweber Electronics
Phone: (216) 464-2970

Cleveland
Arrow Electronics
Phone: (216) 464-2000

Hamilton/Avnet Electronics
Phone: (216) 461-1400

Pioneer Standard Electronics
Phone: (216) 587-3600

Dayton
Arrow Electronics
Phone: (513) 253-9176

Hamilton/Avnet Electronics
Phone: (513) 433-0610

Pioneer Standard Electronics
Phone: (513) 236-9900

TEXAS

Dallas
Component Specialties
Phone: (214) 357-4576

Hamilton/Avnet Electronics
Phone: (214) 661-8661

Schweber Electronics
Phone: (214) 661-5010

Houston
Component Specialties
Phone: (713) 771-7237

Hamilton/Avnet Electronics
Phone: (713) 780-1771

Schweber Electronics
Phone: (713) 784-3600

UTAH

Salt Lake City
Alta Electronics
Phone: (801) 486-7227

Hamilton/Avnet Electronics
Phone: (801) 972-2800

WASHINGTON

Bellevue
Hamilton/Avnet Electronics
Phone: (206) 746-8750

Seattle
Liberty Electronics
Phone: (206) 763-8200

Intermark Electronics
Phone: (206) 767-3160

WISCONSIN

New Berlin
Hamilton/Avnet Electronics
Phone: (414) 784-4510

FOR SIGNETICS PRODUCTS WORLDWIDE:

ARGENTINA

Fapesa I.y.C.
Buenos-Aires
Phone: 652-7438/7478

AUSTRIA

Osterreichische Philips
Wien
Phone: 93 26 11

AUSTRALIA

Philips Industries-ELCOMA
Lane-Cove, N.S.W.
Phone: 421261

BELGIUM

M.B.L.E.
Brussels
Phone: 523 00 00

BRAZIL

Ibrape, S.A.
Sao Paulo
Phone: 284-4511

CANADA

Philips Electron Devices
Toronto
Phone: 425-5161

CHILE

Philips Chilena S.A.
Santiago
Phone: 39-4001

DENMARK

Miniwatt A/S
Kobenhavn
Phone: (01) 69 16 22

FINLAND

Oy Philips Ab
Helsinki
Phone: 1 72 71

FRANCE

R.T.C.
Paris
Phone: 355-44-99

GERMANY

Valvo
Hamburg
Phone: (040) 3296-1

HONG KONG

Philips Hong Kong, Ltd.
Kwuntong
Phone: 3-427232

INDIA

Semiconductors, Ltd.
(REPRESENTATIVE ONLY)
Bombay
Phone: 293-667

INDONESIA

P.T. Philips-Ralin Electronics
Jakarta
Phone: 581058

IRAN

Berkeh Company, Ltd.
Tehran
Phone: 831564

ISRAEL

Rapac Electronics, Ltd.
Tel Aviv
Phone: 477115-6-7

ITALY

Philips S.p.A.
Milano
Phone: 2-6994

JAPAN

Signetics Japan, Ltd.
Tokyo
Phone: (03) 230-1521

KOREA

Kumho & Co.
Seoul
Phone: (76) 5271-5

MEXICO

Electronica S.A. de C.V.
Mexico D.F.
Phone: 533-1180

NETHERLANDS

Philips Nederland B.V.
Eindhoven
Phone: (040) 79 33 33

NEW ZEALAND

E.D.A.C., Ltd.
Wellington
Phone: 873 159

NORWAY

Electronica A.S.
Oslo
Phone: (02) 15 05 90

PHILIPPINES

Philips Industrial Dev., Inc.
Makata-Rizal
Phone: 868951-9

SINGAPORE/MALAYSIA

Philips Singapore Pte., Ltd.
Toa Payoh
Phone: 538811

SOUTH AFRICA

E.D.A.C. (PTY), Ltd.
Johannesburg
Phone: 24-6701-3

SPAIN

Copresa S.A.
Barcelona
Phone: 329 63 12

SWEDEN

Elcoma A.B.
Stockholm
Phone: 08/67 97 80

SWITZERLAND

Philips A.G.
Zurich
Phone: 01/44 22 11

TAIWAN

Philips Taiwan, Ltd.
Taipei
Phone: (02) 551-3101-5

THAILAND/LAOS

Saeng Thong Radio, Ltd.
Bangkok
Phone: 527195, 519763

UNITED KINGDOM

Mullard, Ltd.
London
Phone: 01-580 6633

UNITED STATES

Signetics International Corp.
Sunnyvale, California
Phone: (408) 739-7700

VENEZUELA, PANAMA, ARUBA, TRINIDAD

Instrulab C.A.
Caracas
Phone: 614138

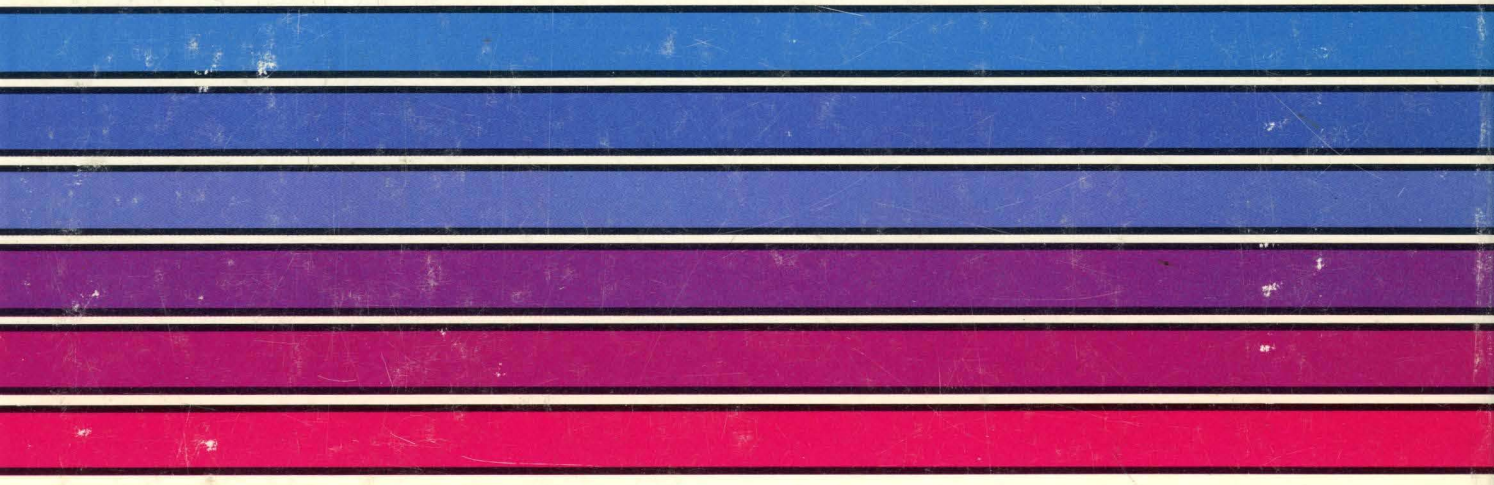
INDEX

BIPOLAR MEMORY

signetics

a subsidiary of **U.S. Philips Corporation**

Signetics Corporation
P.O. Box 9052
811 East Arques Avenue
Sunnyvale, California 94086
Telephone 408/739-7700



Printed in USA Jun. 1977