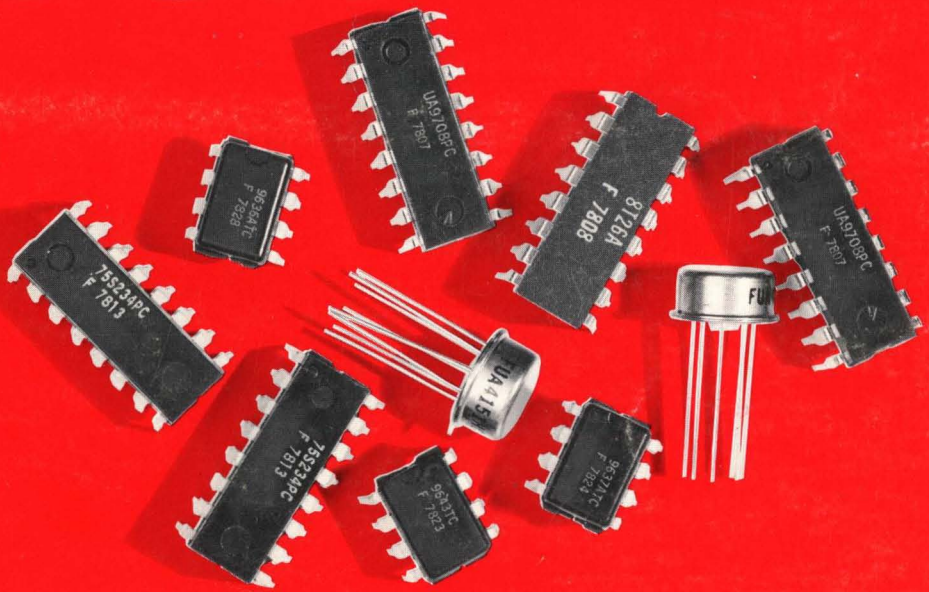
LINEAR INTERFACE DATA BOOK



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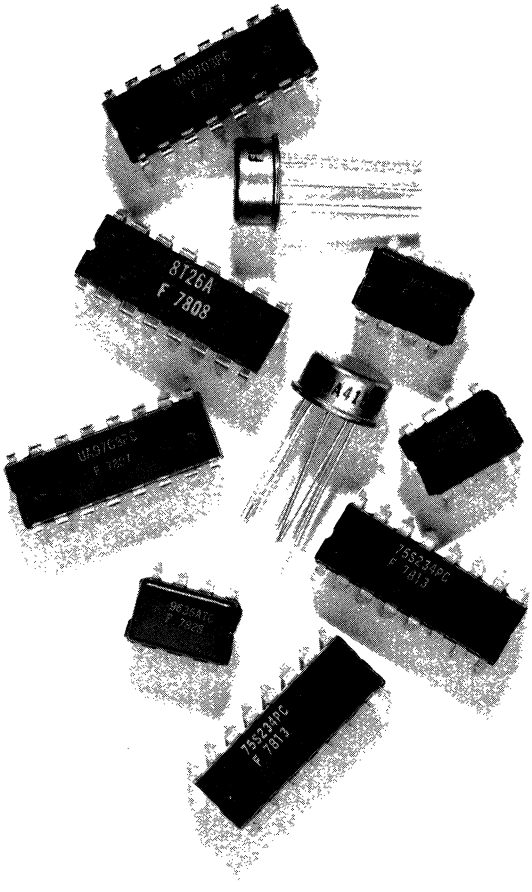
LINEAR INTERFACE DATA BOOK



FAIRCHILD

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INTRODUCTION

The increase in complexity and diversity of Linear Integrated Circuits over the last few years has necessitated a change in the format of the Fairchild Linear Data Books. In this data book, Fairchild is pleased to present important technical information on one of the industries broadest and most advanced family of Linear Interface, Comparator and Data Conversion circuits. Other Fairchild Linear data books will cover Operational Amplifiers, Consumer and Regulator devices.

Fairchild continues to be a pioneer in Linear Interface and Data Conversion products. Today Fairchild's state-of-the-art technology is bringing forth devices like the 9643; MOS/CCD driver, 75S20 series of Schottky core memory sense amplifiers, 9634/6/7/8 series of RS422/423 compatible line circuits, μA9708; micro-processor based 8-bit A/D subsystem, and the CMOS processed μA9706; micro-processor compatible 8 channel, 6-bit D/A converter.

You'll find complete specifications on Fairchild's MOS/CCD memory interface, data transmission, peripheral driver, memory sense amplifier, display interface, data conversion, comparator and special functions. Also included is advanced information on some of Fairchild's Interface circuits to be introduced shortly.

To expedite the designer's search for the right devices to meet various system requirements, several helpful aids are provided — selection guides by function, an LIC cross reference identifying competitive devices with their Fairchild direct replacements or nearest equivalents and the numerical indexes will let you locate specific type numbers quickly. For the Hi Rel customer, Fairchild's Hi Rel processing and Matrix VI are given in a separate section.

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ALPHA NUMERICAL INDEX OF INTERFACE DEVICES AND SELECTION GUIDES

ALPHA-NUMERICAL INDEX

ALPHA-NUMERICAL INDEX (Cont.)

ALPHA-NUMERICAL INDEX (Cont.)

ALPHA-NUMERICAL INDEX (Cont.)

VOLTAGE COMPARATOR SELECTION GUIDE

Device No.	Description	Input Bias Current μA (Max) 25°C	Input Offset Current (Max) 25°C	Input Offset Voltage mV - (Max) 25°C	Voltage Gain (Typ)	Supply Voltage V (Typ)	Response Time ns (Typ)	DTL/TTL Fanout	Temperature Range	Package(s)
μAF111	Fet-Input Voltage Comparator	0 05	0 000025	4.0	200K	+36	200	2	M	5S, 6A
μAF311	Fet-Input Voltage Comparator	0 15	0 000075	10	200K	+36	200	2	C	5S, 6A
μA111	Voltage Comparator Strobed Inputs, Single Supply, Low I_B	0 1	0 04	0.7	200K	±15	200	5	M	5S
μA311	Voltage Comparator Strobed Inputs, Single Supply, Low I_B	0.25	0 06	2.0	200K	±15	200	5	C	5S
μA139	Quad Comparator Single Supply, CMRR incl. gnd	0 1	0 025	5.0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	M	6A
μA139A	Quad Comparator Single Supply, CMRR incl. gnd	0 1	0 025	2.0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	M	6A
μA239	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	5 0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	A	6A, 9A
μA239A	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	2 0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	A	6A, 9A
μA339	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	5.0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	C	6A, 9A
μA339A	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	2.0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	C	6A, 9A
μA710/C	High Speed Differential Voltage Comparator	20/25	3 0/5 0	2 0/5.0	1 75K	+12, -6	40	1	M, C	5S, 3F, 6A, 9A
μA711/C	Dual High Speed Differential Comparator	75 100	10/15	3 5/5 0	1 5K	+12, -6	40	1	M, C	3F, 5F, 6A, 9A
μA734	Precision Comparator Low Drift -3.5 μV/°C	0 15	0 025/0 05	5 0/3 0	25K	±5 to ±15	200	2	M, C	5N, 6A
μA760	High Speed Differential Comparator	60	7 5	6 0	5K	±4.5 to ±6.5	25	2	M, C	5S, 6A
μA2901	Quad Comparator Single Supply, CMRR incl. gnd	0 25	0 05	7 0	200K	±1 to μ18 or from 2 to 36 and gnd	1300	1	A	6A, 9A
μA3302	Quad Comparator Single Supply, CMRR incl. gnd	0 5	0 1	20 0	200K	±1 to ±18 or from 2 to 36 and gnd	1300	1	C	6A, 9A

DATA ACQUISITION PRODUCTS SELECTION GUIDE

Device Number	Function	Operating Temp. Range (°C)	Maximum Non-Linearity (% FS)	Supply Voltage (V)	Package(s)
μA0801A (DAC-08A)	8 bit high speed multiplying D/A converter	-55/+125	±0.1	±15	6B
μA0801 (DAC-08)		-55/+125	±0.19	±15	6B
μA0801H (DAC-08H)		0/+70	±0.1	±15	6B, 9B
μA0801E (DAC-08E)		0/+70	±0.19	±15	6B, 9B
μA0801C (DAC-08C)		0/+70	±0.39	±15	6B, 9B
μA0802 (MC1508-8)	8 bit multiplying D/A converter	-55/+125	±0.19	+5 and -5 to -15	6B
μA0802A (MC1408-8)		0/+70	±0.19		6B, 9B
μA0802B (MC1408-7)		0/+70	±0.39		6B, 9B
μA0802C (MC1408-6)		0/+70	±0.78		6B, 9B
μA9708	6 channel, 8 bit μP compatible A/D converter	-55/+125 0/+70	±0.2	+4.75 to +15	7B 7B, 9B
μA9706	8 channel, 12 bit μP compatible D/A converter	0/+70	±0.01	+5	6A, 9A
μA9706A	7 channel, 12 bit μP compatible D/A converter	0/+70	±0.01	+5	7B, 9B
μA4151	Voltage to frequency converter	0/+70		+8 to +15	5S, 6T, 9T
μA7151	Voltage to frequency converter with op amp	0/+70	±0.5	+8 to +15	6A, 9A
μAF198	Sample and hold Amplifier	-55/+125		±5 to ±18	5S
μAF398	Sample and hold Amplifier	0/+70		±5 to ±18	5S
9650	4-bit current source A/D or D/A	0/+70	±0.2 to ±0.01	+4.5 and -14 or +5.5 and -16	6B

LINE DRIVER SELECTION GUIDE

Description	Output Current Capability (mA)	Propagation Delay Time Typical (ns)	S = Single Ended D = Differential	Party Line Operation	Strobe	Power Supplies (V)	Device Type For Temperature Range		Package Type	Drivers Per Package	Companion Receivers	Additional Features
							55°C to 125°C	0°C to 70°C				
General Purpose Drivers	300	20	S, D	Yes	Yes	5	55450B	75450B	6A 6A, 9A	2	9615 75122/ μA8T14	And Logic Function
	300	20	S	Yes	Yes	5	55451B	75451B	6T 6T, 9T	2		
	100	22	S	Yes	Yes	5	55121/μA8T13	75121/μA8T13	6B 6B, 9B	2	75122/ μA8T14	
	40	12	S, D	No	No	5	9612A	9612E	6T, 5B 6T, 9T, 5B	2	9613	Complimentary Outputs
	40	15	S, D	Yes	Yes	5	9614DM	9614	6B 6B, 9B	2	9615	3 Input AND/ NAND Function
360/370 I/O Interface	100	20	S	Yes	Yes	5		75123/ μA8T23	6B, 9B	2	75124/ μA8T24	
Drivers Meeting EIA Standards	50	10	D	Yes	Yes	5	9634RM	9634	6B 6B, 9B	2	9637A	3-State Output RS-422
	10	60	S	No	Yes	±12		75150	6A, 9A, 6T, 9T	2	75154 9627,9617	RS-232C/ MIL-STD-188C
	10	220	S	No	Yes	±12		μA1488	6A, 9A	4	μA1489 μA1489A	RS-232C
	30	320	S	No	No	±12	9616DM	9616C, E	6A 6A, 9A	3	μA1489/A 9617, 9627	RS-232C/ MIL-STD-188C
	40	10	D	No	No	5	9638RM	9638	6T 6T, 9T	2	9637A	RS-422, High Speed
	17	*	S	No	No	±12	9636ARM	9636A	6T 6T, 9T	2	9637A	RS-423, Slew Rate* Programmable
Current Mode Drivers	18	9	D	Yes	Yes	±5		75112	6A, 9A	2	75107A/B	Glitchless Current Outputs
	6.5	9	D	Yes	Yes	±5	55110A	75110A	6A 6A, 9A	2	75108A/B	

*9636A output slew rates are jointly controlled by a single external resistor.

LINE RECEIVERS SELECTION GUIDE

Description	S = Single Ended D = Differential	Type Of Output*	Propagation Delay Time Typical (ns)	Party Line Operation	Strobe	Power Supplies (V)	Device Type For Temperature Range -55°C to 125°C	Device Type For Temperature Range 0°C to 70°C	Package Type	Receivers Per Package	Companion Drivers	Additional Features
General Purpose Receivers	D	T	17	Yes	Yes	±5		75207*	6A, 9A	2	75110A, 55110A	B versions have input protection diodes for power off condition
	D	O	19	Yes	Yes			75208*	6A, 9A	2		
	D	T	17	Yes	Yes		55107A	75107A	6A, 3I 6A, 9A	2		
							55107B	75107B	6A, 3I 6A, 9A	2	75110A, 75112	
							55108A	75108A	6A, 3I 6A, 9A	2		
	D	O	19	Yes	Yes		55108B	75108B	6A, 3I 6A, 9A	2		
	S	T	30	Yes	Yes	5	55122/μA8T14	75122/ μA8T14	6B 6B, 9B	3	75121/ μA8T13	Hysteresis for improved noise immunity
	D	O or T	20	Yes	Yes	5	9615DM, FM	9615	6B, 4L 6B, 9B	2	9614	±500 mV input sensitivity, ±15 CMRR
	D	T	25	No	No	5	9613	9613C	6T 6T, 9T	2	9612	±15V CMRR
	S	T	35	Yes	Yes	+5 and -10	9622	9622C	6A 6A, 9A	2	9621	Wire — or capability
Receivers For 360/370 I/O Interface	S	T	20	No	Yes	5		75124/ μA8T24	6B, 9B	3	75123/ μA8T13	Hysteresis
Receivers Meeting EIA Standard RS-232-C	S	T	22	No	No	+5 or +12		75154	6B, 9B	4	75150	Hysteresis
	S	R	25	No	No	5		μA1489	6A, 9A	4	μA1488	Response threshold control, 1489A has more Hysteresis than 1489
								μA1489A	6A, 9A	4		
	S	R	50	No	No	±12		9617	6A, 9A	3	9616	
	D	T	60	No	Yes	±12	9627DM	9627	6B, 9B 6B, 9B	2	9616	Also meets MIL-STD-188C Hysteresis
Receivers Meeting EIA Standard RS-422/423	S, D	T	13	Yes	No	5	9637ARM	9637A	6T 6T, 9T	2	9634 9638 9636A	±30mV built in Hysteresis Schottky circuitry also meets MIL-STD-188C

*T = Totem pole, O = Open collector, R = Resistor pull-up

*Not recommended for new designs, but Fairchild will continue to supply these devices for existing applications.

QUAD BUS TRANSCEIVERS

Common Features	Driver Characteristics: Output Current Capability (mA)	Driver Characteristics: t_{pD} Typical (ns)	Driver Characteristics: Strobe Or Enable	Receiver Characteristics: t_{pD} Typical (ns)	Receiver Characteristics: Strobe Or Enable	Device Type For Temperature Range: -55°C to 125°C	Device Type For Temperature Range: 0°C to 70°C	Package Type	Additional Features
• Schottky Circuitry • Single 5 V Supply • Party Line Operation • TTL-Compatible Driver Inputs	100	10	Strobe	10	Strobe	9640DM/26S10	9640/26S10	6B 6B, 9B	• Inverting Bus on 9640/26S10, 9642 • Non-Inverting Bus on 9641/26S11 • 600 mV Receiver Hysteresis on 9642 For Maximum System Noise Margin
	100	12	Strobe	10	Strobe	9641DM/26S11	9641/26S11	6B 6B, 9B	
	100	15	Strobe	8	Strobe	9642DM	9642	6B 6B, 9B	
• Totem-Pole Receiver Outputs • Four Transceivers Per Package	48	12	Enable	8	Enable	μA8T26ADM	μA8T26A	6B 6B, 9B	• 3-State Driver and Receiver Outputs • μA8T26A - Inverting Bus • μA8T28 - Non-Inverting Bus • μP Bus Extender • Replaces NE8T26A and NE8T28
• P-N-P Outputs To Reduce Input Loading	48	12	Enable	8	Enable	μA8T28DM	μA8T28	6B 6B, 9B	

LED DISPLAY DRIVERS

Description	Input Compatibility	Power Supplies (V)	Drivers Per Package	Device Type	Package Type	Additional Features
Segment Drivers	MOS	10	4	75491	6A, 9A	•50mA source/sink capability
		20	4	75491A	6A, 9A	
Digit Drivers		10	6	75492	6A, 9A	•250mA sink capability
		20	6	75492A	6A, 9A	

PERIPHERAL DRIVERS

Maximum Off-State Voltage (V)	Minimum Latch-up Voltage (V)	Maximum Recommended Current (mA)	Typical Delay Time (ns)	Output Clamp Diodes	Drivers Per Package	Input Compatibility	Device Type And Package[5]				Logic Function
							-55°C to 125°C		0°C to 70°C		
30	20	300	25	No	2	TTL, DTL	55450A	6A	75450A	6A, 9A	And*
							55451A	6T	75451A	6T, 9T	And
							55452A	6T	75452A	6T, 9T	Nand
							55453A	6T	75453A	6T, 9T	Or
							55454A	6T	75454A	6T, 9T	Nor
30	20	300	21	No	2	TTL, DTL	55450B	6A	75450B	6A, 9A	And*
							55451B	6T	75451B	6T, 9T	And
							55452B	6T	75452B	6T, 9T	Nand
							55453B	6T	75453B	6T, 9T	Or
							55454B	6T	75454B	6T, 9T	Nor
35	30	300	33	No	2	TTL, DTL	55460	6A	75460	6A, 9A	And*
							55461	6T	75461	6T, 9T	And
							55462	6T	75462	6T, 9T	Nand
							55463	6T	75463	6T, 9T	Or
							55464	6T	75464	6T, 9T	Nor
50	50	350	200	Yes (350 mA)	7	TTL, DTL, CMOS, P-MOS			9665	6B, 9B	Inverting Buffer
						14-V to 25-V P-MOS	9666DM	6B	9666	6B, 9B	
						TTL and 5-V CMOS	9667DM	6B	9667	6B, 9B	
						6-V to 15-V P-MOS, CMOS	9668DM	6B	9668	6B, 9B	
80	55	300	33	No	2	TTL, DTL	55471	6T	75471	6T, 9T	And
							55472	6T	75472	6T, 9T	Nand
							55473	6T	75473	6T, 9T	Or
							55474	6T	75474	6T, 9T	Nor

* With output transistor base connected externally to output of gate
† All plastic packages are on copper lead frames

MOS AND CCD DRIVERS

Supply Voltage (V)	Propagation Delay Time (Typical) (ns)	V_{OH} (Min) (V)	V_{OL} (Max) (V)	Device Type	Package Type	Drivers Per Package	Features
V_{CC} = +5 V_{DD} = 0 to -30	50	+3.5	0.2	9624	6A, 9A	2	• Dual MOS-to-TTL converter • Non-inverting buffer
V_{CC} = +5 V_{DD} = 0 to -30	50	+2.6	0.2	9625	6A, 9A	2	• Dual MOS-to-TTL converter • Inverting buffer
V_{CC1} = +5 V_{CC2} = +5 to +12	9	V_{CC2} - 0.5	0.3	9643	6T, 9T, 6A, 9A	2	• Positive AND TTL-to-MOS/CCD driver • Replaces SN75322 and SN75363 • 9643/4 does not require two external PNP's • High voltage Schottky technology • V_{CC3} supply is not needed • Satisfies F464 CCD memory clock requirements
V_{CC1} = +5 V_{CC2} = +5 to +12	6	V_{CC} - 0.5	0.3	9644	6T, 9T	2	• Dual positive NAND TTL-to-MOS/CCD • Same features as 9643
V_{CC} = +5 V_{DD} = +12	10	V_{DD} - 0.5	0.45	9645 (3245)	7B, 9B	4	• Quad TTL-to-MOS/CCD driver • Replaces Intel 3245 • Satisfies F464 CCD memory requirements
±V = 0 to ±20	10	(+V) -1.0	(-V) +1.0	9646 (DS0026)	6A, 9A 6T, 9T	2	• Dual two phase MOS clock driver • Replaces DS0026 • ±1.5 Amp output current capability

SENSE AMPLIFIERS

Description	Threshold Sensitivity	Common-Mode Range	Type† Of Output	Propagation Delay Time	Device Type For Temperature Range		Package Type	Units Per Package	Additional Features
					-55°C to 125°C	0°C to 70°C			
Core Memory Sense Amplifiers	±2.5mV	±2.5V	R	35ns	55S20	75S20	6B 6B, 9B	1	• Internally compensated ref. amp • Provides memory data register • Complementary outputs
	±2.5mV		R	25ns	55S24	75S24	6B 6B, 9B	2	• Internally compensated ref. amp • Independent strobes
	±4.0mV		R	25ns	5528	7528	6B 6B, 9B	2	• Independent strobes • Test points for strobe timing adjustment
	±4.0mV		O-C	25ns	55232	75232	6B 6B, 9B	2	• Independent strobes • Internally compensated reference amplifier
	±2.5mV		R	25ns	55S234	75S234	6B 6B, 9B	2	• Independent strobes • Internally compensated reference amplifier
	±4.0mV		R	25ns	55238	75238	6B 6B, 9B	2	• Independent strobes • Internally compensated reference amplifier • Test points for strobe timing adjustment
MOS-Memory Sense Amplifiers	±25mV	±3V	T-P	17ns	55107*	75107A*	6A, 3I 6A, 9A	2	• Independent strobes
	±25mV	±3V	O-C	19ns	55108A*	75108A*	6A, 3I 6A, 9A	2	• Independent strobes
	±10mV	±3V	T-P	17ns		75207*	6A, 9A	2	• Independent strobes
			O-C	19ns		75208*	6A, 9A		

† T-P = Totem Pole, O-C = Open Collector, R = Resistor Pull-Up

* See Line Circuit Section for details

MEMORY DRIVERS*

Description	Maximum Output Current	Propagation Delay Time (ns)	Power Supplies	Device Type For Temperature Range		Package Type	Additional Features
				-55°C to 125°C	0°C to 70°C		
Dual Sink/Source Memory Drivers	600mA	35	V_{CC1} - 5 V V_{CC2} variable to 24 V	55325	75325	7B, 4L 7B, 9B	•Also used for high-voltage, high-current driver applications •Output transient voltage protection •Source output terminals swing between V_{CC2} and ground
Quadruple Sink Memory Drivers		35	V_{CC1} - 5 V V_{CC2} variable to 24 V	55327	75327	7B, 4L 7B, 9B	•Also used for high speed magnetic memory applications •Output transient voltage protection •Output capable of swinging between V_{CC2} and ground
Quadruple Memory Drivers		30	V_{CC} = 5 V	55326	75326	7B, 4L 7B, 9B	•Also used for high-voltage, high-current driver applications •Output transient voltage protection •24V output capability

*Also see MOS/CCD driver section

SPECIAL FUNCTIONS-TIMERS AND COUNTERS

Device Number	Function	Time Delay Hours	Free Running Frequency (kHz)	Output Compatibility	Output Current (mA)	Supply Voltage V (Max)	Timing Error %	Package(s)
μA555	Single Timer	1.0	100	TTL	200	+18	1.0	5S, 6T, 9T, 6A
μA556	Dual Timer	1.0	100	TTL	200	+18	1.0	6A, 9A
μA2240	Programmable Timer-Counter	120	—	TTL	5.0	+18	0.5	7B, 9B

SPECIAL FUNCTIONS-TRANSISTOR AND DIODE ARRAYS

Device Number	Function	Balanced Input	Balanced Output	Low Noise	AGC Capability	Multiple Unit	Wideband	Switching Application	V_{CBO}-V	V_{CEO}-V	V_{EBO}-V	I_C-MA	V_{BE} or V_O	Package(s)
μA726*	Temp Controlled Diff Pair	•	•	•	—	—	—	—	40	30	5.0	5.0	2.5	5U
μA3018*	Matched Transistor Array	•	•	—	•	•	•	—	20	15	5.0	50	5.0	5D
μA3018A*	Matched Transistor Array	•	•	—	•	•	•	—	30	15	5.0	50	2.0	5D
μA3019*	Quad Plus Two Diode Array	—	—	—	—	—	—	•	—	—	—	—	5.0	5Q
μA3026*	Dual Diff Amp Transistor Array	—	—	—	—	—	—	—	20	15	5.0	50	5.0	5D
μA3036*	Dual Darlington Transistor Array	•	•	•	—	•	—	—	30	15	5.0	50	—	5Q
μA3039*	Hex Ultra Fast Diode Array	—	—	—	—	—	—	•	—	—	—	—	5.0	5D
μA3045*	Diff Pair Plus Three Transistors	•	•	—	—	•	•	—	20	15	5.0	50	5.0	6A
μA3046	Diff Pair Plus Three Transistors	•	•	—	—	•	•	—	20	15	5.0	50	5.0	6A, 9A
μA3054	Dual Diff Amp Transistor Array	—	—	—	—	•	—	—	20	15	5.0	50	5.0	6A, 9A
μA3086	Dual Diff Plus Three Transistors	•	•	—	—	•	•	—	20	15	5.0	50	—	6A, 9A

*Military grade available

LINEAR INDUSTRY CROSS REFERENCE

LINEAR INDUSTRY CROSS REFERENCE GUIDE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
1458CE	μA1458CHC	
1458CP	μA1458CTC	
1458E	μA1458HC	
1458P	μA1458TC	
1558E	μA1558HM	
3207A		9645
3245	9645/3245	
527		μA760HM
532		μA798TC
536		μA740AHM
556CJ	μA556PC	
709AE	μA709AHM	
709AH	μA709AFM	
709AL	μA709ADM	
709BE	μA709HM	
709BH	μA709FM	
709BL	μA709DM	
709CE	μA709HC	
709CJ	μA709PC	
709CL	μA709DC	
710BE	μA710HM	
710BH	μA710FM	
710BL	μA710DM	
710CE	μA710HC	
710CL	μA710DC	
711BE	μA711HM	
711BH	μA711FM	
711BL	μA711DM	
711CE	μA711HC	
711CJ	μA711PC	
711CL	μA711DC	
723BE	μA723HM	
723BL	μA723DM	
723CE	μA723HC	
723CJ	μA723PC	
723CL	μA723DC	
733DC	μA733DC	
733DM	μA733DM	
733FM	μA733FM	
733HC	μA733HC	
733HM	μA733HM	
741BE	μA741HM	
741BH	μA741FM	
741BL	μA741DM	
741CE	μA741HC	
741CJ	μA741PC	
741CP	μA741TC	
747BE	μA747HM	
747BL	μA747DM	
747CE	μA747HC	
747CJ	μA747PC	
747CL	μA747DC	
748BE	μA748HM	
748BH	μA748FM	
748BL	μA748DM	
748CE	μA748HC	
748CL	μA748DC	
748CP	μA748TC	
75S107		75107APC
75S108		75108APC
75S207		75207PC
75S208		75208PC
75322	9643DC	
75361	9644DC	
75361A		9643DC
75363	9643DC	
75450N	75450APC	
78M05BE	μA78M05HM	
78M05CE	μA78M05HC	
78M06BE	μA78M06HM	
78M06CE	μA78M06HC	
78M08BE	μA78M08HM	
78M08CE	μA78M08HC	
78M12BE	μA78M12HM	
78M12CE	μA78M12HC	
78M15BE	μA78M15HM	
78M15CE	μA78M15HC	
78M20BE	μA78M20HM	
78M20CE	μA78M20HC	
78M24BE	μA78M24HM	
78M24CE	μA78M24HC	
8216	μA8T26A	
8T26A	μA8T26APC	
8T26A	μA8T26ADC	
8T28	μA8T28	
AN217		μA721PC
AM26LS29		9634
AM26LS30		9636A
AM26S10	9640	
AM26S11	9641	
AN559	μA0802	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA1190	TDA1190Z	
CA1310	μA1310	
CA3004T		μA703HC
CA3005T		μA703HC
CA3006T		μA703HC
CA3008		μA741FM
CA3008A		μA741FM
CA3010		μA741HM
CA3010A		μA741HM
CA3011T		μA753TC
CA3012T		μA753TC
CA3013T		μA753TC
CA3014T		μA753TC
CA3015		μA741HM
CA3015A		μA741HM
CA3016		μA741FM
CA3016		μA741FM
CA3018	μA3018HM	
CA3018A	μA3018HM	
CA3019	μA3019HM	
CA3021T		μA757DC
CA3022T		μA757DC
CA3023T		μA757DC
CA3026	μA3026HM	
CA3028AT		μA703HC
CA3028T		μA703HC
CA3029		μA741TC
CA3029A		μA741TC
CA3030		μA741TC
CA3030A		μA741TC
CA3036	μA3036HM	
CA3037		μA741DM
CA3037A		μA741DM
CA3038		μA741DM
CA3038A		μA741DM
CA3039	μA3039HM	
CA3041E		μA3065PC
CA3024E		μA3065PC
CA3043		μA3065PC
CA3044T		μA3064
CA3045	μA3045DM	
CA3046	μA3046DC	
CA3045	μA3054DC	
CA3058E		μA742DC
CA3059		μA742DC

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA3064E	μA3064PC	
CA3064T	μA3064HC	
CA3065E	μA3065PC	
CA3070E	μA780PC	
CA3071E	μA781PC	
CA3072E	μA746PC	
CA3075E	μA3075PC	
CA3078AS		μA776DM
CA3078AT		μA776HM
CA3078S		μA776TC
CA3078T		μA776HC
CA3079		μA742DC
CA3085		μA723HC
CA3085A		μA723HC
CA3085AF		μA723DC
CA3085AS		μA723DC
CA3085B		μA723HM
CA3085BF		μA723DM
CA3085BS		μA723DC
CA3085F		μA723DC
CA3085S		μA723DC
CA3086	μA3086DC	
CA3088E		μA720PC
CA3089E	μA3089PC	
CA3090E		μA758PC
CA3123E	μA720PC	
CA3126Q	μA787PC	
CA3134		TDA1190
CA3458S	1458TC	
CA3458T	1458HC	
CA3558S		1558HM
CA3558T	1558HM	
CA3741CS	μA741TC	
CA3741CT	μA741HC	
CA3741S		μA741HM
CA3741T	μA741HM	
CA3747CE	μA747PC	
CA3747CF		μA747DC
CA3747CT	μA747HC	
CA3747E	μA747DM	
CA3747F	μA747DM	
CA3747T	μA747HM	
CA3748CS	μA748TC	
CA3748CT	μA748HC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
CA3748S		μA748HM
CA3748T	μA748HC	
CA758E	μA758PC	
DAC-08	μA0801	
DAC-08A	μA0801A	
DAC-08C	μA0801C	
DAC-08E	μA0801E	
DS0026	9646/0026	
DS3486		9637A
DS3487		9634
DS3645	9645/3245	
DS3691		9636A
DS3692		9634
DS8834		μA8T26A
DS8835		μA8T26A
DS78LS120		9637A
DS8T26A	μA8T26A	
HA1156	μA1310	
HA11226		μA7300
LA1201		μA721PC
LAS1405	μA78H05KC	
LAS1412	μA78H12KC	
LAS1415	μA78H15KC	
LF111H	μAF111HM	
LF155AH	μAF155AHM	
LF155H	μAF155HM	
LF156AH	μAF156AHM	
LF156H	μAF156HM	
LF157AH	μAF157AHM	
LF157H	μAF157HM	
LF211H	μAF211HM	
LF311H	μAF311HC	
LF355AH	μAF355AHC	
LF355H	μAF355HC	
LF356A	μAF356AHC	
LF356H	μAF356HC	
LF357	μAF357HC	
LF357A	μAF357AHC	
LH0002	SH0002	
LH0021CK		μA791KC
LH0021K		μA791KM
LH0021K/883		μA791KMQB
LH0041		μA759HM
LH0061C		μA791KC
LH0061CK		μA791KM
LH0061K		μA791KM
LH101H		μA741HM
LH201H		μA741HM
LH2101AD		μA747ADM
LH740AH		μA740AHM
LM101AD	μA101ADM	
LM101AF	μA101AFM	
LM101AH	μA101AHM	
LM101D	μA101DM	
LM101H	μA101HM	
LM1011		μA7300
LM102H	μA102HM	
LM104H	μA104HM	
LM105H	μA105HM	
LM106F		μA710FM
LM106H		μA710HM
LM107H	μA107HM	
LM108AD	μA108ADM	
LM108AF	μA108AFM	
LM108AH	μA108AHM	
LM108D	μA108DM	
LM108F	μA108FM	
LM108H	μA108HM	
LM109K	μA109KM	
LM111H	μA111HM	
LM117		μA78GKM
LM120H-05		μA79M05HM
LM120H-12		μA79M12HM
LM120H-15		μA79M15HM
LM120K-05		μA7905KM
LM120K-12		μA7912KM
LM124D	μA124DM	μA3503DM
LM1303N		μA749PC
LM1304N	μA732PC	
LM1307N	μA767PC	
LM1310	μA1310	
LM139	μA139DM	
LM139A	μA139ADM	
LM1414J		μA711DC
LM1458H	μA1458HC	
LM1458N	μA1458TC	
LM1488J	μA1488	9616DC
LM1489AJ	μA1489A	9617DC
LM1489J	μA1489	9617DC
LM1496H	μA796HC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM1496N	μA796PC	
LM1514J		μA711DM
LM1558H	μA1558HM	
LM160H	μA760HM	
LM1800N	μA758PC	
LM1820N	μA720PC	
LM1829N	μA787PC	
LM1841N	μA2136PC	
LM1850N		μA7390PC
LM198	μAF198	
LM210AF	μA201AFM	
LM201AH	μA201AHM	
LM201D	μA201DM	
LM201H	μA201HM	
LM202H	μA202HM	
LM204H	μA204HM	
LM205H	μA205HM	
LM206F		μA710FM
LM206H		μA710HC
LM207H	μA207HM	
LM208AD	μA208ADM	
LM208AF	μA208AFM	
LM208AH	μA208AHM	
LM208D	μA208DM	
LM208F	μA208FM	
LM208H	μA208HM	
LM209K	μA209KM	
LM220H-05		μA79M05HM
LM220H-12		μA79M12HM
LM220H-15		μA79M15HM
LM220K-05		μA7905KM
LM220K-12		μA7912KM
LM220K-15		μA7915KM
LM222N		μA555TC
LM224D	μA224DM	
LM2901N	μA2901PC	μA775PC
LM2902N	μA2902PC	
LM2904N		μA798TC
LM2905N		μA555TC
LM2907N		μA4151TC
LM2917N		μA7151PC
LM301AD	μA301ADC	
LM301AH	μA301AHC	
LM301AN	μA301ATC	
LM3018AH	μA3018HM	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM3018H	μA3018HM	
LM3019H	μA3019HM	
LM302H	μA302HC	
LM3026H	μA3026HM	
LM3039H	μA3039HM	
LM304H	μA304HC	
LM3045D	μA3045DM	
LM3046N	μA3046DC	
LM305AH	μA305AHC	
LM305H	μA305HC	
LM3053N	μA753TC	
LM3054N	μA3054DC	
LM306H		μA710HC
LM3064H	μA3064HC	
LM3065N	μA3065PC	
LM307H	μA307HC	
LM307N	μA307TC	
LM3070N	μA780PC	
LM3075N	μA3075PC	
LM308AD	μ308ADC	
LM308AH	μA308AHC	
LM308D	μA308DC	
LM308H	μA308HC	
LM308N	μA308TC	
LM3086N	μA3086DC	
LM309K	μA309KC	
LM311H	μA311HC	
LM311N	μA311TC	
LM320H-05		μA79M05HC
LM320H-12		μA79M12HC
LM320H-15		μA79M15HC
LM320K-05		μA7905KC
LM320K-12		μA7912KC
LM320K-15		μA7915KC
LM320MP-12		μA79M12AUC
LM320MP-15		μA79M15AUC
LM320MP-5.0		μA79M05AUC
LM320MP-6.0		μA79M06AUC
LM320MP-8.0		μA79M08AUC
LM320T-12		μA7912UC
LM320T-15		μA7915UC
LM320T-18		μA7918UC
LM320T-24		μA7924UC
LM320T-5		μA7905UC
LM320T-6		μA7906UC

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM320T-8		μA7908UC
LM323K	SH323KC	
LM323K	μA78H05KC	
LM324D	μA324DC	μA3403DC
LM324N	μA324PC	μA3403PC
LM339A	μA339ADC	
LM340K-05	μA7805KC	
LM340K-06	μA7806KC	
LM340K-08	μA7808KC	
LM340K-12	μA7812KC	
LM340K-15	μA7815KC	
LM340K-18	μA7818KC	
LM340K-24	μA7824KC	
LM340T-05	μA7805UC	
LM340T-06	μA7806UC	
LM340T-08	μA7808UC	
LM340T-12	μA7812UC	
LM340T-15	μA7815UC	
LM340T-18	μA7818UC	
LM340T-24	μA7824UC	
LM342P-12		μA78C12U1C
LM342P-15		μA78C15U1C
LM342P-18		μA78C18U1C
LM342P-24		μA78C24U1C
LM342P-5.0		
LM342P-6.0		
LM432P-8.0		μA78C08U1C
LM350N		75453BPC
LM351N	75453BPC	
LM358H	μA798HM	
LM360H	μA760HC	
LM376N	μA376TC	
LM380N		TBA820L
LM381AN		μA739DC
LM381N		μA739PC
LM382N		μA739PC
LM383	TDA2002	
LM386		μA7307
LM387N		μA739PC
LM388N		TBA820L
LM390	μAF398	
LM3905N		μA555TC
LM4250H		μA776HM
LM4250CH		μA776HC
LM4250CN		μA776DC

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM4250H		μA776HM
LM5108AJ	75108ADC	
LM55107AJ	55107ADM	
LM55108AJ	55108ADM	
LM55109J	55109DM	
LM55110J	55110A	
LM5524J	55S24	
LM5528J	5528DM	
LM5534J	55S234DM	
LM555CN	μA555TC	
LM556CN	μA556PC	
LM703LH	μA703HC	
LM709CH	μA709HC	
LM709CN	μA709PC	
LM709H	μA709HM	
LM710CH	μA710HC	
LM710CN	μA710PC	
LM710H	μA710HM	
LM711CH	μA711HC	
LM711CN	μA711PC	
LM711H	μA711HM	
LM723CD	μA723DC	
LM723CH	μA723HC	
LM723CN	μA723PC	
LM723D	μA723DM	
LM723H	μA723HM	
LM725AH	μA725AHM	
LM725CH	μA725HC	
LM725H	μA725HM	
LM733CD	μA733DC	
LM733CH	μA733CH	
LM733CN	μA733PC	
LM733D	μA733DM	
LM733H	μA733HM	
LM741CD	μA741DC	
LM741CH	μA741HC	
LM741CN-08	μA741TC	
LM741CN-14	μA741PC	
LM741F	μA741FM	
LM741H	μA741HM	
LM746N	μA746PC	
LM747CD	μA747DC	
LM747CH	μA747HC	
LM747CN	μA747PC	
LM747D	μA747DM	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
LM747H	μA747HM	
LM748CH	μA748HC	
LM748CN	μA748TC	
LM748H	μA748HM	
LM75107AJ	75107ADC	
LM75107AN	75107APC	
LM75108AN	75108APC	
LM75109J	75109DC	
LM75109N	75109PC	
LM75110J	75110A	
LM75110N	75110A	
LM75150J	75150DC	
LM75150N	75150PC	9616DC
LM75154J	75154DC	9617DC
LM75154N	75154PC	
LM75207J	75207DC	
LM75207N	75207PC	
LM75208J	75208DC	
LM75208N	75208PC	
LM7524J	75S24	
LM7524N	75S24	
LM7528J	7528DC	
LM7528N	7528PC	
LM75325J	75325DC	
LM75325N	75325PC	
LM7534J	75S234DC	
LM7534N	75S234PC	
LM7535J	7535DC	
LM7535N	7535PC	
LM75450J	75450BDC	
LM75450N	75450BPC	
LM75451N	75451BTC	
LM75452N	75452BTC	
LM75453N	75453BTC	
LM75454N	75454BTC	
M51728		μA7392
MC1303P		μA749PC
MC1304P	μA732PC	
MC1305P		μA732PC
MC1306		μA7307
MC1307P	μA767PC	
MC1310P	μA1310PC	
MC1311P	μA758PC	
MC1312P	μA1312PC	
MC1324P		μA746PC
MC1326P		μA746PC
MC1327		TDA2522
MC1328P		μA746PC
MC1339P		μA749PC
MC1350P		μA757DC
MC1351P		μA3065PC
MC1352P		μA757DC
MC1353P		μA757DC
MC1355P		μA3065PC
MC1357P	μA2136PC	
MC1358P		μA3065PC
MC1364P	μA3064PC	
MC1370P	μA780PC	
MC1371P	μA781PC	
MC1375P	μA3075PC	
MC1391	μA1391TC	
MC1394P	μA1394TC	
MC1398P		μA787PC
MC1408L6	μA0802C	
MC1408L7	μA0802B	
MC1408L8	μA0802A	
MC1410G		μA733HC
MC1411	9665	
MC1412	9666	
MC1413	9667	
MC1414L		μA711DC
MC1414P		μA711PC
MC1416	9668	
MC1420G		μA733HC
MC1435G		μA749DHC
MC1435L		μA749DC
MC1437L		μA749DC
MC1437P		μA749PC
MC1438R		μA791KC
MC14443		μA9708
MC14447		μA9708
MC1456CG		μA776HC
MC1456CL		μA776DC
MC1456G		μA776HC
MC1456L		μA776DC
MC1458CG	μA1458CHC	
MC1458CP1	μA1458CTC	
MC1458G	μA1458HC	
MC1458P1	μA1458TC	
MC1496G	μA796HC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC1496P	μA796PC	
MC1508L8	μA0802	
MC1510F		μA733FM
MC1510G		μA733HM
MC1514F		μA711FM
MC1514L		μA711DM
MC1520G		μA733HM
MC1535G		μA749HM
MC1535L		μA749DM
MC1537L		μA749DM
MC1550G		μA757DC
MC1556G		μA776HM
MC1556L		μA776DM
MC1558G	μA1558HM	
MC1560G		μA78M00HM
MC1560R		μA7800KM
MC1561G		μA78MGHM
MC1561R		μA78MGHM
MC1563G		μA79MGHM
MC1563R		μA79MGHM
MC1569G		μA78MGHM
MC1569R		μA78GKM
MC1590		μA757DC
MC1596G	μA796HM	
MC1709CG	μA709HC	
MC1709CL	μA709DC	
MC1709CP1	μA709TC	
MC1709CP2	μA709PC	
MC1709F	μA709FM	
MC1709G	μA709HM	
MC1709L	μA709DM	
MC1710CG	μA710HC	
MC1710CL	μA710DC	
MC1710CP	μA710PC	
MC1710F	μA710FM	
MC1710G	μA710HM	
MC1710L	μA710DM	
MC1711CG	μA711HC	
MC1711CL	μA711DC	
MC1711CP	μA711PC	
MC1711F	μA711FM	
MC1711G	μA711HM	
MC1711L	μA711DM	
MC1712CG	μA702HC	
MC1712CL	μA702DC	
MC1712F	μA702FM	
MC1712L	μA702DM	
MC1723CG	μA723HC	
MC1723CL	μA723DC	
MC1723G	μA723HM	
MC1723L	μA723DM	
MC1741CG	μA741HC	
MC1741CG	μA747HC	
MC1741CL	μA741DC	
MC1741CP1	μA741TC	
MC1741CP2	μA741PC	
MC1741F	μA741FM	
MC1741G	μA741HM	
MC1741L	μA741DM	
MC1747CL	μA747DC	
MC1747G	μA747HM	
MC1747L	μA747DM	
MC1748CG	μA748HC	
MC1748CP1	μA748TC	
MC1748G	μA748HM	
MC1776CG	μA776HC	
MC1776G	μA776HM	
MC3245	9645/3345	
MC3301P	μA3301PC	
MC3302P	μA3302PC	
MC3360		μA7307
MC3401P	μA3401PC	
MC3403L	μA3403DC	
MC3403P	μA3403PC	
MC3425		μA7390TC
MC3430		75107APC
MC3433		75108APC
MC3440		9642DC
MC3441		9642DC
MC3443		9642DC
MC3448A	μA3448A	
MC3456	μA556PC	
MC3476	μA776PC	
MC3486		9637A
MC3487		9634
MC3503L	μA3503DM	
MC75107L	75107ADC	
MC75107P	75107APC	
MC75108L	75108ADC	
MC75108P	75108APC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC75109L	75109DC	
MC75109P	75109PC	
MC75110L	75110ADC	
MC75110PC	75110APC	
MC75207L	75207DC	
MC75207P	75207PC	
MC75208L	75208DC	
MC75208P	75208PC	
MC7524L	75S24	
MC7524P	75S24	
MC7528L	7528DC	
MC7528P	7528PC	
MC75325L	75325DC	
MC75325P	75325PC	
MC7534L	755234DC	
MC7534P	755234DC	
MC75365		9645PC
MC75450L	75450BDC	
MC75450P	75450BPC	
MC75451P	75451BTC	
MC75452P	75452BTC	
MC75453P	75453BTC	
MC75454P	75454BTC	
MC75491P	75491PC	
MC75492P	75492PC	
MC7705CP		μA78M05UC
MC7706CP		μA78M06UC
MC7708CP		μA78M08UC
MC7712CP		μA78M12UC
MC7715CP		μA78M15UC
MC7718CP		μA7818UC
MC7720CP		μA78M20UC
MC7724CP		μA78M24UC
MC7805CK	μA7805KC	
MC7805CP	μA7805UC	
MC7806CK	μA7806KC	
MC7806CP	μA7806UC	
MC7808CK	μA7808KC	
MC7808CP	μA7808UC	
MC7812CK	μA7812KC	
MC7812CP	μA7812UC	
MC7815CK	μA7815KC	
MC7815CP	μA7812UC	
MC7818CK	μA7812KC	
MC7818CP	μA7812UC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MC7824CK	μA7824KC	
MC7824CP	μA7824UC	
MC7905CK	μA7905KC	
MC7905CP	μA7905UC	
MC7906CK	μA7906KC	
MC7906CP	μA7906UC	
MC7908CK	μA7908KC	
MC7908CP	μA7908UC	
MC7912CK	μA7912KC	
MC7912CP	μA7912UC	
MC7915CK	μA7915KC	
MC7915CP	μA7915UC	
MC7918CK	μA7918KC	
MC7918CP	μA7918UC	
MC7924CK	μA7924KC	
MC7924CP	μA7924UC	
MC8T13L	μA8T13DM	
MC8T13P	μA8T13PC	
MC8T14L	μA8T14DM	
MC8T23P	μA8T23PC	
MC8T24P	μA8T24PC	
MC8T26A	μA8T26A	
MFC4060A		μA78MGT2C
MFC4062A		μA78MGT2C
MFC4063A		μA78MGT2C
MFC4064A		μA78MGT2C
MFC6030A		μA78MGT2C
MFC6032A		μA78MGT2C
MFC6033A		μA78MGT2C
MFC6034A		μA78MGT2C
MFC8000		μA739PC
MFC8001		μA739PC
MFC8002		μA739PC
MFC8030		μA703HC
MFC8070		μA742DC
MLM101AG	μA101AHM	
MLM104G	μA104HM	
MLM105G	μA105HM	
MLM107G	μA107HM	
MLM109G		μA78M05HM
MLM109K		μA109KM
MLM110G	μA110HM	
MLM201AG	μA201AHM	
MLM204G	μA204HM	
MLM205G	μA205HM	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
MLM207G	μA207HM	
MLM209G		μA78M05HM
MLM209K	μA209KM	μA7805KM
MLM210G	μA210HM	
MLM301AG	μA301AHC	
MLM301AP1	μA301ATC	
MLM304G	μA304HC	
MLM305G	μA305HC	
MLM307G	μA307HC	
MLM309G		μA78M05HC
MLM309K	μA309KC	
MLM310G	μA310HC	
MLM311G	μA311HC	
MLM311P1	μA311TC	
ML1408-6L	μA0802CDC	
ML1408-7L	μA0802BDC	
ML1408-8L	μA0802ADC	
ML1508-8L	μA0802DM	
MMH0026	9646/0026	
NE515A	μA733PC	
NE515K		μA733HC
NE521A		75107APC
NE521F		75107ADC
NE522A		75108APC
NE522F		75108ADC
NE526A		μA760DC
NE526K		μA760HC
NE527K		μA760HC
NE529K		μA760HC
NE536T	μA740HC	μA740HC
NE545		μA7300
NE550A		μA723PC
NE550L		μA723HC
NE555V	μA555TC	
NE556A	μA556PC	
NE556F	μA556DC	
NE592A		μA733PC
NE645		μA7300
N10145	10145A	
N10149	10146	
N5071A	μA781PC	
N5072A	μA746PC	
N5558T	μA1458HC	
N5558V	μA1458TC	
N5570B	μA780PC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
N8T13B	μA8T13PC	
N8T13F	μA8T13DC	
N8T14B	μA8T14PC	
N8T14F	μA8T14DC	
N8T15F		9616DC
N8T16F		9627DC
N8T23B	μA8T23PC	
N8T23F	μA8T23DC	
N8T24B	μA8T24PC	
N8T24F	μA8T24DC	
N8T26A	μA8T26A	
OP-02		μA741AHM
OP-04		μA741AHM
OP-05		μA714HC
OP-07	μA714HC	
PA239A		μA739PC
RC1488D	μA1488	9616DC
RC1489AD	μA1489A	9617DC
RC1489D	μA1489	9617DC
RC4136D	μA4136DC/DM	
RC4136DB	μA4136PC	
RC4136DP	μA4136PC	
RC4151	μA4151	μA7151
RC4152		μA7151
RC4558DN	μA4558TC	
RC4558T	μA4558HC	
RC55109D	55109DM	
RC555DN	μA555TC	
RC556D	μA556DC	
RC556DP	μA556PC	
RC733TF	μA733HC	
RC75107AD	75107ADC	
RC75107AP	75107APC	
RC75108AD	75108ADC	
RC75108ADP	75108APC	
RC75109D	75109DC	
RC75109DP	75109PC	
RC75110D	75110ADC	
RC75150D	75150DC	
RC75154M	75154DC	
RC7524M	75S24DC	
RC7524MP	75S24PC	
RC7528M	7528DC	
RC7528MP	7528PC	
RC75325M	75325DC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
RC75325MP	75325PC	
RC8T13M	μA8T13DC	
RC8T13MP	μA8T13PC	
RC8T14M	μA8T14DC	
RC8T14MP	μA8T14PC	
RC8T23M	μA8T23DC	
RC8T23MP	μA8T23PC	
RC8T24M	μA8T24DC	
RC8T24MP	μA8T24PC	
RC9621D	9621DC	
RC9622D	9622DC	
RM4136D	μA4136DM	
RM55107AD	55107ADM	
RM55108AD	55108ADM	
RM55110D	55110DM	
RM5524M	5524DM	
RM5525M	5525DM	
RM55325M	55325DM	
RM555T	μA555HM	
RM556D	μA556DM	
RM733TF	μA733HM	
RM8T13M	μA8T13DM	
RM8T14M	μA8T14DM	
SE515K		μA733HM
SE526A		μA760DM
SE526K		μA760HM
SE527K		μA760HM
SE529A		μA733DM
SE529K		μA760HM
SE536T		μA740HM
SE550L		μA723HM
SE592K		μA733HM
SH76008		TDAA2002
SH76018		TDA2002
SN2660JA		μA776DM
SN52L022L		μA798HM
SN52L044JA		μA3503DM
SN52309LA		μA78M05HM
SN52506J		μA711DM
SN52510L		μA710HM
SN52514J		μA711DM
SN52520J		μA710DM
SN52558L	μA1558HM	
SN52660L		μA776HM
SN52702J	μA702DM	
SN52702L	μA702HM	
SN52709J	μA709DM	
SN52709L	μA709HM	
SN52710J	μA710DM	
SN52710L	μA710HM	
SN52711J	μA711DM	
SN52711L	μA711HM	
SN52723J	μA723DM	
SN52723L	μA723HM	
SN52741J	μA741DM	
SN52741L	μA741HM	
SN52747J	μA747DM	
SN52747L	μA747HM	
SN52748J	μA748DM	
SN52748L	μA748HM	
SN52771J		μA776DM
SN52771L		μA776HM
SN52777J	μA777DM	
SN52777L	μA777HM	
SN52810J		μA710DM
SN52810L		μA710HM
SN52811J		μA711DM
SN52811L		μA711HM
SN52820J		μA711DM
SN529K		μA733HC
SN5510FA		μA833FM
SN5510L		μA733HM
SN55107AL	55107ADM	
SN55107BJ	55107BDM	
SN55108AJ	55108ADM	
SN551088J	55108BDM	
SN55109J	55109DM	
SN5511FA		μA733FM
SN5511L		μA733HM
SN55110J	55110ADM	
SN55112J	55112DM	
SN55114J	9614DM	
SN55114SB	9614FM	
SN55115J	9615DM	
SN55115SB	9615FM	
SN5512L		μA733HM
SN55121J	55121DM	
SN55122J	55122DM	
SN55123J	55123DM	
SN55124J	55124DM	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN5514L		μA733HM
SN55207J	55207DM	
SN55208J	55208DM	
SN55234J	55S234DM	
SN5524J	55S24DM	
SN55325J	55325DM	
SN55325SB	55325FM	
SN55326SB	55326FM	
SN55327SB	55327FM*	
SN55450BJ	55450BDM	
SN55450J	55450DM	
SN55451BL	55451BHM	
SN55451L	55451HM	
SN55452BL	55452BHM	
SN55452L	55452HM	
SN55453BL	55453BHM	
SN55453L	55453HM	
SN55454BL	55454BHM	
SN55454L	55454HM	
SN55460J	55460DM	
SN55461L	55461HM	
SN55462L	55462HM	
SN55463L	55463HM	
SN55464L	55464HM	
SN71710J	μA710DC	
SN72L022L		μA798HC
SN72L022P		μA798TC
SN72L044JA		μA3403DC
SN72L044N		μA3403PC
SN72301AN	μA301ADC	
SN72301L	μA301AHC	
SN72301P	μA301ATC	
SN72304L	μA104HM	
SN72305AL	μA305AHC	
SN72305L	μA305HC	
SN72307L	μA307HC	
SN72307P	μA307TC	
SN72308AL	μA308AHC	
SN72308AN	μA308ADC	
SN72308L	μA308HC	
SN72308N	μA308DC	
SN72309LA		μA78M05HC
SN72310L	μA310HC	
SN72311L	μA311HC	
SN72311P	μA311TC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN72376P	μA376TC	
SN72440J		μA742DC
SN72440N		μA742DC
SN72506J		μA711DC
SN72506N		μA711PC
SN72510J		μA710DC
SN72510L		μA710HC
SN72510N		μA710PC
SN72514J		μA711DC
SN72514N		μA711PC
SN72555P	μA555TC	
SN72556N	μA556PC	
SN72558L	μA1458HC	
SN72558P	μA1458TC	
SN72660JA		μA776DC
SN72660L		μA776HC
SN72660N		μA776DC
SN72660P		μA776TC
SN72702J	μA702DC	
SN72702L	μA702HC	
SN72709J	μA709DC	
SN72709L	μA709HC	
SN72709P	μA709TC	
SN72710L	μA710HC	
SN72710N	μA710PC	
SN72711J	μA711DC	
SN72711L	μA711HC	
SN72711N	μA711PC	
SN72720J		μA710DC
SN72720N		μA710PC
SN72723J	μA723DC	
SN72723L	μA723HC	
SN72723N	μA723PC	
SN72733J	μA733DC	
SN72733L	μA733HC	
SN72733N	μA733PC	
SN72741J	μA741DC	
SN72741L	μA741HC	
SN72741N	μA741PC	
SN72741P	μA741TC	
SN72747J	μA747DC	
SN72747L	μA747HC	
SN72748J	μA748DC	
SN72748L	μA748HC	
SN72748N	μA748DC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN72748P	μA748TC	
SN72771J		μA776DC
SN72771L		μA776HC
SN72771N		μA776DC
SN72771P		μA776TC
SN72777J	μA777DC	
SN72777L	μA777HC	
SH72777N	μA777DC	
SN72777P	μA777TC	
SN72810J		μA710DC
SN72810L		μA710HC
SN72810N		μA710PC
SN72811J		μA711DC
SN72811L		μA711HC
SN72811N		μA711PC
SN72820J		μA711DC
SN72820N		μA711PC
SN7496	7496	
SN7497	7497	
SN7510L		μA733HC
SN75107AJ	75107ADC	
SN75107AN	75107APC	
SN75107BJ	75107BDC	
SN75107BN	75107BPC	
SN75108AJ	75108ADC	
SN75108AN	75108APC	
SN75108BJ	75108BDC	
SN75108BN	75108BPC	
SN75109J	75109DC	
SN75109N	75109PC	
SN7511L		μA733HC
SN7511N		μA733PC
SN75110AJ	75110ADC	
SN75110AJ	75110APC	
SN75110J	75110ADC	
SN75110N	75110APC	
SN75112J	75112DC	
SN75112N	75112PC	
SN75114J	9614DC	
SN75114N	9614PC	
SN75115J	9615DC	
SN75115N	9615PC	
SN7512L		μA733HC
SN7512N		μA733PC
SN75121J	75121DC	
SN75121N	75121PC	
SN75122J	75122DC	
SN75122N	75122PC	
SN75123J	75123DC	
SN75123N	75123PC	
SN75124J	75124DC	
SN75124N	75124PC	
SN75124L		μA733HC
SN7514P		μA733PC
SN75150J	75150DC	9616DC
SN75150P	75150PC	9616DC
SN75152J	9627DC	
SN75154J	75154DC	9617DC
SN75182N		9615DC
SN75183N		9614DC
SN75188J	1488DC	
SN75189AJ	1489ADC	
SN75189J	1489DC	
SN7520	75S20	
SN75207J	75207DC	
SN75207N	75207PC	
SN75208J	75208DC	
SN75208N	75208PC	
SN75224J	75S24DC	
SN75224N	75S24PC	
SN75225J	75225DC	
SN75225N	75225PC	
SN75232J	75232DC	
SN75232N	75232PC	
SN75234J	75S234DC	
SN75234N	75S234PC	
SN75235J	75235DC	
SN75235N	75235PC	
SN75238J	75238DC	
SN75238N	75238PC	
SN7524J	75S24DC	
SN7524N	75S24PC	
SN7528J	7528DC	
SN7528N	7528PC	
SN75325J	75325DC	
SN75325N	75325PC	
SN75326J	75326DC*	
SN75236N	75326PC*	
SN75327J	75327DC	
SN75327N	75327PC	

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
SN7534J	75S234DC	
SN7534N	75S234PC	
SN75450BJ	75450BDC	
SN75450BN	75450BPC	
SN75450N	75450BPC	
SN75451BL	75451BHC	
SN75451BP	75451BTC	
SN75451P	75451BTC	
SN75452BL	75452BHC	
SN75452BP	75452BTC	
SN75452P	75452BTC	
SN75453BL	75453BHC	
SN75453BP	75453BTC	
SN75453P	75453BTC	
SN75454BL	75454BHC	
SN75454P	75454BTC	
SN75460J	75460DC	
SN75460N	75460PC	
SN75461L	75461HM	
SN75461L	75462HM	
SN75461P	75461TC	
SN75463P	75463TC	
SN75464L	75464HM	
SN75464P	75464TC	
SN75471L	75471HC	
SN75471P	75471TC	
SN75472L	75472HC	
SN75472P	75472TC	
SN75473L	75473HC	
SN75473P	75473TC	
SN75474L	75474HC	
SN75474P	75474TC	
SN75491N	75491PC	
SN75492N	75492PC	
SN76001N	TBA641A12	
SN76005ND		μA706BPC
SN76024ND		μA706BPC
SN76104N	μA732PC	
SN76105N		μA732PC
SN76111N	μA767PC	
SN76115	μA1310	
SN76116N	μA758PC	
SN76131N	μA739PC	
SN76149N	μA749PC	
SN76227		TDA2522
SN76242N	μA780PC	
SN76243N	μA781PC	
SN76246N	μA746PC	
SN76298N		μA787PC
SN76545		TBA920
SN76565N	μA3064PC	
SN76591P	μA1391TC	
SN76594P	μA1394TC	
SN76600P		μA757PC
SN76635N	μA720PC	
SN76642N		μA2136PC
SN76650N		μA757PC
SN76666N	μA3065PC	
SN76669N	μA2136PC	
SN76675N	μA3075PC	
SN76678P	μA753TC	
SN76689N	μA3089PC	
SSS725AJ		μA725AHM
SSS725BJ		μA725EHM
SSS725EJ		μA725EHC
SSS741CJ		μA741EHC
SSS741J		μA741AHM
SSS747CK		μA747EHC
SSS747CP		μA747EDC
SSS747K		μA747AHM
SSS747P		μA747ADM
SSS1408A-6	μA0802C	
SSS1408A-7	μA0802B	
SSS1408A-8	μA0802A	
SSS1508A-8	μA0802	
S5558T	μA1558HM	
S5596K	μA796H	
S8T13F	μA8T13DM	
S8T14F	μA8T14DM	
S8T15F		9616DM
S8T16F		9627DM
TA7157	μA1310	
TAA630S	TAA630S	TDA2522
TBA396		TDA2560
TBA510	TBA510	
TBA520	TBA520	TDA2522
TBA530	TBA530	TDA2530
TBA540	TBA540	
TBA560C	TBA560C	TDA2560
TBA570		μA721PC

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Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
TBA641A12	TBA641A12	
TBA641B11	TBA641B11	
TBA800	TBA800	
TBA810AS	TBA810AS	
TBA810DS	TBA810DS	
TBA810DAS	TBA810DAS	
TBA810S	TBA810S	
TBA920	TBA920	
TBA920S	TBA920S	
TBA970	TBA970	
TBA990	TBA990	TDA2522
TCA600		μA7392
TCA610		μA7392
TCA900		μA7392
TCA910		μA7392
TCA940		μA783P4C
TDA1170	TDA1170	
TDA1270	TDA1270	
TDA1037		TDA2002
TDA1190	TDA1190	
TDA1190Z	TDA1190Z	
TDA1327		TDA2522
TDA2002	TDA2002	
TDA2002A	TDA2002A	
TDA2150		TDA2560
TDA2160		TDA2522
TDA2521	TDA2521	
TDA2522	TDA2522	
TDA2530	TDA2530	
TDA2560	TDA2560	
TDA2590	TDA2590	
TDA2610		TDA1190
TL081		μAF771C
TL081A		μAF771
TL810		μA710HM
TL811		μA711HM
ULN2001A	9665	
ULN2002A	9666	
ULN2003A	9667	
ULN2004A	9668	
ULN2111A		μA2136PC
ULN2113A		μA3065PC
ULN2114A	μA746PC	
ULN2114K	μA746HC	
ULN2120A	μA732PC	

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
ULN2121A		μA767PC
ULN2122A		μA732PC
ULN2124A	μA780PC	
ULN2126A	μA739PC	
ULN2127A	μA781PC	
ULN2128A	μA767PC	
ULN2129A		μA3075PC
ULN2136A	μA2136PC	
ULN2137A	μA720PC	
ULN2165A	μA3065PC	
ULN2209M	μA753TC	
ULN2210A		μA758PC
ULN2224A		μA788PC
ULN2228A		μA788PC
ULN2244A	μA758PC	
ULN2298A		μA787PC
ULX2262A	μA787PC	
ULX2264A	μA3064PC	
ULX2267A	μA3067PC	
ULX2289A	μA3089PC	
YKB2219	μA1310	
μA709CA	μA709PC	
μA709CT	μA709HC	
μA709Q	μA709FM	
μA709T	μA709HM	
μA710CA	μA710HC	
μA710CT	μA710HC	
μA710Q	μA710FM	
μA710T	μA710HM	
μA711CA	μA711PC	
μA711CK	μA711HC	
μA711K	μA711HM	
μA723CA	μA723PC	
μA723CL	μA723HC	
μA723L	μA723HM	
μA733A	μA733DM	
μA733CK	μA733HC	
μA733C1	μA733DC	
μA733K	μA733HM	
μA7330A	μA733PC	
μA7331	μA733DM	
μA740CT	μA740HC	
μA741CA	μA741PC	
μA741CT	μA741HC	
μA741CV	μA741TC	

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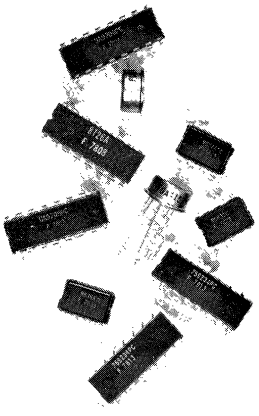
Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
μA741T	μA741HM	
μA747CA	μA747PC	
μA747CK	μA747HC	
μA747K	μA747HM	
μA748CA	μA748DC	
μA748CT	μA748HC	
μA748CV	μA748TC	
μA748T	μA748HC	
μA78L02ACLP	μA78L26AWC	
μA78L05ACLP	μA78L05AWC	
μA78L06ACLP	μA78L62AWC	
μA78L08ACLP	μA78L08AWC	
μA78L12ACLP	μA78L12AWC	
μA78L15ACLP	μA78L15AWC	
μA78M05CKC	μA78M05UC	
μA78M05CLA	μA78M05CHC	
μA78M05MLA	μA78M05HM	
μA78M06CKC	μA78M06UC	
μA78M06CLA	μA78M06CHC	
μA78M06MLA	μA78M06HM	
μA78M08CKC	μA78M08UC	
μA78M08CLA	μA78M08CHC	
μA78M08MLA	μA78M08HM	
μA78M12CKC	μA78M12UC	
μA78M12CLA	μA78M12CHC	
μA78M12MLA	μA78M12HM	
μA78M15CKC	μA78M15UC	
μA78M15CLA	μA78M15CHC	
μA78M15MLA	μA78M15HM	
μA78M20CKC	μA78M20CUC	
μA78M20CLA	μA78M20CHC	
μA78M20MLA	μA78M20HM	
μA78M24CKC	μA78M24CUC	
μA78M24CLA	μA78M24CHC	
μA78M24MLA	μA78M24HM	
μA7805CKA	μA7805KC	
μA7805CKC	μA7805UC	
μA7805MKA	μA7805KM	
μA7806CKA	μA7806KC	
μA7806CKC	μA7806UC	
μA7806MKA	μA7806KM	
μA7808CKA	μA7808KC	
μA7808CKC	μA7808UC	
μA7808MKA	μA7808KM	
μA7812CKA	μA7812KC	
μA7812CKC	μA7812UC	
μA7812MKA	μA7812KM	
μA7815CKA	μA7815KC	
μA7815CKC	μA7815UC	
μA7815MKA	μA7815KM	
μA7818CKC	μA7818UC	
μA7818MKA	μA7818KM	
μA7824CKC	μA7824UC	
μA7824MKA	μA7824KM	
μA7885CKA	μA7885KC	
μA7885CKC	μA7885UC	
μA7885MKA	μA7885KM	
μA79M05CKC	μA79M05AUC	
μA79M05CLA	μA79M05AHC	
μA79M05MLA	μA79M05HM	
μA79M06CKC	μA79M06AUC	
μA79M06CLA	μA79M06AHC	
μA79M06MLA	μA79M06HM	
μA79M08CKC	μA79M08AUC	
μA79M08CLA	μA79M08AHC	
μA79M08MLA	μA79M08HM	
μA79M12CKC	μA79M12AUC	
μA79M12CLA	μA79M12AHC	
μA79M12MLA	μA79M12HM	
μA79M15CLA	μA79M15AHC	
μA79M15MLA	μA79M15HM	
μA79M20CKC	μA79M20AUC	
μA79M20CLA	μA79M20AHC	
μA79M20MLA	μA79M20HM	
μA79M24CKC	μA79M24AUC	
μA79M24CLA	μA79M24AHC	
μA79M24MLA	μA79M24HM	
μA7905CKA	μA7905KC	
μA7905CKC	μA7905UC	
μA7905MKA	μA7905KM	
μA7906CKA	μA7906KC	
μA7906CKC	μA7906UC	
μA7906MKA	μA7906KM	
μA7908CKA	μA7908KC	
μA7908CKC	μA7908UC	
μA7908MKA	μA7908KM	
μA7912CKA	μA7912KC	
μA7912CKC	μA7912UC	
μA7912MKA	μA7912KM	
μA7915CKA	μA7915KC	

LINEAR INDUSTRY CROSS REFERENCE GUIDE

Part Number	Fairchild Direct Replacement	Fairchild Functional Equivalent
μA7915CKC	μA7915UC	
μA7915MKA	μA7915KM	
μA7918CKA	μA7918KC	
μA7918CKC	μA7918UC	
μA7918MKA	μA7918KM	
μA7924CKA	μA7924KC	
μA7924CKC	μA7924UC	
μA7924MKA	μA7924KM	



QUALITY, RELIABILITY AND HI REL PROCESSING

QUALITY, RELIABILITY AND HI REL PROCESSING

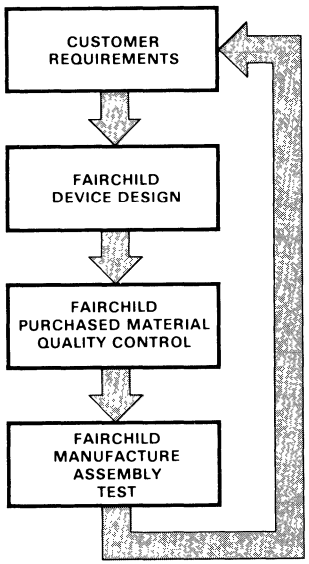
Introduction

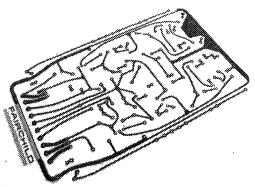
There are three basic ingredients in the manufacture of reliable Linear Circuits. First, the device must be designed with the user's applications and reliability requirements in mind. Secondly, the device must be manufactured with the optimum technology for the application. Thirdly, controls must be established to assure maintenance of the quality/reliability levels established in the design of the device. Consideration is given to the reliability influence of each part of the manufacturing and testing cycle with constant feedback from internal reliability monitoring; customer feedback on the results is a vital factor. The Fairchild reliability concept can be presented as constant feedback system which begins and ends with the customer *(Figure 3-1)*.

Areas of Consideration

Device Applications and Reliability

The reliability cycle begins with the customer. His device application, environment for its usage and end-product reliability requirements are major factors in establishing the quality/reliability levels. The customer is the final judge.





Customer Design Breadboard

Fig. 3-1 Customer Feedback System

Device Design

Inherent component reliability is a function of the product/process design. New Fairchild designs as well as modifications or extensions of existing designs with known performance and reliability characteristics are rigorously evaluated. Three different factors in the manufacture of an IC significantly affect its reliability.

The Silicon Chip — Fairchild's design-technology capability utilizes epitaxial layer to achieve the desired electrical parameter characteristics. The surface influences long-term gain and voltage/leakage stability. The metallization determines mechanical integrity and current distribution.

Chip Assembly — The process and materials used to assemble the chip and package must preserve the inherent reliability of the chip and be inherently reliable to withstand thermal, mechanical and electrical stresses.

The Package — The package must effectively transfer heat from the chip to the outside world and protect the chip during handling and use.

Incoming Quality Control (IQC)

All purchased materials for Fairchild Linear circuits are controlled through central specification control, product engineering, and reliability and quality assurance (R&QA) located in Mountain View. Materials are purchased and inspected per control documents using three IQC methods.

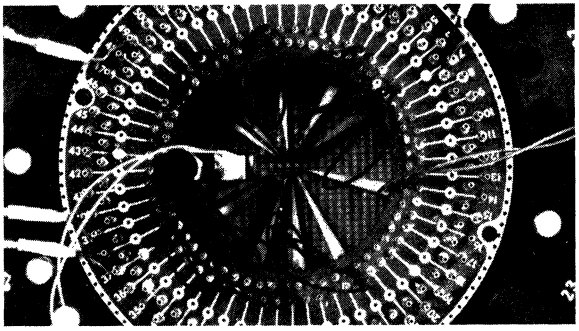
Direct visual and mechanical inspection
Functional testing
Composition analysis utilizing chemical and x-ray techniques from both internal and external sources.

In addition to centralized IQC, each manufacturing facility has a local, fully equipped IQC department. These facilities concentrate on cleanliness, plating quality and functionality. A computer file is made on each vendor's performance and quarterly reports are generated and analyzed.

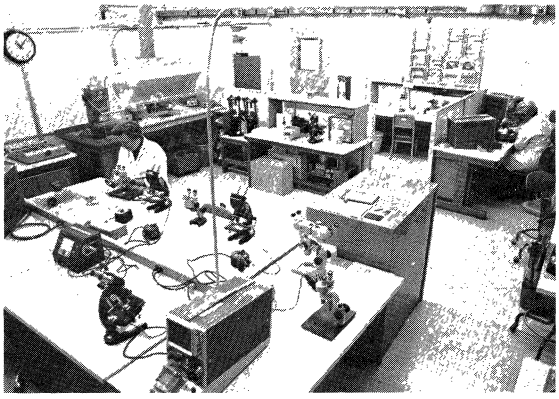
Wafer Manufacture

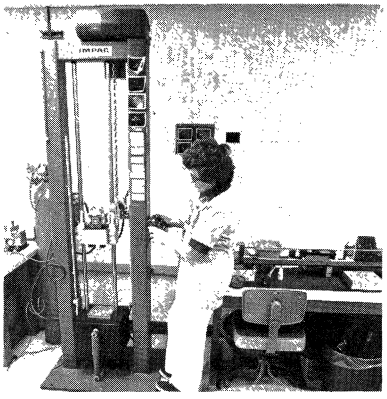
Wafers used to fabricate Fairchild Linear Circuits are made at Fairchild. This includes crystal pulling, slicing, polishing and epitaxial layer growth. Fairchild designs rely on accurate control of thickness and resistivity. All operations have laminar-flow clean-air hoods directly over the work areas. Wafer fabrication is essentially a series of masking and furnace cycles in which geometries are defined and impurities (dopants) introduced to form emitter, base and resistor regions. Daily controls are maintained on furnace temperatures to within ±1°C. Resistivities (ρ_S) of diffused layers are recorded on every run. Each masking step defines a new portion of the device geometry. A post develop inspection is performed to assure that each wafer has been properly exposed and chemically developed before final etching. When the masking and etching procedures are completed, a final inspection assures that the geometry is properly aligned, etched and cleaned. Following each production masking step, a sample inspection is performed by quality control inspectors to verify correct process implementation.

After masking and diffusion, the metallization process completes wafer manufacture. Fairchild uses electron-beam evaporation techniques to deposit gold and aluminum. Deposits are controlled through utilization of automated process sequencing,which includes an automatic thickness controller. Every run is gated through a first optical (1st opt.) inspection before it leaves the wafer fabrication area. Cleanliness, mask alignment, metal adherence (front and back) and general workmanship are inspected.

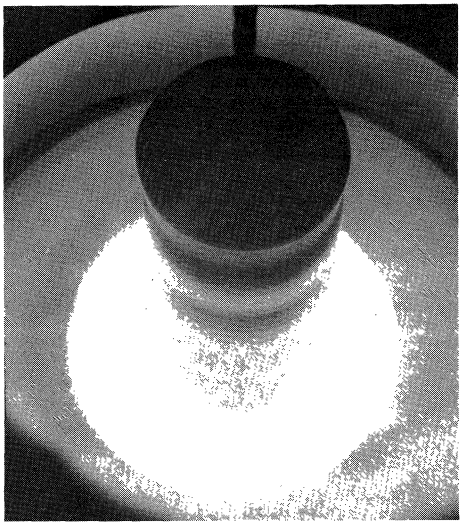


Wafer Probing





IQC Area



Crystal Puller

Wafer Testing
Before the wafers are scribed and broken into dice for assembly onto headers or shipment to a customer as probed dice, they are electrically sorted. Each wafer is automatically probed with multiple tests to duplicate or correlate the dice to the final product test requirements. Rejected dice are ink marked and later scrapped. A final quality control gate is performed before the probed wafers can be forwarded to assembly.

Device Assembly
After the wafers are scribed and broken, a second optical (2nd opt.) QC inspection is performed. The dice are inspected for wafer fabrication (handling) damage, as well as for defects which may cause assembly problems or result in latent reliability problems.

Monitors are performed on both assembly equipment and operators. Machines are shut down if defect control limits are exceeded and suspect material is rejected and 100% screened. Key items inspected are die orientation, voids under die, proper bond formation, wirepull strength and cleanliness.

A third optical (3rd opt.) gate is performed prior to final device sealing. If rejected, the lot is 100% screened by production and resubmitted to QC. Accepted lots are sent to the final seal operation, where the packages are monitored for weld strength and hermeticity (except plastic packages).

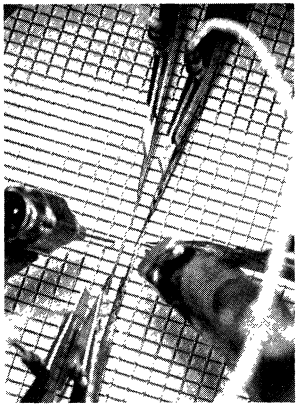
Device Testing
Before shipment, all devices are 100% production tested to the following minimum inspection levels.

Functional dc	0.25% AQL	
25° C dc	0.65% AQL	
25° C ac	1.5% AQL	
Temperature dc	1.5% AQL	
Mechanical/Visual	0.65% AQL	
Marking Performance	15/0 LTPD	
Fine Leak	1.0% AQL	Hermetic Devices Only.
Gross Leak	0.4% AQL	

Customers with special testing requirements are accommodated through an internal specification system. All internal test specifications formatted from customer documents are signed off by QA before they can be issued to the test area.

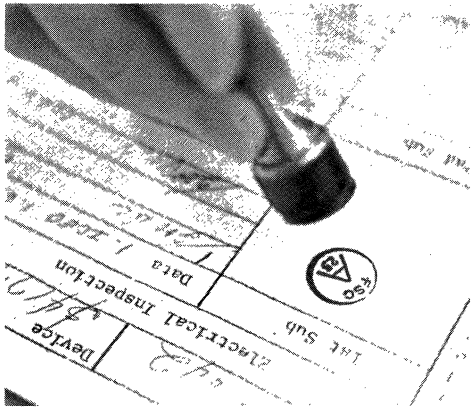
Device Application
The total reliability effort is completed full-cycle with the customer. Operation in the customer application is the final consideration in device reliability. How each device is handled during system assembly by the customer, heat-sunk (mounted) and cooled during operation, and the amount of overload stresses (due to the system malfunction or misuse) greatly impacts the device reliability. Thus, the customer's specification requirements, the manufacturer's device design, manufacture, test, the actual circuit into which the device is inserted and the equipment containing that circuit in the field all affect the device and reliability.

Failure Analysis
Failure analysis results performed by customers and by Fairchild on returned devices provide one of the most important inputs for consideration in Fairchild's total linear reliability concept. Failures generated by line monitors, life tests and field applications are analyzed to provide corrective action in terms of product design, assembly and testing methods. A scanning electron microscope (SEM) and an Auger electron microscope for chemical analysis are available for inspection of materials.



Die Probing

Device Testing



IQC Sign-off

Failure Analysis

Reliability Monitor and Control

Line Monitors

Line monitors are used to monitor the production line on a weekly basis. These monitors are designed to provide a constant feedback on product reliability. The following assembly/test monitors are conducted on a routine basis.

Assembly	Test
Package integrity	High-temperature reverse bias
Lead integrity	Intermittent operating life (power cycling)
Die integrity	High-temperature storage
Die-attach integrity	Temperature cycling
Bond integrity	Thermal shock
	Autoclave*
	85% R.H./85° C biased*

*Applied to plastic devices only.

Extended Reliability Tests

In conjunction with the weekly line-monitor program, Fairchild employs an extended reliability test program which is designed to reflect the long-term stability of Fairchild's Linear products. A summary of these reliability tests is shown in *Table 3-1*.

Quality and Reliability Data

Supplemental brochures are published on an annual basis which provide detailed failure rate data. Please contact Fairchild Sales Offices for additional reliability and quality information.

EXTENDED RELIABILITY TESTS	METAL CAN	PLASTIC
High Temperature Operating Life T_A = 150° C Readouts at 0, 168, 500, 1000 Hours	X	X
Temperature Cycling -65° C to +150° C (MIL-STD-883, Method 1010.1, Cond. C) Readouts at 0, 10, 100 Cycles Hermeticity (1×10^{-7} - TO-5, 1×10^{-6} - TO-3)	X	
Constant Acceleration F = 20K g 1 Min. Ea. 6 Axis (MIL-STD-883, Method 2001)	X	
Impact Shock 1500 g x 5 Blows (MIL-STD-883, Method 2002)	X	
Vibration, Variable Frequency 10 g (MIL-STD-883, Method 2007)	X	
Biased Humidity T_A = 85° C, RH = 85% Readouts at 0, 168, 500, 1000 Hours		X
Thermal Shock -55° C to +125° C Readouts at 0, 10, 100 Cycles MIL-STD-883, Method 1011, Condition C	X	X
Autoclave T_A = 125° C ± 2° C 15 PSI, 24 Hours		X

Table 3-1 Reliability Test Summary

HI REL PROCESSING — MIL-M-38510/MIL STD-883

A unique "company", within Fairchild Linear, is totally dedicated to the processing of high reliability products and to serving the special needs of the HI REL community. It consists of marketing, engineering, production control, manufacturing and quality assurance. Fairchild's HI REL processing facilities are among the most modern and sophisticated in the semiconductor industry. Screening procedures are set up to conform to the most recent version of MIL-STD-883, in conjunction with MIL-M-38510, which establishes standardized requirements for design, material, performance, control and documentation needed to achieve prescribed levels of device quality and reliability.

HI REL Unique II Program

Fairchild's Unique II program fills a longstanding need for a definite and comprehensive program covering HI REL semiconductor products...a program offering users a selection among multi-level screening flows and reliability requirements...a program providing clear and precise definitions on all areas of contractual performance...a program designed to reduce the high costs and delivery delays normally associated with HI REL. The objectives and benefits of the Unique II program for integrated circuits are these:

- Offers a full spectrum of processing options, including full compliance JAN and 883 Classes S, B, and C.
- Offers full compliance with JAN MIL-M-38510 and emphasizes the importance of this program.
- Accommodates the special needs of users' source control and specification control drawings.
- Offers models to aid users in development of source control drawings.
- Takes the mystery out of in-house processing to MIL-STD-883 and to MIL-M-38510 detail specifications. The Unique II program is definitive as to the similarities and differences in these requirements.
- Provides users with alternatives that may be used when JAN slash sheets or QPLs are unavailable, or for programs that demand the highest level of quality and reliability.

Fairchild offers a complete processing capability to fulfill requirements ranging from the least demanding to the most complex, including the following:

- Scanning Electron Microscope (SEM) Inspection
- Level A Visual
- Bond Pull and Die Shear Testing
- Read and Record and Δ Drift Parameters
- Particle Impact Noise Detection (Pin-D) Testing
- Group A, B, C and D Qualification Testing.

Standard Unique II processing flows are given on the following pages; special flows will be quoted on an individual basis.

MATRIX VI — COMMERCIAL AND INDUSTRIAL RELIABILITY PROGRAM

Commercial and industrial users increasingly demand optimized quality and reliability for the semiconductor integrated circuits purchased for their systems. Specific factors — increased integrated circuit usage per board, high costs for receiving inspection, pc board and systems repair, and the frequently immeasurable cost associated with field failures — require the user to attain high quality and reliability coupled with total cost. Matrix VI is designed to meet these user requirements.

Fairchild's Matrix VI Program offers a broad spectrum of screens and high technology/high volume integrated circuit products to meet the user's quality and reliability requirements typically associated with the commercial and industrial marketplace. There are two screening options for each package type, each with a separate degree of reliability and cost level. To simplify a cost-effective analysis, reliability factors have been assigned to each screening level. (See following pages.)

It is the goal of Matrix VI to achieve the highest possible reliability consistent with the user's needs and to avoid "over-buying". Cost-effective reliability is the essence of Matrix VI, the most comprehensive program of its kind now offered to the industrial/commercial marketplace.

JAN PART NUMBERING SYSTEM

J M 38510/ 101 01 B G C

JAN DESIGNATOR

Cannot be marked with "J" unless qualified on Part I or Part II of QLP-38510

General Procurement Spec.

REFERS TO DETAIL SPEC

101 Op Amps
102 Voltage Regulators
103 Comparators
104 Interface
105 733
106 Voltage Followers
107 3-Terminal Voltage Regulators
108 Transistor Arrays
109 Timers
110 Quad Op Amps

Defines Device Type

PROCESSING LEVEL

S
B
C

PACKAGE TYPE

A 14-pin $^1/_4$ x $^1/_4$ Flatpak
B 14-pin $^1/_4$ x $^1/_8$ Flatpak
C 14-pin $^1/_4$ x $^3/_4$ DIP
D 14-pin $^1/_4$ x $^3/_8$ Flatpak
E 16-pin $^1/_4$ x $^3/_4$ DIP
F 16-pin $^1/_4$ x $^3/_8$ Flatpak
G 8-pin Can
H 10-pin $^1/_4$ x $^1/_4$ Flatpak
I 10-pin Can
J 24-pin $^1/_2$ x $1^1/_4$ DIP
K 24-pin $^3/_8$ x $^1/_2$ Flatpak
L 24-pin $^3/_8$ x $^1/_2$ Flatpak
X 3-pin TO-5 Can
Y 2-pin TO-3 Can
Z 24-pin $^1/_4$ x $^3/_8$ Flatpak

LEAD FINISH

A Hot Solder DIP
B Tin Plate
C Gold Plate
X Any of the above

LINEAR JAN GENERIC PART NUMBERS – EXAMPLES

JM38510/	01	02	03	04	05	06	07	08	09	10
101	741	747	101A	108A	2101	2108	118			
102	723									
103	710	711	106	111	2111					
104	55107	55108	9614	9615	55113	7831	7832	7820	7830	
105	733									
106	102	110	2110							
107	109	78M05	78M12	78M15	78M24	7805	7812	7815	7824	
108	3018	3045								
109	555	556								
110	148	149	4741	4136	124					

Note: Dated material. Please contact Fairchild for latest revisions.

HI REL PROCESS SCREENING REQUIREMENTS

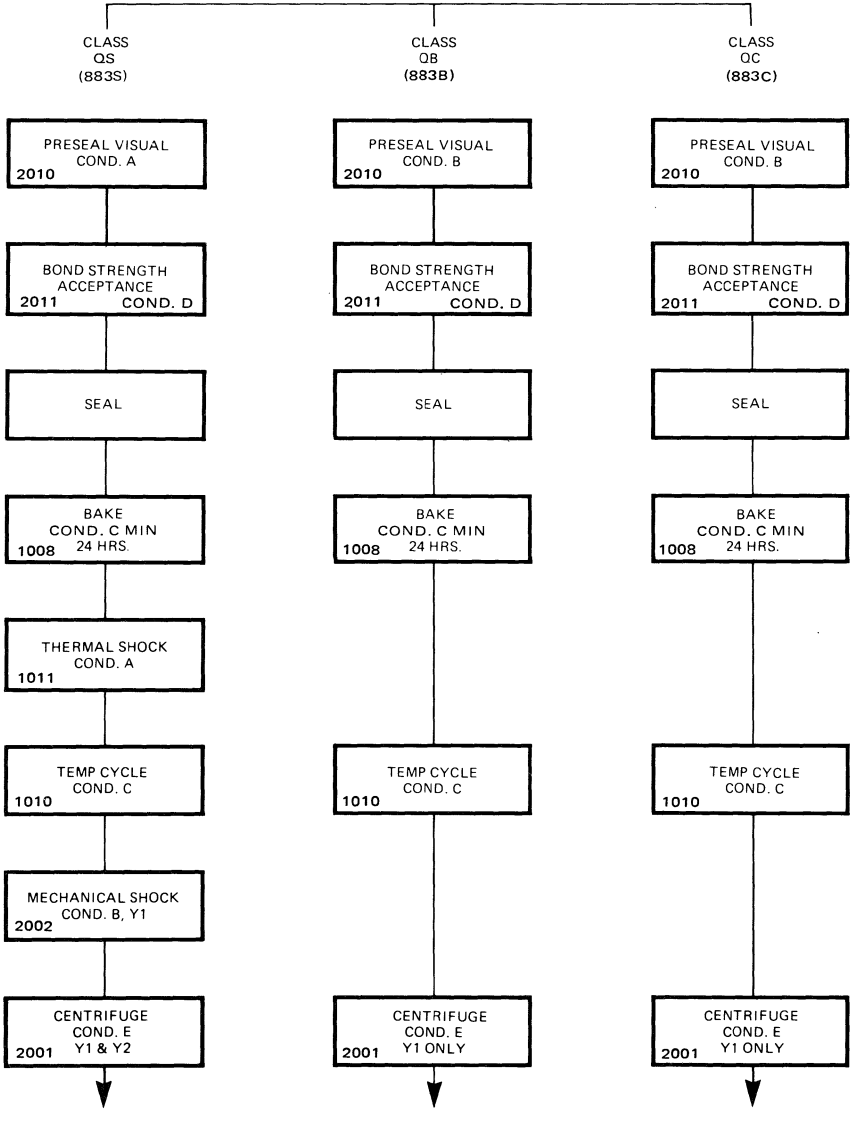
MIL-STD-883B TEST METHODS	DESCRIPTION	JAN M38510 CLASS B	JAN M38510 CLASS C
Preseal Visual MTD. 2010	Cond. A Maximum Visual Criteria Cond. B. Optimum Visual Criteria	PRESEAL VISUAL COND. B	PRESEAL VISUAL COND. B
Bond Strength MTD 2011	Bond strength is monitored on a sample basis three times per shift per machine	BOND STRENGTH COND. D	BOND STRENGTH COND. D
Seal	Devices are hermetically sealed for compliance to MIL-STD-883 requirements	SEAL	SEAL
High Temp Storage MTD 1008	Cond. C Tstg = 150°C	BAKE COND. C MIN 24 HRS.	BAKE COND. C MIN 24 HRS.
Temperature Cycle MTD 1010	Cond. C −65°/150°C 10 cycles	TEMP CYCLE COND. C	TEMP CYCLE COND. C
Constant Acceleration MTD 2001 (Note1)	Cond E 30000 G's X_1, X_2, Y_1, Y_2	CENTRIFUGE COND. E Y_1 ONLY	CENTRIFUGE COND. E Y_1 ONLY
Hermetic Seal MTD 1014 (Note 1)	Cond A Fine-Helium $5x10^{-8}$ cc/sec Cond B Fine-Radiflo $5x10^{-8}$ cc/sec Cond C Gross-FC43/Hot 10^{-3} cc/sec or Gross-FC78/Vacuum 10^{-5} cc/sec	HERMETICITY COND. A/B COND. C	HERMETICITY COND. A/B COND. C
Pre Burn-in Electrical MTD 5004	25°C dc electrical testing to remove rejects prior to submission to burn-in screen	PRE B/I ELECT 25°C dc	
Burn-in Screen MTD 1015	Cond A, Cond B, Cond C Cond D, Cond E, Cond F	BURN IN* 160 HRS 125°C	
Post Burn-in Electrical MTD 5004	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include 25°C dc, 125°C dc, −55°C dc, 25°C dc, 25°C ac and 25°C Functional tests.	PST B/I ELECT 25°C dc +125°C dc −55°C dc 25°C ac 10% PDA	ELECTRICAL 25°C dc 25°C FUNCTIONAL
Quality Conformance Inspection MTD 5005	Group A Electrical Characteristics Group B Package oriented Tests Group C: Life Tests Group D: Environmental Tests	QUALITY CONFORMANCE Gp A, B, C and D	QUALITY CONFORMANCE Gp A, B, C and D
External Visual MTD 2009	3X, 10X magnification: Verify dimensions, configuration, lead structure, marking and workmanship	EXTERNAL VISUAL 100%	EXTERNAL VISUAL 100%
RELIABILITY	Figure of Merit	15	2
ORDERING	Part Number	JM38510/ 10101BCB	JM38510/ 10101CCB
	Part Marking	JM38510/ 10101BCB	JM38510/ 10101CCB

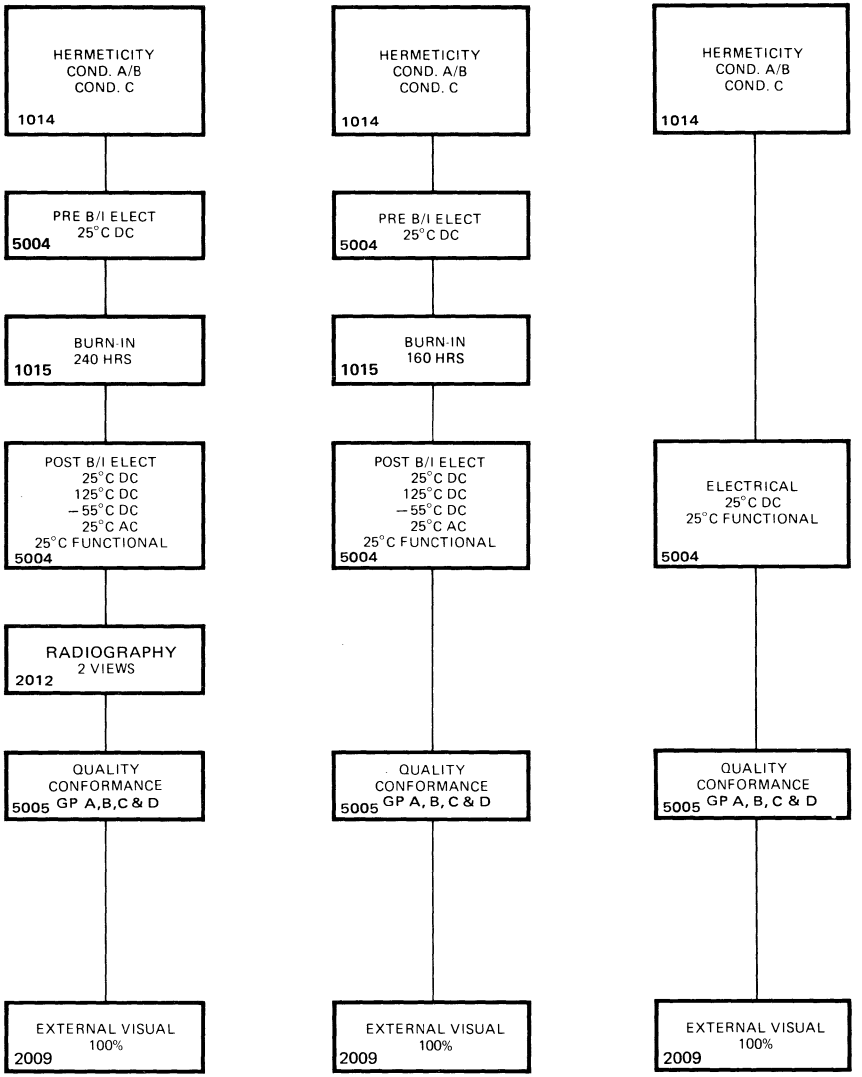
NOTE: RELIABILITY Figure of Merit is the Reliability Improvement Factor from RADC Reliability Notebook, Vol. II, RADC-TR-67-108, Table XII-6, page 419.

1. Not Applicable for T0-3 Cans

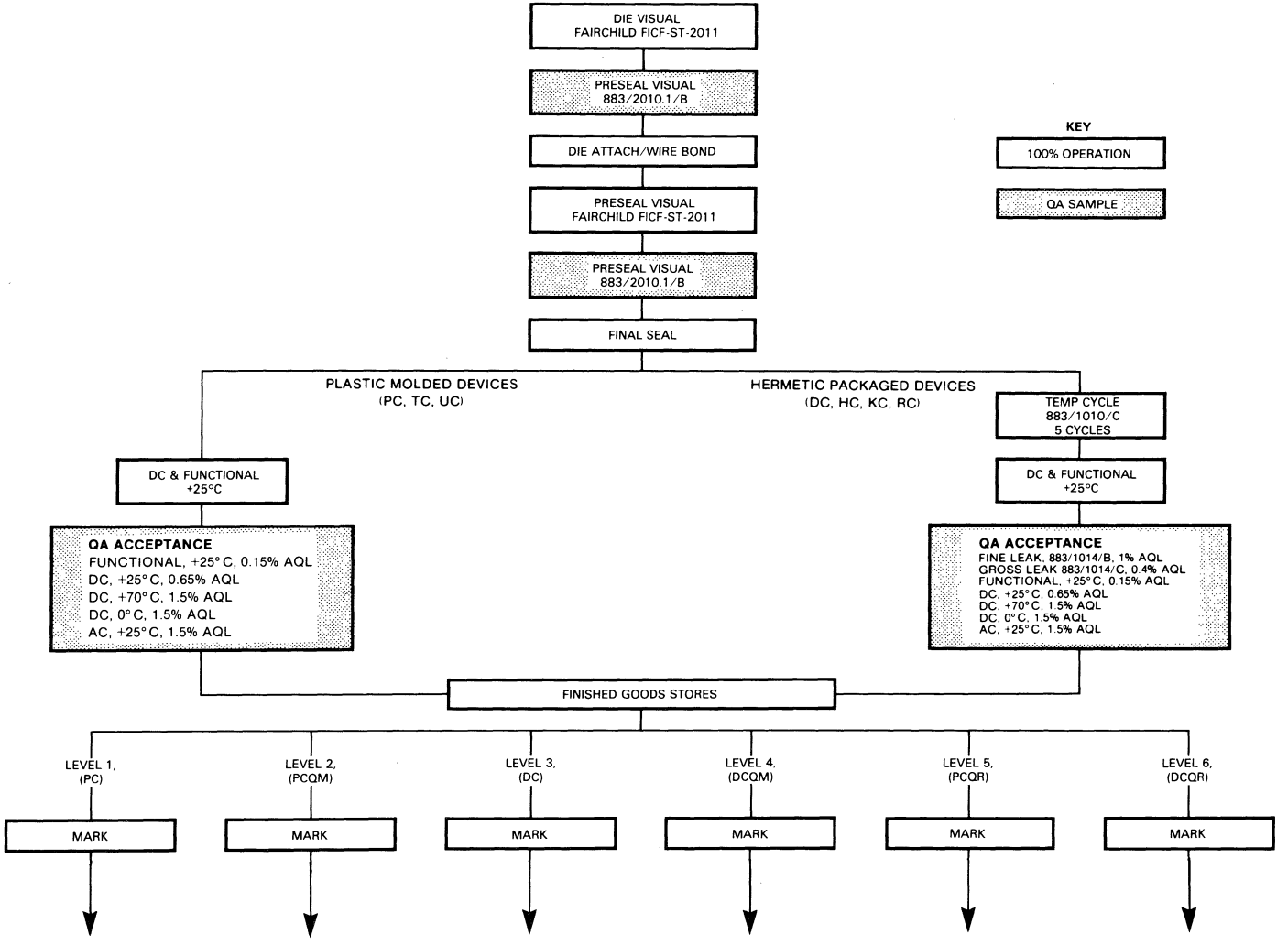
*Time Temperature Curve (method 1015) may be used.

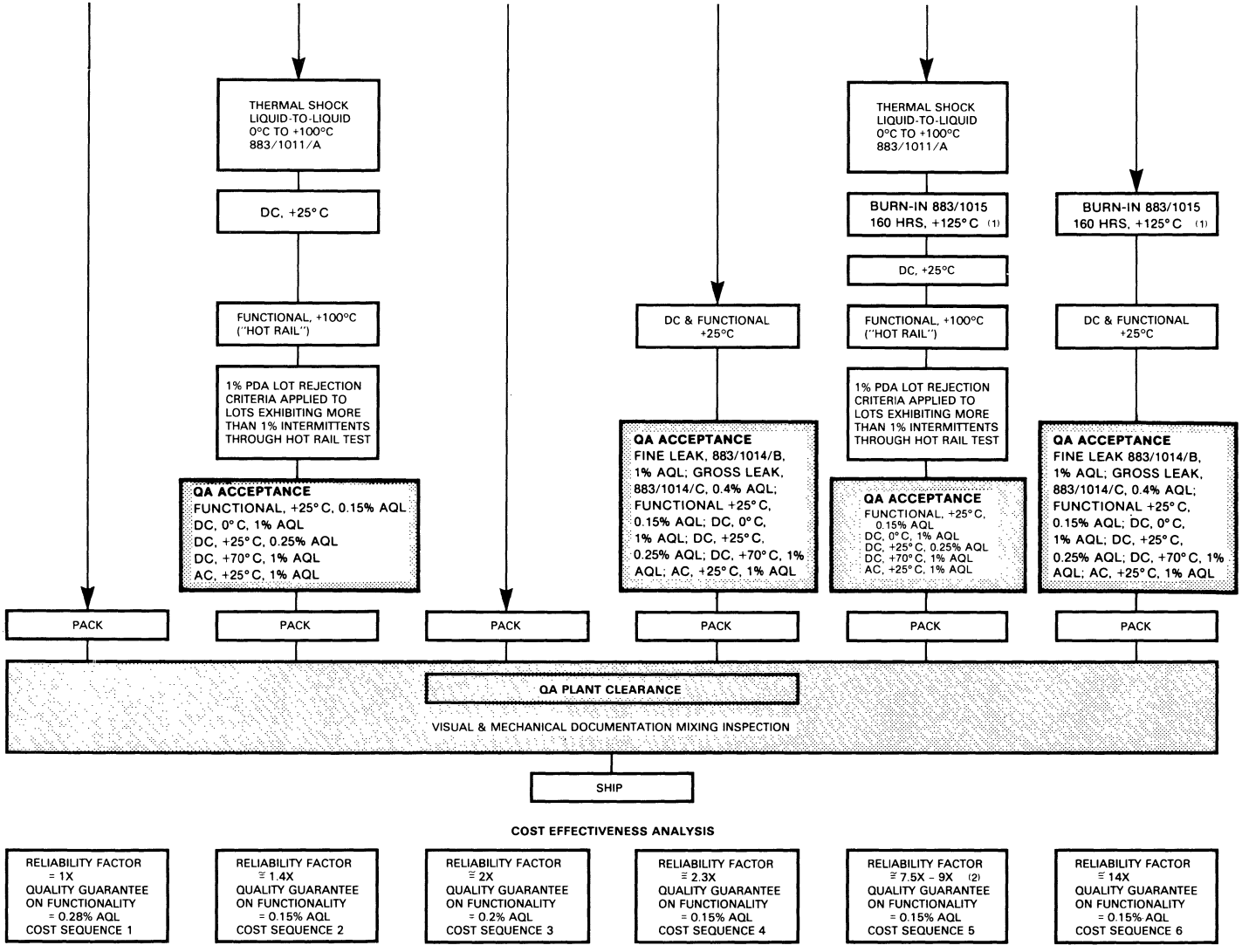
UNIQUE II


CLASS QS (883S)
CLASS QB (883B)
CLASS QC (883C)
PRESEAL VISUAL COND. A 2010
PRESEAL VISUAL COND. B 2010
PRESEAL VISUAL COND. B 2010
BOND STRENGTH ACCEPTANCE 2011 COND. D
BOND STRENGTH ACCEPTANCE 2011 COND. D
BOND STRENGTH ACCEPTANCE 2011 COND. D
SEAL
SEAL
SEAL
BAKE COND. C MIN 1008 24 HRS.
BAKE COND. C MIN 1008 24 HRS.
BAKE COND. C MIN 1008 24 HRS.
THERMAL SHOCK COND. A 1011
TEMP CYCLE COND. C 1010
TEMP CYCLE COND. C 1010
TEMP CYCLE COND. C 1010
MECHANICAL SHOCK COND. B, Y1 2002
CENTRIFUGE COND. E 2001 Y1 & Y2
CENTRIFUGE COND. E 2001 Y1 ONLY
CENTRIFUGE COND. E 2001 Y1 ONLY


HERMETICITY
COND. A/B
COND. C
1014
PRE B/I ELECT
25°C DC
5004
BURN-IN
240 HRS
1015
POST B/I ELECT
25°C DC
125°C DC
−55°C DC
25°C AC
25°C FUNCTIONAL
5004
RADIOGRAPHY
2 VIEWS
2012
QUALITY
CONFORMANCE
5005 GP A,B,C & D
EXTERNAL VISUAL
100%
2009
μA741 DMQS
HERMETICITY
COND. A/B
COND. C
1014
PRE B/I ELECT
25°C DC
5004
BURN-IN
160 HRS
1015
POST B/I ELECT
25°C DC
125°C DC
−55°C DC
25°C AC
25°C FUNCTIONAL
5004
QUALITY
CONFORMANCE
5005 GP A, B, C & D
EXTERNAL VISUAL
100%
2009
μA741 DMQB
HERMETICITY
COND. A/B
COND. C
1014
ELECTRICAL
25°C DC
25°C FUNCTIONAL
5004
QUALITY
CONFORMANCE
5005 GP A, B, C & D
EXTERNAL VISUAL
100%
2009
μA741 DMQC

MATRIX VI PROCESS FLOW OPTIONS & COST EFFECTIVENESS





NOTE:
(1) Temperature Accelerated Testing may be used for MIL-STD-883 method 1015 Test Condition F.
(2) Burn-In has the same relative effectiveness for plastic molded devices as for ceramic/hermetic packaged devices. Assuming a controlled (air conditioned and constant power) field application/environment, the reliability factor would be approximately 9x. But should the field application be in a less controlled and power on/off application, the reliability would be approximately 7.5X.

VOLTAGE COMPARATORS

μAF111 • μAF311

FET INPUT VOLTAGE COMPARATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

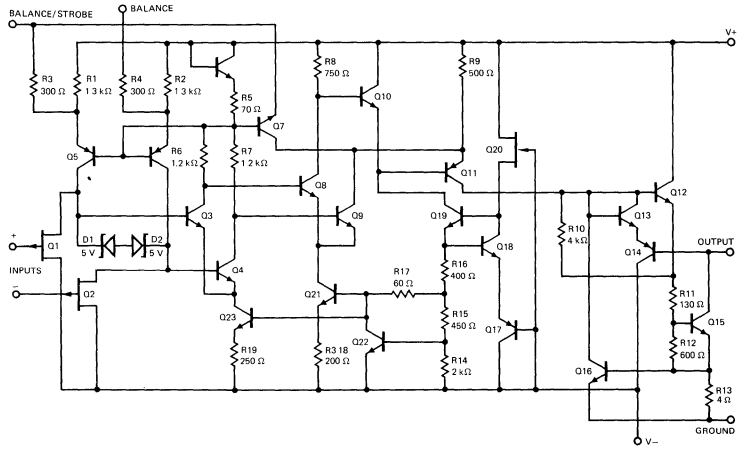
GENERAL DESCRIPTION – The μAF111 and μAF311 are monolithic, FET input Voltage Comparators, constructed using the Fairchild Planar* epitaxial process. The μAF111 series operates from the single 5 V integraetd circuit logic supply to the standard ±15 V operational amplifier supplies. The μAF111 series is intended for a wide range of applications including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.

- **EXTREMELY LOW INPUT BIAS CURRENT** . . . 50 pA MAX (μAF111), 150 pA MAX (μAF311)
- **EXTREMELY LOW INPUT OFFSET CURRENT** . . . 25 pA MAX (μAF111), 75 pA MAX (μAF311)
- **DIFFERENTIAL INPUT VOLTAGE** . . . ±30 V
- **POWER SUPPLY VOLTAGE SINGLE 5.0 V SUPPLY TO ±15 V**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **STROBE CAPABILITY**

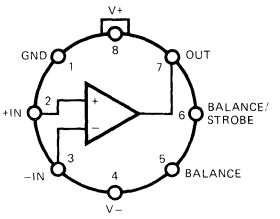
ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	36 V
Output to V– (μAF111)	50 V
(μAF311)	40 V
Ground to V–	30 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 s
Storage Temperature Range (Metal Can)	
Metal Can	–65°C to +150°C
Hermetic DIP	–55°C to +125°C
Operating Temperature Range	
Military (μAF111)	–55°C to +125°C
Commercial (μAF311)	0°C to +70°C
Pin Temperature	
Metal Can, Hermetic DIP (Soldering, 60 s)	300°C

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

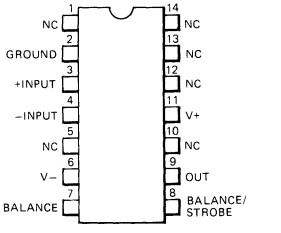


ORDER INFORMATION

TYPE	PART NO.
μAF111	μAF111HM
μAF311	μAF311HC

NOTE: Pin 4 connected to case.

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μAF111	μAF111DM
μAF311	μAF311DC

μAF111

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = -55°C$ to $+125°C$ unless otherwise specified, Note 3.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50$ kΩ		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	25	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		20	50	pA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35$ V $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50$ kΩ			6.0	mV
Input Offset Current (Note 4)	$V_S = \pm 15$ V, $V_{CM} = 0$ (Note 6)		2.0	3.0	nA
Input Bias Current	$V_S = \pm 15$ V, $V_{CM} = 0$ (Note 6)		5.0	7.0	nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq 4.5$ V, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35$ V		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

μAF311

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 0°C$ to $+70°C$ unless otherwise specified, Note 3.

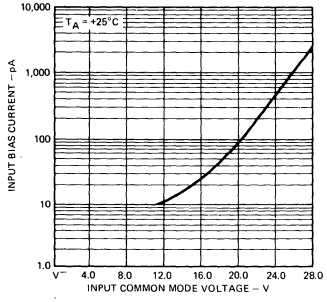
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50$ kΩ		2.0	10	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	75	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		25	150	pA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35$ V $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50$ kΩ			15	mV
Input Offset Current (Note 4)	$V_S = \pm 15$V, $V_{CM} = 0$ (Note 6)		1.0		nA
Input Bias Current	$V_S = \pm 15$ V, $V_{CM} = 0$ (Note 6)		3.0		nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq 4.5$ V, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

NOTES:

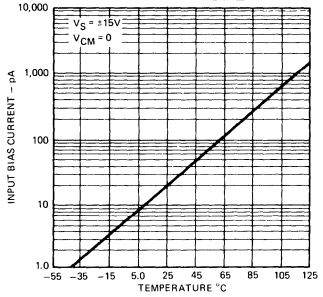
1. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can; 8.3 mW/°C for mini DIP.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5 V supply up to ±15 V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.
6. For input voltages greater than 15 V above the negative supply the bias and offset currents will increase – see typical performance curves.

TYPICAL PERFORMANCE CURVES

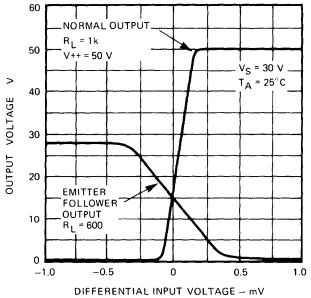
INPUT BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



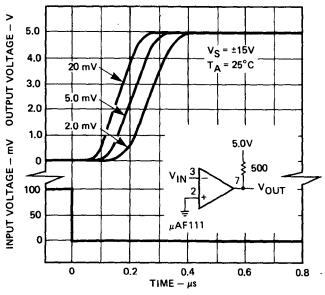
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



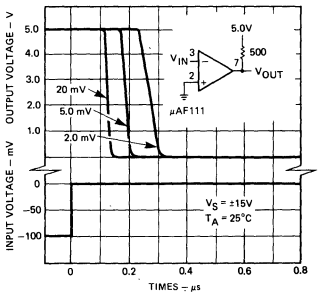
TRANSFER FUNCTION



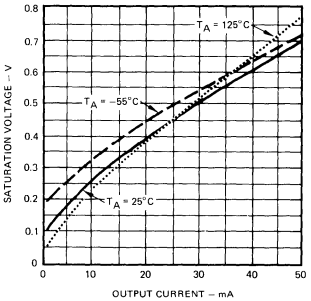
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



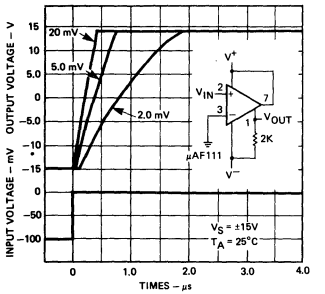
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



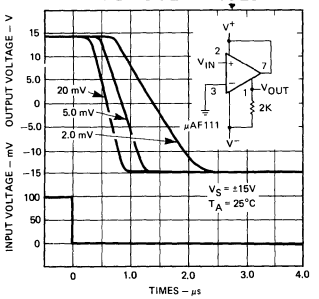
OUTPUT SATURATION VOLTAGE



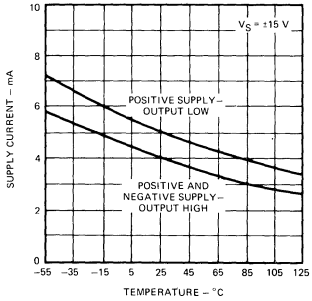
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



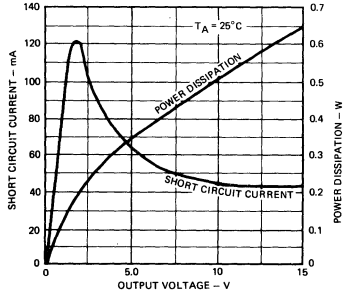
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



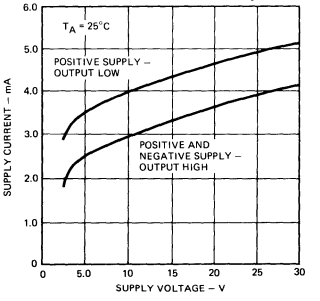
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



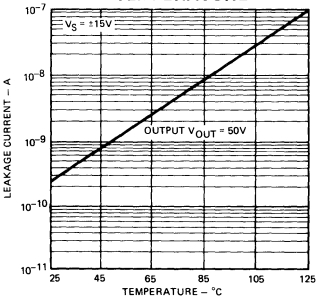
OUTPUT LIMITING CHARACTERISTICS



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



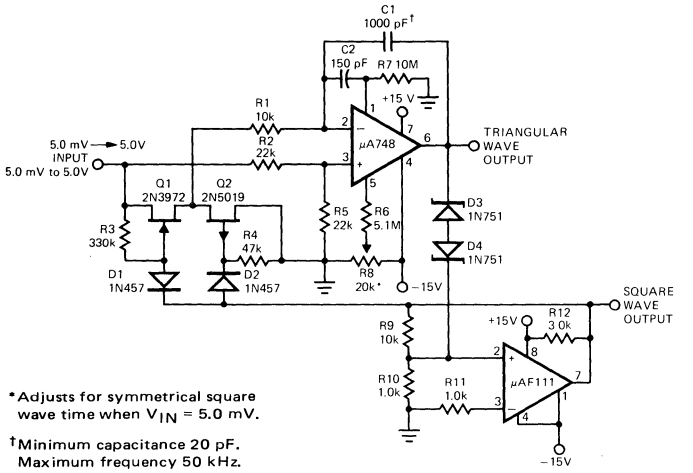
OUTPUT LEAKAGE CURRENT AS A FUNCTION OF TEMPERATURE



4

TYPICAL APPLICATIONS

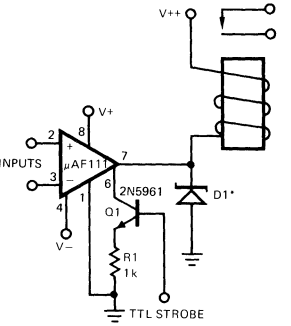
10 Hz TO 10 kHz VOLTAGE CONTROLLED OSCILLATOR



*Adjusts for symmetrical square wave time when V_{IN} = 5.0 mV.

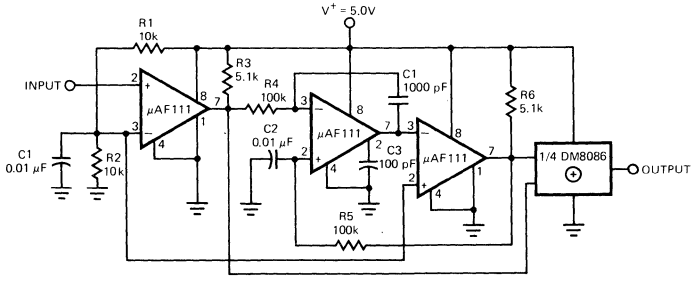
†Minimum capacitance 20 pF. Maximum frequency 50 kHz.

RELAY DRIVER WITH STROBE



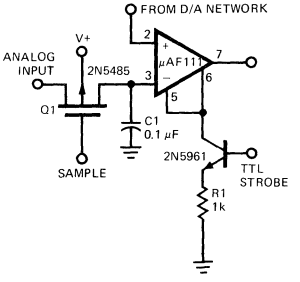
*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

FREQUENCY DOUBLER



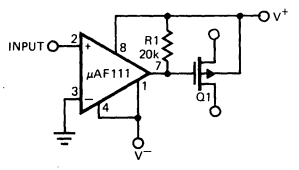
Frequency range:
Input — 5.0 kHz to 50 kHz
Output — 10 kHz to 100 kHz

STROBING OFF BOTH INPUT* AND OUTPUT STAGES

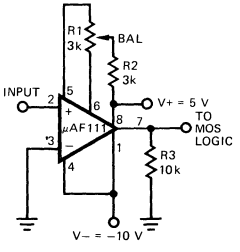


*Typical input current is 50 pA with inputs strobed off.

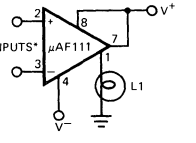
ZERO CROSSING DETECTOR DRIVING MOS SWITCH



ZERO CROSSING DETECTOR DRIVING MOS LOGIC



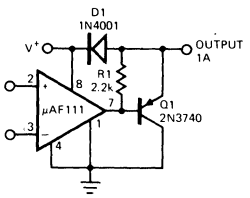
DRIVING GROUND-REFERRED LOAD



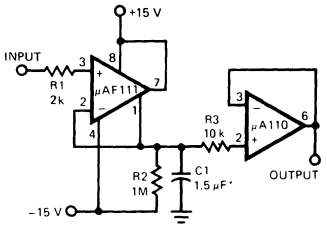
*Input polarity is reversed when using pin 1 as output.

TYPICAL APPLICATIONS (Cont'd)

COMPARATOR AND SOLENOID DRIVER

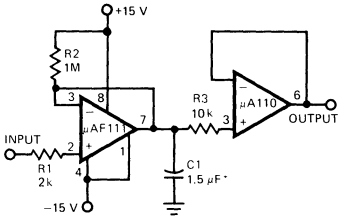


POSITIVE PEAK DETECTOR



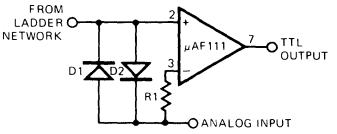
*Solid tantalum

NEGATIVE PEAK DETECTOR

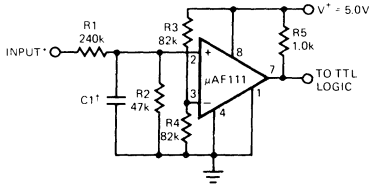


*Solid tantalum

USING CLAMP DIODES TO IMPROVE RESPONSE



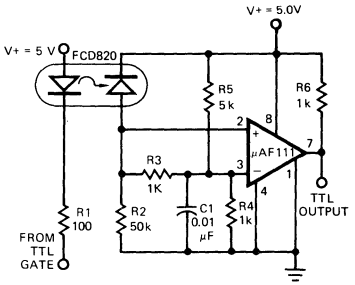
TTL INTERFACE WITH HIGH LEVEL LOGIC



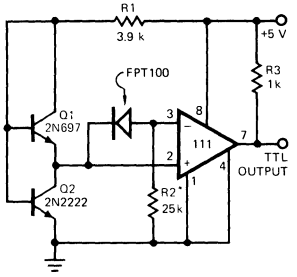
*Values shown are for a 0 to 30 V logic swing and a 15 V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

DIGITAL TRANSMISSION ISOLATOR



PRECISION PHOTODIODE COMPARATOR



*R2 sets the comparison level. At comparison, the photodiode has less than 5.0 mV across it, decreasing leakages by an order of magnitude.

DEFINITIONS:

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT – The change in input offset current over the operating temperature range divided by the operating temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE – The change in input offset voltage over the operating temperature range divided by the operating temperature range.

DIFFERENTIAL INPUT VOLTAGE RANGE – The range of voltage applied between the input terminals for which operation within specifications is assured.

INPUT BIAS CURRENT – The average of the two input currents with no signal applied.

INPUT COMMON MODE VOLTAGE RANGE – The range of common mode input voltage over the device will operate within specifications.

INPUT OFFSET CURRENT – The difference between the two input currents with the output at the logic threshold voltage.

INPUT OFFSET VOLTAGE – The voltage which must be applied to the input terminals to give the logic threshold voltage at the output.

INPUT VOLTAGE RANGE – The range of voltage on either input terminal over which the device will operate as specified.

NEGATIVE OUTPUT VOLTAGE LEVEL – The dc output voltage in the negative direction with the input voltage equal to, or greater than, a minimum specified value.

RESPONSE TIME – The interval between the application of an input step function and the time when the output voltage crosses the logic threshold level.

STROBE CURRENT – The maximum current taken by the strobe terminal during activation.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the dc output in the vicinity of the logic threshold.

μA111 • μA311

VOLTAGE COMPARATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

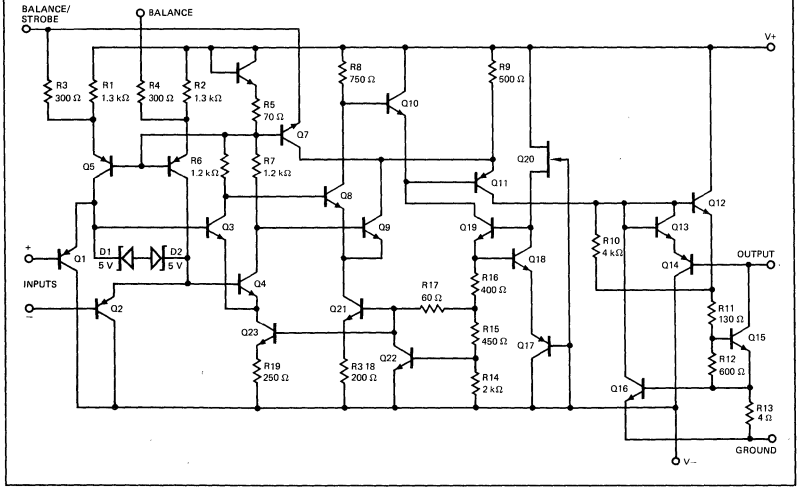
GENERAL DESCRIPTION – the μA111 and μA311 are monolithic, low input current Voltage Comparators, each constructed using the Fairchild Planar* epitaxial process. The μA111 series operates from the single 5 V integrated circuit logic supply to the standard ±15 V operational amplifier supplies. The μA111 series is intended for a wide range of applicatons including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.

- **LOW INPUT BIAS CURRENT – 150 nA MAX (111), 250 nA MAX (311)**
- **LOW INPUT OFFSET CURRENT – 20 nA MAX (111), 50 nA MAX (311)**
- **DIFFERENTIAL INPUT VOLTAGE – ±30 V**
- **POWER SUPPLY VOLTAGE SINGLE 5.0 V SUPPLY TO ±15 V**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **STROBE CAPABILITY**

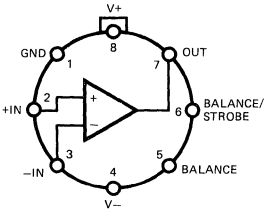
ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	36 V
Output to V– (μA111)	50 V
(μA311)	40 V
Ground to V–	30 V
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Internal Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 s
Storage Temperature Range (Metal Can and Hermetic Mini DIP)	–65°C to +150°C
(Molded Mini DIP)	–55°C to +125°C
Operating Temperature Range	
Military (μA111)	–55°C to +125°C
Commercial (μA311)	0°C to +70°C

EQUIVALENT CIRCUIT



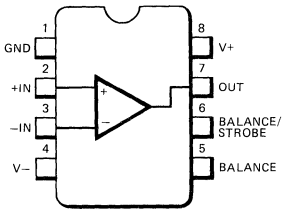
CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA111	μA111HM
μA311	μA311HC

8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
μA111	μA111RM
μA311	μA311RC
μA311	μA311TC

*Planar is a patented Fairchild process

μA111

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = -55°C$ to $+125°C$ unless otherwise specified, Note 3.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50\ k\Omega$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA				
	$T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35$ V				
	$T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50\ k\Omega$			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq 4.5$ V, $V^- = 0$				
	$V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35$ V		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

μA311

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V, $T_A = 0°C$ to $+70°C$ unless otherwise specified, Note 3.

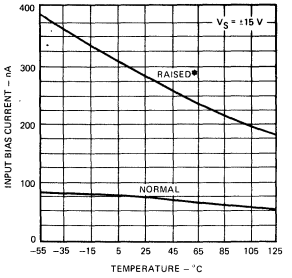
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50\ k\Omega$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA				
	$T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35$ V				
	$T_A = 25°C$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50\ k\Omega$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq 4.5$ V, $V^- = 0$				
	$V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

NOTES:

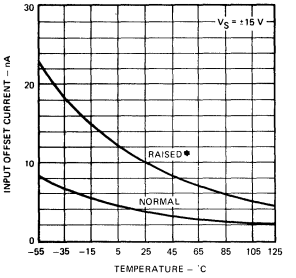
1. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can; 8.3 mW/°C for mini DIP.
3. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5 V supply up to ±15 V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

TYPICAL PERFORMANCE CURVES FOR μA111

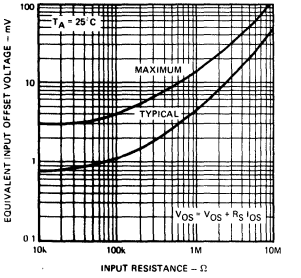
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE

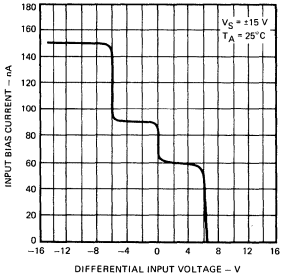


OFFSET VOLTAGE AS A FUNCTION OF INPUT RESISTANCE

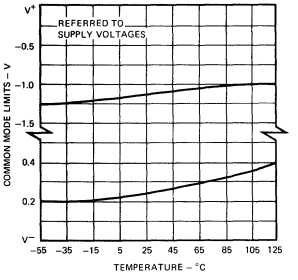


*Pins 5,6 and 8 are shorted.

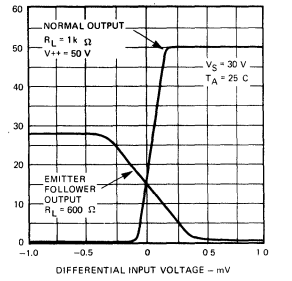
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



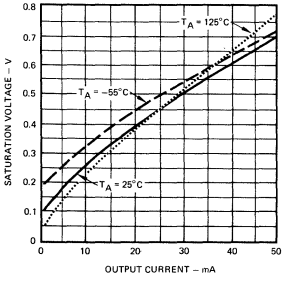
COMMON MODE LIMITS AS A FUNCTION OF TEMPERATURE



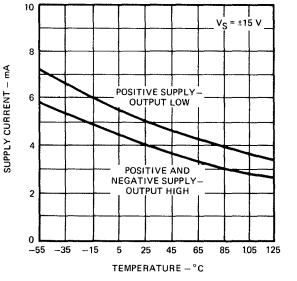
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



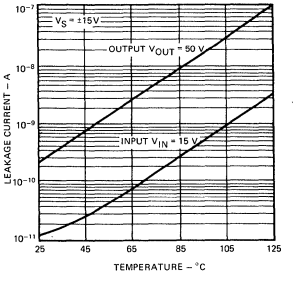
OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

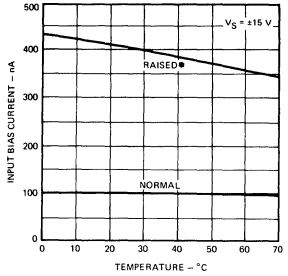


LEAKAGE CURRENTS AS A FUNCTION OF TEMPERATURE

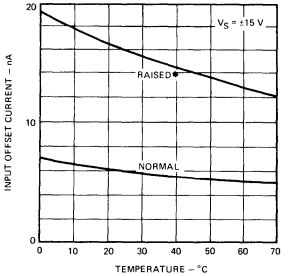


TYPICAL PERFORMANCE CURVES FOR μA311

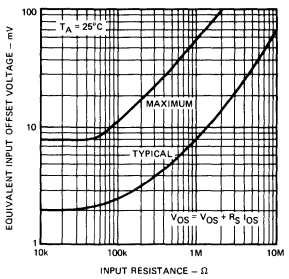
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE

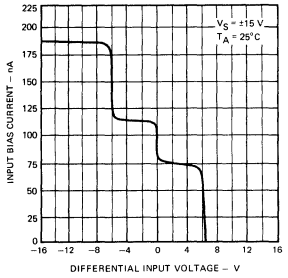


OFFSET VOLTAGE AS A FUNCTION OF INPUT RESISTANCE

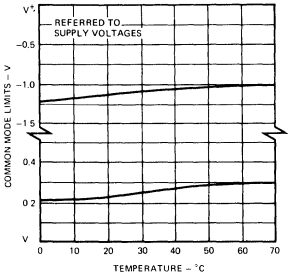


*Pins 5, 6 and 8 are shorted.

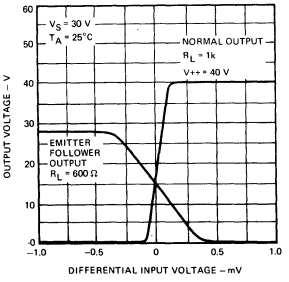
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



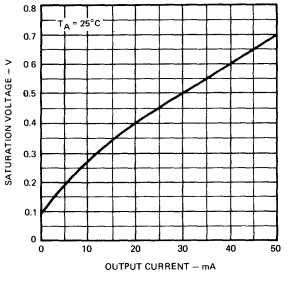
COMMON MODE LIMITS AS A FUNCTION OF TEMPERATURE



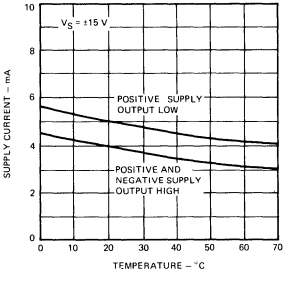
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



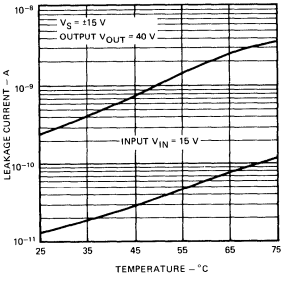
SATURATION VOLTAGE AS A FUNCTION OF CURRENT



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

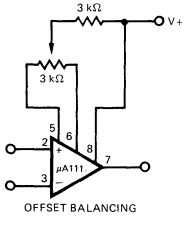


LEAKAGE CURRENT AS A FUNCTION OF TEMPERATURE

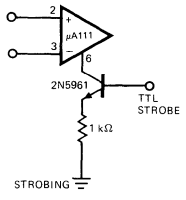


TYPICAL APPLICATIONS

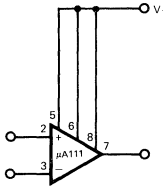
OFFSET NULL CIRCUIT



STROBE CIRCUIT



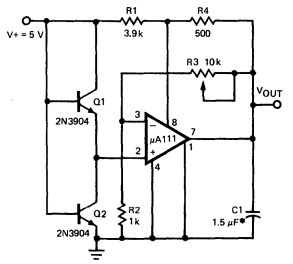
INCREASING INPUT STAGE CURRENT*



*Increases typical common mode slew rate from 7.0 V/μs to 18 V/μs.

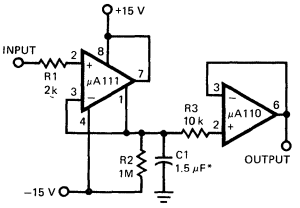
TYPICAL APPLICATIONS (Cont'd)

ADJUSTABLE LOW VOLTAGE REFERENCE SUPPLY



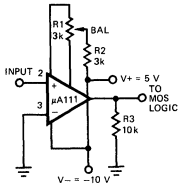
*Solid tantalum

POSITIVE PEAK DETECTOR

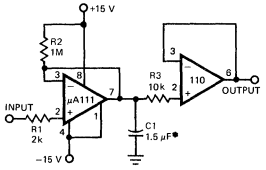


*Solid tantalum

ZERO CROSSING DETECTOR DRIVING MOS LOGIC

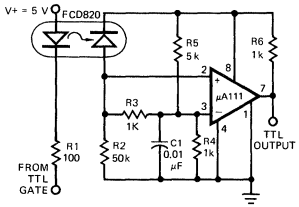


NEGATIVE PEAK DETECTOR

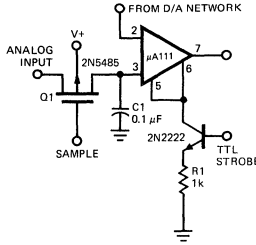


*Solid tantalum

DIGITAL TRANSMISSION ISOLATOR

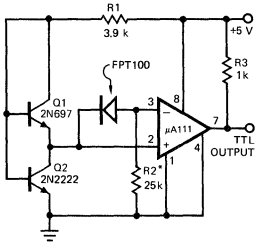


STROBING OF BOTH INPUT AND OUTPUT STAGES



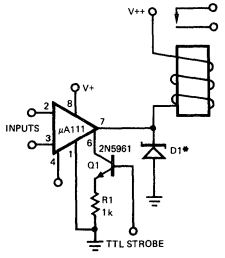
*Typical input current is 50 pA with inputs strobed off.

PRECISION PHOTODIODE COMPARATOR



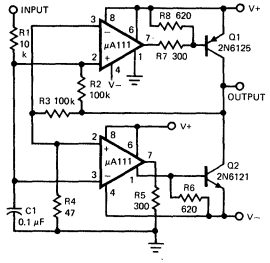
*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

RELAY DRIVER WITH STROBE

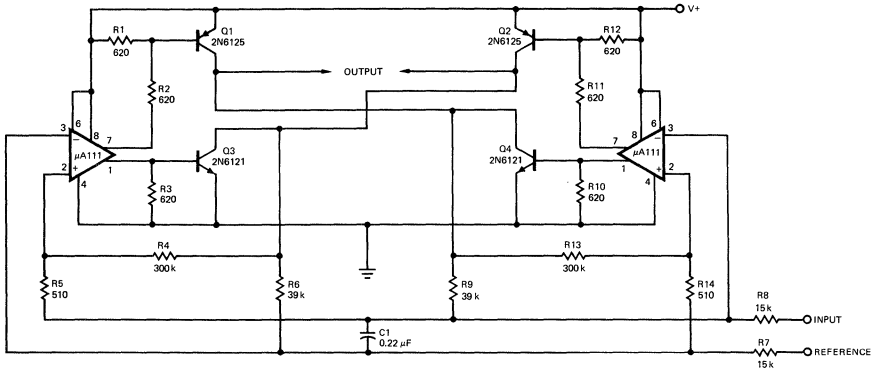


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

SWITCHING POWER AMPLIFIER



SWITCHING POWER AMPLIFIER



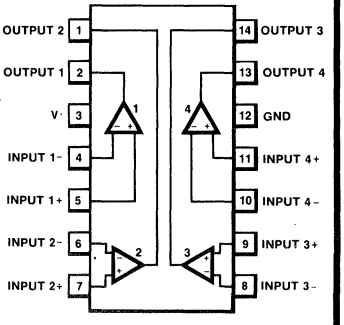
μA139/239/339 • μA139A/239A/339A
μA2901 • μA3302
LOW-POWER, LOW OFFSET VOLTAGE QUAD COMPARATORS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA139 series consists of four independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected PNP input stage allows the input common-mode voltage to include ground.

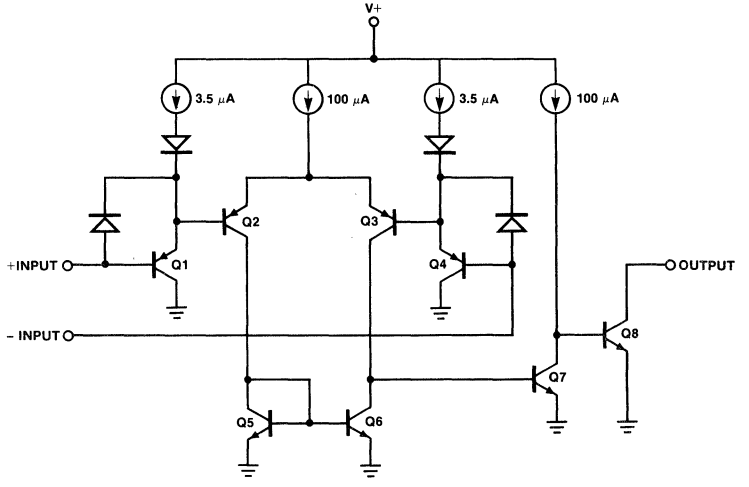
- **SINGLE SUPPLY OPERATION — +2.0 V TO +36 V**
- **DUAL SUPPLY OPERATION — ±1.0 V TO ±18 V**
- **ALLOW COMPARISON OF VOLTAGES NEAR GROUND POTENTIAL**
- **LOW CURRENT DRAIN — 800 μA TYP**
- **COMPATIBLE WITH ALL FORMS OF LOGIC**
- **LOW INPUT BIAS CURRENT — 25 nA TYP**
- **LOW INPUT OFFSET CURRENT — ±5 nA TYP**
- **LOW OFFSET VOLTAGE — ±2 mV**

CONNECTION DIAGRAM
14-PIN DIP

PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



SCHEMATIC DIAGRAM



ORDER INFORMATION

TYPE	PART NO.
μA139A	μA139ADM
μA139	μA139DM
μA239A	μA239ADC
μA239A	μA239APC
μA239	μA239DC
μA239	μA239PC
μA339A	μA339ADC
μA339A	μA339APC
μA339	μA339DC
μA339	μA339PC
μA2901	μA2901DC
μA2901	μA2901PC
μA3302	μA3302DC
μA3302	μA3302PC

ELECTRICAL CHARACTERISTICS (V^+ = 5 V, Note 4)

CHARACTERISTICS	CONDITIONS	μA139A			μA239A, μA339A			μA139			μA239, μA339			μA2901			μA3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A = 25°C, (Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3.0	±20	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = 25°C, (Note 5)		25	100		25	250		25	100		25	250		25	250		25	500	nA
Input Offset Current	$I_{IN(+)}$ - $I_{IN(-)}$, T_A = 25°C		±5.0	±25		±5.0	±50		±5.0	±25		±5.0	±50		±5.0	±50		±5.0	±100	nA
Input Common-Mode Voltage Range	T_A = 25°C, (Note 6)	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	V
Supply Current	R_L = ∞ on all Comparators, T_A = 25°C R_L = ∞, V^+ = 30 V, T_A = 25°C		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8 1.0	1.0 2.5		0.8	2.0	mA
Voltage Gain	R_L ≥ 15 kΩ, V^+ = 15 V (To Support Large V_O Swing), T_A = 25°C	50	200		50	200			200			200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{ref} = 1.4 V, V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C		300			300			300			300			300			300		ns
Response Time	V_{RL} = 5.0 V, R_L = 5.1 kΩ, T_A = 25°C, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)}$ ≥ 1.0 V, $V_{IN(+)}$ = 0, V_O ≤ 1.5 V, T_A = 25°C	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		2.0	16		mA
Saturation Voltage	$V_{IN(-)}$ ≥ 1.0 V, $V_{IN(+)}$ =0, I_{sink} ≤ 4.0 mA, T_A = 25°C		250	400		250	400		250	400		250	400			400		250	500	mV
Output Leakage Current	$V_{IN(+)}$ ≥ 1.0 V, $V_{IN(-)}$ = 0, V_O = 30 V, T_A = 25°C			200			200			200			200			200			200	nA
Input Offset Voltage	(Note 9)			4.0			4.0			9.0			9.0		9.0	15			40	mV
Input Offset Current	$I_{IN(+)}$ - $I_{IN(-)}$			±100			±150			±100			±150		50	200			300	nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300			400		200	500			1000	nA
Input Common-Mode Voltage Range		0		V^+-2.0	0		V^+-2.0	0		V^+-2.0	0		V^+-2.0	0		V^+-2.0	0		V^+-2.0	V
Saturation Voltage	$V_{IN(-)}$ ≥ 1.0 V, $V_{IN(+)}$ = 0, I_{sink} ≤ 4 mA			700			700			700			700		400	700			700	mV
Output Leakage Current	$V_{IN(+)}$ ≥ 1.0 V, $V_{IN(-)}$ = 0, V_O = 30 V			1.0			1.0			1.0			1.0			1.0			1.0	μA
Differential Input Voltage	Keep all V_{IN}'s ≥ 0 V (or V-, if used), (Note 8)			V^+			V^+			36			36	0		V^+			V_{CC}	V

ABSOLUTE MAXIMUM RATINGS

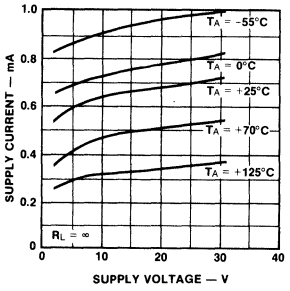
	μA139/μA239/μA339 μA139A/μA239A/μA339A μA2901	μA3302
Supply Voltage, V^+	36 V or ±18 V	28 V or ±14 V
Differential Input Voltage	36 V	28 V
Input Voltage Range	-0.3 V to +36 V	-0.3 V to +28 V
Power Dissipation (Note 1)		
9A, 6A	1 W	1 W
Output Short-Circuit to Gnd, (Note 2)	Continuous	Continuous
Input Current (V_{IN} < -0.3 V), (Note 3)	50 mA	50 mA
Operating Temperature Range		
μA339, μA339A	0° C to +70° C	
μA239, μA239A	-25° C to +85° C	
μA139, μA139A	-55° C to +125° C	
μA2901, μA3302	-40° C to +85° C	
Storage Temperature Range	-65° C to +150° C	-65° C to +150° C
Pin Temperature (Soldering, 10 seconds)	300° C	300° C

NOTES:

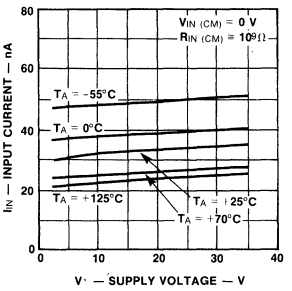
1. For operating at high temperatures, the μA339/μA339A, μA2901 μA3302 must be derated based on a 125° C maximum junction temperature and a thermal resistance of 125° C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The μA139 and μA139A must be derated based on a 150° C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition tiode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which negative, again returns to a value greater than -0.3 V.
4. These specifications apply for $V^+ = 5.0$ V and -55° C ≤ T_A ≤ +125° C, unless otherwise stated. With the μA239/μA239A, all temperature specifications are limited to -25° C ≤ T_A ≤ +85° C, the μA339/μA339A temperature specifications are limited to 0° C ≤ T_A ≤ +70° C, and the μA2901, μA3302 temperature range is -40° C ≤ T_A ≤ +85° C.
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltalge range is V^+ -1.5 V, but either or both inputs can go to +30 V without damage.
7. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained; see typical performance characteristics section.
8. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, comparator will provide a proper output state. The low input voltage state must not be less than -0.3 V or 0.3 V below the magnitude of the negative power supply, if used.
9. At output switch point, $V_O \cong 1.4$ V, $R_S = 0\Omega$ with V^+ from 5 V; and over the full input common-mode range (0 V to V^+ -1.5 V).
10. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5 V supply, V_{IN} should be limited to 25 V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

TYPICAL PERFORMANCE CHARACTERISTICS
μA139/μA239/μA339, μA139A/μA239A/μA339A, μA3302

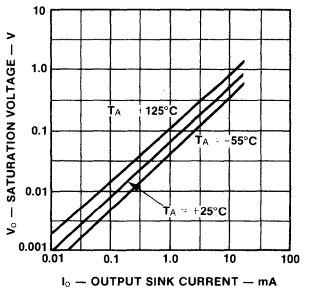
SUPPLY CURRENT



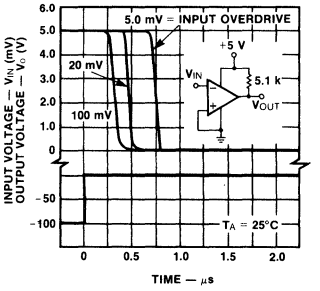
INPUT CURRENT



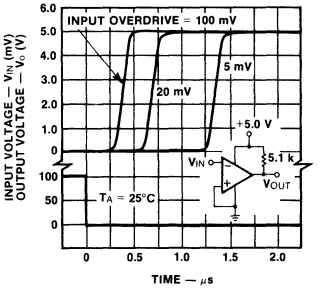
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION

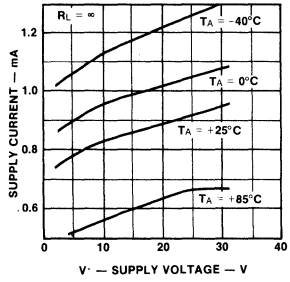


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION

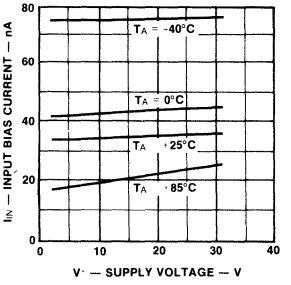


TYPICAL PERFORMANCE CHARACTERISTICS μA2901

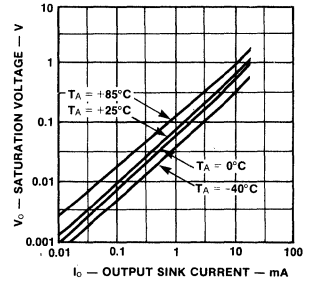
SUPPLY CURRENT



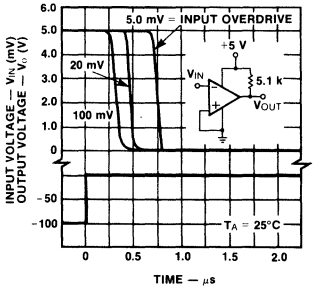
INPUT CURRENT



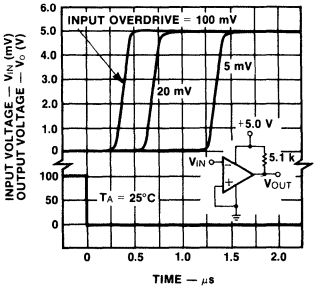
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION



APPLICATION HINTS

The μA139 series are high-gain, wide-bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the μA139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V to 30 V.

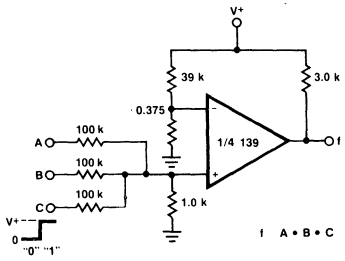
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V (at 25° C). An input clamp diode can be used as shown in the applications section.

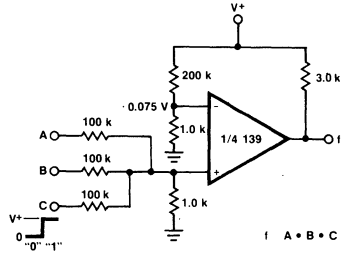
The output of the μA139 series is the uncommitted collector of a grounded-emitter npn output transistor. Many collectors can be tied together to provide an output ORing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the μA139 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60 Ω saturation resistance of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

TYPICAL APPLICATIONS (V+ = 15 V)

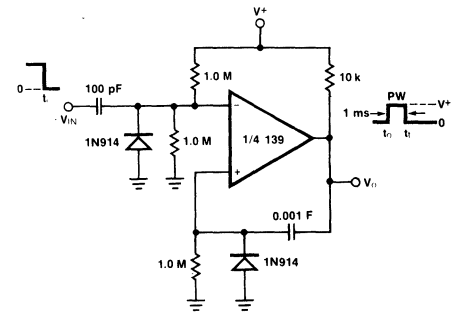
AND GATE



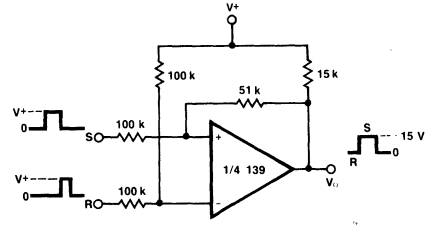
OR GATE



ONE-SHOT MULTIVIBRATOR

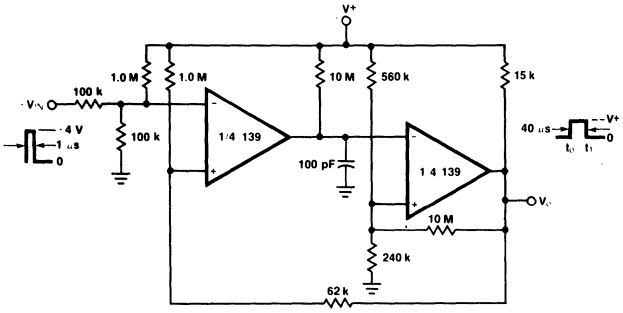


BI-STABLE MULTIVIBRATOR

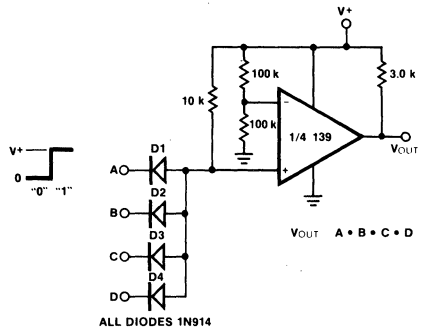


TYPICAL APPLICATIONS (V+ = 15 V) (Cont.)

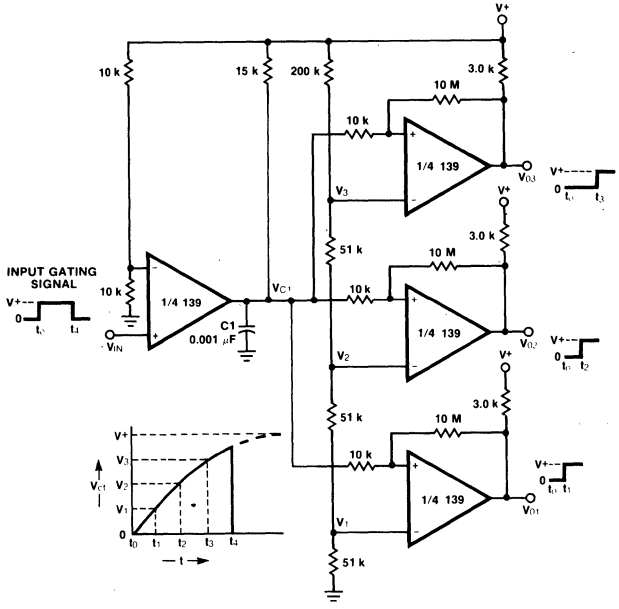
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT



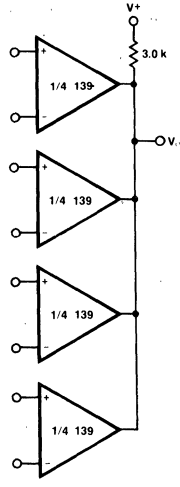
LARGE FAN-IN AND GATE



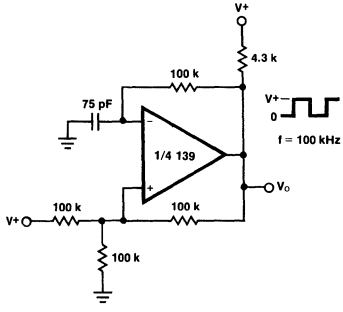
TIME DELAY GENERATOR



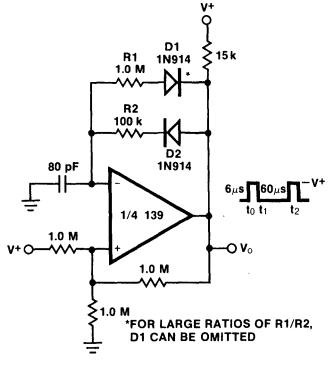
ORING THE OUTPUTS



SQUAREWAVE OSCILLATOR

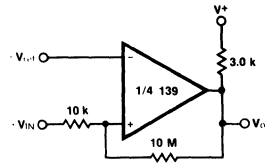


PULSE GENERATOR

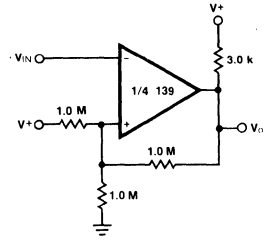


TYPICAL APPLICATIONS (V+ = 15 V) (Cont.)

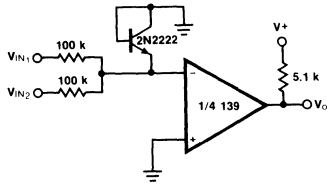
NON-INVERTING COMPARATOR WITH HYSTERESIS



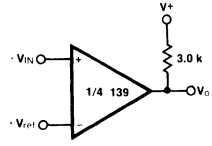
INVERTING COMPARATOR WITH HYSTERESIS



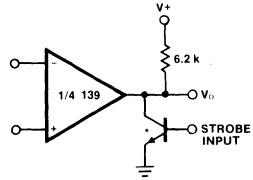
COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY



BASIC COMPARATOR

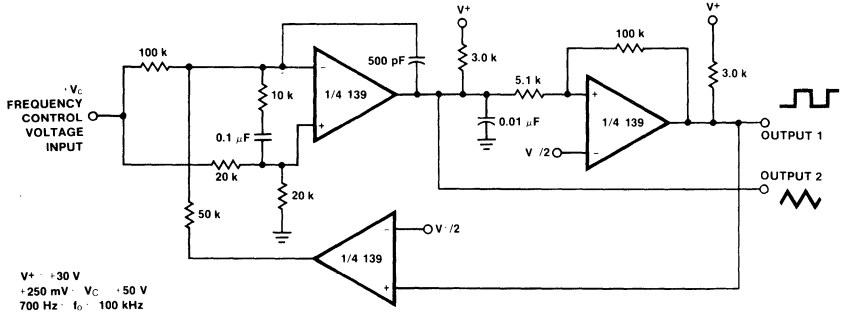


OUTPUT STROBING



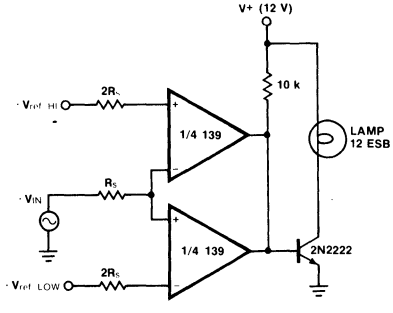
*OR LOGIC GATE WITHOUT PULL-UP RESISTOR

TWO-DECADE HIGH-FREQUENCY VCO

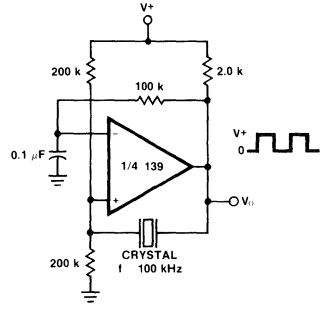


V+ = +30 V
+250 mV ≤ VC ≤ +50 V
700 Hz ≤ f0 ≤ 100 kHz

LIMIT COMPARATOR

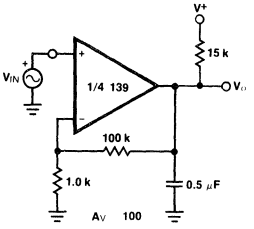


CRYSTAL CONTROLLED OSCILLATOR

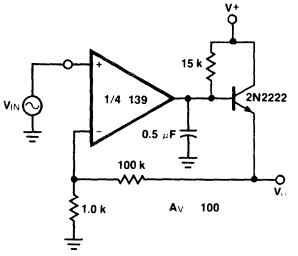


TYPICAL APPLICATIONS (V+ = 15 V) (Cont.)

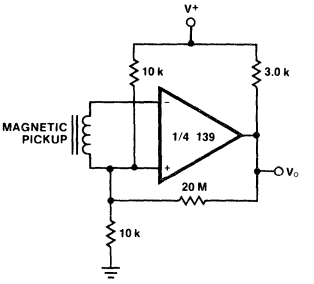
LOW FREQUENCY OP AMP



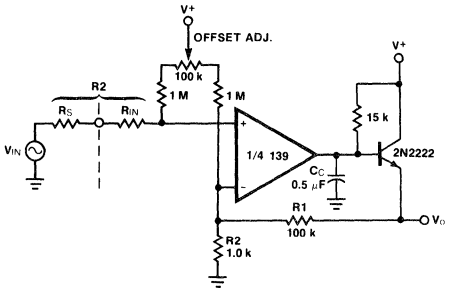
LOW FREQUENCY OP AMP (V_O = 0 V FOR V_{IN} = 0 V)



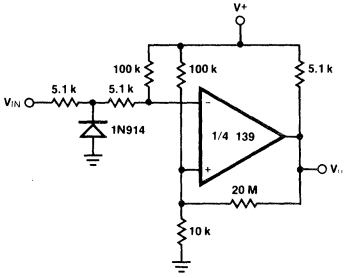
TRANSDUCER AMPLIFIER



LOW FREQUENCY OP AMP WITH OFFSET ADJUST

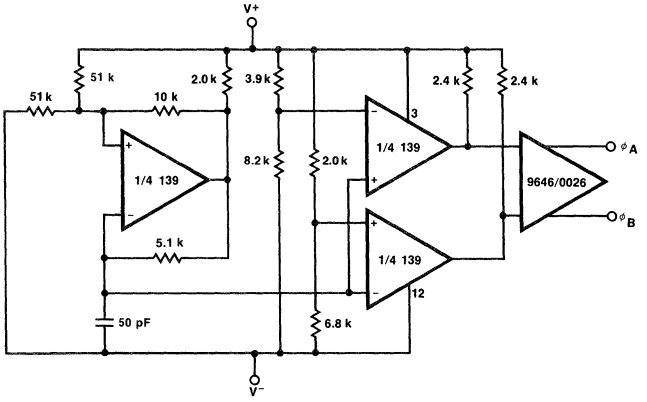


ZERO CROSSING DETECTOR (SINGLE POWER SUPPLY)

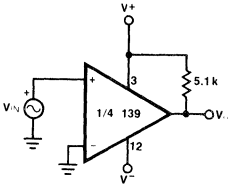


SPLIT-SUPPLY APPLICATIONS V+ = +15V and V- = -15V

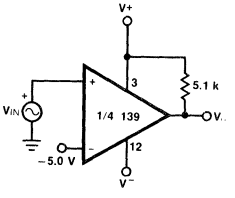
MOS CLOCK DRIVER



ZERO CROSSING DETECTOR



COMPARATOR WITH A NEGATIVE REFERENCE



μA710
HIGH SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUIT

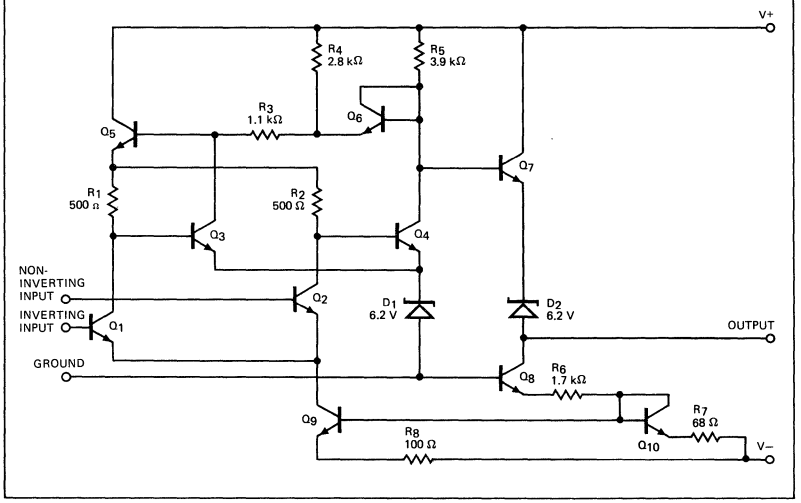
GENERAL DESCRIPTION – The μA710 is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **5 μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

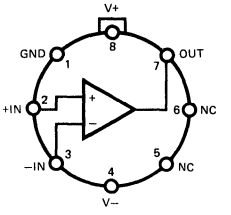
ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Ouput Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Storage Temperature Range	
Metal Can, Hermetic DIP and Flatpak	−65°C to +150°C
Molded DIP	−55°C to +125°C
Operating Temperature Range	
Military (μA710)	−55°C to +125°C
Commercial (μA710C)	0°C to +70°C
Pin Temperature	
Metal Can, Hermetic DIP and Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

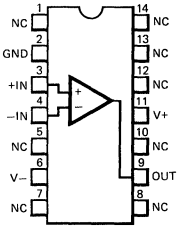


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA710	μA710HM
μA710C	μA710HC

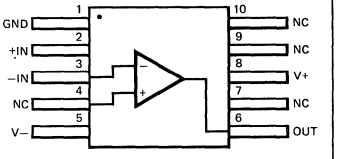
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA710	μA710DM
μA710C	μA710DC
μA710C	μA710PC

10-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
μA710	μA710FM

Notes on following pages.

*Planar is a patented Fairchild process.

μA710

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V+ = 12.0 V, V− = −6.0 V unless otherwise specified.

CHARACTERISTICS	CONDITIONS (Note 2)	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	2.0	2.5		mA
Response Time (Note 3)			40		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = +125°C$		3.5	10	μV/°C
	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = -55°C$		2.7	10	μV/°C
	$T_A = +125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$		5.0	25	nA/°C
	$T_A = 25°C$ to $T_A = -55°C$		15	75	nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	V− = −7.0 V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	80	100		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		1000			
Output HIGH Voltage	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5	1.7		mA
	$T_A = -55°C$, $\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5 mV		4.6	7.0	mA
Power Consumption	V_{OUT} = Gnd, Inverting Input = +10 mV		90	150	mW

μA710C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V+ = 12.0 V, V− = −6.0 V unless otherwise specified

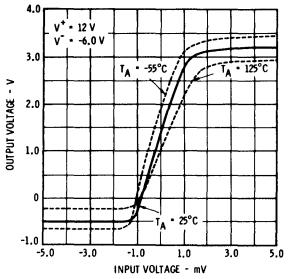
CHARACTERISTICS	CONDITIONS (Note 2)	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		15	50	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		24	100	nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	V = −7.0 V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Output HIGH Voltage	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Output LOW Voltage	$\Delta V_{IN} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5			mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5 mV		4.6	7.0	mA
Power Consumption	V_{OUT} = Gnd, Inverting Input = +10 mV		90	150	mW

NOTES:

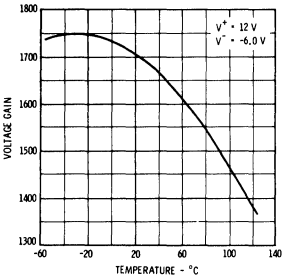
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for DIP, and 7.1 mW/°C for the Flatpak.
2. The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage as follows: For 710, 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C. For 710C, 1.5 V at 0°C, 1.4 V at +25°C, and 1.2 V at +70°C.
3. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

TYPICAL PERFORMANCE CURVES FOR μA710

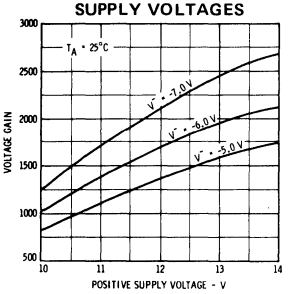
VOLTAGE TRANSFER CHARACTERISTIC



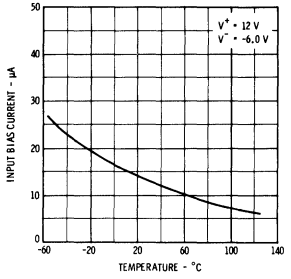
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



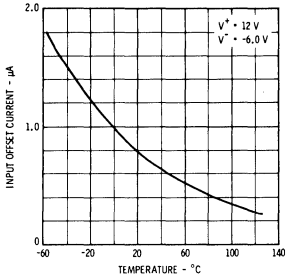
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



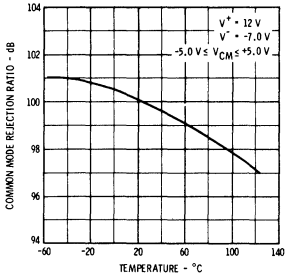
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



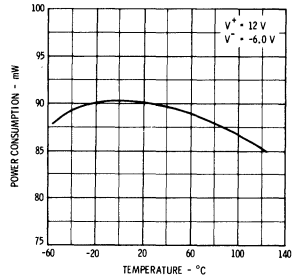
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



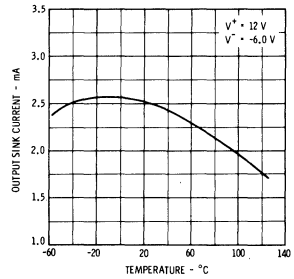
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



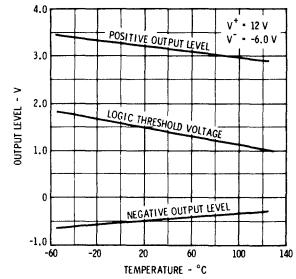
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



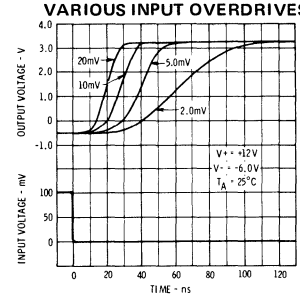
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



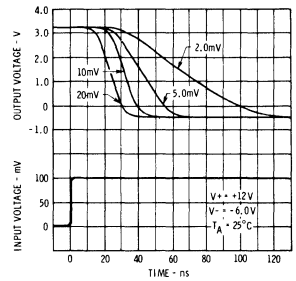
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



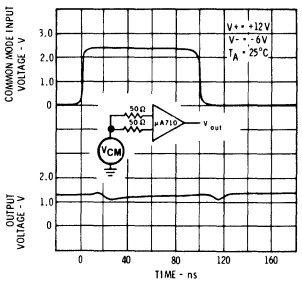
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



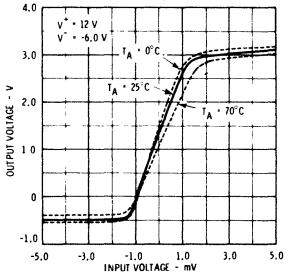
COMMON MODE PULSE RESPONSE



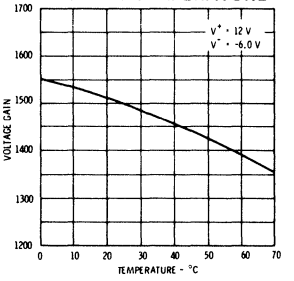
4

TYPICAL PERFORMANCE CURVES FOR μA710C

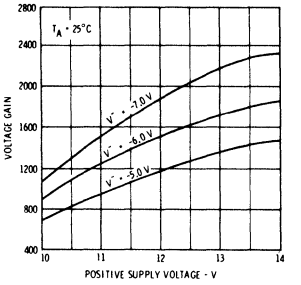
VOLTAGE TRANSFER CHARACTERISTIC



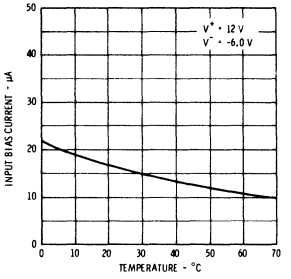
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



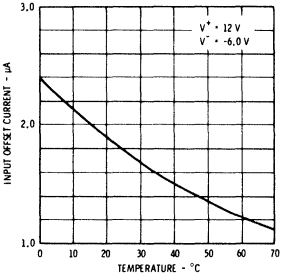
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



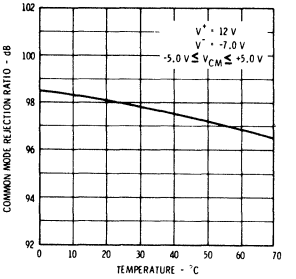
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



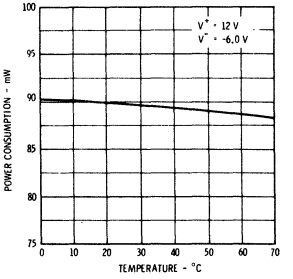
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



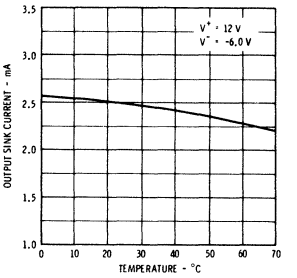
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



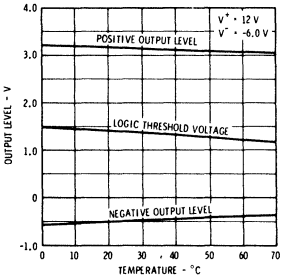
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



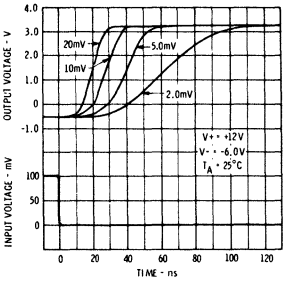
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



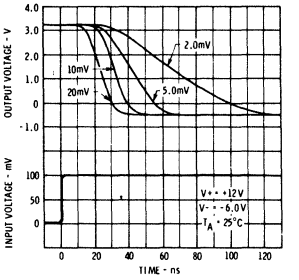
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



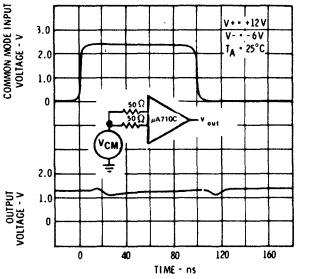
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



μA711

DUAL HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

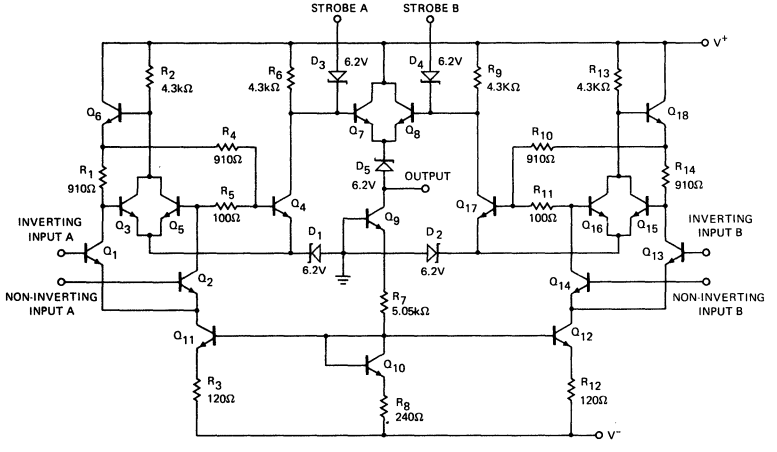
GENERAL DESCRIPTION – The μA711 is a Dual, Differential Voltage Comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-Go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed using the Fairchild Planar* epitaxial process.

- **FAST RESPONSE TIME . . . 40 ns TYPICAL**
- **5 mV MAXIMUM OFFSET VOLTAGE**
- **10μA MAXIMUM OFFSET CURRENT**
- **INDEPENDENT STROBING OF EACH COMPARATOR**

ABSOLUTE MAXIMUM RATINGS

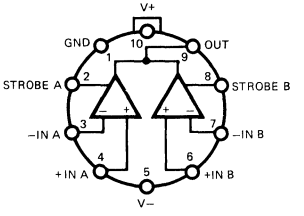
Positive Supply Voltage	+14 V
Negative Supply Voltage	−7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (μA711)	−55°C to +125°C
Commercial (μA711C)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Metal Can, Hermetic DIP and Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



Notes on following page.

CONNECTION DIAGRAMS
10-PIN METAL CAN
(TOP VIEWS)
PACKAGE OUTLINES 5F 5N
PACKAGE CODES H H

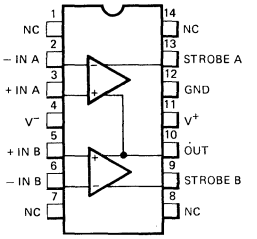


NOTE: Pin 5 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA711	μA711HM
μA711C	μA711HC

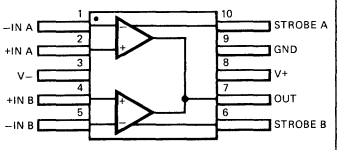
14-PIN DIP
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA711	μA711DM
μA711C	μA711DC
μA711C	μA711PC

10-PIN FLATPAK
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

TYPE	PART NO.
μA711	μA711FM

*Planar is a patented Fairchild process.

μA711

ELECTRICAL CHARACTERISTICS: T_A= 25°C, V^+= 12 V, V^-= −6.0 V unless otherwise specified

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OUT} = +1.4 V, $R_S \leq 200\ \Omega$, V_{CM} = 0		1.0	3.5	mV
	V_{OUT} = +1.4 V, $R_S \leq 200\ \Omega$		1.0	5.0	mV
Input Offset Current	V_{OUT} = 1.4 V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = −7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Output HIGH Voltage	$V_{IN} \geq 10$ mV, I_O = 5mA	2.5	3.5		V
Output LOW Voltage	$V_{IN} \geq 10$ mV	−1.0	−0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3$ V	−1.0		0	V
Output Sink Current	$V_{IN} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{STROBE} = 100 mV		1.2	2.5	mA
Positive Supply Current	V_{OUT} = Gnd, Inverting Input = +5mV		8.6		mA
Negative Supply Current	V_{OUT} = Gnd, Inverting Input = +5mV		3.9		mA
Power Consumption			130	200	mW

The following specifications apply for $-55° C \leq T_A \leq +125° C$:

Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, V_{CM} = 0			4.5	mV
	$R_S \leq 200\ \Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP, and 7.1 mW/°C for the Flatpak.
2. The response time specified (see definitions) is for a 100 mV step input with 5 mV overdrive.
3. The input offset voltage is specified for a logic threshold as follows:
   711: 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C
   711C: 1.5 V at 0°C, 1.4 V at +25°C, 1.2 V at +70°C

μA711C

ELECTRICAL CHARACTERISTICS: T_A= 25°C, V^+= 12 V, V^-= −6.0 V unless otherwise specified

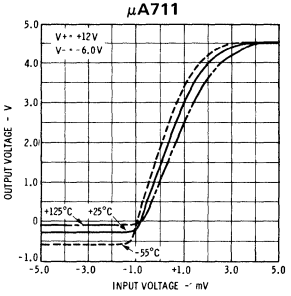
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OUT} = +1.4 V, R_S ≤200 Ω, V_{CM} = 0		1.0	5.0	mV
	V_{OUT} = +1.4 V, R_S ≤200 Ω		1.0	7.5	mV
Input Offset Current	V_{OUT} = +1.4 V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = −7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Output HIGH Voltage	V_{IN} ≥10 mV		4.5	5.0	V
Loaded Output HIGH Voltage	V_{IN} ≥10 mV, I_O = 5 mA	2.5	3.5		V
Output LOW Voltage	V_{IN} ≥10 mV	−1.0	−0.5	0	V
Strobed Output Level	V_{STROBE} ≤0.3 V	−1.0		0	V
Output Sink Current	V_{IN} ≥10 mV, V_{OUT} ≥0	0.5	0.8		mA
Strobe Current	V_{STROBE} = 100 mV		1.2	2.5	mA
Positive Supply Current	V_{OUT} Gnd, Inverting Input = +10mV		8.6		mA
Negative Supply Current	V_{OUT}Gnd, Inverting Input = +10mV		3.9		mA
Power Consumption			130	230	mW

The following specifications apply for 0° C ≤ T_A ≤ +70° C:

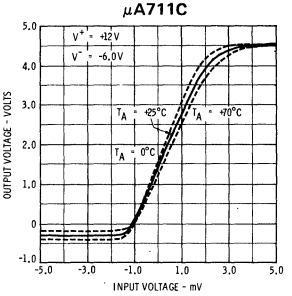
Input Offset Voltage (Note 3)	R_S ≤ 200 Ω, V_{CM} = 0			6.0	mV
	R_S ≤ 200 Ω			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

TYPICAL PERFORMANCE CURVES FOR μA711 AND μA711C

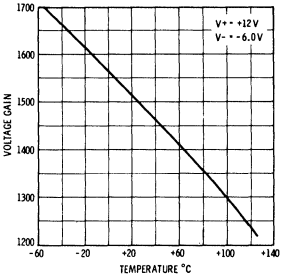
VOLTAGE TRANSFER CHARACTERISTIC μA711



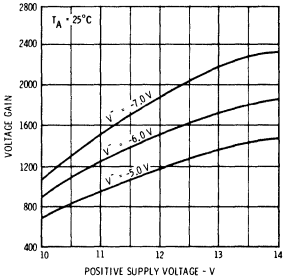
VOLTAGE TRANSFER CHARACTERISTIC μA711C



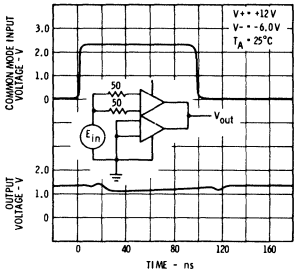
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



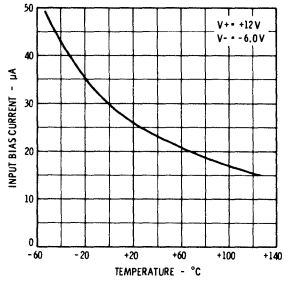
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



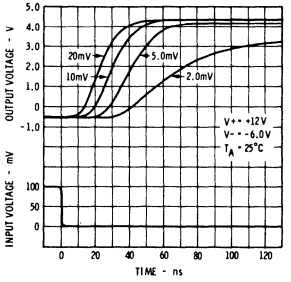
COMMON MODE PULSE RESPONSE



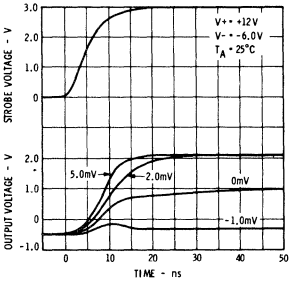
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



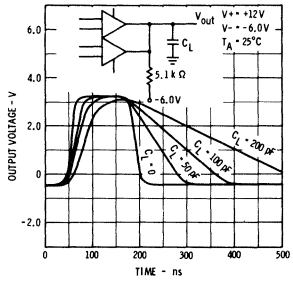
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



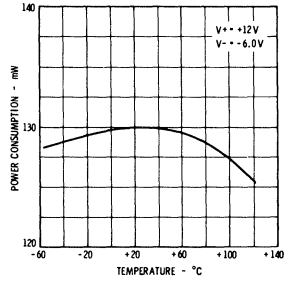
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



μA734

PRECISION VOLTAGE COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

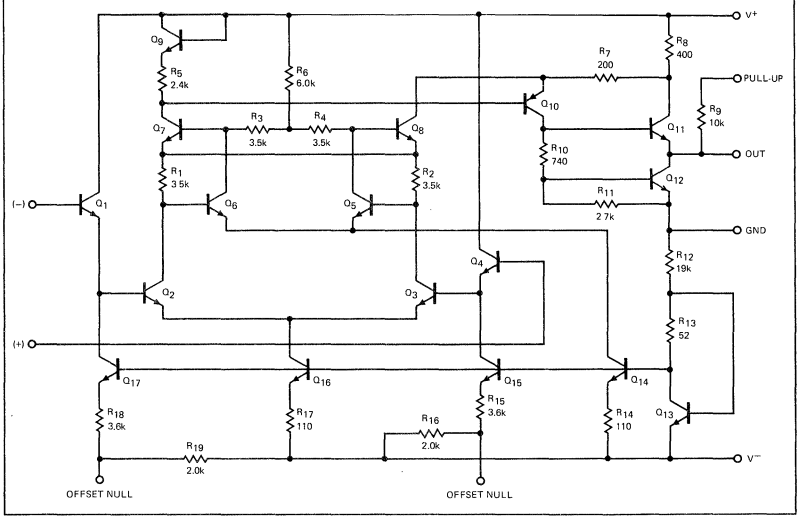
GENERAL DESCRIPTION – The μA734 is a Precision Voltage Comparator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is specifically designed for high accuracy level sensing and measuring applications. The μA734 is extremely useful for analog-to-digital converters with twelve bit accuracies and one mega-bit conversion rates. Maximum resolution is obtained by high gain, low input offset current, and low input offset voltage. Its superior temperature stability can be improved by offset nulling which further reduces offset voltage drift. Balanced or unbalanced supply operation and standard TTL logic compatibility enhance the μA734's versatility.

- **CONSTANT INPUT IMPEDANCE OVER DIFFERENTIAL INPUT RANGE**
- **HIGH INPUT IMPEDANCE – 55 MΩ**
- **LOW DRIFT – 3.5 μV/°C**
- **HIGH GAIN – 60 k**
- **BALANCED OFFSET NULL CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE – ±5 V to ±18 V**
- **TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

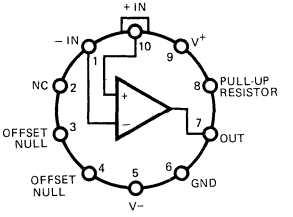
Supply Voltage	±18 V
Peak Output Current	10 mA
Differential Input Voltage	±10 V
Input Voltage Range (Note 1)	±13 V
Voltage Between Offset Null and V⁻	±0.5 V
Internal Power Dissipation (Note 2)	
Metal Can	500 mW
DIP	670 mW
Operating Temperature Range	
Military (μA734)	−55°C to +125°C
Commercial (μA734C)	0°C to +70°C
Storage Temperature Range	
Metal Can, DIP	−65°C to +150°C
Pin Temperature (Soldering, 60 s Max)	300°C

EQUIVALENT CIRCUIT



Notes on following pages.

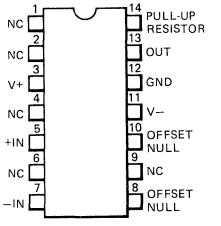
CONNECTION DIAGRAMS
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5N
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA734	μA734HM
μ734C	μA734HC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA734	μA734DM
μA734C	μA734DC

*Planar is a patented Fairchild process.

±15 VOLT OPERATION FOR μA734C

ELECTRICAL CHARACTERISTICS: T_A = 25°C, Pin 8 tied to +15 V, unless otherwise specified, Note 3.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.1	5.0	mV
Input Offset Current			3.5	25	nA
Input Bias Current			30	100	nA
Input Resistance		7.0	55		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	35 k	60 k		V/V
Positive Supply Current — Output LOW			4.0	5.0	mA
Negative Supply Current — Output LOW			1.5	2.0	mA
Power Consumption — Output LOW			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.2	7.5	mV
Input Offset Current			4.0	45	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leq 50\ \Omega$		3.5	20	μV/°C
Average Input Offset Current Drift	T_A = +25°C to +70°C		0.02	0.3	nA/°C
	T_A = +25°C to 0°C		0.05	0.75	nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio V_S = ±5 V to ±18 V	$R_S \leq 50\ k\Omega$		6.0	100	μV/V
Output HIGH Voltage	I_{OUT} = 0.080 mA	7.0			V
	I_{OUT} = 0.080 mA, V_8 = +5.0 V	2.4		5.0	V
Output LOW Voltage	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current — Output LOW				7.0	mA
Negative Supply Current — Output LOW				2.5	mA
Power Dissipation — Output LOW				145	mW

±15 VOLT OPERATION FOR μA734

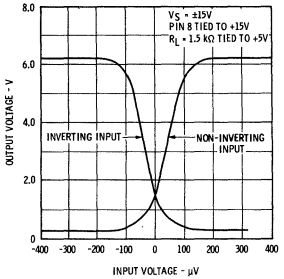
ELECTRICAL CHARACTERISTICS: T_A = 25°C, Pin 8 tied to +15 V, unless otherwise specified, Note 3.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.9	3.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			28	50	nA
Input Resistance		20	60		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	35 k	70 k		V/V
Positive Supply Current — Output LOW			4.0	5.0	mA
Negative Supply Current — Output LOW			1.5	2.0	mA
Power Consumption — Output LOW			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0 V 5 mV Overdrive, 100 mV Pulse		200		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.1	4.0	mV
Input Offset Current			3.0	20	nA
Average Input Offset Voltage Drift Without External Trim	$R_S \leq 50\ k\Omega$		2.5	15	μV/°C
Average Input Offset Current Drift	T_A = +25°C to +125°C T_A = +25°C to −55°C		0.01 0.05	0.1 0.4	nA/°C nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0 V	25 k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio V_S = ±5 V to ±18 V	$R_S \leq 50\ k\Omega$		5.0	100	μV/V
Output HIGH Voltage	I_{OUT} = 0.080 mA I_{OUT} = 0.080 mA, V_8 = +5.0 V	7.0 2.4		 5.0	V V
Output LOW Voltage	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current — Output LOW				7.0	mA
Negative Supply Current — Output LOW				2.5	mA
Power Dissipation — Output LOW				145	mW

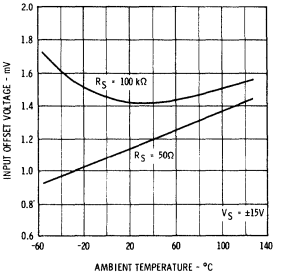
NOTES:
1. Rating applies for ±15 V supplies. For other supply voltages the rating is within 2 V of either supply.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can, 8.3 mW/°C for DIP.
3. Pin numbers refer to metal can package.

TYPICAL PERFORMANCE CURVES FOR μA734 AND μA734C (Note 2)

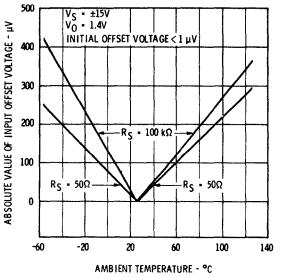
TRANSFER CHARACTERISTICS



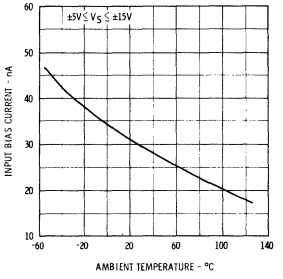
UN-NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



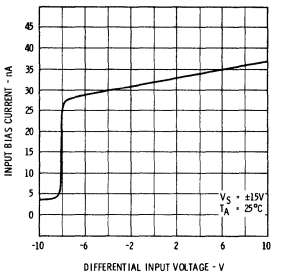
INPUT OFFSET VOLTAGE CHANGE AS A FUNCTION OF AMBIENT TEMPERATURE - NULLED TO ZERO AT 25°C



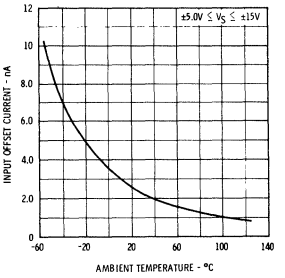
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



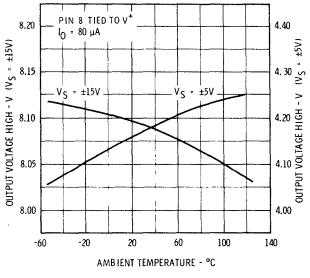
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



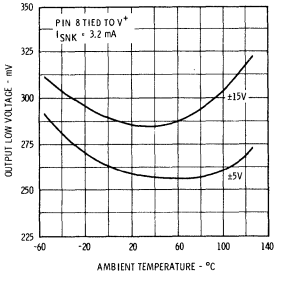
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



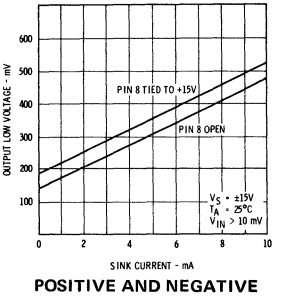
OUTPUT HIGH VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



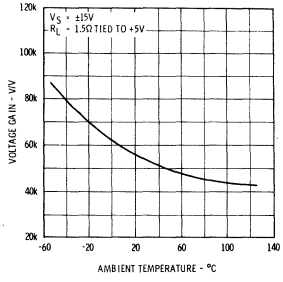
OUTPUT LOW VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



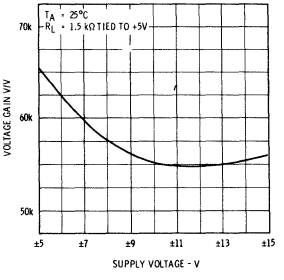
OUTPUT VOLTAGE LOW VS SINK CURRENT



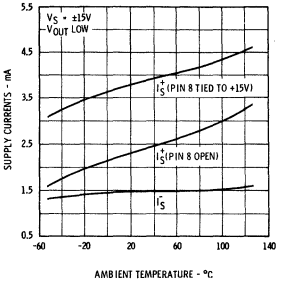
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

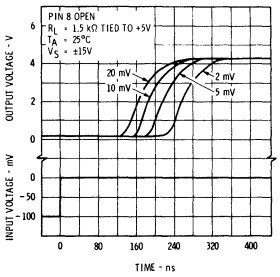


POSITIVE AND NEGATIVE SUPPLY CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE

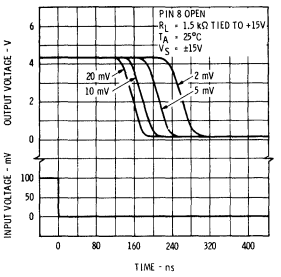


TYPICAL PERFORMANCE CURVES FOR μA734 AND μA734C (Note 2)

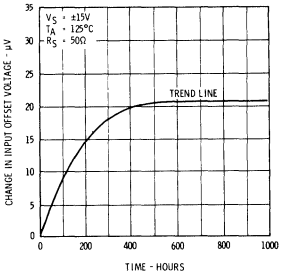
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



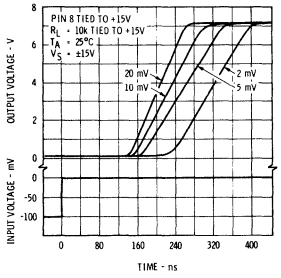
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



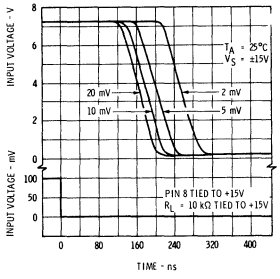
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



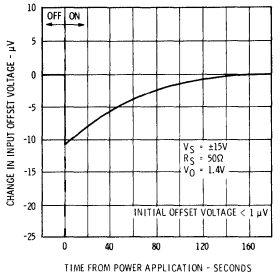
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



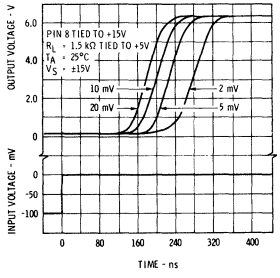
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



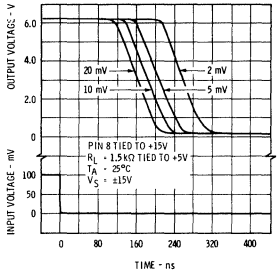
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



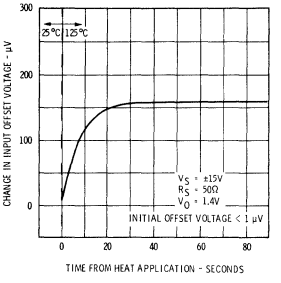
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



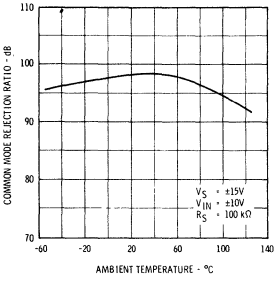
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



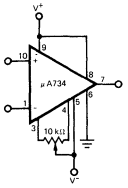
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



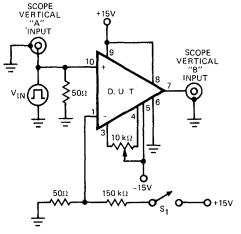
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



OFFSET NULL CIRCUIT (NOTE 2)



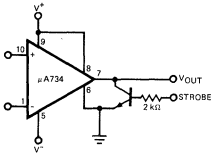
AC TEST CIRCUIT (NOTE 2)



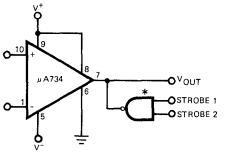
V_{IN} = -100 mV, 100 kHz

TYPICAL APPLICATIONS (Note 2)

STROBE CIRCUITRY

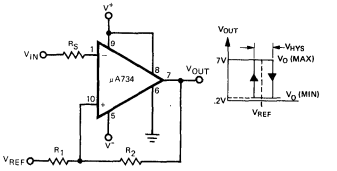


ALTERNATE STROBE CIRCUITRY



* 1/2 9944

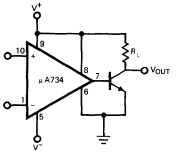
LEVEL DETECTOR WITH HYSTERESIS



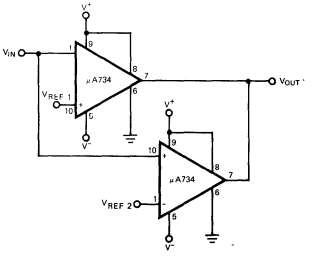
$$R_S = \frac{R_1 R_2}{R_1 + R_2} \quad \text{FOR MINIMUM OFFSET}$$

$$V_{HYS} = \frac{R_1 [V_{O\,MAX} - V_{O\,MIN}]}{R_1 + R_2}$$

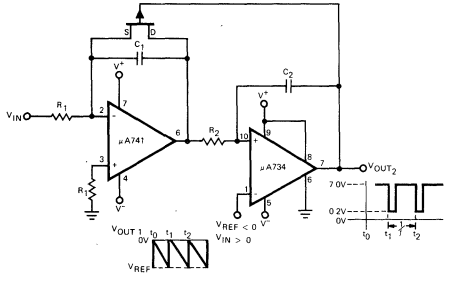
HIGH POWER OUTPUT CIRCUITS



PRECISION DUAL LIMIT GO-NO GO TESTER

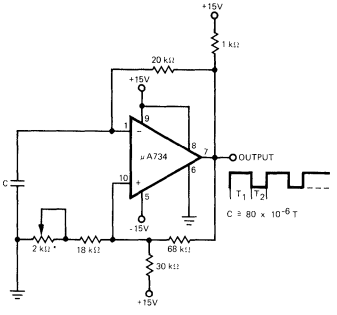


VOLTAGE CONTROLLED OSCILLATOR



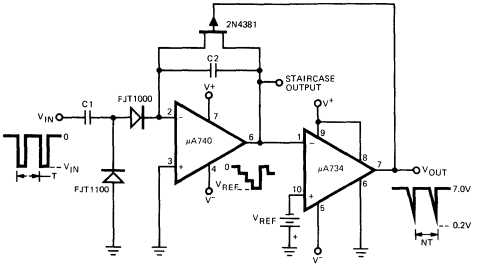
$$f = \frac{V_{IN}}{|V_{REF}| R_1 C_1} \qquad R_2 C_2 > \frac{|V_{REF}| C_1}{I_{DSS}}$$

FREE RUNNING OSCILLATOR



* Adjusts $\frac{T_1}{T_2}$

FREQUENCY DIVIDER & STAIRCASE GENERATOR

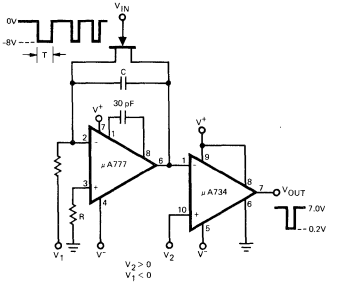


$$|V_{REF}| = 2V_D + N \left[3.5T + 2V_D - \frac{C_1 V_{IN}}{C_2}\right]$$

T In Seconds

V_D for FJT1000 ≈ 0.31V

PULSE WIDTH DISCRIMINATOR

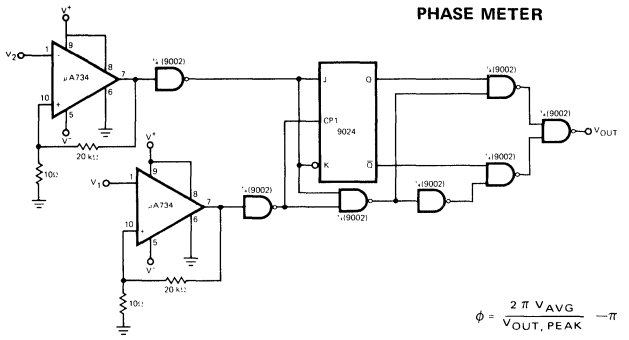


V_{OUT} Pulse Appears

Whenever $T > \frac{R C V_2}{|V_1|}$

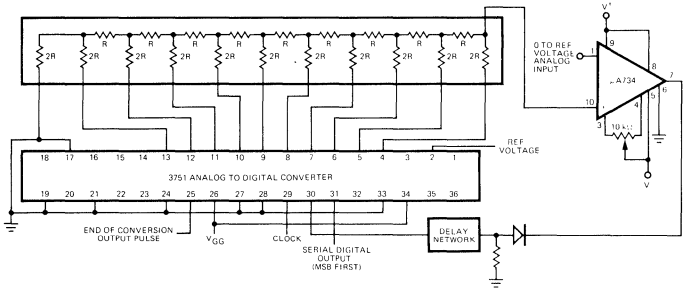
TYPICAL APPLICATIONS (Note 2)

PHASE METER



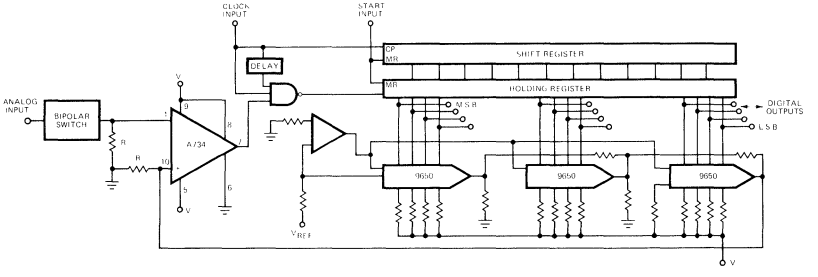
$$\phi = \frac{2\pi V_{AVG}}{V_{OUT,\,PEAK}} - \pi$$

12-BIT A/D CONVERTER



NO. OF BITS	R VALUE
8	12.5kΩ
9	25kΩ
10	50kΩ
12	200kΩ

12-BIT A/D CONVERTER



μA760

HIGH SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

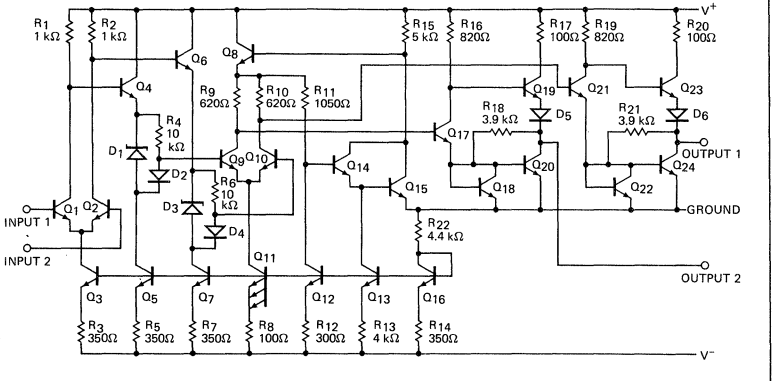
GENERAL DESCRIPTION – The μA760 is a Differential Voltage Comparator offering considerable speed improvement over the μA710 family and operation from symmetric supplies of from ±4.5 V to ±6.5 V. The μA760 can be used in high speed analog to digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The μA760 output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.

- **GUARANTEED HIGH SPEED – 25 ns MAX**
- **GUARANTEED DELAY MATCHING ON BOTH OUTPUTS**
- **COMPLEMENTARY TTL COMPATIBLE OUTPUTS**
- **HIGH SENSITIVITY**
- **USES STANDARD SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

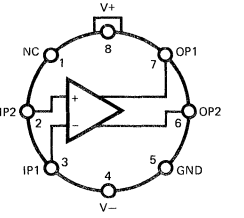
Positive Supply Voltage	+8 V
Negative Supply Voltage	-8 V
Peak Output Current	10 mA
Differential Input Voltage	±5 V
Input Voltage	$V+ \geq V_{IN} \geq V-$
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Operating Temperature Range	
Military (μA760)	-55°C to 125°C
Commercial (μA760C)	0°C to 70°C
Storage Temperature Range	
Metal Can and DIP	-65°C to 150°C

EQUIVALENT CIRCUIT



Notes on following page.

CONNECTION DIAGRAMS
8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H

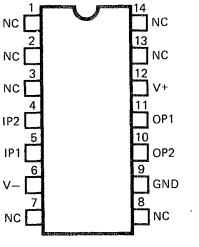


NOTE: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μA760	μA760HM
μA760C	μA760HC

14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA760	μA760DM
μA760C	μA760DC

μA760

ELECTRICAL CHARACTERISTICS: V_S = ±4.5 V to ±6.5 V, T_A = -55°C to +125°C, T_A = 25°C for typical figures unless otherwise specified.

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, T_A = 25°C		18	30	ns
	Note 3, T_A = 25°C			25	ns
	Note 4		16		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	Note 2, T_A = 25°C			5.0	ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	Note 2, T_A = 25°C			7.5	ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, T_A = 25°C			7.5	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = −55°C to T_A = +125°C		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +125°C		2.0		nA/°C
	T_A = 25°C to T_A = −55°C		7.0		nA/°C
Input Voltage Range	V_S = ±6.5V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		V
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0$ mA				
	V_S = ±5.0V	2.4	3.2		V
	I_{OUT} = 80 μA, V_S = ±4.5V	2.4	3.0		V
Output LOW Voltage (either output)	I_{SINK} = 3.2 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	32	mA
Negative Supply Current	V_S = ±6.5V		9.0	16	mA

μA760C

ELECTRICAL CHARACTERISTICS: $V_S = \pm 4.5$ V to ± 6.5 V, $T_A = -55°C$ to $+125°C$, $T_A = 25°C$ for typical figures unless otherwise specified.

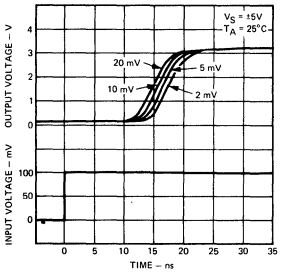
CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance (either output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, $T_A = 25°C$		18	30	ns
	Note 3, $T_A = 25°C$			25	ns
	Note 4		16		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, $T_A = 25°C$			5.0	ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	Note 2, $T_A = 25°C$			5.0	ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	Note 2, $T_A = 25°C$			10	ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	Note 2, $T_A = 25°C$			10	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 0°C$ to $T_A = +70°C$		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		5.0		nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		10		nA/°C
Input Voltage Range	$V_S = \pm 6.5V$	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		
Output HIGH Voltage (either output)	$0 \leq I_{OUT} \leq 5.0$ mA				
	$V_S = \pm 5.0V$	2.4	3.2		V
	$I_{OUT} = 80\ \mu A$, $V_S = \pm 4.5V$	2.5	3.0		V
Output LOW Voltage (either output)	$I_{SINK} = 3.2$ mA		0.25	0.4	V
Positive Supply Current	$V_S = \pm 6.5V$		18	34	mA
Negative Supply Current	$V_S = \pm 6.5V$		9.0	16	mA

NOTES

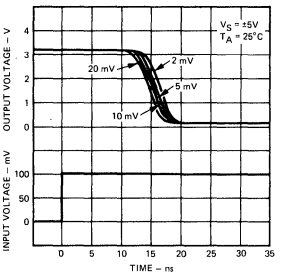
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can and 8.3 mW/°C for the DIP.
2. Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
3. Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.
4. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

TYPICAL PERFORMANCE CURVES FOR μA760 AND μA760C

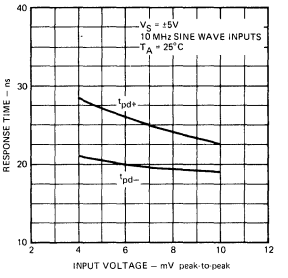
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



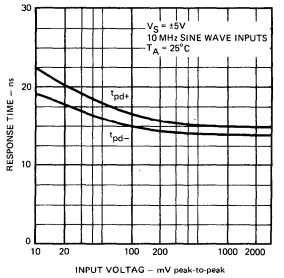
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



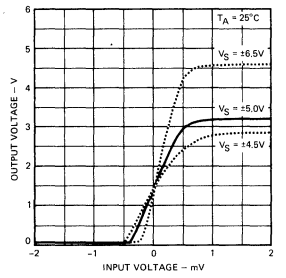
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



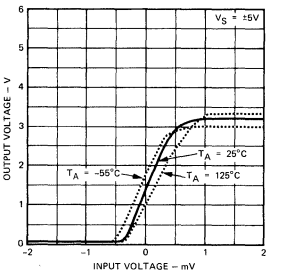
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



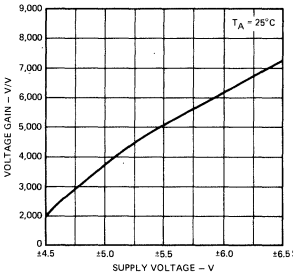
VOLTAGE TRANSFER CHARACTERISTIC



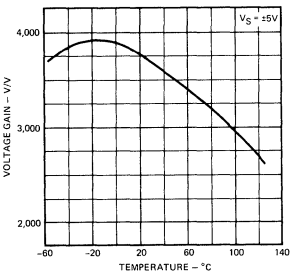
VOLTAGE TRANSFER CHARACTERISTIC



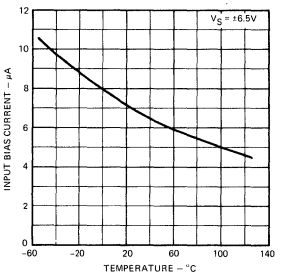
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



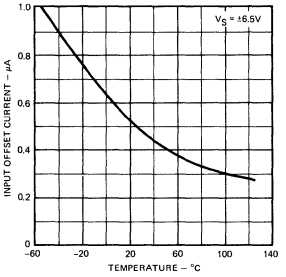
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



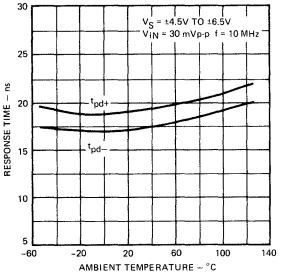
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



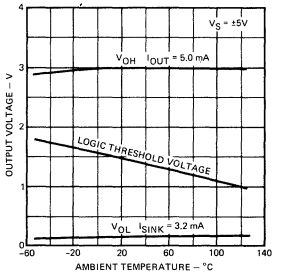
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



RESPONSE TIME AS A FUNCTION OF AMBIENT TEMPERATURE

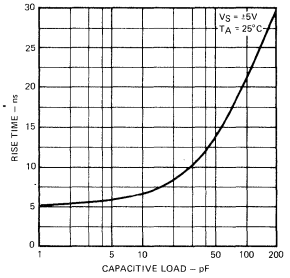


OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE

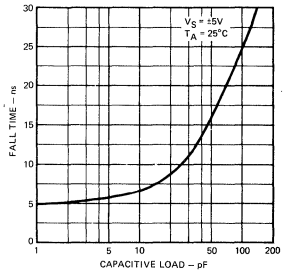


TYPICAL PERFORMANCE CURVES FOR μA760 AND μA760C (Cont'd)

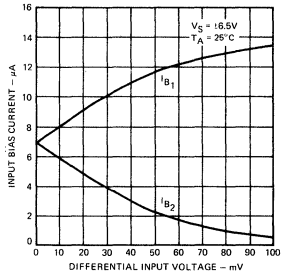
RISE TIME AS A FUNCTION OF CAPACITIVE LOAD



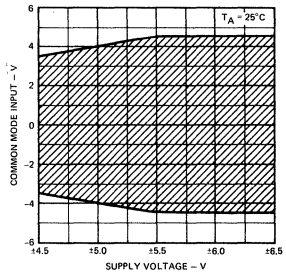
FALL TIME AS A FUNCTION OF CAPACITIVE LOAD



INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



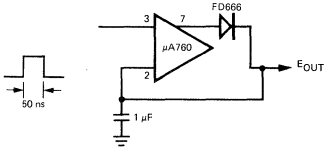
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



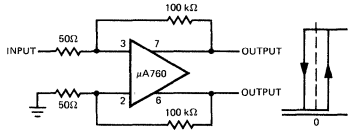
APPLICATIONS

Pin numbers shown are only for Metal Can

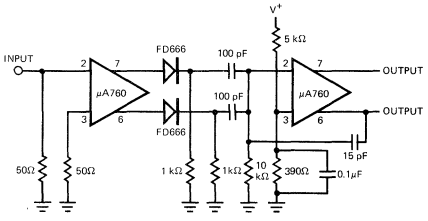
FAST POSITIVE PEAK DETECTOR



LEVEL DETECTOR WITH HYSTERESIS

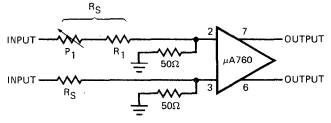


ZERO CROSSING DETECTOR



Total Delay = 30 ns
Input frequency = 300 Hz to 3 MHz
Minimum input voltage = 20 mVpk-pk

LINE RECEIVER WITH HIGH COMMON MODE RANGE



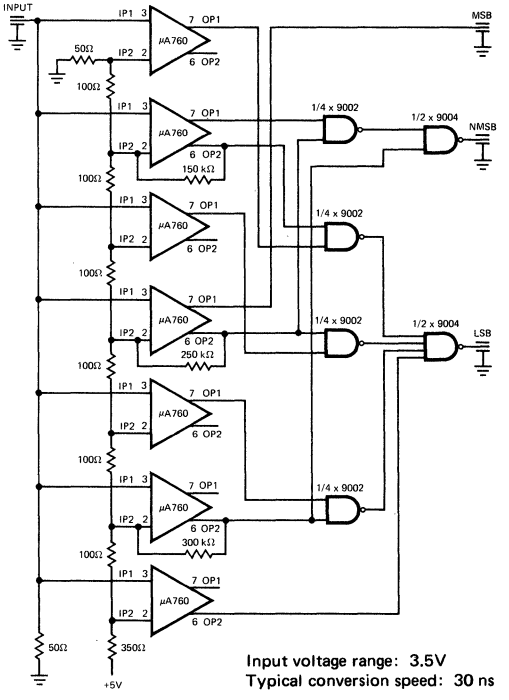
Common mode range = $\pm 4 \times \frac{RS}{50}$ V

Differential Input sensitivity = $5 \times \frac{RS}{50}$ mV

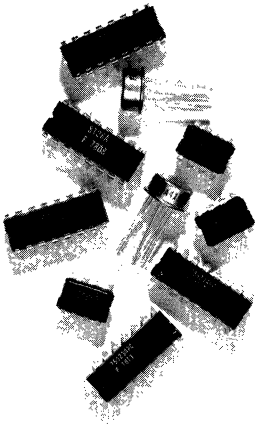
P_1 must be adjusted for optimum common mode rejection.

For R_S = 200Ω
Common mode range = ±16V
Sensitivity = 20 mV

HIGH SPEED 3-BIT A/D CONVERTER



Input voltage range: 3.5V
Typical conversion speed: 30 ns



DATA ACQUISITION

μAF198 • μAF298 • μAF398

MONOLITHIC SAMPLE AND HOLD AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

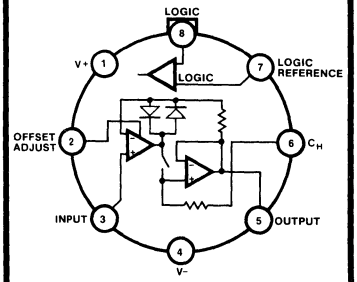
GENERAL DESCRIPTION — The μAF198/298/398 are monolithic sample and hold circuits which utilize J-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the μAF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

- **OPERATES FROM ±5 V TO ±18 V SUPPLIES**
- **LESS THAN 10 μs ACQUISITION TIME**
- **TTL, PMOS, CMOS COMPATIBLE LOGIC INPUT**
- **1.4V DIFFERENTIAL THRESHOLD**
- **0.5 mV TYPICAL HOLD STEP AT C_H = 0.01 μF**
- **LOW INPUT OFFSET**
- **0.002% GAIN ACCURACY**
- **LOW OUTPUT NOISE IN HOLD MODE**
- **INPUT CHARACTERISTICS DO NOT CHANGE DURING HOLD MODE**
- **HIGH SUPPLY REJECTION RATIO IN SAMPLE OR HOLD**
- **WIDE BANDWIDTH**

CONNECTION DIAGRAM
8-PIN METAL CAN

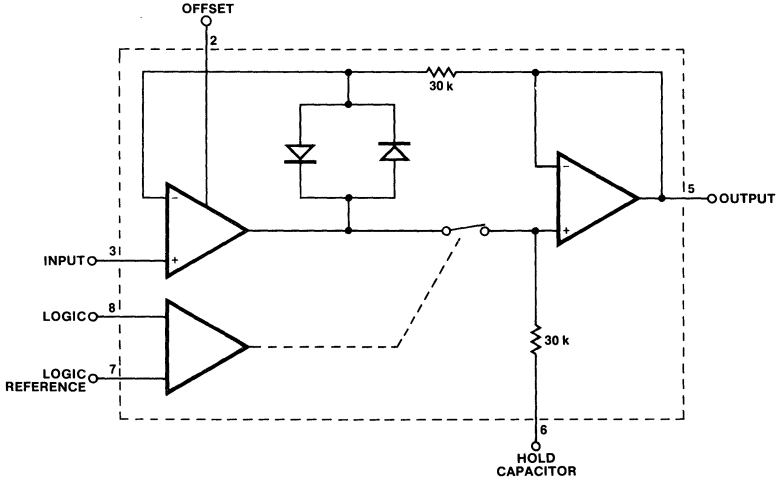
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μAF198	μAF198HM
μAF298	μAF298HC
μAF398	μAF398HC

FUNCTIONAL DIAGRAM



μA0801 (DAC-08) SERIES

8-BIT HIGH SPEED MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA0801A, μA0801H, μA0801, μA0801E and μA0801C are 8-bit multiplying Digital-to-Analog Converters constructed using the Fairchild Planar* epitaxial process. Advanced circuit design achieves very high speed performance with outstanding applications capability and low cost. The μA0801A and μA0801 are specified for the military temperature range (−55°C to +125°C) and the μA0801H, μA0801E and μA0801C are specified for 0°C to +70°C operation.

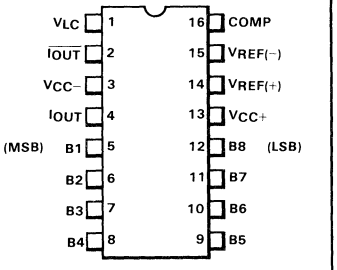
The μA0801 series are pin-for-pin replacements of the DAC-08 series.

- **FAST SETTLING TIME TO 1/2 LSB – 85 ns**
- **FULL SCALE CURRENT PREMATCHED TO ± 1 LSB**
- **DIRECT INTERFACE TO TTL, CMOS, ECL, HTL, PMOS, DTL**
- **LINEARITY TO ± 0.1% MAX OVER TEMPERATURE RANGE**
- **HIGH OUTPUT COMPLIANCE: −10 V TO +18 V**
- **TRUE AND COMPLEMENTED OUTPUTS**
- **WIDE RANGE MULTIPLYING CAPABILITY**
- **LOW FS CURRENT DRIFT: ±10 ppm/°C TYPICALLY**
- **WIDE POWER SUPPLY RANGE: ±4.5 V TO ± 18 V**
- **LOW POWER CONSUMPTION: 33 mW @ ±5 V**
- **EXTERNAL COMPENSATION FOR MAX BANDWIDTH**
- **LOW COST**

ABSOLUTE MAXIMUM RATINGS

$V_{CC}+$ to $V_{CC}-$	36 V
Logic Inputs	$V_{CC}-$ to $V_{CC}-$ plus 36 V
V_{LC}	$V_{CC}-$ to $V_{CC}+$
Reference Inputs (V_{14}, V_{15})	$V_{CC}-$ to $V_{CC}+$
Reference Input Differential Voltage (V_{14} to V_{15})	±18 V
Reference Input Current (I14)	5.0 mA
Power Dissipation	500 mW
Derate above 90°C (Hermetic DIP)	8.3 mW/°C
Derate above 80°C (Flatpak)	7.1 mW/°C
Operating Temperature Range	
μA0801, μA0801A	−55°C to +125°C
μA0801H, μA0801E, μA0801C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

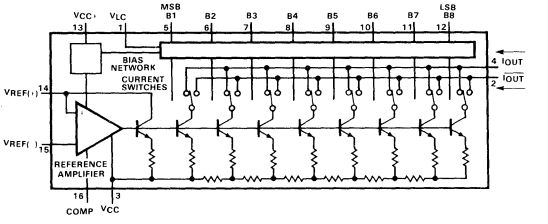
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODE D P F



ORDER INFORMATION

TYPE	PART NO.
μA0801A	μA0801AFM
μA0801A	μA0801ADM
μA0801	μA0801FM
μA0801	μA0801DM
μA0801H	μA0801HDC
μA0801H	μA0801HPC
μA0801E	μA0801EDC
μA0801E	μA0801EPC
μA0801C	μA0801CDC
μA0801C	μA0801CPC

EQUIVALENT CIRCUIT AND PIN CONNECTION DIAGRAM



*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: $T_A = 25°C$

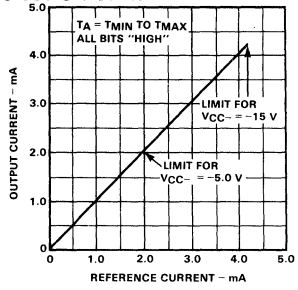
These specifications apply for $V_{CC} = \pm 15$ V, $I_{REF} = 2.0$ mA, $T_A = -55°C$ to $+125°C$ for μA0801A, μA0801, $T_A = 0°C$ to $70°C$ for μA0801H, μA0801E, μA0801C. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution			8	8	8	bits
	Monotonicity			8	8	8	bits
	Non-linearity	μA0801A, μA0801H				±0.1	%FS
		μA0801, μA0801E				±0.19	
		μA0801C				±0.39	
t_S	Settling Time	To ± ½ LSB, all bits switched ON or OFF $T_A = 25°C$	μA0801A, μA0801, μA0801A		85	135	ns
			μA0801E, μA0801C		85	150	
t_{PLH}, t_{PHL}	Propagation Delay	$T_A = 25°C$	Each bit		35	60	ns
			All bits switched		35	60	ns
TCI_{FS}	Full Scale Temperature Coefficient				±10	±50	ppm/°C
V_{OC}	Output Voltage Compliance	Full scale current change < ½ LSB, $R_{OUT} > 20$ mΩ		−10		+18	V
I_{FS4}	Full Scale Current	$V_{REF} = 10.000$ V, $R_{14}, R_{15} = 5.000$ kΩ $T_A = 25°C$	μA0801A, μA0801H,	1.984	1.992	2.000	mA
			μA0801E, μA0801, μA0801C	1.940	1.990	2.040	
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$	μA0801A, μA0801H		±0.5	±4.0	μA
			μA0801, μA0801E		±1.0	±8.0	
			μA0801C		±2.0	±16	
I_{ZS}	Zero Scale Current		μA0801A, μA0801H		0.1	1.0	μA
			μA0801, μA0801E		0.2	2.0	
			μA0801C		0.2	4.0	
I_{FSR}	Output Current Range	$V_{CC-} = -5.0$ V		0	2.0	2.1	mA
		$V_{CC-} = -7.0$ V to −18 V		0	2.0	4.2	mA
V_{IL}	Input LOW Voltage	$V_{LC} = 0$ V				0.8	V
V_{IH}	Input HIGH Voltage			2.0			V
I_{IL}	Input LOW Current	$V_{LC} = 0$ V $V_{IN} = -10$ V to +0.8 V			−2.0	−10	μA
I_{IH}	Input HIGH Current	$V_{IN} = 2.0$ V to 18 V			0.002	10	μA
V_{IS}	Logic Input Swing	$V_{CC-} = -15$ V		−10		+18	V
V_{THR}	Logic Threshold Range	$V_{CC} = \pm 15$ V		−10		+13.5	V
I_{15}	Reference Bias Current				−1.0	−3.0	μA
dI/dt	Reference Input Slew Rate			4.0	8.0		mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$V_{CC+} = 4.5$ V to 18 V			0.0003	0.01	%/%
$PSSI_{FS-}$		$V_{CC-} = -4.5$ V to −18 V $I_{REF} = 1.0$ mA			0.002	0.01	%/%
$I+$	Power Supply Current	$V_{CC} = \pm 5.0$ V, $I_{REF} = 1.0$ mA			2.3	3.8	mA
$I-$					−4.3	−5.8	mA
$I+$		$V_{CC+} = +5.0$ V, $V_{CC-} = -15$ V, $I_{REF} = 2.0$ mA			2.4	3.8	mA
$I-$					−6.4	−7.8	mA
$I+$		$V_{CC} = \pm 15$ V, $I_{REF} = 2.0$ mA			2.5	3.8	mA
$I-$					−6.5	−7.8	mA
P_D	Power Dissipation	$V_{CC} = \pm 5.0$ V, $I_{REF} = 1.0$ mA			33	48	mW
		$V_{CC+} = +5.0$V, $V_{CC-} = -15$ V, $I_{REF} = 2.0$ mA			108	136	mW
		$V_{CC} = \pm 15$ V, $I_{REF} = 2.0$ mA			135	174	mW

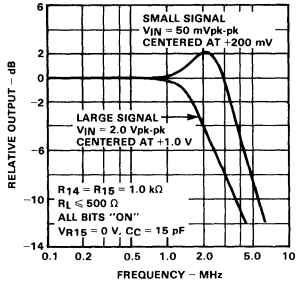
5

TYPICAL PERFORMANCE CURVES

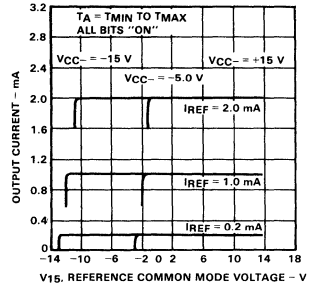
FULL SCALE CURRENT AS A FUNCTION OF REFERENCE CURRENT



REFERENCE INPUT FREQUENCY RESPONSE

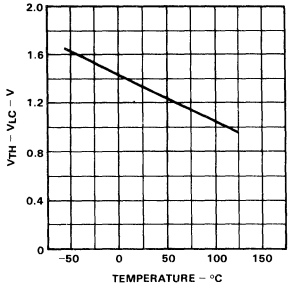


REFERENCE AMP COMMON MODE RANGE

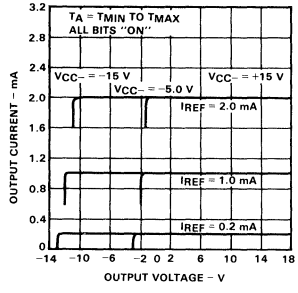


NOTE: POSITIVE COMMON MODE RANGE IS ALWAYS (V_{CC+}) −1.5 V

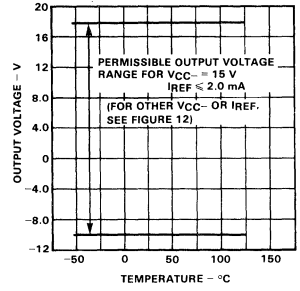
$V_{TH} - V_{LC}$ AS A FUNCTION OF TEMPERATURE



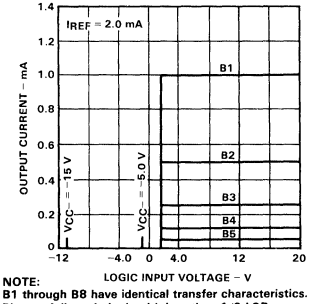
OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



OUTPUT VOLTAGE COMPLIANCE AS A FUNCTION OF TEMPERATURE

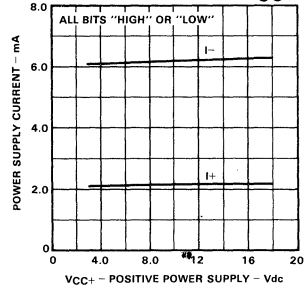


BIT TRANSFER CHARACTERISTICS

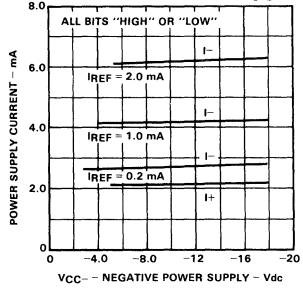


NOTE:
B1 through B8 have identical transfer characteristics. Bits are fully switched, with less than 1/2 LSB error. At less than ±100 mV from actual threshold, these switching points are guaranteed to lie between 0.8 and 2.0 V over the operating temperature range (V_{LC} = 0.0 V)

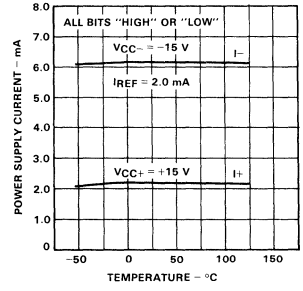
POWER SUPPLY CURRENT AS A FUNCTION OF V_{CC+}



POWER SUPPLY CURRENT AS A FUNCTION OF V_{CC-}



POWER SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



TEST CIRCUITS

BASIC POSITIVE REFERENCE OPERATION

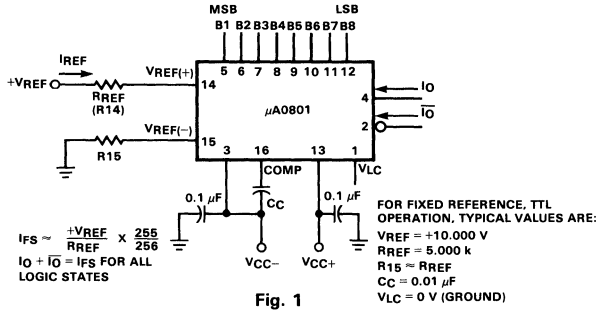


Fig. 1

RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

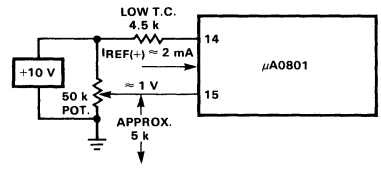
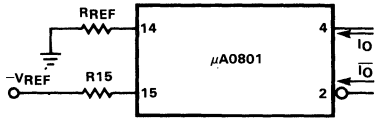


Fig. 2

BASIC NEGATIVE REFERENCE OPERATION

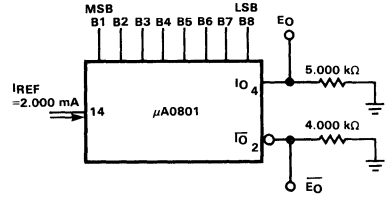


$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

NOTE:
R_{REF} sets I_{FS}; R15 is for bias current cancellation.

Fig. 3

BASIC UNIPOLAR NEGATIVE OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	.000	−9.960	.000
Full Scale − LSB	1	1	1	1	1	1	1	0	1.984	.008	−9.920	−.040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	.992	−5.000	−4.960
Half Scale − LSB	0	1	1	1	1	1	1	1	.992	1.000	−4.960	−5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	.008	1.984	−.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	.000	1.992	.000	−9.960

Fig. 4

HIGH NOISE IMMUNITY CURRENT TO VOLTAGE CONVERSION

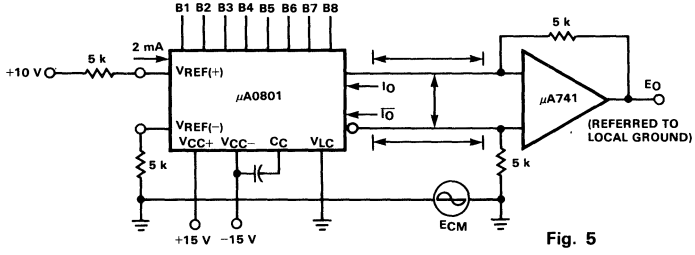


Fig. 5

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos Full Scale − LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	−9.840
Neg Full Scale	0	0	0	0	0	0	0	0	−9.920

- Provides isolation from ground loops
- Symmetrical ±10 V output
- Useful within systems between boards
- True complementary/differential current transmission
- High speed analog signal transmission

BASIC BIPOLAR OUTPUT OPERATION

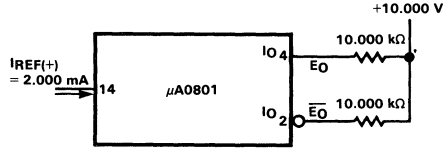
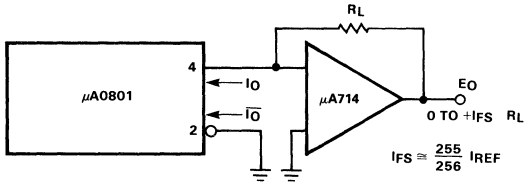


Fig. 6

	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos Full Scale − LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale − LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

TEST CIRCUITS (Cont'd)

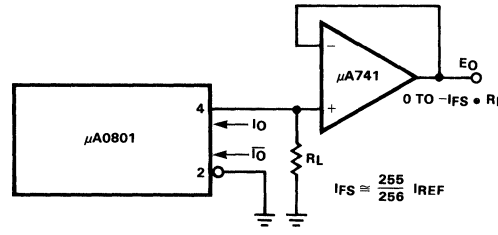
POSITIVE LOW IMPEDANCE OUTPUT OPERATION



For complementary output (operation as negative logic DAC), connect inverting input of Op-Amp to $\overline{IO}$ (Pin 2); connect IO (Pin 4) to ground.

Fig. 7

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



For complementary output (operation as a negative logic DAC), connect non-inverting input of Op-Amp to $\overline{IO}$ (Pin 2); connect IO (Pin 4) to ground.

Fig. 8

PULSED REFERENCE OPERATION

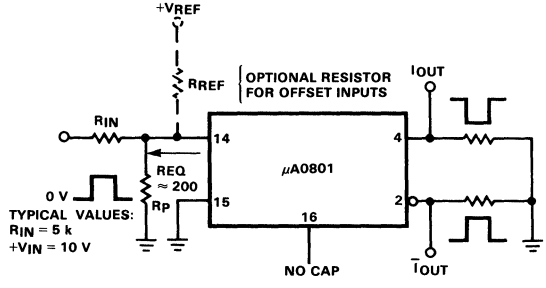


Fig. 9

ACCOMMODATING BIPOLAR REFERENCES

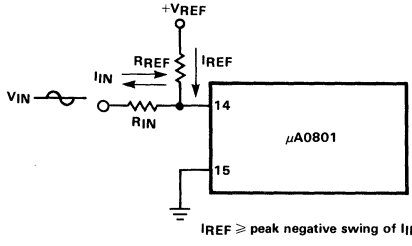


Fig. 10a

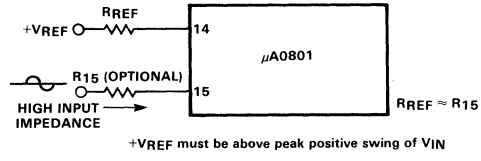


Fig. 10b

TEST CIRCUITS (Cont'd)

INTERFACING WITH VARIOUS LOGIC FAMILIES

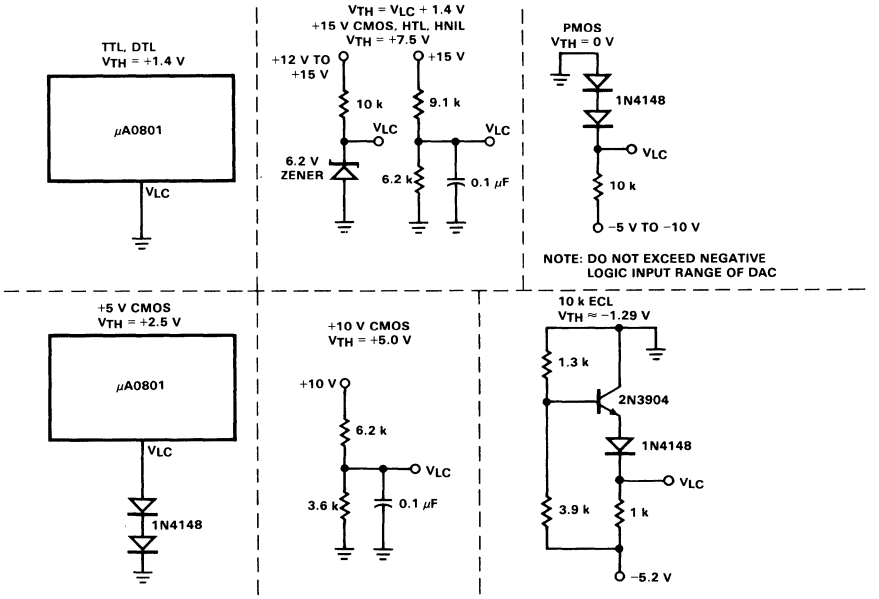


Fig. 11

SETTLING TIME MEASUREMENT

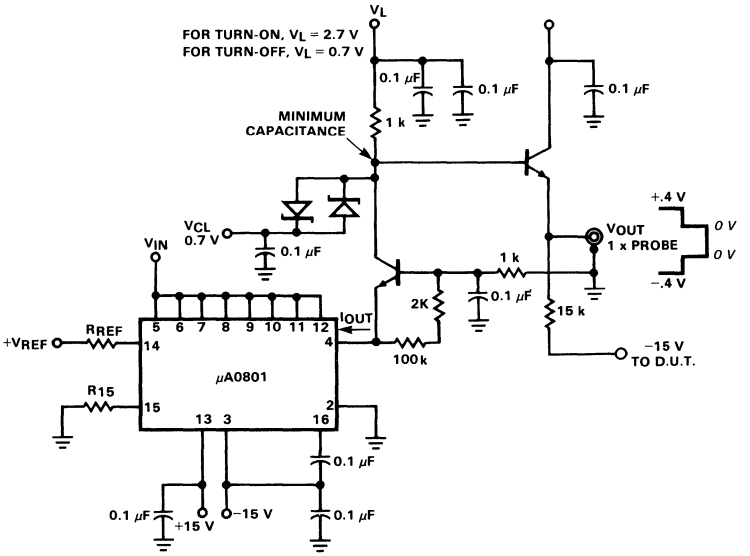


Fig. 12

μA0802 (MC1508/1408) SERIES

8-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA0802, μA0802H, μA0802A, μA0802B, and μA0802C are monolithic 8-bit multiplying Digital-to-Analog Converters constructed using the Fairchild Planar* epitaxial process. It is designed for use where the output current is a linear product of an 8-bit digital word and an analog input voltage. The μA0802 is specified for the military temperature range (−55°C to +125°C) and the μA0802H, μA0802A, μA0802B and μA0802C are specified for 0°C to 70°C operation.

The μA0802 series are pin-for-pin replacements of the MC1508/1408 devices.

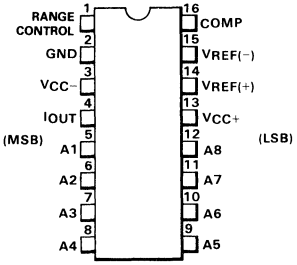
- **RELATIVE ACCURACY: ±0.1% ERROR MAXIMUM μA0802H**
- **RELATIVE ACCURACY: ±0.19% ERROR MAXIMUM μA0802, μA0802A**
- **7 AND 6-BIT ACCURACY AVAILABLE μA0802B, μA0802C**
- **FAST SETTLING TIME TO 1/2 LSB – 85 ns**
- **NON-INVERTING DIGITAL INPUTS ARE TTL AND CMOS COMPATIBLE**
- **OUTPUT VOLTAGE SWING: +0.5 V TO −5.0 V**
- **HIGH-SPEED MULTIPLYING INPUT SLEW RATE 4.0 mA/μs**
- **STANDARD SUPPLY VOLTAGES: +5.0 V AND −5.0 V TO −15 V**
- **LOW FS CURRENT DRIFT: +10 PPM/°C TYPICALLY**
- **LOW POWER CONSUMPTION: 33 mW @ ±5 V**
- **LOW COST**

ABSOLUTE MAXIMUM RATINGS: T_A = +25°C unless otherwise noted

V_{CC}+	5.5 V_{dc}
V_{CC}−	−16.5 V_{dc}
Digital Input Voltage (V5 to V12)	+5.5 V_{dc}
Applied Output Voltage	0.5 V_{dc} to −5.2 V_{dc}
Reference Current (I14)	5.0 mA
Reference Amplifier Inputs (V14, V15)	5.5 V_{dc}, −16.5 V_{dc}
Operating Temperature Range	
μA0802	−55°C to +125°C
μA0802H, μA0802A, μA0802B, μA0802C	0°C to +70°C
Storage Temperature Range	
Pin Temperatures	
Hermetic DIP, Flatpack (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

CONNECTION DIAGRAM
16-PIN

(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
μA0802	μA0802FM
μA0802	μA0802DM
μA0802H	μA0802HDC
μA0802H	μA0802HPC
μA0802A	μA0802ADC
μA0802A	μA0802APC
μA0802B	μA0802BDC
μA0802B	μA0802BPC
μA0802C	μA0802CDC
μA0802C	μA0802CPC

TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

ADDITIONAL ORDER INFORMATION

TYPE	TEMPERATURE RANGE	RELATIVE ACCURACY
μA0802H	0°C to +70°C	±0.1 %
μA0802 (MC1508L-8)	−55°C to +125°C	±0.19 %
μA0802A (MC1408L-8)	0°C to +70°C	±0.19 %
μA0802B (MC1408L-7)	0°C to +70°C	±0.39 %
μA0802C (MC1408L-6)	0°C to +70°C	±0.78 %

* Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: V_{CC+} = +5.0 V, V_{CC-} = − 15 V, V_{REF}/R14 = 2.0 mA, μA0802 T_A = −55°C to 125°C. μA0802H/A/B/C, T_A = 0°C to 70°C, unless otherwise noted. All digital inputs at high logic level.

SYMBOL	CHARACTERISTICS	FIGURE	MIN	TYP	MAX	UNITS
E_r	Relative Accuracy (Error Relative to Full Scale I_O	3				%
	μA0802H				±0.1	
	μA0802, μA0802A		–	–	±0.19	
	μA0802B, See Note 1		–	–	±0.39	
	μA0802C, See Note 1				±0.78	
t_s	Setting Time to Within 1/2 LSB (includes t_{PLH}) (T_A = +25 'C) See Note 2	4	–	85	135	ns
t_{PLH},t_{PHL}	Propagation Delay Time T_A = +25°C	4	–	30	100	ns
TCI_O	Output Full Scale Current Drift		–	±20	–	PPM°C
	Digital Input Logic Levels (MSB)	2				V
V_{IH}	High Level, Logic "1"		2.0	–	–	
V_{IL}	Low Level, Logic "0"		–	–	0.8	
	Digital Input Current (MSB)	2				mA
I_{IH}	High Level, V_{IH} = 5.0 V		–	0	0.04	
I_{IL}	Low Level, V_{IL} = 0.8 V		–	−0.4	−0.8	
I_{15}	Reference Input Bias Current (Pin 15)	2	–	−1.0	−5.0	μA
I_{OR}	Output Current Range	2				
	V_{CC} = −5.0 V		0	2.0	2.1	mA
	V_{CC} = −6.0 to −15 V		0	2.0	4.2	
I_O	Output Current	2				mA
	V_{REF} = 2,000 V, R14 = 1000 Ω		1.9	1.99	2.1	mA
$I_{O(min)}$	Output Current (All bits low)	2	–	0	4.0	μA
V_O	Output Voltage Compliance	2				V
	($E_r \leq 0.19$: at T_A = +25°C)					
	V_{CC-} = −5 V		–	–	−0.6,+0.5	
	V_{CC-} below −10 V		–	–	−5.0,+0.5	
SR I_{REF}	Reference Current Slew Rate	5	–	4.0	–	mA/μs
PSRR(−)	Output Current Power Supply Sensitivity		–	0.5	2.7	μA/V
I_{CC+}	Power Supply Current	2	–	+13.5	+22	mA
I_{CC-}	(All bits low)		–	−7.5	−13.0	
V_{CCR+}	Power Supply Voltage Range	2	+4.5	+5.0	+5.5	V
V_{CCR-}	(T_A = +25°C)		−4.5	−15	−16.5	
P_D	Power Dissipation	2				mW
	All bits low					
	V_{CC-} = −5.0 V		–	105	170	
	V_{CC-} = −15 V		–	190	305	
	All bits high					
	V_{CC-} = −5.0 V		–	90	–	
	V_{CC-} = −15 V			160	–	

NOTES:
1. All current switches are tested to guarantee at least 50% of rated output current.
2. All bits switched.

TYPICAL APPLICATIONS

μA0802
EQUIVALENT CIRCUIT

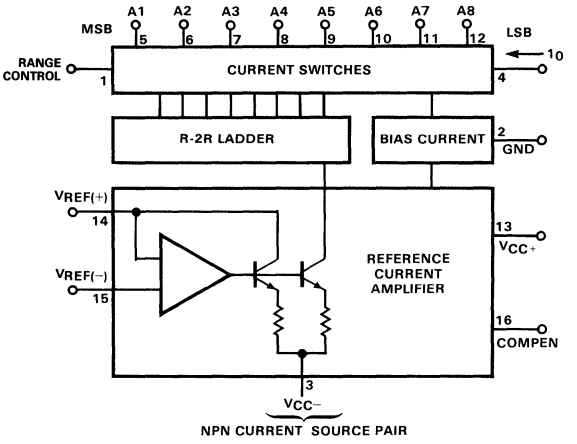
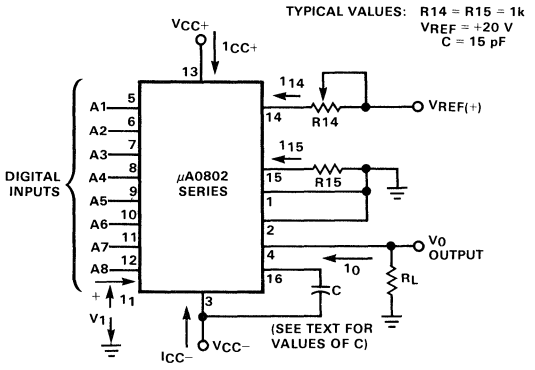


Fig. 1

NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right\}$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

Fig. 2

TYPICAL APPLICATIONS (Cont'd)

RELATIVE ACCURACY TEST CIRCUIT

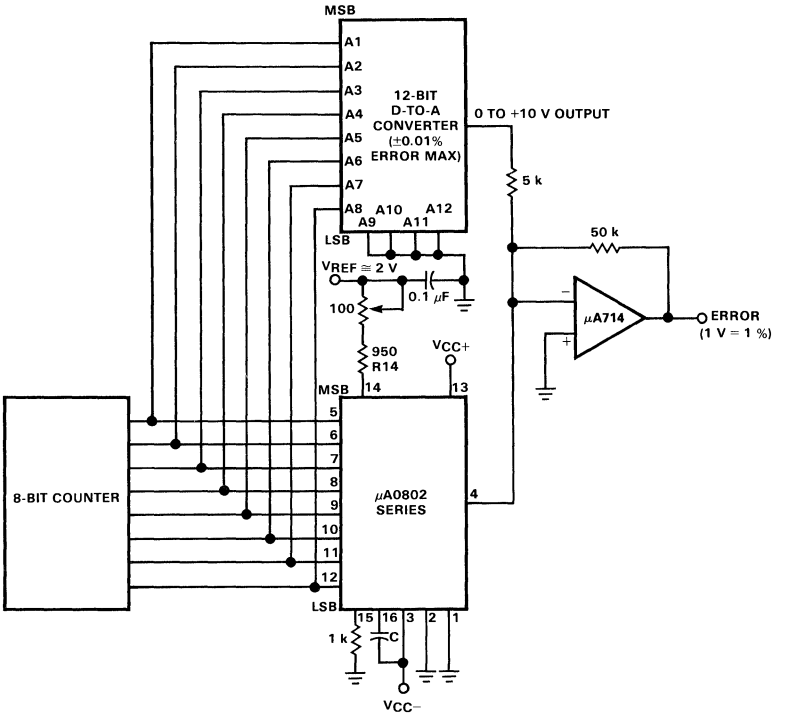


Fig. 3

TRANSIENT RESPONSE AND SETTLING TIME

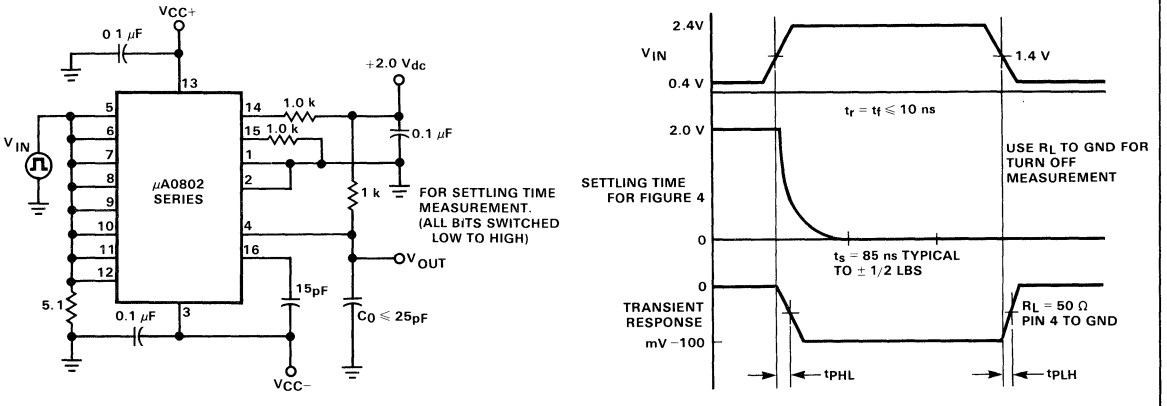


Fig. 4

TYPICAL APPLICATIONS (Cont'd)

POSITIVE V_{REF}

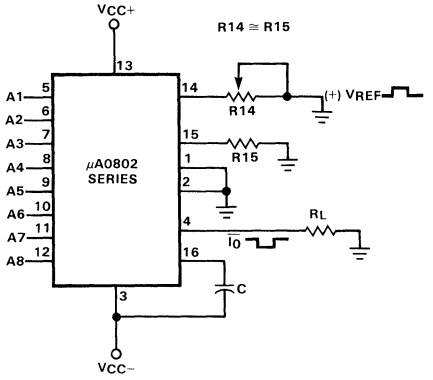


Fig. 5

NEGATIVE V_{REF}

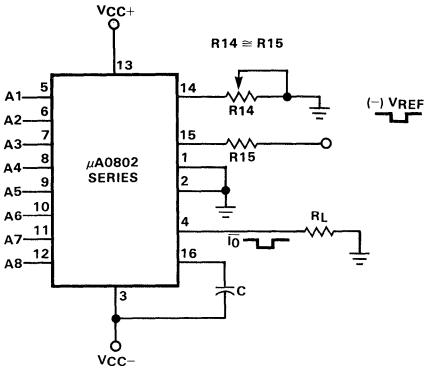
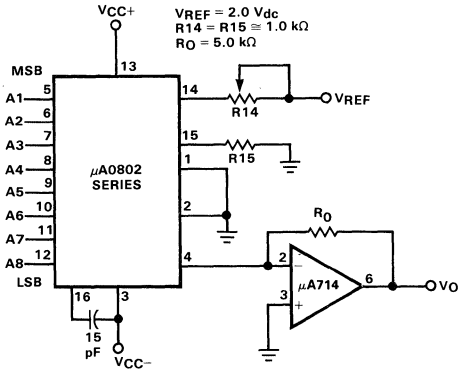


Fig. 6

USE WITH CURRENT–TO–VOLTAGE CONVERTING OP AMP



THEORETICAL V_O

$$V_O = \frac{V_{REF}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

ADJUST V_{REF} R14 OR R_O SO THAT V_O WITH ALL DIGITAL INPUTS AT HIGH LEVEL IS EQUAL TO 9.961 VOLTS.

$$V_O = \frac{2\text{ V}}{1\text{ k}}(5\text{ k})\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\text{ V}\ \frac{255}{256} = 9.961\text{ V}$$

Fig. 7

μA4151 • μA7151

VOLTAGE-TO-FREQUENCY CONVERTERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

DESCRIPTION – The μA4151 is a monolithic building block used to convert dc voltage to digital pulses. The frequency of the output pulses is proportional to the dc input voltage.

The μA4151 consists of a voltage comparator, a monostable multivibrator and a precision switched current source (see block diagram).

The μA7151 is the same device as the μA4151 with a high performance operational amplifier on the same chip. The single supply op amp conditions the input signal and provides a significant improvement in system performance.

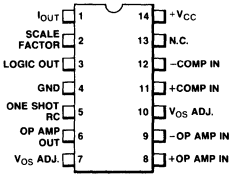
- **SINGLE SUPPLY (+8 V_{DC} TO +30 V_{DC})**
- **LINEARITY TO ±0.05%**
- **PROGRAMMABLE SCALE FACTOR**
- **PULSE OUTPUT COMPATIBLE WITH ANY LOGIC FORM**
- **TEMPERATURE STABILITY TYPICALLY ±100 ppm/°C**
- **HIGH NOISE REJECTION**
- **EASILY TRANSMITTABLE OUTPUT**
- **SIMPLE FULL-SCALE TRIM**
- **SINGLE-ENDED INPUT, REFERENCED TO GROUND**
- **ALSO PROVIDES FREQUENCY-TO-VOLTAGE CONVERSION**
- **HIGH PERFORMANCE OP AMP INCLUDED IN μA7151**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	32 V
Internal Power Dissipation	670 mW
Input Voltage (Comparator)	−0.2 V to $+V_{CC}$
Input Voltage (Op Amp)	−0.2 V to $+V_{CC}$
Logic Out Shorted-to-Ground	continuous
Op Amp Out Shorted-to-Ground	continuous
Op Amp Input Common Mode Voltage Range	+13 V to $-V_S$
Op Amp Output Voltage Range, R_L = 10 kΩ	+2 V to +13 V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperatures	
Molded DIP (Soldering, 10 s)	260°C
Hermetic DIP (Soldering, 60 s)	300°C

CONNECTION DIAGRAMS

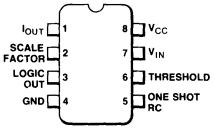
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA7151	μA7151PC

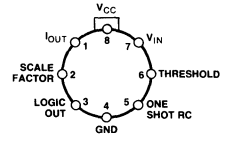
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINES 9T
PACKAGE CODES T



ORDER INFORMATION

TYPE	PART NO.
μA4151	μA4151TC

8-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA4151	μA4151HC

ELECTRICAL CHARACTERISTICS: V_{CC} = +15 V, T_A = 25°C unless otherwise specified.
The following specs apply to the Converter Section only.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	8.0 V ≤ V_{CC} ≤ 15 V	3.0	4.5	7.0	mA
	15 V ≤ V_{CC} ≤ 22 V	3.0	5.5	8.5	
	22 V ≤ V_{CC} ≤ 30 V	3.0	6.5	10.5	
Conversion Accuracy					
Scale Factor	Figure 2, V_1 = 10 V, R_S = 14 kΩ	0.90	1.0	1.10	kHz/V
Drift with Temperature	Figure 2, V_1 = 10 V		±100		ppm/°C
Drift with V_{CC}	Figure 2, 8.0 V ≤ V_{CC} ≤ 18 V, V_1 = 1.0 V		0.2	1.0	%/V
Input Comparator					
Offset Voltage			5.0	10	mV
Offset Current			±50	±100	nA
Input Bias Current			−100	−300	nA
Common Mode Range (Note 1)		0	0 to V_{CC}−2	V_{CC}−3.0	V
One-Shot					
Threshold Voltage, Pin 5		0.63	0.667	0.70	xV_{CC}
Input Bias Current, Pin 5			−100	−500	nA
Reset V_{sat}	Pin 5, I = 2.2 mA		0.15	0.50	V
Current Source					
Output Current (V_S−14 kΩ)	Pin 1, Figure 1, V = 0		138.7		μA
Change with Voltage	Pin 1, V = 0 V to V = 10 V		1.0	2.5	μA
Off Leakage	Pin 1, V = 0 V		1.0	50	nA
Reference Voltage	Pin 2, Figure 1	1.70	1.9	2.08	V
Logic Output					
V_{sat}	Pin 3, I = 3.0 mA		0.15	0.50	V
V_{sat}	Pin 3, I = 2.0 mA		0.10	0.35	V
Off Leakage			0.1	1.0	μA

NOTE 1: Input common mode range includes ground.

μA7151 Op-Amp

ELECTRICAL CHARACTERISTICS: V_S = +15 V and ground T_A = 25°C unless otherwise specified.

CHARACTERISTICS	MIN	TYP	MAX	UNITS
Input Offset Voltage		2.0	5.0	mV
Input Offset Current		10	50	nA
Input Bias Current		−50	−250	nA
Input Impedance		1.0		MΩ
Common Mode Rejection Ratio	70	90		dB
Large Signal Voltage Gain, R_L = 10 k	50	200		V/mV
Slew Rate		0.6		V/μs
Power Supply Rejection Ratio		15	100	μV/V
Output Short Circuit Current	10		40	mA

CIRCUIT DESCRIPTION

The μA7151 consists of five circuit blocks as shown in Figure 1. The blocks may be connected in a variety of ways to construct voltage-to-frequency converters (VFC), frequency-to-voltage cqnverters (FVC), or other circuit functions. The circuit blocks are:

1. A differential input comparator featuring very high gain, low offsets, and a common mode range which includes ground.
2. A one-shot multivibrator with the time constant set by an external RC (T = 1.1RC) connected to the RC terminal, triggered by the output of the comparator being high.
3. A precision switched current source that is turned on to the value of I_{REF} when the one-shot is on and goes to zero when the one-shot is off. The current I_{REF} is set by an external R_S, connected from the scale factor terminal-to-ground and is equal to the reference voltage divided by R_S and is optimized when set to 138 μA.
4. An open collector output that provides a buffered output from the one-shot.
5. An operational amplifier whose common mode range includes ground and has offset null capability. The op amp has high gain, low offset voltage, low input currents, good PSRR and CMRR, and low drift.

PRINCIPLE OF OPERATION

Voltage to Frequency Conversion (VFC)

As a voltage to frequency converter the μA7151/4151 can be connected in several configurations depending on the input voltage, required accuracy, and response time. In all the applications we will see that the input voltage is converted to a current and the circuit will turn the switched current source on at the rate necessary so that the average current from the current source is equal to the input current. As the input voltage (and current) increases, the current source must turn on more often, and the output frequency increases.

SELECTING COMPONENTS FOR THE VFC

Voltage-to-frequency converters can be used for full scale voltages of 100 mV or greater and full scale frequencies of 1 Hz to 100 kHz. Input voltages in excess of $V_{CC}+$ can be accommodated with appropriate resistor dividers to attenuate the voltages. The following components selection guidelines should be used.

1. R_S should be approximately 14 kΩ to optimize the system performance versus temperature. R_S is normally a 12 kΩ fixed resistor and a 5 kΩ pot to be used to adjust the full scale output frequency. Small variations in R_S have minimal effect on system temperature performance. $I_{REF} = V_{REF}/R_S = 1.95\ V/R_S$
2. $R_0\ C_0$ séts the one-shot pulse width, $T_0 = 1.1\ R_0\ C_0$. This pulse width must be shorter than the minimum period of the maximum frequency ie, set it equal to .75 $(1/f_0)$. Therefore, $R_0\ C_0 = .68\ (1/f_0)$. Values of R_0 should be between 6.8 kΩ and 680 kΩ and C_0 should be from .001 μF to 1 μF.
3. R_B should be as low as possible for the highest accuracy, (this reduces the effect of current source R_{OUT}) but must be large enough to insure that the current source output is greater than $V_{IN}\ max/R_B$. Therefore, choose R_B such that $R_B \sim 1.33\ V_{IN}\ max/I_0$.
4. C_B for Figure 2 must be chosen to trade-off between accuracy and response time. Larger values of C_B give greater system accuracy but response time is limited by the $R_B\ D_B$ time constant. A good choice for D_B is $10^{-2}/f_0$.
5. C_1 for Figures 3 and 4 can be selected depending on the output frequency. The smaller C_1 is the faster the system response wil be. C_1 must be large enough to limit the amplifier swing. The op amp will swing a voltage set by I_0T_0/C_1, so if the comparator is biased at 2/3 $V_{CC}+$ this constrains $C_1 > 3\ I_0T_0/2\ V_{CC}+$. A nominal value of $C_1 = 5 \times 10^{-5}/f_0$ meets this requirement.

COMPARISON OF VOLTAGE TO FREQUENCY CIRCUITS

Table I shows a comparison of the three basic circuits set-up for a 0 to 10 V input range and a full scale output of 10 kHz.

FREQUENCY TO VOLTAGE CONVERSION

The μA7151/4151 can be connected as frequency-to-voltage converter (FVC). This circuit basically works by putting out a current pulse per cycle of input frequency and intergrating the current pulses across an output resistor to give an output voltage which is proportional to the average value of I_0 $(I_0T_0f_{IN})$.

TABLE I – APPLICATIONS

	Figure 2	Figure 3	Figure 4
Linearity	1.0%	0.2%	0.05%
Frequency Offset	+10 Hz	0	0
Response Time	135 μs	200 μs	10 μs
Input Voltage	+	+	–
Single Supply	yes	yes	yes
Split Supply	–	–	yes

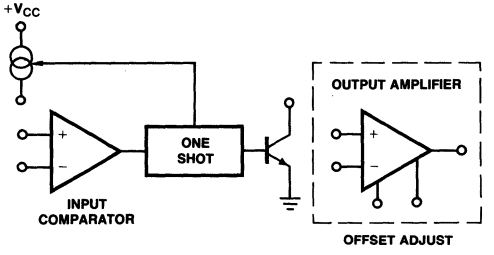


Fig. 1

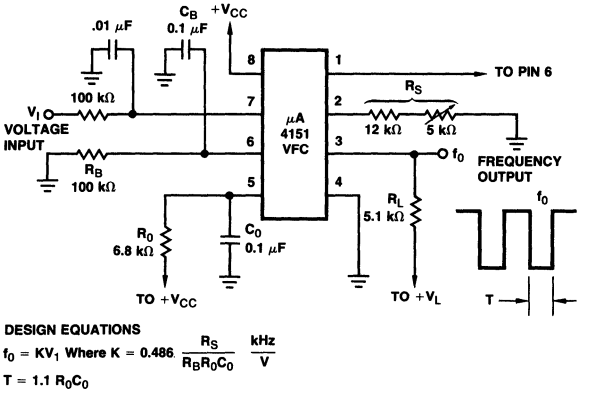


Fig. 2

PRECISION VOLTAGE TO FREQUENCY CONVERTER FOR POSITIVE INPUTS

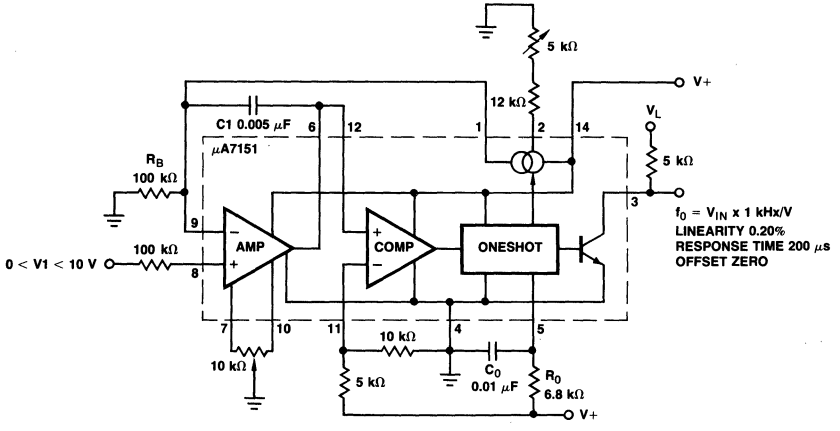


Fig. 3

PRECISION VOLTAGE TO FREQUENCY CONVERTER FOR NEGATIVE INPUTS

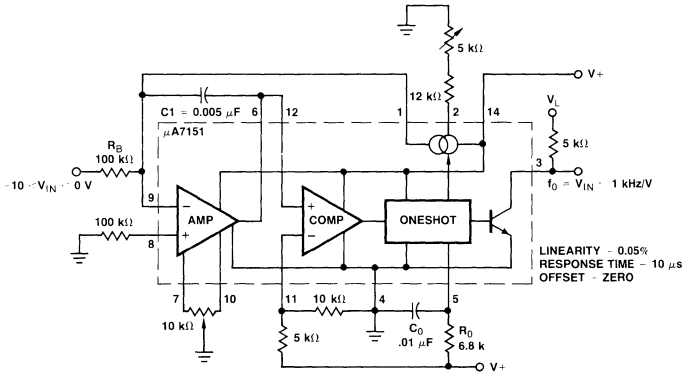


Fig. 4

SINGLE SUPPLY FREQUENCY-TO-VOLTAGE CONVERTER

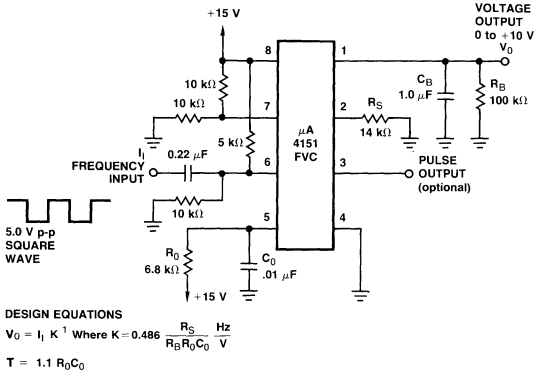


Fig. 5

PRECISION FREQUENCY TO VOLTAGE CONVERTER

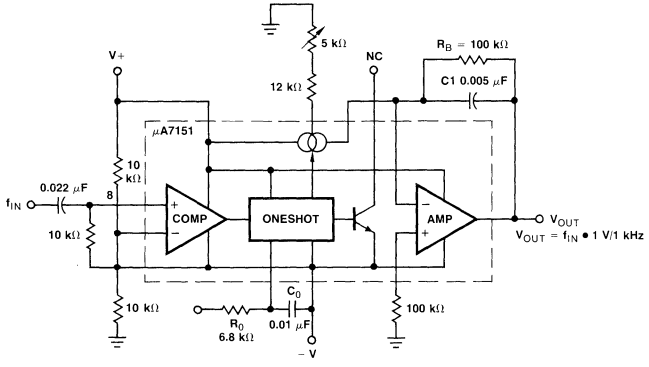


Fig. 6

LOW COST, REMOTE SENSED 8-BIT A/D CONVERTER

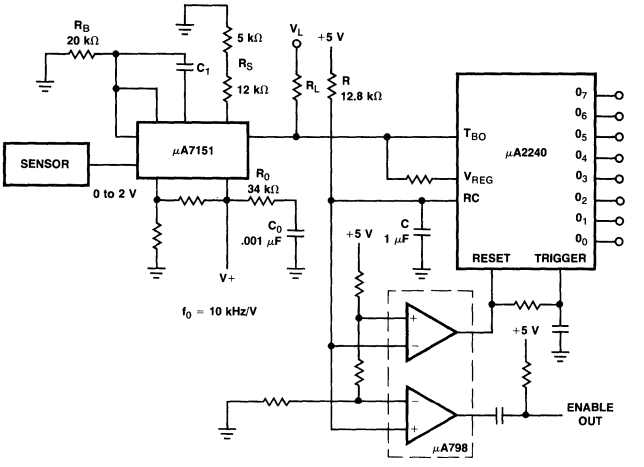


Fig. 7

MOTOR SPEED CONTROLLER

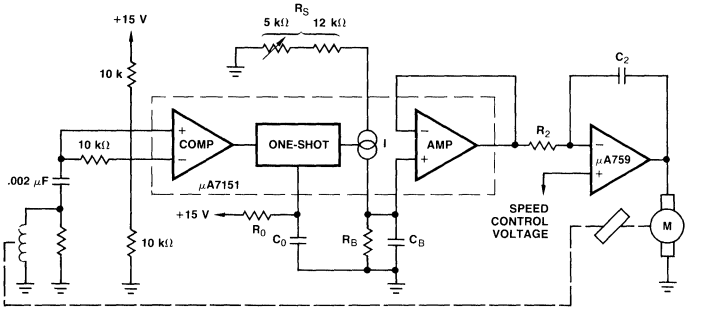


Fig. 8

FSK DEMODULATOR

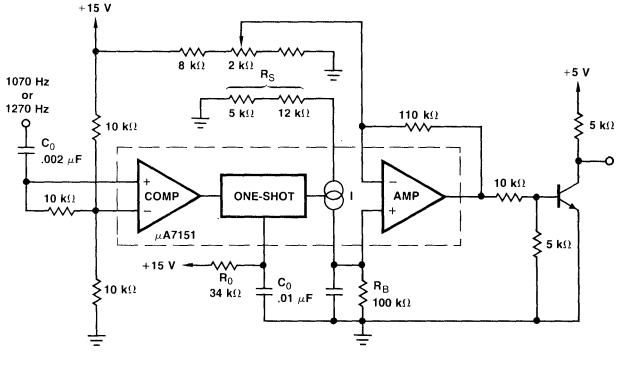


Fig. 9

μA9706 • μA9706A

MULTI-CHANNEL, 12-BIT ACCURATE, μP COMPATIBLE, D/A CONVERTERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

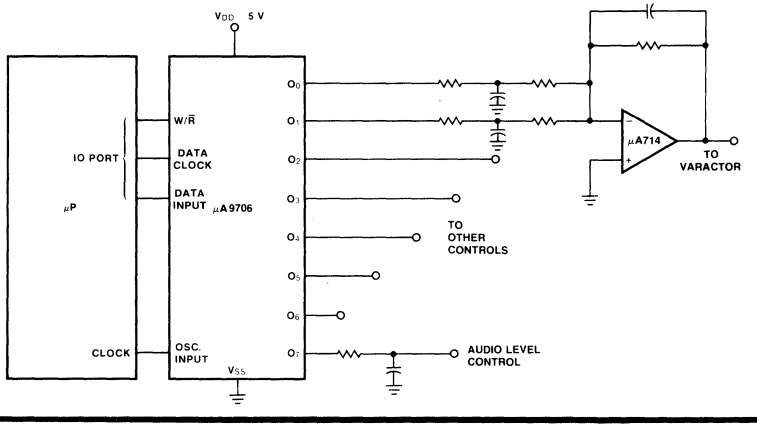
GENERAL DESCRIPTION — The μA9706 and μA9706A are digital-to-analog-converters which allow a microprocessor system to interface and control analog systems. The μA9706 is programmed by 9-bit words, accepted in a serial format, while the μA9706A accepts 9-bit words in parallel 3-bit groups. Both the μA9706 and μA9706A provide conversions on all channels simultaneously and continuously as long as the oscillator signal is present. Digital-to-analog conversion is accomplished using a pulse-width ratio technique for directly controlling the duty cycle of the output pulse streams. Each channel, when appropriately filtered, supplies 6-bit resolution, or 64 discrete analog levels. By properly summing two outputs, the resolution may be controlled up to 12 bits, or 4096 discrete levels. The μA9706 provides 8-channel operation, whereas the μA9706A provides 7-channel operation. Each channel output maintains 12-bit, or ±.01% full-scale, accuracy.

- **MICROPROCESSOR COMPATIBLE**
- **CMOS TECHNOLOGY**
- **LOW COST**
- **8 CHANNELS (μA9706), 7 CHANNELS (μA9706A)**
- **LINEARITY ±0.01%**
- **EXPANDABLE TO 12-BIT RESOLUTION**
- **INTERNAL MEMORY**
- **SINGLE SUPPLY (+5 V)**
- **EXCELLENT STABILITY — NO ADJUSTMENTS**
- **SUITED FOR BUS ORIENTED APPLICATIONS**
  μA9706 — SERIAL INPUT FORMAT
  μA9706A — PARALLEL INPUT FORMAT

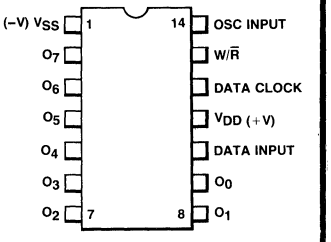
APPLICATIONS

- **Remote Control TV — Tuning, Volume, Color Contrast, Intensity, Hue**
- **Remote Control Audio Systems — Stereo Quadraphonic**
- **Microprocessor Control Systems — Games, Toys Appliances Automotive Industrial Processes Instrumentation**

VARACTOR TUNED 12-BIT RECEIVER SYSTEM



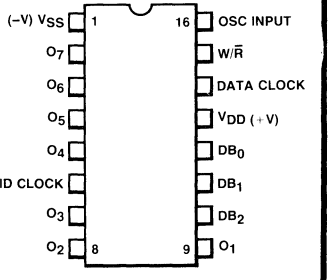
CONNECTION DIAGRAM
μA9706
14-PIN DIP PACKAGE
(TOP VIEW)
PACKAGE OUTLINES 7A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA9706	μA9706PC
μA9706	μA9706DC

CONNECTION DIAGRAM
μA9706A
16-PIN PACKAGE
(TOP VIEW)
PACKAGE OUTLINES 7B 9B
PACKAGE CODES D P

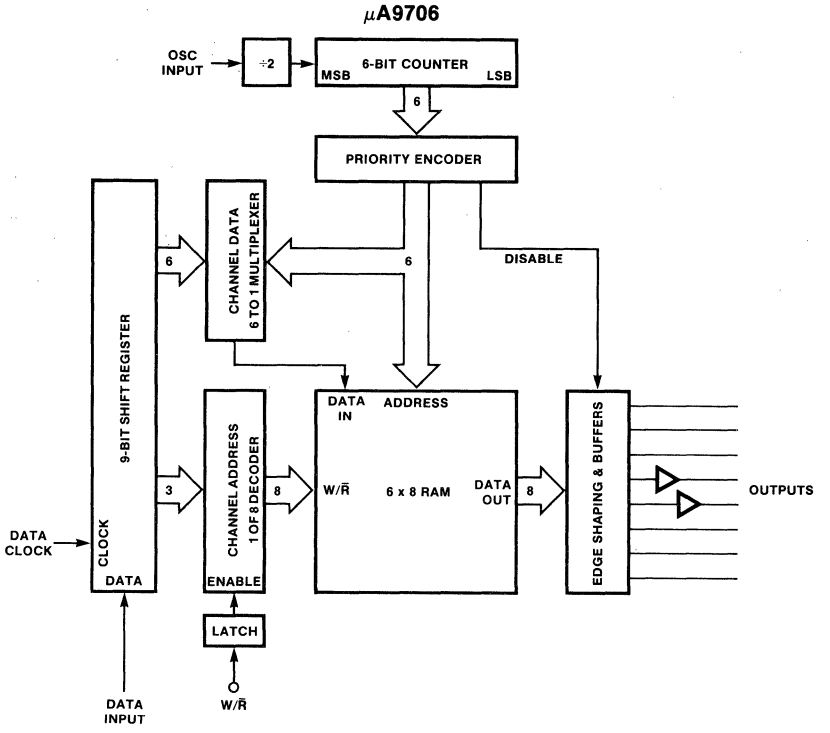


ORDER INFORMATION

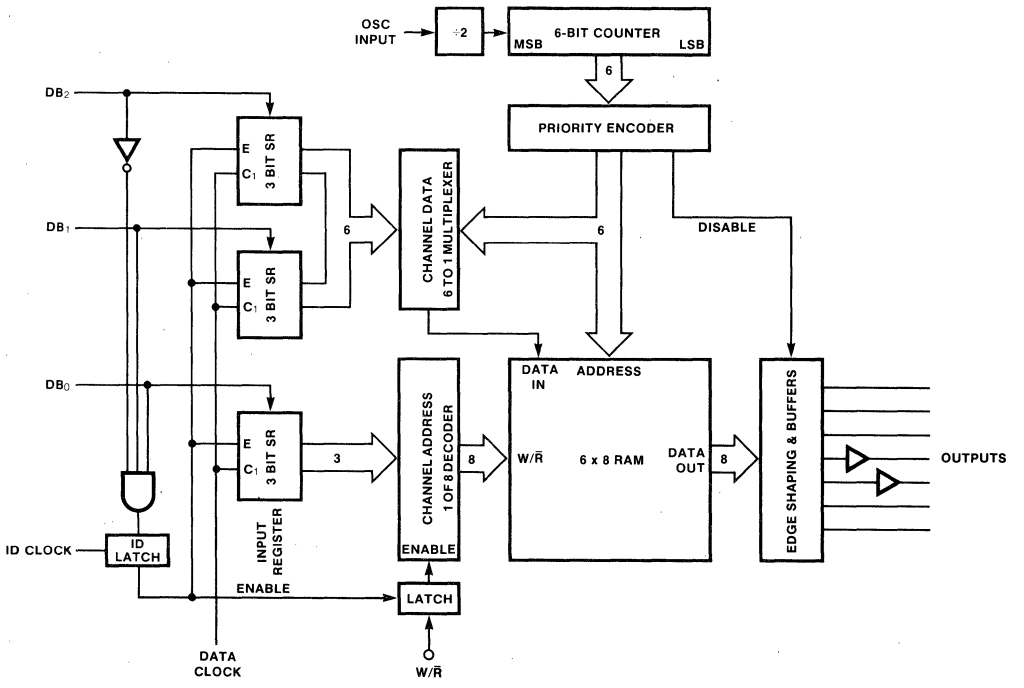
TYPE	PART NO.
μA9706A	μA9706APC
μA9706A	μA9706ADC

FUNCTIONAL DIAGRAMS

μA9706



μA9706A



ABSOLUTE MAXIMUM RATINGS

V_{DD} Relative to V_{SS}	−0.3 V to 5.5 V
Digital Input Range	−0.3 V to V_{DD} +0.3 V
Output Sink or Source Current	25 mA
Operating Temperature	0°C to 85°C
Storage Temperature	−65°C to +150°C
Pin Temperature (Soldering, 10 s)	260°C

ELECTRICAL CHARACTERISTICS: V_{DD} = +5 V, V_{SS} = 0 V, T_A = 0°C to +70°C, f_{osc} = 100 kHz

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS
R_O	Output Resistance (Channels 4 & 5)		30	50	Ω
R_O	Output Resistance (Channels 0, 1, 2, 3, 6, 7)		300	1000	Ω
f_{osc}	Oscillator Frequency	50		2000	kHz
t_H	Data Clock HIGH Time	4			μs
t_L	Data Clock LOW Time	4			μs
$t_{W/R}$	W/$\overline{R}$ Pulse Width	4		$128/f_{osc}$	μs
Error	Linearity			0.01	%
V_{IH}	Voltage Input HIGH			2.7	V
V_{IL}	Voltage Input LOW	0.8			V
I_{DD}	Power Supply Current		40	200	μA
I_{IN}	Input Current			50	μA
C_{IN}	Input Capacitance		8		pF
t_r	Input Rise Time			1.0	μs
t_f	Input Fall Time			1.0	μs
t_s	Input Set-up Time			1.0	μs

FUNCTIONAL DESCRIPTION

The functional blocks of the μA9706 and μA9706A are defined by the pulse-width ratio conversion scheme that they employ. In addition, other requirements which include microprocessor compatibility, multi-channel operation, and simultaneous conversion of all channels add to the basic structure. The μA9706 consists of seven functional blocks: a 6-bit binary counter, a pulse distributor called a priority encoder, 6 x 8 RAM, 1-of-8 channel address decoder, 6-to-1 channel-data multiplexer, 9-bit input shift register, and a set of eight output buffers.

The pulse-width-ratio conversion scheme divides the conversion cycle into binary-weighted time intervals and associates each time interval with a bit position in the 6-bit control word. The control word residing in RAM is then addressed, bit by bit, each bit addressed for the associated time interval. The value of each bit, "1" or "0", controls the output, HIGH or LOW, during this time interval *(see Figure 1)*. In this manner, an output pulse stream is generated with a duty cycle defined by the control word. When the pulse stream is filtered, a dc value is extracted that is proportional to the duty cycle of the pulse stream and, hence, proportional to the control word.

The 6-bit counter generates the fundamental time intervals for the system and may be driven by any open-collector TTL or CMOS logic that produces a square-wave signal with a frequency in the range of 50 kHz to 2 MHz. The time intervals (binary-weighted pulse widths) generated by the counter are decoded by the priority encoder which serves two functions. First, it ensures that each of the six time intervals (control pulses) is used once during the conversion cycle. Second, it distributes the control pulses to both the channel-data multiplexer and to the column-address inputs of the 6 x 8 RAM.

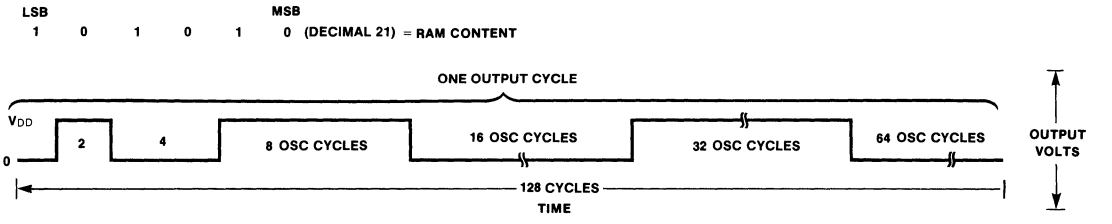


Fig. 1 Output Cycle Example

The channel-data multiplexer is enabled during the write mode so that the 6-bit control word may be written. The 6 x 8 RAM provides the storage capability required for the converter to operate independently of the microprocessor, once the control information has been transferred. Since the control information is stored in RAM, simultaneous conversions continue on all eight channels, unaided by the microprocessor unless changes are required. This is accomplished by addressing a single bit in each of the control words and reading the results out in parallel during each time interval in the conversion cycle. The total cycle time, which is the sum of the six binary-weighted time intervals plus a unit interval (64 clock periods), requires 128 oscillator periods, since the basic oscillator frequency is divided by a factor of two before driving the counter. Conversions may be completed in as little as 64 μs when operating at a 2 MHz clock rate. The control words read from the RAM are directed to the output buffers, six of which have 1 kΩ and two have 50 Ω output impedances. In general, these buffers should drive load impedances larger than the output impedance to reduce the errors caused by the finite output impedance.

Each output is capable of providing 64 discrete output levels representing 6-bit resolution. Since each output pulse stream is accurate to 12 bits, it is possible to sum two outputs and expand the resolution to 12 bits, providing 4096 discrete output levels. This may be easily accomplished by weighting one of the outputs by a factor of 1/64 before summing.

Loading data is a simple procedure that does not affect the conversion cycle. For the μA9706, the 6-bit control word (channel data) and the 3-bit channel address are serially transferred to the 9-bit shift register on the HIGH-to-LOW transitions of the data clock *(Figure 2)*. The data clock has a maximum frequency of 125 kHz with a minimum HIGH and LOW time of 4 μs. Once the nine bits of data have been transferred into the shift register, the data clock must remain static until the write operation is completed to prevent the data from being shifted out of the register. The write mode may be selected after a minimum setup time of 1 μs and is enabled by a HIGH-going W/$\overline{R}$ control pulse. This sets an internal latch that enables the channel-address decoder, which decodes the 3-bit binary channel address, therefore effecting the transfer of the 6-bit control word from the input register to RAM via the channel-data multiplexer at the beginning of the next conversion cycle. The W/$\overline{R}$ pulse has two restrictions: first, it must be equal to or greater than 4 μs in duration; second, it must be less than $128/f_{OSC}$. This latter restriction is necessary to eliminate the possibility of multiple loads occurring from a single W/$\overline{R}$ pulse that could lead to incorrect control-word transfers under certain conditions.

The μA9706A is basically the same as the μA9706 except for two differences: input structure and pin limitation. The μA9706A has three 3-bit shift registers, used for temporary storage of the 3-bit channel address and 6-bit control word. This structure is bus oriented and provides for parallel 3-bit transfers between the microprocessor and the converter *(Figure 3)*. Also, before any transfers can take place, a 3-bit ID code must be accepted. The ID code is provided in parallel over the ID clock and DB_0, DB_1 and DB_2 inputs. After the nine bits of data are transferred to the shift registers, the operation of the μA9706A is identical to the μA9706. The μA9706A provides 7-channel operation as opposed to the 8-channel operation of the μA9706.

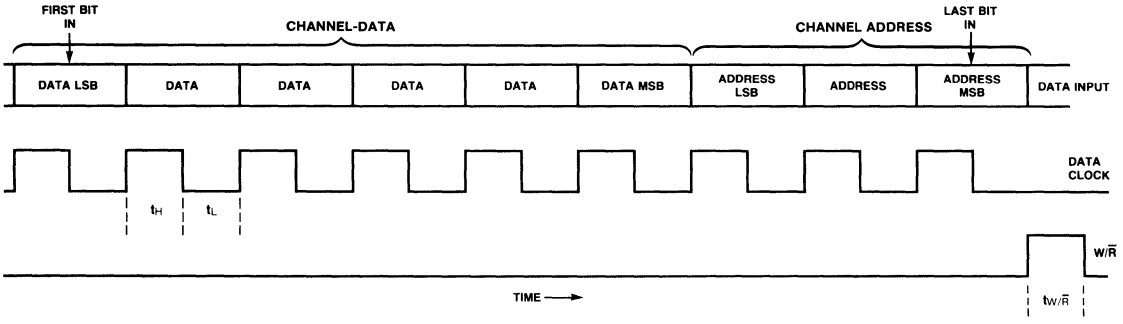


Fig. 2 μA9706 Input Timing and Format

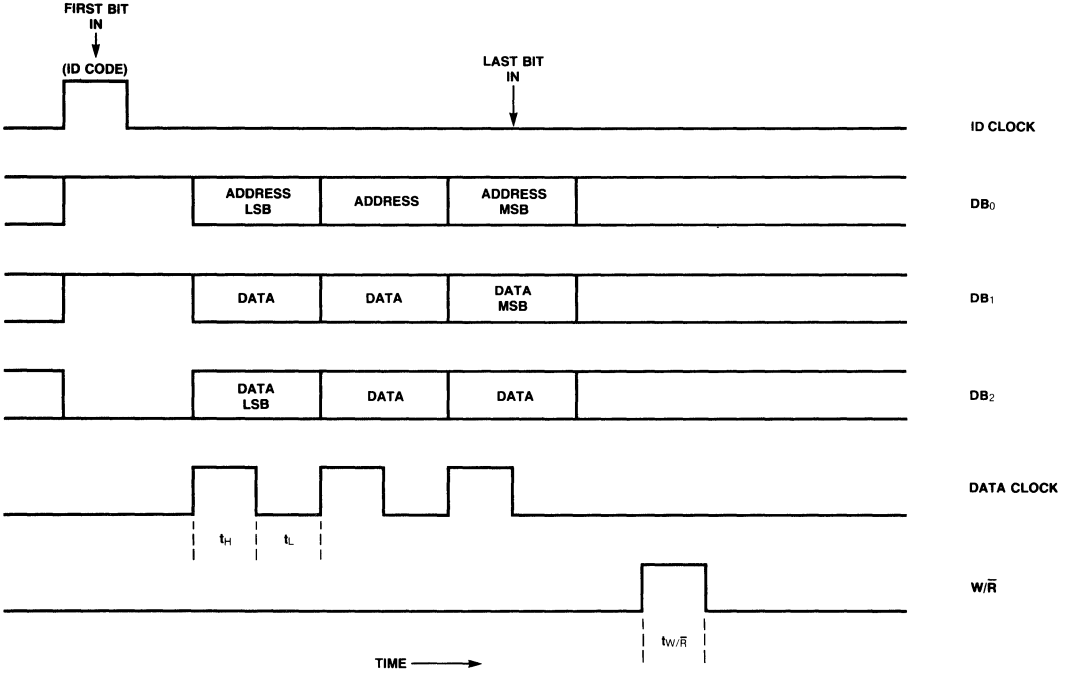
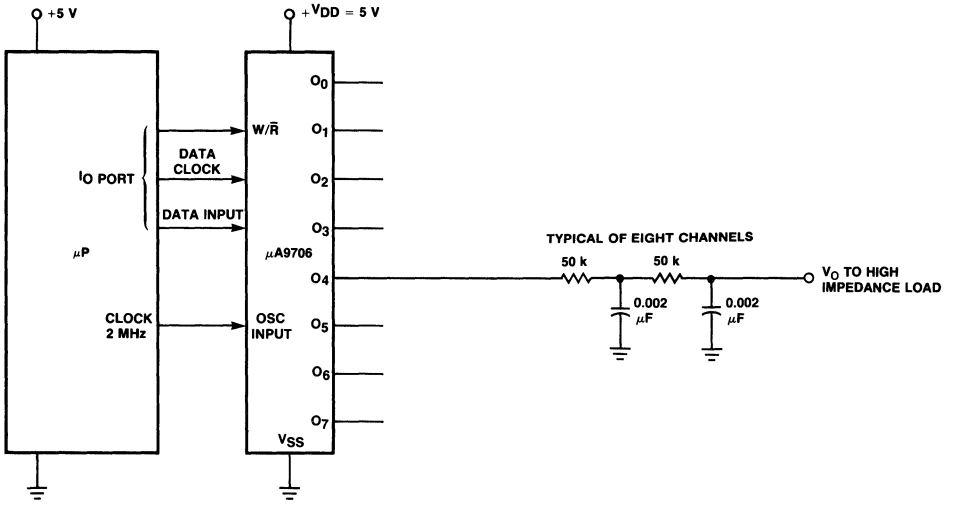


Fig. 3 μA9706A Input Timing and Format

TYPICAL μA9706 SYSTEM



μA9706 F8 OBJECT CODE SUBROUTINE

enter with R_0 = data to be output to 9706
R_1 = address to be output to 9706
entry = H'100'

F8 Object Code

```
M100-130
M0100=20    20 52 20 04 53 20 07
M0108=B0    20 0F B0 40 22 FE 18
M0110=24    0C B0 24 02 B0 40 12
M0118=50    42 12 52 94 EF 41 50
M0120=43    52 70 51 53 40 18 18
M0128=94    E3 20 0B B0 20 0F B0
M0130=1C
```

Port 0 bit 0 = Data Input
Port 0 bit 1 = Data Clock
Port 0 bit 2 = W/$\overline{R}$
Port 0 bit 3 = Scope Trigger

Exit = return, destroyed R_0, R_1, R_2, R_3, Acc

μA9706A F8 OBJECT CODE SUBROUTINE

enter with R_0 = data to be output to 9706A
R_1 = address to be output to 9706A
entry = H'100'

F8 Object Code

```
M100-16D
M0100=20    61 52 53 54 40 18 50
M0108=41    18 51 20 01 F1 13 C2
M0110=52    20 02 F1 C3 53 20 04
M0118=F1    12 C4 54 20 01 F0 13
M0120=13    13 C2 52 20 02 F0 13
M0128=13    C3 53 20 04 F0 13 C4
M0130=54    20 08 F0 12 C2 52 20
M0138=10    F0 12 12 C3 53 20 20
M0140=F0    12 12 12 C4 54 20 3F
M0148=B0    20 7F B0 20 78 B0 20
M0150=79    B0 42 B0 20 10 C2 B0
M0158=43    B0 20 10 C3 B0 44 B0
M0160=20    10 C4 B0 20 7F B0 20
M0168=5F    B0 20 7F B0 1C
```

Port 0 bit 0 = ID clock
Port 0 bit 1 = DB_0
Port 0 bit 2 = DB_1
Port 0 bit 3 = DB_2
Port 0 bit 4 = data clock
Port 0 bit 5 = W/$\overline{R}$
Port 0 bit 6 = scope trigger

Exit = return, destroyed R_0, R_1, R_2, R_3, R_4, Acc

μA9708

6-CHANNEL, 8-BIT, MICROPROCESSOR COMPATIBLE

ANALOG-TO-DIGITAL CONVERTER SUBSYSTEM*

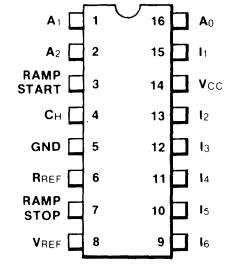
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA9708 is a single slope 8-bit, 6-channel ADC subsystem that provides all of the necessary analog functions for a microprocessor-based data control system. The device uses a microprocessor system like the F3870 or F6800 to provide the necessary addressing, timing and counting functions and includes a 1 of 8 decoder, 8-channel analog multiplexer, sample and hold, ramp integrator, precision ramp reference, and a comparator on a single monolithic chip.

- **MPU COMPATIBLE**
- **EXCELLENT LINEARITY OVER FULL TEMP RANGE - ±0.2% MAX**
- **TYPICAL 300 μs CONVERSION TIME PER CHANNEL**
- **WIDE DYNAMIC RANGE INCLUDES GROUND**
- **AUTO-ZERO AND FULL-SCALE CORRECTION CAPABILITY**
- **RATIOMETRIC CONVERSION—NO PRECISION REFERENCE REQUIRED**
- **SINGLE-SUPPLY OPERATION**
- **TTL COMPATIBLE**
- **DOES NOT REQUIRE ACCESS TO DATA BUS OR ADDRESS BUS**

CONNECTION DIAGRAM
16-PIN DUAL IN-LINE

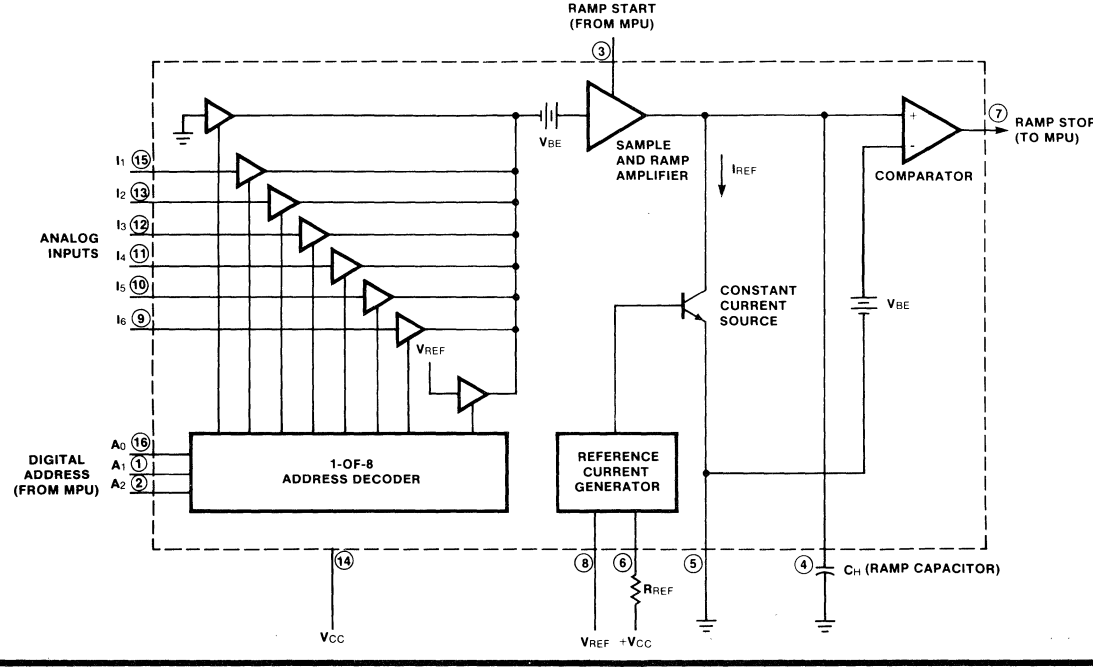
(TOP VIEW)
PACKAGE OUTLINES 7B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA9708	μA9708DM
μA9708	μA9708DC
μA9708	μA9708PC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	18 V
Comparator Output (Ramp Stop)	-0.3 V to +18 V
Analog Input Range	-0.3 V to 30 V
Digital Input Range	-0.3 V to 30 V
Output Sink Current	10 mA
Operating Temperature Range	
μA9708PC, μA9708DC	0° C to 70° C
μA9708DM	-55° C to 125° C
Storage Temperature Range	-65° C to +150° C
Continuous Total Dissipation	
Ceramic DIP Package	900 mW
Plastic DIP Package	1000 mW
Pin Temperature, Ceramic DIP (Soldering, 60 s)	300° C
Plastic DIP (Soldering, 10 s)	260° C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.0	15	V
Reference Voltage (V_{REF})*	2.8		5.25	V
Ramp Capacitor (C_H)	300			pF
Reference Current (I_R)	12		50	μA
Analog Input Range	0		V_{REF}	V
Ramp Stop Output Current			1.6	mA

*2 V ≤ V_{REF} ≤ (V_{CC} -2 V)

CHANNEL SELECTION

INPUT ADDRESS LINE			SELECTED ANALOG INPUT
A_2	A_1	A_0	
0	0	0	Ground
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	V_{REF}

ELECTRICAL CHARACTERISTICS: Over recommended operating conditions, -55°C ≤ T_A ≤ +125°C, for μA9708DM and 0°C ≤ T_A ≤ +70°C for μA9708DC or μA9708PC; unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Conversion Accuracy	E_A	Over entire temperature range (Note 1)		±0.2	±0.3	%
Linearity	E_R	Applies to any one channel (Note 2)		±0.08	±0.2	%
Multiplexer Input Offset Voltage	V_{OSM}	Channel ON		2.0	4.0	mV
Conversion Time Per Channel	t_C	Analog Input = 0v to V_{REF} C_H = 300 pF, I_{REF} = 50 μA		296	350	μs
Acquisition Time	t_A	C_H = 1000 pF		20	40	μs
Acquistion Current	I_A		150			μA
Ramp Start Delay Time	t_O			100		ns
Multiplexer Address Time	t_M			1.0		μs
Digital Input HIGH Voltage	V_{IH}	A_0, A_1, A_2, ramp start	2.0			V
Digital Input LOW Voltage	V_{IL}	A_0, A_1, A_2, ramp start			0.8	V
Analog Input Current	I_B	Channel ON or OFF	-3.0	-1.0		μA
Input LOW Current	I_{IL}	A_0, A_1, A_2, ramp start = 0.4 V	-15	-5		μA
Input HIGH Current	I_{IH}	A_0, A_1, A_2, ramp start = 5.5 V			1.0	μA
Input Offset Current	I_{OS}			1.0	3.0	μA
Comparator Logic "1" Output Leakage Current	I_{OH}	V_{OH} = 15 V			10	μA
Comparator Logic "0" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Power Supply Rejection Ratio	PSRR	(Note 3)	40			dB
Crosstalk Between Any Two Channels		(Note 4)	60			dB
Power Supply Current	I_{CC}	V_{CC} = 5 V to 15 V, I_0 = 0		7.5	15	mA
Input Capacitance	C_{IN}			3.0		pF
Comparator Output Capacitance	C_{OUT}			5.0		pF

NOTES:
1. Conversion accuracy is defined as the deviations from a straight line drawn between the points defined by channel address 000 (0 scale) and channel address 111 (full scale) for all channels.
2. Linearity is defined as the deviation from a straight line drawn between the 0 and full scale points for each channel.
3. Power supply rejection ratio is defined as the conversion error contributed by power supply voltage variations while resolving mid scale on any channel.
4. Crosstalk between channels = 20 log $\frac{\Delta V_{CH}}{\Delta V_i}$

FUNCTIONAL DESCRIPTION

This Analog to Digital Converter is a single-slope 8-bit, 6-channel A/D converter that provides all of the necessary analog functions for a microprocessor-based data/control system. The device uses the processor system to provide the necessary addressing, timing and counting functions and includes a 1 of 8 decoder, 8-channel analog multiplexer, sample and hold, precision current reference, ramp integrator and comparator on a single monolithic chip.

For applications that require auto-zero or auto-calibration, *(See Figures 2-5)* line select address 0, 0, 0 and 1, 1, 1 may be used in conjunction with the arithmetic capability of the microprocessor to provide ground and scaling factors. Address 0, 0, 0 internally connects the input of the ramp generator to ground and may be used for zero offset correction in subsequent conversions. Address 1, 1, 1 internally connects the input of the ramp generator, to the voltage reference, V_{REF}, and may be used for scale factor correction in subsequent conversions. For the following, refer to the Functional Block Diagram.

Six separate external analog voltage inputs may come into terminals I_1-I_6 and the specific analog input to be converted is selected via address terminals A_0-A_2. The analog input voltage level is transferred to the external ramp capacitor connected to pin 4 when the input to the ramp start terminal (pin 3) is at a logic 0 *(See Figure 1)*. The time to charge the capacitor is the acquisition time

which is a function of the output impedance of an amplifier internal to the A/D and the value of the capacitor. After charging the external capacitor the ramp start terminal is switched to a logic 1 which introduces a high impedance between the analog input voltage and the external capacitor.

The capacitor begins to discharge at a controlled rate. The controlled rate of discharge (ramp) is established by the external reference voltage, the external reference resistor, the value of the external capacitor and the internal leakage of the A/D. Connected to the capacitor terminal is a comparator internal to the A/D with its output going to the ramp stop terminal (pin 7). The comparator output is a logical one when the capacitor is charged and switches to a logic 0 when the capacitor is in a discharged state. The ramp time is the time from when ramp start goes high (logic "1") to when ramp stop goes low (logic "0"). The microprocessor must be programmed to determine this conversion time. The ideal (no undesirable internal source impedances, leakage paths, errors on levels where comparator switches or delay time) conversion time is calculated as follows.

$$\text{Ramp Time} = V_1 \left| \frac{C_H}{I_R} \right.$$

Where V_1 = Analog Input Voltage being measured

C_H = External Ramp Capacitor

$$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$$

Where V_{CC} = Power Supply Voltage

V_{REF} = Reference Voltage

R_{REF} = Reference Resistor

In actual use the errors due to a nonideal A/D can be minimized by using a microprocessor to make the calculations. *(See Figures 2 through 5)*

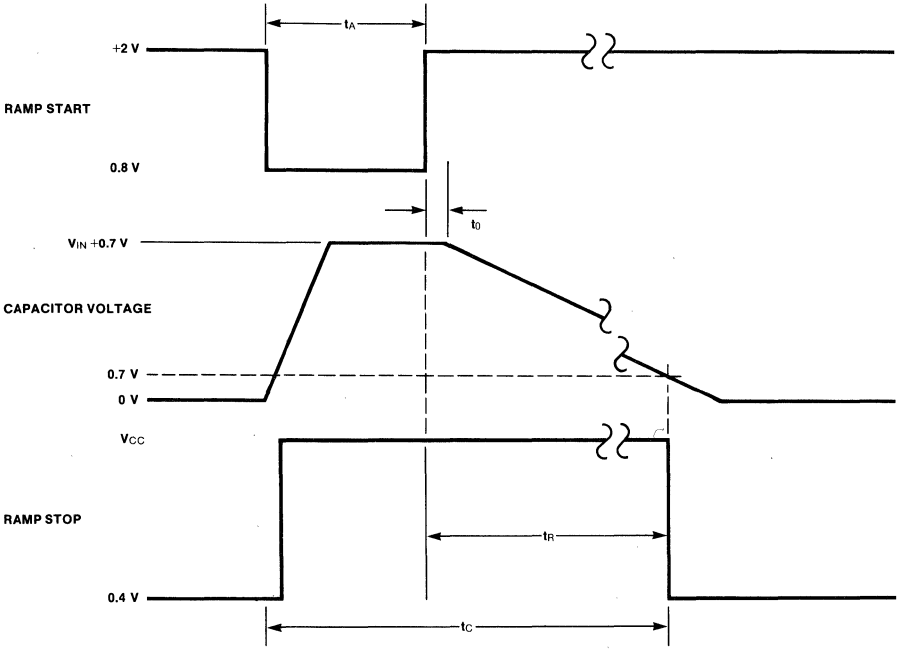


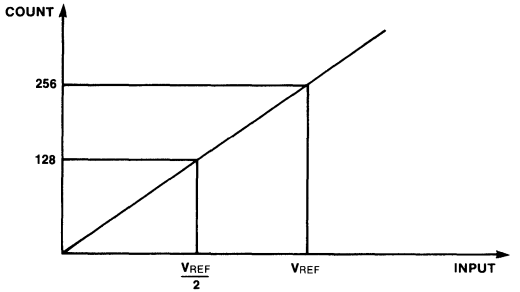
Fig. 1 Equivalent Timing Waveform for Test Circuits and Applications

APPLICATION HINTS AND FORMULAS

1. The capacitor node impedance is approximately 30 μΩ and should have no parallel resistance for proper operation.
2. t_R when $V_{IN} = 0$ V will be finite (i.e., the comparator will always toggle for $V_{IN} \geq 0$ V.)
3. The ramp stop output is open collector, and an external pull up resistor is required.
4. All digital inputs and outputs are TTL compatible.
5. For proper operation timing commences on the 0 to 1 transition of ramp start and terminates on the 1 to 0 transition of ramp stop.
6. $t_A \geq \frac{C_H}{150\ \mu A - I_R} \times V_{REF}$
7. t_R (ramp time) $= \frac{C_H}{I_R} \times V_{IN}$, $t_R\big|_{max} = \frac{C_H}{I_R} \times V_{REF}$
8. $I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$
9. $2\ V \leq V_{REF} \leq (V_{CC} - 2\ V)$
10. Address lines A_0, A_1, A_2 must be stable throughout the sampling interval, t_A.
11. Pin 6 (R_{REF}) should be bypassed to ground via a 0.02 μF capacitor.

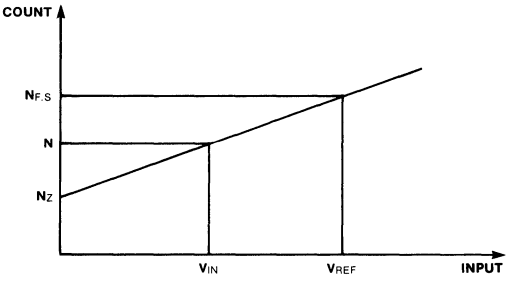
5

AUTO-ZERO AND FULL-SCALE FEATURES



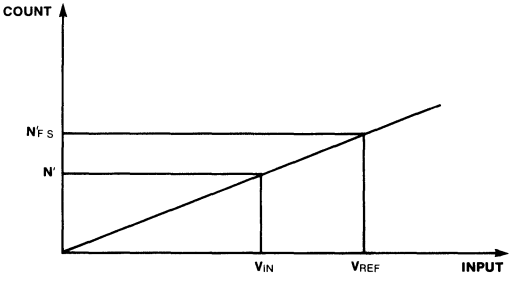
- NO ZERO OFFSET
- NO FULL-SCALE ERROR
- COUNT (N) = $\frac{V_{IN}}{V_{REF}} = 256$

Fig. 2 Ideal Transfer Function



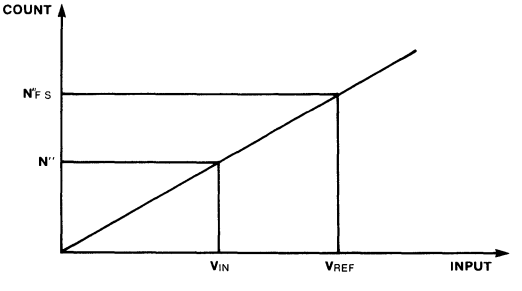
- $N_{F.S.} \neq 256$
- $N_Z \neq 0$
- (N) HAS BOTH FULL-SCALE AND ZERO ERRORS

Fig. 3 Transfer Function with Zero and Full-Scale Error



- $N' = N - N_Z$
- N' HAS FULL-SCALE ERROR

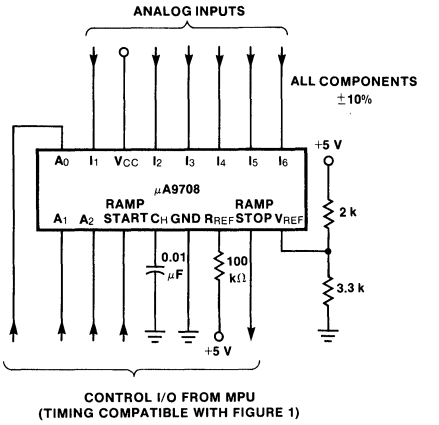
Fig. 4 Zero-Correction Added



- $N'' = (N - N_Z) \times \frac{256}{(N_{F.S.} - N_Z)}$

Fig. 5 Both Zero and Full-Scale Correction Added

TEST CIRCUITS



INPUT TIMING:

$t_A > 400\ \mu s$

$$V_{REF} = \left(\frac{3.3\ k\Omega}{2\ k\Omega + 3.3\ k\Omega}\right) 5\ V = 3.1\ V$$

$$I_R = \frac{5\text{-}3.1}{100\ k\Omega} = 19\ \mu A$$

$$t_R\Big|_{max} = \text{full scale ramp time} = \frac{0.01 \times 10^{-6}}{19 \times 10^{-6}} \times 3.1 = 1.6\ ms$$

NOTE:
For evaluation purposes, the ramp start timing generation can be implemented with a μA555 timer (astable operation) or MPU evaluation kit, and a time internal meter for ramp time measurement. The TIM meter will measure the time between the 0 to 1 transition of the ramp start and the 1 to 0 transition of the ramp stop. The ramp stop is open collector, and must have an external pull up resistor to V_{CC}.

Fig. 6 Slow Speed Evaluation Circuit for Ratiometric Operation

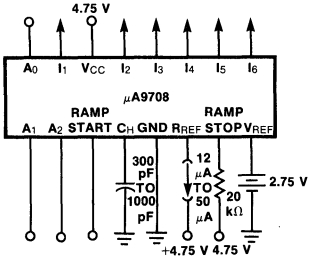


Fig. 7 Linearity/Acquisition Time/Conversion Time Test Circuit

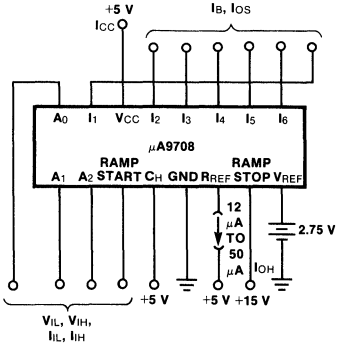
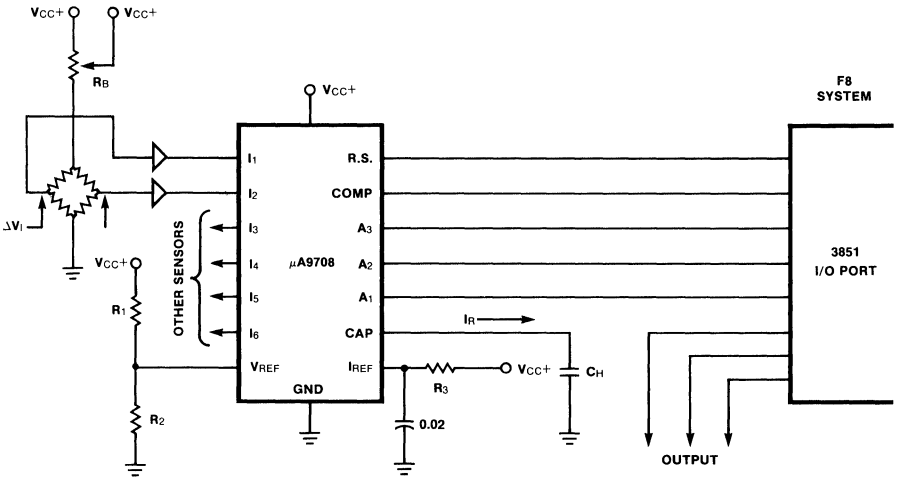


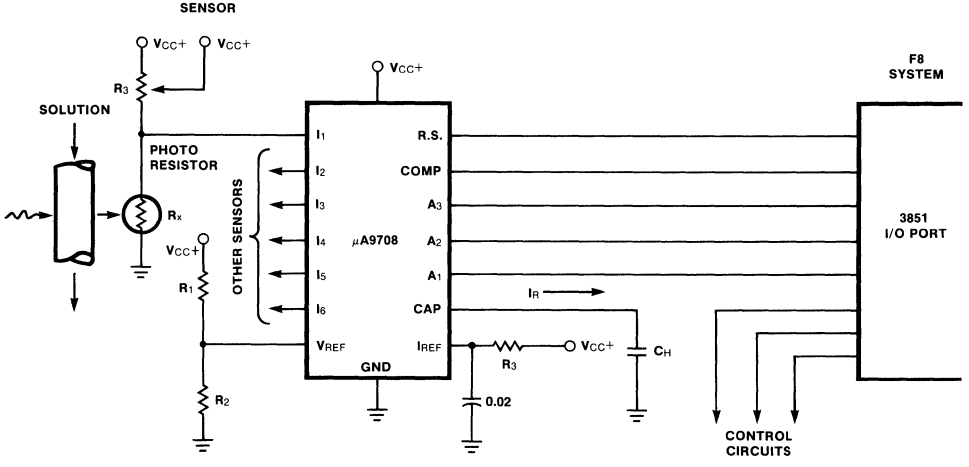
Fig. 8 Static Measurements

TYPICAL APPLICATIONS



ΔV_I = (Applied Force) and can be Linearized (if necessary) in F8 Software.

Ratiometric Strain Gage Sensor/Controller



APPLICATIONS:

- **BEVERAGE BREWERS/DISPENSERS**
- **CHEMICAL SOLUTION CONTROL**
- **AUTOMATIC LIQUID MIXING CONTROL**

$$\text{RAMP CURRENT} = I_R = V_{CC}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{1}{R_3}\right)$$

$$V_I = \left(\frac{R_X}{R_X + R_B}\right) V_{CC+}$$

$$\text{RAMP TIME} = V_I \frac{C_H}{I_R} = \left(\frac{R_X}{R_X + R_B}\right)\left(1 + \frac{R_2}{R_1}\right)\left(C_H R_3\right)$$

Opaque Solution Controller

SYSTEM HINTS:

Several alternatives exist from a hardware/software standpoint in microprocessor based systems using the μA9708.

1. The ramp time measurement may be implemented in software using a register increment, followed by a branch back depending on the status of the ramp stop.

2. Alternately, the ramp stop may be tied into the interrupt structure in systems containing a programmable binary timer. This scheme has the following advantages:

   A. The CPU is not committed during the ramp time interval.
   B. It requires only 4 bits of an I/O port for control signals.

3. The auto-zero/auto-full-scale (see *Figures 2-5*) should use double precision, rounded (as opposed to truncated) arithmatics. Several points are worth noting:

   A. The subtractions are single op code instructions.
   B. The full scale correction uses a multiply by 256 and can be accomplished by a shift left 8 bits (usually one instruction) or placing (N-Nz) in the MSB register and setting the LSB register to zero, for the double precision divide.
   C. The divisor ($N_{F.S.}$ - Nz) MSB's register will always be zero.

These schemes have the following advantages:

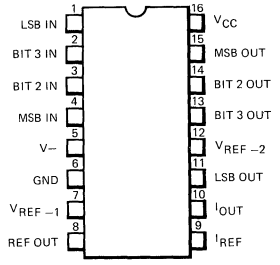
A. No access to the data buss or address buss is required, by the A/D system.
B. 4 I/O bits completely support the A/D system.
C. Since auto full scale/auto zero are implemented in software and long term drift (aging) effects are eliminated.
D. Software overhead is minimal (typically 30 bytes).
E. Where ratiometric operation is permissible, the 4 external components may be ±5% tolerance, including the power supply.

9650
4-BIT CURRENT SOURCE
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 9650 is a high speed, 4-Bit Precision Current Source, intended for use in D/A and A/D converters with up to 12-bit accuracy. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process and consists of a reference transistor and four logic operated precision current sources connected to a single output summing line. Logic inputs are fully TTL compatible under all temperature and supply conditions. A clamp circuit is provided to prevent turn on latchup on the reference input.

- **200 ns SETTLING TIME (12 ± 1/2 LSB)**
- **STANDARD SUPPLY LEVELS**
- **VARIABLE BIT CURRENTS**
- **REFERENCE COMPENSATION**
- **TTL COMPATIBLE**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6B
PACAKGE CODE D



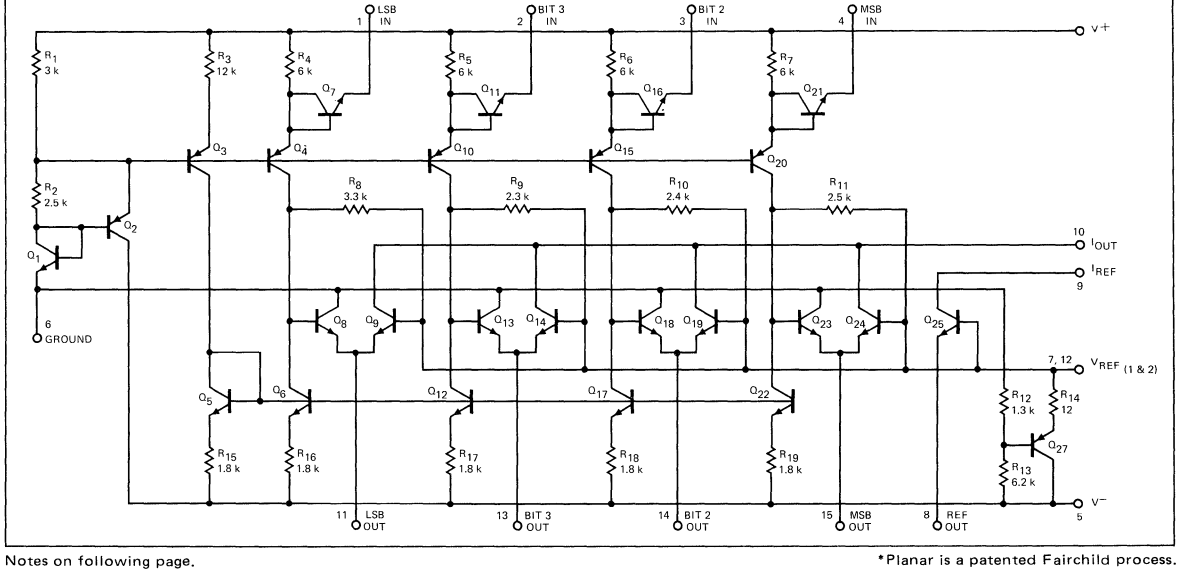
ABSOLUTE MAXIMUM RATINGS

V_{CC}^+	+7 V
V_{CC}^-	–18 V
MSB Current	2.0 mA
Logic Input Voltage	+5.5 V
Power Dissipation (Note 1)	730 mW
Storage Temperature	–65°C to +150°C
Operating Temperature	0°C to 70°C
Pin Temperature (Soldering, 60 s)	+300°C
V_{REF} Inputs	+7 V to V^-
Output (V_{ref} voltage ≥ –7.0 V)	+18 V to V_{REF}

ORDER INFORMATION

TYPE	PART NO.
9650-1C	**9650-1DC**
9650-2C	**9650-2DC**
9650-3C	**9650-3DC**

EQUIVALENT CIRCUIT



Notes on following page.

*Planar is a patented Fairchild process.

9650-1C • 9650-2C • 9650-3C

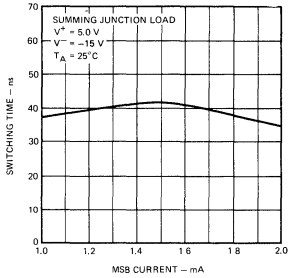
ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, Power Supply Range, 4.5V, –14 V to 5.5 V, –16 V, unless otherwise specified

CHARACTERISTICS (see definitions)	CONDITIONS (TYPE)	MIN.	TYP.	MAX.	UNITS
Linearity	(9650-1C)			±0.01	% of FSI
	(9650-2C)			±0.05	% of FSI
	(9650-3C)			±0.2	% of FSI
Full Scale Output Current Error	(9650-1C)			±0.1	%
	(9650-2C)			±0.2	%
	(9650-3C)			±0.4	%
Power Supply Coefficient of Full Scale Output Current	(9650-1C)			±0.003	%/V
	(9650-2C, 9650-3C)			±0.012	%/V
V_{BE} Range		550		650	mV
h_{FE} of Reference Transistor		300	1000		
Output Impedance	All Bits On		5.0		MΩ
The following specifications apply for $0°C \leq T_A \leq 70°C$					
Accuracy	(9650-1C)			±0.025	% of FSI
	(9650-2C)			±0.1	% of FSI
	(9650-3C)			±0.3	% of FSI
Full Scale Output Current Error	(9650-1C)			0.2	%
	(9650-2C)			0.3	%
	(9650-3C)			0.6	%
Power Supply Coefficient of Full Scale Output Current	(9650-1C)			±0.006	%/V
	(9650-2C, 9650-3C)			±0.024	%/V
Input LOW Voltage	Each Bit On			0.8	V
Input HIGH Voltage	Each Bit Off	2.0			V
Input LOW Current	$V_{IL} = 0.4$ V			–1.6	mA
Input HIGH Current	$V_{IH} = 2.4$ V			40	μA
Output Current	Bit 1 (MSB)		1.0	2.0	mA
	Bit 2		0.5	1.0	mA
	Bit 3		0.25	0.5	mA
	Bit 4 (LSB)		0.125	0.25	mA
Output Current	All Bits Off				
	(9650-1C)		5.0	250	nA
	(9650-2C, 9650-3C)		5.0	500	nA
Output Voltage	Feeding Op Amp Summing Junction		0		V
	Resistive Load	–4.0		V^+	V
Reference Current	Using Compensation Transistor		1.0		mA
V_{REF} Current			±1.0	±2.2	mA
Reference Limit Current	$V_{REF} = 0$ V	20		75	mA
Positive Supply Current	(9650-1C, 9650-2C)			8.0	mA
	(9650-3C)			10	mA
Negative Supply Current	(9650-1C, 9650-2C)			–11	mA
	(9650-3C)			–15	mA

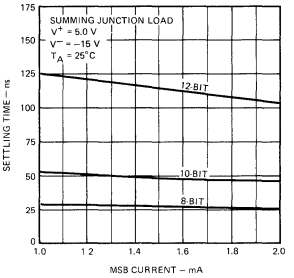
NOTES:
1. Rating applies for ambient temperature to 70°C. Derate linearly at 9.1 mW/°C for ambient temperatures above 70°C.
2. V_{REF} Voltage ≥ -7.0 V.

TYPICAL PERFORMANCE CURVES

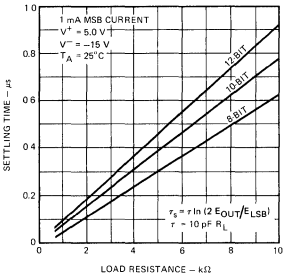
SWITCHING TIME AS A FUNCTION OF MSB CURRENT (50% IN TO 10% OUT)



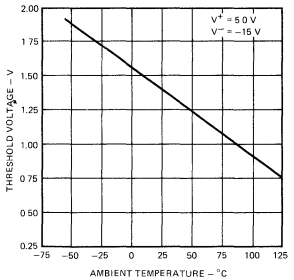
OUTPUT CURRENT SETTLING TIME AS A FUNCTION OF MSB CURRENT (0 TO FSI OUTPUT ± 1/2 LSB)



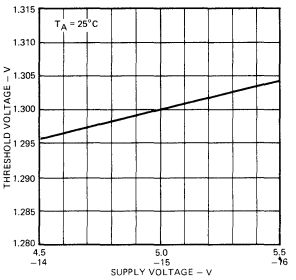
SETTLING TIME AS A FUNCTION OF LOAD RESISTANCE (0 TO FSI OUTPUT ± 1/2 LSB)



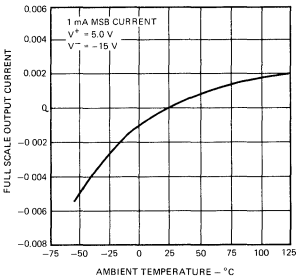
INPUT LOGIC THRESHOLD VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT LOGIC THRESHOLD VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



FULL SCALE OUTPUT CURRENT DRIFT AS A FUNCTION OF AMBIENT TEMPERATURE



5

TRUTH TABLE

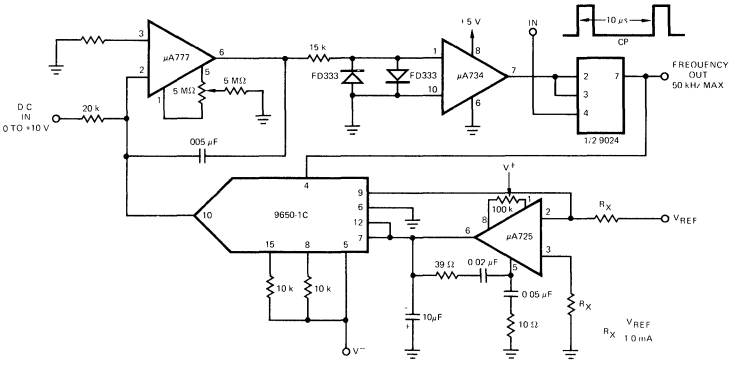
LOGIC INPUT	NOMINAL OUTPUT CURRENT (mA)	LOGIC INPUT	NOMINAL OUTPUT CURRENT (mA)
0000	1.875	1000	0.875
0001	1.750	1001	0.750
0010	1.625	1010	0.625
0011	1.500	1011	0.500
0100	1.375	1100	0.375
0101	1.250	1101	0.250
0110	1.125	1110	0.125
0111	1.000	1111	0.000

9650 KITS REQUIRED TO BUILD D/A – A/D CONVERTERS

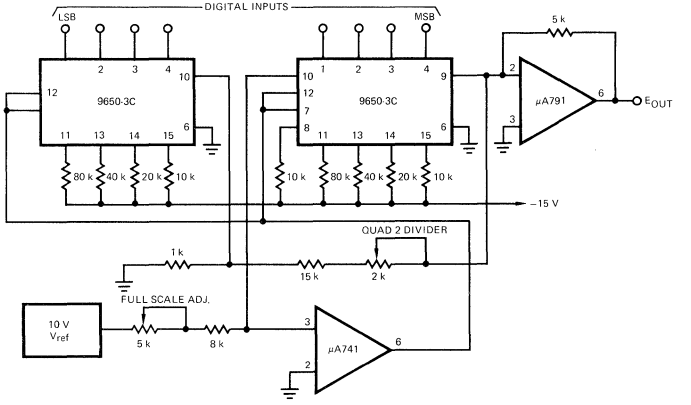
TEMPERATURE RANGE	TYPE		
0°C to +70°C	9650-1C	9650-2C	9650-3C
	NO. OF UNITS		
Accuracy to:			
8 Bits	0	0	2
10 Bits	0	1	2
12 Bits	1	1	1

TYPICAL APPLICATIONS

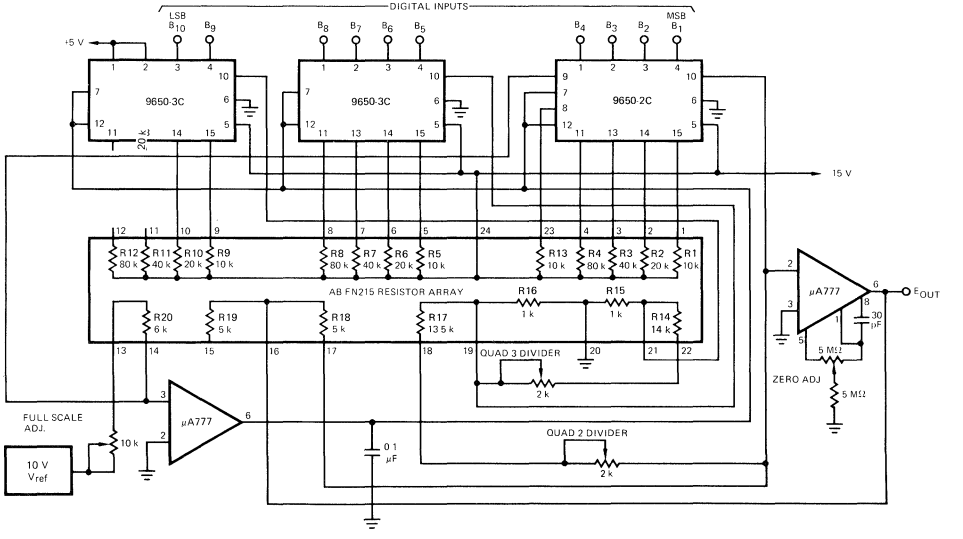
VOLTAGE TO FREQUENCY CONVERTER



8-BIT D/A CONVERTER

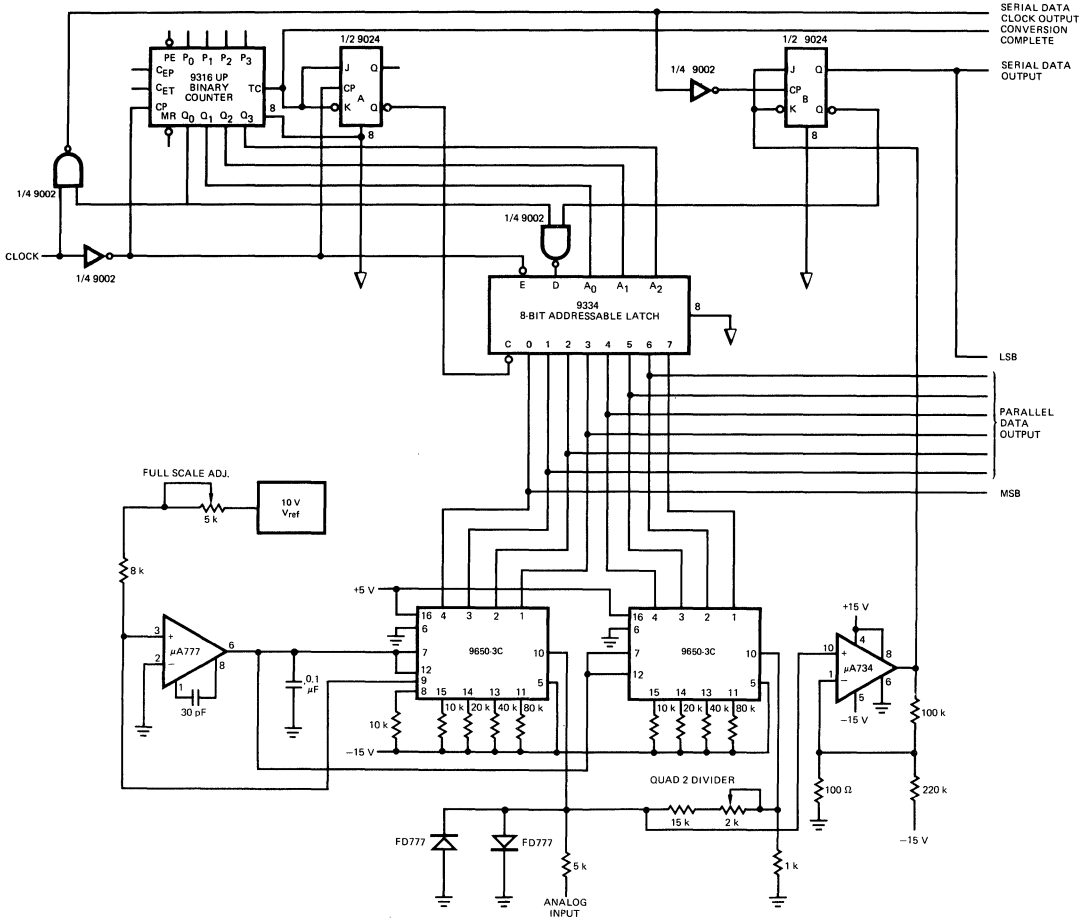


10-BIT D/A CONVERTER



TYPICAL APPLICATIONS (Cont'd)

8-BIT A/D CONVERTER

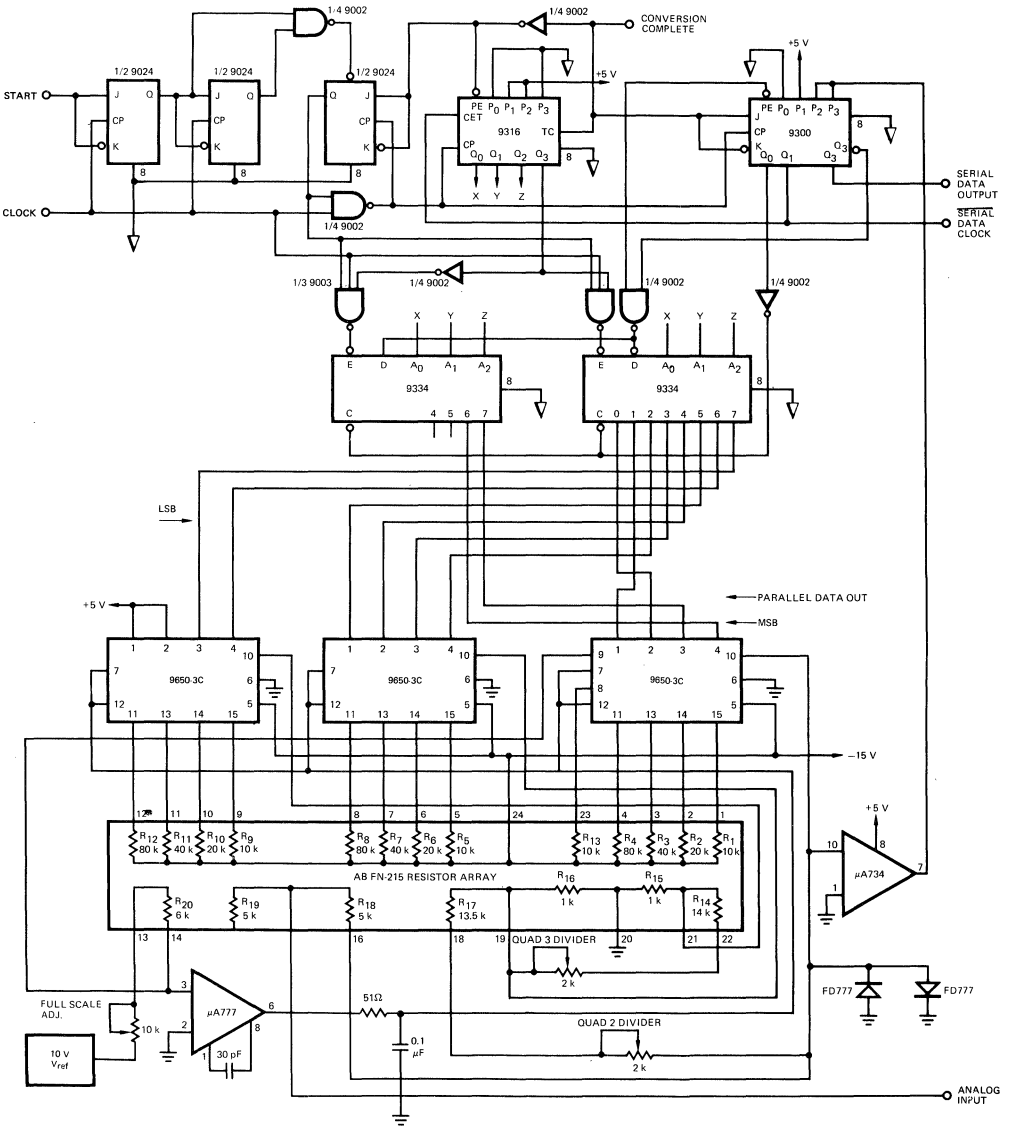


NOTE: Digital gnd. indicated by ⏚

Analog gnd. indicated by ⏚

TYPICAL APPLICATIONS (Cont'd)

10-BIT A/D CONVERTER

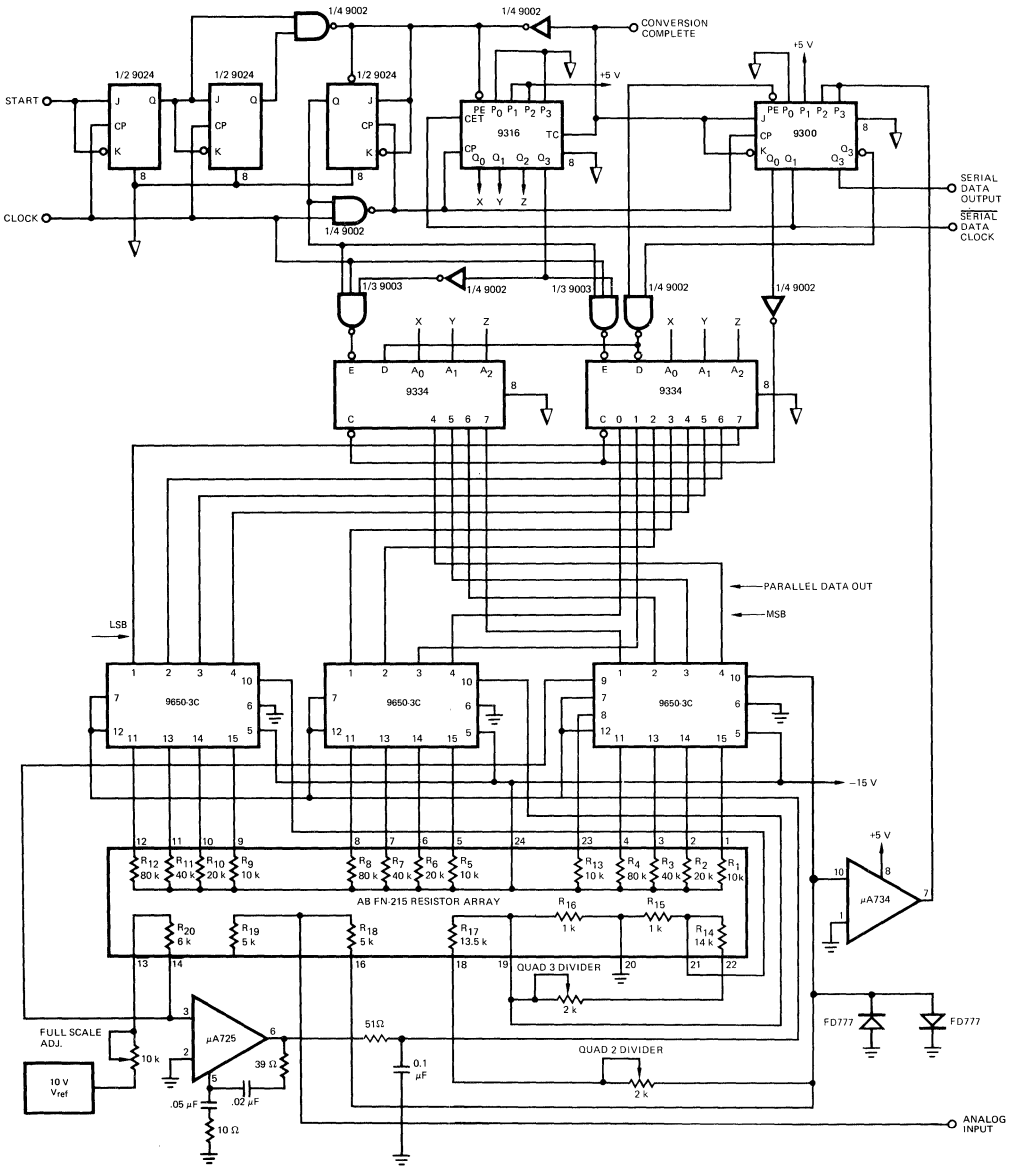


NOTE: Digital gnd. indicated by ⏚

Analog gnd. indicated by ⏚

TYPICAL APPLICATIONS (Cont'd)

12-BIT A/D CONVERTER

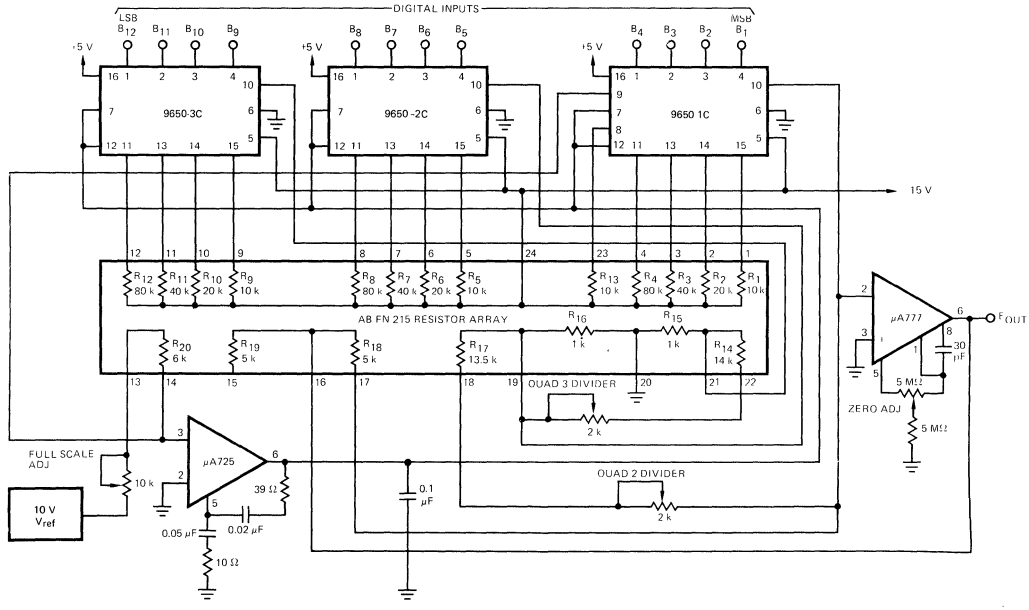


NOTE: Digital gnd. indicated by ⏚

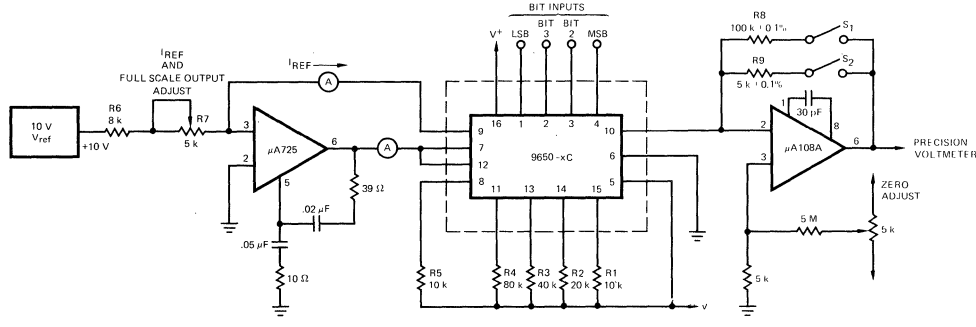
Analog gnd. indicated by ⏚

TYPICAL APPLICATIONS (Cont'd)

12-BIT D/A CONVERTER

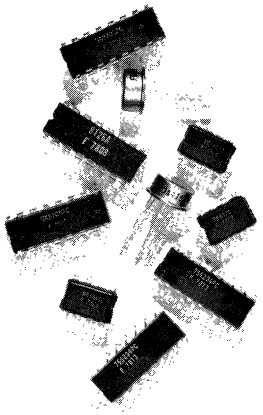


TYPICAL DC TEST CIRCUIT



NOTES:

1. Required resistor ratio tolerances of $R_1 - R_5$ to test the various grades are as follows:
   9650-1C, R_5 to R_2 to R_1 – ±0.005%, R_3 to R_1 – ±0.01%, R_4 to R_1 – ±0.02%.
   9650-2C, R_5 to R_2 to R_1 – ±0.025%, R_3 to R_1 – ±0.05%, R_4 to R_1 – ±0.1%.
   9650-3C, R_5 to R_2 to R_1 – ±0.1%, R_3 to R_1 – ±0.2%, R_4 to R_1 – ±0.4%.
2. S_1 closed and S_2 open for output current (all Bits off) tests only.



LINE CIRCUITS

μA1488

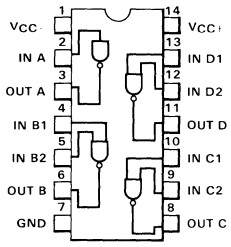
QUAD LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA1488 is an EIA RS-232C specified Quad Line Driver. This device is used to interface data terminals with data communications equipment. The μA1488 is a pin-for-pin replacement of the MC1488.

- **CURRENT LIMITED OUTPUT – ± 10 mA TYP**
- **POWER-OFF SOURCE IMPEDANCE – 300 Ω MIN**
- **SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR**
- **FLEXIBLE OPERATING SUPPLY RANGE**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

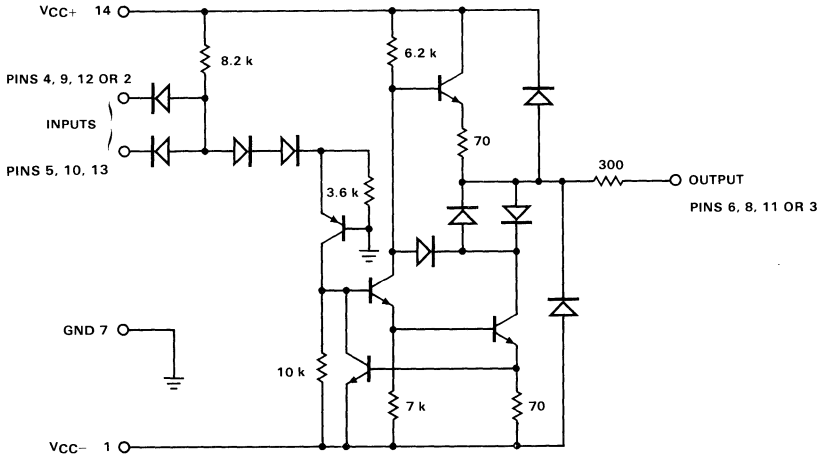
TYPE	PART NO.
μA1488	μA1488DC
μA1488	μA1488PC

ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

Power Supply Voltages	
$V_{CC}+$	+15 V
$V_{CC}-$	−15 V
Input Voltage Range (V_{IR})	−15 V DC to +7.0 V DC
Output Signal Voltage	±15 V DC
Continuous Total Power Dissipation (Note 1)	800 mW
Operating Temperature Range	0°C to 70°C
Pin Temperature	−65°C to +150°C
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Note 1: Above 60°C ambient temperatures, derate linearly at 8.3 mW/°C.

CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



ELECTRICAL CHARACTERISTICS: V_{CC+} = +9.0 V ± 1%, V_{CC-} = −9.0 V ± 1%, T_A = 0 to +70°C, unless otherwise noted.

SYMBOL	CHARACTERISTICS	CONDITIONS	FIG.	MIN	TYP	MAX	UNITS
I_{IL}	Input LOW Current	V_{IL} = 0	1		1.0	1.6	mA
I_{IH}	Input HIGH Current	V_{IH} = 5.0 V	1			10	μA
V_{OH}	Output HIGH Voltage	V_{IL} = 0.8 V, R_L = 3.0 kΩ V_{CC+} = +9.0 V, V_{CC-} = −9.0 V	2	+6.0	+7.0		V
		V_{IL} = 0.8 V, R_L = 3.0 kΩ V_{CC+} = +13.2 V, V_{CC-} = −13.2 V	2	+9.0	+10.5		
V_{OL}	Output LOW Voltage	V_{IH} = 1.9 V, R_L = 3.0 kΩ V_{CC+} = +9.0 V, V_{CC-} = −9.0 V	2	−6.0	−7.0		V
		V_{IH} = 1.9 V, R_L = 3.0 kΩ V_{CC+} = +13.2 V, V_{CC-} = −13.2 V	2	−9.0	−10.5		
I_{OS+}	Positive Output Short-Circuit Current	V_{IL} = 0.8 V (Note 1)	3	+6.0	+10	+12	mA
I_{OS-}	Negative Output Short-Circuit Current	V_{IH} = 1.9 V (Note 1)	3	−6.0	−10	−12	mA
R_{OUT}	Output Resistance	V_{CC+} = V_{CC-} = 0 V, V_O = ±2.0 V	4	300			Ω
I_{CC+}	Positive Supply Current	R_L = ∞ V_{IH} = 1.9 V, V_{CC+} = +9.0 V V_{IL} = 0.8 V, V_{CC-} = +9.0 V V_{IH} = 1.9 V, V_{CC+} = +12 V V_{IL} = 0.8 V, V_{CC+} = +12 V V_{IH} = 1.9 V, V_{CC+} = +15 V V_{IL} = 0.8 V, V_{CC+} = +15 V	5		+15 +4.5 +19 +5.5	+20 +6.0 +25 +7.0 +34 +12	mA
I_{CC-}	Negative Supply Current	R_L = ∞ V_{IH} = 1.9 V, V_{CC-} = −9.0 V V_{IL} = 0.8 V, V_{CC-} = −9.0 V V_{IH} = 1.9 V, V_{CC-} = −12 V V_{IL} = 0.8 V, V_{CC-} = −12 V V_{IH} = 1.9 V, V_{CC-} = −15 V V_{IL} = 0.8 V, V_{CC-} = −15 V	5		−13 −18	−17 −15 −23 −15 −34 −2.5	mA μA mA μA mA mA
P_C	Power Consumption	V_{CC+} = 9.0 V, V_{CC-} = −9.0 V V_{CC+} = 12 V, V_{CC-} = −12 V				333 576	mW

AC CHARACTERISTICS: V_{CC+} = +9.0 V ± 1%, V_{CC-} = −9.0 V ± 1%, T_A = 25°C

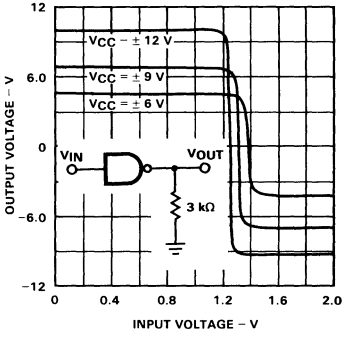
SYMBOL	CHARACTERISTICS	CONDITION	FIG.	MIN	TYP	MAX	UNITS
t_{PLH} t_{PHL}	Propagation Delay Time	R_L = 3.0 kΩ, C_L = 15 pF	6		220 70	350 175	ns
t_f t_r	Fall Time Rise Time	R_L = 3.0 kΩ, C_L = 15 pF	6		70 55	75 100	ns

NOTE 1: Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

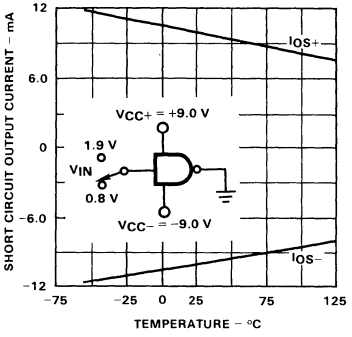
TYPICAL CHARACTERISTICS

T_A = +25°C unless otherwise noted

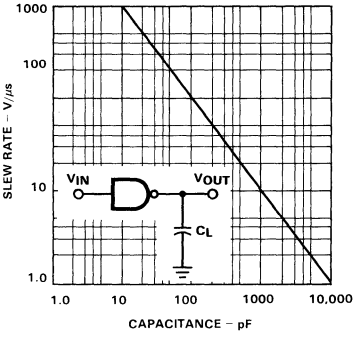
TRANSFER CHARACTERISTICS AS A FUNCTION OF POWER SUPPLY VOLTAGE



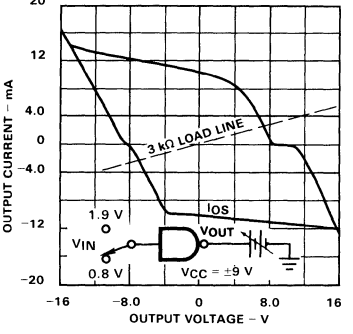
SHORT CIRCUIT OUTPUT CURRENT AS A FUNCTION OF TEMPERATURE



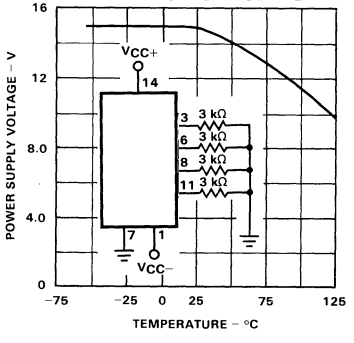
OUTPUT SLEW RATE AS A FUNCTION OF LOAD CAPACITANCE



OUTPUT VOLTAGE AND CURRENT LIMITING CHARACTERISTICS



MAXIMUM OPERATING TEMPERATURE AS A FUNCTION OF POWER SUPPLY VOLTAGE



DC TEST CIRCUITS

Fig. 1. Input Current

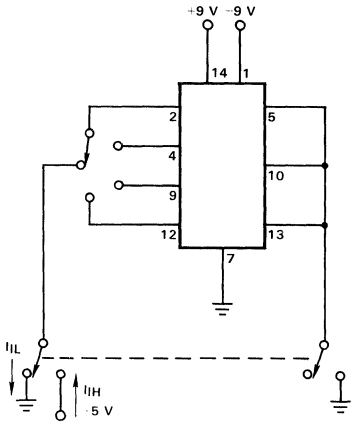


Fig. 2. Output Voltage

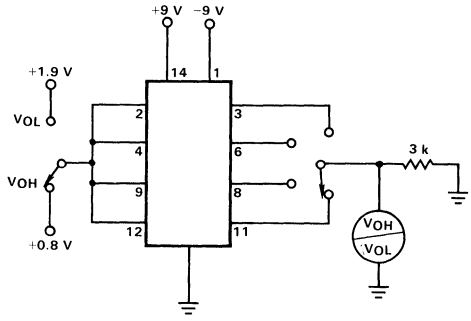


Fig. 3. Output Short-Circuit Current

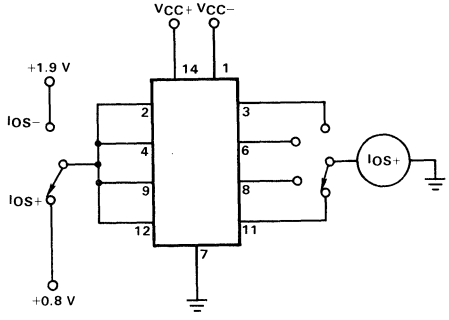


Fig. 4. Output Resistance (Power-off)

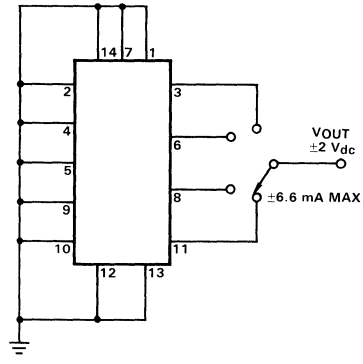


Fig. 5. Power-Supply Currents

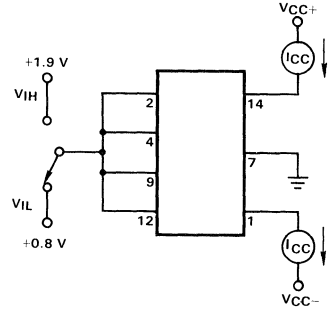
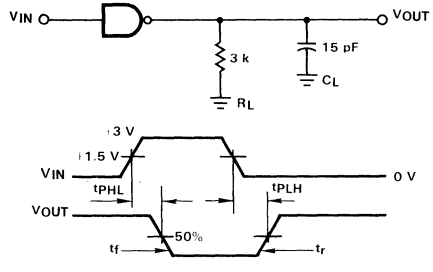


Fig. 6. AC Test Circuit and Voltage Waveform



t_r and t_f are measured 10% to 90%

μA8T13 • 55121 • 75121

DUAL SINGLE-ENDED LINE DRIVERS

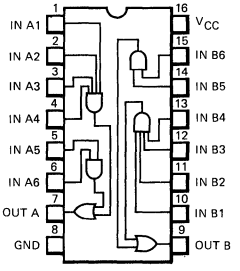
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA8T13/55121/75121 Dual Line Drivers are designed for driving 50 Ω to 500 Ω coaxial cable, strip line, or twisted pair transmission lines. All inputs are TTL or DTL compatible and the emitter-follower outputs enable two or more drivers to operate on the same line in parity line applications.

For a dual line driver to meet the IBM System/360 I/O Interface Specification, see 75123 or 8T23 data sheets.

- **HIGH OUTPUT DRIVE CAPABILITY**
- **HIGH SPEED**
- **INPUT CLAMP DIODES**
- **SINGLE 5 V SUPPLY OPERATION**
- **SHORT CIRCUIT PROTECTED**

CONNECTION DIAGRAM
16-PIN
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ABSOLUTE MAXIMUM RATINGS

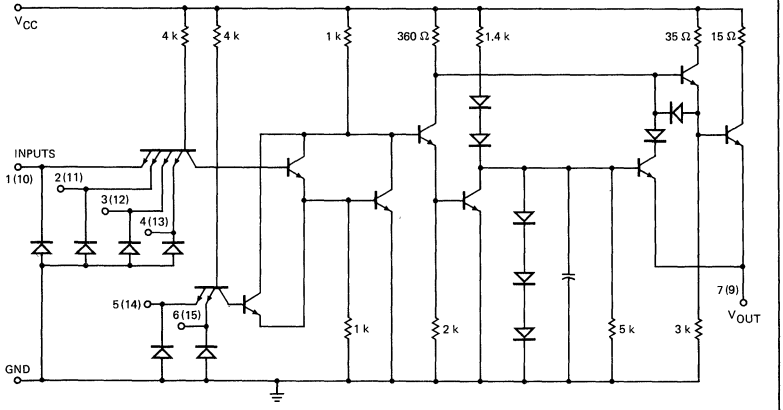
Input Voltage (Note 1)	+6.0 V
Output Voltage (Note 1)	+6.0 V
Supply Voltage (Note 1)	+6.0 V
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	
Military (55121, μA8T13DM)	−55°C to +125°C
Commercial (75121)	0°C to +70°C
Pin Temperatures	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 2)	800 mW

NOTES:
1. Voltages are with respect to the ground pin (pin 8)
2. For Hermetic DIP and Molded DIP rating applies to ambient temperatures up to 60°C, above 60°C derate linearly at 8.3 mW/°C.

ORDER INFORMATION

TYPE	PART NO.
μA8T13 or 55121	μA8T13/55121DM
μA8T13 or 75121	μA8T13/75121DC
μA8T13 or 75121	μA8T13/75121PC

EQUIVALENT CIRCUIT (For Each Driver)



55/75121 FUNCTION TABLE

INPUTS						OUTPUT
1	2	3	4	5	6	
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Inputs Combinations						L

55121, 75121 RECOMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}		4.75	5	5.25	V
Output HIGH Current, I_{OH}				−75	mA
Operating Ambient Temperature, T_A	55121/μA8T13	−55		125	°C
	75121/μA8T13	0		70	°C

ELECTRICAL CHARACTERISTICS: V_{CC+} = 4.75 V to 5.25 V, Ratings apply over recommended temperature range unless noted.

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_{IN}	Input Clamp Voltage	V_{CC} = 5.0 V, I_{IN} = −12 mA			−1.5	V
$V_{(BR)I}$	Input Breakdown Voltage	V_{CC} = 5.0 V, I_{IN} = 10 mA	5.5			V
V_{OH}	Output HIGH Voltage	V_{IH} = 2.0 V, I_{OH} = −75 mA (Note 3)	2.4			V
I_{OH}	Output HIGH Current	V_{CC} = 5.0 V, V_{IH} = 4.5 V V_{OH} = 2.0 V, T_A = 25°C (Note 3)	−100		−250	mA
I_{OL}	Output LOW Current	V_{IL} = 0.8 V, V_{OL} = 0.4 V (Note 3)			−800	μA
$I_{OUT(off)}$	Off-State Output Current	V_{CC} = 0, V_{OUT} = 3.0 V			500	μA
I_{IH}	Input HIGH Current	V_{IN} = 4.5 V			40	μA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V	−0.1		−1.6	mA
I_{OS}	Short-Circuit Output Current	V_{CC} = 5.0 V, T_A = 25°C			−30	mA
I_{CCH}	Supply Current, Outputs HIGH	V_{CC} = 5.25 V, All inputs at 2.0 V Outputs open			28	mA
I_{CCL}	Supply Current, Outputs LOW	V_{CC} = 5.25 V, All inputs at 0.8 V Outputs open			60	mA

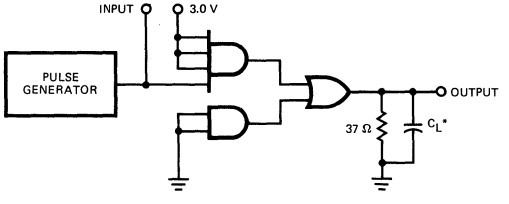
AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C.

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	R_L = 37 Ω, C_L = 15 pF See Test Circuit		11	20	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output			8.0	20	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	R_L = 37 Ω, C_L = 1000 pF See Test Circuit		22	50	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output			20	50	

NOTE:
4. The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.

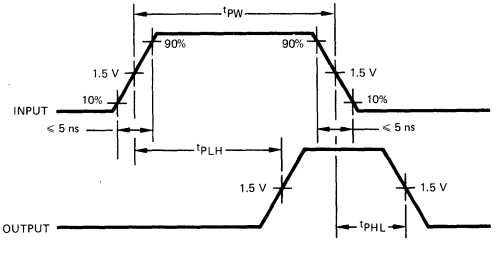
AC CHARACTERISTICS

TEST CIRCUIT



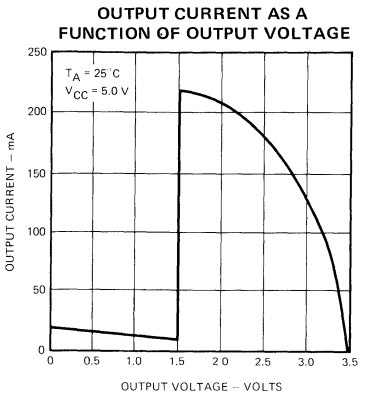
INPUT PULSE:
Amplitude = 2.6 V
t_{PW} = 40 ns (50% Duty Cycle)

VOLTAGE WAVEFORMS



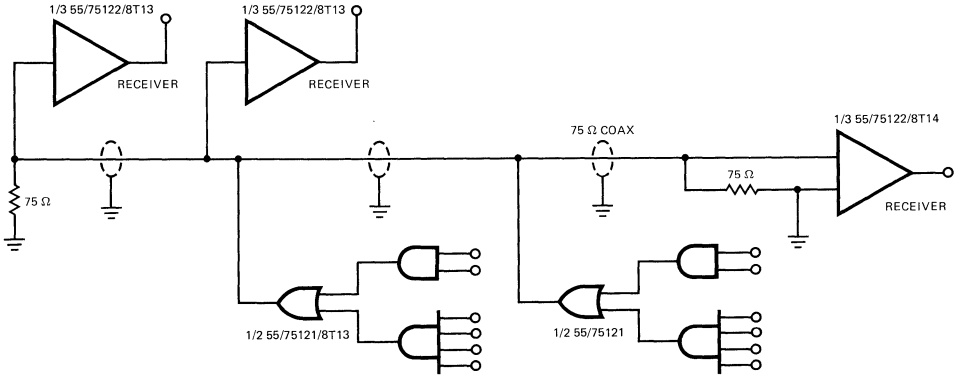
*Includes probe and jig capacitance.

TYPICAL PERFORMANCE CURVE FOR 55121/75121/μA8T13



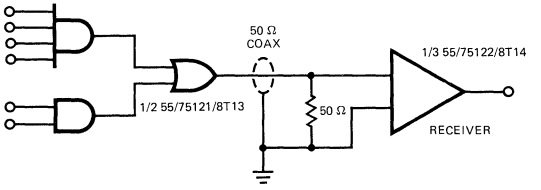
TYPICAL APPLICATIONS

75 Ω PARTY LINE (2 DRIVERS, 3 RECEIVERS)



NOTE: For party line operation, termination of each physical end of the line is recommended.

SIMPLEX OPERATION (1 DRIVER)



NOTE: For simplex operation, the line should be terminated only at the distant receiver site.

μA8T23 • 75123

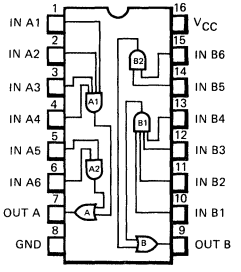
DUAL SINGLE-ENDED LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA8T23/75123 Dual Line Driver meets the requirements of the IBM System/360 I/O Interface Specification for interface drivers. Inputs are TTL/DTL compatible. Logic has been incorporated to ensure that no spurious noise is generated on the transmission line during the power-up and power-down sequence. The outputs are protected from short circuits and have uncommitteed emitter outputs which allows DOT-OR logic to be performed in party line data bus applications.

- **I_{OUT} = 59.3 mA AT 3.11 V**
- **UNCOMMITTED EMITTER OUTPUTS FOR PARTY LINE/WIRED-OR APPLICATIONS**
- **SHORT CIRCUIT PROTECTION**
- **SINGLE 5.0 V SUPPLY OPERATION**
- **AND-OR LOGIC CONFIGURATION**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	+5.5 V
Output Voltage (Note 1)	+7.0 V
Supply Voltage (Note 1)	+7.0 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to 70°C
Pin Temperatures s	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 2)	800 mW

FUNCTION TABLE

INPUTS						OUTPUT
1	2	3	4	5	6	
H	H	H	H	X	X	H
X	X	X	X	H	H	H
ALL OTHER INPUT COMBINATIONS						L

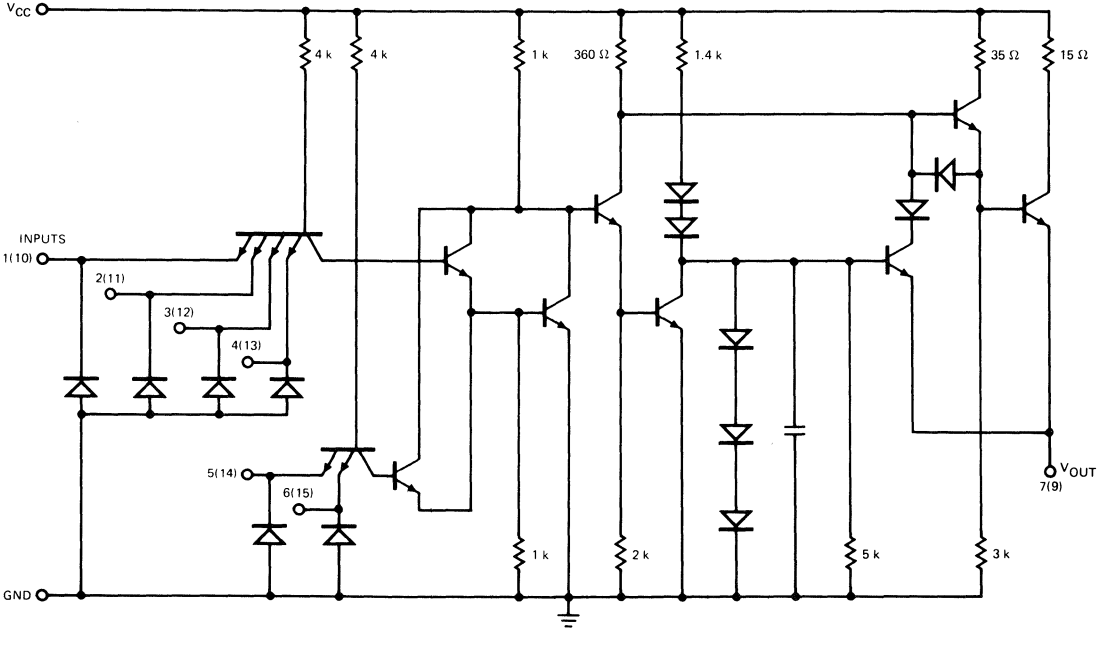
H = HIGH
L = LOW
X = Don't Care

ORDER INFORMATION

TYPE	PART NO.
μA8T23 or 75123	μA8T23/75123DC
μA8T23 or 75123	μA8T23/75123PC

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 60°C. Above 60°C derate linearly at 8.3 mW/°C.

EQUIVALENT CIRCUIT (FOR EACH DRIVER)



RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
Output HIGH Current, I_{OH}			−75	mA
Operating Ambient Temperature, T_A	0		70	°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0 V, I_{IN} = −12 mA				−1.5	V
$V_{(BR)I}$	Input Breakdown Voltage	V_{CC} = 5.0 V, I_{IN} = 10 mA		5.5			V
V_{OH}	Output HIGH Voltage	V_{CC} = 5.0 V, V_{IH} = 2.0 V,	T_A = 25°C	3.11			V
		I_{OH} = −59.3 mA, See Note 3	T_A = 0°C to 70°C	2.9			
I_{OH}	Output HIGH Current	V_{CC} = 5.0 V, V_{IH} = 4.5 V, V_{OH} = 2.0 V, T_A = 25°C, See Note 3		−100		−250	mA
V_{OL}	Output LOW Voltage	V_{IL} = 0.8 V, I_{OL} = −240 μA, See Note 3				0.15	V
$I_{OUT(off)}$	Off-State Output Current	V_{CC} = 0, V_{OUT} = 3.0 V				40	μA
I_{IH}	Input HIGH Current	V_{IN} = 4.5 V				40	μA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V		−0.1		−1.6	mA
I_{OS}	Short-Circuit Output Current	V_{CC} = 5.0 V, T_A = 25°C				−30	mA
I_{CCH}	Supply Current, Outputs HIGH	V_{CC} = 5.25 V, All Inputs at 2.0 V, Outputs Open				28	mA
I_{CCL}	Supply Current, Outputs LOW	V_{CC} = 5.25 V, All Inputs at 0.8 V, Outputs Open				60	mA

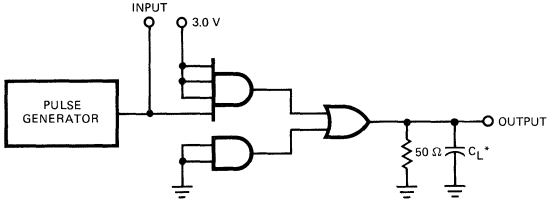
AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	R_L = 50 Ω, C_L = 15 pF		12	20	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW	See Test Circuit		12	20	
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	R_L = 50 Ω, C_L = 100 pF		20	35	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW	See Test Circuit		15	25	

3. The output voltage and current limits are guaranteed for any appropriate combination of HIGH and LOW inputs specified by the function table for the desired output.

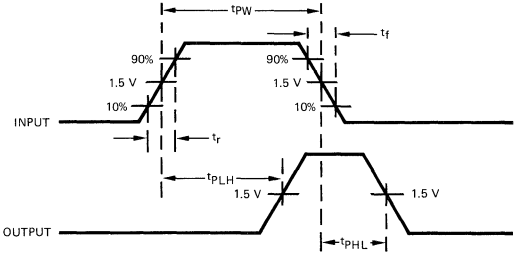
AC CHARACTERISTICS

TEST CIRCUIT



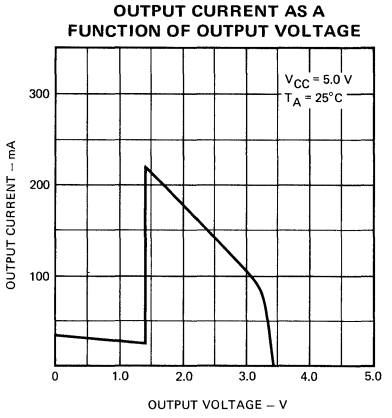
INPUT PULSE:
Amplitude = 2.6 V
t_{PW} = 50 ns (50% Duty Cycle)
$t_r = t_f \leqslant 5$ ns (10% and 90% measurement points)

WAVEFORMS

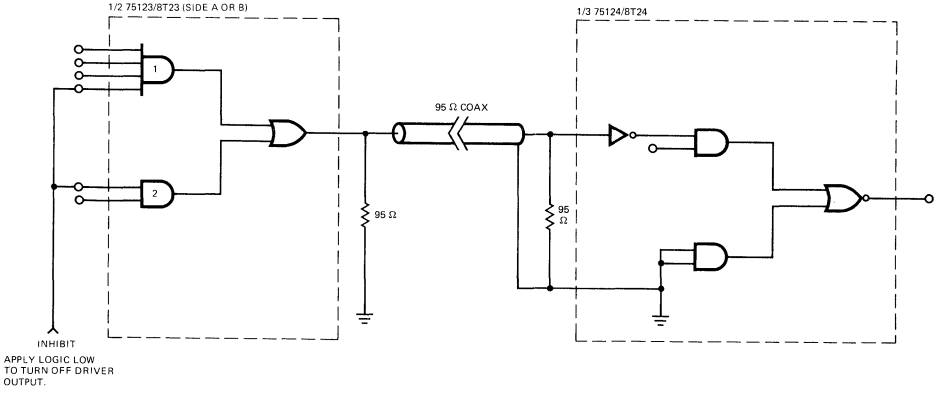


*Includes probe and jig capacitance

TYPICAL PERFORMANCE CURVE FOR 75123/μA8T23



TYPICAL APPLICATION



NOTE: To insure proper logic operation, unused inputs should not be left floating. Tie the unused inputs to V_{CC} through a current limit resistor (2.2kΩ).
To inhibit the driver, apply a logic LOW voltage to one input from gate 1 and 2 as shown above.

55110A • 75110A • 75112

DUAL LINE DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55110A, 75110A and 75112 have improved output current regulation with supply voltage and temperature variations. In addition, the higher current of the 75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the 55107A, 75107A and 75108A line receivers.

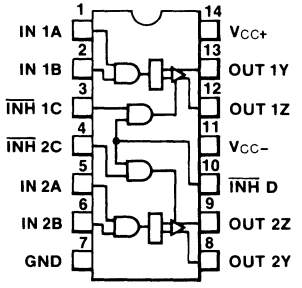
These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the inhibit inputs. The output current is nominally 12 mA for the '110A and 27 mA for the 75112.

The inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high-the output impedance of output transistor is biased to cutoff.

- **GLITCHLESS OUTPUTS - NO OUTPUT TRANSIENTS ON POWER UP OR DOWN**
- **IMPROVED STABILITY OVER SUPPLY VOLTAGE AND TEMPERATURE RANGES**
- **CONSTANT-CURRENT, HIGH-IMPEDANCE OUTPUTS**
- **HIGH SPEED-15 ns**
- **STANDARD SUPPLY VOLTAGES**
- **INHIBITOR AVAILABLE FOR DRIVER SELECTION**
- **HIGH COMMON-MODE OUTPUT VOLTAGE RANGE (-3 V TO 10 V)**
- **TTL INPUT COMPATIBILITY**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
55110A	75110ADM
75110A	75110APC
75110A	75110ADC
75112	75112 PC
75112	75112 DC

ABSOLUTE MAXIMUM RATINGS OVER AMBIENT TEMPERATURE RANGE (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	7 V
Supply voltage, V_{CC-}	-7 V
Input voltage (any input)	5.5 V
Output voltage (any output)	-5 V to 12 V
Continuous total dissipation at (or below) 25°C ambient temperature (see Note 2)	
Ceramic DIP package	900 mW
Plastic DIP package	1700 mW
Operating ambient temperature, 55110A	-55°C to 125°C
75110A, 75112	0°C to 70°C
Storage temperature range	-65°C to 150°C
Pin temperature, Hermetic DIP (soldering 60 s)	300°C
Plastic DIP (soldering 10 s)	260°C

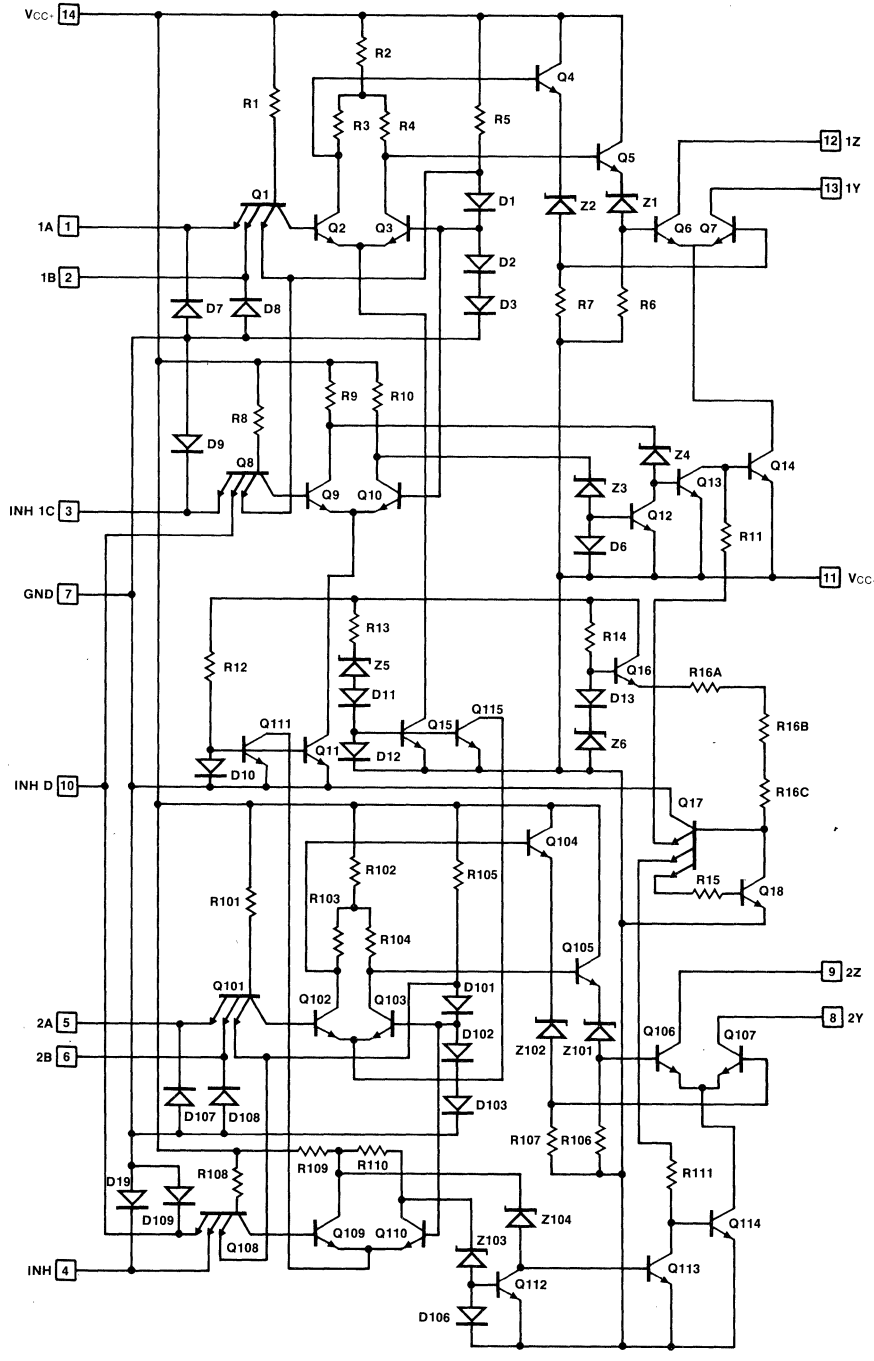
NOTES:
1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C ambient temperature, derate hermetic DIP at 8 mW/°C and plastic DIP at 14 mW/°C.

FUNCTION TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = HIGH level, L = LOW level, X = irrelevant

CIRCUIT SCHEMATIC



RECOMMENDED OPERATING CONDITIONS (SEE NOTE 3)

	55110A			75110A/75112			UNITS
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply Voltage V_{CC-}	-4.5	-5	-5.5	-4.75	-5	-5.25	V
Positive Common Mode Output Voltage	0		10	0		10	V
Negative Common Mode Output Voltage	0		-3	0		-3	V
Operating Free-Air Temperature Range	-55		125	0		70	°C

NOTE 3: When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

ELECTRICAL CHARACTERISTICS: OVER RECOMMENDED OPERATING AMBIENT TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	CHARACTERISTICS		TEST CONDITIONS†	55110A 75110A			75112			UNITS
				MIN	TYP††	MAX	MIN	TYP††	MAX	
V_{IH}	Input HIGH voltage			2			2			V
V_{IL}	Input LOW voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		$V_{CC\pm}$ = MIN, I_{IN} = -12 mA		-0.9	-1.5		-0.9	-1.5	V
$I_{O(on)}$	On-state output current		$V_{CC\pm}$ = MAX, V_{OUT} = 10 V $V_{CC\pm}$ = MIN, V_{OUT} = -3 V	6.5	12 12	15	18	27 27	36	mA
$I_{O(off)}$	Off-state output current		$V_{CC\pm}$ = MIN, V_{OUT} = 10 V			100			100	μA
I_I	Input current at maximum input voltage	A,B or C Inputs	$V_{CC\pm}$ = MAX, V_{IN} = 5.5 V			1			1	mA
		D Input				2			2	
I_{IH}	Input HIGH Current	A,B or C Inputs	$V_{CC\pm}$ = MAX, V_{IN} = 2.4 V			40			40	μA
		D Input				80			80	
I_{IL}	Input LOW Current	A,B or C Inputs	$V_{CC\pm}$ = MAX, V_{IN} = 0.4 V			-3			-3	mA
		D Input				-6			-6	
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled		$V_{CC\pm}$ = MAX, A & B inputs at 0.4 V, C & D inputs at 2 V		23	35		25	40	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled				-34	-50		-65	-100	
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited		$V_{CC\pm}$ = MAX, A,B,C and D inputs at 0.4 V		21			30		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited				-17			-32		

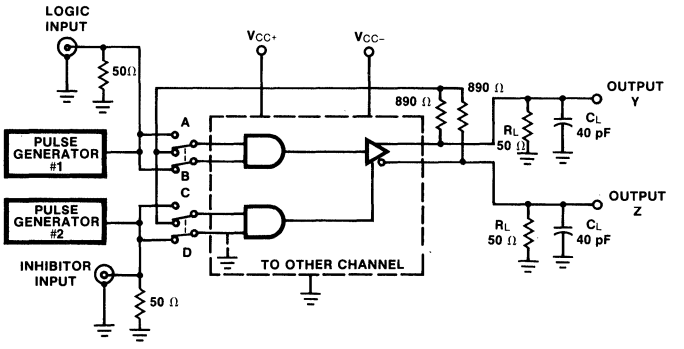
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

††All typical values are V_{CC+} = 5 V, V_{CC-} = -5 V, T_A = 25°C

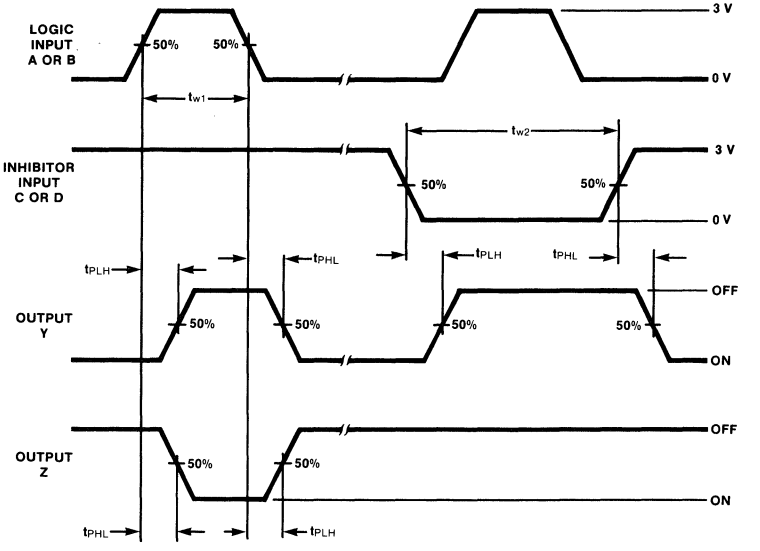
AC CHARACTERISTICS: V_{CC+} = 5 V, V_{CC-} = -5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, LOW to HIGH	A or B	Y or Z	C_L = 40 pF, R_L = 50 Ω, See Figure 1		9	15	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					9	15	ns
t_{PLH}	Propagation Delay Time, LOW to HIGH	C or D	Y or Z			16	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					13	25	ns

CHARACTERISTICS MEASUREMENT INFORMATION



AC TEST CIRCUIT

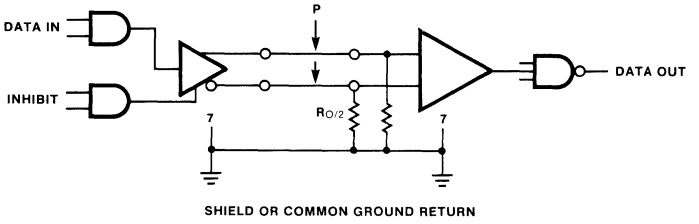


VOLTAGE WAVEFORMS

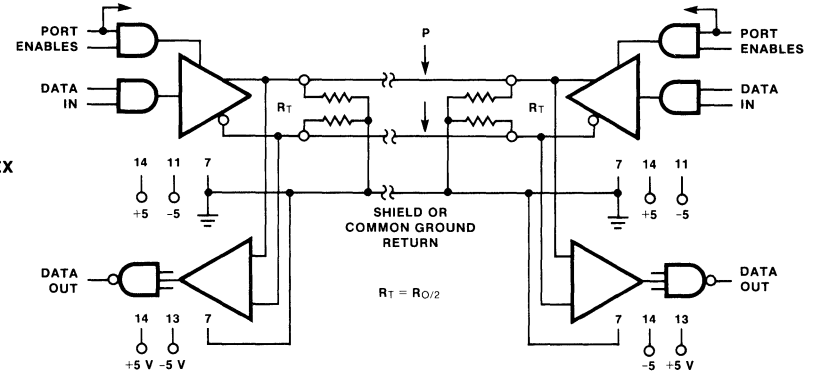
NOTES:
1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{w1} = 500 ns, PRR = 1 MHz, t_{w2} = 1 ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

APPLICATIONS

A. SIMPLEX



B. HALF-DUPLEX



All drivers are 75110A or 75112. Receivers are 75107 or 75108. Twisted pair or coaxial transmission line should be used for minimum noise and cross talk.

When only one driver in a package is being used, the outputs of the other driver should either be grounded or inhibited to reduce power dissipation.

75150

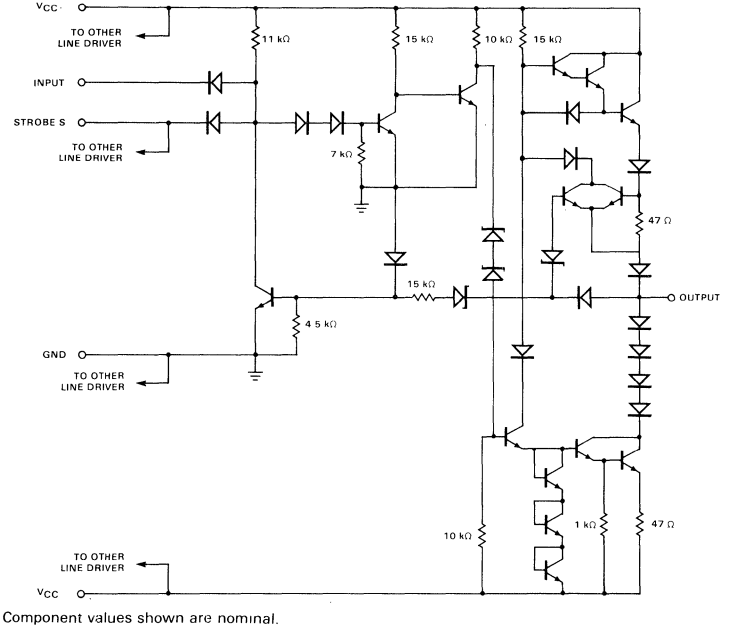
DUAL LINE DRIVER

FAIRCHILD INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12 V and −12 V power supplies.

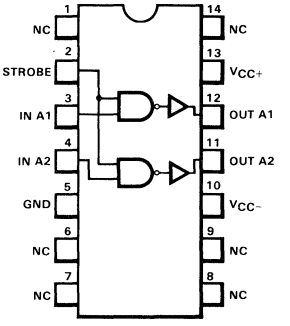
- **WITHSTANDS SUSTAINED OUTPUT SHORT-CIRCUIT TO ANY LOW-IMPEDANCE VOLTAGE BETWEEN −25V AND 25 V**
- **2.0 μs MAX TRANSITION TIME THROUGH THE +3.0 V TO −3.0 V TRANSITION REGION UNDER FULL 2500 pF LOAD**
- **INPUTS COMPATIBLE WITH MOST TTL AND DTL FAMILIES**
- **COMMON STROBE INPUT**
- **INVERTING OUTPUT**
- **SLEW RATE CAN BE CONTROLLED WITH AN EXTERNAL CAPACITOR AT THE OUTPUT**
- **STANDARD SUPPLY VOLTAGES ±12 V**

SCHEMATIC (each line driver)



Component values shown are nominal.

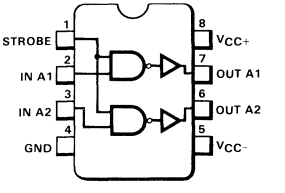
CONNECTION DIAGRAMS
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A, 9A



ORDER INFORMATION

TYPE	PART NO.
75150	75150DC
75150	75150PC

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T, 6T



ORDER INFORMATION

TYPE	PART NO.
75150	75150RC
75150	75150TC

ABSOLUTE MAXIMUM RATINGS (over operating free-air temperature range, unless otherwise noted).

Supply Voltage V_{CC+} (See Note 1)	15 V
Supply Voltage V_{CC-} (See Note 1)	−15 V
Input Voltage (See Note 1)	15 V
Applied Output Voltage (See Note 1)	±25 V
Operating Ampient Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Note 1: Voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNITS
Supply Voltage V_{CC+}	10.8	12	13.2	V
Supply Voltage V_{CC-}	−10.8	−12	−13.2	V
Input Voltage, V_I	0		5.5	V
Applied Output Voltage, V_O			±15	V
Operating Ambient Temperature, T_A	0		70	°C

6

ELECTRICAL CHARACTERISTICS: Over Recommended Operating Free-Air Temperature Range (unless otherwise noted).

SYMBOL	CHARACTERISTICS	TEST FIGURE	TEST CONDITIONS		MIN (See Note 2)	TYP*	MAX	UNITS
V_{IH}	Input HIGH Voltage	1			2.0			V
V_{IL}	Input LOW Voltage	2					0.8	V
V_{OH}	Output HIGH Voltage	2	V_{CC+} = 10.8 V, V_{IL} = 0.8 V,	V_{CC-} = −13.2 V, R_L = 3 kΩ to 7 kΩ	5.0	8.0		V
V_{OL}	Output LOW Voltage	1	V_{CC+} = 10.8 V, V_{IH} = 2 V,	V_{CC-} = −10.8 V, R_L = 3 kΩ to 7 kΩ		−8.0	−5.0	V
I_{IH}	Input HIGH Current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 2.4 V	Data Input		1.0	10	μA
				Strobe Input		2.0	20	
I_{IL}	Input LOW Current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0.4 V	Data Input		−1.0	−1.6	mA
				Strobe Input		−2.0	−3.2	
I_{OS}	Short-Circuit Output Current	4	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	V_O = 25 V		2.0		mA
				V_O = −25 V		−3.0		
				V_O = 0 V, V_I = 3 V		15		
				V_O = 0 V, V_I = 0 V		−15		
I_{CCH+}	Supply Current from V_{CC+}, Output HIGH	5	V_{CC+} = 13.2 V, V_I = 3 V, T_A = 25°C	V_{CC-} = −13.2 V, R_L = 3 kΩ,		10	22	mA
I_{CCH-}	Supply Current from V_{CC-}, Output HIGH					−1.0	−10	mA
I_{CCL+}	Supply Current from V_{CC+}, Output LOW	5	V_{CC+} = 13.2 V, V_I = 3 V, T_A = 25°C	V_{CC-} = −13.2 V, R_L = 3 kΩ,		8.0	17	mA
I_{CCL-}	Supply Current from V_{CC-}, Output LOW					−9.0	−20	mA

NOTE 2: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more negative voltage.

*All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

AC CHARACTERISTICS: $V_{CC+} = 12$ V, $V_{CC-} = -12$ V, $T_A = 25°C$.

SYMBOL	CHARACTERISTICS	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{TLH}	Transition Time, Output LOW to HIGH	6	$C_L = 2500$ pF,	0.2	1.4	2.0	μs
t_{THL}	Transition Time, Output HIGH to LOW		$R_L = 3$ kΩ to 7 kΩ	0.2	1.5	2.0	μs
t_{THL}	Transition Time, Output LOW to HIGH	6	$C_L = 15$ pF,		40		ns
t_{THL}	Transition Time, Output HIGH to LOW		$R_L = 7$ kΩ		20		ns
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	6	$C_L = 15$ pF,		60		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW		$R_L = 7$ kΩ		45		ns

CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUITS*

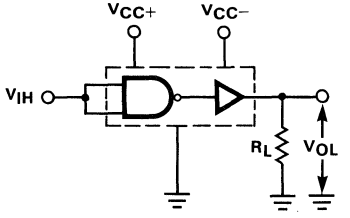


Fig. 1. V_{IH}, V_{OL}

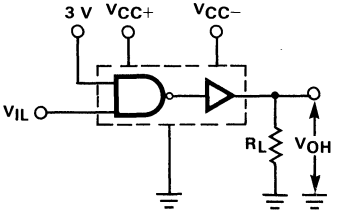


Fig. 2. V_{IL}, V_{OH}

Each input is tested separately.

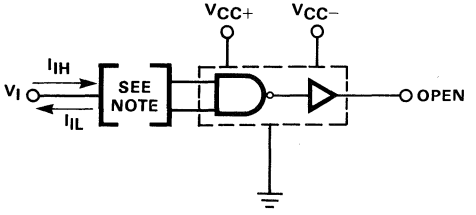


Fig. 3. I_{IH}, I_{IL}

NOTE: When testing I_{IH}, the other input is at 3 V; when testing I_L, the other input is open.

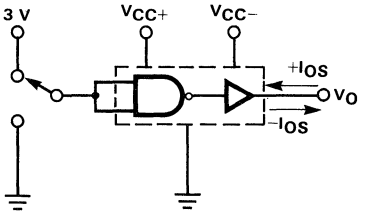


Fig. 4. I_{OS}

I_{OS} is tested for both input conditions at each of the specified output conditions.

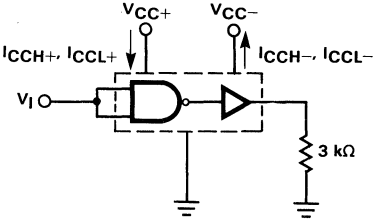


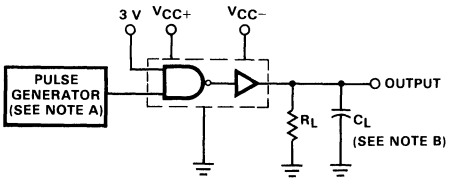
Fig. 5. I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

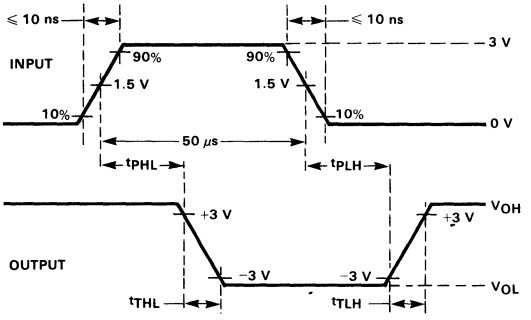
CHARACTERISTICS MEASUREMENT INFORMATION (Cont'd)

SWITCHING CHARACTERISTICS

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_{OUT} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL ELECTRICAL CHARACTERISTICS

OUTPUT CURRENT VERSUS APPLIED OUTPUT VOLTAGE

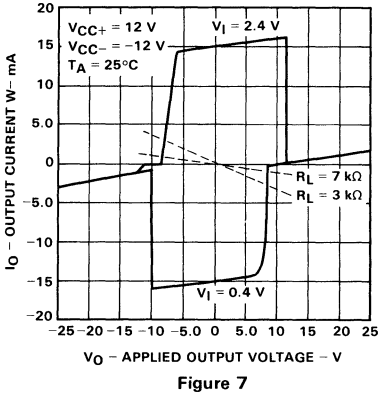


Figure 7

9612 • 9612A • 9612E

DUAL DIFFERENTIAL LINE DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 9612 Dual Differential Line Driver is designed specifically to drive single ended or differential, back matched or terminated transmission lines. The outputs are similar to totem pole TTL outputs, with active pull-up and pull-down, for use in simplex or simplex distribution bus systems. The devices feature a short circuit protected active pull-up. The inputs and outputs have clamp diodes to minimize the effect of line transients. The active pull-up output offers low output impedance allowing back matching or parallel termination of the line. The 9612E and 9612A are specified to drive 50 Ω transmission line at high speed while guaranteeing a maximum skew between outputs of less than 3.5 ns for application requiring high performance line drivers. (9613 is the functional complement).

9612/9612A/9612E

- **SINGLE 5 V SUPPLY**
- **TTL COMPATIBLE INPUTS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS**
- **COMPLEMENTARY OUTPUTS**

9612A/9612E

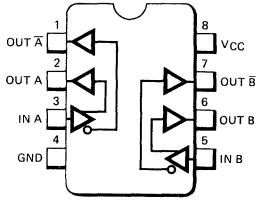
- **GUARANTEED MAXIMUM OUTPUT SKEW**
- **HIGH OUTPUT DRIVE CAPABILITY FOR 50 Ω TRANSMISSION LINES**

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	
9612A	−55°C to +125°C
9612, 9612E	0°C to +70°C
V_{CC}	+7.0 V
V_{IN}	−0.5 V to +5.5 V
Internal Power Dissipation (Note 1)	800 mW
Pin Temperature (Soldering, 10 s)	
Hermetic Mini DIP (Soldering, 60 s)	300°C
Molded Mini DIP (Soldering, 10 s)	260°C

NOTE:
1. For the Hermetic Mini DIP and Molded Mini DIP derate above 30°C at 6.7 mW/°C.

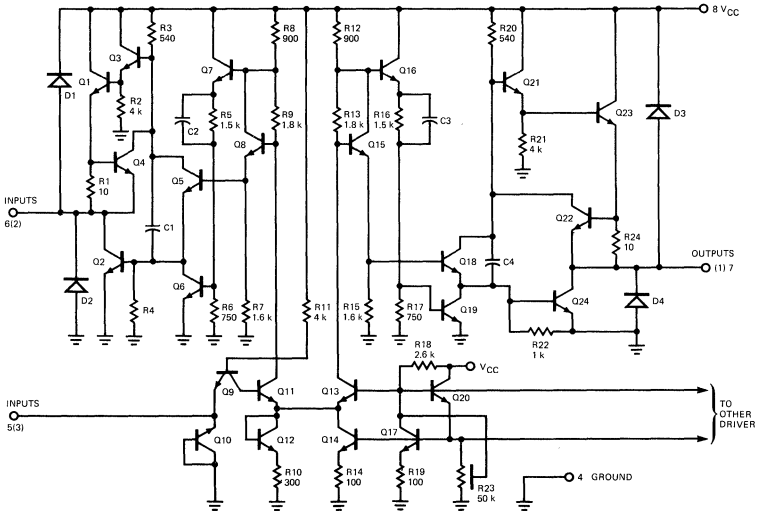
CONNECTION DIAGRAM
8-PIN MINIDIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
9612	9612TC
9612E	9612ETC
9612A	9612ARM
9612	9612RC
9612E	9612ERC

EQUIVALENT CIRCUIT (1/2 of 9612)



ELECTRICAL CHARACTERISTICS: V_{CC}= 5.0 V ± 10%, T_A= −55°C to +125°C, unless otherwise specified

SYMBOL	CHARACTERISTICS	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{OL}	Output LOW Voltage	I_{OL} = 40 mA		200	400	mV
V_{OLC}	Clamped Output LOW Voltage	I_{OLC} = −40 mA	−1.5	−0.8		V
V_{OH}	Output HIGH Voltage	I_{OH} = −40 mA	2.0	2.75		V
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V	−140	−77	−42	mA
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.0			V
I_{IL}	Input LOW Current	V_{IL} = 0.4 V	−1.6			mA
I_{IH}	Input HIGH Current	V_{IH} = 2.4 V			40	μA
I_R	Input Reverse Current	V_R = 4.5 V			1.0	mA
V_{CD}	Input Clamp Diode Voltage	V_{CC} = 4.75 V, I_{IC} = −12 mA, T = 25°C	−1.5	−0.8		V
I_{CC}	Supply Current	Inputs = 0 V, T = 25°C		42	50	mA
I_{max}	Max. Supply Current	Inputs = 0 V, V_{max} = 7.0 V, T = 25°C		59	70	mA

ELECTRICAL CHARACTERISTICS: V_{CC}= 5.0 V ±5%, T_A= 0°C to 70°C, unless otherwise specified

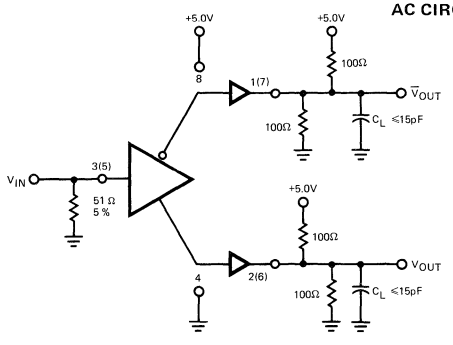
SYMBOL	CHARACTERISTICS	CONDITIONS	LIMITS						UNITS
			9612			9612E			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	Output LOW Voltage	I_{OL} = 40 mA		200	400		200	400	mV
		I_{OL} = 50 mA (9612E only)					250	400	mV
V_{OLC}	Clamped Output LOW Voltage	I_{OLC} = −40 mA	−1.5	−0.8		−1.5	−0.8		V
		I_{OLC} = −50 mA (9612E only)				−1.5	−0.9		V
V_{OH}	Output HIGH Voltage	I_{OH} = −40 mA	2.4	2.75		2.4	2.75		V
		I_{OH} = −50 mA (9612E only)				2.4	2.60		V
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V	−140	−77	−42	−140	−77	−55	mA
V_{IL}	Input LOW Voltage				0.8			0.8	V
V_{IH}	Input HIGH Voltage		2.0			2.0			V
I_{IL}	Input LOW Current	V_{IL} = 0.4 V	−1.6			−1.6			mA
I_{IH}	Input HIGH Current	V_{IH} = 2.4 V			40			40	μA
I_R	Input Reverse Current	V_R = 4.5 V			1.0			1.0	mA
V_{CD}	Input Clamp Diode Voltage	V_{CC} = 4.75 V, I_{IC} = −12 mA	−1.5	−0.8		−1.5	−0.8		V
I_{CC}	Supply Current	Inputs = 0 V		42	50		42	50	mA
I_{max}	Max. Supply Current	Inputs = 0 V, V_{max} = 7.0 V		59	70		59	70	mA

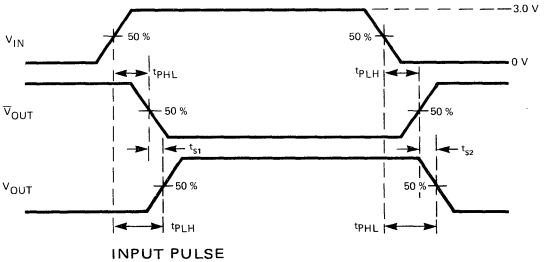
AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, R_L = 100 Ω (Note 1)

SYMBOL	CHARACTERISTICS	CONDITIONS	LIMITS						UNITS
			9612			9612A/9612E			
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Turn Off Time	R_L = 100 Ω (Note 1)			30			20	ns
t_{PHL}	Turn On Time	$C_L \leqslant$ 15 pF			30			20	ns
t_s	Output Skew	See Fig. 1				−3.5		+3.5	ns

NOTE: 1. R_L must be noninductive.

AC CIRCUIT AND WAVEFORMS



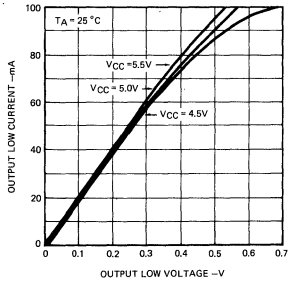


INPUT PULSE
Frequency = 2 MHz Pulse Width = 250 ±10 ns
Amplitude = 3.0 ± 0.1 V $t_r = t_f \leqslant$ 5.0 ns

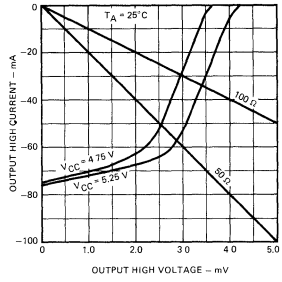
Fig. 1

TYPICAL PERFORMANCE CURVES

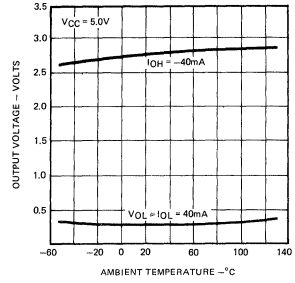
OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



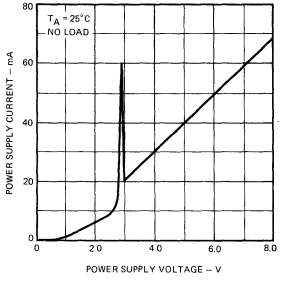
OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



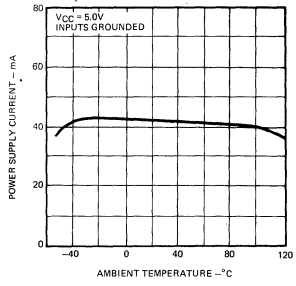
OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



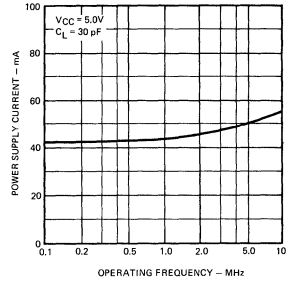
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



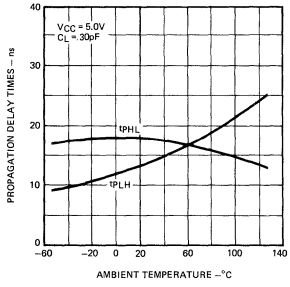
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



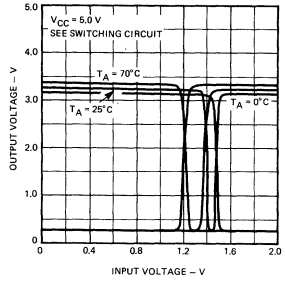
SUPPLY CURRENT AS A FUNCTION OF OPERATING FREQUENCY



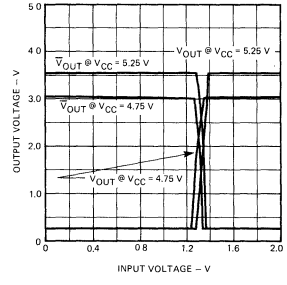
PROPAGATION DELAY TIME AS A FUNCTION OF AMBIENT TEMPERATURE



TRANSFER CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

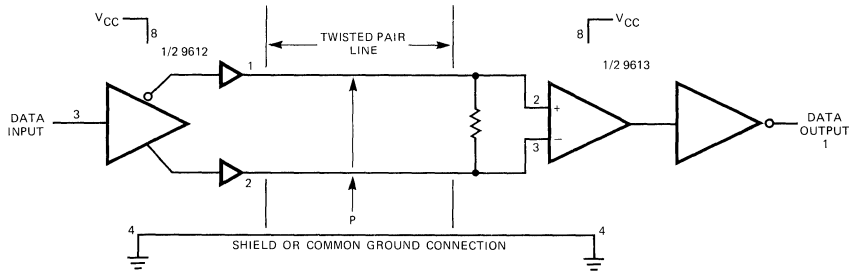


TRANSFER CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

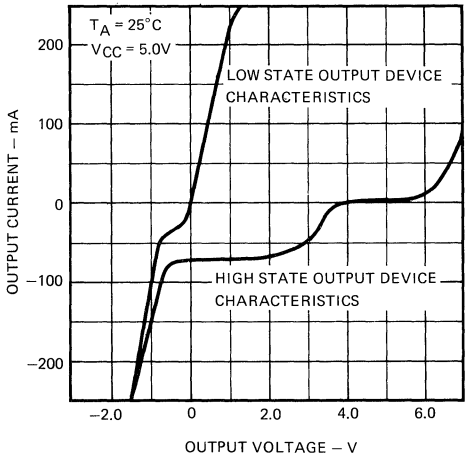


TYPICAL APPLICATIONS

SIMPLEX BALANCED DIFFERENTIAL OPERATION



TYPICAL REFLECTION DIAGRAM



6

9614

DUAL DIFFERENTIAL LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9614 is a TTL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTL, with the active pull up and the pull down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull ups on one side and the uncommitted collectors on the other (See Fig. 5). The active pull up is short circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary providing NAND and AND functions of the inputs, adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both input and output to handle line transients.

- **SINGLE 5 VOLT SUPPLY**
- **TTL COMPATIBLE INPUTS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS**
- **COMPLEMENTARY OUTPUTS FOR NAND, AND OPERATION**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR APPLICATION**
- **MILITARY TEMPERATURE RANGE**

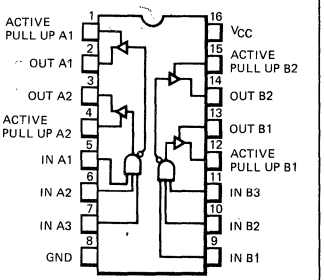
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be imparied)

Storage Temperature Range	−65°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.7 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collector)	−0.5 V to +12 V
Pin Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 1)	670 mW
Operating Temperature Range	
Military (9614)	−55°C to +125°C
Commercial (9614C)	0°C to +70°C

NOTE:

1. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 60°C.

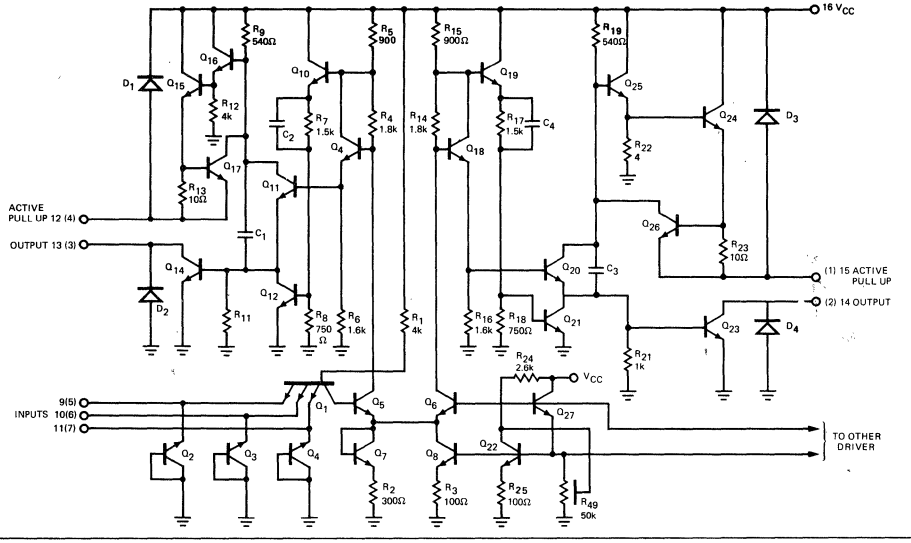
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
9614	9614DM
9614	9614FM
9614C	9614DC
9614C	9614PC

EQUIVALENT CIRCUIT (1/2 9614)



9614

ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V ± 10%.

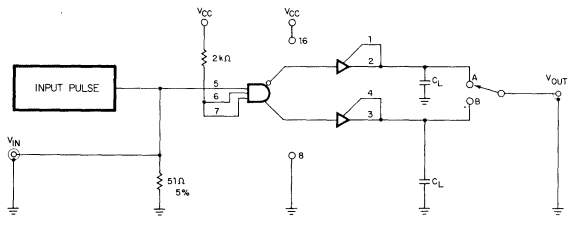
SYMBOL	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS	
		−55°C		+25°C			+125°C				
		MIN	MAX	MIN	TYP	MAX	MIN	MAX			
V_{OL}	Output LOW Voltage		400		200	400		400	mV	I_{OL} = 40 mA	V_{CC} = 4.5 V
V_{OH1}	Output HIGH Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA	V_{CC} = 4.5 V
V_{OH2}		2.0		2.0	2.6		2.0		V	I_{OH} = −40 mA	
I_{SC}	Output Short-Circuit Current			−40	−90	−120			mA	V_{OUT} = 0.0 V	V_{CC} = 5.5 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 12.0 V	V_{CC} = 5.5 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.4 V	V_{CC} = 5.5 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V	V_{CC} = 5.5 V
V_{IL}	Input LOW Voltage		0.8		1.3	0.8		0.8	V	V_{CC} = 5.5 V	
V_{IH}	Input HIGH Voltage	2.0		2.0	1.5		2.0		V	V_{CC} = 4.5 V	
V_{OLC}	Clamped Output LOW Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA	V_{CC} = 5.5 V
I_{CC}	Supply Current				34	50			mA	Inputs = 0 V	V_{CC} = 5.5 V
I_{max}	Supply Current				46	65			mA	Inputs = 0 V	V_{max} = 7.0 V
t_{PLH}	Turn-Off Time				14	20			ns	C_L = 30 pF	V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	20			ns	See Fig. 1	V_M = 1.5 V
V_{CD}	Input Clamp Diode Voltage				−1.0	−1.5			V	V_{CC} = 4.5 V	I_{IC} = −12 mA

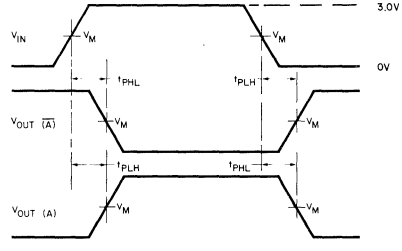
9614C

ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V ± 5%.

SYMBOL	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS	
		0°C		+25°C			+70°C				
		MIN	MAX	MIN	TYP	MAX	MIN	MAX			
V_{OL}	Output LOW Voltage		450		200	450		450	mV	I_{OL} = 40 mA	V_{CC} = 4.75 V
V_{OH1}	Output HIGH Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA	V_{CC} = 4.75 V
V_{OH2}		2.0		2.0	2.6		2.0		V	I_{OH} = −40 mA	
I_{SC}	Output Short-Circuit Current			−40	−90	−120			mA	V_{OUT} = 0.0 V	V_{CC} = 5.25 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 5.25 V	V_{CC} = 5.25 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.45 V	V_{CC} = 5.25 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V	V_{CC} = 5.25 V
V_{IL}	Input LOW Voltage		0.8		1.3	0.8		0.8	V	V_{CC} = 5.25 V	
V_{IH}	Input HIGH Voltage	2.0		2.0	1.5		2.0		V	V_{CC} = 4.75 V	
V_{OLC}	Clamped Output LOW Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA	V_{CC} = 5.25 V
I_{CC}	Supply Current				33	50			mA	Inputs = 0 V	V_{CC} = 5.25
I_{max}	Supply Current				46	70			mA	Inputs = 0 V	V_{max} = 7.0 V
t_{PLH}	Turn-Off Time				14	30			ns	C_L = 30 pF	V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	30			ns	See Fig. 1	V_M = 1.5 V
V_{CD}	Input Clamp Diode Voltage				−1.0	−1.5			V	V_{CC} = 4.75 V	I_{IC} = −12 mA

AC TEST CIRCUIT AND WAVEFORMS



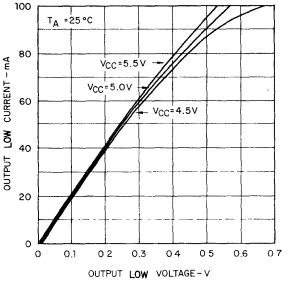


INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

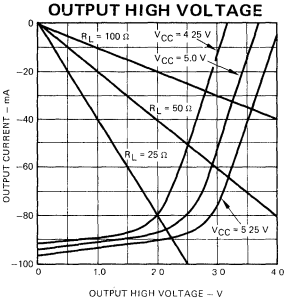
Fig. 1

TYPICAL ELECTRICAL CHARACTERISTICS

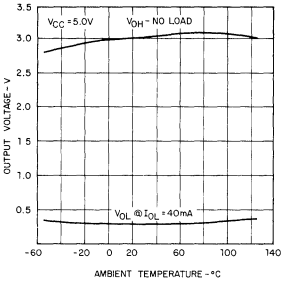
ACTIVE PULL DOWN OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



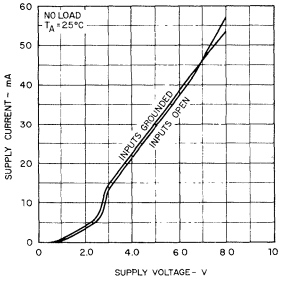
ACTIVE PULL UP OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



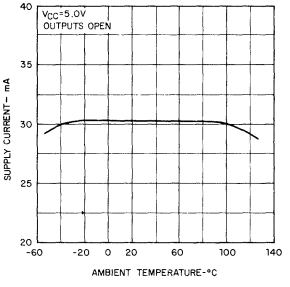
LOGIC LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



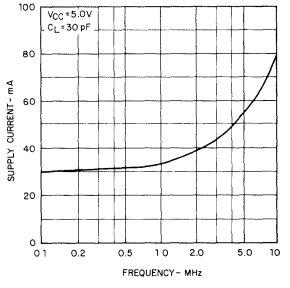
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



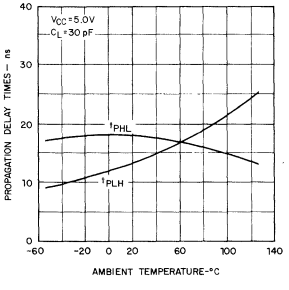
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



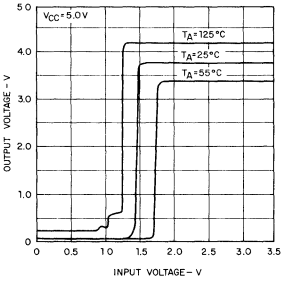
SUPPLY CURRENT AS A FUNCTION OF OPERATING FREQUENCY



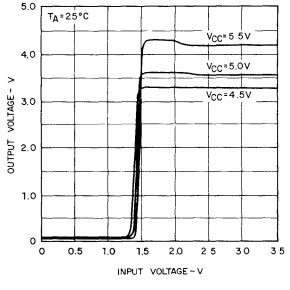
PROPAGATION DELAY TIME AS A FUNCTION OF TEMPERATURE



TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

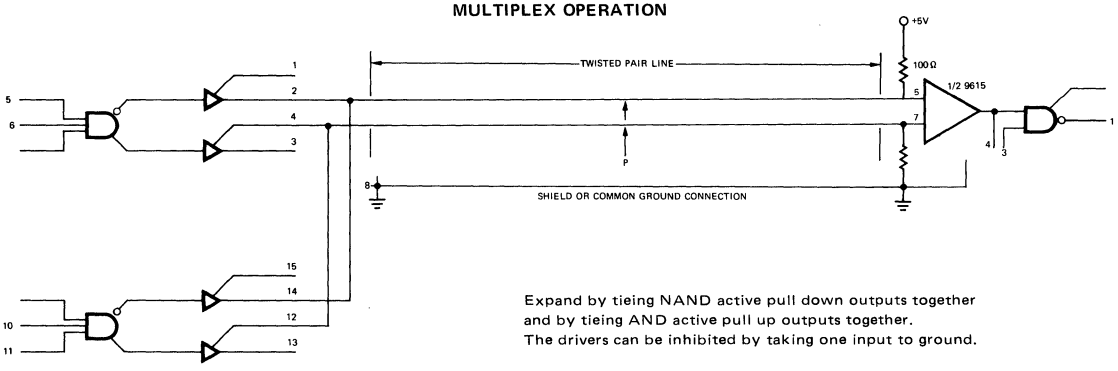


TRANSFER CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



APPLICATIONS

DIFFERENTIAL MODE EXPANSION
MULTIPLEX OPERATION

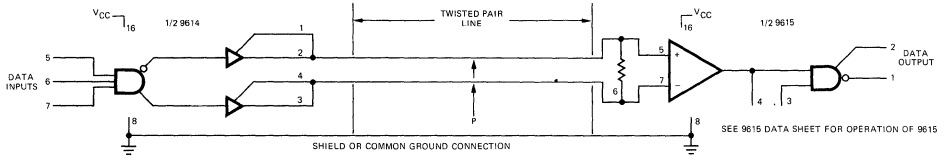


Expand by tieing NAND active pull down outputs together and by tieing AND active pull up outputs together. The drivers can be inhibited by taking one input to ground.

Fig. 2

Note: Only 1 Driver is Enabled At One Time

SIMPLEX – DIFFERENTIAL OPERATION



See 9615 Data Sheet for operation of 9615.

Fig. 3

TYPICAL REFLECTION DIAGRAM

NOTE–SEE 9621 DATA SHEET FOR USAGE OF REFLECTION DIAGRAM

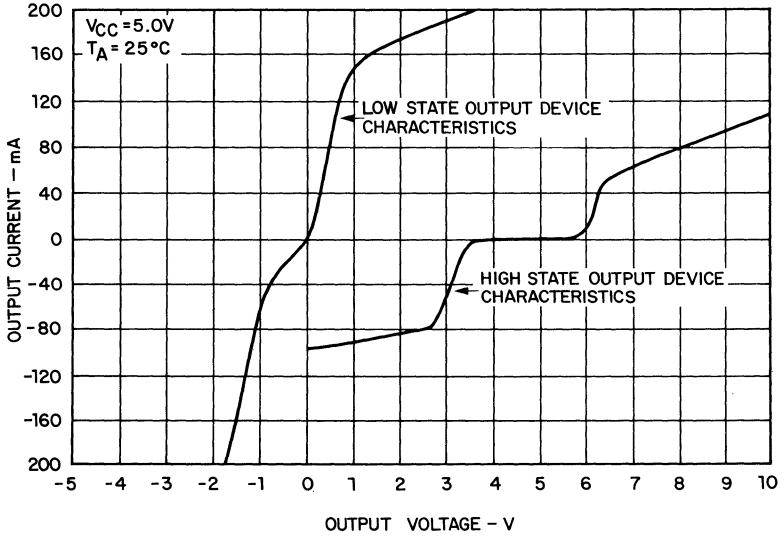


Fig. 4

9616

TRIPLE EIA RS-232-C/MIL-STD-188C LINE DRIVER

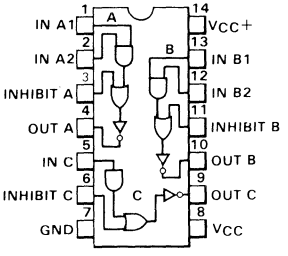
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9616 is a Triple Line Driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24 and/or MIL-STD-188C (by the appropriate device selection). Each driver converts TTL/DTL logic levels to EIA/CCITT and/or MIL-STD-188C logic levels for transmission between data terminal equipment and data communications equipment. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short-circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH on the inhibit terminal interrupts signal transfer and forces the output to a V_{OL} (EIA/CCITT MARK) state.

For the complementary function, see the 9617 Triple EIA RS-232-C Line Receiver and the 9627 Dual EIA RS-232-C and MIL-STD-188C Line Receiver.

- **INTERNAL SLEW RATE LIMITING**
- **MEETS EIA RS-232-C AND CCITT V.24 AND/OR MIL-STD-188C**
- **LOGIC TRUE INHIBIT FUNCTION**
- **OUTPUT SHORT-CIRCUIT CURRENT LIMITING**
- **OUTPUT VOLTAGE LEVELS INDEPENDENT OF SUPPLY VOLTAGES**

CONNECTION DIAGRAM
14-PIN
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
9616	9616DM
9616C	9616DC
9616E	9616EDC
9616C	9616PC
9616E	9616EPC

TRUTH TABLE

INPUT 1	INPUT 2	INHIBIT	OUTPUT
All Sections:			
L	L	L	H
H	H	L	L
L	L	H	L
H	H	H	L
For Channels A and B add:			
L	H	L	H
H	L	L	H
L	H	H	L
H	L	H	L

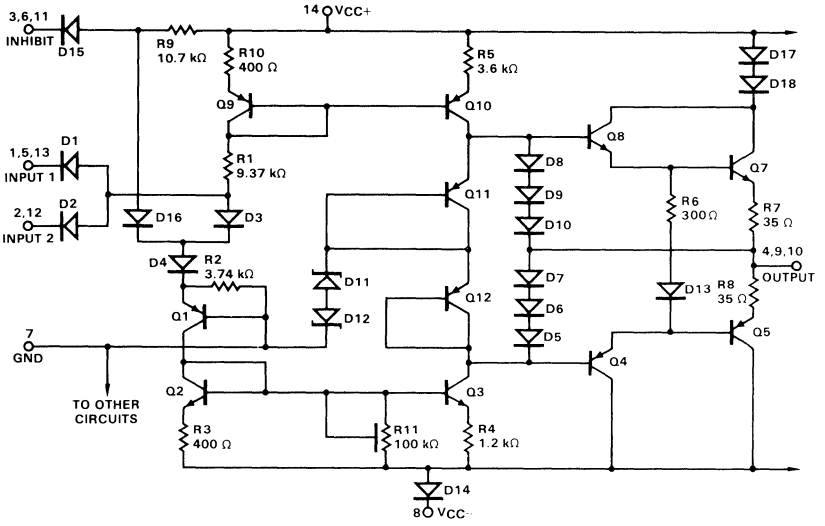
(For Channel C, omit INPUT 2 Column)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±15 V
Input or Inhibit Voltage	−1.5 V to +6.0 V
Output Signal Voltage	±15 V
Internal Power Dissipation (Note 1)	670 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
RS-232 MIL-STD-188 (9616)	−55°C to +125°C
RS-232 (9616C)	0°C to 70°C
RS-232 MIL-STD-188 (9616E)	0°C to 70°C
Pin Temperatures	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

NOTE
1 For Hermetic and Plastic DIP above 60°C derate linearly at 8.3 mW/°C.

EQUIVALENT CIRCUIT (One of three channels)



9616 AND 9616E
RS-232-C and MIL-STD-188C

DC CHARACTERISTICS: $V_{CC} = \pm 12$ V $\pm 10\%$; $R_L \geq 3$ kΩ, See Test Circuit, unless otherwise specified, Note 2

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	Output HIGH Voltage	V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8$ V	5.0	6.0	7.0	V
V_{OL}	Output LOW Voltage	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0$ V	−7.0	−6.0	−5.0	V
	Ripple Rejection	Power Supply Ripple = 2.4 Vp-p, f = 400 Hz		0.25		% of V_{OUT}
V_{OH} to V_{OL}	Output HIGH Voltage to Output LOW Voltage Magnitude Matching Error				±10	%
I_{SC+}	Positive Output Short Circuit Current	$R_L = 0$ Ω, V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8$ V	−45	−25	−12	mA
I_{SC-}	Negative Output Short Circuit Current	$R_L = 0$ Ω, $V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0$ V	+12	+25	+45	mA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	$V_{IN1} = V_{IN2} = 2.4$ V			40	μA
		$V_{IN1} = V_{IN2} = 5.5$ V			1.0	mA
I_{IL}	Input LOW Current	$V_{IN1} = V_{IN2} = 0.4$ V	−1.6	−1.2		mA
I_+	Positive Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8$ V		15	25	mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0$ V		7.5	15	
I_-	Negative Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8$ V	−1.0	0		mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0$ V	−25	−15		
R_{OUT}	Output Resistance, Power On	$R_L = 6$ kΩ, $\Delta I_L = 10$ mA		75		Ω
R_{OUT}	Output Resistance, Power Off	-2.0 V $\leq V_{OUT} \leq +2.0$ V All Inputs and Supply Pins Grounded	300			Ω

NOTES:
2. The operating temperature range for the 9616 is −55°C to +125°C and 9616E is 0°C to +70°C.
3. An external capacitor may be needed to meet signal wave shaping requirements of MIL-STD-188C at the applicable modulation rate. No external capacitor is needed to meet RS-232-C over the operating temperature range of 0°C to +70°C.

9616 AND 9616E
RS232-C and MIL-STD-188C (cont'd)

AC CHARACTERISTICS: $0 \leq T_A \leq 70°C$, Notes 2 and 3

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
	Positive Slew Rate	0 pF $\leq C_L \leq$ 2500 pF, $R_L \geq$ 3 kΩ	4.0	15	30	V/μs
	Negative Slew Rate	0 pF $\leq C_L \leq$ 2500 pF, $R_L \geq$ 3 kΩ	−30	−15	−4.0	V/μs
t_{PLH}	Propagation Delay Time	No Load		320		ns
t_{PHL}	Propagation Delay Time	No Load		320		ns

9616C
EIA RS-232-C

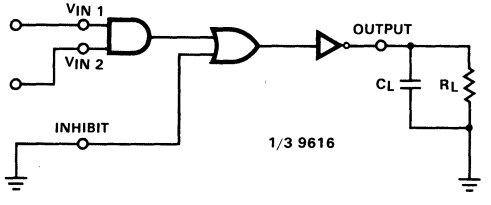
DC CHARACTERISTICS: $V_{CC} = \pm 12$ V ±10%, over operating temperature range, See Test Circuit, R_L = 3 kΩ, unless otherwise specified

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	Output HIGH Voltage	V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8$ V	5.0	6.0	7.5	V
V_{OL}	Output LOW Voltage	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0$ V	−7.5	−6.0	−5.0	V
I_{SC+}	Positive Output Short Circuit Current	$R_L = 0$ Ω, V_{IN1} and/or $V_{IN2} = V_{INHIBIT} = 0.8$ V		−25		mA
I_{SC-}	Negative Output Short Circuit Current	$R_L = 0$ Ω, $V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0$ V		25		mA
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	$V_{IN1} = V_{IN2} = 2.4$ V			40	μA
		$V_{IN1} = V_{IN2} = 5.5$ V			1.0	mA
I_{IL}	Input LOW Current	$V_{IN1} = V_{IN2} = 0.4$ V	−1.6	−1.2		mA
I_+	Positive Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8$ V		15	22	mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0$ V		7.5	13	
I_-	Negative Supply Current	$V_{IN1} = V_{IN2} = V_{INHIBIT} = 0.8$ V	−1.0	0		mA
		$V_{IN1} = V_{IN2} = V_{INHIBIT} = 2.0$ V	−22	−15		
R_{OUT}	Output Resistance, Power Off	-2.0 V $\leq V_{OUT} \leq +2.0$ V, All Inputs and Supply Pins Grounded	300			Ω

AC CHARACTERISTICS: $0 \leq T_A \leq 70°C$, Note 3

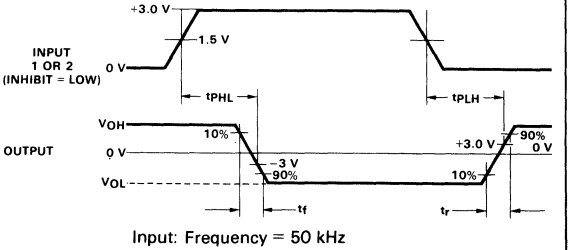
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
	Positive Slew Rate	0 pF $\leq C_L \leq$ 2500 pF, $R_L \geq$ 3 kΩ	4.0	15	30	V/μs
	Negative Slew Rate	0 pF $\leq C_L \leq$ 2500 pF, $R_L \geq$ 3 kΩ	−30	−15	−4.0	V/μs
t_{PLH}	Propagation Delay Time	No Load		320		ns
t_{PHL}	Propagation Delay Time	No Load		320		ns

AC TEST CIRCUIT



Note: Omit V_{IN2} for channel "C".

VOLTAGE WAVEFORMS



Input: Frequency = 50 kHz
Pulse Width = 20 μs
t_r and t_f = 10 ± 5 ns

9634

DUAL 3-STATE DIFFERENTIAL LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

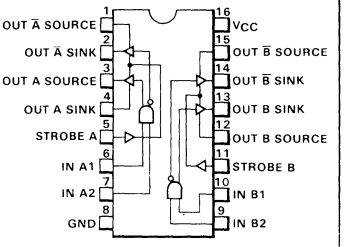
GENERAL DESCRIPTION — The 9634 Dual 3-state Line Driver is designed specifically to meet the EIA standard RS-422. It provides unipolar differential drive to twisted-pair or parallel-wire transmission lines. The outputs are similar to totem-pole TTL circuits but with the active pull-up and pull-down circuits split and brought out to adjacent pins. The active pull-up circuit is short circuit protected. In addition to the normal low-impedance HIGH and LOW states, the 9634 outputs provide a high-impedance OFF state, which is controlled by the output STROBE function. When the output control (STROBE) is HIGH, the associated outputs are high-impedance states neither driving nor loading the line permitting flexibility in party-line or bus applications. The 9634 is specified to drive 50Ω terminated transmission lines at high speeds. The inputs are TTL and CMOS compatible.

- **HIGH-IMPEDANCE OUTPUT STATE FOR PARTY-LINE APPLICATIONS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **HIGH-OUTPUT DRIVE CAPABILITY FOR 50 Ω TRANSMISSION LINES**
- **INDIVIDUAL OUTPUT CONTROLS**
- **INPUT CLAMP DIODES**
- **SCHOTTKY TECHNOLOGY**
- **COMPLEMENTARY OUTPUTS**
- **MEETS THE EIA-RS-422 SPECIFICATION FOR A BALANCED DRIVER**
- **"GLITCHLESS" DIFFERENTIAL OUTPUT**
- **DELAY TIME INCENSITIVE TO BOTH V_{CC} AND TEMPERATURE**

ABSOLUTE MAXIMUM RATINGS

V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +7.0 V
Internal Power Dissipation	800 mW
Operating Temperature	
9634DM	−55°C to +125°C
9634DC, 9634PC	0°C to 70°C
Storage Temperature	−65°C to +150°C
Pin Temperature	
Molded DIP (Soldering, 10 s)	260°C
Hermetic DIP (Soldering, 30 s)	300°C

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
9634	9634DM
9634	9634DC
9634	9634PC

RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTICS	9634DM			9634DC, 9634PC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
I_{OH}	Output HIGH Current			−50			−50	mA
I_{OL}	Output LOW Current			50			50	mA
T_A	Ambient Temperature	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS: Over recommended ambient temperature, unless otherwise noted.

SYMBOL	CHARACTERISTICS	CONDITIONS (Notes 1 and 2)		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage	9634DC, 9634PC				0.8	V
		9634DM, 9634FM				0.7	
V_I	Clamped Input Voltage	V_{CC} = Min, I_{IN} = 18 mA			−1.0	−1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IH} = V_{IH} Min, V_{IL} = V_{IL} Max	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IH} = V_{IH} Min, V_{IL} = V_{IL} Max, I_{OL} = 50 mA				0.5	V
I_{IN}	Input Current at Maximum Input Voltage	V_{CC} = Max, V_{IN} Max = 5.5 V				50	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IH} = 2.7 V				25	μA
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IL} = 0.5 V				−200	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, V_{OUT} = 0 V		−50		−150	mA
$V_T/\overline{V}_T$	Terminated Output Voltage	See Figure 1		2.0			V
$\lvert V_T - \overline{V}_T \rvert$	Output Balance	See Figure 1				0.4	V
$\lvert V_{OS} \rvert, \lvert \overline{V}_{OS} \rvert$	Output Offset Voltage					3.0	V
$\lvert V_{OS} \rvert - \lvert \overline{V}_{OS} \rvert$	Output Offset Balance					0.4	V
$\lvert I_x \rvert$	Output Leakage Current	−0.25 V < Vx < 6.0 V				100	μA
I_{CC}	Supply Current (both drivers)	All input at 0 V, V_{CC} = 5.5 V, no load			48	69	mA
I_{OZ}	Off State High-Impedance State (I_{OUT})	V_{CC} = Max, Strobe input at V_{IL} Max	V_{OUT} = 2.4 V	−200		+200	μA
			V_{OUT} = 0.4 V				

NOTES:
1. Use Min/Max values specified in recommended operating conditions.
2. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.

TERMINATED OUTPUT VOLTAGE AND OUTPUT BALANCE

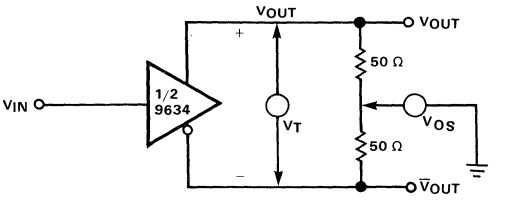
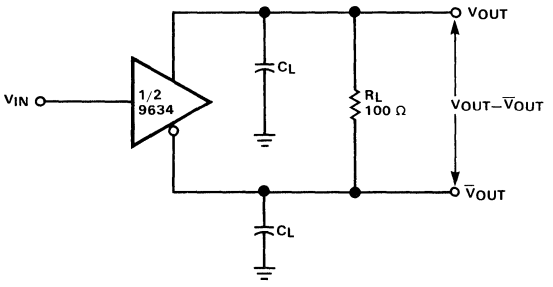


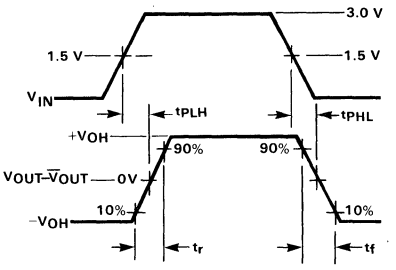
Fig. 1.

AC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} t_{PLH}	Propagation Delay	T_A = 25°C, C_L = 15 pF (Note 2), See Fig. 2		10 10	15 15	ns ns
t_f	Fall Time, 90% – 10%	T_A = 25°C, C_L = 15 pF (Note 2), R_L = 100 Ω See Fig. 2		10	15	ns
t_r	Rise Time, 10% – 90%			10	15	ns
$t_{PA} - t_{P\overline{A}}$	Skew Between Two Outputs			1.0		ns

AC RISE AND FALL TIME TEST CIRCUIT AND WAVEFORMS



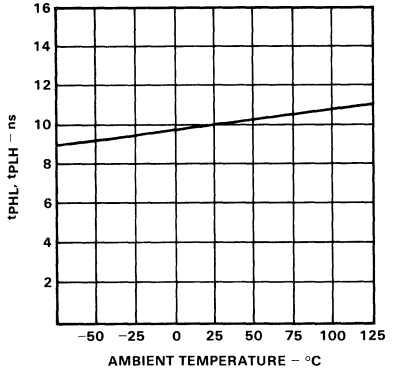


NOTES:

1. The pulse generator has the following characteristics:
   Z_{OUT} = 50 Ω, PRR = 500 kHz
   t_w = 100 ns
2. C_L includes probe and jig capacitance.

Fig. 2.

TYPICAL DELAY CHARACTERISTICS



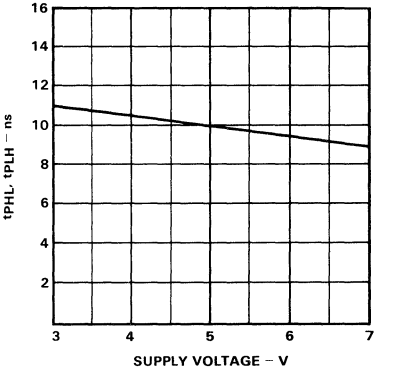


Fig. 3.

9636A

DUAL PROGRAMMABLE SLEW RATE LINE DRIVER (EIA RS-423 DRIVER)

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9636A is a TTL/CMOS compatible, dual, single-ended, line driver which has been specifically designed to satisfy the requirements of EIA Standard RS-423.

The 9636A suitable for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between the wave shaping control (WS) pin and ground. This eliminates any need for external filtering of the output signals. Output voltage levels and slew rates are independent of power supply variations. Current limiting is provided in both output states. The 9636A is designed for nominal power supplies of ±12 V.

Inputs are TTL compatible with input current loading low enough (1/10 U.L.) to be also compatible with CMOS logic. Clamp diodes are provided on the inputs to limit transients below ground.

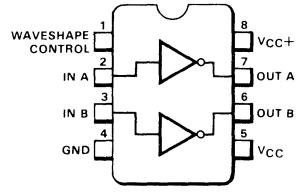
- **PROGRAMMABLE SLEW RATE LIMITING**
- **MEETS EIA RS-423 REQUIREMENTS**
- **AVAILABLE IN COMMERCIAL OR MILITARY TEMPERATURE RANGE**
- **OUTPUT SHORT-CIRCUIT PROTECTION**
- **TTL AND CMOS COMPATIBLE INPUTS**

ABSOLUTE MAXIMUM RATINGS

V_{CC}+ Pin Potential to Ground Pin		V_{CC}- to +15 V
V_{CC}- Pin Potential to Ground Pin		+0.5 to -15 V
V_{CC}+ Pin Potential to V_{CC}- Pin		0 to +30 V
Output Potential to Ground Pin		±15 V
Output Source Current		-150 mA
Output Sink Current		150 mA
Internal Power Dissipation (Note)	9T	1.3 W
	6T	1.15 W
Operating Temperature		
Military (9636ARM)		-55° C to 125° C
Commercial (9636ARC, 9636ATC)		0° C to 70° C
Storage Temperature		-65° C to 150° C
Pin Temperature		
Molded DIP (Soldering, 10 s)		260° C
Hermetic DIP (Soldering, 60 s)		300° C

NOTE:
1. Derate at 7.7 mW/°C for ambient temperatures above 25°C for 6T package and derate 11.1 mW/°C for 9T package.

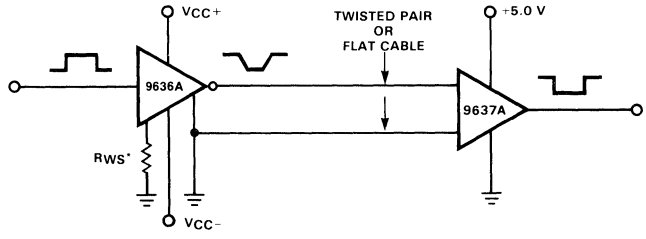
CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



ORDER INFORMATION

TYP	PART NO.
9636A	9636ARM
9636A	9636ARC
9636A	9636ATC

RS-423 SYSTEM APPLICATION



RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	9636ARM			9636ARC, 9636ATC			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Positive Supply Voltage (V_{CC+})	10.8	12	13.2	10.8	12	13.2	V
Negative Supply Voltage (V_{CC-})	-13.2	-12	-10.8	-13.2	-12	-10.8	V
Operating Ambient Temperature (T_A)	-55	25	125	0	25	70	°C
Wave Shaping Resistance (R_{WS})	10		500	10		1000	kΩ

ELECTRICAL CHARACTERISTICS: Over recommended temperature supply voltage and wave shaping resistance ranges unless noted.

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH1}	Output High Voltage	R_L to GND ($R_L = \infty$)	5.0	5.6	6.0	V
V_{OH2}		R_L to GND (R_L = 3 kΩ)	5.0	5.6	6.0	V
V_{OH3}		R_L to GND (R_L = 450Ω)	4.0	5.5	6.0	V
V_{OL1}	Output Low Voltage	R_L to GND ($R_L = \infty$)	-6.0	-5.7	-5.0	V
V_{OL2}		R_L to GND (R_L = 3 kΩ)	-6.0	-5.6	-5.0	V
V_{OL3}		R_L to GND (R_L = 450Ω)	-6.0	-5.4	-4.0	V
R_O	Output Resistance	450 Ω ≤ R_L		25	50	Ω
I_{SC+}	Output Short Circuit Current	V_{OUT} = 0 V, V_{IN} = 0 V (see note)	-150	-60	-15	mA
I_{SC-}	Output Short Circuit Current	V_{OUT} = 0 V, V_{IN} = 2.0 V (see note)	15	60	150	mA
I_{OX}	Output Leakage Current	V_{OUT} = ±6 V, Power-Off	-100		100	μA
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
V_{CD}	Input Clamp Diode	I_{IN} = 15 mA	-1.5	-1.1		V
I_{IL}	Input Low Current	V_{IN} = 0.4 V	-80	-16		μA
I_{IH}	Input High Current	V_{IN} = 2.4 V		1.0	10	μA
		V_{IN} = 5.5 V		10	100	μA
I_{CC+}	Positive Supply Current	V_{CC+} = +12 V, V_{CC-} = -12 V $R_L = \infty$, R_{WS} = 100 kΩ, V_{IN} = 0 V		13	18	mA
I_{CC-}	Negative Supply Current	V_{CC+} = +12 V, V_{CC-} = -12 V $R_L = \infty$, R_{WS} = 100 kΩ, V_{IN} = 0 V	-18	-13		mA

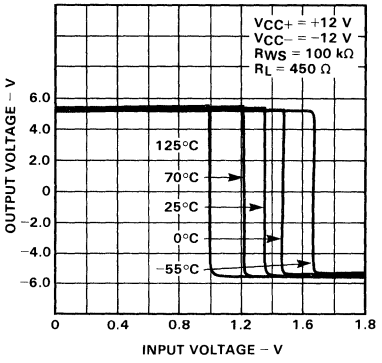
AC CHARACTERISTICS: T_A = 25° C, V_{CC} = ±12 V ± 10%, see AC Test Circuit

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
t_r	Output Rise Time	R_{WS} = 10 kΩ	0.8	1.1	1.4	μs
		R_{WS} = 100 kΩ	8.0	11	14	μs
		R_{WS} = 500 kΩ	40	55	70	μs
		R_{WS} = 1000 kΩ	80	110	140	μs
t_f	Output Fall Time	R_{WS} = 10 kΩ	0.8	1.1	1.4	μs
		R_{WS} = 100 kΩ	8.0	11	14	μs
		R_{WS} = 500 kΩ	40	55	70	μs
		R_{WS} = 1000 kΩ	80	110	140	μs

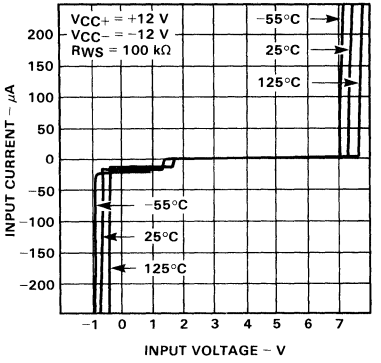
NOTE: Only one output should be shorted at a time.

TYPICAL ELECTRICAL CHARACTERISTICS

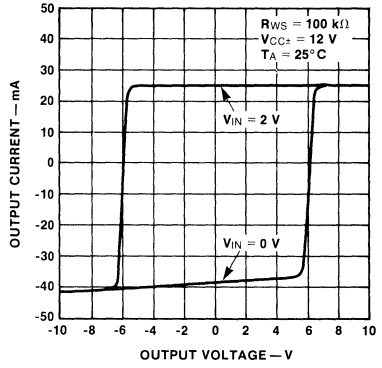
INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF TEMPERATURE



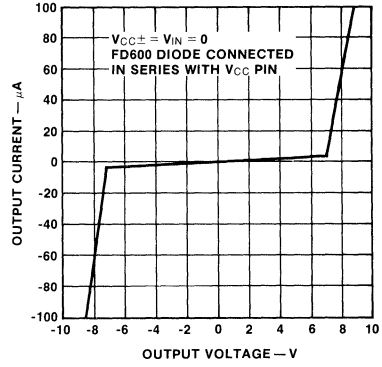
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



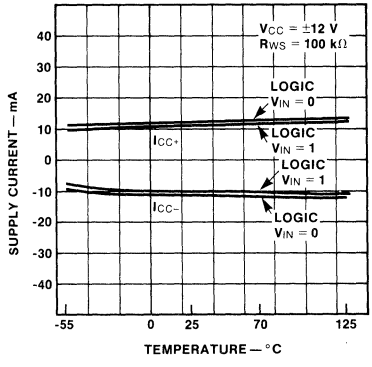
OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE (POWER OFF)



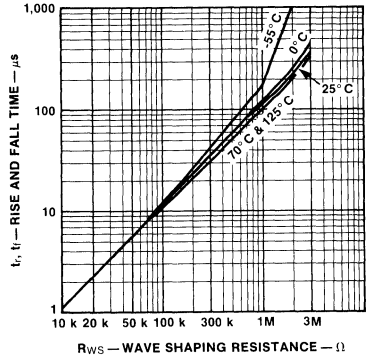
OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE (POWER ON)



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

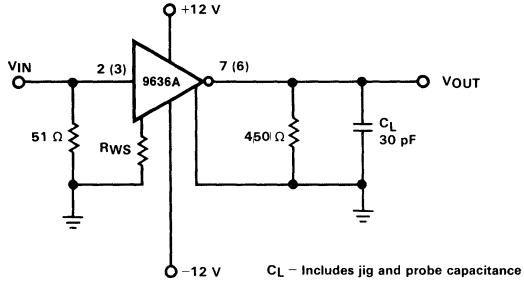


TRANSITION TIME AS A FUNCTION OF R_{WS}



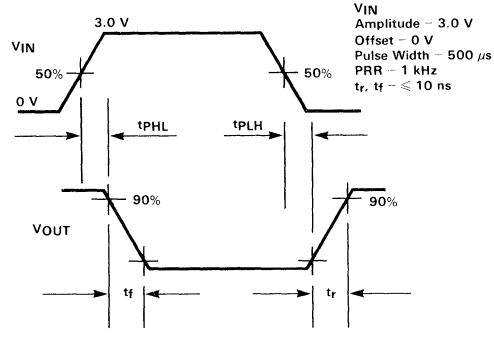
SWITCHING TEST CIRCUIT AND AC WAVEFORMS

TEST CIRCUIT



C_L – Includes jig and probe capacitance

AC WAVEFORMS



9638

DUAL HIGH SPEED DIFFERENTIAL LINE DRIVER (EIA-RS-422)

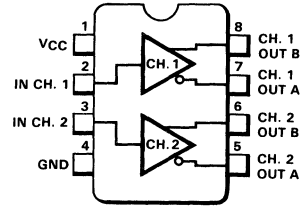
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9638 is a Schottky, TTL-compatible Dual Channel Differential Line Driver, designed specifically to meet the EIA-RS-422 specifications. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem-pole TTL outputs, with active pull-up and pull-down. The device features a short-circuit protected active pull-up with low output impedance and is specified to drive 50 Ω transmission lines at high speed. The mini DIP provides high package density.

- **SINGLE 5 V SUPPLY**
- **SCHOTTKY TECHNOLOGY**
- **TTL AND CMOS COMPATIBLE INPUTS**
- **OUTPUT SHORT-CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **COMPLEMENTARY OUTPUTS**
- **MINIMUM OUTPUT SKEW (<1 ns TYPICAL)**
- **50 mA OUTPUT DRIVE CAPABILITY FOR 50 Ω TRANSMISSION LINES**
- **MEETS EIA-RS-422 SPECIFICATIONS**
- **PROPAGATION DELAY OF LESS THAN 10 ns**
- **"GLITCHLESS" DIFFERENTIAL OUTPUT**
- **DELAY TIME STABLE WITH V_{CC} AND TEMPERATURE VARIATIONS (<2 ns TYPICAL) (FIG. 3)**

CONNECTION DIAGRAM
8-PIN DIP

PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



ORDER INFORMATION

TYPE	PART NO.
9638	9638RM
9638	9638RC
9638	9638TC

ABSOLUTE MAXIMUM RATINGS

V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +7.0 V
Internal Power Dissipation	800 mW
Operating Temperature	
9638RM	−55°C to +125°C
9638RC,9638TC	0°C to 70°C
Storage Temperature	−65°C to +150°C
Pin Temperature	
Molded DIP (Soldering, 10 s)	260°C
Hermetic DIP (Soldering, 30 s)	300°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	CHARACTERISTICS	9638RM			9638RC, 9638TC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
I_{OH}	Output HIGH Current			−50			−50	mA
I_{OL}	Output LOW Current			50			50	mA
T_A	Ambient Temperature	−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS: Over recommended ambient temperature, unless otherwise noted.

SYMBOL	CHARACTERISTICS	CONDITIONS (Notes 1 and 2)		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage	9638RC, 9638TC				0.8	V
		9638RM				0.7	
V_I	Clamped Input Voltage	V_{CC} = Min, I_{IN} = −18 mA			−1.0	−1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IH} = V_{IH} Min, V_{IL} = V_{IL} Max	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IH} = V_{IH} Min, V_{IL} = V_{IL} Max, I_{OL} = 40 mA				0.5	V
I_{IN}	Input Current at Maximum Input Voltage	V_{CC} = Max, V_{IN} Max = 5.5 V				50	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IH} = 2.7 V				25	μA
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IL} = 0.5 V				−200	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, V_{OUT} = 0 V		−50		−150	mA
V_T, $\overline{V}_T$	Terminated Output Voltage	See Figure 1		2.0			V
$V_T - \overline{V}_T$	Output Balance					0.4	V
V_{OS}, $\overline{V}_{OS}$	Output Offset Voltage					3.0	V
$V_{OS} - \overline{V}_{OS}$	Output Offset Balance					0.4	V
I_x	Output Leakage Current	−0.25 V < Vx < 6.0 V				100	μA
I_{CC}	Supply Current (both drivers)	All input at 0 V, V_{CC} = 5.5 V, no load			45	65	mA

NOTES:
1. Use MIN/MAX values specified in recommended operating conditions.
2. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.

DC TEST CIRCUIT

TERMINATED OUTPUT VOLTAGE AND OUTPUT BALANCE

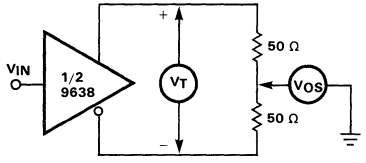


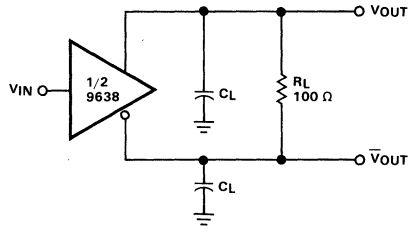
Fig. 1

AC CHARACTERISTICS

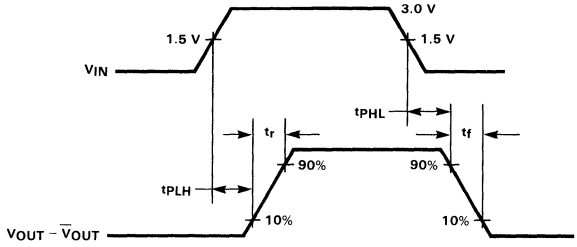
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} t_{PLH}	Propagation Delay	T_A = 25°C, C_L = 15 pF (Note 2), R_L = 100 Ω, See Fig. 2		10 10	15 15	ns ns
t_f	Fall Time, 90% – 10%			10	15	ns
t_r	Rise Time, 10% – 90%			10	15	ns
$t_{PA} - t_{PB}$	Skew Between Outputs A and B			1		ns

AC TEST CIRCUIT AND VOLTAGE WAVEFORM

AC TEST CIRCUIT



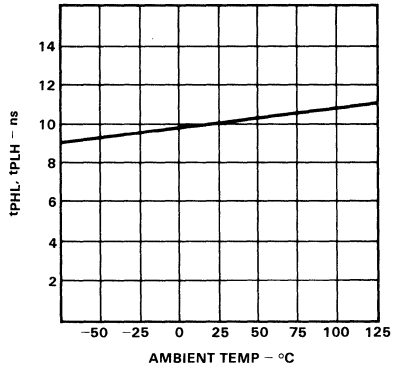
VOLTAGE WAVEFORM



NOTES:
1. The pulse generator has the following characteristics:
   Z_{OUT} = 50 Ω, PRR = 500 kHz
   t_w = 100 ns, t_r = ⩽ 5 ns
2. C_L includes probe and jig capacitance.

Fig. 2

TYPICAL DELAY CHARACTERISTICS



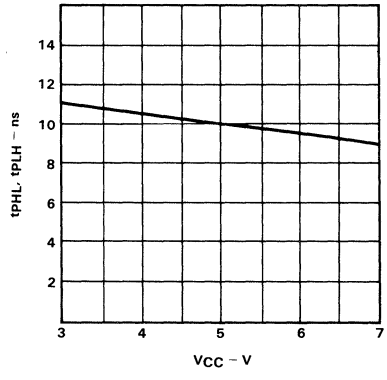


FIG. 3

μA1489 • μA1489A

QUAD LINE RECEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA1489 and the μA1489A are EIA RS-232C specified Quad Line Receivers. These devices are used to interface data terminals with data communications equipment. The μA1489 and μA1489A are pin-for-pin replacements of the MC1489 and MC1489A respectively.

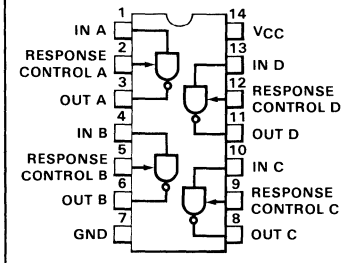
- **INPUT RESISTANCE – 3.0 kΩ TO 7.0 kΩ**
- **INPUT SIGNAL RANGE – ±30 V**
- **INPUT THRESHOLD HYSTERESIS BUILT IN**
- **RESPONSE CONTROL**
  - **a) LOGIC THRESHOLD SHIFTING**
  - **b) INPUT NOISE FILTERING**

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+10 Vdc
Input Voltage Range	±30 Vdc
Output Load Current	20 mA
Continuous Total Power Dissipation (Note 1)	800 mW
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +175°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Note 1: Above 60°C ambient temperature, derate linearly at 8.3 mW/°C.

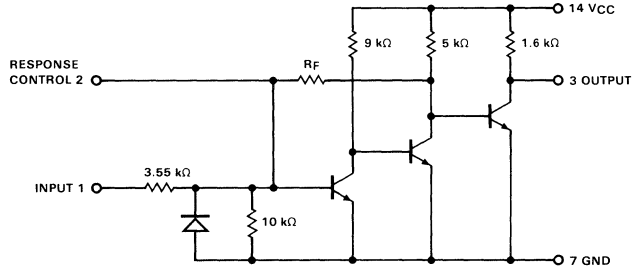
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYP	PART NO.
μA1489	μA1489DC
μA1489	μA1489PC
μA1489A	μA1489ADC
μA1489A	μA1489APC

CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	μA1489	μA1489A
RF	10 kΩ	2 kΩ

ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V ±1%, Response control pin is open, T_A = 0°C to 70°C unless otherwise noted.

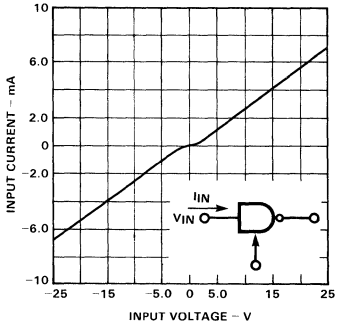
SYMBOL	CHARACTERISTICS	CONDITIONS		FIG	MIN	TYP	MAX	UNITS
I_{IH}	Positive Input Current	V_{IH} = 25 V V_{IH} = 3.0 V		1	3.6 0.43		8.3	mA
I_{IL}	Negative Input Current	V_{IL} = −25 V V_{IL} = −3.0 V		1	−3.6 −0.43		−8.3	mA
V_{IHL}	Input Turn-on Threshold Voltage	T_A = 25°C, $V_{OL} \leq$ 0.45 V	μA1489	2	1.0		1.5	V
			μA1489A		1.75	1.95	2.25	
V_{ILH}	Input Turn-off Threshold Voltage	T_A = 25°C, $V_{OH} \geq$ 2.5 V, I_L = −0.5 mA	μA1489	2	0.75		1.25	V
			μA1489A		0.75	0.8	1.25	
V_{OH}	Output HIGH Voltage	V_{IH} = 0.75 V, I_L = −0.5 mA Input open circuit, I_L = −0.5 mA		2	2.6	4.0	5.0	V
V_{OL}	Output LOW Voltage	V_{IL} = 3.0 V, I_L = 10 mA		2		0.2	0.45	V
I_{OS}	Output Short-circuit Current			3		3.0		mA
I_{CC}	Power Supply Current	V_{IH} = 5.0 V		4		20	26	mA
P_C	Power Consumption	V_{IH} = 5.0 V		4		100	130	mW

AC CHARACTERISTICS: V_{CC} = 5.0 V ±1%, T_A = 25°C

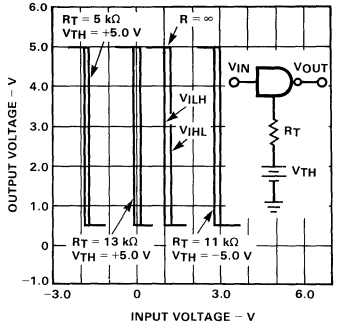
SYMBOL	CHARACTERISTICS	CONDITIONS	FIG.	MIN	TYP	MAX	UNITS
t_{PLH} t_{PHL}	Propagation Delay Time	R_L = 3.9 kΩ R = 390 Ω	5		25 25	85 50	ns
t_r	Rise Time	R_L = 3.9 kΩ	5		120	175	ns
t_f	Fall Time	R_L = 390 Ω			10	20	

TYPICAL PERFORMANCE CURVES

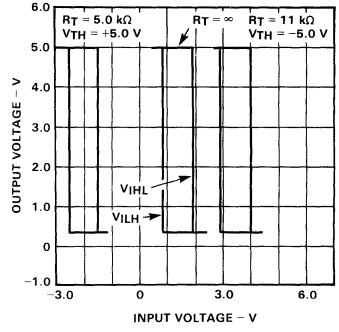
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



μA1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT



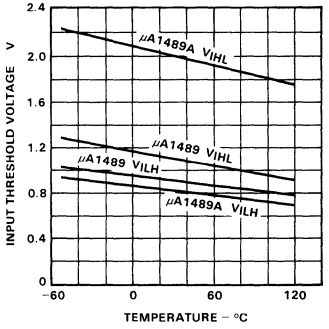
μA1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT



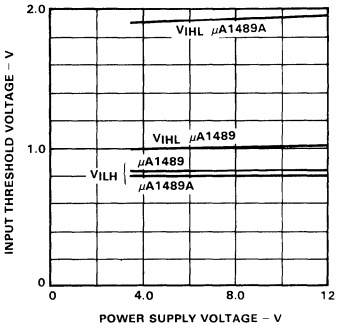
TEST CIRCUIT SAME AS μA1489

TYPICAL PERFORMANCE CURVES (Cont'd)

INPUT THRESHOLD VOLTAGE AS A FUNCTION OF TEMPERATURE



INPUT THRESHOLD VOLTAGE AS A FUNCTION OF POWER SUPPLY VOLTAGE



DC TEST CIRCUITS

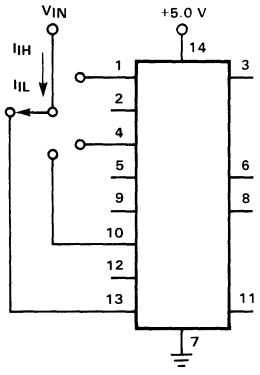


Fig. 1. Input Current

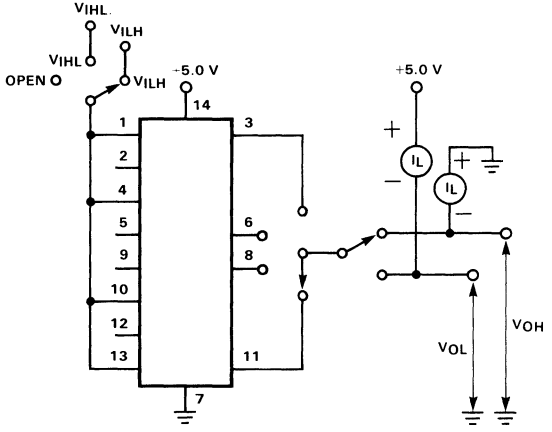


Fig. 2. Output Voltage and Input Threshold Voltage

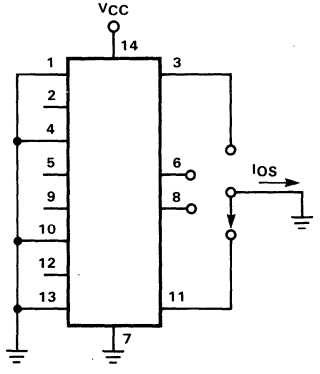


Fig. 3. Output Short-Circuit Current

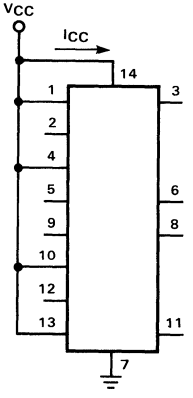
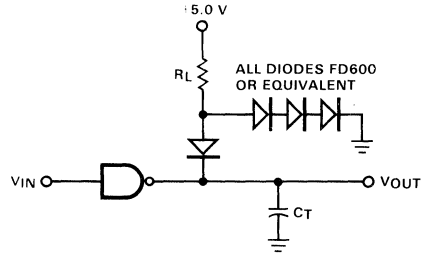
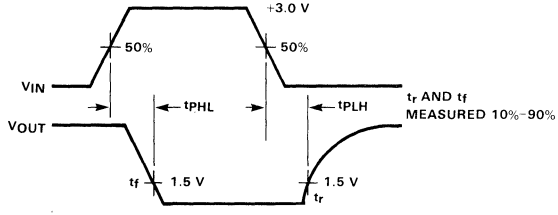


Fig. 4. Power Supply Current

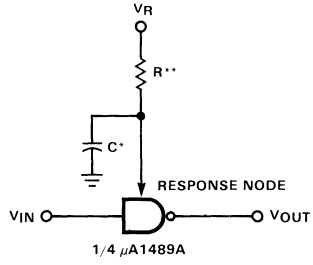
DC TEST CIRCUITS (Cont'd)





C_T = 15 pF = Total parasitic capacitance, which includes probe and jig capacitance.

Fig. 5. AC Test Circuit and Voltage Waveforms



*Capacitor is for noise filtering
**Resistor is for threshold shifting

Fig. 6. Response Control Node

μA8T14 • 55122 • 75122

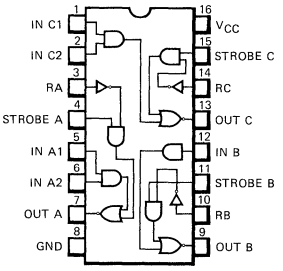
TRIPLE LINE RECEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55122/75122/μA8T14 Triple Line Receiver is designed to receive digital information from coaxial cable, strip line, or twisted pair single ended transmission lines. High input impedance (≈30 kΩ) presents minimal loading to the transmission lines in multiple receiver applications. The 55122/75122/μA8T14 has built-in hysteresis which makes it ideal for such applications as Schmitt triggers, one-shots, and oscillators. Use the 75124 or 8T24 triple line receiver where IBM System/360 I/O Interface Specification must be met.

- **BUILT-IN INPUT THRESHOLD HYSTERESIS**
- **HIGH SPEED**
- **INDEPENDENT CHANNEL STROBING**
- **FANOUT OF 10 TTL LOADS**
- **SINGLE +5.0 V SUPPLY OPERATION**

CONNECTION DIAGRAM
16-PIN
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1) R Input	+6.0 V
1, 2 or S Input	+5.5 V
Output Voltage (Note 1)	+6.0 V
Supply Voltage (Note 1)	+6.0 V
Output Current	±100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (55122, μA8T14DM)	−55°C to +125°C
Commercial (75122)	0°C to +70°C
Pin Temperatures	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 2)	800 mW

FUNCTION TABLE

INPUTS				OUTPUT
1	2*	R	S	
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = HIGH
L = LOW
X = Don't Care

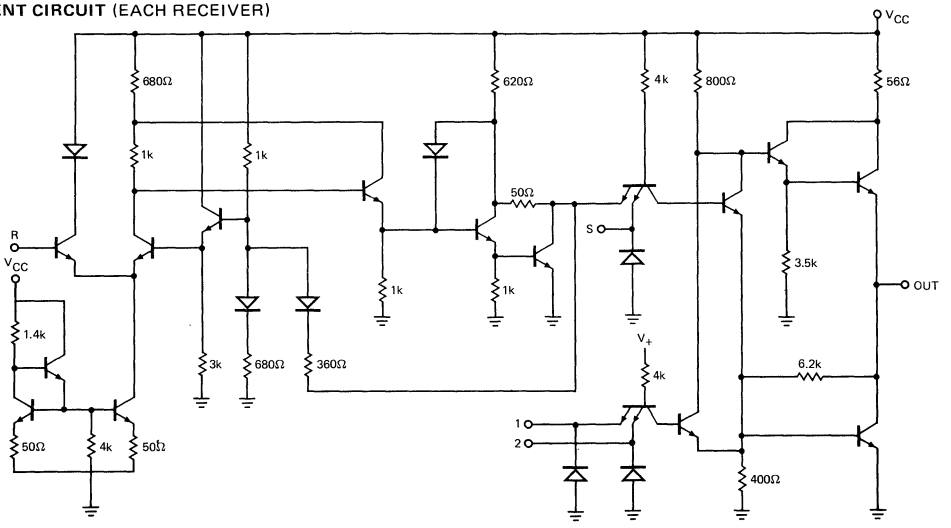
*Input 2 and last two lines of the Function Table are applicable to receivers A and C only.

ORDER INFORMATION

TYPE	PART NO.
μA8T14 or 55122	μA8T14/55122DM
μA8T14 or 75122	μA8T14/75122DC
μA8T14 or 75122	μA8T14/75122PC

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP.

EQUIVALENT CIRCUIT (EACH RECEIVER)



RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}		4.75	5.0	5.25	V
Output HIGH Current, I_{OH}				−500	μA
Output LOW Current, I_{OL}				16	mA
Operating Ambient Temperature, T_A	55122/8T14	−55		125	°C
	75122/8T14	0		70	°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 4.75 V to 5.25 V, T_A = 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage	All Inputs		2.0			V
V_{IL}	Input LOW Voltage	All Inputs				0.8	V
$V_{T+} - V_{T-}$	Hysteresis†	R	V_{CC} = 5.0 V, T_A = 25°C	0.3	0.6		V
V_{IN}	Input Clamp Voltage	In 1, 2 or S	V_{CC} = 5.0 V, I_{IN} = −12 mA			−1.5	V
$V_{(BR)IN}$	Input Breakdown Voltage	In 1, 2 or S	V_{CC} = 5.0 V, I_{IN} = 10 mA	5.5			V
V_{OH}	Output HIGH Voltage		V_{IH} = 0 V, V_{IL} = 0.8 V, I_{OH} = −500 μA, See Note 3	2.6			V
			$V_{IN(A)}$ = 0 V, $V_{IN(B)}$ = 0 V, $V_{IN(S)}$ = 2.0 V, $V_{IN(R)}$ = 1.45 V (See Note 4, I_{OH} = −500 μA	2.6			
V_{OL}	Output LOW Voltage		V_{IH} = 2.0 V, V_{IL} = 0.8 V, I_{OL} = 16 mA, See Note 3			0.4	V
			$V_{IN(A)}$ = 0 V, $V_{IN(B)}$ = 0 V, $V_{IN(S)}$ = 2.0 V, $V_{IN(R)}$ = 1.45 V (See Note 5), I_{OL} = 16 mA			0.4	
I_{IH}	Input HIGH Current	In 1, 2 or S	V_{IN} = 4.5 V			40	μA
		R	V_{IN} = 3.8 V			170	
I_{IL}	Input LOW Current	In 1, 2 or S	V_{IN} = 0.4 V	−0.1		−1.6	mA
I_{OS}	Short-Circuit Output Current‡		V_{CC} = 5.0 V, T_A = 25°C	−50		−100	mA
I_{CC}	Supply Current		V_{CC} = 5.25 V			72	mA

†Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Hysteresis Test Circuit.

‡Not more than one output should be shorted at a time.

NOTES:

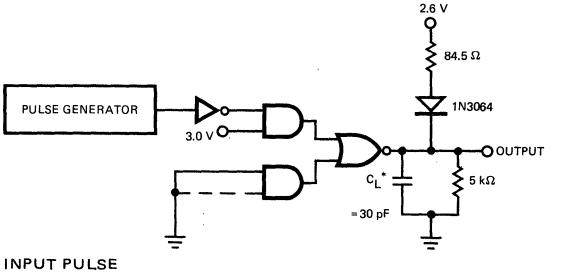
3. The output voltage limits are guaranteed for any appropriate combination of HIGH and LOW inputs specified by the function table for the desired output.
4. Receiver input was at a HIGH level immediately before being reduced to 1.45 V.
5. Receiver input was at a LOW level immediately before being raised to 1.45 V.

AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

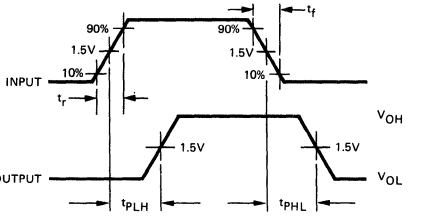
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	See Test Circuit		20	30	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW			20	30	

AC CHARACTERISTICS

TEST CIRCUIT



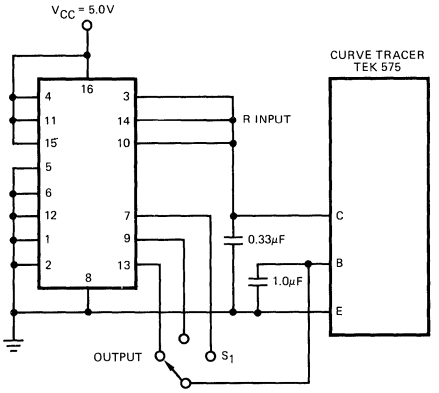
VOLTAGE WAVEFORMS

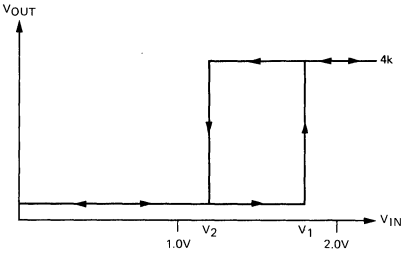


INPUT PULSE
Amplitude = 2.6 V
t_{PW} = 200 ns (50% Duty Cycle)
$t_r = t_f \leqslant 5$ ns (10% and 90% measurement points)

*Includes probe and jig capacitance.

HYSTERESIS TEST CIRCUIT

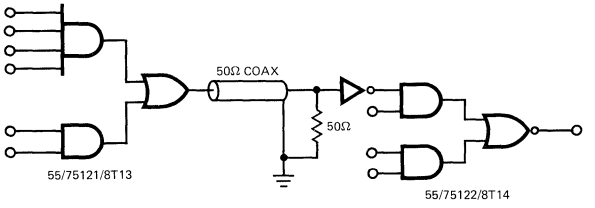


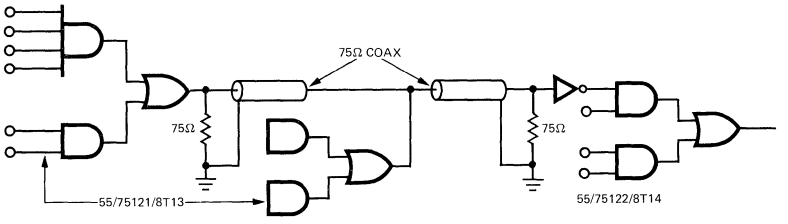


Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Figure 2.

1. V_1 and V_2 must be between 0.8 V minimum and 2.0 V maximum.
2. Hysteresis = $V_1 - V_2 \geq 0.3$ V.

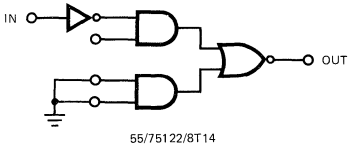
APPLICATIONS

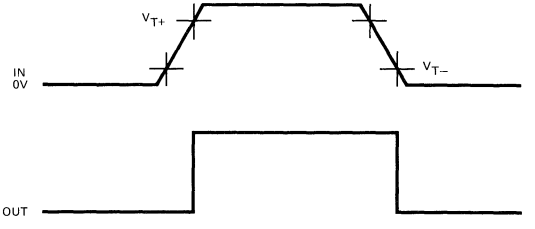




If more than one driver/receiver pair is to be used on each transmission line, the line should be terminated at both ends.

SCHMITT TRIGGER APPLICATION





μA8T24 • 75124

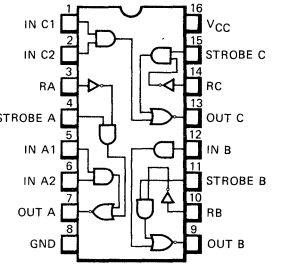
TRIPLE LINE RECEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA8T24/75124 Triple Line Receiver meets IBM System/360 I/O Interface Specifications (File No. S360-19). Logic inputs are fully TTL or DTL compatible. The R (Receive) input is designed to withstand a positive dc input of +7.0 V with power on (V_{CC+} = 5.0 V) and +6.0 V with power off, (V_{CC+} = 0 V) and a negative dc input of 0.15 V with power on or off. This protection allows normal bus operation even if one or more receivers have been powered down.

- **MEETS IBM SYSTEM/360 I/O INTERFACE SPECIFICATION**
- **BUILT-IN INPUT THRESHOLD HYSTERESIS**
- **HIGH SPEED**
- **INDEPENDENT CHANNEL STROBING**
- **FANOUT OF 10 TTL LOADS**
- **SINGLE +5.0 V SUPPLY OPERATION**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ABSOLUTE MAXIMUM RATINGS

Input Voltage (Note 1)	R Input with V_{CC} Applied	7.0 V
	R Input with V_{CC} not Applied	6.0 V
	Logic Inputs	5.5 V
Output Voltage (Note 1)		+7.0 V
Output Current		±100 mA
Supply Voltage (Note 1)		+7.0 V
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range		0°C to +70°C
Pin Temperatures		
Hermetic DIP (Soldering, 60 s)		300°C
Molded DIP (Soldering, 10 s)		260°C
Internal Power Dissipation (Note 2)		800 mW

FUNCTION TABLE

INPUTS				OUTPUT
1	2*	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = HIGH
L = LOW
X = Don't Care

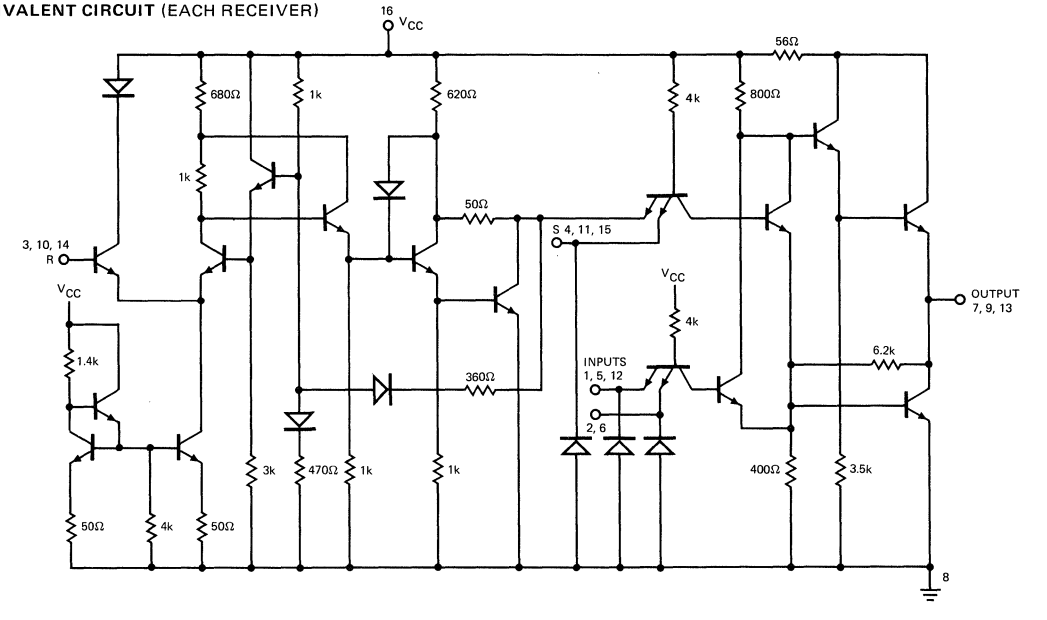
*Input 2 and last two lines of the Function Table are applicable to receivers A and C only.

ORDER INFORMATION

TYPE	PART NO.
μA8T24 or 75124	μA8T24/75124DC
μA8T24 or 75124	μA8T24/75124PC

NOTES:
1. Voltages are with respect to the ground pin (pin 8).
2. Rating applies to ambient temperatures up to 60°C. Above 60°C derate linearly at 8.3 mW/°C.

EQUIVALENT CIRCUIT (EACH RECEIVER)



RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
Output HIGH Current, I_{OH}			−75	mA
Operating Ambient Temperature, T_A	0		70	°C

ELECTRICAL CHARACTERISTICS: V_{CC} = 4.75 to 5.25 V, T_A = 0°C to 70°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage	In 1, 2, or S		2.0			V
		R		1.7			
V_{IL}	Input LOW Voltage	In 1, 2, or S				0.8	V
		R				0.7	
$V_{T+} - V_{T-}$	Hysteresis†	R	V_{CC} = 5.0 V, T_A = 25°C	0.2	0.4		V
V_{IN}	Input Clamp Voltage	In 1, 2, or S	V_{CC} = 5.0 V, I_{IN} = −12 mA			−1.5	V
$V_{(BR)IN}$	Input Breakdown Voltage	In 1, 2, or S	V_{CC} = 5.0 V, I_{IN} = 10 mA	5.5			V
V_{OH}	Output HIGH Voltage		$V_{IH} = V_{IH}$ Min, $V_{IL} = V_{IL}$ Max, I_{OH} = −800 μA, See Note 3	2.6			V
V_{OL}	Output LOW Voltage		$V_{IH} = V_{IH}$ Min, $V_{IL} = V_{IL}$ Max, I_{OL} = 16 mA, See Note 3			0.4	V
I_{IN}	Input Current at Maximum Input Voltage	R	V_{IN} = 7.0 V			5.0	mA
			V_{IN} = 6.0 V, V_{CC} = 0			5.0	
I_{IH}	Input HIGH Current	In 1, 2, or S	V_{IN} = 4.5 V			40	μA
		R	V_{IN} = 3.11 V			170	
I_{IL}	Input LOW Current	In 1, 2, or S	V_{IN} = 0.4 V	−0.1		−1.6	mA
I_{OS}	Short-Circuit Output Current‡		V_{CC} = 5.0 V, T_A = 25°C	−50		−100	mA
I_{CC}	Supply Current		V_{CC} = 5.25 V			72	mA

†Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Hysteresis Test Circuit.

‡Not more than one output should be shorted at a time.

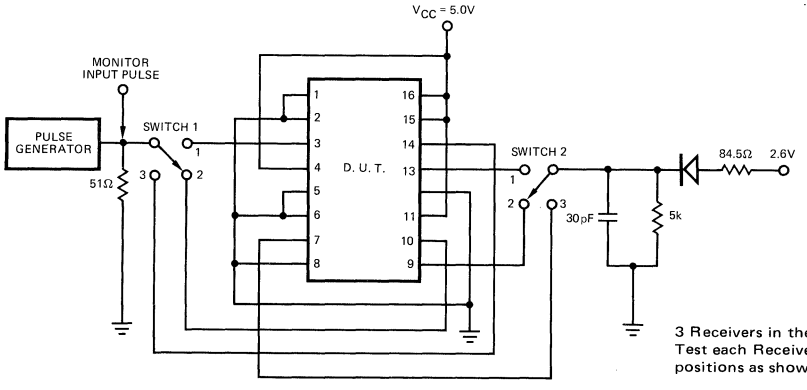
AC CHARACTERISTICS: V_{CC} = 5.0 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH from R Input	See Test Circuit		20	30	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW from R Input			20	30	

3. The output voltage and current limits are guaranteed for any appropriate combination of HIGH and LOW Inputs specified by the Function Table for the desired output.

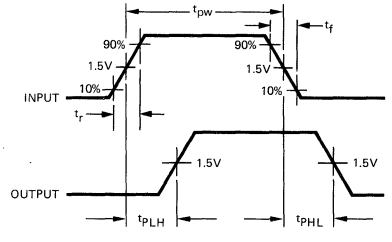
AC CHARACTERISTICS

TEST CIRCUIT



3 Receivers in the package. Test each Receiver using switch positions as shown in Table 1.

WAVEFORMS



INPUT PULSE:
Amplitude = 2.6V
Pulse width = 200ns
(50% Duty Cycle)
$t_r = t_f$ = 5ns (10% to 90%)

TABLE 1		
Receiver no.	Position	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT

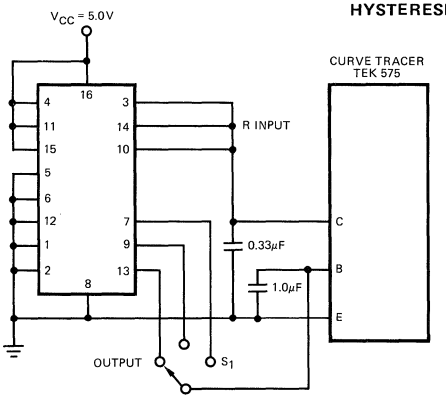
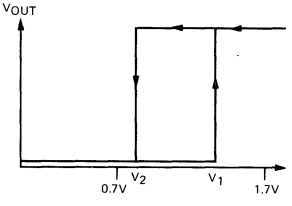


Fig. 1

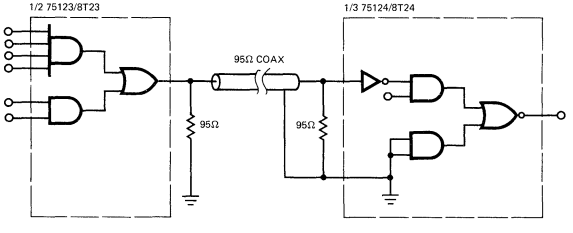


Verify in each of three (3) positions of S_1 (Fig. 1) that the following occurs per Fig. 2.

1. V_1x and V_2 must be between 0.7V minimum and 1.7V maximum.
2. Hysteresis = $V_1 - V_2$

Fig. 2

TYPICAL APPLICATION



55/75107A • 55/75108A
55/75107B • 55/75108B

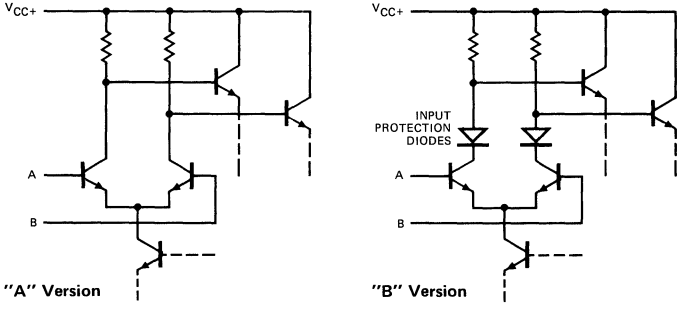
DUAL LINE RECEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

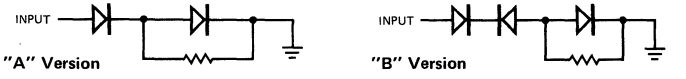
GENERAL DESCRIPTION – The 55/75107A/B and 55/75108A/B are high speed, two-channel Line Receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3V but can be increased to ±15V by the use of input attenuators. Separate or common strobes are available. The 55/75107A/B circuit features an active pull-up (totem pole output). The 55/75108A/B circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the 55109/75109 and 55110/75110 line drivers. The 55/75107A/B and 55/75108A/B line receivers are useful in high speed balanced, unbalanced and party line transmission systems and as data comparators. (See following description of A and B versions.)

- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **HIGH COMMON-MODE REJECTION RATIO**
- **HIGH INPUT IMPEDANCE**
- **HIGH INPUT SENSITIVITY**
- **INPUT COMMON-MODE VOLTAGE RANGE OF ±3 V**
- **SEPARATE OR COMMON STROBES**
- **TTL OR DTL DRIVE CAPABILITY**
- **WIRED-OR OUTPUT CAPABILITY**
- **HIGH DC NOISE MARGINS**
- **STROBE INPUT CLAMP DIODES**
- **55/75107B SERIES DEVICES ARE DIRECT REPLACEMENTS FOR 55/75107A SERIES DEVICES**
- **B VERSION AVAILABLE UPON REQUEST**
- **INPUT IS DIODE PROTECTED AGAINST POWER-OFF LOADING ON B VERSIONS DEVICES**

The essential difference between the 55/75107A and 55/75107B versions is shown in the following schematics of the input stage:

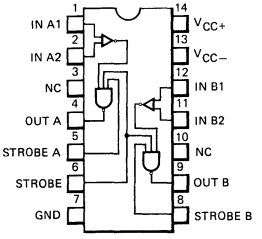


The input protection diodes are useful in certain party-line systems which may have multiple V_{CC+} power supplies and, in which case, may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



This would be a problem in specific systems which might possibly have the transmission lines biased to some potential greater than 1.4 V. Since this is not a widespread application problem, both the A and B versions will be available. The ratings and characteristic specifications of the B versions are the same as those of the A versions. The B versions will be supplied upon request.

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A 3I
PACKAGE CODES D P F

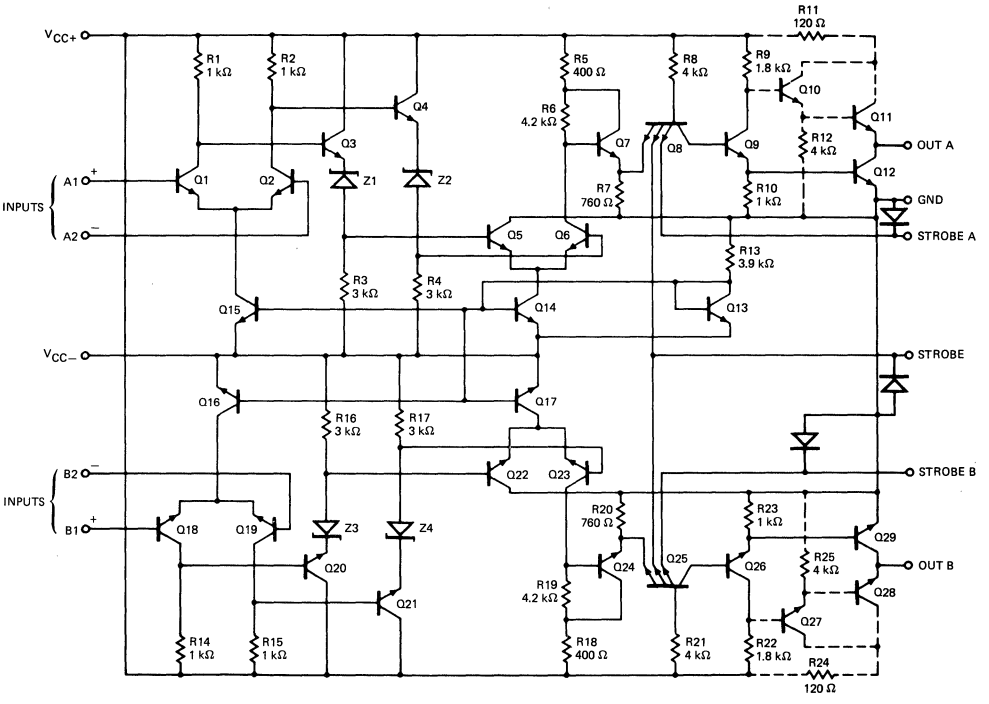


ORDER INFORMATION

TYPE	PART NO.
55107A	55107AFM
55107A	55107ADM
75107A	75107ADC
75107A	75107APC
55108A	55108AFM
55108A	55108ADM
75108A	75108ADC
75108A	75108APC
55107B	55107BFM
55107B	55107BDM
75107B	75107BDC
75107B	75107BPC
55108B	55108BFM
55108B	55108BDM
75108B	75108BDC
75108B	75108BPC

6

EQUIVALENT CIRCUIT



NOTE:
Components shown with dashed lines are applicable to the 55107A/B and 75107A/B only. See preceding description for differences between A and B versions.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	±7 V
Internal Power Dissipation (Note 3)	670 mW
Differential Input Voltage (Note 2)	±6 V
Common Mode Input Voltage (Note 1)	±5 V
Strobe Input Voltage (Note 1)	5.5 V
Operating Temperature Range	
55107A/107B/108A/108B	−55°C to +125°C
75107A/107B/108A/108B	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

Notes on following pages.

ELECTRICAL CHARACTERISTICS 55/75107A, 55/75107B

(Ratings Apply Over Full Ambient Temperature Range With V_{CC+} = Max and V_{CC-} = Max, unless otherwise noted) (Notes 4 & 6)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	Input HIGH Current	V_{DIFF} = 0.5 V, V_{CM} = −3 V to +3 V			30	75	μA
I_{IL}	Input LOW Current	V_{DIFF} = −2 V, V_{CM} = −3 V to +3 V				−10	μA
$I_{IH(G)}$	Gate Input HIGH Current	V_{GATE} = 2.4 V				40	μA
		V_{GATE} = V+				1.0	mA
$I_{IL(G)}$	Gate Input LOW Current	V_{GATE} = 0.4 V				−1.6	mA
$I_{IH(S)}$	Strobe Input HIGH Current	V_{STROBE} = 2.4 V				80	μA
		V_{STROBE} = V+				2.0	mA
$I_{IL(S)}$	Strobe Input LOW Current	V_{STROBE} = 0.4 V				−3.2	mA
V_{OH}	Output HIGH Voltage	I_L = −400 μA, V_{CM} = −3 V to +3 V	V_{CC+} = MIN, V_{CC-} = MIN	2.4			V
V_{OL}	Output LOW Voltage	I_{SINK} = 16 mA, V_{CM} = −3 V to +3 V	V_{CC+} = MIN, V_{CC-} = MIN			0.4	V
I_{SC}	Short-Circuit Output Current	V_{OUT} = 0 (Note 5)		−18		−70	mA
I_{CC+}	Positive Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			18	30	mA
I_{CC-}	Negative Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			−8.4	−15	mA

AC CHARACTERISTICS (V_{CC+} = +5 V, V_{CC-} = −5 V, R_L = 390 Ω, C_L = 50 pF, T_A = 25°C. See Test Circuit)

t_{PLH}(D)	Propagation Delay Time		17	25	ns	
t_{PHL}(D)			17	25	ns	
t_{PLH}(S)			10	15	ns	
t_{PHL}(S)			10	15	ns	

ELECTRICAL CHARACTERISTICS 55/75108A, 55/75108B

(Ratings Apply Over Full Ambient Temperature Range With V_{CC+} = Max and V_{CC-} = Max, unless otherwise noted) (Notes 4 & 6)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	Input HIGH Current	V_{DIFF} = 0.5 V, V_{CM} = −3 V to +3 V			30	75	μA
I_{IL}	Input LOW Current	V_{DIFF} = −2 V, V_{CM} = −3 V to +3 V				−10	μA
$I_{IH(G)}$	Gate Input HIGH Current	V_{GATE} = 2.4 V				40	μA
		V_{GATE} = V+				1.0	mA
$I_{IL(G)}$	Gate Input LOW Current	V_{GATE} = 0.4 V				−1.6	mA
$I_{IH(S)}$	Strobe Input HIGH Current	V_{STROBE} = 2.4 V				80	μA
		V_{STROBE} = V+				2.0	mA
$I_{IL(S)}$	Strobe Input LOW Current	V_{STROBE} = 0.4 V				−3.2	mA
V_{OL}	Output LOW Voltage	I_{SINK} = 16 mA, V_{CM} = −3 V to +3 V	V_{CC+} = MIN, V_{CC-} = MIN			0.4	V
V_{IH}	Output HIGH Current	V_{OUT} = V+	V_{CC+} = MIN, V_{CC-} = MIN			250	μA
I_{CC+}	Positive Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			18	30	mA
I_{CC-}	Negative Supply Current	V_{OUT} = V_{OH}, I_L = 0, T_A = 25°C			−8.4	−15	mA

AC CHARACTERISTICS (V_{CC+} = +5 V, V_{CC-} = −5 V, R_L = 390 Ω, C_L = 15 pF, T_A = 25°C. See Test Circuit)

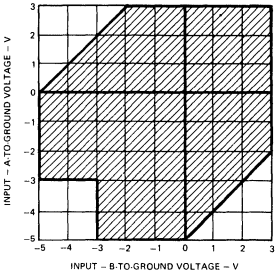
t_{PLH}(D)	Propagation Delay Time		19	25	ns	
t_{PHL}(D)			19	25	ns	
t_{PLH}(S)			13	20	ns	
t_{PHL}(S)			13	20	ns	

6

TRUTH TABLE

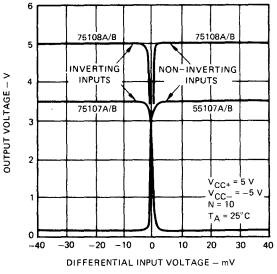
DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

RECOMMENDED COMBINATIONS OF INPUT VOLTAGE FOR LINE RECEIVERS

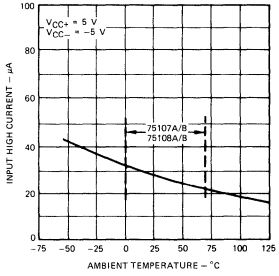


TYPICAL PERFORMANCE CURVES

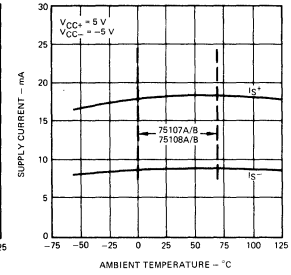
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



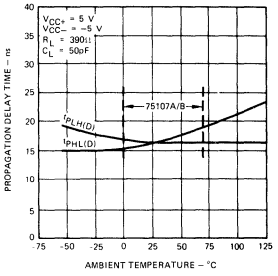
INPUT HIGH CURRENT INTO 1A OR 2A AS A FUNCTION OF AMBIENT TEMPERATURE



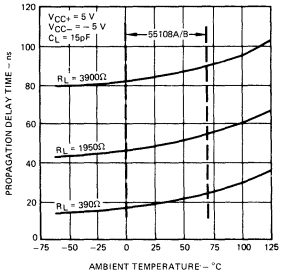
HIGH LOGIC LEVEL SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



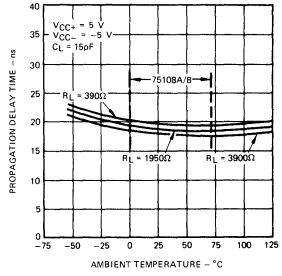
55/75107A, 55/75107B PROPAGATION DELAY TIME (DIFFERENTIAL INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



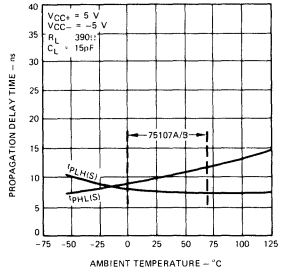
55/75108A, 55/75108B PROPAGATION DELAY TIME LOW-TO-HIGH LEVEL AS A FUNCTION OF AMBIENT TEMPERATURE



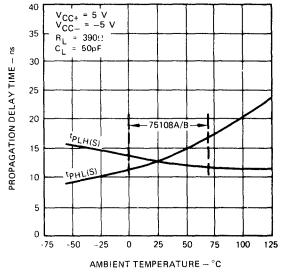
55/75108A, 55/75108B PROPAGATION DELAY TIME HIGH-TO-LOW LEVEL AS A FUNCTION OF AMBIENT TEMPERATURE



55/75107A, 55/75107B PROPAGATION DELAY TIME (STROBE INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



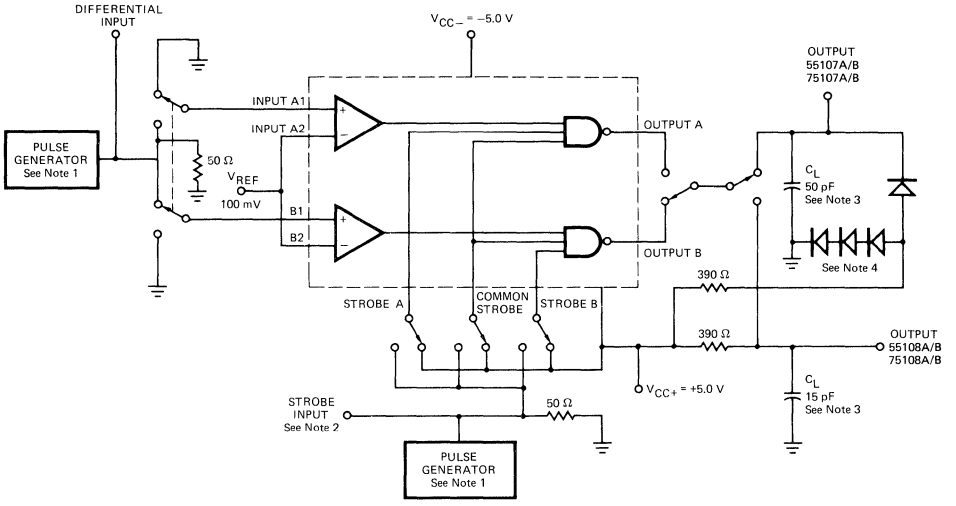
55/75108A, 55/75108B PROPAGATION DELAY TIME (STROBE INPUTS) AS A FUNCTION OF AMBIENT TEMPERATURE



NOTES:
1. These voltages are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (−) terminal.
3. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For Flatpak derate linearly at 7.1 mW/°C above 60°C.
4. For 55107A/B and 55108A/B guaranteed supply voltage range is ±4.5 V to ±5.5 V. Operating temperature range is $-55°C \leq T_A \leq +125°C$. For 75107A/B and 75108A/B guaranteed supply voltage range is ±4.75 V to ±5.25 V. Operating temperature range is $0°C \leq T_A \leq 70°C$.
5. Note more than one (1) output should be shorted at a time.
6. V_{CC-} Max implies V_{CC-} = −5.5 V or −5.25 V, depending on device type.

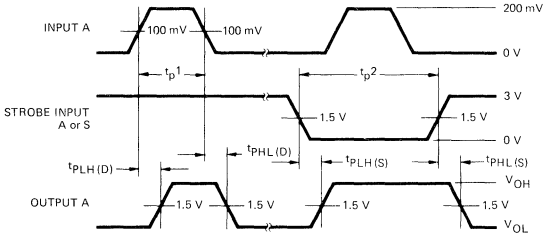
AC CHARACTERISTICS

AC TEST CIRCUIT



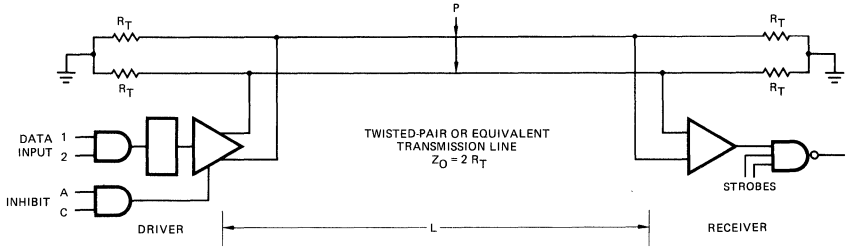
NOTES:
1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 μs, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe A when inputs A1-A2 are being tested: to common Strobe when inputs A1-A2 or B1-B2 are being tested, and to Strobe B when inputs B1-B2 are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

VOLTAGE WAVEFORMS



APPLICATION

BASIC BALANCED-LINE TRANSMISSION SYSTEM



The 55/75107A/B dual line circuits are designed specifically for use in high speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30+1.3L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

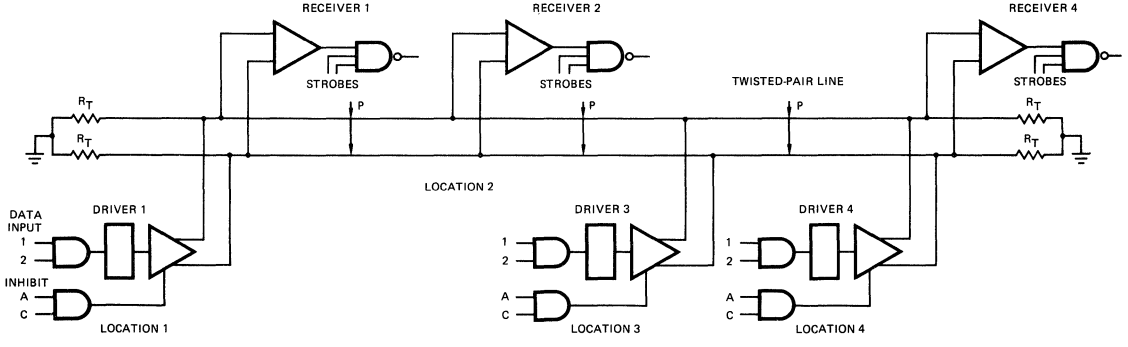
$$V_{DIFF} \simeq 1/2\, I_{OUT(on)} \cdot R_T$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \simeq I_{OUT(on)} \cdot R_T$$

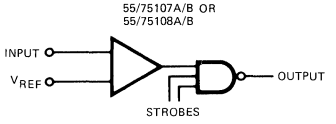
DATA-BUS OR PARTY-LINE SYSTEM



The strobe feature of the receivers and the inhibit feature of the drivers allow the 55/75107A/B dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. The 55/75107A/B device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

APPLICATION (Cont'd)

UNBALANCED OR SINGLE-LINE SYSTEMS



The 55/75107A/B dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.

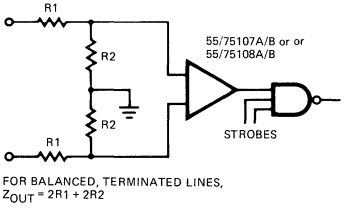
The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3.0 V to +3.0 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

PRECAUTIONS IN THE USE OF 55/75107A/B AND 55/75108A/B DUAL LINE RECEIVERS

The following precaution should be observed when using or testing 55/75107A/B line circuits:

When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0 V and +3.0 V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

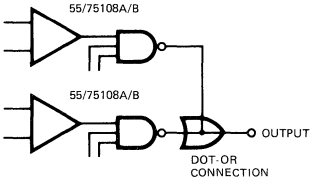
INCREASING COMMON-MODE INPUT VOLTAGE RANGE OF RECEIVER



FOR BALANCED, TERMINATED LINES,
$Z_{OUT} = 2R1 + 2R2$

The 55/75107A/B and 55/75108A/B line receivers feature a common-mode input voltage range of ±3.0 V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common-mode range can be extended by the use of external input attenuators. Common-mode input voltages can in this way be reduced to ±3.0 V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

55108A/75108A DOT-OR OUTPUT CONNECTIONS



The 55/75108A/B line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other 55/75108A/B outputs. This allows a level of logic to be implemented without additional logic delay.

75154

QUAD LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

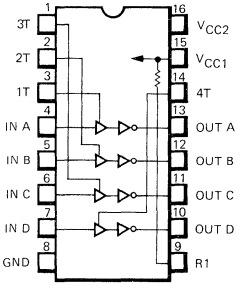
GENERAL DESCRIPTION — The 75154 is a monolithic quadruple line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5 V supply; however, a built-in option allows operation from a 12 V supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

In normal operation, the threshold control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode of operation, if the input voltage goes to zero, the output voltage will remain LOW or HIGH as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go HIGH regardless of the previous input condition.

The 75154 is characterized for operation from 0°C to 70°C.

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P

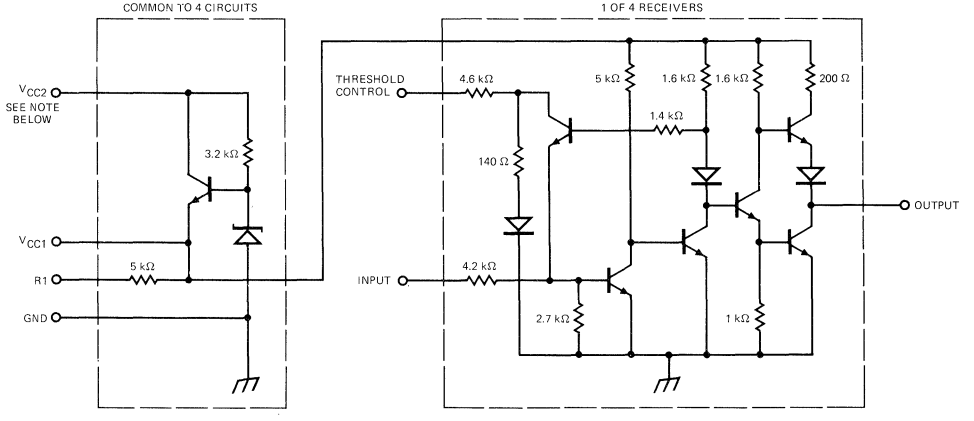


ORDER INFORMATION

TYPE	PART NO.
75154	75154DC
75154	75154PC

- **INPUT RESISTANCE . . . 3 kΩ TO 7 kΩ OVER FULL RS-232C VOLTAGE RANGE**
- **INPUT THRESHOLD ADJUSTABLE TO MEET FAIL-SAFE REQUIREMENTS WITHOUT USING EXTERNAL COMPONENTS**
- **BUILT-IN HYSTERESIS FOR INCREASED NOISE IMMUNITY**
- **INVERTING OUTPUT COMPATIBLE WITH DTL OR TTL**
- **OUTPUT WITH ACTIVE PULL-UP FOR SYMMETRICAL SWITCHING SPEEDS**
- **STANDARD SUPPLY VOLTAGES . . . 5 V OR 12 V**

EQUIVALENT CIRCUIT



Component values shown are nominal ⫛ ...Substrate

NOTE:
When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

ABSOLUTE MAXIMUM RATINGS

Normal Supply Voltage (Pin 15), V_{CC1} (Note 1)	7 V
Alternate Supply Voltage (Pin 16), V_{CC2} (Note 1)	14 V
Input Voltage (Note 1)	±25 V
Continous Total Power Dissipation (Note 2)	800 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Pin Temperatures	
Molded DIP (Soldering, 10 s)	260°C
Hermetic DIP (Soldering, 60 s)	300°C

NOTES:
1. Voltage values are with respect to the network ground terminal.
2. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNITS
Normal Supply Voltage (Pin 15), V_{CC1}	4.5	5	5.5	V
Alternate Supply Voltage (Pin 16), V_{CC2}	10.8	12	13.2	V
Input Voltage			±15	V
Normalized Fan Out from Each Output, N			10	
Operating Temperature, T_A	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMENDED OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	CHARACTERISTICS		TEST FIGURE	TEST CONDITIONS	MIN (Note 3)	TYP†† (Note 3)	MAX (Note 3)	UNITS
V_{IH}	Input HIGH Voltage		1		3.0			V
V_{IL}	Input LOW Voltage		1				−3.0	V
V_{T+}	Positive-Going Threshold Voltage	Normal Operation	1		0.8	2.2	3.0	V
		Fail-Safe Operation			0.8	2.2	3.0	
V_{T-}	Negative-Going Threshold Voltage	Normal Operation	1		−3.0	−1.1	0	V
		Fail-Safe Operation			0.8	1.4	3.0	
$V_{T+}-V_{T-}$	Hysteresis	Normal Operation	1		0.8	3.3	6.0	V
		Fail-Safe Operation			0	0.8	2.2	
V_{OH}	Output HIGH Voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Output LOW Voltage		1	I_{OL} = 16 mA		0.23	0.4	V
R_I	Input Resistance		2	ΔV_I = −25 V to −14 V	3.0	5.0	7.0	kΩ
				ΔV_I = −14 V to −3 V	3.0	5.0	7.0	
				ΔV_I = −3 V to 3 V	3.0	6.0		
				ΔV_I = 3 V to 14 V	3.0	5.0	7.0	
				ΔV_I = 14 V to 25 V	3.0	5.0	7.0	
$V_{I(open)}$	Open-Circuit Input Voltage		3	I_I = 0	0	0.2	2.0	V
I_{OS}	Short-Circuit Output Current†		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply Current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply Current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

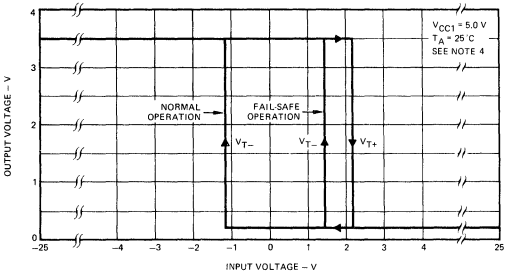
†Not more than one output should be shorted at a time.
‡All typical values are at V_{CC1} = 5 V, T_A = 25°C.
NOTE
3. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3 V is the maximum, the minimum limit is a more-negative voltage.

AC CHARACTERISTICS: V_{CC1}= 5.0 V, T_A= 25°C, N = 10

SYMBOL	CHARACTERISTICS	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Output	6	C_L = 50 pF, R_L = 390 Ω		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Output				20		ns
t_{TLH}	Transition Time, Low-to-High Output				9.0		ns
t_{THL}	Transition Time, High-to-Low Output				6.0		ns

TYPICAL CHARACTERISTICS

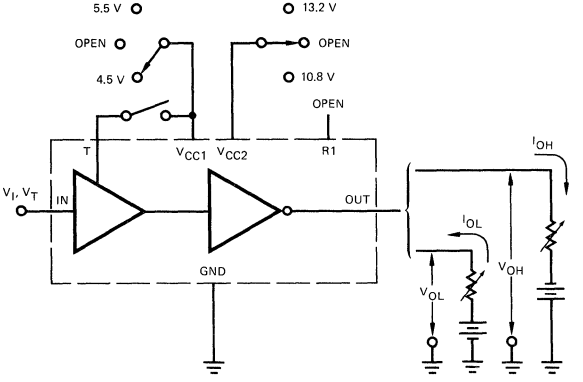
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



NOTE

4. For normal operation, the threshold controls are connected to V_{CC1}, pin 15. For fail-safe operation, the threshold controls are open.

DC TEST CIRCUITS†



NOTES:
A. Momentarily apply −5 V, then 0.8 V.
B. Momentarily apply 5 V, then ground.

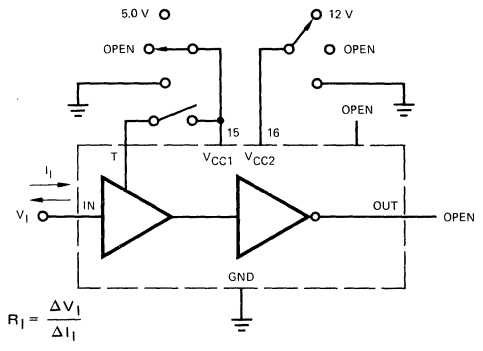
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEST TABLE

TEST	MEASURE	IN	T	OUT	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min, V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note A	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	Pin 15	I_{OH}	T	13.2 V
V_{IL} max, V_{T-} min (normal)	V_{OH}	−3 V	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	−3 V	Pin 15	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max, V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max (normal)	V_{OL}	3 V	Pin 15	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	Pin 15	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note B	Pin 15	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	Pin 15	I_{OL}	T	13.2 V

Fig. 1 V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}.

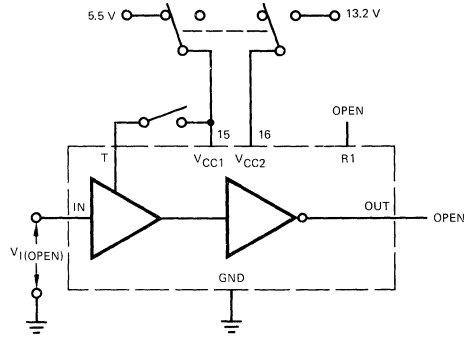
DC TEST CIRCUITS† (Cont'd)



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5 V	Open
Open	GND	Open
Open	Open	Open
Pin 15	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Pin 15	T	12 V
Pin 15	T	GND
Pin 15	T	Open

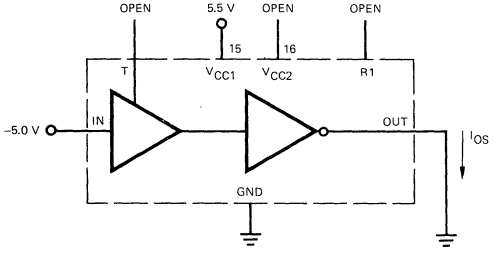
Fig. 2 R_I



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5.5 V	Open
Pin 15	5.5 V	Open
Open	Open	13.2 V
Pin 15	T	13.2 V

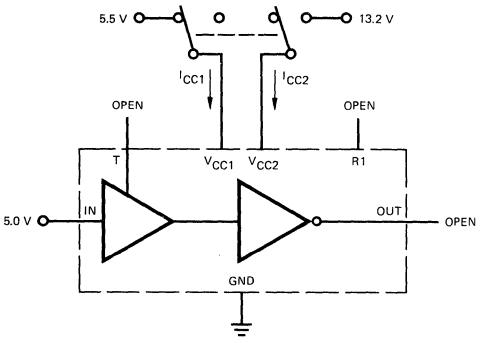
Fig. 3 $V_{I(open)}$



Each output is tested separately.

Fig. 4 I_{OS}

DC TEST CIRCUITS† (Cont'd)



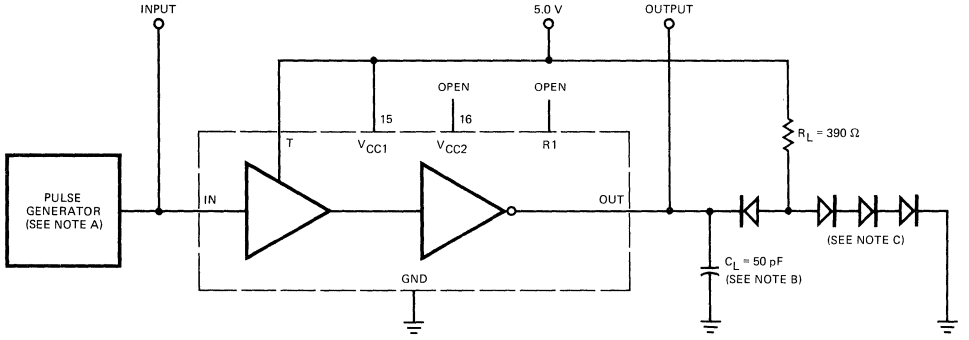
All four line receivers are tested simultaneously.

Fig. 5 I_{CC}

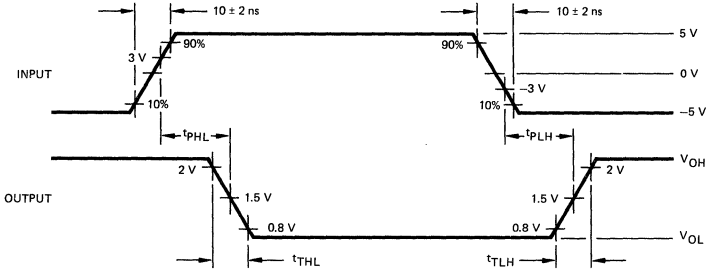
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

AC CHARACTERISTICS

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 200 ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064

9613

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9613 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature range using a single 5.0 V supply. It can receive ± 500 mV of differential data in the presence of high level (± 15 V) common mode voltag es and deliver undistrubed TTL logic to the output.

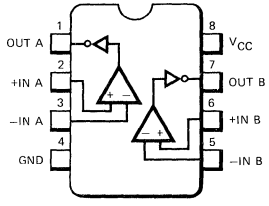
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **SINGLE 5.0 V SUPPLY VOLTAGES**
- **MILITARY TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Supply Voltage (V_{CC} Potential to Ground)	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Pins 2, 3, 5, 6)	±20 V
Differential Input Voltage (+ Input Referred to − Input)	±20 V
Internal Power Dissipation	
Molded DIP, Hermetic DIP (Note 1)	800 mW
Operating Temperature	
9613	−55°C to +125°C
9613C	0°C to +70°C
Storage Temperature	−65°C to +150°C
Pin Temperature	
9613 Hermetic DIP (Soldering, 60 s)	300°C
9613C Molded DIP (Soldering, 10 s)	260°C

NOTES:
1. Rating applies to ambient temperatures up to 30°C. Above 30°C ambient derate linearly at 5.4 mW/°C for Molded DIP and 6.7 mW/°C for Hermetic DIP.

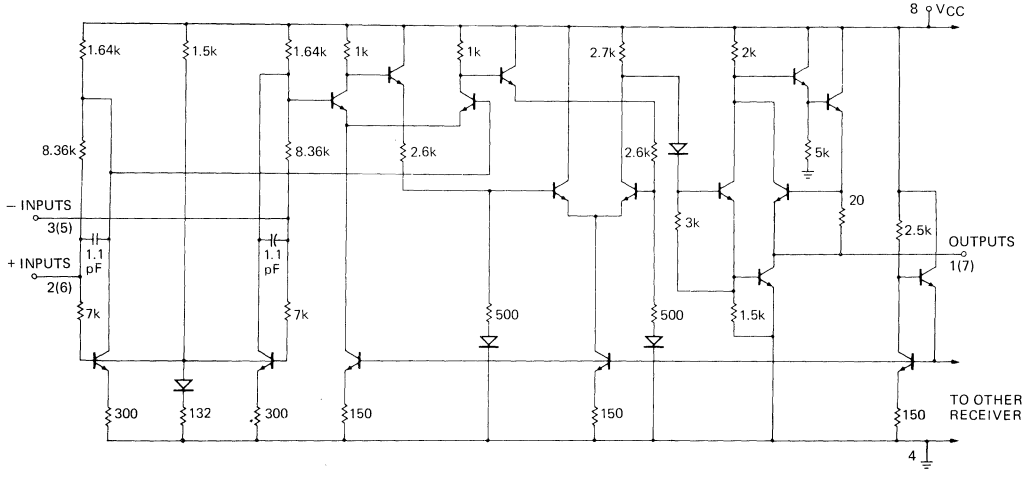
CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



ORDER INFORMATION

TYPE	PART NO.
9613	9613RM
9613C	9613RC
9613C	9613TC

EQUIVALENT CIRCUIT (1/2 9613)



9613

ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V ± 10%, −55°C ≤ T_A ≤ 125°C unless otherwise specified.

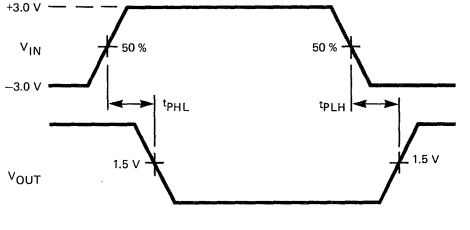
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.28	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4	3.0		V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0 V	−60	−28	−12	mA
R_{IN}	Input Resistance		3.0	4.2		kΩ
V_{CM}	Operating Common Mode Voltage Range	−1.0 V ≤ V_{DIFF} ≤ +1.0 V	−15		+15	V
V_{TH}	Differential Input Threshold Voltage	−5.0 V ≤ V_{CM} ≤ +5.0 V	−0.5		+0.5	V
		−15 V ≤ V_{CM} ≤ +15 V	−1.0		+1.0	V
I_{CC}	Power Supply Current	V_{CC} = 5.25 V		29	50	mA
I_{MAX}	Maximum Supply Current	V_{CC} = 7.0 V		42	70	mA
t_{PLH}	Propagation Delay Time	T_A = 25°C; V_{CC} = 5.0 V; See AC Test Circuit and Waveforms		25	40	ns
t_{PHL}	Propagation Delay Time	T_A = 25°C; V_{CC} = 5.0 V; See AC Test Circuit and Waveforms		23	40	ns

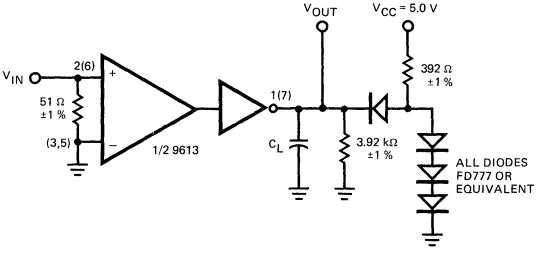
9613C

ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V ± 5%, 0°C ≤ T_A ≤ 70°C unless otherwise specified.

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.28	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −5 mA	2.4	3.0		V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0 V	−60	−28	−12	mA
R_{IN}	Input Resistance		3.0	4.2		kΩ
V_{CM}	Operating Common Mode Voltage Range	−1.0 V ≤ V_{DIFF} ≤ +1.0 V	−15		+15	V
V_{TH}	Differential Input Threshold Voltage	−5.0 V ≤ V_{CM} ≤ +5.0 V	−0.5		+0.5	V
		−15 V ≤ V_{CM} ≤ +15 V	−1.0		+1.0	V
I_{CC}	Power Supply Current	V_{CC} = 5.25 V		29	50	mA
I_{MAX}	Maximum Supply Current	V_{CC} = 7.0 V		42	70	mA
t_{PLH}	Propagation Delay Time	T_A = 25°C; V_{CC} = 5.0 V; See AC Test Circuit and Waveforms		25	40	ns
t_{PHL}	Propagation Delay Time	T_A = 25°C; V_{CC} = 5.0 V; See AC Test Circuit and Waveforms		23	40	ns

AC TEST CIRCUIT AND WAVEFORMS





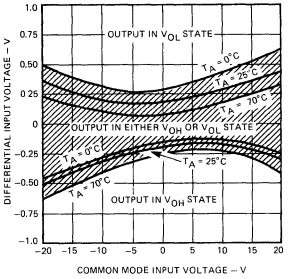
V_{IN}: (PULSE)
Amplitude: 6.0 V
Pulse Width: 100 ns
Duty Cycle: 50 %
$t_r = t_f \leq 5$ ns

C_L = 30 pF ±5 % Including jig capacitance.

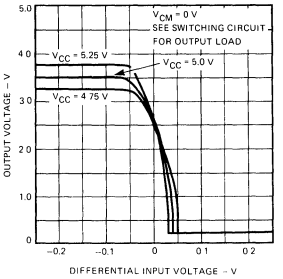
TYPICAL ELECTRICAL CHARACTERISTICS CURVES

9613

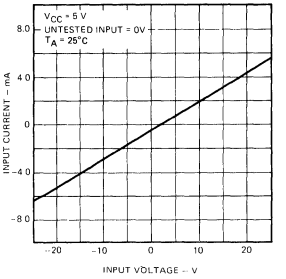
INPUT DIFFERENTIAL THRESHOLD AMBIGUITY AS A FUNCTION OF COMMON MODE INPUT VOLTAGE



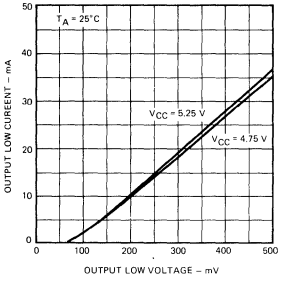
INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF POWER SUPPLY VOLTAGE



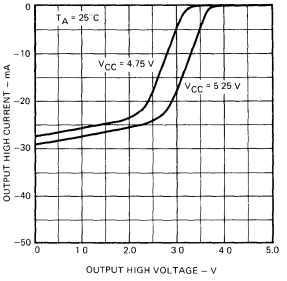
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



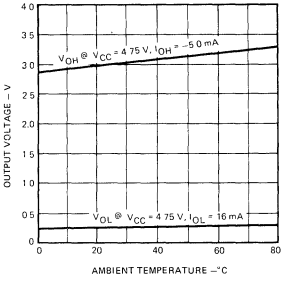
OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



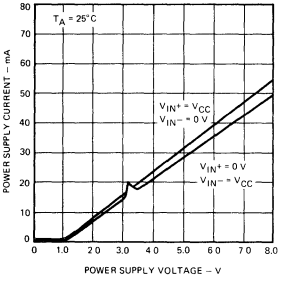
OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



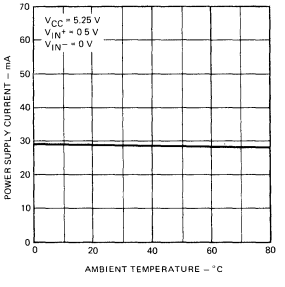
OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



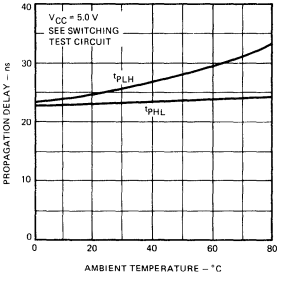
POWER SUPPLY CURRENT AS A FUNCTION OF POWER SUPPLY VOLTAGE



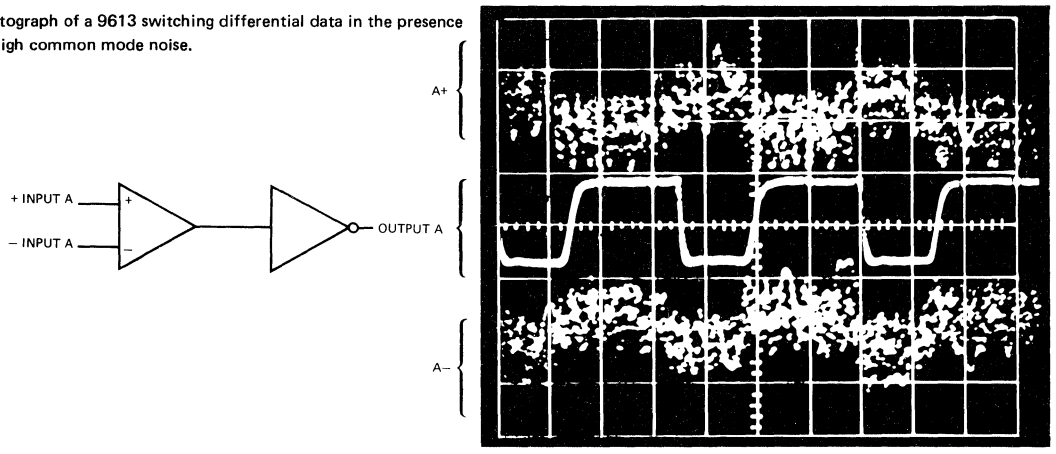
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



PROPAGATION DELAY AS A FUNCTION OF AMBIENT TEMPERATURE



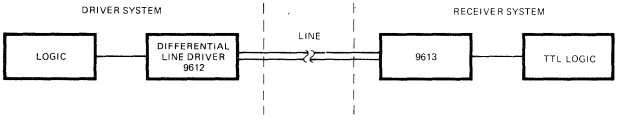
Photograph of a 9613 switching differential data in the presence of high common mode noise.



VERTICAL = 2.0 V DIV. HORIZONTAL = 50 ns/DIV.

Fig. 1

STANDARD USAGE



For example of operation see 9612 data sheet application section.

Fig. 2

9615

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9615 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 V supply. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe and a 130 Ω terminating resistor are provided at the inputs. The output has an uncommitted collector with an active pull up available on an adjacent pin to allow either wire-OR or active pull up TTL output configuration.

- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **CHOICE OF AN UNCOMMITTED COLLECTOR OR ACTIVE PULL UP**
- **STROBE**
- **FULL MILITARY TEMPERATURE RANGE**
- **SINGLE 5 V SUPPLY VOLTAGES**
- **FREQUENCY RESPONSE CONTROL**
- **130 Ω TERMINATING RESISTOR**

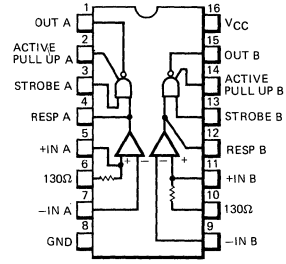
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Pins 5, 6, 7, 9, 10, 11)	±20 V
Voltage Applied to Outputs for HIGH output State without Active Pull Up	−0.5 V to +13.2 V
Voltage Applied to Strobe	−0.5 V to +5.5 V
Pin Temperature Range	
Hermetic DIP, Flatpak (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Internal Power Dissipation (Note 1)	
Operating Temperature Range	670 mW
Military (9615)	−55°C to +125°C
Commercial (9615C)	0°C to +70°C

NOTE:

1. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For the Flatpak, derate linearly at 7.1 mW/°C above 60°C.

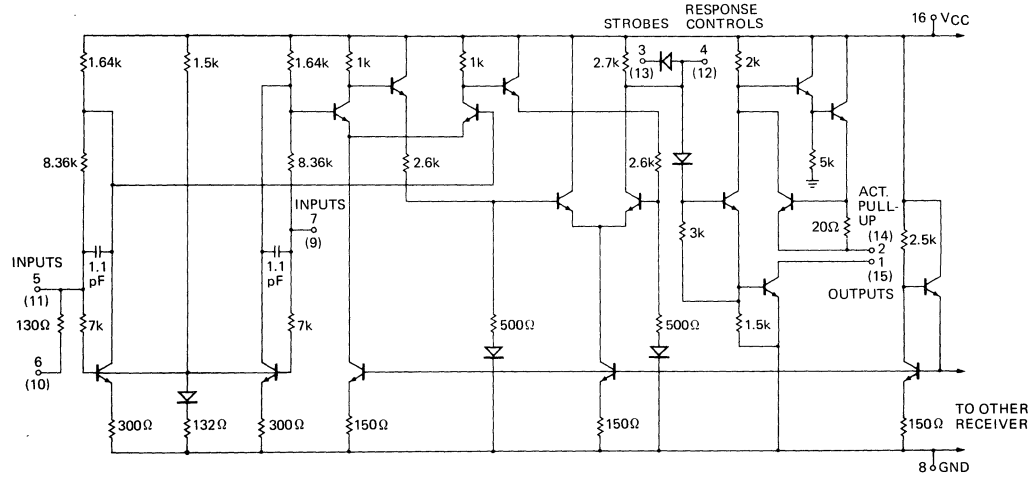
CONNECTION DIAGRAM
16-PIN
(TOP VIEW)
PACKAGE OUTLINES 6B 9B 4L
PACKAGE CODES D P F



ORDER INFORMATION

TYPE	PART NO.
9615	9615DM
9615	9615FM
9615C	9615DC
9615C	9615PC

EQUIVALENT CIRCUIT (1/2 9615)



ELECTRICAL CHARACTERISTICS: V_{CC}= 5.0V ±10%

SYMBOL	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS
		−55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}	Output LOW Voltage		0.40		0.18	0.40		0.40	V	V_{CC} = 4.5 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output HIGH Voltage	2.2		2.4	3.2		2.4		V	V_{CC} = 4.5 V, V_{OUT} = ** I_{OH} = −5.0 mA, *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 12 V, *V_{DIFF} = V_{CC} = 4.5 V
I_{SC}	Output Shorted Current			−15	−39	−80			mA	V_{CC} = 5.5 V, **V_{SC} = 0 V, *V_{DIFF} = −0.5 V
I_{IN}	Input Current		−0.9		−0.49	−0.7		−0.7	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V Other Input = 5.5 V
$I_{IN(ST)}$	Strobe Input Current				−1.15	−2.4			mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			−1.2	−3.4				mA	V_{CC} = 5.5 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	−15	+15	−15	±17.5	+15	−15	+15	V	V_{CC} = 5.0 V, *V_{DIFF} = +1.0V
$I_{R(ST)}$	Strobe Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V, *V_{DIFF} = −0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			77	130	167			Ω	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = GND
V_{TH}***	Differential Input	−500	500	-500	80	500	-500	500	mV	V_{CM} = 0 ; V_{CC} = 5.0V ±10%
	Threshold Voltage	−1.0	1.0	−1.0			−1.0	1.0	V	−15 ≤ V_{CM} ≤ +15V ; V_{CC} = 5.0V ±10%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.5 V, −Inputs = 0 V, +Inputs = 0.5 V
t_{PLH}	Turn-Off Time				30	50			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 1
t_{PHL}	Turn-On Time				30	50			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 1

*V_{DIFF} is a differential input voltage referred from "+IN A" to "−IN A" and from "+IN B" to "−IN B".
**Connect Output "A" to Active Pull up "A" and Output "B" to Active Pull up "B".
***See input-output transfer characteristic graphs on following pages.

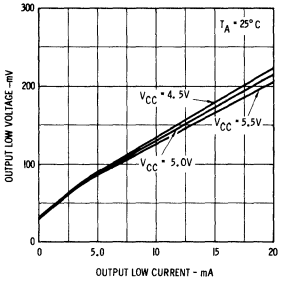
ELECTRICAL CHARACTERISTICS: V_{CC}= 5.0V ±5%

SYMBOL	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS
		0°C		+25°C			+70°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}	Output LOW Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4		V	V_{CC} = 4.75 V, V_{OUT} = ** I_{OH} = –5.0 mA, *V_{DIFF} = –0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 5.25 V, *V_{DIFF} = V_{CC} = 4.75 V
I_{SC}	Output Shorted Current			–14		–100			mA	V_{CC} = 5.25 V, **V_{SC} = 0 V, *V_{DIFF} = –0.5 V
I_{IN}	Input Current		–0.9		–0.49	–0.7		–0.7	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V Other Input = 5.25 V
$I_{IN(ST)}$	Strobe Input Current				–1.15	–2.4			mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			–1.2	–3.4				mA	V_{CC} = 5.25 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	–15	+15	–15	±17.5	+15	–15	+15	V	V_{CC} = 5.0 V, *V_{DIFF} = 1.0V
$I_{R(ST)}$	Strobe Input Leakage Current					5.0		10	μA	V_{CC} = 4.75 V, *V_{DIFF} = –0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			74	130	179			Ω	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = GND
V_{TH} ***	Differential Input	–500	500	–500	–80	500	–500	500	mV	V_{CM} = 0V; V_{CC} = 5.0V ± 5%
	Threshold Voltage	–1.0	1.0	–1.0		1.0	–1.0	1.0	V	-15 ≤ V_{CM} ≤ +15V; V_{CC} = 5.0V ± 5%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.25 V, +Inputs = 0.5 V, –Inputs = 0 V
t_{PLH}	Turn-Off Time				30	75			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 1
t_{PHL}	Turn-On Time				30	75			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 1

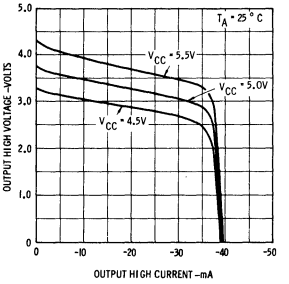
*V_{DIFF} is a differential input voltage referred from "+IN A" to "–IN A" and from "+IN B" to "–IN B".
**Connect Output "A" to Active Pull up "A" and Output "B" to Active Pull up "B".
*** See input-output transfer characteristic graphs on following pages.

TYPICAL ELECTRICAL CHARACTERISTICS FOR 9615 AND 9615C

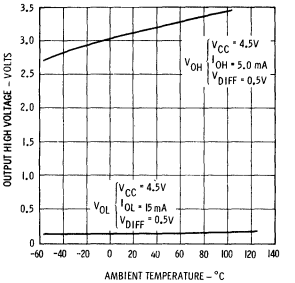
OUTPUT LOW VOLTAGE AS A FUNCTION OF OUTPUT LOW CURRENT



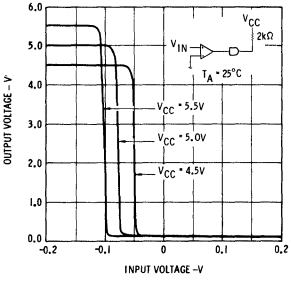
OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



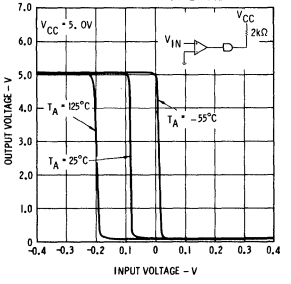
OUTPUT HIGH VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



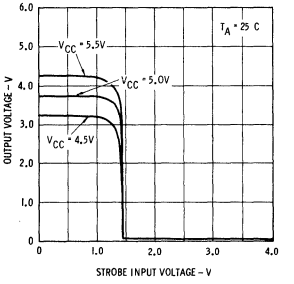
INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF V_{CC}



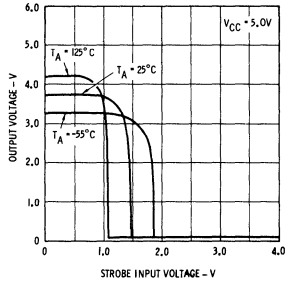
INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF TEMPERATURE



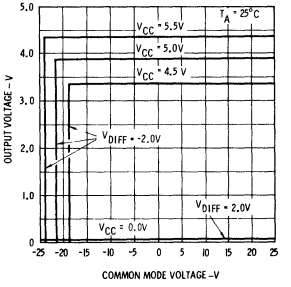
STROBE INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF V_{CC}



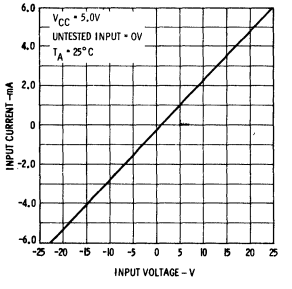
STROBE INPUT/OUTPUT TRANSFER CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE



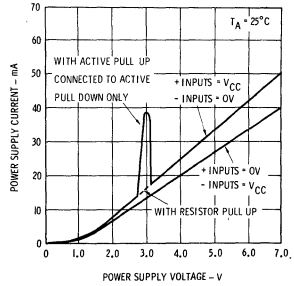
OUTPUT VOLTAGE AS A FUNCTION OF COMMON MODE VOLTAGE



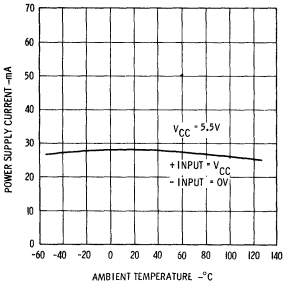
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



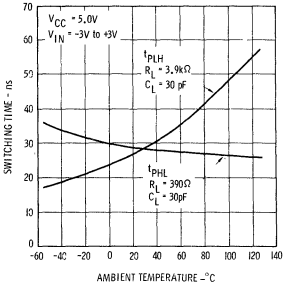
POWER SUPPLY CURRENT AS A FUNCTION OF POWER SUPPLY VOLTAGE



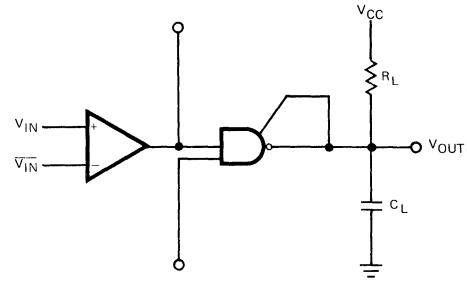
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT



WAVEFORMS

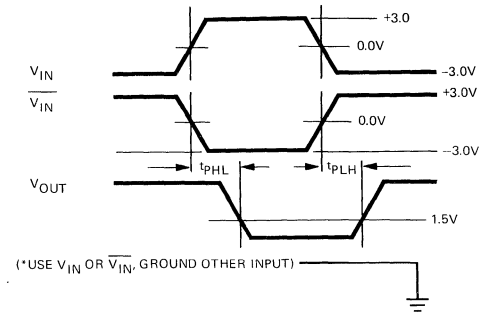
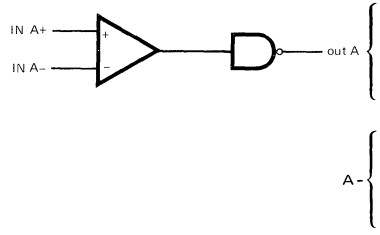
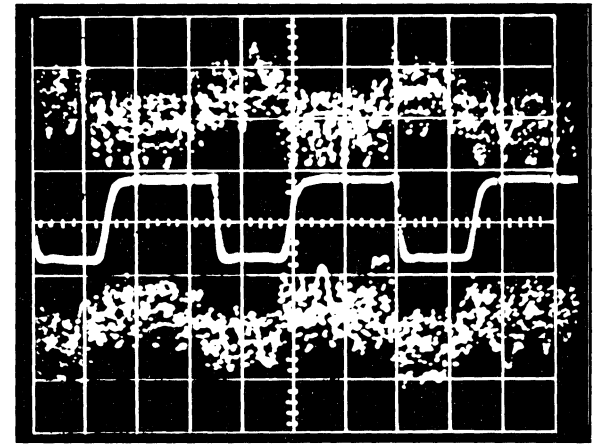


Fig. 1

Photograph of a 9615 switching differential data in the presence of high common mode noise.

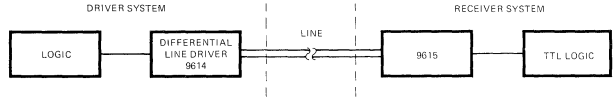




VERTICAL = 2.0 V DIV. HORIZONTAL = 50 ns/DIV.

Fig. 2

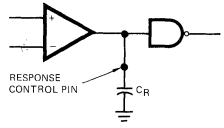
STANDARD USAGE



For example of operation see 9614 data sheet application section.

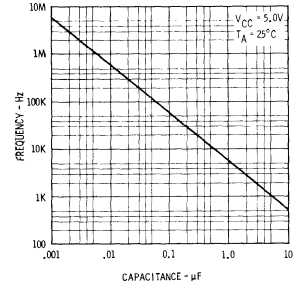
Fig. 3

FREQUENCY RESPONSE CONTROL



Note: 1. C_R>.01 μF may cause slowing of rise and fall times of the output.
2. Due to the mechanism of induction of differential noise, the use of the responce control is not normaly needed.

FREQUENCY RESPONSE AS A FUNCTION OF CAPACITANCE



6

9617

TRIPLE EIA RS-232-C LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

- FOR NEW DESIGNS, THE μA1489/1489A, 75154 OR THE 9637A ARE RECOMMENDED.

GENERAL DESCRIPTION – The 9617 is a monolithic Triple Line Receiver constructed using the Fairchild Planar* process. It is designed to meet the terminator electrical requirements of EIA RS-232-C and CCITT V.24. It receives line signals produced by the 9616, an EIA/CCITT driver, and converts them to TTL compatible logic levels. The inputs have a resistance between 3 kΩ and 7 kΩ and can withstand ±25 V. Each receiver can operate in either hysteresis or non-hysteresis (slicing) modes, and each receiver provides fail-safe operation as defined by Section 2.5 of RS-232-C. Noise immunity may be increased by connecting a capacitor between the response control pin and ground.

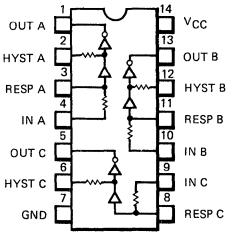
For the hysteresis mode connect the RESP pin to the HYST pin, for the slicing mode leave these pins open.

- **MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS**
- **FAIL-SAFE OPERATION**
- **HYSTERESIS OR NON-HYSTERESIS MODE**
- **INDIVIDUAL RESPONSE CONTROLS**
- **TTL COMPATIBLE OUTPUT**
- **SINGLE +5 V SUPPLY**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 V
Input Voltage	±25 V
Output Current	25 mA
Internal Power Dissipation	630 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

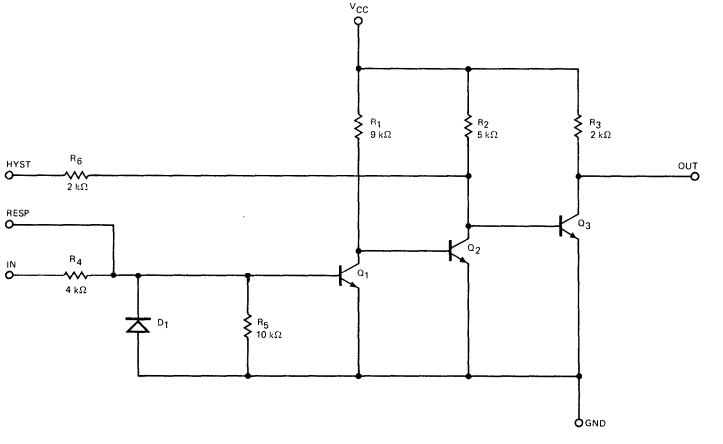
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
9617C	9617DC
9617C	9617PC

EQUIVALENT CIRCUIT (One of three identical circuits)



*Planar is a patented Fairchild process.

9617C

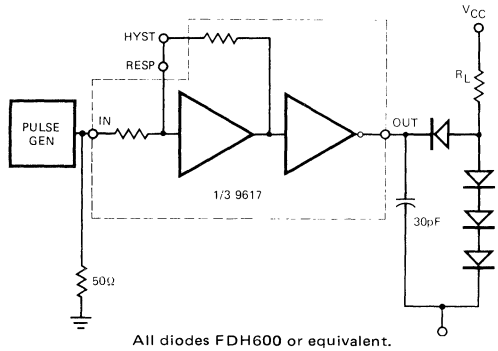
ELECTRICAL CHARACTERISTICS: V_{CC} = +5.0 V ± 5%, T_A = 25°C Response Pin Open, unless otherwise specified.

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	V_I = ±25V	3.0	4.0	7.0	kΩ
E_L	Input Voltage	Open Circuit		0.2	2.0	V
V_{TH+}	Upper Input Threshold Voltage	RESP – HYST Connected	1.75	2.0	2.25	V
V_{TH-}	Lower Input Threshold Voltage	RESP – HYST Connected	0.75	0.85	1.25	V
V_{THX}	Open Loop Threshold Voltage		0.4	1.0	1.2	V
V_{OH}	Output HIGH Voltage	V_{IN} = –3.0V, 0V or open circuit V_{CC} = 4.5V, I_L = –200μA	2.4	3.0		V
V_{OL}	Output LOW Voltage	V_{IN} = +3.0V V_{CC} = 4.5V, I_L = 8.0mA		0.3	0.4	V
I_{SC}	Output Short Circuit Current	V_O = 0V		2.5		mA
I_{CC}	Supply Current	V_{CC} = +5.5V, V_{IN} = 5.0V		12		mA
t_{PLH}	Propagation Delay Time	R_L = 3.9kΩ , Note 1		60		ns
t_r	Rise Time	R_L = 3.9kΩ , Note 1		150		ns
t_{PHL}	Propagation Delay Time	R_L = 390Ω , Note 1		40		ns
t_f	Fall Time	R_L = 390Ω , Note 1		50		ns

Note 1. V_{CC} = 5.0 V, See AC Test Circuit and waveforms

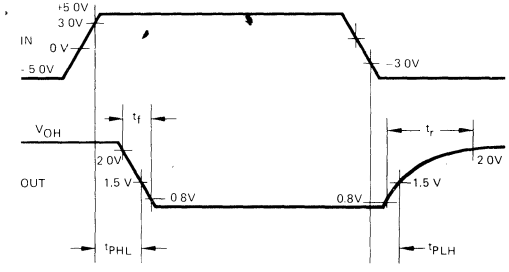
6

AC TEST CIRCUIT



All diodes FDH600 or equivalent.

VOLTAGE WAVEFORMS



Input Pulse Characteristics:

PRR = 1 MHz
PW = 500 ns
$t_r = t_f$ = 10 ± 2 ns (10% to 90%)

NOTE: Wiring capacitance should be minimized between outputs, hysteresis and response pins.

9622
DUAL LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9622 is a Dual Line Receiver designed to discriminate a worst case logic swing of 2.0V from a ±10V common mode noise signal or ground shift. A 1.5V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only ±5% (75 mV) over the military and industrial temperature ranges.

The 9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S_3 (Note 1). A 130Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for eachl line receiver. The output is TTL compatible. The output HIGH level can be increased to +12V by tying it to a positive supply through a resistor. The output circuits allow wired-OR operation.

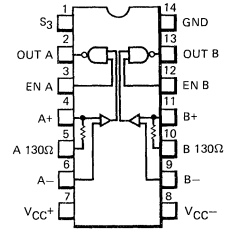
- **TTL COMPATIBLE THRESHOLD VOLTAGE**
- **INPUT TERMINATING RESISTORS**
- **CHOICE OF OUTPUT STATE WITH INPUTS OPEN**
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE**
- **WIRE-OR CAPABILITY**
- **ENABLE INPUTS**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Operating Temperature	
Military (9622)	−55°C to +125°C
Commercial (9622C)	0°C to +70°C
Internal Power Dissipation (Note 2)	
Hermetic DIP, Molded DIP	670mW
V_{CC}+ Pin Potential to Ground Pin	−0.5V to +7V
Input Voltage	±15V
Voltage Applied to Outputs for Output HIGH State	−0.5V to +13.2V
V_{CC}− Pin Potential to Ground Pin	−0.5V to −12V
Enable Pin Potential to Ground Pin	−0.5V to +15V
Pin Temperature	
Hermetic DIP, (Soldering, 60 s)	300°C
Molded DIP, (Soldering, 10 s)	260°C

NOTE
1. S_3 connected to V_{CC}−open inputs causes output to be HIGH.
   S_3 connected to Ground−open inputs causes output to be LOW.
2. Rating applies to ambient temperature up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Hermetic DIP.

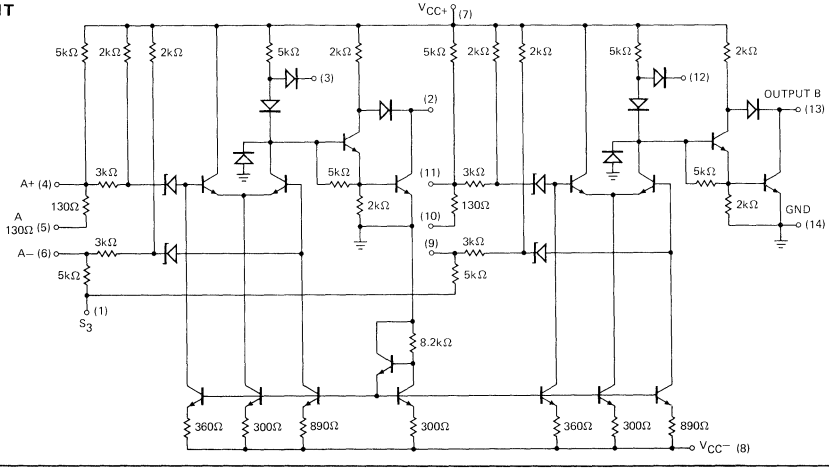
CONNECTION DIAGRAMS
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
9622	9622DM
9622C	9622DC
9622C	9622PC

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V ± 10%, V_{CC-} = −10 V ± 10%.

SYMBOL	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS
		−55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OL}	Output LOW Voltage		0.40		0.17	0.40		0.40	Volts	V_{CC+} = 4.5 V V_{CC-} = −11 V *V_{DIFF} = 2.0 V I_{OL} = 12.4 mA
V_{OH}	Output HIGH Voltage	2.8		3.0	3.3		2.9		Volts	V_{CC+} = 4.5 V V_{CC-} = −9.0 V *V_{DIFF} = 1.0 V I_{OH} = −0.2 mA
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CC+} = 4.5 V V_{CC-} = −11 V *V_{DIFF} = 1.0 V V_{CEX} = 12 V
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.1	−1.3	−3.1	mA	V_{CC+} = 5.0 V V_{CC-} = −10 V *V_{DIFF} = 1.0 V V_{SC} = 0 V
I_{R} (ENABLE)	Enable Input Leakage Current					2.0		5.0	μA	V_{CC+} = 4.5 V V_{CC-} = −11 V S_3 = 4.5 V V_R = 4.0 V
I_{F} (ENABLE)	Enable Input Forward Current		−1.5		−0.96	−1.5		−1.5	mA	V_{CC+} = 5.5 V V_{CC-} = −9.0 V S_3 = 0 V V_F = 0 V
I_{F} (+Input)	+Input Forward Current		−2.3		−1.67	−2.1		−2.0	mA	V_{CC+} = 5.0 V V_{CC-} = −10 V −Input = GND V_F = 0 V
I_{F} (−Input)	−Input Forward Current		−2.6		−1.87	−2.4		−2.3	mA	V_{CC+}, S_3 = 5.0 V V_{CC-} = −10 V +Input = GND V_F = 0 V
V_{IL} (ENABLE)	Input LOW Voltage		1.3		1.4	1.0		0.7	Volts	V_{CC+} = 5.0 V ±10 % V_{CC-} = −10 V ± 10 %
V_{TH}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	Volts	V_{CC+} = 5.0 V ±10 % V_{CC-} = −10 V ±10 %
V_{CM}	Common Mode Voltage			−10	±12	+10			Volts	V_{CC+} = 5.0 V V_{CC-} = −10 V *V_{DIFF} = 1.0 V or 2.0 V
$R_{130\Omega}$	Terminating Resistance			100	130	175			Ω	
I_{CC}	5 V Supply Current				13.7	22.9			mA	V_{CC+} = 5.5 V V_{CC-} = −11 V S_3, +Inputs = 5.5 V, −Inputs = 0 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	V_{CC+} = 5.5 V V_{CC-} = −11 V S_3, +Inputs = 5.5 V, −Inputs = 0 V
t_{PLH}	Turn-Off Time				38	50			ns	V_{CC+} = 5.0 V V_{CC-} = −10 V V_{IN} 0→3 V, R_L = 3.9 kΩ, C_L = 30 pF See AC Test Circuit
t_{PHL}	Turn-On Time				35	50			ns	V_{CC+} = 5.0 V V_{CC-} = −10 V V_{IN} 0→3.0 V, R_L = 0.39 kΩ, C_L = 30 pF See AC Test Circuit

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

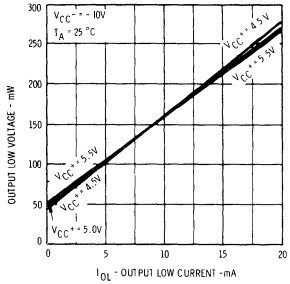
ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V ± 5%, V_{CC-} = −10 V ± 5%.

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	70°C MIN.	70°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OL}	Output LOW Voltage		0.45		0.17	0.45		0.45	Volts	V_{CC+} = 4.75 V V_{CC-} = −10.5 V *V_{DIFF} = 2.0 V I_{OL} = 14.1 mA
V_{OH}	Output HIGH Voltage	2.9		3.0	3.3		2.9		Volts	V_{CC+} = 4.75 V V_{CC-} = −9.5 V *V_{DIFF} = 1.0 V I_{OH} = −0.2 mA
I_{CEX}	Output Leakage Current		80			100		200	μA	V_{CC+} = 4.75 V V_{CC-} = −10.5 V *V_{DIFF} = 1.0 V V_{CEX} = 5.25 V
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.2	−1.3	−3.1	mA	V_{CC+} = 5.0 V V_{CC-} = −10 V *V_{DIFF} = 1.0 V V_{SC} = 0 V
$I_{R\,(ENABLE)}$	Enable Input Leakage Current					5		10	μA	V_{CC+} = 4.75 V V_{CC-} = −10.5 V S_3 = 4.75 V V_R = 4.0 V
$I_{F\,(ENABLE)}$	Enable Input Forward Current		−1.5		−.96	−1.5		−1.5	mA	V_{CC+} = 5.25 V V_{CC-} = −9.5 V S_3 = 0 V V_F = 0 V
$I_{F\,(+Input)}$	+Input Forward Current		−2.6		−1.67	−2.4		−2.3	mA	V_{CC+} = 5.0 V V_{CC-} = −10 V −Input = GND V_F = 0 V
$I_{F\,(-Input)}$	−Input Forward Current		−2.9		−1.87	−2.7		−2.6	mA	V_{CC+}, S_3 = 5.0 V V_{CC-} = −10 V +Input = GND V_F = 0 V
$V_{IL\,(ENABLE)}$	Input LOW Voltage		1.2		1.4	1.0		0.85	Volts	V_{CC+} = 5.0 V ±5 % V_{CC-} = −10 V ±5 %
V_{TH}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	Volts	V_{CC+} = 5.0 V ±5 % V_{CC-} = −10 V ±5 %
V_{CM}	Common Mode Voltage			−7.5	±12	+7.5			Volts	V_{CC+} = 5.0 V V_{CC-} = −10 V *V_{DIFF} = 1.0 V or 2.0 V
$R_{130\Omega}$	Terminating Resistance			91	130	185			Ω	
I_{CC}	5 V Supply Current				13.7	22.9			mA	V_{CC+} = 5.25 V V_{CC-} = −10.5 V S_3, +Inputs = 5.25 V, −Inputs = 0 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	V_{CC+} = 5.25 V V_{CC-} = −10.5 V S_3, +Inputs = 5.25 V, −Inputs = 0 V
t_{PLH}	Turn-Off Time				38	100			ns	V_{CC+} = 5.0 V V_{CC-} = −10 V V_{IN} 0→3.9 V, R_L = 3.9 kΩ, C_L = 30 pF See AC Test Circuit
t_{PHL}	Turn-On Time				35	100			ns	V_{CC+} = 5.0 V V_{CC-} = −10 V V_{IN} 0→3.0 V, R_L = 0.39 kΩ, C_L = 30 pF See AC Test Circuit

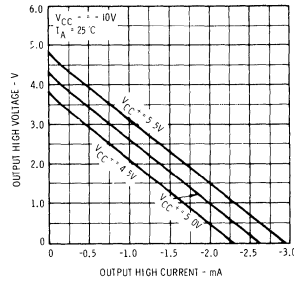
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

TYPICAL PERFORMANCE CURVES FOR 9622 AND 9622C

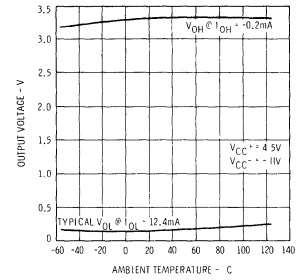
OUTPUT LOW VOLTAGE AS A FUNCTION OF OUTPUT LOW CURRENT



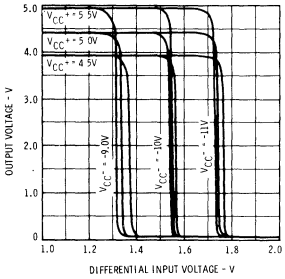
OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



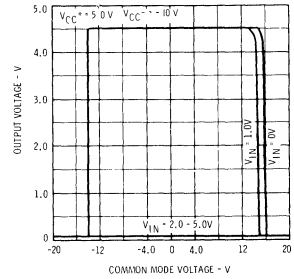
LOGIC LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



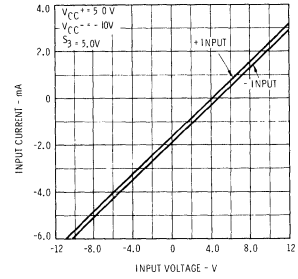
$V_{OUT} - V_{DIFF}$ TRANSFER CHARACTERISTICS



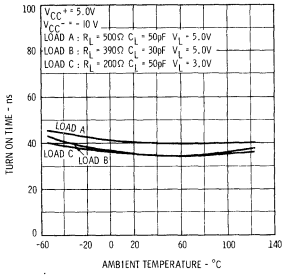
OUTPUT VOLTAGE AS A FUNCTION OF COMMON MODE VOLTAGE



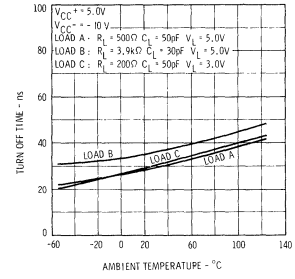
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



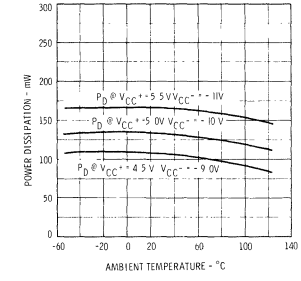
TURN ON TIME AS A FUNCTION OF AMBIENT TEMPERATURE



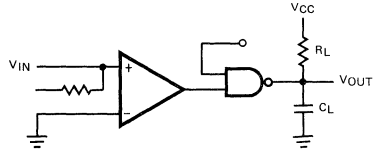
TURN OFF TIME AS A FUNCTION OF AMBIENT TEMPERATURE



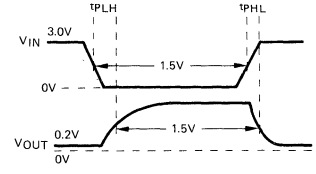
POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



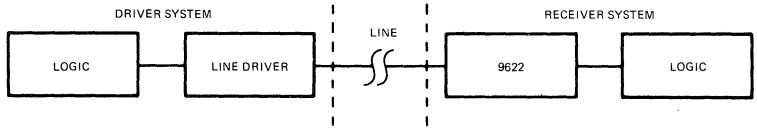
AC TEST CIRCUIT



WAVEFORMS



STANDARD USAGE



9627

DUAL EIA RS-232-C/MIL-STD-188C LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The 9627 is a Dual Line Receiver which meets the electrical interface specifications of EIA RS-232-C and MIL-STD-188C. The input circuitry accomodates ±25V input signals and the differential inputs allow user selection of either inverting or non-inverting logic for the receiver operation. The 9627 provides both a selectable hysteresis range and selectable receiver input resistance. When pin 1 is tied to V_{EE}, the switching points are at +2.6V and −2.6V, thus meeting RS-232-C requirements. When pin 1 is open, the switching points are at +0.45V and −0.45V, thus satisfying the requirements fo MIL-STD-188C LOW level interface. Connecting the R_{IN} pin to the (−) input yields an input impedance in the range of 3kΩ to 7kΩ and satisfies RS-232-C requirements; leaving R_{IN} unconnected, the input resistance will be greater than 6kΩ to satisfy MIL-STD-188C.

The output circuitry is TTL/DTL compatible and will allow "collector-dotting" to generate the wire-AND function. A TTL/DTL strobe is also provided for each receiver. The EIA failsafe mode of operation is shown in the application section of this data sheet.

For the complementary function, see the 9616 triple EIA RS-232C/MIL-STD-188 line driver.

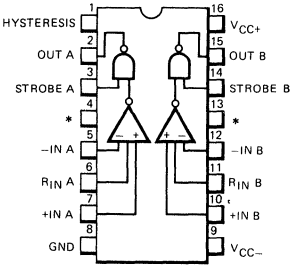
- **EIA RS-232-C INPUT STANDARDS**
- **MIL-STD-188C INPUT STANDARDS**
- **VARIABLE HYSTERESIS CONTROL**
- **HIGH COMMON MODE REJECTION**
- **R_{IN} CONTROL (5kΩ OR 10kΩ)**
- **WIRED-OR CAPABILITY**
- **CHOICE OF INVERTING AND NON-INVERTING INPUTS**
- **OUTPUTS AND STROBE TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

V_{CC+} to Ground	0V to +15V
V_{CC-} to Ground	0V to −15V
Input Voltage Referred to Ground Pin	±25V
Strobe to Ground Voltage	−0.5V to +5.5V
Maximum Applied Output Voltage	−0.5V to +15V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (9627)	−55°C to +125°C
Commercial (9627C)	0°C to +70°C
Internal Power Dissipation (Note 1)	730 mW
Pin Temperature	
Hermetic DIP, (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

NOTE:
1. For Hermetic DIP and Molded DIP rating applies to ambient temperatures up to 65°C, above 65°C derate linearly at 8.3 mW/°C.

CONNECTION DIAGRAM
16-PIN
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P

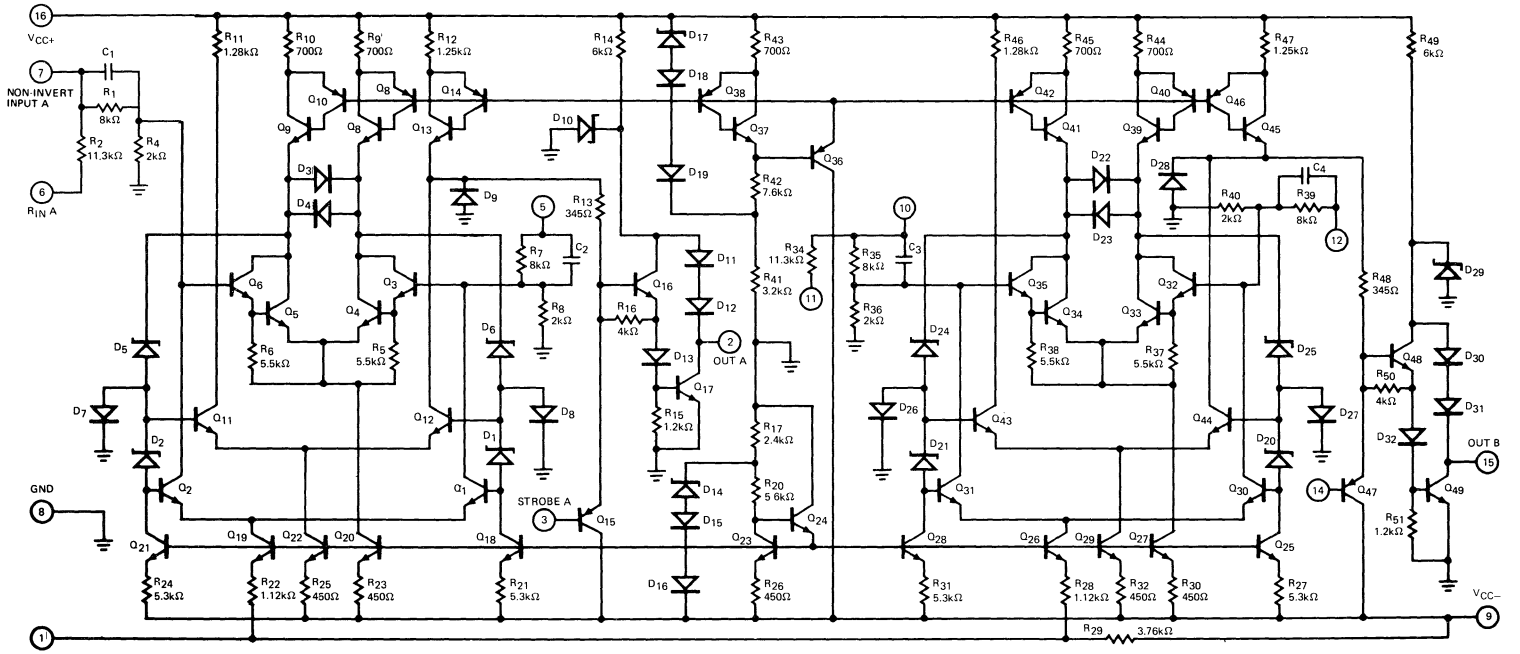


*Internal Connection – make no connection to this pin.

ORDER INFORMATION

TYPE	PART NO.
9627	**9627DM**
9627C	**9627DC**
9627C	**9627PC**

EQUIVALENT CIRCUIT



$C_1 = C_2 = C_3 = C_4 = 1.1$ pF

Pin 4 and 13 = Internal Connection.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 12 V ± 10%, V_{CC-} = −12 V ± 10% over Operating Temperature Range, unless otherwise specified
MIL-STD-188C

SYMBOL	CHARACTERISTICS	CONDITIONS (Pins 6 and 11 Open. Inverting Inputs Open. Pin 1 Open).	MIN	TYP	MAX	UNITS
V_{OL}	Output LOW Voltage	V_{CC+} = +10.8 V, V_{CC-} = −13.2 V Non-Inverting Input = −0.6 V, I_{OL} = 6.4 mA			0.4	V
V_{OH}	Output HIGH Voltage	V_{CC+} = +10.8 V, V_{CC-} = −13.2 V Non-Inverting Input = +0.6 V , I_{OH} = −0.5 mA	2.4			V
I_{SC}	Output Shorted Current	V_{CC+} = +13.2 V, V_{CC-} = −10.8 V Non-Inverting Input = +0.6 V Outputs Grounded			3.0	mA
I_{IH} (Strobe)	Input HIGH Current (Strobe)	V_{CC+} = +10.8 V, V_{CC-} = −13.2 V, V_S = 2.4 V			40	µA
		Non-Inverting Input = +0.6 V, V_S = 5.5 V			1.0	mA
R_{IN}	Input Resistance	V_{CC+} = +13.2 V, V_{CC-} = −13.2 V Non-Inverting Input = +3.0 V or −3.0 V	6.0			kΩ
I_{TH+}	Positive Threshold Current	V_{OUT} = 2.4 V			100	µA
I_{TH-}	Negative Threshold Current	V_{OUT} = 0.4 V	−100			µA
V_{IL} (Strobe)	Input LOW Voltage (Strobe)	$V_{Non\text{-}Inverting\ Input}$ = −0.6 V			0.8	V
V_{IH} (Strobe)	Input HIGH Voltage (Strobe)	$V_{Non\text{-}Inverting\ Input}$ = +0.6 V V_{CC+} = +13.2 V, V_{CC-} = −10.8 V	2.0			V
I_+	Positive Supply Current	$V_{Non\text{-}Inverting\ Input}$ = −0.6 V			18	mA
		T_A = +125°C (9627)			12.4	
I_-	Negative Supply Current	$V_{Non\text{-}Inverting\ Input}$ = +0.6 V	−16			mA
		T_A = +125°C (9627)	−11.4			

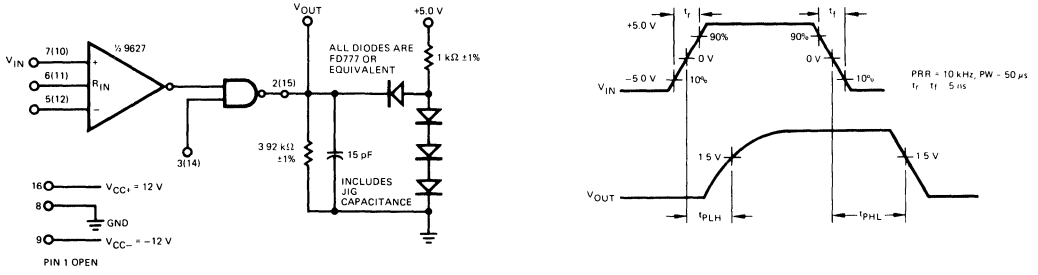
RS-232C

SYMBOL	CHARACTERISTICS	CONDITIONS (Non-Inverting Inputs Connected to Ground, R_{IN} Inputs Connected to Inverting Inputs)	MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	V_{IN} = +3.0 V to +25 V	3.0		7.0	kΩ
		V_{IN} = −3.0 V to −25 V	3.0		7.0	kΩ
V_{IN}	Input Voltage	Open Circuit	−2.0		2.0	V
V_{TH+}	Positive Threshold Voltage				0.6	V
V_{TH-}	Negative Threshold Voltage		−0.6			V

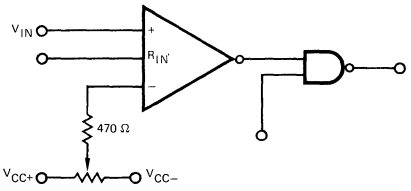
AC CHARACTERISTICS: T_A = +25°C, V_{CC+} = +12 V, V_{CC-} = −12 V
MIL-STD-188C • RS-232-C

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time	See AC Test Circuit		60	250	ns
t_{PHL}	Propagation Delay Time	See AC Test Circuit		84	250	ns

AC TEST CIRCUIT AND WAVEFORMS

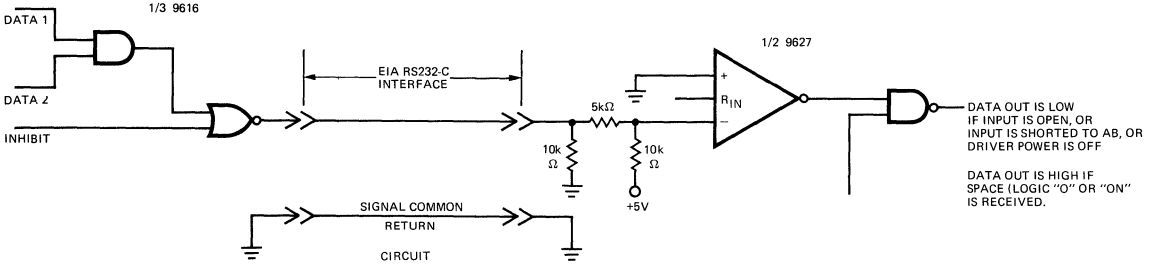


THRESHOLD CURRENT MATCHING CIRCUIT

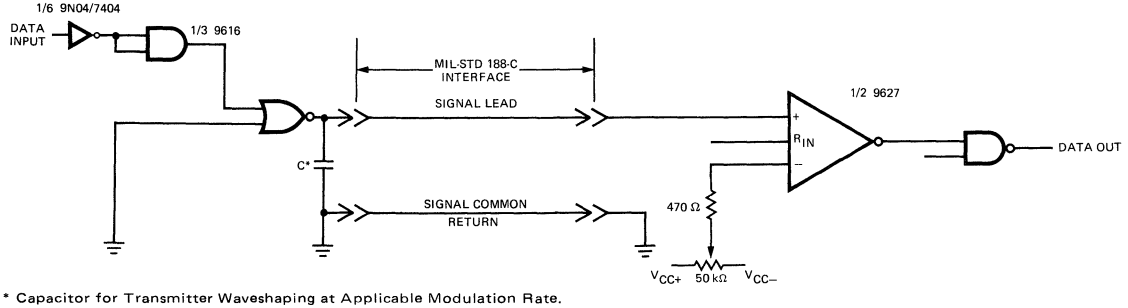


ADJUST POT TO ACHIEVE POSITIVE THRESHOLD CURRENT AND NEGATIVE THRESHOLD CURRENT MATCHING

EIA RS-232-C INTERFACE WITH FAILSAFE RECEIVER (PIN 1 OPEN)



MIL-STD-188C INTERFACE (PIN 1 OPEN)



* Capacitor for Transmitter Waveshaping at Applicable Modulation Rate.

9637A

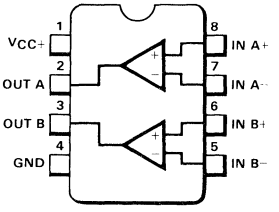
DUAL DIFFERENTIAL LINE RECEIVER (EIA RS-422 AND RS-423 RECEIVER)

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9637A is a Schottky Dual Differential Line Receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422 and RS-423. In addition, the 9637A satisfies the requirements of MIL-STD 188-114 and is inter-operable with the International Standard CCITT recommendations. The 9637A is suitable for use as a line receiver in digital data systems, using either single-ended or differential, unipolar or polar transmission. It requires a single 5 V power supply and has Schottky TTL compatible outputs. The 9637A has an operational input common mode range ±7 V either differentially or to ground.

- **DUAL CHANNELS**
- **SINGLE 5 V SUPPLY**
- **SATISFIES EIA STANDARDS RS-422 AND RS-423**
- **BUILT IN ±35 mV HYSTERESIS**
- **HIGH COMMON MODE RANGE**
- **HIGH INPUT IMPEDANCE**
- **TTL COMPATIBLE OUTPUT**
- **SCHOTTKY TECHNOLOGY**

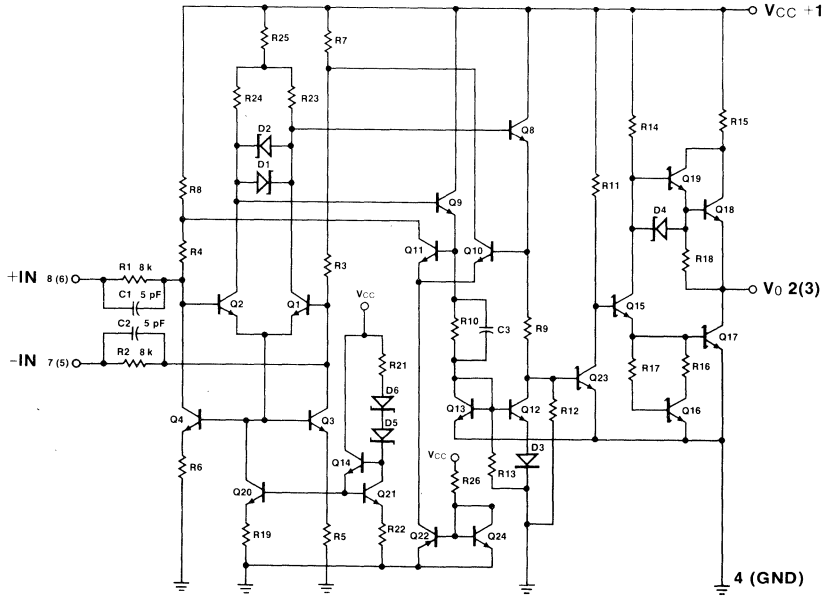
CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
9637A	9637ARM
9637A	9637ARC
9637A	9637ATC

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} Potential to Ground)	-0.5 V to 7.0 V
Input Potential to Ground Pin	±15 V
Differential Input Voltage	±15 V
Output Potential to Ground Pin	-0.5 V to 5.5 V
Output Sink Current	50 mA
Internal Power Dissipation (Note 1) 9T	1.3 W
6T	1.15 W
Operating Temperature; 9637ARM	-55°C to 125°C
9637ARC, 9637ATC	0°C to 70°C
Storage Temperature	-65°C to 150°C
Pin Temperature	
Molded DIP (Soldering, 10 s)	260°C
Hermetic DIP (Soldering, 30 s)	300°C

NOTE:
1. For ambient temperatures above 25°C, derate at 7.7 mW/°C for 6T, and 11.1 mW/°C for 9T package.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	9637ARM			9637ARC, 9637ATC			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage (V_{CC})	4.5	5.0	5.5	4.75	5.0	5.25	V
Operating Ambient Temperature (T_A)	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS: Over recommended temperature and supply voltage ranges, unless otherwise noted.

SYMBOL	CHARACTERISTICS	CONDITIONS (Note 1)	LIMITS (Note 2)			UNITS
			MIN	TYP	MAX	
V_{TH}	Differential Input Threshold Voltage	-7.0 V ≤ V_{CM} ≤ 7.0 V (Note 3)	-0.2		0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage	-7.0 V ≤ V_{CM} ≤ 7.0 V (Note 4)	-0.4		0.4	V
I_{IN}	Input Current	V_{IN} = 10 V, 0 ≤ V_{CC} ≤ 5.5 V (Note 5) V_{IN} = -10 V, 0 ≤ V_{CC} ≤ 5.5 V (Note 5)	 -3.25	1.1 -1.6	3.25	mA mA
V_{OL}	Output LOW Voltage	I_{OL} = 20 mA, V_{CC} = MIN		0.35	0.5	V
V_{OH}	Output HIGH Voltage	I_{OH} = -1.0 mA, V_{CC} = MIN	2.5	3.5		V
I_{SC}	Output Short Circuit Current	V_{OUT} = 0 V, V_{CC} = MAX (Note 6)	-40	-75	-100	mA
I_{CC}	Supply Current	V_{CC} = MAX, $V_{IN(+)}$ = 0.5 V, $V_{IN(-)}$ = GND, (Both outputs low)		35	50	mA
V_{HYST}	Input Hysterisis	V_{CM} = ±7 V (Figure 1)		70		mV

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time LOW to HIGH	Figure 2		15	25	ns
t_{PHL}	Propagation Delay Time HIGH to LOW	Figure 2		13	25	ns

NOTES:
1. Use MIN/MAX values specified in recommended operating conditions.
2. Typical limits are at V_{CC} = 5.0 V and 25°C.
3. V_{DIFF} (Differential Input Voltage) = [(V_{IN+}) - (V_{IN-})]
   V_{CM} (Common Mode Input Voltage) = [(V_{IN+}) - (V_{IN-})]
4. 500 Ω ±1% in series with inputs.
5. The input not under test is tied to ground.
6. Only one output should be shorted at a time.

TYPICAL INPUT/OUTPUT TRANSFER CHARACTERISTICS

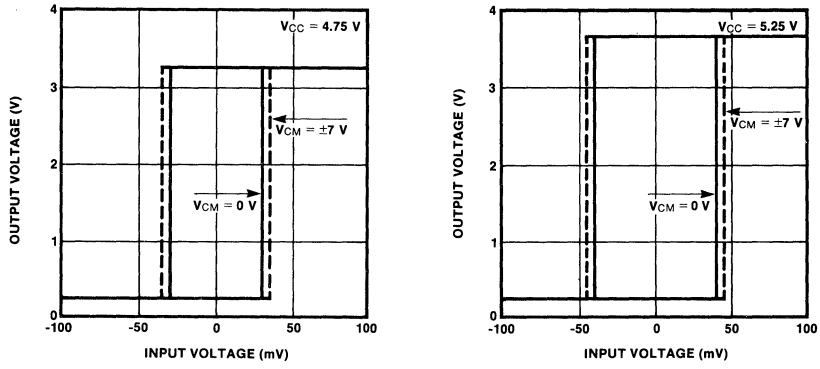
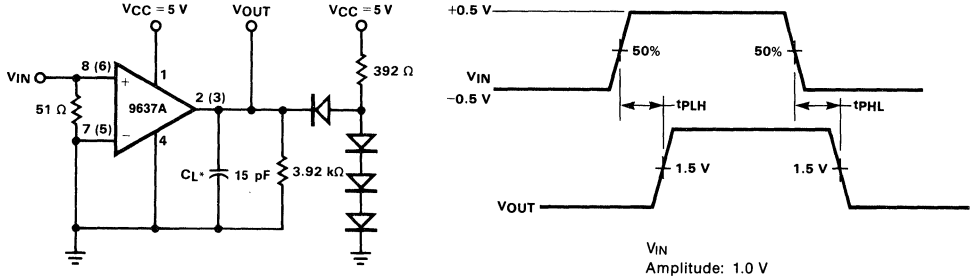


Fig. 1

SWITCHING TEST CIRCUIT AND AC WAVEFORMS



*Includes Jig and Probe Capacitance.
All Diodes are FD700s or Equivalent.

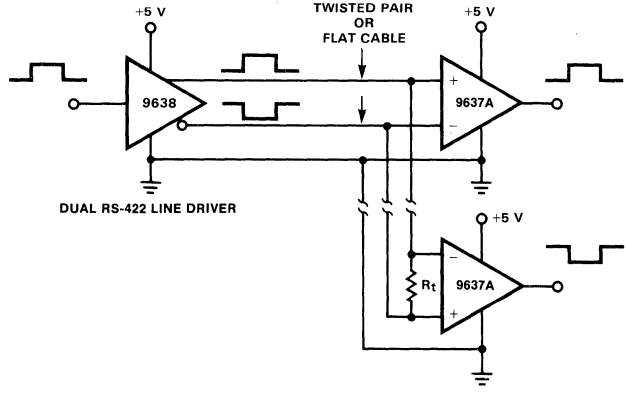
V_{IN}
Amplitude: 1.0 V
Offset: 0.5 V
Pulse Width: 100 ns
PRR: 5 MHz
t_r $t_f \leq 5$ ns

Fig. 2

t_r, $t_f \leq 5$ ns

APPLICATIONS

RS-422 SYSTEM APPLICATION (FIPS 1020)
DIFFERENTIAL SIMPLEX BUS TRANSMISSION



$R_t \geq 50\ \Omega$ for RS-422 operation
R_t combined with input impedance of receivers must be greater than 90 Ω

μA8T26A • μA8T28

QUAD 3-STATE BUS TRANSCEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUIT

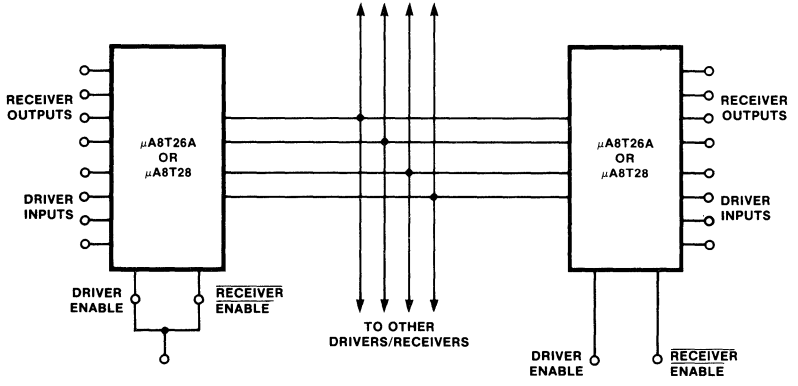
GENERAL DESCRIPTION — μA8T26A and μA8T28 are quad 3-state bus transceivers featuring MPU or MOS compatibility. Both parts feature high-impedance PNP inputs and high-speed operation made possible by the use of Schottky transistor technology.

These devices are useful as bus extenders in systems employing the F6800, F3870 or other comparable MPU families. Maximum input current of 200 μA at the device input pins assures proper operation despite limited drive capability of the MPU chip.

The μA8T26A/28 are identical to the NE8T26A/28 or the MC8T26A/28.

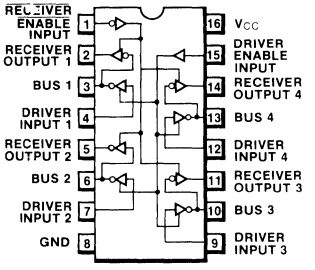
- **μA8T26A — INVERTING BUS**
- **μA8T28 — NON-INVERTING**
- **MPU COMPATIBLE**
- **HIGH-IMPEDANCE PNP INPUTS**
- **HIGH-SPEED SCHOTTKY TECHNOLOGY**
- **+5 V SINGLE SUPPLY OPERATION**
- **3-STATE DRIVERS AND RECEIVERS**

BIDIRECTIONAL BUS APPLICATION



CONNECTION DIAGRAMS
16-PIN DIP (TOP VIEW)
μA8T26A

PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P

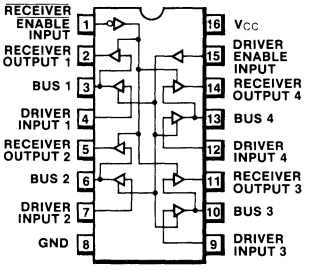


ORDER INFORMATION

TYPE	PART NO.
μA8T26A	μA8T26APC
μA8T26A	μA8T26ADC
μA8T26A	μA8T26ADM

μA8T28

PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA8T28	μA8T28PC
μA8T28	μA8T28DC
μA8T28	μA8T28DM

ABSOLUTE MAXIMUM RATINGS: T_A = 25°C unless otherwise noted

Power Supply Voltage (V_{CC})	8.0 V
Input Voltage (V_I)	5.5 V
Junction Temperature (T_J)	
Ceramic Package	175°C
Plastic Package	150°C
Operating Ambient Temperature Range (T_A)	-55°C to +125°C
Storage Temperature Range (T_{stg})	-65°C to +150°C

ELECTRICAL CHARACTERISTICS: 4.75 V ≤ V_{CC} ≤ 5.25 V for 0°C ≤ T_A ≤ 70°C, and 4.5 V ≤ V_{CC} ≤ 5.5 V for -55°C ≤ T_A ≤ +125°C, unless otherwise noted

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS
	Input Current - LOW Logic State				
$I_{IL(\overline{RE})}$	$\overline{\text{Receiver Enable}}$ Input, $V_{IL(RE)}$ = 0.4 V	—	—	-200	μA
$I_{IL(DE)}$	Driver Enable Input, $V_{IL(DE)}$ = 0.4 V	—	—	-200	
$I_{IL(D)}$	Driver Input, $V_{IL(D)}$ = 0.4 V	—	—	-200	
$I_{IL(B)}$	Bus Receiver Input, $V_{IL(B)}$ = 0.4 V	—	—	-200	
	Input Disabled Current - LOW Logic State				
$I_{IL(D)\ DIS}$	Driver Input, $V_{IL(D)}$ = 0.4 V	—	—	-25	μA
	Input Current - HIGH Logic State				
$I_{IH(\overline{RE})}$	$\overline{\text{Receiver Enable}}$ Input, $V_{IH(RE)}$ = 5.25 V	—	—	25	μA
$I_{IH(DE)}$	Driver Enable Input, $V_{IH(DE)}$ = 5.25 V	—	—	25	
$I_{IH(D)}$	Driver Input, $V_{IH(D)}$ = 5.25 V	—	—	25	
$I_{IH(B)}$	Receiver Input, $V_{IH(B)}$ = 5.25 V (μA8T26 only)	—	—	100	
	Input Voltage - LOW Logic State				
$V_{IL(\overline{RE})}$	$\overline{\text{Receiver Enable}}$ Input	—	—	0.85	V
$V_{IL(DE)}$	Driver Enable Input	—	—	0.85	
$V_{IL(D)}$	Driver Input	—	—	0.85	
$V_{IL(B)}$	Receiver Input	—	—	0.85	
	Input Voltage - HIGH Logic State				
$V_{IH(RE)}$	$\overline{\text{Receiver Enable}}$ Input	2.0	—	—	V
$V_{IH(DE)}$	Driver Enable Input	2.0	—	—	
$V_{IH(D)}$	Driver Input	2.0	—	—	
$V_{IH(B)}$	Receiver Input	2.0	—	—	
	Output Voltage - LOW Logic State				
$V_{OL(B)}$	Bus Driver Output, $I_{OL(B)}$ = 48 mA	—	—	0.5	V
$V_{OL(R)}$	Receiver Output, $I_{OL(R)}$ = 20 mA	—	—	0.5	
	Output Voltage - HIGH Logic State				
$V_{OH(B)}$	Bus Driver Output, $I_{OH(B)}$ = -10 mA	2.4	3.1	—	V
$V_{OH(R)}$	Receiver Output, $I_{OH(R)}$ = -2.0 mA	2.4	3.1	—	
	Receiver Output, $I_{OH(R)}$ = -100 μA, V_{CC} = 5.0 V	3.5	—	—	
	Output Disabled Leakage Current - HIGH Logic State				
$I_{OHL(B)}$	Bus Driver Output, $V_{OH(B)}$ = 2.4 V	—	—	100	μA
$I_{OHL(R)}$	Receiver Output, $V_{OH(R)}$ = 2.4 V	—	—	100	
	Output Disabled Leakage Current - LOW Logic State				
$I_{OLL(B)}$	Bus Output, $V_{OL(B)}$ = 0.5 V	—	—	-100	μA
$I_{OLL(R)}$	Receiver Output, $V_{OL(R)}$ = 0.5 V	—	—	-100	
	Input Clamp Voltage				
$V_{IC(DE)}$	Driver Enable Input $I_{ID(DE)}$ = -12 mA	—	—	-1.0	V
$V_{IC(RE)}$	$\overline{\text{Receiver Enable}}$ Input $I_{IC(RE)}$ = -12 mA	—	—	-1.0	
$V_{IC(D)}$	Driver Input $I_{IC(D)}$ = -12 mA	—	—	-1.0	
	Output Short-Circuit Current, V_{CC} = 5.25 V(1)				
$I_{OS(B)}$	Bus Driver Output	-50	80	-150	mA
$I_{OS(R)}$	Receiver Output	-30	50	-75	
	Power Supply Current				
I_{CC}	V_{CC} = 5.25 V	—	50	87	mA

(1) Only one output may be short-circuited at a time

μA8T26A SWITCHING CHARACTERISTICS: Unless otherwise noted, specifications apply at $T_A = 25°C$ and $V_{CC} = 5.0$ V

SYMBOL	CHARACTERISTICS	FIGURE	TYP	MAX	UNITS
$t_{PLH(R)}$	Propagation Delay Time from Receiver (Bus) Input to HIGH Logic State Receiver Output	1	9	14	ns
$t_{PHL(R)}$	Propagation Delay Time from Receiver (Bus) Input to LOW Logic State Receiver Output	1	6	14	ns
$t_{PLH(D)}$	Propagation Delay Time from Driver Input to HIGH Logic State Driver (Bus) Output	2	10	14	ns
$t_{PHL(D)}$	Propagation Delay Time from Driver Input to LOW Logic State Driver (Bus) Output	2	10	14	ns
$t_{PLZ(RE)}$	Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to HIGH Impedance (Open) Logic State Receiver Output	3	10	15	ns
$t_{PZL(RE)}$	Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to LOW Logic Level Receiver Output	3	15	20	ns
$t_{PLZ(DE)}$	Propagation Delay Time from Driver Enable Input to HIGH Impedance Logic State Driver (Bus) Output	4	15	20	ns
$t_{PZL(DE)}$	Propagation Delay Time from Driver Enable Input to LOW Logic State Driver (Bus) Output	4	19	25	ns

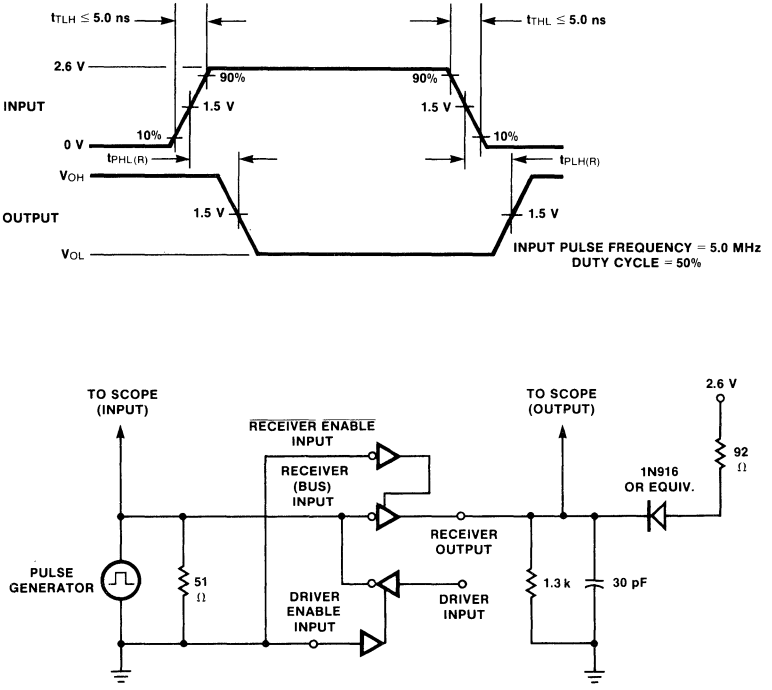


Fig. 1 μA8T26A Test Circuit and Waveforms or Propagation Delay Time from Bus (Receiver) Input to Receiver Output, $t_{PLH(R)}$ and $t_{PHL(R)}$

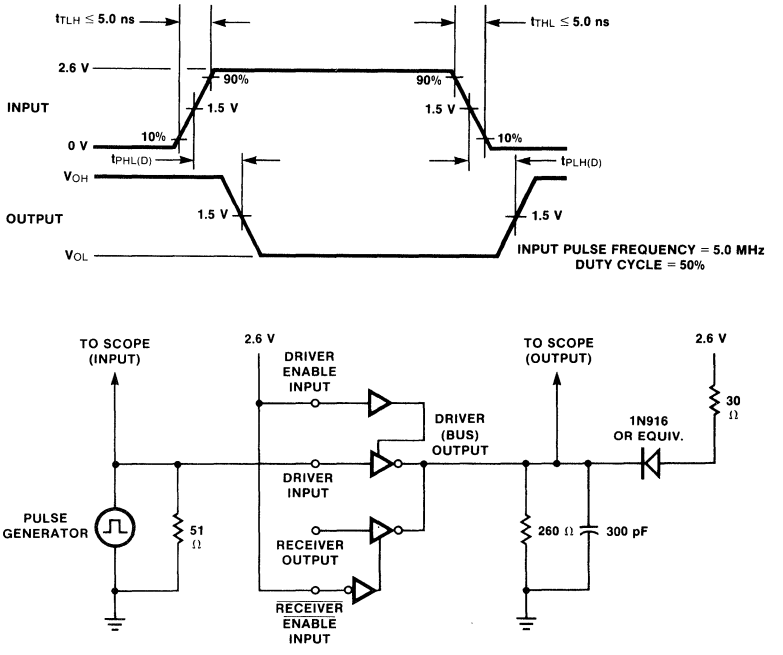


Fig. 2 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Driver Input to Bus (Driver) Output, $t_{PLH(D)}$ and $t_{PHL(D)}$

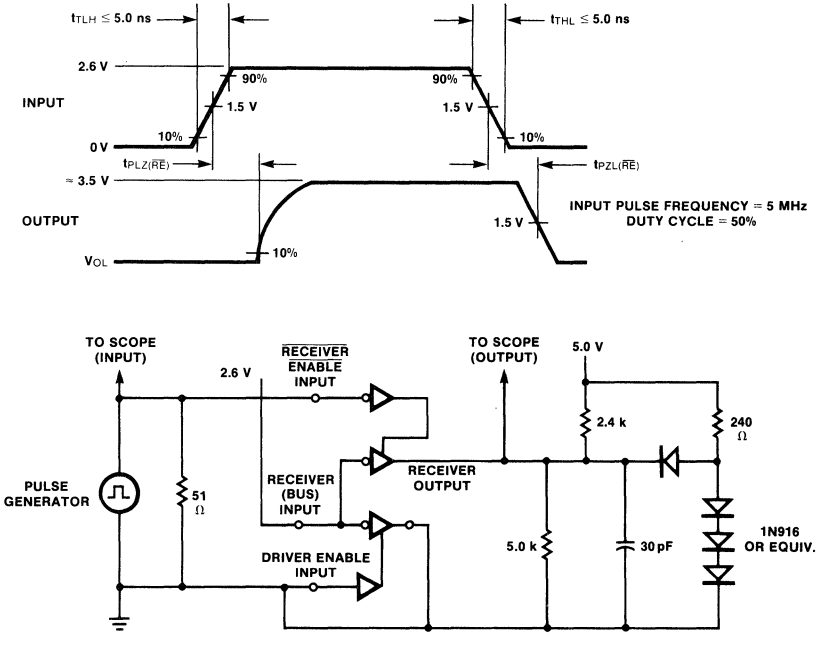


Fig. 3 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Receiver Enable Input to Receiver Output, $t_{PLZ(RE)}$ and $t_{PZL(RE)}$

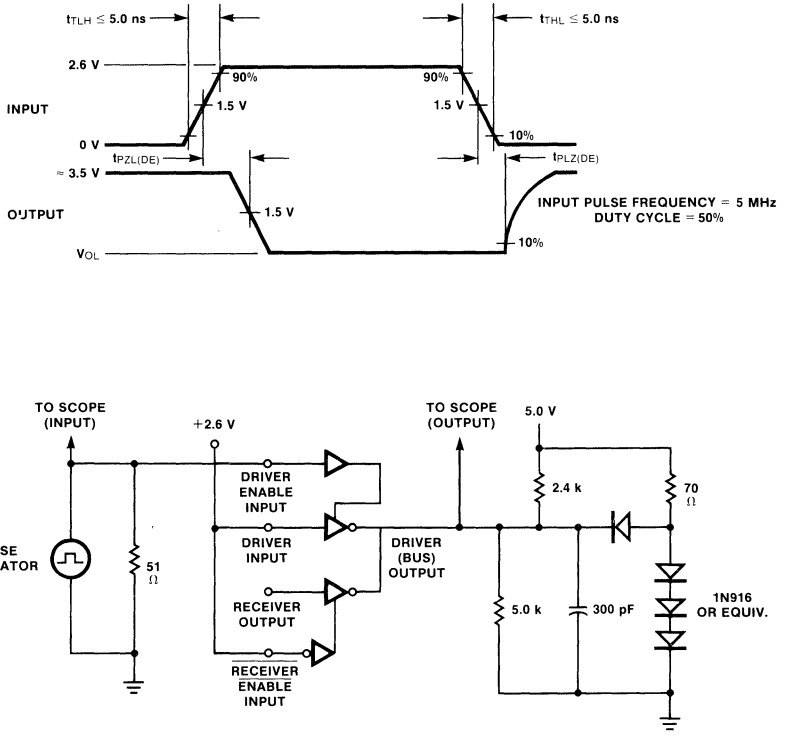


Fig. 4 μA8T26A Test Circuit and Waveforms for Propagation Delay Time from Driver Enable Input to Driver (Bus) Output, $t_{PLZ(DE)}$ and $t_{PZL(DE)}$

μA8T28 SWTICHING CHARACTERISTICS: Unless otherwise noted, V_{CC} = 5.0 V and T_A°C

SYMBOL	CHARACTERISTIC	FIGURE	TYP	MAX	UNITS
$t_{PLH(R)}$ $t_{PHL(R)}$	Propagation Delay Time — Receiver (C_L = 30 pF)	5	-12 -9	17 17	ns
$t_{PLH(D)}$ $t_{PHL(D)}$	Propagation Delay Time — Driver (C_L = 300 pF)	6	-13 -13	17 17	ns
$t_{PZL(RE)}$ $t_{PLZ(RE)}$	Propagation Delay Time — Receiver Enable (C_L = 30 pF)	7	-18 -13	23 18	ns
$t_{PZL(DE)}$ $t_{PLZ(DE)}$	Propagation Delay Time — Driver Enable (C_L = 300 pF)	8	-21 -18	28 23	ns

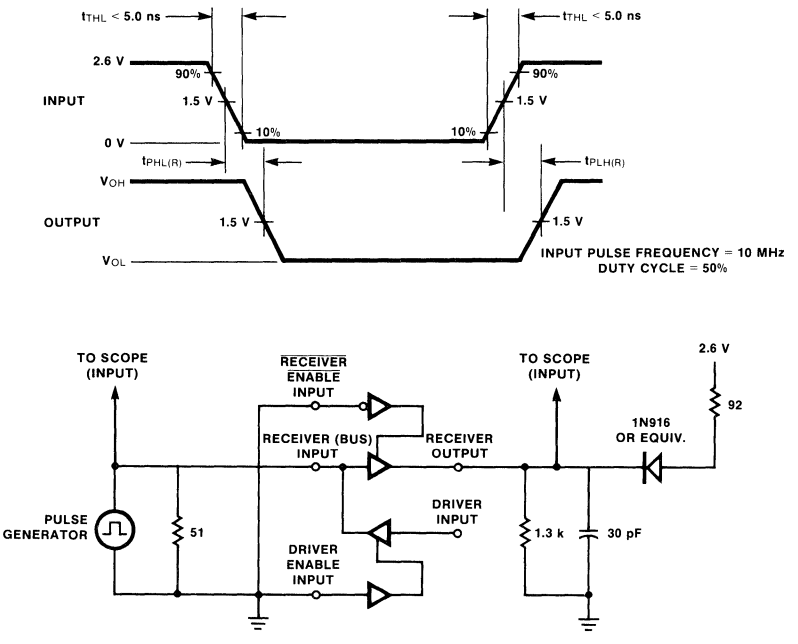


Fig. 5 μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Bus (Receiver) Input to Receiver Output, $t_{PLH(R)}$ and $t_{PHL(R)}$

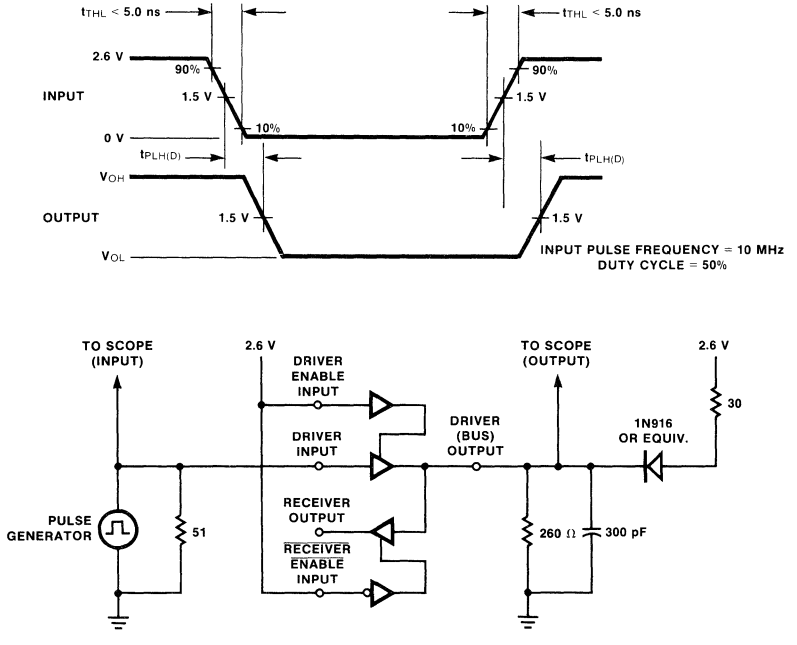


Fig. 6 μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Driver Input to Bus (Driver) Output, $t_{PLH(D)}$ and $t_{PHL(D)}$

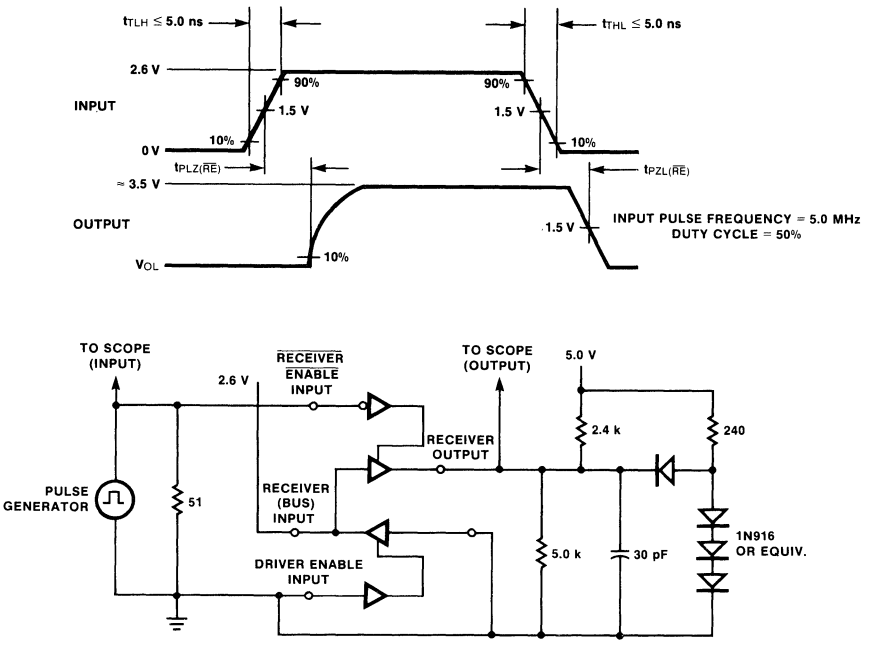


Fig. 7 μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Receiver Enable Input to Receiver Output, $t_{PLZ(RE)}$ and $t_{PZL(RE)}$

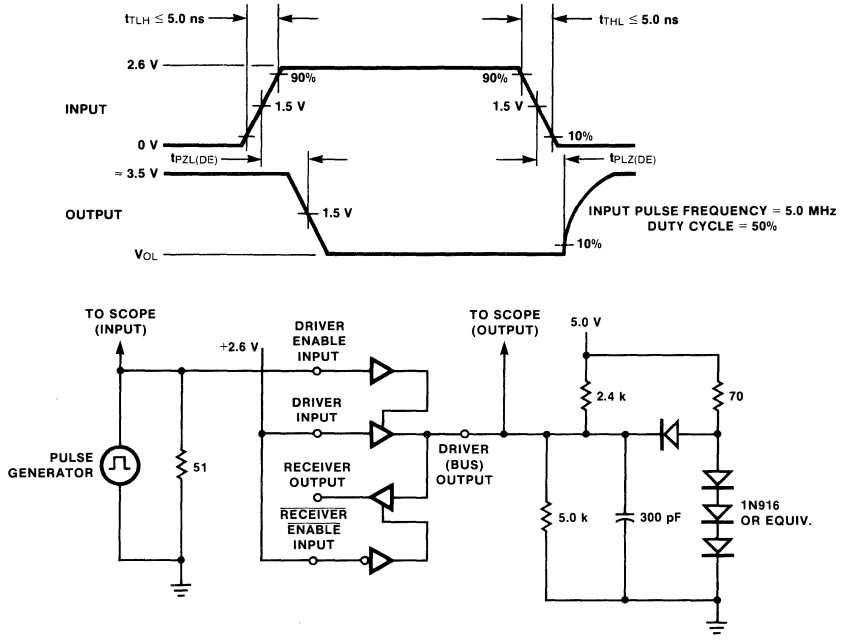


Fig. 8 μA8T28 Test Circuit and Waveforms for Propagation Delay Time from Driver Enable Input to Driver (Bus) Output, $t_{PLZ(DE)}$ and $t_{PZL(DE)}$

9640/26S10 • 9641/26S11 • 9642

QUAD GENERAL PURPOSE BUS TRANSCEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 9640, 9641 and 9642 are High-Speed Quad Bus Transceivers. Each driver output, which is capable of sinking 100 mA at 0.8 V, is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads. The bus output is capable of driving lines having 100 Ω impedance.

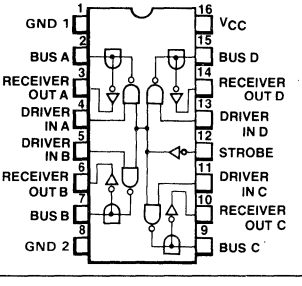
The line can be terminated at both ends and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 V.

The 9640, 9641, and 9642 feature advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

The 9640 and 9641 are pin for pin replacements of the AM26S10 and AM26S11 respectively.

The 9642 is the same device as the 9640 with hysteresis. The hysteresis characteristic of the 9642 receiver is chosen so that the receiver switches to a HIGH logic level when the receiver input is at a HIGH logic level and moves to 1.4 V typically, and switches to a LOW logic level when the receiver input is at a LOW logic level and moves to 2.0 V typically. This hysteresis characteristic allows for increased noise immunity in low speed applications.

- **INPUT TO BUS IS INVERTING ON 9640 AND 9642**
- **INPUT TO BUS IS NON-INVERTING ON 9641**
- **QUAD HIGH-SPEED OPEN COLLECTOR BUS TRANSCEIVERS**
- **DRIVER OUTPUTS CAN SINK 100 mA AT 0.8 V MAXIMUM**
- **ADVANCED SCHOTTKY PROCESSING**
- **PNP INPUTS TO REDUCE INPUT LOADING**
- **600 mV RECEIVER HYSTERESIS (9642 ONLY)**



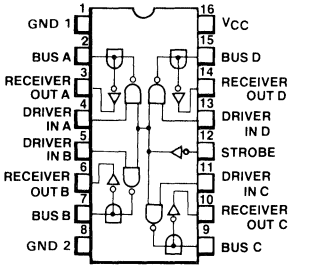
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P

9642

ORDER INFORMATION

TYPE	PART NO.
9642	9642DM
9642	9642DC
9642	9642PC

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P

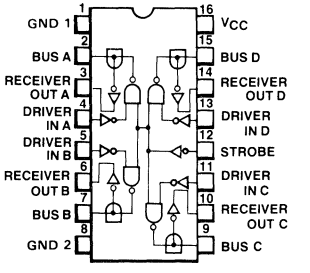


9640

ORDER INFORMATION

TYPE	PART NO.
9640	**9640DM/26S10**
9640	**9640DC/26S10**
9640	**9640PC/26S10**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



9641

ORDER INFORMATION

TYPE	PART NO.
9641	**9641DM/26S11**
9641	**9641DC/26S11**
9641	**9641PC/26S11**

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} Max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, into Bus	200 mA
Output Current, into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5.0 mA

TRUTH TABLES

9640/42

INPUTS		OUTPUTS	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	Y

9641

INPUTS		OUTPUTS	
$\overline{E}$	I	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	Y

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by another Bus Transceiver)

6

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	DM			DC, PC			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Positive Supply Voltage	4.50	5.0	5.5	4.75	5.0	5.25	V
Operating Ambient Temperature − T_A	−55	+25	+125	0	+25	+70	°C

ELECTRICAL CHARACTERISTICS: Over Operating Range, unless otherwise specified

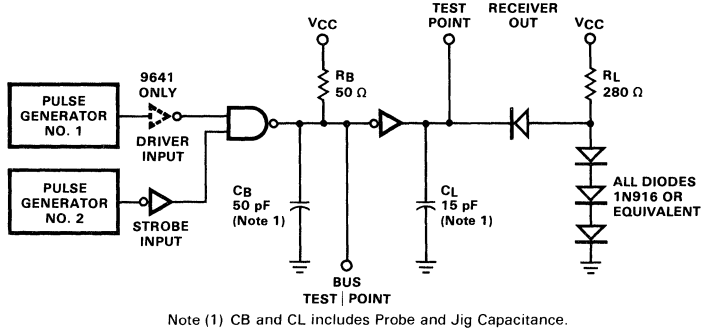
SYMBOL	CHARACTERISTICS	CONDITIONS (Note 1)		MIN	TYP (Note 2)	MAX	UNITS
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN, I_{OH} = −1.0 mA, V_{IN} = V_{IL} or V_{IH}	DM	2.5	3.4		V
			DC, PC	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN, I_{OL} = 20 mA, V_{IN} = V_{IL} or V_{IH}				0.5	V
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed Input Logical HIGH for all Inputs		2.0			V
V_{IL}	Input LOW Level (Except Bus)	Guaranteed Input Logical LOW for all Inputs				0.8	V
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4 V	ENABLE			−0.36	mA
			DATA			−0.54	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7 V	ENABLE			20	μA
			DATA			30	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX, (Note 3)	DM	−20		−55	mA
			DC, PC	−18		−60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX, Enable = GND	9640		45	70	mA
			9641/42			80	

AC CHARACTERISTICS: $T_A = +25°C$, $V_{CC} = 5.0$ V

SYMBOL	CHARACTERISTICS		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Data Input to Bus	9640	$R_B = 50\ \Omega$, $C_B = 50$ pF (Note 1)		10	15	ns
t_{PHL}		9642			10	15	
t_{PLH}		9641			12	19	
t_{PHL}					12	19	
t_{PLH}	Enable Input to Bus	9640			14	18	ns
t_{PLH}		9642			13	18	
t_{PLH}		9641			15	20	
t_{PHL}					14	20	
t_{PLH}	Bus to Receiver Out	9640/41	$R_B = 50\ \Omega$, $R_L = 280\ \Omega$, $C_B = 50$ pF, $C_L = 15$ pF (Note 1)		10	15	ns
t_{PHL}		9642			10		
t_{PLH}		9640/41			10	15	
t_{PHL}		9642			10		
t_r	Bus		$R_B = 50\ \Omega$, $C_B = 50$ pF (Note 1)	4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1 Includes probe and jig capacitance.

AC TEST CIRCUIT



Note (1) CB and CL includes Probe and Jig Capacitance.

Fig. 1

WAVEFORMS

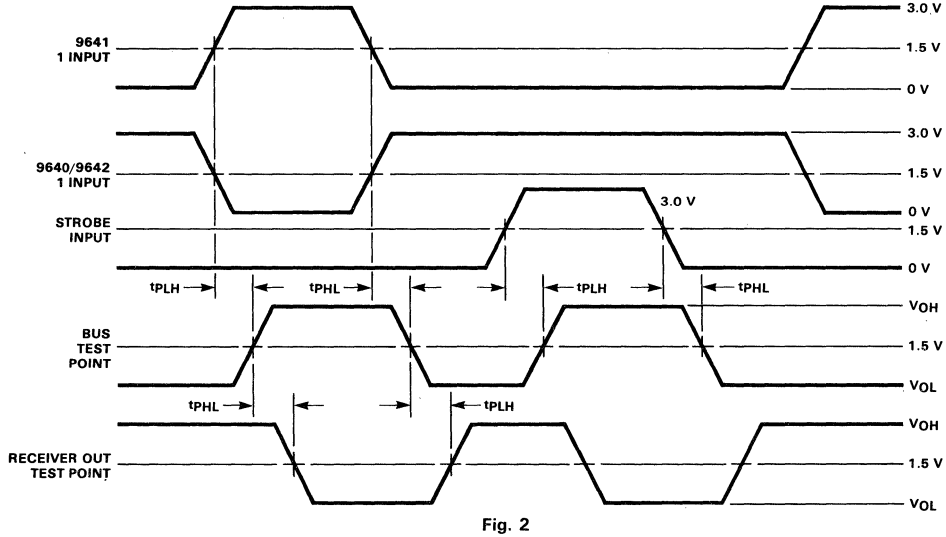


Fig. 2

BUS INPUT/OUTPUT CHARACTERISTICS

SYMBOL	CHARACTERISTICS	CONDITIONS (Note 1)			MIN	TYP (Note 2)	MAX	UNITS
V_{OL}	Output LOW Voltage	V_{CC} = Min	DM	I_{OL} = 40 mA		0.33	0.5	V
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
			DC,PC	I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = Max		V_O = 0.8 V			−50	μA
			DM	V_O = 4.5 V			200	
			DC,PC	V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5 V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4 V V_{CC} = Max		9640/9641 DM		2.0	2.4	V
				9640/9641 DC, PC		2.0	2.25	
				9642	1.8	2.0	2.2	
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4 V V_{CC} = Min		9640/9641 DM	1.6	2.0		V
				9640/9641 DC,PC	1.75	2.0		
				9642	1.2	1.4	1.6	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

RECEIVER INPUT HYSTERESIS CHARACTERISTIC (9642)

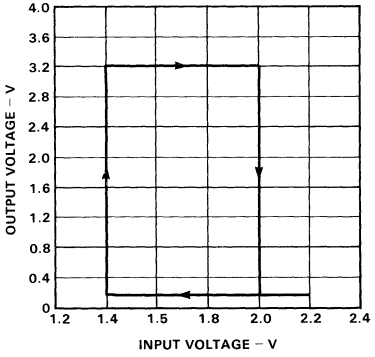
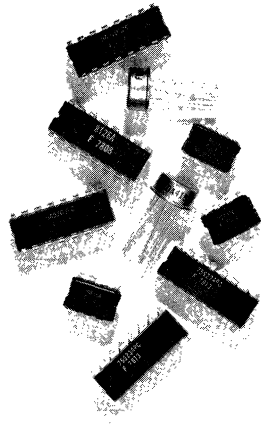


Fig. 3



PERIPHERAL AND DISPLAY DRIVERS

Peripheral Drivers

Display Drivers

55/75450A • 55/75451A • 55/75452A
55/75453A • 55/75454A
DUAL PERIPHERAL DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55/75450A, 55/75451A, 55/75452A, 55/75453A and 55/75454A are Dual High Speed General Purpose Interface Drivers that convert TTL and DTL logic levels to high current drive capability. The 55450A and 75450A feature two TTL NAND gates and two uncommitted transistors. The 55/75451A, 55/75452A, 55/75453A and 55/75454A feature two standard series 74 TTL gates in AND, NAND, OR and NOR configurations respectively, driving the base of two high voltage, high current, uncommitted collector output transistors.

The 55/75450A series offers flexibility in designing high speed logic buffers, power drivers, lamp drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- **NO LATCH-UP AT 20 V**
- **HIGH OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

TEST TABLE 1 — Operating Temperature Range and Supply Voltage Range

	55450A Series	75450A Series
Temperature, T_A	−55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

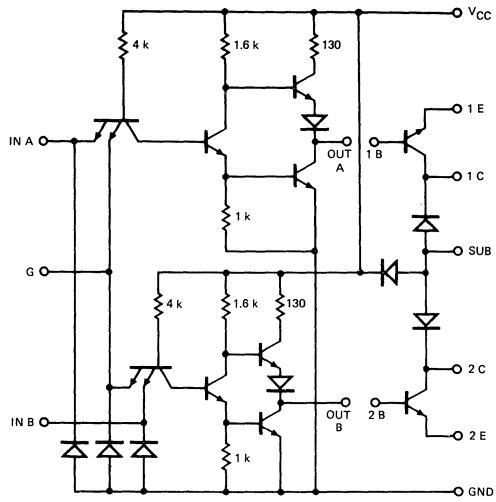
ABSOLUTE MAXIMUM RATINGS

	55450A	75450A	55451A 55452A 55453A 55454A	75451A 75452A 75453A 75454A
Supply Voltage, V_{CC} (See Note 1)	7 V	7 V	7 V	7 V
Input Voltage (See Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage(See Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Base Voltage	35 V	35 V		
Collector to Emitter Voltage (See Note 3)	30 V	30 V		
Emitter to Base Voltage	5 V	5 V		
Output Voltage (See Notes 1 and 4)			30 V	30 V
Continuous Collector Current (See Note 5)	300 mA	300 mA		
Continuous Output Current (See Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (See Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Ambient Temperature Range	−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Pin Temperature				
Molded DIP (Soldering, 10 s)		260°C	260°C	260°C
Hermetic DIP (Soldering, 60 s)	300°C	300°C	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.
6. For the 55450A and 75450A only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP. For the Molded Mini DIP and Ceramic Mini DIP, derate at 6.7 mW/°C above 30°C.

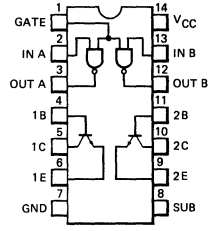
55450A/75450A
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-PIN
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



LOGIC FUNCTION

Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = XY$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
55450A	55450ADM
75450A	75450ADC
75450A	75450APC

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

TTL Gates

SYMBOL	CHARACTERISTICS		TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNIT
V_{IH}	Input HIGH Voltage		1			2			V
V_{IL}	Input LOW Voltage		2					0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = MIN, V_{IL} = 0.8 V I_{OH} = −400 μA		2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = MIN, V_{IH} = 2 V	55450A		0.22	0.5	V
				I_{OL} = 16 mA	75450A		0.22	0.4	
I_I	Input Current at Maximum Input Voltage	Input A	4	V_{CC} = MAX, V_I = 5.5 V				1	mA
		Input G						2	
I_{IH}	Input HIGH Current	Input A	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Input G						80	
I_{IL}	Input LOW Current	Input A	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Input G						−3.2	
I_{OS}	Short Circuit Output Current (Note 9)		5	V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = MAX, V_I = 0 V			2	4	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = MAX, V_I = 5 V			6	11	

NOTES:
8. All typical values at V_{CC} = 5 V, T_A = 25°C.
9. Not more than one output should be shorted at a time.

55450A/75450A

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

Output Transistors

SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP (Note 10)	MAX	UNITS
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			V
$V_{(BR)CER}$	Collector to Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 11)	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C		25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA	55450A	10			
			75450A	20			
		V_{CE} = 3 V, I_C = 300 mA	55450A	15			
			75450A	25			
$V_{BE(sat)}$	Base to Emitter Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450A		0.85	1.2	V
			75450A		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA	55450A		1.05	1.4	V
			75450A		1.05	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450A		0.25	0.5	V
			75450A		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA	55450A		0.5	0.8	V
			75450A		0.5	0.7	V

NOTES:
10. All typical values are at V_{CC} = 5 V, T_A = 25°C.
11. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C.

TTL Gates

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		12		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8		ns

Output Transistors

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS (Note 12)	MIN	TYP	MAX	UNITS
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = −1 V		10		ns
t_r	Rise Time		$I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA		14		ns
t_s	Storage Time		C_L = 15 pF, R_L = 50 Ω		10		ns
t_f	Fall Time				11		ns

Gates and Transistors Combined

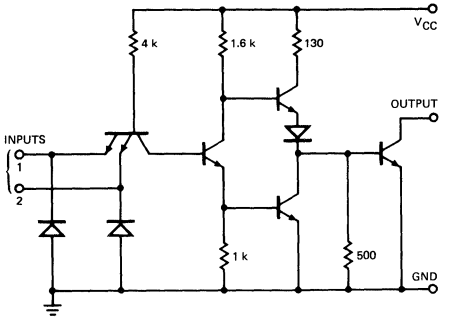
SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		22	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				22	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				10	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				14	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, I_C ≈ 300 mA R_{BE} = 500 Ω	V_S −6.5			mV

NOTE 12. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

7

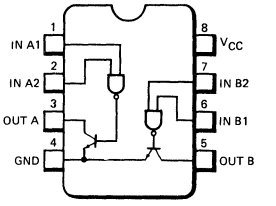
55451A/75451A
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55451A	55451ARM
75451A	75451ARC
75451A	75451ATC

Positive Logic: Z = XY

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 13)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55451A			300	μA
				75451A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55451A		0.25	0.5	V
				75451A		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55451A		0.5	0.8	
				75451A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 5 V			7.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			52	65	mA

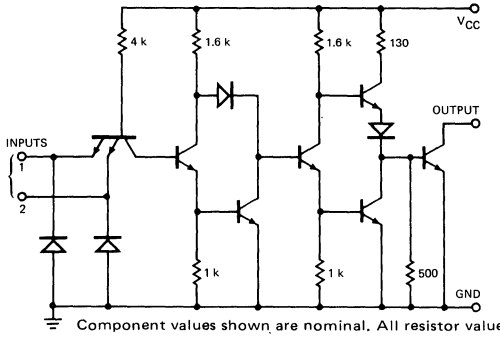
NOTE 13. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISICS: V_{CC} = 5 V, T_A = 25°C.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		20	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				20	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55452A/75452A
DUAL POSITIVE NAND PERIPHERAL DRIVER

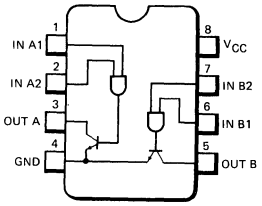
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAM

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55452A	55452ARM
75452A	75452ARC
75452A	75452ATC

Positive Logic: $Z = \overline{XY}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 14)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V	55452A			300	μA
			V_{IL} = 0.8 V	75452A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V	55452A		0.25	0.5	V
			I_{OL} = 100 mA	75452A		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V	55452A		0.5	0.8	
			I_{OL} = 300 mA	75452A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 0 V			11	14	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			56	71	mA

NOTE 14. All typical values are at V_{CC} = 5 V, T_A = 25°C.

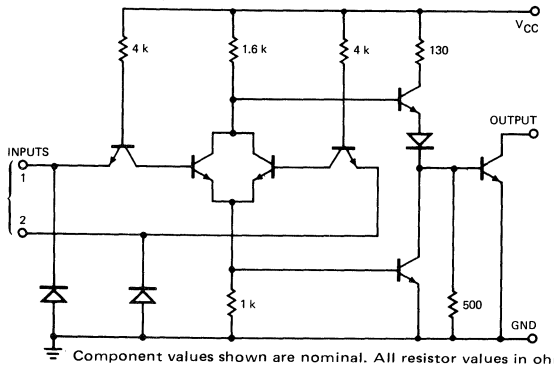
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		25	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55453A/75453A

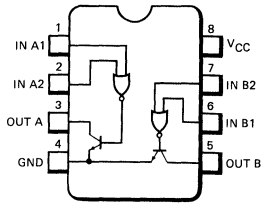
DUAL POSITIVE OR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55453A	55453ARM
75453A	75453ARC
75453A	75453ATC

Positive Logic: $Z = X + Y$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 15)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55453A			300	µA
				75453A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55453A		0.25	0.5	V
				75453A		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55453A		0.5	0.8	
				75453A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			54	68	mA

NOTE 15. All typical values are at V_{CC} = 5 V, T_A = 25°C.

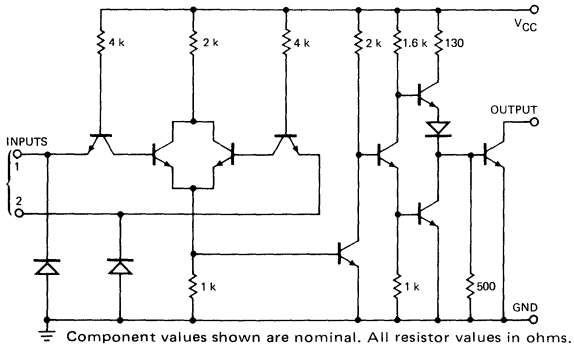
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25 °C.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		20	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				20	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	25	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55454A/75454A

DUAL POSITIVE NOR PERIPHERAL DRIVER

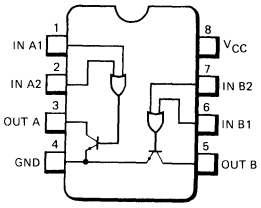
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAM

8-PIN FLATPAK
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55454A	55454ARM
75454A	75454ARC
75454A	75454ATC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 16)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IL} = 0.8 V	55454A			300	μA
				75454A			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55454A		0.25	0.5	V
				75454A		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55454A		0.5	0.8	
				75454A		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			61	79	mA

NOTE 16. All typical values are at V_{CC} = 5 V, T_A = 25°C.

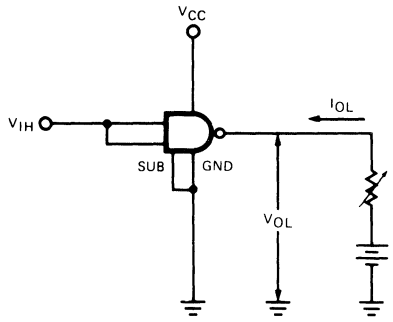
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		25	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				12	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUIT†

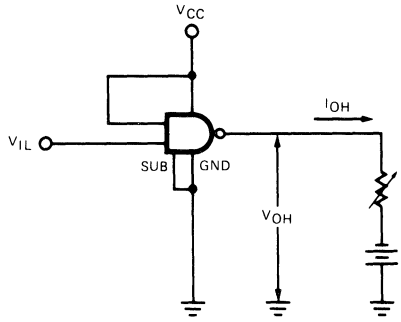
V_{IH}, V_{OL}



Both inputs are tested simultaneously.

Fig. 1

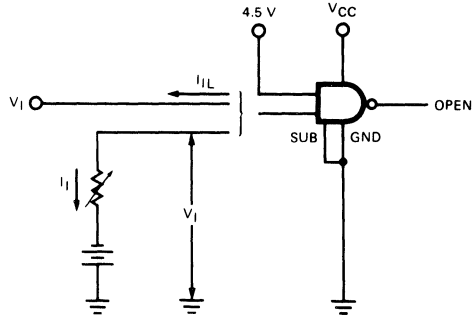
V_{IL}, V_{OH}



Each input is tested separately.

Fig. 2

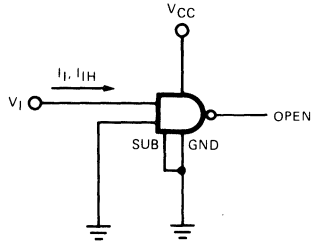
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing V_{CD}, input not under test is open.

Fig. 3

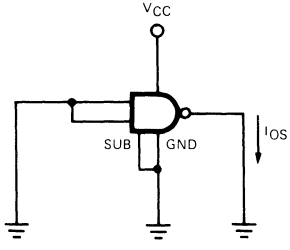
I_I, I_{IH}



Each input is tested separately

Fig. 4

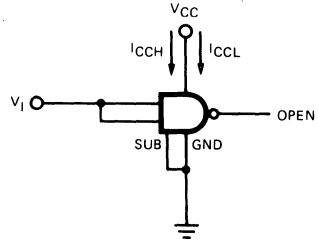
I_{OS}



Each gate is tested separately.
(55450A/75450A only)

Fig. 5

I_{CCH}, I_{CCL}

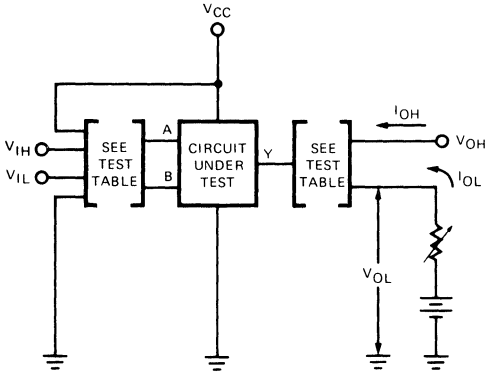


Both gates are tested simultaneously.

Fig. 6

CHARACTERISTICS MEASUREMENT INFORMATION

V_{IH}, V_{IL}, I_{OH}, V_{OL}



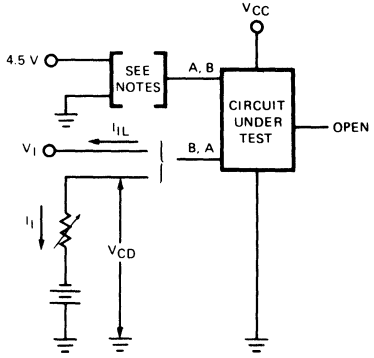
TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75451A	V_{IH}	V_{IH}	V_{OH}	I_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
55/75452A	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	V_{OH}	I_{OH}
55/75453A	V_{IH}	GND	V_{OH}	I_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
55/75454A	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	V_{OH}	I_{OH}

NOTE: Each input is tested separately.

Fig. 7

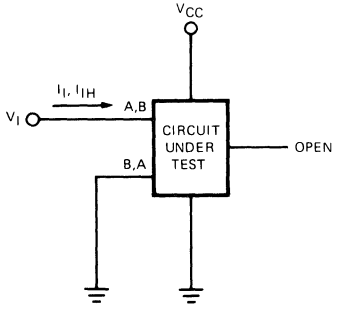
V_{CD}, I_{IL}



NOTES: A. Each input is tested separately.
B. When testing I_{IL} 55/75453A and 55/75454A, the input not under test is grounded. For all other circuits it is at 4.5 V.
C. When testing V_{CD}, input not under test is open.

Fig. 8

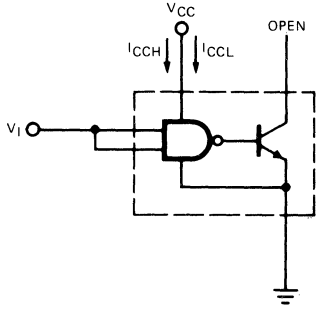
I_I, I_{IH}



Each input is tested separately.

Fig. 9

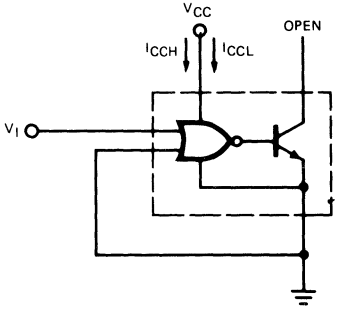
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 10

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

Fig. 11

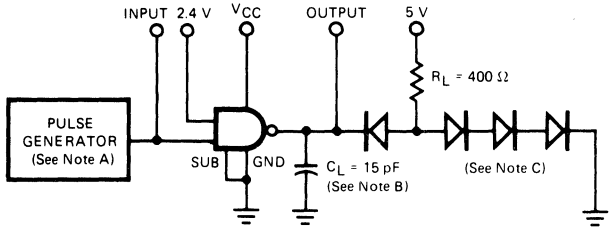
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

CHARACTERISTICS MEASUREMENT INFORMATION

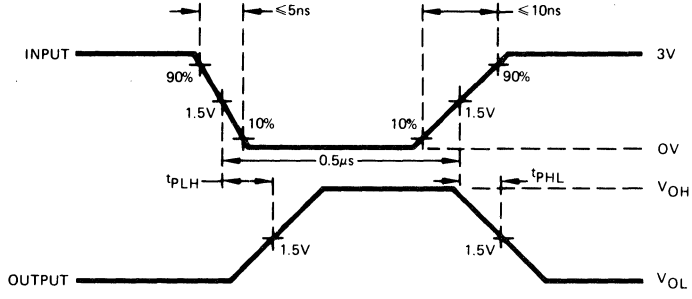
SWITCHING CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE
(55450A, 75450A ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are FD777.

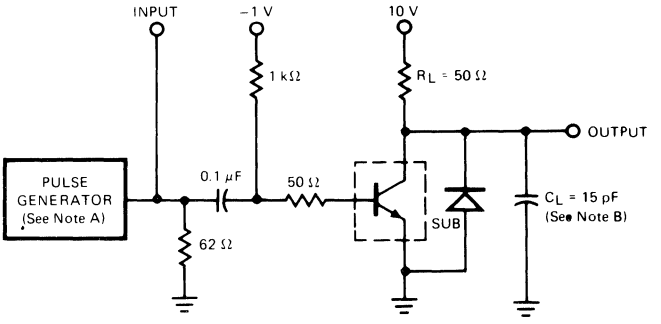
Fig. 12

CHARACTERISTICS MEASUREMENT INFORMATION

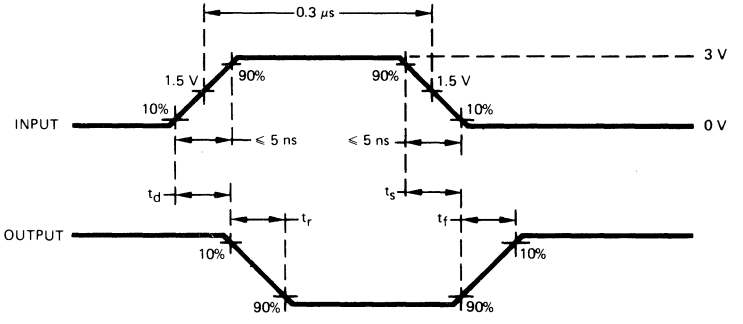
SWITCHING CHARACTERISTICS

SWITCHING TIMES, EACH TRANSISTOR
(55450A, 75450A ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

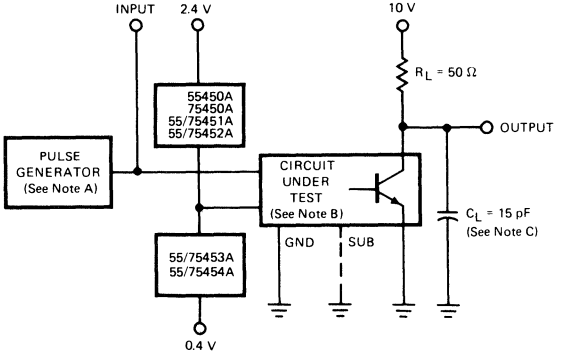
Fig. 13

CHARACTERISTICS MEASUREMENT INFORMATION

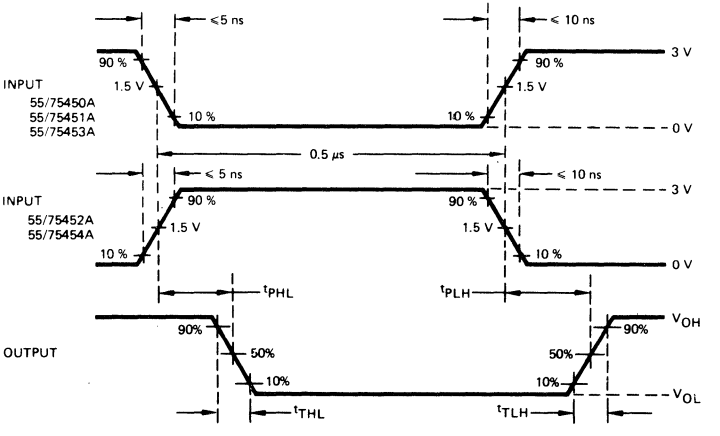
SWITCHING CHARACTERISTICS

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When Testing 55450A/75450A, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

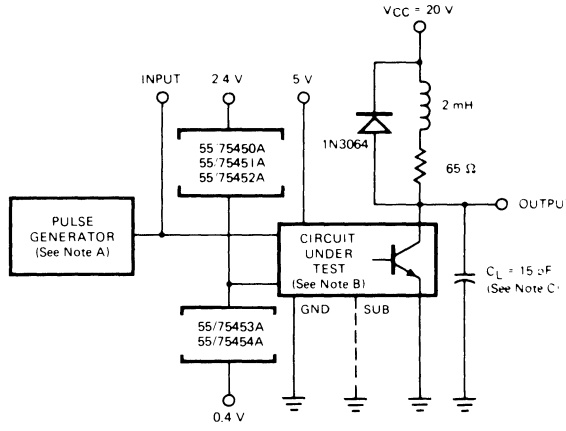
Fig. 14

CHARACTERISTICS MEASUREMENT INFORMATION

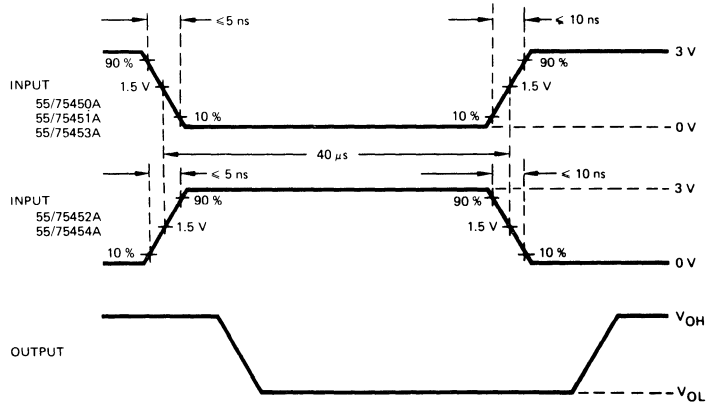
SWITCHING CHARACTERISTICS

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

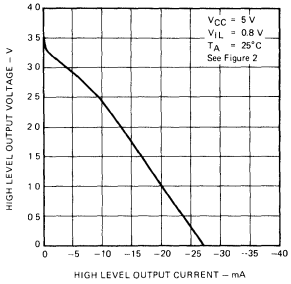


NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing 55450A or 75450A, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

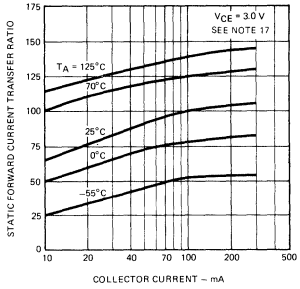
Fig. 15

TYPICAL PERFORMANCE CURVES FOR 75450A SERIES

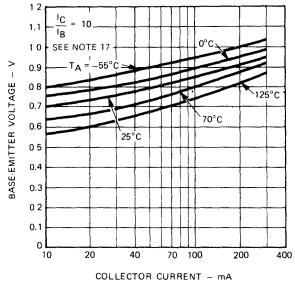
55450A/75450A TTL GATE HIGH-LEVEL OUTPUT VOLTAGE AS A FUNCTION OF HIGH-LEVEL OUTPUT CURRENT



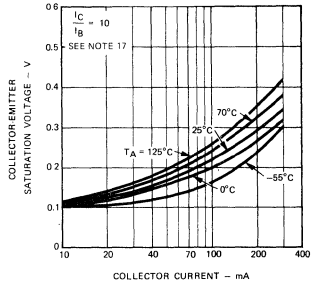
55450A/75450A TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT



55450A/75450A TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



NOTE 17: These parameters must be measured using pulse techniques. t_W = 300 μs, duty cycle $\leqslant$ 2%.

55/75450B • 55/75451B • 55/75452B
55/75453B • 55/75454B
DUAL HIGH SPEED PERIPHERAL DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55/75450B, 55/75451B, 55/75452B, 55/75453B and 55/75454B are Dual High Speed General Purpose Interface Drivers that convert TTL and DTL logic levels to high current drive capability. The 55450B and 75450B feature two TTL NAND gates and two uncommitted transistors. The 55/75451B, 55/75452B, 55/75453B and 55/75454B feature two standard series 74 TTL gates in AND, NAND, OR and NOR configurations respectively, driving the base of two high voltage, high current, uncommitted collector output transistors.

The 55/75450B series offers flexibility in designing high speed logic buffers, power drivers, lamp drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- **NO LATCH-UP AT 20 V**
- **HIGH SPEED SWITCHING**
- **HIGH OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

TEST TABLE 1 – Operating Temperature Range and Supply Voltage Range

	55450B Series	75450B Series
Temperature, T_A	–55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

7

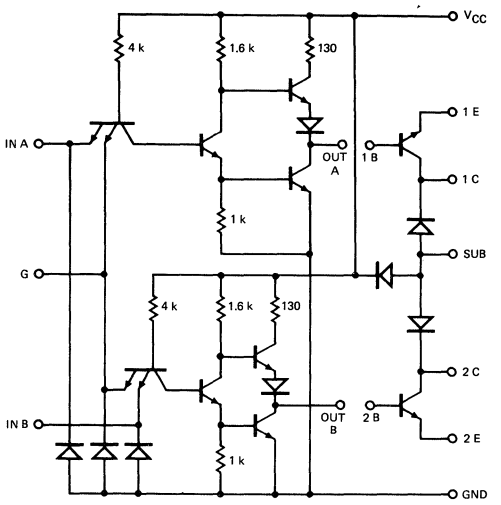
ABSOLUTE MAXIMUM RATINGS

	55450B	75450B	55451B 55452B 55453B 55454B	75451B 75452B 75453B 75454B
Supply Voltage, V_{CC} (See Note 1)	7 V	7 V	7 V	7 V
Input Voltage (See Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage(See Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Substrate Voltage (See Note 6)	35 V	35 V		
Collector to Base Voltage	35 V	35 V		
Collector to Emitter Voltage (See Note 3)	30 V	30 V		
Emitter to Base Voltage	5 V	5 V		
Output Voltage (See Notes 1 and 4)			30 V	30 V
Continuous Collector Current (See Note 5)	300 mA	300 mA		
Continuous Output Current (See Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (See Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Free-Air Temperature Range	–55°C to +125°C	0°C to 70°C	–55°C to +125°C	0°C to 70°C
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C
Pin Temperature:				
Molded DIP (Soldering, 10 s)		260°C	260°C	260°C
Hermetic DIP (Soldering, 60 s)	300°C	300°C	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual circuits may conduct rated current simultaneously.
6. For the 55450B and 75450B only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP. For the Molded Mini DIP and Hermetic Mini DIP, derate at 6.7 mW/°C above 30°C.

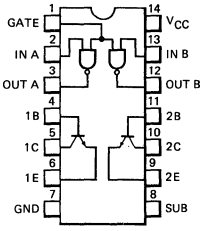
55450B/75450B
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-PIN
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



LOGIC FUNCTION

Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = XY$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
55450B	55450BDM
75450B	75450BDC
75450B	75450BPC

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

TTL Gates

SYMBOL	CHARACTERISTICS		TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNITS
V_{IH}	Input HIGH Voltage		1			2			V
V_{IL}	Input LOW Voltage		2					0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = MIN, I_I = -12 mA				-1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = MIN, V_{IL} = 0.8 V I_{OH} = -400 μA		2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = MIN, V_{IH} = 2 V	55450B		0.22	0.5	V
				I_{OL} = 16 mA	75450B		0.22	0.4	
I_I	Input Current at Maximum Input Voltage	Input A	4	V_{CC} = MAX, V_I = 5.5 V				1	mA
		Input G						2	
I_{IH}	Input HIGH Current	Input A	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Input G						80	
I_{IL}	Input LOW Current	Input A	3	V_{CC} = MAX, V_I = 0.4 V				-1.6	mA
		Input G						-3.2	
I_{OS}	Short Circuit Output Current (Note 9)		5	V_{CC} = MAX		-18		-55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = MAX, V_I = 0 V			2	4	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = MAX, V_I = 5 V			6	11	

NOTES:
8. All typical values at V_{CC} = 5 V, T_A = 25°C.
9. Not more than one output should be shorted at a time.

55450B/75450B

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

Output Transistors

SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP (Note 10)	MAX	UNITS
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0		35			V
$V_{(BR)CER}$	Collector to Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		30			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 11)	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C		25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA	55450B	10			
			75450B	20			
		V_{CE} = 3 V, I_C = 300 mA	55450B	15			
			75450B	25			
$V_{BE(sat)}$	Base to Emitter Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450B		0.85	1.2	V
			75450B		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA	55450B		1.05	1.4	V
			75450B		1.05	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55450B		0.25	0.5	V
			75450B		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA	55450B		0.5	0.8	V
			75450B		0.5	0.7	V

NOTES:
10. All typical values are at V_{CC} = 5 V, T_A = 25°C.
11. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

TTL Gates

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		12	22	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8	15	ns

Output Transistors

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS (Note 12)	MIN	TYP	MAX	UNITS
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = -1 V		8	15	ns
t_r	Rise Time		$I_{B(1)}$ = 20 mA, $I_{B(2)}$ = -40 mA		12	20	ns
t_s	Storage Time		C_L = 15 pF, R_L = 50 Ω		7	15	ns
t_f	Fall Time				6	15	ns

Gates and Transistors Combined

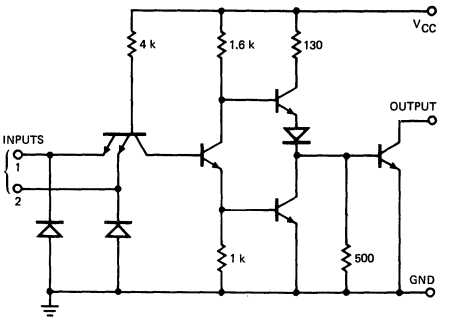
SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		20	30	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				20	30	ns
t_{TLH}	Transition Time, Output LOW to HIGH				7	12	ns
t_{THL}	Transition Time, Output HIGH to LOW				9	15	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, I_C ≈ 300 mA R_{BE} = 500 Ω	V_S -6.5			mV

NOTE 12. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

7

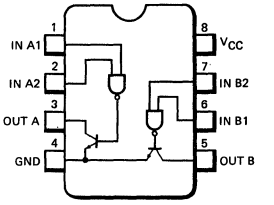
55451B/75451B
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUTS		OUTPUT	
X	Y	Z	
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55451B	55451BRM
75451B	75451BRC
75451B	75451BTC

Positive Logic: Z = XY

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 13)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55451B			300	μA
				75451B			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55451B		0.25	0.5	V
				75451B		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55451B		0.5	0.8	
				75451B		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 5 V			7.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			52	65	mA

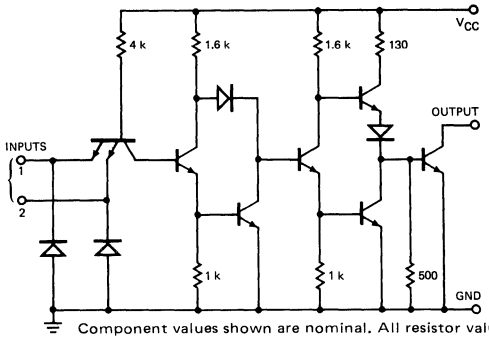
NOTE 13. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		18	25	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				18	25	ns
t_{TLH}	Transition Time, Output LOW to HIGH				5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55452B/75452B
DUAL POSITIVE NAND PERIPHERAL DRIVER

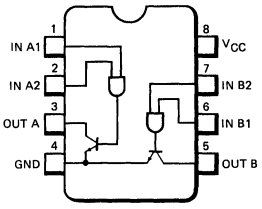
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUTS		OUTPUT	
X	Y	Z	
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55452B	55452BRM
75452B	75452BRC
75452B	75452BTC

Positive Logic: $Z = \overline{XY}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 14)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IL} = 0.8 V	55452B			300	μA
				75452B			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55452B		0.25	0.5	V
				75452B		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55452B		0.5	0.8	
				75452B		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			−1.0	−1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 0 V			11	14	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			56	71	mA

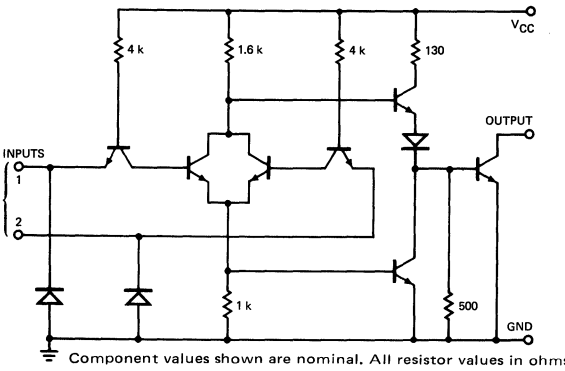
NOTE 14. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		25	35	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				22	35	ns
t_{TLH}	Transition Time, Output LOW to HIGH				5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S −6.5			mV

55453B/75453B
DUAL POSITIVE OR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

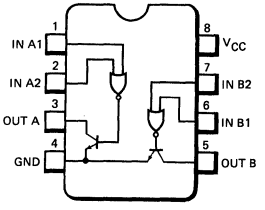
TRUTH TABLE

INPUTS		OUTPUT	
X	Y	Z	
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

CONNECTION DIAGRAMS
8-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
55453B	55453BRM
75453B	75453BRC
75453B	75453BTC

Positive Logic: $Z = X + Y$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 15)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IH} = 2 V	55453B			300	μA
				75453B			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55453B		0.25	0.5	V
				75453B		0.25	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55453B		0.5	0.8	
				75453B		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			54	68	mA

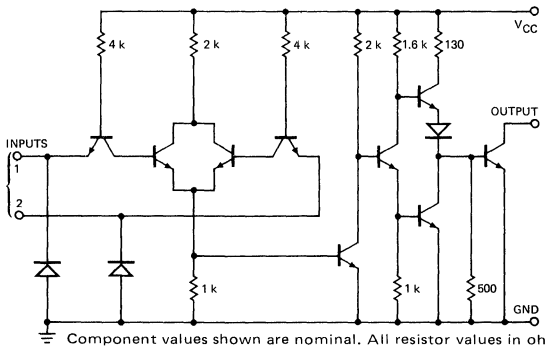
NOTE 15. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		18	25	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				16	25	ns
t_{TLH}	Transition Time, Output LOW to HIGH				5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

55454B/75454B
DUAL POSITIVE NOR PERIPHERAL DRIVER

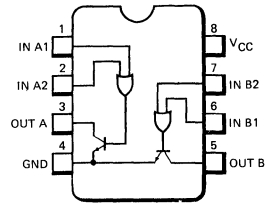
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUTS		OUTPUT	
X	Y	Z	
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55454B	55454BRM
75454B	75454BRC
75454B	75454BTC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 16)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 30 V, V_{IL} = 0.8 V	55454B			300	μA
				75454B			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55454B		0.25	0.5	V
				75454B		0.25	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55454B		0.5	0.8	
				75454B		0.5	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			61	79	mA

NOTE 16. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

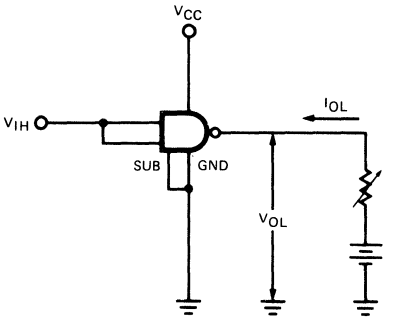
SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		27	35	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				24	35	ns
t_{TLH}	Transition Time, Output LOW to HIGH				5	8	ns
t_{THL}	Transition Time, Output HIGH to LOW				7	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 20 V, $I_O \approx$ 300 mA	V_S -6.5			mV

7

CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUIT†

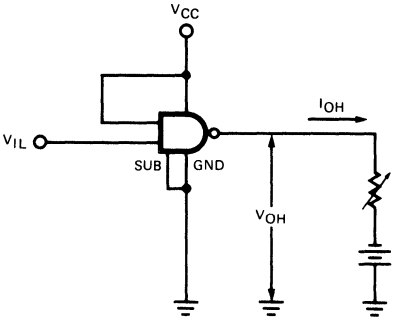
V_{IH}, V_{OL}



Both inputs are tested simultaneously.

Fig. 1

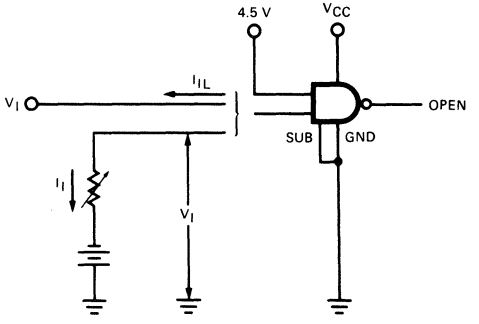
V_{IL}, V_{OH}



Each input is tested separately.

Fig. 2

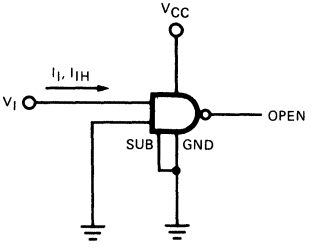
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing V_{CD}, input not under test is open.

Fig. 3

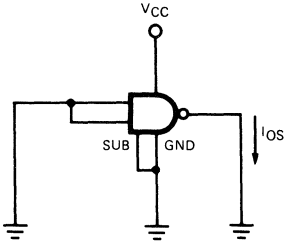
I_I, I_{IH}



Each input is tested separately

Fig. 4

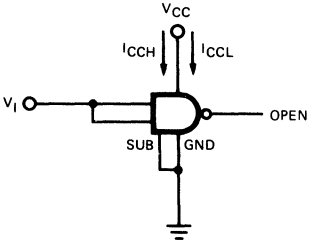
I_{OS}



Each gate is tested separately.
(55450B/75450B only)

Fig. 5

I_{CCH}, I_{CCL}

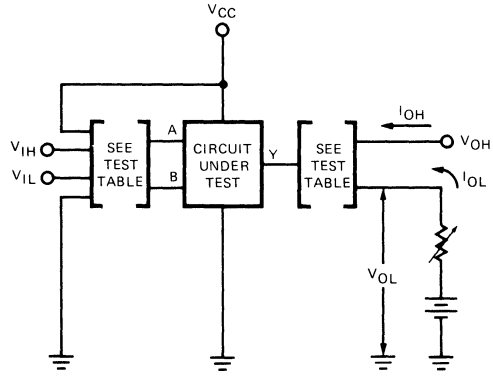


Both gates are tested simultaneously.

Fig. 6

CHARACTERISTICS MEASUREMENT INFORMATION

V_{IH}, V_{IL}, I_{OH}, V_{OL}



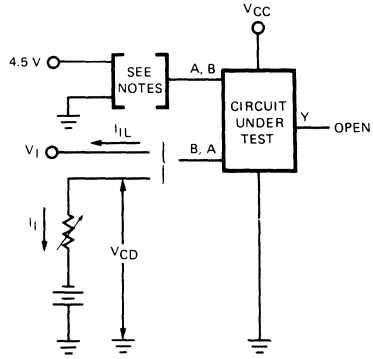
NOTE: Each input is tested separately.

Fig. 7

TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75451B	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75452B	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
55/75453B	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75454B	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

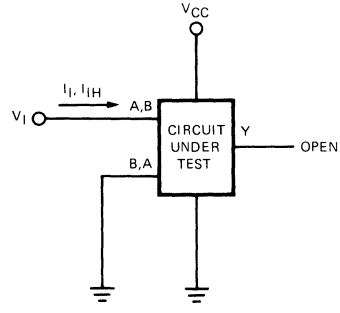
V_{CD}, I_{IL}



NOTES: A. Each input is tested separately.
B. When testing I_{IL} 55/75453B and 55/75454B, the input not under test is grounded. For all other circuits it is at 4.5V.
C. When testing V_{CD}, input not under test is open.

Fig. 8

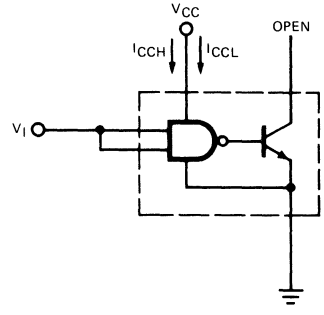
I_I, I_{IH}



Each input is tested separately.

Fig. 9

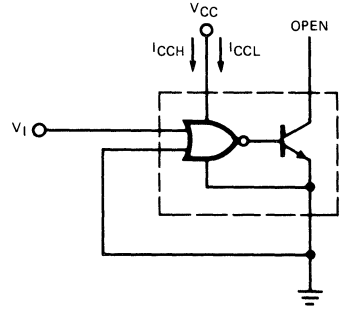
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 10

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

Fig. 11

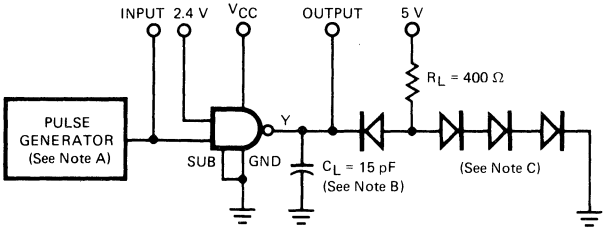
† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

CHARACTERISTICS MEASUREMENT INFORMATION

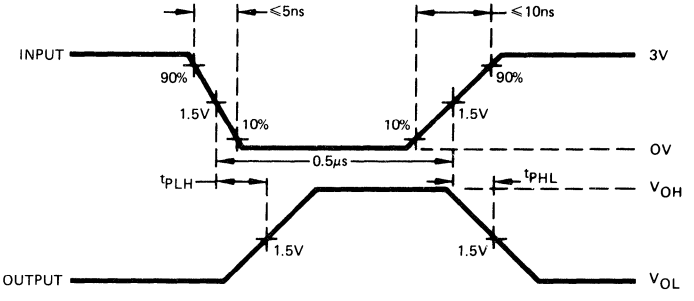
AC CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE (55450B, 75450B ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
B C_L include probe and jig capacitance.
C All diodes are FD777.

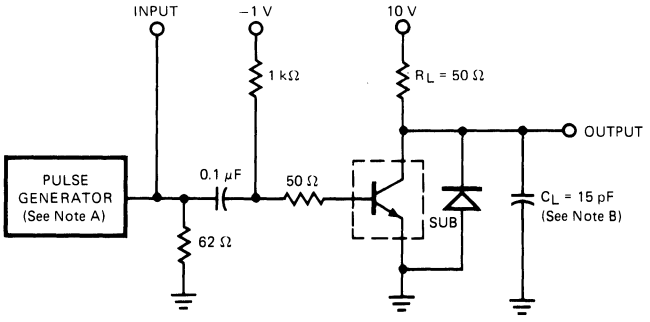
Fig. 12

CHARACTERISTICS MEASUREMENT INFORMATION

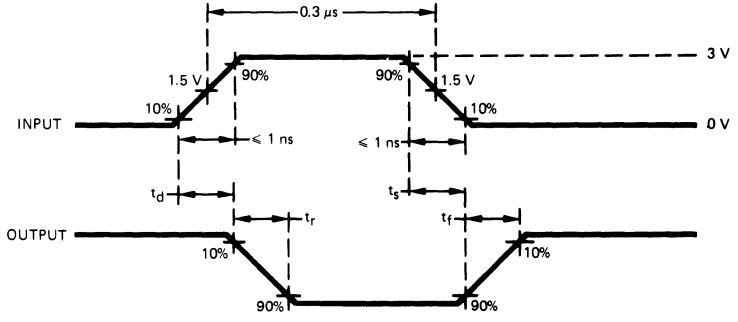
AC CHARACTERISTICS

SWITCHING TIMES, EACH TRANSISTOR (55450B, 75450B ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

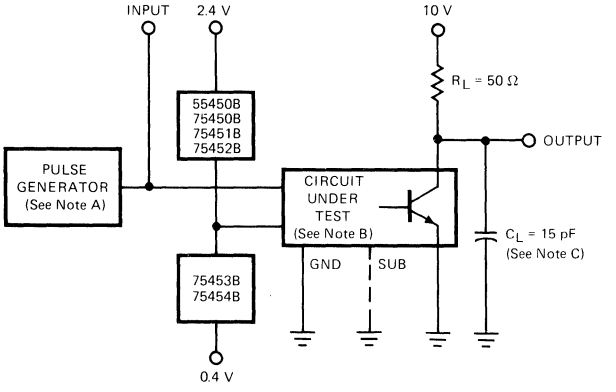
Fig. 13

CHARACTERISTICS MEASUREMENT INFORMATION

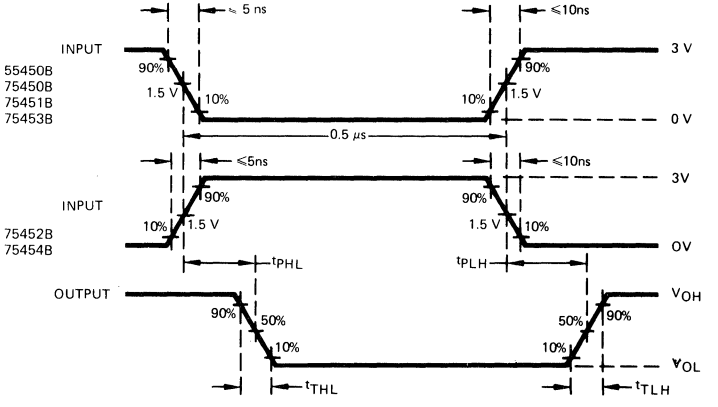
AC CHARACTERISTICS

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:
A. The pulse generator has the following characters : PRR = 1 MHz, $Z_{out} \approx 500\ \Omega$.
B. When testing 55450B/75450B, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

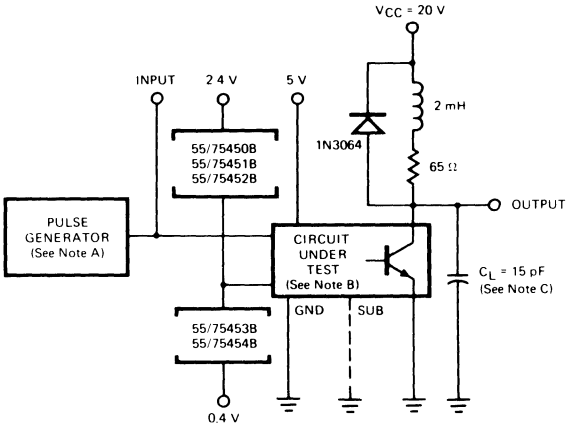
Fig. 14

CHARACTERISTICS MEASUREMENT INFORMATION

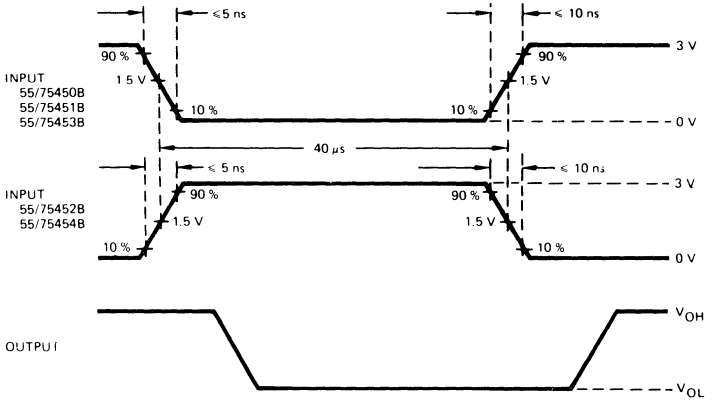
AC CHARACTERISTICS

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

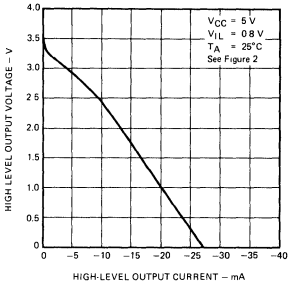


NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing 55450 or 75450, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

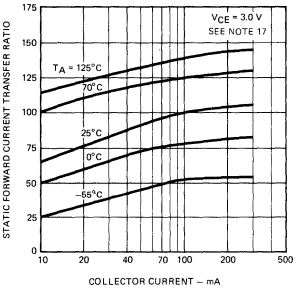
Fig. 15

TYPICAL PERFORMANCE CURVES FOR 75450B SERIES

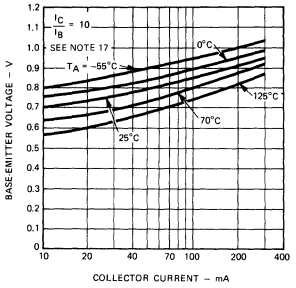
55450B/75450B TTL GATE HIGH-LEVEL OUTPUT VOLTAGE AS A FUNCTION OF HIGH-LEVEL OUTPUT CURRENT



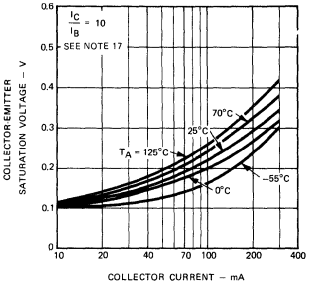
55450B/75450B TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT



55450B/75450B TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



NOTE 17: These parameters must be measured using pulse techniques. t_W = 300 μs, duty cycle ≤ 2%.

55/75460 • 55/75461 • 55/75462
55/75463 • 55/75464
DUAL HIGH VOLTAGE HIGH CURRENT PERIPHERAL DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55/75460 Peripheral Driver Series converts TTL and DTL logic levels to HIGH voltage, HIGH current levels. The 55/75460 Series is directly interchangeable with the 55/75450 Series and affords higher breakdown at the expense of speed. The 55/75460 Series features two 54/74 TTL input gates and two HIGH voltage HIGH current npn uncommitted transistors.

The 55/75461, 55/75462, 55/75463 and 55/75464 feature two standard 54/74 TTL input gates in AND, NAND, OR and NOR configurations, respectively. The logic gates are internally connected to the bases of the npn transistors.

- **NO OUTPUT LATCH-UP AT 30 V**
- **MEDIUM SWITCHING SPEED**
- **300 mA OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

7

TEST TABLE 1 — Operating Temperature Range and Supply Voltage Range

	55460 Series	75460 Series
Temperature, T_A	−55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

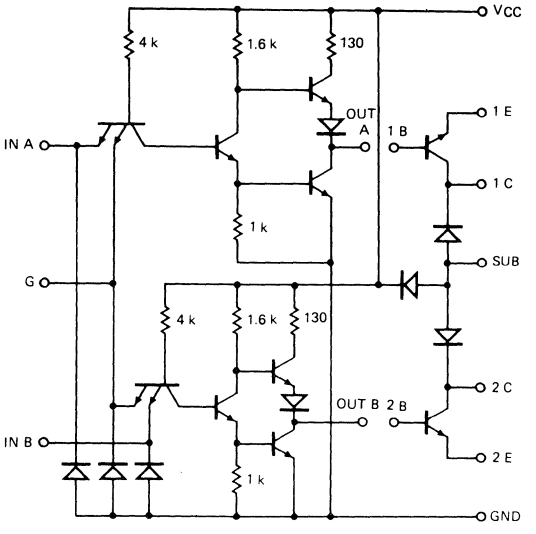
ABSOLUTE MAXIMUM RATINGS

	55460	75460	55461 55462 55463 55464	75461 75462 75463 75464
Supply Voltage, V_{CC} (Note 1)	7 V	7 V	7 V	7 V
Input Voltage (Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage (Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (Note 6)	40 V	40 V		
Collector to Substrate Voltage (Note 6)	40 V	40 V		
Collector to Base Voltage	40 V	40 V		
Collector to Emitter Voltage (Note 3)	40 V	40 V		
Emitter to Base Voltage	5 V	5 V		
Output Voltage (Notes 1 and 4)			35 V	35 V
Continuous Collector Current (Note 5)	300 mA	300 mA		
Continuous Output Current (Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Ambient Temperature Range	−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Pin Temperature				
Molded DIP (Soldering, 10 s)		260°C	260°C	260°C
Hermetic DIP (Soldering, 30 s)	300°C	300°C	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual curcuits may conduct rated current simultaneously.
6. For the 55460 and 75460 only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 70°C ambient temperature, derate linearly at 8.3 mW/°C for hermetic DIP.
   For plastic Mini DIP and hermetic Mini DIP derate above 30°C at 6.7 mW/°C.

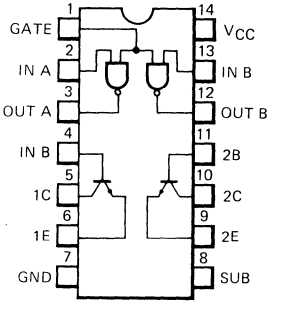
55460/75460
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



LOGIC FUNCTION

Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = \overline{X}\,\overline{Y}$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
55460	55460DM
75460	75460DC
75460	75460PC

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

TTL Gates

SYMBOL	CHARACTERISTICS		TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNITS
V_{IH}	Input HIGH Voltage		1			2			V
V_{IL}	Input LOW Voltage		2					0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = MIN, V_{IL} = 0.8 V I_{OH} = -400 μA		2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = MIN, V_{IH} = 2 V	55460		0.25	0.5	V
				I_{OL} = 16 mA	75460		0.25	0.4	
I_I	Input Current at Maximum Input Voltage	Input A, B	4	V_{CC} = MAX, V_I = 5.5 V				1	mA
		Gate						2	
I_{IH}	Input HIGH Current	Input A, B	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Gate						80	
I_{IL}	Input LOW Current	Input A, B	3	V_{CC} = MAX, V_I = 0.4 V				-1.6	mA
		Gate						-3.2	
I_{OS}	Short Circuit Output Current (Note 9)		5	V_{CC} = MAX		-18	-35	-55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = MAX, V_I = 0 V			2.8	4	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = MAX, V_I = 5 V			7	11	

NOTES:
8. All typical values at V_{CC} = 5 V, T_A = 25°C.
9. Not more than one output should be shorted at a time.

55460/75460

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

Output Transistors

SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP (Note 10)	MAX	UNITS
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0		40			V
$V_{(BR)CER}$	Collector to Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		40			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 11)	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C		25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA	55460 T_A=−55°C	10			
			75460 T_A=0°C	20			
		V_{CE} = 3 V, I_C = 300 mA	55460 T_A=−55°C	15			
			75460 T_A=0°C	25			
$V_{BE(sat)}$	Base to Emitter Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55460		0.85	1.2	V
			75460		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA	55460		1.0	1.4	V
			75460		1.0	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55460		0.25	0.5	V
			75460		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA	55460		0.45	0.8	V
			75460		0.45	0.7	V

NOTES:
10. All typical values are at V_{CC} = 5 V, T_A = 25°C.
11. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

TTL Gates

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		22		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8		ns

Output Transistors

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS (Note 12)	MIN	TYP	MAX	UNITS
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = −1 V		10		ns
t_r	Rise Time		$I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA		16		ns
t_s	Storage Time		C_L = 15 pF, R_L = 50 Ω		23		ns
t_f	Fall Time				14		ns

Gates and Transistors Combined

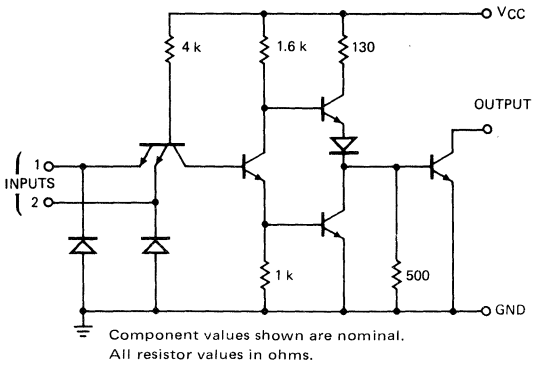
SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		45	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				35	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				10	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_C \approx$ 300 mA R_{BE} = 500 Ω	V_S −10			mV

NOTE 12. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

7

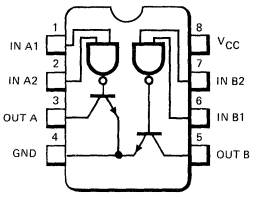
55461/75461
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUT		OUTPUT
1	2	
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55461	55461RM
75461	75461RC
75461	75461TC

Positive Logic: $Z = XY$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 13)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IH} = 2 V	55461			300	μA
				75461			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55461		.16	0.5	V
				75461		.16	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55461		.35	0.8	
				75461		.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			61	76	mA

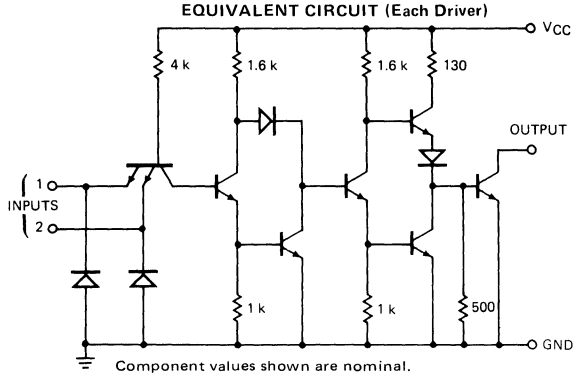
NOTE 13. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

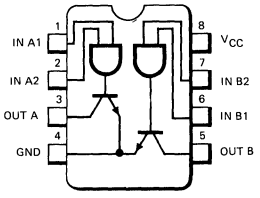
55462/75462
DUAL POSITIVE NAND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55462	7562RM
75462	75462RC
75462	75462TC

Positive Logic: $Z = \overline{XY}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 14)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IL} = 0.8 V	55462			300	μA
				75462			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55462		.16	0.5	V
				75462		.16	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55462		.35	0.8	
				75462		.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			65	76	mA

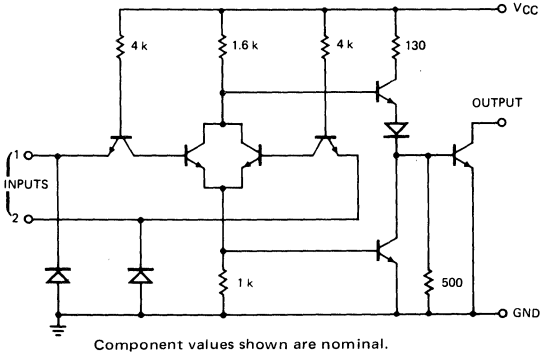
NOTE 14. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25° C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				40	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

55463/75463
DUAL POSITIVE OR PERIPHERAL DRIVER

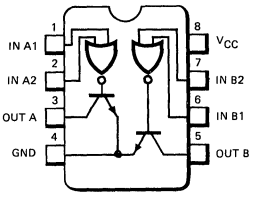
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAM

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off'state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55463	55463RM
75463	75463RC
75463	75463TC

Positive Logic: $Z = X + Y$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 15)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IH} = 2 V	55463			300	μA
				75463			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55463		0.18	0.5	V
				75463		0.18	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55463		0.39	0.8	
				75463		0.39	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current Output HIGH	11	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			63	76	mA

NOTE 15. All typical values are at V_{CC} = 5 V, T_A = 25°C.

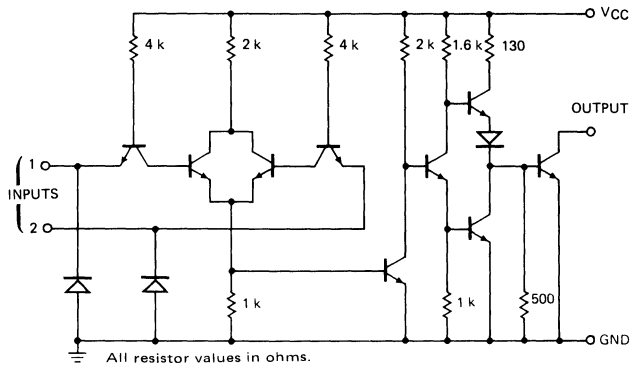
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	25	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

55464/75464

DUAL POSITIVE NOR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



All resistor values in ohms.

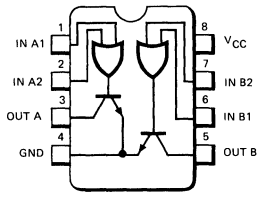
CONNECTION DIAGRAM

8-PIN DIP

(TOP VIEW)

PACKAGE OUTLINE 9T 6T

PACKAGE CODE T R



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55464	55464RM
75464	75464RC
75464	75464TC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 16)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IL} = 0.8 V	55464			300	μA
				75464			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55464		0.17	0.5	V
				75464		0.17	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55464		0.38	0.8	
				75464		0.38	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 0 V			14	19	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			72	85	mA

NOTE 16. All typical values are at V_{CC} = 5 V, T_A = 25°C.

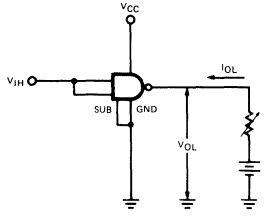
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				40	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUIT†

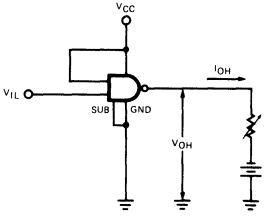
V_{IH}, V_{OL}



Both inputs are tested simultaneously.

Fig. 1

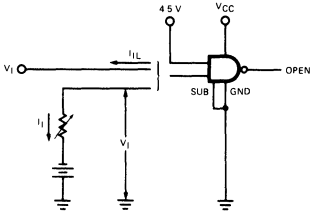
V_{IL}, V_{OH}



Each input is tested separately.

Fig. 2

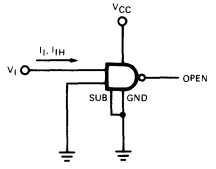
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing V_{CD}, input not under test is open.

Fig. 3

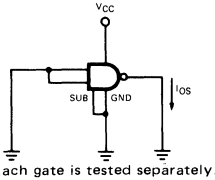
I_I, I_{IH}



Each input is tested separately

Fig. 4

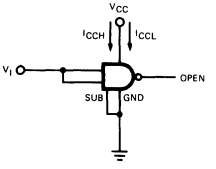
I_{OS}



Each gate is tested separately.
(55460/75460 only)

Fig. 5

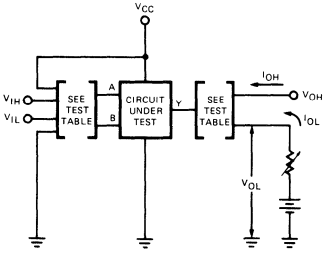
I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

Fig. 6

V_{IH}, V_{IL}, I_{OH}, V_{OL}



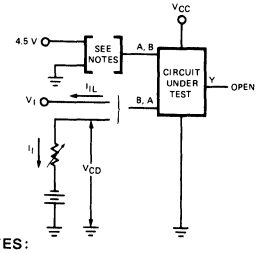
NOTE: Each input is tested separately.

Fig. 7

TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75461	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75462	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
55/75463	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75464	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

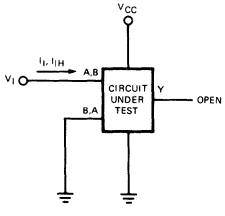
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing I_{IL} 55/75463 and 55/75464, the input not under test is grounded. For all other circuits it is at 4.5V.
C. When testing V_{CD}, input not under test is open.

Fig. 8

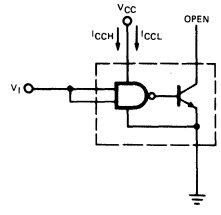
I_I, I_{IH}



Each input is tested separately.

Fig. 9

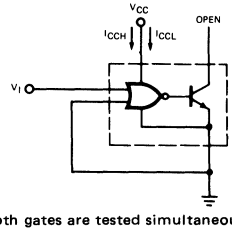
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 10

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

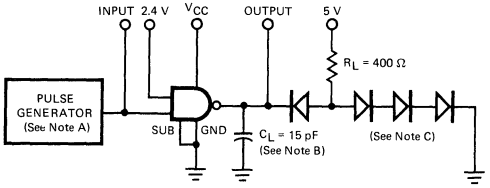
Fig. 11

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

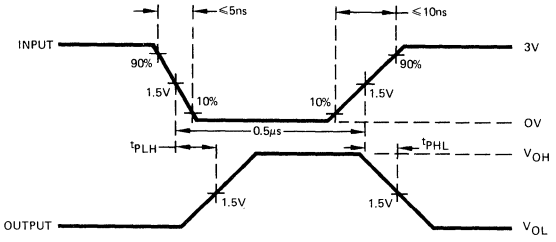
CHARACTERISTICS MEASUREMENT INFORMATION
SWITCHING CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE
(55460, 75460 ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



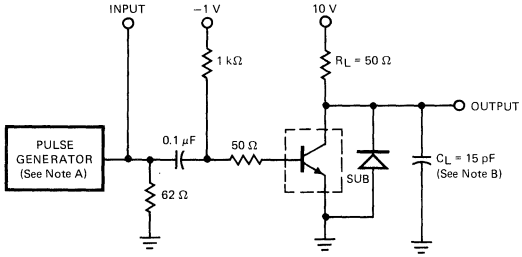
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are FD777.

Fig. 12

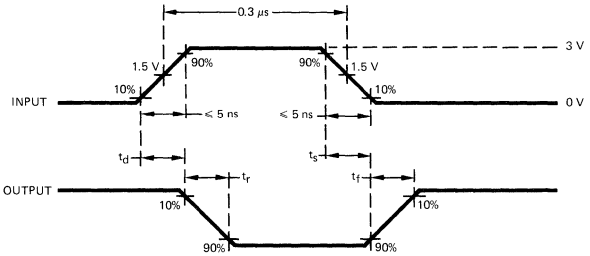
7

SWITCHING TIMES, EACH TRANSISTOR
(55460, 75460 ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS

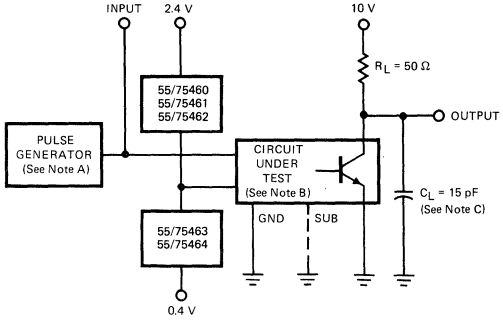


NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

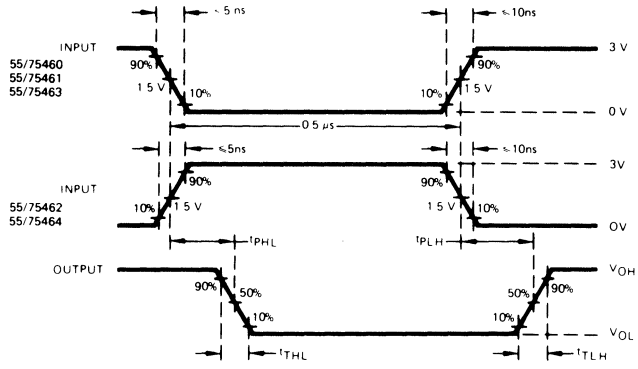
Fig. 13

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

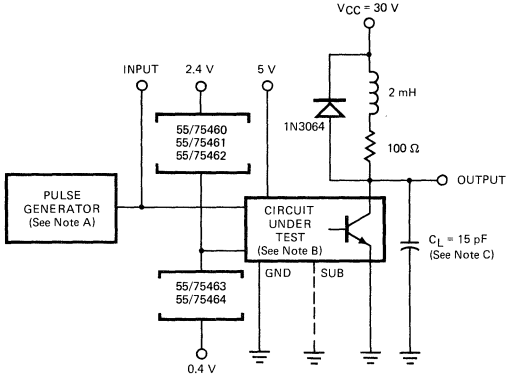


NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing 55460/75460, connect output Y to transistor base and ground the substrate terminal
C. C_L includes probe and jig capacitance.

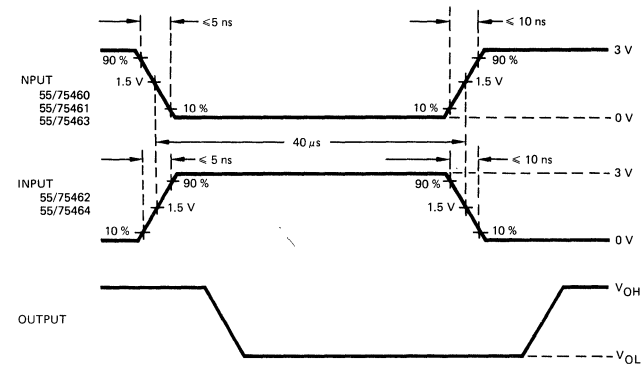
Fig. 14

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

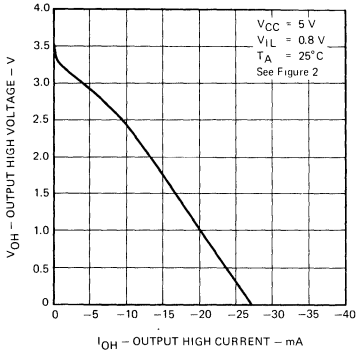


NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing 55460 or 75460, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

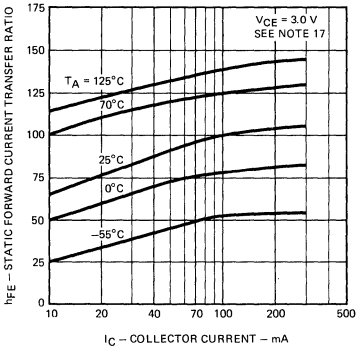
Fig. 15

TYPICAL PERFORMANCE CURVES FOR 55460/75460 SERIES

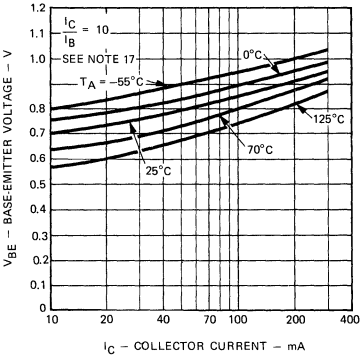
55460/75460 TTL GATE OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



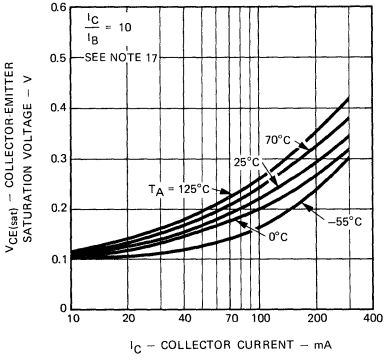
55460/75460 TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT



55460/75460 TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



NOTE 17. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

55/75471 • 55/75472 • 55/75473 • 55/75474

DUAL HIGH VOLTAGE HIGH CURRENT PERIPHERAL DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55/75471 series are dual very high voltage interface peripheral drivers with medium switching speeds. These devices are pin-for-pin replacements of the (55/75451A-55/75454A), (55/75461-55/75464) and the (DS3611-DS3614) peripheral drivers.

The 55/75471 peripheral driver series converts TTL and DTL logic levels to high voltage, high current levels.

The 55/75471, 55/75472, 55/75473 and 55/75474 feature two standard TTL input gates in AND, NAND, OR and NOR configurations respectively. The logic gates are internally connected to the bases of the npn transistors.

The 55/75471 series offers flexibility in designing very high voltage logic buffers, power drivers, lamp drivers, line drivers and relay drivers.

- **HIGH VOLTAGE OUTPUT (80 V)**
- **NO LATCH-UP AT 55 V**
- **HIGH SPEED SWITCHING**
- **HIGH OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

TEST TABLE 1 — Operating Temperature Range and Supply Voltage Range

	55471 Series	75471 Series
Temperature, T_A	−55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

ABSOLUTE MAXIMUM RATINGS

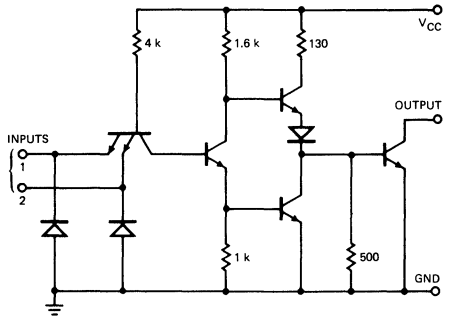
	55471 55472 55473 55474	75471 74572 75473 75474
Supply Voltage, V_{CC} (See Note 1)	7.0 V	7.0 V
Input Voltage (See Note 1)	5.5 V	5.5 V
Interemitter Voltage (See Note 2)	5.5 V	5.5 V
Output Voltage (See Notes 1 and 3)	80 V	80 V
Continuous Collector Current (See Note 4)		
Continuous Output Current (See Note 4)	300 mA	300 mA
Continuous Total Power Dissipation (See Note 5)	800 mW	800 mW
Operating Free-Air Temperature Range	−55°C to +125°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Pin Temperature		
Molded DIP (Soldering, 10 s)	260°C	260°C
Hermetic DIP (Soldering, 60 s)	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.
4. Both halves of these dual circuits may conduct rated current simultaneously.
5. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C for Hermetic DIP and Molded DIP. For the Molded Mini DIP and Hermetic Mini DIP, derate at 6.7 mW/°C above 30°C.

55471/75471

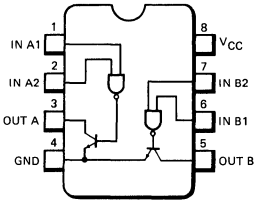
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	L	(on state)
H	L	L	(on state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55471	55471RM
75471	75471RC
75471	75471TC

Positive Logic: Z = XY

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 6)	MAX	UNITS
V_{IH}	Input HIGH Voltage	1			2.0			V
V_{IL}	Input LOW Voltage	1					0.8	V
V_{CD}	Input Clamp Diode Voltage	2	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	1	V_{CC} = MIN, V_{OH} = 80 V, V_{IH} = 2 V	55471			300	μA
				75471			100	
V_{OL}	Output LOW Voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55471		0.16	0.5	V
				75471		0.16	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55471		0.35	0.8	
				75471		0.35	0.7	
I_I	Input Current at Maximum Input Voltage	3	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	2	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	4	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			61	76	mA

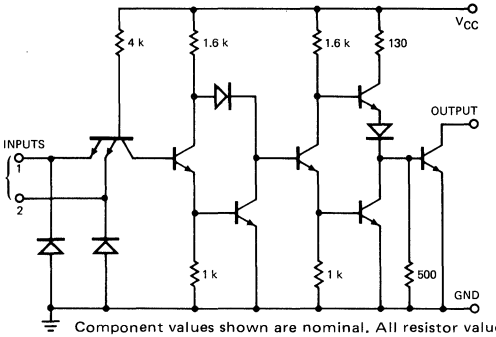
NOTE 6. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	6	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		30	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8.0	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	7	V_S = 55 V, $I_O \approx$ 300 mA	V_S -18			mV

55472/75472
DUAL POSITIVE NAND PERIPHERAL DRIVER

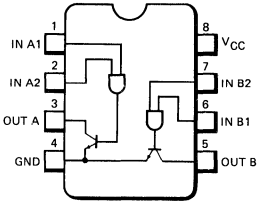
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55472	55472RM
75472	75472RC
75472	75472TC

Positive Logic: $Z = \overline{XY}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 7)	MAX	UNITS
V_{IH}	Input HIGH Voltage	1			2.0			V
V_{IL}	Input LOW Voltage	1					0.8	V
V_{CD}	Input Clamp Diode Voltage	2	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	1	V_{CC} = MIN, V_{OH} = 80 V, V_{IL} = 0.8 V	55472			300	μA
				75472			100	
V_{OL}	Output LOW Voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55472		0.16	0.5	V
				75472		0.16	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55472		0.35	0.8	
				75472		0.35	0.7	
I_I	Input Current at Maximum Input Voltage	3	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	2	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	4	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			65	76	mA

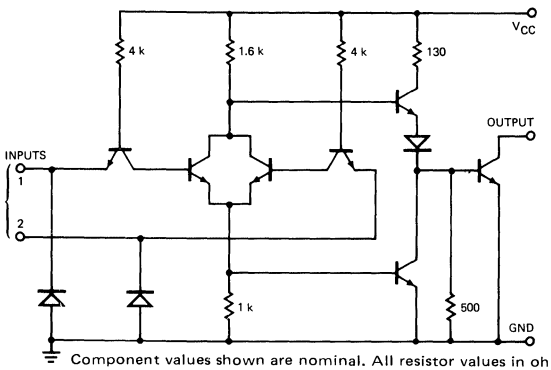
NOTE 7. All typical values are at V_{CC} = 5 V, T_A = 25°C

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	6	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				13	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	7	V_{SS} = 55 V, $I_O \approx$ 300 mA	V_S -18			mV

55473/75473
DUAL POSITIVE OR PERIPHERAL DRIVER

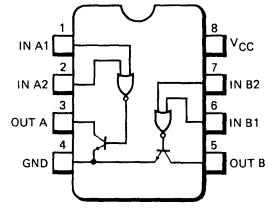
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



ORDER INFORMATION

TYPE	PART NO.
55473	55473RM
75473	75473RC
75473	75473TC

Positive Logic: $Z = X + Y$

TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNITS
V_{IH}	Input HIGH Voltage	1			2.0			V
V_{IL}	Input LOW Voltage	1					0.8	V
V_{CD}	Input Clamp Diode Voltage	2	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	1	V_{CC} = MIN, V_{OH} = 80 V, V_{IH} = 2 V	55473			300	µA
				75473			100	
V_{OL}	Output LOW Voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55473		0.18	0.5	V
				75473		0.18	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55473		0.39	0.8	
				75473		0.39	0.7	
I_I	Input Current at Maximum Input Voltage	3	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	3	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Input LOW Current	2	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	5	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			63	76	mA

NOTE 8. All typical values are at V_{CC} = 5 V, T_A = 25°V

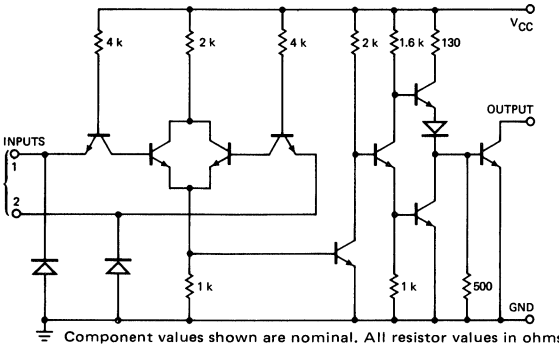
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	6	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		30	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				25	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	25	ns
V_{OH}	HIGH Level Output Voltage After Switching	7	V_S = 55 V, $I_O \approx$ 300 mA	V_S -18			mV

55474/75474

DUAL POSITIVE NOR PERIPHERAL DRIVER

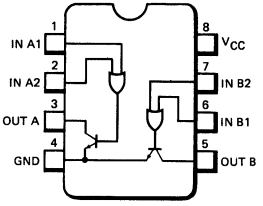
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal. All resistor values in ohms.

CONNECTION DIAGRAMS

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUTS		OUTPUT	
1	2		
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55474	55474RM
75474	75474RC
75474	75474TC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 9)	MAX	UNITS
V_{IH}	Input HIGH Voltage	1			2.0			V
V_{IL}	Input LOW Voltage	1					0.8	V
V_{CD}	Input Clamp Diode Voltage	2	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	Output HIGH Current	1	V_{CC} = MIN, V_{OH} = 80 V, V_{IL} = 0.8 V	55474			300	μA
				75474			100	
V_{OL}	Output LOW Voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55474		0.17	0.5	V
				75474		0.17	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55474		0.38	0.8	
				75474		0.38	0.7	
I_I	Input Current at Maximum Input Voltage	3	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	2	V_{CC} = MAX, V_I = 0.4 V			−1.0	−1.6	mA
I_{CCH}	Supply Current, Output HIGH	5	V_{CC} = MAX, V_I = 0 V			14	19	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			72	85	mA

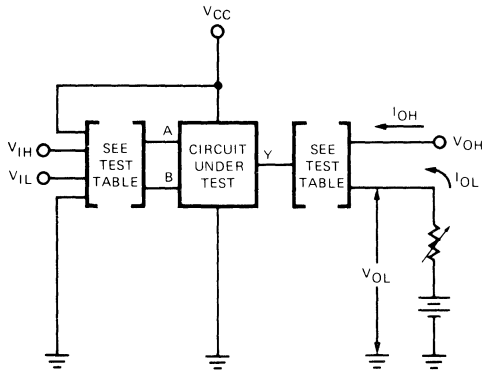
NOTE 9. All typical values are at V_{CC} = 5 V, T_A = 25°C

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	6	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		40	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	7	V_S = 55 V, $I_O \approx$ 300 mA	V_S −18			mV

CHARACTERISTICS MEASUREMENT INFORMATION

V_{IH}, V_{IL}, I_{OH}, V_{OL}



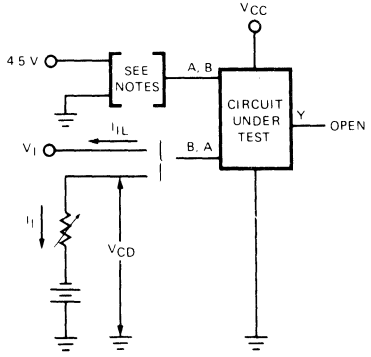
TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75471	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75472	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
55/75473	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75474	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

NOTE: Each input is tested separately.

Fig. 1

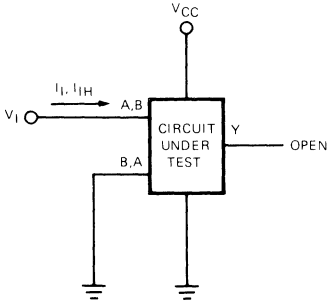
V_{CD}, I_{IL}



NOTES: A. Each input is tested separately.
B. When testing I_{IL} 55/75473 and 55/75474, the input not under test is grounded. For all other circuits it is at 4.5 V.
C. When testing V_{CD}, input not under test is open.

Fig. 2

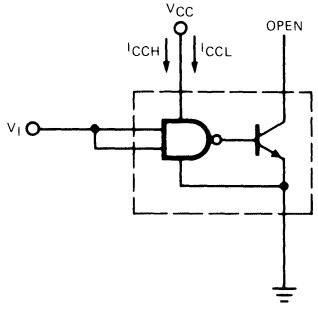
I_I, I_{IH}



Each input is tested separately.

Fig. 3

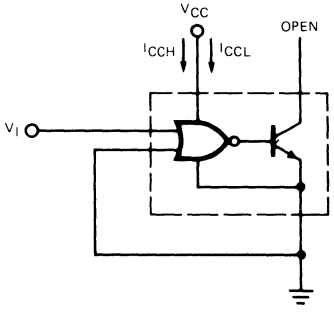
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 4

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

Fig. 5

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

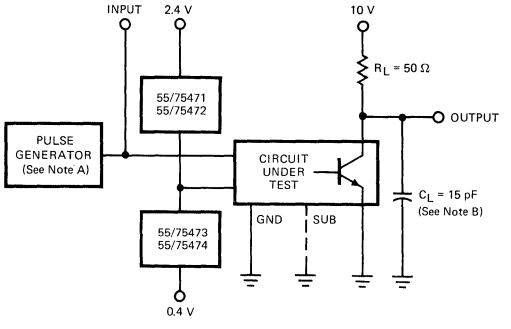
7

CHARACTERISTICS MEASUREMENT INFORMATION

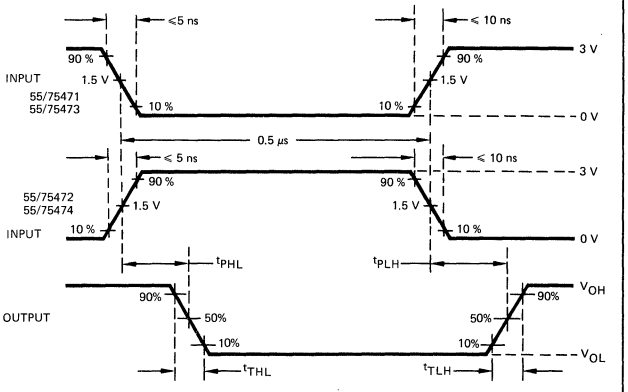
AC CHARACTERISTICS

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



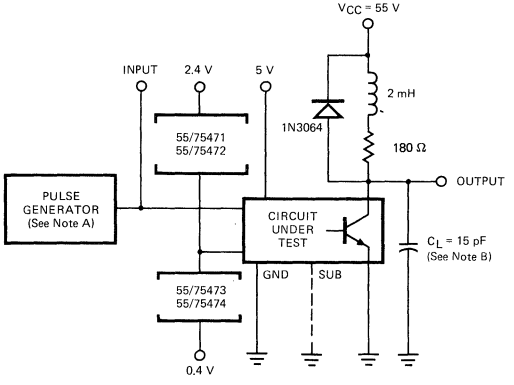
VOLTAGE WAVEFORMS



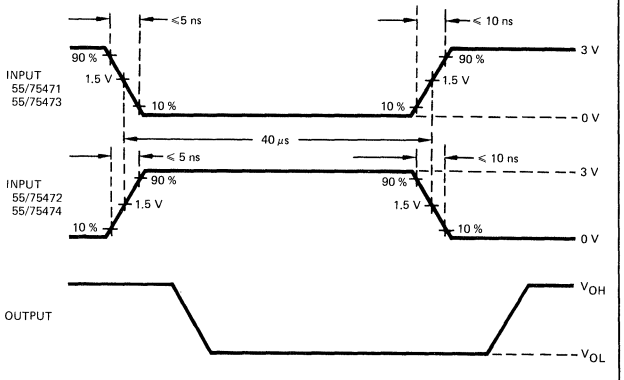
NOTES:
A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 500\ \Omega$.
B. C_L includes probe and jig capacitance.

Fig. 6

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

Fig. 7

9665 • 9666 • 9667 • 9668

HIGH VOLTAGE, HIGH CURRENT DARLINGTON DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 9665, 9666, 9667 and 9668 are comprised of seven high voltage, high current npn Darlington transistor pairs. All units feature common emitter, open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads and appropriate emitter-base resistors for leakage.

The 9665 is a general purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. Input current limiting is done by connecting an appropriate discrete resistor to each input.

The 9666 version does away with the need for any external discrete resistors, since each unit has a resistor and a Zener diode in series with the input. The 9666 was specifically designed for direct interface from PMOS logic (operating at supply voltages from 14 to 25 V) to solenoids or relays.

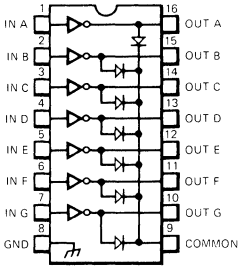
The 9667 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V.

The 9668 has an appropriate input resistor to allow direct operation from CMOS or PMOS outputs operating from supply voltages of 6 to 15 V.

9665, 9666, 9667 and 9668 offer solutions to a great many interface needs, including solenoids, relays, lamps, small motors and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

- **SEVEN HIGH GAIN DARLINGTON TRANSISTOR PAIRS**
- **HIGH OUTPUT VOLTAGE (V_{CE} = 50 V)**
- **HIGH OUTPUT CURRENT (I_C = 350 mA)**
- **DTL, TTL, PMOS, CMOS COMPATIBLE**
- **SUPPRESSION DIODES FOR INDUCTIVE LOADS**
- **2 WATT PLASTIC DIP PACKAGE ON COPPER PIN FRAME**

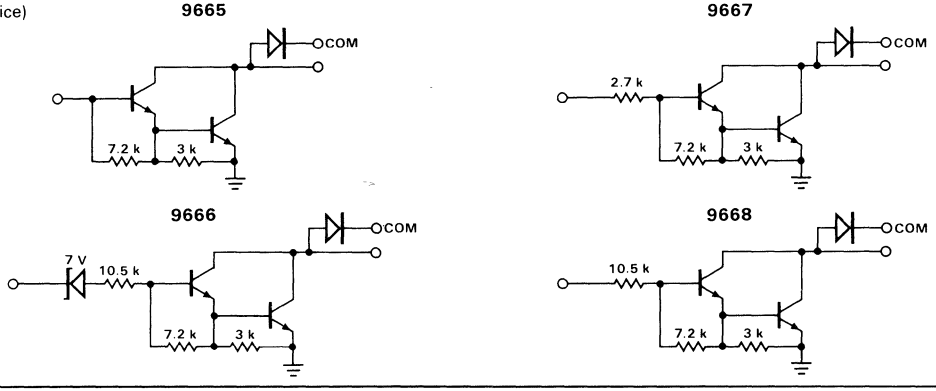
CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6B, 9B
PACKAGE CODE D, P



ORDER INFORMATION

TYPE	PART NO.
9665	9665DC
9665	9665PC
9666	9666DC
9666	9666PC
9667	9667DC
9667	9667PC
9668	9668DC
9668	9668PC

EQUIVALENT CIRCUIT
(Each Device)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Output Voltage, V_{CE}	55 V
Input Voltage, V_{IN}	30 V
Emitter-Base Voltage, V_{EBO}	6 V
Continuous Collector Current, I_C	500 mA
Continuous Base Current, I_B	25 mA
Power Dissipation (6B, Kovar lead frame)	1.0 W
Power Dissipation (9B, Copper lead frame)*	2.0 W
Pin Temperature (Molded DIP, Soldering, 10 s)	260°C
(Hermetic DIP, Soldering, 60 s)	300°C
Ambient Temperature Range (operating), T_A	0°C to +85°C
Storage Temperature Range, T_S	−65°C to +150°C

*Under normal operating conditions, these units will sustain 350 mA per output with $V_{CE(sat)}$ = 1.6 V at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

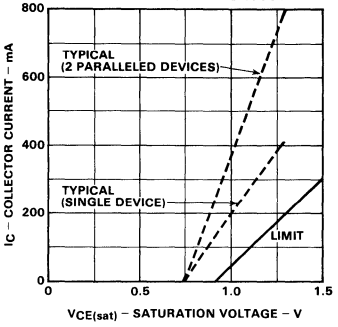
ELECTRICAL CHARACTERISTICS: T_A = 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	TEST FIGURE	TEST CONDITIONS (Note 1)	MIN	TYP	MAX	UNITS
I_{CEX}	Output Leakage Current	1a	V_{CE} = 50 V, T_A = 70°C			100	μA
		1b	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6 V (9666)			500	μA
		1b	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1 V (9668)			500	μA
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	2	I_C = 350 mA, I_B = 500 μA		1.25	1.6	V
		2	I_C = 200 mA, I_B = 350 μA		1.1	1.3	V
		2	I_C = 100 mA, I_B = 250 μA		0.9	1.1	V
$I_{IN(ON)}$	Input Current	3	V_{IN} = 17 V (9666)		0.85	1.3	mA
		3	V_{IN} = 3.85 V (9667)		0.93	1.35	mA
		3	V_{IN} = 5 V (9668)		0.35	0.5	mA
		3	V_{IN} = 12 V (9668)		1.0	1.45	mA
$I_{IN(OFF)}$	Input Current (Note 2)	4	I_C = 500 μA, T_A = 70°C	50	65		μA
$V_{IN(ON)}$	Input Voltage (Note 3)	5	V_{CE} = 2 V, I_C = 300 mA (9666)			13	V
		5	V_{CE} = 2 V, I_C = 200 mA (9667)			2.4	V
		5	V_{CE} = 2 V, I_C = 250 mA (9667)			2.7	V
		5	V_{CE} = 2 V, I_C = 300 mA (9667)			3.0	V
		5	V_{CE} = 2 V, I_C = 125 mA (9668)			5.0	V
		5	V_{CE} = 2 V, I_C = 200 mA (9668)			6.0	V
		5	V_{CE} = 2 V, I_C = 275 mA (9668)			7.0	V
		5	V_{CE} = 2 V, I_C = 350 mA (9668)			8.0	V
h_{FE}	DC Forward Current Transfer Ratio	2	V_{CE} = 2 V, I_C = 350 mA (9665)	1000			
C_{IN}	Input Capacitance				15	30	pF
t_{PLH}	Turn-On Delay		0.5 V_{IN} to 0.5 V_{OUT}			1	μs
t_{PHL}	Turn-Off Delay		0.5 V_{IN} to 0.5 V_{OUT}			1	μs
I_R	Clamp Diode Leakage Current	6	V_R = 50 V			50	μA
V_F	Clamp Diode Forward Voltage	7	I_F = 350 mA		1.7	2.0	V

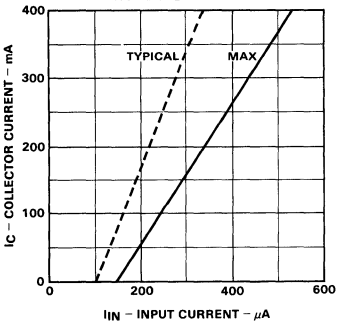
NOTES:
1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guaranteed against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TYPICAL ELECTRICAL PERFORMANCE

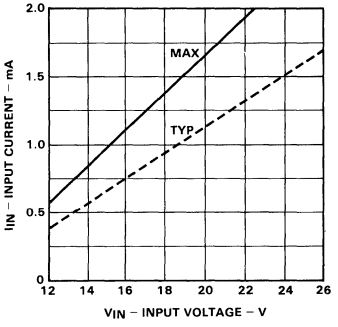
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



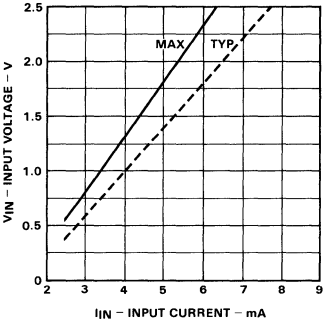
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



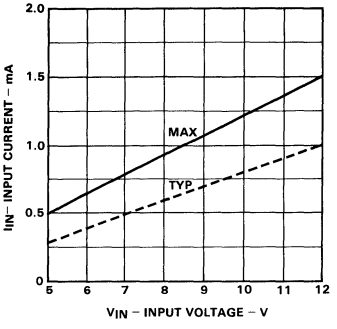
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE 9666



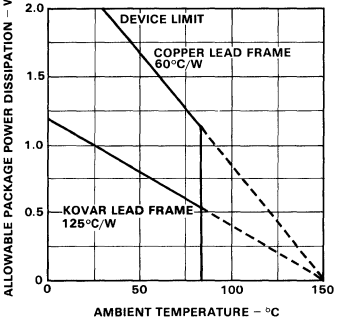
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE 9667



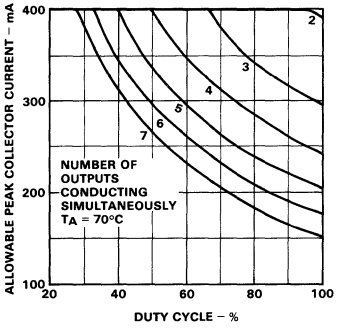
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE 9668



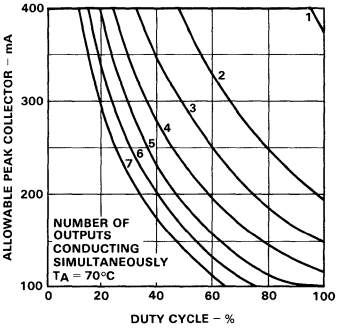
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS (PLASTIC PACKAGE)



PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS (CERAMIC PACKAGE)



7

TEST CIRCUITS

Fig. 1a

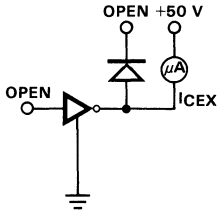


Fig. 1b

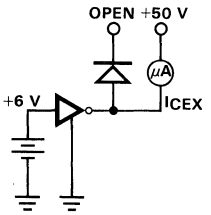


Fig. 2

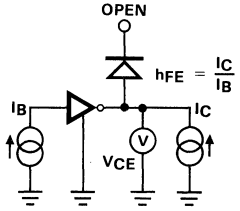


Fig. 3

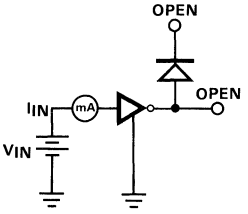


Fig. 4

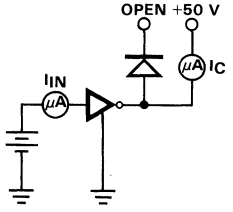


Fig. 5

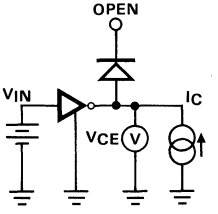


Fig. 6

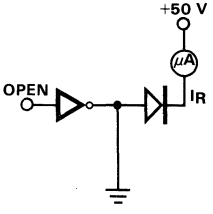
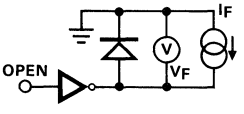
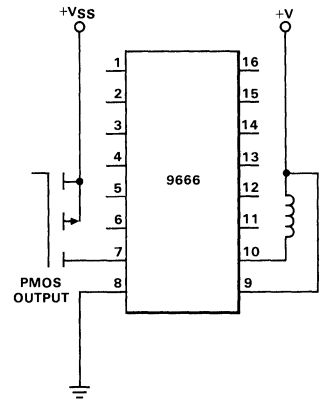


Fig. 7

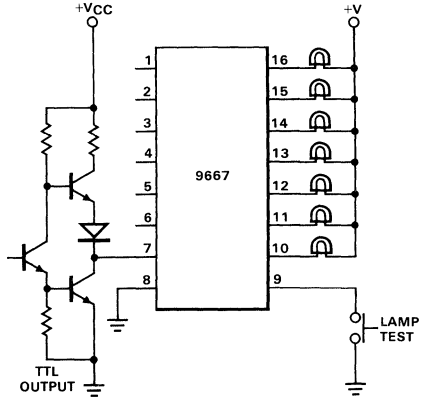


TYPICAL APPLICATIONS

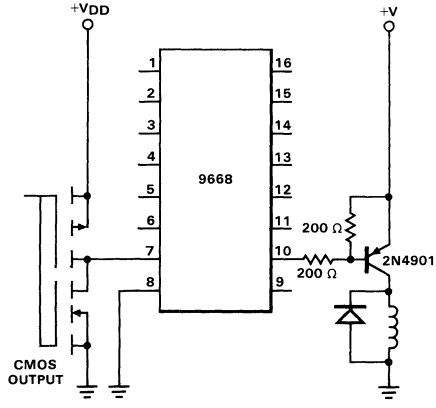
PMOS TO LOAD



TTL TO LOAD



BUFFER FOR HIGHER CURRENT LOADS



55/75491 • 55/75491A
55/75492 • 55/75492A
MOS TO LED SEGMENT AND DIGIT DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION—The 55/75491 and 55/75491A, LED Quad Segment Digit Drivers interface MOS signals to common cathode LED displays. High output current capability makes the devices ideal in time multiplex systems using segment address or digit scan method of driving LEDs to minimize the number of drivers required.

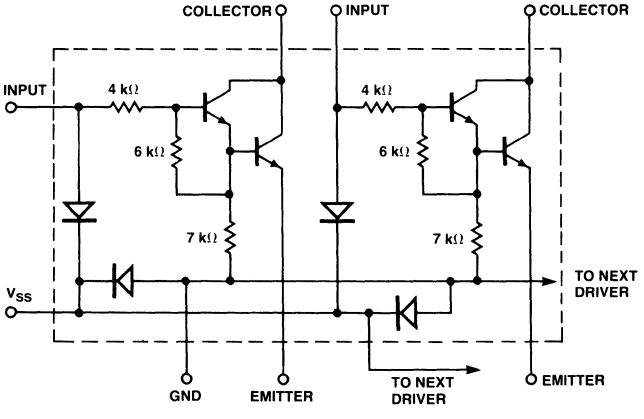
The 55/75492 and 55/75492A, Hex LED/Lamp Drivers convert MOS signals to high output currents for LED display digit select or lamp select. The high output current capability makes the devices ideal in time multiplex systems using segment address or digit scan method of driving LEDs to minimize the number of drivers required.

55/75491 • 55/75491A
- **50 mA SOURCE OR SINK CAPABILITY**
- **LOW INPUT CURRENTS FOR MOS COMPATIBILITY**
- **LOW STANDBY POWER**
- **FOUR HIGH GAIN DARLINGTON CIRCUITS**
- **10 V and 20 V OPERATION**

55/75492 • 55/75492A
- **250 mA SINK CAPABILITY**
- **MOS COMPATIBLE INPUTS**
- **LOW STANDBY POWER**
- **SIX HIGH GAIN DARLINGTON CIRCUITS**
- **10 V and 20 V**

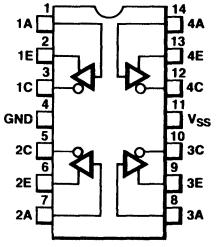
EQUIVALENT CIRCUITS

1/2 OF 75491/75491A



CONNECTION DIAGRAMS
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P

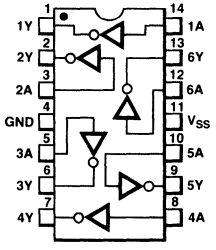
55/75491 • 55/75491A



ORDER INFORMATION

TYPE	PART NO.
55491	55491DM
75491	75491DC
75491	75491PC
55491A	55491ADM
75491A	75491ADC
75491A	75491APC

55/75492 • 55/75492A

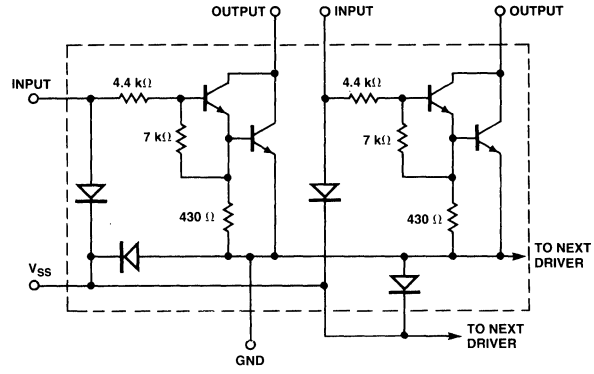


ORDER INFORMATION

TYPE	PART NO.
55492	55492DM
75492	75492DC
75492	75492PC
55492A	55492ADM
75492	75492ADC
75492A	75492APC

EQUIVALENT CIRCUIT

1/3 OF 75492/75492A



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 55/75491, 55/75492	10 V
55/75491A, 55/75492A	20 V
Input Voltage (Note 1)	−5.0 to V_{SS}
Collector (Output) Voltage (Note 2) 55/75491, 55/75492	10 V
55/75491A, 55/75492A	20 V
Collector (Output) to Input Voltage 55/75491, 55/75492	10 V
55/75491A, 55/75492A	20 V
Emitter to Ground Voltage ($V_{IN} \geq$ 5.0 V) 55/75491	10 V
55/75491A	20 V
Emitter to Input Voltage 55/75491, 55/75491A	5.0 V
Continuous Collector Current 55/75491, 55/75491A	50 mA
55/75492, 55/75492A	250 mA
Collector Output Current (75492 and 75492A only) all collectors	600 mA
Continuous Total Power Dissipation (Note 3)	800 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

NOTES:
1. The input is the only device terminal which may be negative with respect to ground.
2. Voltage values are with respect to network ground terminal unless otherwise noted.
3. Above 60°C ambient temperature, derate linearly at 8.3 mW/°C.

55/75491 • 55/75491A
TRUTH TABLE

INPUT	OUTPUT E	OUTPUT C
L	L	H
H	H	L

55/75492 • 55/75492A
TRUTH TABLE

INPUT	OUTPUT
L	H
H	L

55491 • 55491A

ELECTRICAL CHARACTERISTICS: V_{SS} = 10 V for 55491, V_{SS} = 20 V for 55491A, T_A = −55°C to +125°C unless otherwise specified.

SYMBOL	CHARACTERISTICS	CONDITION		MIN	TYP	MAX	UNITS
V_{CEL}	LOW Level Collector to Emitter Voltage	V_{IN} = 8.5 V through 1.0 kΩ I_{OL} = 50 mA, V_E = 5.0 V, T_A = 25°C			0.9	1.2	V
		V_{IN} = 8.5 V through 1.0 kΩ I_{OL} = 50 mA, V_E = 5.0 V			0.9	2.0	V
I_{CH}	Collector HIGH Current	V_{CH} = 10 V, 55491 V_{CH} = 20 V, 55491A	V_E = 0, V_{IN} = 0.7 V			250	μA
		V_{CH} = 10 V, 55491 V_{CH} = 20 V, 55491A	V_E = 0, I_{IN} = 40 μA			250	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10 V, 55491 V_{IN} = 20 V, 55491A	I_{OL} = 20 mA		2.0 4.0	4.0 8.0	mA
I_{ER}	Reverse Biased Emitter Current	I_C = 0, V_{IN} = 0, V_E = 5.0 V				100	μA
I_{SS}	Supply Current					1.0	mA

75491 • 75491A

ELECTRICAL CHARACTERISTICS: V_{SS} = 10 V for 75491, V_{SS} = 20 V for 75491A, T_A = 0°C to 70°C unless otherwise specified.

SYMBOL	CHARACTERISTICS	CONDITION		MIN	TYP	MAX	UNITS
V_{CEL}	LOW Level Collector to Emitter Voltage	V_{IN} = 8.5 V through 1.0 kΩ I_{OL} = 50 mA, V_E = 5.0 V, T_A = 25°C			0.9	1.2	V
		V_{IN} = 8.5 V through 1.0 kΩ I_{OL} = 50 mA, V_E = 5.0 V			0.9	1.5	V
I_{CH}	Collector HIGH Current	V_{CH} = 10 V, 75491 V_{CH} = 20 V, 75491A	V_E = 0, V_{IN} = 0.7 V			100	μA
		V_{CH} = 10 V, 75491 V_{CH} = 20 V, 75491A	V_E = 0, I_{IN} = 40 μA			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10 V, 75491 V_{IN} = 20 V, 75491A	I_{OL} = 20 mA		2.0 4.0	3.3 6.6	mA
I_{ER}	Reverse Biased Emitter Current	I_C = 0, V_{IN} = 0, V_E = 5.0 V				100	μA
I_{SS}	Supply Current					1.0	mA

AC CHARACTERISTIC: V_{SS} = 7.5 V, T_A = 25°C.

SYMBOL	CHARACTERISTICS	CONDITION	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time	R_L = 200 Ω, V_{INH} = 4.5 V		20		ns
t_{PLH}		C_L = 15 pF, V_E = 0		100		ns

55492 • 55492A

ELECTRICAL CHARACTERISTICS: V_{SS} = 10 V for 55492, V_{SS} = 20 V for 55492A, T_A = −55°C to +125°C unless otherwise specified.

SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output LOW Voltage	V_{IN} = 6.5 V through 0.1 kΩ I_{OL} = 250 mA, T_A = 25°C			0.9	1.2	V
		V_{IN} = 6.5 V through 1.0 kΩ I_{OL} = 250 mA			0.9	2.0	V
I_{OH}	Output HIGH Current	V_{OH} = 10 V, 55492	I_{IN} = 40 μA			500	μA
		V_{OH} = 20 V, 55492A					
		V_{OH} = 10 V, 55492	V_{IN} = 0.5 V			500	μA
		V_{OH} = 20 V, 55492A					
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10 V, 55492	I_{OL} = 20 mA		2.0	4.0	mA
		V_{IN} = 20 V, 55492A			4.0	8.0	
I_{SS}	Supply Current					1.0	mA

75492 • 75492A

ELECTRICAL CHARACTERISTICS: V_{SS} = 10 V for 75492, V_{SS} = 20 V for 75492A, T_A = 0°C to 70°C unless otherwise specified.

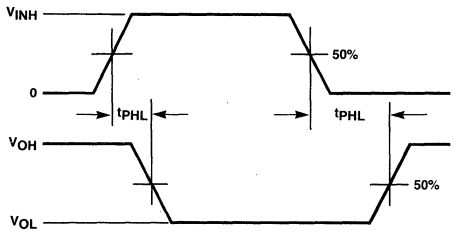
SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output LOW Voltage	V_{IN} = 6.5 V through 1.0 kΩ I_{OL} = 250 mA, T_A = 25°C			0.9	1.2	V
		V_{IN} = 6.5 V through 1.0 kΩ I_{OL} = 250 mA			0.9	1.5	V
I_{OH}	Output HIGH Current	V_{OH} = 10 V, 75492	I_{IN} = 40 μA			200	μA
		V_{OH} = 20 V, 75492A					
		V_{OH} = 10 V, 75492	V_{IN} = 0.5 V			200	μA
		V_{OH} = 20 V, 75492A					
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10 V, 75492	I_{OL} = 20 mA		2.0	3.3	mA
		V_{IN} = 20 V, 75492A			4.0	6.6	
I_{SS}	Supply Current					1.0	mA

AC CHARACTERISTICS: V_{SS} = 7.5 V, T_A = 25°C.

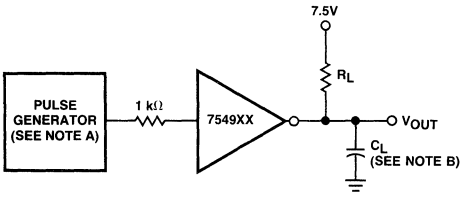
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time	R_L = 39 Ω, V_{IN} = 7.5 V		30		ns
t_{PLH}		C_L = 15 pF		300		ns

NOTE: All typical values are at T_A = 25°C

WAVEFORMS



TEST CIRCUIT

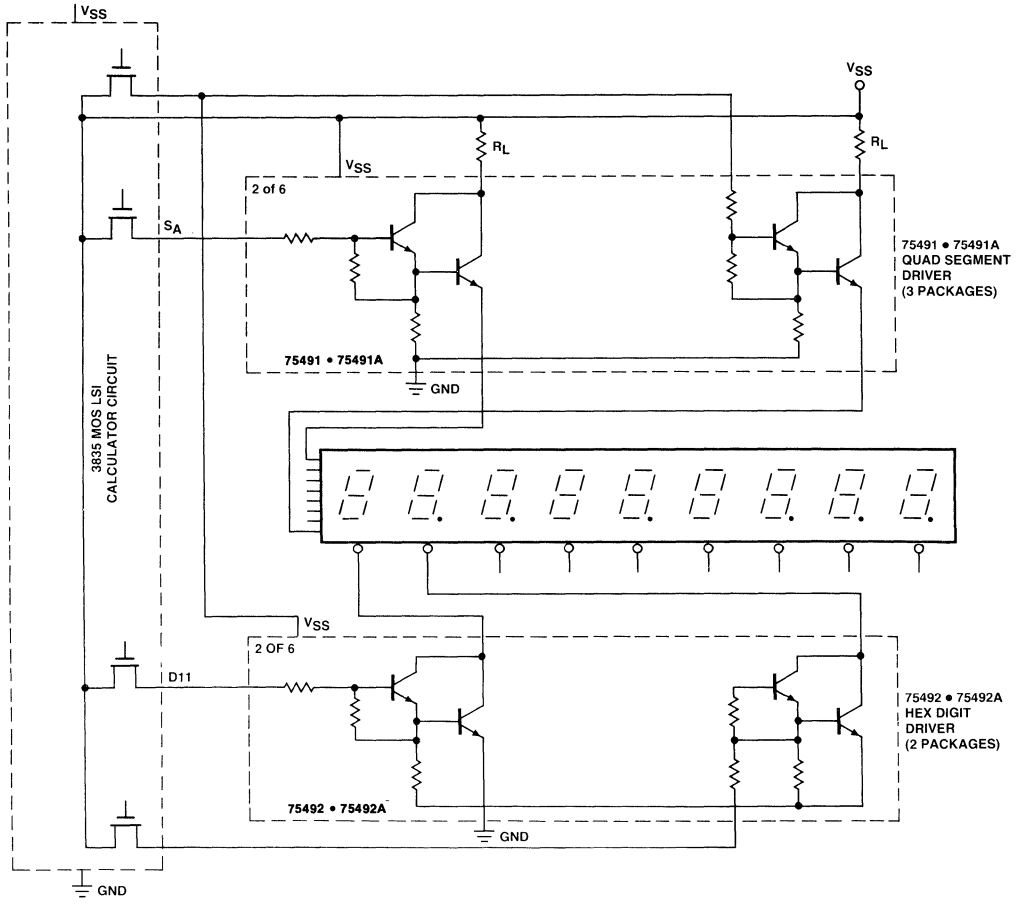


NOTES:

A. The pulse generator has the following characteristics: Z_{OUT} = 50 Ω, PRR = 100 kHz, t_w = 1 μs.

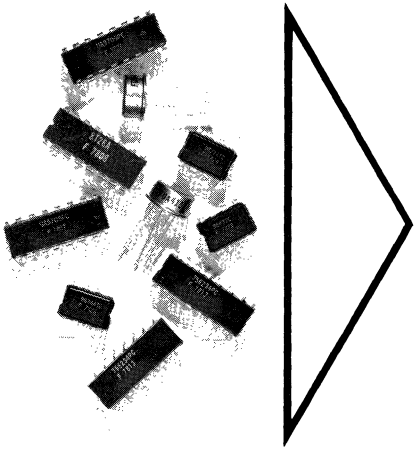
B. C_L includes probe and jig capacitance.

TYPICAL APPLICATION



INTERFACING BETWEEN MOS CALCULATOR CIRCUIT AND LED MULTI-DIGIT DISPLAY

This example of time multiplexing the individual digits in a visible display minimizes display circuitry. Up to twelve digits of a 7-segment display plus decimal point may be displayed using only two 75491/A and two 75492/A drivers.



MEMORY INTERFACE

9624•9625
DUAL TTL, MOS INTERFACE ELEMENT
FAIRCHILD LINEAR INTEGRATED CIRCUIT

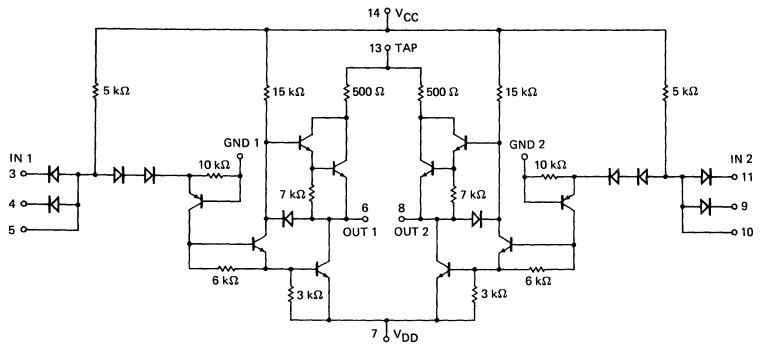
GENERAL DESCRIPTION — The 9624 is a Dual 2-Input TTL Compatible Interface Gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

The 9625 is a dual MOS to TTL level converter. It is designed to convert standard negative MOS logic levels to TTL levels. The 9625 features a high input impedance which allows preservation of the driving MOS logic level.

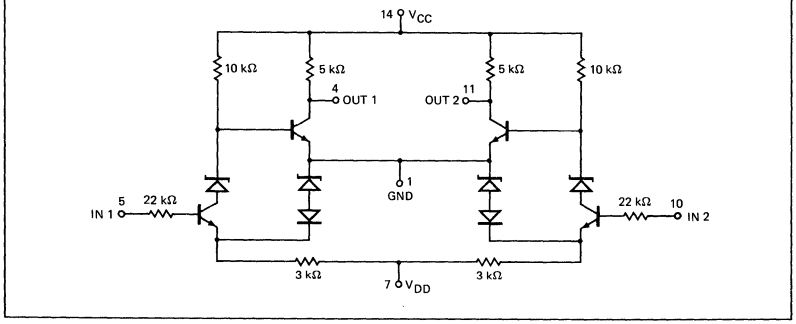
NOTE: The TTL and MOS devices manufactured by Fairchild Semiconductor are considered as positive TRUE logic (the more positive voltage level is assigned the binary state of "1" or TRUE). Following MIL-STD-806B logic symbol specifications, the 9624 is represented as a NAND gate and the 9625 as a non-inverting buffer. This convention (of assuming MOS as a positive TRUE logic) has not been uniformly accepted by the industry; therefore, it is necessary to note that with negative TRUE MOS logic (the more negative voltage level is assigned the binary state "1" or TRUE), the 9624 acts as an AND gate and the 9625 as an inverter.

- **TTL COMPATIBLE INPUTS/OUTPUT**
- **MOS COMPATIBLE OUTPUT/INPUTS**
- **LOW POWER**

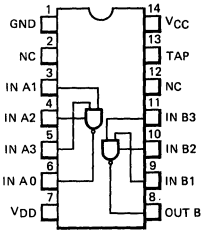
9624 EQUIVALENT CIRCUIT



9625 EQUIVALENT CIRCUIT



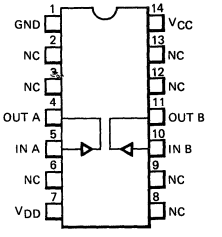
CONNECTION DIAGRAMS
9624
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
9624	9624DM
9624C	9624DC
9624C	9624PC

9625
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
9625	9625DM
9625C	9625DC
9625C	9625PC

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	V_{DD} to +10 V
Voltage Applied to Outputs for HIGH Output State (9624)	V_{DD} to +V_{CC} value
Voltage Applied to Outputs for HIGH Output State (9625)	−0.5 V to V_{CC} value
Input Voltage (dc) (9624)	−0.5 V to +5.5 V
Input Voltage (dc) (9625)	V_{CC} to V_{DD}
V_{DD} Pin Potential to Ground Pin	−30 V to +0.5 V
V_{DD} Pin Potential to Tap Pin (9624)	−30 V to +0.5 V
V_{TAP}	V_{CC} +0.5 V
Internal Power Dissipation (Note 3)	670 mW
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C
Operating Temperature Range	
Military (9624 and 9625)	−55°C to +125°C
Commercial (9624C and 9625C)	0°C to +70°C

9624

ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V ± 10%.

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH1}	Output HIGH Voltage	−1.0		−1.0	−0.5		−1.0		V	V_{CC} = 4.5 V, V_{DD} = −28 V, V_{TAP} = 0 V, I_{OH} = −10 μA
V_{OH2}	Output HIGH Voltage	+3.5		+3.5	+4.0		+3.5		V	V_{CC} = 5.5 V, V_{DD} = −20 V, V_{TAP} = 5.5 V, Inputs at V_{IL}, I_{OH} = −10 μA
V_{OL}	Output LOW Voltage (Note 1)								V	V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{DD} = −15 to 28 V @ V_{IH}, 0 ≤ V_{TAP} ≤ V_{CC} (Note 2)
V_{IH}	Input HIGH Voltage	2.1		1.9			1.7		V	Guaranteed Input HIGH Threshold for all Inputs
V_{IL}	Input LOW Voltage		1.4			1.1		0.8	V	Guaranteed Input LOW Threshold for all Inputs
I_F	Input Load Current		−1.40			−1.25		−1.13	mA	V_{CC} = 5.5 V, V_F = 0.4 V, V_{DD} = −11 to −28 V
I_R	Input Leakage Current		2.0			2.0		5.0	μA	V_{CC} = 5.5 V, V_R = 4.0 V, V_{DD} = −11 to −28 V
I_{CEX}	Output Leakage Current					50			μA	V_{CC} = 5.5 V, V_{TAP} = 0 V, V_{DD} = −28 V, V_{OUT} = 0 V
I_{SC}	Output Short Circut Current	−12	−31	−14		−32	−11	−28	mA	V_{CC} = 4.5 V, V_{TAP} = 0 V, V_{IN} = 0 V, V_{DD} = −11 V, V_{OUT} = −11 V
I_{VCC}	V_{CC} Supply Current					6.1			mA	V_{CC} = 5.5 V, V_{DD} = −15 V, V_{TAP} = 0 V, Inputs Open
I_{MAX}	Max, Current					10			mA	V_{CC} = 10 V, V_{DD} = −30 V, V_{TAP} = 0 V, Inputs Open
t_{PLH}	Propagation Delay				190	250			ns	V_{CC} = 5.0 V, See Figure 1
t_{PHL}	Propagation Delay				50	100			ns	V_{DD} = −13 V, V_{TAP} = 0 V

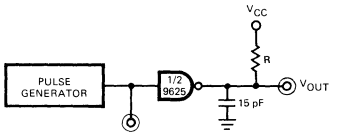
9625

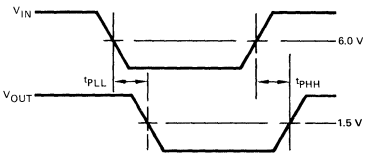
ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V ± 10%.

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN	MAX	MIN	TYP	MAX	MIN MAX		
V_{OH}	Output HIGH Voltage	2.5		2.6			2.5	V	V_{CC} = 4.5 V, I_{OH} = −60 μA, V_{DD} = −11 V, Inputs at V_{IH}
V_{OL}	Output LOW Voltage		0.5			0.5	0.5	V	V_{CC} = 5.5 V, I_{OL} = 1.5 mA V_{CC} = 4.5 V, I_{OL} = 1.2 mA V_{DD} = −11 V, Inputs at V_{IL}
V_{IH}	Input HIGH Voltage		−3.0			−3.0	−3.0	V	Guaranteed Input HIGH Threshold for all Inputs
V_{IL}	Input LOW Voltage	−9.0		−9.0			−9.0	V	Guaranteed Input LOW Threshold for all Inputs
I_F	Input Load Current		210			210	210	μA	V_{CC} = 5.0 V, V_F = −3.0 V, V_{DD} = −13 V
I_{CEX}	Output Leakage Current					50		μA	V_{CC} = V_{CEX} = 4.5 V, V_{DD} = −13 V
I_{VCCL}	Supply Current					4.8		mA	V_{CC} = 5.5 V, V_{DD} = −15 V, V_{IN} = −10 V
I_{VCCH}	Supply Current					2.1		mA	V_{CC} = 5.5 V, V_{DD} = −15 V, V_{IN} = 0 V
I_{VDD}	V_{DD} Supply Current					−9.0		mA	V_{CC} = 5.5 V, V_{DD} = −15 V, Input Open or GND
I_{MAX}	Max, V_{DD} Supply Current					−25		mA	V_{CC} = 8.0 V, V_{DD} = −20 V, V_{IN} = 0 V
t_{PLH}	Propagation Delay				55	100		ns	V_{CC} = 5.0 V, V_{DD} = −13 V
t_{PHL}	Propagation Delay				90	150		ns	See Figure 2

8

9625 AC TEST CIRCUIT AND WAVEFORMS





Rep Rate = 500 kHz
Amplitude = −10 V
Pulse Width = 1.0 μs
t_r, t_f = 20 ns

TESTS	CONDITIONS			
	T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	R (kΩ)
t_{PLL}, t_{PHH}	25	5.0	−13	3.75

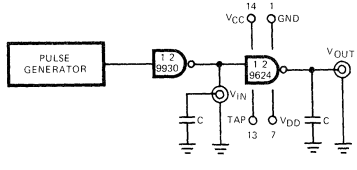
Fig. 2

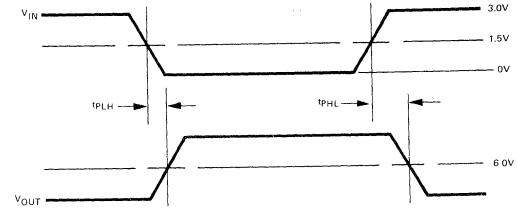
9624C

ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V ± 5%.

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		0°C		+25°C			+70°C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH1}	Output HIGH Voltage	−1.0		−1.0	−0.5		−1.0		V	V_{CC} = 4.75 V, V_{DD} = −28 V, V_{TAP} = 0 V, I_{OH} = −10 μA
V_{OH2}	Output HIGH Voltage	+3.25		+3.25	+3.75		+3.25		V	V_{CC} = 5.25 V, V_{DD} = −20 V, V_{TAP} = 5.25 V, Inputs at V_{IL}, I_{OH} = −10 μA
V_{OL}	Output LOW Voltage (Note 1)								V	V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{DD} = −11 to −28 V @ $0 \leq V_{TAP} \leq V_{CC}$ (Note 2)
V_{IH}	Input HIGH Voltage	2.0		1.9			1.8		V	Guaranteed Input HIGH Threshold for all Inputs
V_{IL}	Input LOW Voltage		1.2			1.1		0.95	V	Guaranteed Input LOW Threshold for all Inputs
I_F	Input Load Current		−1.32			−1.25		−1.20	mA	V_{CC} = 5.25 V, V_F = 0.45 V
I_R	Input Leakage Current		5.0			5.0		10	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = 5.25 V, V_{TAP} = 0 V, V_{DD} = −28 V, V_{OUT} = 0 V
I_{SC}	Output Short-Circuit Current	−12	−31	−14		−32	−12	−31	mA	V_{CC} = 4.75 V, V_{TAP} = 0 V, V_{IN} = 0 V, V_{DD} = −11 V, V_{OUT} = −11 V
I_{VCC}	V_{CC} Supply Current					6.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{TAP} = 0 V, Inputs Open
I_{MAX}	Max, Current					10			mA	V_{CC} = 8.0 V, V_{DD} = −30 V, V_{TAP} = 0 V, Inputs Open
t_{PLH}	Propagation Delay				190	250			ns	V_{CC} = 5.0 V, See Figure 1
t_{PHL}	Propagation Delay				50	100			ns	V_{DD} = −13 V, V_{TAP} = 0 V

9624 AC TEST CIRCUIT AND WAVEFORMS





Rep Rate = 500 kHz
Amplitude = 3 V
Pulse Width = 1 μs
t_r, $t_f \leq$ 10 ns
C = 15 pF

TESTS	CONDITIONS			
	T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	Tap Voltage
t_{PLH},t_{PHL}	25	5.0	−13	0

Fig. 1

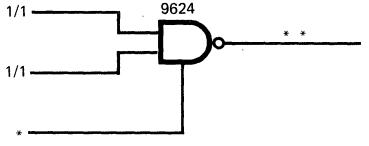
9625C

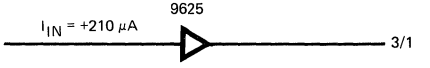
ELECTRICAL CHARACTERISTICS: V_{CC} = 5.0 V ± 5%.

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		0°C		+25°C			+70°C		
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	Output HIGH Voltage	2.5		2.6			2.5		V	V_{CC} = 4.75 V, I_{OH} = −60 μA, V_{DD} = −11 V, Inputs at V_{IH}
V_{OL}	Output LOW Voltage		0.5			0.5		0.5	V	V_{CC} = 5.25 V, I_{OL} = 1.52 mA V_{CC} = 4.75 V, I_{OL} = 1.33 mA Inputs at V_{IL}
V_{IH}	Input HIGH Voltage		−3.0			−3.0		−3.0	V	Guaranteed Input HIGH Threshold for all Inputs
V_{IL}	Input LOW Voltage	−9.0		−9.0			−9.0		V	Guaranteed Input LOW Threshold for all Inputs
I_F	Input Load Current		210			210		210	μA	V_{CC} = 5.0 V, V_F = −3.0 V, V_{DD} = −13 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 4.75 V, V_{DD} = −13 V
I_{VCCL}	Supply Current					4.8			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = −10 V
I_{VCCH}	Supply Current					2.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = 0 V
I_{VDD}	V_{DD} Supply Current					−9.0			mA	V_{CC} = 5.5 V, V_{DD} = −15 V, Input Open or GND
I_{MAX}	Max, V_{DD} Supply Current					−25			mA	V_{CC} = 8.0 V, V_{DD} = −20 V, V_{IN} = 0 V
t_{PLH}	Propagation Delay				55	100			ns	V_{CC} = 5.0 V, V_{DD} = −13 V
t_{PHL}	Propagation Delay				90	150			ns	See Figure 2

NOTES

1. Max = V_{DD} +1.0 V over Temperature Range. Typ = V_{DD} +0.2 V over Temperature Range.
2. At no time shall the voltage from V_{DD} to V_{TAP} exceed 30 V. See Absolute Maximum Ratings.
3. For Hermetic DIP rating applies to ambient temperatures up to 70°C, above 70°C derate linearly at 8.3 mW/°C. For Flatpak derate linearly at 7.1 mW/°C above 60°C.

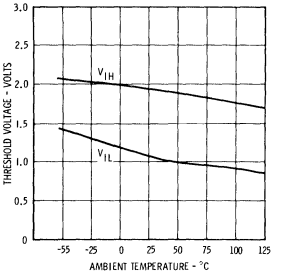




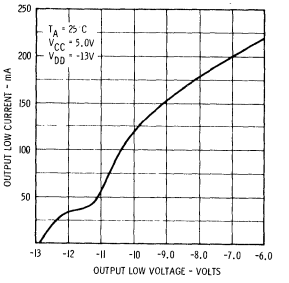
*The extender pin allows the number of inputs to be extended by adding diodes or the DTμL 933 extender.
**Fan out into MOS is limited only by MOS leakage currents.

TYPICAL PERFORMANCE CURVES FOR 9624 AND 9624C

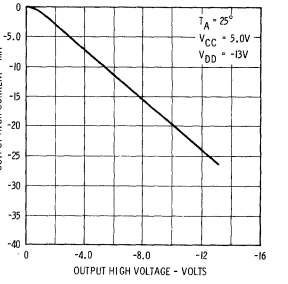
THRESHOLD VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



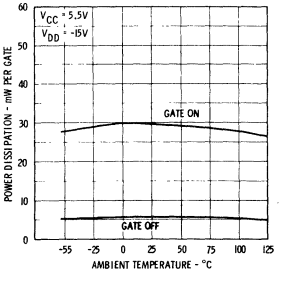
OUTPUT LOW CURRENT AS A FUNCTION OF OUTPUT LOW VOLTAGE



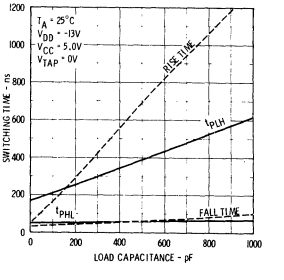
OUTPUT HIGH CURRENT AS A FUNCTION OF OUTPUT HIGH VOLTAGE



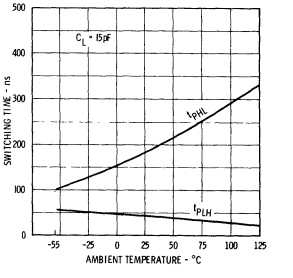
POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



SWITCHING TIME AS A FUNCTION OF LOAD CAPACITANCE

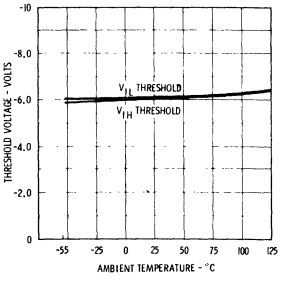


SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE

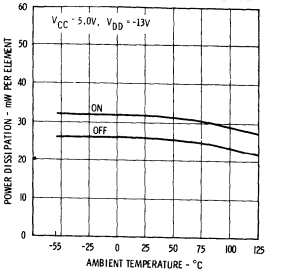


TYPICAL PERFORMANCE CURVES FOR 9625 AND 9625C

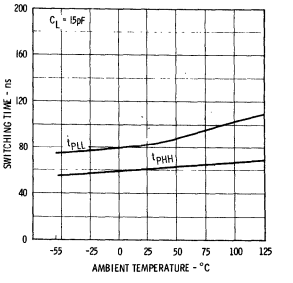
THRESHOLD VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



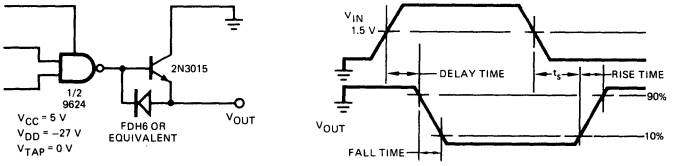
SWITCHING TIME AS A FUNCTION OF AMBIENT TEMPERATURE



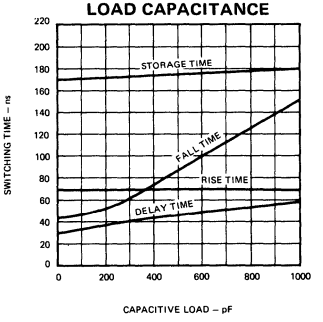
APPLICATIONS

9624 Clock Driving

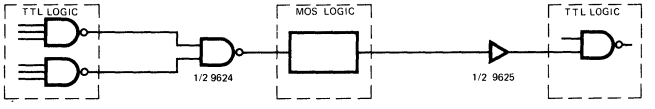
(using a high capacitance drive scheme)



TYPICAL SWITCHING TIMES AS A FUNCTION OF LOAD CAPACITANCE



TYPICAL SYSTEM APPLICATION



9643 • 9644

DUAL TTL TO MOS/CCD DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The 9643 and 9644 are Dual Positive-Logic "AND" and "NAND" TTL-to-MOS Drivers respectively. The 9643 DC/PC is a functional replacement of the SN75322 with one important exception: the two external PNP transistors are no longer needed for operation. The 9643 DC/PC is also a functional replacement for the 75363 with the important exception that the V_{CC3} supply is not needed. The 9644 is a logical inversion of the 9643 and is a functional replacement for the 75361. The pin connections normally used for the external PNP transistors are purposely not internally connected to the 9643 DC/PC.

Both devices have separate driver address inputs with common strobe. Both devices accept standard TTL and DTL input signals and provide high-current and high-voltage output levels suitable for driving MOS/CCD memories. The 9643 may be used to drive the chip-enable clock of the TMS4030 MOS RAM. The 9644 is suitable for driving both clock and address inputs for the TMS4062 and 1103 RAM. The 9643 and 9644 operate from the TTL 5 V supply and the MOS supply.

The 9643 and 9644 are available in 8-pin DIPs for increased board efficiency.

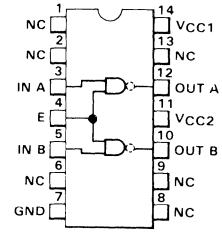
- **SATISFIES CCD MEMORY AND DELAY LINE REQUIREMENTS**
- **DUAL POSITIVE-LOGIC TTL-TO-MOS DRIVERS**
- **OPERATES FROM STANDARD BIPOLAR AND MOS SUPPLY VOLTAGES**
- **HIGH SPEED SWITCHING**
- **TTL AND DTL COMPATIBLE INPUTS**
- **SEPARATE DRIVER ADDRESS INPUTS WITH COMMON STROBE**
- **V_{OH} AND V_{OL} COMPATIBLE WITH POPULAR MOS RAMs**
- **DOES NOT REQUIRE EXTERNAL PNP TRANSISTORS OR V_{CC3}**
- **V_{OH} MINIMUM IS V_{CC2} – 0.5 V**

ABSOLUTE MAXIMUM RATINGS: Over operating ambient temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1)	−0.5 V to 7 V
Supply voltage range of V_{CC2}	−0.5 V to 15 V
Input voltage	5.5 V
Inter-input voltage (see Note 2)	5.5 V
Continuous total dissipation at (or below) 25°C ambient temperature	1000 mW
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C
Pin Temperature	
Molded dip (Soldering, 10 s)	260°C
Hermetic dip (Soldering, 30 s)	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. This rating applies between any two inputs of any one of the gates.

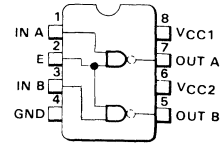
CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
9643	9643DC
9643	9643PC

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 9T 6T
PACKAGE CODES T R



ORDER INFORMATION

TYPE	PART NO.
9643	9643RC
9643	9643TC
9644	9644RC
9644	9644TC

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC1}	4.75	5.0	5.25	V
Supply Voltage, V_{CC2}	4.75	12	15	V
Operating Temperature, T_A	0		70	°C

ELECTRICAL CHARACTERISTICS: Over recommended ranges of V_{CC1}, V_{CC2} and operating ambient temperature unless otherwise noted.

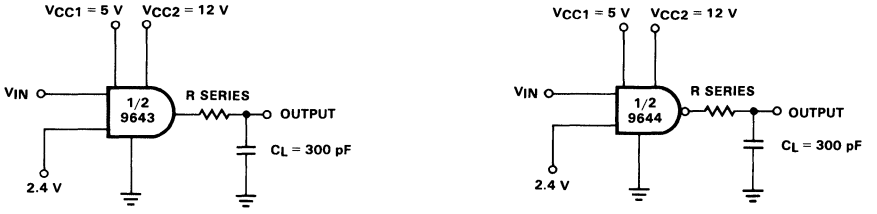
SYMBOL	CHARACTERISTICS	CONDITIONS			MIN	TYP (Note 1)	MAX	UNITS
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = -400 μA			V_{CC2} -0.5	V_{CC2} -0.2		V
V_{OL}	Output LOW Voltage	I_{OL} = 10 mA				0.4	0.5	V
		I_{OL} = 1.0 mA				0.2	0.3	V
I_{IN}	Input Current at Maximum Input Voltage	V_{CC1} = 5.25 V, V_{CC2} = 11.4 V, V_{IN} = 5.25 V					0.1	mA
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V	A Inputs				40	μA
			E Inputs				80	
I_{IL}	Input LOW Current	V_{IN} = 0.4 V	A Inputs	9643			0.5	mA
				9644			0.8	
			E Inputs	9643			-1.0	
				9644			-1.6	
$I_{CC1(L)}$	Supply Current from V_{CC1} All Outputs LOW	V_{CC1} = 5.25 V, V_{CC2} = 12.6 V	No Load	9643		15	19	mA
				9644		14	17	
$I_{CC2(L)}$	Supply Current from V_{CC2} All Outputs LOW	V_{CC2} = 12.6 V	V_{CC1} = 5.25 V	**9643 9644**		5.5	9.5	mA
$I_{CC1(H)}$	Supply Current from V_{CC1} All Outputs HIGH	V_{CC1} = 5.5 V, V_{CC2} = 13.2 V	No Load	9643		9.0	13	mA
				9644		4.0	6.0	
$I_{CC2(H)}$	Supply Current from V_{CC2} All Outputs HIGH	V_{CC2} = 12.6 V	V_{CC1} = 5.25 V	9643 9644		5.5	9.5	mA

NOTE 1: All typical values are at V_{CC1} = 5.0 V, V_{CC2} = 12 V, and T_A = 25°C unless otherwise noted.

AC CHARACTERISTICS: V_{CC1} = 5.0 V, V_{CC2} = 12 V, T_A = 25°C

SYMBOL	CHARACTERISTICS		CONDITIONS (See Figure 1)		MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time	9643 9644	C_L = 300 pF		5.0 3.0	9.0 6.0	17 15	ns ns
t_{DHL}	Delay Time	9643 9644			5.0 3.0	9.0 6.0	17 15	ns ns
t_{TLH}	Rise Time		R_{SERIES} = 0	C_L = 300 pF	6.0	11	17	ns
t_{THL}	Fall Time				6.0	11	17	ns
t_{TLH}	Rise Time		R_{SERIES} = 10Ω		9.0	14	20	ns
t_{THL}	Fall Time				9.0	14	20	ns
$t_{PLH_A} - t_{PLH_B}$ $t_{PHL_A} - t_{PHL_B}$	Skew between outputs A and B					0.5		ns

AC TEST CIRCUIT AND VOLTAGE WAVEFORMS



AC TEST NOTES:

1. The pulse generator has the following characteristics:
   PRR = 1 MHz, Z_{OUT} = 50 Ω
2. C_L includes probe and jig capacitance.

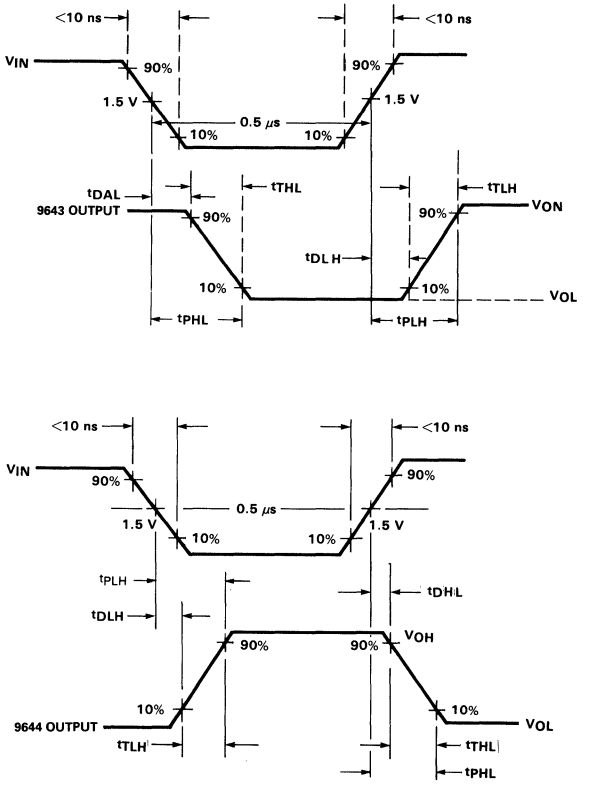


Fig. 1

9645/3245

QUAD TTL-TO-MOS/CCD DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9645/3245 is a high-speed driver intended to be used as a clock (high-level) driver for 18 or 22 pin dynamic NMOS RAMs. It also satisfies the non-overlapping 2-phase clock drive requirements for CCD memories like the F464 (64K) RAM.

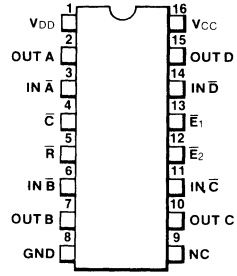
The circuit is designed to operate on nominal +5 V and +12 V power supplies and contains input and output clamp diodes to minimize line reflections.

The device features two common enable inputs, a refresh select input and a clock control input. Internal gating structure is organized so that all four drivers may be deactivated for standby operation, or single driver may be activated for read/write operation or all four drivers may be activated for refresh operation.

The 9645/3245 is a pin for pin replacement of the Intel 3245 Quad TTL-to-MOS Driver, with substantially reduced DC power dissipation.

- **INTERCHANGEABLE WITH INTEL 3245**
- **FOUR HIGH-SPEED, HIGH-CURRENT DRIVERS**
- **CONTROL LOGIC OPTIMIZED FOR MOS RAMs**
- **SATISFIES CCD MEMORY AND DELAY LINE DRIVE REQUIREMENTS**
- **TTL AND DTL COMPATIBLE INPUTS**
- **HIGH VOLTAGE SCHOTTKY TECHNOLOGY**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 7B 9B
PACKAGE CODES D P

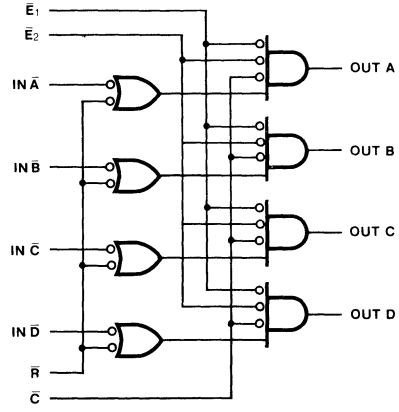


ORDER INFORMATION

TYPE	PART NO.
9645/3245	9645PC/3245
9645/3245	9645DC/3245

8

LOGIC DIAGRAM



TRUTH TABLE					
INPUTS					OUTPUT
CONTROL			ADDRESS		
$\overline{C}$	$\overline{E}_2$	$\overline{E}_1$	INPUT	REFRESH	
H	I	I	I	I	L
I	H	I	I	I	L
I	I	H	I	I	L
I	I	I	H	H	L
L	L	L	L	I	H
L	L	L	I	L	H

H = HIGH LOGIC STATE
L = LOW LOGIC STATE
I = IRRELEVANT

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-10°C to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage, V_{CC}	-0.5 V to +7.0 V
Supply Voltage, V_{DD}	-0.5 V to +14.0 V
All Input Voltages	-1.0 V to V_{DD}
Outputs For Clock Driver	-1.0 V to V_{DD} +1 V
Operating Temperature Range	0°C to +70°C
Junction Temperature (T_J) Ceramic Package	175°C
Plastic Package	150°C

DC CHARACTERISTICS: T_A = 0°C to 70°C, V_{CC} = 5.0 V ±5%, V_{DD} = 12 V ±5%, unless otherwise specified.

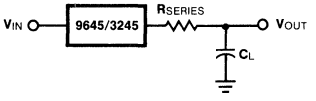
SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{FD}	Input Load Current, IN($\bar{A}$,$\bar{B}$,$\bar{C}$,$\bar{D}$)			-0.25	mA	V_F = 0.45 V
I_{FE}	Input Load Current, ($\bar{R}$, $\bar{C}$, $\bar{E}_1$, $\bar{E}_2$)			-1.0	mA	V_F = 0.45 V
I_{RD}	Data Input Leakage Current			10	μA	V_R = 5.0 V
I_{RE}	Enable Input Leakage Current			40	μA	V_R = 5.0 V
V_{OL}	Output LOW Voltage			0.45	V	I_{OL} = 5 mA, V_{IH} = 2 V
		-1.0			V	I_{OL} = -5 mA
V_{OH}	Output HIGH Voltage	V_{DD}-0.50			V	I_{OH} = -1 mA, V_{IL} = 0.8 V
				V_{DD} + 1.0	V	I_{OH} = 5 mA
V_{IL}	Input LOW Voltage, All Inputs				V	
V_{IH}	Input HIGH Voltage, All Inputs	2			V	
$I_{CC(H)}$	Current From V_{CC}		13	20	mA	V_{CC} = 5.25 V V_{DD} = 12.6 V All Outputs HIGH
$I_{DD(H)}$	Current From V_{DD}		14	20	mA	
$P_{DI(H)}$	Power Dissipation		248	357	mW	
	Power Per Channel		62	90	mW	
$I_{CC(L)}$	Current From V_{CC}		27	35	mA	V_{CC} = 5.25 V V_{DD} = 12.6 V All Outputs LOW
$I_{DD(L)}$	Current From V_{DD}		12	15	mA	
$P_{D2(L)}$	Power Dissipation		296	373	mW	
	Power Per Channel		74	94	mW	

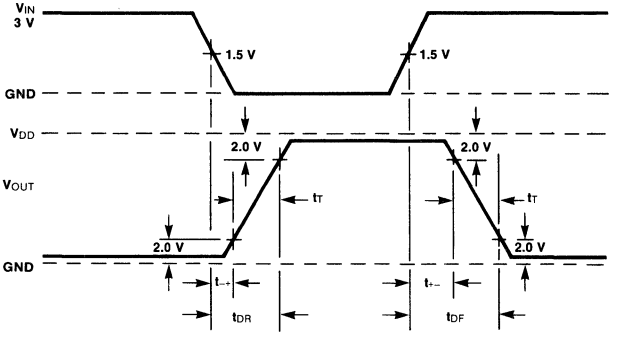
AC CHARACTERISTICS: T_A = 0°C to 70°C, V_{CC} = 5.0 V ±5%, V_{DD} = 12 V ±5% unless otherwise specified.

SYMBOL	CHARACTERISTICS	MIN (1)	TYP (2,4)	MAX (3)	UNITS	TEST CONDITIONS
t_{-+}	Input to Output Delay	5	11		ns	R_{SERIES} = 0
t_{DR}	Delay Plus Rise Time		18	32	ns	R_{SERIES} = 0
t_{+-}	Input to Output Delay	3	7		ns	R_{SERIES} = 0
t_{DF1}	Delay Plus Fall Time		18	32	ns	R_{SERIES} = 0
t_T	Output Transition Time	10	13	20	ns	R_{SERIES} = 20Ω
t_{DR}	Delay Plus Rise Time		27	38	ns	R_{SERIES} = 20Ω
t_{DF2}	Delay Plus Fall Time		24	38	ns	R_{SERIES} = 20Ω

NOTES:
(1.) C_L = 150 pF
(2.) C_L = 200 pF
(3.) C_L = 250 pF
(4.) Typical values are measured at 25°C

AC TEST CIRCUIT AND WAVEFORMS





AC Test Conditions:

Input Pulse Amplitude = 3.0 V
Input PUlse Rise and Fall Times = 5 ns Between 1 volt and 2 volts

9646/0026

DUAL MOS CLOCK DRIVER

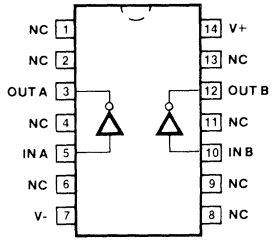
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9646/0026 is a low-cost monolithic dual MOS clock driver, designed for high speed driving of highly capacitive loads in a MOS system. The 9646/0026 is intended for applications in which the output pulse width is logically controlled, i.e., the output pulse width is equal to the input pulse width. 9646/0026 is identical to the DS0026.

- **FAST TRANSITION TIMES - 20ns WITH 1000 pF LOAD**
- **HIGH OUTPUT SWING - 20 V**
- **HIGH OUTPUT CURRENT DRIVE - ±1.5 A**
- **HIGH REPETITION RATE - 5 TO 10 MHz DEPENDING ON LOAD**
- **TTL OR DTL COMPATIBLE INPUTS**
- **LOW POWER CONSUMPTION - 2 mW WHEN IN MOS "0" STATE**
- **+5 V OPERATION FOR N-CHANNEL MOS CAPABILITY**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

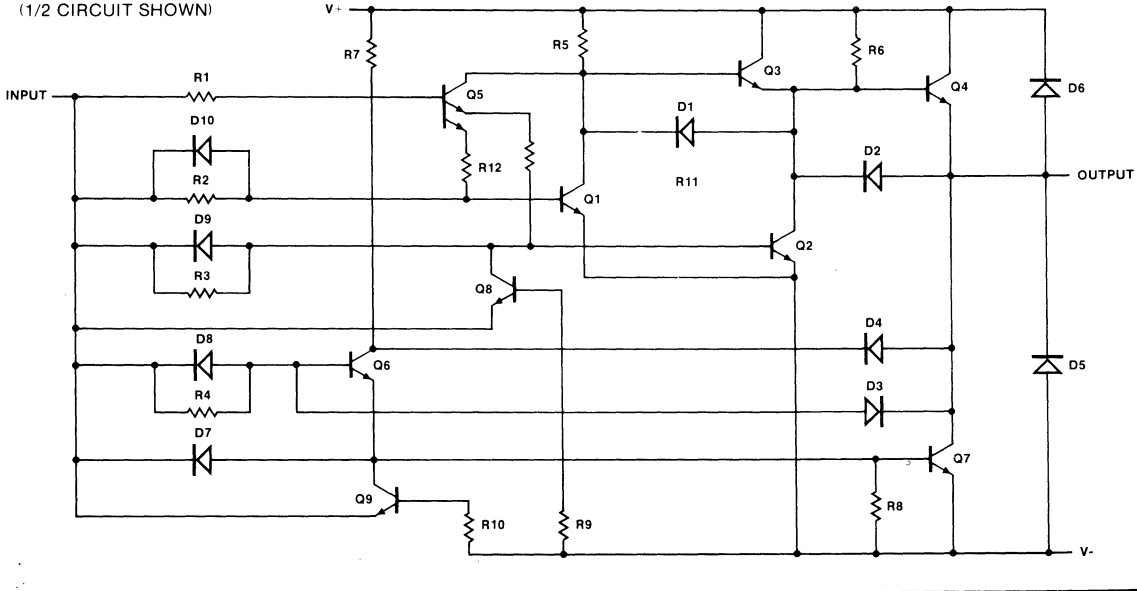
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
9646/0026	9646PC/0026
9646/0026	9646DM/0026

EQUIVALENT CIRCUIT
(1/2 CIRCUIT SHOWN)



ABSOLUTE MAXIMUM RATINGS

V+ - V− Differential Voltage	22 V
Input Current	100 mA
Input Voltage (V_{IN} -V−)	5.5 V
Peak Output Current	1.5 A
Operating Temperature Range	
9646DM/0026	-55°C to +125°C
9646PC/0026	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Pin Temperature (Soldering, 10 s)	300°C

ELECTRICAL CHARACTERISTICS: (Notes 2 and 3)

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logic "1" Input Voltage	V− = 0 V	2	1.5		V
I_{IH}	Logic "1" Input Current	V_{IN} -(V-) = 2.4 V		10	15	mA
V_{IL}	Logic "0" Input Voltage	V− = 0 V		0.6	0.4	V
I_{IL}	Logic "0" Input Current	V_{IN} -(V-) = 0 V		-3	-10	μA
V_{OL}	Logic "1" Output Voltage	V_{IN} -(V-) = 2.4 V		(V-)+0.7	(V-)+1.0	V
V_{OH}	Logic "0" Output Voltage	V_{IN} -(V-) = 0.4 V, $V_{BB} \geq$ V+ +1.0 V	V+ -1.0	V+ -0.7		V
$I_{CC(ON)}$	"ON" Supply Current	(V+) - (V-) = 20 V, V_{IN} - (V-) = 2.4 V one side on		30	40	mA
$I_{CC(OFF)}$	"OFF" Supply Current	(V+) - (V-) = 20 V V_{IN} - (V-) = 0 V		10 50	100 500	μA μA

SWITCHING CHARACTERISTICS: T_A = 25°C (Notes 5 and 7)

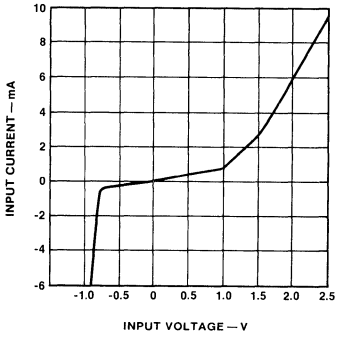
SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON}	Turn-on Delay	Figure 1 Figure 2		5	7.5 11	12	ns ns
t_{OFF}	Turn-off Delay	Figure 1 Figure 2			12 13	15	ns ns
t_r	Rise Time	Figure 1 Note 5	C_L = 500 pF C_L = 1000 pF		15 20	18 35	ns ns
		Figure 2 Note 5	C_L = 500 pF C_L = 1000 pF		30 36	40 50	ns ns
t_f	Fall Time	Figure 1 Note 5	C_L = 500 pF C_L = 1000 pF		12 17	16 25	ns ns
		Figure 2 Note 5	C_L = 500 pF C_L = 1000 pF		28 31	35 40	ns ns

NOTES:
1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
2. These specifications apply for (V+) - (V-) = 10 V to 20 V, C_L = 1000 pF, over the temperature range of -55° C to +125° C for the 9646DM and 0° C to +70° C for the 9646PC.
3. All currents into device pins shown as positive, out of device pins are negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
4. All typical values for the T_A = 25°C.
5. Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

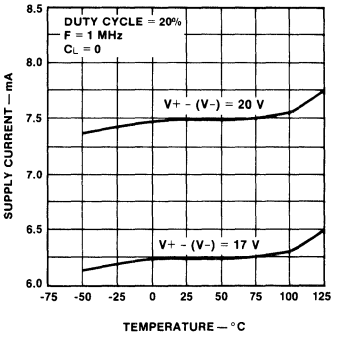
8

TYPICAL PERFORMANCE CURVE

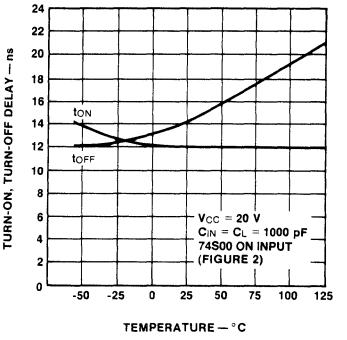
INPUT CURRENT VS INPUT VOLTAGE



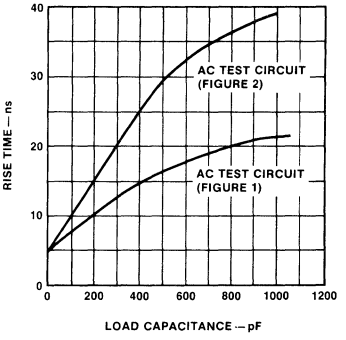
SUPPLY CURRENT VS TEMPERATURE



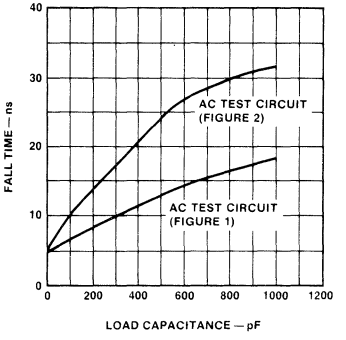
TURN-ON AND TURN-OFF DELAY VS TEMPERATURE



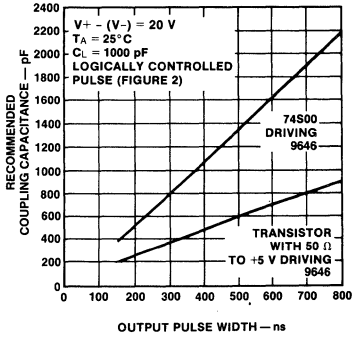
RISE TIME VS LOAD CAPACITANCE



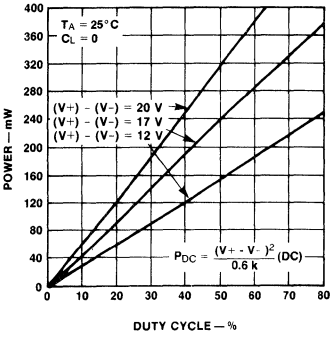
FALL TIME VS LOAD CAPACITANCE

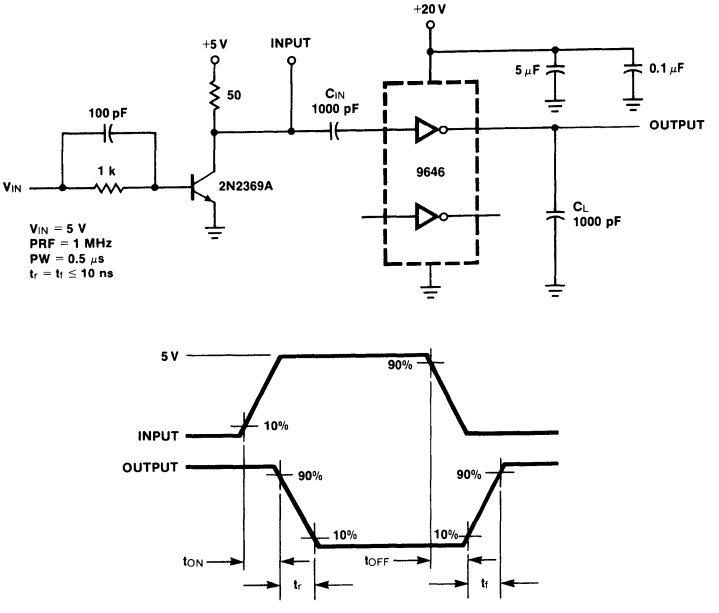


RECOMMENDED INPUT COUPLING CAPACITANCE



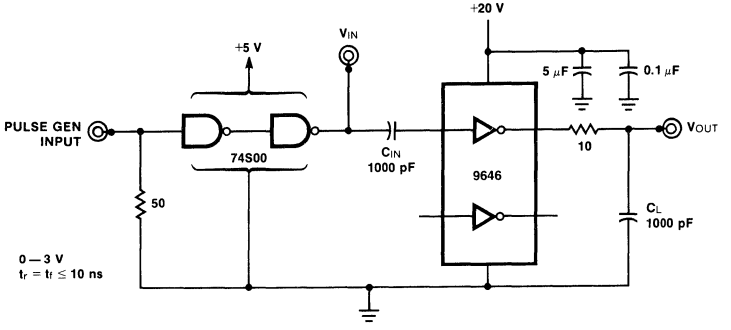
DC POWER (P_{DC}) VS DUTY CYCLE




+20 V
+5 V
INPUT
50
CIN
1000 pF
5 μF
0.1 μF
100 pF
OUTPUT
1 k
VIN
2N2369A
9646
CL
1000 pF
VIN = 5 V
PRF = 1 MHz
PW = 0.5 μs
tr = tf ≤ 10 ns

5 V
90%
INPUT
10%
OUTPUT
90%
90%
10%
10%
tON
tOFF
tr
tf

Fig. 1


+20 V
VIN
+5 V
5 μF
0.1 μF
PULSE GEN
INPUT
74S00
CIN
1000 pF
9646
10
VOUT
50
CL
1000 pF
0 — 3 V
tr = tf ≤ 10 ns

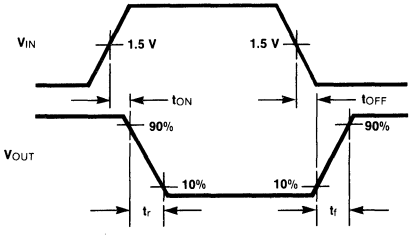

VIN
1.5 V
1.5 V
tON
tOFF
90%
90%
VOUT
10%
10%
tr
tf

Fig. 2

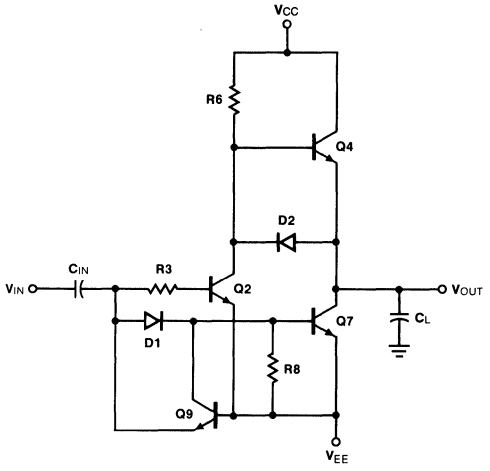


Fig. 3 SIMPLIFIED SCHEMATIC DIAGRAM

APPLICATIONS INFORMATION

OPERATION OF THE 9646/0026

The simplified schematic diagram of 9646/0026, shown in *Figure 3* is useful in explaining the operation of the device. *Figure 3* illustrates that as the input voltage level goes high, diode D1 provides an 0.7 V "dead zone" thus ensuring that Q2 is turned "on" and Q4 is turned "off" before Q7 is turned "on". This prevents undesirable "current spiking" from the power supply, which would occur if Q7 and Q4 were allowed to be "on" simultaneously for an instant of time. Diode D2 prevents "zenering" of Q4 and provides an initial discharge path for the output capacitive load by way of Q2.

As the input voltage level goes low, the stored charge in Q2 is used advantageously to keep Q2 "on" and Q4 "off" until Q7 is "off". Again undesirable "current spiking" is prevented. Due to the external capacitor, the input side of C_{in} goes negative with respect to V_{EE} causing Q9 to conduct momentarily thus assuring rapid turn "off" of Q7.

The complete circuit (equivalent circuit on front page) basically creates Darlington devices of transistors Q7, Q4 and Q2 as shown in the simplified circuit of *Figure 3*. Note that when the input goes negative with respect to V_{EE}, diodes D7 through D10 turn "on" assuring faster turn "off" of transistors Q1, Q2, Q6 and Q7. Resistor R6 insures that the output will charge to within one V_{BE} voltage drop of the V_{CC} supply.

SYSTEM CONSIDERATIONS

Overshoot

In most system applications the output waveform of the 9646/0026 will "overshoot" to some degree. However, "overshoot" can be eliminated or reduced by placing a damping resistor in series with the output. The amount of resistance required is given by: $R_S = 2\sqrt{L/C_L}$ where L is the inductance of the line and C_L is the load capacitance. In most cases a series of damping resistor in the range of 10- to-50Ω will be sufficient. The damping resistor also affects the transition times of the outputs. The speed reduction is given by the formula:

$$t_{THL} \approx t_{TLH} = 2.2\ R_S\ C_L \text{ (R_S is the damping resistor).}$$

Crosstalk

The 9646/0026 is sensitive to crosstalk when the output voltage level is high ($V_O \approx V_{CC}$). With the output in the high voltage level state, Q3 and Q4 are essentially turned "off". Therefore, negative-going crosstalk will pull the output down until Q4 turns "on" sufficiently to pull the output back

towards V_{CC}. This problem can be minimized by placing a "bleeding" resistor from the output to ground. The "bleeding" resistor should be of sufficient size so that Q4 conducts only a few milliamperes. Thus, when noise is coupled, Q4 is already "on" and the line is quickly clamped by Q4. Also note that in the equivalent circuit D6 clamps the output one diode-voltage drop above V_{CC} for positive-going crosstalk.

Power Supply Decoupling

The decoupling of V_{CC} and V_{EE} is essential in most systems. Sufficient capacitive decoupling is required to supply the peak surge currents during switching. At least a 0.1 μF to 1.0 μF low inductive capacitor should be placed as close to each driver package as the layout will permit.

Input Driving

For those applications requiring split power supplies (V_{EE} < GND) ac coupling should be employed. Selection of the input capacitor size is determined by the desired output pulse width. Maximum performance is attained when the voltage at the input of the 9646/0026 discharges to just above the device's threshold voltage (about 1.5 V). Performance curve shows optimum values for C_{in} versus the desired output pulse width. The value for C_{in} may be roughly predicted by:

$$C_{in} = (2 \times 10^{-3}) (PW_O).$$

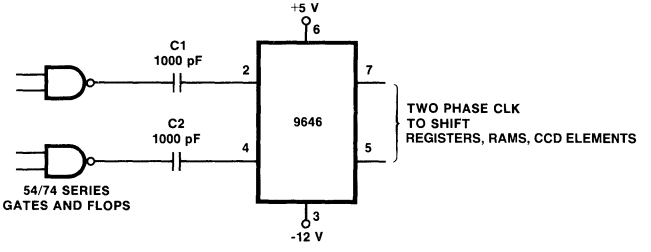
For an output pulse width of 500 ns, the optimum value for C_{in} is:

$$C_{in} = (2 \times 10^{-3}) (500 \times 10^{-9}) = 1000 \text{ pF}.$$

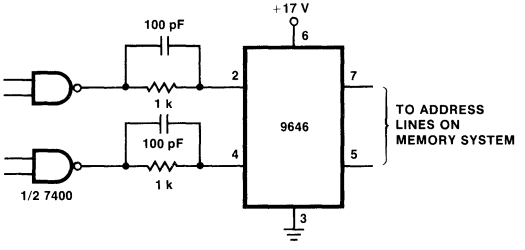
If single supply operation is required (V_{EE} = GND), then dc coupling as illustrated in *Figure 4* can be employed. For maximum switching performance, a speed-up capacitor should be employed with dc coupling. Performance curves show typical switching characteristics for various values of input resistance and capacitance.

TYPICAL APPLICATIONS

AC COUPLED MOS CLOCK DRIVER



DC COUPLED RAM MEMORY ADDRESS OR PRECHARGE DRIVER (POSITIVE SUPPLY ONLY)



55/75S20 • 55/75S24 • 55/75S234

DUAL SCHOTTKY CORE MEMORY SENSE AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 55/75S20 series of Schottky sense amplifiers are designed for use with high-speed core memory systems, where a guaranteed narrow threshold uncertainty of ±2.5 mV is guaranteed.

A unique Schottky circuit design provides inherent stability of the very accurate input threshold levels over a wide range of power supply voltage levels and temperature ranges.

These sense amplifiers detect bipolar millivolt-level differential input signals from the memory and provide the interface circuitry between the memory and the logic section.

The Fairchild 75S20 and 75S24 do not require an external capacitor (C_{ext}) to stabilize the pre-amplifier section of the sense amplifier. No degradation of performance will result if a 100 pF capacitor is connected from pin 1 to ground.

The 55/75S20 circuit may be used to perform the functions of a flip-flop or register which responds to the sense and strobe input conditions.

The 55/75S24 is intended to be used in systems where independent dual channel sensing with separate outputs are required. 55/75S234 is similar to the 55/75S24, but have inverted outputs.

- **MAX ±2.5 mV OF THRESHOLD VOLTAGE UNCERTAINTY**
- **INTERNAL COMPENSATION**
- **SCHOTTKY TECHNOLOGY**
- **HIGH SPEED AND FAST RECOVERY TIME**
- **ADJUSTABLE THRESHOLD VOLTAGE LEVELS**
- **CHOICE OF OUTPUT CIRCUIT FUNCTION**
- **TTL OR DTL DRIVE CAPABILITY**
- **TIME AND AMPLITUDE SIGNAL DISCRIMINATION**

ABSOLUTE MAXIMUM RATINGS Over Operating Ambient Temperature Range (unless otherwise noted).

Supply Voltages (see Note 1)	
V_{CC+}	7 V
V_{CC-}	−7 V
Differential Input Voltage, V_{ID} or V_{REF}	±5 V
Voltage From Any Input to Ground (see Note 2)	5.5 V
Off-State Voltage Applied to Open-Collector Outputs	5.5 V
Storage Temperature Range	−65 °C to 150 °C

RECOMMENDED OPERATING CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC\pm}$ (see Note 1) 75 series	±4.75	±5	±5.25	V
$V_{CC\pm}$ (see Note 1) 55 series	±4.50	±5	±5.5	V
V_{REF}	15		40	mV
Operating Ambient Temperature Range, 55S20 Series			−55 °C to 125 °C	
75S20 Series			0 °C to 70 °C	

NOTES:
1. These voltage values are with respect to network ground terminal.
2. Strobe and gate input voltages must be zero or positive with respect to network ground terminal.

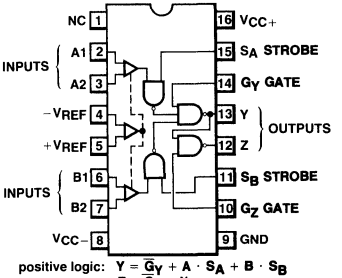
55/75S20

DUAL-CHANNEL SENSE AMPLIFIER WITH COMPLEMENTARY OUTPUTS

FUNCTION TABLE

INPUTS						OUTPUTS	
A	B	G_Y	G_Z	S_A	S_B	Y	Z
X	X	L	X	X	X	H	$\overline{G}_Z$
H	X	X	X	H	X	H	$\overline{G}_Z$
X	H	X	X	X	H	H	$\overline{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



positive logic: $Y = \overline{G_Y} + A \cdot S_A + B \cdot S_B$
$Z = \overline{G_Z} + Y$
$Z = \overline{G_Z} + G_Y(\overline{A} + \overline{S_A})(\overline{B} + \overline{S_B})$

ORDER INFORMATION

TYPE	PART NO.
55S20	55S20DM
75S20	75S20PC
75S20	75S20DC

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A or B†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
Any G or S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A and B are differential voltages (V_{ID}) between A1 and A2 or B1 and B2, respectively. For these circuits, V_{ID} is considered positive regardless of which terminal of each pair is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5 V, V_{CC-} = −5V, over recommended operating temperature range, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNITS
V_T	Differential input threshold voltage (see Note 3)	1	V_{REF} = 15 mV	12.5	15	17.5	mV
			V_{REF} = 40 mV	37.5	40	42.5	
V_{ICF}	Common-mode input firing voltage (see Note 4)	None	V_{REF} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-mode input pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe and gate inputs)	3		2			V
V_{IL}	Low-level input voltage (strobe and gate inputs)	3				0.8	V
V_{OH}	High-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4V			40	μA
I_{IL}	Low-level input current (strobe and gate inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V		−1	−1.6	mA
$I_{OS(Y)}$	Short-circuit output current into Y	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V	−3		−5	mA
$I_{OS(Z)}$	Short-circuit output current into Z	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C		28	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C		−14	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifer to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable pulse present.

8

55/75S20

DUAL-CHANNEL SENSE AMPLIFIER WITH COMPLEMENTARY OUTPUTS

SWITCHING CHARACTERISTICS: $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25°C$

PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(DY)}$	A1-A2 OR B1-B2	Y	15	$C_L = 15$ pF, $R_L = 288\ \Omega$		25	40	ns
$t_{PHL(DY)}$						20		
$t_{PLH(DZ)}$	A1-A2 OR B1-B2	Z	15	$C_L = 15$ pF, $R_L = 288\ \Omega$		30		ns
$t_{PHL(DZ)}$						35	55	
$t_{PLH(SY)}$	STROBE A OR B	Y	15	$C_L = 15$ pF, $R_L = 288\ \Omega$		15	30	ns
$t_{PHL(SY)}$						20		
$t_{PLH(SZ)}$	STROBE A OR B	Z	15	$C_L = 15$ pF, $R_L = 288\ \Omega$		30		ns
$t_{PHL(SZ)}$						35	55	
$t_{PLH(GY, Y)}$	GATE G_Y	Y	16	$C_L = 15$ pF, $R_L = 288\ \Omega$		15	25	ns
$t_{PHL(GY, Y)}$						10		
$t_{PLH(GY, Z)}$	GATE G_Y	Z	16	$C_L = 15$ pF, $F_L = 288\ \Omega$		15		ns
$t_{PHL(GY, Z)}$						20	30	
$t_{PLH(GZ, Z)}$	GATE G_Z	Z	*17	$C_L = 15$ pF, $R_L = 288\ \Omega$		15		ns
$t_{PHL(GZ, Z)}$						10	20	

TYPICAL RECOVERY AND CYCLE TIMES: $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25$ °C

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* $V_{ID} = 2$ V, $t_r = t_f = 20$ ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* $V_{IC} = \pm 2$ V, $t_r = t_f = 20$ ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.

6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

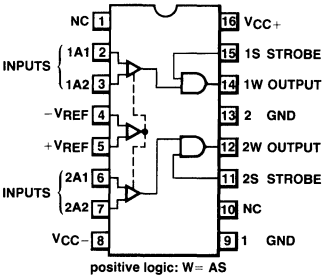
55/75S24

DUAL SENSE AMPLIFIER

FUNCTION TABLE

INPUTS		OUTPUT
A	S	W
H	H	H
L	X	L
X	L	L

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



NC—No internal connection

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ORDER INFORMATION

TYPE	PART NO.
55S24	55S24DM
75S24	75S24DC
75S24	75S24PC

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5 V, V_{CC-} = −5V, over recommended operating temperature range, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNITS
V_T	Differential-input threshold voltage (see Note 3)	8	V_{REF} = 15 mV	12.5	15	17.5	mV
			V_{REF} = 40 mV	37.5	40	42.5	
V_{ICF}	Common-mode input firing voltage (see Note 4)		V_{REF} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	7		2			V
V_{IL}	Low-level input voltage (strobe inputs)	7				0.8	V
V_{OH}	High-level output voltage	7	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	7	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	9	V_{CC+} = 5.25 V, V_{CC-} = +5.25 V, V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	9	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	10	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25 °C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25 °C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25 °C.

NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable pulse present.

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SWITCHING CHARACTERISTICS: $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25$ °C

PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1–A2	W	18	$C_L = 15$ pF, $R_L = 288\,\Omega$		25	40	ns
$t_{PHL(D)}$						20		
$t_{PLH(S)}$	STROBE	W	18	$C_L = 15$ pF, $R_L = 288\,\Omega$		15	30	ns
$t_{PHL(S)}$						20		

TYPICAL RECOVERY AND CYCLE TIMES: $V_{CC+} = 5$ V, $V_{CC-} = -5$ V, $T_A = 25$ °C

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* $V_{ID} = 2V$, $t_r = t_f = 20$ ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* $V_{IC} = \pm 2$ V, $t_r = t_f = 20$ ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

55S234/75S234

DUAL SENSE AMPLIFIERS

FUNCTION TABLE

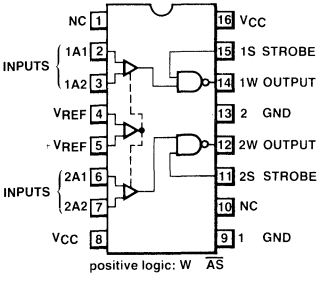
INPUTS		OUTPUT
A	S	W
H	H	L
L	X	H
X	L	H

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_T$ max	$V_{ID} \leq V_T$ min	Irrelevant
S	$V_I \geq V_{IH}$ min	$V_I \leq V_{IL}$ max	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



NC—No internal connection

ORDER INFORMATION

TYPE	PART NO.
55S234	55S234DM
75S234	75S234PC
75S234	75S234DC

55S234/75S234

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5 V, V_{CC-} = −5V, over recommended operating temperature range, unless otherwise noted.

SYMBOL	CHARACTERISTICS	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP‡	MAX	UNITS
V_T	Differential-input threshold voltage (see Note 3)	11	V_{REF} = 15 mV	12.5	15	17.5	mV
			V_{REF} = 40 mV	37.5	40	42.5	
V_{ICF}	Common-mode input firing voltage (see Note 4)		V_{REF} = 40 mV, $V_{I(S)} = V_{IH}$ *Common-Mode Input Pulse:* $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns		±2.5		V
I_{IB}	Differential-input bias current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		30	75	μA
I_{IO}	Differential-input offset current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		0.5		μA
V_{IH}	High-level input voltage (strobe inputs)	12		2			V
V_{IL}	Low-level input voltage (strobe inputs)	12				0.8	V
V_{OH}	High-level output voltage	12	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA	2.4	4		V
V_{OL}	Low-level output voltage	12	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	High-level input current (strobe inputs)	13	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V			1	mA
I_{IL}	Low-level input current (strobe inputs)	13	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current	14	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V	−2.1		−3.5	mA
I_{CC+}	Supply current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25 °C		25	40	mA
I_{CC-}	Supply current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25 °C		−15	−20	mA

‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25 °C.

NOTES: 3. The differential-input threshold voltage (V_T) is defined as the d-c differential-input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.

4. Common-mode input firing voltage is the minimum common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common-mode input signal is applied with a strobe-enable pulse present.

SWITCHING CHARACTERISTICS: V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25 °C

PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1–A2	W	19	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PLH(S)}$	STROBE	W	19	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

TYPICAL RECOVERY AND CYCLE TIMES: V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25 °C

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential-input overload recovery time (see Note 5)	*Differential Input Pulse:* V_{ID} = 2 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common-mode-input overload recovery time (see Note 6)	*Common-Mode Input Pulse:* V_{IC} = ±2 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(min)}$	Minimum cycle time			200		ns

NOTES: 5. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.

6. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode input overload signal prior to the strobe-enable signal.

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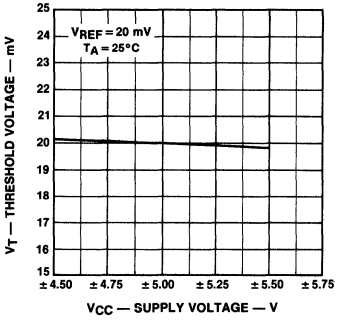
75S20/75S24/75S234

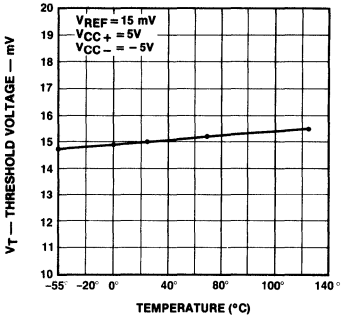
DUAL CORE MEMORY SENSE AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS

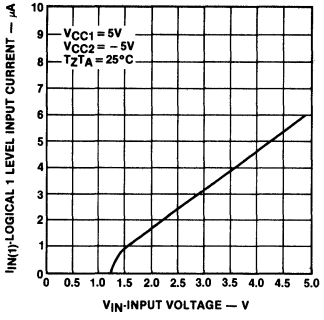
TYPICAL THRESHOLD VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



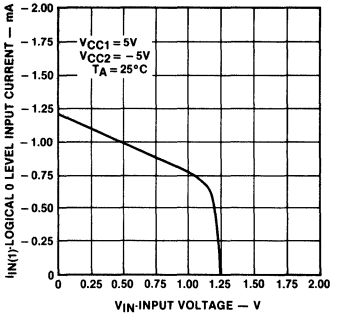
TYPICAL THRESHOLD AS A FUNCTION, VOLTAGE OF TEMPERATURE



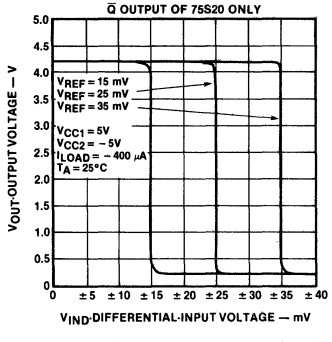
LOGICAL 1 LEVEL INPUT CURRENT VS. INPUT VOLTAGE



LOGICAL 0 LEVEL INPUT CURRENT VS. INPUT VOLTAGE



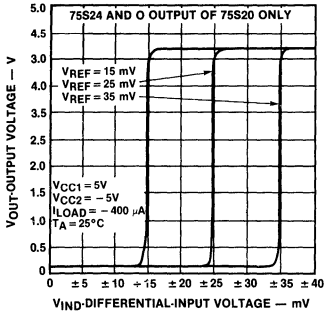
OUTPUT VOLTAGE VS. DIFFERENTIAL INPUT VOLTAGE



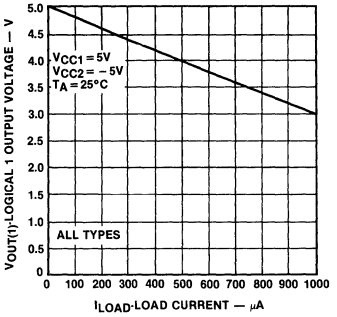
75S20/75S24/75S234
DUAL CORE MEMORY SENSE AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

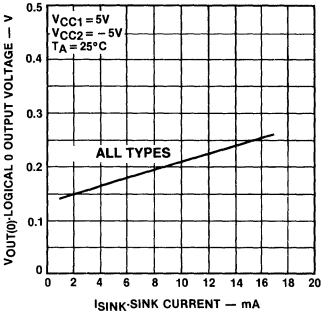
OUTPUT VOLTAGE VS. DIFFERENTIAL-INPUT VOLTAGE



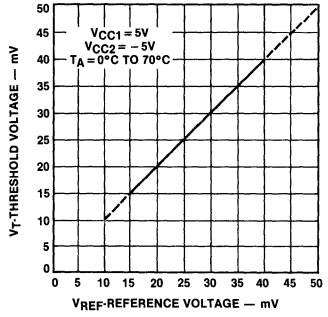
LOGICAL 1 OUTPUT VOLTAGE VS. LOAD CURRENT



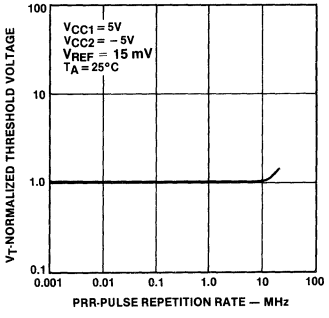
LOGICAL 0 OUTPUT VOLTAGE VS. SINK CURRENT



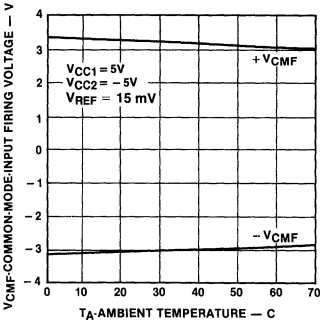
THRESHOLD VOLTAGE VS. REFERENCE VOLTAGE



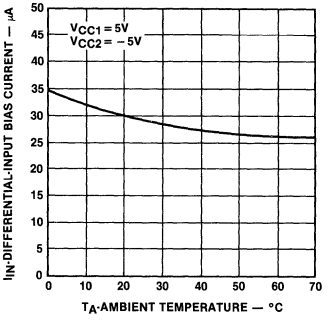
NORMALIZED THRESHOLD VOLTAGE VS. PULSE REPETITION RATE



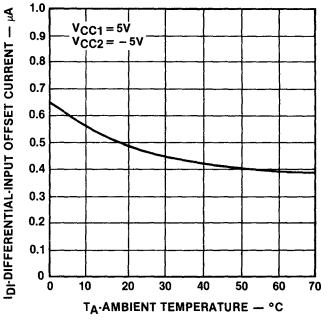
COMMON MODE FIRING VOLTAGE VS. AMBIENT TEMPERATURE



DIFFERENTIAL-INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



DIFFERENTIAL-INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



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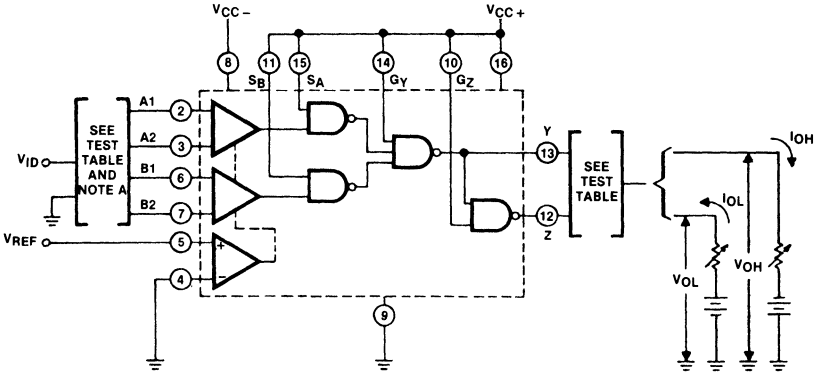
CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUITS†

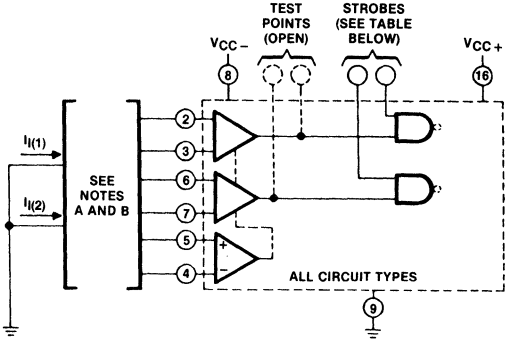


TEST TABLE

CIRCUIT TYPE	INPUTS	V_{REF}	V_{ID}	OUTPUT Y			OUTPUT Z		
				V_O	I_{OH}	I_{OL}	V_O	I_{OH}	I_{OL}
55/75S20	A1-A2 or B1-B2	15 mV	≤12.5 mV	≤0.4 V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	15 mV	≥17.5 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA
	A1-A2 or B1-B2	40 mV	≤37.5 mV	≤0.4V		16 mA	≥2.4 V	−400 μA	
	A1-A2 or B1-B2	40 mV	≥42.5 mV	≥2.4 V	−400 μA		≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with the other pair grounded.

Fig. 1 75S20 V_T



NOTES: A. Each preamplifier is tested separately. Inputs not under test are grounded.
B. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each); $I_{IO} = I_{1(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

CIRCUIT TYPES	APPLY V_{CC+}	APPLY GND	LEAVE OPEN
55/75S20	G_Y, G_Z (14) (10)	S_A, S_B (15) (11)	Y, Z (13) (12)
55/75S24		1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)
55/75S234		1S, 2S, GND 2 (15) (11) (13)	1W, 2W (14) (12)

Fig. 2 I_{IB}, I_{IO}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUITS† (Cont'd)

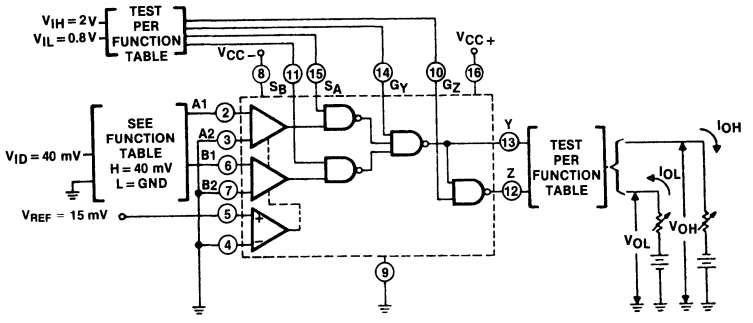
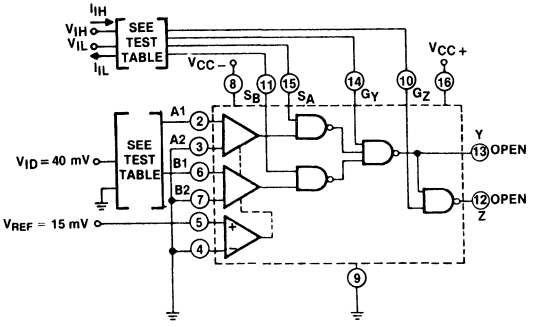


Fig. 3 V_{IH}, V_{IL}, V_{OH}, V_{OL}



TEST TABLE

TEST	INPUT A1	INPUT B1	STROBE S_A	STROBE S_B	GATE G_Y	GATE G_Z
I_{IH} at STROBE S_A	GND	GND	V_{IH}	V_{IL}	V_{IL}	V_{IL}
I_{IH} at STROBE S_B	GND	GND	V_{IL}	V_{IH}	V_{IL}	V_{IL}
I_{IH} at GATE G_Y	V_{ID}	V_{ID}	V_{IH}	V_{IH}	V_{IH}	V_{IL}
I_{IH} at GATE G_G	GND	GND	V_{IL}	V_{IL}	V_{IH}	V_{IH}
I_{IL} at STROBE S_A	V_{ID}	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at STROBE S_B	GND	V_{ID}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Y	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}
I_{IL} at GATE G_Z	GND	GND	V_{IL}	V_{IL}	V_{IL}	V_{IL}

Fig. 4 I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUITS† (Cont'd)

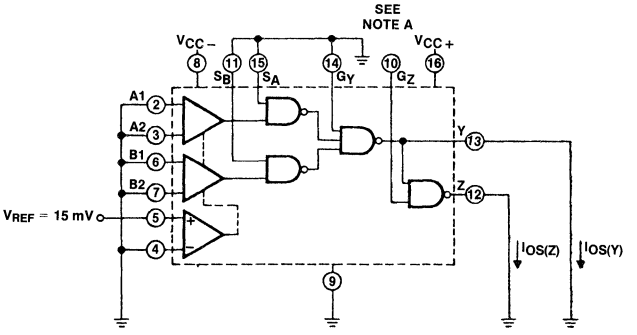
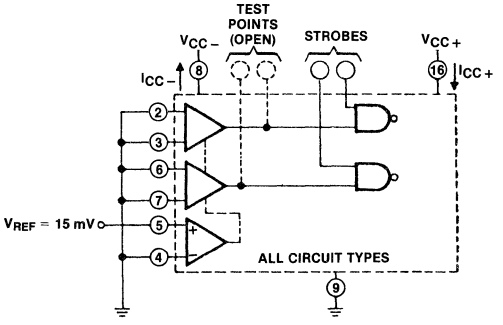


Fig. 5 I_{OS}

NOTE A: When testing $I_{OS(Y)}$, Pin 10 is open; when testing $I_{OS(Z)}$, Pin 10 is grounded.



PIN CONNECTIONS (OTHER THAN THOSE SHOWN ABOVE)

CIRCUIT TYPES	APPLY GND	LEAVE OPEN
55/75S20	G_Y, G_Z, S_A, S_B ⑭ ⑩ ⑮ ⑪	Y, Z ⑬ ⑫
55/75S24	1S, 2S, GND 2 ⑮ ⑪ ⑬	1W, 2W ⑭ ⑫
55/75S234	1S, 2S, GND 2 ⑮ ⑪ ⑬	1W, 2W ⑭ ⑫

Fig. 6 I_{CC+}, I_{CC-}

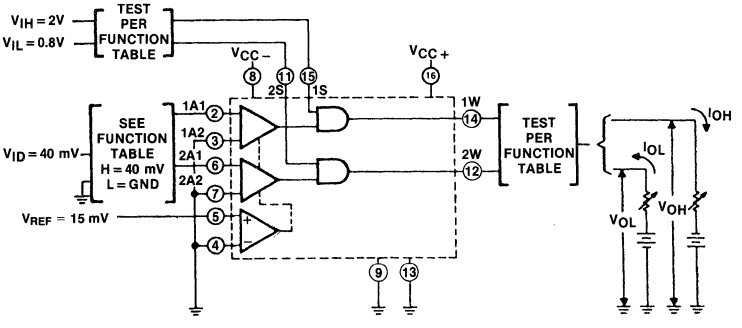
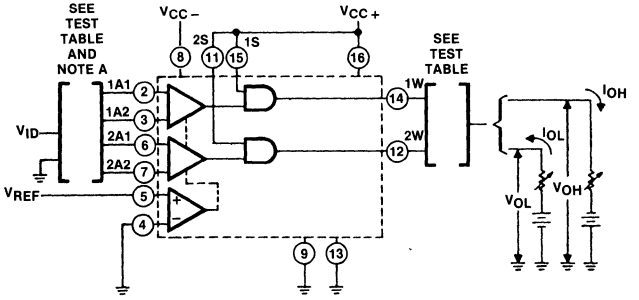


Fig. 7 V_{IH}, V_{IL}, V_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUITS† (Cont'd)

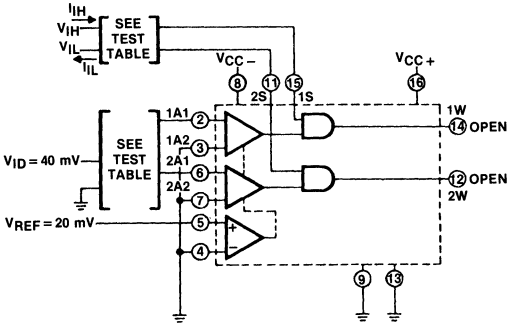


TEST TABLE

CIRCUIT TYPE	INPUTS	V_{REF}	V_{ID}	OUTPUT		
				V_O	I_{OH}	I_{OL}
75S24	A1-A2	15 mV	≤12.5 mV	≤0.4 V		16 mA
	A1-A2	15 mV	≥17.5 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≤37.5 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≥42.5 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

Fig. 8 75S24, V_T



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

Fig. 9 I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUITS† (Cont'd)

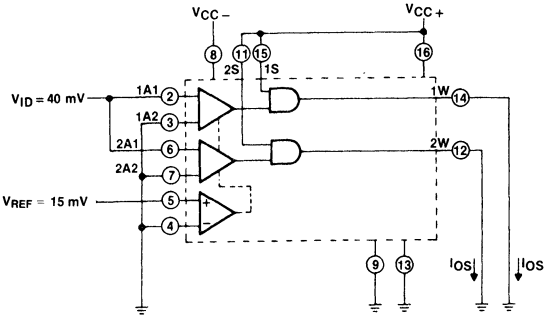
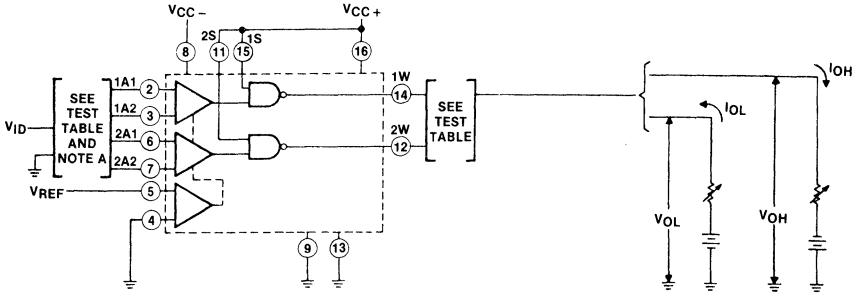


Fig. 10 75S24, I_{OS}



CIRCUIT TYPE	INPUTS	V_{REF}	V_{ID}	OUTPUTS 55/7S234		
				V_O	I_{OH}	I_{OL}
55/7S234	A1-A2	15 mV	≤12.5 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥17.5 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤37.5 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥42.5 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

Fig. 11 75S234, V_T

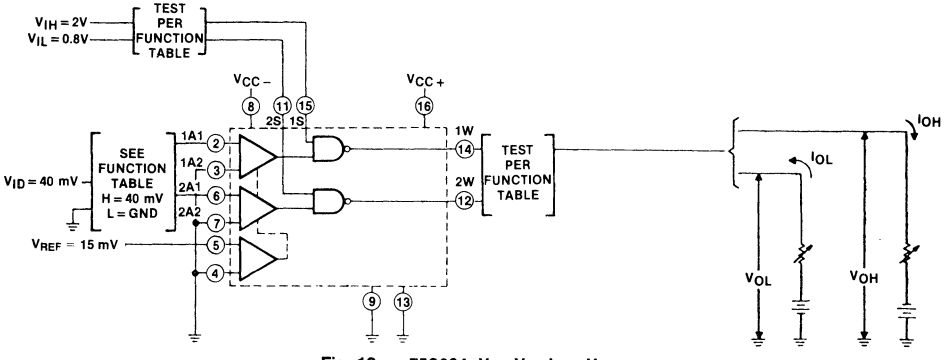
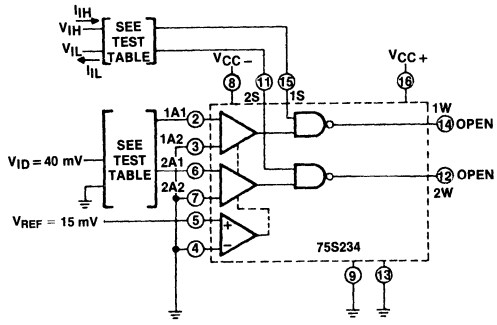


Fig. 12 75S234, V_{IH}, V_{IL}, I_{OH}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUITS† (Cont'd)



TEST TABLE

TEST	INPUT 1A1	INPUT 2A1	STROBE 1S	STROBE 2S
I_{IH} at STROBE 1S	GND	GND	V_{IH}	V_{IL}
I_{IH} at STROBE 2S	GND	GND	V_{IL}	V_{IH}
I_{IL} at STROBE 1S	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at STROBE 2S	GND	V_{ID}	V_{IL}	V_{IL}

Fig. 13 75S234, I_{IH}, I_{IL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

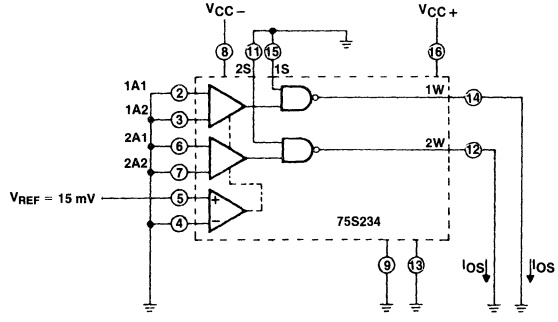
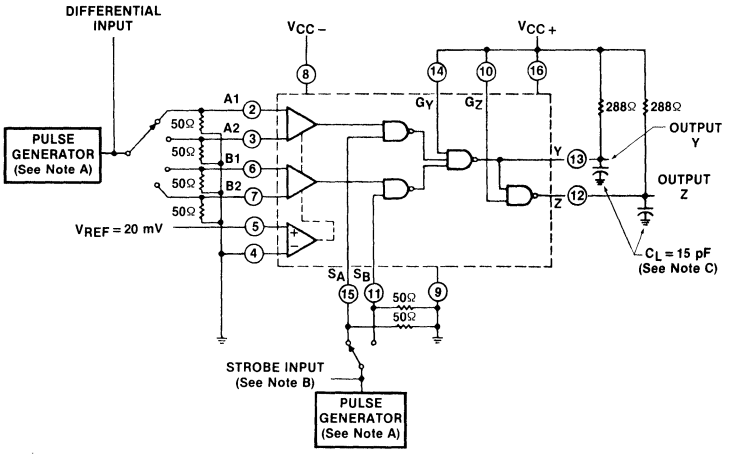


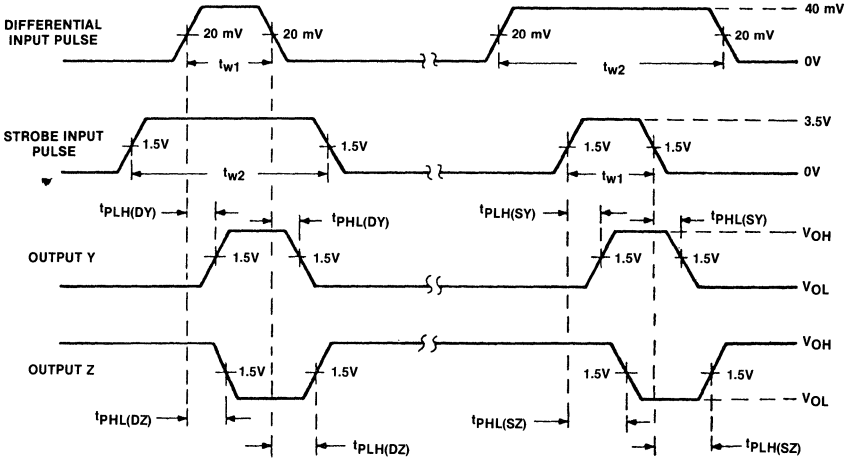
Fig. 14 75S234, I_{OS}

CHARACTERISTICS MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



TEST CIRCUIT



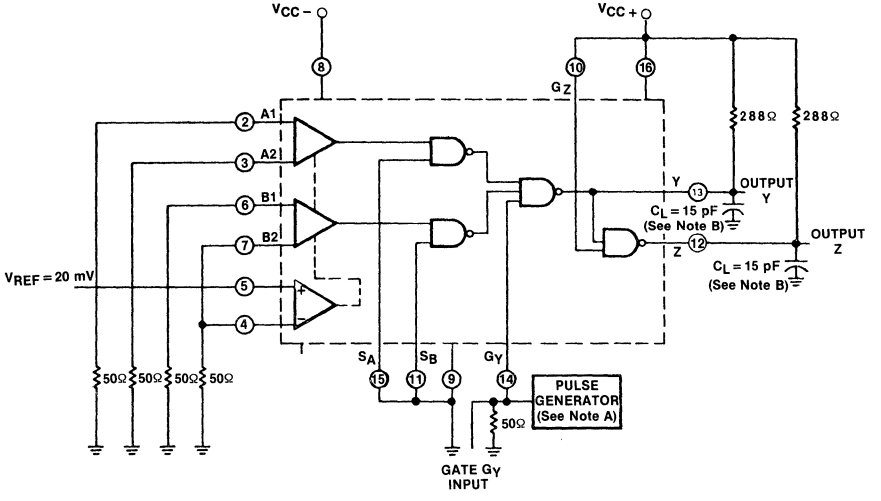
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_O = 50\ \Omega$, $t_r = 15 \pm 5$ ns, $t_f = 15 \pm 5$ ns, $t_{w1} = 100$ ns, $t_{w2} = 300$ ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe S_A when inputs A1-A2 are being tested and to Strobe S_B when inputs B1-B2 are being tested.
C. C_L includes probe and jig capacitance.

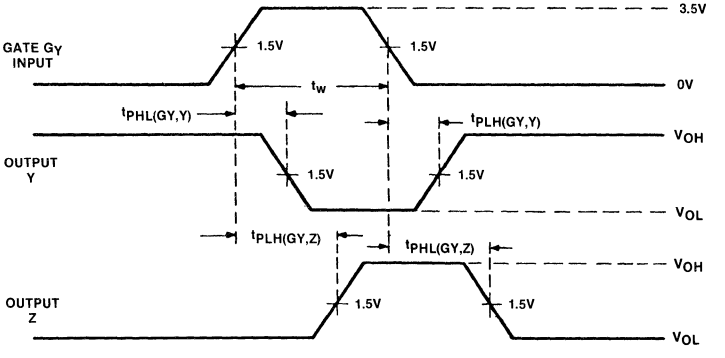
Fig. 15 55/75S20 PROPAGATION DELAY TIMES FROM DIFFERENTIAL AND STROBE INPUTS

CHARACTERISTICS MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Cont'd)



TEST CIRCUIT



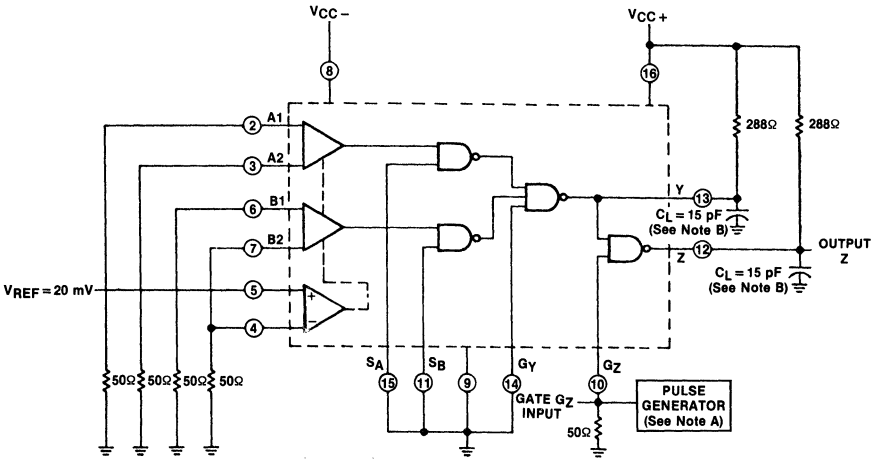
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, $t_r = 15 \pm 5$ ns, $t_f = 15 \pm 5$ns, $t_w = 100$ ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

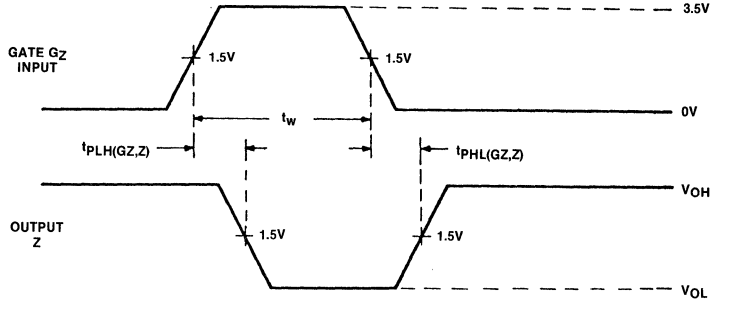
Fig. 16 55/75S20 PROPAGATION DELAY TIMES FROM GATE G_Y

CHARACTERISTICS MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Cont'd)



TEST CIRCUIT



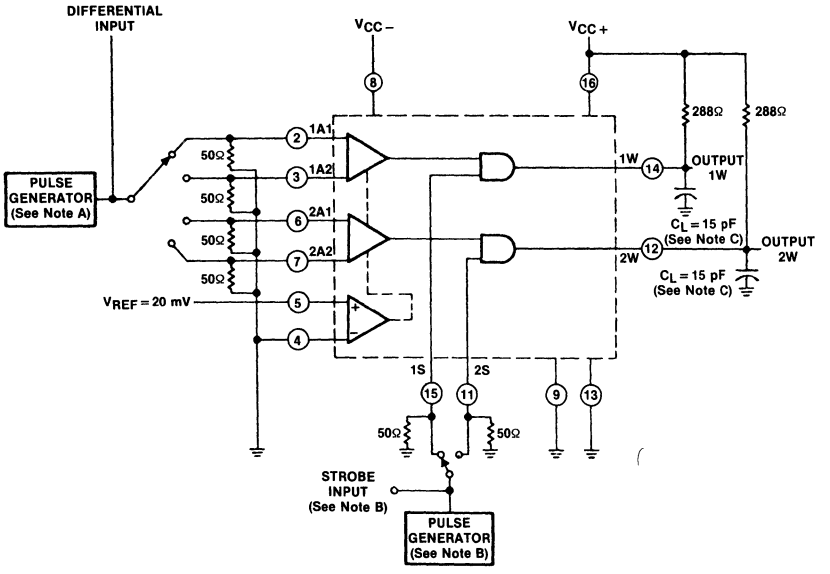
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, $t_r = 15 \pm 5$ ns, $t_f = 15 \pm 5$ ns, $t_w = 100$ ns, and PRR = 1 MHz.
B. C_L includes probe and jig capacitance.

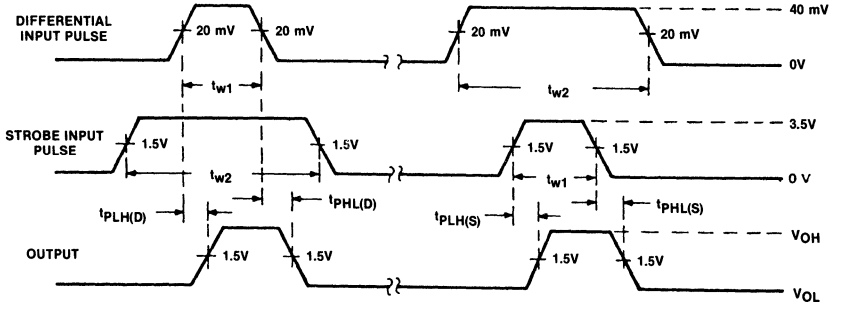
Fig. 17 55/75S20 PROPAGATION DELAY TIMES FROM GATE G_Z

CHARACTERISTICS MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Cont'd)



TEST CIRCUIT



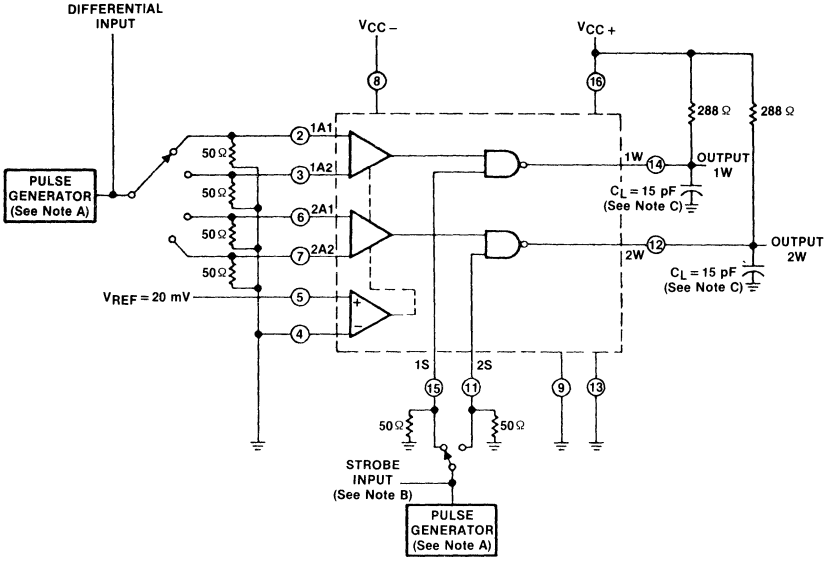
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_O = 50\ \Omega$, $t_r = 15 \pm 5$ ns, $t_f = 15 \pm 5$ ns, $t_{w1} = 100$ ns, $t_{w2} = 300$ ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.
C. C_L includes probe and jig capacitance.

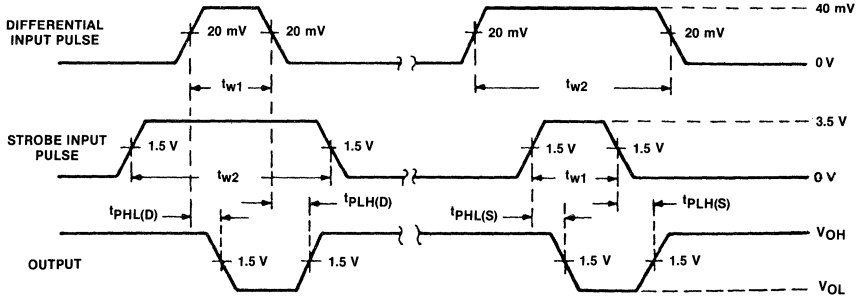
Fig. 18 55/75S24 PROPAGATION DELAY TIMES

CHARACTERISTICS MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Cont'd)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.
B. The strobe input pulse is applied to Strobe 1S when inputs 1A1-1A2 are being tested and to Strobe 2S when inputs 2A1-2A2 are being tested.
C. C_L includes probe and jig capacitance.

Fig. 19 55/75S234 PROPAGATION DELAY TIMES

5520/7520 SERIES

CORE MEMORY SENSE AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 5520/7520 Series Dual Memory Sense Amplifiers are designed for use in high speed core memory systems. These sense amplifiers detect the mV memory signals and transform them into logic levels compatible with TTL and DTL circuits. Independent strobes for each channel provide the capability for performing time discrimination, resulting in the detection of the input signal when the signal to noise ratio is at maximum. A common reference amplifier simultaneously sets the threshold of each sense amplifier, and the reference amplifier and sense amplifier are compensated to reduce the effect of power supply voltage or temperature variation. All gate inputs are compatible with TTL and DTL circuits.

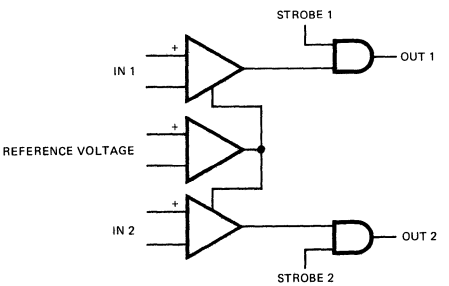
- **HIGH SPEED AND FAST RECOVERY TIME**
- **NARROW THRESHOLD UNCERTAINTY REGION**
- **ADJUSTABLE INPUT THRESHOLD VOLTAGE**
- **TTL COMPATIBLE**
- **VARIOUS LOGIC CONFIGURATIONS**

COMPARISON CHART

The 7520 series of sense amplifiers provides a wide number of options which allow this device to be adapted to a variety of special applications. Differences between the various sense amplifier devices are summarized in the table below. 55XX numbers refer to military grade devices, while the corresponding 75XX number refers to the identical circuit specified for commercial grade. Even numbered devices refer to sense amplifiers specified for a tight threshold voltage distribution.

DEVICE	DECOUPLING CAPACITOR	OUTPUT STAGE	AMPLIFIER TEST POINTS
5528/7528	External		Yes
55232/75232	Internal	Inverted with Open Collector	
55238/75238	Internal	Inverted	Yes

FUNCTIONAL BLOCK DIAGRAM



5520/7520 SERIES ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±7.0 V
Differential Input Voltage	±5.0 V
Logic Input Voltage	±5.5 V
Strobe and Gate Input Voltage	+5.0 V
Off State Output Voltage	+5.5 V
Operating Ambient Temperature Range	
5520 Series	−55°C to +125°C
7520 Series	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Hermetic DIP, (Soldering, 60 s)	+300°C
Molded DIP (Soldering, 10 s)	+260°C
Internal Power Dissipation (Note 1)	730 mW

5520/7520 SERIES RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNITS
V_{CC+}	4.75	5.0	5.25	V
V_{CC-}	−4.75	−5.0	−5.25	V
V_{REF}	15		40	mV

ELECTRICAL CHARACTERISTICS

All electrical characteristics and test conditions for the 5520 devices are identical to those of the corresponding 7520 device, with the exception of the Differential Input Threshold Voltage and Differential Input Bias Circuit. Limits for these parameters are detailed in the table below. All limits which apply to the 7520 circuits for temperatures of 0°C to 70° C apply to the 5520 circuits for the range of −55°C to +125°C.

All ac switching characteristics are guaranteed at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V and T_A = 25°C.

For details of the full electrical characteristics and test circuitry please refer to the corresponding 7520 data.

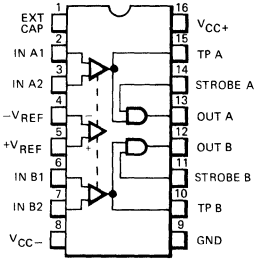
5520 SERIES V_{TH} AND I_{IB} LIMITS

SYMBOL	CHARACTERISTICS	TEST CONDITIONS		EVEN NUMBERED 5520 SERIES DEVICES			ODD NUMBERED 5520 SERIES DEVICES			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Differential Input Threshold Voltage	V_{REF} = 15 mV	T_A = −55°C to 0°C and 70°C to 125°C	10	15	20	8.0	15	22	mV
			T_A = 0°C to 70°C	11	15	19	8.0	15	22	
		V_{REF} = 40 mV	T_A = −55°C to 0°C and 70°C to 125°C	35	40	45	33	40	47	
			T_A = 0°C to 70°C	36	40	44	33	40	47	
I_{IB}	Differential Input Bias Current	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0	T_A = −55°C to 0°C			100			100	μA
			T_A = 0°C to 125°C		30	75		30	75	

NOTES:
1. Derate Hermetic DIP and Molded DIP above 60°C at 8.3 mW/°C.
2. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic-gate threshold voltage level.

7528
SENSE AMPLIFIERS

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
5528	5528DM
7528	7528DC
7528	7528PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	H
L	X	L
X	L	L

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{REF} = 15 mV	11	15	19	mV
			V_{REF} = 40 mV	36	40	44	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{REF} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns		±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3		2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3				0.8	V
V_{OH}	Output HIGH Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA	2.4	4.0		V
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V			1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V		−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V	−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C		25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

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7528
SENSE AMPLIFIERS

AC CHARACTERISTICS: $V_{CC+} = 5.0$ V, $V_{CC-} = -5.0$ V, $T_A = 25°C$

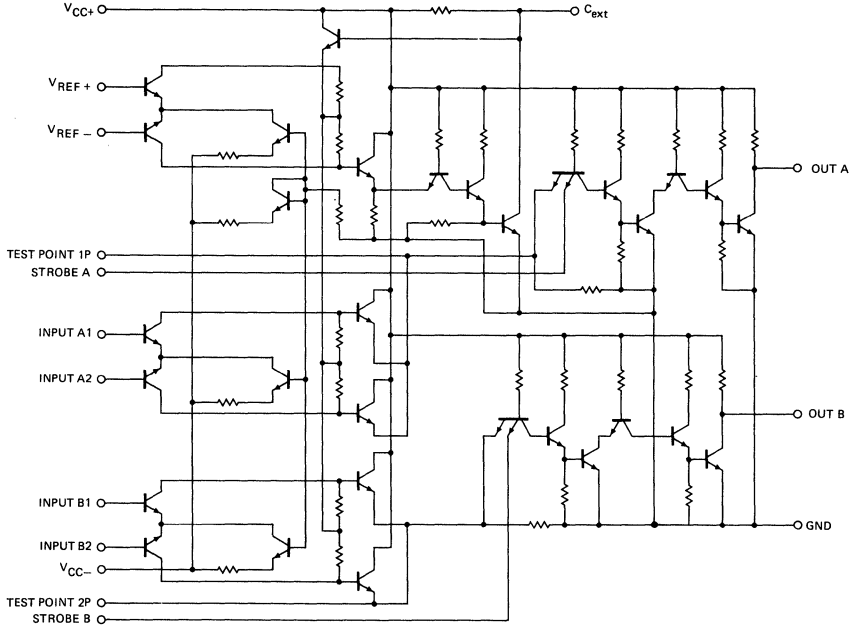
PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1-A2	A	7	$C_L = 15$ pF, $R_L = 288\ \Omega$		25	40	ns
$t_{PHL(D)}$						20		
$t_{PHL(D)}$	STROBE	A	7	$C_L = 15$ pF, $R_L = 288\ \Omega$		15	30	ns
$t_{PHL(S)}$						20		

TYPICAL RECOVERY AND CYCLE TIMES: $V_{CC+} = 5.0$ V, $V_{CC-} = -5.0$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: $V_{ID} = 2.0$ V, $t_f = 20$ ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: $V_{IC} = \pm 2.0$ V, $t_r = t_f = 20$ ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

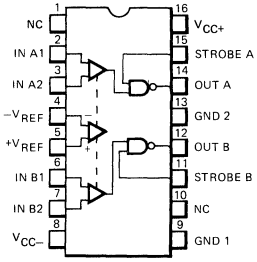
NOTES:
5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

7528
EQUIVALENT CIRCUIT



75232
SENSE AMPLIFIERS

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
55232	55232DM
75232	75232DC
75232	75232PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	L
L	X	H
X	L	H

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{REF} = 15 mV	11	15	19	mV
			V_{REF} = 40 mV	36	40	44	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{REF} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns		±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3		2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3				0.8	V
I_{OH}	Output HIGH Current	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, V_{OH} = 5.25 V			250	μA
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V			1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V		−1.0	−1.6	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C		25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

8

75232
SENSE AMPLIFIERS

AC CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

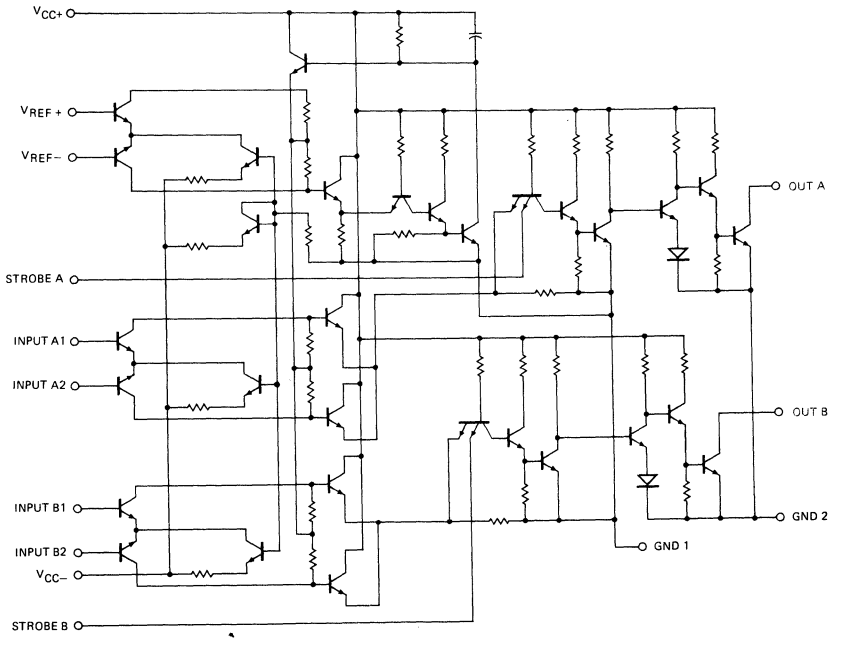
PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1-A2	A	7	C_L = 15 pF, R_L = 230 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PHL(D)}$	STROBE	A	7	C_L = 15 pF, R_L = 230 Ω		25		ns
$t_{PHL(S)}$						15	30	

TYPICAL RECOVERY AND CYCLE TIMES: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: V_{ID} = 2.0 V, $t_r = t_f$ = 20 ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: V_{IC} = ±2.0 V, $t_r = t_f$ = 20 ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

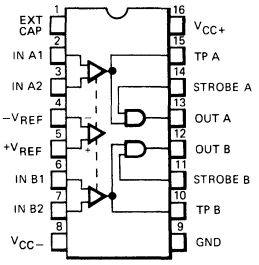
NOTES:
5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

75232
EQUIVALENT CIRCUIT



75238
SENSE AMPLIFIERS

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
55238	55238DM
75238	75238DC
75238	75238PC

FUNCTION TABLE

INPUTS		OUTPUT
A	S	A
H	H	L
L	X	H
X	L	H

DEFINITION OF LOGIC LEVELS

INPUT	H	L	X
A†	$V_{ID} \geq V_{T(MAX)}$	$V_{ID} \leq V_{T(MIN)}$	Irrelevant
S	$V_I \geq V_{IH(MIN)}$	$V_I \leq V_{IL(MAX)}$	Irrelevant

†A is a differential voltage (V_{ID}) between A1 and A2. For these circuits, V_{ID} is considered positive regardless of which terminal is positive with respect to the other.

ELECTRICAL CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNITS
V_T	Differential Input Threshold Voltage (See Note 3)	1	V_{REF} = 15 mV	11	15	19	mV
			V_{REF} = 40 mV	36	40	44	
V_{ICF}	Common Mode Input Firing Voltage (See Note 4)	None	V_{REF} = 40 mV, $V_{I(S)} = V_{IH}$ Common-Mode Input Pulse: $t_r \leq 15$ ns, $t_f \leq 15$ ns, t_w = 50 ns		±2.5		V
I_{IB}	Differential Input Bias Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		30	75	μA
I_{IO}	Differential Input Offset Current	2	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{ID} = 0		0.5		μA
V_{IH}	Input HIGH Voltage (Strobe Inputs)	3		2.0			V
V_{IL}	Input LOW Voltage (Strobe Inputs)	3				0.8	V
V_{OH}	Output HIGH Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OH} = −400 μA	2.4	4.0		V
V_{OL}	Output LOW Voltage	3	V_{CC+} = 4.75 V, V_{CC-} = −4.75 V, I_{OL} = 16 mA		0.25	0.4	V
I_{IH}	Input HIGH Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 2.4 V			40	μA
			V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IH} = 5.25 V			1.0	mA
I_{IL}	Input LOW Current (Strobe Inputs)	4	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, V_{IL} = 0.4 V		−1.0	−1.6	mA
I_{OS}	Short-Circuit Output Current	5	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V	−2.1		−3.5	mA
I_{CC+}	Supply Current from V_{CC+}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C		25	40	mA
I_{CC-}	Supply Current from V_{CC-}	6	V_{CC+} = 5.25 V, V_{CC-} = −5.25 V, T_A = 25°C		−15	−20	mA

‡All typical values are at V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C.

NOTES:
3. The differential input threshold voltage (V_T) is defined as the dc differential input voltage (V_{ID}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
4. Common mode input firing voltage is the minimum common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable pulse present.

75238
SENSE AMPLIFIERS

AC CHARACTERISTICS: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

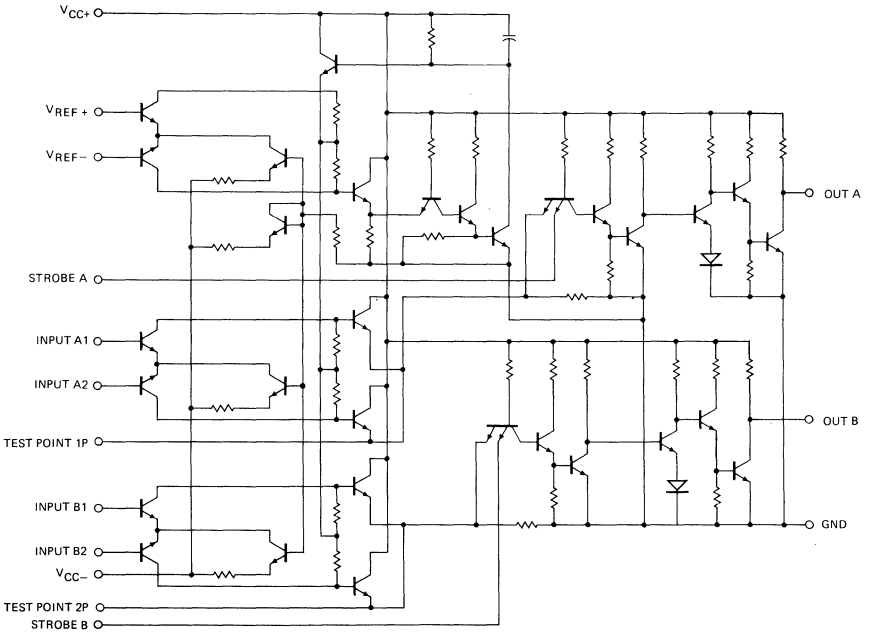
PROPAGATION DELAY TIMES			TEST	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYMBOL	FROM INPUT	TO OUTPUT	FIGURE					
$t_{PLH(D)}$	A1-A2	A	7	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(D)}$						25	40	
$t_{PHL(D)}$	STROBE	A	7	C_L = 15 pF, R_L = 288 Ω		25		ns
$t_{PHL(S)}$						15	30	

TYPICAL RECOVERY AND CYCLE TIMES: V_{CC+} = 5.0 V, V_{CC-} = −5.0 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{orD}	Differential Input Overload Recovery Time (See Note 5)	Differential Input Pulse: V_{ID} = 2.0 V, t_f = 20 ns		20		ns
t_{orC}	Common Mode Input Overload Recovery Time (See Note 6)	Common Mode Input Pulse: V_{IC} = ±2.0 V, t_r = t_f = 20 ns		20		ns
$t_{cyc(MIN)}$	Minimum Cycle Time			200		ns

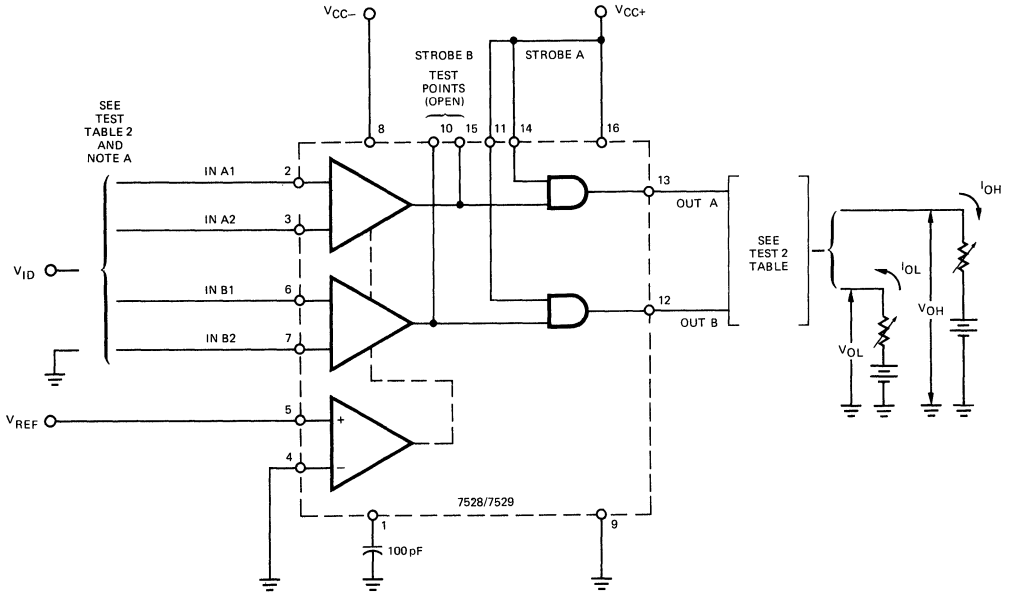
NOTES:
5. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
6. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

75238
EQUIVALENT CIRCUIT



DC TEST CIRCUITS (Cont'd)

7528



TEST TABLE

CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUTS		
				V_O	I_{OH}	I_{OL}
7528	A1-A2 AND B1-B2	15 mV	≤11 mV	≤0.4 V		16 mA
		15 mV	≥19 mV	≥2.4 V	−400 μA	
		40 mV	≤36 mV	≤0.4 V		16 mA
		40 mV	≥44 mV	≥2.4 V	−400 μA	

NOTE A: Each pair of inputs is tested separately with its corresponding output.
Each pair of differential inputs is tested separately with the other pair grounded.

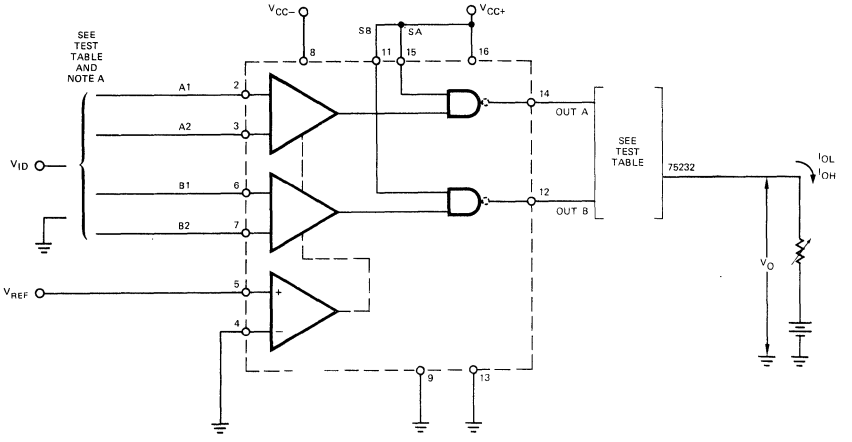
Fig. 1a – 7528 V_T

8

DC TEST CIRCUITS (Cont'd)

75232

PARAMETER MEASUREMENT INFORMATION



TEST TABLE

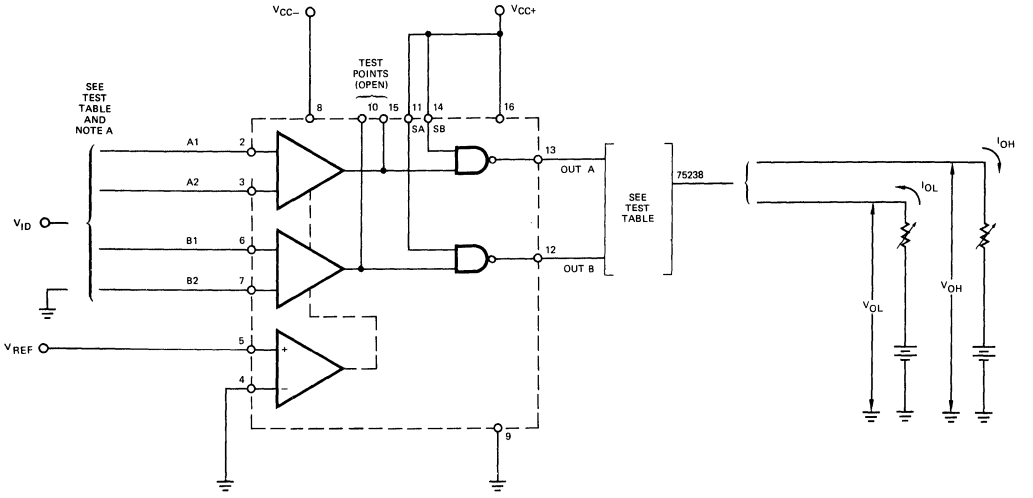
CIRCUIT TYPE	INPUTS	V_{ref}	V_{ID}	OUTPUTS 75232		
				V_O	I_{OH}	I_{OL}
75232	A1-A2	15 mV	≤11 mV	5.25 V	≤250 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	5.25 V	≤250 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

Fig. 1b – 75232 V_T

DC TEST CIRCUITS (Cont'd)

75238



TEST TABLE

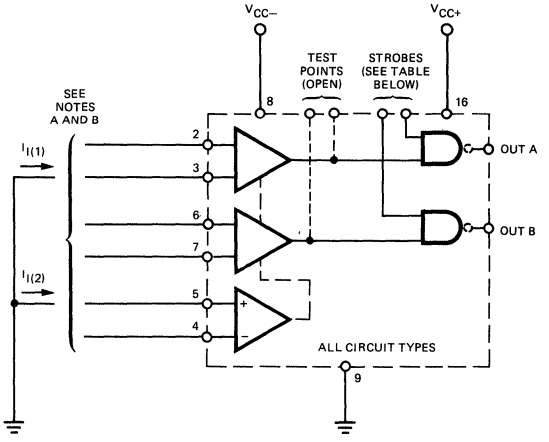
CIRCUIT TYPES	INPUTS	V_{ref}	V_{ID}	OUTPUTS 75238		
				V_O	I_{OH}	I_{OL}
75238	A1-A2	15 mV	≤11 mV	≥2.4 V	−400 μA	
	A1-A2	15 mV	≥19 mV	≤0.4 V		16 mA
	A1-A2	40 mV	≤36 mV	≥2.4 V	−400 μA	
	A1-A2	40 mV	≥44 mV	≤0.4 V		16 mA

NOTE A: Each pair of differential inputs is tested separately with its corresponding output.

Fig. 1c – 75238 V_T

DC TEST CIRCUITS (Cont'd)

ALL CIRCUIT TYPES



PIN CONNECTIONS (Other than those shown above)

CIRCUIT TYPES	100 pF TO GROUND	APPLY GROUND	LEAVE OPEN
7528	External Capacitor (Pin 1)	Strobes A and B (Pins 14, 11)	Test Points 1 and 2 Outputs A and B (Pins 15, 10, 13, 12)
75232	Not Required	Strobes A and B Ground 2 (Pins 15, 11, 13)	Outputs A and B (Pins 14, 12)
75238	Not Required	Strobes A and B (Pins 14, 11)	Test Points 1 and 2 Outputs A and B (Pins 15, 10, 13, 12)

NOTES:
A. Each preamplifier is tested separately. Inputs not under test are grounded.
B. $I_{IB} = I_{I(1)}$ or $I_{I(2)}$ (limit applies to each): $I_{IO} = I_{I(1)} - I_{I(2)}$; $I_{I(1)}$ and $I_{I(2)}$ are the currents into the two inputs of the pair under test.

Fig. 2 – I_{IB}, I_{IO}

DC TEST CIRCUITS (Cont'd)

75232

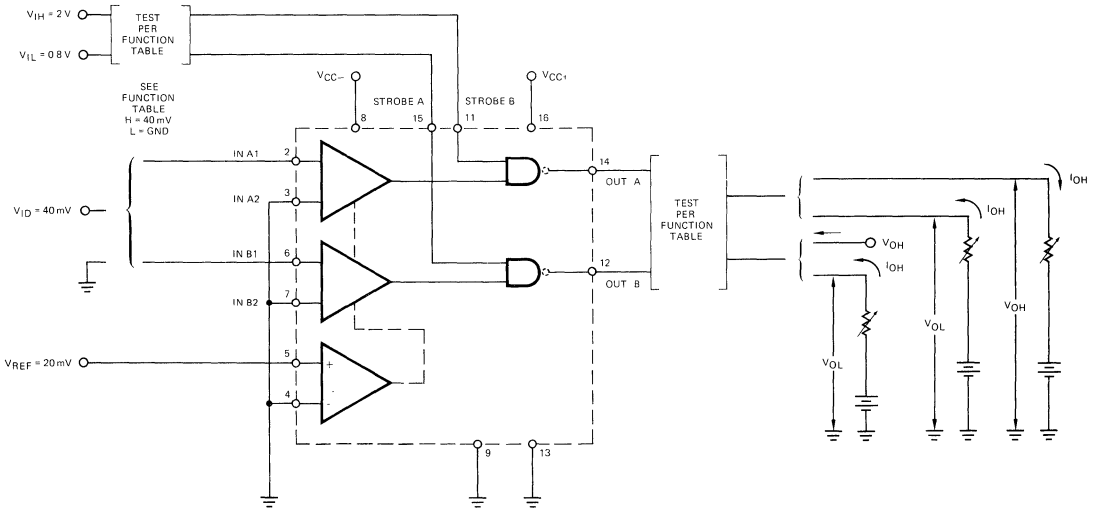
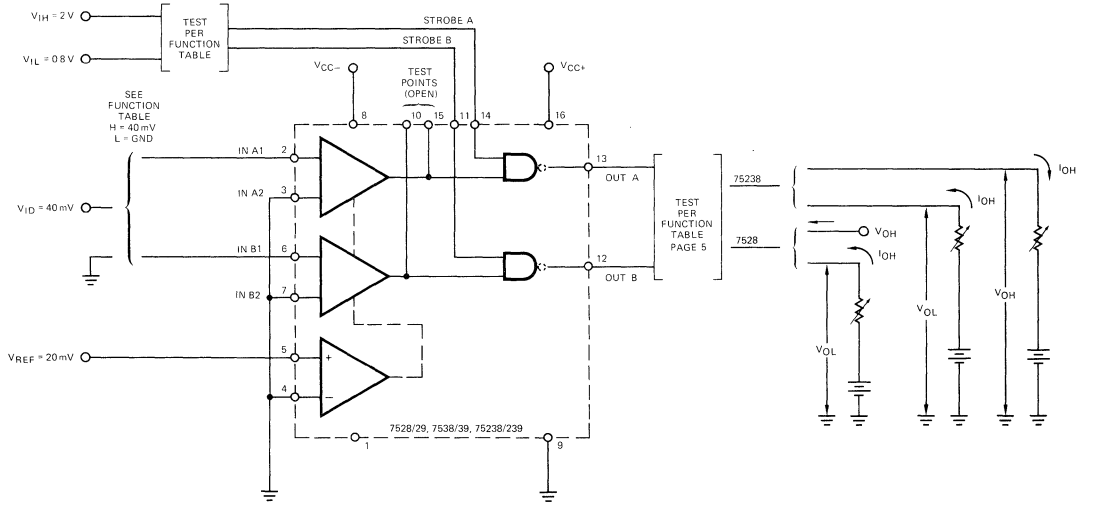


Fig. 3a – 75232 V_{IH}, V_{IL}, V_{OH}, V_{OL}

8

7528/75238

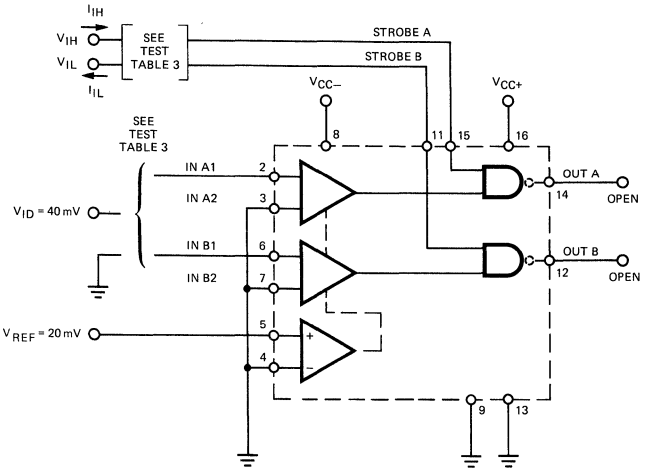


*Required for 7528

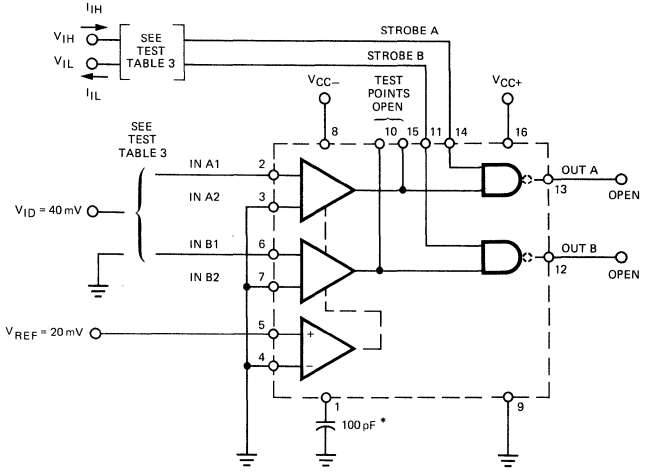
Fig. 3B – V_{IH}, V_{IL}, V_{OH}, V_{OL}

DC TEST CIRCUITS (Cont'd)

75232



7528/75238



*Required for 7528

TEST TABLE 3

TEST	INPUT A1	INPUT B1	STROBE A	STROBE B
I_{IH} at Strobe A	GND	GND	V_{IH}	V_{IL}
I_{IH} at Strobe B	GND	GND	V_{IL}	V_{IH}
I_{IL} at Strobe A	V_{ID}	GND	V_{IL}	V_{IL}
I_{IL} at Strobe B	GND	V_{ID}	V_{IL}	V_{IL}

Fig. 4 – I_{IH}, I_{IL}

DC TEST CIRCUITS (Cont'd)

7528

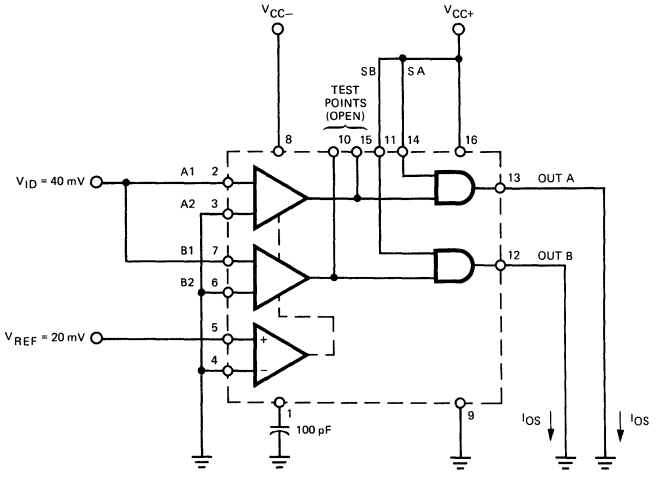


Fig. 5a – I_{OS}

75238

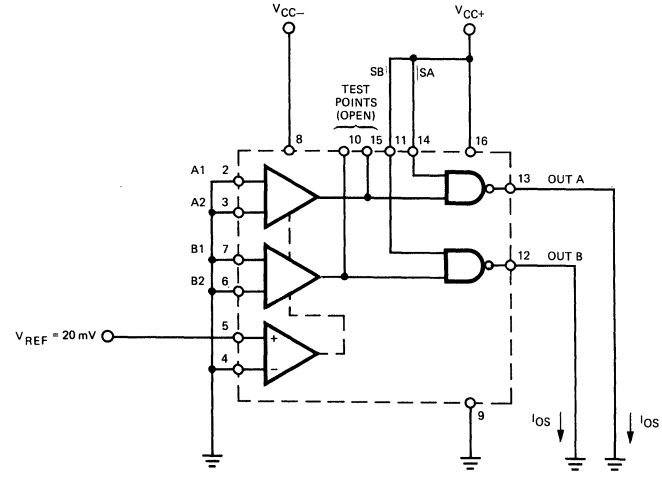
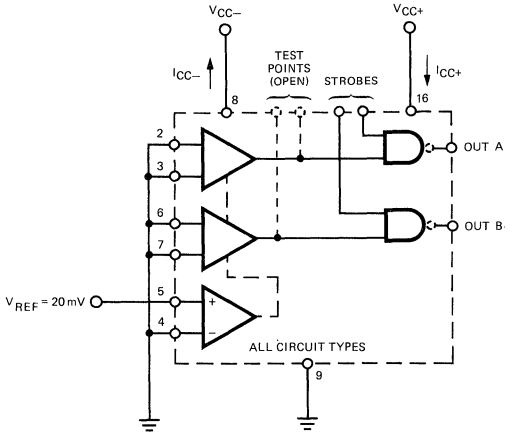


Fig. 5b – I_{OS}

DC TEST CIRCUITS (Cont'd)

ALL CIRCUIT TYPES



*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PIN CONNECTIONS (Other than those shown above)

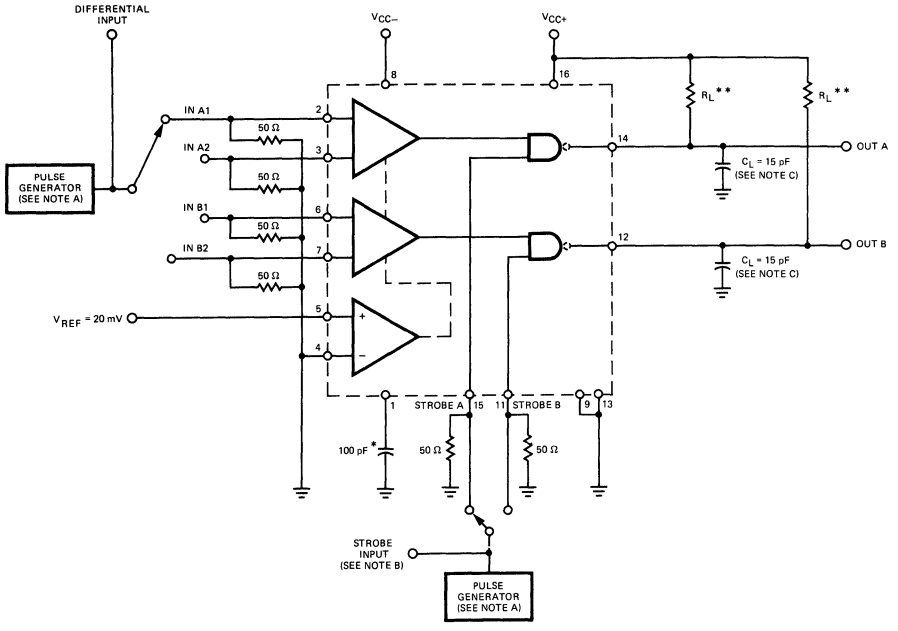
CIRCUIT TYPES	APPLY GROUND	LEAVE OPEN
75232	Strobes A and B Ground 2 (Pins 15, 11, 13)	Outputs A and B (Pins 14, 12)
75238	Strobes A and B (Pins 14, 11)	Test Points 1 and 2 Outputs A and B (Pins 15, 10, 13, 12)
7528	Strobes A and B (Pins 14, 11) 100 pF to GND	Test Points 1 and 2 (Pins 15, 10, 13, 12)

Fig. 6 – I_{CC+}, I_{CC-}

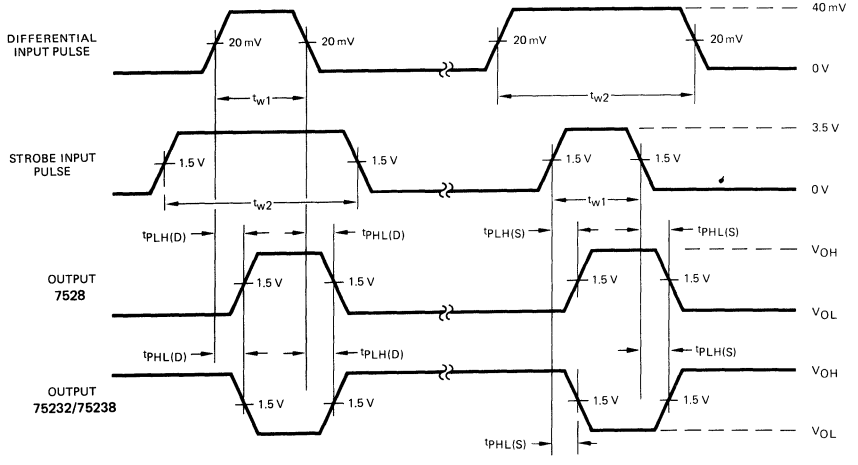
PROPAGATION DELAY TIME

ALL CIRCUITS

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:

A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 15 ± 5 ns, t_f = 15 ± 5 ns, t_{w1} = 100 ns, t_{w2} = 300 ns, and PRR = 1 MHz.

B. The strobe input pulse is applied to strobe A when inputs A1-A2 are being tested and to strobe B when inputs B1-B2 are being tested.

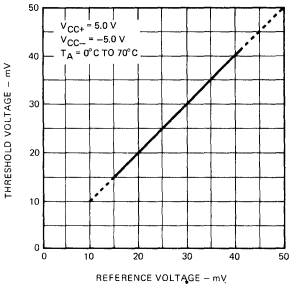
C. C_L includes probe and jig capacitance.

*Required for 7528.

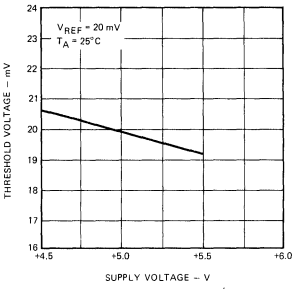
Fig. 7

TYPICAL PERFORMANCE CURVES

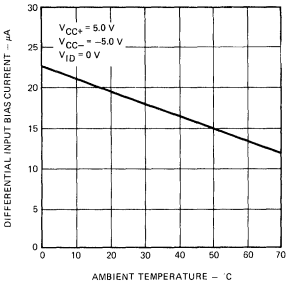
THRESHOLD VOLTAGE AS A FUNCTION OF REFERENCE VOLTAGE



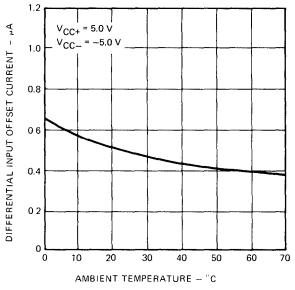
THRESHOLD VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



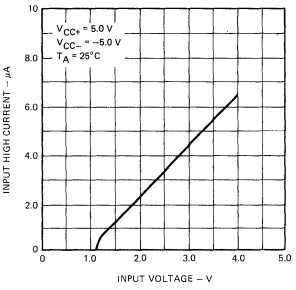
DIFFERENTIAL INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



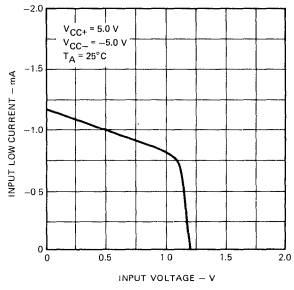
DIFFERENTIAL INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



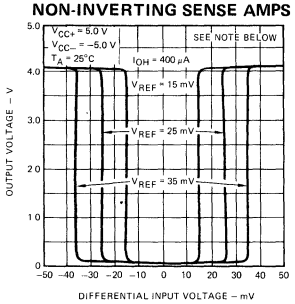
INPUT HIGH CURRENT AS A FUNCTION OF INPUT VOLTAGE



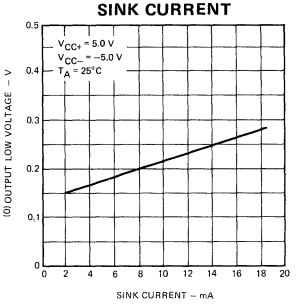
INPUT LOW CURRENT AS A FUNCTION OF INPUT VOLTAGE



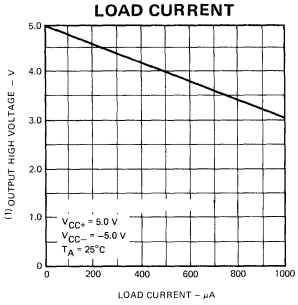
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE FOR ALL NON-INVERTING SENSE AMPS



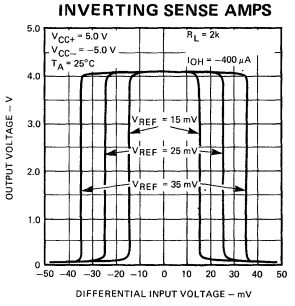
OUTPUT LOW VOLTAGE AS A FUNCTION OF SINK CURRENT



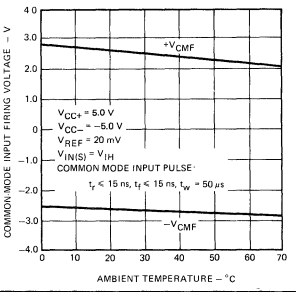
OUTPUT HIGH VOLTAGE AS A FUNCTION OF LOAD CURRENT



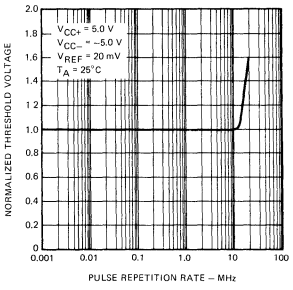
OUTPUT VOLTAGE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE FOR ALL INVERTING SENSE AMPS



COMMON MODE FIRING VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



NORMALIZED THRESHOLD VOLTAGE AS A FUNCTION OF PULSE REPETITION RATE



55325•75325
MEMORY DRIVER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION—The 55325 and 75325 are Memory Drivers for use in magnetic memories constructed on a silicon chip using the Fairchild Planar* process. The device contains four 600 mA switches, two source switches and two sink switches that can be selected by the appropriate logic input and appropriate strobe. The device has adequate base drive to source currents up to 375 mA with V_{CC2} of 15 V or 600 mA with V_{CC2} voltage of 24 V. In applications requiring drive to source currents greater than 375 mA, an external resistor may be used to regulate the source base current to within ±5% and reduce the power dissipation to allow higher source currents at higher ambient temperatures.

Internal voltage surge protection of each of the output sink transistors is provided for switching inductive loads.

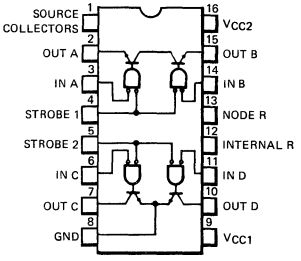
- **600 mA OUTPUT CAPABILITY**
- **FAST SWITCH TIMES**
- **OUTPUT SHORT- CIRCUIT CURRENT**
- **DUAL SINK AND DUAL SOURCE OUTPUTS**
- **MINIMUM TIME SKEW BETWEEN ADDRESS AND OUTPUT CURRENT RISE**
- **24 V CAPABILITY**
- **TTL OR DTL COMPATIBLE**
- **SOURCE BASE DRIVE EXTERNALLY ADJUSTABLE**
- **INPUT CLAMP DIODES**

POSITIVE LOGIC TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS (Note 3)			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
IN A	IN B	IN C	IN D	S1	S2	A	B	C	D
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = HIGH Level, L = LOW Level, X = Don't Care

CONNECTION DIAGRAMS
16-PIN
(TOP VIEW)
PACKAGE OUTLINES 7B 9B 4L
PACKAGE CODES D P F

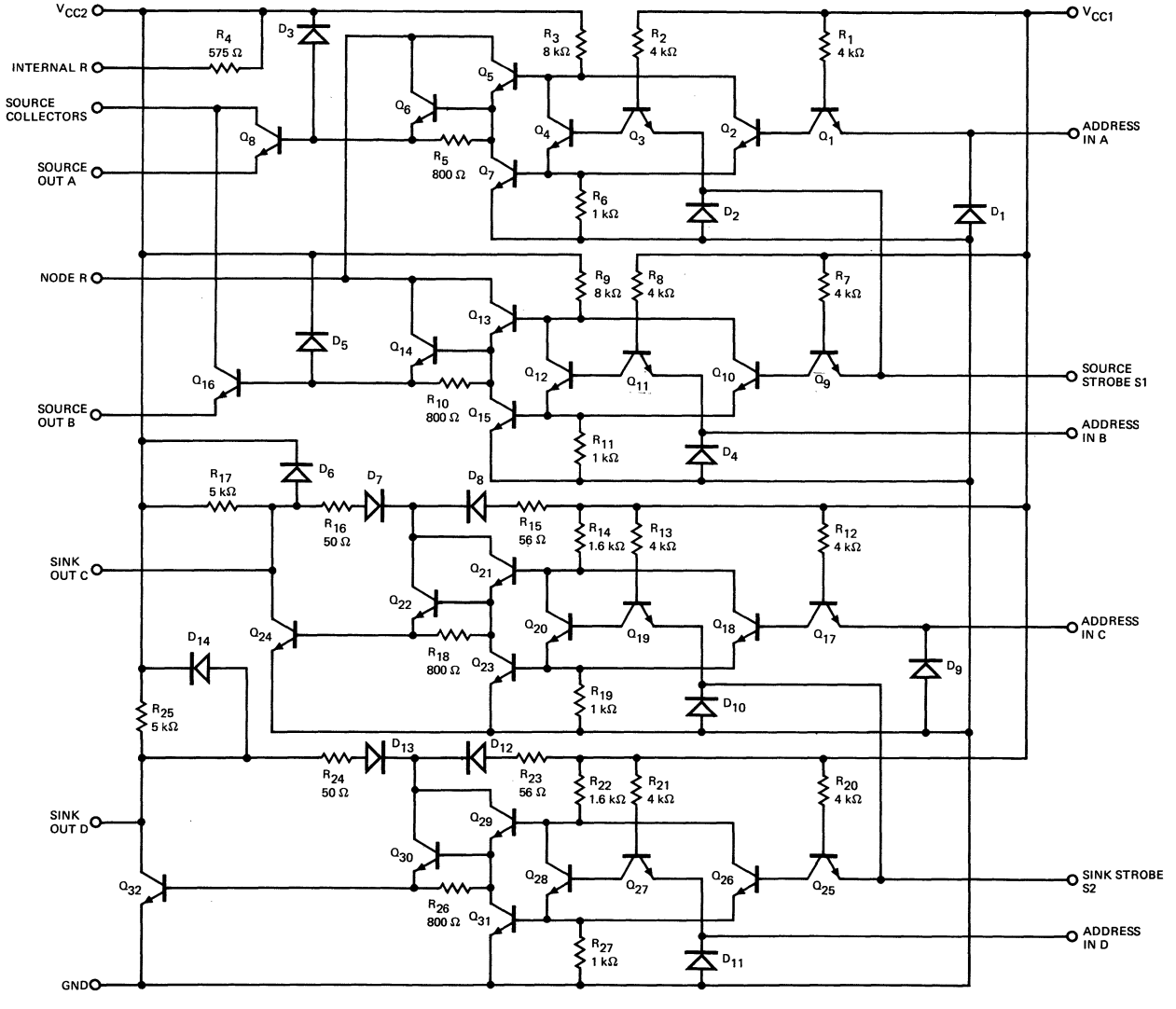


ORDER INFORMATION

TYPE	PART NO.
55325	55325DM
75325	75325DC
55325	55325FM
75325	75325PC

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC1} (Note 1)	+7.0 V
Supply Voltage V_{CC2} (Note 1)	+25 V
Input Voltage (Any Address or Strobe Input)	+5.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
55325	−55°C to +125°C
75325	0°C to +70°C
Internal Power Dissipation (Note 2)	1 W
Pin Temperature	
Hermetic DIP (Soldering, 60 s)	300°C
Molded DIP (Soldering, 10 s)	260°C

55325

ELECTRICAL CHARACTERISTICS: Ratings apply for $-55°C \leq T_A \leq 125°C$, unless otherwise specified.

SYMBOL	CHARACTERISTICS		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage		Fig. 1 & 2		2.0			V
V_{IL}	Input LOW Voltage		Fig. 3 & 4				0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{IN} = −10 mA, T_A = 25°C Fig. 5			−1.3	−1.7	V
I_{OFF}	Source-collectors Terminal Off-State Current		V_{CC1} = 4.5 V, V_{CC2} = 24 V Fig. 1	Full Range			500	μA
				T_A = 25°C		3.0	150	
V_{OH}	Sink Output HIGH Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{OUT} = 0, Fig. 2		19	23		V
V_{SAT}	Saturation Voltage	Source Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{source} \approx$ −600 mA See Notes 3 & 4, and Fig. 3	Full Range			0.9	V
				T_A = 25°C		0.43	0.7	
		Sink Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{sink} \approx$ 600 mA See Notes 3 & 4 and Fig. 4	Full Range			0.9	V
				T_A = 25°C		0.43	0.7	
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 5.5 V, Fig. 5				1.0	mA
		Strobe Inputs					2.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 2.4 V, Fig. 5			3.0	40	μA
		Strobe Inputs				6.0	80	
I_{IL}	Input LOW Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 0.4 V, Fig. 5			−1.0	−1.6	mA
		Strobe Inputs				−2.0	−3.2	
$I_{CC(off)}$	Supply Current, All Sources and Sinks Off	From V_{CC1}	V_{CC1} = 5.5 V, V_{CC2} = 24 V T_A = 25°C, Fig. 6			14	22	mA
		From V_{CC2}				7.5	20	
I_{CC1}	Supply Current from V_{CC1}, Either Sink On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{sink} = 50 mA, T_A = 25°C Fig. 7			55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{source} = −50 mA, T_A = 25°C Fig. 8			32	50	mA

NOTES:

1. Voltage values are with respect to network ground terminal.
2. Refer to Dissipation Derating Curve, Figure 13.
3. Not more than one output is to be on at any one time.
4. Parameters measured using the following pulse techniques; t_W = 200 μs, duty cycle ≤ 2%.

8

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ELECTRICAL CHARACTERISTICS: Rating apply for $0°C \leq T_A \leq 70°C$ unless otherwise specified.

SYMBOL	CHARACTERISTICS		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input HIGH Voltage		Fig. 1 & 2		2.0			V
V_{IL}	Input LOW Voltage		Fig. 3 & 4				0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{IN} = −10 mA, T_A = 25°C Fig. 5			−1.3	−1.7	V
I_{OFF}	Source-collectors Terminal Off-State Current		V_{CC1} = 4.5 V, V_{CC2} = 24 V Fig. 1	Full Range			200	μA
				T_A = 25°C		3.0	200	
V_{OH}	Sink Output HIGH Voltage		V_{CC1} = 4.5 V, V_{CC2} = 24 V I_{OUT} = 0, Fig. 2		19	23		V
V_{SAT}	Saturation Voltage	Source Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{source} \approx$ −600 mA See Notes 3 & 4, and Fig. 3	Full Range			0.9	V
				T_A = 25°C		0.43	0.75	
		Sink Outputs	V_{CC1} = 4.5 V, V_{CC2} = 15 V R_L = 24 Ω, $I_{sink} \approx$ 600 mA See Notes 3 & 4, and Fig. 4	Full Range			0.9	V
				T_A = 25°C			0.75	
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 5.5 V, Fig. 5				1.0	mA
		Strobe Inputs					2.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 2.4 V, Fig. 5			3.0	40	μA
		Strobe Inputs				6.0	80	
I_{IL}	Input LOW Current	Address Inputs	V_{CC1} = 5.5 V, V_{CC2} = 24 V V_{IN} = 0.4 V, Fig. 5			−1.0	−1.6	mA
		Strobe Inputs				−2.0	−3.2	
$I_{CC(off)}$	Supply Current, All Sources and Sinks Off	From V_{CC1}	V_{CC1} = 5.5 V, V_{CC2} = 24 V T_A = 25°C, Fig. 6			14	22	mA
		From V_{CC2}				7.5	20	
I_{CC1}	Supply Current from V_{CC1}, Either Sink On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{sink} = 50 mA, T_A = 25°C Fig. 7			55	70	mA
I_{CC2}	Supply Current from V_{CC2}, Either Source On		V_{CC1} = 5.5 V, V_{CC2} = 24 V I_{source} = −50 mA, T_A = 25°C Fig. 8			32	50	mA

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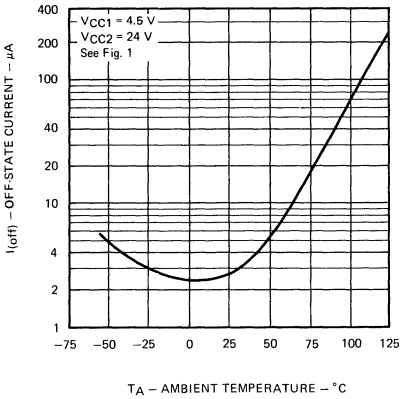
SWITCHING CHARACTERISTICS: V_{CC1} = 5.0 V, T_A = 25°C (See Test Circuit Figures 9 and 10)

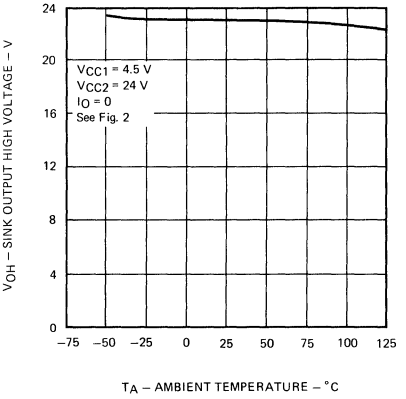
SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time to Source Collectors	9	V_{CC2} = 15 V, R_L = 24 Ω C_L = 25 pF		25	50	ns
t_{PHL}					25	50	
t_{TLH}	Transition Time to Source Outputs	10	V_{CC2} = 20 V, R_L = 1 kΩ C_L = 25 pF		55		ns
t_{THL}					7.0		
t_{PLH}	Propagation Delay Time to Sink Outputs	9	V_{CC2} = 15 V, R_L = 24 Ω C_L = 25 pF		20	45	ns
t_{PHL}					20	45	
t_{TLH}	Transition Time to Sink Outputs	9	V_{CC2} = 15 V, R_L = 24 Ω C_L = 25 pF		7.0	15	ns
t_{THL}					9.0	20	
t_s	Storage Time to Sink Outputs	9	V_{CC2} = 15 V, R_L = 24 Ω C_L = 25 pF		15	30	ns

TYPICAL PERFORMANCE CURVES

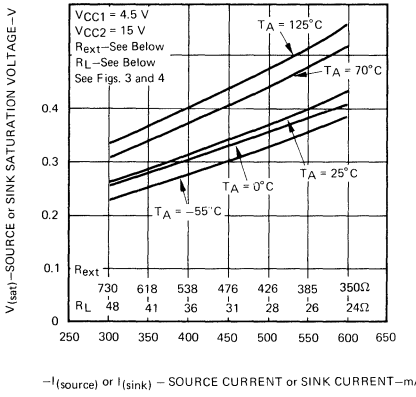
OFF-STATE CURRENT INTO SOURCE COLLECTORS AS A FUNCTION OF AMBIENT TEMPERATURE



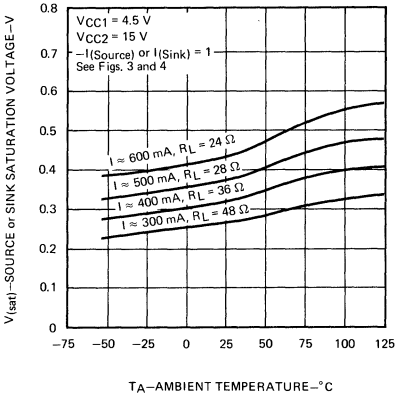
SINK OUTPUT HIGH VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



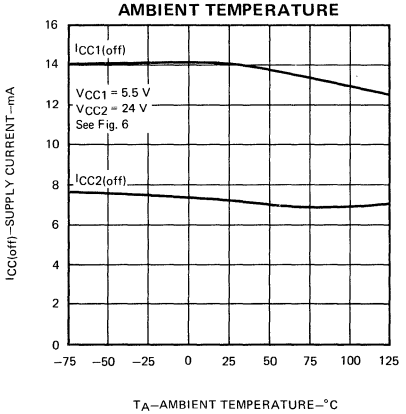
SOURCE OR SINK SATURATION VOLTAGE AS A FUNCTION OF SOURCE CURRENT OR SINK CURRENT



SOURCE OR SINK SATURATION VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



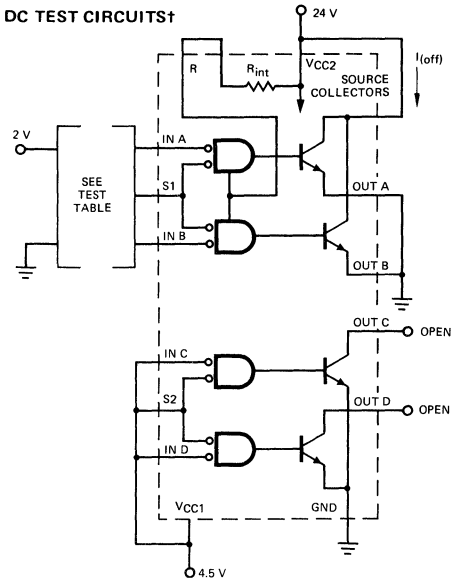
SUPPLY CURRENT, ALL SOURCES AND SINKS OFF AS A FUNCTION OF AMBIENT TEMPERATURE



8

PARAMETER MEASUREMENT INFORMATION

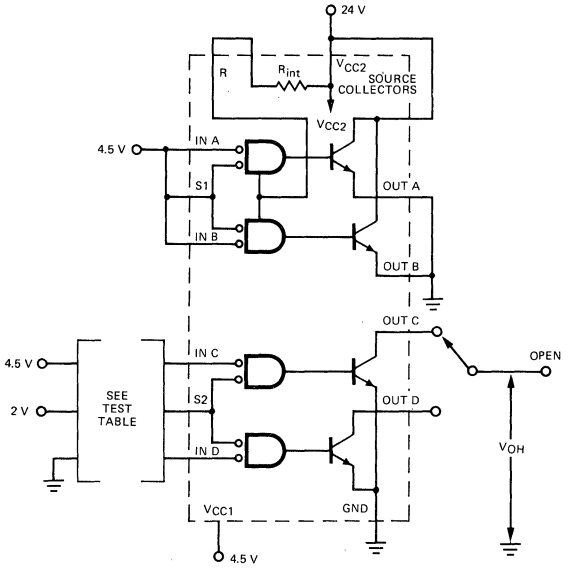
DC TEST CIRCUITS†



TEST TABLE

A	B	S1
GND	GND	2 V
2 V	2 V	GND

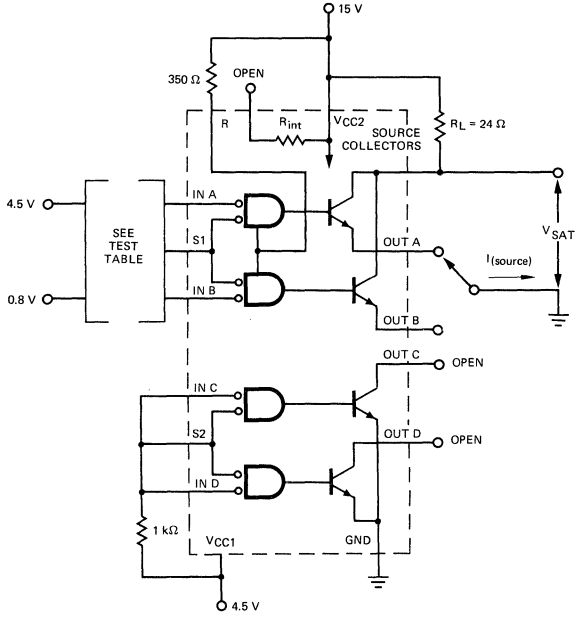
Fig. 1 $I_{(OFF)}$ AND V_{IH}



TEST TABLE

C	D	S2	OUT C	OUT D
2 V	4.5 V	GND	V_{OH}	OPEN
GND	4.5 V	2 V	V_{OH}	OPEN
4.5 V	2 V	GND	OPEN	V_{OH}
4.5 V	GND	2 V	OPEN	V_{OH}

Fig. 2 V_{IH} AND V_{OH}



TEST TABLE

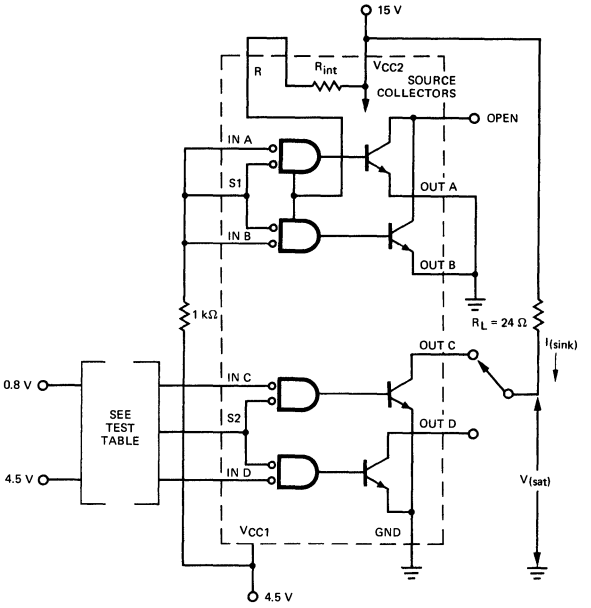
A	B	S1	OUT A	OUT B
0.8 V	4.5 V	0.8 V	GND	OPEN
4.5 V	0.8 V	0.8 V	OPEN	GND

Fig. 3 V_{IL} AND SOURCE $V_{(sat)}$ (Note 4)

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

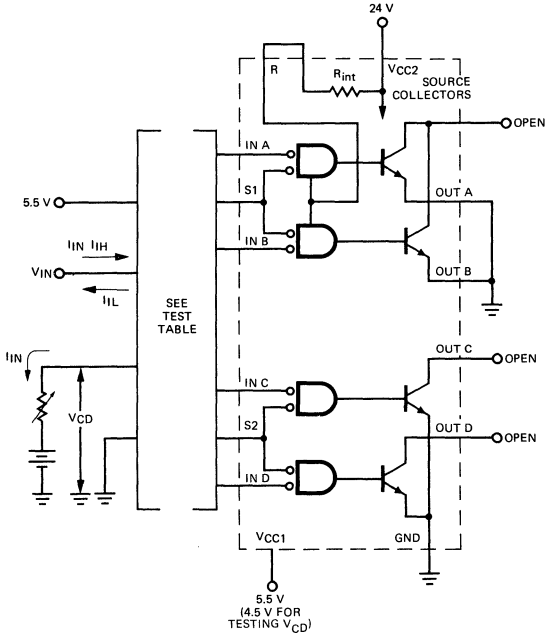
DC TEST CIRCUITS (Cont'd)



TEST TABLE

C	D	S2	OUT C	OUT D
0.8 V	4.5 V	0.8 V	R_L	OPEN
4.5 V	0.8 V	0.8 V	OPEN	R_L

Fig. 4 V_{IL} AND SINK $V_{(sat)}$ (Note 4)



TEST TABLES

I_I, I_{IH}

APPLY V_{IN} = 5.5 V, MEASURE I_{IN} / APPLY V_{IN} = 2.4 V, MEASURE I_{IH}	GROUND	APPLY 5.5 V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_{IN} = 0.4 V, MEASURE I_{IL} / APPLY I_{IN} = −10 mA MEASURE V_{CD}	APPLY 5.5 V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

Fig. 5 V_{CD}, I_{IN}, I_{IH}, AND I_{IL}

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS (Cont'd)

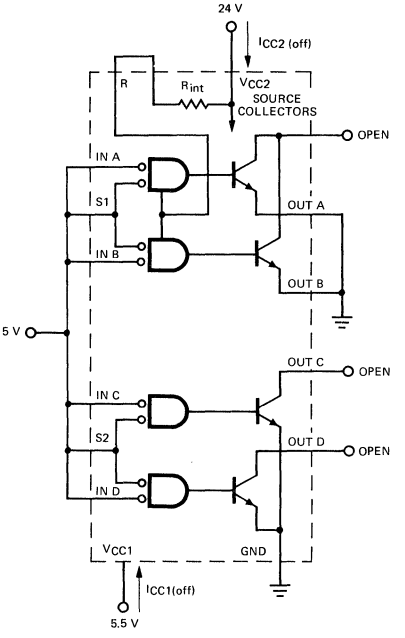
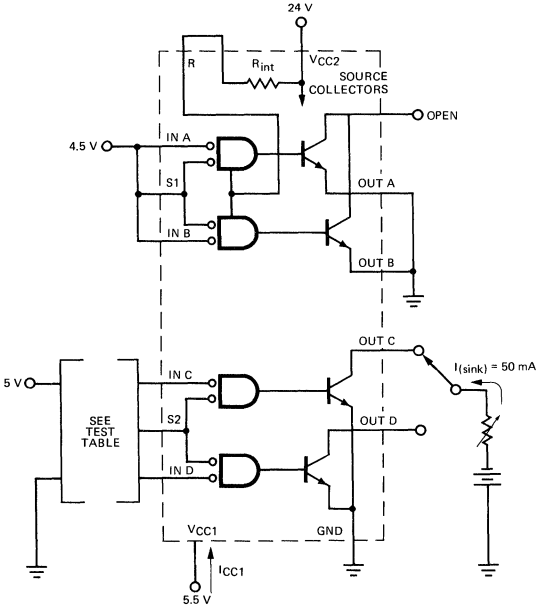


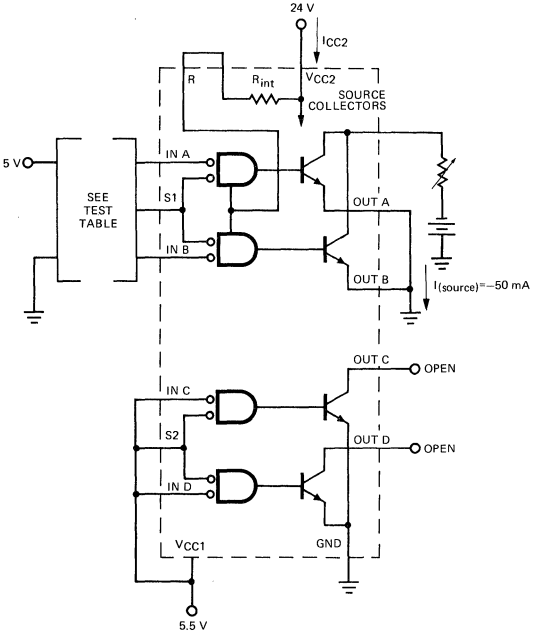
Fig. 6 $I_{CC1(OFF)}$ AND $I_{CC2(OFF)}$



TEST TABLE

C	D	S2	OUT C	OUT D
GND	5 V	GND	I(sink)	OPEN
5 V	GND	GND	OPEN	I(sink)

Fig. 7 I_{CC1}, EITHER SINK ON



TEST TABLE

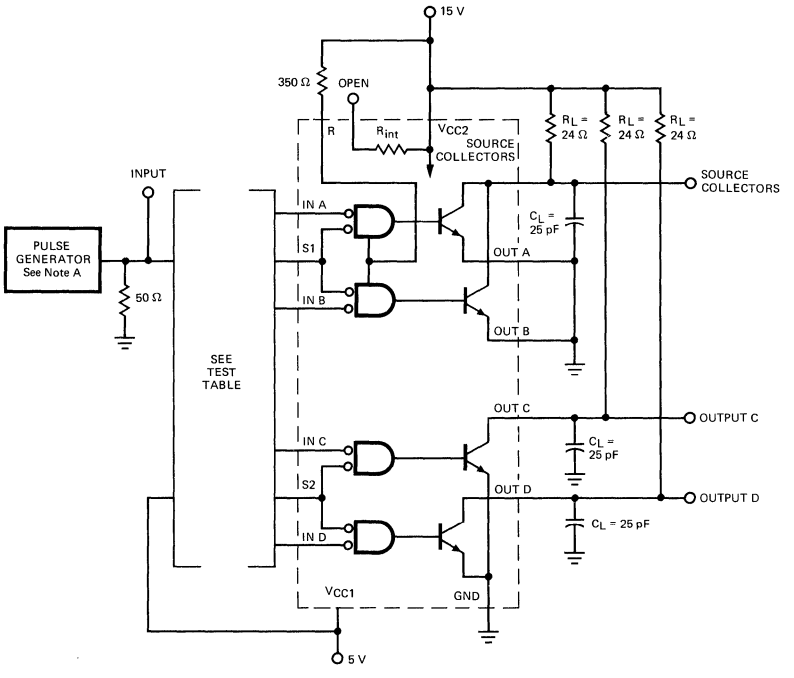
A	B	S1
GND	5 V	GND
5 V	GND	GND

Fig. 8 I_{CC2}, EITHER SOURCE ON

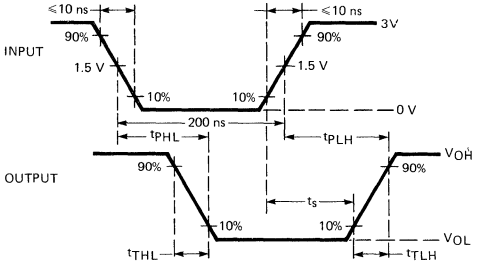
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



VOLTAGE WAVEFORMS



TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink Output C	C and S2	A, B, D and S1
	Sink Output D	D and S2	A, B, C and S1

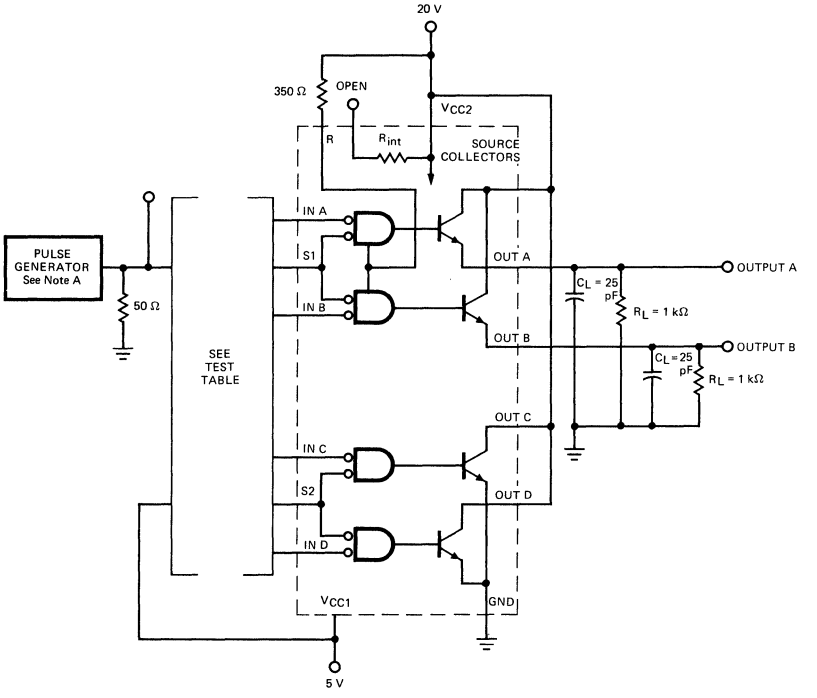
NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%. (f ≤ 50 kHz).
B. C_L includes probe and jig capacitance.

Fig. 9 SWITCHING TIMES

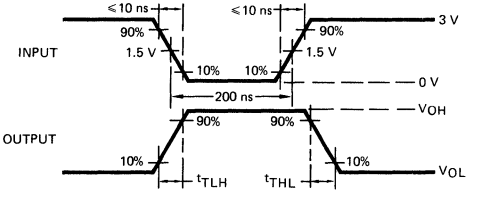
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (Cont'd)



VOLTAGE WAVEFORMS



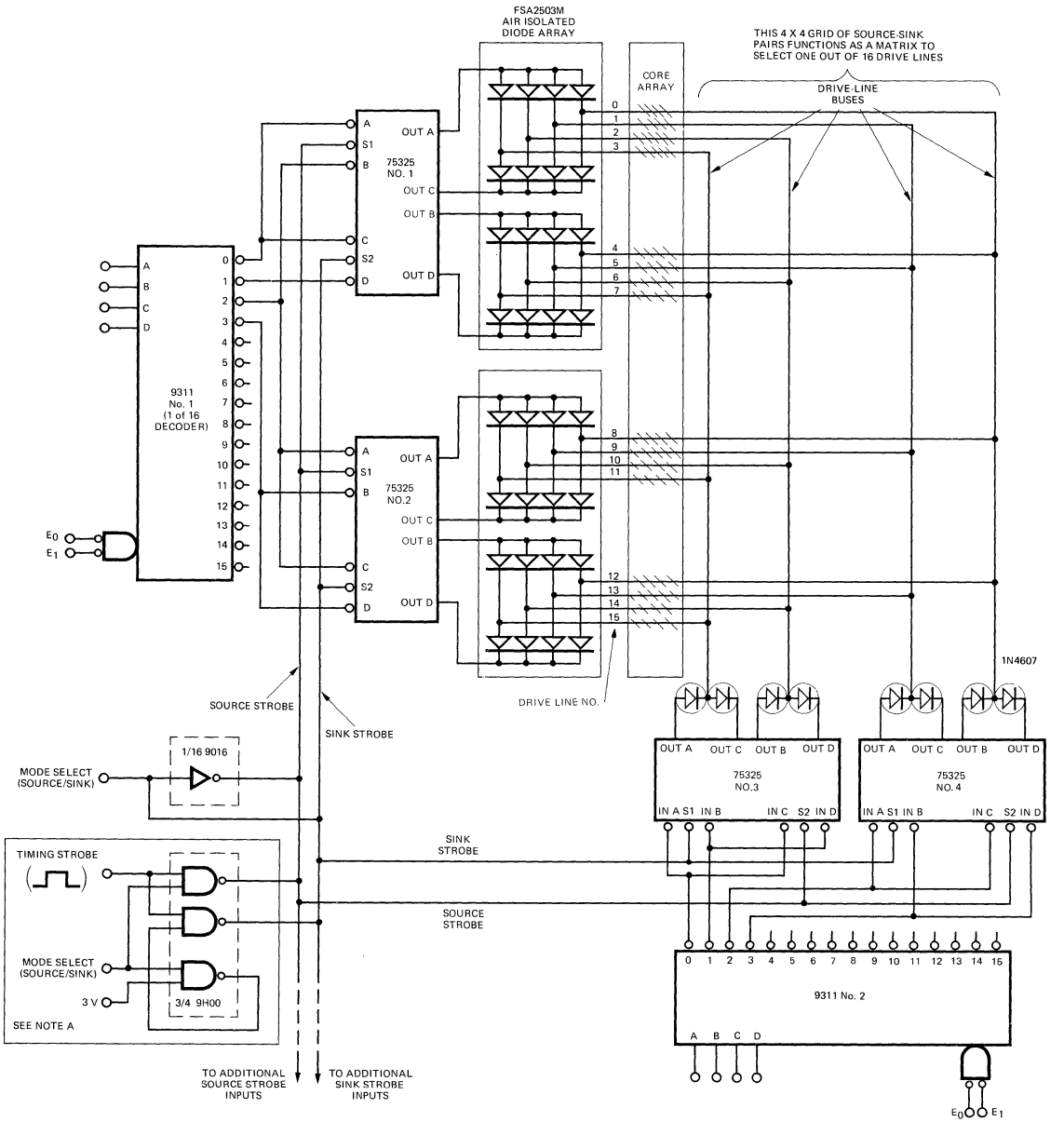
TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5 V
t_{TLH} and t_{THL}	Source Output A	A and S1	B, C, D, and S2
	Source Output B	B and S1	A, C, D, and S2

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 1%. (f ≤ 50 kHz)
B. C_L includes probe and jig capacitance.

Fig. 10 TRANSITION TIMES OF SOURCE OUTPUTS

APPLICATIONS



In memory-drive applications the 75325 (or for full-temperature operation, the 55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 11. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, 9311 No. 1 must be set to 3 (with mode select HIGH), enabling source B of 75325 No. 2 to drive lines 12 through 15, and 9311 No. 2 must be set to 2, providing a sink at C of 75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from HIGH to LOW. The size of such a matrix is limited only by the number of drive-lines that a source sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver.

NOTE A: This optional mode-select and timing-strobe technique can be used in place of the 9N40 mode-select and 9311 timing-strobe when minimum time skew is desired.

Fig. 11 75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES

APPLICATIONS (Cont'd)

EXTERNAL RESISTOR CALCULATION – A typical magnetic-memory word drive requirement is shown in Figure 12. A source-output transistor of one 75325 delivers load current (I_L). The sink-output transistor of another 75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \quad \text{(Equation 1)}$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \quad \text{where: } P_{Rext} \text{ is in mW.} \quad \text{(Equation 2)}$$

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\, I_L \quad \text{where: } I_{CS} \text{ is in mA.} \quad \text{(Equation 3)}$$

As an example, let $V_{CC2(min)} = 20$ V and $V_L = 3$ V while I_L of 500 mA flows.

Using Equation 1,

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

and from Equation 2,

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

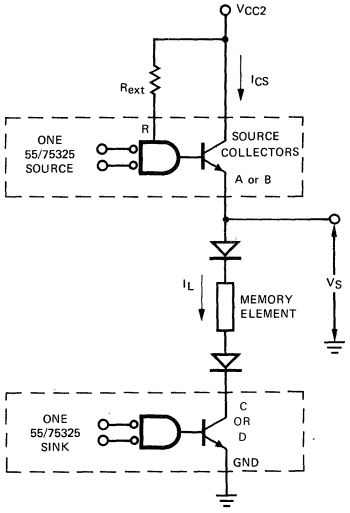
The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.

TYPICAL APPLICATION DATA

EXTERNAL RESISTOR CALCULATION (Cont'd)



NOTES: A. For clarity, partial logic diagrams of two 75325's are shown.
B. Source and sink shown are in different packages.

Fig. 12

THERMAL INFORMATION

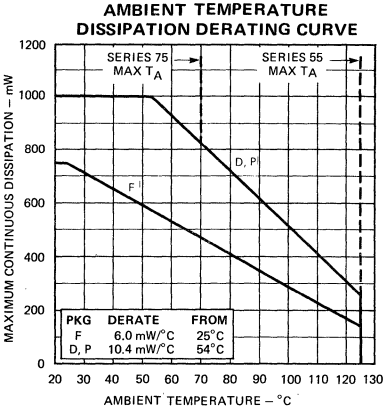


Fig. 13

55326•75326•55327•75327

MEMORY DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55326, 55327, 75326 and 75327 are monolithic integrated circuit quad memory drivers. These devices accept standard TTL decoder input signals and provide high-current and high-voltage output levels suitable for driving magnetic memory elements. Output transistor selection is determined by using one of the four address inputs and the common timing strobe.

The 55326 and 75326 memory drivers can sink up to 600 mA and operate from a single 5 V supply.

The 55327 and 75327 memory switches can source or sink up to 600 mA and operate from two supplies; one of 5.0 V and the other from 4.5 V to 24 V. The 55327 and 75327 can function as either sink drivers or source drivers since the voltages at the output transistor terminals are capable of swinging between V_{CC2} and ground.

55326, 75326 PERFORMANCE

- **QUAD POSITIVE OR SINK MEMORY DRIVERS**
- **600 mA OUTPUT CURRENT SINK CAPABILITY**
- **24 V OUTPUT CAPABILITY**
- **CLAMP VOLTAGE VARIABLE TO 24 V**

55327, 75327 PERFORMANCE

- **QUAD MEMORY SWITCHES**
- **600 mA OUTPUT CURRENT CAPABILITY**
- **V_{CC2} DRIVE VOLTAGE VARIABLE TO 24 V**
- **OUTPUT CAPABLE OF SWINGING BETWEEN V_{CC2} AND GROUND**

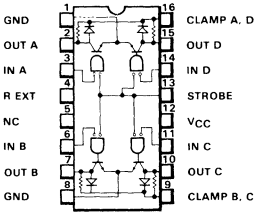
EASE OF DESIGN

- **HIGH-REPETITION-RATE DRIVER COMPATIBLE WITH HIGH-SPEED MAGNETIC MEMORIES**
- **INPUTS COMPATIBLE WITH TTL DECODERS**
- **MINIMUM TIME SKEW BETWEEN STROBE AND OUTPUT-CURRENT RISE**
- **PULSE-TRANSFORMER COUPLING ELIMINATED**
- **DRIVE-LINE LENGTHS REDUCED**

CONNECTION DIAGRAM
16-PIN (TOP VIEW)

PACKAGE OUTLINES 7B, 9B, 4L
PACKAGE CODES D P F

55326/75326



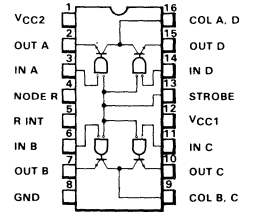
ORDER INFORMATION

TYPE	PART NO.
55326	55326DM
55326	55326FM
75326	75326DC
75326	75326PC

CONNECTION DIAGRAM
16-PIN (TOP VIEW)

PACKAGE OUTLINES 7B, 9B, 4L
PACKAGE CODES D P F

55327/75327



ORDER INFORMATION

TYPE	PART NO.
55327	55327DM
55327	55327FM
75327	75327DC
75327	75327PC

55326

ELECTRICAL CHARACTERISTICS: Ratings apply over recommended temperature range unless otherwise specified.

SYMBOL	CHARACTERISTICS		CONDITIONS†		MIN	TYP††	MAX	UNITS
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC} = 4.5 V, I_{IN} = −10 mA, T_A = 25°C			−1.0	−1.7	V
V_{OH}	Output HIGH Voltage		V_{CC1} = 4.5 V, I_{OUT} = 0		19	23		V
V_{SAT}	Saturation Voltage Sink Outputs		V_{CC} = 4.5 V, I_{sink} ≈ 600 mA, See Note 3	Full Range			0.9	V
				T_A = 25°C		0.43	0.7	
$V_{F(clamp)}$	Output Clamp Diode, Forward Voltage		$V_{(clamp)}$ = 0, $I_{(clamp)}$ = −10 mA, T_A = 25°C				1.5	V
$I_{(clamp)}$	Output Clamp Diode Current, One Output On		I_{sink} = 50 mA, T_A = 25°C			5.0	7.0	mA
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{IN} = 5.5 V				1.0	mA
		Strobe Inputs					4.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{IN} = 2.4 V				40	μA
		Strobe Inputs					160	
I_{IL}	Input LOW Current	Address Inputs	V_{IN} = 0.4 V			−1.0	−1.6	mA
		Strobe Inputs				−4.0	−6.4	
$I_{CC(off)}$	Supply Current, All Outputs Off		All Inputs at 5.0 V, T_A = 25°C			18	25	mA
$I_{CC(on)}$	Supply Current		I_{sink} = 50 mA, T_A = 25°C			58	75	mA

75326

ELECTRICAL CHARACTERISTICS: Ratings apply over recommended temperature range unless otherwise specified.

SYMBOL	CHARACTERISTICS		CONDITIONS†		MIN	TYP††	MAX	UNITS
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC} = 4.5 V, I_{IN} = −10 mA, T_A = 25°C			−1.0	−1.7	V
V_{OH}	Output HIGH Voltage		V_{CC1} = 4.5 V, I_{OUT} = 0		19	23		V
V_{SAT}	Saturation Voltage Sink Outputs		V_{CC} = 4.5 V, I_{sink} ≈ 600 mA, See Note 3	Full Range			0.9	V
				T_A = 25°C		0.43	0.75	
$V_{F(clamp)}$	Output Clamp Diode, Forward Voltage		$V_{(clamp)}$ = 0, $I_{(clamp)}$ = −10 mA, T_A = 25°C				1.5	V
$I_{(clamp)}$	Output Clamp Diode Current, One Output On		I_{sink} = 50 mA, T_A = 25°C			5.0	7.0	mA
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{IN} = 5.5 V				1.0	mA
		Strobe Inputs					4.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{IN} = 2.4 V				40	μA
		Strobe Inputs					160	
I_{IL}	Input LOW Current	Address Inputs	V_{IN} = 0.4 V			−1.0	−1.6	mA
		Strobe Inputs				−4.0	−6.4	
$I_{CC(off)}$	Supply Current, All Outputs Off		All Inputs at 5.0 V, T_A = 25°C			18	25	mA
$I_{CC(on)}$	Supply Current		I_{sink} = 50 mA, T_A = 25°C			58	75	mA

† Unless otherwise noted, V_{CC} = 5.5 V, $V_{(clamp)}$ = 24 V. See Figure 3.
†† All typical values are at T_A = 25°C.

NOTE 3: These characteristics must be measured using pulse techniques; t_W = 200 μs, duty cycle ≤ 2 %.
NOTE 4: For these tests only one output is to be on at any one time.

55327

ELECTRICAL CHARACTERISTICS: Ratings apply over recommended temperature range unless otherwise specified.

SYMBOL	CHARACTERISTICS		CONDITIONS†		MIN	TYP††	MAX	UNITS
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC} = 4.5 V, I_{IN} = −10 mA, T_A = 25°C			−1.0	−1.7	V
$I_{(off)}$	Collectors Terminal Off-state Current		V_{CC1} = 4.5 V, $V_{(col)}$ = 24 V	Full Range			500	μA
				T_A = 25°C			150	
V_{SAT}	Saturation Voltage		V_{CC1} = 4.5 V, V_O = 0 $I_{source} \approx$ −600 mA See Notes 3 and 4	Full Range			0.9	V
				T_A = 25°C		0.43	0.7	
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{IN} = 5.5 V				1.0	mA
		Strobe Inputs					4.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{IN} = 2.4 V				40	μA
		Strobe Inputs					160	
I_{IL}	Input LOW Current	Address Inputs	V_{IN} = 0.4 V			−1.0	−1.6	mA
		Strobe Inputs				−4.0	−6.4	
$I_{CC(off)}$	Supply Current, All Outputs Off	From V_{CC1}	All Inputs at 5.0 V, T_A = 25°C			7.0	10	mA
		From V_{CC2}				13	20	
$I_{CC(on)}$	Supply Current	From V_{CC1}	I_{source} = −50 mA, $V_{(col)}$ = 6.0 V T_A = 25°C, See Note 3			8.0	12	mA
		From V_{CC2}				36	55	

75327

ELECTRICAL CHARACTERISTICS: Ratings apply over recommended temperature range unless otherwise specified.

SYMBOL	CHARACTERISTICS		CONDITIONS†		MIN	TYP††	MAX	UNITS
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_{CD}	Input Clamp Diode Voltage		V_{CC} = 4.5 V, I_{IN} = −10 mA, T_A = 25°C			−1.0	−1.7	V
$I_{(off)}$	Collectors Terminal Off-state Current		V_{CC1} = 4.5 V, $V_{(col)}$ = 24 V	Full Range			200	μA
				T_A = 25°C			200	
V_{SAT}	Saturation Voltage		V_{CC1} = 4.5 V, V_O = 0 $I_{source} \approx$ −600 mA See Notes 3 and 4	Full Range			0.9	V
				T_A = 25°C		0.43	0.75	
I_{IN}	Input Current at Maximum Input Voltage	Address Inputs	V_{IN} = 5.5 V				1.0	mA
		Strobe Inputs					4.0	
I_{IH}	Input HIGH Current	Address Inputs	V_{IN} = 2.4 V				40	μA
		Strobe Inputs					160	
I_{IL}	Input LOW Current	Address Inputs	V_{IN} = 0.4 V			−1.0	−1.6	mA
		Strobe Inputs				−4.0	−6.4	
$I_{CC(off)}$	Supply Current, All Outputs Off	From V_{CC1}	All Inputs at 5.0 V, T_A = 25°C			7.0	10	mA
		From V_{CC2}				13	20	
$I_{CC(on)}$	Supply Current	From V_{CC1}	I_{source} = −50 mA, $V_{(col)}$ = 6.0 V T_A = 25°C, See Note 3			8.0	12	mA
		From V_{CC2}				36	55	

† Unless otherwise noted, V_{CC} = 5.5 V, $V_{(clamp)}$ = 24 V. See Figure 3.
†† All typical values are at T_A = 25°C.

NOTE 3: These characteristics must be measured using pulse techniques; t_W = 200 μs, duty cycle ≤ 2 %.
NOTE 4: For these tests only one output is to be on at any one time.

55326 • 75326

SWITCHING CHARACTERISTICS: V_{CC1} = 5.0 V, T_A = 25°C (See Test Circuit Figure 5)

SYMBOL	CHARACTERISTICS	CONDITIONS (See Note 4)	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time to A, B, C or D	$V_S = V_{(clamp)}$ = 15 V, R_L = 24 Ω, C_L = 25 pF			50	ns
t_{PHL}				25	50	
t_{TLH}	Transition Time to A, B, C or D			7.0	15	ns
t_{THL}				10	20	
t_s	Storage Time to A, B, C or D			24	35	ns
V_{OH}	Output HIGH Voltage	$V_S = V_{(clamp)}$ = 24 V, R_L = 47 Ω, C_L = 25 pF, $I_{sink} \approx$ 500 mA	V_S −25			mV

55327 • 75327

SWITCHING CHARACTERISTICS: V_{CC1} = 5.0 V, T_A = 25°C (See Test Circuit Figure 5)

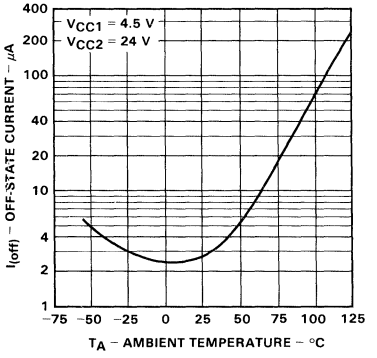
SYMBOL	CHARACTERISTICS	CONDITIONS (See Note 4)	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time to Collectors A,D or B,C	$V_S = V_{CC2}$ = 15 V, R_L = 24 Ω, C_L = 25 pF, See Figure 5 and Note 5		35	55	ns
t_{PHL}				30	55	
t_{TLH}	Transition Time to A,B,C or D	$V_{(col)} = V_{CC2}$ = 20 V, R_L = 100 Ω, C_L = 25 pF, See Figure 6 and Note 5		30		ns
t_{THL}				10		
V_{OH}	Output HIGH Voltage to Collectors A,D or B,C	$V_S = V_{CC2}$ = 24 V, R_L = 47 Ω, C_L = 24 pF, $I_{sink} \approx$ 500 mA, See Figure 5 and Note 5	V_S −25			mV

† Unless otherwise noted, V_{CC} = 5.5 V, $V_{(clamp)}$ = 24 V. See Figure 3.
†† All typical values are at T_A = 25°C.

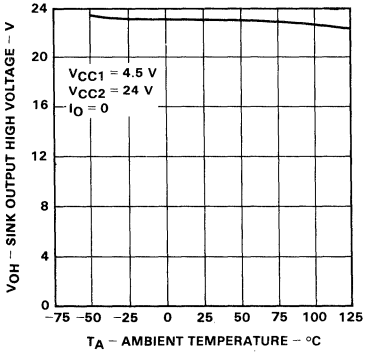
NOTE 3: These characteristics must be measured using pulse techniques; t_W = 200 μs, duty cycle ≤ 2 %.
NOTE 4: For these tests only one output is to be on at any one time.
NOTE 5: A 350 Ω resistor is connected between node R (pin 4) and V_{CC2} (pin 1) with R_{int} (pin 5) open.

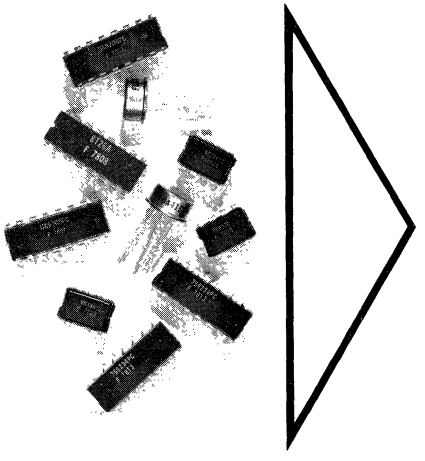
TYPICAL PERFORMANCE CURVES

OFF-STATE CURRENT INTO SOURCE COLLECTORS AS A FUNCTION OF AMBIENT TEMPERATURE – 55327/75327 ONLY



SINK OUTPUT HIGH VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE – 55326/75326 ONLY





TRANSISTOR ARRAYS AND SPECIAL FUNCTIONS

μA3018 • μA3018A • μA3019 • μA3026 • μA3036
μA3039 • μA3045 • μA3046 • μA3054 • μA3086

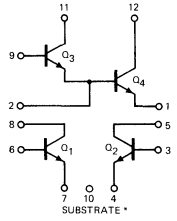
TRANSISTOR AND DIODE ARRAYS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – Fairchild Transistor and Diode Arrays consist of general purpose integrated circuit devices constructed on a single substrate, using the Fairchild Planar* epitaxial process. These arrays are arranged to offer maximum flexibility in circuit design for applications from dc to 120 MHz. Excellent transistor and diode matching and temperature tracking allow circuit techniques unavailable when using discrete devices. Multiple devices in one package permit a greater packing density and cost saving than with individually packaged transistors.

- **PRECISION MONOLITHIC MATCHING**
- **DESIGN FLEXIBILITY**
- **CUSTOM APPLICATIONS**

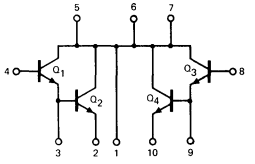
PACAKGE OUTLINE 5D
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3018	μA3018HM
μA3018A	μA3018AHM

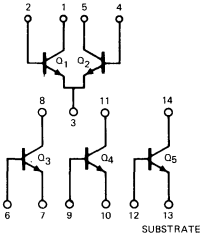
PACKAGE OUTLINE 5Q
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3036	μA3036HM

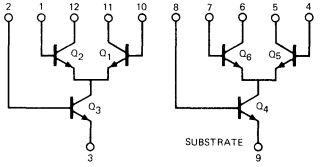
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA3045	μA3045DM
μA3046	μA3046DC
μA3046	μA3046PC
μA3086	μA3086DM

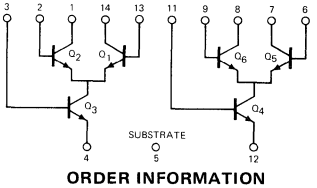
PACKAGE OUTLINE 5D
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3026	μA3026HM

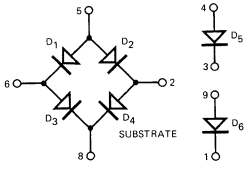
PACAKGE OUTLINE 6A
PACAKGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA3054	μA3054DC

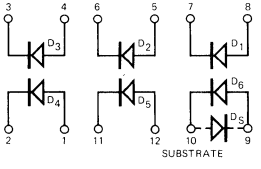
PACAKGE OUTLINE 5D
PACAKGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3019	μA3019HM

PACAKGE OUTLINE 5Q
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA3039	μA3039HM

*Planar is a patented Fairchild process.

μA3018/3018A

- **MATCHED MONOLITHIC GENERAL PURPOSE TRANSISTORS**
- **h_{FE} MATCHED ±10%**
- **V_{BE} MATCHED ±2 mV 3018A (±5 mV 3018)**
- **OPERATION FROM DC TO 120 MHz**
- **WIDE OPERATING CURRENT RANGE**
- **3018A PERFORMANCE CHARACTERISTICS CONTROLLED FROM 10 μA TO 10 mA**
- **LOW NOISE FIGURE – 3.2 dB TYPICAL AT 1 kHz**
- **FULL MILITARY TEMPERATURE RANGE CAPABILITY (–55 TO +125°C)**

APPLICATIONS

- General Use in Signal Processing Systems in dc Through VHF Range
- Custom Design Differential Amplifiers
- Temperature Compensated Amplifiers

ABSOLUTE MAXIMUM RATINGS

	μA3018	**μA3018A**
Power Dissipation (Note 1)		
Any One Transistor	300 mW	300 mW
Total Package	450 mW	450 mW
Temperature Range		
Operating Temperature	–55°C to +125°C	–55°C to +125°C
Storage Temperature	–65°C to +200°C	–65°C to +200°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage, V_{CEO}	15 V	15 V
Collector-to-Base Voltage, V_{CBO}	20 V	30 V
Collector-to-Substrate Voltage, V_{CIO} (Note 2)	20 V	40 V
Emitter-to-Base Voltage, V_{EBO}	5 V	5 V
Collector Current, I_C	50 mA	50 mA

ELECTRICAL CHARACTERISTICS FOR μA3018: $T_A = 25°C$ unless otherwise specified

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CBO}	Collector Cutoff Current	$V_{CB} = 10$ V, $I_E = 0$		0.002	100	nA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 10$ V, $I_B = 0$		See Curve	5.0	μA
I_{CEOD}	Collector Cutoff Current Darlington Pair	$V_{CE} = 10$ V, $I_B = 0$				μA
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	15	24		V
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	$I_C = 10$ μA, $I_E = 0$	20	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	$I_E = 10$ μA, $I_C = 0$	5.0	7.0		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$I_C = 10$ μA, $I_{CI} = 0$	20	60		V
V_{CES}	Collector-to-Emitter Saturation Voltage	$I_B = 1$ mA, $I_C = 10$ mA		0.23		V
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 3$ V, $I_C = 10$ mA $I_C = 1$ mA $I_C = 10$ μA	30	100 100 54		
	Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)	$V_{CE} = 3$ V, $I_{C1} = I_{C2} = 1$ mA	0.9	0.97		
h_{FED}	Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	$V_{CE} = 3$ V, $I_C = 1$ mA $I_C = 100$ μA	1500	5400		
V_{BE}	Base-to-Emitter Voltage	$V_{CE} = 3$ V, $I_E = 1$ mA $I_E = 10$ mA		0.715 0.800		V
$\lvert V_{BE_1} \rvert$ $\lvert V_{BE_2} \rvert$	Input Offset Voltage	$V_{CE} = 3$ V, $I_E = 1$ mA		0.48	5.0	mV
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	$V_{CE} = 3$ V, $I_E = 1$ mA		−1.9		mV/°C
V_{BED} $(V_{9\text{-}1})$	Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	$V_{CE} = 3$ V, $I_E = 10$ mA $I_E = 1$ mA		1.46 1.32		V
$\frac{\Delta V_{BED}}{\Delta T}$	Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$V_{CE} = 3$ V, $I_E = 1$ mA		4.4		mV/°C
$\frac{V_{BE_1}\text{-}V_{BE_2}}{\Delta T}$	Temperature Coefficient: Magnitude of Input-Offset Voltage	$V_{CC} = +6$ V, $V_{EE} = -6$ V		10		μV/°C
NF	Low Frequency Noise Figure	f = 1 kHz, $V_{CE} = 3$ V, $I_C = 100$ μA Source resistance = 1 kΩ		3.25		dB
	Low Frequency, Small-Signal Equivalent Circuit Characteristics:					
h_{fe}	Forward Current-Transfer Ratio	f = 1 kHz, $V_{CE} = 3$ V, $I_C = 1$ mA		110		
h_{ie}	Short Circuit Input Resistance			3.5		kΩ
h_{oe}	Open Circuit Output Conductance			15.6		μmho
h_{re}	Open Circuit Reverse Voltage-Transfer Ratio			1.8×10^{-4}		
	Admittance Characteristics:					
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, $V_{CE} = 3$ V, $I_C = 1$ mA		31 − j 1.5		mmho
Y_{ie}	Input Admittance			0.3 + j 0.04		mmho
Y_{oe}	Output Admittance			0.001 + j 0.03		mmho
Y_{re}	Reverse Transfer Admittance			See Curve		mmho
f_T	Gain-Bandwidth Product	$V_{CE} = 3$ V, $I_C = 3$ mA		500		MHz
C_{eb}	Emitter-to-Base Capacitance	$V_{EB} = 3$ V, $I_E = 0$		0.6		pF
C_{cb}	Collector-to-Base Capacitance	$V_{CB} = 3$ V, $I_C = 0$		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	$V_{CI} = 3$ V, $I_C = 0$		2.8		pF

NOTES:

1. Derate at 5 mW/°C for $T_A > 85°C$.
2. Substrate must be connected to the most negative voltage to maintain normal operation.

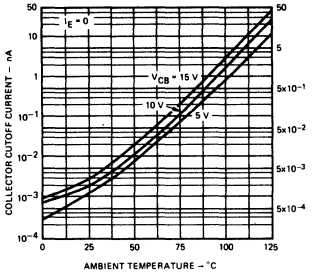
9

ELECTRICAL CHARACTERISTICS FOR μA3018A: $T_A = 25°C$ unless otherwise specified

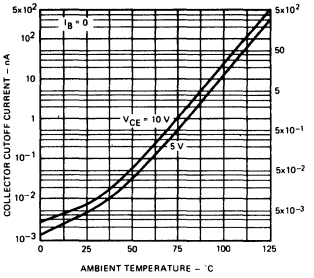
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CBO}	Collector Cutoff Current	$V_{CB} = 10$ V, $I_E = 0$		0.002	40	nA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 10$ V, $I_B = 0$		See Curve	0.5	μA
I_{CEOD}	Collector Cutoff Current Darlington Pair	$V_{CE} = 10$ V, $I_B = 0$			5.0	μA
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	15	24		V
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	$I_C = 10$ μA, $I_E = 0$	30	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	$I_E = 10$ μA, $I_C = 0$	5.0	7.0		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$I_C = 10$ μA, $I_{CI} = 0$	40	60		V
V_{CES}	Collector-to-Emitter Saturation Voltage	$I_B = 1$ mA, $I_C = 10$ mA		0.23	0.5	V
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 3$ V, $I_C = 10$ mA	50	100		
		$V_{CE} = 3$ V, $I_C = 1$ mA	60	100		
		$V_{CE} = 3$ V, $I_C = 10$ μA	30	54		
	Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)	$V_{CE} = 3$ V, $I_{C1} = I_{C2} = 1$ mA	0.9	0.97		
h_{FED}	Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	$V_{CE} = 3$ V, $I_C = 1$ mA	2000	5400		
		$V_{CE} = 3$ V, $I_C = 100$ μA	1000	2800		
V_{BE}	Base-to-Emitter Voltage	$V_{CE} = 3$ V, $I_E = 1$ mA	0.600	0.715	0.800	V
		$V_{CE} = 3$ V, $I_E = 10$ mA		0.800	0.900	
$\lvert V_{BE_1} \rvert$ / $\lvert V_{BE_2} \rvert$	Input Offset Voltage	$V_{CE} = 3$ V, $I_E = 1$ mA		0.48	2.0	mV
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	$V_{CE} = 3$ V, $I_E = 1$ mA		−1.9		mV/°C
V_{BED} (V_{9-1})	Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	$V_{CE} = 3$ V, $I_E = 10$ mA		1.46	1.60	V
		$V_{CE} = 3$ V, $I_E = 1$ mA	1.10	1.32	1.50	
$\frac{\Delta V_{BED}}{\Delta T}$	Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$V_{CE} = 3$ V, $I_E = 1$ mA		4.4		mV/°C
$\frac{V_{BE_1}-V_{BE_2}}{\Delta T}$	Temperature Coefficient: Magnitude of Input-Offset Voltage	$V_{CC} = +6$ V, $V_{EE} = -6$ V		10		μV/°C
NF	Low Frequency Noise Figure	f = 1 kHz, $V_{CE} = 3$ V, $I_C = 100$ μA Source resistance = 1 kΩ		3.25		dB
	Low Frequency, Small-Signal Equivalent Circuit Characteristics:					
h_{fe}	Forward Current-Transfer Ratio	f = 1 kHz, $V_{CE} = 3$ V, $I_C = 1$ mA		110		
h_{ie}	Short Circuit Input Resistance			3.5		kΩ
h_{oe}	Open Circuit Output Conductance			15.6		μmho
h_{re}	Open Circuit Reverse Voltage-Transfer Ratio			1.8×10^{-4}		
	Admittance Characteristics:					
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, $V_{CE} = 3$ V, $I_C = 1$ mA		31 − j 1.5		mmho
Y_{ie}	Input Admittance			0.3 + j 0.04		mmho
Y_{oe}	Output Admittance			0.001 + j 0.03		mmho
Y_{re}	Reverse Transfer Admittance			See Curve		mmho
f_T	Gain-Bandwidth Product	$V_{CE} = 3$ V, $I_C = 3$ mA		500		MHz
C_{eb}	Emitter-to-Base Capacitance	$V_{EB} = 3$ V, $I_E = 0$		0.6		pF
C_{cb}	Collector-to-Base Capacitance	$V_{CB} = 3$ V, $I_C = 0$		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	$V_{CI} = 3$ V, $I_C = 0$		2.8		pF

TYPICAL PERFORMANCE CURVES FOR μA3018/3018A

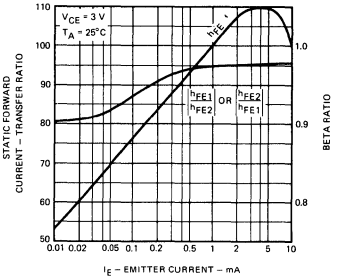
COLLECTOR-TO-BASE CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



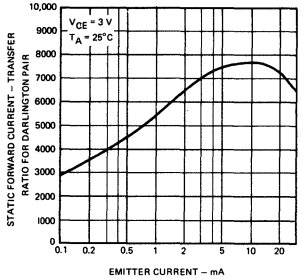
COLLECTOR-TO-EMITTER CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



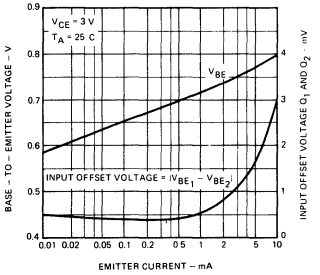
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q1, Q2 AS A FUNCTION OF EMITTER CURRENT



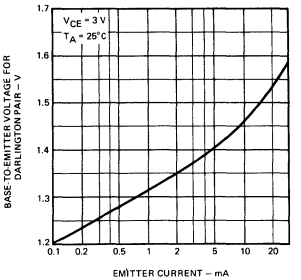
STATIC FORWARD CURRENT-TRANSFER RATIO FOR DARLINGTON CONNECTED TRANSISTORS Q3, Q4 AS A FUNCTION OF EMITTER CURRENT



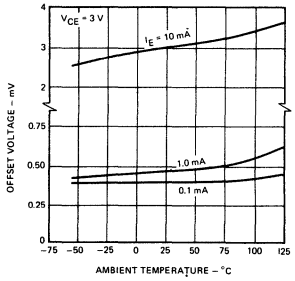
STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE FOR Q1, Q2 AS A FUNCTION OF EMITTER CURRENT



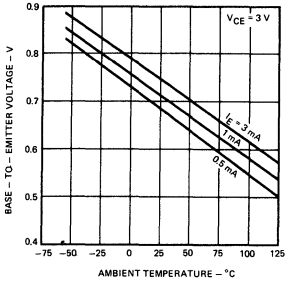
STATIC INPUT VOLTAGE FOR DARLINGTON PAIR Q3, Q4 AS A FUNCTION OF EMITTER CURRENT



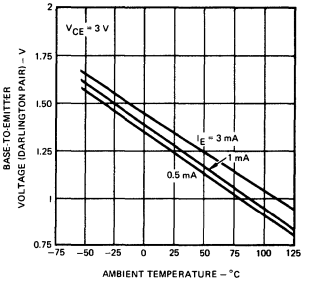
OFFSET VOLTAGE CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE



BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE



STATIC INPUT VOLTAGE FOR DARLINGTON PAIR (Q_3, Q_4) AS A FUNCTION OF AMBIENT TEMPERATURE



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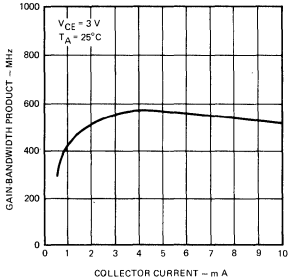
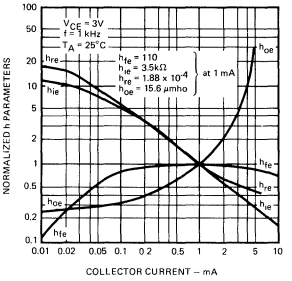
TYPICAL AC CHARACTERISTICS FOR EACH TRANSISTOR

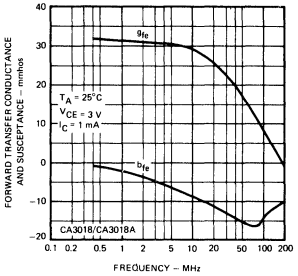
GAIN-BANDWIDTH PRODUCT (f_T) AS A FUNCTION OF COLLECTOR CURRENT



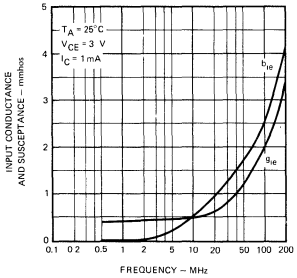
NORMALIZED h PARAMETERS AS A FUNCTION OF COLLECTOR CURRENT



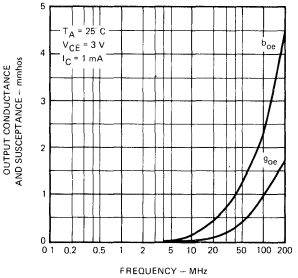
FORWARD TRANSFER ADMITTANCE (Y_{fe}) AS A FUNCTION OF FREQUENCY



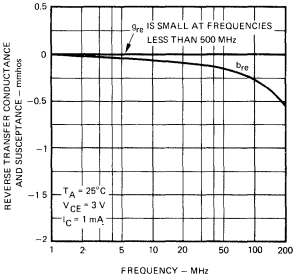
INPUT ADMITTANCE (Y_{ie}) AS A FUNCTION OF FREQUENCY



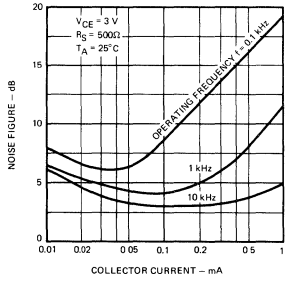
OUTPUT ADMITTANCE (Y_{oe}) AS A FUNCTION OF FREQUENCY



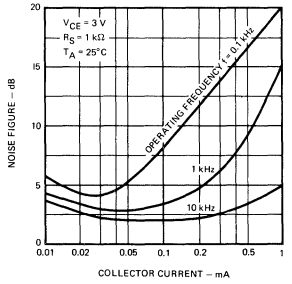
REVERSE TRANSFER ADMITTANCE (Y_{re}) AS A FUNCTION OF FREQUENCY



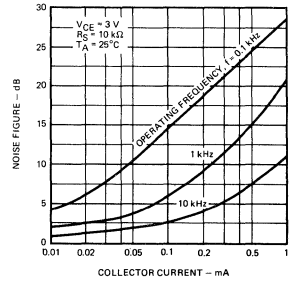
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT,



NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT,



NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT,



μA3019

- **EXCELLENT DIODE MATCHING – 1 mV TYP.**
- **LOW REVERSE LEAKAGE CURRENT – 5 mA TYP.**

APPLICATIONS

- Modulator
- Mixer
- Balanced Modulator
- Analog Switch
- Diode Gate for Chopper-Modulator Applications

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	
For each Diode	20 mW
Total For Device	120 mW
Temperature Range	
Storage Temperature	−65°C to +200°C
Operating Temperature	−55°C to +125°C
Voltage Between Any Pin and Pin 7 (Note 1)	18 V

ELECTRICAL CHARACTERISTICS FOR μA3019: For each diode, $T_A = 25°C$ unless otherwise specified

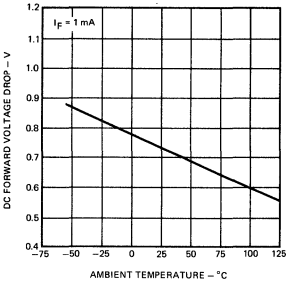
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_F	DC Forward Voltage Drop	DC Forward Current, I_F = 1 mA	–	0.73	0.78	V
BV	DC Reverse Breakdown Voltage (Any Diode)	DC Reverse Current, I_R = −10 μA	4.0	6.0	–	V
BV_S	DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	DC Reverse Current, I_R = −10 μA	25	80	–	V
I_R	DC Reverse (Leakage) Current	DC Reverse Voltage, V_R = −4 V	–	0.0055	10	μA
I_R	DC Reverse (Leakage) Current Between any Diode Unit and Substrate	DC Reverse Voltage, V_R = −4 V	–	0.010	10	μA
$\lvert V_{F_1} - V_{F_2} \rvert$	Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	DC Forward Current, I_F = 1 mA	–	1.0	5.0	mV
C_D	Single Diode Capacitance	Frequency, f = 1 MHz DC Reverse Voltage, V_R = −2 V	–	1.8	–	pF
C_{DQ-I}	Diode Quad-to-Substrate Capacitance	Frequency, f = 1 MHz DC Reverse Voltage, V_R between Pins 2,5,6, or 8 of Diode Quad and Pin 7 (Substrate) = −2 V				
		Pin 2 or 6 to Pin 7	–	4.4	–	pF
		Pin 5 or 8 to Pin 7	–	2.7	–	pF
V_S	Series Gate Switching Pedestal Voltage	See Figure 1	–	10	–	mV

NOTE

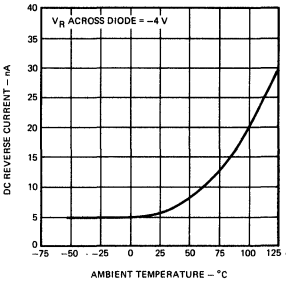
1. Substrate (Pin 7) must be connected to the most negative potential.

TYPICAL PERFORMANCE CURVES FOR μA3019

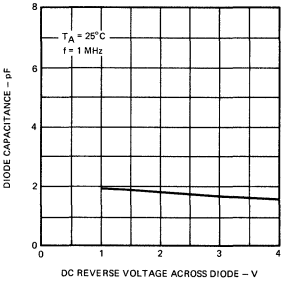
DC FORWARD VOLTAGE DROP (ANY DIODE) AS A FUNCTION OF TEMPERATURE



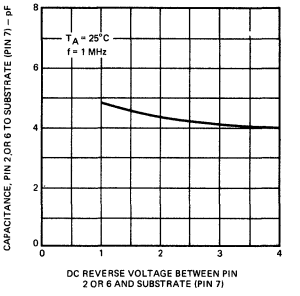
REVERSE (LEAKAGE) CURRENT (ANY DIODE) AS A FUNCTION OF TEMPERATURE



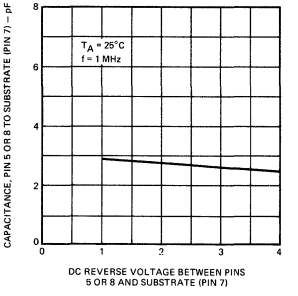
DIODE CAPACITANCE (ANY DIODE) AS A FUNCTION OF REVERSE VOLTAGE



DIODE QUAD-TO-SUBSTRATE CAPACITANCE AS A FUNCTION OF REVERSE VOLTAGE



DIODE QUAD-TO-SUBSTRATE CAPACITANCE AS A FUNCTION OF REVERSE VOLTAGE



SERIES GATE SWITCHING TEST SETUP

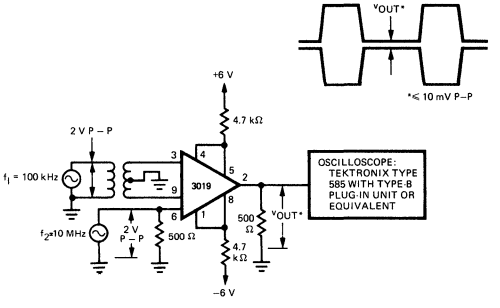


Fig. 1

μA3026/3054

- **LOW INPUT OFFSET VOLTAGE – ±5 mV**
- **WIDEBAND OPERATION**
- **INDEPENDENTLY ACCESSIBLE INPUTS AND OUTPUTS**
- **TWO MATCHED DIFFERENTIAL AMPLIFIERS**

APPLICATIONS

- Dual Sense Amplifiers
- Dual Schmitt Triggers
- Multifunction Combinations – RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Pairs of Balanced Mixers
- Synthesizer Mixers
- Balanced (Push-Pull) Cascode Amplifiers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

	μA3054	μA3026
Power Dissipation (Note 1)		
Any One Transistor	300 mW	300 mW
Total Package	600 mW	750 mW
Temperature Range		
Operating Temperature	−55°C to +125°C	0°C to +85°C
Storage Temperature	−65°C to +200°C	−25°C to +85°C
The following ratings apply for each transistor in the device		
Collector-to-Emitter Voltage, V_{CEO}		15 V
Collector-to-Base Voltage, V_{CBO}		20 V
Collector-to-Substrate Voltage, V_{CIO} (Note 2)		20 V
Emitter-to-Base Voltage, V_{EBO}		5 V
Collector Current, I_C		50 mA

ELECTRICAL CHARACTERISTICS FOR μA3026/3054: $T_A = 25°C$ unless otherwise specified

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
	For Each Differential Amplifier					
V_{IO}	Input Offset Voltage		–	0.45	5	mV
I_{IO}	Input Offset Current	$V_{CB} = 3$ V	–	0.3	2	μA
I_I	Input Bias Current		–	10	24	μA
$I_{C(Q_1)}$ or $I_{C(Q_5)}$ / $I_{C(Q_2)}$ or $I_{C(Q_6)}$	Quiescent Operating Current Ratio	$I_{E(Q_3)} = I_{E(Q_4)} = 2$ mA	–	0.98 to 1.02	–	–
$\frac{\Delta\lvert V_{IO}\rvert}{\Delta T}$	Temperature Coefficient Magnitude of Input-Offset Voltage		–	1.1	–	μV/°C
	For Each Transistor					
V_{BE}	DC Forward Base-to-Emitter Voltage	$V_{CB} = 3$ V, $I_C = 50$ μA	–	0.630	0.700	V
		1 mA	–	0.715	0.800	
		3 mA	–	0.750	0.850	
		10 mA	–	0.800	0.900	
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient of Base to-Emitter Voltage	$V_{CB} = 3$ V, $I_C = 1$ mA	–	−1.9	–	mV/°C
I_{CBO}	Collector-Cutoff Current	$V_{CB} = 10$ V, $I_E = 0$	–	0.002	100	nA
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	15	24	–	V
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	$I_C = 10$ μA, $I_E = 0$	20	60	–	V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$I_C = 10$ μA, $I_{CI} = 0$	20	60	–	V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	$I_E = 10$ μA, $I_C = 0$	5	7	–	V

NOTES
1. For $T_A > 55°C$; 3026 derates at 5 mW/°C and 3054 at 6.67 mW/°C
2. The collector of each transistor of the 3026 and 3054 is isolated from the substrate by an integral diode. Substrate must be connected to the most negative voltage to maintain normal operation.

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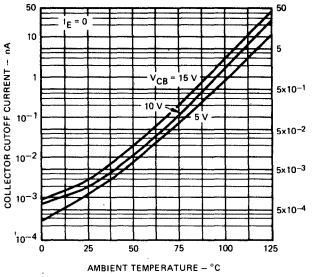
ELECTRICAL CHARACTERISTICS FOR μA3026/3054: $T_A = 25°C$ unless otherwise specified (Cont'd)

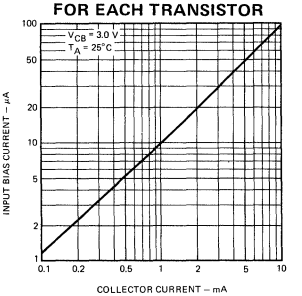
SYMBOL	CHARACTERISTICS (See Test Circuits)	CONDITIONS	MIN	TYP	MAX	UNITS
CMRR	Common-Mode Rejection Ratio for Each Amplifier	$V_{CC} = 12$ V	–	100	–	dB
AGC	AGC Range, One Stage	$V_{EE} = -6$ V	–	75	–	dB
A_V	Voltage Gain, Single Stage Double-Ended Output	$V_x = -3.3$ V	–	32	–	dB
AGC	AGC Range, Two Stage	f = 1 kHz	–	105	–	dB
A_V	Voltage Gain, Two Stage Double-Ended Output		–	60	–	dB
	Low-Frequency, Small-Signal Equivalent-Circuit Characteristics (for Single Transistor):					
h_{fe}	Forward Current-Transfer Ratio		–	110	–	–
h_{ie}	Short Circuit Input Resistance	f = 1 kHz, $V_{CE} = 3$ V,	–	3.5	–	kΩ
h_{oe}	Open Circuit Output Conductance	$I_C = 1$ mA	–	15.6	–	μmho
h_{re}	Open Circuit Reverse Voltage-Transfer Ratio		–	1.8×10^{-4}	–	–
NF	1 Noise Figure (for Single Transistor)	f = 1 kHz, $V_{CE} = 3$ V	–	3.25	–	dB
f_T	Gain-Bandwidth Product (for Single Transistor)	$V_{CE} = 3$ V, $I_C = 3$ mA	–	550	–	MHz
	Admittance Characteristics; Differential Circuit Configuration (for Each Amplifier):					
y_{21}	Forward Transfer Admittance	$V_{CB} = 3$ V	–	−20+j 0	–	mmho
y_{11}	Input Admittance	Each Collector	–	0.22+j 0.1	–	mmho
y_{22}	Output Admittance	$I_C \approx 1.25$ mA	–	0.01+j 0	–	mmho
y_{12}	Reverse Transfer Admittance	f = 1 MHz	–	−0.003+j 0	–	mmho
	Admittance Characteristics; Cascode Circuit Configuration (for Each Amplifier):					
y_{21}	Forward Transfer Admittance	$V_{CB} = 3$ V	–	68-j 0	–	mmho
y_{11}	Input Admittance	Total Stage	–	0.55+j 0	–	mmho
y_{22}	Output Admittance	$I_C \approx 2.5$ mA	–	0+j 0.02	–	mmho
y_{12}	Reverse Transfer Admittance	f = 1 MHz	–	0.004-j 0.005	–	μmho
NF	Noise Figure	f = 100 MHz	–	8	–	dB

TYPICAL PERFORMANCE CURVES FOR μA3026/3054

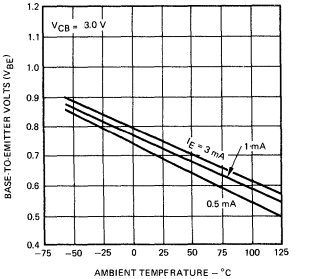
COLLECTOR-TO-BASE CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



INPUT BIAS CURRENT CHARACTERISTIC AS A FUNCTION OF COLLECTOR CURRENT FOR EACH TRANSISTOR

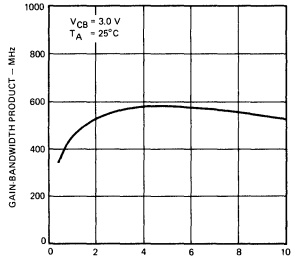


BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR AS A FUNCTION OF AMBIENT TEMPERATURE

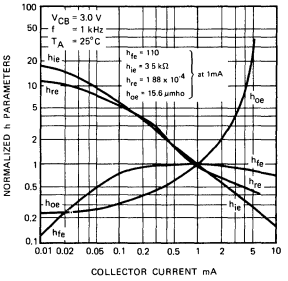


TYPICAL AC CHARACTERISTICS FOR EACH TRANSISTOR FOR μA3026/3054

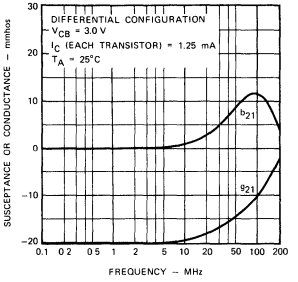
GAIN BANDWIDTH PRODUCT (f_T) AS A FUNCTION OF COLLECTOR CURRENT



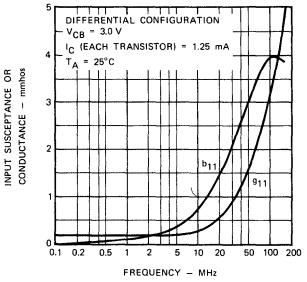
NORMALIZED h PARAMETER AS A FUNCTION OF COLLECTOR CURRENT FOR EACH TRANSISTOR



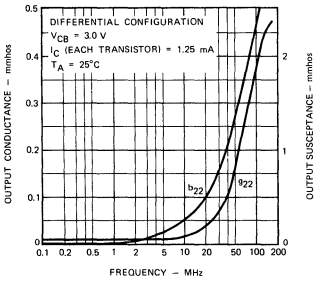
FORWARD TRANSFER ADMITTANCE (Y_{21}) AS A FUNCTION OF FREQUENCY



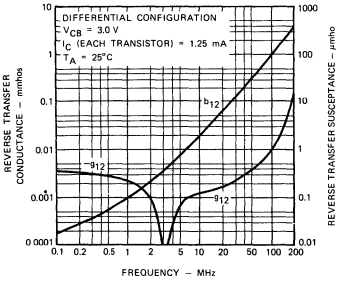
INPUT ADMITTANCE (Y_{11}) AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) AS A FUNCTION OF FREQUENCY

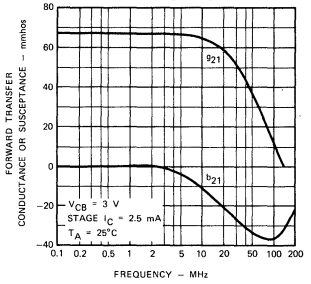


REVERSE TRANSFER ADMITTANCE (Y_{12}) AS A FUNCTION OF FREQUENCY

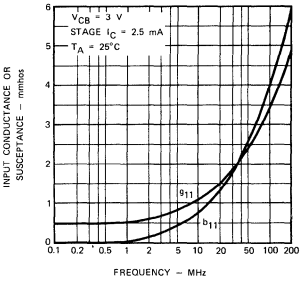


TYPICAL AC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER FOR μA3026/3054

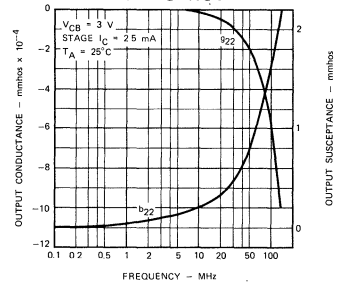
FORWARD TRANSFER ADMITTANCE (Y_{21}) AS A FUNCTION OF FREQUENCY



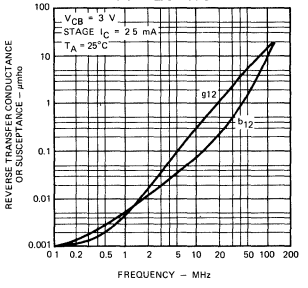
INPUT ADMITTANCE (Y_{11}) AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) AS A FUNCTION OF FREQUENCY



REVERSE TRANSFER ADMITTANCE (Y_{12}) AS A FUNCTION OF FREQUENCY



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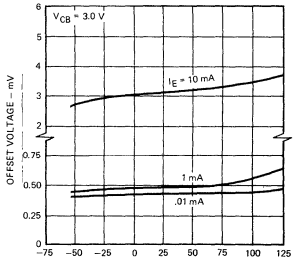
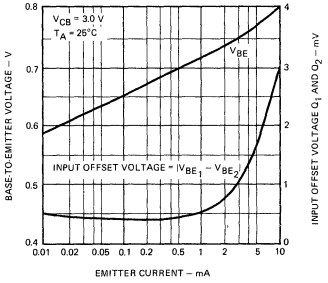
TYPICAL PERFORMANCE CURVES FOR μA3026/3054 (Cont'd)

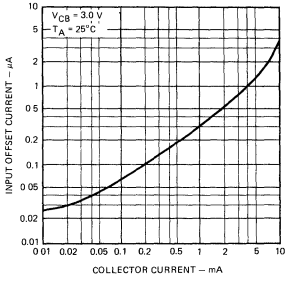
OFFSET VOLTAGE CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE FOR DIFFERENTIAL PAIRS



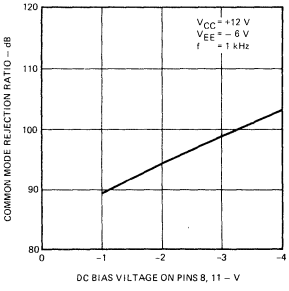
STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIRS AS A FUNCTION OF EMITTER CURRENT



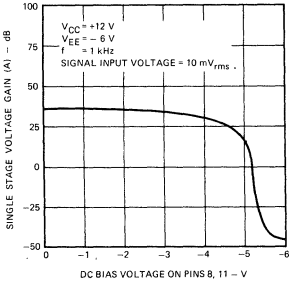
INPUT OFFSET CURRENT FOR MATCHED DIFFERENTIAL PAIRS AS A FUNCTION OF COLLECTOR CURRENT



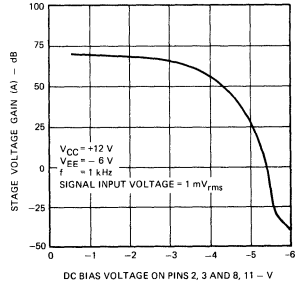
COMMON MODE REJECTION RATIO

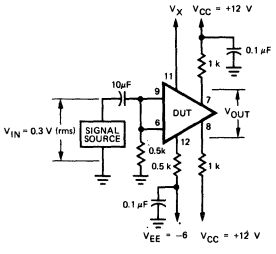


SINGLE STAGE VOLTAGE GAIN

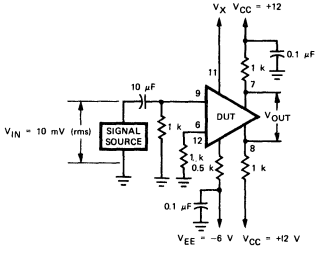


TWO-STAGE VOLTAGE GAIN

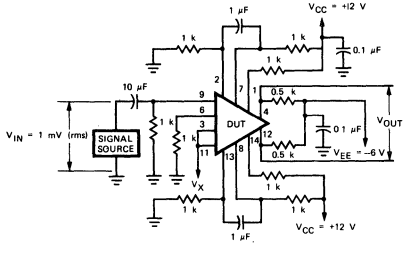




Test setup



Test setup



Test setup

Pin numbers are shown for μ3054 (DIP) only.

μA3036

- **MATCHED TRANSISTOR PERFORMANCE**
- **LOW NOISE PERFORMANCE**
- **200 MHz GAIN BANDWIDTH PRODUCT**

APPLICATIONS

- Stereo Phonograph Preamplifiers
- Low level Stereo and Single Channel Amplifier Stages
- Low noise, Emitter-follower Differential Amplifiers
- Operational Amplifier Drivers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

Power Dissipation	
Any One Transistor	300 mW
Total For Array	300 mW
Temperature Range	
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +200°C
The following ratings apply for each transistor in the array	
Collector-to-Emitter Voltage, V_{CEO}	15 V
Collector-to-Base Voltage, V_{CBO}	30 V
Emitter-to-Base Voltage, V_{EBO}	5 V
Collector Current, I_C	50 mA

ELECTRICAL CHARACTERISTICS FOR μA3036: T_A = 25°C unless otherwise specified

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
	For Each Transistor (Q_1, Q_2, Q_3, Q_4)					
I_{CBO}	Collector Cutoff Current	V_{CB} = 5 V, I_E = 0	–	–	0.5	μA
I_{CEO}	Collector Cutoff Current	V_{CE} = 15 V, I_B = 0	–	–	5.0	μA
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0	15	20	–	V
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0	30	44	–	V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	I_E = 10 μA, I_C = 0	5.0	6.0	–	V
	For Either Input Transistor (Q_1 or Q_3)					
h_{FE}	Static Forward Current-Transfer Ratio	I_{C1} or I_{C3} = 1 mA	30	82	–	–
	For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)					
$V_{(BR)EBO(D)}$	Emitter-to-Base Breakdown Voltage	I_{E2} or I_{E4} = 10 μA	10	12.6	–	V
$h_{FE(D)}$	Static Forward Current-Transfer Ratio	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	1000	4540	–	–
	For Each Input Transistor (Q_1 or Q_3)					
h_{fe}	Short Circuit Forward Current-Transfer Ratio		–	82	–	–
h_{ie}	Short Circuit Input Resistance	f = 1 kHz	–	2.6	–	kΩ
h_{oe}	Open Circuit Output Conductance	I_{C1} or I_{C3} = 1 mA	–	7.0	–	μmho
h_{re}	Open Circuit Reverse Voltage-Transfer Ratio		–	9.8×10^{-5}	–	–
	For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)					
$h_{fe(D)}$	Short Circuit Forward Current-Transfer Ratio	f = 1 kHz	–	1300	–	–
$h_{ie(D)}$	Short Circuit Input Resistance	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	–	82	–	kΩ
$h_{oe(D)}$	Open Circuit Output Conductance		–	108	–	μmho
$h_{re(D)}$	Open Circuit Reverse Voltage-Transfer Ratio		–	2.7×10^{-3}	–	–
E_N	Noise Voltage	f = 100 Hz f = 1 kHz f = 10 kHz	– – –	0.2 0.05 0.012	3.0 0.3 0.1	$\frac{\mu V\ (rms)}{\sqrt{f(Hz)}}$
	For Either Input Transistor (Q_1 or Q_3)					
Y_{fe}	Forward Transfer Admittance		–	0.68 + j 7.9	–	mmho
Y_{ie}	Input Admittance (Output Short Circuited)	f = 50 MHz	–	4.4 + j 5.95	–	mmho
Y_{oe}	Output Admittance (Input Short Circuited)	I_{C1} or I_{C3} = 2 mA	–	1.94 + j 2.64	–	mmho
Y_{re}	Reverse Transfer Admittance (Input Short-Circuited)		–	Negligible	–	mmho
	For Either Darlington Pair (Q_1, Q_2, or Q_3, Q_4)					
$Y_{ie(D)}$	Input Admittance (Output Short Circuited)	f = 50 MHz	–	1.71 + j 2.8	–	mmho
$Y_{oe(D)}$	Output Admittance (Input Short Circuited)	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 2 mA	–	3.96 + j 2.6	–	mmho
$f_{T(D)}$	Gain-Bandwidth Product		150	200	–	MHz

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μA3039

- **EXCELLENT DIODE MATCHING – 1 mV TYP.**
- **REVERSE RECOVERY TIME – 1 ns TYP.**
- **LOW DIODE CAPACITANCE – 0.65 pF @ V_R = –2 V**

APPLICATIONS

- Balanced Modulators or Demodulators
- Ring Modulators
- High Speed Diode Gates
- Analog Switches

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (See note)	
Any One Diode Unit	100 mW
Total for Device	600 mW
Temperature Range	
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +200°C
Voltages and Currents	
Peak Inverse Voltage, PIV for: D_1 - D_5	5 V
D_6	0.5 V
Peak Diode-to-Substrate Voltage, V_{DI} for D_1 - D_5 (term. 1,4,5,8 or 12 to term. 10)	+20,–1 V
DC Forward Current, I_F	25 mA
Peak Recurrent Forward Current, I_f	100 mA
Peak Forward Surge Current, I_f (surge)	100 mA

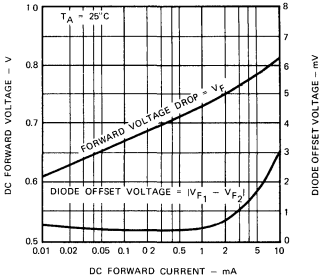
ELECTRICAL CHARACTERISTICS FOR μA3039: For each diode unit, T_A = 25°C unless otherwise specified

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_F	DC Forward Voltage Drop	I_F = 50 μA	–	0.65	0.69	V
		1 mA	–	0.73	0.78	V
		3 mA	–	0.76	0.80	V
		10 mA	–	0.81	0.90	V
BV	DC Reverse Breakdown Voltage	I_R = –10 μA	5.0	7.0	–	V
BV_S	DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	I_R = –10 μA	20	–	–	V
I_R	DC Reverse (Leakage) Current	V_R = –4 V	–	0.016	100	nA
I_R	DC Reverse (Leakage) Current Between any Diode Unit and Substrate	V_R = –10 V	–	0.022	100	nA
$\lvert V_{F_1} - V_{F_2} \rvert$	Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	I_F = 1 mA	–	0.5	5.0	mV
$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	1.0	–	μV/°C
$\frac{\Delta V_F}{\Delta T}$	Temperature Coefficient of Forward Drop	I_F = 1 mA	–	–1.9	–	mV/°C
V_F	DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	I_F = 1 mA	–	0.65	–	V
t_{rr}	Reverse Recovery Time	I_F = 10 mA, I_R = 10 mA	–	1.0	–	ns
R_D	Diode Resistance	f = 1 kHz, I_F = 1 mA	25	30	45	Ω
C_D	Diode Capacitance	V_R = –2 V, I_F = 0	–	0.65	–	pF
C_{DI}	Diode-to-Substrate Capacitance	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF

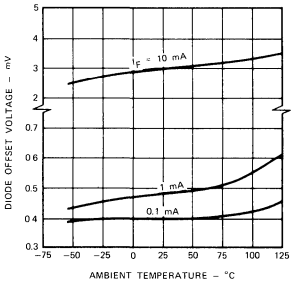
NOTE: Derate at 5.7 mW/°C for $T_A > 55°C$.

TYPICAL PERFORMANCE CURVES FOR μA3039

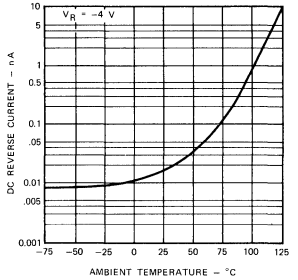
DC FORWARD VOLTAGE DROP (ANY DIODE) AND DIODE OFFSET VOLTAGE AS A FUNCTION OF DC FORWARD CURRENT



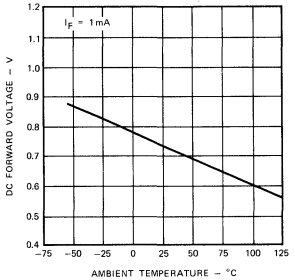
DIODE OFFSET VOLTAGE (ANY DIODE) AS A FUNCTION OF TEMPERATURE



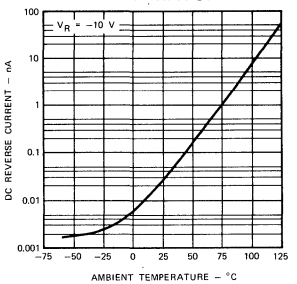
DC REVERSE (LEAKAGE) CURRENT (DIODES 1, 2, 3, 4, 5) AS A FUNCTION OF TEMPERATURE



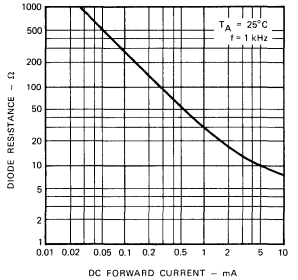
DC FORWARD VOLTAGE DROP (ANY DIODE) AS A FUNCTION OF TEMPERATURE



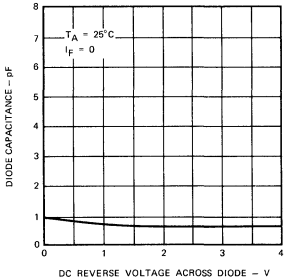
DC REVERSE (LEAKAGE) CURRENT BETWEEN DIODES (1, 2, 3, 4, 5) AND SUBSTRATE AS A FUNCTION OF TEMPERATURE



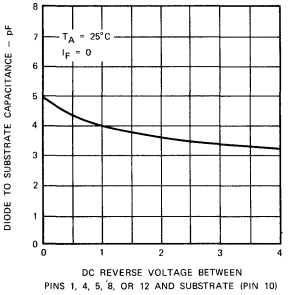
DIODE RESISTANCE (ANY DIODE) AS A FUNCTION OF DC FORWARD CURRENT



DIODE CAPACITANCE (DIODES 1, 2, 3, 4, 5) AS A FUNCTION OF REVERSE VOLTAGE



DIODE-TO-SUBSTRATE CAPACITANCE AS A FUNCTION OF REVERSE VOLTAGE



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μA3045/3046/3086

- **LOW INPUT OFFSET VOLTAGE**
- **WIDEBAND OPERATION**
- **LOW NOISE**

APPLICATIONS

- General Use in all Types of Signal Processing Systems Operating Anywhere in the Frequency Range From DC to VHF
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

	μA3045		μA3046/3086	
Power Dissipation (Note 1)	**Each Transistor**	**Total Package**	**Each Transistor**	**Total Package**
At T_A = 25°C	300 mW	750 mW	300 mW	750 mW
At T_A = 25°C to 55°C			300 mW	750 mW
At T_A = 25°C to 75°C	300 mW	750 mW		
Voltages and Currents				
Collector-to-Emitter Voltage, V_{CEO}	15 V	–	15 V	–
Collector-to-Base Voltage, V_{CBO}	20 V	–	20 V	–
Collector-to-Substrate Voltage, V_{CIO} (Note 2)	20 V	–	20 V	–
Emitter-to-Base Voltage, V_{EBO}	5 V	–	5 V	–
Collector Current, I_C	50 mA	–	50 mA	–
Temperature Range				
Operating Temperature	−55°C to +125°C		(3046) 0°C to +85°C (3086) −40°C to +85°C	
Storage Temperature	−65°C to +200°C		−55°C to +125°C	

ELECTRICAL CHARACTERISTICS FOR μA3045/3046: $T_A = 25°C$ unless otherwise specified

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$	20	60		V
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	15	24		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$I_C = 10\ \mu A$, $I_C = 0$	20	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	$I_E = 10\ \mu A$, $I_C = 0$	5.0	7.0		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 10$ V, $I_E = 0$		0.002	40	nA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 10$ V, $I_B = 0$		See Curve	0.5	μA
h_{FE}	Static Forward Current-Transfer Ratio (Static Beta)	$V_{CE} = 3$ V, $I_C = 10$ mA $I_C = 1$ mA $I_C = 10\ \mu A$	40	100 100 54		
	Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{IO1} - I_{IO2}\rvert$	$V_{CE} = 3$ V, $I_C = 1$ mA		0.3	2.0	μA
V_{BE}	Base-to-Emitter Voltage	$V_{CE} = 3$ V, $I_E = 1$ mA $I_E = 10$ mA		0.715 0.800		V
	Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2}\rvert$	$V_{CE} = 3$ V, $I_C = 1$ mA		0.45	5.0	mV
	Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4}\rvert$, $\lvert V_{BE_4} - V_{BE_5}\rvert$, $\lvert V_{BE_5} - V_{BE_3}\rvert$	$V_{CE} = 3$ V, $I_C = 1$ mA		0.45	5.0	mV
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient of Base-to-Emitter Voltage	$V_{CE} = 3$ V, $I_C = 1$ mA		−1.9		mV/°C
$V_{CE(sat)}$	Collector-to-Emitter Saturation Voltage	$I_B = 1$ mA, $I_C = 10$ mA		0.23		V
$\frac{\lvert\Delta V_{10}\rvert}{\Delta T}$	Temperature Coefficient: Magnitude of Input-Offset Voltage	$V_{CE} = 3$ V, $I_C = 1$ mA		1.1		μV/°C
NF	Low Frequency Noise Figure	$f = 1$ kHz, $V_{CE} = 3$ V, $I_C = 100\ \mu A$, $R_S = 1$ kΩ		3.25		dB
	Low Frequency, Small-Signal Equivalent-Circuit Characteristics:					
h_{fe}	Forward Current-Transfer Ratio	$f = 1$ kHz, $V_{CE} = 3$ V, $I_C = 1$ mA		110		
h_{ie}	Short-Circuit Input Resistance			3.5		kΩ
h_{oe}	Open-Circuit Output Conductance			15.6		μmbo
h_{re}	Open-Circuit Reverse Voltage-Transfer Ratio			1.8×10^{-4}		
	Admittance Characteristics:					
Y_{fe}	Forward Transfer Admittance	$f = 1$ MHz, $V_{CE} = 3$ V, $I_C = 1$ mA		31-j 1.5		
Y_{ie}	Input Admittance			0.3+j0.04		
Y_{oe}	Output Admittance			0.001+j0.03		
Y_{re}	Reverse Transfer Admittance			See Curve		
f_T	Gain-Bandwidth Product	$V_{CE} = 3$ V, $I_C = 3$ mA	300	550		MHz
C_{EB}	Emitter-to-Base Capacitance	$V_{EB} = 3$ V, $I_E = 0$		0.6		pF
C_{CB}	Collector-to-Base Capacitance	$V_{CB} = 3$ V, $I_C = 0$		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	$V_{CS} = 3$ V, $I_C = 0$		2.8		pF

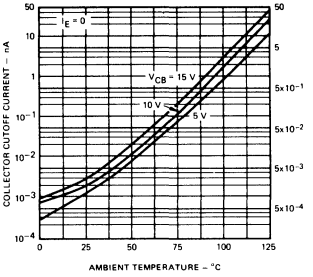
NOTES:
1. μA3046 and μA3086 derate at 6.67 mW/°C for $T_A > 55°C$, μA3045 at 8 mW/°C for $T_A > 75°C$.
2. Substrate (Pin 13) must be connected to the most negative voltage to maintain normal operation.

ELECTRICAL CHARACTERISTICS FOR μA3086: $T_A = 25°C$ unless otherwise specified

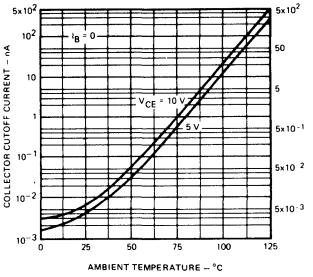
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	$I_C = 10\,\mu A$, $I_E = 0$	20	60		V
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	15	24		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$I_C = 10\,\mu A$, $I_C = 0$	20	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	$I_E = 10\,\mu A$, $I_C = 0$	5.0	7.0		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 10$ V, $I_E = 0$		0.002	100	nA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 10$ V, $I_B = 0$		See Curve	5.0	μA
h_{FE}	Static Forward Current-Transfer Ratio (Static Beta)	$V_{CE} = 3$ V, $I_C = 10$ mA $I_C = 1$ mA $I_C = 10\,\mu A$	40	100 100 54		
	Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{IO1} - I_{IO2}\rvert$	$V_{CE} = 3$ V, $I_C = 1$ mA				μA
V_{BE}	Base-to-Emitter Voltage	$V_{CE} = 3$ V, $I_E = 1$ mA $I_E = 10$ mA		0.715 0.800		V
	Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2}\rvert$	$V_{CE} = 3$ V, $I_C = 1$ mA				mV
	Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4}\rvert$, $\lvert V_{BE_4} - V_{BE_5}\rvert$, $\lvert V_{BE_5} - V_{BE_3}\rvert$	$V_{CE} = 3$ V, $I_C = 1$ mA				mV
$\frac{\Delta V_{BE}}{\Delta T}$	Temperature Coefficient of Base-to-Emitter Voltage	$V_{CE} = 3$ V, $I_C = 1$ mA		−1.9		mV/°C
$V_{CE(sat)}$	Collector-to-Emitter Saturation Voltage	$I_B = 1$ mA, $I_C = 10$ mA		0.23		V
$\frac{\lvert\Delta V_{10}\rvert}{\Delta T}$	Temperature Coefficient: Magnitude of Input-Offset Voltage	$V_{CE} = 3$ V, $I_C = 1$ mA				μV/°C
NF	Low Frequency Noise Figure	$f = 1$ kHz, $V_{CE} = 3$ V, $I_C = 100\,\mu A$ $R_S = 1$ kΩ		3.25		dB
	Low Frequency, Small-Signal Equivalent-Circuit Characteristics:					
h_{fe} h_{ie} h_{oe} h_{re}	Forward Current-Transfer Ratio Short-Circuit Input Resistance Open-Circuit Output Conductance Open-Circuit Reverse Voltage-Transfer Ratio	$f = 1$ kHz, $V_{CE} = 3$ V, $I_C = 1$ mA		110 3.5 15.6 1.8×10^{-4}		 kΩ μmho
	Admittance Characteristics:					
Y_{fe} Y_{ie} Y_{oe} Y_{re}	Forward Transfer Admittance Input Admittance Output Admittance Reverse Transfer Admittance	$f = 1$ MHz, $V_{CE} = 3$ V, $I_C = 1$ mA		31-j 1.5 0.3+j0.04 0.001+j0.03 See Curve		
f_T	Gain-Bandwidth Product	$V_{CE} = 3$ V, $I_C = 3$ mA	300	550		MHz
C_{EB}	Emitter-to-Base Capacitance	$V_{EB} = 3$ V, $I_E = 0$		0.6		pF
C_{CB}	Collector-to-Base Capacitance	$V_{CB} = 3$ V, $I_C = 0$		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	$V_{CS} = 3$ V, $I_C = 0$		2.8		pF

TYPICAL PERFORMANCE CURVES FOR μA3045/3046/3086

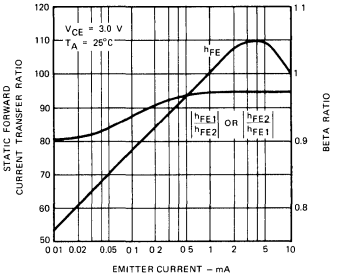
COLLECTOR-TO-BASE CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



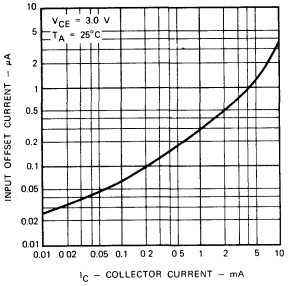
COLLECTOR-TO-EMITTER CUTOFF CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



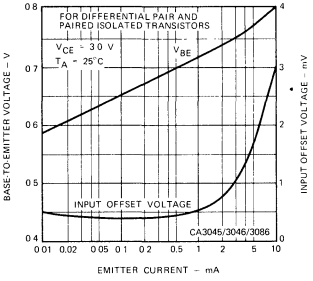
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q1, Q2 AS A FUNCTION OF EMITTER CURRENT



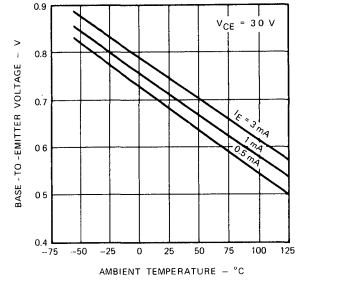
INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q1, Q2 AS A FUNCTION OF COLLECTOR CURRENT



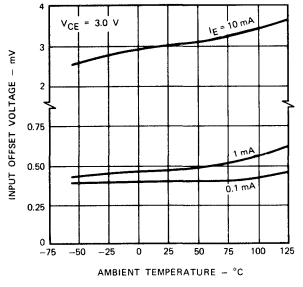
STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE AS A FUNCTION EMITTER CURRENT



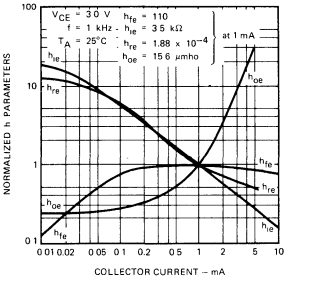
BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AS A FUNCTION OF AMBIENT TEMPERATURE FOR EACH TRANSISTOR



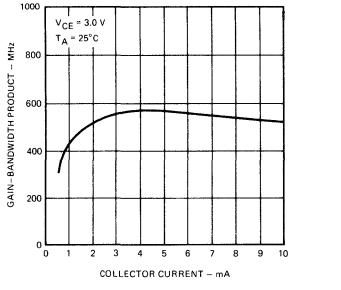
INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS AS A FUNCTION OF AMBIENT TEMPERATURE



NORMALIZED h PARAMETERS AS A FUNCTION OF COLLECTOR CURRENT



GAIN-BANDWIDTH PRODUCT AS A FUNCTION OF COLLECTOR CURRENT



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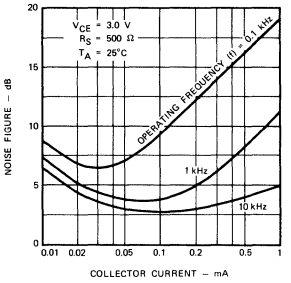
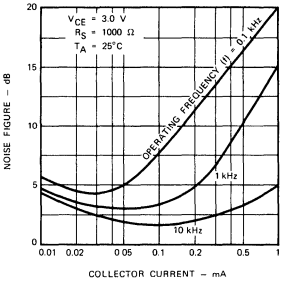
TYPICAL PERFORMANCE CURVES FOR μA3045/3046/3086 (Cont'd)

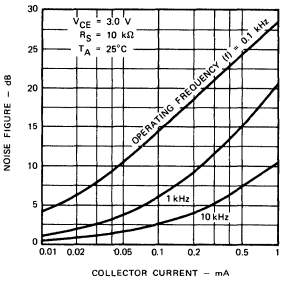
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT



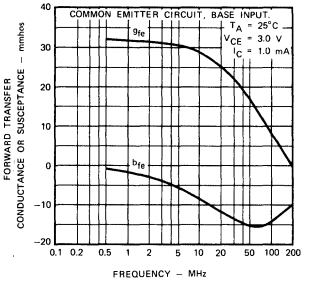
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT



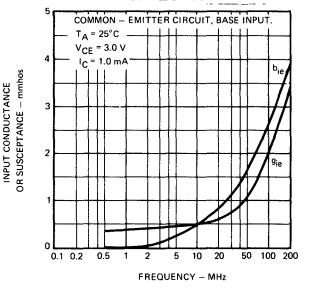
NOISE FIGURE AS A FUNCTION OF COLLECTOR CURRENT



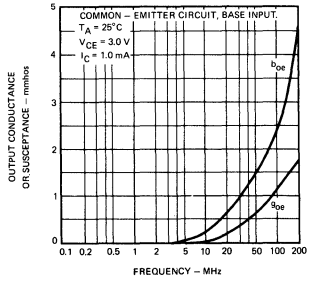
FORWARD TRANSFER ADMITTANCE AS A FUNCTION OF FREQUENCY



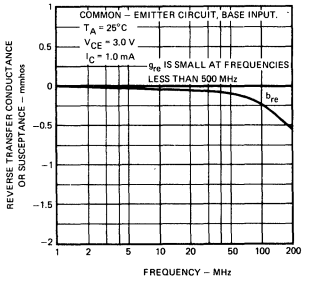
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



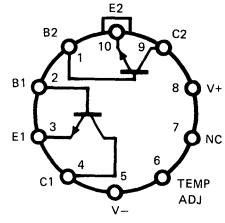
REVERSE TRANSFER ADMITTANCE AS A FUNCTION OF FREQUENCY



μA726
TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA726 is a Monolithic Transistor Pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers. It is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

CONNECTION DIAGRAM
10-PIN METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5U
PACKAGE CODE H



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	
Military (μA726)	−55°C to +125°C
Commercial (μA726C)	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering, 60 seconds)	300°C
Supply Voltage	±18V
Internal Power Dissipation	500mW

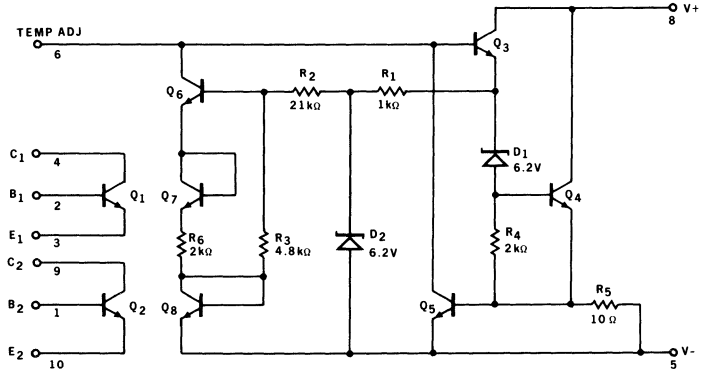
MAXIMUM RATINGS FOR EACH TRANSISTOR

Collector-to-Emitter Voltage, V_{CEO}	30V
Collector-to-Base Voltage, V_{CBO}	40V
Collector-to-Substrate Voltage, V_{CIO}	40V
Emitter-to-Base Voltage, V_{EBO}	5V
Collector Current, I_C	5mA

ORDER INFORMATION

TYPE	PART NO.
μA726	μA726HM
μA726C	μA726HC

EQUIVALENT CIRCUIT



*Planar is a patented Fairchild process.

μA726

ELECTRICAL CHARACTERISTICS: $-55°C \leq T_A \leq +125°C$, $V_S = \pm 15V$, $R_{adj} = 62k\Omega$ unless otherwise specified.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current	$I_C = 10\mu A$, $V_{CE} = 5V$		10	50	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		50	200	nA
Average Input Bias Current	$I_C = 10\mu A$, $V_{CE} = 5V$		50	150	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		250	500	nA
Offset Voltage Change	$I_C = 10\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100k\Omega$		0.3	6.0	mV
	$I_C = 100\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$		0.2	1.0	μV/°C
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$		0.2	1.0	μV/°C
Input Offset Current Drift	$I_C = 10\mu A$, $V_{CE} = 5V$		10		pA/°C
	$I_C = 100\mu A$, $V_{CE} = 5V$		30		pA/°C
Supply Voltage Rejection Ratio	$10\mu A \leq I_C \leq 100\mu A$, $R_S \leq 50\Omega$,		25		μV/V
Low Frequency Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$ BW = .001 Hz to 0.1 Hz		4.0		μV p-p
Broadband Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$ BW = 0.1 Hz to 10kHz		10		μV p-p
Long-term Drift	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	f = 20MHz, $I_C = 100\mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\mu A$, $I_C = 1mA$		0.5	1.0	V

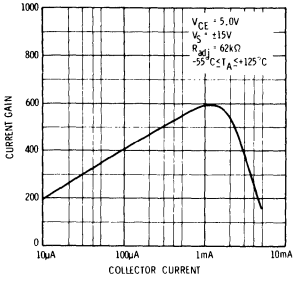
μA726C

ELECTRICAL CHARACTERISTICS: $0°C \leq T_A \leq +85°C$, $V_S = \pm 15V$, $R_{adj} = 75k\Omega$ unless otherwise specified.

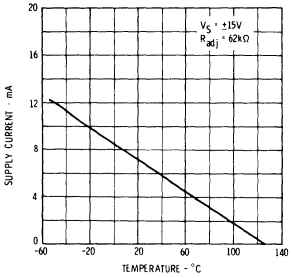
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$10\mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	3.0	mV
Input Offset Current	$I_C = 10\mu A$, $V_{CE} = 5V$		10	100	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		50	400	nA
Average Input Bias Current	$I_C = 10\mu A$, $V_{CE} = 5V$		50	300	nA
	$I_C = 100\mu A$, $V_{CE} = 5V$		250	1000	nA
Offset Voltage Change	$I_C = 10\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100k\Omega$		0.3	6.0	mV
	$I_C = 100\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$I_C = 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		0.2	2.0	μV/°C
Input Offset Current Drift	$I_C = 10\mu A$, $V_{CE} = 5V$		10		pA/°C
	$I_C = 100\mu A$, $V_{CE} = 5V$		30		pA/°C
Supply Voltage Rejection Ratio	$I_C = 100\mu A$, $R_S = 50\Omega$		25		μV/V
Low Frequency Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.001 Hz to 0.1 Hz		4.0		μV p-p
Broadband Noise	$I_C = 10\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10kHz		10		μV p-p
Long-Term Drift	$I_C = 100\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	f = 20MHz, $I_C = 100\mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\mu A$, $I_C = 1mA$		0.5	1.0	V

TYPICAL PERFORMANCE CURVES FOR μA726

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT

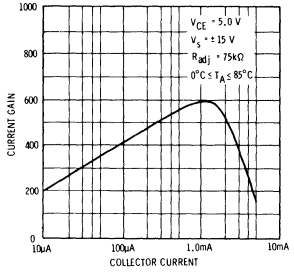


SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

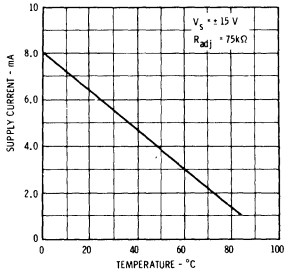


TYPICAL PERFORMANCE CURVES FOR μA726C

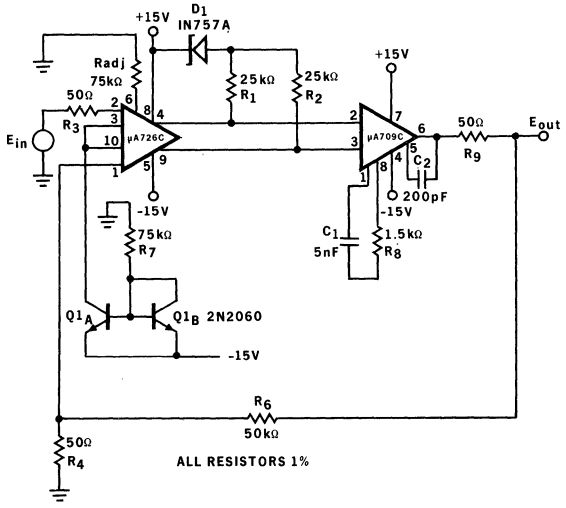
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 AMPLIFIER CIRCUIT



9

μA555
SINGLE TIMING CIRCUIT
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA555 Timing Circuit is a very stable controller for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied ending the time-out.

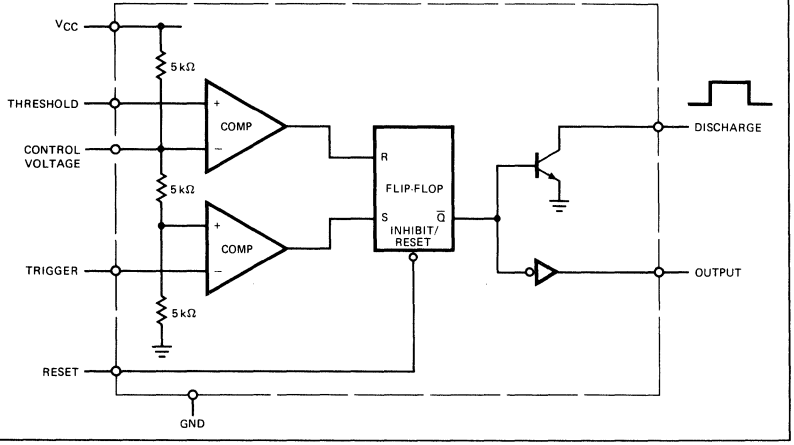
The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

- **MICROSECONDS THROUGH HOURS TIMING CONTROL**
- **ASTABLE OR MONOSTABLE OPERATING MODES**
- **ADJUSTABLE DUTY CYCLE**
- **200 mA SINK OR SOURCE OUTPUT CURRENT CAPABILITY**
- **TTL OUTPUT DRIVE CAPABILITY**
- **TEMPERATURE STABILITY OF 0.005% PER °C**
- **NORMALLY ON OR NORMALLY OFF OUTPUT**
- **DIRECT REPLACEMENT FOR SE555/NE555**

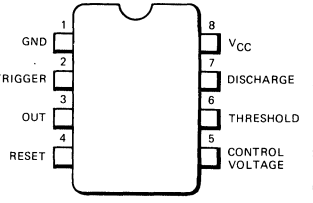
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18 V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
μA555TC/HC	0°C to +70°C
μA555HM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature	
Plastic Mini DIP(9T) (Soldering, 10 s)	260°C
Metal Can (5T) (Soldering, 60 s)	300°C

BLOCK DIAGRAM



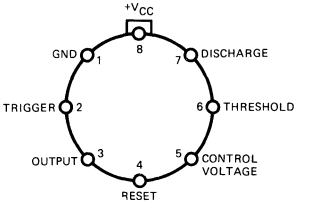
CONNECTION DIAGRAMS
8-PIN MINI DIP
(TOP VIEW)
PACKAGE OUTLINE 9T



ORDER INFORMATION

TYPE	PART NO.
μA555	μA555TC

8-PIN TO-100
(TOP VIEW)
PACKAGE OUTLINE 5T



ORDER INFORMATION

TYPE	PART NO.
μA555	μA555HM
μA555	μA555HC

ELECTRICAL CHARACTERISTICS: T_A= 25°C, V_{CC}= +5.0 V to +15 V, unless otherwise specified

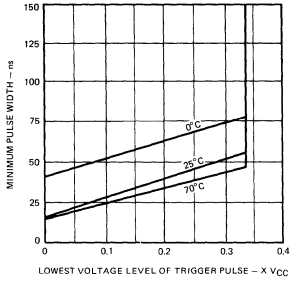
CHARACTERISTICS	TEST CONDITIONS	μA555HM			μA555TC/HC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5.0 V, R_L = ∞		3.0	5.0		3.0	6.0	mA
	V_{CC} = 15 V, R_L = ∞ LOW State (Note 1)		10	12		10	15	mA
Timing Error								
Initial Accuracy	R_A, R_B = 1 kΩ to 100 kΩ		0.5	2.0		1.0		%
Drift with Temperature	C = 0.1 μF (Note 2)		30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%V
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15 V	4.8	5.0	5.2		5.0		V
	V_{CC} = 5.0 V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15 V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5.0 V	2.9	3.33	3.8	2.6	3.33	4.0	V
Output Voltage Drop (LOW)	V_{CC} = 15 V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2.0	2.2		2.0	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5.0 V							
	I_{SINK} = 8.0 mA		0.1	0.25				V
	I_{SINK} = 5.0 mA					0.25	0.35	V
Output Voltage Drop (HIGH)	I_{SOURCE} = 200 mA							
	V_{CC} = 15 V		12.5			12.5		V
	I_{SOURCE} = 100 mA							
	V_{CC} = 15 V	13	13.3		12.75	13.3		V
	V_{CC} = 5.0 V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

NOTES:
1. Supply Current is typically 1.0 mA less when output is HIGH.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of R_A + R_B. For 15 V operation, the max total R = 20 MΩ.
4. For operating at elevated temperatures the device must be derated based on a +125°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

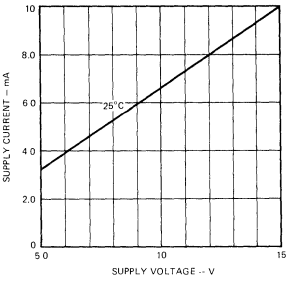
9

TYPICAL PERFORMANCE CURVES

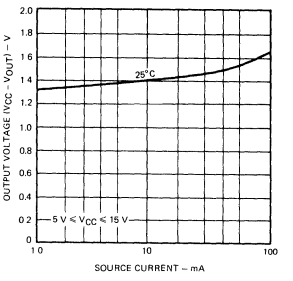
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



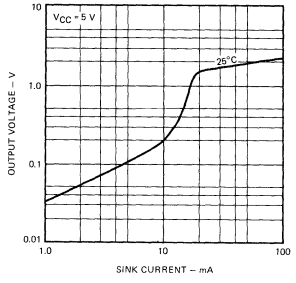
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



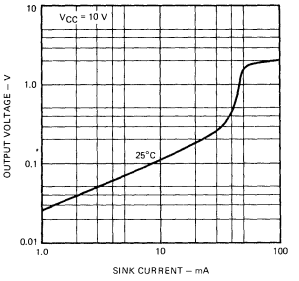
HIGH OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SOURCE CURRENT



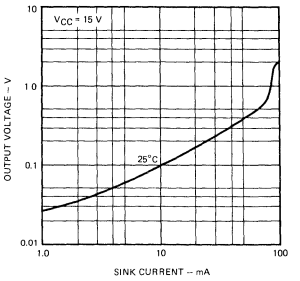
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



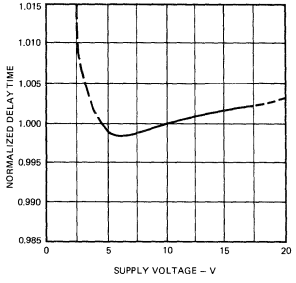
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



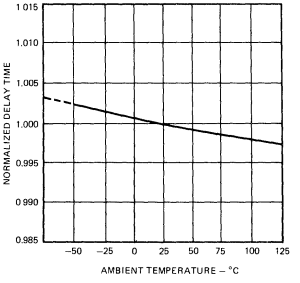
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



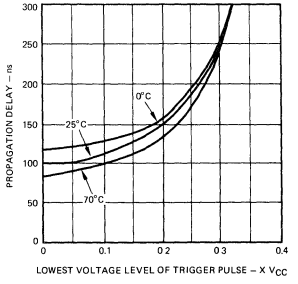
DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE



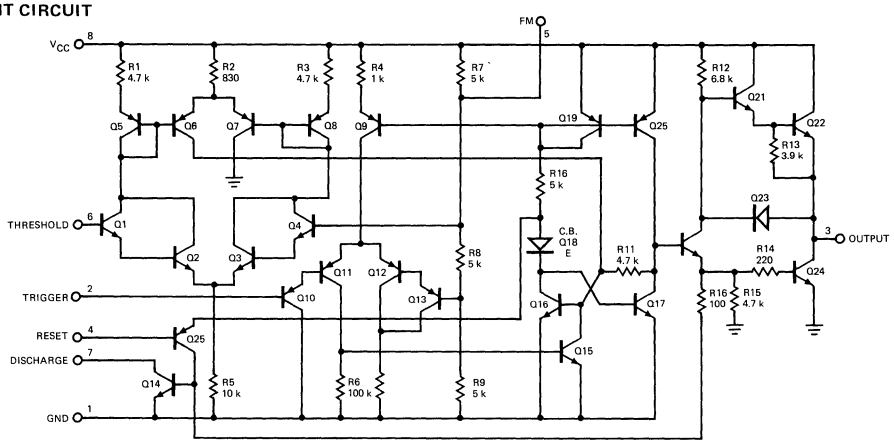
DELAY TIME AS A FUNCTION OF AMBIENT TEMPERATURE



PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



EQUIVALENT CIRCUIT



TYPICAL APPLICATIONS

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to Figure 1 the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 2, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH. The voltage across the capacitor, increases exponentially with the time constant $\tau = R1C1$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 2 shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R1C1$ and is easily determined by Figure 3. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the Trigger terminal (lead 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied high to avoid any possibility of false triggering.

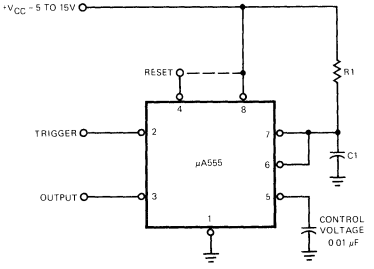


Fig. 1

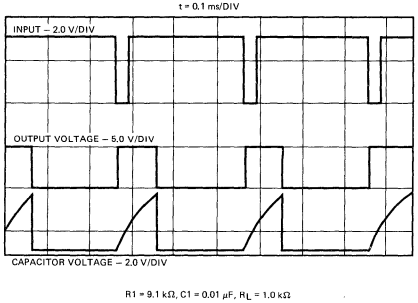


Fig. 2

TIME DELAY AS A FUNCTION OF R1 AND C1

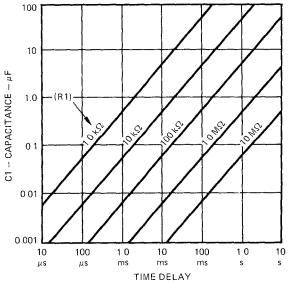


Fig. 3

TYPICAL APPLICATIONS (Cont'd)

ASTABLE OPERATION

When the circuit is connected as shown in Figure 4 (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by Figure 6.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

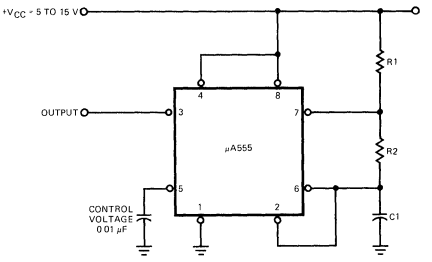


Fig. 4

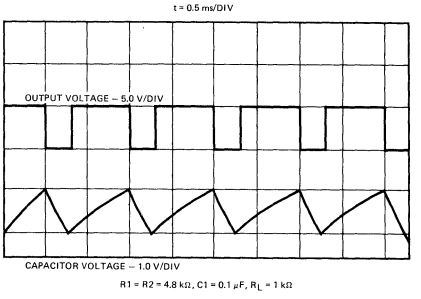


Fig. 5

FREE RUNNING FREQUENCY AS A FUNCTION OF R1, R2 AND C1

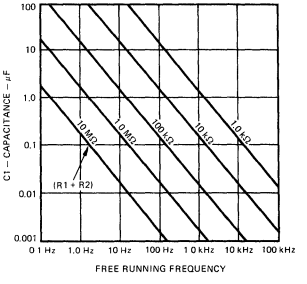


Fig. 6

μA556
DUAL TIMING CIRCUIT
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA556 Timing Circuits are very stable controllers for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied, ending the time-out.

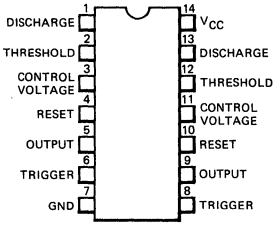
The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

The μA556 Dual Timing Circuit is a pair of 555s for use in sequential timing or applications requiring multiple timers.

- **MICROSECONDS THROUGH HOURS TIMING CONTROL**
- **ASTABLE OR MONOSTABLE OPERATING MODES**
- **ADJUSTABLE DUTY CYCLE**
- **200 mA SINK OR SOURCE OUTPUT CURRENT CAPABILITY**
- **TTL OUTPUT DRIVE CAPABILITY**
- **TEMPERATURE STABILITY OF 0.005% PER °C**
- **NORMALLY ON OR NORMALLY OFF OUTPUT**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



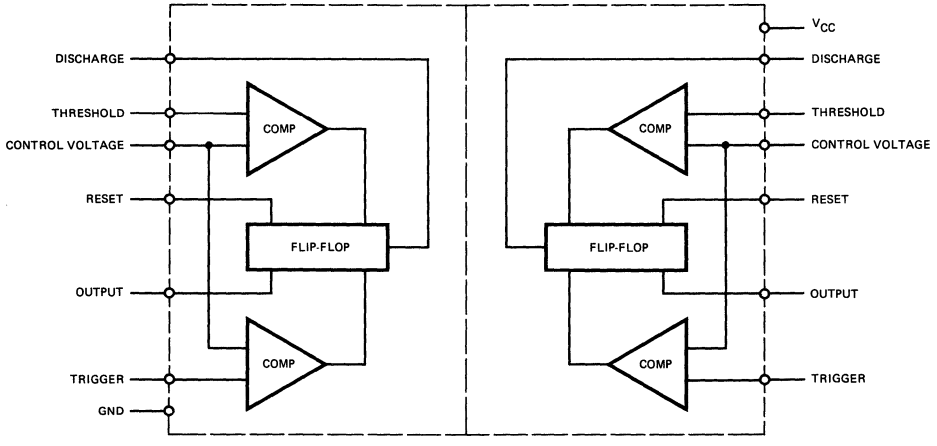
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18 V
Power Dissipation	600 mW
Operating Temperature Ranges	
μA556 DC/PC	0°C to +70°C
μA556DM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Pin Temperature (Soldering)	
(10 s) Plastic DIP (9A)	260°C
(60 s) Ceramic DIP (6A)	300°C

ORDER INFORMATION

TYPE	PART NO.
μA556	μA556DC
μA556	μA556DM
μA556	μA556PC

BLOCK DIAGRAM



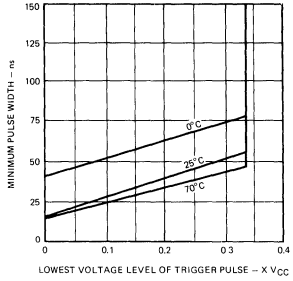
ELECTRICAL CHARACTERISTICS: T_A = 25°C, V_{CC} = +5.0 V to +15 V, unless otherwise specified

CHARACTERISTICS	TEST CONDITIONS	μA556DM			μA556DC/PC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current (Total)	V_{CC} = 5.0 V, R_L = ∞		6.0	10		6.0	12	mA
	V_{CC} = 15 V, R_L = ∞ LOW State (Note 1)		20	22		20	28	mA
Timing Error (Monostable)								
Initial Accuracy	R_A = 2 kΩ to 100 kΩ		0.5	1.5		0.75		%
Drift with Temperature	C = 0.1 μF (Note 2)		30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%V
Timing Error (Astable)								
Initial Accuracy	R_A, R_B = 2 kΩ to 100 kΩ		1.5			2.25		%
Drift with Temperature	C = 0.1 μF (Note 2)		90			150		ppm/°C
Drift with Supply Voltage			0.15			0.3		%V
Threshold Voltage			2/3			2/3		X V_{CC}
Threshold Current	Note 3		30	100		30	100	nA
Trigger Voltage	V_{CC} = 15 V	4.8	5.0	5.2		5.0		V
	V_{CC} = 5.0 V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Control Voltage Level	V_{CC} = 15 V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5.0 V	2.9	3.33	3.8	2.6	3.33	4.0	V
Output Voltage (LOW)	V_{CC} = 15 V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2.0	2.25		2.0	2.75	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5.0 V							
	I_{SINK} = 8.0 mA		0.1	0.25				V
	I_{SINK} = 5.0 mA					0.25	0.35	V
Output Voltage (HIGH)	I_{SOURCE} = 200 mA							
	V_{CC} = 15 V		12.5			12.5		V
	I_{SOURCE} = 100 mA							
	V_{CC} = 15 V	13.0	13.3		12.75	13.3		V
	V_{CC} = 5.0V	3.0	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Discharge Leakage Current			20	100		20	100	nA
Matching Characteristics (Note 4)								
Initial Timing Accuracy			0.05	0.1		0.1	0.2	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%V

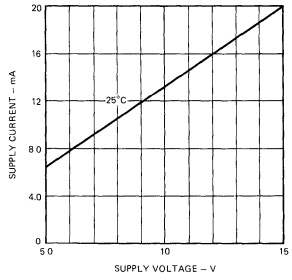
NOTES:
1. Supply current when output is HIGH is typically 1.0 mA less.
2. Tested at V_{CC} = 5 V and V_{CC} = 15 V.
3. This will determine the maximum value of R_A + R_B for 15 V operation. The maximum total R = 20 MΩ.
4. Matching characteristics refer to the difference between performance characteristics of each timer section.

TYPICAL PERFORMANCE CURVES

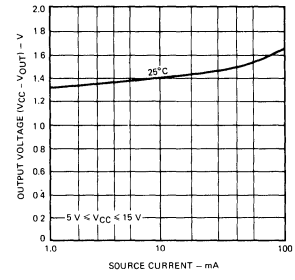
MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



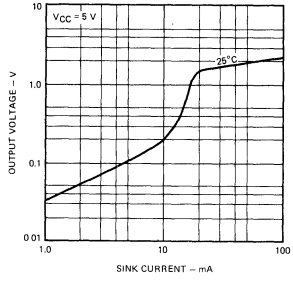
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



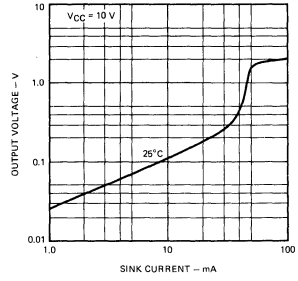
HIGH OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SOURCE CURRENT



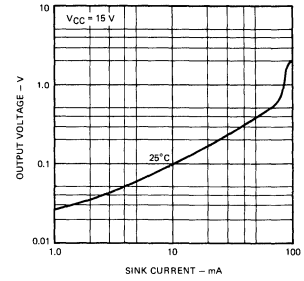
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



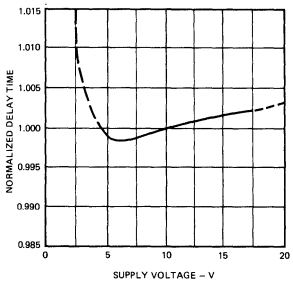
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



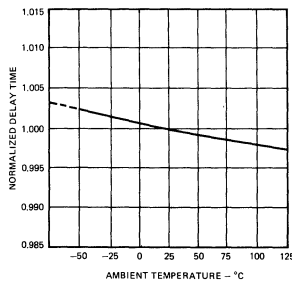
LOW OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT SINK CURRENT



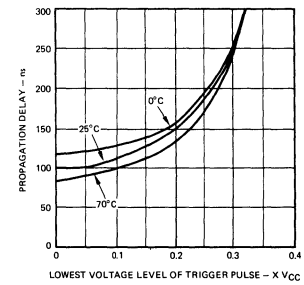
DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE



DELAY TIME AS A FUNCTION OF AMBIENT TEMPERATURE

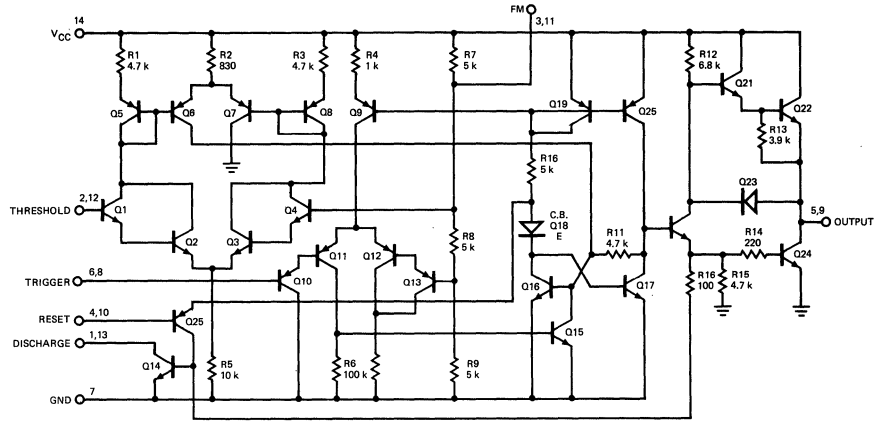


PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



9

EQUIVALENT CIRCUIT (One Half of μA556)



TYPICAL APPLICATIONS

MONOSTABLE OPERATION

In the monostable mode, the timer functions as a one-shot. Referring to Figure 1 the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 6, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH. The voltage across the capacitor, increases exponentially with the time constant $\tau = R1C1$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. Figure 2 shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative-going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R1C1$ and is easily determined by Figure 3. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the Trigger terminal (lead 6) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied high to avoid any possibility of false triggering.

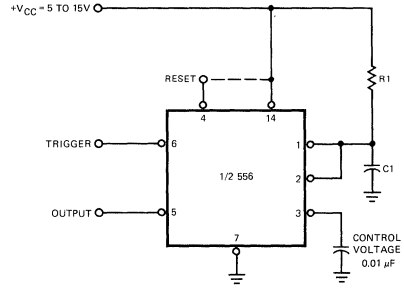


Fig. 1

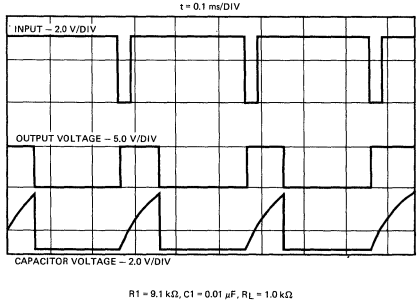


Fig. 2

TIME DELAY AS A FUNCTION OF R1 AND C1

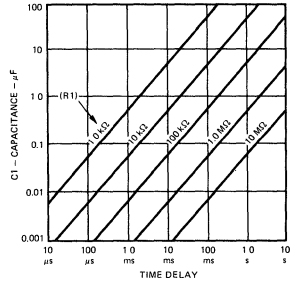


Fig. 3

TYPICAL APPLICATIONS (Cont'd)

ASTABLE OPERATION

When the circuit is connected as shown in Figure 4 (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by Figure 6.

The duty cycle is given by:

$$D = \frac{R2}{R1 + 2R2}$$

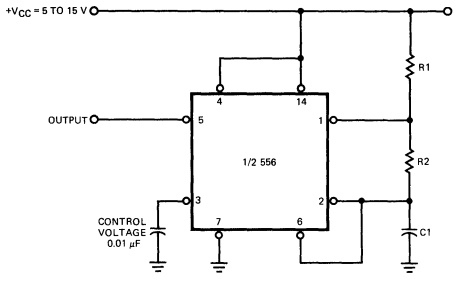
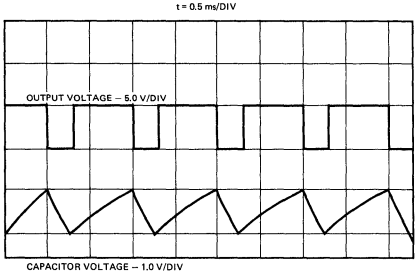


Fig. 4



R1 = R2 = 4.8 kΩ, C1 = 0.1 μF, R_L = 1 kΩ

Fig. 5

FREE RUNNING FREQUENCY AS A FUNCTION OF R1, R2 AND C1

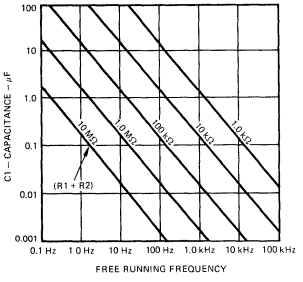


Fig. 6

9

μA2240

PROGRAMMABLE TIMER/COUNTER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

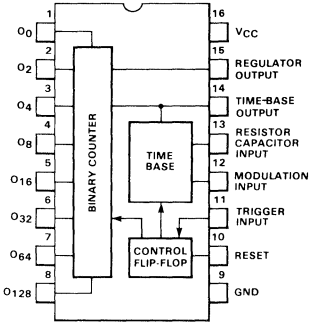
GENERAL DESCRIPTION – The μA2240 Programmable Timer/Counter is a monolithic controller capable of producing accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time-base oscillator, programmable 8-bit counter and control flip-flop. An external resistor capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, 255 frequencies or pulse patterns can be generated from a single RC network. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and DTL compatible for easy interface with digital system. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

- **ACCURATE TIMING FROM MICROSECONDS TO DAYS**
- **PROGRAMMABLE DELAYS FROM 1 RC TO 255 RC**
- **TTL, DTL AND CMOS COMPATIBLE OUTPUTS**
- **TIMING DIRECTLY PROPORTIONAL TO RC TIME CONSTANT**
- **HIGH ACCURACY – 0.5%**
- **EXTERNAL SYNC AND MODULATION CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE**
- **EXCELLENT SUPPLY VOLTAGE REJECTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18 V
Output Current	10 mA
Output Voltage	18 V
Regulator Output Current	5 mA
Maximum Power Dissipation, Note 1	
Package Code D (Ceramic)	750 mW
Code P (Plastic)	650 mW
Operating Temperature Range Package	
Military (μA2240)	−55°C to +125°C
Commercial (μA2240C)	0°C to 70°C

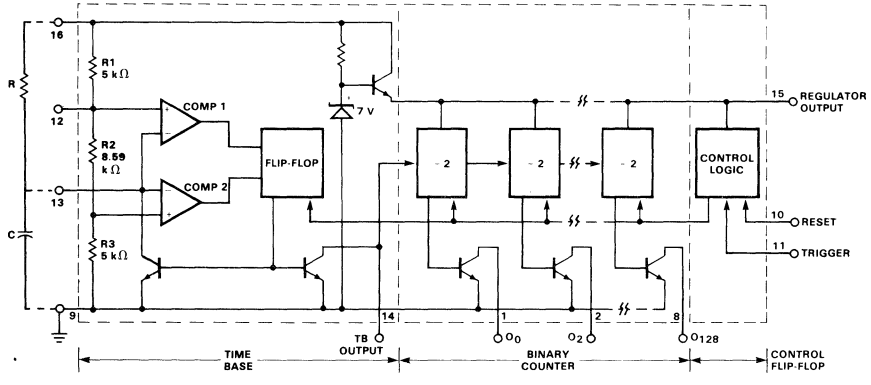
CONNECTION DIAGRAM
16-PIN DIP (TOP VIEW)
PACKAGE OUTLINES 7B, 9B
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μA2240	μA2240DM
μA2240C	μA2240DC
μA2240C	μA2240PC

BLOCK DIAGRAM



NOTE 1: Above 25°C ambient derate linearly at 6.2 mW/°C for Package Code D and at 5.3 mW/°C for Package Code P.

ELECTRICAL CHARACTERISTICS: See Test Circuit Fig. 28, V_{CC} = 5 V, T_A = 25°C, R = 10 kΩ, C = 0.1 μF, unless otherwise noted

CHARACTERISTICS	CONDITIONS	μA2240			μA2240C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
GENERAL CHARACTERISTICS								
Supply Voltage	For $V_{CC} \leq$ 4.5 V, Short Pin 15 to Pin 16	4.0		15	4.0		15	V
Supply Current								
Total Circuit	V_{CC} = 5 V, V_{TR} = 0, V_{RS} = 5 V		3.5	6.0		4.0	7.0	mA
	V_{CC} = 15 V, V_{TR} = 0, V_{RS} = 5 V		12	16		13	18	mA
Counter Only	See Test Circuit, Figure 29		1			1.5		mA
Regulator Output, V_{Reg}	Measured at Pin 15, V_{CC} = 5 V	4.1	4.4		3.9	4.4		V
	V_{CC} = 15 V, See Test Circuit, Figure 30	6.0	6.3	6.6	5.8	6.3	6.8	V
TIME BASE SECTION								
Timing Accuracy (Note 2)	V_{RS} = 0, V_{TR} = 5 V		0.5	2.0		0.5	5.0	%
Temperature Drift	V_{CC} = 5 V, 0°C $\leq T_J \leq$ 75°C		150	300		200		ppm/°C
	V_{CC} = 15 V		80			80		ppm/°C
Supply Drift	$V_{CC} \geq$ 8 V, See Figure 23		0.05	0.2		0.08	0.3	%/V
Max Frequency	R = 1 kΩ, C = 0.007 μF	100	130			130		kHz
Modulation Voltage Level	Measured at Pin 12 V_{CC} = 5 V	3.00	3.50	4.0	2.80	3.50	4.20	V
	V_{CC} = 15 V		10.5			10.5		V
Recommended Range of Timing Components	See Figure 20							
Timing Resistor, R		0.001		10	0.001		10	MΩ
Timing Capacitor, C		0.007		1000	0.01		1000	μF
TRIGGER/RESET CONTROLS								
Trigger	Measured at Pin 11, V_{RS} = 0							
Trigger Threshold			1.4	2.0		1.4	2.0	V
Trigger Current	V_{RS} = 0, V_{TR} = 2 V		8.0			10		μA
Impedance			25			25		kΩ
Response Time (Note 3)			1.0			1.0		μs
Reset	Measured at Pin 10, V_{TR} = 0							
Reset Threshold			1.4	2.0		1.4	2.0	V
Reset Current	V_{TR} = 0, V_{RS} = 2 V		8.0			10		μA
Impedance			25			25		kΩ
Response Time (Note 3)			0.8			0.8		μs
COUNTER SECTION	See Test Circuit, Figure 30							
Max Toggle Rate	V_{RS} = 0, V_{TR} = 5 V Measured at Pin 14	0.8	1.5			1.5		MHz
Input Impedance			20			20		kΩ
Input Threshold		1.0	1.4		1.0	1.4		V
Output:	Measured at Pins 1 through 8							
Rise Time	R_L = 3 kΩ, C_L = 10 pF		180			180		ns
Fall Time			180			180		ns
Sink Current	$V_{OL} \leq$ 0.4 V	3.0	5.0		2.0	4.0		mA
Leakage Current	V_{OH} = 15 V		0.01	8.0		0.01	15	μA

NOTES:
2. Timing error solely introduced by μA2240, measured as % of ideal time base period of T = 1.00 RC.
3. Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

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FUNCTIONAL DESCRIPTION

(Figure 1 and Block Diagram, page 1)

When power is applied to the μA2240 with no trigger or reset inputs, the circuit starts with all outputs HIGH. Application of a positive-going trigger pulse to TRIG, pin 11, initiates the timing cycle. The Trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive-going reset pulse is applied to R, pin 10.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a Reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.

In most timing applications, one or more of the counter outputs are connected to the Reset terminal with S1 closed (*Figure 3*). The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the Reset terminal (switch S1 open), the circuit operates in an astable or free-running mode, following to a trigger input.

Important Operating Information

- Ground connection is pin 9.
- Reset R (pin 10) sets all outputs HIGH.
- Trigger TRIG (pin 11) sets all outputs LOW.
- Time-base TBO (pin 14) can be disabled by bringing the RC input (pin 13) LOW via a 1 k resistor.
- Normal Time-base Output TBO (pin 14) is a negative-going pulse greater than 500 ns.

  Note: Under the conditions of high supply voltages (V_{CC} > 7 V) and low values of timing capacitor (C < 0.1 μF, the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from TBO (pin 14) to ground (pin 9).
- Reset (pin 10) stops the time-base oscillator.
- Outputs $O_0 \ldots O_{128}$ (pins 1-8) sink 2 mA current with $V_{OL} \leq 0.4$ V.
- For use with external clock, minimum clock pulse amplitude should be 3 V, with greater than 1 μs pulse duration.

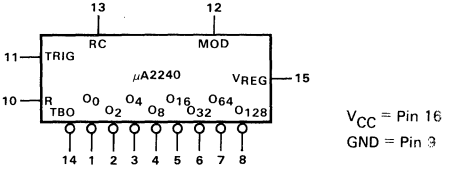


Fig. 1. Logic Diagram

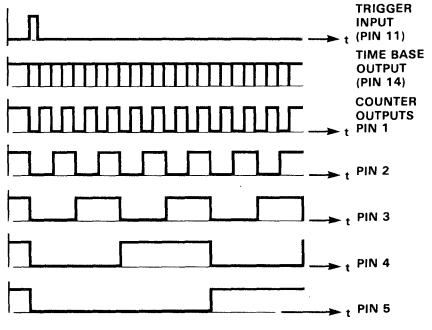


Fig. 2. Timing Diagram of Output Waveforms

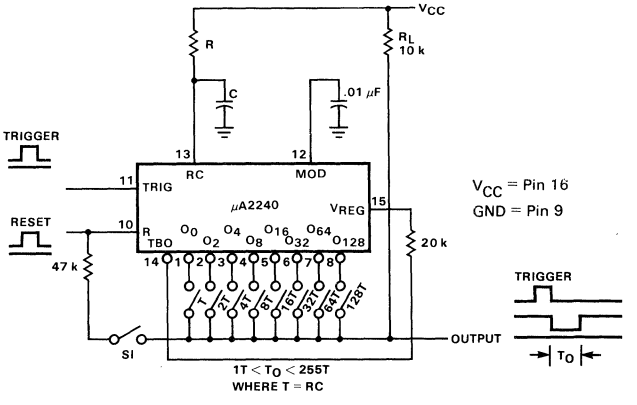


Fig. 3. Basic Circuit Connection for Timing Applications
Monostable: S1 Closed
Astable: S1 Open

CIRCUIT CONTROLS

Counter Outputs (O_0 . . . O_{128}, pins 1 thru 8)

The binary counter outputs are buffered open-collector type stages, as shown in the block diagram on page 1. Each output is capable of sinking 2 mA at 0.4 V V_{OL}. In the Reset condition, all the counter outputs are HIGH or in the non-conducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2*. The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the Programming section.

Reset and Trigger Inputs (R and TRIG, pins 10 and 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11 respectively. The threshold level for these controls is approximately two diode drops (≈ 1.4 V) above ground. Minimum pulse widths for reset and trigger inputs are shown in *Figure 22*. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, pin 12)

The oscillator time-base period, T, can be modulated by applying a dc voltage to MOD, pin 12 (see *Figure 25*). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, pin 12, as shown in *Figure 4*. Recommended sync pulse widths and amplitudes are also given.

The time base can be synchronized by setting the time-base period T to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m)$$

where

m is an integer, $1 \leq m \leq 10$

Figure 5 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

RC Terminal (pin 13)

The time-base period T is determined by the external RC network connected to RC, pin 13. When the time base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC.

Time-Base Output (TBO, pin 14)

The time-base output is an open-collector type stage as shown in the block diagram, page, 1, and requires a 20 kΩ pull-up resistor to pin 15 for proper circuit operation. In the Reset state, the time-base output is HIGH. After triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of *Figure 2*. The time-base output is internally connected to the binary-counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative-going edge of the timing or clock pulses generated at TBO, pin 14. The trigger threshold for the counter section is ≈ +1.4 V. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

When using high supply voltages ($V_{CC} > 7$ V) and a small-value timing capacitor ($C < 0.1$ μF), the pulse width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from pin 14 to ground.

9

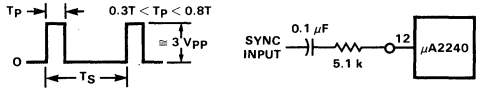


Fig. 4. Operation with External Sync. Signal

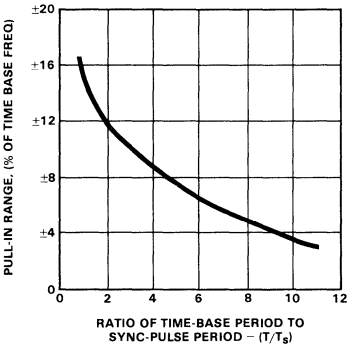


Fig. 5. Typical Pull-in Range for Harmonic Synchronization

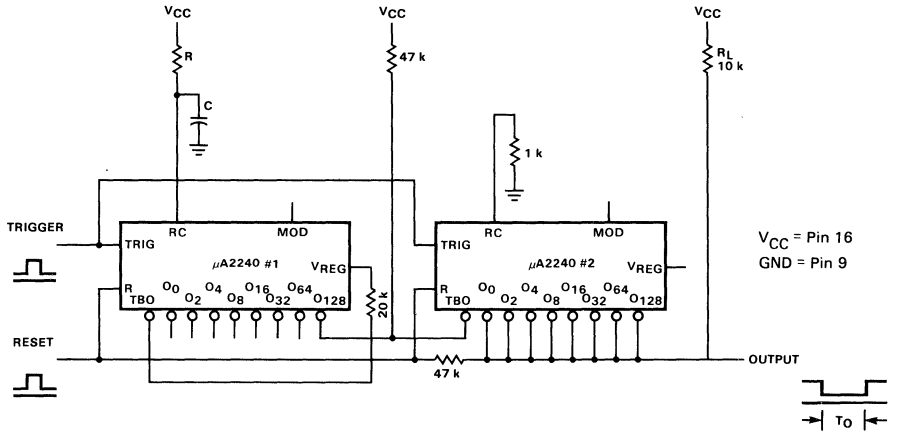


Fig. 6. Cascaded Operation for Long Delays

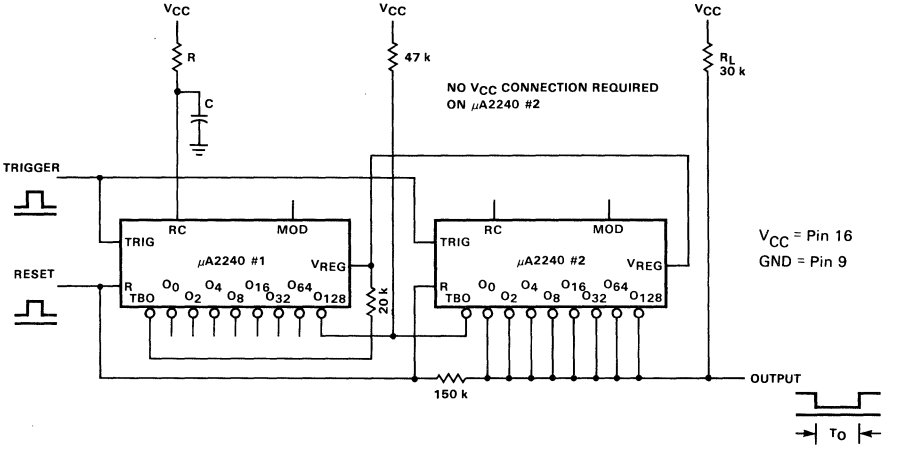


Fig. 7. Low Power Operation of Cascaded Timers

Regulator Output (V_{REG}, pin 15)

The regulator output V_{REG} is used internally to drive the binary counter and the control logic. This terminal can also be used as a supply to additional μA2240 circuits when several timer circuits are cascaded (see *Figure 7*) to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time-base, pin 15 should be shorted to pin 16.

MONOSTABLE OPERATION

Precision Timing

In precision timing applications, the μA2240 is used in its monostable or self-resetting mode. The generalized circuit connection for this application is shown in *Figure 3*. The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration, T_O, and then returns to the HIGH state. The duration of the timing cycle T_O is given as:

$$T_O = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at RC pin 13 (see *Figure 21*) and N is an integer in the range of $1 \leqslant N \leqslant 255$ as determined by the combination of counter outputs $O_0 \ldots O_{128}$, pins 1 through 8, connected to the output bus.

Counter-Output Programming

The binary-counter outputs, $O_0 \ldots O_{128}$, pins 1 through 8 are open-collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each counter output can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32 T. Similarly, if pins 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)\,T = 49$ T. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1\,T \leqslant T_O \leqslant 255$ T.

Ultra Long Time-Delay Application

Two μA2240 units can be cascaded as shown in *Figure 6* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}536$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the Reset and the Trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 7*. In this case, the V_{CC} terminal (pin 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (pins 15) of both units together.

ASTABLE OPERATION

The μA2240 can be operated in its astable or free-running mode by disconnecting the Reset terminal (pin 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free-running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its Reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely. in astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Binary Pattern Generation

In astable operation, as shown in *Figure 8*, the output of the μA2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2* which shows the phase relations between the counter outputs. *Figures 10* and *11* show some

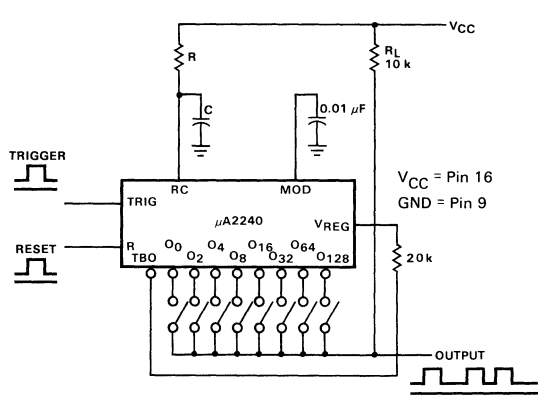


Fig. 8. Operation with External Trigger and Reset Inputs

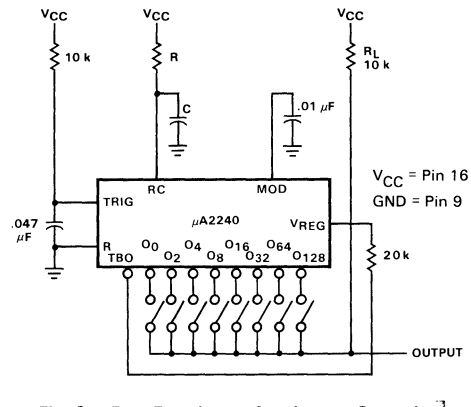


Fig. 9. Free-Running or Continuous Operation

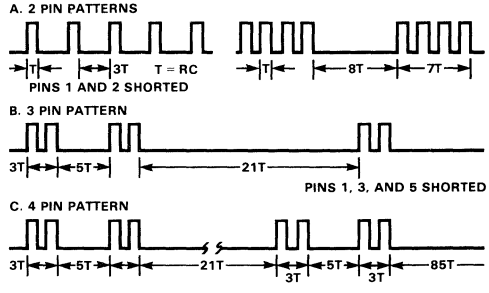


Fig. 10. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

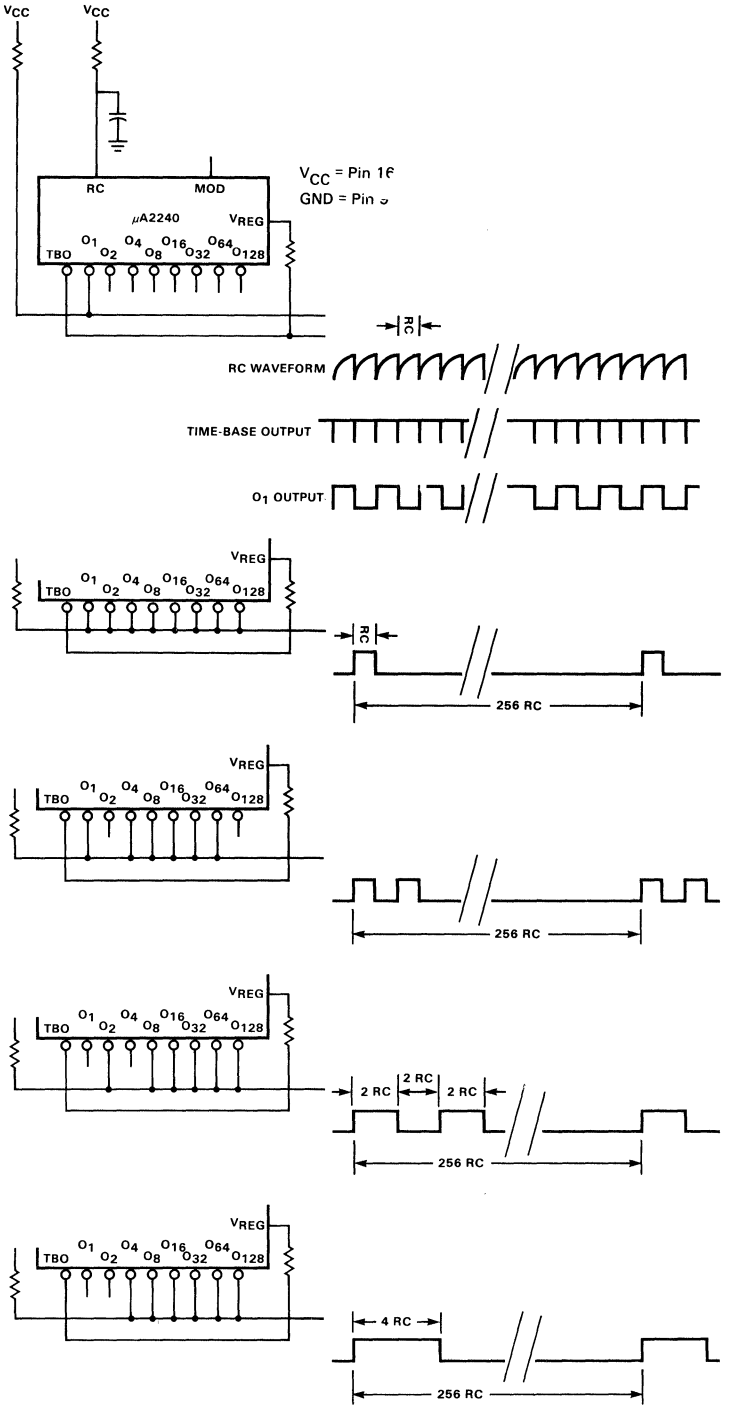


Fig. 11. Continuous Free-run Operation Examples of Output

of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

OPERATION WITH EXTERNAL CLOCK

The μA2240 can be operated with an external clock or time base by disabling the internal time-base oscillator and applying the external clock input to TBO, pin 14. The recommended circuit connection for this application is shown in *Figure 12*. The internal time base is de-activated by connecting a 1 kΩ resistor from RC, pin 13, to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 V is required. Minimum external clock pulse width must be ⩾ 1 μs.

For low power operation with supply voltages of 6 V or less, the internal time base section can be powered down by connecting V_{CC} to pin 15 and leaving pin 16 open. In this configuration, the internal time base does not draw any current and the overall current drain is reduced by ≈ 3 mA.

FREQUENCY SYNTHESIZER

The programmable counter section of the μA2240 can be used to generate 255 discrete frequencies from a given time-base output setting using the circuit connection of *Figure 13*. The circuit output is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) T where N is the programmed count in the counter. The modulus N is the total count corresponding to the counter outputs connected to the output bus. For example, if pins 1, 3 and 4 are connected together to the output bus, the total count is N = 1 + 4 + 8 = 13; and the period of the output waveform is equal to (N + 1) T or 14 T. In this manner, 255 different frequencies can be synthesized from a given time-base setting.

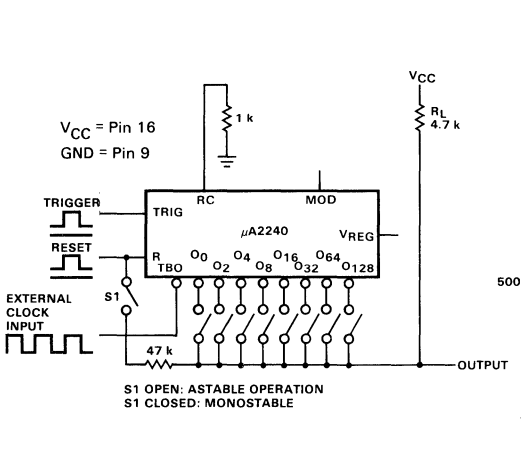


Fig. 12. Operation with External Clock

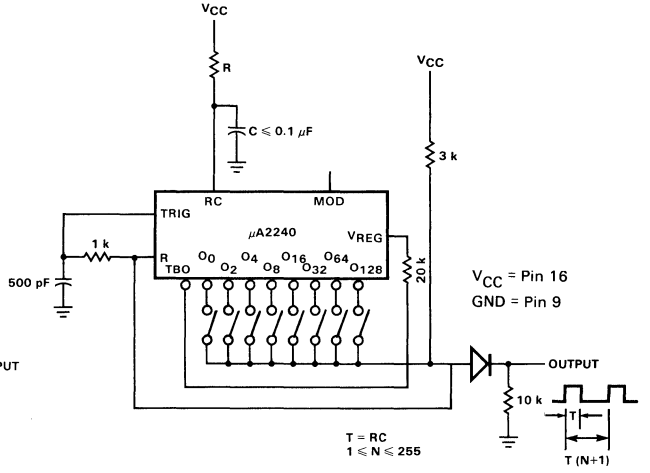


Fig. 13. Frequency Synthesis from Internal Time-Base

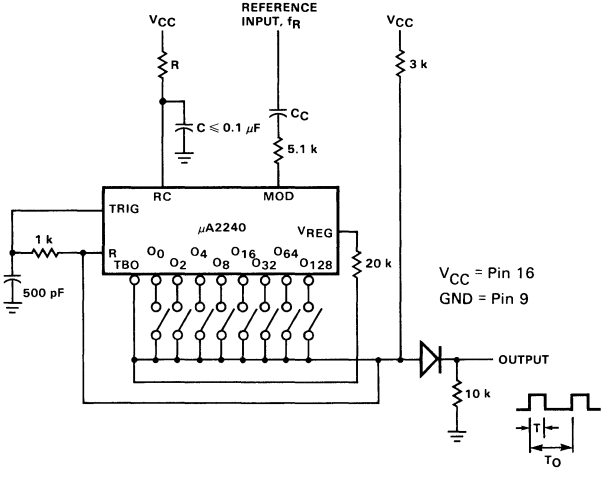


Fig. 14. Frequency Synthesis by Harmonic Locking to an External Reference

SYNTHESIS WITH HARMONIC LOCKING

The harmonic synchronization feature of the μA2240 time base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in *Figure 14* (see *Figures 4* and *5* for external sync waveform and harmonic capture range). If the time base is synchronized to (m)th harmonic of input frequency where $1 \leqslant m \leqslant 10$, the frequency f_O of the output waveform in *Figure 14* is related to the input reference frequency f_R as

$$f_O = f_R \frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leqslant N \leqslant 255$, the circuit of *Figure 14* can produce 2550 different frequencies from a single fixed reference.

The circuit of *Figure 14* can be used to generate frequencies which are not harmonically related to a reference input. For example, by selecting the external RC to set m = 10 and setting N = 5, a 100 Hz output frequency synchronized to 60 Hz power line frequency can be obtained.

STAIRCASE GENERATOR

The μA2240 timer/counter can be interconnected with an external operational amplifier and a precision resistor ladder to form a staircase generator as shown in *Figure 15*. Under Reset condition, the output is LOW. When a trigger is applied, the op amp output goes HIGH and generates a negative-going staircase of 256 equal steps. The time duration of each step is equal to the time-base period T. The staircase can be stopped at any level by applying a disable signal to pin 14, through a steering diode, as shown in *Figure 15*. The count is stopped when pin 14 is clamped at a voltage level ⩽ 1.0 V.

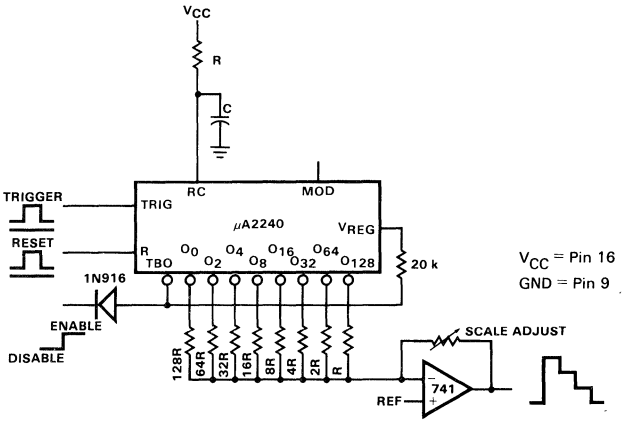


Fig. 15. Staircase Generator

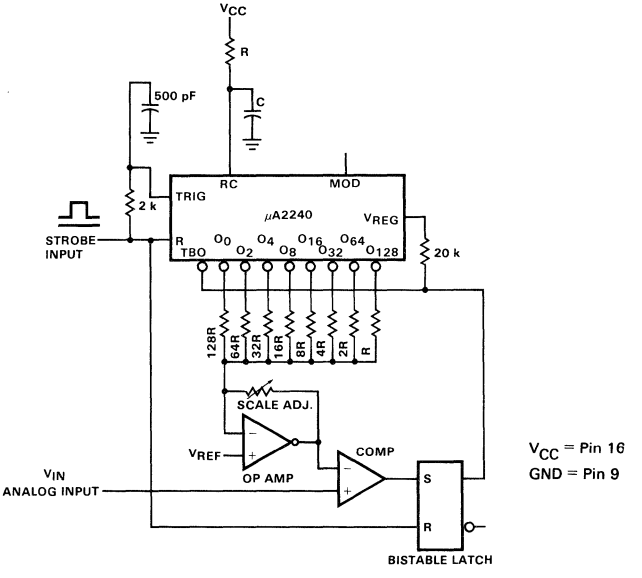


Fig. 16. Digital Sample and Hold Circuit

DIGITAL SAMPLE AND HOLD

Figure 16 shows a digital sample and hold circuit using the μA2240. Circuit operation is similar to the staircase generator described in the previous section. When a strobe input is applied, the RC low-pass network between the Reset and the Trigger inputs resets the timer, then triggers it. This strobe input also sets the output of the bistable latch to a HIGH state and activates the counter.

The circuit generates a staircase voltage at the op amp output. When the level of the staircase reaches that of the analog input to be sampled, the comparator changes state, activates the bistable latch and stops the count. At this point, the voltage level at the op amp output corresponds to the sampled analog input. Once the input is sampled, it is held until the next strobe signal. Minimum recycle time of the system is ≈ 6 ms.

ANALOG-TO-DIGITAL CONVERTER

Figure 17 shows a simple 8-bit A/D converter system using the μA2240. Circuit operation is very similar to that of the digital sample and hold system of *Figure 16*. In the case of A/D conversion, the digital output is obtained in parallel format from the binary-counter outputs with the output at pin 8 corresponding to the most significant bit (MSB). Recycle time is ≈ 6 ms.

DIGITAL TACHOMETER TIME BASE

A digital tachometer requires a time-base generator to supply two pulse outputs at specific intervals, *e.g.*, every second. The first pulse is a command (load) to transfer the accumulated counts in the counter section into latches (memory); the second resets the counter to zero. A simple adjustable time base, accurate to approximately ±0.5%, can be implemented using the circuit in *Figure 18*.

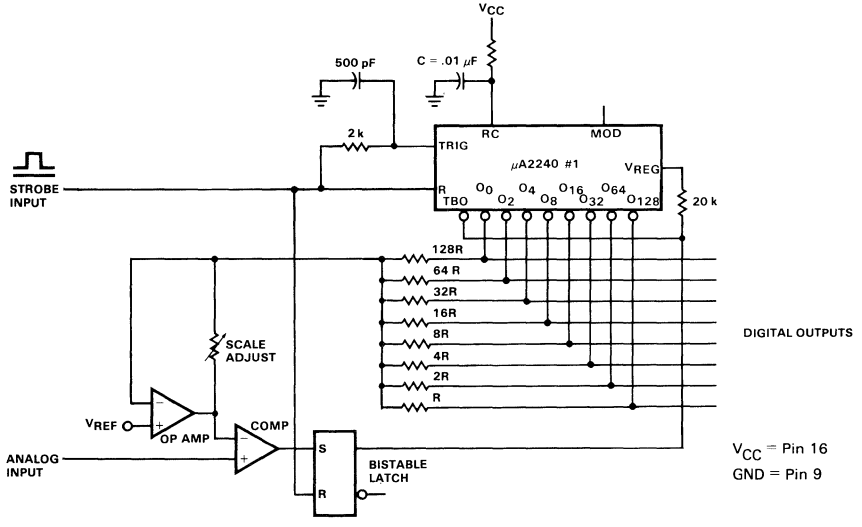


Fig. 17. Analog-to-Digital Converter

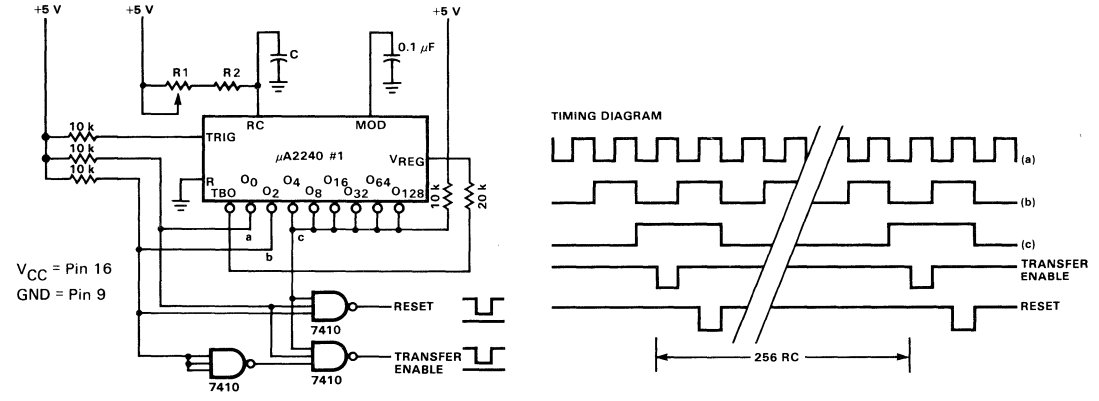


Fig. 18. Simple Time Generator for a Digital Tachometer

TYPICAL ELECTRICAL CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE IN RESET CONDITION

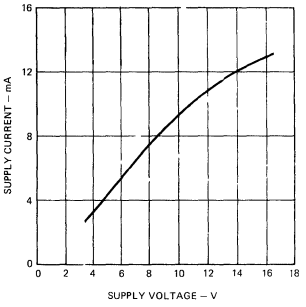


Fig. 19

RECOMMENDED RANGE OF TIMING COMPONENT VALUES

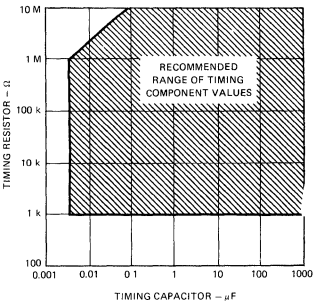


Fig. 20

TIME BASE PERIOD AS A FUNCTION OF EXTERNAL RC

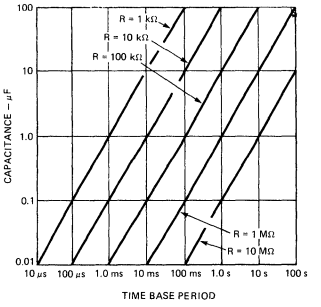


Fig. 21

MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AND RESET AMPLITUDE

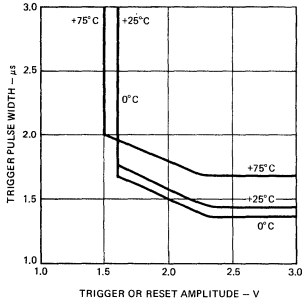


Fig. 22

TIME BASE PERIOD DRIFT AS A FUNCTION OF SUPPLY VOLTAGE

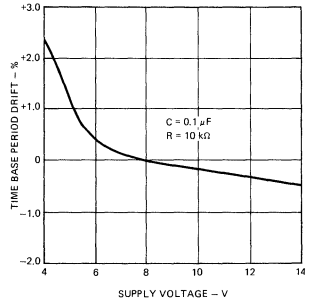


Fig. 23

MINIMUM TRIGGER/RETRIGGER TIMING AS A FUNCTION OF TIMING CAPACITOR

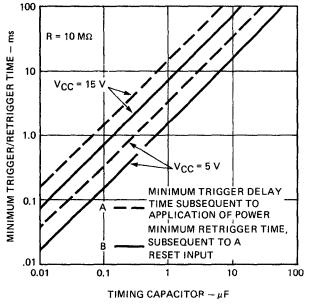


Fig. 24

NORMALIZED CHANGE IN TIME BASE PERIOD AS A FUNCTION OF MODULATION VOLTAGE

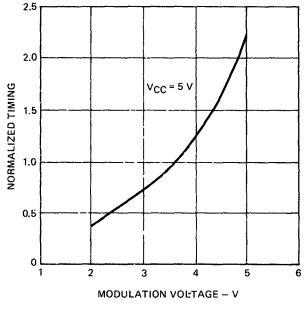


Fig. 25

TIME BASE PERIOD AS A FUNCTION OF TEMPERATURE

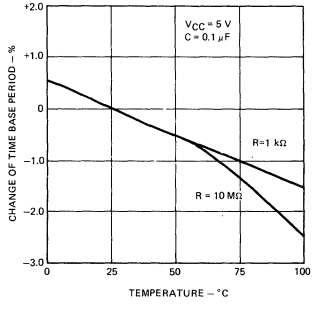


Fig. 26

TIME BASE PERIOD AS A FUNCTION OF TEMPERATURE

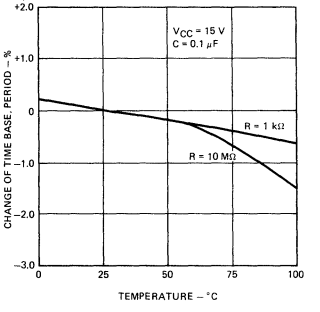


Fig. 27

TEST CIRCUITS

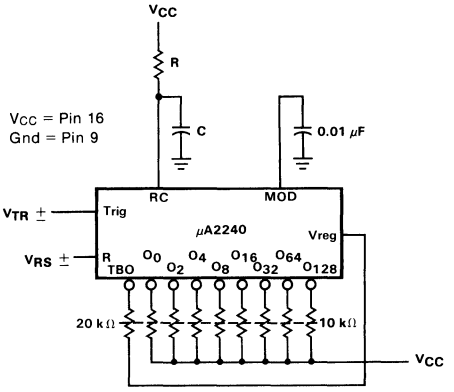


Fig. 28. Generalized Test Circuit

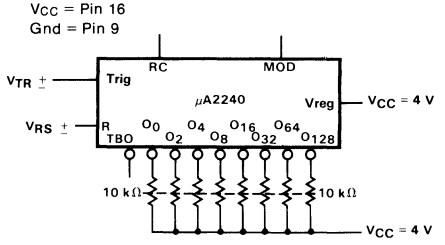


Fig. 29. Test Circuit for Low Power Operation (Time Base Powered Down)

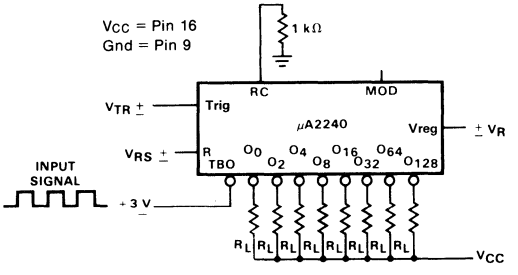


Fig. 30. Test Circuit for Counter Section

μA7391

DC MOTOR SPEED CONTROL CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

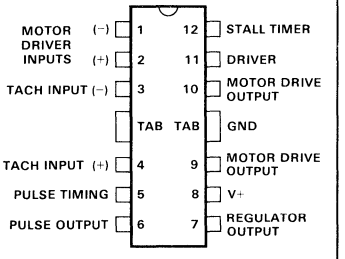
GENERAL DESCRIPTION – The μA7391 is designed for precision, closed-loop, motor speed control systems. It regulates the speed of capstan drive motors in automotive and portable tape players and is useful in a variety of industrial control applications, *e.g.,* floppy disc drive systems, data cartridge drive systems. The device is constructed using the Fairchild Planar* epitaxial process.

The μA7391 compares actual motor speed to an externally presettable reference voltage. The motor speed is determined by frequency to voltage conversion of the input signal provided by tachometer generator. The result of the comparison controls the duty cycle of the pulse width modulated switching motor drive output stage to close the system's negative feedback loop.

Thermal and over-voltage shutdown are included for self-protection, and a "stall-timer" feature allows the motor to be protected from burn-out during extended mechanical jams.

- **PRECISION PERFORMANCE – FREQUENCY-TO-VOLTAGE CONVERSION STABILITY TYPICALLY 0.1% FOR V+ FROM 10 V TO 16 V; 0.3% FOR CASE TEMPERATURE FROM −40°C TO +85°C**
- **HIGH CURRENT PERFORMANCE – 3.5 A STARTING SURGE CURRENT AND 2 A RUNNING CURRENT TO A DC MOTOR**
- **WIDE RANGE TACHOMETER INPUT – 100 mVp-p TO 1.0 Vp-p**
- **LOW EXTERNAL PARTS COUNT**
- **THERMAL SHUTDOWN, OVER-VOLTAGE AND STALL PROTECTION**
- **INTERNAL REGULATOR**
- **WIDE SUPPLY VOLTAGE RANGE – 6.3 V TO 16 V**

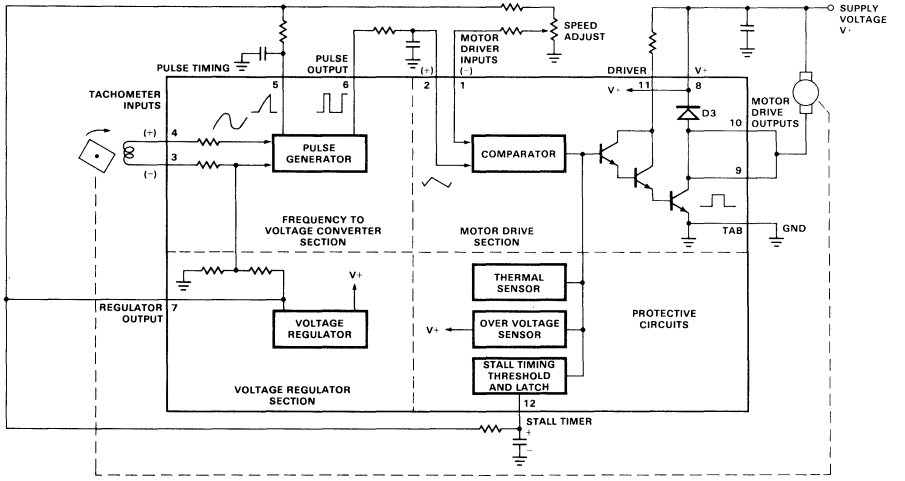
CONNECTION DIAGRAM
12-PIN POWER PACKAGE
(TOP VIEW)
PACKAGE OUTLINE 9W
PACKAGE CODE P6



ORDER INFORMATION

TYPE	PART NO.
μA7391	μA7391PC

BLOCK DIAGRAM



*Planar is a patented Fairchild process.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+), V_8	24 V
Regulator Output Current, I_7	15 mA
Voltage Applied to Pin 5 (Tachometer Pulse Timing)	7 V
Voltage Applied Between Pins 3 and 4 (Tachometer Inputs)	±6 V
DC Voltage Applied to Pin 11 (Driver)	24 V
DC Voltage Applied to Pins 9 or 10 (Motor Drive Output)	V+
Continuous Current through pins 9 and 10:	
Motor Drive Output ON	2.0 A
Repetitive Surge Current through Pins 9 and 10:	
Motor Drive Output ON	3.5 A
Motor Drive Output OFF	2.0 A
Repetitive Surge Current through Pin 11	300 mA
Power Dissipation	Internally Limited
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 s)	260°C

THERMAL DATA

θ_{JC}	Thermal Resistance Junction to Case (tab) (max)	12°C/W
θ_{JA}	Thermal Resistance Junction to Ambient (max)	**70°C/W

**Obtained with tabs soldered to a printed circuit board having a minimum area of copper surrounding the tabs.

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

VOLTAGE REGULATOR SECTION: (TEST CIRCUIT 1)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Current into Pins 9, 10 and 11		7.5	10	mA
Regulator Output Voltage		4.5	5.0	5.5	V
Regulator Output Line Regulation (ΔV_7)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_7)	I_7 from 10 mA to 0		40		mV

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

FREQUENCY TO VOLTAGE CONVERTER SECTION: (TEST CIRCUIT 2)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Tachometer (−) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_4 = V_3$		1.0	10	μA
Tachometer Input Positive Threshold	$(V_4 - V_3)$	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{p-p}
Pulse Timing ON Resistance	$V_5 = 1$ V		300	500	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_7$
Output Pulse Rise Time			0.3		μs
Output Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_6)			0.13	0.25	V
Pulse Output HIGH Saturation ($V_7 - V_6$)			0.12	0.2	V
Pulse Output HIGH Source Current	$V_6 = 1$ V	−340	−260	−180	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	$V_{FV} = 0.25\ V_7$ (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	$V_{FV} = 0.25\ V_7$ (Note 2) T_A from −40°C to +85°C		0.3		%

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ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

MOTOR DRIVE SECTION: (TEST CIRCUIT 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				±20	mV
Input Bias Current			0.1	10	μA
Common Mode Range		0.8		2.5	V
Driver Saturation	$I_9 + I_{10} = 2$ A, $I_{11} = 175$ mA		1.9	2.5	V
Driver Leakage Current	$V_{11} = 16$ V			5.0	μA
Motor Drive Output Saturation	$I_9 + I_{10} = 2$ A, $I_{11} = 55$ mA		0.6	1.1	V
Motor Drive Output Leakage	$V_8 = V_9 = V_{10} = 16$ V			100	μA
Flyback Diode Leakage	$V_9 = V_{10} = 1$ V			30	μA
Flyback Diode Clamp	$I_9 + I_{10} = 2$ A Motor Drive Output Off		1.6	2.5	V

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, TA = 25°C, unless otherwise noted

PROTECTIVE CIRCUITS: (TEST CIRCUIT 4)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	2.5	2.9	3.5	V
Stall Timer Threshold Current	Note 5		0.3	3.0	μA

NOTES:

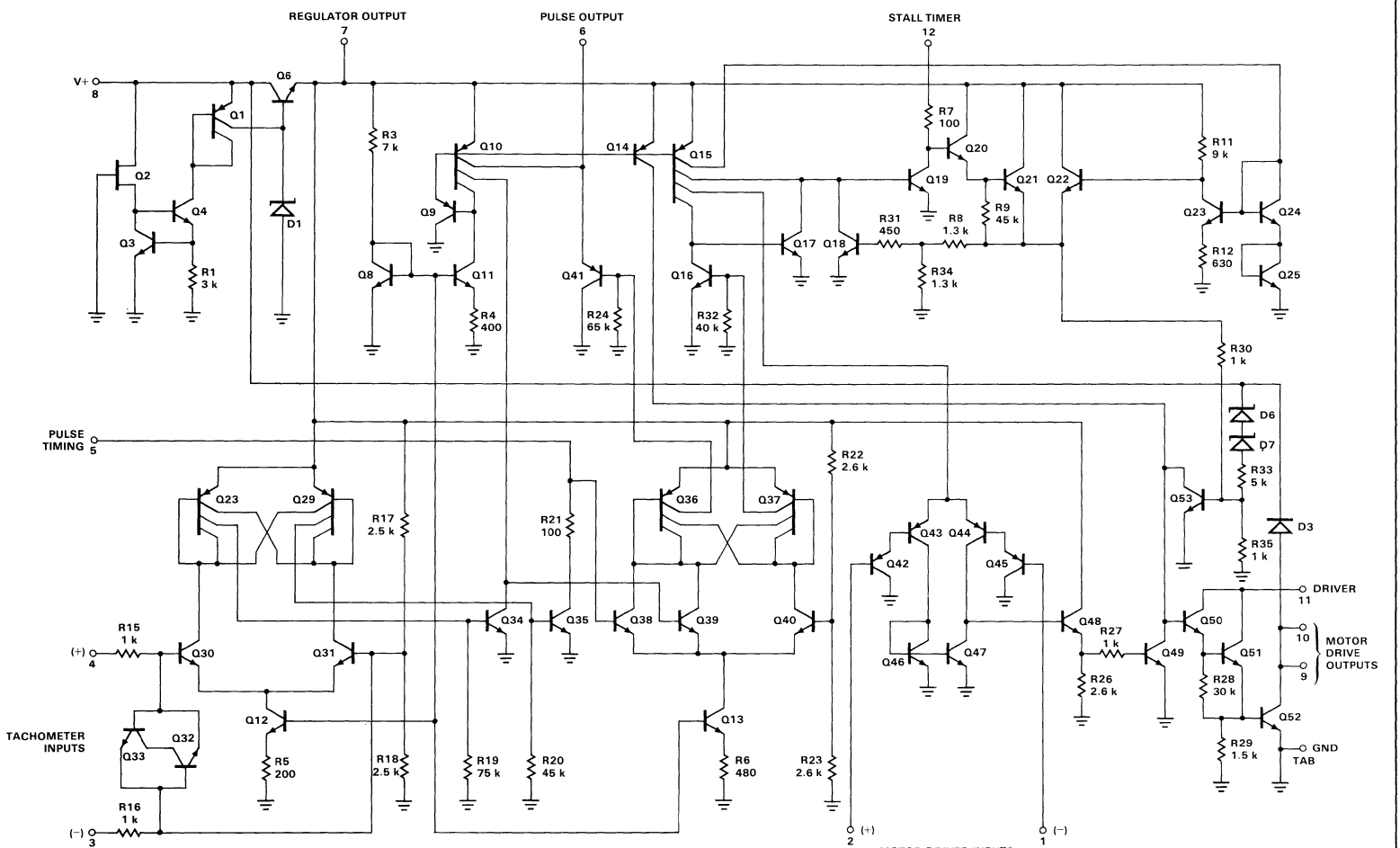
1. Frequency-to-Voltage Conversion, Supply Voltage Stability is defined as:

$$\left[\frac{V_{FV(16\ V)}}{V_{7(16\ V)}}\right] - \left[\frac{V_{FV(10\ V)}}{V_{7(10\ V)}}\right] \div \left[\frac{V_{FV(14.5\ V)}}{V_{7(14.5\ V)}}\right] \times 100\%$$

2. V_{FV} is the integrated dc output voltage from the pulse generator (Pin 6)
3. Frequency-to-Voltage Conversion Temperature Stability is defined as:

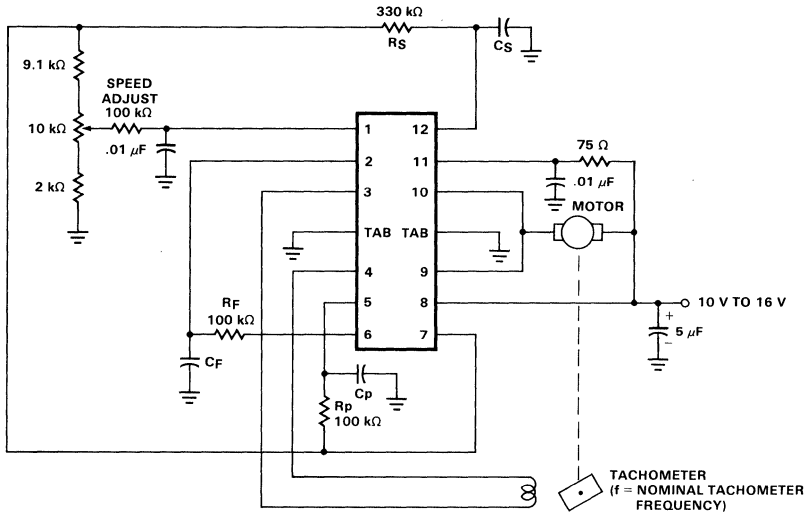
$$\left[\frac{V_{FV(85°C)}}{V_{7(85°C)}}\right] - \left[\frac{V_{FV(-40°C)}}{V_{7(-40°C)}}\right] \div \left[\frac{V_{FV(25°C)}}{V_{7(25°C)}}\right] \times 100\%$$

4. "Driver" and "Motor Drive" circuitry is disabled when these limits are exceeded. If the condition continues for the duration set by the external stall timer components, the circuit is latched off until reset by temporarily opening the power supply input line.
5. If stall timer protection is not required, Pin 12 should be grounded.



EQUIVALENT CIRCUIT

TYPICAL APPLICATION USING MAGNETIC TACHOMETER



TYPICAL COMPONENT VALUES:

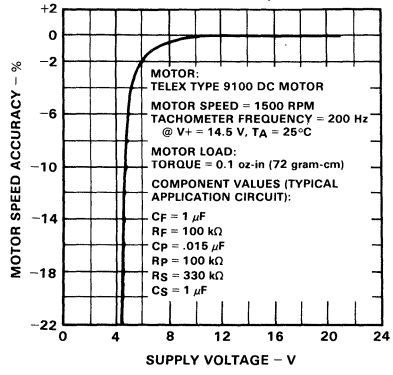
$$Cp = \frac{1}{4\ Rpf}$$

C_F = 10 Cp to 1000 Cp depending on system requirements

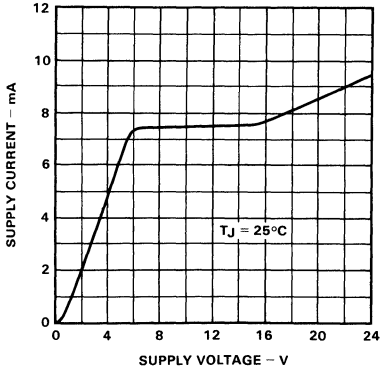
$$CS = \frac{2 \times \text{stall time-out}}{RS}$$

$R_{Motor} \geqslant 5\ \Omega$

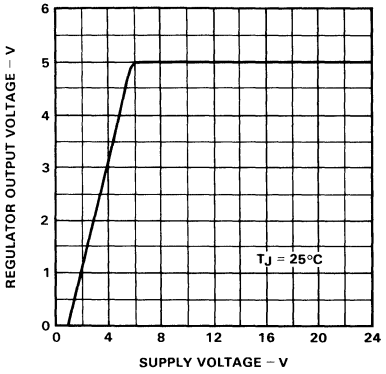
MOTOR SPEED ACCURACY AS A FUNCTION OF SUPPLY VOLTAGE (REFER TO APPLICATION SCHEMATIC)



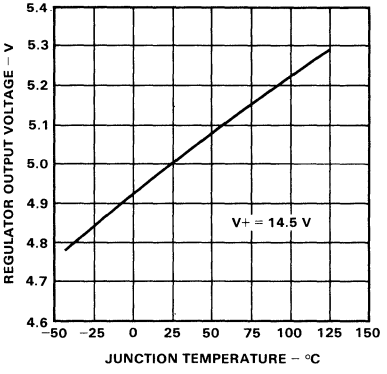
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



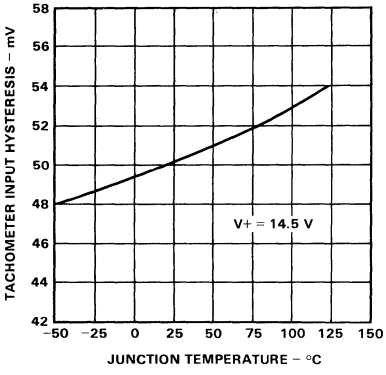
REGULATOR OUTPUT VOLTAGE AS A FUCTION OF SUPPLY VOLTAGE



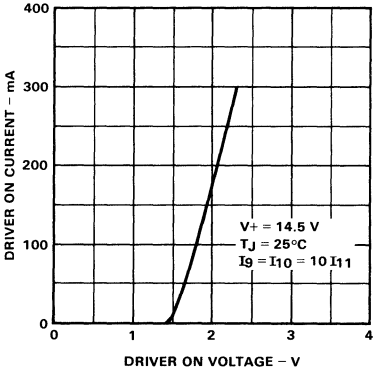
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



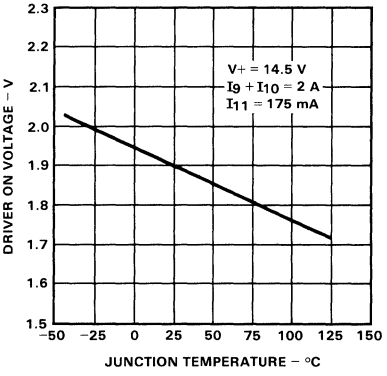
TACHOMETER INPUT HYSTERESIS AS A FUNCTION OF JUNCTION TEMPERATURE



DRIVER ON CURRENT AS A FUNCTION OF DRIVER ON VOLTAGE



DRIVER ON VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



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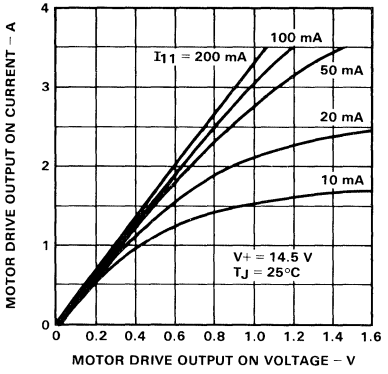
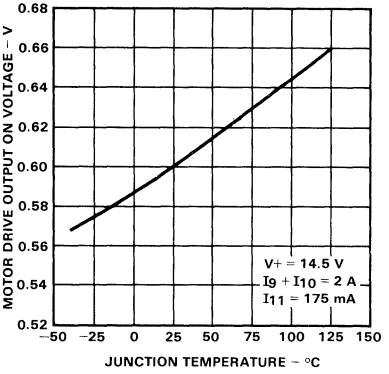
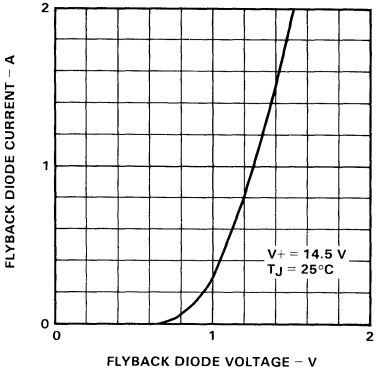
MOTOR DRIVE OUTPUT ON CURRENT AS A FUNCTION OF MOTOR DRIVE OUTPUT ON VOLTAGE



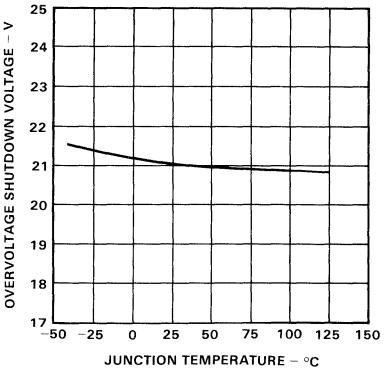
MOTOR DRIVE OUTPUT ON VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



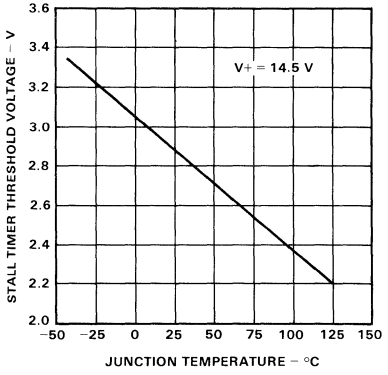
FLYBACK DIODE (D3) CURRENT AS A FUNCTION OF FLYBACK DIODE VOLTAGE



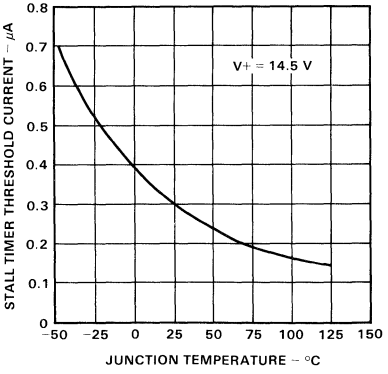
OVERVOLTAGE SHUTDOWN VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



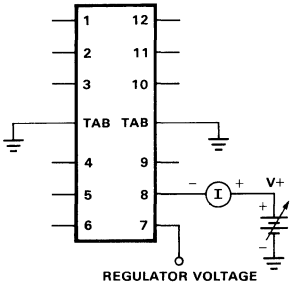
STALL TIMER THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



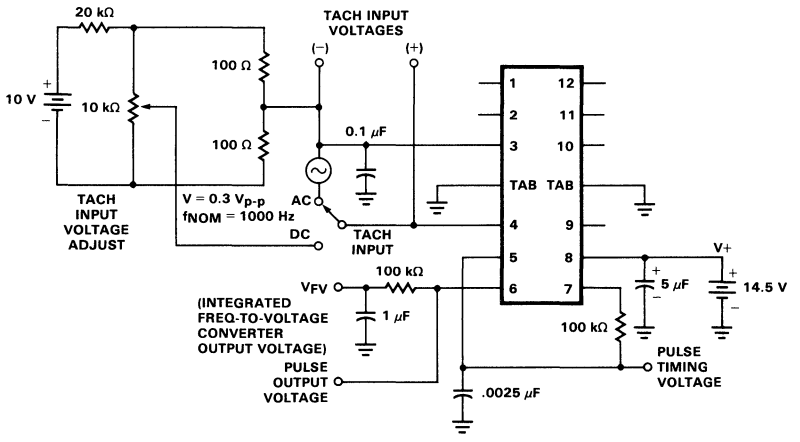
STALL TIMER THRESHOLD CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE



TEST CIRCUIT 1



TEST CIRCUIT 2



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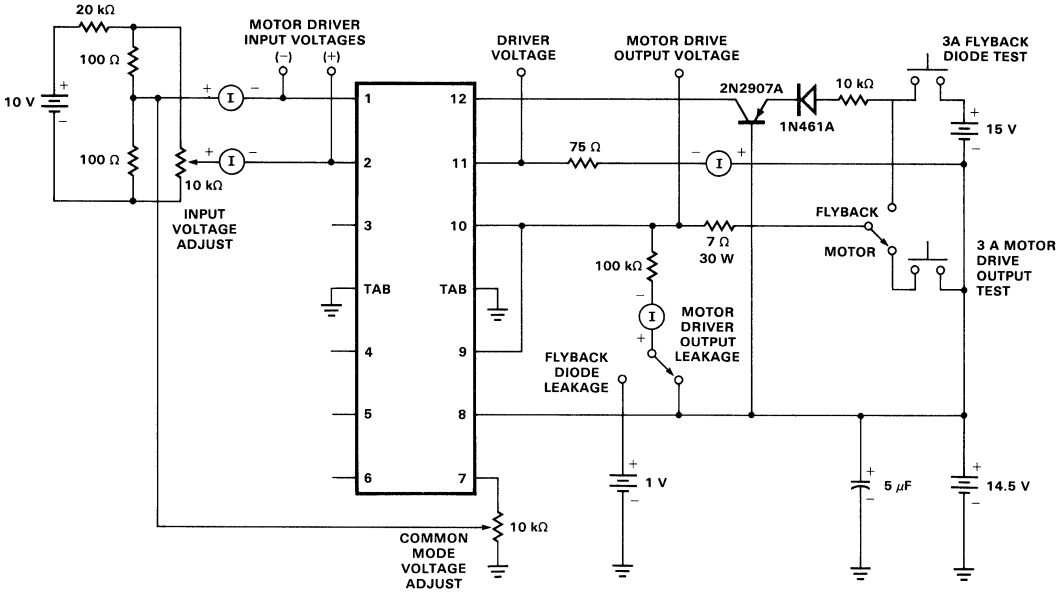
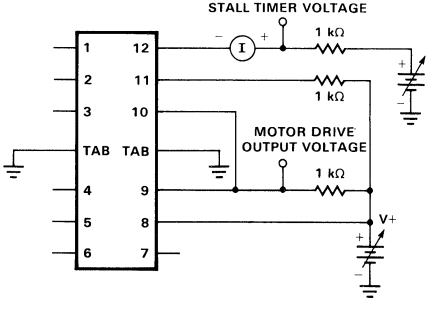
TEST CIRCUIT 3



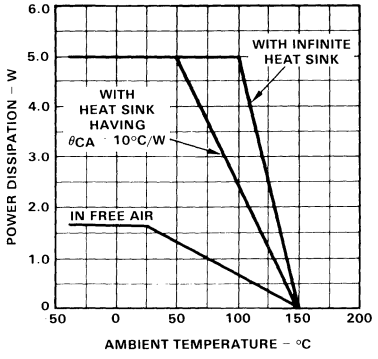
TEST CIRCUIT 4



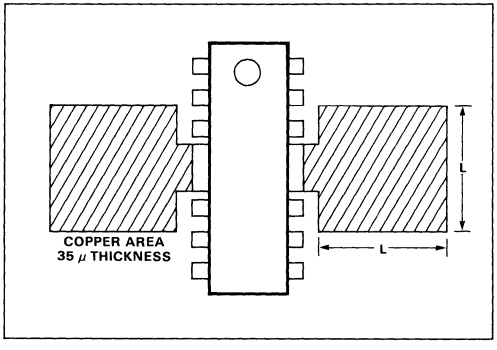
MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by soldering the tabs to an area of copper on the printed circuit board. During soldering the tabs temperature must not exceed 260°C and the soldering temperature time must not be longer than 10 seconds.

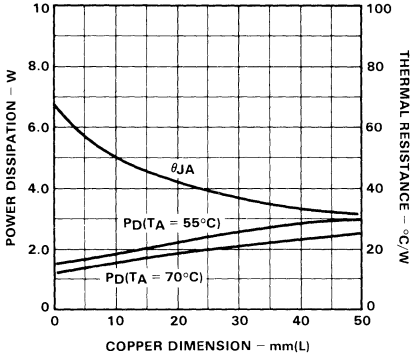
MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



PC BOARD



MAXIMUM POWER DISSIPATION AND TOTAL THERMAL RESISTANCE AS A FUNCTION OF COPPER AREA OF PC BOARD



μA7392

DC MOTOR SPEED CONTROL CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION—The μA7392 is designed for precision, closed-loop, motor speed control systems. It regulates the speed of capstan drive motors in automotive and portable tape players and is useful in a variety of industrial and military control applications, e.g., floppy disc drive systems and data cartridge drive systems. The device is constructed using the Fairchild Planar* epitaxial process.

The μA7392 compares actual motor speed to an externally presettable reference voltage. The motor speed is determined by frequency to voltage conversion of the input signal provided by the tachometer generator. The result of the comparison controls the duty cycle of the pulse width modulated switching motor drive output stage to close the system's negative feedback loop.

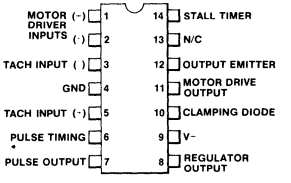
Thermal and over-voltage shutdown are included for self-protection, and a "stall-timer" feature allows the motor to be protected from burn-out during extended mechanical jams.

The μA7392 is a low current compliment to the μA7391 for those applications requiring less current and also to drive high current output stages for very high current applications.

- **PRECISION PERFORMANCE—FREQUENCY-TO-VOLTAGE CONVERSION STABILITY TYPICALLY 0.1% FOR V+ FROM 10 V TO 16 V; 0.3% FOR CASE TEMPERATURE FROM -40°C TO +85°C**
- **HIGH CURRENT PERFORMANCE—1.0 A STARTING SURGE CURRENT AND 300 mA RUNNING CURRENT TO A DC MOTOR**
- **WIDE RANGE TACHOMETER INPUT—100 mVp-p TO 1.0 Vp-p**
- **LOW EXTERNAL PARTS COUNT**
- **THERMAL SHUTDOWN, OVER-VOLTAGE AND STALL PROTECTION**
- **INTERNAL REGULATOR**
- **WIDE SUPPLY VOLTAGE RANGE—6.3 V TO 16 V**
- **EMITTER OF OUTPUT STAGE AVAILABLE FOR EASE IN DRIVING POWER TRANSISTOR OUTPUT STAGES**
- **CLAMPING DIODE AVAILABLE ON SEPARATE PIN**

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 6A, 9A
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA7392	μA7392DM
μA7392C	μA7392DC
μA7392C	μA7392PC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+), V_9, V_{10}, V_{11}	24 V
Regulator Output Current, I_8	15 mA
Voltage Applied to Pin 6 (Tachometer Pulse Timing)	7 V
Voltage Applied Between Pins 3 and 5 (Tachometer Inputs)	±6 V
Continuous Current through Pins 11 and 12 Motor Drive Output ON	0.3 A
Repetitive Surge Current through Pins 11 and 12 (Motor Drive ON)	1.0 A
Repetitive Surge Current through Pins 10 and 11 (Motor Drive OFF)	0.3 A
Power Dissipation	Internally Limited
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range (μA7392)	-55°C to +125°C
Operating Temperature Range (μA7392C)	-40°C to +85°C
Pin Temperature (Soldering 10 s)	260°C

*Planar is a patented Fairchild process

μA7392 and μA7392C

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C, unless otherwise noted

VOLTAGE REGULATOR SECTION: (TEST CIRCUIT 1)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Current into Pin 11		7.5	10	mA
Regulator Output Voltage		4.5	5.0	5.5	V
Regulator Output Line Regulation (ΔV_8)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_8)	I_8 from 10 mA to 0		40		mV

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C, unless otherwise noted

FREQUENCY TO VOLTAGE CONVERTER SECTION: (TEST CIRCUIT 2)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Tachometer (-) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_5 = V_3$		1.0	10	μA
Tachometer input Positive Threshold	($V_5 - V_3$)	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{pk-pk}
Pulse Timing ON Resistance	V_6 = 1 V		300	500	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_8$
Output Pulse Rise Time			0.3		μs
Output Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_7)			0.13	0.25	V
Pulse Output HIGH Saturation ($V_8 - V_7$)			0.12	0.2	V
Pulse Output HIGH Source Current	V_7 = 1 V	-340	-260	-180	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	$V_{FV} = 0.25\ V_8$ (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	$V_{FV} = 0.25\ V_8$ (Note 2) T_A from -40°C to +85°C		0.3		%

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C, unless otherwise noted

MOTOR DRIVE SECTION: (TEST CIRCUIT 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				±20	mV
Input Bias Current			0.1	10	μA
Common Mode Range		0.8		2.5	V
Motor Drive Output Saturation	I_{11} = 300mA		1.3	1.6	V
Motor Drive Output Leakage	$V_{11} = V_{10}$ = 16 V			5	μA
Flyback Diode Leakage	V_{10} = 16 V, V_{11} = 0 V			30	μA
Flyback Diode Clamp Voltage	I_{11} = 300mA Motor Drive Output Off		1.1	1.3	V

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μA7392, μA7392C

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, T_A = 25°C unless otherwise noted

PROTECTIVE CIRCUITS: (TEST CIRCUIT 4)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	2.5	2.9	3.5	V
Stall Timer Threshold Current	Note 5		0.3	3.0	μA

μA7392 ONLY

ELECTRICAL CHARACTERISTICS: V+ = 14.5 V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted

VOLTAGE REGULATOR SECTION: (TEST CIRCUIT 1)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Current into Pin 11		7.5	12	mA
Regulator Output Voltage		4.5	5.0	6.0	V
Regulator Output Line Regulation (ΔV_8)	V+ from 10 V to 16 V V+ from 6.3 V to 16 V		6.0 12	20 50	mV mV
Regulator Output Load Regulation (ΔV_8)	I_8 from 10 mA to 0		40	100	mV

FREQUENCY TO VOLTAGE CONVERTER SECTION: (TEST CIRCUIT 2)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Tachometer (−) Input Bias Voltage			2.4		V
Tachometer (+) Input Bias Current	$V_5 = V_3$		1.0	15	μA
Tachometer Input Positive Threshold	($V_5 - V_3$)	10	25	50	mV_{pk}
Tachometer Input Hysteresis		20	50	100	mV_{p-p}
Pulse Timing ON Resistance	V_6 = 1 V		300	670	Ω
Pulse Timing Switch Threshold		45	50	55	$\%V_8$
Output Pulse Rise Time			0.3		μs
Pulse Fall Time			0.1		μs
Pulse Output LOW Saturation (V_7)			0.13	0.25	V
Pulse Output HIGH Saturation ($V_8 - V_7$)			0.12	0.2	V
Pulse Output HIGH Source Current	V_7 = 1 V	−370	−260	−150	μA
Frequency-to-Voltage Conversion Supply Voltage Stability (Note 1)	F_{FV} = 0.25 V_8 (Note 2) V+ from 10 V to 16 V		0.1		%
Frequency-to-Voltage Conversion Temperature Stability (Note 3)	V_{FV} = 0.25 V_8 (Note 2) T_A from −40°C to +85°C		0.3		%

μA7392 ONLY

ELECTRICAL CHARACTERISTICS Cont. : V+ = 14.5 V, -55°C ≥ TA ≤ +125°C, unless otherwise noted.

MOTOR DRIVE SECTION: (TEST CIRCUIT 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage				±30	mV
Input Bias Current			0.1	10	μA
Common Mode Range		0.8		2.5	V
Motor Drive Output Saturation	I_{11} = 300mA		1.3	1.6	V
Motor Drive Output Leakage	$V_{11} = V_{10}$ = 16 V			10	μA
Flyback Diode Leakage	V_{10} = 16 V, V_{11} = 0 V			30	μA
Flyback Diode Clamp Voltage	I_{11} = 300mA Motor Drive Output Off		1.1	1.3	V

PROTECTIVE CIRCUITS: (TEST CIRCUIT 4)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Junction Temperature	Note 4		160		°C
Overvoltage Shutdown	Note 4	18	21	24	V
Stall Timer Threshold Voltage	Note 5	1.8	2.9	4.0	V
Stall Timer Threshold Current	Note 5		0.3	4.0	μA

NOTES:

1. Frequency-to-Voltage Conversion, Supply Voltage Stability is defined as:

$$\left[\frac{V_{FV}(16\ V)}{V_8(16\ V)}\right] - \left[\frac{V_{FV}(10\ V)}{V_8(10\ V)}\right] \div \left[\frac{V_{FV}(14.5\ V)}{V_8(14.5\ V)}\right] \times 100\%$$

2. V_{FV} is the integrated dc output voltage from the pulse generator (Pin 7)
3. Frequency-to-Voltage Conversion Temperature Stability is defined as:

$$\left[\frac{V_{FV}(85°C)}{V_8(85°\ C)}\right] - \left[\frac{V_{FV}(-40°\ C)}{V_8(-40°\ C)}\right] \div \left[\frac{V_{FV}(25°\ C)}{V_8(25°\ C)}\right] \times 100\%$$

4. "Motor Drive" circuitry is disabled when these limits are exceeded. If the condition continues for the duration set by the external stall timer components, the circuit is latched off until reset by temporarily opening the power supply input line.
5. If stall timer protection is not required, Pin 14 should be grounded.

THERMAL DATA

	TYP	MAX	
θ_{JA} THERMAL RESISTANCE, JUNCTION TO AMBIENT			
PLASTIC (9A)	70	80	°C/W
CERAMIC (6A)	100	120	°C/W

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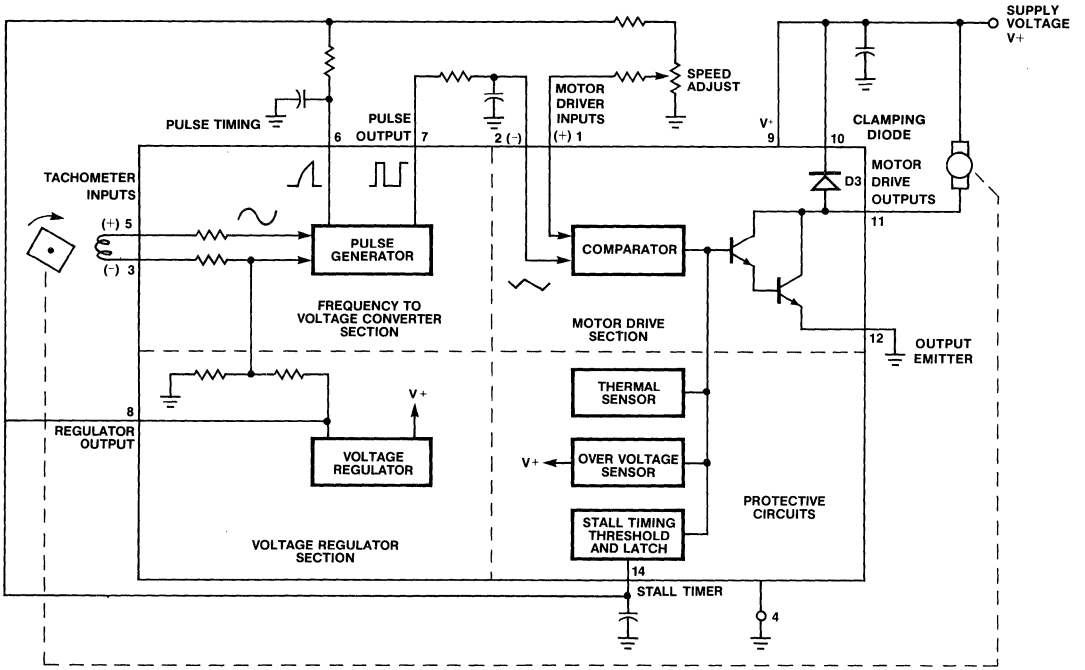
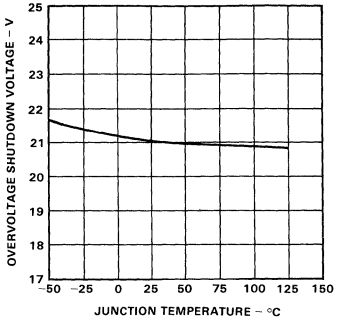
BLOCK DIAGRAM

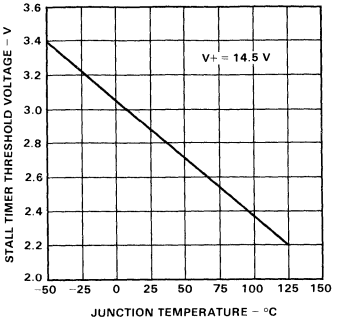


TYPICAL PERFORMANCE CURVES

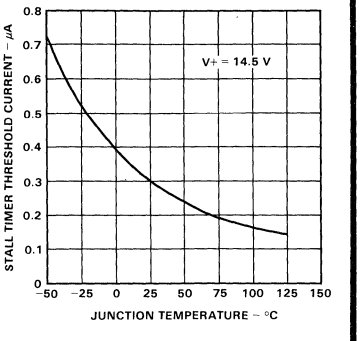
OVERVOLTAGE SHUTDOWN VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



STALL TIMER THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

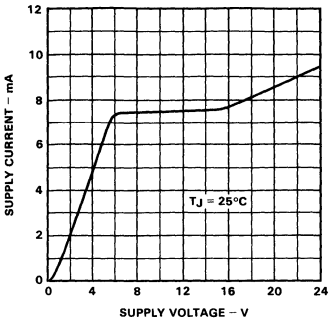


STALL TIMER THRESHOLD CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

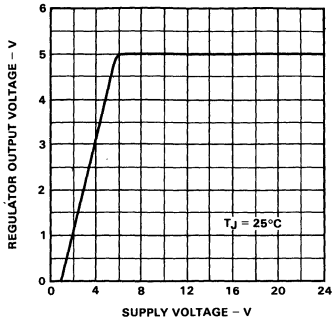


TYPICAL PERFORMANCE CURVES (Cont'd.)

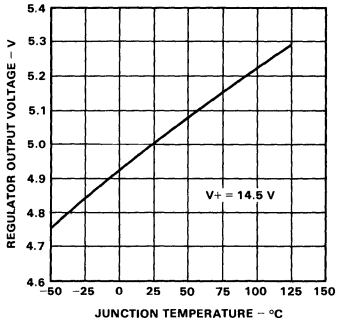
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



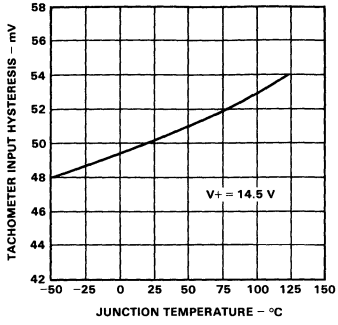
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



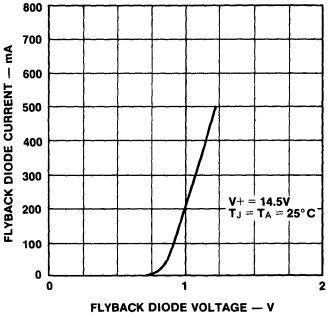
REGULATOR OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



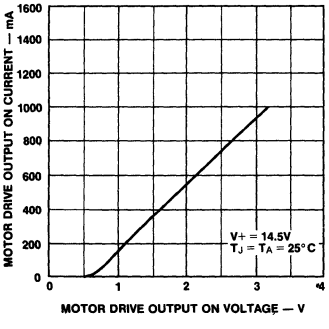
TACHOMETER INPUT HYSTERESIS AS A FUNCTION OF JUNCTION TEMPERATURE



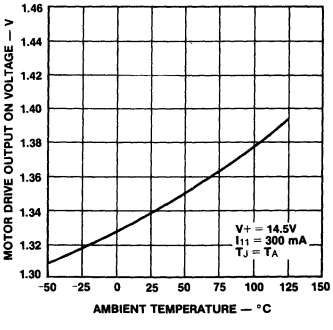
FLYBACK DIODE (D3) CURRENT AS A FUNCTION OF FLYBACK DIODE VOLTAGE



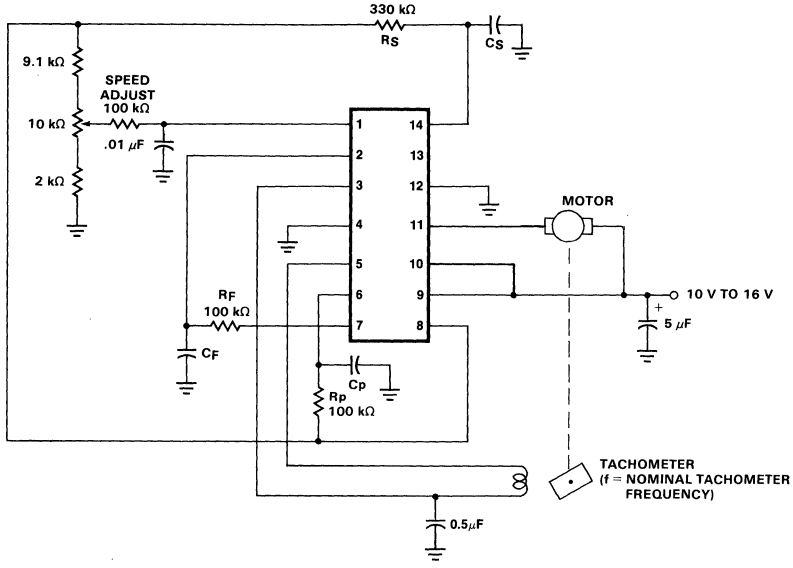
MOTOR DRIVE OUTPUT ON CURRENT AS A FUNCTION OF MOTOR DRIVE OUTPUT ON VOLTAGE



MOTOR DRIVE OUTPUT ON VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL APPLICATION USING MAGNETIC TACHOMETER



TYPICAL COMPONENT VALUES:

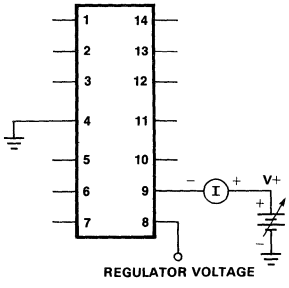
$Cp = \frac{}{4\ Rpf}$

Cf = 10 Cp to 1000 Cp depending on system requirements

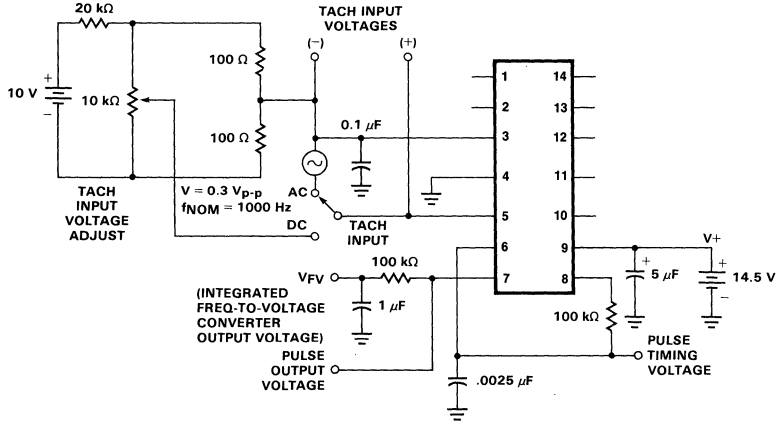
$C_S = \frac{2 \times \text{stall time-out}}{RS}$

$R_{Motor} \geq 5\ \Omega$

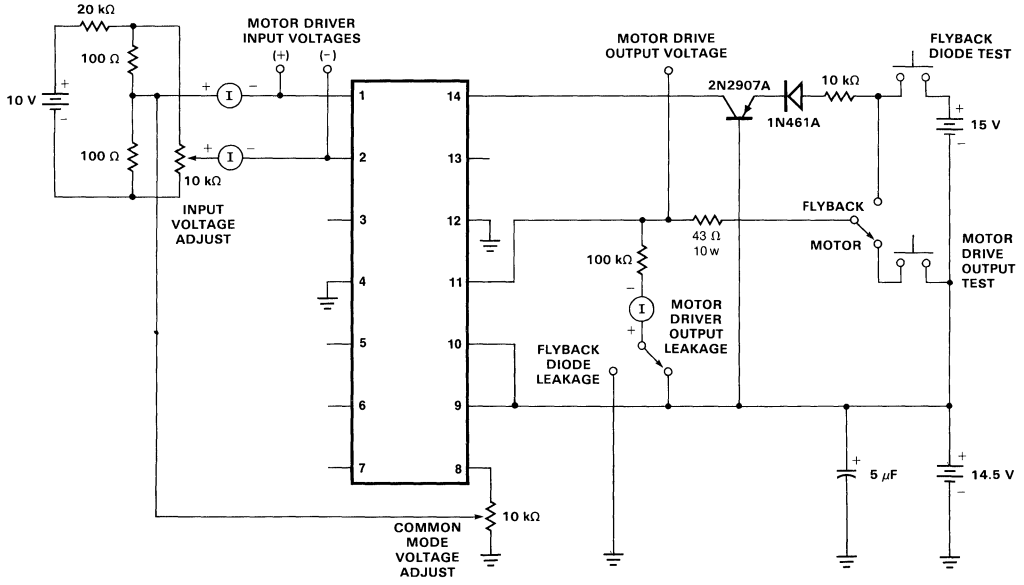
TEST CIRCUIT 1



TEST CIRCUIT 2



TEST CIRCUIT 3



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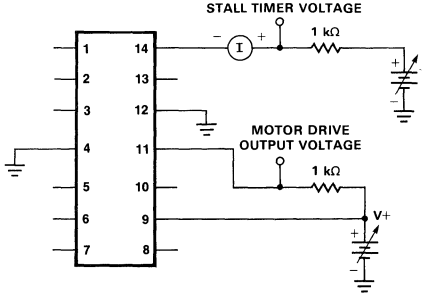
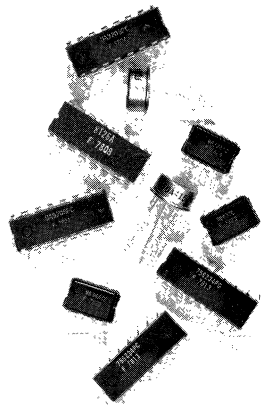
TEST CIRCUIT 4





DATA TRANSMISSION INFORMATION

INTRODUCTION

Digital signals transmitted any distance, only a few inches in some cases or up to several miles, must enter the analog world of transmission lines before arriving at their digitial destinations. Therefore, special attention should be given to the interface between the digital and analog areas — often one of the least understood considerations in a system design. Interface problems occur every time a digital signal is sent from a printed circuit board and, indeed, transmission line theory must often be considered when connecting devices on the same board when using very high-speed logic such as ECL or Schottky TTL. This section is intended to shed some light on this important design procedure — interfacing of systems (or subsystems) for the transmission of information from one location to another via line drivers, transmission lines and line receivers.

To design a data transmission interface, the systems designer must be familiar with several subjects. He needs a good understanding of the effects of pulse excitation on transmission lines, knowledge about the various fundamental forms and modes of data-transmission-line circuit operation, and familiarity with the problems encountered when operating with long transmission lines. He must also have a good working knowledge of line drivers and line receivers, their electrical characteristics, and how and where these devices should be used.

This section is not intended to be a textbook in the formal sense, nor is it a 'cookbook' of applications since each system must be designed based on its unique requirements. It is presented as a refresher on the basics of pulse transmission line theory combined with methods for determining signal quality and feasibility of the particular data transmission system. Only those areas that directly affect the transmission of digital signals are covered. This section contains the essential elements to aid the system designer in making an informed decision regarding the quality of data received at the end of a transmission line.

Section two discusses the general characteristics of transmission lines and their derivations. Here, using a transmission line model, the important parameters of characteristic impedance and propagation delay are developed in terms of their physical and electrical parameters.

The third section explores another important characteristic — reflection coefficient. This concept is combined with the material in section two to present graphical and analytical methods for determining the voltages and currents at any point on a line with respect to distance and time after signal application. The effects of various source resistances and line termination methods on the transmitted signal are discussed.

In section four, the logical progression from the ideal transmission line to the real world of the long transmission line with its attendant losses and problems is made; specifically, the methods to determine the practicality of a certain length of line at a given data rate is discussed. Transmission line effects on various data formats are examined as well as the effects of several types of sources (drivers) on signal quality. A practical means is given to measure signal quality for a given transmission line using readily available test equipment. This, in turn, leads to a chart that provides the designer a way to predict the feasibility of a proposed data-transmission circuit when twisted-pair cable is used. A method to estimate signal quality on coaxial-cable interconnections is also discussed.

Section five describes the various combinations of forms and modes of operation in data-transmission systems. Also described are the circuits that conform to industry standards — EIA RS232C, MIL STD 188C and IBM 360/370 I/O interfaces. A selection guide for available line drivers and receivers integrated circuits and some helpful suggestions for incorporating them into a system complete the section.

In section six, new EIA standards of RS-422 and RS-423 specifications are discussed.

Section 2
DATA TRANSMISSION LINES AND THEIR CHARACTERISTICS

INTRODUCTION
A data transmission line is composed of two or more conductors transmitting electrical signals from one location to another. A parallel transmission line is shown in *Figure 2-1.* To show how the signals (voltages and currents) on the line relate to as yet undefined parameters, a transmission line model is needed.

TRANSMISSION LINE MODEL
Because the wires A and B could not be ideal conductors, they therefore must have some finite resistance. This resistance/conductivity is determined by length and cross-sectional area. Any line model, then, should possess some series resistance representing the finite conductivity of the wires. It is convenient to establish this resistance as a per-unit-length parameter.

Similarly, the insulating medium separating the two conductors could not be a perfect insulator because some small leakage current is always present. These currents and dielectric losses can be represented as a shunt conductance per unit length of line. To facilitate development of later equations, conductance is the chosen term instead of resistance.

If the voltage between conductors A and B *is not variable* with time, any voltage present indicates a static electric field between the conductors. From electrostatic theory it is known that the voltage V produced by a static electric field E is given by

$$V = \int E \cdot dl \qquad (2.1)$$

This static electric field between the wires can only exist if there are free charges of equal and opposite polarity on both wires as described by Coulomb's law.

$$E = \frac{q}{4\pi\epsilon r^2} \qquad (2.2)$$

where E is the electric field in volts per meter, q is the charge in Coulombs, ϵ is the dielectric constant, and r is the distance in meters. These free charges, accompanied by a voltage, represent a capacitance (C = q/V); so the line model must include a shunt capacitive component. Since total capacitance is dependent upon line length, it should be expressed in a capacitance per-unit-length value.

It is known that a current flow in the conductors induces a magnetic field or flux. This is determined by either Ampere's law

$$\oint H \cdot dl = I \qquad (2.3)$$

or the Biot-Savart law

$$dB = \frac{\mu I dl \times r}{4\pi r^3} \qquad (2.4)$$

where r = radius vector (meters)
l = length vector (meters)
I = current (amps)
B = magnetic flux density (Webers per meter)
H = magnetic field (amps per meter)
μ = permeability

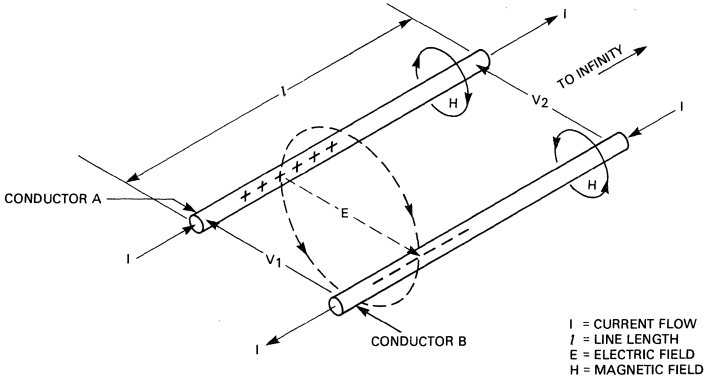


Fig. 2-1. Infinite Length Parallel Wire Transmission Line

If the magnetic flux (ϕ) linking the two wires *is variable* with time, then according to Faraday's law

$$V = \frac{d\phi}{dt} \tag{2.5}$$

A small line section can exhibit a voltage drop — in addition to a resistive drop—due to the changing magnetic flux (ϕ) within the section loop. This voltage drop is the result of an inductance given as

$$V = L\frac{di}{dt} \tag{2.6}$$

Therefore, the line model should include a series inductance per-unit-length term. In summary, it is determined that the model of a transmission line section can be represented by two series terms of resistance and inductance and two shunt terms of capacitance and conductance.

From a circuit analysis point of view, the terms can be considered in any order, since an *equivalent* circuit is being generated. *Figure 2-2* shows three possible arrangements of circuit elements.

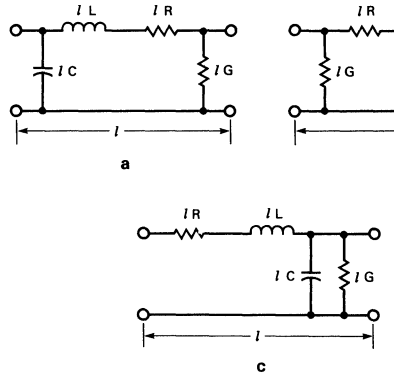


Fig. 2-2. Circuit Elements

For consistency, the circuit shown in *Figure 2-2c* will be used throughout the remainder of this chapter. *Figure 2-3* shows how a transmission line model is constructed by series connecting the short sections into a ladder network.

Before examining the pertinent properties of the model, some comments are necessary on applicability and limitations. A *real* transmission line does not consist of an infinite number of small lumped sections — rather, it is a distributed network. For the lumped model to accurately represent the transmission line, (see *Figure 2-3*) the section length must be quite small in comparison with the shortest wavelengths (highest frequencies) to be used in analysis of the model. Within these limits, as differentials are taken, the section length will approach zero and the model should exhibit the same (or at least very similar) characteristics as the actual distributed parameter transmission line. The model in *Figure 2-3* does not include second order terms such as the increase in resistance due to skin effect or loss terms resulting from non-linear dielectrics. These terms and effects are discussed in the references rather than in this chapter, since they tend to obscure the basic principles under consideration. For the present, assume that the signals applied to the line have their minimum wavelengths a great deal longer than the section length of the model and ignore the second order terms.

INPUT IMPEDANCE OF A TRANSMISSION LINE

The purpose of this section is to determine the input impedance of a transmission line; *i.e.,* what amount of input current i_{in} is needed to produce a given voltage v_{in} across the line as a function of the LRCG parameters in the transmission line, (see *Figure 2-4*).

Combining the series terms lR and lL together simplifies calculation of the series impedance (Z_s) as follows

$$Z_s = l(R + j\omega L) \tag{2.7}$$

Likewise, combining lC and lG produces a parallel impedance Z_p represented by

$$Z_p = \frac{1}{Y_p} = \frac{1}{l(G + j\omega C)} \tag{2.8}$$

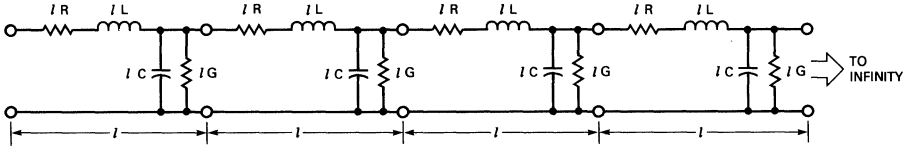


Fig. 2-3. A Transmission Line Model Composed of Short, Series Connected Sections

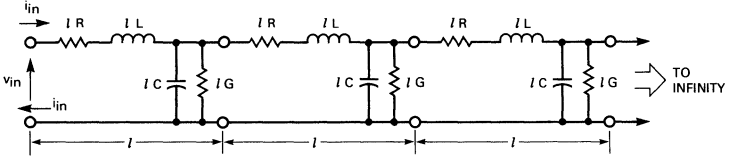


Fig. 2-4. Series Connected Sections to Approximate a Distributed Transmission Line

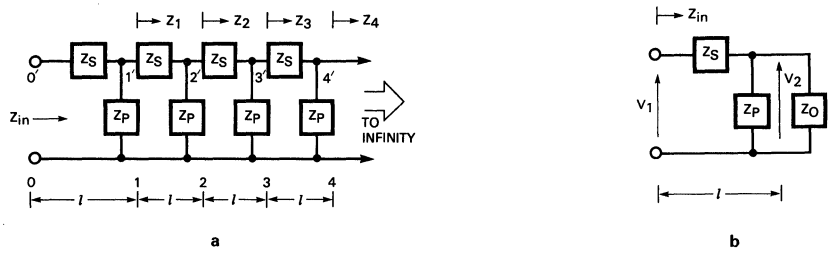


Fig. 2-5. Cascaded Network to Model Transmission Line

Since it is assumed that the line model in *Figure 2-5a* is infinite in length, the impedance looking into any cross section should be equal, that is, $Z_1 = Z_2 = Z_3$, etc. So *Figure 2-5a* can be simplified to the network in *Figure 2-5b* where Z_0 is the characteristic impedance of the line and Z_{in} must equal this impedance ($Z_{in} = Z_0$). From *Figure 2-5b*,

$$Z_{in} = Z_s + \frac{Z_0 Z_p}{Z_0 + Z_p} = Z_0 \qquad (2.9)$$

Multiplying through both sides by ($Z_0 + Z_p$) and collecting terms yields

$$Z_0^2 - Z_s Z_0 - Z_s Z_p = 0 \qquad (2.10)$$

which may be solved by using the quadratic formula to give

$$Z_0 = \frac{Z_s \pm \sqrt{Z_s^2 + 4Z_s Z_p}}{2} \qquad (2.11)$$

Substituting in the definition of Z_s and Z_p from *Equations 2.7* and *2.8, Equation 2.11* now appears as

$$Z_0 = \frac{l(R + j\omega L)}{2} \pm \frac{1}{2}\sqrt{l^2(R + j\omega L)^2 + 4\frac{R + j\omega L}{G + j\omega C}} \qquad (2.12)$$

Now, as the section length is reduced, all the parameters (lR, lL, lG, and lC) decrease in the same proportion. This is because the per-unit-length line parameters R, L, G, and C are constants for a given line. By sufficiently reducing l, the terms in *Equation 2.12* which contain l as multipliers will become negligible when compared to the last term

$$\frac{R + j\omega L}{G + j\omega C}$$

which remains constant during the reduction process. Thus *Equation 2.12* can be rewritten as

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{Z_s Z_p} \qquad (2.13)$$

particularly when the section length l is taken to be very small. Similarly, if a high enough frequency is assumed,

$$\frac{\omega}{2\pi} > 100\ kHz$$

such that the ωL and ωC terms are much larger respectively than the R and G terms, $Z_s = j\omega l L$ and $Z_p = l/j\omega l C$ can be used to arrive at a lossless line value of

$$Z_0 = \sqrt{\frac{L}{C}} \qquad (2.14)$$

In the lower frequency range,

$$\frac{\omega}{2\pi} \cong 1\ kHz$$

the R and G terms dominate the impedance giving

$$Z_0 = \sqrt{\frac{R}{G}} \qquad (2.15)$$

A typical twisted pair would show an impedance versus applied frequency curve similar to that shown in *Figure 2-6.* The Z_0 becomes constant above 100 kHz, since this is the region where the ωL and ωC terms dominate and *Equation 2.13* reduces to *Equation 2.14.* This region above 100 kHz is of primary interest, since the frequency spectrum of the fast rise/fall time pulses sent over the transmission line have a fundamental frequency in the 1-to-50 MHz area with harmonics extending upward in frequency. The expressions for

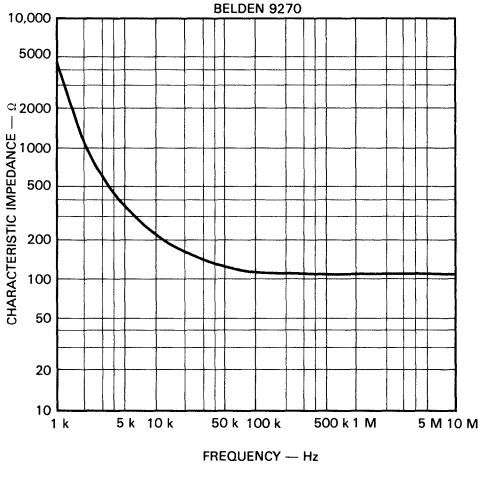


Fig. 2-6. Characteristic Impedance versus Frequency

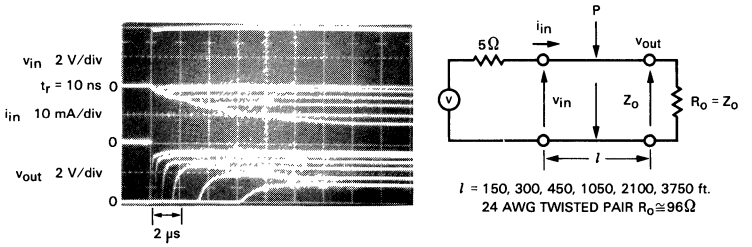


Fig. 2-7. Input Current Into a 96Ω Transmission Line for a 2 V Input Step for Various Line Lengths

Z_0 in *Equations 2.13, 2.14* and *2.15* do not contain any reference to line length, so using *Equation 2.14* as the normal characteristic impedance expression, allows the line to be replaced with a resistor of $R_0 = Z_0$ Ω neglecting any small reactance. This is true when calculating the initial voltage step produced on the line in response to an input current step, or an initial current step in response to an input voltage step.

Figure 2-7 shows a 2 V input step into a 96Ω transmission line (top trace) and the input current required for line lengths of 150, 300, 450, 1050, 2100, and 3750 feet, respectively (second set of traces). The lower traces show the output voltage waveform for the various line lengths. As can be seen, maximum input current is the same for all the different line lengths, and depends only upon the input voltage and the characteristic resistance of the line. Since $R_0 = 96\Omega$ and v_{in} = 2 V, then $i_{in} = v_{in}/R_0 \simeq$ 20 mA as shown by *Figure 2-7.*

A popular method for estimating the input current into a line in response to an input voltage is the formula

$$C(dv/dt) = i$$

where C is the total capacitance of the line (C = C per foot x length of line) and dv/dt is the slew rate of the input signal. If the 3750-foot line, with a characteristic capacitance per unit length of 16 pF/ft is used the formula $C_{total} = (C \times l)$ would yield a total lumped capacitance of .06 μF. Using this C(dv/dt) = i formula with (dv/dt = 2 V/10 ns) as in the scope photo would yield

$$I = \frac{2\ V}{10\ ns} \times .06\ \mu F = 12\ A$$

This is clearly not the case! Actually, since the line impedance is approximately 100Ω , 20 mA are required to produce 2 V across the line. If a signal with a rise time long enough to encompass the time delay of the line is used, ($t_r >> \tau$) then the C(dv/dt) = i formula will yield a reasonable estimate of the peak input current required. In the example, if the dv/dt is 2 V/20 μs, (t_r = 20 μs > τ = 6 μs) then i = 2 V/20 μs x 0.06 μF = 6 mA, which is verified by *Figure 2-8.*

Figure 2-8 shows that C(dv/dt) = i only when the rise time encompasses the capacitance to be lumped. The maximum input current requirement will be with a fast rise time step, but the line is essentially resistive, so $v_{in}/i_{in} = R_0 = Z_0$ will give the actual drive current needed. These effects will be discussed later in Chapter 3.

PHASE SHIFT AND PROPAGATION VELOCITY FOR THE TRANSMISSION LINE

There will probably be some phase shift and loss of signal v_2 with respect to v_1 because of the reactive and resistive parts of Z_s and Z_p in the model *(Figure 2-5b).* Each small section of the line (l) will contribute to the total phase shift and amplitude reduction if a number of sections are cascaded as in *Figure 2-5a.* So, it is important to determine the phase shift and signal amplitude loss contributed by each section.

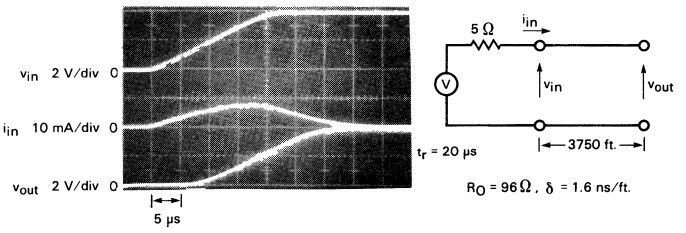


Fig. 2-8. Input Current Into Line with Controlled Rise Time $t_r > 2\tau$

Using *Figure 2-5b,* v_2 can be expressed as

$$v_2 = v_1 \frac{Z_p Z_0}{Z_p + Z_0} \frac{1}{Z_s + Z_p Z_0/(Z_p + Z_0)} \quad (2.16)$$

or

$$\frac{v_1}{v_2} = \frac{Z_s(Z_p + Z_0) + Z_p Z_0}{Z_p Z_0} \quad (2.17)$$

and further simplification yields

$$\frac{v_1}{v_2} = 1 + Z_s \left[\frac{1}{Z_0} + \frac{1}{Z_p} \right] \quad (2.18)$$

Remember that a per-unit-length constant, normally called γ is needed. This shows the reduction in amplitude and the change in the phase per unit length of the sections.

$$\gamma_l = \alpha_l + j\beta_l \quad (2.19)$$

Since

$$v_2 = v_1 \exp(-\gamma_l) = v_1 \exp(-\alpha_l) + v_1 \exp(-j\beta_l) \quad (2.20)$$

where $v_1 \exp(-\alpha_l)$ is the signal attenuation and $v_1 \exp(-j\beta_l)$ is the change in phase from v_1 to v_2,

$$\ln \left[\frac{v_1}{v_2} \right] = \ln \exp(\alpha_l + j\beta_l) = \alpha_l + j\beta_l = \gamma_l \quad (2.21)$$

Thus, taking the natural log of both sides of *Equation 2.18*

$$\ln \left[\frac{v_1}{v_2} \right] = \ln \left[1 + Z_s \left(\frac{1}{Z_0} + \frac{1}{Z_p} \right) \right] \quad (2.22)$$

Substituting *Equation 2.13* for Z_0 and Y_p for $1/Z_p$

$$\gamma_l = \ln \left[1 + Z_s \left(\sqrt{\frac{Y_p}{Z_s}} + Y_p \right) \right] \quad (2.23)$$

Now when allowing the section length l to become small,

$$Y_p = l(G + j\omega C)$$

will be very small compared to the constant $\sqrt{Y_p/Z_s} = 1/Z_0$, since the expression for Z_0 does not contain a reference to the section length l. So *Equation 2.23* can be rewritten as

$$\gamma_l = \ln \left(1 + Z_s \sqrt{\frac{Y_p}{Z_s}} \right) = \ln \left(1 + \sqrt{Y_p Z_s} \right) \quad (2.24)$$

By using the series expansion for the natural log:

$$\ln(1 + \xi) = \xi - \frac{\xi^2}{2} + \frac{\xi^3}{3} - etc. \quad (2.25)$$
$$\simeq \xi \text{ for small } \xi$$

and keeping in mind the $\sqrt{Z_s Y_p}$ value will be much less than one because the section length is allowed to become very small, the higher order expansion terms can be neglected, thereby reducing *Equation 2.24* to

$$\gamma_l = \sqrt{Z_s Y_p} = l \sqrt{(R + j\omega L)(G + j\omega C)} \quad (2.26)$$

If *Equation 2.26* is divided by the section length,

$$\gamma = \frac{\gamma_l}{l} = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (2.27)$$

the propagation constant per unit length is obtained. If the resistive components R and G are further neglected by assuming the line is reasonably short, *Equation 2.26* can be reduced to read

$$\gamma_l = j\beta_l = j\omega l \sqrt{LC} \quad (2.28)$$

Equation 2.28 shows that the lossless transmission line has one very important property: signals introduced on the line have a constant phase shift per unit length with no change in amplitude. This progressive phase shift along the line actually represents a wave traveling down the line with a velocity equal to the inverse of the phase shift per section. This velocity is

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} \quad (2.29)$$

for lossless lines. Because the LRCG parameters of the line are independent of frequency except for those upper frequency constraints previously discussed, the signal velocity given by *Equation 2.29* is also independent of signal frequency. In the practical world with long lines, there is in fact a frequency dependence of the signal velocity. This causes sharp edged pulses to become rounded and distorted. More on these long line effects will be discussed in Chapter 3.

SUMMARY — Characteristic Impedance and Propagation Delay

Every transmission line has a characteristic impedance Z_0, and both voltage and current at any point on the line are related by the formula

$$Z_0 = \frac{v}{i}$$

In terms of the per-unit-length parameters LRCG,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Since $R \ll j\omega L$ and $G \ll j\omega C$ for most lines at frequencies above 100 kHz, the characteristic impedance is best approximated by the lossless line expression

$$Z_0 \simeq \sqrt{\frac{L}{C}}$$

The propagation constant, γ, shows that signals exhibit an amplitude loss and phase shift with the latter actually a velocity of propagation of the signal down the line. For lossless lines, where the attenuation is zero, the phase shift per unit length is

$$\beta = \frac{\beta_l}{l} = \omega \sqrt{LC}$$

This really represents a signal traveling down the line with a velocity

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}}$$

This velocity is independent of the applied frequency.

The larger the LC product of the line, the slower the signal will propagate down the line. A time delay per unit length can also be defined as the inverse of v

$$\delta = \frac{1}{v} = \sqrt{LC} \qquad (2.30)$$

and a total propagation delay for a line of length l as

$$\tau = l\delta = l\sqrt{LC} \qquad (2.31)$$

For a more detailed discussion of characteristic impedances and propagation constants,the reader is referred to the references below.

Hamsher, D.H. (editor); Communications System Engineering Handbook; Chapter 11, McGraw-Hill, New York, 1967.

Reference Data for Radio Engineers, fifth edition; Chapter 22; Howard T. Sams Co., New York, 1970.

Matick, R.F.; Transmission Lines for Digital and Communications Networks; McGraw-Hill, New York, 1969.

Metzger, G. and Vabre, J.P.; Transmission Lines with Pulse Excitation; Academic Press, New York, 1969.

Section 3

REFLECTIONS: COMPUTATIONS AND WAVEFORMS

INTRODUCTION

In Section 2 it was determined that transmission lines have two important properties: one, a characteristic impedance relating instantaneous voltages and currents of waves traveling along the line and, two, a wave propagation velocity or time delay per unit length. In this chapter, both Z_0 and δ are used to compute the line voltages and currents at any point along the line and at any time after the line signal is applied. Also, concepts of reflections and reflection coefficients are explored along with calculating methods for voltages and currents.

THE INITIAL WAVE

Section 2 also showed that for most practical purposes, where fast rise and fall time signals are concerned, the characteristic impedance of the line actually behaves as a pure resistance ($R_0 = \sqrt{L/C}$).

Figure 3-1a shows a generator comprised of a voltage source (magnitude V), a source resistance of R_S ohms, and a switch closing at time t = 0 connected to a lossless, infinite length transmission line having a characteristic resistance, R_0. Because the relationship of v_{in} to i_{in} is known as $v_{in} = R_0 i_{in}$, the lossless transmission line can be replaced with a resistor as shown in *Figure 3-1b*. The loop equation is

$$i_{in}\,(R_S + R_0) = V \qquad (3.1)$$

Substituting v_{in}/R_0 for i_{in} and collecting terms shows

$$v_{in} = V\left(\frac{R_0}{R_0 + R_S}\right) \qquad (3.2)$$

This shows that both source and characteristic resistances act as voltage dividers for the source voltage V. *Figure 3-2* shows voltage and current steps for the various source resistances. Source resistances of less than R_0 produce initial voltage steps on the line which are greater than half the compliance of the source voltage, V. A matched source ($R_S = R_0$) produces voltage steps exactly half of V and source resistances greater than R_0 produce an initial voltage step less than one half V in magnitude. Generators can be classified into three categories:

- Voltage source types where $R_S < R_0$
- Matched source types $R_S = R_0$
- Current source types $R_S > R_0$

Waveforms of these types will be discussed more fully in section 4 on long line effects. Suffice to say that initial voltage wave amplitude depends greatly on source resistance. Voltage source type drivers produce higher amplitude initial voltage waves in the line than either matched source or current source type drivers.

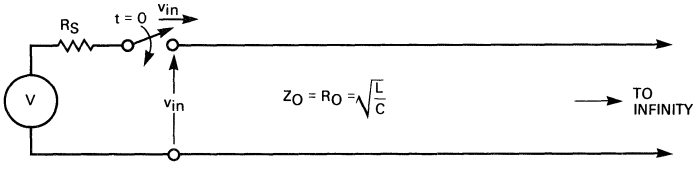


Fig. 3-1a. Generator Driving an Infinite Transmission Line

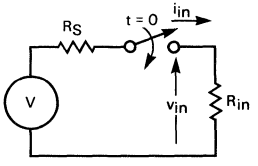


Fig. 3-1b. Thevenin Equivalent for Initial Wave

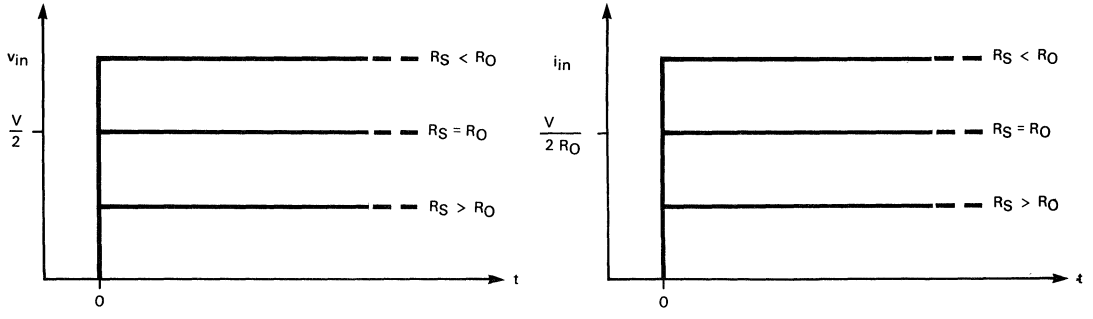


Fig. 3-2. Voltage/Current Steps for Three Source Resistances

CUT LINES AND A MATCHED LOAD

In examining an infinite, lossless line *(Figure 3-3),* it is already known that the ratio of line voltage to current is equal to the characteristic resistance of that line. The line is lossless, and the same voltages and currents should appear at point x down the line after a time delay of $x\delta$. If the line at point x is cut, and a resistor of value R_0 is inserted, there would not be a difference between the cut, terminated finite line and the infinite line. The v_x and i_x waves see the same impedance (R_0) they were launched into at time t = 0, and indeed, the waves are absorbed into R_L (= R_0) after experiencing a time delay of $\tau = x\delta$. So, from an external viewpoint, an infinite-length lossless line behaves as a finite-length lossless line terminated in its characteristic resistance.

KIRCHOFF'S LAWS AND LINE–LOAD BOUNDARY CONDITIONS

The principle of energy conservation, widely known and accepted in the sciences, applies as well to transmission line theory; therefore, energy (as power) must be conserved at boundaries between line and load. This is expressed in an English language equation as follows.

[Power available at the line end] = [Power absorbed by the load] + [Power not absorbed by the load]

Figure 3-4 shows power available at the line end is derived by the following formula. (This is assuming in-phase current and voltage).

$$P_x = i_x \cdot v_x = \frac{v_x^2}{R_0} \tag{3.3}$$

The power *absorbed* by the load will be

$$P_L = v_L \cdot i_L = \frac{v_L^2}{R_L} \tag{3.4}$$

while power *not absorbed* by the load is represented by

$$P_r = v_r \cdot i_r = \frac{v_r^2}{R_0} \tag{3.5}$$

Here, the r subscript stands for reflected (not absorbed) power, voltage or current, respectively.

Applying Kirchoff's laws to point x in *Figure 3-4,* the current to the load is

$$i_L = i_x - i_r \tag{3.6}$$

and voltage across the load is

$$v_L = i_L R_L = v_x + v_r \tag{3.7}$$

To find the ratio of v_r to v_x so that it can be ascertained how much power is absorbed by the load, and how much is not absorbed (therefore, reflected), substitute v_x/R_0 for i_x and v_r/R_0 for i_r into *Equation 3.6*.

$$i_L = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{3.8}$$

Rearranging *Equation 3.7* and substituting for i_L in *Equation 3.8* yields

$$\frac{v_x + v_r}{R_L} = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{3.9}$$

The minus sign associated with v_r/R_0 means, in this case, that the reflected voltage wave v_r travels in the –x direction toward the generator.

Collecting like terms of *Equation 3.9* yields

$$v_x\left(\frac{1}{R_0} - \frac{1}{R_L}\right) = v_r\left(\frac{1}{R_0} - \frac{1}{R_L}\right) \tag{3.10}$$

So,

$$v_r = v_x \frac{\left(\frac{R_L - R_0}{R_0 R_L}\right)}{\left(\frac{R_L + R_0}{R_0 R_L}\right)} = v_x\left(\frac{R_L - R_0}{R_0 + R_L}\right) \tag{3.11}$$

and the desired relation for v_r/v_x is

$$\frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{3.12}$$

This ratio is defined as the voltage reflection coefficient of the load ρ_{VL}

$$\rho_{VL} \equiv \frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{3.13}$$

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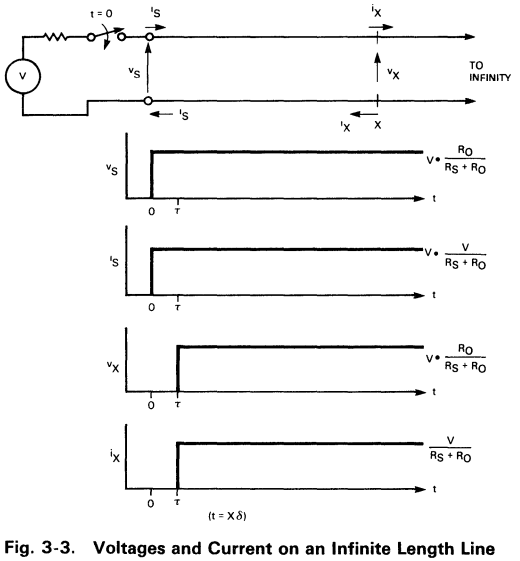


Fig. 3-3. Voltages and Current on an Infinite Length Line

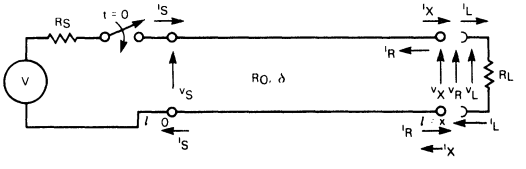


Fig. 3-4. Boundary Conditions at the Line/Load Interface

A similar derivation for currents shows

$$\rho_{IL} = -\frac{R_L - R_0}{R_L + R_0} = -\rho_{VL} \tag{3.14}$$

For the remainder of the chapters, the v or i subscript on the reflection coefficient is dropped, and ρ_L is assumed to be the *voltage* reflection coefficient of the load. Similarly, applying Kirchoff's laws to the source-line interface, the voltage reflection coefficient of the source is

$$\rho_S = \frac{R_S - R_0}{R_S + R_0} \tag{3.15}$$

The current reflection coefficient of the source has the same magnitude as ρ_S, but is opposite in algebraic sign.

When a traveling wave v_x, i_x meets a boundary such as the line load interface, a reflected wave is instantaneously generated so that Kirchoff's laws are satisfied at the boundary conditions. This is the direct result of the conservation of energy principle. Referring again to *Figure 3-4*, the effects of three different termination resistance R_L values are shown.

Case 1, $R_L = R_0$

In this case, R_L is equal to the characteristic resistance of the line. Using *Equation 3.13*, the voltage reflection coefficient of the load ρ_L is

$$\rho_L = \frac{R_0 - R_0}{R_0 + R_0} = \frac{0}{2R_0} = 0 \tag{3.16}$$

Since $v_r/v_x = \rho_L$, then $v_r = \rho_L v_x = 0$ and no reflection is generated. This agrees with the discussion of cut lines and matched load where a line terminated in its characteristic impedance behaves the same as an infinite line. All power delivered by the line is absorbed into the load. The waveforms appear as shown in *Figure 3-5*. The wave starting at the source at time t = 0 is reproduced at point x down the line after a time delay of $t = x\delta = \tau$.

Case 2, $R_L > R_0$

To simplify this case, assume that $R_S = R_0$. This means that the initial voltage is

$$V\frac{R_0}{R_0 + R_0} = \frac{V}{2} \tag{3.17}$$

Also assume $R_L = 3\ R_0$, then the load voltage reflection coefficient is

$$\rho_L = \frac{3R_0 - R_0}{3R_0 + R_0} = +\frac{1}{2} \tag{3.18}$$

The voltage wave arriving at point x at time $t = x\delta$ generates a reflected voltage wave of magnitude

$$v_r = \rho_L v_x = (+\frac{1}{2})(\frac{V}{2}) = \frac{V}{4} \tag{3.19}$$

and the load voltage is

$$v_L = v_x + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{3.20}$$

The reflected voltage wave v_r generated at $t = x\delta = \tau$ travels back down the line toward the source arriving at the source at time $t = 2x\delta = 2\tau$. This wave will be absorbed without generating another reflection because R_S was picked to equal R_0, making ρ_S equal to zero. The source voltage is now

$$v_S + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{3.21}$$

and equilibrium is achieved.

If the circuit in *Figure 3-4* is analyzed using simple circuit theory and neglecting the transmission line effects, it is easily seen that

$$v_S = v_L = V\frac{R_L}{R_0 + R_L} = \frac{3V}{4} \tag{3.22}$$

This agrees exactly with *Equation 3.21* and will always be the case. After all reflections cease and the circuit reaches equilibrium, the steady state voltages and currents on the line are the same as those produced using simple dc circuit analysis. Waveforms for $R_L > R_0$ (specifically $R_L = 3\ R_0$) appear in *Figure 3-6*.

In general, the case where $R_L > R_0$ is viewed in the following manner. Because the line is capable of delivering more pow-

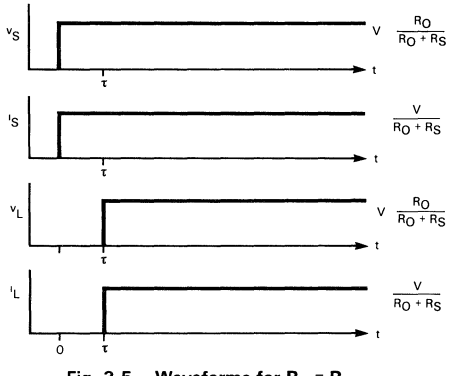


Fig. 3-5. Waveforms for $R_L = R_0$

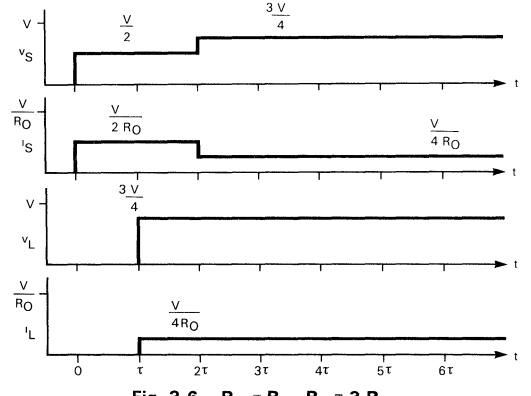


Fig. 3-6. $R_S = R_0$, $R_L = 3\ R_0$

er than can be instantaneously absorbed by the load, the excess power is returned to the source and absorbed in the source resistor (assuming $R_S = R_0$).

An upper limit on the voltage reflection coefficient is found by allowing R_L to go to infinity. In this case, *Equation 3.13* goes to +1.

Case 3, $R_L < R_0$

In this case, again set $R_S = R_0$ and allow R_L to equal $R_0/3$. The initial wave, as before, is

$$v_S = V\frac{R_0}{R_0 + R_S} = \frac{V}{2} \tag{3.23}$$

and the load voltage reflection coefficient is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{\frac{R_0}{3} - R_0}{\frac{R_0}{3} + R_0} = -\frac{1}{2} \tag{3.24}$$

Therefore, the reflected voltage wave v_r is

$$v_r = \rho_L\frac{V}{2} = -\frac{V}{4} \tag{3.25}$$

which starts propagating back toward the source at time $t = \tau$. The load voltage at time $t = \tau$ is

$$v_x + v_r = \frac{V}{2} + -\frac{V}{4} = +\frac{V}{4} \tag{3.26}$$

The (-V/4) reflected wave arrives back at the source at time $t = 2\tau$. Because R_S is set equal to R_0, ρ_S is, then, equal to zero and no reflected wave will be generated. The voltage at the source is now

$$v_S + v_r + \rho_S v_r = \frac{V}{2} + -\frac{V}{4} + 0 = \frac{V}{4} \tag{3.27}$$

From a dc circuit analysis, the steady state voltage is

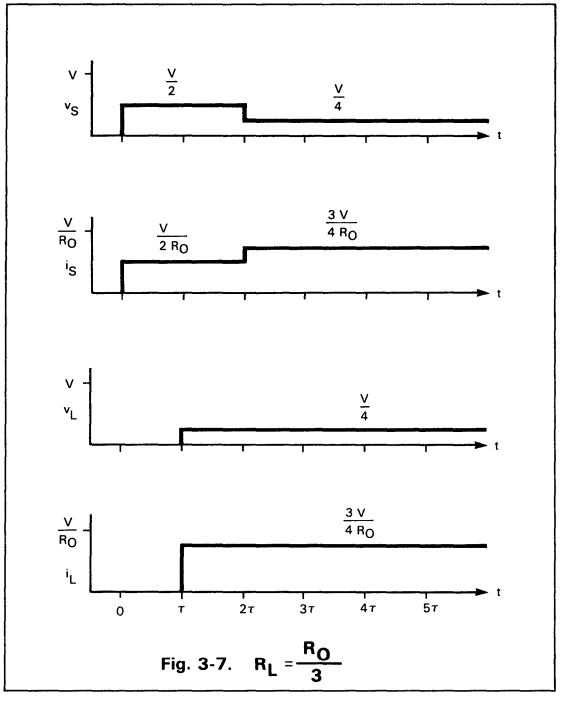


Fig. 3-7. $R_L = \frac{R_0}{3}$

$$V_{SS} = V\frac{R_L}{R_L + R_0} = \frac{V}{4} \tag{3.28}$$

This agrees with the result of *Equation 3.27*. The waveforms for Case 3 ($R_L < R_S$) appear in *Figure 3-7*.

An interpretation of the actions occurring when load resistance is less than the characteristic line resistance is as follows: when power available at the line end is less than the power the load can absorb, a signal is sent back to the source saying, in essence, "send more power".

It has been shown that a ratio of line and load resistance (ρ) can be used to calculate the voltages and currents in terms of a wave arriving at the boundary, possibly generating a reflected, reverse-traveling wave to satisfy the conservation of energy principle at the line-to-load boundary. This ratio is

$$\rho_B = \frac{R_B - R_0}{R_B + R_0} \tag{3.29}$$

where R_B represents the resistance into the boundary, R_B is R_S when considering the source-to-line interface and R_B would be R_L when considering the line-to-load interface. It is obvious that if discussing impedances, then Z_S would be substituted for R_S in *Equation 3.29*, and there may be some phase angle between the voltage and current waves.

The forward traveling wave, v_x, plus the reflected wave, v_r, is equal to the load voltage (V_L). Since v_r is $\rho_L v_x$, this can be expressed as

$$v_x(1 + \rho_L) = v_L \tag{3.30}$$

This quantity $(1 + \rho)$ can be defined as the voltage *transmission* coefficient of the load and it is known that

$$\frac{v_L}{v_x} = (1 + \rho_L) \tag{3.31}$$

The cases with various load resistances can be summarized.

Condition		Circuit at time $t = \tau$ (one line delay time)
1. $R_L = R_0$	$\rho_L = 0$	No reflection is produced—circuit reaches steady state immediately.
2. $R_L > R_0$	$\rho_L > 0$	Positive voltage reflection—wave is sent back toward source. Voltage at load is higher than steady stage voltage (overshoot).
3. $R_L < R_0$	$\rho_L < 0$	Negative voltage reflection—wave is sent back toward source. Voltage at load is lower than steady state voltage (undershoot).

FUNDAMENTAL PRINCIPLES

Before examining the algorithm for keeping track of reflections, there are two principles to keep in mind.

- Energy (as power) is conserved at boundary conditions (as explored previously)
- The principle of linear superposition applies. This means any arbitrary excitation function can be broken down into step functions, or ramps. The reaction of the circuit to each part can be analyzed, and the results can be added together when finished. This means that a positive pulse of duration t is examined by superimposing two step functions,

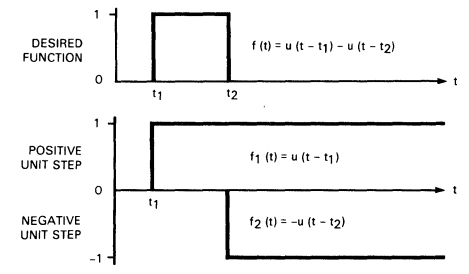


Fig. 3-8. Superposition of Simple Waveforms to Form More Complex Excitations

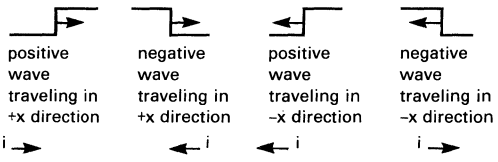


Fig. 3-9. Sign Conventions for Waves

one positive and one negative, starting after a delay of t *(Figure 3-8).* It also means the voltage at any point on the line is the sum of initial voltage plus the sum of all voltage waves that have arrived at or passed through the point up to and including the time of examination. Also, the current on the line is, at any point, the sum of initial current plus any forward or reverse traveling currents passing the point up to and including the time the current is examined.

It has also been established that the steady state solution for voltages and currents on the line can be found by simple dc circuit analysis.

In examining reflection effects for the remainder of this book, the following conventions are used.

A voltage or current wave traveling *toward* the point of interest will have the subscript "i" for *incident* wave.

A voltage or current wave traveling *away* from the point of interest will have the subscript "r" for *reflected* wave,

The subscript "S" means the parameter applied to the *source* (v_S for the voltage at the source, etc.), and

The subscript "L" means the parameter applied to the *load* (v_L for the voltage at the load, etc.)

Sign conventions for voltage waves and their associated currents are shown in *Figure 3-9.*

TABULAR METHOD FOR REFLECTIONS — THE LATTICE DIAGRAM

The waves going up and down the line can be monitored by drawing a time scale, as a vertical line with time increasing in the down direction, to represent the location on the line under examination. Because voltages at the source and load ends of the transmission line are normally of primary interest, two time scales are necessary. Drawing arrows from one time scale to the other as in *Figure 3-10* shows the direction of travel of the waves during a specific time interval. Since the main concern is only with the waveforms at the line ends, time scales are ruled off in multiples of the time delay of the line τ. If a unit-step type wave is launched from the source at time t = 0+, it is known that the magnitude of the wave will persist unchanged until a wave arrives back from the load after a round trip delay time of two line delays. The source time scale then is incremented in multiples of $2m\tau$ where m = 0, 1, 2, 3, . . . Likewise, the first wave arrives at the load after a single time delay, so the first increment ruling on the load time scale is τ, or one time delay of the line. Because the subsequent waves arrive back at the load in increments of 2τ, the load time scale is ruled off in multiples of $(2m + 1)\tau$ where m = 0,1,2,3, . . . The operation of the lattice diagram is discussed using the example in *Figure 3-10b* which is the lattice diagram for the associated circuit.

time t = 0– (just before the switch closes)

The voltages at the source and load are equal with a magnitude of $v_{initial}$. Assume that no initial voltage is present. So, in this case, the voltage at the source and load equals zero.

$$V_{initial} = v_S(0^-) = v_L(0^-) = 0$$

time t = 0+ (just after the switch has closed)

The first wave $v_i(1)$ is launched at the source and begins to travel toward the load end of the line. As previously mentioned, a voltage divider action between R_S and R_0 is used to derive the magnitude of the initial voltage wave.

$$v_i(1) = V\frac{R_0}{R_0 + R_S}$$

At this time, the voltage at the source is the sum of the initial voltage plus the voltage wave $v_i(1)$ just generated.

$$v_S(0+) = v_S(0^-) + v_i(1) = 0 + V\frac{R_0}{R_0 + R_S}$$

Because the switch closure represents a step function, the source voltage remains at this level until a wave returns after reflecting from the load at time $t = 2\tau$

time $t = \tau$

The incident voltage wave $v_i(1)$ now arrives at the load and generates a reflected voltage wave

$$v_r(1) = \rho_L v_i(i); \quad \rho_L = \frac{R_L - R_0}{R_L + R_0}$$

where ρ_L is the voltage reflection coefficient of the load. The reflected voltage wave $v_r(1)$ immediately starts traveling back toward the source becoming the incident voltage wave $v_i(2)$ which arrives back at the source at $t = 2\tau$. The voltage at the load is now the sum of the initial voltage plus the incident voltage wave $v_i(1)$ that just arrived plus the reflected voltage wave that is just departing.

$$v_L(1) = v_L(0^-) + v_i(1) + v_r(1)$$

$$= 0 + v_i(1) + \rho_L v_i(1)$$

$$= v_i(1)\ (1 + \rho_L)$$

Again, because of the step function excitation, the load voltage remains unchanged until the new wave arrives at time $t = 3\tau$.

time $t = 2\tau$

$v_i(2)$ now arrives at the source and generates a reflected voltage wave $v_r(2)$ of magnitude

$$v_r(2) = \rho_S v_i(2); \quad \rho_S = \frac{R_S - R_0}{R_S + R_0}$$

where ρ_S is the source voltage reflection coefficient.

The reflected voltage wave $v_r(2)$ starts back toward the load end of the line and becomes the incident voltage wave $v_i(3)$ arriving at the load at time $t = 3\tau$. The voltage at the source is now the sum of the voltage that was there plus the incident voltage wave just arrived plus the reflected voltage wave just departed for the load.

$$v_S(2) = v_S(0+) + v_i(2) + v_r(2)$$

$$= V\frac{R_0}{R_0 + R_S} + v_i(2) + \rho_S v_i(2)$$

$$= V\frac{R_0}{R_0 + R_S} + v_i(2)\ (1 + \rho_S)$$

time $t = 3\tau$

$v_i(3)$ arrives at the load generating $v_r(3)$

$$v_r(3) = \rho_L v_i(3)$$

$v_r(3)$ departs back toward the source becoming $v_i(4)$ to the source. The load voltage is now

$$v_L(3) = v_L(1) + v_i(3)\ (1 + \rho_L)$$

time $t = 4\tau$

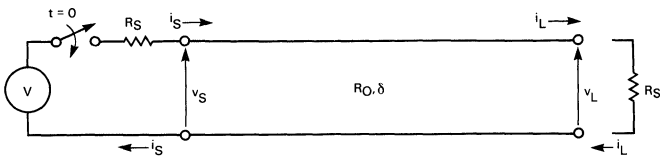
When $v_i(4)$ arrives at the source and generates $v_r(4)$, then

$$v_r(4) = \rho_S v_i(4)$$

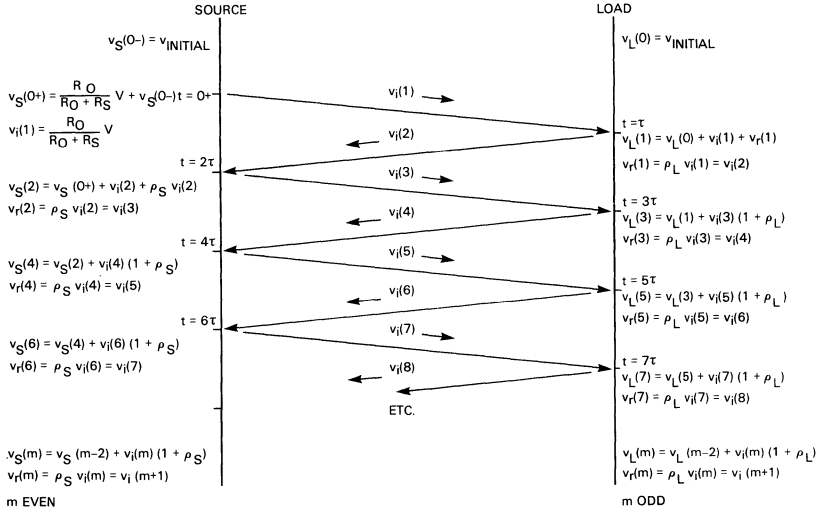
starts back toward the load to become $v_i(5)$ to the load. The load voltage is now

$$v_L(4) = v_L(2) + v_i(4)\ (1 + \rho_L)$$

This process can continue ad infinitum or until no measurable changes are detected. The reflection process at that time is considered complete and the line assumes a steady state condition. Steady state conditions can be found by applying simple dc circuit theory to source load circuits.



(a) Line Circuit to be Analyzed



(b) Lattice Diagram

Fig. 3-10. Reflection Bookkeeping with the Lattice Diagram

Summarizing this lattice diagram method, any time $t = m\tau$ and $m > 1$, the following relationships exist:

If m is odd, the $v_i(m)$ wave is arriving at the load and generates a reflected wave

$$v_r(m) = \rho_L v_i(m)$$

This becomes $v_i(m+1)$ as it starts toward the source. The voltage at the load at time $t = m\tau$ will be

$$v_L(m) = v_L(m-2) + v_i(m)\,(1 + \rho_L)$$

This is the sum of the voltage that was there before the wave arrived, *i.e.*, $v_L(m-2)$, plus the wave arriving $v_i(m)$ and the reflected wave $v_r(m)$ departing.

If m is even, the $v_i(m)$ wave is arriving at the source and generates a reflected wave

$$v_r(m) = \rho_S v_i(m)$$

This becomes $v_i(m+1)$ as it starts toward the load. The voltage at the source is now

$$v_S(m) = v_S(m-2) + v_i(m)\,(1 + \rho_S)$$

This is the sum of the voltage that was present $v_S(m-2)$ plus the incident wave arriving $v_i(m)$ plus the reflected wave departing $v_r(m)$.

The voltage and current at the source end of the line for a lossless line can be expressed as a summation.

$$v_S(t) = \frac{R_0}{R_S + R_0} \bullet \left[e(t)u(t) + \left(1 + \frac{1}{\rho_S}\right) \sum_{n=1}^{\infty} \rho_S{}^n \rho_L{}^n e(t-2n\tau)u(t-2n\tau)\right] \tag{3.32}$$

$$i_S(t) = \frac{1}{R_S + R_0} \bullet \left[e(t)u(t) + \left(1 - \frac{1}{\rho_S}\right) \sum_{n=1}^{\infty} \rho_S{}^n \rho_L{}^n e(t-2n\tau)\,u(t-2n\tau)\right] \tag{3.33}$$

where e(t) is the generator voltage as a function of time, and u(t) is the unit step function.

Likewise, the load voltage and load current for the lossless line can be expressed as a summation.

$$v_L(t) = \frac{R_0}{R_S + R_0} \bullet (1+\rho_L)\left[\sum_{n=0}^{\infty} \rho_S{}^n \rho_L{}^n e(t-(2n+1)\tau)u(t-(2n+1)\tau)\right] \tag{3.34}$$

$$i_L(t) = \frac{1}{R_S + R_0} \bullet (1-\rho_L)\left[\sum_{n=0}^{\infty} \rho_S{}^n \rho_L{}^n e\,(t-(2n+1)\,\tau)\,u\,(t-(2n+1)\,\tau)\right] \tag{3.35}$$

A similar expression of summation can be developed for the voltage (or current) at any point along the line at any time.

Because the lattice diagram is tabular in method, a computer program can be written relieving the designer of bookkeeping and repetitive calculations. A BASIC computer program for lattice diagrams appears in *Figure 3-13.*

LIMITATIONS OF THE LATTICE DIAGRAM METHOD

Before using the lattice diagram to explore reflection effects with various source and load characteristics, it is necessary to pause at this point and examine the models used by the lattice diagram.

First, both the line driver and receiver are simulated either by a constant input or output resistance. The source has two voltage sources and a switch representing the internal source voltage at a time less than zero and equal to (or greater than) zero. The receiver is represented by a single resistor shunting the line end opposite the driver site. The line itself is represented by its characteristic resistance R_0 and its total one-way time delay (τ). This is equal to length times propagation delay per unit length. This model is shown in *Figure 3-11.*

Because most data communication circuits are voltage types, that is, the receiver senses the line voltage to decide if a logic One or logic Zero is present, the primary interest is in voltages at the source and load as a function of time. Major exceptions include the current loops used in teletypewriters, telegraphs, and burglar alarm systems. The majority of data communications circuits used in computers, peripherals, and general controllers are voltage types.

The lattice diagram method cannot easily use source or receiver current/voltage relationships that are non-linear; *i.e.*, not purely resistive. For non-linear current/voltage character-

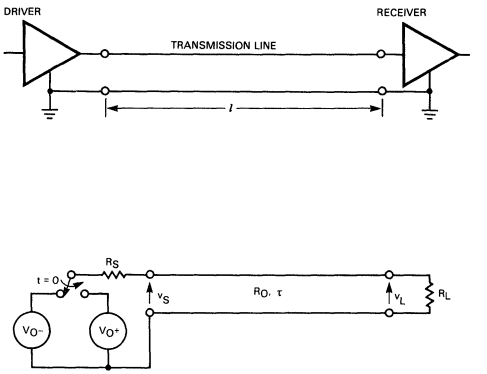


Fig. 3-11. Model used for Lattice Diagram Method

istics such as found in diodes, a graphic method can be used called the reflection diagram or the Bergeron* method.

Signals exchanged using lattice diagrams are of the unit step variety. When ramps or more complex waves are exchanged, the complexity of the bookkeeping increases dramatically. Additionally, the lines are presumed to be lossless, although a constant line attenuation factor could be accommodated without excessive bookkeeping. These limitations should be kept in mind when examining various source and load resistance combinations and their reflection characteristics.

There are three classes of source resistance, $R_S < R_0$, $R_S = R_0$ and $R_S > R_0$. There are also three classes of load resistance, $R_L < R_0$, $R_L = R_0$ and $R_L > R_0$. This gives nine types of single driver, single receiver line circuits. Each circuit will be examined in turn to determine reflection effects for these combinations with evaluations of each combination for voltage type communications.

REFLECTION EFFECTS FOR VOLTAGE SOURCE DRIVERS

Initial waves launched by a voltage source type driver ($R_S < R_0$) are greater than one-half the magnitude of the internal voltage source. Referring to *Figure 3-11,* the initial voltage wave is derived as follows.

$$v_i(1) = (V_{0+} - V_{0-}) \cdot \frac{R_0}{R_0 + R_S} \qquad (3.36)$$

while the voltage at the source at t = 0+ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \cdot \frac{R_L}{R_L + R_S} + v_i(1) \qquad (3.37)$$

If the receiver switching point is at the mean of the driver voltage swing, the initial wave always has sufficient magnitude to indicate the correct logic state as it passes the receiver site. This maximizes the noise margins of the receiver.

Since $R_S < R_0$, the source voltage reflection coefficient ρ_S is less than zero. Any voltage waves, then, arriving back at the source are changed in sign, reduced in amplitude (assuming $R_S > 0\Omega$), and sent back toward the load. If the load resistance equals the characteristic line resistance ($R_L = R_0$), the voltage reflection coefficient of the load is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{0}{2R_0} = 0$$

No reflections, therefore, are generated at the load. The voltage wave produced at the source is reproduced at the load after a time delay of $\tau = \ell\delta$, and the line assumes a steady state condition. *Figure 3-12b* illustrates the source and load voltage waveforms for this case.

If R_L is greater than R_0, ρ_L is positive. Waves arriving at the load generate the same polarity reflections as the arriving waves. ρ_S and ρ_L are of opposite signs, so a dampened oscillatory behavior of the load voltage is expected. The oscillation period or *ringing* is 4τ. The overshoot of v_L from $t = \tau$ to 3τ may cause breakdown of the input circuitry of a receiver, depending on the receiver voltage rating. The undershoot at $t = 3\tau$ to 5τ can reduce the noise immunity of a receiver or even cause a logic level misinterpretation — an error in the data. These waveforms are shown in *Figure 3-12a.*

If R_L is less than R_0, then ρ_L is negative and a wave arriving at the load generates a reflection opposite in polarity to the incident wave. This causes the voltage at the source to overshoot steady state voltage at t = 0. Each reflection returning from the load causes the source voltage to continually step down toward the steady state voltage V_{SS}. These steps last for 2τ, or one round trip delay. Load voltage starts an increasing step-up waveform towards V_{SS} at time $t = \tau$, with steps again taking one round trip delay, 2τ. A line receiver placed in the middle of the line sees an entirely different waveform — dampened oscillations much like the load voltage in *Figure 3-12a.* This is caused by the negative signs of both source and load voltage reflection coefficients. Each time an incident wave arrives at either source or load, the reflected wave generated at that time has a sign opposite to the sign of the incident voltage wave. The voltage at a distance half way down the line is composed of these forward and reverse traveling waves arriving at that point commencing at time $t = 0.5\tau$, and with each new wave passing that point after one line delay (τ). These waveforms are shown in *Figure 3-12c.*

The optimum load resistance for voltage signal communications on transmission lines driven by a low impedance source ($R_S < R_0$) is equal to the characteristic line resistance. Large signal line voltages are produced and there are no reflection effects complicating the waveforms *(Figure 3-12b).*

However, a matched load ($R_L = R_0$) is a dc load on the driver, thus it increases system power dissipation. But, it does preserve signal fidelity and amplitude allowing use of multiple bridging receivers ($R_{in} \gg R_0$) along the line.

The unterminated case ($R_L > R_0$) reduces dc driver loading and also reduces system power dissipation over the matched load case. The unterminated case does, however, allow the load signal to exhibit pronounced overshoot and undershoot around the steady state voltage. If the load signal undershoot places the receiver in its threshold uncertainty region, data errors result. There is a way to "civilize" the voltage waveform of the unterminated line load by trading off signal rise time versus line time delay. This is discussed later.

The final case of $R_S < R_0$ and $R_L < R_0$ is not generally useful in terms of voltage signals produced *(Figure 3-12c.)* Systems using this case consume more power than the previous two cases and have no particular advantage for voltage mode communications.

REFLECTION EFFECTS FOR MATCHED-SOURCE DRIVERS

In all three cases under discussion here, the initial voltage produced by the driver onto the line is

$$v_i(1) = (V_{0+} - V_{0-}) \frac{R_0}{R_0 + R_S} = \frac{1}{2}(V_{0+} + V_{0-}) \qquad (3.38)$$

*A French hydraulic engineer, L.J.B. Bergeron developed the method to study the propagation of water hammer effects in hydraulics. See references, Chapter 2.

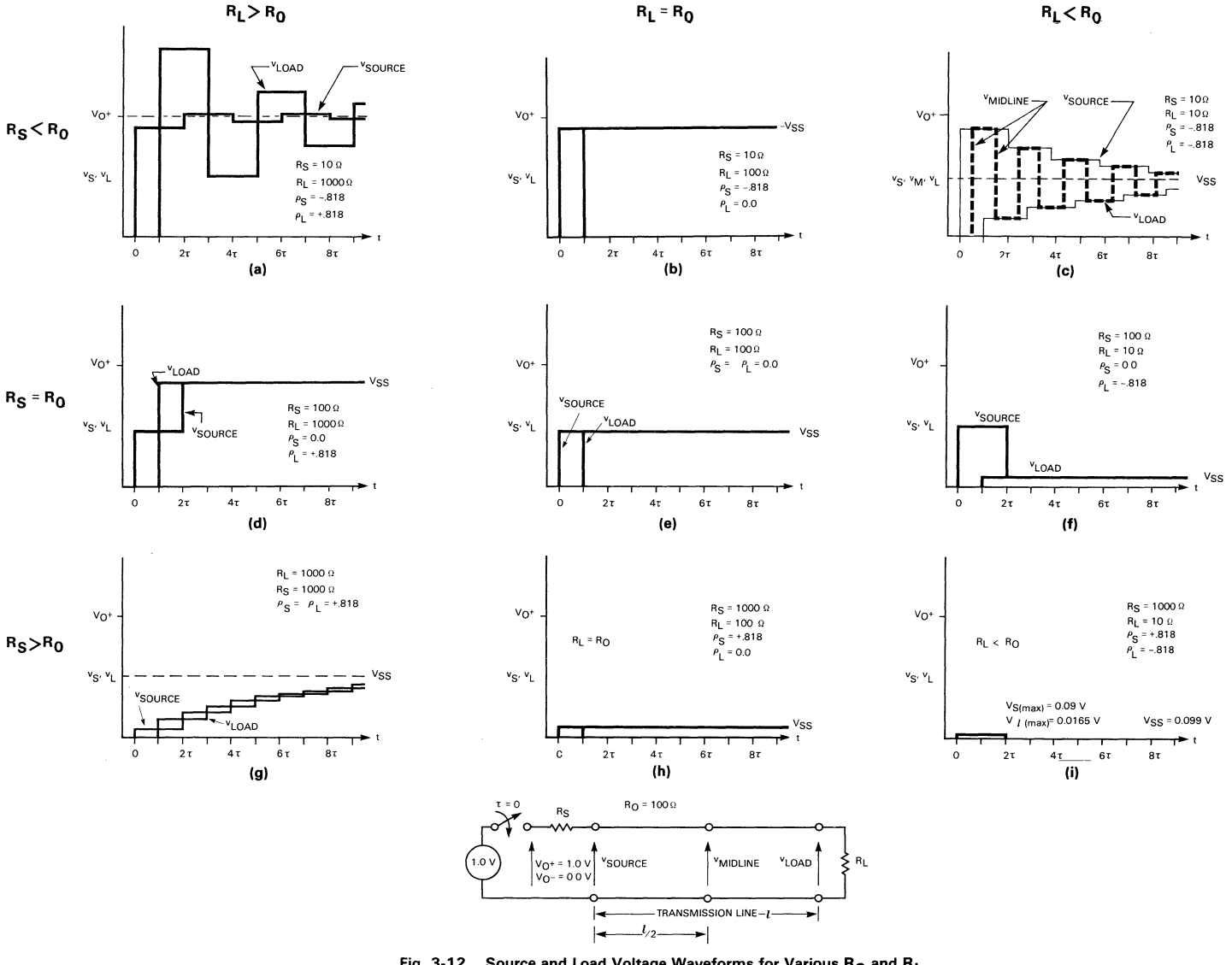


Fig. 3-12. Source and Load Voltage Waveforms for Various R_S and R_L

since $R_S = R_0$. The voltage at the source at time t = 0+ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \cdot \frac{R_L}{R_L + R_S} + v_i(1) \quad (3.39)$$

Assume, for clarity, that initial voltage (V_{0-}) is zero, thus *Equation 3.39* simplifies to

$$v_S(0+) = \frac{V_{0+}}{2} \quad (3.40)$$

Since $R_S = R_0$, ρ_S is equal to zero. This means that load-generated reflections due to load mismatch are absorbed at the source when, at time $t = 2\tau$, the reflected wave arrives back at the source. The line then assumes a steady state throughout. This back match or series termination effect of a matched source allows a wide latitude in choice of load resistance without sacrificing the signal fidelity of the load voltage waveform.

If the load resistance equals the characteristic line resistance $R_L = R_0$, then ρ_L equals zero and no load site reflections are generated. The initial voltage wave arrives at the load at time $t = \tau$ (one line delay) and voltages (and currents) on the line immediately assume steady state conditions (see *Figure 3-12e*). The optimum receiver threshold here is one-half the steady state voltage or $V_{0+}/4$. The main advantage over the voltage source type driver with matched load case ($R_S < R_0$, $R_L = R_0$) is that R_S and R_L resistance tolerances may be relaxed without incurring much signal *ringing*. This effect is due primarily to the termination provided by both line ends, rather than just one line end. Any reflected voltage wave on either system is attenuated by the product of ρ_S and ρ_L for each round trip line delay time. Since the $\rho_S\rho_L$ product for the fully matched case is smaller than the $\rho_S\rho_L$ product for the single matched case, the reflections are attenuated and die out in fewer round trips. For example, if 20% tolerance resistors are used in both cases, ρ_S and ρ_L values for the fully matched case become 0.0 ± 0.0909, which is a $\rho_S\rho_L$ product of ± 0.0033. This means that after one round trip (2τ), the reflection amplitude starting back toward the load would be less than 0.33% of the initial wave.

Using $R_S = 10\ \Omega$, $R_L = 100\ \Omega$, and $R_0 = 100\ \Omega$ as for *Figure 3-12a*, shows the same 20% tolerances applied to the single matched case

$$-0.8519 \leqslant \rho_S \leqslant -0.7857$$

$$-0.0909 \leqslant \rho_L \leqslant +0.0909$$

and

$$|\rho_S\rho_L| \leqslant 0.0774$$

The voltage reflection amplitude after one round trip is a maximum of 7.7% of the initial wave.

The choice between using the single and fully matched system should be carefully considered because the fully matched system does sacrifice signal voltage magnitude to get a decreased dependence on absolute resistor values.

If the load resistance for a matched driver circuit is made much greater than the line resistance, the initial wave arriving at the load at time $t = \tau$ will be almost doubled since ρ_L will be close to +1.0. Because source resistance is set equal to line resistance, ρ_S becomes zero, the reflected voltage wave from the load is absorbed by the source at time $t = 2\tau$, and steady state conditions prevail. Waveforms for this case are shown in *Figure 3-12d.* This is called *back matching* or *series termination.*

The main advantage of series termination is a great reduction in steady state power consumption when compared with the parallel terminated case ($R_S \ll R_0$, $R_L = R_0$). At the same time, series termination provides the same signal fidelity to a receiver placed at the line end. Compare the load voltage waveforms for the two cases in *Figure 3-12b* and *3-12d.* The main disadvantage to series termination is that receivers placed along the line see a waveform similar to that shown for the source in *Figure 3-12d.* That is, receivers along the line see the $V_{0+}/2$ initial wave as it passes that point on the line, and do not see a full signal swing until the load end reflection passes that point. Consequently, receivers along the line do not see a signal sufficient to produce the valid logic state output until the load reflection returns. Depending on actual line length and receiver characteristics, the receiver may even oscillate, having been placed in its linear operation region. With the benefit, then, of reducing system power, the series termination method has a constraint of allowing only one line receiver located at the line load end. The parallel termination method should be used if other receivers along the line are required.

The final case of matched source drivers is with the use of a load resistance less than the characteristic line resistance. The waveforms for this case are shown in *Figure 3-12f.* A line receiver with a threshold of $V_0/4$ placed at the source responds like a positive, edge triggered one-shot and produce a pulse in response to a $+V/2$ initial wave of 2τ duration. Aside from its use as a one-shot, this circuit doesn't seem to offer any advantages for voltage mode communications.

REFLECTION EFFECTS FOR CURRENT-SOURCE DRIVERS

The name *current source drivers* is somewhat of a misnomer, and might be more properly called *current-limited voltage source drivers.* True *current source* drivers such as the 75110 are normally used in conjunction with parallel termination resistors to create a matched source.

The *current source* drivers ($R_S > R_0$) discussed resemble true current sources in the respect that their output resistance is usually much greater than the characteristic line resistance. The initial voltage step produced on the line is thus usually small $v_i(1) = (i_S(1)R_0)$. This is due to the voltage divider action of the driver source resistance and the characteristic line resistance.

Voltage waveforms for a current source type driver either step up to V_{SS}, reach steady state after 2τ, or execute a dampened oscillation around V_{SS}, depending on whether the load resistance R_L is greater, equal, or less than R_0, respectively. The second case $R_L = R_0$ provides signals much the same as the other two cases where $R_L = R_0$, that is, the source voltage steps immediately to V_{SS}, with the load voltage following after one line time delay. Here the amplitude of

the signal is much smaller than previous matched load cases. Since the current source type drivers (75109/110) have high off-state impedances, they allow multiple drivers on the line to produce a data bus or party line. This aspect will be discussed in more detail in Chapter 5. Waveforms for the matched load case are shown in *Figure 3-12h.*

The case $R_L < R_0$ really provides no useful advantage for voltage mode communications. The negative sign for ρ_L and the positive sign for ρ_S lead to dampened oscillatory behavior, or ringing. The maximum perturbation takes place at the source end of the line. Waveforms for this case are similar to those shown in *Figure 3-12a*, and are shown to scale in *Figure 3-12i*. With the given values used to produce the figure, the maximum amplitude ringing appears at the source line end.

The $R_L > R_0$ case is of interest because it is representative of DTL driving a transmission line with the output going from LOW to HIGH. DTL has a high value R_S, (2 kΩ or 6 kΩ) in the HIGH logic state. Since both R_S and R_L are greater than R_0*, both ρ_S and ρ_L are positive. A small voltage step starts from the source at t = 0+; its magnitude is

$$v_i(1) = V\frac{R_0}{R_0 + R_S}$$

Upon arrival at the load at time $t = \tau$, this initial wave generates a positive voltage reflection since $\rho_L > 0$. The voltage reflection arrives back at the source site at time $t = 2\tau$. Since ρ_S is also positive, another positive voltage reflection is launched back toward the load. The process repeats, and the source and load voltages both execute a step-up approach toward steady state voltage V_{SS}. These waveforms are shown in *Figure 3-12g*.

In examining voltage at the line midpoint (x = ℓ/2), a step-up type waveform is seen which is the sum of all the incident voltage waves passing the line midpoint up to the time of examination. The midpoint voltage is expressed as follows.

$$v_m(t) = V_{SS}\left(1 - exp\left[-(t + 0.5\,\tau)/T\right]\right) \quad (3.41)^{**}$$

for $t = n + 0.5\tau$ with n = 0,1,2,3,etc. V_{SS} in *Equation 3.41* is the steady state line voltage

$$V_{ss} = V_{0+} \cdot \frac{R_L}{R_S + R_L}$$

and T is a time constant given by

$$T = -\frac{2\tau}{ln\ (\rho_S \rho_L)} \quad (3.42)^{**}$$

with τ being one line delay ($\tau = l\ \delta$).

Equation 3.41 provides an exact solution for odd multiples of n (n = 1,3,5 . . . , so $t = 1.5\tau$, 3.5τ , 5.5τ . . .), while it approximates $v_m(t)$ for even multiples of n (n = 0,2,4 . . . , so $t = 0.5\tau$, 2.5τ , 4.5τ . . .). The closer the $\rho_S\,\rho_L$ product is to 1, the better *Equation 3.41* predicts $v_m(t)$, particularly for even multiples of n. To illustrate the fitting, the two tables in *Figure 3-13* are generated by the BASIC language computer program *(Table C)* and their data is plotted in *Figure 3-14*.

*Since the input diode is not represented, the representation of DTL input as a single resistor to ground is not strictly correct. For purposes of approximation, this simple representation is used. Treatment of non-linear current/voltage sources and loads is covered by Metzger & Vabre. (op. cit.)

**This equation is presented without derivation, but a procedure similar to that used by Matick (Ref.[2], Chapter 2) can be used.

Table (a). (R_S = 2000 ohms, R_0 = 100 ohms, R_L = 4000 ohms)

RHOS= .904762 RHOL= .951220 TAU= -13.3250
VI(1)= 4.76190E-02 VSS= .666667

TIME	VM(T)	VAPPX	%DIFF
0.5	0.04762	0.04820	+1.220%
1.5	0.09292	0.09292	+0.000%
2.5	0.13390	0.13440	+0.373%
3.5	0.17288	0.17288	+0.000%
4.5	0.20815	0.20858	+0.207%
5.5	0.24170	0.24170	+0.000%
6.5	0.27206	0.27243	+0.136%
7.5	0.30093	0.30093	+0.000%
8.5	0.32705	0.32737	+0.097%
9.5	0.35190	0.35190	+0.000%
10.5	0.37439	0.37466	+0.073%
11.5	0.39577	0.39577	+0.000%
12.5	0.41512	0.41536	+0.057%
13.5	0.43353	0.43353	+0.000%
14.5	0.45018	0.45038	+0.045%
15.5	0.46602	0.46602	+0.000%
16.5	0.48035	0.48053	+0.036%
17.5	0.49399	0.49399	+0.000%
18.5	0.50632	0.50647	+0.030%
19.5	0.51805	0.51805	+0.000%
20.5	0.52867	0.52880	+0.024%
21.5	0.53877	0.53877	+0.000%

Table (b). (R_S = 500 ohms, R_0 = 75 ohms, R_L = 10 kilohms)

RHOS= .739130 RHOL= .985112 TAU= -6.30356
VI(1)= .130435 VSS= .952381

TIME	VM(T)	VAPPX	%DIFF
0.5	0.13043	0.13971	+7.112%
1.5	0.25893	0.25893	+0.000%
2.5	0.35390	0.36066	+1.909%
3.5	0.44746	0.44746	+0.000%
4.5	0.51661	0.52153	+0.952%
5.5	0.58473	0.58473	+0.000%
6.5	0.63509	0.63867	+0.564%
7.5	0.68469	0.68469	+0.000%
8.5	0.72135	0.72396	+0.361%
9.5	0.75747	0.75747	+0.000%
10.5	0.78416	0.78606	+0.242%
11.5	0.81046	0.81046	+0.000%
12.5	0.82990	0.83128	+0.167%
13.5	0.84904	0.84904	+0.000%
14.5	0.86320	0.86420	+0.117%
15.5	0.87714	0.87714	+0.000%
16.5	0.88744	0.88818	+0.083%
17.5	0.89759	0.89759	+0.000%
18.5	0.90510	0.90563	+0.059%
19.5	0.91249	0.91249	+0.000%
20.5	0.91795	0.91834	+0.042%
21.5	0.92334	0.92334	+0.000%

Table (c). BASIC Program Listing

```
100 PRINT"ENTER RS,RO,RL";
110 INPUT R1,RO,R2
120 P1=(R1-RO)/(R1+RO)
130 P2=(R2-RO)/(R2+RO)
140 V1=RO/(R1+RO)
150 K1=2./LOG(P1*P2)
160 V9=R2/(R1+R2)
170 PRINT"RHOS=";P1;"RHOL=";P2;"TAU=";K1
180 PRINT"VI(1)=";V1;"VSS=";V9
190 V=V1
200 PRINT"TIME     VM(T)     VAPPX     %DIFF"
210 FOR T=0.5 TO 20.5 STEP 2.
220 V2=V9*(1.-EXP((T+.5)/K1))
230 P=100.*(V2-V)/V
240 PRINTUSING 250,T,V,V2,P
250 ###.#  -#.#####  -#.#####  +###.###%
260 V1=V1*P2
270 V=V+V1
280 REM   SOURCE END
290 V2=V9*(1.-EXP( (T+1.5)/K1 ) )
300 P=100.*(V2-V)/V
310 PRINTUSING 250,T+1.,V,V2,P
320 V1=P1*V1
330 V=V+V1
340 NEXT T
350 PRINT
360 PRINT
370 PRINT
380 GOTO 100
390 END
```

Fig. 3-13. Comparison of v_m Formula to Computed Midline Voltage

Designers familiar with DTL circuits should quickly recognize that the waveforms shown in *Figure 3-14* are very similar to the rising edge waveforms found when a DTL gate output goes from the LOW to HIGH state. This characteristic waveform has usually been attributed to the series RC circuit (a gate output resistance driving a lumped transmission line capacitance.) The time constant for this approach, based on the C(dv/dt) = i rule from simple circuit theory, provides only an approximation. The actual cause of the waveform shape, however, is due to reflection effects. Unfortunately, the only way to speed up the rising edge is to reduce source resistance, (providing an initial step greater than the receiving threshold) and terminate the line to eliminate the load reflections.

DTL inability to drive transmission lines at high repetition rates is the direct result of the signal rise time limitation caused by positive reflection coefficients for both the source and load. A transmitted positive pulse may be missed if its duration is less than the time required for the load signal to reach the receiver threshold.

The $R_S > R_0$ and $R_L > R_0$ case provides no definite advantages as voltage mode communication is concerned. This case, in fact, poses a definite hazard to high speed data communications because the reflections cause, in effect, a slow, exponential signal transition. Because line delay is a factor, longer lines will only increase the effect.

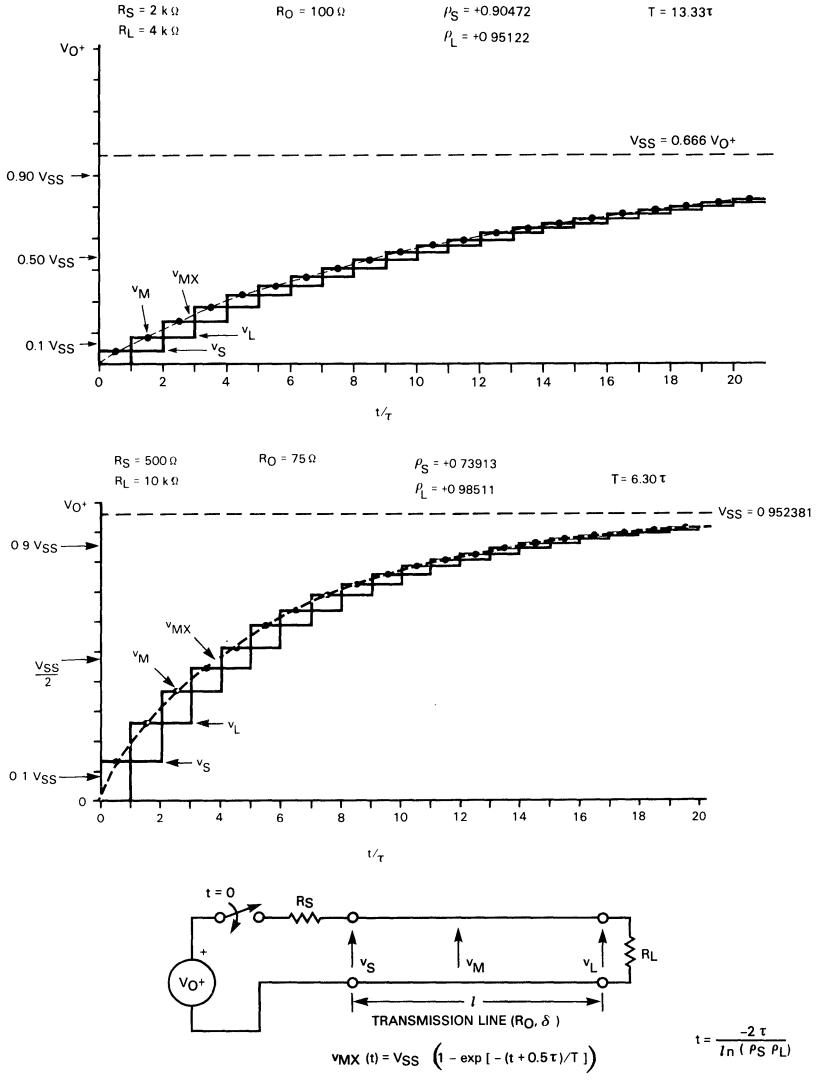


Fig. 3-14. Approximation of Midline Voltage with $R_S > R_0$ and $R_L > R_0$

SUMMARY — Which are the Advantageous Combinations?

In examining the basic combinations of source, line and load resistances, and typical waveforms characteristic of each case, advantageous combinations can be determined. The primary results are tabulated in *Figure 3-15*. Those combinations generally used in voltage mode communications circuits are as follows.

1. Unterminated case ($R_S \ll R_0$, $R_L \gg R_0$). This situation provides low steady state power dissipation and large signal levels, but also shows pronounced "ringing" effects. The "ringing" can be reduced by controlling signal rise/fall time versus τ, or by clamping diodes to limit load signal excursions. This case is representative of TTL circuits and is thus widely employed.

2. The parallel terminated case ($R_S \ll R_0$, $R_L = R_0$) provides large signal levels, and excellent signal fidelity. However, it is power consuming with most of that power dissipated in the load resistor. This case is useful for cleaning up the reflection effects of Case 1 but, at the same time, does require a driver circuit to have its internal current limits set at greater values than those required to produce the desired signal level into the minimum line resistance used. Thus, this case requires power buffer gates such as the 9N40 or 9S140 or specific line driver devices such as the 9612, 9614 9621 or 8T13/23. Ordinary TTL, except for the above mentioned circuits, has too low a current limit point to adequately drive 50 Ω lines.

3. The series terminated or backmatched driver case $R_S = R_0$ $R_L \gg R_0$ provides a low steady state power dissipation system for use with one receiver located at the load end of the line. The positive reflection coefficient of the load is used to approximately double the initial wave arriving at the load. Setting $R_S = R_0$ terminates the reflected wave when it arrives back at the source site after two line delays, and the line then assumes steady state conditions. The use of other receivers located along the line is not recommended, because they will not see the full driver signal swing until the reflection from the load passes their particular

Configuration Name (if any)	(Driver) Source Resistance	(Receiver) Load Resistance	Signal Characteristics	Optimum Receiver Threshold	Line Receivers Allowed at Other Than Load End of Line?	Comments
Unterminated	$\ll R_0$	$\gg R_0$	Ringing pronounced	0.5 V_{SS}	Yes	Undershoot may cause data errors
Parallel terminated	$\ll R_0$	$= R_0$	Excellent fidelity	0.5 V_{SS}	Yes	Load resistor consumes power $P_L = \frac{(V_{SS})^2}{R_L}$
	$\ll R_0$	$\ll R_0$	Awful — different signals at each point on the line	NA	No	Not generally useful
Series terminated or backmatched driver	$= R_0$	$\gg R_0$	Load signal excellent	0.5 V_{SS}	No	Reduced power consumption over parallel termination
Fully matched	$= R_0$	$= R_0$	Excellent fidelity	0.25 V_{SS}	Yes	Greater tolerances on resistors allowed for same fidelity as parallel termination
	$= R_0$	$< R_0$	Load signal like a one-shot	NA	NA	Not generally useful for data, is useful as pulse generator
	$\gg R_0$	$\gg R_0$	Exponential like signal waveforms	0.5 V_{SS}	Yes	Low power comsumption. Increased delay due to signal 'rise' times
	$\gg R_0$	$= R_0$	Small signal amplitude. Excellent fidelity	0.5 V_{SS}	Yes	Produces only small signal voltages compared with other methods. Uses current sinking drivers such as the 75110A, 75112
	$\gg R_0$	$< R_0$	Very small signal amplitudes, also ringing	NA	NA	Not generally useful

Fig. 3-15. Summary of Effects

bridging points. Such receivers could malfunction, as they would see a voltage very close to their threshold, and perhaps even place the line receiver in its linear operating region. This could make the line receiver sensitive to oscillatory, parasitic feedback. If these contraints are acceptable, the series termination method can be used to good advantage in providing the same signal fidelity and signal amplitude as with the parallel termination method, while at the same time, contributing a significant savings in steady state power consumption.

4. The fully matched case $R_S = R_0$, $R_L = R_0$ not only provides excellent signal fidelity all along the line, but also has reduced signal amplitude over that of the parallel terminated case. Additionally, the power consumption is somewhat less than the parallel termination case and the power is divided equally by the source and load. The primary advantage of the fully matched system is that termination resistor tolerances can be relaxed somewhat without incurring large amounts of ringing. This is because both the source and load act as line terminations.

EFFECT OF SOURCE RISE TIME ON WAVEFORMS

Previously, it was assumed that the source-produced signal rise time was always much less than the line time delay (τ). Because the waveforms for the source and load voltage were the superposition of incident and reflected waves occurring at their proper times, and because the shape of each wave was a square edged step function, the resultant source and load waveforms were thus also square edged, or *ideal* in nature. In many practical cases, particularly when line length is short, the source excitation possesses a finite, and non-negligible, rise time. Therefore, depending on the ratio of rise time to line delay, it is possible to have a new wave start arriving at the point of interest *before* the previous wave can reach its final value. The net waveform for voltage or current at that point, then, would consist of the superposition of two or more waves during their time of overlap. To study the superposition effect on signal waveforms, the source excitation is represented as a simple linear ramp rise to its final value of V_{O+}, so

$$e(t) = 0 \text{ for } t < 0$$
$$e(t) = V_{O+} \cdot t/t_r \text{ for } 0 \leq t \leq t_r$$

and

$$e(t) = V_{O+} \text{ for } t > t_r$$

where t_r represents the 0-to-100% source rise time. The circuit model and its lattice diagram are shown in *Figure 3-16*. The values of R_S, R_0 and R_L were chosen to equal those of an actual circuit on hand, allowing the theoretical waveforms, obtained by graphical superposition, to be compared with the measured response of an actual circuit.

Figure 3-17 shows the load voltage v_L, source voltage v_S and source current i_S waveforms versus time for a circuit with a source rise time very much less than τ . The actual waveforms for v_L, v_S and i_S are composed of the superposition of both incident and reflected waves in their proper time sequence. In the figures, these waves are shown as dotted lines. Each wave represents the sum of the incident wave plus its reflection. The resultant v_L, v_S and i_S waveforms (shown as solid lines) are the superposition of the waves represented by the dotted lines. With the exception of a slight rounding of the edges, the actual waveforms for the circuit, shown in the oscilloscope photograph in *Figure 3-17*, closely approximate the waveforms predicted by theory.

If the source excitation is adjusted so that its 0-to-100% rise time t_r is equal to 2τ , each of the $v_i + v_r$ and $i_i + i_r$ waveforms must be modified to include this rise time. The waves will have the same final value as predicted by the lattice diagram, but they now require two line time delays to reach this final value. The v_L, v_S and i_S waveforms consist of the superposition of these linear ramps. Because each wave reaches its final value just as a new wave arrives, their superposition converts the square edged v_L, v_S and i_S waveforms into triangular waveforms. This is shown in *Figure 3-18*. The accompanying oscilloscope photograph shows the close correspondence between the actual and theoretical waveforms whereas an additional oscilloscope photograph in *Figure 3-18* shows the actual waveforms for the case where $t_r = \tau$. Not surprisingly, the $t_r = \tau$ case changes the v_L, v_S and i_S waveforms of the $t_r \ll \tau$ case into trapezoidal forms because each arriving wave reaches its final value well before a new wave arrives.

If the source excitation is adjusted such that its rise time equals three line delays $t_r = 3\tau$, the $v_i + v_r$ and $i_i + i_r$ waves overlap for a period of time equal to τ . That is, each wave reaches only 2/3 of its final value when a new wave starts arriving. Considering the waveform, the load voltage from time τ to 3 τ is

$$v_i(1)\ (1 + \rho_L)\ e\ (t - \tau).$$

Starting at $t = 3\tau$, the wave

$$v_i(3) = v_i(1)\rho_S\rho_L\ e(t - 3\tau).$$

begins arriving from the source, and the load voltage then is the superposition of these two waves. Because $v_i(3)$ is a negative wave ($\rho_S < 0$), the algebraic sum of the last third of the first wave and the first third of the second wave $v_i(3)$ arriving at the load causes the load voltage to reduce in amplitude from the ($t_r \ll \tau$) case. Likewise, the source voltage and source current show reduced amplitudes over the ideal case, due to the overlap period of the waves arriving at the source.

Theoretical and actual waveforms for the $t_r = 3\tau$ case are shown in *Figure 3-19*. Notice that load voltage perturbations and source current i_S requirements are reduced from those of the $t_r \ll \tau$ case. Similarly, the ratio of t_r to τ , can be successively increased. This results in reduced ringing on the load voltage and reduced source current due to the overlapping of more and more $v_i + v_r$ (or $i_i + i_r$) waves. Actual and theoretical waveforms for t_r equal to 4τ , 6τ and 8τ are shown in *Figures 3-20, 3-21* and *3-22,* respectively. In each case, as the t_r to τ ratio is increased, the instantaneous source and load voltages become more equal. The source current is also reduced so that the circuit exhibits fewer reflection effects and the transmission line itself can be considered as a simple interconnection from dc circuit theory.

Using the t_r: τ ratio to reduce reflection effects has many practical advantages in digital design. The low source and high input resistance of TTL or ECL circuits allows one gate to drive many receiving gates. The reflection effects of this unterminated combination, however, can cause data errors or at least lead to reduced noise immunity due to the pronounced load voltage undershoot. Since the rise and fall times of these devices are easily measured, a maximum line length can be set such that the resulting t_r to τ ratio provides the desired reduction in ringing. This is the primary basis for the wiring rules of each logic family and, usually, the t_r to τ ratio is chosen somewhere between 3:1 and 4:1. As an example, the rise and fall time for normal TTL (9N/74N series) is $t_{10\%-90\%}$ = 6 ns. When this is converted to an equivalent linear 0 to 100% time, t_r = 8 ns. A common propagation delay of 1.7 ns/ft, in combination with the requirement that $t_r = 3\tau$, gives the maximum line length of approximately 18 inches. This corresponds with the published recommendation of the various manufacturers for the 9N/74N series TTL circuits. A similar computation of the rise and fall times for other logic families yields their respective line length recommendations. The faster families require shorter line lengths for the same t_r to τ ratio, and slower logic families allow relatively longer line length. This ratio can also be used to make stubs or taps on lines "disappear". In other words, if the stub's time delay is made very short when compared to the t_r of the signal at the stub line location, the stub reflections will have a minimal effect on the line signals. A stub length to generate a t_r: τ ratio of greater than 8:1 is usually considered adequate to negate the stub reflections.

The third primary application of the t_r to τ ratio for controlling reflection effects is that used in some standard data communications interfaces such as EIA-RS232-C. Here, driver slew rate is explicitly controlled. This, along with the implied maximum interconnect cable length serves to produce a t_r: τ ratio of 3:1 or greater. This, in turn, reduces the reflection effects inherent in a voltage source driver, unterminated line system. The main disadvantage of using the t_r: τ ratio to control reflection effects is in the overall time for the signal representing the data to rise above the receiver threshold level. With the parallel terminated method, the minimum time delay was τ or one line delay. When the t_r: τ ratio is used, an additional delay time of approximately 0.5 t_r is added to the line delay yielding, therefore, a greater effective signal propagation delay. This increased delay may or may not be acceptable in the desired system so the trade-off between ease of usage of the unterminated case must be weighed against the increased effective signal delay over that delay obtainable with the terminated case.

Source t in (τ)	$v_i + v_r$ (V)	$i_i + i_r$ (mA)	v_S (V)	i_S (mA)	Load t in (τ)	$v_i + v_r$ (V)	$i_i + i_r$ (mA)	v_L (V)	i_L (mA)
0	0.9400	12.53	0.9400	12.53	1	1.8500	0.40	1.8500	0.40
2	0.1224	-22.64	1.0624	-10.10	3	-1.5500	-0.34	0.3000	0.06
4	-0.1026	18.97	0.9599	8.87	5	1.2986	0.28	1.5986	0.35
6	0.0859	-15.90	1.0458	- 7.03	7	-1.0881	-0.24	0.5106	0.11
8	-0.0720	13.32	0.9738	6.29	9	0.9116	0.20	1.4222	0.31
10	0.0603	-11.17	1.0341	- 4.87	11	-0.7638	-0.17	0.6584	0.14
12	-0.0505	9.36	0.9836	4.48	13	0.6399	0.14	1.2983	0.28
14	0.0424	- 7.84	1.0259	- 3.36	15	-0.5362	-0.12	0.7622	0.16
16	0.0355	6.57	0.9904	3.21	17	0.4492	0.10	1.2114	0.26

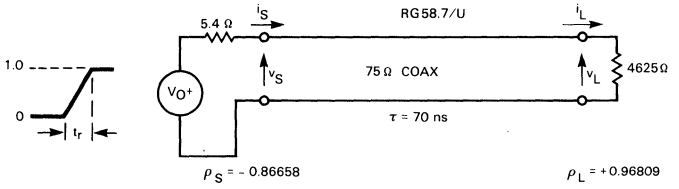
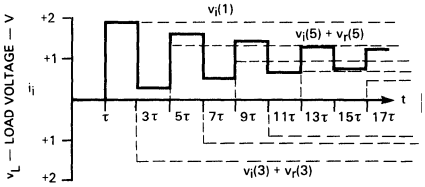
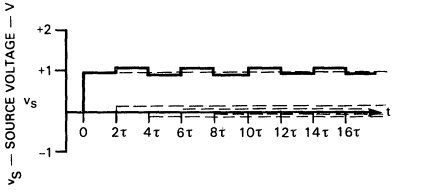


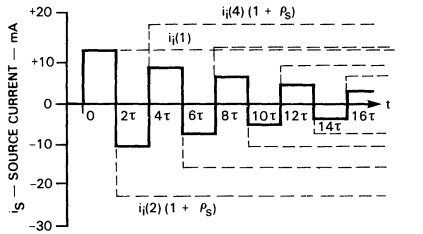
Fig. 3-16. Transmission Line Model and Its Lattice Diagram



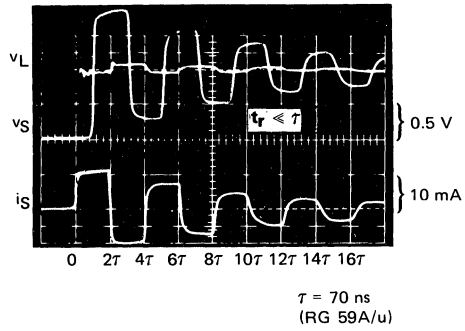
DOTTED LINES ARE $v_i(n)(1 + \rho_S)$ WAVES ARRIVING AT LOAD—THEIR SUM IS THE LOAD VOLTAGE $v_L(t)$ (SOLID LINE)



SOME WAVES OMITTED FOR CLARITY

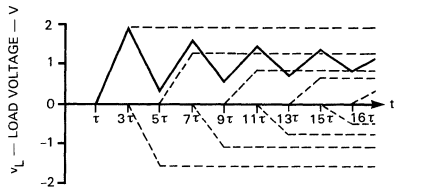


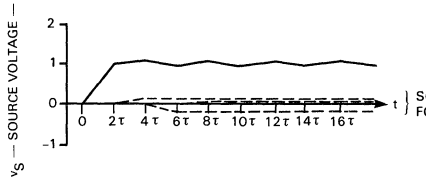
DOTTED LINES ARE $i_i(n)(1 + \rho_S)$ WAVES AT SOURCE. THEIR SUM IS THE SOURCE CURRENT INTO THE LINE $i_S(t)$ (SOLID LINE)



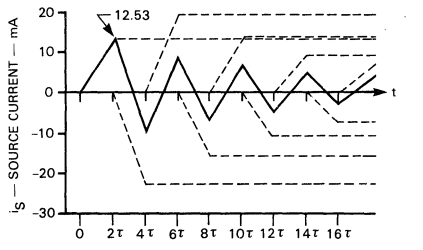
τ = 70 ns
(RG 59A/u)

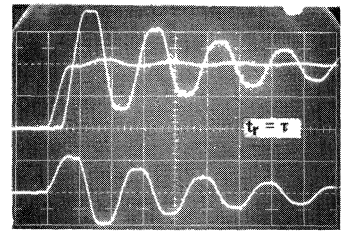
Fig. 3-17. Waveforms for $t_r = 2 \ll \tau$





SOME WAVES OMITTED FOR CLARITY





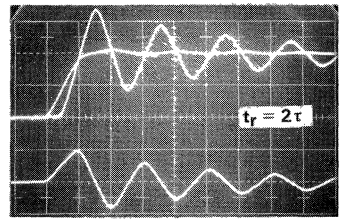
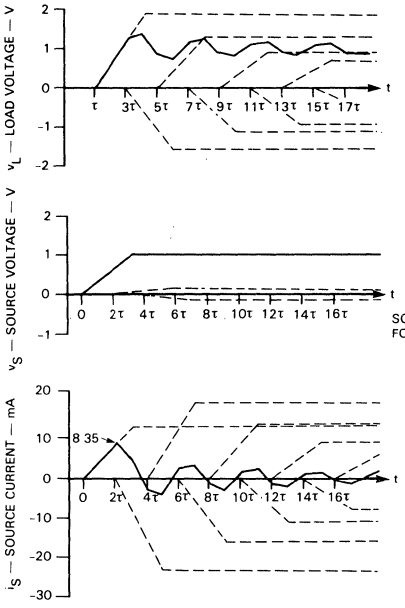


Fig. 3-18. Waveforms for $t_r = 2\tau$



SOME WAVES OMITTED FOR CLARITY

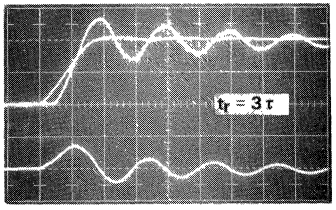
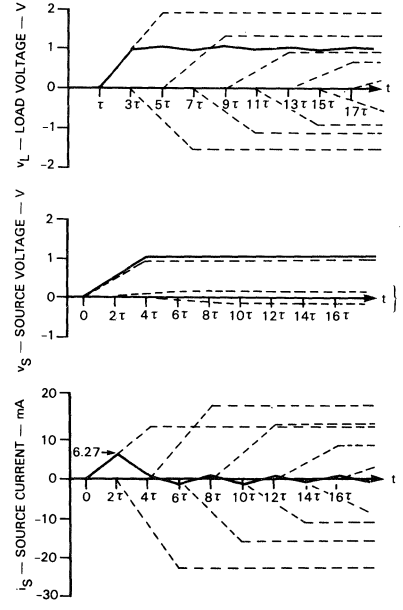


Fig. 3-19. Waveforms for $t_r = 3\tau$



SOME WAVES OMITTED FOR CLARITY

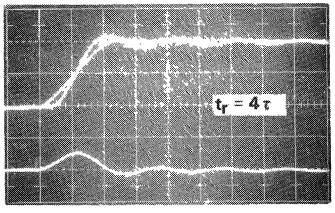
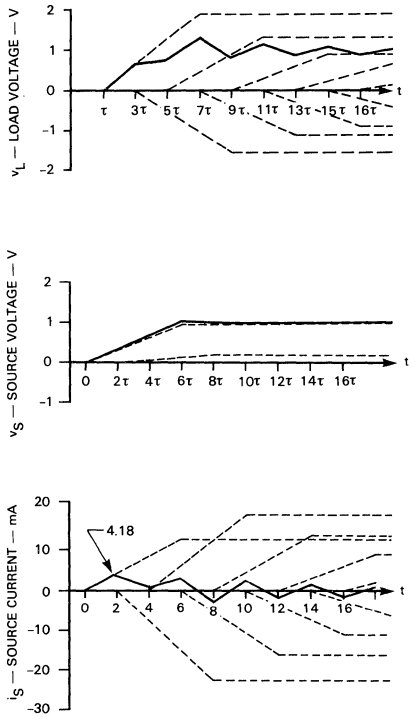


Fig. 3-20. Waveforms for $t_r = 4\tau$



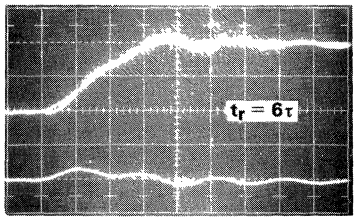
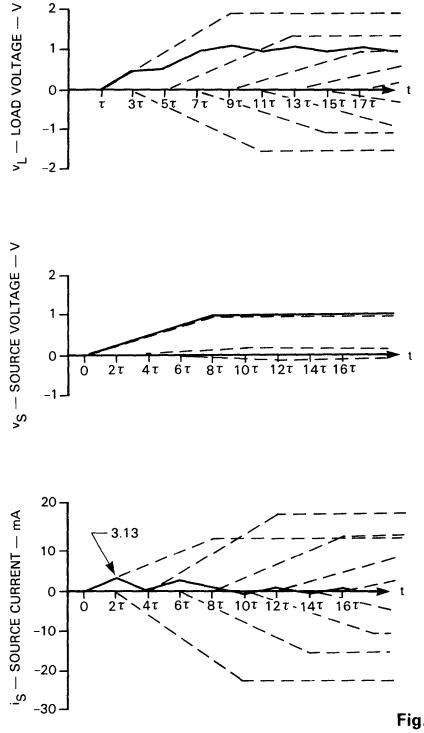


Fig. 3.21. Waveforms for $t_r = 6\tau$



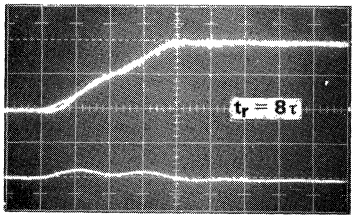


Fig. 3-22. Waveforms for $t_r = 8\tau$

Section 4

LONG TRANSMISSION LINES AND DATA SIGNAL QUALITY

INTRODUCTION

Transmission lines throughout previous chapters have always been treated as ideal lossless lines. As a consequence of this simplified model, the signals passing along the lines did not change in shape, but were only delayed in time. This time delay is given as the product of per-unit-length delay and line length ($\tau = l\delta$). Unfortunately, real transmission lines always possess some finite resistance per unit length due to the resistance of the conductors composing the line. So, the lossless model only represents *short* lines where this resistance term can be neglected. In section 2, the per-unit-length line parameters, L, R, C, G, were assumed to be both constant and independent of frequency (up to the limits mentioned, of course). But with real lines, this is not strictly correct as four effects alter the per-unit-length parameters, making some of them frequency dependent. These four effects are skin effect, proximity effect, radiation loss effect, and dielectric loss effect. These effects and how they influence the intrinsic line parameters are discussed later in this section. Since these effects make simple ac analysis virtually impossible, operational (Laplace) calculus is usually applied to various simplified line models to provide somewhat constrained analytical solutions to line voltages and currents. These analytical solutions are difficult to derive, perhaps even more difficult to evaluate, and their accuracy of prediction depends greatly on line model accuracy. Analytical solutions for various lines (primarily coaxial cables) appear in the references, so only the salient results are examined here.

Engineers designing data transmission circuits are not usually interested in the esoterica of lossy transmission line theory. Instead, they are concerned with the following question: given a line length of x feet and a data rate of n bps, does the system work — and if so — what amount of transition jitter is expected? To answer this question using analytical methods is quite difficult because evaluation of the expressions representing the line voltage or current as a function of position and time is an involved process. The references at the end of this section provide a starting point to generate and evaluate analytical expressions for a given cable.

The effects on the LRCG line parameters, the variations in Z_0, $\alpha(\omega)$, and propagation velocity as a function of applied frequency are discussed later in this section. Using an empirical approach to answer the "how far — how fast" question involves only easily made laboratory measurements on that selected cable. This empirical approach, using the binary eye pattern as the primary measurement tool, enables the construction of a graph showing the line length/data rate/signal quality trade-offs for a particular cable. The terms describing *signal quality* are discussed later in this section. The technique of using actual measurements from cables rather than theoretical predictions is not as subject to error as the analytical approach. The only difficulties in the empirical method are the requirements for a high quality, real time (or random sampling) oscilloscope and, of course, the requisite amount of transmission line to be tested.

Also discussed in this chapter are commonly used pulse codes and ways to estimate coaxial cable signal quality in lieu of eye pattern measurements.

FACTORS CAUSING SIGNAL WAVE SHAPE CHANGES

In the previous sections it was assumed that the transmission lines were ideal so the step functions propagated along the lines without any change in wave shape. Because a single pulse is actually composed of a continuous (Fourier) spectrum, the phase velocity independence on an applied frequency, and the absence of attenuation (R = 0, G = 0) of the ideal line always allows the linear addition of these frequency components to reconstruct the original signal without alteration. For real lines, unfortunately, the series resistance is not quite zero, and the phase velocity is slightly dependent on the applied frequency. The latter results in *dispersion; i.e.,* the propagation velocity will differ for the various frequencies, while the former results in signal *attenuation* (reduction in amplitude). This attenuation may also be a function of frequency. Attenuation and dispersion cause the frequency components of a signal, at some point down the line, to be quite different from the frequency components of the signal applied to the input of the line. Thus, at some point down the line, the frequency components add together to produce a wave shape that may differ significantly from the input signal wave shape. In many ways, then, a real transmission line may be thought of as a distributed lowpass filter with loss. The fast rise and fall times of the signals become progressively "rounded" due to attenuation and dispersion of the high frequency signal components.

It should be noted that there is a theoretical condition where attenuation is independent of frequency and dispersion is zero. This results in a line causing signal amplitude reduction, but no change in signal wave shape. This condition was first discussed by Heavyside and is called the *distortionless* line. To make a line distortionless, the primary line parameters must satisfy the relation $(R/L)=(G/C)$. Because for real lines $(R/L) > (G/C)$, the distortionless line is only of historical interest, and it is not possible to satisfy the $(R/L)=(G/C)$ condition over a sufficiently wide bandwidth to allow a proper transmission of short duration pulses. Over a limited frequency range such as that encountered in telephony (0-4 kHz), the L term can be increased by either adding lumped inductances at fixed intervals along the line or by winding a magnetic material (as a thin tape) around the conductors of the line throughout its length. Lumped loading is commonly applied to long telephone circuits to reduce the signal attenuation over a narrow frequency range; however this linearity is at the expense of in-band attenuation and non-linear delay distortion. The distributed loading method has been tried, but the mechanical characteristics of the magnetic materials have made the winding process very difficult. In any event, neither method allows short pulses to retain their wave shapes. The interest in line loading to produce the Heavyside condition for pulse transmission is therefore largely academic.

The following sections discuss the origins of the second-order effects—skin effect, proximity effect, radiation loss effect, and dielectric loss effect—and their influence on the LRCG transmission line parameters.

- Skin Effect: This phenomenon is based on two facts: a current flow in any real conductor produces an electric field given by Ohm's Law; the current distribution and/

or magnetic field distribution in a conductor is frequency dependent. For dc current in a single isolated conductor, the current density is uniform across the conductor. When alternating current is used, the current density is not uniform across the conductor. Instead, the current tends to concentrate on the conductor surface. Current density continuously increases from the conductor center to its surface, but for practical purposes, the current *penetration depth*, d, is assumed as a dividing line for current density. The current is assumed to flow in a imaginary cylinder of thickness d with a constant current density throughout the cylinder thickness. Distribution of current densities for both actual and assumed models is shown in *Figure 4-1.*

It can be seen that for *classical* skin effects, the penetration depth is given by

$$d = K\frac{1}{\sqrt{f}} \qquad (4.1)$$

where $K=1/\sqrt{\pi\mu\sigma}$, μ = magnetic permeability of the conducting material expressed in henries per unit length, and σ = conductivity of the conducting material. For MKS(SI) units and for a copper conductor

$$\sigma = 5.85 \times 10^{7} \ (\Omega \ meter)^{-1}$$
$$\mu = 4\pi \times 10^{-7} \ (H/meter)$$

in which case, d would be the penetration depth expressed in meters.

Because the skin effect reduces the equivalent conductor cross-sectional area, increasing frequencies cause an increase in the effective resistance per unit length of the line. This in turn leads to signal attenuation increasing with frequency. If the frequency response of a cable is plotted on log-log graph paper, log dB, or Nepers vs log frequency, the curve slope will be 0.5 if the cable losses are primarily governed by *classical* skin effects. The slope of the attenuation curve, along with the attenuation at a particular frequency, can be used to estimate coaxial cable transient response as a function of length.[2,4]

- Proximity Effect: This is a current density redistribution in a conductor due to the mutual repulsion (or attraction) generated by currents flowing in nearby conductors. The current density at those points on the conductor close to neighboring conductors varies from the current density when the conductor is isolated from other conductors. This current density redistribution reduces the effective cross-sectional area of the conductor, thereby increasing the per-unit-length line resistance. This effect is a function of the conductor diameters, the separation of the conductors from each other, and frequency. The analytical evaluation of the proximity effect is quite complicated and except for certain limited cases (see Arnold[11] and Dwight[12]), no general rule of thumb expressions have been proposed. The proximity effect is not present in coaxial cables because of their circular symmetry. The proximity effect is a significant contributor to signal losses particularly in cases of a twisted pair or parallel wire lines.

- Radiation Loss: Radiation losses cause an apparent rise in resistance per unit length increasing with frequency. The mechanism of radiation loss is energy dissipation either as heat or magnetization via eddy currents in nearby metallic or magnetic masses, with the eddy currents induced by line currents. Coaxial cables do not exhibit this effect because the signal magnetic field is confined between the shield and the outside of the center conductor. Ideally, the magnetic field produced by shield current cancels the field produced by current in the center conductor (for points outside the shield).

  Both twisted pair and parallel wire lines exhibit radiation losses and these losses contribute to the effective per-unit-length line resistance. Radiation loss is dependent to a large extent on the characteristics of the materials close to the line; so radiation loss is quite difficult to calculate, but can be measured if necessary.

- Dielectric Loss Effect: Dielectric losses result from leakage currents through the dielectric material. This causes an increase in the shunt conductance per unit length and produces signal attenuation. Fortunately, for most dielectric materials in common use, this loss is very small particularly for frequencies below 250 MHz. For most practical purposes, then, dielectric losses may be neglected as they are usually overshadowed by skin effect losses.

INFLUENCE OF LOSS EFFECTS ON PRIMARY LINE PARAMETERS

Resistance Per Unit Length, R. It is composed of a basic dc resistance term R_{dc} plus the contributions of skin effect, proximity effect and radiation loss effect. For coaxial lines, the proximity and radiation loss effects are negligible in most

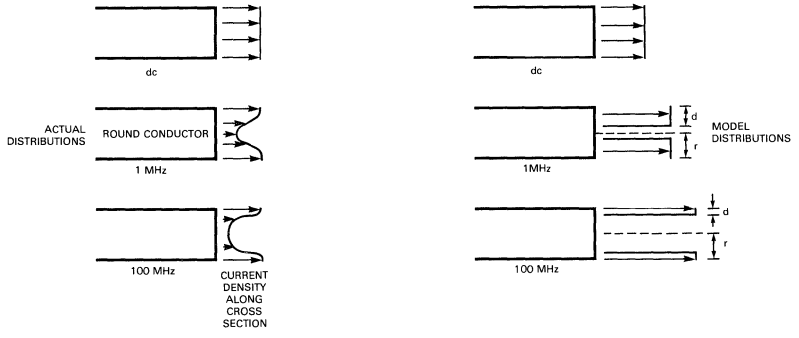


Fig. 4-1. Current Distributions Across and Conductor for Several Frequencies

cases, so the primary contribution is made by the skin effect. Thus the resistance per unit length becomes

$$R = R_{dc} + Ks^m \qquad (4.2)$$

where $0<m<1$.

For 2-wire lines (twisted pair, parallel wire), the resistance per unit length is increased by the skin effect. For closely spaced wires, however, the proximity effect also contributes significantly to a resistance increase. Radiation loss should also be included, but is very difficult to calculate because it depends on the surroundings of the line.

Inductance Per Unit Length, L. It can be shown[5,6] that, as the frequency is increased, the skin effect, proximity effect, and radiation loss effect cause a reduction in the effective per-unit-length self-inductance of the line.

Capacitance Per Unit Length, C. This depends primarily on the dielectric constant of the insulating medium and conductor geometry. This term is constant over a wide range of frequencies for most dielectrics (Teflon®, Polyethylene). For Polyvinylchloride (PVC) insulation, the relative dielectric constant shows a decrease as frequency increases ($\epsilon_r \approx 4.7$ @ 1 kHz, $\epsilon_r \approx 2.9$ @ 100 MHz). The capacitance per unit length, therefore, will show a decrease corresponding with increasing frequency for PVC insulation and little change for most other dielectrics.

Conductance Per Unit Length, G. Because resistance per unit length usually has a much greater magnitude, this value is negligible. When this term cannot be neglected, it is represented as

$$G = \omega C \tan\phi \qquad (4.3)$$

where C is capacitance per unit length, ϕ is the angular frequency ($=2\ \pi f$) and tan ϕ is a dielectric material coefficient. The angle ϕ is called the dielectric loss angle. This angle is usually quite small ($<.005$ radians) for the majority of dielectrics up to several hundred megahertz.

VARIATIONS IN Z_0, α (ω), AND PROPAGATION VELOCITY

The variations in the primary line parameters as a function of frequency shown by *Figure 4-2* have a profound influence on the three secondary line parameters of characteristic impedance, attenuation, and velocity of propagation.

In the expression for the characteristic impedance of a line,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

at low frequencies, $j\omega L$ is small compared to R, and G is small compared to $j\omega C$. So the characteristic impedance is $\sqrt{R/j\omega C}$. At high frequencies, the increase in R is overshadowed by $j\omega L$ even though L is being reduced. With G still much smaller than $j\omega C$, the characteristic impedance is almost a pure resistance $R_0 = \sqrt{L/C}$. The behavior of the characteristic impedance as a function of frequency ($Z_0 = R_0 - jX_0$) is shown in *Figure 4-3*.

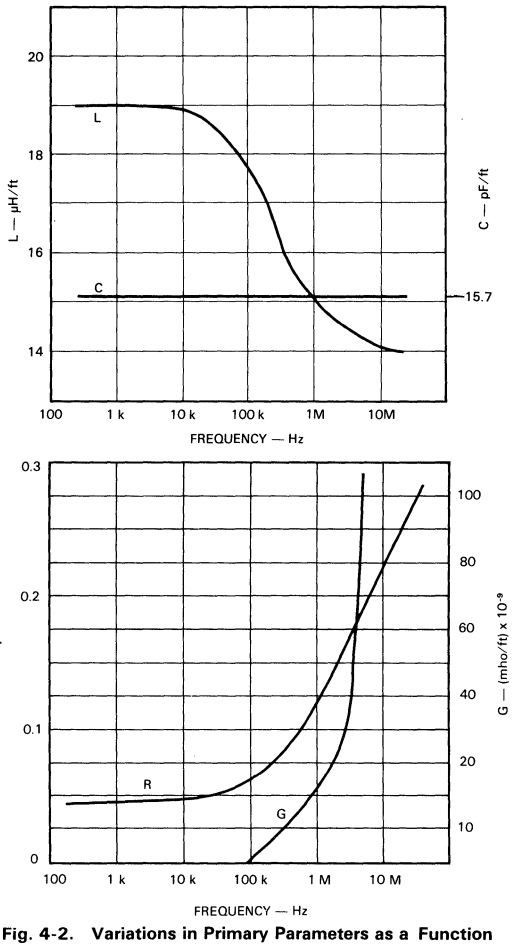


Fig. 4-2. Variations in Primary Parameters as a Function of Frequency (22 AWG Polyethylene Insulated Twisted Pair)

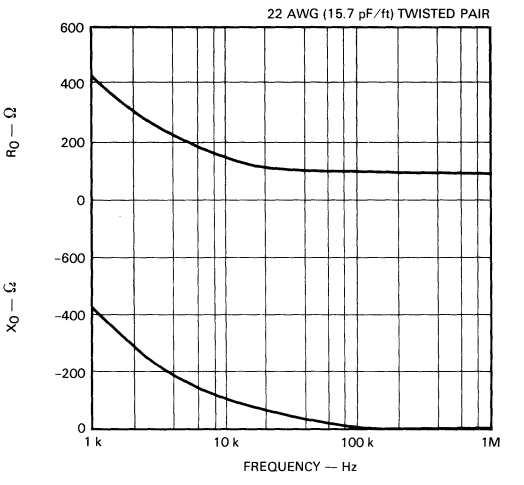


Fig. 4-3. Typical Variation in Z_0 as a Function of Frequencies

®Teflon is a registered trademark of E.I. du Pont de Nemours Company.

Typical behavior of the line attenuation as a function of frequency is shown in *Figure 4-4*. This line attenuation is the real part of the equation

$$\gamma(\omega) = \sqrt{(R + j\omega L)(G + j\omega C)}\,.$$

The change in resistance is the primary contributor to the attenuation increase as a function of frequency. For coaxial cables, this resistance increase is due primarily to the skin effect ($R_{SK} = Kf^m$). The slope of the attenuation curve on a log-log graph (log dB vs log frequency), therefore, is essentially linear and, at the same time, equal to m. For twisted pair and parallel wire lines, proximity effects and radiation losses make the curves less linear, but for high frequencies (over 100 kHz), the attenuation expressed in nepers per unit length is approximated by

$$\alpha \simeq \frac{R}{2}\sqrt{\frac{C}{L}} \qquad (4.4)$$

The R term is, of course, the sum of the dc resistance, plus the incremental resistance due to skin, proximity and radiation loss effects. This R term usually varies as follows.

$$R_{SK} = Kf^m$$

where $0.6 \leq m < 1.0$

The signal velocity propagation ($v = \omega/\beta$) is given by the imaginary part of the propagation constant γ. As shown in Section 3, v is a constant given by $v = \sqrt{LC}$ for lossless lines. For real lines, this value is approached at high frequencies. At low frequencies, however, (when ω is small compared to R/L or G/C), then $v_{LF} \simeq (C/2)\sqrt{R/G}$ and the velocity is reduced. The propagation velocity as a function of frequency is shown in *Figure 4-5*. This variation in signal velocity as a function of signal frequency is *dispersion* which was previously discussed.

The signal at a point down the line represents the sum of that original signal's Fourier spectrum. Because both the attenuation and propagation velocity of these Fourier components increase with frequency, the resultant signal shape at that point down the line depends greatly on the winners of the race to get to that point. The high frequency components, with their faster propagation velocities, arrive first, but the increased attenuation minimizes their effect. The low frequency signals arrive later, but the reduced attenuation allows them a greater influence on the resultant signal. In general, the output signal from the line should show a relatively fast rise up to some signal value (20 to 50% of the final value). This is due to arrival of the high frequency components, followed by a more leisurely rise to the final value as the slower, low frequency components arrive.

SIGNAL QUALITY — TERMS

Before the concepts presented in the previous sections can be used to answer the "how far—how fast" question, some familiarity with the terms describing data and signal quality is necessary.

The primary objective of data transmission is the transfer of *information* from one location to another. The information here is *digital* in nature; *i.e.,* a finite number of separate states or choices. This is in contrast to *analog* which has an infinite number of separate states or a continuous range of choices. The digital information is *binary* or two-valued; thus two different, recognizable electrical states/levels are used to symbolize the digital information. A binary symbol is commonly called a binary-digit or *bit*. A single binary sumbol or bit, by itself, can represent only one of two possible things. To represent alphabetic or numeric characters, a group of bits is arranged to provide the necessary number of unique combinations. This arrangement of bits which is then considered an information unit is called a *byte*. In the same manner that a group of bits can be called a byte, a collection of bytes, considered as a unit, is called a *word*. Selective arrangement of seven bits will provide 2^7 (or 128) distinct character combinations (unique bytes). The American Standard Code for Information Interchange (ASCII) is an excellent example of just such an arrangement—upper and lower case alphabetic, zero to nine numeric, punctuation marks, and miscellaneous information-code control functions.

Now with the means for representing information as bits or bytes, and the means for transmission of the bits (symbols) from one location to another (transmission line), the remain-

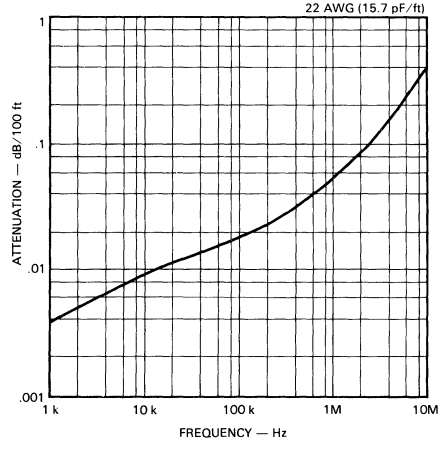


Fig. 4-4. Attenuation vs Frequency

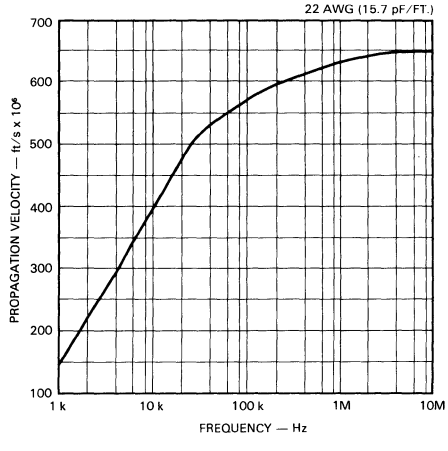


Fig. 4-5. Propagation Velocity vs Frequency

ing task is to ensure that a particular bit arriving at its destination is interpreted in the proper context. To achieve this, both the sender and receiver of the data must accomplish the five following requirements.

1. Agree upon the nominal rate of transmission; or how many bits are to be emitted per second by the sender.

2. Agree upon a specified information code providing a one-to-one mapping ratio of information-to-bit pattern and vice versa.

3. Establish a particular scheme whereby each bit can be properly positioned within a byte by the receiver of the data (assuming that bit-serial transmission is used).

4. Define the protocol (handshaking) sequences necessary to ensure an orderly flow of information.

5. Agree to the electrical states representing the logic values of each bit and the particular pulse code to be used.

These are by no means all of the points that must be agreed upon by sender and receiver—but these are probably the most important. Items 2, 3 and 4 are more or less "software" type decisions, because the actual signal flow along the transmission line is usually independent of these decisions. Because items 1 and 5 are much more dependent on the characteristics of line drivers, line receivers, and transmission lines, they are the primary concern here.

Figure 4-6 represents the components of a typical data transmission system. The *information source* can be a computer terminal or a digitized transducer outout, or any device emitting a stream of bits at the rate of one bit every t_B seconds. This establishes the *information rate* of the system at $1/t_B$ bits per second. The information source in the figure feeds a *source encoder* which performs logic operations not only on the data, but also on the associated clock and, perhaps, the past data bits. Thus, the source encoder produces a binary data stream controlling the *line driver*. The line driver interfaces the source internal logic levels (TTL, MOS, etc.) with transmission line current/voltage requirements. The transmission line conveys signals produced by the line driver to the line receiver. The line receiver makes a decision on the signal logic state by comparing the received signal to a decision threshold level, and the *sink decoder* performs logic operations on the binary bit stream recovered by the line receiver. For example, the sink decoder may extract the clock rate from the data or perhaps detect and correct errors in the data. From the optional sink decoder, the recovered binary data passes to the *information sink*—the destination for the information source data.

Assume for the moment that the source encoder and sink decoder are "transparent"; that is, they will not modify the binary data presented to them in any way. Line driver signals, then, have the same timing as the original bit stream. The data source emits a new bit every t_B seconds. The *pulse code* produced by the source encoder and line driver is called Non-Return to Zero (NRZ), a very common signal in TTL logic systems. A sample bit pattern with its NRZ representation is shown in *Figure 4-7a*. The arrows at the top represent the *ideal instants*, or the times the signal can change state. The term *unit interval* is used to express the time duration of the shortest signaling element. The shortest signaling element for NRZ data is one bit time t_B, so the unit interval for NRZ data is also t_B. The rate at which the signal changes is the *modulation rate* (or signaling speed), and *baud* is the unit of modulation rate. A modulation rate of one baud corresponds to the transmission of one unit interval per second. Thus the modulation rate, in baud, is just the reciprocal of the time for one unit interval. A unit interval of 20 ms, therefore, means the signaling speed is 50 baud. The reason for differentiating between the *information rate* in bits per second (bps) and the *modulation rate* in baud will be clarified after examining some of the other pulse codes later in this chapter.

NRZ data should always be accompanied by a clock signal, *Figure 4-7b*, which tells the receiver when to sample the data signal and thus determine the current logic state. For the example in *Figure 4-7b*, the falling edge of the clock corresponds to the middle of the data bits, so it could be used to transfer the line receiver data output into a binary latch. The falling edge of the clock is thus the *sampling instant* for the data. The line receiver does have a *decision threshold* or slicing point so that voltages above that threshold level produce one logic state output, while voltages below the threshold produce the other logic state at the receiver output. The receiver may incorporate positive feedback to produce *hysteresis* in its transfer function. This reduces the possibility of oscillation in response to slow rise or fall time signals applied to the receiver inputs.

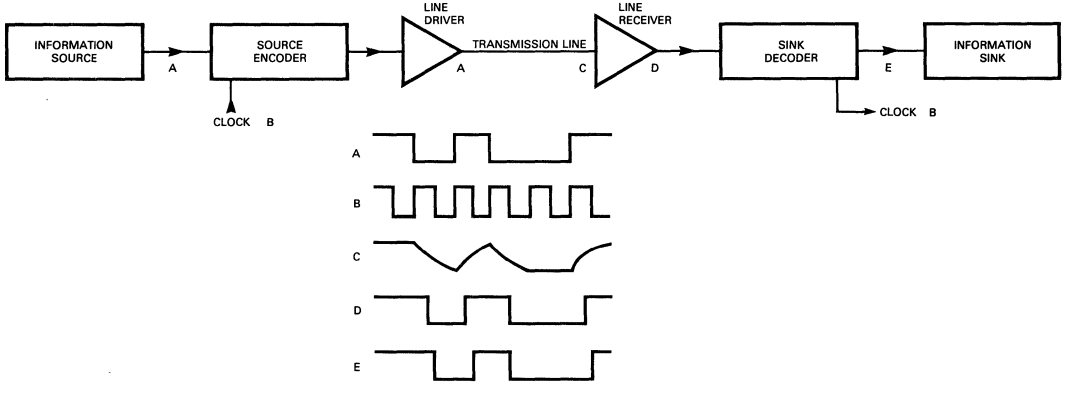


Fig. 4-6. Data Transmission System

Previously in this chapter, it was stated that the fast rise and fall times of signals, corresponding to the transitions between data bits, are rounded out and slowed down by a real transmission line. Each transition of the signal applied to the line by the line driver is transformed to a rounded out transition by the dispersion and attenuation of the transmission line. The resultant signal at the load end of the line consists of the superposition of these transformed transitions. The waves arriving at the load end of the line are shown in *Figure 4-7c* and their superposition is shown in *Figure 4-7d*. It is assumed that the line is terminated in its characteristic resistance so that reflections are not present. The receiver threshold level is shown here, superimposed on the resultant load signal, and the re-converted data output of the line receiver is shown in *Figure 4-7e* along with the ideal instants for the data transitions (tick marks).

Comparing the original data *(Figure 4-7a)* to the recovered data *(Figure 4-7e)* shows that the actual recovered data transitions may be displaced from their ideal instants (tic marks on *Figure 4-7e*). This time displacement of the transitions is due to a new wave arriving at the receiver site before the previous wave has reached its final value. Since the wave representing a previous data bit is *interfering* with the wave representing the present data bit, this phenomenon is called *intersymbol interference* (in telegraphy it is called *characteristic distortion*). The intersymbol interference can be reduced to zero by making the unit interval of the data signal quite long in comparison to the rise/fall time of the signal at the receiver site. This can be accomplished by either reducing the modulation rate for a given line length, or by reducing the line length for a given modulation rate.

Signal quality is concerned with the variance between the ideal instants of the original data signal and the actual transition times for the recovered data signal.

For synchronous signaling, such as NRZ data, the *isochronous distortion* of the recovered data is the ratio of the unit interval to the maximum measured difference irrespective of sign between the actual and theoretical significant instants. The isochronous distortion is, then, the peak-to-peak time jitter of the data signal expressed as a percentage of the unit interval. A 25% isochronous distortion means that the peak-to-peak time jitter of the transition is .25 unit interval (max).

Another type of received-signal time distortion can occur if the decision threshold point is misplaced from its optimum value. If the receiver threshold is shifted up toward the *One signal level*, then the time duration of the One bits shortens with respect to the duration of the *Zero bits*, and vice versa. This is called *bias distortion* in telegraphy and can be due to receiver threshold offset (bias) and/or asymmetrical output levels of the driver. This effects is shown in *Figure 4-8*.

Bias distortion and characteristic distortion (intersymbol interference) together are called *systemic distortion*, because their magnitudes are determined by characteristics within the data transmission system. Another variety of time distortion is called *fortuitous distortion* and is due to factors outside the data transmission system such as noise and crosstalk, which may occur randomly with respect to the signal timing.

SIGNAL QUALITY MEASUREMENT—THE EYE PATTERN

To examine the relative effects of intersymbol interference on random NRZ data and a "dotting"* pattern, see *Figure 4-9*. The top two waveforms represent the NRZ data and dotting pattern as outputs into two identical long transmission lines. The middle two traces illustrate the resultant signals at the line outputs and the bottom two traces show the data output of the line receivers. The respective thresholds are shown as dotted lines on the middle two traces. The arrows indicate the ideal instants for both data and dotting signals.

Notice that the dotting signal (D) is symmetrical, *i.e.*, every One is preceded by a Zero and vice versa, while the NRZ data is random. The resultant dotting signal out of the line is also symmetrical. Because, in this case, the dotting half-cycle time is less than the rise/fall time of the line, the resultant signal out of the line (E) is a *partial response*—it never reach-

*The term dotting pattern is from telegraphy and means an alternating sequence of 1-bits and 0-bits (the "dot dot dot" etc.). Note that an NRZ dotting pattern generates a signal which has a 50% duty cycle and a frequency of $1/2\ t_B$ (Hz).

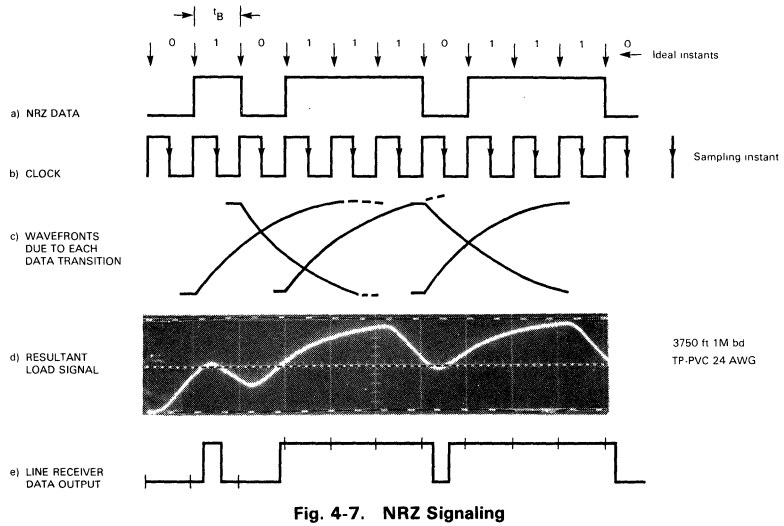


Fig. 4-7. NRZ Signaling

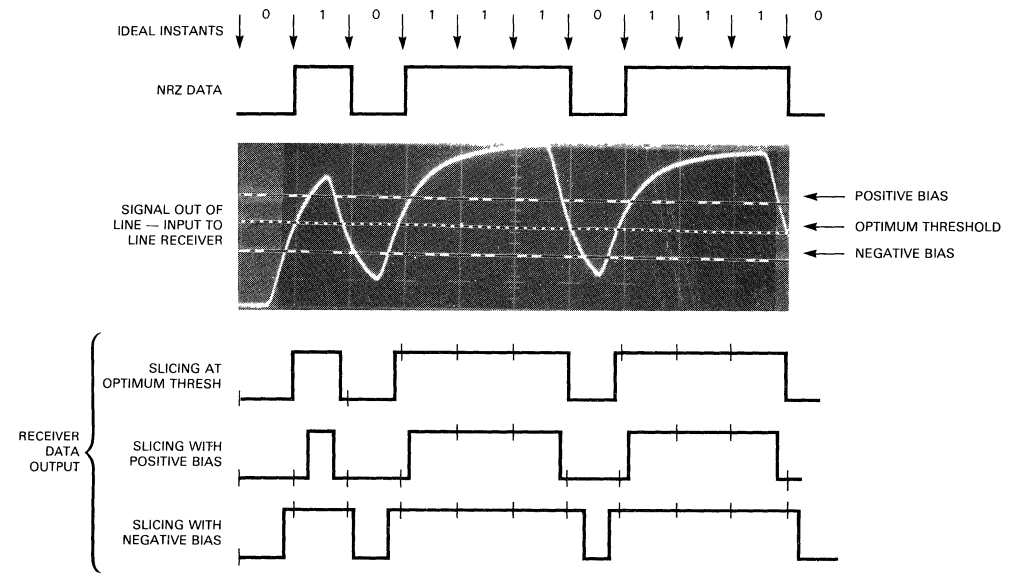


Fig. 4-8. Bias Distortion

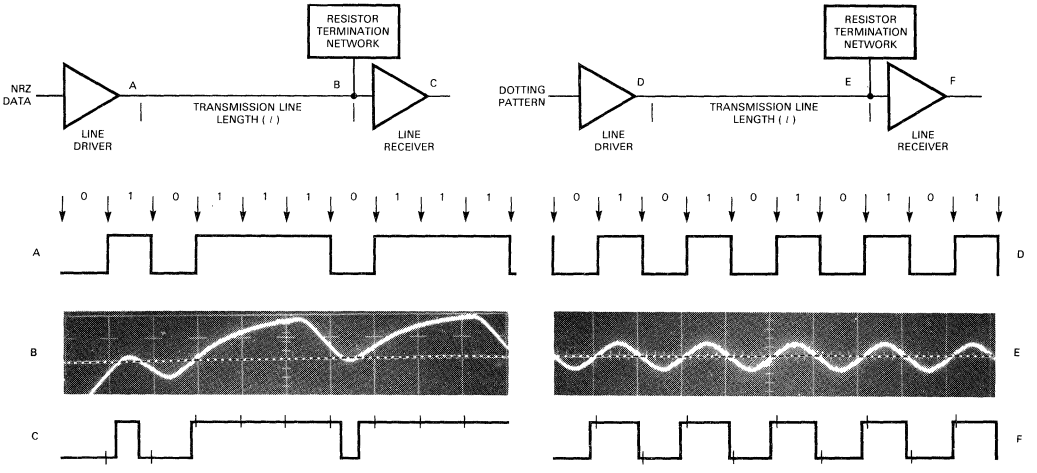


Fig. 4-9. Comparison of NRZ Random Data and "Dotting" Signals

es its final level before changing. The dotting signal, due to its symmetry, does not show intersymbol interference in the same way that a random NRZ signal does. The intersymbol interference in the dotting signal shows up as a uniform displacement of the transitions as shown in *Figure 4-9f*. The NRZ data shows intersymbol interference, in its worst light, due to its unpredictable bit sequence. Thus, whenever feasibility of a data transmission system is to be tested, a random data sequence should be used. This is because a symmetrical dotting pattern or clock signal cannot always show the effects of possible intersymbol interference.

A very effective method of measuring time distortion through a data transmission system is based on the eye pattern. The eye pattern, displayed on an oscilloscope, is simply the superposition—over one unit interval—of all the Zero-to-One and One-to-Zero transitions, each preceded and followed by various combinations of One and Zero, and also constant One

and Zero levels. The name *eye pattern* comes from the resemblance of the open pattern center to an eye. The diagramatic construction of an eye pattern is shown in *Figure 4-10*. The data sequence can be generated by a pseudo-random sequence generator (PRSG), which is a digital shift register with feedback connected to produce a maximum length sequence. The PRSG, requiring only two devices *(Figure 4-11)*, generates a sequence that repeats after 2^{20}-1 bits. Feedback connections for PRSG shift registers from 4 to 20 bits in length are shown in *Figure 4-12*.

Several features of the eye pattern make it a useful tool for measuring data signal quality. *Figure 4-13* shows a typical binary eye pattern for NRZ data. The spread of traces crossing the receiver threshold level (dotted line) is a direct measure of the peak-to-peak transition jitter—isochronous distor-

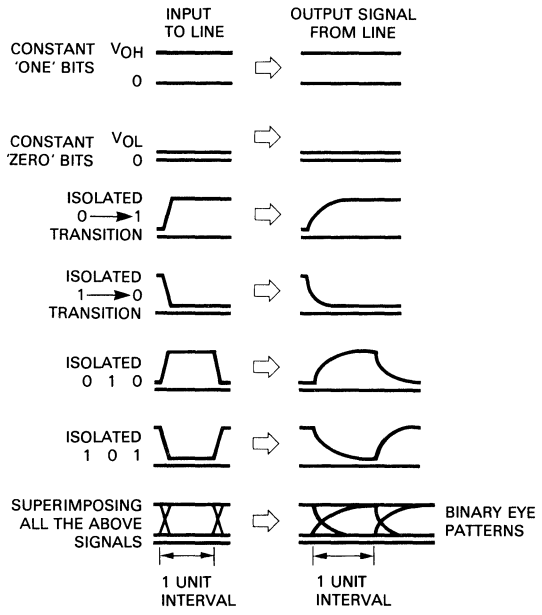


Fig. 4-10. Formation of an Eye Pattern by Superposition

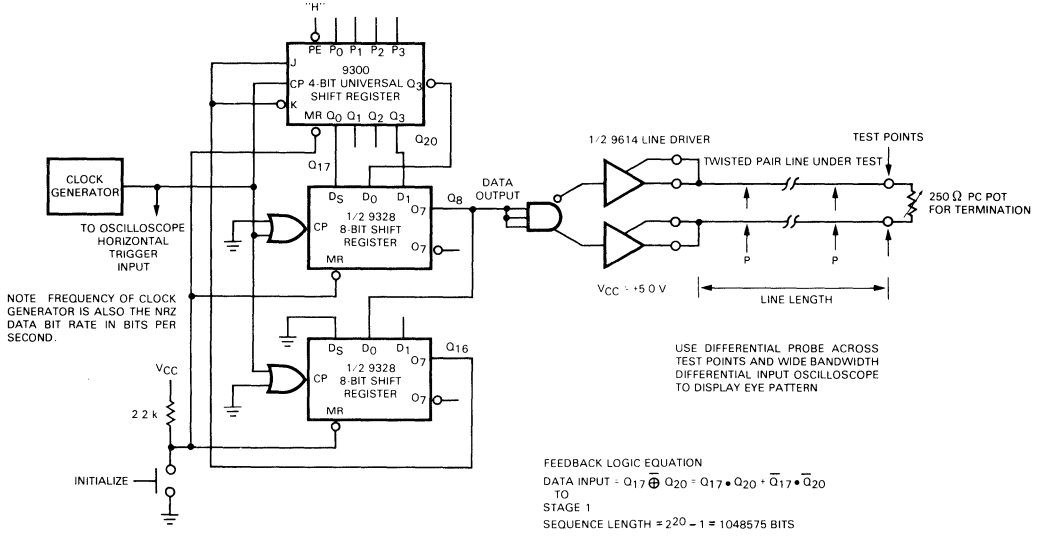
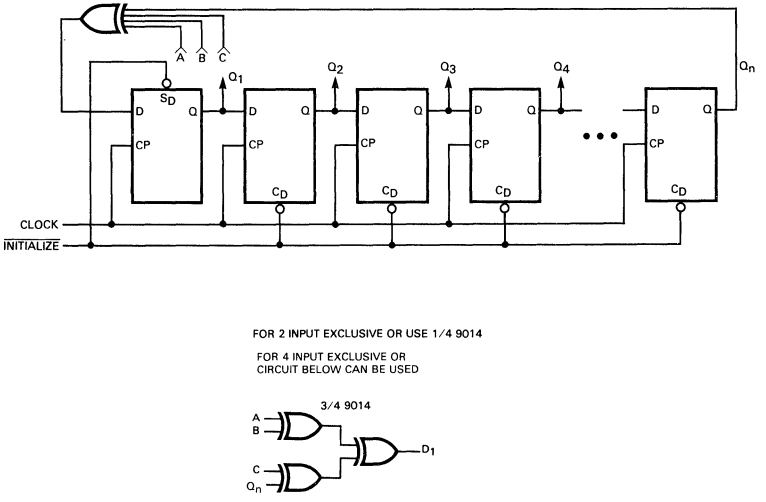


Fig. 4-11. Bench Set-up to Measure Data Signal Quality

tion in a synchronous system—of the data signal. The rise and fall time of the signal can be conveniently measured by using the built-in 0% and 100% references produced by long strings of Zeros and Ones. The height of the trace above or below the receiver threshold level at the sampling instant is the noise margin of the system. If no clear transition-free space in the eye pattern exists, the eye is closed. This indicates that error-free data transmission is not possible at that data rate and line length with that particular transmission line without re-sorting to equalizing techniques. In some extreme cases, error-free data recovery may not be possible even when using equalizing techniques.

The eye pattern can also be used to find the characteristic resistance of a transmission line. The 250 Ω printed circuit-type potentiometer termination resistor *(Figure 4-11)* can be adjusted to yield the minimum overshoot and undershoot of the data signal. *Figure 4-14* shows the NRZ data eye patterns for $R_T > R_O$, $R_T = R_O$ and $R_T < R_O$. The 100% and 0% reference levels are again provided by long strings of Ones and Zeros, and any overshoot or undershoot is easily discernible. The termination resistor is adjusted so that the eye pattern transitions exhibit the minimum perturbations *(Figure 4-14b)*. The resistor is then removed from the transmission line, and its measured value is the characteristic resistance of the line.

By using the eye pattern to measure signal quality at the load end of a given line, a graph can be constructed showing the tradeoffs in signal quality—peak-to-peak jitter—as a function of line length and modulation rate for a specific pulse code. An example graph for NRZ data is shown in *Figure 4-15*. The graph was constructed using eye pattern measurements on a 24 AWG twisted pair line (PVC insulation) driven by a differential voltage source driver (9614) with the line parallel-terminated in its characteristic resistance (96 Ω). The oscilloscope photographs in *Figure 4-16* show the typical eye patterns for NRZ data with various amounts of isochronous distortion. The straight lines represent a "best fit" to the actual measurement points. Since the twisted pair line used was not specifically constructed for pulse service, the graph



Number of Stages, n	Connections A	B	C	Sequence Length, bits
3	Q_2	L	L	7
4	Q_3	L	L	15
5	Q_4	L	L	31
6	Q_5	L	L	63
7	Q_6	L	L	127
8	Q_2	Q_3	Q_4	255
9	Q_5	L	L	511
10	Q_7	L	L	1023
11	Q_9	L	L	2047
12	Q_2	Q_{10}	Q_{11}	4095
13	Q_1	Q_{11}	Q_{12}	8191
14	Q_2	Q_{12}	Q_{13}	16383
15	Q_{14}	L	L	32767
16	Q_{11}	Q_{13}	Q_{14}	65535
17	Q_{14}	L	L	131071
18	Q_{11}	L	L	262143
19	Q_{14}	Q_{17}	Q_{19}	524287
20	Q_{17}	L	L	1048575

Fig. 4-12. Feedback Connection for Various Maximal Sequence Length PRSG

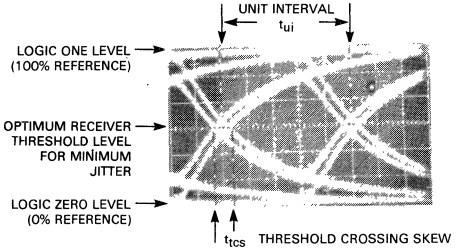


Fig. 4-13. NRZ Data Eye Pattern

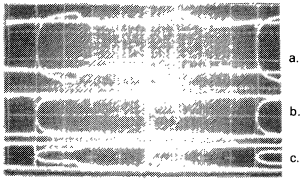


Fig. 4-14. Using Eye Pattern to Determine Characteristic Resistance of Line

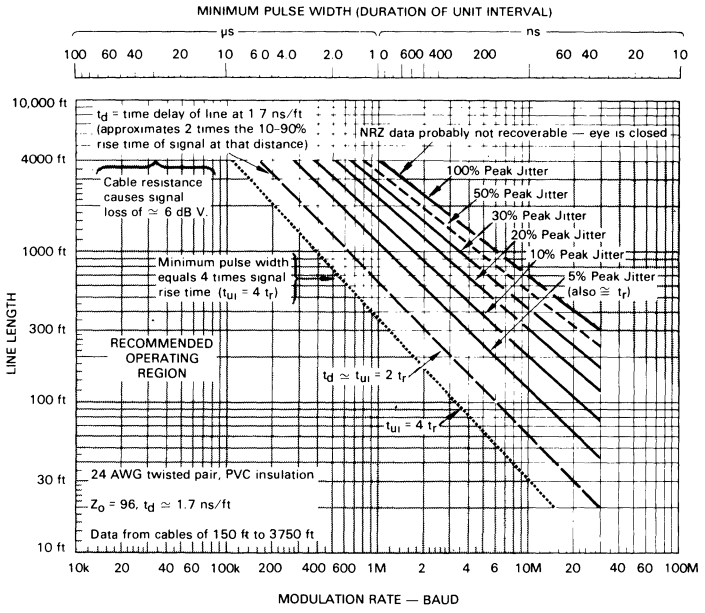


Fig. 4-15. Signal Quality as a Function of Line Length and Modulation Rate for Terminated 24 AWG Twisted Pair (PVC Insulation)

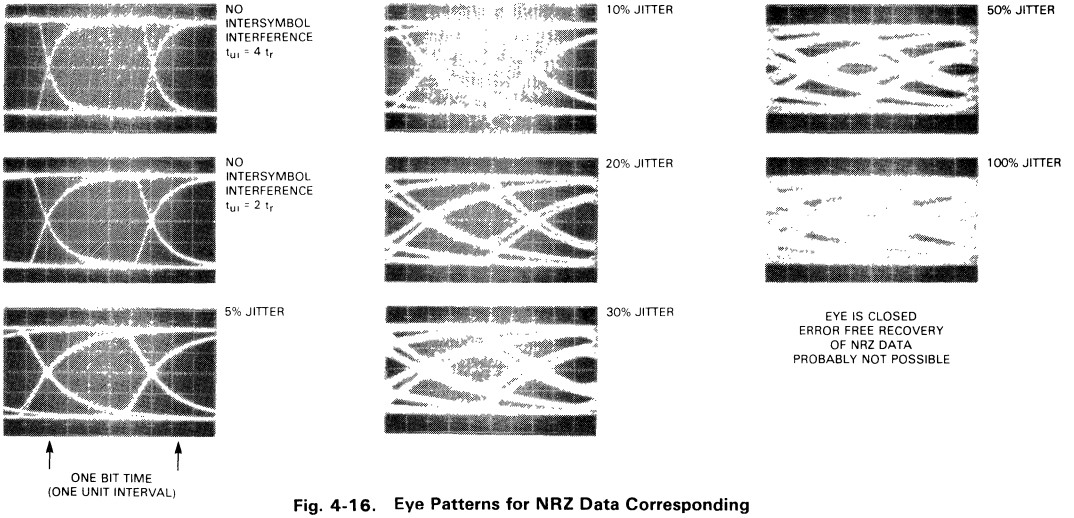


Fig. 4-16. Eye Patterns for NRZ Data Corresponding to Various Peak-to-Peak Transition Jitter

probably represents a reasonably good worst-case condition insofar as signal quality vs line length is concerned. Twisted pair lines with polyethylene or Teflon® insulation have shown better performance at a given length than the polyvinyl chloride insulation. Likewise, larger conductors (20 AWG, 22 AWG) also provide better performance at a given length. Thus, the graph in *Figure 4-15* can be used to estimate feasibility of a data transmission system when the actual cable to be used is unavailable for measurement purposes. The arbitrary cutoff of 4000 feet on the graph was due to an observed signal amplitude loss of 6 dBV (1/2 voltage) of the 24 AWG line at that distance. The cutoff of 10 Mbaud is based on the propagation delays of the typical TTL line drivers and receivers. Field experience has shown that twisted pair transmission systems using TTL drivers and receivers have operated essentially error-free when the line length and modulation rate are kept to within the shaded recommended operating region shown in *Figure 4-15*. This has not precluded operation outisde this region for some systems, but these systems must be carefully designed with particular attention paid to defining the required characteristics of the line, the driver, and the receiver devices. The use of coaxial cable instead of twisted pair lines almost always yields better performance, *i.e.,* greater modulation rate at a given line length

and signal quality. This is because most coaxial cable has a wider bandwidth and reduced attenuation at a given length than twisted pair line (one notable exception is RG 174/U cable). In the next section, a method is discussed that allows a rough estimation of the maximum "safe" modulation rate for a given length of a particular coaxial cable when actual eye pattern measurements cannot be made on that cable.

It should be remembered that, in some ways, the eye pattern gives the *minimum* peak-to-peak transition jitter for a given line length, type, pulse code, and modulation rate. This is because the eye pattern transition spread is the result of intersymbol interference and reflection effects (if present) and this minimum jitter is only obtainable if the following conditions are met.

- The One and Zero signal levels produced by the line driver are symmetrical, and the line receiver's decision threshold (for NRZ signaling) is set to coincide with the mean of those two levels.
- The line is perfectly terminated in its characteristic resistance to prevent reflections from altering the signal threshold crossings.
- The time delays through driver and receiver devices for both logic states is symmetrical and there is no relative skew in the delays (difference between L→H and H→L propagation delays = 0). This is especially important when the device propagation delays become significant fractions of the unit interval for the applicable modulation rate.

If any one of these conditions is not satisfied, the signal quality is reduced (more distortion). The effects of receiver bias or threshold ambiguity and driver offset can be determined by location of the decision threshold(s) on the oscillograph of the eye pattern for that driver/cable modulation rate combination. For eye patterns displaying more than 20% isochronous distortion, the slope of the signal in the transition region is relatively small. Therefore, a small amount of bias results in a large increase in net isochronous distortion. See *Figure 4-17* for a graphic illustration of this effect. In the interest of conservative design practices, systems should always be designed with less than 5% transition spread in the eye pattern. This allows the detrimental effects due to bias to be minimized, thus simplifying construction of line drivers and receivers.

ESTIMATION OF SIGNAL QUALITY IN LIEU OF EYE PATTERN MEASUREMENTS

In many design situations it is not always convenient to measure signal quality using the eye pattern. This can be caused by lack of equipment, time, or unavailability of the transmission line to perform the necessary measurements. In such cases, the following rule of thumb applies: the unit interval should be greater than twice the 10 to 90% rise or fall time of the line, *i.e.,*

$$t_{ui} \geq 2t_{10\text{-}90\%}$$

Eye patterns that meet this criterion show that adherence to this rule will keep the peak-to-peak jitter to less than 5% of the unit interval. If the 10% to 90% rise time cannot be easily measured—as is the case with coaxial cables whose dominant loss mechanism is simple skin effect—then the 10 to 80% rise time may be used instead of the 10 to 90% rise time. The corresponding peak-to-peak jitter, due to intersymbol interference with the $t_{ui} \geq 2\ t_{10\text{-}80\%}$ rule, is usually less than 10%. In any event, if the unit interval is less than the 0 to 50% rise time of the signal at the line end ($t_{ui} < t_{0\text{-}50\%}$), then the error-free recovery of NRZ data is not possible without using equalizing techniques. Sometimes, changing to a pulse code which allows partial response recovery will enable data transmission at an otherwise unusable line length-speed combination. When actual eye pattern measurements cannot be made, an estimate of feasibility can still be obtained by calculating the signal transition time.

N.S. Nahman[2,4] presented a simple method to predict the transient response of a coaxial cable from the cable attenuation. The procedure was based on a graphical analysis technique allowing prediction of the step response of a network from a graph of the imaginary part of the transfer function, in this case the imaginary part of γ (s). The normalized step responses *(Figure 4-18)* are plotted with the abscissa in normalized time (x)

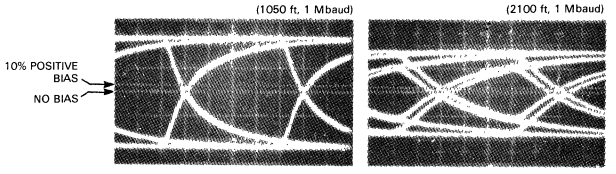
$$x = t/a \tag{4.5}$$

where

$$a = \frac{1}{2\pi f_0}\left[\frac{\alpha(f_0)}{\cos(m\pi/2)}\right]^{\frac{1}{m}} \tag{4.6}$$

and

t = real time,



BIAS	1050 ft	2100 ft
0%	5% ID	20% ID
10%	12% ID	36% ID

Fig. 4-17. Receiver Bias Effect on Total Isochronous Distortion

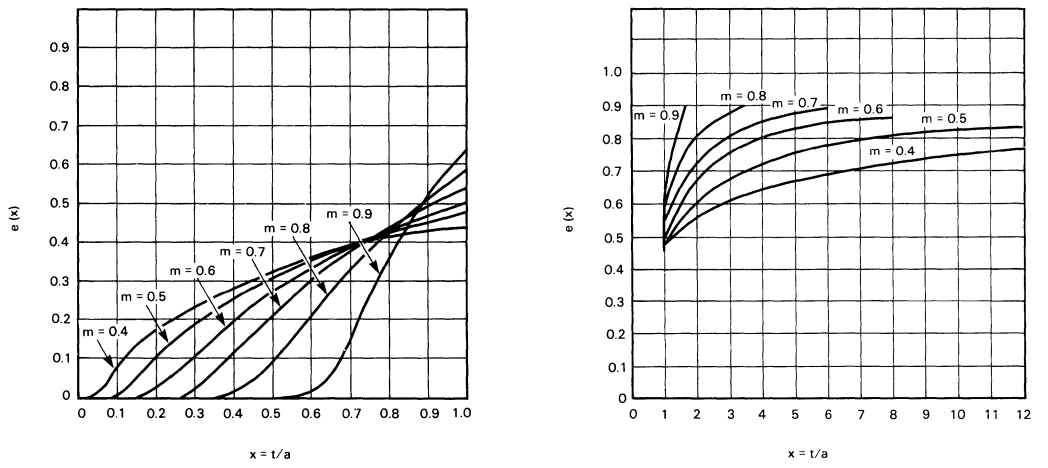


Fig. 4-18. Normalized Step Responses for f^m Law Coaxial Cables (After Nahman[2])

$\alpha(f_0)$ = attenuation of the coaxial cable in nepers at frequency (f_0) for length l. If $\alpha(f_0)$ is known in dB, then division by 8.686 will convert the dB/length into nepers/length (1 neper = 8.686 dB).

m = slope of the attenuation vs frequency curve for the particular coaxial cable when plotted on log-log graph paper (log dB vs log frequency).

$$m = \frac{\log \alpha(f_2) - \log \alpha(f_1)}{\log (f_2) - \log (f_1)}$$

where $f_2 > f_1$ and $\alpha(f_2)$ is the attenuation at frequency (f_2), and log is the common (base 10) logarithm.

Slope m will have a range of $0<m<1$.

Nahman pointed out that this method applies to cables where either the attenuation *or* the phase characteristic can specify the transfer function. This implies that knowledge of either characteristic alone provides sufficient information for the other characteristic; in particular, the Bode condition must be met.

$$\lim_{s\to\infty} \frac{\gamma(s)}{s} = 0$$

For details, see Nahman's paper[2]. In general, a reasonably accurate modified transfer function may be specified satisfying Bode's condition for coaxial cables. Twisted pair and parallel wire lines cannot usually be fully characterized by either attenuation or phase characteristics alone. This is because each has a significant contribution to the overall transfer function. Thus Bode's condition cannot usually be met, so Nahman's method will not yield accurate results.

In a more recent paper[4], he asserted that the primary contributors to the shape of the step response waveform are those frequency components transmitted with less than 20 dB of attenuation. Thus, the predominant slope of the attenuation curve up to 20 dB at that cable length should be used. For short cables (1000 ft) the 20 dB attenuation may occur in the 10 to 100 MHz region. *Equation 4.6* may be modified by factoring out the cable length to produce

$$a = \frac{1}{2\pi f_0}\left[\frac{\alpha_1(f_0)}{\cos(m\pi/2)}\right]^{\frac{1}{m}} \cdot \left[l\right]^{\frac{1}{m}} \qquad (4.7)$$

where $\alpha_1(f_0)$ is now the attenuation (in nepers per unit length and l is the line length. The time for the line signal to rise to 50% is obtained by combining *Equations 4.5* and *4.7 (Equations 5* and *7* in Reference 4).

$$t_{50\%} = \frac{x_{50\%}}{2\pi f_0}\left[\frac{\alpha_1(f_0)}{\cos(m\pi/2)}\right]^{\frac{1}{m}} \cdot \left[l\right]^{\frac{1}{m}} \qquad (4.8)$$

where $x_{50\%}$ is obtained from *Figure 4-18* or the table in *Figure 4-19*. Likewise, combining the expressions for $x_{10\%}$ and $x_{80\%}$ and subtracting gives

$$t_{10\text{-}80\%} = \frac{x_{80\%} - x_{10\%}}{2\pi f_0}\left[\frac{\alpha_1(f_0)}{\cos(m\pi/2)}\right]^{\frac{1}{m}} \cdot \left[l\right]^{\frac{1}{m}} \qquad (4.9)$$

The 10 to 90% rise time can be found similarly by substituting $x_{90\%}$ for $x_{80\%}$ in *Equation 4.9*.

As an example of the use of these equations to predict step response of a coaxial cable, consider RG59A/U cable. The listed attenuation for RG59A/U is[13]

f_0	$\alpha(f_0)$/100 ft (dB)
10 MHz	1.07
100 MHz	3.4
400 MHz	7.0

The slope of the attenuation curve is

$$m = \frac{\log 7.0 - \log 1.07}{\log (400 \times 10^6) - \log (10 \times 10^6)} = \frac{.82}{1.60} = 0.51$$

The attenuation per unit length (in nepers) at 400 MHz is

$$\alpha_1 (400\ MHz) = \frac{7.0}{8.686} \cdot \frac{1}{100\ ft.} = 0.008059\ nepers/ft$$

Thus, the normalization constant, a, is

m	$x_{50\%}$	$x_{10-90\%}$	$x_{10-80\%}$
0.4	1.30	*	14.5
0.5	1.15	*	7.1
0.6	1.00	*	3.5
0.7	0.92	6.6	2.4
0.8	0.89	3.0	1.4
0.9	0.89	1.0	0.7

*90% points not given on graph for these values (Figure 4²)

Fig. 4-19. Normalized Time to Reach Various Percentages of Signal Final Value for Various Values of m

$$a = \frac{1}{2\pi(400 \times 10^6)} \left[\frac{.008059}{\cos[(.51)\pi/2]}\right]^{\frac{1}{.51}} = 6.355 \times 10^{-14}$$

A 140-foot length of line, therefore, should have a $t_{50\%}$ time

$$t_{50\%} = (1.15)(6.355 \times 10^{-14})(140)^{\frac{1}{.51}} = 1.18 \text{ ns}$$

and the 10% to 80% rise time is

$$t_{10\text{-}80\%} = (7.1)(6.355 \times 10^{-14})(140)^{\frac{1}{.51}} = 7.29 \text{ ns}$$

For 1000 ft of RG59A/U, the previous results for 140 ft can be scaled.

$$t_{50\%} = 1.18 \cdot \left[\frac{1000}{140}\right]^{\frac{1}{.51}} = 55.7 \text{ ns}$$

and

$$t_{10\text{-}80\%} = 7.29 \cdot \left[\frac{1000}{140}\right]^{\frac{1}{.51}} = 344.2 \text{ ns}$$

If the desired modulation rate is 1 Mbaud (t_{ui} = 1.0 μs) and the line length is 1000 feet, then the system using RG59/U cable would probably operate satisfactorily. Be aware, however, that if the single slope (m) does not accurately approximate the actual attenuation characteristic of the coaxial cable, then Nahman's method will show considerable error in predicting the signal transition time. RG174/U is a coaxial cable with an attenuation characteristic that has a slope in the 0.3 to 0.65 range depending on the frequency. Thus the method cannot be accurately applied to RG174/U cable.

Also, Nahman's method cannot be applied to commonly available twisted pair or parallel wire lines. This is because knowledge of either the line attenuation or its phase characteristics is not normally sufficient to completely specify the transfer function. Thus, the previously mentioned Bode condition is not satisified, and the analysis previously used cannot be applied satisfactorily.

Experimental tests on various twisted pair cables from 10 to 4000 feet in length have revealed that these cables show a law of $m \simeq 0.6$ for attenuation, but follow an almost linear increase in rise time as cable length is increased. The 10 to 90% rise time usually falls in the following range.

$$\tau \leq t_{10\text{-}90\%} \leq 2\tau$$

where τ is the time delay of the cable per unit length times the cable length. Combining this with the suggestion that the unit interval should be at least twice the 10–90% rise time of the line, then the minimum unit interval should be

$$t_{ui} \geq 4\tau$$

This corresponds with a boundary for recommended operating regions shown in *Figure 4-15*. Experience has shown that adherence to the above relationship with twisted pair cables results in less than 10% peak-to-peak jitter due to intersymbol interference.

OTHER PULSE CODES AND SIGNAL QUALITY

In the preceding sections, the discussion of signal quality has been centered around the use of NRZ signaling, because it represents the simplest and most commonly used pulse code. Other pulse codes have been developed which provide one or more of the following desirable features:

- Compress the overall bandwidth normally required to adequately transmit the signal yet still ensure recovery of the binary data.
- Eliminate the need for a dc response in the transmission medium so that transformer coupling can be used for phantom power distribution on repeated lines. (The elimination of a dc characteristic of the pulse code also allows ac coupling of amplifier circuits).
- Provide a clocking scheme within the signal so that no separate clock channel is required for synchronization.
- Provide built-in error detection.

The following discussion is restricted to the binary class of baseband signals. This simply means that each decision by the line receiver yields one bit of information. The *M*-ary schemes ($M \geq 3$) can encode more than one bit of information per receiver decision*, but these schemes are seldom applied to baseband signaling due to the complexities of the driver and receiver circuits (especially for $M > 3$). M-ary schemes, however, are applied to high speed non-baseband data transmission systems using modems. The price to be paid for the increased bit-packing with multi-level signaling is decreased immunity to noise relative to a binary system. This is because a smaller relative threshold displacement (or amount of noise) is required to produce a signal representing another logic state in the *M*-ary schemes.

In general, the binary class of pulse codes can be grouped into four categories;

- Non-Return to Zero (NRZ)
- Return to Zero (RZ)

*It can be shown that, for *M* levels, the information per receiver decision will be $S = \log_2 M$ bits/decision. Thus, three levels theroetically yield 1.58 bits; four levels yield 2 bits of information, eight levels yield 3 bits. etc.

- Phase Encoded (PE) (sometimes called Split Phase)
- Multi-Level Binary (MLB). (The MLB scheme uses three levels to convey the binary data, but each decision by the line receiver yields only one bit of information.)

A secondary differentiation among the pulse codes is concerned with the algebraic signs of the signal levels. If the signal levels have the same algebraic sign for their voltages (or currents) and differ only in their magnitudes, the signaling is called *unipolar*. A very common example of unipolar signaling is TTL or ECL logic. TTL uses two positive voltages to represent its logic states, while ECL uses two negative voltages for its logic states. The complement of unipolar signaling is *polar* signaling. Here, one logic state is represented by a signal voltage or current having a positive sign and the other logic state is represented by a signal with a negative sign. For binary signals, the magnitude of both signals should be equal, ideally. Their only difference should be in the algebraic signs. This allows the receiver to use ground as its decision threshold reference.

Non-Return to Zero (NRZ) Pulse Codes

There are three NRZ pulse codes: NRZ – Level (NRZ-L), NRZ – Mark (NRZ-M), and NRZ – Space (NRZ-S). NRZ-L is the same pulse code as previously discussed. In NRZ-L signaling, data is represented by a constant signal level during the bit time interval, with one signal level corresponding to one logic state, and the other signal level corresponding to the opposite logic state. In NRZ-M or NRZ-S signaling, however, a change in signal level at the start of a bit interval corresponds to one logic state and no change in signal level at the start of a bit interval corresponds to the opposite logic state. For NRZ-M pulse codes, a change in signal level at the start of the bit interval indicates a logic One (Mark), while no change in signal level indicates a logic Zero (Space). NRZ-S is a logical complement to NRZ-M. A change in signal level means a logic Zero and no change means logic One. With NRZ-M and NRZ-S pulse codes, therefore, there is no direct correspondence between signal levels and logic states as there is with NRZ-L signaling. Any of the NRZ pulse codes may, of course, be used in unipolar or polar form. The NRZ codes are shown in *Figure 4-20*, along with their generation algorithms*, signal levels vs time, and their general power density spectrum.

The degradation in signal quality caused by intersymbol interference for NRZ-L signaling was discussed earlier. Since the minimum signaling element (unit interval) for all three NRZ pulse codes is equal to t_B, the previous signal quality discussion for NRZ-L also applies equally to NRZ-M and NRZ-S pulse codes. The following is a capsule summary of the previous discussion on NRZ signal quality.

*The generation algorithm showing the sequence of signal levels on the line, represented by the set $\{b_n\}$, is determined by the sequence of input logic states, represented by the set $\{a_n\}$. See Bennet[14] for detailed usage of this notation.

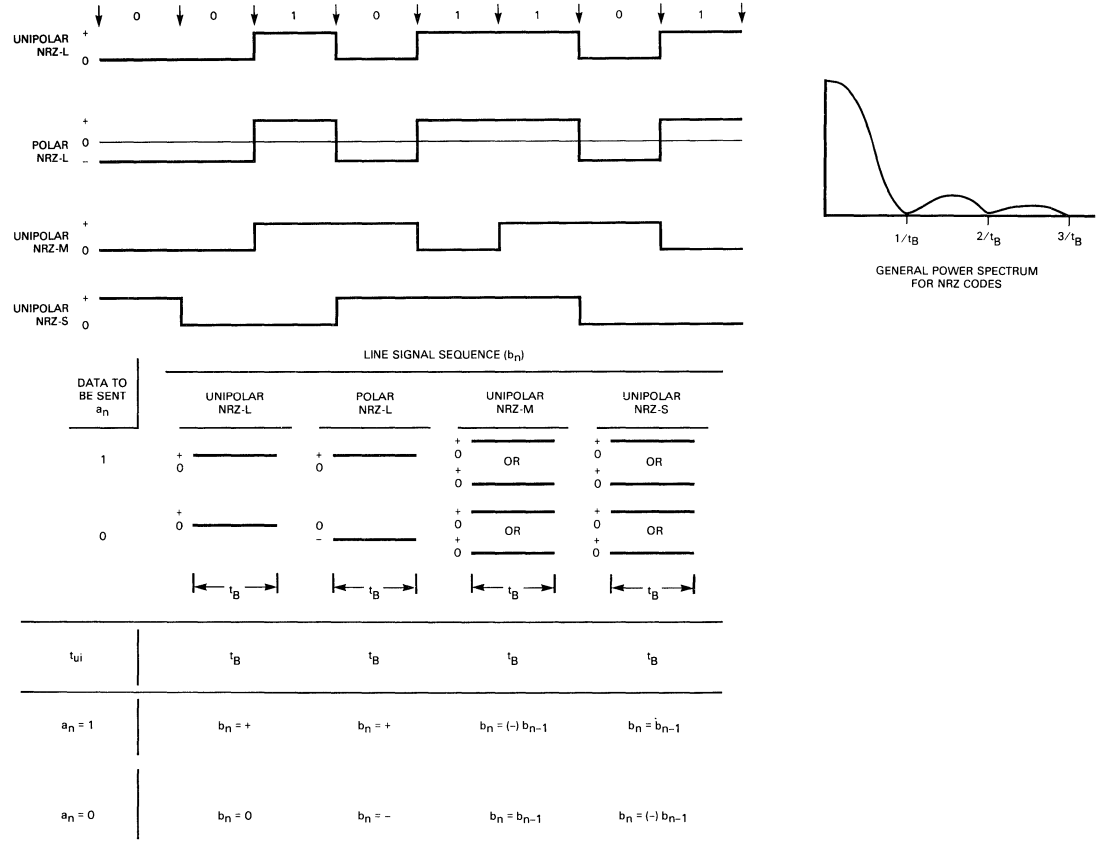


Fig. 4-20. Non-Return to Zero (NRZ) Pulse Codes

- When t_B is less than the 0–50% rise or fall time of the signal at the line end, the open space in the eye pattern closes, thereby indicating error-free data transmission is unlikely.
- When t_B is less than the 10–90% rise or fall time of the line end signal, some intersymbol interference is present and thus, some time jitter in the transitions of the recovered data will be present.

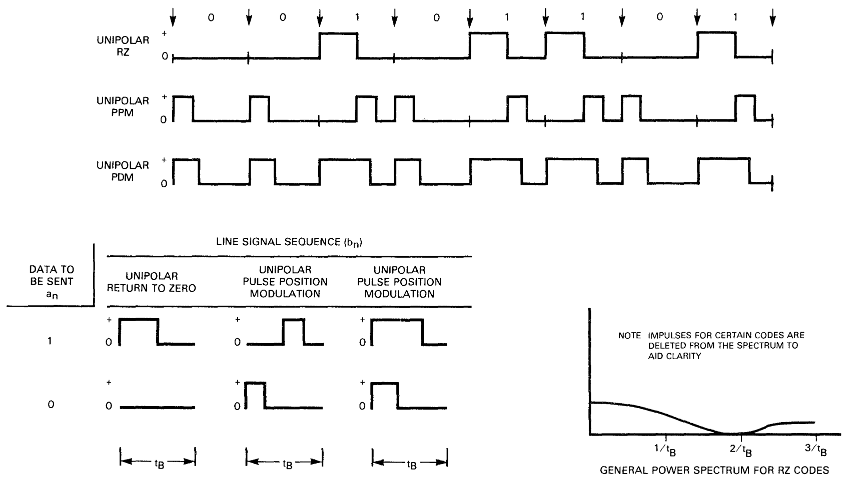
NRZ codes are simple to generate and decode because no precoding or special treatment is required. This simplicity makes them probably the most widely used pulse codes, with NRZ-L the leader by far. NRZ-M has been widely used in digital magnetic recording where it is usually called NRZI for Non-Return to Zero, Invert-on-Ones. In terms of the four desirable features for a pulse code listed at the start of this section, however, none of the NRZ codes are all that great— NRZ codes do possess a strong dc component, and have neither intrinsic clocking, nor error detection features. Even so, their power frequency spectra are used as references for comparison with other pulse codes.

Return to Zero (RZ) Pulse Codes

The RZ group of pulse codes are usually simple combinations of NRZL data and its associated single or double frequency clock. By combining the clock with data, all RZ codes possess some intrinsic synchronization feature. Three representative RZ pulse codes are shown in *Figure 4-21*. Unipolar RZ is formed by performing a logic AND between the NRZ-L data and its clock. Thus a logic Zero is represented by the absence of a pulse during the bit time interval, and a logic One is represented by a pulse as shown. Pulse Position Modulation (PPM) uses a pulse of $t_B/4$ duration beginning at the start of the bit interval to indicate a logic Zero, and a $t_B/4$ pulse beginning at the middle of the bit interval to indicate a logic One. Pulse Duration Modulation (PDM) uses a $t_B/3$ duration pulse for a logic Zero and a $(2/3)\,t_B$ pulse for a logic One, with the rising edge of both pulses coinciding with the start of the bit interval. PDM with $t_B/4$ pulse widths is also used but better results are usually obtained with the $t_B/3$, $2\,t_B/3$ scheme.

The reason for differentiating between information rate and modulation rate can now be further clarified. Each of the RZ pulse codes in *Figure 4-21* has the same information rate; *i.e.,* $1/t_B$ bits per second. Their respective minimum signaling elements (unit intervals) however, are all less than t_B so the *modulation rate* for the RZ pulse code is greater than the *information rate*. Remember that with NRZ signaling, the unit interval and the bit time interval are equal in duration, so the information rate in bps is equal to the modulation rate in bauds. For isochronous NRZ signaling, the measures bps and baud are both synonymous and interchangeable.

Inspection of unipolar RZ signaling reveals that the unit interval is 1/2 bit interval ($t_{ui} = t_B/2$). When this unit interval is less than the 0–50% rise or fall time of the line, the data is likely to be unrecoverable. With a fixed modulation rate, the price paid to include clocking information into unipolar RZ is reduced information rate over that for NRZ signaling. Likewise, for PPM with its unit interval of $t_B/4$, the information rate reduces to 1/4 that of NRZ data under the same conditions. This is because the maximum modulation rate is determined by the 50% rise time of the line which is constant



t_{ui}	$t_B/2$	$t_B/4$	$t_B/3$
$a_n = 1$	$b_n = (+)\{0 \le t < t_B/2$ $b_n = (0)\{t_B/2 \le t < t_B$	$b_n = (+)\{t_B/2 \le t \le 3t_B/4$ $b_n = (0)\{0 \le t < t_B/2$, $3t_B/4 < t < t_B$	$b_n = (+)\{0 \le t < 2t_B/3$ $b_n = (0)\{2t_B/3 \le t < t_B$
$a_n = 0$	$b_n = (0)$	$b_n = (+)\{0 \le t \le t_B/4$ $b_n = (0)\{t_B/4 < t < t_B$	$b_n = (+)\{0 \le t \le t_B/3$ $b_n = (0)\{t_B/3 \le t_B$

Figure 4-21. Return to Zero (RZ) Pulse Codes.

for a given length and type of line. PDM has a unit interval of $t_B/3$ so, for a given maximum modulation rate, the resulting information rate is 1/3 that of NRZ data.

The preceding argument should not be taken as strictly correct—since the actual intersymbol interference patterns for the three RZ codes discussed differ somewhat from the pattern with NRZ codes. A random sequence of NRZ data can easily consist of a long sequence of Zeros followed by a single One and then a long sequence of Zeros, so the $t_{50\%}$ limit can be accurately applied. Unipolar RZ, in response to the same long data sequence, produces a $t_B/2$ pulse, so the $t_{50\%}$ argument can be applied here too. With PPM and PDM, the maximum time that the line signal can be in one state is quite reduced from the NRZ case. For PPM, this time is 1.25 t_B (010 data sequence) while for PDM, it is .67 t_B (see *Figure 4-21*). With PPM and PDM, then, the line signal may never reach the final signal levels that it does with NRZ data. So, the PPM and PDM signals have a head start, so to speak, in reaching the threshold crossing of the receiver. Because of the reduced time that PDM and PPM signal levels are allowed to remain at one signal level, their signaling may still operate at a modulation rate slightly above that where the NRZ data shows 100% transition jitter. Even with this slight correction to the previous discussion, the RZ group of pulse codes still sacrifice information rate in return for synchronization. The PPM scheme appears to be a poor trade in this respect, since PDM allows a greater information rate while retaining the self-clocking feature. Unipolar RZ, because it provides no clocking for a logic Zero signal, is not generally as useful as PDM for baseband data transmission. However, unipolar RZ is used in older digital magnetic tape recorders.

Examination of RZ codes shows only one more desirable feature than NRZ codes: clocking. RZ codes still have a dc component in their power density spectrum *(Figure 4-21)* and their bandwidth is extended (first null at $2/t_B$) over that of NRZ (first null $1/t_B$). RZ codes do not have any intrinsic error detection features.

Phase Encoded (PE) Pulse Codes

The PE group of pulse codes uses signal level transitions to carry both binary data and synchronization information. Each of the codes provides at least one signal level transition per bit interval aiding synchronous recovery of the binary data. Simply stated, Biphase-Level (Biϕ-L) code is binary phase shift keying (PSK) and is the result of an Exclusive-OR logic function performed on the NRZ-L data and its clock; it is further required that the resultant signal be phase coherent (*i.e.,* no glitches). Biphase-Mark (Biϕ-M) and Biphase-Space (Biϕ-S) codes are essentially phase coherent, binary frequency shift keying (FSK). In Biϕ-M, a logic One is represented by a constant level during the bit interval (one-half cycle of the lower frequency $1/(2\ t_B)$, while a logic Zero is represented by one-half cycle of the higher frequency $1/t_B$. In Biϕ-S, the logic states are reversed from those in Biϕ-M. Another way of thinking of Biϕ-M or Biϕ-S is as follows.

- Change signal level at the end of each bit interval regardless of the logic state of the data.
- Change signal level at the middle of each bit interval to mean a particular logic state.

In Biϕ-M (sometimes called diphase), a mid-bit interval change in signal level indicates a logic One (Mark), while no change indicates a logic Zero. For Biϕ-S, no signal level change in the middle of the bit interval means a logic One, while a change means a logic Zero.

In Biϕ-L (also called Manchester Code), a positive-going transition at the middle of the bit interval means a logic Zero, while a negative-going transition there indicates a logic One.

The fourth member of the PE family is Delay Modulation (DM)[15,16] sometimes referred to as Miller code. Here logic One is represented by a mid-bit interval signal level change, and a logic Zero is represented by a signal level change at the end of the bit interval if the logic Zero is followed by another logic Zero. If the logic Zero is immediately followed by a logic One, no signal level transition at the end of the first bit interval is used. The waveforms encoding algorithms, and general power density spectra for the PE pulse code family are shown in *Figure 4-22.*

A brief inspection of the signal waveforms for the three Biphase pulse codes reveals that their minimum signaling element has a duration of one-half bit interval ($t_{ui} = t_B/2$); the longest duration of either signal level is one bit interval. Similarly, DM is seen to have a minimum signaling element of one bit interval ($t_{ui} = t_B$) and the maximum duration of either signal level is two bit intervals (produced by a 101 pattern). Biphase codes should exhibit eye closure (they would not be recoverable without equalization) when $t_{ui} \leq t_{0\text{-}50\%}$. So, a 50% jitter on NRZ signaling approximately corresponds to the Biphase codes non-operation point. Biphase codes, therefore, provide one-half the information rate of NRZ signals at a given maximum modulation rate. This is in exchange for synchronization information and a dc-free spectrum when used in polar form.

DM should have essentially the same intersymbol interference characteristics as NRZ, since the unit interval is the same for both codes. DM may perform slightly better than NRZ, because the maximum duration of either signal level is two bit intervals. Overall, DM is better coding scheme than the Biϕ. It does not require as much bandwidth as Biϕ and still possesses the desirable dc response and synchronization qualities.

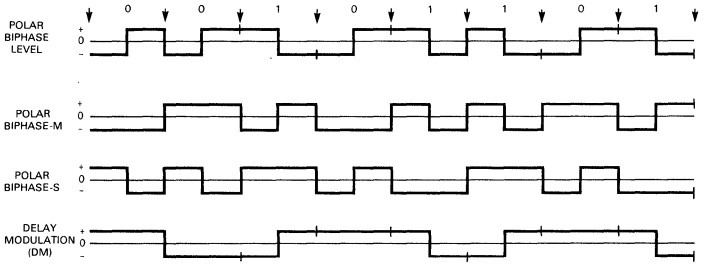
Both Biϕ and DM are good choices for digital magnetic recording[16]; Biϕ is widely used in disc memory equipment, and DM is rapidly gaining acceptance where high bit packing densities are desired. Overall scoring, in terms of the four desirable characteristics, shows the PE pulse codes with three primary features; bandwidth compression, no dc, and intrinsic synchronization.

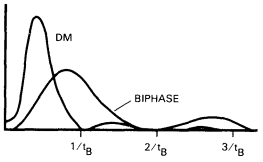
The Biϕ family does not possess any intrinsic error detection scheme. DM does possess the capability of detecting some—but not all—single bit errors. This detection process is accomplished by checking to see if a single level persists longer than two bit intervals, in which case, an error is indicated. DM detection requires two samples per bit interval.

Multi-Level Binary (MLB) Pulse Codes

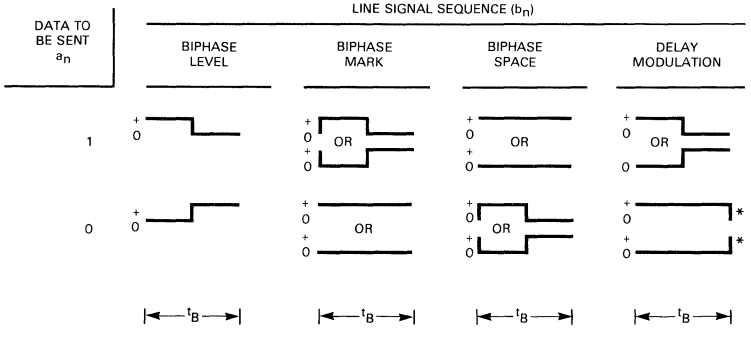
The pulse codes in the MLB group discussed have a common characteristic of using three signal levels (expressed in shorthand notation as +, 0, –) to represent the binary information, but each receiver decision yields only one bit of information. These are sometimes called *pseudoternary* codes to distinguish them from true ternary codes wherein each receiver decision can yield 1.58 information bits.

*Delay Modulation[15,16] has a maximum of 2 t_B without a signal level transition.





GENERAL POWER SPECTRUM FOR SPLIT PHASE CODES



*TRANSITION ONLY IF FOLLOWED BY ANOTHER "0" ($a_{k+1} = 0$)

t_{ui}	$t_B/2$	$t_B/2$	$t_B/2$	t_B
$a_n = 1$	$b_n = (+)\{0 < t < t_B/2$ $b_n = (-)\{t_B/2 \leq t \leq t_B$	‡	$b_n = (-)\ b_{n-1}$* *complement of final level of last b_n	if final value of $b_{n-1} = (+)$ then $b_n = (+)\{0 < t < t_B/2$ and $b_n = (-)\{t_B/2 \leq t \leq t_B$ else, compliment above b_n values for times shown
$a_n = 0$	$b_n = (-)\{0 < t < t_B/2$ $b_n = (+)\{t_B/2 \leq t \leq t_B$	$b_n = (-)\ b_{n-1}$* *complement of final level of last b_n	‡	if final value of $b_{n-1} = (+)$ then $b_n = (+)\{0 \leq t < t_B$ if $a_{n+1} = (0)$ then $b_n = (-)\{t = t_B$ else $b_n = (+)\{t = t_B$ if final value of $b_{n-1} = (-)$ then complement b_n values above

‡ If b_{n-1} final level = (+), then
$b_n = (-)\{0 \leq t < t_B/2$
$b_n = (+)\{t_B/2 \leq t < T_B$

If b_{n-1} final level = (−), then
$b_n = (+)\{0 \leq t < t_B/2$
$b_n = (-)\{t_B/2 \leq t < t_B$

Fig. 4-22. Phase Encoded (PE) Pulse Codes

The most straightforward pulse code in the MLB group is polar RZ *(Figure 4-23)*. Some authors place PRZ in the RZ group, but since PRZ uses three signal levels, it is placed in the MLB group here. A logic One is represented by a positive polarity pulse, and a logic Zero is represented by a negative polarity pulse. Each pulse lasts for one-half bit interval. PRZ has excellent synchronization properties since there is a pulse present during every bit interval.

Bipolar (BP)[17,18] uses a $t_B/2$ duration pulse to signify a logic One, and no pulse during the bit interval to signify a logic Zero. The polarity of the pulses for a logic One is alternated as shown in *Figure 4-23*. Bipolar coding is also known as Alternate Mark Inversion. BP is widely used in Bell Systems T1-PCM carrier systems as a pulse code transmitted along a regenerative repeated transmission line. Since BP has no dc component, the regenerative repeaters along the span line may be transformer coupled and powered by a phantom constant current power loop from the central office. The synchronization properties of BP are excellent if the number of Zero bits transmitted in series is constrained. This constraint on the number of sequential Zeros allows clock circuits in each repeater to remain in synchronization. A scheme called Binary with 6 Zeros Substitution (B6ZS) was developed to replace 6 Zeros with a given signal sequence to offset this loss of synchronization[18]. Bipolar coding has a limited capability to detect single errors, all odd errors, and certain even error combinations which violate the mark alternation rule. Another scheme called High Density Bipolar with 3 Zeros substitution (HDB-3) replaces four successive Zeros (no pulses) with three Zeros followed by a pulse whose polarity violates the Mark alternation rule[19]. Subsequent detection of this pattern (three Zeros and pulse violating the polarity coding rule) causes the receiver to substitute four Zeros for the received 0001 pattern.

In Dicode (DI)[20,21], a polar pulse (either t_B for DI-NRZ or $t_B/2$ for DI-RZ) is sent for every input data transition. The limiting constraint is that the successive pulses must alternate in sign *(Figure 4-22)*. As in NRZ-M and NRZ-S, the actual polarity of the pulses does not necessarily correspond to the logic state of the data (a positive pulse may represent either a Zero-to-One or a One-to-Zero transition of the input data). The power spectrum for DI is the same as for BP (no dc component). Bit synchronization for DI can be obtained in the same manner as for BP, but with DI, the number of bits of the same logic state must be controlled in order for the receiver to maintain bit synchronization. DI also has the intrinsic capability of detecting single bit errors (via two successive positive or negative signal levels), all odd, and some even numbers of errors.

Pair Selected Ternary (PST)[18,22] and Modified PST (MPST)[22] were proposed to minimize the disadvantages of BP coding: loss of synchronization with long strings of Zeros and timing jitter. PST/MPST maintains the strong features of BP: dc free spectrum, single error detection. To produce PST or MPST, the incoming bits are grouped into pairs, and the signal produced on the line is governed by a coding table (see *Figure 4-24*). Two modes are also used in the coding table with a change in mode occurring after a certain bit pair is transmitted. The features of PST/MPST thus include:

- No dc spectral component,
- No loss of synchronization with long strings of Zeros,
- Intrinsic error detection,
- Simplification of requirements for timing extraction circuits with respect to BP.

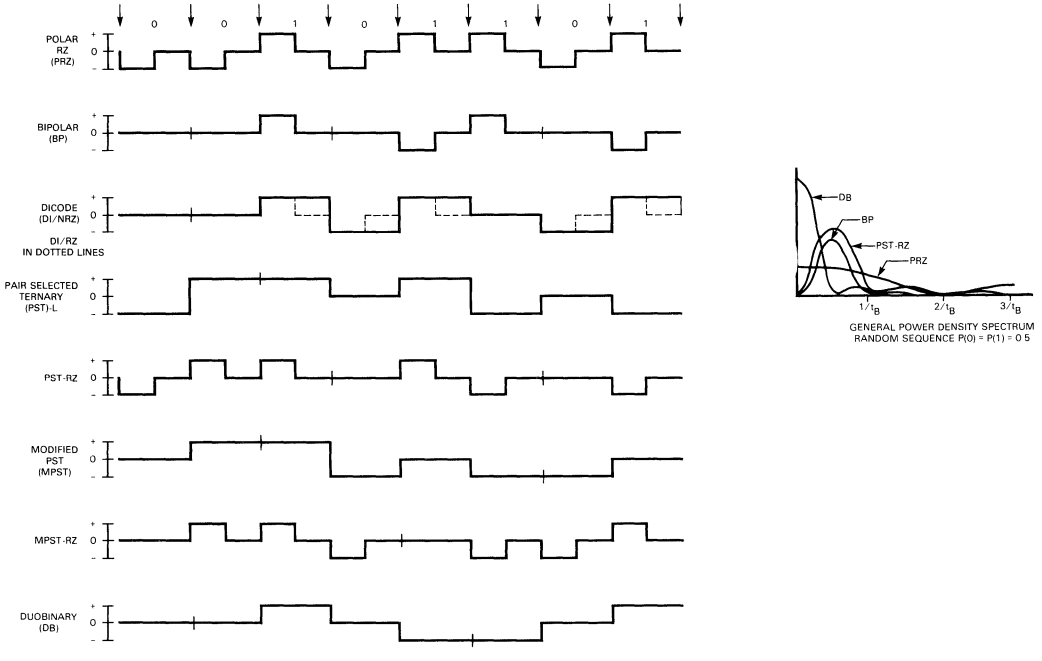


Fig. 4-23. Multilevel Binary (MLB) or Pseudoternary Pulse Codes

MPST coding was developed primarily to speed up the framing process, *i.e.,* selecting which two successive pulses constitute a valid pair, when the probability for a Zero and a One are not equal.

Duobinary[23, 24] is an example of a correlative level coding technique, wherein a correlation exists between successive signal levels. Duobinary uses three signal levels with the middle level corresponding to a logic Zero, and the other two levels corresponding to a logic One. The pseudoternary signal is generated by precoding the input data, which results in constraining the line signal to change only to the neighboring level, *i.e.,* the (+) to (–) and (–) to (+) level changes are not allowed. This precoding process uses controlled intersymbol interference as part of the coding scheme. The benefit is an effective doubling of the bit rate for a given bandwidth and concentration of the power spectrum toward dc *(Figure 4-23).* Duobinary has the capability to detect single errors which violate the encoding rules. In terms of bandwidth utilization, Duobinary ranks first among all the binary and MLB codes[20], but its strong dc component prohibits the use of ac-coupled transmission media. Synchronization properties are similar to NRZ, thus external clocking must be used to recover the data.

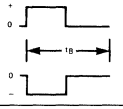
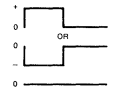
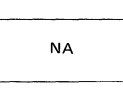
Name	Data to be Sent (a_n)	Line Signal	t_{ui}	Line Signal Sequence (b_n) Generation
Polar Return to Zero (PRZ)	$a_n = 1$ $a_n = 0$		$t_B/2$	$b_n = (+)\begin{cases} 0 \leq t < t_B/2 \\ t_B/2 \leq t < t_B \end{cases}$ $b_n = (0)$ $b_n = (-)\begin{cases} 0 \leq t < t_B/2 \\ t_B/2 \leq t < t_B \end{cases}$ $b_n = (0)$
Bipolar (BP)	$a_n = 1$ $a_n = 0$		$t_B/2$	The polarity of b_n depends on the polarity of b_{n-k} corresponding to the last $a_{n-k} = (1)$. If the last b_{n-k} was a positive pulse (1), then b_n will be a negative pulse (2). If the last b_{n-k} was a negative pulse (2), then b_n will be a positive pulse (1). 1) $b_n = (+)\begin{cases} 0 \leq t < t_B/2 \\ t_B/2 \leq t < t_B \end{cases}$ $b_n = (0)$ 2) $b_n = (-)\begin{cases} 0 \leq t < t_B/2 \\ t_B/2 \leq t < t_B \end{cases}$ $b_n = (0)$
Dicode DI	NA	NA	t_B	$b_n = 0 \quad 0 \leq t < t_B$ If $a_n = a_{n-1}$, $b_n = 0$ or else $b_n = -b_{n-k}$ with b_{n-k} corresponding to last $a_{n-k} \neq a_{n-k-1}$
Pair Selected Ternary (PST-L)	NA	NA	t_B	Pair / Polarities for C_nC_{n+1} $a_n\ a_{n+1}$ / + MODE / – MODE 1 1 / + – / + – 1 0 / + 0 / – 0 0 1 / 0 + / 0 – / [Change mode after transmission of a 10 or 01 a_na_{n+1} pair.] 0 0 / – + / – + $b_n = C_n \begin{cases} 0 \leq t < t_B \end{cases}$
PST-RZ	NA	NA	$t_B/2$	Same pairing and C_nC_{n+1} as above for PST-L. $b_n = C_n\begin{cases} 0 \leq t < t_B/2 \\ t_B/2 \leq t < t_B \end{cases}$ $b_n = (0)$
Modified PST-L (MPST-L)	NA	NA	t_B	Pair / Polarities for C_nC_{n+1} $a_n\ a_{n+1}$ / + MODE / – MODE 1 1 / + 0 / 0 – 1 0 / + – / + – 0 1 / – + / – + 0 0 / 0 + / – 0 $b_n = C_n \begin{cases} 0 \leq t < t_B \end{cases}$ [Change mode after transmission of 00 or 11 a_na_{n+1} pair.]
Modified PST-RZ (MPST-RZ)	NA	NA	$t_B/2$	Same pairing and C_nC_{n+1} table as above for MPST-L. $b_n = C_n\begin{cases} 0 \leq t < t_B/2 \\ t_B/2 \leq t < t_B \end{cases}$ $b_n = (0)$
Duobinary	$a_n = 0$ $a_n = 1$		t_B	If $a_n = 0$ then $b_n = 0$. If $a_n = 1$, then the polarity of b_n depends on the polarity of b_{n-k} for last $a_{n-k} = 1$. If a_n and a_{n-k} are separated by an even number of zeros, then $b_n = b_{n-k}$, if not, then $b_n = (-)b_{n-k}$.

Fig. 4-24. Multilevel Binary Pulse Coding Table

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Section 5
FORMS OF OPERATION

This section discusses the basic forms and modes of operation of data transmission circuits.

- There are two primary forms of signal propagation on transmission lines: single-ended and differential. An examination is made in this chapter of the consequences of each form with respect to system complexity and noise immunity.
- The three primary modes of operation are discussed. The modes refer to the direction of data flow along the line and to whether or not the direction is reversible. For each combination of form and mode of operation, a particular line driver and line receiver is recommended and that specific applications figure is shown.
- An analysis is made of the three most often requested standardized interfaces: EIA RS-232-C, MIL-STD-188C (low level), and the IBM 360/370 Channel I/O interfaces.
- A brief guide is provided for selecting line drivers and line receivers, based on the information presented in the previous chapters. Also, some useful miscellaneous system guidelines are mentioned.

SINGLE-ENDED VS DIFFERENTIAL

There are two basic forms of operation for baseband data transmission circuits: single-ended and differential. The single-ended form uses a single conductor to carry the signal (signal line) with the signal voltage (or current) referenced to a signal return conductor which also may be the common return for other signal conductors. A representation of a single-ended circuit is shown in *Figure 5-1*.

The single-ended form is the simplest way to send data as it requires only one signal line per circuit. This simplicity, however, is often offset by the inability of this form to allow discrimination between a valid signal produced by the driver, and the sum of the driver signal plus externally induced noise signals.

External noise sources can be separated into two primary components: induced noise v_N, and ground potential difference v_{GPD}. Induced noise is usually caused by electrostatic (capacitive) and/or electromagnetic (mutually inductive) coupling between adjacent signal lines, power conductors, etc. The induced noise is referred to as *crosstalk*. A ground potential difference is caused by current flow through the finite resistance and inductance associated with the signal common return. The predominant component of v_{GPD} is usually 60 Hz (the ac mains frequency). Because the receiver sees the sum of the driver output voltage v_O, the induced noise voltage v_N and the ground potential difference v_{GPD} at its input, there is no way the receiver can differentiate between the desired driver signal v_O and a possibly erroneous signal ($v_O + v_N + v_{GPD}$). The ratio of the signal voltage to the signal + noise voltage must be made sufficiently large to aid data recovery by the line receiver. This can be accomplished by several methods:

- Use shielded cable to reduce crosstalk between signal lines.
- Increase driver output signal levels to swamp out the noise signals.
- Reduce the ground circuit impedance to reduce the ground potential difference.
- Isolate the signal leads from power carrying conductors.
- Control slew rate of the driver to reduce capacitively coupled crosstalk between signal leads.
- Incorporate hysteresis in the line receiver to increase relative noise immunity.
- Limit line length to reduce circuit exposure to noise sources.
- Apply a combination of the above.

Each of the above "remedies" has its own disadvantages too. Using shielded cable (coax) is generally expensive; increasing driver signal levels may be costly in terms of system power particularly when the circuit is parallel terminated. Also- reducing ground circuit impedance may not be possible due to the magnitude and characteristics of the external noise sources, and at the very least, adds expense in wire costs. Isolating signal leads from each other and from power conductors may be possible in some systems, but does make interconnecting cables unwieldy. Driver slew rate control and/or hysteresis in the receiver can decrease crosstalk and increase relative dc noise immunity, respectively. They can, however, lead to severe signal quality degradation from bias effects. Both methods increase system delay, thus reducing system operating speed. Line length limiting may not be possible, as the system components may be quite separated from each other. In any event, applying one or more of the above remedies must be carefully considered in light of the individual system requirements. A solution to some of the problems inherent in the single-ended form of operation is offered by the differential form of operation *(Figure 5-2)*.

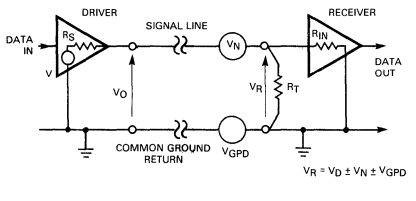


Fig. 5-1. Single-Ended Circuit Form of Operation

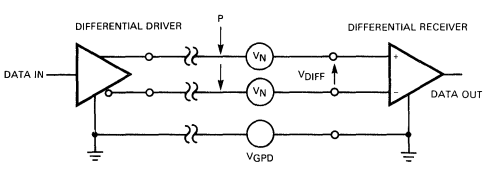


Fig. 5-2. Differential Circuit Form of Operation

As illustrated, the differential form of operation uses a differential driver (essentially two single-ended drivers with one driver always producing the complementary output signal level to the other driver), a twisted pair transmission line and a differential line receiver. The twisted pair line itself offers several features.

- Transverse magnetic fields, produced by external noise sources, induce currents in the line, which are essentially cancelled out by the alternating polarity of the magnetic circuits provided by adjacent twists of the line.
- In a line with perfect longitudinal balance, both wires in the pair are equally affected by electrostatically coupled noise. This results in a net common mode signal with respect to the ground return.
- Ground potential difference also appears as a net common mode signal to the line receiver.

The driver signal appears as a differential voltage to the line receiver, while the noise signals appear as a common mode signal. The two signals, therefore, can be discriminated by a line receiver with a sufficient common mode voltage operating range.

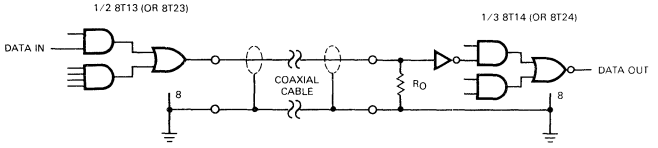
The use of parallel wire cable, *e.g.*, flat or ribbon cable, with differential operation provides approximately the same benefits as provided by a *twisted pair*, with the exception that induced currents caused by transverse magnetic fields do not cancel out. The flat cable presents a single magnetic circuit to the external noise source, instead of the many magnetic circuits of alternating polarity presented by a twisted pair. Thus, with flat cable, this single magnetic circuit allows a transverse magnetic field to induce currents producing a net common mode signal.

The choice of single-ended or differential operation depends to a large degree on the line length (exposure to external noise sources) and on the characteristics of the external noise sources. In high EMI environments, differential operation may provide the extra noise immunity necessary to make system operation feasible, thus offsetting added cost of implementing the differential data transmission circuit.

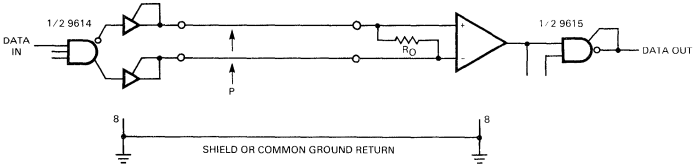
MODES OF OPERATION

The term modes of operation refers to the direction of data flow on the transmission circuit. The fundamental mode of operation is *simplex (Figure 5-3)*, which means unidirectional, non-reversible data flow from the line driver to the line receiver(s). If more than one receiver is used, then the mode can be called a *simplex distribution bus (Figure 5-4)*. The simplex mode of operation can be used with single-ended or differential forms, and with polar or unipolar drivers.

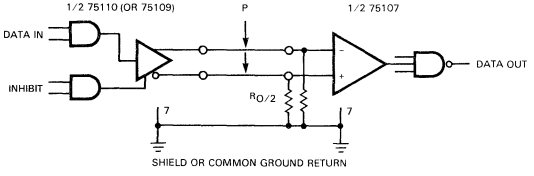
The *half-duplex* mode is a non-simultaneous, reversible data flow between two line driver/receiver pairs called *ports*. These ports are located at opposite ends of a transmission line *(Figure 5-5)*. It is important to provide parallel line terminations at each end of the line to suppress reflections, otherwise system noise immunity and even system speed may suffer. The type of parallel terminations to use is determined by the



a. Single-Ended, Unipolar

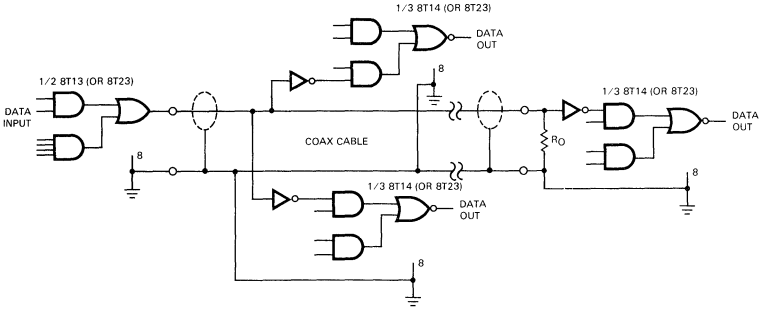


b. Differential, Unipolar (Single Supply)

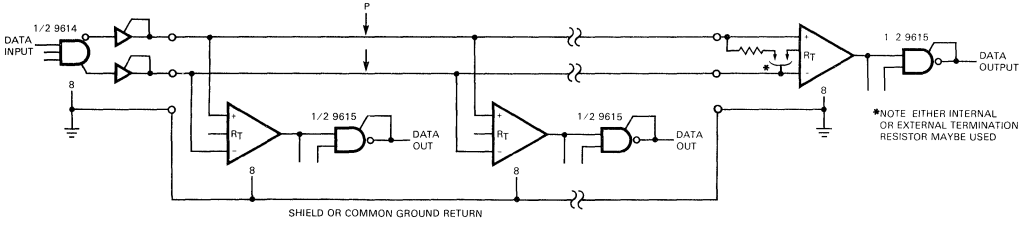


c. Differential, Unipolar (Dual Supply)

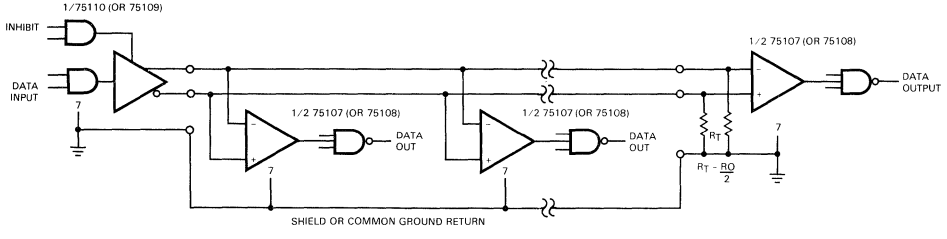
Fig. 5-3. Simplex Modes of Operation



a. Single-Ended, Unipolar (Single Supply)



b. Differential, Unipolar (Single Supply)



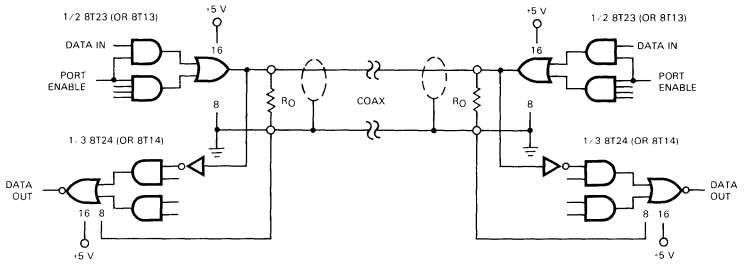
c. Differential, Unipolar (Dual Supply)

Fig. 5-4. Simplex Distribution Bus

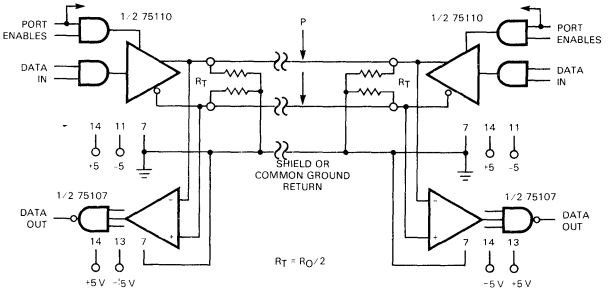
line driver's characteristics. *Figure 5-5* shows three sets of IC drivers and receivers connected with their respective, proper temination networks. Half-duplex operation may also use either single-ended or differential form with polar or unipolar drivers.

Full-Duplex operation is simultaneous, two-way data flow between two ports. It is not usually feasible in baseband signalling, although some bridge-type circuitry has been used[1] The difficulty in baseband full-duplex operation is the separation of the signal levels produced by the two drivers operating on the loop simultaneously. However, non-baseband, full-duplex operation using frequency division multiplexing (FDM) techniques is widely used. The most common example of the FDM full-duplex operation, the 103 type modem, uses frequency shift keying (FSK) and two frequency bands to keep the data paths separate.

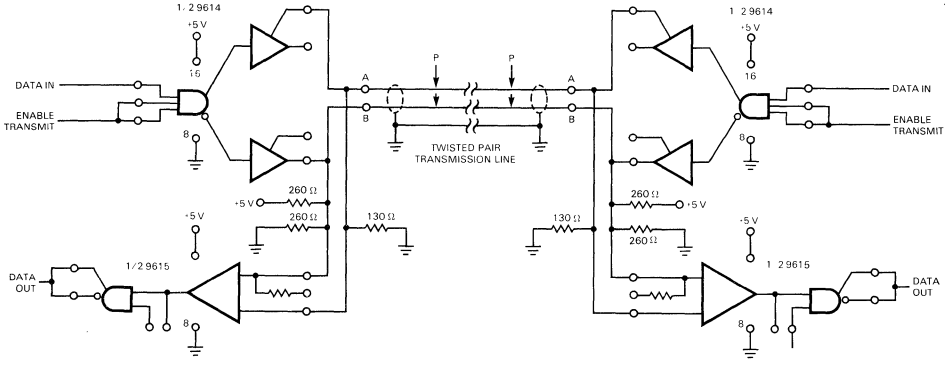
The logical extension to half-duplex operation is *multiplex* sometimes called a *data bus* or *party line (Figure 5-6)*. Multiplex operation is non-simultaneous data flow among three or more ports connected to the same physical transmission line. Like simplex and half-duplex modes, multiplex operation may be used in single-ended or differential form with polar or unipolar drivers.



a. Single-Ended, Unipolar

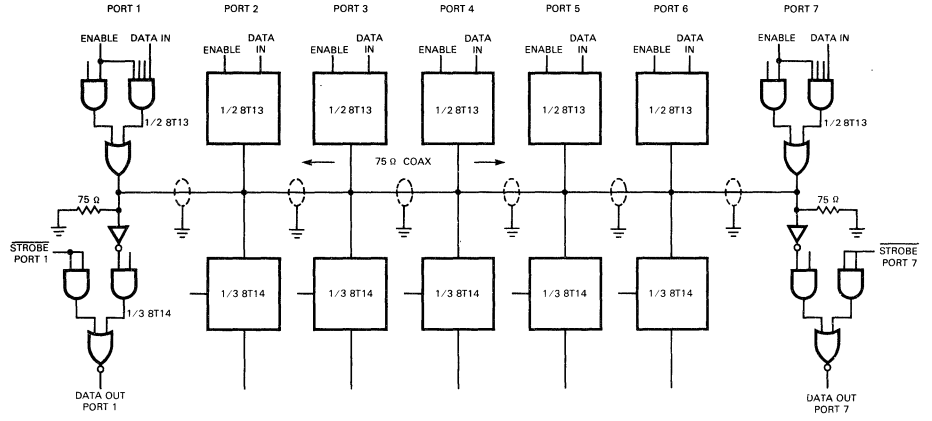


b. Differential, Unipolar (Dual Supply)

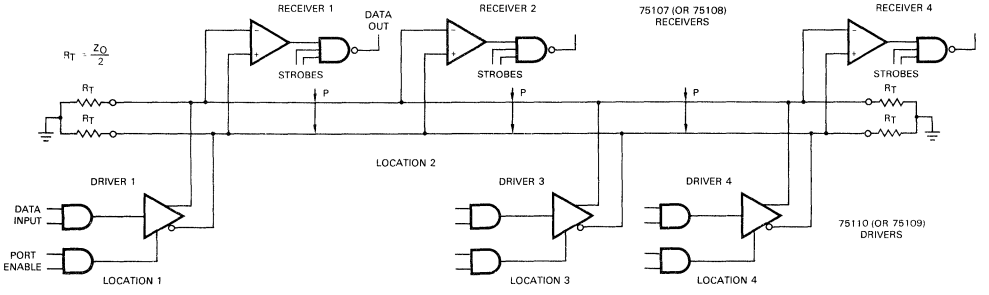


c. Differential, Unipolar, (Single Supply)

Fig. 5-5. Half-Duplex Modes of Operation



a. Single-Ended, Unipolar



b. Differential, Unipolar (Dual Supply)

Fig. 5-6. Multiplex (Data Bus) Operation

The primary advantage of multiplex operation over simplex operation is reduction of wire costs—one physical transmission line can serve where several were once required. The disadvantages of multiplex mode include increased complexity of driver circuits to include an "off" state, and the added logic required to implement bus protocol or "handshaking".

Particularly, when multiplex operation is desired, consideration must be given to the following areas:

- The protocol or *handshaking* required for a particular port on the bus to send data must be designed. The protocol sequence usually involves the following operations.

  1) The port must signal a desire to use the bus (interrupt).

  2) Bus controller must acknowledge interrupt and send *go ahead* command.

  3) Port assumes control of bus and sends data, perhaps preceded by the code to indicate the recipients(s) of the following data.

  4) Receiving port(s) must acknowledge receipt of data.

  5) Transmitting port receives the acknowledgement, and releases control of the bus so that other ports may pass their data.

The overall bus operation is either polled or asynchronous. In polled operation, a central bus controller addresses each port in turn to ask if any data is waiting to be sent. If the addressed port has no traffic, it signals *no data* and the controller inquires at the next port. If the port has some data, then the controller gives a *go ahead* to the port; data is sent, and the controller then inquires at the next port.

In asynchronous operation, any port having data essentially "holds up its hand" and waits for a go-ahead signal to ripple down the series enabling logic. The priority for a particular port is determined by the ports proximity to the master control port which sends a go-ahead down the enable logic chain at regular time intervals. This scheme is well suited to bus-organized minicomputers. The Digital Equipment Corporation's Unibus® and Omnibus® architectures are excellent examples.

- The effect of powered-down drivers and receivers on normal bus operation must also be considered. Integrated circuit drivers and receivers contain parasitic diodes that

are normally reverse biased when the power supply is on. Unless special design techniques are used, these diodes can become forward-biased when the unit is powered-down causing the bus to malfunction.

- The protocol timing must include sufficient time delays to allow for the different port-to-port signal propagation delays.

- Both physical ends of the transmission line comprising a channel for the bus must be terminated to prevent spurious signal levels due to reflections.

- Stubs or taps from the main transmission line should be kept to a minimum length. A *daisy chain* wiring method is preferable to a *tap-off* method. If stubs must be used, then to cause the least perturbations on the line, the stub length should be controlled such that the propagation delay of the stub is less than 1/8 of the signal rise or fall time at the stub-to-line connection point.

- If a 3-state driver system is used (logic Zero, logic One and *off* or driver in high impedance state), some means must be provided to detect the difference between a driver sending data and the all-drivers-off condition. In the 2-state bus system, this problem does not occur because a logic Zero (usually a HIGH) indicates either a logic Zero or that no port is currently sending. A logic One (usually a LOW) on a 2-state system then indicates a port is transmitting a logic One and the receiver should interpret it as such.

- The data format must also be considered:

  Parallel operation is fast but expensive, since it requires one transmission line and the associated interface for every bit of the word (or byte) transmitted in parallel.

  Serial operation is slower, but requires only one transmission line and interface per port. This saving may, however, be partially offset by the need for a parallel-to-serial converter at the transmitting site, and a serial-to-parallel converter at the receiving site.

  The parallel structure is commonly used for rapid exchange of data over short distances; *e.g.*, within a computer or between a computer and peripherals. The serial structure is used for communications over long distances, as between a terminal and its controller.

- A final consideration concerns polled operation of a multiplex system. The amount of time necessary to address and receive acknowledgement from a port must be weighed against the volume of data the ports normally send, and the total number of ports on the bus. If there is a large number of ports on the bus, most of the time might be used by the polling operation with very little time devoted to actual exchange of information. A large number of ports combined with a high relative volume of traffic expected per port can lead to data backing up at each port waiting to be sent, and an overall reduction in information throughout. In a real time system where fast response is essential, serious consideration should be given to splitting up a single large bus into several satellite busses, each with its own polling controller and protocol with respect to the central bus. Queuing theory can be used to estimate the throughput on a bus structure when many variables, including the number of ports, the mean transaction length, and the number of transactions per port per unit time, are known[7].

STANDARDIZED INTERFACES

There are two main ways the interface electrical characteristics become standardized. The first, and probably most common, is informal adoption via proliferation of devices having the specified electrical characteristics. Excellent examples of this informal method are provided by TTL and ECL logic levels, and loading rules. The input/output electrical characteristics of these two logic families have become "standards" because many different manufacturers make devices which can be easily interconnected.

Informal standards may also be born when an equipment manufacturer announces a product that other competing manufacturers wish to directly connect to their respective products. If the original manufacturer of the product has a large share of the market place (and a large number of competitors) an "instant standard" can easily arise. A good example of this is the IBM 360/370 I/O interface (channel to control unit)[2], which is standardized primarily because, first, IBM has a large share of the computer market place; and second, a large number of manufacturers are interested in selling "plug compatible" peripheral devices. Thus, one company's electrical interface may become an informal standard in a very short time. Likewise, minicomputer manufacturers, such as DEC, may have their in-house interface characteristics for their Unibus® and Omnibus® "standardized" via the wide application of their products, and the proliferation of competitive *add-on* manufacturers.

Formal interface standards are usually issued either by collective associations of manufacturers (EIA), U.S. Government and military (FIPS, DCA), international organizations (CCITT, ISO), or other interested organizations (IEEE, ANSI). These standards usually arise when two different pieces of equipment that may be built by two or more different manufacturers must interface, as in data terminals and data modems, or when a government organization is setting up a system which requires interface uniformity. Adherence to the standards is usually voluntary. However, if a manufacturer wishes to sell products in the application area encompassed by the standard, it behooves him to comply if at all feasible. In the past, formal standards have usually adopted the electrical characteristics of a pre-existing interface, especially if the usage of such electrical characteristics was widespread at the time the standard was drafted. The resultant standard is then mostly a blessing given to one set of interface specifications, rather than an optimal, more general solution to data communications interface problems. Lately, both the national and international standards organizations have been seeking greater intercourse with one another, with an effort to produce fewer different electrical interface standards, and ascertain the optimum technical solution to satisfy the greatest number of application requirements. Interoperability and compatibility with pre-existing equipment is a primary requirement in any new standard, consequently much work is devoted to this task.

The majority of requests for standardized interface devices are currently for EIA RS232-C (and CCITT V.24), MIL-STD-188C (low level), and IBM 360/370 I/O. The EIA interface[3] and CCITT V.24[4] are intended for use between data terminal equipment (DTE) and data communications equipment (DCE). The two standards have essentially the same electrical specifications, but differ in signal lead nomenclature. Both standards also specify the protocol to be used between the DTE

and DCE. The interface is a simplex, single-ended, polar, unterminated type with line length and slew rate limiting used for control of reflection effects. The implied maximum cable length is 50 feet, and all signals are referenced to a common signal return lead. The maximum modulation rate on the interface is 20 kbaud. The primary electrical characteristics of the interfaces are listed in *Figure 5-7.*

Fairchild manufactures one triple driver (9616) and two receivers (9617 and 9627) to meet the requirements for this application. The 9616 triple EIA/MIL line driver has two particularly valuable features making it easier to use than other currently available EIA interface drivers. First, the 9616 has internal slew rate limiting which eliminates the need for an external capacitor for each driver. Second, the logic function performed by the 9616 is AND-OR-INVERT (AOI), instead of the usual NAND structure. The AOI still allows the "SPACE-ORing" of two data signals as provided by the NAND type drivers, while activation of the NOR (Inhibit) input to the 9616 forces the driver to a MARK state (called MARK Hold) regardless of the logic states of the data inputs. The latter feature of the 9616 enables the protocol sequence to easily be initiated or terminated without requiring the extra logic gate needed by NAND type drivers performing the same function. More discussion on EIA RS232-C and the 9616/9617 devices is presented in Fairchild Application Note 320. The usage of the 9616/9617 devices as an RS232-C interface is shown in *Figure 5-8.*

Characteristic	EIA RS-232-C Limits		Units	Section in Standard	Notes	MIL-STD-188C (low level) Limits		Units	Section in Standard	Notes
	MIN	MAX				MIN	MAX			
Driver output voltage V_{OH}		25	V	2.6		5	7	V	7.2.2.1	1
Open circuit V_{OL}	-25		V			-7	-5	V		
Driver output voltage V_{OH}	5	15	V	2.6	$3\ k\Omega \leq R_L \leq 7\ k\Omega$					
Loaded output V_{OL}	-15	-5	V							
Driver output resistance										
Power on R_O							100		1.2.1.2	$I_{OUT} \leq 10$ mA
Power off R_O		300		2.5	$-2\ V \leq V_O \leq 2\ V$					
Driver output short circuit current	-500	+500	mA	2.6		-100	+100	mA	7.2.1.2	
Driver output slew rate										
All interchange circuits		30	V/us	2.7(5)		5	15	%UI	7.2.1.3	2
Control circuits	6		V/ms	2.7(3)						
Rate and timing circuits	6		V/ms	2.7(4)						
	4		%UI	2.7(4)						
Receiver input resistance R_{IN}	3	7		2.4	$3\ V \leq V_{IN} \leq 25\ V$	6			7.2.1.4	mod rate $\leq$200 kbaud
Receiver open circuit input bias voltage	-2	+2	V	2.4						
Receiver input threshold										
Output = MARK	-3		V	2.3			+100	μA	7.2.1.6	3
Output = SPACE		3	V			-100		μA		

NOTES:

1. Ripple $\leq$ 0.5%, V_{OH}, V_{OL} matched to within 10% of each other.
2. Waveshaping required on driver output such that the signal rise or fall time is 5 to 15% of the unit interval at the applicable modulation rate (7.2.1.3).
3. Balance between marking and spacing (threshold) currents actually required shall be within 10% of each other (7.2.1.6).

Fig. 5-7. Electrical Characteristics of EIA RS-232-C and MIL-STD-188C (Low Level)

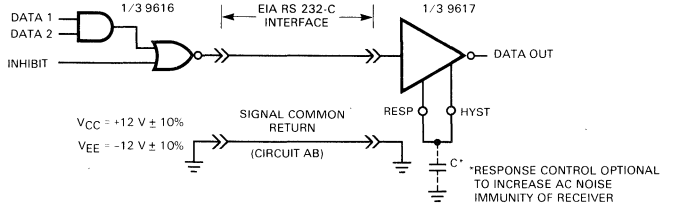


Fig. 5-8. EIA RS-232-C Interface Application

MIL-STD-188C low level interface[5] devices are often requested in conjunction with RS232-C capability. Fortunately, the two standards have overlapping specifications (See *Figure 5-7*) so that one driver designed to satisfy the electrical requirements in MIL-STD-188C also satisfies the electrical requirements in RS232-C. The notable exception is the 5 to 15% driver signal waveshaping requirement in 188C. The 9616 was designed with both specifications in mind, so only an external capacitor on the 9616 output (as shown in *Figure 5-9*) is needed to perform the required waveshaping for MIL-STD-188C at the desired modulation rate.

The electrical characteristics for the receiver in both standards are somewhat different (see *Figure 5-7*) in input resistance and threshold levels, but both standards are satisfied by the 9627 dual EIA/MIL interface receiver. Option strapping on the 9627 allows the user to choose the receiver input resistance (either 3 to 7 kΩ or >6 kΩ) and threshold levels. The 10% threshold matching requirement MIL-STD-188C can be met with the 9627 by a trimming network as shown in *Figure 5-9*.

Where EIA RS232C and MIL-STD-188C (low level) are primarily intended for use on DTE-DCE interfaces, and are *formal* standards, the IBM 360/370 I/O interface is probably the best known example of an *informal* standard interface. The I/O interface[2] is the communications link between a channel in the System 360 or System 370 computer and the various I/O control units. The interface specification delineates electrical characteristics, information formats, and control sequences to pass information between the channel and the peripheral control unit. The primary electrical characteristics are shown in *Figure 5-10*. The interface is a multiplex, single-ended, unipolar variety designed to operate with up to 10 ports on a double terminated 95 transmission line of either coax or tri-lead[6] cable. The 8T23 and 8T24 devices satisfy the requirements in the IBM document[2] for bus drivers and bus receivers respectively. Their use is shown in *Figure 5-11*.

SELECTING LINE DRIVERS AND LINE RECEIVERS

Selecting a line driver—transmission line—line receiver to meet a particular system criterion is a much easier task

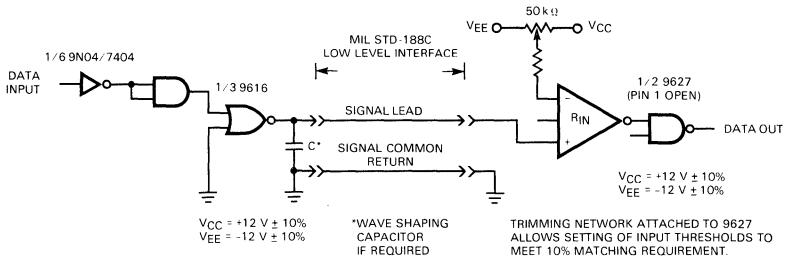


Fig. 5-9. MIL-STD-188C Low Level Interface Application

Characteristic		MIN	MAX	Units	Conditions	Notes
Driver output voltage	Zero state		0.15	V	I_{OUT} = 240 μA	
	One state	3.11		V	I_{OUT} = -59.3 mA	1
			5.85	V	I_{OUT} = -30 μA	2
			7.0	V	I_{OUT} = -123 mA	3
Receiver input thresholds	V_{IH}		1.7	V		
	V_{IL}	0.7		V		
Receiver input current	I_{IH}		0.42	mA	V_{IN} = 3.11 V	
	I_{IL}	-0.24		mA	V_{IN} = 0.15 V	
Receiver input resistance	R_{IN}	4	20	kΩ		
Receiver input operating		-0.15	7	V	power on in receiver	
Voltage range		-0.15	6	V	power off in receiver	

Neither drivers nor receivers will cause spurious noise on the line during a power-up or power-down sequence.

NOTES:

1. Current flow out of driver (2 terminators, 10 receivers).
2. Current flow out of driver (one receiver, no terminator).
3. Current flow out of driver during over-voltage interval to driver.

Fig. 5-10. Electrical Characteristics for IBM System 360/370 Channel I/O Interface[2]

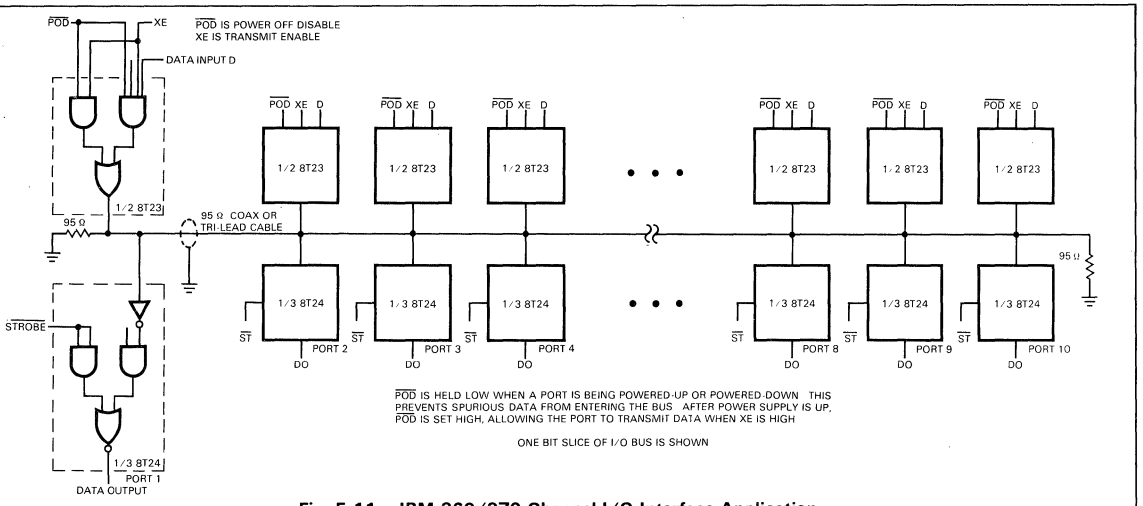


Fig. 5-11. IBM 360/370 Channel I/O Interface Application

than initially choosing the target system characteristics. The former is a relatively simple process of comparing the device characteristics to the design goals. The latter is a difficult matter because of the large number of variables involved. Designing from scratch, however, is not an impossible task. The primary choices to be made are as follows:

- Simplex or multiplex operation of the lines.
- Single-ended or differential operation.
- Pulse code.
- Signal quality vs line length trade-off for particular pulse codes selected.
- Line termination method.

With these choices in mind, *Figure 5-12* was constructed to recommend the optimum Fairchild devices for the particular applications constraints.

SYSTEMS CONSIDERATIONS

The following points should be considered when using transmission line interface circuitry.

- The most limiting factor to data rate with long lines (> 50 feet) is usually the rise and fall time of the cable. The use of the eye pattern allows easy measurement of signal quality (amount of time jitter).

- Differential forms are preferable to single-ended forms where high noise environments are present. Opto-isolators and transformers offer high common mode operating ranges and ground isolation. With transformers, a dc-free, self-clocking code such as Biϕ (digital binary phase modulation) is useful.

- The total number of ports on a multiplex system should be restricted so that the parallel combination of the input impedance of receivers and the output impedances of disabled drivers is greater than the characteristic resistance of the transmission line.

- Ground returns are necessary for proper operation of integrated circuit line drivers and receivers. This may be accomplished by connecting the shield of the line to the ground pins of ICs connected to the line.

- Data rates above 10 Mbaud will usually require ECL to be used instead of TTL types for the drivers and receivers, because of the 20 to 50 ns propagation delays in the TTL compatible devices.

- Liberal use of .01 to .1 μF capacitors to decouple the power supplies feeding line drivers and receivers is recommended. One capacitor per power supply for every two to four devices is usually sufficient.

REFERENCES

1. R. Gaiser; "Two-Wire DC Baseband System for Two-Way Simultaneous Data Transmission at High Speeds", Conference Record of 1970 International Conference on Communications; paper 70-CP-283-COM, pp. 16-33 to 16-41.

2. IBM System 360 and System 370 I/O Interface Channel to Control Unit Original Equipment Manufacturers Information; IBM document GA22-6974-1, July 1972.

3. EIA RS-232-C; Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange; Electronic Industries Association, August 1969.

4. CCITT, White Book, Volume VIII; International Telecommunication Union, 1969, recommendation V.24 (revised and reissued as V.28).

5. MIL-STD-188C, Department of Defense; Low Level Interface, section 7.2, November 1969.

6. J.T. Kolias; "TRI-LEAD: A New Interconnection Scheme for Computers", Electronic Packaging and Production, February 1972, pp. 80-90.

7. J. Martin; Systems Analysis for Data Transmission, Prentice-Hall, New York, 1972.

Standard

Interface	Recommended Driver/Receiver		Comments	Fig.
EIA RS 232-C	9616, 1488, 75150	9617, 1489, 75154	0 to 20,000 bps. maximum cable length implied in standard is 50'.	5.8
MIL STD 188C	9616	9627	Use capacitor from 9616 output to ground to provide wave-shaping at applicable modulation rate.	5-9
IBM 360 I/O	8T23, 75123	8T24, 75124	Recommended maximum of 10 ports on bus.	5-11

Single-Ended Simplex

Line Length (feet)	Maximum Data Rate (NRZ Data)	Line* Type and Z_0	Recommended Driver/Receiver		Comments	Fig.
0 - 2'	20M bps	SW, TP, COAX > 90 Ω	TTL Gate	TTL Gate	Unterminated line. Obey loading rules.	
2 - 20'	10M bps	TP, TPS, COAX > 90 Ω	9009 or 7440	TTL Gate	Use parallel terminated line with more than one receiver. Use series terminated line with only one receiver.	5-1
		COAX ≥50 Ω	9S140	TTL Gate	Use parallel terminated line with more than one receiver. Use series terminated line with only one receiver.	5-1
20 - 500'	10M bps@ 20' 0.5M bps@500'	TPS, COAX ≥ 50 Ω	8T13,75121	8T14,75122	Use parallel terminated line.	5-3
> 500'					Not recommended. Use balanced differential form to gain system noise immunity.	

Single-Ended Multiplex

0 - 2'	10M bps	SW	Open Collector TTL	TTL Gate	Use wired-AND with low value (< 1 kΩ) collector pull up resistor. Obey loading rules.	
2 - 20'	10M bps	TP, COAX > 75 Ω	8T13,75121 or 8T23,75123	8T14,75122 or 8T24,75124	Single +5 V supply. Use parallel termination at both ends of bus.	5-6d
20 - 500'	10M bps @ 20' 0.5M bps@500'	COAX > 95 Ω	8T23,75123	8T24,75124	Use parallel termination at both ends of bus. Single +5 V supply required.	5-11 5-11
> 500'					Not recommended. Use balanced differential form to gain system noise immunity.	

Differential Simplex

0 - 50'	10M bps	TP > 50 Ω, TPS > 80 Ω	9612	9613/15	Use parallel termination. Single +5 V supply required.	5-3b 5-4b
			9614	9613/15		
			75110A/ 112	75107/ 108	Split parallel termination. +5 and -5 V supplies required.	5-3c
50 - 4,000'	Use signal quality graph.	TPS > 50 Ω, > 80 Ω	9612	9613/15	Use parallel termination. Single +5 V supply required.	5-3b 5-4b
			9614	9613/15		
			75110A/ 112	75107/ 108	Use split parallel termination. +5 V and -5 V supplies required.	5-3c
> 4,000'					Cable loss exceeds 6 dBV. Perhaps non-baseband techniques should be used, (i.e., MODEMS).	

Differential Multiplex

0 - 50'	15M bps	TP, TPS >90 Ω	75110A/ 112	75107/ 108	Use split parallel termination at each end of line. Requires +5 V and -5 V supplies.	5-6b
		TP, TPS >90 Ω	9614	9615	Connect as shown in half duplex differential circuit. Requires single +5 V supply.	5-5c
50 - 4,000'	Use signal quality graph.	TPS >90 Ω	75110A/ 112	75107/ 108	Use split parallel termination at each end of line. Requires +5 and -5 V supplies.	5-6b
> 4,000'					Cable loss exceeds 6 db V. Perhaps non-baseband techniques should be used, (i.e., MODEMS).	

*SW — Single Wire over Ground Connection
TP — Twisted Pair
TPS — Shielded Twisted Pair
COAX — Coaxial Cable

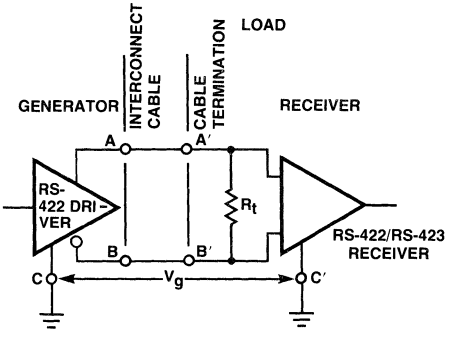
Fig. 5-12. Selection Guide for Line Drivers/Line Receivers

Section 6
SATISFYING EIA STANDARDS RS-422 AND RS-423

The Electronic Industries Association, EIA, has this year released new standards for binary digital interfaces between Data Communication Equipment (modems), and Data Terminal Equipment (CRT Terminals, teletypewriters, etc.). These standards are RS-422, Electrical Characteristics of Balanced Voltage Digital Interface Circuits, and RS-423, Electrical Characteristics of Unbalanced Voltage Digital Interface Circuits. RS-423 replaces the electrical section of RS-232-C, the existing EIA standard, and expands its capabilities to include operations at higher data rates and over greater distances. RS-422 incorporates a technology not covered by RS-232-C, defining a balanced, differential, high speed interface. The following table provides a brief comparison of the recommended maximums for these standards.

EIA Standard	Cable Length (Recommended Maximum)	Data Rate (Recommended Maximum)
RS-232-C	50 ft.	20 Kbps
RS-423	4000 ft. @ 1 Kbps	100 Kbps @ 40 ft.
RS-422	4000 ft. @ 100 Kbps	10 Mbps @ 40 ft.

Development of RS-422 and RS-423 was initiated during 1973 when the existing standard, RS-232-C was due for review. (EIA reviews its standards on a five year cycle). At this time it was decided to bring out a new standard that would eliminate the deficiencies of RS-232-C and to reconcile it with the standards CCITT V. 24 (now revised to V. 28) and MIL-STD-188C with the hope that one standard or very similar standards would cover the military, international and commercial areas. In addition, it was intended that the resulting standard should be readily implemented with integrated circuitry and should facilitate an orderly transition from existing RS-232-C equipment without forcing obsolescence or expensive retrofits. At this time the structure of standards at EIA was evolving such that three separate standards, electrical, functional and mechanical, together would replace RS-232-C.



AB: Generator Interface
A'B': Load Interface
R_t Cable Termination Resistance (Optional)
C: Generator Circuit Ground
C': Load Circuit Ground
V_g: Ground Potential Difference

Fig. 6-1 RS-422 Balanced Interface Circuit

There are several areas for improvement in the electrical section of RS-232-C. It has been felt that the driver and receiver circuits as well as the interchange circuit, in general, were underspecified. More specifically, the voltage levels of the interchange signals are larger than necessary or desirable at ± 15 V. The maximum cable length was too short at 50 feet, the data rate was too low at 20 kilobits-per-second, and no provision for multiple receivers was provided. Additionally, the low common mode operating range and susceptibility to crosstalk made some applications risky. The interconnecting cable, itself, was only addressed in terms of length and capacitance.

The influence of RS-422 and RS-423 has been pervasive. The proposed Federal Standards 1020 and 1030 accept RS-422 and RS-423, respectively, without change. The proposed MIL-STD-188-114 incorporates RS-422 and RS-423 with only a minor addition. These standards are also being utilized by ANSI, the Public Data Networks Interface, and at the international level they are included in CCITT provisional recommendations X.26 (unbalanced) and X.27 (balanced).

RS-422 Driver (Balanced)

RS-422 allows either a unipolar or a polar driver. The unipolar approach offers a potentially cheaper system as its operation requires only a single power supply but at the expense of introducing a common mode component to the signal. The polar approach offers the potential of minimizing any common mode signal, but requires two power supplies for operation.

The generator or driver specified in RS-422 is a circuit with low impedance, balanced, voltage source outputs that provide a differential signal voltage in the range of 2 to 6 volts. (Refer to *Figure 6-1*). The two

RS-422 DRIVER CHARACTERISTICS			LIMITS		
			MIN	MAX	UNITS
Output Voltage — Open Circuit: Vo, Voa, Vob					
(See Figure 6-2)		Vo	−6.0	6.0	V
		Voa	−6.0	6.0	V
		Vob	−6.0	6.0	V
Output Voltage — Terminated: Vt					
(See Figure 6-3)		$\|Vt\|$	2.0		V
			0.5 Vo		V
Output Voltage Matching Error:					
(See Figure 6-3)	$(\|Vt\| - \|\overline{Vt}\|)$		−0.4	0.4	V
($\overline{Vt}$ is the output voltage of the opposite binary state.)					
Output Offset Voltage: Vos					
(See Figure 6-3)		Vos	−3.0	3.0	V
Output Offset Voltage Matching Error:					
(See Figure 6-3)	$(\|Vos\| - \|\overline{Vos}\|)$		−0.4	0.4	V
($\overline{Vos}$ is the output offset voltage of the opposite binary state.)					
Output Short Circuit Current: Isa, Isb					
(See Figure 6-4)		Isa	−150	150	mA
		Isb	−150	150	mA
Output Leakage Current — Power Off: Ixa, Ixb					
(See Figure 6-5)		Ixa	−100	100	μA
($-0.25\ V \leq Vx \leq 6.0\ V$)		Ixb	−100	100	μA
Transition Time — Differential: t_r, t_f					
(See Figure 6-6)	$t_b < 200$ ns	t_r		20	ns
		t_f		20	ns
	$t_b \geq 200$ ns	t_r		0.1 t_b	ns
		t_f		0.1 t_b	ns

signal states are defined as the MARK or OFF state, where terminal A is negative with respect to terminal B, and the SPACE or ON state, where terminal A is positive with respect to terminal B. A summary of the specifications is contained in the preceeding table.

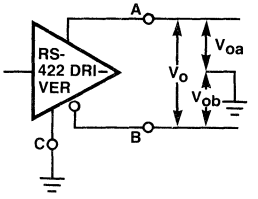


Fig. 6-2 Output Voltage — Open Circuit — Test Circuit (RS-422)

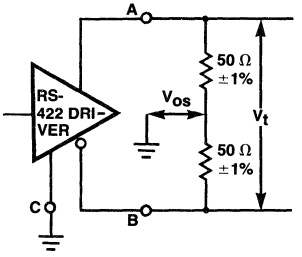


Fig. 6-3 Output Voltage — Terminated — Test Circuit (RS-422)

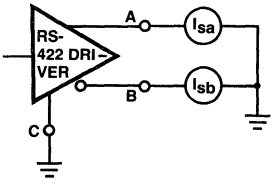


Fig. 6-4 Output Short Circuit Current — Test Circuit (RS-422)

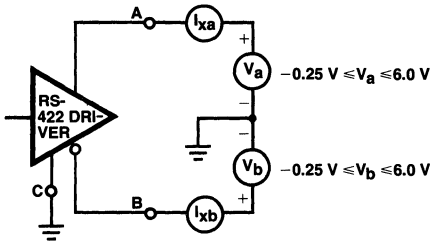


Fig. 6-5 Output Leakage Current — Power Off — Test Circuit (RS-422)

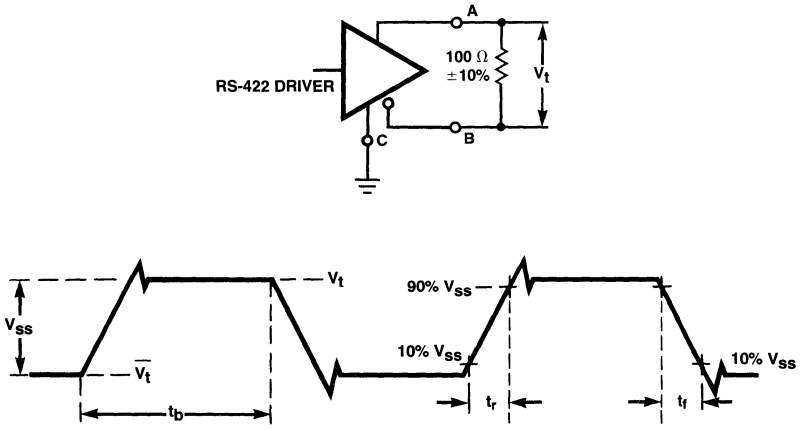


Fig. 6-6 Switching Test Circuit (RS-422)

In addition, the standard requires that the differential signal change monotonically in the transition region, defined as between the 10% and 90% points of the signal change, that any overshoot or undershoot be less than 10% of V_{SS}, and at no time outside of the transition region shall the instantaneous magnitude of V_t be greater than 6 volts or be less than 2 volts.

The fault conditions that a driver must withstand without damage, under either a power-on or power-off condition are:

a. Driver output open circuit
b. Differential output short circuit
c. Output short circuit to ground
d. Output short circuit to any other lead included in RS-422 and RS-423.

These fault conditions imply that the driver must withstand a 150 milliampere source with a voltage range of ±10 volts (signal plus common mode) being connected to its outputs.

The terminated output requirement ($|V_t| \geq 0.5|Vo|$) limits the combined output impedance of the differential outputs to less than 100 ohms. Variations in the total output impedance between output states are also limited. The output voltage matching specification ($|V_t| - |V_t| \leq 0.4$ V) restricts the change to

less than 20 ohms in the case of the open circuit output voltage magnitudes being equal. An output offset requirement ($|V_{OS}| \leq 3.0$ V) limits the amount of common mode signal the driver can generate. This requirement in conjunction with the offset matching specification further limits any mismatch between the voltage levels or impedances of the two outputs. The output current range has a specified maximum ($|I_S| \leq 150$ mA) and an implied minimum of 20 milliamperes required by the combination of the minimum signal (2.0 V) into a 100 ohm load.

The monotonicity requirement places a unique restriction on differential output circuits. It should be noted that unless the transitions of the individual outputs overlap, a flat or zero-slope region develops in the differential transition. While a zero-slope region, in itself, may not violate the monotonicity requirement, any ringing or system noise occurring at this point in time could. This requirement can be satisfied if the individual transition times are kept longer than the device propagation delays; but, this eventually compromises the system's maximum data rate. Closely matched propagation delays would permit high speed operation while insuring a monotonic differential signal.

RS-423 Driver (Unbalanced)

The generator or driver specified in RS-423 is a circuit with a low impedance, unbalanced, voltage source output that provides a signal of 4 to 6 V in magnitude. (Refer to *Figure 6-7*). The two signal states are defined as the MARK or OFF state when the A terminal of the driver is negative with respect to terminal C and the SPACE or ON state when the A terminal is positive with respect to terminal C. A summary of specifications is contained in the following table.

RS-423 DRIVER CHARACTERISTICS			LIMITS		
			MIN	MAX	UNITS
Output Voltage — Open Circuit: Vo (See Figure 6-8)		Vo(space)	4.0	6.0	V
		Vo(mark)	−6.0	−4.0	V
Output Voltage — Terminated: V_t (See Figure 6-9)		|Vt|	4.0		V
			0.9 Vo		V
Output Short Circuit Current: Is (See Figure 6-10)		Is	−150	150	mA
Output Leakage Current — Power Off: Ix (See Figure 6-11) (−6.0 V ≤ Vx ≤ 6.0 V)		Ix	−100	100	μA
Transition Times: t_r, t_f (See Figure 6-12)	$t_b > 1.0$ ms	t_r	100	300	μs
		t_f	100	300	μs
	$t_b \leq 1.0$ ms	t_r	0.1 t_b	0.3 t_b	μs
		t_f	0.1 t_b	0.3 t_b	μs

In addition, the standard requires that the signal change monotonically in the transition region, defined as the 10% to 90% portion of the signal change, that any overshoot or undershoot be less than 10% of the signal amplitude, and that at no time, after the transition region is traversed, shall the instantaneous magnitude of V_{SS} be greater than 6 V or less than 4 V.

The fault conditions this driver must withstand in either a power-on or power-off condition are:

a. Driver output open circuit
b. Output short circuit to ground
c. Output short circuit to signal return
d. Output short circuit to any other lead included in RS-422 or RS-423

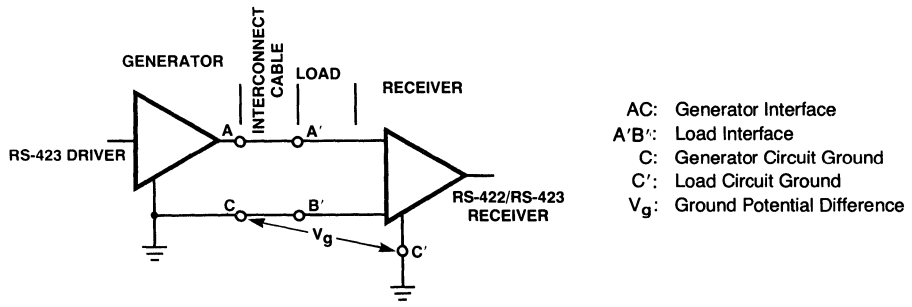


Fig. 6-7 RS-423 Unbalanced Interface Circuit

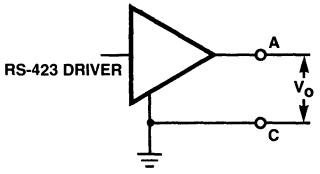


Fig. 6-8 Output Voltage — Open Circuit — Test Circuit (RS-423)

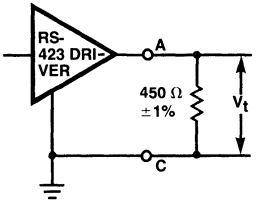


Fig. 6-9 Output Voltage — Terminated — Test Circuit (RS-423)

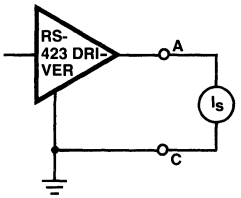


Fig. 6-10 Output Short Circuit Current Test Circuit (RS-423)

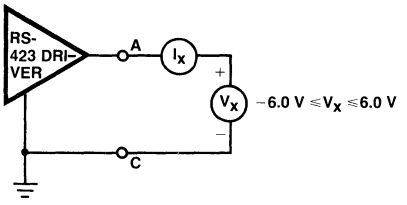


Fig. 6-11 Output Leakage Current — Power Off — Test Circuit (RS-423)

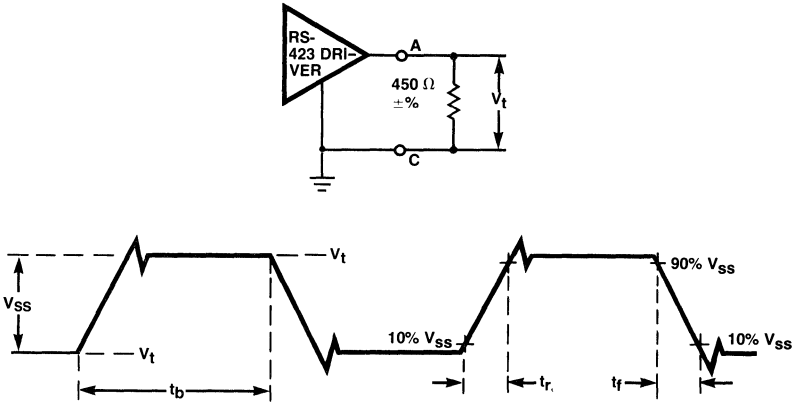


Fig. 6-12 Switching Test Circuit (RS-423)

As with the balanced driver, this implies that the unbalanced driver must withstand a 150 mA source with a voltage range of ± 10 V being connected to its output.

The unbalanced driver output impedance is established by the terminated output specification ($|V_t| > 0.9\ V_O$). Since there are no output matching or offset requirements, there are no restrictions on output impedance or voltage levels matching between output states. If, however, the driver requires an external waveshaping method which incorporates an external resistor, then a mismatch between states in the output impedance could be of consequence. The output current range has a specified maximum ($|I_S| \leq 150$ mA) and an implied minimum of 7.8 milliamperes required by the combination of a minimum signal (4.0 V) into a 450 Ω load.

Since this is not a differential output device, the monotonicity requirements are not as complex as in the case of the balanced driver. However, concern must be given to the amount of crossover distortion permitted during transitions.

RS-422/RS-423 Receiver

The standards RS-422 and RS-423 are written to have identical receiver specifications such that a single device design could satisfy both standards. Such a receiver would operate in the balanced system (RS-422) between the differential outputs of the driver and in the unbalanced system (RS-423) between the driver output and the signal common return. The receiver specified in RS-422 and RS-423 is a differential circuit with balanced input impedance larger than 4 kilohms and a differential input threshold magnitude less than 200 mV over a ±7 Vcommon mode range. A summary of the specifications is contained in the following table.

RS-422/RS-423 RECEIVER CHARACTERISTICS		LIMITS		
		MIN	MAX	UNITS
Input Current: Iia, Iib (See Figure 6-14) (−10 V ≤Via ≤10 V; Vib=0) (−10 V ≤Vib ≤10 V; Via=0) (Iia and Iib must be in the shaded portion of the graph.)	 Iia Iib	(See Figure 6-14)		 mA mA
Differential Input Voltage — Threshold: Vth (See Figure 6-15) (−7.0 V ≤ Vcm ≤7.0 V)	 Vth	−200	200	mV
Differential Input Voltage — Threshold Balance: (See Figure 6-16) (−7.0 V ≤Vcm ≤7.0 V)	Vth Bal Vth Bal	−400	400	mV
Differential Input Voltage — Operating Range: (See Figure 6-17)	Vdiff Vdiff	−6.0	6.0	V
Differential Input Voltage — Maximum: (See Figure 6-17)	Vdiff max Vdiff max	−12.0	12.0	V
Input Voltage — Maximum: (See Figure 6-17)	Via Vib	−10 −10	10 10	V V

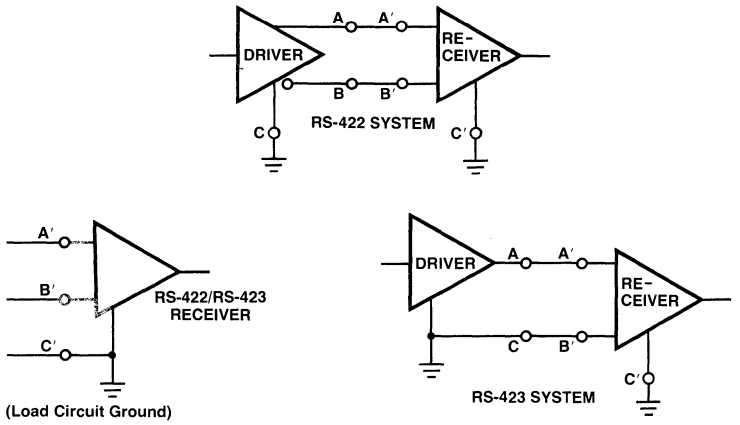


Fig. 6-13 RS-422/RS-423 Receiver

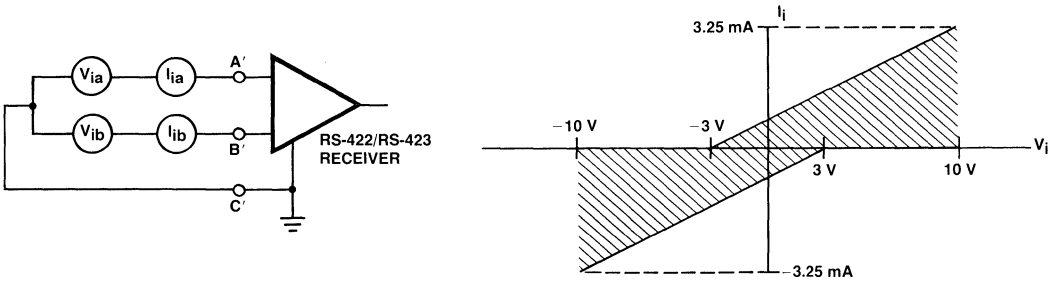


Fig. 6-14 Input Current — Voltage Test Circuit (RS-422/RS-423)

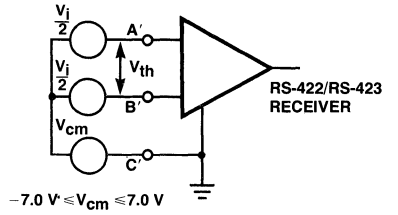


Fig. 6-15 Differential Input Voltage — Threshold — Test Circuit (RS-422/RS-423)

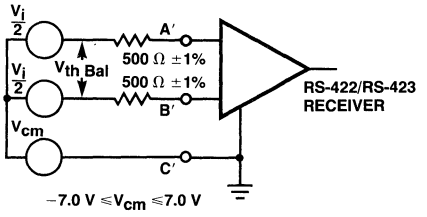


Fig. 6-16 Differential Input Voltage — Threshold Balance — Test Circuit (RS-422/RS-423)

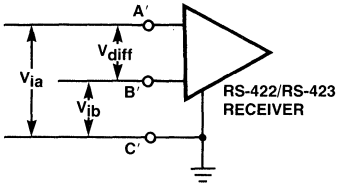


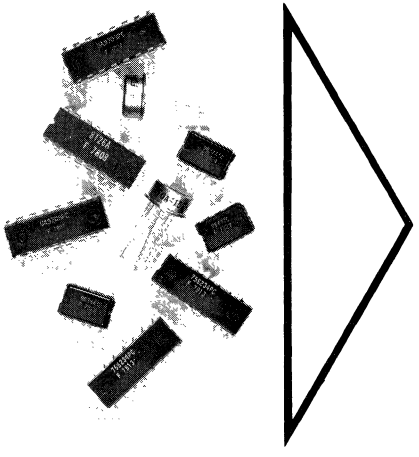
Fig. 6-17 Input Voltage Test Circuit (RS-422/RS-423)

The graph used to specify the input current voltage characteristic of the receiver limits the input resistance to be greater than 4 kilohms when there exists a ± 3 V bias in the driver. Permitting an internal bias allows receivers to be designed that require only a single power supply for operation. The input balance requirement restricts not only the input threshold accuracy of the receiver, but also any mismatch of its input resistance.

New Products

Efforts are ongoing at Fairchild to develop a family of products satisfying these standards. The first of these announced products are:

9634 Dual 3-State Differential Line Driver (RS-422 Driver)
9638 Dual Differential Line Driver (RS-422 Driver)
9636A Dual Single-Ended Line Driver (RS-423 Driver)
9637A Dual Differential Line Receiver (RS-422/RS-423 Receiver)



ORDER INFORMATION, DICE POLICY AND PACKAGE OUTLINES

ORDER INFORMATION

Three basic units of information are contained in the code.

9636A	T	C
Device Type	Package Type	Temperature Range

DEVICE TYPE

This group of alpha numeric characters defines the data sheet which specifies the device functional and electrical characteristics.

PACKAGE TYPE

One letter represents the basic package style.

- D = Dual In-line Package (Hermetic, Ceramic)
- F = Flatpak (Hermetic)
- H = Metal Can Package
- J = Metal Power Package (TO-66 Outline)
- K = Metal Power Package (TO-3 Outline)
- P = Dual In-line Package (Molded)
- R = Mini DIP (Hermetic, Ceramic)*
- T = Mini DIP (Molded)
- U = Power Package (Molded, TO-220 Outline)

*Refer to individual data sheets for details. For special requirements, contact factory.

Different outlines exist within each package style to accommodate various die sizes and number of leads. Specific dimensions for each package can be found in the PACKAGE OUTLINES section of this catalog.

TEMPERATURE RANGE

Two basic temperature grades are in common use:

C = Commercial/Industrial/Consumer	M = Military
0°C to +70/75°C	−55°C to +125°C
−20°C to +85°C	−55°C to + 85°C
−40°C to +60°C	
−40°C to +85°C	

Exact values and conditions are indicated on the individual data sheets.

EXAMPLES

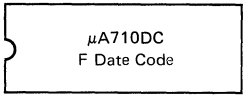
1. μA710FM
   This number code indicates a μA710 Voltage Comparator in a flatpak with military temperature rating capability.

2. μA725EHC
   This number code indicates a μA725 Instrumentation Operational Amplifier, electrical option E, in a metal can with a commercial temperature rating capability.

3. μA725EHCG
   This number code indicates the identical device as in example 2. Except it has a gold plated kovar header; the standard header is tin dipped.

DEVICE IDENTIFICATION/MARKING

All Fairchild standard catalog linear circuits will be marked as the following example:



UNIQUE 38510 PROCESSING

Additional processing to Fairchild Unique 38510 specifications is indicated by noting the appropriate requirements (QB, QC) after the standard order code.

Detailed ordering procedures are provided in the OEM price list.

MATRIX VI PROGRAM

Additional screening to the Fairchild Matrix VI program is indicated by the QM or QR suffix to the standard order code.

OLD ORDER CODES

Devices may continue to be purchased against old order codes (Example: U5R7723393; now 723HC). However, all products will be marked with new order codes unless otherwise specified.

DICE POLICY

GENERAL INFORMATION

Fairchild linear integrated circuits, constructed using the Fairchild Planar* epitaxial process, are available in dice form incorporating these features:

- Commercial or Military Selection (Military Limits Probed at 25°C)
- MIL-STD-883, Method 2010.2, Condition B Visual
- Gold Backing
- Glass Passivation
- Protective Packaging

ELECTRICAL CHARACTERISTICS

Each die electrically tested at 25°C to guarantee commercial dc parameters.

Military grade dice are guardband tested at 25°C dc to guarantee military temperature range operation.

QUALITY ASSURANCE

All Fairchild linear dice are 100% visually inspected and conform to MIL-STD-883, Method 2010.2, Condition B. In addition, quality control visually inspects the dice to a given sampling plan.

Each die is gold backed to aid die attach. Most diec are available with glass passivation coating with only the bonding pads exposed.

SHIPPING PACKAGES

Linear dice are packaged in containers with an anti-static sheet inserted between the lid and the dice. This sheet guards against electrostatic damage during shipment and storage.

The clear plastic carrier allows visual inspection of all the packaged dice. Each carrier is heat sealed within a transparent bag. A small piece of dehydrator paper with humidity indicating color is inserted in each bag prior to sealing.

ORDER INFORMATION

Each linear integrated circuit die has a unique order code which describes the device type, the dice designation and type of electrical tests performed. The dice designation is denoted by a "C" and wafer designation is denoted by a "W." Examples follow:

Generic Type	Dice Order Code	Wafer Order Code
μA741C**	μA741CC	μA741WC
μA3045	μA3045CC	μA3045WC
75450B	75450BCC	75450BWC
μA101A	μA101ACC	μA101AWC
μA796C	μA796CC	μA796WC

**Some device types imply a military or commercial range by the generic type. Where this does not occur the suffix should be:

XM Military Grade Die or XC Commercial Grade Die

SPECIAL CHIP PROCESSING

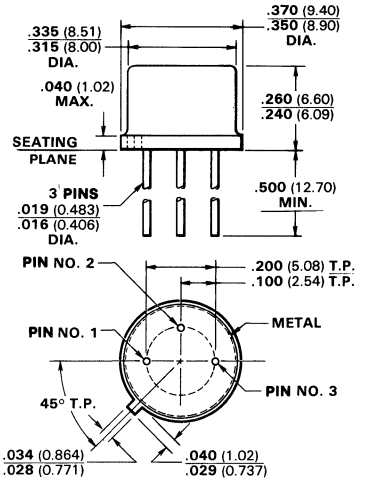
If there is a need for additional testing or processing, Fairchild will negotiate with the customer to meet his requirements.

PRODUCT AVAILABLE IN DICE FORM

Please refer to FSC OEM Price List for product available in die form.

*Planar is a patented Fairchild process.

In Accordance with JEDEC (TO-39) OUTLINE



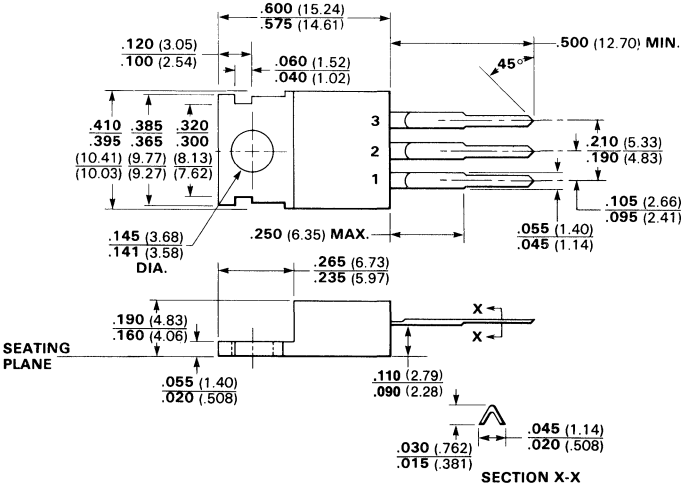
BF

NOTES:
Pins are gold-plated kovar
Pin 3 connected to case
50 mil kovar header
Package weight is 1.23 grams

5K

NOTES:
Pins are gold-plated kovar
Pin 3 connected to case
50 mil kovar header
Package weight is 1.23 grams

In Accordance with JEDEC (TO-220) OUTLINE



EC

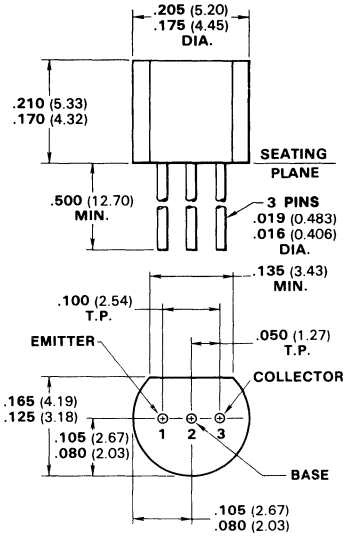
NOTES:
Package is silicone plastic with boron nickel-plated copper tab and pins
Mechanically interchangable with TO-66
Center pin is electrical contact with the mounting tab
Package weight is 2.1 grams

GH

NOTES:
Package is silicone plastic with nickel-plated copper tab and pins
Center pin is electrical contact with the mounting tab
Package weight is 2.1 grams
*Mechanically interchangable with TO-66

All dimensions in inches (bold) and millimeters (parentheses)

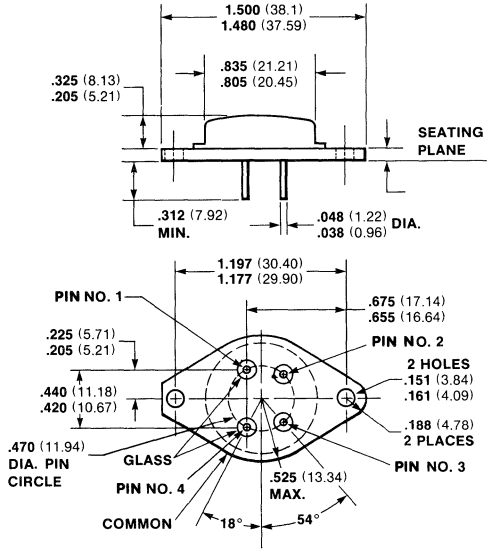
In Accordance with JEDEC TO-92 OUTLINE



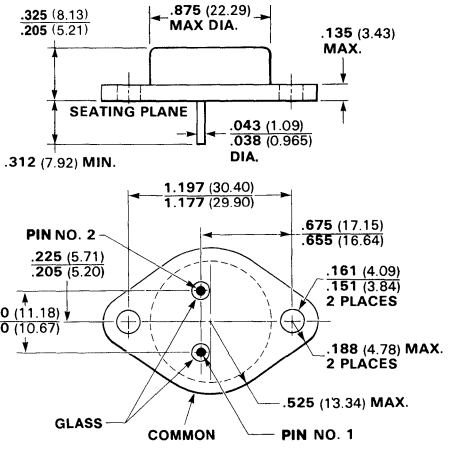
EI

NOTES:
Pins are tin-plated copper
Package material is transfer molded thermosetting plastic
ECB configuration
Package weight is 0.25 gram

In Accordance with JEDEC (TO-3) OUTLINE-4-PIN



JEDEC TO-3 OUTLINE*



GJ

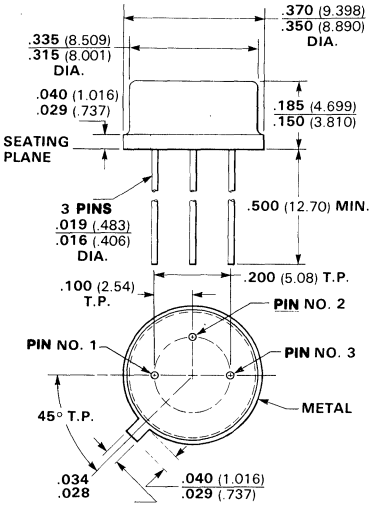
NOTES:
Pins are gold-plated or solder dipped alloy 52
Pins 1 and 2 electrically isolated from case
Case is third electrical connection
Aluminum package with copper slug, pins are soldered in
Package weight is 7.4 grams
Aluminum cap (may be dome-type, depending prod. line)
*Except pin diamater

GK

NOTES:
Pins are gold-plated or solder dipped alloy 52
All pins electrically isolated from case
Package weight is 7.4 grams
*Except number of pins and pin diameter

All dimensions in inches (bold) and millimeters (parentheses)

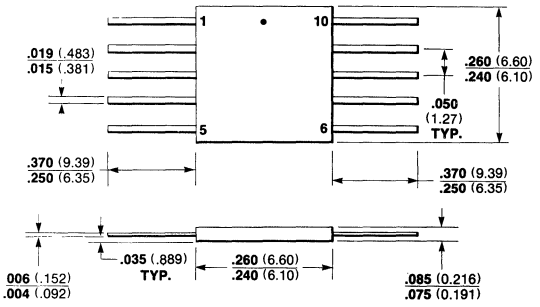
JEDEC TO-39 OUTLINE*



HC

NOTES:
Pins are gold-plated kovar
Pin 3 connected to case
Package weight is 1.23 grams
50 mil kovar header
*Dimensions same as JEDEC TO-39 except for can height

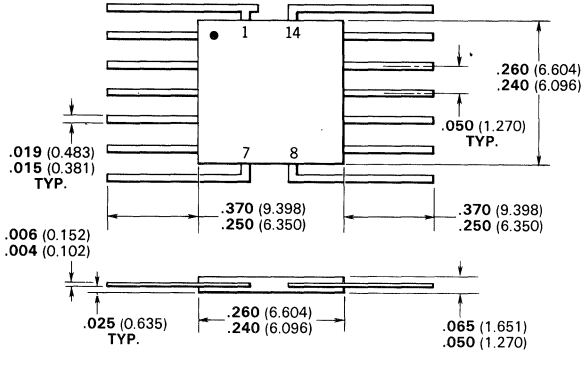
In Accordance with
JEDEC (TO-91) OUTLINE
10-PIN CERPAK



3F

NOTES:
Pins are tin plated 42 alloy
Hermetically sealed alumina package
Cavity size is .130 diamater
Package weight is 0.26 grams

In Accordance with
JEDEC (TO-86) OUTLINE
14-PIN CERPAK

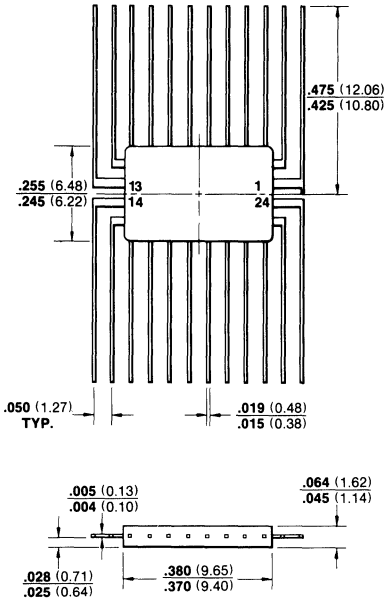


3I

NOTES:
Pins are tin-plated 42 alloy
Hermetically sealed alumina package
Pin 1 orientation may be either tab or dot
Cavity size is .130
Package weight is 0.26 gram

All dimensions in inches (bold) and millimeters (parentheses)

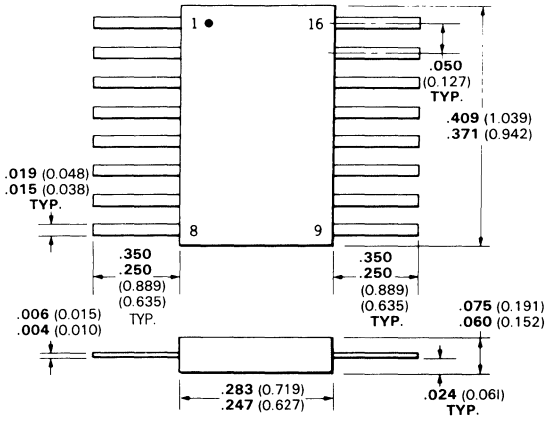
24-PIN FLATPAK



3M

NOTES:
Pins are gold-plated kovar
Package material is kovar
Cavity size is .120 x .235 (3.05 x 5.97)
Package weight is 0.8 gram

16-PIN CERPAK



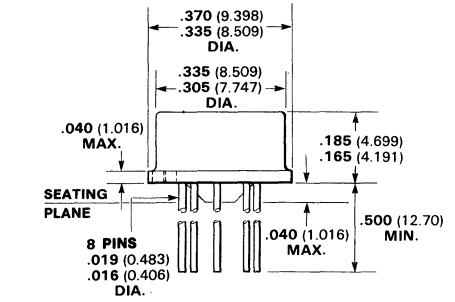
4L

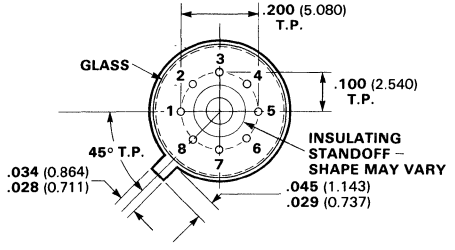
NOTES:
Pins are alloy 42
Package weight is 0.4 gram
Hermetically sealed beryllia package

11

All dimensions in inches (bold) and millimeters (parentheses)

In Accordance with
JEDEC (TO-99) OUTLINE





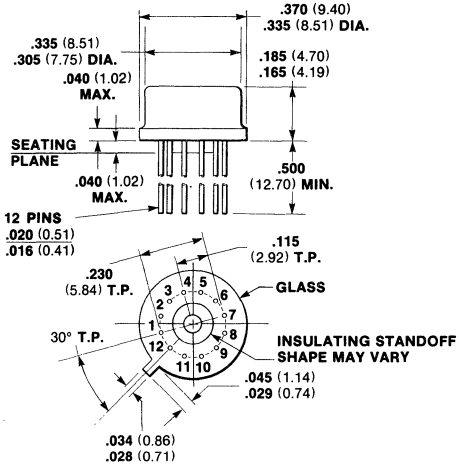
5B

NOTES:
Pins are gold-plated kovar
Seven pins thru leads No. 4 connected to case
15 mil kovar header
Package weight is 1.22 grams

5L

NOTES:
Pins are gold-plated kovar
Eight pins thru
15 mil kovar header
Package weight is 1.22 grams

JEDEC TO-101 OUTLINE

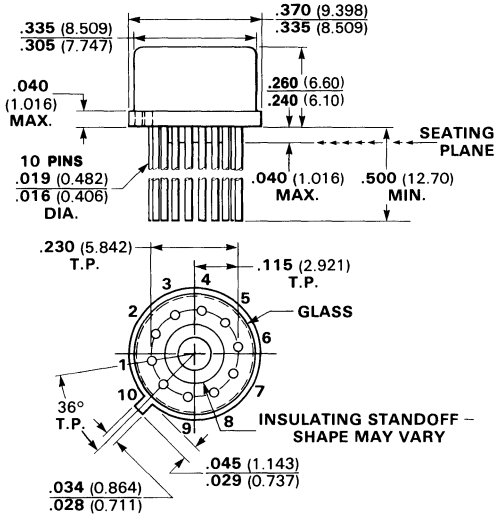


5D

NOTES:
Pins are solder dipped to the seating plane.
Twelve pins thru
*Similar to JEDEC TO-101
Package weight is 1.4 grams

All dimensions in inches (bold) and millimeters (parentheses)

In Accordance with
JEDEC (TO-100) OUTLINE



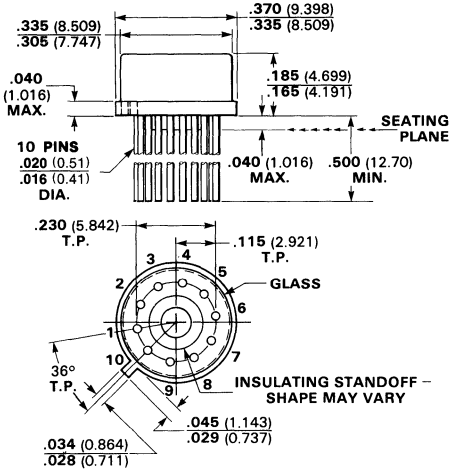
5E

NOTES:
Pins are gold-plated kovar
Ten pins thru
15 mil kovar header
Package weight is 1.32 grams

5F

NOTES:
Pins are gold-plated kovar
Nine pins through, pin 5 connected to case
15 mil kovar header
Package weight is 1.32

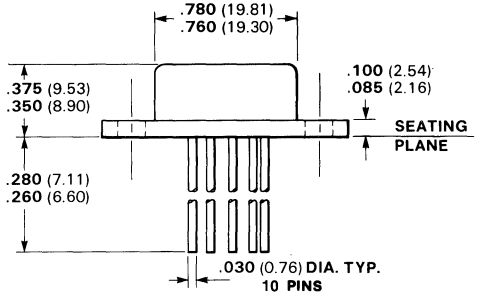
JEDEC TO-100 OUTLINE

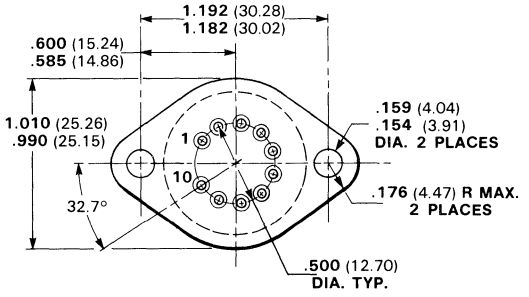


5G

NOTES:
Pins are gold-plated kovar
Twelve pins thru
*Similar to JEDEC TO-101
Package weight is 1.08 grams

JEDEC TO-3 OUTLINE*





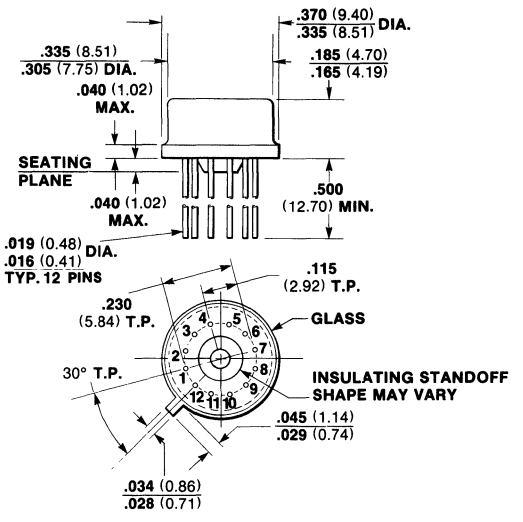
5H

NOTES:
Package material is nickel-plated CRS
Pin material is alloy 52
Glass material is corning 9010
Pin, post and base gold-plated
*Except height and number of pins

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

In Accordance with JEDEC (TO-100) OUTLINE



5I

NOTES:
Pins are solder dipped to the seating plane
Ten pins thru
High RTH package
15 mil kovar header
Package weight is 1.32 grams

5N

NOTES:
Pins are solder-dipped to the seating plane
Nine pins through, pin 5 connected to case
15 mil kovar header
Package weight is 1.32 grams

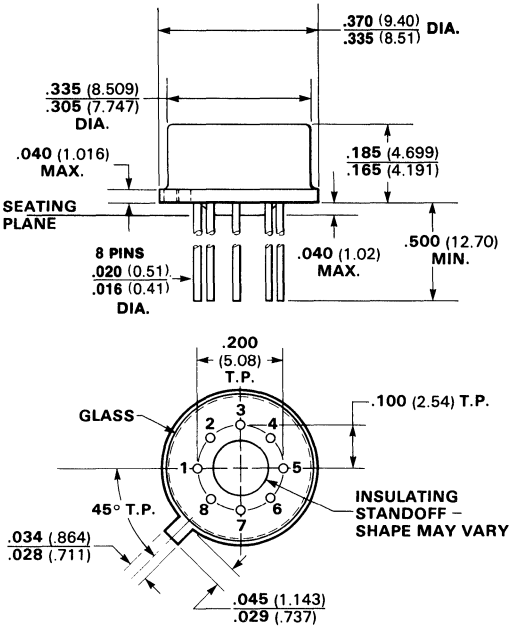
5Q

NOTES:
Pins are solder dipped to the seating plane
Ten pins thru
15 mil kovar header
Package weight is 1.32 grams

5U

NOTES:
Pins are gold-plated kovar
Ten pins through
High RTH package
15 mil kovar header
Package weight is 1.32 grams

In Accordance with JEDEC (TO-99) OUTLINE



5M

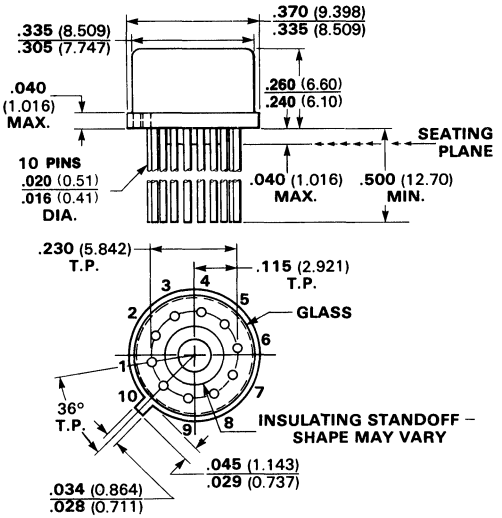
NOTES:
Pins are solder dipped to seating plane
Eight pins thru
15 mil kovar header
Package weight is 1.22 grams

5T

NOTES:
Pins are gold-plated kovar
Eight pins thru
*Dimensions similar to JEDEC TO-100
except for 8 pins spaced 45° apart.
Package weight is 1.22 grams.

All dimensions in inches (bold) and millimeters (parentheses)

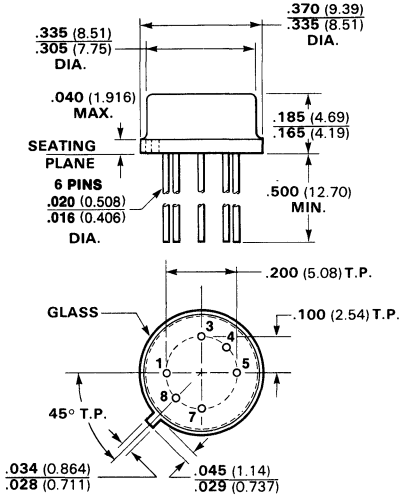
JEDEC TO-96 OUTLINE*



5R

NOTES:
Pins are gold-plated kovar.
Nine pins thru, Pin No. 5 is connected to case
15 mil kovar header
Package weight is 1.32 grams.
*Dimensions similar to JEDEC TO-96 except for standoff.

In Accordance with
JEDEC TO-78 OUTLINE



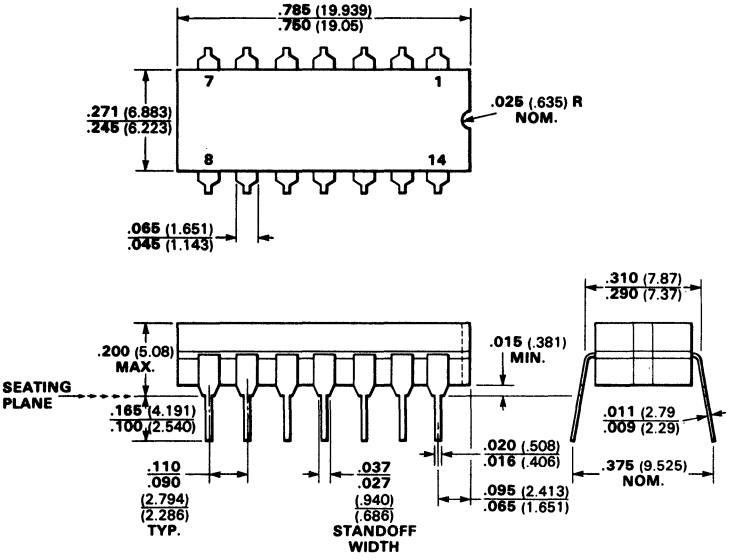
5Z

NOTES:
Pins are gold plated kovar.
Six pins thru.
Pins 2 and 6 are omitted.
Package weight is 0.95 gram.

All dimensions in inches (bold) and millimeters (parentheses)

PACKAGE OUTLINES

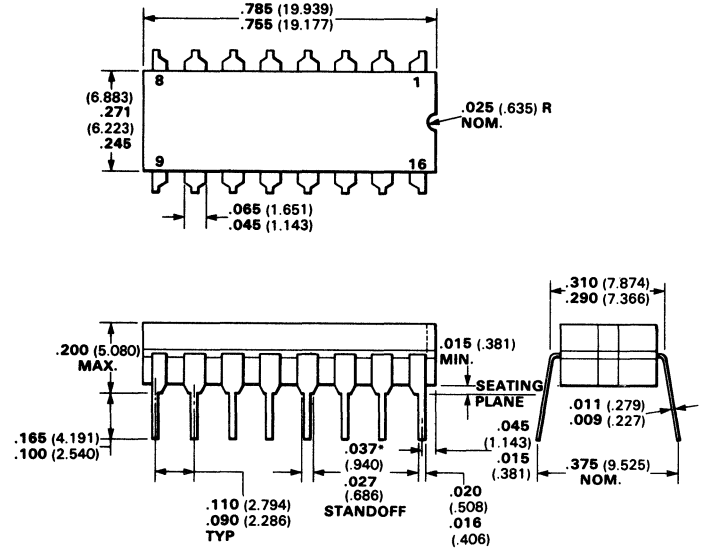
In Accordance with
JEDEC (TO-116)
14-PIN HERMETIC DUAL IN-LINE



6A

NOTES:
Pins are intended for insertion in hole rows on .300" (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin
Pins are alloy 42
Package weight is 2.0 grams

16-PIN HERMETIC DUAL IN-LINE

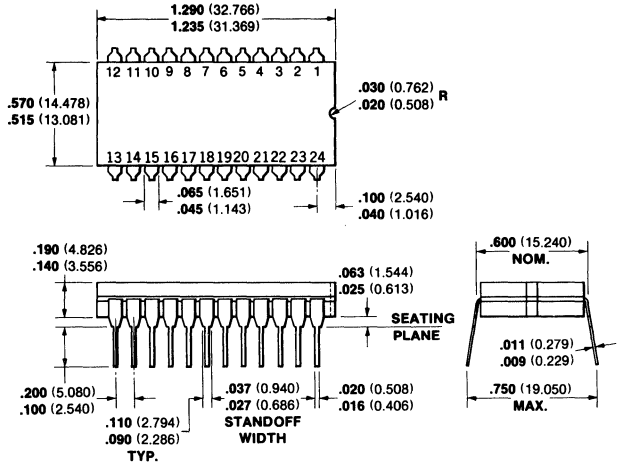


6B

NOTES:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" centers (7.62)
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin (0.51)
Hermetically sealed alumina package
Cavity size is .110 x .140 (2.79 x 3.56)
Package weight is 2.0 grams
*The .037-.027 dimension does not apply to the corner pins

All dimensions in inches (bold) and millimeters (parentheses)

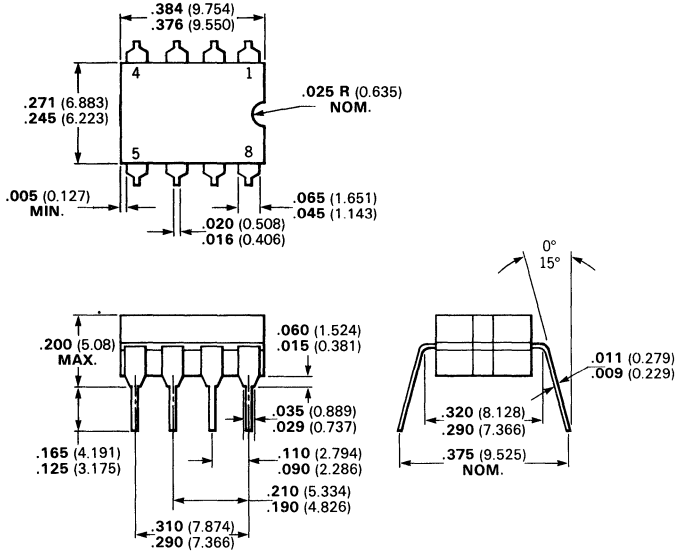
24-PIN DUAL IN-LINE



6N

NOTES:
Pins are tin-plated 42 alloy
Package material is alumina
Pins are intended for insertion in hole rows on .600 (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is .230 x .230 (5.84 x 5.84)
Package weight is 6.5 grams

8-PIN DUAL IN-LINE



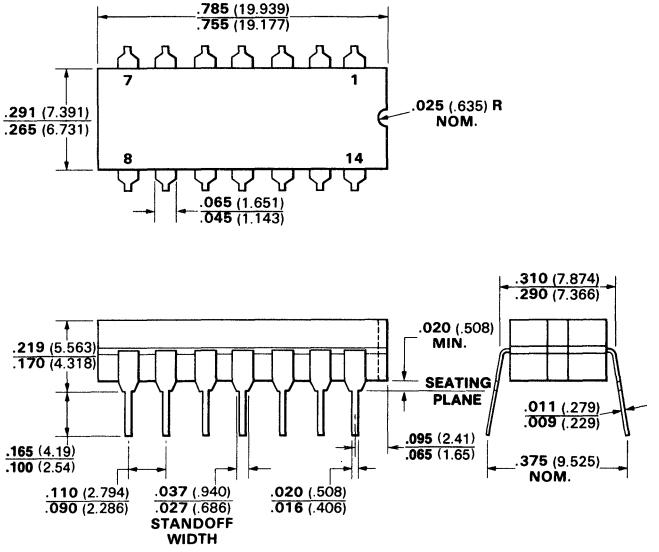
6T

NOTES:
Pins are tin-plated kovar
Pins are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Hermetically sealed alumina package
Cavity size is .110 x .140
Package weight is 1.0 grams

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

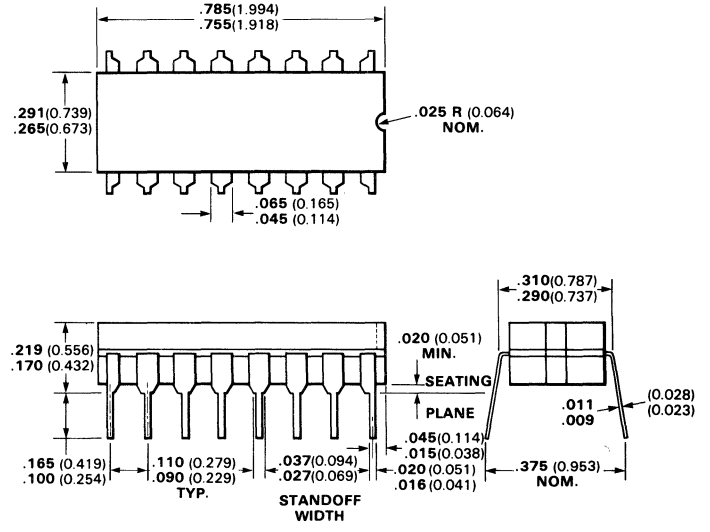
In Accordance with
14-PIN DUAL IN-LINE
(JEDEC TO-116 OUTLINE)



7A

NOTES:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" (7.62) centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for a conventional .020" (0.51) diameter pin.
Hermetically sealed alumina package.
Cavity size is .130 x .250 (3.30 x 6.35)
*Similar to JEDEC TO-116 except for package width.
Package weight is 2.2 grams.

16-PIN DUAL IN-LINE

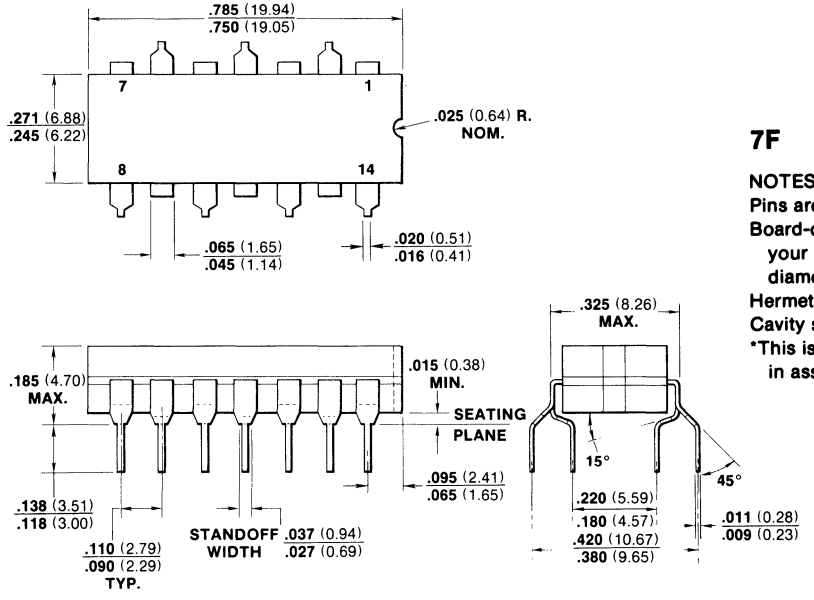


7B

NOTES:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" (7.72) centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin (0.51)
Hermetically sealed alumina package
Cavity size is .130 x .230
*The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.2 grams

All dimensions in inches (bold) and millimeters (parentheses)

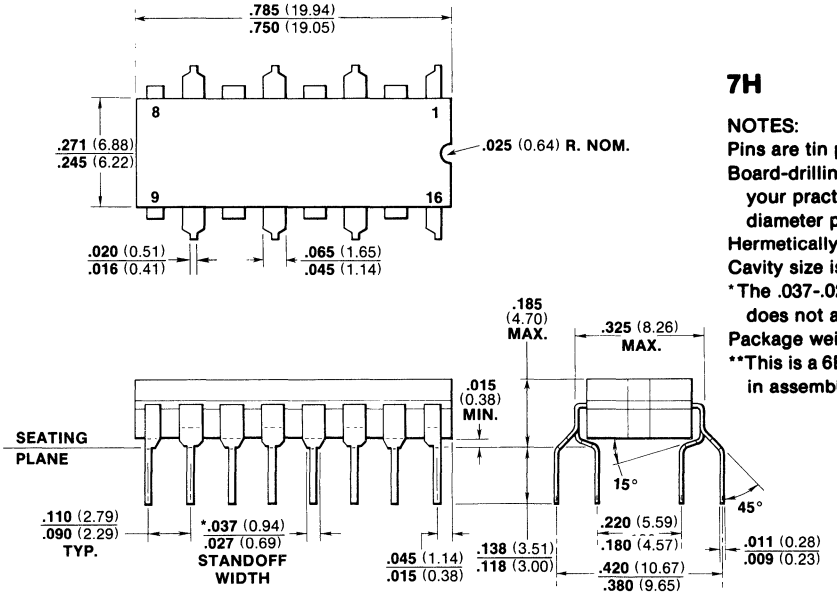
14-PIN QUAD IN-LINE (JEDEC TO-116 OUTLINE)*



7F

NOTES:
Pins are tin-plated kovar
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Hermetically sealed alumina package
Cavity size is .110 x .140 (2.79 x 3.56)
*This is a 6A package with the pins formed in assembly

16-PIN QUAD** IN-LINE



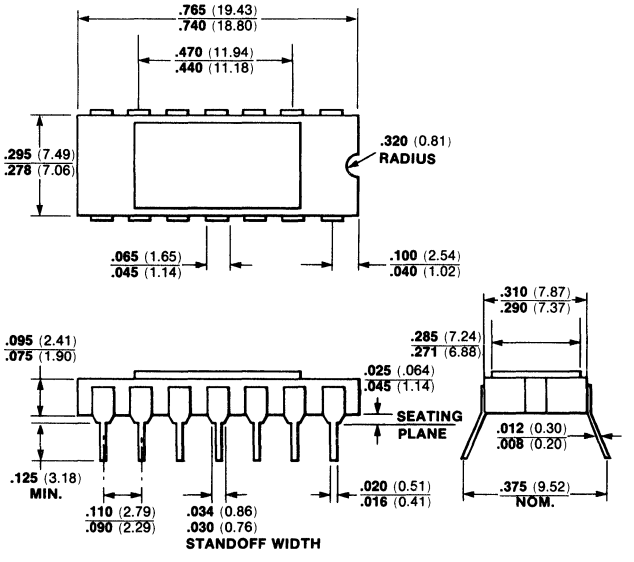
7H

NOTES:
Pins are tin plated kovar
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Hermetically sealed alumina package
Cavity size is .110 x .140 (2.79 x 3.56)
*The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.0 grams.
**This is a 6B package with the pins formed in assembly.

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

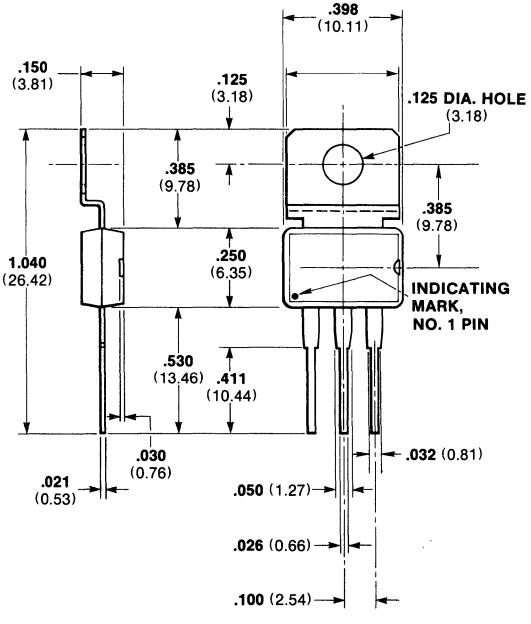
14-PIN DUAL IN-LINE (METAL CAP)



7N

NOTES:
Pins are gold-plated kovar
Package material is alumina
Pins are intended for insertion in hole rows on .300" centers (7.62)
They are purposely shipped "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Low temperature seal
Cavity size is .170 x .215 (4.32 x 5.46)
Package weight is 1.3 grams.

3-PIN SINGLE SIDE POWER PLASTIC MINIDIP

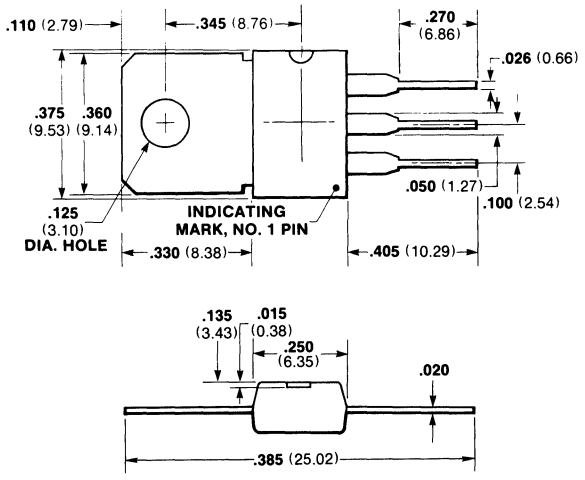


8Y (U-1)

NOTES:
Pins are tin plated copper
Package weight is 0.6 gram
Package material is plastic
Tab is electrically insulated from pins
This package is intended to be mounted with the tab flush with the top of the P.C. board or heat sink. A No. 4 screw may be used to secure the package. Thermal compound is recommended.
All dimensions nominal.

All dimensions in inches (bold) and millimeters (parentheses)

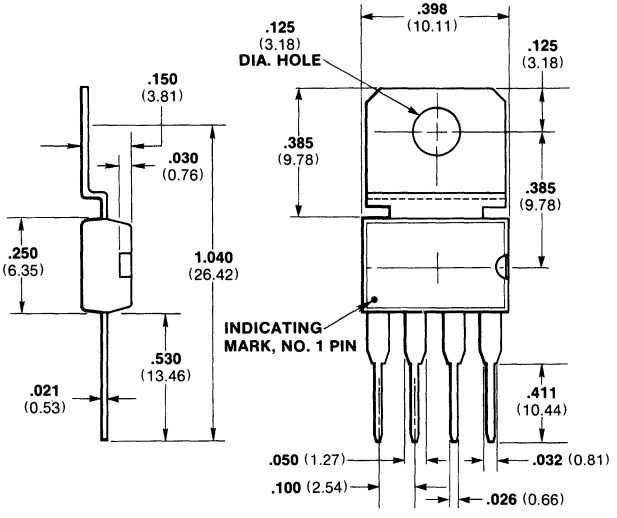
3-PIN SINGLE SIDE POWER PLASTIC MINIDIP



8Y (U-2)

NOTES:
Pins are tin plated copper
Package weight is 0.6 grams
Package material is plastic
Center pin is electrical contact with mounting tab
For detailed package configuration, refer to FSB-90717
All dimensions nominal

4-PIN SINGLE SIDE POWER PLASTIC MINIDIP



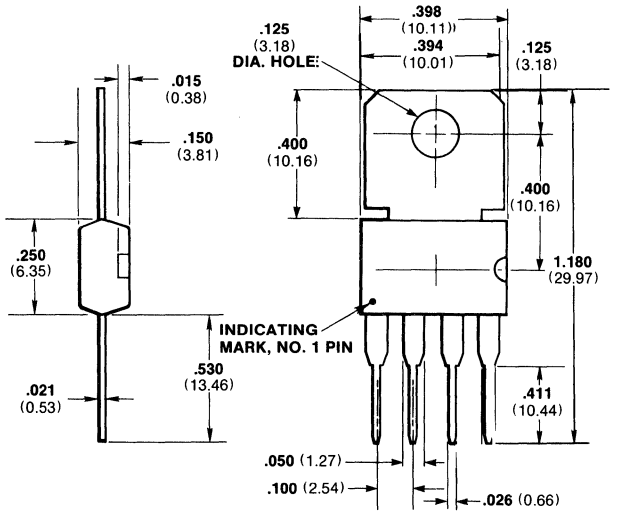
8Z (U-1)

NOTES:
Package is plastic with tin-plated copper pins
Board-drilling dimensions should equal your practice for .033 (0.84) inch diameter pins
Package weight is 0.6 gram
Tab is electrically insulated from pins
This package is intended to be mounted with the tab flush with the top of the PC board or heat sink. A No. 4 screw may be used to secure the package. Thermal compound is recommended.

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

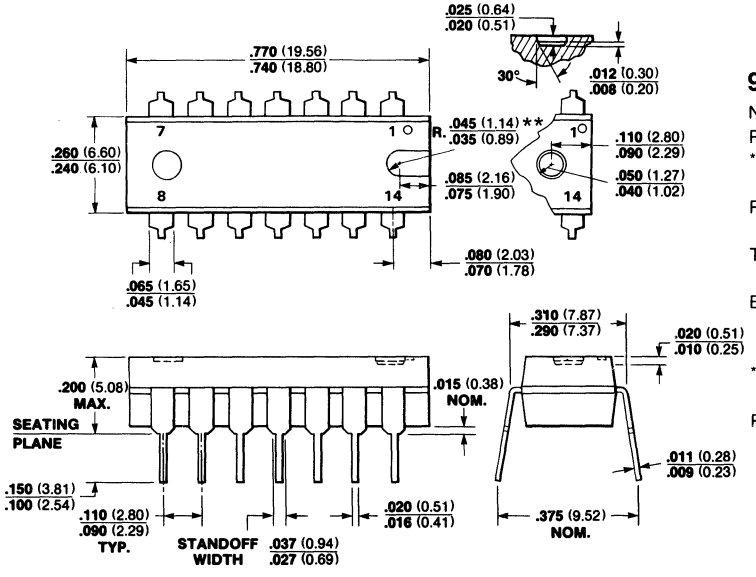
4-PIN SINGLE SIDE POWER PLASTIC MINIDIP



8Z (U-2)

NOTES:
Package is plastic with tin-plated pins
Board-drilling dimensions should equal your practice for .033 (0.84) inch diameter pin
Package weight is 0.6 gram
Tab is electrically insulated from pins

In Accordance with 14-PIN *PLASTIC DUAL IN-LINE (JEDEC TO-116 OUTLINE)

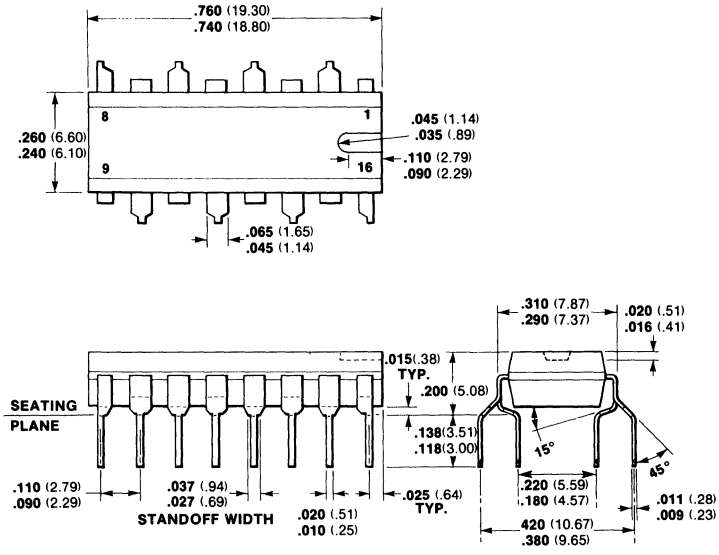


9A

NOTES:
Pins are tin plated kovar
*Package material varies depending on the product line
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.508) inch diameter pin
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 gram

All dimensions in inches (bold) and millimeters (parentheses)

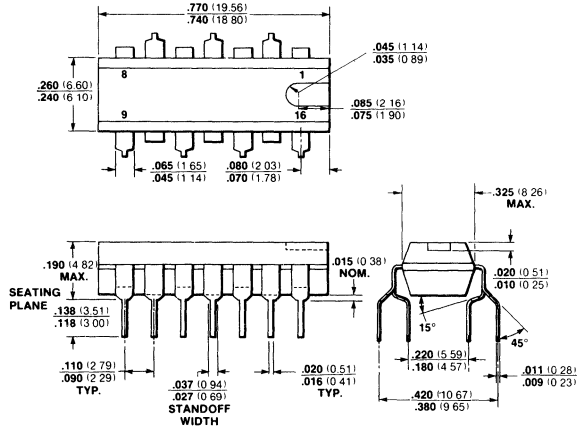
16-PIN PLASTIC* DUAL IN-LINE



9B

NOTES:
Pins are tin-plated kovar or alloy 42 nickel.
Pins are intended for insertion in hole rows on .300" (7.62) centers
Pins purposely have a "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch (0.51) diameter pin
Package weight is 0.9 gram
*Package material varies depending on the product line
***The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
**Notch or ejector hole varies depending on the product line

14-PIN PLASTIC QUAD IN-LINE (JEDEC TO-116 OUTLINE*)



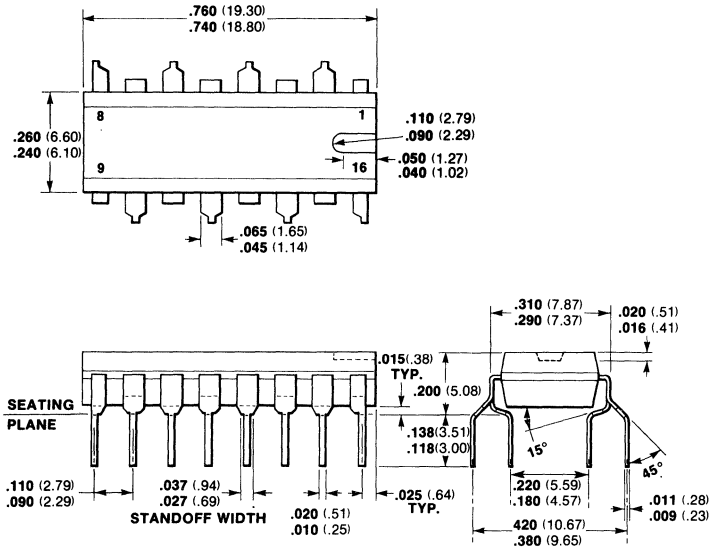
9C

NOTES:
Package is epoxy with tin-plated kovar pins
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Package weight is 0.9 gram
*This is a 9A package with the pins formed in assembly. Only the notched and epoxy version is used

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

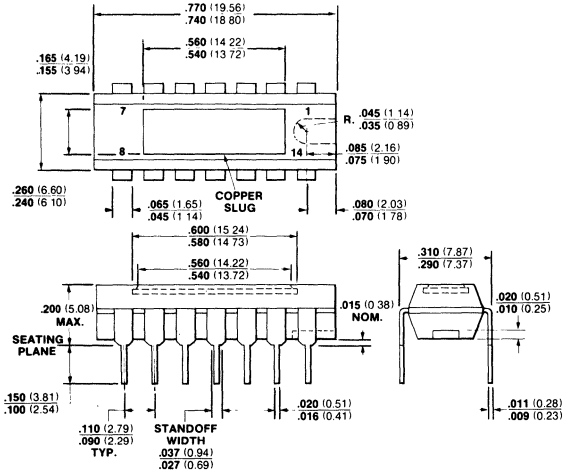
16-PIN MOLDED QUAD IN-LINE
9D QUAD PACKAGE FOR ALL
TAA, TBA, TDA TYPES



9D

NOTES:
Pins are tin-plated copper
Pins are intended for insertion in hole rows on .300" (7.62) centers
Board-drilling dimensions should equal your practice for .020 inch (0.51) diameter pin
Package weight is 0.9 gram
*Package material varies depending on the product line
**The .037-.027 (0.94-0.69) dimension does not apply to the corner pins

14-PIN PLASTIC DUAL IN-LINE
(WITH COPPER SLUG)

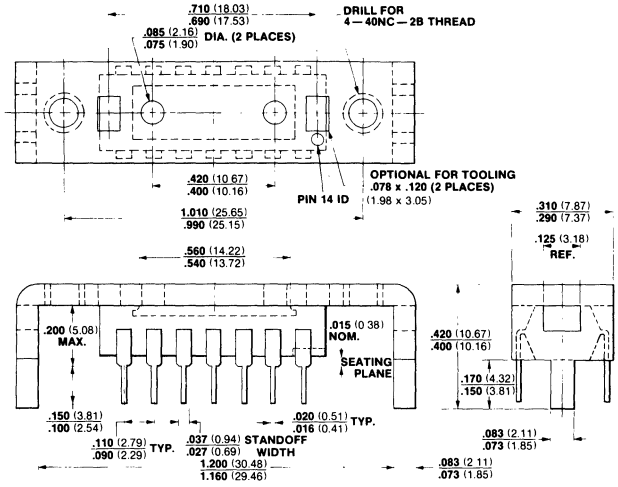


9H

NOTES:
Pins are gold-plated kovar
Board-drilling dimensions should equal your practice for .020 (0.51) inch diamater pin
Package material is epoxy with copper slug
Package weight is 0.9 gram

All dimensions in inches (bold) and millimeters (parentheses)

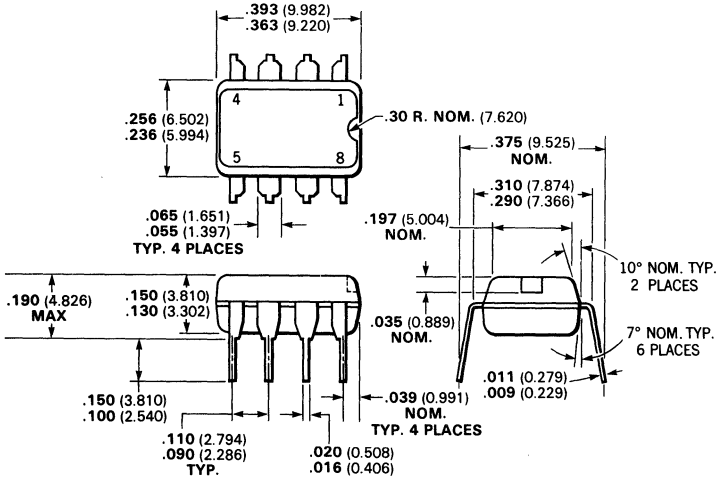
14-PIN PLASTIC DUAL IN-LINE (COPPER SLUG AND HEAT BRACKET)*



9J

NOTES:
Pins are gold-plated kovar
Package material is epoxy with copper slug and tin-plated copper bracket
Board-drilling dimensions should equal your practice for .020 (0.51) diameter pin
*Package is the same as 9H except that a heat bracket is attached

8-PIN PLASTIC DUAL IN-LINE



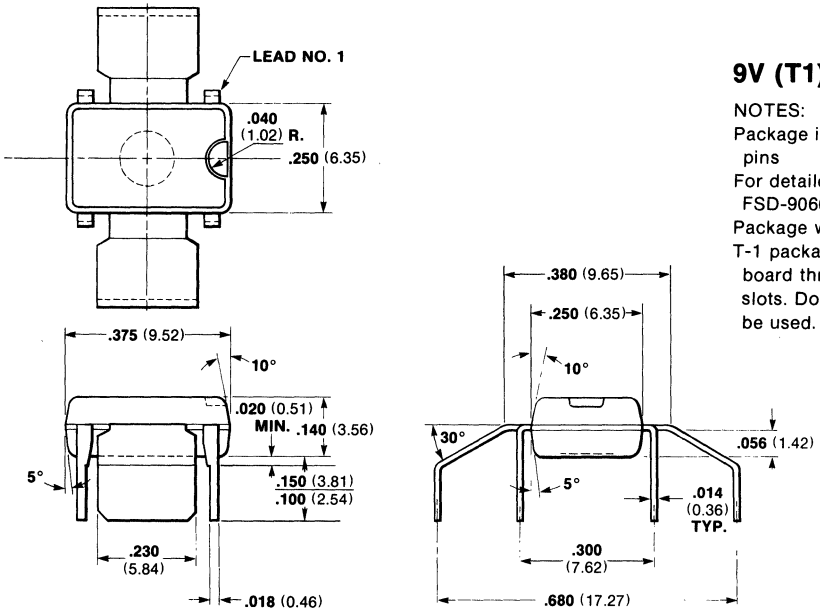
9T

NOTES:
Pins are tin or gold-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.51) inch diamater pin
Package weight is 0.6 gram

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

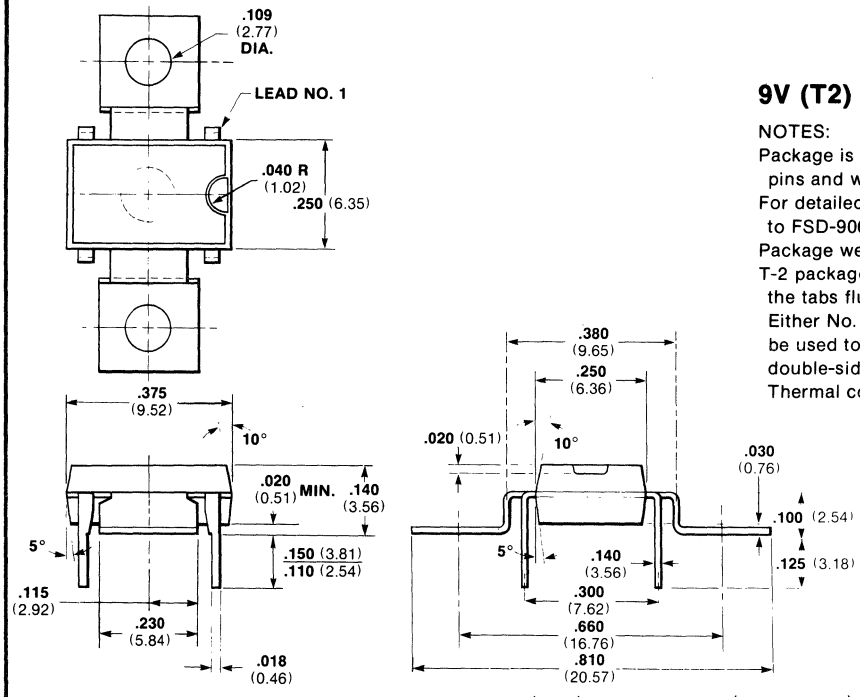
4-PIN POWER MINIDIP



9V (T1)

NOTES:
Package is plastic with tin-plated copper pins
For detailed package configuration refer to FSD-90669
Package weight is 0.6 gram
T-1 package can be soldered to the PC board through .0230" x .020 (0.584 x 0.51) slots. Double or single-sided boards may be used.

4-PIN POWER MINIDIP

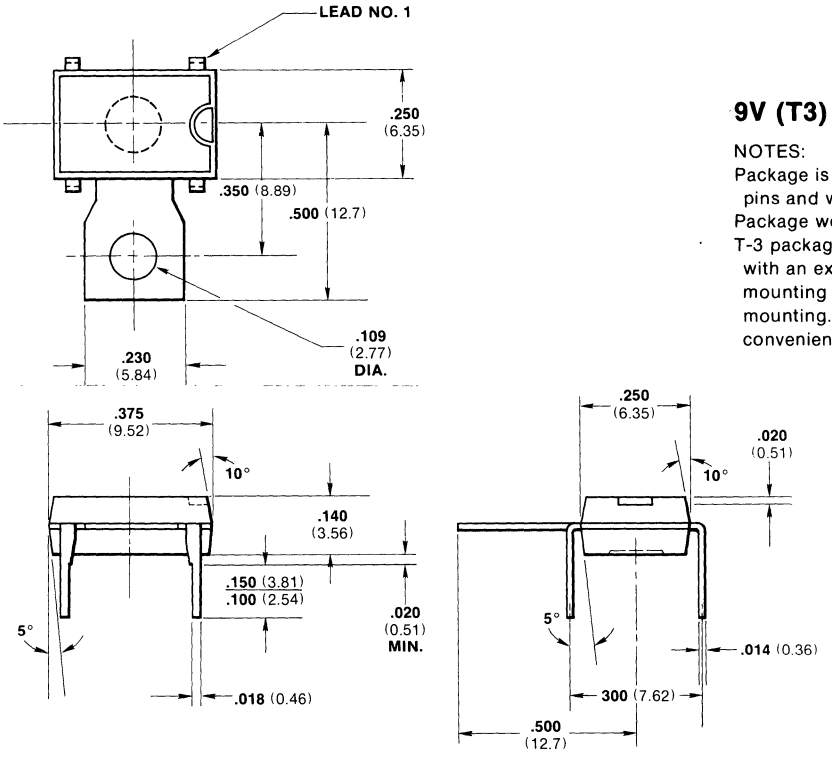


9V (T2)

NOTES:
Package is plastic with tin-plated copper pins and wings
For detailed package configuration refer to FSD-90670.
Package weight is 0.6 gram
T-2 package is intended to be mounted with the tabs flush with the top of the PC board. Either No. 2-56 screws or No. 2 rivets may be used to secure the package. Single or double-sided PC boards may be used. Thermal compound is recommended.

All dimensions in inches (bold) and millimeters (parentheses)

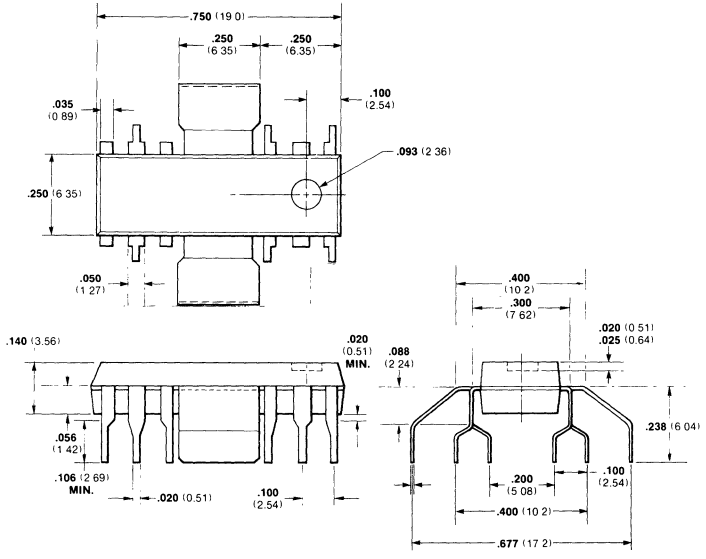
4-PIN POWER MINIDIP



9V (T3)

NOTES:
Package is plastic with tin-plated copper pins and wings
Package weight is 0.6 gram
T-3 package is intended for applications with an external heat sink. A No. 2 mounting hole is provided for case of mounting. The tab may be bent to any convenient angle.

12-PIN POWER PLASTIC DUAL IN-LINE



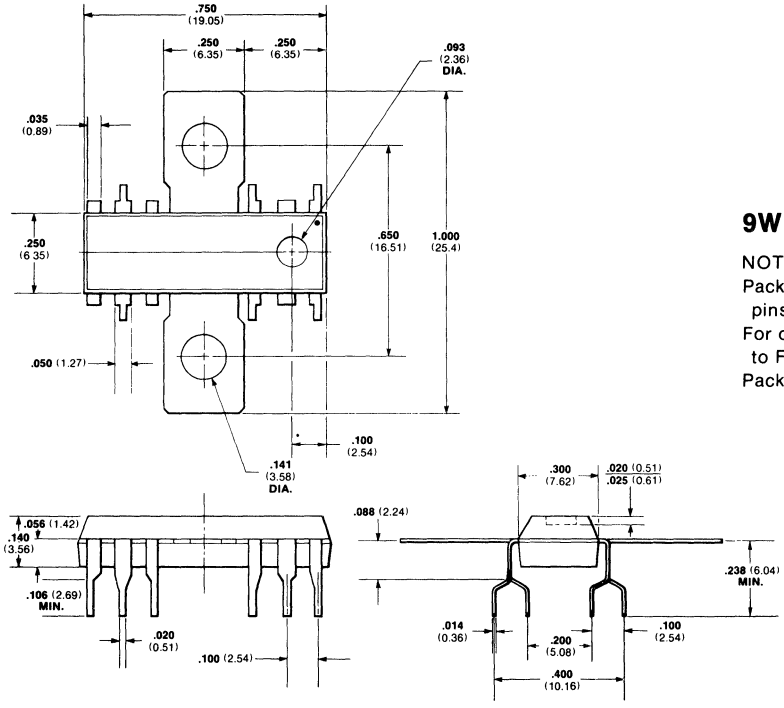
9W (P3)

NOTES:
Package is plastic with tin plated copper pins and wings
For detailed package configuration refer to FSB-90698
Package weight is 0.9 gram

All dimensions in inches (bold) and millimeters (parentheses)

FAIRCHILD PACKAGE OUTLINES

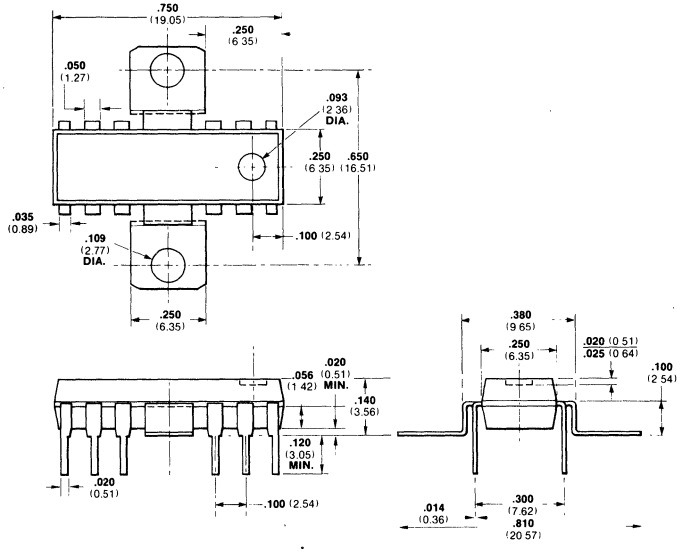
12-PIN POWER PLASTIC DUAL IN-LINE



9W (P4)

NOTES:
Package is plastic with tin-plated copper pins and wings
For detailed package configuration refer to FSB-90699
Package weight is 0.9 gram

12-PIN POWER PLASTIC DUAL IN-LINE

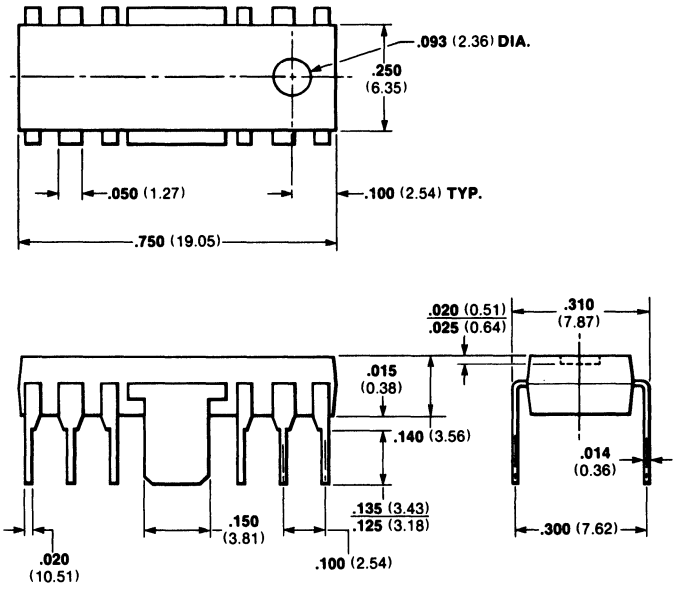


9W (P5)

NOTES:
Package is plastic with tin-plated copper pins and wings
For detailed package configuration refer to FSD-90740.
Package weight is 0.9 gram

All dimensions in inches (bold) and millimeters (parentheses)

12-PIN PLASTIC DUAL IN-LINE



9W (P6)

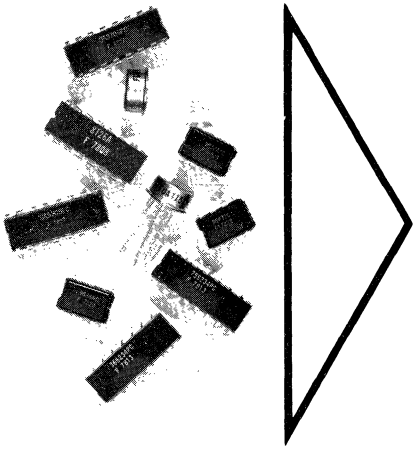
NOTES:

Package is plastic with tin-plated copper pins and wings

Package weight is 0.9 gram

The heat sinking tabs are electrically connected to the most negative potential pin

All dimensions in inches (bold) and millimeters (parentheses)



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