RCA

Solid
State

Industrial · Industrial · Industrial · Industrial · Industrial · Industrial · Ind

Bipolar · BiMOS · I2L · Gold CHIP · MOS · Bipolar · BiMOS · I2L · Gold CHI

Consumer · Consumer · Consumer · Consumer · Consumer · Consumer · Co

Linear Integrated Circuits

SSD-240A

RCA
Linear Integrated Circuits

This DATABOOK contains complete technical information on the full line of RCA standard commercial linear integrated circuits and MOS field-effect transistors for both industrial and consumer applications. An Index to Devices provides a complete listing of types, together with an indication of package options available for each of them.

The pages immediately following the Index to Devices include photographs of the packages used for RCA linear integrated circuits and MOS/FET's, a product-classification chart, recommended operating and handling considerations, a list of special terms and symbols used in the characterization of RCA linear integrated circuits and MOS/FET's, and a cross-reference directory that indicates RCA types recommended as direct replacements for other manufacturers' types.

Three separate data sections provide definitive ratings and electrical characteristics for (1) Linear Integrated Circuits for Industrial Applications, (2) Linear Integrated Circuits for Consumer Applications, and (3) MOS Field-Effect Transistors (MOS/FET's). Data pages for individual devices are included as nearly as possible in alpha-numerical sequence of type numbers. Because some devices are grouped together to show similarity of function or data, individual type numbers may be out of sequence. If you don't find the data on a specific type where you expect it to be, check the Index to Devices.

The DATABOOK also includes dimensional outlines for all currently available packages and selected RCA Application Notes on RCA Linear Integrated Circuits and MOS/FET's.

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RCA Solid State

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CA124	E	G	—	—	—	—	796	29
CA139	E	G	—	—	—	—	795	32
CA139A	E	G	—	—	—	—	795	32
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CA224	E	G	—	—	—	—	796	29
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CA747	T	E	G	—	—	—	531	50
CA747C	T	E	G	H	GH	—	531	50
CA748	T	S	E*	G	—	—	531	50
CA748C	T	S	E*	G	H	GH	531	50
CA758	E	—	—	—	—	—	760	295
CA810	Q	QM	—	—	—	—	1154	298
CA810A	Q	QM	—	—	—	—	1154	298
CA920	E	—	—	—	—	—	1132	301
CA1190	Q	—	—	—	—	—	1155	303
CA1310	E	—	—	—	—	—	761	306
CA1352	E	—	—	—	—	—	961	309
CA1391	E*	—	—	—	—	—	981	310
CA1394	E*	—	—	—	—	—	981	310
CA1398	E	—	—	—	—	—	686	312
CA1458	T	S	E*	G	H	GH	531	50
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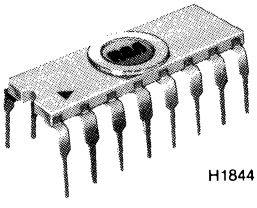
40822	TO-72	465	470
40823	TO-72	465	470
40841	TO-72	489	471

Packages

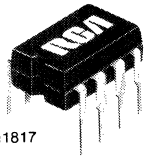
D Suffix
Dual-In-Line Welded-Seal Ceramic Package



H1844

14 and 16-lead versions

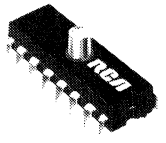
E Suffix
Dual-In-Line Plastic Package



H1817

8, 14, and 16-lead versions

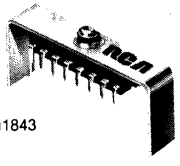
E Suffix
Power Stud Plastic Dual-In-Line Package



H1828

CA3134E only

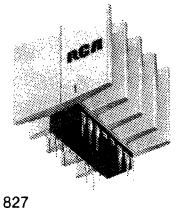
EM Suffix
Modified 16-lead Dual-In-Line Plastic Package



H1843

CA3134EM only

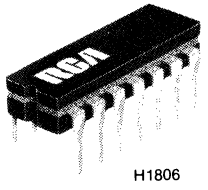
EM Suffix
Modified 16-lead Dual-In-Line Plastic Package



H1827

CA3131EM, CA3132EM only

F Suffix
Dual-In-Line Frit-Seal Ceramic Package



H1806

14 and 16-lead versions

Product Classification Chart

Industrial Circuits

OPERATIONAL AMPLIFIERS

General Purpose

Single Unit	Dual Unit
CA101	CA158
CA107	CA258
CA201	CA358
CA207	CA747
CA301	CA1458
CA307	CA1558
CA741	CA2904
CA748	Quad Unit
CA6741•	CA124
	CA224
	CA324
	CA3401

General Purpose Wideband

Single Unit
CA3008
CA3010
CA3015
CA3016
CA3029
CA3030
CA3037
CA3038
CA3100*
CA3130*
CA3140*
CA3160*
Dual Unit
CA3240*

Variable

High Current
CA3094
Micropower
CA3060
CA3078
CA3080
CA6078•

DIFFERENTIAL AMPLIFIERS

CA3000
CA3001
CA3004
CA3005
CA3006
CA3007
CA3026
CA3028
CA3049
CA3050
CA3051
CA3053
CA3054
CA3102

ARRAYS

Amplifier/Diode

Amplifier
CA3026
CA3035
CA3048
CA3049
CA3052
CA3054
CA3060
CA3102
Diode
CA3019
CA3039
CA3141

Transistor

CA3018	CA3095
CA3036	CA3096
CA3045	CA3097
CA3046	CA3118
CA3050	CA3127
CA3051	CA3138
CA3081	CA3146
CA3082	CA3183
CA3083	CA3600▲
CA3084	CA3724
CA3086	CA3725
CA3093	

VOLTAGE REGULATORS

CA723
CA3085

ZERO-VOLTAGE SWITCHES

CA3058
CA3059
CA3079

VOLTAGE COMPARATORS

Single Unit
CA111
CA211
CA311
CA3098+
CA3099+
Dual Unit
CA3290*
Quad Unit
CA139
CA239
CA339

SPECIAL-FUNCTION CIRCUITS

A/D Converter
CA3162
BCD-to-7-Segment Decoder/Driver
CA3161
Memory Sense Amplifier
CA1541
Four-Quadrant Multiplier
CA3091
Timer
CA555
Programmable Schmitt Trigger
CA3098

MOS/FET's

Single Gate	Dual Gate
3N128	3N140
3N138	3N141
3N139	3N159
3N142	Dual Gate
3N143	Protected
3N152	3N187
3N153	3N200
3N154	40819

Consumer Circuits

BROADBAND (VIDEO) AMPLIFIERS

CA3002
CA1352
CA3020
CA3021
CA3022
CA3023
CA3040

MULTIPLEX DECODERS

CA758
C1310
CA3090A

AM/FM COMMUNICATIONS CIRCUITS

CA2111A
CA3011
CA3012
CA3013
CA3014
CA3043
CA3075
CA3076
CA3088
CA3089
CA3123
CA3163
CA3189

AUDIO CIRCUITS

Preamplifiers
CA3036
CA3052
Drivers
CA3094
Power Amplifiers
CA810
CA2002
CA2004
CA3131
CA3132

FM IF CIRCUITS

Subsystems
CA2111A
CA3013
CA3014
CA3043
CA3075
CA3089
CA3189
Gain Blocks
CA3011
CA3012
CA3076

TV RECEIVER CIRCUITS

Tuning
CA3163
CA3166
CA3168
AFT
CA3044
CA3064
CA3139
Sound IF
CA1190
CA2111A
CA3041
CA3042
CA3065
CA3134
PIX IF
CA270
CA1352
CA3068
CA3136
Remote Control
CA3035
"Jungle" Circuits
CA3120
CA3142

Chroma Systems
CA1398
CA3066
CA3067
CA3070
CA3071
CA3072
CA3121
CA3125
CA3126
CA3128
CA3151
CA3170
Luminance Processors
CA3135
CA3143
CA3144
Horizontal Systems
CA1391
CA1394
CA920A
CA3159
CA3172

MOS/FET's

Single Gate	Dual Gate
40467A	Protected
40468A	3N204
40559A	3N205
Dual Gate	3N206
40600	3N211
40601	3N212
40602	3N213
40603	40673
40604	40820
	40821
	40822
	40823
	40841

• Low-noise versions of CA741 and CA3078 * BiMOS types ▲CMOS type + Programmable

tions, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

*Trade Mark: Emerson and Cumming, Inc.

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

$V_{BE(sat)}$	base-to-emitter saturation voltage
$V_{(BR)CBO}$	collector-to-base breakdown voltage
$V_{(BR)CES}$	collector-to-emitter breakdown voltage
$V_{(BR)DI}$	dc breakdown voltage between diode and substrate
$V_{(BR)R}$	dc reverse breakdown voltage
$V_{(BR)EBO}$	emitter-to-base breakdown voltage
$V_{(BR)GSSF}$	dc gate-to-source forward breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G1SSF}$	dc gate-No.1-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)G2SSF}$	dc gate No.2-to-source forward breakdown voltage, all other terminals shorted to source (dual-gate types)
$V_{(BR)GSSR}$	dc gate-to-source reverse breakdown voltage, all other terminals shorted to source (single-gate types)
$V_{(BR)G2SSR}$	dc gate-No.2-to-source reverse breakdown voltage, all other terminals shorted to source (dual-gate types)
V_{CBO}	collector-to-base voltage
V_{CC}	drain supply voltage used as a second positive supply voltage. It is $\leqslant V_{DD}$ and referenced to V_{SS}
VCO	voltage controlled oscillator
V_{CEO}	collector-to-emitter voltage
$V_{CEO(sus)}$	collector-to-emitter sustaining voltage
V_{CIO}	collector-to-substrate voltage
V_{CP}	charge pump voltage
V_{DD}	drain supply voltage (the most positive supply voltage; always referenced to ground)
V_{DG}	drain-to-gate voltage (single-gate types)
V_{DG1}	drain-to-gate-No.1 voltage (dual-gate types)
V_{DG2}	drain-to-gate-No.2 voltage (single-gate types)
V_{DIO}	diode-to-substrate voltage
V_{DR}	diode reverse voltage
V_{DS}	drain-to-source voltage
V_{EE}	source voltage (the most negative supply voltage in a 3-supply voltage system)
V_F	dc forward voltage
$\Delta V_F/\Delta T$	temperature coefficient of forward voltage drop
V_{GH}	channel gate input voltage, high level
V_{GL}	channel gate input voltage, low level
V_{GS}	gate-to-source voltage
$V_{GS(TH)}$	gate-to-source threshold voltage
$V_{GS(Off)}$	gate-to-source cutoff voltage (single-gate types)
V_{G1S}	gate-No.1-to-source voltage (dual-gate type)
$V_{G1S(Off)}$	gate-No.1-to-source cutoff voltage (dual-gate types)
V_{G2S}	gate-No.2-to-source voltage (dual-gate types)
$V_{G2S(off)}$	gate-No.2-to-source cutoff voltage (dual-gate types)
V_I	input voltage
$V_{I(Lim)}$	input limiting voltage
V_{ICR}	common-mode input voltage range
V_{IL}	input-voltage, low level
V_{IH}	input-voltage, high level
V_{IO}	input offset voltage
$\lvert V_{IO}\rvert$	magnitude of input offset voltage
$\Delta V_{IO}/\Delta T$	temperature coefficient of magnitude of input offset voltage
$\Delta V_{IO}/\Delta T$	temperature coefficient of input offset voltage drift
$\Delta V_{IO}/\Delta V^+$	positive input-offset-voltage sensitivity
$\Delta V_{IO}/\Delta V^-$	negative input-offset-voltage sensitivity
αV_{IO}	average temperature coefficient of input-offset voltage
$V_{i(Lim)}$	input limiting voltage (knee)
V_{knee}	protective diode knee voltage (protected gate types)
V_N	output noise voltage
V_O	output voltage
$\Delta V_O/\Delta V^-$	dc supply voltage sensitivity
$\Delta V_O/\Delta V^+$	dc supply voltage sensitivity
$V_{O(rms)}$	open-loop output voltage swing
ΔV_O	output voltage temperature coefficient
$V_{Op\text{-}p}$	output voltage swing
$V_{O(af)}$	recovered af voltage
V_{OL}	output voltage, low level; the voltage level at an output when the input logic conditions have been set to establish logic LOW output.
V_{OO}	output offset voltage
V_{OH}	output voltage, high level; the voltage level at an output when the input logic conditions have been set to establish a logic HIGH output.
V_{OM}^+	maximum output voltage
V_{OM}^-	maximum output voltage
V_{QP}	charge pump voltage
V_{QPL}	charge pump input voltage, low level
V_{QPH}	charge-pump input voltage, high level
V_{REF}	reference voltage
V_{REG}	regulated supply voltage
V_{RR}	supply voltage rejection ratio
V_{TH}	input threshold voltage
V_Z	zener voltage
Y_{fs}	magnitude of small-signal, common-source, short-circuit forward transfer admittance (transadmittance)
Y_{is}	small-signal, common-source, short-circuit, input-admittance (conductance, real part of admittance; susceptance, imaginary part of admittance)
Y_{os}	small-signal, common-source, short-circuit, output admittance
$\lvert Y_{rs}\rvert$	magnitude of small-signal, common-source, short-circuit, reverse transadmittance
$<Y_{rs}$	phase angle of small-signal, common-source, short-circuit, reverse transadmittance
$(-)_{rs}$	angle of reverse transadmittance, common-source circuit
Z_1	input impedance
Z_O	output impedance
Z_Z	zener impedance
ϕ	phase angle
ϕ	phase margin
η	efficiency
$\phi\cdot L$	open-loop phase lag

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
LM311L	CA311T
LM311N	CA311G, CA311E
LM311N-14	CA311G,CA311E
LM311P	CA311G, CA311E
LM311T	CA311T
LM318H	CA3130T
LM324AD	CA324AG
LM324AN	CA324AG, CA324AF
LM324D	CA324G
LM324F	CA324G
LM324J	CA324G
LM324N	CA324G, CA324E
LM339AD	CA339AG
LM339AF	CA339AG
LM339AJ	CA339AG
LM339AN	CA339AG, CA339AE
LM339A	CA339G, CA339E
LM339D	CA339G
LM339F	CA339G
LM339J	CA339G
LM339N	CA339G, CA339E
LM358AH	CA358AT
LM358AN	CA358AG, CA358AE
LM358AT	CA358AT
LM358JG	CA358G
LM358H	CA358
LM358L	CA358T
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LM358P	CA358G, CA358E
LM358T	CA358T
LM393N	CA3290E
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LM555H	CA555T
LM555N	CA555G, CA555E
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LM723N	CA723E
LM741CH	CA741CT
LM741CJ	CA741CG
LM741CN	CA741CG, CA741CE
LM741H	CA741T
LM741N	CA741G, CA741E
LM746N	CA3072
LM747CD	CA747CG
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LM747CN	CA747CG, CA747CE
LM747D	CA747G
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LM748CN	CA748CG, CA748CE
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LM1391N	CA1391E
LM1394N	CA1394E
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LM1458J	CA1458G
LM1458N	CA1458G, CA1458E
LM1558H	CA1558T
LM1558J	CA1558G
LM1558N	CA1558G, CA1558E
LM1800N	CA758E
LM1820N	CA3123E
LM1845N	CA3120E
LM2111N	CA2111AE
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LM2904N	CA2904G
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LM3070N	CA3070
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LM3089N	CA3089E, CA3189E
LM3126N	CA3126E
LM3146AN	CA3146AE
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MC1357PQ	CA2111AQ
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MC1364G	CA3064T
MC1364P	CA3064E
MC1370P	CA3070
MC1371P	CA3071
MC1375P	CA3075
MC1389P	CA3089E, CA3189E
MC1391P	CA1391E
MC1394P	CA1394E
MC1398P	CA1398E
MC1455G	CA555CT
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MC1458G	CA1458T
MC1458L	CA1458T
MC1458P	CA1458G, CA1458E
MC1458P1	CA1458G, CA1458E
MC1458T	CA1458T
MC1541L	CA1541D
MC1555G	CA555T
MC1555P1	CA555CG, CA555CE
MC1555U	CA555G
MC1558JG	CA1558T
MC1558G	CA1558T
MC1558L	CA1558T
MC1558P	CA1558G, CA1558E
MC1558P1	CA1558G, CA1558E
MC1558T	CA1558T
MC1558U	CA1558G
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MC1723CP	CA723CE
MC1723G	CA723T
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MC1741CP2	CA741CG,CA741CE
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MC1741L	CA741G
MC1741U	CA741G
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MC1747CL	CA747CG
MC1747G	CA747T
MC1747L	CA747G
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MC1748CP1	CA748CG, CA748CE
MC1748CU	CA748CG
MC1748G	CA748T
MC1748U	CA748G
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MC3386P	CA3086
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MLM101AU	CA101AG
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MLM107U	CA101G
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MLM139L	CA139G
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MLM307U	CA307G
MLM311G	CA311T
MLM311P1	CA311G, CA311E
MLM311U	CA311G
MLM324L	CA324G, CA324E

Cross-Reference Directory for Linear Integrated Circuits

Industry Type	RCA Replacement Type
SN76666N	CA3065
SN76675N	CA3075
SN76676P	CA3076
SN76689N	CA3089E, CA3189E
SP3724	CA3724G
SP3725	CA3725G
SSS101AJ	CA101AT
SSS101AP	CA101AG, CA101AE
SSS107J	CA107T
SSS107P	CA107G, CA107E
SSS201AJ	CA201AT
SSS201AP	CA201AG, CA201AE
SSS207J	CA207T
SSS301AJ	CA301AT
SSS301AP	CA301AG, CA301AE
SSS741CJ	CA741CT
SSS1458J	CA1458T
SSS1558J	CA1558T
TBA810S	CA810Q
TBA810AS	CA810QM
TDA2002V	CA2002
TDA2002H	CA2002M
TBB0747	CA747CT
TBB0748	CA748CT
TBB0748B	CA748CE
TBB1458B	CA1458E
TBC0747	CA747T
TCA270	CA270
TDA3081N	CA3081
TDA3082N	CA3082
TDA3083N	CA3083
TDB0723	CA723CT
TDB0723A	CA723CE
TDC0723	CA723T
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U5B7741393	CA741CT
U5B7748312	CA748T
U5B7748393	CA748CT
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ULN2111A	CA2111AE
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ULN2125A	CA3120E
ULN2127A	CA3071
ULN2129A	CA3075
ULN2137A	CA3123E
ULN2165A	CA3065
ULN2210A	CA1310E
ULN2212B	CA3012
ULN2262A	CA3126Q
ULN2264A	CA3064
ULN2266A	CA3066
ULN2267A	CA3067
ULN2269A	CA3121E
ULN2289A	CA3089E, CA3189E
ULN2298A	CA1398E
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μA101AD	CA101AG
μA101D	CA101G
μA101H	CA101T
μA107H	CA107T
μA111H	CA111T
μA111R	CA111G
μA201AD	CA201AG
μA201AH	CA201AT
μA201D	CA201G
μA201H	CA201AT
μA207H	CA207T
μA301AD	CA301AG
μA301AH	CA301AT
μA307H	CA307T
μA307T	CA307G, CA307E
μA301AT	CA301AG, CA301AE
μA311H	CA311T
μA311R	CA311G
μA311T	CA311G, CA311E
μA555HC	CA555CT
μA555HM	CA555T
μA555TC	CA555CG, CA555CE
μA720PC	CA3123E
μA723CA	CA723CE
μA723CK	CA723CT
μA723CL	CA723CT
μA723CN	CA723CE
μA723DM	CA723E
μA723HC	CA723CT
μA723HM	CA723T
μA723K	CA723T
μA723MN	CA723E
μA723ML	CA723T
μA723PC	CA723CE
μA741CJG	CA741CG
μA741CJ	CA741CG
μA741CN	CA741CG,CA741CE
μA741CL	CA741T
μA741CP	CA741CG, CA741CE
μA741CT	CA741CT
μA741DC	CA741G
μA741DM	CA741G
μA741HC	CA741CT
μA741HM	CA741T
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μA741MJ	CA741G
μA741ML	CA741T
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μA746PC	CA3072
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μA747CN	CA747CG, CA747CE
μA747DC	CA747CG
μA747DM	CA747G
μA747HC	CA747CT
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μA747PC	CA747G, CA747E
μA747A	CA747E
μA747K	CA747T
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μA748CJ	CA748CG
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μA478CP	CA748G,CA748E
μA748CT	CA748CT
μA748DC	CA748CG
μA748DM	CA748G, CA748E
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μA748MJG	CA748G
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μA780PC	CA3070
μA781PC	CA3071
μA787PC	CA3126Q
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μA3018AHM	CA3018A
μA3019HM	CA3019
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μA3036HM	CA3036
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μA3065PC	CA3065
μA3066PC	CA3066
μA3075PC	CA3075
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μPC151A	CA741CT
μPC151C	CA741CG, CA741CE
μPC157A	CA301AT
μPC157C	CA301AG, CA301AE
μPC251A	CA747CT
μPC251C	CA1458G, CA1458E
μPC301AC	CA301AG, CA301AE
μPC311C	CA311G, CA311E
μPC324C	CA324G, CA324E
μPC339C	CA339G, CA339E
μPC741C	CA741CG, CA741CE
μPC1458C	CA1458G, CA1458E

Linear Integrated Circuits for Industrial Applications

Technical Data

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS▲ Supply Voltage ($V^{\pm}$) = 5 to 15 V		LIMITS CA101 Min.	CA101 Typ.	CA101 Max.	CA201 Min.	CA201 Typ.	CA201 Max.	UNITS	LIMITS CA101A CA201A Min.	CA101A CA201A Typ.	CA101A CA201A Max.	CA301A Min.	CA301A Typ.	CA301A Max.	UNITS
Input Offset Voltage V_{IO}	T_A=25°C	$R_S \leq 10k\Omega$	–	1	5	–	2	7.5	mV	–	–	–	–	–	–	mV
		$R_S \leq 50k\Omega$	–	–	–	–	–	–		–	0.7	2	–	2	7.5	
		$R_S \leq 10k\Omega$	–	–	6	–	–	10		–	–	–	–	–	–	
		$R_S \leq 50k\Omega$	–	–	–	–	–	–		–	–	3	–	–	10	
Average Temperature Coefficient of Input Offset Voltage αV_{IO}		$R_S \leq 10k\Omega$	–	6	–	–	10	–	µV/°C	–	–	–	–	–	–	µV/°C
		$R_S \leq 50\Omega$	–	3	–	–	6	–		–	–	–	–	–	–	
			–	–	–	–	–	–		–	3	15	–	6	30	
Average Temperature Coefficient of Input Offset Current αI_{IO}	−55°C to +25°C		–	–	–	–	–	–	nA/°C	–	0.02	0.2	–	–	–	nA/°C
	0°C to +25°C		–	–	–	–	–	–		–	–	–	–	0.02	0.6	
	+25°C to +70°C		–	–	–	–	–	–		–	–	–	–	0.01	0.3	
	+25°C to +125°C		–	–	–	–	–	–		–	0.01	0.1	–	–	–	
Input Offset Current I_{IO}	T_A=0°C		–	–	–	–	150	750	nA	–	–	–	–	–	–	nA
	T_A=25°C		–	40	200	–	100	500		–	1.5	10	–	3	50	
	T_A=70°C		–	–	–	–	50	400		–	–	–	–	–	–	
	T_A=125°C		–	10	200	–	–	–		–	–	–	–	–	–	
			–	–	–	–	–	–		–	–	20	–	–	70	
	T_A=−55°C		–	100	500	–	–	–		–	–	–	–	–	–	
Input Bias Current I_{IB}	T_A=−55°C		–	0.28	1.5	–	–	–	µA	–	–	–	–	–	–	µA
	T_A=0°C		–	–	–	–	0.32	2		–	–	–	–	–	–	
	T_A=25°C		–	0.12	0.5	–	0.25	1.5		–	0.03	0.075	–	0.07	0.25	
			–	–	–	–	–	–		–	–	0.1	–	–	0.3	
Supply Current $I^{\pm}$	T_A=25°C	$V^{\pm}$=15V	–	–	–	–	–	–	mA	–	–	–	–	1.8	3	mA
		$V^{\pm}$=20V	–	1.8	3	–	1.8	3		–	1.8	3	–	–	–	
	T_A=125°C	$V^{\pm}$=20V	–	1.2	2.5	–	–	–		–	1.2	2.5	–	–	–	
Open-Loop Differential Voltage Gain A_{OL}	T_A=25°C $V^{\pm}$=15V V_O=±10V	$R_L \geq 2k\Omega$	50	160	–	20	150	–	V/mV	50	160	–	25	160	–	V/mV
		$V^{\pm}$=15V $R_L \geq 2k\Omega$	25	–	–	15	–	–		25	–	–	15	–	–	
Input Resistance R_I	T_A=25°C		0.3	0.8	–	0.1	0.4	–	MΩ	1.5	4	–	0.5	2	–	MΩ
Output Voltage Swing V_{OPP}	$V^{\pm}$=15V	R_L=10kΩ	±12	±14	–	±12	±14	–	V	±12	±14	–	±12	±14	–	V
	$V^{\pm}$=15V	R_L=2kΩ	±10	±13	–	±10	±13	–		±10	±13	–	±10	±13	–	
Common-Mode Input-Voltage Range V_{ICR}	$V^{\pm}$=15V		±12	–	–	±12	–	–	V	–	–	–	±12	–	–	V
	$V^{\pm}$=20V		–	–	–	–	–	–		±15	–	–	–	–	–	
Common-Mode Rejection Ratio CMRR		$R_S \leq 10k\Omega$	70	90	–	65	90	–	dB	–	–	–	–	–	–	dB
		$R_S \leq 50k\Omega$	–	–	–	–	–	–		80	96	–	70	90	–	
Supply-Voltage Rejection Ratio PSRR		$R_S \leq 10k\Omega$	70	90	–	70	90	–	dB	–	–	–	–	–	–	dB
		$R_S \leq 50k\Omega$	–	–	–	–	–	–		80	96	–	70	90	–	

▲ Characteristics applicable over operating temperature range (T_A) as shown below, unless otherwise specified: CA101, CA101A: −55 to +125°C; CA201A: −25 to +85°C; CA201, CA301A: 0 to 70°C

	CA101	CA201	CA101A	CA201A	CA301A	
Max. V_{IO} (T_A = 25°C)	5	7.5	2	2	7.5	mV
Max. I_{IO} (T_A = 25°C)	200	500	10	10	50	nA
Min. A_{OL} (T_A = 25°C)	50	20	50	50	25	V/mV
T_A Range (Operating)	−55 to +125	0 to +70	−55 to +125	−25 to +85	0 to +70	°C
Slew Rate (Summing ampl.)	–	–	10	10	10	V/µs

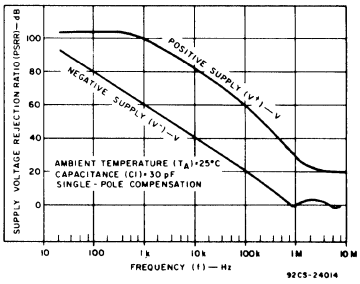


Fig. 15 — Supply voltage rejection ratio vs. frequency.

Two-Pole Compensation

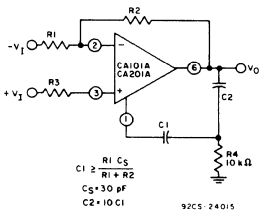


Fig. 16 — Test circuit employing two-pole compensation.

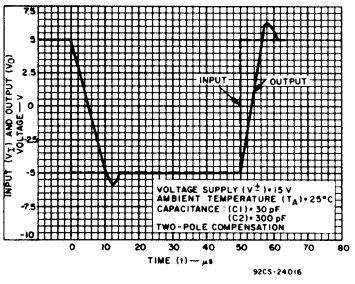


Fig. 17 — Voltage follower pulse response.

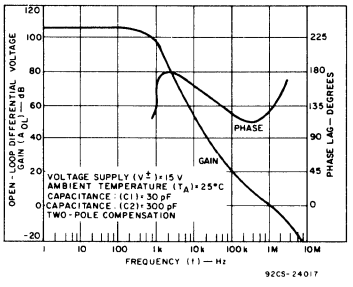


Fig. 18 — Voltage gain and phase lag vs. frequency.

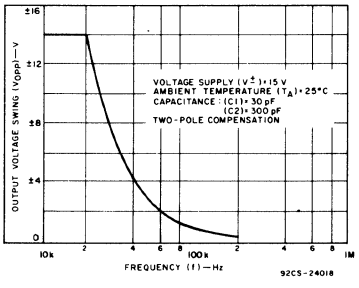


Fig. 19 — Output voltage swing vs. frequency.

Feed-Forward Compensation

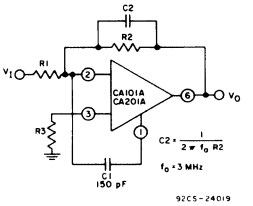


Fig. 20 — Test circuit employing feedforward compensation.

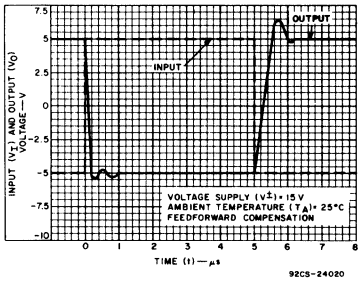


Fig. 21 — Inverter pulse response.

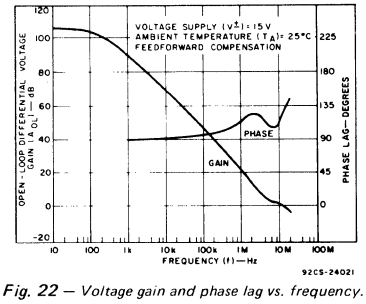


Fig. 22 — Voltage gain and phase lag vs. frequency.

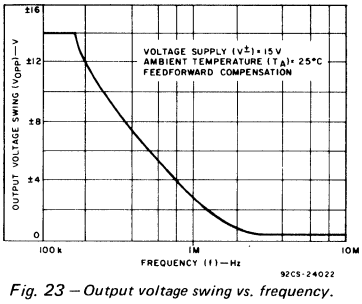


Fig. 23 — Output voltage swing vs. frequency.

CA101A AND CA201A

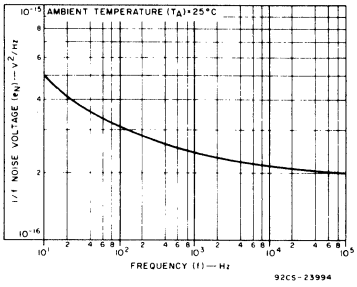


Fig. 24 — I/f noise voltage vs. frequency.

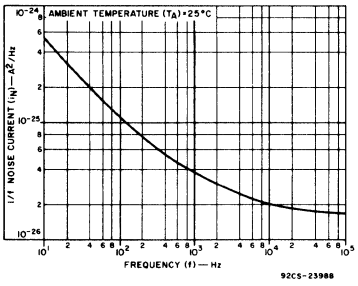


Fig. 25 — I/f noise current vs. frequency.

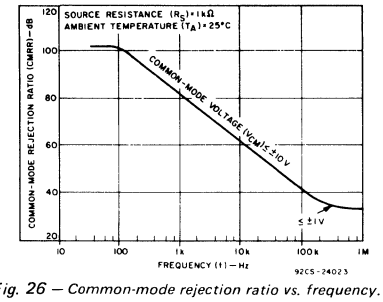


Fig. 26 — Common-mode rejection ratio vs. frequency.

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^\circ C$:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals):	
CA107, CA207	44 V
CA307	36 V
DC INPUT VOLTAGE	±15 V
(For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage)	
DIFFERENTIAL INPUT VOLTAGE	±30 V
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION UP TO $T_A = 70^\circ C$	500 mW
Above $T_A = 70^\circ C$ Derate linearly at	6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating – CA107	−55°C to +125°C
CA207	−25°C to +85°C▲
CA307	0°C to +70°C†
Storage – All Types	−65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

*For type CA307 continuous short circuit is allowed for Case Temperature to +70°C and ambient temperature to +55°C.

▲Types CA207G, S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of −25 to +85°C.

†Types CA307G, E, S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.

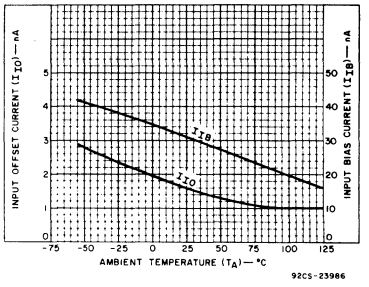


Fig. 4 – Input offset and input bias currents vs. ambient temperature.

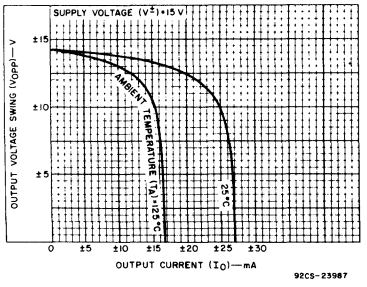


Fig. 5 – Output voltage swing vs. output current.

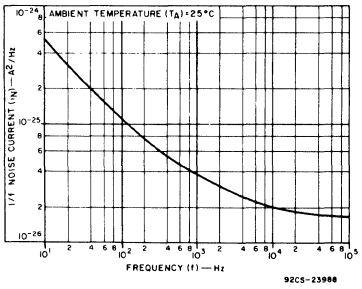


Fig. 6 – 1/f noise current vs. frequency.

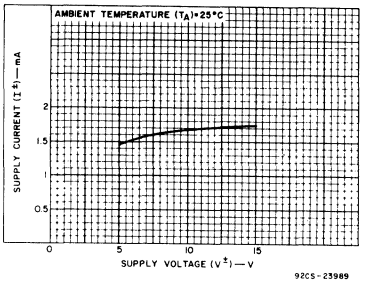


Fig. 7 – Supply current vs. supply voltage.

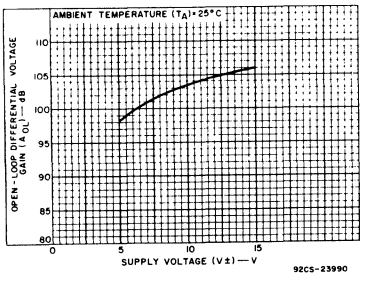


Fig. 8 – Open-loop differential voltage gain vs. supply voltage.

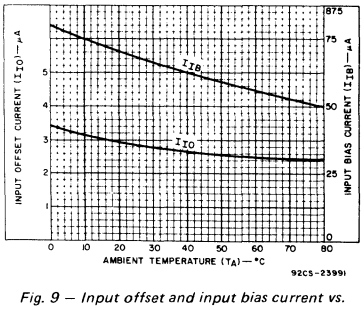


Fig. 9 – Input offset and input bias current vs. ambient temperature.

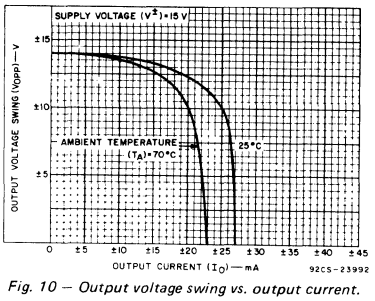


Fig. 10 – Output voltage swing vs. output current.

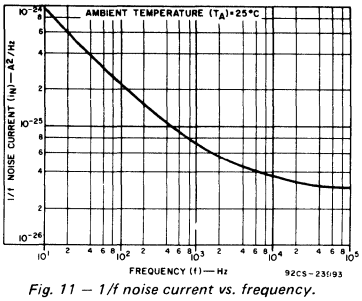


Fig. 11 – 1/f noise current vs. frequency.

Voltage Comparators

For Commercial and Industrial Applications

"G" Suffix Types—Hermetic Gold-CHIP in Dual-In-Line Plastic Package

"E" Suffix Types—Standard Dual-In-Line Plastic Package

"T" and "S" Suffix Types—TO-5 Style Package

Applications

- **Multivibrators**
- **Positive and negative peak detectors**
- **Crystal oscillators**
- **Zero-crossing detectors**
- **Solenoid, relay, and lamp drivers**

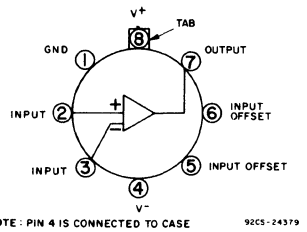
Features

- **Single- or dual-supply operation**
- **Power consumption — 135 mW at ±15 V**
- **Strobe capability**
- **Low input-offset current:**
  CA111, CA211 — 4 nA(typ.)
  CA311 — 6 nA(typ.)
- **Differential input-voltage range — ±30 V**
- **Directly interchangeable with National Semiconductor LM111, LM211, and LM311 Series types**

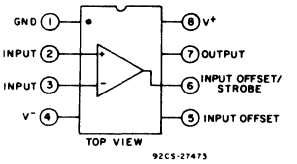
The RCA-CA111, CA211, and CA311 are monolithic voltage comparators that operate from dual supplies up to ±15 V, or from single supplies down to 5 V. This single-supply capability makes the outputs of these devices compatible with RTL, DTL, TTL, and MOS circuits. In addition, they can drive lamps or relays, and switch voltages up to 50 V (CA311, 40 V) at currents as high as 50 mA.

The inputs and the outputs of the CA111, CA211, and CA311 can be isolated from system ground, allowing the output to drive loads referred to ground, V^+, or V^-.

All types are available in hermetic gold-CHIP dual-in-line plastic packages (G suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA311 is also available in the 8-lead dual-in-line plastic package ("MINI-DIP",E suffix), and in chip form (H suffix).



Functional diagram for TO-5 style package.



Functional diagram for plastic package.

Type \ Feature	Max. V_{IO} (mV)	Max. I_{IO} (nA)	Max. I_{IB} (nA)	Temp. Range (T_A) °C	Package (Suffix)
CA111	3	10	100	−55 to +125	G,S,T
CA211	3	10	100	−25 to +85▲	G,S,T
CA311	7.5	50	250	0 to +70†	G,E,S,T

MAXIMUM RATINGS, *Absolute Maximum Values at $T_A = 25°C$*

DC SUPPLY VOLTAGE (between V^+ and V^- terminals) . . . . . 36 V
DC INPUT VOLTAGE* . . . . . ±15 V
DIFFERENTIAL INPUT VOLTAGE . . . . . ±30 V
OUTPUT TO NEGATIVE SUPPLY VOLTAGE (V_{7-4}):
  CA111, CA211 . . . . . 50 V
  CA311 . . . . . 40 V
GROUND TO NEGATIVE SUPPLY VOLTAGE (V_{1-4}) . . . . . 30 V
OUTPUT SHORT-CIRCUIT DURATION . . . . . 10 s
DEVICE DISSIPATION:
  Up to $T_A = 25°C$ . . . . . 500 mW
  Above $T_A = 25°C$ . . . . . derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
  Operating:
    CA111 . . . . . −55 to +125°C
    CA211 . . . . . −25 to +85°C▲
    CA311 . . . . . 0 to +70°C†
  Storage, all types . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ±1/32 in. (1.59 ±0.79 mm)
  from case for 10 seconds max. . . . . +265°C

*This rating applies for ±15 V supplies. The positive input-voltage limit is 30 V above the negative supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

▲ Types CA211G,S, and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of −25 to +85°C.

† Types CA311G,E,S and T can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS: SUPPLY VOLTAGE ($V^{\pm}$) = 15 V UNLESS OTHERWISE SPECIFIED		LIMITS: CA111 CA211 TYP.	CA111 CA211 MAX.	CA311 TYP.	CA311 MAX.	UNITS
Input Offset Voltage, V_{IO}	$R_s \leq 5\ k\Omega$, Note 2	T_A=25°C	0.7	3	2	7.5	mV
		Note 1	–	4	–	10	
Saturation Voltage	V_I = −5 mV, I_O = 50 mA (For CA311, $V_I \leq$ −10 mV)	T_A=25°C	0.75	1.5	–	–	V
	$V^+ \geq$4.5 V, V^-=0, $V_I \leq$ −6 mV, $I_{SINK} \leq$ 8 mA (For CA311, $V_I \leq$ −10 mV)	Note 1	0.23	0.4	–	–	
Input Voltage Range, V_{IPP}		Note 1	±14	–	±14	–	V
Input Offset Current, I_{IO}	Note 2	T_A = 25°C	4	10	6	50	nA
		Note 1	–	20	–	70	
Input Bias Current, I_{IB}	Note 2	T_A=25°C	60	100	100	250	nA
		Note 1	–	150	–	300	
Positive Supply Current, I^+		T_A = 25°C	5.1	6	5.1	7.5	mA
Negative Supply Current, I^-		T_A=25°C	4.1	5	4.1	5	mA
Output Leakage Current	$V_I \geq$5 mV, V_O = 35 V (For CA311, $V_I \geq$ −10 mV)	T_A=25°C	0.2	10	–	–	nA
		Note 1	0.1	0.5	–	–	μA
Strobe On Current		T_A=25°C	3	–	3	–	mA
Voltage Gain, A		T_A=25°C	200	–	200	–	V/mV
Response Time	100 mV Input Step with 5 mV overdrive voltage	T_A=25°C	200	–	200	–	ns

Note 1: Ambient temperature (T_A) over applicable operating temperature range as shown below.

CA111	CA211	CA311
−55 to +125°C	−25 to +85°C	0 to +70°C

Note 2: The input offset characteristics given are the values required to drive the output to within 1 V of either supply with a 1-mA load. These characteristics define an error band which takes into account the worst-case effects of voltage gain and input impedance. The input offset voltage, input offset current, and input bias current specifications apply for any supply voltage from a 5 V single supply up to a ±15 V dual supply.

TYPICAL CHARACTERISTICS – CA111, CA211 (CONT'D)

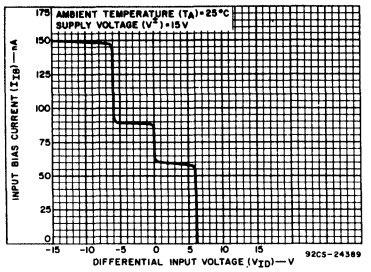


Fig. 10 – Input characteristcs.

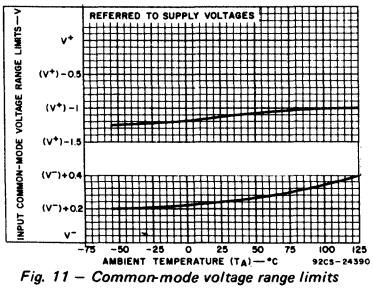


Fig. 11 – Common-mode voltage range limits vs. ambient temperature.

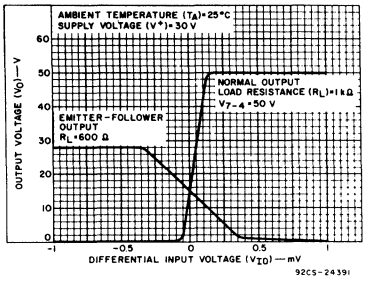


Fig. 12 – Transfer function.

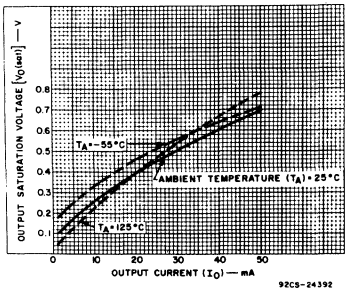


Fig. 13 – Output saturation voltage vs. output current.

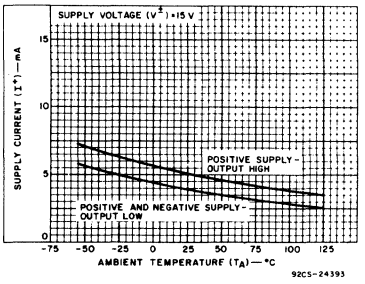


Fig. 14 – Supply current vs. ambient temperature.

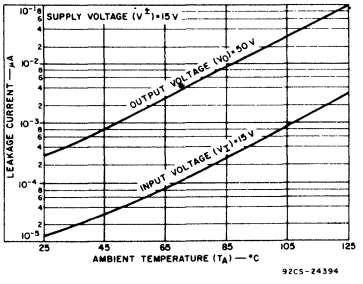


Fig. 15 – Input and output leakage current vs. ambient temperature.

Quad Operational Amplifiers

"E" Suffix Types: Standard Dual-In-Line Plastic Package
"G" Suffix Types: Hermetic Gold-Chip Dual-In-Line Plastic Package

For Commercial, Industrial, and Military Applications

The RCA-CA124, -CA224, and -CA324 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specifically to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range of from 0 V to $V^+ - 1.5$ V (single-supply operation) make the CA124, CA224, and CA324 suitable for battery operation.

The CA124, CA224, and CA324 are supplied in a 14-lead dual-in-line plastic package (E suffix), or in a hermetic gold-chip 14-lead dual-in-line plastic package (G suffix) to provide true hermetic performance. The CA324 is also available in chip form (H suffix), and as a hermetic gold-chip (HG suffix).

Features:

- **Operation from single or dual supplies**
- **Unity-gain bandwidth . . . . . 1 MHz (typ.)**
- **DC voltage gain . . . . . 100 dB (typ.)**
- **Input bias current . . . . . 45 nA (typ.)**
- **Input offset voltage . . . . . 2 mV (typ.)**
- **Input offset current . . . . . 5 nA (typ.) for CA224, CA324**
  3 nA (typ.) for CA124
- **Replacement for industry types 124, 224, 324**

Applications

- **Summing amplifiers**
- **Multivibrators**
- **Oscillators**
- **Transducer amplifiers**
- **DC gain blocks**

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE	32 V or ±16 V
DIFFERENTIAL INPUT VOLTAGE	±32 V
INPUT VOLTAGE	−0.3 V to +32 V
INPUT CURRENT ($V_I < -0.3$ V)†	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

*The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device.

†This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

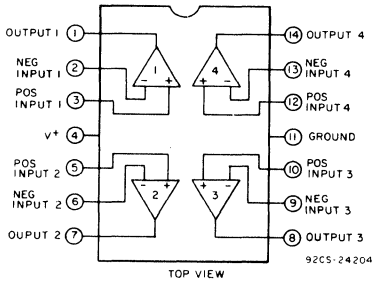


Fig. 1 – Functional diagram.

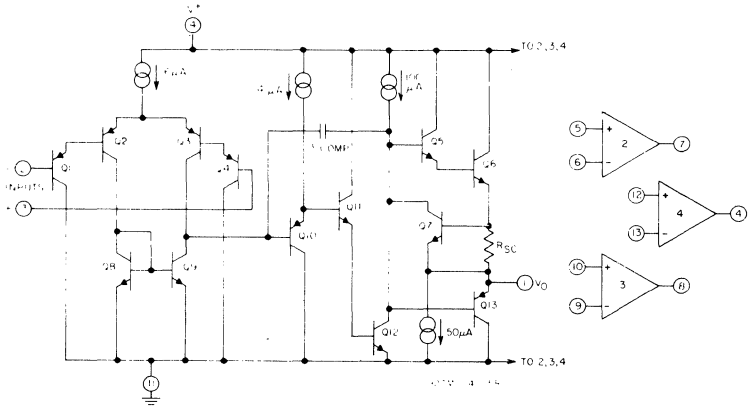


Fig. 2–Schematic diagram–one of four operational amplifiers.

TYPICAL CHARACTERISTICS CURVES

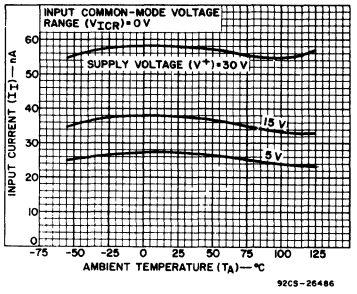


Fig. 3—Input current vs. ambient temperature.

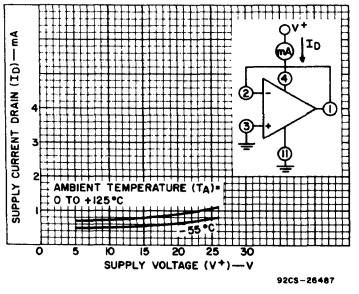


Fig. 4—Supply current drain vs. supply voltage.

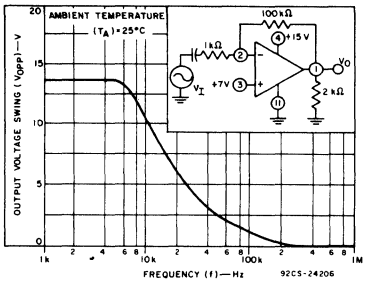


Fig. 5—Large-signal frequency response.

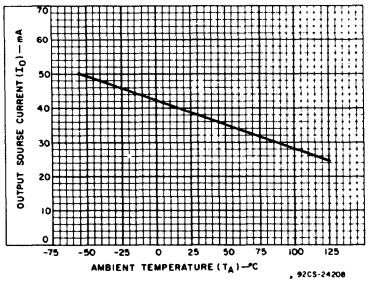


Fig. 6—Output current vs. ambient temperature.

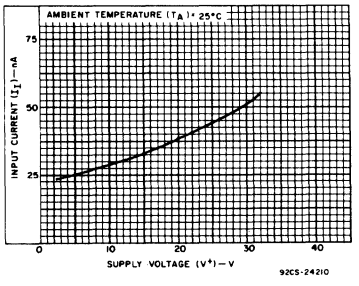


Fig. 7—Input current vs. supply voltage.

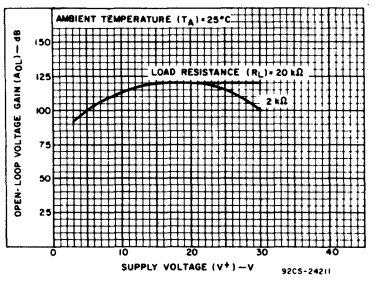


Fig. 8—Voltage gain vs. supply voltage.

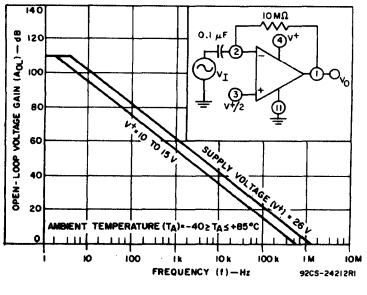


Fig. 9—Open-loop frequency response.

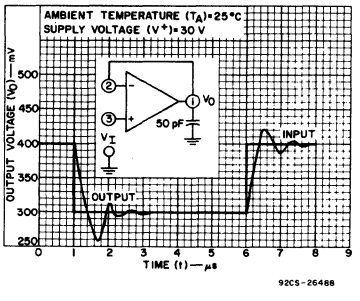


Fig. 10—Voltage follower pulse response (small signal).

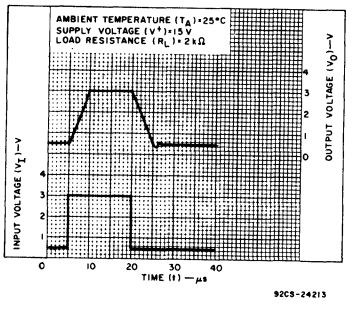


Fig. 11—Voltage follower pulse response.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS $V^+ = 5$ V, Unless otherwise indicated		LIMITS CA139 Min.	CA139 Typ.	CA139 Max.	CA139A Min.	CA139A Typ.	CA139A Max.	UNITS
Input Offset Voltage (V_{IO}) At Output Switch Point V ≅ 1.4 V	V_{REF} = 1.4 V, R_S = 0	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ≥0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	V_I^- = 1 V, V_I^+ = 0 V, $I_{SINK} \leq$ 4 mA	25°C	–	250	500	–	250	500	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	$V^+-1.5$	0	–	$V^+-1.5$	V
		Note 1	0	–	V^+-2	0	–	V^+-2	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	3	25	–	3	25	nA
		Note 1	–	–	100	–	–	100	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	100	–	25	100	nA
		Note 1	–	–	300	–	–	300	
Supply Current (I^+)	$R_L = \infty$ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	$V_I^+ \geq 1$ V, V_I^- = 0, V_O = 5 V	25°C	–	0.1	–	–	0.1	–	nA
	$V_I^+ \geq 1$ V, V_I^- = 0, V_O = 30 V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	$V_I^- \geq 1$ V, V_I^+ = 0, $V_O \leq$ +1.5 V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	$R_L \geq 15$ kΩ, V^+=15 V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, V_{RL} = 50 V, R_L = 5.1 kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	V_{RL} = 5 V, R_L = 5.1 kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.
CA139, CA139A (−55 to +125°C) | CA239, CA239A (−25 to +85°C) | CA339, CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than −0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V^+) − 1.5 V, but either or both inputs can go to +30 V without damage.

TYPICAL CHARACTERISTICS (Cont'd)

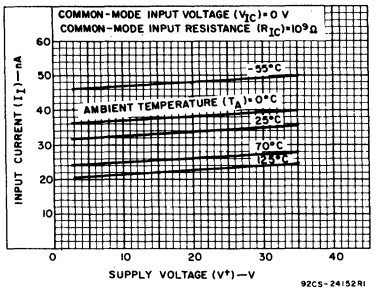


Fig. 4—Input current vs. supply voltage.

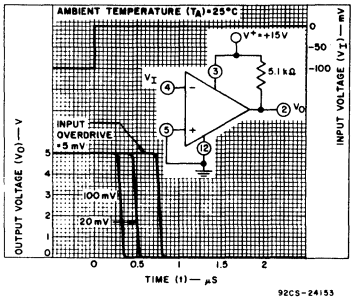


Fig. 5—Response time for various input overdrives—negative transition.

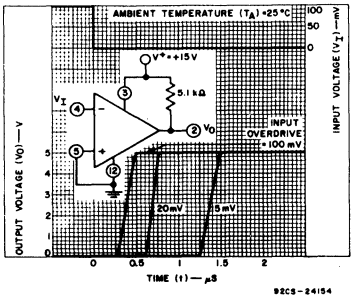


Fig. 6—Response time for various input overdrives—positive transition.

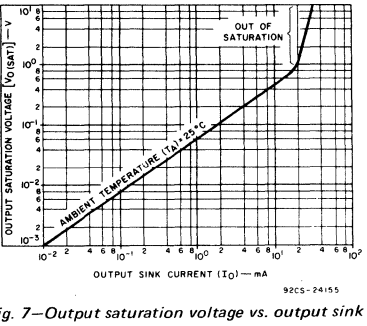


Fig. 7—Output saturation voltage vs. output sink current.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904 Types

Dual Operational Amplifiers

For Commercial, Industrial, and Military Applications

The RCA-CA158, –CA158A, –CA258, –CA258A, –CA358, –CA358A, and CA-2904 types consist of two independent, high gain, internally frequency compensated operational amplifiers which are designed specifically to operate from a single power supply over a wide range of voltages. They may also be operated from split power supplies. The supply current is basically independent of the supply voltage over the recommended voltage range.

These devices are particularly useful in interface circuits with digital systems and can be operated from the single common 5 Vdc power supply. They are also intended for transducer amplifiers, dc gain blocks and many other conventional op amp circuits which can benefit from the single power supply capability.

The CA158, CA158A, CA258, CA258A, CA358 and CA358A types are supplied in hermetic gold-CHIP 8-lead dual-in-line plastic packages (G suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads (DIL-CAN, S suffix). The CA2904 is supplied only in the gold-CHIP plastic package (G suffix).

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are an equivalent to or a replacement for the industry types 158, 158A, 258, 258A, 358, 358A, and 2904.

Features:

- **Internal frequency compensation for unity gain**
- **High dc voltage gain – 100 dB typ.**
- **Wide bandwidth at unity gain – 1 MHz typ.**
- **Wide power supply range:**
  - **Single supply . . . . . 3 to 30 V**
  - **Dual supplies . . . . . ± 1.5 to ± 15 V**
- **Low supply current – 1.5 mA typ.**
- **Low input bias current**
- **Low input offset voltage and current**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to V^+ range**
- **Large output voltage swing – 0 to V^+ –1.5 V**

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE, V^+:	
CA2904	26 V or ± 13 V
Other Types	32 V or ± 16 V
DIFFERENTIAL INPUT VOLTAGE:	
CA2904	± 26 V
Other Types	± 32 V
INPUT VOLTAGE	–0.3 V to V^+ V
INPUT CURRENT ($V_I < -0.3$ V) +	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	630 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/^{o}C
AMBIENT TEMPERATURE RANGE:	
Operating	–55 to + 125^{o}C
Storage	–65 to + 150^{o}C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 300 ^{o}C

+ This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than –0.3 V dc.

* The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

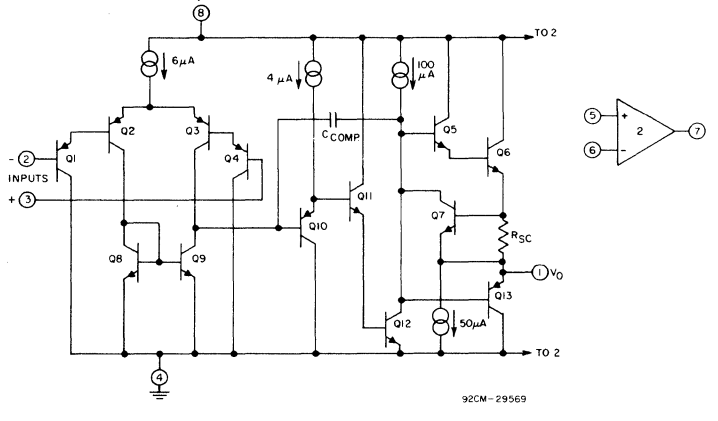


Fig. 1 – Schematic diagram – one of two operational amplifiers.

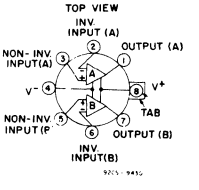


Fig. 2 – Functional diagram for CA158, CA258, and CA358 S- and T-suffix types.

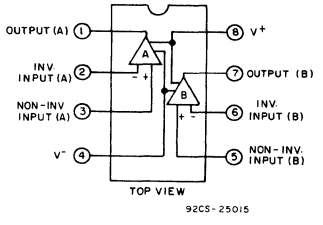


Fig. 3 – Functional diagram for CA158, CA258, CA358, and CA2904 G-suffix types.

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS Supply Voltage (V^+) = 5 V Unless Otherwise Specified	LIMITS CA258A (G, T, S) Min.	Typ.	Max.	UNITS
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	1	3	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	15	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	40	80	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –25 to +85°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

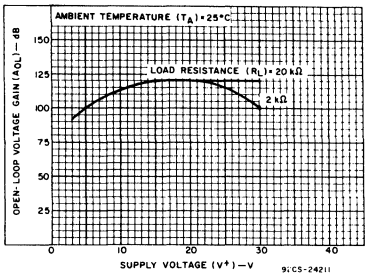


Fig.8 – Voltage gain as a function of supply voltage.

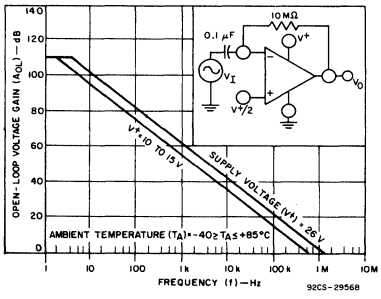


Fig.9 – Open-loop frequency response.

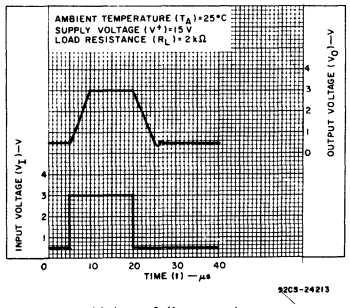


Fig.10 – Voltage follower pulse response.

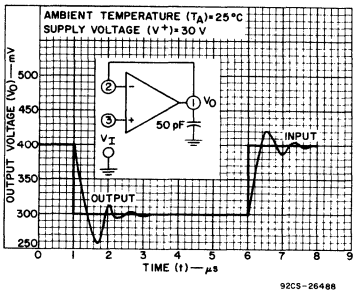


Fig.11 – Voltage follower pulse response (small signal).

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS Supply Voltage (V^+) = 5 V Unless Otherwise Specified	LIMITS CA158 (G, T, S) CA258 (G, T, S) Min.	Typ.	Max.	UNITS
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq 2$ kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –55 to + 125°C (CA158); T_A = –25 to +85°C (CA258)				
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	300	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

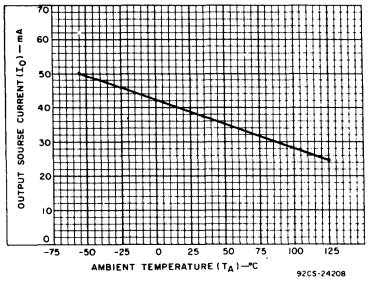


Fig. 16 — Output current as a function of ambient temperature.

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of thedevice. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS Supply Voltage (V^+) = 5 V Unless Otherwise Specified	LIMITS CA2904G			UNITS
		Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	$R_L \geq 10\ k\Omega$	0	–	$V^+ -1.5$	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, $V^+ = 30$ V	0	–	$V^+ -1.5$	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	$V_I^+ = +1$ V, $V_I^- = 0$ V, $V^+ = 15$ V	20	40	–	mA
Output Current (Sink), I_O	$V_I^+ = 0$ V, $V_I^- = 1$ V, $V^+ = 15$ V	10	20	–	mA
Short Circuit Output Current	$R_L = 0$ (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq 2\ k\Omega$, $V^+ = 15$ V (For large V_O swing)	–	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	50	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	50	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –40 to + 85°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	10	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	$R_S = 0$	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	45	200	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	$V^+ = 30$ V, Note 2	0	–	$V^+ -2$	V
Supply Current, I^+	$R_L = \infty$ On All Ampl.	–	0.7	1.2	mA
	$R_L = \infty$, $V^+ = 30$ V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: $V_O = 1.4\ V_{DC}$, $R_S = 0\ \Omega$ with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$, $V^+ = 5$ to 15 V unless otherwise specified*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA555			CA555C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
DC Supply Voltage, V^+		4.5	–	18	4.5	–	16	V
DC Supply Current (Low State)*, I^+	$V^+ = 5$ V, $R_L = \infty$	–	3	5	–	3	6	mA
	$V^+ = 15$ V, $R_L = \infty$	–	10	12	–	10	15	mA
Threshold Voltage, V_{TH}		–	(2/3)V^+	–	–	(2/3)V^+	–	V
Trigger Voltage	$V^+ = 5$ V	1.45	1.67	1.9	–	1.67	–	V
	$V^+ = 15$ V	4.8	5	5.2	–	5	–	
Trigger Current		–	0.5	–	–	0.5	–	μA
Threshold Current▲, I_{TH}		–	0.1	0.25	–	0.1	0.25	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		–	0.1	–	–	0.1	–	mA
Control Voltage Level	$V^+ = 5$ V	2.9	3.33	3.8	2.6	3.33	4	V
	$V^+ = 15$ V	9.6	10	10.4	9	10	11	V
Output Voltage Drop: Low State, V_{OL}	$V^+ = 5$ V, $I_{SINK} = 5$ mA	–	–	–	–	0.25	0.35	V
	$I_{SINK} = 8$ mA	–	0.1	0.25	–	–	–	
	$V^+ = 15$ V, $I_{SINK} = 10$ mA	–	0.1	0.15	–	0.1	0.25	
	$I_{SINK} = 50$ mA	–	0.4	0.5	–	0.4	0.75	
	$I_{SINK} = 100$ mA	–	2.0	2.2	–	2.0	2.5	
	$I_{SINK} = 200$ mA	–	2.5	–	–	2.5	–	
High State, V_{OH}	$V^+ = 5$ V, $I_{SOURCE} = 100$ mA	3.0	3.3	–	2.75	3.3	–	V
	$V^+ = 15$ V, $I_{SOURCE} = 100$ mA	13.0	13.3	–	12.75	13.3	–	
	$I_{SOURCE} = 200$ mA	–	12.5	–	–	12.5	–	
Timing Error (Monostable): Initial Accuracy	R_1, R_2 = 1 to 100 kΩ, C = 0.1 μF, Tested at $V^+ = 5$ V, $V^+ = 15$ V	–	0.5	2	–	1	–	%
Frequency Drift with Temperature		–	30	100	–	50	–	p/m/ ^oC
Drift with Supply Voltage		–	0.05	0.2	–	0.1	–	%/V
Output Rise Time, t_r		–	100	–	–	100	–	ns
Output Fall Time, t_f		–	100	–	–	100	–	ns

* When the output is in a high state, the dc supply current is typically 1 mA less than the low-state value.

▲ The threshold current will determine the sum of the values of R_1 and R_2 to be used in Fig. 16 (astable operation): the maximum total $R_1 + R_2 = 20$ MΩ.

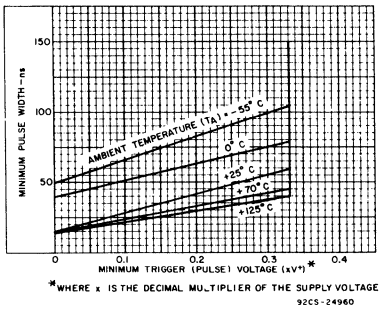


Fig. 4 – Minimum pulse width vs. minimum trigger voltage.

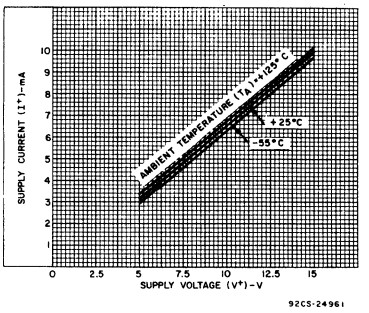


Fig. 5 – Supply current vs. supply voltage.

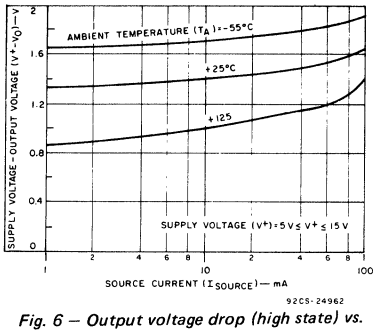


Fig. 6 – Output voltage drop (high state) vs. source current.

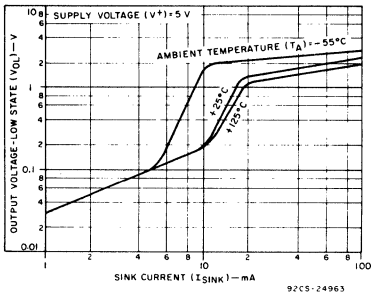
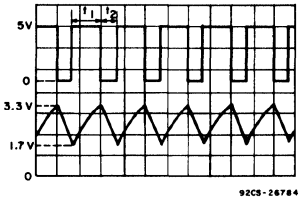


Fig.7 – Output voltage-low state vs. sink current at $V^+ = 5$ V.



Top Trace: Output voltage (2V/div. and 0.5 ms/div.)
Bottom Trace: Capacitor voltage (1 V/div. and 0.5 ms/div.)

Fig. 17 – Typical waveforms for repeat cycle timer.

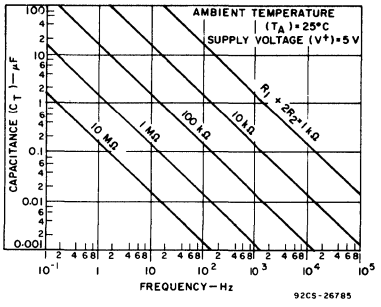


Fig. 18 – Free running frequency of repeat cycle timer with variation in capacitance and resistance.

ELECTRICAL CHARACTERISTICS at T_A = 25 C, $V^+ = V_C = V_I$ = 12 V, V^- = 0, V_O = 5 V, I_L = 1 mA, C_1 = 100 pF, C_{REF} = 0, R_{SCP} = 0, unless otherwise specified. Divider impedance R_1R_2 R_1+R_2 at non-inverting input, Term. 5, = 10 kΩ (see Fig. 23).

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Regulator Current, I_Q	I_L = 0, V_I = 30 V	–	2.3	3.5	–	2.3	4	mA
Input Voltage Range, V_I		9.5	–	40	9.5	–	40	V
Output Voltage Range, V_O		2	–	37	2	–	37	V
Differential Input-Output Voltage, V_I–V_O		3	–	38	3	–	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (See Note 1)	V_I = 12 to 40 V	–	0.02	0.2	–	0.1	0.5	%V_O
	V_I = 12 to 15 V	–	0.01	0.1	–	0.01	0.1	
	V_I = 12 to 15 V, T_A = −55 to +125°C	–	–	0.3	–	–	–	
	V_I = 12 to 15 V, T_A = O to 70°C	–	–	–	–	–	0.3	
Load Regulation (See Note 1)	I_L = 1 to 50 mA	–	0.03	0.15	–	0.03	0.2	%V_O
	I_L = 1 to 50 mA, T_A = −55 to +125°C	–	–	0.6	–	–	–	
	I_L = 1 to 50 mA, T_A = 0 to 70°C	–	–	–	–	–	0.6	
Output-Voltage Temp. Coefficient, $\triangle V_O$	T_A = −55 to +125°C	–	0.002	0.015	–	–	–	%/°C
	T_A = 0 to 70°C	–	–	–	–	0.003	0.015	
Ripple Rejection (See Note 2)	f = 50 Hz to 10 kHz	–	74	–	–	74	–	dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF	–	86	–	–	86	–	
Short-Circuit Limiting Current, I_{LIM}	R_{SCP} = 10 Ω, V_O = 0	–	65	–	–	65	–	mA
Equivalent Noise RMS Output Voltage, V_N (See Note 2)	BW = 100 Hz to 10 kHz, C_{REF} = 0	–	20	–	–	20	–	μV
	BW = 100 Hz 10 kHz, C_{REF} = 5 μF	–	2.5	–	–	2.5	–	

Note 1: Line and load regulation specifications are given for condition of a constant chip temperature. For high-dissipation conditions, temperature drifts must be separately taken into account.

Note 2: For C_{REF}, see Fig. 23.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

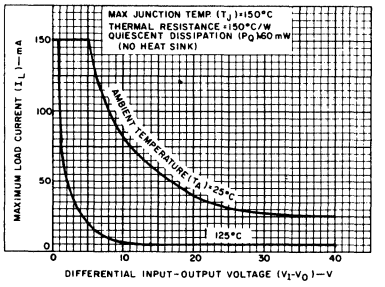


Fig. 5 – Max. load current vs differential input-output voltage.

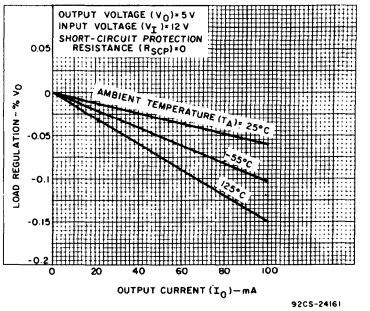


Fig. 6 – Load regulation without current limiting.

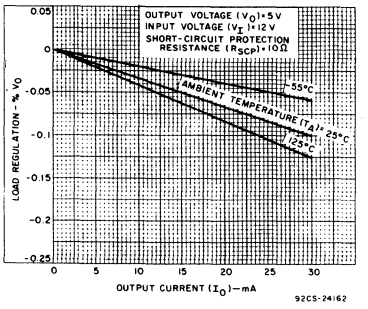


Fig. 7 – Load regulation with current limiting.

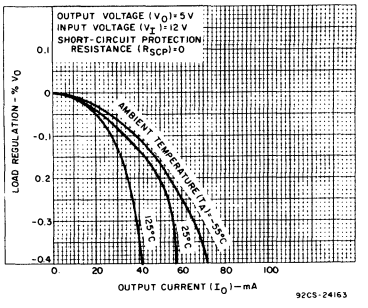


Fig. 8 – Load regulation with current limiting.

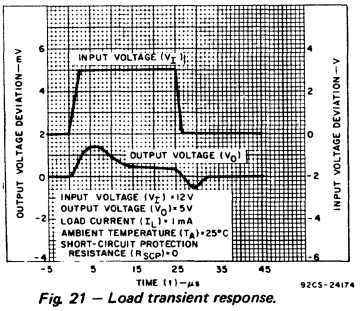


Fig. 21 – Load transient response.

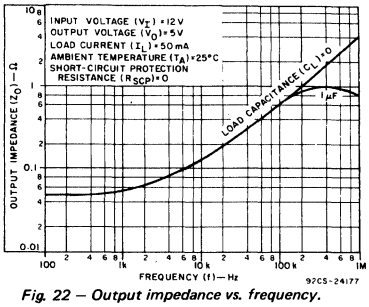
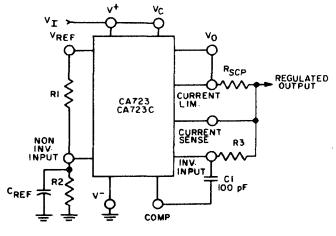


Fig. 22 – Output impedance vs. frequency.

TYPICAL APPLICATION CIRCUITS



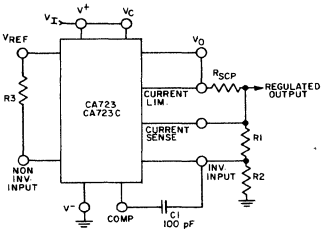
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 50 mA)	1.5 mV

Note: $R3 = \frac{R1\ R2}{R1+R2}$ for minimum temperature drift

92CS-24178

Fig. 23 – Low-voltage regulator circuit (V_O = 2 to 7 volts).



CIRCUIT PERFORMANCE DATA:

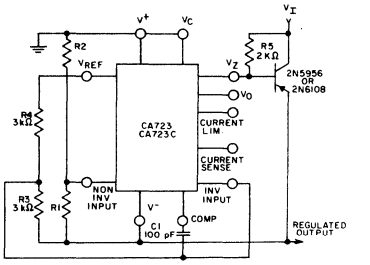
REGULATED OUTPUT VOLTAGE	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 50 mA)	4.5 mV

Note: $R3 = \frac{R1\ R2}{R1+R2}$ for minimum temperature drift

R3 may be eliminated for minimum component count.

92CS-24179

Fig. 24 – High-voltage regulator circuit (V_O = 7 to 37 volts).



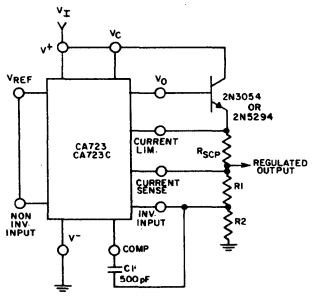
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	−15 V
LINE REGULATION (ΔV_I = 3 V)	1 mV
LOAD REGULATION (ΔI_L = 100 mA)	2 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24180R1

Fig. 25 – Negative-voltage regulator circuit.

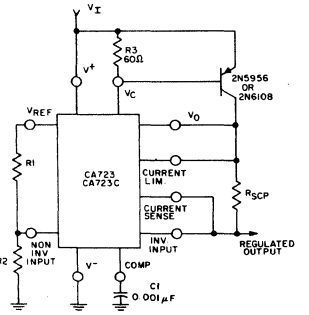


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 1 A)	15 mV

92CS-24181R1

Fig. 26 – Positive-voltage-regulator circuit (with external n-p-n pass transistor).

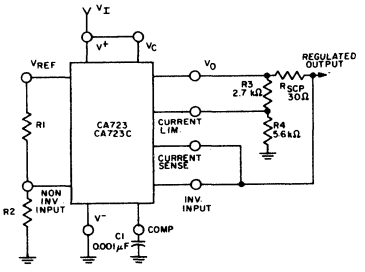


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 1 A)	5 mV

92CS-24182R1

Fig. 27 – Positive voltage-regulator circuit (with external p-n-p pass transistor).

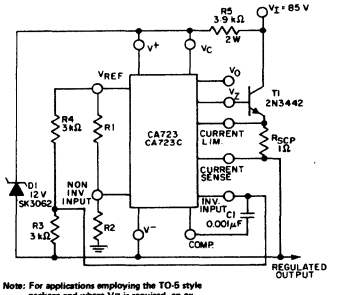


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 10 mA)	1 mV
SHORT-CIRCUIT CURRENT	20 mA

92CS-24183

Fig. 28 – Foldback current-limiting circuit.



Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	50 V
LINE REGULATION (ΔV_I = 20 V)	15 mV
LOAD REGULATION (ΔI_L = 50 mA)	20 mV

92CS-24184

Fig. 29 – Positive-floating regulator circuit.

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)
CA1458	dual	int.	no	20k	6	0 to +70▲
CA1558	dual	int.	no	50k	5	−55 to +125
CA741C	single	int.	yes	20k	6	0 to +70▲
CA741	single	int.	yes	50k	5	−55 to +125
CA747C	dual	int.	yes*	20k	6	0 to +70▲
CA747	dual	int.	yes*	50k	5	−55 to +125
CA748C	single	ext.	yes	20k	6	0 to +70▲
CA748	single	ext.	yes	50k	5	−55 to +125

*In the 14-lead dual-in-line plastic package only.

▲All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

Type No.	PACKAGE TYPE AND SUFFIX LETTER										FIG. No.
	TO-5 STYLE			PLASTIC		Gold-CHIP PLASTIC		CHIP	Gold-CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L	8L	14L				
CA1458	T		S	E		G		H	GH		1d, 1h
CA1558	T		S	E		G					1d, 1h
CA741C	T		S	E		G		H	GH		1a, 1e
CA741	T		S	E		G				L	1a, 1e
CA747C		T			E		G	H	GH		1b, 1f
CA747		T			E		G				1b, 1f
CA748C	T		S	E		G		H	GH		1c, 1g
CA748	T		S	E		G					1c, 1g

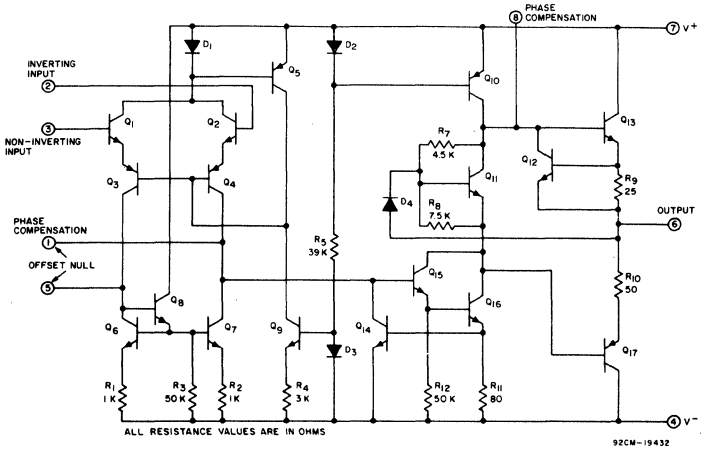
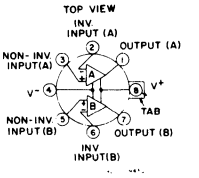
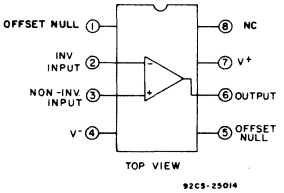


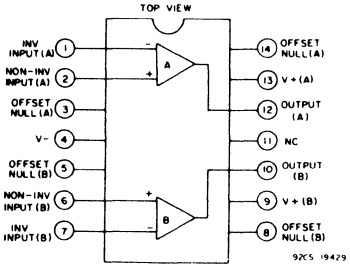
Fig.2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.



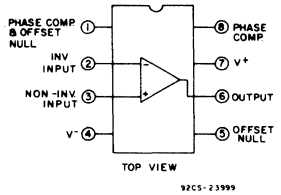
1d.—CA1458S,CA1458T,CA1558S, and CA1558T and internal phase compensation.



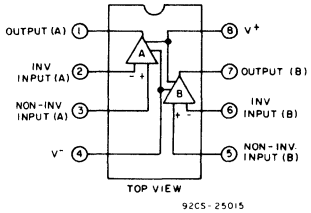
1e.—CA741CE,CA741CG,CA741E, and CA741G with internal phase compensation.



1f.—CA747CE,CA747CG,CA747E, and CA747G with internal phase compensation.



1g.—CA748CE,CA748CG,CA748E, and CA748G with external phase compensation.



1h.—CA1458E,CA1458G,CA1558E, and CA1558G with internal phase compensation.

Fig. 1 — Functional Diagrams (Cont'd)

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, V^+ = 15 V, V^- = −15 V	Ambient Temperature, T_A	LIMITS CA741C CA747C* CA748C CA1458* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S \leq 10\,k\Omega$	25 °C	–	2	6	mV
		0 to 70 °C	–	–	7.5	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		0 to 70 °C	–	–	300	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		0 to 70 °C	–	–	800	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$ $V_O = \pm 10$ V	25 °C	20,000	200,000	–	
		0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\,k\Omega$	25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	25 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	25 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	25 °C	±10	±13	–	
		0 to 70 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
Device Dissipation, P_D		25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS $V^{\pm}$ = ±15 V	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance, R_O		75	Ω
Output Short-Circuit Current		25	mA
Transient Response: Rise Time, t_r	Unity gain V_I = 20 mV R_L = 2 kΩ $C_L \leq$ 100 pF	0.3	μs
Overshoot		5	%
Slew Rate, SR: Closed-loop	$R_L \geq 2\,k\Omega$	0.5	V/μs
Open-loop▲		40	

▲ Open-loop slew rate applies only for types CA748C and CA748.

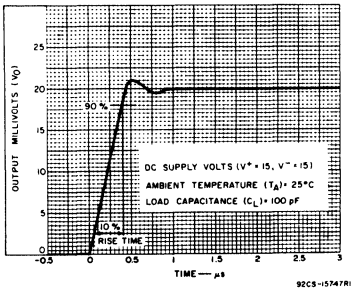


Fig.8—Output voltage vs. transient response time for CA741C and CA741.

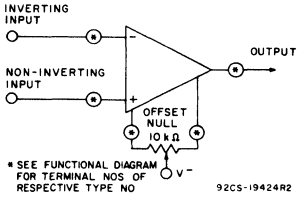


Fig.9—Voltage-offset null circuit for CA741C, CA741, CA747CE, CA747CG, CA747E, and CA747G.

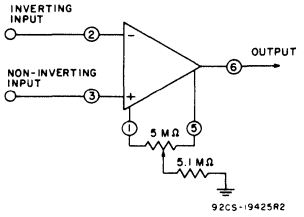


Fig.10—Voltage-offset null circuit for CA748C and CA748.

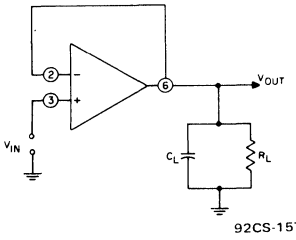


Fig.11—Transient response test circuit for all types.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS: $V^+ = 5V$, $V^- = -5V$; V_{TH} ADJ. = $-5V \pm 1\%$, (Term. 13); $C_{EXT} = 0.01\ \mu F$; $T_A = 25°C$ (unless indicated otherwise)		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Static (DC) Characteristics							
Power Dissipation	P_D			–	140	180	mW
Input Offset Current	I_{IO}			–	1	2	μA
Input Bias Current:							
$T_A = 25°C$	I_{IB}		$V_5 = V_6 = V_3 = V_4 = 0$	–	5	25	μA
$T_A = -55°C$				–	–	50	
Output Voltage:							
High	V_{OH}	$I_{OM} = 200\ \mu A$		3	–	–	V
Low –							
$T_A = 25°C$	V_{OL}	$V_{14} = 5\ V$, $I_9 = 10\ mA$		–	–	350	mV
$T_A = 125°C$				–	–	400	
Strobe Load Current	I_S	$V_{12} = 0$		–	–	1.5	mA
Strobe Reverse Current:							
$T_A = 25°C$	I_{SR}	$V_{12} = 5V$		–	–	2	μA
$T_A = 125°C$				–	–	25	
Input Gate Load Current	I_G	$V_{10} = V_{11} = 0$		–	–	2.5	mA
Input Gate Reverse Current:							
$T_A = 25°C$	I_{GR}	$V_{10} = V_{11} = 5V$		–	–	2	μA
$T_A = 125°C$				–	–	25	
Switching Characteristics							
Input Threshold Voltage:							
$T_A = 25°C$	V_{TH}			14	17	20	mV
$T_A = -55$ to $125°C$				12	17	22	
Input Offset Voltage	V_{IO}			–	1	6	mV
Input Gate Voltage:							
High	V_{GH}	$V_3 = V_5 = 25\ mV$,		–	1.6	–	V
Low	V_{GL}	$V_4 = V_6 = 0$		–	0.7	–	
Common-Mode Range:							
Input Gate High	V_{CM}			–	±1.5	–	V
Input Gate Low				–	±1.5	–	
Differential-Mode Range:							
Input Gate High	V_{DH}			–	±600	–	mV
Input Gate Low	V_{DL}			–	±1.5	–	V
Propagation Delay:							
Input to Amplifier Output	t_{IA}	$V_3 = 25\ mV$ (pulsed),		–	10	15	ns
Input to Output	t_{IO}	$V_{12} = 2V$		–	20	30	
Strobe to Output	t_{SO}	$V_3 = V_4 = V_5 = V_6 = 0$, $V_{12} = 2V$ (pulsed)		–	15	20	
Gate Input to Amplifier Output	t_{GA}	$V_{11} = 2V$ (pulsed)		–	10	15	
Gate Input to Amplifier Input	t_{GI}	$V_3 = 25\ mV$		–	30	35	
Common-Mode Recovery Time:							
Input Gate High	t_{CMR}	$V_3 = V_5 = 1.5\ V$		–	15	30	ns
Input Gate Low				–	15	30	
Differential-Mode Recovery Time:							
Input Gate High	t_{DR}	$V_3 = V_5 = 400\ mV$		–	30	–	ns
Input Gate Low				–	0	–	

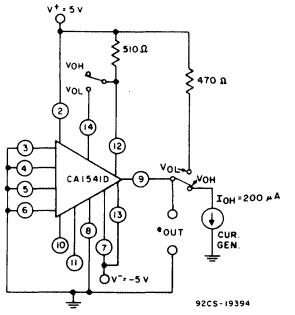
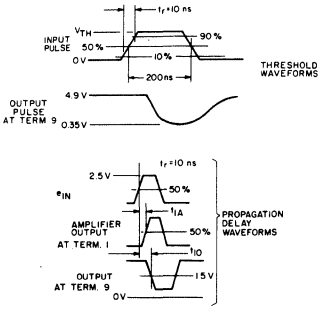


Fig. 5 – Test circuit for measurement of low (V_{OL}) and high (V_{OH}) output voltage levels.



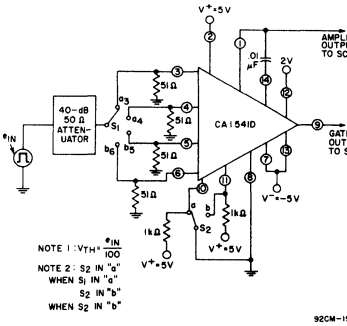


Fig. 6 – Threshold propagation delay, gate and input-offset test circuit with associated pulse wave forms.

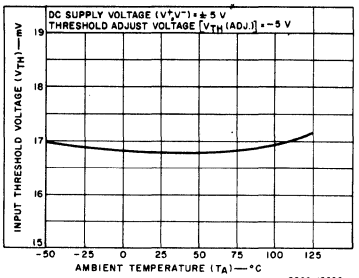


Fig. 7a – Input V_{TH} vs. T_A.

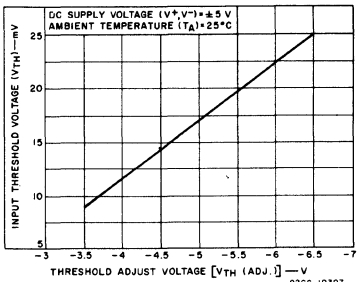


Fig. 7b – Input V_{TH} vs. V_{TH} (ADJ.).

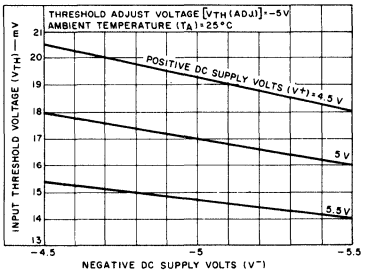


Fig. 7c – Input V_{TH} vs. V^-.

FM IF Amplifier-Limiter and Quadrature Detector

For FM IF and TV Sound IF Applications

The CA2111A, on a single monolithic chip, provides a multi-stage wideband amplifier-limiter, a quadrature detector, and an emitter-follower output stage. This device is designed for use in FM receivers and in the sound IF sections of TV receivers. In addition, an output terminal is provided which allows the use of the amplifier-limiter as a straight 60-dB wideband amplifier.

The amplifier-limiter features the excellent limiting characteristics of 3 cascaded differential amplifiers.

The quadrature detector requires only one coil in the associated outboard circuit and therefore, tuning is a simple procedure.

A unique feature of the CA2111A is its exceptionally low AFC voltage drift over the full operating-temperature range.

This device can be supplied in either dual-in-line or quad-in-line 14-lead plastic packages (CA2111AE and CA2111AQ, respectively).

Features:

- **Direct replacement for ULN2111A and MC1357**
- **Good sensitivity: Input limiting voltage (knee) (400 μV typ. at 10.7 MHz; 250 μV typ. at 4.5 MHz and 5.5 MHz)**
- **Excellent AM rejection (45 dB typ. at 10.7 MHz)**
- **Provision for output from 3-stage IF amplifier section**
- **Low harmonic distortion**
- **Quadrature detection permits simplified single-coil tuning**
- **Extremely low AFC voltage drift over full operating-temperature range**
- **Minimum number of external parts required**

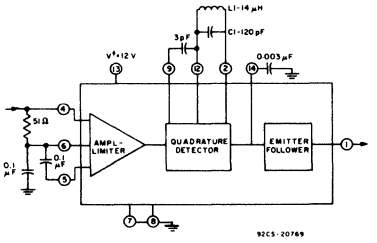


Fig. 1—Block diagram of CA2111A and associated outboard components.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC Supply Voltage [between terminals 13 (V^+) and 7 (V^-)]	16	V
Device Dissipation:		
Up to T_A = 60°C	600	mW
Above T_A = 60°C	derate linearly 6.7 mW/°C	
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max.	+265	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
DC Voltage:						
At Terminal 1	V_1	V^+ = 12V	–	5.4	–	V
		= 8V	–	3.7	–	
At Terminals 4, 5, 6, 10	$V_{4,5,6,10}$	V^+ = 8V	–	1.35	–	
At Terminals 2, 12	$V_{2,12}$		–	3.5	–	
DC Current (into Terminal 13)						
At V^+ = 8V			–	14	–	mA
At V^+ = 12V	I_{13}		–	16	–	
Amplifier Input Resistance	R_4	f_0 = 10.7 MHz	–	7	–	kΩ
Amplifier Input Capacitance	C_4		–	11	–	pF
Detector Input Resistance	R_{12}		–	70	–	kΩ
Detector Input Capacitance	C_{12}		–	2.7	–	pF
Amplifier Output Resistance	R_{10}		–	60	–	Ω
Detector Output Resistance	R_1		–	200	–	Ω
De-Emphasis Resistance	R_{14}		–	8.8	–	kΩ

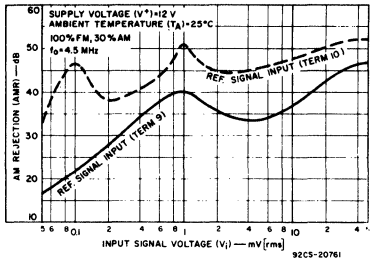


Fig. 2—AM rejection vs input voltage (4.5 MHz).

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
FM Modulation Frequency = 400 Hz, Source Resistance = 50Ω

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: f_0 = 10.7 MHz, Δf = ± 75 KHz, V^+ = 12V	TEST CONDITIONS: f_0 = 10.7 MHz, Δf = ± 75 KHz, V^+ = 8V	TEST CONDITIONS: f_0 = 4.5 MHz, Δf = ± 25 KHz, V^+ = 12V	TEST CONDITIONS: f_0 = 5.5 MHz, Δf = ± 50 KHz, V^+ = 12V	UNITS	TEST CIRCUIT OR CHARACTERISTIC CURVES FIG. NO.
		LIMITS TYP.	LIMITS MAX.	LIMITS TYP.	LIMITS MAX.		
AMPL-LIMITER							
Input Limiting Threshold Voltage	V_i(lim) (4)	400	600	400	600	V (RMS)	7, 6, 8, 9
AM Rejection‡ *	AMR(1)	45	–	37	–	dB	2, 7, 5, 6
Ampl. Voltage Gain▲	A_V(10)	55	–	55	–	dB	7
DETECTOR							
Recovered Audio‡ Output Voltage	V_o(AF) (1)	0.48	–	0.3	–	V (RMS)	6, 7, 8, 9
Total Harmonic‡ Distortion	THD(1)	1	–	1	–	%	7

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: f_0 = 10.7 MHz, Δf = ± 75 KHz, V^+ = 12V	TEST CONDITIONS: f_0 = 10.7 MHz, Δf = ± 75 KHz, V^+ = 8V	TEST CONDITIONS: f_0 = 4.5 MHz, Δf = ± 25 KHz, V^+ = 12V	TEST CONDITIONS: f_0 = 5.5 MHz, Δf = ± 50 KHz, V^+ = 12V	UNITS	TEST CIRCUIT OR CHARACTERISTIC CURVES FIG. NO.
		LIMITS TYP.	LIMITS MAX.	LIMITS TYP.	LIMITS MAX.		
AMPL-LIMITER							
Input Limiting Threshold Voltage	V_i(lim) (4)	400	600	400	600	V (RMS)	7, 6, 8, 9
AM Rejection‡ *	AMR(1)	45	–	37	–	dB	2, 7, 5, 6
Ampl. Voltage Gain▲	A_V(10)	55	–	55	–	dB	7
DETECTOR							
Recovered Audio‡ Output Voltage	V_o(AF) (1)	0.48	–	0.3	–	V (RMS)	6, 7, 8, 9
Total Harmonic‡ Distortion	THD(1)	1	–	1	–	%	7

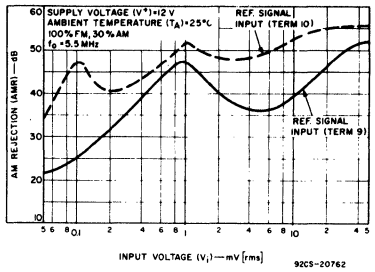


Fig. 3—AM rejection vs input voltage (5.5 MHz).

‡V_i = 10 mV (RMS) ▲$V_i \leq 50$ μV (rms) *100% FM, 30% AM

DC Amplifier

- Designed for use in Communication, Telemetry, Instrumentation, and Data-Processing Equipment
- Balanced differential-amplifier configuration with controlled constant-current source to provide outstanding versatility
- Built-in temperature stability for operation from -55°C to +125°C
- Companion Application Note, ICAN 5030 "Applications of RCA CA3000 Integrated Circuit DC Amplifier" covers characteristics of different operating modes, frequency considerations, 10 MHz narrow band tuned amplifier design, crystal oscillator design, and many other application aids
- 10-Lead hermetic TO-5 style package

HIGHLIGHTS

- Input Impedance . . . . . 195 kΩ typ.
- Voltage Gain. . . . . 30 dB typ.
- Common-Mode Rejection Ratio . . . 98 dB typ.
- Input Offset Voltage. . . . . 1.4 mV typ.
- Push-Pull Input and Output
- Frequency Capability
  DC to 30 MHz (with external C and R)
- Wide AGC Range. . . . . 90 dB typ.

APPLICATIONS

- Schmitt Trigger
- RC-Coupled Feedback Amplifier
- Mixer
- Comparator
- Modulator
- Crystal Oscillator
- Sense Amplifier

ABSOLUTE-MAXIMUM VOLTAGE LIMITS

at T_{FA} = 25°C

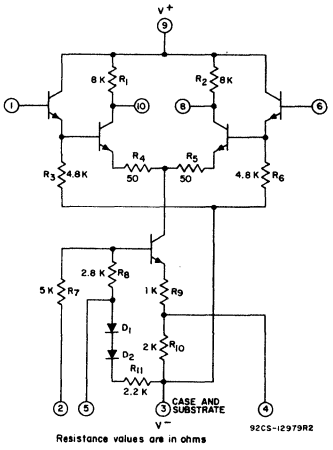
OPERATING-TEMPERATURE RANGE . . . −55°C to +125°C
STORAGE-TEMPERATURE RANGE . . . −65°C to +150°C
LEAD-TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

MAXIMUM POWER SUPPLY VOLTAGE . . 16 or ±8 V

MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE . . ±4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE . . ±2 V
MAXIMUM DEVICE DISSIPATION:
From −55°C to 85°C. . . . . 450 mW
Above 85°C . . . . . Derate 5 mW/°C

ELECTRICAL CHARACTERISTICS, at T_{FA} = 25°C, V_{CC} = +6V, V_{EE} = -6V, unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified		TEST CIRCUITS	LIMITS TYPE CA3000				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}				-	1.4	5	mV	2
Input Offset Current	I_{IO}				-	1.2	10	μA	2
Input Bias Current	I_{IB}				-	23	36	μA	3
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS 4	5						
		NC	NC		-	2.6	-	V	4
		NC	VEE		-	4.2	-	V	4
		VEE	NC		-	-1.5	-	V	4
		VEE	VEE		-	0.6	-	V	4
Device Dissipation	P_D	NC	NC		-	30	-	mW	NONE
DYNAMIC CHARACTERISTICS									
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kHz		6	28	32	-	dB	5
		Double-Ended Output f = 1 kHz		6	-	38	-	dB	5
Bandwidth at -3 dB Point	BW	V_i = 10 mV, R_s = 1 kΩ			-	650	-	kHz	7
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kHz		6	-	6.4	-	V(P-P)	NONE
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		9	70	98	-	dB	8
Single-Ended Input Impedance	Z_{IN}	f = 1 kHz		11	70K	195K	-	Ω	10
Single-Ended Output Impedance	Z_{OUT}	f = 1 kHz		13	5.5K	8K	10.5K	Ω	12
Total Harmonic Distortion	THD	R_S=1kΩ f = 1 kHz V_O=42V_{p-p}			-	0.2	5	%	14
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kHz		15	80	90	-	dB	NONE



Resistance values are in ohms

Fig.1 SCHEMATIC DIAGRAM

STATIC CHARACTERISTICS FOR TYPE CA3000

INPUT OFFSET VOLTAGE AND CURRENT vs TEMPERATURE

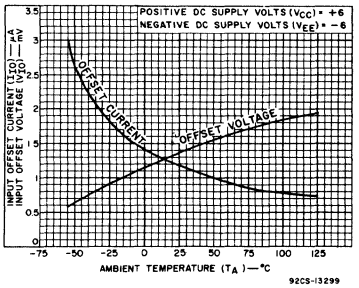


Fig.2

INPUT BIAS CURRENT vs TEMPERATURE

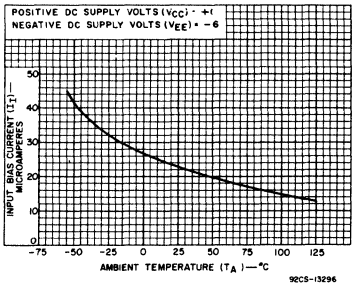


Fig.3

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

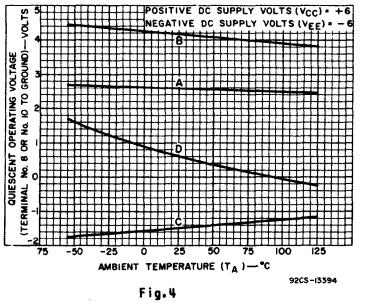


Fig.4

Video and Wideband Amplifier

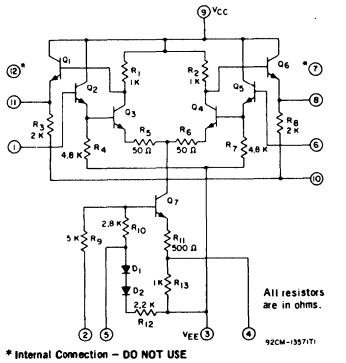
- Designed for use in Video Systems and Communication Equipment
- Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility
- Built-in temperature stability for operation from -55°C to +125°C
- Emitter follower input & output
- Companion Application Note ICAN5038 "Application of the RCA-CA3001 Integrated-Circuit Video Amplifier", covers different operating modes, gain control, distortion, swing capability, 3 stage amplifier design, and a Schmitt trigger study.
- 12-Lead Hermetic TO-5 Style Package

HIGHLIGHTS

• Push-Pull Input & Output	
• AGC Range	60 dB typ.
• Bandwidth	29 MHz
• Input Resistance	150 kΩ typ.
• Output Resistance	45 Ω typ.
• Voltage Gain	19 dB typ.
• Input Offset Voltage	1.5 mV typ.

APPLICATIONS

- Schmitt Trigger
- Mixer
- Modulator
- DC, IF, & Video Amplifier



* Internal Connection – DO NOT USE

Fig.1 - Schematic Diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS at T_A = 25°C

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals.
All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10	0 -6 +6
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10 & No.11	0 -6 +6
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

OPERATING TEMPERATURE RANGE	-55°C to +125°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	± 4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	± 2.5 V
MAXIMUM DEVICE DISSIPATION:	
-55 to 85°C	450 mW
Above 85°C	Derate linearly 5 mW/°C

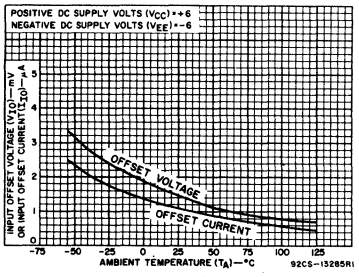


Fig.2 - Input offset voltage and current vs. temperature.

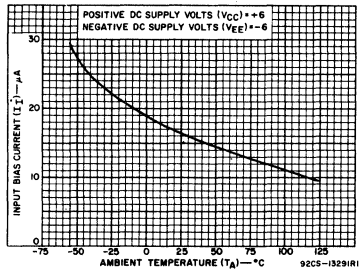


Fig.3 - Input bias current vs. temperature.

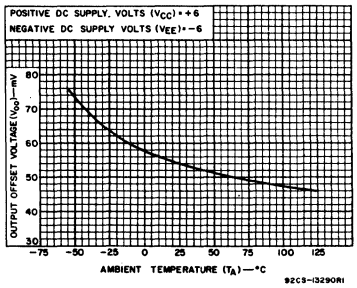


Fig. 4 - Output offset voltage vs. temperature.

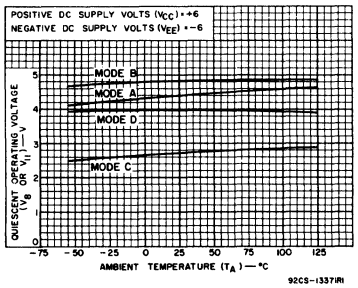


Fig. 5 - Quiescent operating voltage vs. temperature.

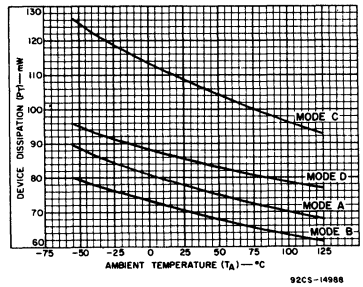
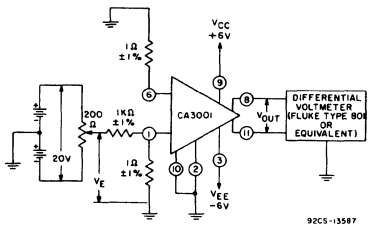


Fig. 6 - Device dissipation vs. temperature.



1. Adjust V_E for $V_{OUT(DC)} = 0 \pm 0.1$ V 2. Measure V_E and record input offset voltage (V_{IO}) in mV as $V_{IO} = \frac{V_E}{1000}$

Fig. 12 - Input offset voltage test circuit.

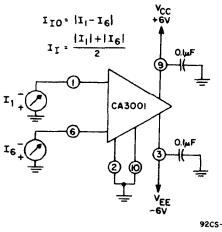
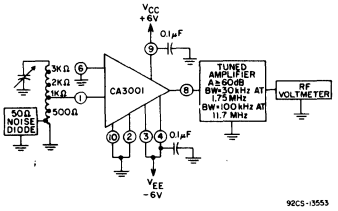
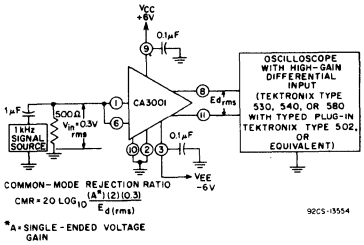


Fig. 13 - Input offset current and input bias current test circuit.



* Separate tuned input circuits are used for 1.75 MHz and 11.7 MHz. Source-resistance matching taps adjusted with circuit tuned to resonance and with 50-ohm resistor connected to simulate noise diode.

Fig. 14 - Noise figure test circuit.



*A = SINGLE-ENDED VOLTAGE GAIN

Fig. 15 - Common-mode rejection ratio test circuit.

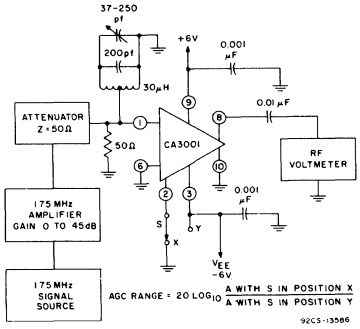


Fig. 16 - AGC range test circuit.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{CC} = +6 V, V_{EE} = -6 V

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS TERMINALS No.3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED	TEST CIRCUITS	LIMITS CA3002				TYPICAL CHARACTERISTICS CURVES
			Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:								
Input Offset Voltage	V_{IO}		4	-	2.2	-	mV	2
Input Unbalance Current	I_{IU}			-	2.2	10	μA	2
Input Bias Current	I_I			-	20	36	μA	3
Quiescent Operating Voltage		MODE A: TERMINAL 2 = V_{EE}, TERMINAL 4 = NC		-	2.8	-	V	4
		MODE B: TERMINAL 2 = V_{EE}, TERMINAL 4 = V_{EE}		-	3.9	-	V	4
Device Dissipation	P_T			-	55	-	mW	None
DYNAMIC CHARACTERISTICS:								
Differential Voltage Gain (Single-Ended Input and Output)	A_{DIFF}	V_{IN} = 10 mV, f = 1.75 MHz, R_S = 50Ω		19	24	-	dB	5 & 15
Bandwidth at -3 dB Point	BW	R_S = 50Ω, V_{IN} = 10 mV		-	11	-	MHz	6
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	-		-	5.5	-	V_{P-P}	None
Noise Figure	NF	f = 1.75 MHz R_S = 1 kΩ	8	-	4	8	dB	7
Input Impedance Components: Parallel Input Resistance	R_{IN}	f = 1.75 MHz	None	-	100k	-	Ω	None
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz	None	-	4	-	pF	None
Output Resistance	R_{OUT}	f = 1.75 MHz	14	-	70	-	Ω	9a & 9b
AGC Range (Maximum Voltage Gain to Complete Cutoff	AGC	f = 1.75 MHz	13	60	80	-	dB	12

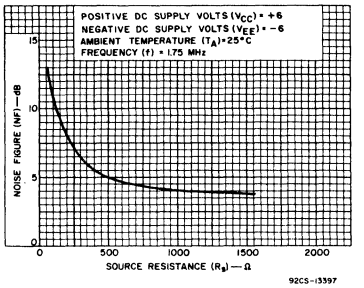
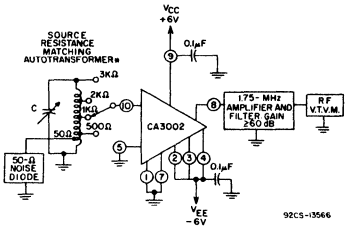


Fig. 7 - Noise figure vs source resistance.



*Taps are adjusted to provide indicated equivalent values of R_S with tank tuned to resonance at 1.75 MHz, and a 50-Ω resistor connected to simulate the noise diode.

Fig. 8 - Noise figure.

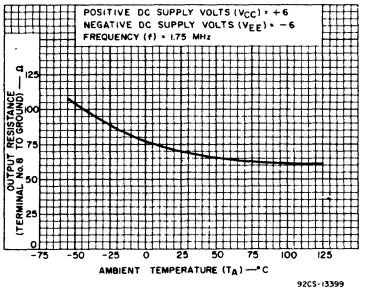


Fig. 9a - Output resistance vs temperature.

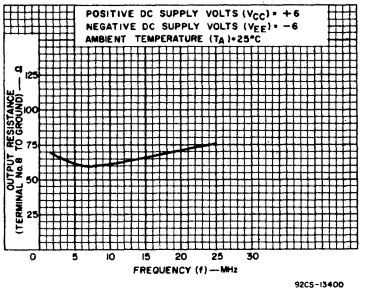


Fig. 9b - Output resistance vs frequency.

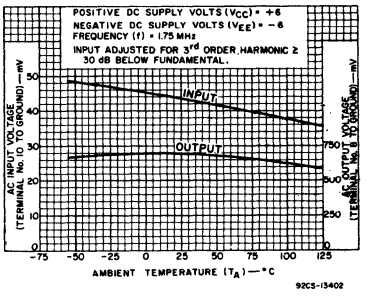
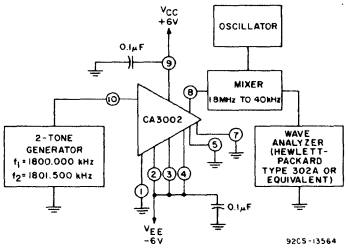


Fig. 10 - Input level for — 30 dB intermodulation vs. temperature



1) Increase both input-signal tones until the $2f_2$-$f1$ and $2f_1$-$f2$ output-signal voltages are 30 dB below the f_1 and f_2 output-signal voltages.
2) Measure rms values of the input and output signal voltages.
3) The measured input signal voltage is that value when the 3rd-harmonic intermodulation products are 30 dB below the fundamental outputs.

Fig. 11 - Intermodulation Test Circuit.

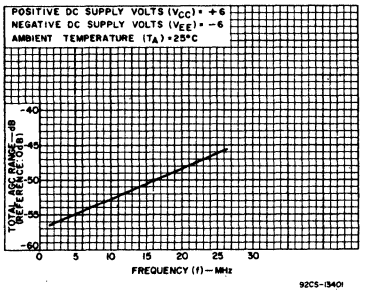
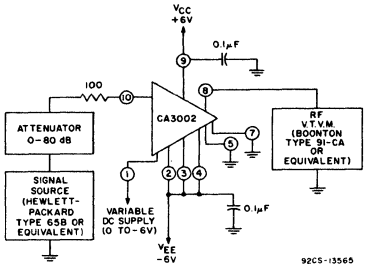


Fig. 12 - AGC range vs frequency.



1) Set attenuator at 80 dB attenuation.
2) Set variable dc supply voltage at 0 V.
3) Increase signal input voltage until RF V.T.V.M. indicates 5 mV output.
4) Set variable dc supply voltage at -6 V.
5) Adjust attenuator until RF V.T.V.M. again indicates 5 mV output.
6) Change in attenuator setting in dB is total AGC Range.

Fig. 13 - AGC range.

ELECTRICAL CHARACTERISTICS, at T_{FA} = 25° C, V_{CC} = +6V, V_{EE} = -6 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Open Unless Otherwise Specified		TEST CIRCUIT	LIMITS TYPE CA3004				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}			Fig.4	–	1.7	5	mV	Fig.2
Input Offset Current	I_{IO}			Fig.5	–	0.125	5	μA	Fig.2
Input Bias Current	I_I			Fig.5	–	21	40	μA	Fig.3
		TERMINALS 4	5						
Quiescent Operating Current	I_9 or I_{11}	NC	NC	Fig.8	–	1	–	mA	Fig.6
		V_{EE}	NC	Fig.8	–	2.7	–	mA	Fig.6
		NC	V_{EE}	Fig.8	–	0.45	–	mA	Fig.6
		V_{EE}	V_{EE}	Fig.8	–	1.25	–	mA	Fig.6
Quiescent Operating Current Ratio	I_9/I_{11}			Fig.8	–	1.1	–	–	Fig.7
Device Dissipation	P_T			Fig.8	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS									
Power Gain	G_P	f = 100 Mc/s		Fig.11	10	12	–	dB	Fig.9
Noise Figure	NF	f = 100 Mc/s		Fig.11	–	6.3	9	dB	Fig.10
Common Mode Rejection Ratio	CMR	f = 1 Kc/s		Fig.13	–	98	–	dB	Fig.12
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 Mc/s		Fig.14	-60	–	–	dB	NONE

DEFINITIONS OF TERMS

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Quiescent Operating Current Ratio

The ratio of the Quiescent operating currents in the two output terminals.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Common-Mode Voltage Gain

The ratio of the signal voltages developed between the two output terminals to the signal voltage applied to the two input terminals connected in parallel for ac.

Differential Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device

INPUT OFFSET VOLTAGE TEST CIRCUIT

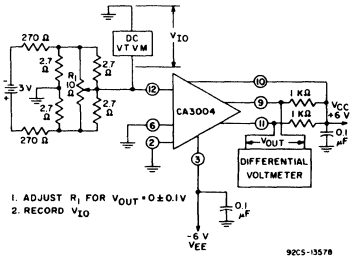


Fig.4

INPUT OFFSET CURRENT AND BIAS CURRENT TEST CIRCUIT

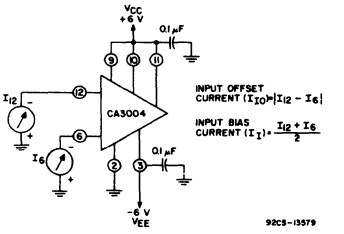


Fig.5

QUIESCENT OPERATING CURRENT VS TEMPERATURE

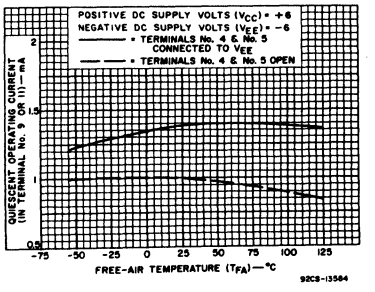


Fig.6

TEST CIRCUIT FOR TYPE CA3004

QUIESCENT OPERATING CURRENT RATIO VS TEMPERATURE

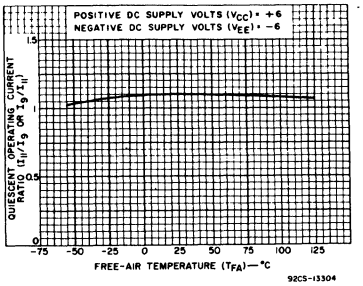
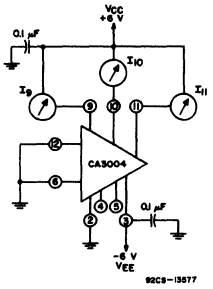


Fig.7

QUIESCENT OPERATING CURRENT, QUIESCENT OPERATING CURRENT RATIO, AND DEVICE DISSIPATION TEST CIRCUIT



$P_T = V_{CC}(I_9 + I_{10} + I_{11}) + V_{EE} I_3$

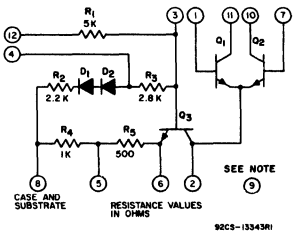
Fig.8

RF Amplifiers

- Designed for use in Communications Equipment
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide Unexcelled Versatility
- Built-in Temperature Stability for Operation from -55° C to +125° C
- Companion Application Note, ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC limiter, detector, and amplifier design considerations.
- 12-Lead Hermetic TO-5 Style Package.

- Push-Pull Input and Output
- Wide and Narrow Band Amplifier
- AGC
- Detector
- RF, IF, and Video Frequency Capability
- Operation from DC to 100 MHz
- Mixer
- Limiter
- Modulator
- Cascode Amplifier

SCHEMATIC DIAGRAM FOR CA3005 AND CA3006



NOTE: Connect Terminal No.9 to most positive dc supply voltage used for circuit.

Fig.1

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated voltage conditions for other terminals.
All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3.5	+3.5	7	0
			8	-6
			9	+6
			10	+6
			11	+6
			12	0
2	TEST POINT: DO NOT APPLY VOLTAGE FROM EXTERNAL SOURCE			
3	-9.5	0	1	0
			7	0
			8	-9.5
			9	+6
			10	+6
			11	+6
			12	0
4	-6	0	1	0
			7	0
			8	-6
			9	+6
			10	+6
			11	+6
			12	0
5	-12	0	1	0
			7	0
			9	+6
			10	+6
			11	+6
			12	0
6	-6	0	1	0
			7	0
			9	+6
			10	+6
			11	+6
			12	-6
7	-3.5	+3.5	1	0
			8	-6
			9	+6
			10	+6
			11	+6
			12	0

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	-12	0	1	0
			7	0
			9	+6
			10	+6
			11	+6
			12	0
9	0	+12	1	0
			7	0
			8	-6
			10	+6
			11	+6
			12	0
10	0	+12	1	0
			7	0
			8	-6
			9	+6
			11	+6
			12	0
11	0	+12	1	0
			7	0
			8	-6
			9	+6
			10	+6
			12	0
12	-9.5	0	8	-9.5
			9	+6
			10	+6
			11	+6
CASE	Internally connected to Terminal No.8 (substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±3.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . -2.5 V, +3.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

INPUT OFFSET VOLTAGE AND CURRENT

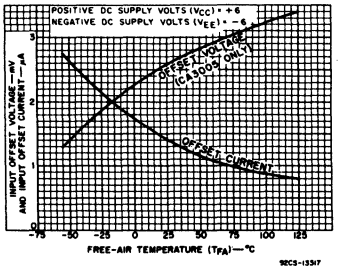


Fig.2

INPUT OFFSET VOLTAGE TEST CIRCUIT

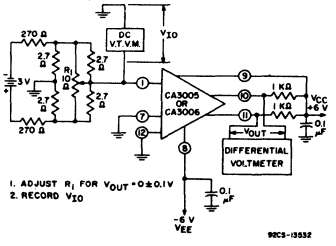


Fig.3

INPUT BIAS CURRENT

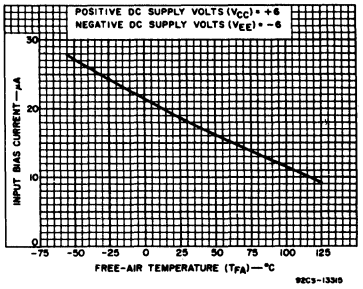


Fig.4

COMMON-MODE-REJECTION RATIO

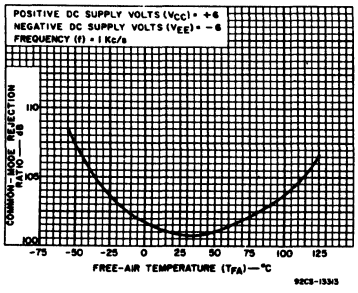


Fig. 13

COMMON–MODE-REJECTION RATIO TEST CIRCUIT

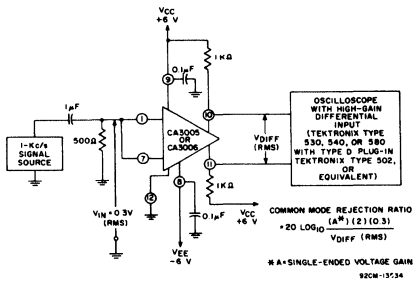


Fig. 14

AGC RANGE TEST CIRCUIT

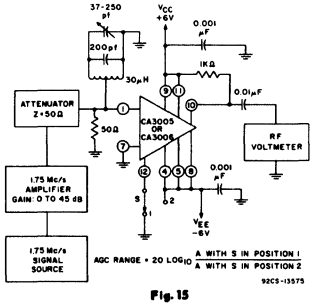


Fig. 15

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_A = 25° C

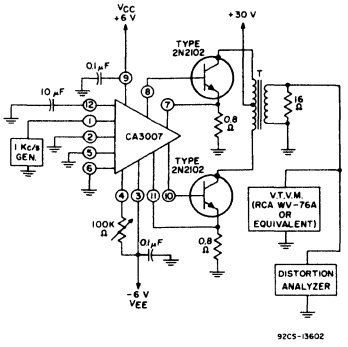
Indicated voltage limits for each terminal can be applied under the specified operating conditions for other terminals. All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$, or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
2	-8	0	3	-8
			6	0
			7	0
			9	+6
			11	0
3	-10	0	6	0
			7	0
			9	+6
			11	0
4	-8.5	0	6	0
			7	0
			9	+6
			11	0
5	-2.5	+2.5	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
6	-3	0	2	0
			3	-6
			7	0
			9	+6
			11	0
7	-2.5	+2.5	1	0
			2	0
			3	-6
			5	0
			6	0
			9	+6

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
9	0	+10	2	0
			3	-6
			6	0
			7	0
			11	0
10	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
11	-2.5	+2.5	1	0
			2	0
			3	-6
			6	0
			7	0
			9	+6
12	-2	0	2	0
			3	-6
			6	0
			7	0
			9	+6
			11	0
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

TYPICAL DYNAMIC CHARACTERISTIC AND TEST CIRCUITS FOR CA3007

POWER GAIN AND TOTAL HARMONIC DISTORTION TEST CIRCUIT



T (Output Transformer):
Primary Impedance = 2000 Ω C.T.
Secondary Impedance = 16 Ω
Efficiency = 45% approx.
(STANCOR TYPE TA-10 OR EQUIVALENT)

Fig.6

INPUT IMPEDANCE TEST CIRCUIT

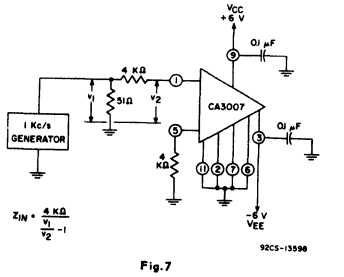


Fig.7

COMMON-MODE REJECTION RATIO vs TEMPERATURE

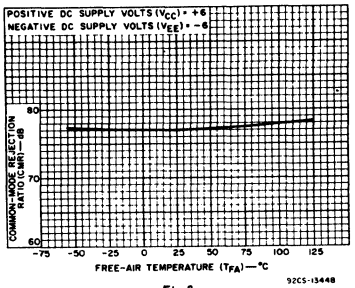
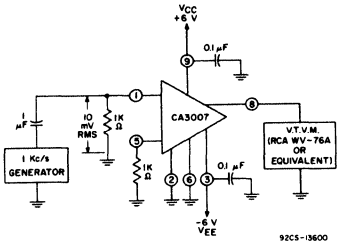
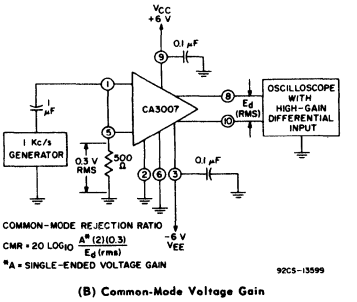


Fig.8

COMMON-MODE REJECTION-RATIO TEST CIRCUITS



(A) Single-Ended Differential Voltage Gain



(B) Common-Mode Voltage Gain

Fig.9

CA3008, CA3010, CA3015, CA3016, CA3029,CA3030, CA3037, CA3038

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 (CA3008, CA3016, CA3029, CA3030, CA3037, CA3038) Terminal No.5 (CA3010, CA3015) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3008 CA3010 CA3029 CA3037 Min.	Typ.	Max.	CA3016 CA3015 CA3030 CA3038 Min.	Typ.	Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	1.08 -	5 -	- -	- 1.37	- 5	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.54 -	5 -	- -	- 1.07	- 5	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	5.3 -	12 -	- -	- 9.6	- 24	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	30 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V 8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		- -	102 -	- -	- -	- 500	- -		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Common-Mode Rejection Ratio	CMRR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	10 -	14 -	- -	- 5	- 7.8	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	200 -	- -	- -	- 92	- -	Ω	15
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	0.5 to -4 -	- -	- -	- 0.65 to -8	- -	- -	V	none

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

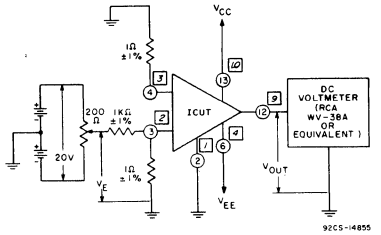


Fig.4

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the difference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\text{ (Step 2)} - V_{OUT}\text{ (Step 3)}}{\text{2 volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal (13) or [10]

I_E = Direct Current out of Terminal (6) or [4]

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

INPUT OFFSET VOLTAGE AND CURRENT

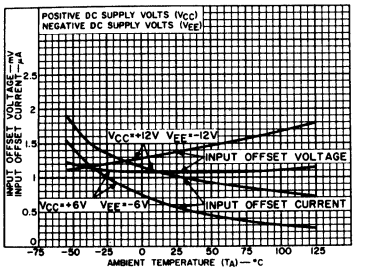


Fig.2

INPUT BIAS CURRENT

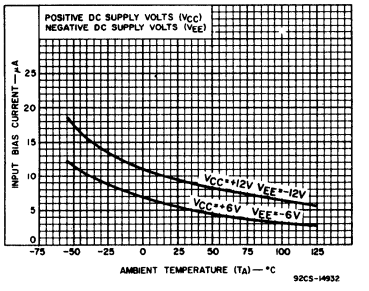


Fig.3

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

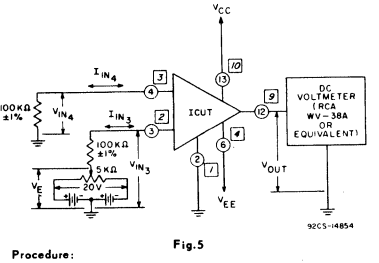


Fig.5

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}.
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008, CA3016, CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

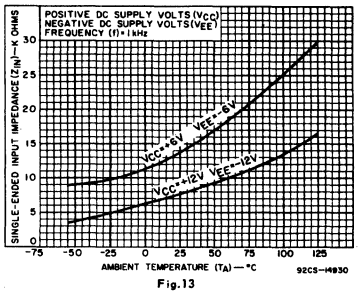


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

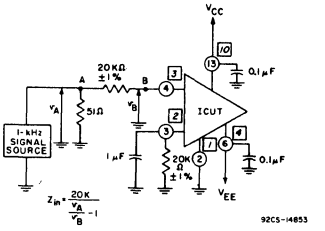


Fig.14

OUTPUT IMPEDANCE vs. TEMPERATURE

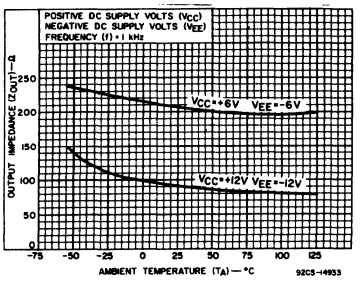


Fig.15

OUTPUT IMPEDANCE TEST CIRCUIT

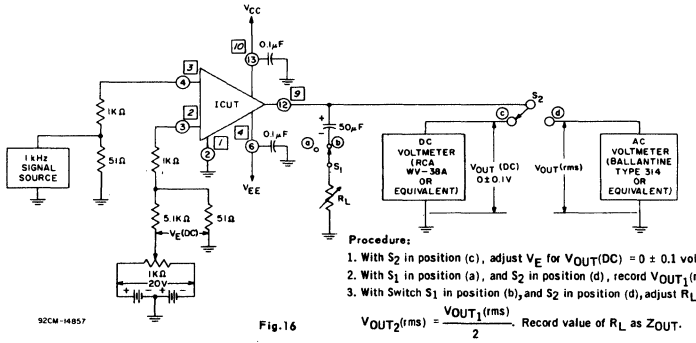


Fig.16

Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b), and S_2 in position (d), adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.

CA3008A, CA3010A, CA3015A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010A	CA3008A, CA3029A, CA3037A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010A	CA3008A, CA3029A, CA3037A	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
-	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 (CA3008A, CA3029A, CA3037A) 4 & 9 (CA3010A)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010A (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015A	CA3016A, CA3030A, CA3038A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015A	CA3016A, CA3030A, CA3038A	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
-	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 (CA3016A, CA3030A, CA3038A) 4 & 9 (CA3015A)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015A (Substrate) DO NOT GROUND				

	CA3008A, CA3016A, CA3037A, CA3038A	CA3010A, CA3015A, CA3029A, CA3030A
OPERATING TEMPERATURE RANGE	-55°C to +125°C	-40°C to +85°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-65°C to +150°C

	CA3016A, CA3030A, CA3038A	CA3015A, CA3008A, CA3029A, CA3037A, CA3010A
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3008A, CA3016A, CA3029A, CA3030A, CA3037A, CA3038A;
Italic Numbers in Square Boxes are for CA3010A, CA3015A

INPUT OFFSET VOLTAGE AND CURRENT

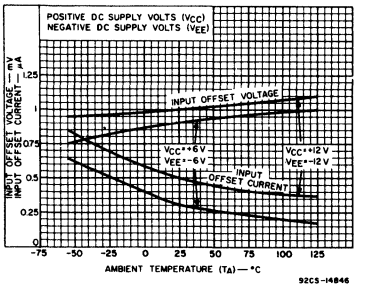


Fig.2

INPUT BIAS CURRENT

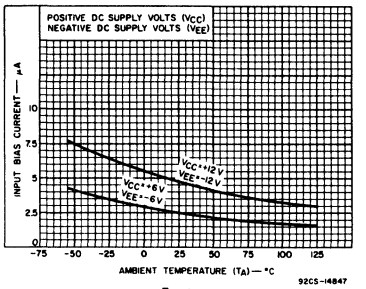


Fig.3

INPUT OFFSET VOLTAGE, INPUT OFFSET VOLTAGE SENSITIVITY, AND DEVICE DISSIPATION TEST CIRCUIT

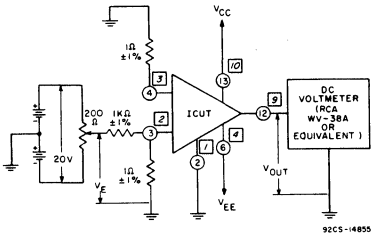


Fig.4

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal 13 or *10*

I_E = Direct Current out of Terminal 6 or *4*

INPUT OFFSET CURRENT AND INPUT BIAS CURRENT TEST CIRCUIT

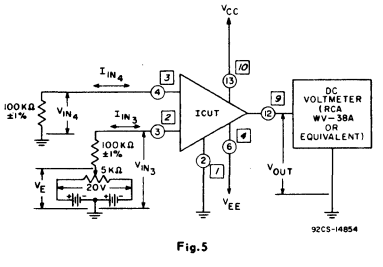


Fig.5

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

COMMON-MODE REJECTION RATIO vs. FREQUENCY

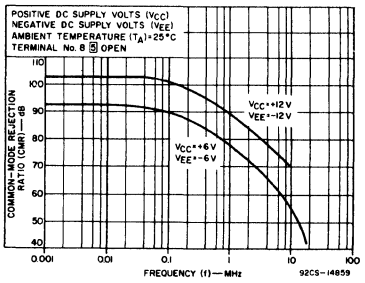


Fig.12

SINGLE-ENDED INPUT IMPEDANCE vs. TEMPERATURE

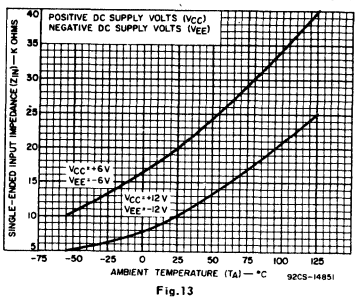


Fig.13

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

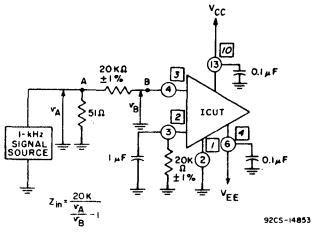


Fig.14

OUTPUT IMPEDANCE TEST CIRCUIT

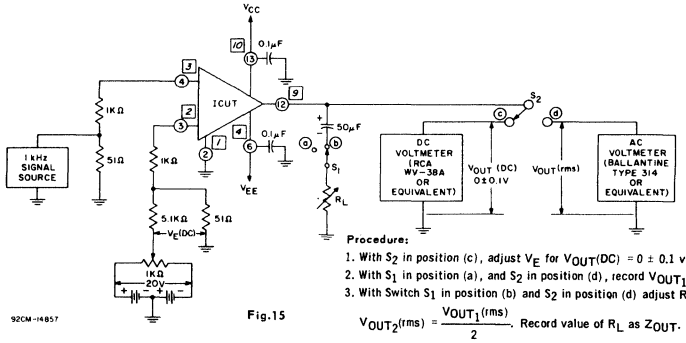
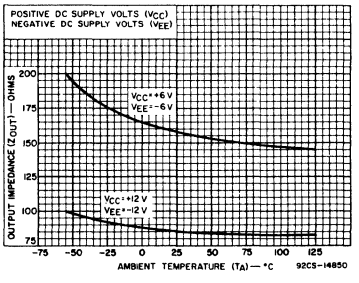


Fig.15

Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b) and S_2 in position (d) adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.



OUTPUT IMPEDANCE vs. TEMPERATURE

Fig.16

NOISE FIGURE vs. FREQUENCY

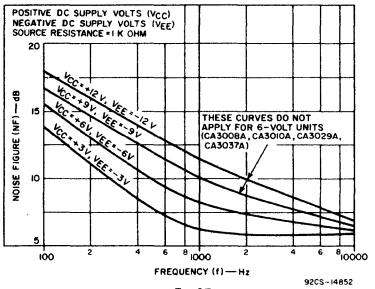


Fig.17

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES
		SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERATURE T_A	RCA CA3011			RCA CA3012				
		Fig.	Mc/s	Volts	°C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation *	P_T	6	-	6	-55	-	80	-	66	80	135	mW	
					+25	60	90	133	66	90	121	mW	
					+125	-	70	-	65	70	121	mW	
			-	7.5	-55	-	130	-	97	130	190	mW	
					+25	95	120	187	97	120	167	mW	
					+125	-	100	-	95	100	167	mW	
			-	10	-55	-	-	-	150	210	275	mW	
					+25	-	-	-	150	190	255	mW	
					+125	-	-	-	150	160	255	mW	
Voltage Gain**	A	9	1	6	-55	-	55	-	50	55	-	dB	
					+25	60	66	-	60	66	-	dB	
					+125	-	61	-	50	61	-	dB	
		9	1	7.5	-55	-	59	-	55	59	-	dB	
					+25	65	70	-	65	70	-	dB	
					+125	-	65	-	55	65	-	dB	
		9	1	10	-55	-	-	-	55	61	-	dB	
					+25	-	-	-	65	71	-	dB	
					+125	-	-	-	55	66	-	dB	
		9	4.5	7.5	+25	60	67	-	60	67	-	dB	5
			10.7	7.5	+25	55	61	-	55	61	-	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	7	4.5	7.5	+25	-	3	-	-	3	-	kΩ	2
Parallel Input Capacitance	C_{IN}	7	4.5	7.5	+25	-	7	-	-	7	-	pF	2
Output Impedance Components: Parallel Output Resistance	R_{OUT}	8	4.5	7.5	+25	-	31.5	-	-	31.5	-	kΩ	3
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	+25	-	4.2	-	-	4.2	-	pF	3
Noise Figure	NF	10	4.5	7.5	+25	-	8.7	-	-	8.7	-	dB	
Input Limiting Voltage (Knee)	$v_{i(lim)}$	9	4.5	7.5	+25	-	300	450	-	300	400	μV	

* The total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

DISSIPATION TEST SETUP

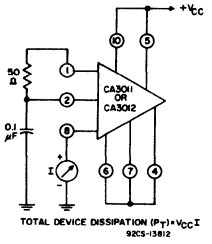


Fig. 6

INPUT-IMPEDANCE COMPONENTS TEST SETUP

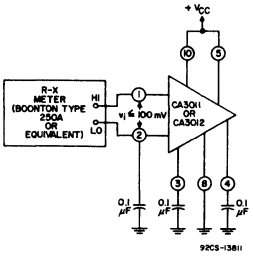


Fig. 7

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

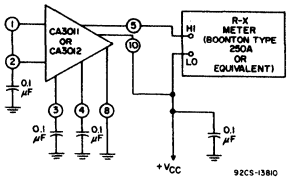
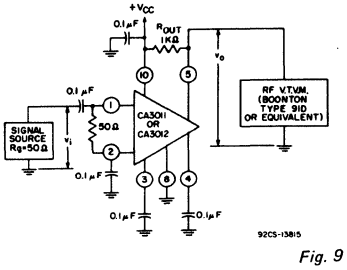


Fig. 8

VOLTAGE-GAIN TEST SETUP



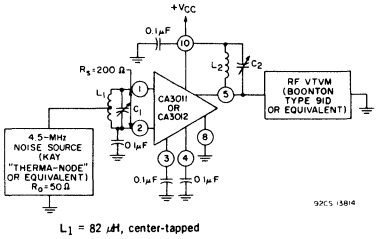
PROCEDURES

A - Voltage Gain:
1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

B - Input Limiting Voltage (Knee):
1) Repeat Steps A1 and A2, using v_i = 100 mV
2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.
3) Record v_i as Input Limiting Voltage (Knee).

Fig. 9

NOISE FIGURE TEST SETUP



L_1 = 82 μH, center-tapped
L_2 = 2.36 μH
C_1, C_2 = Arco Type 423 padder, or equivalent

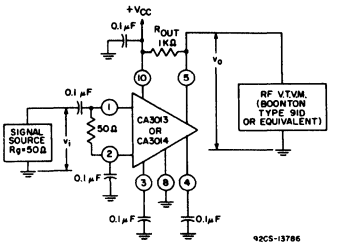
Fig. 10

ELECTRICAL CHARACTERISTICS (See Page 8 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES
		SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERATURE T_A	RCA CA3013			RCA CA3014				
		Fig.	Mc/s	volts	°C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation*	P_T	3	–	6	-55	–	80	–	73	80	120	mW	
					+25	60	90	133	73	90	110	mW	
					+125	–	70	–	60	70	110	mW	
		3	–	7.5	-55	–	130	–	106	130	170	mW	
					+25	87	120	187	106	120	150	mW	
					+125	–	100	–	90	100	150	mW	
		3	–	10	-55	–	–	–	165	210	250	mW	
					+25	–	–	–	165	190	230	mW	
					+125	–	–	–	150	160	230	mW	
Voltage Gain**	A	4	1	6	-55	–	55	–	50	55	–	dB	
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
		4	1	7.5	-55	–	59	–	55	59	–	dB	
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
		4	1	10	-55	–	–	–	55	61	–	dB	
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
		4	4.5	7.5	+25	60	67	–	60	67	–	dB	5
			10.7	7.5	+25	55	60	–	55	60	–	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	6	4.5	7.5	+25	–	3	–	–	3	–	kΩ	7
Parallel Input Capacitance	C_{IN}	6	4.5	7.5	+25	–	7	–	–	7	–	pF	7
Output-Impedance Components: Parallel Output Resistance	R_{OUT}	8	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	9
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	9
Noise Figure	NF	10	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	11
Input Limiting Voltage (Knee)	v_i(lim)	14	4.5	7.5	+25	–	300	450	–	300	400	μV	13
Recovered AF Voltage	v_o(af)	14	4.5	6	+25	–	155	–	–	155	–	mV	13
				7.5	+25	128	188	–	135	188	–	mV	
				10	+25	–	–	–	–	220	–	mV	
Amplitude-Modulation Rejection	AMR	15	4.5	7.5	+25	–	50	–	–	50	–	dB	–
Discriminator Output Resistance	R_O(disc)	–	4.5	7.5	+25	–	60	–	–	60	–	Ω	–
Total Harmonic Distortion	THD	14	4.5	7.5	+25	–	1.8	–	–	1.8	–	%	12

* Total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

VOLTAGE-GAIN TEST SETUP



PROCEDURE:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$.
4) Repeat Steps 1, 2, and 3 for each frequency and/or temperature desired.

Fig. 4

VOLTAGE GAIN vs. FREQUENCY

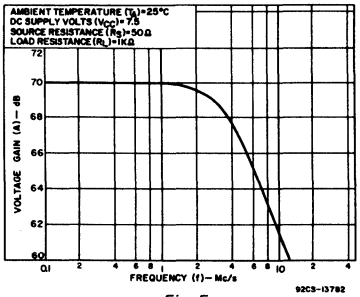


Fig. 5

INPUT-IMPEDANCE COMPONENTS TEST SETUP

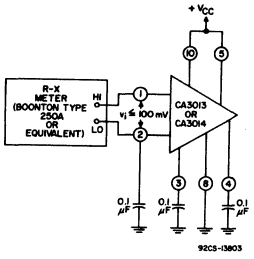


Fig. 6

INPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

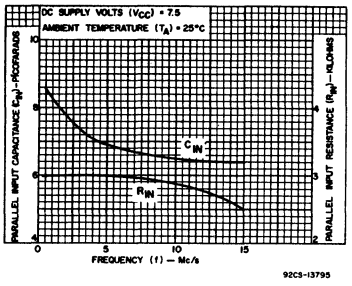


Fig. 7

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

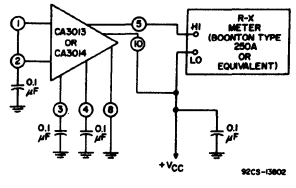


Fig. 8

OUTPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

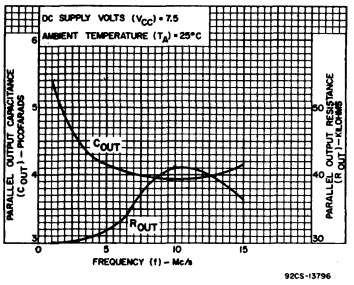


Fig. 9

General-Purpose Transistor Arrays

TWO ISOLATED TRANSISTORS AND A DARLINGTON-CONNECTED TRANSISTOR PAIR

For Low-Power Applications at Frequencies from DC Through the VHF Range

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

APPLICATIONS

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array" for suggested Applications.

FEATURES

- Matched monolithic general purpose transistors
- H_{FE} matched ± 10%
- V_{BE} matched ± 2 mV CA3018A (± 5mV CA3018)
- Operation from DC to 120 MHz
- Wide operating current range
- CA3018A performance characteristics controlled from 10μ A to 10mA
- Low noise figure - - 3.2 dB typical at 1KHz
- Full military temperature range capability (-55 to + 125°C)
- The CA3018 is available in a sealed-junction Beam Lead version (CA3018L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".
- Supplied in the hermetic 12-lead TO-5 style package.

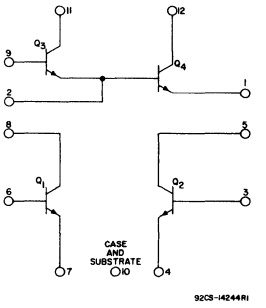


Fig. 1 - Schematic Diagram for CA3018 and CA3018A

Maximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	450	450	mW
Derate at 5 mW/°C for $T_A > 85°C$			
Temperature Range:			
Operating	-55 to + 125	-55 to + 125	°C
Storage	-65 to + 150	-65 to + 150	°C
LEAD TEMPERATURE (During Soldering)			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO}	15	15	V
Collector-to-Base Voltage, V_{CBO}	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO}	5	5	V
Collector Current, I_C	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

STATIC CHARACTERISTICS

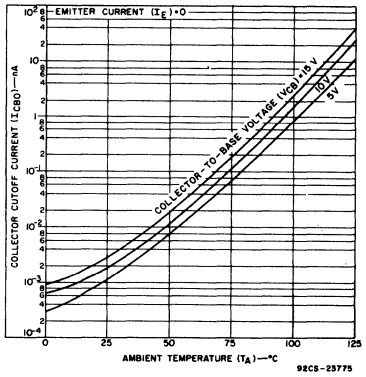


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

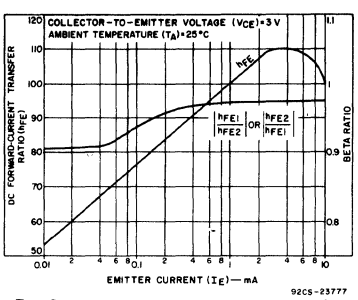


Fig. 3 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q, and Q_2 vs Emitter Current.

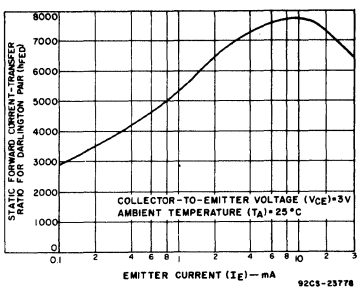


Fig. 4 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transisters Q_3 and Q_4 vs Emitter Current.

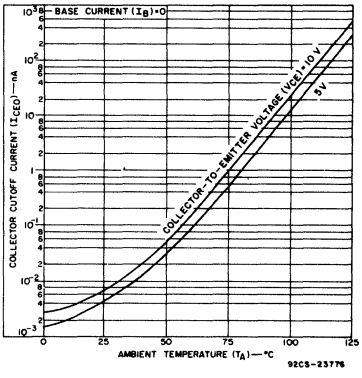


Fig. 7 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

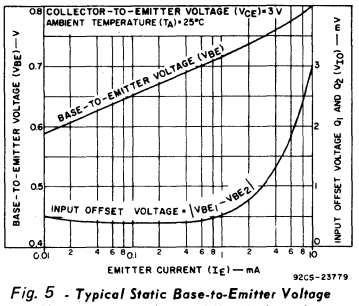


Fig. 5 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q_1 and Q_2 vs Emitter Current.

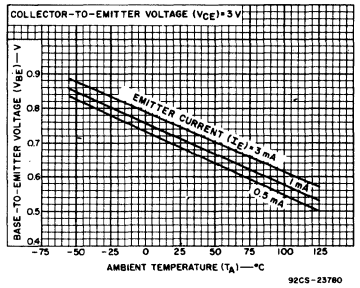


Fig. 6 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS			CA3018			CA3018A				
Low Frequency Noise Figure	NF	f=1 KHz, V_{CE}=3V, I_C=100μA Source resistance=1 KΩ	–	3.25	–	–	3.25	–	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	–	110	–	–	110	–	–	12
Short-Circuit Input Impedance	h_{ie}		–	3.5	–	–	3.5	–	KΩ	12
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	1.8×10^{-4}	–	–	1.8×10^{-4}	–	–	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	–	31-j1.5	–	–	31-j1.5	–	mmho	13
Input Admittance	Y_{ie}		–	0.3+j0.04	–	–	0.3+j0.04	–	mmho	14
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA	300	500	–	300	500	–	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	–	0.6	–	–	0.6	–	pF	–
Collector-to-Base Capacitance	C_{CB}	V_{CB}=3V, I_C=0	–	0.58	–	–	0.58	–	pF	–
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	–	2.8	–	–	2.8	–	pF	–

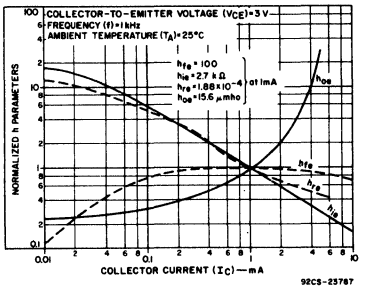


Fig.12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

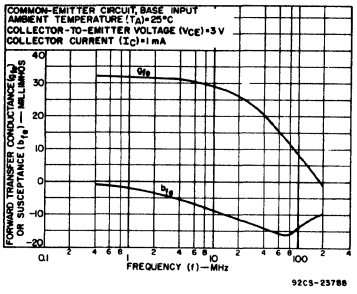


Fig.13 - Forward Transfer Admittance (Y_{fe})

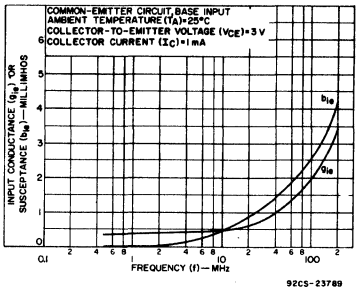


Fig.14 - Input Admittance (Y_{ie})

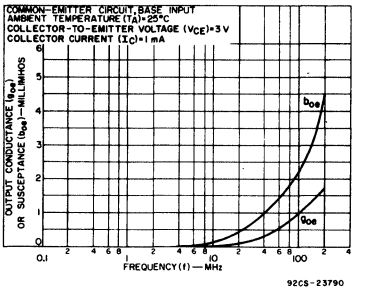


Fig.15 - Output Admittance (Y_{oe})

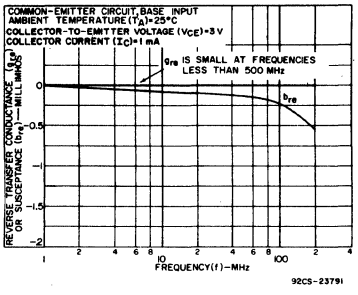


Fig.16 - Reverse Transfer Admittance (Y_{re})

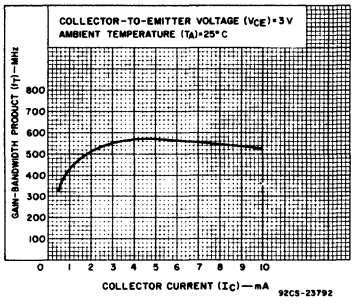


Fig.17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

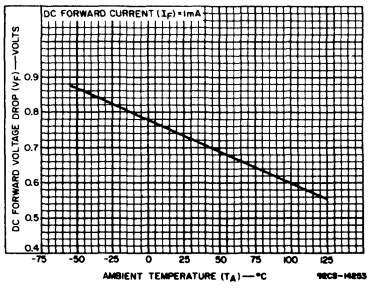


Fig. 2 – DC forward voltage drop (any diode) as a function of temperature.

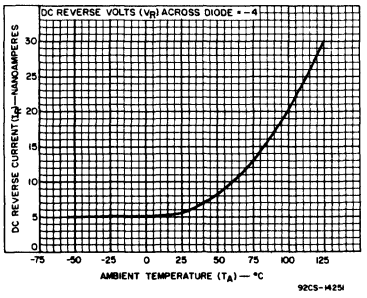


Fig. 3 – Reverse (leakage) current (any diode) as a function of temperature.

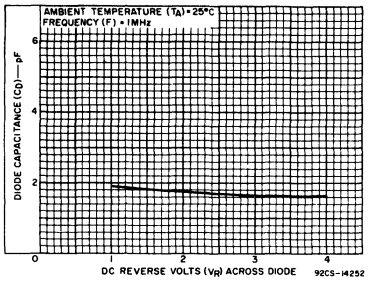


Fig. 4 – Diode capacitance (any diode) as a function of reverse voltage.

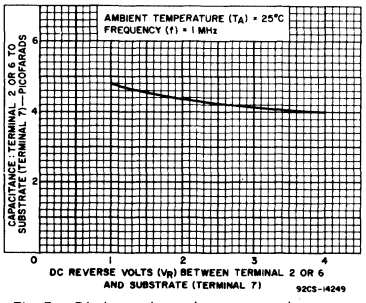


Fig. 5 – Diode quad-to-substrate capacitance as a function of reverse voltage.

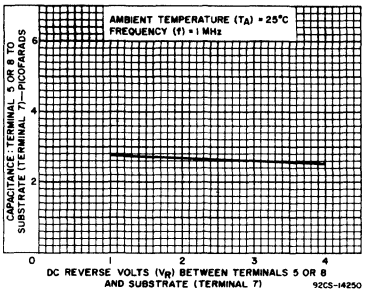


Fig. 6 – Diode quad-to-substrate capacitance as a function of reverse voltage.

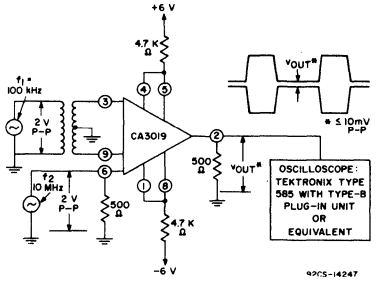


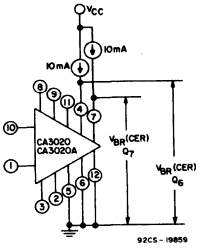
Fig. 7 – Series gate switching test setup.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

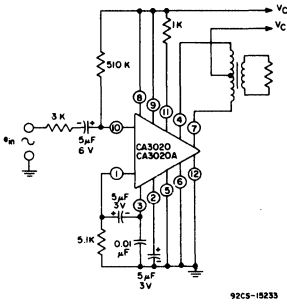
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS CA3020			LIMITS CA3020A			UNITS
		CIRCUIT AND PROCEDURE	DC SUPPLY VOLTAGE								
		FIG.	V_{CC1}	V_{CC2}	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CER}$	2a	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 & Q_7	I_4 IDLE I_7 IDLE	4	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	4	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 & Q_7	I_4 CUTOFF I_7 CUTOFF	4	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differetial Amplifier Current Drain	I_{CC1}	4	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	4	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	4	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	4	9.0	2.0	-	2.35	-	-	2.35	-	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA
Emitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	
Collector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3 dB Point	BW		6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output	$P_{O(MAX)}$	6	6.0	6.0	200	300[a]	-	200	300[a]	-	mW
			9.0	9.0	400	550[a]	-	400	550[a]	-	
			9.0	12.0	-	-	-	800	1000[b]	-	
Sensitivity for P_{OUT} = 400 mW	e_{IN}	6	9.0	9.0	-	35[a]	55	-	-	-	mV
Sensitivity for P_{OUT} = 800 mW	e_{IN}	6	9.0	12.0	-	-	-	-	50[b]	100	mV
Input Resistance---- Terminal 3 to Ground	R_{IN3}	9	6.0	6.0	-	1000	-	-	1000	-	Ω
Junction-to-Case Thermal Resistance	θ_{J-C}	-	-	-	-	-	60	-	-	60	°C/W

a R_{CC} = 130 Ω

b R_{CC} = 200 Ω



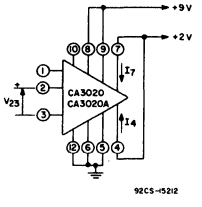
a. Collector-to-emitter breakdown voltage (Q_6 & Q_7) circuit



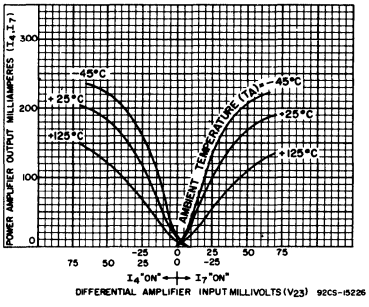
b. Typical audio amplifier circuit utilizing the CA3020 or CA3020A as an audio preamplifier and class B power amplifier

Fig.2

TYPICAL TRANSFER CHARACTERISTICS



a. Test Setup



b. Characteristics with R_{10} shorted out

Fig.3

TYPICAL PERFORMANCE DATA

An External Radiator is Recommended for High Ambient Temperature Operation

CHARACTERISTICS	SYMBOLS	CA3020	CA3020A	UNITS
Power Supply Voltage	V_{CC_1}	9.0	9.0	V
	V_{CC_2}	9.0	12.0	
Zero Signal Current Diff. Ampl.	I_{CC_1}	15	15	mA
Zero Signal Current Output Ampl.	I_{CC_2}	24	24	
Maximum Signal Current Diff. Ampl.	I_{CC_1}	16	16.6	mA
Maximum Signal Current Output Ampl.	I_{CC_2}	125	140	
Maximum Power Output at THD = 10%	Po	550	1000	mW
Sensitivity	e_{IN}	35	45	mV
Power Gain	G_P	75	75	dB
Input Resistance	R_{IN}	55	55	kΩ
Efficiency	η	45	55	%
Signal-to-Noise Ratio	S/N	70	66	dB
THD at 150 mW level		3.1	3.3	%
Test Signal Frequency from 600Ω Generator		1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance	R_{CC}	130	200	Ω

MEASUREMENT OF INPUT RESISTANCE

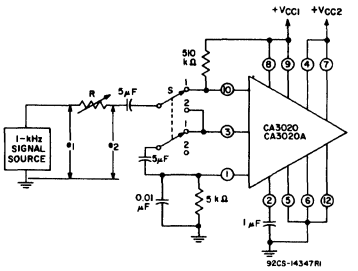


Fig.9

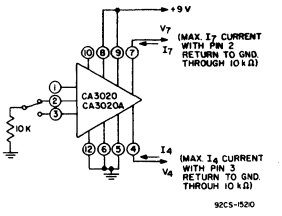
PROCEDURES:

Input Resistance Terminal 10 to Ground ($R_{IN_{10}}$)

1. Apply desired value of V_{CC_1} and V_{CC_2} and set S in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as $R_{IN_{10}}$

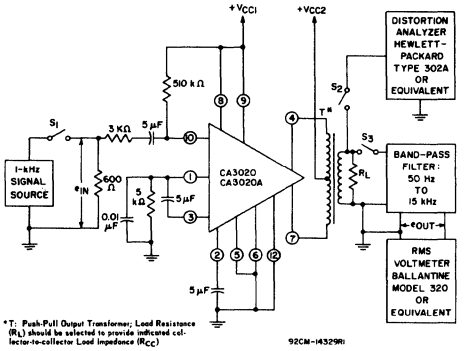
Input Resistance Terminal 3 to Ground (R_{IN_3})

1. Apply desired value of V_{CC_1} and V_{CC_2} set S in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN_3}



a. Test Setup

MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION



*T: Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load Impedance (R_{CC})

PROCEDURES:

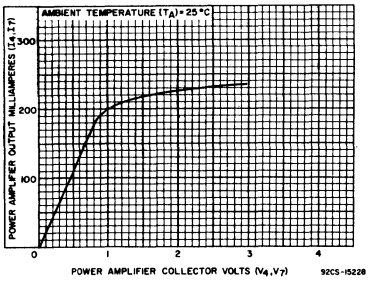
Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as e_{OUT_1} (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT_2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10} \frac{e_{OUT_1}}{e_{OUT_2}}$.

Total Harmonic Distortion

1. Close S_1 and S_2; open S_3
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

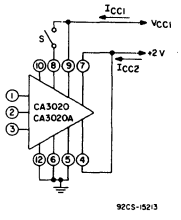
Fig.10



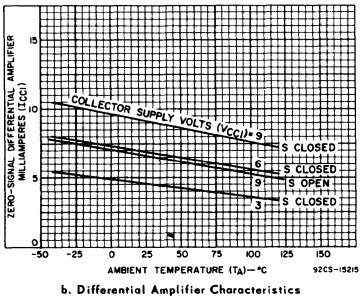
b. Characteristic

Fig.11

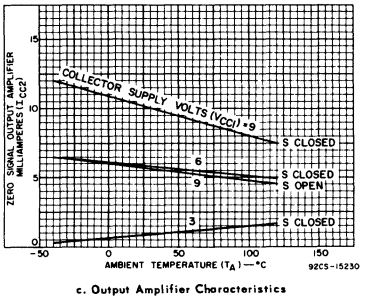
ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE



a. Test Setup



b. Differential Amplifier Characteristics



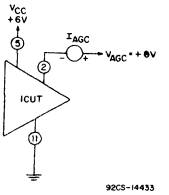
c. Output Amplifier Characteristics

Fig.12

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, V_{CC} = +6V, unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS									UNITS	TYPICAL CHARACTERISTIC CURVE
		TEST SETUP AND PROCEDURE	FEEDBACK RESISTANCE (R_β) BETWEEN TERMINALS 3 AND 7	FREQUENCY f	CA3021 (TA5219)			CA3022 (TA5236)			CA3023 (TA5218)				
		Fig.	Ω	MHz	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Fig.
Device Dissipation	P_T	2	∞	-	1	4	8	–	–	–	–	–	–	mW	3a,d
			∞	–	–	–	–	5	12.5	24	–	–	–	mW	3b,d
			∞	–	–	–	–	–	–	–	24	35	48	mW	3c,d
Quiescent Output Voltage	V_O	2	39k	–	–	2.2	–	–	–	–	–	–	–	V	–
			10k	–	–	–	–	–	1.9	–	–	–	–	V	
			4.7k	–	–	–	–	–	–	–	–	1.3	–	V	
AGC Source Current	I_{AGC}	4	V_{AGC} =+6V		–	0.8	–	–	0.8	–	–	0.8	–	mA	–
Voltage Gain	A	5	560k	0.5	50	56	–	–	–	–	–	–	–	dB	6a
			39k	0.8	40	46	–	–	–	–	–	–	–	dB	6a,d
			39k	2.5	–	–	–	50	57	–	–	–	–	dB	6b
			10k	3	–	–	–	40	44	–	–	–	–	dB	6b,d
			18k	5	–	–	–	–	–	–	50	53	–	dB	6c
			4.7k	10	–	–	–	–	–	–	40	44	–	dB	6c,d
Bandwidth at -3 dB Point	BW	5	39k	–	0.8	2.4	–	–	–	–	–	–	–	MHz	6a
			10k	–	–	–	–	3	7.5	–	–	–	–	MHz	6b
			4.7k	–	–	–	–	–	–	–	10	16	–	MHz	6c
Input-Impedance Components: Input Resistance	R_{IN}	7	39k	1	–	4000	–	–	–	–	–	–	–	Ω	–
			10k	5	–	–	–	–	1300	–	–	–	–	Ω	
			4.7k	10	–	–	–	–	–	–	–	300	–	Ω	
Input Capacitance	C_{IN}	7	39k	1	–	11	–	–	–	–	–	–	–	pF	–
			10k	5	–	–	–	–	18	–	–	–	–	pF	
			4.7k	10	–	–	–	–	–	–	–	13	–	pF	
Output Resistance	R_{OUT}	8	39k	1	–	300	–	–	–	–	–	–	–	Ω	–
			10k	5	–	–	–	–	120	–	–	–	–	Ω	
			4.7k	10	–	–	–	–	–	–	–	100	–	Ω	
Noise Figure	NF	9	39k	1	–	4.2	8.5	–	–	–	–	–	–	dB	–
			10k	1	–	–	–	–	4.4	8.5	–	–	–	dB	
			4.7k	1	–	–	–	–	–	–	–	6.5	8.5	dB	
AGC Range	AGC	10	–	1	–	33	–	–	–	–	–	–	–	dB	–
			–	5	–	–	–	–	33	–	–	–	–	dB	
			–	10	–	–	–	–	–	–	–	33	–	dB	
Maximum Output Voltage (RMS Value)	V_{out}	5	39k	1	–	0.6	–	–	–	–	–	–	–	V(rms)	–
			10k	5	–	–	–	–	0.7	–	–	–	–	V(rms)	
			4.7k	10	–	–	–	–	–	–	–	0.5	–	V(rms)	

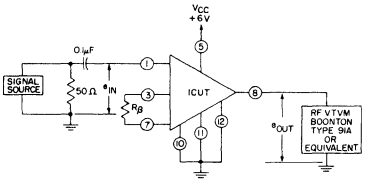
TEST SETUP FOR MEASUREMENT OF AGC SOURCE CURRENT



I_{AGC} IS THE CURRENT FLOWING INTO TERMINAL 2.

Fig. 4

TEST SETUP FOR MEASUREMENTS OF VOLTAGE-GAIN, -3dB BANDWIDTH, AND MAXIMUM OUTPUT VOLTAGE



PROCEDURES

Voltage Gain:

(a) Set e_{in} = 0.5 mV at frequency specified, read e_{out} Voltage Gain

(A) = 20 $\log_{10} \frac{e_{out}}{e_{in}}$

Bandwidth:

(a) Set e_{out} to a convenient reference voltage at f = 100 kHz and record corresponding value of e_{in}.

(b) Increase the frequency, keeping e_{in} constant until e_{out} drops 3-dB. Record Bandwidth.

Fig. 5

VOLTAGE GAIN VS FREQUENCY FOR CA3021

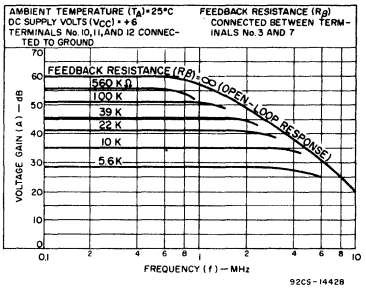


Fig. 6(a)

VOLTAGE GAIN VS FREQUENCY FOR CA3022

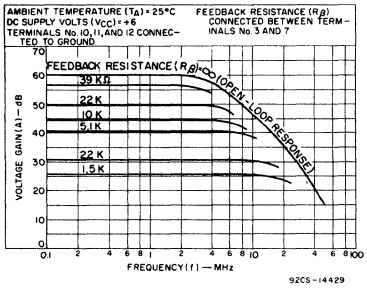


Fig. 6(b)

VOLTAGE GAIN VS FREQUENCY FOR CA3023

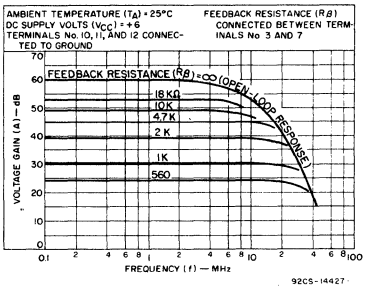


Fig. 6(c)

VOLTAGE GAIN VS TEMPERATURE FOR CA3021, CA3022, AND CA3023

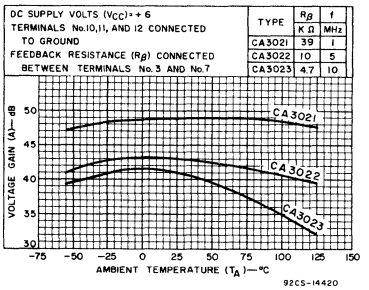


Fig. 6(d)

Dual Independent Differential Amplifiers

For Low-Power Applications at Frequencies from DC to 120 MHz

The CA3026 and CA3054 each consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3026 and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

APPLICATIONS

- Dual sense amplifiers
- Dual Schmitt triggers
- Multifunction combinations -- RF Mixer, Oscillator; Converter, IF
- IF amplifiers (differential and or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascode limiters
- Synchronous detectors
- Pairs of balanced mixers
- Synthesizer mixers
- Balanced (push-pull) cascode amplifiers

FEATURES

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage -- ±5 mV
- Full military temperature range capability -- -55°C to +125°C
- Limited temperature range -- 0°C to 85°C for CA3054

- **The CA3054 is available in a sealed-junction Beam-Lead version (CA3054L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**
- **CA3026—Hermetic 12-lead TO-5 package**
- **CA3054—14-lead dual-in-line plastic package**

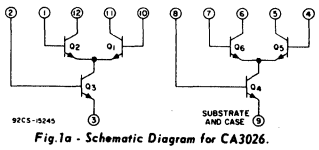


Fig.1a - Schematic Diagram for CA3026.

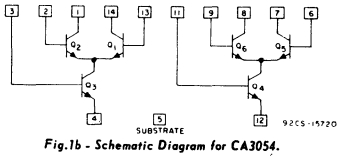


Fig.1b - Schematic Diagram for CA3054.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3026	CA3054	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	600	750	mW
For T_A > 55°C	Derate at 5	6.67	mW/°C
Temperature Range:			
Operating	-55 to + 125		°C
Storage	-65 to + 150		°C
Lead Temperature (During Soldering):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1† and horizontal terminal 3† is +15 to -5 volts.

† For CA3026; corresponding terminals for CA3054 are vertical terminal 2 and horizontal terminal 4.

CA3054 TERMINAL No. → / CA3026 TERMINAL No. ↓	13 / 10	14 / 11	1 / 12	2 / 1	3 / 2	4 / 3	6 / 4	7 / 5	8 / 6	9 / 7	11 / 8	12 / Note 1 9	5 / Note 1 9
13	10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*
14	11			*	*	*	+20 0	*	*	*	*	*	+20 0
1	12				+20 0	*	+20 0	*	*	*	*	*	+20 0
2	1					*	+15 -5	*	*	*	*	*	*
3	2						+1 -5	*	*	*	*	*	*
4	3							*	*	*	*	*	*
6	4								0 -20	*	+5 -5	+15 -5	*
7	5									*	*	*	+20 0
8	6										+20 0	*	+20 0
9	7											*	+15 -5	*
11	8												+1 -5	*
12	9													*
5	9													Ref Substrate

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

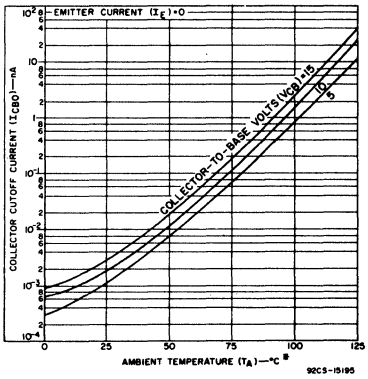
Note 1: In the CA3026 terminal No.9 is connected to the emitter of Q_6, the reference substrate, and the case; therefore, the case should not be grounded. Two terminal 9 columns (CA3026) appear in the voltage rating chart because it is a composite chart for both the CA3026 and the CA3054. Wherever an asterisk is shown in one column 9 and a rating is shown in the other column 9, the asterisk should be ignored.

Maximum Current Ratings

CA3054 TERMINAL No.●	CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
13	10	5	0.1
14	11	50	0.1
1	12	50	0.1
2	1	5	0.1
3	2	5	0.1
4	3	0.1	-50
6	4	5	0.1
7	5	50	0.1
8	6	50	0.1
9	7	5	0.1
11	8	5	0.1
12	9	0.1	50

● Terminal No.10 of CA3054 is not used

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

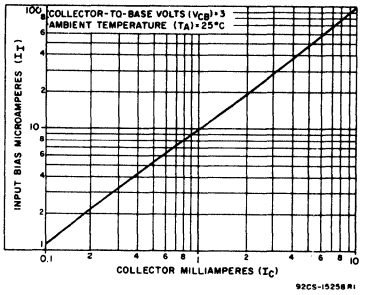
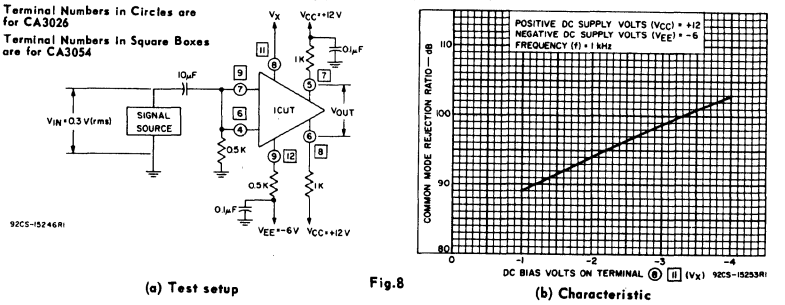


Fig.3 - Input bias current characteristic vs collector current for each transistor.

TYPICAL DYNAMIC CHARACTERISTICS

COMMON MODE REJECTION RATIO

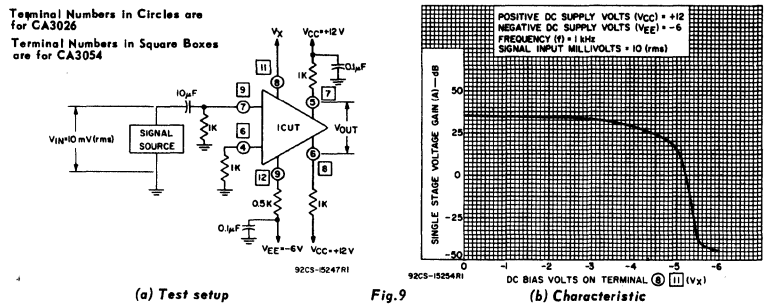


(a) Test setup

Fig.8

(b) Characteristic

SINGLE-STAGE VOLTAGE GAIN

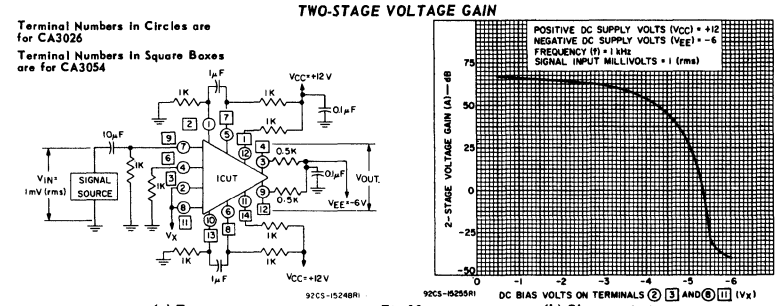


(a) Test setup

Fig.9

(b) Characteristic

TWO-STAGE VOLTAGE GAIN



(a) Test setup

Fig.10

(b) Characteristic

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

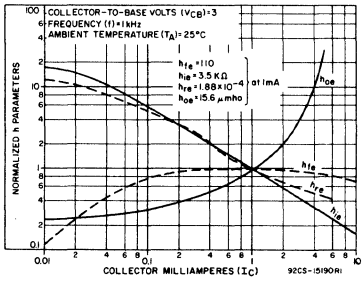


Fig.11 - Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

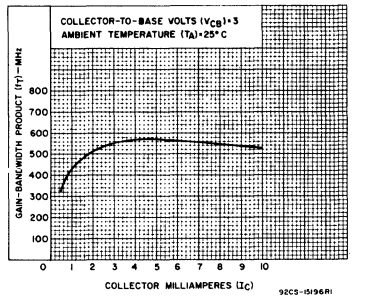


Fig.12 - Gain-bandwidth product (f_T) vs collector current.

DIFFERENTIAL/CASCODE AMPLIFIERS

For Communications and Industrial Equipment at Frequencies from DC to 120 MHz

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical dc and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

APPLICATIONS

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio, and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator • Mixer • Limiter
- Companion Application Note, ICAN 5337 "Application of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.

FEATURES

- Controlled for Input Offset Voltage, Input Offset Current, and Input Bias Current (CA3028B)
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide Unexcelled Versatility
- Single- and Dual-Ended Operation
- Operation from DC to 120 MHz
- Balanced-AGC Capability
- Wide Operating-Current Range

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:
- At T_A up to 55°C (CA3028AF, CA3028BF, CA3053F) ..... 750 mW
- At T_A > 55°C (CA3028AF, CA3028BF, CA3053F) ..... Derate linearly 6.67 mW/°C
- At T_A up to 85°C (CA3028A, CA3028B, CA3053) ..... 450 mW
- At T_A > 85°C (CA3028A, CA3028B, CA3053) Derate linearly 5 mW/°C

AMBIENT-TEMPERATURE RANGE:
- Operating ..... −55°C to +125°C
- Storage ..... −65°C to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

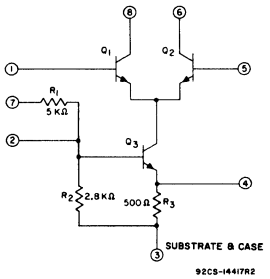


Fig.1 - Schematic diagram for CA3028A, CA3028B and CA3053.

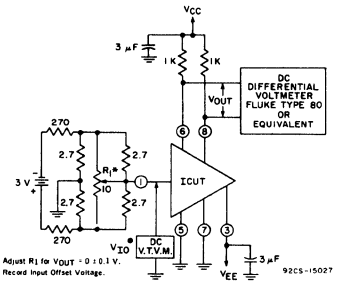


Fig.2 - Input offset voltage test circuit for CA3028B.

The CA3028A, CA3028B, and CA3053 are available in the packages shown below. When ordering these devices, it is important to add the appropriate suffix letter to the device.

Package 8-Lead TO-5	Suffix Letter	CA3028A	CA3028B	CA3053
TO-5	T	√	√	√
With Dual-In-Line Formed Leads (DIL-CAN)	S	√	√	√
Beam-Lead	L	√		
Chip	H	√		

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15▲	0 to -15▲	0 to -15▲	+5 to -5	*	*	+20⊕ to 0
2			+5 to -11	+5 to -1	+15♦ to 0	*	+15♦ to 0	*
3‡				+10 to 0	+15♦ to 0	+30● to 0	+15♦ to 0	+30● to 0
4					+15♦ to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

▲ Limit is -12V for CA3053

⊕ Limit is +15V for CA3053

♦ Limit is +12V for CA3053

● Limit is +24V for CA3028A and +18V for CA3053

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVES Fig.
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
STATIC CHARACTERISTICS															
			$+V_{CC}$	$-V_{EE}$											
Input Offset Voltage	V_{IO}	2	6V	6V	-	-	-	-	0.98	5	-	-	-	mV	4
			12V	12V	-	-	-	-	0.89	5	-	-	-		
Input Offset Current	I_{IO}	3a	6V	6V	-	-	-	-	0.56	6	-	-	-	μA	4
			12V	12V	-	-	-	-	1.06	6	-	-	-		
Input Bias Current	I_I	3a	6V	6V	-	16.6	70	-	16.6	40	-	-	-	μA	5a
			12V	12V	-	36	106	-	36	80	-	-	-		
		3b	9V	-	-	-	-	-	-	-	-	29	85		5b
			12V	-	-	-	-	-	-	-	-	36	125		
Quiescent Operating Current	I_6 or I_8	3a	6V	6V	0.8	1.25	2	1	1.25	1.5	-	-	-	mA	6a 7
			12V	12V	2	3.3	5	2.5	3.3	4	-	-	-		
		3b	9V	-	-	-	-	-	-	-	1.2	2.2	3.5		6b
			12V	-	-	-	-	-	-	-	2.0	3.3	5.0		
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I_7	8a	12V	V_{AGC} =+9	-	1.28	-	-	1.28	-	-	-	-	mA	8b
			12V	V_{AGC} = +12	-	1.65	-	-	1.65	-	-	-	-		
		-	9V	-	-	-	-	-	-	-	-	1.15	-		-
			12V	-	-	-	-	-	-	-	-	1.55	-		
Input Current (Terminal No.7)	I_7	-	6V	6V	0.5	0.85	1	0.5	0.85	1	-	-	-	mA	-
			12V	12V	1	1.65	2.1	1	1.65	2.1	-	-	-		
Device Dissipation	P_T	3a	6V	6V	24	36	54	24	36	42	-	-	-	mW	9
			12V	12V	120	175	260	120	175	220	-	-	-		
		3b	9V	-	-	-	-	-	-	-	-	50	80		-
			12V	-	-	-	-	-	-	-	-	100	150		

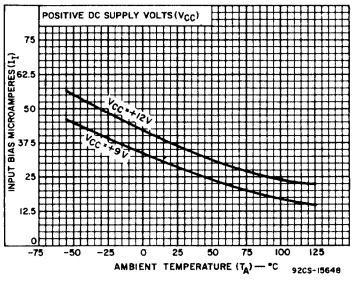


Fig.5b - Input bias current vs. ambient temperature for CA3053.

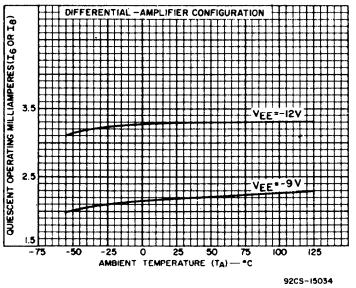


Fig.6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

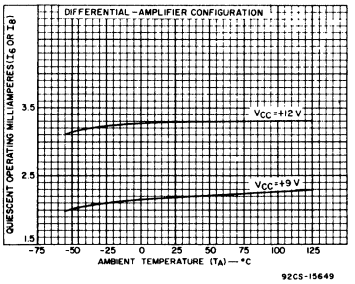


Fig.6b - Quiescent operating current vs. ambient temperature for CA3053.

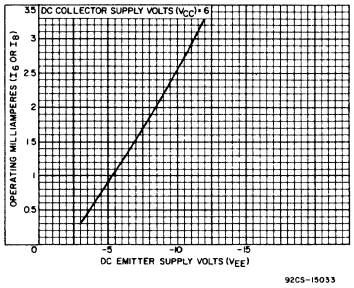


Fig.7 - Operating current vs. V_{EE} voltage for CA3028A and CA3028B.

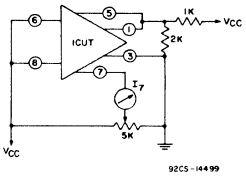


Fig.8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

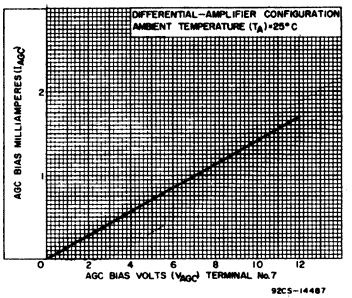


Fig.8b - AGC bias current vs. bias volts (terminal No.7) for CA3028A and CA3028B.

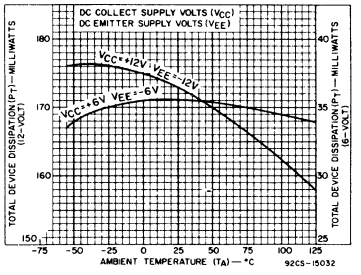
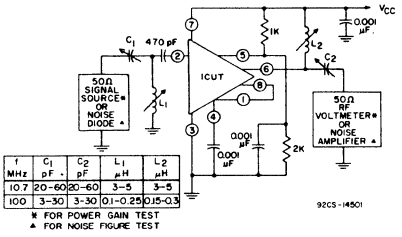


Fig.9 - Device dissipation vs. temperature for CA3028A and CA3028B.



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	20-60	20-60	3-5	3-5
100	3-30	3-30	0.1-0.25	0.15-0.3

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.

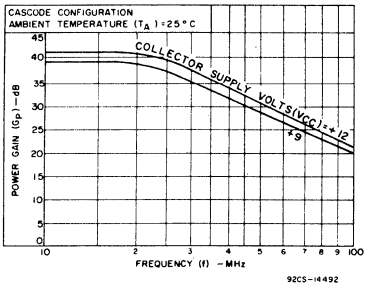


Fig.10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

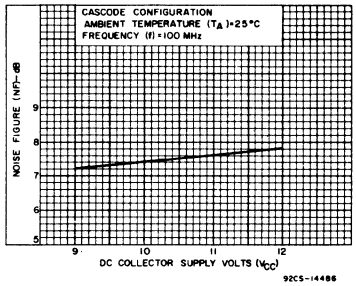
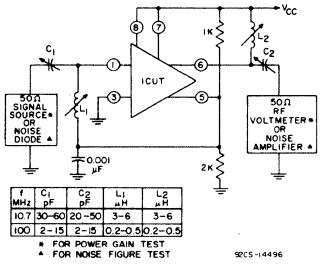


Fig.10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig.11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No.7 connected to V_{CC}) for CA3028A, CA3028B and CA3053.*

* 10.7 MHz Power Gain Test Only.

TYPICAL TEST CIRCUITS AND CHARACTERISTICS

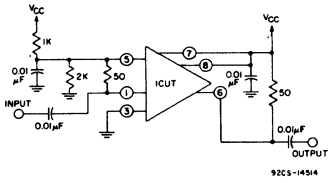


Fig.20a - Output power test circuit for CA3028A and CA3028B.

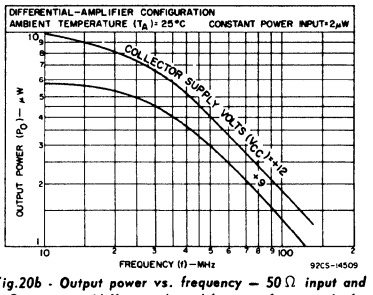


Fig.20b - Output power vs. frequency — 50 Ω input and 50 Ω output (differential-amplifier configuration) for CA3028A and CA3028B.

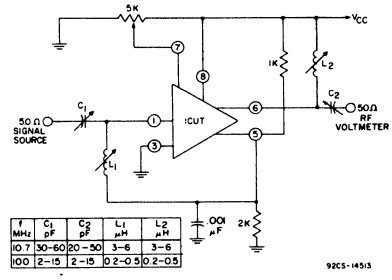


Fig.21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

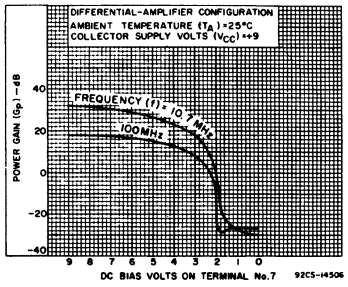


Fig.21b - AGC characteristics for CA3028A and CA3028B.

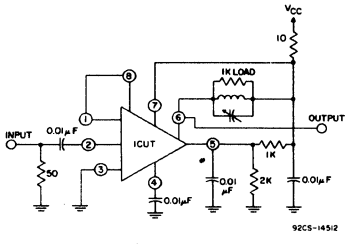


Fig.22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

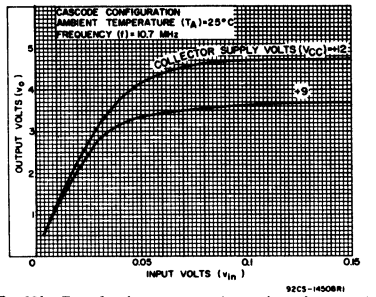


Fig.22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

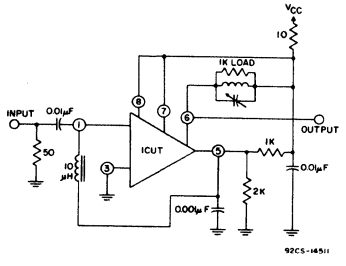


Fig.22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

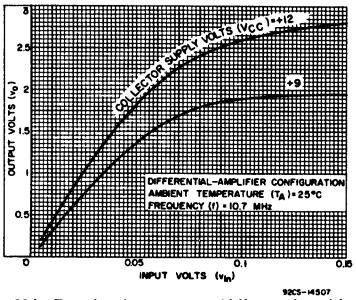
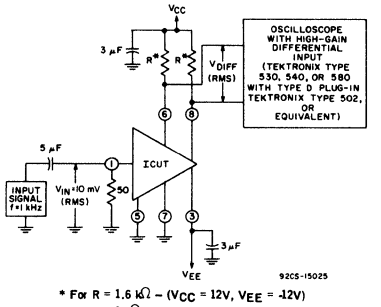
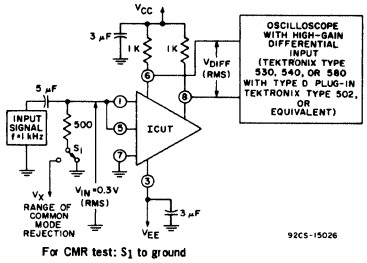


Fig.22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.



* For R = 1.6 kΩ — (V_{CC} = 12V, V_{EE} = -12V)
For R = 2 kΩ — (V_{CC} = 6 V, V_{EE} = -6V)

Fig.23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.



For CMR test: S_1 to ground

For input common-mode voltage range test: S_1 to V_X

Common mode rejection ratio = $20 \log_{10} \frac{(A^*)\,(2)\,(0.3)}{V_{DIFF}\,(RMS)}$

* A = Single-ended voltage gain.

Fig.24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.

Diode Array

Six Matched Diodes on a Common Substrate

ULTRA-FAST LOW-CAPACITANCE MATCHED DIODES

For Applications in Communications and Switching Systems

The RCA-CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

APPLICATIONS

- Balanced modulators or demodulators
- Ring modulators
- High speed diode gates
- Analog switches

FEATURES

- Excellent reverse recovery time – 1 ns typ.
- Matched monolithic construction – V_F matched within 5 mV
- Low diode capacitance – C_D = 0.65 pF typical at V_R = –2 V
- The CA3039 is available in a sealed-junction Beam-Lead version (CA3039L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

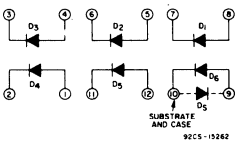


Fig. 1 - Schematic Diagram for CA3039

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:
- Any one diode unit . . . . . 100 mW
- Total for device . . . . . 600 mW
- For T_A > 55°C . . . . . derate linearly 5.7 mW/°C

TEMPERATURE RANGE:
- Operating . . . . . –55 to +125°C
- Storage . . . . . –65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . + 265°C

PEAK INVERSE VOLTAGE, PIV for: D_1–D_5 . . 5 V
D_6 . . . 0.5 V

PEAK DIODE-TO-SUBSTRATE VOLTAGE, V_{DI} for D_1–D_5 (term. 1,4,5,8 or 12 to term. 10) . . + 20, –1 V

DC FORWARD CURRENT, I_F . . . . . 25 mA

PEAK RECURRENT FORWARD CURRENT, I_f . 100 mA

PEAK FORWARD SURGE CURRENT, $I_{f(surge)}$. 100 mA

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CHARACTERISTIC CURVES FIG.
DC Forward Voltage Drop	V_F	I_F = 50 μA	–	0.65	0.69	V	2
		1 mA	–	0.73	0.78	V	
		3 mA	–	0.76	0.80	V	
		10 mA	–	0.81	0.90	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = –10 μA	5	7	–	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = –10 μA	20	–	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = –4 V	–	0.016	100	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = –10 V	–	0.022	100	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	0.5	5	mV	2
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	–	1	–	μV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	–1.9	–	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	–	0.65	–	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω	7
Diode Capacitance	C_D	V_R = –2 V, I_F = 0	–	0.65	–	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF	9

TYPICAL CHARACTERISTICS

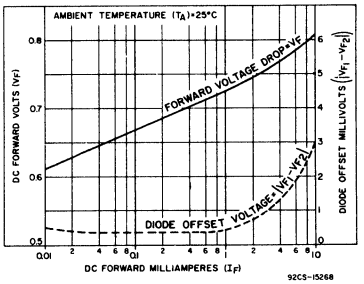


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

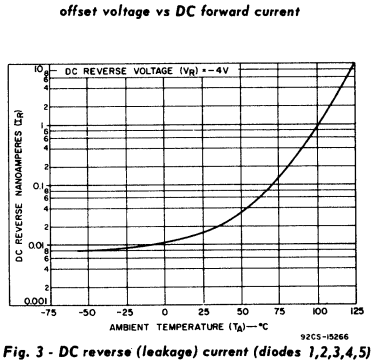


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

This device is supplied in the hermetic 12-lead TO-5 style package.

Video and Wideband Amplifier

For Industrial and Commercial Equipment at Frequencies up to 200 MHz

The RCA CA3040 is a monolithic silicon integrated circuit designed to meet the requirements of a wide variety of applications requiring high gain and wide bandwidth. The cascode-connected differential amplifier achieves a double-ended gain of 37 dB with a typical 3 dB bandwidth of 55 MHz. Emitter-Follower input and output stages provide the desirable high input impedance and low output impedance for coupling to other circuits.

The CA3040 includes two biasing options, allowing the user to optimize his design over the entire military temperature range of -55 to +125°C. **Bias Mode A** yields a substantially constant voltage at the output terminals for applications using DC coupling to succeeding stages or requiring maximum dynamic range over the temperature range. DC output voltage varies less than 0.1 volt (typically) over the entire temperature range while gain varies ±2 dB. **Bias Mode B** provides extremely stable gain over the temperature range. Gain variation is 0 dB (typically) in this Bias Mode. DC variation is ±0.8 volt.

Provisions are also made for stabilizing the operating point for either single or split power supplies.

FEATURES

- High Differential Push-Pull Voltage Gain..... 37 dB typ.
  Single-Ended Voltage Gain..... 31 dB typ.
- Wide (3dB) Bandwidth..... 55 MHz typ.
- Balanced Input and Output
- High Input Resistance..... 150 kΩ typ.
- Low Output Resistance..... 125 Ω typ.
- Bias Options for Temperature Compensation:
  Bias Mode A: "Constant" Voltage
  Bias Mode B: "Constant" Gain
- **Supplied in the hermetic 12-lead TO-5 style package**

APPLICATIONS

- Video Amplifier
- Modulator
- Mixer
- Schmitt Trigger
- IF Amplifier
- DC Amplifier
- Sense Amplifier

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION * . . . . . 450 mW
Derating factor for T_A > 85°C . . . . . 5 mW/°C
TEMPERATURE RANGE:
Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

* Limitation imposed by the thermal resistance of package.

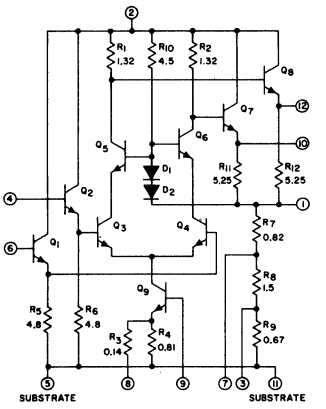


Fig.1 - Schematic Diagram for CA3040

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 2 with respect to terminal 11 is 0 to +14 volts.

TERMINAL No.	1	2	3	4	5▲	6	7	8	9	10	11▲	12
1		0 -14	*	*	+14 0	*	+10 -10	*	*	*	+14 0	*
2			*	+14 0	+14 0	+14 0	*	*	*	+14 0	+14 0	+14 0
3				*	+5 -3	*	*	*	*	*	+5 -3	*
4					*	+3 -3	*	*	*	*	*	*
5▲					▲	*	+10 -3	*	+3 -7	*	0 Note 1	*
6							*	*	*	*	*	*
7								*	*	*	+10 -3	*
8									+3 -3	*	*	*
9										*	+7 -3	*
10											*	*
11▲											▲	*
12												

▲ Reference Substrate

Note 1: External connection required for proper operation.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	-	-
3	5	5
4	1	0.1
5	-	-
6	1	0.1
7	5	5
8	5	5
9	1	0.1
10	-	10
11	-	-
12	-	10

STATIC CHARACTERISTICS TEST CIRCUITS

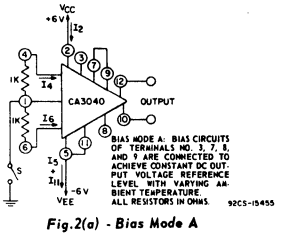


Fig.2(a) - Bias Mode A

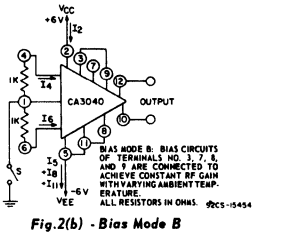


Fig.2(b) - Bias Mode B

OPERATING CONSIDERATIONS

General

The CA3040 is designed to provide flexibility in the selection of power supply configurations and to provide the circuit designer the choice between two modes of temperature-compensated performance. Mode A, which provides constant DC output voltage, is recommended for most applications. The control of the operating point provided by this mode maintains the dynamic range of the device while gain variation over most of the range is less than ±1 dB. Mode B provides constant gain for applications where this consideration is critical, but will exhibit a reduction of dynamic range at the temperature extremes.

Power Supply Considerations

Figures 2 and 3 illustrate the use of the CA3040 with balanced dual supplies and single power supplies, respectively. Both figures demonstrate that the inputs may be directly referenced to the center point of the supply (ground in Fig.2) by closing the included switch. This is the natural connection in Fig.2. This connection is optional, however, and need not be made. Use of this connection in Fig.3 implies the presence of another DC supply or a "stiff" bleeder. If such a source is present its use is suggested in order to maintain maximum common mode range. Dynamic performance and dynamic range of the output circuit are unaffected by the choice of biasing scheme used so that in most cases direct connection of Terminal No.1 to the center point of the supply is not required. Where direct connection is not used, Terminals No.4 and No.6 must be biased from Terminal No.1 for proper operation.

High-Frequency Considerations

Stable high-frequency operation requires that proper high-frequency construction techniques be followed. The photograph of Fig.6 illustrates the precautions taken in the construction of the test circuit of Fig.3.

Extreme caution is required because of the extended gain bandwidth capability of the device. Oscillations have been observed in the 400-to-800 MHz range when precautions were not taken. In addition to normal considerations of shielding, parts layout, and isolation, the following specific suggestions are made:

1. Use sockets only when necessary. Sockets, when used, must provide shielding within the pin circle. The socket shown in the chassis of Fig.6 is a Barnes MG-1201, or equivalent, modified by drilling a 1/8" hole in the center and inserting a grounded brass pin.
2. Do not bypass Terminal No.9 in normal operation. Fig.3 shows the use of neutralization between Terminal No.9 and one output to balance the amplifier at high frequencies. Experience shows that stable operation, while possible, is difficult to achieve if Terminal No.9 is bypassed to ground.
3. In DC testing, 1 kΩ, 1/4 W carbon resistors should be soldered directly to the socket Terminals No.4 and No.6 to suppress parasitic oscillations. All current carrying connections are made at the other end of the resistors. Direct sensing of Terminal No.4 or No.6 voltage should not be attempted.

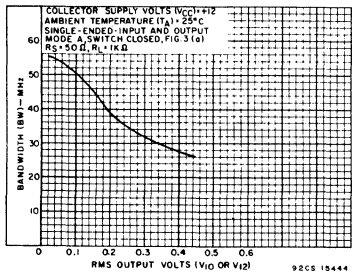


Fig.7 - 3dB Bandwidth vs Single-Ended Output Voltage

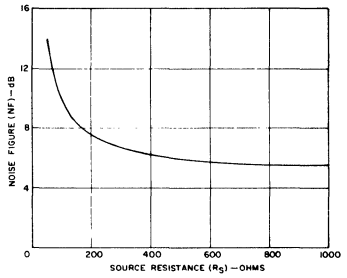


Fig.8 - Noise Figure (NF) vs Source Impedance

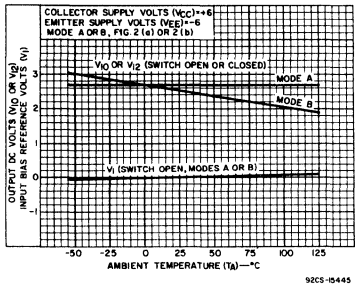


Fig.9 - Output Volts or Input Bias Reference Volts vs Ambient Temperature

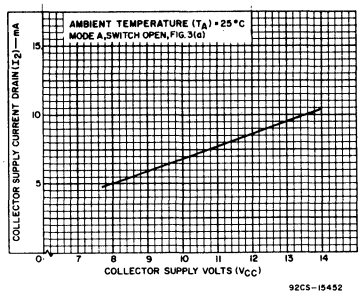


Fig.10 - Collector Supply Current Drain (I_2) vs Collector Supply Voltage (V_{CC})

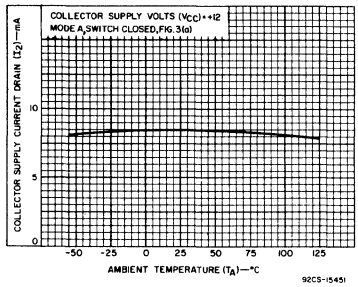


Fig.11 - Collector Supply Current Drain (I_2) vs Ambient Temperature

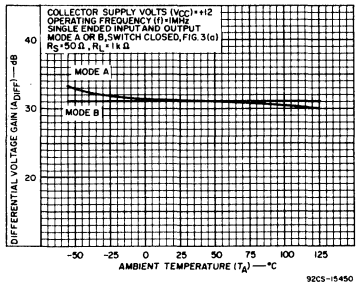


Fig.12 - Single-Ended Differential Voltage Gain vs Ambient Temperature

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS
DYNAMIC CHARACTERISTICS						
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF

STATIC CHARACTERISTICS

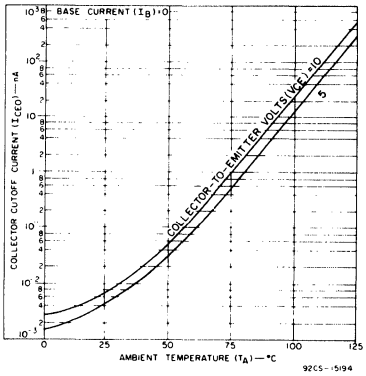


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

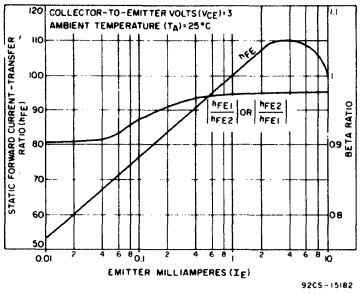


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

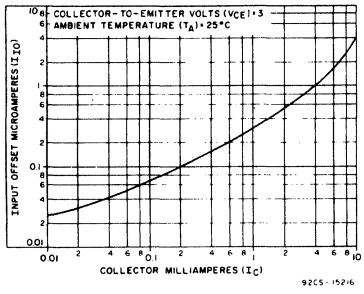


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

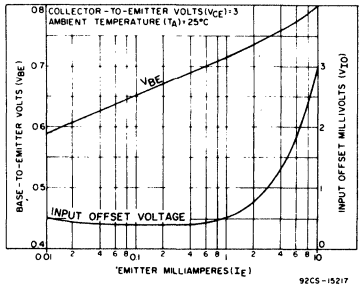


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

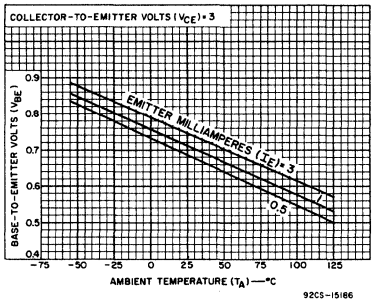


Fig. 7 — Typical base-to-emitter voltage characteristics vs ambient temperature for each transistor.

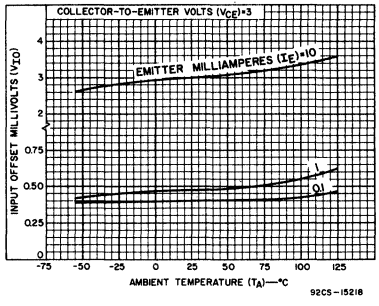


Fig. 8 — Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

Amplifier Array

FOUR INDEPENDENT AC AMPLIFIERS

For Low-Noise and General AC Applications In Industrial Service

The RCA CA3048 is a silicon monolithic integrated circuit consisting of four independent identical AC amplifiers which can operate from a single-ended power supply.

The amplifiers include internal DC bias and feedback to provide temperature-stabilized operation. They may be used in a wide variety of AC applications in which operational amplifiers have previously been used.

Each high gain amplifier has a high impedance non-inverting input, and a lower impedance inverting input for the application of feedback. Two power-supply terminals and two ground terminals are provided to reduce internal and external coupling between amplifiers.

The CA3048 is supplied in a 16-lead dual-in-line plastic package.

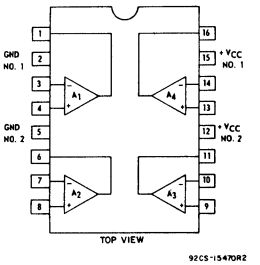


Fig.1 - Block diagram for CA3048.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:
- At T_A = 55°C ..... 750 mW
- Above T_A = 55°C ..... Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:
- Operating ..... -40°C to +85°C
- Storage ..... -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ±0.79mm) from case for 10 seconds max. ..... +265°C

POWER SUPPLY VOLTAGE ..... +16 V

AC INPUT VOLTAGE ..... 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	-3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*		*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

FEATURES

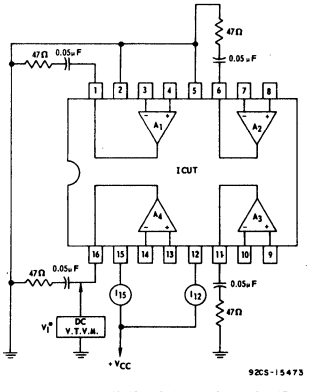
- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

- Noise figure at 1 kHz ..... 2 dB typ.
- High voltage gain ..... 53 dB min.
- High input resistance ..... 90 kΩ typ.
- Undistorted output voltage ..... 2 V rms min.
- Output Impedance ..... 1 kΩ typ.
- Open-loop bandwidth ..... 300 kHz typ.

APPLICATIONS

- Multi-channel or cascade operation
- Low-level preamplifiers
- Equalizers
- Linear signal mixers
- Tone generators
- Multivibrators
- AC integrators



* CONNECT TO APPROPRIATE TERMINAL TO READ VOLTAGE

Fig.2 - Test circuit for measurement of collector supply voltage and currents.

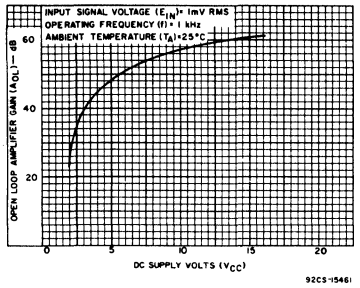


Fig.7 - Typical amplifier gain vs DC supply voltage.

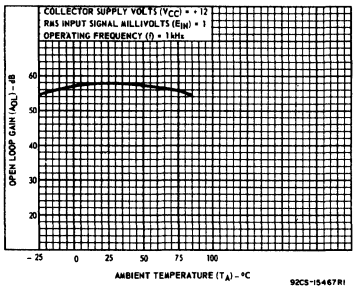


Fig.8 - Typical open-loop gain vs ambient temperature.

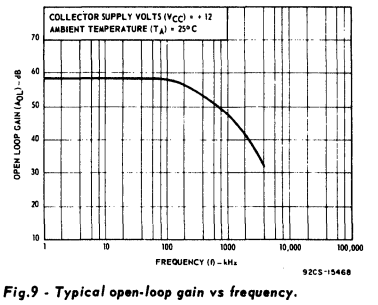


Fig.9 - Typical open-loop gain vs frequency.

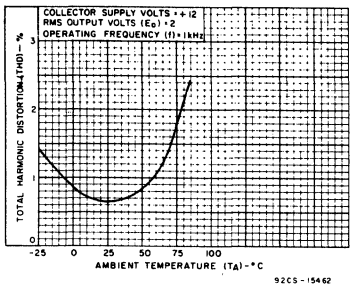
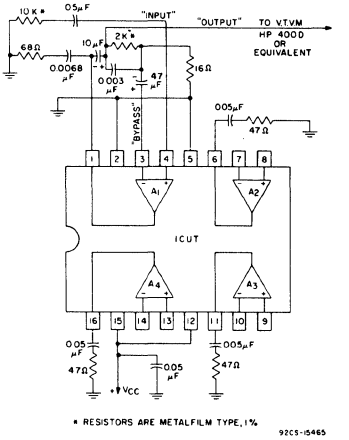


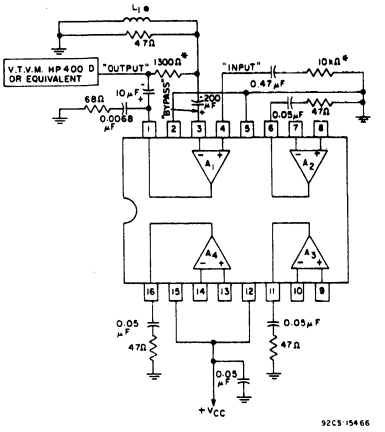
Fig.10 - Typical total harmonic distortion vs ambient temperature.



To test Amplifiers 1, 2, 3, or 4, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.11 - Test circuit for measurement of broadband noise characteristic.

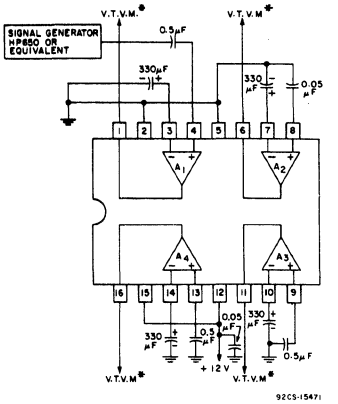


● L_1 - 2.5 millihenry inductor, dc resistance 0.3 ohms or less.

* Resistors metal film type, 1%. To test amplifiers, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.12 - Test circuit for measurement of "weighted" output noise voltage characteristic.



* V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig.13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

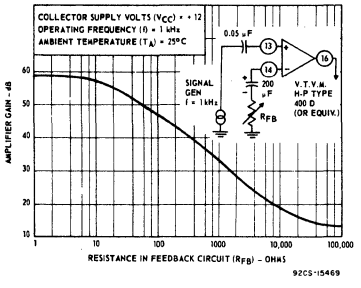


Fig.14 - Typical amplifier gain vs feedback resistance.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3048 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig.14 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3048, as in other devices having high gain-bandwidth product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3048 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIRCUIT FIG.	CA3049T LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	---	0.25	---	mV	-4
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2 mA		1	---	0.3	---	μA	---
Input Bias Current	I_{IB}			1		13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\lvert\frac{\Delta V_{IO}}{\Delta T}\rvert$			1	---	1.1	---	μV/°C	4
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V, I_C = 1 mA		---	---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6 V, I_C = 1 mA		---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		---	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_B = 0, I_E = 0		---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		---	5	7	---	V	---
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 KH$_3$, R_S = 500 Ω, I_C = 1 mA		---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6 V, I_C = 5 mA		---	---	1.35	---	GH_z	11
Collector-Base Capacitance	C_{CB}	I_C = 0, V_{CB} = 5V	*	---	---	0.28	---	pF	8
			**	---	---	0.28	---	pF	
Collector-Substrate Capacitance	C_{CI}	I_C = 0, V_{CI} = 5V			---	1.65	---	pF	8
For Each Differential Amplifier									
Common-Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2 mA		---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	---	23	---	dB	---
Noise Figure	NF	V_{CC} = 12V	Cascode	3	---	4.6	---	dB	---
Input Admittance	Y_{11}	For Cascode Configuration, $I_3 = I_9$ = 2 mA	Cascode	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration, $I_3 = I_9$ = 4mA (each collector $I_C \simeq$ 2mA)	Cascode	---	---	0 - j 0.006	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

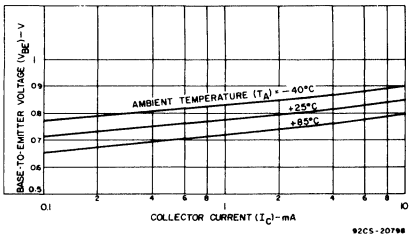


Fig. 6—Base-to-emitter voltage vs. collector current.

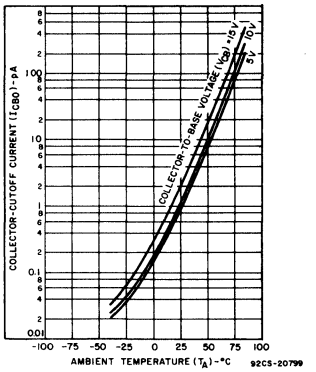


Fig. 7—Collector-cutoff current vs. temperature.

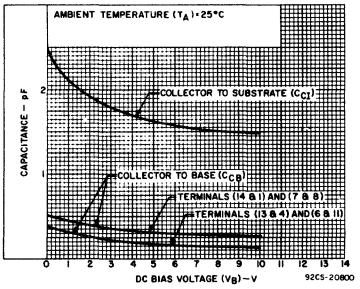


Fig. 8—Capacitance vs. dc bias voltage.

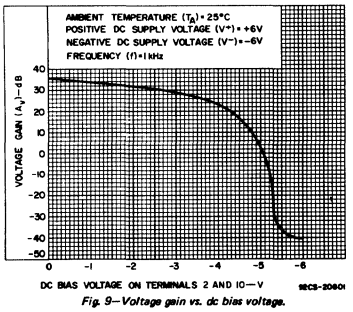


Fig. 9—Voltage gain vs. dc bias voltage.

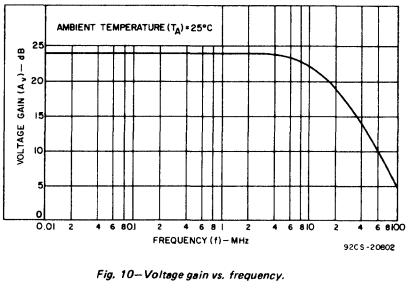


Fig. 10—Voltage gain vs. frequency.

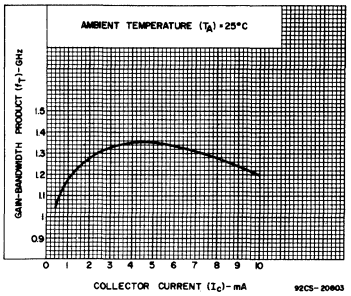


Fig. 11—Gain-bandwidth product vs. collector current.

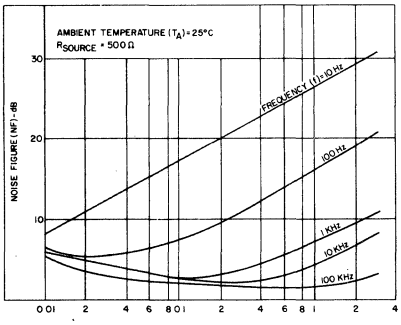


Fig. 12—1/f noise figure vs. collector current.

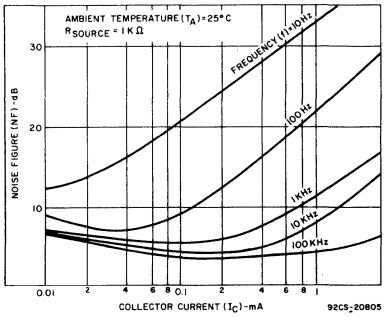


Fig. 13—1/f noise figure vs. collector current.

Typical Output Admittance Characteristics for CA3049T and CA3102E

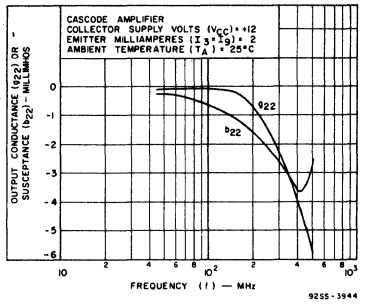


Fig. 20—Output admittance (Y_{22}) vs. frequency.

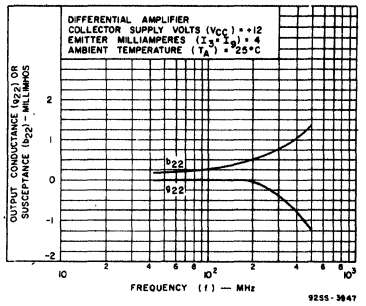


Fig. 21—Output admittance (Y_{22}) vs. frequency.

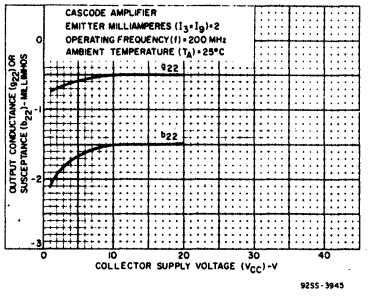


Fig. 22—Output admittance (Y_{22}) vs. collector supply voltage.

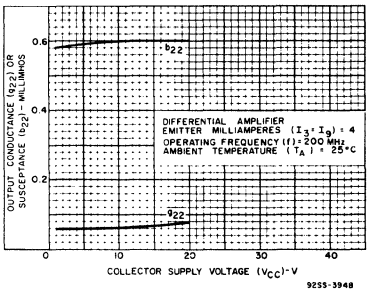


Fig. 23—Output admittance (Y_{22}) vs. collector supply voltage.

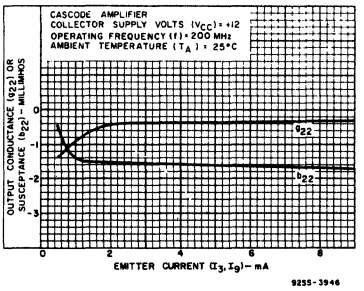


Fig. 24—Output admittance (Y_{22}) vs. emitter current.

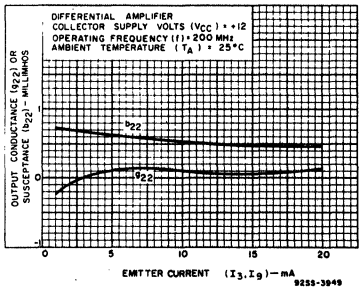


Fig. 25—Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

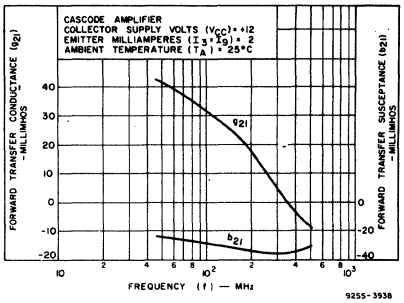


Fig. 26—Forward transfer admittance (Y_{21}) vs. frequency.

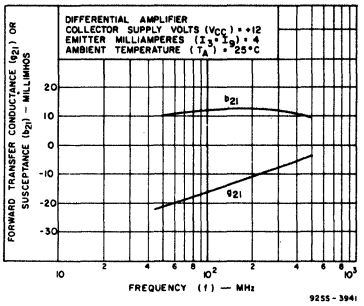


Fig. 27—Forward transfer admittance (Y_{21}) vs. frequency.

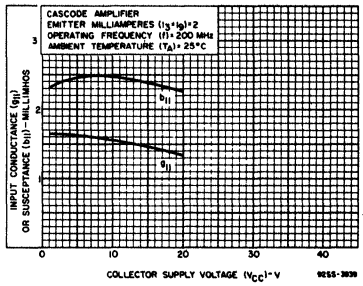


Fig. 28—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

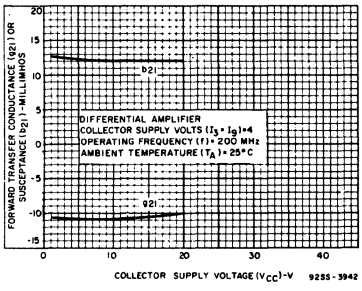


Fig. 29—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

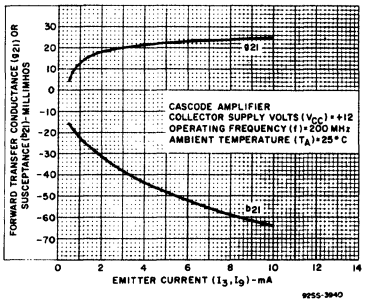


Fig. 30—Forward transfer admittance (Y_{21}) vs. emitter current.

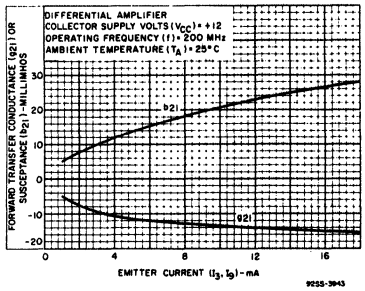


Fig. 31—Forward transfer admittance (Y_{21}) vs. emitter current.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3050/CA3051			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Amplifier Characteristics								
Input Offset Voltage	V_{IO}		–	–	1.5	5	mV	2a,b
Input Offset Current	I_{IO}		–	–	7	70	nA	3a,b
Input Bias Current	I_{IB}		–	–	200	500	nA	4a,b
Quiescent Operating Current Ratio	$\frac{(I_4+I_{12})}{I_3}$ or $\frac{(I_6+I_7)}{I_3}$	V_{CC} = + 6 V, I_3 = 2 mA	–	0.9	1.00	1.13	–	5a,b
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 50 μA	–	–	0.645	0.700	V	6
		V_{CE} = 3 V, I_C = 1 mA	–	–	0.725	0.800		
		V_{CE} = 3 V, I_C = 3 mA	–	–	0.760	0.850		
		V_{CE} = 3 V, I_C = 10 mA	–	–	0.805	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	–	–	-1.9	–	mV/°C	7
Transistor Characteristics								
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	0.002	100	nA	8
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V	–
DYNAMIC								
Transistor Characteristics								
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	–	–	0.78	–	pF	9
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	–	–	0.47	–	pF	9
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	–	–	1.92	–	pF	9
Amplifier Characteristics								
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 5 V, I_C = 3 mA	–	–	600	–	MHz	10
Forward Transadmittance (With single-ended input and output)	$\lvert y_{21} \rvert$	V_{CC} = 10 V, I_3 = 2 mA f = 1 MHz	11	7	9	11	mmho	11
Bandwidth at -3 dB Point	BW	V_{CC} = 10 V, I_3 = 2 mA	11	–	4.3	–	MHz	11
Input Impedance	Z_I	V_{CC} = 10 V, I_3 = 2 mA f = 1 KHz	12	–	460	–	kΩ	12
Output Impedance	Z_O	I_3 = 2 mA, f = 1 KHz	13	–	170	–	kΩ	13
Common-Mode Rejection Ratio	CMR	I_3 = 2 mA, f = 1 KHz	–	–	65	–	dB	–
AGC Range	AGC	I_3 = 2 mA, f = 1 KHz Terminal No.3 Grounded	11	–	60	–	dB	–

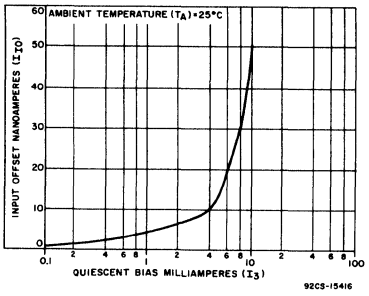


Fig.3(a) - Typical input offset current vs quiescent bias current.

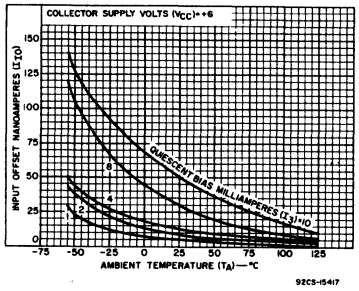


Fig.3(b) - Typical input offset current vs ambient temperature.

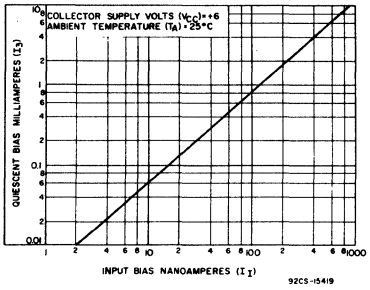


Fig.4(a) - Typical quiescent bias current vs input bias current.

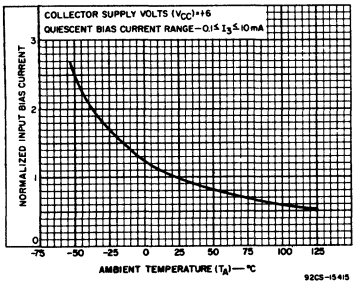


Fig.4(b) - Typical normalized input bias current vs ambient temperature.

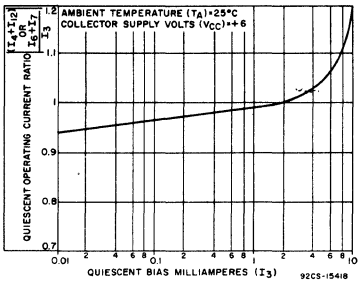


Fig.5(a) - Typical quiescent operating current ratio vs quiescent bias current.

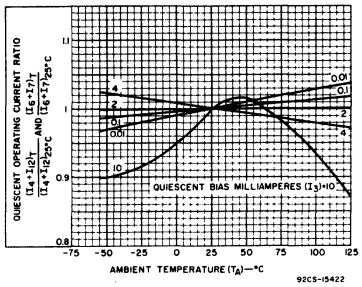


Fig.5(b) - Typical quiescent operating current ratio vs ambient temperature.

Zero-Voltage Switches

For 50/60 and 400 Hz Thyristor Control Applications

The RCA-CA3058, CA3059, and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see Fig. 1) as follows:

1. Limiter-Power Supply—Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier—Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector—Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit—Provides high-current pulses to the gate of the power controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (see Fig. 1):

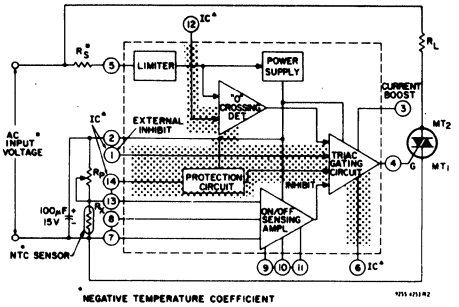
1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

For an explanation of these functions see Operating Considerations. For detailed application information, see companion Application Note, ICAN-6182, "Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)".

The CA3058 is supplied in a hermetic 14-lead dual-in-line ceramic package. Types CA3059 and CA3079 are supplied in 14-lead dual-in-line plastic packages.

Applications:

- **Relay control**
- **Heater control**
- **Valve control**
- **Lamp control**
- **Synchronous switching of flashing lights**
- **On-off motor switching**
- **Differential comparator with self-contained power supply for industrial applications**
- **Photosensitive control**
- **Power one-shot control**



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE:
Circuitry, within shaded areas, not included in CA3079

- See chart

▲ IC = Internal Connection - - DO NOT USE (Terminal Restriction applies only to CA3079).

Fig. 1—Functional block diagram of CA3058, CA3059, and CA3079.

Features	CA3058	CA3059	CA3079
■ 24V, 120V, 208/230V, 277V at 50 60, or 400 Hz operation	√	√	√
■ Differential Input	√	√	√
■ Low Balance Input Current (max.) -μA	1	1	2
■ Built-in Protection Circuit for opened or shorted sensor (Term. 14)	√	√	
■ Sensor Range (R_X) - kΩ	2 to 100	2 to 100	2 to 50
■ DC Mode (Term 12)	√	√	
■ External Trigger (Term. 6)	√	√	
■ External Inhibit (Term. 1)	√	√	
■ DC Supply Volts (max.)	14	14	10
■ Operating Temperature Range - °C		−55 to +125	

MAXIMUM RATINGS,
Absolute-Maximum Values at T_A = 25°C

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 7):
CA3058, CA3059 ..... 14 V
CA3079 ..... 10 V
DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 8);
CA3058, CA3059 ..... 14 V
CA3079 ..... 10 V
PEAK SUPPLY CURRENT (TERMS. 5 AND 7) ..... ±50 mA
OUTPUT PULSE CURRENT (TERM. 4) ..... 150 mA

POWER DISSIPATION:
Up to T_A=75°C – CA3058 ..... 700 mW
Up to T_A=55°C – CA3059,CA3079 ... 700 mW
Above T_A=75°C – CA3058 ..... Derate Linearly 8 mW/°C
Above T_A=55°C – CA3059,CA3079 ..... Derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... −55 to +125°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

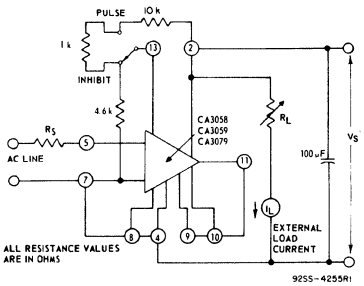


Fig. 2(a)—DC supply voltage test circuit for CA3058, CA3059, and CA3079.

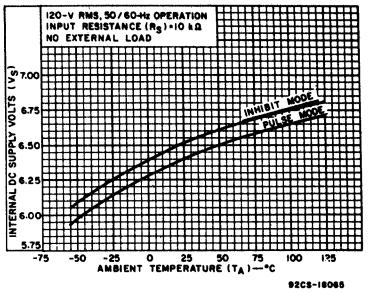


Fig. 2(b)—DC supply voltage vs. ambient temperature for CA3058, CA3059 and CA3079.

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS T_A = 25°C (Unless Indicated Otherwise)	LIMITS			UNITS
		Min.	Typ.	Max.	
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)•					
DC Supply Voltage, V_S					
Inhibit Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6.1	6.5	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.8	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.4	–	V
Pulse Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6	6.4	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.7	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.3	–	V
At 50/60 Hz (CA3058) *See Fig. 2*	R_S = 8 kΩ, I_L = 0, T_A = −55 to +125°C	5.5	–	7.5	V
Gate Trigger Current, I_{GT}[4] *See Figs. 3, 5(a)*	Terms. 3 and 2 connected, V_{GT} = 1 V	–	105	–	mA
Peak Output Current (Pulsed), I_{OM}[4]	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	–	mA
With Internal Power Supply	Terms. 3 and 2 connected, Gate Trigger Voltage (V_{GT})=0	90	124	–	mA
	Term. 3 open, V^+=12 V, V_{GT}=0	–	170	–	mA
With External Power Supply *See Figs. 5, 6*	Terms. 3 and 2 connected, V^+=12 V, V_{GT} = 0	–	240	–	mA
Inhibit Input Ratio, V_9/V_2					
All Types	Voltage Ratio of Term. 9 to 2	0.465	0.485	0.520	–
CA3058 *See Fig. 7*	T_A = −55 to +125°C	0.450	–	0.520	–
Total Gate Pulse Duration:*					
For positive dv/dt, t_P					
50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz	C_{EXT} = 0, R_{EXT} = ∞	–	12	–	μs
For negative dv/dt, t_N					
50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz *See Fig. 8*	C_{EXT} = 0, R_{EXT} = ∞	–	10	–	μs
Pulse Duration After Zero Crossing (50-60 Hz):					
For positive dv/dt, t_{P1}	C_{EXT} = 0	–	50	–	μs
For negative dv/dt, t_{N1} *See Fig. 8*	R_{EXT} = ∞	–	60	–	μs
Output Leakage Current, I_4 Inhibit Mode:					
All Types		–	0.001	10	μA
CA3058 *See Fig. 9*	T_A = −55 to +125°C	–	–	20	μA
Input Bias Current, I_I					
CA3058, CA3059		–	220	1000	nA
CA3079 *See Fig. 10*		–	220	2000	nA

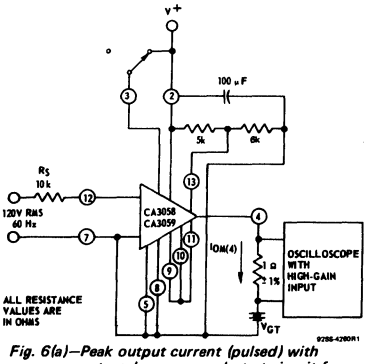


Fig. 6(a)—Peak output current (pulsed) with external power supply test circuit for CA3058 and CA3059.

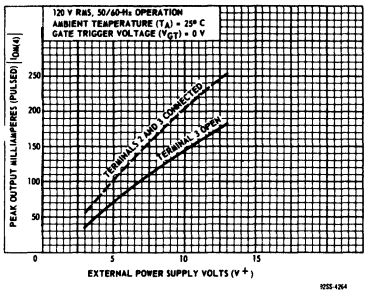


Fig. 6(b)—Peak output current (pulsed) vs. external power supply voltage for CA3058 and CA3059.

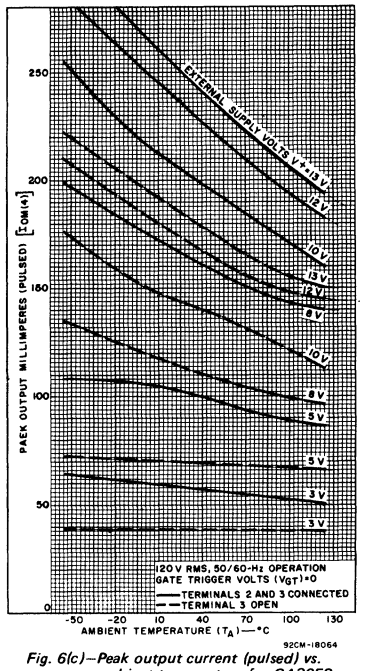


Fig. 6(c)—Peak output current (pulsed) vs. ambient temperature for CA3058 and CA3059.

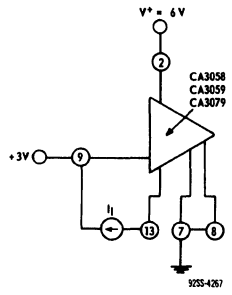


Fig. 10—Input bias current test circuit for CA3058, CA3059, and CA3079.

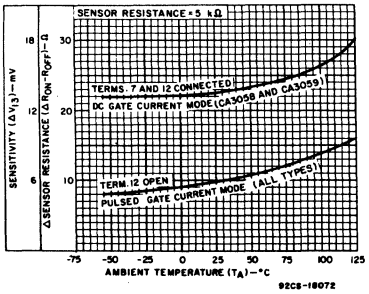


Fig. 12—Sensitivity vs. ambient temperature for CA3058, CA3059, and CA3079.

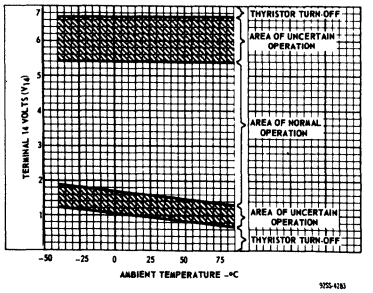
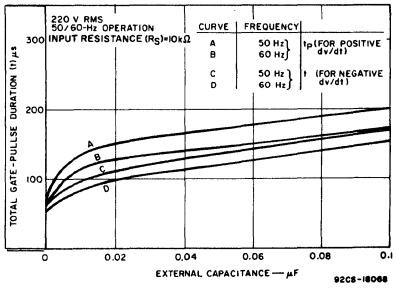
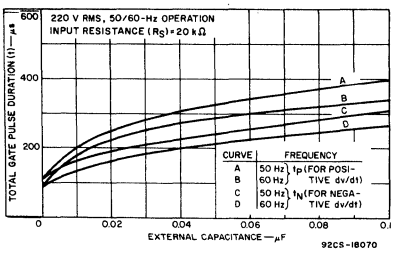


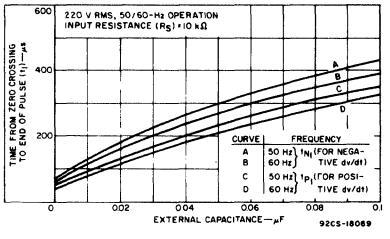
Fig. 13—Operating regions for built-in protection circuit for CA3058 and CA3059.



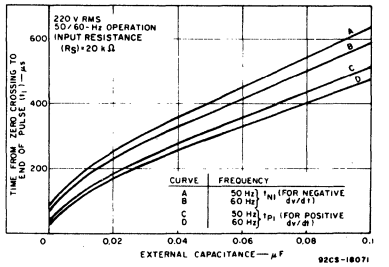
(a)



(b)



(c)



(d)

Fig. 11—Relative pulse width and location of zero crossing for 220-volt operation for CA3058, CA3059, and CA3079.

OPERATING CONSIDERATIONS

Power Supply Considerations for CA3058, CA3059, and CA3079

The CA3058, CA3059, and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3(b) and 3(c).

Power Supply Considerations for CA3058 and CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5(a).

Operation of Built-in Protection for the CA3058, CA3059

A special feature of the CA3058 and CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2 mA with a 5 kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2 kΩ and 100 kΩ.
3. The ratio of R_X to R_P, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

External Inhibit Function for the CA3058 and CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10 μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3058 and CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

ELECTRICAL CHARACTERISTICS (CA3060D)
For each amplifier at T_A = 25°C, V^+ = 6 V, V^- = -6 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVES Fig.	LIMITS Amplifier Bias Current I_{ABC} = 1 μA MIN.	TYP.	MAX.	I_{ABC} = 10 μA MIN.	TYP.	MAX.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a, b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a, b	1.3	2.3	–	15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	4.6	5	–	4.5	4.8	–	4.5	4.7	–	V
Negative	V_{OM^-}	7	5.8	5.95	–	5.8	5.95	–	5.7	5.9	–	V
Amplifier Supply Current (each amplifier)	I_A	8a, b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P	–	–	0.10	0.17	–	1	1.45	–	10	14.5	mW
Input Offset-Voltage Sensitivity*: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	120	–	2	120	–	2	120	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$	–	–	20	120	–	20	120	–	30	120	
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a, b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–	4.4 to -5.1 min. 4.7 to -5.3 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			V
Slew Rate (Test ckt., Fig. 13	SR		–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25°C, I_Z = 0.1 mA)												
						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature-Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:
(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test ---
V^+ is reduced to 5 volts for V^+ sensitivity
V^- is reduced to -5 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +5 V and -6 V supplies}}{\text{1 volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset - Voffset for -5 V and +6 V supplies}}{\text{1 volt}}$

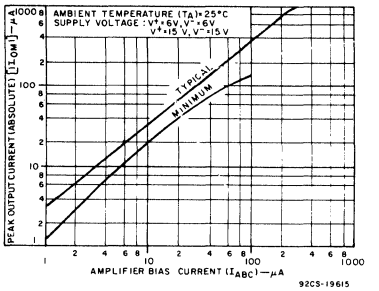


Fig.6a—Peak output current vs. amplifier bias current.

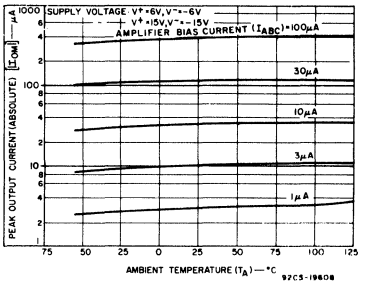


Fig.6b—Peak output current vs. ambient temperature.

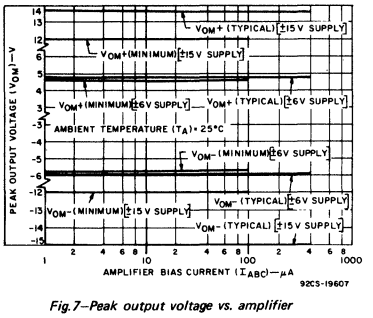


Fig.7—Peak output voltage vs. amplifier bias current.

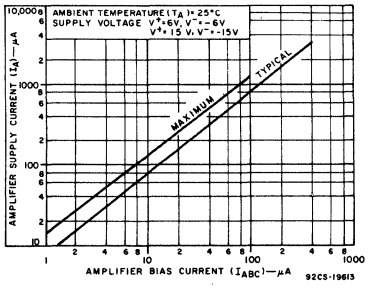


Fig.8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

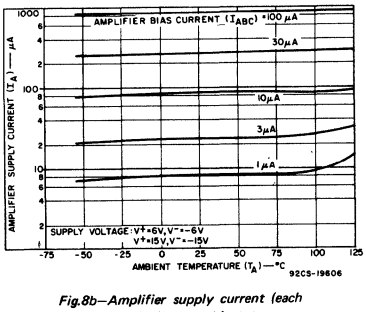


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

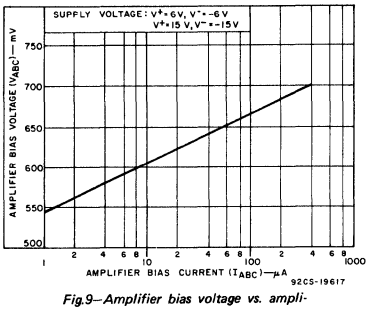


Fig.9—Amplifier bias voltage vs. amplifier bias current.

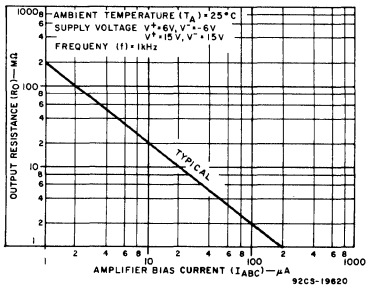


Fig.14—Output resistance vs. amplifier bias current.

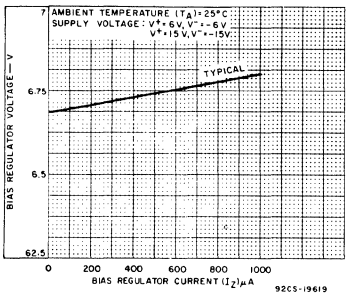


Fig.15—Bias regulator voltage vs. bias regulator current.

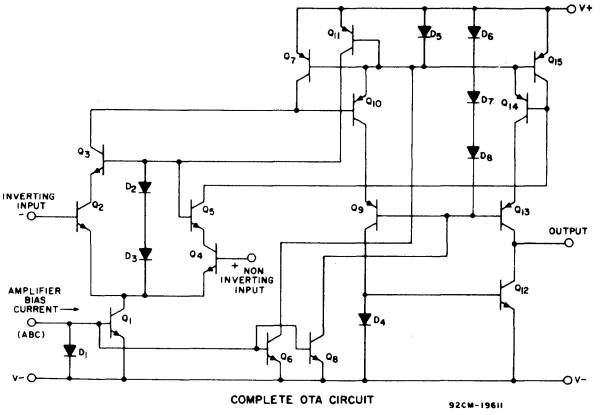


Fig.16 – Complete schematic diagram showing one of the three operational transconductance amplifiers.

OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

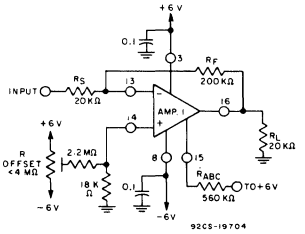


Fig.17—20-dB amplifier using the CA3060.

Circuit Requirements
Closed loop voltage gain = 10 (20 dB)
Offset voltage adjustable to zero
Current drain as low as possible
Supply voltage = ±6 V
Maximum input voltage = ±50 mV
Input resistance = 20 kΩ
Load resistance = 20 kΩ
Device: CA3060

Calculation

1. Required transconductance g_{21}.
   Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

$$g_{21} = A_{OL}/R_L$$

$$= 100/18\ k\Omega$$

$$\cong 5.5\ mmho$$

(R_L = 20 kΩ in parallel with 200 kΩ

≅ 18 kΩ)

2. Selection of suitable amplifier bias current.
   The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5 mmho an amplifier bias current I_{ABC} of 20 μA is suitable.

3. Determination of Output Swing Capability.
   For a loop gain of 10 the output swing is ±0.5 V and the peak load current 25 μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20 kΩ than R_F = 200 kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200 kΩ = 2.5 μA.

   The total amplifier current output requirements are, therefore, ±27.5 μA. Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20 μA the amplifier output current is ±40 μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. Calculation of bias resistance.
   For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5\ k\Omega \text{ or } \cong 560\ k\Omega$$

5. Calculation of offset adjustment circuit.
   In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

$$\text{i.e. } \frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18\ k\Omega$$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e. $200 \times 10^{-9} \times 18 \times 10^3$ volts), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV = ±8.6 mV

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48\ \mu A$$

With a supply voltage of ±6 V, this current can be provided by a 10 MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 MΩ was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-kΩ load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-kΩ 15-pF load modifies the frequency characteristic.

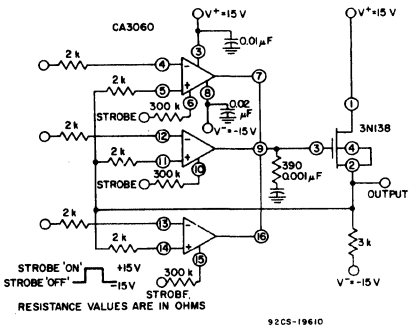


Fig.23—Three-channel multiplexer.

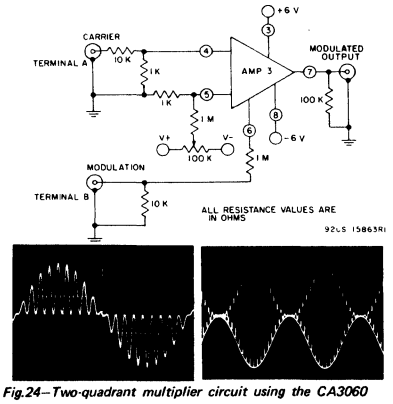


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N138 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at ±6 volts is also possible with several minor changes. First, the resistance in series with amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100 μA of strobe—"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

The phase compensation network consists of a single 390Ω resistor and a 1000-pF capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is 0.3 volts/μsec. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

NON LINEAR APPLICATIONS

AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to V^-.

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.

Four-Quadrant Multiplier

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_O(1) = [-V_X]\ [g_{21}(1)] \qquad \text{(Eq.3)}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_O(2) = [+V_X]\ [g_{21}(2)] \qquad \text{(Eq. 4)}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\ [g_{21}(2) - g_{21}(1)] \qquad \text{(Eq. 5)}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{(Eq. 6)}$$

Hence,

$$g_{21}(2) \approx k\ [\,(V\text{-}) + V_Y\,]. \qquad \text{(Eq. 7)}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\ [(V\text{-}) - V_Y]. \qquad \text{(Eq. 8)}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left\{[(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\right\} \text{ or}$$

$$V_O \approx 2\,k\,R_L\,V_X\,V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the *X* and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

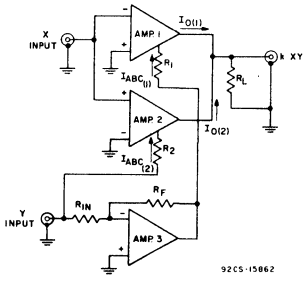


Fig.25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

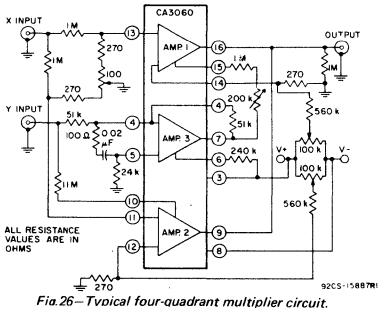


Fig.26—Typical four-quadrant multiplier circuit.

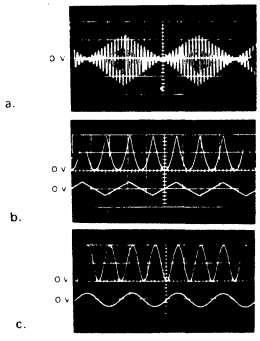


Fig.27—Voltage waveforms of four-quadrant multiplier circuit.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CIRCUIT FIG. NO.
Static Characteristics							
DC Voltage:							
At Terminal 7	V_7	V^+ = 11.2 V	–	6.1	–	V	6
At Terminal 8	V_8		–	5.4	–	V	
At Terminal 12	V_{12}		–	5.2	–	V	
DC Current (into Terminal 5):							
At V^+ = 8.5 V	I_5	–	8.5	15	–	mA	6
At V^+ = 11.2 V			–	17.5	–	mA	
At V^+ = 12.5 V			–	19	29	mA	
Dynamic Characteristics at V^+ = 11.2							
IF AMPLIFIER							
Input Limiting Voltage (knee, – 3dB point)	V_I(lim)	f_0 = 10.7 MHz f(Modulation) = 400 Hz Deviation = ±75 kHz	–	250	600	μV	3
AM Rejection	AMR	f_0 = 10.7 MHz f(Modulation) = 400 Hz FM: Deviation = ±75 kHz AM: Modulation = 30%	–	55	–	dB	5
Input Impedance Components:							
Parallel Resistance	R_I	f_0 = 10.7 MHz	–	4.5	–	kΩ	–
Parallel Capacitance	C_I	V_{IN} = 10 mV RMS	–	4.5	–	pF	
DETECTOR							
Recovered AF Voltage (at Terminal 12)	V_O(AF)	f_0 = 10.7 MHz f(Modulation) = 400 Hz	–	1.5	–	V	3
Total Harmonic Distortion	THD	Deviation = ± 75 kHz	–	1	2	%	
AUDIO PREAMPLIFIER							
Voltage Gain	A(AF)	V_{IN} = 100 mV, f_0 = 400 Hz	–	21	–	dB	4
Total Harmonic Distortion	THD	V_{OUT} = 2 V, f_0 = 400 Hz	–	1.5	5	%	4

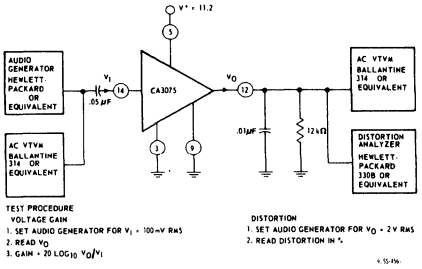


Fig.4 – Test circuit for audio preamplifier voltage gain and total harmonic distortion

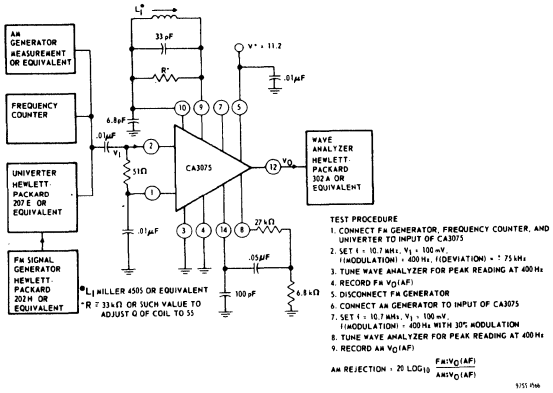


Fig.5 – Test circuit for AM rejection

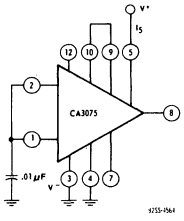
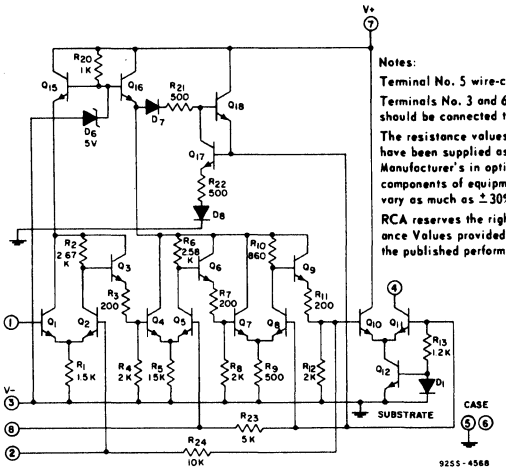


Fig. 6- Test circuit for static characteristics



Notes:

Terminal No. 5 wire-connected to the case.

Terminals No. 3 and 6 which are connected to the substrate should be connected to the most negative point in the circuit.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturer's in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

Fig. 4 - Schematic diagram of CA3076.

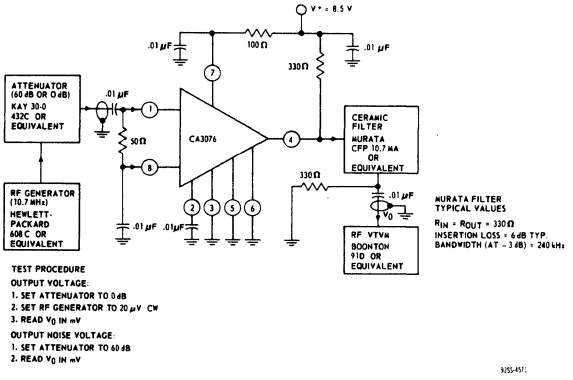


Fig. 5 - 10.7 MHz voltage gain and noise test circuit

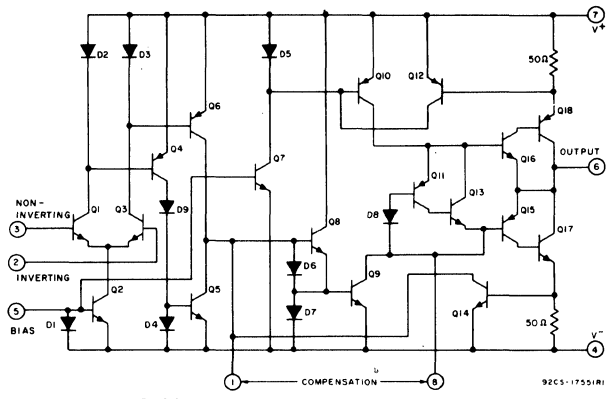


Fig.2-Schematic diagram of the CA3078T and CA3078AT.

Typical Values Intended Only for Design Guidance at T_A = 25°C and V^+ = +6 V, V^- = 6 V

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CA3078AT		CA3078T	UNITS
			R_{SET} = 5.1 MΩ I_Q = 20 μA	R_{SET} = 1 MΩ I_Q = 100 μA	R_{SET} = 1 MΩ I_Q = 100 μA	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T_A$	R_S ≤10 KΩ	5	6	6	μV/°C
Input Offset Current Drift	$\Delta V_{IO}/\Delta T_A$	R_S ≤10 KΩ	6 3	70	70	pA/°C
Open-Loop Bandwidth	BW_{OL}	3dB pt	0 3	2	2	kHz
Slew Rate: Unity Gain	SR	See Figs.	0 027	0.04	0.04	V/μs
Comparator		20, 21	0 5	1 5	1.5	
Transient Response		10% to 90% Rise Time	3	2 5	2.5	μs
Input Resistance	R_I		7 4	1 7	0.87	MΩ
Output Resistance	R_O		1	0 8	0.8	KΩ
Equiv. Input Noise Voltage	e_N(10 Hz)	R_S 0	40	–	25	nV/√Hz
Equiv. Input Noise Current	i_N(10 Hz)	R_S 1 MΩ	0 25	–	1	pA/√Hz

ELECTRICAL CHARACTERISTICS, at T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTICS SYMBOLS	TYPICAL VALUES				UNITS
	CA3078AT		CA3078T		
	V^+ = +1.3V, V^- = -1.3V R_{SET} = 2 MΩ I_Q = 10 μA	V^+ = +0.75V, V^- = -0.75V R_{SET} = 10 MΩ I_Q = 1 μA	V^+ = +1.3V, V^- = -1.3V R_{SET} = 2 MΩ I_Q = 10 μA	V^+ = 0.75V, V^- = -0.75V R_{SET} = 10 MΩ I_Q = 1 μA	
V_{IO}	0,7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1 7	0.5	nA
I_{IB}	3.7	0 45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	μA
P_D	26	1.5	26	1 5	μW
V_{OPP}	1 4	0.3	1 4	0.3	V
V_{ICR}	−0.8 to +1.1	−0.2 to +0.5	−0.8 to +1.1	−0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM^\pm}$	12	0 5	12	0.5	mA
$\Delta V_{IO}/\Delta V^\pm$	20	50	20	50	μV/V

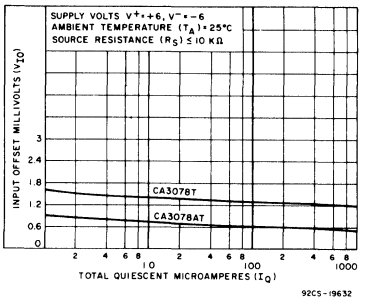


Fig.3 – Input offset voltage vs. total quiescent current.

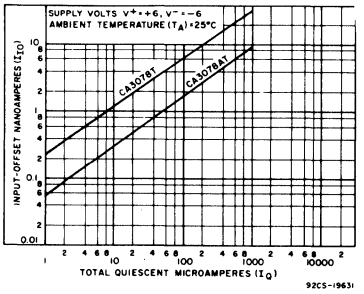


Fig.4 – Input offset current vs. total quiescent current.

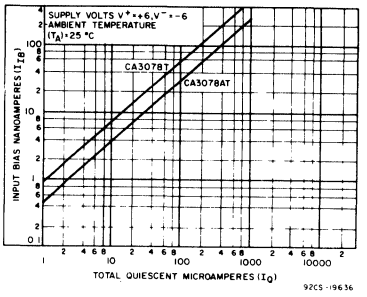


Fig.5 – Input bias current vs. total quiescent current.

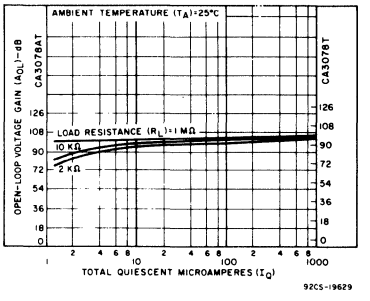


Fig.6 – Open-loop voltage gain vs. total quiescent current.

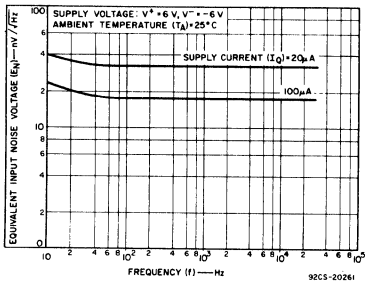


Fig.18 – Equivalent input noise voltage vs. frequency.

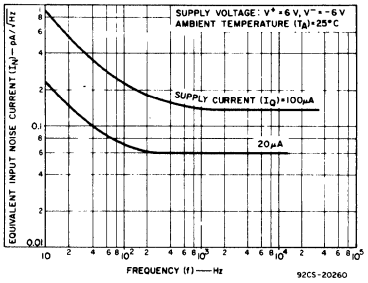


Fig.19 – Equivalent input noise current vs. frequency.

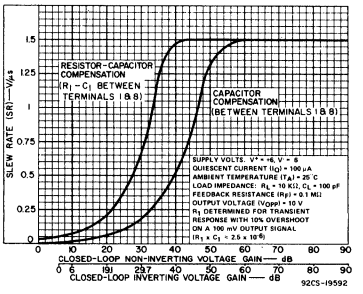


Fig.20 – Slew rate vs. closed-loop gain for I_Q = 100 μA – CA3078T.

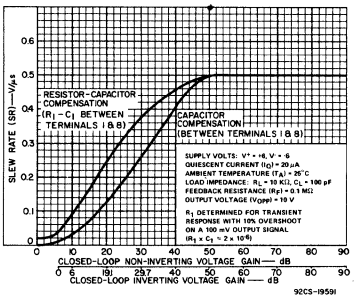


Fig.21 – Slew rate vs. closed-loop gain for I_Q = 20 μA – CA3078AT.

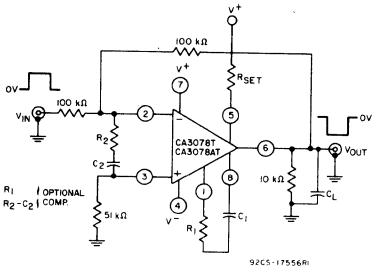


Fig.22 – Transient response and slew-rate, unity gain (inverting) test circuit.

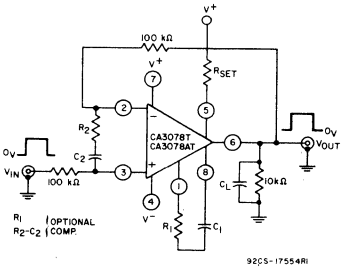


Fig.23 – Slew, rate, unity gain (non-inverting) test circuit.

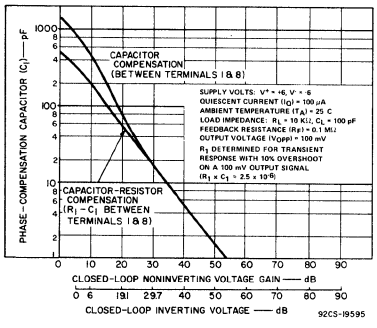


Fig.24 – Phase compensation capacitance vs. closed-loop gain – CA3078T.

Table I - Unity-gain slew rate vs. compensation – CA3078T and CA3078AT

SUPPLY VOLTS: V^+ = 6, V^- = -6
OUTPUT VOLTAGE (V_O) = ±5V
LOAD RESISTANCE (R_L) = 10 kΩ
TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE of 100 mV
AMBIENT TEMPERATURE (T_A) = 25°C

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078T – I_Q = 100 μA	kΩ	pF	kΩ	μF	V/μs	kΩ	pF	kΩ	μF	V/μs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078AT – I_Q = 20 μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

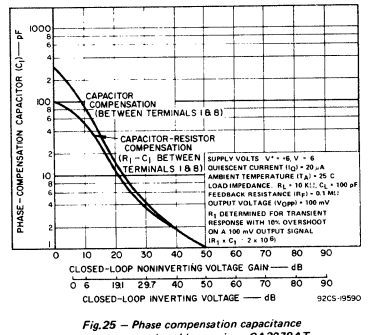


Fig.25 – Phase compensation capacitance vs. closed-loop gain – CA3078AT.

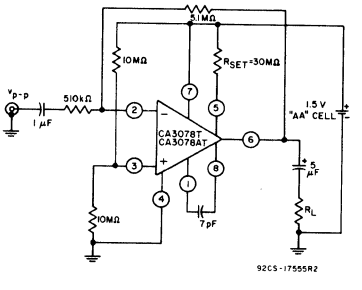


Fig.27 – Inverting 20-dB amplifier circuit.

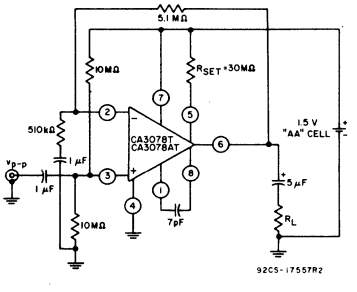


Fig.28 – Non-inverting 20-dB amplifier circuit.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS (V^+ = 15 V, V^- = −15 V, I_{ABC} = 500 μA, T_A = 25°C (unless indicated otherwise))	CA3080 CA3080E CA3080S LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage	V_{IO}		–	0.4	5	mV
		T_A = 0 to 70°C	–	–	6	
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		T_A = 0 to 70°C	–	–	7	
Forward Transconductance (large signal)	g_m		6700	9600	13000	μmho
		T_A = 0 to 70°C	5400	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$	R_L = 0	350	500	650	μA
		R_L = 0, T_A = 0 to 70°C	300	–	–	
Peak Output Voltage:						
Positive	V^+_{OM}	R_L = ∞	12	13.5	–	V
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						
Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080 CA3080E CA3080S	
Input Offset Voltage	V_{IO}	I_{ABC} = 5 μA	0.3	mV
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	I_{ABC} = 500 μA to I_{ABC} = 5 μA	0.2	mV
Peak Output Current	I_{OM}	I_{ABC} = 5 μA	5	μA
Peak Output Voltage:				
Positive	V^+_{OM}	I_{ABC} = 5 μA	13.8	V
Negative	V^-_{OM}		−14.5	
Magnitude of Leakage Current		I_{ABC} = 0, V_{TP} = 0	0.08	nA
		I_{ABC} = 0, V_{TP} = 36 V	0.3	
Differential Input Current		I_{ABC} = 0, V_{DIFF} = 4 V	0.008	nA
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				
Maximum (uncompensated)	SR		75	V/μs
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}		2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

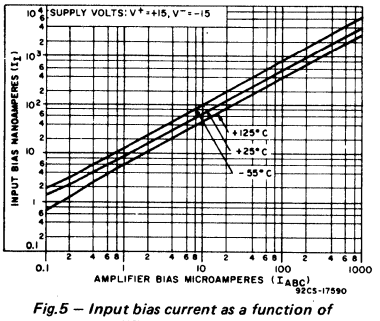


Fig.5 – Input bias current as a function of amplifier bias current.

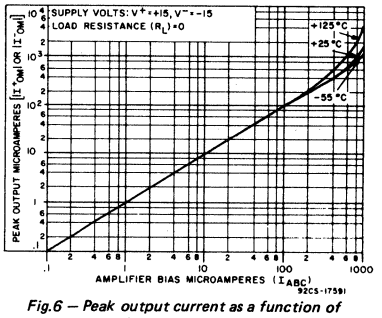


Fig.6 – Peak output current as a function of amplifier bias current.

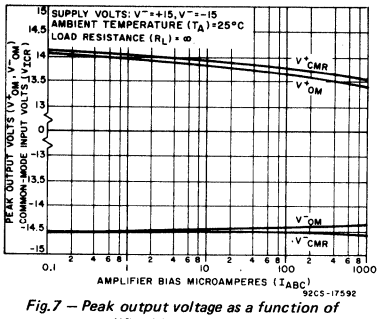


Fig.7 – Peak output voltage as a function of amplifier bias current.

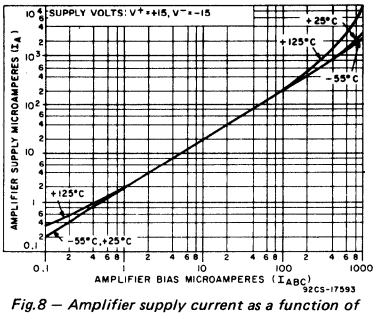


Fig.8 – Amplifier supply current as a function of amplifier bias current.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

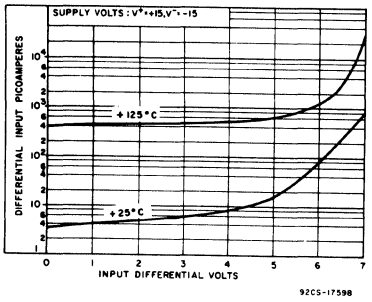


Fig. 13 – Input current as a function of input differential voltage.

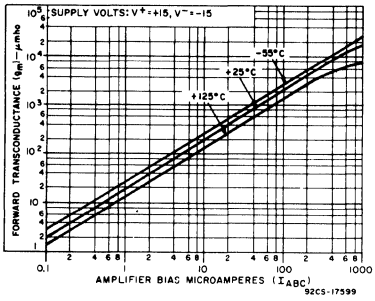


Fig. 14 – Transconductance as a function of amplifier bias current.

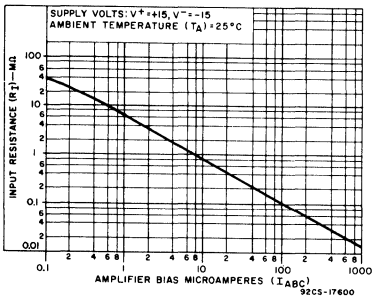


Fig. 15 – Input resistance as a function of amplifier bias current.

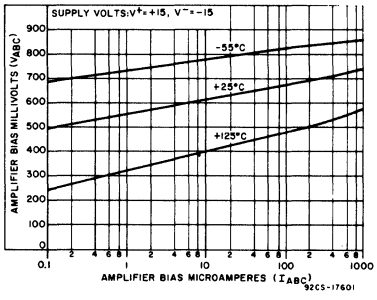


Fig. 16 – Amplifier bias voltage as a function of amplifier bias current.

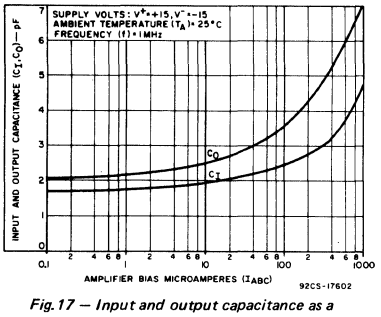


Fig. 17 – Input and output capacitance as a function of amplifier bias current.

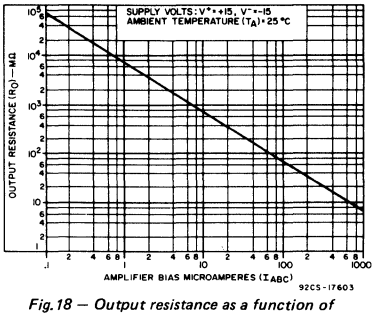


Fig. 18 – Output resistance as a function of amplifier bias current.

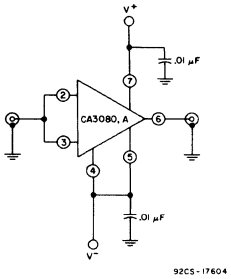


Fig. 19 – Input-to-output capacitance test circuit.

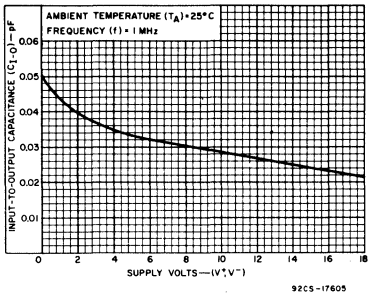
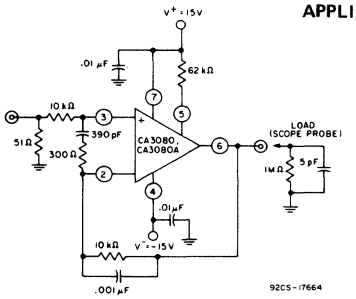


Fig. 20 – Input-to-output capacitance as a function of supply voltage.

APPLICATIONS



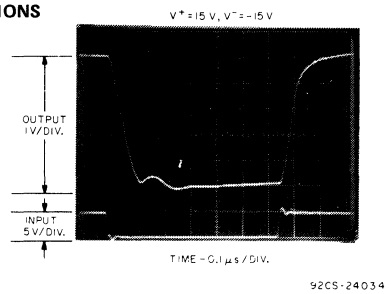
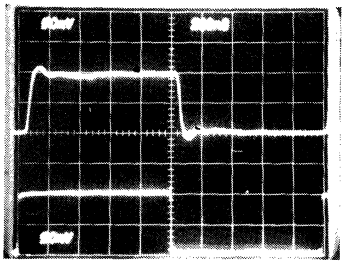


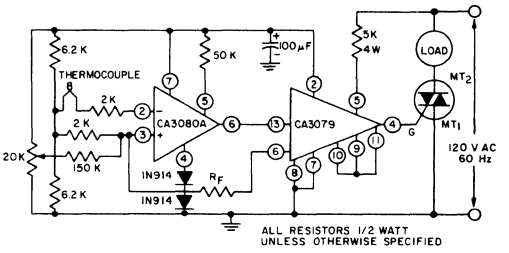
Fig. 21 – Schematic diagram of the CA3080 and CA3080A in a unity-gain voltage follower configuration and associated waveform.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200 ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)

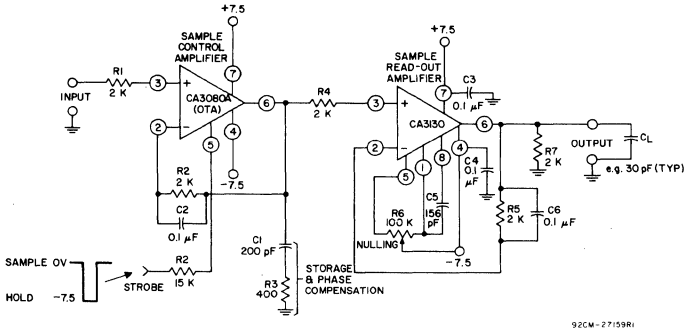
92CS-27883

Fig.28 – Input and output response for circuit shown in Fig. 25.



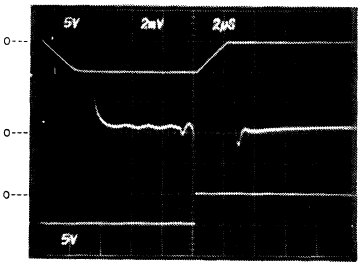
92CS-22619RI

Fig.29 – Thermocouple temperature control with CA3079 zero voltage switch as the output amplifier.



92CM-27159RI

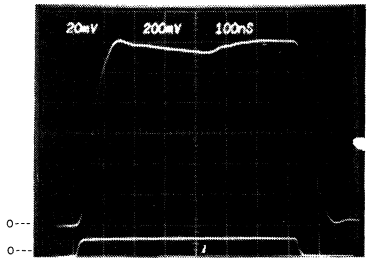
Fig.30 – Schematic diagram of the CA3080A in a sample-hold circuit with BiMos output amplifier.



TOP TRACE: OUTPUT—5 V/DIV. & 2 μs/DIV.
CENTER TRACE: DIFFERENTIAL COMPARISON OF INPUT & OUTPUT—2 mV/DIV. & 2 μs/DIV.
BOTTOM TRACE: INPUT—5 V/DIV. & 2 μs/DIV.

92CS-27161

Fig.31 – Large-signal response for circuit shown in Fig. 30.



TOP TRACE: OUTPUT — 20 mV/DIV. & 100 ns/DIV.
BOTTOM TRACE: INPUT—200 mV/DIV. & 100 ns/DIV.

92CS-27160

Fig.32 – Small-signal response for circuit shown in Fig. 30.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C = 500 μA, I_E = 0	–	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 500 μA, I_E = 0, I_B = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	16	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_C = 500 μA	–	5	6.9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 0.5 V, I_C = 30 mA	–	30	68	–	
		V_{CE} = 0.8 V, I_C = 50 mA	–	40	70	–	
Base-to-Emitter Saturation Voltage	$V_{BE\ sat}$	I_C = 30 mA, I_B = 1 mA	3	–	0.87	1.0	V
Collector-to-Emitter Saturation Voltage: CA3081, CA3082	$V_{CE\ sat}$	I_C = 30 mA, I_B = 1 mA	–	–	0.27	0.5	V
CA3081		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.7	
CA3082		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	1	μA

TYPICAL READ-OUT DRIVER APPLICATIONS

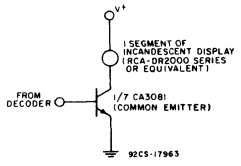


Fig.6—Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.

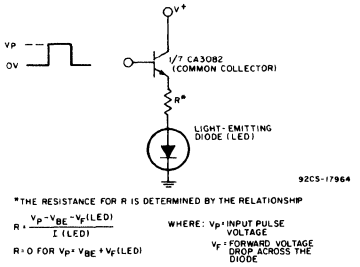


Fig.7—Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

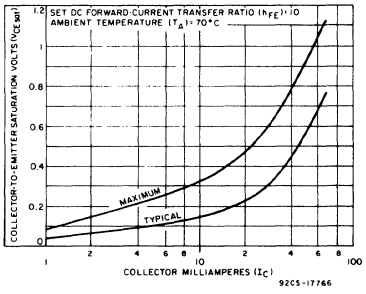


Fig.5 – V_{CEsat} vs I_C at 70°C

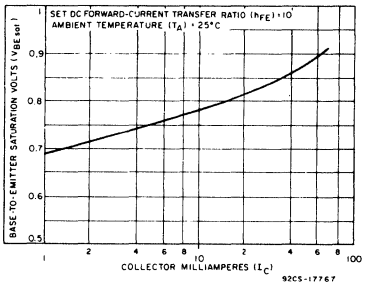


Fig.6 – V_{BEsat} vs I_C

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

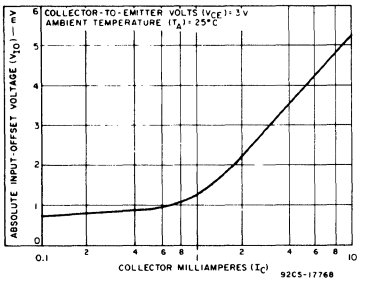


Fig.7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

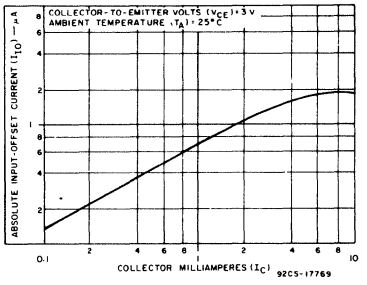


Fig.8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Characteristics Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-Cutoff Current	I_{CBO}	V_{CB} = −10V, I_E = 0	2	–	−0.055	−100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	3	–	−0.12	−100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_{CE} = −100μA, I_B = 0	–	−40	−70	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_{CB} = −100μA, I_E = 0	–	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_{EB} = −100μA, I_C = 0	–	−40	−100	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 100μA	–	40	100	–	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_E = 1mA, I_B = 100μA	4	–	−0.125	−0.25	V
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	5	−0.50	−0.59	−0.68	V
DC Forward-Current Transfer Ratio	h_{FE}	I_E = 100μA, V_{CE} = −10V	7	15	40	–	
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Magnitude of Input Offset Voltage	$\lvert V_{IO} \rvert$	I_E = 100μA, V_{CE} = −10V	8	–	0.422	6	mV
Input Offset Current	I_{IO}	I_E = 100μA, V_{CE} = −10V	–	−0.6	0	0.6	μA
For Transistors Q3 and Q4 (Current-Mirror Configuration):							
Collector Current (Normalized)	I_C/I_5	V_{CE} = −5V, V_{CIO} = −5V,	10	0.85	1.00	1.15	
Magnitude of Collector Current Ratio	$\lvert I_C(Q3)/I_C(Q4) \rvert$	Term. 13 = Gnd. I_5 = −100μA,	11	0.90	1.00	1.10	
For Transistors Q5 and Q6 (Darlington Configuration):							
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	–	–	–	−1.0	μA
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	13	0.92	1.07	1.20	V
DC Forward-Current Transfer Ratio	h_{FE}	I_E = 100μA, V_{CE} = −10V	15	100	1230	–	

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only For Design Guidance

Magnitude of Temperature Coefficient:							
V_{BE} (for each transistor)	$\lvert \Delta V_{BE}/\Delta T \rvert$	I_E = 100μA,	6		−1.78		mV/°C
V_{IO} (as a differential amplifier)	$\lvert \Delta V_{IO}/\Delta T \rvert$	V_{CE} = −10V	9		0.54		μV/°C
V_{BE} (Darlington configuration)	$\lvert \Delta V_{BE}/\Delta T \rvert$		14		−3.7		mV/°C
For Each Transistor:							
Input Resistance	R_I	f = 1kHz, V_{CE} = −10V,	19		9		kΩ
Output Resistance	R_O	I_C = −100μA	20	–	600	–	kΩ
Forward Transconductance	g_m		22	–	3	–	mmho
Collector-to-Base Capacitance	C_{CBO}	I_{CB} = 0	23	–	3.3	–	pF
Collector-to-Emitter Capacitance	C_{CEO}	I_{CE} = 0	23	–	2.5	–	pF
Base-to-Substrate Capacitance	C_{BIO}	I_{CIO} = 0	23	–	4.5	–	pF

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

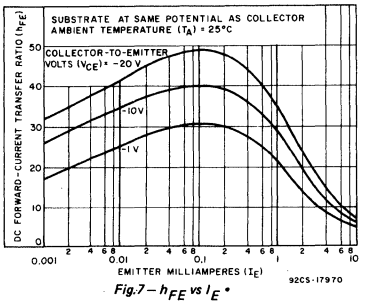


Fig.7 – h_{FE} vs I_E.

STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

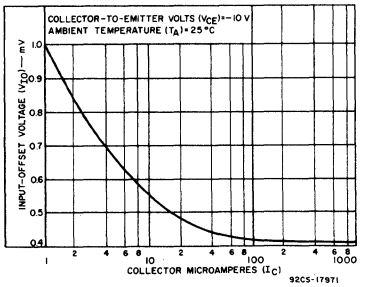


Fig.8—V_{IO} vs I_C, (transistors Q1 and Q2 as a differential amplifier).

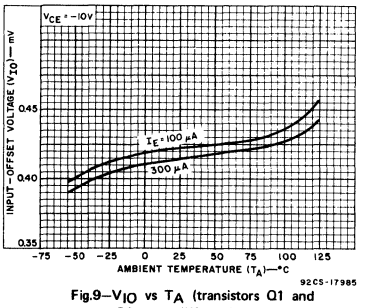


Fig.9—V_{IO} vs T_A (transistors Q1 and Q2 as a differential amplifier).

STATIC CHARACTERISTICS FOR CURRENT-MIRROR CONFIGURATION

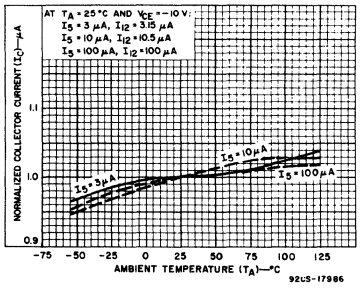


Fig.10—Normalized I_C vs T_A (transistors Q3 and Q4 in a current-mirror configuration.

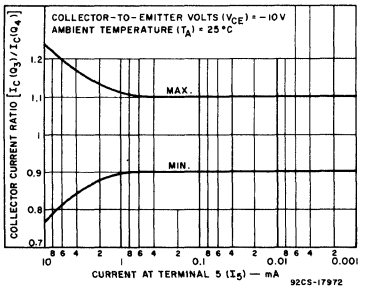


Fig.11—I_C ratio vs I_5 (transistors Q3 and Q4 in a current-mirror configuration.

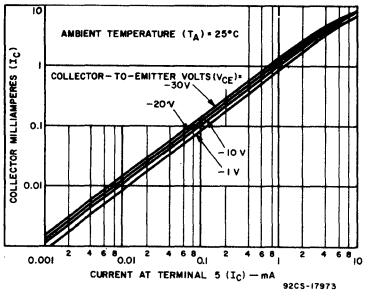


Fig.12 – I_C vs I_5 (transistors Q3 and Q4 in a current-mirror configuration).

Positive Voltage Regulators

For Regulated Voltages from 1.7 V to 46 V at Currents up to 100 mA

RCA-CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30 V (CA3085), 7.5 to 40 V (CA3085A), and 7.5 to 50 V (CA3085B) and a minimum regulated output voltage of 26 V (CA3085), 36 V (CA3085A), and 46 V (CA3085B).

The CA3085A is unilaterally interchangeable with the CA3055.

The CA3085 is available in a sealed-junction Beam-Lead version (CA3085L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

These types are supplied in the 8-lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8-lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS, CA3085BS). The CA3085 is also supplied in the 8-lead dual-in-line plastic package ("MINI-DIP", CA3085E), and in chip form (CA3085H).

Features

- **Up to 100 mA output current**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.025%**
- **Pin compatible with LM100 Series**
- **Adjustable output voltage**
- Low noise

Applications

- **Shunt voltage regulator**
- **Current regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Combination positive and negative voltage regulator**
- **Dual tracking regulator**
- See Application Note ICAN-6157 "Applications of the CA3085-Series Monolithic IC Voltage Regulators".

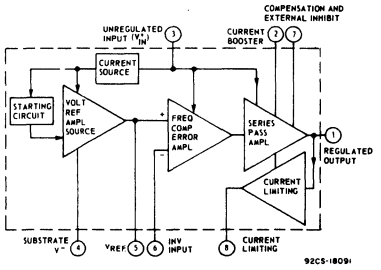


Fig. 1—Block diagram of CA3085 Series.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

POWER DISSIPATION: WITHOUT HEAT SINK	WITH HEAT SINK (TO-5 ONLY)
up to T_A = 55°C ..... 630 mW	up to T_C = 55°C .... 1.6 W
above T_A = 55°C derate linearly @6.67 mW/°C	above T_C = 55°C .... derate linearly at 16.7 mW/°C

TEMPERATURE RANGE:
Operating ..... −55 to +125°C
Storage ..... −65 to +150°C

UNREGULATED INPUT VOLTAGE:
CA3085 ..... 30 V
CA3085A ..... 40 V
CA3085B ..... 50 V

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

Maximum Voltage Ratings
The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	•	•	•	•	•	+10 0
6	–	–	•	•	•	•	•	•
7	–	–	–	+3 −10	+3 −10	•	•	+7 0
8	–	–	–	–	+5 −1	•	•	•
1	–	–	–	–	–	+10 −1	0 −1	+1 0
2	–	–	–	–	–	–	0 −1	+7 0
3	–	–	–	–	–	–	–	+1 0
4	–	–	–	–	–	–	–	Substrate & Case

* Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡ 30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

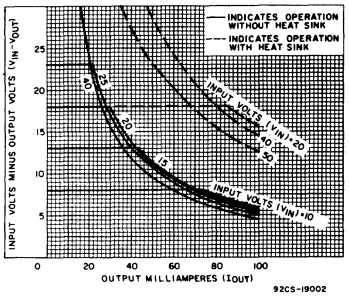


Fig. 3—Dissipation limitation ($V_{IN}-V_{OUT}$ vs. I_{OUT}).

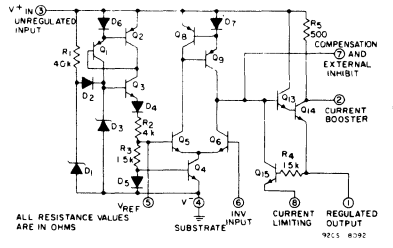


Fig. 2—Schematic diagram of CA3085 Series.

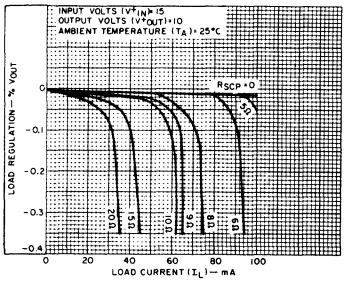


Fig. 4—Load regulation characteristics.

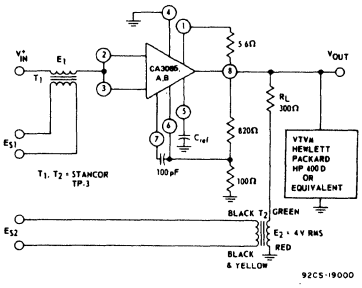


Fig.13– Test circuit for ripple rejection and output resistance.

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1kHz so that E_2 = 4V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}(R_L/E_2)$

Ripple Rejection – I

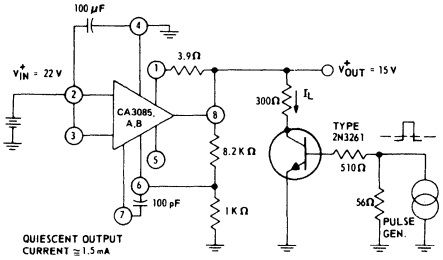
Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1kHz so that E_1 = 3V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection – II

Conditions

1. Repeat Ripple Rejection I with C_{REF} = 2 μF



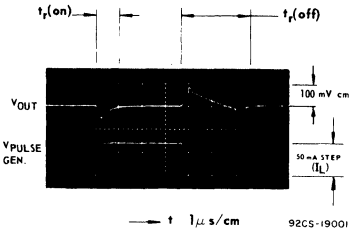
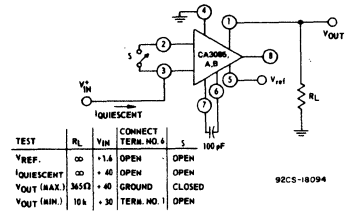
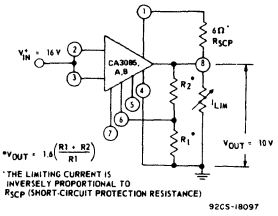


Fig.14– Turn-on and turn-off recovery time test circuit with associated waveforms.



TEST	R_L	V_{IN}	CONNECT TERM. NO. 6	S
V_{REF}	∞	+1.6	OPEN	OPEN
$I_{QUIESCENT}$	∞	+40	OPEN	OPEN
V_{OUT} (MAX.)	365Ω	+40	GROUND	CLOSED
V_{OUT} (MIN.)	10k	+30	TERM. NO. 1	OPEN

Fig.15– Test circuit for V_{REF}, $I_{quiescent}$, $V_{OUT(max.)}$, $V_{OUT(min.)}$.



*THE LIMITING CURRENT IS INVERSELY PROPORTIONAL TO R_{SCP} (SHORT-CIRCUIT PROTECTION RESISTANCE)

Fig.16– Test circuit for limiting current

TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES

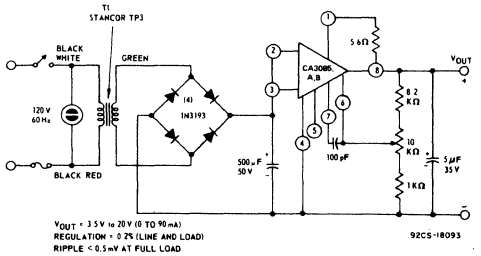
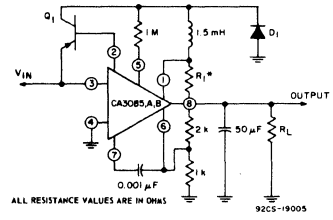


Fig.17– Application of the CA3085 Series in a typical power supply.



D1: RCA-1N1763A OR EQUIVALENT
Q1 RCA-2N5322 OR EQUIVALENT
*R1 = 0.7 I_L (MAX.)

Fig.18– Typical switching regulator circuit.

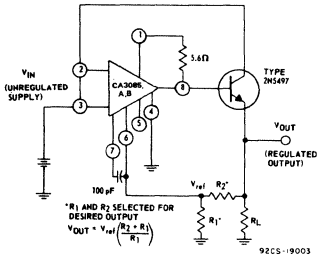


Fig.19– Typical high-current voltage regulator circuit.

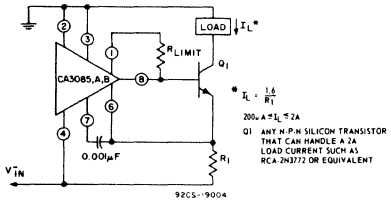
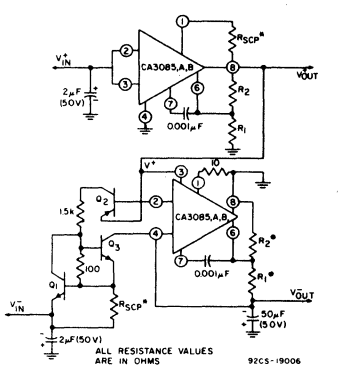


Fig.20– Typical current regulator circuit.



ALL RESISTANCE VALUES ARE IN OHMS

Q1 RCA 2N2102 OR EQUIVALENT
Q2 ANY P-N-P SILICON TRANSISTOR (RCA 2N5322 OR EQUIVALENT)
Q3 ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE THE DESIRED LOAD CURRENT (RCA-2N3772 OR EQUIVALENT)

*$V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)$
*R_{SCP} SHORT-CIRCUIT PROTECTION RESISTANCE

Fig.21– Combination positive and negative voltage regulator circuit.

ELECTRICAL CHARACTERISTICS at T_A = 25°C Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		–	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1kΩ		–	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	–
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8×10^{-4}	–
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 − j1.5	mmho
Input Admittance	Y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	Y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	Y_{re}			11	See Curve	–
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		–	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		–	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		—	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

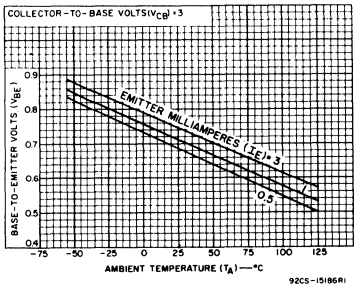


Fig.6 – V_{BE} vs T_A.

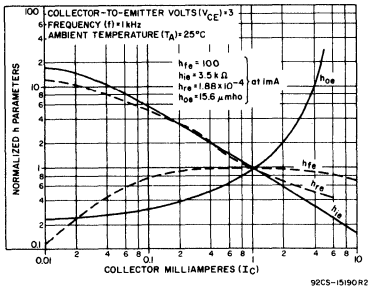


Fig.7 – Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

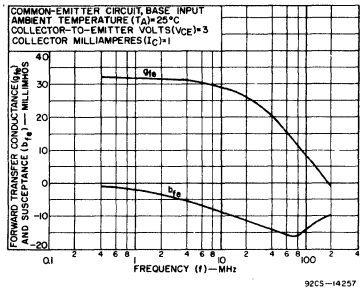


Fig.8 – y_{fe} vs f.

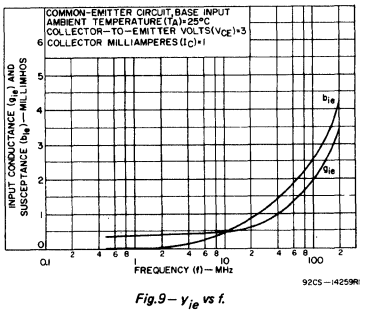


Fig.9 – y_{ie} vs f.

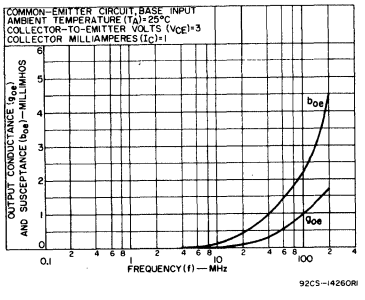


Fig.10 – y_{oe} vs f.

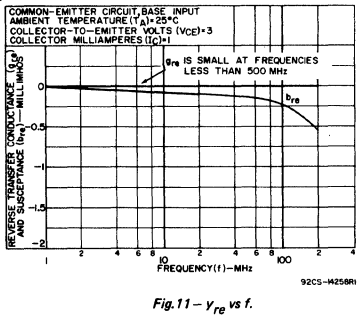


Fig.11 – y_{re} vs f.

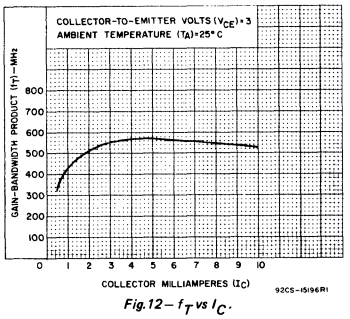


Fig.12 – f_T vs I_C.

ELECTRICAL CHARACTERISTICS, For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: T_A = 25°C, I_{IB} = 0.5 mA, V^+ = 15 V, V^- = -15 V	Circuit and/or Char. Curve	LIMITS: Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
INPUT CIRCUIT							
Input Balance (Correction) Currents:							
At x Input	I_{IC}	x = 0	–	-20	-2.1	+20	μA
At y Input		y = 0	–	-20	-8.7	+20	μA
Feedthrough Linearity Balance (Correction) Current	I_{OC}		–	-34	-2.9	+34	μA
OUTPUT CIRCUIT							
Output Offset Current	I_{OO}	x & y = 0,	–	-10	-0.23	+10	μA
Output Offset Voltage	V_{OO}	I_{OO} thru R_L = 33kΩ	–	-0.330	-0.0076	+0.330	V
Output Peak Current Swing	$\lvert I_O \rvert$	Thru R_L = 24kΩ	3	0.41	0.45	–	mA
Output Peak Voltage Swing	$\lvert V_O \rvert$	Across R_L = 33kΩ	4	12	12.9	–	V
DC SUPPLIES & BIASING							
Current Drain (Idling):							
At Term. 4		V^- = -15 V	–	–	2.9	4.5	mA
At Term. 12		V^+ = +15 V	–	–	2.0	3.0	mA
Reference Voltage	V_{ref}	Measured across Terms. 6 & 4 at I = 1mA	–	5.5	6.1	6.7	V
DYNAMIC CHARACTERISTICS							
Output Current	I_O	With I = 0.2mA at each input	–	–	0.21	0.32	mA
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$			11	0.69	1.0	1.7	
Accuracy		Worst case at 25°C	–	–	2.6	4.0	% of
Linearity				–	1.7	3.0	10 V
Feedthrough Voltage:							
At y = 20V p-p, x = 0			–	–	9	20	mV
At x = 20V p-p, y = 0			–	–	9	20	p-p

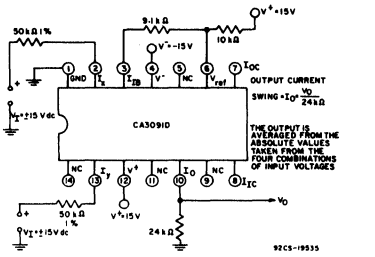


Fig.3—Test circuit for measurement of output current swing capability.

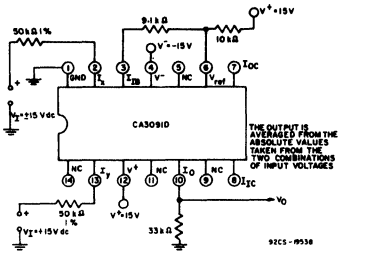


Fig.4—Test circuit for measurement of output voltage swing capability.

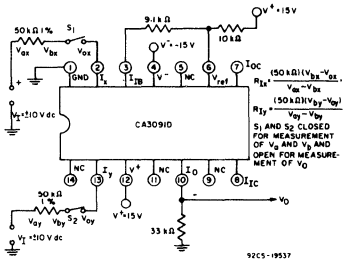


Fig.5—Test circuit for measurement of input resistance.

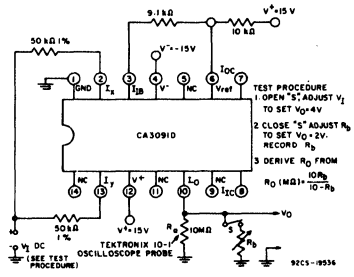


Fig.6—Test circuit for measurement of output resistance.

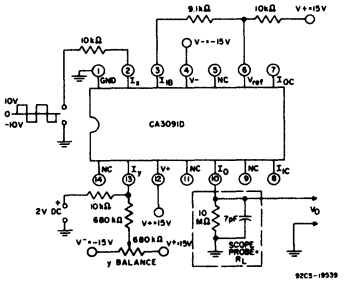


Fig.7—Test circuit for measurement of maximum slew rate.

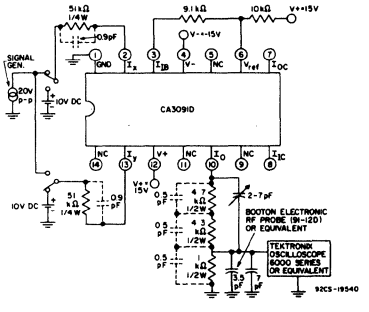


Fig.8—Test circuit for measurement of frequency response.

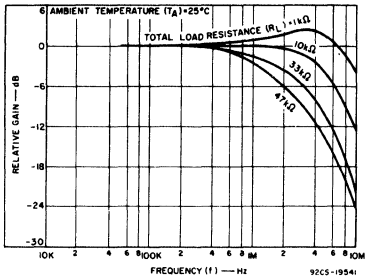
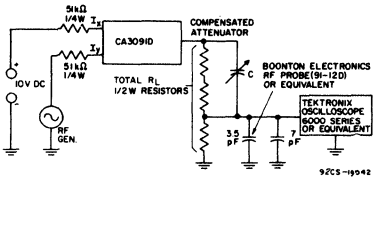


Fig.9- y-input frequency response characteristic curve with associated test circuit.



V_{ref}.
Temperature compensated zener connected to the −15 volt supply to provide a reference voltage as an aid in setting up a stable I_{IB}.

V_X, V_Y
The input voltages to be multiplied.

x-Balance Circuit
Sets the output to the zero level when the x-input is in the zero state.

y-Balance Circuit
Sets the output to the zero level when the y-input is in the zero state.

Accuracy
Accuracy defines the degree of error encountered in the operation of the multiplier. It is portrayed on a contour map by isomers (contour lines). Isomers with the highest values indicate "less-accurate" operation of the multiplier. (See illustrative Contour Map in Fig. 12.)

Contour Map
The contour map, shown in Fig. 12, is a graphical portrayal of the multiplier errors in the x, y input plane. Each contour line, termed "isomer", connects those points whose error values (in millivolts) are equal in magnitude. For example, a −20 mV contour line with points at V_X = 5V and V_Y = −3V indicates that the output voltage is 20 mV less than the theoretical output product (kV_XV_Y). This error voltage, presented in percent of full-scale input (±10 V), defines the "accuracy" of the device. Thus, a 20-mV error voltage represents an "accuracy" of 0.2% as derived from the equation:

$$\text{Accuracy} = \frac{20\ \text{mV}}{10} \times 100\% = 0.2\%.$$

A contour map provides a true indication of multiplier performance in each of the four quadrants. Each CA3091D is comprehensively tested and must provide the specified accuracy in the four quadrants.

Current Converter
This portion of the IC combines the multiplier's differential-amplifier output currents and converts them to a single-ended output current.

Current Sources
These circuits provide the biasing currents for the various circuits in the IC. The I_{IB} terminal provides the control current for the current-source circuit.

Feedthrough
Feedthrough occurs when an output signal is produced even though one of the input signals is zero. Consequently, feedthrough signal characteristics constitute a source of error in the operation of a multiplier. In the CA3091D, for example, the feedthrough signal output is specified to be less than 20 mV p-p when either terminal is set at 20 V p-p and the other terminal is set to zero.

I_{IB}
Circuit biasing control current.

I_{IC}
See I_{OC}.

I_O
Output product current ($k_I I_X I_Y = I_O$), where $k_I = kR_f^2 / R_L$

I_{OC}, I_{IC}
Compensatory input and output currents required to correct unlinearity along the x axis. (Optional for low-level signal use.)

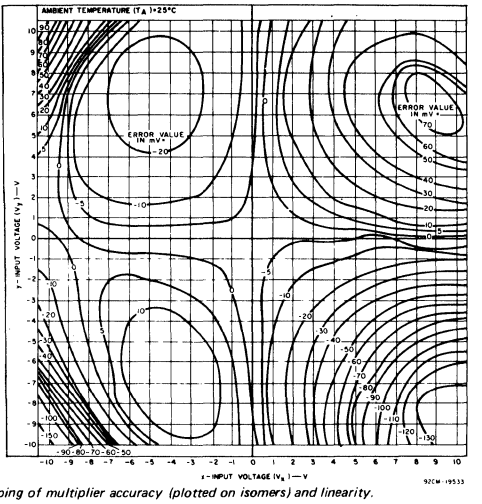
I_X, I_Y
Input currents to be multiplied.

k
Voltage Scale Factor (determines the gain of the multiplier).

k_I
Current Scale Factor (k_I) = $(R_f^2 / R_L)k$.

k adjust
Scale-Factor Adjustment.

Linearity
"Linearity" indicates the degree of multiplier error (i.e. deviation from "straight-line" characteristics) along each of the four boundaries of the input x, y field. These boundaries are formed when one input is held at one of the two maximum values (10 volts or −10 volts) and the other input is swept through the voltage range. (See Contour Map for additional information.)



Note: See "Contour Map" in "Symbols, Terms and Definitions" Section.

Fig.12—Contour mapping of multiplier accuracy (plotted on isomers) and linearity.

Linearity Adjust
An external circuit to provide vernier adjustment for optimum linearity. This control should be adjusted before adjusting the y-balance control.

Linearity Balance Circuit (Low-Level)
This circuit makes the multiplier's transfer function linear for low-level x-input signals.

Linearity Compensator
Internal circuitry that converts input current into a non-linear voltage, a requisite for producing a linear output in the differential amplifiers of the multiplier circuit.

Multiplier Circuitry
Provides the product of the two input voltages.

Multiplier Transfer Function
This function mathematically describes the interaction of the two inputs and the resulting output signal. The basic transfer function for a multiplier is

$$k(V_X + V_{Xe})(V_Y + V_{Ye}) = V_O + V_{Oe}$$

where: k = k factor and represents the basic gain of the multiplier

V_X, V_Y = the external inputs to be multiplied

V_O = the desired value of the product output signal

V_{Xe}, V_{Ye} = the "effective" errors that occur at the inputs of the multiplier and cause an output signal when either input is in a zero state.

V_{Oe} = the error voltage that develops at the output of the multiplier

DC correction factors are added to the multiplier inputs and output to compensate for the errors and offset variations. A complex linearity error term appears in the transfer function; however, this term is not included in the above equation for the purpose of clarity.

OPERATING CONSIDERATIONS

Operation of a Multiplier

A multiplier is, essentially, a gain-controlled amplifier (See Fig. 13) that multiplies the input signal (V_X) with the external gain controlling signal (V_Y) to produce the resultant output (V_O). The gain is externally adjustable by a coefficient (k). Stated simply, a multiplier produces an output voltage that is the linear product of two input voltages.

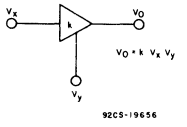
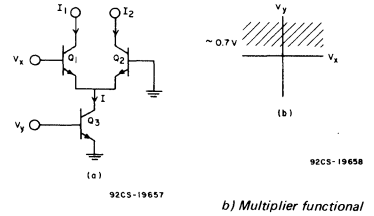


Fig.13—Gain-controlled amplifier.

The basic multiplier, shown in Fig. 14a, is a two-quadrant multiplier. The input signal (V_X) may have either a positive or negative polarity whereas, the external gain-controlling signal (V_Y) must be positive and greater than the base-to-emitter voltage (Fig. 14b). The output current ($I_1 - I_2$) of the differential amplifier, comprised of transistors Q1 and Q2, is related to both the input signal (V_X) and the current source (I). Since the current source (I) is related to the gain controlling signal (V_Y) the output current ($I_1 - I_2$), therefore, is related to both V_X and V_Y.



a) Basic circuit.

b) Multiplier functional only in shaded region.

Fig.14—Two-quadrant multiplier.

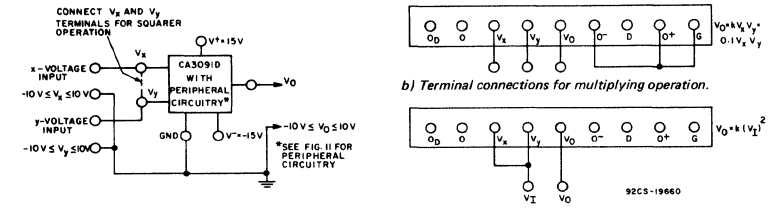
This relationship is essentially non-linear; thus an appropriate linearization circuit must be provided in the input stage to achieve the following linear relationship:

$$I_1 - I_2 = k' V_X V_Y \qquad \text{(Eq. 1)}$$

where k' is a constant

Table II — Divider Alignment Procedure

Step No.	Set V_z V	Set V_y V	Measure	Output Coupling	Test Equipment Used	Adjust	Notes
1	–	–	–	–	–	–	Set all potentiometers to center of range.
2	0	V_S	V_O	ac	ac – VM	O_{zero}	Adjust for minimum reading.
3	0	10V dc	V_O	dc	dc – VM	$x_{balance}$	Adjust for OV dc output.
4	V_S	V_S	V_O	ac	ac – VM	$y_{balance}$	* Adjust for minimum reading.
5	5V dc	5V dc	V_O	dc	dc – VM	k_{adjust}	Adjust for 10 V dc output.



a) Circuit arrangement for multiplier or squarer operation.

b) Terminal connections for multiplying operation.

c) Terminal connections for squarer operation.

Fig.18—Multifunction circuit-board arrangement with terminal connections for multiplier and squarer operation.

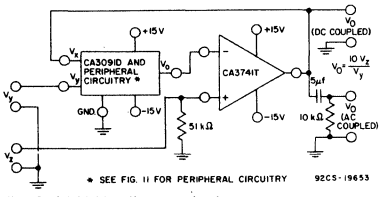


Fig.19—(a) Divider alignment circuit.

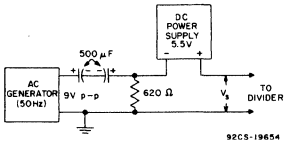
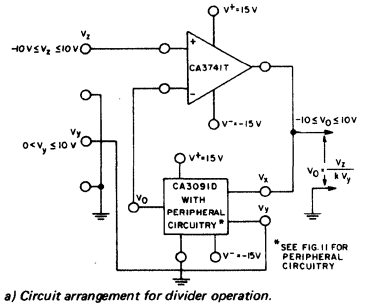
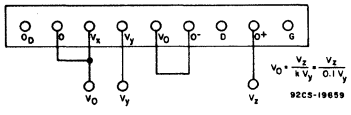


Fig.19—(b) Circuit to provide offset ac signal for use in divider alignment procedure.

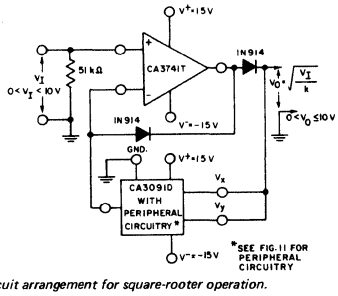


a) Circuit arrangement for divider operation.

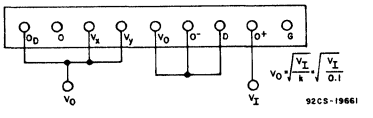


b) Terminal connections for divider operation.

Fig.20—Multifunction circuit-board arrangement with terminal connections for divider operation.



a) Circuit arrangement for square-rooter operation.



b) Terminal connections for square-rooter operation.

Fig.21—Multifunction circuit-board arrangement with terminal connections for square-rooter operation.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	5.5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	1	μA
DC Forward Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	40	76	–	
		V_{CE} = 3V, I_C = 50mA	40	75	–	
Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	–	0.40	0.70	V
Forward Base-to-Emitter Temp. Coefficient	$\Delta V_{BE}/\Delta T$	I_E = 10mA	–	-1.9	–	mV/°C
For Transistors Q1 and Q2 (As a Differential Amplifier):						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		–	0.7	2.5	μA
Temp. Coefficient of Offset Voltage	$\lvert\Delta V_{IO}/\Delta T\rvert$	–	–	5	–	μV/°C
For Each Zener Diode						
Zener Voltage	V_Z	I_Z = 10mA	6.3	7	7.7	V
Zener Impedance	z_Z	I_Z = 10mA, f = 1 kHz	–	15	25	Ω
Zener Reverse Current	I_{ZR}	V_Z = +5V	–	–	1	μA
Zener Voltage Temp. Coefficient	$\Delta V_Z/\Delta T$	I_Z = 10mA	– i.e.	+3.6 +.05	–	mV/°C %/°C
Zener-to-Substrate Breakdown Voltage	$V_{(BR)ZIO}$	I_Z = 100μA (Terminals 7 & 9)	20	60	–	V
Dissipation		Refer to Example in Application "a"	–	–	250	mW
For Diode (D1)						
Diode Forward Voltage	V_{DF}	I_C = 10mA, V_{CE} = 3V	0.65	0.74	0.85	V
Diode Forward Current	I_{DF}		–	–	50	mA
Diode Reverse-Breakdown Voltage	$V_{(BR)DR}$	I_{DR} = 500μA	5.5	6.9	–	V
Diode-to-Substrate Breakdown Voltage	$V_{(BR)DIO}$	I_{Diode} = 100μA (Terminal 10)	20	60	–	V
Diode Forward-Voltage Temp. Coefficient	$\Delta V_{DF}/\Delta T$	I_{DF} = 5mA	–	-1.9	–	mV/°C

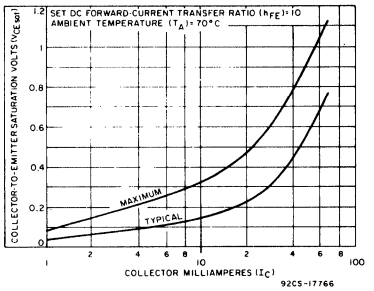


Fig. 5 – V_{CEsat} vs I_C at 70°C

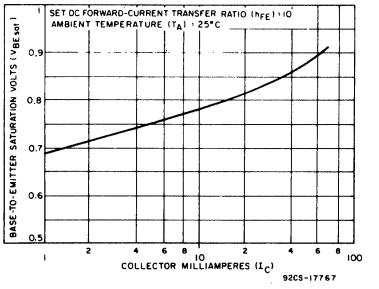


Fig. 6 – V_{BEsat} vs I_C

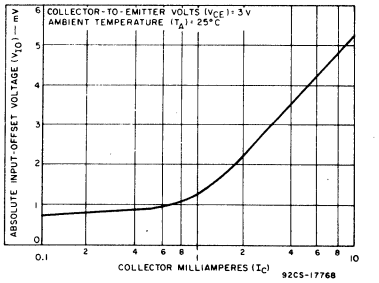


Fig. 7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

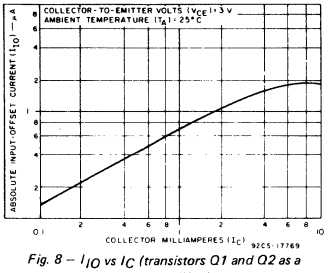


Fig. 8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier)

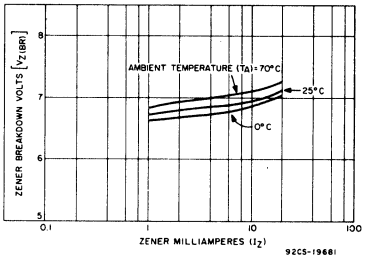


Fig. 9 – Typical Zener breakdown voltage vs current

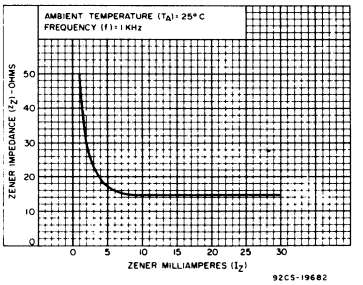


Fig. 10 – Typical Zener impedance vs current

Programmable Power Switch/Amplifier

For Control & General-Purpose Applications

CA3094T,S,E: For Operation Up to 24 Volts
CA3094AT,S,E: For Operation Up to 36 Volts
CA3094BT,S: For Operation Up to 44 Volts

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100 mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transistors. The CA3094 has the generic characteristics of the RCA-CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100 mA.

The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100 μA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).

The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs.28,29 and 30 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), and in chip form ("H" suffix).

Features:

- **Designed for *single* or dual power supply**
- **Programmable: strobing, gating, squelching, AGC capabilities**
- **Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)**
- **High-power, single-ended class A amplifier will deliver power output of 0.6 watt (1.6 W device dissipation)**
- **Total harmonic distortion (THD) @ 0.6 W in class A operation — 1.4% typ.**
- **High current-handling capability — 100 mA (avg.), 300 mA (peak)**
- **Sensitivity controlled by varying bias current**
- **Output: "sink" or "drive" capability**

Applications:

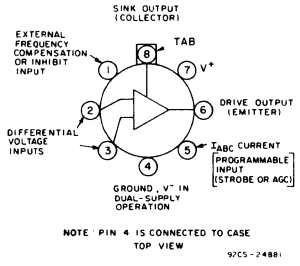
- **Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor**
- **Over-current, over-voltage, over-temperature protectors**
- **Dual-tracking power supply with RCA-CA3085**
- **Wide-frequency-range oscillator ■ Analog timer**
- **Level detector ■ Alarm systems ■ Voltage follower**
- **Ramp-voltage generator ■ High-power comparator**
- **Ground-fault interrupter (GFI) circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

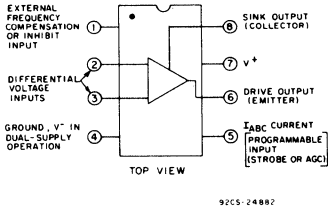
	CA3094	CA3094A	CA3094B	
DC SUPPLY VOLTAGE:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC DIFFERENTIAL INPUT VOLTAGE (Terminals 2 and 3)	± 5*			V
DC COMMON-MODE INPUT VOLTAGE	Term. 4 ≤ Term. 2 & 3 ≤ Term. 7			
PEAK INPUT SIGNAL CURRENT (Terminals 2 and 3)	± 1			mA
PEAK AMPLIFIER BIAS CURRENT (Terminal 5)	2			mA
OUTPUT CURRENT:				
Peak	300			mA
Average	100			mA
DEVICE DISSIPATION:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
THERMAL RESISTANCE (Junction to Air)	140			°C/W
AMBIENT TEMPERATURE RANGE:				
Operating	−55 to +125			°C
Storage	−65 to +150			°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

FUNCTIONAL DIAGRAMS



TO-5 Style Package



Plastic Package

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Min.	Typ.	Max.	
OUTPUT PARAMETERS (Differential Input Voltage = 1V)					
Peak Output Voltage: (Terminal No. 6) With Q13 "ON" V^+OM With Q13 "OFF" $V-OM$	V^+ = 30 V R_L = 2 kΩ to ground	26 –	27 0.01	– 0.05	V V
Peak Output Voltage: (Terminal No. 6) Positive V^+OM Negative $V-OM$	V^+ = +15 V, V^- = -15 V R_L = 2 kΩ to −15 V	+11 –	+12 −14.99	0.5 – −14.95	V V
Peak Output Voltage: (Terminal No. 8) With Q13 "ON" V^+OM With Q13 "OFF" $V-OM$	V^+ = 30 V R_L = 2 kΩ to 30 V	29.95 –	29.99 0.040	– –	V V
Peak Output Voltage: (Terminal No. 8) Positive V^+OM Negative $V-OM$	V^+ = 15 V, V^- = − 15 V R_L = 2 kΩ to + 15 V	+14.95 –	+14.99 14.96	– –	V V
Collector-to-Emitter Saturation Voltage (Terminal No. 8) $V_{CE(sat)}$	V^+ = 30 V I_C = 50 mA Terminal No.6 grounded	–	0.17	0.80	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)	V^+ = 30 V	–	2	10	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13}) h_{fe}	V^+ = 30 V V_{CE} = 5 V I_C = 50 mA	16,000	100,000	–	
Output Capacitance: Terminal No. 6 C_O Terminal No. 8	f = 1 MHz All Remaining Terminals Tied to Terminal No. 4	– –	5.5 17	– –	pF pF
TRANSFER PARAMETERS					
Voltage Gain A	V^+ = 30 V I_{ABC} = 100 μA ΔV_{out} = 20 V R_L = 2 kΩ	20,000 86	100,000 100	– –	V/V dB
Forward Transconductance To Terminal No. 1 g_m		1650	2200	2750	μmhos
Slew Rate: Open Loop: Positive Slope Negative Slope	I_{ABC} = 500 μA R_L = 2 kΩ	– –	500 50	– –	V/μs V/μs
Unity Gain (Non-Inverting, Compensated)	I_{ABC} = 500 μA R_L = 2 kΩ	–	0.7	–	V/μs

TYPICAL CHARACTERISTICS CURVES (Cont'd)

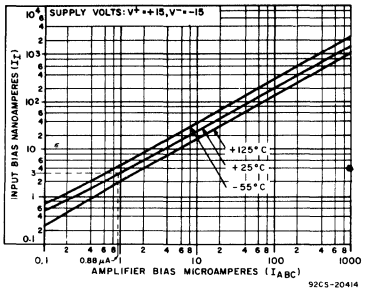


Fig.4 – Input bias current vs. amplifier bias current (I_{ABC}, terminal No.5).

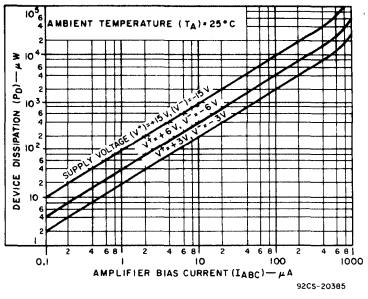


Fig.5 – Device dissipation vs. amplifier bias current (I_{ABC}, terminal No.5).

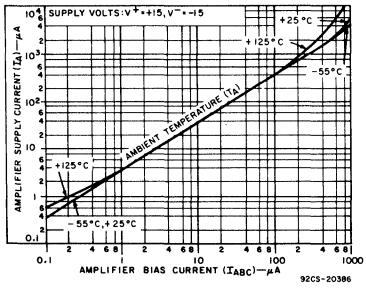


Fig.6 – Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No.5).

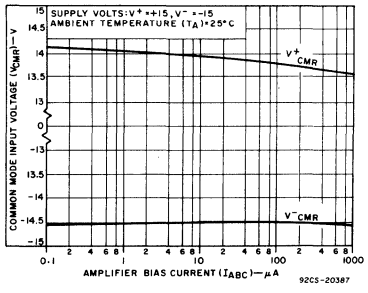


Fig.7 – Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

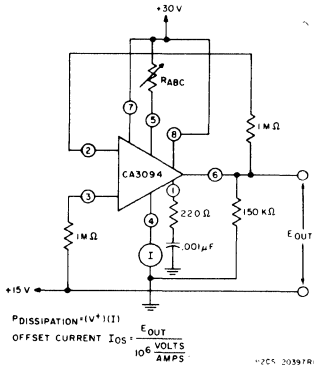


Fig. 18 – Input offset current test circuit.

TEST CIRCUITS (Cont'd)

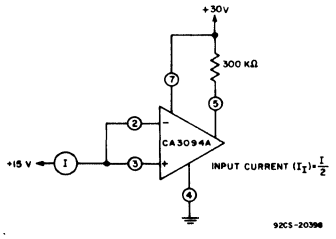


Fig. 19 – Input bias current test circuit.

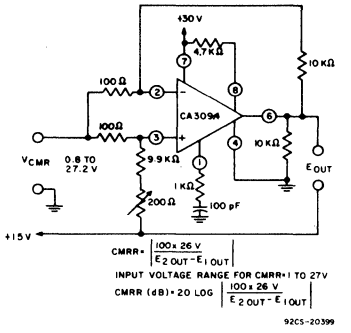
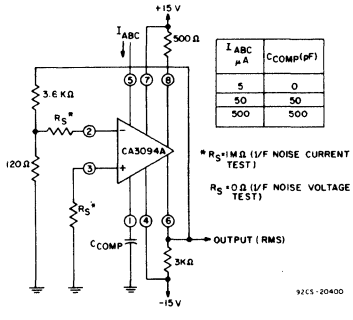
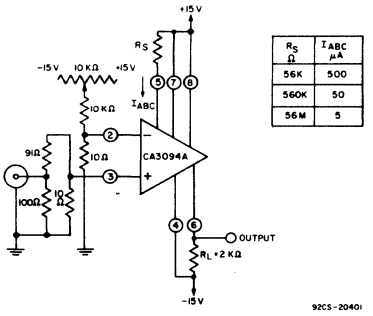


Fig. 20 – Common-mode range and rejection ratio test circuit.



IABC μA	CCOMP (pF)
5	0
50	50
500	500

Fig. 21 – I/F noise test circuit.



RS Ω	IABC μA
56K	500
560K	50
56M	5

Fig. 22 – Open-loop gain vs frequency test circuit.

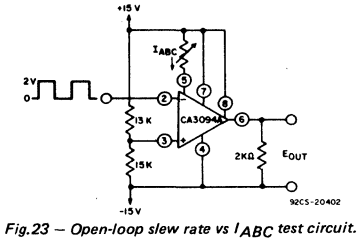


Fig. 23 – Open-loop slew rate vs I_{ABC} test circuit.

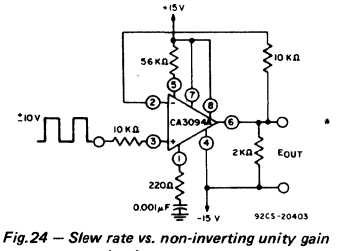
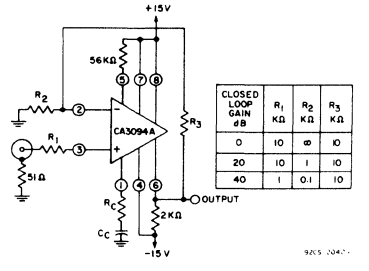


Fig. 24 – Slew rate vs. non-inverting unity gain test circuit.



CLOSED LOOP GAIN dB	R1 KΩ	R2 KΩ	R3 KΩ
0	10	∞	10
20	10	1	10
40	1	0.1	10

Fig. 25 – Phase compensation test circuit.

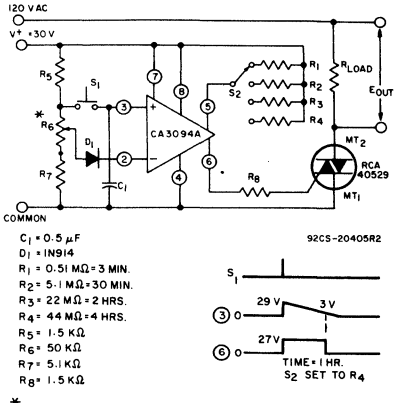


Fig. 26 – Presettable analog timer.

TYPICAL APPLICATIONS

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/ Switch Amplifier IC".

Design Considerations

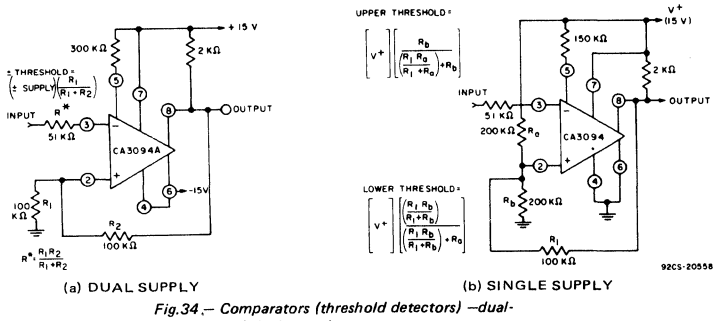
The selection of the optimum amplifier bias current (I_{ABC}) depends on –

1. The Desired Sensitivity – the higher the I_{ABC}, the higher the sensitivity – i.e., a greater-drive current capability at the output for a specific voltage change at the input.
2. Required Input Resistance – the lower the I_{ABC}, the higher the input resistance.

If the desired sensitivity and requred input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100 μA, since the CA3094 is characterized at this value of amplifier bias current.

The CA3094 is extremely versatile and can be used in a wide variety of applications.

TYPICAL APPLICATIONS (Cont'd)



(a) DUAL SUPPLY (b) SINGLE SUPPLY

Fig.34 – Comparators (threshold detectors) –dual- and single-supply types.

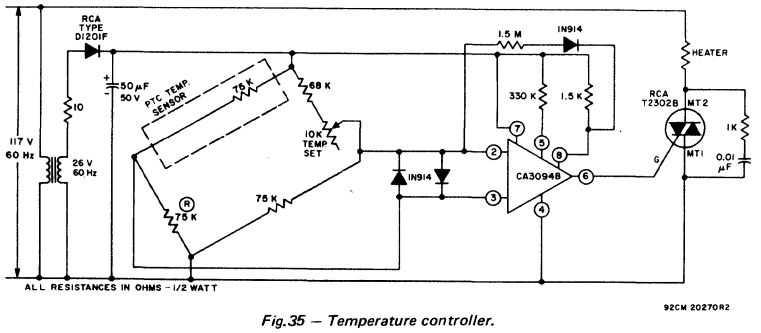


Fig.35 – Temperature controller.

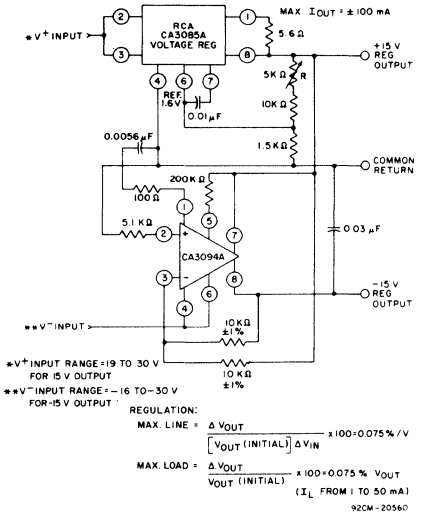


Fig.36 – Dual-voltage tracking regulator.

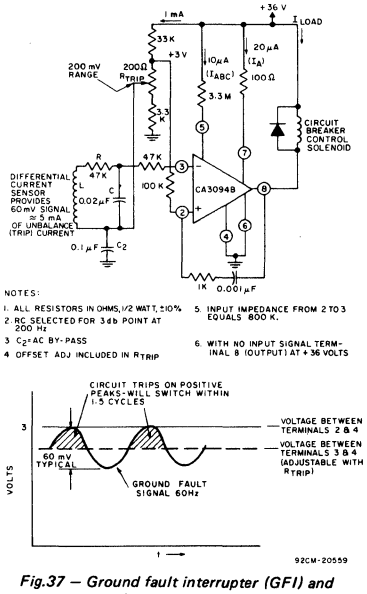


Fig.37 – Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.

Super-Beta Transistor Array

Differential Cascode Amplifier Plus 3 Independent Transistors

RCA-CA3095E is a monolithic array of transistors connected as a super-beta differential cascode amplifier with three independent n-p-n transistors. (Refer to Fig. 1 for following description.)

The differential cascode amplifier incorporates two cascode amplifiers consisting of transistors Q1, Q3 and Q2, Q4, respectively, plus a voltage-limiting circuit, consisting of diodes D1, D2 and p-n-p transistor Q5. Two of these transistors, Q1 and Q2, are super-beta types that have an $h_{FE} > 1000$ and are capable of operating over a wide current range of 1 μA to 2 mA. Each of these types comprises the input section of its respective cascode amplifier. The output section of each cascode amplifier employs a conventional n-p-n transistor, Q3, Q4, respectively. The output signal is obtained at the collectors of these transistors. See Operating Considerations for bias considerations of the differential cascode amplifier.

The exceptionally high-beta characteristics of Q1 and Q2, plus the large signal-voltage swing capability of Q3 and Q4, make the composite differential cascode amplifier an excellent choice for a broad range of small-signal, high-input-impedance amplifier applications including low-noise video amplifiers. This amplifier is also recommended for use in long-interval timers, oscillators, and long-duration one-shot applications.

The independent transistors, Q6, Q7 and Q8, are high-voltage silicon n-p-n conventional types for general use in signal processing systems in the frequency range from dc through vhf. Separate terminals for each of these transistors permit maximum flexibility in circuit design.

The CA3095E is supplied in a 16-lead dual-in-line plastic package and operates over the ambient temperature range of −55°C to +125°C

Features

- Two super-beta n-p-n transistors – $h_{FE} > 1000$
- Voltage-limiting circuitry (D1, D2, Q5)
- Operation possible at I_{IB} down to < 1 nA
- Matched pair (Q1 and Q2) –
  V_{IO} = 5 mV max. at I_C = 100 μA dc
  I_{IO} = 20 nA max. at I_C = 100 μA dc
- Wide current range – < 1 μA to 2 mA

Independent Transistors:

- h_{FE} = 300 typ. for each transistor
- Wide current range – < 1 μA to 10 mA
- Matched general-purpose transistors
- High voltage – V_{CBO} = 45 V max.

Applications

Differential Cascode Amplifier:

- Super-beta pre-amplifier for op-amp
- High-impedance dc meter amplifier
- Low-noise video amplifier
- Piezoelectric transducer amplifier
- Long-interval timer
- Long-duration one-shot multivibrator
- Comparator with high-input impedance
- Long-time-constant integrator
- Photocell amplifier
- Low-noise amplifier—for operation from high-source impedances

Independent Transistors:

- General use in signal processing systems in dc through vhf range

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25 °C*

Power Dissipation:		
Any One Transistor	300	mW
Total Package–		
Up to 25 °C	750	mW
Above 25 °C ..... derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−55 to +150	°C
Lead Temperature (During Soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C
Voltage and Current Ratings Apply for Each Specified Transistor:		
Super-Beta Transistors (Q1, Q2)–		
Collector-to-Base Voltage (V_{CBO})	6	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional N-P-N Transistors (Q3, Q4, Q6, Q7, Q8)–		
Collector-to-Base Voltage (V_{CBO})	45	V
Collector-to-Emitter Voltage (V_{CEO})	35	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional P-N-P Transistor (Q5)–		
Collector-to-Base Voltage (V_{CBO})	−45	V
Collector-to-Emitter Voltage (V_{CEO})	−35	V
Limiting Circuit Current ($I_{Pin\ 11}$)	20	mA

* The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

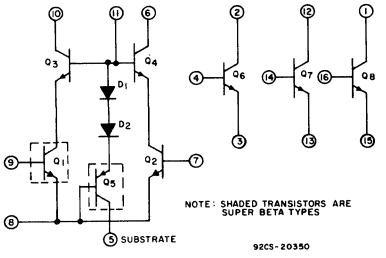


Fig. 1–Functional diagram.

STATIC CHARACTERISTICS

Characteristics	Symbol	Test Conditions (T_A = 25 °C)		Limits Min.	Limits Typ.	Limits Max.	Units
Characteristics Apply for Each Super-Beta Cascode Amplifier Transistor Pair (Q1, Q3) and (Q2, Q4), Unless Indicated Otherwise							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0 See Note 1		6	–	–	V
Emitter-to-Base Breakdown Voltage (Applies only to Q1 & Q2)	$V_{(BR)EBO}$	I_E = 100 μA, I_C = 0 Term. 9 to 8 or Term. 7 to 8		6	8		V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100 μA, I_B = I_E = 0		45	–	–	V
Collector Cutoff Current	I_{CER}	V_{6-8} or V_{10-8} = 10 V, I_{11} = 100 μA R_{BE} = 100 MΩ			–	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{10-8} = 5 V or V_{6-8} = 5 V	I_C = 1 mA	–	1500	–	
			I_C = 100 μA	1000	2000	5000	
			I_C = 10 μA	–	1500	–	
Base-to-Emitter Voltage (Applies only to Q1 & Q2)	V_{BE}	I_C = 100 μA, V_{6-8} or V_{10-8} = 5 V		0.50	0.59	0.68	V
Saturation Voltage	V_{sat}	I_6 or I_{10} = 1 mA, I_{11} = 100 μA, I_7 or I_9 = 100 μA		–	0.22	0.7	V
For Cascode Amplifiers as a Differential Matched Pair							
Magnitude of Input-Offset Voltage	$\lvert I_{IO} \rvert$	I_C = 100 μA		–	1	5	mV
Magnitude of Input-Offset Current	$\lvert I_{IO} \rvert$	V_{6-8} = V_{10-8} = 5 V		–	4	20	nA
Magnitude of Input-Offset Voltage Drift (Temp. Coeff.)	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$			–	3.3	–	μV/°C
Magnitude of Input-Offset Current Drift (Temp. Coeff.)	$\frac{\lvert \Delta I_{IO} \rvert}{\Delta T}$			–	0.05	–	nA/°C

Note 1: Terminal No. 9 to terminals 10 and 11 connected or terminal No. 7 to terminals 6 and 11 connected.

Test Circuits for Measurement of Super-Beta Cascode Amplifier Characteristics

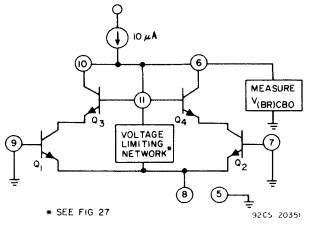


Fig. 2–$V_{(BR)CBO}$ test circuit.

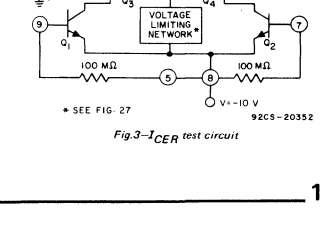


Fig. 3–I_{CER} test circuit

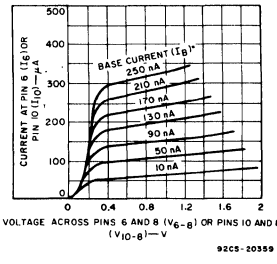


Fig.10—I-V characteristics for the super-beta cascode pairs.

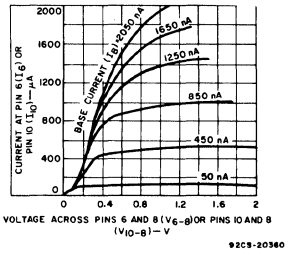


Fig.11—I-V characteristics for the super-beta cascode pairs.

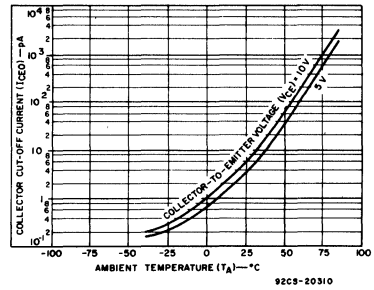


Fig.12—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CE} = 5 V, 10 V).

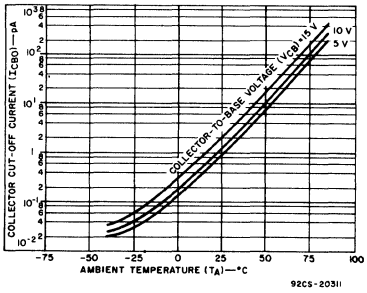


Fig.13—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CB} = 5 V, 10 V, 15 V).

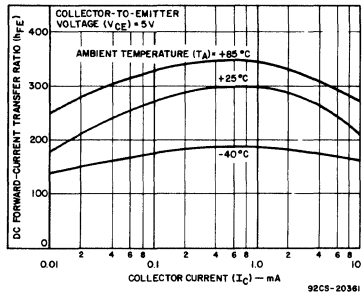


Fig.14—h_{FE} vs. I_C for each conventional transistor (Q6, Q7, Q8).

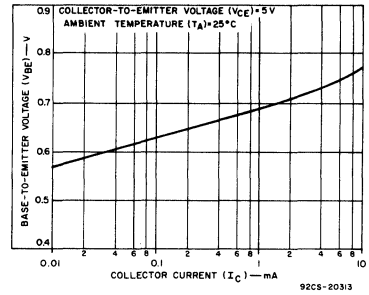


Fig.15—V_{BE} as a function of collector current for the conventional transistors.

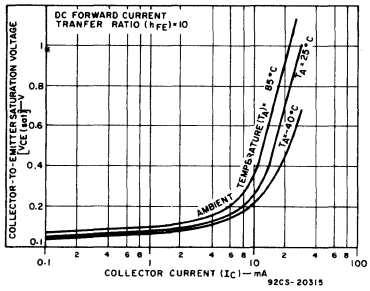


Fig.16—$V_{CE(sat)}$ as a function of collector current for the conventional transistors.

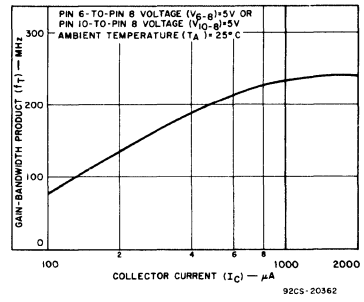


Fig.17—Gain bandwidth product vs collector current for the super-beta cascode pairs.

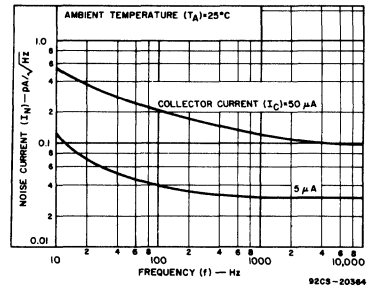


Fig.18—I_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

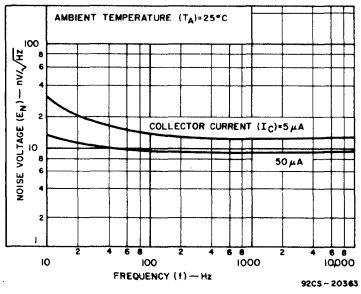


Fig.19—E_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

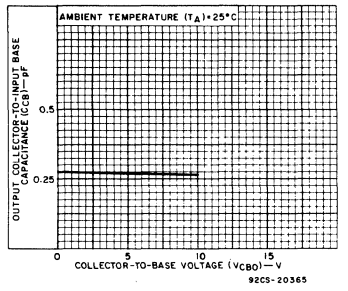


Fig.20—C_{CB} vs. V_{CBO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

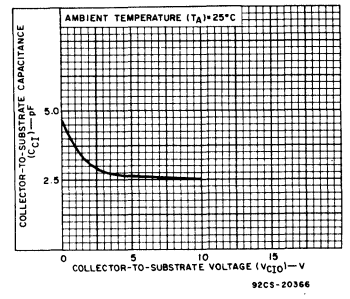


Fig.21—C_{CI} vs. V_{CIO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

TYPICAL APPLICATIONS (Cont'd)

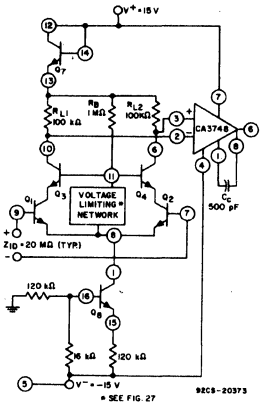


Fig.29—Super-beta Op-Amp with resistor drive network.

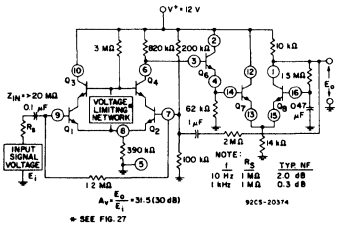


Fig.30—High-input-impedance, low-noise amplifier circuit.

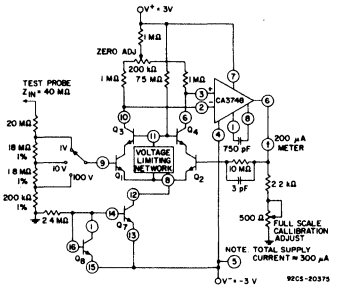


Fig.31—Typical high-input-impedance dc voltmeter circuit.

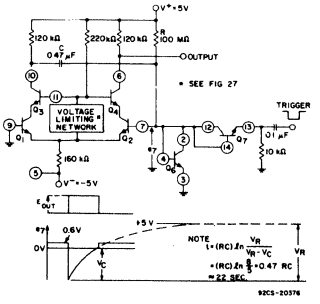


Fig.32—Long-delay monostable multivibrator circuit.

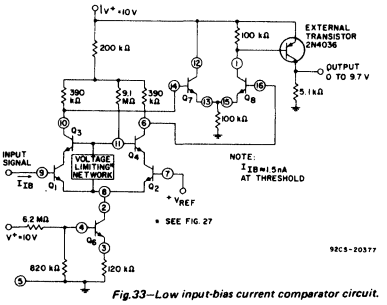


Fig.33—Low input-bias current comparator circuit.

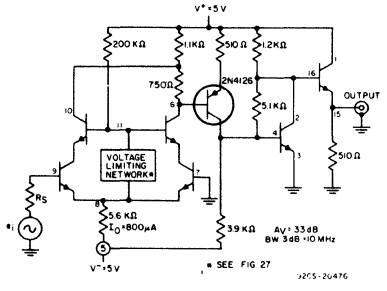


Fig.34—CA3095E wideband amplifier.

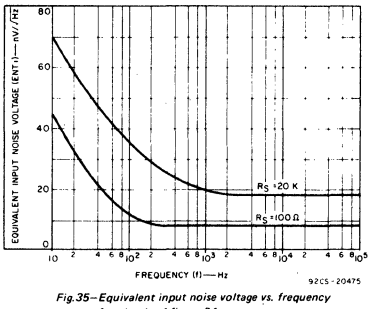


Fig.35—Equivalent input noise voltage vs. frequency for circuit of figure 34.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each n-p-n Transistor											
I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.001	40	–	0.001	100	–	0.001	100	nA
I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.006	100	–	0.006	1000	–	0.006	1000	nA
$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	35	50	–	35	50	–	24	35	–	V
$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	45	100	–	45	100	–	30	80	–	V
$V_{(BR)CIO}$	I_{CI} = 10 μA, $I_B = I_E$ = 0	45	100	–	45	100	–	30	80	–	V
$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	6	8	–	6	8	–	6	8	–	V
V_Z	I_Z = 10 μA	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA	–	0.24	0.5	–	0.24	0.7	–	0.24	0.7	V
V_{BE}	I_C = 1 mA, V_{CE} = 5 V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE}		150	390	500	150	390	500	100	390	670	
$\lvert\Delta V_{BE}/\Delta T\rvert$	I_C = 1 mA, V_{CE} = 5 V	–	1.9	–	–	1.9	–	–	1.9	–	mV/°C

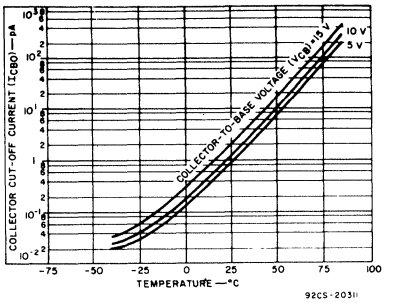


Fig. 3 – Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

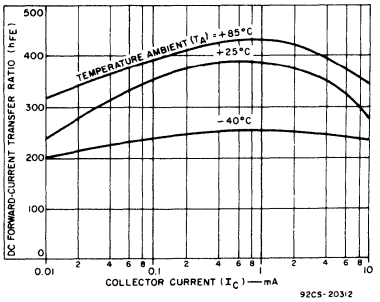


Fig. 4 – Transistor (n-p-n) h_{FE} as a function of collector current.

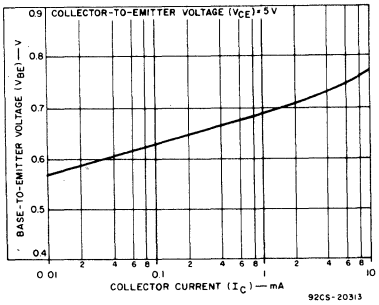


Fig. 5 – V_{BE} (n-p-n) as a function of collector current.

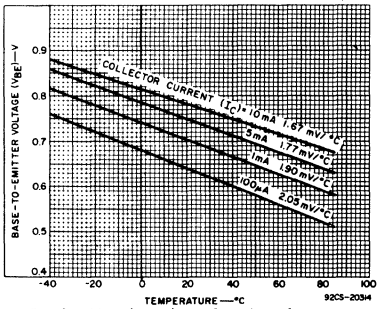


Fig. 6 – V_{BE} (n-p-n) as a function of temperature.

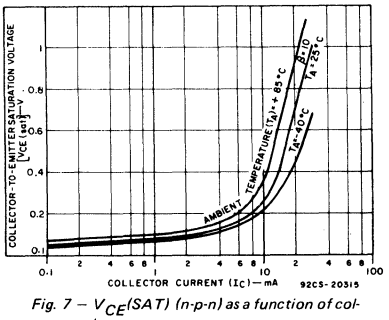


Fig. 7 – V_{CE}(SAT) (n-p-n) as a function of collector current.

DYNAMIC

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Typical Values Intended Only for Design Guidance

CHARACTERISTICS	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, V_{CE} = 5 V, I_C = 1 mA, R_S = 1 kΩ	2.2	dB
Low-Frequency, Input Resistance, R_i	f = 1.0 kHz, V_{CE} = 5 V, I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance, R_o		80	kΩ
Admittance Characteristics:	f = 1 MHz, V_{CE} = 5 V, I_C = 1 mA		
Forward Transfer Admittance, $\frac{g_{fe}}{Y_{fe}\ b_{fe}}$		7.5 −j13	mmho
Input Admittance, $\frac{g_{ie}}{Y_{ie}\ b_{ie}}$		2.2 j3.1	mmho
Output Admittance, $\frac{g_{oe}}{Y_{oe}\ b_{oe}}$		0.76 j2.4	mmho
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 1.0 mA	280	MHz
	V_{CE} = 5 V, I_C = 5 mA	335	
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = 3 V	0.75	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = 3 V	0.46	pF
Collector-to-Substrate Capacitance, C_{CI}	V_{CI} = 3 V	3.2	pF
For Each p-n-p Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, I_C = 100 μA, R_S = 1 kΩ	3	dB
Low-Frequency Input Resistance, R_i	f = 1 kHz, V_{CE} = 5 V, I_C = 100 μA	27	kΩ
Low-Frequency Output Resistance, R_o		680	kΩ
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 100 μA	6.8	MHz
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = −3 V	0.85	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = −3 V	2.25	pF
Base-to-Substrate Capacitance, C_{BI}	V_{BI} = 3 V	3.05	pF

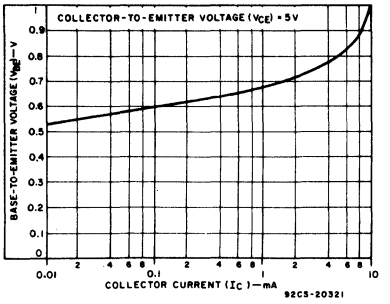


Fig. 12 – V_{BE} (p-n-p) as a function of collector current.

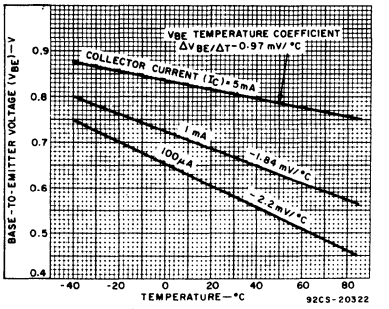


Fig. 13 – V_{BE} (p-n-p) as a function of temperature.

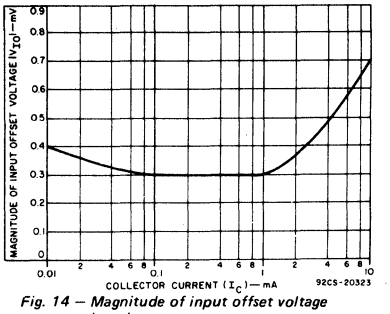


Fig. 14 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor Q_1–Q_2.

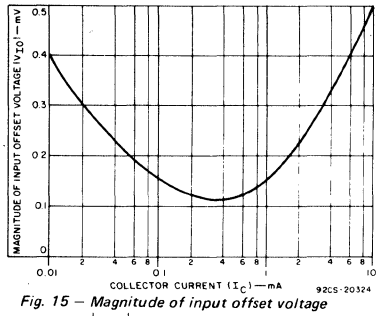


Fig. 15 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistor Q_4–Q_5.

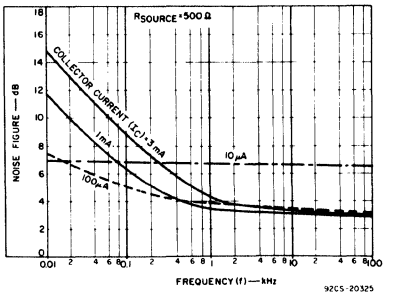


Fig. 16 – Noise figure as a function of frequency for n-p-n transistors.

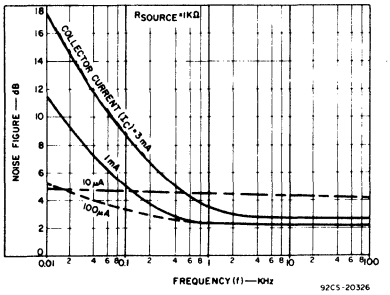


Fig. 17 – Noise figure as a function of frequency for n-p-n transistors.

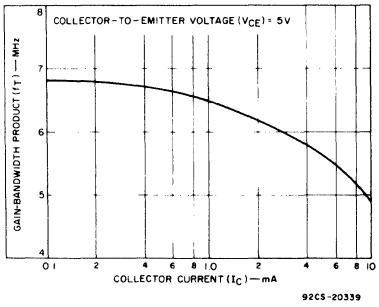


Fig. 30 – Gain-bandwidth product as a function of collector current (p-n-p).

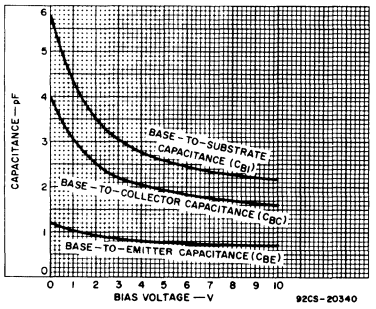


Fig. 31 – Capacitance as a function of bias voltage (p-n-p).

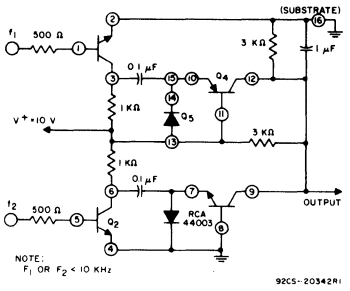


Fig. 32 – Frequency comparator using CA3096E.

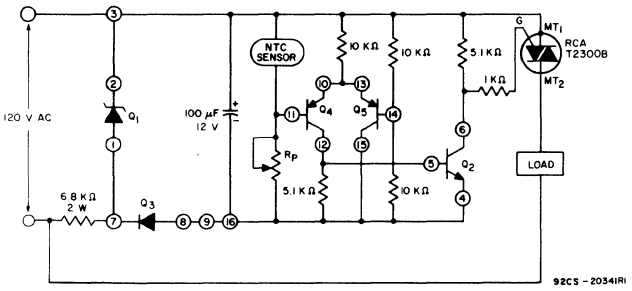


Fig. 33 – Line-operated level switch using CA3096AE or CA3096E.

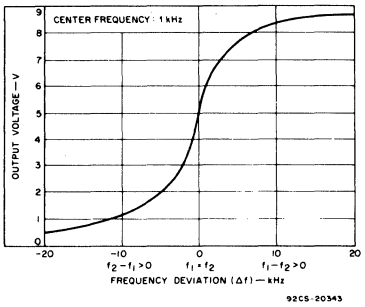


Fig. 34 – Frequency comparator characteristics.

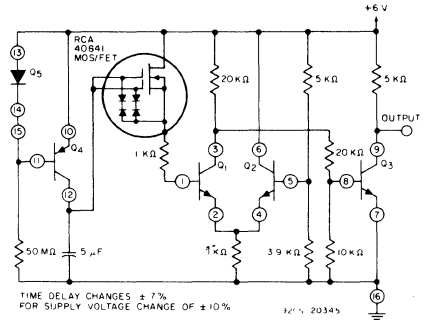


Fig. 35 – One-minute timer using CA3096AE and a MOS/FET.

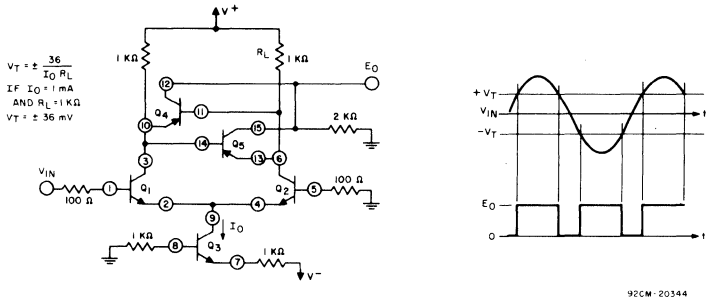


Fig. 36 – CA3096AE small-signal zero-voltage detector having noise immunity.

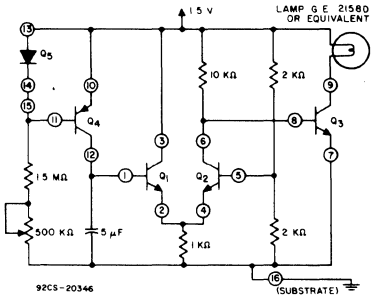


Fig. 37 – Ten-second timer operated form 1.5-volt supply using CA3096E.

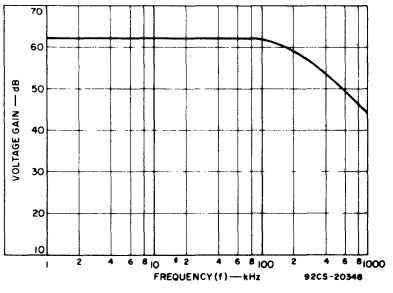


Fig. 38 – Gain-frequency characteristics.

Thyristor/Transistor Array

For Military, Commercial, and Industrial Applications

RCA-CA3097E Thyristor/Transistor Array is a monolithic integrated circuit that enables circuit designers to further integrate control systems. The CA3097E consists of five independent and completely isolated elements on one chip: an n-p-n transistor, a p-n-p/n-p-n transistor pair, a zener diode, a programmable unijunction transistor (PUT), and a sensitive-gate silicon controlled rectifier (SCR).

The CA3097 is supplied in either the 16-lead dual-in-line plastic package ("E" suffix) or the chip version ("H" suffix), and operates over the full military-temperature range of −55 to +125°C.

Includes:

- Uncommitted n-p-n Transistor
- Sensitive-Gate Silicon Controlled Rectifier
- Programmable Unijunction Transistor (PUT)
- p-n-p/n-p-n Transistor Pair
- Zener Diode
- Separate Substrate Connection

Features:

- Complete isolation between elements
- n-p-n transistor – V_{CEO} = 30 V (min.) I_C = 100 mA (max.)
- p-n-p/n-p-n transistor pair – beta ≥ 8000 (typ.) @ I_C = 10 mA, individual p-n-p, n-p-n, or transistor pair operation
- Programmable unijunction transistor (PUT) – peak-point current = 15 nA (typ.) at R_G = 1 MΩ; V_{AK} = ±30 V
- (PUT) Extremely long RC time constants with low value of external capacitor
- Sensitive-gate silicon controlled rectifier (SCR) – 150 mA forward current (max.)
- Zener-diode impedance (Z_Z) = 15Ω (typ.) at 10 mA

Applications:

- Timers
- Light dimmers/motor controls
- Oscillators
- "One-shot" multivibrators
- Voltage regulators
- Comparators, Schmitt triggers
- Constant-current sources
- Amplifiers
- Logic circuits
- SCR triggering
- Pulse Circuits

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Isolation Voltage, any terminal to substrate*	+50 V
Dissipation, Total Package:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly at 6.67 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C
Each n-p-n Transistor (Q3,Q5)	
The following ratings apply with terminals 6 & 9 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	30 V
Collector-to-Base Voltage (V_{CBO})	50 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	100 mA
Base Current (I_B)	20 mA
Dissipation (P_D)	500 mW
p-n-p Transistor (Q4)	
The following ratings apply with terminals 7 & 8 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	−40 V
Collector-to-Base Voltage (V_{CBO})	−50 V
Emitter-to-Base Voltage (V_{EBO})	−40 V
Collector Current (I_C)	−10 mA
Base Current (I_B)	−3 mA
Dissipation (P_D)	200 mW
p-n-p/n-p-n Transistor Pair (Q3,Q4)	
Dissipation (P_D)	500 mW
Programmable Unijunction Transistor, PUT (Q1)	
Gate-to-Cathode Positive Voltage (V_{GK})	30 V
Gate-to-Cathode Negative Voltage (V_{GKR})	5 V
Gate-to-Anode Negative Voltage (V_{GA})	30 V
Anode-to-Cathode Voltage (V_{AK})	±30 V
DC Anode Current	150 mA
Peak Anode Non-Recurrent Forward (On-State) Current (10 μs pulse)	2 A
Total Average Dissipation	300 mW
Silicon Controlled Rectifier, SCR (Q2)	
Repetitive Peak Reverse Voltage (V_{RRXM}), R_{GK} = 1 KΩ	30 V
Repetitive Peak Off-State Voltage (V_{DRXM}), R_{GK} = 1 kΩ	30 V
DC On-State Current (I_{TDC})	150 mA
Peak Surge (Non-Repetitive) On-State Current (10 μs pulse)	2 A
Forward Peak Gate Current (I_{GFM})	20 mA
Peak Gate-to-Cathode Reverse Voltage (V_{GRM})	5 V
Total Average Dissipation	300 mW
Zener Diode, (Z1)	
DC Current (I_Z)	25 mA
Dissipation (P_D)	250 mW

* One or more of the terminals of each element of the CA3097E is isolated from the substrate by a junction diode. In order to maintain electrical isolation between elements, the substrate terminal must be connected to a voltage which is no more positive than that of any other terminal. To avoid undesirable coupling between elements, the substrate terminal (terminal 10) should be maintained at either dc or signal (ac) ground.

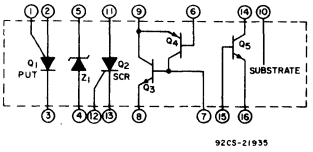


Fig. 1 – Schematic diagram of CA3097E.

TYPICAL CHARACTERISTICS

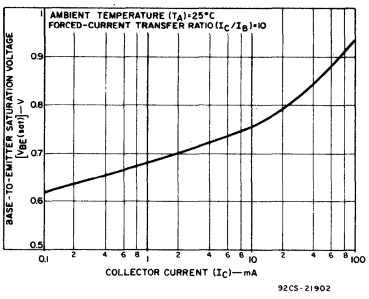


Fig.2 – Base-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

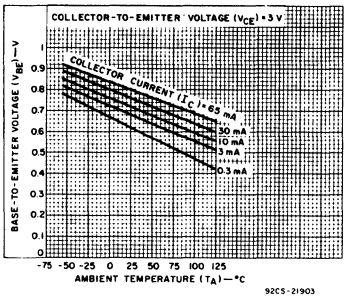


Fig.3 – Base-to-emitter voltage vs. ambient temperature for n-p-n transistors Q3 & Q5.

ELECTRICAL CHARACTERISTICS (Cont'd.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT), Q1							
OFFSET VOLTAGE	V_T*	V_S = 10V, R_G = 10kΩ	11,22[a]	0.2	–	0.7	V
		V_S = 10V, R_G = 1MΩ		0.2	–	0.7	
ANODE-TO-CATHODE ON-STATE VOLTAGE	V_F	I_F = 50mA	12	–	0.90	1.5	V
		I_F = 100mA		–	1	–	
PEAK OUTPUT VOLTAGE	V_{OM}	C = 0.22μF Anode Supply Voltage = 20V	13,23	–	10	–	V
PEAK-POINT CURRENT	I_P	V_S = 10V, R_G = 10kΩ	14,22[a]	–	0.55	1	μA
		V_S = 10V, R_G = 1MΩ	–	–	0.015	0.15	
VALLEY-POINT CURRENT	I_V	V_S = 10V, R_G = 10kΩ	17,15	4	40	–	μA
		V_S = 10V, R_G = 1MΩ	16	–	–	25	
GATE REVERSE CURRENT	I_{GAO}	V_S = 30V	22[c]	–	0.02	–	nA
GATE REVERSE CURRENT	I_{GKS}	Anode-To-Cathode Short, V_S = 30V	22[d]	–	0.2	–	nA
OUTPUT PULSE RISE TIME	t_r	Anode-Supply Voltage = 20V C = 0.22 μF	23	–	60	–	ns
SILICON CONTROLLED RECTIFIER (SCR), Q2							
PEAK OFF-STATE CURRENT: FORWARD	I_{DXM}	V_{DRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	μA
REVERSE	I_{RXM}	V_{RRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	
FORWARD DC VOLTAGE DROP	V_T	I_T = 50 mA	18	–	0.90	1.5	V
GATE-TO-SOURCE TRIGGER CURRENT	I_{GS}	T_A = 25°C	26	–	33	100	μA
		T_A = −55°C	26	–	50	–	
DC GATE-TRIGGER VOLTAGE	V_{GT}	V_L = 10V, R_L = 100Ω	19	–	0.55	0.75	V
HOLDING CURRENT	I_{HO}	R_{GK} = 1kΩ	20,24	–	1.2	–	mA
CRITICAL RATE-OF-RISE OF OFF-STATE VOLTAGE	dv/dt	EXPONENTIAL RISE, R_{GK} = 1kΩ, V_{DRXM} = 30V	25	–	150	–	V/μs
GATE-CONTROLLED TURN-ON TIME	t_{gt}	See Fig. 33	33	–	50	–	ns
CIRCUIT-COMMUTATED TURN-OFF TIME	t_q	See Fig. 33	33	–	10	–	μs
ZENER DIODE, Z1							
ZENER VOLTAGE	V_Z	I_Z = 10mA	21	7.2	8	8.8	V
ZENER IMPEDANCE	Z_Z	I_Z = 10mA, f = 1kHz		–	15	25	Ω
ZENER VOLTAGE TEMPERATURE COEFFICIENT	$(\Delta V_Z/V_Z)/\Delta T$	I_Z = 10mA		–	+0.05	–	%/°C
	$\Delta V_Z/\Delta T$			–	+4	–	mV/°C
ZENER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)ZIO}$	I_Z = 100μA TERM. 5 TO SUBSTRATE		50	80	–	V

* $V_T = V_P - V_S$ (Fig. 22)

TYPICAL CHARACTERISTICS (CONT'D)

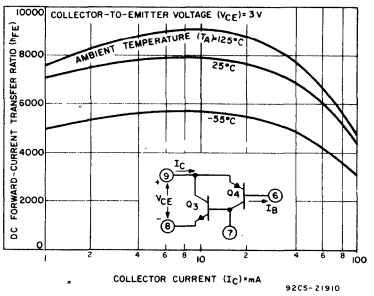


Fig. 10 – DC forward-current transfer ratio vs. collector current for transistor pair Q3, Q4.

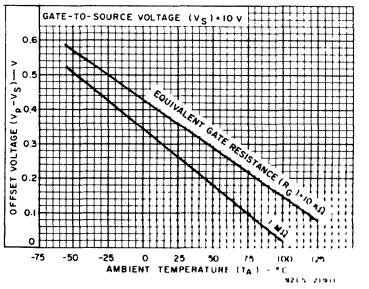


Fig. 11 – Offset voltage vs. ambient temperature for Q1 (PUT).

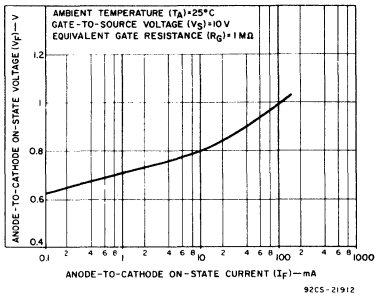


Fig. 12 – Anode-to-cathode on-state voltage vs. anode-to-cathode on-state current for Q1 (PUT).

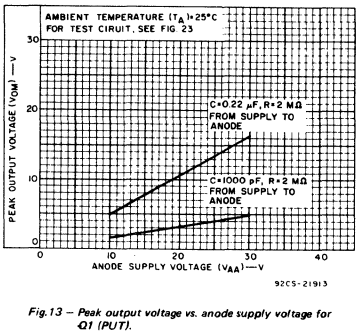


Fig. 13 – Peak output voltage vs. anode supply voltage for Q1 (PUT).

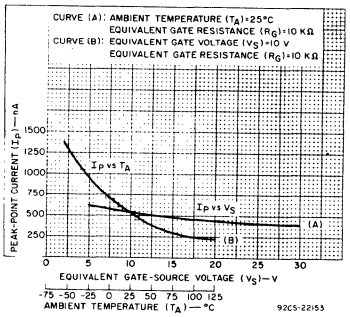


Fig. 14 – Peak-point current vs. gate-source voltage and ambient temperature for Q1 (PUT).

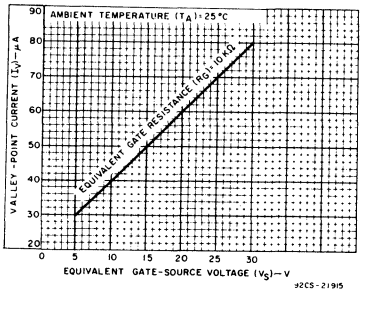


Fig. 15 – Valley-point current vs. gate-source voltage for Q1 (PUT).

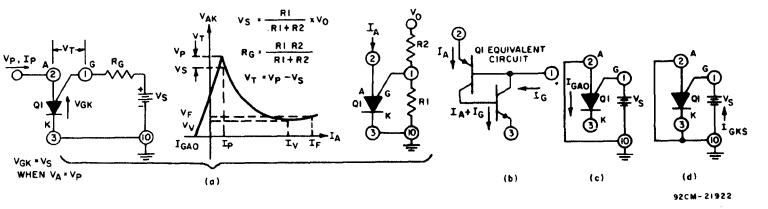


Fig. 22 – General anode characteristics for Q1 (PUT).

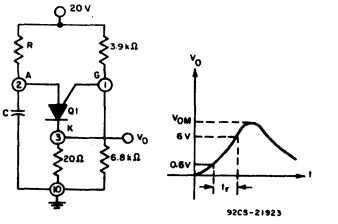


Fig. 23 – Output pulse characteristics for Q1 (PUT).

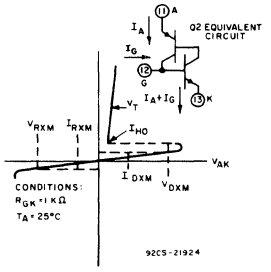


Fig. 24 – Principle voltage-current characteristics for Q2 (SCR).

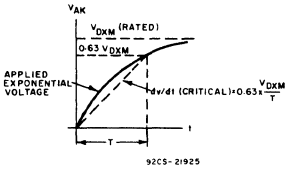


Fig. 25 – Definition of critical rate of rise of off-state voltage for Q2 (SCR).

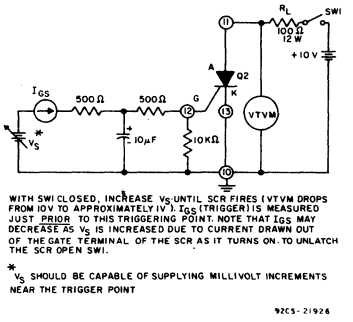


Fig. 26 – Test circuit for determining I_{GS} in Q2 (SCR).

APPLICATIONS CIRCUITS

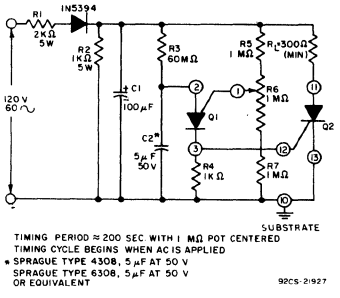


Fig. 27 – AC line-operated one-shot timer.

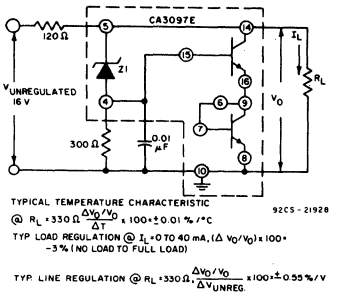


Fig. 28 – Temperature-compensated shunt regulator.

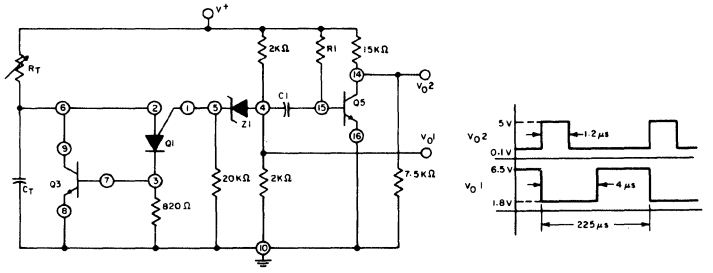


Fig. 29 – Pulse generator.

Programmable Schmitt Trigger
— With Memory
—Dual-Input Precision Level Detectors

Applications:

- **Control of relays, heaters, LED's lamps, photo-sensitive devices, thyristors, solenoids, etc.**
- **Signal reconditioning**
- **Phase and frequency modulators**
- **On/off motor switching**
- **Schmitt triggers, level detectors**
- **Time delays**
- **Overvoltage, overcurrent, overtemperature protection**
- **Battery-operated equipment**
- **Square and triangular-wave generators**

Features:

- **Programmable operating current**
- **Micropower standby dissipation**
- **Direct control of currents up to 150 mA**
- **Low input on/off current of less than 1 nA for programmable bias current of 1 μA**
- **Built-in hysteresis: 20 mV max.**
- **Programmable hysteresis: 20 mV to V^+**
- **Dual reference input**
- **High sensor range: 100 Ω to 100 MΩ**
- **Stable predictable switching levels**
- **Temperature-compensated reference voltage**
- **Power can be strobed off via term. 2**

The RCA-CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with maximum operating voltage of ±8 volts. It can directly control currents up to 150 mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3098 contains the following major circuit-function features (see Fig. 1):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and otuput stages: these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

The CA3098 is supplied in the 8-lead dual-in-line plastic package ("Mini-Dip", E suffix), 8-lead TO-5 style package (T suffix), 8-lead TO-5-style package with formed leads "DIL-CAN" (S suffix), and in chip form (H suffix).

For information on another RCA Dual-Input Precision Level Detector, see the data bulletin for the RCA-CA3099E, File No. 620.

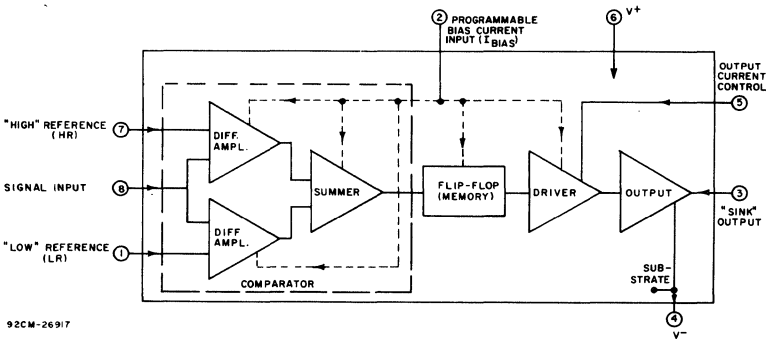


Fig. 1 – Block diagram of CA3098 programmable Schmitt trigger.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

Supply Voltage Between Terminals 6 and 4,	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 8 and 1, and Terminals 7 and 8	10	V
Operating Voltage Range:		
Term. 8	V^- to V^+	
Term. 7	(V^- plus 2.0 V) to V^+	
Term. 1	(V^-) to (V^+ minus 2.0 V)	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programmable Bias Current (Term. 2)	1	mA
Output Current Control (Term. 5)	15	mA
Power Dissipation:		
Without Heat Sink:		
Up to T_A = 55°C		
CA3098S, CA3098T	630	mW
CA3098E	630	mW
Above T_A = 55°C Derate linearly at	6.67	mW/°C
With Heat Sink:		
Up to T_A = 55°C		
CA3098S, CA3098T	1.6	W
Above T_A = 55°C		
CA3098S, CA3098T Derate linearly at	16.67	mW/°C
Ambient Temperature Range (All Packages):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Input Offset Voltage: "Low" Ref., $V_{IO(LR)}$	V_{LR} = Gnd, V_{HR} = 3 V, I_{BIAS} = 100 μA	5	−15	−3	6	mV
"High" Ref., $V_{IO(HR)}$	V_{HR} = Gnd, V_{LR} = −3 V, I_{BIAS} = 100 μA	6	−10	±10	10	
Temp. Coeff: "Low" Ref.	−55 °C to + 125 °C	7	–	4.5	–	μV/°C
"High" Ref.	−55 °C to + 125 °C	8	–	±8.2	–	
Min. Hysteresis Voltage $V_{IO(HR-LR)}$:	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	9	–	3	20	mV
Temp. Coeff.	−55°C to + 125 °C	10	–	6.7	–	μV/°C
Output Saturation Voltage, $V_{CE}(SAT)$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	11,12	–	0.72	1.2	V
Total Supply Current, I_{TOTAL}: "ON"	V_I = 4 V, V_{REG} = 6 V; V^+ = 12 V, I_{BIAS} = 100 μA	13,14	500	710	800	μA
"OFF"	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		400	560	750	μA
Input Bias Current, I_{IB}: $I_{B(p-n-p)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	15	–	42	100	nA
$I_{B(n-p-n)}$	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		–	28	100	nA
Output Leakage Current, $I_{CE(OFF)}$	Current from Term. 3 when Q46 is "OFF"	–	–	–	10	μA
Switching Times: Delay, t_d	I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V	18	–	600	–	ns
Fall, t_f			–	50	–	ns
Rise, t_r			–	500	–	ns
Storage, t_s			–	4.5	–	μs
Output Current, I_O	V^+ = 12 V, I_{BIAS} = 50 μA	–	100	–	–	mA

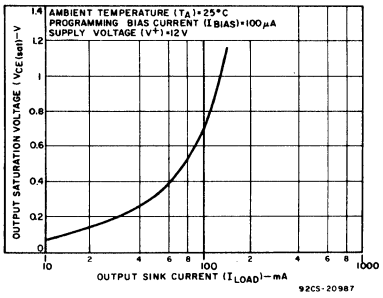


Fig. 11 – Output saturation voltage vs. output sink current.

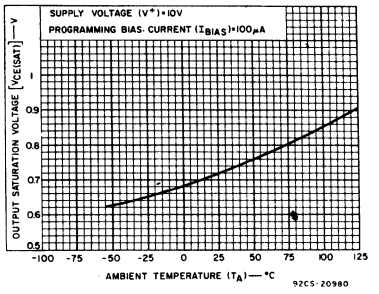


Fig. 12 – Output saturation voltage vs. ambient temperature.

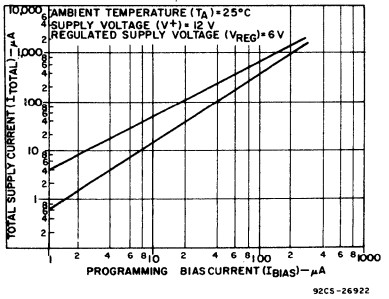


Fig. 13 – Total supply current vs. programming bias current.

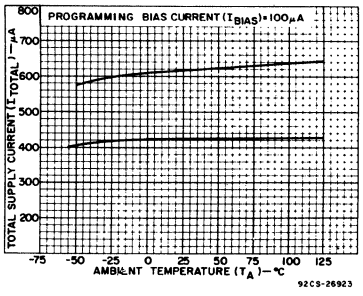


Fig. 14 – Total supply current vs. ambient temperature.

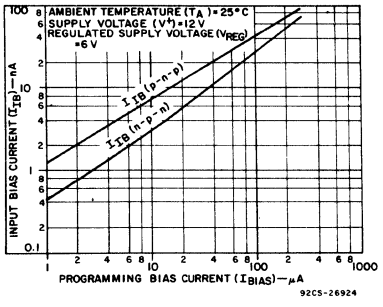


Fig. 15 – Input bias current vs. programming bias current.

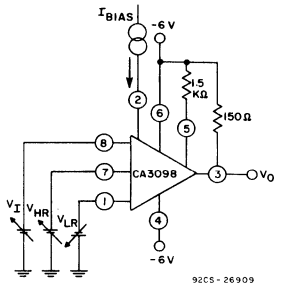


Fig. 16 – Input-offset voltage test circuit.

Programmable Comparator - - With Memory

RCA-CA3099E Programmable Comparator is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3099E can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with a maximum operating voltage of ± 8 volts. It can directly control currents up to 150 mA. It operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3099E contains the following six (6) major circuit-function features (Figure 1):

1. **Differential amplifiers and summer;** the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. **Flip-flop;** the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. **Driver and output stages;** these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. **Programmable operating current;** the circuit incorporates a separate terminal to permit programming the desired quiescent operating current and performance parameters.
5. **Internal sources of reference voltage and programmable bias current;** an integral circuit supplies a temperature-compensated reference voltage ($V_b/2$) which is about 1/2 of the externally applied bias voltage (V_b). Additionally, integral circuitry can optionally be used to supply an uncompensated constant-current source of bias (I_{bias}).
6. **Voltage regulator;** provides optional on-chip voltage regulation when power for the CA3099E is provided by an unregulated supply.

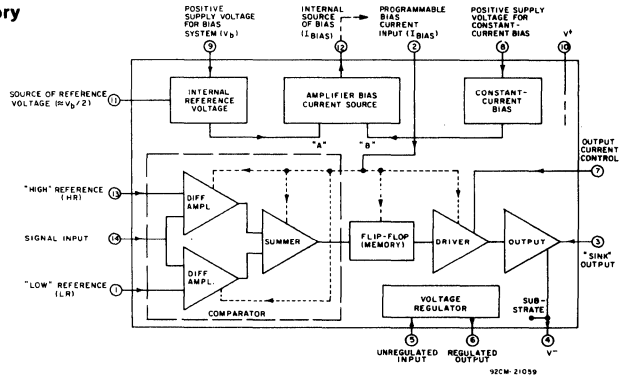


Fig. 1—Block diagram of CA3099E programmable comparator.
(See page 3 for general description of circuit operation.)

Features:

- **Programmable operating current**
- **Micro-power standby dissipation**
- **Directly controls current up to 150 mA**
- **Low input on/off current of less than 1 nA for programmable bias current of 1 μA**
- **Built-in hysteresis: 10 mV max.**
- **Programmable hysteresis: 10 mV to V^+**
- **Dual reference input**
- **High sensor range: 100 Ω to 100 MΩ**
- **Stable predictable switching levels**
- **Temperature-compensated reference voltage**

Applications:

- **Control of relays, heaters, LED's, lamps, photo-sensitive devices, thyristors, solenoids, etc.**
- **Signal reconditioning**
- **Phase and frequency modulators**
- **On/off motor switching**
- **Schmitt triggers, level detectors**
- **Time delays**
- **Overvoltage, overcurrent, overtemperature protection**
- **Battery-operated equipment**
- **Square and triangular-wave generators**

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

Supply Voltage Between Terminals 10 and 4, 9 and 4, 8 and 4	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 14 and 1, and Terminals 13 and 14	10	V
Operating Voltage Range:		
Term. 14	0 V to V^+	
Term. 13	2.0 V to V^+	
Term. 1	0 V to V^+ minus 2.0 V	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programming Bias Current (Term. 2)	1	mA
Output Current Control (Term. 7)	15	mA
Power Dissipation:		
Up to T_A = 55°C	750	mW
Above T_A = 55°C, Derate Linearly at	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Termperature (During Soldering):		
At distance not less than 1/32 inch (0.79 mm) from seating plane for 10 s maximum	+265	°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C *(Unless otherwise indicated)*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C Unless Otherwise Indicated	FIG. No.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Reference Voltage	V_{REF}	Term. 9 = 12 V, Term.4 = Grd, Term.11 = Test	–	5.7	6	6.3	V
Reference Voltage Temperature Coefficient			–	–	100	–	μV/°C
Regulated Supply Voltage	V_{REG}	Term.5 1K to 12V, Term.4 = Grd, Term.6 10K to Grd	5	6	7.2	8	V
Regulated Supply Voltage Temperature Coefficient			5	–	2.9	–	mV/°C
Input Offset Voltage: "Low" Reference	V_{IO} (LR)	V_{LR} = Grd, V_{HR} = 3 V, I_{BIAS} = 100 μA	20, 6	−8	−3	2	mV
"High" Reference	V_{IO} (HR)	V_{HR} = Grd, V_{LR} = −3 V, I_{BIAS} = 100 μA	20, 7	−5	±1	5	
"Low" Reference Temp. Coefficient		−55°C to +125°C	20, 8	–	4.5	20	μV/°C
"High" Reference Temp. Coefficient		−55°C to +125°C	20, 9	–	±8.2	±20	
Min. Hysteresis Voltage	$V_{IO(HR-LR)}$	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21, 10	–	3	10	mV
Min. Hysteresis Voltage Temperature Coefficient		−55°C to +125°C	11	–	6.7	20	μV/°C
Output Saturation Voltage	$V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,12,13	–	0.72	1.2	V
Total Supply Current: I_{TOTAL} "ON"	I_{TOTAL}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	600	710	800	μA
I_{TOTAL} "OFF"		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	420	560	750	
Input Bias Current: $I_{B(p-n-p)}$	I_{IB}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	33	200	nA
$I_{B(n-p-n)}$		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	20	60	
Output Leakage Current	$I_{CE(OFF)}$	Current from Term.3 when Q46 is "OFF"	–	–	–	10	μA
Internal Bias Current	I_{IBC}		18,19	120	200	280	
Switching Times:							
Delay	t_d	I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V	22	–	600	–	ns
Fall	t_f		22	–	50	–	
Rise	t_r		22	–	500	–	
Storage	t_s		22	–	4.5	–	μs

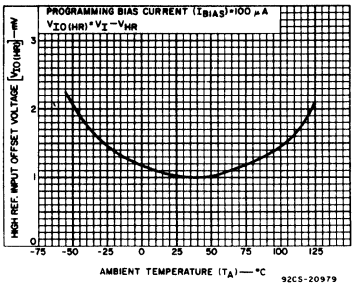


Fig. 9 – Input-offset voltage ("high" reference) vs. ambient temperature.

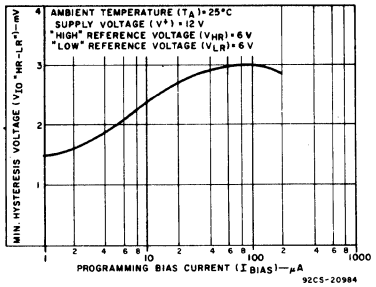


Fig. 10 – Min. hysteresis voltage vs. programming bias current.

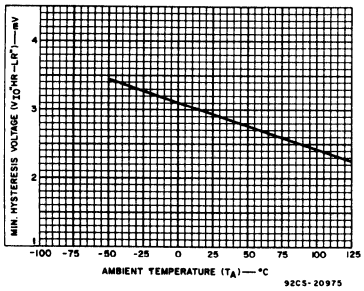


Fig. 11 – Min. hysteresis voltage vs. ambient temperature.

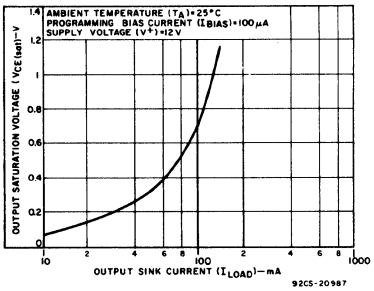


Fig. 12 – Output saturation voltage vs. output sink current.

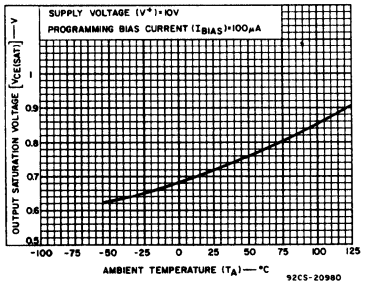


Fig. 13 – Output saturation voltage vs. ambient temperature.

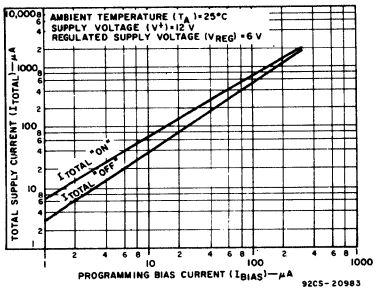


Fig. 14 – Total supply current vs. programming bias current.

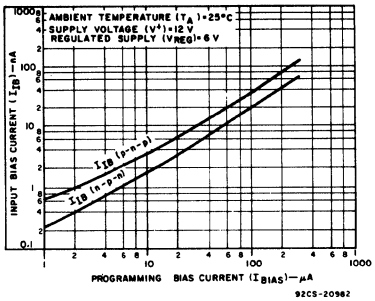


Fig. 15 – Input bias current vs. programming bias current.

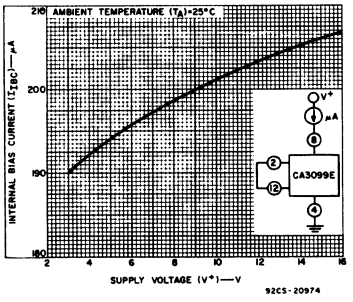


Fig. 16 – Internal bias current vs. supply voltage.

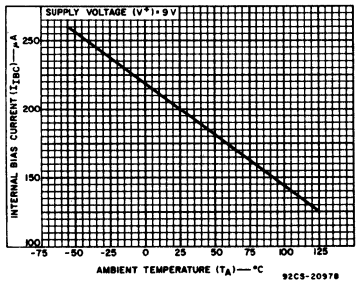


Fig. 17 – Internal bias current vs. ambient temperature.

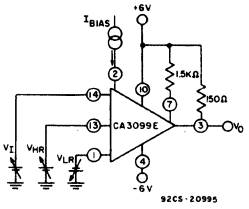


Fig. 18 – Input-offset voltage test circuit.

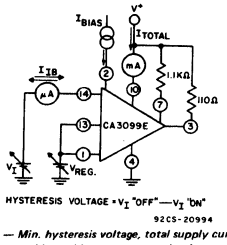


Fig. 19 – Min. hysteresis voltage, total supply current, and input bias current test circuit.

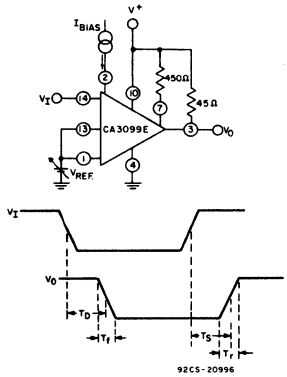


Fig. 20 – Switching time test circuit.

For application information, see Data Bulletin File No. 620.

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C:*

CHARACTERISTICS	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15 V UNLESS OTHERWISE SPECIFIED	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC					
Input Offset Voltage, V_{IO}	V_O = 0 ± 0.1 V	–	± 1	± 5	mV
Input Bias Current, I_{IB}	V_O = 0 ± 1 V	–	0.7	2	μA
Input Offset Current, I_{IO}	V_O = 0 ± 1 V	–	± 0.05	± 0.4	μA
Low-Frequency Open-Loop Voltage Gain, A_{OL}●	V_O = ± 1 V Peak, F = 1 kHz	56	61	–	dB
Common-Mode Input Voltage Range, V_{ICR}	CMRR ≥ 76 dB	± 12	+14 −13	–	V
Common-Mode Rejection Ratio, CMRR	V_I Common Mode = ± 12 V	76	90	–	dB
Maximum Output Voltage: Positive, V_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	+9	+11	–	V
Maximum Output Voltage: Negative, V_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	−9	−11	–	V
Maximum Output Current: Positive, I_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	+15	+30	–	mA
Maximum Output Current: Negative, I_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	−15	−30	–	mA
Supply Current, I^+	V_O = 0 ± 0.1 V, R_L ≥ 10 KΩ	–	8.5	10.5	mA
Power-Supply Rejection Ratio, PSRR	ΔV^+ = ± 1 V, ΔV^- = ± 1 V	60	70	–	dB
DYNAMIC					
Unity-Gain Crossover Frequency, f_T	C_C = 0, V_O = 0.3 V (P-P)	–	38	–	MHz
1-MHz Open-Loop Voltage Gain, A_{OL}	f = 1 MHz, C_C = 0, V_O = 10 V (P-P)	36	42	–	dB
Slew Rate, SR: 20-dB Amplifier	A_V = 10, C_C = 0, V_I = 1 V (Pulse)	50	70	–	V/μs
Slew Rate, SR: Follower Mode	A_V = 1, C_C = 10 pF, V_I = 10 V (Pulse)	–	25	–	V/μs
Power Bandwidth, PBW▲: 20-dB Amplifier	A_V = 10, C_C = 0, V_O = 18 V (P-P)	0.8	1.2	–	MHz
Power Bandwidth, PBW▲: Follower Mode	A_V = 1, C_C = 10 pF, V_O = 18 V (P-P)	–	0.4	–	MHz
Open-Loop Differential Input Impedance, Z_I	F = 1 MHz	–	30	–	KΩ
Open-Loop Output Impedance, Z_O	F = 1 MHz	–	110	–	Ω
Wideband Noise Voltage Referred to Input, e_N(Total)	BW = 1 MHz, R_S = 1 KΩ	–	8	–	μV_{RMS}
Settling Time, t_s [To Within ± 50 mV of 9 V Output Swing]	R_L = 2 KΩ, C_L = 20 pF	–	0.6	–	μs

▲ Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$ ● Low-frequency dynamic characteristic

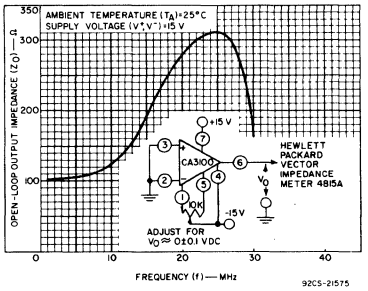


Fig. 7 – Typical open-loop output impedance vs. frequency.

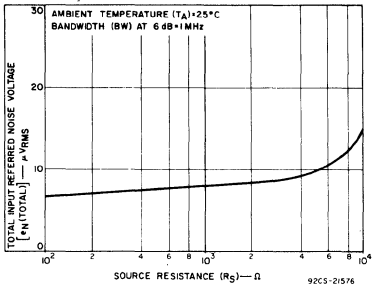


Fig. 8 – Wideband input noise voltage vs. source resistance.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

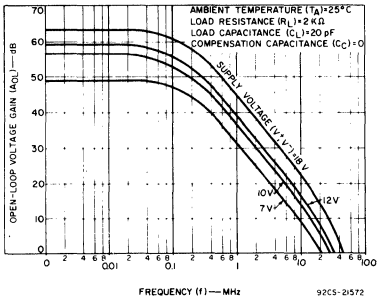


Fig. 4 – Open-loop gain vs. frequency and supply voltage.

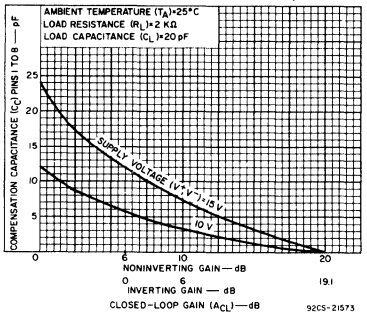


Fig. 5 – Required compensation capacitance vs. closed-loop gain.

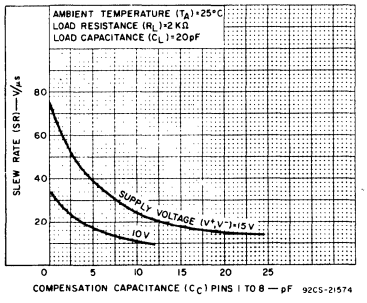


Fig. 6 – Slew rate vs. compensation capacitance.

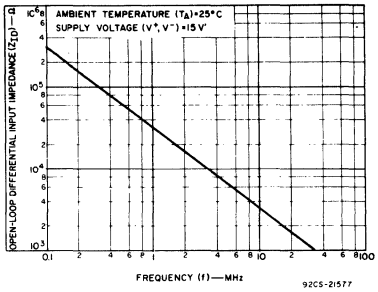


Fig. 9 – Typical open-loop differential input impedance vs. frequency.

TYPICAL APPLICATIONS

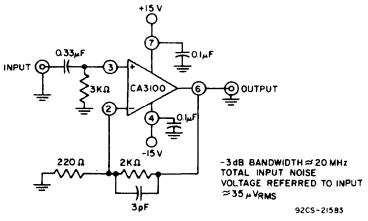


Fig. 21 – 20 dB video amplifier.

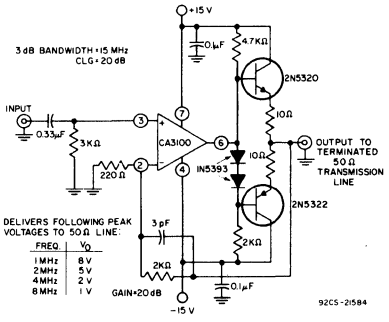


Fig. 22 – 20 dB video line driver.

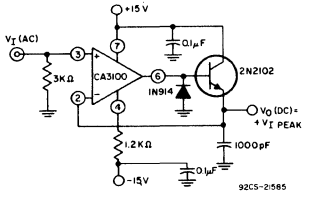


Fig. 23 – Fast positive peak detector.

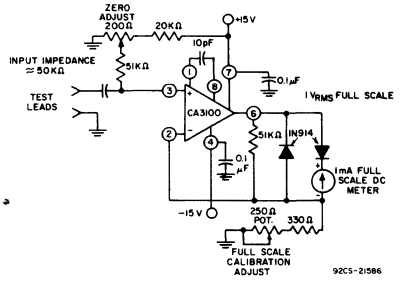
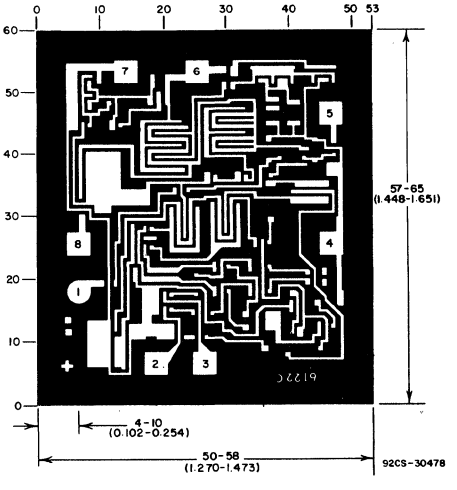


Fig. 24 – 1 MHz meter-driver amplifier.

Chip Dimensions and Pad Layout



CA3100H Chip

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

COMPARISON OF RELATED PREDECESSOR TYPE WITH TYPES IN THIS DATA BULLETIN

	DATA FILE NO.	V_{CEO} min.	V_{CBO} min.	V_{CE} sat. typ. V	V_{BE} typ. V	I_C max. mA	C_{CB} typ. pF	C_{CI} typ. pF	C_{EB} typ. pF
				I_C=10 mA	I_C=1 mA				
CA3018	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3018A	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3118AT		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3118T		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=10mA	I_C=1 mA				
CA3046	341	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3146AE		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3146E		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=50mA	I_C=10 mA				
CA3083	481	15	20	0.4	0.74	100	–	–	–
CA3183AE		40	50	1.7	0.75	75	–	–	–
CA3183E		30	40	1.7	0.75	75	–	–	–

STATIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C		LIMITS CA3118AT, CA3146AE Min.	CA3118AT, CA3146AE Typ.	CA3118AT, CA3146AE Max.	CA3118T, CA3146E Min.	CA3118T, CA3146E Typ.	CA3118T, CA3146E Max.	UNITS
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		50	72	–	40	72	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		40	56	–	30	56	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10μA, I_B = 0, I_E = 0		50	72	–	40	72	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0		5	7	–	5	7	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0		–	see curve	5	–	see curve	5	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0		–	0.002	100	–	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=5V	I_C=10 mA	–	85	–	–	85	–	–
			I_C=1 mA	30	100	–	30	100	–	
			I_C=10μA	–	90	–	–	90	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 1 mA		0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 10mA, I_B = 1 mA		–	0.33	–	–	0.33	–	V
For transistors Q3 and Q4 (Darlington Configeration):										
Collector-Cutoff Current (CA3118AT and CA3118T only)	I_{CEO}	V_{CE} = 10V, I_B = 0		–	–	5	–	–	–	μA
DC Forward-Current Transfer Ratio (CA3118AT and CA3118T only)	h_{FE}	V_{CE} = 5V, I_C = 1 mA		1500	9000	–	1500	9000	–	–
Base-to-Emitter (Q3 to Q4)	V_{BE}	V_{CE}=5V	I_E = 10mA	–	1.46	–	–	1.46	–	V
			I_E = 1mA	–	1.32	–	–	1.32	–	
Magnitude of Base-to-Emitter Temperature Coefficient	$\lvert\frac{\Delta V_{BE}}{\Delta T}\rvert$	V_{CE} = 5V, I_E = 1mA		–	4.4	–	–	4.4	–	mV/°C
For transistors Q1 and Q2 (AS a Differential Amplifier):										
Magnitude of Input Offset Voltage $\lvert V_{BE1} - V_{BE2}\rvert$	$\lvert V_{IO}\rvert$	V_{CE} = 5V, I_E = 1mA		–	0.48	5	–	0.48	5	mV
Magnitude of h_{FE} Ratio (CA3118AT and CA3118T only)		V_{CE} = 5V, $I_{C1} = I_{C2}$ = 1mA		0.9	1.0	1.1	0.9	1.0	1.1	–
Magnitude of Base-to-Emitter Temperature Coefficient	$\lvert\frac{\Delta V_{BE}}{\Delta T}\rvert$	V_{CE} = 5V, I_E = 1mA		–	1.9	–	–	1.9	–	mV/°C
Magnitude of V_{IO} ($V_{BE1} - V_{BE2}$) Temperature Coefficient	$\lvert\frac{\Delta V_{IO}}{\Delta T}\rvert$	V_{CE} = 5V, $I_{C1} = I_{C2}$ = 1mA		–	1.1	–	–	1.1	–	μV/°C
Magnitude of Input Offset Current $\lvert I_{IO_1} - I_{IO_2}\rvert$ (CA3146AE and CA3146E only)	I_{IO}	V_{CE} = 5V, $I_{C_1} = I_{C_2}$ = 1 mA		–	0.3	2	–	0.3	2	μA

TYPICAL STATIC CHARACTERISTICS CURVES– CA3118 and CA3146 SERIES (cont'd Fig.2 to 12)

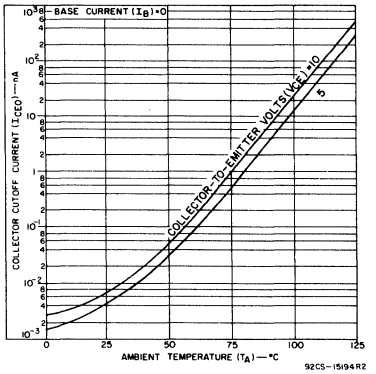


Fig. 2 – I_{CEO} vs. T_A for any transistor.

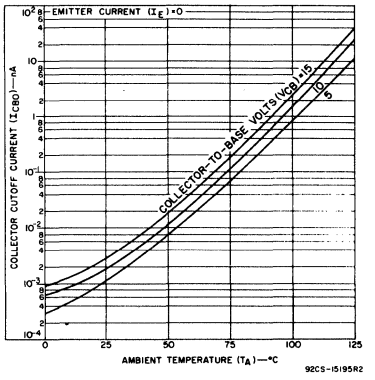


Fig. 3 – I_{CBO} vs. T_A for any transistor.

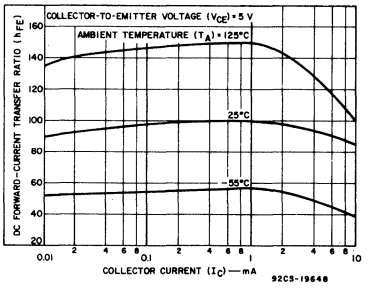


Fig. 4 – h_{FE} vs. I_C for any transistor.

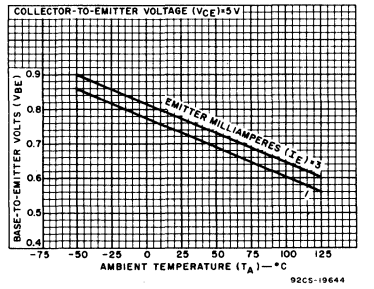


Fig. 5 – V_{BE} vs. T_A for any transistor.

TYPICAL STATIC CHARACTERISTICS CURVES– CA3118 and CA3146 SERIES (Fig.2 to 12)

TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR)–CA3118,CA3146 SERIES (Fig. 13 to 22)

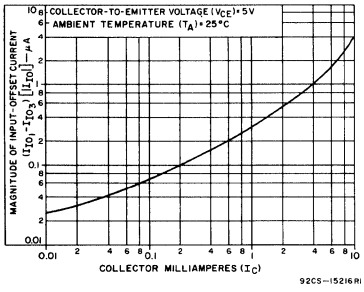


Fig. 12 – I_{IO} vs. I_C (Q1 and Q2) for types CA3146AE and CA3146E.

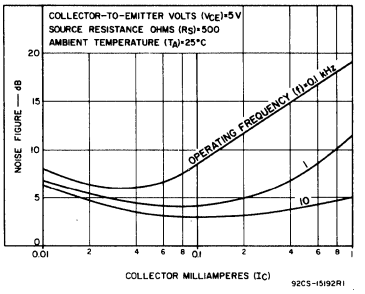


Fig. 13 – NF vs. I_C @ R_S = 500Ω.

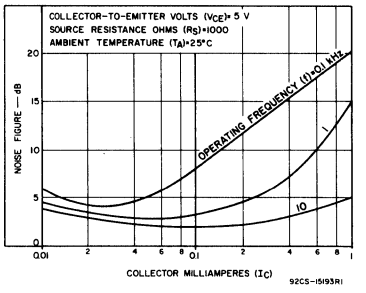


Fig. 14 – NF vs. I_C @ R_S = 1kΩ.

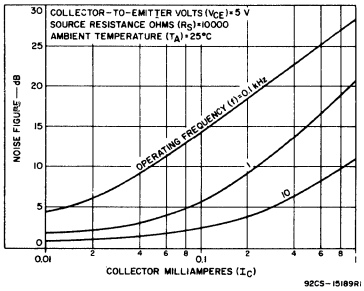


Fig. 15 – NF vs. I_C @ R_S = 10kΩ.

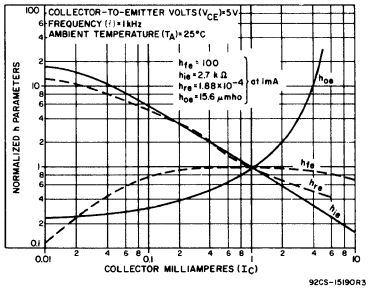


Fig. 16 – h_{fe}, h_{ie}, h_{oe}, h_{re} vs. I_C.

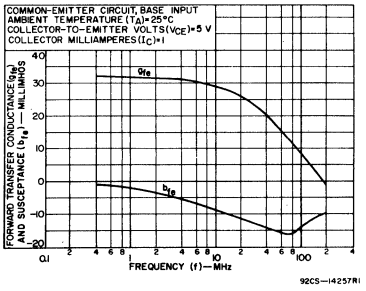


Fig. 17 – y_{fe} vs. f.

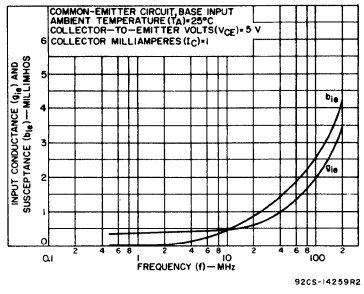


Fig. 18 – y_{ie} vs. f.

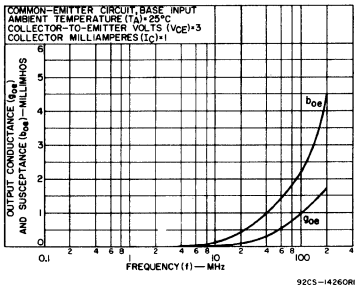


Fig. 19 – y_{oe} vs. f.

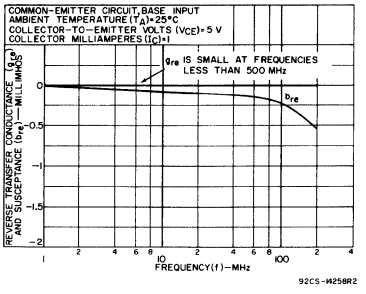


Fig. 20 – y_{re} vs. f.

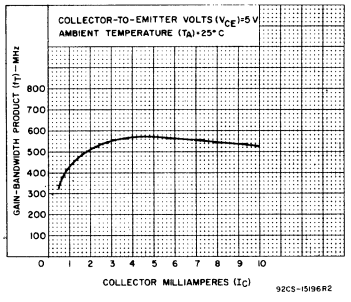


Fig. 21 – f_T vs. I_C.

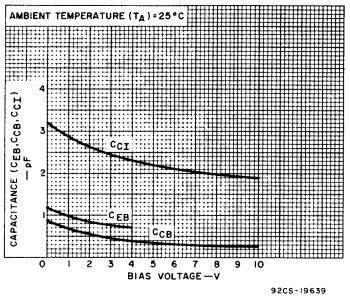


Fig. 22 – C_{EB}, C_{CB}, C_{CI} vs. bias voltage

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

RCA-CA3127E* consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127E useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127E provides close electrical and thermal matching of the five transistors.

The CA3127E is supplied in a 16-lead dual-in-line plastic package and operates over the full military temperature range of −55 to +125°C.

* Formerly RCA Dev. No. TA6206.

MAXIMUM RATINGS,
Absolute-Maximum Values:

POWER DISSIPATION, P_D:
- Any one transistor . . . . . 85 mW
- Total Package:
- For T_A up to 75°C . . . . . 425 mW
- For T_A > 75°C Derate
- Linearly at . . . . . 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating . . . . . −55 to +125°C
- Storage . . . . . −65 to +125°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

The following ratings apply for each transistor in the device:
- Collector-to-Emitter Voltage, V_{CEO} . . . 15 V
- Collector-to-Base Voltage, V_{CBO} . . . . 20 V
- Collector-to-Substrate Voltage, V_{CIO}* . . 20 V
- Collector Current, I_C . . . . . 20 mA

*The collector of each transistor of the CA3127E is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

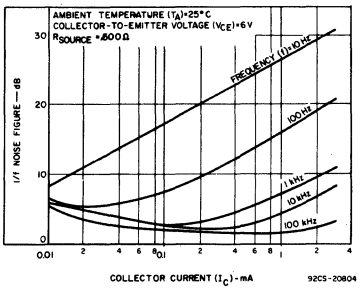


Fig. 2 — 1/f noise figure as a function of collector current at R_{SOURCE} = 500 Ω.

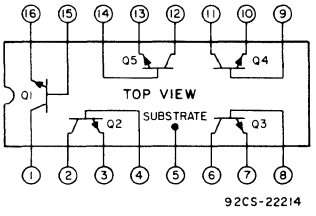


Fig. 1 — Schematic diagram of CA3127E.

Features:

- Gain-Bandwidth Product (f_T) > 1 GHz
- Power Gain = 30 dB (typ.) at 100 MHz
- Noise Figure = 3.5 dB (typ.) at 100 MHz
- Five independent transistors on a common substrate

Applications:

- VHF amplifiers
- Multifunction combinations— RF/mixer/oscillator
- Sense amplifiers
- Synchronous detectors
- VHF mixers
- IF Converter
- IF amplifiers
- Synthesizers
- Cascade amplifiers

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:						
Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0		20	32	–	V
Collector-to-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0		15	24	–	V
Collector-to-Substrate Breakdown Voltage	I_{C1} = 10 μA, I_B = 0, I_E = 0		20	60	–	V
Emitter-to-Base Breakdown Voltage*	I_E = 10 μA, I_C = 0		4	5.7	–	V
Collector-Cutoff-Current	V_{CE} = 10 V, I_B = 0		–	–	0.5	μA
Collector-Cutoff-Current	V_{CB} = 10 V, I_E = 0		–	–	40	nA
DC Forward-Current Transfer Ratio	V_{CE} = 6 V	I_C = 5 mA	35	88	–	
		I_C = 1 mA	40	90	–	
		I_C = 0.1 mA	35	85	–	
Base-to-Emitter Voltage	V_{CE} = 6 V	I_C = 5 mA	0.71	0.81	0.91	V
		I_C = 1 mA	0.66	0.76	0.86	
		I_C = 0.1 mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1 mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	V_{CE} = 6 V, I_C = 1 mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

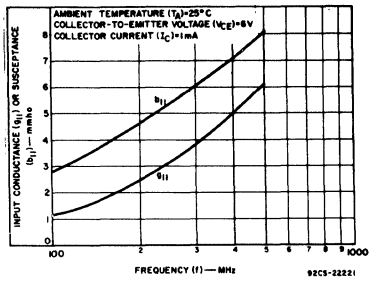


Fig. 10 – Input admittance (Y_{11}) as a function of frequency.

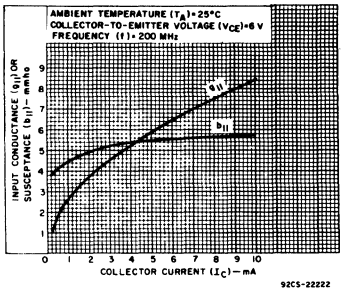


Fig. 11 – Input admittance (Y_{11}) as a function of collector current.

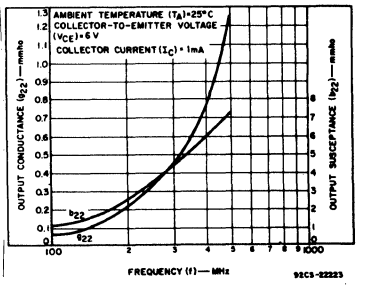


Fig. 12 – Output admittance (Y_{22}) as a function of frequency.

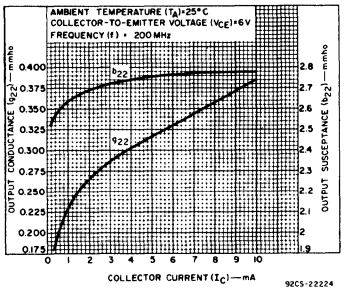


Fig. 13 – Output admittance (Y_{22}) as a function of collector current.

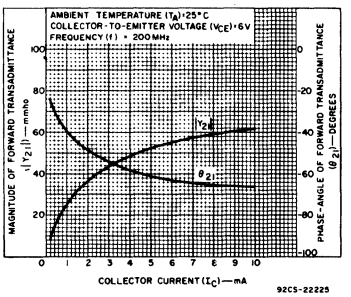


Fig. 14 – Forward transadmittance (Y_{21}) as a function of collector current.

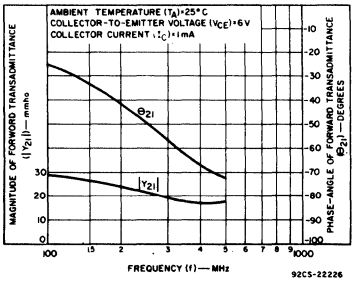


Fig. 15 – Forward transadmittance (Y_{21}) as a function of frequency.

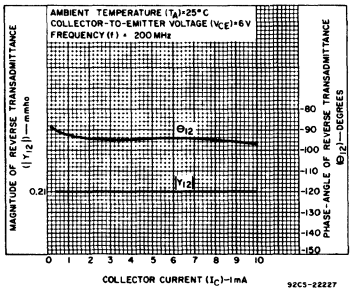


Fig. 16 – Reverse transadmittance (Y_{12}) as a function of collector current.

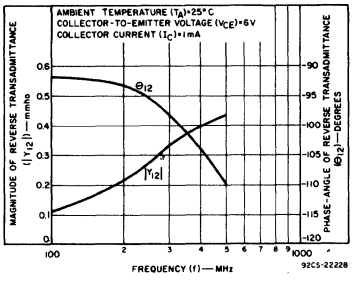


Fig. 17 – Reverse transadmittance (Y_{12}) as a function of frequency.

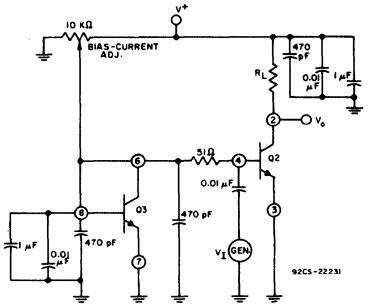


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.

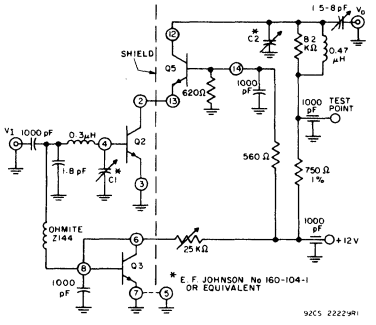


Fig. 19 – 100-MHz power-gain and noise-figure test circuit.

This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

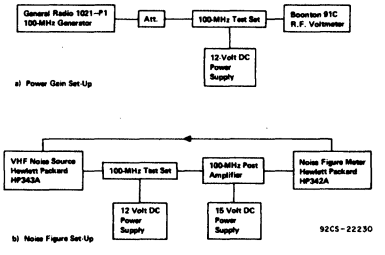


Fig. 20 – Block diagrams of power-gain and noise-figure test set-ups.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK −
UP TO 55°C ..... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK −
AT 125°C ..... 418 mW
BELOW 125°C ... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (all types) ..... −55 to + 125°C
STORAGE (all types) ..... −65 to + 150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 mm) FROM CASE
FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or to either supply.

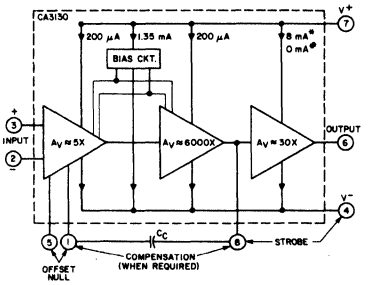


Fig. 3 – Block diagram of the CA3130 Series.

ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS									Units
	CA3130B (T,S)			CA3130A (T,S,E)			CA3130 (T,S,E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	8	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 V_{p-p}, R_L=2 kΩ	100	110	–	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	86	100	–	80	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V
Maximum Output Voltage:										
At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	12	13.3	–	V
V_{OM}^-	–	0.002	0.01	–	0.002	0.01	–	0.002	0.01	
At R_L= ∞ V_{OM}^+	14.99	15	–	14.99	15	–	14.99	15	–	
V_{OM}^-	–	0	0.01	–	0	0.01	–	0	0.01	
Maximum Output Current:										
I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	12	20	45	
Supply Current, I^+:										
V_O=7.5 V, R_L= ∞	–	10	15	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	–	2	3	
Input Current, I_I*	–	Fig.12	15	–	Fig.12	–	–	Fig.12	–	nA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	5	15	–	10	–	–	10	–	μV/°C
Large-Signal Voltage	50 k	320 k	–	–	320 k	–	–	320 k	–	V/V
Gain, A_{OL}*	94	110	–	–	110	–	–	110	–	dB

* T_A = −55 to +125°C, $V^{\pm}$ = ±7.5 V (I_I and $\Delta V_{IO}/\Delta T$), V_O = 10 V_{p-p} and R_L = 2 kΩ (A_{OL}).

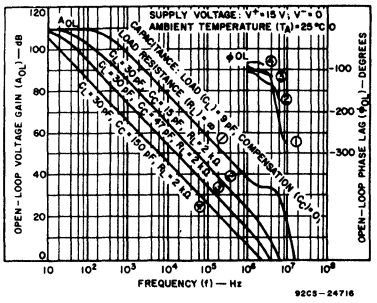


Fig. 4 – Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

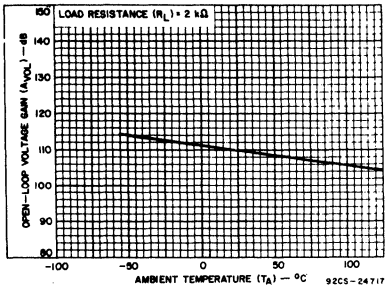


Fig. 5 – Open-loop gain vs. temperature.

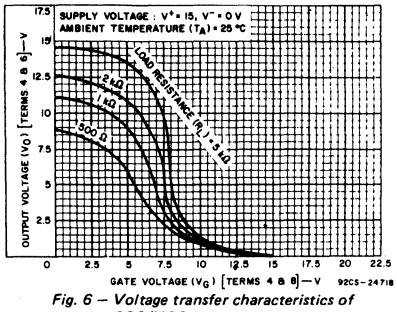


Fig. 6 – Voltage transfer characteristics of COS/MOS output stage.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages—The circuit of the CA3130 is shown in Fig. 1. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes nonconductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage, Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are nonlinear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5 pA at T_A=25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig.11 contains data showing the variation of input current as a function of common-mode input voltage at T_A = 25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied

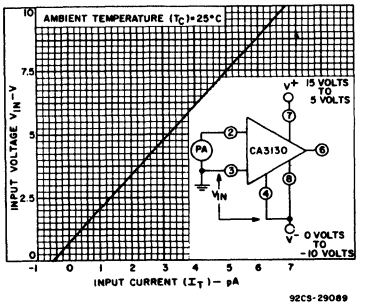


Fig.11 — Input current vs. common-mode voltage.

voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig.12 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

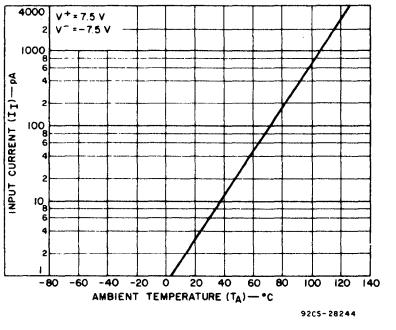


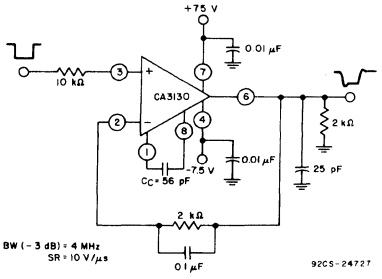
Fig.12 — Input current vs. ambient temperature.

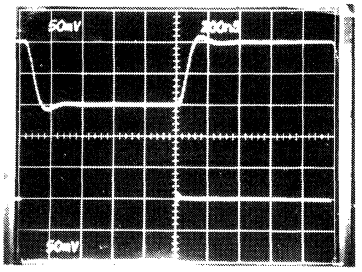
In applications requiring the lowest practical input current and incremental increases in

†For general information on the characteristics of COS/MOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "COS/MOS Transistor Array".

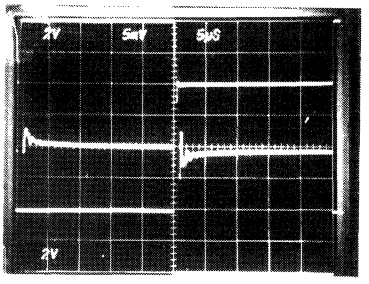
suited to service as voltage followers. Fig. 16 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 17, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 17a with input-signal ramping. The waveforms in Fig. 17b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 17b also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.





Top Trace: Output
Bottom Trace: Input
(a) Small-signal response (50 mV/div. and 200 ns/div.)



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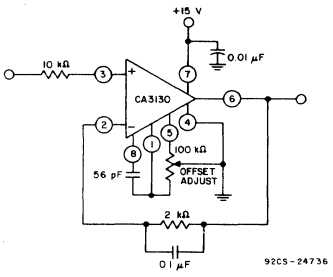
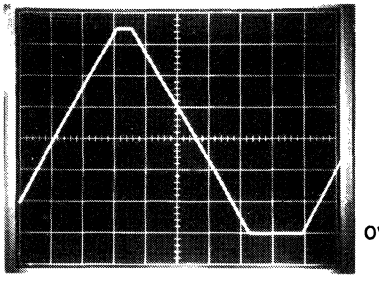
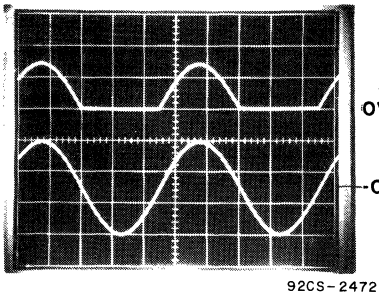
Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)
(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

Fig. 16 – Split-supply voltage follower with associated waveforms.





(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



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Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)
(b) Output-waveform with ground-reference sine-wave input

Fig. 17 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig.9 in ICAN-6080).

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.18 This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig.18.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Fig. 19. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to $-R2/R1$. When the equality of the two equations shown in Fig. 19 is satisfied, the full-wave output is symmetrical.

Peak Detectors

Peak-detector circuits are easily implemented with the CA3130, as illustrated in Fig. 20 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the

*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.

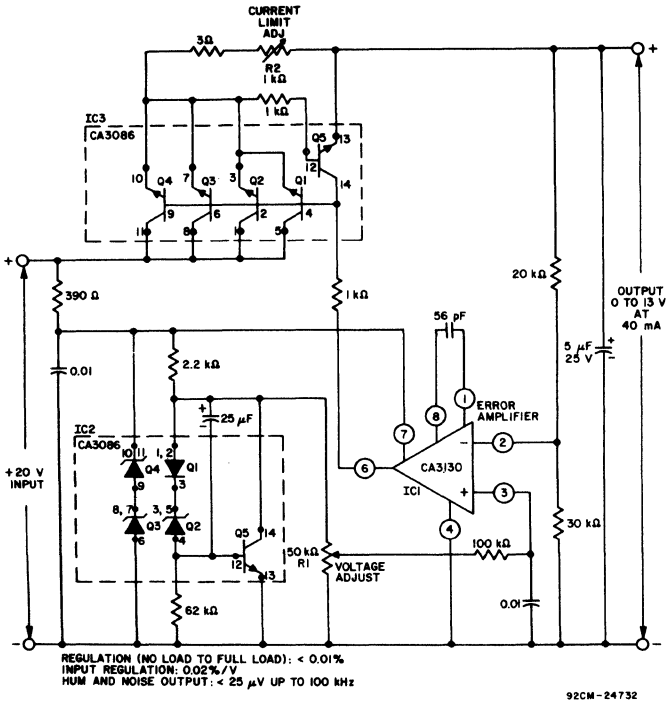


Fig.21 – Voltage regulator circuit (0 to 13 V at 40 ma).

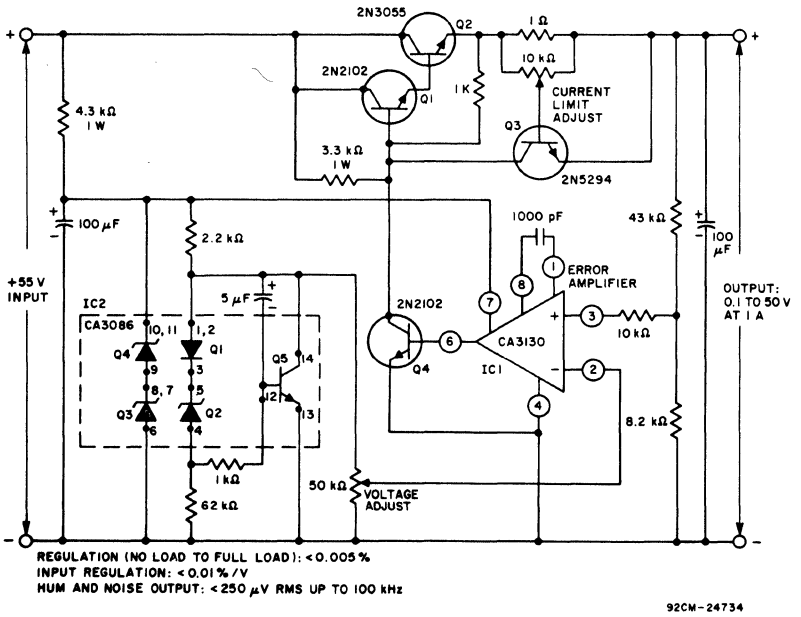


Fig.22 – Voltage regulator circuit (0.1 to 50 V at 1 A).

justment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 23. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

Fig. 24 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

*See File No. 475 and ICAN-6668.

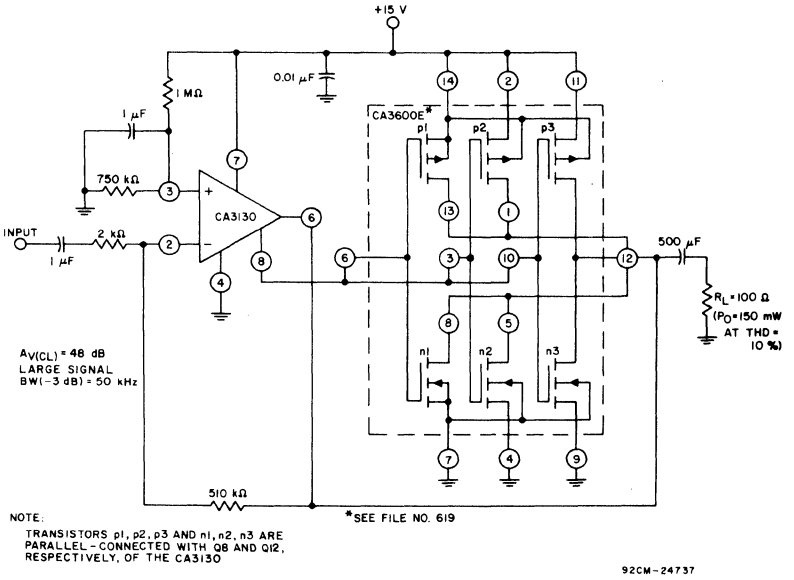
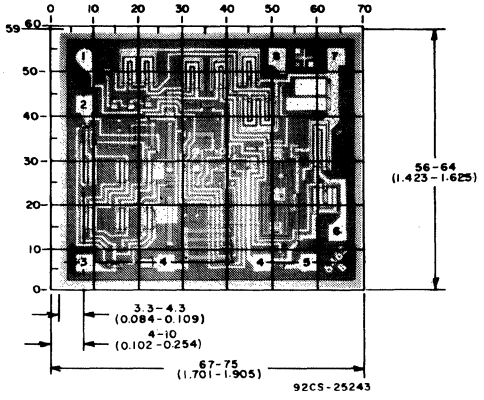


Fig. 25 – COS/MOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CA3130H.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Characteristic		Test Conditions	LIMITS						Units
			CA3138G			CA3138AG			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO}(sus)$*		I_C = 1 mA, I_B = 0	15	20	–	15	20	–	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$		I_C = 10 μA	20	55	–	25	60	–	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$		I_C = 10 μA, I_E = 0	20	55	–	25	60	–	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$		I_E = 10 μA, I_C = 0	5	7.2	–	5	7.2	–	V
Base-to-Emitter Saturation Voltage, $V_{BE}(sat)$*		I_C = 500 mA, I_B = 12.5 mA	0.7	0.81	1.1	0.7	0.81	1.1	V
Collector-to-Emitter Saturation Voltage, $V_{CE}(sat)$*		I_C=500 mA, I_B = 12.5 mA	–	0.26	0.4	–	0.26	0.4	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 15 V	–	0.03	1	–	0.02	0.1	μA
	I_{CEO}	V_{CE} = 10 V	–	0.5	–	–	0.3	1.0	
	I_{EBO}	V_{EB} = 4 V	–	0.01	–	–	0.01	0.1	
Static Forward-Current Transfer Ratio (Beta), h_{FE}*		I_C=10 mA, V_{CE} = 5 V	–	–	–	35	140	–	
		I_C = 100 mA, V_{CE} = 5 V	80	160	450	80	160	450	
		I_C = 500 mA, V_{CE} = 5 V	95	170	500	95	170	500	
		I_C = 1 A, V_{CE} = 5 V	40	170	–	40	170	–	
Small-Signal Forward Current Transfer Ratio, h_{fe}		I_C = 50 mA, V_{CE} = 10 V, f = 100 MHz	2	–	–	2	–	–	
Collector-to-Base Capacitance, C_{CB}		V_{CB} = 10 V, I_E = 0	–	18	–	–	18	–	pF
Emitter-to-Base Capacitance, C_{EB}		V_{EB} = 0.5 V, I_C = 0	–	77	–	–	77	–	pF
Rise Time (See Test Ckt. Fig. 6), t_r		I_C = 570 mA	–	6	–	–	6	–	ns
Fall Time (See Test Ckt. Fig. 6), t_f		I_{B1} = 30 mA	–	100	–	–	100	–	ns
Delay Time (See Test Ckt. Fig. 6), t_d		I_{B2} = 0	–	7.5	–	–	7.5	–	ns
Storage Time (See Test Ckt. Fig. 6), t_s			–	850	–	–	850	–	ns

*Pulse Conditions: width = 300 μs; duty cycle = 1%.

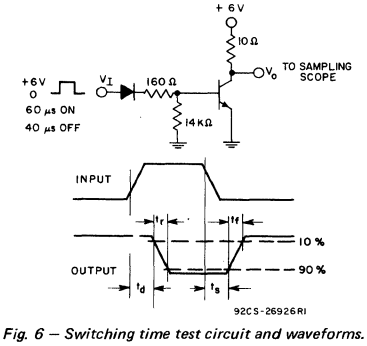


Fig. 6 – Switching time test circuit and waveforms.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25^oC$		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage Adjustment Resistor		Typ.Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}		43	18	4.7	kΩ
Input Resistance	R_I			1.5	1.5	1.5	TΩ
Input Capacitance	C_I			4	4	4	pF
Output Resistance	R_O			60	60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 39)	e_n	BW = 140 kHz, R_S = 1 MΩ		48	48	48	μV
Equivalent Input Noise Voltage (See Fig.10)	e_n	f = 1 kHz	R_S = 100 Ω	40	40	40	$nV/\sqrt{Hz}$
		f = 10 kHz		12	12	12	
Short-Circuit Current to Opposite Supply	Source I_{OM^+}			40	40	40	mA
	Sink I_{OM^-}			18	18	18	mA
Gain-Bandwidth Product, (See Figs. 5 &18)	f_T			4.5	4.5	4.5	MHz
Slew Rate, (See Fig.6)	SR			9	9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	220	220	μA
Transient Response: Rise Time	t_r	R_L = 2 kΩ, C_L = 100 pF		0.08	0.08	0.08	μs
Overshoot (See Fig. 37)				10	10	10	%
Settling Time at 10 V_{p-p}, (See Fig.17)	t_s 1 mV	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower		4.5	4.5	4.5	μs
	t_s 10 mV			1.4	1.4	1.4	

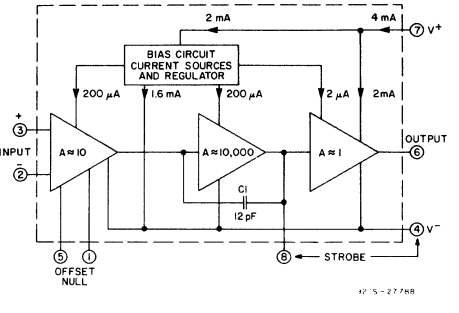


Fig.2 – Block diagram of CA3140 series.

CIRCUIT DESCRIPTION

Fig.2 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensating capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The schematic circuit diagram of the CA3140 is shown in Fig.3. It consists of a differential-input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second Stage – Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage – The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

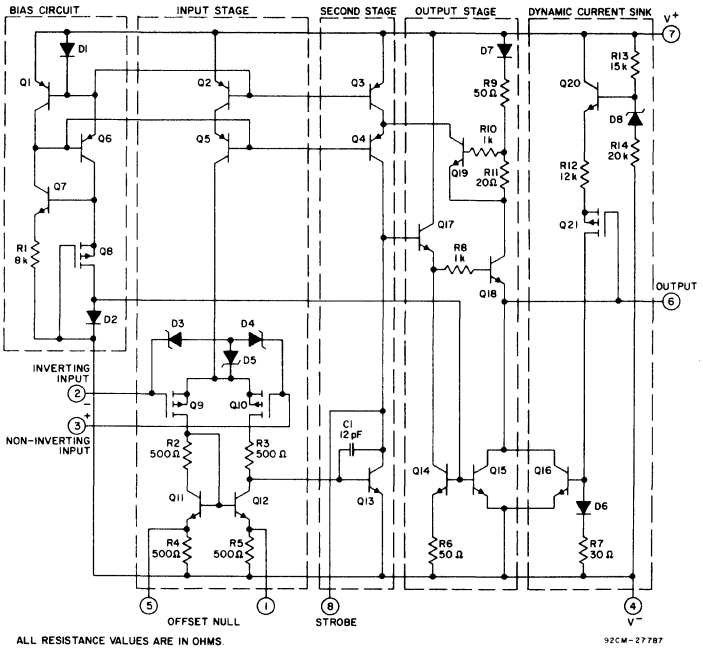


Fig.3 – Schematic diagram of CA3140 series.

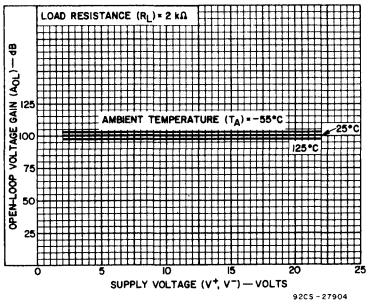


Fig.4 – Open-loop voltage gain vs supply voltage and temperature.

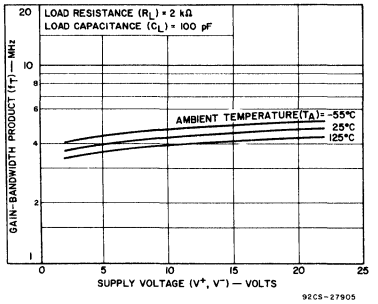


Fig.5 – Gain-bandwidth product vs supply voltage and temperature.

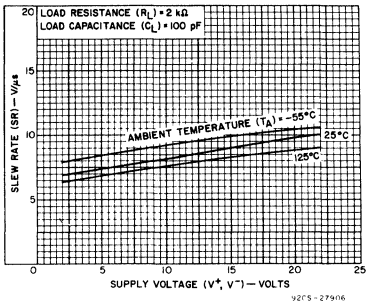


Fig.6 – Slew rate vs supply voltage andtemperature.

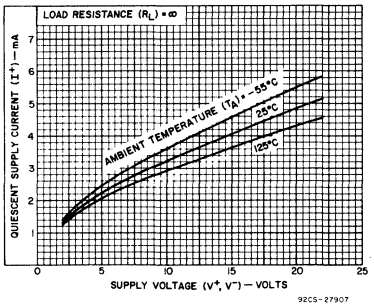


Fig.7 – Quiescent supply current vs supply voltage and temperature.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE

At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$

CHARACTERISTIC		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage	$\|V_{IO}\|$	0.8	2	5	mV
Input Offset Current	$\|I_{IO}\|$	0.1	0.1	0.1	pA
Input Current	I_I	2	2	2	pA
Input Resistance		1	1	1	TΩ
Large-Signal Voltage Gain	A_{OL}	100 k	100 k	100 k	V/V
(See Figs.4,18)		100	100	100	dB
Common-Mode Rejection Ratio,	CMRR	20	32	32	μV/V
		94	90	90	dB
Common-Mode Input-Voltage Range	V_{ICR}	−0.5	−0.5	−0.5	V
(See Fig.20)		2.6	2.6	2.6	
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	32	100	100	μV/V
		90	80	80	dB
Maximum Output Voltage	V_{OM}^+	3	3	3	V
(See Figs.13,20)	V_{OM}^-	0.13	0.13	0.13	
Maximum Output Current:					
Source	I_{OM}^+	10	10	10	mA
Sink	I_{OM}^-	1	1	1	
Slew Rate (See Fig.6)		7	7	7	V/μs
Gain-Bandwidth Product (See Fig.5)	f_T	3.7	3.7	3.7	MHz
Supply Current (See Fig.7)	I^+	1.6	1.6	1.6	mA
Device Dissipation	P_D	8	8	8	mW
Sink Current from Term. 8 to Term. 4 to Swing Output Low		200	200	200	μA

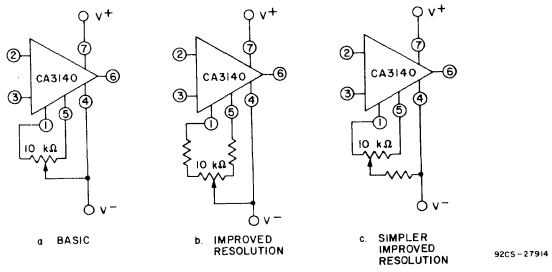


Fig.15 – Three offset-voltage nulling methods.

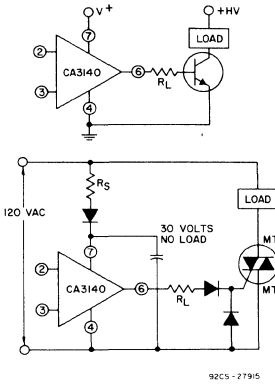


Fig.16 – Methods of utilizing the $V_{CE(sat)}$ sinking-current capability of the CA3140 series.

BANDWIDTH AND SLEW RATE

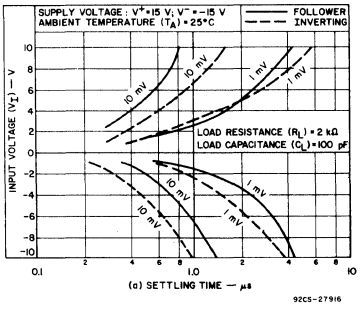
For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open-loop −3 dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Fig.17 shows the typical settling time required to reach 1 mV or 10 mV of the final value for various levels of large signal inputs for the voltage-follower and inverting unity-gain amplifiers. The exceptionally fast settling time characteristics shown in Fig.18 are largely due to the high combination of high gain and wide bandwidth of the CA3140.

INPUT CIRCUIT CONSIDERATIONS

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.



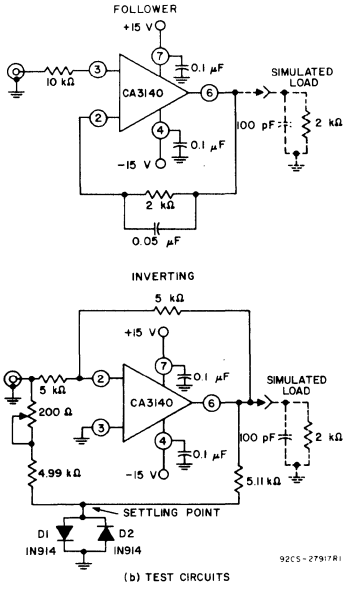


Fig.17 – Input voltage vs settling time.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig.19 shows typical input-terminal current versus ambient temperature for the CA3140.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Fig.14 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetircal, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar a transistor input stage.

SUPER SWEEP FUNCTION GENERATOR

A function generator having a wide tuning range is shown in Fig.21. The 1,000,000/1 adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting read-out amplifier of the tri-

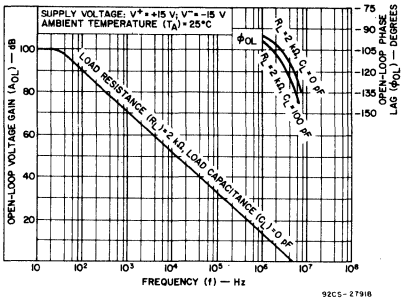


Fig.18 – Open-loop voltage gain and phase lag vs frequency.

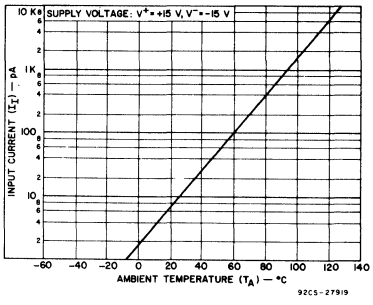


Fig.19 – Input current vs ambient temperature.

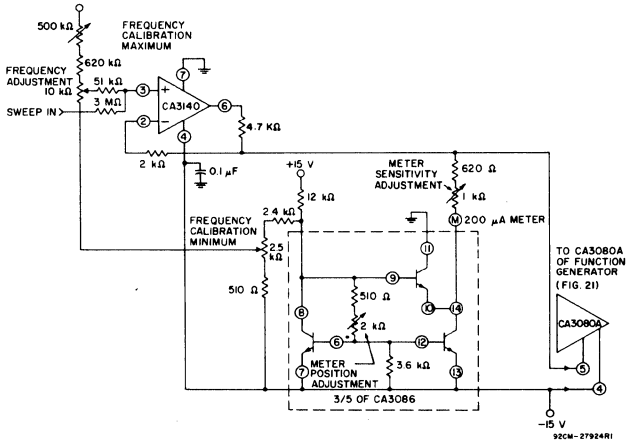


Fig. 22 – Meter driver and buffer amplifier.

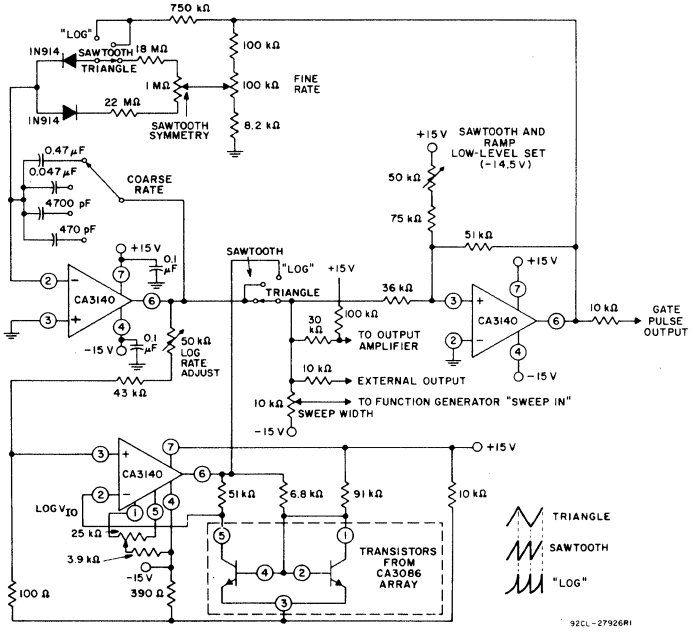


Fig. 24 – Sweeping generator.

establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necesary.

Two adjustments are used for the meter. The meter sensitivity control sets the meter-scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects 1/6 of full scale for each decade change in frequency.

SINE-WAVE SHAPER

The circuit shown in Fig. 23 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero-crossing slope is established by the 10-kΩ

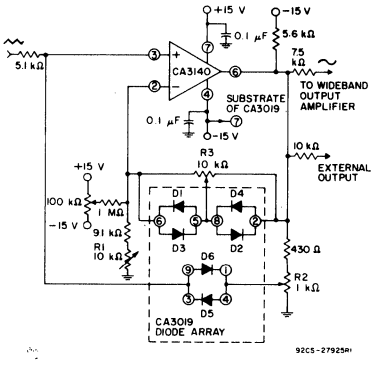


Fig. 23 – Sine-wave shaper.

potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1-kΩ resistor and 10-kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage-follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine-wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessarv

SWEEPING GENERATOR

Fig. 24 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

WIDEBAND OUTPUT AMPLIFIER

Fig. 25 shows a high-slew-rate, wideband amplifier suitable for use as a 50-ohm transmission-line driver. This circuit, when used in conjunction with the function generator and sine-wave shaper circuits shown in Figs. 21 and 23 provides 18 volts peak-to-peak output open-circuited, or 9 volts peak-to-peak output when terminated in 50 ohms. The slew rate required of this amplifier is 28 volts/μs (18 volts peak-to-peak x π x 0.5 MHz).

system is a serious consideration, the more usual current-sampling resistor-type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series-pass element for the conventional current-limiting system, Fig. 27, because high-power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat-sink VERSAWATT transistor is used as the series-pass element in the foldback current system, Fig.28, since dissipation levels will only approach 10 watts. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3 kΩ and 100 kΩ divider network connected to the base of the current-sensing transistor.

Both regulators, Figs. 27 and 28, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200 μV as read with a meter having a 10-MHz bandwidth.

Fig.31 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn-on rise is due to the slow rate of rise of the reference voltage. Fig. 29 (b) shows the transient response of the regulator with the switching of a 20-Ω load at 20 volts output.

TONE CONTROL CIRCUITS

High-slew-rate, wide-bandwidth, high-output voltage capability and high input impedance are all characteristics required of tone-control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figs. 30 and 31.

The first circuit, shown in Fig. 31, is the Baxandall tone-control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small-size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ± 15 dB at 100 Hz and 10 kHz, respectively. Full peak-to-peak output is available up to at least 20 kHz due to the high slew rate of the CA3140. The amplifier gain is −3 dB down from its "flat" position at 70 kHz.

Fig. 30 shows another tone-control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20-dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No.3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No.3, August, 1972.

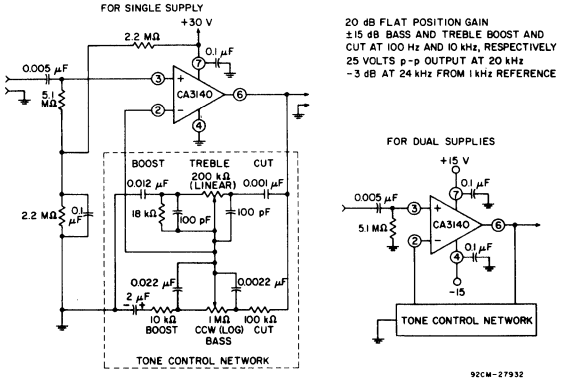


Fig. 30 — Tone control circuit using CA3130 series (20-dB midband gain).

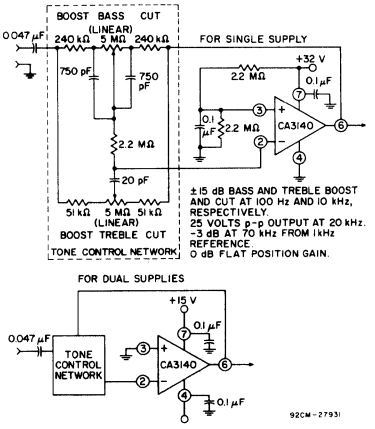


Fig. 31 — Baxandall tone control circuit using CA3140 series.

WIEN BRIDGE OSCILLATOR

Another application of the CA3140 that makes excellent use of its high input-impedance, high-slew-rate, and high-voltage qualities is the Wien Bridge sine-wave oscillator. A basic Wien Bridge oscillator is shown in Fig. 32. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/2\pi RC$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain-bandwidth product of the CA3140.

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

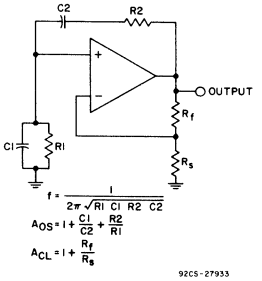


Fig. 32 — Basic Wien bridge oscillator circuit using an operational amplifier.

Fig. 33 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_f of Fig. 32). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1-μF polycarbonate capacitors and 22 MΩ for the frequency determining network, the operating frequency is 0.007 Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180 kHz will reach a slew rate of approximately 9 volts/μs when its amplitude is 16 volts peak-to-peak.

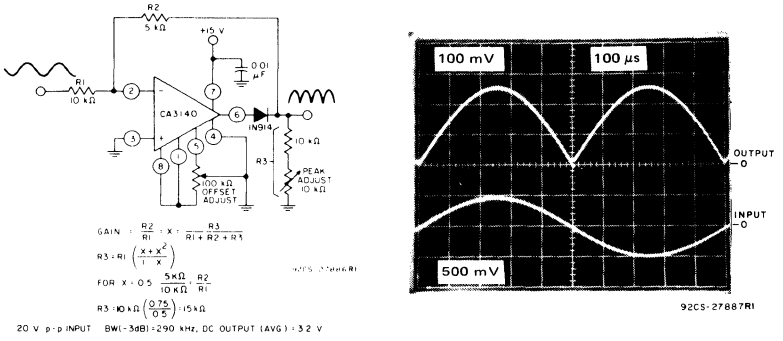


Fig. 37 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

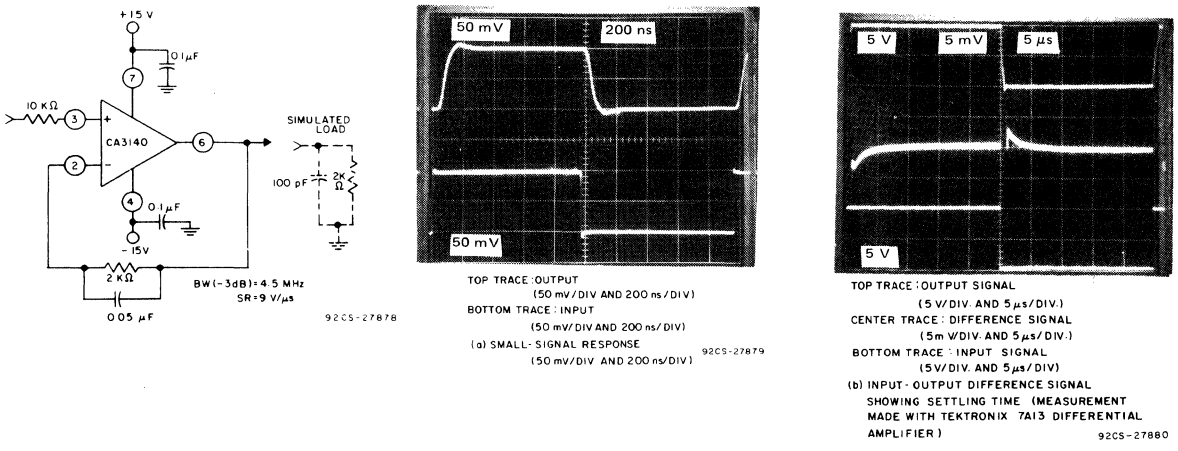


Fig. 38 — Split-supply voltage-follower test circuit and associated waveforms.

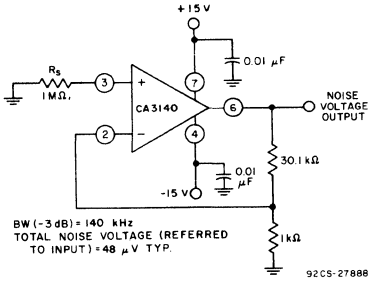
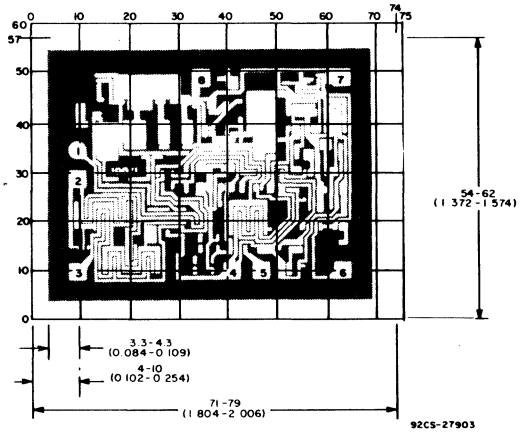


Fig. 39 — Test circuit amplifier (30-dB gain) used for wideband noise measurement.



CA3140H Chip

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

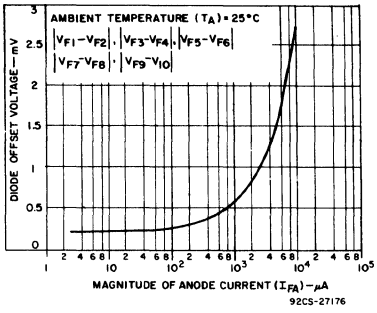


Fig. 4 — Diode offset voltage vs. magnitude of anode current.

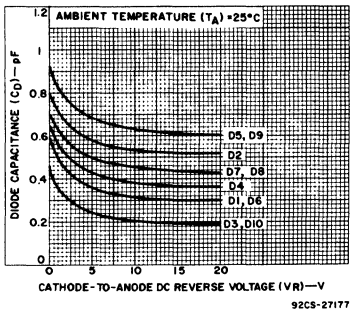


Fig. 5 — Diode capacitance vs. cathode-to-anode reverse voltage.

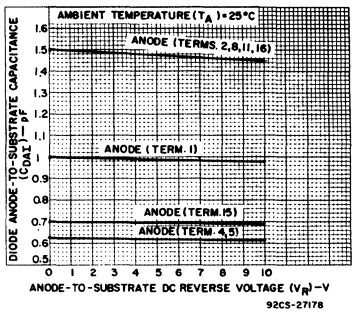


Fig. 6 — Diode anode-to-substrate capacitance vs. reverse voltage.

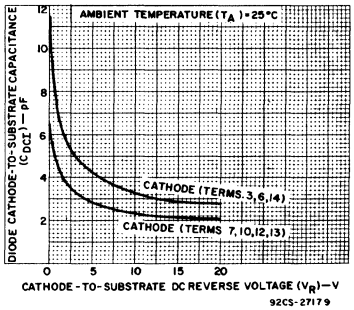


Fig. 7 — Diode cathode-to-substrate capacitance vs. cathode-to-substrate DC reverse voltage.

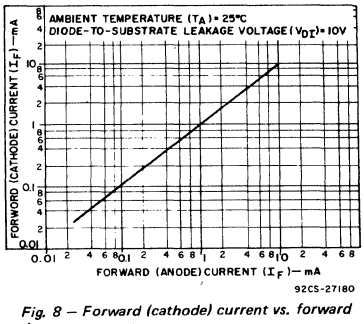


Fig. 8 — Forward (cathode) current vs. forward (anode) current.

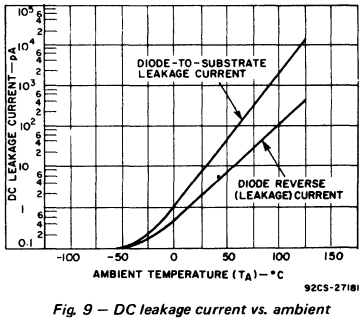


Fig. 9 — DC leakage current vs. ambient temperature.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC INPUT VOLTAGE... (V^+ +8 V) to (V^- –0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK –
UP TO 55°C ..... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK –
AT 125°C ..... 418 mW
BELOW 125°C ... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (All Types).... –55 to +125°C
STORAGE (All Types) ..... –65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS									Units
	CA3160B (T, S)			CA3160A (T, S, E)			CA3160 (T, S, E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.8	2	–	2	5	–	6	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	20	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 V_{p-p}, R_L=2 kΩ	100	110	–	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	86	100	–	80	95	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	–0.5 to 12	10	0	–0.5 to 12	10	0	–0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	100	–	32	150	–	32	320	μV/V
Maximum Output Voltage:										
At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	12	13.3	–	V
V_{OM}^-	–	0.002	0.01	–	0.002	0.01	–	0.002	0.01	
At R_L=∞ V_{OM}^+	14.99	15	–	14.99	15	–	14.99	15	–	
V_{OM}^-	–	0	0.01	–	0	0.01	–	0	0.01	
Maximum Output Current:										
I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	12	20	45	
Supply Current, I^+:										
V_O=7.5 V, R_L=∞	–	10	15	–	10	15	–	10	15	mA
V_O = 0 V, R_L =∞	–	2	3	–	2	3	–	2	3	
Input Current, I_I*	–	Fig.11	15	–	Fig.11	–	–	Fig.11	–	nA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	5	15	–	6	–	–	8	–	μV/°C
Large-Signal Voltage Gain, A_{OL}*	50 k	320 k	–	–	320 k	–	–	320 k	–	V/V
	94	110	–	–	110	–	–	110	–	dB

* T_A = –55 to +125°C, $V^{\pm}$ = ±7.5 V (I_I and $\Delta V_{IO}/\Delta T$), V_O = 10 V_{p-p} and R_L = 2 kΩ (A_{OL}).

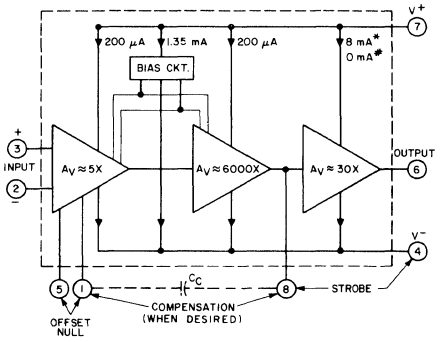
CIRCUIT DESCRIPTION

Fig.3 is a block diagram of the CA3160 series COS/MOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3160 series circuits are ideal for single-supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in Fig.3, provide the total gain of the CA3160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive COS/MOS digital circuits in comparator applications).

Input Stages – The circuit of the CA3160 is shown in Fig.1. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-Stage – Most of the voltage gain in the CA3160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30-pF capacitor and 2-kΩ resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit – At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
* WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4
# WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

Fig. 3 – Block diagram of the CA3160 Series.

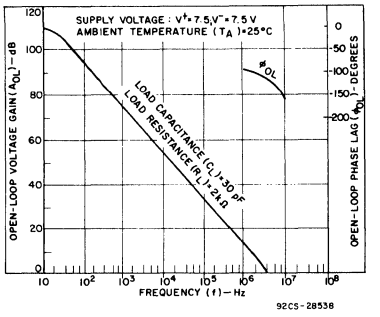


Fig.4 – Open-loop voltage gain and phase shift vs. frequency for various values of C_L and R_L.

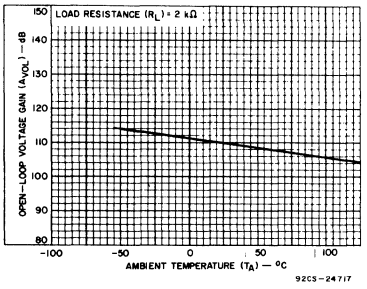


Fig.5 – Open-loop gain vs. temperature.

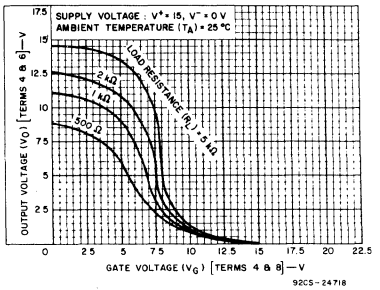


Fig.6 – Voltage transfer characteristics of COS/MOS output stage.

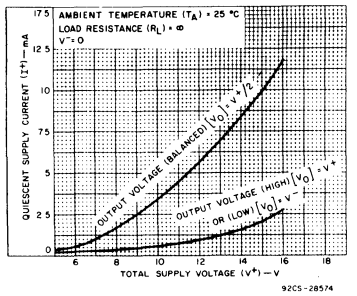


Fig.7 – Quiescent supply current vs. supply voltage.

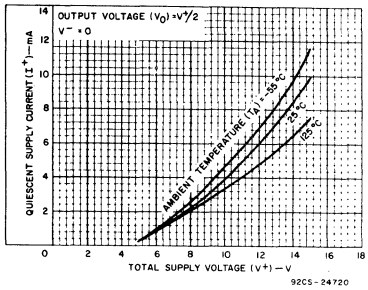


Fig.8 – Quiescent supply current vs. supply voltage at several temperatures.

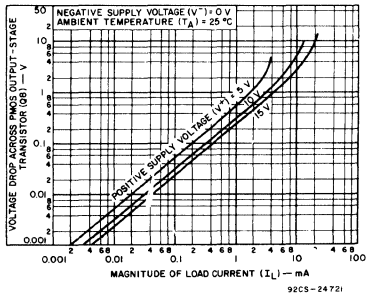


Fig.9 – Voltage across PMOS output transistor (Q8) vs. load current.

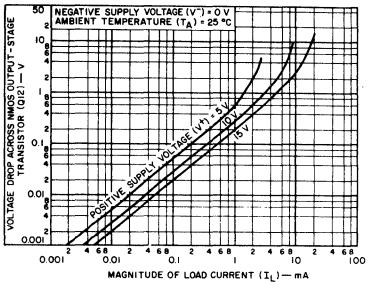


Fig.10 – Voltage across NMOS output transistor (Q12) vs. load current.

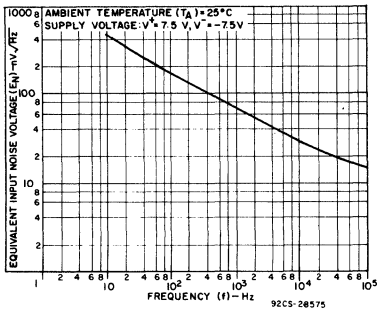


Fig.11 – Equivalent noise voltage vs. frequency.

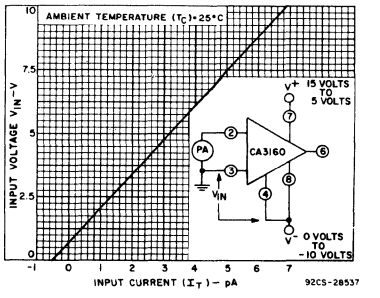


Fig.12 – Input current vs. common-mode voltage.

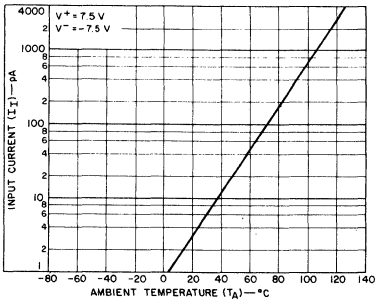


Fig. 13 – Input current vs. ambient temperature.

This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

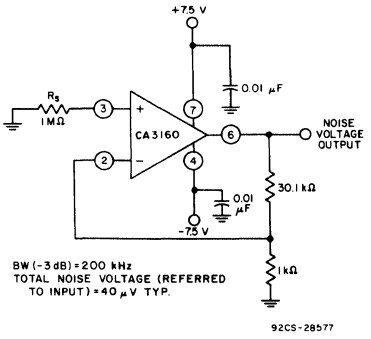


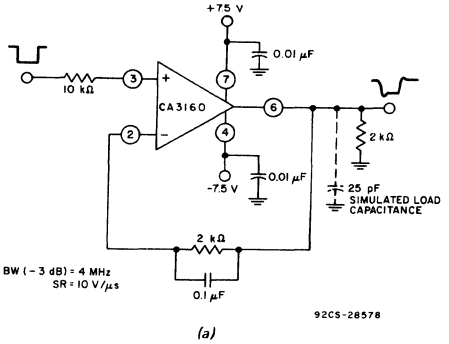
Fig. 16 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

TYPICAL APPLICATIONS

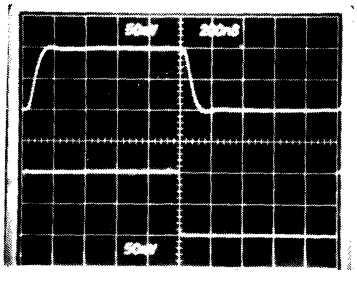
Voltage Followers

Operational amplifiers with very high input resistances, like the CA3160, are particularly suited to service as voltage followers. Fig.17 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3160 in a split-supply configuration.

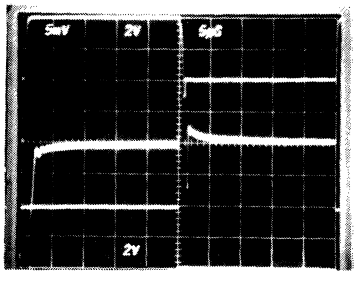
A voltage follower, operated from a single supply, is shown in Fig.18 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig.18b with input-signal ramping. The waveforms in Fig.18c show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig.18c also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3160 in a single-supply voltage-follower application.



(a)



(b) Small Signal Response
Top Trace: Output
Bottom Trace: Input



(c) Input-Output Difference Signal Showing Settling Time
Top Trace: Output Signal
Center Trace: Difference Signal 5 mV/div
Bottom Trace: Input Signal

Fig. 17 – Split-supply voltage follower with associated waveforms.

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.19. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with COS/MOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig.19.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Error-Amplifier in Regulated Power Supplies

The CA3160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Fig.20 uses a CA3160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero volts with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

* "Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.

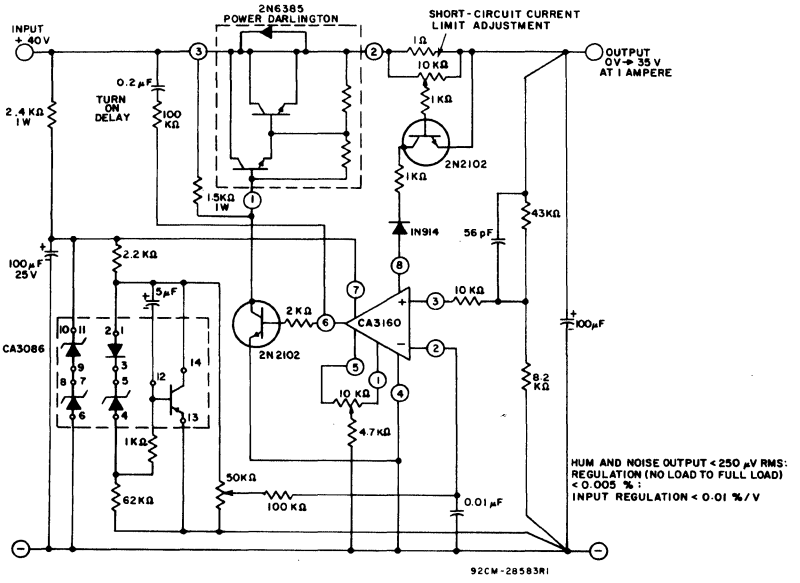


Fig.20 – Voltage regulator circuit (0.1 to 35 V at 1 A).

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig.21. The oscillator operates with a tracking error in the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (terminal 6) of A_1 (a CA3130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{avg} = V\ T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{avg} = V1$. This circuit condition is accomplished by feeding an output signal from terminal 6 of A_2 through R_4, D_4 to the inverting terminal (terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig.22 illustrates an application in which a number of the CA3160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10 KΩ current-limiting resistor. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

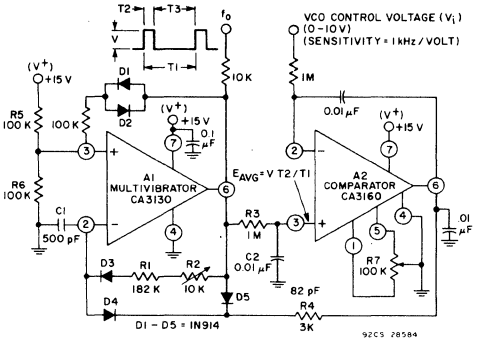


Fig.21 – Voltage-controlled oscillator.

Function Generator

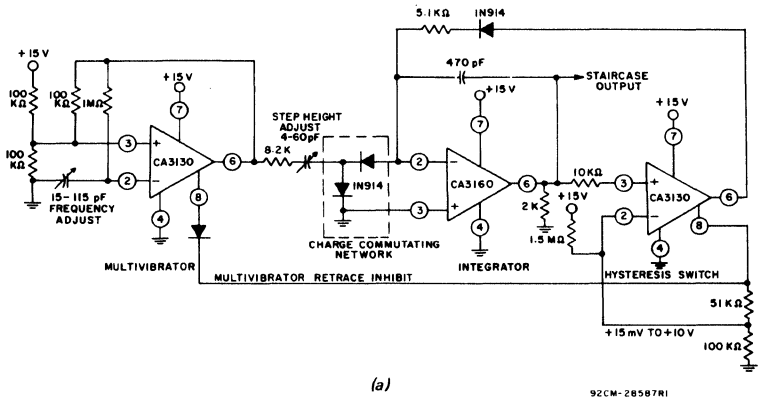
A function generator having a wide tuning range is shown in Fig.23. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA3160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500 kHz and 1 MHz. Capacitors C4, C5, and the trimmer potentiometer in series with C5 maintain essentially constant (±10%) amplitude up to 1 MHz.

Staircase Generator

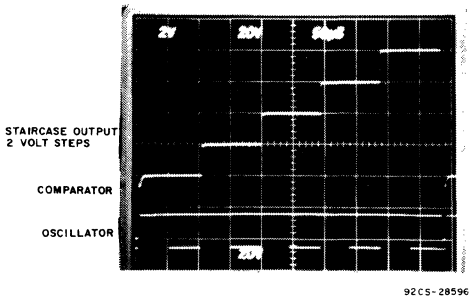
Fig.24 shows a staircase generator circuit utilizing three COS/MOS operational amplifiers. Two CA3130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA3160, is used as a linear staircase generator.

Picoammeter Circuit

Fig. 25 is a current-to-voltage converter configuration utilizing a CA3160 and CA3140 to provide a picoampere meter for ±3 pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA3160 at ground potential,



(a)



(b) — Staircase Generator Waveform
Top Trace: Staircase Output
2 Volt Steps
Center Trace: Comparator
Bottom Trace: Oscillator

Fig. 24 — Staircase generator.

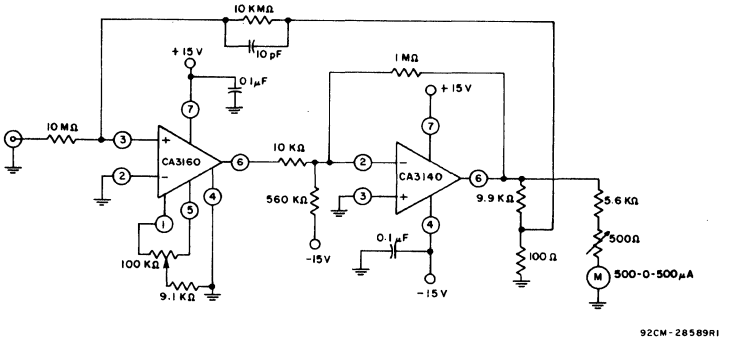


Fig.25 — Current-to-voltage converter to provide a picoammeter with ± 3 pA full-scale deflection.

output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9-KΩ resistor in series with a 100-ohm resistor sets the voltage at the 10-KMΩ resistor (in series with Terminal 3) to ±30 mV full-scale deflection. This 30-mV signal results from ±3 volts appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9 KΩ and 100-ohm network similar to that used in voltmeter circuit shown in Fig. 22, a current range of 3 pA to 1 nA full scale can be handled with the single 10-KMΩ resistor.

Single-Supply Sample-and-Hold System

Fig. 26 shows a single-supply sample-and-hold system using a CA3160 to provide a high input impedance and an input-voltage range of 0 to 10 volts. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100-KΩ bias-voltage potentiometer on the positive input of the CA3080A. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320 mV at the amplifier bias circuit terminal (5) at least ± 100 pA of output current will be available.

Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA3160 is shown in Fig. 27. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1 volts. The 500-ohm potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA3160 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig.28, three COS/MOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA3160. In the Class A mode of CA3600E shown, a typical device consumes

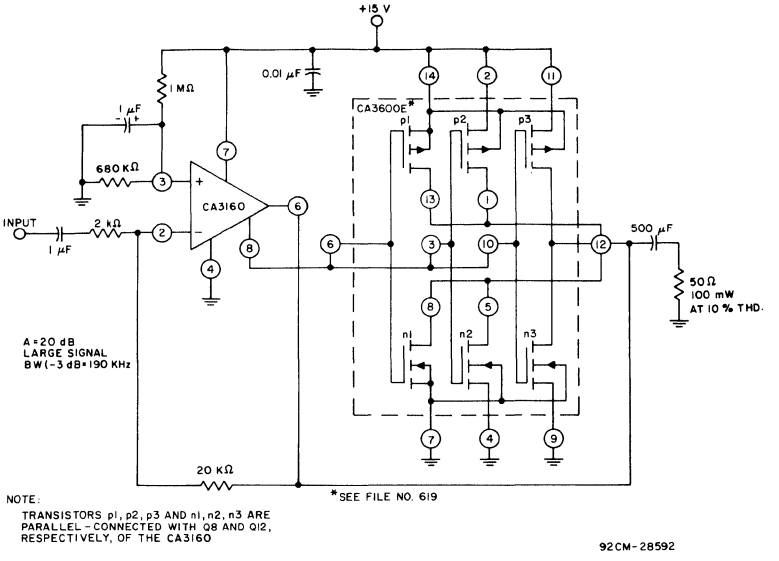
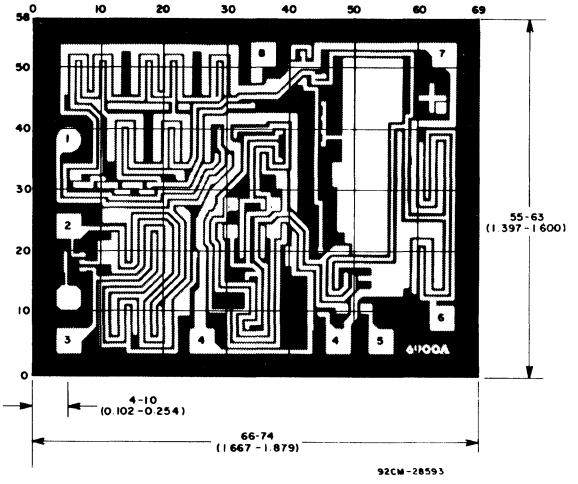


Fig.28 – COS/MOS transistor array (CA3600E) connected as power booster in the output stage of the CA3160.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photograph and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

TRUTH TABLE

BINARY STATE	INPUTS				OUTPUTS							DISPLAY
	2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	L	L	L	L	L	L	L	L	L	L	H	0
1	L	L	L	H	H	L	L	H	H	H	H	1
2	L	L	H	L	L	L	H	L	L	H	L	2
3	L	L	H	H	L	L	L	L	H	H	L	3
4	L	H	L	L	H	L	L	H	H	L	L	4
5	L	H	L	H	L	H	L	L	H	L	L	5
6	L	H	H	L	L	H	L	L	L	L	L	6
7	L	H	H	H	L	L	L	H	H	H	H	7
8	H	L	L	L	L	L	L	L	L	L	L	8
9	H	L	L	H	L	L	L	L	H	L	L	9
10	H	L	H	L	H	H	H	H	H	H	L	—
11	H	L	H	H	L	H	H	L	L	L	L	E
12	H	H	L	L	H	L	L	H	L	L	L	H
13	H	H	L	H	H	H	H	L	L	L	H	L
14	H	H	H	L	L	L	H	H	L	L	L	P
15	H	H	H	H	H	H	H	H	H	H	H	BLANK

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 7 and 14) . . . . . +7 V
INPUT VOLTAGE (terminal 10 or 11 to ground) . . . . . ±15 V
DEVICE DISSIPATION:
Up to T_A = +55°C . . . . . 750 mW
Above T_A = +55°C . . . . . derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating . . . . . 0 to +75°C
Storage . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0/79 mm) from case for 10 seconds max. . . . . +265°C

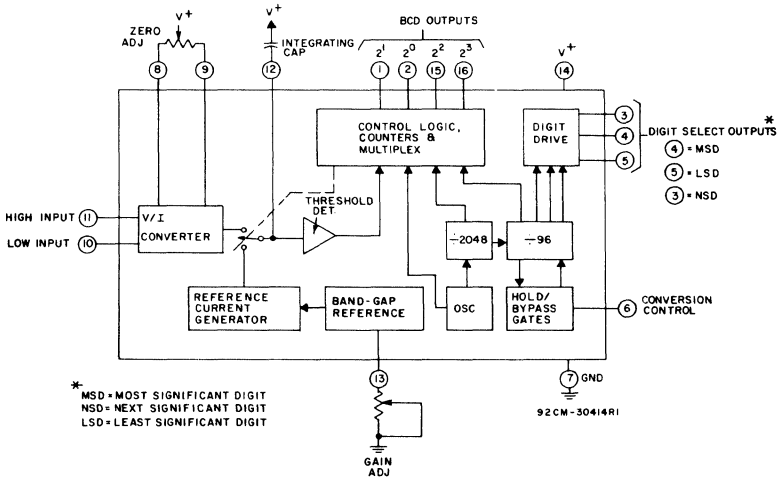


Fig. 1 – Functional block diagram of the CA3162E.

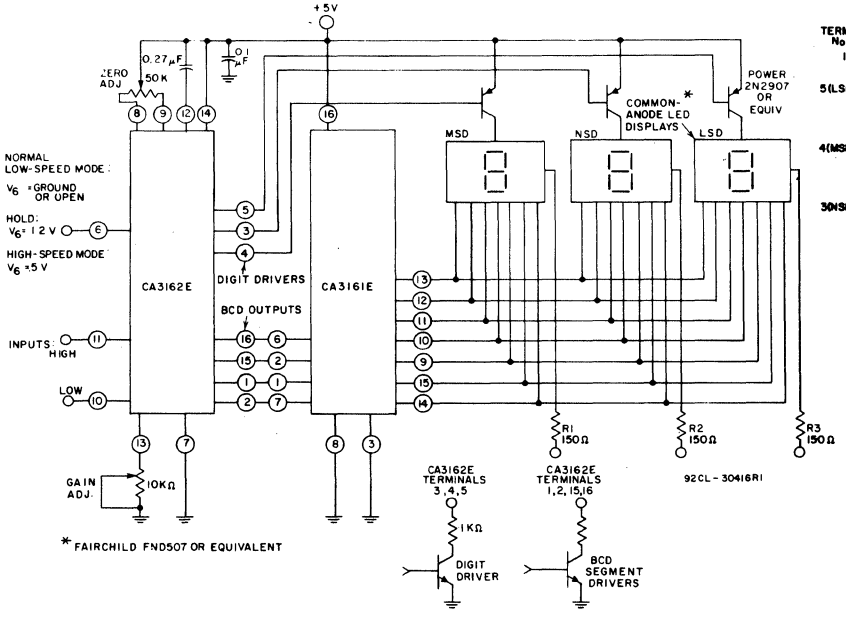


Fig. 2 – Basic digital readout system using the CA3162E and the CA3161E.

that the multiplex rate is unchanged. Fig. 3 shows the timing of conversion and digit select pulses for the high-speed mode. Note that the basic A/D conversion process requires approximately 5 ms in both modes.

The "EEE" or "___" displays indicate that the range of the system has been exceeded in the positive or negative direction, respectively. Negative voltages to −99 mV are displayed with the minus sign in the MSD. The BCD code is 1010 for a negative overrange (___) and 1011 for a positive overrange (EEE).

System Application

Fig. 2 is the block diagram of a basic system using the CA3162E and the CA3161E. An actual-size PC board layout for this circuit is shown in Fig. 4. The BCD outputs of the CA3162E drive the BCD inputs of the CA3161E BCD-to-7-segment decoder directly. The seven-segment outputs are multiplexed to the three LED displays. The digits are selected by terminals 3, 4, and 5 (CA3162E), which provide base current to the external p-n-p transistors. The p-n-p's, in turn, provide current to the anodes of the display. Adjustment procedures for the gain and zero potentiometers are given in Note 1 of the Electrical Characteristics chart.

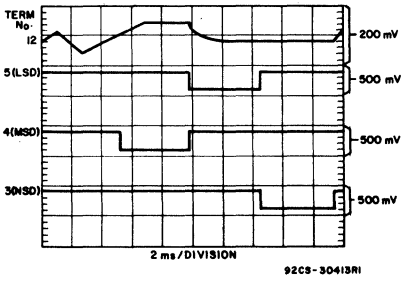


Fig. 3 – High speed mode timing diagram.

CA3162E Liquid Crystal Display (LCD) Application

Fig. 6 shows the CA3162E in a typical LCD application. LCD's may be used in favor of LED displays in applications requiring lower power dissipation, such as battery-operated equipment, or when visibility in high-ambient-light conditions is desired.

Multiplexing of LCD digits is not practical, since LCD's must be driven by an ac signal and the average voltage across each segment is zero. Three CD4056B liquid-crystal decoder/drivers are therefore used. Each CD4056B contains an input latch so that the BCD data for each digit may be latched into the decoder using the inverted digit-select outputs of the CA3162E as strobes.

Inverters G1 and G2 are used as an astable multivibrator to provide the ac drive to the LCD backplane. Inverters G3, G4, and G5 are the digit-select inverters and require pull-up resistors to interface the open-collector outputs of the CA3162E to COS/MOS logic. The BCD outputs of the CA3162E may be connected directly to the corresponding CD4056B inputs (using pull-up resistors). In this arrangement, the CD4056B decodes the negative sign (–) as an "L" and the positive overload indicator (E) as an "H".

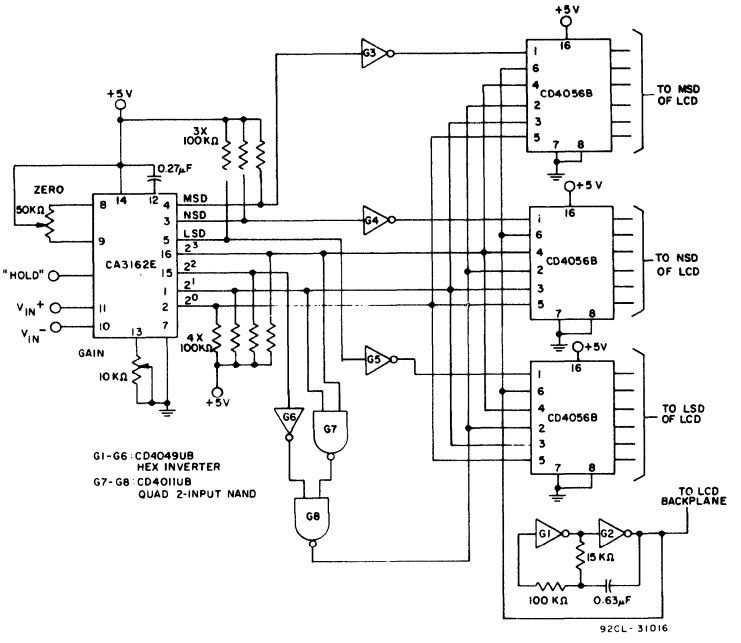


Fig. 6 – Typical LCD application.

CA3162E Common-Cathode, LED Display Application

Fig. 7 shows the CA3162E connected to a CD4511B decoder/driver to operate a common-cathode LED display. Unlike the CA3161E, the CD4511B remains blank for all BCD codes greater than nine. After 999 mV the display blanks rather than displaying EEE, as with the CA3161E. When displaying negative voltage, the first digit remains blank instead of (–), and during a negative overrange the display blanks.

The additional logic shown within the dotted area of Fig. 7 restores the negative sign (–), allowing the display of negative numbers as low as –99 mV. Negative overrange is indicated by a negative sign (–) in the MSD position. The rest of the display is blanked. During a positive overrange, only segment b of the MSD is displayed.

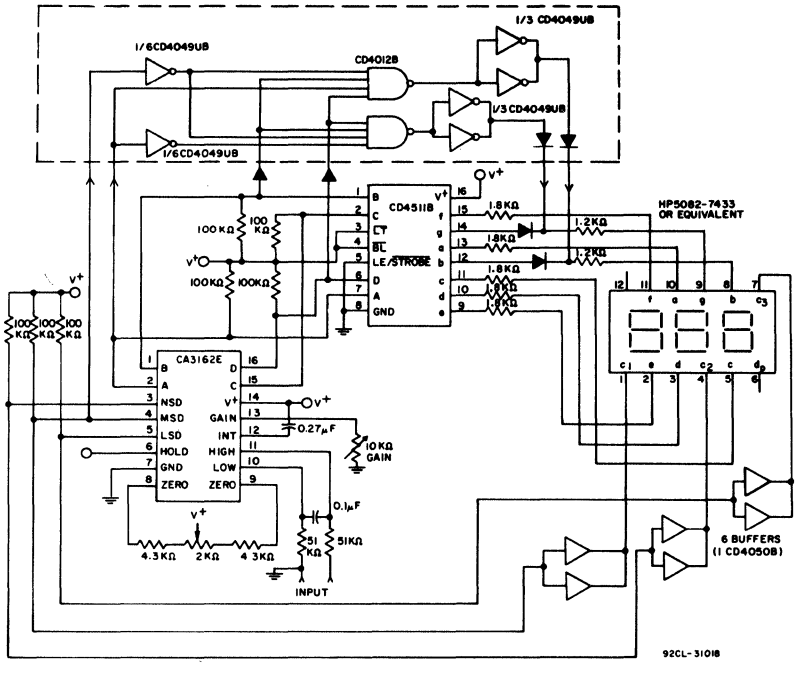


Fig. 7 – Typical common-cathode LED application.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 9 V

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Operating Voltage		7	9	11	V
Common-Mode Input Voltage Range, V_{ICR}	(V^+ –2 V) = 7 V	0	–	7	V
Low-Battery Trigger Voltage	External adjust (increase only)	7.3	7.7	7.9	V
Horn Driver $V_{CE(SAT)}$	Term. 8 = 100 mA	–	0.5	–	V
	Term. 8 = 300 mA	–	1	–	
Reference Voltage		5.8	6.2	6.6	V
Input Leakage Current, I_L	Term. 2	–	–	1	pA
	Term. 2 at 50°C	–	–	2.5	
	Term. 3	–	–	50	
Standby Current (13 MΩ from Term. 4 to gnd)	No LED connected	–	8*	12	μA
	LED connected–20 mA for 30 ms every 60s	–	18	–	
	Photoelectric operation – LED photocurrent = 0.6 A (5 sec. rate)	–	13	–	
Reference Source Current		5	–	–	μA
LED Driver Sink Current		40	50	–	mA
Interconnect Current Source	I_{Sink} = 10 μA typ.	–	2.8	–	mA
Sink	I_{Source} = 1.3 mA typ.	–	50	–	μA
Low-Battery Adjust, Term.5 Input Current		50	70	100	nA
Timing Current	Term. 13	10	–	50	nA
LED Blink Period	Adjustable	–	–	1	PPM
LED Pulse Width	Fixed	–	30	–	ms
Remote Fan-Out		20	–	–	
Alarm Pulse Duty Cycle (4.7 MΩ from Term. 11 to gnd	On-time	–	95	–	%
	On-time = 95%	–	0.5	–	sec.
	Off-time = 5%	–	0.026	–	

* Adjustable to 5 μA

OPERATING MODES TRUTH TABLE

Condition	Smoke Ionization Chamber	Low Battery	Led 6	Alarm Horn 8	Alarm Enable Pulser 11	System Interconnect 12	Remote Unit Status
Normal	No	No	Blink	Off	X	Low	Off
Low Battery	No	Yes	Blink	Beep	X	Low	Off
Smoke In Chamber	Yes	X	On	Pulsed*	Resistor to ground	High	On
External Input A1 From Remote Unit	No	No	Blink	On**	High	High	On

** Alarm Horn follows mode programmed for internal system input. For example, if terminal 11 has resistor connected to ground, horn will beep. If terminal 11 is connected to V^+, horn will be "on."

X = Don't Care

Blink & Beep = 30 msec (fixed) every 50 sec (ADJ)

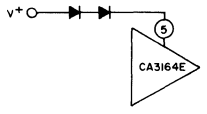
Pulsed = 95% "on" time – Period is determined by resistor from terminal 11 to ground-5% Off Time

* Horn "Continuous" if terminal 11 is connected to V^+

Connections for Optional Functions

1. Low Battery Adjustment – Terminal 5

Add diodes as shown below to increase the the low-battery trigger point.



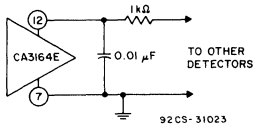
2. Sounder Operating Mode

Continuous sound on alarm – connect terminal 11 to V^+.

Pulsed sound on alarm – connect resistor between terminal and ground.

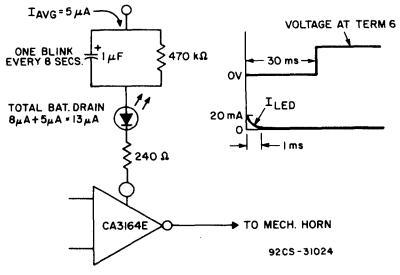
3. Remote (Interconnect)

Connect terminal 12 to same terminal on all other units (fan out = 20 units). When interconnecting units for the remote-alarm function, the extremely low currents involved make it extremely important that a provision be made for limiting externally induced transients into the remote terminal. For example, inadvertent contact with external power sources or electrical storm activity may cause triggering of the remote alarm function. The circuit below will reduce the possibility of such occurences.



4. LED On-Time Adjustment

Option 1: The CA3164E is designed to provide a fixed LED on-time of approximately 30 ms. For applications requiring a reduction in on-time the following circuit is recommended:



This circuit reduces the LED on-time but does not affect the horn on-time of 30 ms. When using this configuration during the continuous-alarm mode (smoke in chamber) the LED will be off instead of on, as shown in the truth table. If the horn is pulsed during the alarm mode, the LED will blink at the pulse rate.

Dual BiMOS Operational Amplifiers

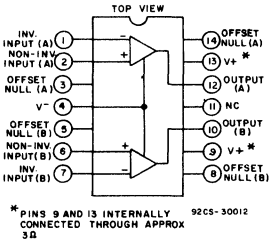
With MOS/FET Input, Bipolar Output

The RCA-CA3240A and CA3240 are dual versions of the popular CA3140-series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5 V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

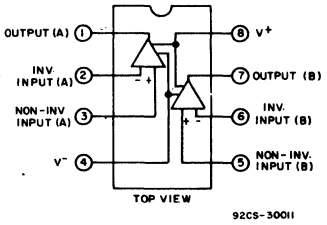
The CA3240A and CA3240 are supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix), and in the 14-lead dual-in-line plastic package (E1 suffix). They are pin-compatible with the industry standard 747 and 1458 operational amplifiers in similar packages. The CA3240A and CA3240 have an operating-temperature range of −40 to +85°C. The offset null feature is available only when these types are supplied in the 14-lead dual-in-line plastic package (E1 suffix).

Features:

- **Dual version of CA3140**
- **Internally compensated**
- **MOS/FET input stage**
  - **(a) Very high input impedance (Z_{IN}) − 1.5 TΩ typ.**
  - **(b) Very low input current (I_I) − 10 pA typ. at ± 15 V**
  - **(c) Wide common-mode input-voltage range (V_{ICR}) − can be swung 0.5 volt below negative supply-voltage rail**
  - **(d) Rugged input stage − bipolar diode protected**
- **Directly replaces industry types 747 and 1458 in most applications**
- **Operation from 4-to-36 volts single or dual supplies**
- **Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts**
- **Wide bandwidth − 4.5 MHz unity gain at ± 15 V or 30 V**
- **High voltage-follower slew rate − 9 V/μs**
- **Output swings to within 0.5 volt of negative supply at $V^+ = 5$ V, $V^- = 0$**



E1 Suffix
Pin compatible with the industry-standard 747



E Suffix
Pin compatible with the industry-standard 1458

Fig. 1 − Functional diagrams.

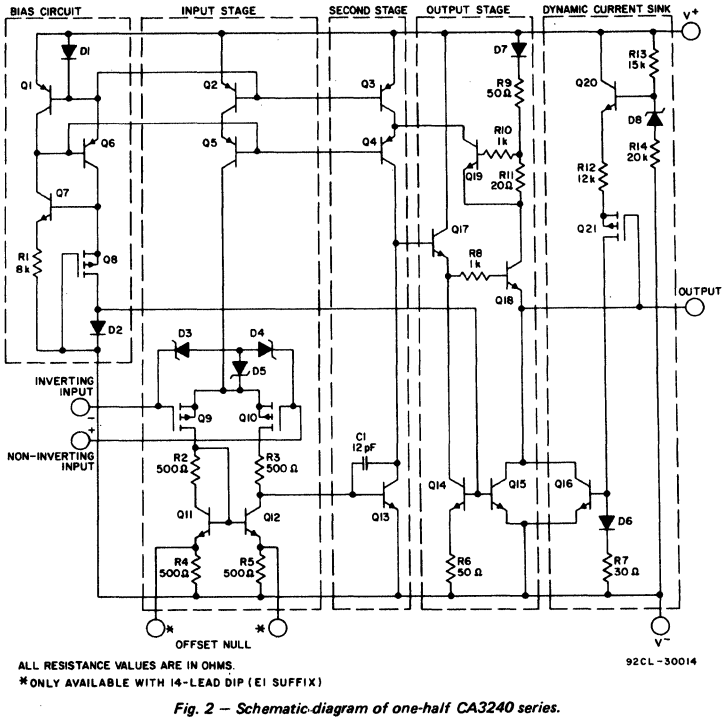


Fig. 2 − Schematic diagram of one-half CA3240 series.

Applications:

- **Ground-referenced single-supply amplifiers in automobile and portable instrumentation**
- **Sample and hold amplifiers**
- **Long-duration timers/multivibrators (microseconds−minutes−hours)**
- **Photocurrent instrumentation**
- **Active filters** ■ **Intrusion alarm systems**
- **Comparators** ■ **Instrumentation amplifiers**
- **Function generators** ■ **Power supplies**

Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2 and Q5 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14-lead plastic package (E1 suffix) is provided through the use of this current mirror.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25°C$		TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typ. Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Max. V_{IO}		18	4.7	kΩ
Input Resistance	R_I			1.5	1.5	TΩ
Input Capacitance	C_I			4	4	pF
Output Resistance	R_O			60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 21)	e_n	BW=140 kHz, R_S = 1 MΩ		48	48	μV
Equivalent Input Noise Voltage (See Fig. 10)	e_n	f= 1 kHz	R_S= 100 Ω	40	40	nV/√Hz
		f=10 kHz		12	12	
Short-Circuit Current to Opposite Supply Source	I_{OM}^+			40	40	mA
Sink	I_{OM}^-			11	11	
Gain-Bandwidth Product (See Figs. 5 and 19)	f_T			4.5	4.5	MHz
Slew Rate (See Fig. 6)	SR			9	9	V/μs
Transient Response: Rise Time	t_r	R_L=2 kΩ, C_L=100 pF		0.08	0.08	μs
Overshoot (See Fig. 20)	t_r	R_L=2 kΩ, C_L=100 pF		10	10	%
Settling Time at 10 V_{p-p}, (See Fig. 17)	1 mV / 10 mV t_s	R_L=2 kΩ, C_L=100 pF, Voltage Follower		4.5 / 1.4	4.5 / 1.4	μs
Crosstalk		f = 1 kHz		120	120	dB

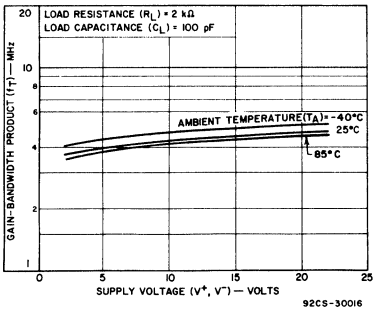


Fig. 5 — Gain-bandwidth product as a function of supply voltage and temperature.

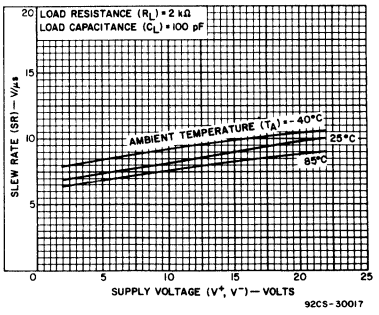


Fig. 6 — Slew rate as a function of supply voltage and temperature.

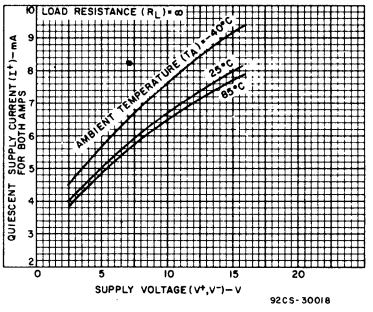


Fig. 7 — Quiescent supply current as a function of supply voltage and temperature.

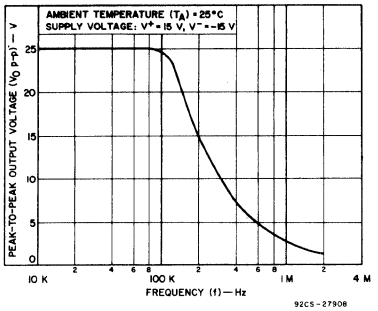


Fig. 8 — Maximum output voltage swing as a function of frequency.

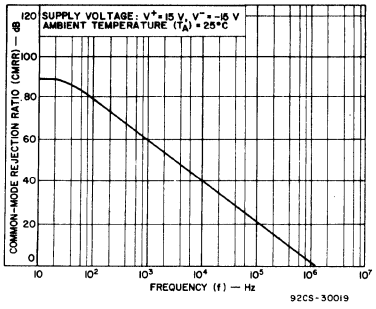


Fig. 9 — Common-mode rejection ratio as a function of frequency.

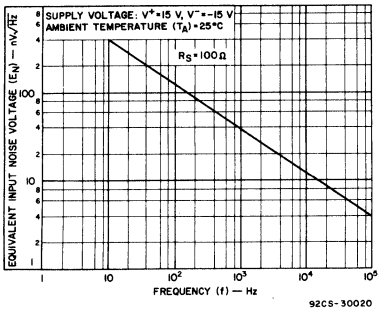


Fig. 10 — Equivalent input noise voltage as a function of frequency.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE
At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25°C$

CHARACTERISTIC		TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Input Offset Voltage,	$\|V_{IO}\|$	2	5	mV
Input Offset Current,	$\|I_{IO}\|$	0.1	0.1	pA
Input Current,	I_I	2	2	pA
Input Resistance		1	1	TΩ
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}	100 k	100 k	V/V
		100	100	dB
Common-Mode Rejection Ratio,	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 22)	V_{ICR}	−0.5	−0.5	V
		2.6	2.6	
Power-Supply Rejection Ratio,	PSRR	31.6	31.6	μV/V
		90	90	dB
Maximum Output Voltage,	V_{OM}^+	3	3	V
(See Figs. 16,22)	V_{OM}^-	0.3	0.3	
Maximum Output Current: Source,	I_{OM}^+	20	20	mA
Sink	I_{OM}^-	1	1	
Slew Rate (See Fig. 6)		7	7	V/μs
Gain-Bandwidth Product, (See Fig. 5)	f_T	4.5	4.5	MHz
Supply Current, (See Fig. 7)	I^+	4	4	mA
Device Dissipation,	P_D	20	20	mW

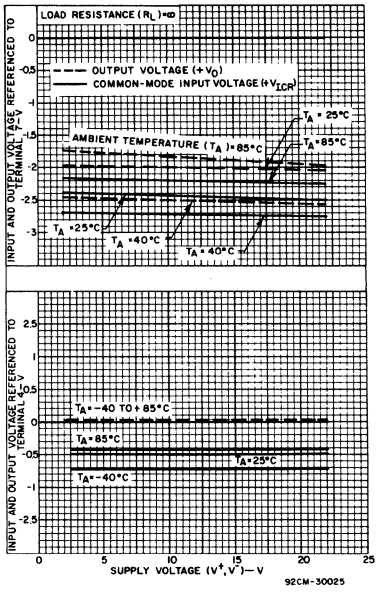


Fig. 16 — Output-voltage-swing capability and common-mode input-voltage range as a function of supply voltage and temperature.

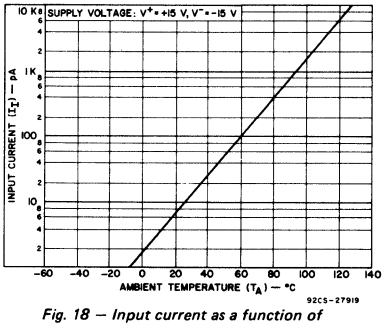


Fig. 18 — Input current as a function of ambient temperature.

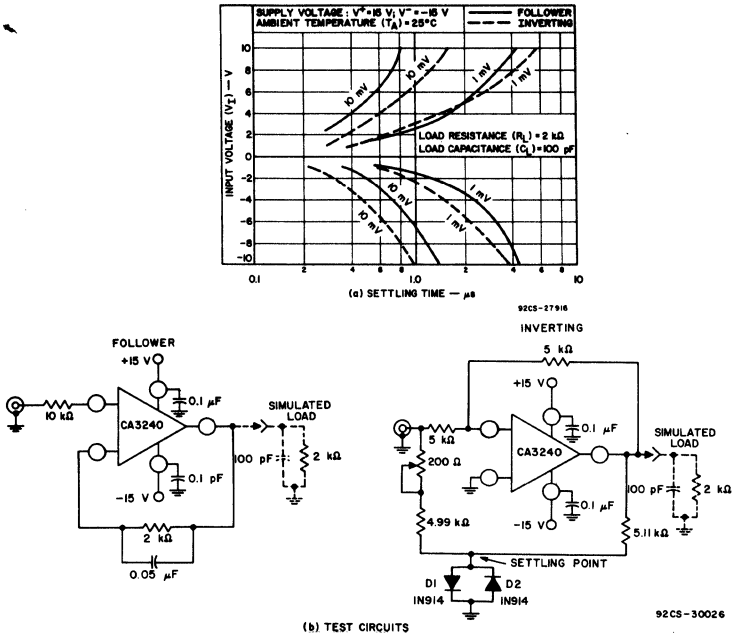


Fig. 17 — Input voltage as a function of settling time.

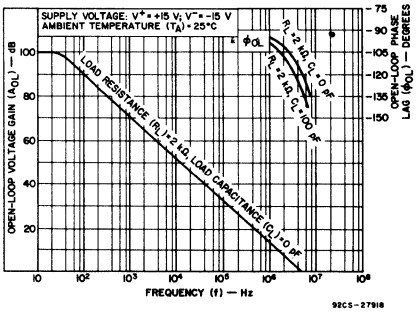


Fig. 19 — Open-loop voltage gain and phase lag as a function of frequency.

TYPICAL APPLICATIONS

On/Off Touch Switch

The on/off touch switch shown in Fig. 26 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-kΩ resistor and 36-kΩ/42-kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

Dual Level Detector (window comparator)

Fig. 27 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5-V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Fig. 26. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Fig. 28 uses the CA3240E as a voltage-error and current-sensing amplifier. The CA3240E is ideal for this application because its input common-mode voltage-range includes ground, allowing the supply to adjust from 20 mV to 25 V without requiring an additional negative input voltage. Also, the ground reference capability of the CA-3240E allows it to sense the voltage across the 1-Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40 W. Fig. 29 shows the transient response of the supply during a 100-mA to 1-A load transition.

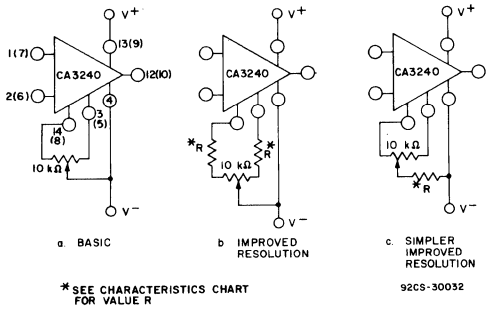


Fig. 25 — Three offset-voltage nulling methods. (CA3240AE1, CA3240E1 only.)

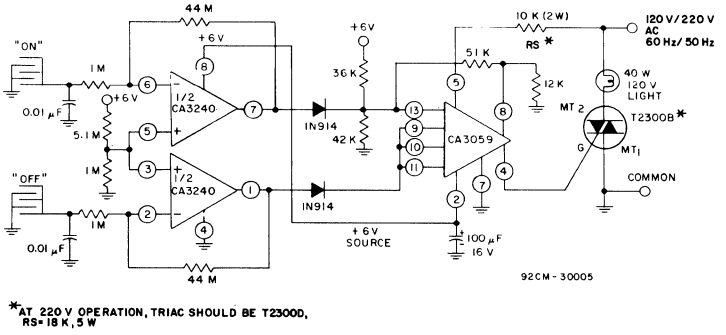


Fig. 26 — On/off touch switch.

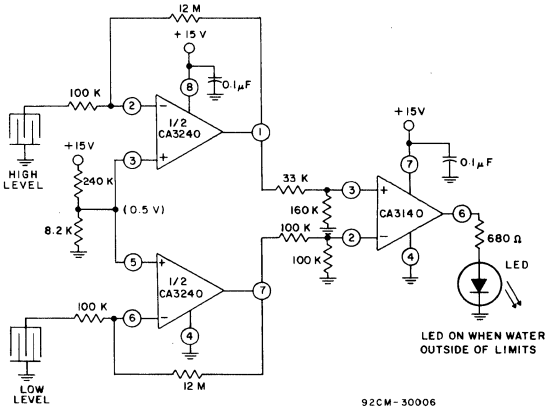


Fig. 27 — Dual level detector.

Differential Light Detector

In the circuit shown in Fig. 32, the CA3240E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

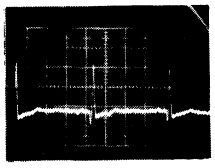


Fig. 31 – Typical electrocardiogram waveform.

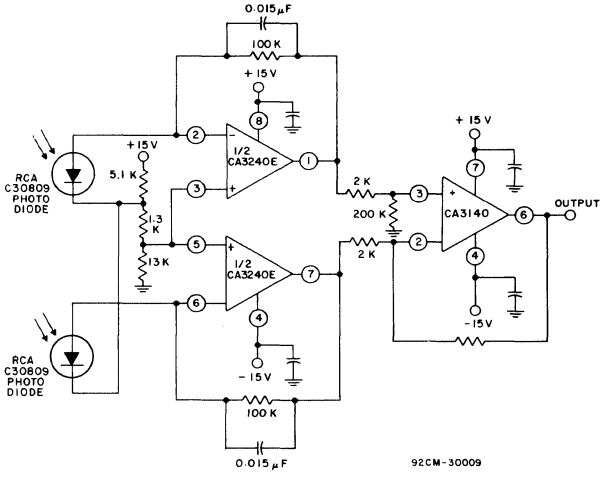
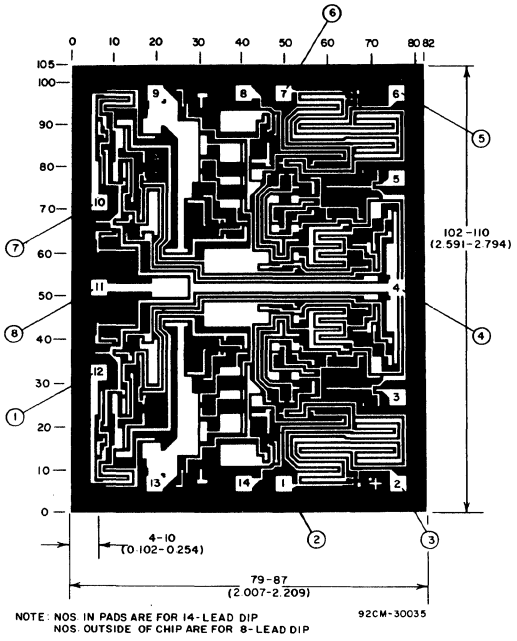


Fig. 32 – Differential light detector.

CA3240H Dimensions and Pad Layout



NOTE: NOS. IN PADS ARE FOR 14-LEAD DIP
NOS. OUTSIDE OF CHIP ARE FOR 8-LEAD DIP

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

ELECTRICAL CHARACTERISTICS at T_A = −55 to +125°C

CHARACTERISTIC	TEST CONDITIONS	V^+	CA3290B Typ.	CA3290B Max.	CA3290A Typ.	CA3290A Max.	CA3290 Typ.	CA3290 Max.	UNITS
Input Offset Voltage, V_{IO}	V_{IC}=1.4 V, V_O=1.4 V	5 V	3.5	–	4.5	–	8.5	–	mV
	V_{IC}=0 V, V_O=0 V	±15 V	3.5	–	8.5	–	8.5		
Temp. Coefficient of Input Offset Voltage, $\Delta V_{IO}/\Delta T$			8	–	8	–	8	–	μV/°C
Input Offset Current, I_{IO}	V_{IC}=1.4 V	5 V	2	22	2	28	2	32	nA
	V_{IC}=0 V	±15 V	7	22	7	28	7	32	
Input Current, I_I▲	V_{IC}=1.4 V	5 V	2.8	32	2.8	45	2.8	55	nA
	V_{IC}=0 V	±15 V	13	32	13	45	13	55	
Supply Current, I^+*	R_L = ∞	5 V	0.85	1.6	0.85	1	0.85	1.6	mA
		30 V	1.62	3.5	1.62	3	1.62	3.5	
Voltage Gain, A_{OL}	R_L=15 kΩ	±15 V	150	–	150	–	150	–	V/mV
			103	–	103	–	103	–	dB
Saturation Voltage	V^+=5 V, 4 mA, $+V_I$=0 V, $-V_I$=1 V	+125°C	0.22	0.7	0.22	0.7	0.22	0.7	V
		−55°C	0.1	–	0.1	–	0.1	–	
Output Leakage Current, I_{OL}		15 V	65	–	65	–	65	–	nA
		36 V	130	1k	130	1k	130	1k	

▲At T_A = +125°C
*At T_A = −55°C

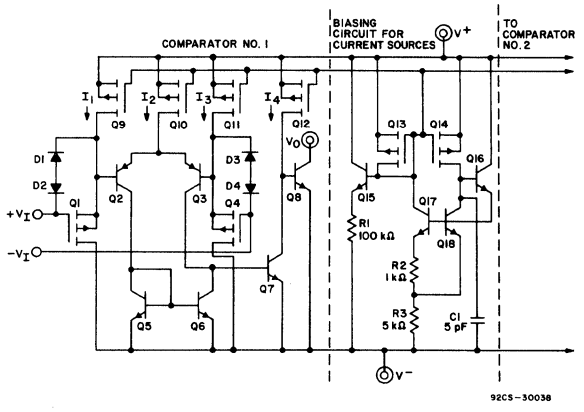


Fig. 2 – Schematic diagram of CA3290 (only one is shown).

In essence, Q1 and Q4 function as source-followers to drive Q2 and Q3, respectively, with zener diodes D1 through D4 providing gate-oxide protection against input voltage transients (e.g., static electricity). The current flow in Q1 and Q2 is established at approximately 50 microamperes by constant-current sources I_1 and I_3, respectively. Since Q1 and Q4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode range. As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential dc voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q7 and Q8. The collector of Q8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink-current capability.

The detailed schematic diagram for one comparator and the common current-source biasing is shown in Fig. 2. PMOS transistors Q9 through Q12 are the current-source elements identified in Fig. 1 as I_1 through I_4, respectively. Their gate-source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right-hand portion of the Fig. 2. The currents supplied by Q10 and Q12 are twice those supplied by Q9 and Q11. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q9 through Q12.

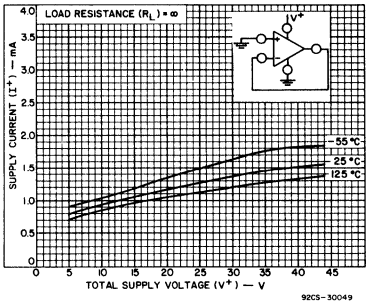


Fig. 3 – Supply current as a function of supply voltage (both amplifiers).

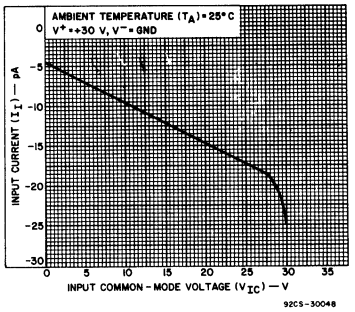


Fig. 4 – Input current as a function of input common-mode voltage.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTIC	TEST COND. V^+	LIMITS CA3290 Min.	LIMITS CA3290 Typ.	LIMITS CA3290 Max.	UNITS
Input Offset Voltage, V_{IO} V_{IC}=1.4 V, V_O=1.4 V	5 V	–	7.5	20	mV
V_{IC}=0 V, V_O=0 V	±15 V	–	7.5	20	
Input Current, I_I V_{IC}=1.4 V	5 V	–	3.5	50	pA
V_{IC}=0 V	±15 V	–	12	50	
Input Offset Current, I_{IO} V_{IC}=1.4 V	5 V	–	2	30	pA
V_{IC}=0 V	±15 V	–	7	30	
Common-Mode Input-Voltage Range, V_{ICR} V_O=1.4 V	5 V	V^+–3.5, V^-	V^+–3.1, V^-–1.5	–	V
V_O=0 V	±15 V	V^+–3.8, V^-	V^+–3.4, V^-–1.6	–	
Supply Current, I^+ R_L = ∞	30 V	–	1.35	3	mA
	5 V	–	0.8	1.4	
Voltage Gain, A_{OL} R_L = 15 kΩ	±15 V	25	800	–	V/mV
		88	118	–	dB
Output Sink Current V_O=1.4 V	5 V	6	30	–	mA
Saturation Voltage +V_I=0 V, –V_I=1 V, 4 mA	5 V	–	0.12	0.4	V
Output Leakage Current, I_{OL}	15 V	–	100	–	pA
	36 V	–	500	–	
Response Time R_L=5.1 kΩ Rising Edge	15 V	–	1.2	–	μs
Falling Edge		–	200	–	ns
Common-Mode Rejection Ratio, CMRR	±15 V	–	44	562	μV/V
	5 V	–	100	562	
Power-Supply Rejection Ratio, PSRR	±15 V	–	15	316	μV/V
Large-Signal Response Time R_L=5.1 kΩ	15 V	–	500	–	ns
	5 V	–	400	–	

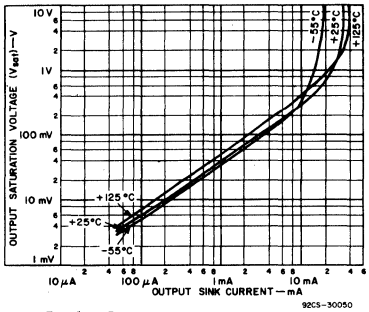
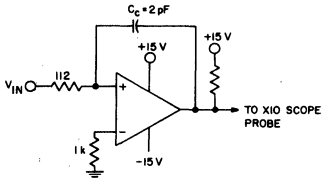
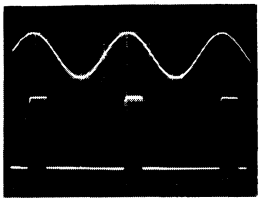


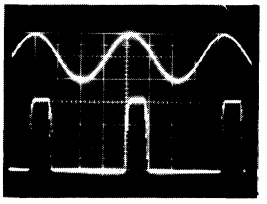
Fig. 9 – Output saturation voltage as a function of output sink current.





WITH C_c

TOP TRACE ≈ 4.5 mV/DIV = V_{IN}
BOTTOM TRACE = 10 V/DIV = V_{OUT}
H = 5 μs/DIV



WITHOUT C_c

TOP TRACE ≈ 4.5 mV/DIV
BOTTOM TRACE = 10 V/DIV
H = 5 μs/DIV

92CM-30059

Fig. 10 – Parasitic-oscillations test circuit and associated waveforms.

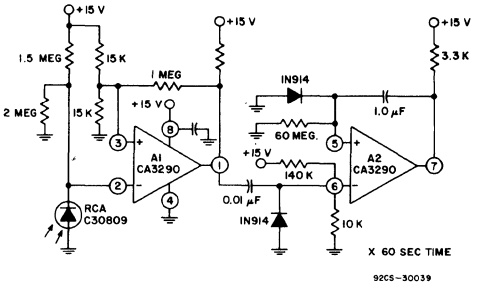


Fig. 13 – Light-controlled one-shot timer.

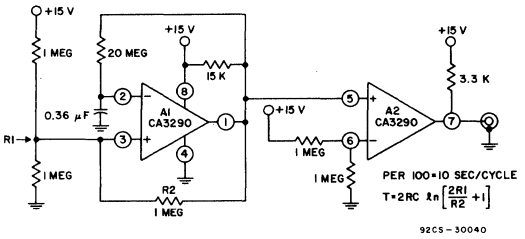


Fig. 14 – Low-frequency multivibrator.

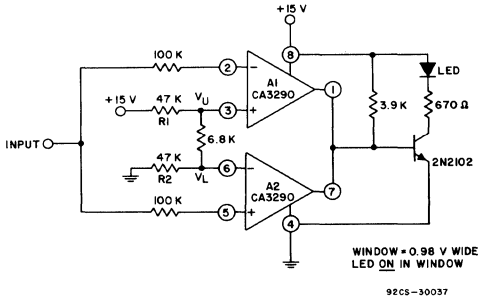


Fig. 15 – Window comparator.

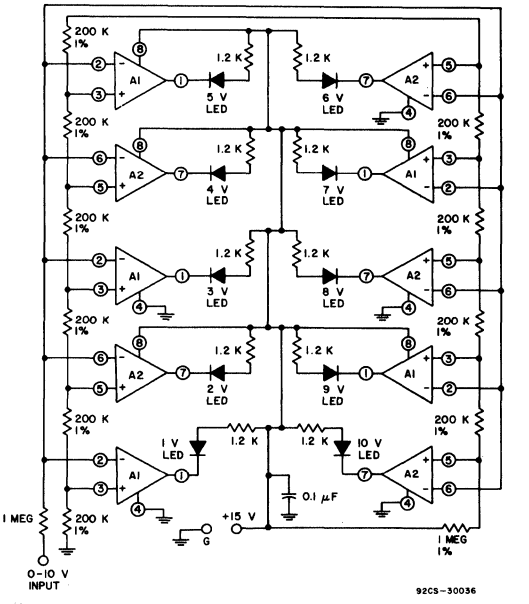
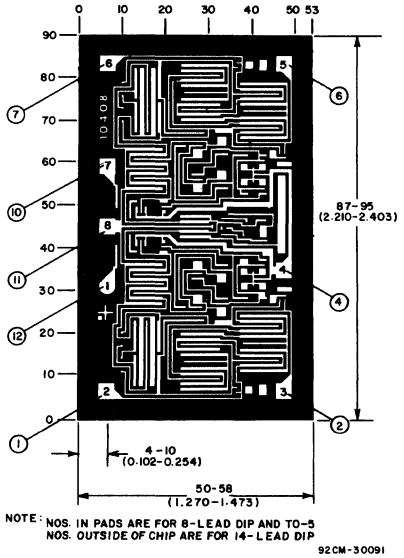


Fig. 16 – 1 LED bar-graph driver.



Dimensions and pad layout for the CA3290H.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = 15 V (Unless Indicated Otherwise)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
STATIC					
Output Voltage:					
High, V_{OH}		13.5	14.2	–	V
Low, V_{OL}		–	0.03	0.1	
Max. Undistorted Output Swing, V_{OP-P}	0°C<T_A<75°C	10	13.5	–	
Output Current:					
Source, I_{SOURCE}		5	10	–	mA
Sink, I_{SINK}		0.5	1	–	
Total Quiescent Current: I_Q					
Noninverting inputs open		–	6.9	10	mA
Noninverting inputs grounded		–	7.8	14	
Input Bias Current, I_{IB}	R_L = ∞ T_A = 25°C	–	50	300	nA
	R_L = ∞ 0°C ≤T_A≤75°C	–	–	500	
DYNAMIC					
Open-Loop Voltage Gain, A_{OL}	T_A = 25°C	1000	2000	–	V/V
	0°C≤T_A≤75°C	800	–	–	
Input Resistance, R_I		0.1	1	–	MΩ
Slew Rate, SR	C_L = 100 pF, R_L = 5 kΩ	–	0.6	–	V/μs
Unity Gain Gandwidth, BW		–	5	–	MHz
Phase Margin, ϕ		–	70	–	Degrees
Power Supply Rejection	f = 100 Hz	–	55	–	dB
Channel Separation, e_{01}/e_{02}	f = 1 kHz	–	65	–	dB

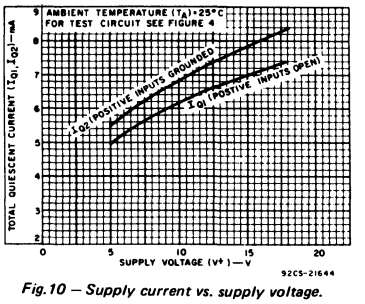


Fig.10 – Supply current vs. supply voltage.

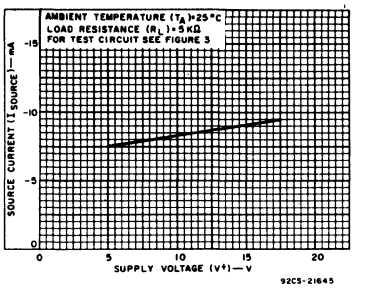


Fig.11 – Source current vs. supply voltage.

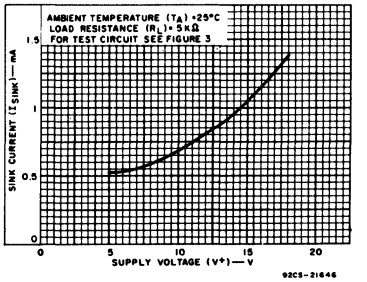


Fig.12 – Sink current vs. supply voltage.

TEST CIRCUITS

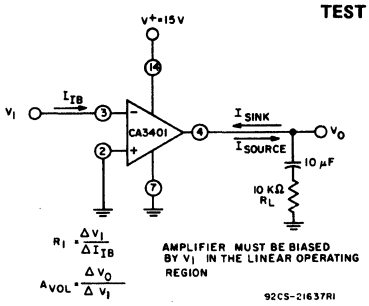


Fig.6 – Open-loop gain and input resistance, input bias current and output current test circuit.

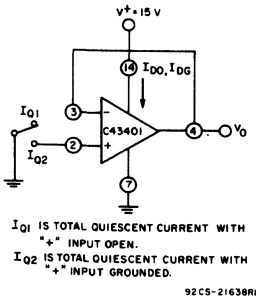


Fig.7 – Quiescent power supply current test circuit.

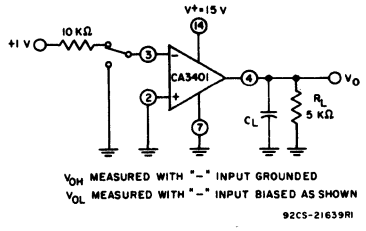


Fig.8 – Output voltage swing test circuit.

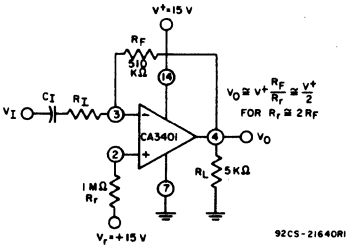


Fig.9 – Peak-to-peak output voltage test circuit.

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYPICAL CURVE OR CIRCUIT FIG. NO.	LIMITS			UNIT
				Min.	Typ.	Max.	
For Each p-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=−10 V, V_{GS}=−3.6 V	2,3,4	−0.5	−1.1	−2.0	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=−10 μA	–	–	−1.75	–	V
Gate-to-Source Voltage Differential (p_1 vs. p_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=−100 μA, V_{DS}=−10 V	5	–	±4	±20	mV
Forward Transconductance	g_{fs}	I_D=−1 mA, f=1 kHz	6	–	920	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=−1 mA, f=1 kHz, R_s=0 Ω	7	–	0.03	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=−1 mA, f=1 kHz, R_s=1 MΩ	7	–	0.2	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (p_1/p_2)	I_{MTR}	I_1=−100 μA, V_{DS}=−10 V	30	0.7	1.1	1.5	–
Gate-Terminal Current	I_{GT}	V_{DS}=−10 V, V_{GS}=−3.5 V	–	–	±0.015	−40	nA
Input Capacitance	C_I	–	–	–	6.3	–	pF
Output Capacitance	C_O			–	3	–	pF
Input-to-Output Capacitance	C_{I-O}	–		–	0.75	–	pF
For Each n-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=+10 V, V_{GS}=+3.6 V	2,3,4	0.4	0.9	1.6	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=10 μA	–	–	1.5	–	V
Gate-to-Source Voltage Differential (n_1 vs n_2)	$\lvert V_{GS1}\ V_{GS2}\rvert$	I_D=100 μA, V_{DS}=+10 V	5		±30	–	mV
Forward Transconductance	g_{fs}	I_D=1 mA, f=1 kHz	6		860	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=1 mA, f=1 kHz, R_s=0 Ω	7	–	0.2	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=1 mA, f=1 kHz, R_s=1 MΩ	7	–	0.3	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (n_1/n_2)	I_{MTR}	I_1=100 μA, V_{DS}=+10 V	29	0.7	1.3	2.0	–
Gate-Terminal Current	I_{GT}	V_{DS}=+10 V, V_{GS}=+3.7 V	–	–	±0.01	+40	nA
Input Capacitance	C_I	–	–	–	5.5	–	pF
Output Capacitance	C_O	–	–	–	2.0	–	pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	0.35	–	pF
For Each COS/MOS Transistor Pair							
Drain Current	I_{DD}	V_{DD}=+10 V	9,10	1.0	2.2	4.0	mA
Drain-to-Source Cutoff Current	$I_{DD(off)}$	V_{DD}=+10 V, V_{SS}=0 V Gate Voltage(V_G)=+10 V or 0 V	8	–	0.5	100	nA
DC Output Voltage	V_O	V_{DD}=+10 V	10	4.2	5.0	5.8	V
Forward Transconductance	g_{fs}	V_{DD}=+10 V, f = 1 kHz	6	–	2300	–	μmho
Slew Rate (Open-Loop)	SR	V_{DD}=+15 V	10	–	95	–	V/μs
Amplifier Voltage Gain	A_{OL}	V_{DD}=+10 V, f=1 kHz, R_b=22 MΩ R_s=50 Ω	10,11	–	32		dB
Gate-Terminal Current	I_{GT}	V_{DD}=+10 V	10	–	±0.005	±20	nA
Broadband Output Noise Voltage	E_{ON}	V_{DD}=+10 V, R_b=22 MΩ, R_s=10 kΩ	10,11	–	500		μV
Input Capacitance	C_I	–	–	–	11.8		pF
Output Capacitance	C_O	–	–	–	5.0		pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	1.1		pF

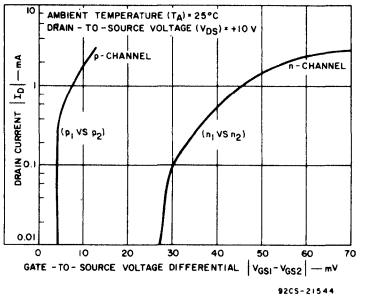


Fig. 5– Gate-to-source voltage differential vs. drain current.

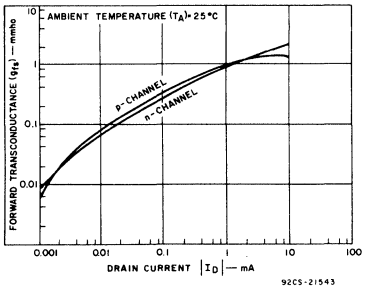


Fig. 6– Forward transconductance vs. drain current.

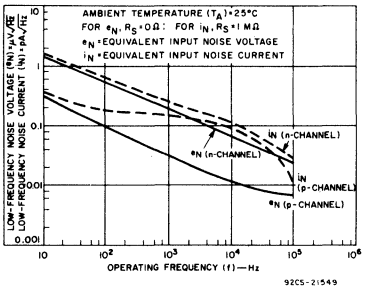


Fig. 7– Noise voltage and noise current vs. operating frequency.

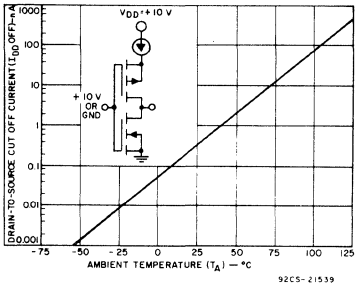


Fig. 8– Drain-to-source cutoff current vs. ambient temperature.

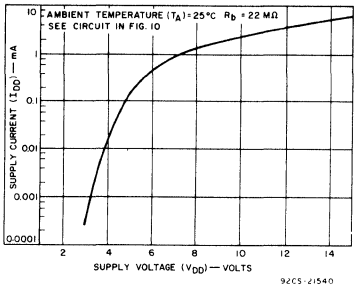


Fig.9 – Typical V_{DD} vs. I_{DD} characteristics for amplifier circuits of Fig.10 and Fig.15.

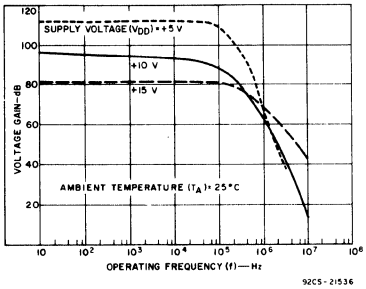


Fig. 17– Typical voltage gain vs. operating frequency characteristics for three-stage COS/MOS transistor-pair amplifier in Fig. 16.

APPLICATIONS – Post-Amplifiers for Op-Amps (Cont'd)

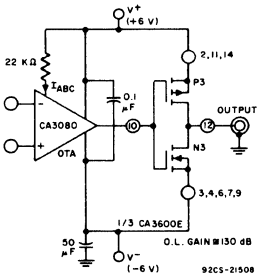


Fig. 18– COS/MOS transistor-pair used as post-amplifier to op-amp in open-loop circuit.

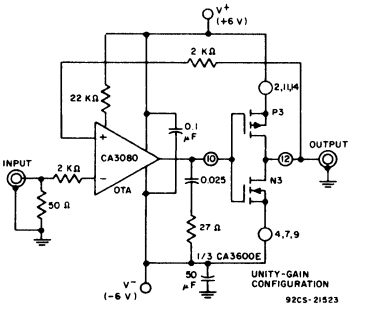


Fig. 19– COS/MOS transistor-pair used as post-amplifier to op-amp in unity-gain circuit.

Multivibrators, Threshold Detectors, and Comparators

Descriptions of several circuits using COS/MOS transistor-pairs in both monostable and astable multivibrators have been published. The characteristics of COS/MOS pairs are also ideal for mating with micropower op-amps in circuits such as the precision multistable circuits shown in Fig. 22. In these circuits precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080 Operational Transconductance Amplifier. Moreover, speed vs. power consumption tradeoffs can be made by adjustment of the Amplifier-Bias-Current (I_{ABC}) supplied to terminal 5 of the CA3080. The quiescent power consumption of the circuits shown in Fig. 22 is typically 6 mW, but can be made to operate in the micropower region by suitable modifications.

The schematic diagram of a programmable micropower comparator, shown in Fig. 23 employs the combination of an op-amp (CA3080A) and COS/MOS transistor-pairs in the CA3600E. Quiescent power consumption of the circuit is about 10 μW(typ.). When the comparator is strobed "ON", transistor P1 is driven into conduction and the OTA becomes active. Under these conditions, the circuit consumes 420 μW and responds to a differential-input signal in about 8 μs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 ns but the power consumption is increased to 21 mW. The differential amplifier input common-mode range for this circuit is −1 V to +10.5 V. Voltage gain of this micropower comparator is typically 130 dB.

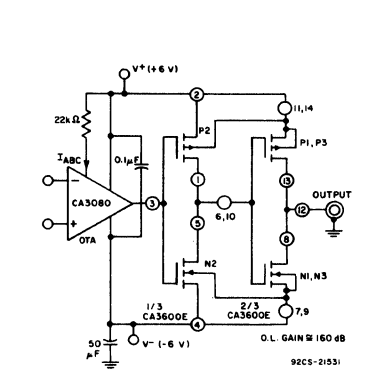


Fig. 20– COS/MOS transistor-pairs used as two-stage post-amplifier to op-amp in open-loop circuit.

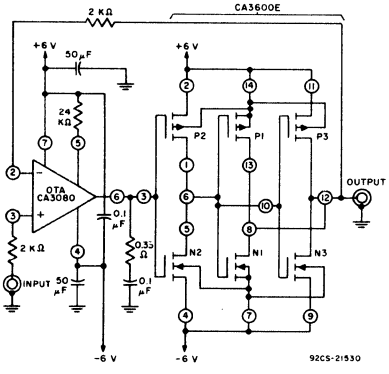


Fig. 21– Unity-gain amplifier uses COS/MOS transistor-pairs as two-stage post-amplifier to op-amp.

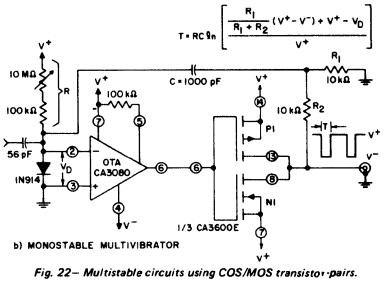


Fig. 22– Multistable circuits using COS/MOS transistor-pairs.

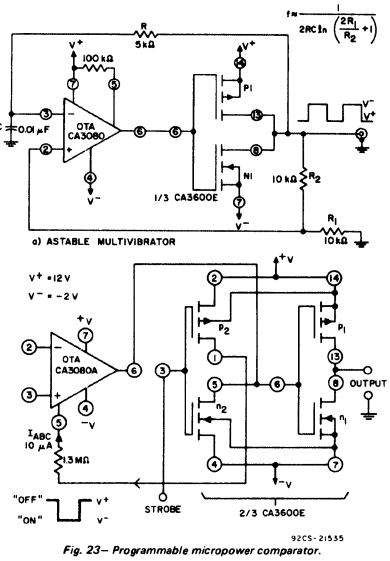
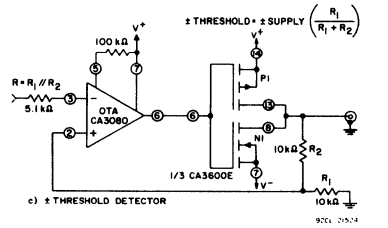


Fig. 23– Programmable micropower comparator.



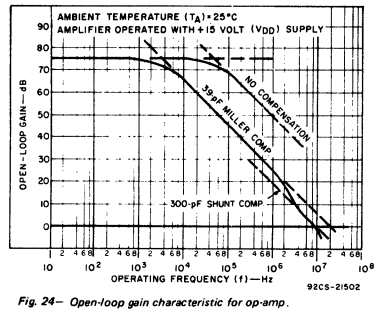


Fig. 24– Open-loop gain characteristic for op-amp.

High-Current N-P-N Transistor Arrays

Four Individual Sealed-Junction High-Current N-P-N Transistors

The RCA-CA3724G and -CA3725G are high-current n-p-n transistor arrays each containing 4 individual sealed-junction high-current n-p-n transistors. They are intended for high-current, high-speed switching and driver applications.

These devices are alike except for breakdown voltage ratings.

The CA3724G and CA3725G are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of −55°C to +125°C. The transistor chips used in these packages are of the sealed-junction type to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure.

The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

Applications:

- **Core-Memory Driver**
- **High-Speed Switching**
- **High-Current LED Driver**
- **High-Voltage Switching**
- **Relay and Solenoid Driver**
- **Lamp Driver**

Features:

- **High Current – 1 A**
- **High Breakdown Voltage:**
  CA3725G = 80 V dc min. $V_{(BR)CES}$ @ I_C = 10 μA
  CA3724G = 70 V dc min. $V_{(BR)CES}$ @ I_C = 10 μA
- **Fast Switching Speeds:**
  t_{on} = 30 ns typ. @ I_C = 500 mA
  t_{off} = 36 ns typ. @ I_C = 500 mA
- **"Hermetic Chip" Construction**
- **Silicon Nitride Passivated**
- **Platinum Silicide Ohmic Contacts**
- **Gold Chip-Metallization**
- **Electrically similar and pin compatible with industry types MPQ3724, MPQ3725; FPQ3724, FPQ3725; DH3724, DH3725; SP3724, SP3725 in similar packages**

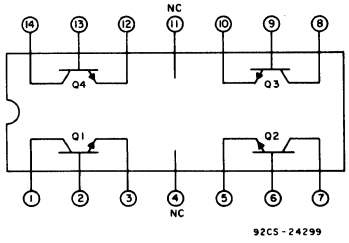


Fig. 1—Terminal diagram (top view).

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

		CA3724G	CA3725G	
COLLECTOR-TO-EMITTER VOLTAGE With Base Open	V_{CEO}	40	50	V
COLLECTOR-TO-BASE VOLTAGE With Emitter Open	V_{CBO}	70	80	V
EMITTER-TO-BASE VOLTAGE With Collector Open	V_{EBO}	6	6	V
COLLECTOR CURRENT	I_C	1.0	1.0	A
POWER DISSIPATION:	P_D			
At T_A up to 25°C:				
For Each Transistor		1.0	1.0	W
Total Package		2.0	2.0	W
At T_A above 25°C derate linearly		20		mW/°C
AMBIENT TEMPERATURE RANGE:				
Operating		−55 to +125	−55 to +125	°C
Storage		−65 to +150	−65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):				
At distance 1/32" (3.17 mm) from seating plane for 10 s max.		300	300	°C

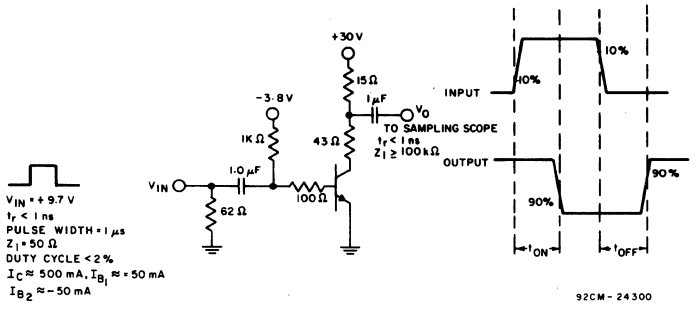


Fig. 2—Switching time test circuit.

Operational Amplifiers

CA6078AT — Micropower Type
CA6741T — General-Purpose Type

For Applications where Low Noise (Burst + 1/f) is a Prime Requirement

Virtually free from "popcorn" (burst) noise: device rejected if any noise burst exceeds 20 μV (peak), referred to input over a 30-second time period.

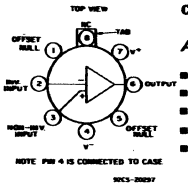
RCA-CA6078AT and CA6741T are low-noise linear IC operational amplifiers that are virtually free of "popcorn" (burst) noise.

These low-noise versions of the CA3078AT and CA3741T are a result of improved processing developments and rigid burst-noise inspection criteria. A highly selective test circuit (See Fig. 2) assures that each type meets the rigid low-noise standards shown in the data section. This low-burst-noise property also assures excellent performance throughout the 1/f noise spectrum.

In addition the CA6078AT and CA6741T offer the same features incorporated in the CA3078AT and CA3741T respectively, including output short-circuit protection, latch-free operation, wide common-mode and differential-mode signal ranges, and low-offset nulling capability.

For detailed data, characteristics curves, schematic diagram, dimensional outline, and test circuits, refer to the Operational Amplifier Data Bulletins File No. 531 and 535. In addition, for details of considerations in burst-noise measurements, refer to Application Note, ICAN-6732, "Measurement of Burst ("Popcorn") Noise in Linear IC's".

The CA6078AT and CA6741T utilize the hermetically sealed 8-lead TO-5 type package. The CA6078AT and the CA6741T can also be supplied on request with dual-in-line formed leads. These types are identified as the CA6078AS and CA6741S. This formed-lead configuration conforms to that of the 8-lead dual-in-line (Mini—Dip) package.



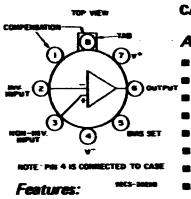
CA6741T

Applications:

- Low-noise AC amplifier
- Narrow-band or band-pass filter
- Integrator or differentiator
- DC amplifier
- Summing amplifier

Features:

- Internal phase compensation
- Input bias current: 500 nA max.
- Input offset current: 200 nA max.
- Open-loop voltage gain: 50,000 (94 dB) min.
- Input offset voltage: 5 mV max.



CA6078AT

Applications:

- Portable electronics
- Medical electronics
- DC amplifier
- Narrow-band or band-pass filter
- Integrator or differentiator
- Instrumentation
- Telemetry
- Summing amplifier

Features:

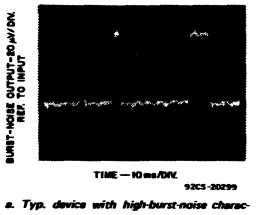
- Open-loop voltage gain: 40,000 (92 dB) min.
- Input offset voltage: 3.5 mV max.
- Operates with low total supply voltage: 1.5 V min. (±0.75 V)
- Low quiescent operating current: adjustable for application optimization
- Input bias current: adjustable to below 1 nA

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

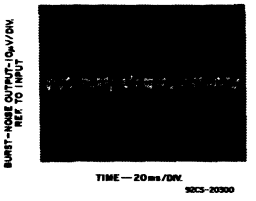
	CA6741T	CA6078AT
DC Supply Voltage (between V+ and V− terminals)	44 V	36 V
Differential-Mode Input Voltage	±30 V	±6 V
Common-Mode DC Input Voltage ▲	±15 V	V+ to V−
Device Dissipation:		
Up to 75°C (CA6741T), Up to 125° (CA6078AT)	500 mW	250 mW
Above 75°C	Derate linearly 5 mW/°C	—
Temperature Range:		
Operating	−55 to +125 °C	−55 to +125 °C
Storage	−65 to +150 °C	−65 to +150 °C
Output Short-Circuit Duration●	No limitation	No limitation
Lead Temperature (During soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	300 °C	300 °C

▲If Supply Voltage is less than ±15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

●Short circuit may be applied to ground or to either supply.

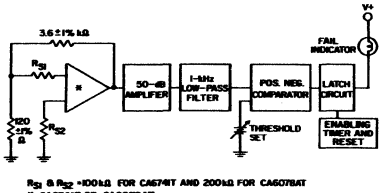


a. Typ. device with high-burst-noise characteristic.



b. Typ. device controlled for burst noise.

Fig.1—Typ. waveforms of type with high burst noise and type controlled for burst noise.



R_{S1} & R_{S2} = 100 kΩ FOR CA6741T AND 200 kΩ FOR CA6078AT
* CA6741T OR CA6078AT
92CS-19423

Fig.2—Block diagram of burst-noise "popcorn" test equipment.

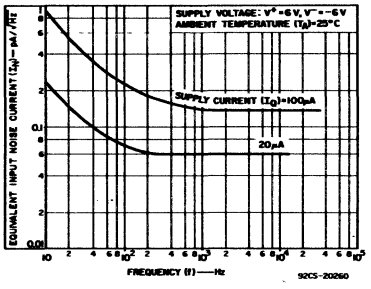


Fig.3—I_N vs. Frequency for CA6078AT.

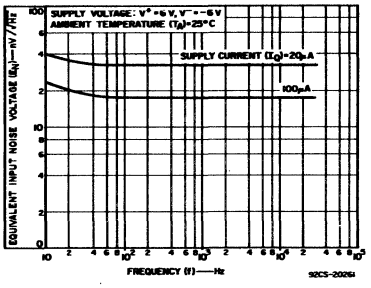


Fig.4—E_N vs. Frequency for CA6078AT.

Linear Integrated Circuits for Consumer Applications

Technical Data

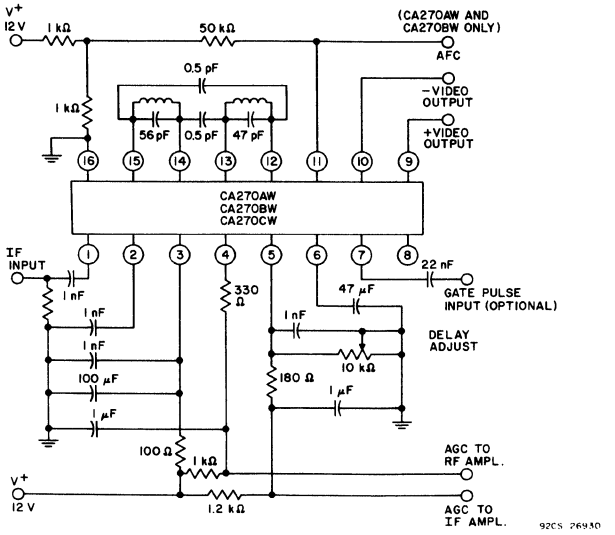


Fig. 4—Test circuit for CA270AW, CA270BW, and CA270CW.

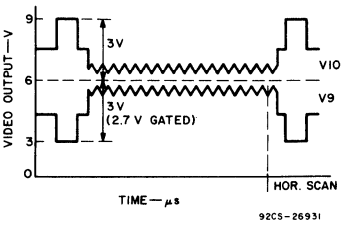


Fig. 5—Typical waveforms for video outputs.

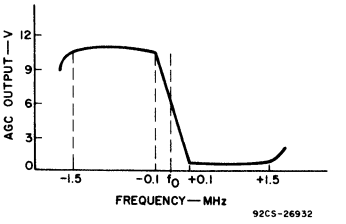


Fig. 6—Typical AFC characteristic.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Supply Voltage (V^+) = 12 V, and Referenced to Test Circuit (Fig. 4).

CHARACTERISTIC	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Voltage, V^+	V^+=12 V		10.2	12	13.8	V
Supply Current, I^+ (See Fig. 2)	V^+=12 V		22	40	56	mA
Video Characteristics: DC Output Voltage, Term.9 (See Fig. 5)	Zero Signal	CA270AW	5.7	6	6.3	V
		CA270BW	5.8	6	6.2	
		CA270CW	5.5	6	6.5	
DC Output Voltage, Term.10 (See Fig. 5)	Zero Signal	CA270AW	5.6	6	6.4	V
		CA270BW	5.7	6	6.3	
		CA270CW	5.5	6	6.5	
Sync Tip Output Voltage, Term.9	Output=AGC threshold (non-gated)		–	3	–	V
AC Input Voltage, Terms.1,2	Input for output= AGC threshold		50	70	100	mV
Input Res.,Term.1			–	3.3	–	KΩ
Input Res., Term.2			–	3.3	–	KΩ
Video Bandwidth, Term.9	At output = –3 dB		–	5	–	MHz
Differential Gain	See Note 1		–	–	10	%
Differential Phase	See Note 1		–	–	10	deg
Intermod. Products: Beat Freq.,1.6 MHz	See Note 1 (95% sat.		–	–	–60	dB
Beat Freq.,2.8 MHz	blue colour bar)		–	–	–67	dB
Rejection at Carrier Freq., Terms.9,10,11	F=Video Carrier; V_{IN} for Term.9(dc)=3.7V		–40	–	–	dB
Rejection,Twice Carrier Freq.,Terms.9,10,11	F=2X Video Carrier; V_{IN} for Term.9(dc) =3.7 V		–40	–	–	dB
AGC Characteristics: Sat.Voltage, Term.4	Zero Sig.; I_4 = 10 mA		–	–	0.3	V
Sat. Voltage, Term.5	Zero Sig.; I_5 = 10 mA		0.7	–	1.2	V

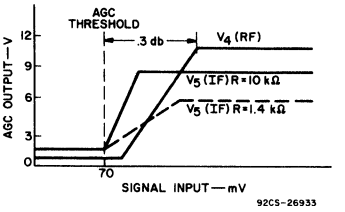


Fig. 7—Typical AGC characteristics.

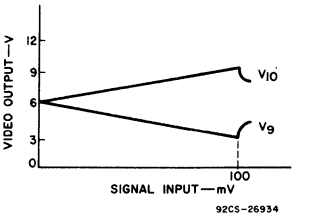


Fig. 8—Typical transfer characteristics.

RC Phase-Locked-Loop Stereo Decoder

For FM Multiplex Systems

Features:

- **Low distortion (THD): 0.4% (typ.)**
- **Excellent SCA rejection: 70 dB typ.**
- **RC oscillator**
- **High-audio-channel separation: 45 dB**
- **Power supply range: 10 to 16 V dc**
- **Requires only one adjustment for complete alignment**
- **Low-impedance outputs**
- **Stereo indicator lamp drive: 150 mA typ.**

RCA-CA758E is a monolithic silicon integrated circuit RC phase-lock loop stereo decoder intended for FM solid-state stereo multiplex systems.

The CA758E is pin compatible and electrically equivalent to industry types μA758, MC1311P, LM1800, and ULX2244.

The CA758E decodes the multiplexed stereo input signal into left and right channel audio output signals. The decoder also suppresses SCA (storecast) transmissions when present in the composite stereo signal.

The decoder uses a minimum of external components, and requires one adjustment (oscillator frequency) for complete alignment. In addition, the CA758E provides automatic mono-stereo mode switching and energizes a stereo indicator lamp.

The CA758E is supplied in a 16-lead dual-in-line plastic package and operates over an ambient temperature range of −40 to +85°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC Supply Voltage	+18 V
DC Supply Voltage (for ⩽a 15-second period)	+22 V
DC Voltage at Term. 7 (Lamp Driver Circuit with Lamp "OFF")	+22 V
Device Dissipation:	
Up to T_A = 70°C	730 mW
Above T_A = 70°C derate linearly	9.1 mW/°C
Ambient Temperature Range:	
Operating	−40 to +85°C
Storage	−65 to +150°C
Lead Temperature (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C

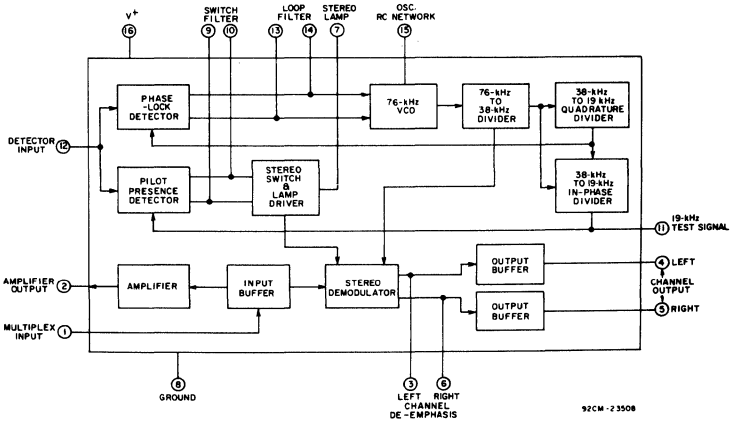
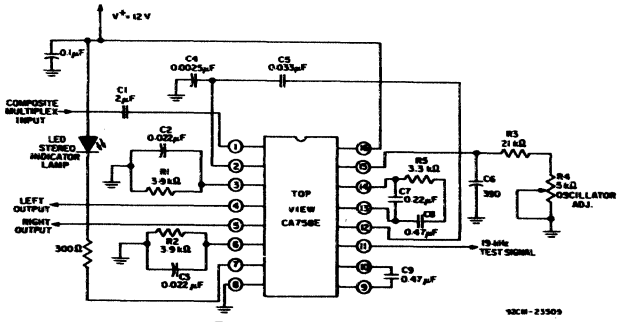


Fig. 1 – Functional block diagram of the CA758E.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig. 7 unless otherwise specified) V^+ = 12 V, T_A = 25°C, Multiplex Input Signal (L=R, pilot "OFF") = 300 mV RMS, 19-kHz Pilot Level = 30 mV RMS, f (modulation) = 400 Hz or 1 kHz	LIMITS Min.	Typ.	Max.	UNITS
Static Characteristics					
Total Current	Lamp "OFF"	–	26	35	mA
Maximum Available Lamp Current		75	150	–	mA
DC Voltage at Term. 7 (Lamp Driver)	I (Lamp) = 50 mA	–	1.3	1.8	V
DC Voltage Shift at either Term. 4 or 5 (Output)	Stereo-to-Mono Operation	–	30	150	mV
Dynamic Characteristics					
Power Supply Ripple Rejection	For a 200-Hz, 200-mV RMS Signal	35	45	–	dB
Input Resistance		20	35	–	kΩ
Output Resistance		0.9	1.3	2.0	kΩ
Channel Separation (Stereo)	At f = 100 Hz	–	40	–	dB
	f = 400 Hz	30	45	–	dB
	f = 10 kHz	–	45	–	dB
Channel Balance (Monaural)		–	0.3	1.5	dB
Voltage Gain	At f = 1 kHz	0.5	0.9	1.4	V/V
Pilot Input Level:					
19-kHz Input	Lamp "ON"	–	15	20	mV RMS
19-kHz Input	Lamp "OFF"	2.0	7.0	–	mV RMS
Hysteresis	Lamp "OFF"	3.0	7.0	–	dB
Capture Range (Deviation from 76-kHz Center Frequency)		±2.0	±4.0	±6.0	%
Total Harmonic Distortion	Multiplex Input Signal = 600 mV RMS (Pilot "OFF")	–	0.4	1.0	%
19-kHz Rejection		25	35	–	dB
38-kHz Rejection		25	45	–	dB
SCA (Storecast) Rejection	Measured Composite Signal: 80% Stereo, 10% Pilot, 10% SCA	–	70	–	dB
Voltage-Controlled Oscillator (VCO) Tuning Resistance	Total Resistance (Term. 15 to 8) required to set f_{REF} = 19 kHz ± 10 Hz (Term. 11)	21.0	23.3	25.5	kΩ
Voltage-Controlled Oscillator Frequency Drift	0° ⩽ T_A ⩽ 25°C	–	+0.1	±2	%
	25° ⩽ T_A ⩽ 70°C	–	−0.4	±2	%



NOTES:

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified.

C_1 = +100%, −20%

C_6 = ±1% in test circuit and ±5% in typical application.

R_3 = ±1%

R_4 = ±10%

R_1 and R_2 = ±1% in test circuit and ±5% in typical application.

Fig. 7— Test circuit for measurement of dynamic characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS (Referenced to Fig. 7)

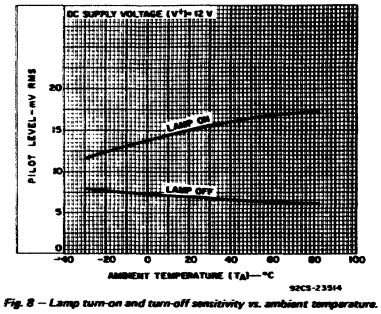


Fig. 8 – Lamp turn-on and turn-off sensitivity vs. ambient temperature.

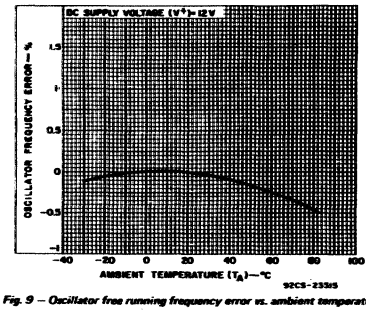


Fig. 9 – Oscillator free running frequency error vs. ambient temperature.

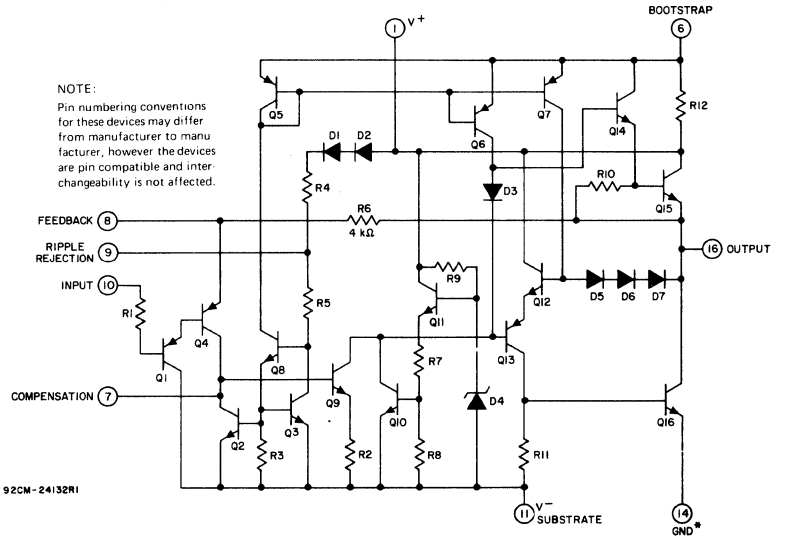


Fig. 1 – Schematic diagram of CA810Q, CA810QM.

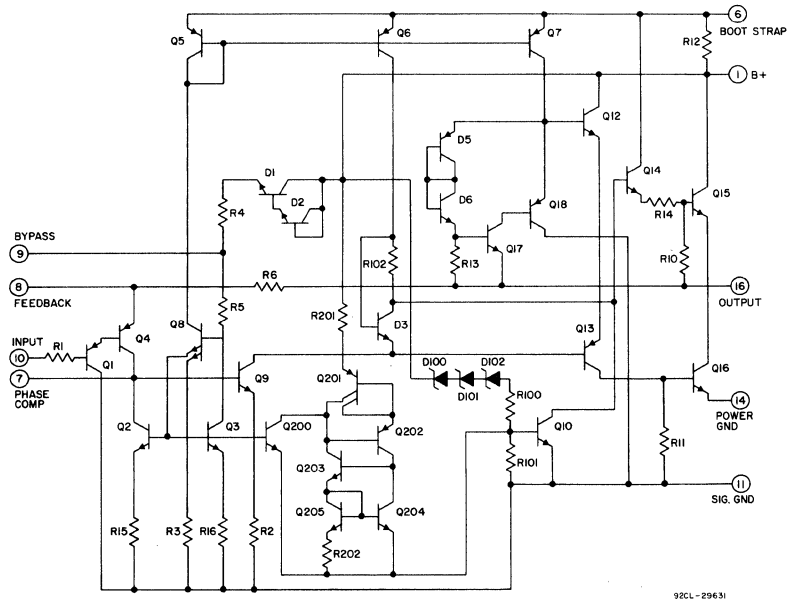


Fig. 3 – Schematic diagram of CA810AQ, CA810AQM.

Thermal Shut-Down

The thermal-limiting network incorporated in the CA810 Series circuits provides protection against damage due to excessive semiconductor temperatures that may result from high ambient temperatures and/or excessive dissipation, e.g., as encountered in sustained overloads. As indicated in Fig.2 the thermal-limiting feature automatically reduces the supply current (and output power) at the higher temperatures.

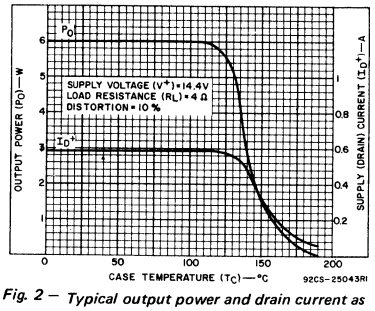


Fig. 2 – Typical output power and drain current as a function of case temperature for all types.

Load-Dump Voltage-Surge Protection

The maximum operating supply voltage of the CA810AQ and CA810AQM is 20 V, and internal protection is provided for peaks of up to 40 V, as shown in Fig. 4. Supply-voltage peaks of more than 40 V will require an LC network between the supply and terminal 5. An LC network, such as the one shown in Fig. 8, provides protection against supply-voltage surges of up to 120 V for 2 ms. This type of protection is ON when the supply voltage (pulsed or dc) exceeds 20 V.

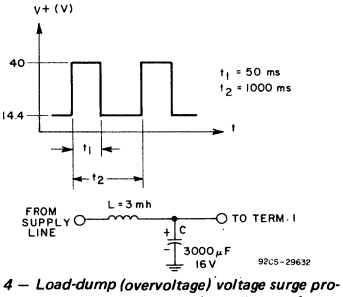


Fig. 4 – Load-dump (overvoltage) voltage surge protection network and timing diagram for CA810AQ and CA810AQM.

TV Horizontal Oscillator

For Color and Monochrome Receivers

The RCA-CA920AE* is a silicon monolithic integrated circuit intended for use in the horizontal stages of color and monochrome television receivers. This device performs the functions of a sync separator, noise gate, and horizontal oscillator with dual-time-constant switching in the fly-wheel loop. It also generates automatic phase control between horizontal flyback pulses and the horizontal oscillator frequency and provides fast edge switching drive for transistor or thyristor horizontal output stages.

The CA920AE is compatible with the industry type TBA920 in both lead arrangement and electrical operation, although the CA-920AE features reduced operating current.

The CA920AE is supplied in the 16-lead dual-in-line plastic package.

*Formerly Dev. Type No. TA6773.

Features:

- **Sync separator**
- **Noise gate input**
- **Internal precision timing ramp**
- **Dual-time-constant phase-locked loop**
- **Output suitable for transistor or thyristor deflection systems**
- **Reduced power dissipation**

MAXIMUM RATINGS, *Absolute Maximum Values:*

DC SUPPLY VOLTAGE	13.2 V
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	Derate linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265°C

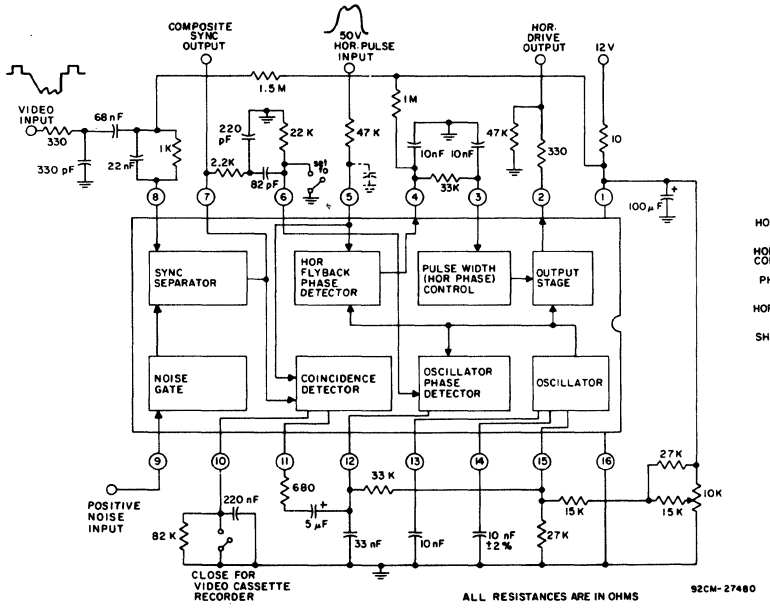
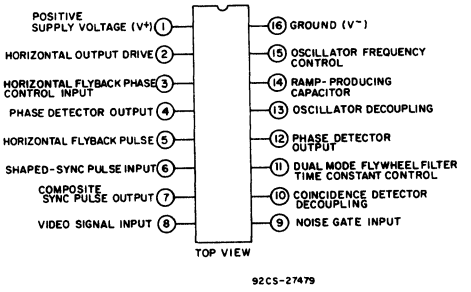


Fig. 1 — Functional block diagram of the CA920AE with typical peripheral circuitry.

TERMINAL ASSIGNMENT



TV Sound IF and Audio Output Subsystems

"GQ" Suffix Type — Hermetic Gold-CHIP in Quad-In-Line Plastic Package

The RCA-CA1190GQ combines the sound IF and audio output subsystems on a single monolithic integrated circuit to provide a television sound system. Each device includes a multistage IF amplifier-limiter, an FM detector, and an audio power amplifier that is designed to drive, primarily, an 8-, 16-, or 32-ohm speaker.

The CA1190GQ is electrically and mechanically equivalent to industry type TDA1190Z. The CA1190GQ differs from the TDA1190Z primarily in its provisions for external feedback components and a higher value volume control.

The CA1190GQ is supplied in the hermetic Gold-CHIP (G suffix) 16-lead quad-in-line plastic package with an integral bent-down wing-tab heat sink (Q suffix), intended for printed circuit board mounting.

The transistor chips used in the hermetic Gold-CHIP plastic package are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

Features:

- **Nominal power output: 4 W at V^+=24 V, R_L=16Ω, dist. = 10%; 2 W at V^+=12 V, R_L = 8Ω, dist.=10%**
- **Wide power-supply range: 9 to 28 V**
- **Low quiescent current: 25 mA typ.**
- **5-kHz deviation sensitivity: 1 W output typ.**
- **3-dB limiting sensitivity: 50 μV typ.**
- **Excellent AM rejection: 50 dB typ.**
- **Differential peak detector — requires one tuned coil**
- **Electronic volume control with improved taper and single wire control**

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 24 V, DC Volume Control Rx = 0 Ω, R_L = 16 Ω unless otherwise indicated. Refer to Fig. 1.

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics					
Current into Term. 14	P_o = 0	10	25	40	mA
Dynamic Characteristics					
IF Amplifier: Input Limiting Voltage, (At −3 dB point), V_1 (lim)	f_o = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz	—	50	100	μV
AM Rejection, AMR	f_o = 4.5 MHz, f_m = 400 Hz, Modulation Index = 0.3, V_{IN} = 1 mV	40	50	—	dB
Deviation Sensitivity	f_o = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, V_I = 1 mV, Rx = 0, Deviation necessary to obtain 4 Vrms across 16 Ω (1 W)	—	5	—	kHz
Minimum Audio Output	f_o = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, V_I = 1 mV, R_X = 15 kΩ	—	—	10	mVrms
Distortion at P_o = 1.5 W	f_o = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, V_{IN} = 1 mV	—	—	3	%
Signal to Noise Ratio	V_{out} at Δf = 0 with Rx adjusted for V_{out} = 4 Vrms at Δf = ± 25 kHz	50	—	—	dB

MAXIMUM RATINGS, *Absolute-Maximum Valu*

DC SUPPLY VOLTAGE (Between Term. 14 V^+ and ground tabs)	+ 28	V
OUTPUT PEAK CURRENT:		
Repetitive	1.5	A
Non-repetitive	2	A
INPUT SIGNAL VOLTAGE (Between Terms. 1 and 2)	±3	V
DEVICE DISSIPATION:		
With Infinite Heat Sink —		
Up to T_A = 90°C derate linearly	5	W
Above T_A = 90°C	83.3	mW/°C
With No Heat Sink — (free air) —		
Up to T_A = 25°C	1.75	W
Above T_A = 25°C derate linearly	14	mW/°C
THERMAL RESISTANCE:		
Junction to ground tabs	12	°C/W
AMBIENT TEMPERATURE RANGE:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At a distance 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

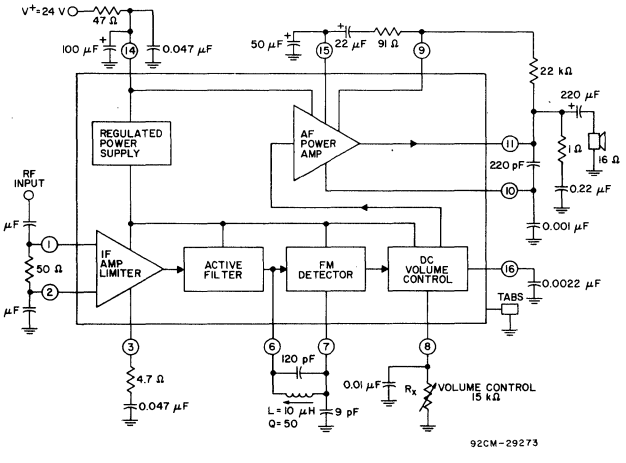


Fig.1 — Block diagram of the CA1190GQ in a typical application.

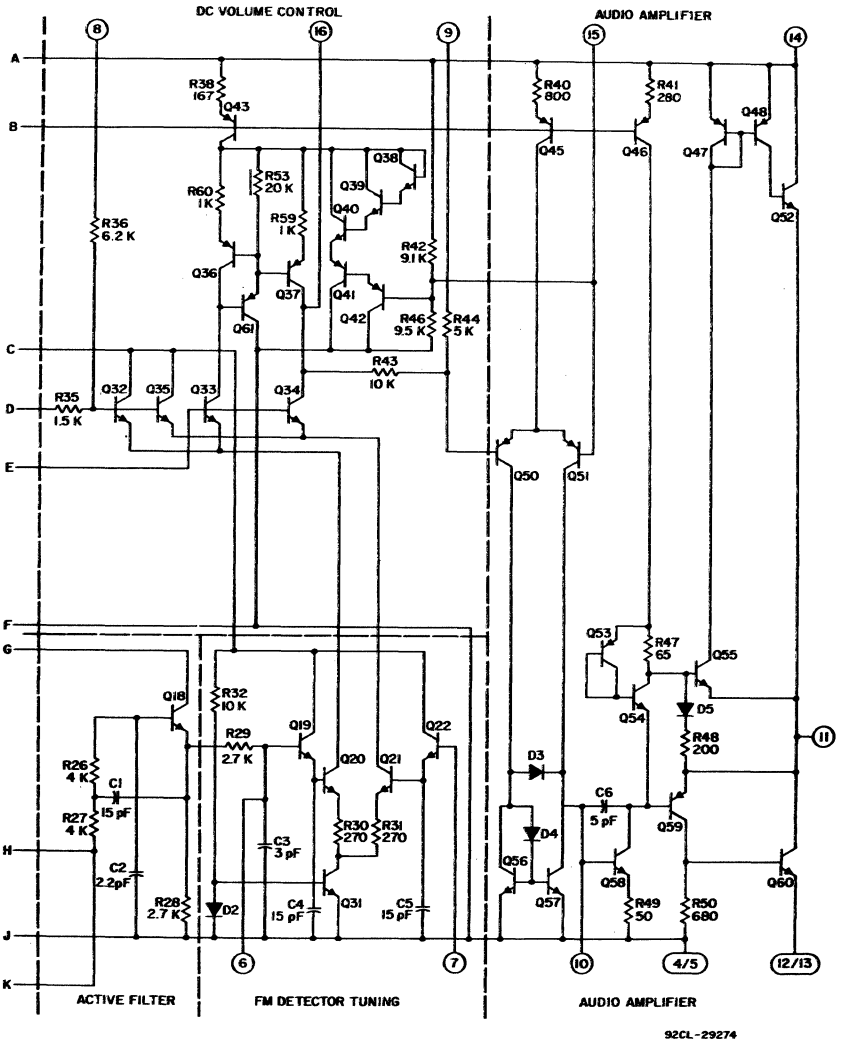


Fig.2 – Schematic diagram (cont'd).

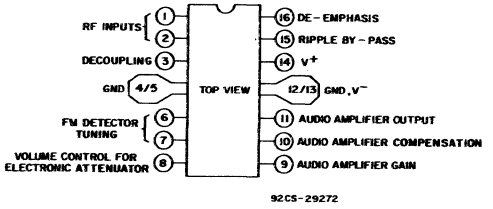


Fig.3 – Terminal diagram.

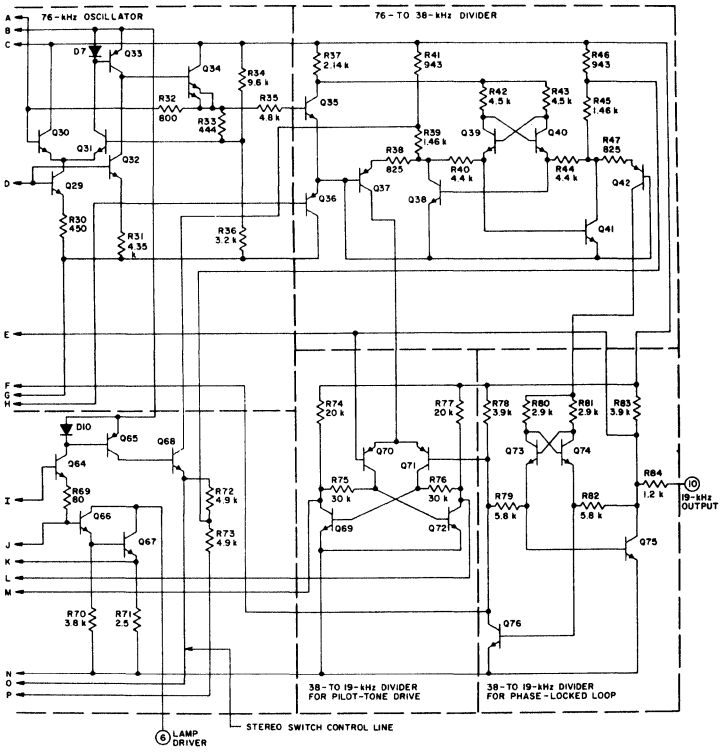
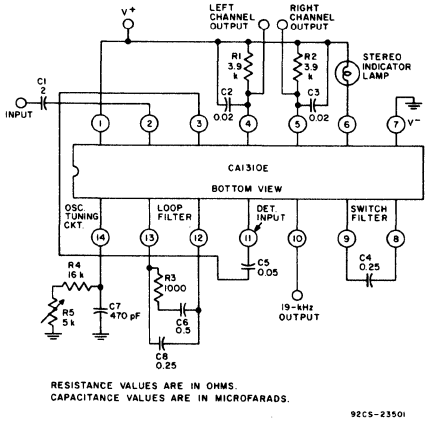


Fig. 2 – Schematic diagram of the CA1310E (Cont'd).



NOTES

A buffered 3-volt positive-going square wave is available at Term. 10. The alignment of the free-running oscillator frequency may be checked at this point with a frequency counter.

C1: A lower value input coupling capacitor may be used in place of the 2-μF value if reduced separation at low frequencies is acceptable.

C4: The time constant for the stereo switch level detector circuit is calculated by C4 x 53,000 ohms ±30% with a maximum dc voltage drop across C4 of 0.25 volt (Term. 8 positive) and a pilot level voltage of 100 mV RMS. Signal voltage across C4 is negligible.

C5: The recommended 0.05-μF capacitor provides a 1.75° phase lead at 19 kHz.

R1, R2: Load resistance values are related to supply voltage as follows:

Minimum Supply Voltage	8	10	12	V
Maximum Load Resistance	2.7	4.3	6.2	kΩ

R3, C6, C8: C8 may be omitted, R3 = 100 ohms and C6 = 0.25 μF, if relaxed circuit performance is acceptable.

R4, R5, C7: If a capture range greater than ±3% typ. is required, reduce value of C7 and increase values of R4, R5 proportionally. However, beat-note distortion is increased at high signal levels because of oscillator-phase jitter. R4, C7 = ±1% in test circuit and ±5% in typical application.

Fig. 3 – Test circuit for measurement of dynamic characteristics.

TV Video IF Amplifier

With AGC and Keyer Circuit

The RCA-CA1352E is a monolithic integrated circuit designed for use as an if amplifier in monochrome or color TV receivers. It features a high-gain gated AGC system with a 68-dB range (typ.). A delayed forward AGC output is adjustable by means of a potentiometer. Either positive- or negative-going sync may be used for this system.

The CA1352E is supplied in the 14-lead dual-in-line plastic package, and is directly interchangeable with the industry type 1352 in similar packages.

Features

- **High 45-MHz gain – 53 dB (typ.)**
- **High-gain gated AGC system – with either positive- or negative-going sync.**
- **Adjustable rf AGC delay to tuner**
- **AGC gain reduction – 68 dB (typ.)**

TYPICAL STATIC CHARACTERISTICS
at $T_A = 25^\circ C$, $V^+ = 12$ V

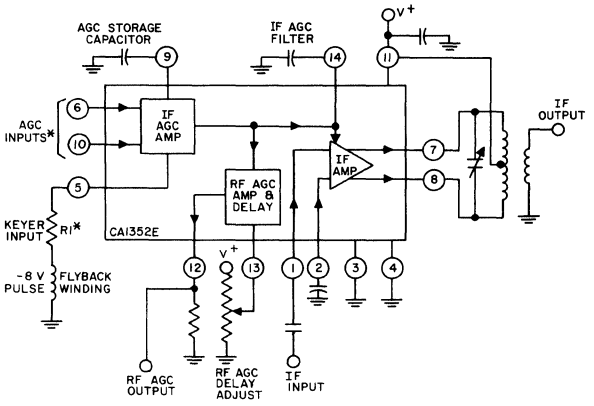
Total Current ($I_7 + I_8 + I_{11}$)	27 mA
Output Stage Current ($I_7 + I_8$)	5.7 mA

TYPICAL DYNAMIC CHARACTERISTICS
at $T_A = 25^\circ C$, $V^+ = 12$ V

AGC Range	68 dB
Power Gain	53 dB
Minimum rf AGC Range (term. 12)	0.2 V
Maximum rf AGC Range (term. 12)	7 V

MAXIMUM RATINGS, *Absolute-Maximum Values*
At $T_A = 25$

SUPPLY VOLTAGE:	
Between terminals 4 and 11	18 V
Between terminals 7 or 8 and 4	18 V
INPUT VOLTAGE (terminal 1 or 2)	10 V p-p
AGC INPUT VOLTAGE (terminal 6 or 10)	6 V
DEVICE DISSIPATION:	
Up to $T_A = 55^\circ C$	750 mW
Above $T_A = 55^\circ C$ derate linearly at	7.9 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C



SYNC POLARITY	* VOLTAGE AT TERMINAL 6	* VOLTAGE AT TERMINAL 10	* VALUE OF RI – Ω
NEGATIVE	5.5 V, 2 V, 0 V	1 TO 4 V NOM = 2 V	0
POSITIVE	1 TO 8 V NOM = 4.5	4.5 V, 0 V	3.9k

92CS-24136RI

Fig. 1 – CA1352E block diagram and typical AGC test set-up.

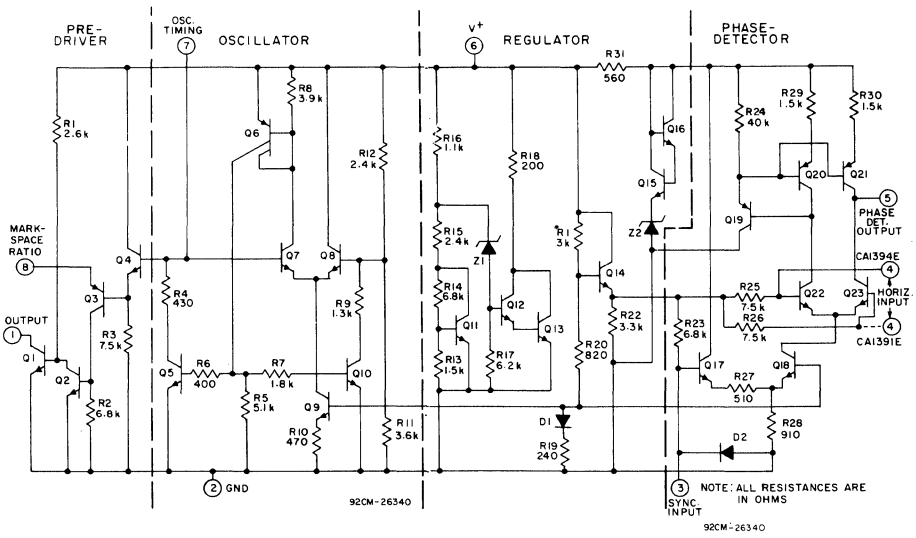


Fig.2 – Schematic diagram of CA1391E, CA1394E.

The phase detector is isolated from the remainder of the circuit by R31, Z2, Q15 and Q16. The phase detector consists of the comparator Q22 and Q23, and the gated current source Q18. Negative-going sync pulses at terminal 3 turn off Q17, and the current division between Q22 and Q23 is then determined by the phase relationship of the sync and the sawtooth waveform at terminal 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents flow in the collectors of Q22 and Q23 during each half of the sync pulse period. The current in Q22 is turned around by current mirror Q20 and Q21 so that there is no net output current at terminal 5 for balanced conditons. When a phase offset occurs, current flows either in or out of terminal 5. In circuit applications, this terminal is connected to terminal 7 through an external low-pass filter, thereby controlling the oscillator.

Shunt regulation for the circuit is obtained by using a V_{BE} and zener multiplier. Resistors R13 and R14 multiply the V_{BE} of Q11, and the ratio of R15 and R16 multiplies the voltage of the zener diode Z1.

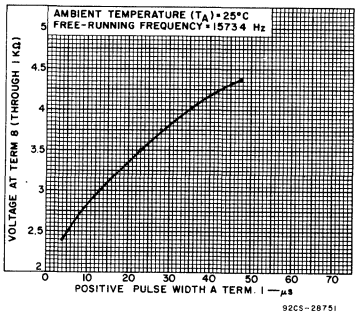


Fig.3 – Duty cycle at the pre-drive output (term.1) as it is affected by the input at term. 8.

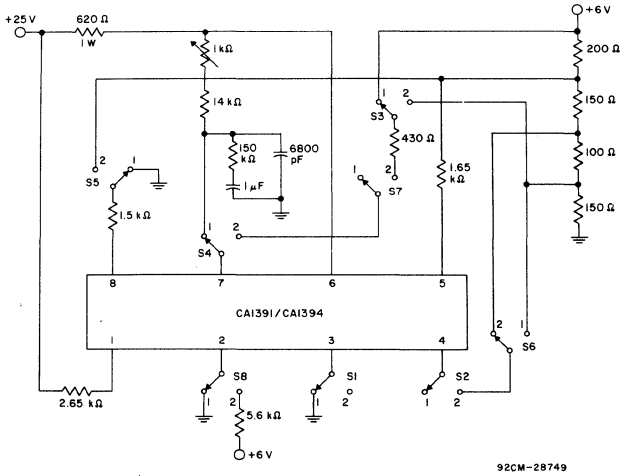


Fig.4 – DC test circuit.

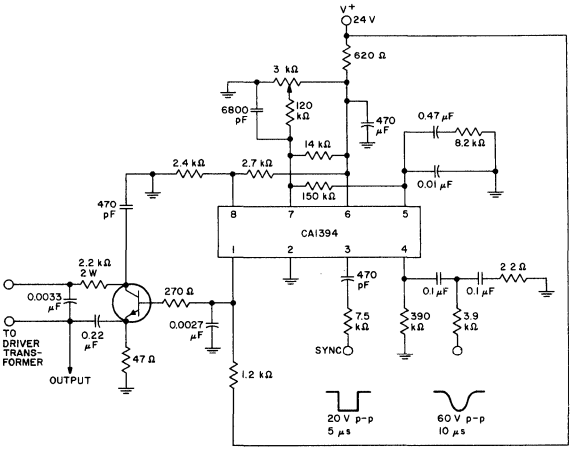


Fig.5 – Typical circuit application.

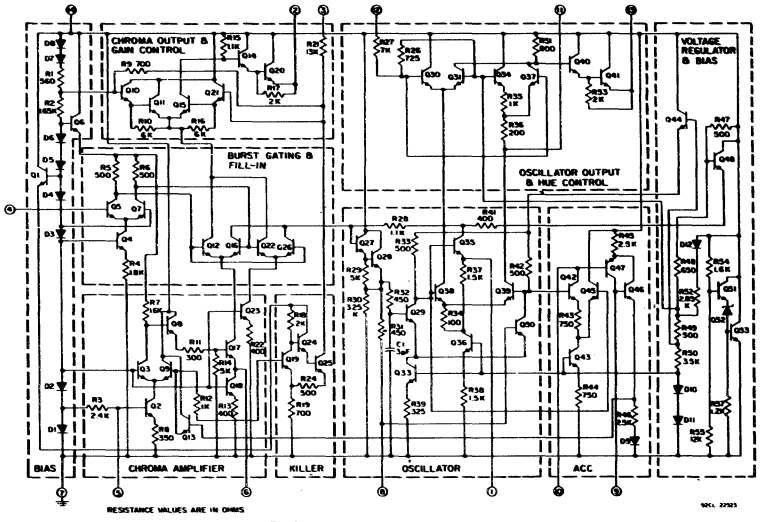


Fig. 3 – Schematic diagram of the CA1398E.

TEST SET-UP PROCEDURE FOR OSCILLATOR

Remove the horizontal keying and chroma inputs and adjust C_X to obtain a free-running oscillator frequency of 3.579545 MHz ±10 Hz. Under the same Test Conditions described in the Electrical Characteristics Chart for Oscillator Lock-Up, vary L1 (approx. 20 μH) and/or C1 (approx. 1000 pF) to obtain the initial conditions for amplitude and phase oscillator lock-up.

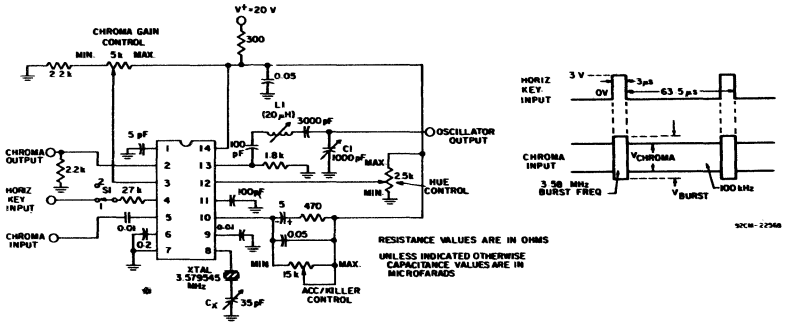


Fig. 4 – Typical static and dynamic characteristics test circuit for the CA1398E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 14.4 V
Unless otherwise specified (See Figure 2)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage, V^+		8	–	18	V
Quiescent Output Voltage, V_O	Measure at Term. 4	6.4	7.2	8	V
Quiescent Drain Current, I_D	Measure at Term. 5	–	45	80	mA
Output Power, P_O	THD = 10%, A = 40 dB, f = 1 KHz; V^+ = 14.4V; R_L = 4 Ω	4.8	5.2	–	W
	V^+ = 14.4V; R_L = 2 Ω	7	8	–	W
	V^+ = 16 V; R_L = 4 Ω	–	6.5	–	W
	V^+ = 16 V; R_L = 2 Ω	–	10	–	W
Input Saturation Voltage, $V_{I(RMS)}$		400	–	–	mV
Input Sensitivity, e_I	A = 40 dB, f = 1 KHz; P_O = 0.5 W, R_L = 4 Ω	–	15	–	mV
	P_O = 0.5 W, R_L = 2 Ω	–	11	–	mV
	P_O = 5.2 W, R_L = 4 Ω	–	55	–	mV
	P_O = 8 W, R_L = 2 Ω	–	50	–	mV
Frequency Response (–3 dB)	R_L = 4 Ω, C_X = 39 nF, R_X = 39 Ω (See Figs.15,20)	40 to 15000			Hz
Input Resistance, R_I (Term. 1)	f = 1 KHz	70	150	–	KΩ
Open-Loop Voltage Gain, A_{OL}	R_L = 4 Ω, f = 1 KHz	–	80	–	dB
Closed-Loop Voltage Gain, A	R_L = 4Ω, f = 1 KHz	39.5	40	40.5	dB
Input Noise Voltage, e_N	Freq. Resp. = 40 to 15,000 Hz (–3 dB)	–	4	–	μV
Input Noise Current, i_N	Freq. Resp. = 40 to 15,000 Hz (–3 dB)	–	60	–	pA
Efficiency, η	A = 40 dB, f = 1 KHz; P_O = 5.2 W, R_L = 4 Ω	–	68	–	%
	P_O = 8 W, R_L = 2 Ω	–	58	–	%
Power Supply Rejection Ratio, PSRR	R_L = 4 Ω, A = 40 dB, Rg = 10 KΩ, f_{ripple} = 100 Hz, V_{ripple} = 0.5 V	30	35	–	dB

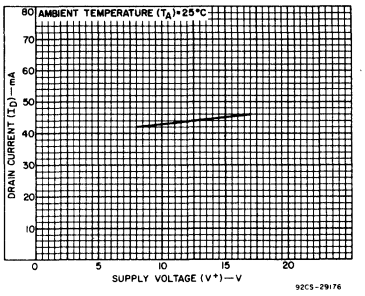


Fig. 4 – Typical quiescent drain current as a function of supply voltage.

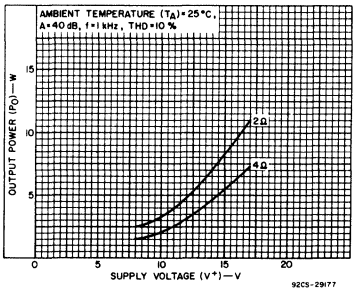


Fig. 5 – Typical output power as a function of supply voltage.

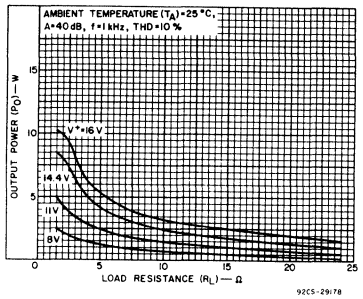


Fig. 6 – Typical output power as a function of load resistance.

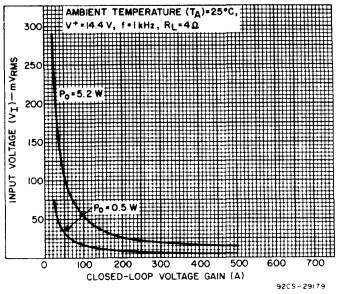


Fig. 7 – Typical input voltage as a function of closed-loop voltage gain.

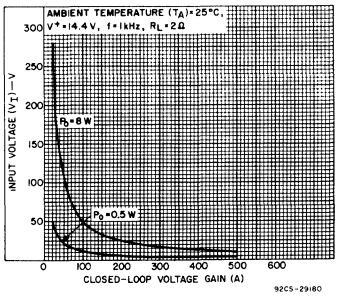


Fig. 8 – Typical input voltage as a function of closed-loop voltage gain.

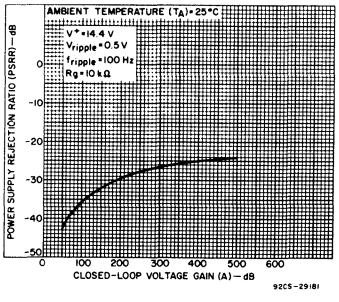


Fig. 9 – Typical power supply rejection ratio as a function of closed-loop voltage gain.

12-Watt Audio Power Amplifier

The RCA-CA2004 is a monolithic silicon class B audio power amplifier designed for driving loads as low as 3.2 Ω. It provides a high output current capability (up to 3.5 A), and very low harmonic and cross-over distortion.

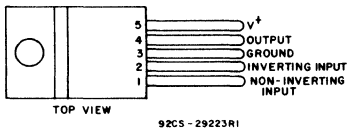
The CA2004 is supplied in a hermetic tri-metal Gold-CHIP encapsulated in the 5-lead plastic TO-220-style VERSA-V package. All leads (except term. 3) are electrically insulated from the mounting flange, eliminating the need for insulating hardware. The VERSA-V package is available with two lead configurations. The CA2004 has a vertical-mount lead form, and the CA2004M has a horizontal-mount lead form.

Features:

- **Hermetic Gold-CHIP encapsulated in a 5-lead plastic TO-220-style package (VERSA-V)**
- **Thermal overload protection**
- **Drives load impedance as low as 3.2 Ω**
- **Deflection amplifier capability**
- **Output current capability of up to 3.5 A**
- **Few external components**
- **VERSA-V power transistor package-requires no electrical insulation**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	28 V
OPERATING SUPPLY VOLTAGE	26 V
OUTPUT PEAK CURRENT:	
REPETITIVE	3.5 A
NON-REPETITIVE	4.5 A
POWER DISSIPATION, P_D at T_A = 90°C	15 W
THERMAL RESISTANCE, JUNCTION TO CASE	4°C/W
AMBIENT-TERMPERATURE RANGE:	
OPERATING	0 to +125°C
STORAGE	−40 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 12 s max.	260°C



TERMINAL ASSIGNMENT

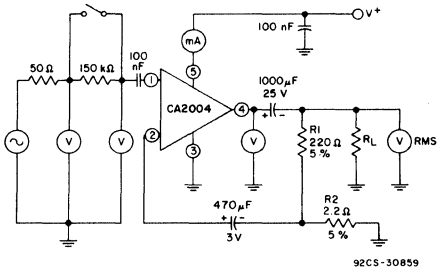


Fig. 1 – Test circuit.

Thermal Shut-Down

Thermal shut-down occurs if the output overloads (temporary or permanent), the ambient temperature is excessive, or the junction temperature is excessive. None of these conditions results in device damage. They merely cause a temporary automatic reduction of output power and drain current.

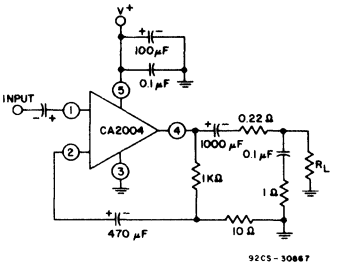


Fig. 2 – Typical application.

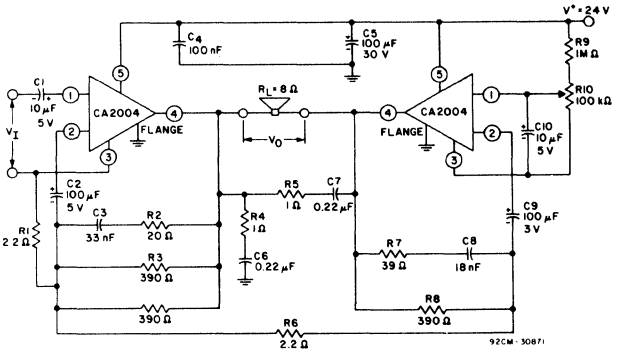


Fig. 3 – 25 W circuit-bridge application.

Ultra-High-Gain Wide-Band Amplifier Array

- Three Individual General-Purpose Amplifiers
- Ideal for service in Remote-Control Amplifiers — — e.g., TV Receivers
- Available in two electrically identical versions: CA3035 with straight leads; CA3035V1 with formed leads

HIGHLIGHTS

- Three separate amplifiers — gain and bandwidth for each amplifier can be adjusted with suitable external circuitry
- Amplifiers operable independently or in cascade
- Exceptionally high cascade voltage gain — 129 dB typ. at 40 kHz
- Low noise performance
- Wide-band response
- All amplifiers single-ended — only one power supply required
- Wide operating temperature range — -55°C to +125°C
- Built-in temperature compensation
- Hermetically sealed, all-welded 10-lead TO-5-style metal package with straight or formed leads

ABSOLUTE-MAXIMUM RATINGS:

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Device Dissipation ..... 300 mW
Input Voltage ..... 1 V p-p
Supply Voltage ..... +15V
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUITS AND CHARACTERISTICS CURVES	LIMITS CA3035, CA3035V1 Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
Quiescent Operating Voltage	V3 V5 V7	V_{CC} = +9V	Fig.3	– – –	2 1.9 4.9	– – –	V V V
Total Current Drain	I_d	V_{CC} = +9V, R_{L3} = 5KΩ	Fig.3	3.5	5	7.5	mA
DYNAMIC CHARACTERISTICS							
Voltage Gain: Amplifier No.1 Amplifier No.2 Amplifier No.3	 A_1 A_2 A_3	 f = 40 kHz, V_{CC} = +9V		 40 40 38	 44 46 42	 – – –	 dB dB dB
Output Voltage Swing	V_{out} V_{1out} V_{2out} V_{3out}	 R_{L1} = 10KΩ R_{L2} = 10KΩ R_{L3} = 5KΩ Sinusoidal Output, V_{CC} = +9V		 – – –	 2 2.6 8	 – – –	 Vp-p Vp-p Vp-p
Input Resistance: Amplifier No.1 Amplifier No.2 Amplifier No.3	 R_1in R_2in R_3in	 f = 40 kHz		 – – –	 50K 2K 670	 – – –	 Ω Ω Ω
Output Resistance	R_1out R_2out R_3out	 f = 40 kHz		 – – –	 270 170 100K	 – – –	 Ω Ω Ω
Bandwidth at -3dB point: Amplifier No.1 Amplifier No.2 Amplifier No.3	 BW_1 BW_2 BW_3	 V_{CC} = +9V	 Fig.5 Fig.6 Fig.7	 – – –	 500 2.5 2.5	 – – –	 kHz MHz MHz
Noise Figure Amplifier No.1	NF_1	f = 1 kHz, R_S = 1 KΩ	Fig.4	–	6	7	dB
Sensitivity		V_{CC} = +13 V Relay (K_1) Current = 7.5 mA	Fig.2	–	100	150	μV

SCHEMATIC DIAGRAM FOR CA3035 AND CA3035V1

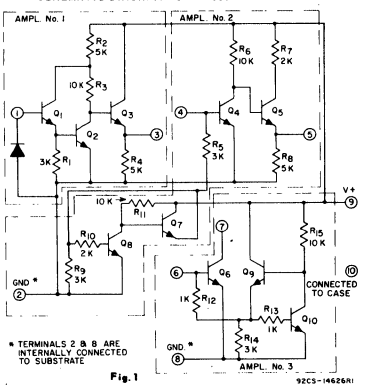


Fig. 1

TYPICAL REMOTE CONTROL SYSTEM

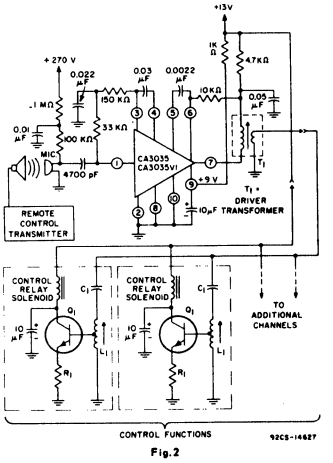


Fig.2

STATIC CHARACTERISTICS TEST CIRCUIT

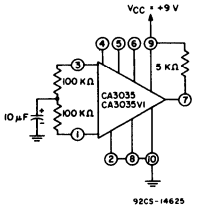
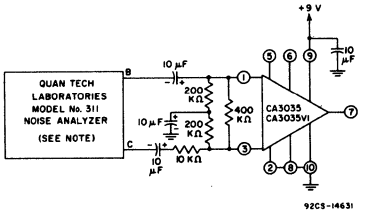


Fig.3

NOISE FIGURE TEST CIRCUIT



NOTE: SET ALL INTERNAL POWER SUPPLIES ON QUAN TECH NOISE ANALYZER TO ZERO VOLTS.

Fig.4

ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3041 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP AND PROCEDURE Fig.	TEST CONDITIONS: SPECIAL CONDITIONS	LIMITS: TYPE CA3041 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
Total Device Dissipation	P_T	11	T_A = 0°C	220	245	270	mW	2
			T_A = +25°C	225	250	275	mW	
			T_A = +85°C	230	255	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	-		10.5	11.2	12.3	V	-
Quiescent Operating Current (into Terminal 11)	I_{11}	11		0.25	0.63	1	mA	-
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	11	V_{CC} = +9 V applied directly to Terminal 14	7	11	16	mA	-
Input-Impedance Components: Parallel Input Resistance	R_i	3	f = 4.5 MHz	-	11	-	kΩ	-
Parallel Input Capacitance	C_i	3		-	5	-	pF	-
Output-Impedance Components: Parallel Output Resistance	R_o	-		-	100	-	kΩ	-
Parallel Output Capacitance	C_o	-		-	4	-	pF	-
Input Limiting Voltage (Knee)	$V_{i(lim)}$	7		-	150	200	μV (rms)	4
Amplitude-Modulation Rejection	AMR	10		45	58	-	dB	9
IF-Amplifier Voltage Gain	$A_{(IF)}$	5		-	67	-	dB	4
Recovered AF Voltage: 1. At FM-Detector Output	$V_{o(af)}$	-	R_L = 50 kΩ, Δf = ±25 kHz THD = 0.7% (typ.)	-	250	-	mV (rms)	-
2. At AF-Driver Output in Test Setup		-	THD < 5%	8	9	-	V (rms)	-
Total Harmonic Distortion	THD	7	$V_{o(af)}$ = 8 V(rms)	-	1.5	5	%	-
Discriminator Output Resistance	$R_{o(dis)}$	-	f = 1 kHz	-	10	-	kΩ	-
AF-Amplifier Input Resistance	$R_{i(af)}$	-		-	100	-	kΩ	-
AF-Amplifier Output Resistance	$R_{o(af)}$	-		-	30	-	kΩ	-
AF-Driver Voltage Gain	A_{af}	6		-	41	-	dB	8

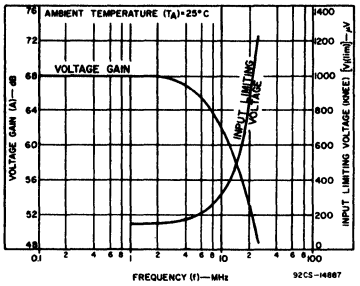
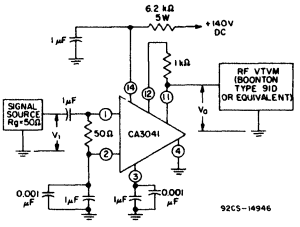


Fig.4 - Typical IF-amplifier voltage gain and input-limiting voltage (knee) characteristics.



PROCEDURE:

A - Voltage Gain:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

Fig.5 - Test setup for measurement of IF-amplifier voltage gain.

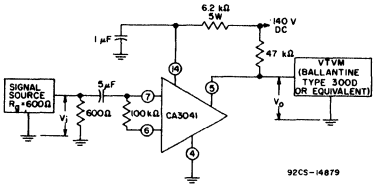
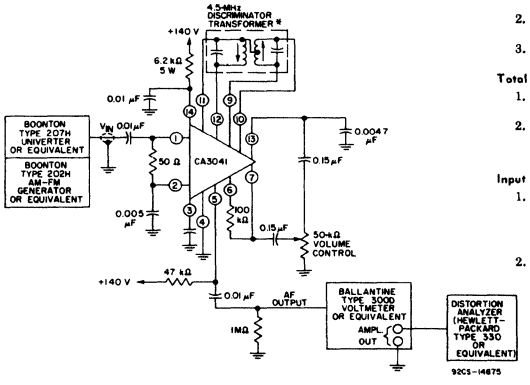


Fig.6 - Test setup for measurement of AF-amplifier voltage gain.



* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.7 - Test setup for measurement of input limiting voltage (Knee), recovered AF voltage, and total harmonic distortion.

PROCEDURES:

Recovered AF Voltage:

1. Set Input Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1 kHz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output.
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 300 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (300 mV - 3 dB = 210 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).

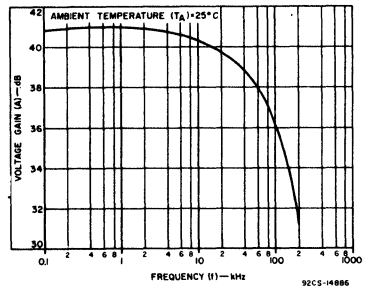


Fig.8 - Typical AF-driver voltage-gain characteristic

Wideband Amplifier, FM Detector, AF Preamplifier/Driver

CA3042

For Sound Sections of TV Receivers Using Transistor-Type AF Output Amplifiers

FEATURES

- high sensitivity – input limiting voltage (knee) = 150 μV typ. at 4.5 MHz
- 6-mA audio drive capability
- excellent AM rejection – 58 dB typ. at 4.5 MHz
- inherent high stability – internally shielded
- internally Zener-diode-regulated voltage supply
- low harmonic radiation
- wide frequency capability – <100 kHz to >20 MHz
- low harmonic distortion

RCA Integrated Circuit Type CA3042 provides, in a single monolithic silicon chip, a major sub-system for the sound sections of TV receivers. As shown in the Schematic Diagram (Fig.1) and the TV Receiver Block Diagrams (Figs.2A and 2B) the CA3042 contains a multistage wide-band if-amplifier section, an FM-detector stage, a Zener-diode-regulated power-supply section, and an af-amplifier section specifically designed to drive directly an n-p-n audio output transistor or a high-gain audio output pentode tube.

In FM receivers, the CA3042 can be used to provide if amplification and limiting, FM detection, and af preamplification.

The CA3042 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The CA3042 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitably punched printed-circuit boards.

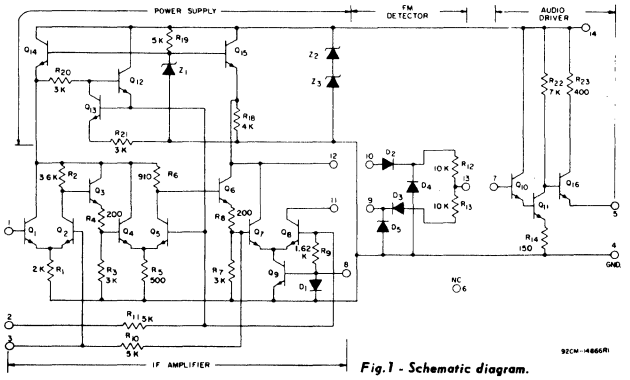


Fig.1 - Schematic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

OPERATING-TEMPERATURE RANGE	−40° to +85°C
STORAGE-TEMPERATURE RANGE	−65° to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:	
Between Terminals 1 and 3	±3 V
MAXIMUM DEVICE DISSIPATION:	
At Ambient up to +25°C	950 mW
Temperatures above +25°C	Derate at 10.8 mW/°C

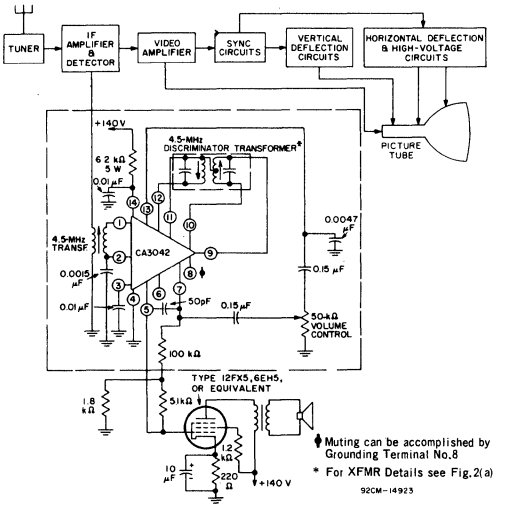


Fig.2(b) - Block diagram of typical TV receiver utilizing the CA3042 and a 12FX5, 6EH5, or equivalent.

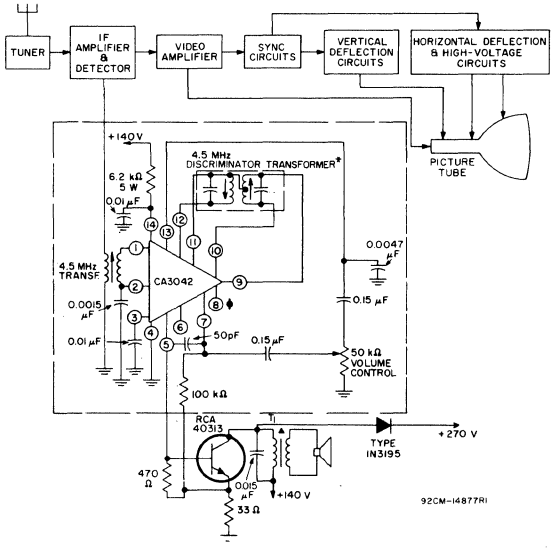
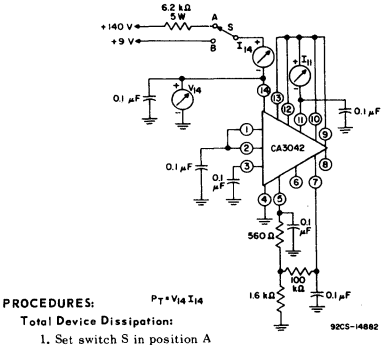


Fig. 2(a) - Block diagram of typical TV receiver utilizing transistor RCA-40313.



PROCEDURES: $P_T = V_{14} I_{14}$

Total Device Dissipation:

1. Set switch S in position A
2. Measure and record V_{14} and I_{14}.
3. Determine Total Device Dissipation from $P_T = V_{14} I_{14}$

Quiescent Operating Current into Terminal 11:

1. Turn switch S to position B
2. Measure I_{11} and record as Quiescent Operating Current into Terminal 11.

9-Volt Current Drain:

1. Set switch S in position B
2. Measure I_{14} and record as 9-Volt Current Drain.

Fig.3 - Test setup for measurement of total device dissipation, quiescent current into terminal No.11, and 9-volt current drain.

ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3042 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP AND PROCEDURE Fig.	TEST CONDITIONS: SPECIAL CONDITIONS	LIMITS: TYPE CA3042 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
Total Device Dissipation	P_T	3	T_A = 0°C	200	230	260	mW	4
			T_A = +25°C	210	240	270	mW	
			T_A = +85°C	220	250	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	–		10.5	11.2	12.3	V	–
Quiescent Operating Current (into Terminal 11)	I_{11}	3		0.25	0.63	1	mA	–
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	3	V_{CC} = +9 V applied directly to Terminal 14	8	12	18	mA	–
Input-Impedance Components: Parallel Input Resistance	R_I	5	f = 4.5 MHz	–	11	–	kΩ	–
Parallel Input Capacitance	C_I	5	f = 4.5 MHz	–	5	–	pF	–
Output-Impedance Components: Parallel Output Resistance	R_O	–		–	100	–	kΩ	–
Parallel Output Capacitance	C_O	–		–	4	–	pF	–
Input Limiting Voltage (Knee)	$V_{i(lim)}$	11		–	150	200	μV (rms)	8
Amplitude-Modulation Rejection	AMR	7	f = 4.5 MHz	45	58	–	dB	
IF-Amplifier Voltage Gain	$A_{(IF)}$	6	f = 4.5 MHz	–	67	–	dB	8
Recovered AF Voltage: 1. At FM-Detector Output	$V_{O(af)}$	11	f = 4.5 MHz, Δf = ±25 kHz, R_L = 50 kΩ, THD = 0.7% (typ.)	–	250	–	mV (rms)	–
2. At AF-Driver Output in Test Setup		11	f = 4.5 MHz, Δf = ±25 kHz, R_L = 322 Ω, THD < 5%	500	800	–	mV (rms)	–
3. At AF-Driver Output in TV-Receiver Sound System		2A or 2B	f = 4.5 MHz, Δf = ±25 kHz, R_L = 150 kΩ, THD = 1.5% (typ.)	–	3	–	V (rms)	–
Total Harmonic Distortion: 1. In Test Setup	THD	11	f = 4.5 MHz, Δf = ±25 kHz, $V_{O(af)}$ = 500 mV (rms)	–	1.5	5	%	–
2. In TV Receiver Sound System		2A or 2B	f = 4.5 MHz, Δf = ±25 kHz, $V_{O(af)}$ = 1.3 V (rms)	–	1	–	%	–
FM-Detector Output Resistance	$R_{O(det)}$	–	f = 1 kHz	–	10	–	kΩ	–
AF-Driver Input Resistance	$R_{I(af)}$	–	f = 1 kHz	–	100	–	kΩ	–
AF-Driver Output Resistance	$R_{O(af)}$	–	f = 1 kHz	–	250	–	Ω	–
AF-Driver Voltage Gain	A_{af}	9	f = 1 kHz, R_S = 50 Ω, C_1 = 0	–	30	–	dB	10

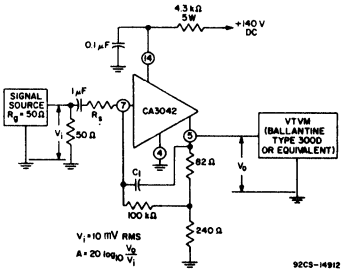


Fig.9 - Test setup for measurement of AF amplifier voltage gain.

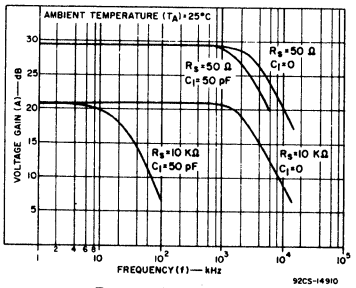
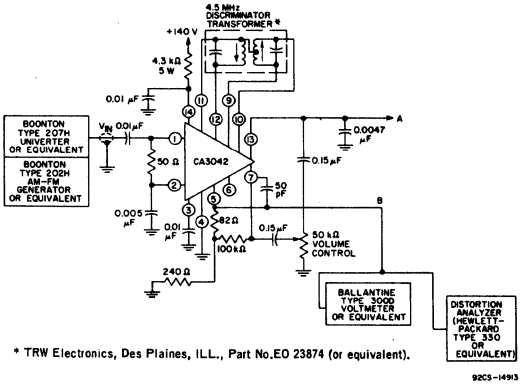


Fig.10 - Typical AF amplifier voltage gain characteristics.



* TRW Electronics, Des Plaines, ILL., Part No.EO 23874 (or equivalent).

PROCEDURES:

Recovered AF Voltage:

1. Set Input Signal Generator as follows:
   - Output frequency = 4.5 MHz
   - Modulating frequency = 1 kHz
   - Deviation = ±25 kHz
   - Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 500 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (500 mV - 3 dB = 350 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).

Fig.11 - Test setup for measurement of input limiting voltage (knee), recovered AF voltage, and total harmonic distortion.

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range between horizontal terminal 5 and vertical terminal 3 is +6 to 0 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		+4 -4	0 -5	*	*	*	*	*	*	0 -5	*	Note(1)
2			0 -3	*	*	*	*	*	*	0 -3	*	*
3				+6 0	+6 0	+15 +2	+6 0	+6 0	+6 0	0	Note(2)	+3 0
4					+2 -4	*	*	*	*	0 -6	*	*
5						*	*	*	*	0 -6	+6 0	*
6							*	*	*	-2 -15	*	*
7								Note(1)	*	0 -6	*	*
8									*	0 -6	*	*
9										0 -6	*	*
10											Note(2) 0	+3 0
11												*
12												

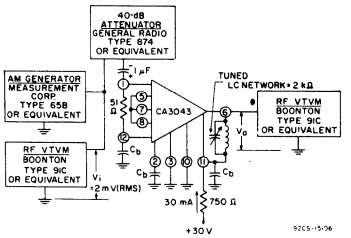
MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	-
2	-	-
3	0.1	40
4	-	20
5	-	-
6	-	-
7	-	-
8	-	-
9	-	20
10	0.1	40
11	40	0.1
12	-	-

Note 1: These terminals should be connected through a dc resistance to any terminal which does not exceed 100 ohms.

Note 2: Pin 11 may be connected to any positive voltage source through a suitable resistor provided its current rating is not exceeded.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.



Voltage Gain = $20 \log_{10} 100 \frac{V_o}{V_i}$

C_b - Bypass Capacitor, 0.1 μF electrolytic in parallel with 0.01 μF

$I_6(lim) = \frac{V_o}{2K\Omega}$, v_i = 100 mV(RMS)

* Output circuit should be completely shielded from the input circuit at the socket.

Fig.4 - Voltage gain test circuit.

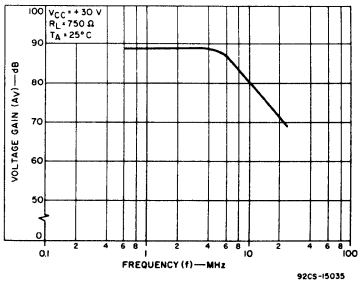
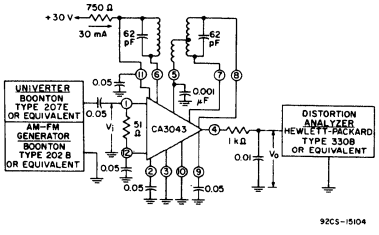


Fig.5 - Voltage gain vs frequency.



PROCEDURE:

1. Recovered Audio Voltage $v_{o(af)}$ –
   Set input frequency to 10.7 MHz,
   v_i = 1 mV(RMS), modulating frequency = 1 kHz
   Deviation = ±75 kHz
   Record v_o as measured on the Distortion Analyzer meter scale.
   This is the recovered Audio Voltage $v_{o(af)}$
2. 3 dB Limiting Sensitivity $v_{i(lim)}$ –
   Reduce v_i until $v_{o(af)}$ drops 3 dB.
   Record this value of v_i as $v_{i(lim)}$
3. Total Harmonic Distortion THD –
   Reset v_i to 1 mV(RMS) and operate Distortion Analyzer per manufacturer's instructions to measure THD.

* See Fig.9 for details on Discriminator Transformer.

Fig.6 - Input limiting voltage (knee), recovered AF voltage, and total harmonic distortion test circuit.

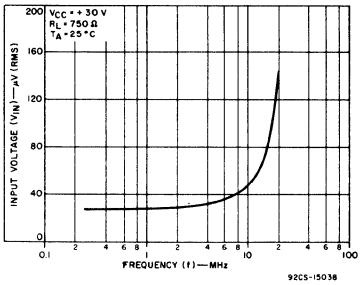
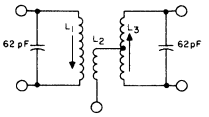
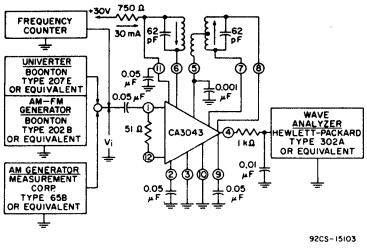


Fig.7 - Input limiting voltage (knee) at -3 dB point vs frequency.



Coil Form, Outside Diameter = 7/32"
Can = 1/2" square X 1-1/8" long
Slugs - Radio Industries Type MP34/MP100 Material
L_1 & L_3 = 20 Turns 5-44 litz wire universal wound
L_2 = 10 Turns 5-44 litz wire wound bifilar with L_1
L_1 & L_3 coupling adjusted to 520 kHz peak to peak separation on S curve when operated in circuit shown in Fig.6.

Fig.9 - 10.7-MHz discriminator transformer for CA3043.



PROCEDURE:

A. Connect FM Generator to CA3043 input.
   Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz
   Deviation = ±75 kHz.
   Tune Wave Analyzer to peak reading at 1 kHz and record recovered Audio Voltage $v_{o(af)FM}$.
B. Disconnect FM Generator and Connect AM Generator to CA3043 input.
   Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz, percent modulation = 50%.
   Tune Wave Analyzer to peak reading and record recovered audio voltage $v_{o(af)AM}$
   Amplitude Modulation Rejection Ratio = $20 \log_{10} \frac{V_{o(af)FM}}{V_{o(af)AM}}$

Fig.8 - Amplitude modulation rejection test circuit.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS FIG.	TEST CONDITIONS	LIMITS CA3044 and CA3044V1 MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS								
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = -55°C	90	120	150	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = 25°C	110	140	170	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = +125°C	130	160	190	mW	-
9-Volt Current Drain	I_T	3	V_{10} = 9 V	2.5	4	5.5	mA	-
Zener Regulating Voltage - DC Supply Voltage at Terminal 10	V_{10}	3	V_{CC} = 30 V, R_S = 1.5 kΩ	10.5	11.2	11.9	V	-
Quiescent Operating Current into Terminal 2	I_2	3		1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4	V_4	-		5.0	6.5	8.0	V	-
Quiescent Operating Voltage at Terminal 5	V_5	-		5.0	6.5	8.0	V	-
Output Offset Voltage between Terminals 4 and 5	V_{4-5}	-		-1.5	0	1.5	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER)								
Input Limiting Voltage (Knee)	V_i Limiting	4	f=45.75 MHz	-	75	-	mV	-
Input Admittance	y_{11}	-	f = 45.75 MHz, V_{CC} = 30 V, R_S = 1.5 kΩ	-	0.5+j1.1	-	mmho	-
Reverse Transfer Admittance	y_{12}	-		-	3.8+j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-		-	-11.7 +10.1	-	mmho	-
Output Admittance	y_{22}	-		-	0.077+j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC								
Correction-Control Voltage at Terminal 4	V corr. (4)	5	V_{CC} = +30 V, V_{in} = 200 mV RMS, f_0 = MHz as indicated	% of V_{10}		% of V_{10}		
			45.750 - 0.025	85	-	-	V	6,7
			45.750 + 0.025	-	-	33	V	
			45.750 - 0.900	75	-	-	V	7
			45.750 + 0.900	-	-	43	V	
			45.750 - 1.500	-	-	85	V	
			45.750 + 1.500	33	-	-	V	
Correction-Control Voltage at Terminal 5	V corr. (5)	5	45.750 - 0.025	-	-	33	V	6,7
			45.750 + 0.025	85	-	-	V	
			45.750 - 0.900	-	-	43	V	7
			45.750 + 0.900	75	-	-	V	
			45.750 - 1.500	33	-	-	V	
			45.750 + 1.500	-	-	85	V	

DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

The CA3044 and CA3044VI are specifically intended for use in the AFT system of color television receivers. Each device is tested so that the control voltages generated by the circuit meet the critical requirements of the system. Figure 5 is the schematic diagram of the test circuit.

Figure 6 and 7 show the control voltages generated at terminals 4 and 5 of the Integrated Circuit as a function of the frequency deviation from the nominal center frequency. Figure 6 shows the region within 25 KHz of the center frequency while Figure 7 covers the entire bandwidth of the system. The horizontal reference lines on the figures are generated by a voltage divider connected between the power supply voltage on Terminal 10 and ground. The dynamic control voltages are compared with these references according to the Output vs Frequency Deviation Table. For example: when the frequency deviation is -25 KHz the control voltage at Terminal 4 is greater than the reference A voltage; the control voltage at Terminal 5 is less than the reference B voltage.

The shape of the correction voltage characteristics is dependent to a large degree upon transformer characteristics and the parts layout. In order to closely duplicate the curves shown, the printed circuit board shown in Figure 8 and the parts layout shown in Figure 9 should be followed as closely as possible.

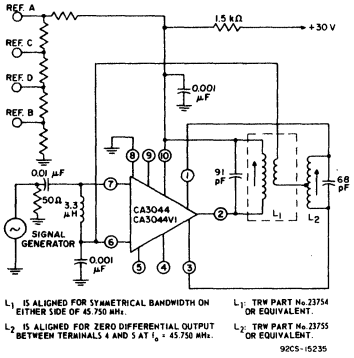


Fig.5 - Correction voltage test circuit for CA3044 and CA3044VI.

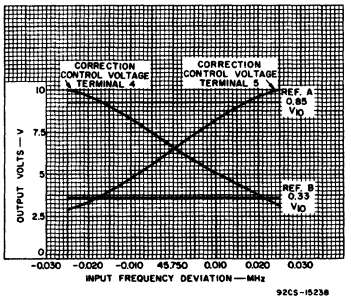


Fig.6 - Typical narrow-band dynamic control voltage characteristics.

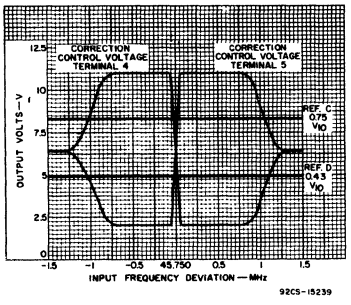


Fig.7 - Typical wide-band dynamic control voltage characteristics.

DEFINITIONS OF TERMS

Input Limiting Voltage (Knee) [v_i(lim)]
The input signal voltage which will cause the output signal to decrease 3 dB from its maximum level.

Total Device Dissipation (P_T)
The total power drain of the device with no signal applied and no external load current.

Quiescent Operating Voltage
The dc voltage at the output terminal, with respect to ground, with no signal applied.

Quiescent Operating Current
The average (dc) value of the current in either output, terminal, with no signal applied.

Output Offset Voltage
The dc voltage between output terminals with no signal applied.

Control Voltage
The dc voltage at either output terminal with respect to ground with an RF signal of specified frequency applied.

Four Independent AC Amplifiers

Special-Function Sub-System for Stereo Preamplifiers, Magnetic Pickups, Tape Heads, etc.

APPLICATIONS

- **Full-function stereo preamplifiers**
- **Tape recorder and playback preamplifiers**
- **Tone Generators**

FEATURES

- **Four AC amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Operates from single-ended supply**

EACH AMPLIFIER

- **High voltage gain . . . . 53 dB min.**
- **High input resistance . . 90 k Ω typ.**
- **Undistorted output voltage 2 V rms min.**
- **Output Impedance . . . 1 k Ω typ.**
- **Open-loop bandwidth . . 300 kHz typ.**

The RCA-CA3052 is a silicon monolithic integrated circuit designed specifically for stereo preamplifier service. The circuit consists of four independent ac amplifiers which can operate from a single-ended supply.

The CA3052 can operate as an equalizer amplifier in tape recorders, magnetic cartridge phonograph applications, and tone control amplifiers. It can provide all of the amplification necessary for a full-function stereo preamplifier.

The CA3052 is supplied in a 16-lead dual-in-line plastic package.

RCA-CA3052 is schematically identical with the CA3048 Amplifier Array (File No. 377). Each amplifier of the CA3048 is tightly specified for equivalent output noise under a variety of test methods. The CA3052 is specified using RIAA test methods for equivalent input noise using one test method for amplifiers 1 and 4, and an appropriately different method for amplifiers 2 and 3.

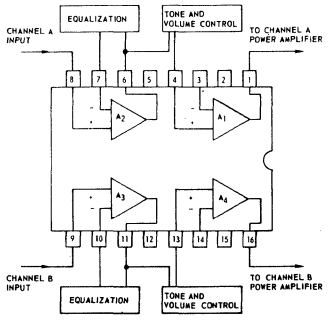


Fig. 1 – Block diagram of stereo preamplifier using CA3052.

ABSOLUTE-MAXIMUM RATING at T_A = 25°C:

POWER SUPPLY VOLTAGE . . . . . +16 V

AC INPUT VOLTAGE . . . . . 0.5 V rms

DISSIPATION:

Up to T_A = 55°C . . . . . 750 mW

Above T_A = 55°C . . . . . Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . −40°C to +85°C

Storage . . . . . −65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max. . . . . +265°C

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 −16	*
2			*	+2 −3.6	0	*	*	+2 −3.6	+2 −3.6	*	*	+16 0	+2 −3.6	*	+16 0	0 −16
3				+5 −5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 −2	*	*	*	*	*	*	*	*	*	*	*
5						0 −16	*	+2 −3.6	+2 −3.6	*	0 −16	+16 0	+2 −3.6	*	+16 0	*
6							*	*	*	*	*	*	0 −16	*	*	*
7								+5 −5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 −5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 −16	*	*	*
13														+5 −5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

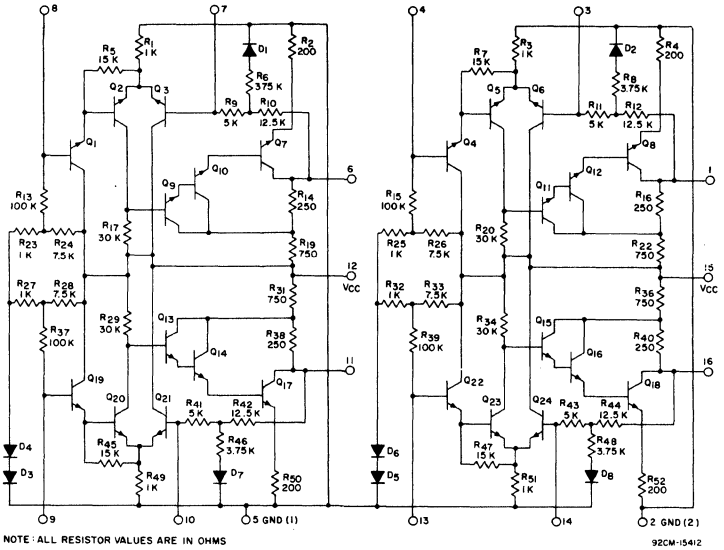


Fig. 2 — Schematic diagram for CA3052.

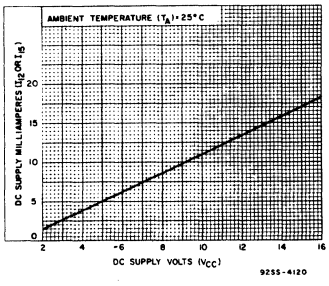


Fig. 4 — Typical DC supply current vs supply voltage.

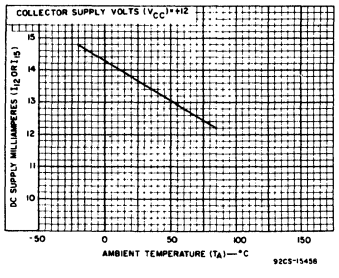


Fig. 5 — Typical DC supply current vs ambient temperature.

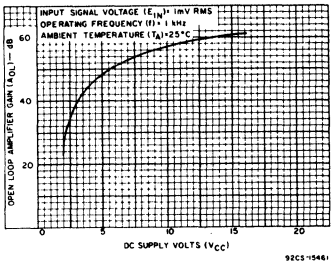


Fig. 7 — Typical amplifier gain vs DC supply voltage.

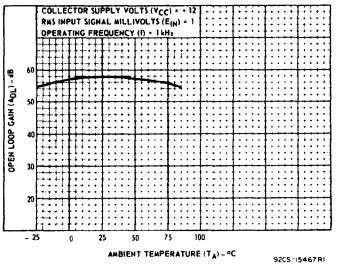


Fig. 8 — Typical open-loop gain vs ambient temperature.

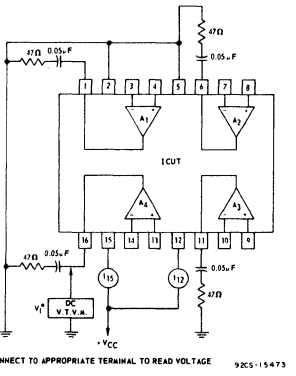
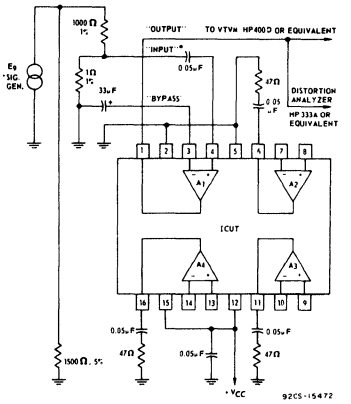


Fig. 3 — Test circuit for measurement of collector supply voltage and currents.



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_S to 2 volts will make E_S = 2 mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig. 6 — Test circuit for measurement of distortion, open-loop gain, and bandwidth characteristics.

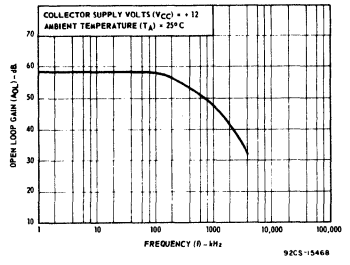


Fig. 9 — Typical open-loop gain vs frequency.

TV Automatic Fine Tuning Circuit

RCA-CA3064 and CA3064E represent the third generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications. They provide all of the signal-processing components needed (with the exception of the tuned-phase-detector transformer) to derive the AFT correction signals from the output of the video-if amplifier. The CA3064 is supplied in the 10-formed-lead TO-5 style package, and the CA3064E in the 14-lead dual-in-line plastic package. Both types operate over the temperature range of −55 to +125°C.

The CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1 but embody a higher-gain input amplifier which provides a 20-dB improvement in sensitivity. The increased sensitivity extends the application of a proven AFT system to the low-level if-amplifier stages in TV receivers.

Because the CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1, refer to Application Note ICAN-5831, "Application of the RCA CA3044 and CA3044V1 Integrated Circuits in Automatic Fine-Tuning Systems" for general application information.

Features:

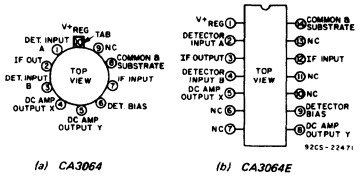
- **Cascode type high-gain amplifier (18 mV input for rated output)**
- **Internal voltage regulator**
- **Differential detector**
- **For use with either color or monochrome**
- **Differential amplifier**
- **Bipolar outputs**
- **Wide operating-temperature range; −55 to +125°C**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DEVICE DISSIPATION:
Up to T_A = 25°C . . . . . 700 mW
Above T_A = 25°C . . . . . derate linearly 5.6 mW/°C

AMBIENT TEMPERATURE RANGE:
Operating . . . . . −55 to +125°C
Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max.. . . . . 265°C



(a) CA3064 *(b) CA3064E*

Fig.2 – Terminal assignment diagrams.

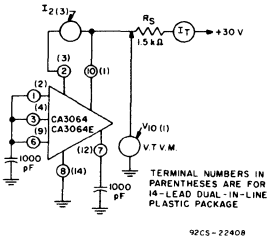


Fig. 3 – Test setup: Measurement of total device dissipation, zener regulating voltage, quiescent operating current at terminal 2 (3).

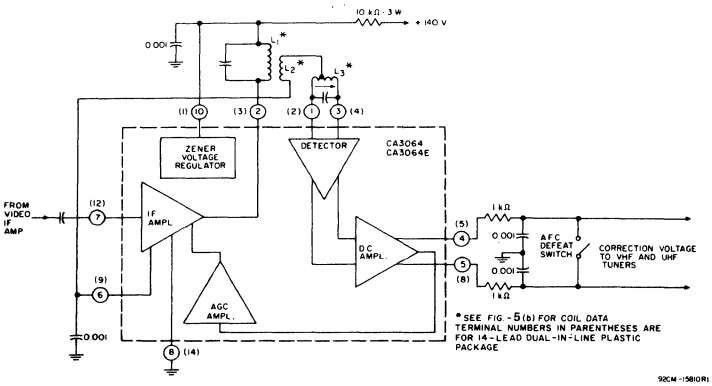


Fig.1 – Block diagram of typical operating circuit utilizing the CA3064 and CA3064E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS	TEST CONDITIONS		LIMITS CA3064, CA3064E			UNITS	CHARACTERISTIC CURVES
		FIG.			MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS									
Device Dissipation	P_D	3	V+ = 30V, R_S = 1.5kΩ	T_A = −25°C	-	135	150	mW	-
				T_A = +25°C	130	140	150		-
				T_A = +85°C	-	145	150		-
Current Drain at 10.5 Volts	I_T	3	$V_{10(1)}$ = 10.5 V		4	6.5	9.5	mA	-
Zener Regulated Voltage – DC Supply Voltage at terminal 10(1)*	$V_{10(1)}$	3			10.9	11.8	12.8	V	-
Quiescent Operating Current into Terminal 2(3)	$I_{2(3)}$	3			1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4(5)	$V_{4(5)}$	-	V+ = 30 V, R_S = 1.5 kΩ		5	6.9	8	V	-
Quiescent Operating Voltage at Terminal 5(8)	$V_{5(8)}$	-			5	6.9	8	V	-
Output Offset Voltage between Terminals 4 and 5(5 and 8)	V_{4-5} (5-8)	-			-1	0	1	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER IN TO-5 STYLE PACKAGE)									
Input Voltage Sensitivity	V_I sensitivity	5	V+ = +30 V, V_I = 18 mV		Correction Voltage Output as shown in table below.				
Input Admittance	y_{11}	-	f = 45.75 MHz, V+ = 30 V, R_S = 1.5 kΩ		-	0.41 + j1.0	-	mmho	-
Reverse Transfer Admittance	y_{12}	-			-	0 +j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-			-	24.5 - j29	-	mmho	-
Output Admittance	y_{22}	-			-	0.04 + j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC									
Correction-Control Voltage at Terminal 4(5)	V corr. 4(5)	5	V+ = +30 V, V_I = 18 mV RMS, f_0 = MHz as indicated		% of V_{10} (1)		% of V_{10} (1)		
				45.750 - 0.030	85	-	-	V	6,7
				45.750 + 0.030	-	-	25	V	
				45.750 - 0.900	80	-	-	V	7
				45.750 + 0.900	-	-	35	V	
				45.750 - 1.500		-	80	V	
				45.750 + 1.500	35	-		V	
Correction-Control Voltage at Terminal 5(8)	V corr. 5(8)	5		45.750 - 0.030	-	-	25	V	6,7
				45.750 + 0.030	85	-	-	V	
				45.750 - 0.900	-	-	35	V	7
				45.750 + 0.900	80	-	-	V	
				45.750 - 1.500	35	-	-	V	
				45.750 + 1.500	-	-	80	V	

* Terminal numbers in parentheses are for 14-lead dual-in-line plastic package.

IF Amplifier-Limiter, FM Detector, Electronic Attenuator, Audio Driver

For Television Sound-System Applications

The RCA CA3065 Television Sound System is a monolithic integrated circuit which combines a multistage IF amplifier limiter, an FM detector, an electronic attenuator, a zener diode regulated power supply, and an audio amplifier-driver that is designed to directly drive an npn power transistor or high-transconductance tube. Because the circuit is so inclusive, a minimum number of external components is required. A block diagram of the integrated circuit television sound system is shown in Fig. 1.

The CA3065 with its advanced circuit design provides a high-performance multistage subsystem for the sound system of a television receiver. A particular feature of the CA3065 is the electronic attenuator which performs the conventional volume control function. Volume control is accomplished when the bias levels in the attenuator are changed by means of a variable resistor connected between Terminal 6 and ground (attenuation in excess of 60 dB is attained). Because no audio signal is present in this control, hum or noise pickup can be bypassed. In most cases, only a single unshielded wire is required between the IF board and the variable resistor (volume control).

The CA3065 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device into suitably punched printed-circuit boards.

FEATURES:

- Electronic attenuator - replaces conventional volume control
- Differential peak detector - requires one single tuned coil
- Internal Zener diode regulated supply
- Inherent high stability
- Excellent AM rejection - 50 dB typ. at 4.5 MHz
- Low harmonic distortion
- High sensitivity - 200 μV limiting (knee) at 4.5 MHz
- Audio drive capability - 6 mA p-p
- Undistorted audio output voltage - 7 V p-p

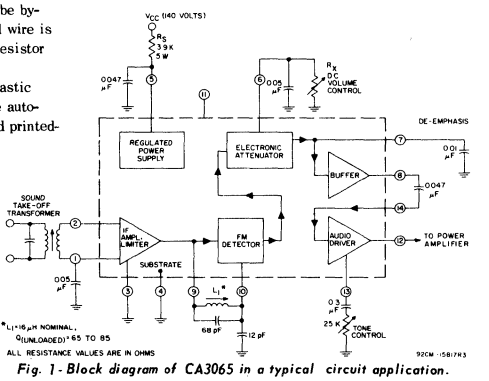


Fig. 1 - Block diagram of CA3065 in a typical circuit application.

MAXIMUM RATINGS, *Absolute Maximum Values*, at T_A = 25°C

Input Signal Voltage (between Terminals 1 and 2)	±3	V
Power Supply Current (Terminal 5)	50	mA
Power Dissipation:		
Up to T_A = 25°C	850	mW
Above T_A = 25°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	-40 to +85	°C
Storage	-65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 9 with respect to terminal 3 is 0 to +4 volts.

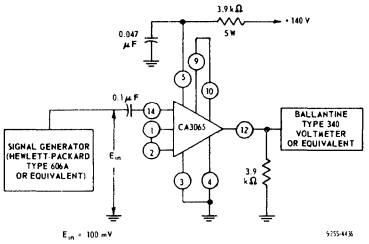
TERMINAL No.	4	5	6	7	8	9	10	11	12	13	14	1	2	3
4		SUBSTRATE CONNECTION – ALWAYS CONNECT TO TERMINAL 3												
5			+13 0	+13 0	+13 0	*	*	INTERNAL CONNECTION DO NOT USE	+13 0	+13 0	*	*	*	NOTE 1
6				*	*	*	*		*	*	*	*	*	+13 −5
7					+1 −4	*	*		*	*	*	*	*	+13 0
8						*	*		*	*	*	*	*	*
9							*		*	*	*	*	*	+4 0
10									*	*	*	*	*	+4 −5
11									INTERNAL CONNECTION DO NOT USE					
12										+4 −1	*	*	*	*
13											*	*	*	*
14												*	*	+3 −5
1													+5 −5	+5 −5
2														+4 −5
3														

MAXIMUM CURRENT RATINGS

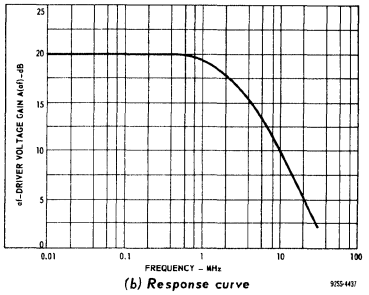
TERMINAL No.	I_{IN} mA	I_{OUT} mA
4	SUBSTRATE: CONNECT TO TERMINAL 3	
5	50	1
6	1	1
7	1	1
8	0.5	6
9	1	1
10	1	0.1
11	INT. CONN. DO NOT USE	
12	0.5	6
13	1	2
14	1	0.1
1	1	0.1
2	1	0.1
3	0.1	50

Note 1: Terminal No. 5 may be connected to any positive voltage through a suitable resistor provided that the current and dissipation ratings of the CA3065 are not exceeded.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if specified limits between all other terminals are not exceeded.



(a) Test circuit



(b) Response curve

Fig. 6 - Frequency response of af-amplifier section of CA3065

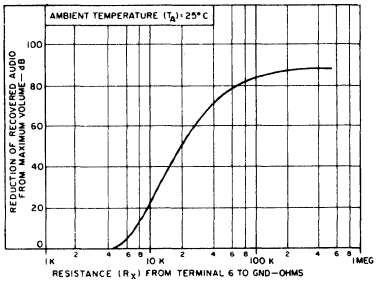


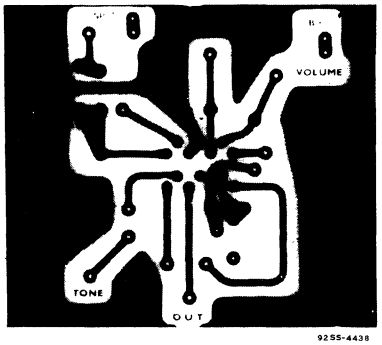
Fig. 7 - Gain reduction vs. resistance (terminal 6 to gnd)

OPERATING CONSIDERATIONS

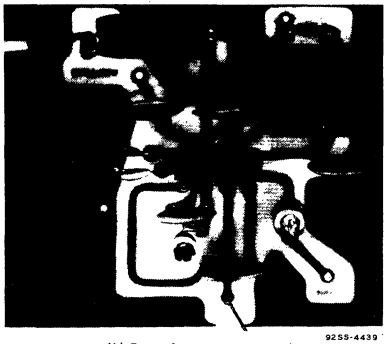
The CA3065 may be used to drive a video output transistor or a high-transconductance output tube.

As in all TV receivers, precaution should be taken to prevent destruction of the CA3065 in the event of cascade arcs originating in the picture tube or in the output tube. In the case of arcing in the output tube a resistor of 150 k in series with terminal No. 12 and the grid of the tube is usually sufficient protection.

To prevent damage from picture tube arcs, a careful analysis of board layout and coupling modes (electrostatic or magnetic) may be necessary to suggest alternate layouts or appropriate locations for the placement of spark gaps to absorb the high energy discharge.



*(a) Printed circuit board – bottom view**



*(b) Parts layout – top view**

Fig. 8 - Recommended parts layout for TV receiver sound strip using CA3065.

* A 200 mil square grid was used in the layout of passive components on the printed circuit board. The Quad-in-line formed leads conform to a standard grid spacing of 100 mil centers.

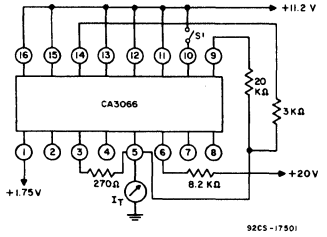


Fig. 2 - Static characteristics test circuit for CA3066.

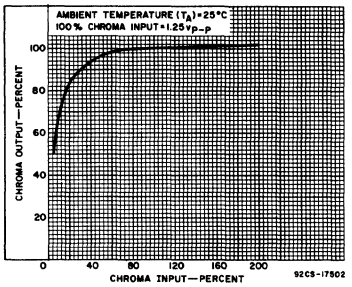


Fig. 3 - Typical ACC characteristic of chroma output vs chroma input for CA3066.

CA3067 CHROMA DEMODULATOR

The CA3067 contains the separate functional systems of a dc tint control and a demodulator. The phase shift of the tint amplifier system is accomplished by functional control of the fixed phase signal from the CA3066 oscillator output. This regenerated reference subcarrier is applied to terminal No. 3 and driven differentially into phase shift circuits. The tint adjustment controls the vector addition of phase shifted signals after which a limiting amplifier removes any remaining amplitude modulation. The output of the tint amplifier at terminal No. 1 is phase separated for the required reference subcarrier phase at terminal No. 6 and No. 12 (terminal No. 12 lags terminal No. 6 by approximately 76°). These terminals are inputs to the demodulator drive amplifiers. The demodulators consist of two sets of balanced detectors which receive their reference subcarrier from the demodulator drive amplifiers. The chroma signal input from the CA3066 is applied to terminal No. 14. The chroma signal differentially drives the demodulators. The demodulation components are matrixed and dc-shifted in voltage to give R−Y, G−Y, and B−Y color difference components with close dc balance and proper amplitude ratios. The output amplifiers of the CA3067 are specially designed to meet the low-impedance driving source requirements of the high-level color output amplifiers. A special feature of the CA3067 is R−C filtering of high frequency demodulation components. Terminal No. 4 is a zener diode for use as a regulated voltage reference at 11.9V. When the zener reference element is not used, the power supply should be maintained at +11.2 ±0.5 volts.

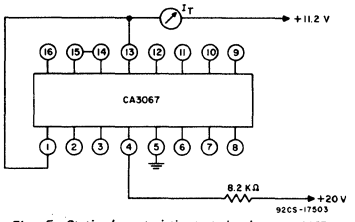


Fig. 5 - Static characteristics test circuit for CA3067.

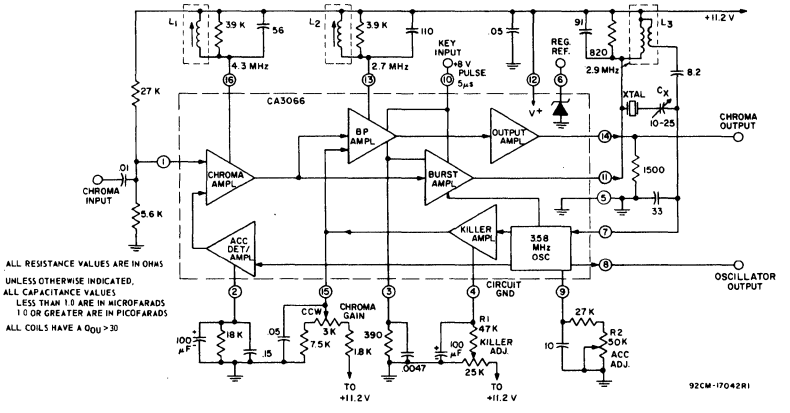


Fig. 4 - Dynamic characteristics test circuit for CA3066.

DYNAMIC CHARACTERISTICS TEST PROCEDURE

Steps 1, 2, and 3 are performed with no Chroma input (v_1 = 0)

1. Adjust ACC potentiometer for V_2 = +0.65V.
2. Adjust Killer potentiometer for V_4 = +1.2V.
3. Adjust capacitor C_x (crystal trimmer) so that frequency of oscillator is 3.579545 MHz.
4. Unless otherwise noted, the chroma gain control is at maximum gain (fully clockwise).
5. The chroma input test signal is a 52.5 μs "line" at subcarrier frequency, and 10 cycles of burst at 46.5% of the "line" amplitude. The chroma input (v_1) is in peak-to-peak volts of "line" amplitude.
6. The chroma output (v_{14}) is the same as the chroma input (v_1) except that the burst is removed and keying overshoot occurs in the retrace period. The chroma output is in peak-to-peak volts of "line" amplitude.
7. The oscillator output (v_8) is the CW output at terminal No. 8 and is in peak-to-peak volts. Some modulation of oscillation dampening between burst injection is visible.

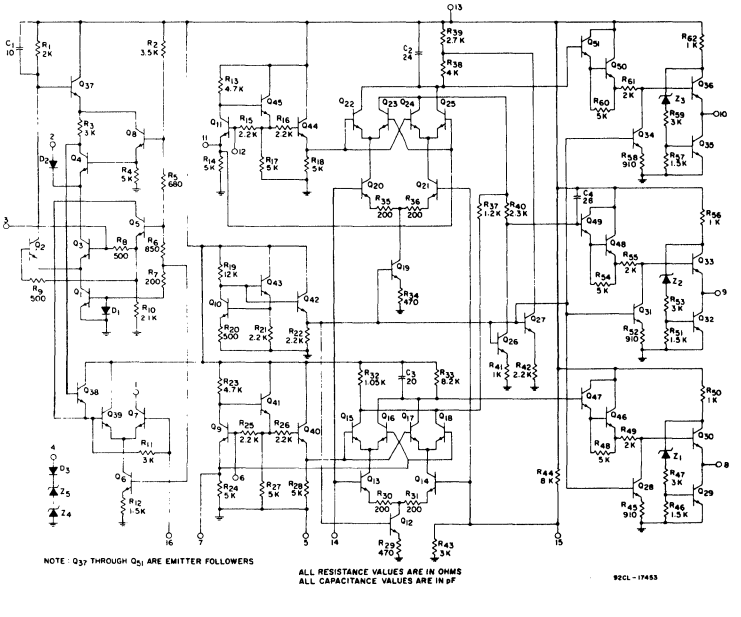


Fig. 6 - CA3067 schematic diagram.

Television Video IF System

RCA-CA3068 is a monolithic integrated circuit that incorporates an entire video TV-IF subsystem on a single chip. Innovations in integrated circuit design, in addition to the many active devices and closely matched components utilized in the circuit, make the CA3068 ideally suited for use in color and black-and-white TV receivers.

The primary functions performed by the IF subsystem are video IF amplification, linear detection, video output amplification, AGC from a keyed supply, AGC delay for tuner, sound carrier detection, sound carrier amplification, and a buffered AFT output. The advanced circuit design of the CA3068 also includes secondary functions for improved noise immunity and minimal airplane flutter. An isolated zener reference diode, incorporated in the IC, provides a convenient and economical means for controlling the regulated voltage supply. The inherent wide bandwidth capability (10-70 MHz) and high overall gain (87 dB) make the CA3068 suitable for other AM IF applications whose frequencies range within this bandwidth.

The CA3068 utilizes a unique 20-lead quad-in-line plastic package. This package also includes a wrap-around shield that serves to minimize interlead capacitances.

FEATURES:

- High-gain wide-band IF amplifier: 75 dB typ. at 45 MHz
- Gain reduction with excellent stability: 50 dB typ. at 45 MHz
- Video detector with linear characteristics
- Video amplifier: 12 dB gain
- Impulse noise limiter
- Keyed AGC with noise immunity circuits
- Delayed AGC for tuner
- Buffered AFT output
- Separate sound IF intercarrier amplification
- Sound carrier detector
- 4.5 MHz sound carrier amplifier
- Isolated zener reference diode for regulated voltage supply
- See ICAN-6303, "A Single IC for the Complete PIX-IF System in TV Receivers" for Schematic Diagram

MAXIMUM RATINGS, *Absolute Maximum Values, at $T_A = 25°C$*

DC Supply Voltage:		
Between Terminals 15 and 5*	11.3	V
Terminal 7 (Collector to ground)	20	V
Terminal 9 (Collector to ground)	20	V
DC Current (into Terminal 18)	2	mA
Device Dissipation:		
Up to $T_A = 60°C$	600	mW
Above $T_A = 60°C$	derate linearly 6.7 mW/°C	
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	− 65 to +150	°C
Lead Temperature (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

* This rating does not apply when using the internal zener reference in conjunction with the pass transistor.

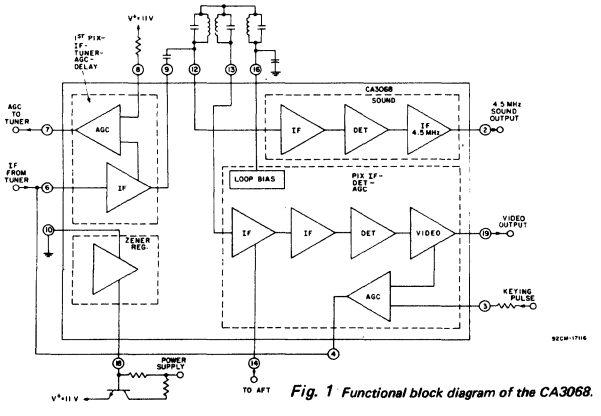


Fig. 1 Functional block diagram of the CA3068.

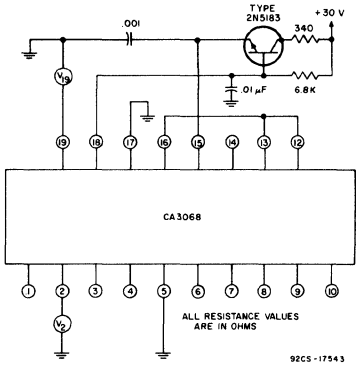
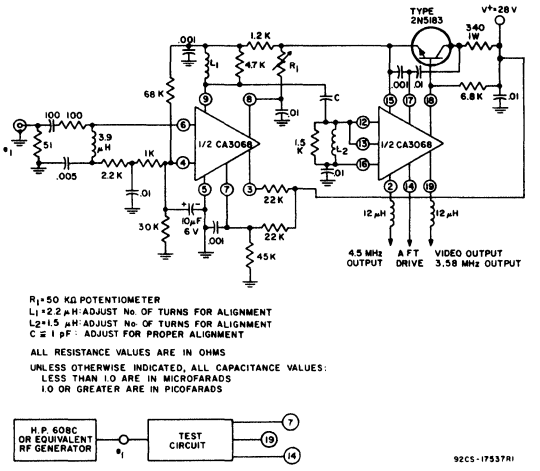
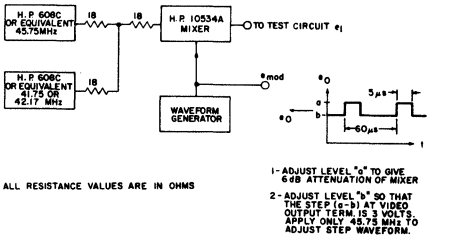


Fig. 2 – Test circuit for measurement of white level (V_{19}) and terminal 2 voltage (V_2).



(a) Test setup for measurement of video sensitivity, sync. tip level, delay bias, AFT drive voltage.



(b) Test setup for measurement of sound and chroma outputs.

Fig. 3 – Typical dynamic test circuit diagrams.

Television Chroma System

The RCA CA3070, CA3071, and CA3072 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3070 is a complete subcarrier regeneration system featuring a new concept of phase control applied to the oscillator circuit. The CA3071 is a chroma amplifier system and the CA3072 performs the demodulation function.

The CA3070 utilizes the 16-lead plastic dual-in-line package; the CA3071 and CA3072 are supplied 14-lead plastic dual-in-line packages.

SYSTEM FEATURES

CA3070

- Voltage Controlled Oscillator
- Keyed APC & ACC Detectors
- DC Hue Control
- Shunt Regulator

CA3071

- ACC Controlled Chroma Amplifier
- DC Chroma Gain Control
- Color Killer
- Amplifier Short-Circuit Protection

CA3072

- Synchronous Detector with Color Difference Matrix
- Emitter-Follower Output Amplifiers with Short-Circuit Protection

CA3070
Chroma Signal Processor

The CA3070 is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3071 is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval.

The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 14 of the CA3071. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator.

To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3070 includes a shunt regulator to establish a 12-volt dc supply.

Maximum Voltage and Current Ratings at T_A = +25°C

Terminal No.	Voltage▲ Min. Volts	Voltage▲ Max. Volts	Terminal No.	Current I_I mA	Current I_O mA
1	0	*	1	20	1
2	0	+16	2	–	–
3	0	+16	3	–	–
4	–5	N2	4	20	1
6	–	–	10	N3	1
7	–	–	11	–	–
8	–	–	12	–	–
10	0	N3	13	20	1
11	0	N1	14	20	1
12	0	N1			
13	0	N1			
14	0	N1			
15	0	+16			
16	0	+16			

▲ With respect to terminal No.5 and with terminal No. 10 connected through 470Ω to +24 V.

N1 Regulated voltage at terminal No. 10.

N2 Controlled by max. input current.

N3 Limited by dissipation.

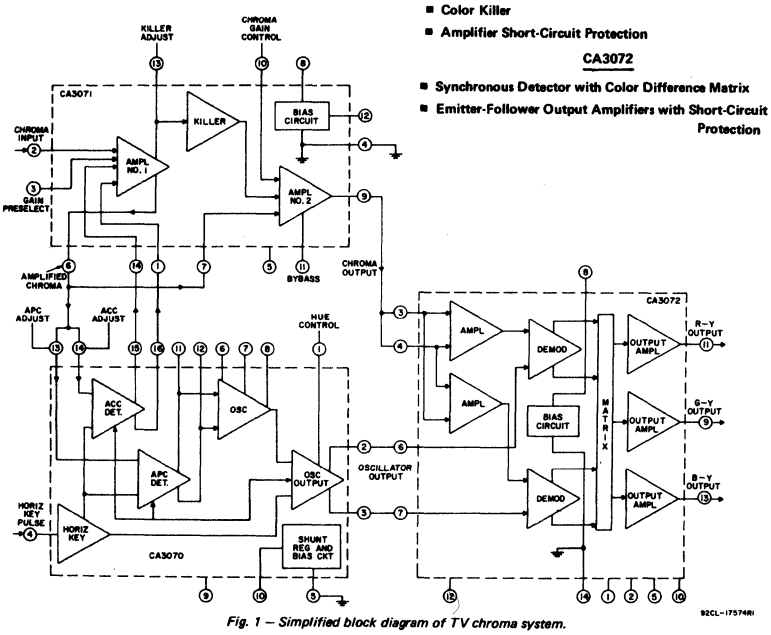


Fig. 1 – Simplified block diagram of TV chroma system.

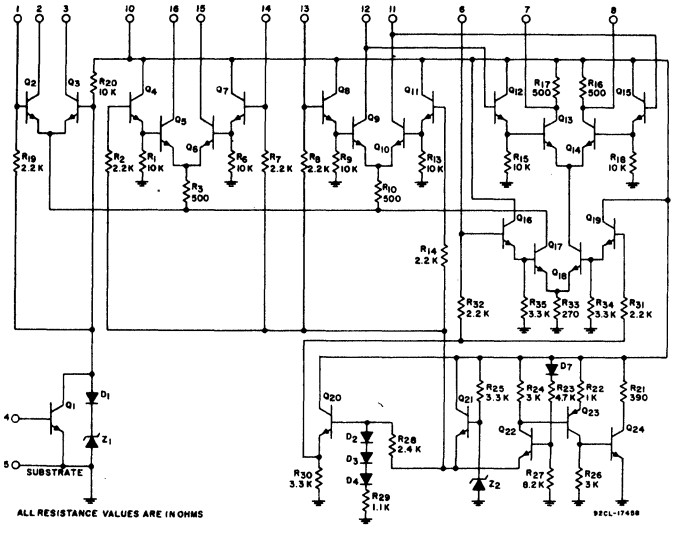


Fig. 2 – Schematic diagram CA3070.

CA3071 Chroma Amplifier

The CA3071 is a combined two-stage chroma amplifier and functional control circuit. The input signal is received from the video amplifier and applied to terminal No. 2 of the input amplifier stage. The first amplifier stage is part of the ACC system and is controlled by differential adjustment from the ACC input terminal Nos. 1 and 14. The output of the 1st amplifier is directed to terminal No. 6 from where the signal may be applied to the ACC detection system of the CA3070 or an equivalent circuit. The output at terminal No. 6 is also applied to terminal No. 7 which is the input to the 2nd amplifier stage. Another output of the 1st amplifier at terminal No. 13 is directed to the killer adjustment circuit.

The dc voltage level at terminal No. 13 rises as the ACC differential voltage decreases with a reduction in the burst amplitude. At a pre-set condition determined by the killer adjustment resistor the killer circuit is activated and causes the 2nd chroma amplifier stage to be cut off. The 2nd chroma amplifier stage is also gain controlled by the adjustment of dc voltage at terminal No. 10. The output of the 2nd chroma amplifier stage is available at terminal No. 9. The typical output termination circuit that is shown, provides differential chroma drive signal to the demodulator circuit. Both amplifier outputs utilize emitter-followers with short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at $T_A = 25°C$*

DC Supply Voltage (Terminal 8 to Terminal 4)	30	VDC
Device Dissipation:		
Up to $T_A = +70°C$	530	mW
Above $T_A = +70°C$	Derate Linearly at 6.7	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/32 in (3.17 mm) from seating plane for 10 s max.	+265	°C

Maximum Voltage and Current Ratings @ $T_A = +25°C$

Current			Voltage*		
Terminal No.	I_I mA	I_O mA	Terminal No.	MIN VOLTS	MAX VOLTS
1	5	1.0	1	−5	+15
2	5	1.0	2	−5	+5
3	10	10	3	0	+2
6	1.0	20	6	0	+24
7	5	1.0	7	−5	+5
9	1.0	20	8	0	+30
12	1.0	5	9	0	+24
14	5	1.0	10	0	+24
			11	0	+24
			12	0	+20
			13	0	+20
			14	−5	+15

* With reference to terminal No. 4 and with +24 V on terminal No. 8 except for the rating given for terminal No. 8.

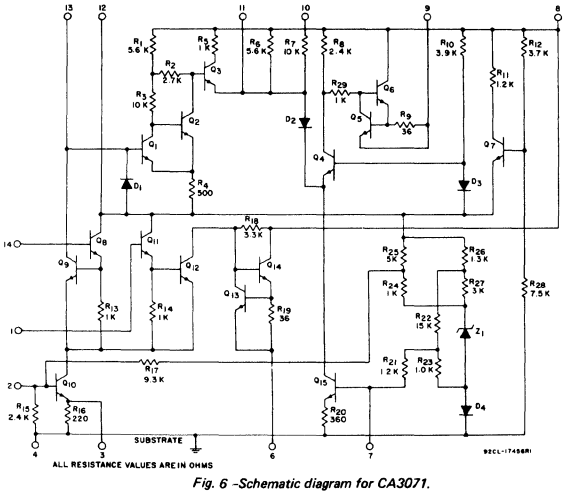


Fig. 6 -Schematic diagram for CA3071.

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

CHARACTERISTICS	SYMBOLS (Measure)	SPECIAL TEST CONDITIONS	LIMITS CA3071 MIN.	LIMITS CA3071 TYP.	LIMITS CA3071 MAX.	UNITS	CURVES & TEST CIRCUITS FIG.
Static Characteristics							
Voltages							
Bias Reference Terminal	V_{12}	S_1 Open, S_2 Open	-	17.3	-	V	7
Ampl. No. 1 Chroma Input	V_2	S_1 Open, S_2 Open	-	1.75	-		
Ampl. No. 1 Chroma Output Balanced	V_6	S_1 Open, S_2 Open	-	20	-		
Unbalanced	V_6	S_1 Open, S_2 Closed	-	13.5	-		
Ampl. No. 2 Chroma Input	V_7	S_1 Open, S_2 Open	-	1.5	-		
Ampl. No. 2 Chroma Output	V_9	S_1 Closed, S_2 Open	-	20.6	-		
Supply Current	I_T	S_1 Open, S_2 Open	17	24.5	31	mA	
Dynamic Characteristics							
Amplifier No. 1 Voltage Gain	A_{V1}	E_g 30 mV_{RMS} Measure v_6	14	-	-	dB	8
Amplifier No. 2 Voltage Gain	A_{V2}	V_g 1.0 V (RMS) Measure v_7	-	14	-	dB	
Max. Chroma Output Voltage	v_9		-	2	-	V_{RMS}	11
10% Chroma Gain Control Reference Voltage	V_8-V_{10}	E_g - 50 mV_{RMS}, adjust Chroma Gain Control to Change v_9 to 10% of Maximum Chroma Output	2.1	3.8	6.8	V	8
Output Voltage, Killer Off	v_9	S_1 in Position 2 E_g - 50 mV_{RMS}, adjust "Killer Adjust" for an abrupt decrease in V_9		-	12	mV RMS	
Output Voltage, Chroma Off	v_9	E_g - 50 m V_{RMS}, adjust Chroma control to min. Chroma Output	-	-	12	mV RMS	
Bandwidth: Amplifier No. 1	BW		-	12	-	MHz	9, 10
Amplifier No. 2			-	30	-		
Ampl. No. 1 Input Impedance	r_{i1}		-	2	-	kΩ	8
	c_{i1}		-	4	-	pF	
Ampl. No. 1 Output Impedance	r_{o1}		-	85	-	Ω	
Ampl. No. 2 Input Impedance	r_{i2}		-	2.1	-	kΩ	
	c_{i2}		-	3.5	-	pF	
Ampl. No. 2 Output Impedance	r_{o2}		-	85	-	Ω	

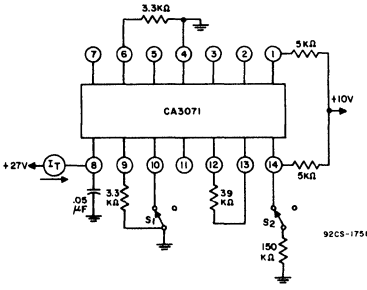


Fig. 7 - Static characteristics test circuit—CA3071.

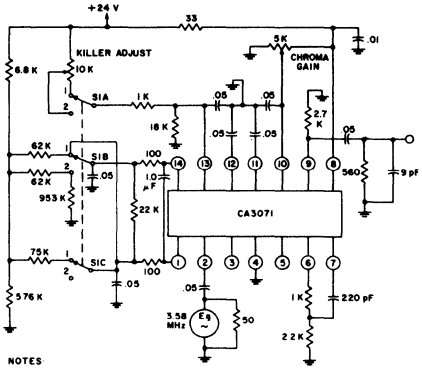


Fig. 8 - Dynamic characteristics circuit-CA3071.

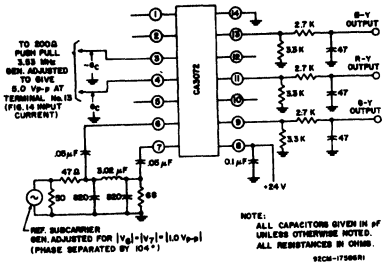


Fig. 14 - Dynamic characteristics test circuit for CA3072.

Application Information

TYPICAL APPLICATION CIRCUIT FOR THE CHROMA SYSTEM

The circuit of *Fig.15* is a complete signal processing system for color TV. The RCA types CA3070, CA3071 and CA3072 monolithic integrated circuits are respectively used as the subcarrier regenerator, chroma amplifier, and chroma demodulator.

The input to the system is the chroma signal which may be taken from the first or second video stage and is coupled into the CA3071 chroma amplifier through a bandpass filter. The outputs from the system are the color difference signals which are intended to drive high level amplifiers. Luminance mixing may be external to the picture tube or, the difference signals may be amplified and applied to the picture tube grid or cathode, where they are internally mixed with the luminance signal.

Other input requirements to the system are the power supply voltage of +24 volts and the horizontal keying pulse. The power supply voltage should be maintained within ±3 volts of the recommended value of +24 volts. The total current for the system is approximately 70 milliamperes. The horizontal keying pulse input to the subcarrier regenerator is approximately +4 volts peak and centered on the burst as seen at terminal Nos. 13 and 14 of the CA3070. The pulse width should be maintained as close as possible to the recommended value of 4.5 microseconds.

CA3070 Circuit Operation

The CA3070 circuit as shown in Fig. 2, consists of an oscillator, automatic phase control (APC) detector, automatic chroma control (ACC) detector, gated oscillator output amplifier and a shunt regulator. The shunt regulator provides the necessary bias stability for the 3.579545 MHz oscillator, as well as the bias to all functions of the CA3070 circuit. The regulation voltage is nominally +12 volts as measured at terminal No. 10.

The APC and ACC detectors are synchronous detectors which are keyed by the horizontal input pulse. This form of detection eliminates the need for a burst separator as an individual amplifier stage. When a positive pulse is present at terminal No. 4, the oscillator output is cutoff and the oscillator drive signal is diverted to the APC and ACC detectors. Referring to Fig. 2, the APC detector (Q_9 & Q_{10}) and the ACC detector (Q_5 & Q_6) are emitter driven from the

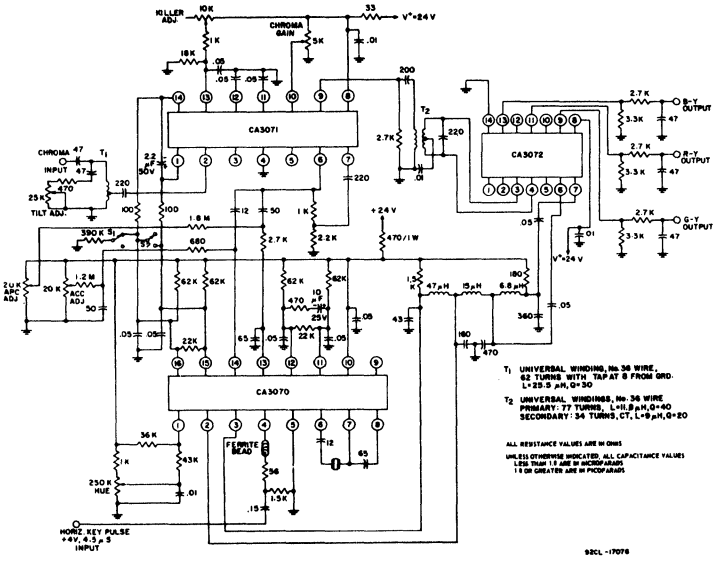


Fig. 15 – Typical chroma system for color-TV receivers utilizing RCA-CA3070, CA3071, and CA3072.

oscillator transistor (Q_{17}), when the oscillator output amplifier transistors (Q_2 & Q_3) are cutoff. The chroma signal is applied to terminal Nos. 13 and 14. There is oscillator current drive to the APC and ACC detectors during the keying interval; burst separation is effectively accomplished by the gating action of the detectors. A further advantage of the keying action is the high gain made possible as a result of the low average current flow of the APC and ACC detectors. High resistor values of 62 kilohms at the detector output terminals provide proper detector bias consistent with the duty factor of the keying pulse. For a wider keying pulse, it is necessary that smaller values of detector load resistors be used.

In the absence of the keying pulse (line period), the resistor, R_{20}, biases the oscillator's output amplifier transistors (Q_2 & Q_3) on by keeping their emitters at a higher potential than the base bias voltages of Q_5, Q_6, Q_9, and Q_{10}. The 3.58 MHz signal is now present at terminal Nos. 2 & 3. Photographs of oscilloscope traces for one line period at the terminal Nos. 1, 2, and 3 are shown in Fig.16. The effect of the keying pulse is shown in Fig.16a, and the cutoff of the oscillator output amplifier is shown in Fig.16(b) and 16c.

The oscillator section of the CA3070 consists of the loop formed by Q_{18} and the emitter driven differential pair, Q_{13} & Q_{14}. The signal output from terminal Nos. 7 & 8 is coupled through the series tuned crystal circuit back through terminal No. 6 to Q_{16} & Q_{17}. The collector of Q_{17} drives the oscillator output amplifier and the APC & ACC detectors. Q_{17} is emitter coupled to transistor Q_{18}. The oscillator frequency and phase control is accomplished by the differential drive from the APC detector to transistors Q_{12} & Q_{15} which control the balance of Q_{13} & Q_{14}. The resulting phase of the feedback loop is determined by the relative amplitudes of the oscillator output signal at terminal Nos. 7 and 8. The 65 pF capacitor between terminal No. 7 and 8 provides the phase shifting component as the balance of Q_{13} and Q_{14} is varied. In this way the APC detector controls the crystal frequency at which the phase shift is cancelled in the feedback loop.

The controls for the CA3070 subcarrier regenerator circuit are the APC balance, the ACC balance, and the hue control. The hue control is a dc balance adjustment of the oscillator output amplifier transistors Q_2 & Q_3. A phase delay network between the output terminals Nos. 2 & 3 determines the range of the hue control, which for the value shown in Fig. 15, is approximately 90°.

The ACC adjustment sets the initial balance of the ACC drive to the input of the CA3071 in Fig. 15 (terminal Nos. 1 and 14 of the CA3071). The APC is a frequency adjustment of the oscillator through the balance control of the APC detector.

As a setup adjustment, for both the ACC and APC, switch S1 is opened and S2 is closed. The chroma input to the system is removed and the dc voltage at terminal No. 6 of the CA3071 is noted. The switch S2 is then opened and the ACC adjusted to set the voltage at terminal No. 6 to that previously noted. Alternatively, the differential dc voltage at terminal Nos. 15 & 16 of the CA3070 may be set to 0 mV (±2 mV) when S1 and S2 are open, and the CA3071 is removed from the circuit.

Fig. 16(a) - CA3070 terminal No. 1 7.5 V oscillator "gate off" pulse.

Fig. 16(b) - CA3070 terminal No. 2, 3.5 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

Fig. 16(c) - CA3070 terminal No. 3, 2.0 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

Fig. 21(a) - CA3072 - terminal No. 3 or 4, chroma input signal, 220 mV_{p-p}, one horizontal line

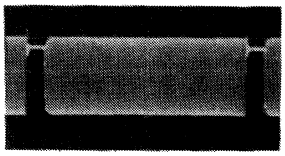


Fig. 21(b) - CA3072 - terminal No. 6 or 7, reference subcarrier 1.2 V_{p-p}, one horizontal line

Fig. 21(c) - CA3072 terminal No. 13, 4.8 v_{p-p} B-Y output, one horizontal line

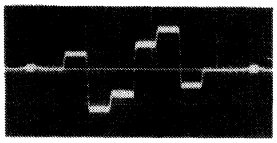


Fig. 21(d) - CA3072 - terminal No. 11, 5.2 v_{p-p} R-Y output, one horizontal line

Fig. 21(e) - CA3072 - terminal No. 9, 1.2 v_{p-p} G-Y output, one horizontal line

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS T_A = 25°C, V+ = 12 V	TEST CIRCUIT FIG. NO.	TYPICAL VALUES	UNITS
Static (DC) Characteristics					
DC Voltages:					
Terms. 1, 4, 9, 11	$V_{1,4,9,11}$		1	0.7	V
Terms. 2, 7, 8	$V_{2,7,8}$			1.4	V
Term. 10	V_{10}			5.6	V
Term. 12	V_{12}			0	V
Term. 15	V_{15}			3.5	V
DC Current:					
Term. 3	I_3		1	0.35	mA
Term. 6	I_6			1.0	mA
Term. 10	I_{10}			20	mA
Term. 13	I_{13}			0	mA
Term. 16	I_{16}			1.2	mA
Dynamic Characteristics					
Detector Output		30% Modulation	4	75	mV RMS
Audio Amplifier Gain	A_{AF}	f = 1 kHz	4	30	dB
Audio Distortion		V_{OUT} = 100 mV	4	0.2	%
Sensitivity:		f_{IN} = 1 MHz			
At Converter Stage Input		Signal-to-Noise Ratio (S/N) = 20 dB	2	200	μV/m
At RF Stage Input			4	100	μV/m
Total Harmonic Distortion	THD	30% Modulation	4	1.0	%
Input Resistance:	R_I				
At Transistor Q1				3500	Ω
At Transistor Q5		No AGC,		2000	Ω
Input Capacitance:	C_I				
At Transistor Q1		Input signal frequency		12	pF
At Transistor Q5		(f_{IN}) = 1 MHz		17	pF
Feedback Capacitance:	C_{FB}				
At Transistor Q1				1.5	pF
At Transistor Q5				1.5	pF

The typical characteristics for the CA3088E are intended for guidance purposes in evaluating this device for equipment design.

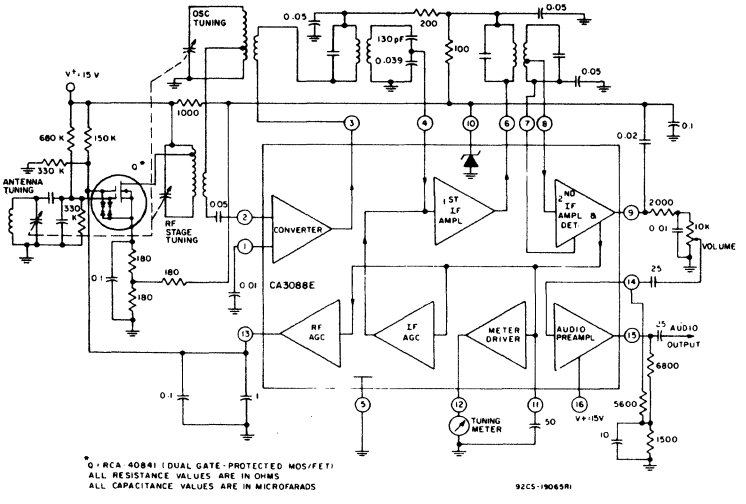
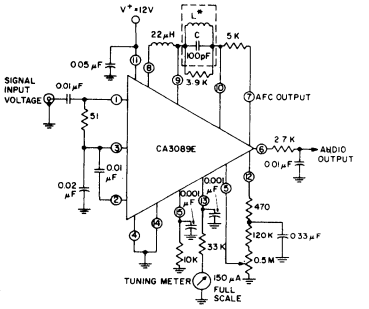


Fig.4—Typical AM broadcast receiver using the CA3088E with optional RF amplifier stage.

MAXIMUM RATINGS, *Absolute Maximum Values, at $T_A = 25^oC$*

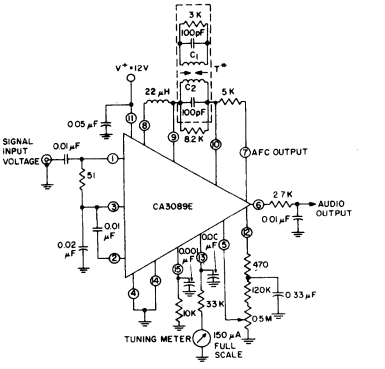
DC Supply Voltage:		
Between Terminals 11 and 4	16	V
Between Terminals 11 and 14	16	V
DC Current (out of Terminal 15)	2	mA
Device Dissipation:		
Up to $T_A = 60^oC$	600	mW
Above $T_A = 60^oC$	derate linearly 6.7 mW/^oC	
Ambient Temperature Range:		
Operating	−55 to +125	^oC
Storage	-65 to +150	^oC
Lead Temperature (During Soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.	+265	^oC



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_0(UNLOADED) ≅ 75 (G I AUTOMATIC MFG DIV. EX22741 OR EQUIVALENT)

92CM-19040R

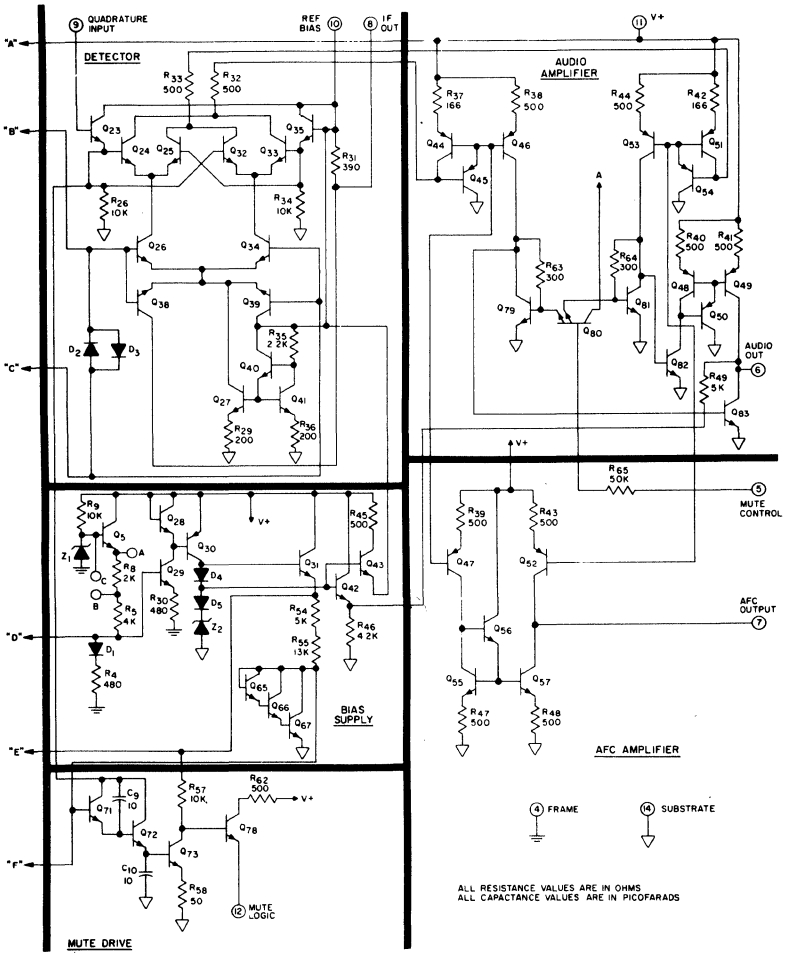
Fig.3-Test circuit for CA3089E using a single-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS
*T: PRI. − Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20 T OF 34ø ON 7/32" DIA FORM
SEC − Q_0(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20 T OF 34ø ON 7/32" DIA FORM
kQ (PER CENT OF CRITICAL COUPLING) ≅ 70 %
(ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4 mm

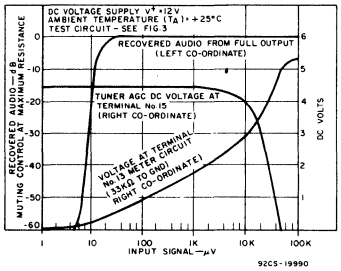
92CM-19041R1

Fig.4-Test circuit for CA3089E using a double-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS
ALL CAPACTANCE VALUES ARE IN PICOFARADS

Fig.2-Schematic diagram of the CA3089E.



92CS-19990

Fig.5-Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

Stereo Multiplex Decoder

For FM Stereo Multiplex Systems

RCA-CA3090AQ , a monolithic silicon integrated circuit, is a stereo multiplex decoder intended for FM multiplex systems.

The CA3090AQ is the successor to the CA3090Q; it offers three major advantages over the CA3090Q as follows:

1. Can directly drive a stereo indicator lamp with a current drain of up to 100 mA.
2. Stereo Defeat/Enable control-voltage specifications.
3. Capable of operation with lower distortion.

This stereo multiplex decoder requires only one low-inductance tuning coil (requires only one adjustment for complete alignment), provides automatic stereo switching, energizes a stereo indicator lamp, and operates from a wide range of voltage supplies.

Figure 1 shows the block diagram for the CA3090AQ. The input signal from the detector is amplified by a low-distortion preamplifier and simultaneously applied to both the 19-kHz and 38-kHz synchronous detectors. A 76-kHz signal, generated by a local voltage-controlled oscillator (VCO), is counted down by two frequency dividers to a 38-kHz signal and to two 19-kHz signals in phase quadrature.

The 19-kHz pilot-tone supplied by the FM detector is compared to the locally generated 19-kHz signal in a synchronous detector. The resultant signal controls the voltage controlled oscillator (VCO) so that it produces an output signal to phase-lock the stereo decoder with the pilot tone. A second synchronous detector compares the locally generated 19-kHz signal with the 19-kHz pilot tone. If the pilot tone exceeds an externally adjustable threshold voltage, a Schmitt trigger circuit is energized. The signal from the Schmitt trigger lights the stereo indicator, enables the 38-kHz synchronous detector, and automatically switches the CA3090AQ from monaural to stereo operation. The output signal from the 38-kHz detector and the composite signal from the preamplifier are applied to a matrixing circuit from which emerge the resultant left and right channel audio signals. These signals are applied to their respective left and right post amplifiers for amplification to a level sufficient to drive most audio amplifiers.

The CA3090AQ may be used without the stereo defeat/enable function (see Fig. 6) if a control voltage for this function is not readily available. In this case, Terminal 4 should be grounded.

The CA3090AQ utilizes the 16-lead quad-in-line plastic package and operates over the ambient temperature range of −55°C to +125°C.

Features:

- **Requires the use of only one low-inductance tuning coil**
- **Automatic stereo switching**
- **Directly drives a stereo indicator lamp up to 100 mA**
- **Includes driver for stereo-lamp indicator**
- **Operates from a wide range of power supplies: 10 to 16 volts**
- **Requires only one adjustment for alignment**
- **Switching from monaural to stereo and stereo to monaural produces no audible thumps**
- **Low distortion: under 0.22% (typ.)**
- **Separate dc input permits stereo defeat or enable**
- **High signal output: directly drives audio amplifiers**
- **Excellent SCA (storecast) rejection: 55 dB typ.**
- **High audio channel separation: 40 dB typ.**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC SUPPLY VOLTAGE	16 V
CURRENT AT TERM. 12	100 mA
INPUT SIGNAL VOLTAGE (COMPOSITE)■	400 mV
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265°C

■ For stereo operation, a minimum input signal voltage (composite) of 40 mV is required.

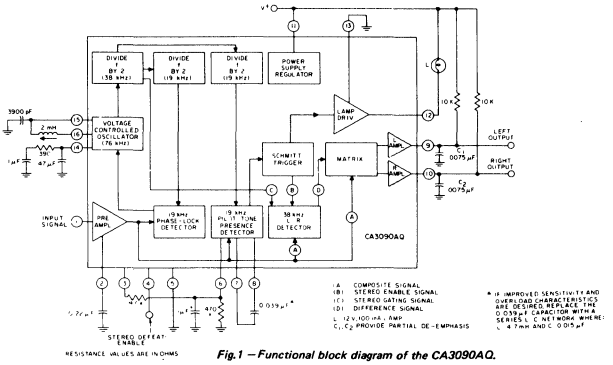


Fig. 1 – Functional block diagram of the CA3090AQ.

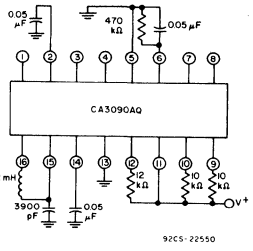


Fig. 2 – Test circuit for DC characteristics.

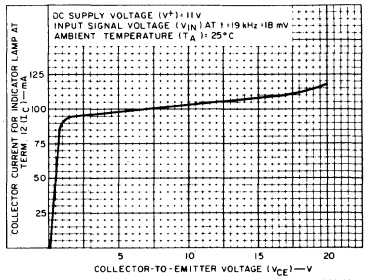


Fig. 3 – Indicator lamp characteristics (I_C vs. V_{CE}).

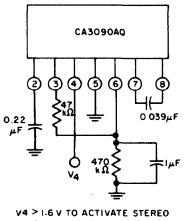


Fig. 4 – Test circuit for use with stereo defeat/enable.

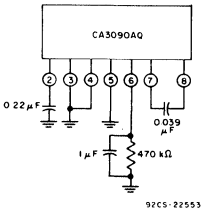


Fig. 5 – Test circuit for use without stereo defeat/enable.

TV Signal Processors ("Jungle" Circuits)

For Color and Monochrome Receivers

The RCA-CA3120E and CA3142E are monolithic silicon integrated circuit TV signal processors for use in color or monochrome receivers. These circuits provide low-impedance video output signals, stripped synchronization signals in both polarities, and AGC output signals for IF (reverse) and tuner (forward and/or reverse).

The circuit designs of the CA3120E and CA3142E feature impulse noise inversion, delay techniques to reduce the deleterious effects of impulse noise in the receiver AGC and sync circuits. In addition, they incorporate standard AGC strobing techniques. The AGC noise lockout circuit is deleted in the CA3142E.

These devices are supplied in the 16-lead dual-in-line plastic package.

Features:

- **Internal impulse noise processing**
- **Sync separator — low impedance, dual polarity**
- **Strobed AGC system** ■ **IF AGC output**
- **Delayed outputs for forward or reverse AGC tuners**
- **Automatic noise threshold and AGC detector level control**
- **High-impedance video input**
- **Low-impedance video output**
- **Choice of external time constants for sync separator**
- **Negative power supply not required**
- **RF AGC delay externally controlled**

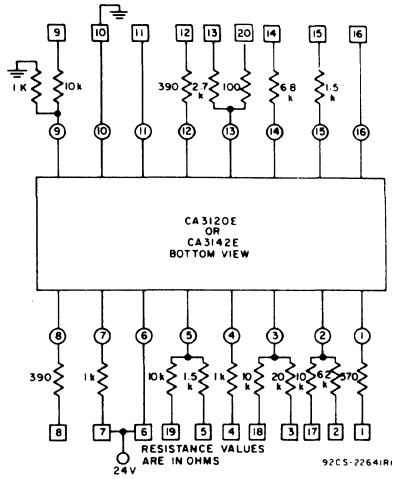


Fig. 2 — Test circuit for measuring electrical characteristics of the CA3120E and CA3142E. Refer to Figs. 7 and 8 for switch selector positions.

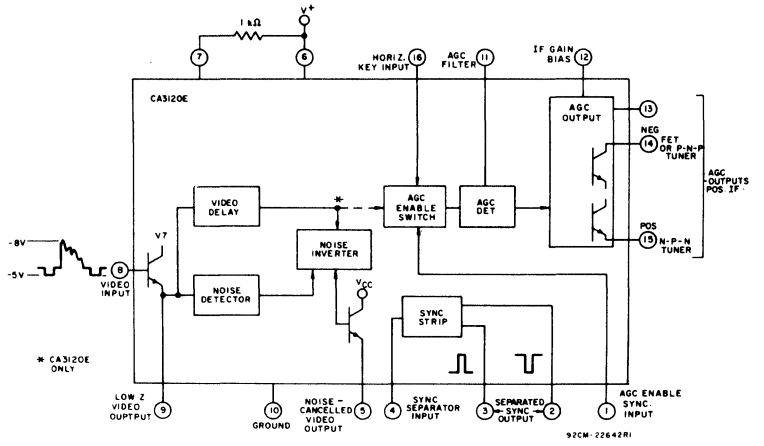


Fig. 1 — Simplified block diagram of the CA3120E and CA3142E.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

DC SUPPLY VOLTAGE	30 V
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C. . . . . Derate linearly at 7.9	mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85 °C
Storage	−65 to +150 °C
LEAD TEMPERATURE (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265 °C

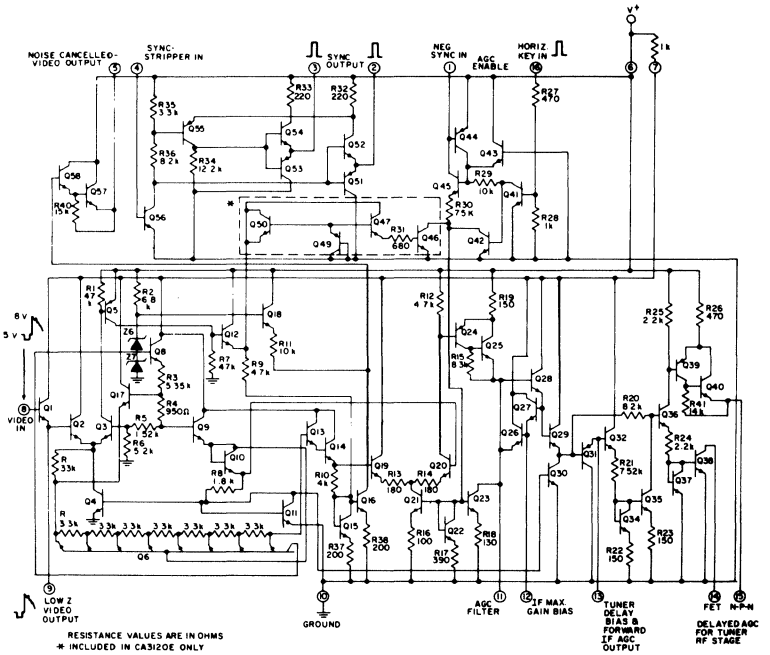


Fig. 3 — Schematic diagram of the CA3120E and CA3142E.

CHARACTERISTIC	TEST CONDITIONS — SWITCH NUMBERS — SWITCH POSITION																	TERMINAL MEASURED
	1	*2*	*3*	*4*	*5*	*8*	*9*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*19*	*20*	
I_{T24}	2	3	1	2	1	2	3	1	1	3	2	1	2	2	2	1	5	*2 6 7 9 14*
V_{TH}	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	1	3	*8*
V_5	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	2	3	*19*
$V_{TH(SEP)}$	3	1	2	1	1	*	3	3	4	1	1	2	1	2	2	2	1	*
$I_{4(OFF)}$	3	1	2	4	2	1	1	1	1	1	1	2	1	2	2	1	1	I_4
V_{2L}	1	2	2	3	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{2H}	3	3	1	1	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{3L}	3	3	1	1	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
V_{3H}	3	3	1	3	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
$I_{11(CH)}$	2	1	2	5	2	1	1	5	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(DISCH)}$	2	1	2	5	1	2	3	6	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(LEAK)}$	2	1	2	5	2	1	1	6	4	3	2	2	1	2	2	1	5	I_{11}
V_{11}	2	1	2	5	1	2	3	2	3	3	1	2	2	2	2	1	5	V_{11}
V_{12}	3	1	2	5	2	1	1	3	4	3	1	2	1	2	2	1	5	V_{12}
$V_{13(LOW)}$	3	1	2	5	2	2	3	1	1	2	1	2	1	2	2	1	2	V_{13}
$V_{13(HIGH)}$	3	1	2	5	2	2	3	7	4	3	2	1	1	2	2	1	4	V_{20}
$I_{14(OFF)}$	3	1	2	5	2	2	3	3	4	3	3	1	1	2	2	1	5	I_{14}
$I_{14(ON)}$	3	1	2	5	2	2	3	8	4	3	3	1	1	2	2	1	5	I_{14}
$I_{15(OFF)}$	3	1	2	5	2	2	3	3	4	3	2	3	1	2	2	1	5	I_{15}
$I_{15(ON)}$	3	1	2	5	2	2	3	8	4	3	2	3	1	2	2	1	5	I_{15}

CAUTION: Remove power before selecting or adjusting switches.

* Reduce voltage at Terminal 8 until V_{19} decreases. $V_{TH(SEP)} = V_{TH} - V_8$.

NOTE: Switch numbers in italics correspond to numbers in square boxes in Figs. 2 and 8.

Fig.7 – Test condition values for associated switches 1 through 20 (switches 6, 7, and 10 are omitted). Refer to Figs. 2 and 8 for test circuit and test-condition selector-switch arrangements.

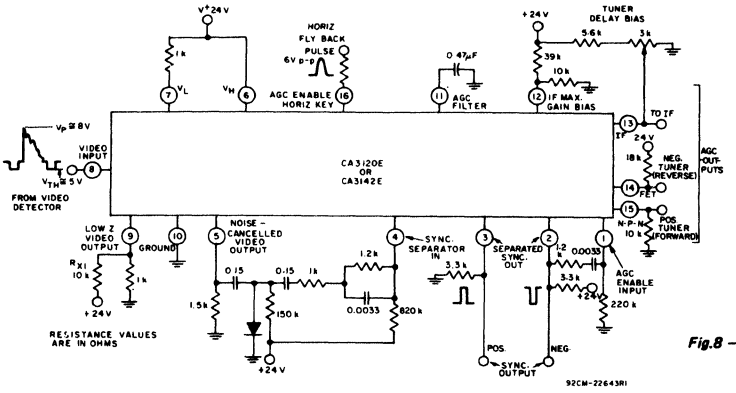
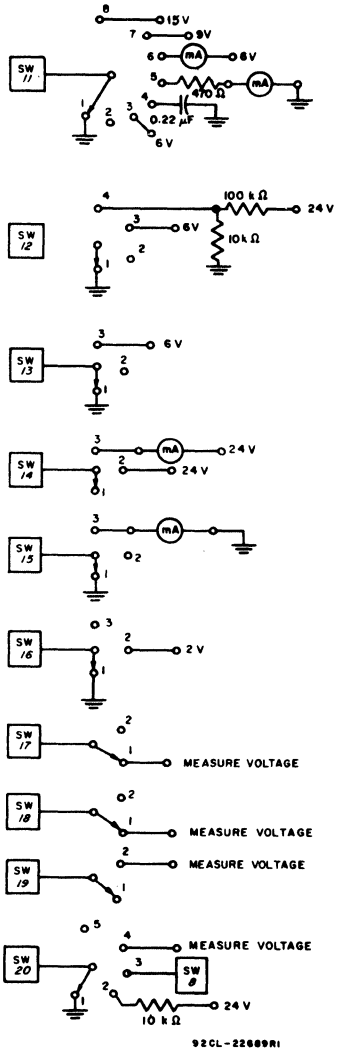


Fig.9 – Typical application using the CA3120E and CA3142E.



NOTE: The italicized numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 2 and 7.

CAUTION: Remove power before selecting or adjusting switches

Fig.8 – Test condition selector switch arrangement for measuring the electrical characteristics of the CA3120E and CA3142E.

(Figure 8 continued on the next page)

TV Chroma Amplifier/ Demodulator

Provides Complete System for Processing Chroma When Used with RCA-CA3070 or CA3170 "G" Suffix Type-Hermetic Gold-CHIP in Dual-in-Line Plastic Package

Features:

- **Excellent linearity in dc chroma gain-control circuit**
- **Improved filtering resulting in reduced 7.2 MHz output from the color demodulators**
- **Current limiting for short-circuit protection**
- **Good tolerance to B+ supply variations**
- **Good temperature coefficient stability**
- **Gold-CHIP for increased reliability**

RCA-CA3121G is a monolithic silicon integrated circuit chroma amplifier/demodulator with ACC and killer control for color-TV receivers. It is designed to function compatibly with the CA3070 or CA3170 in a two-package chroma system. Figs. 5 and 6 show a functional block diagram and the outboard circuitry of a typical two-package chroma system incorporating the CA3121G and CA3170, respectively.

The CA3121G is supplied in a 16-lead dual-in-line plastic package with hermetic Gold-CHIP (G suffix).

The transistor chips used in the hermetic Gold-CHIP plastic packages are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminents without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multilayered, highly corrosion-resistant, terminal-connection system of unique design is employed.

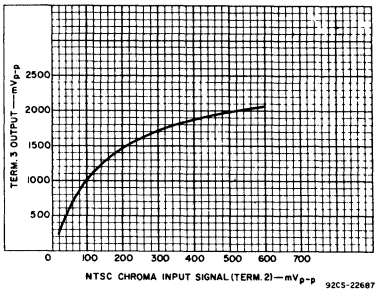


Fig. 2 – Typical ACC plot for the CA3121G when used with the CA3070.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Supply Voltage	30 V
Device Dissipation:	
Up to T_A = 15°C	1 W
Above T_A = 55°C	derate linearly 10.5 mW/°C
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (During Soldering)	
At distance 1/16" ±1/32" (1.59 ±0.79 mm) from case for 10 s max.	+265°C

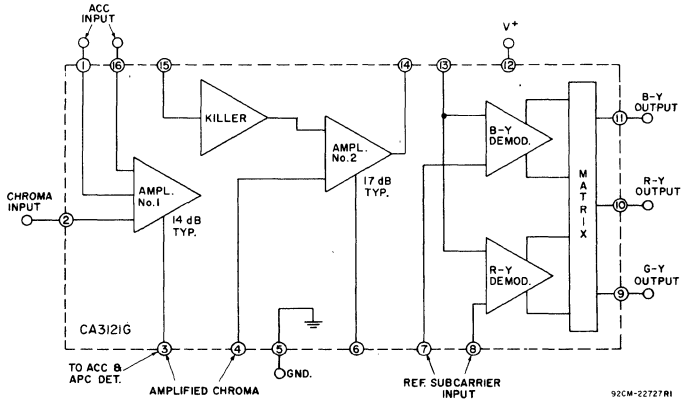


Fig. 1 – Functional block diagram of the CA3121G.

CIRCUIT OPERATION

The CA3121G consists of three basic circuit sections: (1) amplifier No.1, (2) amplifier No.2, and (3) demodulator. Amplifier No.1 contains the circuitry for automatic chroma control (ACC) and color-killer sensing. The output of amplifier No.1 (Terminal 3) is coupled to the Chroma Signal Processor (CA3070, CA3170 or equivalent) for ACC and automatic phase control (APC) operation and to the input of amplifier No.2 (Terminal 4) containing the chroma gain control circuitry. The signal from the color-killer circuit in amplifier No.1 acts upon amplifier No.2 to greatly reduce its gain.

The output from amplifier No.2 (Terminal 14) is applied, through a filtering network, to the demodulator input (Terminal 13).

The demodulator also receives the R-Y and B-Y demodulation subcarrier signals (Terminals 7 and 8) from the oscillator output of the Chroma Signal Processor. The R-Y and B-Y demodulators and the matrix network contained in the demodulator section of the CA3121G reconstruct the G-Y signal to achieve the R-Y, G-Y, and B-Y color difference signals. These high-level outputs signals with low impedance outputs are suitable for driving high-level R, G, and B output amplifiers. Internal capacitors are included on each output to filter out unwanted harmonics. For additional operating information and signal waveforms, refer to Television Chroma System (utilizing RCA-CA3070, CA3071, CA3072), File No. 468.

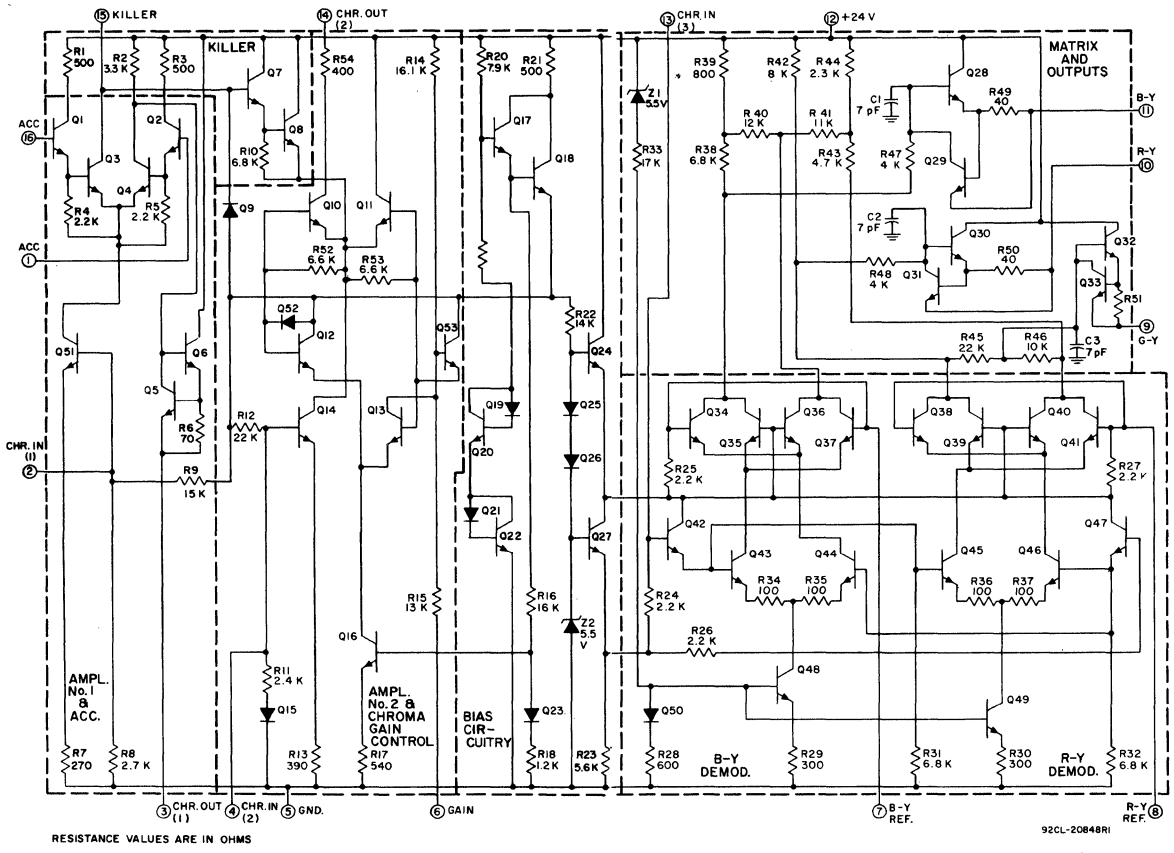


Fig. 4 – Schematic diagram of the CA3121G .

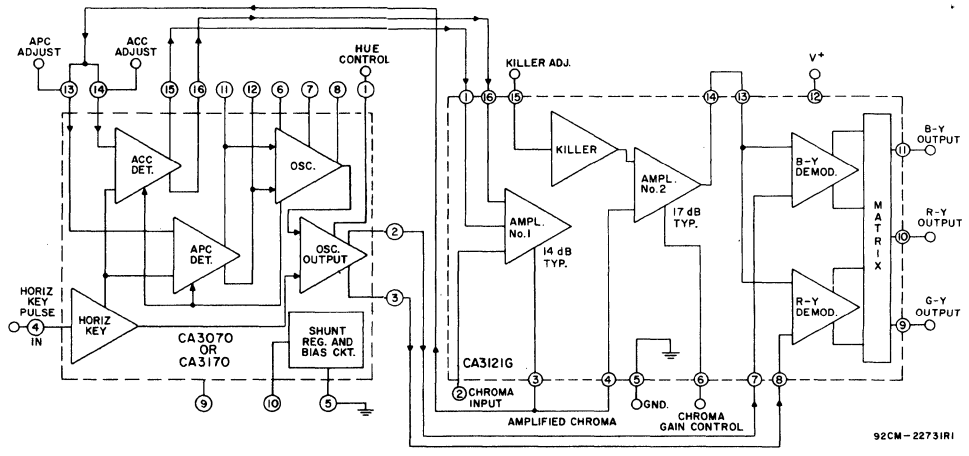


Fig. 5 – Simplified functional diagram of a two-package TV chroma system utilizing the CA3121G and CA3070 or CA3170 .

AM Radio Receiver Subsystem

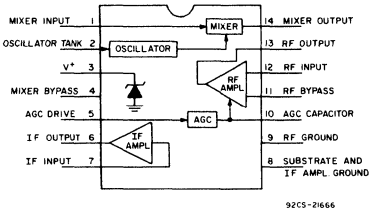
Includes RF Amplifier, IF Amplifier, Mixer, Oscillator, AGC Detector, and Voltage Regulator

The CA3123E* is a monolithic silicon integrated circuit that provides an rf amplifier, if amplifier, mixer, oscillator, AGC detector, and voltage regulator on a single chip. It is intended for use in super-heterodyne AM radio receiver applications particularly in automobiles. The CA3123E is supplied in a 14-lead dual-in-line plastic package and operates over the temperature range of −55° to 125°C.

* Formerly RCA Dev. No. TA6155

Features:

- **Low-noise, low-R_b' rf stage in cascode connection — eliminates Miller-Effect regeneration and allows controlled power rise by the choice of external components**
- **Mixer-oscillator stage with internal feedback — eliminates need for tapped or multi-winding oscillator coils**
- **Cascode if amplifier with controlled output impedance and negligible Miller Effect — eliminates regeneration and selectivity skewing**
- **Frequency-counter AGC circuit — allows control of AGC response by selection of the coupling capacitor**
- **Integral regulation with built-in surge protection**
- **Separately accessible amplifiers**



Terminal assignment diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
At Terminal No. 3 (V^+)	9 V
At Terminal No. 6 (IF Output)	40 V
At Terminal No. 13 (RF Output)	20 V
At Terminal No. 14 (Mixer Output)	20 V
DC CURRENT:	
Into Terminal No. 3 (V^+)	35 mA
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16" ± 1/3" (1.59 mm ± 0.79 mm) from case for 10 s max.	265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics In Circuit of Fig. 3						
DC Voltage:						
At Terminals 1, 4	V_1,V_4			4.7		V
At Terminals 2, 3, 14	V_2,V_3,V_{14}			6.8		V
At Terminal 5	V_5			0.25		V
At Terminal 6	V_6			12		V
At Terminal 7	V_7			0.76		V
At Terminals 8, 9	V_8,V_9			0		V
At Terminals 10, 11	V_{10},V_{11}			0.71		V
At Terminal 12	V_{12}			0.71		V
At Terminal 13	V_{13}			4.0		V
DC Current:						
Into Terminals 1, 4, 5, 7 8, 9, 10, 11, 12	I_1,I_4,I_5,I_7, I_8,I_9,I_{10},I_{11},I_{12}			0		mA
Into Terminal 2	I_2			1.2		mA
Into Terminal 3	I_3			15		mA
Into Terminal 6	I_6			4.3		mA
Into Terminal 13	I_{13}			4.5		mA
Into Terminal 14	I_{14}			0.170		mA
Performance Characteristics In Circuit of Fig. 3						
Sensitivity		Input Signal to Dummy Antenna at f_{IN}=1 MHz, 30% AM Modulation at f_{MOD}=400 Hz, for 11 mV output at V_O	–	2.3	5	μV
Signal-to-Noise Ratio	S/N	Ratio of Output at V_O with Modulation ON and then OFF, Input Signal=100 μV, 30% AM Modulation at f_{MOD}=400 Hz	34	43	–	dB
Overload Distortion		Input Signal set at 1 MHz, 90% AM Modulation, Distortion at V_O must be ≤ 10%	160000	400000	–	μV

Dynamic Characteristics For Indicated Stages In Circuit of Fig. 3

Stage	Parallel Capacitance Input pF	Parallel Capacitance Output pF	Parallel Resistance Input Ω	Parallel Resistance Output Ω	Transconductance μmhos
RF Amplifier	80	6	750	2 x 10^6 min.	140000
IF Amplifier	35	3.5	950	10^4	80000
Mixer	6	2	2000	2 x 10^6 min.	2500 (Mixer) 3000 (Amplifier)

TYPICAL CHARACTERISTICS

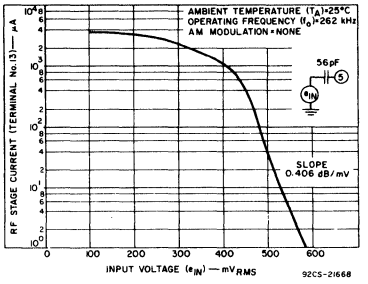


Fig. 1 — Control of RF stage by signal into Terminal No.5.

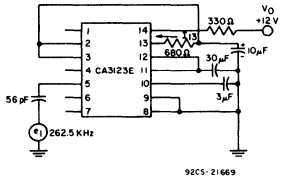


Fig. 2—Test circuit for Fig. 1.

Television Chroma Demodulator

RCA-CA3125E is a monolithic silicon integrated-circuit chroma demodulator having three separate demodulators with independent phase control. It is designed to function compatibly with the CA1398E IC Chroma Processor as well as other commercially available Chroma Processors in R-G-B Systems of color-TV receivers. The CA3125E is supplied in a 14-lead dual-in-line plastic package.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25°C$

SUPPLY VOLTAGE	25 V
SUPPLY CURRENT	20 mA
AMBIENT-TEMPERATURE RANGE:	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

Features:

- **Luminance input**
- **Blanking control input**
- **Three separate demodulators with independent phase control**
- **Low output offset voltage** ..... **0.4 V**

TYPICAL STATIC CHARACTERISTICS AT $T_A = 25°C$, $V^+ = +20$ VOLTS

SUPPLY CURRENT	9.6 mA
BRIGHTNESS CONTROL VOLTAGE:	
Measured with 8 volts at Terminals 11, 12, and 13	1.4 V
MAX. OUTPUT DIFFERENCE VOLTAGE:	
Measured between any two of Terminals 11, 12, and 13	±0.4 V
MAXIMUM DC DETECTOR UNBALANCE VOLTAGE:	
DC voltage shift on Terminals 11, 12, and 13 when Terminals 1, 2, and 3 are alternately biased 0.5 volt positive, then negative with reference to Terminal 14	+150 mV

TYPICAL DYNAMIC CHARACTERISTICS AT $T_A = 25°C$, $V^+ = +20$ volts

BLUE CHROMA GAIN:	
Peak-to-peak voltage at Terminal 11 with 1.0 volt peak-to-peak applied differentially between Terminals 6 and 7, and with a subcarrier injection voltage of 1 volt peak-to-peak	7.36 Vp-p
RED GAIN RATIO:	
$\frac{\text{Peak-to-peak voltage at Terminal 13}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100$	100%
GREEN GAIN RATIO:	
$\frac{\text{Peak-to-peak voltage at Terminal 12}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100$	30%
LUMINANCE GAIN:	
Peak-to-peak voltage measured at Terminals 11, 12, and 13, with a peak-to-peak voltage of 0.1 volt applied to Terminals 6 and 7 (common mode), and with no subcarrier injection	0.7 Vp-p

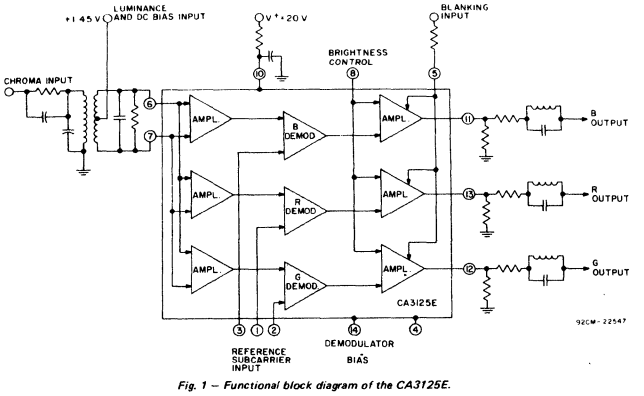


Fig. 1 – Functional block diagram of the CA3125E.

2. When the overload detector is used, a large resistor (nominally 47,000 ohms) must be placed in series with Terminal 16 to set the required RC time constant. The same RC network series serves to set the killer time constant.
3. The setting of the free-running oscillator frequency requires the presence of the keying pulse. The free-running frequency will be erroneous if Terminal 1 is dc shorted during the setting operation because of the dc offset voltage introduced to the AFPC detector.
4. Care must be taken in PC board designs to provide reasonable isolation between the oscillator portion of the circuit (Terminals 6, 7, and 8) and the chroma input (Terminal 1).

Overload Detector

The overload detector accomplishes two purposes:

1. It prevents oversaturation due to low burst-to-chroma ratios.
2. It prevents overload conditions due to noise.

Both of these conditions are discussed in more detail in ICAN-6247. The extent to which the overload detector is used depends upon the individual receiver design goals. If greater than 0.5-volt peak-to-peak output is desired, the chroma output at Terminal 15 can be tapped to yield any desired degree of overload detector action.

Chroma Gain Control

The chroma gain control operates by varying the base bias on current source transistor Q25. To ensure proper temperature tracking of the chroma gain control, it is essential that the control be operated from a supply source derived from the reference voltage at Terminal 12. Because the control operates from a current source, chroma gain is much more predictable and far less temperature sensitive than controls that steer current by means of a differential amplifier. The typical chroma gain characteristic for the CA3126Q is shown in Fig. 3.

Subcarrier Regenerator Oscillator

The oscillator filter consists of a 3.579545-MHz crystal, a 680-ohm resistor, and a 10-pF capacitor connected in series across Terminals 6 and 7. A 33-pF capacitor, shunt connected from Terminal 7 to ground, rolls off higher-order harmonics, thereby preventing oscillation at the crystal third-harmonic frequency. A curve of the typical static phase error as a function of the free-running oscillator frequency is shown in Fig. 4. It should be noted that the slope of the curve determines the dc gain of the phase-locked loop, i.e., 40 Hz per degree.

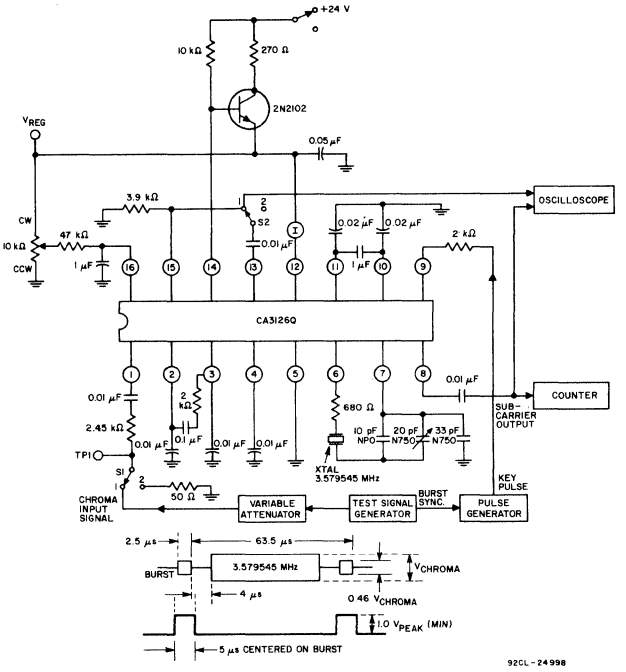


Fig. 2–Test circuit for CA3126Q.

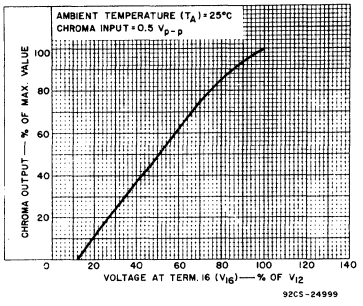


Fig. 3–Chroma gain control.

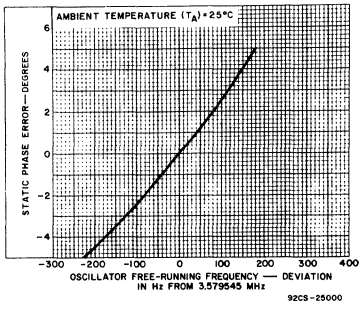


Fig. 4–Static phase error.

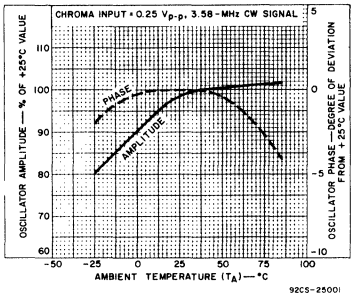


Fig. 5–Amplitude and phase variations of oscillator output vs. temperature.

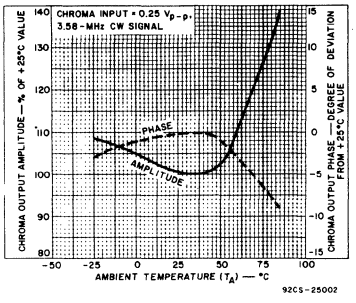


Fig. 6–Amplitude and phase variations of chroma output vs. temperature.

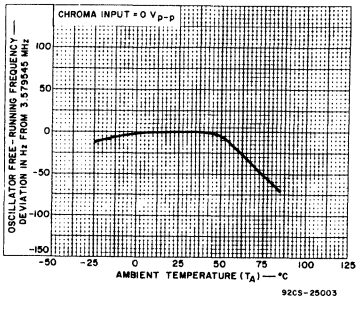


Fig. 7–Variation of oscillator free-running frequency vs. temperature.

Thermal Considerations

The circuit of the CA3126Q is thermally compensated to achieve the optimal operating characteristics over the normal operating temperature range of TV receivers. Figs. 5 and 6 show the oscillator- and chroma-output amplitudes and phases as a function of temperature (Terminals 8 and 15), respectively. Both the oscillator- and chroma-output amplitudes and phases are measured relative to the chroma-input phase. The performance of the oscillator free-running frequency as a function of temperature is shown in Fig. 7. All the temperature plots are characteristic of the test circuit with the indicated component types and values given in Fig. 2.

5-Watt Audio Amplifiers

With Integral Heat Sink

RCA-CA3131EM and CA3132EM are audio amplifiers with integral preamplifier stages on single integrated-circuit monolithic chips.

Utilizing a uniquely designed package with an integral heat sink, these devices can provide a power-output signal in excess of five watts at an ambient temperature of 25°C.

The CA3131EM employs an internal feedback network that sets the over-all gain of the amplifier to typically 48 dB.

The CA3132EM omits the internal feedback network. This arrangement offers the circuit designer a wide latitude in the choice of an external feedback network more suitable to a specific application.

Both types are encapsulated in a 16-lead dual-in-line plastic package with 4 center leads removed.

The CA3131EM and CA3132EM are electrically equivalent to and pin compatible with types SN76013 and SN76023, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE, V^+	28 V
CONTINUOUS OUTPUT POWER, P_O (with R_L = 8 Ω and V^+ = 24 V)	8 W RMS
MINIMUM RECOMMENDED LOAD IMPEDANCE, R_L	8 Ω
AMBIENT OPERATING TEMPERATURE, T_A (at 6 W RMS Output Power)	70 °C
STORAGE TEMPERATURE RANGE	−55 to +150 °C

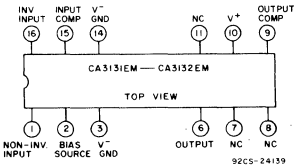


Fig. 1—Terminal assignment of the CA3131EM and CA3132EM.

Features:

- **Power Output: 4 W min., 5 W typ.**
- **Complete amplifier including: preamplifier stages, power-output amplifier, and integral heat sink**
- **High power-supply rejection ratio**
- **Operating voltage: V^+ = 24 V typ.**
- **Available with internal feedback (CA3131EM) or without feedback (CA3132EM)**

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 24 V

Characteristic	Symbol	Conditions	Values Min.	Values Typ.	Unit
Input Impedance	Z_I		200k	–	Ω
Power Output	P_O	At clipping onset			
		R_L = 8 Ω	4	–	W
		R_L = 16 Ω	3	–	W
Closed-Loop Gain — CA3131EM	A	f = 1 kHz	46	48	dB
Supply Current	I^+	Zero signal	–	10	mA
Total Harmonic Distortion	THD	P_O = 50 mW–4 W, R_L = 8 Ω	–	1	%
		P_O = 50 mW–3 W, R_L = 15 Ω	–	1	%
Noise Voltage	V_n	f=20 Hz–20 kHz	–	1.5	mV RMS

Determining External Component Values (Refer to Figs. 2 & 3)

The dc quiescent output voltage is set by the voltage at Terminal 1. This voltage, in turn, is set by the internal voltage at Terminal 2 less I_I (input current, fixed by $R_A + R_B$, for Q4). The voltage at Terminal 2 is set slightly above half the supply voltage to allow for the voltage drop across $R_A + R_B$. Filter R_BC3 attenuates any ac ripple injected from the supply line and prevents positive feedback to Terminal 1. The rejection of supply voltage is a direct function of the filter attenuation.

The input impedance of the audio amplifiers is a function of the closed-loop gain and the magnitude of the Q8 current. In practice the input impedance is well above 1 megohm. The input signal, applied through C2, sees an impedance equivalent to the resistance of R_A connected in parallel with the amplifier input impedance. Hence, the value of R_A in most cases is dominant in establishing the input signal impedance.

The value of C1 depends on the regulation of the power supply. It is possible for the amplifier to work with a value of C1 as low as 0.1 μF to attenuate high-frequency signals in the supply line. Ideally, C1 should be placed as near Terminal 10 as possible. An electrolytic capacitor should be used for C1 if the power supply is poorly regulated to avoid ripple at the output.

Capacitor C6 at Terminal 15 provides over-all compensation. If a 1000-pF capacitor is used for C6, then the first breakpoint for a 46-dB closed-loop gain occurs at 200 kHz. Higher capacitance values will cause the constant current from Q10 to charge C6 on the positive voltage swing and thus limit the slew rate at high-signal levels. Because p-n-p transistor Q19 has a lower gain-bandwidth product (f_T) than the n-p-n transistors, C7 is connected to Terminal 9 to compensate for gain losses occurring in the negative voltage swings.

The use of the filter networks C8 and R_D at the output Terminal 6 is a standard requirement for class B audio outputs driving reactive speaker loads. Capacitor C8 compensates for the speaker inductance and R_D limits the current surges through C8.

The value of the coupling capacitor C9 to the load determines the low-frequency response of the amplifier.

Closed-Loop Gain

The closed-loop gain for either type is set by the ratio (R1 + R2)/R1. These resistors are included in the CA3131EM circuit and are external when used with the CA3132EM. In either type, the low-frequency value (−3 dB point) is reached when the impedance of C5 equals the value of R1.

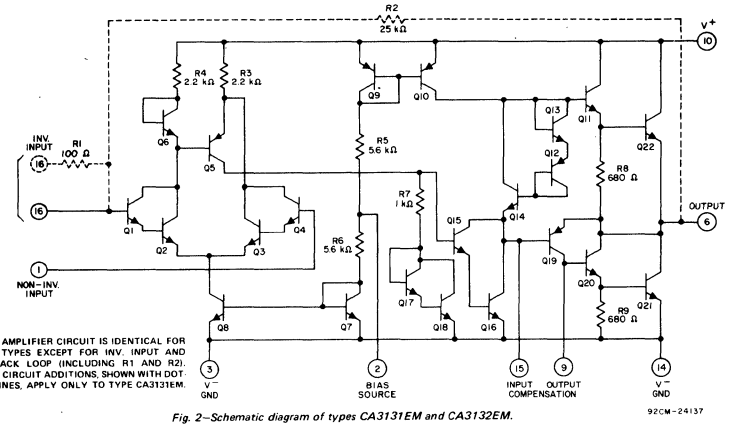
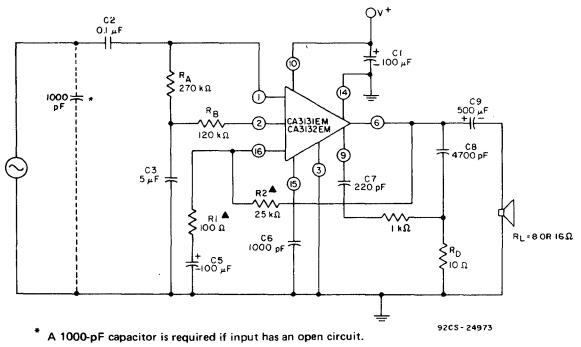


Fig. 2—Schematic diagram of types CA3131EM and CA3132EM.



* A 1000-pF capacitor is required if input has an open circuit.

▲ External resistors R1 and R2 are used only with the CA3132EM. When testing the CA3131EM, omit R1 and R2 and connect the (+) termination of C5 to Terminal 16.

Fig. 3—Test circuit for types CA3131EM and CA3132EM.

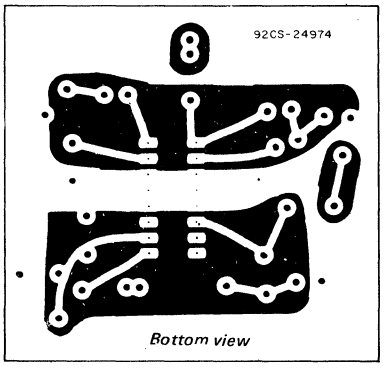


Fig. 4—Printed-circuit board (actual size) containing the test circuit, shown in Fig. 3, for the CA3131EM.

ELECTRICAL CHARACTERISTICS
Test Conditions: T_A = 25°C, V^+ = +30 V (applied to Term. 1), DC Volume Control, R_X = 75 kΩ, R_L = 16 Ω, unless otherwise indicated. Refer to Fig.2.

CHARACTERISTIC	SPECIAL TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Static Characteristics					
Current into Term. 1, I_1	P_O = 0	15	30	45	mA
Dynamic Characteristics					
IF AMPLIFIER: Input Limiting Voltage, V_{15}(lim) (at −3 dB point)	f_O = 45 MHz, f_m = 400 Hz, Δf = ±25 kHz	–	200	400	μV
AM Rejection, AMR	f_O = 4.5 MHz, f_m = 400 Hz, Modulation Index = 0.3, V_{15} = 20 mV	40	50	–	dB
Input Resistance, R_I	V_{15} = 35 mV	–	25	–	kΩ
Input Capacitance, C_I	V_{15} = 35 mV	–	3	–	pF
DETECTOR: Recovered af Voltage (Term. 9), V_O(af)	f_O = 4.5 MHz, f_m = 400 Hz, Δf = ±25 kHz, V_{15} = 100 mV	–	700	–	mV
Total Harmonic Distortion, (THD)		–	0.8	3	%
Output Resistance, R_O	At Term. 9	–	7.5	–	kΩ
ATTENUATOR: Maximum Attenuation	R_X = 0	–	10	15	mV
UNATTENUATED AUDIO: Recovered af Voltage (Term. 8), V_O(af)	f_O = 4.5 MHz, f_m = 400 Hz, Δf = ±25 kHz, V_{15} = 100 mV	–	600	–	mV
Total Harmonic Distortion (THD)		–	0.8	–	%
AUDIO POWER AMPLIFIER: Voltage Gain, A(af)	f = 1 kHz	–	35	–	dB
System Total Harmonic Distortion THD (System)	P_O = 1 W (I_T = 140 mA typ.)	–	1.5	–	%
	P_O = 2 W (I_T = 180 mA typ.)	–	1.6	3	%
Power Output, P_O	THD (System) = 10% (I_T = 210 mA typ.)	–	5*	–	W
Input Resistance, (R_I(af)	f = 1 kHz	–	100	–	kΩ

* With suitable heat sink for the CA3134G.

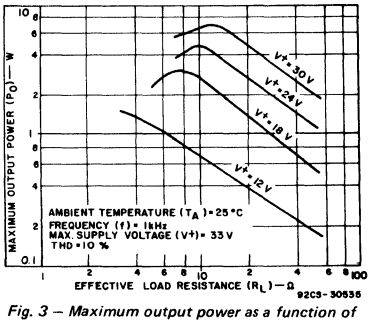


Fig. 3 – Maximum output power as a function of effective load resistance.

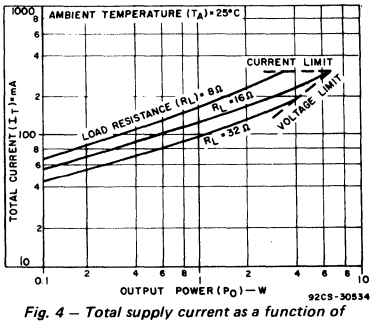


Fig. 4 – Total supply current as a function of output power.

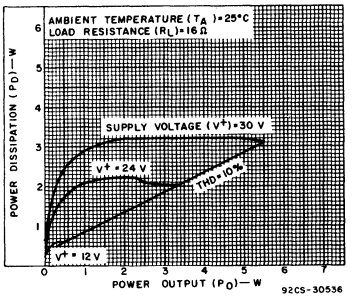


Fig. 5 – Power dissipation as a function of output power.

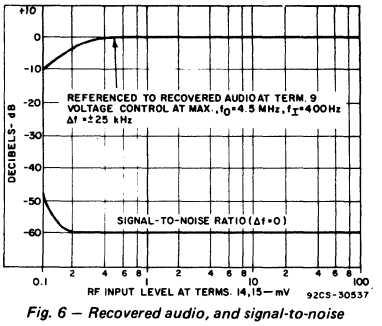


Fig. 6 – Recovered audio, and signal-to-noise ratio as a function of rf input level.

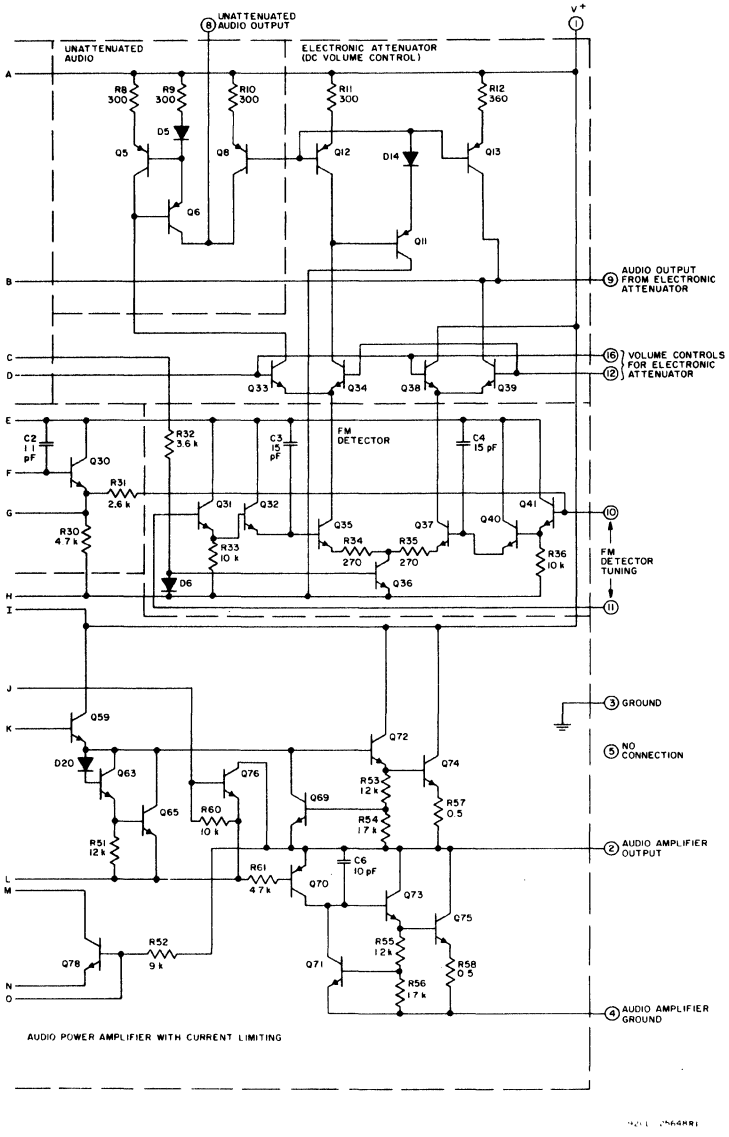


Fig.7 – Schematic diagram of the CA3134 .

DYNAMIC ELECTICAL CHARACTERISTICS at T_A = 25°C (See Fig. 4)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Min. Video Gain	S1, S2 = 1; S3, S4 = 2 V_{IN} = 70 mV_{RMS}, f = 100 kHz, V_{16} = 12 V	0.2	0.35	0.5	V_{RMS}
Max. Video Gain	S2 = 1; S1, S3, S4 = 2 V_{IN} = 70 mV_{RMS}, f = 100 kHz, V_{16} = 0 V	1.6	2.1	2.6	V_{RMS}
Limited Video Gain	S2, S4 = 1, S1, S3 = 2 V_{IN} = 70 mV_{RMS}, f = 100 kHz, V_{16} = 0 V	–	0.3	–	V_{RMS}
Min. Chroma Gain	S1, S3 = 1; S2, S4 = 2; V_{16} = 12 V; chroma in = 530 mV_{RMS}, f = 3.58 MHz	–	0.095	–	V_{RMS}
Max. Chroma Gain	S3 = 1; S2 = 2, V_{16} = 0 V; chroma in; S1 = 2, S4 = 2 530 mV_{RMS}, f = 3.58 MHz	0.5	0.65	0.8	V_{RMS}
Video Freq. Response	S2 = 1, S1, S3, S4 = 2 V_{IN} = 70 mV_{RMS}; V_{16} = 0 V; f = 3.58 MHz	1	1.9	2.8	V_{RMS}
Chroma Phase Angle	S3 = 1; S2 = 2; V_{16} = 0 V; chroma in; S1 = 2, S4 = 2 530 mV_{RMS}, f = 3.58 MHz	12	19.5	27	Degrees
Chroma Gain with V^+ Variation	Vary V^+ from 10.8 V (REF.) to 13.2 V V_{16} = 50% of V^+; S1, S3 = 1 S2, S4 = 2	–	1.5	–	dB
Video Gain with V^+ Variation	Vary V^+ from 10.8 V (REF.) to 13.2 V V_{16} = 50% of V^+; S1, S2 = 1 S3, S4 = 2	–	1.5	–	dB

Typical max. luminance input before clipping (f = 100 kHz):

V_{16}	INPUT
+12 V	2.5 V_{p-p}
+6 V	0.75 V_{p-p}
0 V	0.45 V_{p-p}

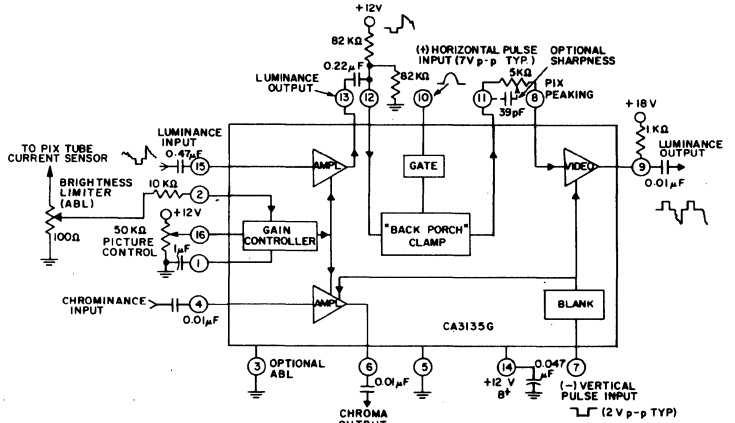


Fig. 1 – Block diagram.

CIRCUIT DESCRIPTION

(See fig. 2 for schematic diagram).

A video (luminance) signal from the receiver's "second detector" is coupled through a capacitor to term. 15 with sync-negative polarity. For purposes of the following amplifier, the level is clamped at the most negative point (sync tips) at the input (this is not the point at which the final "black"-level clamping, or dc restoration, is performed). The capacitor at term. 15 is charged on the most negative excursions of the signal by conduction of Q4. Positive signal excursions lift the emitter of Q4 into cutoff. The signal voltage on R3 develops a signal current in Q6. The current passes through Q7 and Q8, the division of current depends on the condition of the gain-adjusted signal voltage on the load resistors (discussed below). The gain-adjusted signal voltage on the load resistors is converted to current by the emitter-follower Q14 into R9, and fed into the current mirror, Q15, Q16, and Q17. The output of the current mirror develops a voltage across R13. The dc level is shifted by withdrawing some current from the input to the mirror. The fixed dc-level shifting current is developed in R6 and its diode string and is mirrored in Q13. Because the dc level is altered by adjustment of the gain, compensating dc currents that depend on these adjustments are fed into the mirrors through R13 and R29. The compensations are arranged so that, as gain is varied, the dc level of "black" is approximately constant at the output term. 13. The output is driven by emitter follower Q18, which has a short-circuit pulldown protection circuit, R14 and Q19. A constant-current source Q20 loads the emitter-follower to prevent distortion in the emitter-follower that may result from using a resistive load. The constant current is derived by mirroring the current in the diode D23. The resistor R15 prevents serious interaction with another current source mirrored from this point in case Q20 saturates.

The video output signal at term. 13 is coupled by a capacitor to term. 12. The polarity has not been inverted by the first amplifier, and sync is in the negative direction at this point. Black-level clamping is accomplished by application of a flyback pulse to term. 10. Between pulse peaks, Q29 is not conducting, and the base of Q24 goes up to the supply voltage so that term. 12 can be at any voltage between ground and the supply. While the flyback pulse is positive, that is during the blanking interval, the base of Q24 is held at about 2.8 volts. The most positive signal excursion during that time will cause Q24 to conduct with the result that the capacitor feeding term. 12 is charged until the most positive point of the signal is just at the conduction point, about 3.5 volts. The most positive part of the signal *during blanking* is the "back porch" or black-level reference. During trace time, the signal swings more positive, but the dc level of black is preserved regardless of the levels

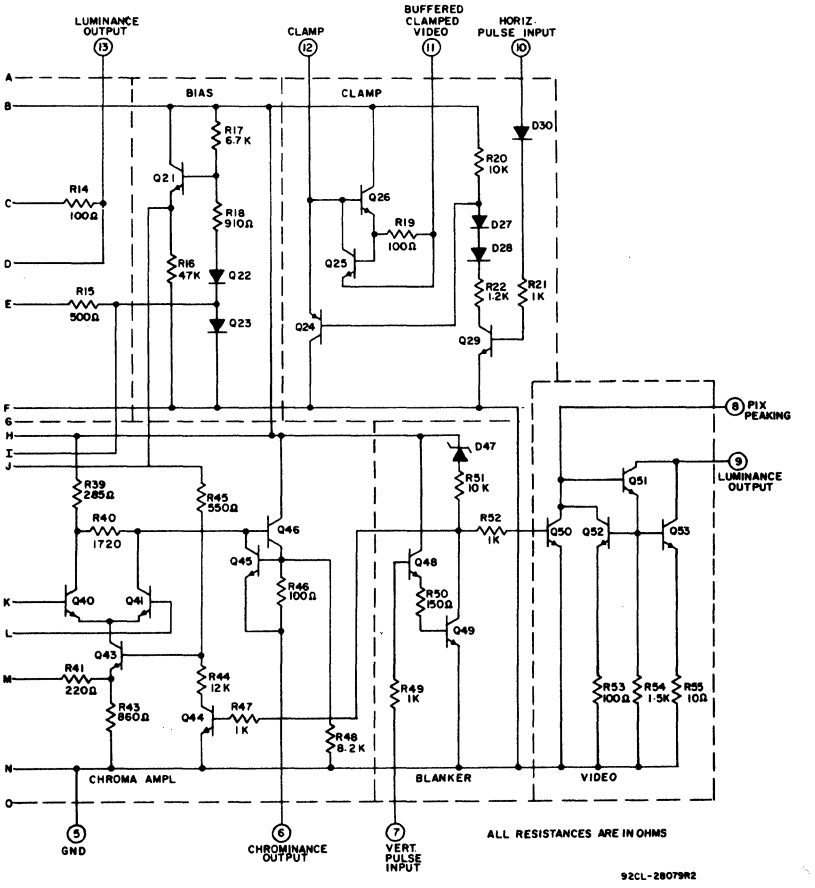


Fig. 2 – Schematic diagram

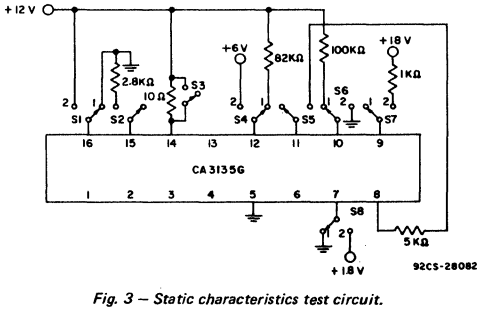


Fig. 3 – Static characteristics test circuit.

Preliminary Data

TV Video IF Phase-Locked-Loop Synchronous Detector for Color TV Receivers

Features:

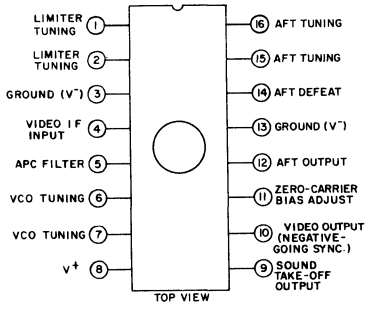
- PLL carrier oscillator with wide pull-in and hold-in range
- Excellent low-level detector linearity
- Noise inversion at video output
- Wide range, variable zero-carrier level adjustment
- Automatic Fine Tuning (AFT) Detector
- Separate output for sound take-off
- 12-volt power supply

The RCA-CA3136E is a linear IC synchronous detector employing a phase-locked oscillator to demodulate the 45.75-MHz video if signals in color-TV receivers. The CA3136E features AFT voltage for dc control of the tuner; an adjustment for the zero-carrier dc level at the video output terminal; an amplifier arrangement for inverting noise impulses toward the black level; and a separate output terminal (non-inverting) for the sound if.

The CA3136E is supplied in a 16-lead plastic "power-stud" dual-in-line package.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Power Supply Voltage	15 V
Power Supply Current	100 mA
Input Signal Voltage	1 Vrms
Device Dissipation:	
With no Heat Sink:	
Up to T_A = 25°C	1.4 W
Above T_A = 25°C	derate linearly at 11.1 mW/°C
With Infinite Heat Sink:	
Up to T_A = 70°C	6.5 W
Above T_A = 70°C	derate linearly at 83.3 mW/°C
Thermal Resistance:	
$R_{\theta JS}$ (Junction to Stud)	12 °C/W
Ambient Temperature Range:	
Operating	−40 to +85°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At a distance 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	265°C



92CS-28845

TERMINAL DIAGRAM

SUGGESTED GENERAL ALIGNMENT PROCEDURE

Fig. 1 shows a block diagram of the CA3136 in a typical circuit indicating the internal functions as well as the external circuitry and signals. A 45.75-MHz, 100-mVrms (50-ohm) signal is applied to the VIDEO IF INPUT (Terminal 4). While monitoring the VIDEO OUTPUT (Terminal 10), make the following adjustments in the indicated sequence; (1) adjust the VCO TUNING coil for a dc signal (lock). (2) Adjust the LIMITER TUNING coil for a minimum dc voltage on Terminal 10. (3) Adjust the VCO TUNING coil for 5.2 Vdc on Terminal 5 (with 12 volt supply on Terminal 8). (4) Close the AFT DEFEAT switch and note the dc voltage at the AFT OUTPUT (Terminal 12). (5) Return the AFT DEFEAT switch to its open position, and adjust the AFT TUNING coil for the same dc voltage noted when the AFT DEFEAT switch was closed. (6) Remove the rf input and adjust the ZERO CARRIER BIAS potentiometer for 7 volts dc on the VIDEO OUTPUT (Terminal 10). This final adjustment completes the alignment procedure.

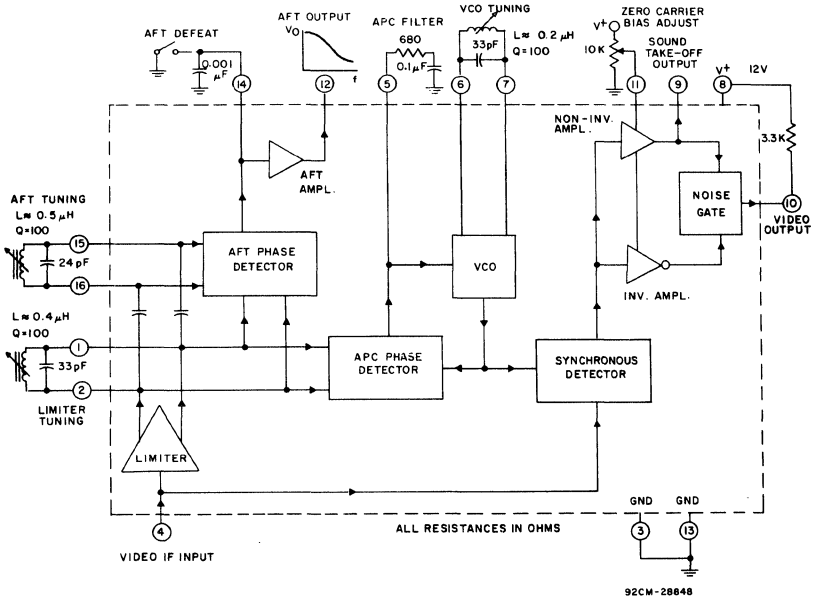


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Fig. 1 – Block diagram of the CA3136 in a typical circuit application.

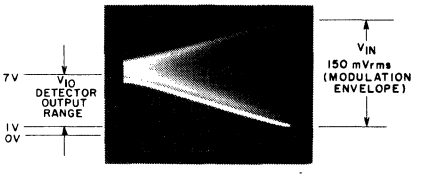


Fig. 2 – Typical detector output linearity.

TYPICAL ELECTRICAL CHARACTERISTICS

At $V^+ = 12$ VDC, $f_c = 45$ MHz, $T_A = 25^oC$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	VALUE	UNITS
Supply Current	$I_8 + I_{10}$		60	mA
Video-Output Voltage	V_{10}	Zero Carrier Bias Adjust	7	V_{DC}
Noise-Inversion Offset Voltage	V_{10}	Referenced to Zero-Carrier Level	0.3	V_{DC}
Sound IF-Take-Off Output Voltage	V_9	$V_{10} = 7\ V_{DC}$	7.7	V_{DC}
AFT Output Voltage	V_{12}	AFT Defeat Switch Closed	3	V_{DC}
Oscillator Pull-In Range			3	MHz
Oscillator Hold-In Range			6	MHz
Detector Conversion Gain			30	dB
Video Bandwidth			9	MHz
Carrier Rejection at Video Output: fc = 45 MHz			30	dB
2 fc = 90 MHz			40	dB
Video IF Parallel Input Impedance: Resistance at Term. 4	R_p		4	kΩ
Capacitance at Term. 4	C_p		5	pF
Sound Take-Off Output Resistance at Term. 9	R_o	1 MHz	50	Ω
Video Output Resistance at Term. 10	R_o	1 MHz	50	Ω

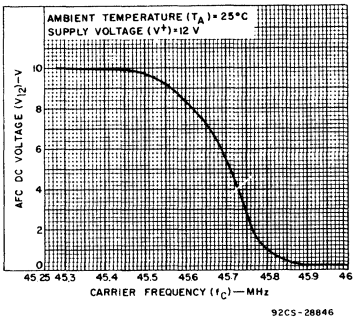


Fig. 4 – Typical AFT output of CA3136.

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $V^+ = 11.2$ V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
STATIC (See Fig.2)						
Supply Current	I_T		–	35	47	mA
Reference Subcarrier Input	V_{16}		–	6.7	–	VDC
Oscillator Reference Inputs	V_9, V_{10}		–	3.8	–	VDC
R-Y, G-Y, B-Y Outputs	V_6, V_7, V_8		–	5	–	VDC
Chroma Input	V_3		–	1.2	–	VDC
DYNAMIC (See Fig.3)						
Tint and Sensitivity Limiting	V_{11}	V_{16} = 200 mV p-p @ 3.58 MHz	200	300	–	mVp-p
Tint Limiting	V_{11}	V_{16} = 800 mV p-p @ 3.58 MHz	–	425	600	mVp-p
Tint Amplifier* Phase Reference	ϕV_{11}	V_{16} = 400 mV p-p, Term.1 = 11.2 VDC	–35	–25	–15	Degrees
Tint Control▲ Range	$\Delta\phi_{11}$	V_{16} = 800 mV p-p, Term.1 = 1.2 VDC	–130	–110	–80	Degrees
Ratio G-Y to R-Y	V_7/V_6	V_{16} = 400 mV p-p,	28	33	38	%
Ratio B-Y to R-Y	V_8/V_6	V_3 = 40 mV p-p	108	120	132	%
Demodulated Chroma Output R-Y	V_6	V_{16} = 400 mV p-p, V_3 = 40 mV p-p	350	550	–	mV p-p
Color Difference Output (Bandwidth at 3 dB)		V_3 = 40 mV p-p	–	900	–	kHz
Maximum Color Difference Outputs: R-Y	V_6	V_{16} = 400 mV p-p, V_3 = 300 mVp-p	1.5	2.2	–	V_{p-p}
G-Y	V_7		0.42	0.7	–	
B-Y	V_8		1.6	2.65	–	
"Flesh Detector" Reference:		Set-Up: Term.2 = 1.6 V, Term.1 = 11.2 V, Term.16 = 400 mV p-p @ 0° Reference Angle, Term.3 = 40 mV p-p @ 10° Reference Angle, S_1 Closed (Term.15 at GND)	Reference Set-Up			
"Flesh Detector": Phase	ϕ_{11}	Same Set-up except S_1 open	–	0	–	Degrees
Amplitude	V_{11}		–	275	–	%
"Flesh Detector": Phase	ϕ_{11}	Same Set-up except Term.3 at 190° angle	–	0	–	Degrees
Amplitude	V_{11}		–	100	–	%
Small-Signal Output Resistance (Terms.6,7,8)	r_o		–	50	–	Ω
Small-Signal Input Resistance: Term.3	r_i		–	3	–	kΩ
Terms.9&10			–	2.5	–	

* Phase angle of term. 11 referenced to term. 16 phase angle.

▲ Phase angle of term. 11 with term. 1 = 1.2 V minus phase angle of term. 11 with term. 1 = 11.2 V.

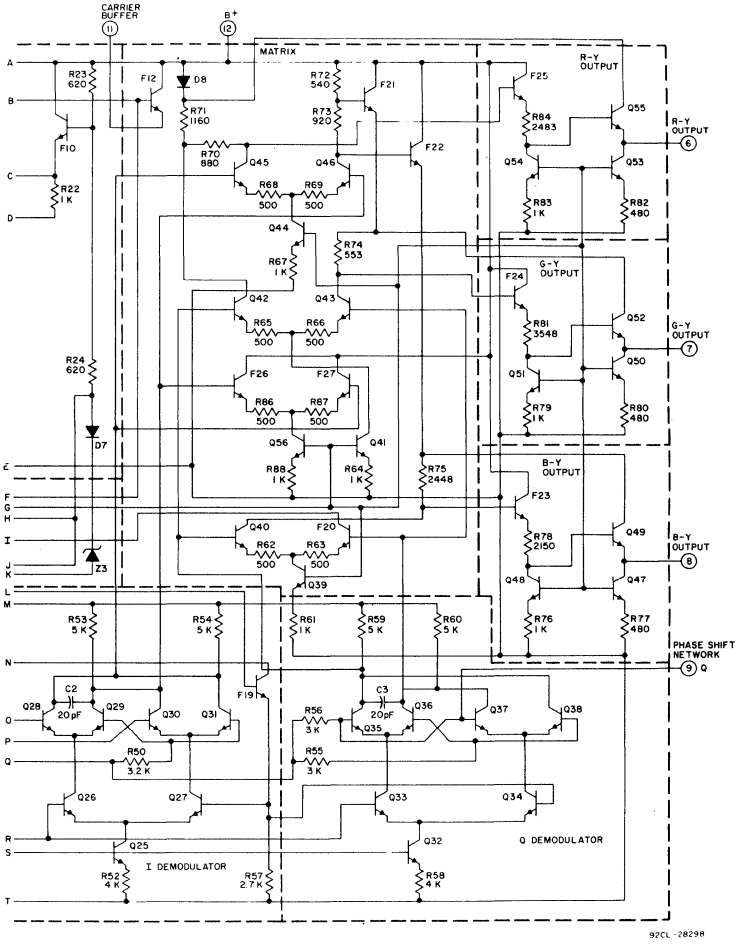


Fig.4 – CA3137E Schematic diagram.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $V^+ = 28$ V (Unless Otherwise Specified)

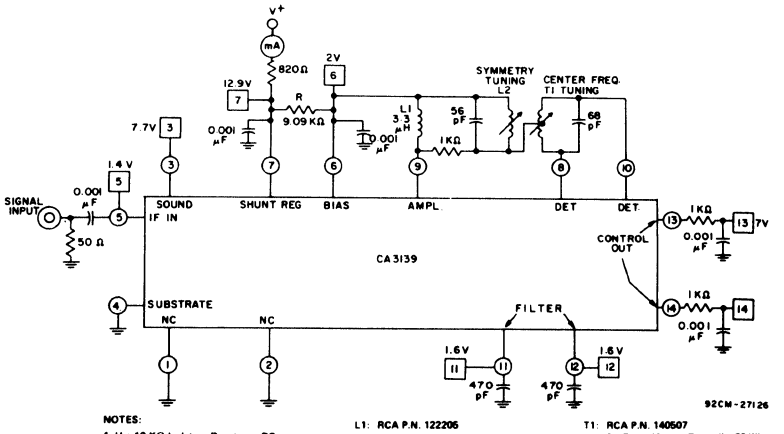
See Test Circuit, Fig. 2

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
NO SIGNAL INPUT				
Supply Current, I^+		15	20	mA
Low Voltage at Term. 7[1]	$V^+ = 20.8$ V	11	14.5	V
Shunt Reg. Voltage		12	14.5	V
Quiescent Voltage at Term. 3		4.5	10	V
Quiescent Voltage[2] at Terms. 13 and 14	Term. 13 connected to Term. 14	6	8.5	V
Quiescent Difference Voltage, Terms. 13 to 14		−0.8	+0.8	V
Quiescent Voltage at Term. 6		1.4	2.6	V
SIGNAL INPUT = 15 mV_{RMS} (Unless Otherwise Specified), Note 3				
Correction Voltage at Term. 13	f = 44.65 MHz	2.2	4.7	V
	f = 45.69 MHz	1.2	4.4	
	f = 45.81 MHz	9.6	13.8	
	f = 46.85 MHz	9.1	12.1	
Correction Voltage at Term. 14	f = 44.65 MHz	9.1	12.1	V
	f = 45.69 MHz	9.6	13.8	
	f = 45.81 MHz	1.2	4.4	
	f = 46.85 MHz	2.2	4.7	
4.5 MHz Output	Two-Tone Input f1 = 45.75 MHz at 15 mV f2 = 41.25 MHz at 5 mV	50	200	mV_{RMS}

NOTES: 1. $I_7 = 12$ mA maximum at $V_7 = 11$ V.

2. $V_{13} = 0.55\ V_Z \pm 0.7$ V

3. Resistor from term. 6 to term. 7 = 9.09 KΩ. Crossover steepens and "bow tie" width increases when resistor is decreased in value. Total peak swing decreases slightly.



NOTES:
1. Use 10 KΩ Isolation Resistor at DC Voltmeter Probe Tip When Making DC Measurements.
2. Typical No-Signal DC Potentials Are Shown.
3. Boxes Represent Test Points.

L1: RCA P.N. 122206
L2: RCA P.N. 14133
4½ Turns #22 Wire, O.D. = 0.25" (Typ.)
Q (Unloaded) = 100 (Min.)
f = 41.25 MHz
Inductance = 0.18 μh (Typ.)

T1: RCA P.N. 140507
3½ Turns (Center Tapped) #20 Wire, O.D. = 0.35" (Typ.)
Q (Unloaded) = 140 (Min.)
f = 45.75 MHz
Inductance = 0.18 μh (Typ.)

Fig. 2 — Test circuit.

CIRCUIT DESCRIPTION

The CA3139 consists of five functional circuits as shown in the block diagram, Fig. 1 (see Fig. 5 for schematic diagram).

1) **Cascode Amplifier** — Consists of emitter-follower Q1, common-emitter amplifier Q2, and common-base amplifier Q3.

2) **Bias Circuit** — Consists of Q4 and resistors R1, R4, R5, and an external resistor (user selectable) connected to the voltage regulator, terminal 7. The nominal value of the external resistor is 9.1 kΩ. Reduced values will raise the gain of the cascode amplifier chain, and higher values will reduce the gain. If the gain is increased, the AFT "Bow Tie" width will increase and the crossover slope will increase (become steeper). The input transistor Q1 is internally biased, so AC coupling is normally used to the input terminal 5.

3) **Intercarrier Mixer/Amplifier** — The output of the cascode amplifier at terminal 9 is also internally connected to the intercarrier mixer/amplifier chain consisting of transistors Q13 through Q17 and associated components. The video IF carrier at 45.75-MHz and the FM sound IF carrier at 41.25-MHz are down-converted to a 4.5-MHz FM signal by Q14. A low-pass filter removes the carriers and upper conversion signal components. The 4.5-MHz FM signal is further amplified and filtered by Q16 and C3. The FM sound output signal is at terminal 3. The gain with respect to a 5-mV sound carrier (tested with a 15-mV video carrier) input signal at terminal 5 is 10 to 40 when the resistor is connected between terminals 6 and 7 is 9.09 kΩ.

4) **AFT Detector and DC Amplifier** — Consists of Q6 through Q12 and related components. The detector inputs at terminals 8 and 10 are connected to the external discriminator transformer and biased through the transformer at terminal-6 potential. The total current through transistors Q7 and Q8 is held constant by the current-mirror transistors Q10, Q11, and Q12. External filter capacitors connected to terminals 11 and 12 assure that peak detection is accomplished. The AFT output voltages are shown in the Electrical Characteristics chart, and a graphical representation is shown in Fig. 4.

5) **Voltage Regulator** — An active shunt regulator, consisting of D1, D2, Z1, Z2, and Q5, is included to reduce the dynamic resistance.

TV Luminance Processor

The CA3143E is a monolithic silicon integrated circuit that performs the luminance processing functions of amplification; contrast, brightness and peaking control; blanking; and black-level clamping.

This device, when used in conjunction with the CA3126Q chroma processor and the CA3137E chroma demodulator, will provide a luminance/chrominance system having excellent tracking of controls. The CA3143E is supplied in a 14-lead dual-in-line plastic package.

Features:

- **Black-level clamping**
- **Linear dc controls for brightness, contrast, and peaking**
- **Horizontal and vertical blanking**
- **Operates with standard or tapped delay line**

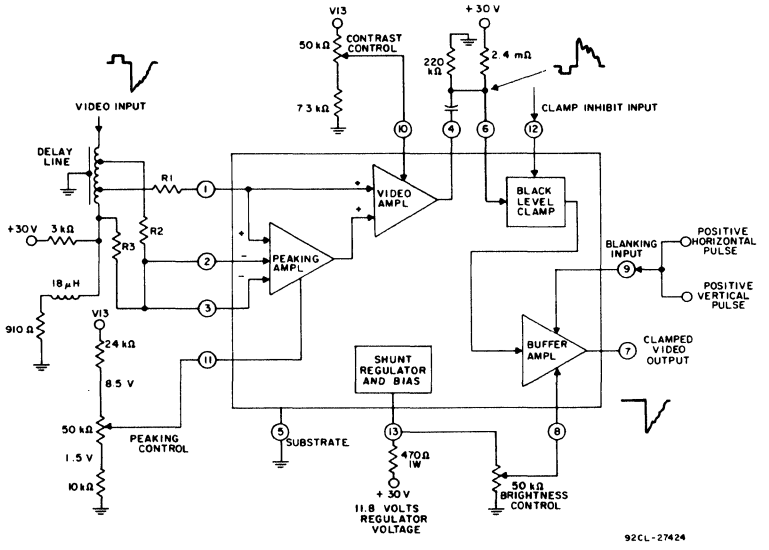


Fig.1 – Functional block diagram.

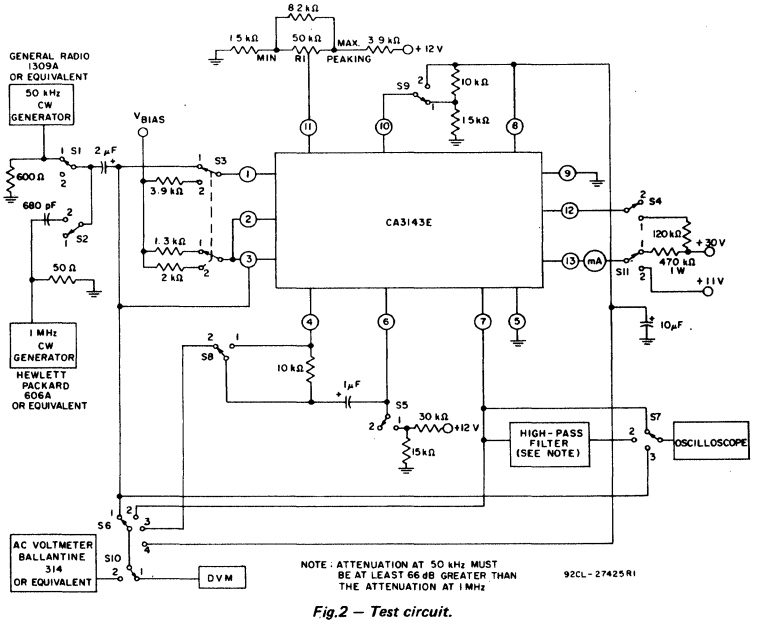


Fig.2 – Test circuit.

CIRCUIT DESCRIPTION

Fig. 1 is a block diagram of the CA3143E indicating the internal functions as well as external circuitry and signals. The video input signal with positive-going sync is applied to the input of the tapped delay line. Signals from fixed taps of the delay line are applied to terminals 1, 2 and 3 of the CA3143E. In referring to Fig.4, the signal from the delay line tap A is applied to the video input at terminal 1. The signals from taps B and C are summed where $V_A + V_B = V_{sum}$. The signal (V_{sum}) is then applied to the parallel connection of the peaking input terminals, 2 and 3. The video input signal is applied to a non-inverting input of the peaking amplifier while the peaking input signal (V_{sum}) is applied to an inverting input of the peaking amplifier.

Low-frequency video components are unattenuated, while high-frequency components are attenuated as a function of the delay-line tap points. The peaking amplifier is a differential amplifier, so that the output is proportional to V_1 minus V_{sum}. At low frequencies, the signal at terminals 2 and 3 is unattenuated, and the peaking amplifier produces no output at these frequencies. However, at high frequencies the signal at terminals 2 and 3 is attenuated thus, the peaking amplifier output consists of high-frequency video. The peaking control setting determines the amplitude of the peaking signal which is then fed to the video amplifier, where it is added to the video input signal and amplified. The setting of the peaking control does not substantially affect the dc quiescent voltage at terminal 4.

The low-impedance video amplifier output is at terminal 4. The signal is fed through an external coupling capacitor to terminal 6, the black-level clamp input. The action of the black-level clamp is such that it clamps to the black level rather than to the sync level. Refer to the circuit diagram in Fig.3. Consider the situation where no signal is applied to terminal 12. Terminal 6 is biased through diode D2. The signal at terminal 6 will clamp its most negative excursion (sync pulse) to the anode voltage of D2. However, if a positive pulse is applied to terminal 12 during the sync interval, the anode of D2 is forced to ground due to saturation of Q17. The clamp is thus disabled, and terminal 6 will clamp to the next lower signal level, the black level.

MAXIMUM RATINGS, *Absolute-Maximum Values*:

DC SUPPLY CURRENT (Into Terminal 13)* . . . . . 59.5 mA
DEVICE DISSIPATION:*
Up to $T_A = 55^oC$ . . . . . 750 mW
Above $T_A = 55^oC$ . . . . . derate linearly 7.9 mW/^oC
AMBIENT–TEMPERATURE RANGE:
Operating . . . . . –40 to +85^oC
Storage . . . . . –65 to +150^oC
LEAD TEMPERATURE (During soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 s max. . . . . +265^oC

* Although the CA3143E is rated for maximum dissipation of 750 mW, it is recommended that the current into terminal 13 be limited by external circuit resistance to 39 mA for a typical voltage at terminal 13 of 11.8 volts.

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

Characteristic	Bias Volts (V)	Test Conditions: Switch Numbers S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	LIMITS Min.	Typ.	Max.	UNITS
		Switch Positions For Characteristics Measurements														
STATIC																
Voltage: At Term. 13 (V13)	6.1	2	1	1	2	2	4	1	2	2	1	1	11	11.8	13.2	V
Quiescent Voltage At Term. 4 (V4)	6.1	2	1	1	2	2	3	1	2	2	1	1	3.3	4	5.7	V
Quiescent Voltage At Term. 7 (V7)	6.1	2	1	1	2	2	2	1	2	2	1	1	7.1	7.7	8.3	V
Current into Term.13 (Term.13 Connected to +11 V) (I13)	6.1	2	1	1	2	2	3	1	2	2	1	2	10	19	30	mA
DYNAMIC																
Wide-Band Gain (Note 1)	5.8	1	1	1	2	1	2	1	1	1	2	1	6	8.3	11	dB
Contrast Gain Reduction (Note 2)	5.8	1	1	1	2	1	2	1	1	2	2	1	27	30	–	dB
Peaking Gain (Note 1)	5.8	1	1	2	2	1	2	1	1	1	2	1	15	18.4	22	dB
Peaking Gain Reduction (Note 3)	5.8	1	1	2	2	1	2	1	1	1	2	1	16	18	–	dB
Max. Intermodulation Distortion: 2V (Note 4)	5.8	1	–	1	1	1	2	–	2	1	2	1	–	20	–	%
3V (Note 5)	5.8	1	–	1	1	1	2	–	2	1	2	1	–	40	–	%

Note 1: Set 50-kHz generator for 100 mVp-p. Adjust R1 Peaking Control (See Fig.2) for minimum setting. Measure wide-band gain at terminal 7.

Note 2: Set 50-kHz generator for 100 mVp-p. Adjust R1 for minimum setting. Measure contrast gain reduction at terminal 7.

Note 3: Set 50-kHz generator for 100 mV-p-p. Adjust R1 for maximum setting. Measure peaking gain reduction at terminal 7.

Note 4: Adjust R1 for minimum setting. With S2 at switch position1 and S7 at switch position 3, set 50-kHz generator for 2 Vp-p. Then with S2 at switch position 2, set 1 MHz generator for 100 mVp-p. Then with S7 at switch position 2, measure downward modulation of the 1-MHz signal due to the 50-kHz signal.

Note 5: Repeat step 4 except that the 50-kHz generator must be set at 3 Vp-p.

The clamped video signal at terminal 6 is amplified and inverted at terminal 7. Blanking is accomplished by applying horizontal and vertical sync pulses to terminal 9. The pulses turn ON p-n-p transistor Q6 which shorts the base of transistor Q15 to the terminal 13 supply voltage. The brightness control function is accomplished by varying the voltage on terminal 8. The gain of the inverter stage remains constant, but the dc reference voltage follows the terminal 8 voltage. The contrast control function is accomplished by varying the voltage of terminal 10. Increasing the voltage on terminal 10 lowers the gain of the video amplifier. This reduction in gain does not substantially affect the dc quiescent voltage at terminal 4.

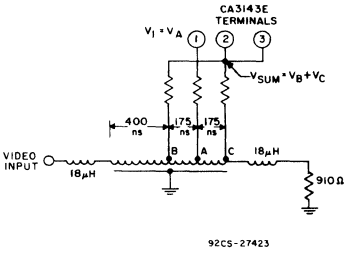
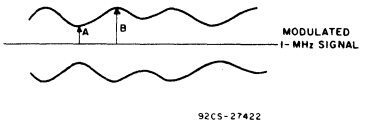


Fig.4 – Tapped delay line.



A = Amplitude of 50 kHz signal at deepest trough
B = Peak amplitude of 50 kHz signal
Downward Modulation = $\frac{B-A}{B}$

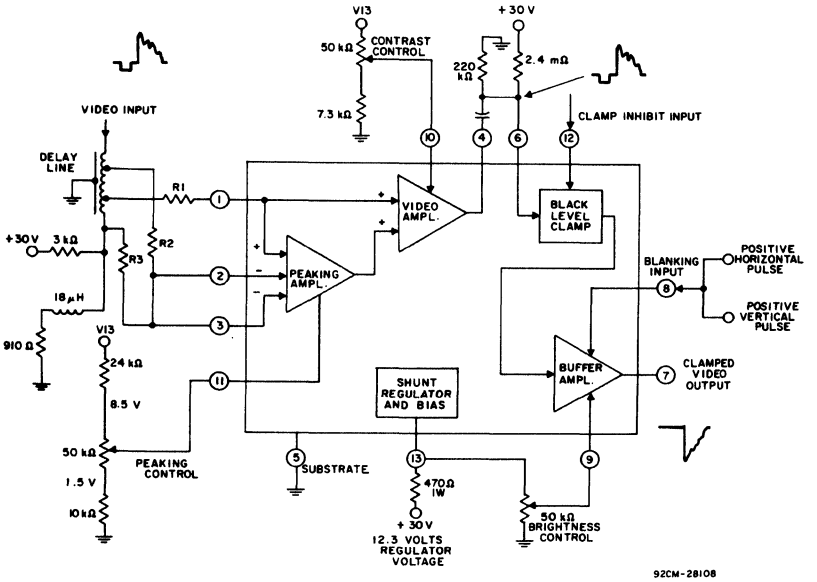


Fig. 1 – Functional block diagram.

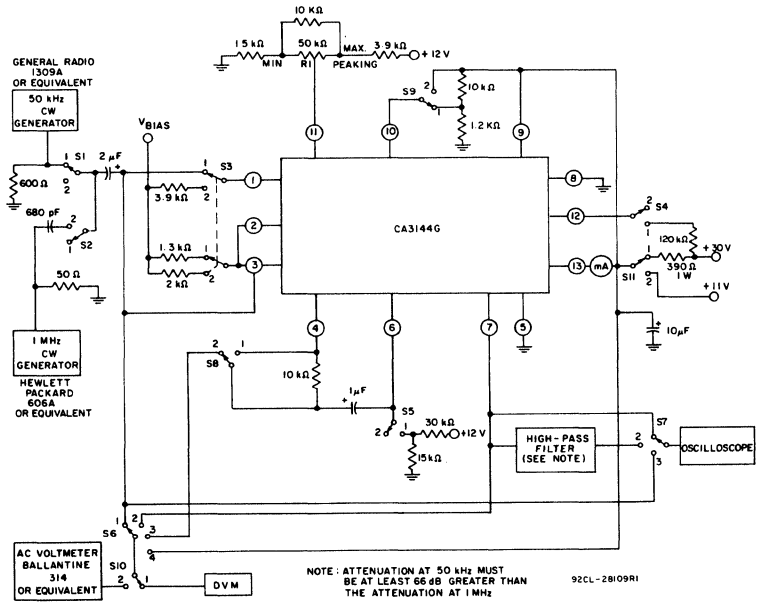


Fig. 2– Test circuit.

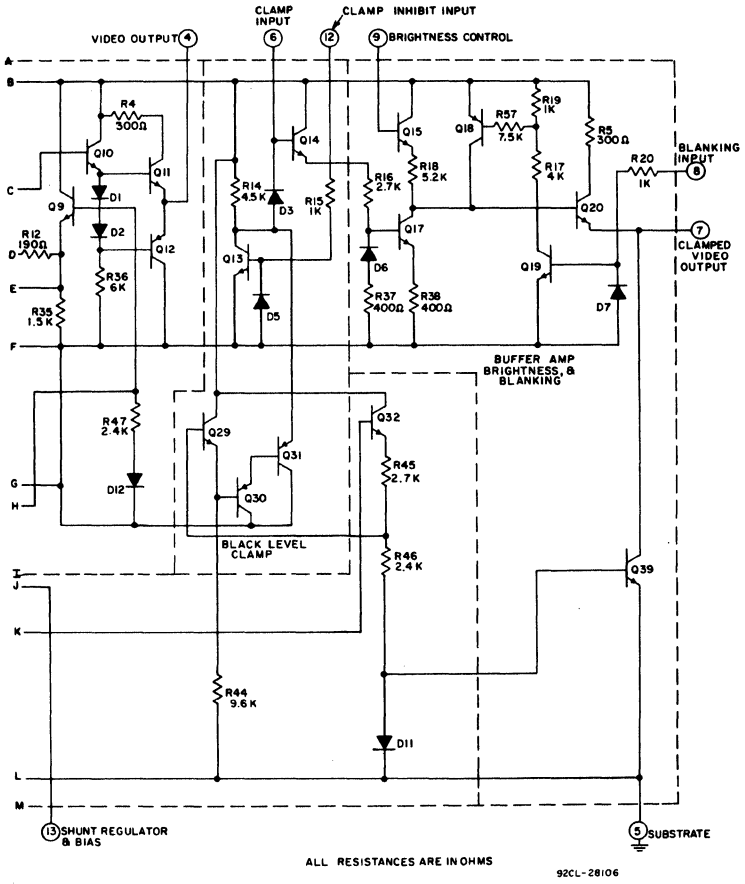


Fig. 3– Schematic diagram

minals 2 and 3 is attenuated thus, the peaking amplifier output consists of high-frequency video. The peaking control setting determines the amplitude of the peaking signal which is then fed to the video amplifier, where it is added to the video input signal and amplified. The setting of the peaking control does not substantially affect the dc quiescent voltage at terminal 4.

The low-impedance video amplifier output is at terminal 4. The signal is fed through an external coupling capacitor to terminal 6, the black-level clamp input. The action of the black-level clamp is such that it clamps to the black level rather than to the sync level. Refer to the circuit diagram in Fig. 1. Consider the situation where no signal is applied to terminal 12. Terminal 6 is biased through diode D3. The signal at terminal 6 will clamp its most negative excursion (sync pulse) to the anode voltage of D3. However, if a positive pulse is applied to terminal 12 during the sync interval, the anode of D3 is forced to ground due to saturation of Q13. The clamp is thus disabled, and terminal 6 will clamp to the next lower signal level, the black level.

The clamped video signal at terminal 6 is amplified and inverted at terminal 7. Blanking is accomplished by applying horizontal and vertical sync pulses to terminal 8. The pulses turn ON p-n-p transistor Q18 which shorts the base of transistor Q20 to the terminal 13 supply voltage. The brightness control function is accomplished by varying the voltage on terminal 9. The gain of the inverter stage remains constant, but the dc reference voltage follows the terminal 8 voltage. The contrast control function is accomplished by varying the voltage of terminal 10. Increasing the voltage on terminal 10 lowers the gain of the video amplifier. This reduction in gain does not substantially affect the dc quiescent voltage at terminal 4.

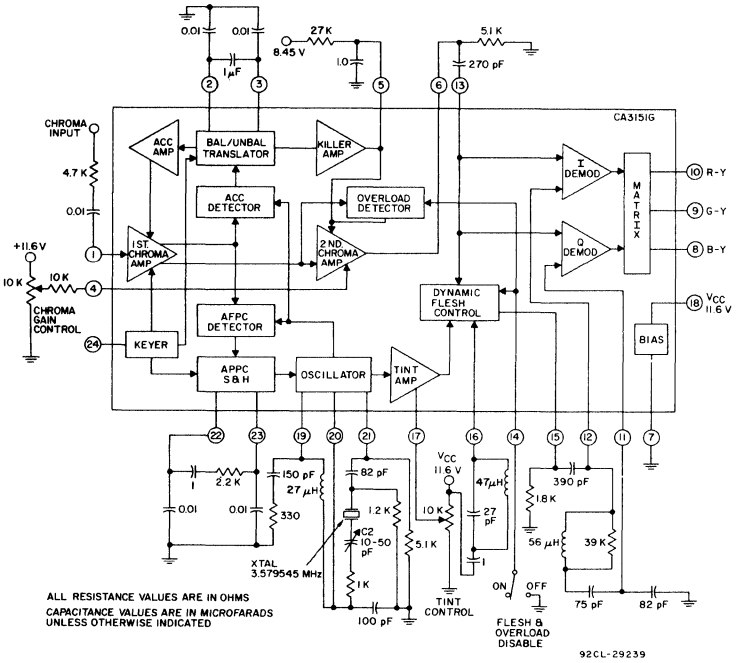


Fig. 1 – Functional diagram, static test circuit, and typical application circuit.

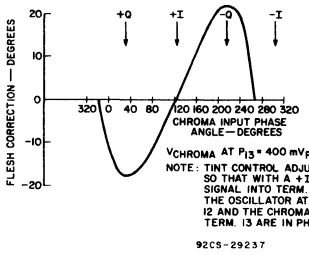
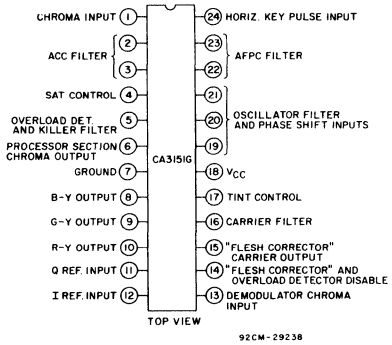


Fig. 2 – "Flesh" correction of oscillator phase angle as a function of chroma input phase angle.

TERMINAL DIAGRAM



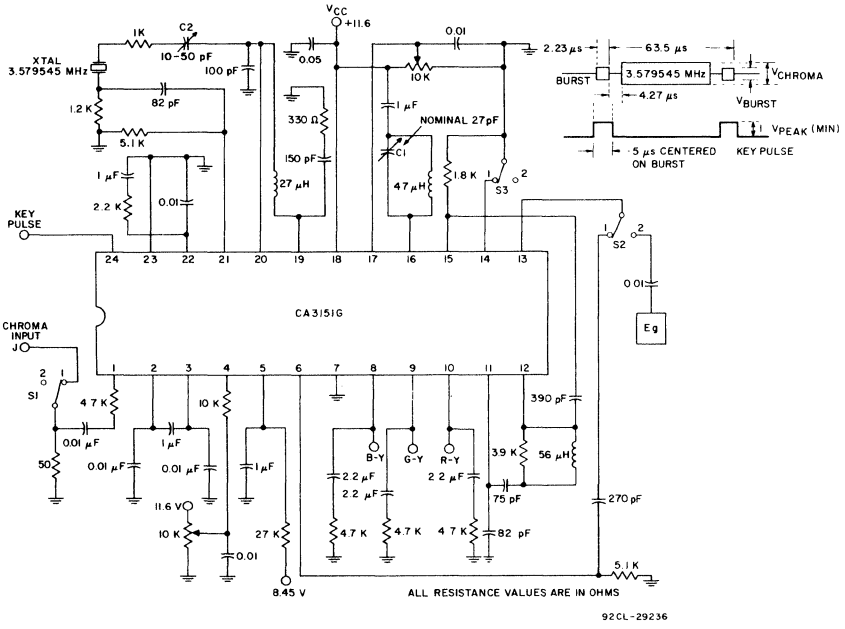


Fig. 3 – Dynamic test circuit.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- Between Terms. 15 and 4 . . . . . 16 V
- Between 470 Ω connected to Term. 12 and 4 . . . . . 35 V

DC SUPPLY CURRENT:
- At Term. 15 . . . . . 20 mA
- At Term. 12 . . . . . 30 mA

DEVICE DISSIPATION:
- Up to T_A = +55°C . . . . . 750 mW
- Above T_A = +55°C . . . . . Derate linearly at 7.9 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating . . . . . −40 to +85°C
- Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Operating Supply Voltage, V_{15}	See Note 1	12	14.2	V
Supply Current, I_{15}		3	15	mA
Shunt Regulator Voltage, V_{12}		10.9	13	V
Shunt Regulator Current, I_{12}	V_{12} = 10.5 V	6	20	mA
Tuner AGC High Voltage, V_{10}		18.5	21	V
Tuner AGC Low Voltage, V_{10}		0.3	1.3	V
AGC Current, I_2	Non-Keyed	80	500	μA
AGC Current (Peak), I_2	Keyed Source Current	0.7	3	mA
AGC Current (Peak), I_2	Keyed Sink Current	150	680	μA
Horizontal Key Input	Through 100 kΩ connected to Term. 1	25	35	V
Video Output High Voltage, V_{16}	At Zero Carrier	7	10	V
Video Output Low Voltage, V_{16}	At 30 mV Input	0.9	2	V
Sensitivity Voltage, V_{16}	At 400 μV Input	0.9	5	V
Noise		–	12	^{mV}(RMS)
Chroma	45.75 MHz, 10 mV; 42.17 MHz, 3 mV	0.7	1.6	V (RMS)
AFT Drive		35	85	^{mV}(RMS)
Distortion	50 kHz, 80% Modulated, Sync TIP Equiv. 30 ^{mV}(RMS)	–	10	%
Delay Voltage	Through 15kΩ connected to Term. 7. See note 2	0	V_{15}	V

Note 1: V_{15} MIN. should be at least 0.6 V above Terminal 12 potential. Lower voltage may cause some "white" compression.

Note 2: Zero voltage corresponds to maximum delay at signal input = 30 ^{mV} (RMS).

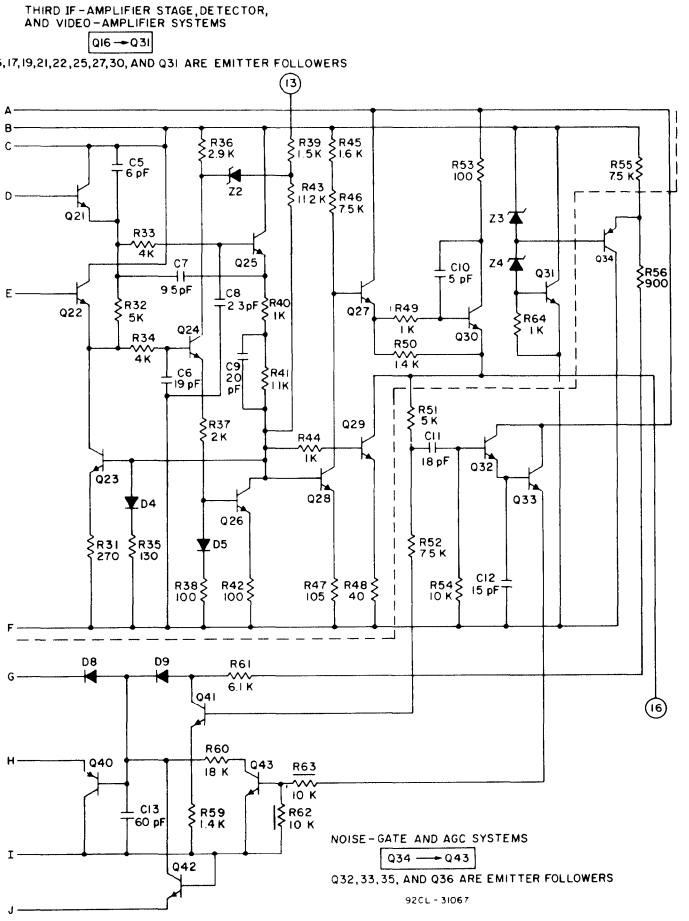


Fig. 2 – Schematic diagram for the CA3153G.

Q38, Q36, and Q35 to resistor R57 to form the charge current for the external agc filter capacitor at Terminal 2.

A constant-current discharge path for the capacitor at Terminal 2 is provided by current mirror components D7 and Q37 during the key-pulse duration. Thus the external agc filter capacitor is charged or discharged during the key-pulse interval only by the difference in current between the charge- and discharge currents. At the end of the key-pulse duration, C13 is discharged, and the charge and discharge current paths at Terminal 2 are turned off. Diode D8 provides a lower-gain agc path for turn-on during channel acquisition.

Noise-Gate System (See Fig. 3)

The circuit components, C11, R54, Q32, Q33, and Q43 perform the function of a statistical system to reduce agc gain during "spike" noise. The noise gate turns on for large amplitude fast signals and reduces the agc loop gain.

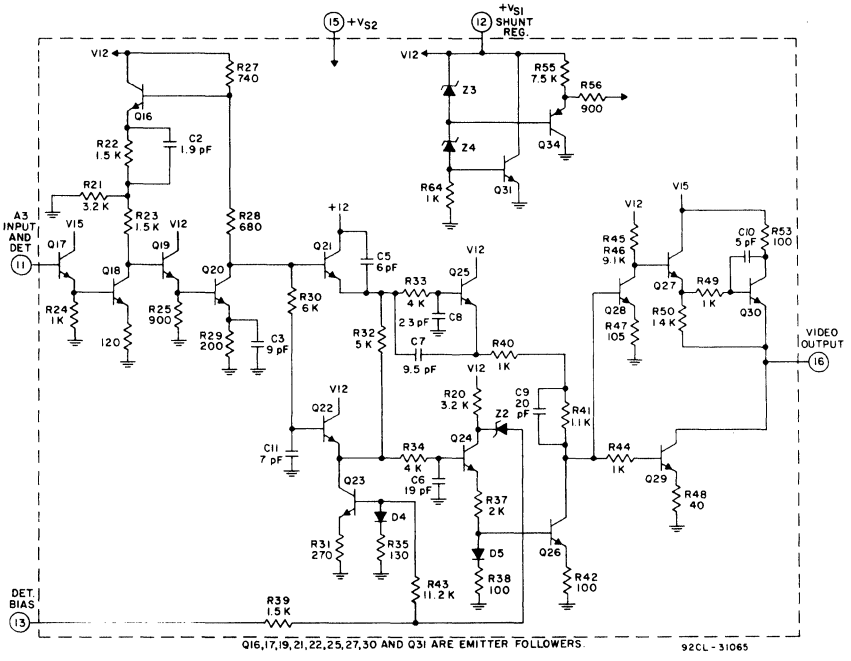


Fig. 5 – Third IF-amplifier stage, detector, and video-amplifier systems of CA3153G (Q16 → Q31).

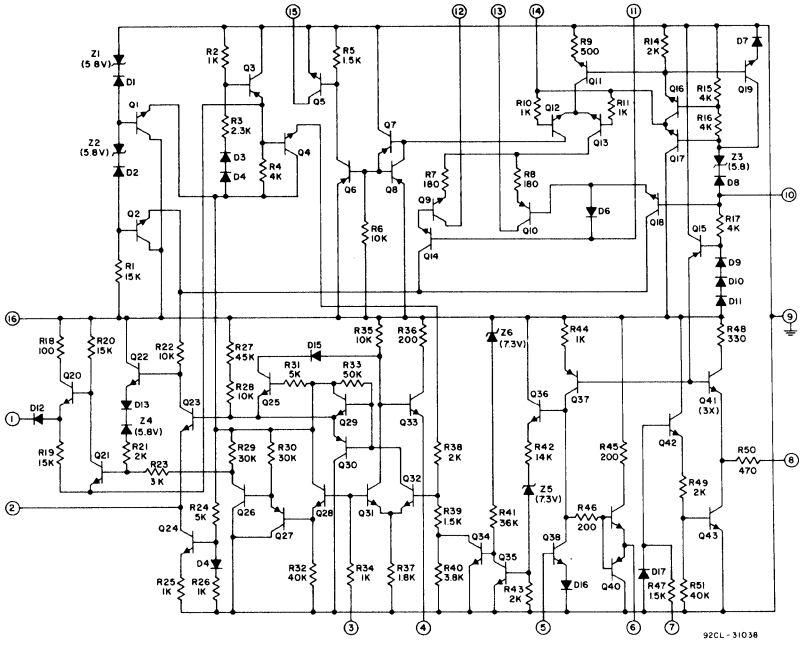


Fig. 3 – Schematic diagram of the CA3159G.

Circuit Description

The negative sync video input at terminal 3 is the detected video if. This video signal is buffered and V_{be} compensated by emitter-followers Q28, Q27, and Q26. The buffered video signal is applied between the base of Q21 and a temperature-stable 2-V reference. Q21 is normally in saturation, and the negative sync pulse imparts a positive swing to the base of Q20. Q20 is used as a peak rectifier driving a capacitor at terminal 1. The voltage at terminal 1 is the AGC control voltage that sets the if gain such that the sync pulses drop to just below the 2 V level, driving Q21 out of saturation.

The above description is for a normal video signal; the presence of noise pulses more negative than the sync tip level would lower the gain to that level, thus disturbing the picture. A gated noise-inversion threshold is provide at the base of Q32 to compensate for these noise pulses. The threshold is about 1.5 V during trace time, but is reduced to about 1 V during coincidence of the sync and flyback pulses. When the video signal is more negative than the noise threshold, Q32 conducts and pulls the base and emitter of Q30 low. Without noise, Q23 conducts 0.5 mA with its collector at 7 V, which holds Q22 in cutoff. Q29 has an emitter load provided by an external 1 kΩ resistor and a series capacitor: when its base is switched low, its collector switches high. The resulting flow of current in Q23 overrides the normal negative-going pulse in the direct signal path and holds Q21 in saturation.

The video input to terminal 3 also operates the sync channel, beginning with Q31. Because Q32 is normally cut off, Q31 acts as an amplifer with a moderate gain to its collector, and a positive sync signal appears at terminal 4. If the noise pulse is more negative than the noise threshold at the base of Q32, the base of Q30 is pulled down as discussed above. In addition to operating the AGC noise inverter, the Q30 current passes through Q25 to the amplifier load resistor, R35, and cancels the potentially positive pulse at that point.

The positive sync signal at terminal 4 is coupled through an RC network to terminal 5 for sync separation. In essence, the network permits Q38 to clamp the positive peaks, so the most positive part of the signal is amplified by Q38 while the rest is beyond cutoff. The separated sync, a negative pulse at the collector of Q38, follows two paths. First, the sync operates an output driver to terminal 6, which drives the outboard diode phase detector. Second, the negative pulse cuts off the current through Q36, which otherwise holds Q35 in saturation, thus enabling a current in R41 to turn Q34 on and thereby shift the noise threshold voltage.

Terminal 7 receives a positive flyback pulse that supplies R41 with the signal to complete the coincidence gate that alters the noise threshold when sync and flyback pulses are in phase. The buffered and clipped flyback pulse also turns Q43 on, which, in conjunction with an external integrating capacitor, forms a sawtooth waveform. This sawtooth (at flyback rate) is phase compared with the sync pulse that was separated from the video input.

The phase detector works against an internal bias point brought out to terminal 10, and the phase detector output applied to terminal 11 is slightly positive or negative relative to terminal 10. This voltage differential with terminal 10 determines the division of current between Q9 and Q10, which are part of the voltage controlled oscillator. The oscillator consists of the current source Q11, differential amplifier Q12 and Q13, and differential amplifier Q9 and Q10. The frequency is determined primarily by a series LC circuit connected between terminals 13 and 14 (terminals 12 and 13 have resistor loads to the positive supply). If the entire oscillator current passes through Q10 to terminal 13, the oscillator operates at the frequency at which the phase shift in the LC circuit is zero. If the current is sent through Q9 to terminal 12, however, it must go through an external capacitor between terminals 12 and 13 and then through the original LC circuit and the circuit is tuned differently. Intermediate proportions of current division will produce intermediate oscillator frequencies. The oscillator current output from Q12 provides base drive for the 31.5 kHz output at terminal 15.

ELECTRICAL CHARACTERISTICS At T_A = 25°C, V^+ = 5 VDC, V^- = 0 VDC; see Figs. 1 & 2

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current, I^+	Terms. (1+2), Fig. 1	30	60	90	mA
UHF Bandswitch Input Voltage, V_{BH}	High level	2.4	–		V
VHF Bandswitch Input Voltage, V_{BL}	Low level	–	–	0.8	V
UHF Bandswitch Input Current, I_{BH}	V_{BH} = 20 VDC, Fig. 1	–	–	0.5	mA
VHF Bandswitch Input Current, I_{BL}	V_{BL} = 0 VDC, Fig. 1	–	–	–1	mA
UHF Sensitivity Level Input Voltage, V_{IN}(U)	f_{IN} = 450 to 950 MHz, $f_{OUT} = f_{IN}/256$, Fig. 2	–	–	80	mVRMS
VHF Sensitivity Level Input Voltage, V_{IN}(V)	f_{IN} = 90 to 275 MHz, $f_{OUT} = f_{IN}/64$, Fig. 2	–	–	40	mVRMS
Output Voltage, V_O	Terms, 4 or 5, Fig. 2	0.65	1	–	V_{p-p}
Output Voltage Rise of Fall Time, t_r,t_f		–	70	–	ns

Operational Amplifier (See Fig. 2)
Electrical Characteristics at T_A = 25°C, $V^{\pm}$ = 32.5 V, V_{BS} = 18 V, Terms 4 & 5 grounded

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES	UNITS
Input Bias Voltage, V_{13}	I_{13} = 4 mA, Feedback = 1 MΩ	2.5	V_{DC}
Input Bias Voltage, V_{13}	I_{13} = 6 mA, Feedback = 1 MΩ	2.6	V_{DC}
Input Bias Voltage, V_{14}	I_{14} = 4 mA, Feedback = 1 MΩ	3.3	V_{DC}
Diode Voltage (term. 14 to term. 13)	I_{14} = 4 mA, Term. 13 = Reference	0.8	V_{DC}
Diode Voltage (term. 13 to term. 14)	I_{13} = 4 mA, Term. 14 = Reference	0.8	V_{DC}
Output Voltage Low, V_{OL}	I_{14} = 4 mA, Resistance between Terms. 1 and 12 = 10 kΩ	0.2	V_{DC}
Output Voltage High, V_{OH}	V_{14} = 0 V, I_{13} = 4 mA, Resistance between Terms. 1 and 12 = 10 kΩ	28	V_{DC}
Input Offset Voltage, V_{IO}	V_{13} = 0 V, Term. 1 connected to Term. 14	10	mV
Supply Current, I^+	V_4 = 1 V, Feedback (Terms. 1 to 14) = 1 MΩ	14	mA
Output Sink Current, I_{OL}	I_{14} = 4 mA, V_1 = 32.5 V	25	mA
Output Source Current, I_{OH}	I_{13} = 4 mA, V_1 = V_{14} = 0V	−15	mA
Input Bias Current, I_{IB} (term. 14)	V_{13} = 0 V, Term. 1 connected to Term. 14	0.5	nA
Common-Mode Rejection Ration, CMRR		65	dB
Power Supply Rejection Ratio, PSRR		75	dB
Open-Loop Voltage Gain, A_{OL}		80	dB

Band-Select Switch (See Fig. 3)
Electrical Characteristics at T_A = 25°C, V^+ = 32.5 V, V_{BS} = 18 V, Terms. 4 & 5 grounded
Terms. 6, 7, 9 = 100 kΩ to ground

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES	UNITS
Logic Inputs "A" & "B" Sink Current		100	μA
Logic Inputs "A" & "B" Source Current	I_9 = −90 mA, V_{10} = V_{11} = 2.4 V	−5	μA
Output Leakage Current, Terms. 6, 7, 9		2	μA
Output Saturation Voltage: Term. 9	I_9 = −90 mA, V_{10} = V_{11} = 2.4 V	0.6	V
Term. 9	I_9 = −60 mA, V_{10} = V_{11} = 24 V	0.3	V
Term. 7	I_7 = −90 mA, V_{10} = 0 V, V_{11} = 24 V	0.6	V
Term. 7	I_7 = −60 mA, V_{10} = 0 V, V_{11} = 2.4 V	0.3	V
Term. 6	I_6 = −90 mA, V_{10} = 2.4 V, V_{11} = 0 V	0.6	V
Term. 6	I_6 = −60 mA, V_{10} = 24 V, V_{11} = 0 V	0.3	V

Preliminary Data

CA3168E

2-Digit BCD-to-7-Segment Decoder/Driver

For Common-Anode LED Displays

The RCA-CA3168E is a monolithic integrated circuit intended for 2-digit display such as "numbers" for TV and "CB" channel selection, and other 0-99 numerical or counting for consumer or industrial indicator applications. It consists of two independent BCD-to-7-segment decoder/drivers. Two sets of BCD inputs are buffered with p-n-p differential amplifier stages internally referenced to 1.7 V. Each of the eight input terminals draws less than 15 μA and is provided with an internal protection circuit.

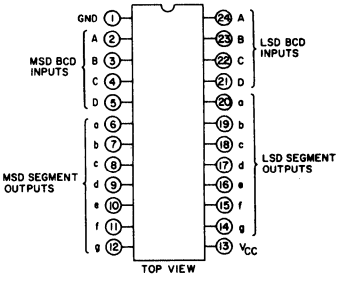
Decoding is accomplished with I^2L ROM's. The fourteen output terminals are buffered with Darlington pairs driving common-emitter output transistors. Each output is capable of sinking 25 mA for an LED common-anode display device. The supply-voltage range (V_{CC}) is intended to be 4.5 V to 6 V. The output voltage (V_O) must not exceed 12 V, which provides for a wide range of common-anode voltage sources.

The CA3168E is supplied in the 24-lead dual-in-line plastic package.

Features:

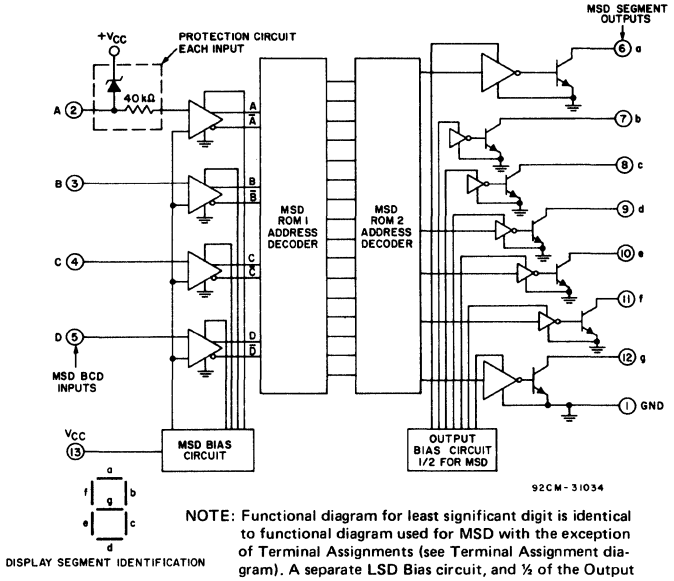
- **Separate BCD inputs and segment outputs for each digit**
- **Input loading less than 15 μA**
- **I^2L logic with buffered inputs and outputs**
- **Internal input overrange protection circuit**
- **5-V supply operation**
- **Internal biasing circuits**
- **Output drive capability of 25 mA per segment**
- **Open collector outputs drive indicators directly**

CA3168E TERMINAL ASSIGNMENT



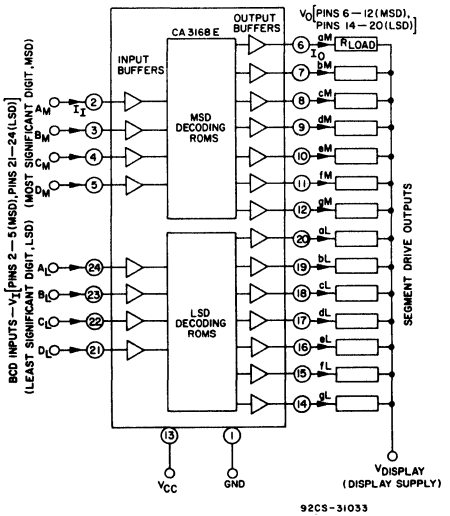
MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY-VOLTAGE, V_{CC}	6 V
INPUT-VOLTAGE (MIN./MAX.)	$-0.3/V_{CC}$ V
INPUT CURRENT (PROTECTION CIRCUIT)	±10 mA
OUTPUT VOLTAGE, V_O	12 V
OUTPUT SEGMENT CURRENT, $I_{DISPLAY}$	25 mA
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +70°C
Storage	−55 to +150°C
POWER DISSIPATION:	
Up to +70°C	400 mW
Above +70°C	derate linearly at 8.7 mW/°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C



NOTE: Functional diagram for least significant digit is identical to functional diagram used for MSD with the exception of Terminal Assignments (see Terminal Assignment diagram). A separate LSD Bias circuit, and ½ of the Output Bias Circuit is used for LSD.

Fig. 1 – Functional diagram for Most Significant Digit (MSD).



NOTE: See truth table for test sequence of input/output logic tests and Minimum $R_{LOAD} = \frac{V_{DISPLAY} - V_{OL}}{\text{Max. } I_{DISPLAY}}$ For each of the 14 segment drive output terminals. (LED is not used in test circuit)

Fig. 2 – Test circuit.

TV Chroma System

"G" Suffix Type-Hermetic Gold-CHIP in Dual-In-Line Plastic Package

The RCA-CA3170G is a monolithic silicon integrated circuit that performs the functions of subcarrier regeneration, ACC and APC detection, and tint control in color television receivers. It is designed to function compatibly with the CA3121E TV Chroma Amplifier/Demodulator in a 2-package chroma system.

The CA3170G is a TV Chroma System of advanced design that incorporates all the features of the CA3070E but with the added advantage of the modified Hue Control Characteristic. With the CA3170G, the designer can provide a front panel hue control that functions linearly over its entire range, a particularly desirable consumer feature.

Features:

- **Voltage-controlled oscillator**
- **Keyed APC and ACC detectors**
- **DC hue control**
- **Shunt regulator**

MAXIMUM RATINGS, *Absolute-Maximum:*

DEVICE DISSIPATION:*
- Up to $T_A = 55^\circ C$ . . . . . 750 mW
- Above $T_A = 55^\circ C$ . . . . . derate linearly 7.9 mW/°C

AMBIENT–TEMPERATURE RANGE:
- Operating . . . . . −40 to +85°C
- Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During soldering):
- At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max. . . . . +265°C

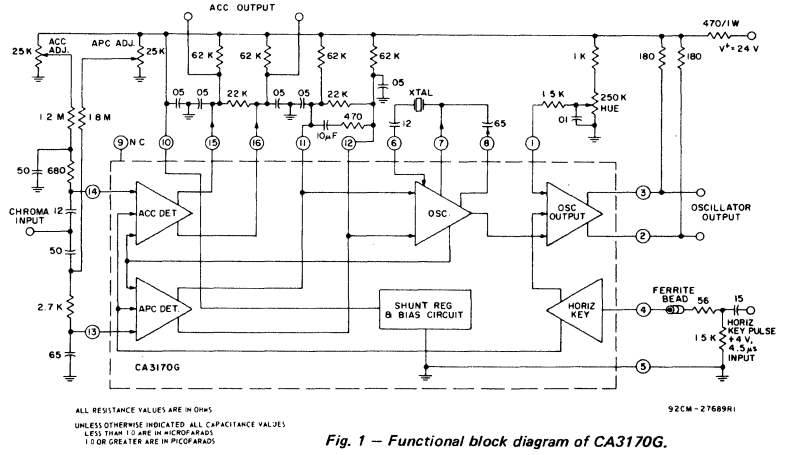


Fig. 1 – Functional block diagram of CA3170G.

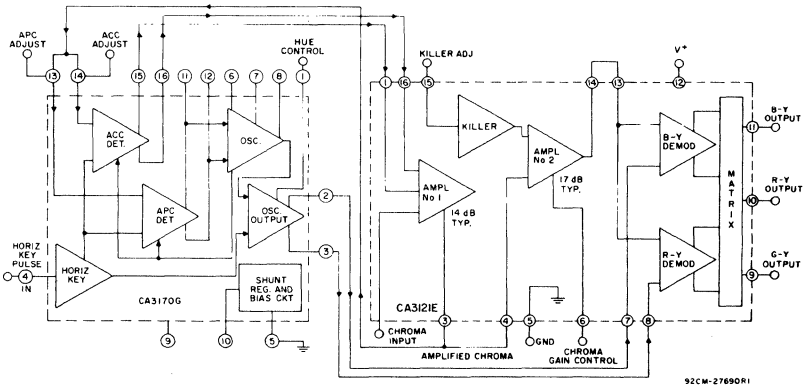


Fig. 2 – Simplified functional diagram of a two-package TV chroma system utilizing the CA3170G and CA3121E.

The CA3170G is supplied in the 16-lead dual-in-line plastic package with a hermetic Gold-CHIP (G suffix). The chips used in the hermetic Gold-CHIP plastic packages are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multilayered, highly corrosion-resistant, terminal-connection system of unique design is employed.

CIRCUIT DESCRIPTION

The CA3170G is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3121E is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval. The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 16 of the CA3121E. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator. To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue

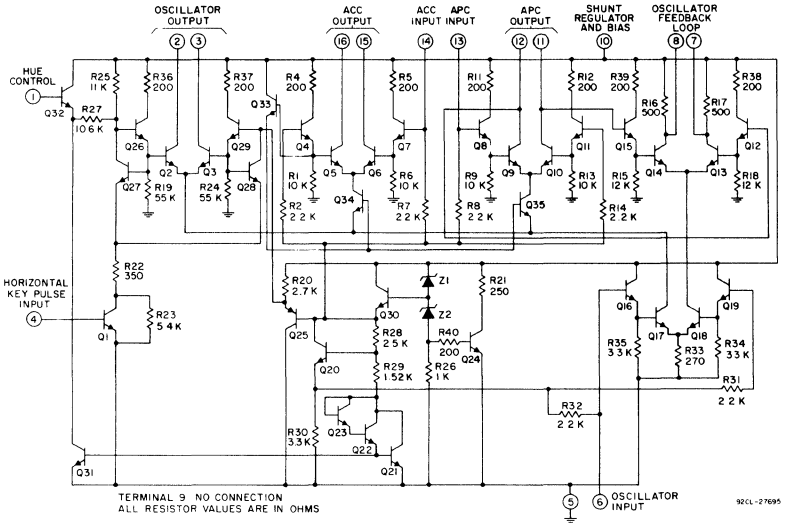


Fig. 6 – Schematic diagram of the CA3170G.

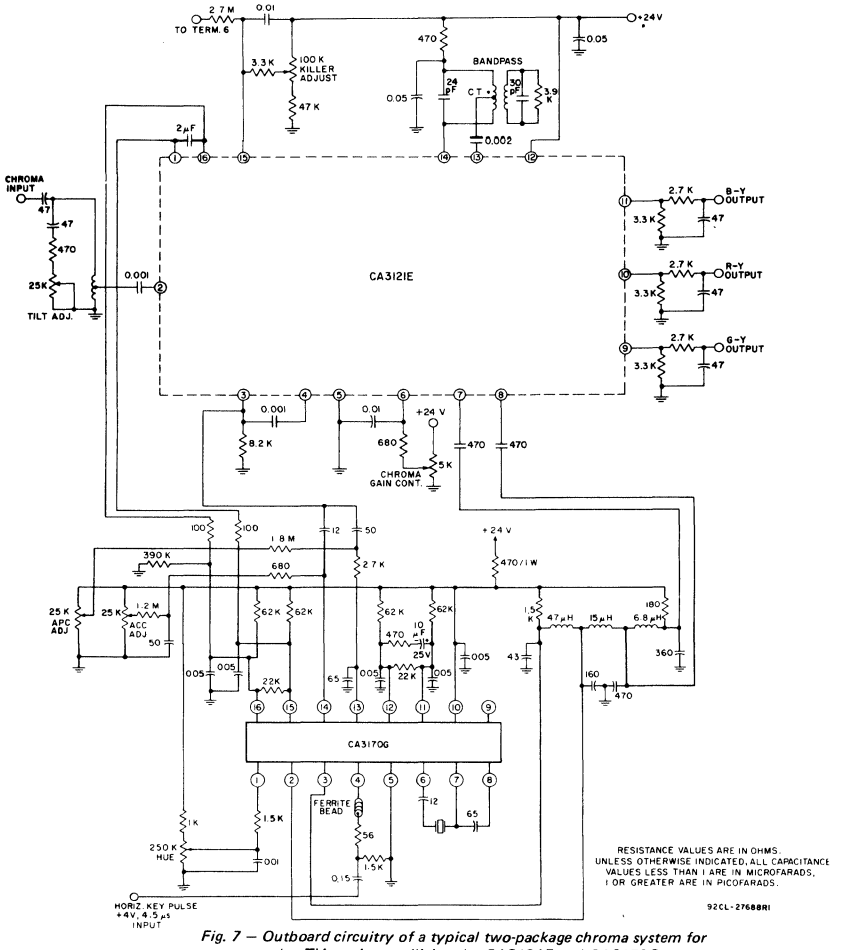


Fig. 7 – Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3121E and CA3170G.

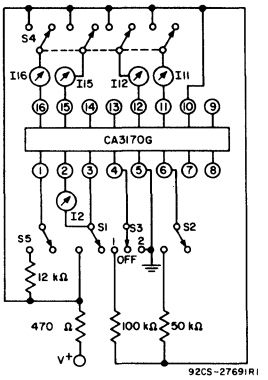


Fig. 8 – Static characteristics test circuit

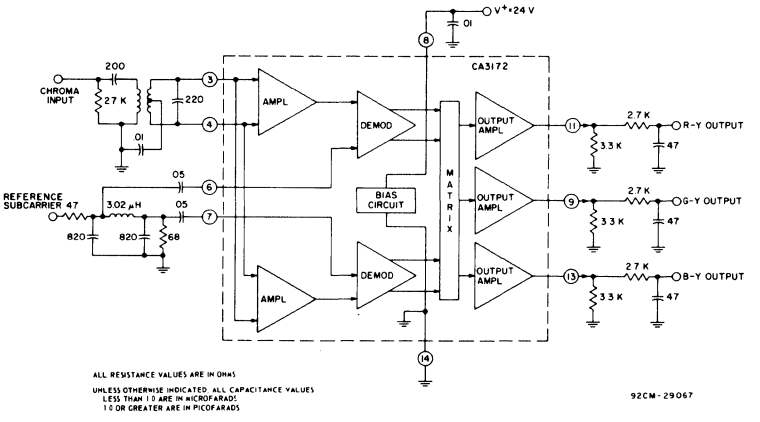


Fig. 1 – Functional diagram of RCA-CA3172.

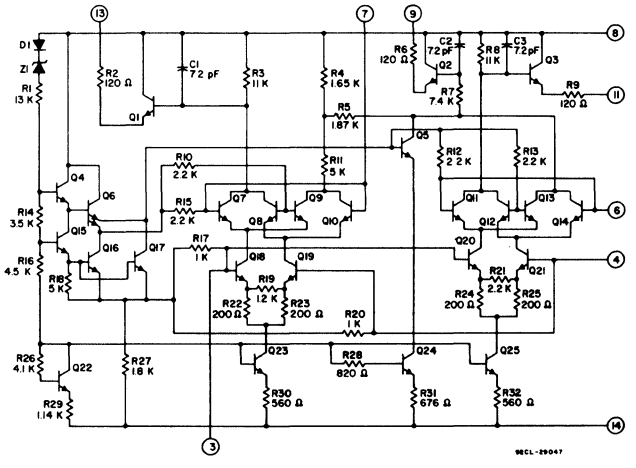


Fig. 2 – Schematic diagram for CA3172.

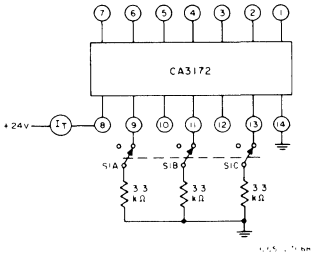


Fig. 3 – Static characteristics test circuit.

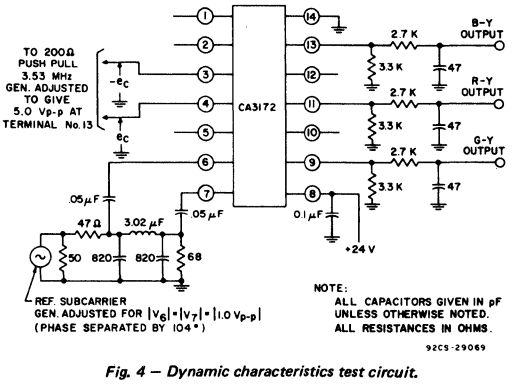
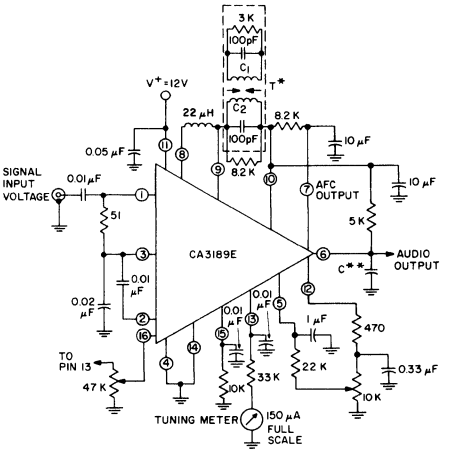


Fig. 4 – Dynamic characteristics test circuit.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V^+ = 12 Volts

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
				Circuit or Fig. No.	Min.	Typ.	Max.	
Static (DC) Characteristics								
Quiescent Circuit Current	I_{11}	No signal input, Non muted		2,6	20	31	40	mA
DC Voltages: Terminal 1 (IF Input)	V_1				1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2				1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3				1.2	1.9	2.4	V
Terminal 15 (RF AGC)	V_{15}				7.5	9.5	11	V
Terminal 10 (DC Reference)	V_{10}				5	5.6	6	V
Dynamic Characteristics								
Input Limiting Voltage (−3 dB point)	V_I(lim)	V_{IN} = 0.1 V, AM Mod. = 30%	f_O = 10.7 MHz,	2,6	–	12	25	μV
AM Rejection (Term. 6)	AMR				45	55	–	dB
Recovered AF Voltage (Term. 6)	V_O(AF)				325	500	650	mV
Total Harmonic Distortion:* Single Tuned (Term. 6)	THD	V_{IN} = 0.1 V	$f_{mod.}$ = 400 Hz,	6	–	0.5	1	%
Double Tuned (Term. 6)	THD		Deviation ±75 kHz	2	–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)	S + N/N			2,6	65	72	–	dB
Deviation Mute Frequency	$f_{DEV.}$		$f_{mod.}$ = 0	4,6,7	–	±40	–	kHz
RF AGC Threshold	V_{16}			2,6	–	1.25	–	V
On Channel Step	V_{12}	V_{IN} = 0.1 V	$f_{DEV.}$ < ±40 kHz	6	–	0	–	V
			$f_{DEV.}$ > ±40 kHz		–	5.6	–	

*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.



ALL RESISTANCE VALUES ARE IN OHMS

*T: PRI. – Q_O(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20 T OF 34¢ ON 7/32" DIA. FORM

SEC. – Q_O(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20 T OF 34¢ ON 7/32" DIA. FORM

kQ (PER CENT OF CRITICAL COUPLING) ≅ 70 %

(ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV

ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT

"E" TYPE SLUGS, SPACING 4 mm

**C = 0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)

= 0.015 μF FOR 75 μs DEEMPHASIS (USA) 92CM-29954

Fig. 2 – Test circuit for CA3189E using a double-tuned detector coil.

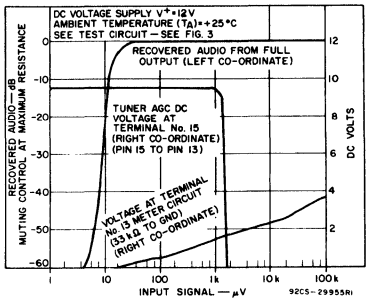


Fig. 3 – Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

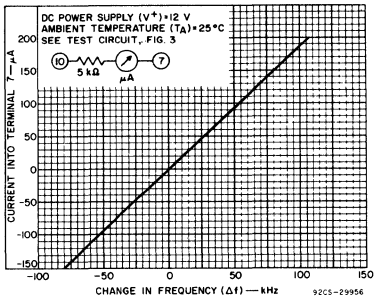


Fig. 4 – AFC characteristics (current at Term. 7 as a function of change in frequency).

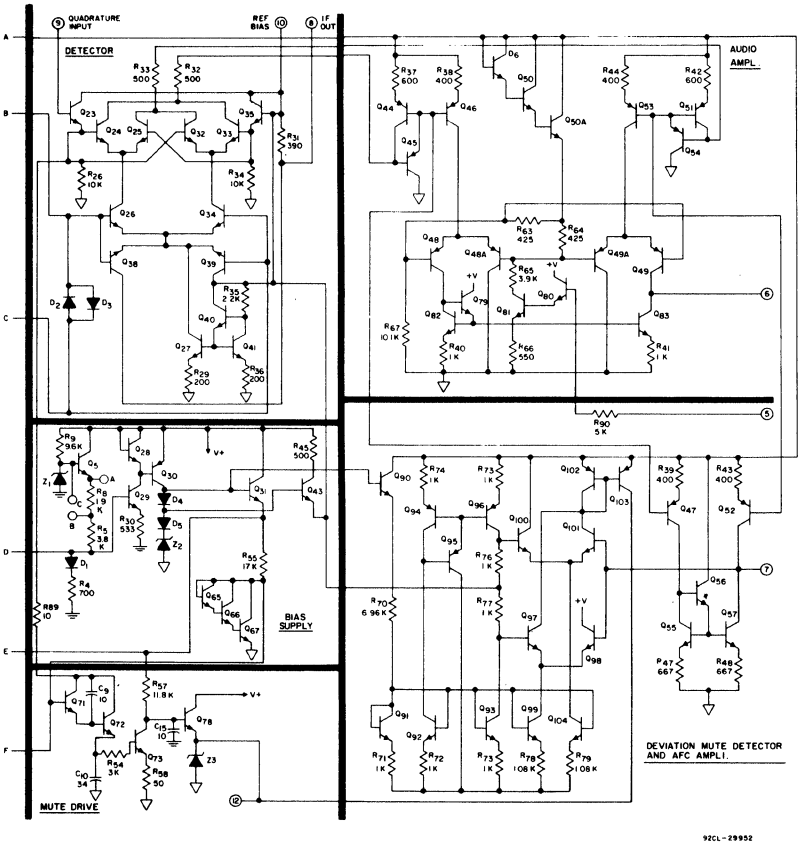
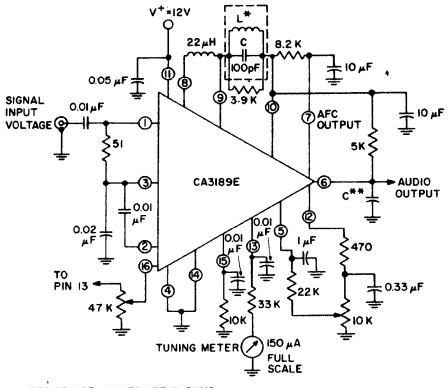


Fig. 5 — Schematic diagram of the CA3189E



ALL RESISTANCE VALUES ARE IN OHMS

*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O(UNLOADED)≅75 (TOKO No. KACS K586HM OR EQUIVALENT)

**C = 0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)
= 0.015 μF FOR 75 μs DEEMPHASIS (USA)

92CM-29953

Fig. 6 — Test circuit for CA3189E using a single-tuned detector coil.

TV Chroma Amplifier/ Demodulator

Provides Complete System for Processing Chroma When Used with RCA-CA3070 or CA3170 "G" Suffix Type-Hermetic Gold-CHIP in Dual-In-Line Plastic Package

Features:

- **Excellent linearity in dc chroma gain-controlled circuit**
- **Improved filtering resulting in reduced 7.2-MHz output from the color demodulators**
- **Current limiting for short-circuit protection**
- **Good tolerance to B+ supply variations**
- **Good temperature coefficient stability**
- **Gold-CHIP for increased reliability**

The RCA-CA3221G is a monolithic silicon integrated circuit chroma amplifier/demodulator with ACC, saturation control, and killer control for use in NTSC color TV receivers. It is designed to function compatibly with the CA3070 or CA3170 in a 2-package chroma system. The CA3221G is functionally identical to the industry standard CA3121, but has a modified saturation control as well as a modified color difference matrix.

The CA3221G is supplied in the 16-lead dual-in-line plastic package with a hermetic Gold-CHIP (G suffix). The transistor chips used in the hermetic Gold-CHIP plastic packages are of the sealed-junction type designed to provide protection against the deteriorating effects of humidity and other surface contaminants without the need for a hermetic package enclosure. The semiconductor junctions are sealed by utilizing a silicon nitride passivation layer. A multilayered, highly corrosion-resistant, terminal-connection system of unique design is employed.

MAXIMUM RATINGS at $T_A = 25°C$

Supply Voltage	30 V
Device Dissipation:	
Up to $T_A = 55°C$	1 W
Above $T_A = 55°C$	derate linearly 10.5 mW/°C
Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (During Soldering)	
At distance 1/16" ±1/32" (1.59 ±0.79 mm) from case for 10 s max.	+265°C

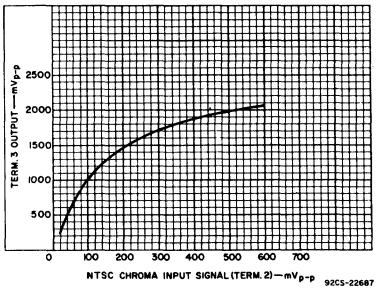


Fig. 2 – Typical ACC plot for the CA3221G when used with the CA3070.

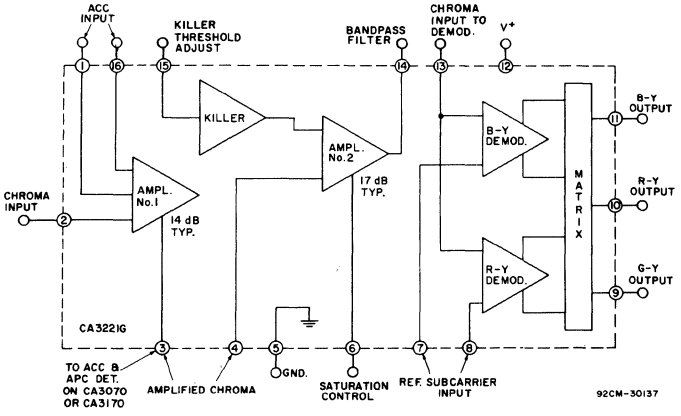


Fig. 1 – Functional block diagram of the CA3221G.

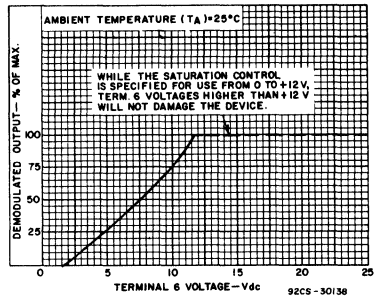


Fig. 3 – Saturation control characteristic.

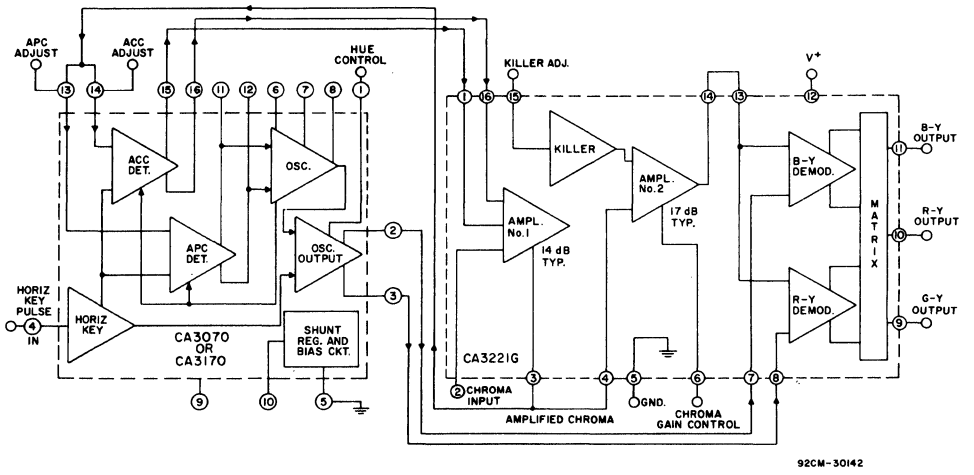


Fig. 4 — Simplified functional diagram of a two-package TV chroma system utilizing the CA3221G and CA3070 or CA3170.

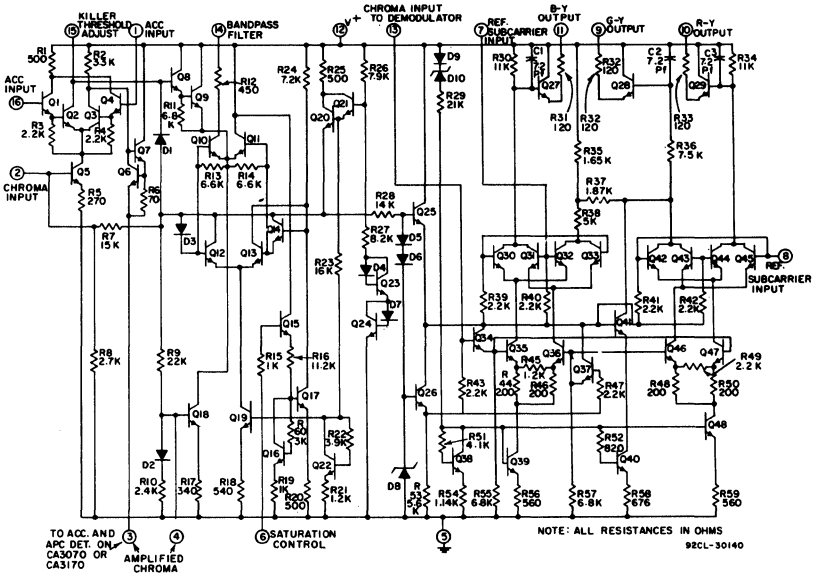
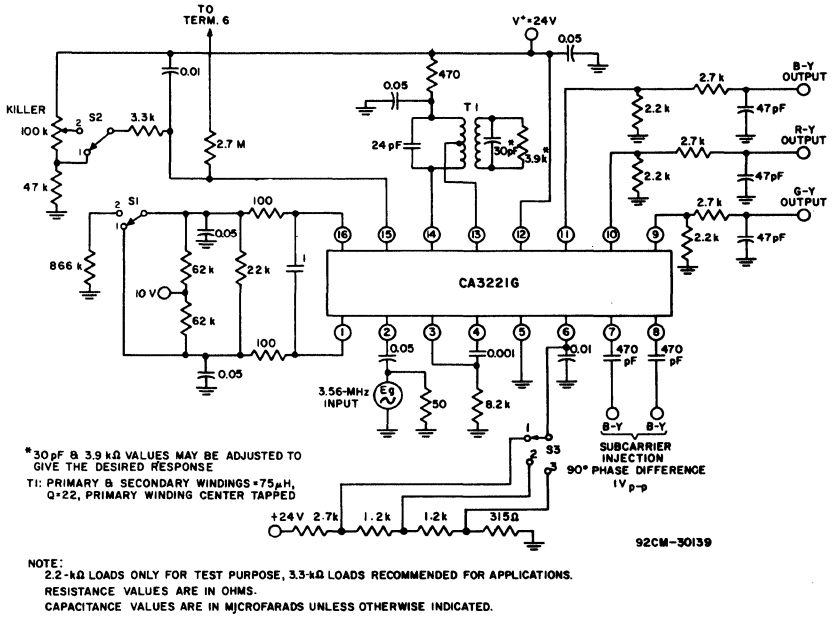


Fig. 5 — Schematic diagram of CA3221G.



NOTE:
2.2-kΩ LOADS ONLY FOR TEST PURPOSE, 3.3-kΩ LOADS RECOMMENDED FOR APPLICATIONS.
RESISTANCE VALUES ARE IN OHMS.
CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE INDICATED.

Fig. 7 – Typical characteristics test circuit for the CA3221G.

MOS Field-Effect Transistors
Technical Data

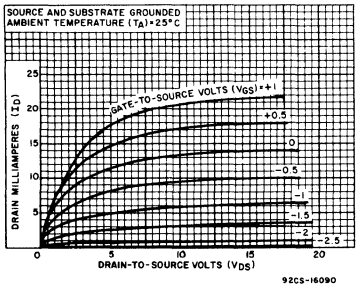


Fig. 4 - Drain current vs. drain-to-source voltage

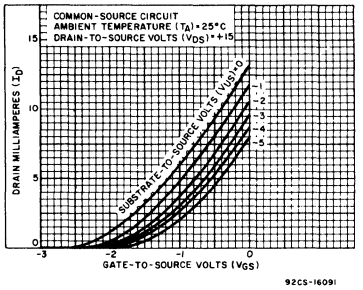


Fig. 5 - Drain current vs. gate-to-source voltage (V_{GS})

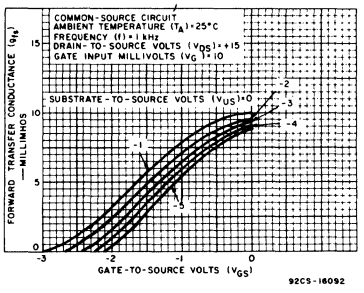


Fig. 6 - Forward transconductance vs. gate bias voltage

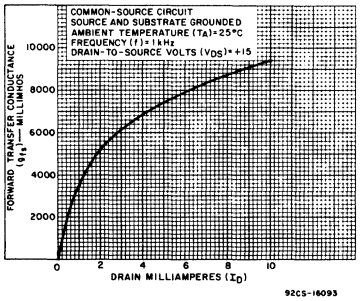


Fig. 7 - Forward transconductance vs. drain current

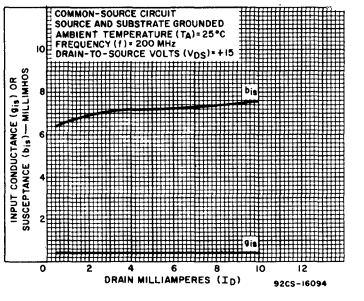


Fig. 8 - Input admittance vs. drain current

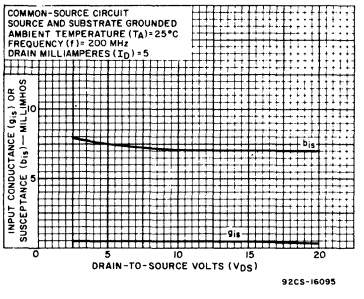


Fig. 9 - Input admittance vs. drain-to-source voltage

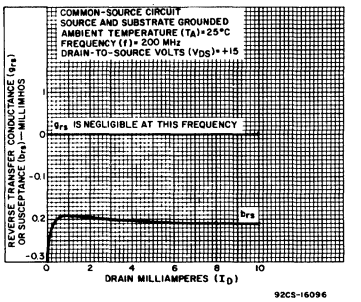


Fig. 10 - Reverse transadmittance vs. drain current

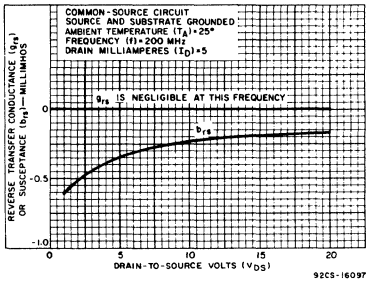


Fig. 11 - Reverse transadmittance vs. drain-to-source voltage

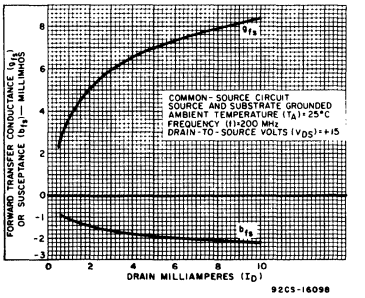


Fig. 12 - Forward transadmittance vs. drain current

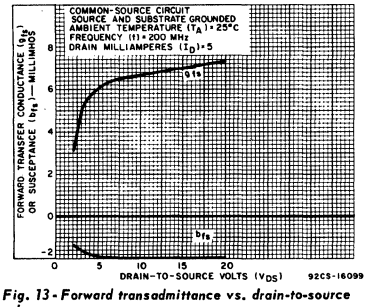


Fig. 13 - Forward transadmittance vs. drain-to-source voltage

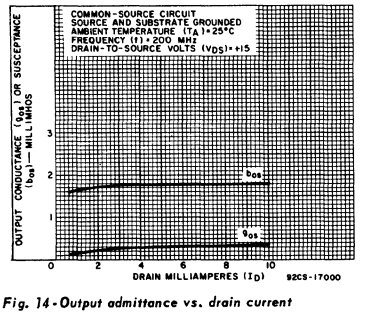


Fig. 14 - Output admittance vs. drain current

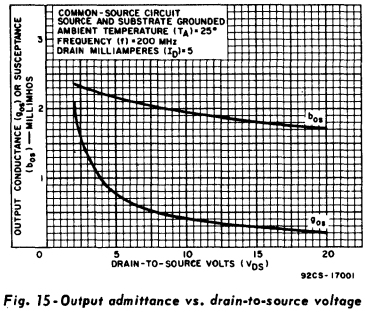


Fig. 15 - Output admittance vs. drain-to-source voltage

SILICON MOS TRANSISTOR

N-Channel Depletion Type

For Audio, Video, and RF Amplifier Applications in Communications, Instrumentation and Control Circuits

RCA 3N139 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is a general purpose transistor especially suited for audio, video, and rf applications, and for wide-band amplifier designs. The insulated gate provides a very high input resistance (10^{14} Ω typ.) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N139 also has a high transconductance, a low value of input capacitance (3 pF typ.), and a very low feedback capacitance (0.19 pF typ.).

The 3N139 is hermetically sealed in the standard 4-lead JEDEC TO-72 package.

Maximum Ratings, *Absolute-Maximum Values:*

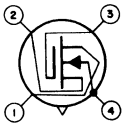
DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+35 max. V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+35, -0.3 max. V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+35, -0.3 max. V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	±10 max. V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max. V
PEAK VOLTAGE, GATE-TO-ALL OTHER TERMINALS; V_{GS}, V_{GD}, V_{GB}, non-repetitive	±42 max. V
DRAIN CURRENT, I_D	50 max. mA
TRANSISTOR DISSIPATION, P_T:	
At ambient temperatures up to 25°C	330 mW
above 25°C	Derate linearly at 2.2 mW/°C
AMBIENT TEMPERATURE RANGE:	
Storage	-65 to +175 °C
Operating	-65 to +175 °C
LEAD TEMPERATURE (During Soldering):	
At distance not closer than 1/32 inch to seating surface for 10 seconds max.	265 max. °C

* Metal-Oxide-Semiconductor

FEATURES

- high input resistance $R_{GS} = 10^{14}$ Ω typ.
- low input capacitance $C_{iss} = 3$ pF typ.
- low feed back capacitance $C_{rss} = 0.2$ pF typ.
- low gate leakage current $I_{GSS} = 0.1$ nA typ.
- high drain-to-source voltage: +35 max. V

TERMINAL ARRANGEMENT



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

ELECTRICAL CHARACTERISTICS, at T_A = 25° C Unless Otherwise Specified. Bulk (Substrate) Connected to Source

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS			UNITS
		FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC GATE-TO-SOURCE VOLTAGE V_{GS}	DC DRAIN CURRENT I_D	Min.	Typ.	Max.	
		MHz	V	V	mA				
Drain-to-Source Cutoff Current	$I_{D(OFF)}$		15	-8		—	—	50	μA
Zero-Bias Drain Current*	I_{DSS}		15	0		5	15	25	mA
Gate Reverse Current	I_{GSS}	T_A = 25°C	0	±10		—	—	1	nA
		T_A = 100°C	0	±10		—	—	100	nA
Gate-to-Source Cutoff Voltage	$V_{GS(OFF)}$		15		0.05	-2	-4	-6	V
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15		5	0.05	0.2	0.4	pF
Input Resistance	r_{is}	100	15		5		12	—	kΩ
Input Capacitance	C_{iss}	100	15		5	—	3	10	pF
Output Resistance	r_{os}	100	15		5		6	—	kΩ
Output Capacitance	C_{oss}	100	15		5	—	1.4	—	pF
Forward Transconductance	g_{fs}	1 kHz	15		5		5	—	mmho

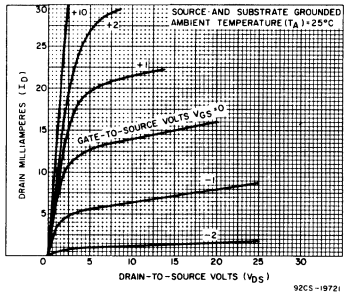


Fig. 1 – Drain Current vs Drain Voltage

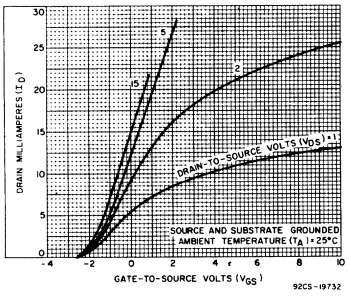


Fig. 2 – Drain Current vs Gate-to-Source Voltage

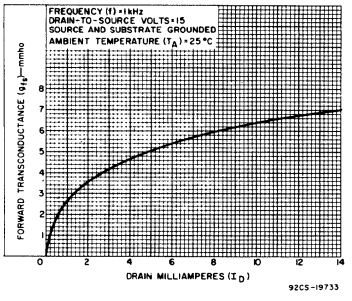


Fig. 3 – 1 kHz forward transconductance vs drain current

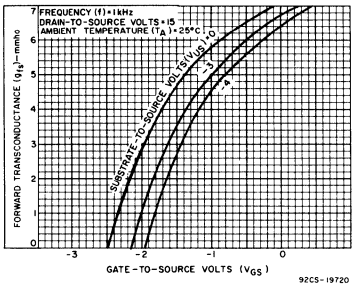
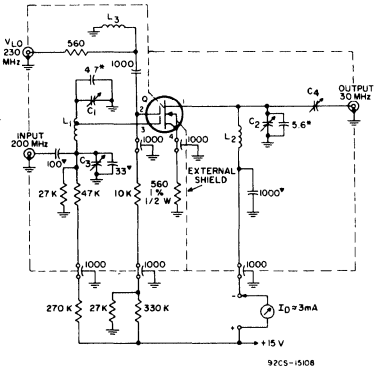


Fig. 4 – 1 KHz forward transconductance vs gate-to-source voltage



Q = 3N141.

▼ Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1, C_2: 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.

C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.

L_1: 5 turns silver-plated 0.02" thick, 0.07"±0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding.

L_2: Ohmite Z-144 RF choke or equivalent.

L_3: J.W. Miller Co. #4580 0.1 μH RF choke or equivalent.

Note: If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

Fig.2 - Conversion power gain test circuit for type 3N141.

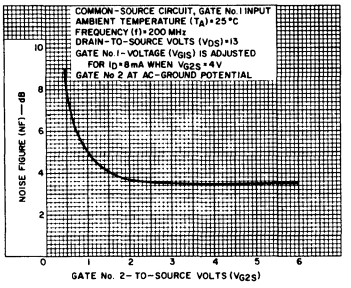


Fig.3 - NF vs V_{G2S}.

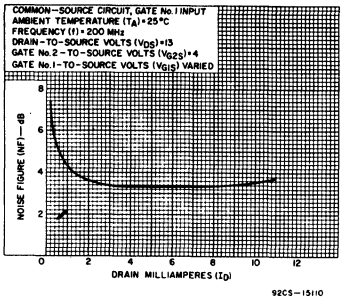


Fig.4 - NF vs I_D.

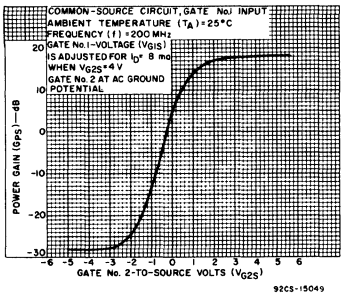


Fig.5 - G_{PS} vs V_{G2S} (For 3N140).

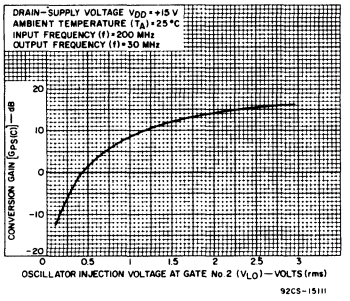


Fig.6 - $G_{PS(C)}$ vs V_{LO} (For 3N141).

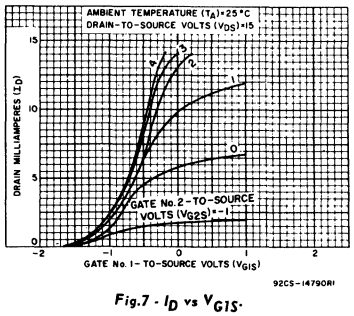


Fig.7 - I_D vs V_{G1S}.

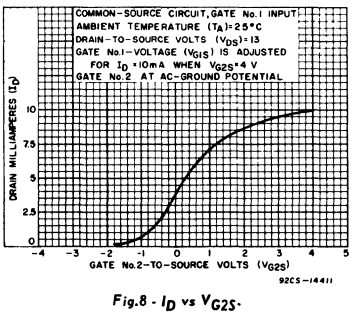


Fig.8 - I_D vs V_{G2S}.

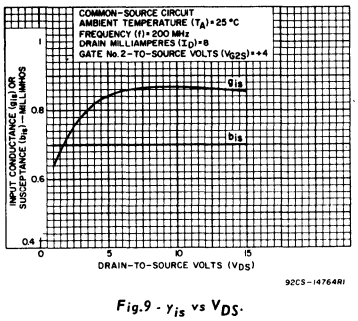


Fig.9 - y_{is} vs V_{DS}.

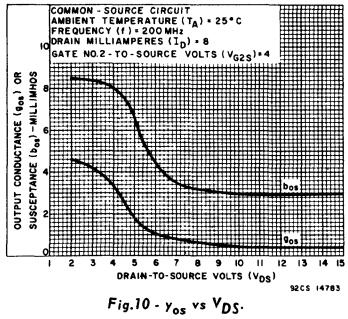


Fig.10 - y_{os} vs V_{DS}.

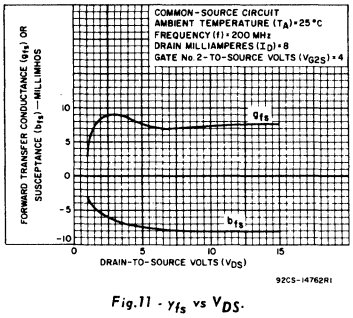


Fig.11 - y_{fs} vs V_{DS}.

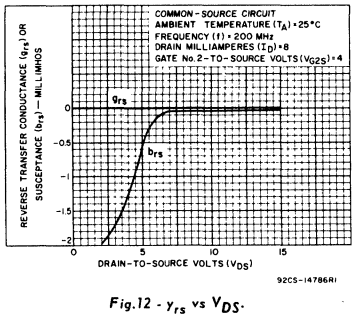


Fig.12 - y_{rs} vs V_{DS}.

Silicon MOS Transistor

N-Channel Depletion Type

For Industrial and Military Applications to 175 MHz

The 3N142 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type utilizing the MOS■ construction.

The 3N142 is intended primarily for use as the rf amplifier in FM receivers and general amplifier applications at frequencies up to 175 MHz.

The wide dynamic range of the 3N142 reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

■ Metal-Oxide-Semiconductor

Applications

- **RF amplifier, Mixer, and Oscillator in:**
  CB and Mobile Communication Receivers
  Aircraft and Marine Receivers
  CATV and MATV Equipment
- **Industrial Control Circuits**
- **Variable Attenuators**
- **Current Limiters**
- **Instrumentation Equipment**
- **High-Impedance Timing Circuits**

Maximum Ratings, Absolute-Maximum Values at T_A = 25° C

*DRAIN-TO-SOURCE VOLTAGE, V_{DS}	±20	V
*DRAIN-TO-GATE VOLTAGE, V_{DG}	±20	V
*GATE-TO-SOURCE VOLTAGE, V_{GS}:		
Continuous	+1 to −8	V
Peak ac	±15	V
*DRAIN CURRENT, I_D	50	mA
*TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	Derate at 2.2	mW/°C
*AMBIENT TEMPERATURE RANGE:		
Storage	−65 to +175	°C
Operating	−65 to +175	°C
*LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32" from seating surface for 10 seconds max.	265	°C

*In accordance with JEDEC Registration Data Format JS-9 RDF11-B

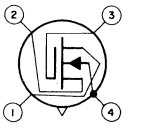
Performance Features

- **Large dynamic range**
- **Enhanced signal-handling capability for low cross-modulation**
- **Dual-polarity gate permits positive and negative swing without degradation of input impedance**
- **Reduced spurious responses in FM receivers**
- **Permits use of vacuum-tube biasing techniques**
- **Excellent thermal stability for critical oscillator designs**

Device Features

- **High input resistance – 1000 megohms**
- **Low feedback capacitance – 0.35 pF max.**
- **Low noise figure – 2.5 dB typ.**
- **High useful power gain – neutralized – 16 dB min. at 100 MHz**
- **Hermetically sealed TO – 72 metal package**

TERMINAL DIAGRAM



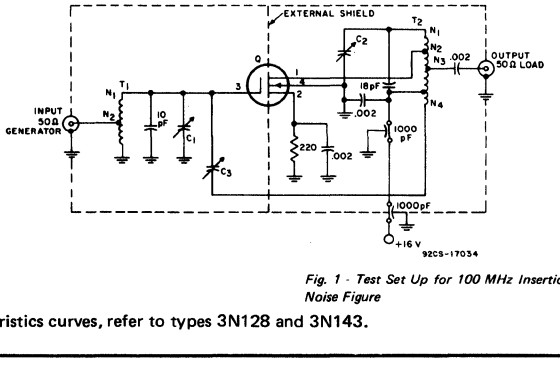
LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

ELECTRICAL CHARACTERISTICS: (At T_A = 25° C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

	CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
*	Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = −8 V, T_A = 25° C	-	0.0001	1	nA
			V_{DS} = 0, V_{GS} = −8 V, T_A = 125° C	-	-	200	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 25° C	-	0.0001	1	nA
			V_{DS} = 0, V_{GS} = +1, T_A = 125° C	-	-	200	nA
*	Zero-Bias Drain Current**	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	25	mA
*	Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = −8 V	-	-	50	μA
*	Gate-to-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	-0.5	-3	-8	V
*	Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	μmho
*	Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
*	Small-Signal Short-Circuit Reverse Transfer Capacitance‡	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.10	0.22	0.35	pF
*	Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.5	7	pF
*	Input Admittance	Y_{is}	Common Source Configuration f = 100 MHz V_{DS} = 15V I_D = 5 mA	-	0.155+J3.45	-	mmho
*	Forward Transfer Admittance	Y_{fs}		-	7.5−J0.9	-	mmho
*	Output Admittance	Y_{os}		-	0.21+J0.9	-	mmho
*	Maximum Available Power Gain	MAG	V_{DS} = 15 V, I_D = 5 mA, f = 100 MHz	-	26	-	dB
	Maximum Usable Power Gain (Fixed Neutralization)	MUG		-	17	-	
*	Insertion Power Gain** (Fixed Neutralization)	G_{ps}		16	-	-	dB
*	Noise Figure**	NF	V_{DS} = 15 V, I_D = 5 mA, f = 100 MHz	-	2.5	4	dB

* In accordance with JEDEC Registration Data Format JS-9 RDF-11B ‡ Three-Terminal Measurement: Source Returned to Guard Terminal
**See Fig. 1



T_1 N_1 = 6 Turns #20 Tinned Copper Wire; ¼" I.D. ½" Long
Q_o = 205, N_1/N_2 = 4.85

T_2 $N_1 + N_4$ = 6¾ Turns #20 Tinned Copper Wire ¼" I.D. ⅝" Long
Q_o = 190 N_1/N_2 = 1.9 N_1/N_3 = 12.3 N_1/N_4 = 8

C_1 = 10 pF Variable Air Capacitor (Hammarlund Mac-10 or Equivalent)
C_2 = 5 pF Variable Air Capacitor (Hammarlund Mac-5 or Equivalent)
C_3 = 0.7-3 pF Piston-Type Variable Air Capacitor (Erie 535C or Equivalent)
Q = 3N142

Fig. 1 - Test Set Up for 100 MHz Insertion Power Gain and Noise Figure

For characteristics curves, refer to types 3N128 and 3N143.

SILICON INSULATED GATE FIELD-EFFECT TRANSISTOR

N-Channel Depletion Type

RCA 3N153 is a silicon, insulated-gate field-effect transistor of the N-channel depletion type, utilizing the MOS* construction. It is intended primarily for critical chopper and multiplex applications up to 60 MHz.

The insulated gate provides a very high value of input resistance (10^{10} ohms typ) which is relatively insensitive to temperature and is independent of gate-bias conditions (positive, negative, or zero bias). The 3N153 also features extremely low feedback capacitance (0.34 pF typ) and virtually zero inherent offset voltage.

This transistor features a Terminal Arrangement in which the gate and source connections are interchanged to provide maximum isolation between the output (drain) and the input (gate) terminals. Although this new basing configuration does not appreciably change the measured device feedback capacitance, it permits the use of external inter-terminal shields to reduce the feedback due to external capacitances, particularly on printed circuit boards. This feature makes it possible to minimize feedthrough capacitance.

The 3N153 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

* Metal-Oxide-Semiconductor

Maximum Ratings, Absolute-Maximum Values:

(Substrate connected to source unless otherwise specified)

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	max.	V
DRAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+20, -0.3	max.	V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+20, -0.3	max.	V
DC GATE-TO-SOURCE VOLTAGE, V_{GS}	+6, -8	max.	V
PEAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14	max.	V
DRAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10)	50	max.	mA
TRANSISTOR DISSIPATION, P_T:			
At ambient temperatures from -65 to +25°C	400	max.	mW
above 25°C	derate linearly at 2.67		mW/°C
AMBIENT TEMPERATURE RANGE:			
Storage	-65 to +175		°C
Operating	-65 to +175		°C
LEAD TEMPERATURE (During soldering):			
At distance ≥ 1/32" to seating surface for 10 seconds max.	265	max.	°C

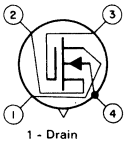
FEATURES

- excellent thermal stability
- virtually zero inherent offset voltage
- low leakage current: 50 pA max.
- low "on" resistance — $r_{DS(on)}$ = 200 Ω typ.
- high "off" resistance — $R_{DS(off)}$ = 10^{10} Ω typ.
- low feedback capacitance — C_{rss} = 0.34 pF typ.
- low input capacitance — C_{iss} = 6 pF typ.

APPLICATIONS

- Choppers
- Multiplexers
- Servo Amplifiers
- Computer Operational Amplifiers
- Sampling Circuits
- Electrometer Amplifiers

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N153 Min.	Typ.	Max.	UNITS
Gate-Leakage Current	I_{GSS}	V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 25°C V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 125°C	- -	0.1 -	50 1	pA nA
Static Drain-to-Source "ON" Resistance	$r_{DS(on)}$	V_{GS} = 0V, V_{DS} = 0V	-	200	300	Ω
Drain-to-Source "OFF" Resistance	$R_{DS(off)}$	V_{GS} = -8V, V_{DS} = +1V	10^9	10^{10}	-	Ω
Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{GS} = -8V, V_{DS} = +1V, T_A = 25°C V_{GS} = -8V, V_{DS} = +1V, T_A = 125°C	- -	0.1 0.1	1 1	nA μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz V_{DS} = 15V, I_D = 5 mA, f = 1 MHz	- -	0.34 0.25	0.5 0.38	pF pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz	-	6	8	pF
Small-Signal, Drain-to-Source Capacitance	C_{ds}	V_{DS} = 0V, V_{GS} = -8V, f = 1 MHz	-	-	3	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	V_{GS} = 0V, V_{DS} = +15V	-	10,000	-	μmho
Offset Voltage	V_0	V_{GS} = +6,-8V; V_{DS} = 0V	-	0*	-	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings of 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No.107-1.0.1, or equivalent.

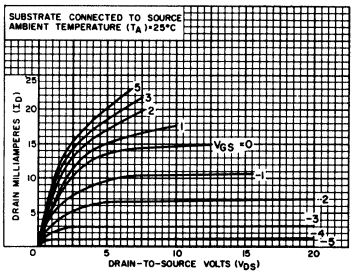


Fig.1 - Drain current vs. drain-to-source voltage.

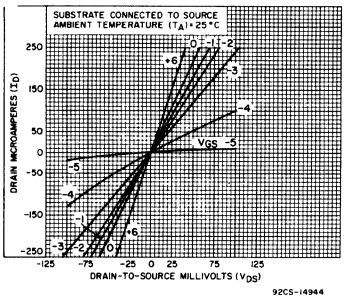


Fig.2 - Low-level drain current vs. drain-to-source voltage.

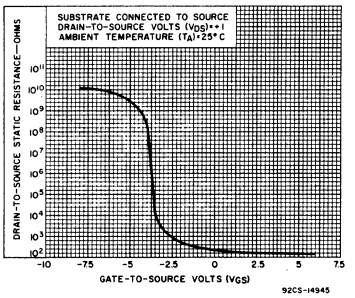


Fig.3 - Drain-to-source static resistance vs. gate-to-source voltage.

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTOR

N-Channel Depletion Type

For Military and Industrial Low-Noise RF-Amplifier Applications Up to 300 MHz

The 3N159 is an n-channel silicon, depletion type, dual insulated-gate, field-effect transistor utilizing the MOS** construction. It has exceptional characteristics for rf-amplifier applications at frequencies up to 300 MHz. This transistor features a series arrangement of two separate channels, each channel having an independent control gate.

Type 3N159 has an exceptionally low-noise figure, which makes this type particularly suitable for critical vhf applications. When used in a common-source configuration in which gate No.2 is ac grounded, this device reduces oscillator feedthrough to the antenna thereby minimizing oscillator radiation.

The 3N159 is hermetically sealed in the metal JEDEC TO-72 package.

** Metal-Oxide-Semiconductor.

APPLICATIONS

- RF amplifier in military and industrial communications equipment
- aircraft, marine and vehicular receivers
- CATV and MATV equipment
- telemetry and multiplex equipment

Maximum Ratings, *Absolute-Maximum Values:*
at T_A = 25°C

DRAIN-TO-SOURCE VOLTAGE, V_{DS} . . . . . 0 to +20 V

GATE-No.1-TO-SOURCE VOLTAGE, V_{G1S}:
- Continuous (dc) . . . . . -8 to +1 V
- Peak ac . . . . . -8 to +20 V

GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:
- Continuous (dc) . . . . . -8 to 40% of V_{DS} V
- Peak ac . . . . . -8 to +20 V

DRAIN-TO-GATE VOLTAGE:
V_{DG1} or V_{DG2} . . . . . +20 V

DRAIN CURRENT, I_D
- Pulsed: Pulse duration ≤ 20 ms, duty factor ≤ 0.15 . . . . . 50 mA

TRANSISTOR DISSIPATION, P_T:
- At ambient temperatures up to 25°C . . . . . 400 mW
- above 25°C . . . . . derate linearly at 2.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Storage and Operating . . . . . -65 to +175 °C

LEAD TEMPERATURE (During soldering):
- At distances ≥ 1/32 inch from seating surface for 10 seconds max. . . . . 265 °C

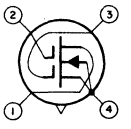
PERFORMANCE FEATURES

- wide dynamic range permits large-signal handling before overload
- dual-gate permits simplified agc circuitry
- virtually no agc power required
- greatly reduces spurious responses in FM receivers
- permits use of vacuum-tube biasing techniques
- excellent thermal stability
- superior cross-modulation performance and greater dynamic range than bipolar or single-gate field-effect transistors

DEVICE FEATURES

- low gate leakage currents — — I_{G1SS} & I_{G2SS} = 1 nA max.
- high forward transconductance — — g_{fs} = 7000 μmho min.
- high unneutralized RF power gain — — G_{ps} = 16 dB min. at 200 MHz
- low vhf noise figure — — NF = 3.5 dB max. at 200 MHz

TERMINAL DIAGRAM



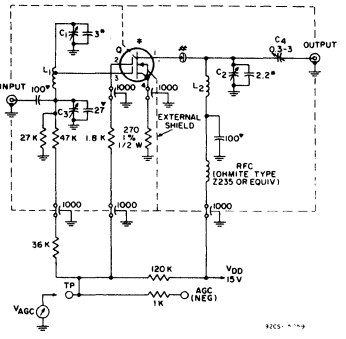
LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

ELECTRICAL CHARACTERISTICS, at T_A = 25°C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS 3N159 Min.	Typ.	Max.	UNITS
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +16V, I_D = 200 μA, V_{G2S} = +4V	-	-2	-4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +16V, I_D = 200 μA, V_{G1S} = 0	-	-2	-4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = -20V, V_{G2S} = 0, V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G1S} = +1V, V_{G2S} = 0, V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G1S} = -20V, V_{G2S} = 0, V_{DS} = 0, T_A = 125°C	-	-	0.2	μA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = -20V, V_{G1S} = 0, V_{DS} = 0, T_A = 25°C	-	-	1	nA
		V_{G2S} = +1, V_{DS} = 0, V_{G1S} = 0, T_A = 25°C	-	-	1	nA
		V_{G2S} = -20V, V_{G1S} = 0, V_{DS} = 0, T_A = 125°C	-	-	0.2	μA
Zero-Bias Drain Current	I_{DSS}*	V_{DD} = +14V, V_{G1S} = 0, V_{G2S} = +4V	5	18	30	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DD} = +14V, I_D = 10 mA, V_{G2S} = +4V, f = 1 kHz	7000	10,000	18,000	μmho
Cutoff Forward Transconductance (Gate-No.1-to-Drain)	$g_{fs(off)}$	V_{DD} = +14V, V_{G1S} = -0.5V, V_{G2S} = -2V, f = 1 kHz	-	-	100	μmho
Small-Signal, Short-Circuit Input Capacitance▲	C_{iss}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 MHz	3	5.5	7	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1)♦	C_{rss}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 MHz	0.01	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}	V_{DS} = +13V, I_D = 10 mA, V_{G2S} = +4V, f = 1 MHz	-	2.2	-	pF
Maximum Usable Power Gain (See Fig.1 for Measurement Circuit)	MUG	V_{DD} = +15V, R_S = 270Ω, R_G = 50Ω, f = 200 MHz	16	18	22	dB
Measured Noise Figure (See Fig.1 for Measurement Circuit)	NF	V_{DD} = +15V, R_S = 270Ω, f = 200 MHz, R_G = 50Ω	-	2.5	3.5	dB

* Pulse Test: Pulse duration ≤ 20 ms, duty factor ≤ 0.15.
▲ Capacitance between Gate No.1 and all other terminals.
♦ Three-Terminal Measurement with Gate No.2 and Source Returned to Guard Terminal.

For characteristics curves refer to types 3N140, 3N141.



* Tubular ceramic
▼ Disc ceramic
Ferrite bead (1/2 used); Indiana General No. H 1742C-(A-147) or F1157-1-H or equivalent.
‡ VHF plug in socket Jettron CD72-148 and CD72149 (part No.7977-1) or equivalent.

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent.
C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.
C_4: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent.
L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1 2 turns from C_1 end of winding.
L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - 200-MHz power gain and noise-figure test circuit for type 3N159.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C unless otherwise specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
* Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		-0.5	-2	-4	V
* Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		-0.5	-2	-4	V
* Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
* Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V V_{G2S} = +4 V V_{G1S} = 0		5	15	30	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 kHz		7000	12,000	18,000	μmho
* Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz		4.0	6.0	8.5	pF
* Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1) ♦	C_{rss}			0.005	0.02	0.03	pF
* Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2.0	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 200 MHz		16	18	22	dB
Maximum Available Power Gain	MAG			–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG			–	20▲	–	dB
Noise Figure (see Fig. 1)	NF			–	3.5	4.5	dB
* Magnitude of Forward Transadmittance	$\|Y_{fs}\|$			–	12,000	–	μmho
* Phase Angle of Forward Transadmittance	θ			–	-35	–	Degrees
Magnitude of Reverse Transadmittance	$\|Y_{rs}\|$			–	25	–	μmho
Angle of Reverse Transadmittance	θ_{rs}			–	-25	–	Degrees
* Input Resistance	r_{iss}			–	1.0	–	kΩ
* Output Resistance	r_{oss}			–	2.8	–	kΩ
Gate-to-Source * Forward Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA		6.5	10	–	V
Gate No. 2	$V_{(BR)G2SSF}$						
Gate-to-Source * Reverse Breakdown Voltage: Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = -100 μA		-6.5	-10	–	V
Gate No. 2	$V_{(BR)G2SSR}$						

▲Limited only by practical design considerations.

† Capacitance between Gate No. 1 and all other terminals

♦ Three-terminal measurement with Gate No. 2 and Source returned to ground terminal.

* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

OPERATING CONSIDERATIONS

The flexible leads of the 3N187 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

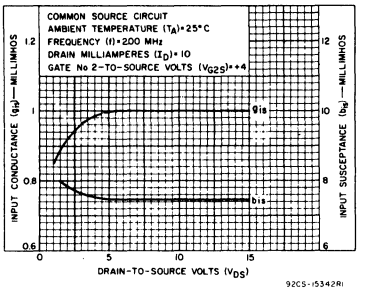


Fig. 8 - y_{is} vs. V_{DS}

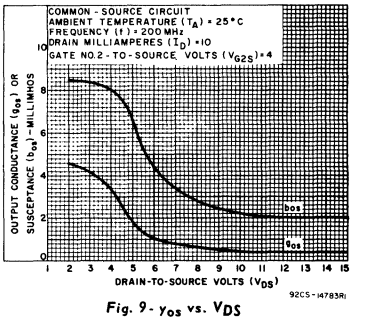


Fig. 9 - y_{os} vs. V_{DS}

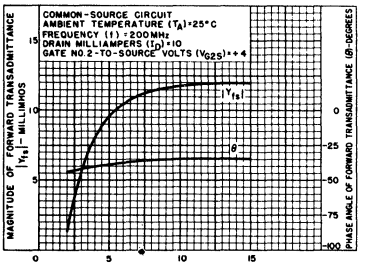


Fig. 10 - y_{fs} vs. V_{DS}

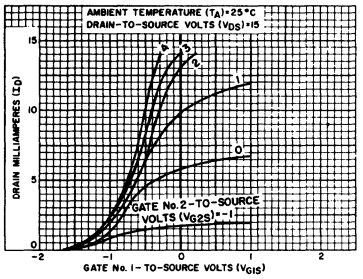


Fig. 6 - I_D vs. V_{G1S}

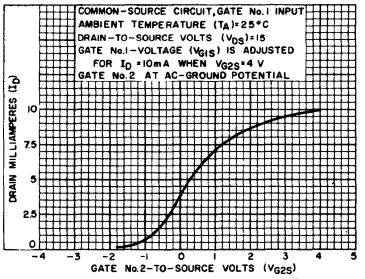


Fig. 7 - I_D vs. V_{G2S}

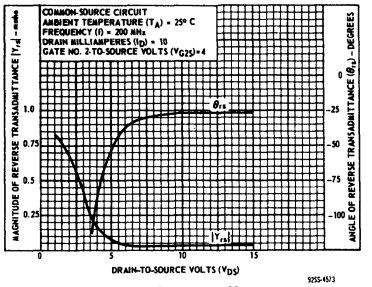


Fig. 11 - y_{rs} vs. V_{DS}

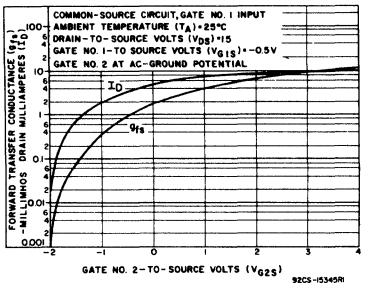


Fig. 24 - g_{fs} and I_D vs. V_{G2S}

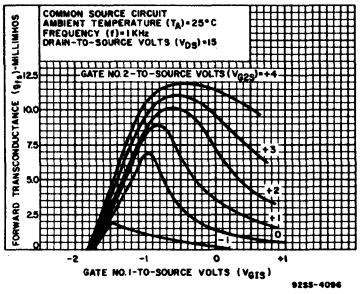


Fig. 25. - g_{fs} vs. V_{G1S}

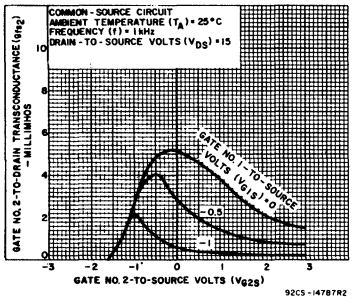


Fig. 26 - g_{fs_2} vs. V_{G2S}

ELECTRICAL CHARACTERISTICS at T_A = 25°C unless otherwise specified		SYMBOLS	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
* Gate No. 1-to-Source Cutoff Voltage		$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G2S} = +4 V		-0.1	-1	-3	V
* Gate No. 2-to-Source Cutoff Voltage		$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G1S} = 0		-0.1	-1	-3	V
* Gate No. 1-Terminal Forward Current		I_{G1SSF}	V_{G1S} = +1 V, V_{G2S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
* Gate No. 1-Terminal Reverse Current		I_{G1SSR}	V_{G1S} = -6 V, V_{G2S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
* Gate No. 2-Terminal Forward Current		I_{G2SSF}	V_{G2S} = +6 V, V_{G1S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
* Gate No. 2-Terminal Reverse Current		I_{G2SSR}	V_{G2S} = -6 V, V_{G1S} = V_{DS} = 0	T_A = 25°C	–	–	50	nA
				T_A = 100°C	–	–	5	μA
* Zero-Bias Drain Current		I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V		0.5	5.0	12	mA
* Forward Transconductance (Gate No. 1-to-Drain)		g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V	f = 1 kHz	10,000	15,000	20,000	μmho
Small-Signal, Short-Circuit Input Capacitance†		C_{iss}		f = 1 MHz	4.0	6.0	8.5	pF
* Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦		C_{rss}			0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance		C_{oss}			–	2.0	–	pF
* Power Gain (see Fig. 1)		G_{PS}		f = 400 MHz	10	12.5	–	dB
Noise Figure (see Fig. 1)		NF			–	3.9	6.0	dB
* Bandwidth		BW			28	–	38	MHz
* Gate-to-Source Forward Breakdown Voltage	Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	V_{G2S} = V_{DS} = 0	6.5	–	13	V
	Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} = V_{DS} = 0				
* Gate-to-Source Reverse Breakdown Voltage	Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	V_{G2S} = V_{DS} = 0	-6.5	–	-13	V
	Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} = V_{DS} = 0				

*In accordance with JEDEC registration data format (JS-9 RDF-19A)

†Capacitance between Gate No. 1 and all other terminals.
♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.

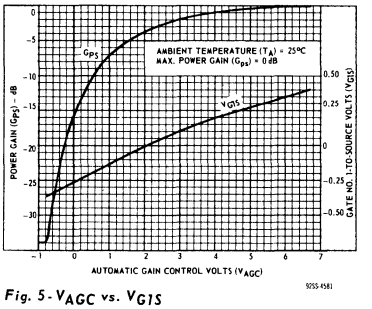


Fig. 5 - V_{AGC} vs. V_{G1S}

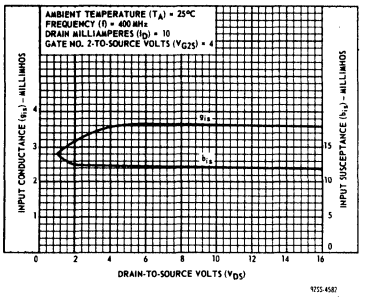


Fig. 6 - y_{is} vs. V_{DS}

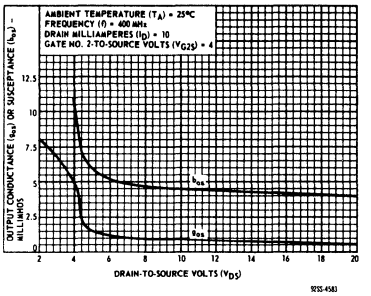


Fig. 7 - y_{os} vs. V_{DS}

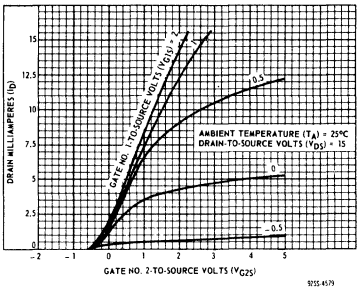


Fig. 3 - I_D vs. V_{G2S}

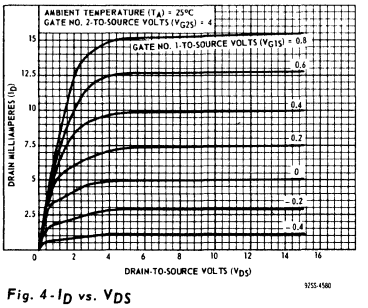


Fig. 4 - I_D vs. V_{DS}

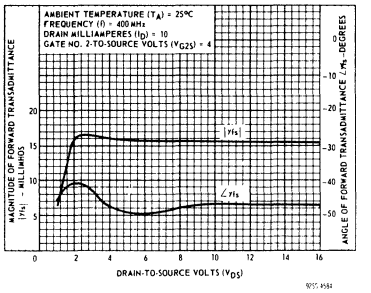


Fig. 8 - y_{fs} vs. V_{DS}

Silicon Dual-Insulated-Gate Field-Effect Transistors

With Integrated Gate-Protection Circuits
For VHF TV Applications

3N204 – RF Amplifier
3N205 – Mixer
3N206 – TV IF Amplifier

The RCA-3N204, 3N205, and 3N206 are n-channel silicon, depletion type, dual-insulated gate, field-effect transistors intended for vhf TV applications. Integrated back-to-back diodes protect the gates from excessive input voltages.

The 3N204 is intended for use in vhf rf amplifiers and delivers linear, low-noise amplification. Its extremely low feedback capacitance allows high-gain stable operation without neutralization. The 3N205 is specified for low noise vhf mixer applications. The 3N206 is intended for use in tuned high-frequency amplifiers such as TV if strips.

Features:

- **Low C_{rss} – 0.03 pF max.**
- **High $|Y_{fs}|$ – 14 mmho typ. for 3N204 and 3N205**
- **Integrated gate-protection diodes**

MAXIMUM RATINGS,
Absolute Maximum Values at $T_A = 25^oC$

* DRAIN-TO-GATE No.1 VOLTAGE	30	V
* DRAIN-TO-GATE No.2 VOLTAGE	30	V
* DRAIN-TO-SOURCE VOLTAGE	25	V
* GATE No.1-TERMINAL FORWARD CURRENT▲	10	mA
* GATE No.2-TERMINAL FORWARD CURRENT▲	10	mA
* GATE No.1-TERMINAL REVERSE CURRENT	−10	mA
* GATE No.2-TERMINAL REVERSE CURRENT	−10	mA
* CONTINUOUS DRAIN CURRENT	50	mA
* DEVICE DISSIPATION:		
Up to $T_A = 25^oC$	360	mW
Above $T_A = 25^oC$ derate linearly	2.4	mW/°C
Up to $T_C = 25^oC$	1.2	W
Above $T_C = 25^oC$ derate linearly	8	mW/°C
* AMBIENT TEMPERATURE RANGE:		
Operating	−65 to +175	°C
Storage	−65 to +200	°C
* LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+300	°C

▲ Forward gate-terminal current is the current into a gate terminal with a forward-gate-to-source voltage applied. This voltage is of such polarity that an increase in its magnitude causes the channel resistance to decrease.

* In accordance with JEDEC registration data format (JS-9 RDF-19B)

OPERATING CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
3N204					
* Common-Source Spot Noise Figure, NF	V_{DD}=18 V, V_{GG}=7 V, f = 200 MHz, See Fig.13	–	–	3.5	dB
* Small-Signal Common-Source Insertion Power Gain, G_{ps}		20	–	28	dB
* Bandwidth, BW		7	–	12	MHz
* Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=18 V, ΔG_{ps}=−30dB,[1] f=200 MHz, See Fig. 13	0	–	−2	V
* Common-Source Spot Noise Figure, NF	V_D=15 V, V_{G2S} = 4 V, f = 450 MHz, I_D = 10 mA, See Figs. 15 and 16	–	–	5	dB
* Small-Signal Common Source Insertion Power Gain, G_{ps}		14	–	–	dB
3N205					
* Small-Signal Conversion Power Gain, G_{ps} (conv)	V_{DD}=18 V, f_{LO}=245 MHz,[3] f_{RF}=200 MHz, See Fig.17	17	–	28	dB
* Bandwidth, BW		4	–	7	MHz
3N206					
* Common-Source Spot Noise Figure, NF	V_{DD}=24 V, V_{GG}=6 V, f=45 MHz, See Fig. 14	–	–	4	dB
* Small-Signal Common-Source Insertion Power Gain, G_{ps}		25	–	35	dB
* Bandwidth, BW		3	–	6	MHz
* Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=24 V, ΔG_{ps}=−30dB,[2] f=45 MHz, See Fig. 14	−1.6	–	0.6	V

*In accordance with JEDEC registration data format (JS-9 RDF-19B).

1. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7V.
2. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 6V.
3. Amplitude at input from local oscillator is 3 V RMS.

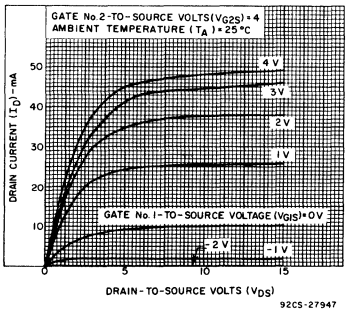


Fig.1 – Drain current vs. drain-to-source volts (pulse-tested with pulse duration = 300 μs, duty cycle ≤2%).

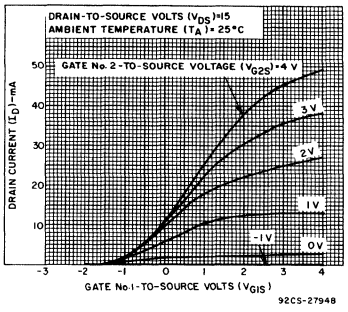


Fig.2 – Drain current vs. gate-No.1-to-source volts (pulse-tested with pulse duration = 300 μs, duty cycle ≤ 2%).

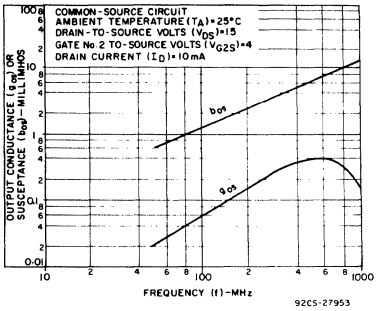


Fig.7 — Y_{os} vs. f

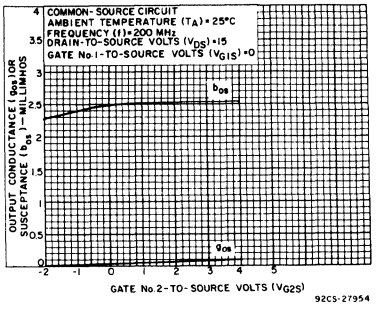


Fig.8 — Y_{os} vs. V_{G2S}

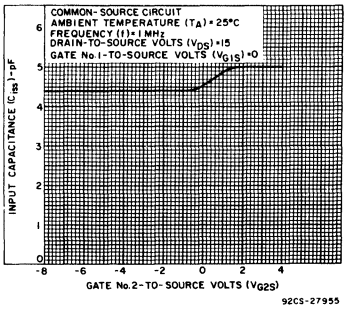


Fig.9 — C_{iss} vs. V_{G2S}

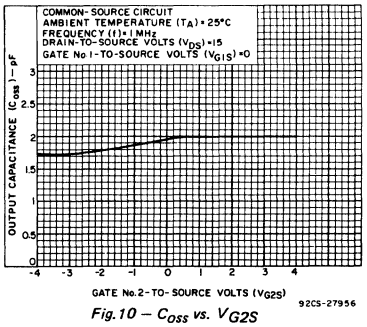
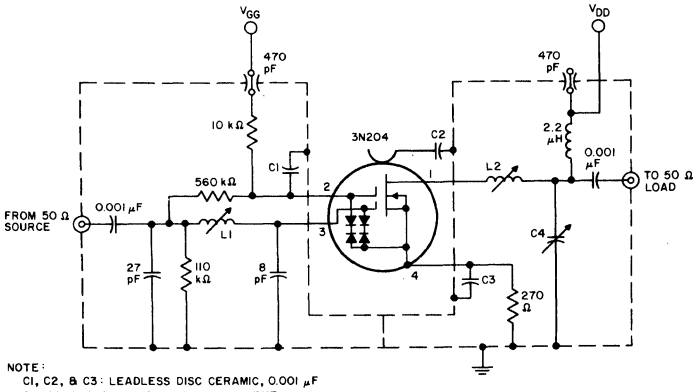


Fig.10 — C_{oss} vs. V_{G2S}



NOTE:
C1, C2, & C3: LEADLESS DISC CERAMIC, 0.001 μF
C4: ARCO 462, 5-80 pF, OR EQUIVALENT
L1: 3 TURNS No. 18 WIRE, 3/16 INCH-DIA. ALUMINUM SLUG
L2: 9 TURNS No. 20 WIRE, 3/16 INCH-DIA. ALUMINUM SLUG

92CS-27960

Fig.12 — 200-MHz power gain, gain-control voltage, and noise-figure test circuit for 3N204.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).

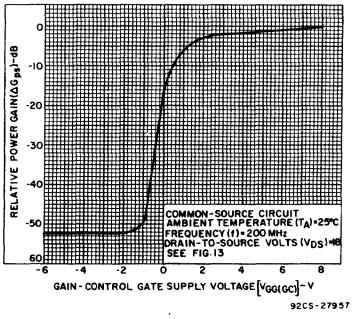


Fig.11 — ΔG_{ps} vs. $V_{GG(GC)}$

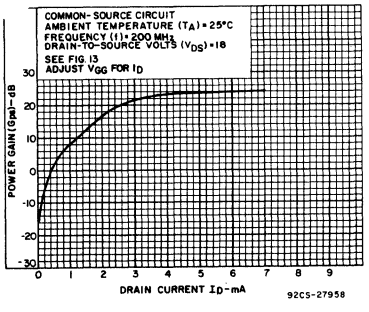
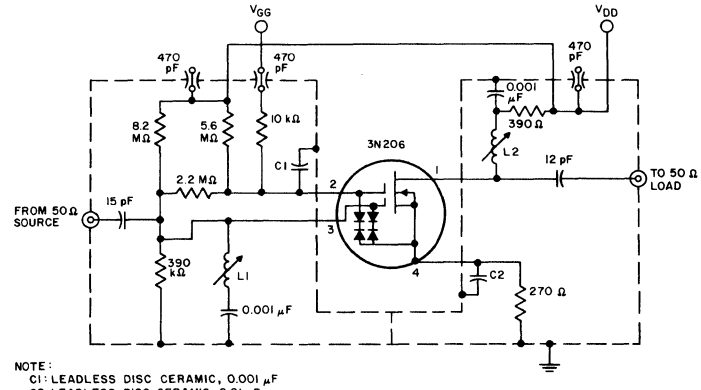


Fig.13 — G_{ps} vs. I_D

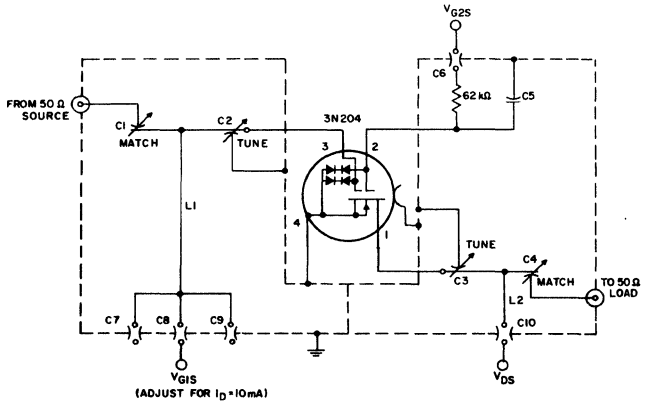


NOTE:
C1: LEADLESS DISC CERAMIC, 0.001 μF
C2: LEADLESS DISC CERAMIC, 0.01 μF
L1: 8 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG
L2: 9 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG

92CM-27959

Fig.14 — —45-MHz power-gain and noise-figure test circuit for 3N206.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).

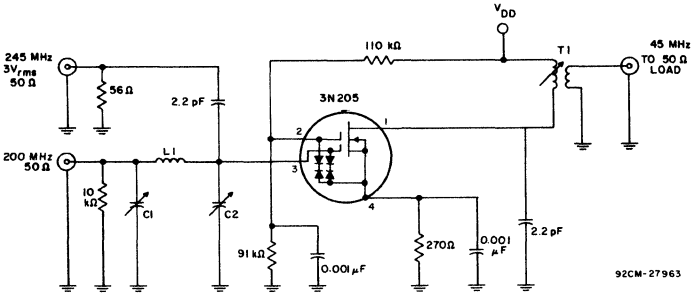


NOTE:
FOR TEST FIXTURE, SEE PICTORAL DRAWING IN FIGURE 16
C1 THRU C4: SEE FIGURE 16, NOTE D
C5: 0.001 μF LEADLESS DISC CAPACITOR
C6 THRU C10: ALLEN-BRADLEY F5AU 0.001 μF FEED-THROUGH CAPACITORS, OR EQUIVALENT
L1 & L2: SEE FIGURE 16

92CM-27961

Fig. 16 – –450-MHz power-gain and noise-figure test circuit for 3N204.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).



NOTE:
C1: ARCO 462, 5–80 pF, or EQUIVALENT
C2: ARCO 460, 1.5–15 pF, OR EQUIVALENT
L1: 4 TURNS No.14 WIRE, 1/4 INCH INSIDE DIA.

T1: PRI: 16 TURNS No.30 WIRE CLOSE WOUND ON 1/4 INCH DIA. FORM, TYPE "J" SLUG
SEC: 5 TURNS No.30 WIRE CENTERED OVER PRIMARY

Fig. 17 – –200 MHz-to-45-MHz circuit for conversion power gain for 3N205.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).

ELECTRICAL CHARACTERISTICS, At T_A = 25°C (unless otherwise specified)

	CHARACTERISTIC	TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
*	Drain-to-Source Breakdown Voltage, $V_{(BR)DS}$	I_D = 10μA, $V_{G1S}=V_{G2S}$ = −4V	3N211	27	–	V
			3N212	27	–	
			3N213	35	–	
*	Gate No.1-to-Source Forward Breakdown Voltage, $V_{(BR)G1SSF}$[1]	I_{G1}=10mA, $V_{G2S}=V_{DS}$=0		6	–	V
*	Gate No.1-to-Source Reverse Breakdown Voltage, $V_{(BR)G1SSR}$[1]	I_{G1}= −10mA, $V_{G2S}=V_{DS}$=0		−6	–	V
*	Gate No.2-to-Source Forward Breakdown Voltage, $V_{(BR)G2SSF}$[1]	I_{G2}=10mA, $V_{G1S}=V_{DS}$=0		6	–	V
*	Gate No.2-to-Source Reverse Breakdown Voltage, $V_{(BR)G2SSR}$[1]	I_{G2}= −10mA, $V_{G1S}=V_{DS}$=0		−6	–	V
*	Gate No.1-Terminal Forward Current, I_{G1SSF}	V_{G1S}=5V, $V_{G2S}=V_{DS}$=0		–	10	nA
*	Gate No.1-Terminal Reverse Current, I_{G1SSR}	V_{G1S}= −5V, $V_{G2S}=V_{DS}$=0	T_A=25°C	–	−10	nA
			T_A=150°C	–	−10	μA
*	Gate No.2-Terminal Forward Current, I_{G2SSF}	V_{G2S}=5V, $V_{G1S}=V_{DS}$=0		–	10	nA
*	Gate No.2-Terminal Reverse Current, I_{G2SSR}	V_{G2S}= −5V, $V_{G1S}=V_{DS}$=0	T_A=25°C	–	−10	nA
			T_A=150°C	–	−10	μA
*	Zero-Gate No.1-Voltage Drain Current, I_{DS}[2]	V_{DS}=15V, V_{G1S}=0, V_{G2S}=4V		6	40	mA
*	Gate No.1-to-Source Cutoff Voltage, $V_{G1S(off)}$	V_{DS}=15V, V_{G2S}=4V, I_D=20μA	3N211	−0.5	−5.5	V
			3N212	−0.5	−4	
			3N213	−0.5	−5.5	
*	Gate No.2-to-Source Cutoff Voltage, $V_{G2S(off)}$	V_{DS}=15V, V_{G1S}=0, I_D=20μA	3N211	−0.2	−2.5	V
			3N212	−0.2	−4	
			3N213	−0.2	−4	
*	Small-Signal Common-Source Forward Transfer Admittance, $\lvert y_{fs}\rvert$[3]	V_{DS}=15V, V_{G1S}=0, V_{G2S}=4V, f=1 kHz	3N211	17	40	mmho
			3N212	17	40	
			3N213	15	35	
*	Small-Signal Common-Source Reverse Transfer Capacitance, C_{rss}	V_{DS}=15V, V_{G2S}=4V, I_D=1mA, f=1MHz		0.005	0.05	pF

*In accordance with JEDEC registration data format (JS-9 RDF-19B).

1. All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage-limiting network is functioning properly.
2. This characteristic must be measured using pulse techniques (t_W = 300μs, duty cycle ≤ 2%).
3. This characteristic must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate No.1 with gate No.2 at ac ground.

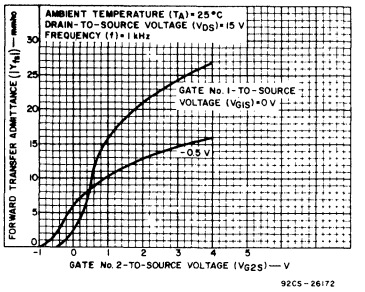


Fig. 5 – $|Y_{fs}|$ vs. V_{G2S} for 3N211 and 3N212.

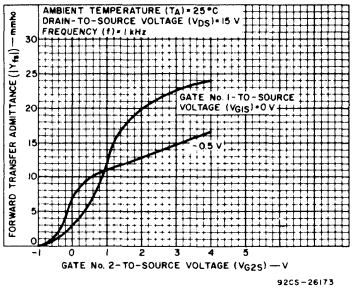


Fig. 6 – $|Y_{fs}|$ vs. V_{G2S} for 3N213.

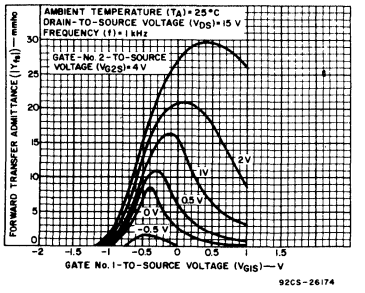


Fig. 7 – $|Y_{fs}|$ vs. V_{G1S} for 3N211, and 3N212.

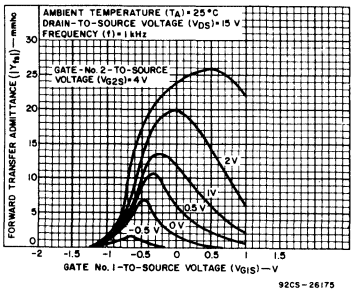
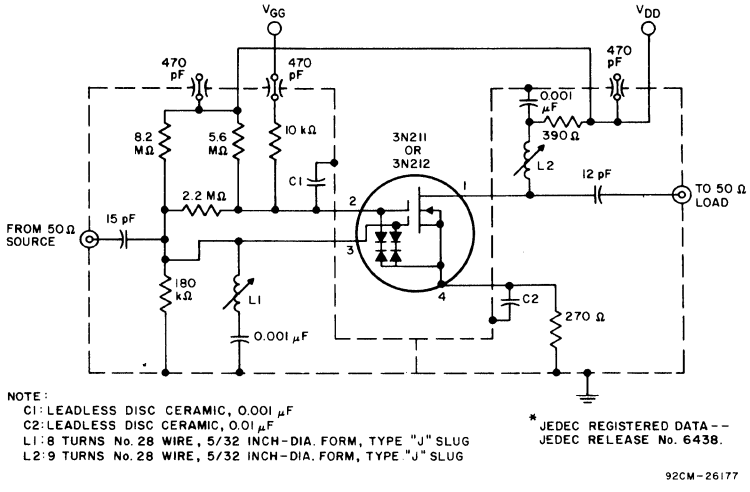


Fig. 8 – $|Y_{fs}|$ vs. V_{G1S} for 3N213.



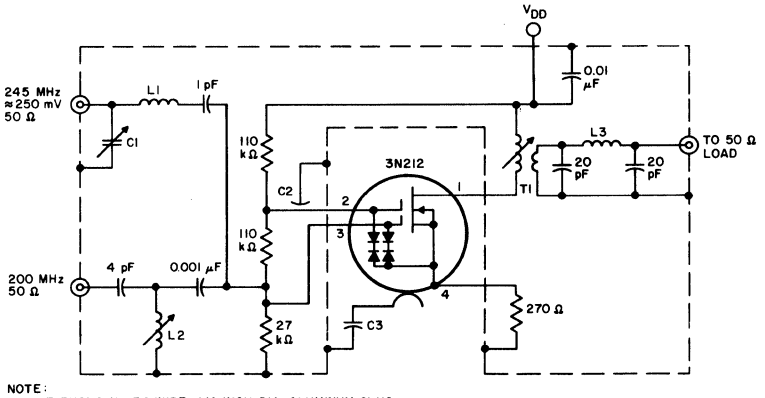
NOTE:
C1: LEADLESS DISC CERAMIC, 0.001 μF
C2: LEADLESS DISC CERAMIC, 0.01 μF
L1: 8 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG
L2: 9 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG

* JEDEC REGISTERED DATA -- JEDEC RELEASE No. 6438.

92CM-26177

Fig. 10—45 MHz power gain and noise figure test circuit for 3N211 and 3N213.*

TEST CIRCUITS (CONT'D)



NOTE:
L1: 7 TURNS No. 34 WIRE, 1/4 INCH DIA. ALUMINUM SLUG
L2: 5 1/2 TURNS No. 20 WIRE, 1/4 INCH DIA. ALUMINUM SLUG
L3: 7 TURNS No. 24 WIRE, 1/4 INCH DIA. AIR CORE
T1: PRI: 25 TURNS No. 30 WIRE CLOSE WOUND ON 1/4 INCH DIA. FORM, TYPE "J" SLUG
SEC: 4 TURNS No. 30 WIRE CENTERED OVER PRIMARY
C1: ARCO TYPE 462, 5-80 pF
C2: 0.001 μF LEADLESS DISC
C3: 0.01 μF LEADLESS DISC

92CM-26178

* JEDEC REGISTERED DATA -- JEDEC RELEASE No. 6438.

Fig. 11—200 MHz-to-45 MHz circuit for conversion power gain for 3N212.*

MOS Silicon Transistors

N-Channel Depletion Types

For RF Amplifier and Mixer Applications in FM and AM/FM Receivers

RCA-40468A and 40559A are silicon insulated-gate field-effect transistors of the n-channel depletion type utilizing the MOS* construction. They are intended primarily for use as the rf amplifier and mixer, respectively, in FM receivers covering the 88 to 108 MHz band, but can be used for general amplifier applications at frequencies up to 125 MHz. For circuit design and typical performance data refer to RCA Application Note AN3535 "An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer".

The wide dynamic range of these transistors reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

Operating as a neutralized amplifier at 100 MHz, the 40468A can provide a power gain of 17 dB (typ.). A power gain of 14 dB (typ.) can be realized without neutralization.

* Metal-Oxide-Semiconductor.

Performance Features:

- **reduced spurious responses in FM tuners**
- **reverse bias on substrate improves linearity**
- **reduced cross-modulation effects in AM receivers**

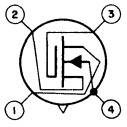
Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25^oC$:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	+20	V
DRAIN-TO-GATE VOLTAGE, V_{DG}	+20	V
GATE-TO-SOURCE VOLTAGE, V_{GS}:		
CONTINUOUS (dc)	+1, -8	V
PEAK ac	±15	V
DRAIN CURRENT, I_D	25	mA
TRANSISTOR DISSIPATION:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate at 2.2	mW/°C
AMBIENT TEMPERATURE RANGE:		
Storage	-65 to +175	°C
Operating	-65 to +175	°C
LEAD TEMPERATURE (During Soldering):		
At distances not closer than 1/32 inch to seating surface for 10 seconds maximum	265	°C

Device Features:

- **high forward transconductance - - gfs = 7500 μmho typ. for 40468A**
- **low feedback capacitance - - C_{rss} = 0.35 pF max. for 40468A, 0.38 pF max. for 40559A**
- **high useful power gains - - neutralized - 17 dB typ., unneutralized - 14 dB typ.**
- **hermetically sealed in TO-72 metal package**

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$
With Bulk (Substrate) Connected to Source Unless Otherwise Specified

Characteristics	Symbols	TEST CONDITIONS			LIMITS						Units
		Frequency f	DC Drain-to-Source V_{DS}	DC Drain Current I_D	RCA-40468A RF Amplifier			RCA-40559A Mixer			
		MHz	V	mA	Min.	Typ.	Max.	Min.	Typ.	Max.	
Drain-to-Source Cutoff Current	$I_{D(off)}$	-	12	V_{GS} = -8V	-	-	100	-	-	500	μA
Gate Leakage Current	I_{GSS}	-	0	V_{GS} = -8V	-	-	1	-	-	1	nA
		-	0	V_{GS} = +1V	-	-	1	-	-	1	nA
Zero-Bias Drain Current	I_{DSS}	-	15	V_{GS} = 0	5	15	30	5	15	30	mA
Small-Signal, Short-Circuit Forward Transconductance	g_{fs}	1 kHz	15	5	-	7500	-	-	-	-	μmho
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15	5	-	0.25	0.35	-	0.25	0.38	pF
Input Capacitance	C_{iss}	1	15	5	-	5.5	-	-	5.5	-	pF
Admittance	-	RF | Mixer		RF | Mixer	-			-			-
Input Admittance	Y_{is}	100 MHz	15	5 | 3	0.155 + j 3.45			0.14 + j 3.38			mmho
Forward Transfer Admittance	Y_{fs}	100 MHz	15	5 | 3	7.4 + j 0.9			-			mmho
Output Admittance	Y_{os}	100 MHz | 10.7 MHz	15	5 | 3	0.21 + j 0.9			0.076 + j 0.153			mmho
Forward Conversion Transconductance	$g_{fs(c)}$	1 kHz	15	3	-	-	-	-	2800*	-	μmho
Maximum Available Power Gain	MAG	100	15	5	-	26	-	-	-	-	dB
Maximum Usable Power Gain (Unneutralized)	MUG	100	15	5	-	14	-	-	-	-	dB
Maximum Usable Power Gain (Neutralized)	MUG	100	15	5	14	17	-	-	-	-	dB
Maximum Available Conversion Gain	MAG_C	f_{in} = 100 f_{out} = 10.7	15	3	-	-	-	-	22	-	dB
Noise Figure	NF	100	15	5	-	3.5	5	-	-	-	dB

* Bulk (Substrate)-to-Source Volts (V_{BS}) = -3.

For characteristics curves, refer to types 3N128 and 3N143.

SILICON DUAL INSULATED-GATE FIELD-EFFECT TRANSISTORS

N-Channel Depletion Types
For FM Tuner Applications

RCA 40603 and 40604 are n-channel silicon, depletion type, dual insulated-gate, field-effect transistors utilizing the MOS construction.

These devices have exceptional characteristics for rf-amplifier (40603) and mixer applications (40604) in FM tuners and other commercial equipment operating at frequencies up to approximately 150 MHz. These transistors feature a series arrangement of two separate channels, each channel having an independent control gate. For amplifier applications the 40603 with its wide dynamic range provides substantially better cross-modulation performance and relative freedom from spurious responses than is obtainable with bipolar or single-gate field-effect transistors. The mixing function performed by the 40604 is unique in that the signal applied to gate No.2 is used to modulate the input-gate (gate No.1) transfer characteristic. This technique is superior to conventional "square law" mixing, which can only be accomplished in the non-linear region of the device transfer characteristic.

Because of the low feedback capacitance (0.02 typ. pF) the 40603 can provide a power gain of 25 dB (typ.) at 100 MHz in an unneutralized amplifier circuit.

The gain of the rf stage can be controlled by applying agc voltage to gate No.2. Virtually no agc power is required for full gain reduction.

The 40603 and 40604 are hermetically sealed in JEDEC TO-72 packages.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	0 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-8 to +1	V
Peak ac	-8 to +20	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-8 to 40% of V_{DS}	V
Peak ac	-8 to +20	V
DRAIN-TO-GATE VOLTAGE, V_{DG1} or V_{DG2}	+20	V
DRAIN CURRENT, I_D (Pulsed):		
Pulse duration ≤ 20 ms, duty factor ≤ 0.15	50	mA
TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	400	mW
above 25°C	derate linearly at 2.67 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥ 1/32" from seating surface for 10 seconds max.	265	°C

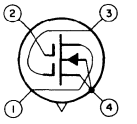
PERFORMANCE FEATURES

- large dynamic range permits large-signal handling before overload
- dual gates allow product mixing with extremely low harmonic generation
- greatly reduces spurious responses in FM receivers
- permits use of vacuum-tube biasing techniques
- *excellent thermal stability*
- superior cross-modulation performance and greater dynamic range than bipolar and single-gate field-effect transistors

DEVICE FEATURES

- extremely low feedback capacitance
  C_{rss} = 0.02 pF typ.
- high unneutralized RF power gain
  MUG = 25 dB (typ.) for 40603
- low noise figure
  NF = 2.5 dB typ. for 40603

TERMINAL DIAGRAM



Lead 1 — Drain
Lead 2 — Gate No. 2
Lead 3 — Gate No. 1
Lead 4 — Source, Substrate and Case

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS 40603 RF AMPLIFIER Typ.	40603 RF AMPLIFIER Max.	40604 MIXER Typ.	40604 MIXER Max.	UNITS
Gate No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G2S} = +4 V	-2	--	-2	--	V
Gate No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G1S} = 0	-2	--	-2	--	V
Gate No.1 Leakage Current	I_{G1SS}	V_{G1S} = -20 V, V_{G2S} = 0, V_{DS} = 0	--	1	--	1	nA
Gate No.2 Leakage Current	I_{G2SS}	V_{G2S} = -20 V, V_{G1S} = 0, V_{DS} = 0	--	1	--	1	nA
Zero-Bias-Voltage Drain Current	I_{DSS}	V_{G2S} = +4 V, V_{G1S} = 0, V_{DS} = +13 V	18	--	18	--	mA
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate-No.1)	C_{rss}	V_{DS} = +13 V, I_D = 10 mA, f = 1 MHz, V_{G2S} = +4 V	0.02	0.03	0.02	0.03	pF
Input Capacitance	C_{iss}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 MHz	5.5	--	5.5	--	pF
Output Capacitance	C_{oss}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 100 MHz	2.1	--	2.3	--	pF
Input Resistance	r_{is}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 100 MHz	3.5	--	3.5	--	kΩ
Output Resistance	r_{os}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V; f = 100 MHz	4	--	--	--	kΩ
		f = 10.7 MHz	--	--	20	--	kΩ
Forward Transconductance	g_{fs}	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 kHz	10,000	--	2800*	--	μmho
Maximum Available Power Gain	MAG	V_{DS} = +13 V, I_D = 10 mA, V_{G2S} = +4 V, f = 100 MHz, f_{out} for 40604 (mixer) = 10.7 MHz	26	--	21	--	dB
Maximum Usable Power Gain (Unneutralized)	MUG		25▲	-	--	--	dB
Noise Figure	NF		2.5	--	--	--	dB

* conversion transconductance
▲ or limited by design considerations

For characteristics curves, refer to type 3N140.

Silicon Dual-Insulated-Gate Field-Effect Transistor

N-Channel Depletion Type

With Integrated Gate-Protection Circuits

For RF Amplifier Applications up to 250 MHz

RCA-40819 is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor (FET).

The excellent overall performance characteristics of the RCA-40819 make it useful for a wide variety of rf-amplifier applications at frequencies up to 250 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 40819 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac grounding Gate No.2. The reduced capacitance allows operation at maximum gain *without neutralization* and reduces local oscillator feedthrough to the antenna -- features of special importance in rf and if amplifiers.

Special back-to-back diodes are diffused directly into the MOS pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts and protect the gates against damage in all normal handling and usage.

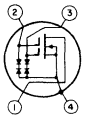
The back-to-back diode configuration permits the 40819 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The 25-volt drain-to-source rating permits the use of higher voltage power supplies.

The 40819 is hermtically sealed in the metal JEDEC TO-72 package.

TERMINAL DIAGRAM

LEAD 1 - DRAIN
LEAD 2 - GATE No.2
LEAD 3 - GATE No.1
LEAD 4 - SOURCE, SUBSTRATE, AND CASE



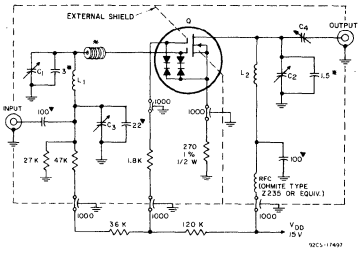
ELECTRICAL CHARACTERISTICS, at T_A = 25° C unless otherwise specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Gate-No.1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G2S} = +4 V	–	–2	–4	V
Gate-No.2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 200 μA, V_{G1S} = 0	–	–2	–4	V
Gate-No.1-Leakage Current	I_{G1SS}	V_{G1S} = ± 6 V, V_{DS} = 0, V_{G2S} = 0	–	–	50	nA
Gate-No.2-Leakage Current	I_{G2SS}	V_{G2S} = ± 6 V, V_{DS} = 0, V_{G1S} = 0	–	–	50	nA
Zero-Bias Drain Current	I_{DSS}	V_{DS} = + 15 V, V_{G2S} = +4 V, V_{G1S} = 0	5	15	35	mA
Forward Transconductance (Gate-No.1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 kHz	–	12,000	–	μmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 1 MHz	–	6	–	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No.1)♦	C_{rss}		0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}		–	2	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V, f = 200 MHz	14	18	–	dB
Maximum Available Power Gain	MAG		–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG		–	20*	–	dB
Noise Figure (see Fig. 1)	NF		–	3.5	6.0	dB
Magnitude of Forward Transadmittance	$\|Y_{fs}\|$		–	12,000	–	μmho
Phase Angle of Forward Transadmittance	θ		–	–35	–	degrees
Input Resistance	r_{iss}		–	1	–	kΩ
Output Resistance	r_{oss}		–	2.8	–	kΩ
Protective Diode Knee Voltage	V_{knee}	I_{diode} (reverse) = ±100 μA	–	±10	–	V

* Limited only by practical design considerations.

† Capacitance between Gate No.1 and all other terminals.

♦ Three-terminal measurement with Gate No.2 and Source returned to guard terminal.



#Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in OD; 0.03 in ID; 0.063 in thickness.

Q = 40673

▼Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1: 1.8 – 8.7 pF variable air capacitor: E. F. Johnson Type 160-104, or equivalent.

C_2*: 1.5 – 5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in thick, 0.075-0.085 in wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4-1/2 turns silver-plated 0.02 in thick, 0.085-0.095-in wide, 5/16-in; ID Coil = .90 in long.

Fig. 1. 200 MHz power gain and noise figure test circuit

For characteristics curves, refer to type 3N187.

Device Features

- **back-to-back diodes protect each gate against handling and in-circuit transients**
- **high forward transconductance: g_{fs} = 12,000 μmho (typ.)**
- **high unneutralized RF power gain: G_{ps} = 18 dB (typ.) at 200 MHz**
- **low VHF noise figure: 3.5 dB (typ.) at 200 MHz**
- **low gate leakage currents: I_{G1SS} & I_{G2SS} = 50 nA at T_A = 25° C**
- **increased drain-to-source voltage rating: V_{DS} = –0.2 to +25 V**

Performance Features

- **superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s**
- **wide dynamic range permits large-signal handling before overload**
- **virtually no agc power required**
- **greatly reduces spurious responses in FM receivers**
- **dual gate permits simplified AGC circuitry**

Applications

- **RF amplifier, mixer, and IF amplifier in military, industrial, and consumer communications equipment**
- **aircraft and marine vehicular receivers**
- **CATV and MATV equipment**
- **telemetry and multiplex equipment**

Absolute Maximum Values, at T_A = 25°C:

Drain-to-Source Voltage, V_{DS}	–0.2 to +25	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+31	V
Drain Current, I_D	50	mA
Transistor Dissipation, P_T:		
At T_A up to 25°C	330	mW
At T_A above 25°C	derate linearly 2.2	mW/°C
Ambient Temperature Range:		
Operating and Storage	–65 to +175	°C
Lead Temperature (During Soldering):		
At distances 1/32 in from seating surface for 10 s max.	265	°C

Maximum Ratings

Continuous Working Voltage#, at T_A = 25°C:

Gate No.1-to-Source Voltage, V_{G1S}	–6 to +3	V
Gate No.2-to-Source Voltage, V_{G2S}	–6 to +6 or 40% of V_{DS} (whichever value is less)	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+25	V

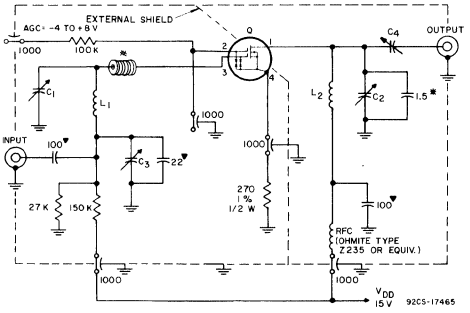
Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the absolute Maximum Ratings are not exceeded.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS 40820 Min.	40820 Typ.	40820 Max.	40821 Min.	40821 Typ	40821 Max	UNITS
Gate No. 1 to Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G2S}= +4V			1	3	-	-1	-3	V
Gate No. 2 to Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS}= +15V, I_D=200μA, V_{G1S}=0		-	-1	-3	-	-1	-3	V
Gate to Source Forward Breakdown Voltage Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} I_{G2SSF} 100 μA	V_{G2S} V_{DS} 0		9	-	-	11	-	V
Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} V_{DS} 0		9	-	-	11	-	V
Gate to Source Reverse Breakdown Voltage Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} I_{G2SSR} 100 μA	V_{G2S} V_{DS} 0		9	-	-	11	-	V
Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} V_{DS} 0		9	-	-	11	-	V
Gate No. 1 Terminal Forward Current	I_{G1SSF}	V_{DS} V_{G2S} 0	V_{G1S} 6 V	-	-	50	-	-	-	nA
			V_{G1S} 4.5 V		-	-	-	-	50	nA
Gate No. 1 Terminal Reverse Current	I_{G1SSR}	V_{DS} V_{G2S} 0	V_{G1S} 6 V		-	50	-	-	-	nA
			V_{G1S} 4.5 V					-	50	nA
Gate No. 2 Terminal Forward Current	I_{G2SSF}	V_{DS} V_{G1S} 0	V_{G2S} 6 V			50	-		-	nA
			V_{G2S} 4.5 V		-		-		50	nA
Gate No. 2 Terminal Reverse Current	I_{G2SSR}	V_{DS} V_{G1S} 0	V_{G2S} -6 V		-	50	-	-	-	nA
			V_{G2S} 4.5 V		-	-	-	-	50	nA
Zero-Bias Drain Current	I_{DS}	V_{DS} +15 V, V_{G1S} 0, V_{G2S} +4 V		0.5	8	15	0.5	8	20	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} +15 V I_D 10 mA V_{G2S} +4 V	f 1 kHz	-	12000	-	-	12000	-	μmho
Small Signal, Short Circuit Input Capacitance♦	C_{iss}		f 1 MHz		6	8.5		6	9	pF
Small Signal, Short Circuit, Reverse Transfer Capacitance (Drain to Gate No. 1)♦	C_{rss}			0.005	0.02	0.03	0.005	0.02	0.04	pF
Small Signal, Short Circuit Output Capacitance	C_{oss}				2	-	-	2	-	pF
Power Gain (see Fig. 6)	G_{PS}			14	17	-	-	-	-	dB
Noise Figure (see Fig. 6)	NF		f 200 MHz	-	4.5	6	-	-	-	dB
Conversion Gain	$G_{PS(C)}$		f 200/44 MHz		-	-	11	-	-	dB

♦ Capacitance between Gate No. 1 and all other terminals

♦ Three terminal measurement with Gate No. 2 and Source returned to guard terminal.



*Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in OD; 0.03 in ID, 0.063 in. thickness.

Q = 40820

▼ Disc ceramic.

* Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1: 1.8 – 8.7 pF variable air capacitor: E. F. Johnson Type 160-104, or equivalent.

C_2: 1.5 – 5 pF variable air capacitor: E. F. Johnson Type 160-102, or equivalent.

C_3: 1 – 10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8 – 4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in thick, 0.075-0.085 in wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.80 in.

L_2: 4-1/2 turns silver-plated 0.02 in. thick, 0.085-0.095 in wide, 5/16-in. ID Coil ≈ 0.90 in. long.

Fig.2 – 200 MHz power gain and noise figure test circuit for type 40820.

Table 1 – y parameters vs. frequency

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz) 50	100	200	250	UNITS
Y Parameters						
Input Conductance	g_{is}	0.08	0.33	1.0	1.6	mmho
Input Susceptance	b_{is}	1.8	3.6	7.5	9.8	mmho
Magnitude Forward Transadmittance	$\|Y_{fs}\|$	12	12	12	12.3	mmho
Angle of Forward Transadmittance	$<Y_{fs}$	–2	–13	–35	–45	degrees
Output Conductance	g_{os}	0.10	0.18	0.36	0.42	mmho
Output Susceptance	b_{os}	0.5	1.0	2.0	2.6	mmho
Magnitude of Reverse Transadmittance	$\|Y_{rs}\|$	8	12	25	40	μmho
Angle of Reverse Transadmittance	$<Y_{rs}$	–88	-73	–25	–10	degrees

Silicon Dual-Insulated Gate Field-Effect Transistor

N-Channel Depletion Type

With Integrated Gate-Protection Circuits

General-Purpose Economy Type for Applications from DC to 500 MHz

RCA-40841 is an n-channel silicon, depletion type, dual-insulated gate, field-effect transistor intended for general-purpose applications from DC to frequencies up to 500 MHz.

This MOS/FET provides excellent power gain, linear-circuit operation and has a wide dynamic operating range. Its square-law characteristics result in low cross-modulation performance over the AGC range. Its dual-gate construction reduces feedback capacitance by shielding Gate No. 1 from the drain, and makes it possible to isolate the local oscillator signal from the incoming signal by applying the two signals to separate gates. The very low feedback capacitance of this device eliminates the need for neutralization in circuits using the dual-gate configuration. Use of the device in the RF input stage of a receiver reduces local oscillator feed-through to the antenna. The 40841 requires negligible AGC power, provides automatic delay when AGC is applied to Gate No. 2, and exhibits slight input impedance variations during AGC functioning. The device has exceptionally high input impedance, an attribute for timing-circuit design.

Back-to-back diodes are fabricated on the same monolithic silicon pellet as the MOS/FET to protect the gates against damage due to electrostatic charges frequently encountered during normal handling. These back-to-back diodes also function as "transient trappers" by limiting in-circuit transient voltages that exceed ±10 volts.

Maximum ratings and electrical characteristics are included in the data for operation of the 40841 as the equivalent of a single-gate device. For single-gate operation, connect Gate No. 1 (Term. 2) to Gate No. 2 (Term. 3), as shown in the Terminal Diagrams on Page 2. The 40841 MOS/FET is hermetically sealed in the metal JEDEC TO-72 package.

Device Features:

- back-to-back diodes protect gate insulation against damage due to static changes frequently encountered during handling
- high forward transconductance: g_{fs} = 12,000 μmho (typ.)
- high power gain: G_{ps} = 32 dB (typ.) at 44 MHz
- gate leakage currents: I_{G1SS} and I_{G2SS} = 60 nA (max.) at T_A = 25°C
- high input impedance
- excellent thermal stability

Performance Features:

- superior cross-modulation performance and greater dynamic range than bipolar and junction-gate FETs
- wide dynamic range permits large-signal handling before overloading
- virtually no agc power required
- greatly reduced spurious responses in AM and FM receivers
- dual-gate configuration permits simplified AGC circuitry
- operates at frequencies to 500 MHz without neutralization in circuits utilizing the dual-gate configuration
- operates up to UHF with low-noise performance

The following dual-gate MOS/FET types are specified for applications requiring premimum-grade performance: 3N200, 3N187, 40673, 40819, 40820, 40821, 40822, and 40823.

Detailed information, utilizing RCA dual-gate protected MOS/FETs in RF applications, is given in the following RCA Application Notes: AN-4431 "RF Applications of the Dual-Gate MOS/FET up to 500 MHz" and AN-4018 "Design of Gate-Protected MOS Field-Effect Transistors".

Applications:

- DC amplifiers
- RF amplifiers
- mixers
- IF amplifiers
- video amplifiers
- differential amplifiers
- frequency multipliers
- phase splitters
- industrial timers — long time delays
- thyristor trigger circuits
- choppers
- voltage-controlled attenuators
- constant-current source
- voltage regulators
- telemetry & multiplex
- servo amplifiers
- proximity switches

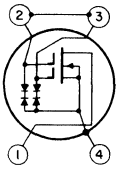
Maximum Ratings

	Dual-Gate Configuration	Single-Gate Configuration	
Absolute Maximum Values, at T_A = 25°C:			
Drain-to-Source Voltage, V_{DS}	−0.2 to +18	−0.2 to +18	V
Gate Terminal Current, I_{G1S} or I_{G2S}	±100	–	μA
Gate Terminal Current, I_{GS}	–	±100	μA
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+24	–	V
Drain-to-Gate Voltage, V_{DG}	–	+24	V
Drain Current, I_D	50	50	mA
Transistor Dissipation:			
At T_A up to 25°C	330	330	mW
At T_A above 25°C	derate linearly 2.2 mW/°C		
Ambient Temperature Range:			
Operating and Storage	−65 to +175	−65 to +175	°C
Lead Temperature (During Soldering):			
At distances 1/32 in from seating surface for 10 s max.	265	265	°C
Continuous Working Voltage#, at T_A = 25°C:			
Gate No. 1-to-Source Voltage, V_{G1S}	−4.5 to +3	–	V
Gate No. 2-to-Source Voltage, V_{G2S}	-4.5 to +4.5 or 40% of V_{DS} (whichever value is less)	–	V
Gate-to-Source Voltage, V_{GS}	–	−4.5 to +3	V
Drain-to-Gate Voltage, V_{DG1} or V_{DG2}	+20	–	V
Drain-to-Gate Voltage, V_{DG}	–	+20	V

#Continuous Working Voltage Ratings must be observed to maintain device characteristics. These ratings are based on long-term continuous voltage operation but may be exceeded for short durations (e.g. testing of device characteristics), provided the Absolute Maximum Ratings are not exceeded.

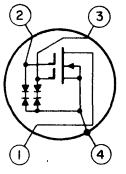
TERMINAL DIAGRAMS

SINGLE-GATE CONFIGURATION



LEAD 1—DRAIN
LEADS—2 AND 3—GATE
LEAD 4—SOURCE, SUBSTRATE AND CASE

DUAL-GATE CONFIGURATION



LEAD 1—DRAIN
LEAD 2—GATE No.2
LEAD 3—GATE No.1
LEAD 4—SOURCE SUBSTRATE AND CASE

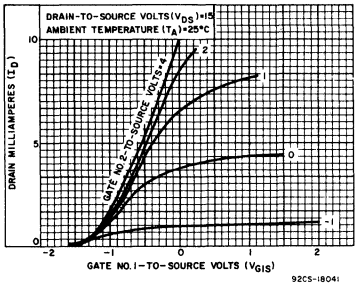


Fig.1—I_D vs. V_{G1S}.

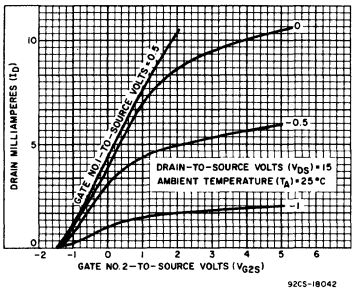


Fig.2—I_D vs. V_{G2S}.

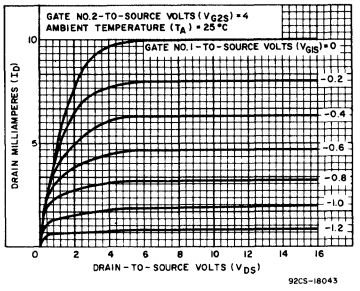


Fig.3—I_D vs. V_{DS}.

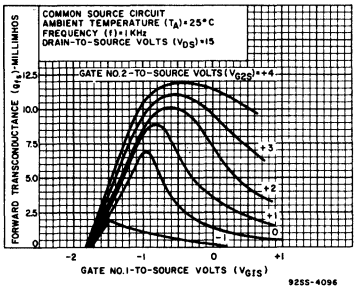
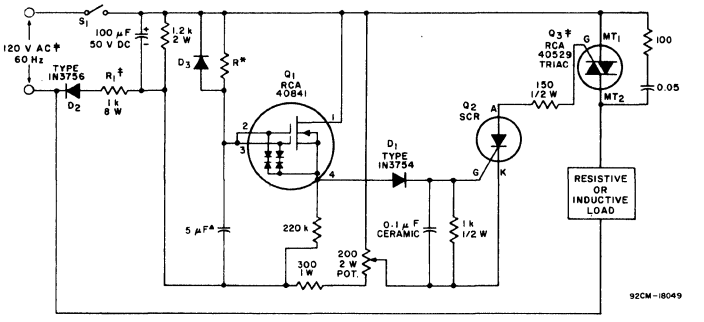


Fig.4—g_{fs} vs. V_{G1S}.

SOLID-STATE TIMER FOR INDUSTRIAL APPLICATIONS



▲ Cornell-Dubilier Electronics—Type MMW or equivalent.

• R controls duration of time delay. At R = 60 MΩ up to 5-minute delay (IRC resistor, Type CGH or equivalent)

‡ This circuit can also be used at supply voltages of 240 V AC and 24V AC (60Hz) by changing the values of R1 and Q3.

TIMING CIRCUIT CHARACTERISTICS

T_A = −25°C to +60°C

Accuracy: ±10% (over temperature)

Repeatability: ±3% (at 25°C)

Reset Time: Less than 150 ms

Q2: V_{DRM} = 60V
I_{GT} = 200μA
I_T = 0.8A

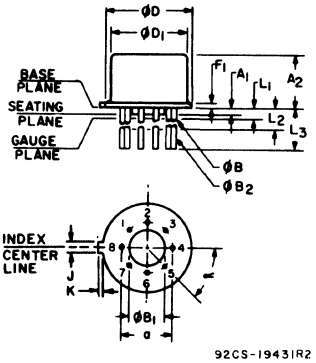
D3: I_R = 1 nA
V_R = 60V

Fig.12—Typical timing circuit utilizing the 40841 in a single-gate configuration.

Dimensional Outlines

TO–5 STYLE PACKAGES

(T) Suffix (JEDEC MO-002-AL) 8-Lead TO-5 Style

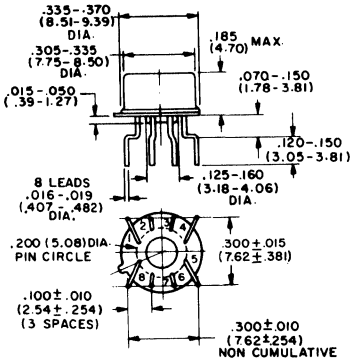


SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.200 TP		2	5.88 TP	
A_1	0.010	0.050		0.26	1.27
A_2	0.165	0.185		4.20	4.69
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0.125	0.160		3.18	4.06
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	45° TP			45° TP	
N	8		6	8	
N_1	3		5	3	

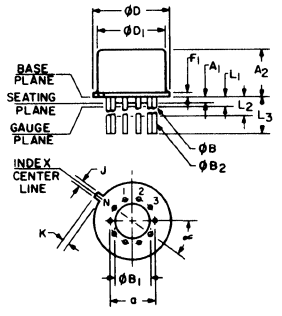
NOTES

1. Refer to JEDEC Publication No 95 for Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radium of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

(S) Suffix 8-Lead TO-5 Style with Dual-In-Line Formed Leads (DIL-CAN)



(T) Suffix (JEDEC MO-006-AF) 10-Lead TO-5 Style



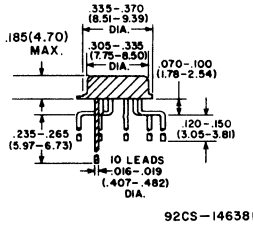
SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
a	0.230 TP		2	5.84 TP	
A_1	0	0		0	0
A_2	0.165	0.185		4.19	4.70
øB	0.016	0.019	3	0.407	0.482
$øB_1$	0	0		0	0
$øB_2$	0.016	0.021	3	0.407	0.533
øD	0.335	0.370		8.51	9.39
$øD_1$	0.305	0.335		7.75	8.50
F_1	0.020	0.040		0.51	1.01
j	0.028	0.034		0.712	0.863
k	0.029	0.045	4	0.74	1.14
L_1	0.000	0.050	3	0.00	1.27
L_2	0.250	0.500	3	6.4	12.7
L_3	0.500	0.562	3	12.7	14.27
α	36° TP			36° TP	
N	10		6	10	
N_1	1		5	1	

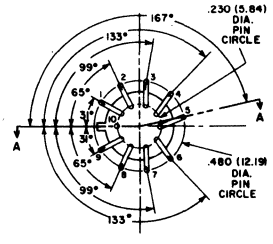
NOTES:

1. Refer to Rules for Dimensioning Axial Lead Product Outlines.
2. Leads at gauge plane within 0.007" (0.178 mm) radius of True Position (TP) at maximum material condition.
3. øB applies between L_1 and L_2. $øB_2$ applies between L_2 and 0.500" (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70 mm).
4. Measure from Max. øD.
5. N_1 is the quantity of allowable missing leads.
6. N is the maximum quantity of lead positions.

92CS-15835

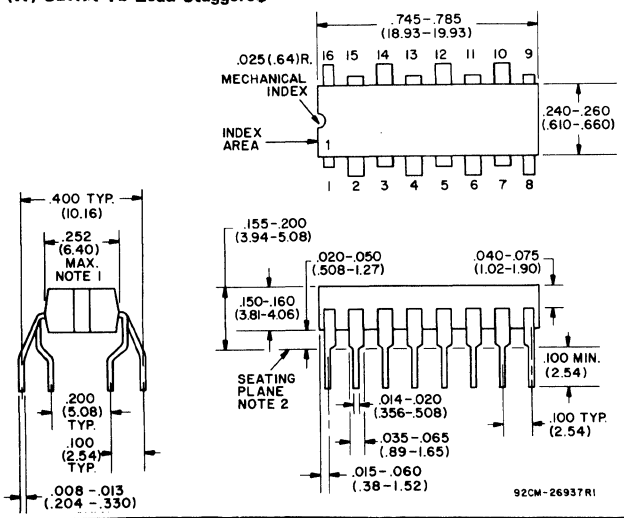
(V) Suffix 10 Formed Leads Radially Arranged TO-5 Type



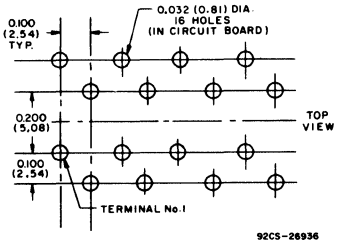


QUAD IN-LINE PACKAGES (Cont'd)

(W) Suffix 16-Lead Staggered



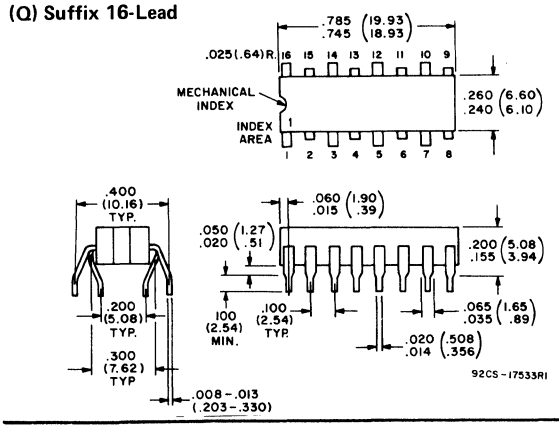
Recommended Mounting – Hole Dimensions and Spacing



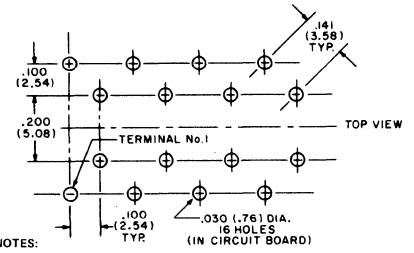
NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

(Q) Suffix 16-Lead



Recommended Mounting – Hole Dimensions and Spacing

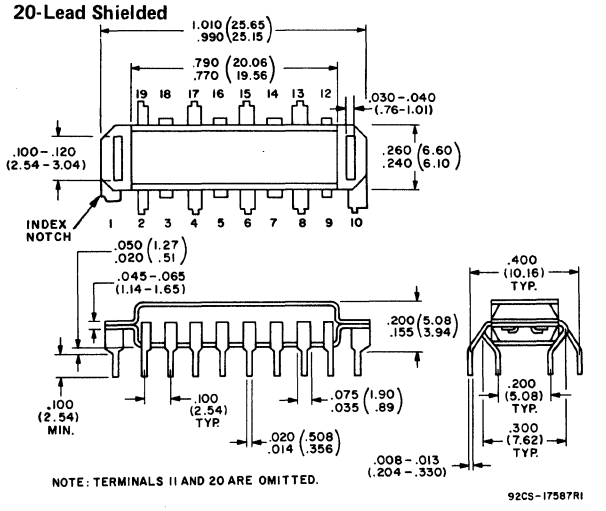


NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

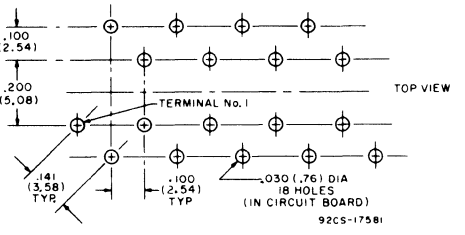
Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

92CS-17580

20-Lead Shielded



Recommended Mounting – Hole Dimensions and Spacing

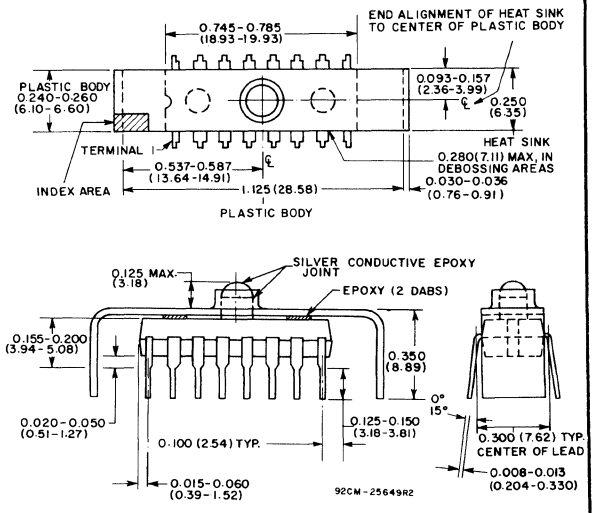


NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

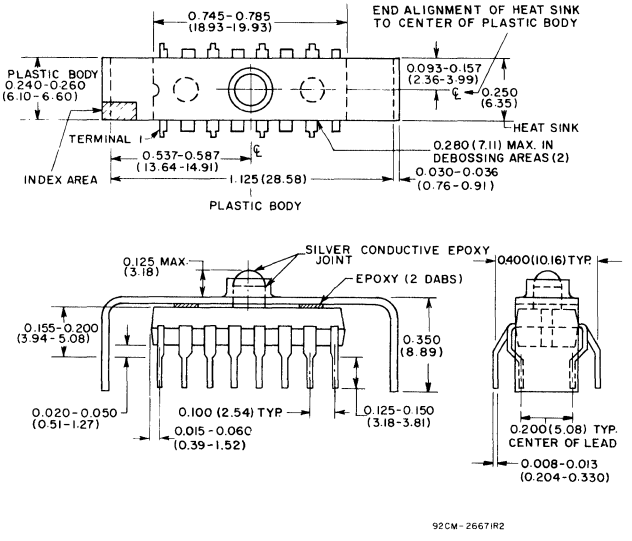
Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

DUAL-IN-LINE AND QUAD-IN-LINE PLASTIC PACKAGES
(Power Stud and Heat-Sink Types)

(EM) Suffix
16-Lead with Integral Strap Heat Sink

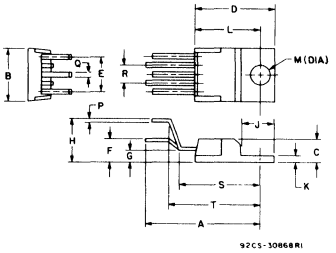


(QM) Suffix
16-Lead Staggered with Integral Strap Heat Sink



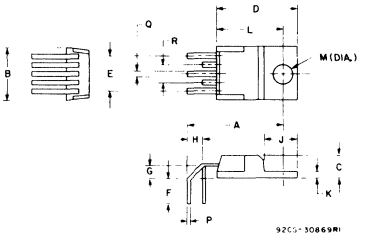
TO-220-STYLE (VERSA-V) PLASTIC PACKAGE

VERTICAL MOUNT



SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.876	0.896	22.25	22.75
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.168	0.188	4.268	4.775
G	0.100	0.104	2.540	2.641
H	0.320	0.340	8.128	8.638
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530
S	0.600	0.630	15.24	16.00
T	0.680	0.710	17.27	18.03

HORIZONTAL MOUNT (M Suffix)



SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.726	0.746	18.44	18.94
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.221	0.251	5.614	6.375
G	0.100	0.104	2.540	2.641
H	0.143	0.163	3.633	4.140
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530

Application Notes

Because the published y_{rs} value for the 3N200 is very small, the circuit y_{rs} values may differ significantly from the y_{rs} values shown in Table 1 and hence, may result in an unstable operating condition. It is impossible to provide data for all possible mounting combinations, therefore, a recommended mounting arrangement is shown in Fig. 2. The source and substrate in the TO-72 package of the 3N200 are internally connected to lead No. 4 and the case. The source-lead inductance can be reduced, if the case is used as the source connection. Fig. 2 illustrates a partial component layout in which the case is held by a clamp or other fingered device. The clamp is soldered to a feedthrough capacitor to provide an effective, very-low inductance bypass to RF signals. This mounting arrangement still permits the use of a source resistor for DC stability, and enables the case to provide isolation between the input and output circuit in addition to the isolation afforded by the shield.

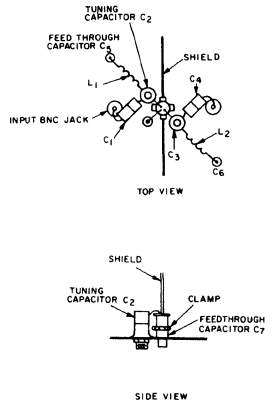


Fig. 2 – Partial component layout of 400-MHz amplifier circuit

The reduction of source-lead inductance provides in addition to greater stability, a lower input and output conductance. Table 2 shows the differences in "y" parameter values at 400 MHz when measured with the source connection made to lead No. 4 (in accordance with the published data for the 3N200) and when measured with the case connected directly to the ground plane of the test jig. The magnitude of reverse transadmittance is halved with a significant change in its phase angle. The input conductance is reduced by 30%, and the output conductance is reduced by 13%. A recalculation of the expressions for MAG, MUG, and Linvill Criteria (C) shows a significant improvement in gain and circuit stability.

While it is difficult to provide accurate information on the effects of shielding between the input and output circuits, its effect can be demonstrated when all other feedback components have been reduced to negligible values. The circuit, shown in Fig. 3 (for component layout see Fig. 2), was measured both with and without a shield. The maximum gain, without the shield, averaged 0.8 dB lower than with the use of the shield.

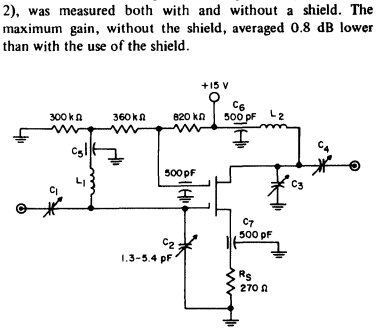


Fig. 3 – 400-MHz amplifier circuit

When receiver sensitivity is an important consideration in the design of an RF amplifier, a compromise must be made in the circuit power gain to achieve a lower noise factor. A contour plot of noise figure as a function of generator source admittance is shown in Fig. 4. Each contour is a plot of noise figure as a function of the generator source conductance and susceptance. Data for the noise figure were obtained from a test amplifier designed with very low feedback. Even though the area of very low-noise figure in the curves in Fig. 4 cover a broad range of source admittance, impedance-matching for maximum power gain could result in

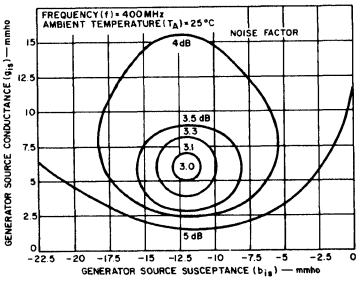


Fig. 4 – Noise factor vs. generator source (input) admittance (y_{is})

a relatively poor noise figure. As shown in Table 2, the input conductance (g_{is}) with the case grounded is 2.5 mmho. With the reactive portion tuned out, the noise factor at power matched conditions is almost 1 dB higher than the optimum noise figure. However, matching to 5.0 mmho results in a near optimum noise factor with a loss of only 0.5 dB in gain. In addition, impedance matching to high conductance also benefits crossmodulation performance, as will be discussed in a later section.

Gate Protection Diodes

The diodes incorporated into RCA dual-gate MOS FETs, for gate protection, have been designed to minimize RF loading on the input circuits. The small amount of RF loading results in only a fraction of a dB loss in power gain and a negligible increase in the noise figure. The advantages of diode protection, greatly outweigh the slight loss in power gain, especially in an RF amplifier intended for the input stage of a receiver.

In addition to the protection afforded in normal handling, the diodes also provide in-circuit protection against events such as: static discharge due to contact with the antenna, delay in transmit-receive switching, or connection of an antenna with an accumulated charge to the receiver.

Crossmodulation

Crossmodulation is an important consideration because it is an inherent device characteristic where circuit considerations are secondary. Crossmodulation is the transfer of modulation from an undesired signal on a desired signal caused by the non-linear characteristics of a device.

Crossmodulation is proportional to the third-order term of the expansion of the I_D - V_{GS} curve. It is normally specified as the undesired signal voltage required to produce a crossmodulation factor of 0.01. The crossmodulation factor is defined as the percent modulation on a desired carrier by the modulated undesired signal divided by the percent modulation of the undesired signal.[4]

Inspection of the I_D - V_{G1S} curve of Fig. 5 offers an insight to the possible crossmodulation as a function of gain-reduction performance. When both channels of the 3N200 are fully conducting current, as shown by the V_{G2S} = 4-volt curve, the device approximately follows a square-law characteristic. If the I_D - V_{G1S} curve was ideal, the third-order term would be zero; but in practical cases, the third-order term and crossmodulation have some low values.

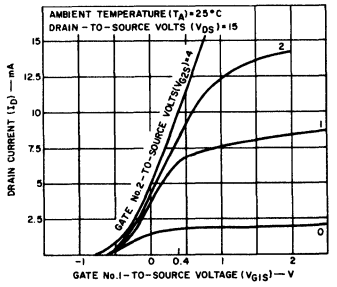


Fig. 5 – Drain current (I_D) vs. gate No. 1-to-source voltage (V_{G1S})

CHARACTERISTICS	SYMBOL	FREQUENCY (f) = 400 MHz		UNITS
		Normal Connection	Case Grounded	
Maximum Available Power Gain	MAG	13.0	15.7	dB
Maximum Usable Power Gain (unneutralized)	MUG	13.8	19.4	dB
Linvill Stability Factor, C	C	0.615	0.335	mmho
"y" Parameters				
Input Conductance	g_{is}	3.6	2.5	mmho
Input Susceptance	b_{is}	11.2	11.7	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	15.5	15.5	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	-47.0	-40.0	degrees
Output Conductance	g_{os}	0.8	0.65	mmho
Output Susceptance	b_{os}	4.25	4.25	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs} \rvert$	0.14	0.07	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	14.0	49.0	degrees

Table 2 – "y" Parameters at 400 MHz with source connection to lead No. 4 and with case connected to ground plane of test jig

Some Applications of a Programmable Power/Switch Amplifier

by L. R. Campbell and H. A. Wittlinger

The RCA-CA3094 unique monolithic programmable power switch/amplifier IC consists of a high-gain preamplifier driving a power-output amplifier stage. It can deliver average power of 3 watts or peak power of 10 watts to an external load, and can be operated from either a single or dual power supply. This Note briefly describes the characteristics of the CA3094, and illustrates its use in the following circuit applications:

Class A instrumentations and power amplifiers

Class A driver-amplifier for complementary power transistors

Wide-frequency-range power multivibrators

Current- or voltage-controlled oscillators

Comparators (threshold detectors)

Voltage regulators

Analog timers (long time delays)

Alarm systems

Motor-speed controllers

Thyristor-firing circuits

Battery-charger regulator circuits

Ground-fault-interrupter circuits

Circuit Description

The CA3094 series of devices offers a unique combination of circuit flexibility and power-handling capability. Although these monolithic IC's dissipate only a few microwatts when quiescent, they have a high current-output capability (100 milliamperes average, 300 milliamperes peak) in the active state, and the premium-grade devices can operate at supply voltages up to 44 volts.

Fig. 1 shows a schematic diagram of the CA3094. The portion of the circuit preceding transistors Q_{12} and Q_{13} is the preamplifier section and is generically similar to that of the RCA-CA3080 Operational Transconductance Amplifier (OTA).[1,2] The CA3094 circuits can be gain-programmed by either digital and/or analog signals applied to a separate Amplifier-Bias-Current (I_{ABC}) terminal (No. 5 in Fig. 1) to control circuit sensitivity. Response of the amplifier is essentially linear as a function of the current at terminal 5. This additional signal input "port" provides added flexibility in many applications. Thus, the output of the amplifier is a function of input signals applied differentially at terminals 2 and 3 and/or in a single-ended configuration at terminal 5. The output portion of the monolithic circuit in the CA3094 consists of a Darlington-connected transistor pair with access provided to both the collector and emitter terminals to provide capability to "sink" and/or "source" current.

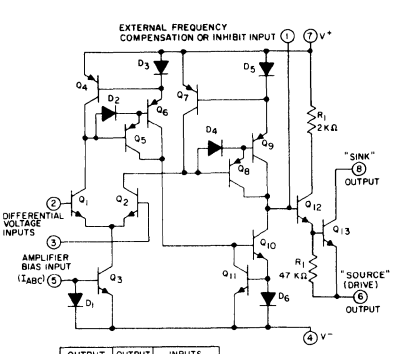


Fig. 1–CA3094 circuit schematic diagram.

The CA3094 series of circuits consists of six types that differ only in voltage-handling capability and package options, as shown below; other electrical characteristics are identical.

Package Options	Maximum Voltage Rating
CA3094S; CA3094T	24 V
CA3094AS; CA3094AT	36 V
CA3094BS; CA3094BT	44 V

The suffix "S" indicates circuits packaged in TO-5 enclosures with leads formed to an 8-lead dual-in-line configuration (0.1" pin spacing). The suffix "T" indicates circuits packaged in 8-lead TO-5 enclosures with straight leads. The generic CA3094 type designation is used throughout this Note.

Class A Instrumentation Amplifiers

One of the more difficult instrumentation problems frequently encountered is the conversion of a differential input signal to a single-ended output signal. Although this conversion can be accomplished in a straightforward design through the use of classical op-amps, the stringent matching requirements of resistor ratios in feedback networks make the conversion particularly difficult from a practical standpoint. Because the gain of the preamplifier section in the CA3094 can be defined as the product of the transconductance and the load resistance ($g_m R_L$), feedback is not needed to obtain predictable open-loop gain performance. Fig. 2 shows the CA3094 in this basic type of circuit.

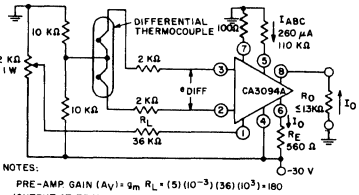


Fig. 2–Open-loop instrumentation amplifier with differential input and single-ended output.

The gain of the preamplifier section (to terminal No. 1) is $g_m R_L = (5 \times 10^{-3})(36 \times 10^3) = 180$. The transconductance g_m is a function of the current into terminal No. 5, I_{ABC}, the amplifier-bias-current. In this circuit an I_{ABC} of 260 microamperes results in a g_m of 5 millimhos. The operating point of the output stage is controlled by the 2-kilohm potentiometer. With no differential input signal (e_{diff} = 0), this potentiometer is adjusted to obtain a quiescent output current I_O of 12 milliamperes. This output current is established by the 560-ohm emitter resistor, R_E, as follows:

$$I_O \approx \frac{(g_m R_L)(e_{diff})}{R_E}$$

Under the conditions described, an input swing e_{diff} of ±26 millivolts produces a variation in the output current I_O of ±8.35 milliamperes. The nominal quiescent output voltage is 12 milliamperes times 560 ohms or 6.7 volts. This output level drifts approximately –4 millivolts, or –0.0595 per cent, for each °C change in temperature. Output drift is caused by temperature-induced variations in the base-emitter voltage of the two output transistors, Q_{12} and Q_{13}.

Fig. 3 shows the CA3094 used in conjunction with a resistive-bridge input network; and Fig. 4 shows a single-supply amplifier for thermocouple signals. The RC networks* connected between terminals 1 and 4 in Figs. 3 and 4 provide compensation to assure stable operation.

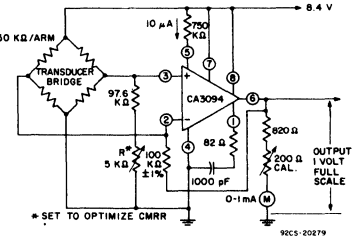


Fig. 3–Single-supply differential-bridge amplifier.

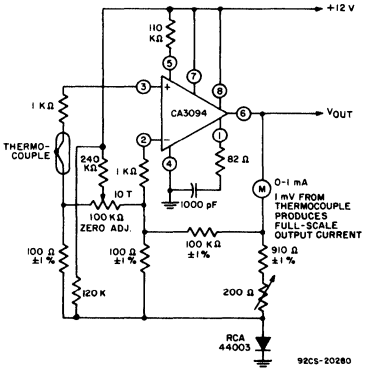


Fig. 4–Single-supply amplifier for thermocouple signals.

Class A Power Amplifiers

The CA3094 is attractive for power-amplifier service because the output transistor can control current up to 100 milliamperes (300 milliamperes peak), the premium devices (CA3094B) can operate at supply voltages up to 44 volts, and the TO-5 package can dissipate power up to 1.6 watts when equipped with a suitable heat sink that limits the case temperature to 55°C.

Fig. 5 shows a Class A amplifier circuit using the CA3094A that is capable of delivering 280 milliwatts to a 350-ohm resistive load. This circuit has a voltage gain of 60 dB and a 3-dB bandwidth of about 50 kHz. Operation is stable without the use of a phase-compensation network. Potentiometer R is used to establish the quiescent operating point for class A operation.

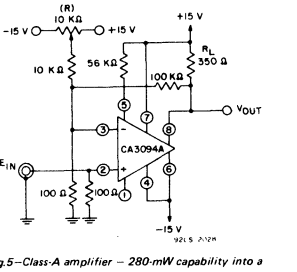


Fig. 5–Class-A amplifier – 280-mW capability into a resistive load.

*The components of the RC network are chosen so that

$$\frac{1}{2\pi RC} \approx 2 \text{ MHz}.$$

excess of 10 watts when used in this type of circuit. The frequency of oscillation f_{OSC} is determined by the resistor ratios, as follows:

$$f_{OSC} = \frac{1}{2RC\ln[(2R_1/R_2)+1]}$$

where $$R1 = \frac{R_A R_B}{R_A + R_B}$$

Provisions can easily be made in the circuit of Fig. 11 to vary the multivibrator pulse length while maintaining an essentially constant pulse repetition rate. The circuit shown in Fig. 12 incorporates a potentiometer Rp for varying the width of pulses generated by the astable multivibrator to drive a light-emitting diode (LED).

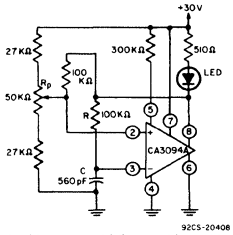


Fig.12—Astable power multivibrator with provisions for varying duty cycle.

Fig. 13 shows a circuit incorporating independent controls (R_{ON} and R_{OFF}) to establish the "on" and "off" periods of the current supplied to the LED. The network between points "A" and "B" is analogous in function to that of the 100-kilohm resistor R in Fig. 12.

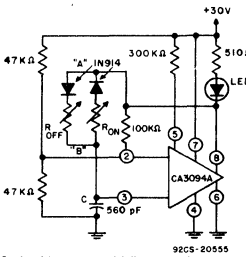


Fig.13—Astable power multivibrator with provisions for independent control of LED "on-off" periods.

The CA3094 is also suitable for use in monostable multivibrators, as shown in Fig. 14. In essence, this circuit is a pulse counter in which the duration of the output pulses is independent of trigger-pulse duration. The meter reading is a function of the pulse repetition rate which can be monitored with the speaker.

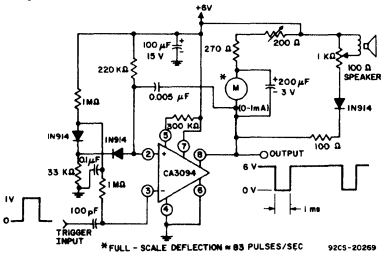


Fig.14—Power monostable multivibrator.

Current- or Voltage-Controlled Oscillators

Because the transconductance of the CA3094 varies linearly as a function of the amplifier bias current (I_{ABC}) supplied to terminal 5, the design of a current- or voltage-controlled oscillator is straightforward, as shown in Fig. 15. Fig. 16 and 17 show oscillator frequency as a function of I_{ABC} for a current-controlled oscillator for two different values of capacitor C in Fig. 15. The addition of an appropriate resistor (R) in series with terminal 5 in Fig. 15 converts the circuit into a voltage-controlled oscillator. Linearity with respect to either current or voltage control is within 1 per cent over the middle half of the characteristics. However, variation in the symmetry of the output pulses as a function of frequency is an inherent characteristic of the circuit in Fig. 15, and leads to distortion when this circuit is used to drive the phase detector in phase-locked-loop applications. This type of distortion can be eliminated by interposing an appropriate flip-flop between the output of the oscillator and the phase-locked discriminator circuits.

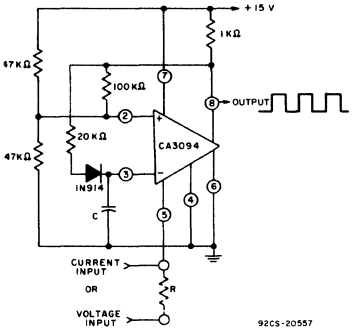


Fig.15—Current- or voltage-controlled oscillator.

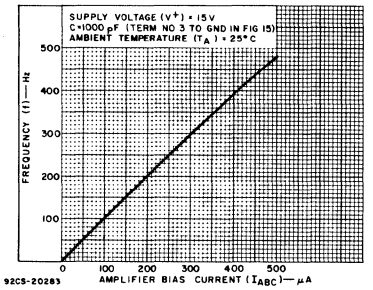


Fig.16—Frequency as a function of I_{ABC} for C=1000 pF for circuit in Fig. 15.

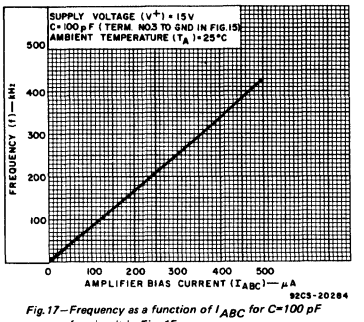


Fig.17—Frequency as a function of I_{ABC} for C=100 pF for circuit in Fig. 15.

Comparators (Threshold Detectors)

Comparator circuits are easily implemented with the CA3094, as shown by the circuits in Fig. 18. The circuit of Fig. 18(a) is arranged for dual-supply operation; the input voltage exceeds the positive threshold, the output voltage swings essentially to the negative supply-voltage rail (it is assumed that there is negligible resistive loading on the output terminal). An input voltage that exceeds the negative threshold value results in a positive voltage output essentially equal to the positive supply voltage. The circuit in Fig. 18(b), connected for single-supply operation, functions similarly.

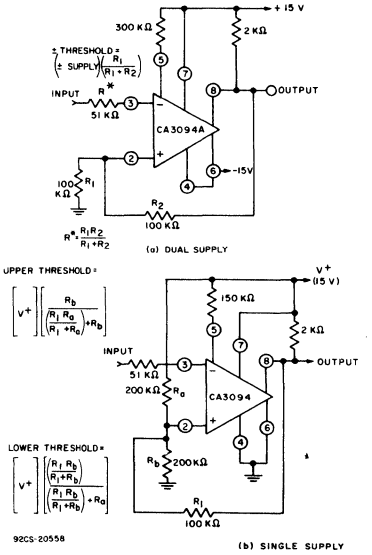


Fig.18—Comparators (threshold detectors) — dual- and single-supply types.

Fig. 19 shows a dual-limit threshold detector circuit in which the high-level limit is established by potentiometer R1

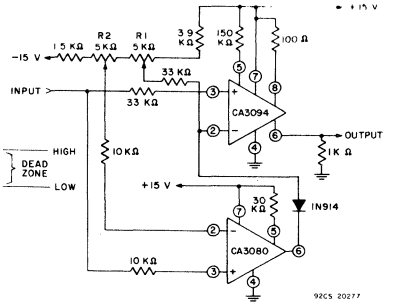


Fig.19—Dual-limit threshold detector.

and the low-level limit is set by potentiometer R2 to actuate the CA3080 low-limit detector.[1,2] A positive output signal is delivered by the CA3094 whenever the input signal exceeds either the high-limit or the low-limit values established by the appropriate potentiometer settings. This output voltage is approximately 12 volts with the circuit shown.

The high current-handling capability of the CA3094 makes it useful in Schmitt power-trigger circuits such as that shown in Fig. 20. In this circuit, a relay coil is switched whenever the

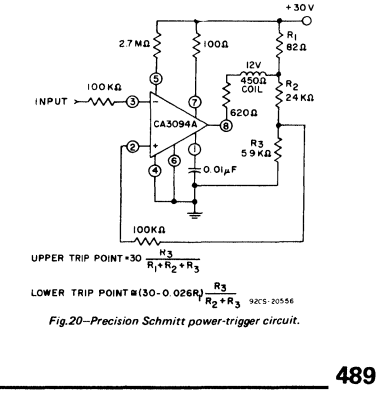


Fig.20—Precision Schmitt power-trigger circuit.

Alarm Circuit

Fig. 25 shows an alarm circuit utilizing two "sensor" lines. In the "no-alarm" state, the potential at terminal 2 is lower than the potential at terminal 3, and terminal 5 (I_{ABC}) is driven with sufficient current through resistor R_5 to keep the output voltage "high". If either "sensor" line is opened, shorted to ground, or shorted to the other sensor line, the output goes "low" and activates some type of alarm system. The back-to-back diodes connected between terminals 2 and 3 protect the CA3094 input terminals against excessive differential voltages.

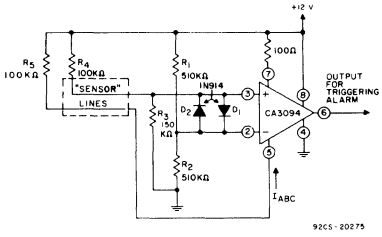


Fig.25–Alarm system.

Motor-Speed Controller System

Fig. 26 illustrates the use of the CA3094 in a motor-speed controller system. Circuitry associated with rectifiers D_1 and D_2 comprises a full-wave rectifier which develops a train of half-sinusoid voltage pulses to power the dc motor. The motor speed depends on the peak value of the half-sinusoids and the period of time (during each half-cycle) the SCR is conductive.

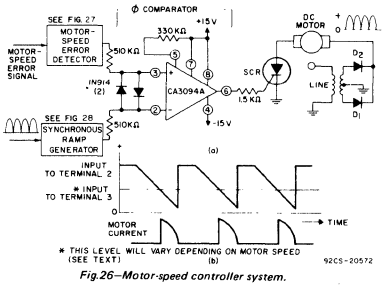


Fig.26–Motor-speed controller system.

The SCR conduction, in turn, is controlled by the time duration of the positive signal supplied to the SCR by the phase comparator. The magnitude of the positive dc voltage supplied to terminal 3 of the phase comparator depends on motor-speed error as detected by a circuit such as that shown in Fig. 27. This dc voltage is compared to that of a fixed-amplitude ramp wave generated synchronously with the ac-line-voltage frequency. The comparator output at terminal 6 is "high" (to trigger the SCR into conduction) during the period when the ramp potential is less than that of the error voltage on terminal 3. The motor-current conduction period is increased as the error voltage at terminal 3 is increased in the positive direction. Motor-speed accuracy of ±1 per cent is easily obtained with this system.

Motor-Speed Error Detector. Fig. 27(a) shows a motor-speed error detector suitable for use with the circuit of Fig. 26. A CA3080 operational transconductance amplifier is used as a voltage comparator. The reference for the comparator is established by setting the potentiometer R so that the voltage at terminal 3 is more positive than that at terminal 2 when the motor speed is too low. An error voltage E_1 is derived from a tachometer driven by the motor. When the motor speed is too low, the voltage at terminal 2 of the voltage comparator is less positive than that at terminal 3, and the output voltage at terminal 6 goes "high". When the motor speed is too high, the opposite input conditions exist, and the output voltage at terminal 6 goes "low". Fig. 27(b) also shows these conditions graphically, with a linear transition region between the "high" and "low" output levels. This linear transition region is known as "proportional bandwidth". The slope of this region is determined by the proportional bandwidth control to establish the error-correction response time.

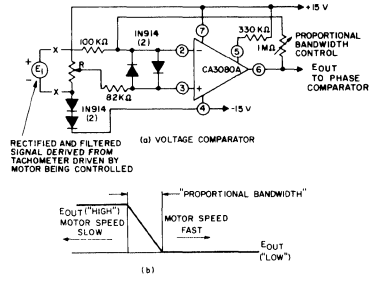


Fig. 27–Motor speed error detector.

Synchronous Ramp Generator. Fig. 28 shows a schematic diagram and signal waveforms for a synchronous ramp generator suitable for use with the motor-controller circuit of Fig. 26. Terminal 3 is biased at approximately +2.7 volts (above the negative supply voltage). The input signal E_{IN} at terminal 2 is a sample of the half-sinusoids (at line frequency) used to power the motor in Fig. 26. A synchronous ramp signal is produced by using the CA3094 to charge and discharge capacitor C_1 in response to the synchronous toggling of E_{IN}.

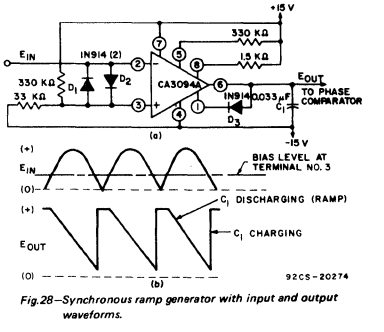


Fig.28–Synchronous ramp generator with input and output waveforms.

The charging current for C_1 is supplied by terminal 6. When terminal 2 swings more positive than terminal 3, transistors Q_{12} and Q_{13} in the CA3094 (Fig. 1) lose their base drive and become non-conductive. Under these conditions, C_1 discharges linearly through the external diode D_3 and the Q_{10}, D_6 path in the CA3094 to produce the ramp wave. The E_{out} signal is supplied to the phase comparator in Fig. 26.

Thyristor Firing Circuits

Temperature Controller. In the temperature control system shown in Fig. 29, the differential input of the CA3094 is connected across a bridge circuit comprised of a PTC (positive-temperature-coefficient) temperature sensor, two 75-kilohm resistors, and an arm containing the temperature set control. When the temperature is "low", the resistance of the PTC-type sensor is also low; therefore, terminal 3 is more positive than terminal 2 and an output current from terminal 6 of the CA3094 drives the triac into conduction. When the temperature is "high", the input conditions are reversed and the triac is cut off. Feedback from terminal 8 provides hysteresis to the control point to prevent rapid cycling of the system. The 1.5-kilohm resistor between terminal 8 and the positive supply limits the triac gate current and develops the voltage for the hysteresis feedback. The excellent power-supply-rejection and common-mode-rejection ratios of the CA3094 permit accurate repeatability of control despite appreciable power-supply ripple. The circuit of Fig. 29 is equally suitable for use with NTC (negative-temperature-coefficient) sensors provided the positions of the sensor and the associated resistor R are interchanged in the circuit. The diodes connected back-to-back across the input terminals of the CA3094 protect the device against excessive differential input signals.

Thyristor Control from AC-Bridge Sensor. Fig. 30 shows a line-operated thyristor-firing circuit controlled by a CA3094 that operates from an ac-bridge sensor. This circuit is particularly suited to certain classes of sensors that cannot be operated from dc. The CA3094 is inoperative when the high side of the ac line is negative because there is no I_{ABC} supply to terminal 5. When the sensor bridge is unbalanced so that terminal 2 is more positive than terminal 3, the output stage of the CA3094 is cut off when the ac line swings positive, and the output level at terminal 8 of the CA3094 goes "high". Current from the line flows through the 1N3193 diode to charge the 100-microfarad reservoir capacitor, and also provides current to drive the triac into conduction. During the succeeding negative swing of the ac line, there is sufficient remanent energy in the reservoir capacitor to maintain conduction in the triac.

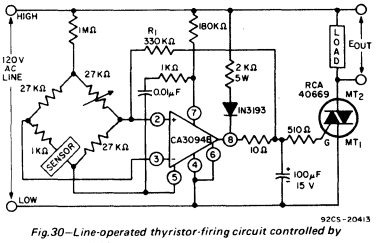


Fig.30–Line-operated thyristor-firing circuit controlled by ac-bridge sensor.

When the bridge is unbalanced in the opposite direction so that terminal 3 is more positive than terminal 2, the output of the CA3094 at terminal 8 is driven sufficiently "low" to "sink" the current supplied through the 1N3193 diode so that the triac gate cannot be triggered. Resistor R_1 supplies the hysteresis feedback to prevent rapid cycling between turn-on and turn-off.

Battery-Charger Regulator Circuit

The circuit for a battery-charger regulator circuit using the CA3094 is shown in Fig. 31. This circuit accurately limits the peak output voltage to 14 volts, as established by the zener

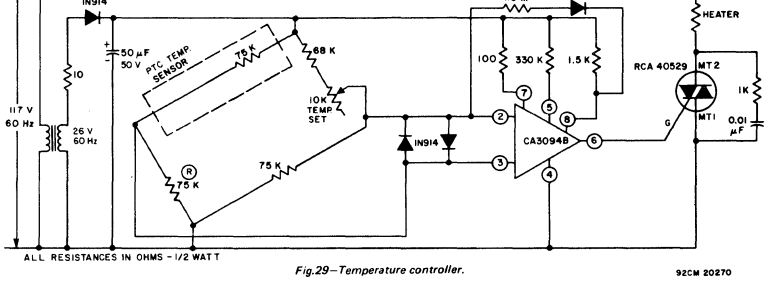


Fig.29–Temperature controller.

An IC Operational-Transconductance-Amplifier (OTA) With Power Capability

by L. Kaplan and H. Wittlinger

In 1969, RCA introduced the first triple operational-transconductance-amplifier or OTA. The wide acceptance of this new circuit concept prompted the development of the single, highly linear operational-transconductance-amplifier, the CA3080. Because of its extremely linear transconductance characteristics with respect to amplifier bias current, the CA3080 gained wide acceptance as a gain-control block. The CA3094 improved on the performance of the CA3080 through the addition of a pair of transistors; these transistors extended the current-carrying capability to 300 milliamperes, peak. This new device, the CA3094, is useful in an extremely broad range of circuits in consumer and industrial applications; this paper describes only a few of the many consumer applications.

WHAT IS AN OTA?

The OTA, operational-transconductance-amplifier, concept is as basic as the transistor; once understood, it will broaden the designer's horizons to new boundaries and make realizable designs that were previously unobtainable. Fig. 1 shows an equivalent diagram of the OTA. The differential input circuit is the same as that found on many modern operational amplifiers. The remainder of the OTA is composed of current mirrors as shown in Fig. 2. The geometry of these mirrors is such that the current gain is unity. Thus, by highly degenerating the current mirrors, the output current is precisely defined by the differential-input amplifier. Fig. 3 shows the output-current transfer-characteristic of the amplifier. The shape of this characteristic remains

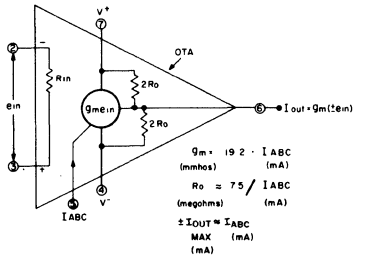


Fig. 1– Equivalent diagram of the OTA.

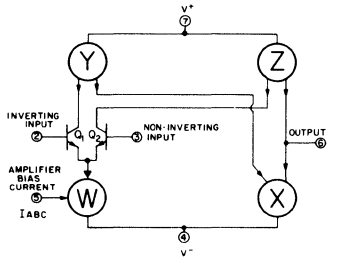


Fig. 2– Current mirrors W, X, Y, and Z used in the OTA.

constant and is independent of supply voltage. Only the maximum current is modified by the bias current.

The major controlling factor in the OTA is the input amplifier bias current I_{ABC}; as explained in Fig. 1, the total output current and gm are controlled by this current. In addition, the input bias current, input resistance, total supply current, and output resistance are all proportional to this amplifier bias current. These factors provide the key to the performance of this most flexible device, an idealized

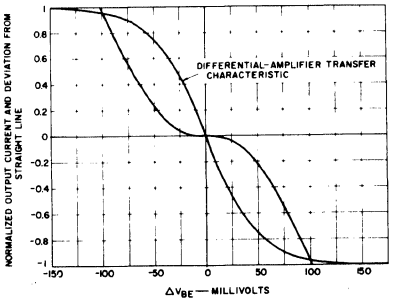


Fig. 3– The output-current transfer-characteristic of the OTA is the same as that of an idealized differential amplifier.

differential amplifier, i.e., a circuit in which differential input to single-ended output conversion can be realized. With this knowledge of the basics of the OTA, it is possible to explore some of the applications of the device.

DC Gain Control

The methods of providing dc gain-control functions are numerous. Each has its advantage – simplicity, low cost, high level control, low distortion. Many manufacturers who have nothing better to offer propose the use of a four-quadrant multiplier. This is analogous to using an elephant to carry a twig. It may be elegant but it takes a lot to keep it going! When operated in the gain-control mode, one input of the standard transconductance multiplier is offset so that only one half of the differential input is used; thus, one-half of the multiplier is being thrown away.

The OTA, while providing excellent linear amplifier characteristics, does provide a simple means of gain control. For this application the OTA may be considered the realization of the ideal differential amplifier in which the full differential amplifier gm is converted to a single-ended output. Because the differential amplifier is ideal, its gm is directly proportional to the operating current of the differential-amplifier; in the OTA the maximum output current is equal to the amplifier bias current I_{ABC}. Thus, by varying the amplifier bias current, the amplifier gain may be varied: $A = G_m R_L$ where R_L is the output load resistance. Fig. 4 shows the basic configuration of the OTA dc gain-control circuit.[1]

As long as the differential input signal to the OTA remains under 50-millivolts peak-to-peak, the deviation from a linear transfer will remain under 5 percent. Of course, the total harmonic distortion will be considerably less than this value. Signal excursions beyond this point only result in an undesired "compressed" output. The reason for this compression can be seen in the transfer characteristic of the differential amplifier in Fig. 3. Also shown in Fig. 3 is a curve depicting the departure from a linear line of this transfer characteristic.

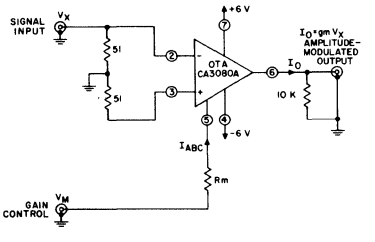


Fig. 4– Basic configuration of the OTA dc gain-control circuit.

The actual performance of the circuit shown in Fig. 4 is plotted in Fig. 5. Both signal-to-noise ratio and total harmonic distortion are shown as a function of signal input. Figs. 5(b) and (c) show how the signal-handling capability of the circuit is extended through the connection of diodes on

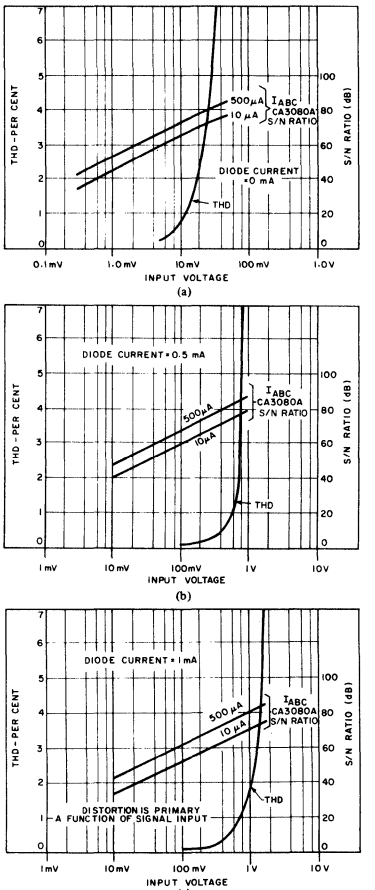


Fig. 5– Performance curves for the circuits of Figs. 4 and 6.

the input as shown in Fig. 6.[2] Fig. 7 shows total system gain as a function of amplifier bias current for several values of diode current. Fig. 8 shows an oscilloscope photograph of the CA3080 transfer characteristic as applied to the circuit of Fig. 4. The oscilloscope photograph of Fig. 9 was obtained with the circuit shown in Fig. 6. Note the improvement in

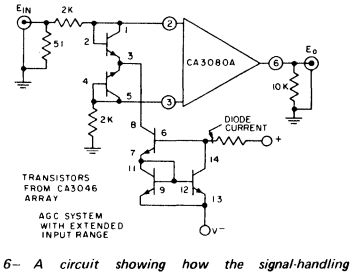


Fig. 6– A circuit showing how the signal-handling capability of the circuit of Fig. 4 can be extended through the connection of diodes on the input.

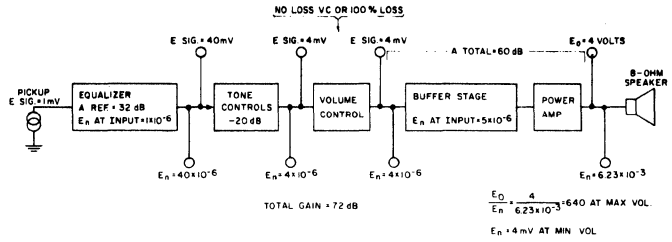


Fig. 12– Block diagram of a system using a "losser"-type tone-control circuit.

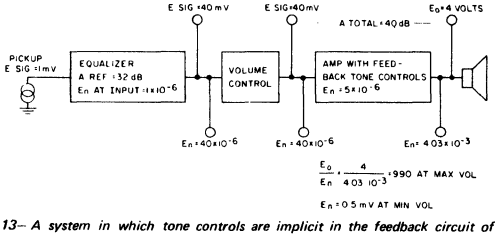


Fig. 13– A system in which tone controls are implicit in the feedback circuit of the power amplifier.

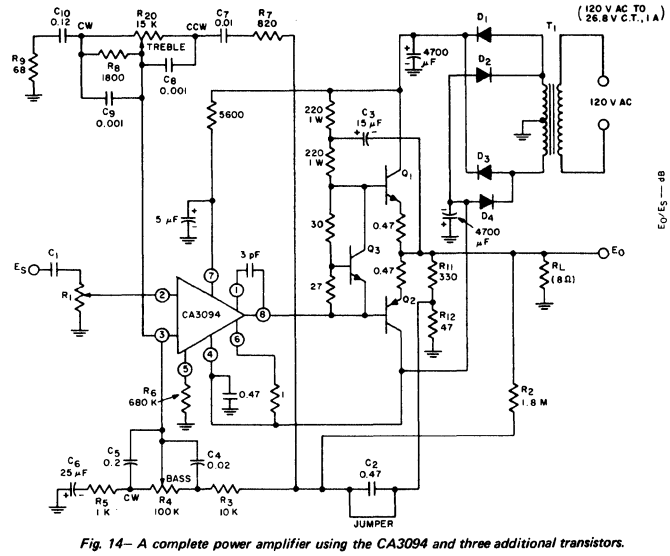


Fig. 14– A complete power amplifier using the CA3094 and three additional transistors.

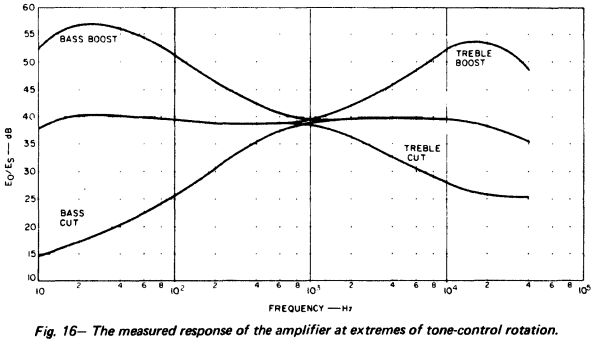


Fig. 16– The measured response of the amplifier at extremes of tone-control rotation.

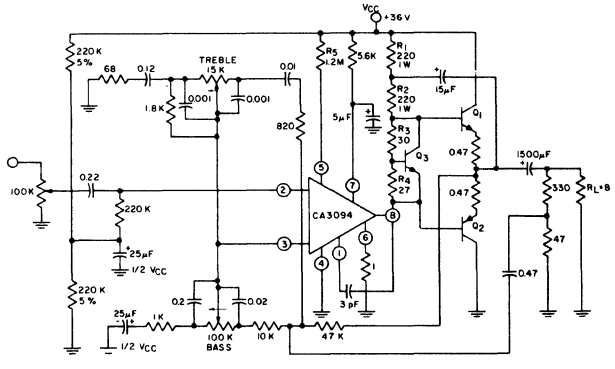


Fig. 15– A power amplifier operated from a single supply.

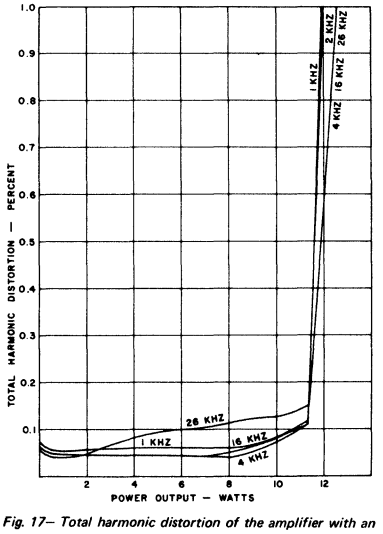


Fig. 17– Total harmonic distortion of the amplifier with an unregulated power supply.

network includes R3, R4, R5, C4, and C5. C6 blocks the dc from the feedback network so that the dc gain from input to the feedback takeoff point is unity. The residual dc-output-voltage at the speaker terminals is then $I_{ABC} R_1 \frac{R_{11} + R_{12}}{R_{12}}$ where R_1 is the source resistance. The input bias current is then $\frac{I_{ABC}}{2\beta} = -\frac{(V_{CC} - V_{be})}{2\beta R6}$. The treble network consists of R7, R8, R9, R10, C7, C8, C9, and C10. Resistors R7 and R9 limit the maximum available cut and boost, respectively. The boost limit is useful in curtailing heating due to finite turn-off time in the output units. The limit is also desirable when there are tape recorders nearby. The cut limit aids the stability of the amplifier by cutting the loop gain at higher frequencies where phase shifts become significant.

In cases in which absolute stability under all load conditions is required, it may be necessary to insert a small inductor in the output lead to isolate the circuit from capacitive loads. A 3-microhenry inductor (1 ampere) in parallel with a 22-ohm resistor is adequate. The derivation of circuit constants is shown in Appendix B. Curves of control action versus electrical rotation are also given.

Performance

Fig. 16 is a plot of the measured response of the complete amplifier at the extremes of tone-control rotation. A comparison of Fig. 16 with the computed curves of Fig. B4 (Appendix B) shows good agreement. The total harmonic distortion of the amplifier with an unregulated power supply is shown in Fig. 17; IM distortion is plotted in Fig. 18. Hum and noise are typically 700 microvolts at the output, or 83-dB down.

COMPANION RIAA PREAMPLIFIER

Many available preamplifiers are capable of providing the drive for the power amplifier of Fig. 14. Yet the unique characteristics of the amplifier – its power supply, input impedance, and gain – make possible the design of an RIAA

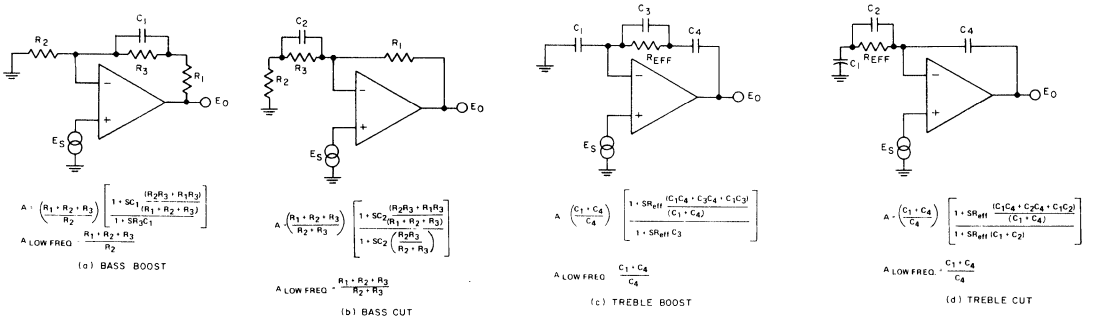


Fig. B1– Four operational-amplifier circuit configurations and the gain expressions for each.

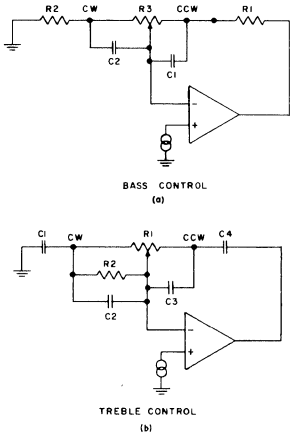


Fig. B2– Cut and boost bass and treble controls that have the characteristics of the circuits of Fig. B1.

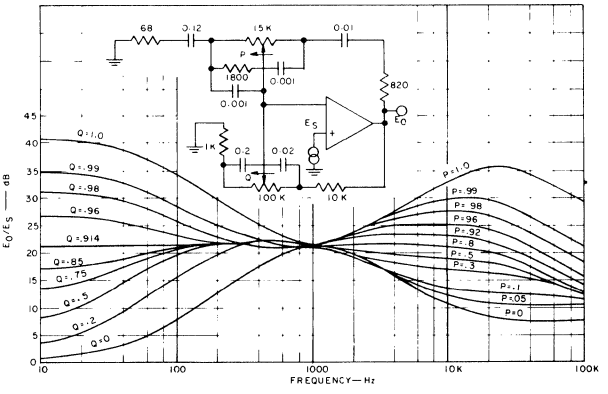


Fig. B3– A plot of the response of the circuit of Fig. 14 with bass and treble tone controls combined at various settings of both controls.

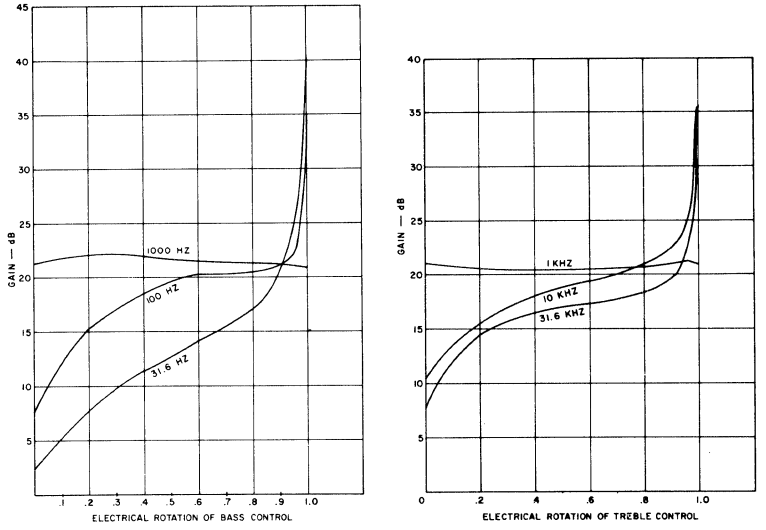


Fig. B4– The information of Fig. B3 plotted as a function of electrical rotation.

91-percent of its total resistance. The amplitude response of the treble control is, however, never completely "flat"; a computer was used to generate response curves as controls were varied.

Fig. B3 is a plot of the response with bass and treble tone controls combined at various settings of both controls. The values shown are the practical ones used in the actual design. Fig. B4 shows the information of Fig. B3 replotted as a function of electrical rotation. The ideal taper for each control would be the complement of the 100-Hz plot for the bass control and the 10-kHz response for the treble control. The mechanical center should occur at the crossover point in each case.

References*

1. "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers," H. A. Wittlinger, RCA Application Note ICAN-6668
2. "A New Wide-band Amplifier Technique," B. Gilbert, IEEE Journal of Solid State Circuits, Vol. SC-3, No. 4, December, 1968.
3. "Trackability," James A. Kogar, *Audio*, December 1966
4. *RCA Linear Integrated Circuits Manual*, RCA Technical Series IC-42

*RCA publications available through RCA Solid State Division, Box 3200, Somerville, N.J., 08876.

teristics for various values of R_{SC} are shown in Fig. 4.

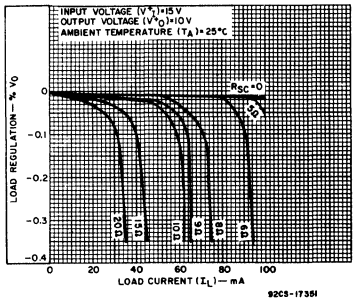


Fig. 4– Load regulation characteristics for circuit of Fig. 3.

When this circuit is used to provide high output currents at low output voltages, care must be exercised to avoid excessive IC dissipation. In the circuit of Fig. 3, this dissipation control can be accomplished by increasing the primary-to-secondary transformer ratio (a reduction in V_I) or by using a dropping resistor between the rectifier and the CA3085 regulator. Fig. 5 gives data on dissipation limitation (V_I-V_O vs. I_O) for CA3085-series circuits.

The short-circuit current is determined as follows:

$$I_{SC} = \frac{V_{BE}}{R_{SC}} \approx \frac{0.7}{R_{SC}} \text{ amperes} \qquad (2)$$

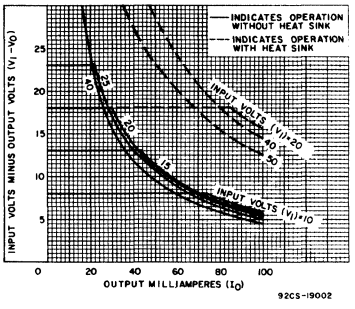


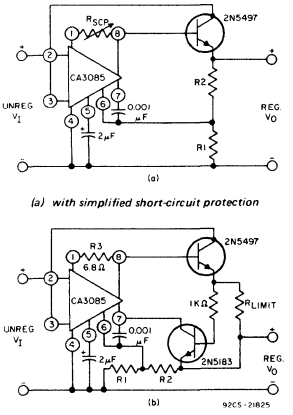
Fig. 5– Dissipation limitation ($V_I - V_O$ vs. I_O) for CA3085 series circuits.

The line- and load-regulation characteristics for the circuit shown in Fig. 3 are approximately 0.05 per cent of the output voltage.

High-Current Voltage Regulator

When regulated voltages at currents greater than 100 milliamperes are required, the CA3085 can be used in conjunction with an external n-p-n pass-transistor as shown in the circuits of Fig. 6. In these circuits the output current available from the regulator is increased in accordance with the h_{FE} of the external n-p-n pass-transistor. Output currents up to 8 amperes can be regulated with these circuits. A Darlington power transistor can be substituted for the 2N5497 transistor when currents greater than 8 amperes are to be regulated.

A simplified method of short-circuit protection is used in connection with the circuit of Fig. 6(a). The variable resistor R_{SCP} serves two purposes: (1) it can be adjusted to optimize the base drive requirements (h_{FE}) of the particular 2N5497 transistor being used, and (2) in the event of a short-circuit in the regulated output voltage the base drive current in the 2N5497 will increase, thereby increasing the voltage drop across R_{SCP}. As this voltage-drop increases the short-circuit protection system within the CA3085 correspondingly reduces the output current available at terminal 8, as described previously. It should be noted that the degree of short-circuit protection depends on the value of R_{SCP}, i.e., design compromise is required in choosing the value of R_{SCP} to provide the desired base drive for the 2N5497 while maintaining the desired short-circuit protection. Fig. 6(b) shows an alternate circuit in which an additional transistor (2N5183) and two resistors have been added as an auxiliary short-circuit protection feature. Resistor R3 is used to establish the desired base drive for the 2N5497, as described above. Resistor R_{limit} now controls the short-circuit output current because, in the event of a short-circuit, the voltage drop developed across its terminals increases sufficiently to increase the base drive to the 2N5183 transistor. This increase in base drive results in reduced output from the CA3085 because collector current flow in the 2N5183 diverts base drive from the Darlington output stage of the CA3085 (see Fig. 2) through terminal 7. The load regulation of this circuit is typically 0.025 per cent with 0 to 3-ampere load-current variation; line regulation is typically 0.025 per cent/volt change in input voltage.



(a) with simplified short-circuit protection

(b) with auxiliary short-circuit protection

Fig. 6– High-current voltage regulator using n-p-n pass transistor.

Voltage Regulator with Low V_I-V_O Difference

In the voltage regulators described in the previous section, it is necessary to maintain a minimum difference of about 4 volts between the input and output voltages. In some applications this requirement is prohibitive. The circuit shown in Fig. 7 can deliver an output current in the order of 2 amperes with a V_I-V_O difference of only one volt.

It employs a single external p-n-p transistor having its base and emitter connected to terminals 2 and 3, respectively, of the CA3085. In this circuit, the emitter of the output transistor (Q14 in Fig. 2) in the CA3085 is returned to the negative supply rail through an external resistor (R_{SCP}) and two series-connected diodes (D1, D2). These forward-biased diodes maintain Q6 in the CA3085 within linear-mode operation. The

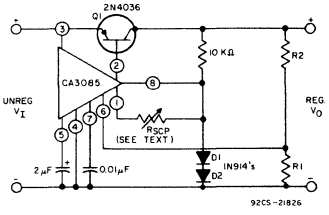


Fig. 7– Voltage regulator for low $V_I - V_O$ difference.

choice of resistors R1 and R2 is made in accordance with Eq. (1). Adequate frequency compensation for this circuit is provided by the 0.01-microfarad capacitor connected between terminal 7 of the CA3085 and the negative supply rail.

Fig. 8, which shows the output impedance of the circuit of Fig. 7 as a function of frequency, illustrates the excellent ripple-rejection characteristics of this circuit at frequencies below 1 kHz. Lower output impedances at the higher frequencies can be provided by connecting an appropriate capacitor across the output voltage terminals. The addition of a capacitor will, however, degrade the ability of the system to react to transient-load conditions.

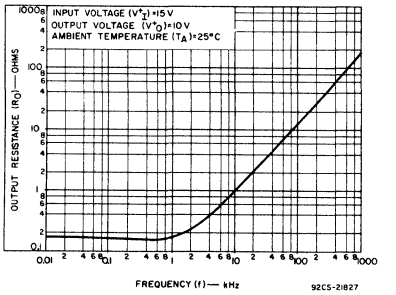


Fig. 8– Output resistance vs. frequency for circuit of Fig. 7.

High-Voltage Regulator

Fig. 9 shows a circuit that uses the CA3085 as a voltage-reference and regulator control device for high-voltage power supplies in which the voltages to be regulated are well above the input-voltage ratings of the CA3085-series circuits. The external transistors Q1 and Q2 require voltage ratings in excess of the maximum input voltage to be regulated. Series-pass transistor Q2 is controlled by the collector current of Q1, which in turn is controlled by the normally regulated current output supplied by the CA3085. The input voltage for the CA3085 regulator at terminal 3 is supplied through dropping resistor R3 and the clamping zener diode D1. The values for resistor R1 and R2 are determined in accordance with Eq. (1).

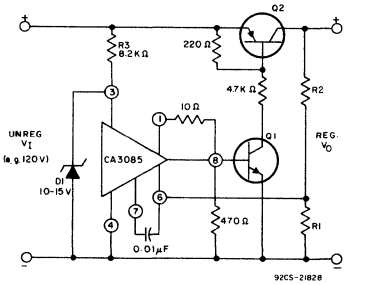


Fig. 9– High-voltage regulator.

Negative-Voltage Regulator

The CA3085 is used as a negative-supply voltage regulator in the circuit shown in Fig. 10. Transistor Q3 is the series-pass transistor. It should be noted that the CA3085 is effectively connected across the load-side of the regulated system. Diode D1 is used initially in a "circuit-starter" function; transistor Q2 "latches" D1 out of its starter-circuit function so that the CA3085 can assume its role in controlling the pass-transistor Q3 by means of Q1.

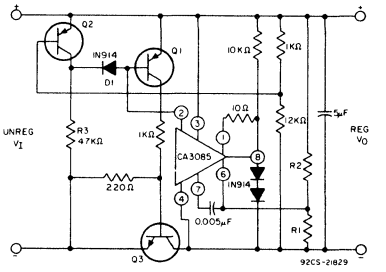


Fig. 10– Negative-voltage regulator.

Operation of the circuit is as follows: current through R3 and D1 provides base drive for Q1, which in turn provides

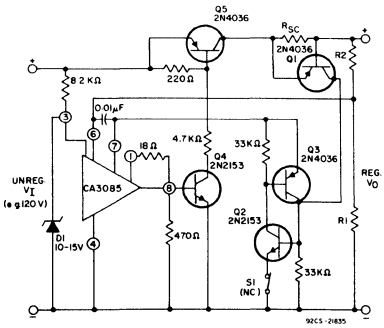


Fig. 16– High-voltage regulator incorporating current "snap-back" protection.

Switching Regulator

When large input-to-output voltage differences are necessary, the regulators described above are inefficient because they dissipate significant power in the series-pass transistor. Under these conditions, high-efficiency operation can be achieved by using a switching-type regulator of the generic type shown in Fig. 17(a). Transistor Q1 acts as a keyed switch and operates in

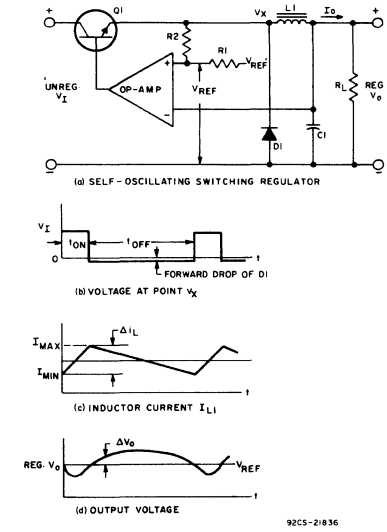


Fig. 17– Switching regulator and associated waveforms.

either a saturated or cut-off condition to minimize dissipation. When transistor Q1 is conductive, diode D1 is reverse-biased and current in the inductance L1 increases in accordance with the following relationship:

$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt \qquad (10)$$

where V is the voltage across the inductance L1. The current through the inductance charges the capacitor C1 and supplies current to the load. The output voltage rises until it slightly exceeds the reference voltage V_{ref}. At this point the op-amp removes base drive to Q1 and the unregulated input voltage V_I is "switched off". The energy stored in the inductor L1 now causes the voltage at V_X to swing in the negative direction and current flows through diode D1, while continuing to supply current into the load R_L. As the current in the inductor falls below the load current, the capacitor C1 begins to discharge and V_O decreases. When V_O falls slightly below the value of V_{ref}, the op-amp turns on Q1 and the cycle is repeated. It should be apparent that the output voltage oscillates about V_{ref} with an amplitude determined by R1 and R2. Actually, the value of V_{ref} varies from being slightly more positive than V_{ref} when Q1 is conducting, to being slightly more negative than V_{ref} when D1 is conducting. The voltage and current waveforms are shown in Fig. 17(b), (c), and (d).

Design Example: The following specifications are used in decomputations for a switching regulator:

$V_I = 30$ V, $V_O = 5$ V, $I_O = 500$ mA,
switching frequency = 20 kHz,
output ripple = 100 mV.

If it is assumed that transistor Q1 is in steady-state saturated operation with a low voltage-drop, the current in the inductor is given by Eq. 10, as follows:

$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt = \left(\frac{V_I - V_O}{L1}\right) t_{on} \qquad (11)$$

When transistor Q1 is off, the current in the inductor is given by:

$$i_L \cong \frac{(V_O + V_{D1})\ t_{off}}{L1} \qquad (12)$$

From Eq. 11,

$$L_1 = \frac{(V_I - V_O)}{i_L} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \qquad (13)$$

If i_{max} is 1.3 I_L, then during t_{on} the current in the inductor (i_L) will be 0.5 A x 1.3 = 0.65 A; therefore, Δi_L = 0.15 A

Substitution in Eq. 13 yields

$$L_1 = \frac{(30-5)}{0.15} \cdot \frac{1}{(20 \times 10^3)} \cdot \frac{5}{30} = 1.4 \text{ mH} \qquad (14)$$

Current discharge from the capacitor C1 is given by:

$$i_c = C\frac{dv}{dt} \qquad (15)$$

Thus, $\Delta i_c = C\frac{\Delta v}{\Delta t}$, or $C = \frac{\Delta i_c\ \Delta t}{\Delta v}$

Since $i_c = i_L$ and $\Delta t = t_{off}$, then

$$C = \frac{\Delta i_L\ t_{off}}{\Delta v}$$

Substitution for the value of i_L from Eq. 13 yields

$$C = \frac{\left(\frac{V_I - V_O}{L1}\right) \cdot \frac{1}{f} \cdot \left(\frac{V_O}{V_I}\right) \cdot t_{off}}{\Delta v} \qquad (16)$$

The total period $T = t_{off} + t_{on}$, and $T = \frac{1}{f}$. Therefore,

$$t_{off} = \frac{1}{f} - t_{on} \qquad (17)$$

For optimum efficiency t_{on} should be

$$\cong \left(\frac{V_O}{V_I}\right) T \cong \left(\frac{V_O}{V_I}\right) \frac{1}{f} \qquad (18)$$

Substitution for t_{on} in Eq. 18 yields

$$t_{off} = \frac{1}{f} - \left(\frac{V_O}{V_I}\right)\frac{1}{f} = \frac{1}{f}\left(1 - \frac{V_O}{V_I}\right) \qquad (19)$$

Substitution for t_{off} in Eq. 16 yields

$$C = \frac{\frac{(V_I - V_O)}{L_1} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \cdot \frac{1}{f} \cdot \left(1 - \frac{V_O}{V_I}\right)}{\Delta v}$$

Substitution of numerical values in Eq. 20 produces the following value for C:

$$C = \frac{\frac{30-5}{1.4 \times 10^{-3}} \cdot \frac{1}{20 \times 10^3} \cdot \frac{5}{30} \cdot \frac{1}{20 \times 10^3} \cdot \left(1 - \frac{5}{30}\right)}{10^{-1}} = 63\ \mu F$$

A switching-regulator circuit using the CA3085 is shown in Fig. 18. The values of L and C (1.5 millihenries and 50 microfarads, respectively) are commercially available components having values approximately equal to the computed values in the previous design example.

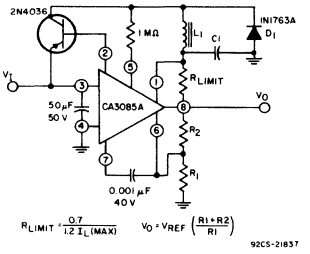
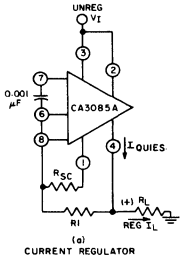


Fig. 18– Typical switching regulator circuit.

Current Regulators

The CA3085 series of voltage regulators can be used to provide a constant source or sink current. A regulated-current supply capable of delivering up to 100 milliamperes is shown in Fig. 19(a). The regulated load current is controlled by R1 because the current flowing through this resistor must establish a voltage difference between terminals 6 and 4 that is equal to the internal reference voltage developed between terminals 5 and 4. The actual regulated current, reg I_L, is the sum of the quiescent regulator current and the current through R1, i.e.,

$$\text{reg } I_L = I_{quiescent} + I_{R1}$$



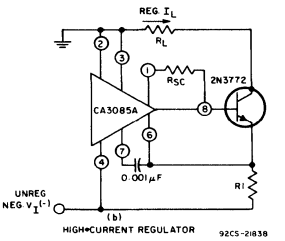


Fig. 19– Constant current regulators.

Fig. 19(b) shows a high-current regulator using the CA3085 in conjunction with an external n-p-n transistor to regulate currents up to 3 amperes. In this circuit the quiescent regulator current does not flow through the load and the output current can be directly programmed by R1, i.e.,

$$\text{Reg } I_L = \frac{V_{ref}}{R1}$$

With this regulator currents between 1 milliampere and 3 amperes can be programmed directly. At currents below 1 milliampere inaccuracies may occur as a result of leakage in the external transistor.

A Dual-Tracking Voltage Regulator

A dual-tracking voltage regulator using a CA3085 and a CA3094A* is shown in Fig. 20. The CA3094A is basically an op-amp capable of supplying 100 milliamperes of output current.

Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)

by A.C.N. Sheng, G.J. Granieri, J. Yellin, and T. McNulty

RCA-CA3058, CA3059 and CA3079 zero-voltage switches are monolithic integrated circuits designed primarily for use as trigger circuits for thyristors in many highly diverse ac power-control and power-switching applications. These integrated-circuit switches operate from an ac input voltage of 24, 120, 208 to 230, or 277 volts at 50, 60, or 400 Hz.

The CA3059 and CA3079 are supplied in a 14-terminal dual-in-line plastic package. The CA3058 is supplied in a 14-terminal dual-in-line ceramic package. The electrical and physical characteristics of each type are detailed in RCA Data Bulletin File No. 490.

RCA zero-voltage switches (ZVS) are particularly well suited for use as thyristor trigger circuits. These switches trigger the thyristors at zero-voltage points in the supply-voltage cycle. Consequently, transient load-current surges and radio-frequency interference (RFI) are substantially reduced. In addition, use of the zero-voltage switches also reduces the rate of change of on-state current (di/dt) in the thyristor being triggered, an important consideration in the operation of thyristors. These switches can be adapted for use in a variety of control functions by use of an internal differential comparator to detect the difference between two externally developed voltages. In addition, the availability of numerous terminal connections to internal circuit points greatly increases circuit flexibility and further expands the types of ac power-control applications to which these integrated circuits may be adapted. The excellent versatility of the zero-voltage switches is demonstrated by the fact that these circuits have been used to provide transient-free temperature control in self-cleaning ovens, to control gun-muzzle temperature in low-temperature environments, to provide sequential switching of heating elements in warm-air furnaces, to switch traffic signal lights at street intersections, and to effect other widely different ac power-control functions.

FUNCTIONAL DESCRIPTION

RCA zero-voltage switches are multistage circuits that employ a diode limiter, a zero-crossing (threshold) detector, an on-off sensing amplifier (differential comparator), and a Darlington output driver (thyristor gating circuit) to provide the basic switching action. The dc operating voltages for these stages is provided by an internal power supply that has sufficient current capability to drive external circuit elements, such as transistors and other integrated circuits. An important feature of the zero-voltage switches is that the output trigger pulses can be applied directly to the gate of a triac or a silicon controlled rectifier (SCR). The CA3058 and CA3059 also feature an interlock (protection) circuit that inhibits the application of these pulses to the thyristor in the event that the external sensor should be inadvertently opened or shorted. An external inhibit connection (terminal No. 1) is also available so that an external signal can be used to inhibit the output drive. This feature is not included in the CA3079; otherwise, the three integrated-circuit zero-voltage switches are electrically identical.

Over-all Circuit Operation

Fig. 1 shows the functional interrelation of the zero-voltage switch, the external sensor, the thyristor being triggered, and the load elements in an on-off type of ac power-control system. As shown, each of the zero-voltage switches incorporates four functional blocks as follows:

(1) Limiter-Power Supply – Permits operation directly from an ac line.

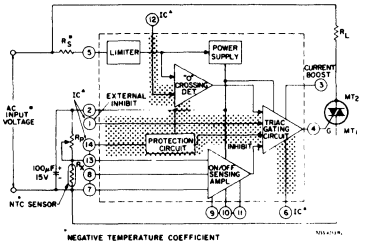
(2) Differential On/Off Sensing Amplifier – Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.

(3) Zero-Crossing Detector – Synchronizes the output pulses of the circuit at the time when the ac cycle is at a zero-voltage point and thereby eliminates radio-frequency inteference (RFI) when used with resistive loads.

(4) Triac Gating Circuit – Provides high-current pulses to the gate of the power-controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (shown in Fig. 1):

(1) A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

Fig. 1 – Functional block diagrams of the zero-voltage switches CA3058, CA3059, and CA3079.

(2) Thyristor firing may be inhibited through the action of an internal diode gate connected to terminal 1.

(3) High-power dc-comparator operation is provided by overriding the action of the zero-crossing detector. This override is accomplished by connecting terminal 12 to terminal 7. Gate current to the thyristor is continuous when terminal 13 is positive with respect to terminal 9.

Fig. 2 shows the detailed circuit diagram for the integrated-circuit zero-voltage switches. (The diagrams shown in Figs. 1 and 2 are representative of all three RCA zero-voltage switches, i.e., the CA3058, CA3059, and CA3079; the shaded areas indicate the circuitry that is not included in the CA3079.)

The limiter stage of the zero-voltage switch clips the incoming ac line voltage to approximately ±8 volts. This signal is then applied to the zero-voltage-crossing detector, which generates an output pulse each time the line voltage passes through zero. The limiter output is also applied to a rectifying diode and an external capacitor, C_F, that comprise the dc power supply. The power supply provides approximately 6 volts as the V_{CC} supply to the other stages of the zero-voltage switch. The on-off sensing amplifier is basically a differential comparator. The thyristor gating circuit contains a driver for direct triac triggering. The gating circuit is enabled when all the inputs are at a "high" voltage, i.e., the line voltage must be approximately zero volts, the sensing-amplifier output must be "high," the external voltage to terminal 1 must be a logical "0", and, for the CA3058 and CA3059, the output of the fail-safe circuit must be "high." Under these conditions, the thyristor (triac or SCR) is triggered when the line voltage is essentially zero volts.

Thyristor Triggering Circuits

The diodes D_1 and D_2 in Fig. 2 form a symmetrical clamp that limits the voltages on the chip to ±8 volts; the diodes D_7 and D_{13} form a half-wave rectifier that develops a positive voltage on the external storage capacitor, C_F.

The output pulses used to trigger the power-switching thyristor are actually developed by the zero-crossing detector and the thyristor gating circuit. The zero-crossing detector consists of diodes D_3 through D_6, transistor Q_1, and the associated resistors shown in Fig. 2. Transistors Q_1 and Q_6 through Q_9 and the associated resistors comprise the thyristor gating circuit and output driver. These circuits generate the output pulses when the ac input is at a zero-voltage point so that RFI is virtually eliminated when the zero-voltage switch and thyristor are used with resistive loads.

The operation of the zero-crossing detector and thyristor gating circuit can be explained more easily if the on state (i.e., the operating state in which current is being delivered to the thyristor gate through terminal 4) is considered as the operating condition of the gating circuit. Other circuit elements in the zero-voltage switch inhibit the gating circuit unless certain conditions are met, as explained later.

In the on state of the thyristor gating circuit, transistors Q_8 and Q_9 are conducting, transistor Q_7 is off, and transistor Q_6 is on. Any action that turns on transistor Q_7 removes the drive from transistor Q_8 and thereby turns off the thyristor. Transistor Q_7 may be turned on directly by application of a minimum of ±1.2 volts at 10 microamperes to the external-inhibit input, terminal 1. (If a voltage of more than

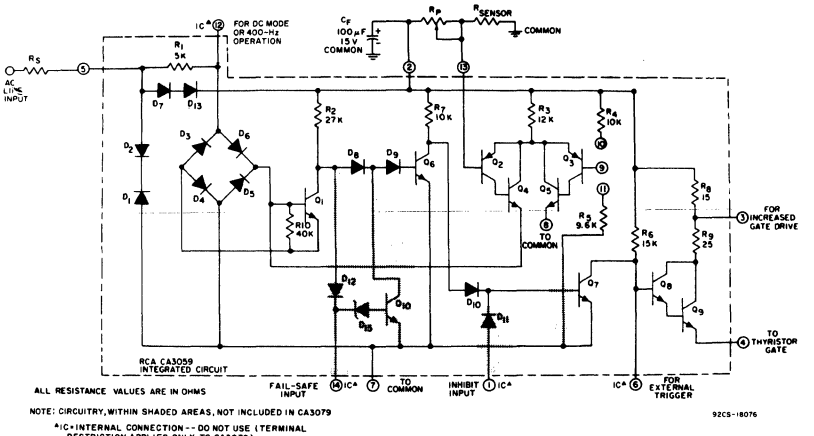


Fig. 2 – Schematic diagram of zero-voltage switches CA3058, CA3059, and CA3079.

more positive than the breakdown voltage of diode D_{15}, activation of the protection circuit is not possible. For this reason, loading the internal supply may cause this circuit to malfunction, as may selection of the wrong external supply voltage. Fig. 7 shows a guide for the proper operation of the protection circuit when an external supply is used with a typical integrated-circuit zero-voltage switch.

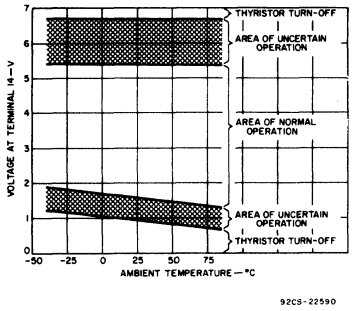


Fig. 7 – Operating regions for built-in protection circuits of a typical zero-voltage switch.

SPECIAL APPLICATION CONSIDERATIONS

As pointed out previously, the RCA integrated-circuit zero-voltage switches (CA3058, CA3059, and CA3079) are exceptionally versatile units that can be adapted for use in a wide-variety of power-control applications. Full advantage of this versatility can be realized, however, only if the user has a basic understanding of several fundamental considerations that apply to certain types of applications of the zero-voltage switches.

Operating-Power Options

Power to the zero-voltage switch may be derived directly from the ac line, as shown in Fig. 1, or from an external dc power supply connected between terminals 2 and 7, as shown in Fig. 8. When the zero-voltage switch is operated directly from the ac line, a dropping resistor R_S of 5,000 to 10,000 ohms must be connected in series with terminal 5 to limit the current in the switch circuit. The optimum value for this resistor is a function of the average current drawn from the internal dc power supply, either by external circuit elements or by the thyristor trigger circuits, as shown in Fig. 9. The chart shown in Fig. 1 indicates the value and dissipation rating of the resistor R_S for ac line voltages of 24, 120, 208 to 230, and 277 volts.

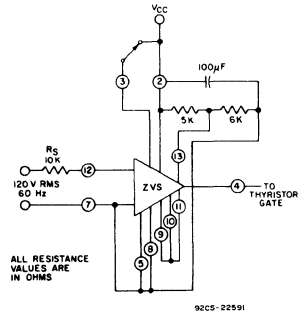


Fig. 8 – Operation of the zero-voltage switch from an external dc power supply connected between terminals 2 and 7.

Half-Cycling Effect

The method by which the zero-voltage switch senses the zero crossing of the ac power results in a half-cycling phenomenon at the control point. Fig. 10 illustrates this phenomenon. The zero-voltage switch senses the zero-voltage

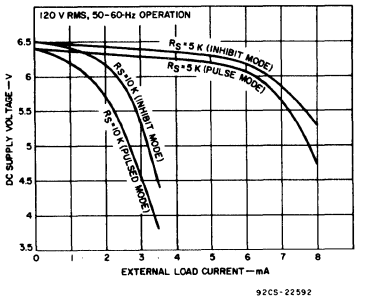


Fig. 9 – DC supply voltage as a function of external load current for several values of dropping resistance R_S.

crossing every half-cycle, and an output, for example pulse No. 4, is produced to indicate the zero crossing. During the remaining 8.3 milliseconds, however, the differential amplifier in the zero-voltage switch may change state and inhibit any further output pulses. The uncertainity region of the differential amplifier, therefore, prevents pulse No. 5 from triggering the triac during the negative excursion of the ac line voltage.

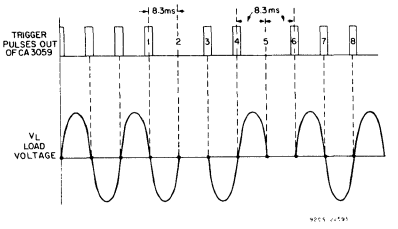


Fig. 10 – Half-cycling phenomenon in the zero-voltage switch.

When a sensor with low sensitivity is used in the circuit, the zero-voltage switch is very likely to operate in the linear mode. In this mode, the output trigger current may be sufficient to trigger the triac on the positive-going cycle, but insufficient to trigger the device on the negative-going cycle of the triac supply voltage. This effect introduces a half-cycling phenomenon, i.e., the triac is turned on during the positive half-cycle and turned off during the negative half-cycle.

Several techniques may be used to cope with the half-cycling phenomenon. If the user can tolerate some hystersis in the control, then positive feedback can be added around the differential amplifier. Fig. 11 illustrates this technique. The tabular data in the figure lists the recommended values of resistors R_1 and R_2 for different sensor impedances at the control point.

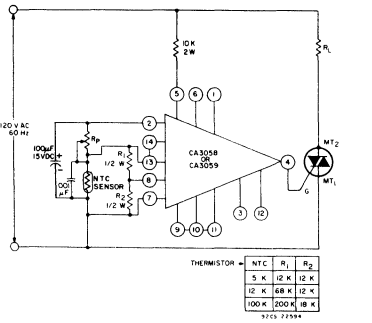


Fig. 11 – CA3058 or CA3059 on-off controller with hysteresis.

If a significant amount (greater than ±10%) of controlled hysteresis is required, then the circuit shown in Fig. 12 may be employed. In this configuration, external transistor Q_1 can be used to provide an auxiliary timed-delay function.

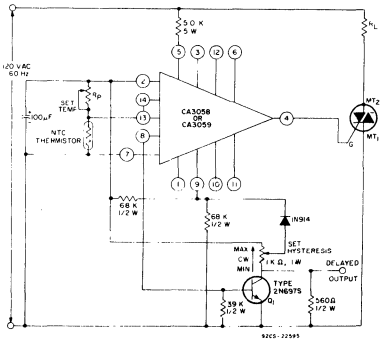


Fig. 12 – CA3058 or CA3059 on-off controller with controlled hysteresis.

For applications that require complete elimination of half-cycling without the addition of hysteresis, the circuit shown in Fig. 13 may be employed. This circuit uses a CA3098E integrated-circuit programmable comparator with a zero-voltage switch. A block diagram of CA3098E is shown in Fig. 14. Because the CA3098E contains an integral flip-flop, its output will be in either a "0" or "1" state. Consequently the zero-voltage switch cannot operate in the linear mode, and spurious half-cycling operation is prevented. When the signal-input voltage at terminal 8 of the CA3098E is equal to or less than the "low" reference voltage (LR), current flows from the power supply through resistor R_1 and R_2, and a logic "0" is

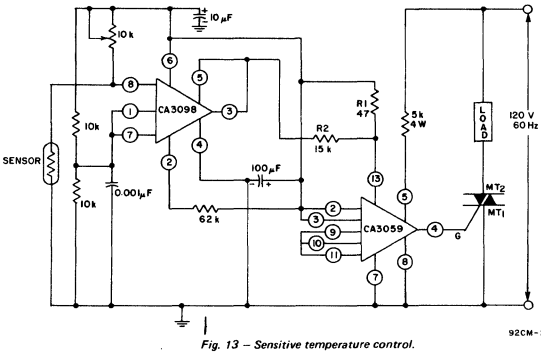


Fig. 13 – Sensitive temperature control.

Circuits that use a sensitive-gate triac to shift the firing point of the power triac by approximately 90 degrees have been designed. If the primary load is inductive, this phase shift corresponds to firing at zero current in the load. However, changes in the power factor of the load or tolerances of components will cause errors in this firing time.

The circuit shown in Fig. 19 uses a CA3086 integrated-circuit transistor array to detect the absence of load current by sensing the voltage across the triac. The internal zero-crossing detector is disabled by connection of terminal 12 to terminal 7, and control of the output is made through the external inhibit input, terminal 1. The circuit permits an output only when the voltage at point A exceeds two V_{BE} drops, or 1.3 volts. When A is positive, transistors Q_3 and Q_4 conduct and reduce the voltage at terminal 1 below the inhibit state. When A is negative, transistors Q_1 and Q_2 conduct. When the voltage at point A is less than ±1.3 volts, neither of the transistor pairs conducts; terminal 1 is then pulled positive by the current in resistor R_3, and the output in inhibited.

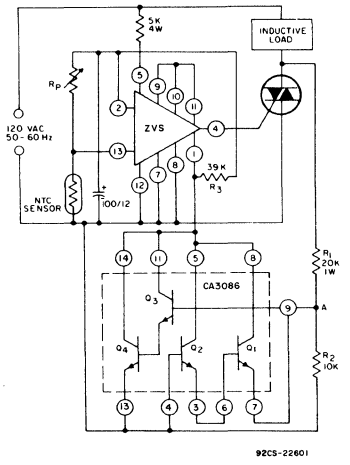


Fig. 19 – Use of the CA3058 or CA3059 together with CA3086 for switching inductive loads.

The circuit shown in Fig. 19 forms a pulse of gate current and can supply high peak drive to power traics with low average current drain on the internal supply. The gate pulse will always last just long enough to latch the thyristor so that there is no problem with delaying the pulse to an optimum time. As in other circuits of this type, RFI results if the load is not suitably inductive because the zero-crossing detector is disabled and initial turn-on occurs at random.

The gate pulse forms because the voltage at point A when the thyristor is on is less than 1.3 volts: therefore, the output of the zero-voltage switch is inhibited, as described above. The resistor divider R_1 and R_2 should be selected to assure this condition. When the triac is on, the voltage at point A is approximately one-third of the instantaneous on-state voltage (v_T) of the thyristor. For most RCA thyristors, v_T (max) is less than 2 volts, and the divider shown is a conservative one. When the load current passes through zero, the triac commutates and turns off. Because the circuit is still being driven by the line voltage, the current in the load attempts to reverse, and voltage increases rapidly across the "turned-off" triac. When this voltage exceeds 4 volts, one portion of the CA3086 conducts and removes the inhibit signal to permit application of gate drive. Turning the triac on causes the voltage across it to drop and thus ends the gate pulse. If the latching current has not been attained, another gate pulse forms, but no discontinuity in the load current occurs.

Provision of Negative Gate Current

Triacs trigger with optimum sensitivity when the polarity of the gate voltage and the voltage at the main terminal 2 are similar (I^+ and II^- modes). Sensitivity is degraded when the polarities are opposite (I^- and III^+ modes). Although RCA triacs are designed and specified to have the same sensitivity in both I^- and III^+ modes, some other types have very poor sensitivity in the III^+ condition. Because the zero-voltage switch supplies positive gate pulses, it may not directly drive some higher-current triacs of these other types.

The circuit shown in Fig. 20(a) uses the negative-going voltage at terminal 3 of the zero-voltage switch to supply a negative gate pulse through a capacitor. The curve in Fig. 20(b) shows the approximate peak gate current as a function of gate voltage V_G. Pulse width is approximately 80 microseconds.

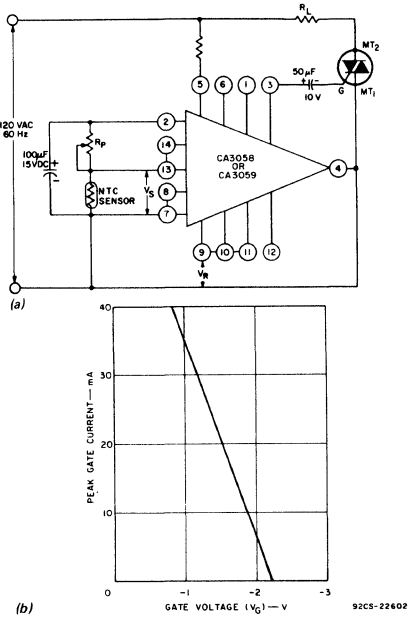


Fig. 20 – Use of the CA3058 or CA3059 to provide negative gate pulses: (a) schematic diagram; (b) peak gate current (at terminal 3) as a function of gate voltage.

Operation with Low-Impedance Sensors

Although the zero-voltage switch can operate satisfactorily with a wide range of sensors, sensitivity is reduced when sensors with impedances greater than 20,000 ohms are used. Typical sensitivity is one per cent for a 5000-ohm sensor and increases to three per cent for a 0.1-megohm sensor.

Low-impedance sensors present a different problem. The sensor bridge is connected across the internal power supply and causes a current drain. A 5000-ohm sensor with its associated 5000-ohm series resistor draws less than 1 milliampere. On the other hand, a 300-ohm sensor draws a current of 8 to 10 milliampers from the power supply.

Fig. 21 shows the 600-ohm load line of a 300-ohm sensor on a redrawn power-supply regulation curve for the zero-voltage switch. When a 10,000-ohm series resistor is used, the voltage across the circuit is less than 3 volts and both sensitivity and output current are significantly reduced. When a 5000-ohm series resistor is used, the supply voltage is nearly 5 volts, and operation is approximately normal. For more consistent operation, however, a 4000-ohm series resistor is recommended.

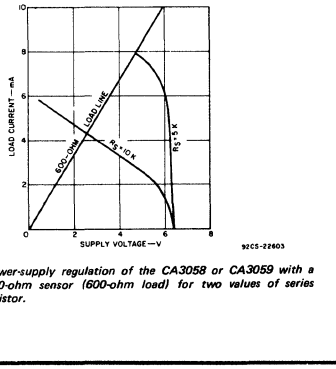


Fig. 21 – Power-supply regulation of the CA3058 or CA3059 with a 300-ohm sensor (600-ohm load) for two values of series resistor.

Although positive-temperature-coefficient (PTC) sensors rated at 5 kilohms are available, the existing sensors in ovens are usually of a much lower value. The circuit shown in Fig. 22 is offered to accommodate these inexpensive metal-wound

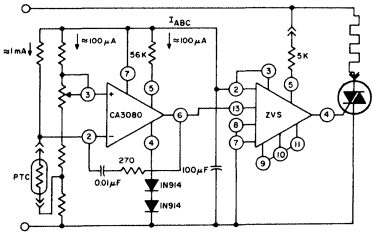


Fig. 22 – Schematic diagram of circuit for use with low-resistance sensor.

sensors. A schematic diagram of the RCA CA3080 integrated-circuit operational transconductance amplifier used in Fig. 22, is shown in Fig. 23. With an amplifier bias current, I_{ABC}, of 100 microamperes, a forward transconductance of 2 milliohms is achieved in this configuration. The CA3080 switches when the voltage at terminal 2 exceeds the voltage at terminal 3. This action allows the sink current, I_s, to flow from terminal 13 of the zero-voltage switch (the input impedance to terminal 13 of the zero-voltage switch is approximately 50 kilohms); gate pulses are no longer applied to the triac because Q_2 of the zero-voltage switch is on. Hence, if the PTC sensor is cold, i.e., in the low resistance state, the load is energized. When the temperature of the PTC sensor increases to the desired temperature, the sensor enters the high resistance state, the voltage on terminal 2 becomes greater than that on terminal 3, and the triac switches the load off.

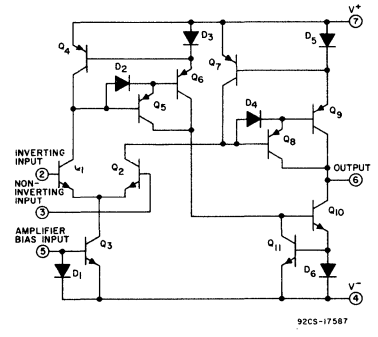


Fig. 23 – Schematic diagram of the CA3080.

Further cycling depends on the voltage across the sensor. Hence, very low values of sensor and potentiometer resistance can be used in conjunction with the zero-voltage switch power supply without causing adverse loading effects and impairing system performance.

Interfacing Techniques

Fig. 24 shows a system diagram that illustrates the role of the zero-voltage switch and thyristor as an interface between the logic circuitry and the load. There are several basic interfacing techniques. Fig. 25(a) shows the **direct input** technique. When the logic output transistor is switched from the on state (saturated) to the off state, the load will be turned on at the next zero-voltage crossing by means of the interfacing zero-voltage switch and the triac. When the logic output transistor is switched back to the on state, zero-crossing pulses from the zero-voltage switch to the triac

TEMPERATURE CONTROLLERS

Fig. 29 shows a triac used in an on-off temperature-controller configuration. The triac is turned on at zero voltage whenever the voltage V_s exceeds the reference

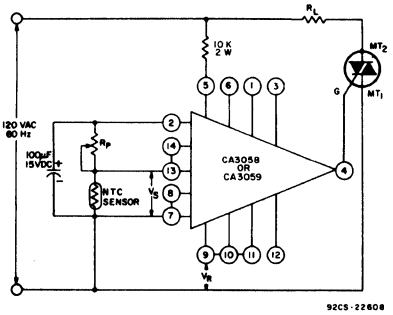


Fig. 29 – CA3058 or CA3059 on-off temperature controller.

voltage V_r. The transfer characteristic of this system, shown in Fig. 30(a), indicates significant thermal overshoots and undershoots, a well-known characteristic of such a system. The differential or hysteresis of this system, however, can be further increased, if desired, by the addition of positive feedback.

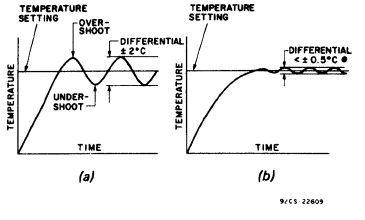


Fig. 30 – Transfer characteristics of (a) on-off and (b) proportional control systems.

For precise temperature-control applications, the proportional-control technique with synchronous switching is employed. The transfer curve for this type of controller is shown in Fig. 30(b). In this case, the duty cycle of the power supplied to the load is varied with the demand for heat required and the thermal time constant (inertia) of the system. For example, when the temperature setting is increased in an on-off type of controller, full power (100 per cent duty cycle) is supplied to the system. This effect results in significant temperature excursions because there is no anticipatory circuit to reduce the power gradually before the actual set temperature is achieved. However, in a proportional control technique, less power is supplied to the load (reduced duty cycle) as the error signal is reduced (sensed temperature approaches the set temperature).

Before such a system is implemented, a time base is chosen so that the on-time of the triac is varied within this time base. The ratio of the on-to-off time of the triac within this time interval depends on the thermal time constant of the system and the selected temperature setting. Fig. 31 illustrates the principle of proportional control. For this operation, power is supplied to the load until the ramp voltage reaches a value greater than the dc control signal supplied to the opposite side of the differential amplifier. The triac then remains off for the remainder of the time-base period. As a result, power is "proportioned" to the load in a direct relation to the heat demanded by the system.

For this application, a simple ramp generator can be realized with a minimum number of active and passive components. A ramp having good linearity is not required for proportional operation because of the nonlinearity of the

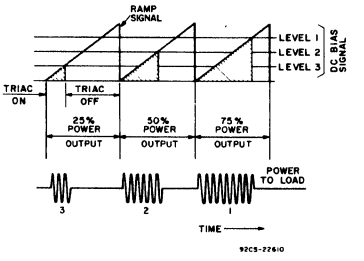


Fig. 31 – Principles of proportional control.

thermal system and the closed-loop type of control. In the circuit shown in Fig. 32, the ramp voltage is generated when the capacitor C_1 charges through resistors R_0 and R_1. The time base of the ramp is determined by resistors R_2 and R_3, capacitor C_2, and the breakover voltage of the D3202U* diac.

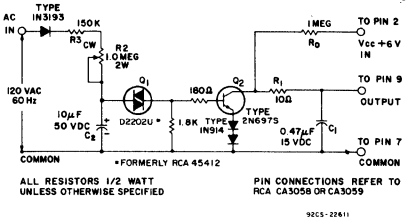


Fig. 32 – Ramp generator.

When the voltage across C_2 reaches approximately 32 volts, the diac switches and turns on the 2N697S transistor and 1N914 diodes. The capacitor C_1 then discharges through the collector-to-emitter junction of the transistor. This discharge time is the retrace or flyback time of the ramp. The circuit shown can generate ramp times ranging from 0.3 to 2.0 seconds through adjustment of R_2. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system, but long with respect to the period of the 60-Hz line voltage. Fig. 33 shows a triac connected for the proportional mode.

lag the incoming line voltage. The motors, however, are switched by the triacs at zero current, as shown in Fig. 34(b).

The problem of driving inductive loads such as these motors by the narrow pulses generated by the zero-voltage switch is solved by use of the sensitive-gate RCA-40526 triac. The high sensitivity of this device (3 milliamperes maximum) and low latching current (approximately 9 milliamperes) permit synchronous operation of the temperature-controller circuit. In Fig. 34(a), it is apparent that, though the gate pulse V_g of triac Y_1 has elapsed, triac Y_2 is switched on by the current through R_{L1}. The low latching current of the RCA-40526 triac results in dissipation of only 2 watts in R_{L1}, as opposed to 10 to 20 watts when devices that have high latching currents are used.

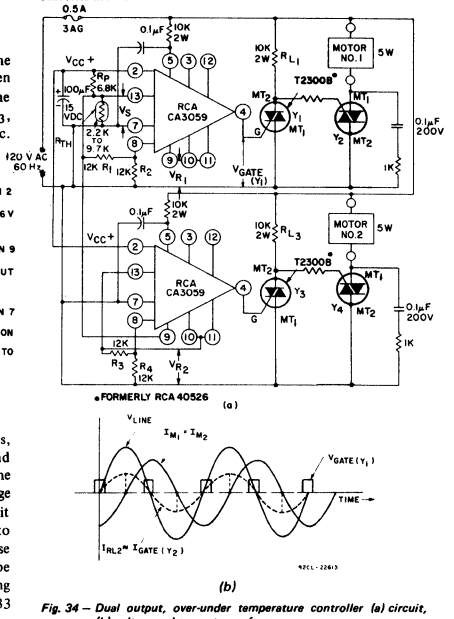


Fig. 34 – Dual output, over-under temperature controller (a) circuit, (b) voltage and current waveforms.

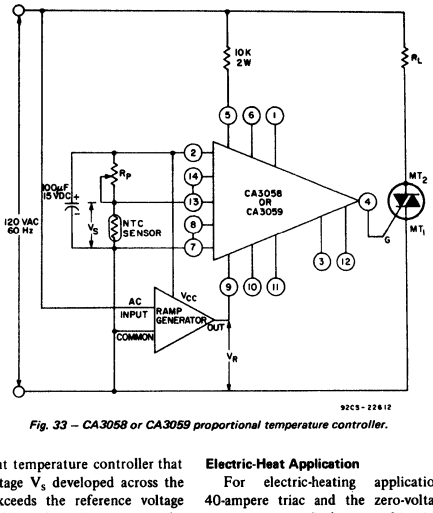


Fig. 33 – CA3058 or CA3059 proportional temperature controller.

Fig. 34(a) shows a dual-output temperature controller that drives two triacs. When the voltage V_s developed across the temperature-sensing network exceeds the reference voltage V_{R1}, motor No. 1 turns on. When the voltage across the network drops below the reference voltage V_{R2}, motor No. 2 turns on. Because the motors are inductive, the currents I_{M1}

Electric-Heat Application

For electric-heating applications, the RCA-2N5444 40-ampere triac and the zero-voltage switch constitute an optimum pair. Such a combination provides synchronous switching and effectively replaces the heavy-duty contactors which easily degrade as a result of pitting and wearout from

* Formerly RCA 45412

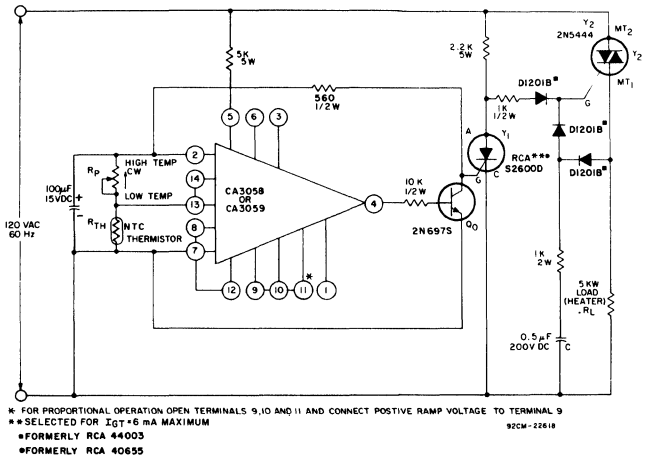


Fig. 39 – CA3058 or CA3059 integral-cycle temperature controller that features a protection circuit and no half-cycling effect.

When the ac line swings negative, capacitor C discharges through the triac gate to trigger the triac on the negative half-cycle. The diode-resistor-capacitor "slaving network" triggers the triac on negative half-cycle to provide only **integral cycles** of ac power to the load.

When the temperature being controlled reaches the desired value, as determined by the thermistor, then a positive voltage level appears at terminal 4 of the zero-voltage switch. The SCR then starts to conduct at the beginning of the positive input cycle to shunt the trigger current away from the gate of the triac. The triac is then turned off. The cycle repeats when the SCR is again turned OFF by the zero-voltage switch.

The circuit shown in Fig. 39 is similar to the configuration in Fig. 38 except that the protection circuit incorporated in the zero-voltage switch can be used. In this new circuit, the NTC sensor is connected between terminals 7 and 13, and transistor Q_0 inverts the signal output at terminal 4 to nullify the phase reversal introduced by the SCR (Y_1). The internal power supply of the zero-voltage switch supplies bias current to transistor Q_0.

Of course, the circuit shown in Fig. 39 can readily be converted to a **true proportional integral-cycle temperature controller** simply by connection of a positive-going ramp voltage to terminal 9 (with terminals 10 and 11 open), as previously discussed in this Note.

Thermocouple Temperature Control

Fig. 40 shows the CA3080A operating as a pre-amplifier for the zero-voltage switch to form a zero-voltage switching circuit for use with thermocouple sensors.

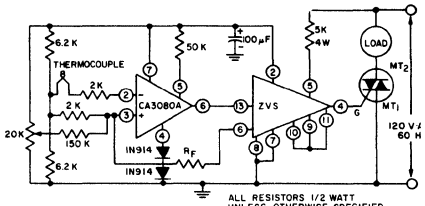


Fig. 40 – Thermocouple temperature control with zero-voltage switching.

Thermocouple Temperature Control with Zero-Voltage Load Switching

Fig. 41 shows the circuit diagram of a thermocouple temperature control system using zero-voltage load switching. It should be noted that one terminal of the thermocouple is connected to one leg of the supply line. Consequently, the thermocouple can be "ground-referenced", provided the appropriate leg of the ac line is maintained at ground. The comparator, A_1 (a CA3130), is powered from a 6.4-volt source of potential provided by the zero-voltage-switch (ZVS) circuit (a CA3079). The ZVS, in turn, is powered off-line through a series-dropping resistor R6. Terminal 4 of the ZVS provides trigger-pulses to the gate of the load-switching triac in response to an appropriate control signal at terminal 9.

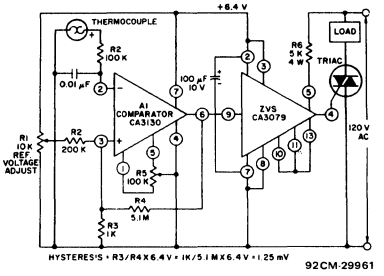


Fig. 41 – Thermocouple temperature control with zero-voltage switching.

The CA3130 is an ideal choice for the type of comparator circuit shown in Fig. 41 because it can "compare" low voltages (such as those generated by a thermocouple) in the proximity of the negative supply rail. Adjustment of potentiometer R1 drives the voltage-divider network R3, R4 so that reference voltages over the range of 0 to 20 millivolts can be applied to noninverting terminal 3 of the comparator. Whenever the voltage developed by the thermocouple at terminal 2 is more positive than the reference voltage applied at terminal 3, the comparator output is toggled so as to sink current from terminal 9 of the ZVS; gate pulses are then no longer applied to the triac. As shown in Fig. 41, the circuit is provided with a control-point "hysteresis" of 1.25 millivolts.

Nulling of the comparator is performed by means of the following procedure: Set R1 at the low end of its range and short the thermocouple output signal appropriately. If the triac is in the conductive mode under these conditions, adjust nulling potentiometer R5 to the point at which triac conduction is interrupted. On the other hand, if the triac is in the non-conductive mode under the conditions above, adjust R5 to the point at which triac conduction commences. The thermocouple output signal should then be unshorted, and R1 can be set to the voltage threshold desired for control-circuit operation.

MACHINE CONTROL AND AUTOMATION

The earlier section on interfacing techniques indicated several techniques of controlling ac loads through a logic system. Many types of automatic equipment are not complex enough or large enough to justify the cost of a flexible logic system. A special circuit, designed only to meet the control requirements of a particular machine, may prove more economical. For example, consider the simple machine shown in Fig. 42; for each revolution of the motor, the belt is advanced a prescribed distance, and the strip is then punched. The machine also has variable speed capability.

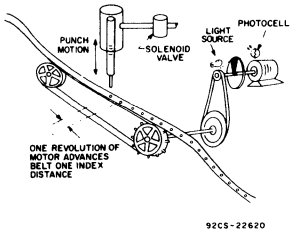


Fig. 42 – Step-and-punch machine.

The typical electromechanical control circuit for such a machine might consist of a mechanical cambank driven by a separate variable speed motor, a time delay relay, and a few logic and power relays. Assuming use of industrial-grade controls, the control system could get quite costly and large. Of greater importance is the necessity to eliminate transients generated each time a relay or switch energizes and deenergizes the solenoid and motor. Fig. 43 shows such transients, which might not affect the operation of this machine, but could affect the more sensitive solid-state equipment operating in the area.

A more desirable system would use triacs and zero-voltage switching to incorporate the following advantages:

a. Increased reliability and long life inherent in solid-state devices as opposed to moving parts and contacts associated with relays.

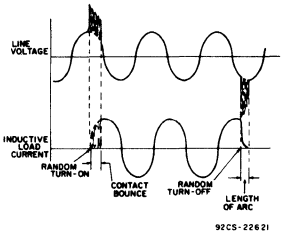


Fig. 43 – Transients generated by relay-contact bounce and non-zero turn-off of inductive load.

b. Minimized generation of EMI/RFI using zero-voltage switching techniques in conjunction with thyristors.
c. Elimination of high-voltage transients generated by relay-contact bounce and contacts breaking inductive loads, as shown in Fig. 42.
d. Compactness of the control system.

The entire control system could be on one printed-circuit board, and an over-all cost advantage would be achieved. Fig. 44 is a timing diagram for the proposed solid-state

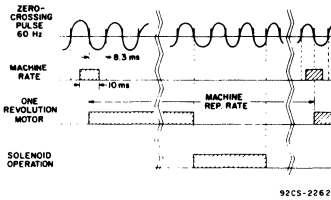


Fig. 44 – Timing diagram for proposed solid-state machine control.

SYNCHRONOUS LIGHT FLASHER

Fig. 50 shows a simplified version of the synchronous-switching traffic light flasher shown in Fig. 49.

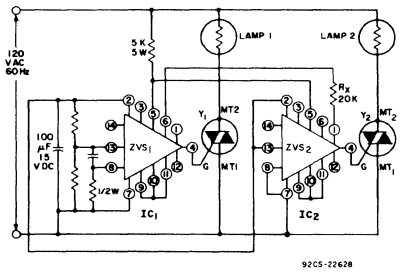


Fig. 50 – Synchronous light flasher.

Flash rate is set by use of the curve shown in Fig. 16. If a more precise flash rate is required, the ramp generator described previously may be used. In this circuit, ZVS_1 is the master control unit and ZVS_2 is slaved to the output of ZVS_1 through its inhibit terminal (terminal 1). When power is applied to lamp No. 1, the voltage of terminal 6 on ZVS_1 is high and ZVS_2 is inhibited by the current in R_x. When lamp No. 1 is off, ZVS_2 is not inhibited, and triac Y_2 can fire. The power supplies operate in parallel. The on-off sensing amplifier in ZVS_2 is not used.

TRANSIENT-FREE SWITCH CONTROLLERS

The zero-voltage switch can be used as a simple solid-state switching device that permits ac currents to be turned on or off with a minimum of electrical transients and circuit noise.

The circuit shown in Fig. 51 is connected so that, after the control terminal 14 is opened, the electronic logic waits until the power-line voltage reaches a zero crossing before power is applied to the load Z_L. Conversely, when the control terminals are shorted, the load current continues until it reaches a zero crossing. This circuit can switch a load at zero current whether it is resistive or inductive.

The circuit shown in Fig. 52 is connected to provide the opposite control logic to that of the circuit shown in Fig. 51. That is, when the switch is closed, power is supplied to the load, and when the switch is opened, power is removed from the load.

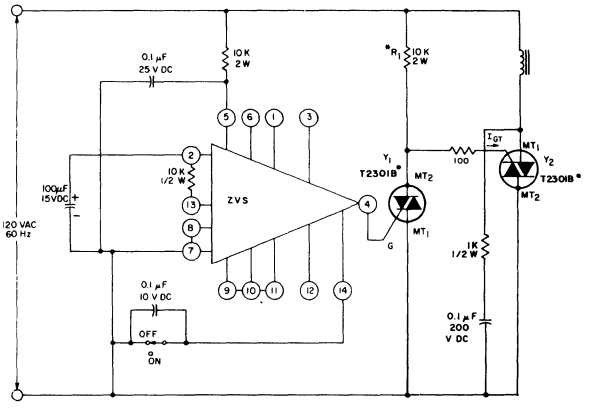
In both configurations, the maximum rms load current that can be switched depends on the rating of triac Y_2. If Y_2 is an RCA-2N5444 triac, an rms current of 40 amperes can be switched.

DIFFERENTIAL COMPARATOR FOR INDUSTRIAL USE

Differential comparators have found widespread use as limit detectors which compare two analog input signals and provide a go/no-go, logic 'one" or logic "zero" output, depending upon the relative magnitudes of these signals. Because the signals are often at very low voltage levels and very accurate discrimination is normally required between them, differential comparators in many cases employ differential amplifiers as a basic building block. However, in many industrial control applications, a high-performance differential comparator is not required. That is, high resolution, fast switching speed, and similar features are not essential. The zero-voltage switch is ideally suited for use in such applications. Connection of terminal 12 to terminal 7 inhibits the zero-voltage threshold detector of the zero-voltage switch, and the circuit becomes a differential comparator.

Fig. 53 shows the circuit arrangement for use of the zero-voltage switch as a differential comparator. In this application, no external dc supply is required, as is the case with most commercially available integrated-circuit comparators; of course, the output-current capability of the zero-voltage switch is reduced because the circuit is operating in the dc mode. The 1000-ohm resistor R_G, connected between terminal 4 and the gate of the triac, limits the output current to approximately 3 milliamperes.

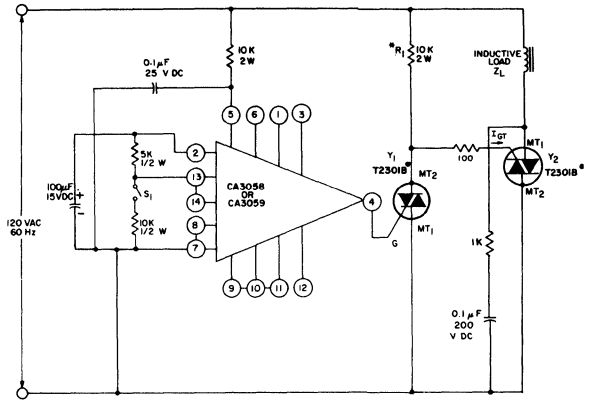
When the zero-voltage switch is connected in the dc mode, the drive current for terminal 4 can be determined from a curve of the external load current as a function of dc voltage



*IF Y_2, FOR EXAMPLE, IS A 40-AMPERE TRIAC, THEN R_1 MUST BE DECREASED TO SUPPLY SUFFICIENT I_{GT} FOR Y_2.

• FORMERLY RCA 40691

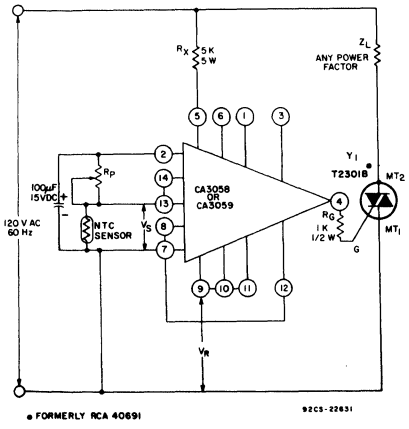
Fig. 51 – Zero-voltage switch transient-free switch controller in which power is supplied to the load when the switch is open.



*IF Y_2, FOR EXAMPLE, IS A 40-AMPERE TRIAC, R_1 MUST BE DECREASED TO SUPPLY SUFFICIENT I_{GT} FOR Y_2

• FORMERLY RCA 40691

Fig. 52 – Zero-voltage switch transient-free switch controller in which power is applied to the load when the switch is closed.



• FORMERLY RCA 40691

Fig. 53 – Differential comparator using the CA3058 or CA3059 integrated-circuit zero-voltage switch.

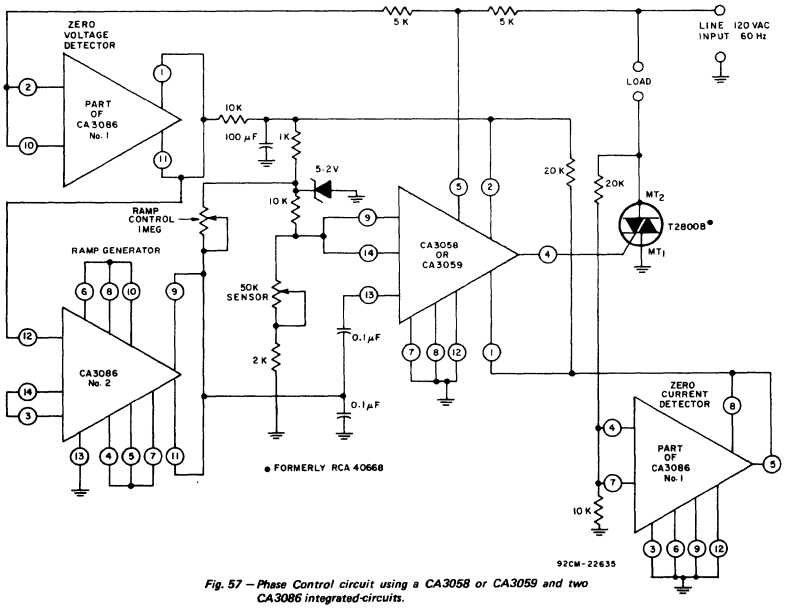


Fig. 57 – Phase Control circuit using a CA3058 or CA3059 and two CA3086 integrated-circuits.

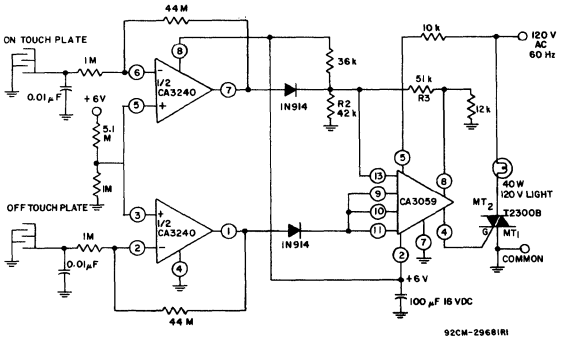


Fig. 58 – On-off touch switch.

control circuits. This signal must be electrically isolated from the three-phase power system.

3. Three separate triac gating signals are required.
4. For operation with resistive loads, the zero-voltage switching technique should be used to minimize any radio-frequency interference (RFI) that may be generated.

Isolation of DC Logic Circuitry

As explained earlier under **Special Application Considerations**, isolation of the dc logic circuitry* from the ac line, the triac, and the load circuit is often desirable even in many single-phase power-control applications. In control circuits for polyphase power systems, however, this type of isolation is essential, because the common point of the dc logic circuitry cannot be referenced to a common line in all phases.

In the three-phase circuits described in this section, photo-optic techniques (i.e., photo-coupled isolators) are used to provide the electrical isolation of the dc logic command signal from the ac circuits and the load. The photo-coupled isolators consist of an infrared light-emitting diode aimed at a silicon photo transistor, coupled in a common package. The light-emitting diode is the input section, and the photo transistor is the output section. The two components provide a voltage isolation typically of 1500 volts. Other isolation techniques, such as pulse transformers, magnetoresistors, or reed relays, can also be used with some circuit modifications.

Resistive Loads

Fig. 59 illustrates the basic phase relationships of a balanced three-phase resistive load, such as may be used in heater applications, in which the application of load power is controlled by zero-voltage switching. The following conditions are inherent in this type of application:

1. The phases are 120 degrees apart; consequently, all three phases cannot be switched on simultaneously at zero voltage.
2. A single phase of a wye configuration type of three-wire system cannot be turned on.
3. Two phases must be turned on for initial starting of the system. These two phases form a single-phase circuit which is out of phase with both of its component phases. The single-phase circuit leads one phase by 30 degrees and lags the other phase by 30 degrees.

These conditions indicate that in order to maintain a system in which no appreciable RFI is generated by the switching action from initial starting through the steady-state operating condition, the system must first be turned on, by zero-voltage switching, as a single-phase circuit and then must revert to synchronous three-phase operation.

Fig. 60 shows a simplified circuit configuration of a three-phase heater control that employs zero-voltage synchronous switching in the steady-state operating condition, with random starting. In this system, the logic command to turn on the system is given when heat is required, and the command to turn off the system is given when heat is not required. Time proportioning heat control is also possible through the use of logic commands.

The three photo-coupled inputs to the three zero-voltage switches change state simultaneously in response to a "logic command". The zero-voltage switches then provide a positive pulse, approximately 100 microseconds in duration, only at a zero-voltage crossing relative to their particular phase. A balanced three-phase sensing circuit is set up with the three zero-voltage switches each connected to a particular phase on their common side (terminal 7) and referenced at their high side (terminal 5), through the current-limiting resistors R4, R5, and R6, to an established artificial neutral point. This artificial neutral point is electrically equivalent to the inaccessible neutral point of the wye type of three-wire load and, therefore, is used to establish the desired phase relationships. The same artificial neutral point is also used to establish the proper phase relationships for a delta type of three-wire load. Because only one triac is pulsed on at a time, the diodes (D1, D2, and D3) are necessary to trigger the opposite-polarity triac, and, in this way, to assure initial latching-on of the system. The three resistors (R1, R2, and R3) are used for current limiting of the gate drive when the opposite-polarity triac is triggered on by the line voltage.

In critical applications that require suppression of all generated RFI, the circuit shown in Fig. 61 may be used. In addition to synchronous steady-state operating conditions, this circuit also incorporates a zero-voltage starting circuit. The start-up condition is zero-voltage synchronized to a single-phase, 2-wire, line-to-line circuit, comprised of phases A and B. The logic command engages the single-phase start-up zero-voltage switch and three-phase photo-coupled isolators OC13, OC14, OC15 through the photo-coupled

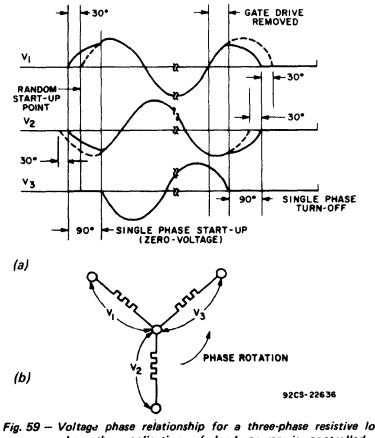


Fig. 59 – Voltage phase relationship for a three-phase resistive load when the application of load power is controlled by zero-voltage switching: (a) voltage waveforms, (b) load-circuit orientation of voltages. (The dashed lines indicate the normal relationship of the phases under steady-state conditions. The deviation at start-up and turn-off should be noted.)

* The dc logic circuitry provides the low-level electrical signal that dictates the state of the load. For temperature controls, the dc logic circuitry includes a temperature sensor for feedback. The RCA integrated-circuit zero-voltage switch, when operated in the dc mode with some additional circuitry, can replace the dc logic circuitry for temperature controls.

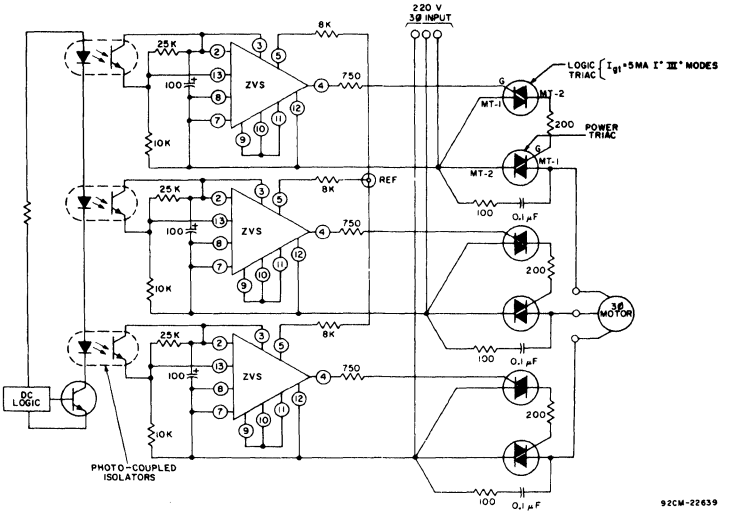


Fig. 62 – Triac three-phase control circuit for an inductive load, i.e., three-phase motor.

Considerations in Low-Noise Performance

Fig.5 shows the schematic diagram of a noise model useful in a review of the considerations pertinent to optimizing low-noise performance in amplifier operation.

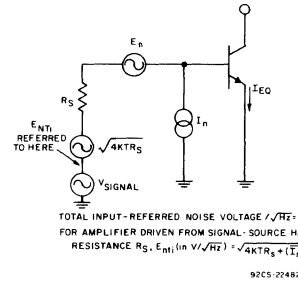


Fig. 5 – Sources of noise in the transistor-amplifier stage.

This model illustrates that consideration must be given to three major sources of noise:

1. Noise contributed by the "thermal-noise" voltage developed across the signal-source resistance, R_s. The magnitude of this voltage in $V/\sqrt{Hz}$ is approximately equal to $\sqrt{4KTR_s}$ for a 1-cycle bandwidth, where k is Boltzmann's constant (1.38 x 10^{-23} joule/°K), T is the temperature in degrees Kelvin, and R_s is the source resistance in ohms.
2. The noise voltage, E_n, resulting from the combined effects of shot noise due to emitter current flow and thermal noise due to transistor base resistance. These effects add in rms fashion to give a total E_n equal to $(E_{shot}^2 + 4KTr_b')^{1/2}$. The shot-noise component, E_{shot}, is inversely proportional to the square root of I_{EQ}, and has a value

$$E_{shot} = \frac{14.2 \times 10^{-12}}{\sqrt{I_{EQ}}} (V/Hz.)$$

   In super-beta transistors, the base resistance component of E_n tends to dominate, particularly at currents greater than 10 microamperes. In addition, this component of E_n has been experimentally found to be inversely related to operating current. Therefore, the total value of E_n is inversely related to operating current I_{EQ}. For example, the CA3095E has a total 1-kHz E_n of approximately 15 nV/$\sqrt{Hz}$ at a collector current of 5 microamperes and approximately 8 nV/$\sqrt{Hz}$ at 50 microamperes.
3. The noise current, I_n, resulting from the combined "shot noise" generated by the flow of base current and the 1/f noise generated in the transistor. The magnitude of I_n is approximately proportional to $\sqrt{I_{IB}}$, where I_{IB} is the base current. The value of I_n is typically 0.12 pA/$\sqrt{Hz}$ at f = 10 Hz when the super-beta differential-cascode amplifier in the CA3095E is operating at I_{EQ} = 5 μA. I_n decreases to approximately 0.03 pA$\sqrt{Hz}$ at f = 1 kHz.

When each input terminal in a differential amplifier is driven from a source resistance (R_s), the total noise voltage (referred to the input, see Fig. 5) per unit bandwidth is given by:

$$E_{nti}\ (in\ V/\sqrt{Hz}) = \sqrt{2KTR_s + 2(\overline{I_nR_s})^2 + (E_n)^2}$$

When amplifiers are driven from low source impedances, E_n is the predominant factor in noise contributions, whereas the effect of I_n predominates when input signals are supplied from high source impedances. Consequently, since the CA3095E operates with very high beta at very low operating currents, it has exceptionally low values of I_n, and is an excellent choice to amplify signals from high source resistances when low amplifier noise contribution is desired. Additionally, the incidence of "popcorn" (burst) noise[2] is low in the CA3095E, a characteristic which further enhances its suitability for use in amplifying signals supplied from high-impedance sources. Figs. 6 and 7 show typical data on I_n and E_n characteristics, respectively, as a function of frequency, for the super-beta transistors in the CA3095E.

Because the operating current of the super-beta transistors in the CA3095E is adjustable over a wide range, the circuit designer can optimize the operating current for maximum

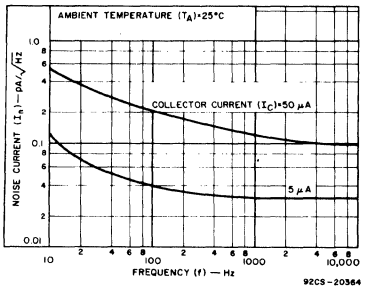


Fig. 6 – Noise current I_n as a function of frequency f for each super-beta cascode-amplifier transistor pair (Q_1 - Q_3 and Q_2 - Q_4).

signal-to-noise ratio at a particular frequency and source resistance. This adjustment is accomplished by selecting an operating point for which E_n is approximately equal to $\sqrt{2}\,I_n\,R_s$. For example, the optimum operating collector currents in the differential-cascode amplifier are about 5 microamperes when the amplifier is to be driven from two 300-kilohm source resistors. For operation from higher source resistances, the currents should be proportionately lower, and vice versa. Operating currents in the range from 0.1 to 1.0 milliampere are recommended when the amplifier is to be operated as a low-noise video amplifier. At these current levels, the gain-bandwidth product (f_T) is increased significantly with respect to low collector current operation.

ILLUSTRATIVE CIRCUIT APPLICATIONS

Like other RCA transistor-array IC's, the CA3095E offers the circuit designer a class of solid-state devices featuring matched electrical and thermal characteristics, compactness, ease of physical handling, economy, and versatility of use. The

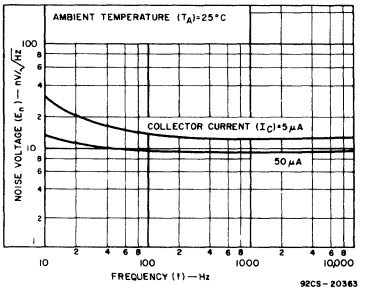


Fig.7 – Noise voltage E_n as a function of frequency f for each super-beta cascode-amplifier transistor pair (Q_1–Q_3 and Q_2–Q_4).

CA3095E is an electronic "building block" which permits the designer to optimize performance of a particular circuit for gain, noise, power consumption, bandwidth, and/or other specific considerations. Some typical circuit applications of the CA3095E are described below.

High-Input-Resistance Low-Noise Amplifier

The CA3095E contains all the transistors necessary for the construction of a low-noise, feedback amplifier having a high input resistance ($R_{IN} \cong 20$ MΩ) and a 3-dB bandwidth of about 50 kHz. In the circuit shown in Fig. 8, voltage gain is provided by a cascade of two stages, the differential-cascode stage (Q_1, Q_3 - Q_2, Q_4) and the differential stage (Q_7, Q_8). Transistor Q_6 is an interstage emitter-follower. The voltage gain of the amplifier (approximately 30 dB with the circuit values shown) is essentially established by the ratio of R_8 to the parallel combination of R_5 and R_6. The R_8, C_2 network couples feedback around the entire amplifier. Capacitor C_4 provides stabilizing compensation. The output-voltage swing (E_O) is typically 3 volts, peak-to-peak. Typical noise-figure data are shown in Fig. 8. Power consumption of the amplifier

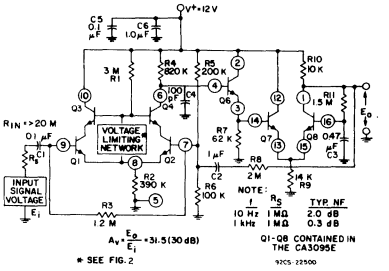


Fig. 8 – High-input-resistance, low-noise amplifier circuit.

is typically about 750 microamperes at a supply voltage of 12 volts, although the current in transistors Q_1 and Q_2 is less than 5 microamperes.

Low-Noise Video Amplifier

The circuit shown in Fig. 9 illustrates the use of super-beta transistors in the input stage of a video amplifier. The circuit is capable of delivering 4 volts, peak-to-peak, of output signal with a typical gain of 33 dB across a bandwidth from dc to 10 MHz (3-dB point). In this application, each super-beta transistor is biased for operation at about 400 microamperes to achieve wideband operation. The super-beta transistor characteristics minimize the contributions to noise generated by noise current (I_n) in the input stage. The equivalent input-noise-voltage-vs-frequency characteristics for the entire amplifier circuit are shown in Fig.10. Transistors Q_1 through Q_4 are connected as an emitter-coupled pair of cascode amplifiers with a single-ended load resistor, R_3, to drive a discrete transistor Q-PNP. This combination provides sufficient current gain to drive Q_6, the voltage-gain-stage transistor, with load resistor R_8. Resistor R_7 provides a path for dc and ac feedback around this stage. Transistor Q_8 is an emitter-follower output stage. The typical current drain of the amplifier is approximately 8 milliamperes at a total supply voltage of 10 volts.

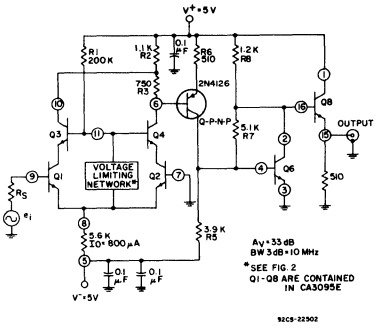


Fig. 9 – Video amplifier.

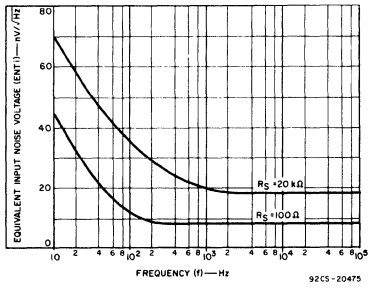


Fig. 10 – Equivalent input noise voltage vs frequency for the circuit of Fig. 9.

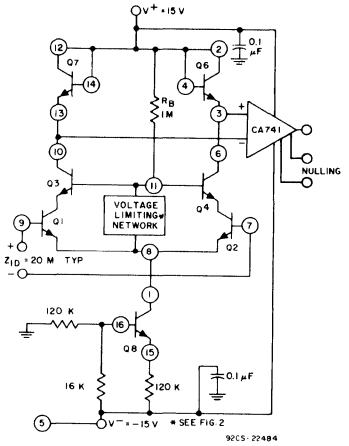


Fig. 14 – Op-amp with unity gain preamplifier.

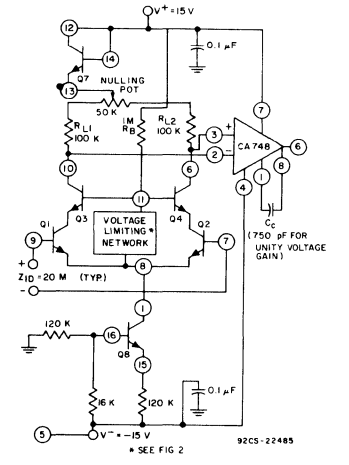


Fig. 15 – Op-amp with high-gain preamplifier.

reactance of the coupling capacitor C must be much lower than 5 megohms to achieve the high-input-impedance characteristic described above.) The low-drift, long-time-constant integrator circuit shown in Fig. 16(b) is another excellent application for the CA3095E super-beta transistor array. Because exceedingly low input bias currents permit the use of a high-value integrating resistor, R, without introducing substantial error, long-time-constant integration can be accomplished. The low input-offset-voltage drift characteristic of the super-beta transistors also contributes to low-error performance. Further reductions in error effects, particularly with temperature variation, can be achieved by using a temperature compensated bias-current source (e.g., R_1–R_3, D_1). In the circuit of Fig.15, such an arrangement could be implemented by using Q_6 in a diode connected fashion to serve as D_1. With such an arrangement, temperature-compensated bias current is applied to the inverting input terminal.

High-Input-Impedance DC-Voltmeter Circuit

The combination of a preamplifier circuit using the CA3095E in conjunction with a CA748 op-amp as described above is adaptable to dc-voltmeter circuits requiring high input impedance, as illustrated by the circuit of Fig. 17. An appropriate resistor-divider network is provided to develop a dc input signal at terminal 9 of the CA3095E with transistors Q_1 - Q_3 and Q_2 - Q_4 connected in the differential-cascode

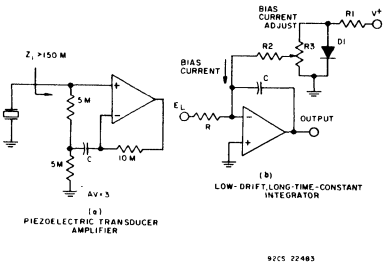


Fig. 16 – Typical super-beta op-amp applications:
(a) piezoelectric transducer amplifier
(b) low-drift, long-time-constant integrator.

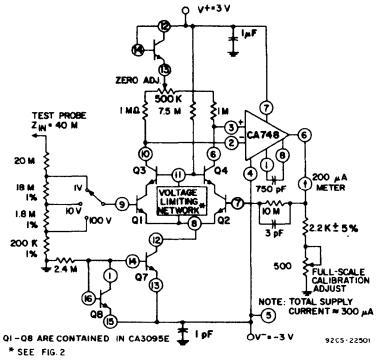


Fig. 17 – Typical high-input-impedance dc-voltmeter circuit.

arrangement. Biasing and dc feedback are applied at terminal 7 of the CA3095E through a 10-megohm resistor. The CA748 op-amp drives a 200-microampere meter calibrated in terms of the voltages to be measured. A full-scale reading occurs when the voltage applied to pin 9 is 500 millivolts dc. The entire circuit is nulled with the 500-kilohm zero-adjustment potentiometer. The total power-supply requirement is only 6 volts with a supply current of only 300 microamperes; this requirement can be met with batteries. The input impedance of this simple circuit is approximately 40 megohms on all scales.

Preamplifier for Tape-Head Signals

The exceptional low-noise characteristics of the CA3095E make it suitable for preamplifier service in professional-grade tape-playback systems. A typical circuit with equalization for NAB standards (7.5 in/s) is shown in Fig. 18. Transistors Q_1 and Q_3 are cascode-connected as the input stage, and transistor Q_6 is connected as a common-emitter post-amplifier. Transistors Q_2 and Q_4 are non-conductive because the emitter-base junction in Q_2 and the base-collector junction in Q_4 are shunted by external wiring. Equalization for the NAB tape-playback, frequency-response characteristics is provided by the R_1, C_1, C_2 network connected in the ac feedback path; DC feedback stabilization is provided by the path through resistor R_2. The amplifier has an over-all gain of about 37 db at 1 kHz, and can deliver output voltages in the order of 25 volts, peak-to-peak. The circuit configuration of Fig.18 is preferred to the differential-amplifier configuration because it limits the input-noise contribution to that of a single transistor (e.g., Q_1).

Preamplifier for Signals from Magnetic-Phonograph Cartridges

The exceptional low-noise characteristics of the CA3095E are also of great use in preamplifier service in equipment used to reproduce signals from magnetic phonograph cartridges. A typical circuit for this application with equalization for RIAA

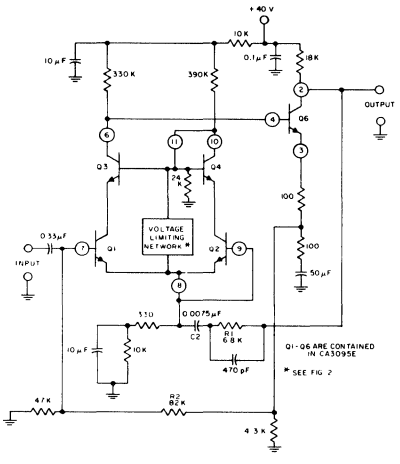


Fig. 18 – Tape play-back preamplifier equalized for NAB standards (7.5 in/s).

playback standards is shown in Fig. 19. Transistors Q_1 and Q_3 are cascode-connected as the input stage, and transistor Q_6 is connected as a common-emitter post-amplifier. Transistor Q_2 and Q_4 are non-conductive because the emitter-base junction in Q_2 and the base-collector junction in Q_4 are shunted by external wiring. Equalization for the RIAA phonograph-frequency-response characteristics is provided by the R_1, C_1 network connected in the ac feedback path. DC feedback stabilization is provided by the path through resistor R_2. The amplifier has an over-all gain of about 40 dB at 1 Hz, and can deliver output voltages in the order of 25 volts, peak-to-peak. The dynamic range of these circuits is typically about 95 dB with the gains indicated.

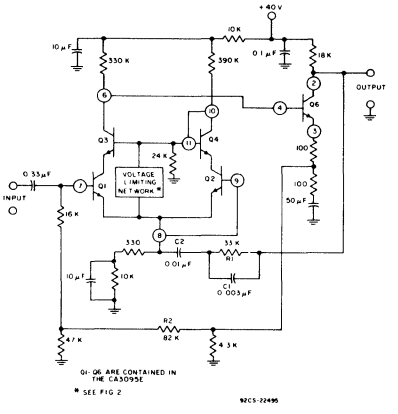


Fig. 19 – Preamplifier equalized for RIAA standards applicable to magnetic phonograph catridges.

ACKNOWLEDGMENT

The circuits of Figs. 18 and 19 were designed by L.A. Kaplan.

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1. "Super-Beta Transistor Array," CA3095E, RCA Data File No. 591.
2. "Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits," T. J. Robe, RCA Application Note ICAN-6732.
3. "Operational Amplifiers," RCA Data File No. 531.

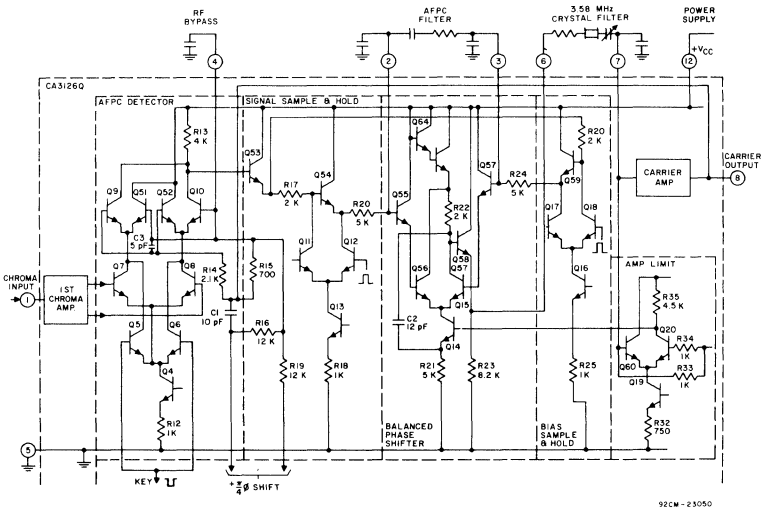


Fig. 3– Subcarrier regeneration circuit.

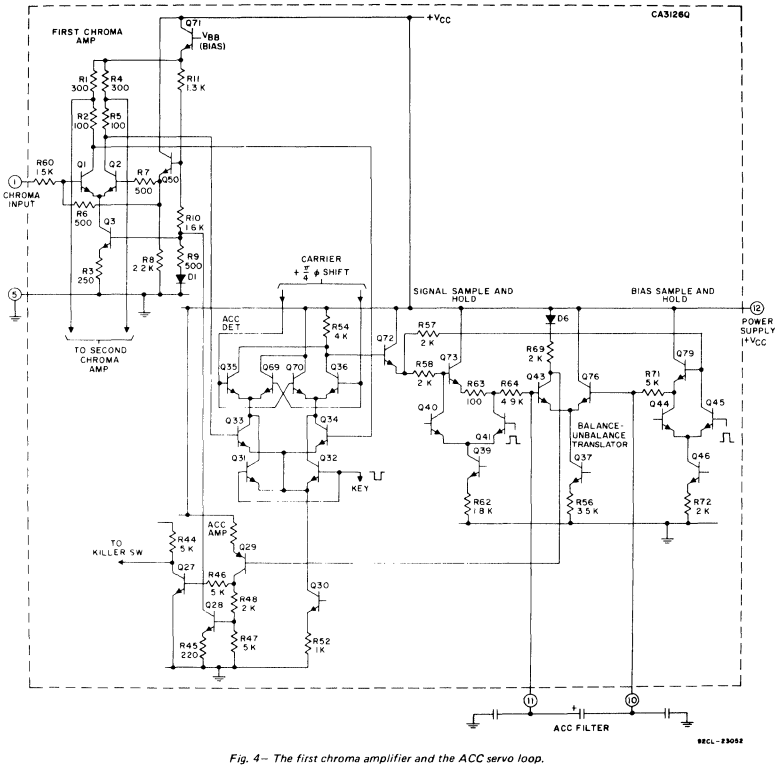


Fig. 4– The first chroma amplifier and the ACC servo loop.

detector from the switching pulses generated in the sampling circuits. The sample-and-hold action is accomplished by controlling the conduction current in transistor Q_{54} thus alternating the charge path during those intervals. During the sampling interval, transistor Q_{54} conducts and its emitter exhibits a relatively low impedance in comparison with the value of the integrated charging resistor R_{20}. The detected or sampled signal is stored in the AFPC filter capacitor which, with R_{20}, determines the time constant during this time interval. During the hold period, transistor Q_{54} is off and the filter time constant is several orders of magnitude larger than previously. The discharge of the filter capacitor is reduced to very small base bias currents only and little of the stored information is lost.

The "on" and "off" condition of the transistor Q_{54} is determined by the state of the transistor-pair Q_{11} and Q_{12}. During the "on" (sampling) interval, a signal from the horizontal rate keyer disables transistor Q_{11} and the collector current of the transistor Q_{12} maintains the transistor Q_{54} in the "on" condition. During the "off" (hold) period, transistors Q_{11} and Q_{12} change their states and the transistor Q_{54} is "off".

The bias sample-and-hold circuit, similar in structure to the above-described circuit, consists of the sampling switch Q_{59} and the transistor-pair Q_{17} and Q_{18}. This circuit, also activated by a signal from a horizontal rate keyer, samples the quiescent potential of the phase detector. The two signals, the error and the bias, processed by the sampling circuits, are stored in filter capacitors, and are applied to opposite terminals of a differential phase control. The phase control circuit synchronizes the reference carrier produced by the VCO.

Depending on the free-running frequency of the VCO, the detected signal is in the form of positive or negative going pulse trains which are then stored in a filter capacitor. The sampling switch has equal drive capabilities for both polarities of the signal; a requirement of particular importance in the presence of noise signals. Non-linear operation of the detector and sampling circuit would produce a rectified dc component causing an erroneous detuning of the VCO.

The VCO Loop

The amplification and amplitude limiting of the oscillator signal takes place in the amplifier-limiter formed by the transistor-pair Q_{60} and Q_{20}. The output from Q_{20} is fed to the dc controlled phase-shifter and returns to the amplifier through a crystal filter. The amplifier operates in a non-inverting mode, hence, the total phase shift through the phase-shifter plus crystal filter must be a multiple of 2π radians. The crystal filter is tuned to the subcarrier frequency and the filter band-width is determined by a resistor in series with the crystal. The DC controlled phase-shifter has a phase range of approximately $\pm \frac{\pi}{4}$ radians, and a phase change activated by a control signal results in a corresponding oscillator frequency change.

In the phase-shifter, the oscillator signal available at the collector of Q_{20} is applied to the base of Q_{14} from which it proceeds along two paths. An integrated capacitor C_2 couples this signal from the emitter of Q_{14} to the collector load of Q_{15} and, at this point, the signal is phase-shifted by approximately $\pi/4$ radians. In the second path, the signal arriving at the collector of Q_{15} passes through a current splitter formed by the transistor-pair Q_{56}, Q_{15}. This signal is reduced to a level determined by the control voltage at the bases of transistors Q_{56} and Q_{15}. At one extreme, transistor Q_{15} is OFF and the signal at the collector of Q_{15} arrives through the capacitor C_2 only. Conversely, with transistor Q_{15} ON, and Q_{56} OFF, the signal arriving through the transistor Q_{15} is phase-oriented so that the resultant signal has a phase of $+3/4\ \pi$ radians. The phase-control is linear throughout most of the control range.

A buffer amplifier is used to supply the CW carrier required for the demodulators, and the carrier is available at terminal 8. Internally, the buffer amplifier supplies the two synchronous detectors. Two R-C phase-shifters fed from the buffer amplifier provide the required phase orientation. A low-pass R_{14}-C_3 filter shifts the carrier to the AFPC detector by $-\pi/4$ while a high-pass filter provides a $+\pi/4$ oriented carrier for the ACC-killer detector.

AMPLITUDE CONTROL OF THE CHROMINANCE SIGNAL

Two cascaded amplifier stages serve to process the chroma signal and several signals are developed to control the gain of each stage.

First Chroma Amplifier and ACC Servo Loop

The first chroma amplifier, shown in Fig. 4, is controlled by the burst responsive ACC-killer detector only. The amplifier formed by the transistor-pair Q_1, Q_2 is driven single-ended by the applied composite chroma signal. The amplified output from this stage drives differentially the synchronous ACC-killer detector. The gain of the first amplifier is a function of the dc emitter current supplied by the constant current source Q_3. This current source is biased to provide a nominal current and, hence, a nominal gain in the first amplifier stage. The bias of the current source is reduced in response to a detected burst signal and the gain of the first stage diminishes correspondingly.

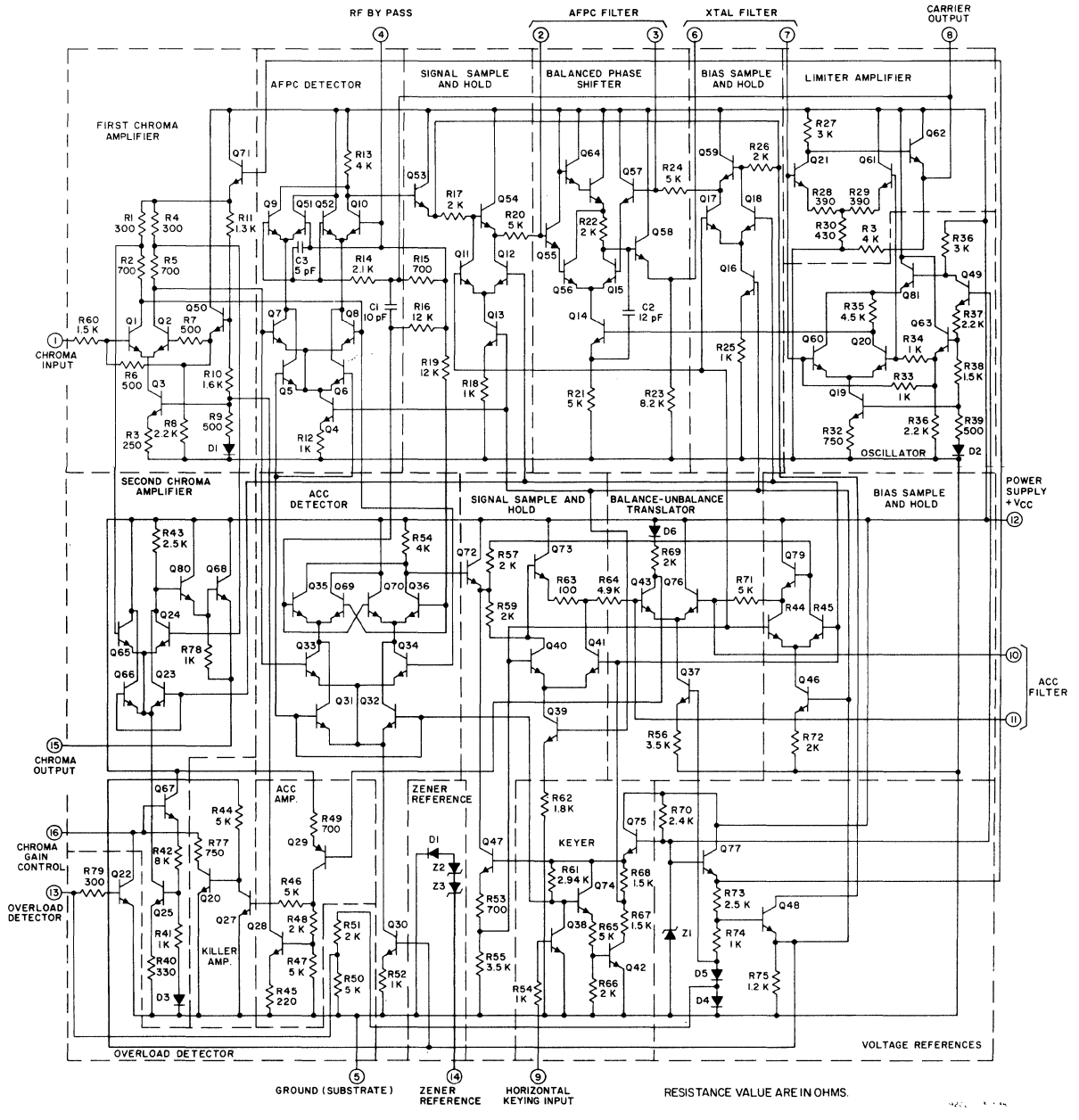


Fig. 7– Complete circuit diagram showing details of the keying circuit and internal bias circuits.

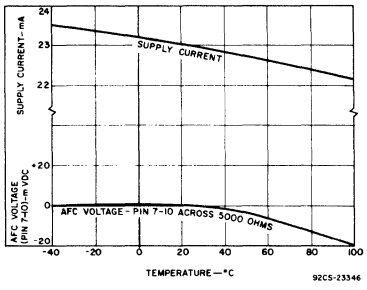
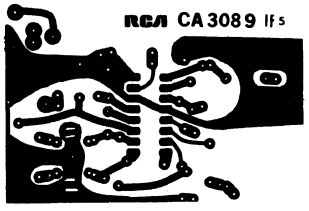


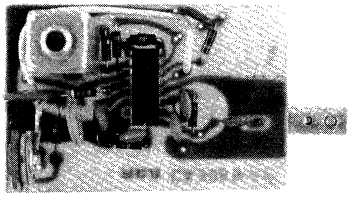
Fig. 7– Supply current and AFC voltage as a function of temperature.

exhibit inductive reactance at their terminals. The nominal input impedance of the CA3089E is approximately 9,000 ohms, and it is not recommended that an impedance match be attempted. Most commercial receivers use ceramic-filter frequency-selective elements that normally have source impedances of 500 ohms or less. When these filters are properly terminated with loading resistors, the typical source impedance is further decreased to 250 ohms or less. Higher levels of source impedance are possible with very careful circuit layout; however, the maintenance of stability could be difficult.

The CA3089E has a frequency response that is typically flat to 20 MHz; consequently, the device can provide useful gain well above that frequency. If the device is used at lower frequencies, the larger-value bypass capacitors required may not be adequate to bypass the higher frequencies. Double bypassing with lower-value capacitors can overcome such a problem. Another means of alleviating the problem is to externally reduce the frequency response by using a small capacitance across the output load of the device.



a) Bottom view of printed-circuit board.

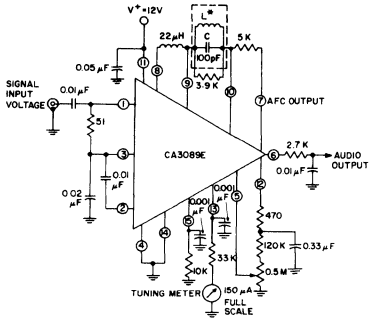


b) Component side — top view.

Fig. 8.– CA3089E and outboard components mounted on a printed circuit board.

Quadrature-Detector Circuits

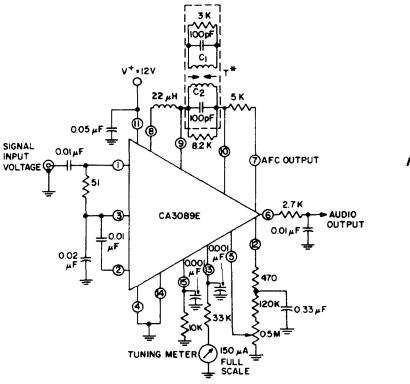
The quadrature-detector tuned circuit is connected between pins 9 and 10. The signal voltage at pin 8 is normally coupled to pin 9 through a choke. The circuit values for the detector network are determined by several factors, the primary one being distortion at a particular level of recovered audio. Distortion is determined by the phase linearity of the quadrature network and is not influenced by the device unless excessive, recovered audio overdrives the audio circuit. With a single tuned network, the phase linearity improves as the bandwidth increases; however, recovered audio decreases. A satisfactory compromise for most FM-receiver applications is reflected in the circuit of Fig. 9(a). This circuit typically provides 400 millivolts rms of recovered audio with less than 0.5-percent distortion. Because a double-tuned circuit has better phase linearity over a wider bandwidth, distortion figures of less than 0.1-percent are attainable with the network used in the circuit of Fig. 9(b). Proper alignment and coupling adjustment of the double-tuned circuit are most easily accomplished while viewing the resulting S curve. Initial adjustment of the primary tuning slug to the proper crossover is made with the secondary slug removed. The secondary tuning slug is then



ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O(UNLOADED) ≅ 75 (G.I. AUTOMATIC MFG. DIV. EX22741 OR EQUIVALENT)

92CM-19040R1

(a)



ALL RESISTANCE VALUES ARE IN OHMS
*T: PRI. – Q_O(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20 t OF 34 ø ON 7/32" DIA. FORM
SEC. – Q_O(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20 t OF 34 ø ON 7/32" DIA. FORM
kQ (PERCENT OF CRITICAL COUPLING) ≅ 70 %
(ADJUSTED FOR COIL VOLTAGE V_C = 150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4 mm

92CM-19041R1

(b)

Fig. 9– (a) Test circuit for the CA3089E using a single-tuned detector coil, (b) test circuit for the CA3089E using a double-tuned detector coil.

adjusted until a slight "ripple" is observed moving along the S curve. If the ripple is excessive (enough to distort the S curve) the coupling is too tight. If no ripple is observed, the coupling is too loose. As the ripple moves through the crossover point, it will be observed that the S curve becomes more linear near the center frequency. Slight readjustment of both slugs may be necessary for final alignment. The best performance can then be achieved by slight adjustment while measuring distortion. The coupling may be varied by either moving the coils or by changing the value of the secondary load resistor.

Various circuit values can be used to obtain the same recovered audio, but the basic conditions of circuit bandwidth and phase linearity must be maintained. The detector circuit also sets up conditions which are required for proper operation of the mute circuit. The rf voltage on pin 9 must be held at approximately 175 millivolts rms, ±25 millivolts. The reason for this requirement is discussed subsequently in connection with the mute logic circuit. The approximate voltage at pin 9 is determined from the equivalent circuit shown in Fig. 10.

The peak-to-peak voltage on pin 9 is:

$$|V_9| \cong |V_8| \frac{R1}{\omega L_{ch}}$$

where R1 is the total parallel resistance and V8 is approximately 300 millivolts, peak-to-peak.

The Q of the tuned circuit between pins 9 and 10 may be affected by the effective Q of the choke between pins 8 and 9 and the series resistor R31 in the CA3089E. All of the above factors should be considered in selecting circuit values. Table I lists some typical combinations of component values under various conditions.

A choke is normally selected to equalize delays in the signal path and in the limiter–quadrature path. It also reduces the if harmonic content across the quadrature circuit. In some cases, such as in narrow-band applications, it may become necessary to use a capacitor as the coupling component where large values of inductance with high Q's are difficult to obtain. If a capacitor is used, the phase of the recovered audio and AFC voltage will be reversed, some asymmetry of the S curve may result, and the distortion may be adversely affected to a small degree.

As indicated above, the inductance between pins 8 and 9 tends to equalize delays in the detector signal paths. The matching of elements of the IC in the balanced detector

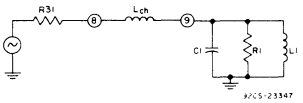


Fig. 10– Equivalent circuit used to determine approximate voltage on pin 9 of the CA3089E in Fig. 9.

circuit results in an AFC output with a very small offset when referred to the voltage at pin 10. For most applications, the inherent offset variation is well within tolerances, and does not affect circuit performance. In some narrow-band applications, however, the offset becomes more critical because of the very narrow bandwidth. In such situations, the combination of normal production variations of the device and the external circuit components results in receiver detuning when the AFC loop is closed. This detuning results in an increased distortion of the recovered audio. This distortion can be corrected with the addition of a variable capacitor from pin 8 to ground to provide phase compensation. The capacitor can be adjusted to provide zero AFC offset with minimum distortion. Generally, the offset is in one direction for a given set of conditions. The addition of a fixed capacitor will minimize variations sufficiently to satisfy many applications. A value of 5 picofarads is an effective value for the circuit of Fig. 9(a) with the recommended PC-board layout. Conversely, the offset created by using a capacitor between pins 8 and 9, as mentioned earlier, may be compensated by placing an inductance between pins 8 and 10.

Audio and AFC Circuits

The audio and AFC circuits are very similar, and both develop the same audio signal at their respective output terminals. The audio output voltage on pin 6 is developed across an internal, nominal, 5,000-ohm resistor (R49) connected to the 5.6-volt reference. In addition, the audio signal level can be attenuated by providing a direct current into pin 5 without any shift in its dc level. The audio output,

455 kHz without the use of external circuitry. The rf-AGC and mute logic circuits do not develop sufficient dc voltage

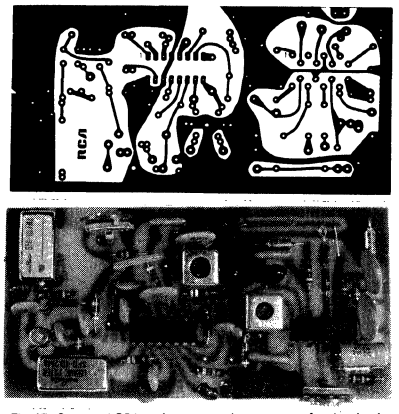


Fig. 15—Suggested PC-board pattern and parts layout for the circuit of Fig. 14.

to perform their functions, and the meter output signal loses its logarithmic characteristic and exhibits peaks and valleys as input signal is increased. Operation of the rf-AGC and mute logic circuits may be enhanced by the addition of a dc amplifier and inverter to each circuit. A simple example using a CA3096E IC transistor array is shown in Fig. 16.[3]

The CA3089E may be used effectively in narrow-band communication receivers. In double-conversion receivers, some of the functions of the CA3089E are negated at a 455-kHz intermediate frequency. However, if a 10.7-MHz intermediate frequency is used, all of the auxiliary features

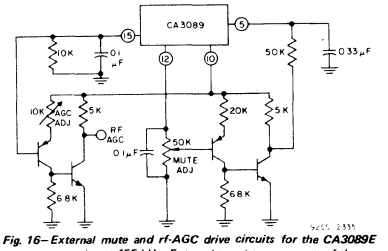


Fig. 16—External mute and rf-AGC drive circuits for the CA3089E operating at 455 kHz. External transistors are parts of the CA3096E n-p-n/p-n-p transistor array.

may be used, but another set of problems is encountered. The small deviation signals encountered in narrow-band systems require the use of high-Q circuits in the quadrature detector, as indicated in Table I. However, variations in external-component parameters with temperature changes may cause the tuned frequency of the detector to drift out of the if pass band. Normally temperature-compensated components are necessary. The CA3089E, operating in conjunction with an inexpensive operational transconductance amplifier,[4,5] provides means of locking the tuned circuit to the incoming frequency. Fig. 17 shows the block diagram of such a system. The AFC output voltage developed across the resistor between pins 7 and 10 is amplified by the op-amp and drives a varactor to maintain the tuned frequency on the incoming-signal frequency.

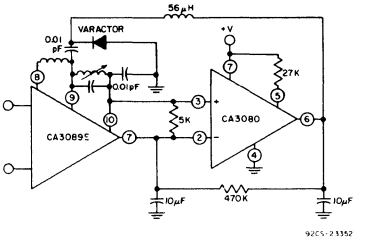


Fig. 17—Detector frequency-stabilization circuit.

The CA3089E may also be used as the core of an ultra-linear FM generator; Fig. 18 shows the circuit. The carrier is generated by the CA3089E with the introduction of feedback from the output terminal, pin 8. The carrier is modulated by the varactor connected across the tuned circuit at the input of the CA3089E. The varactor is driven by the output of the differential amplifier, A1, using a CA3028 IC.[6,7] This differential-amplifier stage is driven at one of its input terminals by the audio modulating signal. Negative feedback of the audio signal is provided by driving the other differential-amplifier input from the recovered audio output of the CA3089E at pin 6. The detector circuit uses a double-tuned transformer to produce audio with very little distortion at pin 6. This feedback technique results in a very low distortion modulation. The rf output of the CA3089E at pin 8 is essentially a square wave, and is fed to a tuned-amplifier stage to buffer the signal and restore the sine-wave-shaped rf output signal.

Acknowledgments

The author thanks Jack Craft for his aid and suggestions in many discussions and Frank Curley for his aid in circuit construction and collection of data.

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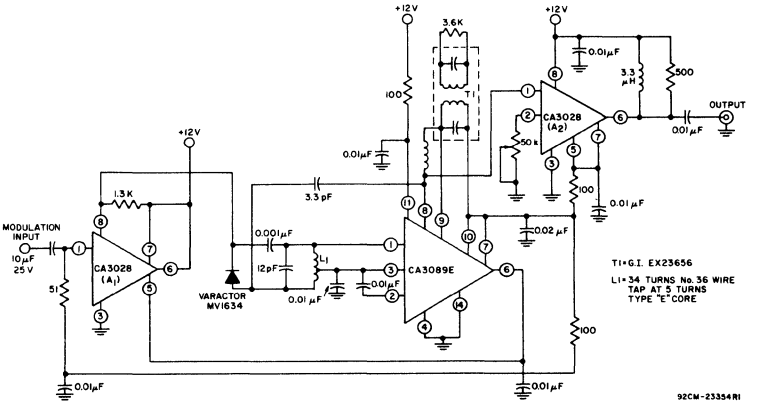


Fig. 18—FM generator circuit.

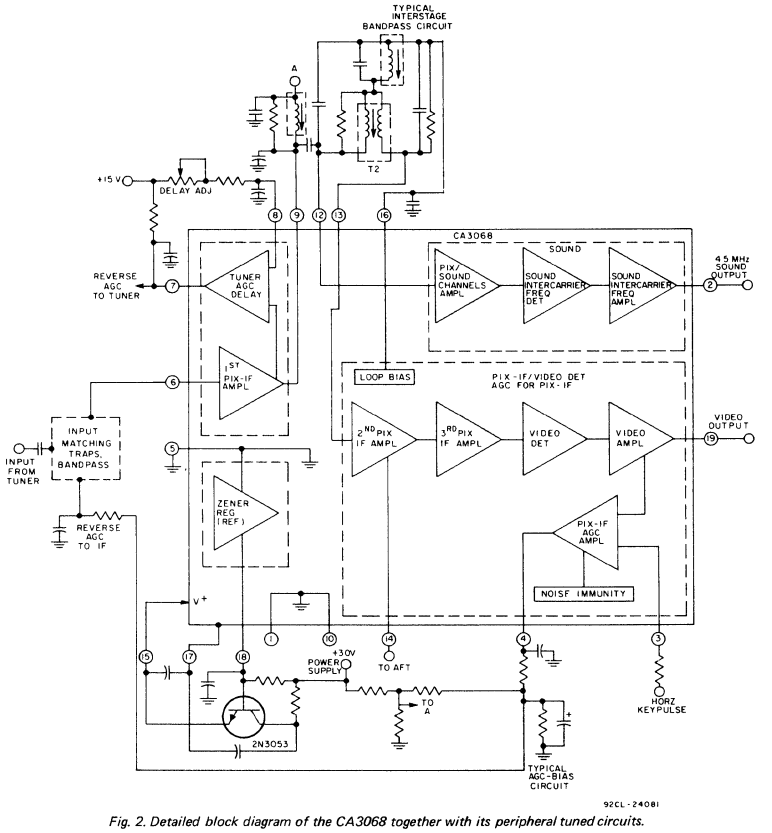


Fig. 2. Detailed block diagram of the CA3068 together with its peripheral tuned circuits.

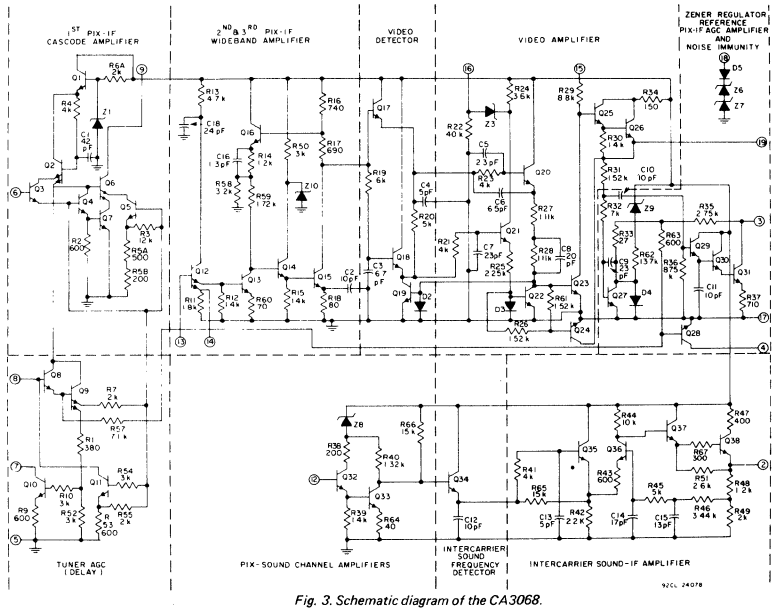


Fig. 3. Schematic diagram of the CA3068.

this composite waveform drive the keyed agc amplifier Q27, which in turn drives Q28. Without a video rf signal there is no video signal output, and Q27 conducts during the keying intervals (the horizontal pulse is connected to terminal 3). As the detected signal level increases in amplitude and the output voltage at terminal 19 approaches its typical operational level of 7 volts peak-to-peak, the peak potential at the base of Q27 begins to fall below 0.8 volt. Under these conditions, the keying current formerly channeled through Q27 is diverted through diode D4. As the signal level rises even higher, a greater portion of the Q27 collector current is diverted through D4, and the base current to Q28 is proportionately increased. A 10-microfarad capacitor is normally connected between terminal and ground and is, by this connection, put in shunt with Q28. The charge on this external capacitor is maintained through a bleeder resistor to V+. As the base current to Q28 increases, Q28 discharges the capacitor at a rate that is proportional to the base current of Q28. Integration of the total charge on the capacitor over the keying interval yields a dc level (agc voltage) that is inversely proportional to the incoming signal level; i.e., agc voltage approaches zero as the signal increases.

Any high-performance agc system must have noise-immunity characteristics in order to avoid the establishment of false agc levels. AGC developed from random noise can produce "wash-out", "blank raster" and/or a momentary "loss of sync". The CA3068 is designed with an improved noise-immunity circuit that essentially removes the keying current during periods of high noise input. The active devices responsible for providing protection against this deleterious effect of the impulse noise are the "noise detector", Q29, and the "noise clamp" Q31, which is driven by Q30. Impulse noise is channeled through the high-pass filter network consisting of C10 and R36 to the detector input Q29. Q29 and C11 comprise a conventional peak detector. The dc level across C11, which is proportional to the level of impulse noise, turn on Q30 and Q31, thereby clamping the keying supply voltage (terminal 3) to ground. In actual operation, the terminal-3 supply has a series resistance that is large enough to limit the peak current into the zener diode (Z5) to approximately 0.8 milliampere. When Q31 conducts, it shunts this current to ground.

The sound-if-channel and PIX-IF-channel signals whose "carrier" frequencies are 41.25 MHz and 45.75 MHz, respectively, are applied to terminal 12. Q32 functions as a buffer between the interstage-tuned-circuits associated with terminal 12 and the PIX/sound-channels amplifier, Q33. The intercarrier frequency (the difference frequency between the PIX and sound "carrier" frequencies) is detected by the peak detector Q34 and C12. The resultant 4.5 MHz FM sound-intercarrier signal is fed to transistor Q35. This transistor and Q36 form a differential pair that provides an amplified intercarrier sound-if signal to the base of Q37. A feedback system through the RC networks in the Darlington emitter-follower output of Q37 provides bandpass shaping in the region of 4.5 MHz while maintaining a low dc gain. The low level of dc gain is desirable because the circuit receives its bias in an open-loop manner from terminal 16. The bandpass of this amplifier system is fairly broad, and even though it is optimized for 4.5 MHz operation, there is relatively high output at other intercarrier frequencies, as shown in the curve in Fig. 4.

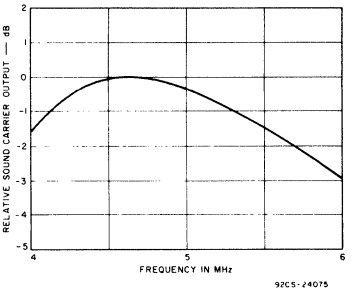


Fig. 4. Relative sound-carrier output as a function of frequency.

The internal zener reference-diode consists of the series diode arrangement shown connected between terminal 18 and the substrate in Fig. 3. A regulator-circuit configuration showing the

itor connected between terminal 4 and ground. An RC decoupling network smooths the age ripple associated with the charge and discharge of the 10-microfarad capacitor at the horizontal-oscillator frequency rate. The age system is normally keyed from the horizontal-output circuit in the TV system. This keying pulse should be applied to terminal 3. The magnitude of the pulse should be sufficient to supply a nominal peak current value of 0.8 milliampere into terminal 3. The value of the series resistor R_S associated with terminal 3 may be computed as follows: During the conduction period (with keying applied), the constant-voltage components within the integrated circuit account for:

$V_k = 8.2$ V

(It is assumed that I3 = 0.8 mA)

If the keying-pulse magnitude, V_p, is 15 V, then:

$$I3 = 0.8\ \text{mA} = \frac{15 \cdot V_k}{R_S} = \frac{(15 \cdot 8.2)\ \text{V}}{R_S}$$

$R_S = 8.5$ kilohms

The sound output is derived from terminal 2 at a level compatible with the input requirements of a TV-sound-if-subsystem IC, such as the RCA CA3065. There is also a dc component of approximately 6.7 volts present at terminal 2. Coupling networks to subsequent circuits must contain a suitable dc-blocking capacitor.

Small chokes located in the sound and video outputs (terminals 2 and 19) should be self-resonating at the intermediate frequencies to prevent if leakage into subsequent stages.

The CA3068 if subsystem has an internal zener reference-diode that permits operation of the subsystem with an external voltage-regulator pass transistor. A suggested circuit arrangement is shown as part of the over-all if schematic diagram in Fig. 5 (b). The voltage-regulator pass-transistor has a nominal output voltage of 11.2 volts. Bypassing of the V+ supply with reference to the if subsystem is important, and the suggested arrangement shown in the application circuit (Fig. 10) should be used. Specifically, terminal 15 should be bypassed to terminal 17 on the CA3068. Even though terminal 17 is at dc ground potential, it should not be tied to ground but rather should be bypassed in the manner shown to avoid mutual impedance coupling within the CA3068.

MONOCHROME TV

The delayed-age circuits used in the CA3068 were originally intended to control a MOSFET in the rf-stage of the TV tuner. This arrangement permits direct application of the delayed-age voltage from the CA3068 to the tuner. In monochrome receivers, however, it is common practice to employ a bipolar transistor in the rf-stage of the tuner, and a circuit with a "forward"-age characteristic is required to control the rf-stage. This characteristic is easily established by means of an inverter network utilizing a p-n-p transistor, as shown in the circuit of Fig. 9.

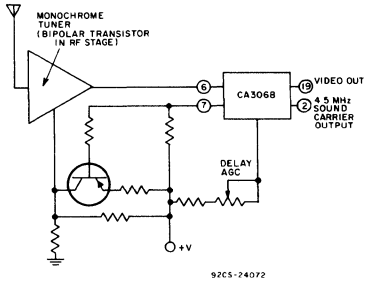


Fig. 9. Block diagram of an if system for a monochrome receiver showing peripheral age circuit.

As the input signal level increases, the forward-age delay voltage is developed at the tuner when the voltage at terminal 7 of the CA3068 decreases. The age voltage applied to the rf-stage of the tuner (Fig. 9) is derived from the collector of the p-n-p transistor. As the delay-age voltage is generated at terminal 7 of the CA3068, the base of the p-n-p inverter is driven into conduction, which causes more current to flow through the collector circuit, so that a positive (or forward) age potential is generated for the bipolar transistor in the tuner.

TV RECEIVER PIX–IF CIRCUIT APPLICATIONS

In this section, the application of the CA3068 integrated circuit in a color and a monochrome TV receiver is described. The circuits shown were constructed on single-sided copper PC boards.

As previously noted, because of the high gain encountered in PIX-IF design, positive feedback must be avoided if the amplifier is to remain free of spurious oscillation. To this end, the optimization of printed board layout and component placement is essential. The proper choice of bypassing components and signal-path layout is necessary to avoid feedback through ground loops.

IF CIRCUIT FOR COLOR TV RECEIVER

The schematic diagram of an if system for a color-TV receiver is shown in Fig. 10. A parts list and illustrations showing the PC-board component layout (top view) and the actual printed circuit (bottom view of board) are shown in Appendix A. Since most current color-TV receivers employ automatic-fine-tuning (AFT) systems, an AFT system using the CA3064 has also been included on the same board; Fig. 10 includes the AFT circuit.

The if-response is determined by the triple-tuned circuit, which consists of three traps: two preceding the IC and an interstage double-tuner circuit with one trap. In the tripled-tuned circuit, the two bridge-T traps are used to provide attenuation of the adjacent-channel picture carrier (frequency 39.75 MHz) and adjacent-channel sound carrier frequency (47.25 MHz). A

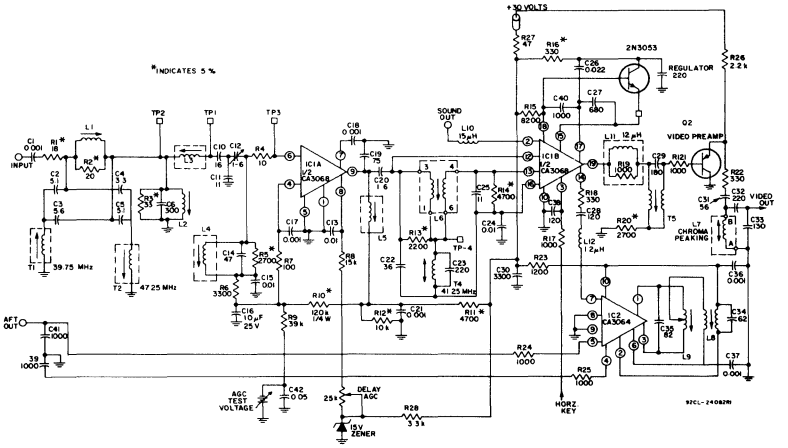


Fig. 10. Schematic diagram of a typical application of the CA3068 to a PIX-IF circuit for a color-TV system. A template of the printed circuit board used to construct this circuit, a diagram of the position of all components on the board, a block diagram of the location of major components on the board, and a circuit parts list are given in Appendix A.

common bridge impedance consisting of parallel-connected L1 and R2 is used. Adjustment of L1 for best null of the 47.25 MHz trap assures the desired 60-dB minimum attenuation.

The triple-tuned circuit provides, at center frequency, a source resistance to the IC of 800 ohms and a voltage gain of three from the input to pin 6 of the IC. The first section of the triple-tuned circuit consists of L2 and C6. Capacitor C6 is in parallel resonance with coil L2 at 44 MHz. The third section of the triple-tuned circuit consists of coil L4 and capacitor C14. Coupling and voltage-gain from L2 to L4 are provided by the second section, coil L3 and capacitors C10, C11, and C12. The inductive reactance of L3 is made 75 times larger than that of L2 to provide a high degree of tuned-circuit isolation for ease of alignment.

The circuit provides protection against interference resulting from a strong rf signal which might inadvertently be introduced between the tuner and the if stage. Parasitic resonance and couplings have been minimized to maintain a high degree of attenuation at frequencies remote from the if-resonance frequency.

The interstage double-tuned bandpass circuit, with a bifilar T-trap at 41.25 MHz, is similar to that commonly used in the third stage of color-TV receivers. The sound and picture carriers are present at the input (terminal 12) to the 4.5 MHz sound-if detector circuit. Trapping action removes the 41.25 MHz sound carrier at terminal 13 to prevent a difference-frequency beat of 0.92 MHz with the chroma subcarrier at 42.17 MHz. The picture carrier and chroma subcarrier entering terminal 13 are amplified, detected, and additionally amplified as detected video signal. If the sound carrier is not attenuated by the 41.25 MHz trap, the carrier will be detected as a large 4.5 MHz difference-signal in the video output. A 4.5 MHz trap (T5) is included to prevent interference of a residual 4.5 MHz intercarrier signal in the chroma and luminance circuits.

The chroma peaking circuit compensates for the slope of the video response, as shown in Figs. 11 (a), 11 (b) and 11 (c). The actual slope and shape of the video response between 3.08 MHz and 4.08 MHz will vary because of normal component tolerance. The chroma-peaking coil, L7, has two cores, one to adjust inductance to center the response at 3.58 MHz, and the other to adjust chroma output level and bandwidth. The latter core controls circuit Q with little effect on over-all inductance.

Photographs of the detected sweep-response characteristics are shown in Fig. 12. The sweep-response of Fig. 12 (f) shows the interstage alignment from TP3 (of Fig. 10) to terminal 9 of the CA3068. The sweep-response curves in Figs. 12 (a) through 12 (e) show 60 dB of age range from a level of 100 microvolts (Fig. 12 (e)) to 100 millivolts (Fig. 12 (a)).

The alignment procedure for the color-TV PIX-IF system using the CA3068, Fig. 10, is given in Appendix A.

IF CIRCUIT FOR MONOCHROME TV RECEIVER

The schematic diagram for a PIX-IF system for a monochrome TV system that employs the CA3068 is shown in Fig. 13. A PC-board component-layout diagram (top view), the actual printed circuit (bottom view of board), and a circuit parts list are shown in Appendix B. A sound-if system using the CA3065 has been included to show the simplicity with which it can be used in conjunction with the CA3068.

The selectivity is provided in two sections, an input single-tuned circuit with trap, and a double-tuned interstage circuit. The resistive pad, R1, R2, and R3 of Fig. 13, is used to terminate the link-cable and isolate cable effects from the high-Q input circuit. The bridge-T trap-circuit is used to give maximum attenuation to the adjacent-channel sound carrier. Precision components (R2, C1, C2) achieve a good null at 47.25 MHz

Although this Application Note describes subsystem designs in TV receivers, the CA3068 is also applicable in AM communications systems requiring performance at frequencies within the range of 10 to 70 MHz.

REFERENCES

1. RCA Data Bulletin File No. 396 concerning the CA3064 and CA3064E, "TV Automatic Fine Tuning Circuit", or the RCA DATABOOK, 1975 Series SSD-201C.
2. RCA Data Bulletin File No. 412 concerning the CA3065, "TV IF Sound System", or the RCA DATABOOK, 1975 Series SSD-201C.
3. RCA Data Bulletin File No. 467 concerning the CA3068, "Television Video IF System", or the RCA DATABOOK, 1975 Series SSD201C.

APPENDIX A – THE COLOR CIRCUIT

ALIGNMENT PROCEDURE FOR THE COLOR CIRCUIT

Preliminary Adjustments and Calibration

1. Adjust delay-agc (noise pot) fully cw.
2. Connect supplies as indicated on schematic diagram (Fig. 10), set bias to zero.
3. Set sweep generator to 10 millivolts as indicated on Boonton 91DA meter with 56-ohm termination.

Step 1 - IF Interstage Alignment

a. Ground TP1 with short clip lead.
b. Connect sweep generator with 56-ohm termination and 1000-picofarad decoupling capacitor to TP3.
c. Connect oscilloscope to video output.
d. Adjust bias for 5-volt peak-to-peak response on oscilloscope.
e. Adjust bottom core of T4 for minimum at 41.25 MHz.
f. Adjust L5 and L6 for symmetrical response with PIX and color markers equal (Fig. 12 (a)): L5 controls markers and L6 controls tilt.
g. Adjust top and bottom cores of T4 simultaneously, top core for maximum rejection of 41.25 MHz and bottom core to maintain minimum 41.25 MHz.

Step 2 - IF Overall Alignment

a. Leave ground clip lead on TP1.
b. Remove sweep input from TP3.
c. Connect TP2 through a 1000-picofarad capacitor to TP3.
d. Connect sweep generator to input.
e. Readjust variable bias to maintain 5-volts peak-to-peak response on oscilloscope.
f. Adjust T1 for minimum 39.75 MHz.
g. Adjust T2 for minimum 47.25 MHz.
h. Adjust L2 for equal height of PIX and color markers.
i. Remove ground-clip lead from TP1 and 1000-picofarad capacitor from between TP2 and TP3.
j. Maintain 5-volts peak-to-peak response on oscilloscope by re-adjusting bias.
k. Adjust L3 and L4 simultaneously for symmetrical response with PIX and color markers equal: L4 controls markers and L3 controls tilt.
l. Adjust bandpass trimmer, C12, to place PIX and color markers at 40 percent while readjusting L3 and L4 (Fig. 12 (b)).
m. Re-adjust T1 for minimum at 39.75 MHz if necessary.
n. Re-adjust T2 for minimum at 49.25 MHz. Then adjust L2 to maximize the rejection at 47.25 MHz.

AFT Alignment

a. With oscilloscope on AFT output, adjust bias for 10-volts peak-to-peak response.
b. Adjust L8 for maximum 45.75 MHz.
c. Adjust L9 for crossover at 45.75 MHz.
d. Re-adjust L8 and L9 to obtain symmetry.
e. Adjust L8 to obtain maximum width.

Color-Circuit Parts List

Capacitors		Resistors (All values in ohms)	
C1	0.001μF	R1	18
C2	5.1pF	R2	20
C3	5.6pF	R3	33
C4	3.3pF	R4	10
C5	5.1pF	R5	2.7k
C6	300pF	R6	3.3k
C10	16pF	R7	100
C11	11pF	R8	15k
C12	1-6pF	R9	39k
C13	0.01μF	R10	120k
C14	47pF	R11	4.7k
C15	0.01μF	R12	10k
C16	10μF	R13	2.2k
C17	0.001μF	R14	4.7k
C18	0.001μF	R15	8.2k
C19	7.5pF	R16	330
C20	1.6pF	R17	1k
C21	0.001μF	R18	330
C22	3.6pF	R19	1k
C23	220pF	R20	2.7k
C24	0.01μF	R21	1k
C25	11pF	R22	330
C26	0.022μF	R23	1.2k
C27	680pF	R24	1k
C28	120pF	R25	1k
C29	180pF	R26	2.2k
C30	0.022μF	R27	47
C31	56pF	R28	3.3k
C32	220pF	R29	25k
C33	130pF		
C34	62pF		
C35	82pF		
C36	0.001μF		
C40	1000pF		
C41	1000pF		
C42	1000pF		

Inductors	RCA Stock No.
L1	132159
L2	132161
L3	132839
L4	132658
L5	137126
L6	132146
T1	132839
T2	132157
T4	132150
T5	132135

APPENDIX B – THE MONOCHROME CIRCUIT

ALIGNMENT PROCEDURE FOR THE MONOCHROME-CIRCUIT

Step 1 -

1. Connect +20 volts to appropriate points on board.
2. Connect sweep generator to input
3. Connect dc bias voltage to appropriate point on board.
4. Adjust sweep generator for 10-millivolt input.
5. Adjust bias voltage for 5-volt, peak-to-peak output.

Step 2 -

1. Adjust LT for minimum response at 47.25 MHz.
2. Adjust L2 for maximum at 44.5 MHz.
3. Adjust L6, L7 for bandpass shown in Fig. 14 (b). The curve should have 3-MHz bandwidth centered at 44.5 MHz.

Monochrome-Circuit Parts List

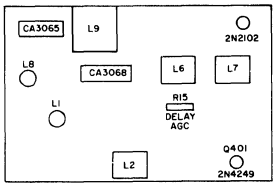
Capacitors	
C1	3.0pF
C2	3.0pF
C3	6.8pF
C4	3.9pF
C5	0.001μF
C6	12μF
C7	0.001μF
C8	0.001μF
C9	6.8pF
C10	0.01μF
C11	20pF
C12	15pF
C13	0.001μF
C14	18pF
C15	0.01μF
C16	0.001μF
C17	0.001μF
C18	5μF
C19	4700pF
C20	68pF
C21	12pF
C22	4pF
C23	82pF
C24	0.047μF
C25	0.047μF
C26	0.01μF
C27	0.047μF

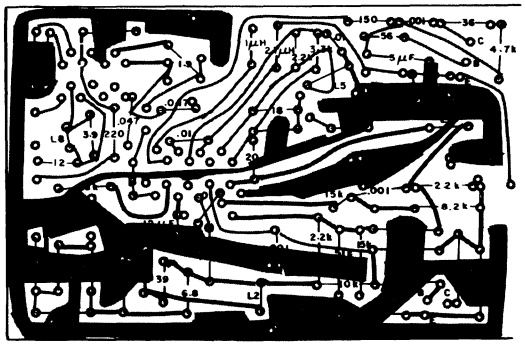
Inductors	RCA Stock No.
L1	131655
L2	133463
L3	1.0μH
L4	12.0μH
L5	134754*
L6	131465
L7	133546
L8	130120
L9	130121

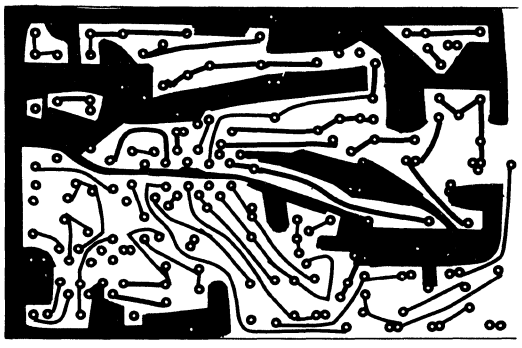
*(9 turns No. 23 wire; use 1/2 W resistor to form coil)

Resistors (All values in ohms)	
R1	18
R2	27
R3	91
R4	15k
R5	3.3k
R6	10k
R7	1.0k
R8	33k
R9	51k
R10	270
R11	2.2k
R12	120k
R13	2.2k
R14	15k
R15	25k
R16	8.2k
R17	2.2k
R18	3.3k
R19	150
R20	56
R21	36
R22	220
R23	5.6k

THE MONOCHROME CIRCUIT







figuration is used to minimize capacitive feed-through coupling via the base-collector junction of the p-n-p transistor.

Another multiplex system using the OTA's clocked by a COS/MOS flip-flop is shown in Fig. 6. The high output voltage capability of the COS/MOS flip-flop permits the circuit to be driven directly without the need for p-n-p level-shifting transistors.

A simple RC phase-compensation network is used on the output of the OTA in the circuits shown in Figs. 5 & 6. The values of the RC-network are chosen so that $\frac{1}{2\pi RC} \cong 2\text{MHz}$.

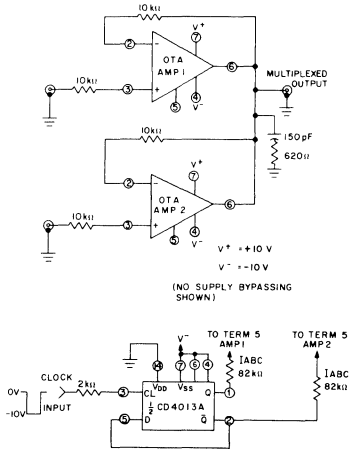
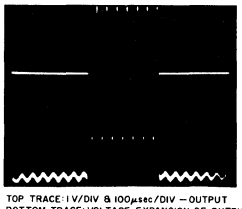


Fig. 6– Schematic diagram of a two-channel linear multiplex system using a COS/MOS flip-flop to gate two OTAs.

This RC-network is connected to the point shown because the lowest-frequency pole for the system is usually found at this point. Fig. 7 shows an oscilloscope photograph of the multiplex circuit functioning with two input signals. Fig. 8

TOP TRACE: MULTIPLEXED OUTPUT 1V/DIV & 100μsec/DIV
BOTTOM TRACE: TIME EXPANSION OF SWITCHING BETWEEN INPUTS 2V/DIV & 5μsec/DIV

Fig. 7– Voltage waveforms for circuit of Fig. 6; top trace: multiplexed output; lower trace: time expansion of switching between inputs.



TOP TRACE: 1V/DIV & 100μsec/DIV – OUTPUT
BOTTOM TRACE: VOLTAGE EXPANSION OF OUTPUT 1mV/DIV & 100μsec/DIV ISOLATION IS IN EXCESS OF 80 db

Fig. 8– Voltage waveforms for circuit of Fig. 6; top trace: output; lower trace: voltage expansion of output; isolation in excess of 80 dB.

shows an oscilloscope photograph of the output of the multiplexer with a 6-V p-p, sine wave signal (22 kHz) applied to one amplifier and the input to the other amplifier grounded. This photograph demonstrates an isolation of at least 80 dB between channels.

Sample-and-Hold Circuits

An extension of the multiplex system application is a sample-and-hold circuit (Fig. 9), using the strobing characteristics of the OTA amplifier bias-current (ABC) terminal as a means of control. Fig. 9 shows the basic system using the CA3080A as an OTA in a simple voltage-follower configuration with the phase-compensation capacitor serving the additional function of sampled-signal storage. The major consideration for the use of this method to "hold" charge is that neither the charging amplifier nor the signal readout device significantly alter the charge stored on the capacitor. The CA3080A is a particularly suitable capacitor-charging amplifier because its output resistance is more than 1000 MΩ under cut-off conditions, and the loading on the storage capacitor during the hold-mode is minimized. An effective solution to the read-out requirement involves the use of an RCA 3N138 insulated-gate field-effect transistor (MOS/FET) in the feedback loop. This transistor has a maximum gate-leakage current of 10 picoamperes; its loading on the charge "holding" capacitor is negligible. The open-loop voltage-gain of the system (Fig. 9) is approximately 100 dB if the MOS/FET is used in the source-follower mode to the CA3080A as the input amplifier. The open-loop output impedance $(\frac{1}{g_m})$ of the 3N138 is approximately 220 Ω because its transconductance is about 4,600 μmho at an operating current of 5 mA. When the CA3080A drives the 3N138 (Fig. 9), the closed loop operational-amplifier output impedance characteristic

$$Z_{out} \cong \frac{Z_O \text{ (open-loop)}}{A \text{ (open-loop voltage-gain)}}$$

$$\cong \frac{220\ \Omega}{100\text{dB}} \cong \frac{220\ \Omega}{10^5} \cong 0.0022\ \Omega$$

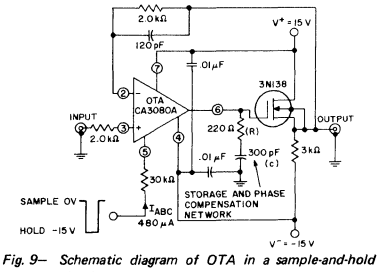
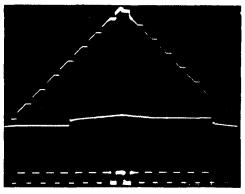


Fig. 9– Schematic diagram of OTA in a sample-and-hold circuit.

Fig. 10 shows a "sampled" triangular signal. The lower trace in the photograph is the sampling signal. When this signal goes negative, the CA3080A is cutoff and the signal is "held" on the storage capacitor, as shown by the plateaus on the triangular wave-form. The center trace is a time expansion of the top-most transition (in the upper trace) with a time scale of 2 μsec/div.



TOP TRACE: SAMPLED SIGNAL 1V/DIV & 20μsec/DIV
CENTER TRACE: TOP PORTION OF UPPER SIGNAL 1V/DIV & 2μsec/DIV
BOTTOM TRACE: SAMPLING SIGNAL 20V/DIV & 20μsec/DIV

Fig. 10– Waveforms for circuit of Fig. 9; top trace: sampled signal; center trace: top portion of upper signal; lower trace: sampling signal.

Once the signal is acquired, variation in the stored-signal level during the hold-period is of concern. This variation is primarily a function of the cutoff leakage current of the CA3080A (a maximum limit of 5 ηA), the leakage of the storage element, and other extraneous paths. These leakage currents may be either "positive" or "negative" and, consequently, the stored-signal may rise or fall during the "hold" interval. The term "tilt" is used to describe this condition. Fig. 11 shows the expected pulse "tilt" in microvolts as a function of time for various values of the compensation/storage capacitor. The horizontal axis shows three scales representing leakage currents of 50 ηA, 5 ηA, 500 pA.

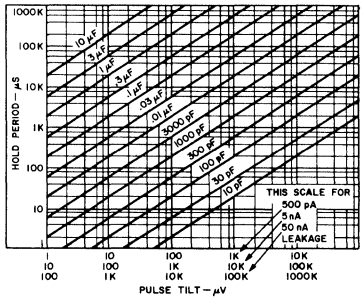
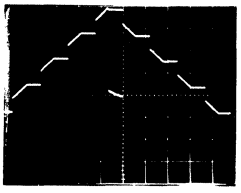


Fig. 11– Chart showing "tilt" in sample-and-hold potentials as a function of hold time with load capacitance as a parameter.

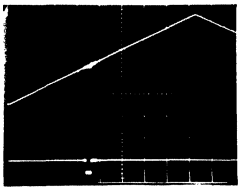
Fig. 12 shows a dual-trace photograph of a triangular signal being "sampled-and-held" for approximately 14 ms with a 300 pF storage capacitor. The center trace (expanded to 20 mV/div) shows the worst-case "tilt" for all the steps shown in the upper trace. The total equivalent leakage current in this case is only 170 pA $(I = C\frac{dv}{dt})$.



TOP TRACE: SAMPLED SIGNAL 1V/DIV & 20msec/DIV
CENTER TRACE WORSE CASE TILT 20mV/DIV & 20msec/DIV

Fig. 12– Oscilloscope photo of "triangular-voltage" being sampled by circuit of Fig. 9.

Fig. 13 is an oscilloscope photograph of a ramp voltage being sampled by the "sample-and-hold" circuit of Fig. 9. The input signal and sampled-output signal are superimposed. The lower trace shows the sampling signal. Data shown in Fig. 13 were recorded with supply voltages of ±10 V and the series input resistor at terminal 5 was 22 kΩ.



TOP TRACE: INPUT AND OUTPUT SUPERIMPOSED 1V/DIV & 2μsec/DIV
BOTTOM TRACE: SAMPLING SIGNAL 20V/DIV & 2μsec/DIV

Fig. 13– Oscilloscope photo of "ramp-voltage" being sampled by circuit of Fig. 9.

the circuit of Fig. 20 as an emitter-follower to drive the p-n-p transistor, variations due to base-emitter characteristics are considerably reduced due to the complementary nature of the n-p-n base-emitter junctions. Moreover, the temperature coefficients of the two base-emitter junctions tend to cancel one another. Fig. 21 shows a configuration using one transistor in the RCA type CA3018A n-p-n transistor-array as

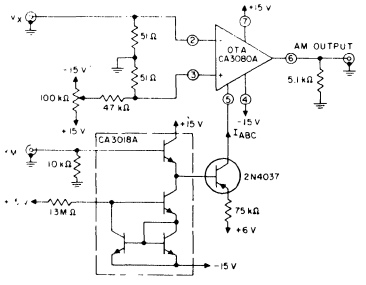


Fig. 21– Amplitude modulator using OTA controlled by p-n-p and n-p-n transistors.

an input emitter-follower, with the three remaining transistors of the transistor-array connected as a current-source for the emitter – followers. The 100-kΩ potentiometer shown in these schematics is used to null the effects of amplifier input offset voltage. This potentiometer is adjusted to set the output voltage symmetrically about zero. Figs. 22a and 22b show oscilloscope photographs of the output voltages obtained when the circuit of Fig. 19 is used as a modulator for both sinusoidal and triangular modulating signals. This method of modulation permits a range exceeding 1000:1 in the gain, and thus provides modulation of the carrier input in excess of 99%. The photo in Fig. 22c shows the excellent isolation achieved in this modulator during the "gated-off" condition.

Four-Quadrant Multipliers

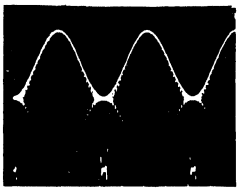
A single CA3080A is especially suited for many low-frequency, low-power four-quadrant multiplier applications. The basic multiplier circuit of Fig. 23 is particularly useful for waveform generation, doubly balanced modulation, and other signal processing applications, in portable equipment, where low-power consumption is essential and accuracy requirements are moderate. The multiplier configuration is basically an extension of the previously discussed gain-controlled configuration (Fig. 19).

To obtain a four-quadrant multiplier, the first term of the modulation equation (which represents the fixed carrier) must be reduced to zero. This term is reduced to zero by the placement of a feedback resistor (R) between the output and the inverting input terminal of the CA3080A, with the value of the feedback resistor (R) equal to $1/g_m$. The output current is $I_O = g_m(-Vx)$ because the input is applied to the inverting terminal of the OTA. The output current due to the resistor (R) is $\frac{Vx}{R}$. Hence, the two signals cancel when $R = 1/g_m$. The current for this configuration is:

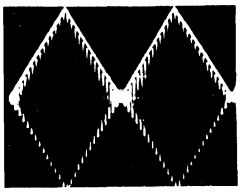
$$I_O = \frac{-19.2\ Vx\ Vm}{Rm} \text{ and } Vm = Vy$$

The output signal for these configurations is a "current" which is best terminated by a short-circuit. This condition can be satisfied by making the load resistance for the multiplier output very small. Alternatively, the output can be applied to a current-to-voltage converter shown in Fig. 24.

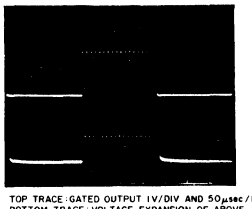
In Fig. 23, the current "cancellation" in the resistor R is a direct function of the OTA differential amplifier linearity. In the following example, the signal excursion is limited to ±10 mV to preserve this linearity. Greater signal-excursions on the input terminal will result in a significant departure from linear operation (which may be entirely satisfactory in many applications).



TOP TRACE: MODULATION FREQUENCY INPUT ≃20 VOLTS P-P & 50 μsec/DIV
CENTER TRACE AMPLITUDE MODULATE OUTPUT 500mV/DIV & 50 μsec/DIV
BOTTOM TRACE: EXPANDED OUTPUT TO SHOW DEPTH OF MODULATION 20mV/DIV & 50 μsec/DIV



TOP TRACE: MODULATION FREQUENCY INPUT 20 VOLTS & 50 μsec/DIV
BOTTOM TRACE: AMPLITUDE MODULATED OUTPUT 500mV/DIV & 50 μsec/DIV



TOP TRACE: GATED OUTPUT 1V/DIV AND 50 μsec/DIV
BOTTOM TRACE: VOLTAGE EXPANSION OF ABOVE SIGNAL – SHOWING NO RESIDUAL 1mV/DIV AND 50 μsec/DIV – AT LEAST 80 db OF ISOLATION fq = 100 kHz

Fig. 22– a) Oscilloscope photo of amplitude modulator circuit of Fig. 19 with $R_m = 40\ k\Omega$, $V^+ = 10$ v and $V^- = -10$ V. Top trace: modulation frequency input ≃ 20-V p-p; center trace: amplitude modulated output 500-mV/div.; lower trace: expanded output to show depth of modulation, 20 mV/div.; b) triangular modulation; top trace: modulation frequency input ≃ 20 V; lower trace: amplitude modulated output 500 mV/div.; c) square wave modulation, top trace: gated output 1 V/div.; lower trace: expanded scale, showing no residual (1 mV/div) and at least 80 dB of isolation at fq = 100 kHz.

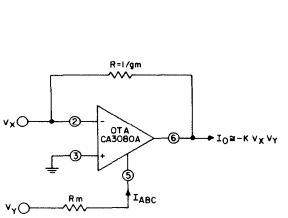


Fig. 23– Basic four quadrant analog multiplier using an OTA.

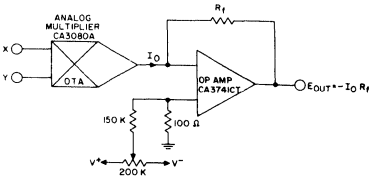


Fig. 24– OTA analog multiplier driving an op-amp that operates as a current-to-voltage converter.

Fig. 25 shows a schematic diagram of the basic multiplier with the adjustments set-up to give the multiplier an accuracy of approximately ±7 percent "full-scale". There are only three adjustments: 1) one is on the output, to

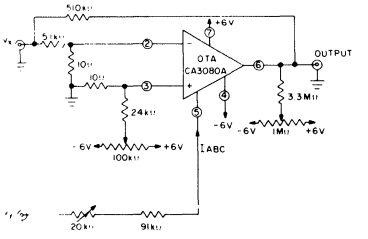


Fig. 25– Schematic diagram of analog multiplier using OTA.

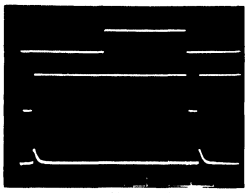
compensate for slight variations in the current-transfer ratio of the current-mirrors (which would otherwise result in a symmetrical output about some current level other than zero); 2) the adjustment of the 20-kΩ potentiometer establishes the g_m of the system equal to the value of the fixed resistor shunting the system when the Y-input is zero; 3) compensates for error due to input offset voltage.

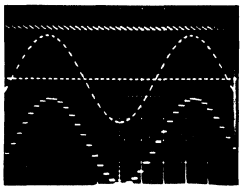
Procedure for adjustment of the circuit:

1. a) Set the 1 MΩ output-current balancing potentiometer to the center of its range
   b) Ground the X- and Y- inputs
   c) Adjust the 100 kΩ potentiometer until a zero-V reading is obtained at the output.
2. a) Ground the Y-input and apply a signal to the X-input through a low source-impedance generator. (It is essential that a low impedance source be used; this minimizes any change in the g_m balance or zero-point due to the 50-μA Y-input bias current).
   b) Adjust the 20-kΩ potentiometer in series with Y-input until a reading of zero-V is obtained at the output. This adjustment establishes the g_m of the CA3080A at the proper level to cancel the output signal. The output current is diverted through the 510-kΩ resistor.
3. a) Ground the X-input and apply a signal to the Y-input through a low source-impedance generator.
   b) Adjust the 1-MΩ resistor for an output voltage of zero-V.

There will be some interaction among the adjustments and the procedure should be repeated to optimize the circuit performance.

Fig. 26 shows the schematic of an analog multiplier circuit with a 2N4037 p-n-p transistor replacing the Y-input "current" resistor. The advantage of this system is the higher input resistance resulting from the current-gain of the p-n-p transistor. The addition of another emitter-follower preceding the p-n-p transistor (shown in Fig. 21) will further increase the current gain while markedly reducing the effect of the V_{be} temperature-dependent characteristic and the offset voltage of the two base-emitter junctions.





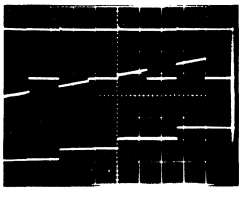


Fig. 30– (a) Waveforms showing timing of flip-flop, delay–"one-shot" and the strobing pulse to the sample-and-hold circuit (Fig. 28): top trace: flip-flop output (5 V/div); center trace: "one-shot" output (5 V/div); lower trace: pulse at collector of 2N4037 transistor (0.1 V/div); b) Waveforms showing the decoding operation from the decoder keying pulse (top traces) to the recovered "decoded" sampled output (lower traces). 1) top trace: collector of 2N4037; center trace: multiplexed output with one channel input grounded; lower trace: decoded output; 2) Expanded scale of (1).

a constant-current transistor. Phase compensation is applied at the interface of the CA3080 and the 3N138 MOS/FET shown in Fig. 9.

Another variation of this generic form of amplifier utilizes the RCA CD4007A (COS/MOS) "inverter" as an amplifier driven by the CA3080. Each of the three "inverter"/amplifiers in the CD4007A has a typical voltage gain of 30 dB. The gain of a single COS/MOS "inverter"/amplifier coupled with the 100 dB gain of the CA3080 yields a total forward-gain of about 130 dB. Use of a two-stage COS/MOS amplifier configuration will increase the total open-loop gain of the system to about 160 dB (100,000,000). Figs. 31 through 34 show examples of these configurations. Each COS/MOS "inverter"/amplifier can sink or source a current of 6 mA (typ.). In Figs. 33 and 34, two COS/MOS "inverter"/amplifiers have been connected in parallel to provide additional output current.

The open-loop slew-rate of the circuit in Fig. 31 is approximately 65 V/μsec. When compensated for the unity-gain voltage-follower mode, the slew-rate is about 1 V/μsec (shown in Fig. 32). Even when the three "inverter"/

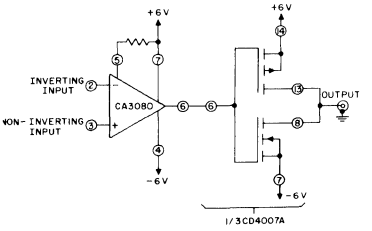


Fig. 31– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (open-loop mode). For greater current output the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown. Open-loop gain ≃ 130 dB.

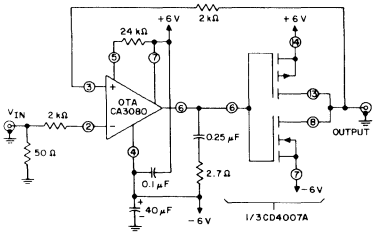


Fig. 32– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (unity-gain closed-loop mode). For greater current output, the two remaining amplifiers of the CD4007A may be connected in parallel with the single stage shown.

amplifiers in the CD4007A are connected as shown in Fig. 33, the open-loop slew-rate remains at 65 V/μsec. A slew-rate of about 1 V/μsec is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 34. Fig. 35 contains oscilloscope photos of input-output waveforms under small-signal and large-signal conditions for the circuits of Figs. 32 and 34. These photos illustrate the inherent stability of the OTA and COS/MOS circuits operating in concert.

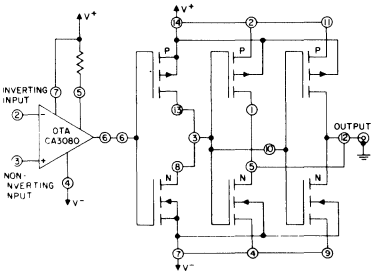


Fig. 33– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (open-loop mode). gain ≃ 160 dB.

Precision Multistable Circuits

The micropower capabilities of the CA3080, when combined with the characteristics of the CD4007A COS/MOS "inverter"/amplifiers, are ideally suited for use in connection with precision multistable circuits. In the circuits of Figs. 31, 32, 33, and 34, for example, power-supply current drawn by the COS/MOS "inverter"/amplifier approaches zero as the output voltage swings either positive or negative, while the CA3080 current-drain remains constant.

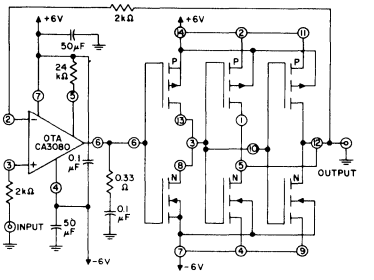


Fig. 34– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (unity gain closed-loop mode).

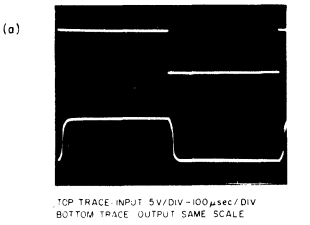


Fig. 35– a) Waveforms for circuit of Fig. 32 with large signal input; b) Waveforms for circuit of Fig. 32 with small signal input; c) Waveforms for circuit of Fig. 34 with large signal input; d) Waveforms for circuit of Fig. 34 with small signal input.

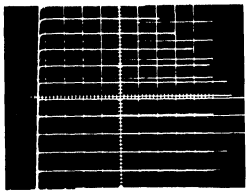


Fig. F— Photo showing results of Fig. E.

Fig. G shows the current-division within the "mirror" assuming a "unit" (1) of current in transistors (Q2 and Q3.

The resulting current-transfer ratio $I_2/I_1 = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$; Fig. C shows this equation plotted as a function of beta. It is significant that the current transfer ratio (I_2/I_1) is improved by the β^2 term, and reduces the significance of the $2\beta + 2$ term in the denominator.

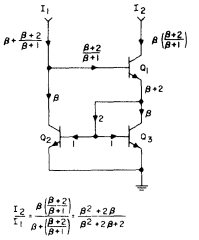


Fig. G— Current flow analysis of Fig. E.

Conclusions

The Operational Transconductance Amplifier (OTA) is a unique device with characteristics particularly suited to applications in multiplexing, amplitude modulation, analog multiplications, gain control, switching circuitry, multivibrators, comparators, and a broad spectrum of micropower circuitry. The CA3080 is ideal for use in conjunction with COS/MOS (Complementary-Symmetry MOS) IC's being operated in the linear mode.

Acknowledgements

The author is indebted to C. F. Wheatly for many helpful discussions. Valued contributions in circuit evaluation were made by A. J. Visioli Jr. and J. H. Klinger.

References

1 RCA's Linear Integrated Circuits Manual, Basic Circuits Section.
2 RCA published data for CA3060 File No. 404

provides enough gain to bring the input signal level to an amplitude suitable for fm detection, but not so high as to cause PC layout or coupling problems, Fig. 2.

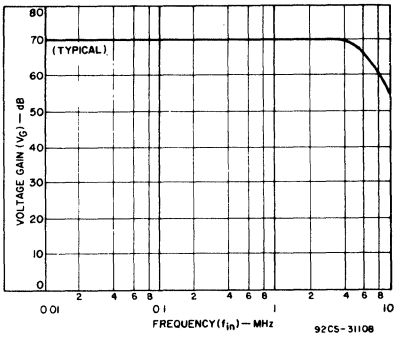


Fig. 2 - Voltage gain of if amplifier as a function of frequency.

As shown in Fig. 4, the if amplifier consists of four stages of differential amplifiers, Q15-Q16, Q19-Q20, Q23-Q24, and Q27-Q28, using resistors R13, R16, R19, and R24 as constant-current sinks; each stage is followed by emitter followers, Q17, Q21, and Q25. Because the differential amplifier functions as a limiter, am signals are eliminated and the signal into Q30 consists of constant-amplitude, frequency-modulated square waves. These square waves are shaped into approximate sine waves by Q30 and its associated RC networks to assure proper operation of the fm detector. The signal output from R31 into the base of Q41 and to terminal 10 is a constant-amplitude fm sine wave.

FM Detector

The fm sine wave at terminal 10 constitutes the input signal to the differential peak detector stage. The extracted signal contains the audio information. The detector section is formed by the differential amplifier configuration comprising transistors Q31, Q32, Q35, Q36, Q40, and Q41. Transistors Q31 and Q41 are emitter followers that operate at approximately 0.3 mA and provide high impedance at each input of the detector (terminals 10 and 11). Transistors Q32 and Q40, which operate at approximately 10 microamperes, along with the 15-picofarad capacitors C3 and C4 and the external frequency-sensitive network on terminals 10 and 11, perform peak or envelope detection. As shown in Fig. 1, this frequency-sensitive network consists of a parallel LC network in series with a 6.8-pF capacitor. The signal voltage (from Q30) is applied across the entire network connected to terminal 10. The portion of the signal from Q30 that is across the external 6.8-pF capacitor is applied to terminal 11, and the resulting difference in these signals provides the basic S curve used in the recovery of the audio signal from the fm signal.

An advantage of the differential peak detector is that it requires the alignment of only one single-tuned coil. This coil (L in Fig. 1) can be aligned by any one of the following methods (with an input terminated in 50 ohms, f_O = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, and a voltage at terminal 15 (V_{15}) ≃ 100 mV rms):

1. Tune L for maximum recovered audio. To minimize thermal effects on alignment, the volume control should be adjusted so that the maximum recovered audio level at the load is limited to a low power level (approximately 0.1 watt or less).
2. Tune L for maximum recovered audio and fine tune for minimum distortion.
3. With no rf input signal, note the dc voltage at terminal 9. Then apply a 4.5-MHz cw signal and adjust the detector coil L until the dc voltage at terminal 9 is the same as the value noted.

After aligning the differential peak detector coil, align the input transformer by reducing the fm input signal level until the recovered audio level drops approximately 3 dB. Then tune the input transformer for a maximum recovered audio level while the input level of the if amplifier-limiter is below its limiting point. Fig. 3 shows the recovered audio, am rejection, and signal-to-noise ratio for the CA3134 as a function of rf input level.

Volume Control and Electronic Attenuator

Control of the audio signal detected by the differential peak detector is accomplished by differential amplifiers Q33-Q34 and Q38-Q39.

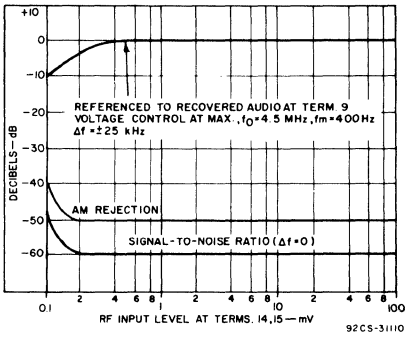


Fig. 3 - Recovered audio and signal-to-noise ratio as functions of rf input level.

The volume is controlled when the bias levels of the differential amplifiers are changed by a current flowing through an external fixed resistor between terminals 12 and 16. The amount of current flowing through this external resistor (which determines the level of recovered audio) is controlled by the position of the variable resistance (volume control) relative to ground. The voltage reference at terminal 16 is established by internal zener diode Z2, approximately 6 volts. The maximum level of recovered audio, therefore, occurs when no currents other than the base currents for Q34 and Q39 are being drawn from the zener diode through the external resistor. When the volume control is adjusted for the minimum level of recovered audio, the current drawn from terminal 16 should be limited to less than 1 milliampere.

This method of controlling the recovered audio has a very predictable volume-control taper, which can be modified to suit the designer's preference by changing the external component values. In addition, it allows for either a one- or two-wire volume control. The one-wire volume control (Fig. 4, alternate volume-control circuit) requires only one wire from the printed circuit board to the external volume control, but requires that the value of the variable resistor be large (approximately 500 kilohms) and that the resistor have an audio taper to assure an acceptable change of audio output level with a linear change (rotation) of the volume-control. The two-wire volume control allows the use of a volume control having a lower value of resistance and a linear taper.

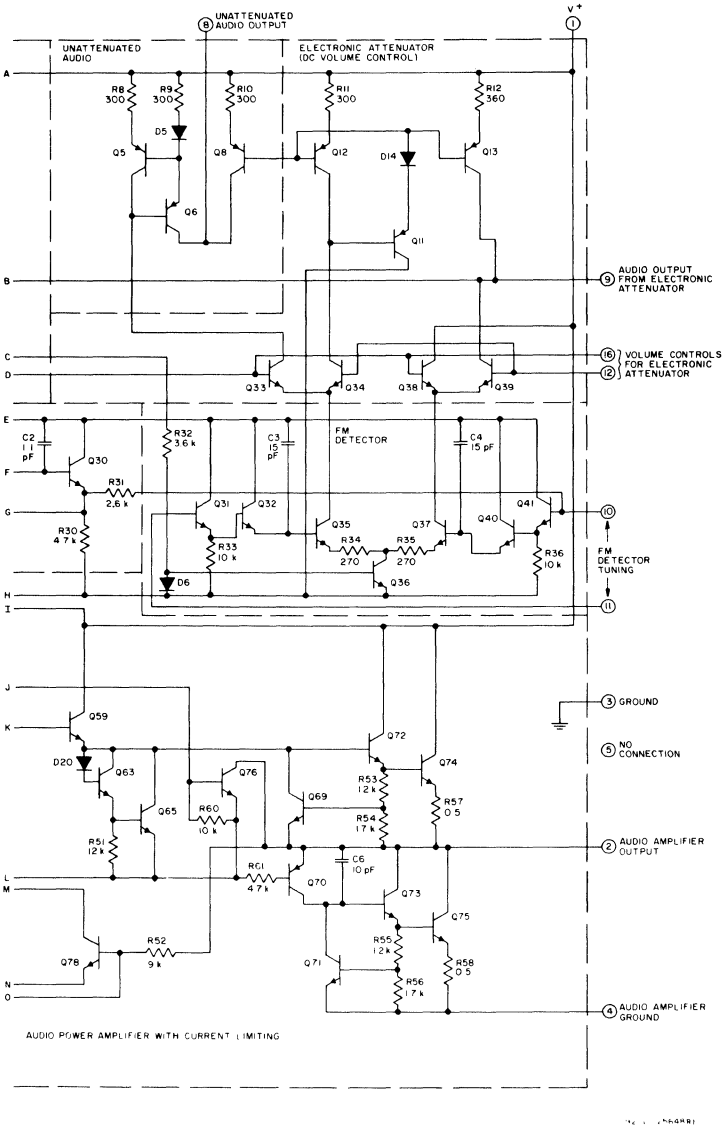


Fig. 4 – Schematic diagram of CA3134.

nents, especially costly electrolytic capacitors. The input impedance (at terminal 7) is typically 100 kilohms (R59). Fig. 5 shows the frequency response of the audio power amplifier and Fig. 6 its efficiency. Both current limiting and thermal shutdown protection are provided. Current limiting is accomplished by limiting the drive to the output transistors from the driver transistors Q72 and Q73. The limiting drive is determined by the feedback from R53, R54, and Q69 to Q72, and R55, R56, and Q71 to Q73. When the peak output current exceeds approximately 0.8 ampere, the voltage developed across the emitters of Q72 and Q73 will cause Q69 and Q71, respectively, to conduct, thereby limiting the drive to the output transistors Q74, Q75.

When the chip temperature exceeds 150 °C, the thermal-sensing portion of the CA3134 begins to shut down the power amplifier by removing the bias from the power amplifier driver stages. The temperature at which the thermal shutdown circuitry is activated is determined by the relative areas of D9, Q66, and D18 and those of Q49, D11, D12, and D13. When Q49 conducts, transistors Q79, Q68, and Q76 are in turn biased into

Acknowledgment

The author is indebted to both Jack Craft for many helpful discussions and Wayne Austin for his suggestions in the preparation of this Note. The contributions of H. Chinery in the electrical characterization of the CA3134 and Ralph Thompson in the mechanical characterization of the stud package are acknowledged.

References

1. RCA Solid State Data Sheet for CA3134 types, "TV Sound IF and Audio Output Systems," File No. 1097.

2. Method of attaching heat sinks similar to the type provided with the CA3134GM or GQM to the CA3134G. First apply a non-conductive epoxy (Uniset structural adhesive or equivalent) to the top side of the plastic package. Then apply a conductive epoxy (Dupont 5504A or equivalent) in the hole of the heat sink and around the stud projecting from the plastic package. To assure good thermal conduction, use sufficient conductive epoxy to allow the excess to be forced through the hole when the heat sink is fitted over the stud. Stress applied to the stud should be limited to less than 3 in-lbs (approximately 0.35 newton-meter), 15 lbs (approximately 65 newtons) of tension, and 100 lbs (approximately 445 newtons) of compression.

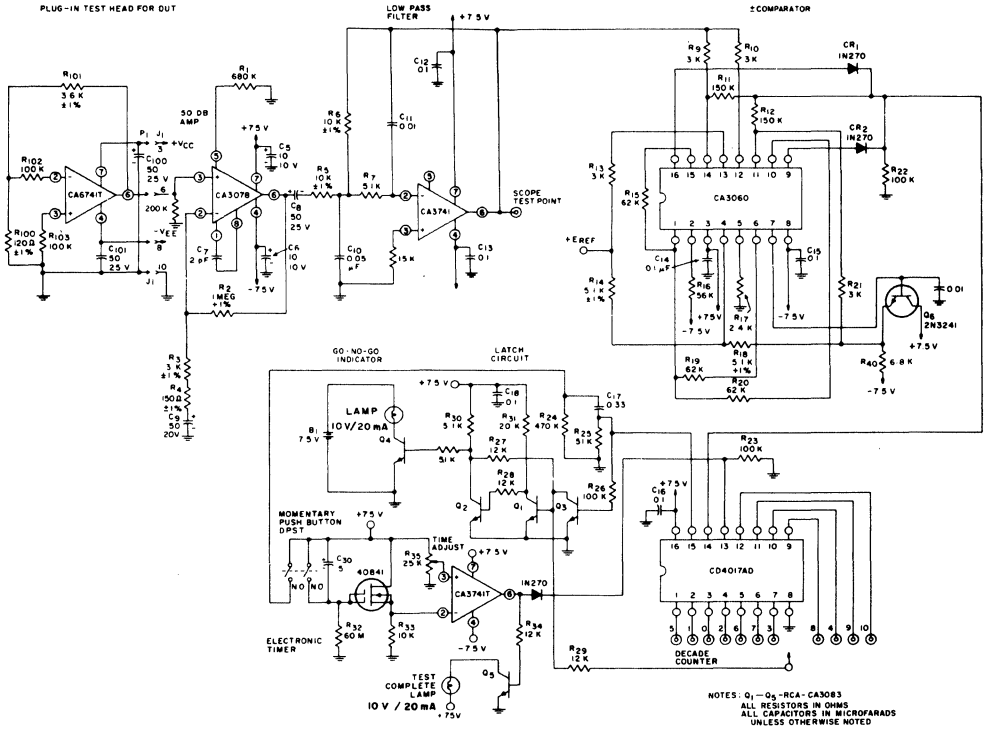


Fig. 2b— Complete schematic diagram for burst noise test-set.

currents consistent with the gain-bandwidth requirements of the particular application.

In the test for burst noise, the source resistance (Rs) seen by the input terminals of the DUT, is a key test parameter. Burst noise causes effects which are equivalent to a spurious current-source at the device input and, therefore, burst-noise current generates an equivalent input noise-voltage in proportion to the magnitude of the source resistance through which it flows. Accordingly, to increase the sensitivity of the test system, it is desirable to use the highest source resistance consistent with the input offset-current of the DUT. For example, an Op-Amp which has 0.1 μA input offset current could realistically be tested with source-resistance in the order of 100KΩ (10 mV input offset), whereas a 1 MΩ source-resistance (100 mV input offset) could cause excessive offset in the output. For 741 type Op-Amps a 100kΩ resistance is recommended.

Burst-noise generation in amplifiers is usually more pronounced at lower temperatures (particularly below 0°C). Consequently, consideration must be given to the temperature of the DUT in relation to the temperature range under which the device is expected to perform in a particular operation.

A test parameter of importance is the time duration of observation. Because the frequency of burst-noise occurrence is frequently less than once every few seconds, the minimum test period should be in the range of from 15 to 30 seconds.

Pass-Fail Criteria

A test system built to accommodate the test philosophy outlined above has the ability to reject or pass a DUT on the basis of two variables: burst-amplitude and the frequency of burst occurrence. The burst-amplitude which will trip the counter can be no lower than the background l/f noise peaks of burst-free units, otherwise normal background noise will fail the DUT.

The background noise peaks depend on the source termination Rs, the wide band l/f noise figure of the DUT, and the test system bandwidth. A good estimate of the normal background noise-peak levels can be computed from the definition of noise factor and an empirically determined noise-crest factor of approximately 6:1. The crest-factor is the ratio of the maximum peak-noise voltage to the RMS noise voltage. The noise factor is defined as the ratio of the total noise power at the amplifier output to the output-noise power due to the source resistors alone. In terms of the RMS noise voltages at the input terminals of the amplifier this is equivalent to:

$$\text{Noise Factor (F)} = \frac{E^2\text{input noise total}}{E^2\text{noise source resist}} = \frac{(E_{NTi})^2}{(E_{NRS})^2} \quad (1)$$

E_{NTi} is the total input noise-voltage, i.e., the sum of noise generated in the source termination resistance and noise generated by the DUT.

E_{NRs} is that part of E_{NTi} due to Rs alone.

$$\text{Therefore,} \quad E_{NTi} = (\sqrt{F})\,(E_{NRs}). \quad (2)$$

E_{NRs} can be computed by using the well known expression for "white-noise" generated across the terminals of a resistor (R):

$$E_{NR}(\text{RMS}) = \sqrt{4kTBR} \quad (3)$$

where k = Boltzmans Constant = 1.372×10^{-23} j/°K

T = Absolute Temperature in °K
B = Noise Bandwidth in Hz
R = Value of the resistor in ohms.

Thus, at a room temperature of 290°K

$$E_{NR}(\text{RMS}) = 1.28 \times 10^{-10}\sqrt{BR}$$

For example, a 100 kΩ resistor preceding a system with a bandwidth of 1 kHz will generate a noise-voltage of

$$(1.28 \times 10^{-10}) \quad (\sqrt{10^3 \cdot 10^5}) \quad = 1.28\ \mu V_{RMS}$$

Both inputs of an Op-Amp are usually terminated in Rs, hence it is necessary to combine the effects of both resistors to determine the effective E_{NRs} at the input of the DUT. Because the noise voltages from these two resistors are uncorrelated their voltages must be added vectorally rather than algebraically.

$$E_{NRs}\,(\text{effective}) = \sqrt{(E_{NRs1})^2 + (E_{NRs2})^2} \quad (4)$$

because $E_{NRs1} = E_{NRs2}$, when $R_{s1} = R_{s2}$

$$E_{NRs}\,(\text{effective} = (\sqrt{2})\ (E_{NRs})$$

and for 1 kHz bandwidth at 290°K

$$E_{NRs}\,(\text{effective}) = (\sqrt{2})\,(1.28\ \mu V) = 1.81\ \mu V_{RMS}.$$

If in this example, the DUT has a wideband l/f noise figure of 4 dB (2.5:1 power ratio) the total RMS background noise-voltage at the input will be

$$E_{NTi} = (\sqrt{F})\ (E_{NRs})\ \text{(from eq.(2))}$$
$$= (\sqrt{2.5})\ (1.81) = 2.9\ \mu V_{RMS}$$

operated, "On-Off" switching of nearby equipment introduces detectable transients into the system. These problems are eliminated by placing the test circuitry in a completely shielded enclosure with a hinged top for easy access to the test unit. The external noise problem is best solved by use of a shielded enclosure and by use of a battery-operated power-supply contained within the enclosure. Fig. 6 shows a photo of the circuit board layouts of the test unit.

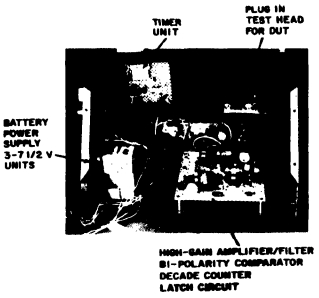


Fig. 6— Photo of circuit-board layout.

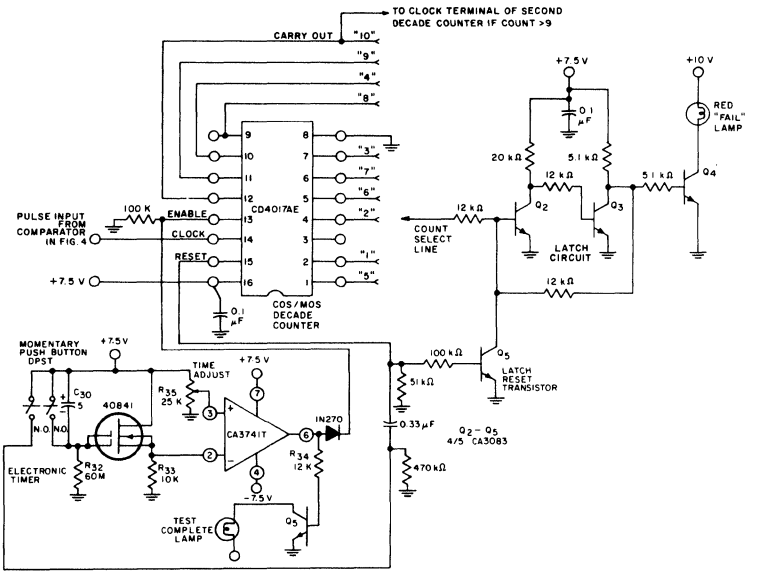


Fig. 5— Counter-latch-timer-control circuit schematic.

voltages: a 50-dB amplifier; a 10-dB, 42-MHz amplifier; a twin-T bandpass amplifier; a 20-dB, 10-MHz bandpass amplifier; and a voltage-follower.

ICAN-5269 . . . . . 7 pages
Integrated Circuits for FM Broadcast Receivers
This Note describes several approaches to FM receiver design using silicon monolithic integrated circuits. The tuner section is described first, and then the if-amplifier and detector sections. Performance characteristics are described where applicable. The FM receivers discussed are designed for use from a +9-volt supply. The key to design simplicity is the use of the RCA multifunction integrated circuits CA3005, CA3012, and CA3014. The CA3005 may be used as a cascode rf amplifier, a differential rf amplifier, a mixer-oscillator, and an if amplifier; the CA3012 and CA3014 perform if amplification, limiting, detection, and preamplification.

ICAN-5296 . . . . . 5 pages
Application of the RCA-CA3018 Integrated-Circuit Transistor Array
The CA3018 integrated circuit consists of four silicon epitaxial transistors produced by a monolithic process on a single chip mounted in a 12-lead TO-5 package. The four active devices, two isolated transistors plus two transistors with an emitter-base common connection, are especially suitable for applications in which closely matched device characteristics are required, or in which a number of active devices must be interconnected with non-integrable components such as tuned circuits, large-value resistors, variable resistors, and microfarad bypass capacitors. Such areas of application include if, rf (through 100 MHz), video, agc, audio, and dc amplifiers.

ICAN-5299 . . . . . 6 pages
Application of the RCA-CA3019 Integrated-Circuit Diode Array
The CA3019 integrated circuit diode array provides four diodes internally connected in a diode-quad arrangement plus two individual diodes. Its applications include gating, mixing, modulating, and detecting circuits. Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations. Consequently, the CA3019 is particularly useful in circuit configurations that require either a balanced diode bridge or identical diodes.

ICAN-5337 . . . . . 10 pages
Application of the RCA-CA3028A and CA-3028B Integrated-Circuit RD Amplifiers in the HF and VHF Ranges
The CA3028A and CA3028B monolithic-silicon integrated circuits are single-stage differential amplifiers intended for service in communications systems operating at frequencies up to 100 MHz with single power supplies. This Note provides technical data and recommended circuits for use of the CA3028A and CA3028B in rf amplifiers, autodyne converters, if amplifiers, and limiters. The CA3028A and CA3028B are suitable for use in a wide range of applications in dc, audio, and pulse amplifier service; they have been used as sense amplifiers, preamplifiers for low-level transducers, and dc differential amplifiers.

ICAN-5338 . . . . . 14 pages
Application of the RCA-CA3021, CA3022, and CA3023 Integrated-Circuit, Wideband Amplifiers
The CA3021, CA3022, and CA3023 integrated circuits are multipurpose high-gain amplifiers designed for use in video and AM or FM if stages in single-power-supply systems. Specifically, they can be used in video amplifiers operating at frequencies through 30 MHz, AM and FM if amplifiers, and buffer amplifiers in which an isolation capability greater than 60 dB at 1 MHz is desired.

ICAN-5380 . . . . . 7 pages
Integrated - Circuit Frequency - Modulation if Amplifiers
The discussion in this Note shows that the simplest approach to the use of the CA3012 and CA3028 integrated circuits in FM if-amplifier strips is to replace each stage in present discrete-transistor if strips with a differential amplifier. This integrated-circuit approach requires a minimum of re-engineering because a cascade of individually tuned if stages is used. From a performance point of view, this approach results in better AM rejection than that obtained with discrete circuits because of the inherent limiting achieved with the differential-amplifier configuration.

ICAN-5766 . . . . . 8 pages
Application of the RCA-CA3020 and CA3020A Integrated-Circuit Multipurpose Wideband Power Amplifiers
The CA3020 and CA3020A integrated circuits are multipurpose, multifunction power amplifiers designed for use as power-output amplifiers and driver stages in portable and fixed communications equipment and in ac servo-control systems. The flexibility of these circuits and the high-frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video amplifiers, and video line drivers. Voltage gains of 60 dB or more are available with a 3-dB bandwidth of 8 MHz. Applications covered include audio, wideband, and driver amplifiers.

ICAN-5831 . . . . . 5 pages
Application of the RCA-CA3044 and CA3044VI Integrated Circuits in Automatic-Fine-Tuning Systems
This Note describes the use of the CA3044 and CA3044VI integrated circuits as automatic fine-tuning (AFT) system components and discusses the advantages of integrated circuits in this application. The CA3044VI is electrically identical to the CA3044, but is supplied with formed leads for easier printed-circuit-board mounting. The construction and performance of a typical automatic-fine-tuning system for a color television system are examined.

ICAN-5841 . . . . . 4 pages
Feedback-Type Volume-Control Circuits for RCA-CA3041 and CA3042 Integrated Circuits
This Note describes feedback-type volume controls for use with RCA-CA3041 and CA3042 integrated circuits in television receivers. In television sets using these integrated circuits, the volume control is often located remote from the amplifier. The long leads required in such a configuration sometimes pick up undesirable signals that, in turn, cause the system to exhibit hum and noise at low volume levels. The proposed feedback-type volume control reduces hum and noise pick-up by reducing the gain of the system rather than the signal level, and thus eliminates the cost of shielding the leads.

ICAN-6259 . . . . . 10 pages
Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Demodulator
The CA3090AQ integrated-circuit provides features heretofore unavailable to the receiver designer. This device needs only a single tuning adjustment, which reduces to a minimum the manual effort during assembly; the phase-locked loop maintains performance under conditions of temperature variations, humidity, and aging. The compactness of the CA3090AQ and of the required external components, added to the other attributes, makes this stereo decoder a significant advancement in the state of the art of stereo decoder designs.

ICAN-6302 . . . . . 9 pages
Description and Application of the RCA-CA3120E Integrated-Circuit TV-Signal Processor
The CA3120E is a 16-pin, dual-in-line-monolithic-silicon integrated circuit that processes a video signal and provides the following outputs: non-inverted video output; noise-processed, inverted video output; dual-polarity, composite synchronization signals; and automatic gain-control signals (agc). The IC, which can be used in color or monochrome TV receivers, requires a single-polarity power supply (positive) and includes impulse noise inversion and delay circuits that reduce the deleterious effects of impulse noise in the receiver agc and synchronization (sync) circuits. Standard agc strobing techniques are also used. The agc and impulse-noise thresholds are automatically set and require no controls. The if maximum-gain bias and the tuner agc delay may be adjusted for optimun. TV-receiver performance; the time constant for the sync-separator input can also be optimized by the set designer.

ICAN-6724 . . . . . 8 pages
A Flexible Integrated-Circuit Color Demodulator for Color Television
This Note describes the circuit operation and application of the CA3067 in a color television receiver. The CA3067, which is supplied in a quad-in-line 16-lead plastic package, provides the following color-demodulator circuit functions: amplification, balanced chroma demodulation, dc-operated tint (phase) control, and zener-diode voltage regulation.

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