STANDARD MICROSYSTEMS CORPORATION

DATA CATALOG 1981

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PART NUMBER INDEX

FUNCTIONAL INDEX

Data Communication Products

Part Number	Name	Description	Max Baud Rate	Power Supplies	Package	Page
COM 1553A	MIL-STD-1553A UART	MIL-STD-1553 (Manchester) Interface Controller	1 MB	+5	40 DIP	19-34
COM 1671	ASTRO	Asynchronous/Synchronous Transmitter/Receiver, Full Duplex,5-8 data bit, 1X or 32X clock	1 MB	+5, −5, +12	40 DIP	35-50
COM 1863	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	40 KB	+5	40 DIP	51-58
COM 2017	UART	Universal Asynchronous Receiver Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit	25 KB	+5, −12	40 DIP	59-66
COM 2017H	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit	40 KB	+5, −12	40 DIP	59-66
COM 2502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 2 stop bit	25 KB	+5, −12	40 DIP	59-66
COM 2502H	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 2 stop bit	40 KB	+5, −12	40 DIP	59-66
COM 2601	USRT	Universal Synchronous Receiver/ Transmitter, STR, BSC, Bi-sync compatible	250 KB	+5, −12	40 DIP	67-74
COM 2651[1]	USART/PCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bits; 1, 1½, 2 stop bit, 1X, 16X, 64X clock	1 MB	+5	28 DIP	75-76
COM 5025	Multi-Protocol USYNRT	SDLC, HDLC, ADCCP, Bi-sync, DDCMP compatible, automatic bit stuffing/ stripping, frame detection/generation, CRC generation/checking, sync detection	1.5 MB	+5, +12	40 DIP	77-88
COM 8004	32 Bit CRC Generator/ Checker	Companion device to COM 5025 for 32 bit CRC	2.0 MB	+5	20 DIP	89-94
COM 8017	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit	40 KB	+5	40 DIP	95-102
COM 8018	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	40 KB	+5	40 DIP	51-58
COM 8251A	USART	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	64 KB (sync) 9.6 KB (async)	+5	28 DIP	103-118
COM 8502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 2 stop bit	40 KB	+5	40 DIP	95-102

[1] For future release

Printer

CHARACTER GENERATOR

Part Number	Description	Scan	Max Access Time	Power Supplies	Package	Page
CG 4103[3]	5x7x64	Column	1.2 μsec	+5, −12 or ±12	28 DIP	163-166

SHIFT REGISTER

Part Number	Description	Feature	Max Clock Freq.	Power Supply	Package	Page
SR 5015-XX	Quad Static Shift Register Mask Programmable Length	Load, Recirculate, Shift Controls,	1 MHz	+5	16 DIP	167-170
SR 5015-80	Quad 80 Bit Static					
SR 5015-81	Quad 81 Bit Static					
SR 5015-133	Quad 133 Bit Static					
SR 5017	Quad 81 Bit	Shift Left/Shift Right, Recirculate Controls, Asynchronous clear	1 MHz	+5	16 DIP	171-174
SR 5018	Quad 133 Bit					

Microprocessor Peripheral

ROM

Part Number	Description	Access Time	Power Supply	Package	Page
ROM 2316E[1][3]	16K ROM; 16,384 bits organized 2048x8	450 nsec	+5	24 DIP	221-222
ROM 4732[3]	32K ROM; 32,768 bits organized 4096x8	450 nsec	+5	24 DIP	223-226
ROM 36000[1][3]	64K ROM; 65,536 bits organized 8192x8	250 nsec	+5	24 DIP	227-230

FLOPPY DISK

Part Number	Description	Sector Format	Density	IBM Compatible	Write Pre-compensation	Power Supplies	Package	Page
FDC 1791[1]	Floppy Disk Controller/Formatter	Soft	Double	Yes	External	+5, +12	40 DIP	241-242
FDC 1792[1]		Soft	Single	Yes	External	+5, +12	40 DIP	241-242
FDC 1793[1]		Soft	Double	Yes	External	+5, +12	40 DIP	241-242
FDC 1794[1]		Soft	Single	Yes	External	+5, +12	40 DIP	241-242
FDC 3400	Floppy Disk Data Handler provides serial/parallel interface, sync detection	Hard	N.A.	N.A.	No	+5, −12	40 DIP	231-238
FDC 7003[1]	Floppy Disk Controller/Formatter	Soft	Single/ Double	Yes	Internal	+5	40 DIP	239-240

CASSETTE/CARTRIDGE

Part Number	Description	Max Data Rate	Features	Power Supply	Package	Page
CCC 3500	Cassette/Cartridge Data Handler	250K bps	Sync byte detection, Read While Write	+5, −12	40 DIP	243-250

[1]For future release
[3]May be custom mask programmed

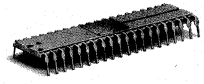
Baud Rate Generator

All Baud Rate Generators are programmable dividers capable of providing 16 output frequencies* for UARTs or USARTs from either an on-chip crystal oscillator or an external frequency input. "T" versions utilize an external frequency input only. Dual Baud Rate Generators provide two output frequencies simultaneously for full duplex communication.

Baud Rate Generators providing all standard baud rates from various popular crystal frequencies are available. In addition the baud rate generator may be custom mask programmed for other divisors.

*except as noted

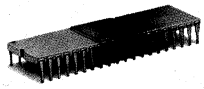
Part Number	Description	Features	Power Supplies	Package	Page
COM 5016	Dual Baud Rate Generator	On-chip oscillator or external frequency input	+5, +12	18 DIP	177-178
COM 5016T	Dual Baud Rate Generator	External frequency input	+5, +12	18 DIP	177-178
COM 5026	Single Baud Rate Generator	On-chip oscillator or external frequency input	+5, +12	14 DIP	179-180
COM 5026T	Single Baud Rate Generator	External frequency input	+5, +12	14 DIP	179-180
COM 5036	Dual Baud Rate Generator	COM 5016 with additional output of input frequency ÷ 4	+5, +12	18 DIP	181-182
COM 5036T	Dual Baud Rate Generator	COM 5016T with additional output of input frequency ÷ 4	+5, +12	18 DIP	181-182
COM 5046	Single Baud Rate Generator	COM 5026 with additional output of input frequency ÷ 4	+5, +12	14 DIP	183-188
COM 5046T	Single Baud Rate Generator	COM 5026T with additional output of input frequency ÷ 4	+5, +12	14 DIP	183-188
COM 8046	Single Baud Rate Generator	32 baud rates; 1X, 16X, 32X clock outputs; single +5 volt supply	+5	16 DIP	189-190
COM 8046T	Single Baud Rate Generator	COM 8046 with external frequency input only	+5	16 DIP	189-190
COM 8116	Dual Baud Rate Generator	Single +5 volt version of COM 5016	+5	18 DIP	191-192
COM 8116T	Dual Baud Rate Generator	Single +5 volt version of COM 5016T	+5	18 DIP	191-192
COM 8126	Single Baud Rate Generator	Single +5 volt version of COM 5026	+5	14 DIP	193-194
COM 8126T	Single Baud Rate Generator	Single +5 volt version of COM 5026T	+5	14 DIP	193-194
COM 8136	Dual Baud Rate Generator	Single +5 volt version of COM 5036	+5	18 DIP	195-196
COM 8136T	Dual Baud Rate Generator	Single +5 volt version of COM 5036T	+5	18 DIP	195-196
COM 8146	Single Baud Rate Generator	Single +5 volt version of COM 5046	+5	14 DIP	197-198
COM 8146T	Single Baud Rate Generator	Single +5 volt version of COM 5046T	+5	14 DIP	197-198



Keyboard Encoder

Part Number	No. of Keys	Modes	Features	Standard Fonts Suffix	Standard Fonts Description	Power Supplies	Package	Page
KR-2376 XX[3]	88	3	2 Key Rollover	-ST	ASCII	+5, −12	40 DIP	207-210
KR-3600 XX[3]	90	4	2 Key or N Key Rollover	-ST -STD -PRO	ASCII ASCII Binary Sequential	+5, −12	40 DIP	211-218

[3]May be custom mask programmed



CRT Display

VTAC® TIMING CONTROLLERS

Part Number	Description	Features	Display Format	Max Clock	Power Supplies	Package	Page
CRT 5027	provides all of the timing and control for interlaced and non-interlaced CRT display		programmable	4 MHz	+5, +12	40 DIP	121-128
CRT 5037		balanced beam interlace	programmable	4 MHz	+5, +12	40 DIP	121-128
CRT 5047		fixed format	80 column 24 row	4 MHz	+5, +12	40 DIP	129-130
CRT 5057		line-lock	programmable	4 MHz	+5, +12	40 DIP	121-128
CRT 9007[1]	CRT video processor and controller	sequential or row-table driven memory	programmable	4 MHz	+5	40 DIP	131-134
CRT 96364A/B	complete CRT processor	on-chip cursor and write control	64 column 16 row	1.6 MHz	+5	28 DIP	137-144

VDAC™ DISPLAY CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supply	Package	Page
CRT 8002A[2,3]	Provides complete display and attributes control for alphanumeric and graphics display. Consists of 7x11x128 character generator, video shift register, latches, graphics and attributes circuits.	7x11 dot matrix, wide graphics, thin graphics. on-chip cursor	reverse video blank blink underline strike-thru	20 MHz	+5	28 DIP	145-154
CRT 8002B[2,3]				15 MHz			
CRT 8002C[2,3]				10 MHz			

CHARACTER GENERATORS

Part Number	Description	Max Frequency	Power Supply	Package	Page
CRT 7004A[3,4]	7x11x128 character generator, latches, video shift register	20 MHz	+5	24 DIP	155-159
CRT 7004B[3,4]		15 MHz			
CRT 7004C[3,4]		10 MHz			

ROW BUFFER

Part Number	Description	Max Row Length	Power Supply	Package	Page
CRT 9006-83[1]	8 bit wide serial cascadable row buffer memory for CRT or printer	83 characters	+5	24 DIP	135-136
CRT 9006-135		135 characters			

[1] For future release
[2] Also available as CRT 8002A,B,C-001 Katakana
CRT 8002A,B,C-003 5X7 dot matrix
[3] May be custom mask programmed
[4] Also available as CRT 7004A,B,C-003 5X7 dot matrix

SMC CROSS REFERENCE GUIDE

Description	SMC Part #	AMD	AMI	E.A.	Fairchild	G.I.	Harris	Intel	Inte
UART (1½ SB)**	COM 2017	—	S1883	—	—	AY 5-1013A	—	—	–
UART (1, 2 SB)**	COM 2502	—	—	—	—	AY 5-1013	—	—	–
UART (N-Channel)**	COM 8017	—	S6850*	—	—	AY 3-1015	HM6402	—	IM6
UART (N-Channel)**	COM 8502	—	—	—	—	AY 3-1015	HM6403*	8251*	IM6
UART (N-Channel)*	COM 1863	—	S1602	—	—	—	—	—	–
USRT	COM 2601	—	S2350*	—	—	—	—	—	–
ASTRO	COM 1671	—	—	—	—	—	—	—	–
PCI	COM 2651	—	—	—	—	—	—	—	–
USART	COM 8251A	8251A	—	—	—	—	—	8251A	–
Multi-Protocol, USYNRT	COM 5025	—	—	—	F3846* F6856*	—	—	—	–
Dual Baud Rate Gen.	COM 5016/36 COM 8116/36	—	—	—	—	—	—	—	–
Single Baud Rate Gen.	COM 5026/46 COM 8126/46	—	—	—	F4702*	—	HD4702* HD6405*	—	–
88 Key KB Encoder	KR 2376	—	—	—	—	AY 5-2376	—	—	–
90 Key KB Encoder	KR 3600	—	—	EA2007* 2030* 2007*	—	AY 5-3600	—	—	–
Character Generator	CRT 7004	—	S8564*	—	—	—	—	—	–
Character Generator	CRT 8002	—	—	—	—	—	—	—	–
Character Generator	CG 4100	—	S8499	—	—	RO 5-2240S*	—	—	–
Shift Register	SR 5015	—	S2182/3/5	—	—	—	—	—	–
Shift Register	SR 5017	—	—	—	—	—	—	—	–
CRT Controller	CRT 5037	—	—	—	—	—	—	8275*	–
ROM	ROM 4732	AM 9232	S68332	8332	—	RO 3-9332	—	2332*	–
ROM	ROM 36000	—	S4264*	—	—	RO 3-9364	—	—	–

*Functional Equivalent

**Most UART's are interchangeable; consult the factory for detailed information on interchangeability.

MOS hnology	Mostek	Motorola	National	NEC	Signetics	Solid State Scientific	Synertec	T.I.	W.D.
—	—	—	MM5303*	μPD369*	—	—	—	TMS6011	TR1602
—	—	—	—	—	2536	—	—	—	TR1402
—	—	MC6850*	—	—	—	SCR1854	—	—	—
—	—	—	—	—	—	—	—	—	TR1983*
—	—	—	—	—	—	—	—	—	TR1863
—	—	—	—	—	—	—	—	—	—
—	—	—	INS1671	—	—	—	—	—	UC1671
—	—	—	—	—	2651	—	—	—	—
—	—	—	INS8251	μPD8251A	—	—	—	—	—
—	—	—	—	μPD379*	2652	SND5025	—	—	SD1933*
—	—	—	—	—	—	—	—	—	BR1941L
—	—	MC14411*	MM5307*	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—
S1009*	—	—	MM5740*	μPD364*	—	—	—	TMS5001	—
—	—	MCM66700* MC6570*	DM8678*	—	2609*	—	—	—	—
—	—	—	—	—	—	—	—	—	—
31004* 32027*	MK2002	MC1132*	M5240*	—	—	—	—	TMS4103	—
—	MK1007*	—	5054*	—	2532*	—	—	TMS3113* TMS3114*	—
—	—	—	—	—	—	—	—	—	—
—	MK3807	MC6845*	DP8350*	—	—	SND5027 SND5037	6545*	TMS9927	—
332	—	MCM8332	—	μPD2332	2632	—	SY2332	TMS4732	—
364*	MK36000	MCM68A364*	MM52864*	μPD2364*	2664*	—	SY2364*	TMS4764*	—

Innovation in microelectronic technology is the key to growth at Standard Microsystems.

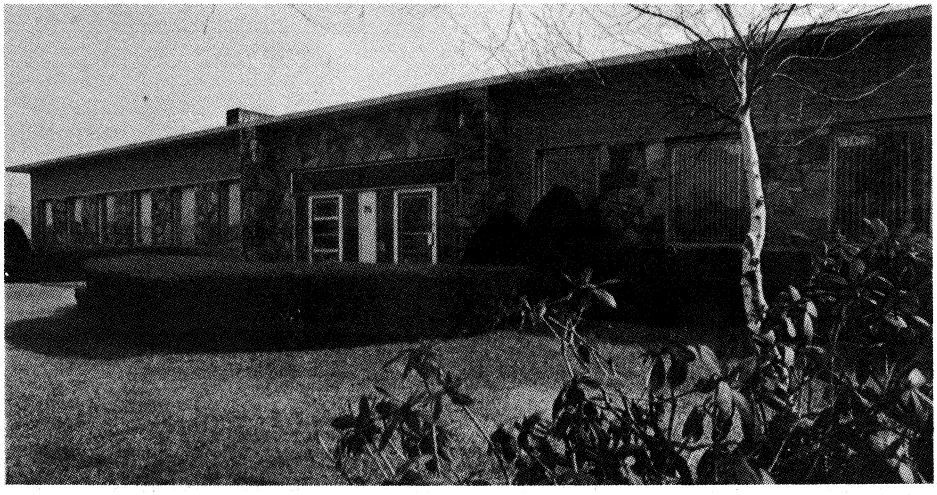
Since its inception, Standard Microsystems has been a leader in creating new technology for metal oxide semiconductor large scale integrated (MOS/LSI) circuits.

For example, while the first MOS/LSI processes were P-channel, it was recognized very early that an N-channel process would greatly improve switching speeds and circuit density. However, the fundamental problem of parasitic currents needed to be solved. The research and development staff at Standard Microsystems recognized this problem and directed its energy toward the development of its now-famous COPLAMOS® technology. COPLAMOS® defines a self-aligned, field-doped, locally oxidized structure which produces high-speed, high-density N-channel IC's.

In addition, on-chip generation of substrate bias, also pioneered by Standard Microsystems, when added to the COPLAMOS® technology, results in the ability to design dense, high-speed, low-power N-channel MOS integrated circuits through the use of one external power supply voltage.

Again recognizing a need and utilizing its staff of qualified process experts, Standard Microsystems developed the CLASP® process. The need was for fast turnaround, easily programmable semi-custom LSI technology. The development was CLASP,® a process that utilizes ion implantation to define either an active or passive device which allows for the presence of a logical 1 or 0 in the matrix of a memory or logic array. This step is accomplished after all wafer manufacturing steps are performed including metalization and final passiviation layer formation. Thus, the wafer can be tested and stored until customer needs dictate the application, a huge saving in turnaround time and inventory costs.

These innovations in both process and circuit technology have received widespread industry recognition. In fact, many of the world's most prominent semiconductor companies have been granted patent and patent/technology licenses covering various aspects of these technologies. The companies include Texas Instruments, IBM, General Motors, ITT and Western Electric.



Our engineering staff follows the principle that "necessity is the mother of invention."

This philosophy led Standard Microsystems Corporation to COPLAMOS,® CLASP® and other innovative developments. It also brings companies to us to solve tough problems that other suppliers can't.

But it's a philosophy that involves more than just developing the next generation of MOS/LSI devices.

Such exploration, for example, helped Standard Microsystems recognize the need for communication controllers to handle the latest data communication protocols. As a result, Standard Microsystems was the first to introduce a one-chip LSI controller for HDLC protocols — the COM 5025.

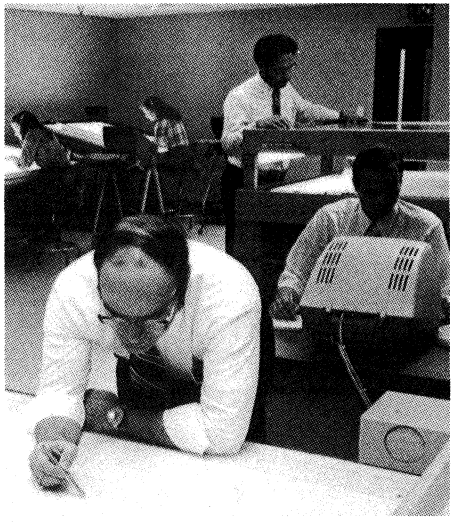
The COM 5025 is so versatile it can actually provide the receiver/transmitter functions for all the standard bit and byte oriented synchronous protocols, including SDLC, HDLC, ADCCP, bi-sync and DDCMP.

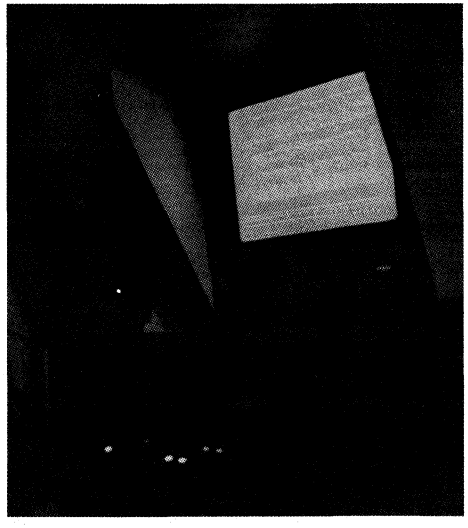
In another area, CRT display systems have traditionally required a great deal of support circuitry for the complex timing, refresh and control functions.

This need led the engineers at Standard Microsystems to develop the CRT 5027 Video Timer and Controller (VTAC®) that provides all these functions on a single chip. This left the display, graphics and attributes control spread over another 20 or 30 SSI, MSI and LSI devices. Standard Microsystems combined all these functions in the CRT 8002 Video Display Attributes Controller VDAC™). The COPLAMOS® process was used to achieve a 20 MHz video shift register, and CLASP® was used for fast turnaround of character font changes through its last stage programmability.

So from 60 to 80 integrated circuits, Standard Microsystems reduced display and timing to 2 devices, drastically reducing the cost and size of today's CRT terminal.

Achievements like these help keep Standard Microsystems custom and standard products in the forefront of technology with increased speeds and densities, and a lower cost per function.





Improvements in processing and manufacturing keep pace with advances in semiconductors.

With the phenomenal growth of the electronics industry, innovation is, of course, highly desirable. But if the products are to perform as designed, they also have to be reliable.

That's why at Standard Microsystems we take every means to insure the utmost quality and dependability. Consequently, "state-of-the-art" applies not only to our products, but to the way we manufacture them.

In wafer fabrication, the latest equipment and techniques are employed. In addition to conventional processing equipment, we use ion implantation technology extensively. We also use plasma reactors for much of our etching and stripping operations to maintain tight tolerances on process parameters.

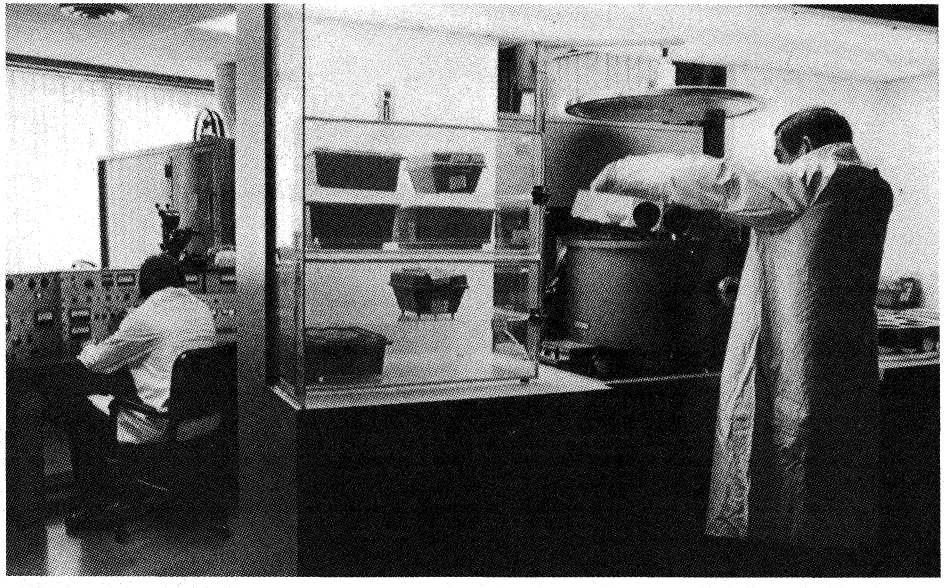
To make plastic packaging immune to moisture, we use a process that deposits a protective (passivating) layer of silicon nitride on the device surface.

Standard Microsystems processes include high and low voltage P-channel metal gate, N-channel silicon gate (COPLAMOS®), high-speed N-channel silicon gate with depletion mode devices, and CLASP.® In general, these processes have been engineered so that they are also compatible with most industry standard processes.

One obvious advantage our total capability gives customers, is that they can bring us their project at any stage in the development process. For instance, they may already have gone through system definition. Or they may have gone all the way to prototype masks, and only want production runs.

It makes no difference to Standard Microsystems. We can enter the process at any level.

Our full service capability lets us make full use of the technologies we develop. We can produce any quantity of semiconductors customers may require. And we can offer them one of the fastest turnaround times in the industry.



SMC microcircuits are built under the industry's most carefully controlled conditions.

Standard Microsystems uses the latest equipment and techniques for assembly — just as it does for processing. Automatic wire-bonding which we introduced recently to expand Standard Microsystems' capacity is a typical example.

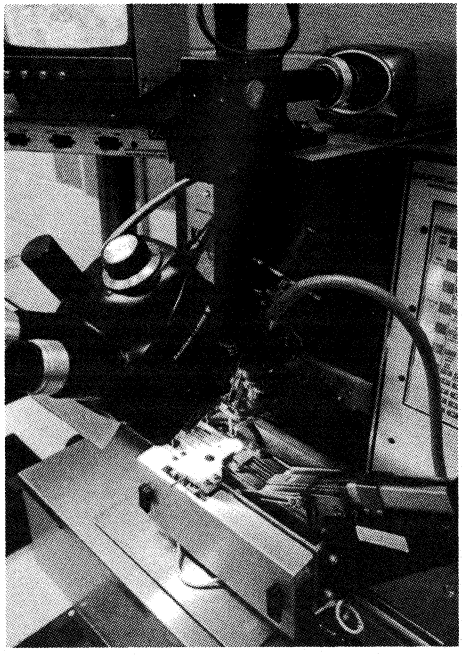
However, nothing is left to chance. To make sure every IC performs the way it should, each product is subjected to 37 quality control checks during assembly. Every run that comes out of wafer fabrication is analyzed to insure that all of its DC electrical characteristics are within specifications. Standard Microsystems' computerized analysis techniques, in fact, are second to none in the industry.

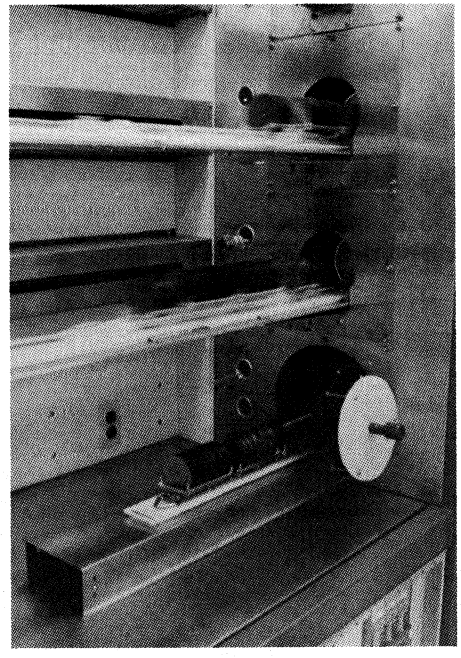
Tightly-controlled QC measures include die and pre-seal inspection and wire-pull, among others. Assembled parts are further subjected to vigorous mechanical tests including centrifuge, temperature cycling, and hermeticity testing.

Naturally, to perform all these tests properly requires adequate personnel. That's why 35% of all Standard Microsystems production technicians are assigned to the Quality Control Department.

Many tests are computer-controlled. In addition, we use dedicated equipment designed to simulate the customers' systems requirements.

Thanks to the dedication of Standard Microsystems' highly-motivated technical staff and well-trained production personnel, Standard Microsystems has one of the highest product yields in the industry.





SMC can supply standard microcircuits or custom-design them to your requirements.

The product mix at Standard Microsystems is approximately half custom products and half standard products.

This makes Standard Microsystems the ideal company to talk with if you're undecided which direction to take.

As a matter of fact, a combination of custom and standard may actually be best for you.

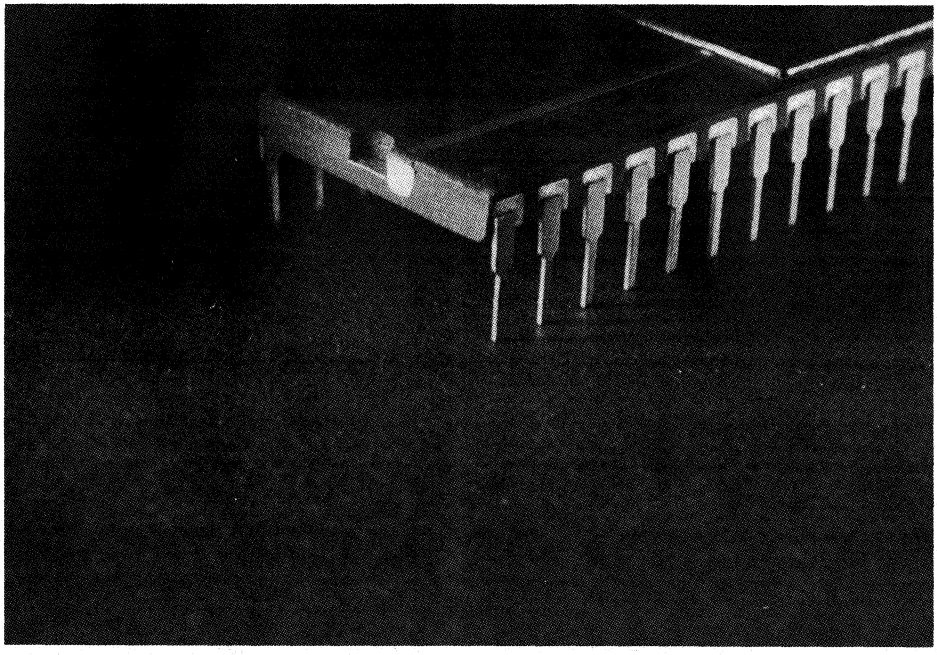
Since our processes are industry compatible, we can enter a program at any level: 1. Complete system design and definition; 2. Artwork generation; 3. Wafer processing.

If you need quick turnaround on mask-programmable options, we can also combine COPLAMOS® technology with CLASP® (which stands for COPLAMOS® Last Stage Programmable), to provide the solution.

As for standard products, Standard Microsystems makes one of the widest lines of standard MOS/LSI circuits for data communications and computer peripherals in the industry.

Standard Microsystems custom circuits have found their way into such industrial, computer, and aerospace applications as computer peripherals, modems, telecommunications, data communications, home entertainment, word processing, pay TV, and many other consumer and industrial uses. In fact, Standard Microsystems has created over 100 different custom designs for the above applications.

Standard or custom LSI? Bring your requirements to Standard Microsystems. We'll give you an unbiased recommendation as to which is the best route for you to take.



STANDARD MICROSYSTEMS CORPORATION
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(516) 273-3100 · TWX-510-227-8898
We keep ahead of our competition so you can keep ahead of yours.

Quality Assurance

It is well understood at Standard Microsystems that for an integrated circuit to be attractive to a system designer, it must provide not only state-of-the-art circuit function, but do so with a high degree of reliability.

The manufacture of reliable quality product is no accident. Although testing is necessary to flag problems as soon as possible, it is an old adage that quality cannot be tested into a product, but must be designed in and built in.

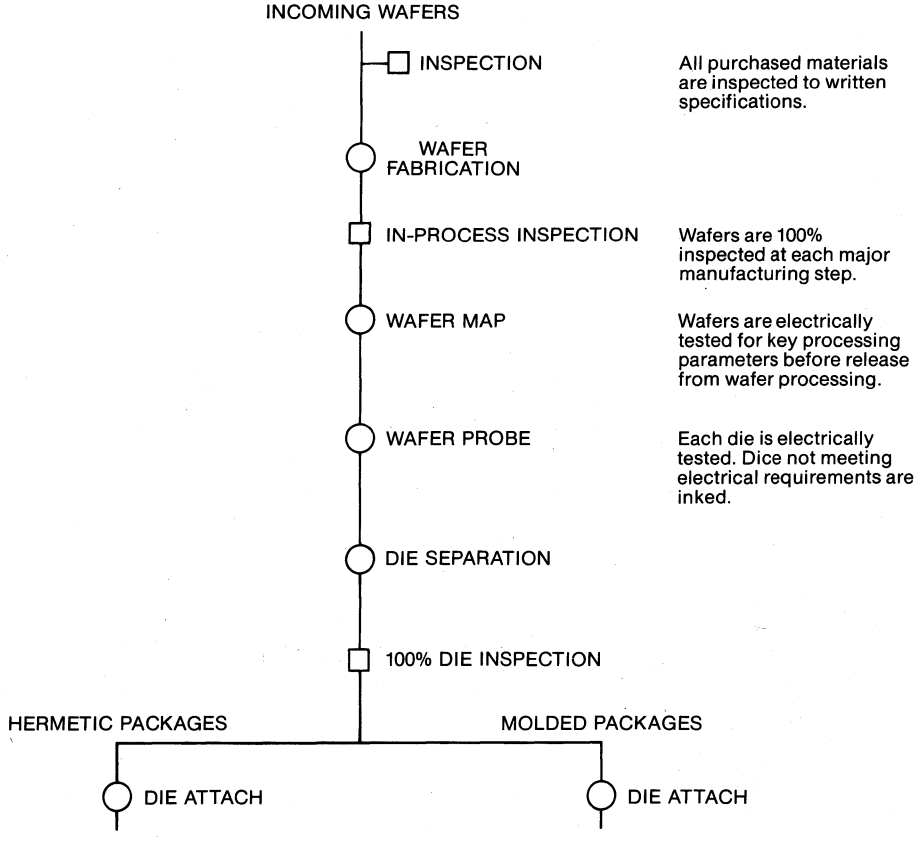
The design of a reliable product is assured by adherence to tested and proven design rules. Before any change in design rules or processing steps is accepted for production, sample runs are exhaustively evaluated for both basic reliability and consistent manufacturability.

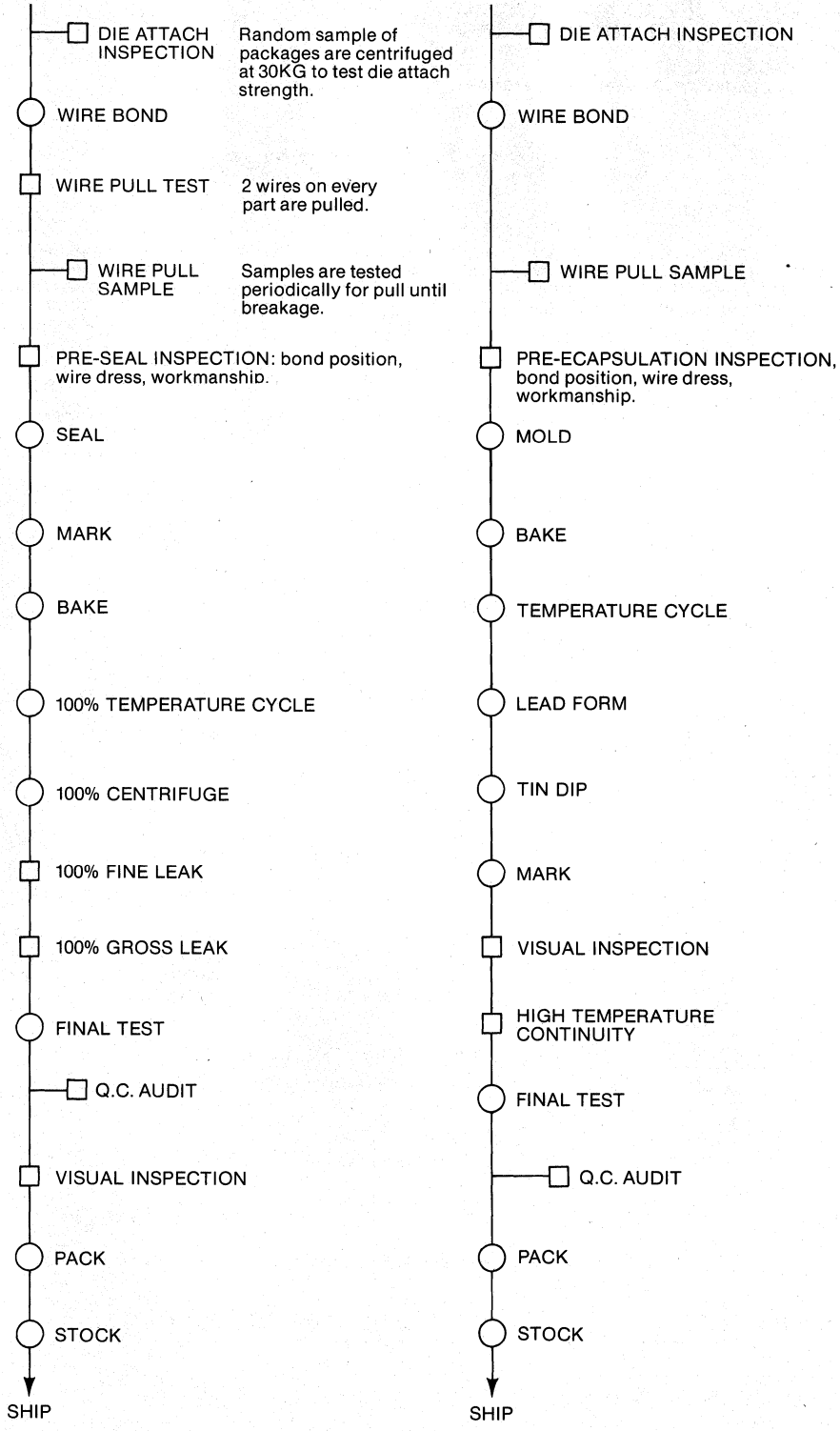
The manufacturing flow is closely monitored by quality assurance to insure not only that all potential failures are identified and rejected, but that proper standards are met for the processing itself. Clean room standards, calibrations and work methods are all monitored.

In addition, test and field failures are analyzed in conjuction with design and process engineering to monitor and correct any possible flaws in either design or manufacture.

Product flow and screening for standard devices is shown on the following flow charts. In addition, MIL-STD-883 level B screening may be done on request.

STANDARD PROCESSING




DIE ATTACH INSPECTION
Random sample of packages are centrifuged at 30KG to test die attach strength.
WIRE BOND
WIRE PULL TEST
2 wires on every part are pulled.
WIRE PULL SAMPLE
Samples are tested periodically for pull until breakage.
PRE-SEAL INSPECTION: bond position, wire dress, workmanship.
SEAL
MARK
BAKE
100% TEMPERATURE CYCLE
100% CENTRIFUGE
100% FINE LEAK
100% GROSS LEAK
FINAL TEST
Q.C. AUDIT
VISUAL INSPECTION
PACK
STOCK
SHIP
DIE ATTACH INSPECTION
WIRE BOND
WIRE PULL SAMPLE
PRE-ECAPSULATION INSPECTION, bond position, wire dress, workmanship.
MOLD
BAKE
TEMPERATURE CYCLE
LEAD FORM
TIN DIP
MARK
VISUAL INSPECTION
HIGH TEMPERATURE CONTINUITY
FINAL TEST
Q.C. AUDIT
PACK
STOCK
SHIP

Data Communication Products

Part Number	Name	Description	Max Baud Rate	Power Supplies	Package	Page
COM 1553A	MIL-STD-1553A UART	MIL-STD-1553 (Manchester) Interface Controller	1 MB	+5	40 DIP	19-34
COM 1671	ASTRO	Asynchronous/Synchronous Transmitter/Receiver, Full Duplex,5-8 data bit, 1X or 32X clock	1 MB	+5, −5, +12	40 DIP	35-50
COM 1863	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	40 KB	+5	40 DIP	51-58
COM 2017	UART	Universal Asynchronous Receiver Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit	25 KB	+5, −12	40 DIP	59-66
COM 2017H	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit	40 KB	+5, −12	40 DIP	59-66
COM 2502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 2 stop bit	25 KB	+5, −12	40 DIP	59-66
COM 2502H	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 2 stop bit	40 KB	+5, −12	40 DIP	59-66
COM 2601	USRT	Universal Synchronous Receiver/ Transmitter, STR, BSC, Bi-sync compatible	250 KB	+5, −12	40 DIP	67-74
COM 2651[1]	USART/PCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bits; 1, 1½, 2 stop bit, 1X, 16X, 64X clock	1 MB	+5	28 DIP	75-76
COM 5025	Multi-Protocol USYNRT	SDLC, HDLC, ADCCP, Bi-sync, DDCMP compatible, automatic bit stuffing/ stripping, frame detection/generation, CRC generation/checking, sync detection	1.5 MB	+5, +12	40 DIP	77-88
COM 8004	32 Bit CRC Generator/ Checker	Companion device to COM 5025 for 32 bit CRC	2.0 MB	+5	20 DIP	89-94
COM 8017	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit	40 KB	+5	40 DIP	95-102
COM 8018	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	40 KB	+5	40 DIP	51-58
COM 8251A	USART	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	64 KB (sync) 9.6 KB (async)	+5	28 DIP	103-118
COM 8502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex,5-8 data bit, 1, 2 stop bit	40 KB	+5	40 DIP	95-102

[1] For future release

STANDARD MICROSYSTEMS CORPORATION
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We keep ahead of our competition so you can keep ahead of yours.

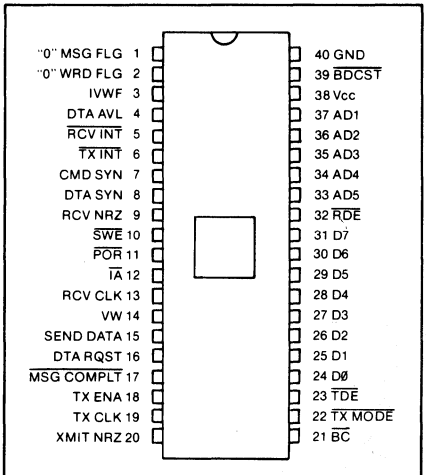
COM 1553A
μPC FAMILY
Preliminary Data

MIL-STD-1553A "SMART®"

FEATURES

- ☐ Support of MIL-STD-1553A
- ☐ Operates as a: Remote Terminal Responding Bus Controller Initiating
- ☐ Performs Parallel to Serial Conversion when Transmitting
- ☐ Performs Serial to Parallel Conversion when Receiving
- ☐ Compatible with HD-15531 Manchester Encoder/ Decoder
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N Channel MOS Technology
- ☐ Available in PC Board Form from Grumman Aerospace Corporation

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

GENERAL DESCRIPTION

The COM 1553A SMART® (Synchronous Mode Avionics Receiver/Transmitter) is a special purpose COPLAMOS N-Channel MOS/LSI device designed to provide the interface between a parallel 8-bit bus and a MIL-STD-1553A serial bit stream.

The COM 1553A is a double buffered serial/parallel and parallel/serial converter providing all of the "hand shaking" required between a Manchester decoder/ encoder and a microprocessor as well as the protocol handling for both a MIL-STD-1553 bus controller and remote terminal.

The COM 1553A performs the following functions in response to a 16 bit Command Word. It provides address detection for the first five bits of the serial data input. If all 1's appear in the address field, a broadcast signal is generated. The sixth bit is decoded as mode: transmit or receive. The next five bits are decoded for zero message flag and special flags in the subaddress/mode field. The last five bits (word-count field) are decoded determining the number of words to be received or transmitted.

When receiving data sync the COM 1553A performs a serial to parallel conversion, buffers the 16 bit message word, and formats it into two parallel (8 bit) bytes for presentation to the I/O bus under processor or hard wired logic control.

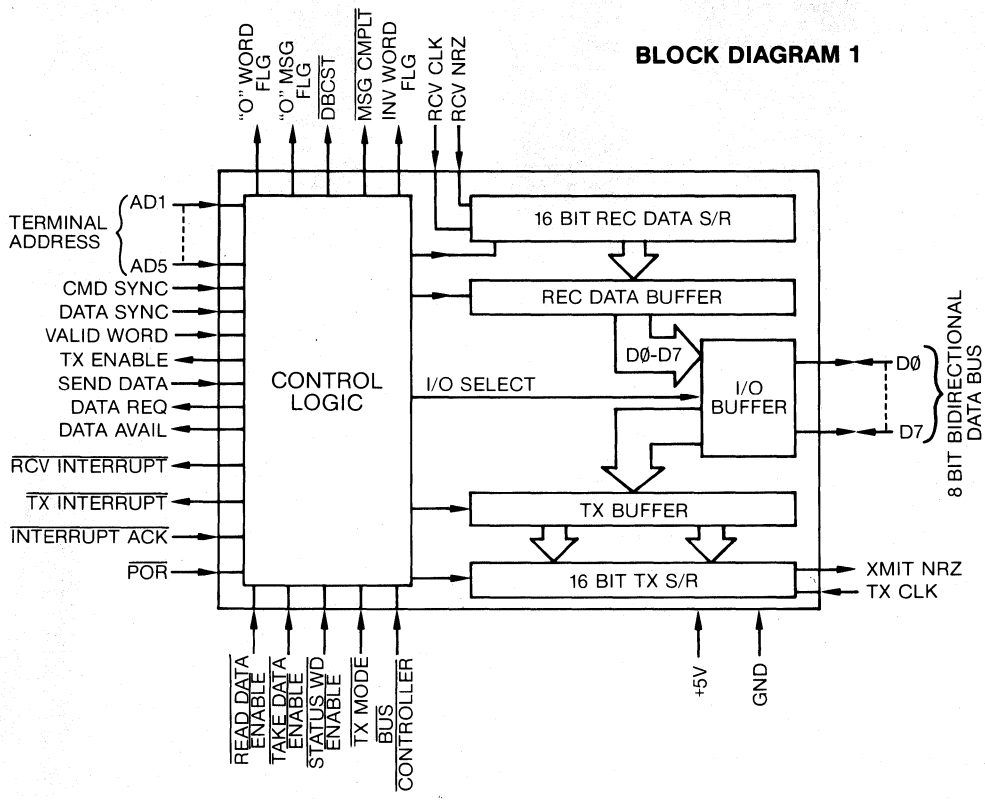
In the transmit mode the COM 1553A takes two parallel 8 bit data words from the I/O bus and serially transmits the resultant 16 bit word to the Manchester encoder. This is done under the control of Send Data. To facilitate data transfer the COM 1553A provides all necessary buffering and storage for transmitted and received data. It also provides all necessary hand shaking, control flags and interrupts to a processor or hard wired logic terminal. See block diagram 1.

The COM 1553A can be set up as either a remote terminal or a bus controller interface.

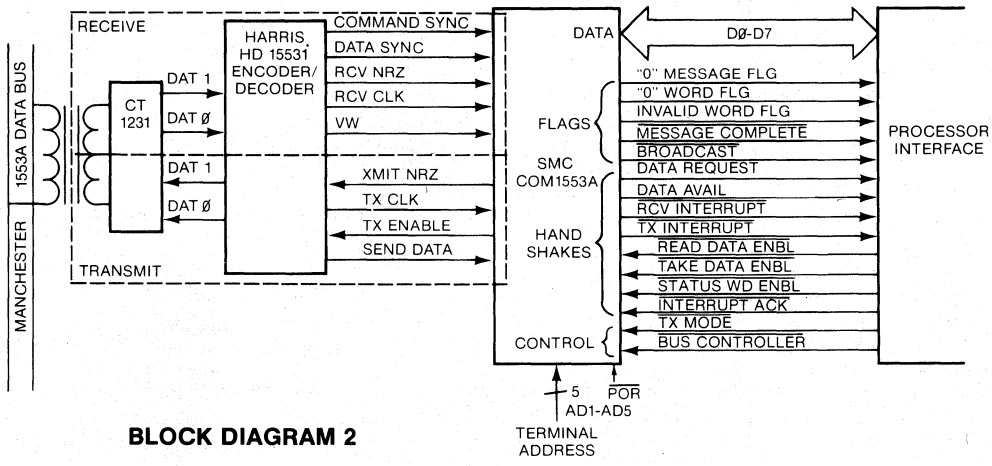
The COM 1553A is compatible with Harris' HD-15531 CMOS Manchester Encoder-Decoder chip and interfaces directly with it. A 3 device kit consisting of: SMC's COM 1553A, Harris' HD-15531 and Circuit Technology's CT1231 forms a complete system interface for the message structure of MIL-STD-1553A. See block diagram 2.

Note: All terminology utilized in this data sheet is consistent with MIL-STD-1553.

BLOCK DIAGRAM 1



BLOCK DIAGRAM 2



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	"Ø" MESSAGE FLAG	ØMF	The ZERO MESSAGE FLAG output is set when the 7th through 11th bits of the NRZ serial input data in a command envelope (see figure 1) are zero. ØMF is an open drain output.
2	"Ø" WORD FLAG	ØWF	The ZERO WORD FLAG output is set when the 12th through 16th bits of the NRZ serial input data in a command envelope (see figure 1) are zero. ØWF is an open drain output.
3	INVALID WORD FLAG	IVWF	The INVALID WORD FLAG output is set when the word just received has an invalid parity bit or invalid format. IVWF is an open drain output.
4	DATA AVAILABLE	DTA AVL	DATA AVAILABLE is set when a word received is ready to be read. When the COM 1553A is the bus controller, DTA AVL occurs on command, status or data words. When the COM 1553A is a remote terminal, DTA AVL is set only on data words. DTA AVL is an open drain output.
5	$\overline{\text{RECEIVE INTERRUPT}}$	$\overline{\text{RCV INT}}$	$\overline{\text{RECEIVE INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a zero and the first 5 bits match AD1-AD5. $\overline{\text{RCV INT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$, or if the line is not active for 32 receive clocks.
6	$\overline{\text{TRANSMIT INTERRUPT}}$	$\overline{\text{TX INT}}$	$\overline{\text{TRANSMIT INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a one, and the first 5 bits match AD1-AD5. $\overline{\text{TXINT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$.
7	COMMAND SYNC	CMD SYN	COMMAND SYNC is an input from the Manchester decoder and must be high for 16 receive clocks enveloping the receive NRZ data of a command word.
8	DATA SYNC	DTA SYN	DATA SYNC is an input from the Manchester decoder and must be high for 16 receive clocks enveloping the receive NRZ data of a data word.
9	RECEIVER NRZ	RCV NRZ	Receiver serial input from Manchester decoder. Data must be stable during the rising edge of the receive clock.
10	$\overline{\text{STATUS WORD ENABLE}}$	$\overline{\text{SWE}}$	$\overline{\text{SWE}}$ is the output enable for the following open drain outputs: ØMF ØWF IVWF DTA AVL $\overline{\text{DTA RQ}}$ $\overline{\text{MSG CPLT}}$
11	$\overline{\text{POWER ON RESET}}$	$\overline{\text{POR}}$	$\overline{\text{POWER ON RESET}}$. Active low for reset.
12	$\overline{\text{INTERRUPT ACKNOWLEDGE}}$	$\overline{\text{IA}}$	$\overline{\text{IA}}$ resets $\overline{\text{TX INT}}$, $\overline{\text{REC INT}}$, ØMF, ØWF and $\overline{\text{BRD CST}}$. $\overline{\text{IA}}$ may occur between the trailing edges of receive clocks 6 and 10, or between the leading edge of receive clock 12 and the falling edge of receive clock 15, or after the falling edge of clock 17.
13	RECEIVE CLOCK	RCV CLK	The RECEIVE CLOCK is synchronous with the Receiver NRZ input during the command sync or data sync envelopes.
14	VALID WORD	VW	This input is driven by the VALID WORD output of the Manchester Decoder. VW should occur immediately after the rise of the first RCV CLK following the fall DATA SYNC or COMMAND SYNC.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
15	SEND DATA	SD	SEND DATA is a "handshake" signal received from the Manchester encoder indicating that the encoder is ready for the COM 1553A to transmit data. SD will bracket 16 transmit data clocks. The contents of the transmitter buffer will be transferred into the transmit register when SD is low.
16	DATA REQUEST	DTA RQST	DATA REQUEST is an open drain output which is set high when the transmitter holding register is ready to accept more data.
17	$\overline{\text{MESSAGE COMPLETE}}$	$\overline{\text{MSG CMPLT}}$	In the receive mode the $\overline{\text{MESSAGE COMPLETE}}$ output is set low when the appropriate number of data words have been received. In the transmit mode, $\overline{\text{MSG CMPLT}}$ indicates that the appropriate number of command, status or data words have been transmitted. When the COM 1553A is a bus controller, $\overline{\text{MSG CMPLT}}$ will be asserted low when 33 command status or data words have been transmitted. $\overline{\text{MSG CMPLT}}$ is an open drain output.
18	TRANSMIT ENABLE	TXENA	A TRANSMIT ENABLE signal will be sent to the Manchester Encoder to initiate transmission of a word. TXENA is generated under the following conditions: 1) COM 1553A is a bus controller: A $\overline{\text{TXMODE}}$ pulse will set TXENA. A second $\overline{\text{TXMODE}}$ pulse will reset TXENA. 2) COM 1553A is a remote terminal. A Transmit Command from the Controller will cause a $\overline{\text{TRANSMIT INTERRUPT}}$ (see pin 6). When this is acknowledged by a TXMODE pulse from the system, TXENA will be set. TXENA will then be reset by either A) Send Data Command associated with the last data word. B) a second $\overline{\text{TXMODE}}$ pulse. 3) COM 1553A is a remote terminal. The falling edge of a DATA SYNC associated with the last data word of a message while in the receive mode. TXENA will be reset during the next SEND DATA envelope.
19	TRANSMIT CLOCK	TXCLK	Transmitter shift clock.
20	TRANSMIT NRZ	XMIT NRZ	Serial data output to the Manchester Encoder.
21	$\overline{\text{BUS CONTROLLER}}$	$\overline{\text{BC}}$	$\overline{\text{BC}}$ determines whether the COM 1553A is acting as bus controller ($\overline{\text{BC}} = 0$) or as a remote terminal ($\overline{\text{BC}} = 1$).
22	$\overline{\text{TRANSMIT MODE}}$	$\overline{\text{TXMODE}}$	$\overline{\text{TXMODE}}$ is a system input controlling transmission. See TXENA (pin 18).
23	$\overline{\text{TAKE DATA ENABLE}}$	$\overline{\text{TDE}}$	$\overline{\text{TDE}}$ is an input from the system initiating transmission. Two $\overline{\text{TDE}}$ pulses are required for each 16 bit data word, one for each 8 data bits placed on DØ-D7.
24-31	DATA BUS	DØ-D7	Bidirectional 8 bit Data Bus to the system. DØ is the LSB. DØ-D7 present open drain outputs.
32	$\overline{\text{READ DATA ENABLE}}$	$\overline{\text{RDE}}$	$\overline{\text{RDE}}$ is an input from the system instructing the COM 1553A to place the received data onto DØ-D7. Two $\overline{\text{RDE}}$ pulses are required per 16 bit data word, one for each 8 bits.
33-37	ADDRESS	AD5-AD1	AD1-AD5 provide addressing to the COM 1553A. Each input has a pull-up resister allowing simple switching to ground to select the user address.
38	POWER SUPPLY	VCC	+5 Volt supply.
39	$\overline{\text{BROADCAST}}$	$\overline{\text{BDCST}}$	$\overline{\text{BDCST}}$ is set low when a "broadcast" command word (the address bits all set to "one") is being received. $\overline{\text{BDCST}}$ is reset by $\overline{\text{IA}}$.
40	GROUND	GND	Ground

OPERATION...RECEIVE MODE

The COM 1553A is considered in the receive mode when TXENA = 0. The most significant bit of both command and data words is received first.

Message reception is initiated when CMD SYN goes high. The next 16 receive clocks are used to shift serial data into RCV NRZ.

The first 5 bits of a command word designate a remote terminal address. These 5 bits are compared with AD1-5. Should the address bits compare, the sixth bit is examined. If it is a zero, a $\overline{\text{RECEIVE INTERRUPT}}$ is generated. If it is a one, a $\overline{\text{TRANSMIT INTERRUPT}}$ is generated.

Bit fields 7-11 and 12-16 are examined for all zeros. All zeros in bit field 7-11 denotes a "ZERO MESSAGE" and all zeros in bit field 12-16 denotes a "ZERO WORD."

Receipt of a data word is indicated when DTA SYN goes high.

When DTA SYN or CMD SYN goes low, the contents of the 16 bit receive register are loaded into the receive buffer. The buffer is organized into two groups of 8 bits each. The most significant 8 bits (byte 1) will be enabled onto the 8 bit data bus on receipt of the first $\overline{\text{RDE}}$ pulse ($\overline{\text{RDE1}}$). The second byte will be enabled on receipt of the second $\overline{\text{RDE}}$ pulse ($\overline{\text{RDE2}}$).

A DATA AVAILABLE is generated for data words only. However, data will be available on DØ-D7 for both command and data words.

If 32 clocks are received after the rising edge of CMD SYN or DTA SYN an "Idle Line Reset" condition exists. This implies that a new CMD SYN or DTA SYN has not yet been received within 16 clocks of the fall of the previous sync signal. The "Idle Line Reset" will reset the following signals:

$\overline{\text{REC INT}}$	"0" MSG FLG
$\overline{\text{TX INT}}$	"0" WRD FLG
$\overline{\text{BRD CST}}$	

When the commanded number of data words have been received, a $\overline{\text{MESSAGE COMPLETE}}$ signal is generated.

As the transmitter and receiver registers operate independently, the COM 1553A will receive its own transmission. The following signals are inhibited during transmission:

$\overline{\text{BC}} = 0$	$\overline{\text{BC}} = 1$
$\overline{\text{REC INT}}$	DAT AVL
$\overline{\text{XMT INT}}$	IVWF
$\overline{\text{BRD CST}}$	$\overline{\text{REC INT}}$
ØWF	$\overline{\text{XMT INT}}$
ØMF	ØMG
JAM MESSAGE ERROR*	ØWF
	$\overline{\text{BRD CST}}$
	JAM MESSAGE ERROR*

*JAM MESSAGE ERROR is an internal signal. See OPERATION...TRANSMIT MODE.

SECTION III

OPERATION...TRANSMIT MODE

The COM 1553A is considered in the transmit mode when TXENA = 1. This is caused by a $\overline{\text{TXMODE}}$ pulse (see description of pin functions, pin 18). The $\overline{\text{TXMODE}}$ pulse in turn is a system response to a transmit command from the receiver.

When the Manchester Encoder receives TXENA = 1, it will respond with SEND DATA = 1. The COM 1553A will then send the system a DATA REQUEST.

Data is loaded into the transmitter data buffer from the 8 bit data bus by pulsing $\overline{\text{TDE}}$. The 8 most significant bits are loaded in by the first $\overline{\text{TDE}}$ pulse ($\overline{\text{TDE1}}$), the 8 least significant bits by the second $\overline{\text{TDE}}$ pulse ($\overline{\text{TDE2}}$).

When SEND DATA (pin 15) is low, the transmitter shift register inputs will follow either the transmit buffer output, JAM ADDRESS or JAM MESSAGE ERROR signals. When SEND DATA is high, the shift register parallel inputs are disabled and the shift register contents are shifted out in NRZ form using the 16 negative edges in the send data envelope.

To facilitate transmission of the status word from a remote terminal, the COM 1553A will "jam" the first (most significant) 6 bits of the status word into the transmit register when $\overline{\text{BC}}$ is high. These bits will automatically be sent at the first SEND DATA pulse. In general for MIL-STD-1553A the remaining 10 bits will normally be all zeros and will automatically be sent out as such. If it is desired to send additional status information (for MIL-STD-1553B), a $\overline{\text{TDE1}}$ pulse will load the least significant 2 bits of the first 8 bit byte, and a $\overline{\text{TDE2}}$ will load all 8 bits of the second byte. Note that these TDE pulses must be sent (and data presented) before the first SD = 1 response from the Manchester Encoder.

A JAM ADDRESS occurs when 1) a transmit command is addressed to the COM 1553A 2) A $\overline{\text{TXMODE}}$ pulse is received and 3) a valid word signal is received. Upon a JAM ADDRESS the COM 1553A will load its address into the first 5 bits of the transmit register.

Alternatively, a JAM ADDRESS will also occur at the fall of the last data sync after valid receive command has been detected.

The JAM ADDRESS function will be inhibited if a "0" word and "0" message condition exists in the command word. The JAM ADDRESS will be reset by the leading edge of SEND DATA.

The JAM MESSAGE ERROR function occurs when, in the receive mode, a data word is not followed by a VALID WORD signal. JAM MESSAGE ERROR consists of loading a one in the sixth bit location of the transmit shift register (the message error location).

JAM MESSAGE ERROR is inhibited when the transmit command word contains "0" Message and "0" Word fields.

When the commanded number of data words has been transmitted a $\overline{\text{MESSAGE COMPLETE}}$ signal will be generated.

GENERAL OPERATION NOTES

1. BUS CONTROLLER. When $\overline{BC} = 0$, signifying that the COM 1553A is the bus controller the following is true:
   A. DTA AVL is generated on the rising edge of the 17th receive clock following a Command Sync or Data Sync. This allows the bus controller to receive command, status or data words regardless of their address.
   B. TXENA is contingent only on $\overline{TXMODE}$. A bus controller can therefore transmit whenever it desires.
   C. The jam functions are inhibited.

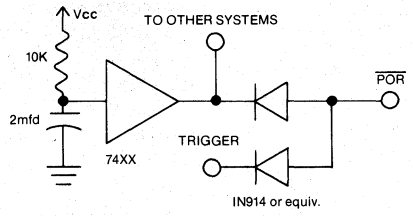
2. INVALID WORD FLAG. When $\overline{BC} = 0$, IVWF will be set if the Valid Word input (from the Manchester decorder) does not go high following receipt of all words. This includes words received from the same device's transmitter. (This provides a validity test of the controller transmission).
   When $\overline{BC} = 1$, IVWF will be set if Valid Word does not go high following receipt of all command and address words addressed to the terminal.
   IVWF will be set for the following conditions:

Message type	*Word*	*Terminal is*	*IVWF generated*
Transit Group	Transmit command	receiving	yes
	Status word	transmitting	no
	Data word	transmitting	no
Receive Group	Receive command	receiving	yes
	Data word	receiving	yes
	Status word	transmitting	no
Receive/Transmit Group (this terminal addressed to receive)	Receive command	receiving	yes
	Transmit command	receiving	no
	Status word	receiving	no
	Data word	receiving	yes
	Status word	transmitting	no
Receive/Transmit group (this terminal addressed to transmit)	Receive command	receiving	no
	Transmit command	receiving	yes
	Status word	transmitting	no
	Data word	transmitting	no
	Status word	receiving	no

3. $\overline{POWER\ ON\ RESET}$. During power-up, $\overline{POR}$ is a low to high exponential with a minimum low time, after the supply is within specified limits, of 10 microseconds. $\overline{POR}$ may also occur asynchronously anytime after power has stabilized.
   $\overline{POR}$ initializes the following outputs:

ØMG	$\overline{REC\ INT}$	$\overline{TDE}$
ØWF	$\overline{MSG\ CMPLT}$	DTA AVL
$\overline{BRD\ CST}$	IVW	TXENA
$\overline{XMT\ INT}$	$\overline{RDE}$	DTA RQ

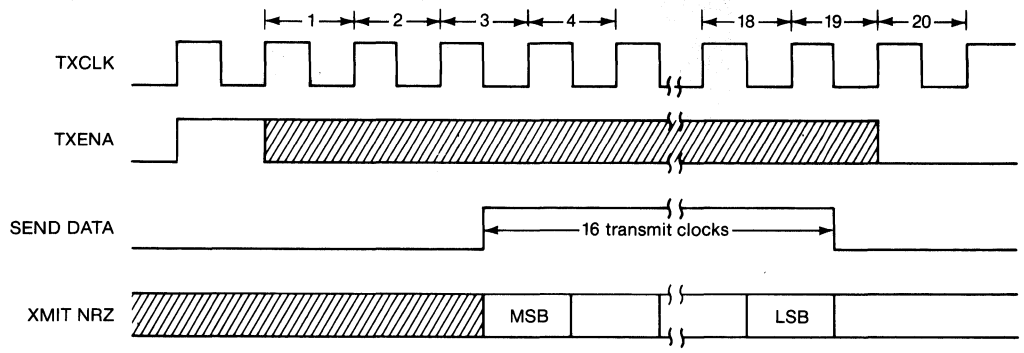
   The following circuit may be used to implement $\overline{POR}$.



4. WORD COUNT: Word count is decoded as follows:

D1	*D2*	*D3*	*D4*	*D5*	*Word Count*
0	0	0	0	1	1
0	0	0	1	0	2
1	1	1	1	1	31
0	0	0	0	0	32

TRANSMIT TIMING FIGURE 1



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

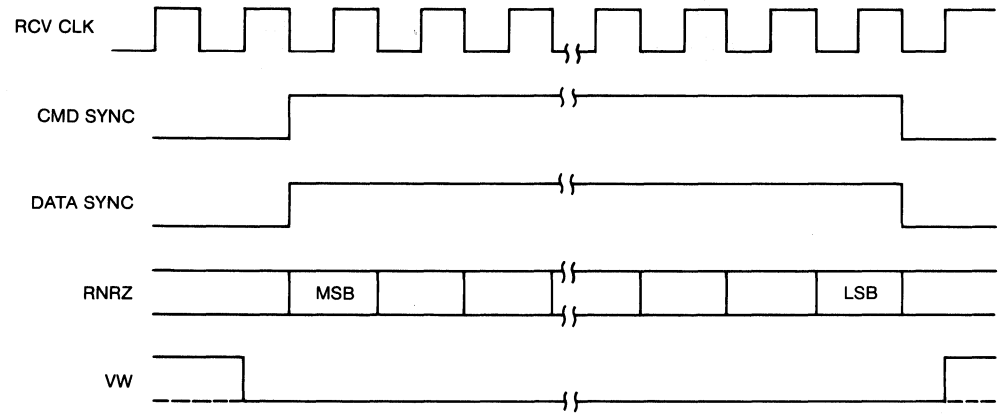
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C, V_{CC} = +5 ±5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	3.0			V	
Output Voltage Levels					
Low Level V_{OL}			0.4	V	I_{OL} = -1.6 mA, except open drain
High Level V_{OH}	3.0	4.0		V	I_{OH} = 100 μA, except open drain
Low Level V_{OL}			0.4	V	I_{OL} = -1.6 mA, open drain output
Output Leakage, I_{LO}			10	μA	
Input Current, AD1-AD5		60		μA	V_{IN} = 0V
Output Capacitance		5	10	pf	
Input Capacitance		10	25	pf	
Power Dissipation			500	mW	

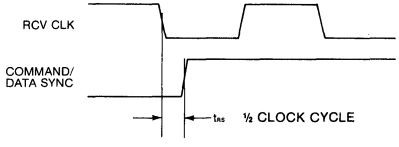
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
AC CHARACTERISTICS						
Clock Frequency	f_T, f_R	980	1000	1020	KHz	
Clock Duty Cycle		45	50	55	%	
Rise and fall times, $\overline{IA}$, $\overline{TDE}$ $\overline{TX\ MODE}$, $\overline{SWE}$, $\overline{RDE}$	t_r, t_f			20	ns	
rise and fall times, all other inputs	t_r, t_f			50	ns	
receiver clock-NRZ	t_{RN}			65	ns	figure 3B
receiver clock-sync delay	t_{SR}			85	ns	figure 3B
receiver clock-VW delay	t_{RV}			100	ns	figure 3B
VW reset delay	t_{VS}			500	ns	figure 3C
transmit clock-TX ENA delay	t_{TX}	25			ns	figure 4A
TX ENA pulse width	t_{XW}	60			ns	figure 4A
transmit clock-send data set-up	t_{TS}			40	ns	figure 4B
transmit clock-send data hold time	t_{ST}			140	ns	figure 4C
transmit clock fall to NRZ	t_{TN}	0			ns	figure 4B
transmit clock rise to NRZ	t_{NT}	95			ns	figure 4B
$\overline{TX\ MODE}$ pulse width	t_{MW}	150			ns	figure 5A
$\overline{TX\ MODE}$ to TX ENA delay	t_{MX}			750	ns	figure 5B
VALID word to TX ENA delay	t_{VX}			750	ns	figure 5B
Data sync to TX ENA delay	t_{DX}			750	ns	figure 5C
TX ENA reset delay	t_{SX}			750	ns	figure 5C
DATA SET-up time	t_{D1}	100			ns	figure 6A
$\overline{TDE}$ pulse width	t_{D2}	150			ns	figure 6A
Data Hold time	t_{D3}	100			ns	figure 6A
Cycle time	t_{D4}	450		16000	ns	figure 6A
DTA RQST Delay	t_{D5}	450			ns	figure 6A
Output Enable time	t_{D6}	100			ns	figure 6B
$\overline{RDE}$ Pulse width	t_{D7}	150			ns	figure 6B
receive cycle time	t_{D8}	450		17000	ns	figure 6B
Flag delay time	t_{D9}	450			ns	figure 6B
Output disable time	t_{D10}	100			ns	figure 6B
SEND DATA delay	t_{D11}	2.5		3.5	μs	figure 6C
TDE off delay	t_{D12}	1.5			μs	figure 6C
$\overline{TDE1}$ delay	t_{D13}	500			ns	figure 6C
SYN to $\overline{RDE}$	t_{D14}	500			ns	figure 6D
RDE to SYN	t_{D15}			2.5	μs	figure 6D
Status word Enable	t_{SE}			100	ns	figure 8A
Status word Disable	t_{SD}			100	ns	figure 8A
Flag delay time	t_{CF}			1	μs	figure 8B
VW delay time	t_{CV}			90	ns	figure 8B
IVWF delay time	t_{CI}			450	ns	figure 8B
DTA AVL delay time	t_{CD}			500	ns	figure 8B
DTA RQST delay time	t_{SR}			450	ns	figure 8C
$\overline{BRD\ CST}$ delay time	t_{RB}			2	μs	figure 8C
$\overline{BRD\ CST}$ pulse width	t_{BW}	1			μs	figure 8D
flag reset delay	t_{IB}			750	ns	figure 8D, 8E
Interrupt delay	t_{RI}			1.5	μs	figure 8D
IA pulse width	t_{IA}	150			ns	figure 8D
Interrupt pulse width	t_{IW}	1			μs	figure 8D
Flag reset time	t_{FR}			450	ns	figure 8F
DTA AVL reset delay	t_{RD}			750	ns	figure 8F
IVWF reset delay	t_{RV}			750	ns	figure 8F
$\overline{MSG\ CMPLT}$ turn-on delay	t_{MR}			1.5	μs	figure 9A, 9B
$\overline{MSG\ CMPLT}$ turn-on delay	t_{MF}			1.5	μs	figure 9A, 9C

RECEIVE TIMING FIGURE 2

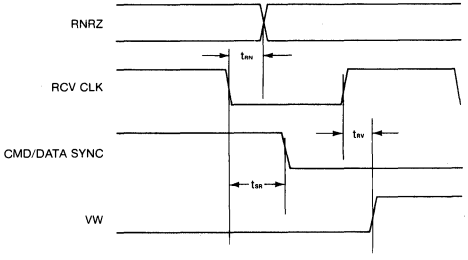


RECEIVER INPUT TIMING FIGURE 3

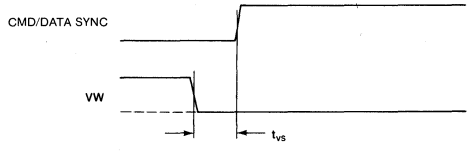
3A



3B

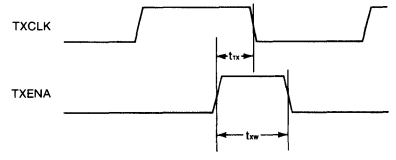


3C

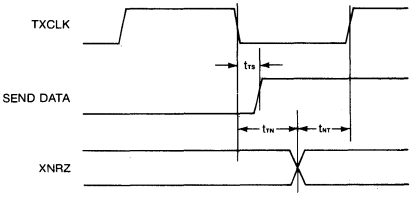


TRANSMITTER TIMING FIGURE 4

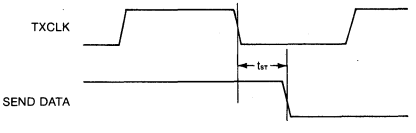
4A



4B

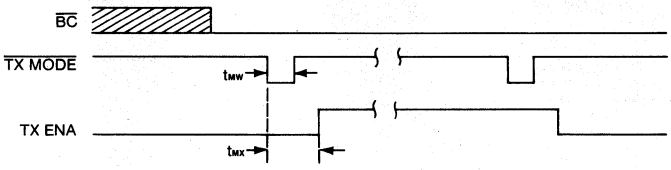


4C

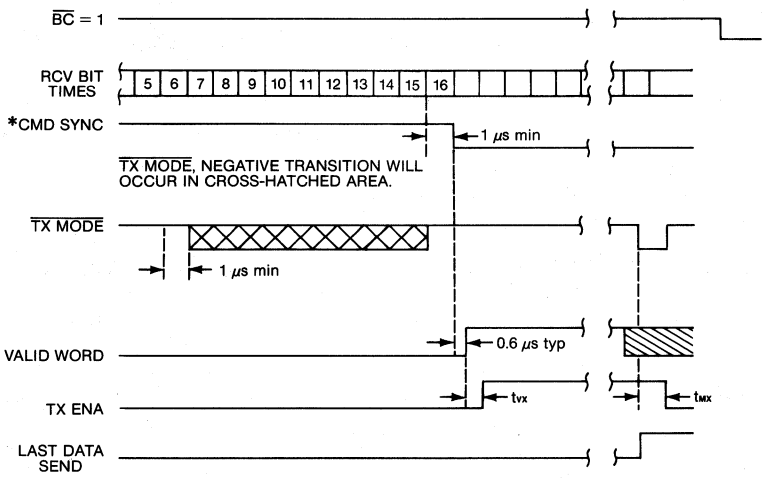


TRANSMIT ENABLE (TX ENA) TIMING FIGURE 5

5A

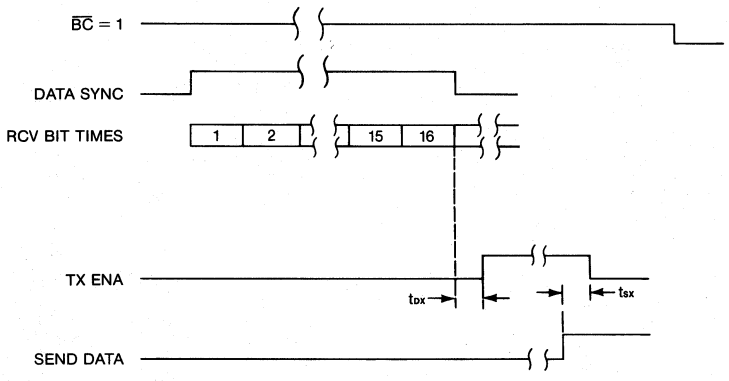


5B*



*THIS IS A CMD WORD BEING RECEIVED. IT IS ADDRESSED TO THIS BUFFER AND THE T/R BIT = 1. TX ENA IS RESET BY 2ND TX MODE NEGATIVE TRANSITION OR BY LAST SEND DATA (MESSAGE COMPLETE FUNCTION).

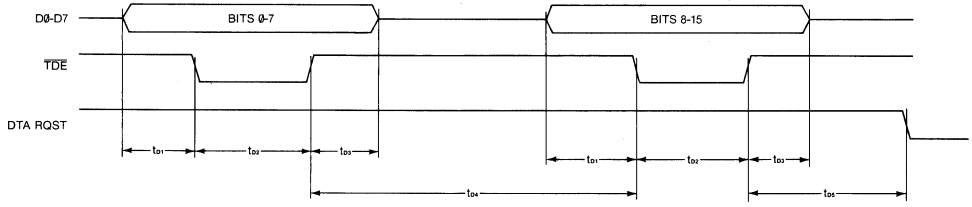
5C**



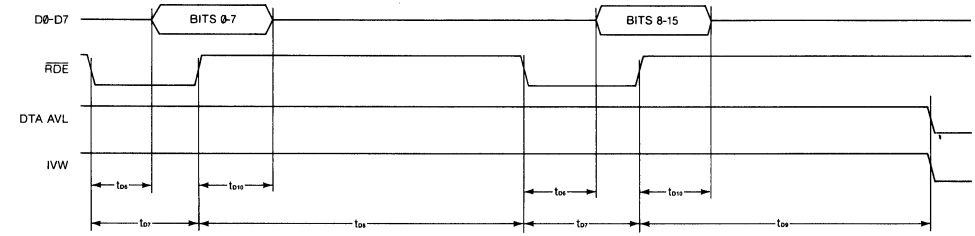
**THIS IS THE LAST DATA WORD BRING RECEIVED. THIS TERMINAL PREVIOUSLY HAD RECEIVED A REC CMD WORD WITH OUR ADDRESS AND A REC/XMIT BIT = 0 DURING THIS MESSAGE SEQUENCE. TX ENABLE IS SET BY MSG CMPLT FUNCTION AND RESET BY RECEIPT OF SEND DATA.

DATA BUS TIMING FIGURE 6

6A

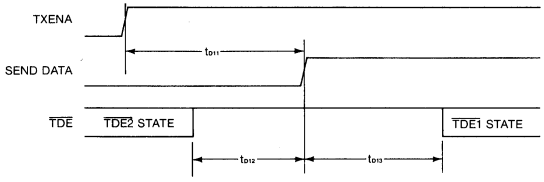


6B



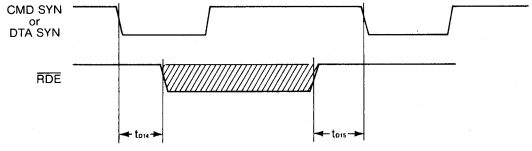
DATA BUS TIMING FIGURE 6

6C

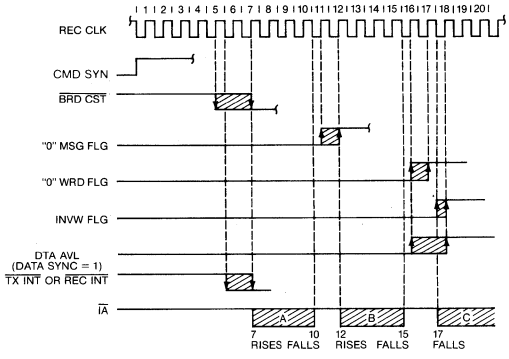


NOTE: SEND DATA RISING EDGE INITIALIZES $\overline{TDE}$ TO $\overline{TDE}$1 STATE

6D



$\overline{IA}$ RESETS FIGURE 7



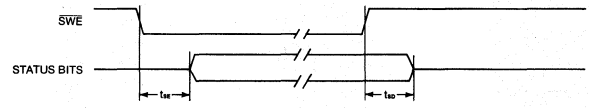
$\overline{IA}$ OCCURRING DURING ZONE A RESETS: BRD CST. TX INT. REC INT.

$\overline{IA}$ OCCURRING DURING ZONE B RESETS: BRD CST. TX INT. REC INT. "0" MSG FLG.

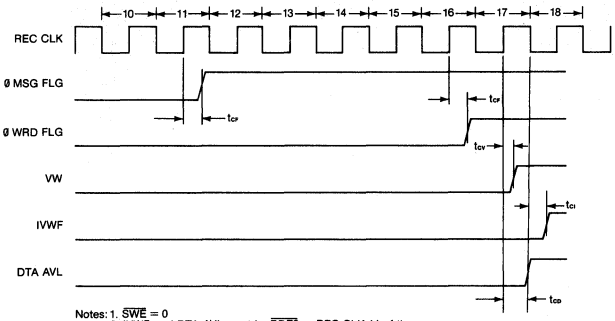
$\overline{IA}$ OCCURRING DURING ZONE C RESETS: BRD CST. TX INT. REC INT. "0" MSG FLG. "0" WRD FLG.

STATUS FLAGS FIGURE 8

8A

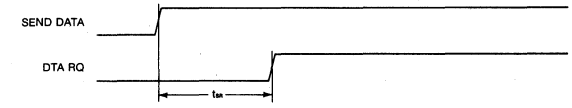


8B

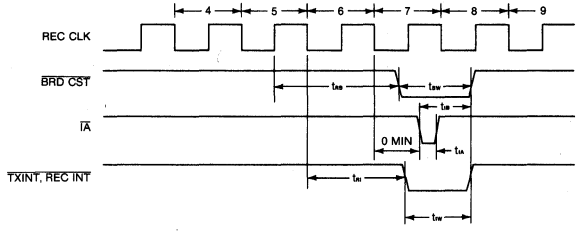


Notes: 1. $\overline{SWE} = 0$
2. IVWF and DTA AVL reset by $\overline{RDE2}$ or REC CLK 14 of the next word

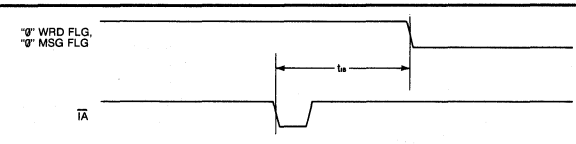
8C



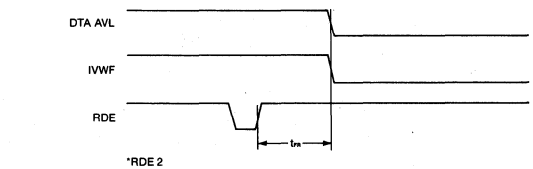
8D



8E

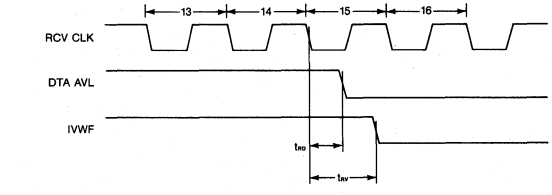


8F



*RDE 2

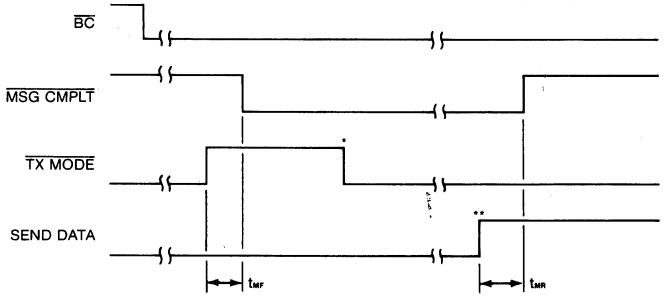
If RDE is not used to reset IVWF and RDE, then they are reset by RCV CLK 14 as shown below.



MESSAGE COMPLETE FIGURE 9

BUS CONTROLLER MODE

9A

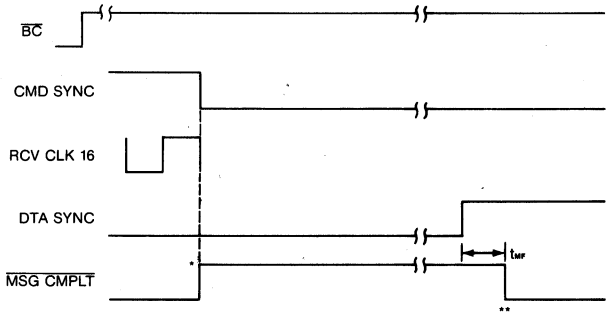


*WORD COUNTER IS PRESET TO 33

**MSG CMPLT SET t_{MR} MAX AFTER RISE OF 33RD SEND DATA PULSE

REMOTE TERMINAL, RECEIVE COMMAND RECEIVED

9B

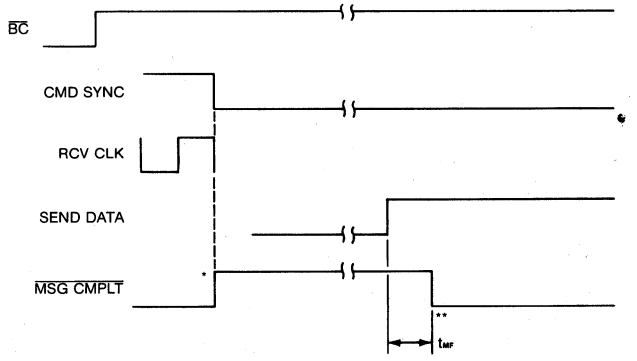


*WORD COUNTER PRESET TO COUNT IN COMMAND WORD

**MSG CMPLT GENERATED BY LAST DATA SYNC OF THE MESSAGE GROUP

REMOTE TERMINAL, TRANSMIT COMMAND RECEIVED

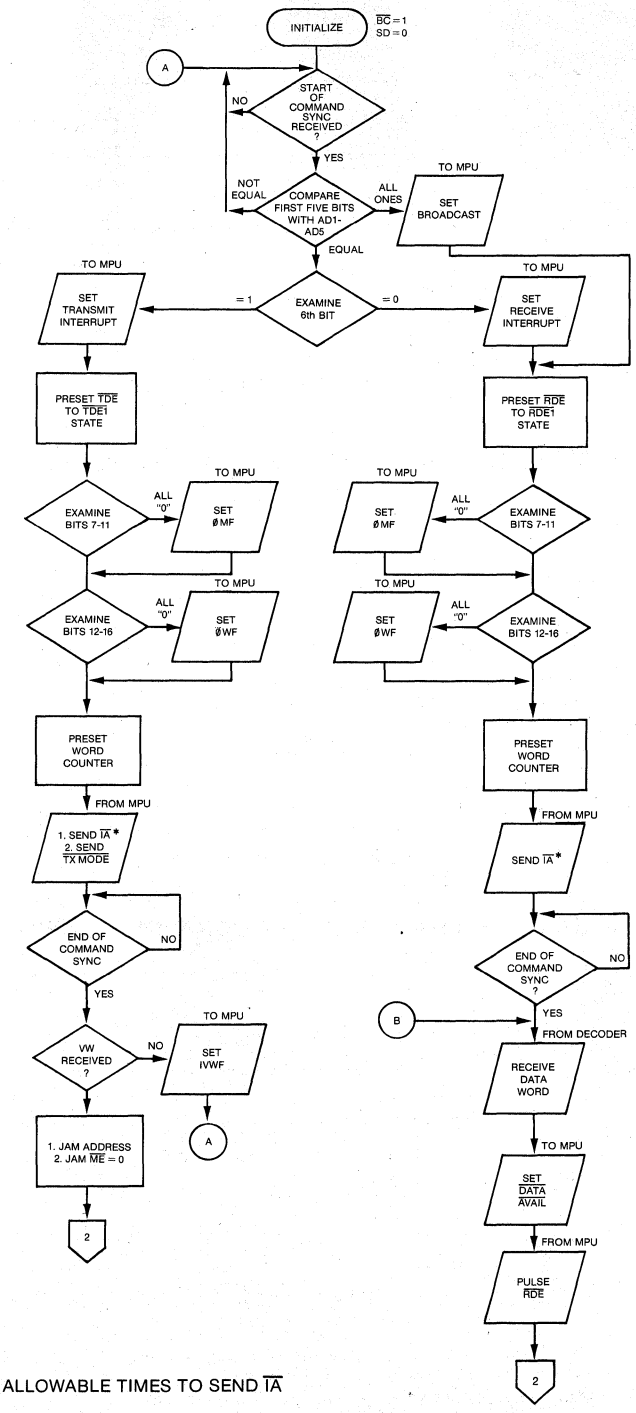
9C



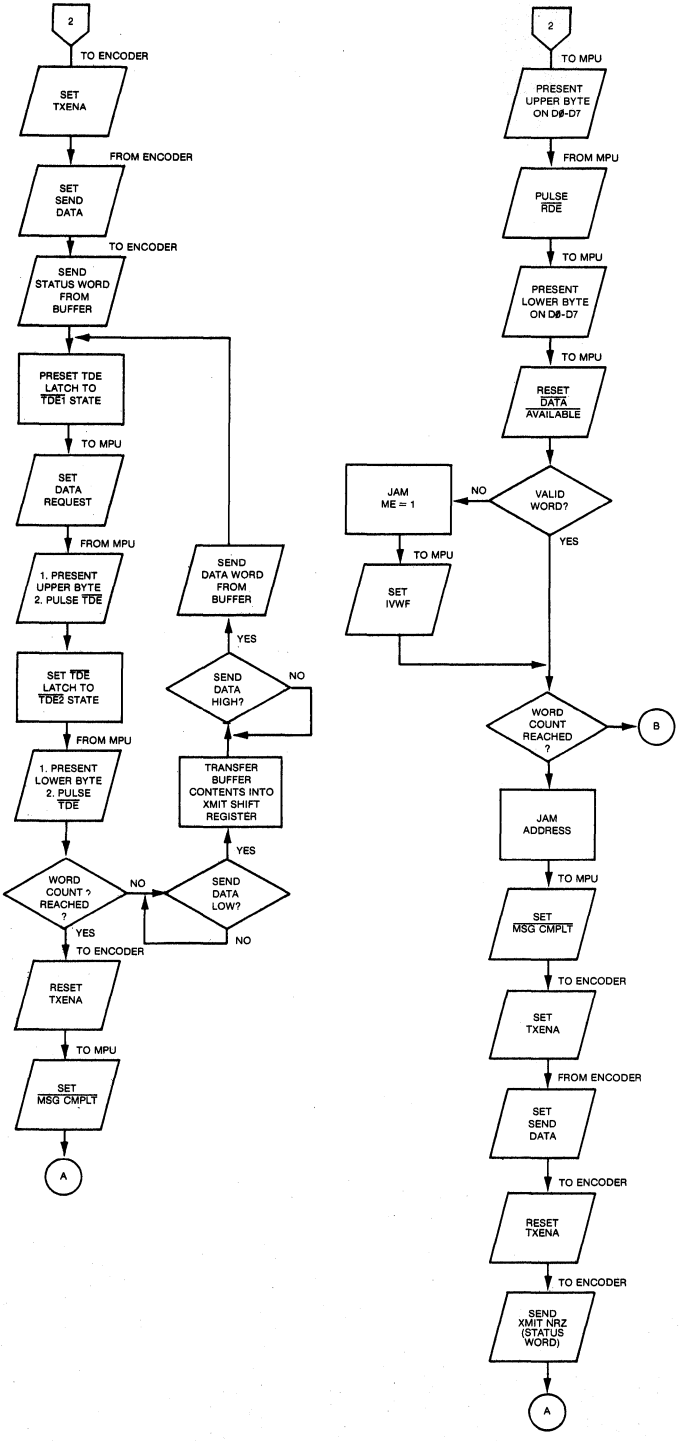
*WORD COUNTER PRESET TO TRANSMIT COMMAND WORD FIELD PLUS 1. THIS ALLOWS FOR THE STATUS WORD.

**MSG CMPLT GENERATED BY THE LAST SEND DATA OF THE TRANSMIT MESSAGE GROUP.

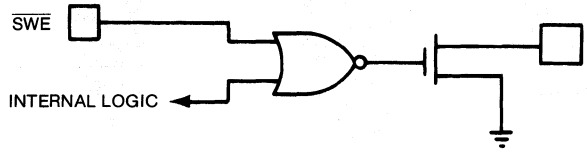
TYPICAL SYSTEM OPERATION



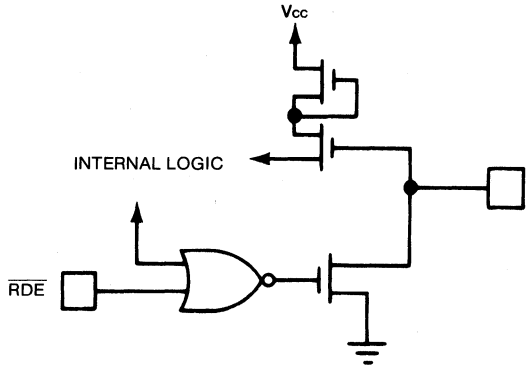
*SEE FIGURE 7 FOR ALLOWABLE TIMES TO SEND $\overline{IA}$


2
TO ENCODER
SET TXENA
FROM ENCODER
SET SEND DATA
TO ENCODER
SEND STATUS WORD FROM BUFFER
PRESET TDE LATCH TO TDE1 STATE
TO MPU
SET DATA REQUEST
FROM MPU
1. PRESENT UPPER BYTE 2. PULSE TDE
SET TDE LATCH TO TDE2 STATE
FROM MPU
1. PRESENT LOWER BYTE 2. PULSE TDE
WORD COUNT ? REACHED ?
NO
YES
TO ENCODER
RESET TXENA
TO MPU
SET MSG CMPLT
A
SEND DATA LOW?
YES
NO
TRANSFER BUFFER CONTENTS INTO XMIT SHIFT REGISTER
SEND DATA HIGH?
YES
NO
SEND DATA WORD FROM BUFFER
2
TO MPU
PRESENT UPPER BYTE ON DØ-D7
FROM MPU
PULSE RDE
TO MPU
PRESENT LOWER BYTE ON DØ-D7
TO MPU
RESET DATA AVAILABLE
VALID WORD?
NO
YES
JAM ME = 1
TO MPU
SET IVWF
WORD COUNT REACHED ?
B
JAM ADDRESS
TO MPU
SET MSG CMPLT
TO ENCODER
SET TXENA
FROM ENCODER
SET SEND DATA
TO ENCODER
RESET TXENA
TO ENCODER
SEND XMIT NRZ (STATUS WORD)
A

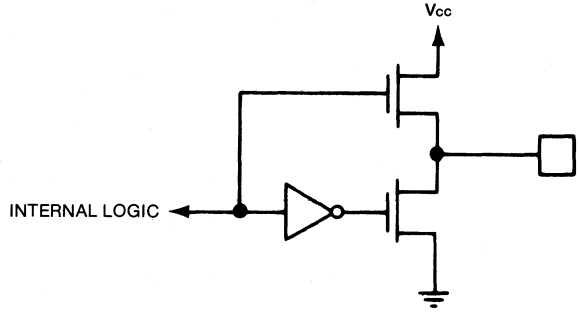
OPEN DRAIN OUTPUT
FIGURE 10



DØ-D7 INPUT/OUTPUT
FIGURE 11



OTHER OUTPUTS
FIGURE 12



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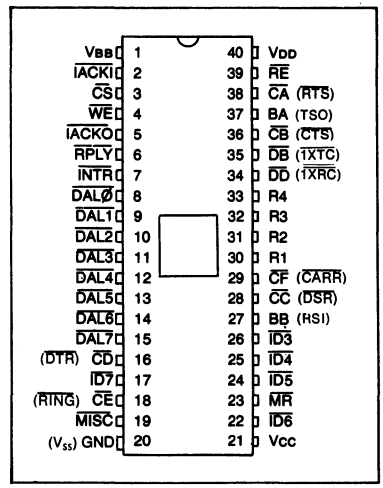
Asynchronous/Synchronous Transmitter-Receiver

ASTRO

FEATURES

- ☐ SYNCHRONOUS AND ASYNCHRONOUS
  - Full Duplex Operations
- ☐ SYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Two Successive SYN Characters Sets Synchronization
  - Programmable SYN and DLE Character Stripping
  - Programmable SYN and DLE-SYN Fill
- ☐ ASYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Selection
  - Start Bit Verification
  - Automatic Serial Echo Mode
- ☐ BAUD RATE—DC TO 1M BAUD
- ☐ 8 SELECTABLE CLOCK RATES
  - Accepts 1X Clock and Up To 4 Different 32X Baud Rate Clock Inputs
  - Up to 47% Distortion Allowance With 32X Clock
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data
  - 8-Bit Bi-Directional Bus For Data, Status, and Control Words
  - All Inputs and Outputs TTL Compatible
  - Up To 32 ASTROS Can Be Addressed On Bus
  - On-Line Diagnostic Capability
- ☐ ERROR DETECTION
  - Parity, Overrun and Framing

PIN CONFIGURATION



- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Pin for Pin replacement for Western Digital UC1671 and National INS 1671
- ☐ Baud Rate Clocks Generated by COM5036 @ 1X and COM5016-6 @ 32X

APPLICATIONS

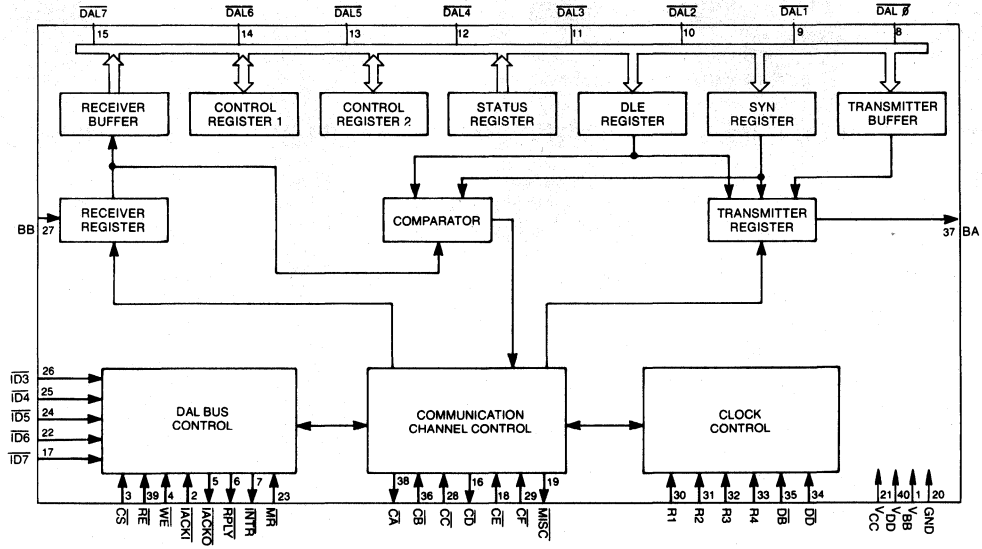
Synchronous Communications
Asynchronous Communications
Serial/Parallel Communications

General Description

The COM1671 (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO contains several "handshaking" signals to insure easy interfacing with modems or other peripheral devices such as display terminals. In addition, a programmable diagnostic mode allows the selection of an internal looping feature which allows the device to be internally connected for processor testing.

The COM1671 provides the system communication designer with a software responsive device capable of handling complex communication formats in a variety of system applications.



Organization

Data Access Lines — The DAL bus is an 8-bit bi-directional port over which all address, data, control, and status transfers occur. In addition to transferring data and control words the DAL bus also transfers information related to addressing of the device, reading and writing requests, and interrupting information.

Receiver Buffer — This 8-bit parallel register presents assembled received characters to the DAL bus when requested through a Read operation.

Receiver Register — This 8-bit shift register inputs the received data at a clock rate determined by Control Register 2. The incoming data is assembled to the selected character length and then transferred to the Receiver Buffer with logic zeroes filling out any unused high-order bit positions.

Syn Register — This 8-bit register is loaded from the DAL bus by a Write operation and holds the synchronization code used for receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Buffer during transmission. This register cannot be read onto the DAL bus. It must be loaded with logic zeroes in all unused high-order bits.

Comparator — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or the DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Buffer. A bit in the Status Register is set when stripping is effected. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

DLE Register — This 8-bit register is loaded from the DAL bus by a Write operation and holds the DLE character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

Status Register — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL bus by a Read operation.

Control Registers — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL bus by a Write operation or read onto the DAL bus by a Read operation. The registers are cleared by a Master Reset.

Transmitter Buffer — This 8-bit parallel register holds data transferred from the DAL bus by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

Transmitter Register — This 8-bit shift register is loaded from the Transmitter Buffer, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the serial data output.

Astro Operation

Asynchronous Mode

Framing of asynchronous characters is provided by a Start bit (logic 0) at the beginning of a character and a Stop bit(s) (logic 1) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit(s). The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit(s) after reception of the last character bit (including the parity bit, if selected). If the Stop bit(s) is a logic 1, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit(s) is a logic 0, the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic 0 when sampled at the theoretical center of the assumed Start bit. As long as the Receiver input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit(s) location, the first sampled logic one is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Buffer is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character (including the parity bit, if selected), then the insertion of a 1, 1.5, or 2 bit length Stop condition. If the Transmitter Buffer is full, the next character transmission starts after the transmission of the Stop bit(s) of the present character in the Transmitter Register. Otherwise, the Mark (logic 1) condition is continually transmitted until the Transmitter Buffer is loaded.

Synchronous Mode

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two contiguous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Buffer, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by the contents of Control Register 2. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Buffer is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

Astro Operation

Receiver

The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receiver Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit with +0%, —3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Check by 1/32nd of a bit period. The Sampling clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic one, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is transferred to the Receiver Buffer; the unused, higher order bits are filled with logic zero's. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Registers. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is transferred to the Receiver Buffer. This error flag indicates that a character has been lost; new data is lost while the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the content of the SYN or the DLE register are not loaded into the Receiver Buffer, and the DR interrupt is not generated, if Bit 3 of Control Register 2 (CR23) or Bit 4 of Control Register 1 (CR14) are set respectively, and SYN Detect and DLE Detect are set with the next non SYN or non DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter

Information is transferred to the Transmitter Buffer by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data occurs only when the Request to Send bit is set to a logic 1 in Control Register 1 and the $\overline{\text{Clear To Send}}$ input is logic 0. Information is normally transferred from the Transmitter Buffer to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Buffer if the Force DLE signal condition is enabled (Bits 5 and 6 of Control Register 1 set to a logic 1). The control bit CR15 must be set prior to loading of a new character in the Transmitter Buffer to insure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Buffer Empty Flag such that transmission of characters occurs within two clock times of the loading of the Transmitter Buffer, when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Buffer is empty. If the Transmitter Buffer is empty, when the Transmitter Register is ready for a new character, the Transmitter enters an idle state. During this idle time a logic 1 will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (CR16 = 1), the idle state will be filled by DLE-SYN character transmission in that order. When entering the Transparent mode DLE must precede the contents of the Transmitter Buffer. This is accomplished by setting of Bit 5 of Control Register 1.

If the transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the $\overline{\text{Clear To Send}}$ goes high the transmitted data output will go high.

When the Transmitter parity is enabled, the selected Odd or Even parity bit is inserted into the last data bit of the character in place of the last bit of the Transmitter Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

Input/Output Operations

All Data, Control, and Status words are transferred over the Data Access Lines (DAL 0-7). Additional input lines provide controls for addressing a particular ASTRO, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller that an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or input takes data from the ASTRO and places it on the DAL bus, while a Write or Output places data from the DAL bus into the ASTRO.

A Read or Write operation is initiated by the placement of an eight-bit address on the DAL bus by the Controller. When the Chip Select signal goes to a logic 0 state, the ASTRO compares Bits 7-3 of the DAL bus with its hard-wired ID code (Pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its RPLY line low to acknowledge its readiness to transfer data. Bit 0 must be a logic O in Read or Write operation. A setup time must exist between CS and the RE or WE signals to allow chip selection prior to read/write operations.

Read

Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	Status Register
110	Receiver Buffer

When the Read Enable (RE) line is set to a logic 0 condition by the Controller the ASTRO gates the contents of the addressed register onto the DAL bus. The Read operation terminates, and the device becomes unselected, when both the Chip Select and Read Enable return to a logic 1 condition. Reading of the Receiver Buffer clears the Data Received Status bit. The data is removed from the DAL bus when the RE signal returns to the logic high state.

Write

Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	SYN and DLE Register
110	Transmitter Buffer

When the Write Enable (WE) line is set to a logic 0 condition by the Controller the ASTRO gates the data from the DAL bus into the addressed register. If data is written into the Transmitter Buffer, the TBMT Status bit is cleared to a logic zero.

The 100 address loads both the SYN and DLE registers. After writing into the SYN register the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses or other ASTROs resets this condition such that the next 100 will address the SYN register.

Interrupts

The following conditions generate interrupts:

Data Received (DR)
Indicates transfer of a new character to the Receiver Buffer while the Receiver is enabled.

Transmitter Buffer Empty (TBMT)
Indicates that the Transmitter Buffer is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty Transmitter Buffer, or after the character is transferred to the Transmitter Register making the Transmitter Buffer empty.

Carrier On
Indicates Carrier Detector input goes low and the Data Terminal Ready (DTR) bit (CR10) is high.

Carrier Off
Indicates Carrier Detector input goes high and the Data Terminal Ready (DTR) bit (CR10) is high.

Data Set Ready On
Indicates the Data Set Ready input goes low and the Data Terminal Ready (DTR) bit (CR10) is high.

Data Set Ready Off
Indicates the Data Set Ready input goes high and the Data Terminal Ready (DTR) bit (CR10) is high.

Ring On
Indicates the Ring Indicator input goes low and the Data Terminal Ready (DTR) bit (CR10) is low.

Each time an interrupt condition exists the INTR output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the Interrupt request by setting the Chip Select (CS) and the Interrupt Acknowledge Input (IACKI) to the ASTRO to a low state. On this transition all non-interrupting devices receiving the IACKI signal set their Interrupt Acknowledge Output (IACKO) low, enabling lower priority daisy-chained devices to respond to the interrupt request. The highest priority device that is interrupting will then set its RPLY line low. This device will place its ID code on Bit Positions 7-3 of the DAL bus when a low RE signal is received. The data is removed from the DAL bus when the Read Enable (RE) signal returns to the logic one state. To reset the Interrupt condition (INTR) Chip Select (CS) and IACKI must be received by the ASTRO.

Description of Pin Functions

Pin No.	Symbol	Pin Name	I/O	Function
1	V_{BB}	POWER SUPPLY	PS	− 5 Volts
21	V_{CC}	POWER SUPPLY	PS	+ 5 Volts
40	V_{DD}	POWER SUPPLY	PS	+ 12 Volts
20	V_{SS}	GROUND	GND	Ground
23	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	The Control and Status Registers and other controls are cleared when this input is low.
8-15	$\overline{DAL0}$-$\overline{DAL7}$	$\overline{DATA\ ACCESS\ LINES}$	I/O	Eight-bit bi-directional bus used for transfer of data, control status, and address information.
17	$\overline{ID7}$	$\overline{SELECT\ CODE}$	I	Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
22	$\overline{ID6}$		I	
24	$\overline{ID5}$		I	
25	$\overline{ID4}$		I	
26	$\overline{ID3}$		I	
3	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	The low logic transition of $\overline{CS}$ identifies a valid address on the DAL bus during Read and Write operations.
39	$\overline{RE}$	$\overline{READ\ ENABLE}$	I	This input, when low, gates the contents of the addressed register from a selected ASTRO onto the DAL bus.
4	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I	This input, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
7	$\overline{INTR}$	$\overline{INTERRUPT}$	O	This open drain output, to facilitate WIRE-ORing, goes low when any interrupt conditions occur.
2	$\overline{IACKI}$	$\overline{INTERRUPT\ ACKNOWLEDGE\ IN}$	I	When the Controller (determining the interrupting ASTRO) makes this input low, the ASTRO places its ID code on the DAL bus and sets reply low if it is interrupting, otherwise it makes $\overline{IACKO}$ a low.
5	$\overline{IACKO}$	$\overline{INTERRUPT\ ACKNOWLEDGE\ OUT}$	O	This output goes low in response to a low $\overline{IACKI}$ if the ASTRO is not the interrupting device.
6	$\overline{RPLY}$	$\overline{REPLY}$	O	This open drain output, to facilitate WIRE-ORing, goes low when the ASTRO is responding to being selected by an address on the DAL bus or in affirming that it is the interrupting source.

Description of Pin Functions

Pin No.	Symbol	Pin Name	I/O	Function
30 31 32 33	R1 R2 R3 R4	CLOCK RATES	I I I I	These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by bits 0-2 of Control Register 2.
37	BA	TRANSMITTED DATA	O	This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.
27	BB	RECEIVED DATA	I	This input receives serial data into the ASTRO.
38	$\overline{CA}$	$\overline{REQUEST\ TO\ SEND}$	O	This output is enabled by bit 1 of Control Register 1 and remains in a low state during transmitted data from the ASTRO.
36	$\overline{CB}$	$\overline{CLEAR\ TO\ SEND}$	I	This input, when low, enables the transmitter section of the ASTRO.
28	$\overline{CC}$	$\overline{DATA\ SET\ READY}$	I	This input generates an interrupt when going ON or OFF while the Data Terminal Ready signal is ON. It appears as bit 6 in the Status Register.
16	$\overline{CD}$	$\overline{DATA\ TERMINAL\ READY}$	O	This output is generated by bit 0 in Control Register 1 and indicates Controller readiness.
18	$\overline{CE}$	$\overline{RING\ INDICATOR}$	I	This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the OFF condition.
29	$\overline{CF}$	$\overline{CARRIER\ DETECTOR}$	I	This input from the Data Set generates an interrupt when going ON or OFF if Data Terminal Ready is ON. It appears as bit 5 in the Status Register.
35	$\overline{DB}$	$\overline{TRANSMITTER\ TIMING}$	I	This input is the Transmitter 1X Data Rate Clock. Its use is selected by bits 0-2 of Control Register 2. The transmitted data changes on the negative transition of this signal.
34	$\overline{DD}$	$\overline{RECEIVER\ TIMING}$	I	This input is the Receiver 1X Data Rate Clock. Its use is selected by bits 0-2 of Control Register 2. The Received Data is sampled by the ASTRO on the positive transition of this signal.
19	$\overline{MISC}$	$\overline{MISCELLANEOUS}$	O	This output is controlled by bits 4 and 5 of Control Register 1 and is used as an extra programmable signal.

Device Programming

The two 8-bit Control Registers of the ASTRO determine the operative conditions of the ASTRO chip.

Control Register 1

BIT 7	6	5	4	3	2	1	0
SYNC/ASYNC 0 – LOOP MODE 1 – NORMAL MODE	ASYNC 0 – NONBREAK MODE 1 – BREAK MODE TX SYNC 0 – TRANSMITTER NON TRANSPARENT MODE 1 – TRANSMITTER TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0 – 1½ or 2 STOP BIT SELECTION 1 – SINGLE STOP BIT SELECTION ASYNC (TRANS. DISABLED) 0 – $\overline{\text{MISC}}$ OUT = 1 1 – $\overline{\text{MISC}}$ OUT = 0 SYNC (CR16 = 0) 0 – NO PARITY GENERATED 1 – TRANSMIT PARITY ENABLED SYNC (CR16 = 1) 0 – NO FORCE DLE 1 – FORCE DLE	ASYNC 0 – NON ECHO MODE 1 – AUTO ECHO MODE SYNC (CR12 = 1) 0 – DLE STRIPPING NOT ENABLED 1 – DLE STRIPPING ENABLED SYNC (CR12 = 0) 0 – $\overline{\text{MISC}}$ OUT = 1 1 – $\overline{\text{MISC}}$ OUT = 0	ASYNC 0 – NO PARITY ENABLED 1 – PARITY CHECK ENABLED ON RECEIVER AND PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0 – RECEIVER PARITY CHECK IS DISABLED 1 – RECEIVER PARITY CHECK IS ENABLED	SYNC/ASYNC 0 – RECEIVER DISABLED 1 – RECEIVER ENABLED	SYNC/ASYNC 0 – SETS $\overline{\text{RTS}}$ OUT = 1 1 – SETS $\overline{\text{RTS}}$ OUT = 0	SYNC/ASYNC 0 – SETS $\overline{\text{DTR}}$ OUT = 1 1 – SETS $\overline{\text{DTR}}$ OUT = 0

Bit 0

Controls the Data Terminal Ready output on Pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The $\overline{\text{DTR}}$ output is inverted from the state of CR10.

Bit 1

Controls the Request to Send output on Pin 38 to control the CA circuit of the Data Set. The $\overline{\text{RTS}}$ output is inverted from the state of CR11. A logic 1 combined with a low logic Clear to Send input enables the Transmitter and allows TBMT interrupts to be generated. A logic 0 disables the Transmitter and turns off the external Request to Send signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The Request to Send output may be used for other functions such as Make Busy on 103 Data Sets.

Bit 2

A logic 1 enables the ASTRO to receive data into the Receiver Buffer, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

Bit 3

Asynchronous Mode

A logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

Synchronous Mode

A logic 1 bit enables check of parity on received characters only. Note: Transmitter parity enable is controlled by CR15.

Bit 4

Asynchronous Mode

A logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmitter Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeroes (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

Synchronous Mode

A logic 1, with the Receiver enabled does not allow assembled Receiver data matching the DLE register contents to be transferred to the Receiver Buffer; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on Pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver, a logic 1 on this bit also causes the Receiver timing to synchronize on Mark-To-Space transitions.

Bit 5

Asynchronous Mode

A logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes transmission of 2 stop bits for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on Pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

Synchronous Mode

A logic 1 combined with a logic 0 on Bit 6 of Control Register 1 enables Transmit parity; if CR15=0 or CR16=1 no parity is generated. When set to a logic 1 with Bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Buffer as part of the Transmitter Transparent mode.

Bit 6

Asynchronous Mode

A logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Buffer.

Synchronous Mode

A logic 1 conditions the Transmitter to a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE character can be forced ahead of any character in the Transmitter Buffer (Bit 5 above). When forcing DLE transmission, Bit 5 should be set to a logic 1 prior to loading the Transmitter Buffer, otherwise the character in the latter register may be transferred to the Transmitter Register prior to sending the DLE character.

Bit 7

A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

a. The Transmit Data is connected to the Receive Data with the BA pin held in a Mark condition and the input to the BB pin disregarded.

b. With a 1X clock selected, the Transmitter Clock also becomes the Receive Clock.

c. The Data Terminal Ready (DTR) Control bit is connected to the $\overline{\text{Data Set Ready}}$ ($\overline{\text{DSR}}$) input, with the $\overline{\text{Data Terminal Ready}}$ ($\overline{\text{DSR}}$) output pin held in an OFF condition (logic high), and the $\overline{\text{DSR}}$ input pin is disregarded.

d. The Request to Send Control bit is connected to the $\overline{\text{Clear To Send}}$ ($\overline{\text{CTS}}$) and $\overline{\text{Carrier Detector}}$ ($\overline{\text{CF}}$) inputs, with the $\overline{\text{Request To Send}}$ ($\overline{\text{RTS}}$) output pin held in an OFF condition (logic high), and the $\overline{\text{CTS}}$ and $\overline{\text{Carrier Detector}}$ input pins are disregarded.

e. The $\overline{\text{Miscellaneous}}$ pin is held in an OFF (logic high) condition.

A logic 1 on Bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

Control Register 2

Control Register 2, unlike Control Register 1, cannot be changed at any time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state.

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0 – ASYNCHRONOUS MODE 1 – SYNCHRONOUS MODE	SYNC/ASYNC 0 – EVEN PARITY SELECT 1 – ODD PARITY SELECT	ASYNC 0 – RECEIVER CLK = RATE 1 1 – RECEIVER CLOCK DETERMINED BY BITS 2-0 SYNC (CR16 = 0) 0 – NO SYN STRIP 1 – SYN STRIP SYNC (CR16 = 1) 0 – NO DLE-SYN STRIP 1 – DLE-SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 – 1X CLOCK 001 – RATE 1 CLOCK 010 – RATE 2 CLOCK 011 – RATE 3 CLOCK 100 – RATE 4 CLOCK 101 – RATE 4 CLOCK ÷ 2 110 – RATE 4 CLOCK ÷ 4 111 – RATE 4 CLOCK ÷ 8

Bits 0-2
These bits select the Tranmit and Receive clocks.

Bits	Clock Source	
2 1 0	Tx	Rx
0 0 0	1X Clock (Pin 35)	1X Clock (Pin 34)
0 0 1	Rate 1 32X clock (Pin 30)	
0 1 0	Rate 2 32X clock (Pin 31) *	
0 1 1	Rate 3 32X clock (Pin 32) *	
1 0 0	Rate 4 32X clock (Pin 33) *	
1 0 1	Rate 4 32X clock (Pin 33) (÷ 2) *†	
1 1 0	Rate 4 32X clock (Pin 33) (÷ 4) *†	
1 1 1	Rate 4 32X clock (Pin 33) (÷ 8) *†	

NOTES:
*Rx clock is modified by bit 3 in the asynchronous mode.
†Rate 4 is internally dividable so that the required 32X clock may be derived from an applied 64X, 128X, or 256X clock which may be available.

Bits 3

Asynchronous Mode

A logic 0 selects the Rate 1 32X clock input (Pin 30) as the Receiver clock rate and a logic 1 selects the same clock rate for the Receiver as selected by Bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by Bits 2-0.

Synchronous Mode

A logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip (CR14) is a logic 1, or all SYN characters in the Non-transparent mode to be stripped out and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as is transferred to the Receiver Buffer.

Bit 4
A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

Bit 5
A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

Bits 6-7
These bits select the full character length (including parity, if selected) as shown above. When parity is enabled it must be considered as a bit when making character length selection (5 bits plus parity = 6 bits).

Status Register

The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set.

7	6	5	4	3	2	1	0
• Data Set Change	• Data Set Ready (DSR)	• Carrier Detector	• Framing Error • Syn Detect	• DLE Detect • Parity Error	• Overrun Error	• Data Received (DR)	• Transmitter Buffer Empty (TBMT)

Bit 0
A logic 1 indicates that the Transmitter Buffer may be loaded with new data. It is set to a logic 1 when the contents of the Transmitter Buffer is transferred to the Transmitter Register. It is cleared when the Transmitter Buffer is loaded from the DAL bus, or when the Transmitter is disabled.

Bit 1
A logic 1 indicates that an entire character has been received and transferred into the Receiver Buffer. It is cleared when the Receiver Buffer is read onto the DAL bus, or the Receiver is disabled.

Bit 2
A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Buffer has not been read and Data Received is not reset, at the time a new character is to be transferred to the Receiver Buffer. This bit is cleared when no Overrun condition is detected (the next character transfer time) or when the Receiver is disabled.

Bit 3
When the DLE Strip is enabled (CR14) the Receiver parity check is disabled and this bit is set to a logic 1 if the previous character to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is reset on the next character transfer or on a Status Register Read. If DLE Strip is not enabled this bit is set to a logic 1 when the Receiver is enabled, Receiver parity (CR13) is also enabled, and the last received character has a Parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in both modes when the Receiver is disabled.

Bit 4

Asynchronous Mode

A logic 1 indicates that the received data did not have a valid stop bit, while the Receiver was enabled, which indicates a Framing error. This bit is set to a logic 0 if the stop bit (logic 1) was detected.

Synchronous Mode

A logic 1 indicates that the contents of the Receiver Register matches the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character.

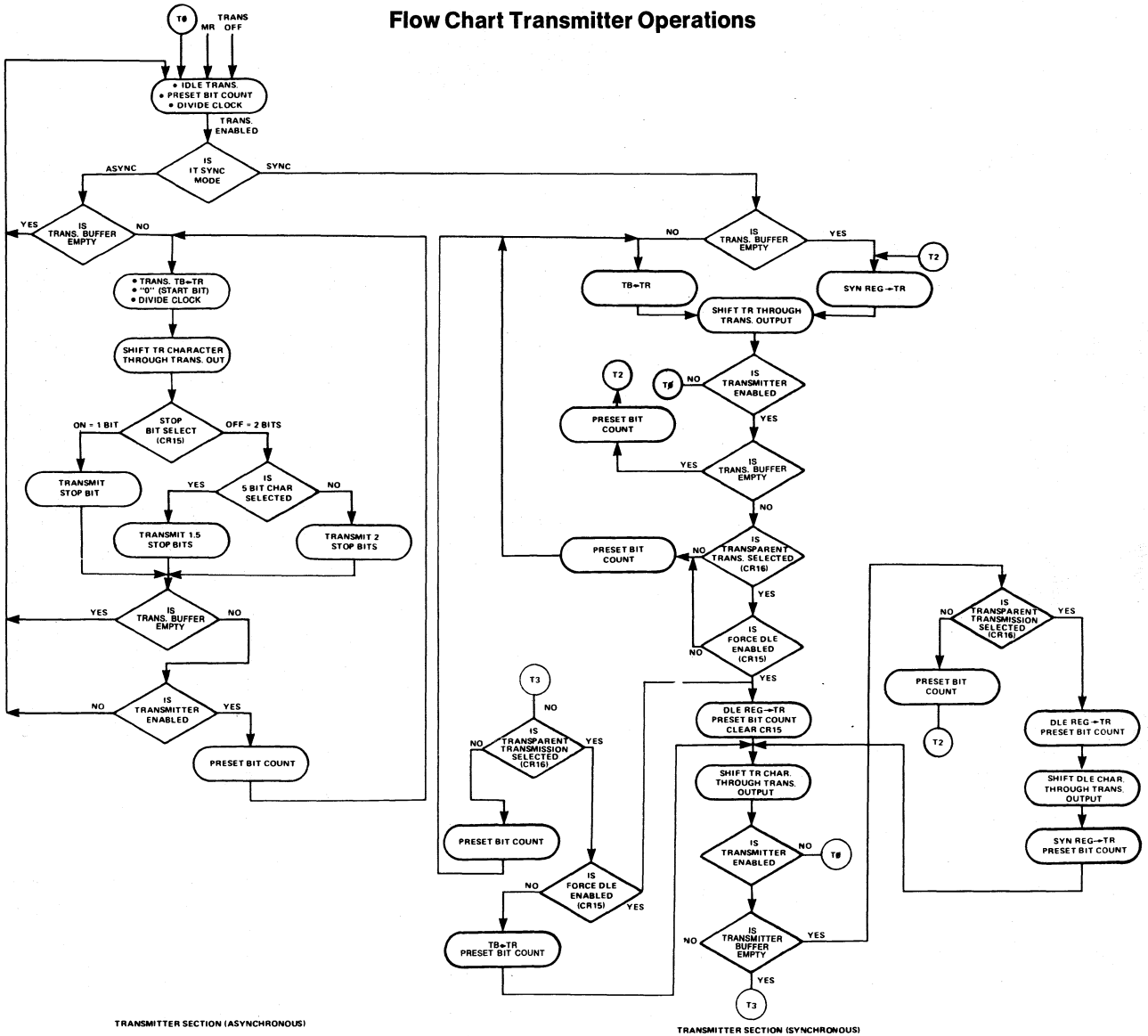
In both modes the bit is cleared when the Receiver is disabled.

Bit 5
This bit is the logic complement of the $\overline{\text{Carrier Detector}}$ input on Pin 29.

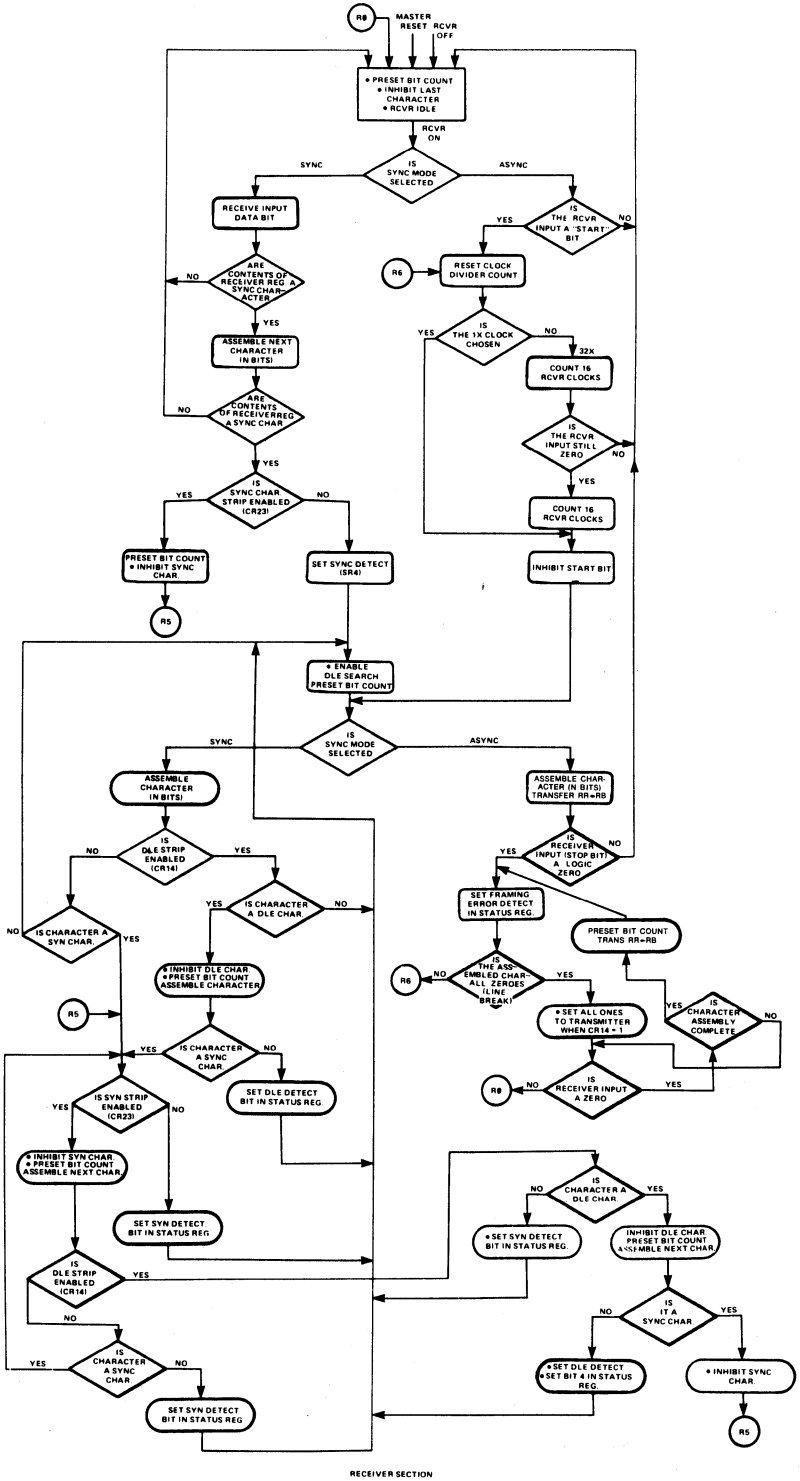
Bit 6
This bit is the logic complement of the $\overline{\text{Data Set Ready}}$ input on Pin 28. With 202-type Data Sets it can be used for Secondary Receive.

Bit 7
This bit is set to a logic 1 whenever there is a change in state of the $\overline{\text{Data Set Ready}}$ or $\overline{\text{Carrier Detector}}$ inputs while Data Terminal Ready (CR10) is a logic 1 or the $\overline{\text{Ring Indicator}}$ is turned ON, with DTR a logic 0. This bit is cleared when the Status Register is read onto the DAL bus.

Flow Chart Transmitter Operations

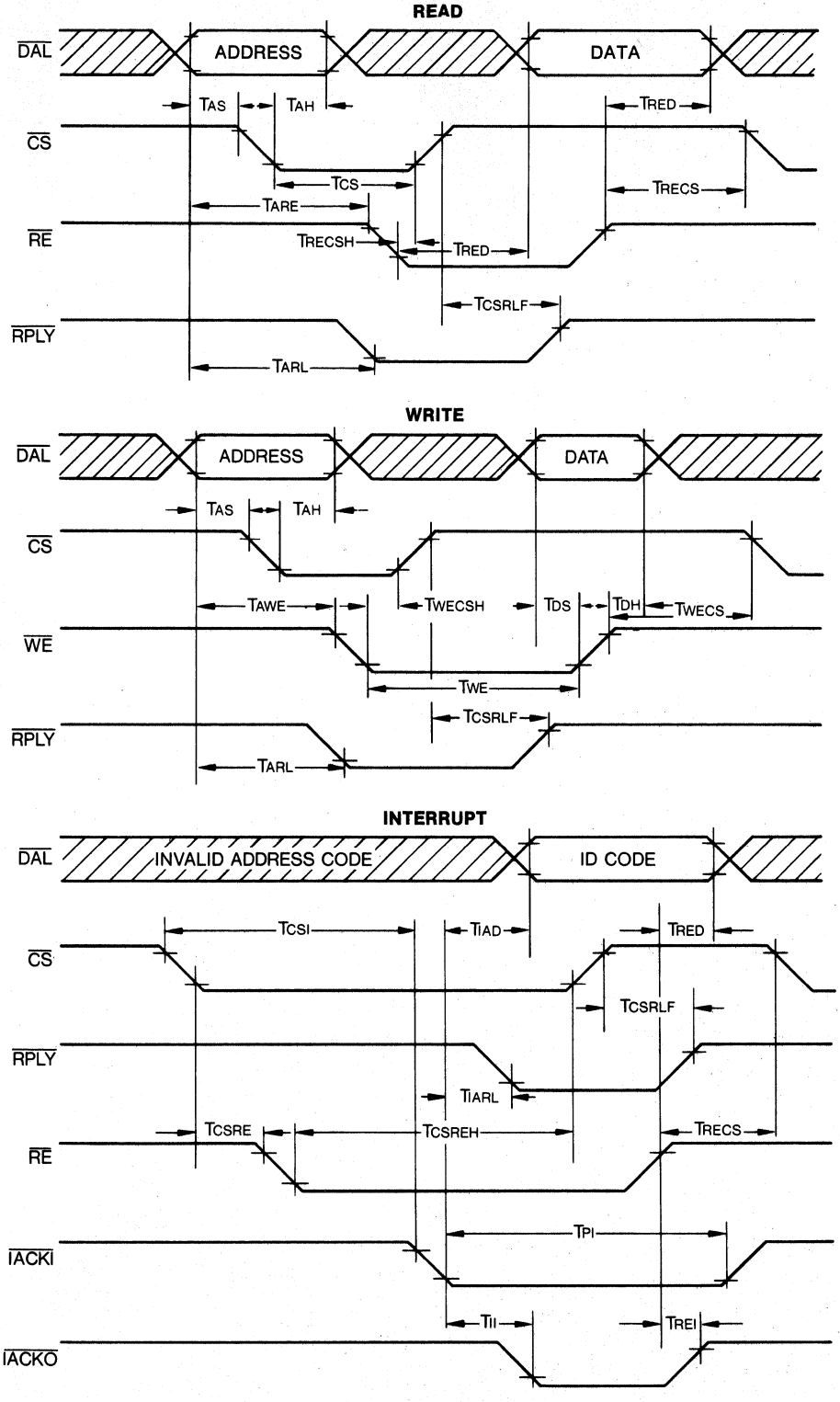


Flow Chart Receiver Operations



RECEIVER SECTION

SECTION III


READ
DAL
ADDRESS
DATA
TAS
TAH
TRED
CS
TCS
TRECS
TARE
RE
TRECSH
TRED
TCSRLF
RPLY
TARL
WRITE
DAL
ADDRESS
DATA
TAS
TAH
CS
TAWE
TWECSH
TDS
TDH
TWECS
WE
TWE
TCSRLF
RPLY
TARL
INTERRUPT
DAL
INVALID ADDRESS CODE
ID CODE
TCSI
TIAD
TRED
CS
TCSRLF
RPLY
TIARL
TCSRE
TCSREH
TRECS
RE
TPI
IACKI
TII
TREI
IACKO

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

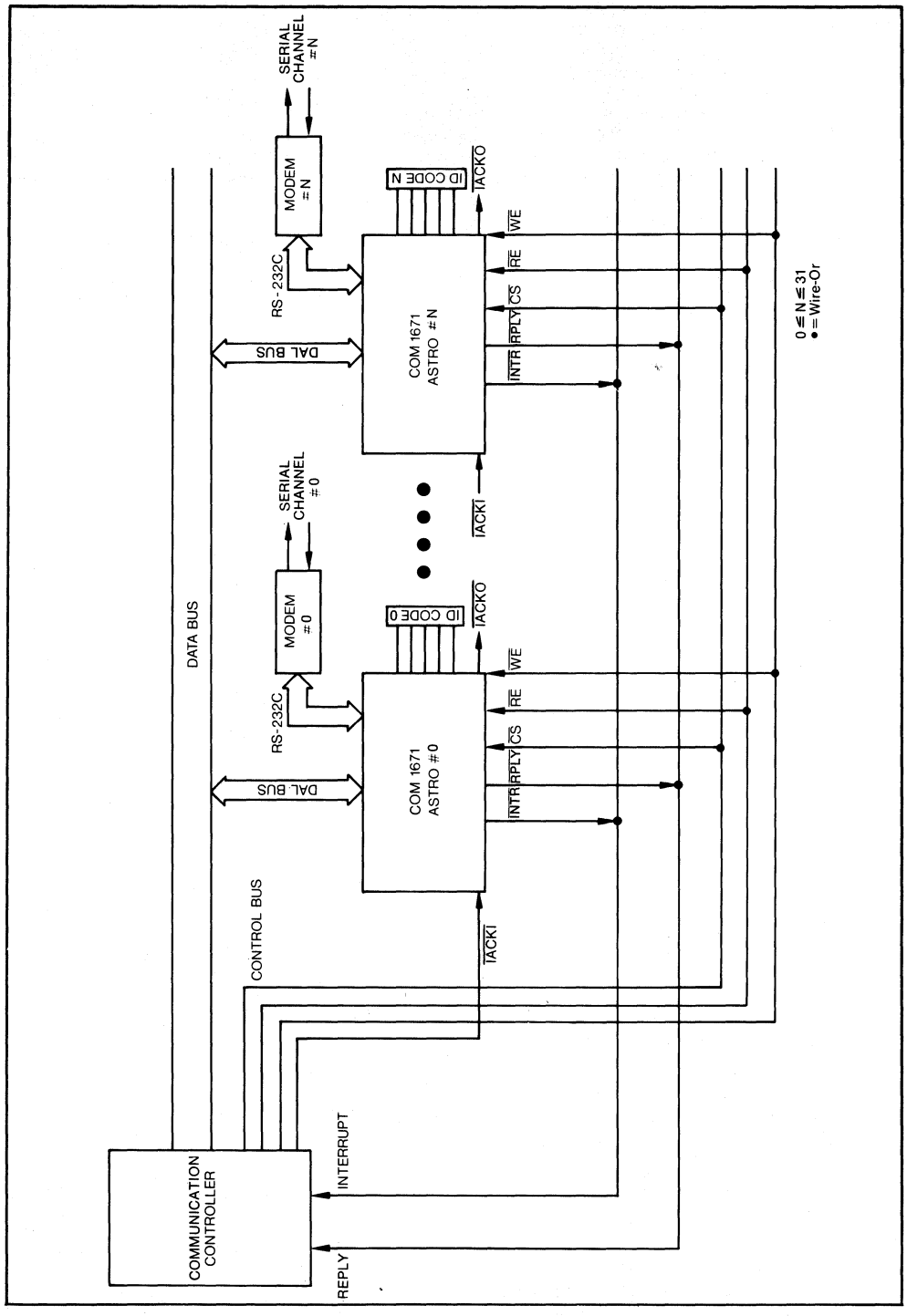
ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted)

Parameter		Min	Typ.	Max.	Unit	Comments
D.C. Characteristics						
INPUT VOLTAGE LEVELS						
Low Level, V_{IL}				0.8	V	
High Level, V_{IH}		2.4			V	
OUTPUT VOLTAGE LEVELS						
Low Level, V_{OL}			0.4		V	I_{OL} = 1.6ma
High Level, V_{OH}		2.4				I_{OH} = 100 μa
INPUT LEAKAGE						
Data Bus			5.0	10.0	μa	0 ≤ V_{IN} ≤ 5 v
All others			5.0	10.0	μa	V_{IN} = +12v
POWER SUPPLY CURRENT						
I_{CC}				80.0	ma	
I_{DD}				10.0	ma	
I_{BB}				1.0	ma	
A.C. Characteristics						T_A = 25°C
CLOCK-RCP, TCP						
frequency			1.0		MHz	
DAL Bus						
T_{AS}	Address Set-Up Time	0			ns	
T_{AH}	Address Hold Time	150			ns	
T_{ARL}	Address to $\overline{RPLY}$ Delay			400	ns	
T_{CS}	$\overline{CS}$ Width	250			ns	
T_{CSRLF}	$\overline{CS}$ to Reply OFF Relay	0		250	ns	R_L = 2.7 KΩ
Read						
T_{ARE}	Address and $\overline{RE}$ Spacing	250			ns	
T_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{RED}	$\overline{RE}$ to Data Out Delay			180	ns	C_L = 20 pf
Write						
T_{AWE}	Address to $\overline{WE}$ Spacing	250			ns	
T_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	20			ns	
T_{WE}	$\overline{WE}$ Width	200		1000	ns	
T_{DS}	Data Set-Up Time	150			ns	
T_{DH}	Data Hold Time	100			ns	
T_{WECS}	$\overline{WE}$ to $\overline{CS}$ Spacing	250			ns	
Interrupt						
T_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	0			ns	
T_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	250			ns	
T_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{PI}	$\overline{IACKI}$ Pulse Width	200			ns	
T_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay			250	ns	See Note 1.
T_{RED}	$\overline{RE}$ OFF to $\overline{DAL}$ Open Delay			180	ns	
T_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay			250	ns	See Note 1.
T_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay			200	ns	
T_{REI}	$\overline{RE}$ OFF to $\overline{IACKO}$ OFF Delay			250	ns	

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.

Multiple ASTRO System in Daisy-Chain Configuration



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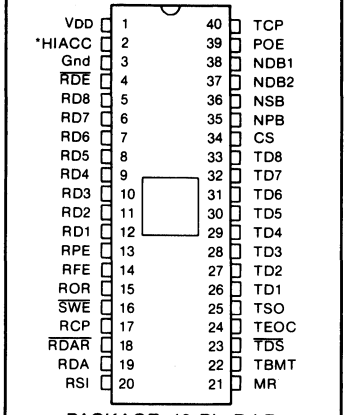
COM 1863
COM 8018
μPC FAMILY

Universal Asynchronous Receiver/Transmitter
UART

FEATURES

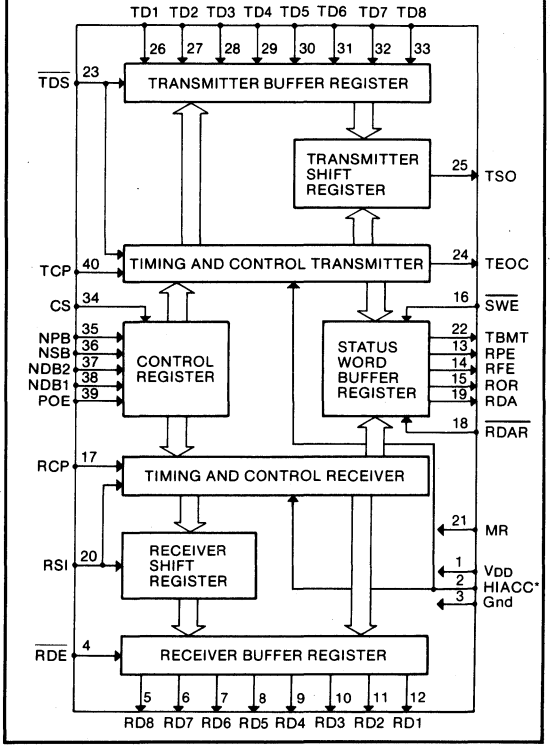
- ☐ Compatible with TR1863 timing
- ☐ High accuracy 32X clock mode: 48.4375% Receiver Distortion Immunity and improved RDA/ROR operation
- ☐ High Speed Operation—62.5K baud, 200ns strobes
- ☐ Single +5V Power Supply
- ☐ Direct TTL Compatibility—no interfacing circuits required
- ☐ Input pull-up options: COM 8018 has low current pull-up resistors; COM 1863 has no pull up resistors
- ☐ Full or Half Duplex Operation—can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered—eliminates need for precise external timing
- ☐ Improved Start Bit Verification—decreases error rate
- ☐ 46.875% Receiver Distortion Immunity
- ☐ Fully Programmable—data word length; parity mode; number of stop bits: one, one and one-half, or two
- ☐ Master Reset—Resets all status outputs and Receiver Buffer Register
- ☐ Three State Outputs—bus structure oriented
- ☐ Low Power—minimum power requirements
- ☐ Input Protected—eliminates handling problems
- ☐ Ceramic or Plastic DIP Package—easy board insertion
- ☐ Baud Rates available from SMC's COM 8046, COM 8116, COM 8126, COM 8136, COM 8146 baud rate generators

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's patented COPLAMOS® technology and employs depletion mode loads, allowing operation from a single +5V supply. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7, or 8 data bits, odd/even or no parity, and 1 or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

*If pin 2 is taken to a logic 1 the COM 1863 or the COM 8018 will operate in a high accuracy mode. If pin 2 is connected to -12V, GND, a valid logic zero, or left unconnected, the high accuracy feature is disabled, and the UART will operate in a 16X clock mode.

DESCRIPTION OF OPERATION—TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 or 32 times the desired baud rate is applied, and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

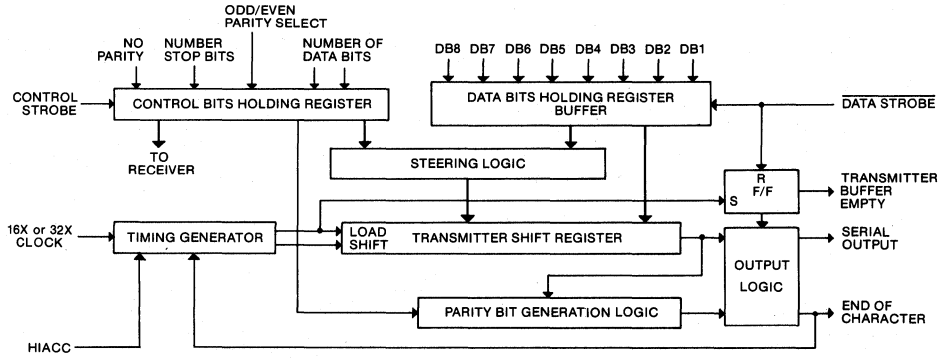
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the data strobe ($\overline{TDS}$) has been pulsed, the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the $\overline{TBMT}$ signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TEOC goes low, TSO goes low (the start bit), and TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

TRANSMITTER BLOCK DIAGRAM



DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 or 32 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

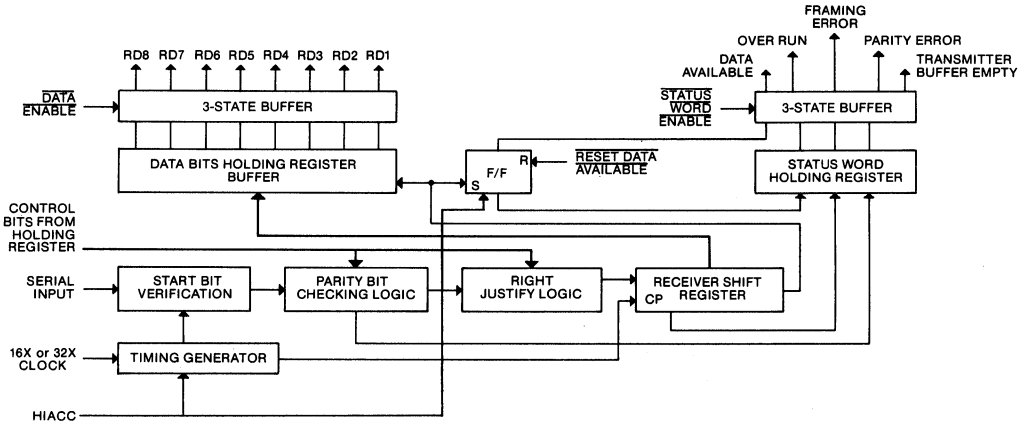
Data reception begins when the serial input line transitions for mark (high) to space (low). If the RSI line remains spacing for 15/32 to 17/32 bit times (in the 16X mode, HIACC = 0) or 31/64 to 33/64 bit times (in the 32X mode, HIACC = 1), a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

If the received parity bit is incorrect, the parity error flip-flop of the status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, the framing error flip-flop is set high, indicating a framing error.

On the negative RCP edge preceding the stop-bit center sample, internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high, or the $\overline{RDAR}$ signal is low, the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

Subsequently the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

RECEIVER BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{DD}	Power Supply	+5 volt Supply
2	HIACC	High Accuracy Mode	Enables 32X clock and improved RDA/ROR operation. See NOTE on high accuracy mode.
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.
5-12	RD8-RD1	Receiver Data Outputs	These are the eight 3-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.

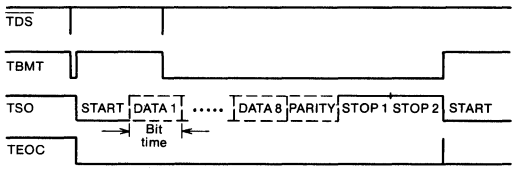
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
15	ROR	Receiver Over Run	This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output reset not completed) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) or 32 times (32X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level. $\overline{RDAR}$ must have gone low and come high again before ROR is sampled to avoid overrun indication.
19	RDA	Receiver Data Available	This 3-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE, ROR and RD1-RD8 to a low-level.
22	TBMT	Transmitter Buffer Empty	This 3-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character	This output appears as a high-level during the last half clock cycle of the last stop bit. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted: the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.

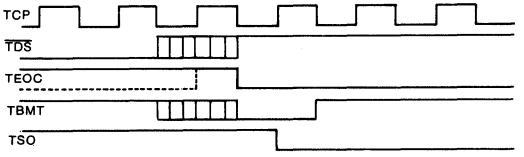
DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of two stop bits when programming a 5 data bit word generates 1.5 stop bits.
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) or 32 times (32X) the desired transmitter baud rate.

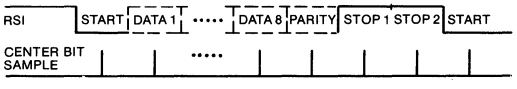
TRANSMITTER TIMING— 8 BIT, PARITY, 2 STOP BITS



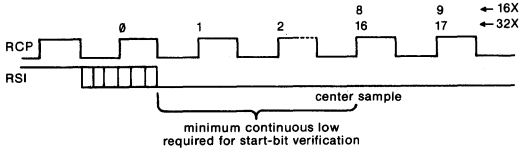
TRANSMITTER START-UP



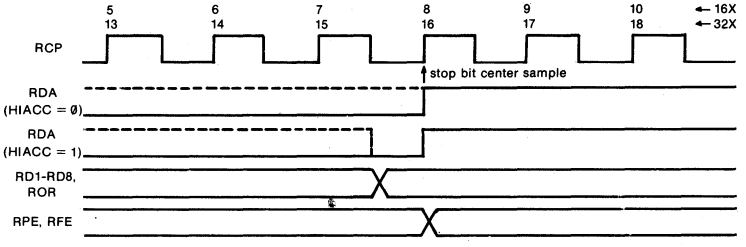
RECEIVER TIMING— 8 BIT, PARITY, 2 STOP BITS



START BIT DETECT AND VERIFY



RECEIVER TIMING DETAIL



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin (except Pin 2), with respect to ground	−0.3V
Negative Voltage on Pin 2, with respect to ground	−13.2V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that at clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{DD} = +5V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	$I_{OL} = 1.6mA$
High-level, V_{OH}	2.4			V	$I_{OH} = -100\mu A$
INPUT CURRENT					
Low-level, I_{IL}			300	μA	V_{IN} = GND, COM 8018 only
INPUT LEAKAGE			±10	μA	COM 1863 only
OUTPUT CURRENT					
Leakage, I_{LO}			±10	μA	$\overline{SWE} = \overline{RDE} = V_{IH}$, $0 \leq V_{OUT} \leq +5V$
Short circuit, I_{OS}**			40	mA	$V_{OUT} = 0V$
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	$\overline{SWE} = \overline{RDE} = V_{IH}$
POWER SUPPLY CURRENT					
I_{CC}			25	mA	All outputs = V_{OH}, All inputs = V_{DD}
A.C. CHARACTERISTICS					$T_A = +25°C$, See Timing Diagrams
CLOCK FREQUENCY	DC		1.0	MHz	RCP, TCP
PULSE WIDTH					
Clock	0.45			μs	RCP, TCP
Master reset	500			ns	MR
Control strobe	200			ns	$\overline{CS}$
Transmitter data strobe	200			ns	$\overline{TDS}$
Receiver data available reset	200			ns	$\overline{RDAR}$
INPUT SET-UP TIME					
Data bits	0			ns	TD1-TD8
Control bits	0			ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	0			ns	TD1-TD8
Control bits	0			ns	NPB, NSB, NDB2, NDB1, POE
ENABLE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable			250	ns	$\overline{RDE}$: T_{PD1}, T_{PD0}
Status word enable			250	ns	$\overline{SWE}$: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY			250	ns	$\overline{RDE}$, $\overline{SWE}$

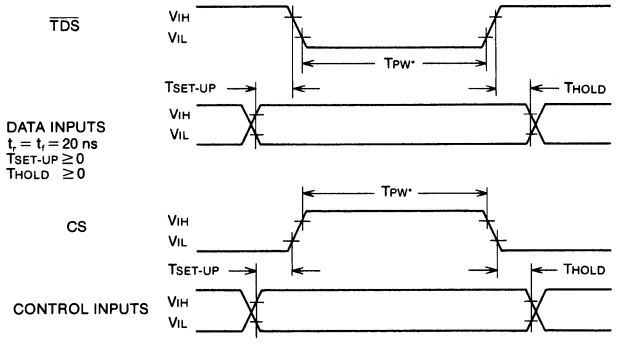
**Not more than one output should be shorted at a time.

NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within 1½ clock period (TCP) after the trailing edge of $\overline{TDS}$.

2. The start bit (mark to space transition) will always be detected within one RCP clock period, guaranteeing a maximum start bit slippage of ±1/32 or ±1/64 of a bit time.

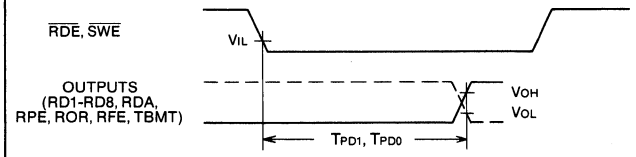
3. The 3-state output has 3 states: 1) low impedance to V_{DD} 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

DATA/CONTROL TIMING DIAGRAM



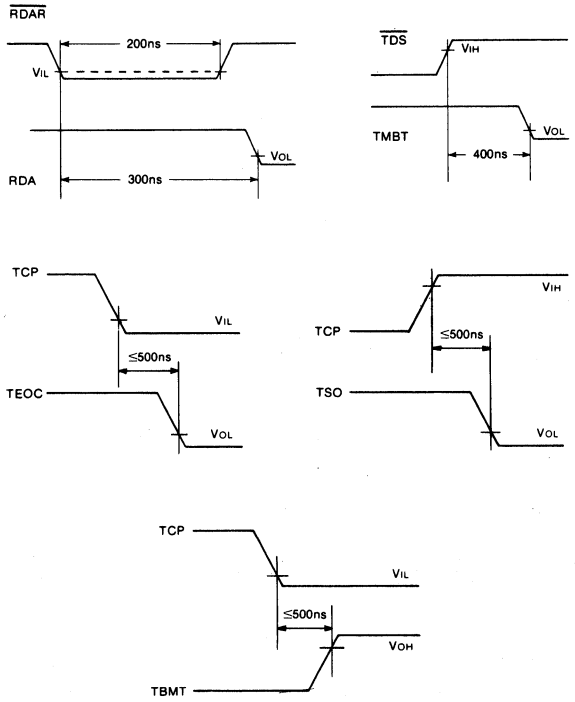
*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

OUTPUT TIMING DIAGRAM



NOTE: Waveform drawings not to scale for clarity.

ADDITIONAL TIMING INFORMATION



NOTES ON COM 8018 AND COM 1863 HIGH-ACCURACY AND IMPROVED RDA/ROR MODE

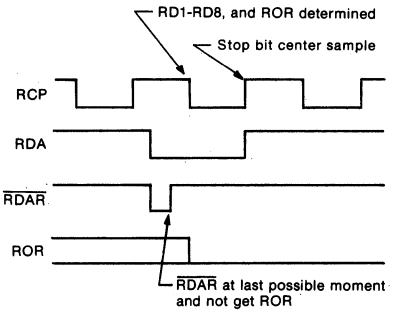
The HIACC mode is enabled by applying a logic "one" to pin 2. If this pin is left unconnected, or connected to GND, −12V, or a logic "zero," the HIACC mode is disabled. The HIACC input has an internal pull-down resistor.

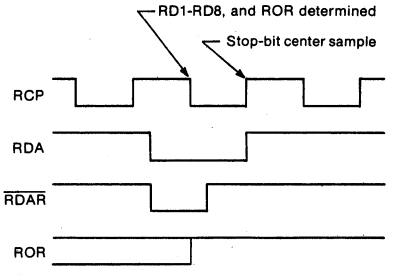
When the HIACC mode is selected, the TX and RX halves both operate on 32X instead of 16X clocks. Also, RDA is notched during the one half receiver clock cycle preceding the stop bit center sample when RD1-RD8 and ROR are changing.

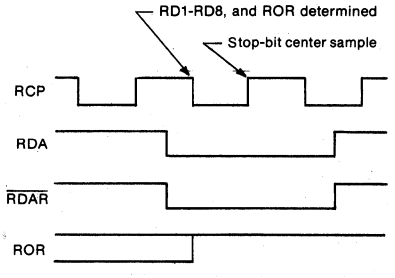
Whether or not the HIACC mode is selected, RDA must be low and RDAR must have returned high to avoid setting ROR. If RDAR is held low past the stop-bit center sample, RDA will go high after RDAR returns high.

The maximum current HIACC will supply if connected to −13.2V is 3.5mA.

IMPROVED RDA/ROR OPERATION TIMING DIAGRAMS



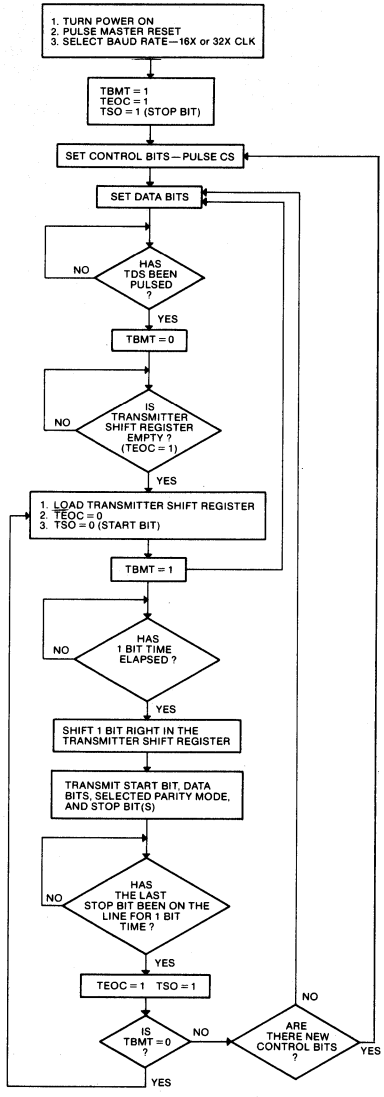




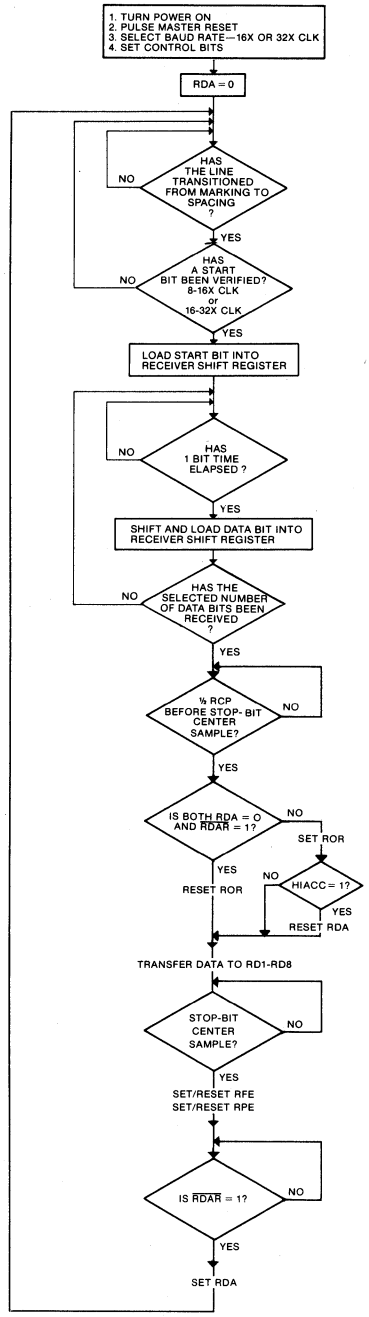
Protection against missing the ROR flag

SECTION III

FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



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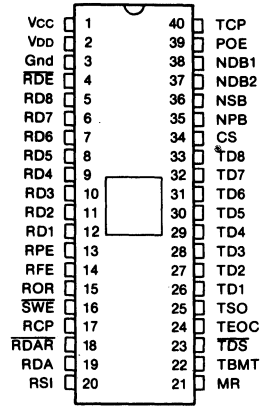
COM2502
COM2017
COM2502/H
COM2017/H

Universal Asynchronous Receiver/Transmitter UART

Pin Configuration

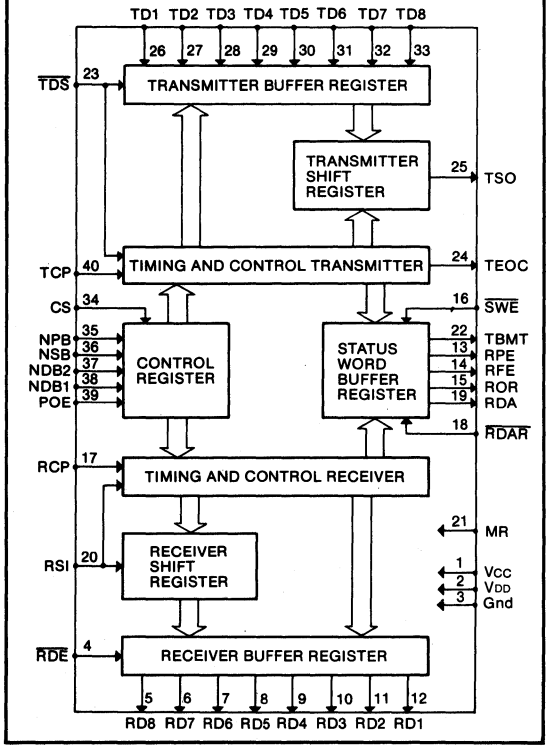


PACKAGE: 40-Pin D.I.P.

FEATURES

- ☐ Direct TTL Compatibility — no interfacing circuits required
- ☐ Full or Half Duplex Operation — can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered — eliminates need for precise external timing
- ☐ Start Bit Verification — decreases error rate
- ☐ Fully Programmable — data word length, parity mode, number of stop bits; one, one and one-half, or two
- ☐ High Speed Operation — 40K baud, 200ns strobes
- ☐ Master Reset — Resets all status outputs
- ☐ Tri-State Outputs — bus structure oriented
- ☐ Low Power — minimum power requirements
- ☐ Input Protected — eliminates handling problems
- ☐ Ceramic or Plastic Dip Package — easy board insertion

Functional Block Diagram



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolothic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7 or 8 data bits, odd/even or no parity, and 1, or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code from the COM 2017 or COM 2017/H. The UART can operate in either the full or half duplex mode. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

DESCRIPTION OF OPERATION— TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

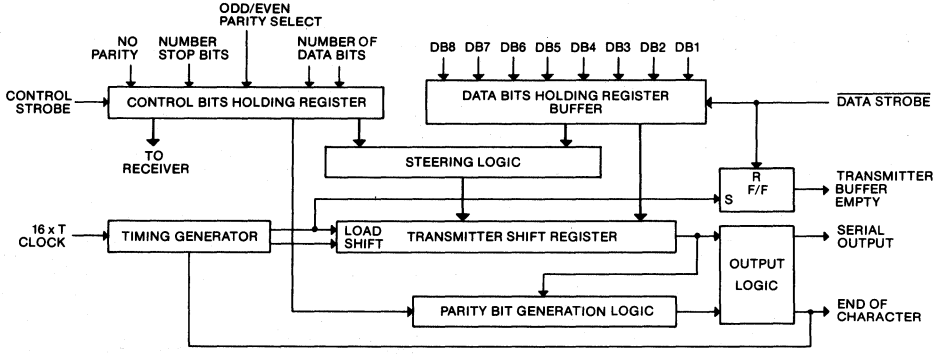
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the date strobe ($\overline{TDS}$) has been pulsed the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the TBMT signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TSO goes low (the start bit), TEOC goes low, the TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

TRANSMITTER BLOCK DIAGRAM



DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions from mark (high) to space (low). If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

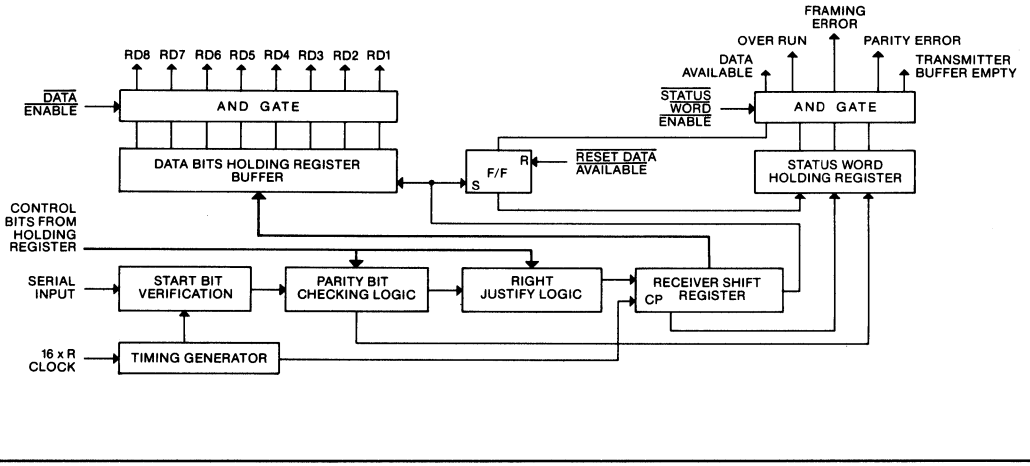
If the transmitted parity bit does not agree with the received parity bit, the parity error flip-flop of the

status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, due to an improperly framed character, the framing error flip-flop is set high, indicating a framing error.

Once a full character has been received internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

At this time the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

RECEIVER BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{CC}	Power Supply	+5 volt Supply
2	V_{DD}	Power Supply	−12 volt Supply
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.
5-12	RD8-RD1	Receiver Data Outputs	These are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.

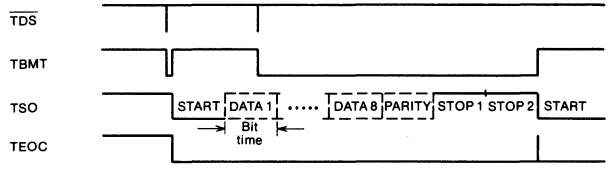
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
15	ROR	Receiver Over Run	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level.
19	RDA	Receiver Data Available	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level.
22	TBMT	Transmitter Buffer Empty	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character	This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.

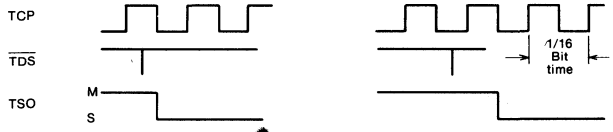
DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of 2 stop bits when programming a 5 data bit word generates 1.5 stop bits from the COM 2017 or COM 2017/H.
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

TRANSMITTER TIMING—8 BIT, PARITY, 2 STOP BITS

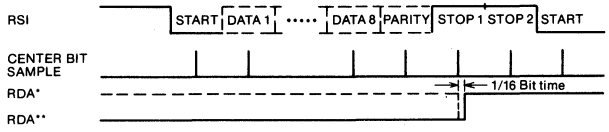


TRANSMITTER START-UP



Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of $\overline{TDS}$.

RECEIVER TIMING—8 BIT, PARITY, 2 STOP BITS



*The RDA line was previously not reset (ROR = high-level).
**The RDA line was previously reset (ROR = low-level).

START BIT DETECT/VERIFY

If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° C to +70° C
Storage Temperature Range ..... −55° C to +150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = +5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = 100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 4
OUTPUT CURRENT					
Leakage, I_{LO}			−1	μA	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}, 0 ≤ V_{OUT} ≤ +5V
Short circuit, Ios**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}, All inputs = V_{CC}
I_{DD}			28	mA	
A.C. CHARACTERISTICS					T_A = +25° C
CLOCK FREQUENCY					
(COM2502, COM2017)	DC		400	KHz	RCP, TCP
(COM2502H, COM2017H)	DC		640	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			μs	RCP, TCP
Master reset	500			ns	MR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	$\overline{TDS}$
Receiver data available reset	200			ns	$\overline{RDAR}$
INPUT SET-UP TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable			350	ns	$\overline{RDE}$: T_{PD1}, T_{PD0}
Status word enable			350	ns	$\overline{SWE}$: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY			350	ns	$\overline{RDE}$, $\overline{SWE}$

**Not more than one output should be shorted at a time.

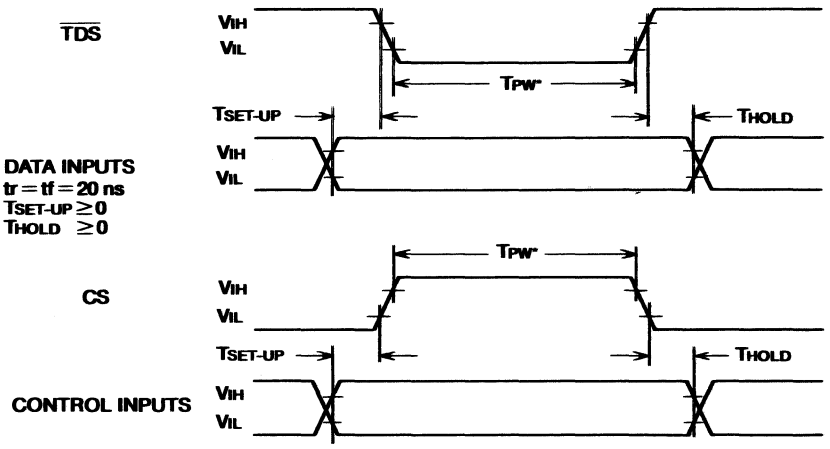
NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within one clock period (TCP) after the trailing edge of $\overline{TDS}$.

2. The start bit (mark to space transition) will always be detected within one clock period of RCP, guaranteeing a maximum start bit slippage of 1/16th of a bit time.

3. The tri-state output has 3 states: 1) low impedance to V_{CC} 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms. The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

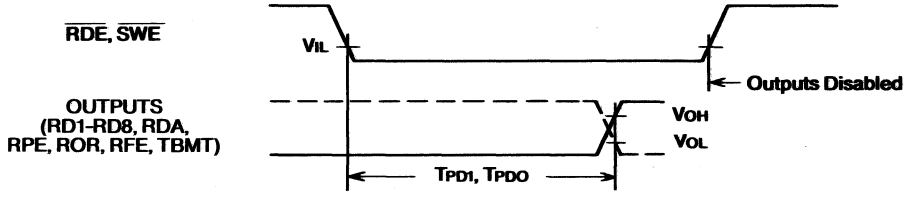
4. Under steady state conditions no current flows for TTL or MOS interfacing. (COM 2502 or COM 2502/H)

DATA/CONTROL TIMING DIAGRAM

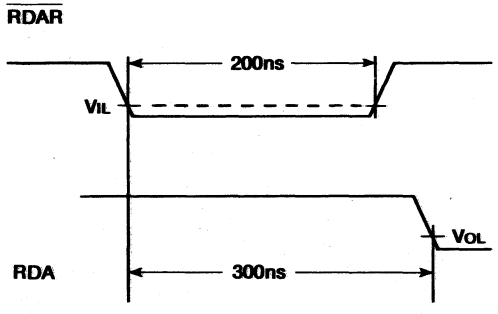


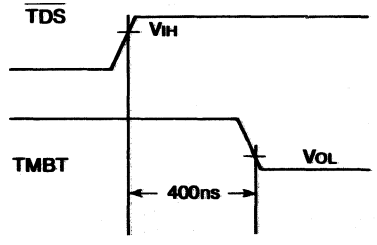
*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

OUTPUT TIMING DIAGRAM

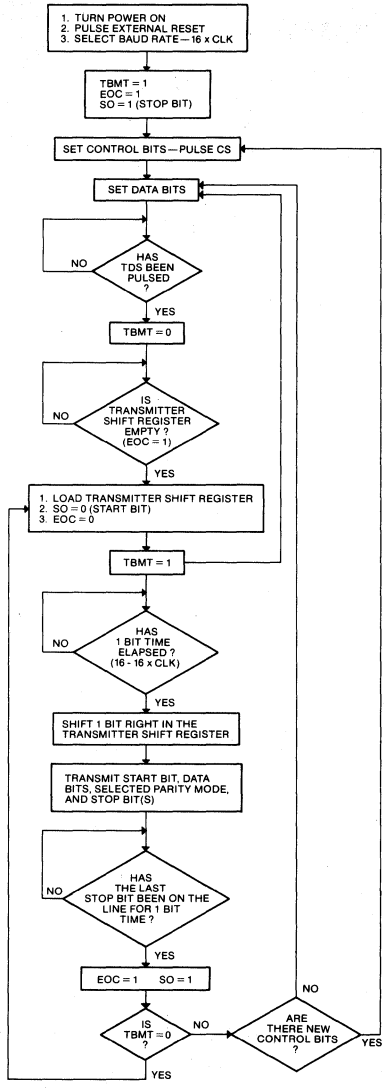


NOTE: Waveform drawings not to scale for clarity.

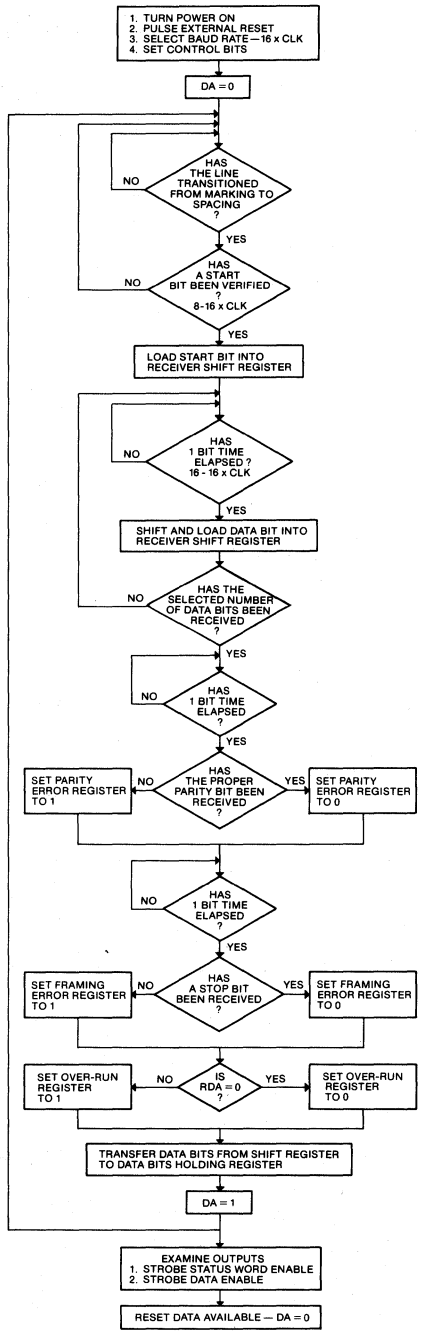




FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11787
(516) 273-3100 · TWX-510-227-8898

Universal Synchronous Receiver/Transmitter USRT

FEATURES

- ☐ STR, BSC — Bi-sync and interleaved bi-sync modes of operation
- ☐ Fully Programmable — data word length, parity mode, receiver sync character, transmitter sync character
- ☐ Full or Half Duplex Operation — can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered — eliminates need for precise external timing
- ☐ Directly TTL Compatible — no interface components required
- ☐ Tri-State Data Outputs — bus structure oriented
- ☐ IBM Compatible — internally generated SCR and SCT signals
- ☐ High Speed Operation — 250K baud, 200ns strobes
- ☐ Low Power — 300mW
- ☐ Input Protected — eliminates handling problems
- ☐ Dip Package — easy board insertion

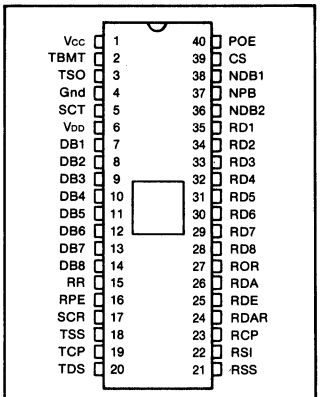
APPLICATIONS

- ☐ Bi-Sync Communications
- ☐ Cassette I/O
- ☐ Floppy Disk I/O

GENERAL DESCRIPTION

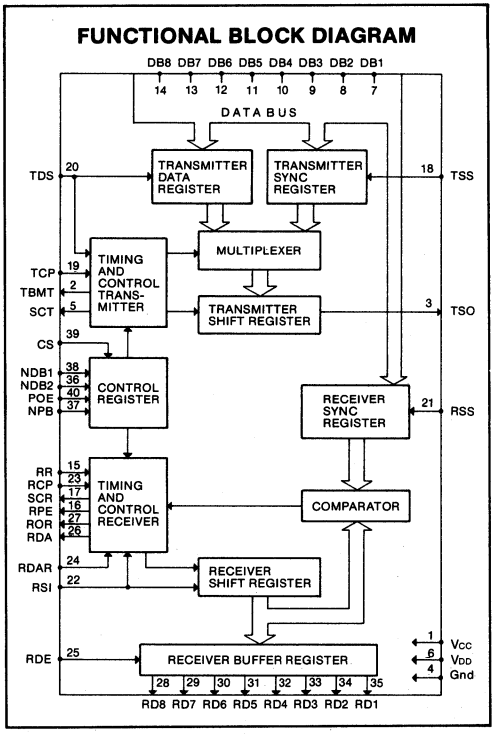
The Universal Synchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with synchronous (STR, BSC, Bi-sync, and interleaved bi-sync) data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology, allowing all inputs and outputs to be directly TTL compatible. The duplex mode, baud rate, data word length, parity mode, receiver sync character, and transmitter sync character are independently programmable through the use of external controls. The USR/T is fully double buffered and internally generates the sync character received and sync character transmitted signals. These programmable features provide the user with the ability to interface with all synchronous peripherals.

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{CC}	Power Supply	+5 volt Supply
2	TBMT	Transmitter Buffer Empty	This output is at a high-level when the transmitter data buffer register may be loaded with new data.
3	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. This character is extracted from the transmitter data buffer register provided that a TDS pulse occurs during the presently transmitted character. If TDS is not pulsed, the next transmitted character will be extracted from the transmitter sync register.
4	GND	Ground	Ground
5	SCT	Sync Character Transmitted	This output is set high when the character loaded into the transmitter shift register is extracted from the transmitter sync register, indicating that the TDS was not pulsed during the previously transmitted character. This output is reset low when the character to be transmitted is extracted from the transmitter data buffer register. This can only occur if TDS is pulsed.
6	V_{DD}	Power Supply	−12 volt Supply
7-14	DB1-DB8	Data Bus Inputs	This 8 bit bus inputs information into the receiver sync register under control of the RSS strobe, into the transmitter sync register under control of the TSS strobe, and into the transmitter data buffer register under control of the TDS strobe. The strobes operate independently of each other. Unused bus inputs may be in either logic state. The LSB should always be placed on DB1.
15	RR	Receiver Reset	This input should be pulsed to a high-level after power turn-on. This resets the RDA, SCR, ROR, and RPE outputs to a low-level. The transition of the RR input from a high-level to a low-level sets the receiver into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the SCR output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register.
16	RPE	Receiver Parity Error	This output is a high-level if the received character parity bit does not agree with the selected parity.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
17	SCR	Sync Character Received	This output is set high each time the character loaded into the receiver buffer register is identical to the character in the receiver sync register. This output is reset low the next time the receiver buffer register is loaded with a character which is not a sync character.
18	TSS	Transmitter Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter sync register.
19	TCP	Transmitter Clock	The positive going edge of this clock shifts data out of the transmitter shift register, at a baud rate equal to the TCP clock frequency.
20	TDS	Transmitter Data Buffer Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter data buffer register.
21	RSS	Receiver Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the receiver sync register.
22	RSI	Receiver Serial Input	This input accepts the serial bit input stream.
23	RCP	Receiver Clock	The negative-going edge of this clock shifts data into the receiver shift register, at a baud rate equal to the RCP clock frequency.
24	RDAR	Receiver Data Available Reset	A high-level input resets the RDA output to a low-level.
25	RDE	Received Data Enable	A high-level input enables the outputs (RD8-RD1) of the receiver buffer register
26	RDA	Receiver Data Available	This output is at a high-level when an entire character has been received and transferred into the receiver buffer register.
27	ROR	Receiver Over-Run	This output is at a high-level if the previously received character is not read (RDA not reset) before the present character is transferred into the receiver buffer register.
28-35	RD8-RD1	Receiver Data Output	These are the 8 tri-state data outputs enabled by RDE. Unused data output lines, as selected by NDB1 and NDB2, have a low level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
36, 38	NDB2, NDB1	Number of Data Bits	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8

DESCRIPTION OF PIN FUNCTIONS

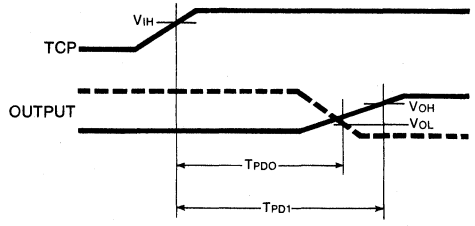
PIN NO.	SYMBOL	NAME	FUNCTION
37	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted. In addition, it is necessary that the received character contain no parity bit. Also, the RPE output is forced to a low-level. See pin 40, POE.
39	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, POE, and NPB) into the control bits register. This line may be strobed or hard wired to a high-level.
40	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the reciever and transmitter, as per the following table:

NPB	POE	MODE
L	L	odd parity
L	H	even parity
H	X	no parity

X = don't care

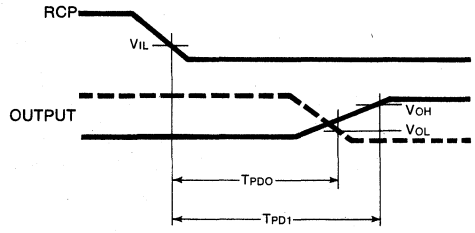
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

Transmitter

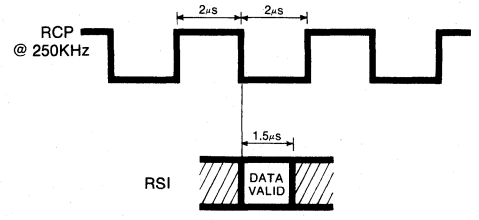


OUTPUT	TPDO	TPD1	UNITS
TBMT	NA	2.0	μs
SCT	1.0	1.5	μs
TSO	1.0	1.0	μs

Receiver



OUTPUT	TPDO	TPD1	UNITS
RDA	NA	1.0	μs
ROR	2.0	2.5	μs
RPE	2.0	2.5	μs
SCR	2.0	2.5	μs
RD1-RD8	2.5	2.5	μs



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° C to +70° C
Storage Temperature Range ..... −55° C to +150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = +5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = −100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 1
OUTPUT CURRENT					
Leakage, I_{LO}			−1	μA	RDE = V_{IL}, O ≤ V_{OUT} ≤ +5V
Short circuit, Ios**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	R_{DE} = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}
I_{DD}			28	mA	All outputs = V_{OH}
A.C. CHARACTERISTICS					T_A = +25° C
CLOCK FREQUENCY	DC		250	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			μs	RCP, TCP
Receiver reset	1			μs	RR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	TDS
Transmitter sync strobe	200			ns	TSS
Receiver sync strobe	200			ns	RSS
Receiver data available reset	200			ns	RDAR
INPUT SET-UP TIME					
Data bits	>0			ns	DB1-DB8
Control bits	>0			ns	NPB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	>0			ns	DB1-DB8
Control bits	>0			ns	NPB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

**Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing. A switching current of 1.6 mA maximum flows during a transition of the input.
2. The three-state output has 3 states:
   1) low impedance to V_{CC}
   2) low impedance to GND
   3) high impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.

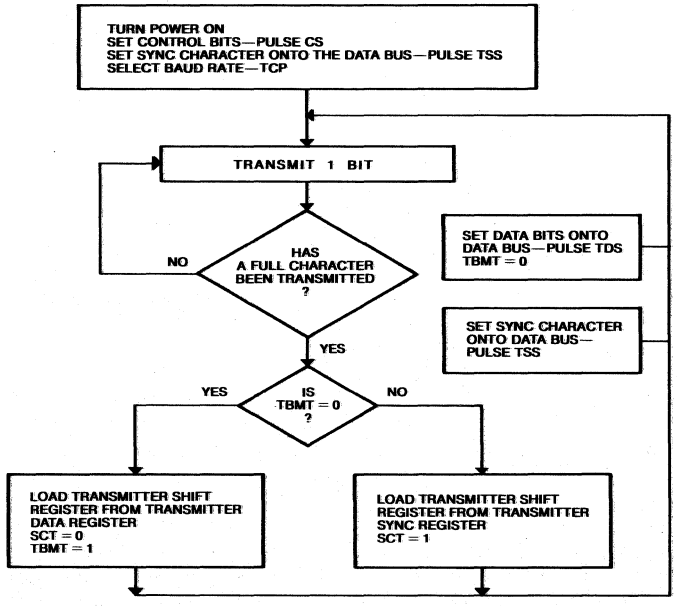
DESCRIPTION OF OPERATION—RECEIVER/TRANSMITTER

The input clock frequency for the receiver is set at the desired receiver baud rate and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the Receiver Reset input transitions from a high-level to a low-level the receiver is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the Sync Character Received output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. The receiver provides flags for Receiver Data Available, Receiver Over Run, Receiver Parity Error, and Sync Character Received. Full double buffering eliminates the need for precise external timing by allowing one full character time for received data to be read out.

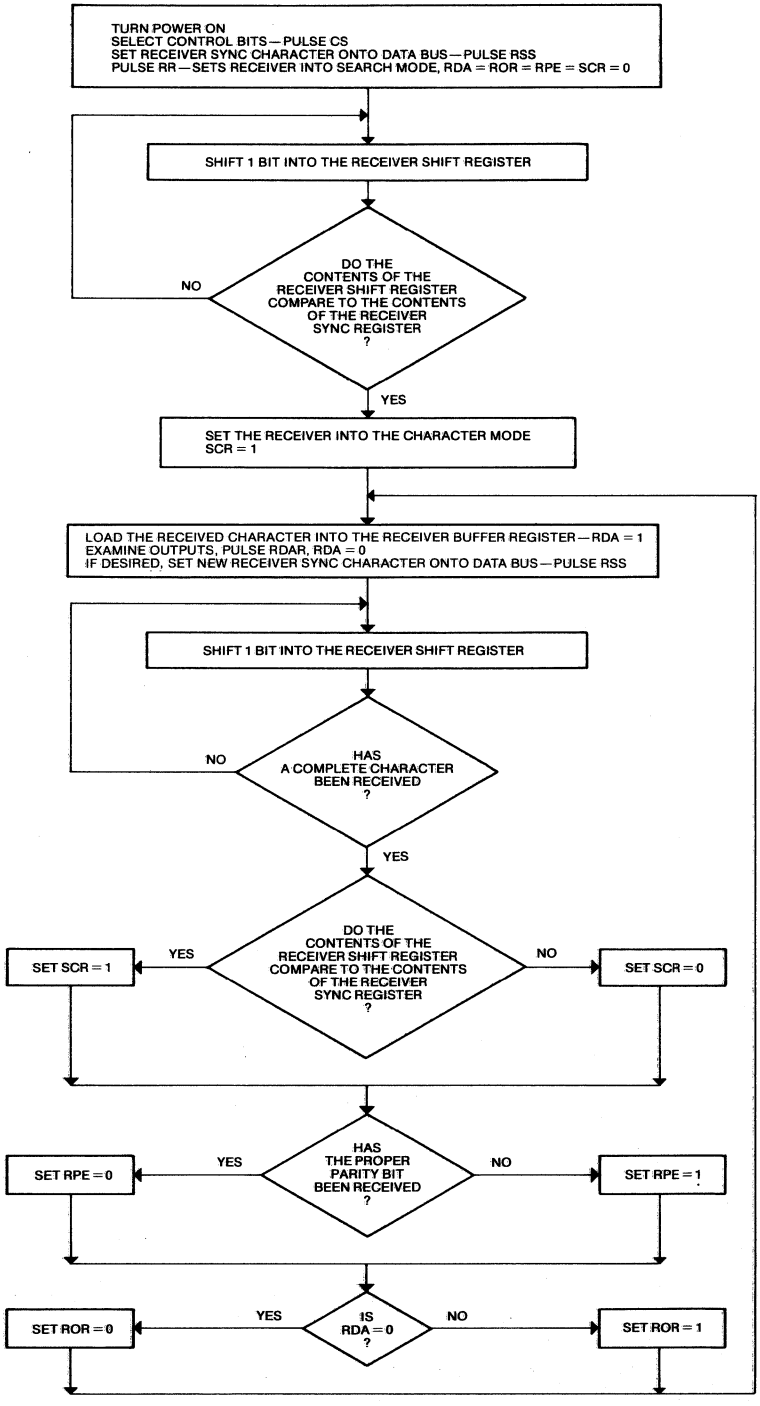
The input clock frequency for the transmitter is set at the desired baud rate and the desired transmitter sync character is loaded into the transmitter sync register. Internal logic decides if the character to be transmitted out of the transmitter shift register is extracted from the transmitter data register or the transmitter sync register. The next character transmitted is extracted from the transmitter data register provided that a Transmitter Data Strobe pulse occurs during the presently transmitted character. If the Transmitter Data Strobe is not pulsed, the next transmitted character is extracted from the transmitter sync register and the Sync Character Transmitted output is set to a high level. Full double buffering eliminates the need for precise external timing by allowing one full character time to load the next character to be transmitted.

There may be 5, 6, 7, or 8 data bits and odd/even or no parity bit. All inputs and outputs are directly TTL compatible. Tri-state data output levels are provided for the bus structure oriented signals. Input strobe widths of 200ns, output propagation delays of 250ns, and receiver/transmitter rates of 250K baud are achieved.

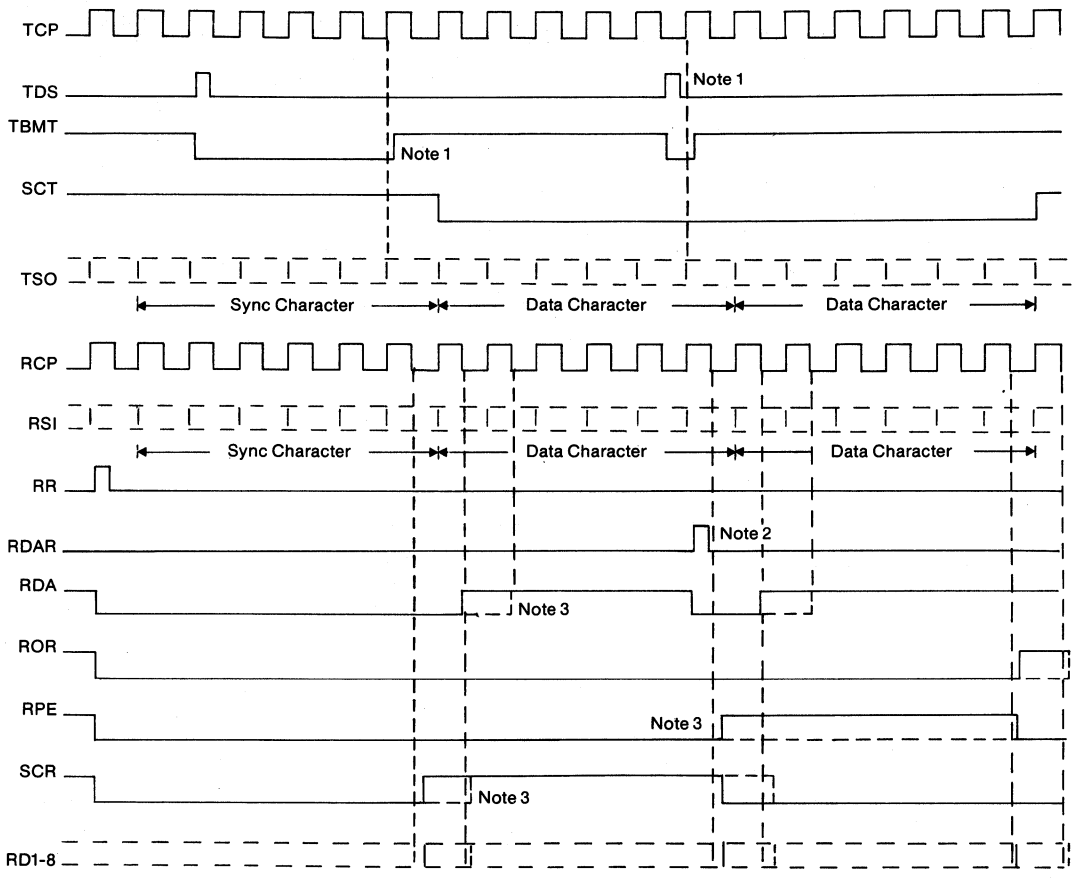
FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



USRT TIMING DIAGRAM



NOTE 1
The transmitter shift register is loaded with the next character at the positive clock transition corresponding to the leading edge of the last bit of the current character on the TSO output. TBMT is set high approximately two microseconds after this clock transition. If it is desired that the next character be extracted from the transmitter data register the leading edge of the TDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an ROR indication the leading edge of the RDAR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input.

NOTE 3
The ROR, RPE, SCR and RD1-RD8 outputs are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input. The RDA output is set high at the next negative clock transition.

The solid waveforms correspond to a control register setting of 5 data bits and a parity bit. The dashed waveforms are for a setting of 6 data bits and no parity bit.

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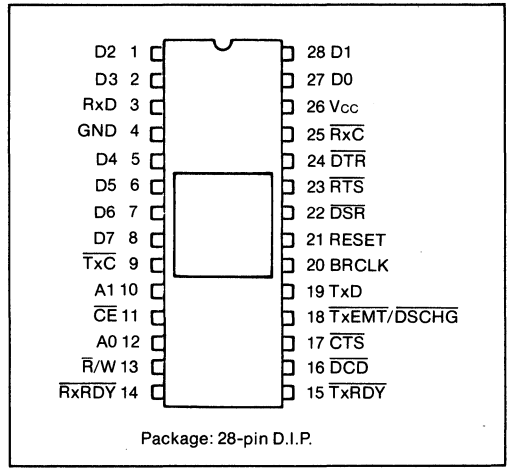
COM 2651* COM 2651-1* COM 2651-2*
μPC FAMILY

Programmable Communication Interface PCI

FEATURES

- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —Selectable 1 or 2 SYNC Characters
  - —Internal Character Synchronization
  - —Transparent or Non-Transparent Mode
  - —Automatic SYNC or DLE-SYNC Insertion
  - —SYNC or DLE Stripping
  - —Odd, Even, or No Parity
  - —Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - —Line Break Detection and Generation
  - —1, 1½, or 2-Stop Bit Detection and Generation
  - —False Start Bit Detection
  - —Odd, Even, or No Parity
  - —Parity, Overrun, and framing error detect
  - —Local or remote maintenance loop back mode
  - —Automatic serial echo mode
- ☐ Baud Rates
  - —DC to 1.0M Baud (Synchronous)
  - —DC to 1.0M Baud (1X, Asynchronous)
  - —DC to 62.5K Baud (16X, Asynchronous)
  - —DC to 15.625K Baud (64X, Asynchronous)
- ☐ Double Buffering of Data

PIN CONFIGURATION



Package: 28-pin D.I.P.

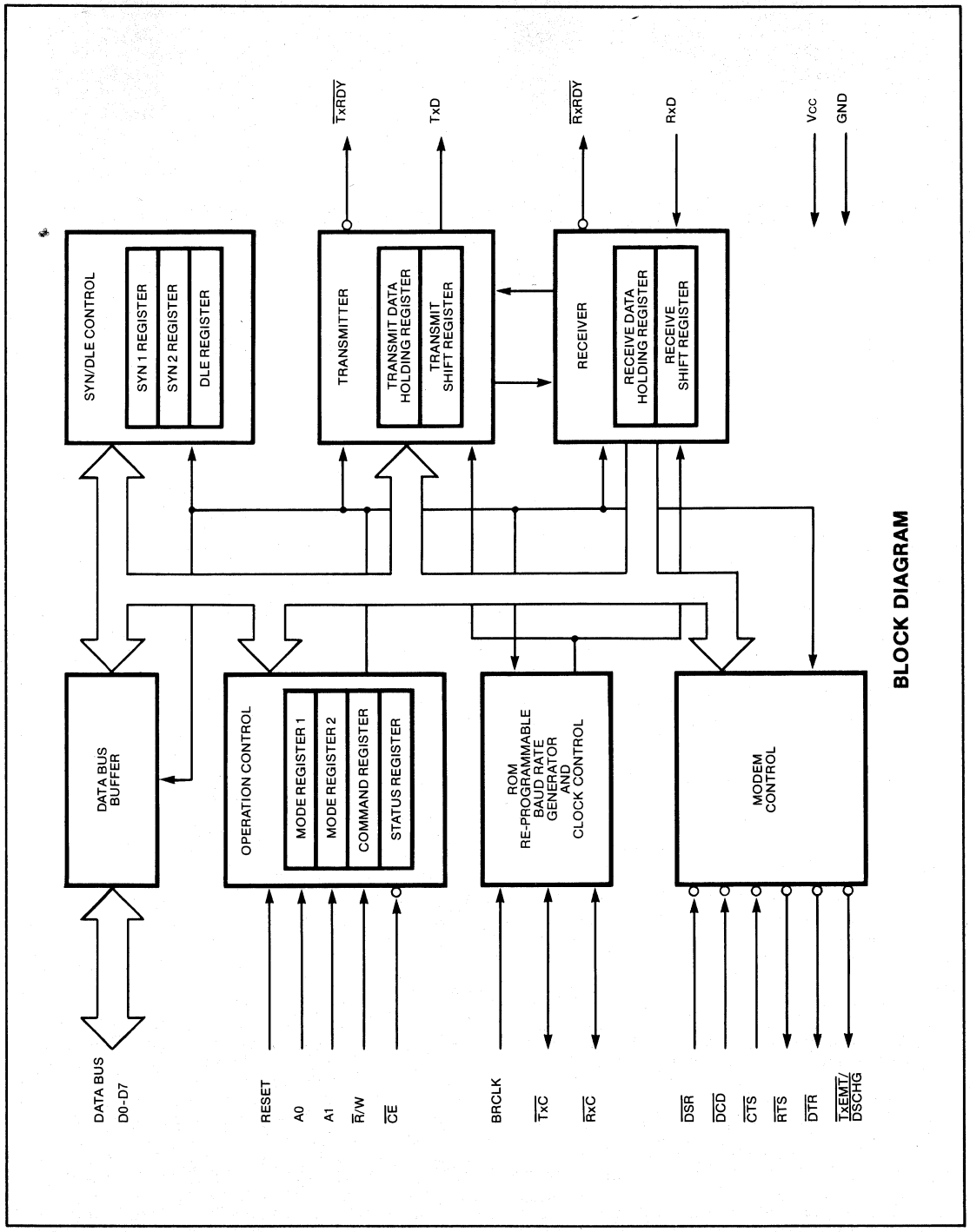
- ☐ Internal or External Baud Rate Clock
  - —16 Internal Rates:50 to 19,200 Baud, or 45.5 to 38,400 for COM 2651-2
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required
- ☐ Compatible with 2651, INS2651

GENERAL DESCRIPTION

The COM 2651 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology that meets the majority of asynchronous and synchronous data communication requirements, by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. The on-chip baud rate generator can be ROM reprogrammed to accommodate different baud rates and different starting frequencies.

The COM 2651 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.

*FOR FUTURE RELEASE



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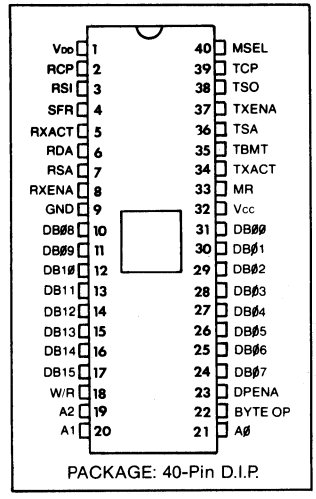
COM 5025
μPC FAMILY

Multi-Protocol Universal Synchronous Receiver/Transmitter
USYNR/T

FEATURES

- ☐ Selectable Protocol—Bit or Byte oriented
- ☐ Direct TTL Compatibility
- ☐ Three-state Input/Output BUS
- ☐ Processor Compatible—8 or 16 bit
- ☐ High Speed Operation—1.5 M Baud—typical
- ☐ Fully Double Buffered—Data, Status, and Control Registers
- ☐ Full or Half Duplex Operation—independent Transmitter and Receiver Clocks
  —individually selectable data length for Receiver and Transmitter
- ☐ Master Reset—resets all Data, Status, and Control Registers
- ☐ Maintenance Select—built-in self checking

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

BIT ORIENTED PROTOCOLS—SDLC, HDLC, ADCCP
- ☐ Automatic bit stuffing and stripping
- ☐ Automatic frame character detection and generation
- ☐ Valid message protection—a valid received message is protected from overrun
- ☐ Residue Handling—for messages which terminate with a partial data byte, the number of valid data bits is available

SELECTABLE OPTIONS:
- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —None
- ☐ Primary or Secondary Station Address Mode
- ☐ All Parties Address—APA
- ☐ Extendable Address Field—to any number of bytes
- ☐ Extendable Control Field—to 2 bytes
- ☐ Idle Mode—idle FLAG characters or MARK the line
- ☐ Point to Point, Multi-drop, or Loop Configuration

BYTE ORIENTED PROTOCOLS—BiSync, DDCMP
- ☐ Automatic detection and generation of SYNC characters

SELECTABLE OPTIONS:
- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Variable SYNC character—5, 6, 7, or 8 bits
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —VRC (odd/even parity)
  —None
- ☐ Strip Sync—deletion of leading SYNC characters after synchronization
- ☐ Idle Mode—idle SYNC characters or MARK the line

APPLICATIONS

- ☐ Intelligent Terminals
- ☐ Line Controllers
- ☐ Network Processors
- ☐ Front End Communications
- ☐ Remote Data Concentractors
- ☐ Communication Test Equipment
- ☐ Computer to Computer Links
- ☐ Hard Disk Data Handler

General Description

The COM 5025 is a COPLAMOS® n channel silicon gate MOS/LSI device that meets the majority of synchronous communications requirements, by interfacing parallel digital systems to synchronous serial data communication channels while requiring a minimum of controller overhead.

The COM 5025 is well suited for applications such as computer to modem interfaces, computer to computer serial links and in terminal applications. Since higher level decisions and responses are made or initiated by the controller, some degree of intelligence in each controller of the device is necessary.

Newly emerging protocols such as SDLC, HDLC, and ADCCP will be able to utilize the COM 5025 with a high degree of efficiency as zero insertion for transmission and zero deletion for reception are done automatically. These protocols will be referred to as Bit Oriented Protocols (BOP). Any differences between them will be discussed in their respective sections. Conventional synchronous protocols that are control character oriented such as BISYNC can also utilize this device. Control Character oriented protocols will be referred to as CCP protocols. Other types of protocols that operate on a byte or character count basis can also utilize the COM 5025 with a high degree of efficiency in most cases. These protocols, such as DDCMP will also be referred to as CCP protocols.

The COM 5025 is designed to operate in a synchronous communications system where some external source is expected to provide the necessary received serial data, and all clock signals properly synchronized according to EIA standard RS334. The external controller of the chip will provide the necessary control signals, intelligence in interpreting control signals from the device and data to be transmitted in accord with RS334.

The receiver and transmitter are as symmetrical as possible without loss of efficiency. The controller of the device will be responsible for all higher level decisions and interpretation of some fields within message frames. The degree to which this occurs is dependent on the protocol being implemented. The receiver and transmitter logic operate as two totally independent sections with a minimum of common logic.

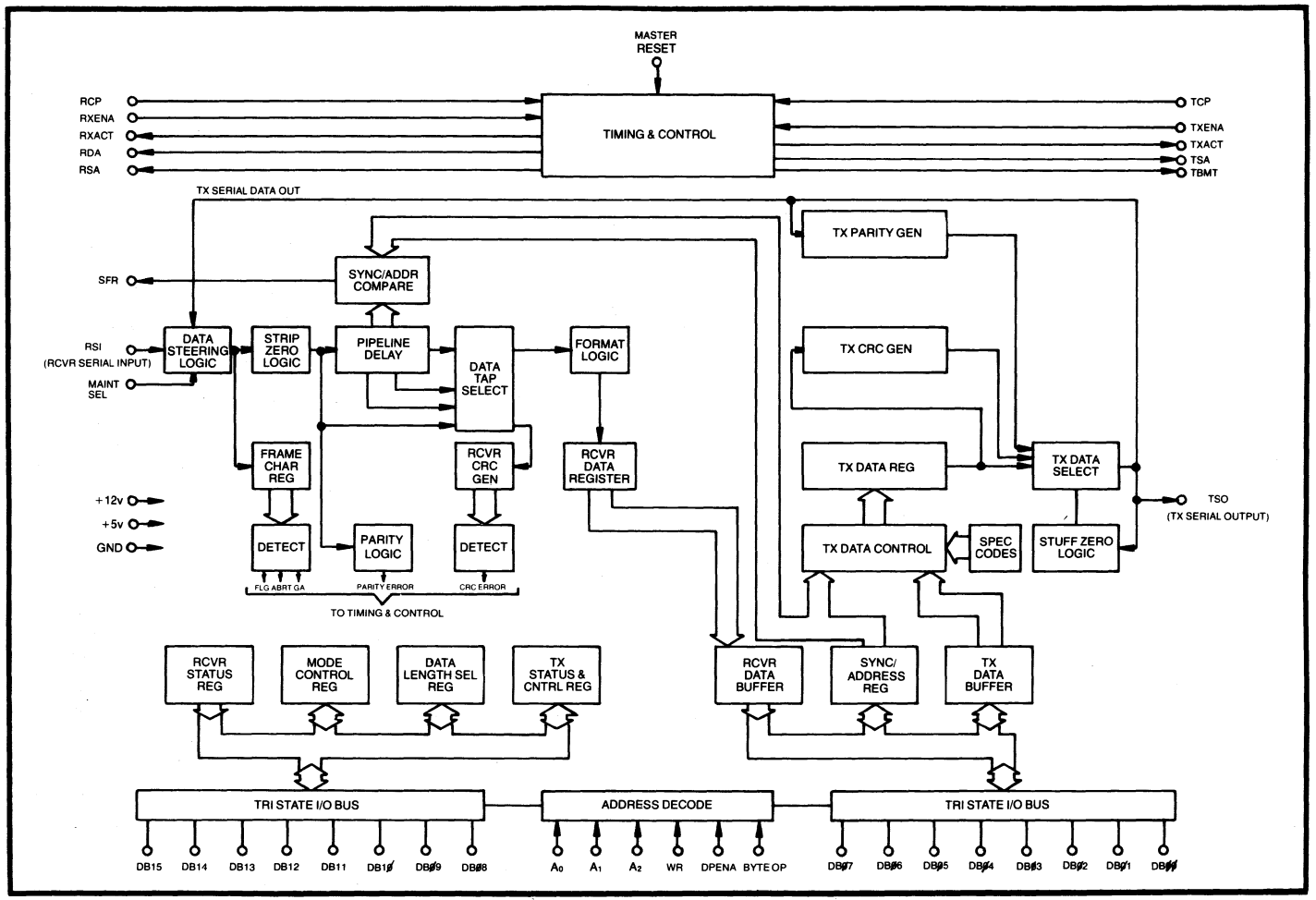
References:

1. ANSI—American National Standards Institute
   X353, XS34/589
   202-466-2299
2. CCITT—Consultative Committee for International Telephone and Telegraph
   X.25
   202-632-1007
3. EIA—Electronic Industries Association
   TR30, RS334
   202-659-2200
4. IBM
   General Information Brochure, GA27-3093
   Loop Interface—OEM Information, GA27-3098
   System Journal—Vol. 15, No. 1, 1976; G321-0044

Terminology

Term	Definition	Term	Definition
BOP	Bit Oriented Protocols: SDLC, HDLC, ADCCP	GA	01111111 (0 (LSB) followed by 7-1's)
CCP	Control Character Protocols: BiSync, DDCMP	LSB	First transmitted bit, First received bit
TDB	Transmitter Data Buffer	MSB	Last transmitted bit, Last received bit
RDB	Receiver Data Buffer	RDP	Receiver Data Path
TDSR	Transmitter Data Shift Register	TDP	Transmitter Data Path
FLAG	01111110	LM	Loop Mode
ABORT	11111111 (7 or more contiguous 1's)		

BLOCK DIAGRAM



Description of Pin Functions

Pin No.	Symbol	Name	I/O	Function
1	V_{DD}	Power Supply	PS	+12 volt Power Supply.
2	RCP	Receiver Clock	I	The positive-going edge of this clock shifts data into the receiver shift register.
3	RSI	Receiver Serial Input	I	This input accepts the serial bit input stream.
4	SFR	Sync/Flag Received	O	This output is set high, for 1 clock time of the RCP, each time a sync or flag character is received.
5	RXACT	Receiver Active	O	This output is asserted when the RDP presents the first data character of the message to the controller. In the BOP mode the first data character is the first non-flag character (address byte). In the CCP mode: 1. if strip-sync is set; the first non-sync character is the first data character 2. if strip-sync is not set; the first data character is the character following the second sync. In the BOP mode the trailing (next) FLAG resets RXACT. In the CCP mode RXACT is never reset, it can be cleared via RXENA.
6	RDA	Receiver Data Available	O	This output is set high when the RDP has assembled an entire character and transferred it into the RDB. This output is reset by reading the RDB.
7	RSA	Receiver Status Available	O	This output is set high: 1. CCP—in the event of receiver over run (ROR) or parity error (if selected), 2. BOP—in the event of ROR, CRC error (if selected) receiving REOM or RAB/GA. This output is reset by reading the receiver status register or dropping of RXENA.
8	RXENA	Receiver Enable	I	A high level input allows the processing of RSI data. A low level disables the RDP and resets RDA, RSA and RXACT.
9	GND	Ground	GND	Ground
10	DBØ8	Data Bus	I/O	Bidirectional Data Bus.
11	DBØ9	Data Bus	I/O	Bidirectional Data Bus.
12	DB1Ø	Data Bus	I/O	Bidirectional Data Bus.
13	DB11	Data Bus	I/O	Bidirectional Data Bus.
14	DB12	Data Bus	I/O	Bidirectional Data Bus.
15	DB13	Data Bus	I/O	Bidirectional Data Bus.
16	DB14	Data Bus	I/O	Bidirectional Data Bus.
17	DB15	Data Bus	I/O	Bidirectional Data Bus.
18	W/R	Write/Read	I	Controls direction of data port. W/R=1, Write. W/R=0, Read.
19	A2	Address 2	I	Address input—MSB.
20	A1	Address 1	I	Address input.
21	AØ	Address 0	I	Address input—LSB.
22	BYTE OP	Byte Operation	I	If asserted, byte operation (data port is 8 bits wide) is selected. If BYTE OP=0, data port is 16 bits wide.
23	DPENA	Data Port Enable	I	Strobe for data port. After address, byte op, W/R and data are set-up DPENA may be strobed. If reading the port, DPENA may reset (depending on register selected by address) RDA or RSA. If writing into the port, DPENA may reset (depending on register selected by address) TBMT.
24	DBØ7	Data Bus	I/O	Bidirectional Data Bus—MSB.
25	DBØ6	Data Bus	I/O	Bidirectional Data Bus.
26	DBØ5	Data Bus	I/O	Bidirectional Data Bus.
27	DBØ4	Data Bus	I/O	Bidirectional Data Bus.
28	DBØ3	Data Bus	I/O	Bidirectional Data Bus.
29	DBØ2	Data Bus	I/O	Bidirectional Data Bus.
30	DBØ1	Data Bus	I/O	Bidirectional Data Bus.
31	DBØØ	Data Bus	I/O	Bidirectional Data Bus—LSB.
32	V_{CC}	Power Supply	PS	+5 volt Power Supply.
33	MR	Master Reset	I	This input should be pulsed high after power turn on. This will: clear all flags, and status conditions, set TBMT=1, TSO=1 and place the device in the primary BOP mode with 8 bit TX/RX data length, CRC CCITT initialized to all 1's.
34	TXACT	Transmitter Active	O	This output indicates the status of the TDP. TXACT will go high after asserting TXENA and TSOM coinsidently with the first TSO bit. This output will reset one half clock after the byte during which TXENA is dropped.
35	TBMT	Transmitter Buffer Empty	O	This output is at a high level when the TDB or the TX Status and Control Register may be loaded with the new data. TBMT=0 on any write access to TDB or TX Status and Control Register. TBMT returns high when the TDSR is loaded.
36	TSA	Transmitter Status Available	O	TERR bit, indicating transmitter underflow. Reset by MR or assertion of TSOM.
37	TXENA	Transmitter Enable	I	A high level input allows the processing of transmitter data.
38	TSO	Transmitter Serial Output	O	This output is the transmitted character.
39	TCP	Transmitter Clock	I	The positive going edge of this clock shifts data out of the transmitter shift register.
40	MSEL	Maintenance Select	I	Internally RSI becomes TSO and RCP becomes $\overline{TCP}$. Externally RSI is disabled and TSO=1.

Wire "OR" with DBØØ-DBØ7 For 8 bit data bus

Definition of Terms
Register Bit Assignment Chart 1 and 2

Data Bus	Term	Definition
DBØ8	RSOM	Receiver Start of Message—read only bit. In BOP mode only, goes high when first non-flag (address byte) character loaded into RDB. It is cleared when the second byte is loaded into the RDB.
DBØ9	REOM	Receiver End of Message—read only bit. In BOP mode only, set high when last byte of data loaded into RDB, or when an ABORT character is received. It is cleared on reading of Receiver Status Register or dropping of RXENA.
DB1Ø	RAB/GA	Received ABORT or GO AHEAD character, read only bit. In BOP mode only, if LM=0 this bit is set on receiving an ABORT character; if LM=1 this bit is set on receiving a GO AHEAD character. This is cleared on reading of Receiver Status Register or dropping of RXENA.
DB11	ROR	Receiver Over Run—read only bit. Set high when received data transferred into RDB and previous data has not been read, indicating failure to service RDA within one character time. Cleared on reading of Receiver Status Register or dropping of RXENA.
DB12-14	A, B, C	Assembled Bit Count—read only bits. In BOP mode only, examine when REOM=1. ABC=0, message terminated on stated boundary. ABC=XXX, message terminated (by FLAG or GA) on unstated boundary, binary value of ABC = number of valid bits available in RDB (right hand justified).
DB15	ERR CHK	Error Check—read only bit. In BOP set high if CRC selected and received in error, examine when REOM=1. In CCP mode: 1. set high if parity selected and received in error, 2. if CRC selected (tested at end of each byte) ERR CHK = 1 if CRC GOOD, ERR CHK = 0 if CRC NOT GOOD. Controller must determine the last byte of the message.
DB8	TSOM	Transmitter Start of Message—W/R bit. Provided TXENA=1, TSOM initiates start of message. In BOP, TSOM=1 generates FLAG and continues to send FLAG's until TSOM=0, then begin data. In CCP: 1. IDLE=0, transmit out of SYNC register, continue until TSOM=0, then begin data. 2. IDLE=1 transmit out of TDB. In BOP mode there is also a Special Space Sequence of 16-0's initiated by TSOM=1 and TEOM=1. SSS is followed by FLAG.
DB9	TEOM	Transmit End of Message—W/R bit. Used to terminate a message. In BOP mode, TEOM=1 sends CRC, then FLAG; if TXENA=1 and TEOM=1 continue to send FLAG's, if TXENA=0 and TEOM=1 MARK line. In CCP: 1. IDLE=0, TEOM=1 send SYNC, if TXENA=1 and TEOM=1 continue to send SYNC's, if TXENA=0 and TEOM=1 MARK line. 2. IDLE=1, TEOM=1, MARK line.
DB1Ø	TXAB	Transmitter Abort—W/R bit. In BOP mode only, TXAB=1 finish present character then: 1. IDLE=0, transmit ABORT 2. IDLE=1, transmit FLAG.
DB11	TXGA	Transmit Go Ahead—W/R bit. In BOP mode only, modifies character called for by TEOM. GA sent in place of FLAG. Allows loop termination—GA character.
DB15	TERR	Transmitter Error—read only bit. Underflow, set high when TDB not loaded in time to maintain continuous transmission. In BOP automatically transmit: 1. IDLE=0, ABORT 2. IDLE=1, FLAG. In CCP automatically transmit: 1. IDLE=0, SYNC 2. IDLE=1, MARK. Cleared by TSOM.
DB8-1Ø	X, Y, Z	Z Y X —W/R bits. These are the error control bits. 0 0 0 $X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "1" 0 0 1 $X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "0" 0 1 0 Not used 0 1 1 $X^{16}+X^{15}+X^2+1$—CRC16 1 0 0 Odd Parity—CCP Only 1 0 1 Even Parity—CCP Only 1 1 0 Not Used 1 1 1 Inhibit all error detection and transmission Note: Do not modify XYZ until both data paths are idle
DB11	IDLE	IDLE mode select—W/R bit. Affects transmitter only. In BOP—control the type of character sent when TXAB asserted or in the event of data underflow. In CCP—controls the method of initial SYNC character transmission and underflow, "1" = transmit SYNC from TDB., "0"=transmit SYNC from SYNC/ADDRESS register.
DB12	SEC ADD	Secondary Address Mode—W/R bit. In BOP mode only—after FLAG looks for address match prior to activating RDP, if no match found, begin FLAG search again. SEC ADD bit should not be set if EXADD=1 or EXCON=1.
DB13	STRIP SYNC/LOOP	Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping.
DB14	PROTOCOL	PROTOCOL—W/R bit. BOP=0, CCP=1
DB15	*APA	All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP.
DB13-15	TXDL	Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 0 0 1 One bit per character* *For data length only, not to be used for SYNC character (CCP mode).
DB8-1Ø	RXDL	Receiver Data Length—W/R bits. RXDL3 RXDL2 RXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character
DB11	EXCON	Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD =1.
DB12	EXADD	Extended Address Field—W/R bit. In receiver only; LSB of address byte tested for a "1". If NO—continue receiving address bytes, if YES go into control field. EXADD bit should not be set if SEC ADD =1.

Receiver Status Register

Transmitter Status and Control Register

Mode Control Register

Data Length Select Register

SECTION III

*Note: Product manufactured before 1Q79 may not have this feature.

Register Bit Assignment Chart 1

REGISTER	DPØ7	DPØ6	DPØ5	DPØ4	DPØ3	DPØ2	DPØ1	DPØØ
Receiver Data Buffer (Read Only- Right Justified- Unused Bits=0)	RD7 MSB	RD6	RD5	RD4	RD3	RD2	RD1	RDØ LSB
Transmitter Data Register (Read/Write- Unused Inputs=X)	TD7 MSB	TD6	TD5	TD4	TD3	TD2	TD1	TDØ LSB
Sync/Secondary Address (Read/Write- Right Justified- Unused Inputs=X)	SSA7 MSB	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSAØ LSB

Register Bit Assignment Chart 2

REGISTER	DP15	DP14	DP13	DP12	DP11	DP1Ø	DPØ9	DPØ8
Receiver Status (Read Only)	ERR CHK	C	B	A	ROR	RAB/GA	REOM	RSOM
TX Status and Control (Read/Write)	TERR (Read Only)	0	0	0	TXGA	TXAB	TEOM	TSOM
Mode Control (Read/Write)	*APA	PROTOCOL	STRIP SYNC/ LOOP	SEC ADD	IDLE	Z	Y	X
Data Length Select (Read/Write)	TXDL3	TXDL2	TXDL1	EXADD	EXCON	RXDL3	RXDL2	RXDL1

* Note: Product manufactured before 1Q79 may not have this feature.

Register Address Selection

1) BYTE OP = 0, data port 16 bits wide

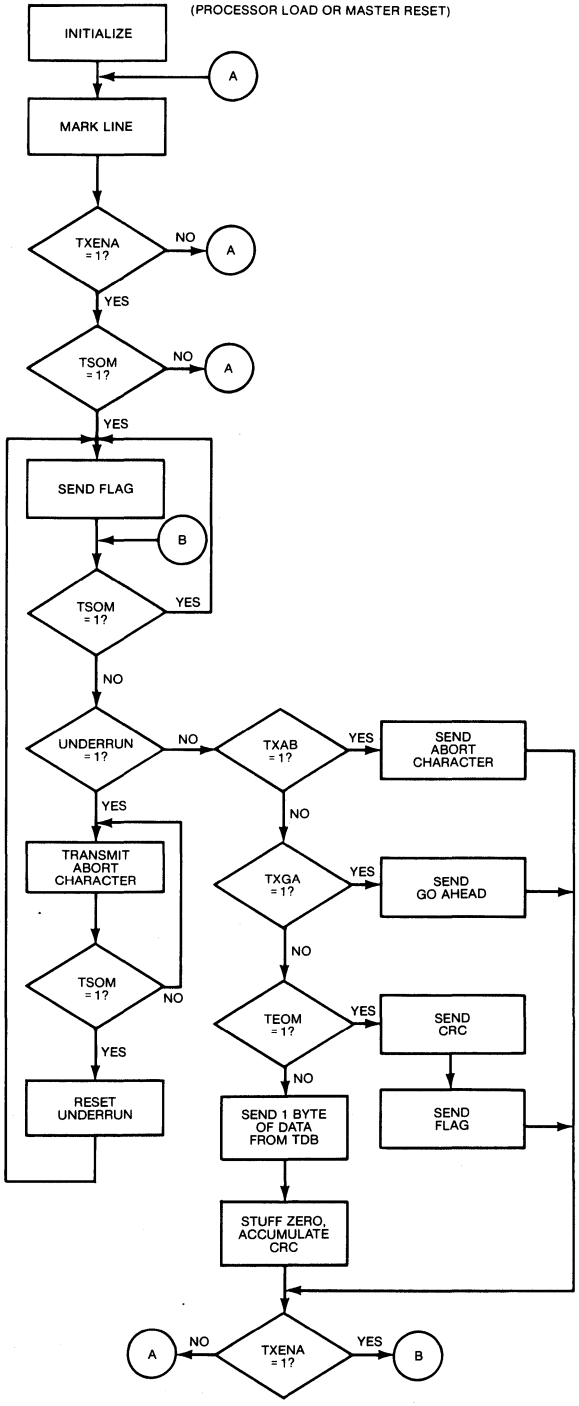
A2	A1	AØ	Register
0	0	X	Receiver Status Register and Receiver Data Buffer
0	1	X	Transmitter Status and Control Register and Transmitter Data Buffer
1	0	X	Mode Control Register and SYNC/Address Register
1	1	X	Data Length Select Register

X = don't care

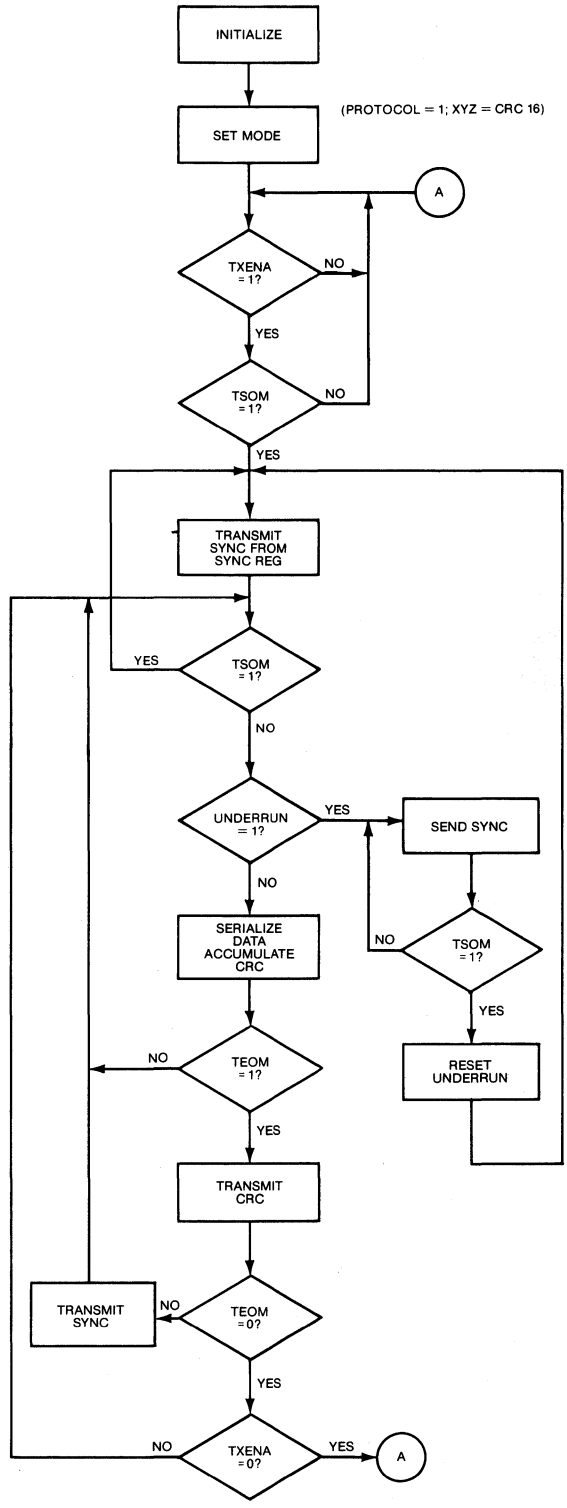
2) BYTE OP = 1, data port 8 bits wide

A2	A1	AØ	Register
0	0	0	Receiver Data Buffer
0	0	1	Receiver Status Register
0	1	0	Transmitter Data Buffer
0	1	1	Transmitter Status and Control Register
1	0	0	SYNC/Address Register
1	0	1	Mode Control Register
1	1	0	———————
1	1	1	Data Length Select Register

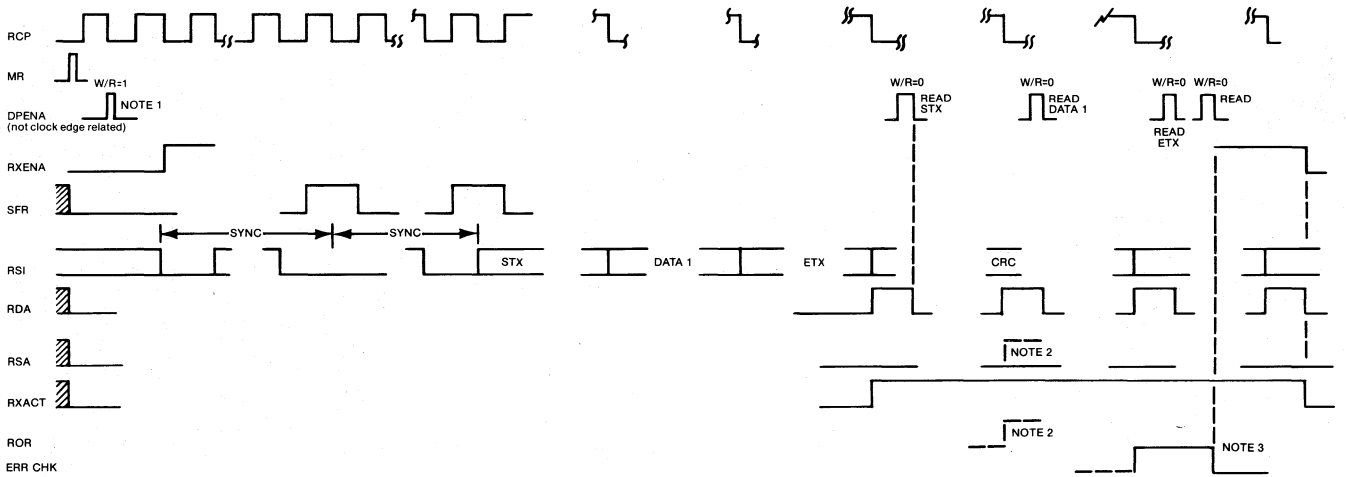
BOP TRANSMITTER OPERATION



CCP TRANSMITTER OPERATION

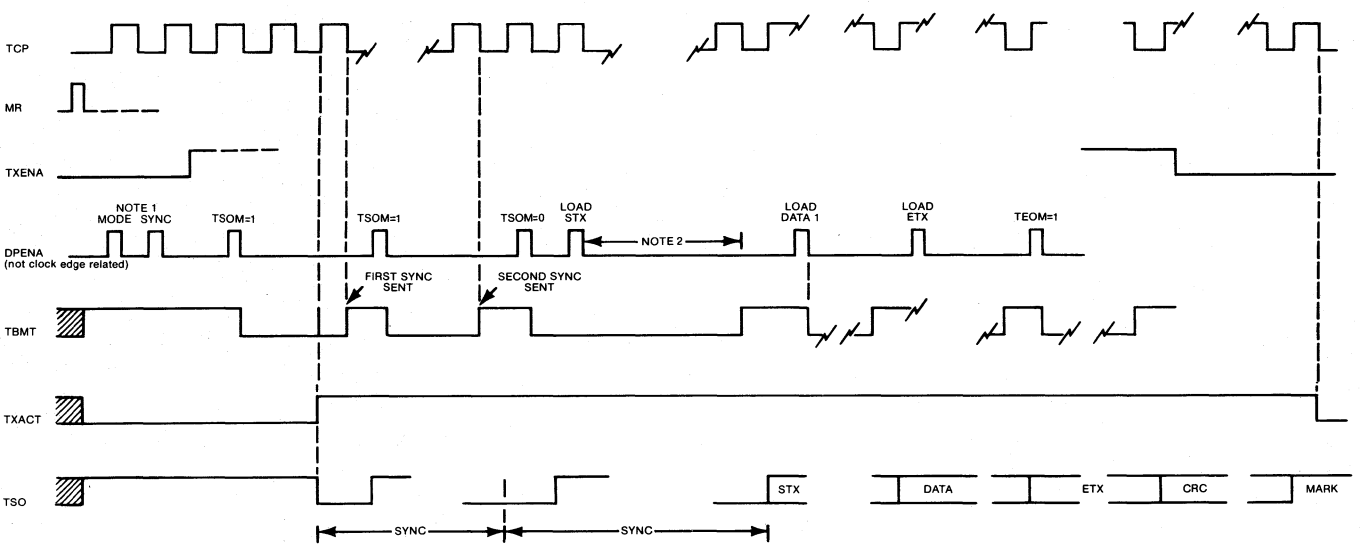


CCP RECEIVER TIMING



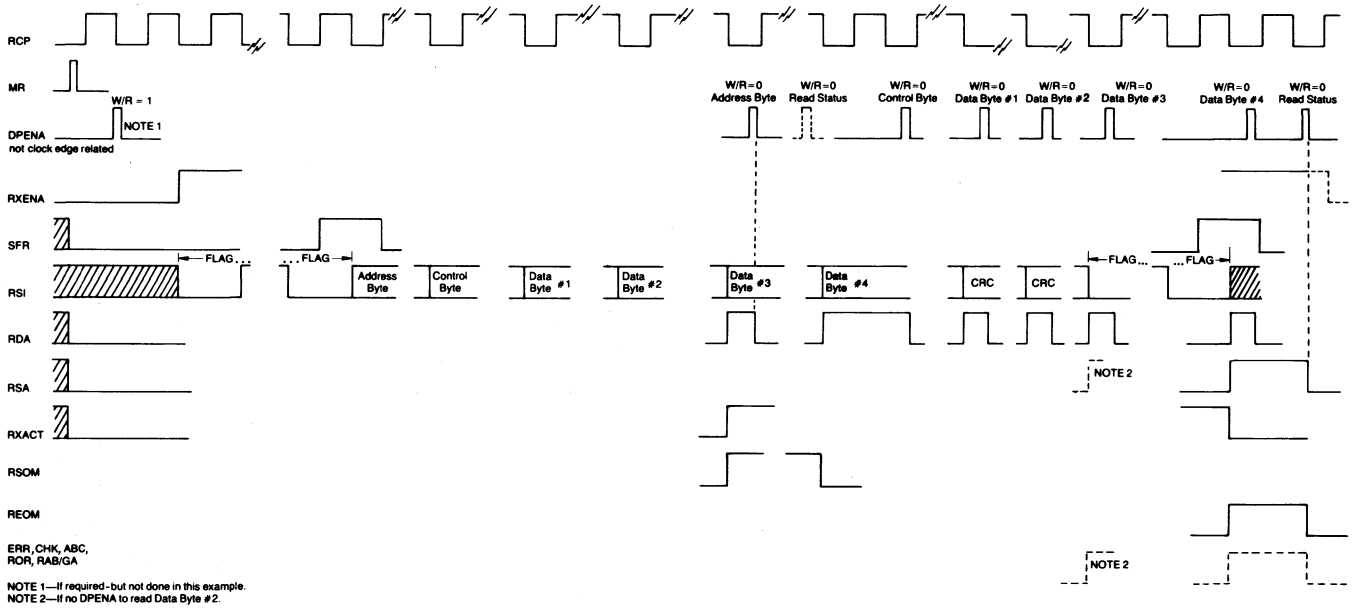
NOTE 1—Mode set for CCP with CRC selected
NOTE 2—If overrun had occured—no READ STX
NOTE 3—ERR CHK must be sampled before next byte or before RXENA brought low

CCP TRANSMITTER OPERATION



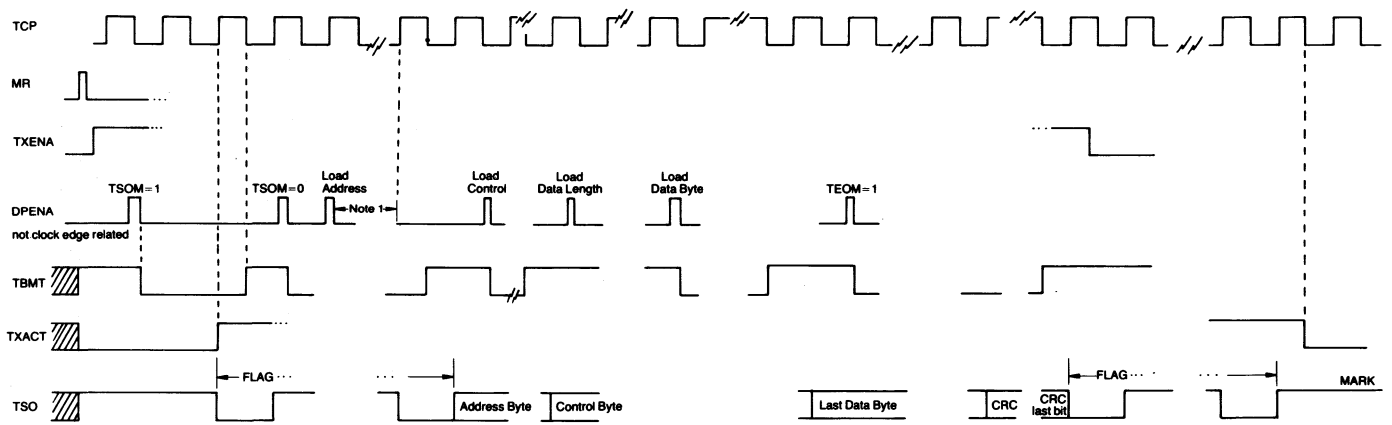
NOTE 1—Mode is CCP with CRC selected
NOTE 2—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT=1 to avoid underrun

BOP RECEIVER TIMING



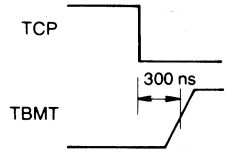
NOTE 1—If required-but not done in this example.
NOTE 2—If no DPENA to read Data Byte #2.

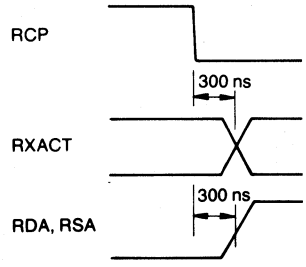
BOP TRANSMITTER OPERATION

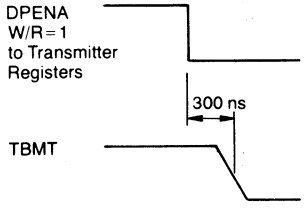


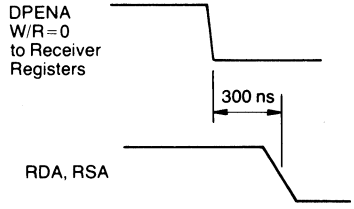
Note 1—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT=1. To avoid underrun.

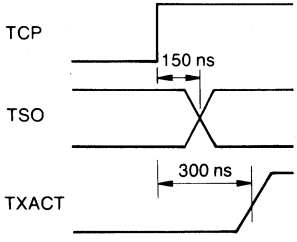
AC TIMING DIAGRAMS

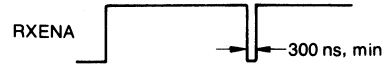








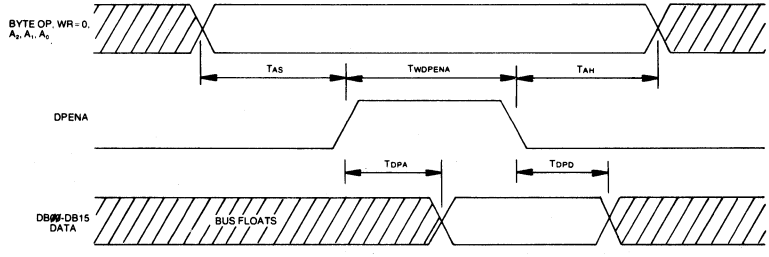




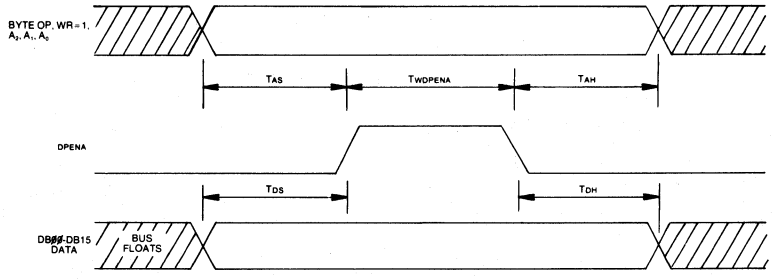
Resets: RDP-RDA, RSA, RXACT, receiver into search mode (for FLAG)

Note: Unless otherwise specified all times are maximum.

Data Port Timing



READ FROM USYNR/T



WRITE TO USYNR/T

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

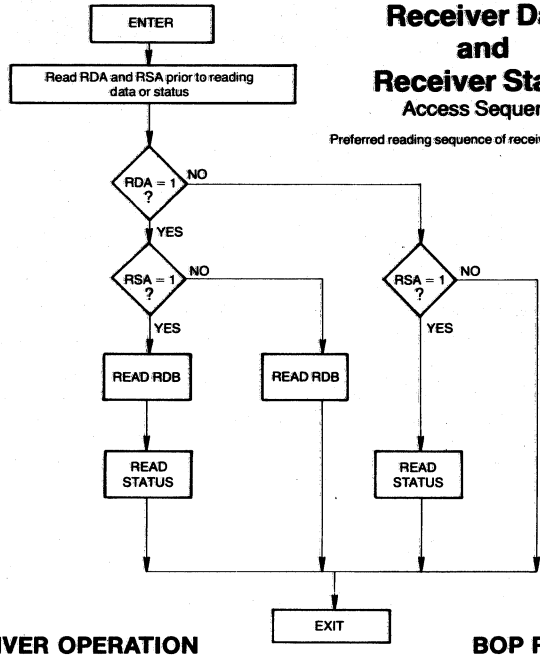
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

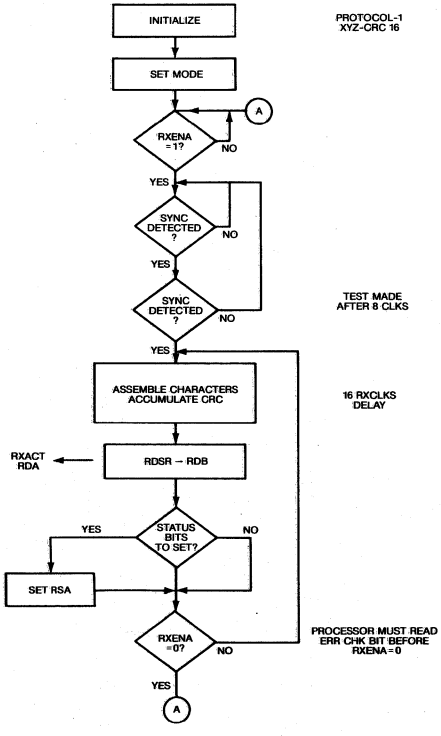
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	2.4				I_{OH}=40μa
INPUT LEAKAGE					
Data Bus		5.0	50.0	μa	0≤V_{IN}≤5v, DPENA=0 or W/R=I
All others				μa	V_{IN}=+5v
INPUT CAPACITANCE					
Data Bus, C_{IN}				pf	
Address Bus, C_{IN}				pf	
Clock, C_{IN}				pf	
All other, C_{IN}				pf	
POWER SUPPLY CURRENT					
I_{CC}			70	ma	
I_{DD}			90	ma	
A.C. Characteristics					T_A=25°C
CLOCK-RCP, TCP					
frequency	DC		1.5	MHz	
PW_H	325			ns	
PW_L	325			ns	
t_r, t_f		10		ns	
DPENA, T_{WDPENA}	250		50 μs	ns	
Set-up Time, T_{AS}	0			ns	
Byte Op, W/R					
A_2, A_1, A_0					
Hold Time, T_{AH}	0			ns	
Byte Op, WIR,					
A_2, A_1, A_0					
DATA BUS ACCESS, T_{DPA}			150	ns	
DATA BUS DISABLE DELAY, T_{DPD}			100	ns	
DATA BUS SET-UP TIME, T_{DBS}	0			ns	
DATA BUS HOLD TIME, T_{DBH}	100			ns	
MASTER RESET, MR	350			ns	

Receiver Data and Receiver Status Access Sequence

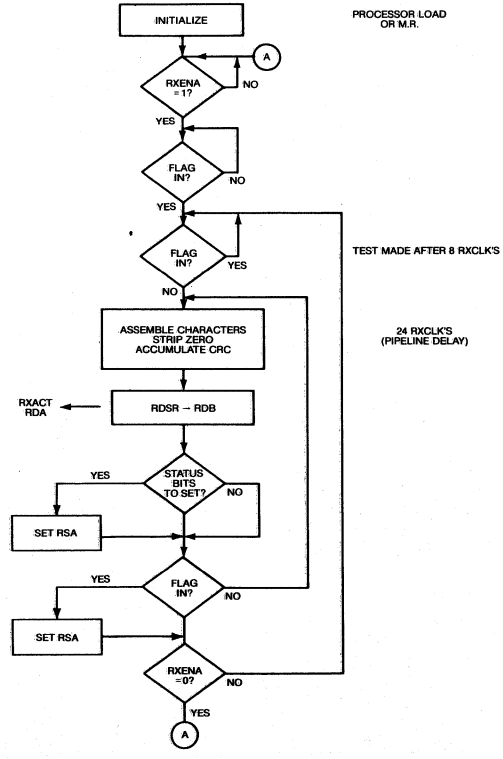
Preferred reading sequence of receiver RDA and RSA.



CCP RECEIVER OPERATION



BOP RECEIVER OPERATION



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We keep ahead of our competition so you can keep ahead of yours.

Dual 32 Bit CRC SDLC Generator/Checker CRC-32

FEATURES

- ☐ SDLC 32 bit CRC
- ☐ COM 5025 USYNRT Companion
- ☐ Data Rate—2MHz typical
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N-Channel MOS Technology

GENERAL DESCRIPTION

SMC's COM 8004 is a dual 32-bit CRC Generator/Checker for use with SDLC protocols. It is a companion device to SMC's COM 5025 USYNRT. It operates at bit rates from DC to 2.0 MHz from a single +5v supply and is housed in a 20 lead x 0.3 inch DIP. All inputs and outputs are TTL compatible with full noise immunity.

The COM 8004 is comprised of two independent halves, and each half may be operated in the check or generate mode. The polynominal used in computations is:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$.

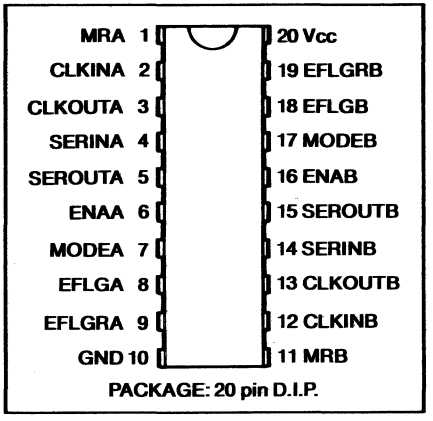
The CRC register is initialized to all ones and the result is inverted before being appended to the message. The expected remainder is:
$X^{31} + X^{30} + X^{26} + X^{25} + X^{24} + X^{18} + X^{15} + X^{14} + X^{12} + X^{11} + X^{10} + X^8 + X^6 + X^5 + X^4 + X^3 + X + 1$.

Each half has a nine-bit serial data shift register. Data moves on the positive edge of the clock, and all clocked inputs are designed for zero-hold-time (e.g. 7474). A "clock out" pin provides gated clocks to the accompanying USYNRT (COM 5025).

In the generate mode, computation is initiated upon detection of a flag character in the serial bit stream. CRC computation proceeds upon the serial data until a second flag is detected. CLK OUT to the SDLC transmitter is then halted, and the 32-bit CRC is passed out; CLK OUT is then resumed, and the flag character is passed out. Nonsignificant zeros are automatically stripped and stuffed, and shared flags are supported. If the data between flags is less than two full bytes, the CRC is discarded and the serial data stream remains unaltered.

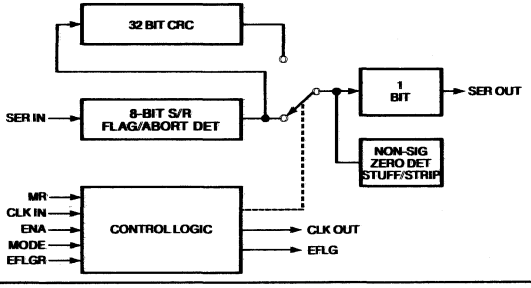
In the check mode, computation is similarly initiated upon detection of a flag. Detection of a second flag causes the conditional setting of the error flag. A separate reset pin is provided for the error flag. No error is flagged on messages of less than two full bytes between flags. Detection of an abort character (7 consecutive ones) in either mode causes computation to be reset and a search for an opening flag resumed.

PIN CONFIGURATION

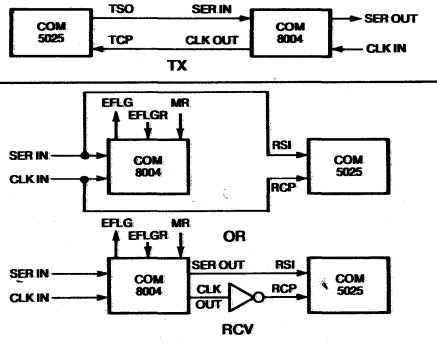


PACKAGE: 20 pin D.I.P.

BLOCK DIAGRAM
FOR ONE-HALF OF THE COM 8004



TYPICAL SYSTEM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	MASTER RESET-A	MRA	MRA presets the CRC calculation in Section A of the COM 8004 to all ones and forces the "pipeline" (8 shift register bits and the output flip-flop) to a logic "1" (Mark). The COM 8004 will only exit the reset state when MRA has been released and all 8 bits of a FLAG (01111110) have been received.
2	CLOCK INPUT-A	CLKINA	Baud Rate Clock for Section A.
3	CLOCK OUTPUT-A	CKLOUTA	Clock output from Section A. This is used to provide the clock for the USYNRT. CLKOUTA will normally track CLKINA. In the generate mode, when the last flag bit has been shifted into the shift register of the COM 8004, CLKOUTA will be held high until the CRC check character has been sent out. After the last bit of the CRC character is transmitted, CLKOUTA will resume tracking CLKINA.
4	SERIAL INPUT-A	SERINA	Serial input to the COM 8004 Section A. For transmission, SERINA is connected to the transmitter serial output of the USYNRT. For receiving, SERINA is connected to the received data output of the modem.
5	SERIAL OUTPUT-A	SEROUTA	Serial output from Section A of the COM 8004. For transmission, SEROUTA is connected to the transmit data input of the modem. For receiving, SEROUTA may be connected to the serial data input of the USYNRT.
6	ENABLE-A	ENAA	When ENAA is low, section A of the COM 8004 will pass data from SERINA to SEROUTA after a nine bit delay without alteration and without checking or generating CRC. If ENAA is high, CRC generation or checking will be enabled. ENAA is gated into the COM 8004 by the rising edge of CLKINA.
7	MODE SELECT-A	MODEA	MODEA determines whether Section A of the COM 8004 is in the receive (CRC check) Mode or transmit (CRC generate) Mode. Logic "1" selects CRC check. Logic "0" selects CRC generate.
8	ERROR FLAG-A	EFLGA	EFLGA will go high if, when in the CRC check mode, section A of the COM 8004 has detected an error. EFLGA can only be reset by a MASTER RESET (MRA) or by ERROR FLAG RESET (EFLGRA).
9	ERROR FLAG RESET-A	EFLGRA	A logic "1" on EFLGRA will reset EFLGA. If EFLGRA is kept at a logic "1," it will inhibit the setting of EFLGA.
10	GROUND	GND	Ground.
11	MASTER RESET-B	MRB	Master reset for Section B. See MRA for description.
12	CLOCK IN-B	CLKINB	Clock input for Section B. See CLKINA for description.
13	CLOCK OUT-B	CLKOUTB	Clock output for Section B. See CLKOUTA for description.
14	SERIAL INPUT-B	SERINB	Serial input for Section B. See SERINA for description.
15	SERIAL OUTPUT-B	SEROUTB	Serial output for Section B. See SEROUTA for description.
16	ENABLE-B	ENAB	CRC enable for Section B. See ENAA for description.
17	MODE SELECT-B	MODEB	Mode select for Section B. See MODEA for description.
18	ERROR FLAG-B	EFLGB	Error Flag for Section B. See EFLGA for description.
19	ERROR FLAG RESET-B	EFLGRB	Error flag reset for Section B. See EFLGRA for description.
20	POWER SUPPLY	V_{CC}	+5 volt power supply input.

OPERATION

The COM 8004 has 3 modes of operation, as selected by the ENABLE and MODE SELECT inputs. They are:

ENABLE	MODE SELECT	
0	0	CRC Disabled. Data is shifted from SERIN to SEROUT with no computation performed. Serial delay is 9 bit times.
0	1	Same as above.
1	0	CRC generation mode.
1	1	CRC check mode.

In the CRC generation and check modes, calculations begin upon receipt of the first data character after an opening FLAG. "Stuffed zeroes" are stripped for the purpose of the CRC calculation. CRC calculation will continue until either a MASTER RESET occurs, ENABLE is brought to logic zero, an ABORT character is received, or a closing FLAG is received.

CRC Generation

Upon detection of a closing FLAG character, CLKOUT is left high (stopping USYNRT activity), and the CRC accumulation is shifted out by CLKIN. CLKOUT then resumes clocking, and the FLAG (which has been stored in the shift register) is shifted out. The CRC check data is inverted before this data is transmitted. Zero-stuffing is performed on the inverted CRC check data.

During the time CKLOUT is forced high and CRC check data is being shifted out, data on SERIN will be ignored.

If an ABORT character is received, CRC calculation will cease after the last "1" bit of the ABORT character is shifted into the shift register. Data will pass through the COM 8004 without effect until a FLAG is received.

CRC Check (Reception)

When the last bit of a closing flag enters the shift register, ERRCHK will go high on the following positive CLKIN transition if a CRC error is detected.

Operation Notes

Note 1: The minimum message size is sixteen significant bits following an opening flag. A stuffed zero is not considered a significant bit. If the message is less than 16 bits, the data will pass through the COM 8004 without being affected.

If the sixteenth received bit is the fifth consecutive one, but is not followed by a stuffed zero before a FLAG, the COM 8004 will detect the FLAG but the minimum message will not have occurred. CRC calculation will begin anew after this FLAG is detected.

01111110 DDDDDDDD DD011111 (MISSING STUFFED 0) 01111110

OPENING FLAG — LAST "1" IN THE BIT 16 LOCATION. — CLOSING FLAG

Note 2: If the seventeenth bit of a message followed by a FLAG is the fifth consecutive one, but the stuffed zero is missing, the following will occur:

A) CRC Generate Mode: The last "one" bit, bit 17, will not be calculated into the CRC, but will appear at the serial output. The first bit of the CRC character will be forced to a zero, therefore looking like a stuffed zero.

B) CRC Check Mode: The last "one" bit, bit 17, will not be calculated into the CRC.

01111110 DDDDDDDD DDD01111 1 (MISSING STUFFED 0) 01111110

OPENING FLAG — LAST "1" IN THE BIT 17 LOCATION. — CLOSING FLAG

Note 3: If a stuffed zero is missing in the middle or end of a message, the reaction will depend on the next bit. If it is a one, a FLAG or ABORT may be detected. If an ABORT is detected, the message and the CRC checking is aborted. If a FLAG is detected, a CRC error will be detected.

If the missing zero is followed by a zero, the CRC computation will continue, but the zero bit will be stripped, causing a CRC error.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground .....-0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5 Volts ±5%, unless otherwise noted)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS						
Input Voltage Levels						
Low Level	V_{IL}			0.8	V	
High Level	V_{IH}	2.0			V	
Output Voltage Levels						
Low Level	V_{OL}			0.4	V	I_{OL} = 1.6 mA
High Level	V_{OH}	2.4			V	I_{OH} = -100 μA
Input Capacitance	C_{IN}		10	25	pf	
Power Supply Current	I_{CC}			100	mA	
AC CHARACTERISTICS						T_A = 25°C
Clock Frequency	f_{IN}			2	MHz	
Clock Pulse Width—High	t_{CLKH}	350			ns	Figure 1
Input Set-Up Time	t_{DC}	100			ns	Figure 1
Input Hold Time	t_{CD}	0			ns	Figure 1
Master Reset Pulse Width	t_{PW}	250			ns	Figure 2
Reset Delay	t_{MR}			250	ns	Figure 2
Error Flag Delay	t_{FD}			300	ns	Figure 3
Error Flag Reset Delay	t_{FR}			100	ns	Figure 4
ERRST Pulse Width	t_{EW}	100			ns	Figure 4
Clock Propagation Delay	t_{PD}			150	ns	Figure 5
SEROUT Propagation Delay	t_{SD}			150	ns	Figure 5

Figure 1

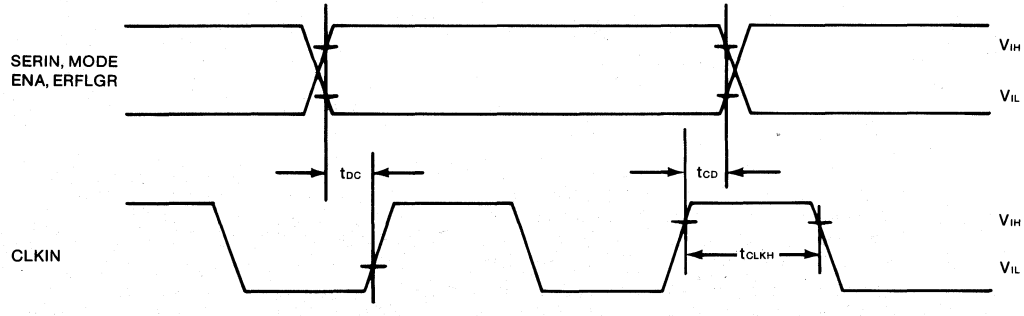


Figure 2

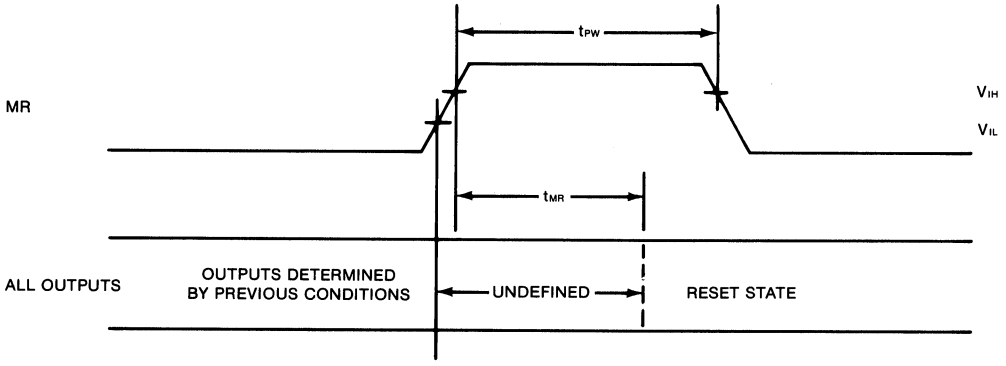


Figure 3

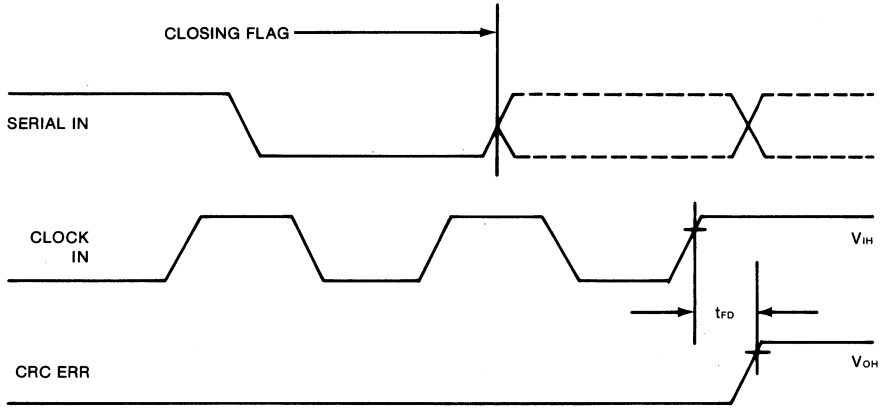


Figure 4

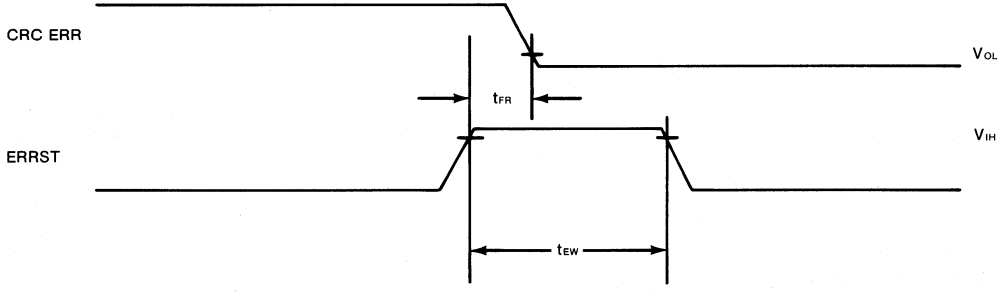
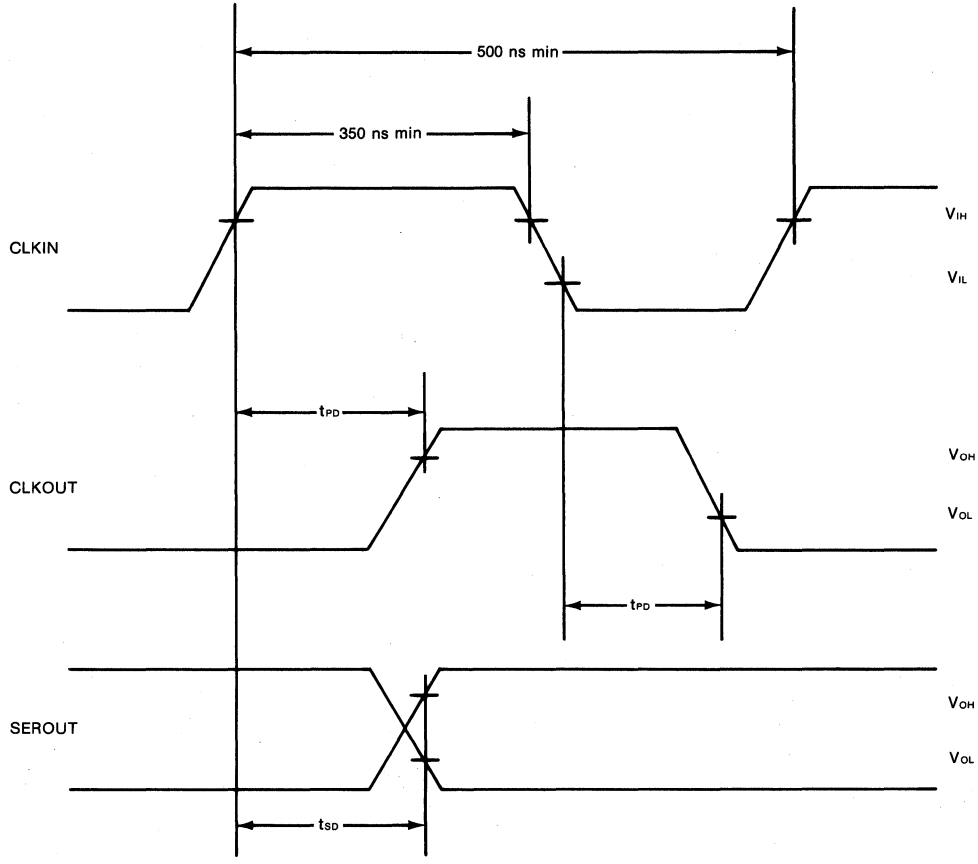


Figure 5



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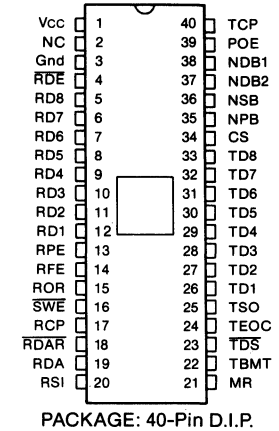
COM 8017
COM 8502

Universal Asynchronous Receiver/Transmitter
UART

Pin Configuration

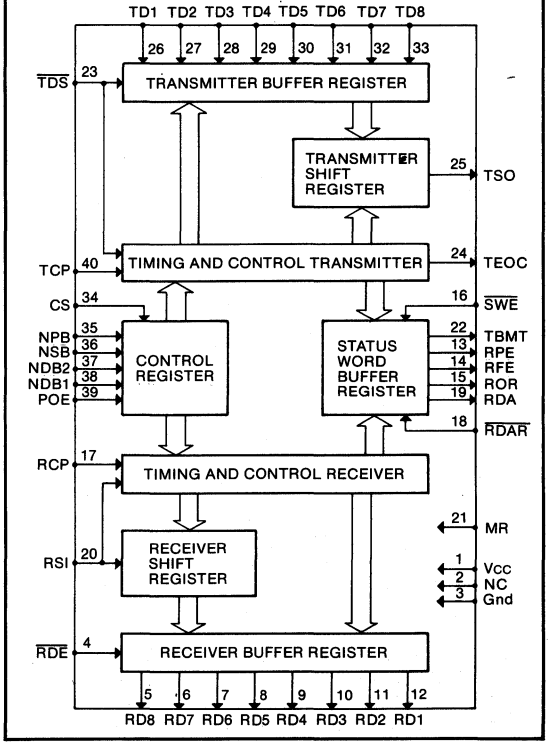


PACKAGE: 40-Pin D.I.P.

FEATURES

- ☐ Single +5V Power Supply
- ☐ Direct TTL Compatibility — no interfacing circuits required
- ☐ Full or Half Duplex Operation — can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered — eliminates need for precise external timing
- ☐ Start Bit Verification — decreases error rate
- ☐ Fully Programmable — data word length; parity mode; number of stop bits: one, one and one-half, or two
- ☐ High Speed Operation — 40K baud, 200ns strobes
- ☐ Master Reset — Resets all status outputs
- ☐ Tri-State Outputs — bus structure oriented
- ☐ Low Power — minimum power requirements
- ☐ Input Protected — eliminates handling problems
- ☐ Ceramic or Plastic Dip Package — easy board insertion
- ☐ Compatible with COM 2017, COM 2502
- ☐ Compatible with COM 8116, COM 8126, COM 8136, COM 8146, COM 8046 Baud Rate Generators

Functional Block Diagram



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolothic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's patented COPLAMOS® technology and employs depletion mode loads, allowing operation from a single +5V supply. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7 or 8 data bits, odd/even or no parity, and 1, or 2 stop bits. In addition the COM 8017 will provide 1.5 stop bits when programmed for 5 data bits and 2 stop bits. The UART can operate in either the full or half duplex mode. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

DESCRIPTION OF OPERATION—TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

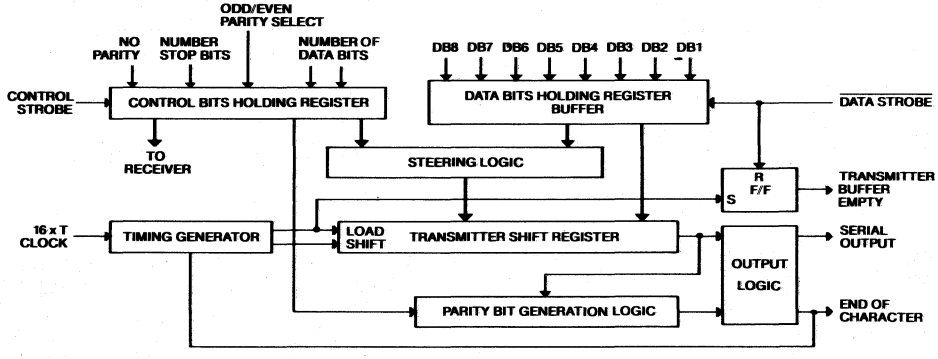
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the date strobe ($\overline{TDS}$) has been pulsed the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the TBMT signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TSO goes low (the start bit), TEOC goes low, the TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

TRANSMITTER BLOCK DIAGRAM



DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions from mark (high) to space (low). If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

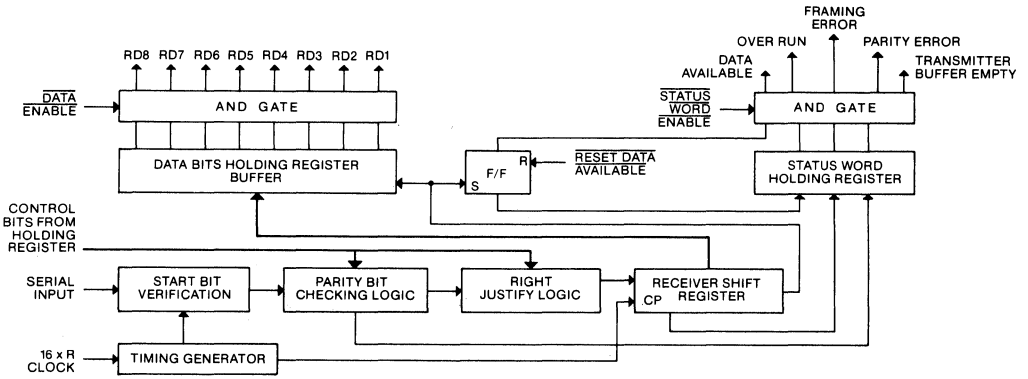
If the transmitted parity bit does not agree with the received parity bit, the parity error flip-flop of the

status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, due to an improperly framed character, the framing error flip-flop is set high, indicating a framing error.

Once a full character has been received internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

At this time the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

RECEIVER BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{CC}	Power Supply	+5 volt Supply
2	NC	No Connection	No Connection
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.
5-12	RD8-RD1	Receiver Data Outputs	These are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.

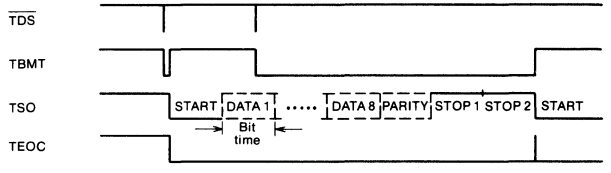
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
15	ROR	Receiver Over Run	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level.
19	RDA	Receiver Data Available	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level.
22	TBMT	Transmitter Buffer Empty	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character	This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.

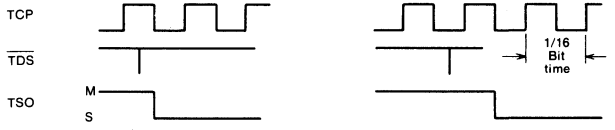
DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of 2 stop bits when programming a 5 data bit word generates 1.5 stop bits from the COM 2017 or COM 2017/H.
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

TRANSMITTER TIMING—8 BIT, PARITY, 2 STOP BITS

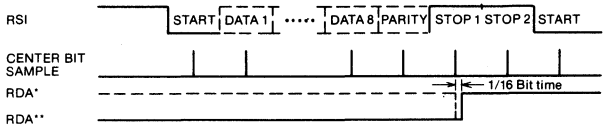


TRANSMITTER START-UP



Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of TDS.

RECEIVER TIMING—8 BIT, PARITY, 2 STOP BITS



*The RDA line was previously not reset (ROR = high-level).
**The RDA line was previously reset (ROR = low-level).

START BIT DETECT/VERIFY

If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin. with respect to ground ..... −0.3V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that at clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	0		0.8	V	
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	$I_{OL} = 1.6mA$
High-level, V_{OH}	2.4			V	$I_{OH} = -100\mu A$
INPUT CURRENT					
Low-level, I_{IL}			300	μA	$V_{IN} = GND$
OUTPUT CURRENT					
Leakage, I_{LO}			±10	μA	$\overline{SWE} = \overline{RDE} = V_{IH}$, $0 \leq V_{OUT} \leq +5V$
Short circuit, I_{OS}**			30	mA	$V_{OUT} = 0V$
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	$\overline{SWE} = \overline{RDE} = V_{IH}$
POWER SUPPLY CURRENT					
I_{CC}			25	mA	All outputs = V_{OH}, All inputs = V_{CC}
A.C. CHARACTERISTICS					$T_A = +25°C$
CLOCK FREQUENCY					
COM8502, COM 8017	DC		640	KHz	RCP, TCP
PULSE WIDTH					
Clock	0.7			μs	RCP, TCP
Master reset	500			ns	MR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	$\overline{TDS}$
Receiver data available reset	200			ns	$\overline{RDAR}$
INPUT SET-UP TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable			350	ns	$\overline{RDE}$: T_{PD1}, T_{PD0}
Status word enable			350	ns	$\overline{SWE}$: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY			350	ns	$\overline{RDE}$, $\overline{SWE}$

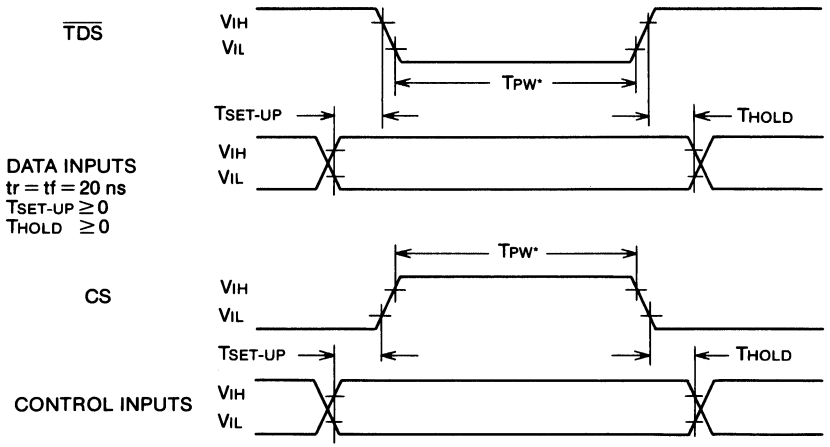
**Not more than one output should be shorted at a time.

NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within one clock period (TCP) after the trailing edge of $\overline{TDS}$.

2. The start bit (mark to space transition) will always be detected within one clock period of RCP, guaranteeing a maximum start bit slippage of 1/16th of a bit time.

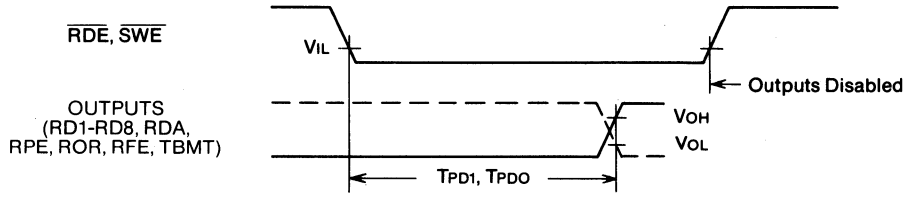
3. The tri-state output has 3 states: 1) low impedance to V_{CC} 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

DATA/CONTROL TIMING DIAGRAM

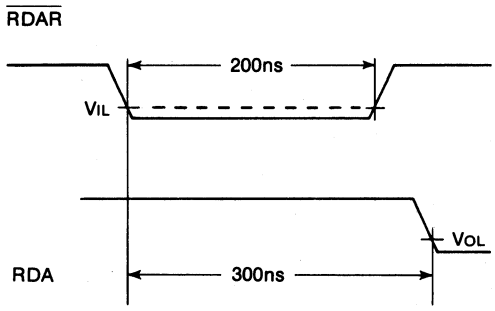


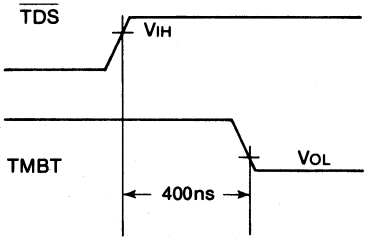
*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

OUTPUT TIMING DIAGRAM

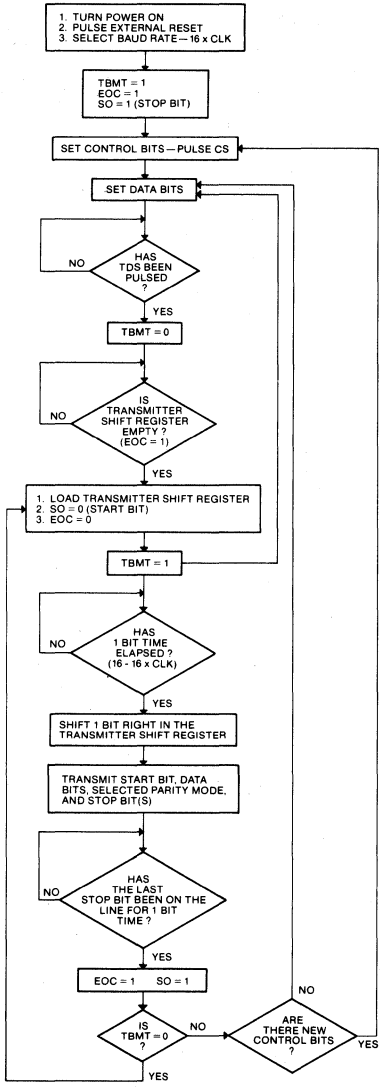


NOTE: Waveform drawings not to scale for clarity.

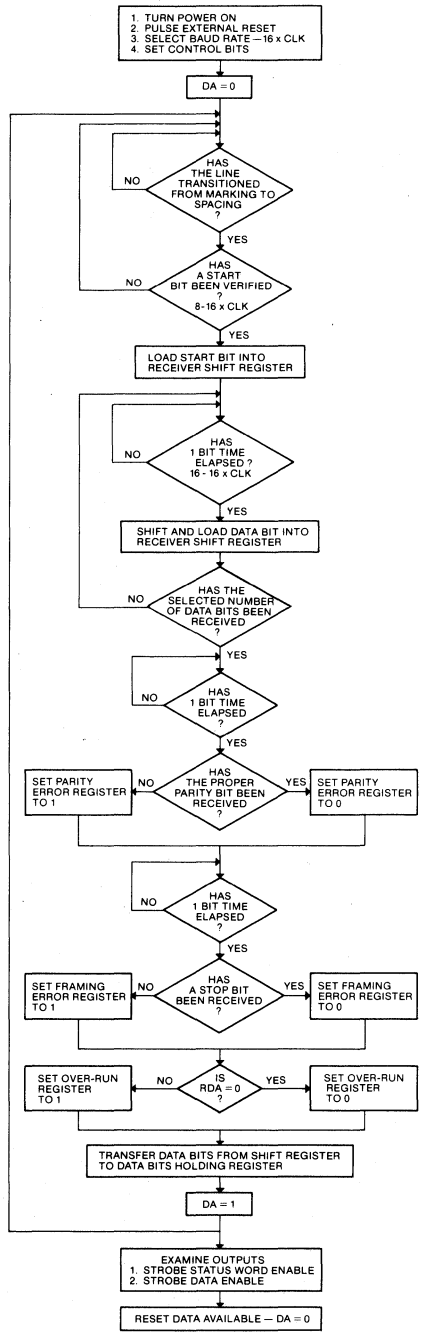




FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



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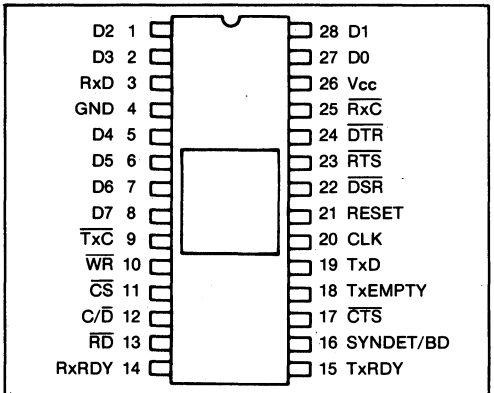
COM 8251A
μPC FAMILY

Universal Synchronous/Asynchronous Receiver/Transmitter USART

FEATURES

- ☐ Asynchronous or Synchronous Operation
  - —Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate—1, 16 or 64 X Baud Rate
    - Break Character Generation
    - 1, 1½ or 2 Stop Bits
    - False Start Bit Detection
    - Automatic Break Detect and Handling
  - —Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
    - Programmable Sync Character(s)
- ☐ Baud Rate—Synchronous—DC to 64K Baud
  —Asynchronous—DC to 9.6K Baud
- ☐ Baud Rates available from SMC's COM 8116, COM 8126, COM 8136, COM 8146, and COM 8046
- ☐ Full Duplex, Double Buffered Transmitter and Receiver
- ☐ Odd parity, even parity or no parity bit
- ☐ Parity, Overrun and Framing Error Flags
- ☐ Modem Interface Controlled by Processor
- ☐ All Inputs and Outputs are TTL Compatible

PIN CONFIGURATION



PACKAGE: 28-pin D.I.P.

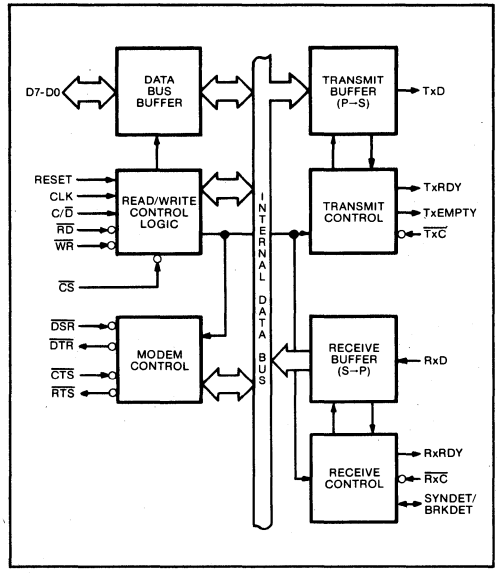
- ☐ Compatable with Intel 8251A, NEC μPD8251A
- ☐ Single +5 Volt Supply
- ☐ Separate Receive and Transmit TTL Clocks
- ☐ Enhanced version of 8251
- ☐ 28 Pin Plastic or Ceramic DIP Package
- ☐ COPLAMOS® N-Channel MOS Technology

GENERAL DESCRIPTION

The COM 8251A is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology that meets the majority of asynchronous and synchronous data communication requirements by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM 8251A is an enhanced version of the 8251.

The COM 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asychronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status, including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1, 2, 27, 28, 5-8	D2, D3, D0, D1, D4-D7	DATA BUS	I/O	An 8-bit, 3-state bi-directional DATA BUS used to interface the COM 8251A to the processor data bus. Data is transmitted or received by the bus in response to input/output or Read/Write instructions from the processor. The DATA BUS also transfers Control words, Command words, and Status.
3	RxD	RECEIVER DATA	I	This input receives serial data into the USART.
4	GND	GROUND	GND	Ground
9	$\overline{TxC}$	$\overline{TRANSMITTER\ CLOCK}$	I	The $\overline{TRANSMITTER\ CLOCK}$ controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1X, 16X, or 64X the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
10	$\overline{WR}$	$\overline{WRITE\ DATA}$	I	A "zero" on this input instructs the COM 8251A to accept the data or control word which the processor is writing out to the USART via the DATA BUS.
11	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	A "zero" on this input enables the USART for reading and writing to the processor. When $\overline{CS}$ is high, the DATA BUS is in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.
12	C/$\overline{D}$	CONTROL/$\overline{DATA}$	I	The Control/$\overline{Data}$ input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the DATA BUS. 0 = Data; 1 = Control/Status
13	$\overline{RD}$	$\overline{READ\ DATA}$	I	A "zero" on this input instructs the COM 8251A to place the data or status information onto the DATA BUS for the processor to read.
14	RxRDY	RECEIVER READY	O	The RECEIVER READY output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
15	TxRDY	TRANSMITTER READY	O	TRANSMITTER READY signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information polled operaton. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the processor.
16	SYNDET/ BRKDET	SYNC DETECT/ BREAK DETECT	I/O	The SYNDET feature is only used in the Synchronous mode. The USART may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal SYNC mode, the SYNDET output will go to a "one" when the COM 8251A has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second contiguously detected SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input is sampled during the negative half cycle of $\overline{RxC}$ and will cause the COM 8251A to start assembling data character on the next rising edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the COM 8251A is in SYNC. When external SYNC DETECT is programmed, the internal SYNC $\overline{DETECT}$ is disabled.

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
16 (cont.)				The SYNDET/BRKDET pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the BREAK DETECT output will go high when an all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx Data returns to a logic one state or upon chip RESET. The state of BREAK DETECT can also be read as a status bit.
17	$\overline{CTS}$	$\overline{CLEAR\ TO\ SEND}$	I	A "zero" on the $\overline{CLEAR\ TO\ SEND}$ input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one). If either a TxEN off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART written prior to the Tx Disable command before shutting down.
18	TxE	TRANSMITTER EMPTY	O	The TRANSMITTER EMPTY output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around". The TxEN bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a SYNC character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded; an underflow condition. If the USART is operating in the two SYNC character mode, both SYNC characters will be transmitted before the message can resume. TxE does not go low when the SYNC characters are being shifted out. TxE goes low upon the processor writing a character to the USART.
19	TxD	TRANSMITTER DATA	O	This output is the transmitted serial data from the USART. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed.
20	CLK	CLOCK PULSE	I	The CLK input provides for internal device timing. External inputs and outputs are not referenced to CLK, but the CLK frequency must be greater than 30 times the RECEIVER or TRANSMITTER CLOCKS in the 1X mode and greater than 4.5 times for the 16X and 64X modes.
21	RESET	RESET	I	A "one" on this input forces the USART into the "idle" mode where it will remain until reinitialized with a new set of control words. RESET causes: RxRDY = TxRDY = TxEmpty = SYNDET/BRKDET = 0; TxD = $\overline{DTR}$ = $\overline{RST}$ = 1. Minimum RESET pulse width is 6 t_{CY}, CLK must be running during RESET.
22	$\overline{DSR}$	$\overline{DATA\ SET\ READY}$	I	The $\overline{DATA\ SET\ READY}$ input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
23	$\overline{RTS}$	$\overline{REQUEST\ TO\ SEND}$	O	The $\overline{REQUEST\ TO\ SEND}$ output is controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
24	$\overline{DTR}$	$\overline{DATA\ TERMINAL\ READY}$	O	The $\overline{DATA\ TERMINAL\ READY}$ output is controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
25	$\overline{RxC}$	$\overline{RECEIVER\ CLOCK}$	I	The $\overline{RECEIVER\ CLOCK}$ is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1, 16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1X, 16X or 64X or Synchronous operation at 1X the Baud Rate. Data is sampled into the USART on the rising edge of $\overline{RxC}$.
26	V_{CC}	V_{CC} SUPPLY VOLTAGE	PS	+5 volt supply

DESCRIPTION OF OPERATION—ASYNCHRONOUS

Transmission—

When a data character is written into the USART, it automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at a transmission rate of $\overline{TxC}$, $\overline{TxC}$/16 or $\overline{TxC}$/64, as defined by the Mode Instruction.

If no data characters have been loaded into the USART, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

Receive—

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge (high to low transition) at RxD signals the possible beginning of a START bit and a new character. The receiver is thus prevented from starting in a "BREAK" state. The START bit is verified by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After the STOP bit time, the input character is loaded into the paralled Data Bus Buffer of the USART and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

DESCRIPTION OF OPERATION—SYNCHRONOUS

Transmission—

As in Asynchronous transmission, the TxD output remains "high" (marking) until the USART receives the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ at the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Data Protocols require that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the USART Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until the new data characters are available for transmission. If the USART becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

Receive—

In Synchronous receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, the ENTER HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the contents of the Receive Buffer are compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the (two contiguous) SYNC character(s) programmed have been detected, the USART leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost. Under this condition the Rx register will be cleared to all "ones".

OPERATION AND PROGRAMMING

The microprocessor program controlling the COM 8251A performs these tasks:

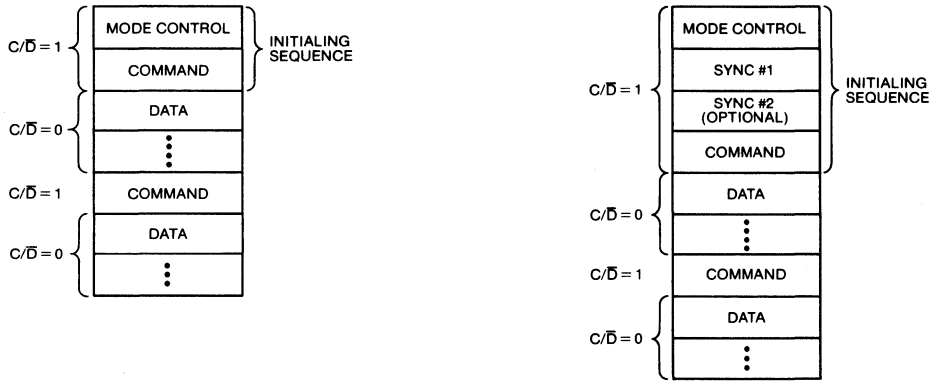
- Outputs control codes
- Inputs status
- Outputs data to be transmitted
- Inputs data which has been received

Control codes determine the mode in which the COM 8251A will operate and are used to set or reset control signals output by the COM 8251A.

The Status register contents will be read by the program monitoring this device's operation in order to determine error conditions, when and how to read data, write data or output control codes. Program logic may be based on reading status bit levels, or control signals may be used to request interrupts.

INITIALIZING THE COM 8251A

Figure 1. Control Word Sequences for Initialization



The COM 8251A may be initialized following a system RESET or prior to starting a new seral I/O sequence. The USART must be RESET (external or internal) following power up and subsequently may be reset at any time following completion of one activity and preceding a new set of operations. Following a reset, the COM 8251A enters an idle state in which it can neither transmit nor receive data.

The COM 8251A is initialized with two, three or four control words from the processor. Figure 1 shows the sequence of control words needed to initialize the COM 8251A, for synchronous or for asynchronous operation. Note that in asynchronous operation a mode control is output to the device followed by a command. For synchronous operation, the mode control is followed by one or two SYNC characters, and then a command.

Only a single address is set aside for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a RESET (external or internal), the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as SYNC characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following a RESET input or following an internal reset command. A reset operation (internal via IR or external via RESET) will cause the USART to interpret the next "control write", which should immediately follow the reset, as a Mode Instruction.

After receiving the control words the USART is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. Concurrently, the USART is ready to receive serial data.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	USART → Data Bus
0	1	0	0	Data Bus → USART
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

MODE CONTROL CODES

The COM 8251A interprets mode control codes as illustrated in Figures 2 and 3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse, as programmed. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character. In the case of a programmed character length of less than 8 bits, the least significant DATA BUS unused bits are "don't care" when writing data to the USART and will be "zeros" when reading data. Rx data will be right justified onto D0 and the LSB for Tx data is D0.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus in synchronous mode a character will consist of five, six, seven or eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1½ or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1½ stop bits can only be specified with a 16X or 64X baud rate factor. In these two cases, the half stop bit will be equivanlent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

COMMAND WORDS

Command words are used to initiate specific functions within the COM 8251A such as, "reset all error flags" or "start searching for sync". Consequently, Command Words may be issued by the processor to the COM 8251A at any time during the execution of a program in which specific functions are to be initialized within the communication circuit.

Figure 4 shows the format for the Command Word.

Figure 4. COM 8251A Control Command

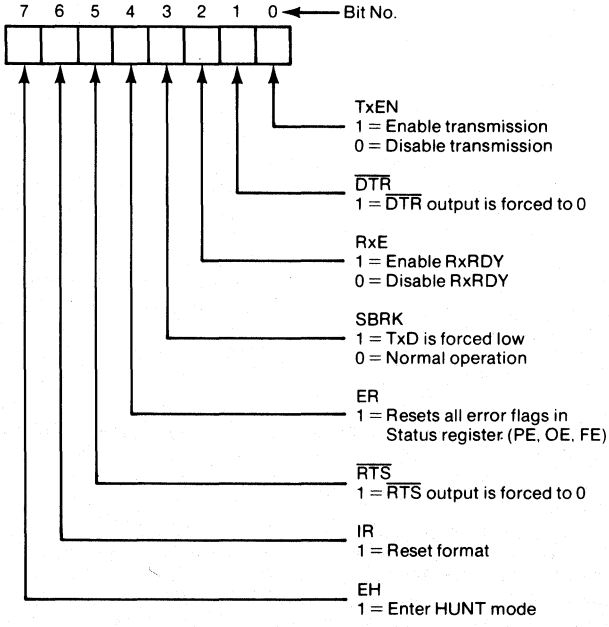


Figure 2. Synchronous Mode Control Code.

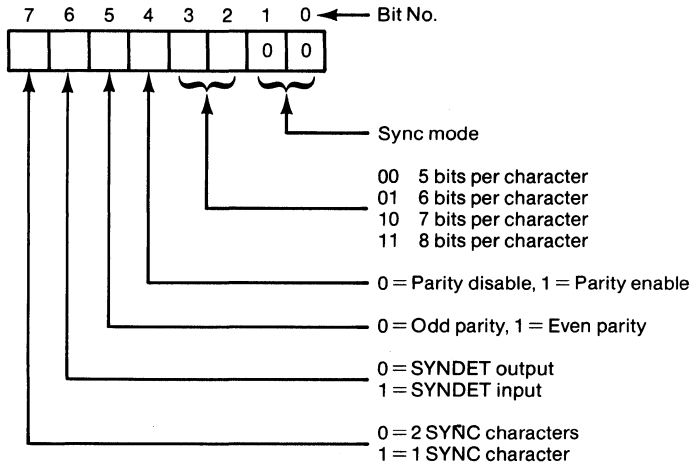
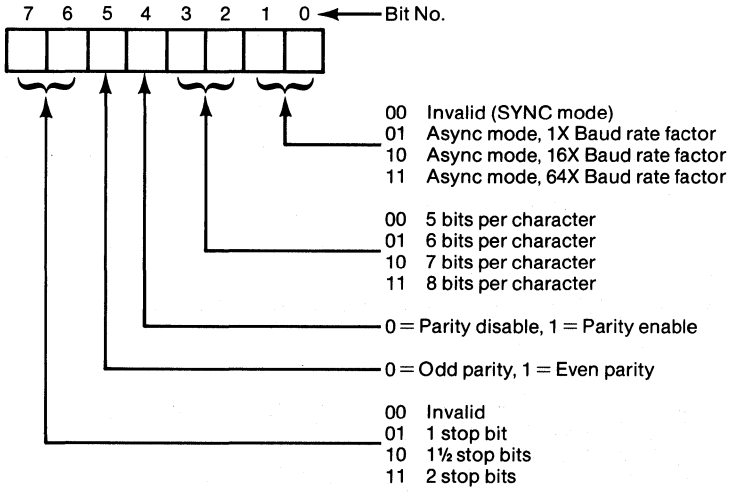


Figure 3. Asynchronous Mode Control Code.



Bit 0 of the Command Word is the Transmit Enable bit (TxEN). Data transmission for the COM 8251A cannot take place unless TxEN is set (assuming $\overline{CTS} = 0$) in the command register. The TX Disable command is prevented from halting transmission by the Tx Enable logic until all data previously written has been transmitted. Figure 5 defines the way in which TxEN, TxE and TxRDY combines to control transmitter operations.

Bit 1 is the Data Terminal Ready ($\overline{DTR}$) bit. When the $\overline{DTR}$ command bit is set, the $\overline{DTR}$ output connection is active (low). $\overline{DTR}$ is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the Receiver Enable Command bit (RxE). RxE is used to enable the RxRDY output signal. RxE, when zero, prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the Receive Character Buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and transferred to the Receiver Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

Figure 5.
Operation of the Transmitter Section as a Function of TxE, TxRDY and TxEN

TxEN	TxE	TxRDY	
1	1	1	Transmit Output Register and Transmit Character Buffer empty. TxD continues to mark if COM 8251A is in the asynchronous mode. TxD will send SYNC pattern if COM 8251A is in the Synchronous Mode. Data can be entered into Buffer.
1	0	1	Transmit Output Register is shifting a character. Transmit Character Buffer is available to receive a new byte from the processor.
1	1	0	Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission.
0	0/1	0/1	Transmitter is disabled.

Bit 3 is the Send Break Command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "0" level, (spacing) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the COM 8251A to remove SBRK.

Bit 4 is the Error Reset bit (ER). When a Command Word is transferred with the ER bit set, all three error flags (PE, OE, FE) in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the COM 8251A. No latch is provided in the Command Register to save the ER command bit.

Bit 5, the Request To Send Command bit ($\overline{RTS}$), sets a latch to reflect the $\overline{RTS}$ signal level. The output of this latch is created independently of other signals in the COM 8251A. As a result, data transfers may be made by the processor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of $\overline{RTS}$.

Bit 6, the Internal Reset (IR), causes the COM 8251A to return to the Idle mode. All functions within the COM 8251A cease and no new operation can be resumed until the circuit is reinitialized. If the operating mode is to be altered during the execution of a processor program, the COM 8251A must first be reset. Either the RESET input can be activated, or the Internal Reset Command can be sent to the COM 8251A. Internal Reset is a momentary function performed only when the command is issued.

Bit 7 is the Enter Hunt command bit (EH). The Enter Hunt mode command is only effective for the COM 8251A when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input, clear the Rx register to all "ones", and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will continue indefinitely until EH is reset when a subsequent Command Word is sent, when the IR command is sent to the COM 8251A, or when SYNC characters are recognized. Parity is not checked in the EH mode.

STATUS REGISTER

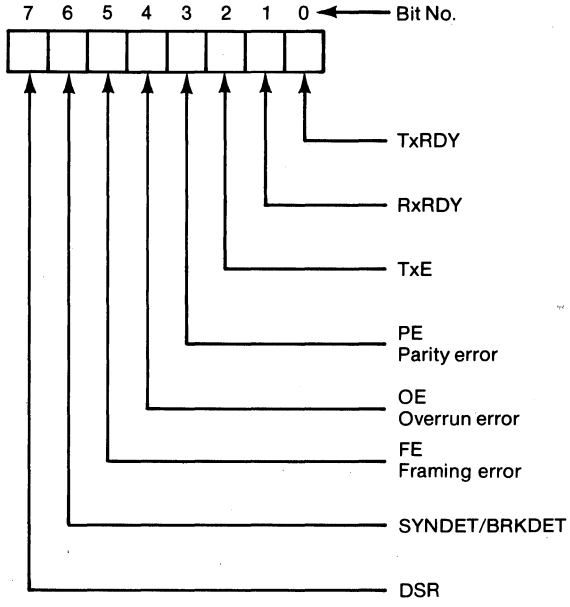
The Status Register maintains information about the current operational status of the COM 8251A. Status can be read at any time, however, the status update will be inhibited during status read. Figure 6 shows the format of the Status Register.

TxRDY signals the processor that the Transmit Character Buffer is empty and that the COM 8251A can accept a new character for transmission. The TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY (status bit) = Tx Character Buffer Empty
TxRDY (pin 15) = Tx Character Buffer Empty • $\overline{CTS}$ • TxEN

RxRDY signals the processor that a completed character is holding in the Receive Character Buffer Register for transfer to the processor.

Figure 6. The COM 8251A Status Register



TxE signals the processor that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits. PE does not inhibit USART operation. PE is reset by the ER bit.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before being transferred to the processor. OE does not inhibit USART operation. OE is reset by the ER bit.

FE (Async only) is the character framing error which indicates that the asynchronous mode byte stored in the Receiver Character Buffer was received with incorrect bit format ("0" stop bit), as specified by the current mode. FE does not inhibit USART operaton. FE is reset by the ER bit.

SYNDET is the synchronous mode status bit associated with internal or external sync detection.

DSR is the status bit set by the external $\overline{\text{Data Set Ready}}$ signal to indicate that the communication Data Set is operational.

All status bits are set by the functions described for them. SYNDET is reset whenever the processor reads the Status Register. OE, FE, PE are reset by the error reset command or the internal reset command or the RESET input. OE, FE, or PE being set does not inhibit USART operation.

Many of the bits in the status register are copies of external pins. This dual status arrangement allows the USART to be used in both Polled and Interrupt driven environments. Status update can have a maximum delay of 16 t_{CY} periods.

Note:

1. While operating the receiver it is important to realize that the RxE bit of the Command Instruction only inhibits the assertion of RxRDY; it does not inhibit the actual reception of characters. As the receiver is constantly running, it is possible for it to contain extraneous data when it is enabled. To avoid problems this data should be read from the USART and discarded. This read should be done immediately following the setting of the RxE bit in the asynchronous mode, and following the setting of EH in the synchronous mode. It is not necessary to wait for RxRDY before executing the dummy read.
2. ER should be performed whenever RxE of EH are programmed. ER resets all error flags, even if RxE = 0.
3. The USART may provide faulty RxRDY for the first read after power-on or for the first read after the receiver is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. This is not the case for the first read after hardware or software reset after the device opration has been established.
4. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through an internal flip-flop which clears itself, assuming the External Sync Detect assertion has removed, upon a status read. As long as External Sync Detect is asserted, External Sync Detect Status will remain high.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that as clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
D.C. Characteristics					
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.2$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu A$
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ TO 0.45V
I_{IL}	Input Leakage		±10	μA	$V_{IN} = V_{CC}$ TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High
Capacitance					$T_A = 25°C$, $V_{CC} = GND$
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND
A.C. Characteristics					
Bus Parameters (Note 1)					
Read Cycle:					
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	250		ns	
t_{RD}	Data Delay from $\overline{READ}$		200	ns	Note 3, $C_L = 150$ pF
t_{DF}	$\overline{READ}$ to Data Floating	10	100	ns	
Write Cycle:					
t_{AW}	Address Stable Before $\overline{WRITE}$	0		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	0		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	250		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	150		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	0		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4
Other Timings:					
t_{CY}	Clock Period	.320	1.35	μs	Notes 5, 6
t_{ϕ}	Clock High Pulse Width	120	$t_{CY}-90$	ns	
$t_{\overline{\phi}}$	Clock Low Pulse Width	90		ns	

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_R, t_F	Clock Rise and Fall Time	5	20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	
f_{Tx}	Transmitter Input Clock Frequency				
	1X Baud Rate	DC	64	kHz	
	16X Baud Rate	DC	310	kHz	
	64X Baud Rate	DC	615	kHz	
t_{TPW}	Transmitter Input Clock Width				
	1X Baud Rate	12		t_{CY}	
	16X and 64X Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1X Baud Rate	15		t_{CY}	
	16X and 64X Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1X Baud Rate	DC	64	kHz	
	16X Baud Rate	DC	310	kHz	
	64X Baud Rate	DC	615	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1X Baud Rate	12		t_{CY}	
	16X and 64X Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1X Baud Rate	15		t_{CY}	
	16X and 64X Baud Rate	3		t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		150	ns	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of last Bit		24	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		150	ns	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		24	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$		16	t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Data Bit		20	t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)		8	t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		20	t_{CY}	Note 7

NOTES: 1. AC timings measured $V_{OH} = 2.0$, $V_{OL} = 0.8$, and with load circuit of Figure 1.
2. Chip Select ($\overline{CS}$) and Command/$\overline{Data}$ ($C/\overline{D}$) are considered as Addresses.
3. Assumes that Address is valid before $R\overline{D}\downarrow$.
4. This recovery time is for RESET and Mode Initialization. Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.
5. The TxC and RxC frequencies have the following limitations with respect to CLK.
For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$
6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during RESET.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

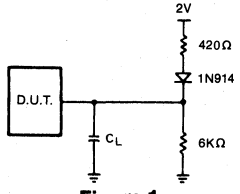
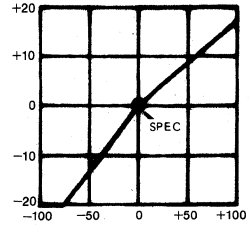


Figure 1.

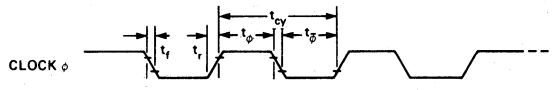
TEST LOAD CIRCUIT

Typical Δ Output Delay Versus Δ Capacitance (pF)

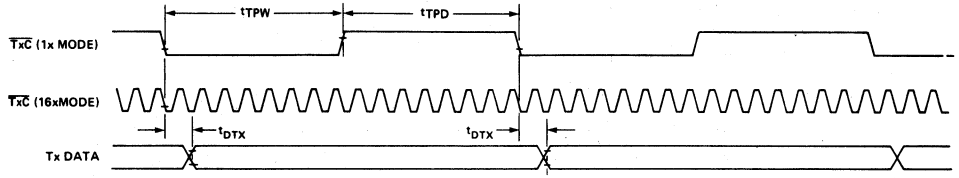


WAVEFORMS

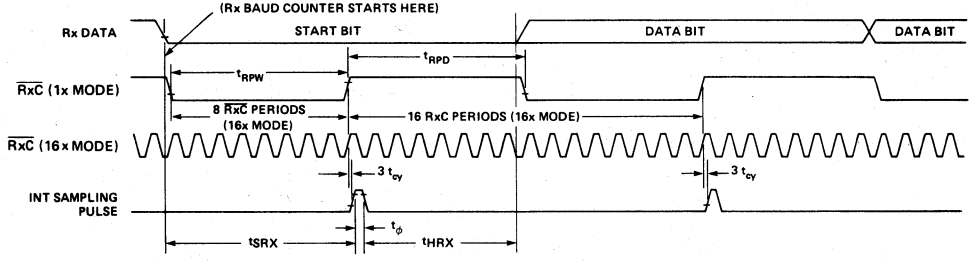
System Clock Input



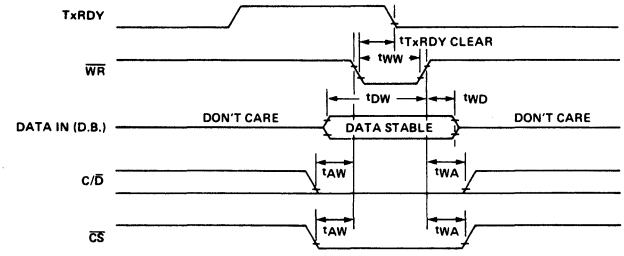
Transmitter Clock & Data



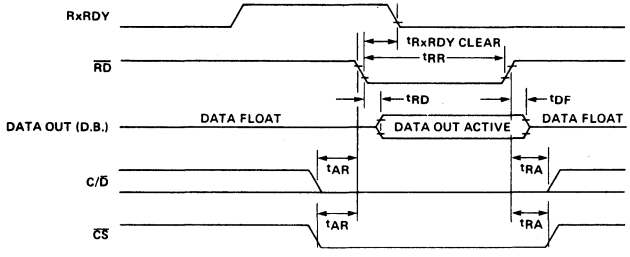
Receiver Clock & Data



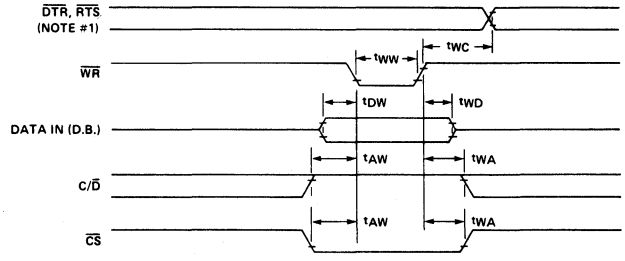
Write Data Cycle (CPU → USART)



Read Data Cycle (CPU ← USART)

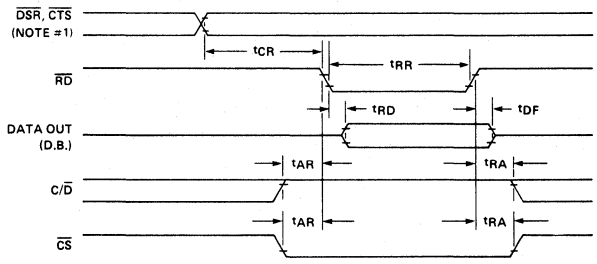


Write Control or Output Port Cycle (CPU → USART)



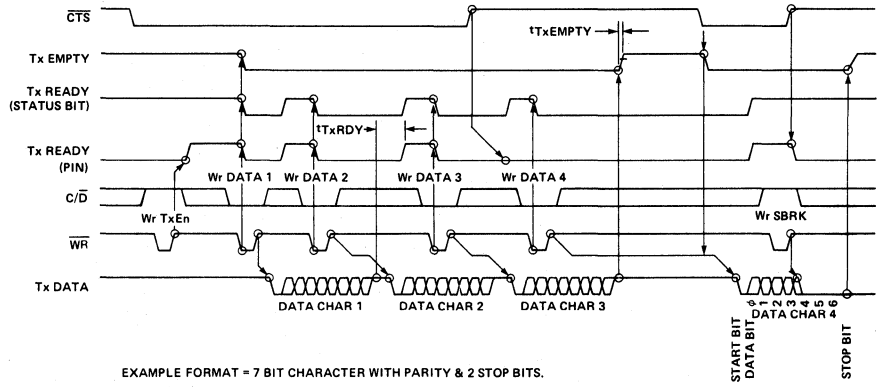
NOTE #1: T_{WC} INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE.

Read Control or Input Port (CPU ← USART)



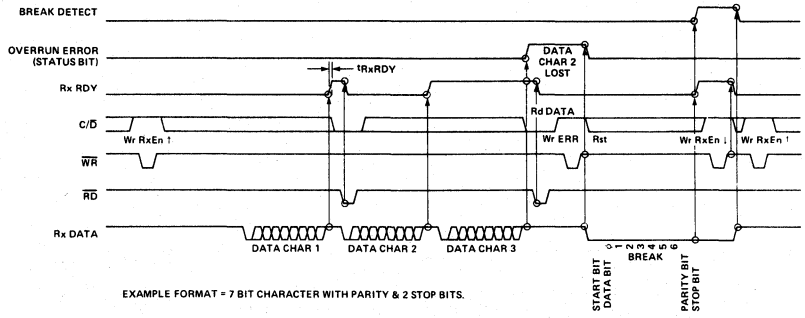
NOTE #1: T_{CR} INCLUDES THE EFFECT OF $\overline{CTS}$ ON THE TxENBL CIRCUITRY.

Transmitter Control & Flag Timing (ASYNC Mode)



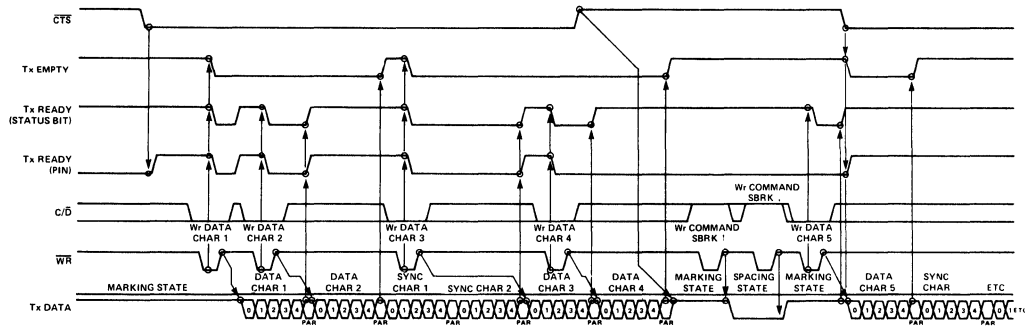
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

Receiver Control & Flag Timing (ASYNC Mode)



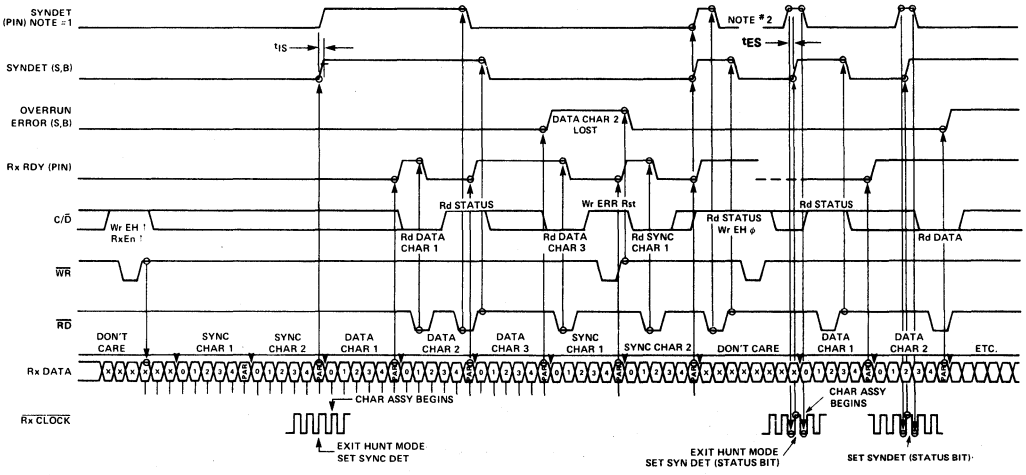
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

Transmitter Control & Flag Timing (SYNC Mode)



EXAMPLE FORMAT = 5 BIT CHARACTER WITH PARITY, 2 SYNC CHARACTERS.

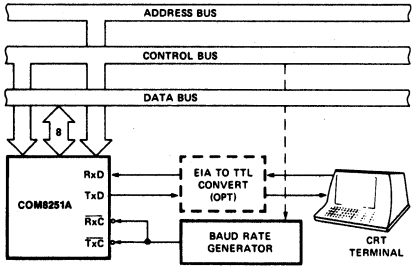
Receiver Control & Flag Timing (SYNC Mode)



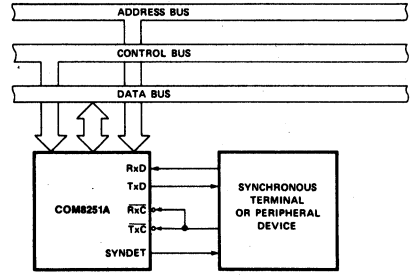
NOTE #1: INTERNAL SYNC, 2 SYNC CHARACTERS, 5 BITS, WITH PARITY
NOTE #2: EXTERNAL SYNC, 5 BITS, WITH PARITY

APPLICATION OF THE COM8251A

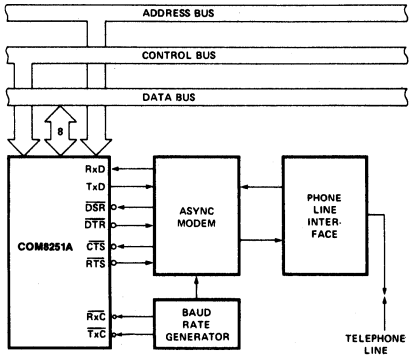
Asynchronous Serial Interface to CRT Terminal, DC to 9600 Baud



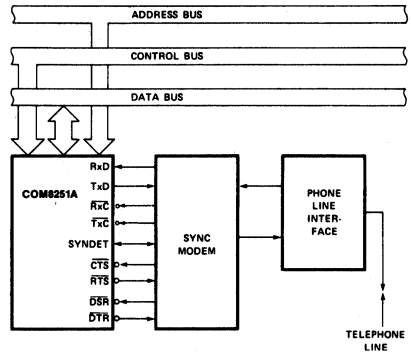
Synchronous Interface to Terminal or Peripheral Device



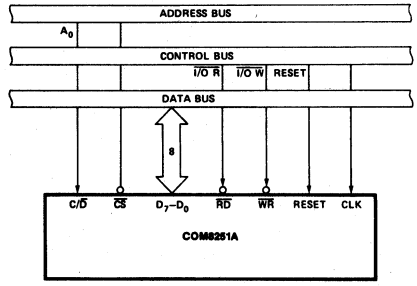
Asynchronous Interface to Telephone Lines



Synchronous Interface to Telephone Lines



COM8251A Interface to μP Standard System Bus



CRT Display

VTAC® TIMING CONTROLLERS

Part Number	Description	Features	Display Format	Max Clock	Power Supplies	Package	Page
CRT 5027	provides all of the timing and control for interlaced and non-interlaced CRT display		programmable	4 MHz	+5, +12	40 DIP	121-128
CRT 5037		balanced beam interlace	programmable	4 MHz	+5, +12	40 DIP	121-128
CRT 5047[3]		fixed format	80 column 24 row	4 MHz	+5, +12	40 DIP	129-130
CRT 5057		line-lock	programmable	4 MHz	+5, +12	40 DIP	121-128
CRT 9007[1]	CRT video processor and controller	sequential or row-table driven memory	programmable	4 MHz	+5	40 DIP	131-134
CRT 96364A/B	complete CRT processor	on-chip cursor and write control	64 column 16 row	1.6 MHz	+5	28 DIP	137-144

SECTION IV

VDAC™ DISPLAY CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supply	Package	Page
CRT 8002A[2,3]	Provides complete display and attributes control for alphanumeric and graphics display. Consists of 7x11x128 character generator, video shift register, latches, graphics and attributes circuits.	7x11 dot matrix, wide graphics, thin graphics. on-chip cursor	reverse video blank blink underline strike-thru	20 MHz	+5	28 DIP	145-154
CRT 8002B[2,3]				15 MHz			
CRT 8002C[2,3]				10 MHz			

CHARACTER GENERATORS

Part Number	Description	Max Frequency	Power Supply	Package	Page
CRT 7004A[3,4]	7x11x128 character generator, latches, video shift register	20 MHz	+5	24 DIP	155-159
CRT 7004B[3,4]		15 MHz			
CRT 7004C[3,4]		10 MHz			

ROW BUFFER

Part Number	Description	Max Row Length	Power Supply	Package	Page
CRT 9006-83[1]	8 bit wide serial cascadable row buffer memory for CRT or printer	83 characters	+5	24 DIP	135-136
CRT 9006-135		135 characters			

[1] For future release
[2] Also available as CRT 8002A,B,C-001 Katakana
CRT 8002A,B,C-003 5X7 dot matrix
[3] May be custom mask programmed
[4] Also available as CRT 7004A,B,C-003 5X7 dot matrix

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11787
(516) 273-3100 · TWX-510-227-8898

We keep ahead of our competition so you can keep ahead of yours.

CRT 5027
CRT 5037
CRT 5057*

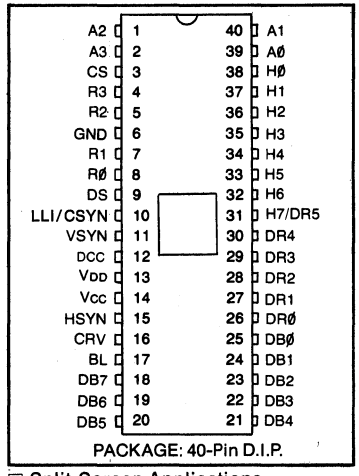
μPC FAMILY

CRT Video Timer and Controller
VTAC®

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (1-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Lock Line Input (CRT 5057)
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync (CRT 5027, CRT 5037)
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask Option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60Hz, 50Hz,...
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Character Format: 5x7, 7x9,...
- ☐ Programmable Vertical Data Positioning
- ☐ Balanced Beam Current Interlace (CRT 5037)
- ☐ Graphics Compatible

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
- ☐ Interlace or Non-Interlace operation
- ☐ TTL Compatibility
- ☐ BUS Oriented
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology
- ☐ Compatible with CRT 8002 VDAC™
- ☐ Compatible with CRT 7004

GENERAL DESCRIPTION

The CRT Video Timer and Controller Chip (VTAC)® is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

Three versions of the VTAC® are available. The CRT 5027 provides non-interlaced operation with an even or odd number of scan lines per data row, or interlaced operation with an even number of scan lines per data row. The CRT 5037 may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes. Programming the CRT 5037 for an odd number of scan lines per data row eliminates character distortion caused by the uneven beam current normally associated with odd field/even field interlacing of alphanumeric displays.

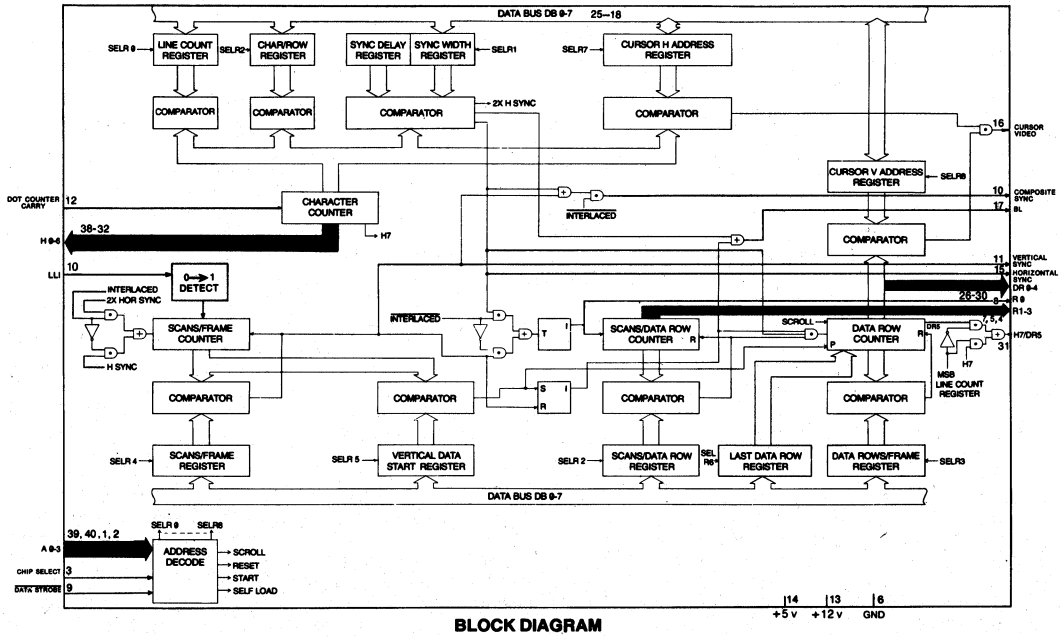
The CRT 5057 provides the ability to lock a CRT's vertical refresh rate, as controlled by the VTAC's® vertical sync pulse, to the 50 Hz or 60 Hz line frequency thereby eliminating the so called "swim" phenomenon. This is particularly well suited for European system requirements. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to the line lock input. The VTAC® will inhibit generation of vertical sync until a zero to one transition on this input is detected. The vertical sync pulse is then initiated within one scan line after this transition rises above the logic threshold of the VTAC.®

To provide the pin required for the line lock input, the composite sync output is not provided in the CRT 5057.

*FOR FUTURE RELEASE

Description of Pin Functions

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DBØ-7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that it is being addressed
39, 40, 1, 2	AØ-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
9	$\overline{DS}$	Data Strobe	I	Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
12	DCC	DOT Counter Carry	I	Carry from off chip dot counter establishing basic character clock rate. Character clock.
38-32	HØ-6	Character Counter Outputs	O	Character counter outputs.
7, 5, 4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line count (REG.Ø) is ≥128; otherwise output is MSB of Data Row Counter.
8	RØ	Scan Counter LSB	O	Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, RØ will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, RØ will toggle at the data row rate.
26-30	DRØ-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN/ LLI	Composite Sync Output/ Line Lock Input	O/I	Composite sync is provided on the CRT 5027 and CRT 5037. This output is active in non-interlaced mode only. Provides a true RS-170 composite sync wave form. For the CRT 5057, this pin is the Line Lock Input. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to this pin.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	V_{CC}	Power Supply	PS	+5 volt Power Supply
13	V_{DD}	Power Supply	PS	+12 volt Power Supply



BLOCK DIAGRAM

Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:	
Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 15 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.
Vertical Formatting:	
Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (≡ 3H).
Vertical Data Start	8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is set to the data row address at the top of the page.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

SECTION IV

Additional Features

Device Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a 1Ø1Ø address on A3-Ø. The device will remain reset at the top of the even field page until a start command is executed by presenting a 111Ø address on A3-Ø.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on A3-Ø, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the Ø111 address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 1Ø11) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

Control Registers Programming Chart

Horizontal Line Count: Total Characters/Line = N + 1, N = 0 to 255 (DB0 = LSB)

Characters/Data Row:

DB2	DB1	DB0		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay: = N, from 1 to 7 character times (DB0 = LSB) (N = 0 Disallowed)

Horizontal Sync Width: = N, from 1 to 15 character times (DB3 = LSB) (N = 0 Disallowed)

Skew Bits

DB7	DB6	Sync/Blank Delay (Character Times)	Cursor Delay
0	0	0	0
1	0	1	0
0	1	2	1
1	1	2	2

Scans/Frame 8 bits assigned, defined according to the following equations:
Let X = value of 8 assigned bits. (DB0 = LSB)

1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.

Range = 513 to 1023 scans/frame, odd counts only.

2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).

Range = 256 to 766 scans/frame, even counts only.

In either mode, vertical sync width is fixed at three horizontal scans (=3H).

Vertical Data Start: N = number of raster lines delay after leading edge of vertical sync of vertical start position. (DB0 = LSB)

Data Rows/Frame: Number of data rows = N + 1, N = 0 to 63 (DBO = LSB)

Last Data Row: N = Address of last dsplayed data row, N = 0 to 63, ie; for 24 data rows, program N = 23. (DB0 = LSB)

Mode: Register, 1, DB7 = 1 establishes Interlace.

Scans/Data Row:

Interlace Mode

CRT 5027: Scans per Data Row = N + 1 where N = programmed number of data rows. N = 0 to 15. Scans per data row must be even counts only.

CRT 5037, CRT 5057: Scans per data Row = N + 2. N = 0 to 14, odd or even counts.

Non-Interlace Mode

CRT 5027, CRT 5037, CRT 5057: Scans per Data Row = N + 1, odd or even count. N = 0 to 15.

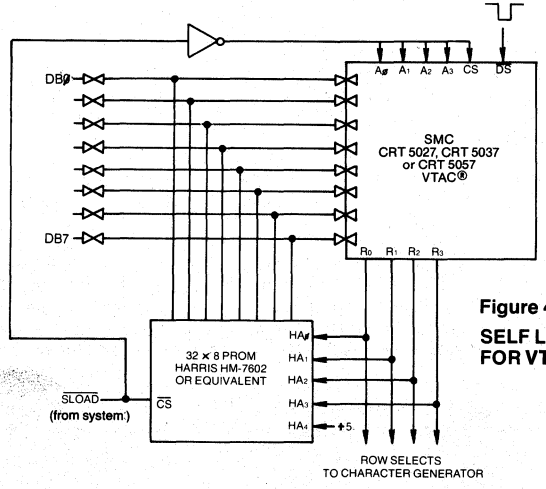


Figure 4.
SELF LOADING SCHEME FOR VTAC® SET-UP

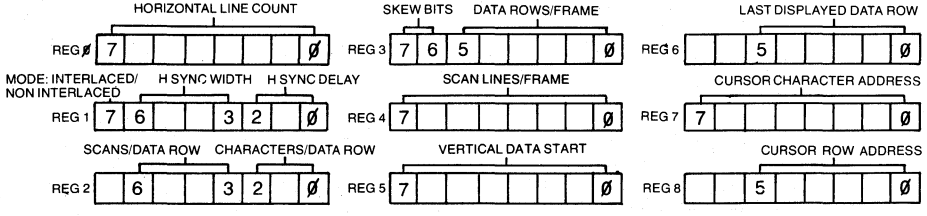
Register Selects/Command Codes

A3	A2	A1	AØ	Select/Command	Description
0	0	0	0	Load Control Register Ø	See Table 1
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Initiated Self Load	Command from processor instructing VTAC® to enter Self Load Mode (via external PROM)
1	0	0	0	Read Cursor Line Address	
1	0	0	1	Read Cursor Character Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address*	
1	1	0	1	Load Cursor Line Address*	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on A3-Ø long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one VTAC®, the Dot Counter Carry should be held low when the command is removed.

*NOTE: During Self-Load, the Cursor Character Address Register (REG 7) and the Cursor Row Address Register (REG 8) are enabled during states Ø111 and 1ØØØ of the R3-RØ Scan Counter outputs respectively. Therefore, Cursor data in the PROM should be stored at these addresses.

TABLE 1

BIT ASSIGNMENT CHART



AC TIMING DIAGRAMS

FIGURE 1 VIDEO TIMING

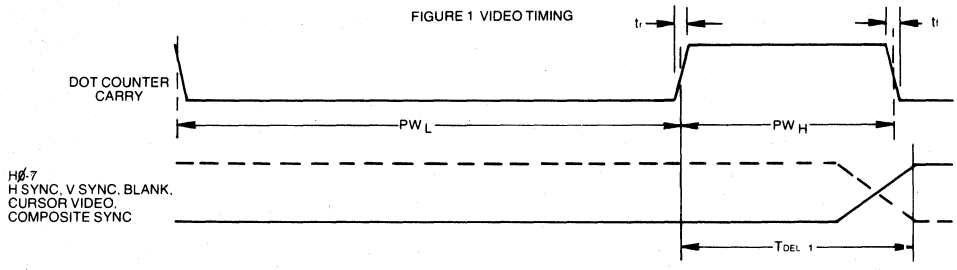


FIGURE 2 LOAD/READ TIMING

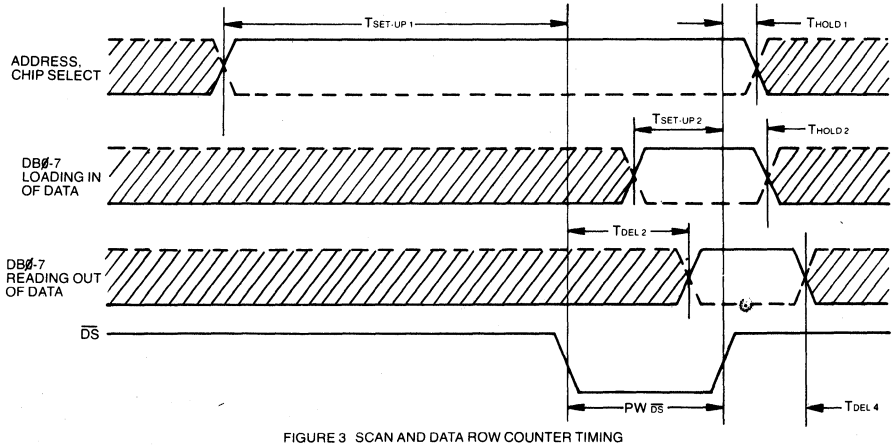
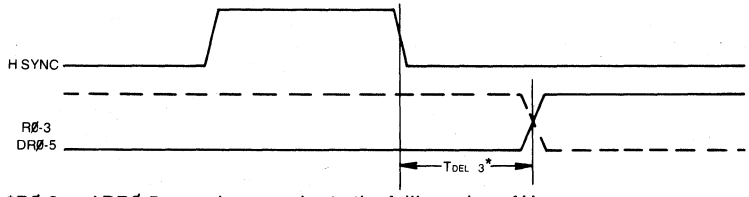
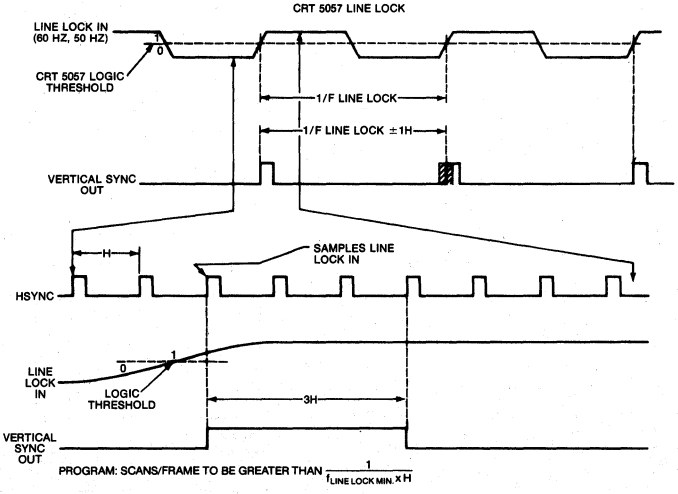


FIGURE 3 SCAN AND DATA ROW COUNTER TIMING



*RØ-3 and DRØ-5 may change prior to the falling edge of H sync



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

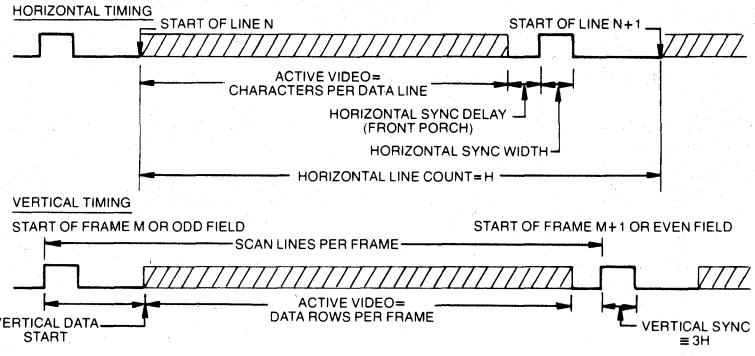
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}−1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level—V_{OL} for RØ-3			0.4	V	I_{OL}=3.2ma
Low Level—V_{OL} all others			0.4	V	I_{OL}=1.6ma
High Level—V_{OH} for RØ-3, DBØ-7	2.4				I_{OH}=80μa
High Level—V_{OH} all others	2.4				I_{OH}=40μa
INPUT CURRENT					
Low Level, I_{IL} (Address, CS only)			250	μA	V_{IN}=0.4V
Leakage, I_{IL} (All Inputs except Address, CS)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data Bus, C_{IN}		10	15	pF	
$\overline{DS}$, Clock, C_{IN}		25	40	pF	
All other, C_{IN}		10	15	pF	
DATA BUS LEAKAGE in INPUT MODE					
I_{DB}			10	μA	$0.4V \leq V_{IN} \leq 5.25V$
POWER SUPPLY CURRENT					
I_{CC}		80	100	mA	
I_{DD}		40	70	mA	
A.C. CHARACTERISTICS					T_A = 25°C
DOT COUNTER CARRY					
frequency	0.2		4.0	MHz	Figure 1
PW_H	35			ns	Figure 1
PW_L	215			ns	Figure 1
t_r, t_f		10	50	ns	Figure 1
DATA STROBE					
$PW_{\overline{DS}}$	150ns		10μs		Figure 2
ADDRESS, CHIP SELECT					
Set-up time	125			ns	Figure 2
Hold time	50			ns	Figure 2
DATA BUS—LOADING					
Set-up time	125			ns	Figure 2
Hold time	75			ns	Figure 2
DATA BUS—READING					
T_{DEL2}			125	ns	Figure 2, CL=50pF
T_{DEL4}	5		60	ns	Figure 2, CL=50pF
OUTPUTS: HØ-7, HS, VS, BL, CRV, CS-T_{DEL1}			125	ns	Figure 1, CL=20pF
OUTPUTS: RØ-3, DRØ-5					
T_{DEL3}	*		750	ns	Figure 3, CL=20pF

*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

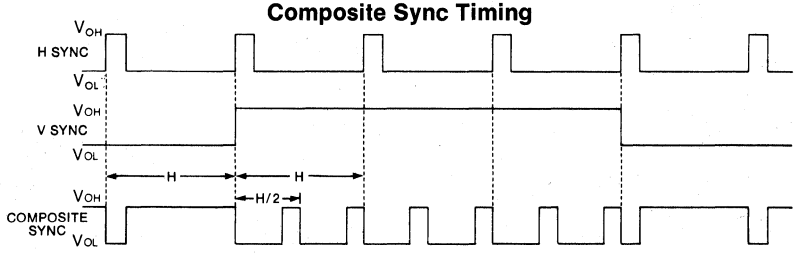
Restrictions

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputed by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe ($\overline{DS}$) signal to the device.
2. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

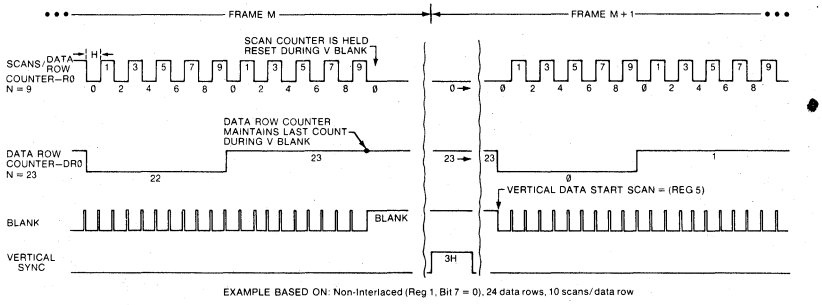
General Timing



Composite Sync Timing



Vertical Sync Timing



EXAMPLE BASED ON: Non-Interlaced (Reg 1, Bit 7 = 0), 24 data rows, 10 scans/data row

Start-up, CRT 5027

When employing microprocessor controlled loading of the CRT 5027's registers, the following sequence of instructions is necessary:

ADDRESS	COMMAND
1 1 1 0	Start Timing Chain
1 0 1 0	Reset
0 0 0 0	Load Register 0
.	.
.	.
.	.
0 1 1 0	Load Register 6
1 1 1 0	Start Timing Chain

The sequence of START RESET LOAD START is necessary to insure proper initialization of the registers.

This sequence is not required if register loading is via either of the Self Load modes. This sequence is optional with the CRT 5037 or CRT 5057.

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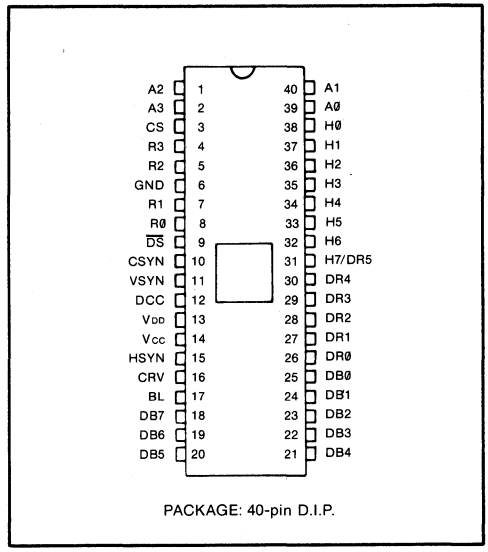
We keep ahead of our competition so you can keep ahead of yours.

Preprogrammed CRT Video Timer and Controller VTAC®

FEATURES

- ☐ Preprogrammed (Mask-Programmed) Display Format
  - 80 Characters Per Data Row
  - 24 Data Rows Per Frame
  - 9 Scan Lines Per Data Row
- ☐ Preprogrammed Monitor Sync Format
  - 262 Scan Lines Per Frame
  - 6 Character Times for Horizontal Front Porch
  - 8 Character Times for Horizontal Sync Width
  - 6 Character Times for Horizontal Back Porch
  - 16 Scan Lines for Vertical Front Porch
  - 3 Scan Lines for Vertical Sync Width
  - 27 Scan Lines for Vertical Back Porch
  - Non-Interlace
  - 15.720KHz Horizontal Scan Rate
  - 60Hz Frame Refresh Rate
- ☐ Fixed Character Rate
  - 1.572MHz Character Rate (636.13ns/Character)
  - 11.004MHz Dot Rate (90.88ns/Dot) for 7 Dot Wide Character Block
- ☐ Character Format
  - 5 X 7 Character in a 7 X 9 Block
- ☐ Compatible with CRT 8002B-003 VDAC™
- ☐ Compatible with CRT 7004B-003
- ☐ May be mask-programmed with other display formats

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

SECTION IV

GENERAL DESCRIPTION

The two chip combination of SMC's CRT 5047 and CRT 8002B-003 effectively provide all of the video electronics for a CRT terminal. This chip set along with a μC form the basis for a minimum chip count CRT terminal.

The CRT 5047 Video Timer and Controller is a special version of the CRT 5037 VTAC® which has been ROM-programmed with a fixed format. It is especially effective for low-cost CRT terminals using an 80 X 24 display format with a 5 X 7 character matrix. The use of a fixed ROM program in the CRT 5047 eliminates the software overhead normally required to specify the display parameters and simplifies terminal software design.

The Cursor Character Address Register and the Cursor Row Address Register are the only two registers accessible by the processor. The CRT 5047 is easily initialized by the following sequence of commands:

Reset Load Control Register 6 Start Timing Chain

The parameters of the CRT 5047 have been selected to be compatible with most CRT monitors. The horizontal timing is programmed so that when the two character skew delay of the CRT 8002 VDAC™ is taken into account, the effective timing is: Horizontal Front Porch—four characters, and Horizontal Back Porch—eight characters.

Figure 1 shows the contents of the internal CRT 5047 registers. Other mask-programmed versions of the CRT 5037 are available. Consult SMC for more information.

VTAC® WORK SHEET

1. H CHARACTER MATRIX (No. of Dots): . 5
2. V CHARACTER MATRIX (No. of Horiz. Scan Lines): 7
3. H CHARACTER BLOCK (Step 1 + Desired Horiz. Spacing = No. in Dots): .. 7
4. V CHARACTER BLOCK (Step 2 + Desired Vertical Spacing = No. in Horiz. Scan Lines): 9
5. VERTICAL FRAME (REFRESH) RATE (Freq. in Hz): 60
6. DESIRED NO. OF DATA ROWS: 24
7. TOTAL NO. OF ACTIVE "VIDEO DISPLAY" SCAN LINES (Step 4 x Step 6 = No. in Horiz. Scan Lines): 216
8. VERT. SYNC DELAY (No. in Horiz. Scan Lines): 16
9. VERT. SYNC (No. in Horiz. Scan Lines; T= 190.8 μs*): 3
10. VERT. SCAN DELAY (No. in Horiz. Scan Lines; T= 1.718 ms*): 27
11. TOTAL VERTICAL FRAME (Add steps 7 thru 10 = No. in Horiz. Scan Lines): ... 262
12. HORIZONTAL SCAN LINE RATE (Step 5 x Step 11 = Freq. in KHz): 15.720
13. DESIRED NO. OF CHARACTERS PER HORIZ. ROW: 80
14. HORIZ. SYNC DELAY (No. in Character Time Units; T = 3.817 μs**): 6
15. HORIZ. SYNC (No. in Character Time Units; T = 5.090 μs**): 8
16. HORIZ. SCAN DELAY (No. in Character Time Units; T = 3.817 μs**): 6
17. TOTAL CHARACTER TIME UNITS IN (1) HORIZ. SCAN LINE (Add Steps 13 thru 16): 100
18. CHARACTER RATE (Step 12 x Step 17 = Freq. in MHz): 1.572
19. CLOCK (DOT) RATE (Step 3 x Step 18 = Freq. in MHz): 11.004

*Vertical Interval **Horizontal Interval

REG. #	ADDRESS A3 A0	FUNCTION	BIT ASSIGNMENT	HEX.	DEC.
0	0000	HORIZ. LINE COUNT 100	0 1 1 0 0 0 1 1	63	99
1	0001	INTERLACE 0 H SYNC WIDTH 8 H SYNC DELAY 6	0 1 0 0 0 1 1 0	46	70
2	0010	SCANS/DATA ROW 9 CHARACTERS/ROW 80	X 1 0 0 0 1 0 1	45	69
3	0011	SKEW CHARACTERS 0,0 DATA ROWS 24	0 0 0 1 0 1 1 1	17	23
4	0100	SCANS/FRAME 262 X = 3	0 0 0 0 0 0 1 1	03	03
5	0101	VERTICAL DATA START = 3 + VERTICAL SCAN DELAY: SCAN DELAY 27 DATA START 30	0 0 0 1 1 1 1 0	1E	30
6*	0110	LAST DISPLAYED DATA ROW (= DATA ROWS)	X X	–	–

*Register 6 has an initialization option. It is loaded with the data contained in Register 3 by a "Load Register 6" command. The "Up Scroll" command can be used to effect scrolling operations.

Figure 1: CRT 5047 Mask Programmed Registers

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CRT 9007*
μPC FAMILY

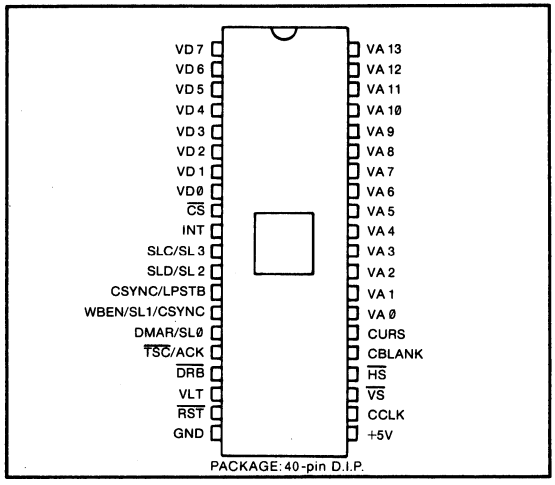
PRELIMINARY

CRT Video Processor and Controller VPAC

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per Data Row (8-240)
  - Data Rows per Frame (2-256)
  - Raster Scans per Data Row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (4-2048)
  - Front Porch — Horizontal (Negative or Positive)
  - — Vertical
  - Sync Width — Horizontal (1-128 Character Times)
  - — Vertical (2-256 Scan Lines)
  - Back Porch — Horizontal
  - — Vertical
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Composite Blanking
  - Cursor Coincidence
- ☐ Binary Addressing of Video Memory
- ☐ Row-Table Driven or Sequential Video Addressing Modes
- ☐ Programmable Status Row Position and Address Registers
- ☐ Bidirectional Partial or Full Page Smooth Scroll
- ☐ Attribute Assemble Mode
- ☐ Double Height Data Row Mode
- ☐ Double Width Data Row Mode
- ☐ Programmable DMA Burst Mode
- ☐ Configurable with a Variety of Memory Contention Arrangements
- ☐ Light Pen Register
- ☐ Cursor Horizontal and Vertical Position Registers
- ☐ Maskable Processor Interrupt Line
- ☐ Internal Status Register
- ☐ Three-state Video Memory Address Bus
- ☐ Partial or Full Page Blank Capability
- ☐ Two Interlace Modes: Enhanced Video and Alternate Scan Line

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

- ☐ Ability to Delay Cursor and Blanking with respect to Active Video
- ☐ ROM Version for Vital Screen Parameters
- ☐ Programmable for Horizontal Split Screen Applications
- ☐ Graphics Compatible
- ☐ Ability to Externally Sync each Raster Line, each Field
- ☐ Single +5 Volt Power Supply
- ☐ TTL Compatible on All Inputs and Outputs
- ☐ One Pin Processor Interface
- ☐ VT-100 Compatible
- ☐ RS-170 Interlaced Composite Sync Available

GENERAL DESCRIPTION

The CRT 9007 VPAC is a next generation video processor/controller — an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the VPAC provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register shown in Figure 1 points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode each row in the video dispay is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The VPAC works with a variety of memory contention schemes including operation with a Single Row Buffer such as the CRT 9006 (Figure 2), a Double Row Buffer (Figure 3), or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and VPAC status. Twelve of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 12 registers contain the "vital screen parameters". An alternate high volume version of the chip contains these parameters in ROM such that chip initialization is unnecessary.

*For Future Release

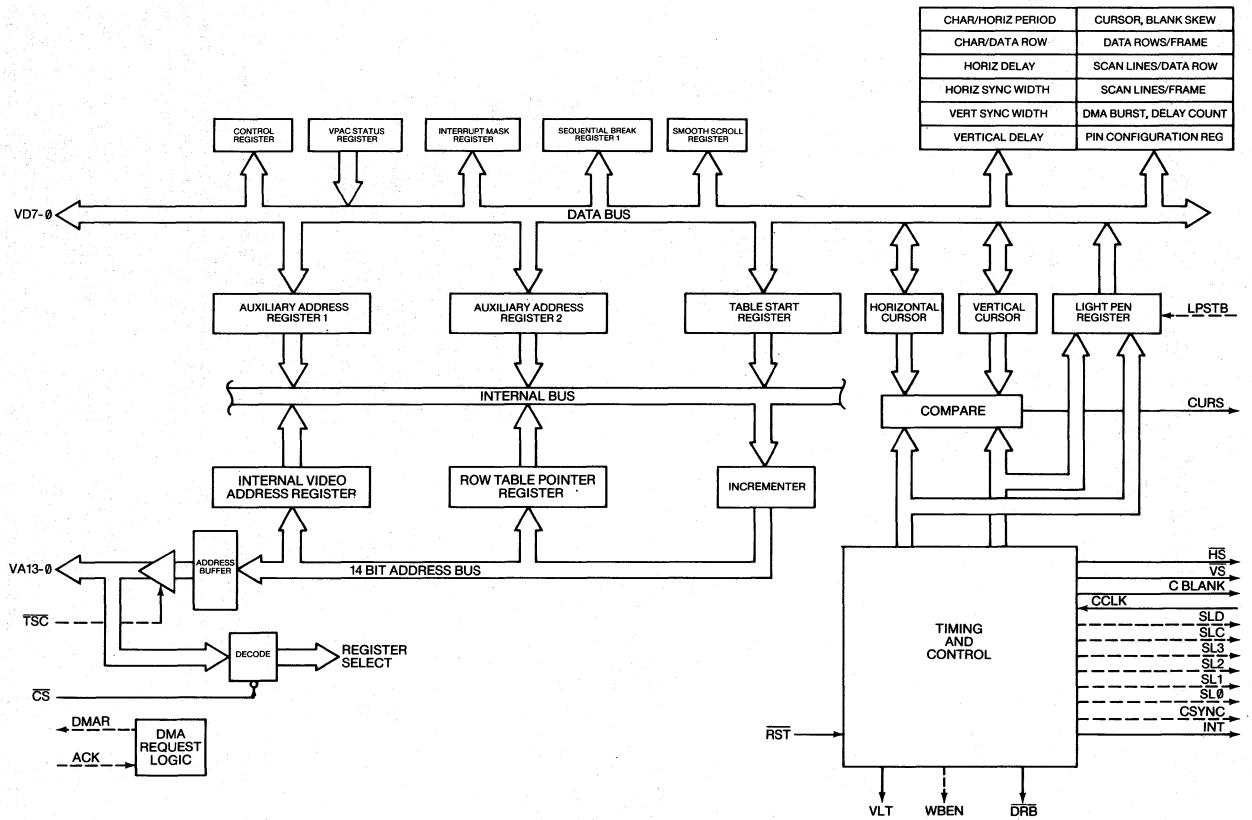


Figure 1. CRT9007 Block Diagram

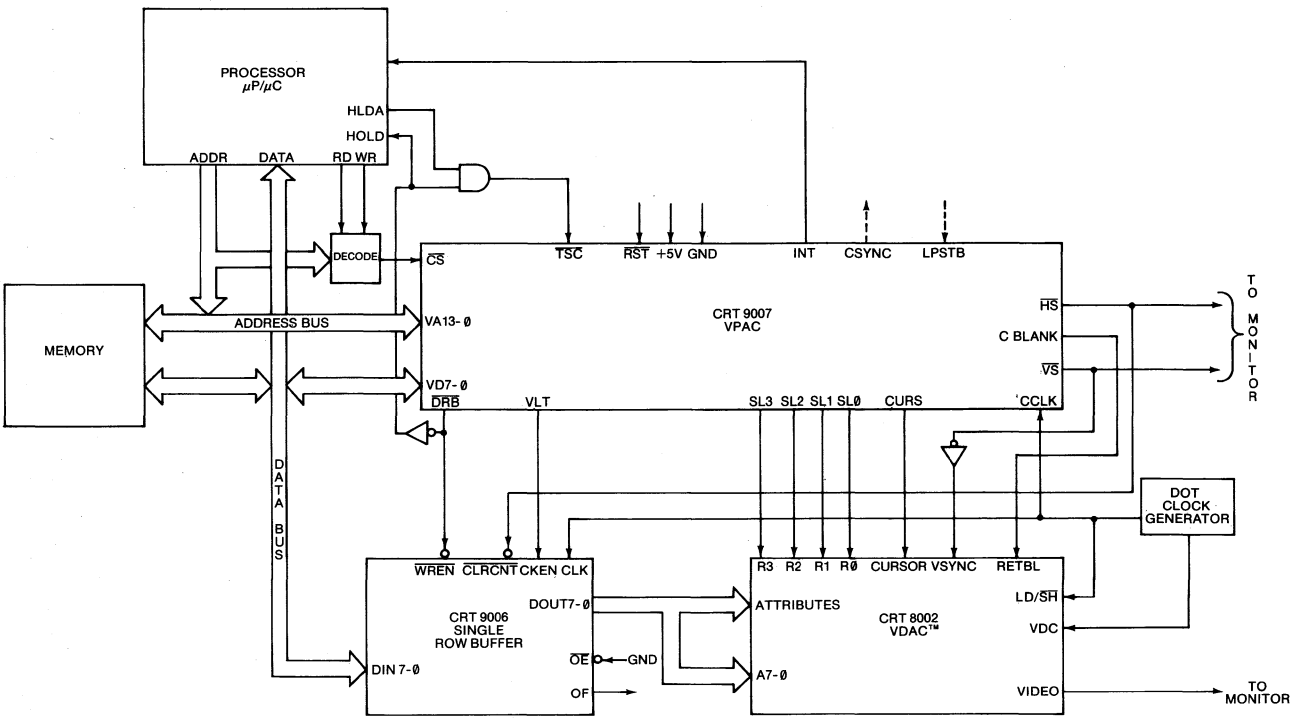


Figure 2. VPAC Configuration With Single Row Buffer

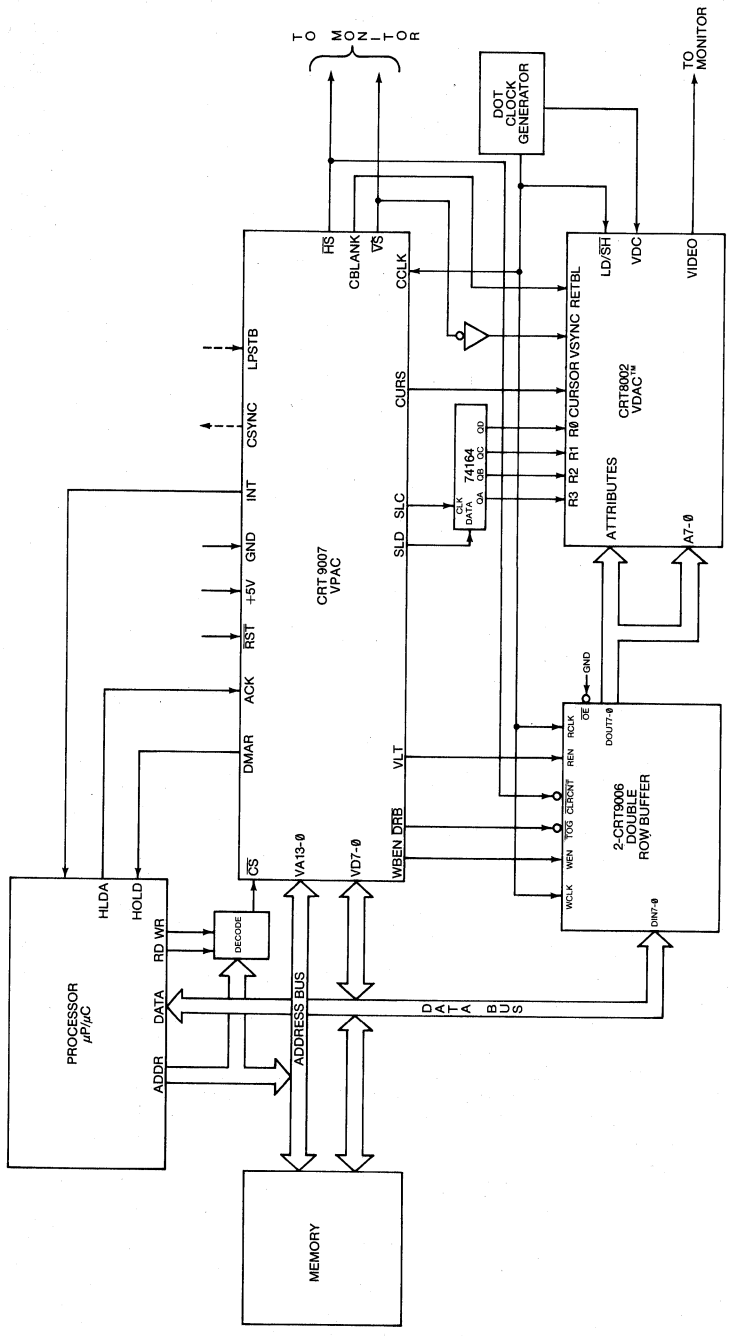


Figure 3. VPAC Configuration With Double Row Buffer

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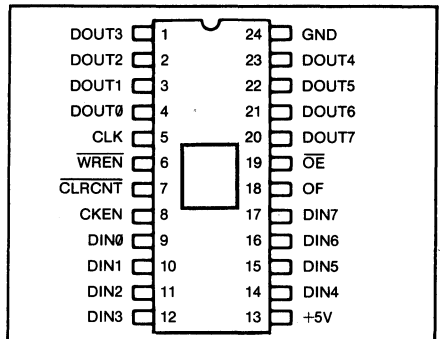
Single Row Buffer
SRB

FEATURES:

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Provides 8 Bit Wide Variable Length Serial Memory
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for Invisible Attributes or Character Widths of Greater than 8 Bits
- ☐ Three-State Outputs
- ☐ 4MHz Typical Read/Write Data Rate
- ☐ Static Operation
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 24 Pin Dual In Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible Inputs and Outputs
- ☐ Available in 135 Byte Maximum Length (CRT 9006-135) or 83 Byte Maximum Length (CRT 9006-83)

PIN CONFIGURATION



Package: 24-pin D.I.P.

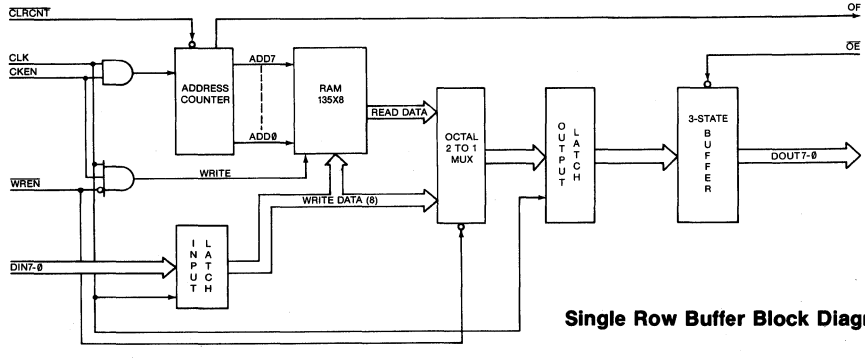
APPLICATIONS:

- ☐ CRT Data Row Buffer
- ☐ Block-Oriented Buffer
- ☐ Printer Buffer
- ☐ Synchronous Communications Buffer
- ☐ Floppy Disk Sector Buffer

SECTION IV

GENERAL DESCRIPTION

The SMC Single Row Buffer (SRB) provides a low cost solution to memory contention between the system processor and CRT controller in video display systems.
The SRB is a RAM-based buffer which is loaded with character data from system memory during the first scan line of each data row. While data is being written into the RAM it is also being output through the multiplexer onto the Data Ouput (DOUT) Lines. During subsequent scan lines in the data row, the system will disable Write Enable (WREN) and cause data to be read out from the internal RAM for CRT screen refresh, thereby releasing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row. The SRB enhances processor throughput and permits a flicker-free display of data.



Single Row Buffer Block Diagram

*FOR FUTURE RELEASE

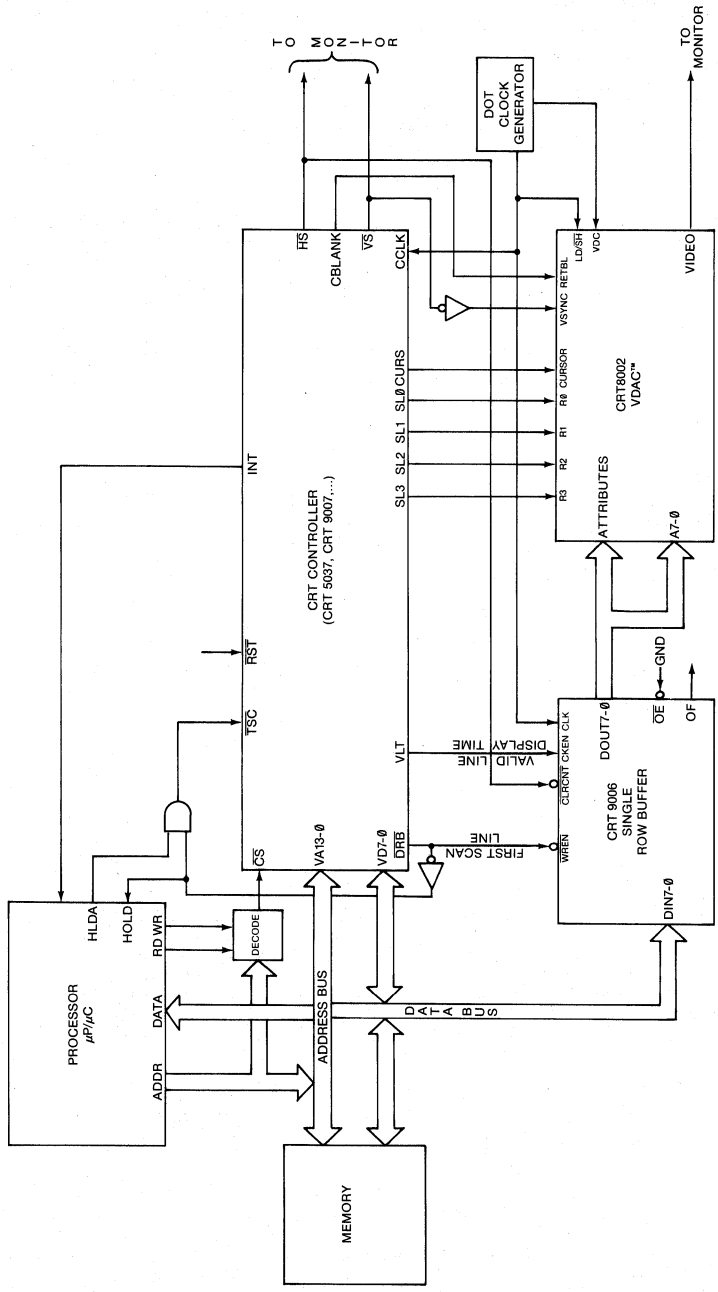


Figure 2: Typical CRT Controller Configuration With Single Row Buffer

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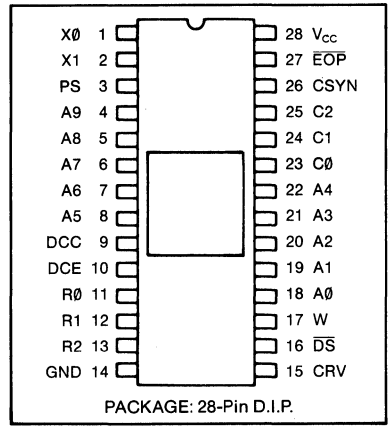
CRT 96364 A
CRT 96364 B
μPC FAMILY
Preliminary Specifications

CRT Controller

FEATURES
- ☐ Single +5v power supply
- ☐ 16 line x 64 character display
- ☐ On chip sync oscillator
- ☐ Complete cursor control
- ☐ Automatic scrolling
- ☐ Erase functions built in
- ☐ Performs character entry during horizontal sync
- ☐ Internal blinking cursor
- ☐ Page linking logic built in
- ☐ LS-TTL compatible
- ☐ Compatible with CRT 8002, CRT 7004

PIN CONFIGURATION



PACKAGE: 28-Pin D.I.P.

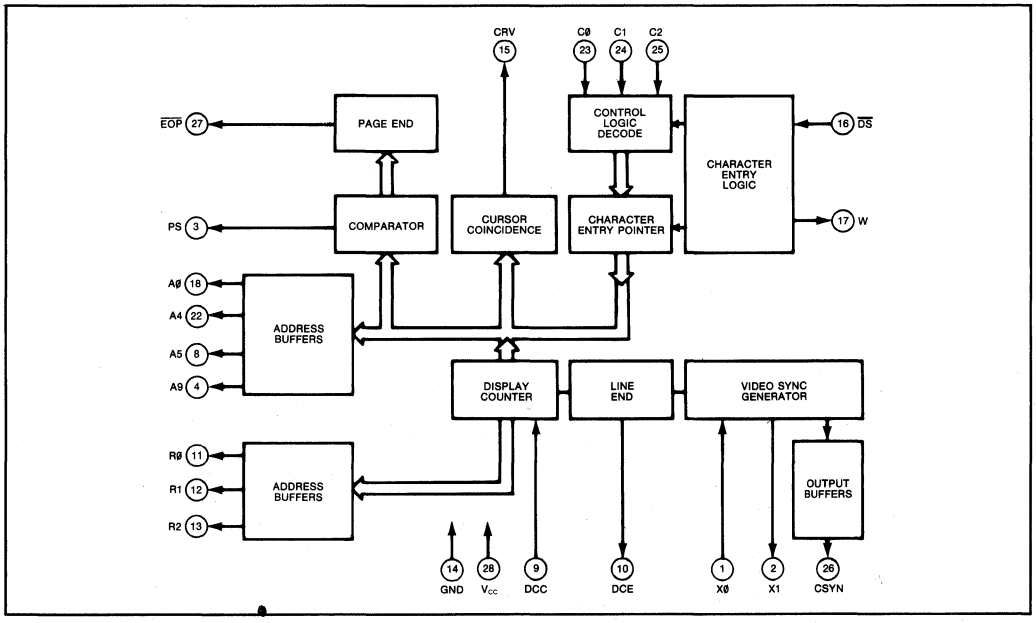
GENERAL DESCRIPTION

The CRT 96364 A/B is a CRT Controller which controls all of the functions associated with a 16 line x 64 character video display. Functions include CRT refresh, character entry, and cursor management.

The CRT 96364 A/B contains an internal oscillator which produces the composite sync output. The CRT 96364 B generates a 60 Hz vertical sync while the CRT 96364 A generates a 50 Hz vertical sync.

Standard functions such as ERASE PAGE, ERASE LINE, and ERASE TO END OF LINE make the CRT 96364 A/B easy to interface to any computer or microprocessor, or to use as a stand-alone video processor.

The CRT 96364 A/B requires only +5v power at less than 100 mA. It is manufactured in COPLAMOS® N channel silicon gate technology.



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1 2	Crystal in Crystal out	XØ X1	Pin one is the sync clock input. It may be driven directly from a TTL gate or from a parallel mode crystal connected between pins one and two. When a crystal is used, a 10 MΩ resistor should be connected in parallel. For standard 60 Hz line operation, a 1.018 MHz frequency source or crystal is required (with the CRT 96364B). For 50 Hz line operation, the CRT 96364A requires a 1.008 MHz crystal.
3	Page Select	PS	PS provides automatic page selection when two pages of memory are used. A "zero" output indicates selection of page 1; a logic "one" indicates page 2.
4-8	Memory Address	A9-A5	Upper order memory address lines; A6-A9 determine which lines of text are being refreshed or written. A5 along with AØ-A4 determine the character position.
9	Character Clock	DCC	Character clock input. Addresses are changed on the trailing edge of DCC.
10	Dot Clock Enable	DCE	A logic zero from DCE is used to inhibit oscillation of the dot clock for retrace blanking.
11-13	Row Address	RØ-R2	Character Generator row addresses. Blanks are generated by forcing RØ-R2 to "000". During character entry, R2 gates data into memory to control the erase function. Row addressing follows the sequence 0-1-2-3-4-5-6-7-0-0-0-0-increment text line-0-1-2-etc.
14	Ground	GND	Ground
15	Cursor	CRV	Cursor video output. Indicates cursor location by a 2 Hz blinking underline.
16	Data Strobe	$\overline{DS}$	The rising edge of $\overline{DS}$ strobes the appropriate CØ-C2 control word into the CRT 96364A/B.
17	Write	W	A positive going signal which indicates that the CRT 96364A/B is allowing a memory write. W is approximately 4 μs, and occurs during H sync. Memory address lines are latched at the cursor address during W.
18-22	Memory Address	AØ-A4	Lower order memory addresses. AØ-A4 plus A5 (pin 8) determine the character position.
23-25	Command Inputs	CØ-C2	Command inputs are strobed into the CRT 96364A/B by $\overline{DS}$. Functions are as follows: **Function** — C_2 C_1 C_0 Page erase and cursor home (top-left) — 0 0 0 Erase to end of line and return cursor (to left) — 0 0 1 Line feed (cursor down) — 0 1 0 No operation* — 0 1 1 Cursor left (one position) — 1 0 0 Erasure of cursor-line — 1 0 1 Cursor up (one position) — 1 1 0 Normal character. Write signal is generated and cursor position is incremented — 1 1 1 * In order to suppress non-displayed characters
26	Composite Sync	CSYN	Positive logic composite sync output. Horizontal sync is generated during VSYNC and $\overline{VSYNC}$ time. A vertical sync output may be generated by logically "ANDing" CSYN and DCE.
27	End of Page	$\overline{EOP}$	This output is used to increment an external page counter when using more than one page of memory.
28	Power Supply	V_{CC}	+ 5 volt supply.

OPERATION

The CRT 96364A/B provides all of the control functions required by a CRT display with a minimum of external circuitry.

The cursor and erase commands may be decoded from the data bus by a low cost 256 x 4 PROM. The CRT 96364A/B then provides the necessary cursor movement and gates the memory for writing or erasing. Erase is controlled by providing a write signal to RAM, and gating "zeros" to the RAM input bus. Use of an external PROM allows user selection of control words.

The RAM write command, "W", is generated during horizontal retrace. At this time, the RAM address is set to the cursor address. Immediately following the write command, the RAM addresses revert to refresh addressing and the cursor is shifted one character.

CURSOR

The cursor location is indicated by an alternating high on pin 15 (CRV) at row 7, and a low on pin 15 with RØ-R2 forced low at rows 0-6. These alternate at a 2 Hz rate. If CRV is used to force the display on, the result will be a blink of the cursor character position alternating with an underline at a 2 Hz rate.

CHARACTER ENTRY

When a Normal Character code (C2, C1, CØ = 1, 1, 1) and a Data Strobe are received, the write command will be generated during horizontal retrace. If, at the end of the horizontal retrace, the cursor is at the last position on a line, a carriage return and line feed will automatically occur. When the cursor is at the last position of the last line, a carriage return and up-scroll will automatically occur.

EXTRA FUNCTIONS

By using the fourth bit of the decoder PROM as a write enable signal, and properly programming the PROM, the additional commands of Home Cursor, Return Cursor, and Roll Screen may be generated. This is done by inhibiting the W signal to the page memory and inputting the control codes, respectively, of Page Erase and Home Cursor, Erase to end of line and Return Cursor, and Line Feed.

SCROLLING

Scrolling of the screen text will occur under any of the following characteristics:

1. Inputting a line feed command when the cursor is at the bottom line of the screen.
2. Inputting a character when the cursor is at the bottom right hand side of the screen.

Scrolling will result in the entire top line of the screen being erased and all of the remaining lines shifting up. Alternatively, a Roll (defined as all of the lines shifting up with the previous top line reappearing at the bottom of the screen) may be performed by inhibiting the write signal to the page memory as described in "Extra Functions."

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+7.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

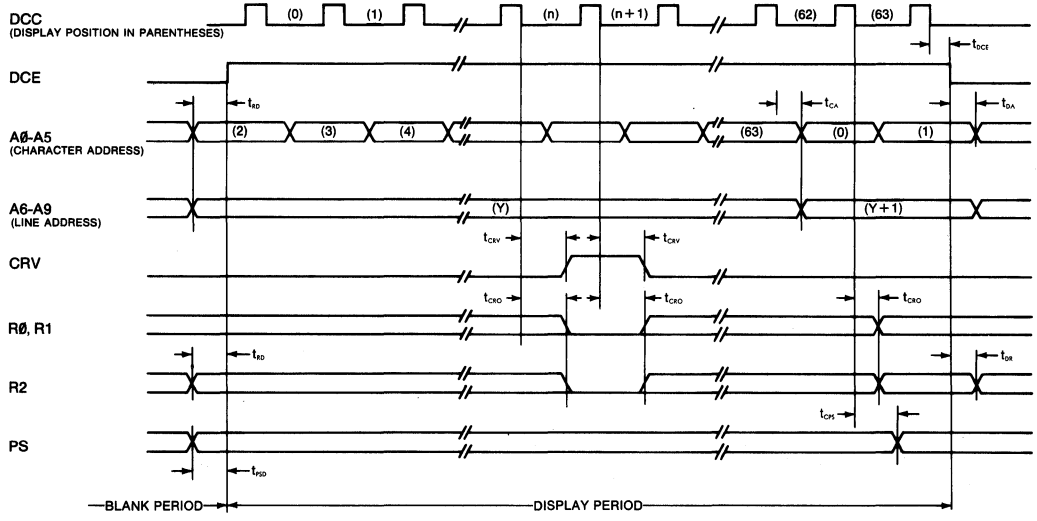
ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS (except DCC)					
Low-level, V_{IL}			0.65	V	excluding DCC
High-level, V_{IH}	2.2			V	excluding DCC
INPUT VOLTAGE LEVELS—DCC					
Low-level, V_{IL}			0.65	V	
High-level, V_{IH}	3.5			V	
OUTPUT VOLTAGE LEVELS (DCE Only)					
Low-level, V_{OL}			0.4	V	I_{OL}=1.9 mA
High-level, V_{OH}	2.2			V	I_{OH}=−100 μA
OUTPUT VOLTAGE LEVELS (except DCE)					
Low-level, V_{OL}			0.4	V	I_{OL}=0.36 mA
High-level, V_{OH}	2.2			V	I_{OH}=−100 μA
INPUT CURRENT					
Low-level, I_{IL}			10	μA	$0 \leq V_{IN} \leq +5V$
INPUT CAPACITANCE					
All inputs, C_{IN} (except DCE)		5		pF	V_{IN}=GND
C_{IN} (DCC Only)		25		pF	V_{IN}=GND
POWER SUPPLY CURRENT					
I_{CC}		100	120	mA	

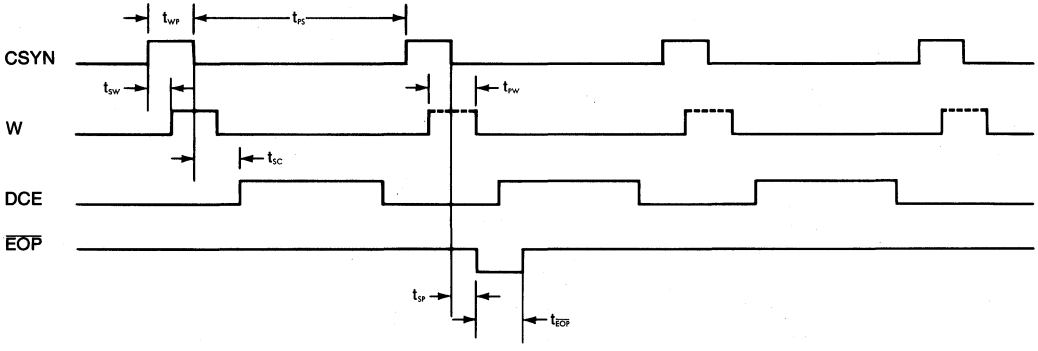
AC CHARACTERISTICS

PARAMETERS	SYMBOL	VALUES			UNIT
		MIN.	TYP.	MAX.	
Frequency of control clock DCC	f_{DCC}		1.6		MHz
Crystal Frequency CRT 9364A	f_X		1.008		MHz
CRT 9364B	f_X		1.018		MHz
DCC pulse width	t_{DCC}	200			ns
Rise and fall times	t_r t_f		20	40	ns
Refresh memory address access time	t_{CA}		200	250	ns
Character memory address access time	t_{CRO}		200	250	ns
PS access time (read)	t_{CPS}		300	1000	ns
CRV access time	t_{CRV}		200	250	ns
DCE access time (high to low)	t_{DCE}		100		ns
SYNC period	t_{PS}		64		μs
SYNC pulse width	t_{WP}		4		μs
DCE access time (low to high level)	t_{SC}		11		μs
$\overline{EOP}$ access time (high to low level)	t_{SP}		1	1.5	μs
W access time (low to high)	t_{SW}		500	1000	ns
W pulse width	t_{PW}		4		μs
$\overline{EOP}$ pulse width	$t_{\overline{EOP}}$		10		μs
Address to rising edge of DCE delay	t_{AD}	0		2.1	μs
Falling edge of DCE to Address delay	t_{DA}	0		1	μs
Row to rising edge of DCE delay	t_{RD}	0		2.1	μs
Falling edge of DCE to row delay	t_{DR}	0		1	μs
PS to rising edge of DCE delay	t_{PSD}	0			μs

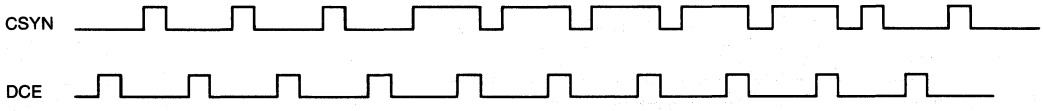
LINE TIMING



SYNC TIMING



FRAME TIMING



SECTION IV

DATA INPUT TIMING

Asynchronous Operation

PARAMETER	SYMBOL	Value MIN	TYP	MAX	UNIT
DS Pulse Width	t_{PW}	0.5			μs
CØ-C2 Set Up Time	t_{CDS}	1			μs
CØ-C2 Hold Time	t_{DSC}	90			μs
Minimum Strobe Period (Operation Execution Time)	t_{DS}				

FUNCTION	C2	C1	CØ		
Page Erase & Cursor Home	0	0	0	132	ms
Erase to End of Line & Return Cursor	0	0	1	4.2	ms
Line Feed (Cursor Down)	0	1	0	130*	μs
No Operation	0	1	1	80	μs
Cursor Left	1	0	0	80	μs
Erasure of Cursor Line	1	0	1	8.3	ms
Cursor Up	1	1	0	80	μs
Normal Character	1	1	1	130*	μs

*Will increase to 8.3 ms when text scroll occurs. See "Scrolling" for conditions.

Synchronous Operation

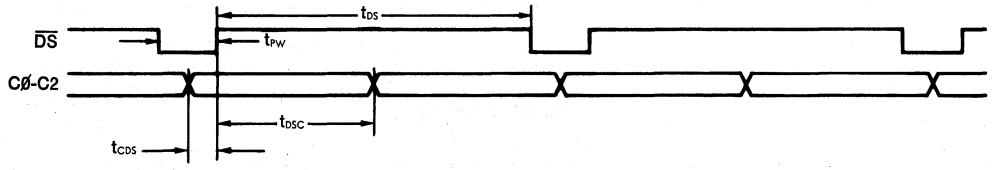
PARAMETER	SYMBOL	Value MIN	TYP	MAX	UNIT
DS Pulse Width	t_{PW}	0.5			μs
C0-C2 Set-Up Time	t_{CDS}	1			μs
C0-C2 Hold Time	t_{DSC}	16			μs
DS Set Up Time	t_{SDS}	1			μs
Minimum Strobe Period (Operation Execution Time)	t_{DS}				

FUNCTION	C2	C1	CØ		
Page Erase & Cursor Home	0	0	0	132	ms
Erase to End of Line & Return Cursor	0	0	1	4.2	ms
Line Feed (Cursor Down)	0	1	0	64*	μs
No Operation	0	1	1	64	μs
Cursor Left	1	0	0	64	μs
Erasure of Cursor Line	1	0	1	8.3	ms
Cursor Up	1	1	0	64	μs
Normal Character	1	1	1	64*	μs

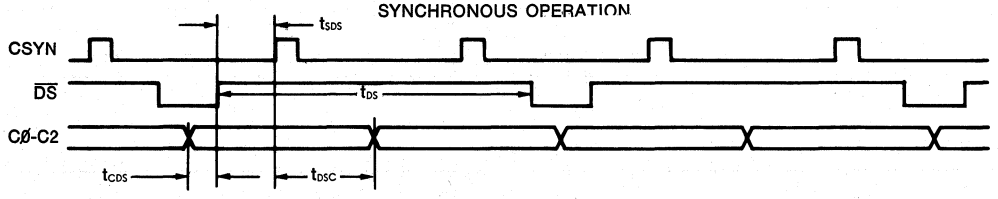
*Will increase to 8.3 ms when text scroll occurs. See "Scrolling" for conditions.

DATA INPUT TIMING

ASYNCHRONOUS OPERATION



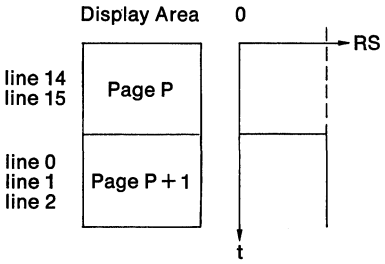
SYNCHRONOUS OPERATION



MULTIPLE PAGE DISPLAY

When linking two or more pages, the $\overline{EOP}$ and RS signals may be used to allow a "moving window" text display.

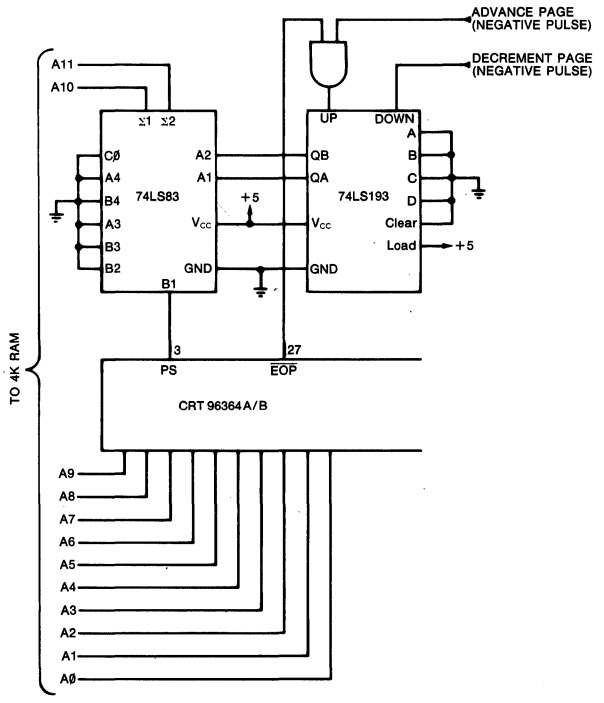
PS (Page Select) indicates the end of page location. If a scroll has occurred, PS will show the transition from the end of line 15 of page P and the beginning of line 0 of page P + 1.



To properly maintain the memory address when displaying more than two pages, $\overline{EOP}$ pulses low at the point in time when page P is scrolled completely off the screen. At this time, RS will remain low for the entire frame since page P + 1 is now the only displayed page.

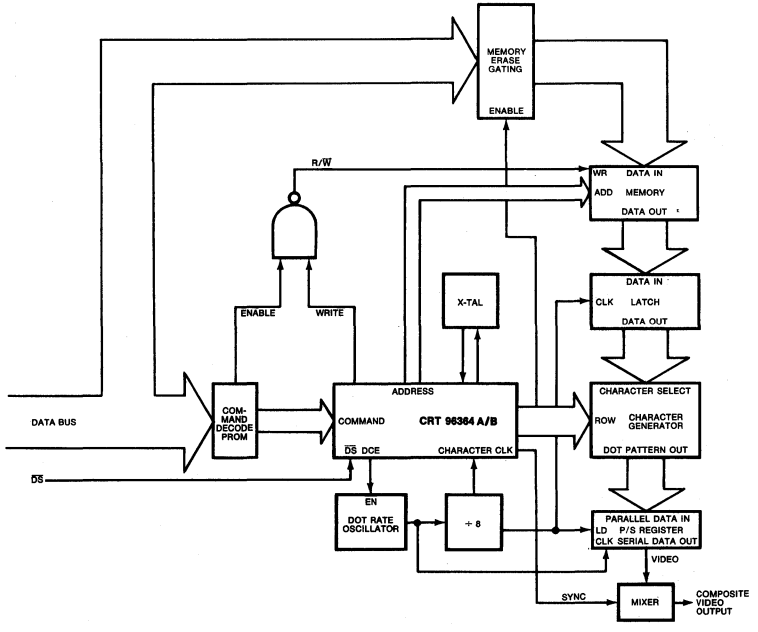
The circuit at the right will allow scrolling through 4 pages of memory.

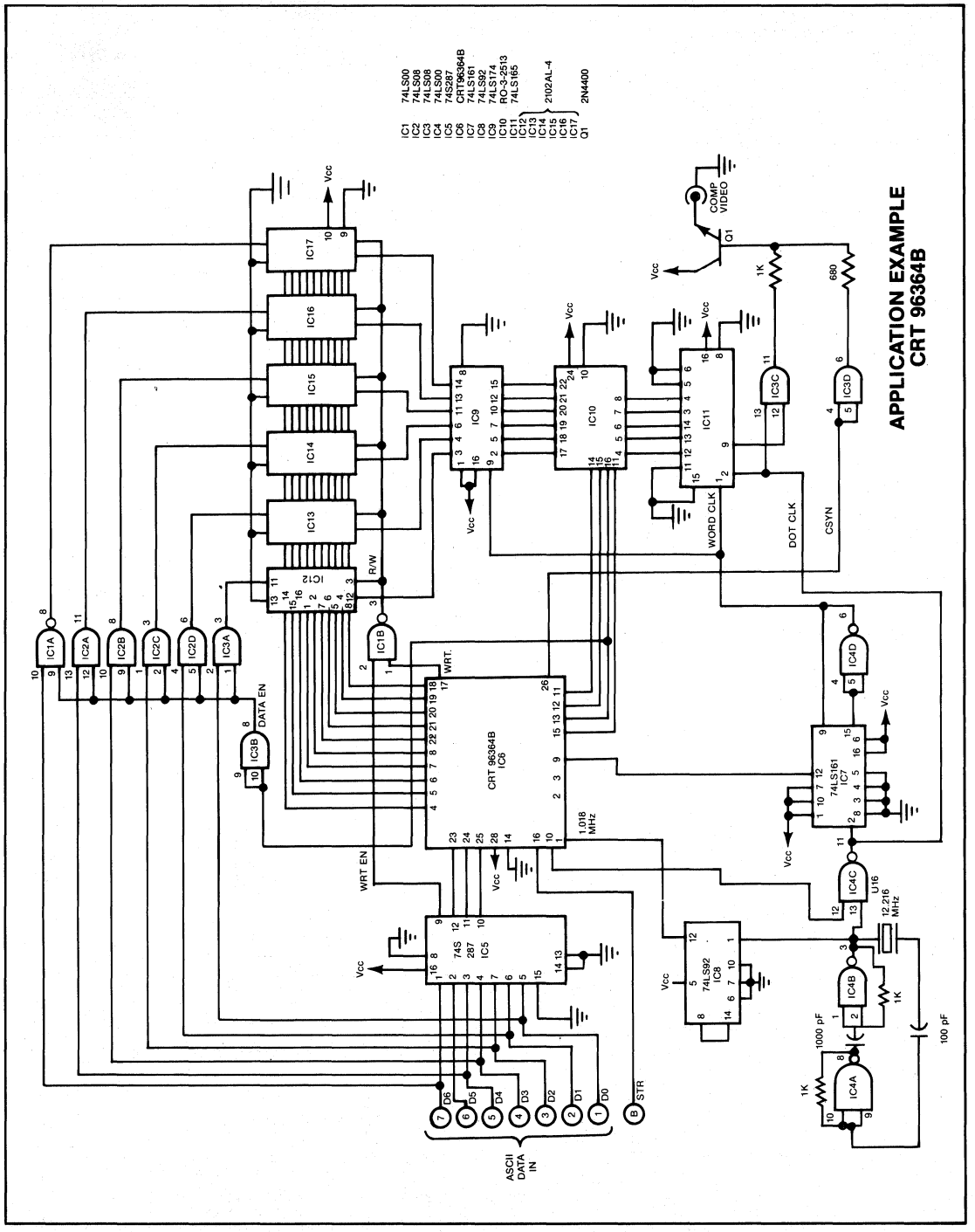
4 PAGE DISPLAY



SECTION IV

TYPICAL SYSTEM APPLICATION





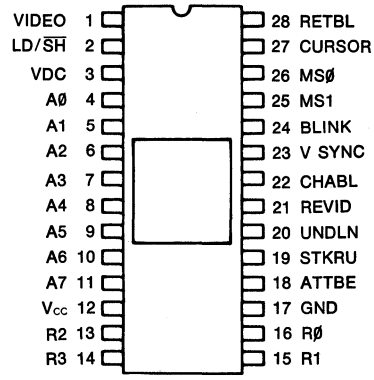
STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11787
(516) 273-3100 · TWX-510-227-8898

CRT Video Display Attributes Controller Video Generator VDAC™

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 8002A 20MHz
    - CRT 8002B 15MHz
    - CRT 8002C 10MHz
    - Access time 400ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ Four on chip cursor modes
  - Underline
  - Blinking underline
  - Reverse video
  - Blinking reverse video
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM
- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM and options
- ☐ Compatible with CRT 5027 VTAC®

PIN CONFIGURATION



General Description

The SMC CRT 8002 Video Display Attributes Controller (VDAC) is an N-channel COPLAMOS® MOS/LSI device which utilizes CLASP® technology. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002 VDAC is a companion chip to SMC's CRT 5027 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002 video output may be connected directly to a CRT monitor video input. The CRT 5027 blanking output can be connected directly to the CRT 8002 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

Four cursor modes are available on the CRT 8002. They are: underline, blinking underline, reverse video block, and blinking reverse video block. Any one of these can be mask programmed as the cursor function. There is a separate cursor blink rate which can be mask programmed to provide a 15 Hz to 2 Hz blink rate.

The CRT 8002 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5 Hz to 1.0 Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002 can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

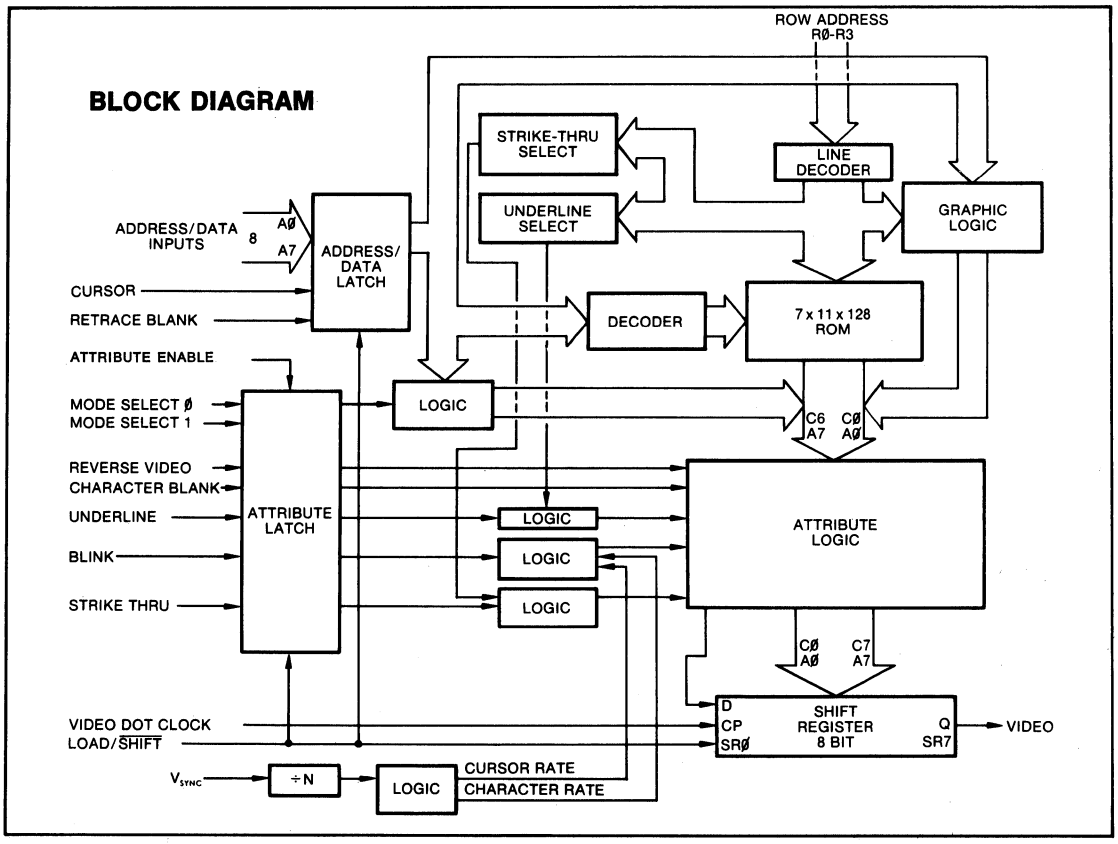
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= +5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{iL}			0.8	V	
High-level, V_{IH}	4.3			V	See Figure 6
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL}=0.4 mA, 74LSXX load
High-level, V_{OH}	2.4			V	I_{OH}=−20μA
INPUT CURRENT					
Leakage, I_L (Except CLOCK)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Leakage, I_L (CLOCK Only)			50	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
LD/$\overline{SH}$		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	
A.C. CHARACTERISTICS					
See Figure 6, 7					

SYMBOL	PARAMETER	CRT 8002A		CRT 8002B		CRT 8002C		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VDC	Video Dot Clock Frequency	1.0	20	1.0	15	1.0	10	MHz
PW_H	VDC—High Time	15.0		23		40		ns
PW_L	VDC—Low Time	15.0		23		40		ns
t_{CY}	LD/$\overline{SH}$ cycle time	400		533		800		ns
t_r, t_f	Rise, fall time		10		10		10	ns
t_{SET-UP}	Input set-up time	≥0		≥0		≥0		ns
t_{HOLD}	Input hold time	15		15		15		ns
t_{PDI}, t_{PDO}	Output propagation delay	15	50	15	65	15	100	ns
t_1	LD/$\overline{SH}$ set-up time	10		15		20		ns
t_2	LD/$\overline{SH}$ hold time	5		5		5		ns

BLOCK DIAGRAM



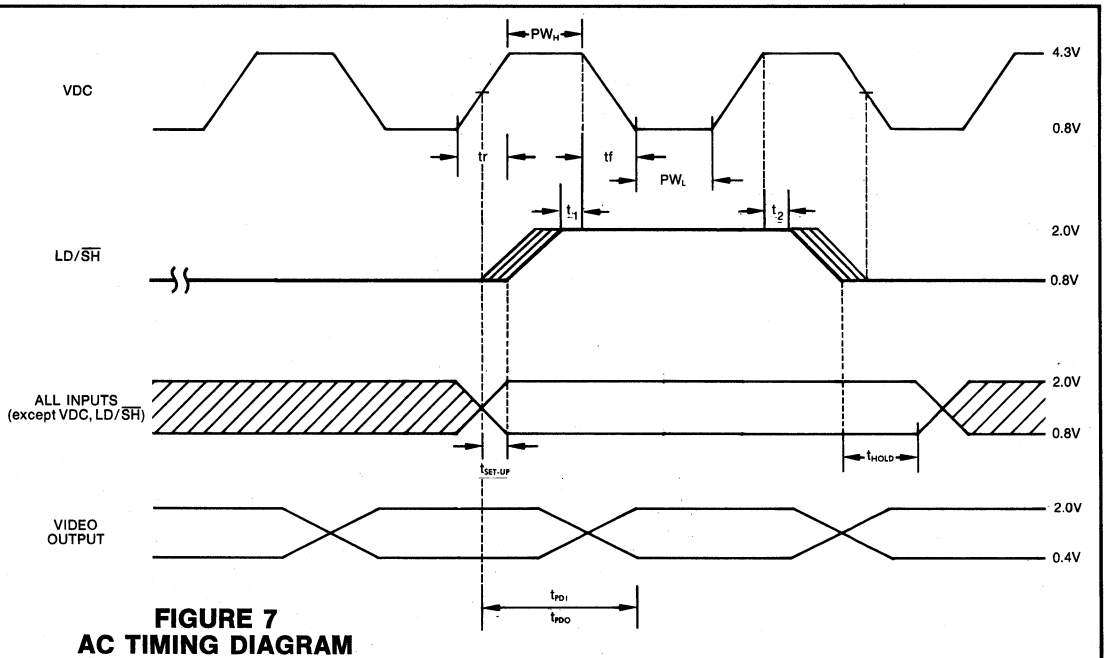


FIGURE 7
AC TIMING DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1	VIDEO	Video Output	O	The video output contains the dot stream for the selected row of the alphanumeric, wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs. In the alphanumeric mode, the characters are ROM programmed into the 77 dots, (7X11) allocated for each of the 128 characters. See figure 5. The top row (RØ) and rows R12 to R15 are normally all zeros as is column C7. Thus, the character is defined in the box bounded by R1 to R11 and CØ to C6. When a row of the ROM, via the attribute logic, is parallel loaded into the 8-bit shift-register, the first bit serially shifted out is C7 (A zero; or a one in REVID). It is followed by C6, C5, through CØ. The timing of the Load/$\overline{\text{Shift}}$ pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4. When the next Load/$\overline{\text{Shift}}$ pulse appears the next character's row of the ROM, via the attribute logic, is parallel loaded into the shift register and the cycle repeats.
2	LD/$\overline{\text{SH}}$	Load/$\overline{\text{Shift}}$	I	The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/$\overline{\text{Shift}}$ input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (AØ-A7) are latched on the negative transition of the Load/$\overline{\text{Shift}}$ input. See timing diagram, figure 7.
3	VDC	Video Dot Clock	I	Frequency at which video is shifted.
4-11	AØ-A7	Address/Data	I	In the Alphanumeric Mode the 7 bits on inputs (AØ-A6) are internally decoded to address one of the 128 available characters (A7 = X). In the External Mode, AØ-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Modes AØ-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode AØ-A2 is used to define the 3 line segments.
12	V_{CC}	Power Supply	PS	+5 volt power supply
13,14,15,16	R2,R3,R1,RØ	Row Address	I	These 4 binary inputs define the row address in the current character block.
17	GND	Ground	GND	Ground
18	ATTBE	Attribute Enable	I	A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select Ø, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/$\overline{\text{Shift}}$ pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 7.
19	STKRU	Strike-Thru	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which strike-thru is to be placed as well as to program the strike-thru to be 1 to N raster lines high. Actually, the strike-thru decoder (mask programmable) logic allows the strike-thru to be any number or arrangement of horizontal lines in the character block. The standard strike-thru will be a double line on rows R5 and R6.
20	UNDLN	Underline	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which underline is to be placed as well as to program the underline to be 1 to N raster lines high. Actually, the underline decoder (mask programmable) logic allows the underline to be any number or arrangement of horizontal lines in the character block. The standard underline will be a single line on R11.
21	REVID	Reverse Video	I	When this input is low and RETBL = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1.
22	CHABL	Character Blank	I	When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1.
23	V SYNC	V SYNC	I	This input is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle). The divisors can be programmed from ÷ 4 to ÷ 30 for the cursor (÷ 8 to ÷ 60 for the character).
24	BLINK	Blink	I	When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the programmed character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The standard character blink rate is 1.875 Hz.
25 26	MS1 MSØ	Mode Select 1 Mode Select Ø	I I	These 2 inputs define the four modes of operation of the CRT 8002 as follows: Alphanumeric Mode — In this mode addresses AØ-A6 (A7 = X) are internally decoded to address 1 of the 128 available ROM characters. The addressed character along with the decoded row will define a 7 bit output from the ROM to be loaded into the shift register via the attribute logic. Thin Graphics Mode — In this mode AØ-A2 (A3-A7 = X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 2. The top of the entity will begin on row 0000 and will end on a mask programmable row.

MS1	MSØ	MODE
1	1	Alphanumeric
1	0	Thin Graphics
0	1	External Mode
0	0	Wide Graphics

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
25 26 (cont.)				External Mode – In this mode the inputs AØ-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM. ROM or RAM. See figure 3. Wide Graphics Mode—In this mode the inputs AØ-A7 will define a graphic entity as described in figure 1. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs RØ to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory. These 4 modes can be intermixed on a per character basis.
27	CURSOR	Cursor	I	When this input is enabled 1 of the 4 pre-programmed cursor modes will be activated. The cursor mode is on-chip mask programmable. The standard cursor will be a blinking (at 3.75Hz) reverse video block. The 4 cursor modes are: Underline—In this mode an underline (1 to N raster lines) at the programmed underline position occurs. Blinking Underline—In this mode the underline blinks at the cursor rate. Reverse Video Block—In this mode the Character Block is set to reverse video. Blinking Reverse Video Block—In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video. The cursor functions are listed in table 1.
28	RETBL	Retrace Blank	I	When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/Shift pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time.

SECTION IV

TABLE 1

CURSOR	RETBL	REVID	CHABL	UNDLN*	FUNCTION
X	1	X	X	X	"0" S.R. All
0	0	0	0	0	D (S.R.) All
0	0	0	0	1	"1" (S.R.)*
					D (S.R.) All others
0	0	0	1	X	"0" (S.R.) All
0	0	1	0	0	D (S.R.) All
0	0	1	0	1	"0" (S.R.)*
					D (S.R.) All others
0	0	1	1	X	"1" (S.R.) All
Underline*	0	0	0	X	"1" (S.R.)*
					D (S.R.) All others
Underline*	0	0	1	X	"1" (S.R.)*
					"0" (S.R.) All others
Underline*	0	1	0	X	"0" (S.R.)*
					D (S.R.) All others
Underline*	0	1	1	X	"0" (S.R.)*
					"1" (S.R.) All others
Blinking** Underline*	0	0	0	X	"1" (S.R.)* Blinking
					D (S.R.) All others
Blinking** Underline*	0	0	1	X	"1" (S.R.)* Blinking
					"0" (S.R.) All others
Blinking** Underline*	0	1	0	X	"0" (S.R.)* Blinking
					D (S.R.) All others
Blinking** Underline*	0	1	1	X	"0" (S.R.)* Blinking
					"1" (S.R.) All others
REVID Block	0	0	0	0	D (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					D (S.R.) All others
REVID Block	0	0	1	X	"1" (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					D (S.R.) All others
REVID Block	0	1	0	0	D (S.R.) All
REVID Block	0	1	0	1	"1" (S.R.)*
					D (S.R.) All others
REVID Block	0	1	1	X	"0" (S.R.) All
Blink** REVID Block	0	0	0	0	Alternate Normal Video/REVID At Cursor Blink Rate
Blink** REVID Block	0	0	0	1	
Blink** REVID Block	0	0	1	X	
Blink** REVID Block	0	1	0	0	
Blink** REVID Block	0	1	0	1	
Blink** REVID Block	0	1	1	X	

*At Selected Row Decode **At Cursor Blink Rate

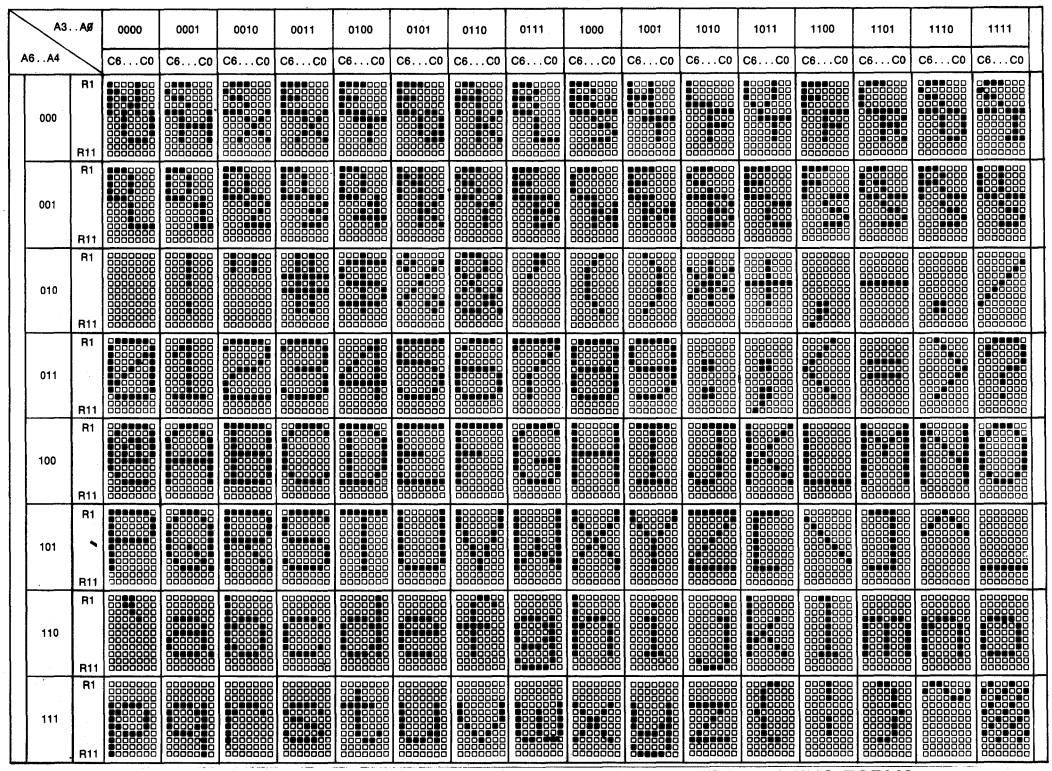
Note: If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate.

FIGURE 5
ROM CHARACTER BLOCK FORMAT

											ROWS	R3	R2	R1	RØ
(ALL ZEROS) →	0	0	0	0	0	0	0	0	—	—	RØ	0	0	0	0
	0	0	0	0	0	0	0	0	—	—	R1	0	0	0	1
	0	0	0	0	0	0	0	0	—	—	R2	0	0	1	0
	0	0	0	0	0	0	0	0	—	—	R3	0	0	1	1
	0	0	0	0	0	0	0	0	—	—	R4	0	1	0	0
	0	0	0	0	0	0	0	0	—	—	R5	0	1	0	1
77 BITS (7 x 11 ROM)	0	0	0	0	0	0	0	0	—	—	R6	0	1	1	0
	0	0	0	0	0	0	0	0	—	—	R7	0	1	1	1
	0	0	0	0	0	0	0	0	—	—	R8	1	0	0	0
	0	0	0	0	0	0	0	0	—	—	R9	1	0	0	1
	0	0	0	0	0	0	0	0	—	—	RIØ	1	0	1	0
	0	0	0	0	0	0	0	0	—	—	R11	1	0	1	1
	0	0	0	0	0	0	0	0	—	—	R12	1	1	0	0
	0	0	0	0	0	0	0	0	—	—	R13	1	1	0	1
(ALL ZEROS)	0	0	0	0	0	0	0	0	—	—	R14	1	1	1	0
	0	0	0	0	0	0	0	0	—	—	R15	1	1	1	1
	*C7	C6	C5	C4	C3	C2	C1	CØ	—	—					

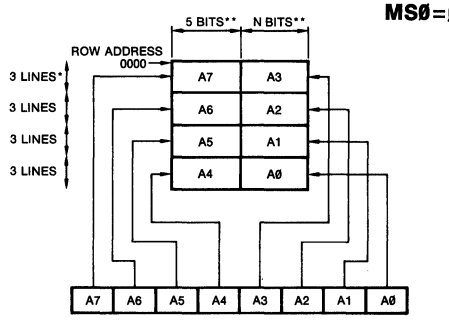
EXTENDED ZEROS (BACK FILL) FOR INTERCHARACTER SPACING (NUMBER CONTROLLED BY LD/$\overline{SH}$, VDC TIMING)

*COLUMN 7 IS ALL ZEROS (REVID = 0)
COLUMN 7 IS SHIFTED OUT FIRST



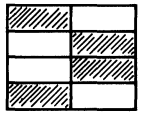
CONSULT FACTORY FOR CUSTOM FONT AND OPTION PROGRAMMING FORMS.

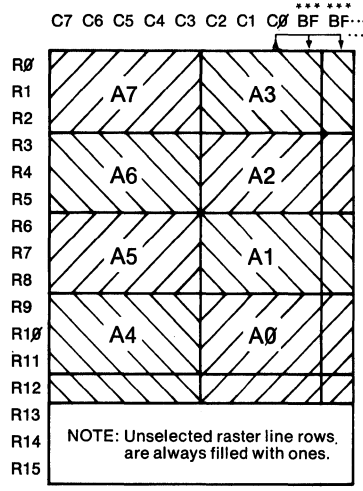
FIGURE 1
WIDE GRAPHICS MODE
MSØ=Ø MS1=Ø



*ON CHIP ROM PROGRAMMABLE TO 2, 3, OR 4 LINE MULTIPLES
**CAN BE PROGRAMMED FROM 1 TO 7 BITS
***LENGTH DETERMINED BY LD/$\overline{SR}$, VDC TIMING

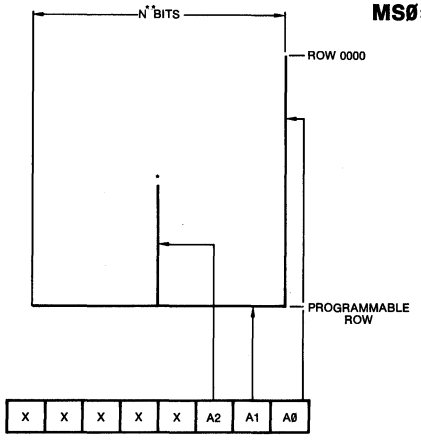
EXAMPLE: 10010110



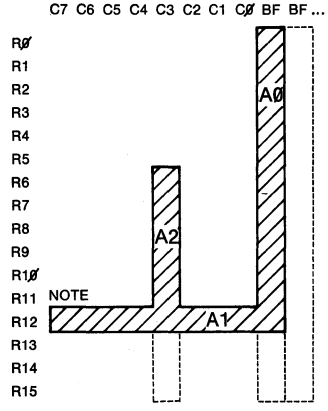


BF = back fill

FIGURE 2
THIN GRAPHICS MODE
MSØ=Ø MS1=1



X = DON'T CARE
* THE INSIDE SEGMENT IS MASK PROGRAMMABLE TO ROW 0000
** LENGTH DETERMINED BY LD/$\overline{SR}$, VDC TIMING



NOTE: When A1 = "1", the underline row/rows are deleted. When A1 = "0", the underline, if selected, will appear.

BF = back fill

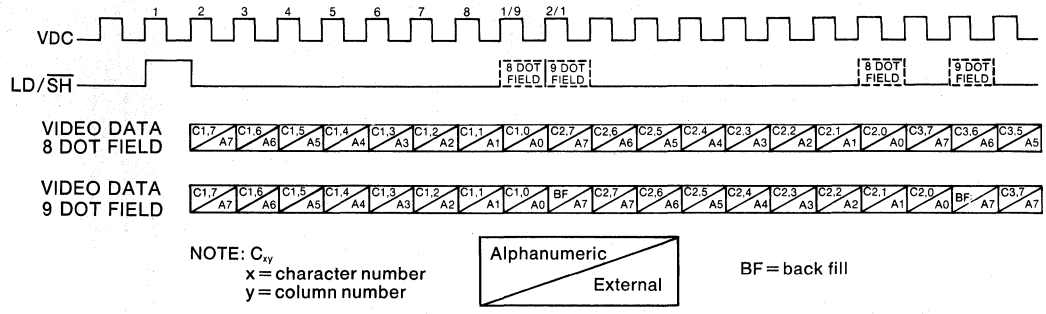
FIGURE 3
EXTERNAL MODE
MSØ=1 MS1=Ø

	C7	C6	C5	C4	C3	C2	C1	CØ	BF	BF	···
RØ – R15	A7	A6	A5	A4	A3	A2	A1	AØ	A7	A7	···

BF = back fill

SECTION IV

FIGURE 4 TYPICAL VIDEO OUTPUT



NOTE: C_{xy}
x = character number
y = column number

Alphanumeric / External

BF = back fill

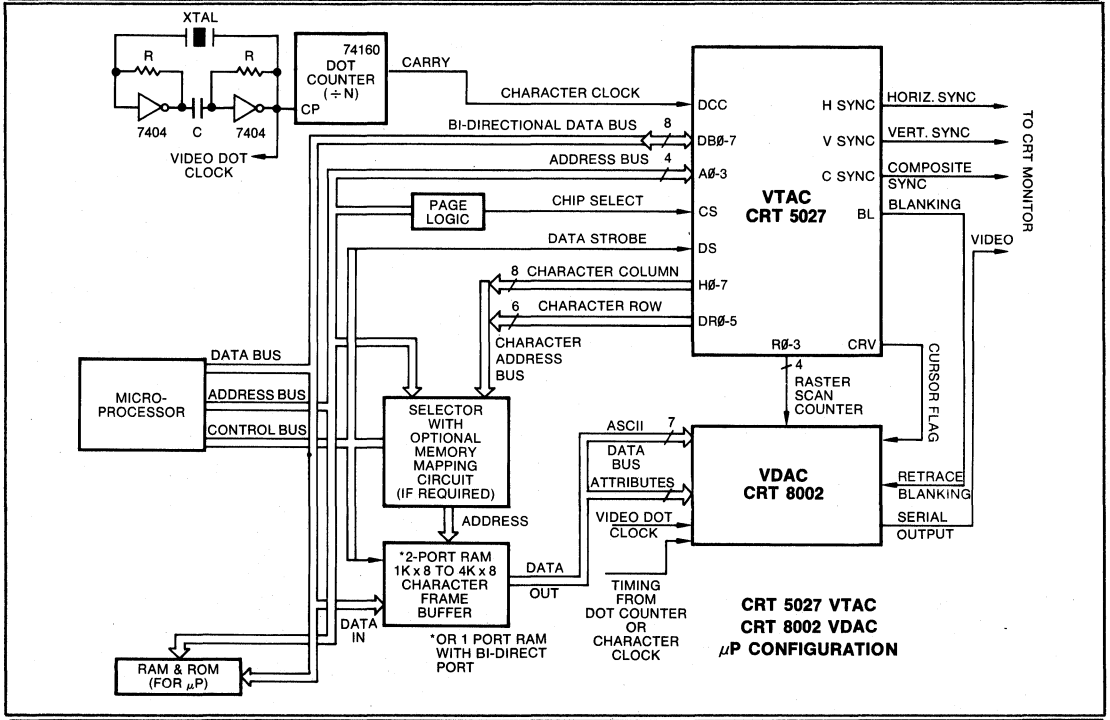
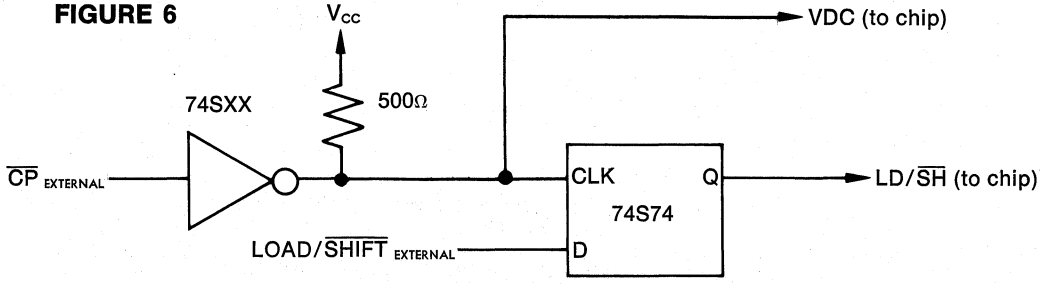


FIGURE 6



STANDARD MICROSYSTEMS CORPORATION
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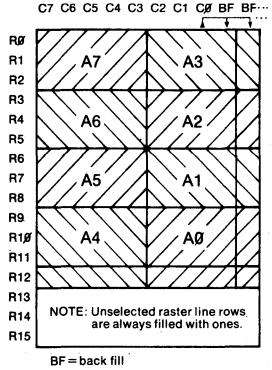
CRT 8002-001 (KATAKANA) CODING INFORMATION

CRT Video Display-Controller Video Generator VDAC™

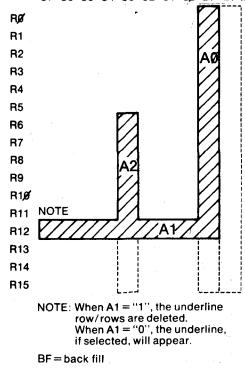
A6..A4 \ A3..A0		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0
000	R1																
	R11																
001	R1																
	R11																
010	R1																
	R11																
011	R1																
	R11																
100	R1																
	R11																
101	R1																
	R11																
110	R1																
	R11																
111	R1																
	R11																

WIDE GRAPHICS MODE



BF = back fill

THIN GRAPHICS MODE



NOTE: When A1 = "1", the underline row/rows are deleted.
When A1 = "0", the underline, if selected, will appear.

BF = back fill

ATTRIBUTES

Underline
Underline will be a single horizontal line at row R11

Cursor
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

Blink Rate
The character blink rate will be 1.875 Hz

Strike-Thru
The strike-thru will be a double line at rows R5 and R6

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We keep ahead of our competition so you can keep ahead of yours.

CRT 8002-003
(5 X 7 ASCII)
CODING INFORMATION

CRT Video Display-Controller Video Generator VDAC™

A6..A4 \ A3..A0		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0
000	R1																
	R11																
001	R1																
	R11																
010	R1																
	R11																
011	R1																
	R11																
100	R1																
	R11																
101	R1																
	R11																
110	R1																
	R11																
111	R1																
	R11																

WIDE GRAPHICS MODE

THIN GRAPHICS MODE

ATTRIBUTES

Underline
Underline will be a single horizontal line at R8

Cursor
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

Blink Rate
The character blink rate is 1.875 Hz

Strike-Thru
The strike-thru will be a single horizontal line at R4

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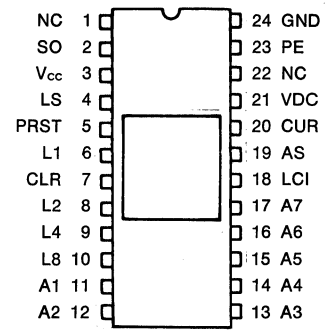
Dot Matrix Character Generator

128 Characters of 7 × 11 Bits

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 7004A 20MHz
    - CRT 7004B 15MHz
    - CRT 7004C 10MHz
    - Access time 400ns
- ☐ No descender circuitry required
- ☐ On chip cursor
- ☐ On chip character address buffer
- ☐ On chip line address buffer
- ☐ Single +5 volt power supply
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM
- ☐ Compatible with CRT 5027 VTAC®
- ☐ Enhanced version of CG5004L-1

PIN CONFIGURATION



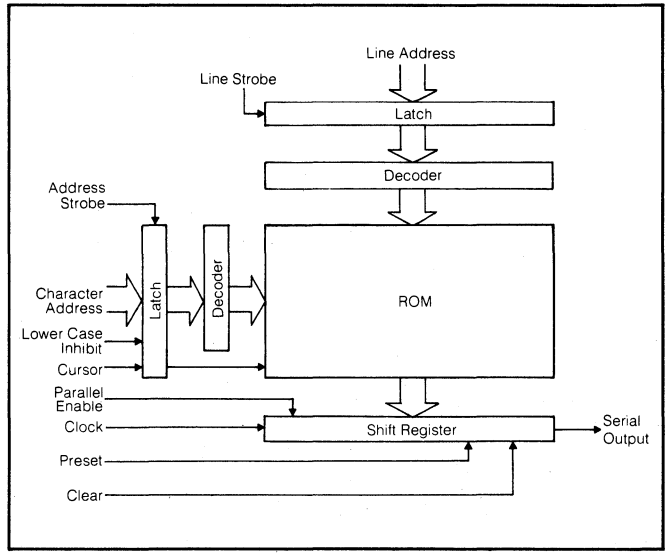
PACKAGE: 24-Pin D.I.P.

GENERAL DESCRIPTION

SMC's CRT 7004 is a high speed character generator with a high speed video shift register designed to display 128 characters in a 7 x 11 dot matrix. The CRT 7004 is an enhanced, pin for pin compatible, version of SMC's CG5004L-1. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply. This process permits reduction of turn-around time for ROM patterns.

The CRT 7004 is a companion chip to SMC's CRT 5027 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

FUNCTIONAL BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

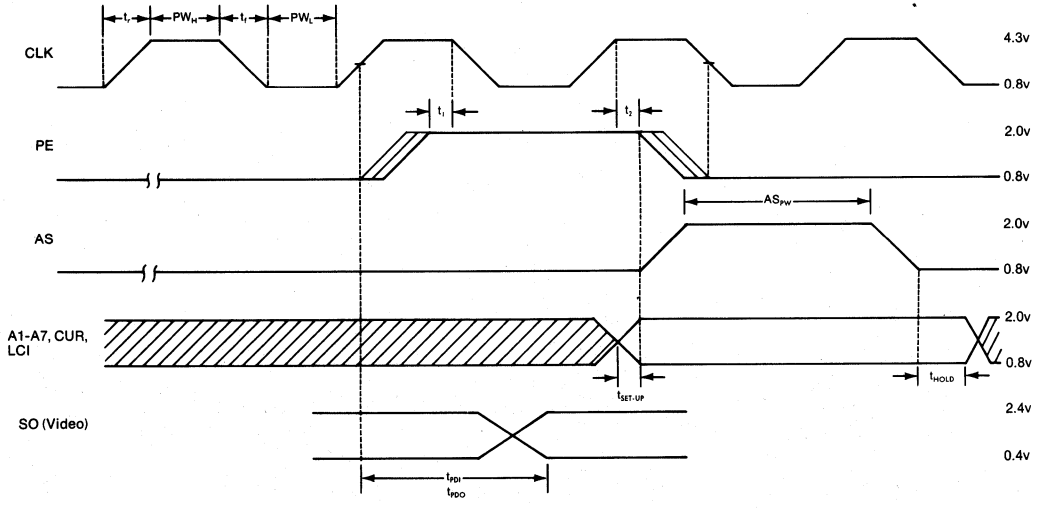
ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	4.3			V	See AC Timing Diagram
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL}=0.4 mA, 74LSXX load
High-level, V_{OH}	2.4			V	I_{OH}=−20μA
INPUT CURRENT					
Leakage, I_L			100	μA	V_{IN}=O. LS, AS, A1-A7, Cursor LCI
			10	μA	$O \leq V_{IN} \leq V_{CC}$, All others
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
PE		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	

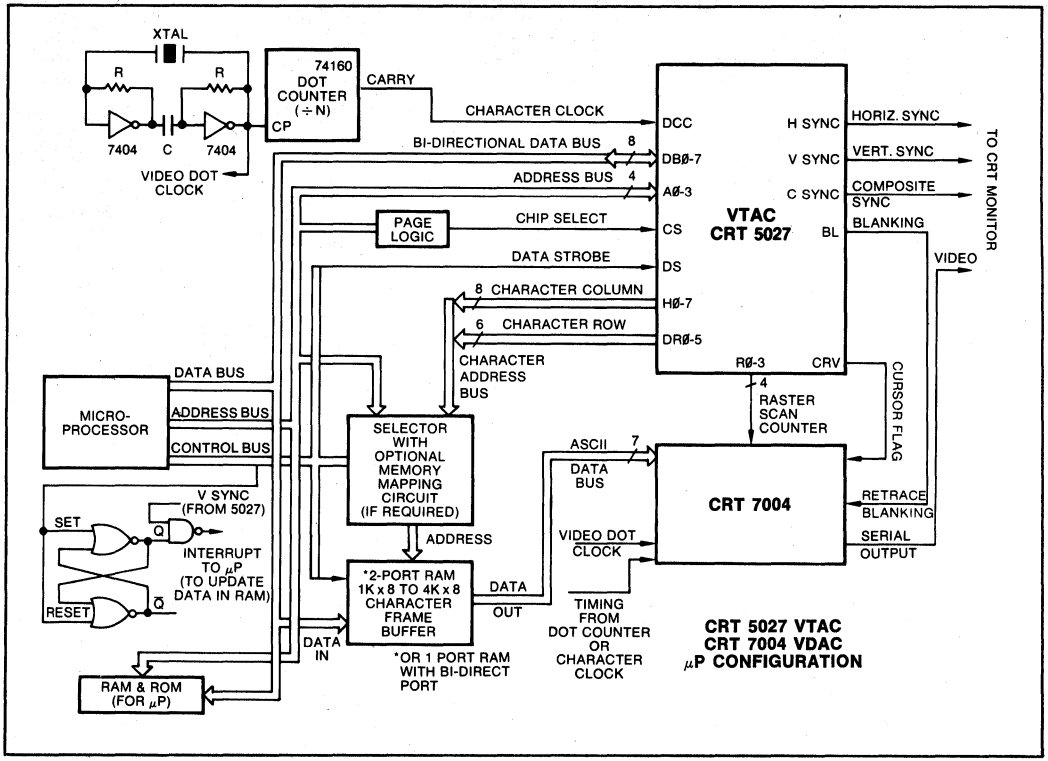
SYMBOL	PARAMETER	CRT 7004A		CRT 7004B		CRT 7004C		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VDC	Video Dot Clock Frequency	1.0	20	1.0	15	1.0	10	MHz
PW_H	VDC—High Time	13.5		21		36		ns
PW_L	VDC—Low Time	13.5		21		36		ns
$t_{CY}AS$	Address strobe to PE high	400		533		800		ns
$t_{CY}LS$	Line strobe to PE high	1.0		1.0		1.0		μs
t_r, t_f	Rise, fall time		10		10		10	ns
t_1	PE set-up time	5		20		20		ns
t_2	PE hold time	15		15		15		ns
AS_{PW}	Address strobe pulse width	50		50		50		ns
LS_{PW}	Line strobe pulse width	50		50		50		ns
t_{SET-UP}	Input set-up time	≥0		≥0		≥0		ns
t_{HOLD}	Input hold time	15		15		15		ns
t_{Pd1}, t_{Pd0}	Output propagation delay		45		60		90	ns

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	NC	No Connection	
2	SO	Serial Output	The output of the dynamic shift register is clocked out on this pin. The serial input to this shift register is internally grounded; thus zeros are shifted in while data is shifted out.
3	V_{CC}	Power Supply	+5 volt supply
4	LS	Line Strobe	A positive pulse on this input enters data from the L1, L2, L4, L8 lines into the line address holding register. The LS input may be left open, in which case it is pulled up to V_{CC} by an internal resistor. Data on the L1 to L8 inputs is then entered directly into the register without any latching action.
5	PRST	Preset	A high level on this input forces the last stage of the shift register and the serial output to a logic high.
6,8,9,10	L1, L2, L4, L8	Line Address	A binary number N, on these four inputs address the Nth line of the character font for N = 1—11. If lines 0, 12, 13, 14 or 15 are addressed, the parallel inputs to the shift register are all forced low.
7	CLR	Clear	A high level on this input forces the last stage of the shift register and the serial output to a logic low and will be latched (for a character time) by PE. Clear overrides preset.
11-17	A1-A7	Character Address	The seven-bit word on these inputs is decoded internally to address one of the 128 available characters.
18	LCI	Lower Case Inhibit	A high level on this input transforms the address of a lower case character into that of the equivalent upper case character. This is internally achieved by forcing A6 low whenever A7 and LCI are high.
19	AS	Address Strobe	A positive pulse on this input enters data from the A1-A7, LCI and CUR inputs into the holding register. The AS input may be left open, in which case it is pulled up to V_{CC} by an internal resistor. The data on the A1-A7, LCI and CUR inputs is then entered directly into the register without any latching action.
20	CUR	Cursor*	A high level on this input causes the cursor pattern to be superimposed on the pattern of the character addressed, i.e., the two patterns are OR-ed to generate the parallel inputs to the shift register. The standard cursor is presented as a double underscore on rows 10 and 11.
21	CLK	Clock	Frequency at which video (SO) is shifted.
22	NC	No Connection	
23	PE	Parallel Enable	A high level on this input loads the word at the output of the ROM into the shift register. The PE input must then be brought low again to allow the shift register to clock out this word.
24	GND	Ground	Ground

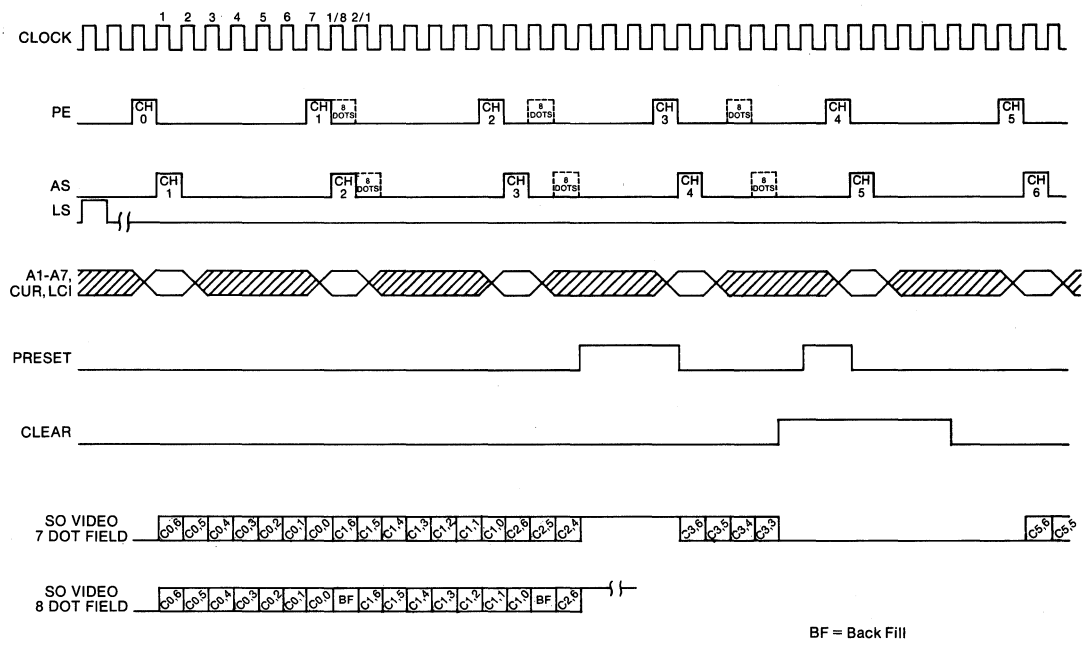


AC TIMING DIAGRAM

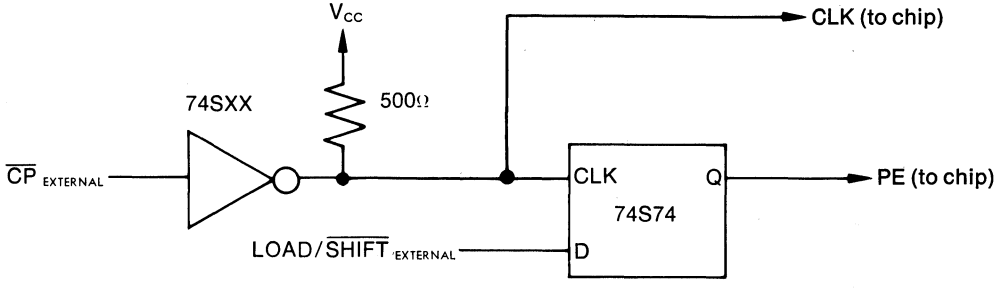


A7..A5 \ A4..A1	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0
000	R1 ... R11															
001	R1 ... R11															
010	R1 ... R11															
011	R1 ... R11															
100	R1 ... R11															
101	R1 ... R11															
110	R1 ... R11															
111	R1 ... R11															

*CONSULT FACTORY FOR CUSTOM FONT AND CURSOR OPTION.



TYPICAL VIDEO OUTPUT



NOTE

The differences between the CRT 7004 and CG5004L-1 are detailed below:

CG5004L-1	CRT 7004
1. If both the Preset and Clear inputs are brought high simultaneously the Serial Output is disabled and may be wire-ORed.	1. Clear overrides Preset, no output disable is possible.
2. All Inputs $V_{IH} = V_{CC} - 1.5v$	2. All inputs (except CLK) $V_{IH} = 2.0v$, min. CLK $V_{IH} = 4.3v$, min.
3. SO $V_{OL} = 0.4v$ @ $I_{OL} = 0.2mA$	3. SO $V_{OL} = 0.4v$ @ $I_{OL} = 0.4mA$ 74LSXX load
4. Shift Register is static	4. Shift Register is dynamic
5. Clear—directly forces the output low; when released, the output is determined by the state of the shift register output.	5. Clear directly forces the output low and will be latched (for a character time) by PE.
6. General Timing Differences—See Timing Diagram	6. General Timing Differences—See Timing Diagram

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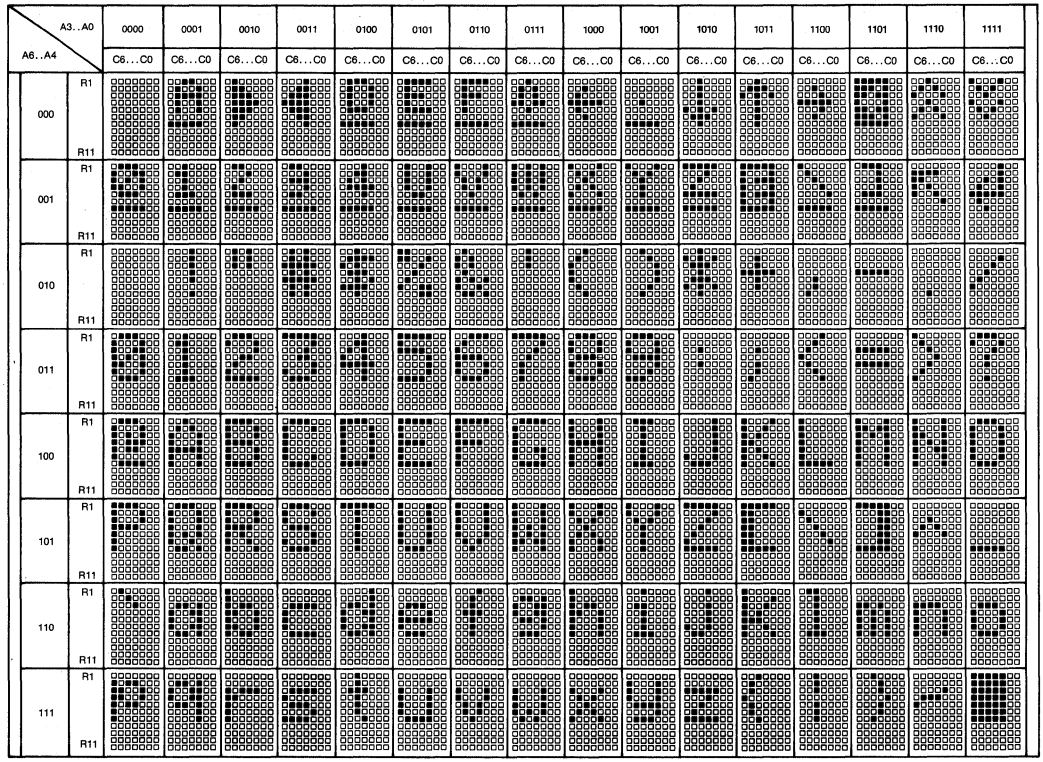
Dot Matrix Character Generator



The Cursor for the CRT 7004-003 is presented as a double underscore on Rows 8 and 9.

Printer

CHARACTER GENERATOR

Part Number	Description	Scan	Max Access Time	Power Supplies	Package	Page
CG 4103[3]	5x7x64	Column	1.2 μsec	+5, −12 or ±12	28 DIP	163-166

SHIFT REGISTER

Part Number	Description	Feature	Max Clock Freq.	Power Supply	Package	Page
SR 5015-XX[3]	Quad Static Shift Register Mask Programmable Length	Load, Recirculate, Shift Controls,	1 MHz	+5	16 DIP	167-170
SR 5015-80	Quad 80 Bit Static					
SR 5015-81	Quad 81 Bit Static					
SR 5015-133	Quad 133 Bit Static					
SR 5017	Quad 81 Bit	Shift Left/Shift Right, Recirculate Controls, Asynchronous clear	1 MHz	+5	16 DIP	171-174
SR 5018	Quad 133 Bit					

[3]May be custom mask programmed

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CG4103

CHARACTER GENERATOR

2240-Bit Programmable (ROM) 64 Characters of 5 x 7 Bits

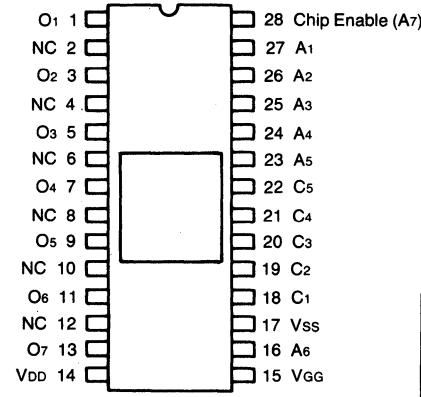
FEATURES

- ☐ Static Operation, no clocks required.
- ☐ 2240-Bit Capacity, fully decoded
- ☐ 64 Characters of 35 Bits (5 x 7)
- ☐ Column by Column Output—Column Scan
- ☐ TTL Compatible
- ☐ Wired "OR" Capability for memory expansion
- ☐ Power Supplies: +14v, −14v or +12v, −12v, or +5v, −12v
- ☐ Eliminates need for +12v power supply
- ☐ Single mask custom programming

APPLICATIONS

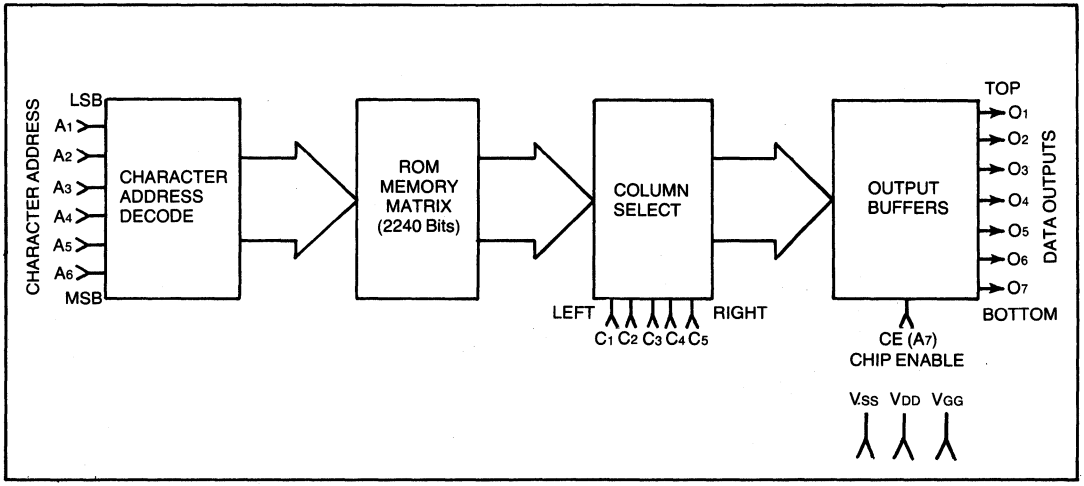
- ☐ Matrix Printers
- ☐ Vertical Scan Alphanumeric Displays
- ☐ Billboard and Stock Market Displays
- ☐ Strip Printer
- ☐ LED Matrix Arrays

PIN CONFIGURATION



NC = No Connection

BLOCK DIAGRAM



General Description

The CG4100 Series MOS Read Only Memories (ROMs) are designed specifically for dot-matrix character generation where column by column output data is desired. Each ROM contains 2240 bits of programmable storage, organized as 64 characters, each having 5 columns of 7 bits.

The output word appears as a 5 word sequence on each of the output lines. Sequence is controlled by the 5 Column Select lines. By strobing the first select line, the first group of 7 bits (first column) is obtained at the output. By sequentially strobing C_1 through C_5 the font of the addressed character would be displayed. The character address may remain fixed while the column select changes.

Since only 6 address bits are required in order to decode the 64 stored characters, the seventh bit (A_7) may be used as a chip enable. The chip enable (CE) in conjunction with the single ended open drain output buffers allow for memory expansion through wired "OR" connection.

The CG4100 Series contains an USASCII character font. Custom memory patterns are provided through the use of customer provided encoding sheets, tapes, or card decks.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... −25°C to + 85°C
Storage Temperature Range ..... −55°C to +150°C
Voltage on any Pin, with respect to V_{SS} ..... +0.3V to −30V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

RECOMMENDED OPERATING CONDITIONS ($-25°C \leq T_A \leq +85°C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Suppy Voltage	V_{SS}		0.0		V
Supply Voltage	V_{DD}	−12.0	−14.0	−16.0	V
Supply Voltage	V_{GG}	−24.0	−28.0	−29.0	V
Input Voltage, logic "O" Logic "O"=most positive level	V_{IH}	$V_{SS}-1.5$	V_{SS}		V
Input Voltage, logic "I" Logic "I"=most negative level	V_{IL}		V_{DD}	$V_{SS}-11$	V

Note: The design of the CG4100 permits a broad range of operation that allows the user to take advantage of readily available power supplies; e.g. +5V, −12V. See "Operational Interface—To/From TTL logic" diagram.

ELECTRICAL CHARACTERISTICS ($V_{SS}=+14v$, $V_{GG}=-14v$, V_{DD}=Ground, $T_A=25°C$, unless otherwise noted)

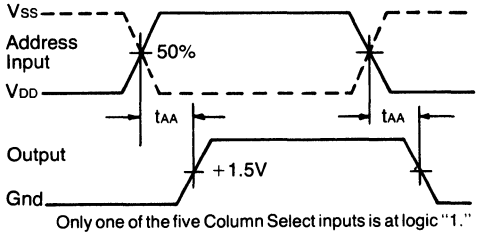
Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output Blank Current	I_{OB}	—	—	10	μa	V_{DD} applied to output see Note 1.
Output Dot Current	I_{OD}	2.5	—	—	ma	V_{DD} applied to output see Note 1.
Input Leakage Current	I_{IN}	—	—	10	μa	V_{IN}=OV
Output Voltage	V_O	—	2.0	—	V	I_O=0.5ma
		—	5.0	—	V	I_O=2.0ma
Address Access Time	t_{AA}	—	—	1200	ns	
Column Select Access Time	t_{CA}	—	—	600	ns	
Chip Enable Access Time	t_{CE}	—	—	400	ns	
Power Dissipation		—	—	400	mw	Output unconnected

Note 1: An output dot is defined as the ON state of the MOS output transmitter. An output blank is defined as the OFF state.

Description of Pin Functions

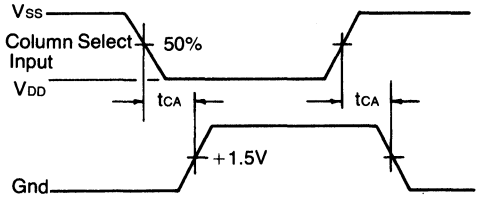
Pin No.	Symbol	Name	Function
1, 3, 5, 7 9, 11, 13	O_1, O_2, O_3, O_4 O_5, O_6, O_7	Outputs	7 Data Outputs
14	V_{DD}	V_{DD}	Usually connected to Ground
15	V_{GG}	V_{GG}	Negative power supply: −14v or −12v
16	A_6	Address	Bit 6 of the character address
17	V_{SS}	V_{SS}	Positive power supply: +14v or +12v or +5v
18-22	C_1-C_5	Column Select	Column Select inputs
23-27	A_5-A_1	Address	Bits 1 through 5 of the character address
28	CE(A_7)	Chip Enable	Chip Enable for memory expansion

ADDRESS ACCESS TIMING



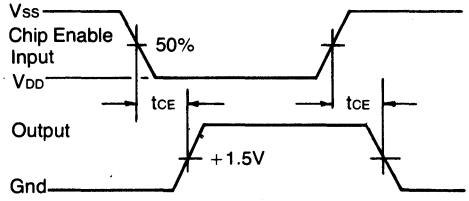
Only one of the five Column Select inputs is at logic "1."
Chip Enable input is at logic "1."

COLUMN SELECT ACCESS TIMING



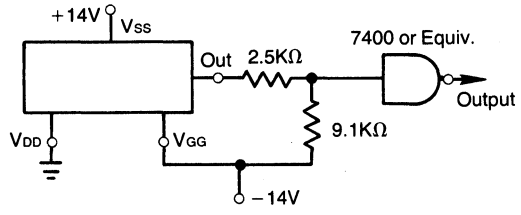
All Column Select inputs are at logic "0" except one under test.
Address inputs are set in a dc state.
Chip Enable input is at logic "1."

CHIP ENABLE ACCESS TIMING



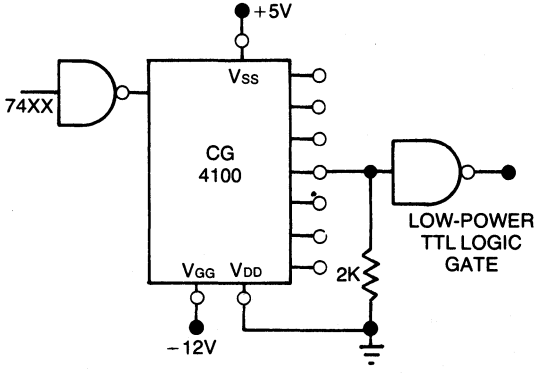
Only one of the five Column Select inputs is a logic "1."
Address inputs are set in a dc state.

AC TEST CIRCUIT

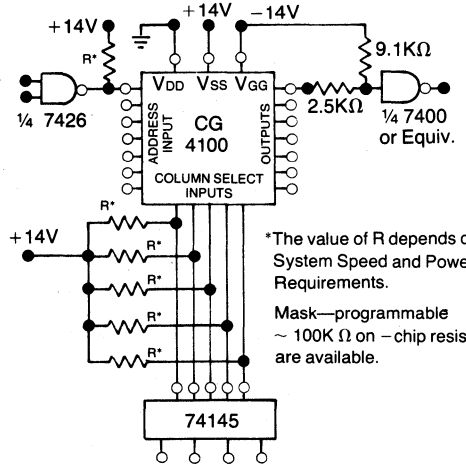


$t_r = t_f < 50$ ns for all timing diagram forcing functions.
All output waveforms are measured at the output of the 7400 TTL gate.

OPTIONAL INTERFACE TO/FROM TTL LOGIC

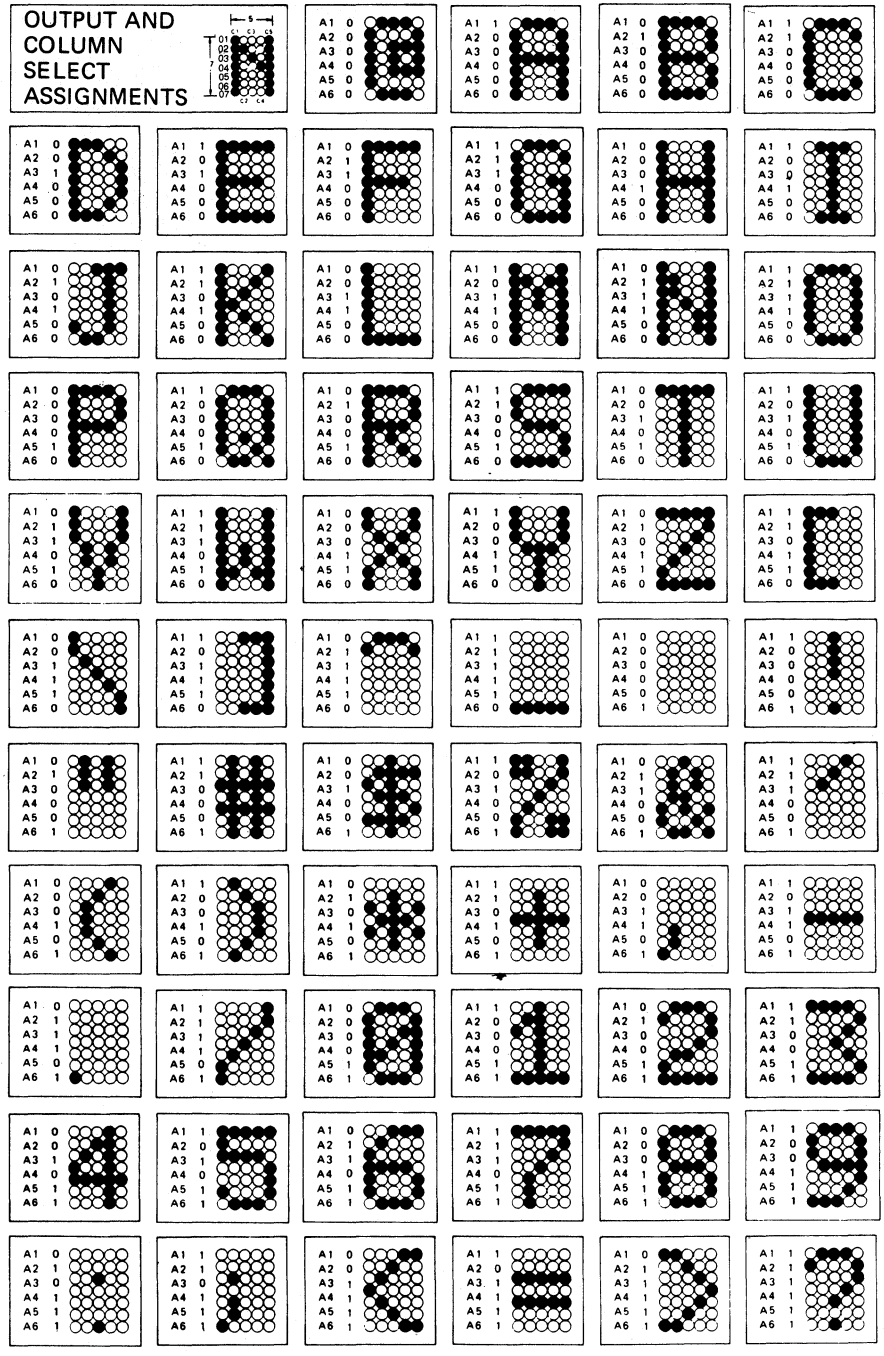


INTERFACE TO TTL LOGIC



*The value of R depends on System Speed and Power Requirements.

Mask—programmable ~ 100K Ω on −chip resistors are available.



Pin-for-Pin Equivalent for: TMS 4103 MK2002 S8499.

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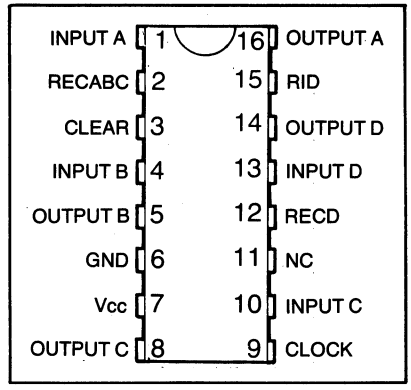
SR 5015-XXX
SR 5015-80
SR 5015-81
SR 5015-133

Quad Static Shift Register

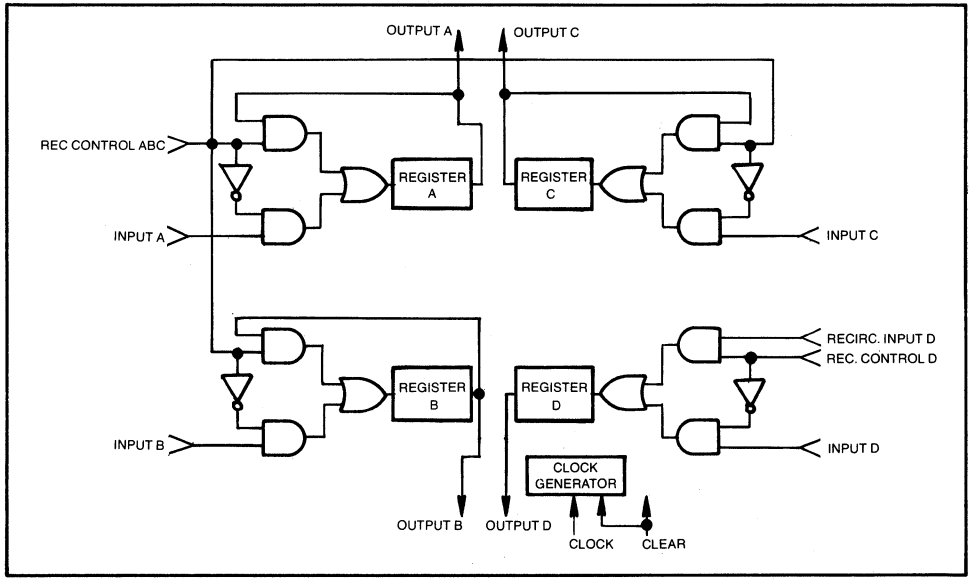
FEATURES
- ☐ COPLAMOS® N Channel Silicon Gate Technology
- ☐ Variable Length—Single Mask Programmable—1 to 134 bits
- ☐ Directly TTL-compatible on all inputs, outputs, and clock
- ☐ Clear function
- ☐ Operation guaranteed from DC to 1.0 MHz
- ☐ Recirculate logic on-chip
- ☐ Single +5.0V power supply
- ☐ Low clock input capacitance
- ☐ 16 pin ceramic DIP Package
- ☐ Pin for Pin replacement for AMI S2182, 83, 85

APPLICATIONS
- ☐ Memory Buffering
- ☐ Unique Buffering Lengths
- ☐ Terminals

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION V

General Description

The SMC SR 5015-XXX is a quad static shift register family fabricated using SMC's COPLAMOS® N channel silicon gate process which provides a higher functional density and speed on a monolithic chip than conventional MOS technology. The COPLAMOS® process provides high speed operation, low power dissipation, low clock input capacitance, and single +5 volt power supply operation.

These shift registers can be driven by either T²L circuits or by MOS circuits and provide driving capability to MOS or T²L circuits. This device consists of four separate static shift registers with independent input and output terminals and logic for loading, recirculating or shifting information. The SR 5015-80, SR 5015-81, and SR 5015-133 are respectively 80, 81, and 133 bit quad shift registers.

The recirculate control pin is common for registers A, B, and C. Register D has an independent recirculate control pin as well as a recirculate input pin.

A clear pin has been provided that will cause the shift register to be cleared when the pin is at V_{CC}. A single T²L clock is required for operation.

The transfer of data into the register is accomplished on the low-to-high transition of the clock with the recirculate control low. For long term data storage the clock may be stopped and held in either logic state. Recirculate occurs when the recirculate control is high. Output data appears on the low-to-high transition of the clock pulse.

Bits 81 and 133 are available for flag storage.

This device has been designed to be used in high speed buffer storage systems and small recirculating memories.

Special custom configurations are achieved via single mask programming in lengths of 1 to 134 bits.

MAXIMUM GUARANTEED RATINGS*

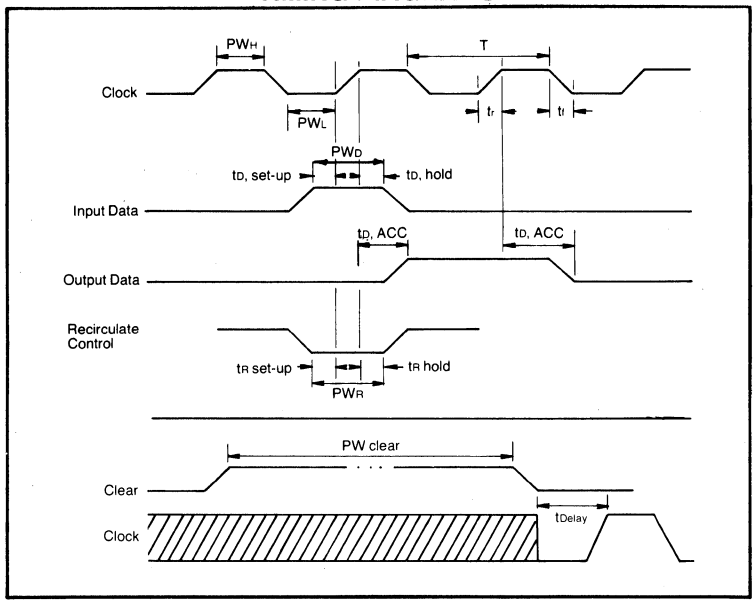
Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}−1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	V_{CC}−1.5	4.0		V	I_{OH}=100μa
INPUT LEAKAGE CURRENT			1.0	μa	V_{IN}=V_{CC}
CLOCK, CLEAR			25	pf	
All Other			10	pf	
POWER SUPPLY CURRENT			80	ma	
A.C. Characteristics					T_A=+25°C
CLOCK					
PW_H	300			ns	
PW_L	600			ns	
Transition, t_r, t_f		0.02	1.0	μs	
Repetition Rate, 1/T	0		1.0	MHz	
t Delay	300			ns	
INPUT DATA					
t_D, set-up	100			ns	
t_D, hold	200			ns	
PW_D	300			ns	
OUTPUT DATA					
t_D, ACC		200	350	ns	
RECIRCULATE CONTROL					
t_R, set-up	200			ns	
t_R, hold	300			ns	
PW_R	500			ns	
CLEAR					
PW_{CLEAR}	20			μs	

TIMING DIAGRAMS

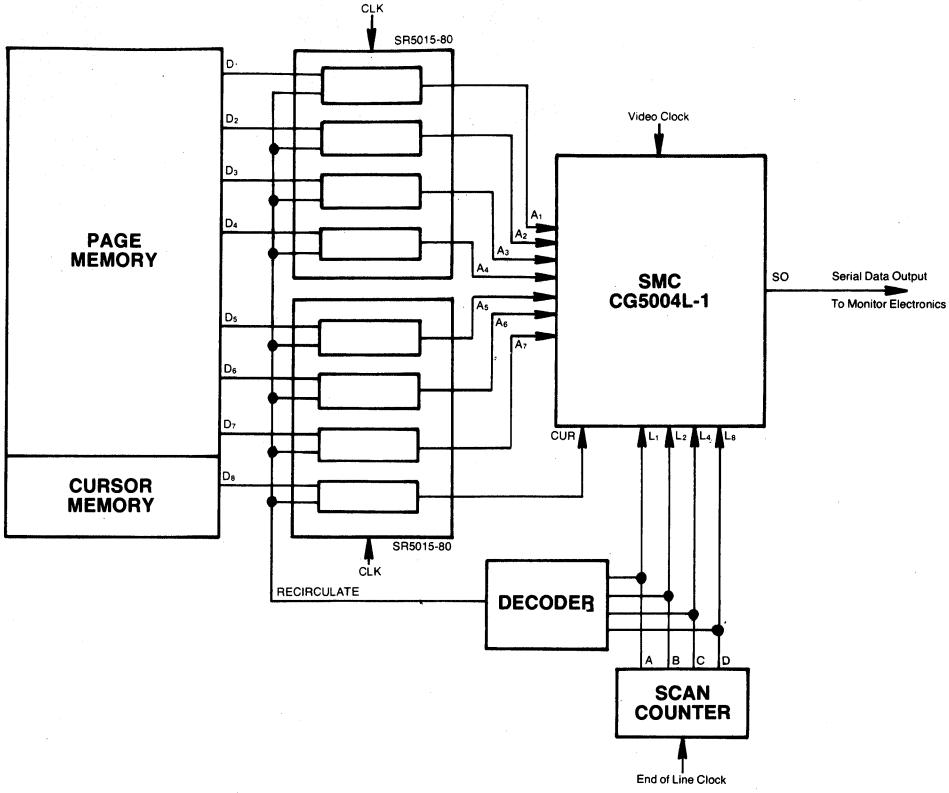


SECTION V

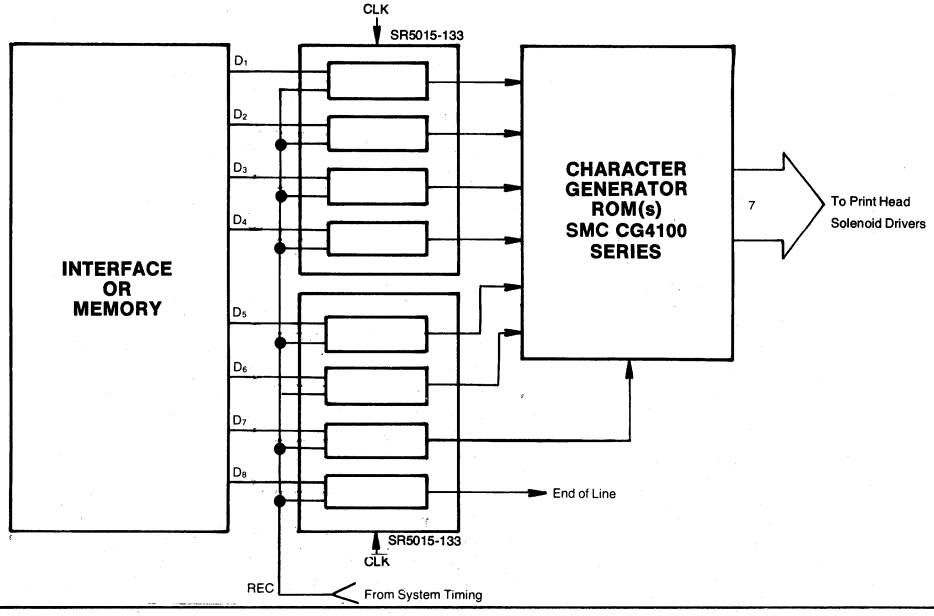
Description of Pin Functions

Pin No.	Symbol	Name	Function
1	A	Input A	Input signal which is either high or low depending on what word is to be loaded into shift register.
2	RECABC	Recirculate ABC	Input signal when high disconnects inputs from registers and connects outputs to inputs, thus recirculating data. Recirculates only A, B, C outputs.
3	CLR	Clear	Input signal when high forces outputs to a low state immediately and clears all the registers.
4	B	Input B	Input signal for B register.
5	O_B	Output B	Output signal for B register.
6	GND	GND	Power supply Ground.
7	V_{CC}	+5 Volt	5 volt power supply.
8	O_C	Output C	Output signal for C register.
9	CLK	Clock Input	Input signal which is normally low and pulses high to shift data into the registers. The data is clocked in on low to high edge of clock.
10	C	Input C	Input signal for C register.
11	NC	NC	
12	RECD	Recirculate Control D	Input signal which is normally low and, when goes high, disconnects Input D to register and connects Recirculate Input D to register.
13	D	Input D	Input signal for D register.
14	O_D	Output D	Output signal for D register.
15	RID	Recirculate Input D	Input signal which is the input to the D register when Recirculate Control D is high: RECD=1.
16	O_A	Output A	Output signal for A register.

Line Buffer for CRT Display . . . 80 Characters per line.



Line Buffer for Matrix Printer . . . 132 Characters per line.



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SR 5017
SR 5018

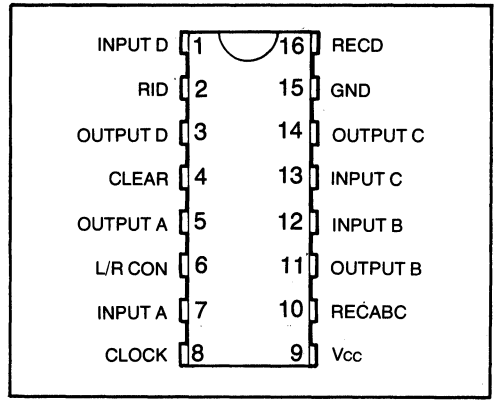
Quad Static Shift Right/Shift Left Shift Register

Last In First Out Buffer
LIFO

FEATURES

- ☐ COMPLAMOS® N-Channel Silicon Gate Technology.
- ☐ Quad 81 bit or Quad 133 bit
- ☐ Directly Compatible with T²L, MOS
- ☐ Operation Guaranteed from DC to 1.0MHz
- ☐ Recirculate logic on-chip
- ☐ Single +5.0V power supply
- ☐ Low clock input capacitance
- ☐ Single phase clock at T²L levels
- ☐ Clear function
- ☐ 16-pin Ceramic DIP Package

PIN CONFIGURATION

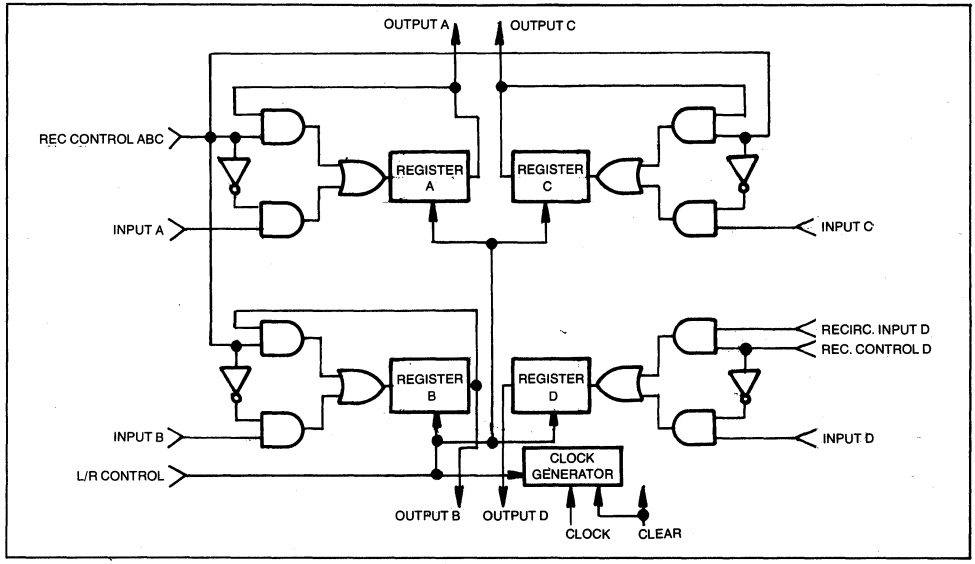


APPLICATIONS

- ☐ Bi-Directional Printer
- ☐ Computers—Push Down Stack—LIFO
- ☐ Buffer data storage—memory buffer
- ☐ Delay lines—delay line processing
- ☐ Digital filtering
- ☐ Telemetry Systems
- ☐ Terminals
- ☐ Peripheral Equipment

SECTION V

BLOCK DIAGRAM



General Description

The SMC SR 5017 and SR 5018 are quad 133 (SR 5017) and quad 81 (SR 5018) bit static shift registers utilizing SMC's COPLAMOS® N channel silicon gate process. The COPLAMOS® process provides high speed operation, low power dissipation, low clock input capacitance, and requires only a single +5 volt power supply.

These shift registers can be driven by either T²L circuits or by MOS circuits and provide driving capability to MOS to T²L circuits.

This device consists of four separate static shift registers with independent input and output terminals and logic for loading, recirculating or shifting information right or left. This shift left/shift right (L/R Control) control input is common to all registers.

The recirculate control input is common for registers A, B, and C. Register D has an independent recirculate control input as well as a Recirculate Input.

A Clear input has been provided that will cause the shift register to be cleared when the input is at V_{CC}. A single T²L clock input is required for operation.

The transfer of data into the register is accomplished on the low-to-high transition of the clock with the recirculate control low. For long term data storage the clock may be stopped and held in either logic state. Recirculate occurs when the recirculate control is high. Output data appears on the low-to-high transition of the clock pulse.

Bits 81 or 133 are available for flag storage.

MAXIMUM GUARANTEED RATINGS*

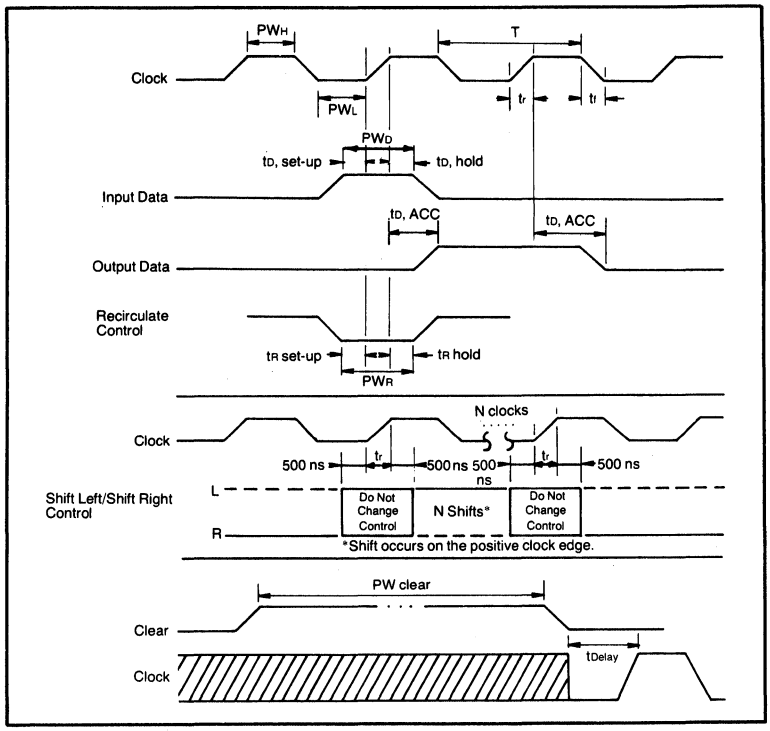
Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}—1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	V_{CC}—1.5	4.0		V	I_{OH}=100μa
INPUT LEAKAGE CURRENT			1.0	μa	V_{IN}=V_{CC}
CLOCK, CLEAR			25	pf	
All Other			10	pf	
POWER SUPPLY CURRENT			100	ma	
A.C. Characteristics					T_A=+25°C
CLOCK					
PW_H	300			ns	
PW_L	600			ns	
Transition, t_r, t_f		0.02	1.0	μs	
Repetition Rate, 1/T	0		1.0	MHz	
t Delay	500			ns	
INPUT DATA					
t_D, set-up	150			ns	
t_D, hold	150			ns	
PW_D	300			ns	
OUTPUT DATA					
t_D, ACC		200	350	ns	
RECIRCULATE CONTROL					
t_R, set-up	200			ns	
t_R, hold	300			ns	
PW_R	500			ns	
CLEAR					
PW_{CLEAR}	20			μs	

Timing Diagram

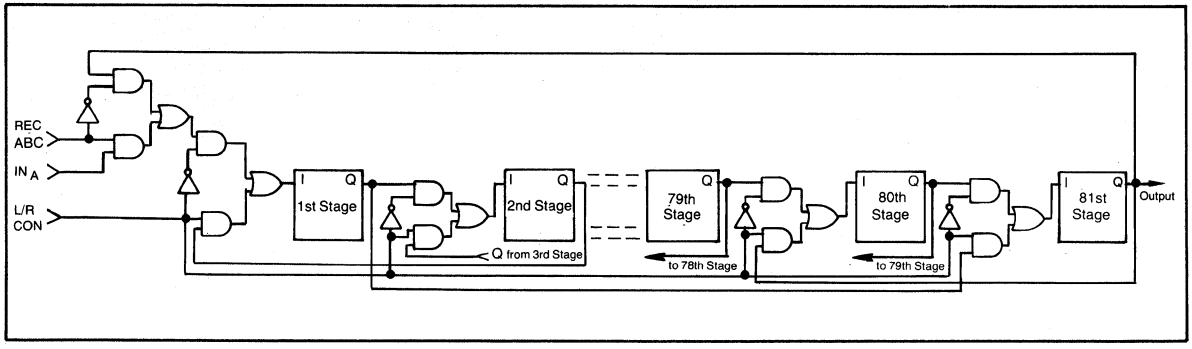


SECTION V

Description of Pin Functions

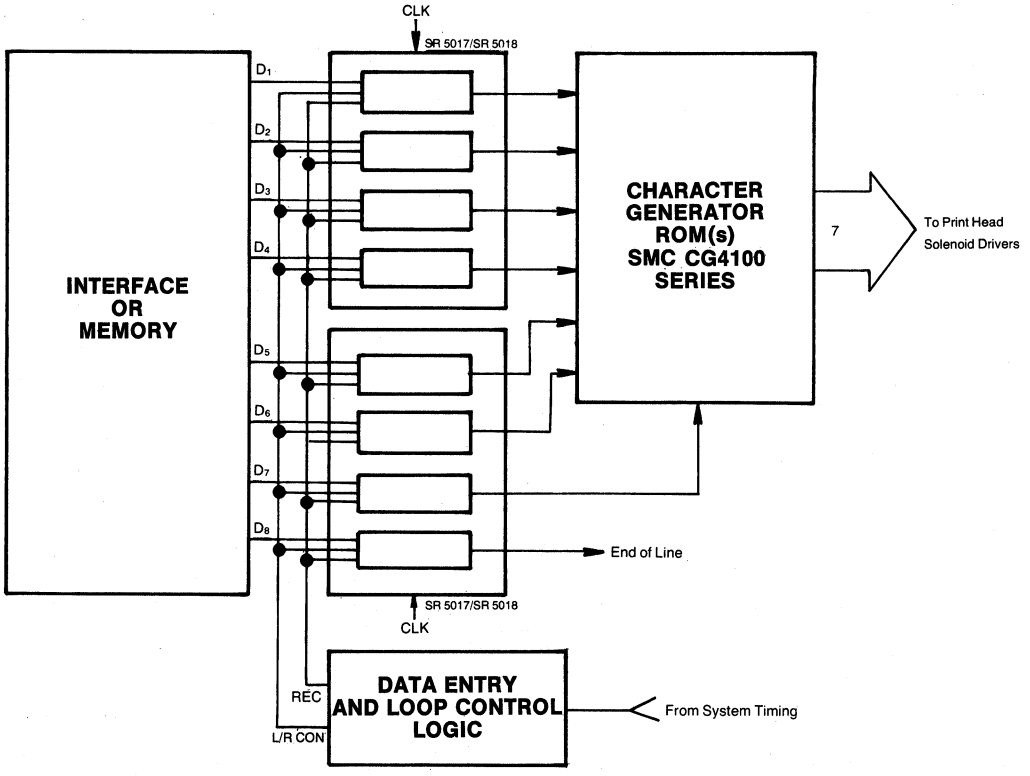
Symbol	Name	Pin	Function
D	Input D	1	Input signal for D register.
RID	Recirculate Input D	2	Input signal which is the input to the D register when recirculate control D is high: RECD = 1.
O_D	Output D	3	Output signal for D register.
CLR	Clear	4	Input signal when high forces outputs to a low state immediately and clears all the registers.
O_A	Output A	5	Output signal for A register.
L/R CON	Shift Left/Shift Right Control	6	Input signal which is low for loading data and for shifting right. When L/R CON is high, the register will shift left.
A	Input A	7	Input signal which is either high or low depending on what word is to be loaded into shift register.
CLK	Clock Input	8	Input signal which is normally low and pulses high to shift data into the registers. The data is clocked in on low to high edge of clock.
V_{CC}	5 Volt	9	5 volt power supply.
RECABC	Recirculate ABC	10	Input signal when high disconnects inputs from registers and connects outputs to inputs, thus recirculating data. Recirculates only A, B, C outputs.
O_B	Output B	11	Output signal for B register.
B	Input B	12	Input signal for B register.
C	Input C	13	Input signal for C register.
O_C	Output C	14	Output signal for C register.
GND	GND	15	Ground.
RECD	Recirculate Control D	16	Input signal which is normally low and, when goes high, disconnects Input D to register and connects RECIRCULATE INPUT D to register.

Logic Diagram



APPLICATION

Line Buffer for Bidirectional Matrix Printer . . . 80/132 characters per line



Baud Rate Generator

All Baud Rate Generators are programmable dividers capable of providing 16 output frequencies* for UARTs or USARTs from either an on-chip crystal oscillator or an external frequency input. "T" versions utilize an external frequency input only. Dual Baud Rate Generators provide two output frequencies simultaneously for full duplex communication.

Baud Rate Generators providing all standard baud rates from various popular crystal frequencies are available. In addition the baud rate generator may be custom mask programmed for other divisors.

*except as noted

Part Number	Description	Features	Power Supplies	Package	Page
COM 5016	Dual Baud Rate Generator	On-chip oscillator or external frequency input	+5, +12	18 DIP	177-178
COM 5016T[3]	Dual Baud Rate Generator	External frequency input	+5, +12	18 DIP	177-178
COM 5026	Single Baud Rate Generator	On-chip oscillator or external frequency input	+5, +12	14 DIP	179-180
COM 5026T[3]	Single Baud Rate Generator	External frequency input	+5, +12	14 DIP	179-180
COM 5036	Dual Baud Rate Generator	COM 5016 with additional output of input frequency ÷ 4	+5, +12	18 DIP	181-182
COM 5036T[3]	Dual Baud Rate Generator	COM 5016T with additional output of input frequency ÷ 4	+5, +12	18 DIP	181-182
COM 5046	Single Baud Rate Generator	COM 5026 with additional output of input frequency ÷ 4	+5, +12	14 DIP	183-188
COM 5046T[3]	Single Baud Rate Generator	COM 5026T with additional output of input frequency ÷ 4	+5, +12	14 DIP	183-188
COM 8046	Single Baud Rate Generator	32 baud rates; 1X, 16X, 32X clock outputs; single +5 volt supply	+5	16 DIP	189-190
COM 8046T[3]	Single Baud Rate Generator	COM 8046 with external frequency input only	+5	16 DIP	189-190
COM 8116	Dual Baud Rate Generator	Single +5 volt version of COM 5016	+5	18 DIP	191-192
COM 8116T[3]	Dual Baud Rate Generator	Single +5 volt version of COM 5016T	+5	18 DIP	191-192
COM 8126	Single Baud Rate Generator	Single +5 volt version of COM 5026	+5	14 DIP	193-194
COM 8126T[3]	Single Baud Rate Generator	Single +5 volt version of COM 5026T	+5	14 DIP	193-194
COM 8136	Dual Baud Rate Generator	Single +5 volt version of COM 5036	+5	18 DIP	195-196
COM 8136T[3]	Dual Baud Rate Generator	Single +5 volt version of COM 5036T	+5	18 DIP	195-196
COM 8146	Single Baud Rate Generator	Single +5 volt version of COM 5046	+5	14 DIP	197-198
COM 8146T[3]	Single Baud Rate Generator	Single +5 volt version of COM 5046T	+5	14 DIP	197-198

[3]May be custom mask programmed

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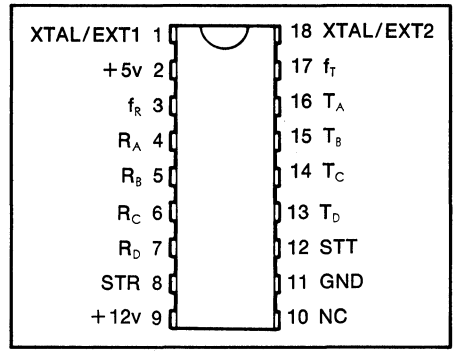
COM 5016
COM 5016T

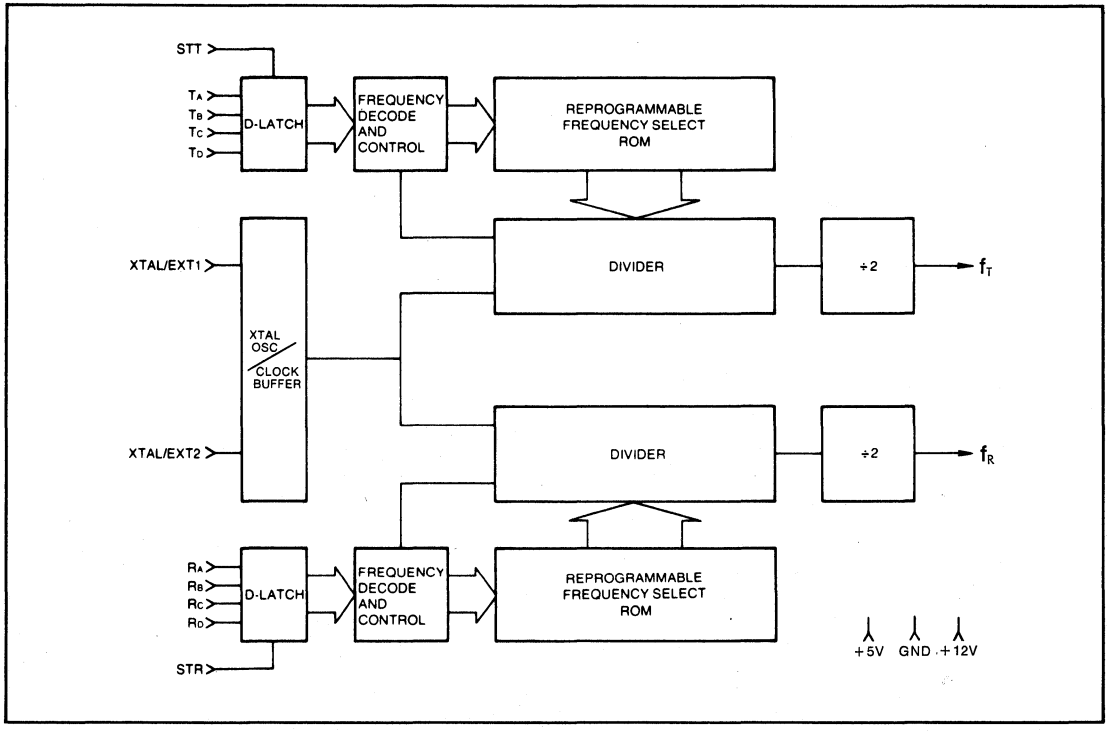
Dual Baud Rate Generator
Programmable Divider

FEATURES
- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION VI

General Description

The Standard Microsystems COM 5016 Dual Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 32 externally selectable frequencies.

The COM 5016 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, on each of the independent dividers, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs on each divider section may be strobe (150ns) or DC loaded. As the COM 5016 is a dual baud rate generator, full duplex (independent receive and transmit frequencies) operation is possible.

The COM 5016 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using one of the frequency outputs it is possible to generate additional divisions of the master clock frequency by cascading COM 5016's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5016 can be driven by either an external crystal or TTL logic level inputs; COM 5016T is driven by TTL logic level inputs only.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	V_{DD}	Power Supply	+12 volt supply
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

For electrical characteristics, see page 185.

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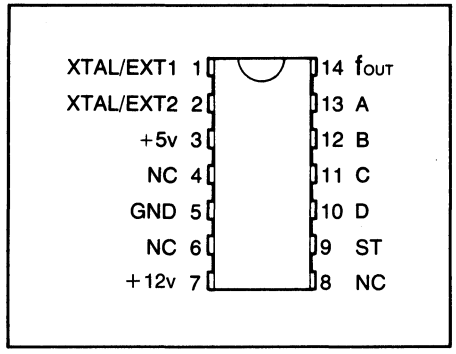
COM 5026
COM 5026T

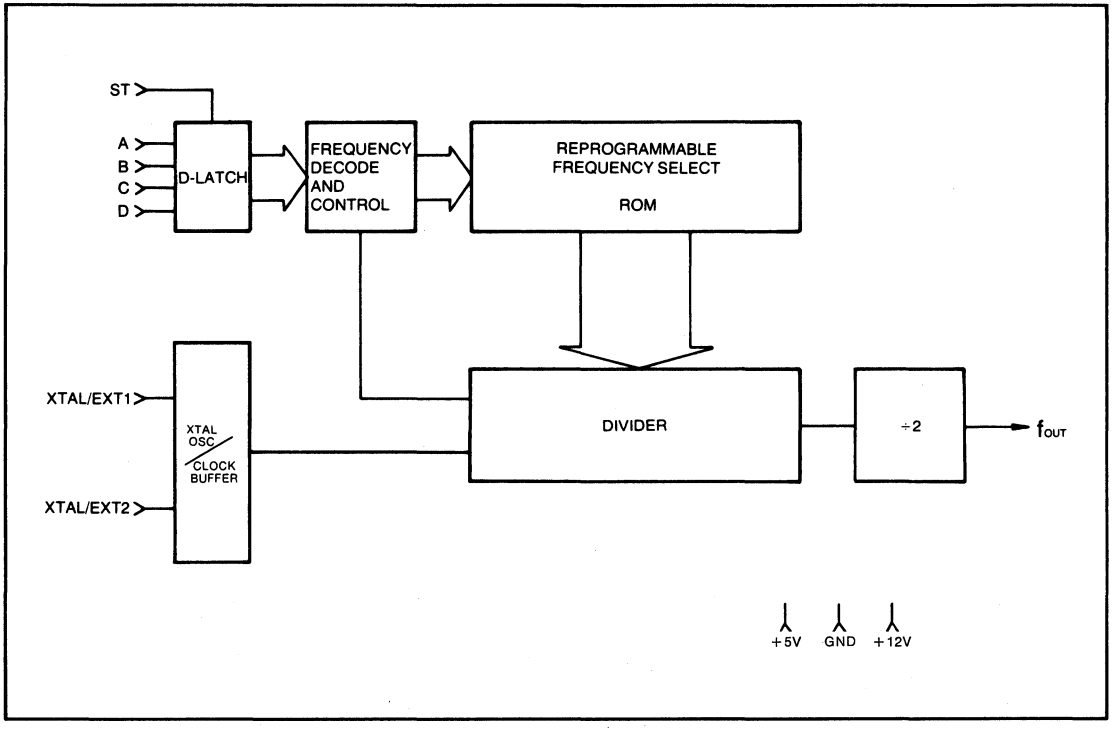
Baud Rate Generator
Programmable Divider

FEATURES
- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION VI

GENERAL DESCRIPTION

The Standard Microsystems COM 5026 Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 16 externally selectable frequencies.

The COM 5026 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs may be strobe (150ns) or DC loaded.

The COM 5026 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using the frequency output, it is possible to generate additional divisions of the master clock frequency by cascading COM 5026's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5026 can be driven by either an external crystal or TTL logic level inputs; COM 5026T is driven by TTL logic level inputs only.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt Supply
4,6,8	NC	No Connection	
5	GND	Ground	Ground
7	V_{DD}	Power Supply	+12 volt Supply
9	ST	Strobe	A high-level strobe loads the Input Address (A_A, A_B, A_C, A_D) into the Input Address register. This input may be strobed or hard wired to a high-level,
10-13	A_D, A_C, A_B, A_A	Input Address	The logic level on these inputs. as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency as selected by the Input Address.

For electrical characteristics, see page 185.

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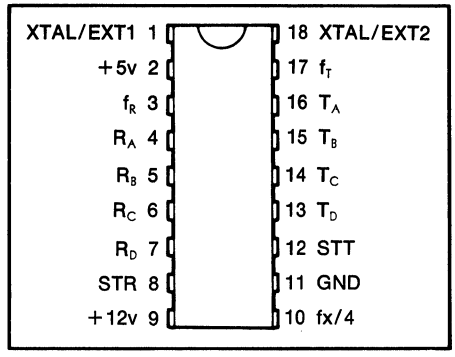
COM 5036
COM 5036T

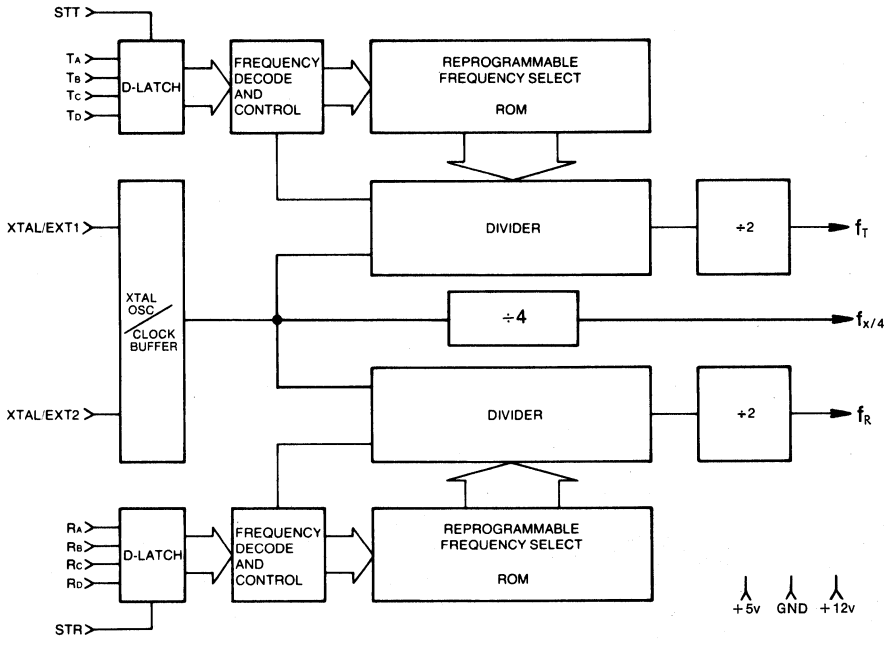
Dual Baud Rate Generator
Programmable Divider

FEATURES
- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ High frequency reference output
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION VI

General Description

The Standard Microsystems COM 5036 Dual Baud Rate Generator/Programmable Divider is an N-channel COP-LAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 32 externally selectable frequencies.

The COM 5036 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, on each of the independent dividers, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs on each divider section may be strobe (150ns) or DC loaded. As the COM 5036 is a dual baud rate generator, full duplex (independent receive and transmit frequencies) operation is possible.

The COM 5036 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using one of the frequency outputs it is possible to generate additional divisions of the master clock frequency by cascading COM 5036's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5036 can be driven by either an external crystal or TTL logic level inputs; COM 5036T is driven by TTL logic level inputs only.

The COM 5036 provides a high frequency reference output at one-quarter (1/4) the XTAL/EXT input frequency.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	V_{DD}	Power Supply	+12 volt supply
10	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divider Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

For electrical characteristics, see page 185.

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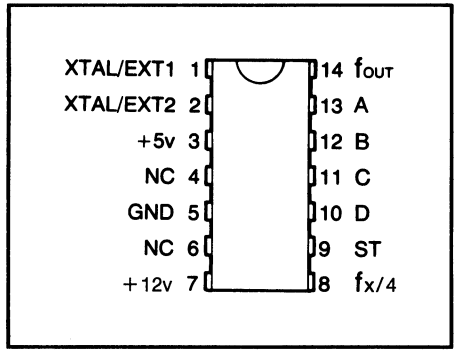
COM 5046
COM 5046T

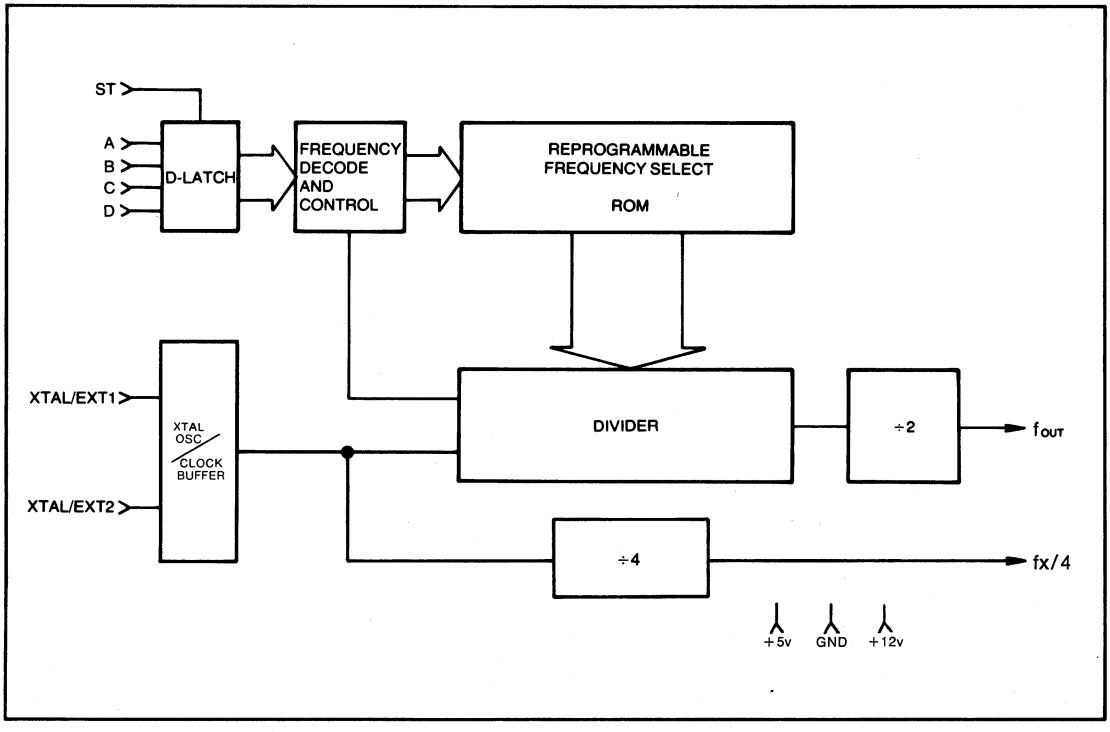
Baud Rate Generator
Programmable Divider

FEATURES
- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ High frequency reference output
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION VI

GENERAL DESCRIPTION

The Standard Microsystems COM 5046 Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 16 externally selectable frequencies.

The COM 5046 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs; as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs may be strobe (150ns) or DC loaded.

The COM 5046 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using the frequency output, it is possible to generate additional divisions of the master clock frequency by cascading COM 5046's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5046 can be driven by either an external crystal or TTL logic level inputs; COM 5046T is driven by TTL logic level inputs only.

The COM 5046 provides a high frequency reference output at one-quarter (1/4) the XTAL/EXT input frequency.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt Supply.
4,6	NC	No Connection	
5	GND	Ground	Ground
7	V_{DD}	Power Supply	+12 volt Supply.
8	$f_{X/4}$	Reference Frequency	High frequency reference output @ (1/4) f_{IN}
9	ST	Strobe	A high-level strobe loads the Input Address (A_A, A_B, A_C, A_D) into the Input Address register. This input may be strobed or hard wired to a high-level,
10-13	A_D, A_C, A_B, A_A	Input Address	The logic level on these inputs. as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency as selected by the Input Address.

For electrical characteristics, see page 185.

ELECTRICAL CHARACTERISTICS COM5016, COM5016T, COM5026, COM5026T, COM5036, COM5036T, COM5046, COM5046T

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

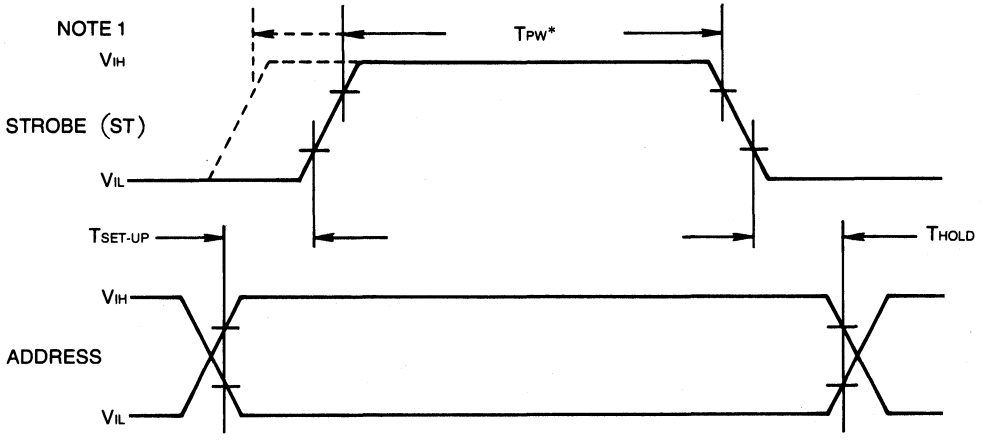
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding XTAL inputs
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 1.6ma
			0.5	V	I_{OL} = 3.2ma
High-level, V_{OH}	V_{CC}−1.5	4.0		V	I_{OH} = 100μA
INPUT CURRENT					
Low-level, I_{IL}			0.3	mA	V_{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
EXT INPUT LOAD		8	10		Series 7400 unit loads
POWER SUPPLY CURRENT					
I_{CC}		28	45	mA	
I_{DD}		12	22	mA	
A.C. CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY		5.0688		MHz	XTAL, EXT
PULSE WIDTH					
Clock					50% Duty Cycle ±5%
Strobe	150		DC	ns	See Note 1.
INPUT SET-UP TIME					
Address	50			ns	See Note 1.
INPUT HOLD TIME					
Address	50			ns	
STROBE TO NEW FREQUENCY DELAY			3.5	μs	$=1/f_{IN}$ (18)

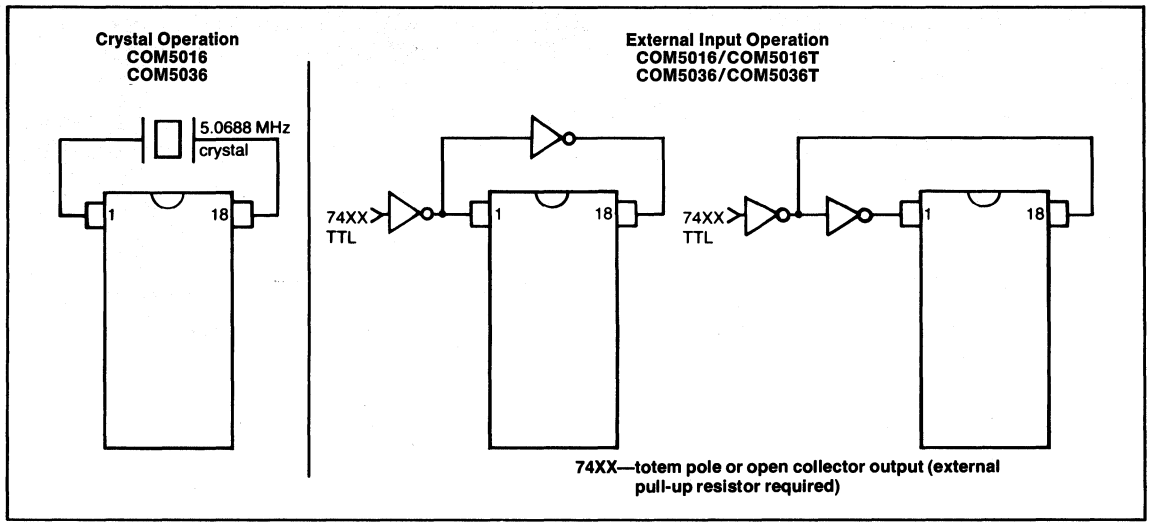
Note 1: Input set-up time can be decreased to ≥ 0ns by increasing the minimum strobe width by 50ns to a total of 200ns.

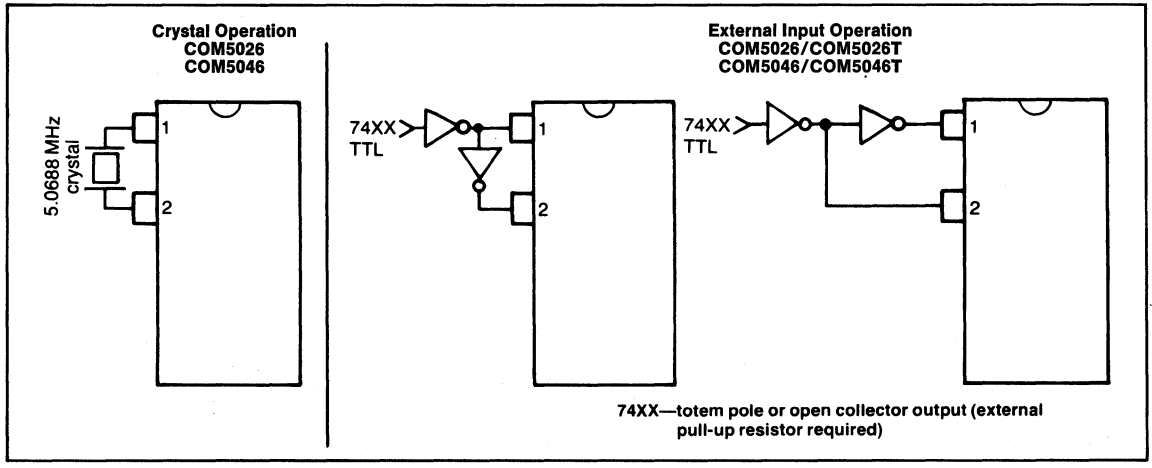
TIMING DIAGRAM



*Address need only be valid during the last T_{PW}, Min time of the input strobe.

SECTION VI





For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

Crystal Specifications

User must specify termination (pin, wire, other)
Prefer: HC-18/U or HC-25/U
Frequency — 5.0688 MHz, AT cut
Temperature range 0°C to 70°C
Series resistance $<50\ \Omega$
Series Resonant
Overall tolerance ± .01%
or as required

Crystal manufacturers (Partial List)

Northern Engineering Laboratories
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

Bulova Frequency Control Products
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

CTS Knights Inc.
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

Crystek Crystals Corporation
1000 Crystal Drive
Fort Myers, Florida 33901
(813) 936-2109

APPLICATIONS INFORMATION

Charge pump techniques using the +5 volt power supply can be used to generate the +12 volt power supply required. The +12 volt power supply of figure 1 will supply the 22 milli-amps that is typically required.

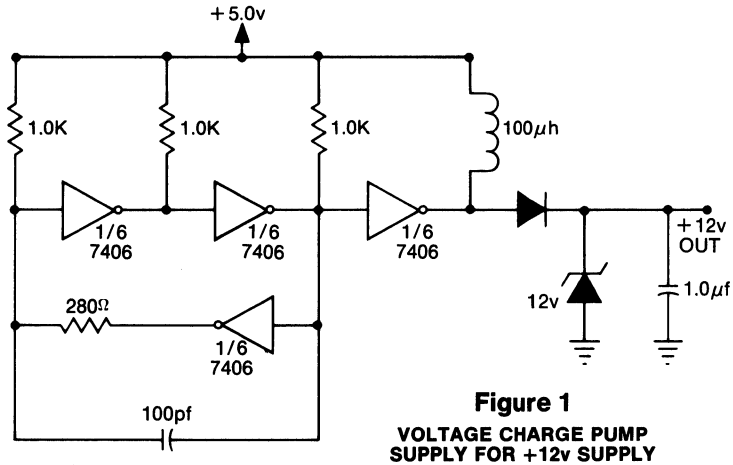


Figure 1
VOLTAGE CHARGE PUMP SUPPLY FOR +12v SUPPLY

When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that the clamp circuit of figure 2 or a Semtech* bi-polarity silicon transient suppressor such as the 1N6110 be used.

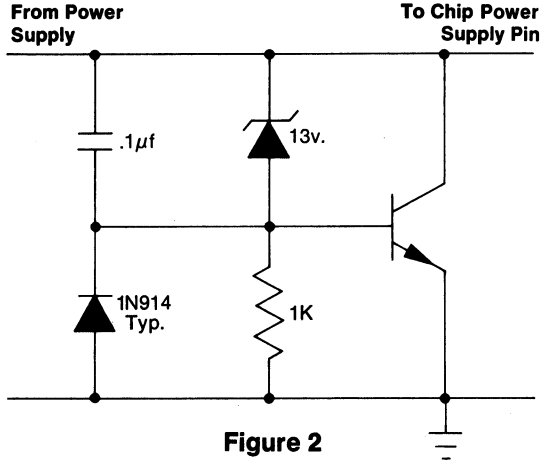


Figure 2
OVER-VOLTAGE PROTECTION CIRCUIT

*SEMTECH CORPORATION
652 Mitchel Road
Newbury Park, California 91320
213-628-5392

SECTION VI

Baud Rate Generator Output Frequency Options

Table 1. (16X clock)

CRYSTAL FREQUENCY = 5.0688 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19.200	307.2	316.8	3.125	50/50	16

Table 2. (16X clock)

CRYSTAL FREQUENCY = 4.9152 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7589	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

Table 3. (32X clock)

CRYSTAL FREQUENCY = 5.0688 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 32X Clock	Actual Frequency 32X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	1.6 KHz	1.6 KHz	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.306	.06	*	1177
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	316.8	3.125	50/50	16
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

Table 4. (16X clock)

CRYSTAL FREQUENCY = 5.0688 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	—	—	6.93406 KHz	—	—	731
0	0	0	1	—	—	6.91514	—	—	733
0	0	1	0	—	—	6.89633	—	—	735
0	0	1	1	—	—	6.87761	—	—	737
0	1	0	0	—	—	6.84049	—	—	741
0	1	0	1	—	—	6.82207	—	—	743
0	1	1	0	—	—	6.80376	—	—	745
0	1	1	1	—	—	6.74940	—	—	751
1	0	0	0	45.45	0.7272 KHz	0.72723	—	50/50	6970
1	0	0	1	56.88	0.91008	0.91018	0.01	*	5569
1	0	1	0	58.30	0.93280	0.93290	0.02	*	5433
1	0	1	1	66.66	1.06656	1.06666	—	50/50	4752
1	1	0	0	74.20	1.18720	1.18735	0.01	*	4269
1	1	0	1	165.00	2.64000	2.64000	—	50/50	1920
1	1	1	0	200.00	3.20000	3.20000	—	50/50	1584
1	1	1	1	1050.00	16.80000	16.83980	0.24	*	301

Table 5. (16X clock)

CRYSTAL FREQUENCY = 4.608 MHz

Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	5760
0	0	0	1	75	1.2	1.2	—	50/50	3840
0	0	1	0	110	1.76	1.76012	0.007	50/50	2618
0	0	1	1	134.5	2.152	2.15226	0.01	*	2141
0	1	0	0	150	2.4	2.4	—	50/50	1920
0	1	0	1	300	4.8	4.8	—	50/50	960
0	1	1	0	600	9.6	9.6	—	50/50	480
0	1	1	1	1200	19.2	19.2	—	50/50	240
1	0	0	0	1800	28.8	28.8	—	50/50	160
1	0	0	1	2000	32.0	32.0	—	50/50	144
1	0	1	0	2400	38.4	38.4	—	50/50	120
1	0	1	1	3600	57.6	57.6	—	50/50	80
1	1	0	0	4800	76.8	76.8	—	50/50	60
1	1	0	1	7200	115.2	115.2	—	50/50	40
1	1	1	0	9600	153.6	153.6	—	50/50	30
1	1	1	1	19200	307.2	307.2	—	*	15

OUTPUT FREQUENCY OPTIONS

Part No.	Dash Number				
	Table 1	Table 2	Table 3	Table 4	Table 5
5016/5016T	STD	−5	−6	N/A	N/A
5026/5026T	STD	−5	−6	−30	N/A
5036/5036T	STD	N/A	N/A	N/A	−80**
5046/5046T	STD	N/A	N/A	N/A	N/A

*When Duty Cycle is not exactly 50%, it is 50% ± 10%.

**Output appears on f_R (pin 3) only. . . . Output frequency selection via R_A, R_B, R_C, R_D.

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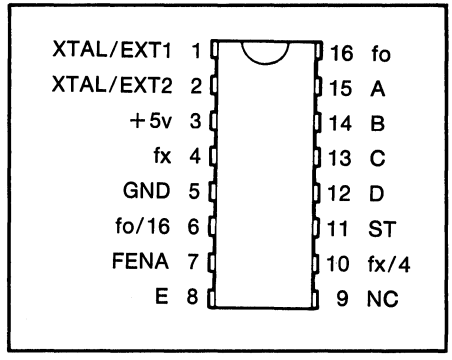
COM 8046
COM 8046T

Baud Rate Generator
Programmable Divider

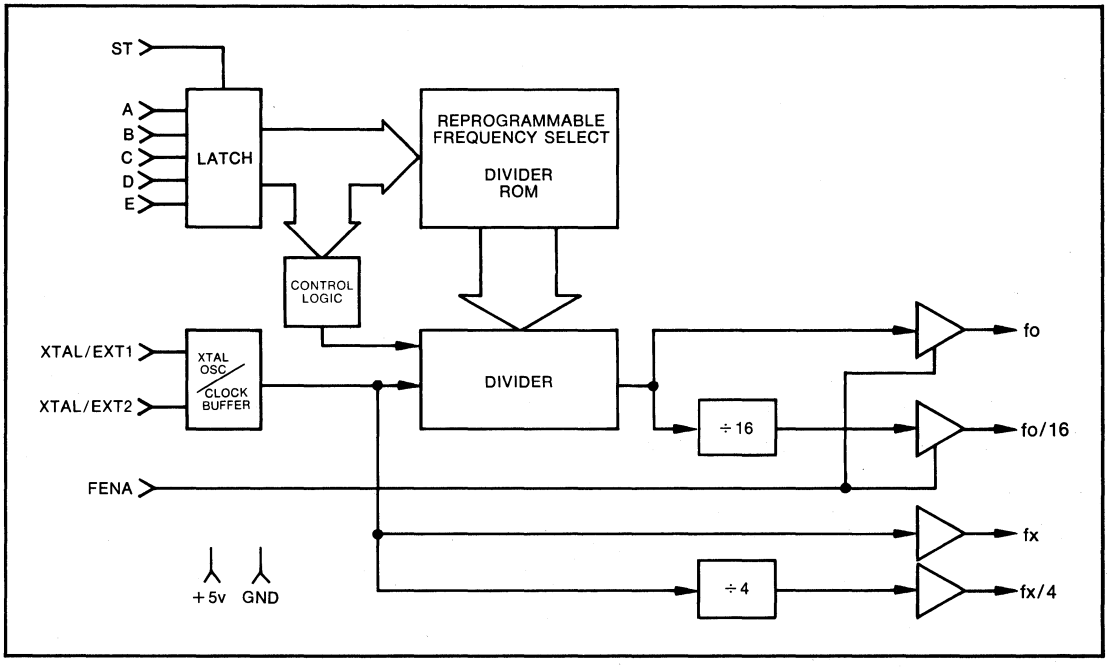
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 32 output frequencies
- ☐ 32 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatible
- ☐ 1X Clock via fo/16 output
- ☐ Crystal frequency output via fx and fx/4 outputs
- ☐ Output disable via FENA

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION VI

General Description

The Standard Microsystems COM 8046 is an enhanced version of the COM 5046 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8046 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 1X, 16X and 32X UART/USRT/ASTRO/USYNRT devices.

The COM 8046 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8046T. TTL outputs used to drive the COM 8046 or COM 8046T should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The reference frequency (fx) is used to provide two high frequency outputs: one at fx and the other at fx/4. The fx/4 output will drive one standard 7400 load, while the fx output will drive two 74LS loads.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency f_O. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period. The output of the divider is also divided internally by 16 and made available at the $f_O/16$ output pin. The $f_O/16$ output will drive one and the f_O output will drive two standard 7400 TTL loads. Both the f_O and $f_O/16$ outputs can be disabled by supplying a low logic level to the FENA input pin. Note that the FENA input has an internal pull-up which will cause the pin to rise to approximately V_{CC} if left unconnected.

The divisor ROM contains 32 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turn-around-time for ROM patterns.

The five divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the five divisor select bits; strobe activity is not required. This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current f_O half-cycle All five data inputs have pull-ups identical to that of the FENA input, while the strobe input has no pull-up.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4	f_X	f_X	Crystal/clock frequency reference output
5	GND	Ground	Ground
6	$f_O/16$	$f_O/16$	1X clock output
7	FENA	Enable	A low level at this input causes the f_O and $f_O/16$ outputs to be held high. An open or a high level at the FENA input enables the f_O and $f_O/16$ outputs.
8	E	E	Most significant divisor select data bit. An open at this input is equivalent to a logic high.
9	NC	NC	No connection
10	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
11	ST	Strobe	Divisor select data strobe. Data is sampled when this input is high, preserved when this input is low.
12-15	D,C,B,A	D,C,B,A	Divisor select data bits. A=LSB. An open circuit at these inputs is equivalent to a logic high.
16	f_O	f_O	16X clock output

For electrical characteristics, see page 199.

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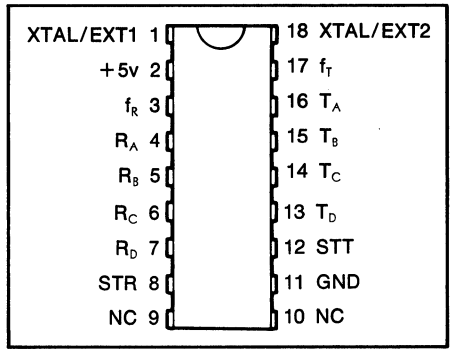
COM 8116
COM 8116T

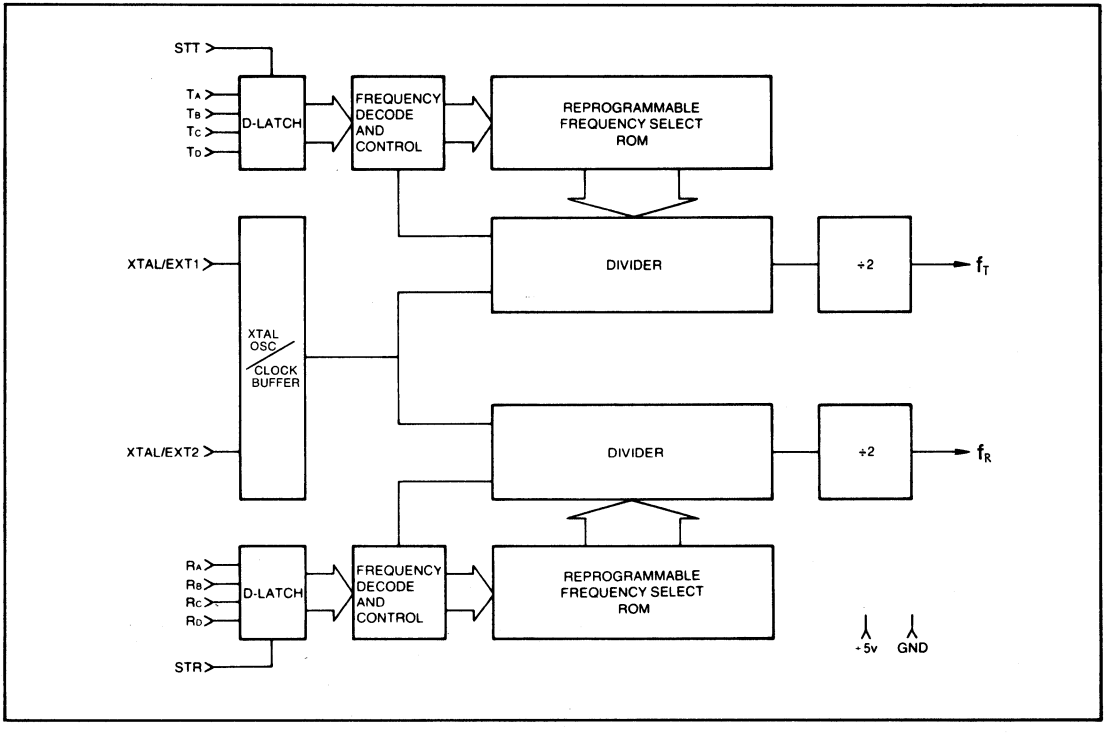
Dual Baud Rate Generator
Programmable Divider

FEATURES
- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5016

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION VI

General Description

The Standard Microsystem's COM 8116 is an enhanced version of the COM 5016 Dual Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8116 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8116 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 18. Parts suitable for use only with an external TTL reference are marked COM 8116T. TTL outputs used to drive the COM 8116 or COM 8116T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies f_T, f_R. The dividers are capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

Each of the two divisor ROMs contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology allowing up to 32 different divisors on custom parts. This process permits reduction of turn-around time for ROM patterns. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). The divisor select inputs have pull-up resistors; the strobe inputs do not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	NC	No Connection	
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

For electrical characteristics, see page 199.

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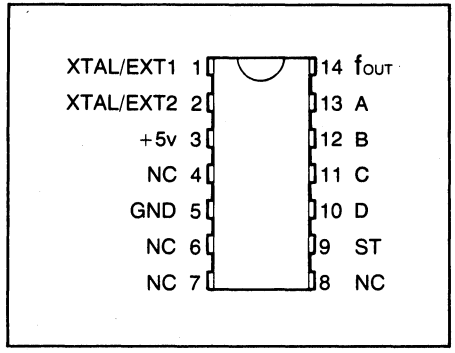
COM 8126
COM 8126T

Baud Rate Generator
Programmable Divider

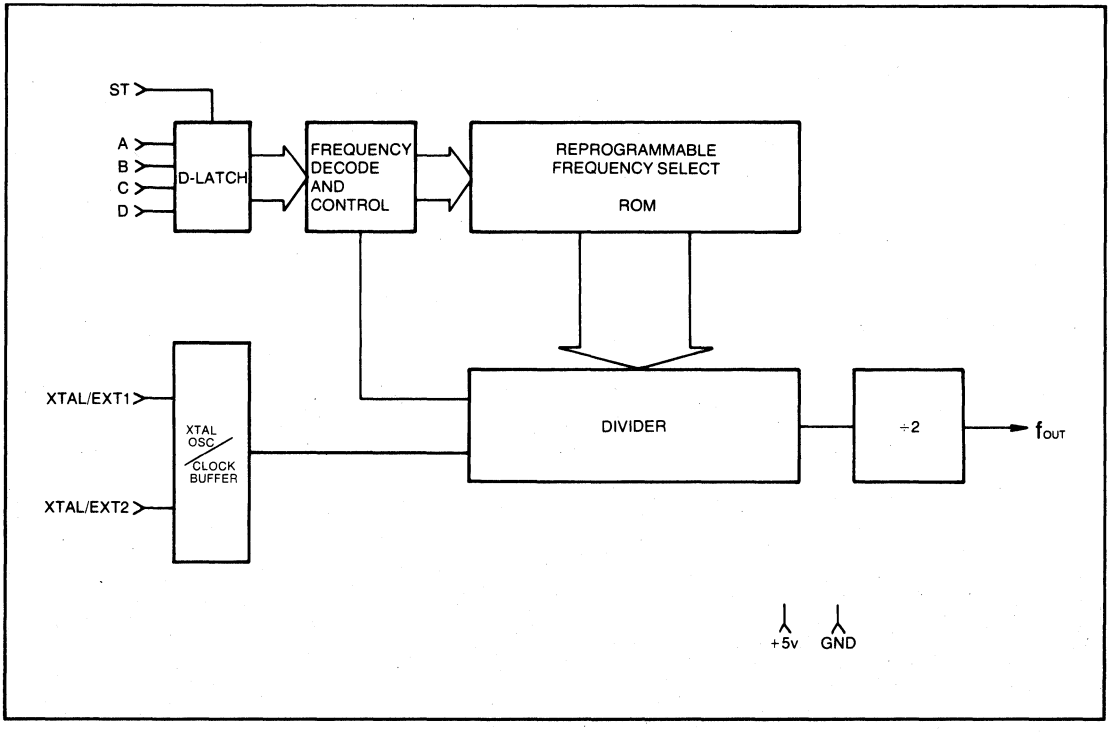
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5026

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION VI

General Description

The Standard Microsystem's COM 8126 is an enhanced version of the COM 5026 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8126 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8126 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8126T. TTL outputs used to drive the COM 8126 or COM 8126T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The divisor ROM contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turnaround time for ROM patterns. The four divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current f_{OUT} half-cycle. The divisor select inputs have pull-up resistors; the strobe input does not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4,6,7,8	NC	No Connection	
5	GND	Ground	Ground
9	ST	Strobe	A high level strobe loads the input data (A, B, C, D) into the input divisor select register. This input may be strobed or hard-wired to a high level.
10-13	D,C, B, A	Divisor Select Data Bits	The logic level on these inputs as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency selected by the divisor select data bits.

For electrical characteristics, see page 199.

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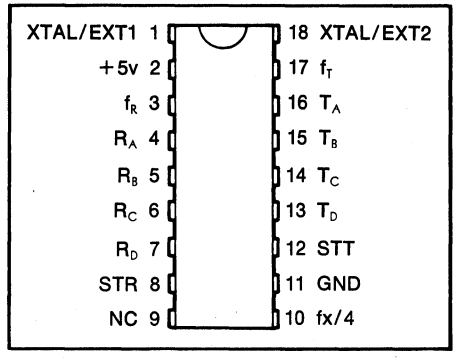
COM 8136
COM 8136T

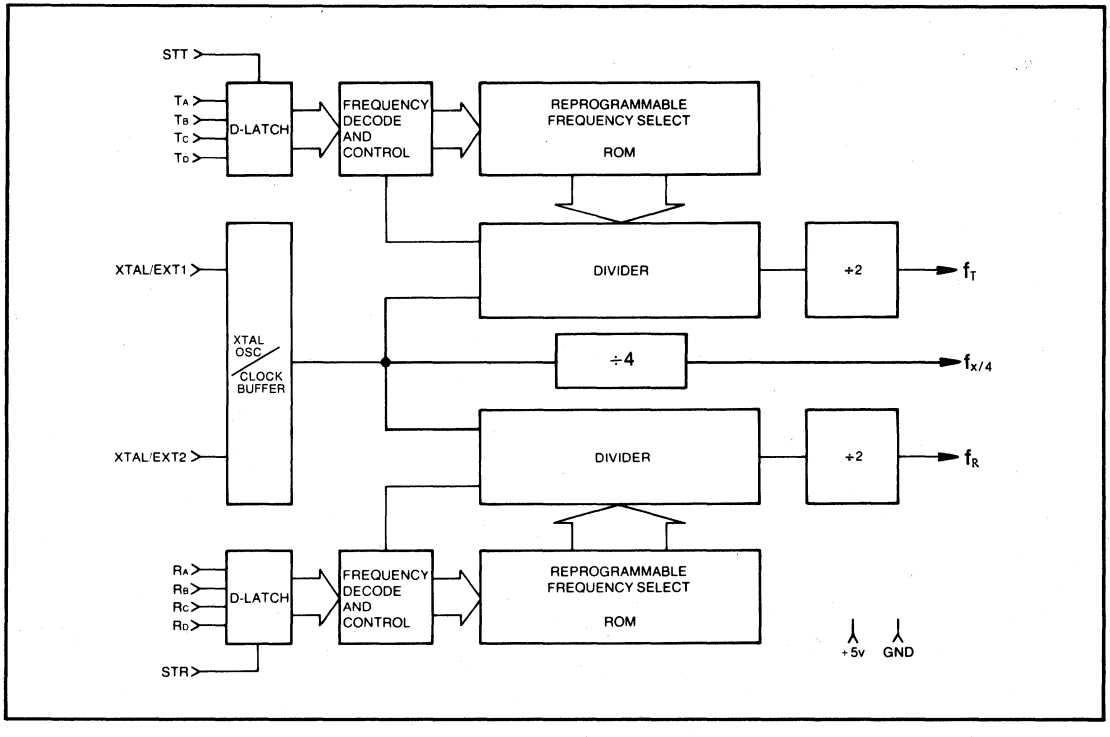
Dual Baud Rate Generator
Programmable Divider

FEATURES
- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ High frequency reference output
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5036

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION VI

General Description

The Standard Microsystem's COM 8136 is an enhanced version of the COM 5036 Dual Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8136 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8136 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 18. Parts suitable for use only with an external TTL reference are marked COM 8136T. TTL outputs used to drive the COM 8136 or COM 8136T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies f_T, f_R. The dividers are capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The reference frequency (fx) is used to provide a high frequency output at fx/4.

Each of the two divisor ROMs contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology allowing up to 32 different divisors on custom parts. This process permits reduction of turn-around time for ROM patterns. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). The divisor select inputs have pull-up resistors; the strobe inputs do not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	NC	No Connection	
10	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divider Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

For electrical characteristics, see page 199.

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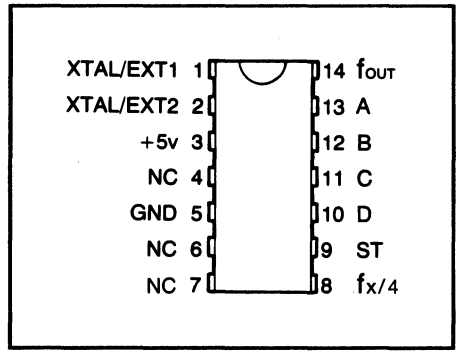
COM 8146
COM 8146T

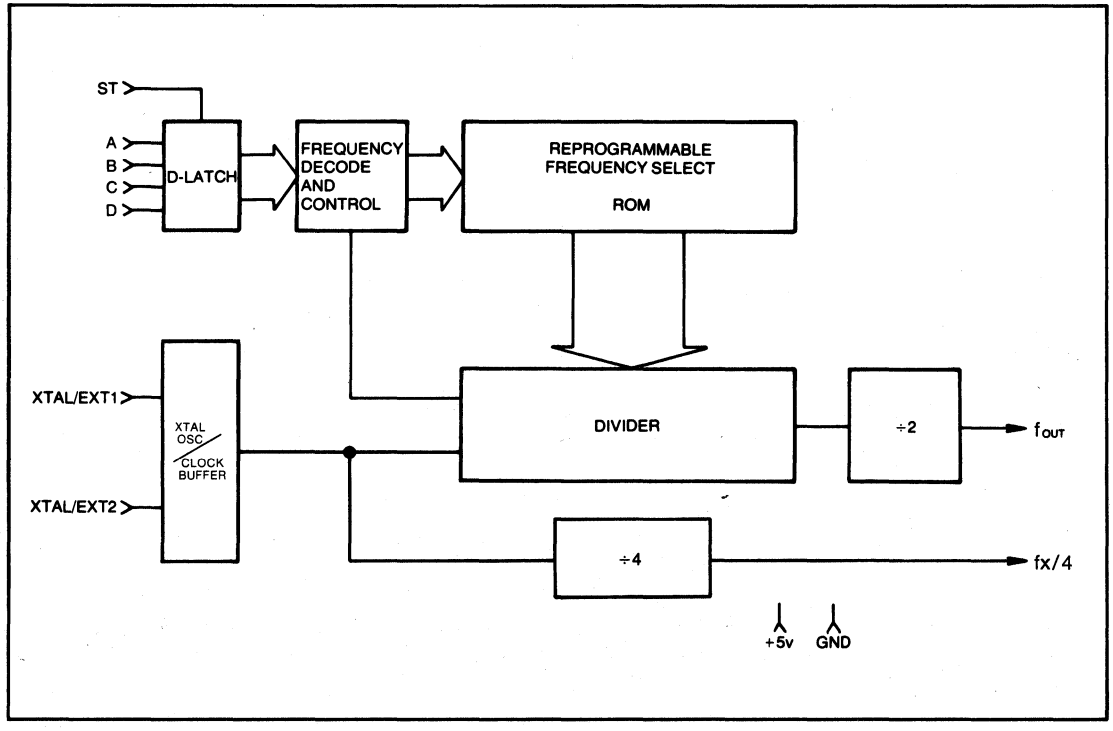
Baud Rate Generator
Programmable Divider

FEATURES
- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ High frequency reference output
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5046

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION VI

General Description

The Standard Microsystem's COM 8146 is an enhanced version of the COM 5046 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8146 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8146 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8146T. TTL outputs used to drive the COM 8146 or COM 8146T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The reference frequency (fx) is used to provide a high frequency output at fx/4.

The divisor ROM contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turn-around time for ROM patterns. The four divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current f_{OUT} half-cycle. The divisor select inputs have pull-up resistors; the strobe input does not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4,6,7	NC	No Connection	
5	GND	Ground	Ground
8	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
9	ST	Strobe	A high level strobe loads the input data (A, B, C, D) into the input divisor select register. This input may be strobed or hard-wired to a high level.
10-13	D,C,B,A	Divisor Select Data Bits	The logic level on these inputs as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency selected by the divisor select data bits.

For electrical characteristics, see page 199.

ELECTRICAL CHARACTERISTICS COM8046, COM8046T, COM8116, COM8116T, COM8126, COM8126T, COM8136, COM8136T, COM8146, COM8146T

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

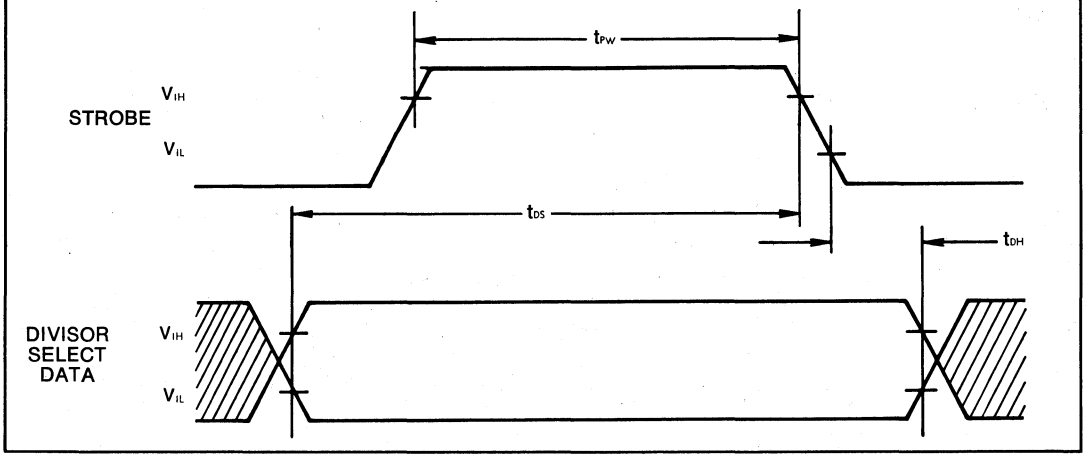
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

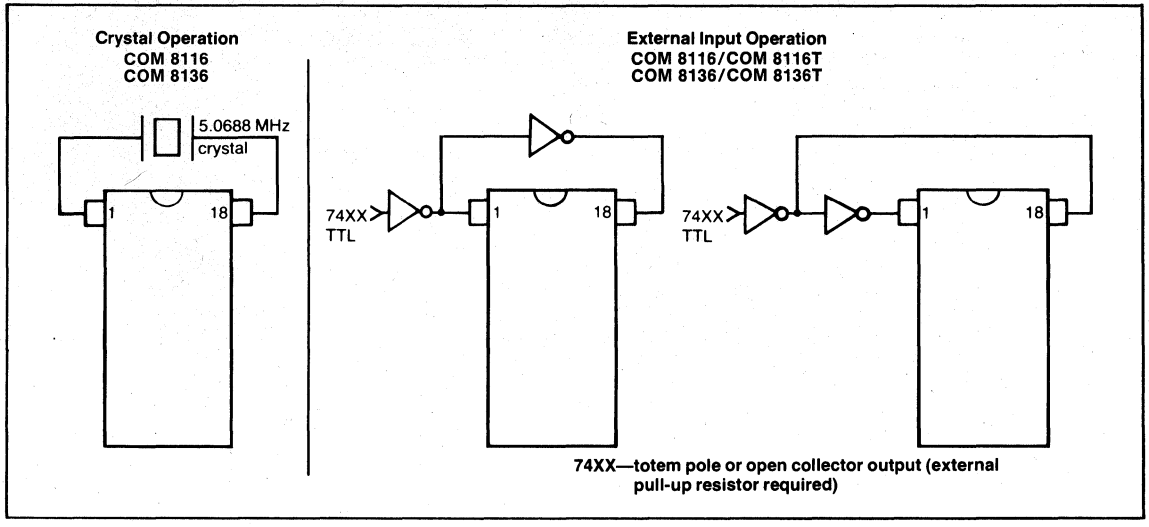
ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, unless otherwise noted)

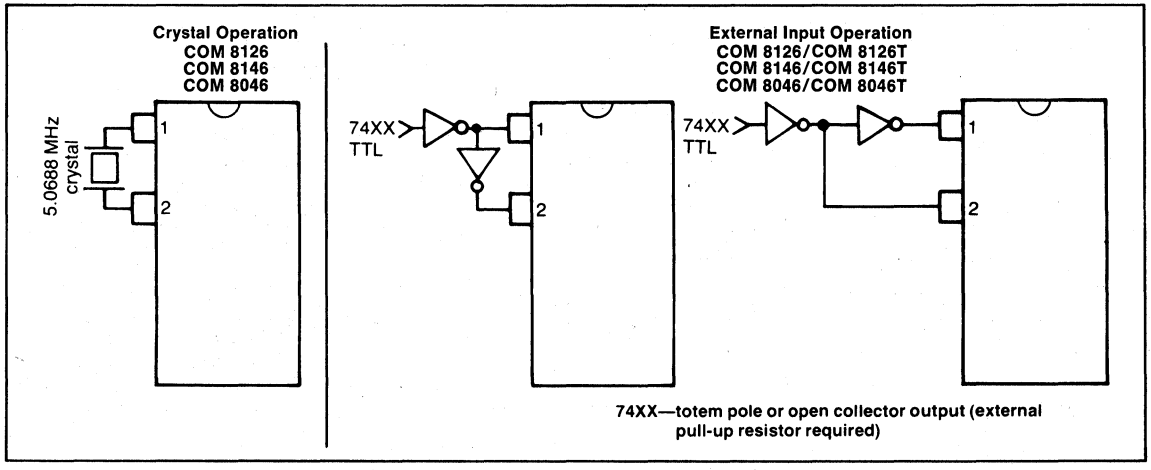
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	2.0			V	excluding XTAL inputs
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL}=1.6mA, for $f_X/4$, $f_O/16$
			0.4	V	I_{OL}=3.2mA, for f_O, f_R, f_T
			0.4	V	I_{OL}=0.8mA, for f_X
High-level, V_{OH}	3.5			V	I_{OH}=−100μA; for f_X, I_{OH}=−50μA
INPUT CURRENT					
Low-level, I_{IL}			-0.1	mA	V_{IN}=GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pF	V_{IN}=GND, excluding XTAL inputs
EXT INPUT LOAD		8	10		Series 7400 equivalent loads
POWER SUPPLY CURRENT					
I_{CC}			50	mA	
A.C. CHARACTERISTICS					T_A= +25°C
CLOCK FREQUENCY, f_{IN}	0.01		7.0	MHz	XTAL/EXT, 50% Duty Cycle ±5% COM 8046, COM 8126, COM 8146
	0.01		5.1	MHz	XTAL/EXT, 50% Duty Cycle ±5% COM 8116, COM 8136
STROBE PULSE WIDTH, t_{PW}	150		DC	ns	
INPUT SET-UP TIME					
t_{DS}	200			ns	
INPUT HOLD TIME					
t_{DH}	50			ns	
STROBE TO NEW FREQUENCY DELAY			3.5	μs	@ f_X=5.0 MHz

TIMING DIAGRAM



SECTION VI





For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

Crystal Specifications

User must specify termination (pin, wire, other)
Prefer: HC-18/U or HC-25/U
Frequency — 5.0688 MHz, AT cut
Temperature range 0°C to 70°C
Series resistance $<50\ \Omega$
Series Resonant
Overall tolerance ± .01%
or as required

Crystal manufacturers (Partial List)

Northern Engineering Laboratories
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

Bulova Frequency Control Products
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

CTS Knights Inc.
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

Crystek Crystals Corporation
1000 Crystal Drive
Fort Myers, Florida 33901
(813) 936-2109

COM 8046
COM 8046T

Table 2

REFERENCE FREQUENCY = 5.068800MHz

Divisor Select EDCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
00000	50.00	32X	1.60000	3168	50.00	1.600000	0.0000%
00001	75.00	32X	2.40000	2112	75.00	2.400000	0.0000%
00010	110.00	32X	3.52000	1440	110.00	3.520000	0.0000%
00011	134.50	32X	4.30400	1177	134.58	4.306542	0.0591%
00100	150.00	32X	4.80000	1056	150.00	4.800000	0.0000%
00101	200.00	32X	6.40000	792	200.00	6.400000	0.0000%
00110	300.00	32X	9.60000	528	300.00	9.600000	0.0000%
00111	600.00	32X	19.20000	264	600.00	19.200000	0.0000%
01000	1200.00	32X	38.40000	132	1200.00	38.400000	0.0000%
01001	1800.00	32X	57.60000	88	1800.00	57.600000	0.0000%
01010	2400.00	32X	76.80000	66	2400.00	76.800000	0.0000%
01011	3600.00	32X	115.20000	44	3600.00	115.200000	0.0000%
01100	4800.00	32X	153.60000	33	4800.00	153.600000	0.0000%
01101	7200.00	32X	230.40000	22	7200.00	230.400000	0.0000%
01110	9600.00	32X	307.20000	16	9900.00	316.800000	3.1250%
01111	19200.00	32X	614.40000	8	19800.00	633.600000	3.1250%
10000	50.00	16X	0.80000	6336	50.00	0.800000	0.0000%
10001	75.00	16X	1.20000	4224	75.00	1.200000	0.0000%
10010	110.00	16X	1.76000	2880	110.00	1.760000	0.0000%
10011	134.50	16X	2.15200	2355	134.52	2.152357	0.0166%
10100	150.00	16X	2.40000	2112	150.00	2.400000	0.0000%
10101	300.00	16X	4.80000	1056	300.00	4.800000	0.0000%
10110	600.00	16X	9.60000	528	600.00	9.600000	0.0000%
10111	1200.00	16X	19.20000	264	1200.00	19.200000	0.0000%
11000	1800.00	16X	28.80000	176	1800.00	28.800000	0.0000%
11001	2000.00	16X	32.00000	158	2005.06	32.081013	0.2532%
11010	2400.00	16X	38.40000	132	2400.00	38.400000	0.0000%
11011	3600.00	16X	57.60000	88	3600.00	57.600000	0.0000%
11100	4800.00	16X	76.80000	66	4800.00	76.800000	0.0000%
11101	7200.00	16X	115.20000	44	7200.00	115.200000	0.0000%
11110	9600.00	16X	153.60000	33	9600.00	153.600000	0.0000%
11111	19200.00	16X	307.20000	16	19800.00	316.800000	3.1250%

COM 8116
COM 8116T
COM 8126
COM 8126T

COM 8136
COM 8136T
COM 8146
COM 8146T

Table 1

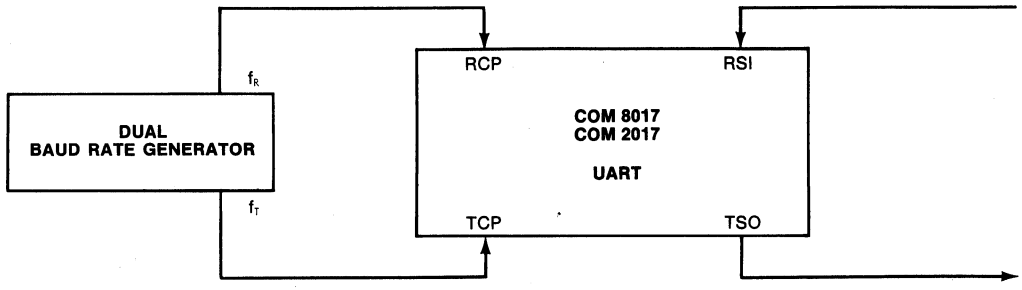
REFERENCE FREQUENCY = 5.068800MHZ
(STANDARD PART)

Divisior Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	16X	0.80000	6336	50.00	0.800000	0.0000%
0001	75.00	16X	1.20000	4224	75.00	1.200000	0.0000%
0010	110.00	16X	1.76000	2880	110.00	1.760000	0.0000%
0011	134.50	16X	2.15200	2355	134.52	2.152357	0.0166%
0100	150.00	16X	2.40000	2112	150.00	2.400000	0.0000%
0101	300.00	16X	4.80000	1056	300.00	4.800000	0.0000%
0110	600.00	16X	9.60000	528	600.00	9.600000	0.0000%
0111	1200.00	16X	19.20000	264	1200.00	19.200000	0.0000%
1000	1800.00	16X	28.80000	176	1800.00	28.800000	0.0000%
1001	2000.00	16X	32.00000	158	2005.06	32.081013	0.2532%
1010	2400.00	16X	38.40000	132	2400.00	38.400000	0.0000%
1011	3600.00	16X	57.60000	88	3600.00	57.600000	0.0000%
1100	4800.00	16X	76.80000	66	4800.00	76.800000	0.0000%
1101	7200.00	16X	115.20000	44	7200.00	115.200000	0.0000%
1110	9600.00	16X	153.60000	33	9600.00	153.600000	0.0000%
1111	19200.00	16X	307.20000	16	19800.00	316.800000	3.1250%

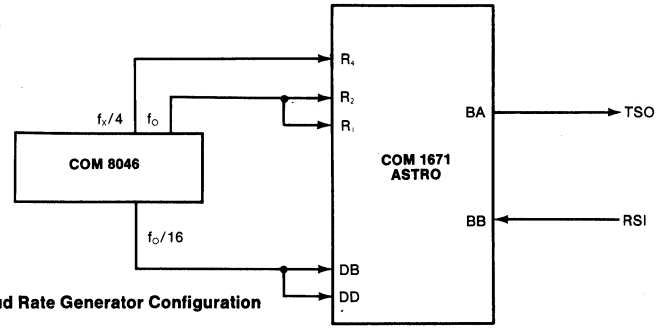
Table 2

REFERENCE FREQUENCY = 4.915200MHz
(COM81__ __ –5)

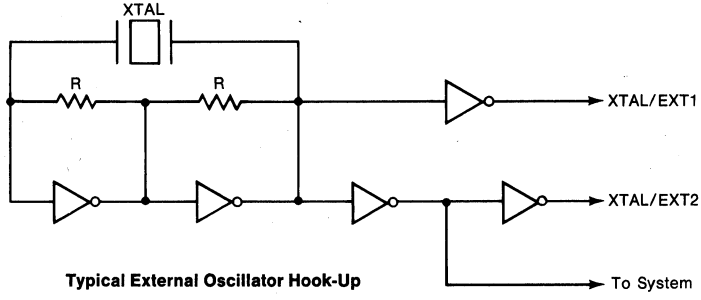
Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	16X	0.80000	6144	50.00	0.800000	0.0000%
0001	75.00	16X	1.20000	4096	75.00	1.200000	0.0000%
0010	110.00	16X	1.76000	2793	109.93	1.758983	0.0100%
0011	134.50	16X	2.15200	2284	134.50	2.152000	0.0000%
0100	150.00	16X	2.40000	2048	150.00	2.400000	0.0000%
0101	300.00	16X	4.80000	1024	300.00	4.800000	0.0000%
0110	600.00	16X	9.60000	512	600.00	9.600000	0.0000%
0111	1200.00	16X	19.20000	256	1200.00	19.200000	0.0000%
1000	1800.00	16X	28.80000	171	1796.49	28.743859	0.1949%
1001	2000.00	16X	32.00000	154	1994.81	31.916883	0.2597%
1010	2400.00	16X	38.40000	128	2400.00	32.000000	0.0000%
1011	3600.00	16X	57.60000	85	3614.11	57.825882	0.3921%
1100	4800.00	16X	76.80000	64	4800.00	76.800000	0.0000%
1101	7200.00	16X	115.20000	43	7144.19	114.306976	0.7751%
1110	9600.00	16X	153.60000	32	9600.00	153.600000	0.0000%
1111	19200.00	16X	307.20000	16	19200.00	307.200000	0.0000%



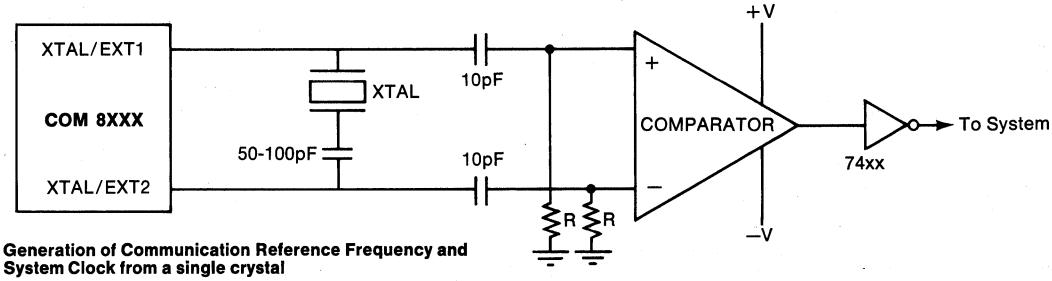
Typical UART—Dual Baud Rate Generator Configuration
Full Duplex—Split Speed



Typical ASTRO—Baud Rate Generator Configuration



Typical External Oscillator Hook-Up



Generation of Communication Reference Frequency and System Clock from a single crystal

SECTION VI

Keyboard Encoder

Part Number	No. of Keys	Modes	Features	Standard Fonts Suffix	Standard Fonts Description	Power Supplies	Package	Page
KR-2376 XX[3]	88	3	2 Key Rollover	-ST	ASCII	+5, −12	40 DIP	207-210
KR-3600 XX[3]	90	4	2 Key or N Key Rollover	-ST -STD -PRO	ASCII ASCII Binary Sequential	+5, −12	40 DIP	211-218

[3] May be custom mask programmed

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11787
(516) 273-3100 · TWX-510-227-8898

We keep ahead of our competition so you can keep ahead of yours.

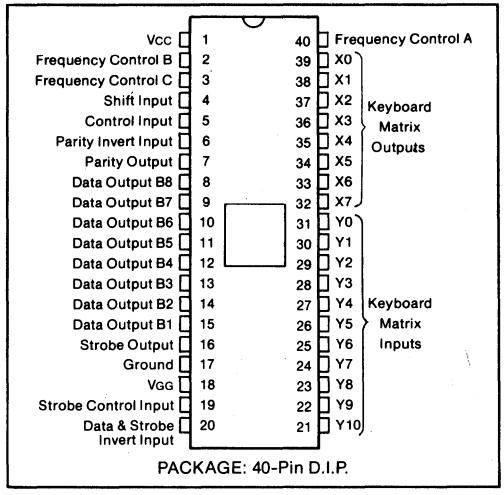
KR2376-XX

Keyboard Encoder Read Only Memory

FEATURES

- ☐ Outputs directly compatible with TTL/DTL or MOS logic arrays.
- ☐ External control provided for output polarity selection.
- ☐ External control provided for selection of odd or even parity.
- ☐ Two key roll-over operation.
- ☐ N-key lockout.
- ☐ Programmable coding with a single mask change.
- ☐ Self-contained oscillator circuit.
- ☐ Externally controlled delay network provided to eliminate the effect of contact bounce.
- ☐ One integrated circuit required for complete keyboard assembly.
- ☐ Static charge protection on all input and output terminals.
- ☐ Entire circuit protected by a layer of glass passivation.

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

GENERAL DESCRIPTION

The SMC KR2376-XX is a 2376-bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

The KR2376-XX is fabricated with low threshold, P-channel technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip, available in a 40 pin dual-in-line package.

TYPICAL CONNECTION OF KR2376-XX

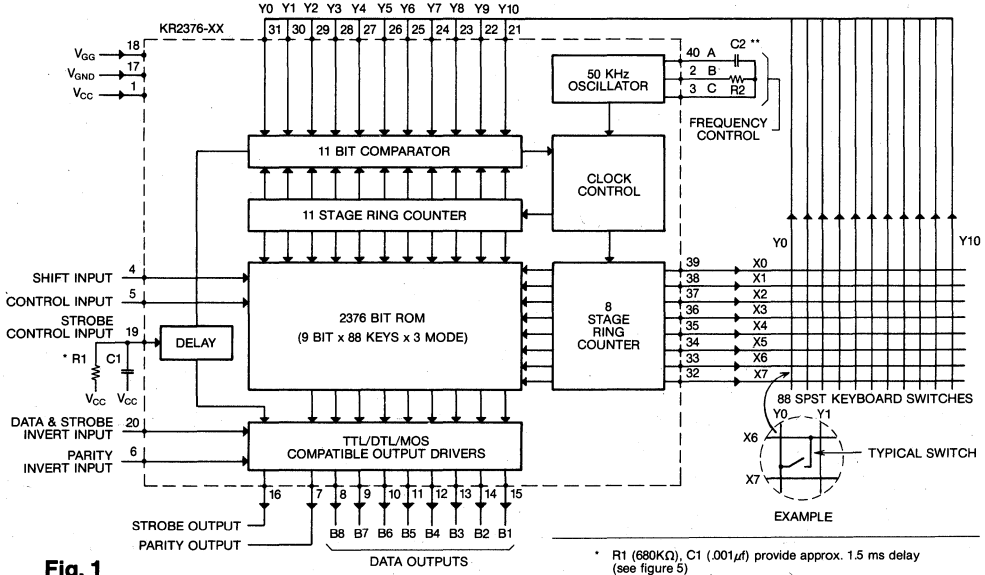


Fig. 1

* R1 (680KΩ), C1 (.001μf) provide approx. 1.5 ms delay (see figure 5)

** R2 (100KΩ), C2 (50pf) provide 50KHz clock frequency (see figure 6)

SECTION VII

MAXIMUM GUARANTEED RATINGS†

Operating Temperature Range ..... 0° C to +70° C
Storage Temperature Range ..... −65° C to +150° C
GND and V_{GG}, with respect to V_{CC} ..... −20V to +0.3V
Logic Input Voltages, with respect to V_{CC} ..... −20V to +0.3V

† Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0° C to +70° C, V_{CC} = +5V ±0.5V, V_{GG} = −12V ±1.0V, unless otherwise noted)

Characteristics	Min	Typ	Max	Unit	Conditions
CLOCK	20	50	100	KHz	see fig.1 footnote (**) for typical R-C values
DATA INPUT					
Logic "0" Level			+0.8	V	
Logic "1" Level	V_{CC}-1.5			V	
Input Capacitance			10	pf	
INPUT CURRENT					
*Control, Shift & Y0 thru Y10	10	100	140	μA	V_{IN} = +5.0V
*Control, Shift & Y0 thru Y10	5	30	50	μA	V_{IN} = Ground
Data Invert, Parity Invert		.01	1	μA	V_{IN} = −5.0V to +5.0V
DATA OUTPUT & X OUTPUT					
Logic "0" Level			+0.4	V	I_{OL} = 1.6mA (see fig. 7)
Logic "1" Level	V_{CC}-1.0			V	I_{OH} = 100 μA
POWER CONSUMPTION		140	200	mW	Nom. Power Supp. Voltages (see fig. 8)
SWITCH CHARACTERISTICS					
Minimum Switch Closure	see timing diagram-fig. 2				
Contact Closure Resistance between X1 and Y1			300	Ohm	
Contact Open Resistance between X1 and Y1	1×10^7			Ohm	

*Inputs with Internal Resistor to V_{GG}

DESCRIPTION OF OPERATION

The KR2376-XX contains (see Fig. 1), a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9-bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and to the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

SPECIAL PATTERNS

Since the selected coding of each key is defined during the manufacture of the chip, the coding can be changed to fit any particular application of the keyboard. Up to 264 codes of up to 8 bits (plus one parity bit) can be programmed into the KR2376-XX ROM covering most popular codes such as ASC11, EBCD1C, Selectric, etc., as well as many specialized codes. The ASC11 code is available as a standard pattern. For special patterns, use Fig. 9.

TIMING DIAGRAM

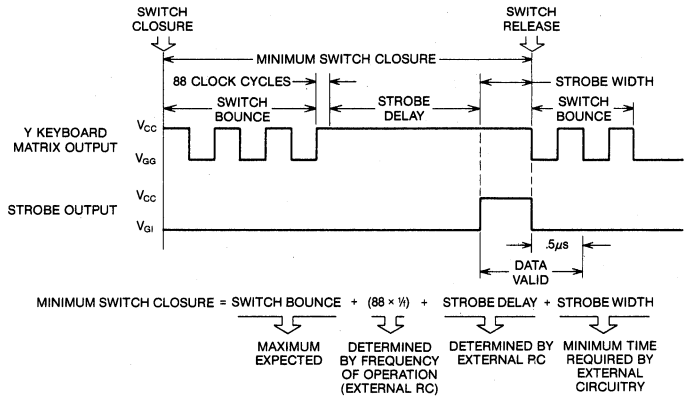
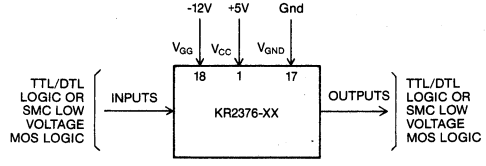


Fig. 2

POWER SUPPLY CONNECTIONS FOR TTL/DTL OPERATION



POWER SUPPLY CONNECTIONS FOR MOS OPERATION

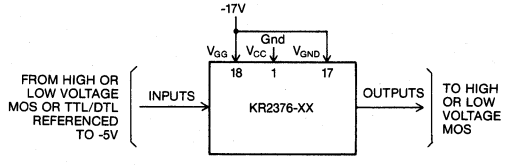
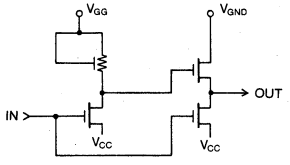


Fig. 3

OUTPUT DRIVER & "X" OUTPUT STAGE TO KEYBOARD



"Y" INPUT STAGE FROM KEYBOARD

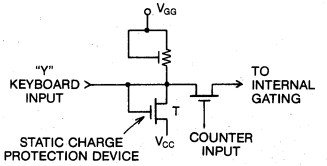


Fig. 4

STROBE DELAY VS. C_1

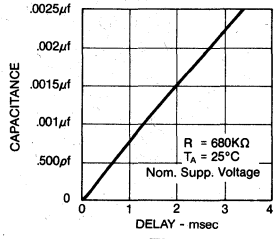


Fig. 5

OSCILLATOR FREQUENCY VS. C_2

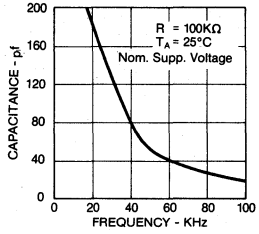


Fig. 6

TYP. OUTPUT ON RESISTANCE VS. GATE BIAS VOLTAGE

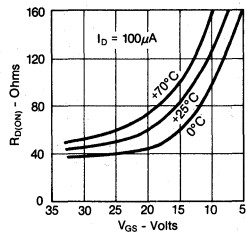


Fig. 7

TYP. POWER CONSUMPTION VS. TEMPERATURE

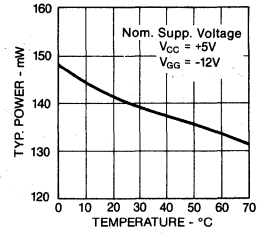


Fig. 8

CODE ASSIGNMENT CHART
KR2376-ST
8 Bit ASCII, odd parity

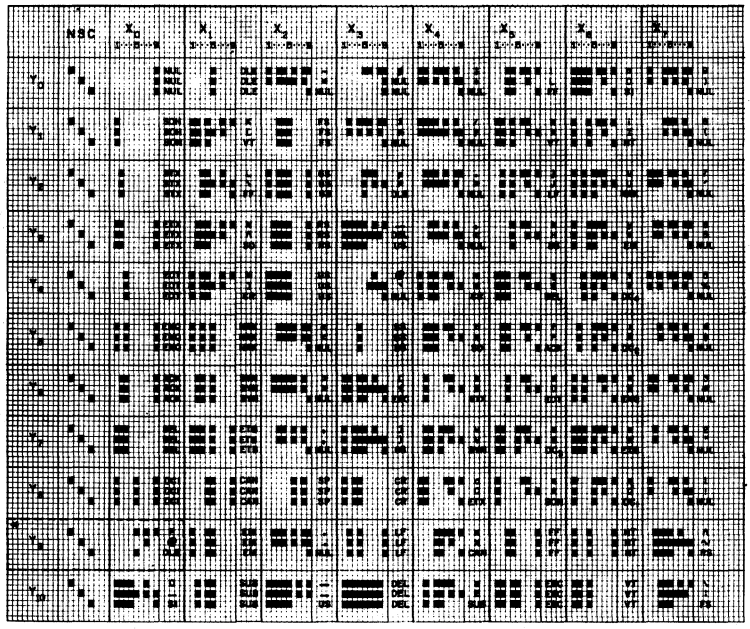
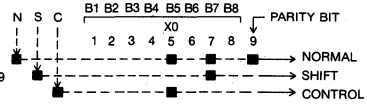


Fig. 9



(Code representative of key depression at location X0-Y9 and proper mode selection)

N = Normal Mode
S = Shift Mode
C = Control Mode
■ = Output Logic "1" (see data B1-B8)
Logic "1" = +5.0V
Logic "0" = Ground

DATA (B1-B8) INVERT TRUTH TABLE

DATA & STROBE INVERT INPUT (Pin 20)	CODE-ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA & STROBE INVERT INPUT (Pin 20)	INTERNAL STROBE	STROBE OUTPUT (Pin 16)
1	1	0
0	0	0
1	0	1
0	1	1

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (Pin 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (Pin 7)
1	1	0
0	1	1
1	0	1
0	0	0

MODE SELECTION

$\overline{S}$ $\overline{C}$ = N
S $\overline{C}$ = S
$\overline{S}$ C = C
S C = INVALID (SPURIOUS DATA)

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11787
(516) 273-3100 · TWX-510-227-8898

We keep ahead of our competition so you can keep ahead of yours.

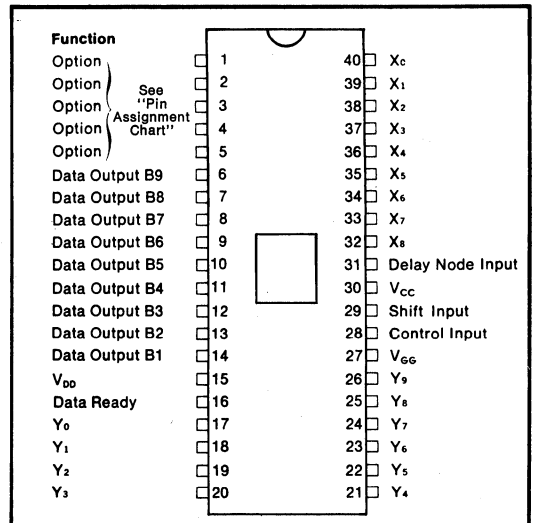
KR3600-XX
KR3600-ST
KR3600-STD
KR3600-PRO

Keyboard Encoder Read Only Memory

FEATURES

- Data output directly compatible with TTL
- N Key rollover or lockout operation
- Quad mode
- Lockout/rollover selection externally selected as option
- On chip-master/slave oscillator
- All 10 output bits available
- Fully buffered data outputs
- Output enable provided as option
- Data compliment control provided as option
- Pulse or level data ready output signal provided as an option
- Any key down output provided as an option
- Contact bounce circuit provided to eliminate contact bounce
- Static charge protection on all input/outputs
- Pin for Pin replacement for GI AY-5-3600

PIN CONFIGURATION



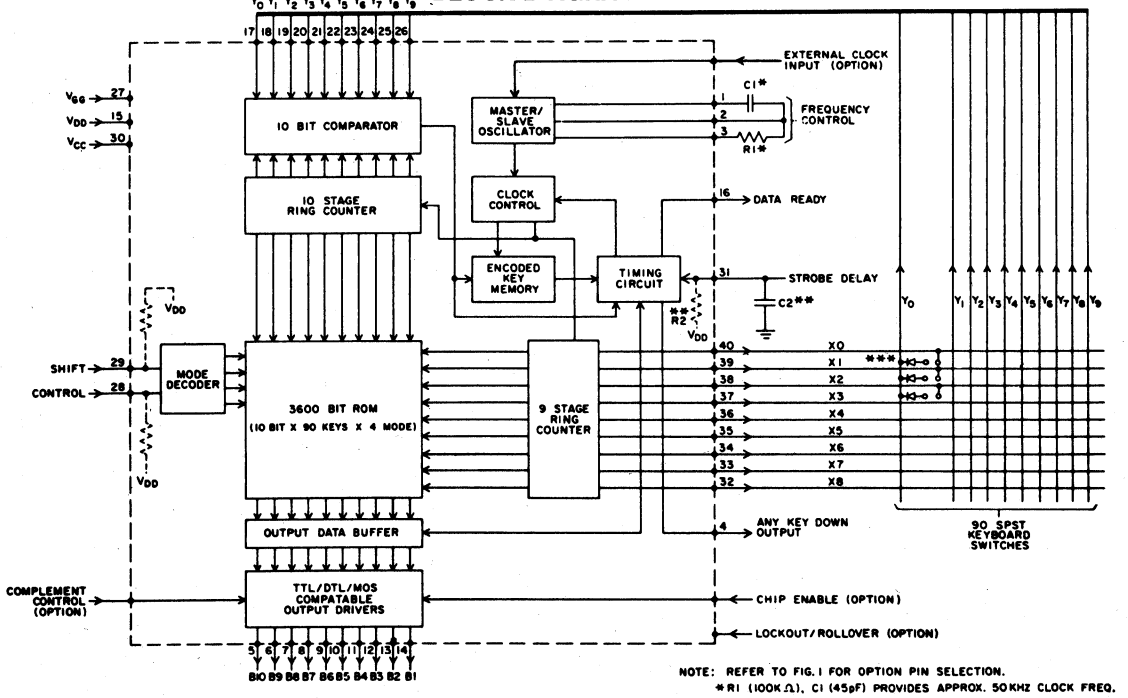
PACKAGE: 40-Pin D.I.P.

GENERAL DESCRIPTION

The SMC Microsystems KR3600-XX is a Keyboard Encoder containing a 3600 bit read only memory and all the logic necessary to encode single pole single throw keyboard closures into a 10 bit code.

The KR3600-XX is fabricated with a low voltage p channel technology and contains the equivalent of 5000 transistors on a monolithic chip in a 40 lead dip ceramic package.

BLOCK DIAGRAM



NOTE: REFER TO FIG. 1 FOR OPTION PIN SELECTION.
*R1 (100K Ω), C1 (45pF) PROVIDES APPROX. 50KHZ CLOCK FREQ.
**C2 (300nS DELAY/ CPF) R2 SUPPLIED INTERNALLY.
***DIODES NECESSARY FOR COMPLETE nKEY ROLLOVER OPERATION.

SECTION VII

DESCRIPTION OF OPERATION

The KR3600 contains a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby conditions, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y_0-Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER — When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT — When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

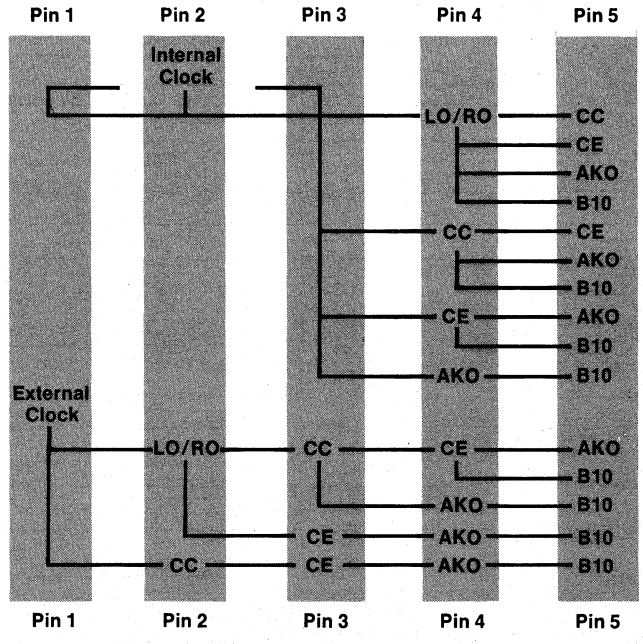
SPECIAL PATTERNS — Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the KR3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes.

CUSTOM CODING INFORMATION

The custom coding information for SMC's 3600 Bit Keyboard Encoder ROM should be transmitted to SMC. The Truth Table should be completed on the format supplied.

LEGEND

CC = Complement Control
AKO = Any Key Down Output
B10 = B10 (Data) Output
LO/RO = Lockout/Rollover
CE = Chip Enable
Internal Clock = Self Contained Oscillator
External Clock = External Frequency Source



OPTION SELECTION/PIN ASSIGNMENT

FIGURE 1

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, V_{CC}	+0.3 V
Negative Voltage on any Pin, V_{CC}	−25 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC} = +5V ±5%, V_{GG} = −12V ±1.0V, V_{DD} = GND, unless otherwise noted)

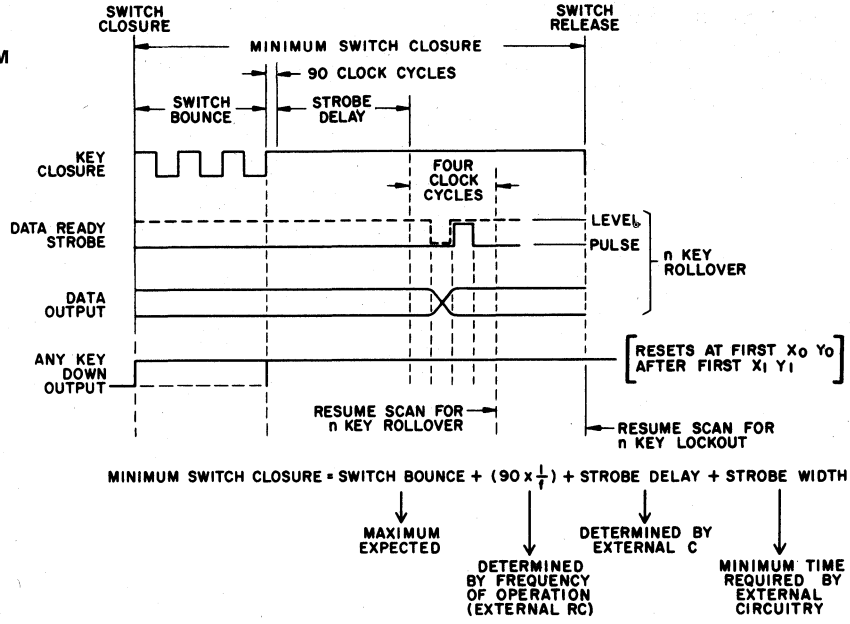
Characteristics	Min	Typ**	Max	Units	Conditions
Clock Frequency	10	50	100	KHz	See Block diagram footnote* for typical R-C values
External Clock Width	7	—	—	μs	
Data & Clock Input (Shift, Control, Compliment Control, Lockout/Rollover, Chip Enable & External Clock)					
Logic "0" Level	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{CC}−1.5	—	V_{CC}+0.3	V	
Shift & Control Input Current	75	150	220	μA	V_{IN} = +5V
X Output (X_0-X_8)					
Logic "1" Output Current	40	250	500	μA	V_{OUT} = V_{CC} (See Note 2)
	600	1300	4000	μA	V_{OUT} = V_{CC}−1.3V
	900	2000	6500	μA	V_{OUT} = V_{CC}−2.0V
	1500	2000	14,000	μA	V_{OUT} = V_{CC}−5V
	3000	10,000	23,000	μA	V_{OUT} = V_{CC}−10V
Logic "0" Output Current	8	30	60	μA	V_{OUT} = V_{CC}
	6	25	50	μA	V_{OUT} = V_{CC}−1.3V
	5	20	45	μA	V_{OUT} = V_{CC}−2.0V
	2	10	30	μA	V_{OUT} = V_{CC}−5V
	—	0.5	5	μA	V_{OUT} = V_{CC}−10V
Y Input (Y_0-Y_9)					
Trip Level	V_{CC}−5	V_{CC}−3	V_{CC}−2	V	Y Input Going Positive (See Note 2)
Hysteresis	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	18	100	170	μA	V_{IN} = V_{CC}
	14	80	150	μA	V_{IN} = V_{CC}−1.3V
	13	50	130	μA	V_{IN} = V_{CC}−2.0V
	5	40	110	μA	V_{IN} = V_{CC}−4.0V
Unselected Y Input Current	9	40	80	μA	V_{IN} = V_{CC}
	7	30	70	μA	V_{IN} = V_{CC}−1.3V
	6	25	60	μA	V_{IN} = V_{CC}−2.0V
	3	15	40	μA	V_{IN} = V_{CC}−5V
	—	0.5	20	μA	V_{IN} = V_{CC}−10V
Input Capacitance	—	3	10	pF	at 0V (All Inputs)
Switch Characteristics					
Minimum Switch Closure	—	—	—	—	See Timing Diagram
Contact Closure Resistance	—	—	300	Ω	Z_{CC}
	1 x 10^7	—	—	Ω	Z_{CO}
Strobe Delay					
Trip Level (Pin 31)	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)	−3	−5	−9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready					
Logic "0"	—	—	0.4	V	I_{OL} = 1.6m A
Logic "1"	V_{CC}−1	—	—	V	I_{OH} = 1.0m A
	V_{CC}−2	—	—	V	I_{OH} = 2.2m A
Power					
I_{CC}	—	12	22	mA	V_{CC} = +5V
I_{GG}	—	12	22	mA	V_{GG} = −12V

**Typical values are at +25°C and nominal voltages.

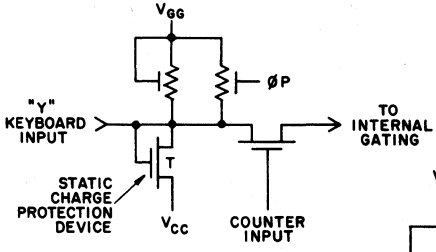
NOTE
1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

SECTION VII

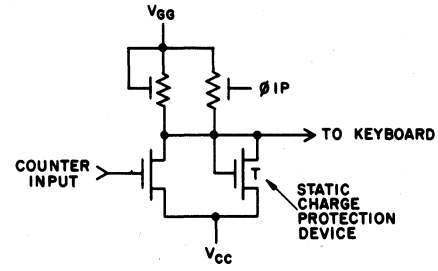
TIMING DIAGRAM



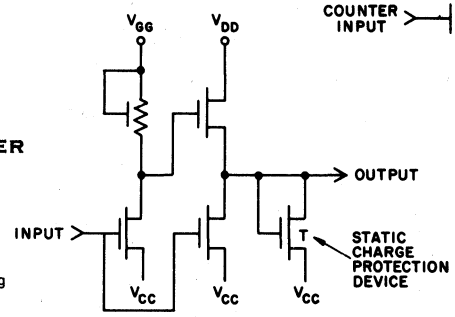
"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

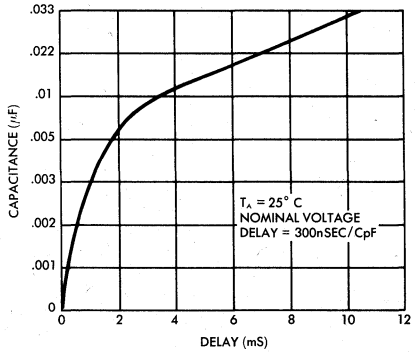


OUTPUT DRIVER

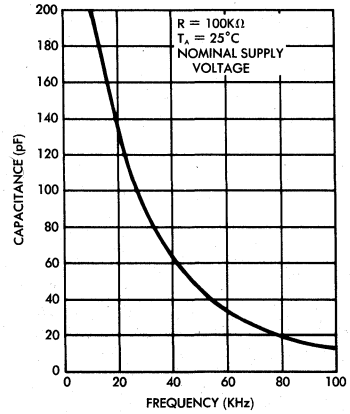


NOTE: Output driver capable of driving one TTL load with no external resistor. Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{GG}

STROBE DELAY vs. C_2



OSCILLATOR FREQUENCY vs. C_1



KR3600-STD

XY	Normal B-12345678910	Shift B-12345678910	Control B-12345678910	Shift Control B-12345678910
00	1 1000111001	< 0011111001	1 1000111011	SUB 0101100001
01	q 1000110101	Q 1000100101	q 1000111111	DLE 0000100001
02	a 1000010101	A 1000000101	a 1000011111	@ 0000000101
03	z 0101110101	Z 0101100101	z 0101111111	P 0000100101
04	HT 1001000001	HT 1001000001	HT 1001000001	I 1001000101
05	H 0001000101	H 0001000101	H 0001000101	H 0001000111
06	+ 1101011001	+ 1101011001	+ 1101011001	+ 1101011111
07	SO 0111001001	> 0111111001	SO 0111000001	SO 0111000011
08	p 0000110101	@ 0000000101	NUL 0000000001	NUL 0000000001
09	1 1000111001	! 1000011001	SOH 1000000001	SOH 1000000001
10	2 0100111001	@ 0000000101	2 0100111011	ETB 1110100001
11	w 1110110101	W 1110100101	w 1110111111	^ 0011100101
12	s 1100110101	S 1100100101	s 1100111111	A 1000000101
13	x 0001110101	X 0001100101	x 0001111111	Q 1000100101
14	RS 0111100001	RS 0111100001	RS 0111100001	FS 0011100001
15	% 1010011001	% 1010011001	% 1010011001	% 1010011011
16	m 1011010101	] 1011100101	CR 1011000001	CR 1011000001
17	SI 1111000001	SI 1111000001	SI 1111000001	SI 1111000011
18	n 0111010101	^ 0111100101	SO 0111000001	SO 0111000001
19	2 0100111001	" 0100011001	STX 0100000001	STX 0100000001
20	3 1100111001	# 1100011001	3 1100111011	NAK 1010100001
21	e 1010010101	E 1010000101	e 1010011111	DC3 1100100001
22	d 0010010101	D 0010000101	d 0010011111	B 0100000101
23	c 1100010101	C 1100000101	c 1100011111	R 0100100101
24	— 1111100100	— 1111100100	— 1111100100	^ 0111100100
25	$ 0010011001	$ 0010011001	$ 0010011001	$ 0010011011
26	L 0011000101	L 0011000101	L 0011000101	L 0011000111
27	US 1111100001	US 1111100001	US 1111100001	US 1111100011
28	6 0110111001	& 0110011001	ACK 0110000001	ACK 0110000001
29	k 1101010101	[1101100101	DEL 1111111101	DEL 1111111101
30	4 0010111001	$ 0010011001	4 0010111011	DC4 0010100001
31	r 0100110101	R 0100100101	r 0100111111	ENQ 1010000001
32	f 0110010101	F 0110000101	f 0110011111	C 1100000101
33	SP 0000011000	SP 0000011000	SP 0000011000	SP 0000011000
34	CAN 0001101000	(0001011000	CAN 0001100000	BS 0001000000
35	CR 1011000001	CR 1011000001	CR 1011000001	M 1011000101
36	[1101111101	[1101111101	[1101111111	K 1101000101
37	VT 1101000000	VT 1101000000	VT 1101000000	VT 1101000010
38	7 1110111001	' 1110011001	BEL 1110000001	BEL 1110000001
39	" 0100011001	" 0100011001	" 0100011001	" 0100011011
40	5 1010111001	% 1010011001	5 1010111011	STX 0100000001
41	t 0010110101	T 0010100101	t 0010111111	EOT 0010000001
42	g 1110010101	g 1110000101	G 1110011111	D 0010000101
43	v 0110110101	V 0110100101	v 0110111111	S 1100100101
44	ETX 1100000001	ETX 1100000001	ETX 1100000001	ETX 1100000001
45	] 1011111101	] 1011111101	] 1011111111	N 0111000101
46	? 1111111001	? 1111111001	? 1111111011	[1101100101
47	— 1011011001	— 1011111001	— 1011011001	— 1011011011
48	) 1001011001	) 1001011001	) 1001011001	) 1001011011
49	SP 0000011001	SP 0000011001	SP 0000011001	SP 0000011011
50	6 0110111001	> 0111111001	6 0110111011	SOH 1000000001
51	y 1001110101	Y 1001100101	y 1001111111	DC1 1000100001
52	h 0001010101	H 0001000101	h 0001011111	E 1010000101
53	b 0100010101	B 0100000101	b 0100011111	T 0010100101
54	: 0101111001	* 0101011001	: 0101111011	SYN 0110100001
55	> 0111111001	> 0111111001	> 0111111011	Z 0101100101
56	; 1101111001	+ 1101011001	; 1101111011	Y 1001100101
57	NUL 0000000001	NUL 0000000001	NUL 0000000001	NUL 0000000001
58	* 0101011001	* 0101011001	* 0101011001	* 0101011011
59	! 1000011001	! 1000011001	! 1000011001	! 1000011011
60	7 1110111001	& 0110011001	7 1110111011	ETX 1100000001
61	u 1010110101	U 1010100101	u 1010111111	BEL 1110000001
62	j 0101010101	J 0101000101	j 0101011111	F 0110000101
63	n 0111010101	N 0111000101	n 0111011111	U 1010100101
64	= 1011111000	= 1011111000	= 1011111010	~ 0111111100
65	< 0011111001	< 0011111001	< 0011111011	W 1110100101
66	p 0000110101	P 0000100101	p 0000111111	J 0101000101
67	0 0000111001	) 1001011001	0 0000111011	DC2 0100100001
68	& 0110011001	& 0110011001	& 0110011001	& 0110011011
69	# 1100011001	# 1100011001	# 1100011001	# 1100011011
70	8 0001111001	* 0101011001	8 0001111011	ESC 1101100001
71	i 1001010101	I 1001000101	i 1001011111	ACK 0110000001
72	k 1101010101	K 1101000101	k 1101011111	G 1110000101
73	m 1011010101	M 1011000101	m 1011011111	V 0110100101
74	/ 1111011001	? 1111111001	/ 1111011001	' 1110011001
75	' 1110011001	" 0100011001	' 1110011001	" 0100011001
76	LF 0101000000	LF 0101000000	LF 0101000000	GS 1011100000
77	= 1011111001	+ 1101011001	= 1011111001	+ 1101011001
78	FF 0011001001	< 0011111001	FF 0011000001	FF 0011000011
79	(0001011001	(0001011001	(0001011001	(0001011011
80	9 1001111001	(0001011001	9 1001111011	EM 1001100001
81	o 1111010101	O 1111000101	o 1111011111	] 1011100101
82	l 0011010101	L 0011000101	l 0011011111	X 0001100101
83	, 0011011001	, 0011011001	, 0011011001	, 0011011011
84	. 0111011001	. 0111011001	. 0111011001	. 0111011011
85	; 1101111001	: 0101111001	; 1101111001	: 0101111001
86	] 1011100101	[1101100101	] 1011100101	[1101100101
87	- 1011011001	— 1111100101	- 1011011001	— 1111100101
88	0 0000111001	0 0000111001	0 0000111001	0 0000111001
89	9 1001111001	) 1001011001	HT 1001000001	HT 1001000001

Options:
Internal oscillator (pins 1, 2, 3)
Any key down (pin 4) positive output
N key rollover only

Pulse data ready signal
Internal resistor to V_{DD} on shift and control pins
KR3600-STD outputs provides ASC II bits 1-6 on B1-B6, and bit 7 on B8

KR 3600-ST

XY	Normal B-123456789	Shift B-123456789	Control B-123456789	Shift/Control B-123456789
00	\ 000001101	~ 011111101	NUL 000000001	RS 011110001
01	= 101111010	+ 110101001	GS 101110001	VT 110100010
02	DC3 110010010	DC3 110010010	DC3 110010010	DC3 110010010
03	— 101101001	— 111110101	CR 101100010	US 111110010
04	BS 000100010	BS 000100010	BS 000100010	BS 000100010
05	0 000011001	0 000011001	0 000011001	0 000011001
06	• 011101001	• 011101001	• 011101001	• 011101001
07	000000000	000000000	000000000	000000000
08	000000000	000000000	000000000	000000000
09	000000000	000000000	000000000	000000000
10	/ 111101010	? 111111001	ST 111100001	US 111110010
11	• 011101001	> 011111010	SO 011100010	RS 011110001
12	? 001101010	< 001111001	FF 001100001	FS 001110010
13	m 101101110	M 101100101	CR 101100010	CR 101100010
14	n 011101110	N 011100101	SO 011100010	SO 011100010
15	b 010001110	B 010000101	STX 010000010	STX 010000010
16	v 011011110	V 011010101	SYN 011010010	SYN 011010010
17	c 110001101	C 110000110	ETX 110000001	ETX 110000001
18	x 000111101	X 000110110	CAN 000110001	CAN 000110001
19	z 010111110	Z 010110101	SUB 010110010	SUB 010110010
20	LF 010100001	LF 010100001	LF 010100001	LF 010100001
21	\ 001110101	; 001111110	FS 001110010	FS 001110010
22	DEL 111111110	DEL 111111110	DEL 111111110	DEL 111111110
23	[110110110	] 101110110	ESC 110110001	GS 101110001
24	7 111011010	7 111011010	7 111011010	7 111011010
25	8 000111010	8 000111010	8 000111010	8 000111010
26	9 100111001	9 100111001	9 100111001	9 100111001
27	000000000	000000000	000000000	000000000
28	000000000	000000000	000000000	000000000
29	000000000	000000000	000000000	000000000
30	; 110111010	: 010111001	ESC 110110001	SUB 010110010
31	l 001101101	L 001100110	FF 001100001	FF 001100001
32	k 110101110	K 110100101	VT 110100010	VT 110100010
33	j 010101101	J 010100110	LF 010100001	LF 010100001
34	h 000101110	H 000100101	BS 000100010	BS 000100010
35	g 111001110	G 111000101	BEL 111000010	BEL 111000010
36	f 011001101	F 011000110	ACK 011000001	ACK 011000001
37	d 001001110	D 001000101	EOT 001000010	EOT 001000010
38	s 110011110	S 110010101	DC3 110010010	DC3 110010010
39	a 100001110	A 100000101	SOH 100000010	SOH 100000010
40	000000000	000000000	000000000	000000000
41	{ 110111101	} 101111101	ESC 110110001	GS 101110001
42	GR 101100010	GR 101100010	GR 101100010	GR 101100010
43	' 111001001	" 010001001	BEL 111000010	STX 010000010
44	4 001011010	4 001011010	4 001011010	4 001011010
45	5 101011001	5 101011001	5 101011001	5 101011001
46	6 011011001	6 011011001	6 011011001	6 011011001
47	000000000	000000000	000000000	000000000
48	000000000	000000000	000000000	000000000
49	000000000	000000000	000000000	000000000
50	p 000011110	P 000010101	DEL 000010010	DEL 000010010
51	o 111101101	O 111100110	SI 111100001	SI 111100001
52	i 100101101	I 100100110	HT 100100001	HT 100100001
53	u 101011110	U 101010101	NAK 101010010	NAK 101010010
54	y 100111110	Y 100110101	EM 100110010	EM 100110010
55	t 001011101	T 001010110	DC4 001010001	DC4 001010001
56	r 010011101	R 010010110	DC2 010010001	DC2 010010001
57	e 101001101	E 101000110	ENQ 101000001	ENQ 101000001
58	w 111011101	W 111010110	ETB 111010001	ETB 111010001
59	q 100011101	Q 100010110	DC1 100010001	DC1 100010001
60	000000000	000000000	000000000	000000000
61	000000000	000000000	000000000	000000000
62	DC2 010010001	DC2 010010001	DC2 010010001	DC2 010010001
63	000000000	000000000	000000000	000000000
64	1 100011010	1 100011010	1 100011010	1 100011010
65	2 010011010	2 010011010	2 010011010	2 010011010
66	3 110011001	3 110011001	3 110011001	3 110011001
67	000000000	000000000	000000000	000000000
68	000000000	000000000	000000000	000000000
69	000000000	000000000	000000000	000000000
70	0 000011001	) 100101010	DLE 000010010	HT 100100001
71	9 100111001	(000101001	EM 100110010	BS 000100010
72	8 000111010	* 010101010	CAN 000110001	LF 010100001
73	7 111011010	& 011001010	ETB 111010001	ACK 011000001
74	6 011011001	^ 011110110	SYN 011010010	RS 011110001
75	5 101011001	% 101001010	NAK 101010010	ENQ 101000001
76	4 001011010	$ 001001001	DC4 001010001	EOT 001000010
77	3 110011001	# 110001010	DC3 110010010	ETX 110000001
78	2 010011010	@ 000000110	DC2 010010001	NUL 000000001
79	1 100011010	! 100001001	DC1 100010001	SOH 100000010
80	000000000	000000000	000000000	000000000
81	000000000	000000000	000000000	000000000
82	000000000	000000000	000000000	000000000
83	000000000	000000000	000000000	000000000
84	000000000	000000000	000000000	000000000
85	SP 000001010	SP 000001010	NUL 000000001	NUL 000000001
86	000000000	000000000	000000000	000000000
87	DC1 100010001	DC1 100010001	DC1 100010001	DC1 100010001
88	HT 100100001	HT 100100001	HT 100100001	HT 100100001
89	ESC 110110001	ESC 110110001	ESC 110110001	ESC 110110001

Options: Pin 1, 2, 3—Internal oscillator
Pin 4—Lockout (logic 1), rollover (logic 0)
Pin 5—Any key down output

All outputs complemented

XY	Normal	Shift	Control	Shift/Control
00	000000000	001000000	010000000	011000000
01	000000001	001000001	010000001	011000001
02	000000010	001000010	010000010	011000010
03	000000011	001000011	010000011	011000011
04	000000100	001000100	010000100	011000100
05	000000101	001000101	010000101	011000101
06	000000110	001000110	010000110	011000110
07	000000111	001000111	010000111	011000111
08	000001000	001001000	010001000	011001000
09	000001001	001001001	010001001	011001001
10	000001010	001001010	010001010	011001010
11	000001011	001001011	010001011	011001011
12	000001100	001001100	010001100	011001100
13	000001101	001001101	010001101	011001101
14	000001110	001001110	010001110	011001110
15	000001111	001001111	010001111	011001111
16	000010000	001010000	010010000	011010000
17	000010001	001010001	010010001	011010001
18	000010010	001010010	010010010	011010010
19	000010011	001010011	010010011	011010011
20	000010100	001010100	010010100	011010100
21	000010101	001010101	010010101	011010101
22	000010110	001010110	010010110	011010110
23	000010111	001010111	010010111	011010111
24	000011000	001011000	010011000	011011000
25	000011001	001011001	010011001	011011001
26	000011010	001011010	010011010	011011010
27	000011011	001011011	010011011	011011011
28	000011100	001011100	010011100	011011100
29	000011101	001011101	010011101	011011101
30	000011110	001011110	010011110	011011110
31	000011111	001011111	010011111	011011111
32	000100000	001100000	010100000	011100000
33	000100001	001100001	010100001	011100001
34	000100010	001100010	010100010	011100010
35	000100011	001100011	010100011	011100011
36	000100100	001100100	010100100	011100100
37	000100101	001100101	010100101	011100101
38	000100110	001100110	010100110	011100110
39	000100111	001100111	010100111	011100111
40	000101000	001101000	010101000	011101000
41	000101001	001101001	010101001	011101001
42	000101010	001101010	010101010	011101010
43	000101011	001101011	010101011	011101011
44	000101100	001101100	010101100	011101100
45	000101101	001101101	010101101	011101101
46	000101110	001101110	010101110	011101110
47	000101111	001101111	010101111	011101111
48	000110000	001110000	010110000	011110000
49	000110001	001110001	010110001	011110001
50	000110010	001110010	010110010	011110010
51	000110011	001110011	010110011	011110011
52	000110100	001110100	010110100	011110100
53	000110101	001110101	010110101	011110101
54	000110110	001110110	010110110	011110110
55	000110111	001110111	010110111	011110111
56	000111000	001111000	010111000	011111000
57	000111001	001111001	010111001	011111001
58	000111010	001111010	010111010	011111010
59	000111011	001111011	010111011	011111011
60	000111100	001111100	010111100	011111100
61	000111101	001111101	010111101	011111101
62	000111110	001111110	010111110	011111110
63	000111111	001111111	010111111	011111111
64	100000000	101000000	110000000	111000000
65	100000001	101000001	110000001	111000001
66	100000010	101000010	110000010	111000010
67	100000011	101000011	110000011	111000011
68	100000100	101000100	110000100	111000100
69	100000101	101000101	110000101	111000101
70	100000110	101000110	110000110	111000110
71	100000111	101000111	110000111	111000111
72	100001000	101001000	110001000	111001000
73	100001001	101001001	110001001	111001001
74	100001010	101001010	110001010	111001010
75	100001011	101001011	110001011	111001011
76	100001100	101001100	110001100	111001100
77	100001101	101001101	110001101	111001101
78	100001110	101001110	110001110	111001110
79	100001111	101001111	110001111	111001111
80	100010000	101010000	110010000	111010000
81	100010001	101010001	110010001	111010001
82	100010010	101010010	110010010	111010010
83	100010011	101010011	110010011	111010011
84	100010100	101010100	110010100	111010100
85	100010101	101010101	110010101	111010101
86	100010110	101010110	110010110	111010110
87	100010111	101010111	110010111	111010111
88	100011000	101011000	110011000	111011000
89	100011001	101011001	110011001	111011001

Options:
Internal oscillator (pins 1, 2, 3)
Lockout/rollover (pin 4), with internal resistor to VDD
Lockout is logic 1
Any key down (pin 5), positive output
Pulse data ready
Internal resistor to VDD on shift & control pins

DESCRIPTION

The KR 3600 PRO is a MOS/LSI device intended to simplify the interface of a microprocessor to a keyboard matrix. Like the other KR 3600 parts, the KR 3600 PRO contains all of the logic to de-bounce and encode keyswitch closures, while providing either a 2-key or N-key rollover.

The output of the KR 3600 PRO is a simple binary code which may be converted to a standard information code by a PROM or directly by a microprocessor. This permits a user maximum flexibility of key layout with simple field programming.

The code in the KR 3600 is shown in Table I. The format is simple: output bits 9, 8, 7, 6, 5, 4 and 1 are a binary sequence. The count starts at X0, Y0 and increments through X0Y1, X0Y2...X8Y9. Bit 9 is the LSB; bit 1 is the MSB.

Bits 2 and 3 indicate the mode as follows:

Bit 2	Bit 3	
0	0	Normal
0	1	Shift
1	0	Control
1	1	Shift Control

For maximum ease of use and flexibility, an internal scanning oscillator is used, with pin selection of N-key lockout (also known as 2-key rollover) and N-key rollover. An "any-key-down" output is provided for such uses as repeat oscillator keying.

Figure 1 shows a PROM-encoded 64 key, 4 mode application, using a 256x8 PROM, and Figure 2 a full 90 key, 4 mode application, utilizing a 512x8 PROM.

If N-key rollover operation is desired, it is recommended that a diode be inserted in series with each switch as shown. This prevents "phantom" key closures from resulting if three or more keys are depressed simultaneously.

FIGURE 1
KR 3600 PRO TYPICAL APPLICATION
64 KEY, 4 MODE

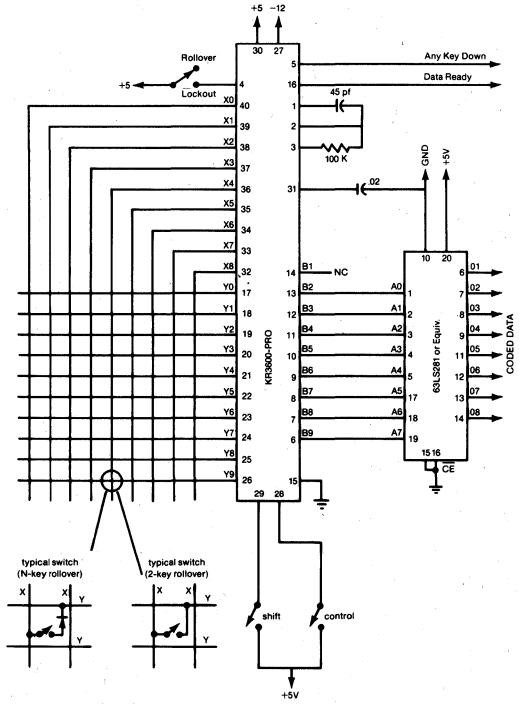
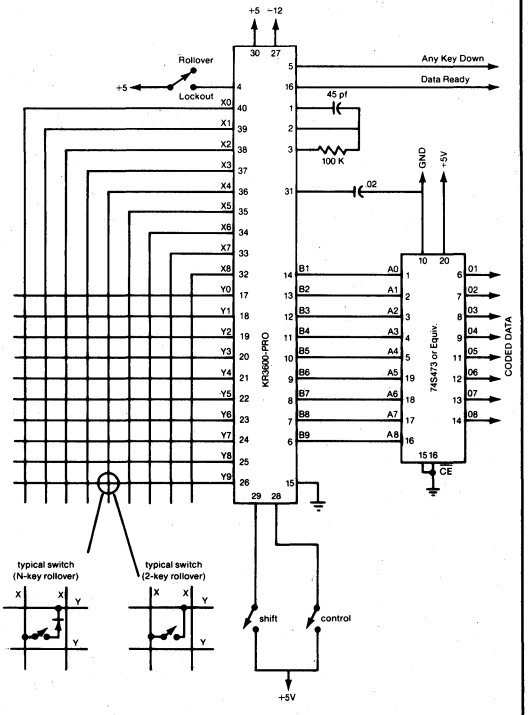


FIGURE 2
KR 3600 PRO TYPICAL APPLICATION
90 KEY, 4 MODE



Microprocessor Peripheral

ROM

art Number	Description	Access Time	Power Supply	Package	Page
DM 2316E[1][3]	16K ROM; 16,384 bits organized 2048x8	450 nsec	+5	24 DIP	221-222
DM 4732[3]	32K ROM; 32,768 bits organized 4096x8	450 nsec	+5	24 DIP	223-226
DM 36000[1][3]	64K ROM; 65,536 bits organized 8192x8	250 nsec	+5	24 DIP	227-230

FLOPPY DISK

Part Number	Description	Sector Format	Density	IBM Compatible	Write Pre-compensation	Power Supplies	Package	Page
FDC 1791[1]	Floppy Disk Controller/Formatter	Soft	Double	Yes	External	+5, +12	40 DIP	241-242
FDC 1792[1]		Soft	Single	Yes	External	+5, +12	40 DIP	241-242
FDC 1793[1]		Soft	Double	Yes	External	+5, +12	40 DIP	241-242
FDC 1794[1]		Soft	Single	Yes	External	+5, +12	40 DIP	241-242
FDC 3400	Floppy Disk Data Handler provides serial/parallel interface, sync detection	Hard	N.A.	N.A.	No	+5, −12	40 DIP	231-238
FDC 7003[1]	Floppy Disk Controller/Formatter	Soft	Single/ Double	Yes	Internal	+5	40 DIP	239-240

CASSETTE/CARTRIDGE

art Number	Description	Max Data Rate	Features	Power Supply	Package	Page
CC 3500	Cassette/Cartridge Data Handler	250K bps	Sync byte detection, Read While Write	+5, −12	40 DIP	243-250

For future release
May be custom mask programmed

SECTION VIII

STANDARD MICROSYSTEMS CORPORATION
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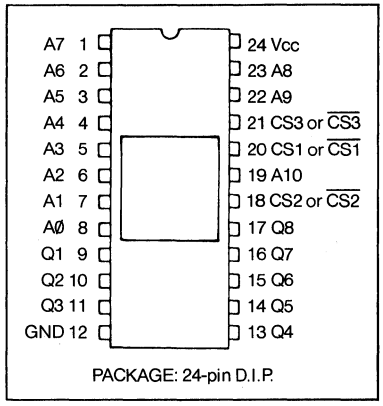
(516) 273-3100 · TWX-510-227-8898
We keep ahead of our competition so you can keep ahead of yours.

2048 X 8-Bit Static Read-Only Memory 16K ROM

FEATURES

- ☐ 2048 x 8 Organization
- ☐ All Inputs and Outputs TTL-Compatible
- ☐ Fully Static (No Clocks, No Refresh)
- ☐ Single + 5v Power Supply
- ☐ Maximum Access Time...450ns
- ☐ Minimum Cycle Time...450ns
- ☐ Low Power Dissipation
- ☐ Three-State Outputs for Wire-OR Expansion
- ☐ Industry Standard 24 pin DIP Pin Out
- ☐ Pin Compatible with Intel 2316E and GI RO3-9316
- ☐ Three programmable chip select inputs for Chip Select Flexibility
- ☐ Automated Custom Programming—Formats—Media
- ☐ COPLAMOS® N-Channel MOS Technology

PIN CONFIGURATION



PACKAGE: 24-pin D.I.P.

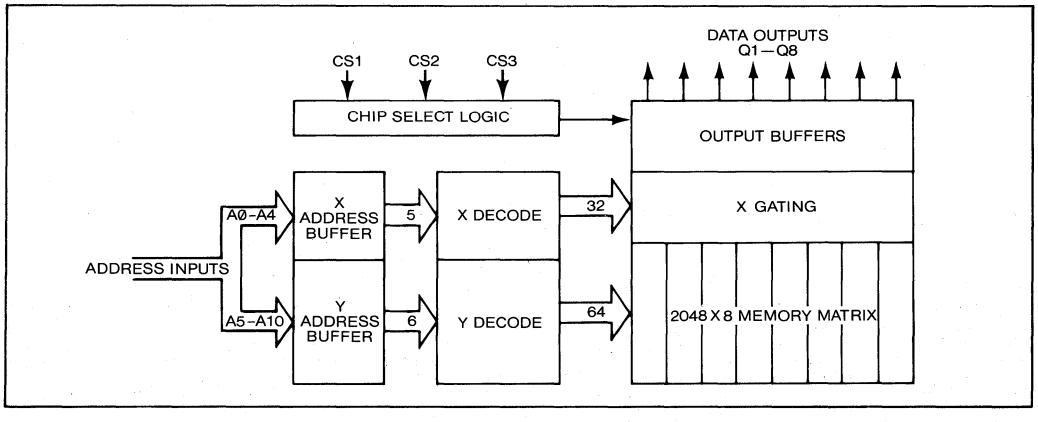
GENERAL DESCRIPTION

The ROM 2316E is a 16,384-bit read-only memory organized as 4096 words of 8-bit length. This makes the ROM 2316E ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any external pull-up resistor. Each output can drive one Series 74 or 74S load without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus, facilitating easy memory expansion. Three chip select controls allow data to be read. These controls are programmable, providing additional system decode flexibility allowing eight 16K ROMs to be OR-tied without external decoding. The data is always available, it is not dependent on external CE clocking.

The ROM 2316E is designed for high-density fixed-memory applications such as logic function generation and microprogramming.

BLOCK DIAGRAM



*FOR FUTURE RELEASE

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +7.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

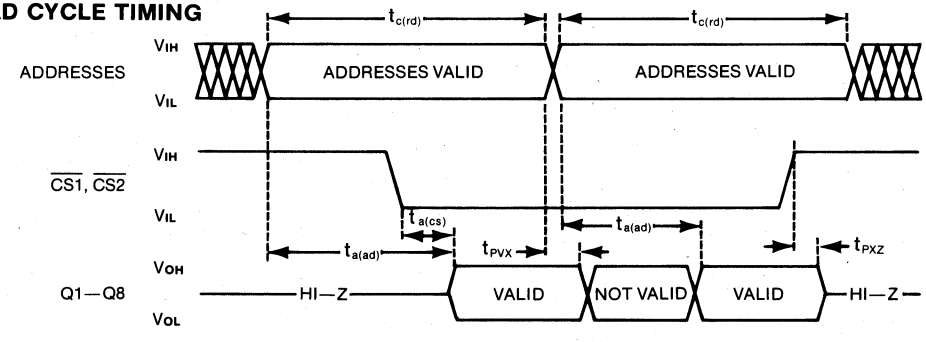
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.65	V	
High-level, V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 2.0mA
High-level, V_{OH}	2.4			V	I_{OH} = −200μA
INPUT CURRENT					
Low-level, I_{IL}			10	μA	$0V \leq V_{IN} \leq V_{CC}$
OUTPUT CURRENT					
I_{OL}			±10	μA	Chip Deselected
INPUT CAPACITANCE					
All inputs, C_{IN}			7	pF	
OUTPUT CAPACITANCE					
All Outputs, C_{OUT}			10	pF	
POWER SUPPLY CURRENT					
I_{CC}					
A.C. CHARACTERISTICS					1 Series 74 TTL load, C_L = 100 pF
Read cycle time, $t_{c(rd)}$	450			ns	
Access time from address, $t_{a(ad)}$			450	ns	
Access time from chip select, $t_{a(cs)}$			200	ns	
Previous output data valid after address change, t_{PVX}			450	ns	
Output disable time from chip select, t_{PXZ}			200	ns	

READ CYCLE TIMING



STANDARD MICROSYSTEMS CORPORATION
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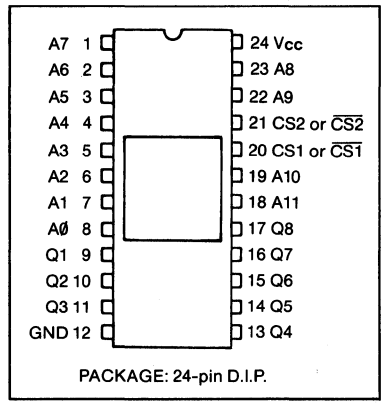
(516) 273-3100 · TWX-510-227-8898
We keep ahead of our competition so you can keep ahead of yours.

4096 X 8-Bit Static Read-Only Memory 32K ROM

FEATURES

- ☐ 4096 x 8 Organization
- ☐ All Inputs and Outputs TTL-Compatible
- ☐ Fully Static (No Clocks, No Refresh)
- ☐ Single +5v Power Supply
- ☐ Maximum Access Time...450ns
- ☐ Minimum Cycle Time...450ns
- ☐ Typical Power Dissipation...580mW
- ☐ Three-State Outputs for Wire-OR Expansion
- ☐ Industry Standard 24 pin DIP Pin Out
- ☐ Pin Compatible with TMS 4732, TMS 4700, TMS 2708 and Intel 2316E
- ☐ Two programmable chip select inputs for Chip Select Flexibility
- ☐ Automated Custom Programming—Formats—Media
- ☐ COPLAMOS® N-Channel MOS Technology

PIN CONFIGURATION



PACKAGE: 24-pin D.I.P.

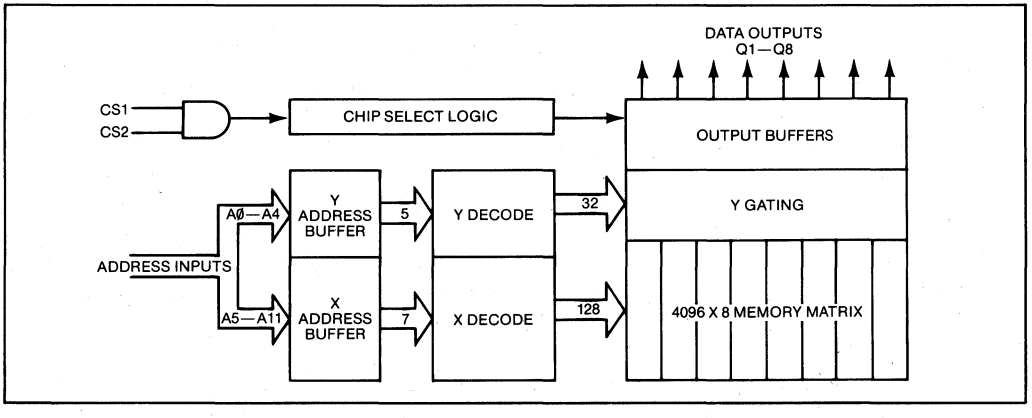
GENERAL DESCRIPTION

The ROM 4732 is a 32,768-bit read-only memory organized as 4096 words of 8-bit length. This makes the ROM 4732 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any external pull-up resistor. Each output can drive one Series 74 or 74S load without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus, facilitating easy memory expansion. Two chip select controls allow data to be read. These controls are programmable, providing additional system decode flexibility allowing four 32K ROMs to be OR-tied without external decoding. The data is always available, it is not dependent on external CE clocking.

The ROM 4732 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. Systems utilizing 1024 x 8-bit ROMs or 1024 x 8-bit EPROMs can expand to the 4096 x 8-bit ROM 4732 with changes only to pins 18, 19, and 21. To upgrade from the 2316E, simply replace CS2 with A11 on pin 18.

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +7.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

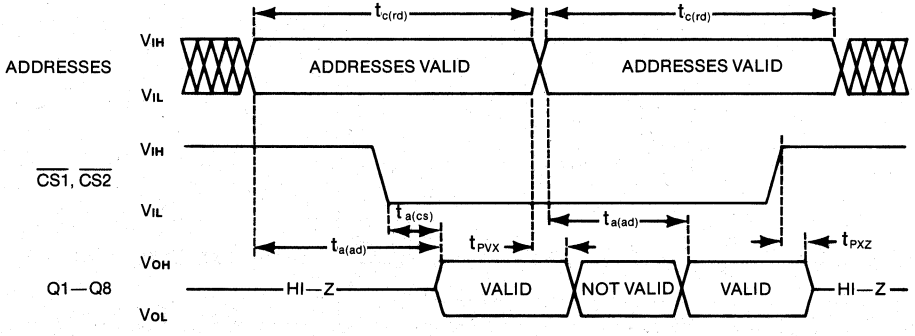
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.65	V	
High-level, V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 2.0mA
High-level, V_{OH}	2.4			V	I_{OH} = −200μA
INPUT CURRENT					
Low-level, I_{IL}			10	μA	$0V \leq V_{IN} \leq V_{CC}$
OUTPUT CURRENT					
I_{OL}			±10	μA	Chip Deselected
INPUT CAPACITANCE					
All inputs, C_{IN}			7	pF	
OUTPUT CAPACITANCE					
All Outputs, C_{OUT}			10	pF	
POWER SUPPLY CURRENT					
I_{CC}			150	mA	
A.C. CHARACTERISTICS					1 Series 74 TTL load, C_L = 100 pF
Read cycle time, $t_{c(rd)}$	450			ns	
Access time from address, $t_{a(ad)}$			450	ns	
Access time from chip select, $t_{a(cs)}$			200	ns	
Previous output data valid after address change, t_{PVX}			450	ns	
Output disable time from chip select, t_{PXZ}			200	ns	

READ CYCLE TIMING



Description of Pin Functions

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 18, 19, 22, 23	A7, A6, A5, A4, A3, A2, A1, AØ, A11, A10, A9, A8	Addresses	I	The 12-bit positive-logic address is decoded on-chip to select one of 4096 words of 8-bit length in the memory array. AØ is the least significant bit and A11 the most significant bit of the word address. The address valid interval determines the device cycle time.
9, 10, 11, 13, 14, 15, 16, 17	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	Data Outputs	0	The eight outputs must be enabled by both chip select controls before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least significant bit, Q8 the most significant bit. The outputs will drive TTL circuits without external components.
12	GND	Ground	GND	Ground
20, 21	CS1, CS2	Chip Select	I	Each chip select control can be programmed during mask fabrication to be active with either a high or a low level input. When both chip select signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either chip select is not active, all eight outputs are in a high-impedance state.
24	V_{cc}	Power Supply	PS	+5 volt power supply

PROGRAMMING DATA

PROGRAMMING REQUIREMENTS: The ROM 4732 is a fixed program memory in which the programming is performed via computer aided techniques by SMC at the factory during the manufacturing cycle to the specific customer inputs supplied in the punched computer card format below. The device is organized as 4096 8-bit words with address locations numbered Ø to 4095. The 8-bit words can be coded as a 2-digit hexadecimal number between ØØ and FF. All data words and addresses in the following format are coded in hexadecimal numbers. In coding, all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least significant bit and Q8 the most significant bit. For addresses, AØ is least significant bit and A11 is the most significant bit.

Every card should include the SMC Custom Device Number in the form ROXXXX (4 digit number to be assigned by SMC) in column 75 through 80.

PROGRAMMABLE CHIP SELECTS: The chip select inputs shall be programmed according to the data punched in columns 73 and 74. Every card should include in column 73 a 1 if the output is to be enabled with a high level at CS2 or a Ø (zero) to enable the output with a low level at CS2. The column 74 entry is the same for programming CS1.

PROGRAMMED DATA FORMAT: The format for the cards to be supplied to SMC to specify that data to be programmed is provided below. The card deck for each device consists of 128 cards with each card containing data for 32 memory locations.

CARD COLUMN	HEXADECIMAL FORMAT
1 to 3	Hexadecimal address of first word on the card
4	Blank
5 to 68	Data. Each 8-bit memory byte is represented by two ASCII characters to represent a hexadecimal value of '00' or 'FF'.
69, 70	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from column 1 to 68, evaluate modulo 256 (carry from high order bit ignored). (For purposes of calculating the checksum, the value of Column 4 is defined to be zero.) Adding together, modulo 256, all 8-bit bytes from Column 1 to 68 (Column 4 = 0), then adding the checksum, results in zero.
71, 72	Blank
73	One (1) or zero (Ø) for CS2
74	One (1) or zero (Ø) for CS1
75, 76	RO
77 to 80	XXXX (4 digit number assigned by SMC)

ALTERNATIVE INPUT MEDIA

In addition to the preferred 80 column "IBM Card," customers may submit their ROM bit patterns on 9-track 800-BPI mag tape, 8-channel perforated paper tape, EPROM, ROM, etc. Where one of several nationwide time sharing services is mutually available, arrangements may be made with the factory to communicate the ROM definition data directly through the service computer. Format requirements and other information required to use alternative input media may be obtained through SMC sales personnel.

ALTERNATIVE DATA FILE FORMATS

In addition to the standard SMC format, it is possible to furnish data to SMC in other formats if prearranged with the factory. Non-standard formats may be acceptable. Contact SMC sales personnel.

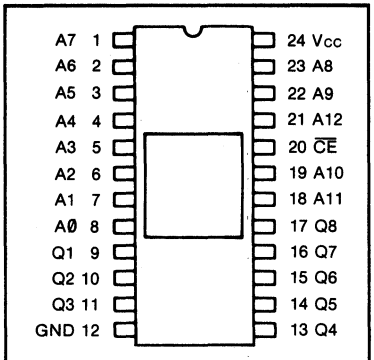
STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11787
(516) 273-3100 TWX-510-227-8898
We keep ahead of our competition so you can keep ahead of yours.

8192 X 8-Bit Static Read-Only Memory
64K ROM

FEATURES

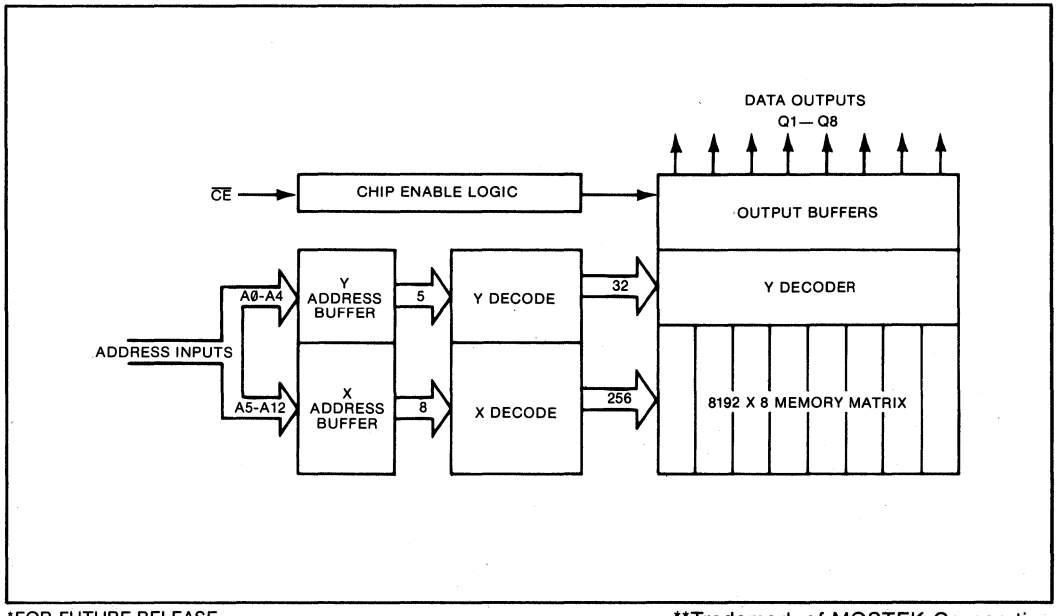
- ☐ 8192 X 8 Organization
- ☐ All Inputs and Outputs TTL-Compatible
- ☐ Edge Activated**
- ☐ Single +5V±10% Power Supply
- ☐ Maximum Access Time...250ns
- ☐ Minimum Cycle Time...375ns
- ☐ Low Power Consumption...220mW max active
- ☐ Low Standby Power Dissipation...35mW typical
- ☐ Three-State Outputs for Wire-OR Expansion
- ☐ Industry Standard 24 Pin DIP Pin Out
- ☐ Pin Compatible with MOSTEK MK36000-4
- ☐ On-Chip Address Latches
- ☐ Outputs drive 2 TTL loads and 100pf
- ☐ COPLAMOS® N-Channel MOS Technology

PIN CONFIGURATION



PACKAGE: 24-pin D.I.P.

BLOCK DIAGRAM



*FOR FUTURE RELEASE

**Trademark of MOSTEK Corporation

SECTION VIII

GENERAL DESCRIPTION

The ROM 36000 is a new generation N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the ROM 36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

The ROM 36000 utilizes what is fast becoming an industry standard method of device operation. Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 35mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed. The ROM 36000 features onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be wire- 'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The ROM 36000 operates from a single +5 volt power supply with a wide ±10% tolerance, providing the widest operating margins available. The ROM 36000 is packaged in the industry standard 24 pin DIP.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... −0.5V to +7V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... −65°C to +150°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±10%, unless otherwise noted)

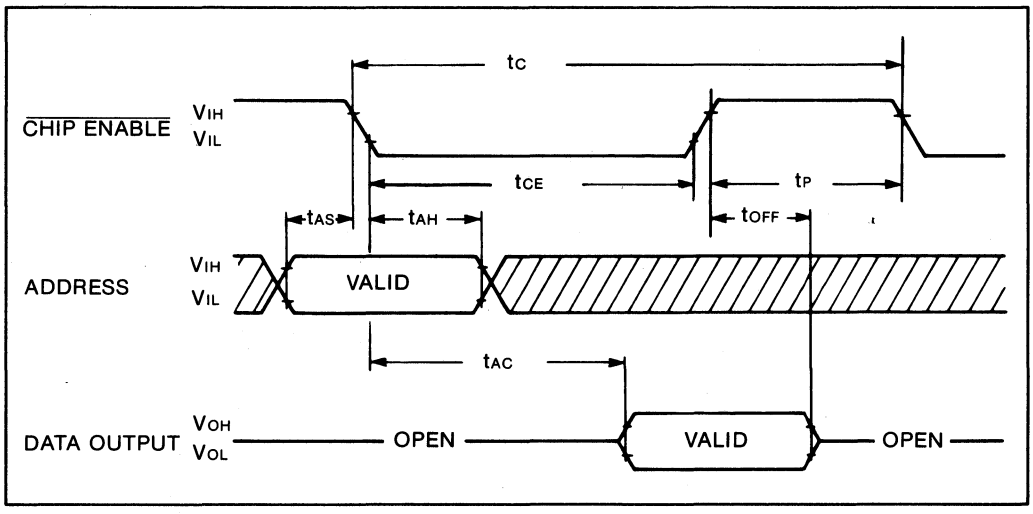
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	6
Input Logic 0 Voltage	V_{IL}	−0.5		0.8	Volts	
Input Logic 1 Voltage	V_{IH}	2.0		V_{CC}	Volts	
DC ELECTRICAL CHARACTERISTICS						
V_{CC} Power Supply Current (Active)	I_{CC1}			40	mA	1
V_{CC} Power Supply Current (Standby)	I_{CC2}		7		mA	7
Input Leakage Current	$I_{I(L)}$	−10		10	µA	2
Output Leakage Current	$I_{O(L)}$	−10		10	µA	3
Output Logic "0" Voltage @ I_{OUT} = 3.3mA	V_{OL}			0.4	Volts	
Output Logic "1" Voltage @ I_{OUT} = −220µA	V_{OH}	2.4			Volts	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
AC ELECTRICAL CHARACTERISTICS						
Cycle Time	t_C	375			ns	4
$\overline{CE}$ Pulse Width	t_{CE}	250				4
$\overline{CE}$ Access Time	t_{AC}			250	ns	4
Output Turn Off Delay	t_{OFF}			60	ns	4
Address Hold Time Referenced to $\overline{CE}$	t_{AH}	60			ns	
Address Setup Time Referenced to $\overline{CE}$	t_{AS}	0			ns	
CE Precharge Time	t_P	125			ns	
CAPACITANCE						
Input Capacitance	CI		5		pF	5
Output Capacitance	CO		7		pF	5

NOTES:

1. Current is proportional to cycle rate. I_{CCI} is measured at the specified minimum cycle time.
2. V_{IN} = 0V to 5.5V.
3. Device unselected; V_{OUT} = 0V to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts
6. A minimum 100μs time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.
7. $\overline{CE}$ high.

TIMING DIAGRAM



OPERATION

The ROM 36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the onchip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

PROGRAMMING

Standard Microsystems Corporation will accept data input in the form of 8K, 16K, 32K and 64K EPROMS and 8K, 16K, 32K and 64K ROMS. If other programming media is preferable, please consult the factory.

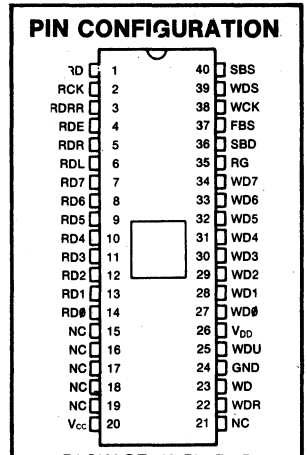
Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and to supply the best product possible.

Floppy Disk Hard Sector Data Handler HSDH

FEATURES

- ☐ Hard-Sectored Operation — performs all data operations
- ☐ Single or Double Density Operation — recording code independent
- ☐ Minifloppy or Standard Floppy compatible
- ☐ Programmable Sync Byte
- ☐ Internal Sync Byte Detection and Byte Framing
- ☐ Fully Double Buffered
- ☐ Data Overrun/Underrun Detection
- ☐ Dual Disk Operation — Write on one disk drive while simultaneously reading from another
- ☐ Tri-State Output Bus for processor compatibility
- ☐ TTL Compatible Inputs and Outputs

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

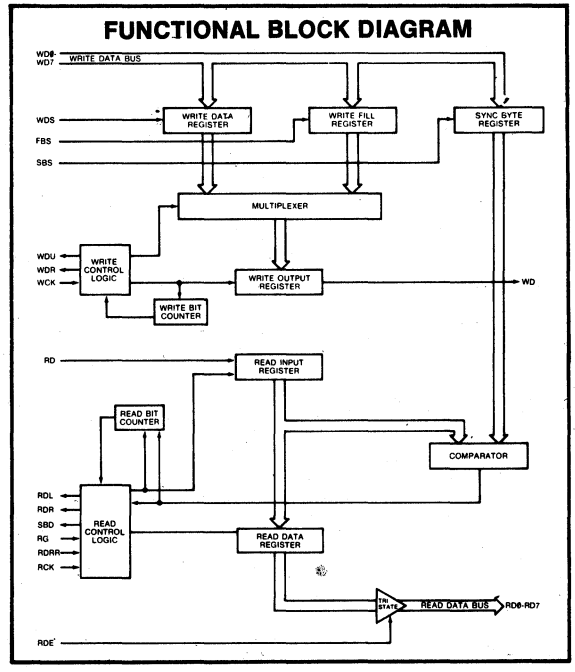
GENERAL DESCRIPTION

The FDC3400 is an MOS integrated circuit which simplifies the data interface between a processor and a floppy disk drive. During a write operation, the HSDH receives data from the processor and shifts it out bit-serially to the floppy disk data encoding logic. Similarly, during a read operation the HSDH receives a bit-serial stream of read data from the floppy disk data separator, establishes byte synchronization by detecting the sync byte, and transfers data on a byte by byte basis to the processor.

The HSDH detects data overrun and underrun conditions and indicates these conditions on its status lines. A data underrun causes write data to be written onto the disk from a special programmable fill register until new data is entered into the write data buffer or until the write operation is ended.

Separate read and write data registers permit simultaneous read and write operations on two different drives for enhanced system throughput. The HSDH is fully double buffered and all inputs and outputs are TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION OF OPERATION

Prior to reading or writing on the disk, the read/write head must be positioned and loaded onto the desired track.

Write Operation

The Write Clock is set at the desired bit rate (usually 125, 250, or 500KHz), and the desired fill byte is written into the Write Fill Register. After the external logic makes the write enable to the drive active, the first byte to be written should be loaded into the Write Data Register. This byte is then loaded into the Write Output Register and shifted out bit serially to the external write encoding logic. The first bit shifted out of each byte is the LSB. Whenever a byte is transferred from the Write Data Register to the Write Output Register, Write Data Request becomes active and requests another byte from the processor. If new data is not loaded into the Write Data Register before the Write Output Register becomes empty, then the Write Output Register is loaded with data from the Write Fill Register and the Write Data Underrun status line is set. WDU is reset the next time WDS is pulsed. At the end of the write operation, the processor should return the external write enable line to an inactive state.

Read Operation

The Read Clock is set at the desired bit rate (usually 125, 250, or 500KHz) and the desired sync byte is loaded into the Sync Byte Register. When the processor wishes to read a sector of data it causes a transition on the Read Gate input to set the read logic into a sync byte search mode. In the search mode the serial read data bit stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found, by definition, when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the Sync Byte Detected output is set high. This byte is then loaded into the Read Data Register and the read logic is set into the byte mode. In this mode each byte read is loaded into the Read Data Register and Read Data Request is made active high for each byte. The processor responds to each Read Data Request by enabling the output bus with Read Data Enable, reading the data byte from the Read Data Register, and resetting Read Data Request by pulsing Read Data Request Reset. If the processor fails to respond to Read Data Request within one byte time, the Read Data Lost status line is set. When the processor has read the required amount of data it may reset Read Gate to an inactive-high level.

System Operation — Additional Features

Automatic Sector Fill

In some applications, such as the end of a logical file, the system buffer may contain less than a full sector of data. In this case the processor need supply only this data to the FDC3400. The FDC3400 will then underrun, setting the Write Data Underrun Status line and thereby causing the remainder of the sector to fill with bytes taken from the Write Fill Register. This operation continues until the processor returns the disk's write enable signal to an inactive level.

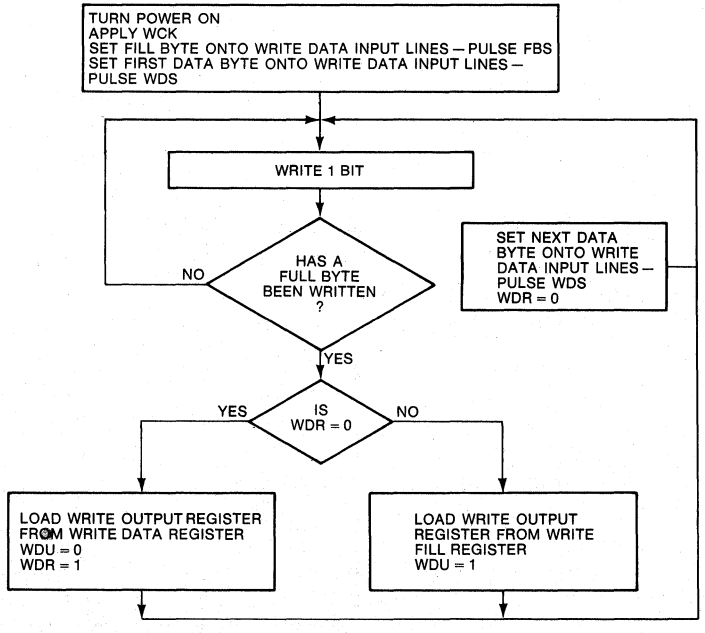
Byte Search

After byte synchronization has been established during a read operation, the processor may load a different byte into the Sync Byte Register. Whenever that byte occurs in the data being read, the Sync Byte Detected status line will go high. This feature permits the processor to search for the occurence of a specific byte while reading a sector.

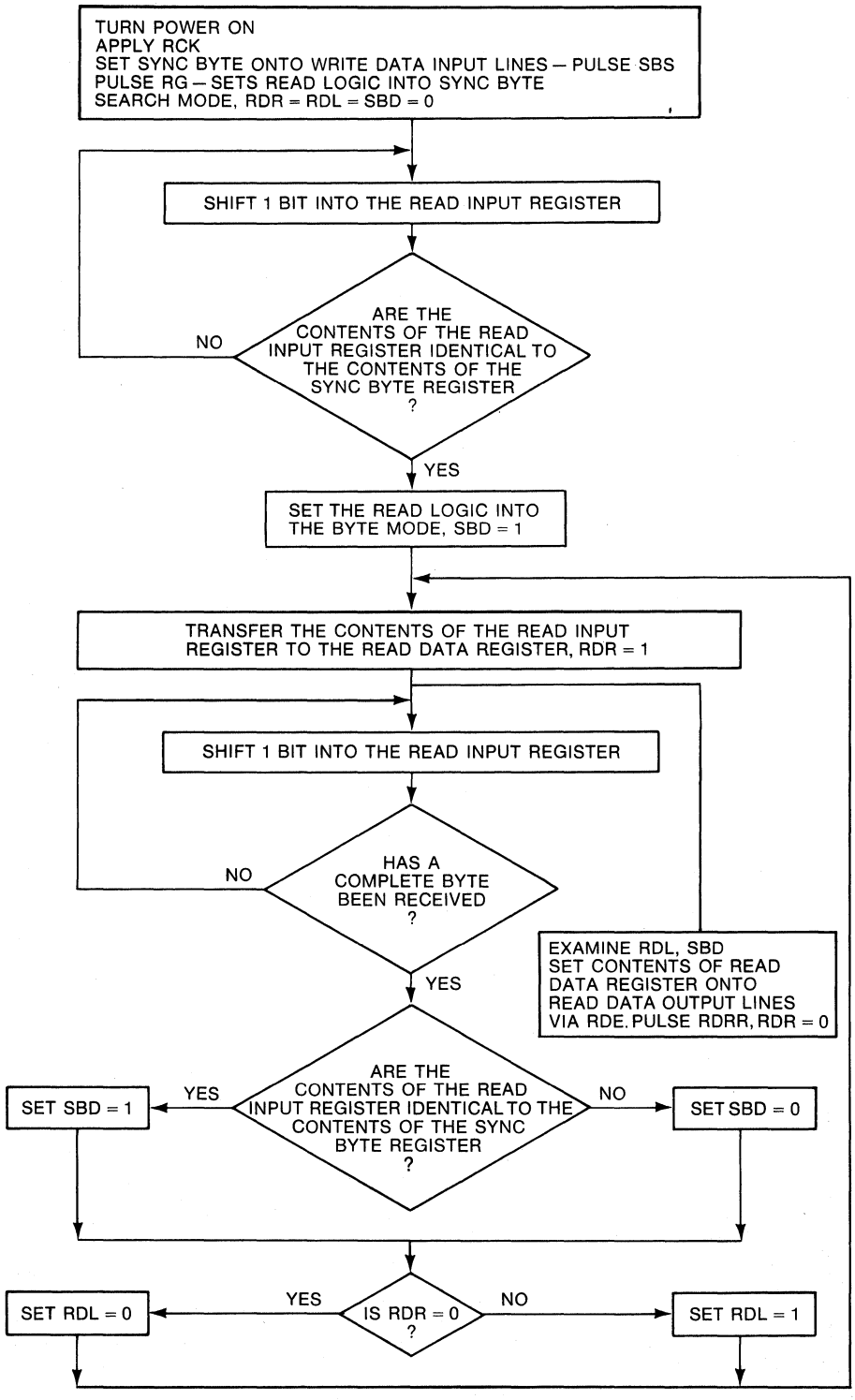
Multiple Byte Synchronization

Some systems use two or more contiguous sync bytes to establish byte synchronization. For these applications, the number of Read Data Requests received while Sync Byte Detected remains active-high may be counted by the processor to establish valid synchronization.

FLOW DIAGRAM — WRITE DATA



FLOW DIAGRAM — READ DATA



DESCRIPTION OF PIN FUNCTIONS

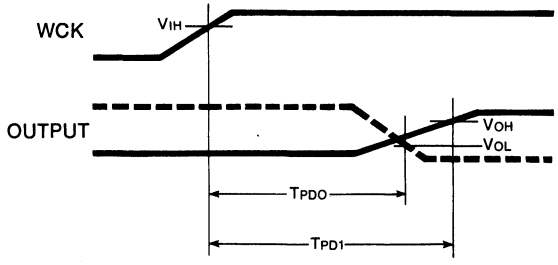
PIN NO.	SYMBOL	NAME	FUNCTION
1	RD	Read Data	The Read Data input accepts the serial data stream from the floppy disk data separator.
2	RCK	Read Clock	The negative-going edge of the Read Clock input shifts Read Data into the Read Input Register.
3	RDRR	Read Data Request Reset	An active-high pulse input on the Read Data Request Reset input resets the RDR output to a low level.
4	RDE	Read Data Enable	An active-high level on the Read Data Enable line gates the outputs of the Read Data Register onto the Read Data Output lines.
5	RDR	Read Data Request	The Read Data Request output is made active-high when an assembled byte is transferred from the Read Input Register to the Read Data Register.
6	RDL	Read Data Lost	The Read Data Lost output is made active-high, if the byte presently in the Read Data Register is not read (RDR not reset) by the processor before the next byte is loaded into the Read Data Register.
7-14	RD7-RDØ	Read Data Output	When enabled by RDE the tri-state Read Data Output lines present the data in the Read Data Register to the processor. When RDE is inactive-low the RD7-RDØ lines are held at a high-impedance state.
15-19	NC		Not Connected
20	V_{CC}	Power Supply	+5 volt supply
21	NC		Not Connected
22	WDR	Write Data Request	The Write Data Request output is made active-high when the Write Data Register becomes empty and requires a data byte. It is reset to a low level when WDS occurs to load the Write Data Register. If WDR is not serviced by the time the next byte is required by the Write Output Register, the byte stored in the Write Fill Register is written onto the disk and the WDU line is made active high.
23	WD	Write Data	The Write Data output presents the serial stream of data to the external write data encoder. Each byte is normally provided from the Write Data Register provided that a WDS pulse occurs during the presently written byte. If WDS is not pulsed, the next byte to be written will be extracted from the Write Fill Register.
24	GND	Ground	Ground
25	WDU	Write Data Underrun	The Write Data Underrun output is set active-high when the processor fails to respond to the WDR signal within one byte time. When WDU occurs the data written on the disk is extracted from the Write Fill Register. This line is reset when WDS is pulsed.
26	V_{DD}	Power Supply	−12 volt supply
27-34	WDØ-WD7	Write Data Input	The Write Data Input lines present information to the Write Data Register, the Write Fill Register, and the Sync Byte Register under control of their respective strobes. The strobes operate independently of each other. The LSB should always be placed on WDØ.
35	RG	Read Gate	This input should be pulsed to a high-level after power turn on to reset RDR, SBD, and RDL to an inactive-low level. The high-to-low transition of RG sets the read logic into the sync byte search mode. In this mode the serial Read Data stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found by definition when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the SBD output is set active-high. The sync byte just read is then transferred into the Read Data Register; RDR is set high, and the read logic is set into the byte mode. In this mode each byte read is transferred into the Read Data Register.
36	SBD	Sync Byte Detected	The Sync Byte Detected output is set active-high each time the byte loaded into the Read Data Register is identical to the byte in the Sync Byte Register. This output is reset low the next time the Read Data Register is loaded with a byte which is not a sync byte.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
37	FBS	Fill Byte Strobe	The Fill Byte Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Write Fill Register.
38	WCK	Write Clock	Each positive-going edge of this clock shifts one bit out of the Write Output Register onto WD.
39	WDS	Write Data Strobe	The Write Data Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Write Data Register.
40	SBS	Sync Byte Strobe	The Sync Byte Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Sync Byte Register.

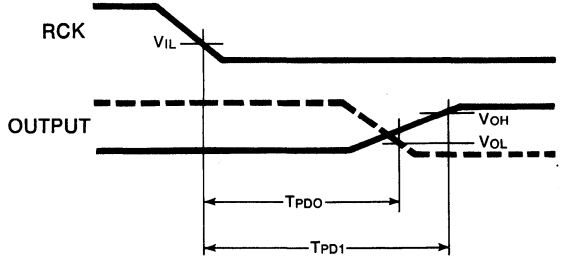
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

WRITE DATA

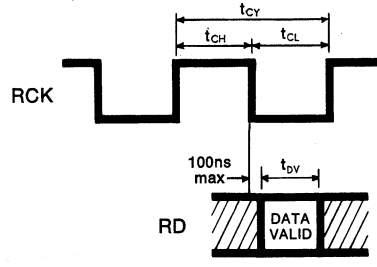


OUTPUT	T_{PDO}	T_{PD1}	UNITS
WDR	NA	2.0	µS
WDU	1.0	1.5	µS
WD	1.0	1.0	µS

READ DATA

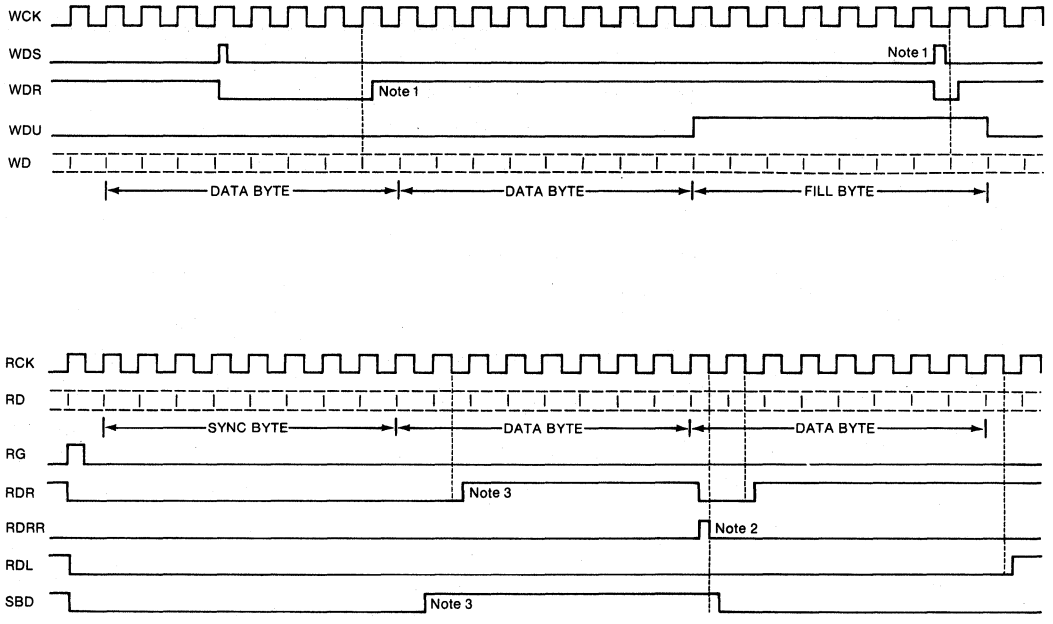


OUTPUT	T_{PDO}	T_{PD1}	UNITS
RDR	NA	1.5	µS
RDL	2.0	2.5	µS
SBD	2.0	2.5	µS
RDØ-RD7	2.5	2.5	µS



MIN. TIMING	FDC3400	FDC3400-1	UNITS
t_{CY}	4.0	2.0	µS
t_{CH}	1.0	0.5	µS
t_{CL}	2.0	1.0	µS
t_{DV}	1.4	0.9	µS

HSDH TIMING DIAGRAM



NOTE 1
The Write Output Register is loaded with the next byte at the positive clock transition corresponding to the leading edge of the last bit of the current byte on the WD output. WDR is set high approximately two microseconds after this clock transition. If it is desired that the next byte be extracted from the Write Data Register the leading edge of the WDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an RDL indication the leading edge of the RDRR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input.

NOTE 3
The RDL, SBD and RD0-RD7 output are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input. The RDR output is set high at the next negative clock transition.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Load Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25V

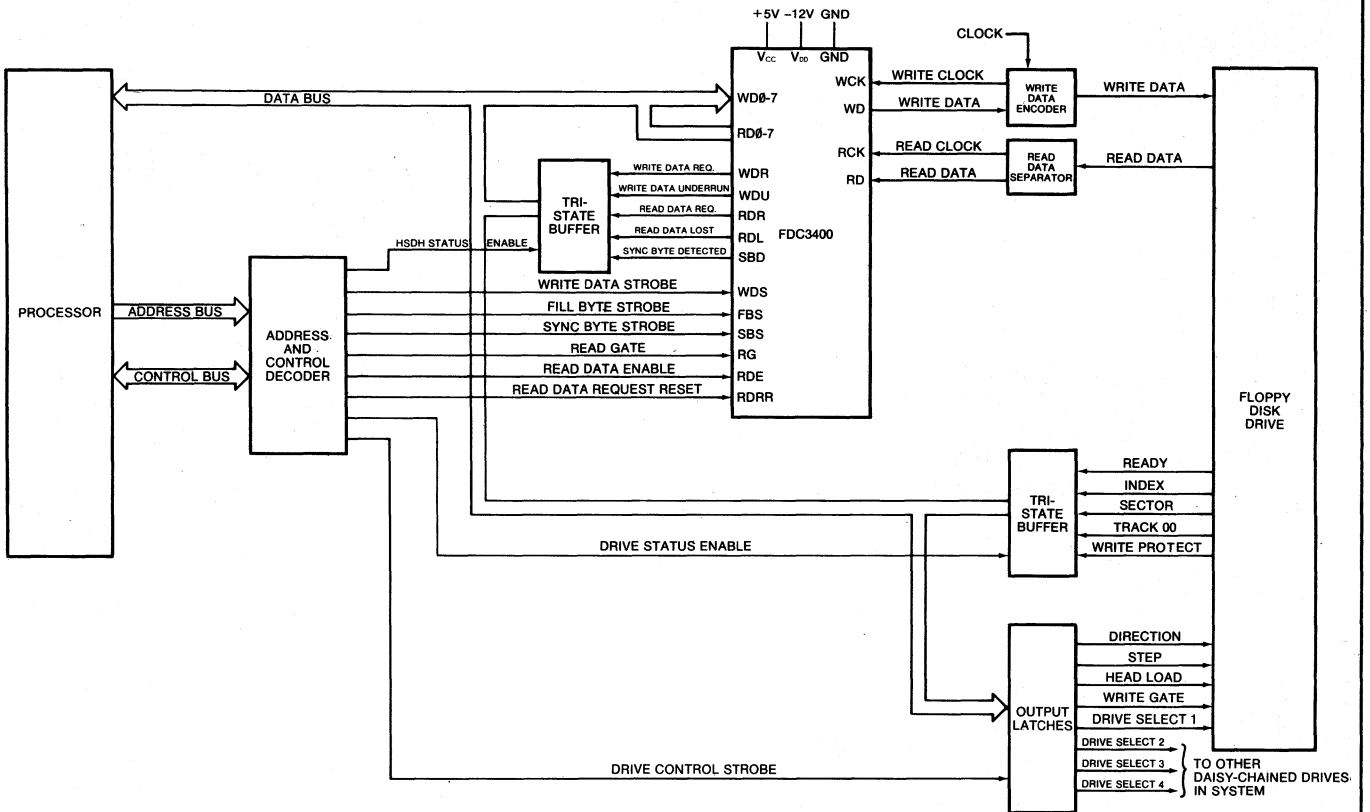
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5% V_{DD} = −12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = −100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	See note 1
OUTPUT CURRENT					
Leakage, I_{LO}			-1	μA	RDE = V_{IL}, 0 ≤ V_{OUT} ≤ +5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pF	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pF	RDE = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}
I_{DD}			28	mA	
A.C. CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY	DC		250	KHz	RCK, WCK
	DC		500	KHz	RCK, WCK, FDC3400-1
PULSE WIDTH					
Clock	1			μs	RCK, WCK
	0.5			μs	RCK, WCK, FDC3400-1
Read Gate	1			μs	RG
Write Data Strobe	200			ns	WDS
Fill Byte Strobe	200			ns	FBS
Sync Byte Strobe	200			ns	SBS
Read Data Request Reset	200			ns	RDRR
INPUT SET-UP TIME					
Write Data Inputs	0			ns	WDØ-WD7
INPUT HOLD TIME					
Write Data Inputs	0			ns	WDØ-WD7
STROBE TO OUTPUT DELAY					Load = 20pf + 1 TTL input
Read Data Enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

**Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing.
   A switching current of 1.6mA maximum flows during a high to low transition of the input.
2. The tri-state output has 3 states:
   1) low-impedance to V_{CC}
   2) low-impedance to GND
   3) high-impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.



TYPICAL CCC 3500 INTERFACE TO PROCESSOR AND CASSETTE/CARTRIDGE DRIVE

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11787
(516) 273-3100 · TWX-510-227-8898

We keep ahead of our competition so you can keep ahead of yours.

FDC 7003*
μPC FAMILY

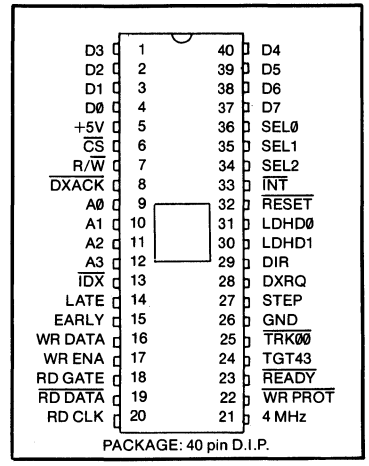
PRELIMINARY

Floppy Disk Controller FDC II

FEATURES

- ☐ FULLY PROGRAMMABLE DATA FORMATS
  - Single or Double Density IBM Soft-Sectored Format (up to 500K bps)
  - Number of Sectors (up to 128)
  - Number of Bytes per Sector (up to 8K)
- ☐ DATA OPERATIONS
  - Automatic Sector Search and Verification
  - Macro Read/Write Commands—Seek/Read or Seek/Write/Verify in One Command
  - Multiple Sector Read/Write—via Sector Count Register
  - Fully Double Buffered
  - Write Data Verification
  - String Search Command—Compares Data in Memory to Data on the Disk
  - Internal Address Mark Detection
  - CRC Data Error Checking
  - Data Overrun/Underrun Detection
  - Write Protect Capability
  - Write Precompensation Outputs
  - Optional Internal Write Precompensation
- ☐ TRACK MOTION OPERATION
  - Seek Command—Moves Head to Desired Track
  - Programmable Track-to-Track Seek Time
  - Selectable Head Settling Time
  - Programmable Head Load Delay
  - Up to 256 Tracks per Side
  - Programmable Head Unload Delay
  - Two Track Registers and Two Head Unload Timers for Control of Two Drives
- ☐ SYSTEM INTERFACE
  - 8-Bit Bi-Directional Three-State Bus for Transfer of Data, Status, and Control
  - Byte-Oriented DMA or Programmed I/O Data Transfer
  - Interrupts System at Completion of Operation
  - Read/Write on one Drive while Seeking on another for Enhanced System Throughput
  - Three On-Chip Status Registers
  - TTL Compatible Inputs and Outputs
  - +5 Volt Only Operation
- ☐ FLOPPY DISK INTERFACE
  - Controls up to 4 Double-Sided Drives
  - Compatible with Standard (8") Floppy Disk Drives
  - Compatible with Mini-Floppy (5¼") Disk Drives

PIN CONFIGURATION



PACKAGE: 40 pin D.I.P.

GENERAL DESCRIPTION

The FDC 7003 is a 40 pin DIP COPLAMOS® n-channel depletion-load MOS/LSI device which performs the complex interface function between a processor and a Floppy Disk Drive. The FDC offers many features which reduce computer service overhead resulting in greater system throughput. For example, the controller performs track seek/verify, write and write verification without processor intervention. Enhanced system throughput is offered by the ability to seek on one drive while reading or writing on another.

The device is capable of reading, writing, and initializing diskettes in single or double density. It is compatible with both the single density and double density IBM soft-sectored formats. The FDC provides the system designer with the flexibility needed to accommodate various disk data formats. The number of bytes per sector, the number of sectors per track and the number of tracks per side are fully programmable.

The FDC interfaces to a processor via an 8-bit bi-directional three-state bus. This assures efficient data transfer and processor compatibility. Three addressable internal Status Registers provide complete status information to the processor. The processor operates upon the FDC via eight registers which are used during command execution: a Command Register, a Data Register, two Current Track Registers, a Seek Track Register, a Current Sector Register, a Sector Count Register, and a Compare Count Register. Four additional control registers permit customizing the FDC to the selected drive and modes of operation.

The following command functions are available:

Restore	Step-Out	Seek	Read Data
Step	Step-In	Track Verify	Compare Data
Write Data	Read Address	Format Track	
Write Verify	Read Track	Software Reset	

The FDC will interface to both the standard (8") floppy disk drive and the minifloppy (5¼") drive. Compatibility with the products of several manufacturers is assured by the inclusion of a wide range of programmable Track-to-Track Seek Times and Head Load Times.

The FDC requires +5 volts only and all inputs and outputs are TTL compatible.

*FOR FUTURE RELEASE

FDC 7003 REGISTER TABLE

A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
				STATUS REGISTER A							
0	0	0	0	INT	R/W DONE	SEEK DONE	INDEX DET	READY CHG	COMPARE FOUND	ILLEGAL	R/W STATUS
				STATUS REGISTER B							
0	0	0	1	WR PROT	ID RNF	DATA RNF	CRC ERROR	DATA LOST	TRACK ERROR	DATA AM1	DATA AMØ
				STATUS REGISTER C							
0	0	1	0	DXRQ	R/W BUSY	SEEK BUSY	INDEX	READY	TRACK ZERO	LDHD1	LDHDØ
0	0	1	1	**COMMAND**							
				CONTROL A							
0	1	0	0	STEP INTERVAL						SEEK LATENCY	
				CONTROL B							
0	1	0	1	HEAD UNLOAD DELAY			HEAD LOAD LATENCY				
				CONTROL C							
0	1	1	0	INT ENABLE	MFM	SEEK OVERLAP	INDEX INT ENA	READY INT ENA	SEL2	SEL1	SELØ
				CONTROL D							
0	1	1	1	HALF SPEED	RESERVED	INTERNAL PRECOMP	MODIFY TGT43	IBM LEN	GAP2 LEN	DEL DATA INT ENA	FF/4E LEN
1	0	0	0	**CURRENT TRACK Ø**							
1	0	0	1	**CURRENT TRACK 1**							
1	0	1	0	**SEEK TRACK**							
1	0	1	1	**RESERVED**							
1	1	0	0	**COMPARE COUNT**							
1	1	0	1	**SECTOR COUNT**							
1	1	1	0	SIDE	**CURRENT SECTOR**						
1	1	1	1	**DATA**							

FDC 7003 COMMAND STRUCTURE

COMMAND	COMMAND REGISTER CONTENTS D7	D6	D5	D4	D3	D2	D1	D0
RESTORE	Ø	Ø	Ø	Ø	h	v	Ø	Ø
SEEK	Ø	Ø	1	Ø	h	v	Ø	Ø
TRACK VERIFY	Ø	1	Ø	Ø	Ø	1	Ø	Ø
STEP IN	Ø	1	Ø	1	Ø	v	u	Ø
STEP OUT	Ø	1	1	Ø	Ø	v	u	Ø
STEP	Ø	1	1	1	Ø	v	u	Ø
READ DATA	1	Ø	Ø	Ø	h	m	$\overline{T}$	Ø
COMPARE DATA	1	Ø	Ø	1	h	m	Ø	Ø
WRITE DATA	1	Ø	1	Ø	h	m	a_1	a_0
WRITE VERIFY	1	Ø	1	1	h	m	a_1	a_0

COMMAND	COMMAND REGISTER CONTENTS D7	D6	D5	D4	D3	D2	D1	D0
READ TRACK DATA ONLY	1	1	Ø	Ø	Ø	Ø	Ø	Ø
READ TRACK CLK/DATA	1	1	Ø	Ø	Ø	Ø	1	Ø
FORMAT TRACK AUTO	1	1	Ø	1	Ø	Ø	Ø	Ø
FORMAT TRACK CLK/DATA	1	1	Ø	1	Ø	Ø	1	Ø
READ ADDRESS	1	1	1	Ø	Ø	Ø	S	Ø
SOFTWARE RESET	1	1	1	1	R3	R2	R1	RØ

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We keep ahead of our competition so you can keep ahead of yours.

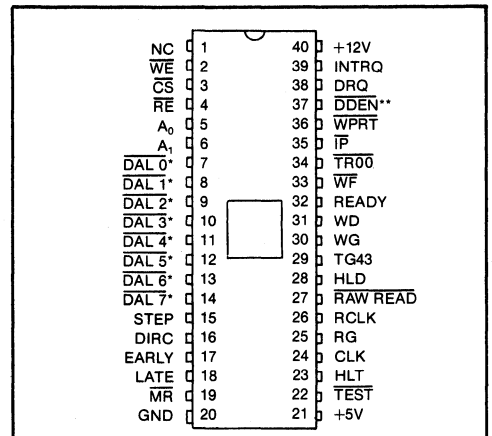
FDC 1791*
FDC 1792*
FDC 1793*
FDC 1794*
μPC FAMILY

Floppy Disk Controller/Formatter FDC

FEATURES

- ☐ SOFT SECTOR FORMAT COMPATIBILITY
- ☐ AUTOMATIC TRACK SEEK WITH VERIFICATION
- ☐ ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- ☐ READ MODE
  - Single/Multiple Record Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- ☐ WRITE MODE
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- ☐ PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers/Comprehensive Status Information
- ☐ WRITE PRECOMPENSATION (MFM AND FM)

PIN CONFIGURATION



*TRUE BUS FOR FDC 1793 and FDC 1794
**MUST BE LEFT OPEN FOR FDC 1792 and FDC 1794
PACKAGE: 40 pin D.I.P.

- ☐ WINDOW EXTENSION (IN MFM)
- ☐ INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- ☐ COMPATIBLE WITH FD1791, FD1792, FD1793, FD1794

GENERAL DESCRIPTION

The FDC 179X is an MOS/LSI device which performs the functions of a Floppy Disk Controller/Formatter in a single chip implementation. The basic FDC 179X chip design has evolved into four specific parts: FDC 1791, FDC 1792, FDC 1793 and the FDC 1794.

This FDC family performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8" and 5¼" (mini-floppy) drives with single or double density storage capabilities are supported. These n-channel MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk.

The FDC 1791 is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The FDC 1791 contains enhanced features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensate.

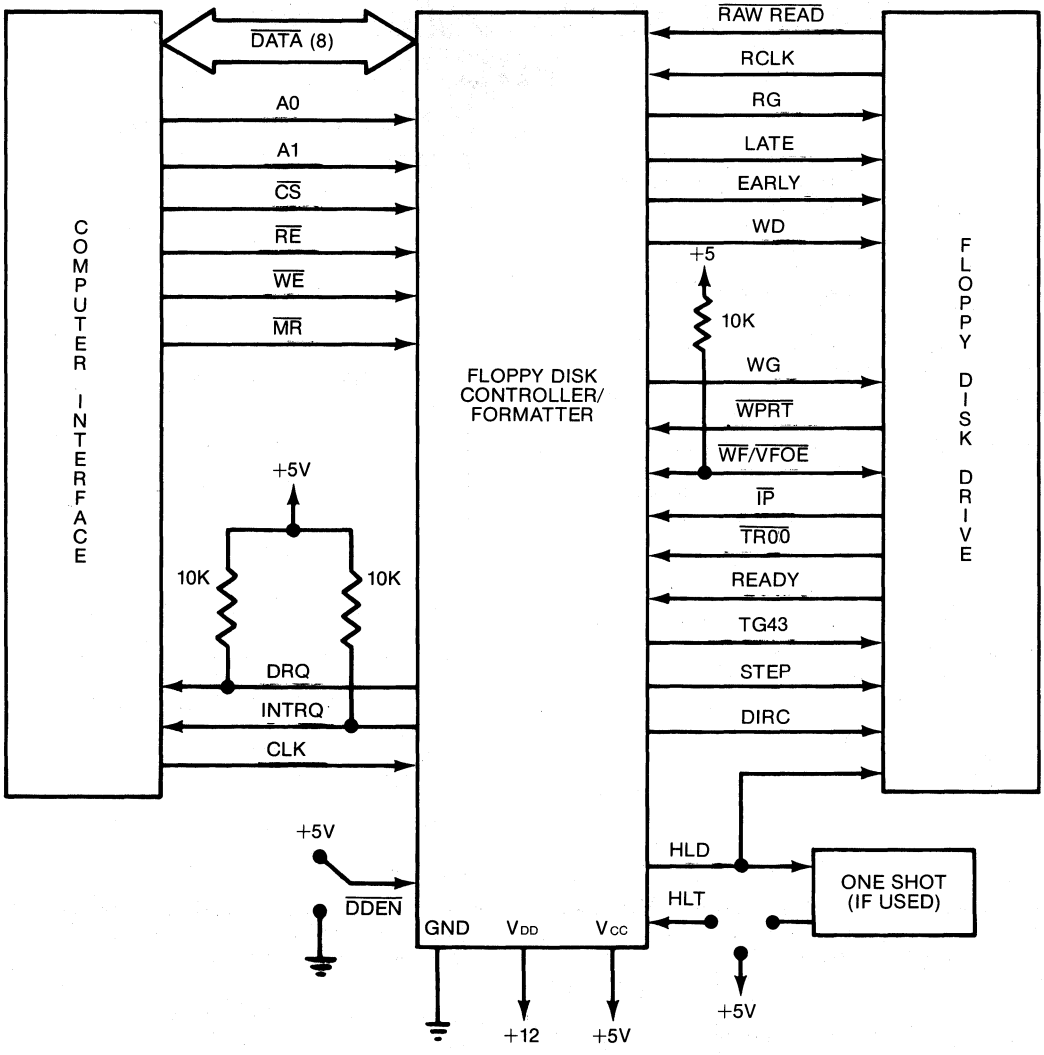
The FDC 1793 is identical to the FDC 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The FDC 1792 operates in the single density mode only. Pin 37 (DDEN) of the FDC 1792 must be left open for proper operation. The FDC 1794 is identical to the FDC 1792 except the DAL lines are TRUE for systems that utilize true data busses.

The processor interface consists of an 8 bit bidirectional bus for data, status, and control word transfers. This family of controllers is configured to operate on a multiplexed bus with other bus-oriented devices.

*FOR FUTURE RELEASE

System Block Diagram

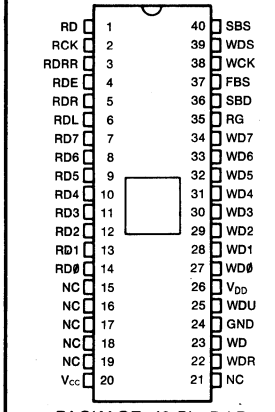


Cassette/Cartridge Data Handler CCDH

FEATURES

- ☐ Facilitates Magnetic Tape Cassette or Cartridge to Processor Interfacing
- ☐ Performs All Data Operations
- ☐ Up to 250K bps Data Transfer Rate
- ☐ Recording Code Independent
- ☐ Compatible with Standard and Mini Cassettes
- ☐ Compatible with Standard and Mini 3M-type Cartridges
- ☐ Read-While-Write Operation for Write Verification In Dual Gap Head Systems
- ☐ Programmable Sync Byte
- ☐ Internal Sync Byte Detection and Byte Framing
- ☐ Fully Double Buffered
- ☐ Data Overrun/Underrun Detection
- ☐ Tri-State Output Bus for Processor Compatibility
- ☐ TTL Compatible Inputs and Outputs

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

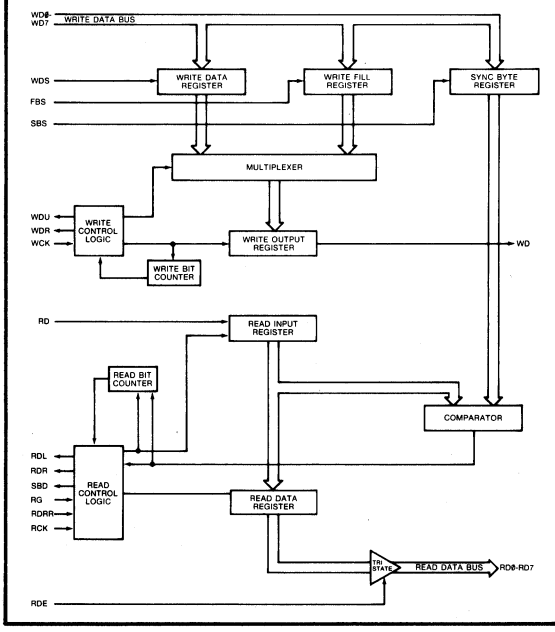
GENERAL DESCRIPTION

The CCC 3500 is an MOS integrated circuit which simplifies the data interface between a processor and a magnetic tape cassette or cartridge drive. During a write operation the CCDH receives data from the processor and shifts it out bit serially to the cassette/cartridge data encoding logic. Similarly during a read operation the CCDH receives a bit-serial stream of read data from the cassette/cartridge data recovery circuit, establishes byte synchronization by detecting the sync byte, and transfers data on a byte by byte basis to the processor.

The CCDH detects data overrun and underrun conditions and indicates these conditions on its status lines. A data underrun causes data from a special programmable fill register to be written onto the cassette/cartridge until new data is entered into the write data buffer or until the write operation is ended.

Separate read and write data registers permit simultaneous read and write operations. Drives with dual gap heads may utilize this read-while-write feature for write data verification thereby enhancing system throughput and reliability. The CCDH is fully double buffered and all inputs and outputs are TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



SECTION VIII

DESCRIPTION OF OPERATION

Write Operation

After power-on, the Write Clock is set at the desired bit rate and the desired fill byte is written into the Write Fill Register. After the external control logic has caused the tape to come up to operating speed and activated the write enable signal, the first byte to be written should be loaded into the Write Data Register. This byte is then loaded into the Write Output Register and shifted out bit serially to the external write encoding logic. The first bit shifted out of each byte is the LSB. Whenever a byte is transferred from the Write Data Register to the Write Output Register, Write Data Request becomes active and requests another byte from the processor. If new data is not loaded into the Write Data Register before the Write Output Register becomes empty, then the Write Output Register is loaded with data from the Write Fill Register and the Write Data Underrun status line is set. WDU is reset the next time WDS is pulsed. At the end of the write operation, the processor should return the external write enable line to an inactive state.

Read Operation

After power-on, the desired sync byte is loaded into the Sync Byte Register. After the external control logic has initiated forward motion and the tape has come up to operating speed, the processor produces a positive-to-negative transition on the Read Gate input to set the read logic into the sync byte search mode. In the search mode the serial read data bit stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found, by definition, when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the Sync Byte Detected output is set high. This byte is then loaded into the Read Data Register and the read logic is set into the byte mode. In this mode each byte read is loaded into the Read Data Register and Read Data Request is made active high for each byte. The processor responds to each Read Data Request by enabling the output bus with Read Data Enable, reading the data byte from the Read Data Register, and resetting Read Data Request by pulsing Read Data Request Reset. If the processor fails to respond to Read Data Request within one byte time, the Read Data Lost status line is set. When the processor has read the required amount of data it may reset Read Gate to an inactive-high level and stop tape motion.

System Operation — Additional Features

Automatic Block Fill

In some applications, such as the end of a logical file, the system buffer may contain less than a full block of data. In this case the processor need supply only this data to the CCC 3500. The CCC 3500 will then underrun, setting the Write Data Underrun Status line and thereby causing the remainder of the block to fill with bytes taken from the Write Fill Register. This operation continues until the processor returns the drive's write enable signal to an inactive level.

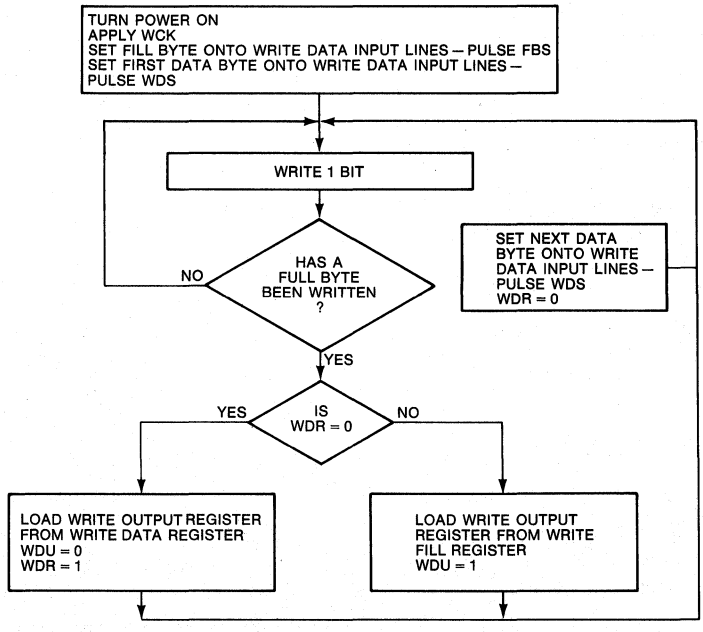
Byte Search

After byte synchronization has been established during a read operation, the processor may load a different byte into the Sync Byte Register. Whenever that byte occurs in the data being read, the Sync Byte Detected status line will go high. This feature permits the processor to search for the occurrence of a specific byte while reading a block.

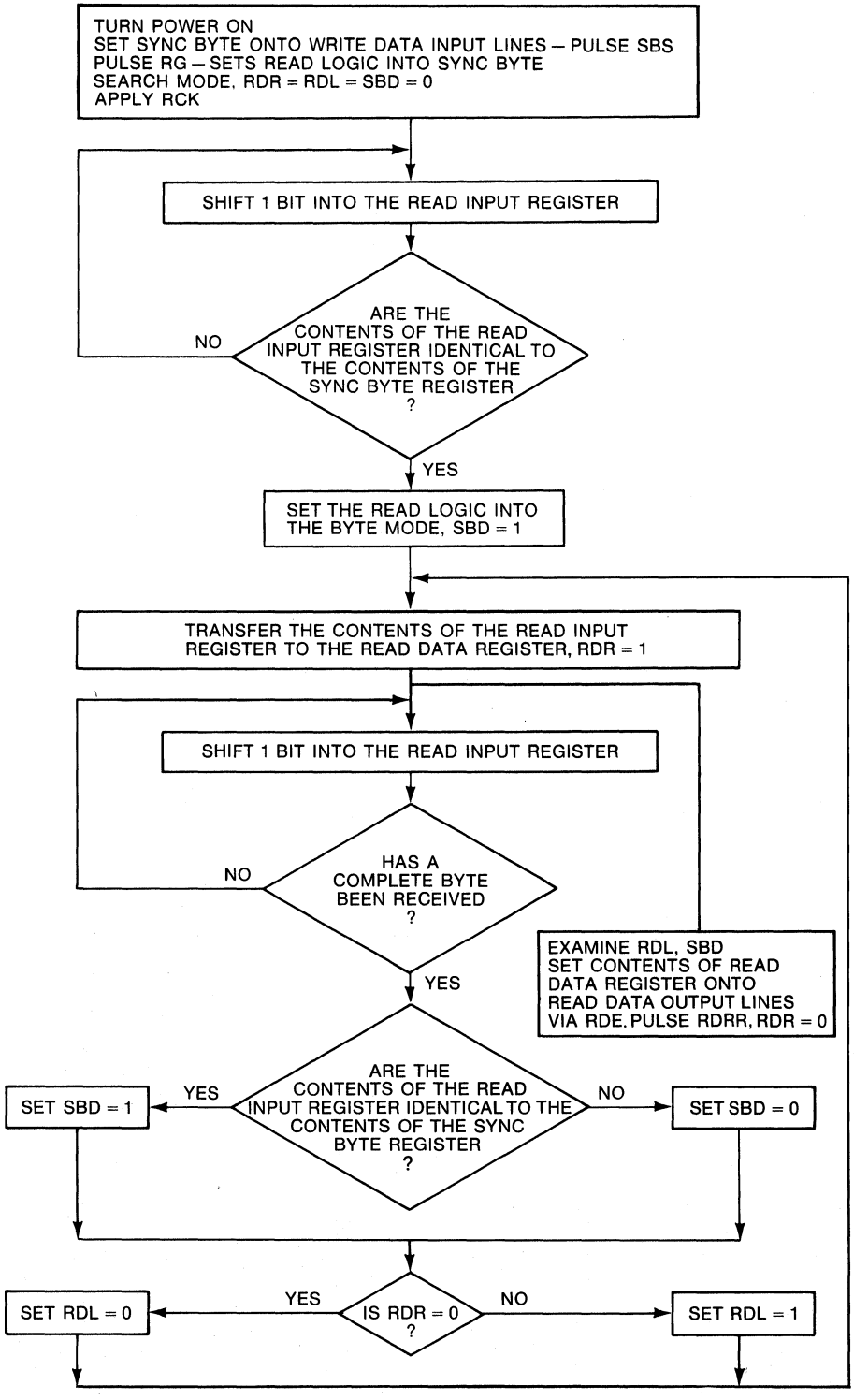
Multiple Byte Synchronization

Some systems use two or more contiguous sync bytes to establish byte synchronization. For these applications, the number of Read Data Requests received while Sync Byte Detected remains active-high may be counted by the processor to establish valid synchronization.

FLOW DIAGRAM — WRITE DATA



FLOW DIAGRAM — READ DATA



DESCRIPTION OF PIN FUNCTIONS

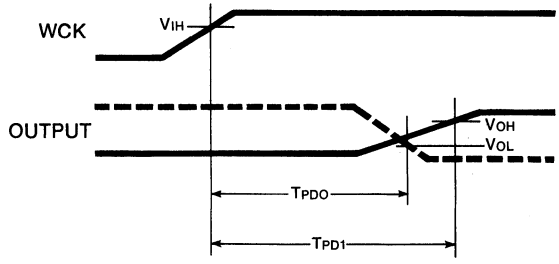
PIN NO.	SYMBOL	NAME	FUNCTION
1	RD	Read Data	The Read Data input accepts the serial data stream from the cassette/cartridge data recovery circuit.
2	RCK	Read Clock	The negative-going edge of the Read Clock input shifts Read Data into the Read Input Register.
3	RDRR	Read Data Request Reset	An active-high pulse input on the Read Data Request Reset input resets the RDR output to a low level.
4	RDE	Read Data Enable	An active-high level on the Read Data Enable line gates the outputs of the Read Data Register onto the Read Data Output lines.
5	RDR	Read Data Request	The Read Data Request output is made active-high when an assembled byte is transferred from the Read Input Register to the Read Data Register.
6	RDL	Read Data Lost	The Read Data Lost output is made active-high, if the byte presently in the Read Data Register is not read (RDR not reset) by the processor before the next byte is loaded into the Read Data Register.
7-14	RD7-RDØ	Read Data Output	When enabled by RDE the tri-state Read Data Output lines present the data in the Read Data Register to the processor. When RDE is inactive-low the RD7-RDØ lines are held at a high-impedance state.
15-19	NC		Not Connected
20	V_{CC}	Power Supply	+5 volt supply
21	NC		Not Connected
22	WDR	Write Data Request	The Write Data Request output is made active-high when the Write Data Register becomes empty and requires a data byte. It is reset to a low level when WDS occurs to load the Write Data Register. If WDR is not serviced by the time the next byte is required by the Write Output Register, the byte stored in the Write Fill Register is written onto the cassette/cartridge and the WDU line is made active high.
23	WD	Write Data	The Write Data output presents the serial stream of data to the external write data encoder. Each byte is normally provided from the Write Data Register provided that a WDS pulse occurs during the presently written byte. If WDS is not pulsed, the next byte to be written will be extracted from the Write Fill Register.
24	GND	Ground	Ground
25	WDU	Write Data Underrun	The Write Data Underrun output is set active-high when the processor fails to respond to the WDR signal within one byte time. When WDU occurs the data written on the disk is extracted from the Write Fill Register. This line is reset when WDS is pulsed.
26	V_{DD}	Power Supply	−12 volt supply
27-34	WDØ-WD7	Write Data Input	The Write Data Input lines present information to the Write Data Register, the Write Fill Register, and the Sync Byte Register under control of their respective strobes. The strobes operate independently of each other. The LSB should always be placed on WDØ.
35	RG	Read Gate	This input should be pulsed to a high-level after power turn on to reset RDR, SBD, and RDL to an inactive-low level. The high-to-low transition of RG sets the read logic into the sync byte search mode. In this mode the serial Read Data stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found by definition when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the SBD output is set active-high. The sync byte just read is then transferred into the Read Data Register; RDR is set high, and the read logic is set into the byte mode. In this mode each byte read is transferred into the Read Data Register.
36	SBD	Sync Byte Detected	The Sync Byte Detected output is set active-high each time the byte loaded into the Read Data Register is identical to the byte in the Sync Byte Register. This output is reset low the next time the Read Data Register is loaded with a byte which is not a sync byte.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
37	FBS	Fill Byte Strobe	The Fill Byte Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Write Fill Register.
38	WCK	Write Clock	Each positive-going edge of this clock shifts one bit out of the Write Output Register onto WD.
39	WDS	Write Data Strobe	The Write Data Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Write Data Register.
40	SBS	Sync Byte Strobe	The Sync Byte Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Sync Byte Register.

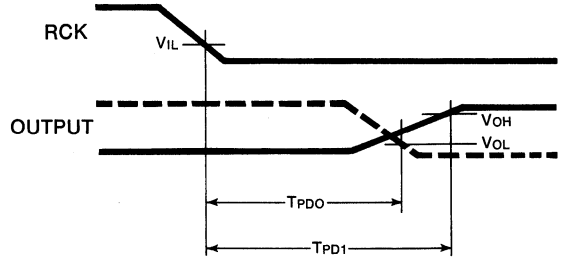
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

WRITE DATA

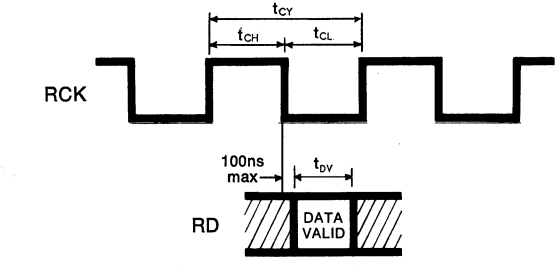


OUTPUT	T_{PDO}	T_{PD1}	UNITS
WDR	NA	2.0	µS
WDU	1.0	1.5	µS
WD	1.0	1.0	µS

READ DATA



OUTPUT	T_{PDO}	T_{PD1}	UNITS
RDR	NA	1.5	µS
RDL	2.0	2.5	µS
SBD	2.0	2.5	µS
RDØ-RD7	2.5	2.5	µS



MIN. TIMING	CCC 3500	UNITS
t_{CY}	4.0	µS
t_{CH}	1.0	µS
t_{CL}	2.0	µS
t_{DV}	1.4	µS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Load Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

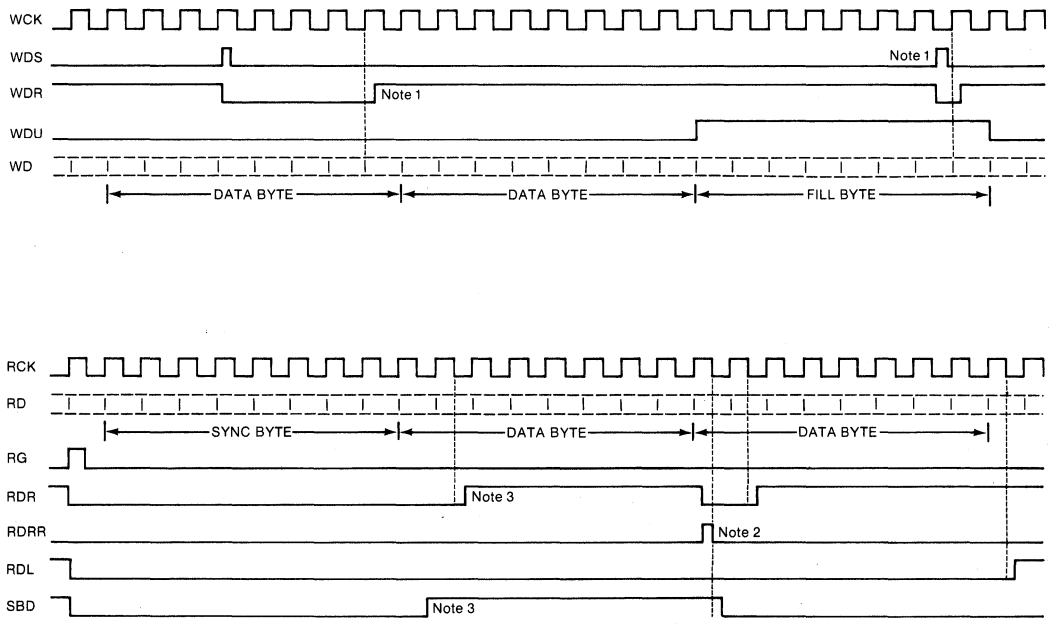
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5% V_{DD} = −12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = −100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	See note 1
OUTPUT CURRENT					
Leakage, I_{LO}			-1	μA	RDE = V_{IL}, 0 ≤ V_{OUT} ≤ +5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pF	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pF	RDE = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}
I_{DD}			28	mA	
A.C. CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY	DC		250	KHz	RCK, WCK
PULSE WIDTH					
Clock	1			μs	RCK, WCK
Read Gate	1			μs	RG
Write Data Strobe	200			ns	WDS
Fill Byte Strobe	200			ns	FBS
Sync Byte Strobe	200			ns	SBS
Read Data Request Reset	200			ns	RDRR
INPUT SET-UP TIME					
Write Data Inputs	0			ns	WDØ-WD7
INPUT HOLD TIME					
Write Data Inputs	0			ns	WDØ-WD7
STROBE TO OUTPUT DELAY					Load = 20pf + 1 TTL input
Read Data Enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

**Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing.
   A switching current of 1.6mA maximum flows during a high to low transition of the input.
2. The tri-state output has 3 states:
   1) low-impedance to V_{CC}
   2) low-impedance to GND
   3) high-impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.

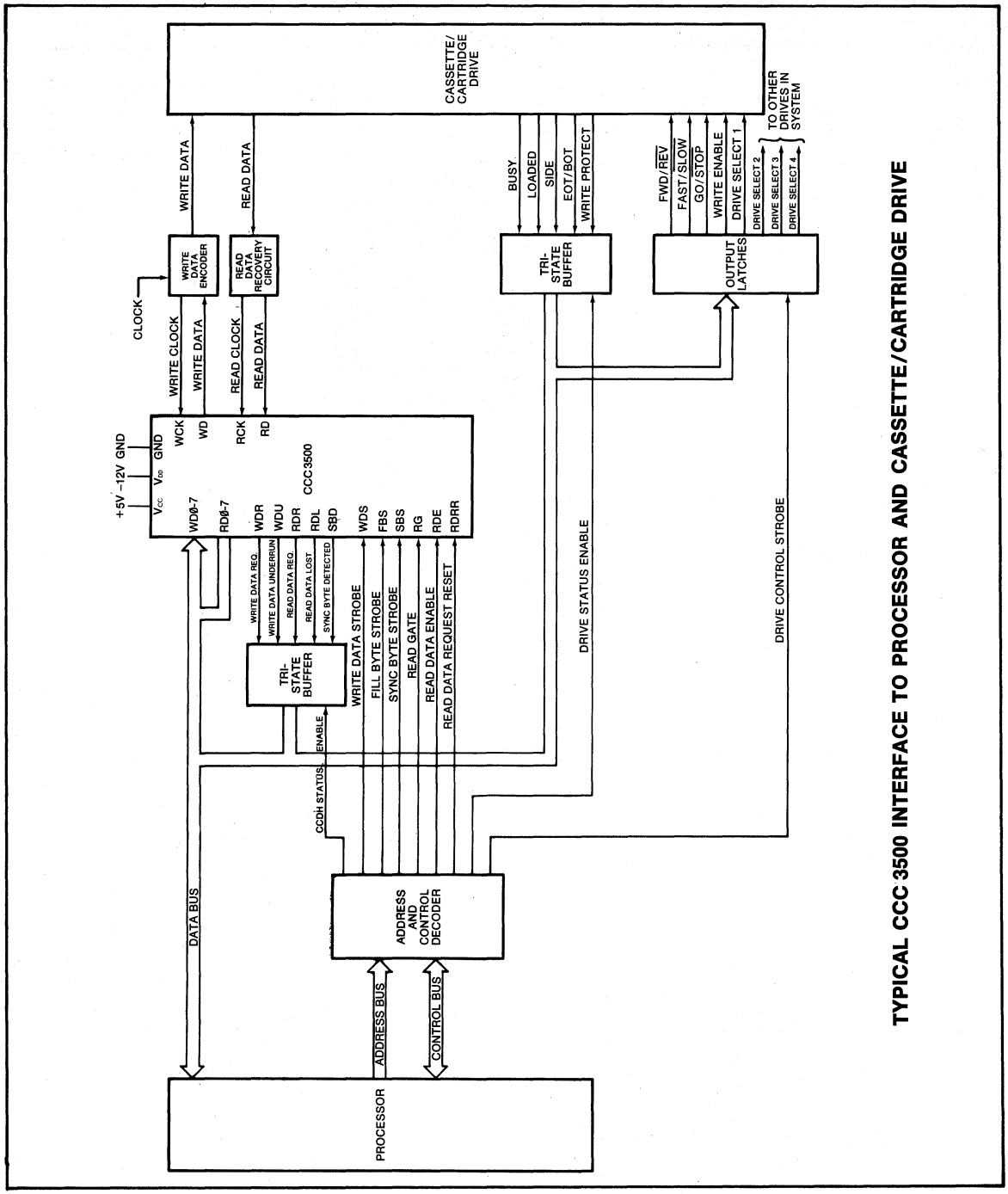
CCDH TIMING DIAGRAM



NOTE 1
The Write Output Register is loaded with the next byte at the positive clock transition corresponding to the leading edge of the last bit of the current byte on the WD output. WDR is set high approximately two microseconds after this clock transition. If it is desired that the next byte be extracted from the Write Data Register the leading edge of the WDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an RDL indication the leading edge of the RDRR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input.

NOTE 3
The RDL, SBD and RD0-RD7 output are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input. The RDR output is set high at the next negative clock transition.

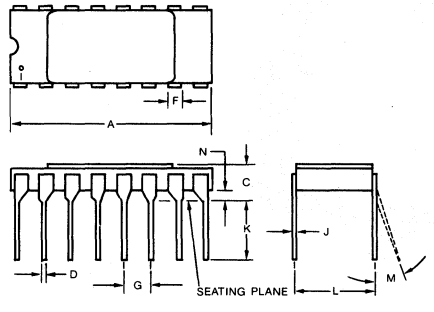


TYPICAL CCC 3500 INTERFACE TO PROCESSOR AND CASSETTE/CARTRIDGE DRIVE

SECTION VIII

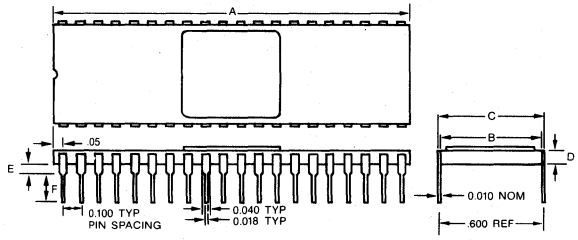
Package Outlines

14, 16, 18, 20 PIN HERMETIC PACKAGE

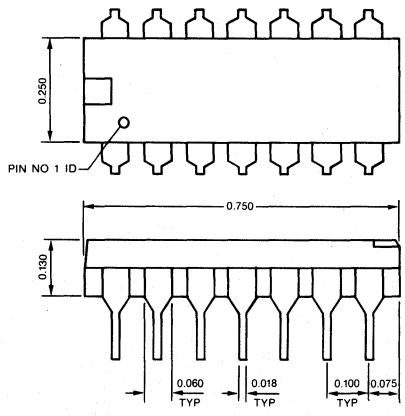


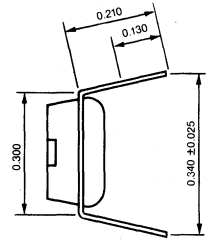
DIM	14 LEAD		16 LEAD		18 LEAD		20 LEAD	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.670	.760	.790	.810	.885	.915	.965	.995
C		.175		.175		.175		.175
D	.015	.021	.015	.021	.015	.021	.015	.021
F	.048	.060	.048	.060	.048	.060	.048	.060
G	.090	.110	.090	.110	.090	.110	.090	.110
J	.008	.012	.008	.012	.008	.012	.008	.012
K	.100		.100		.100		.100	
L	.295	.325	.295	.325	.295	.325	.295	.325
M		10°		10°		10°		10°
N	.025	.060	.025	.060	.025	.060	.025	.060

24, 28, 40 LEAD HERMETIC DIP



DIM	24 LEAD		28 LEAD		40 LEAD	
	MIN	MAX	MIN	MAX	MIN	MAX
A	1.188	1.212	1.386	1.414	1.980	2.020
B	.568	.598	.568	.598	.568	.598
C	.590	.610	.590	.610	.590	.610
D	.070	.090	.070	.090	.070	.090
E	.025	.060	.025	.060	.025	.060
F	.100		.100		.100	

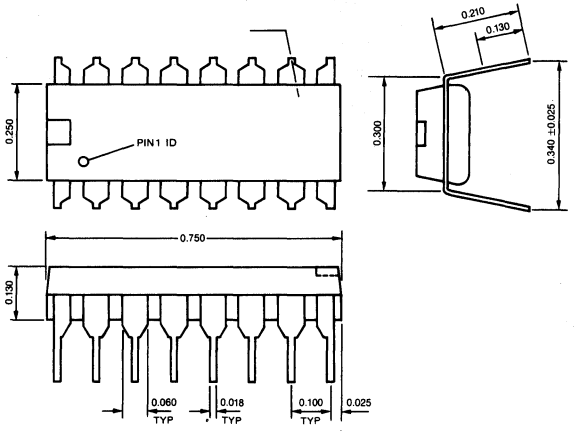




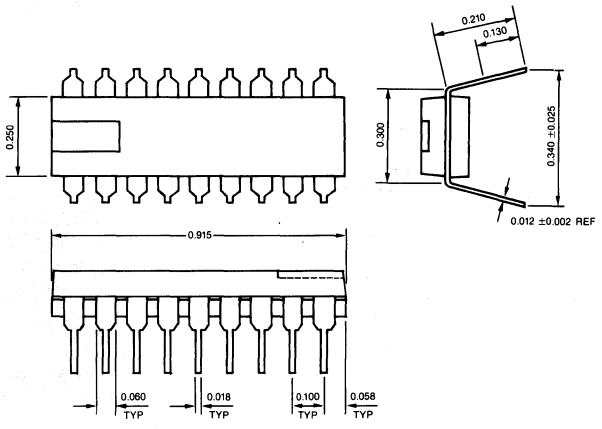
14 LEAD PLASTIC DIP

ALL UNITS INCHES UNLESS OTHERWISE SPECIFIED

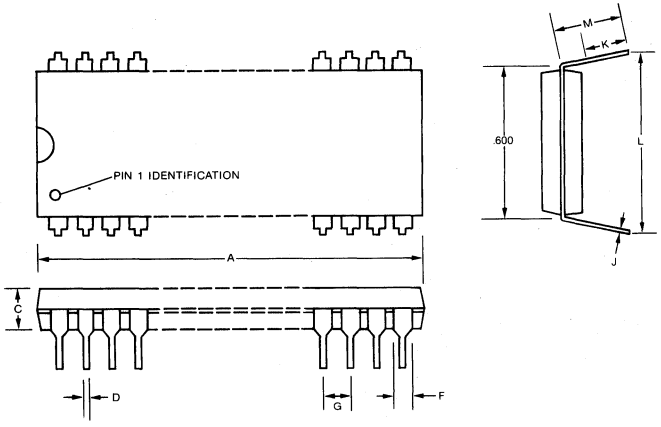
16 LEAD PLASTIC DIP



18 LEAD PLASTIC DIP



24, 28, 40 PIN PLASTIC DIP



DIM	24 LEAD		28 LEAD		40 LEAD	
	MIN	MAX	MIN	MAX	MIN	MAX
A	1.245	1.255	1.445	1.455	2.045	2.055
C	.145	.155	.145	.155	.145	.155
D	.018 TYP		.018 TYP		.018 TYP	
F	.060 TYP		.060 TYP		.060 TYP	
G	.099	.101	.099	.101	.099	.101
J	.010	.014	.010	.014	.010	.014
K	.120		.120		.120	
L	.645	.675	.645	.675	.645	.675
M	.210		.210		.210	

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