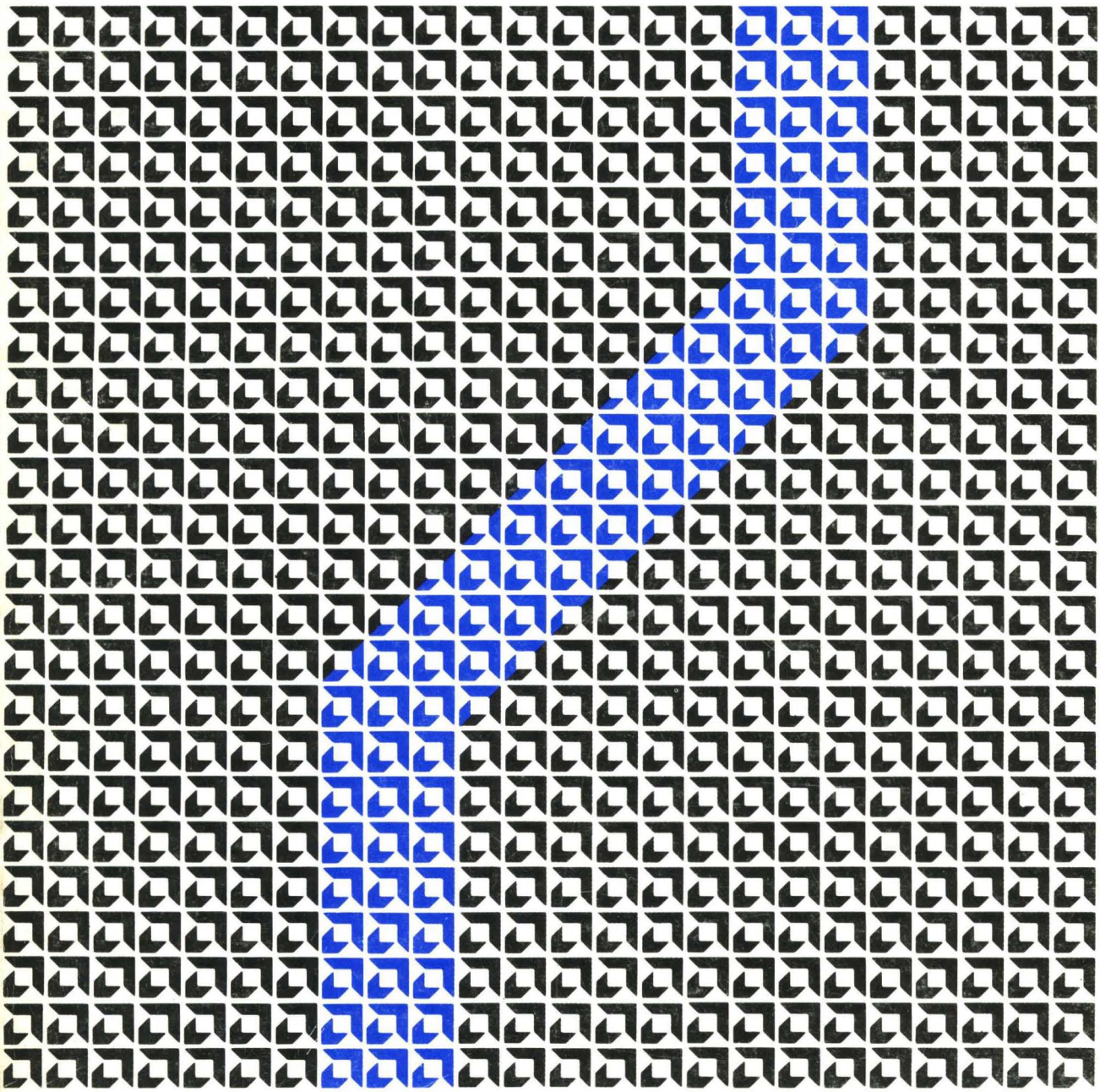
Advanced Micro Devices

Bipolar/MOS Memories Data Book



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Advanced Micro Devices

Bipolar/MOS Memories Data Book

The International Standard of Quality guarantees these electrical AQLs on all parameters over the operating temperature range: 0.1% on MOS RAMs & ROMs; 0.2% on Bipolar Logic & Interface; 0.3% on Linear, LSI & Logic & other memories.

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IMOX is a trademark of Advanced Micro Devices.

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Bipolar PROM

Functional Index and Selection Guide

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Part Number	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages	Comments	Page No.
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Am27PS43	4096 x 8	N.A.	N.A.	3S	24	D, P, F, L	Power switched	–
Am27S45	2048 x 8	N.A.[2]	185/185	3S	24	D, P, L	Output registers, asynchronous initialize, THINDIP Pkg[3]	2-116
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Am27S47	2048 x 8	N.A.[2]	185/185	3S	24	D, P, L	Output registers, synchronous initialize, THINDIP Pkg[3]	2-116
Am27S47A	2048 x 8	N.A.[4]	185/185	3S	24	D, P, L	Ultra fast, output registers, synchronous initialize, THINDIP Pkg[3]	2-116

Notes: 1. Replaces Am27LS08/09
2. Contains built-in pipeline registers: nominal address to clock setup time = 35ns (typ), clock to output = 20ns (typ).
3. 300-mil lateral pin spacing.
4. Contains built-in pipeline registers: nominal address to clock setup time = 25ns (typ), clock to output = 15ns (typ).
5. I_{CC} are power up and power down current limits respectively.

Bipolar Memory RAM

Functional Index and Selection Guide

BIPOLAR ECL RAM

Part Number	Organization	Access Time COML/MIL Max	I_{EE} COML/MIL Max	ECL Series	Number of Pins	Packages	Comments	Page No.
Am10415SA	1024 x 1	15/20	−150/−165	10K	16	D, P, F, L		3-62
Am10415A	1024 x 1	20/25	−150/−165	10K	16	D, P, F, L		3-62
Am10415	1024 x 1	35/40	−150/−165	10K	16	D, P, F, L		3-62
Am100415A	1024 x 1	15/−	−150/−	100K	16	D, P, F, L		3-69
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Am10470SA	4096 x 1	15/20	−230/−255	10K	18	D, F[1], L		3-76
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Am10470	4096 x 1	35/40	−200/−220	10K	18	D, F[1], L		3-76
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Am100470A	4096 x 1	25/−	−195/−	100K	18	D, F[1], L		3-83
Am100470	4096 x 1	35/−	−195/−	100K	18	D, F[1], L		3-83
Am10474A	1024 x 4	15/20	−230/−255	10K	24	D, F, L		3-74
Am10474	1024 x 4	25/30	−230/−220	10K	24	D, F, L		3-74
Am100474A	1024 x 4	15/−	−230/−	100K	24	D, F, L		3-75
Am100474	1024 x 4	25/−	−200/−	100K	24	D, F, L		3-75

Note: 1. For flat package consult factory.

BIPOLAR TTL RAM

Part Number	Organization	Access Time COML/MIL Max	I_{CC} COML/MIL Max	Output	Number of Pins	Packages (Note 1)	Comments	Page No.
Am27S02A	16 x 4	25/30	100/105	OC	16	D, P, F, L	Ultra Fast	3-1
Am27S03A	16 x 4	25/30	100/105	3S	16	D, P, F, L		3-1
Am27S02	16 x 4	35/50	105/105	OC	16	D, P, F, L		3-1
Am27S03	16 x 4	35/50	125/125	3S	16	D, P, F, L		3-1
Am27LS02	16 x 4	55/65	35/38	OC	16	D, P, F, L	Low Power	3-7
Am27LS03	16 x 4	55/65	35/38	3S	16	D, P, F, L		3-7
Am74/54S289	16 x 4	35/50	105/105	OC	16	D, P, F, L		3-16
Am74/54S189	16 x 4	35/50	125/125	3S	16	D, P, F, L		3-16
Am27S06A	16 x 4	25/30	100/105	OC	16	D, P, F, L	Noninverting Outputs	3-26
Am27S07A	16 x 4	25/30	100/105	3S	16	D, P, F, L		3-26
Am27S06	16 x 4	35/50	100/105	OC	16	D, P, F, L		3-26
Am27S07	16 x 4	35/50	100/105	3S	16	D, P, F, L		3-26
Am27LS06	16 x 4	55/65	35/38	OC	16	D, P, F, L	Noninverting Outputs, Low Power	3-32
Am27LS07	16 x 4	55/65	35/38	3S	16	D, P, F, L		3-32
Am3101A	16 x 4	35/50	100/105	OC	16	D, P, F, L		3-16
Am3101-1	16 x 4	35/50	100/105	OC	16	D, P, F, L	Write Transparent[2]	3-11
Am3101	16 x 4	50/60	100/105	OC	16	D, P, F, L		3-11

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

BIPOLAR TTL RAM (Cont.)

Part Number	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages (Note 1)	Comments	Page No.
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Am74/5489-1	16 x 4	35/50	100/105	OC	16	D, P, F, L	Write Transparent[2]	3-11
Am74/5489	16 x 4	50/60	100/105	OC	16	D, P, F, L		3-11
Am27LS00A	256 x 1	35/45	115/115	3S	16	D, P, F, L	Ultra Fast	3-36
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Am27LS00	256 x 1	45/55	70/70	3S	16	D, P, F, L	Fast, Low Power	3-36
Am27LS01	256 x 1	45/55	70/70	OC	16	D, P, F, L		3-36
Am27LS00-1A	256 x 1	35/45	115/115	3S	16	D, P, F, L	Noninverting Outputs	3-42
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Am27LS00-1	256 x 1	45/55	70/70	3S	16	D, P, F, L		3-42
Am27LS01-1	256 x 1	45/55	70/70	OC	16	D, P, F, L		3-42
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Am93425	1024 x 1	45/65	155/170	3S	16	D, P, F, L		3-57
Am93412A	256 x 4	35/45	155/170	OC	22[3]	D, P, F, L	Ultra Fast	3-47
Am93422A	256 x 4	35/45	155/170	3S	22[3]	D, P, F, L		3-47
Am93412	256 x 4	45/60	155/170	OC	22[3]	D, P, F, L		3-47
Am93422	256 x 4	45/60	155/170	3S	22[3]	D, P, F, L		3-47
Am93L412A	256 x 4	45/55	80/90	OC	22[3]	D, P, F, L	Low Power	3-52
Am93L422A	256 x 4	45/55	80/90	3S	22[3]	D, P, F, L		3-52
Am93L412	256 x 4	60/75	80/90	OC	22[3]	D, P, F, L		3-52
Am93L422	256 x 4	60/75	80/90	3S	22[3]	D, P, F, L		3-52

Notes: 1. D = Hermetic DIP, P = Molded DIP, F = Cerpak, L = Chip-Pak™.
2. Complement of data in is available on the outputs in the write mode when both $\overline{CS}$ and $\overline{WE}$ are low.
3. Cerpak (F) is 24 pin.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MOS Memory

1K STATIC RAMs

Functional Index and Selection Guide

Part Number	Organization	Access Time (ns)	Power Dissipation (mW) Standby	Active	Pins	Supply Voltage (V)	Temp Range	Package	Page No.
Am9101A	256 x 4	500	47	290	22	5	C, M	D, P	4-1
Am91L01A	256 x 4	500	38	173	22	5	C, M	D, P	4-1
Am9101B	256 x 4	400	47	290	22	5	C, M	D, P	4-1
Am91L01B	256 x 4	400	38	173	22	5	C, M	D, P	4-1
Am9101C	256 x 4	300	47	315	22	5	C, M	D, P	4-1
Am91L01C	256 x 4	300	38	189	22	5	C, M	D, P	4-1
Am9101D	256 x 4	250	47	315	22	5	C	D, P	4-1
Am9111A	256 x 4	500	47	290	18	5	C, M	D, P	4-7
Am91L11A	256 x 4	500	38	173	18	5	C, M	D, P	4-7
Am9111B	256 x 4	400	47	290	18	5	C, M	D, P	4-7
Am91L11B	256 x 4	400	38	173	18	5	C, M	D, P	4-7
Am9111C	256 x 4	300	47	315	18	5	C, M	D, P	4-7
Am91L11C	256 x 4	300	38	189	18	5	C, M	D, P	4-7
Am9111D	256 x 4	250	47	315	18	5	C	D, P	4-7
Am9112A	256 x 4	500	47	290	16	5	C, M	D, P	4-13
Am91L12A	256 x 4	500	38	173	16	5	C, M	D, P	4-13
Am9112B	256 x 4	400	47	290	16	5	C, M	D, P	4-13
Am91L12B	256 x 4	400	38	173	16	5	C, M	D, P	4-13
Am9112C	256 x 4	300	47	315	16	5	C, M	D, P	4-13
Am91L12C	256 x 4	300	38	189	16	5	C, M	D, P	4-13
Am9112D	256 x 4	250	47	315	16	5	C	D, P	4-13
Am9122-25	256 x 4	25	–	660	22	5	C	D, P	4-19
Am9122-35	256 x 4	35	–	660	22	5	C, M	D, P	4-19
Am91L22-35	256 x 4	35	–	440	22	5	C	D, P	4-19
Am91L22-45	256 x 4	45	–	440	22	5	C, M	D, P	4-19
Am91L22-60	256 x 4	60	–	248	22	5	C	D, P	4-19

4K STATIC RAMs

Am21L41-12	4096 x 1	120	25	200	18	5	C	D, P	4-25
Am21L41-15	4096 x 1	150	25	200	18	5	C	D, P	4-25
Am21L41-20	4096 x 1	200	25	200	18	5	C	D, P	4-25
Am21L41-25	4096 x 1	250	25	250	18	5	C	D, P	4-25
Am9044B	4096 x 1	450		350	18	5	C, M	D, P	4-31
Am90L44B	4096 x 1	450		250	18	5	C, M	D, P	4-31
Am9044C	4096 x 1	300		350	18	5	C, M	D, P	4-31
Am90L44C	4096 x 1	300		250	18	5	C, M	D, P	4-31
Am9044D	4096 x 1	250		350	18	5	C, M	D, P	4-31
Am90L44D	4096 x 1	250		250	18	5	C, M	D, P	4-31
Am9044E	4096 x 1	200		350	18	5	C	D, P	4-31
Am90L44E	4096 x 1	200		250	18	5	C	D, P	4-31
Am9244B	4096 x 1	450	150	350	18	5	C, M	D, P	4-31
Am92L44B	4096 x 1	450	100	250	18	5	C, M	D, P	4-31
Am9244C	4096 x 1	300	150	350	18	5	C, M	D, P	4-31
Am92L44C	4096 x 1	300	100	250	18	5	C, M	D, P	4-31
Am9244D	4096 x 1	250	150	350	18	5	C, M	D, P	4-31
Am92L44D	4096 x 1	250	100	250	18	5	C, M	D, P	4-31
Am9244E	4096 x 1	200	150	350	18	5	C	D, P	4-31
Am92L44E	4096 x 1	200	100	250	18	5	C	D, P	4-31
Am9114B	1024 x 4	450		350	18	5	C, M	D, P, F	4-35
Am91L14B	1024 x 4	450		250	18	5	C, M	D, P, F	4-35
Am9114C	1024 x 4	300		350	18	5	C, M	D, P, F	4-35
Am91L14C	1024 x 4	300		250	18	5	C, M	D, P, F	4-35
Am9114E	1024 x 4	200		350	18	5	C, M	D, P	4-35
Am91L14E	1024 x 4	200		250	18	5	C	D, P	4-35
Am9124B	1024 x 4	450	150	350	18	5	C, M	D, P, F	4-35
Am91L24B	1024 x 4	450	100	250	18	5	C, M	D, P, F	4-35
Am9124C	1024 x 4	300	150	350	18	5	C, M	D, P, F	4-35
Am91L24C	1024 x 4	300	100	250	18	5	C, M	D, P, F	4-35

4K STATIC RAMs (Cont.)

Part Number	Organization	Access Time (ns)	Power Dissipation (mW) Standby	Active	Pins	Supply Voltage (V)	Temp. Range	Package	Page No.
Am2147-35	4096 x 1	35	165	990	18	5	C	D	4-39
Am2147-45	4096 x 1	45	165	990	18	5	M	D, L	4-39
Am2147-55	4096 x 1	55	165	990	18	5	C, M	D, L	4-39
Am2147-70	4096 x 1	70	110	880	18	5	C, M	D, L	4-39
Am21L47-45	4096 x 1	45	83	688	18	5	C	D	4-39
Am21L47-55	4096 x 1	55	83	688	18	5	C	D	4-39
Am2148-55	1024 x 4	55	165	990	18	5	C, M	D, L	4-45
Am2148-70	1024 x 4	70	165	990	18	5	C, M	D, L	4-45
Am2149-55	1024 x 4	55	–	990	18	5	C, M	D, L	4-45
Am2149-70	1024 x 4	70	–	990	18	5	C, M	D, L	4-45

16K STATIC RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation (mW) Standby	Active	Pins	Supply Voltage (V)	Temp Range	Package	Page No.
Am9128-10	2048 x 8	100	83	660	24	5	C	D, P	4-51
Am9128-15	2048 x 8	150	83	550	24	5	C, M	D, P	4-51
Am9128-20	2048 x 8	200	165	660	24	5	C, M	D, P	4-51
Am9128-70*	2048 x 8	70	165	770	24	5	C	D, P	4-51
Am9167-45*	16384 x 1	45	165	660	20	5	C	D	4-57
Am9167-55*	16384 x 1	55	165	660	20	5	C, M	D	4-57
Am9168-45*	4096 x 4	45	165	660	20	5	C	D	4-58
Am9168-55*	4096 x 4	55	165	660	20	5	C, M	D	4-58

*Available in 1983.

DYNAMIC RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation (mW) Standby	Active	Pins	Supply Voltage (V)	Temp Range	Package	Page No.
Am9016C	16384 x 1	300	20	420	16	+12 ±5	C, L	P, D, L	4-59
Am9016D	16384 x 1	250	20	420	16	+12 ±5	C, L	P, D, L	4-59
Am9016E	16384 x 1	200	20	420	16	+12 ±5	C, L	P, D, L	4-59
Am9016F	16384 x 1	150	20	420	16	+12 ±5	C	P, D, L	4-59

ROMs

Part Number	Organization	Access Time (ns)	Temp Range	Supply Voltage	Pins	Operating Power Max (mW)	Outputs	Page No.
8316E	2048 x 8	450	C, M	+5	24	499	3-State	5-1
Am9218B	2048 x 8	450	C, M	+5	24	368	3-State	5-1
Am9218C	2048 x 8	350	C	+5	24	368	3-State	5-1
Am9232B	4096 x 8	450	C, M	+5	24	420	3-State	5-4
Am9232C	4096 x 8	300	C	+5	24	420	3-State	5-4
Am9232D	4096 x 8	250	C	+5	24	420	3-State	5-4
Am9233B	4096 x 8	450	C, M	+5	24	420	3-State	5-4
Am9233C	4096 x 8	300	C	+5	24	420	3-State	5-4
Am9233D	4096 x 8	250	C	+5	24	420	3-State	5-4
Am9264B	8192 x 8	450	C, M	+5	24	440	3-State	5-8
Am9264C	8192 x 8	300	C	+5	24	440	3-State	5-8
Am9264D	8192 x 8	250	C	+5	24	440	3-State	5-8
Am9265B	8192 x 8	450	C, M	+5	28	440, 110[1]	3-State	5-12
Am9265C	8192 x 8	300	C	+5	28	440, 110[1]	3-State	5-12
Am9265D	8192 x 8	250	C	+5	28	440, 110[1]	3-State	5-12
Am92128B	16384 x 8	450	C, M	+5	28	440, 137[1]	3-State	5-15
Am92128C	16384 x 8	300	C	+5	28	440, 137[1]	3-State	5-15
Am92128D	16384 x 8	250	C	+5	28	440, 137[1]	3-State	5-15
Am92256B	32768 x 8	450	C	+5	28	660, 165[1]	3-State	5-18
Am92256C	32768 x 8	300	C	+5	28	660, 165[1]	3-State	5-18
Am92256D	32768 x 8	250	C	+5	28	660, 165[1]	3-State	5-18

Note: 1. Standby

U.V. ERASABLE PROMs

Part Number	Organization	Access Time (ns)	Temp Range	Operating Power – Act/Stby Max (mW)	Supply Voltages	Outputs	Number of Pins	Page No.
Am1702A	256 x 8	1000	C, L	676	−9, +5	3-State	24	6-1
Am1702AL	256 x 8	1000	C, L	–	−9, +5	3-State	24	6-1
Am1702A-1	256 x 8	550	C, L	676	−9, +5	3-State	24	6-1
Am1702AL-1	256 x 8	550	C, L	–	−9, +5	3-State	24	6-1
Am1702A-2	256 x 8	650	C, L	676	−9, +5	3-State	24	6-1
Am1702AL-2	256 x 8	650	C, L	–	−9, +5	3-State	24	6-1
Am2708/9708	1024 x 8	450/480	C, M	800	+5, +12, −5	3-State	24	6-7
Am2708-1	1024 x 8	350	C	800	+5, +12, −5	3-State	24	6-7
Am2716	2048 x 8	450	C, I, L, M	525/132	+5	3-State	24	6-11
Am9716	2048 x 8	300	C	525/132	+5	3-State	24	6-11
Am2716-1	2048 x 8	350	C, I, L	525/132	+5	3-State	24	6-11
Am2716-2	2048 x 8	390	C	525/132	+5	3-State	24	6-11
Am2732	4096 x 8	450	C, I, L, M	787/157	+5	3-State	24	6-16
Am2732-1	4096 x 8	350	C	787/157	+5	3-State	24	6-16
Am2732-2	4096 x 8	390	C	787/157	+5	3-State	24	6-16
Am2732A*	4096 x 8	250	C	787/184	+5	3-State	24	6-21
Am2764-2	8192 x 8	200	C, I	525/105	+5	3-State	28	6-22
Am2764	8192 x 8	250	C, I, M	525/105	+5	3-State	28	6-22
Am2764-3	8192 x 8	300	C, I	525/105	+5	3-State	28	6-22
Am2764-4	8192 x 8	450	C, I, M	525/105	+5	3-State	28	6-22
Am27128*	16384 x 8	250	C	525/210	+5	3-State	28	6-27

*Available first quarter 1983

Temperature Ranges

C = Commercial 0 to 70°C
M = Military −55 to +125°C
L = Extended −55 to +85°C or +100°C
I = Industrial −40 to +85°C

Package Types

D = Cerdip
P = Plastic
F = Flat Pack
L = Leadless Chip Carrier

Bipolar PROM

Cross Reference Guide

AMD Part No.	Size	Organization	Output	Package Pins	TAA COM'L/MIL Max	Fairchild	Fujitsu	Harris	Intel	Monolithic Memories	National	Raytheon	Signetics	TI
Am27LS18[1]	256	32 x 8	OC	16	50/65					53/63LS080			N/S82S23	TBP18SA030
Am27LS19[1]	256	32 x 8	3S	16	50/65					53/63LS081			N/S82S123	TBP18S030
Am27S18	256	32 x 8	OC	16	40/50			HM7602		53/6330-1	DM75/8577 DM54/74S188		N/S82S23	TBP18SA030
Am27S18A	256	32 x 8	OC	16	25/35					53/6330-1				
Am27S19	256	32 x 8	3S	16	40/50			HM7603		53/6331-1	DM75/8578 DM54/74S288		N/S82S123	TBP18S030
Am27S19A	256	32 x 8	3S	16	25/35					53/6331-1				
Am27S20	1024	256 x 4	OC	16	45/60	93417		HM7610A	M3601	53/6300-1	DM54/74S387	29660	N/S82S126	TBP24SA10
Am27S20A	1024	256 x 4	OC	16	30/40					53/6300-1				
Am27S21	1024	256 x 4	3S	16	45/60	93427		HM7611A	M3621	53/6301-1	DM54/74S287	29661	N/S82S129	TBP24S10
Am27S21A	1024	256 x 4	3S	16	30/40					53/6301-1				
Am27S12	2048	512 x 4	OC	16	50/60	93436		HM7620A	M3602	53/6305-1	DM54/74S570	29610	N/S82S130	
Am27S12A	2048	512 x 4	OC	16	30/40				3602					
Am27S13	2048	512 x 4	3S	16	50/60	93446		HM7621A	M3622	53/6306-1	DM54/74S571	29611	N/S82S131	
Am27S13A	2048	512 x 4	3S	16	30/40									
Am27S15	4096	512 x 8	3S	24	60/90			HM7647R					N/S82S115	
Am27S25	4096	512 x 8	3S	24	N.A.[2]									
Am27S25A	4096	512 x 8	3S	24	N.A.[4]									
Am27S27	4096	512 x 8	3S	22	N.A.[2]									
Am27S28	4096	512 x 8	OC	20	55/70		MB7123	HM7648		53/6348	DM54/74S473	29620	N/S82S146	TBP28SA42
Am27S28A	4096	512 x 8	OC	20	35/45									
Am27S29	4096	512 x 8	3S	20	55/70		MB7124	HM7649		53/6349	DM54/74S472	29621	N/S82S147	TBP28S42
Am27S29A	4096	512 x 8	3S	20	35/45									
Am27S30	4096	512 x 8	OC	24	55/70	93438		HM7640A	M3604	53/6340	DM77/87S475	29624	N/S82S140	TBP28SA46
Am27S30A	4096	512 x 8	OC	24	35/45									
Am27S31	4096	512 x 8	3S	24	55/70	93448		HM7641A	M3624	53/6341	DM77/87S474	29625	N/S82S141	TBP28S46
Am27S31A	4096	512 x 8	3S	24	35/45									
Am27S32	4096	1024 x 4	OC	18	55/70	93452	MB7121E	HM7642A	M3605	53/6352	DM54/74S572	29640	N/S82S136	TBP24SA41
Am27S32A	4096	1024 x 4	OC	18	35/45		MB7121H							
Am27S33	4096	1024 x 4	3S	18	55/70	93453	MB7122E	HM7643A	M3625	53/6353	DM54/74S573	29641	N/S82S137	TBP24S41
Am27S33A	4096	1024 x 4	3S	18	35/45		MB7122H			53/63S441A				
Am27S35	8192	1024 x 8	3S	24	N.A.[2]									
Am27S35A	8192	1024 x 8	3S	24	N.A.[4]									
Am27S37	8192	1024 x 8	3S	24	N.A.[2]						DM87SR81			
Am27S37A	8192	1024 x 8	3S	24	N.A.[4]									
Am27S180	8192	1024 x 8	OC	24	60/80	93450	MB7131	HM7680		53/6380	DM77/87S180	29630	N/S82S180	TBP28SA86
Am27S180A	8192	1024 x 8	OC	24	35/50									
Am27S181	8192	1024 x 8	3S	24	60/80	93451	MB7132	HM7681	M3628	53/6381	DM77/87S181	29631	N/S82S181	TBP28S86
Am27S181A	8192	1024 x 8	3S	24	35/50									
Am27PS181	8192	1024 x 8	3S	24								29633		
Am27PS181A	8192	1024 x 8	3S	24										
Am27S280[3]	8192	1024 x 8	OC	24	60/80					53/6380JS				
Am27S280A[3]	8192	1024 x 8	OC	24	35/50									
Am27S281[3]	8192	1024 x 8	3S	24	60/80					53/6381JS				
Am27S281A[3]	8192	1024 x 8	3S	24	35/50									

BIPOLAR PROM CROSS REFERENCE GUIDE

AMD Part No.	Size	Organization	Output	Package Pins	TAA COM'L/MIL Max	Fairchild	Fujitsu	Harris	Intel	Monolithic Memories	National	Raytheon	Signetics	TI
Am27PS281	8192	1024 x 8	3S	24	35/50									
Am27PS281A[3]	8192	1024 x 8	3S	24										
Am27S184	8192	2048 x 4	OC	18	50/55		MB7127	HM7684		53/63100	DM77/87S184	29650	N/S82S184	TBP24SA81
Am27S184A	8192	2048 x 4	OC	18	35/45		MB7127H							
Am27S185	8192	2048 x 4	3S	18	50/55		MB7128	HM7685		53/63101	DM77/87S185	29651	N/S82S185	TBP24S81
Am27S185A	8192	2048 x 4	3S	18	35/45		MB7128H			53/63S841A				
Am27LS184	8192	2048 x 4	OC	18	60/65									
Am27LS185	8192	2048 x 4	3S	18	60/65									
Am27PS185	8192	2048 x 4	3S	18	60/65							29653		
Am27S190	16384	2048 x 8	OC	24	50/65	93510	MB7137	HM76160			DM77/87S190	29680	N/S82S190	
Am27S190A	16384	2048 x 8	OC	24	35/50									
Am27S191	16384	2048 x 8	3S	24	50/65	93511	MB7138	HM76161	M3636B		DM77/87S191	29681	N/S82S191	TBP28S166
Am27S191A	16384	2048 x 8	3S	24	35/50				M3636B-1					
Am27PS191	16384	2048 x 8	3S	24	65/75							29683		
Am27PS191A	16384	2048 x 8	3S	24	50/65									
Am27S290[3]	16384	2048 x 8	OC	24	50/65									
Am27S290A[3]	16384	2048 x 8	OC	24	35/50									
Am27S291[3]	16384	2048 x 8	3S	24	50/65							29681S		
Am27S291A[3]	16384	2048 x 8	3S	24	35/50									
Am27PS291[3]	16384	2048 x 8	3S	24	65/75							29683S		
Am27PS291A[3]	16384	2048 x 8	3S	24	50/65									
Am27S40	16384	4096 x 4	OC	20	50/65			HM76164						
Am27S40A	16384	4096 x 4	OC	20	35/50									
Am27S41	16384	4096 x 4	3S	20	50/65		MB7134	HM76165		53/63S1641		29641	N/S82S195	
Am27S41A	16384	4096 x 4	3S	20	35/50					53/63S1641A				
Am27PS41	16384	4096 x 4	3S	20	50/65							29643		
Am27S43	32768	4096 x 8	3S	24	N.A.		MB7142		3632				N/S82S321	
Am27S43A	32768	4096 x 8	3S	24	N.A.									
Am27PS43	32768	4096 x 8	3S	24	N.A.									
Am27S45	16384	2048 x 8	3S	24	N.A.[2]									
Am27S45A	16384	2048 x 8	3S	24	N.A.[4]									
Am27S47	16384	2048 x 8	3S	24	N.A.[2]									
Am27S47A	16384	2048 x 8	3S	24	N.A.[4]									

Notes: 1. Replaces Am27LS08/LS09.
2. Contains built-in pipeline registers: nominal address to clock setup time = 35ns (typ), clock to output = 20ns (typ).
3. 300-mil lateral pin spacing.
4. Contains built-in pipeline registers: nominal address to clock setup time = 25ns (typ), clock to output = 15ns (typ).

Bipolar Memory RAM

TTL and ECL Cross Reference Guide

BIPOLAR ECL RAM CROSS REFERENCE GUIDE

AMD Part No.	Organization	No. of Pins	ECL Series	TAA COM'L/MIL	IEE COM'L/MIL	Fairchild	Fujitsu	Hitachi	Motorola	National	Signetics	Siemens
Am10415SA	1024 x 1	16	10K	15/20	−150/−165			HM2110-2 HM2110-1			10415A	
Am10415A	1024 x 1	16	10K	20/25	−150/−165	F10415A	MBM10415AN	HM2110-2 HM2110-1	MCM10146	DM10415	10415	GXB10415
Am10415	1024 x 1	16	10K	35/40	−150/−165	F10415	MBM10415A	HM2110		DM10415A		
Am100415A	1024 x 1	16	100K	15/−	−150/−						100415A	
Am100415	1024 x 1	16	100K	20/−	−150/−	F100415A					100415	
Am10470SA	4096 x 1	18	10K	15/20	−230/−255		MBM10470A	HM10470-1				
Am10470A	4096 x 1	18	10K	25/30	−200/−220	F10470A		HM10470	MCM10470A		10470A	
Am10470	4096 x 1	18	10K	35/40	−200/−220	F10470	MBM10470			DM10470		
Am100470SA	4096 x 1	18	100K	15/−	−230/−		MBM100470A	HM100470-1				
Am100470A	4096 x 1	18	100K	25/−	−195/−			HM100470			100470A	
Am100470	4096 x 1	18	100K	35/−	−195/−	F100470	MBM100470					
Am10474A	1024 x 1	24	10K	15/−	−230/−			HM10474-1				
Am10474	1024 x 1	24	10K	25/−	−230/−	F10474	MBM10474	HM10474				
Am100474A	1024 x 1	24	100K	15/−	−230/−			HM100474-1				
Am100474	1024 x 1	24	100K	25/−	−230/−	F100474		HM100474				GXB100474

BIPOLAR TTL RAM CROSS REFERENCE GUIDE

AMD Part No.	Organization	No. of Pins	Output	TAA (ns) COM'L/MIL	ICC (mA) COM'L/MIL	Fairchild	Intel	Intersil	M.M.I.	Motorola	National	Signetics	TI	
Am27S02A	16 x 4	16	OC	25/30	100/105				6560A		DM74/54S289A			
Am27S03A	16 x 4	16	3S	25/30	100/105				6561		DM74/54S189A			
Am27S02	16 x 4	16	OC	35/50	105/105	93403 74S289					DM74/54S289	N/S82S25		
Am74/54S289	16 x 4	16	OC	35/50	105/105		3101A	5501	65/5560	4064		N/S74/54S289	SN74/54S289	
Am3101A	16 x 4	16	OC	35/50	105/105							N3101A		
Am27S03	16 x 4	16	3S	35/50	125/125	93405 74S189			65/5561		DM74/54S189	N/S74/54S189	SN74/54S189	
Am74/54S189	16 x 4	16	3S	35/50	125/125						DM85/7599			
Am27LS02	16 x 4	16	OC	55/65	35/38				L65/5560		DM74/54LS289			
Am27LS03	16 x 4	16	3S	55/65	35/38				L65/5561		DM74/54LS189			
Am27S06A(1)	16 x 4	16	OC	25/30	100/105									Proprietary
Am27S07A(1)	16 x 4	16	3S	25/30	100/105									Proprietary
Am27S06(1)	16 x 4	16	OC	35/50	100/105									Proprietary
Am27S07(1)	16 x 4	16	3S	35/50	100/105									Proprietary
Am27LS06(1)	16 x 4	16	OC	55/65	35/38									Proprietary
Am27LS07(1)	16 x 4	16	3S	55/65	35/38									Proprietary
Am3101-1(2)	16 x 4	16	OC	35/50	100/105	7489	3101				DM74/5489		SN74/5489	
Am74/5489-1(2)	16 x 4	16	OC	35/50	100/105									
Am3101(2)	16 x 4	16	OC	50/60	100/105									
Am74/5489(2)	16 x 4	16	OC	50/60	100/105									
Am31L01A(2)	16 x 4	16	OC	55/65	35/38									Proprietary
Am31L01(2)	16 x 4	16	OC	80/90	35/38									Proprietary
Am27LS00A	256 x 1	16	3S	35/45	115/115									Proprietary
Am27LS01A	256 x 1	16	OC	35/45	115/115									Proprietary
Am27LS00	256 x 1	16	3S	45/55	70/70	93L420 93421 93L421	3106		65/5531	4256	DM74/54S200	N/S82S116 N/S82S16	SN74/54S201 SN74/54S200 SN74/54LS200	

BIPOLAR TTL RAM CROSS REFERENCE GUIDE (Cont.)

AMD Part No.	Organization	No. of Pins	Output	T_{AA} (ns) COM'L/MIL	I_{CC} (mA) COM'L/MIL	Fairchild	Intel	Intersil	M.M.I.	Motorola	National	Signetics	TI	
Am27LS01	256 x 1	16	OC	45/55	70/70	93411 93L411	3107		65/5530		DM74/54S206	N/S82S117 N/S82S17	SN74/54S301 SN74/54S300 SN74/54LS300	
Am27LS00-1A[1]	256 x 1	16	3S	35/45	115/115									Proprietary
Am27LS01-1A[1]	256 x 1	16	OC	35/45	115/115									Proprietary
Am27LS00-1[1]	256 x 1	16	3S	45/55	70/70									Proprietary
Am27LS01-1[1]	256 x 1	16	OC	45/55	70/70									Proprietary
Am93415A	1024 x 1	16	OC	30/40	155/170	93415A	2115					N/S82S110		
Am93425A	1024 x 1	16	3S	30/40	155/170	93425A	2125					N/S82S111		
Am93415	1024 x 1	16	OC	45/60	155/170	93415	2115			MCM93415		N/S82S10	SN74/54S314	
Am93425	1024 x 1	16	3S	45/60	155/170	93425	2125			MCM93425		N/S82S11	SN74/54S214	
Am93412A	256 x 4	22[3]	OC	35/45	155/70	93412A								
Am93422A	256 x 4	22[3]	3S	35/45	155/70	93422A								
Am93412	256 x 4	22[3]	OC	45/60	155/170	93412				MCM93412				
Am93422	256 x 4	22[3]	3S	45/60	155/170	93422				MCM93422				
Am93L412A	256 x 4	22[3]	OC	45/55	80/90	93L412A								
Am93L422A	256 x 4	22[3]	3S	45/55	80/90	93L422A								
Am93L412	256 x 4	22[3]	OC	60/75	80/90	93L412								
Am93L422	256 x 4	22[3]	3S	60/75	80/90	93L422								

Notes: 1. Noninverting outputs.
2. Write transparent; complement of data-in is available on the outputs in the Write Mode when both $\overline{CS}$ and $\overline{WE}$ are low.
3. Cerpak is 24 pin.

Competitive MOS Memory Cross Reference

AMI	AMD
S2333	Am9233
S2364	Am9265
S4216B	Am9218
S4264	Am9264
S68A364	Am9264[2]
S6831B	Am9218
S68332	Am9232

EA	AMD
EA-2316E/8316E	Am9218
EA-2364	Am9264
EA-23128	Am92128
EA-8332	Am9232
EA-8333	Am9233

FAIRCHILD	AMD
F16K	Am9016
F2114	Am9114
F2114L	Am9114
F2533	Am2833
F2708	Am2708
F3341	Am2841
F3341A	Am2841A
F3347	Am2847
F3357-2	Am2847
F4116	Am9016
F93422	Am9122
F93L422	Am91L22

FUJITSU	AMD
MBM2147	Am2147
MBM2148	Am9148
MBM2149	Am9149
MBM2716	Am2716
MBM2732	Am2732
MBM2764	Am2764
MBM4044	Am9044
MBM8114	Am9114
MB8116	Am9016
MB8128	Am9128
MB8216	Am9016
MB8414 (CMOS)	Am91L14[2]
MB8416 (CMOS)	Am9128[2]

G.I.	AMD
RO3-9322	Am9232

HITACHI	AMD
HM4334 (CMOS)	Am91L14[2]
HN462532	Am2732[3]
HN462716	Am2716
HN462732	Am2732
HM4716A	Am9016
HM472114	Am9114
HM4847	Am2147
HM6116 (CMOS)	Am9128[2]
HM6147 (CMOS)	Am2147[2]
HM6148 (CMOS)	Am9148[2]

INTEL	AMD
1402A	Am2802
1403A	Am2803
1404A	Am2804
1405A	Am2805
1406	Am1406
1407	Am1407

INTEL (Cont.)	AMD
1506	Am1506
1507	Am1507
1702A	Am1702A
1702AL	Am1702AL
2114A	Am9114
2114AL	Am91L14
2117	Am9016
2128	Am9128
2141	Am21L41
2147	Am2147
2148	Am9148
2149	Am9149
2316/8316E	Am9218
2332	Am9233
2364	Am9265
2401	Am2401
2405	Am2405
2708	Am2708
2716	Am2716
2732	Am2732
2732A	Am2732
2764	Am2764
27128	Am27128

MOSTEK	AMD
MK1002P	Am2810
MK1007	Am2847
MK2147	Am2147
MK2716	Am2716
MK2764	Am2764
MK32000	Am9232
MK34000	Am9218
MK36000	Am9264
MK37000	Am9265
MK3702	Am1702A
MK3708	Am2708
MK38000	Am92256[3]
MK4104	Am9244[2]
MK4104	Am21L41
MK4116	Am9016
MK4802	Am9128

MOTOROLA	AMD
MCM2114	Am9114
MCM2147	Am2147
MCM2708	Am2708
MCM2716	Am2716
MCM2532	Am2732[3]
MCM4016	Am9128
MCM4116	Am9016
MCM58366	Am9264
MCM68A364	Am9264[2]
MCM68B364	Am9264[2]
MCM68308	Am9208
MCM68332	Am9232
MCM68365	Am9264[2]
MCM8316E	Am9218

NATIONAL	AMD
MM1402A	Am2802
MM1403A	Am2803
MM1404A	Am2804
MM1702A	Am1702A
MM2114	Am9114
MM2114L	Am9114
MM2116	Am9128

NATIONAL (Cont.)	AMD
MM2147	Am2147
MM2708	Am2708
MM2716	Am2716
MM4006	Am1406
MM4007	Am1407
MM4025	Am2825
MM4026	Am2826
MM4027	Am2827
MM4055	Am2855
MM4056	Am2856
MM4057	Am2857
MM5025	Am2855
MM5026	Am2826
MM5027	Am2827
MM5055	Am2855
MM5057	Am2857
MM5058	Am2833
MM5202AQ	Am1702A
MM52116	Am9218
MM52132	Am9232
MM52164	Am9264
MM5235	Am9265
MM5257	Am9044
MM5258	Am9218
MM5290	Am9016

NEC	AMD
μPD2114L	Am9114
μPD2147	Am2147
μPD2149	Am9149
μPD2316E	Am9218
μPD2332	Am9232
μPD23128	Am92128[2]
μPD2364	Am9264
μPD2708	Am2708
μPD2716	Am2716
μPD4104	Am92L44[2]
μPD4104	Am21L41[2]
μPD416	Am9016
μPD444 (CMOS)	Am91L14[2]
μPD446 (CMOS)	Am9128[2]
μPD6514 (CMOS)	Am91L14[2]
μPD2732	Am2732

SIGNETICS	AMD
1702A	Am1702A
2332	Am9233
2364	Am9265[2]
23128	Am92128[2]
2502	Am2802
2503	Am2803
2504	Am2804
2505	Am2805
2506	Am1406/1506
2507	Am1407/1507
2512	Am2806
2521	Am2809
2524	Am2807
2525	Am2808
2532	Am2847
2533	Am2833
2616	Am9218
2632	Am9232
2664	Am9264

COMPETITIVE
MOS MEMORY CROSS REFERENCE (Cont.)

SYNERTEK	AMD
SY1402	Am2802
SY1403	Am2803
SY1404	Am2804
SY2101	Am9101
SY2111	Am9111
SY2112	Am9112
SY2114	Am9114
SY2114L	Am9114
SY2128	Am9128
SY2316E	Am9218
SY2332	Am9232
SY2333	Am9233
SY2364	Am9264
SY2365	Am9265
SY23128	Am92128
SY2405	Am2405
SY2802	Am2802
SY2803	Am2803
SY2804	Am2804
SY2825	Am2825
SY2826	Am2826
SY2827	Am2827
SY2833	Am2833

T.I.	AMD
TMS2147	Am2147
TMS2149	Am9149
TMS2708	Am2708
TMS2516	Am2716
TMS2532	Am2732[3]
TMS3114	Am2814
TMS3120	Am2847
TMS3128	Am2809
TMS3133	Am2833
TMS3406	Am1406
TMS3407	Am1407
TMS2412	Am2802
TMS3413	Am2803
TMS3414	Am2804
TMS4016	Am9128
TMS40L44	Am90L44
TMS4044	Am9044
TMS40L45	Am91L14
TMS4045	Am9114
TMS4116	Am9016
TMS4244	Am9244
TMS4245	Am9124
TMS4732	Am9232
TMS4764	Am9264

TOSHIBA	AMD
TC5516 (CMOS)	Am9128[2]
TMM2016	Am9128
TMM2732D	Am2732-1
TMM323D	Am2716
TMM416	Am9016

Notes: 1. 110mW Standby Power Dissipation.
2. Pin-for-pin functional equivalent.
3. Different pinout.

Testing High-Performance Bipolar Memory

1

By Bob Lutz
Advanced Micro Devices

Testing High-Performance Bipolar Memory

INTRODUCTION

During the last several years, the state-of-the-art of TTL compatible bipolar memory integrated circuits has advanced very rapidly. Device complexity has increased dramatically not only in terms of the memory storage capacity but also by the addition of new on-chip functions such as the inclusion of output data registers. Simultaneously, advances in bipolar LSI design and manufacturing technology have generated significant improvements in the performance levels of bipolar memory. Similarly, the complexity and performance levels of systems which employ these devices have grown. The concomitant growth of system complexity has placed additional demands on both the device manufacturer and the user's incoming inspection area to assure the performance capabilities of each component before it is assembled into the system.

Several test equipment manufacturers now supply sophisticated, computer controlled testers for these inspection tasks. Most of this equipment is inherently capable of the millivolt and nanosecond accuracies which are required; most memory testers can generate the complex waveforms and test patterns needed. However, the details of applying this equipment to a specific test problem, including the problem of interfacing the tester to the device-under-test, are usually left to the user. The purpose of this application note is to discuss several problems which are frequently encountered when testing high performance bipolar memory devices, and to aquaint the user with how such problems may be identified, measured and corrected.

WHAT MAKES A MEMORY GOOD?

Before discussing the specifics of bipolar memory testing problems, it is important to understand the basic characteristics which these devices should exhibit. Clearly each device must meet all product specification parameters but, first and foremost, a bipolar memory should be fast! Address access time (delay from address input to data output), enable access time, and enable recovery time should be as small as possible. High performance is often the primary reason for using bipolar memory. Similarly, the performance of the ideal bipolar memory should remain relatively constant with changes in supply voltage, ambient temperature and output load capacitance. Fast devices, offering stable performance over a broad range of conditions, permit the user to qualify a smaller number of part types; one fast device can accommodate many standard as well as high performance applications. Such devices provide added safety margin for the system design, permit simplification of system test and debug, and assure trouble-free system performance in the field. Hence the "best" memory is a fast, stable device which not only meets a given user specification, but also offers the extra performance needed for a broad range of applications.

Advanced Micro Devices offers a family of bipolar Random Access Memories (RAMs) and Programmable Read Only Memories (PROMs) which are designed to meet this idealized definition as closely as possible. First, each AMD device is designed to meet a "military design goal." This means AMD bipolar memories are designed to provide the extra margins and higher output drive capabilities needed to assure proper performance over the extended military supply voltage and operating temperature ranges. This often necessitates the use of more advanced design techniques such as on-chip regulators, temperature and voltages compensation networks, and feedback circuits. Second, AMD has conceived and developed an advanced, oxide separated, ion implanted manufacturing process called IMOX™. Developed specifically for the production of high density bipolar memories, this technology provides both high density and excellent performance in a truly reliable and manufacturable process. This combination of advanced design and fabrication technologies assures the military user of receiving components which are intended for his application while providing the commercial user with the extra margins, performance advantages and procurement benefits mentioned above.

THE SYSTEM ENVIRONMENT

To understand the problems of high-performance memory testing, it is helpful to understand the electrical environment in which the memory devices will actually operate, i.e., the typical system environment. The system designer must address and resolve several critically important questions if the system is to consistently perform to its design specifications. These questions include:

1. What noise voltages can the system's logic and memory devices tolerate?
2. What are the sources of system noise?
3. What can be done to control and minimize this noise?

The first question is answered relatively easily. The magnitude of noise which can be tolerated relates directly to the worst case noise immunity specified for the logic family. Noise immunity is simply the difference between the worst case output levels (V_{OH} and V_{OL}) of the driving circuit and the worst case input voltage requirements (V_{IH} and V_{IL}, respectively) of the receiving circuit. For TTL devices the worst case noise immunity is typically 400mV for both the high and low logic levels.

If "system noise" is defined as the sum of things which subtract from this noise immunity, several sources can be identified. A few of the most important sources found in a digital, TTL system are listed below:

- Cross-Talk: The desire to pack system components as tightly as possible inevitably causes signal wires or PC board traces to be placed in close proximity. The lead-to-lead capacitance and mutual inductance thus created (see Figure 1) causes "noise" voltages to appear when adjacent signal paths switch.
- Transmission Line Reflections: Like it or not, every signal path in the system has transmission line characteristics. TTL signal paths are usually not designed as transmission lines, with predictable and uniform characteristic impedances. This is partly because of the higher costs implied for multilayer PC boards with internal ground planes, termination resistors, etc. It is also the result of TTL logic's limited ability to drive the low impedance lines provided by current PC board technologies. Hence, TTL signal paths do exhibit the ringing and reflection problems associated with improperly terminated transmission lines. These reflections subtract from the available noise immunity as shown in Figure 2.
- Ground Network Noise: Most high-performance systems employ large numbers of high-performance ICs. These devices typically draw large I_{CC} currents from the power supply. Cumulatively, these currents can reach several amperes per board. Such currents, flowing in the ground network, cause non-negligible DC voltage drops to occur; not all device ground pins are at zero volts. Since the output levels and the input thresholds of each TTL device reference the local ground (Figure 3a), these drops also subtract from the available noise immunity. Additional noise margin losses occur each time the device outputs switch. This occurs because large currents must flow to rapidly charge and discharge the interconnect and input capacitances which load each output. These charging currents flow in a loop (Figure 3b) through the ground network which is normally a simple interconnection of

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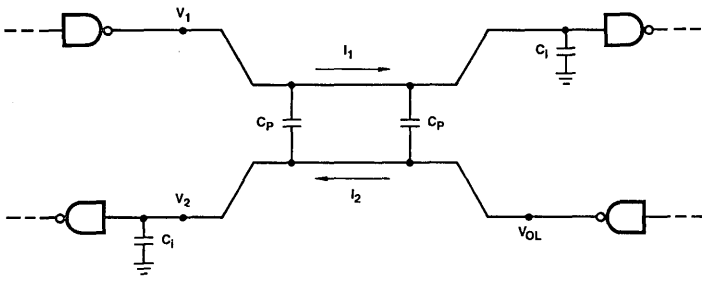
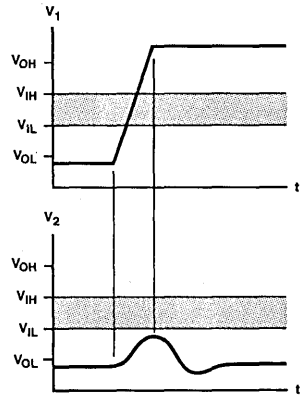
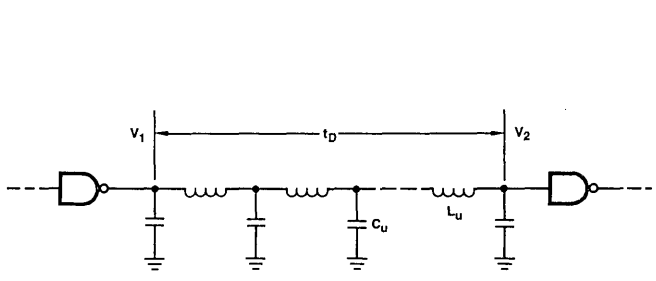
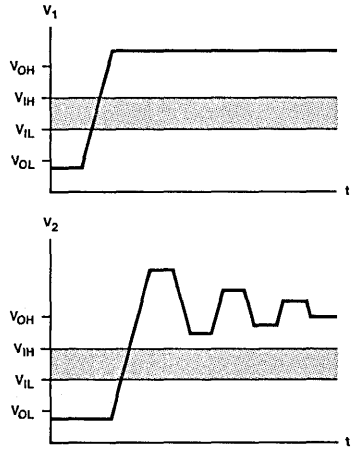




As V_1 switches, I_1 flows to charge the input capacitance C_i. I_2 flows as a result of mutual inductance. The V_1 voltage change is also coupled directly to V_2 through the parasitic line-to-line capacitances, C_p.

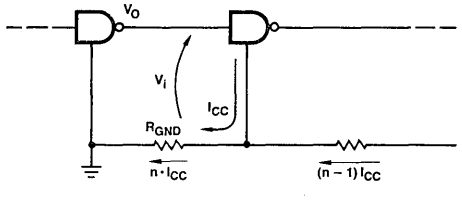
Figure 1. An Example of Cross-Talk





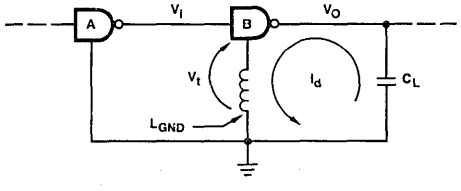
The unit length capacitance and inductance (C_u and L_u) give each system connection transmission line characteristics. Without a matched termination, switching at V_1 causes reflection voltages to appear at V_2, reducing noise immunity.

Figure 2. Line Reflections



$V_i = V_O - (n \cdot I_{CC})\, R_{GND}$

a) DC Ground "Noise"



When V_i goes HIGH, V_O goes LOW discharging C_L. The discharge current I_d flows through the ground inductance L_{GND}, creating a transient voltage V_t. The input voltage seen by gate B is actually $V_i - V_t$.

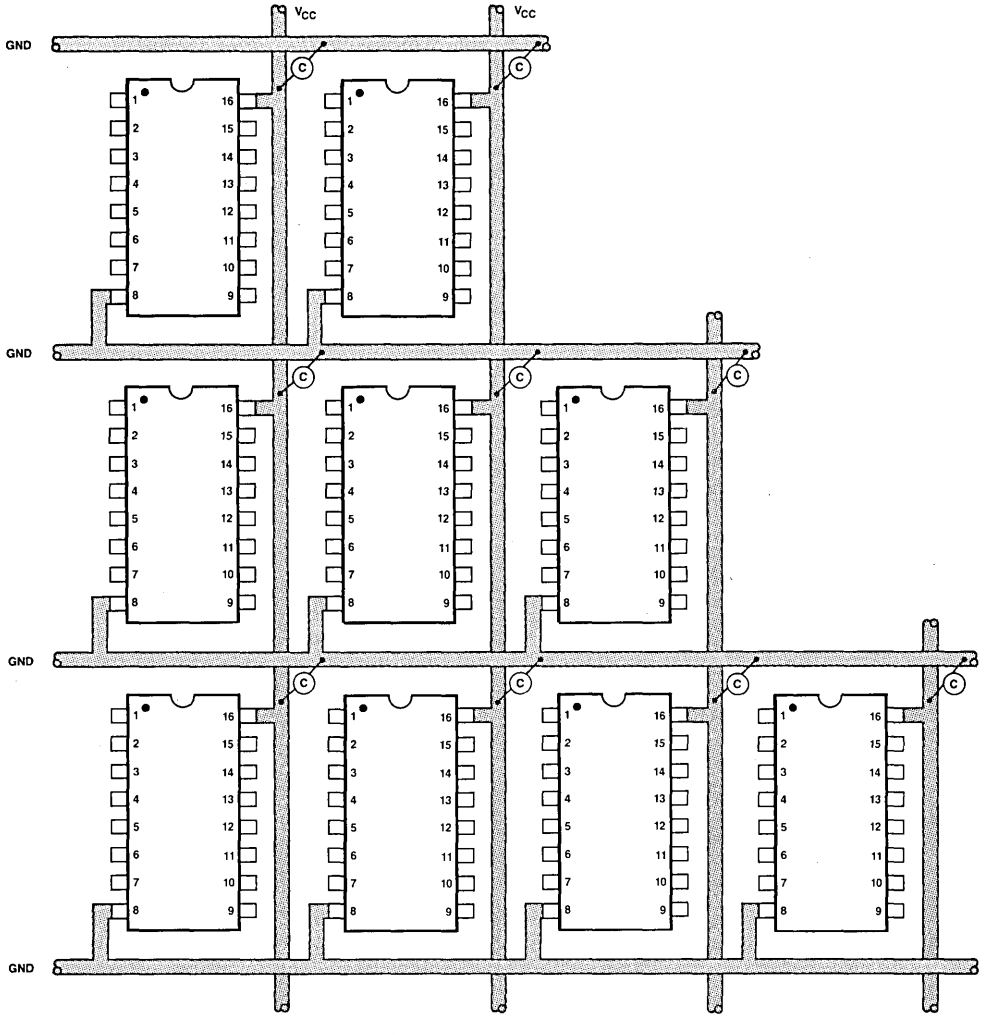
b) Transient Ground Noise

Figure 3.

wires, each with some value of resistance and inductance per unit length. Some additional resistive drops occur. But, the rapid changes in these currents (large di/dt), occurring as charging starts and stops, mean a transient ground noise voltage is also generated. This voltage obeys the law of v = L(di/dt) where L is the ground circuit inductance and di/dt is the rate of change of the charging currents. Notice that adding local bypass capacitors can only reduce this voltage by paralleling the ground inductance with the V_{CC} network inductance. Bypassing cannot eliminate this problem because these capacitors shunt the devices and not the ground and V_{CC} network inductances where the noise is generated.

Controlling and minimizing noise in a digital system becomes more challenging as the system performance requirements increase. These requirements demand devices capable of short propagation delays, e.g., ultra-fast memories with excellent drive characteristics to minimize fully loaded access times. Since noise margin violations result in system malfunctions, the system designer must define a set of rules governing the physical construction techniques to be used within the system. These rules address a host of considerations including power distribution, AC grounding, lead placement, line termination requirements, logic loading (fan in and fan out), and interconnect delays. Specifying these rules is a complex process of making appropriate cost-performance tradeoffs.

For a medium to high performance system, these rules might specify arranging devices in an array with V_{CC} power traces running vertically up the columns while ground metal running horizontally between the rows. Inserting bypass capacitors at each grid intersection forms an AC ground mesh (Figure 4), limiting the amount of ground inductance at each array site. If limits are also placed on the total capacitance each device may drive (cumulative interconnect and input capacitance on all outputs), the total charging currents may be controlled thus limiting



Note: Transient ground currents flow in four directions from each device ground: right and left on the ground bus; up and down the V_{CC} bus after passing through the local bypass capacitor, C. Equivalent ground inductance is very low.

Figure 4. Example of an AC Ground Mesh

the noise immunity eroded by ground circuit noise. Similarly, the distance between adjacent traces and the maximum length of unterminated lines may be specified to control noise immunity losses caused by cross-talk and termination mismatches. Ultra-high performance systems may require additional measures; e.g., multilayer boards with true ground planes or increased usage of line drivers and receivers. Though the preceding descriptions have been simplified, it should be clear that distances between driving and receiving devices, the quantity and distribution of load capacitance, as well as the AC ground network integrity are all essential elements of the system design.

THE MEMORY TEST ENVIRONMENT

Ideally the test system hardware and fixtures would be designed to even more stringent rules than those used for the system. This is reasonable as the tester is the standard employed for accepting or rejecting components used in the system. Because a collection of additional objectives constrain the test environment, designing test hardware to equally or more stringent rules is usually impractical.

Memory testers must test many types of components under a variety of conditions. Tests performed include DC parametric tests, functional and AC tests with complex test patterns, and margin tests to assure device operation at the extremes of applied conditions and supply voltage. To accomplish this, connections to sets of programmable input drivers and output receivers (comparators), multiple device bias and power supplies, relays to permit connection of the DC parametric test unit, and special load circuits must all converge at the test site.

To provide flexibility and facilitate repair, test hardware must be modular. This requirement dictates placing the hardware (drivers, receivers, etc.) on many small PC boards which then must talk to the DUT (device under test) through additional wiring and connectors.

Frequently the quantity of parts tested necessitates mating an automatic device handler to the tester. Handlers also provide capabilities for testing at temperature extremes when needed. The DUT must be tested inside this equipment, requiring still more wiring between the test head and the actual test site.

Ideally, all test hardware would be located immediately adjacent to the test site to minimize cross-talk, reflections and ground noise. However, this objective must be compromised to address the other objectives and constraints outlined above. Techniques commonly employed in making this compromise are illustrated in Figure 5. Notice that DUT drivers are remote from the test site, driving signal to the DUT through "series terminated" transmission lines. Similarly the receivers are some distance from the test site, receiving signals from the DUT through a series of connectors and wires which can degrade the signal. Most annoying of all, the test site ground connection has been compromised. This single path must carry heavy transient and DC currents during test and should provide a very solid, low impedance reference against which all AC and DC tests are made. Accumulating resistance and inductance in this path jeopardizes the integrity of all test results.

Hence, the electrical environment provided at the test site is generally inferior to the actual system environment where the memory component will be used.

TEST RELATED PROBLEMS AND SOLUTIONS

Accurately measuring or verifying memory performance in the test system environment requires a recognition of its inherent limitations. Outlined below are five problem areas commonly encountered when testing high-performance bipolar memories. Methods of identifying and alleviating these problems are indicated.

- Contending with Ground Noise: Ground noise is one of the most common and troublesome test problems. As defined above, ground noise is caused by switching currents flowing through the ground network impedance. Whereas the system environment (Figure 4) may provide multiple low inductance ground paths into a ground mesh or plane, the tester provides one long, higher inductance path back to the test system ground (Figure 5). This path includes handler contacts, connectors and the DUT load board, all of which increase ground

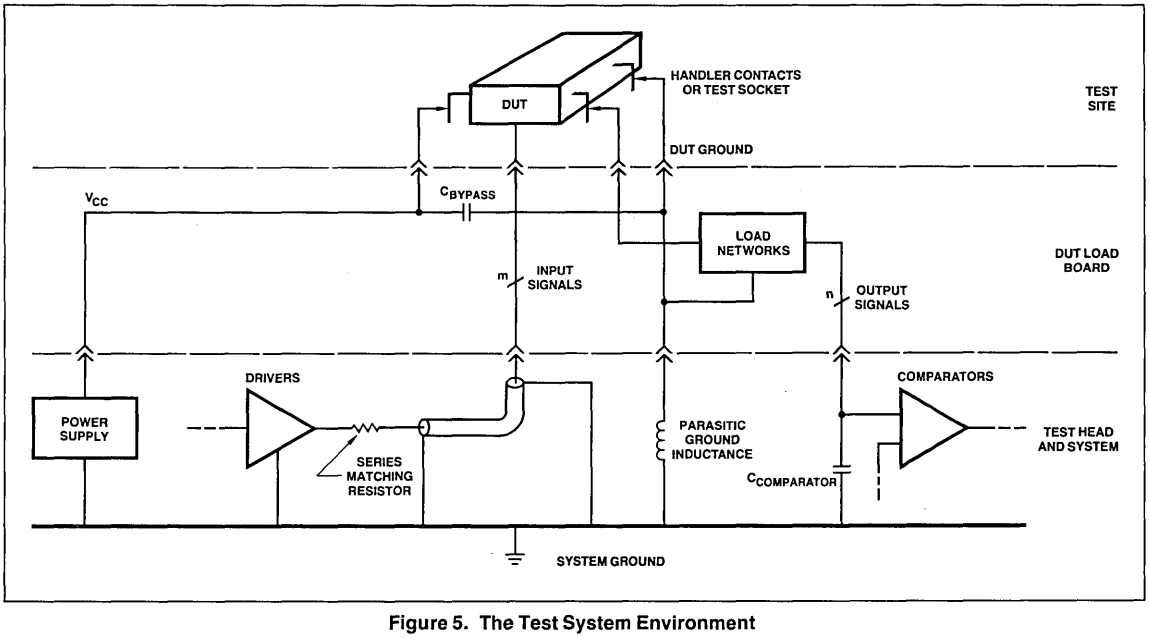


Figure 5. The Test System Environment

inductance and resistance. Transient currents which result when the DUT switches can be enormous. Consider the case of a byte wide (8 output) memory functional test. At some point in the test sequence, all memory outputs will switch from high to low (V_{OH} to V_{OL}) at the same instant, discharging all eight load capacitances simultaneously. If the input capacitance of the receiver is 40pF and the interconnect capacitance of the test fixture is 10pF, the total load capacitance driven by all device outputs would be 400pF. A fast memory device could discharge this load at a 1V/ns rate. The relationship i = C(dv/dt) implies peak charging currents of 400mA must flow through ground. As Figure 6 illustrates, this charging current does not build to its full value instantaneously. For a fast device the time required to go from zero to full charging current would approximate 2ns A resultant ground current di/dt of 200mA/ns is implied. If the ground inductance is 1 nanohenry (approximate inductance of 1 inch of straight, small guage wire), then v = L(di/dt) predicts AC ground noise of 200mV. As you have probably guessed, the typical test site ground inductance exceeds 1nh. The path is longer and it is usually not a straight line connection. Actual tester ground noise of up to 800mV is common when testing high-performance byte wide memories. This noise can be measured easily with a high bandwidth oscilloscope by attaching the scope ground to the actual test system ground and monitoring the DUT ground pin with one channel.

Excessive ground noise creates several problems. First, this noise is capacitively coupled to the input drive signals through the DUT input capacitances; if large enough, DC coupling through the DUT input clamp diodes can occur (Figure 7). The DUT output levels are, of course, referenced to the DUT ground potential whereas the receiver board is referenced to test system ground, introducing inaccuracy in access time measurements, etc.

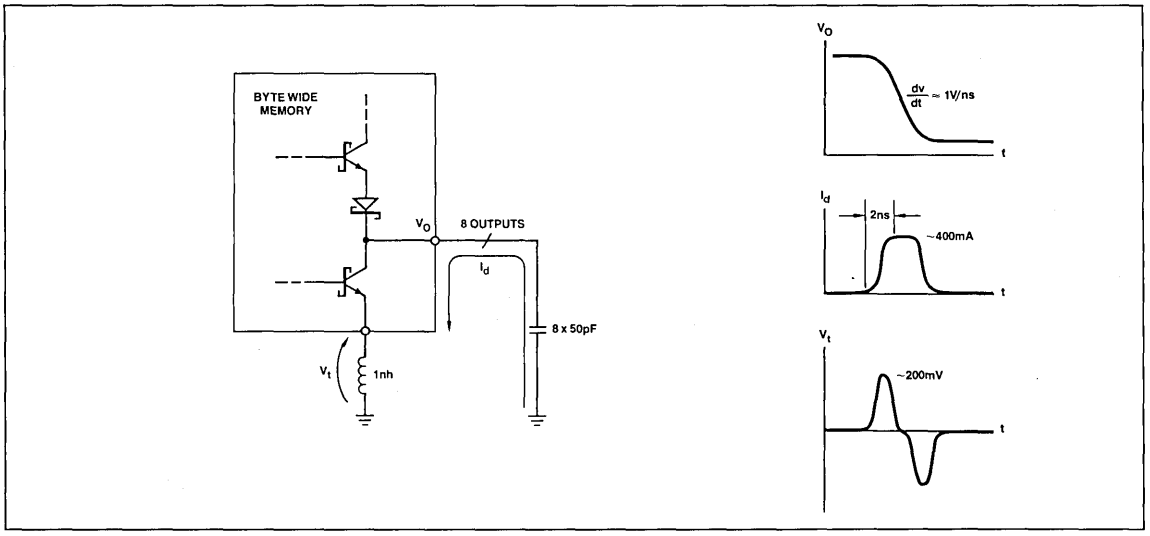
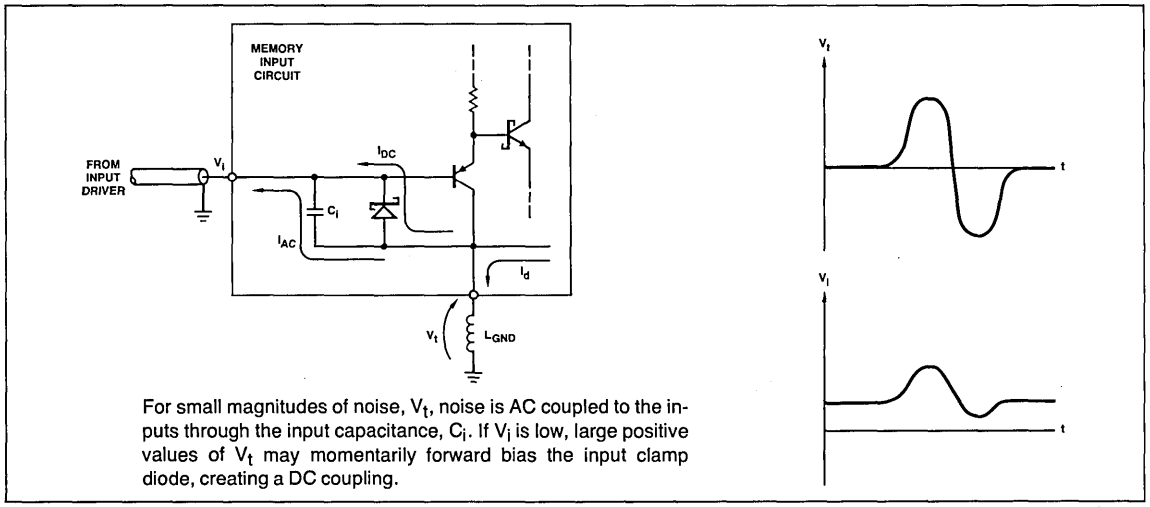


Figure 6. Byte Wide Memory Ground Transients



For small magnitudes of noise, V_t, noise is AC coupled to the inputs through the input capacitance, C_i. If V_i is low, large positive values of V_t may momentarily forward bias the input clamp diode, creating a DC coupling.

Figure 7. Ground Noise Coupling to the Inputs

Worst of all severe ground noise can make functional testing at or near the guaranteed input levels (V_{IH} and V_{IL}) impossible. To demonstrate, assume the device ground noise reaches a positive 0.8V with respect to test system ground during output switching. Assume the input driver high level is programmed to 2.0V, minimum V_{IH} for most TTL devices. The actual voltage between a "high" DUT input and its ground is only 1.2V. The typical room temperature threshold voltage of a TTL device is 1.5V, and the device interprets 1.2V as a logic "low." This causes the memory to access a new memory location momentarily. The resultant momentary change in output data interferes with access time measurements. In severe cases, this momentary switching of output data creates additional ground noise which also feeds back to the inputs resulting in sustained oscillations. This noise interaction can also be viewed with a dual trace oscilloscope as shown in Figure 8. Channel A of the scope is connected to the address input while channel B monitors the DUT ground pin. The input voltage, as seen by the DUT, can be viewed directly by putting the scope in "A – B," algebraic subtract mode. Note the scope ground is connected to test system ground as before. Attaching scope ground to the DUT pin ground should be avoided as this creates a "ground loop." If connected this way, large noise currents flow in the alternate ground path provided by the scope back to earth ground; this interferes with the scope's ability to measure high-speed events and modifies the condition which is to be observed.

Several techniques can be employed to reduce ground noise problems:

- Keep the ground path as short as possible; use large diameter wire and "straight line" wiring techniques.
- Minimize the number of series connections in the DUT ground path; provide as many parallel ground connections as possible through each remaining connector.
- If the system uses a Kelvin (force – sense) ground system, terminate the system by shorting force to sense on the DUT load board. Kelvin systems provide DC accuracy, but their response times are much too slow to aid in the suppression of ground noise at the test site. Terminating Kelvin early sacrifices a little DC accuracy, but the ability to use the previous sense line as second, low impedance ground path usually improves the overall test accuracy.
- Provide multiple high frequency bypass capacitors as close as possible to the DUT, and again on the DUT load board. This allows the V_{CC} wiring to serve as an extra AC ground path for high frequency ground noise.
- Reduce the DUT load capacitance (receiver and interconnect capacitance) as much as possible; avoid using low values of load resistors. Both techniques reduce the transient currents, thus improving test accuracy. When necessary, DUT output drive capability can usually be verified with DC tests.
- If V_{IL} and V_{IH} tests are necessary, measure the maximum amount of ground noise that the specific device type to be tested generates in the actual test site. Set the input drive levels no tighter than "V_{IH} plus the maximum noise" and "V_{IL} minus the maximum noise." Using tighter limits over tests the device!
- Alternatively, use DC bench tests on a sample basis to verify that input margins are acceptable. This is a sound practice as the input thresholds of bipolar devices are ex-

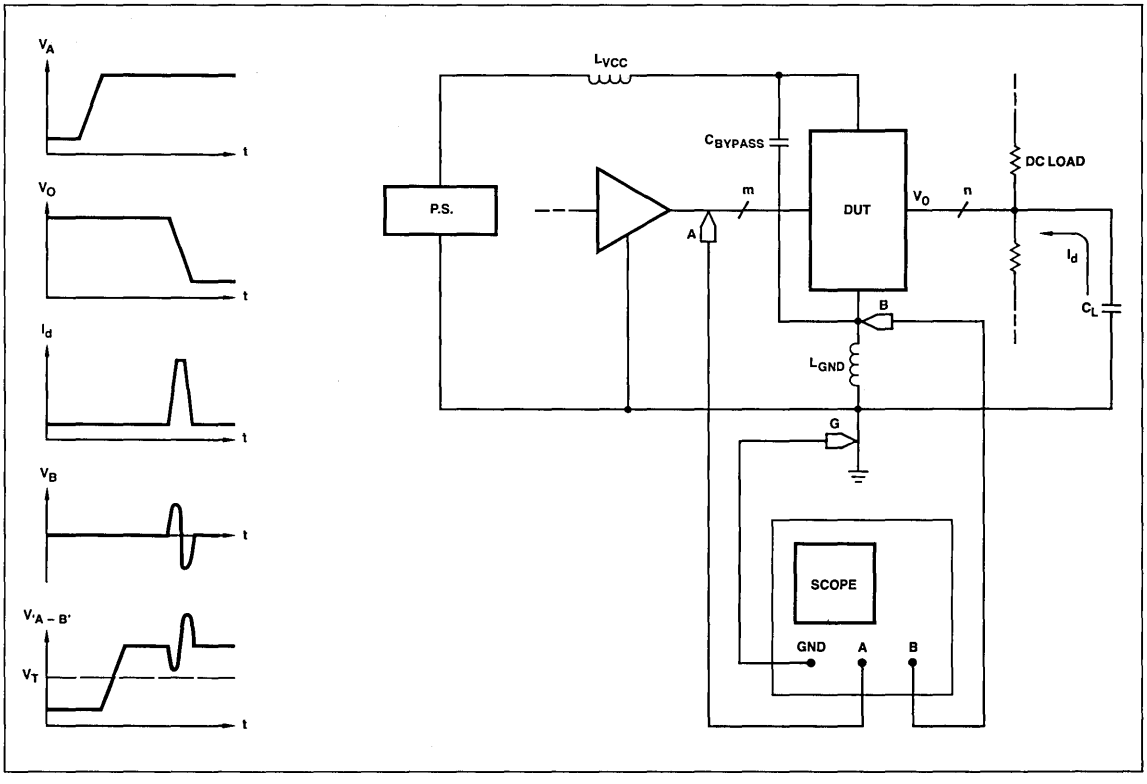


Figure 8. Monitoring Ground Noise

tremely insensitive to fabrication process variations. Virtually any process variation or defect which would result in a threshold failure would also result in the catastrophic failure of other tests.

- DC verification of V_{IL} and V_{IH} can also be performed on the test system, but care must be exercised to insure that input voltages NEVER cross through the 0.8 to 2.0V window; voltages residing in this window can cause the DUT to switch, triggering sustained oscillations.

- The Output "Tank Circuit": A second common problem encountered is resonance in the circuitry which connects the DUT outputs to the output comparators or receivers. This resonance occurs because the wire connecting the DUT outputs to the receivers is actually an inductor connected in series with the comparator input capacitance, forming a series resonant tank circuit (Figure 9). This load circuit is quite different from the typical loading situation found in a system environment. Notice that the capacitance in the tester tends to be a single large value of capacitance, lumped at the end of the DUT output drive line. The load capacitance in the system is generally smaller and it is distributed along the drive line; this configuration looks much more like a transmission line, with per unit length values of inductance and capacitance, than it does a resonant tank. The resonant frequencies found at the test site vary with wire length and capacitive load, but tend to be in the 100 – 500MHz range. The input voltage sensed by the receiver is actually the voltage at the center connection within the tank circuit, which can ring violently when the outputs switch; measurement errors of 5ns or more can occur. A good evaluation technique for this problem is to compare the waveforms observed at the output of the device with a "shmoo plot" of the output. Assuming a simple pattern is used, differences in these results may indicate a resonance problem.

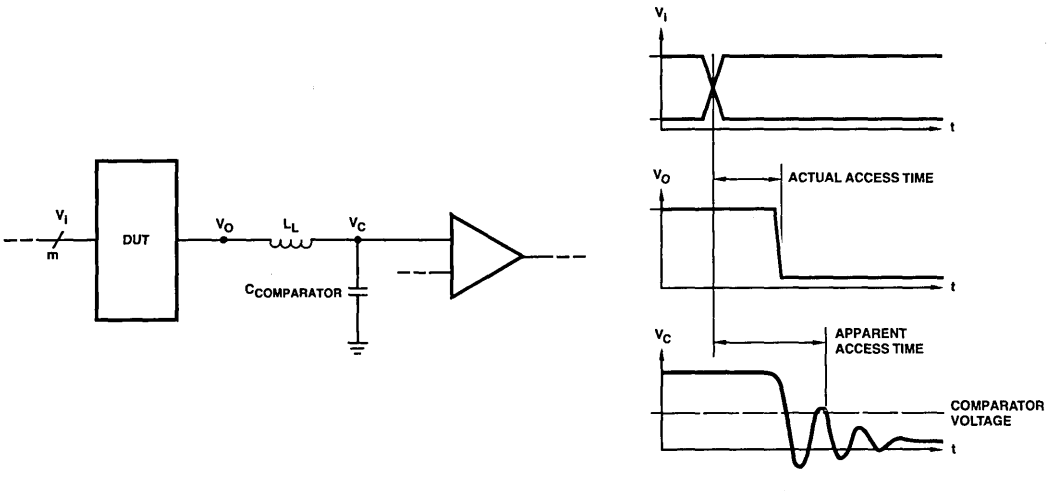
  Corrective action for this problem includes:

  - Use short, low inductance connections from the DUT output to the receiver; minimize comparator and interconnect capacitance. Both techniques raise the resonant frequency of the tank circuit which limits the time measurement error and reduces the DUT's ability to stimulate ringing in the tank.
  - Use twisted pair wiring techniques to connect DUT outputs to the receivers. Though this raises the capacitance slightly, it reduces the purely inductive character of the interconnect, usually tending to reduce ringing.

- Minimizing Cross-Talk: Cross-talk between the input and output lines of the DUT is also a common problem. Obviously, the greater the number of paths which must be packed into a given area, the greater the problem. The signal coupling that occurs adds noise to both the input lines, making V_{IH} and V_{IL} testing difficult, and output lines, reducing the accuracy of timing measurements. Techniques which tend to reduce cross-talk include the following:

  - Keep wires as short as possible and avoid laying wires on top of each other.
  - Reduce output loading to minimize the magnitude of current transients which could be coupled into adjacent lines.
  - Use twisted pair or coaxial cable wherever possible; take care to tie all grounds from these transmission lines together at both ends.
  - Use ground plane or ground mesh techniques in the load board and the handler interface if possible. A true ground plane permits the use "strip" transmission lines which not only minimize cross-talk, but also reduce ground noise.

  Though expensive, ground plane techniques offer the test engineer a consistent reference voltage which can be used to identify and segregate the various components and sources of noise.



L_L, the interconnect inductance and $C_{COMPARATOR}$ form a series resonant tank circuit which can cause time measurement errors.

Figure 9. Resonance at the Outputs

CONCLUSION

Advanced Micro Devices has invested significantly in the development of advanced, high-performance bipolar memory technologies and products. As the preceding discussion demonstrates, the memory tester presents a very different environment to the memory device than does the system. The additional constraints placed on the tester virtually guarantee that devices which function in this "worst case" environment will perform satisfactorily in the system. However, this worst case environment may also selectively reject the best performing devices; i.e., those with the fastest access times and best drive characteristics. This occurs because high-performance devices magnify the problems found in the tester environment. The information presented here should aid the component engineer in recognizing and resolving these special test environment problems. Attention to these details will reward the bipolar memory user by assuring acceptance of the best and broadest range of bipolar memories currently available.

Bipolar Programmable Read Only Memory (PROM) Index

Am27S18A • Am27S19A
Am27S18 • Am27S19

256-Bit Generic Series Bipolar PROM
(32 x 8 bits with ultra fast access time)

"A" VERSION ADVANCED INFORMATION

2

DISTINCTIVE CHARACTERISTICS

- High Speed – 25ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

FUNCTIONAL DESCRIPTION

The Am27S18A/18 and Am27S19A/19 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 32 x 8 configuration, they are available in both open collector Am27S18A/18 and three-state Am27S19A/19 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_4 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_7 go to the off or high impedance state.

GENERIC SERIES CHARACTERISTICS

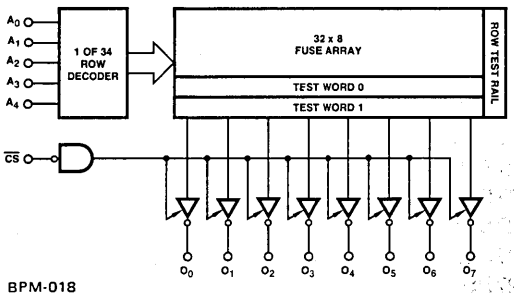
This Am27S18A/18 and Am27S19A/19 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

BLOCK DIAGRAM



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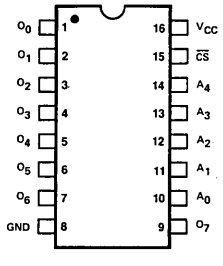
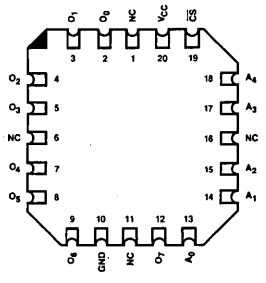
CONNECTION DIAGRAMS
Top Views

DIP



BPM-020

Chip-Pak™ L-20-1



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Note: Pin 1 is marked for orientation.

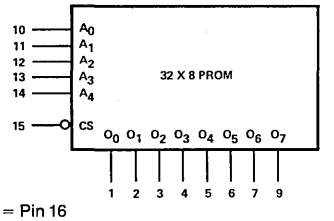
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}					0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					25	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX				90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $V_{\overline{CS}}$ = 2.4V		V_O = 4.5V			40	μA
			Note 2	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)				4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)				8		

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

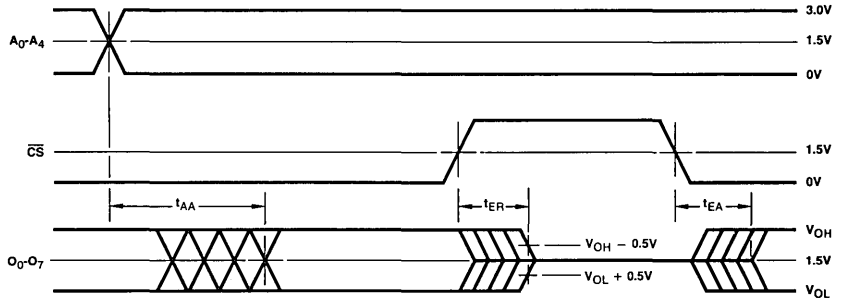
SWITCHING CHARACTERISTICS OVER OPERATING RANGE
"A" VERSION ADVANCED INFORMATION

Parameter	Description	Test Conditions	Typ 5V 25° A	Typ 5V 25° STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	18	25	25	40	35	50	ns
t_{EA}	Enable Access Time		13	15	20	25	25	30	ns
t_{ER}	Enable Recovery Time		13	15	20	25	25	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

2

SWITCHING WAVEFORMS



BPM-021

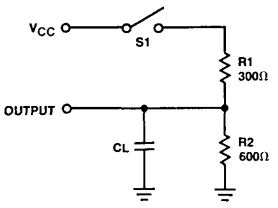
Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-022

PROGRAMMING

The Am27S18A/18 and Am27S19A/19 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

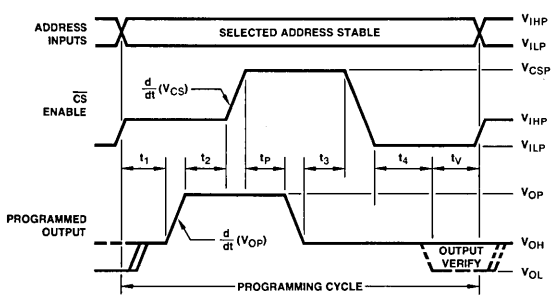
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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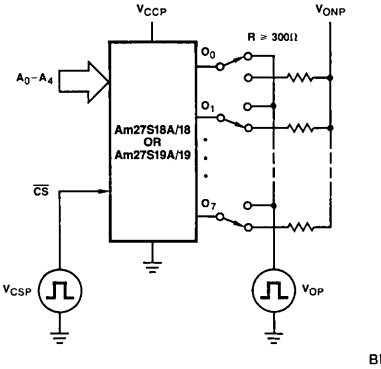
SIMPLIFIED PROGRAMMING DIAGRAM



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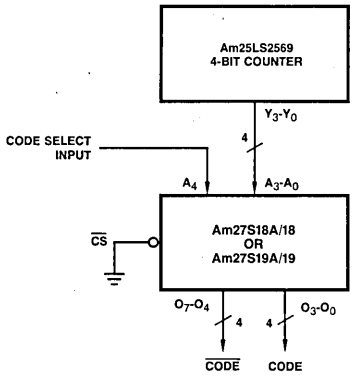
APPLYING THE Am27S18A/18 AND Am27S19A/19

The Am27S18A/18 and Am27S19A/19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal of BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am27S18A/18 or Am27S19A/19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.



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TRUTH TABLE

ADDRESS					COMPLEMENT				TRUE				
A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE
0	0	0	0	1	1	0	1	1	0	1	0	0	
0	0	0	1	0	1	0	1	0	0	1	0	1	
0	0	0	1	1	1	0	0	1	0	1	1	0	
0	0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	0	1	0	1	1	1	1	0	0	0	
0	0	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	1	1	0	1	0	1	1	0	1	0	
0	1	0	0	0	0	1	0	0	1	0	1	1	
0	1	0	0	1	0	0	1	1	1	1	0	0	
0	1	0	1	0	X	X	X	X	X	X	X	X	
0	1	0	1	1	X	X	X	X	X	X	X	X	
0	1	1	0	0	X	X	X	X	X	X	X	X	
0	1	1	0	1	X	X	X	X	X	X	X	X	
0	1	1	1	0	X	X	X	X	X	X	X	X	
0	1	1	1	1	X	X	X	X	X	X	X	X	
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE
1	0	0	0	1	1	1	1	0	0	0	0	1	
1	0	0	1	0	1	1	0	0	0	0	1	1	
1	0	0	1	1	1	1	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	1	0	1	1	0	
1	0	1	0	1	1	0	0	0	0	1	1	1	
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1	1	1	0	0	0	1	0	1	1	0	1	0	
1	1	1	0	1	0	1	0	0	1	0	1	1	
1	1	1	1	0	0	1	1	0	1	0	0	1	
1	1	1	1	1	0	1	1	1	1	0	0	0	

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80S	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S18A/18 Am27S19A/19	715-1407-1	PA 16-6 and 32 x 8 L	IM 32 x 8-16 AMD	SA 3-1	DIS-156 AM	DA 22	AM 110-2

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
25ns	AM27S18APC	AM27S19APC	P-16-1	C-1	COM'L
	AM27S18APCB	AM27S19APCB	P-16-1	B-1	
	AM27S18ADC	AM27S19ADC	D-16-1	C-1	
	AM27S18ADCB	AM27S19ADCB	D-16-1	B-1	
	AM27S18ALC	AM27S19ALC	L-20-1	C-1	
	AM27S18ALCB	AM27S19ALCB	L-20-1	B-1	
35ns	AM27S18ADM	AM27S19ADM	D-16-1	C-3	MIL
	AM27S18ADMB	AM27S19ADMB	D-16-1	B-3	
	AM27S18AFM	AM27S19AFM	F-16-1	C-3	
	AM27S18AFMB	AM27S19AFMB	F-16-1	B-3	
	AM27S18ALM	AM27S19ALM	L-20-1	C-3	
	AM27S18ALMB	AM27S19ALMB	L-20-1	B-3	
40ns	AM27S18PC	AM27S19PC	P-16-1	C-1	COM'L
	AM27S18PCB	AM27S19PCB	P-16-1	B-1	
	AM27S18DC	AM27S19DC	D-16-1	C-1	
	AM27S18DCB	AM27S19DCB	D-16-1	B-1	
	AM27S18LC	AM27S19LC	L-20-1	C-1	
	AM27S18LCB	AM27S19LCB	L-20-1	B-1	
50ns	AM27S18DM	AM27S19DM	D-16-1	C-3	MIL
	AM27S18DMB	AM27S19DMB	D-16-1	B-3	
	AM27S18FM	AM27S19FM	F-16-1	C-3	
	AM27S18FMB	AM27S19FMB	F-16-1	B-3	
	AM27S18LM	AM27S19LM	L-20-1	C-3	
	AM27S18LMB	AM27S19LMB	L-20-1	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Refer to

Am27S18 • Am27S19

Bipolar Memory PROM Product Specification

The Am29750A is replaced by the Am27S18 (open collector).

The Am29751A is replaced by the Am27S19 (three-state).

Am27LS18 • Am27LS19

Low-Power Schottky 256-Bit Generic Series Bipolar PROM

DISTINCTIVE CHARACTERISTICS

- High Speed – 55ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

FUNCTIONAL DESCRIPTION

The Am27LS18 and Am27LS19 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 32 x 8 configuration, they are available in both open collector Am27LS18 and three-state Am27LS19 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_4 and holding chip select input, $\overline{CS}$, at a logic LOW. If either chip select input goes to a logic HIGH, O_0-O_7 go to the OFF or high impedance state.

GENERIC SERIES CHARACTERISTICS

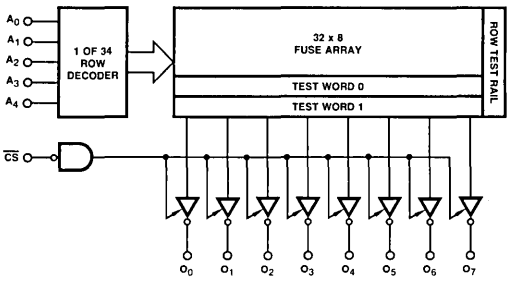
The Am27LS18 and Am27LS19 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

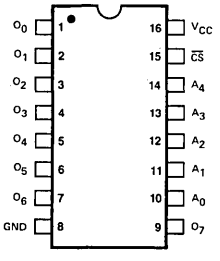
BLOCK DIAGRAM



BPM-018

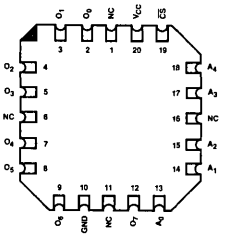
CONNECTION DIAGRAMS
Top Views

DIP



BPM-020

Chip-Pak™ L-20-1



BPM-288

Note: Pin 1 is marked for orientation.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

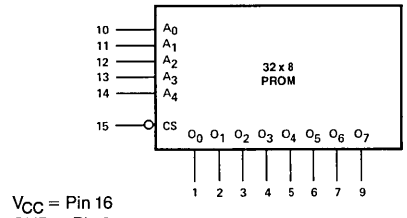
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

BPM-019

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
V_{OH} (Am27LS19 only)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V			25	μA
I_{SC} (Am27LS19 only)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 3)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX		60	80	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $\overline{CS}$ = 2.4V; V_O = 4.5V			40	μA
		V_{CC} = MAX, $\overline{CS}$ = 2.4V; Am27LS19 Only; V_O = 2.4V			40	μA
		V_{CC} = MAX, $\overline{CS}$ = 2.4V; Am27LS19 Only; V_O = 0.4V			−40	μA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 4)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 4)		8		pF

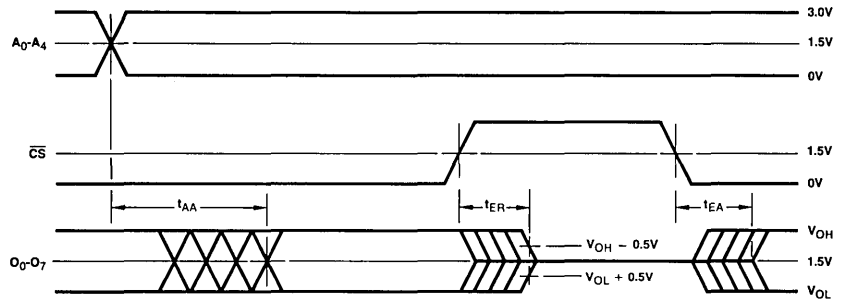
Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	30	55	75	ns
t_{EA}	Enable Access Time		22	40	50	ns
t_{ER}	Enable Recovery Time		18	35	40	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

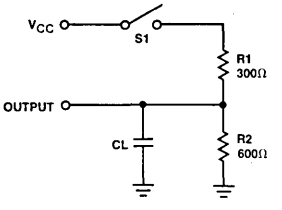
BPM-021

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE. "OFF" STATE

AC TEST LOAD



BPM-022

PROGRAMMING

The Am27LS18 and Am27LS19 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

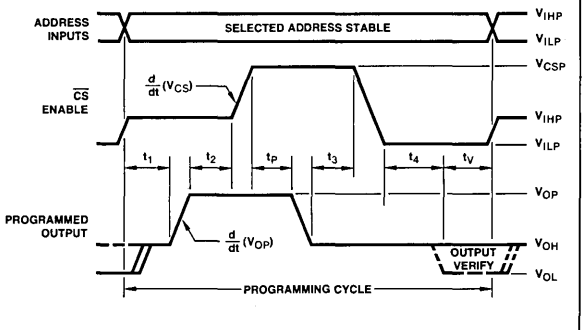
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

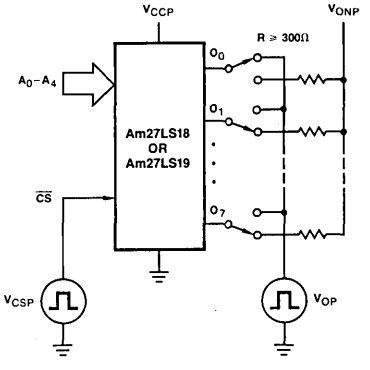
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-023

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-024

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am27LS18 • Am27LS19 ADAPTERS AND CONFIGURATORS	715-1407-1	PA16-6 and 32 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 32 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

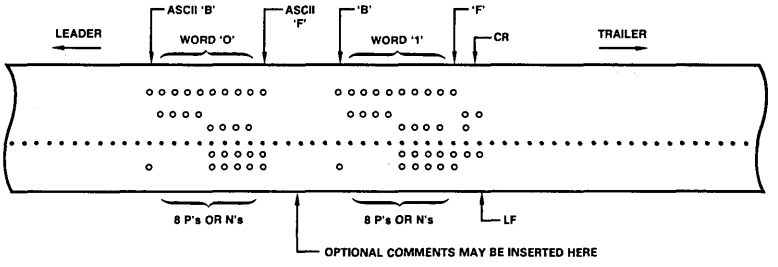
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNFF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :    ::::::::::    :
Ø31   BNNNNPPPNF   END (R) (L)

(R) = CARRIAGE RETURN
(L) = LINE FEED
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	H	L	L	L	H	H	H	H	H	L
L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	H	L	H	L	L	H	H	H	L	L
		⋮						⋮				
H	H	H	H	H	L	L	L	L	H	H	H	L

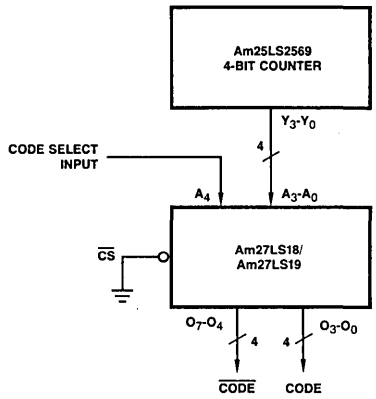
ASCII PAPER TAPE



BPM-025

APPLYING THE Am27LS18 AND Am27LS19

The Am27LS18 and Am27LS19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am27LS18 or Am27LS19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.



BPM-026

TRUTH TABLE

ADDRESS					COMPLEMENT				TRUE				
A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE
0	0	0	0	1	1	0	1	1	0	1	0	0	
0	0	0	1	0	1	0	1	0	0	1	0	1	
0	0	0	1	1	1	0	0	1	0	1	1	0	
0	0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	0	1	0	1	1	1	1	0	0	0	
0	0	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	1	1	0	1	0	1	1	0	1	0	
0	1	0	0	0	0	1	0	0	1	0	1	1	
0	1	0	0	1	0	0	1	1	1	1	0	0	
0	1	0	1	0	X	X	X	X	X	X	X	X	
0	1	0	1	1	X	X	X	X	X	X	X	X	
0	1	1	0	0	X	X	X	X	X	X	X	X	
0	1	1	0	1	X	X	X	X	X	X	X	X	
0	1	1	1	0	X	X	X	X	X	X	X	X	
0	1	1	1	1	X	X	X	X	X	X	X	X	
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE
1	0	0	0	1	1	1	1	0	0	0	0	1	
1	0	0	1	0	1	1	0	0	0	0	1	1	
1	0	0	1	1	1	1	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	1	0	1	1	0	
1	0	1	0	1	1	0	0	0	0	1	1	1	
1	0	1	1	0	1	0	1	0	0	1	0	1	
1	0	1	1	1	1	0	1	1	0	1	0	0	
1	1	0	0	0	0	0	1	1	1	1	0	0	
1	1	0	0	1	0	0	1	0	1	1	0	1	
1	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	0	1	1	0	0	0	1	1	1	1	0	
1	1	1	0	0	0	1	0	1	1	0	1	0	
1	1	1	0	1	0	1	0	0	1	0	1	1	
1	1	1	1	0	0	1	1	0	1	0	0	1	
1	1	1	1	1	0	1	1	1	1	0	0	0	

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H* Unipak Rev H* (Code 16 02)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27LS18/19	715-1407-1	PA 16-6 and 32 x 8(L)	IM 32 x 8-16-AMD	SA 3-1 B 32 x 8/16	DIS-156 AM	DA-22	AM110

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
55ns	AM27LS18PC	AM27LS19PC	P-16-1	C-1	COM'L
	AM27LS18PCB	AM27LS19PCB	P-16-1	B-1	
	AM27LS18DC	AM27LS19DC	D-16-1	C-1	
	AM27LS18DCB	AM27LS19DCB	D-16-1	B-1	
	AM27LS18LC	AM27LS19LC	L-20-1	C-1	
	AM27LS18LCB	AM27LS19LCB	L-20-1	B-1	
75ns	AM27LS18DM	AM27LS19DM	D-16-1	C-3	MIL
	AM27LS18DMB	AM27LS19DMB	D-16-1	B-3	
	AM27LS18FM	AM27LS19FM	F-16-1	C-3	
	AM27LS18FMB	AM27LS19FMB	F-16-1	B-3	
	AM27LS18LM	AM27LS19LM	L-20-1	C-3	
	AM27LS18LMB	AM27LS19LMB	L-20-1	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27S20A • Am27S21A
Am27S20 • Am27S21

1024-Bit Generic Series Bipolar PROM
(256 x 4 bits with ultra fast access time)

"A" VERSION ADVANCED INFORMATION

2

DISTINCTIVE CHARACTERISTICS

- High Speed – 30ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- *Common Generic PROM series electrical characteristics* and simple programming procedures
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

The Am27S20A/20 and Am27S21A/21 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

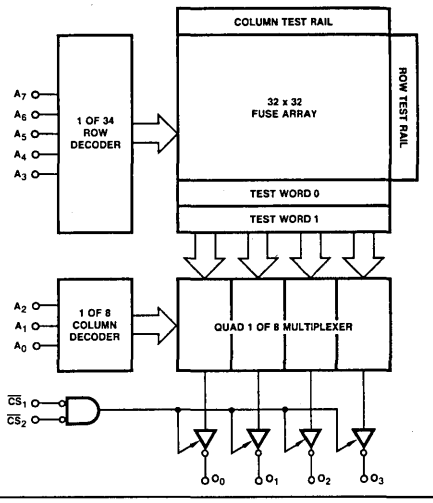
Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

FUNCTIONAL DESCRIPTION

The Am27S20A/20 and Am27S21A/21 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 256 x 4 configuration, they are available in both open collector Am27S20A/20 and three-state Am27S21A/21 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_7 and holding chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, at a logic LOW. If either chip select input goes to a logic HIGH, O_0-O_3 go to the OFF or high impedance state.

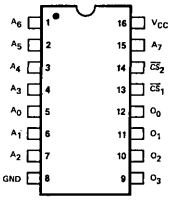
BLOCK DIAGRAM



BPM-027

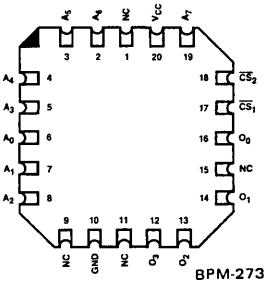
CONNECTION DIAGRAMS – Top Views

DIP



BPM-029

Chip-Pak™ L-20-1



BPM-273

Note: Pin 1 is marked for orientation.

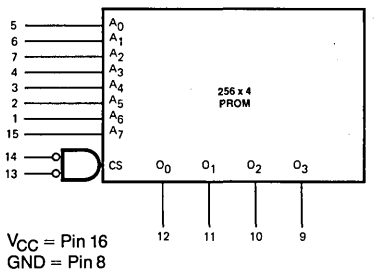
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

BPM-028

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V			25	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX		100	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS}_1}$ = 2.4V (Note 2), V_O = 4.5V			40	μA
		V_{CC} = MAX, $V_{\overline{CS}_1}$ = 2.4V (Note 2), V_O = 2.4V			40	μA
		V_{CC} = MAX, $V_{\overline{CS}_1}$ = 2.4V (Note 2), V_O = 0.4V			−40	μA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)		8		pF

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

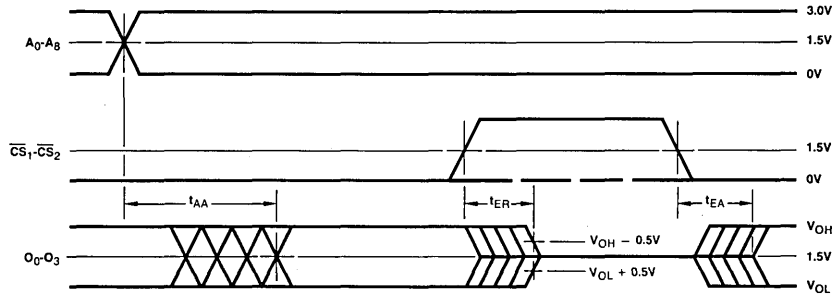
SWITCHING CHARACTERISTICS OVER OPERATING RANGE
"A" VERSION ADVANCED INFORMATION

Parameter	Description	Test Conditions	Typ 5V 25°C A	Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	20	25	30	45	40	60	ns
t_{EA}	Enable Access Time		15	15	20	20	25	30	ns
t_{ER}	Enable Recovery Time		15	15	20	20	25	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

2

SWITCHING WAVEFORMS



Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

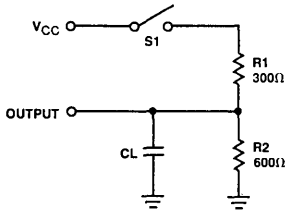
BPM-030

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-031

PROGRAMMING

The Am27S20A/20 and Am27S21A/21 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled, and the output level is sensed to determine if the link has opened. Most links will open within 50μsec. Occassionlly a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

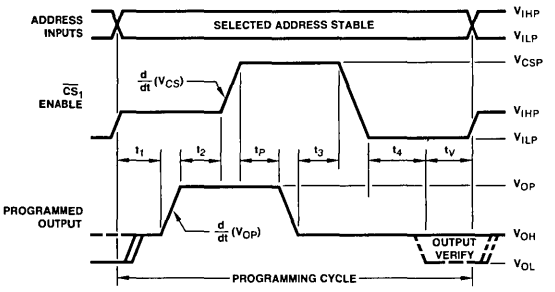
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

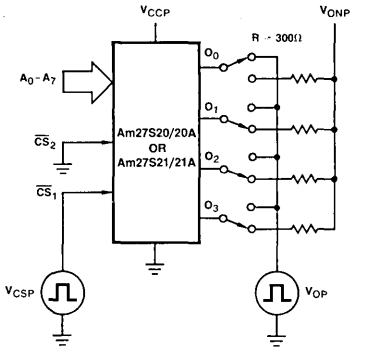
Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-032

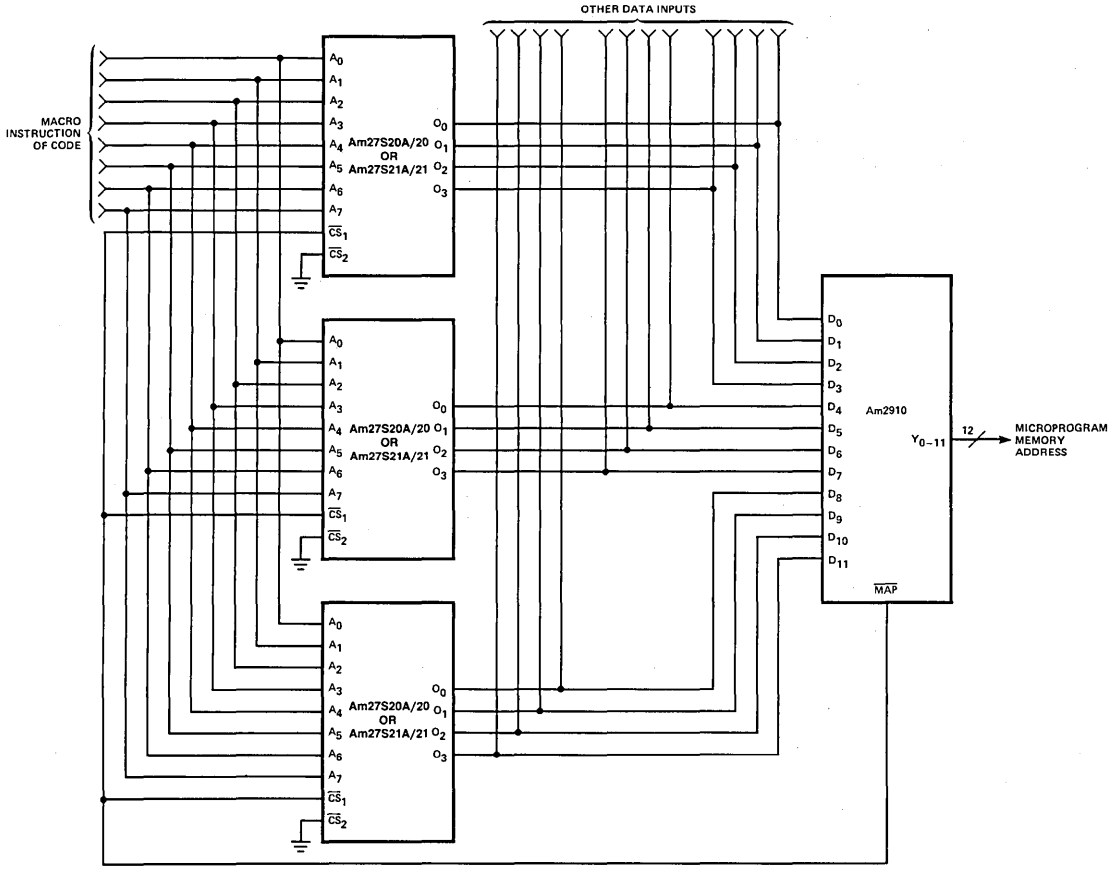
SIMPLIFIED PROGRAMMING DIAGRAM



BPM-274

APPLYING THE Am27S20A/20 AND Am27S21A/21

Typical application of the Am27S20A/20 and Am27S21A/21 is shown below. The Am27S20A/20 and the Am27S21A/21 are employed as mapping ROMs in a microprogram computer control unit. The eight-bit macroinstruction from main memory is brought into the A_0-A_7 inputs of the mapping ROM array. The instruction is mapped into a 12-bit address space with each PROM output supplying 4 bits. The 12 bits of address are then supplied to the "D" inputs of the Am2910 as a possible next address source for microprogram memory. The $\overline{MAP}$ output of the Am2910 is connected to the $\overline{CS}_1$ input of the Am27S20A/20/21A/21 such that when the $\overline{CS}_1$ input is HIGH, the outputs of the PROMs are either HIGH in the case of the Am27S20A/20 or in the three-state mode in the case of the Am27S21A/21. In both cases the $\overline{CS}_2$ input is grounded; thus data from other sources are free to drive the D inputs of the Am2910 when $\overline{MAP}$ is HIGH.



MICROPROGRAMMING INSTRUCTION MAPPING BPM-275

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S20A/21A Am27S20/21	715-1408-1	PA 16-5 and 256 x 4(L)	IM 256 x 4-16 AMD	SA 4-2	DIS-133 AM	DA 21	AM130-2

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
30ns	AM27S20APC	AM27S21APC	P-16-1	C-1	COM'L
	AM27S20APCB	AM27S21APCB	P-16-1	B-1	
	AM27S20ADC	AM27S21ADC	D-16-1	C-1	
	AM27S20ADCB	AM27S21ADCB	D-16-1	B-1	
	AM27S20ALC	AM27S21ALC	L-20-1	C-1	
	AM27S20ALCB	AM27S21ALCB	L-20-1	B-1	
40ns	AM27S20ADM	AM27S21ADM	D-16-1	C-3	MIL
	AM27S20ADMB	AM27S21ADMB	D-16-1	B-3	
	AM27S20AFM	AM27S21AFM	F-16-1	C-3	
	AM27S20AFMB	AM27S21AFMB	F-16-1	B-3	
	AM27S20ALM	AM27S21ALM	L-20-1	C-3	
	AM27S20ALMB	AM27S21ALMB	L-20-1	B-3	
45ns	AM27S20PC	AM27S21PC	P-16-1	C-1	COM'L
	AM27S20PCB	AM27S21PCB	P-16-1	B-1	
	AM27S20DC	AM27S21DC	D-16-1	C-1	
	AM27S20DCB	AM27S21DCB	D-16-1	B-1	
	AM27S20LC	AM27S21LC	L-20-1	C-1	
	AM27S20LCB	AM27S21LCB	L-20-1	B-1	
60ns	AM27S20DM	AM27S21DM	D-16-1	C-3	MIL
	AM27S20DMB	AM27S21DMB	D-16-1	B-3	
	AM27S20FM	AM27S21FM	F-16-1	C-3	
	AM27S20FMB	AM27S21FMB	F-16-1	B-3	
	AM27S20LM	AM27S21LM	L-20-1	C-3	
	AM27S20LMB	AM27S21LMB	L-20-1	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am29760A • Am29761A

1024-Bit Generic Series Bipolar PROM

Refer to

Am27S20 • Am27S21

Bipolar Memory PROM Product Specification

The Am29760A is replaced by the Am27S20 (open collector).

The Am29761A is replaced by the Am27S21 (three-state).

Am27S12A • Am27S13A
Am27S12 • Am27S13

2048-Bit Generic Series Bipolar PROM
(512 x 4 bits with ultra fast access time)

"A" VERSION ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- High Speed – 30ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

The Am27S12A/12 and Am27S13A/13 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

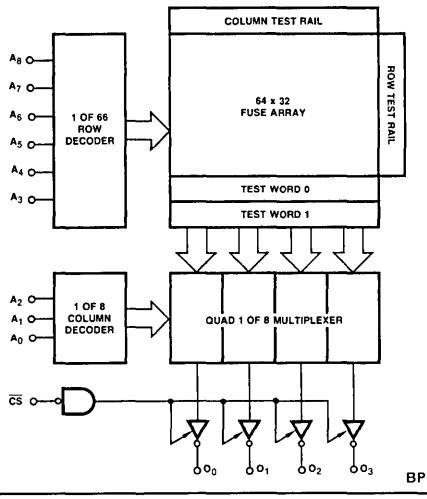
Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

FUNCTIONAL DESCRIPTION

The Am27S12A/12 and Am27S13A/13 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 4 configuration, they are available in both open collector Am27S12A/12 and three-state Am27S13A/13 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_8 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the off or high impedance state.

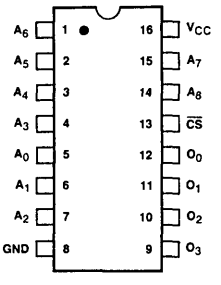
BLOCK DIAGRAM



BPM-001

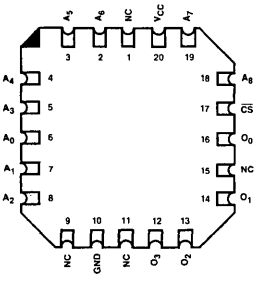
CONNECTION DIAGRAMS – Top Views

DIP



BPM-003

Chip-Pak™ L-20-1



BPM-263

Note: Pin 1 is marked for orientation.

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

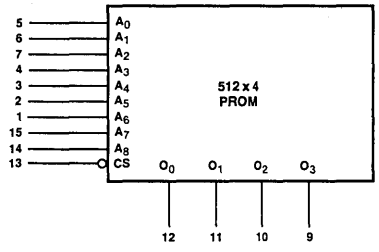
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

BPM-002

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}					0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					25	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX				100	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $\overline{CS}$ = 2.4V		V_O = 4.5V			40	μA
			(Note 2)	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)				4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)				8		

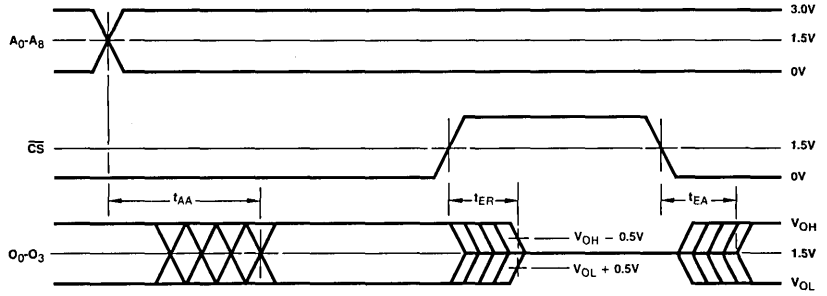
Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE "A" VERSION ADVANCED INFORMATION

Parameter	Description	Test Conditions	Typ 5V 25°C A	Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	20	30	30	50	40	60	ns
t_{EA}	Enable Access Time		15	15	20	25	25	30	ns
t_{ER}	Enable Recovery Time		15	15	20	25	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

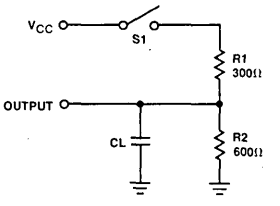
BPM-004

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-005

PROGRAMMING

The Am27S12A/12 and Am27S13A/13 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{CS}$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

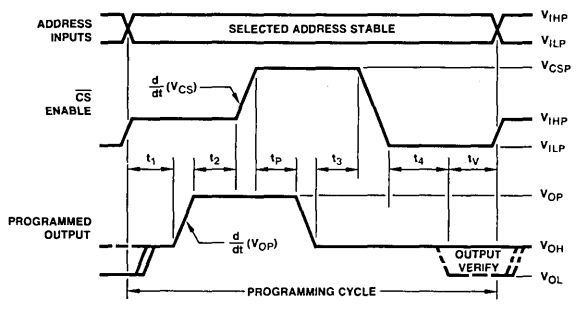
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

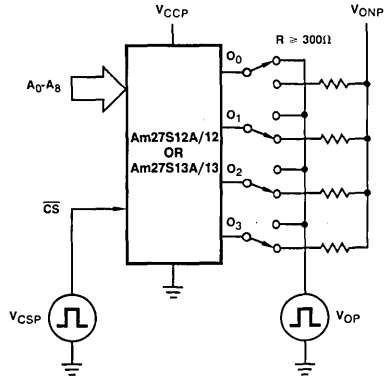
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-006

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-264

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S12A/13A Am27S12/13	715-1408-2	PA 16-5 and 512 x 4(L)	IM 512 x 4-16-AMD	SA 4-1	DIS-134 AM	DA-21	AM130-3

*Rev shown is minimum approved revision.

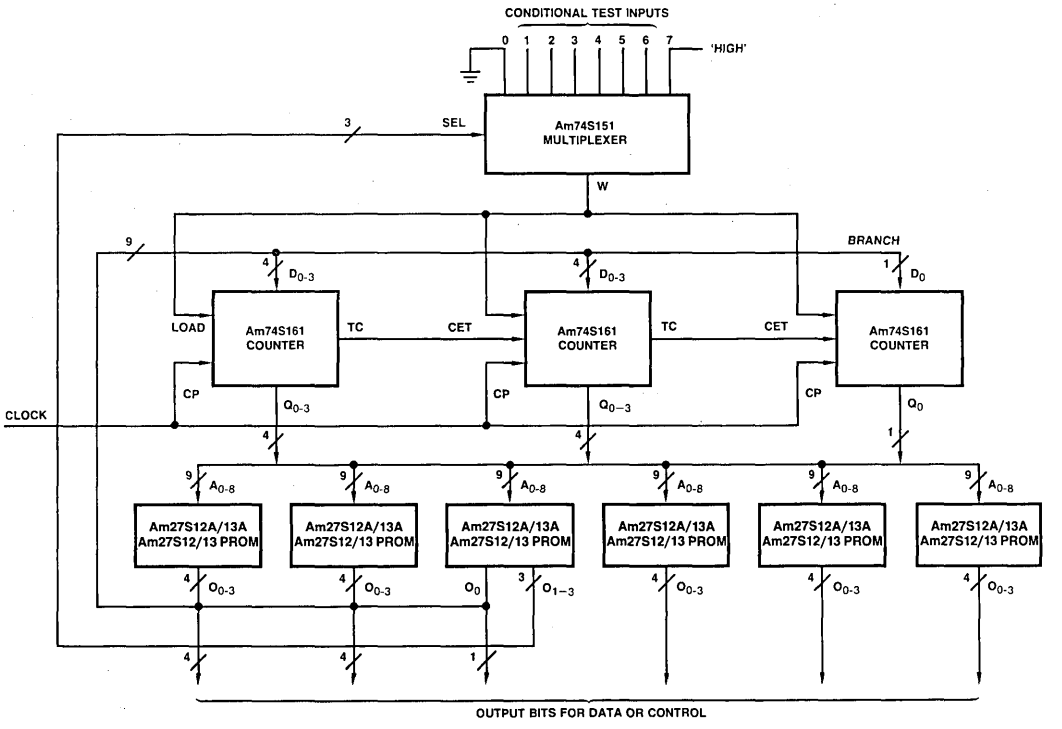
OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

APPLYING THE Am27S12A/12 AND Am27S13A/13

The Am27S12A/12 and Am27S13A/13 can be used with a high speed counter to form a pico-controller for microprogrammed systems. A typical application is illustrated below wherein a multiplexer, under control of one of the PROMs, is continuously sensing the CONDITIONAL TEST INPUTS. When the selected condition occurs, a HIGH signal will result at the multiplexer output causing a predetermined branch address to be loaded into the parallel inputs of the counters on the next clock pulse. The counter then accesses the preprogrammed data or control information sequence from the Am27S12A/12 or Am27S13A/13 PROMs.



BPM-009

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
30ns	AM27S12APC	AM27S13APC	P-16-1	C-1	COM'L
	AM27S12APCB	AM27S13APCB	P-16-1	B-1	
	AM27S12ADC	AM27S13ADC	D-16-1	C-1	
	AM27S12ADCB	AM27S13ADCB	D-16-1	B-1	
	AM27S12ALC	AM27S13ALC	L-20-1	C-1	
	AM27S12ALCB	AM27S13ALCB	L-20-1	B-1	
40ns	AM27S12ADM	AM27S13ADM	D-16-1	C-3	MIL
	AM27S12ADMB	AM27S13ADMB	D-16-1	B-3	
	AM27S12AFM	AM27S13AFM	F-16-1	C-3	
	AM27S12AFMB	AM27S13AFMB	F-16-1	B-3	
	AM27S12ALM	AM27S13ALM	L-20-1	C-3	
	AM27S12ALMB	AM27S13ALMB	L-20-1	B-3	
50ns	AM27S12PC	AM27S13PC	P-16-1	C-1	COM'L
	AM27S12PCB	AM27S13PCB	P-16-1	B-1	
	AM27S12DC	AM27S13DC	D-16-1	C-1	
	AM27S12DCB	AM27S13DCB	D-16-1	B-1	
	AM27S12LC	AM27S13LC	L-20-1	C-1	
	AM27S12LCB	AM27S13LCB	L-20-1	B-1	
60ns	AM27S12DM	AM27S13DM	D-16-1	C-3	MIL
	AM27S12DMB	AM27S13DMB	D-16-1	B-3	
	AM27S12FM	AM27S13FM	F-16-1	C-3	
	AM27S12FMB	AM27S13FMB	F-16-1	B-3	
	AM27S12LM	AM27S13LM	L-20-1	C-3	
	AM27S12LMB	AM27S13LMB	L-20-1	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am29770 • Am29771

2048-Bit Generic Series Bipolar PROM

Refer to

Am27S12 • Am27S13

Bipolar Memory PROM Product Specification

The Am29770 is replaced by the Am27S12 (open collector).

The Am29771 is replaced by the Am27S13 (three-state).

Am27S15

4096-Bit Generic Series Bipolar PROM (512 x 8 Bits with Output Data Latches)

DISTINCTIVE CHARACTERISTICS

- On-chip data latches
- Latched true and complemented output enables for easy word expansion
- Predetermined OFF outputs on power-up
- Plug-in replacement for the 82S115
- Fast access time – 60ns commercial and 90ns military maximum
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

FUNCTIONAL DESCRIPTION

The Am27S15 is an electrically programmable Schottky read only memory incorporating on-chip data and enable latches. The device is organized as 512 words of 8 bits and features three-state outputs with full 16mA drive capability.

When in the transparent mode, with the strobe (ST) input HIGH, reading stored data is accomplished by enabling the chip ($\overline{E}_1$ LOW and E_2 HIGH) and applying the binary word address to the address inputs, A_0-A_8. In this mode, changes of the address inputs cause the outputs, Q_0-Q_7, to read a different stored word; changes of either enable input level disable the outputs, causing them to go to the high impedance state.

Dropping the strobe input to the LOW level places the device in the latched mode of operation. The output condition present (reading a word of stored data or disabled) when the strobe goes LOW remains at the outputs, regardless of further address or enable transitions, until a positive (LOW to HIGH) strobe transition occurs. With the strobe HIGH, Q_0-Q_7 again respond to the address and enable input conditions.

If the strobe is LOW (latched mode) when V_{CC} power is first applied, the outputs will be in the disabled state, eliminating the need for special "power-up" design precautions.

GENERIC SERIES CHARACTERISTICS

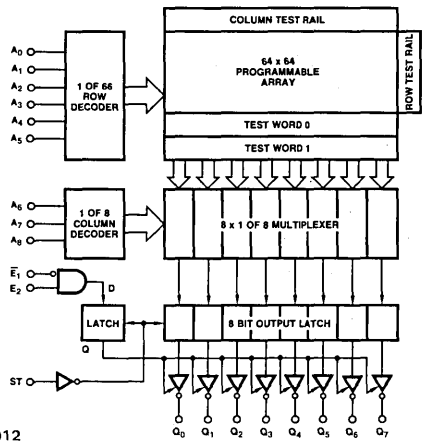
This 4K PROM is a member of an Advanced PROM series incorporating common electrical characteristics and programing procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

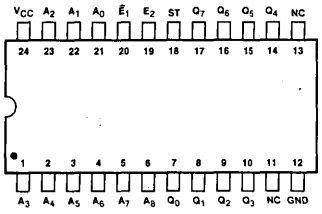
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

BLOCK DIAGRAM



BPM-012

CONNECTION DIAGRAM – Top View



BPM-011

Note: Pin 1 is marked for orientation. NC = No connection.

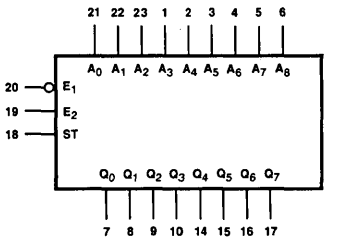
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5 to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12
(Pins 11 and 13 open)

BPM-010

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA, V_{IN} = V_{IH} or V_{IL}	COM'L	2.7			Volts
			MIL	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)	COM'L			0.85	Volts
			MIL			0.80	
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V	COM'L			−0.100	mA
			MIL			−0.150	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				25	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	COM'L	−20		−70	mA
			MIL	−15		−65	
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = MAX	COM'L		125	175	mA
			MIL		125	185	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $\overline{VE_1}$ = 2.4V, VE_2 = 0.4V	V_O = 4.5V			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			12		

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

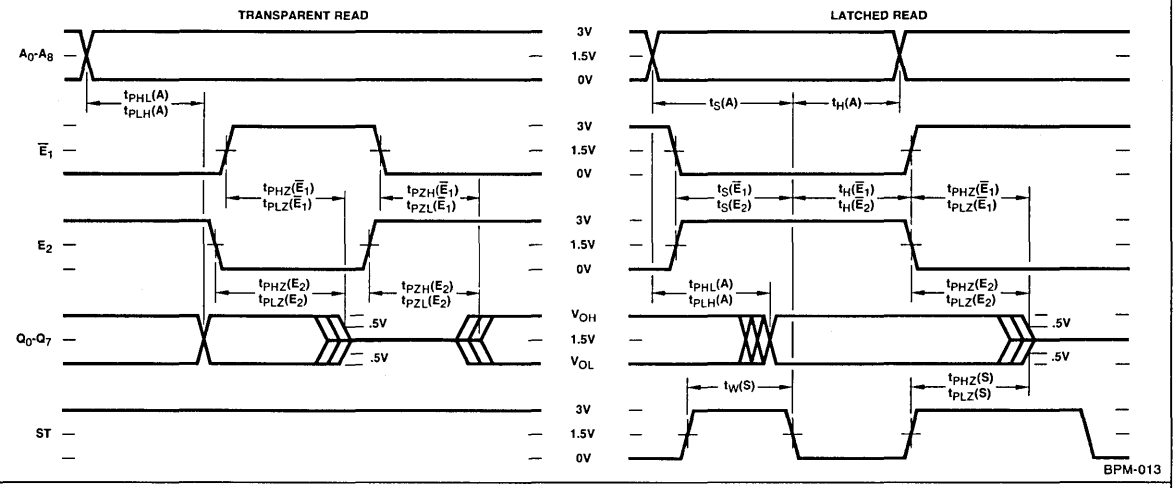
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions	Typ. (Note 1)	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
$t_{PHL}(A)$ $t_{PLH}(A)$	Transparent Mode Address to Output Access Time	C_L = 30pF S_1 Closed (See AC Test Load Below)	35		60		90	ns
$t_W(S)$	Strobe Pulse Width (HIGH)		10	30		40		ns
$t_S(A)$	Address to Strobe (LOW) Set-up Time		35	60		90		ns
$t_H(A)$	Address to Strobe (LOW) Hold Time		−10	0		5		ns
$t_S(\overline{E}_1)$ $t_S(E_2)$	Enable to Strobe (LOW) Set-up Time			40		50		ns
$t_H(\overline{E}_1)$ $t_H(E_2)$	Enable to Strobe (LOW) Hold Time		0	10		10		ns
$t_{PZH}(\overline{E}_1,E_2)$ $t_{PZL}(\overline{E}_1,E_2)$	Transparent Mode Enable to Output Enabled (HIGH or LOW) Time	C_L = 30pF S_1 Closed for t_{PZL}, & Open for t_{PZH}	20		40		50	ns
$t_{PHZ}(S)$ $t_{PLZ}(S)$	Strobe Delatch (HIGH) to Output Disabled (OFF or HIGH impedance) Time	C_L = 5pF (Note 2) S_1 closed for t_{PLZ} & Open for t_{PHZ}			35		45	ns
$t_{PHZ}(\overline{E}_1,E_2)$ $t_{PLZ}(\overline{E}_1,E_2)$	Transparent Mode Enable to Output Disabled (OFF or high impedance) Time		20		40		50	ns

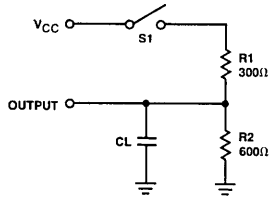
Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
3. Tests are performed with input rise and fall times (10% to 90%) of 5ns or less.

2

SWITCHING WAVEFORMS

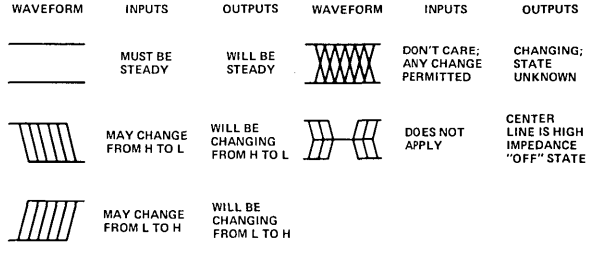


AC TEST LOAD



BPM-014

KEY TO TIMING DIAGRAM



PROGRAMMING

The Am27S15 is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}_1$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled and the output level sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

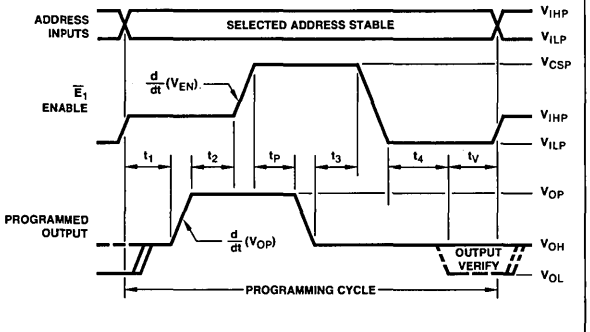
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{ENP}	$\overline{E}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0.0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}_1$ Voltage Change	100	1000	V/μsec
t_p	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

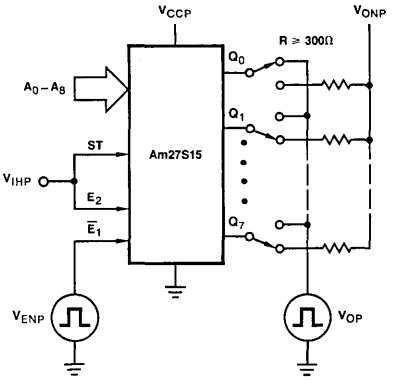
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-015

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-016

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260	
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev G* 919-1286-1 Rev G*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12
Am27S15	715-1411-1	PA 24-14 and 512 x 8(L)	IM 512 x 8-24-27S15-AMD	SA 17-3B 512 x 8/24	DIS-165 AMD	DA 33

*Rev shown is minimum approved revision.

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OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
60ns	AM27S15PC	P-24-1	C-1	COM'L
	AM27S15PCB	P-24-1	B-1	
	AM27S15DC	D-24-1	C-1	
	AM27S15DCB	D-24-1	B-1	
90ns	AM27S15DM	D-24-1	C-3	MIL
	AM27S15DMB	D-24-1	B-3	
	AM27S15FM	F-24-1	C-3	
	AM27S15FMB	F-24-1	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27S25A • Am27S25

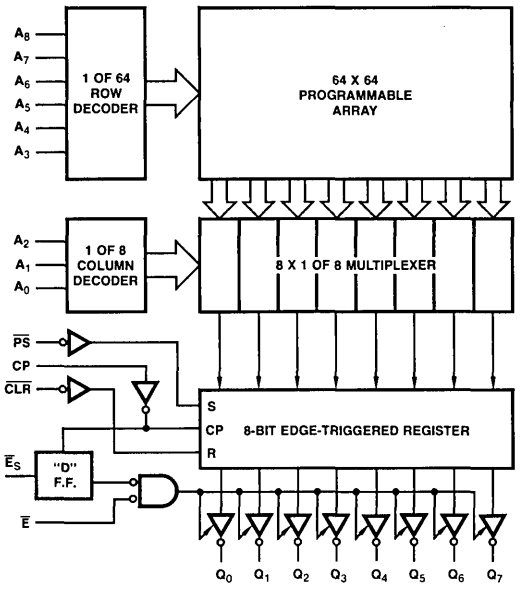
4K-Bit (512 x 8) Generic Series IMOX™ Bipolar High Performance Registered PROM with PRESET and CLEAR INPUTS

"A" VERSION ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Member of AMD's Generic Family of 8-bit wide registered PROMs
- On-chip edge-triggered registers – ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Buffered common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Standard version – 50ns max setup and 27ns max clock-to-output allows system speed improvements
- "A" version offers improved AC performance in critical paths (30ns max setup and 20ns max clock-to-output)
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ>98%)
- AC performance is factory tested utilizing programmed test words and columns
- 100% MIL-STD-883C processing
- Guaranteed to INT-STD-123

BLOCK DIAGRAM



BPM-330

FUNCTIONAL DESCRIPTION

The Am27S25A/25 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 512-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S25A/25 also offer maximum flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs (Q_0-Q_7) to be in the OFF or high-impedance state. Reading data is accomplished by first applying the binary word address to the address inputs (A_0-A_8) and a logic LOW to the synchronous enable ($\overline{E}_S$). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable ($\overline{E}$) is also LOW, stored data will appear on the outputs (Q_0-Q_7). If $\overline{E}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state regardless of the state of $\overline{E}$. The outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level. Following the positive clock edge the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively elimated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

The Am27S25 has buffered asynchronous $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs. These functions are common to all registers and are useful during power up timeout sequences. With outputs enabled the $\overline{\text{PS}}$ input asserted LOW will cause all outputs to be set to a logic 1 (HIGH) state. When the $\overline{\text{CLR}}$ input is LOW, the internal flip-flops of the data register are reset and, a logic 0 (LOW) will appear on all outputs. These functions will control the state of the data register, independent of all other inputs but exclusive of each other.

IMOX is a trademark of Advanced Micro Devices, Inc.

GENERIC SERIES CHARACTERISTICS

The Am27S25A/25 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming equipment) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields and produce excellent parametric correlation.

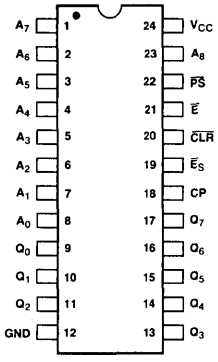
Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large nonconductive gaps that ensure long-term reliability. Extensive operating testing has shown that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage-compensated bias network to provide excellent parametric performance over the full military power supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

2

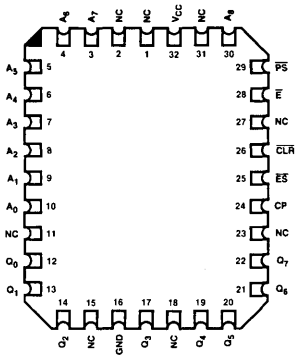
CONNECTION DIAGRAMS
Top Views

DIP



BPM-331

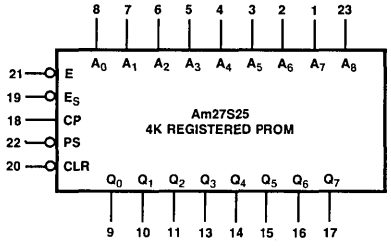
Chip-Pak™ L-32-2



BPM-332

Note: Pin 1 is marked for orientation.

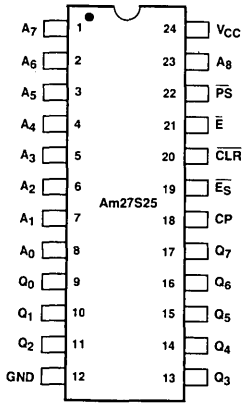
LOGIC SYMBOL



BPM-333

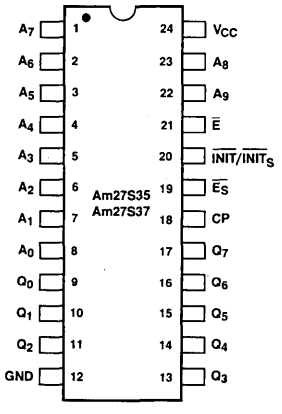
V_{CC} = Pin 24
GND = Pin 12

AMD's GENERIC FAMILY OF 8-WIDE REGISTERED PROMs



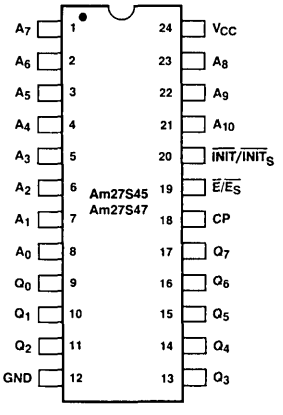
BPM-334

512 x 8



BPM-335

1024 x 8



BPM-336

2048 x 8

Note: Pin 1 is marked for orientation.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 3)		−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX			120	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $V_{\overline{E}}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 4)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 4)			12		pF

Notes: 1. Typical values are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

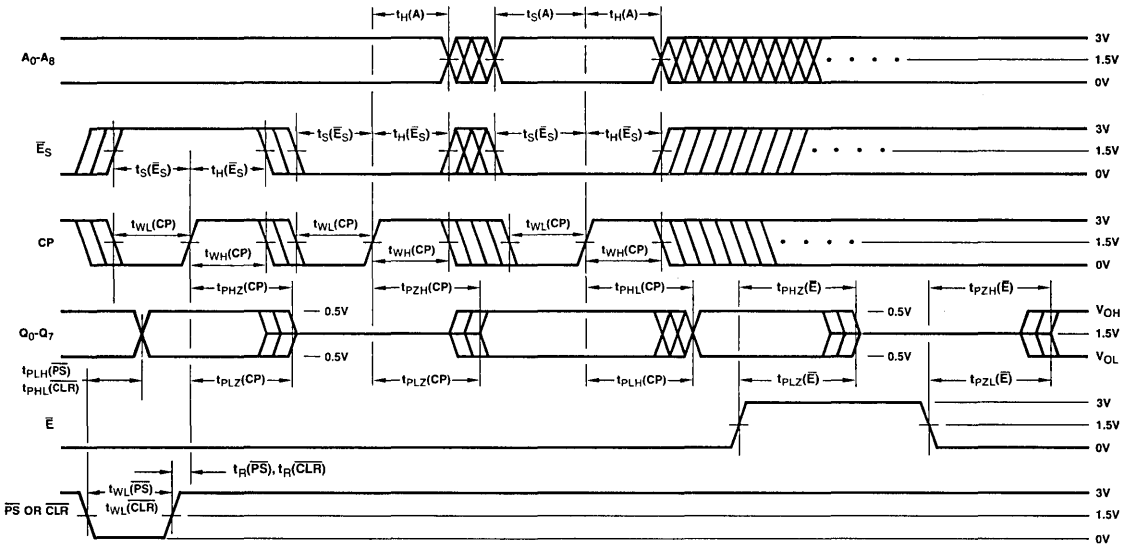
SWITCHING CHARACTERISTICS OVER OPERATING RANGE (See Notes on Testing)
'A' VERSION ADVANCE INFORMATION

Parameters	Description		Typ (Note 1)	Am27S25A COM'L Min	Am27S25A COM'L Max	Am27S25A MIL Min	Am27S25A MIL Max	Am27S25 COM'L Min	Am27S25 COM'L Max	Am27S25 MIL Min	Am27S25 MIL Max	Units
$t_S(A)$	Address to CP (HIGH) Setup Time		35	30		35		50		55		ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−10	0		0		0		0		ns
$t_{PHL}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)	All Outputs Simultaneous	15		20		25		27		30	ns
$t_{PLH}(CP)$		Single Output (Note 3)	13		15		20		23		26	
$t_{WH}(CP)$ / $t_{WL}(CP)$	CP Width (HIGH or LOW)			20		20		20		20		ns
$t_S(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Setup Time		5	10		15		10		15		ns
$t_H(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Hold Time		−2	5		5		5		5		ns
$t_{PHL}(\overline{CLR})$ / $t_{PLH}(\overline{PS})$	Delay from $\overline{PRESET}$ or $\overline{CLEAR}$ (LOW) to Outputs (LOW or HIGH)		16		20		25		25		30	ns
$t_R(\overline{PS})$ / $t_R(\overline{CLR})$	$\overline{PRESET}$ or $\overline{CLEAR}$ Recovery (Inactive) to CP (HIGH)		10	20		25		20		25		ns
$t_{WL}(\overline{PS})$ / $t_{WL}(\overline{CLR})$	$\overline{PRESET}$ or $\overline{CLEAR}$ Pulse Width		10	20		25		30		25		ns
$t_{PZL}(CP)$ / $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW)		18		25		30		35		45	ns
$t_{PZL}(\overline{E})$ / $t_{PZH}(\overline{E})$	Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW)		15		25		30		35		45	ns
$t_{PLZ}(CP)$ / $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or High Impedance) (Note 4)		21		25		30		35		45	ns
$t_{PLZ}(\overline{E})$ / $t_{PHZ}(\overline{E})$	Delay from E_1 (HIGH) to Inactive Output (OFF or High Impedance) (Note 4)		15		25		30		35		45	ns

Notes: 1. Typical values are at V_{CC} = 5.0V and T_A = 25°C.
2. Tests are performed with input 10 to 90% rise and fall times of 5ns or less.
3. Single register performance numbers provided for comparison with discrete register test data.
4. t_{PHZ} and t_{PLZ} are measured to the V_{OH} −0.5V and V_{OL} +0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.

SWITCHING WAVEFORMS

(See Notes on Testing)



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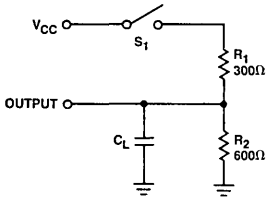
NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any test.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

AC TEST LOAD



BPM-338

Notes: 1. C_L = 50pF for all switching characteristics except t_{PLZ} and t_{PHZ}.
2. C_L = 5pF for t_{PLZ} and t_{PHZ}.
3. S_1 is closed for all tests except for t_{PZH} and t_{PHZ}.
4. All device test loads should be located within 2" of device outputs.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
——— ———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

PROGRAMMING

The Am27S25A/25 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip enabled, and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

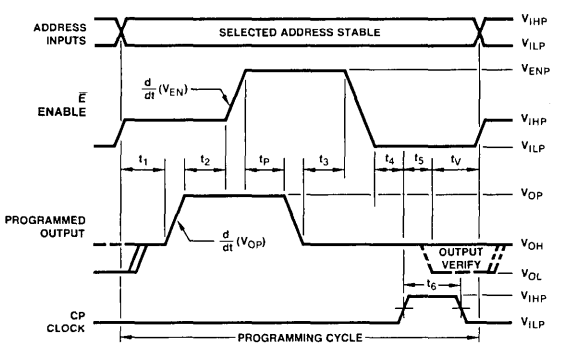
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{ENP}}$	$\overline{E}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{EN}})/dt$	Rate of $\overline{E}$ Voltage Change	50	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

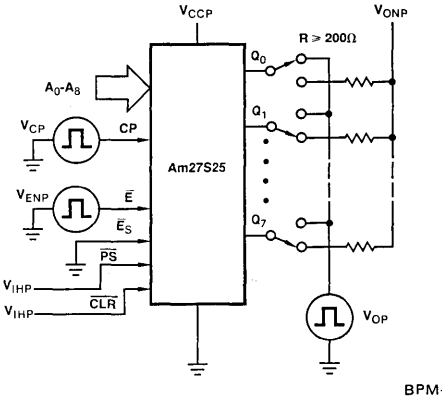
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_7 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-339

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-340

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 735 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev G* 919-1286-1 Rev G* Unipak Rev H 003 (Code 62 65)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Socket Adapters Am27S25	715-1617	PA 24-16 and 512 x 8(L)	IM 512 x 8-27S25 AMD	SA 31-2 B 512 x 8/24	DIS-213 AM	DA 31-5	AM 190-2

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

Speed Selection (Setup Time)	Order Code	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
30ns	AM27S25APC	P-24-1AA (Note 4)	C-1	COM'L
	AM27S25APCB	P-24-1AA (Note 4)	B-1	
	AM27S25ADC	D-24-1AA	C-1	
	AM27S25ADCB	D-24-1AA	B-1	
	AM27S25ALC	L-32-2	C-1	
	AM27S25ALCB	L-32-2	B-1	
35ns	AM27S25ADM	D-24-1AA	C-3	MIL
	AM27S25ADMB	D-24-1AA	B-3	
	AM27S25AFM	F-24-1	C-3	
	AM27S25AFMB	F-24-1	B-3	
	AM27S25ALM	L-32-2	C-3	
	AM27S25ALMB	L-32-2	B-3	
50ns	AM27S25PC	P-24-1AA (Note 4)	C-1	COM'L
	AM27S25PCB	P-24-1AA (Note 4)	B-1	
	AM27S25DC	D-24-1AA	C-1	
	AM27S25DCB	D-24-1AA	B-1	
	AM27S25LC	L-32-2	C-1	
	AM27S25LCB	L-32-2	B-1	
55ns	AM27S25DM	D-24-1AA	C-3	MIL
	AM27S25DMB	D-24-1AA	B-3	
	AM27S25FM	F-24-1	C-3	
	AM27S25FMB	F-24-1	B-3	
	AM27S25LM	L-32-2	C-3	
	AM27S25LMB	L-32-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. This package will be available soon. Consult Factory.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

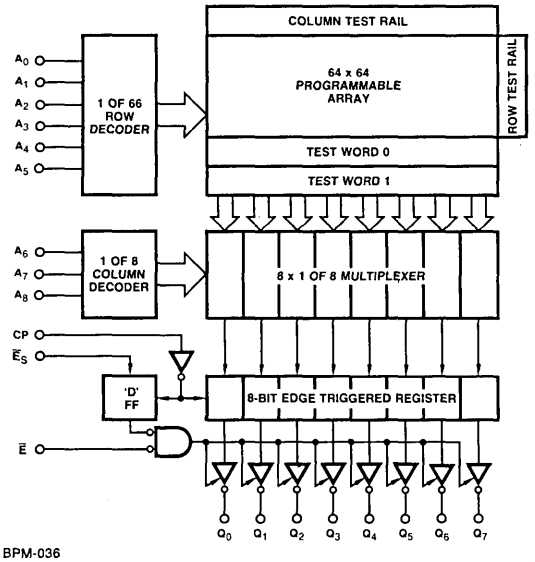
Am27S27

4096-Bit Generic Series Bipolar Registered PROM (512 x 8 Bits with D-Type Output Data Register)

DISTINCTIVE CHARACTERISTICS

- On-chip edge triggered registers – Ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up
- Fast 55ns address setup and 27ns clock to output times
- Excellent performance over the military range
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

BLOCK DIAGRAM



BPM-036

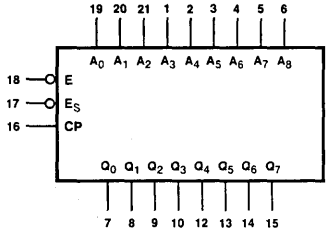
FUNCTIONAL DESCRIPTION

The Am27S27 is a 512 word x 8-bit PROM which incorporates an on-chip D-type, master-slave data register with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost of pipelined microprogrammed system and other designs wherein accessed PROM data is temporarily stored in a register. The Am27S27 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs, Q_0-Q_7, to be in the OFF or high impedance state, eliminating the need for a register clear input. Reading data is accomplished by first applying the binary word address to the address inputs, A_0-A_8, and a logic LOW to the synchronous output enable, $\overline{E}_S$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, CP, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{E}$, is also LOW, stored data will appear on the outputs, Q_0-Q_7. If $\overline{E}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. The outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip, edge triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

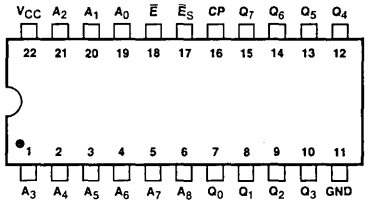
LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

BPM-037

CONNECTION DIAGRAM
Top View



BPM-038

Note: Pin 1 is marked for orientation.

GENERIC SERIES CHARACTERISTICS

The Am27S27 is a member of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 11) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	250mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}		0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		130	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $\overline{VE}$ = 2.4V; V_O = 4.5V			40	μA
		V_{CC} = MAX., $\overline{VE}$ = 2.4V; V_O = 0.4V			−40	μA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)		5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)		12		pF

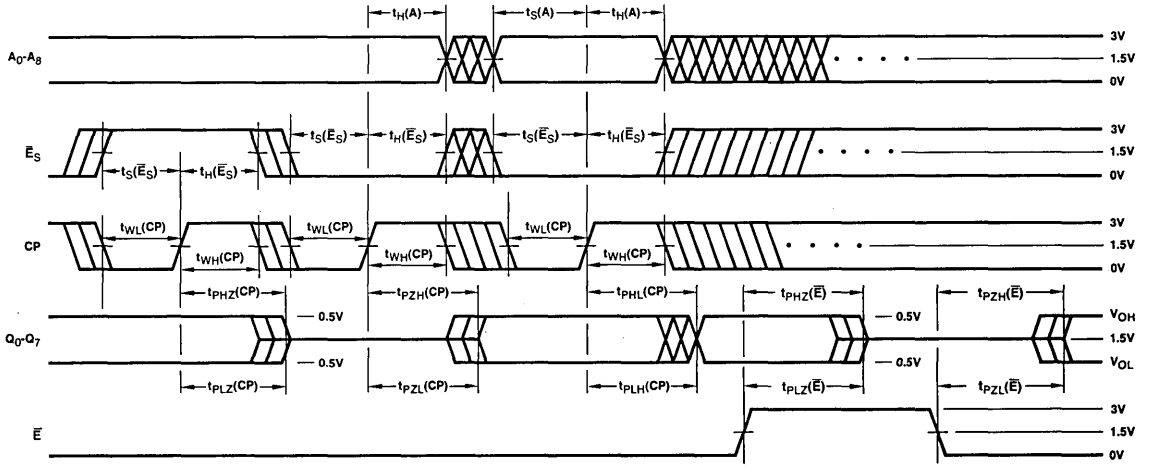
Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions	Typ 5V 25°C	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_S(A)$	Address to CP (HIGH) Setup Time	C_L = 30pF S_1 closed. (See AC Test Load below)	40	55		65		ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−15	0		0		ns
$t_{PHL}(CP)$ $t_{PLH}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)		15		27		30	ns
$t_{WH}(CP)$ $t_{WL}(CP)$	CP Width (HIGH or LOW)		10	30		40		ns
$t_S(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Setup Time		10	25		30		ns
$t_H(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Hold Time		−10	0		0		ns
$t_{PZL}(CP)$ $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW)	C_L = 30pF S_1 closed for t_{PZL} and open for t_{PZH}	15		35		45	ns
$t_{PZL}(\overline{E})$ $t_{PZH}(\overline{E})$	Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW)		15		40		45	ns
$t_{PLZ}(CP)$ $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or High Impedance)	C_L = 5pF (Note 1) S_1 closed for t_{PLZ} and open for t_{PHZ}	15		35		45	ns
$t_{PLZ}(\overline{E})$ $t_{PHZ}(\overline{E})$	Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or High Impedance)		10		30		40	ns

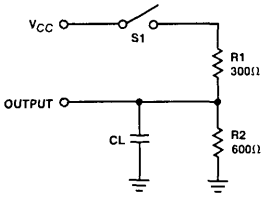
Notes: 1. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
2. Tests are perfomed with input 10% to 90% rise and fall times of 5ns or less.

SWITCHING WAVEFORMS

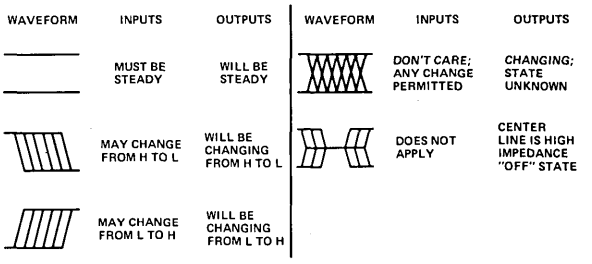


BPM-039

AC TEST LOAD



KEY TO TIMING DIAGRAM



BPM-040

PROGRAMMING

The Am27S27 is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

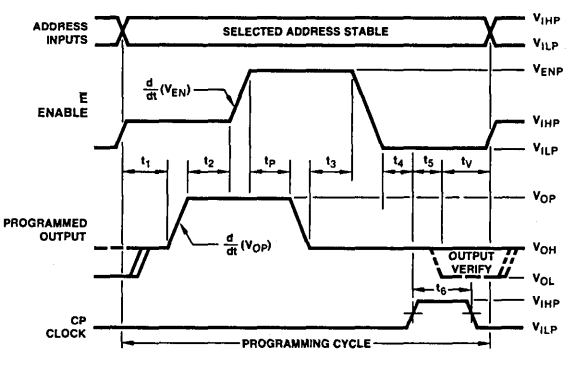
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	V
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	V
V_{ILP}	Input LOW Level During Programming	0.0	0.45	V
V_{ENP}	$\overline{E}$ Voltage During Programming	14.5	15.5	V
V_{OP}	Output Voltage During Programming	19.5	20.5	V
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	V
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}$ Voltage Change	50	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

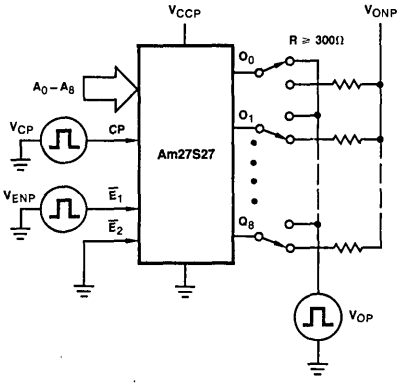
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-041

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-042

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260	
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev G* 919-1286-1 Rev G*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12
Am27S27	715-1412-2	PA 22-4 and 512 x 8(L)	IM 512 x 8-22-27S27-AMD	SA 18 B 512 x 8/22	DIS-168 AMD	DA 28

*Rev shown is minimum approved revision.

2

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ORDERING INFORMATION

Speed Selection ($t_S(A)$)	Order Code	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
55ns	AM27S27PC AM27S27PCB AM27S27DC AM27S27DCB	P-22-1 P-22-1 D-22-1 D-22-1	C-1 B-1 C-1 B-1	COM'L
65ns	AM27S27DM AM27S27DMB	D-22-1 D-22-1	C-3 B-3	MIL

Notes: 1. P = Molded DIP, D = Hermetic DIP. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am29775

4096-Bit Generic Series Bipolar PROM with Register

Refer to

Am27S27

Bipolar Memory PROM Product Specification

The Am29775 is replaced by the Am27S27 (three-state).

Am27S28A • Am27S29A
Am27S28 • Am27S29

4096-Bit Generic Series Bipolar PROM
(512 x 8 bits with ultra fast access time)
"A" VERSION – ADVANCED INFORMATION

2

DISTINCTIVE CHARACTERISTICS

- High Speed – 35ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

The Am27S28A/28 and Am27S29A/29 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test rows are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

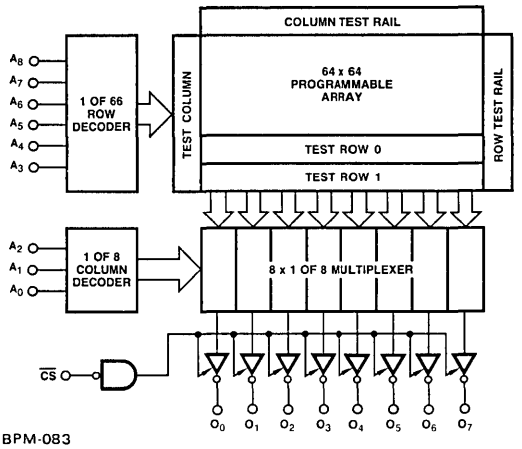
Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

FUNCTIONAL DESCRIPTION

The Am27S28A/28 and Am27S29A/29 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 8 configuration, they are available in both open collector Am27S28A/28 and three-state Am27S29A/29 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_8 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_7 go to the off or high impedance state.

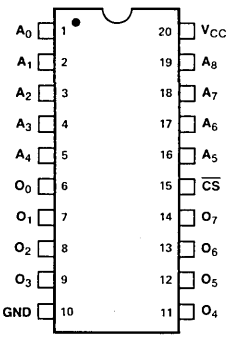
BLOCK DIAGRAM



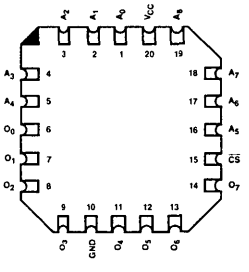
BPM-083

CONNECTION DIAGRAMS – Top Views

DIP



Chip-Pak™ L-20-1



Note: Pin 1 is marked for orientation.

BPM-085 BPM-286

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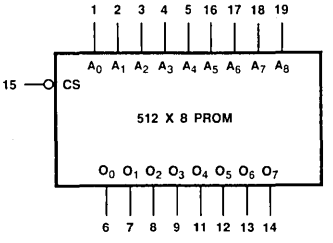
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

BPM-084

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}					0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					25	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX				105	160	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $V_{\overline{CS}}$ = 2.4V		V_O = 4.5V			40	μA
			(Note 2)	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)				4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)				8		

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

"A" VERSION ADVANCED INFORMATION

Parameter	Description	Test Conditions	Typ 5V 25°C A	Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	30	35	35	55	45	70	ns
t_{EA}	Enable Access Time		12	15	20	25	25	30	ns
t_{ER}	Enable Recovery Time		12	15	20	25	25	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three-state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

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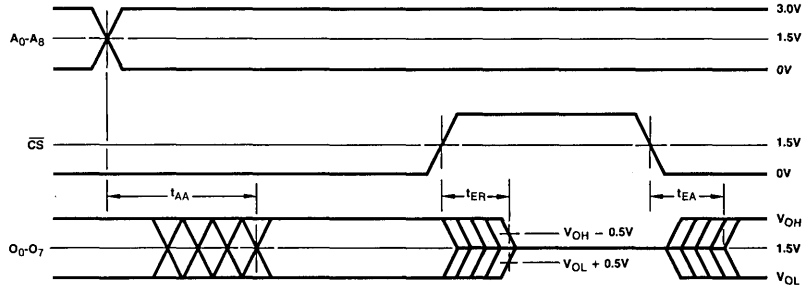
SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

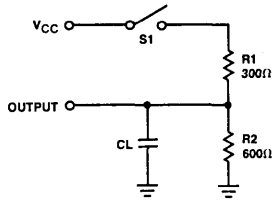
BPM-086

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
——— ———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-087

PROGRAMMING

The Am27S28A/28 and Am27S29A/29 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

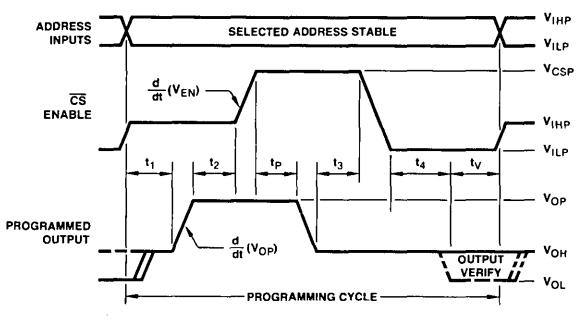
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0.0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	v/μsec
t_p	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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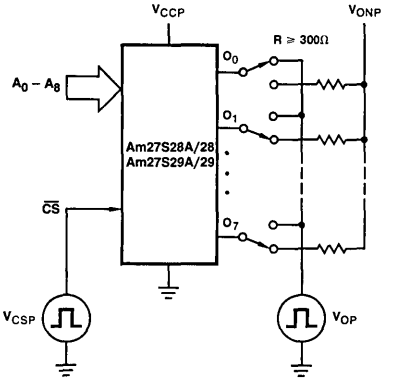
SIMPLIFIED PROGRAMMING DIAGRAM



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PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S28A/29A Am27S28/29	715-1413	PA 20-4 and 512 x 8 (L)	IM 512 x 8-20-AMD	SA 6	DIS-158 AM	DA-34	AM120-3

*Rev shown is minimum approved revision.

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OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
40ns	AM27S28APC	AM27S29APC	P-20-1	C-1	COM'L
	AM27S28APCB	AM27S29APCB	P-20-1	B-1	
	AM27S28ADC	AM27S29ADC	D-20-1	C-1	
	AM27S28ADCB	AM27S29ADCB	D-20-1	B-1	
	AM27S28ALC	AM27S29ALC	L-20-1	C-1	
	AM27S28ALCB	AM27S29ALCB	L-20-1	B-1	
50ns	AM27S28ADM	AM27S29ADM	D-20-1	C-3	MIL
	AM27S28ADMB	AM27S29ADMB	D-20-1	B-3	
	AM27S28ALM	AM27S29ALM	L-20-1	C-3	
	AM27S28ALMB	AM27S29ALMB	L-20-1	B-3	
55ns	AM27S28PC	AM27S29PC	P-20-1	C-1	COM'L
	AM27S28PCB	AM27S29PCB	P-20-1	B-1	
	AM27S28DC	AM27S29DC	D-20-1	C-1	
	AM27S28DCB	AM27S29DCB	D-20-1	B-1	
	AM27S28LC	AM27S29LC	L-20-1	C-1	
	AM27S28LCB	AM27S29LCB	L-20-1	B-1	
70ns	AM27S28DM	AM27S29DM	D-20-1	C-3	MIL
	AM27S28DMB	AM27S29DMB	D-20-1	B-3	
	AM27S28LM	AM27S29LM	L-20-1	C-3	
	AM27S28LMB	AM27S29LMB	L-20-1	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27S30A • Am27S31A
Am27S30 • Am27S31

4096-Bit Generic Series Bipolar PROM
(512 x 8 bits with ultra fast access time)

"A" VERSION ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- High Speed – 35ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

The Am27S30A/30 and Am27S31A/31 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test rows are preprogrammed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

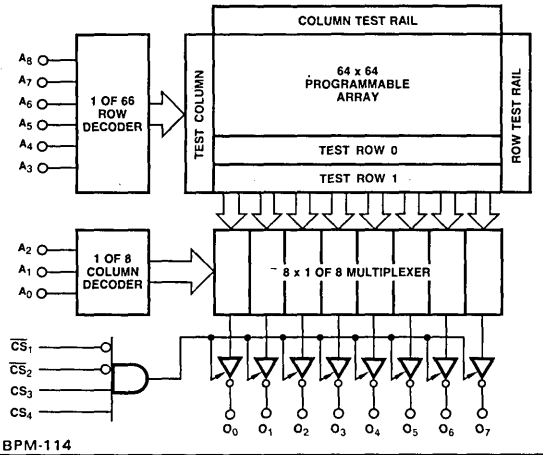
Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

FUNCTIONAL DESCRIPTION

The Am27S30A/30 and Am27S31A/31 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 8 configuration, they are available in both open collector Am27S30A/30 and three-state Am27S31A/31 output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_8 and holding $\overline{CS}_1$ and $\overline{CS}_2$ LOW and $\overline{CS}_3$ and CS_4 HIGH. All other valid input conditions on $\overline{CS}_1$, $\overline{CS}_2$, CS_3 and CS_4 place O_0-O_7 into the OFF or high impedance state.

BLOCK DIAGRAM



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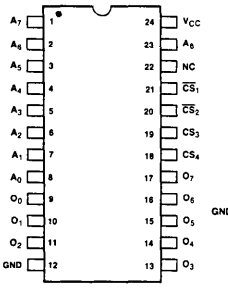
CONNECTION DIAGRAMS – Top Views

DIP



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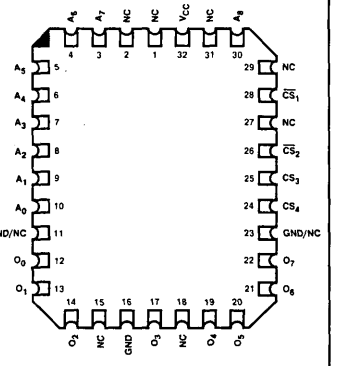
Chip-Pak™ L-32-2



Note: Pin 1 is marked for orientation.

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This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

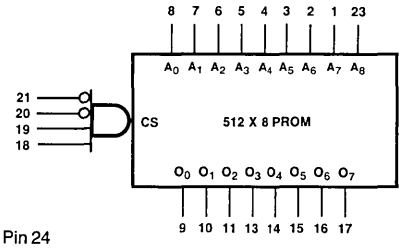
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12
(Pin 22 Open)

BPM-115

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}					0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					25	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX				115	175	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $V_{\overline{CS}_1}$ = 2.4V		V_O = 4.5V			40	μA
			(Note 2)	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)				4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)				8		

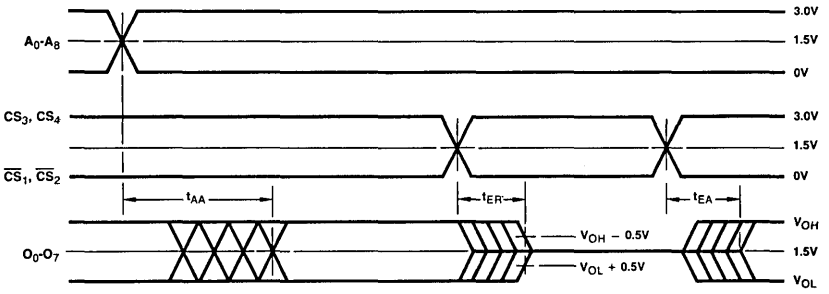
Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE
"A" VERSION ADVANCED INFORMATION

Parameter	Description	Test Conditions	Typ 5V 25°C A	Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	30	35	35	55	45	70	ns
t_{EA}	Enable Access Time		12	15	20	25	25	30	ns
t_{ER}	Enable Recovery Time		12	15	20	25	25	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while chip is disabled is determined externally.

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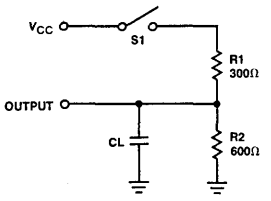
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
——— ———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-118

PROGRAMMING

The Am27S30A/30 and Am27S31A/31 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

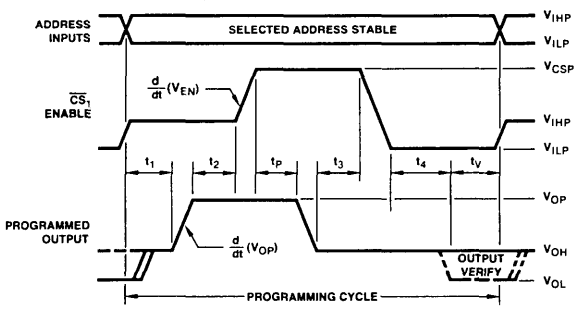
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0.0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{CS}_1$ Voltage Change	100	1000	V/μsec
t_p	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

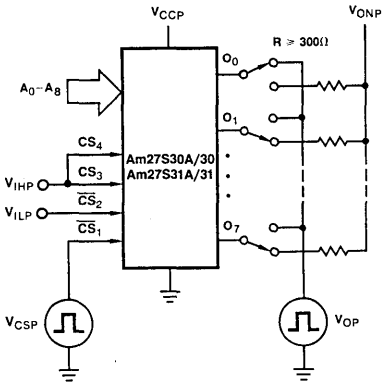
Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-119

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-262

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260	
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12
Am27S30A/31A Am27S30/31	715-1545	PA 24-13 and 512 x 8(L)	IM 512 x 8-24-AMD	SA 22-6	DIS-135 AM	DA 29

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
40ns	AM27S30APC	AM27S31APC	P-24-1AC	C-1	COM'L
	AM27S30APCB	AM27S31APCB	P-24-1AC	B-1	
	AM27S30ADC	AM27S31ADC	D-24-1AC	C-1	
	AM27S30ADCB	AM27S31ADCB	D-24-1AC	B-1	
	AM27S30ALC	AM27S31ALC	L-32-2	C-1	
	AM27S30ALCB	AM27S31ALCB	L-32-2	B-1	
50ns	AM27S30ADM	AM27S31ADM	D-24-1AC	C-3	MIL
	AM27S30ADMB	AM27S31ADMB	D-24-1AC	B-3	
	AM27S30AFM	AM27S31AFM	F-24-1	C-3	
	AM27S30AFMB	AM27S31AFMB	F-24-1	B-3	
	AM27S30ALM	AM27S31ALM	L-32-2	C-3	
	AM27S30ALMB	AM27S31ALMB	L-32-2	B-3	
55ns	AM27S30PC	AM27S31PC	P-24-1AC	C-1	COM'L
	AM27S30PCB	AM27S31PCB	P-24-1AC	B-1	
	AM27S30DC	AM27S31DC	D-24-1AC	C-1	
	AM27S30DCB	AM27S31DCB	D-24-1AC	B-1	
	AM27S30LC	AM27S31LC	L-32-2	C-1	
	AM27S30LCB	AM27S31LCB	L-32-2	B-1	
70ns	AM27S30DM	AM27S31DM	D-24-1AC	C-3	MIL
	AM27S30DMB	AM27S31DMB	D-24-1AC	B-3	
	AM27S30FM	AM27S31FM	F-24-1	C-3	
	AM27S30FMB	AM27S31FMB	F-24-1	B-3	
	AM27S30LM	AM27S31LM	L-32-2	C-3	
	AM27S30LMB	AM27S31LMB	L-32-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27S32A • Am27S33A
Am27S32 • Am27S33

4096-Bit Generic Series Bipolar PROM
(1024 x 4 bits with ultra fast access time)

2

DISTINCTIVE CHARACTERISTICS

- High Speed – 35ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

The Am27S32A/32 and Am27S33A/33 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

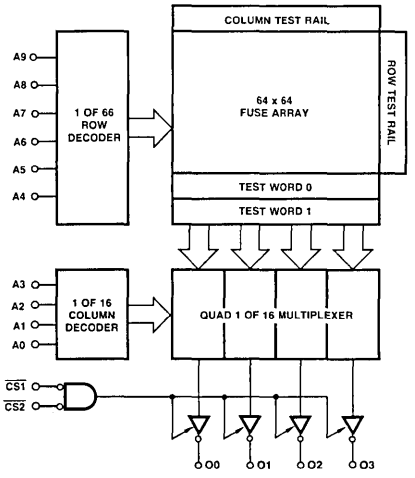
Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

FUNCTIONAL DESCRIPTION

The Am27S32A/32 and Am27S33A/33 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 4 configuration, they are available in both open collector Am27S32A/32 and three-state Am27S33A/33 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_9 and holding the chip select input, $\overline{CS_1}$, and $\overline{CS_2}$ LOW. If either chip select input goes to a logic HIGH, O_0-O_3 go to the off or high impedance state.

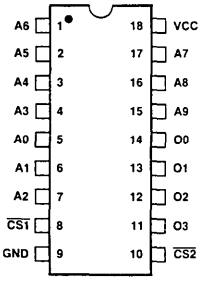
BLOCK DIAGRAM



BPM-090

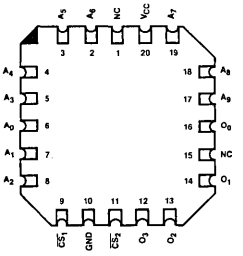
CONNECTION DIAGRAMS
Top Views

DIP



BPM-092

Chip-Pak™ L-20-1



Note: Pin 1 is marked for orientation.

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Chip-Pak is a trademark of Advanced Micro Devices, Inc.

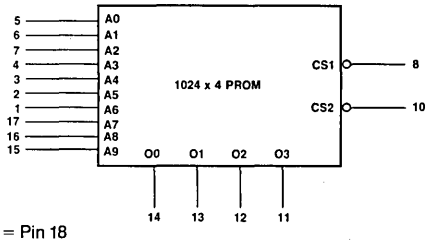
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +VCC max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	250mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

BPM-091

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA, V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA, V_{IN} = V_{IH} or V_{IL}				0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				25	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)		−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	COM'L		105	140	mA
			MIL		105	145	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS_1}}$ = 2.4V	V_O = 4.5V			40	μA
			(Note 2) V_O = 2.4V			40	
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)			12		

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

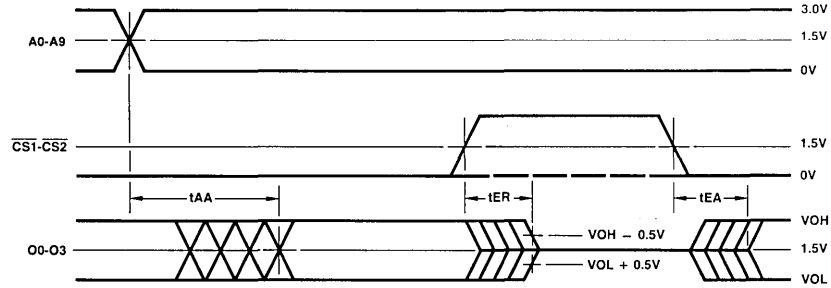
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions	Typ 5V 25°C A	Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	25	38	35	55	45	70	ns
t_{EA}	Enable Access Time		18	20	25	25	30	30	ns
t_{ER}	Enable Recovery Time		18	20	25	25	30	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

2

SWITCHING CHARACTERISTICS



Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

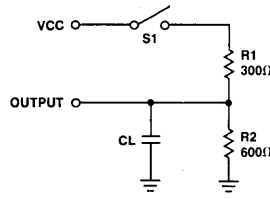
BPM-093

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
▨	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-094

PROGRAMMING

The Am27S32A/32 and Am27S33A/33 are manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including VCC should be removed for a period of 5 seconds after which programming may be resumed.

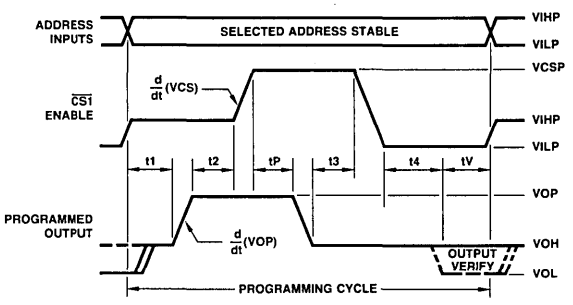
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min	Max	Units
VCCP	VCC During Programming	5.0	5.5	Volts
VIHP	Input HIGH Level During Programming	2.4	5.5	Volts
VILP	Input LOW Level During Programming	0.0	0.45	Volts
VCSP	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
VOP	Output Voltage During Programming	19.5	20.5	Volts
VONP	Voltage on Outputs. Not to be Programmed	0	VCCP+0.3	Volts
IONP	Current into Outputs. Not to be Programmed		20	mA
d(VOP)/dt	Rate of Output Voltage Change	20	250	V/μsec
d(VCS)/dt	Rate of $\overline{CS}_1$ Voltage Change	100	1000	V/μsec
tP	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5	15	msec

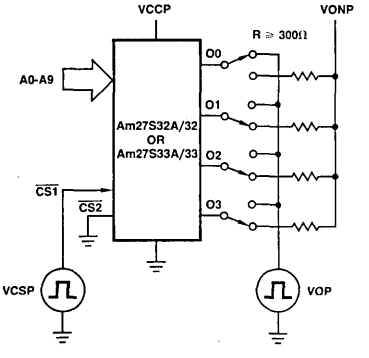
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e. not to the midpoints.
2. Delays t1, t2, t3 and t4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During tv, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to VONP through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-095

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-291

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S32A/33A Am27S32/33	715-1414	PA 18-6 and 1024 x 4(L)	IM 1024 x 4-18-AMD	SA 24	DIS 136 AM	DA 38	AM170-2

*Rev shown is minimum approved revision.

2

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

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35ns	AM27S32APC	AM27S33APC	P-18-1	C-1	COM'L
	AM27S32APCB	AM27S33APCB	P-18-1	B-1	
	AM27S32ADC	AM27S33ADC	D-18-1	C-1	
	AM27S32ADCB	AM27S33ADCB	D-18-1	B-1	
	AM27S32ALC	AM27S33ALC	L-20-1	C-1	
	AM27S32ALCB	AM27S33ALCB	L-20-1	B-1	
45ns	AM27S32ADM	AM27S33ADM	D-18-1	C-3	MIL
	AM27S32ADMB	AM27S33ADMB	D-18-1	B-3	
	AM27S32ALM	AM27S33ALM	L-20-1	C-3	
	AM27S32ALMB	AM27S33ALMB	L-20-1	B-3	
55ns	AM27S32PC	AM27S33PC	P-18-1	C-1	COM'L
	AM27S32PCB	AM27S33PCB	P-18-1	B-1	
	AM27S32DC	AM27S33DC	D-18-1	C-1	
	AM27S32DCB	AM27S33DCB	D-18-1	B-1	
	AM27S32LC	AM27S33LC	L-20-1	C-1	
	AM27S32LCB	AM27S33LCB	L-20-1	B-1	
70ns	AM27S32DM	AM27S33DM	D-18-1	C-3	MIL
	AM27S32DMB	AM27S33DMB	D-18-1	B-3	
	AM27S32LM	AM27S33LM	L-20-1	C-3	
	AM27S32LMB	AM27S33LMB	L-20-1	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Flat packages are available upon special request. Consult factory.

Am27S65 • Am27S75 • Am27S85

Generic Series 4-Wide Bipolar IMOX™ Registered PROMs with SSR™ Diagnostics Capability

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

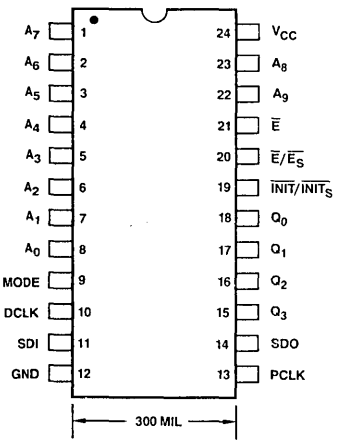
- On-chip edge-triggered registers – ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register for serial observability and controllability of the output register
- High speed – 25ns address setup and 15ns clock to output delay
- Programmable synchronous and asynchronous enables
- Optional synchronous or asynchronous $\overline{\text{INITIALIZE}}$
- Increased drive capability, 24mA I_{OL} COM'L
- THINDIP, 24-pin, 300-mil lateral center package increases overall board density
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ >98%)
- AC performance is factory tested utilizing programmed test words and columns
- 100% MIL-STD-883C processing
- Guaranteed to INT-STD-123

SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS CAPABILITIES

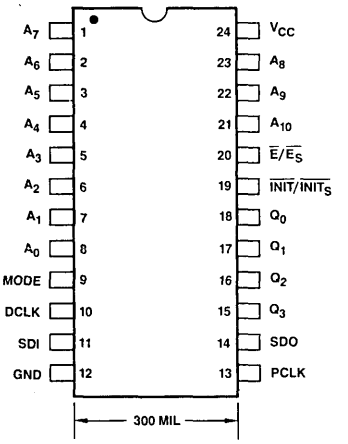
- Serial access to output register to allow input of diagnostic control information
- Serial access of output register allows observation of register data
- Eliminates the need for diagnostics code internal to the PROM, allowing increased applications code density
- Simplified diagnostics increases system reliability
- Separate diagnostic register allows real time "snap shot" of machine state

4-WIDE REGISTERED PROMs WITH SSR DIAGNOSTICS CONNECTION DIAGRAMS

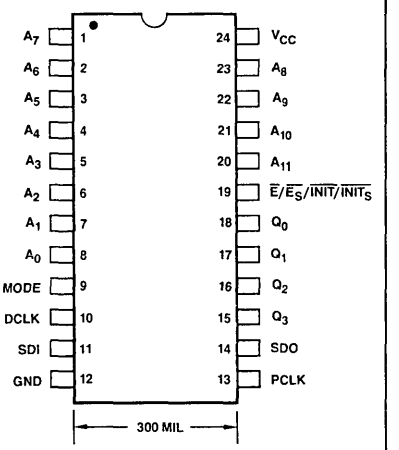
Am27S65 (1K x 4)



Am27S75 (2K x 4)



Am27S85 (4K x 4)



Note: Pin 1 is marked for orientation.

BPM-341

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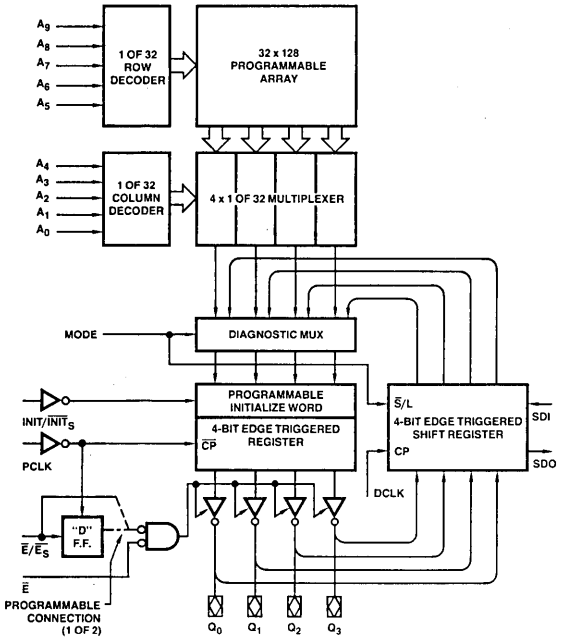
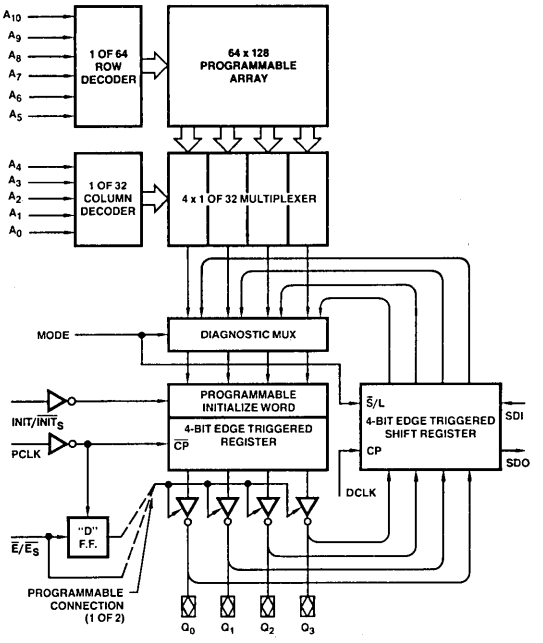
BLOCK DIAGRAMS

Am27S65



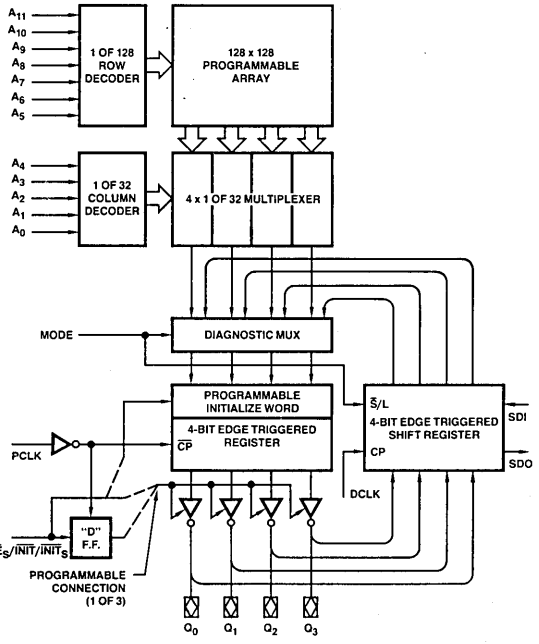
BPM-342

Am27S75



BPM-343

Am27S85



BPM-344

Am27S35A • Am27S35
Am27S37A • Am27S37

8K-Bit (1024 x 8) Generic Series IMOX™
Bipolar High Performance Registered PROM with Programmable INITIALIZE

DISTINCTIVE CHARACTERISTICS

- Member of AMD's Generic Family of 8-bit wide registered PROMs
- On-chip edge-triggered registers – ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Versatile programmable register $\overline{\text{INITIALIZE}}$ either asynchronous (Am27S35A/35) or synchronous (Am27S37A/37)
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Fast standard version – 40ns max setup and 25ns max clock-to-output allows system speed improvements
- "A" version offers improved AC performance in critical paths (35ns max setup and 20ns max clock-to-output)
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ>98%)
- AC performance is factory tested utilizing programmed test words and columns
- 100% MIL-STD-883C processing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

The Am27S35A/35 and Am27S37A/37 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

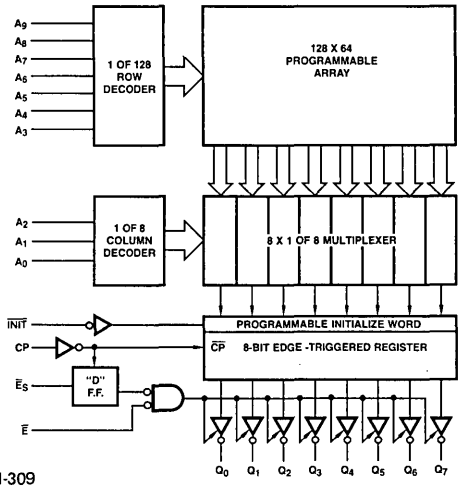
All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming equipment) these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to insure extremely high field programming yields and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large nonconductive gaps that ensure long-term reliability. Extensive operating testing has shown that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage-compensated bias network to provide excellent parametric performance over the full military power supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

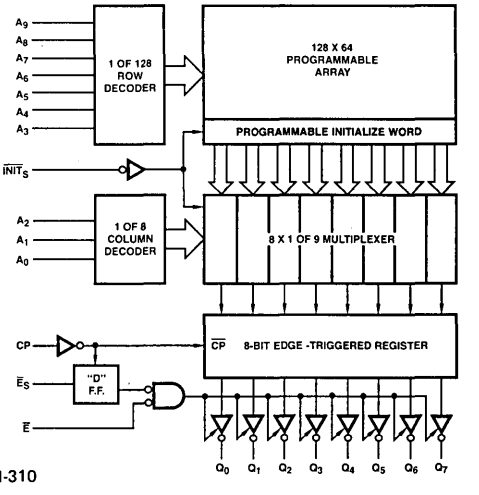
BLOCK DIAGRAMS

Am27S35



BPM-309

Am27S37



BPM-310

IMOX is a trademark of Advanced Micro Devices, Inc.

FUNCTIONAL DESCRIPTION

The Am27S35A/35 and Am27S37A/37 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 1024-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S35A/35 and Am27S37A/37 also offer maximum flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E_S}$) flip-flop will be in the set condition causing the outputs (Q_0-Q_7) to be in the OFF or high impedance state. Reading data is accomplished by first applying the binary word address to the address inputs (A_0-A_9) and a logic LOW to the synchronous enable ($\overline{E_S}$). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable ($\overline{E}$) is also LOW, stored data will appear on the outputs (Q_0-Q_7). If $\overline{E_S}$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state regardless of the value of $\overline{E}$. The outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level. Following the positive clock edge the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively elimated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

These devices also contain a built-in initialize function. When activated, the initialize control input ($\overline{INIT}$) causes the contents of an additional (1025th) 8-bit word to be loaded into the on-chip register.This extra word is user programmable. Since each bit is individually programmable, the initialize function can be used to load any desired combination of HIGHs and LOWs into the register. In the unprogrammed state, activating $\overline{INIT}$ will perform a register CLEAR (all outputs LOW). If all bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

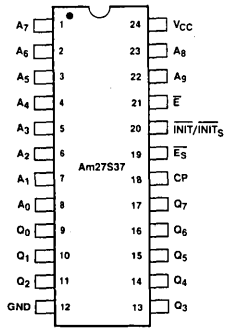
This ability to tailor the initialize outputs to the system requirements simplifies system design and enhances performance. The initialize function is useful during power up and timeout sequences. This flexible feature can also facilitate implementation of other sophisticated functions such as a built-in "jump-start" address.

The Am27S35A/35 has an asynchronous initialize input ($\overline{INIT}$). Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the slave flip-flops of the register independent of all other inputs(including CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

The Am27S37A/37 has a synchronous $\overline{INIT_S}$ input. Applying a LOW to the $\overline{INIT_S}$ input causes an immediate load of the programmed initialize word into the master flip-flops of the register only independent of all other inputs (including CP). To bring this data to the device outputs, the synchronous enable ($\overline{E_S}$) should be held LOW until the next LOW-to-HIGH transition of the clock (CP). Following this, the data will appear on the outputs after the asynchronous enable ($\overline{E}$) is brought LOW.

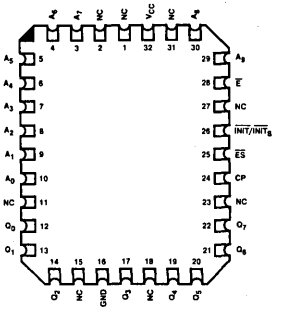
CONNECTION DIAGRAMS
Top Views

DIP



BPM-311

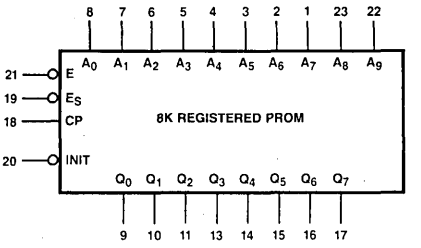
Chip-Pack™
L-32-2



BPM-312

Note: Pin 1 is marked for orientation.

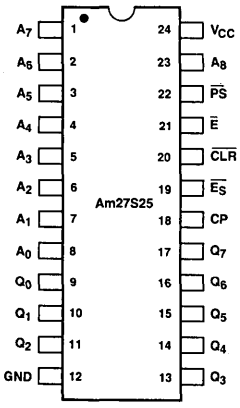
LOGIC SYMBOL



BPM-313

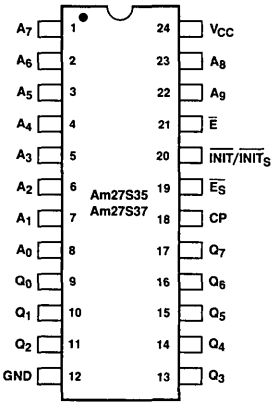
V_{CC}=Pin 24
GND=Pin 12

AMD's GENERIC FAMILY OF 8-WIDE REGISTERED PROMs



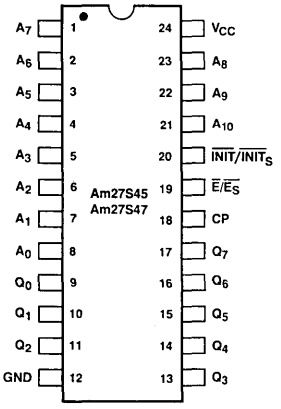
BMP-314

512 x 8



BPM-315

1024 x 8



BPM-316

2048 x 8

Note: Pin 1 is marked for orientation.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

2

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 3)		−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX			130	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $V_{\overline{E_1}}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 4)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 4)			12		

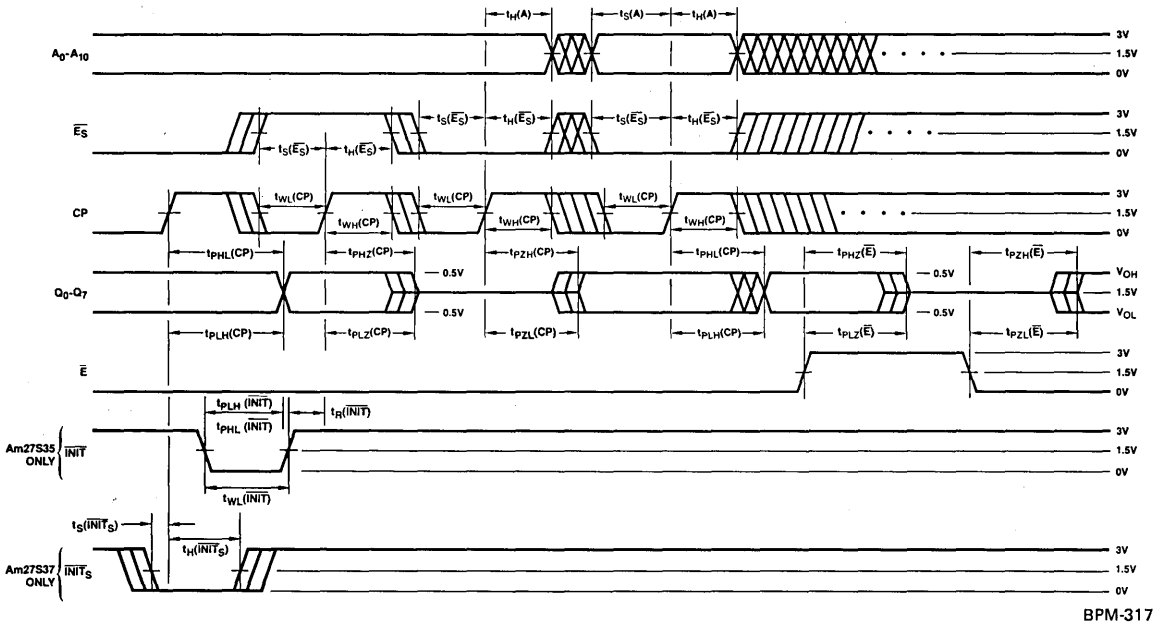
Notes: 1. Typical values are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (See Notes on Testing)

Parameters	Description		Typ (Note 1)	Am27S35A • Am27S37A COM'L Min	Am27S35A • Am27S37A COM'L Max	Am27S35A • Am27S37A MIL Min	Am27S35A • Am27S37A MIL Max	Am27S35 • Am27S37 COM'L Min	Am27S35 • Am27S37 COM'L Max	Am27S35 • Am27S37 MIL Min	Am27S35 • Am27S37 MIL Max	Units
$t_S(A)$	Address to CP (HIGH) Setup Time		25	35		40		40		45		ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−4	0		0		0		0		ns
$t_{PHL}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)	All Outputs Simultaneous	13		20		25		25		30	ns
$t_{PLH}(CP)$		Single Output (Note 3)	11		18		21		20		23	
$t_{WH}(CP)$ / $t_{WL}(CP)$	CP Width (HIGH or LOW)			20		20		20		20		ns
$t_S(\overline{E_S})$	$\overline{E_S}$ to CP (HIGH) Setup Time		5	15		15		15		15		ns
$t_H(\overline{E_S})$	$\overline{E_S}$ to CP (HIGH) Hold Time		−2	5		5		5		5		ns
$t_{PHL}(\overline{INIT})$ / $t_{PLH}(\overline{INIT})$	Delay from $\overline{INIT}$ (LOW) to Outputs (LOW or HIGH)	Am27S35 Only	20		30		35		35		40	ns
$t_R(\overline{INIT})$	$\overline{INIT}$ Recovery (Inactive) to CP (HIGH)		8	20		20		20		20		ns
$t_{WL}(\overline{INIT})$	$\overline{INIT}$ Pulse Width		10	25		30		25		30		ns
$t_S(\overline{INIT_S})$	$\overline{INIT_S}$ to CP (HIGH) Setup Time	Am27S37 Only	18	25		30		30		35		ns
$t_H(\overline{INIT_S})$	$\overline{INIT_S}$ to CP (HIGH) Hold Time		−5	0		0		0		0		ns
$t_{PZL}(CP)$ / $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW)		15		25		30		30		35	ns
$t_{PZL}(\overline{E})$ / $t_{PZH}(\overline{E})$	Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW)		15		25		30		30		35	ns
$t_{PLZ}(CP)$ / $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or High Impedance) (Note 4)		15		25		30		30		35	ns
$t_{PLZ}(\overline{E})$ / $t_{PHZ}(\overline{E})$	Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or High Impedance) (Note 4)		10		25		30		30		35	ns

Notes:
1. Typical values are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. Tests are performed with input 10 to 90% rise and fall times of 5ns or less.
3. Single register performance numbers provided for comparison with discrete register test data.
4. t_{PHZ} and t_{PLZ} are measured to the $V_{OH} - 0.5V$ and $V_{OL} + 0.5V$ output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.

SWITCHING WAVEFORMS
(See Notes on Testing)



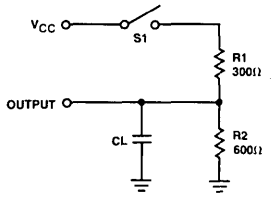
BPM-317

NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any test.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

AC TEST LOAD



BPM-040

Notes: 1. C_L = 50pF for all switching characteristics except t_{PLZ} and t_{PHZ}.
2. C_L = 5pF for t_{PLZ} and t_{PHZ}.
3. S_1 is closed for all tests except for t_{PZH} and t_{PHZ}.
4. All device test loads should be located within 2" of device outputs.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

PROGRAMMING

The Am27S35A/35 and Am27S37A/37 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}$ and $\overline{INIT}/\overline{INIT_S}$ inputs are at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip enabled, and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

The initialize word is programmed by setting the $\overline{INIT}/\overline{INIT_S}$ input to a logic LOW and programming the desired initialize word, output by output, in the same manner as any other address location. This is easily implemented by inverting the A_{10} address input from a PROM programmer and applying this signal to the $\overline{INIT}/\overline{INIT_S}$ input. Using this method the initialize word would be programmed as address 1024.

When $\overline{INIT}/\overline{INIT_S}$ is asserted LOW the internal programming circuitry for all other addresses is deselected.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

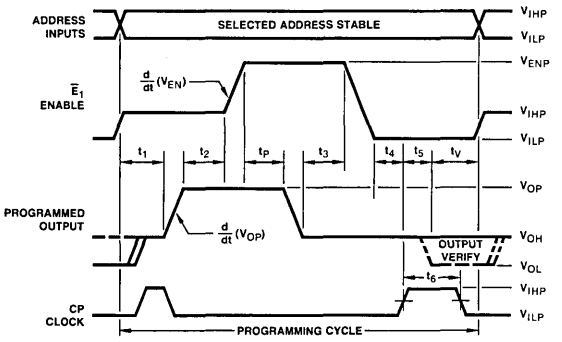
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{ENP}}$	$\overline{E}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{EN}})/dt$	Rate of $\overline{E}$ Voltage Change	50	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

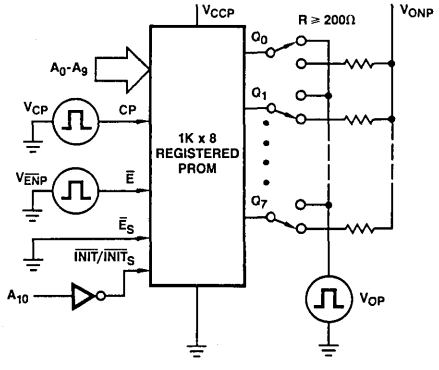
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_6 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-318

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-319

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev G* 919-1286-1 Rev G* Unipak Rev H 003 (Code 62 66)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Socket Adapters Am27S35 Am27S37	715-1723	PA 24-18 and 1025 x 8(L)	IM 1024 x 8-27S35/ 37-AMD	SA 31-1 B 1024 x 8/24	DIS-218 AM	DA 65	AM 190-3

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

Speed Selection (Setup Time)	Order Code: Asynchronous $\overline{\text{INITIALIZE}}$	Order Code: Synchronous $\overline{\text{INITIALIZE}}$	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM27S35APC	AM27S37APC	P-24-1AA (Note 4)	C-1	COM'L
	AM27S35APCB	AM27S37APCB	P-24-1AA (Note 4)	B-1	
	AM27S35ADC	AM27S37ADC	D-24-1AA	C-1	
	AM27S35ADCB	AM27S37ADCB	D-24-1AA	B-1	
	AM27S35ALC	AM27S37ALC	L-32-2	C-1	
	AM27S35ALCB	AM27S37ALCB	L-32-2	B-1	
40ns	AM27S35ADM	AM27S37ADM	D-24-1AA	C-3	MIL
	AM27S35ADMB	AM27S37ADMB	D-24-1AA	B-3	
	AM27S35AFM	AM27S37AFM	F-24-1	C-3	
	AM27S35AFMB	AM27S37AFMB	F-24-1	B-3	
	AM27S35ALM	AM27S37ALM	L-32-2	C-3	
	AM27S35ALMB	AM27S37ALMB	L-32-2	B-3	
40ns	AM27S35PC	AM27S37PC	P-24-1AA (Note 4)	C-1	COM'L
	AM27S35PCB	AM27S37PCB	P-24-1AA (Note 4)	B-1	
	AM27S35DC	AM27S37DC	D-24-1AA	C-1	
	AM27S35DCB	AM27S37DCB	D-24-1AA	B-1	
	AM27S35LC	AM27S37LC	L-32-2	C-1	
	AM27S35LCB	AM27S37LCB	L-32-2	B-1	
45ns	AM27S35DM	AM27S37DM	D-24-1AA	C-3	MIL
	AM27S35DMB	AM27S37DMB	D-24-1AA	B-3	
	AM27S35FM	AM27S37FM	F-24-1	C-3	
	AM27S35FMB	AM27S37FMB	F-24-1	B-3	
	AM27S35LM	AM27S37LM	L-32-2	C-3	
	AM27S35LMB	AM27S37LMB	L-32-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. This package will be available soon. Consult Factory.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27S180A • Am27S181A
Am27S280A • Am27S281A

Ultra Fast Access Time

Am27S180 • Am27S181
Am27S280 • Am27S281

Fast Access Time
1024 x 8 Bit Generic Series Bipolar IMOX™ PROM

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DISTINCTIVE CHARACTERISTICS

Part Number	Package Width	Other Features
Am27S180A	24-Pin, Plug in Replacement for Industry Standard 600-mil Configuration No Board Changes Required	Ultra fast – 35ns max
Am27S181A		
Am27S180		Fast – 60ns max
Am27S181		
Am27S280A	New Space-Saving 24-Pin, THINDIP, 300-mil Configuration Increases Overall Board Density	Ultra fast – 35ns max
Am27S281A		
Am27S280		Fast – 60ns max
Am27S281		

IMOX is a trademark of Advanced Micro Devices, Inc.

DISTINCTIVE CHARACTERISTICS

- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Members of Generic PROM series utilizing standard programming algorithm
- 100% processed to MIL-STD-883C
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

These 8K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming equipment) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

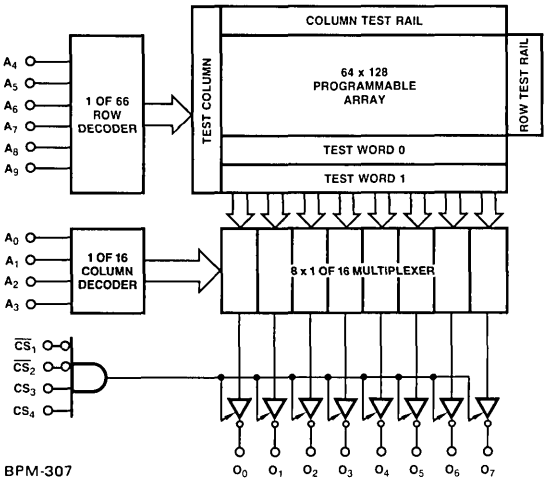
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

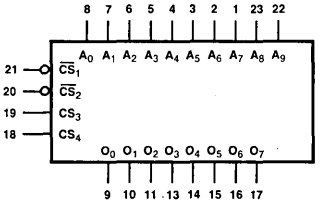
These 8K PROMs are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 8 configuration, they are available in both open collector (Am27S180A/180 and Am27S280A/280) and three-state (Am27S181A/181 and Am27S281/281) output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_9 and holding $\overline{CS}_1$ and $\overline{CS}_2$ LOW and CS_3 and CS_4 HIGH. All other valid input conditions on $\overline{CS}_1$, $\overline{CS}_2$, CS_3 and CS_4 place O_0-O_7 into the OFF or high impedance state.

BLOCK DIAGRAM



BPM-307

LOGIC DIAGRAM

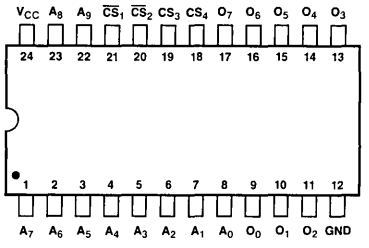


BPM-099

V_{CC} = Pin 24
GND = Pin 12

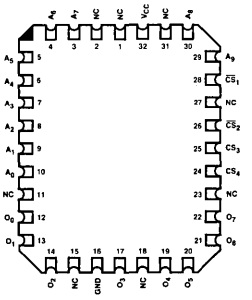
CONNECTION DIAGRAMS – Top Views

DIP



BPM-100

Chip-Pak™



BPM-279

Note: Pin 1 is marked for orientation.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

2

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)	COM'L	−20	−40	−90	mA
			MIL	−15	−40	−90	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX			115	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS}_1}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)			4.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)			8.0		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

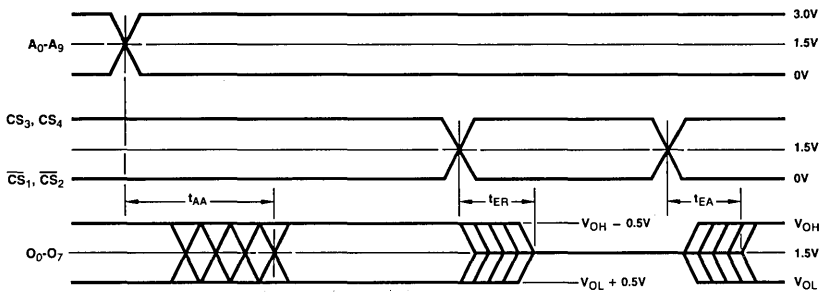
Am27S180A/S181A/S280A/S281A/S180/S181/S28O/S281

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	Typ 5V 25°C A	Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1, 2, 3)	25	30	35	60	50	80	ns
t_{EA}	Enable Access Time		10	10	25	40	30	50	ns
t_{ER}	Enable Recovery Time		10	10	25	40	30	50	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three-state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage to with S_1 open to V_{OH} – 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} + 0.5V level with S_1 closed.

SWITCHING WAVEFORMS



Note: Level on output while chip is disabled is determined externally.

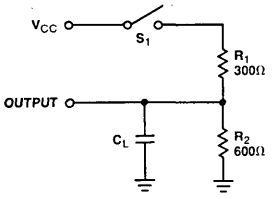
BPM-101

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
——— ———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-208

PROGRAMMING

The entire Generic PROM Series is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the devices, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

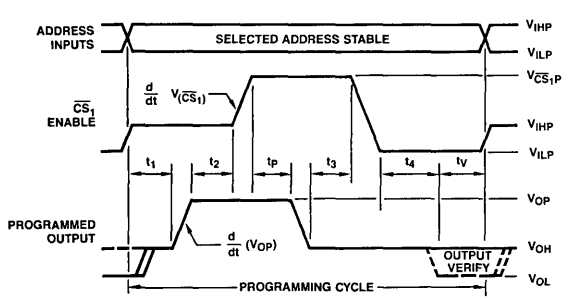
2

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{CS}_1P}$	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{CS}_1})/dt$	Rate of $\overline{CS}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

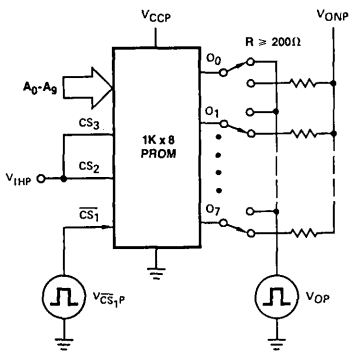
Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-209

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-308

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920 and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H* Unipak Rev K* (Code 16 37)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S180A/181A Am27S180/181	715-1545-2	PA 24-13 and 1024 x 8(L)	IM 1024 x 8-24-AMD	SA 22-7 B 1024 x 8/24	DIS-137 AM	DA 29	AM100-6
Am27S280A/281A Am27S280/281	715-1545-3	PA 24-28 and 1024 x 8(L)	IM 1024 x 8-24-27S280/281-AMD	SA 29 B 1024 x 8/24	DIS-214 AM	DA 60	AM190-6

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM27S180APC	AM27S181APC	P-24-1AC	C-1	COM'L
	AM27S180APCB	AM27S181APCB	P-24-1AC	B-1	
	AM27S280APC	AM27S281APC	P-24-1AA (Note 4)	C-1	
	AM27S280APCB	AM27S281APCB	P-24-1AA (Note 4)	B-1	
	AM27S180ADC	AM27S181ADC	D-24-1AC	C-1	
	AM27S180ADCB	AM27S181ADCB	D-24-1AC	B-1	
	AM27S280ADC	AM27S281ADC	D-24-1AA	C-1	
	AM27S280ADCB	AM27S281ADCB	D-24-1AA	B-1	
	AM27S180ALC	AM27S181ALC	L-32-2	C-1	
	AM27S180ALCB	AM27S181ALCB	L-32-2	B-1	
50ns	AM27S180ADM	AM27S181ADM	D-24-1AC	C-3	MIL
	AM27S180ADMB	AM27S181ADMB	D-24-1AC	B-3	
	AM27S280ADM	AM27S281ADM	D-24-1AA	C-3	
	AM27S280ADMB	AM27S281ADMB	D-24-1AA	B-3	
	AM27S180AFM	AM27S181AFM	F-24-1	C-3	
	AM27S180AFMB	AM27S181AFMB	F-24-1	B-3	
	AM27S180ALM	AM27S181ALM	L-32-2	C-3	
	AM27S180ALMB	AM27S181ALMB	L-32-2	B-3	
60ns	AM27S180PC	AM27S181PC	P-24-1AC	C-1	COM'L
	AM27S180PCB	AM27S181PCB	P-24-1AC	B-1	
	AM27S280PC	AM27S281PC	P-24-1AA (Note 4)	C-1	
	AM27S280PCB	AM27S281PCB	P-24-1AA (Note 4)	B-1	
	AM27S180DC	AM27S181DC	D-24-1AC	C-1	
	AM27S180DCB	AM27S181DCB	D-24-1AC	B-1	
	AM27S280DC	AM27S281DC	D-24-1AA	C-1	
	AM27S280DCB	AM27S281DCB	D-24-1AA	B-1	
	AM27S180LC	AM27S181LC	L-32-2	C-1	
	AM27S180LCB	AM27S181LCB	L-32-2	B-1	
80ns	AM27S180DM	AM27S181DM	D-24-1AC	C-3	MIL
	AM27S180DMB	AM27S181DMB	D-24-1AC	B-3	
	AM27S280DM	AM27S281DM	D-24-1AA	C-3	
	AM27S280DMB	AM27S281DMB	D-24-1AA	B-3	
	AM27S180FM	AM27S181FM	F-24-1	C-3	
	AM27S180FMB	AM27S181FMB	F-24-1	B-3	
	AM27S180LM	AM27S181LM	L-32-2	C-3	
	AM27S180LMB	AM27S181LMB	L-32-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads. AC = 600 mil center package. AA = 300 mil center package.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. This package will be available soon. Consult factory.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27PS181A • Am27PS281A

Ultra Fast Access Time

Am27PS181 • Am27PS281

Fast Access Time

8,192-Bit Generic Series IMOX™ Bipolar PROM

1024 x 8 Bits with Power-Down Via $\overline{CS}_1$

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

Part Number	Package Width	Other Features
Am27PS181A	24-Pin, Plug in Replacement for Industry Standard 600-mil Configuration No Board Changes Required	Ultra fast – 50ns max
Am27PS181		Fast – 65ns max
Am27PS281A	New Space-Saving 24-Pin, THINDIP, 300-mil Configuration Increases Overall Board Density	Ultra fast – 50ns max
Am27PS281		Fast – 65ns max

IMOX is a trademark of Advanced Micro Devices, Inc.

DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts – enhances reliability through total system heat reduction
- Plug in replacement for industry standard product – no board changes required
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Rapid recovery from power-down state provides minimum delay
- Members of generic PROM series utilizing standard programming algorithm
- 100% processed to MIL-STD-883C
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

These 8K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

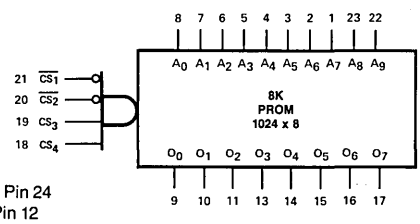
All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

LOGIC SYMBOL



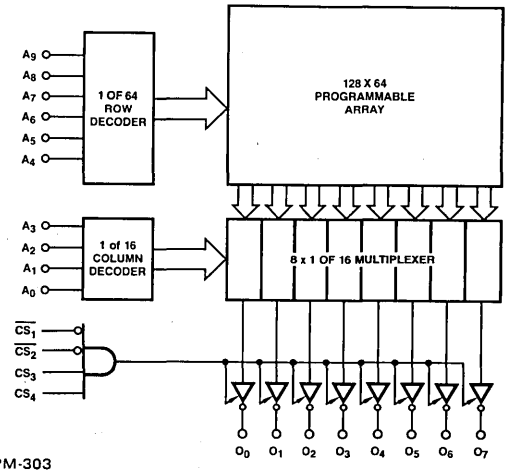
V_{CC} = Pin 24
GND Pin 12

BPM-302

FUNCTIONAL DESCRIPTION

These 8K PROMs are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 8 configuration, they are available in both the standard 600-mil package (Am27PS181A/181) and the space-saving THINDIP, 300-mil package (Am27PS281A/281) versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_9$ and holding $\overline{CS}_1$ and $\overline{CS}_2$ LOW and CS_3 and CS_4 HIGH. All other input combinations on $\overline{CS}_1$, $\overline{CS}_2$, CS_3 and CS_4 place $O_0 - O_7$ into the OFF or high impedance state and reduce I_{CC} by more than 50%.

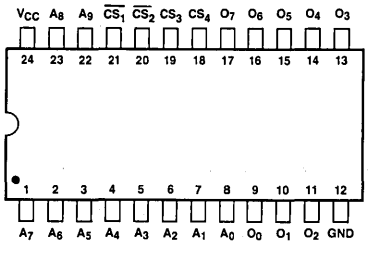
BLOCK DIAGRAM



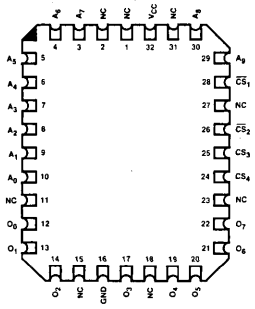
BPM-303

CONNECTION DIAGRAMS – Top Views

DIP



Chip-Pak™ L-32-2



Note: Pin 1 is marked for orientation.

BPM-304

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA, V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA, V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	COM'L	−20	−40	−90	mA
			MIL	−15	−40	−90	
I_{CC}	Power Supply Current	All inputs = GND			115	185	mA
I_{CCD}	Power Down Supply Current	$\overline{CS_1}$ = 2.7V, All other inputs = GND			50	80	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS_1}}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			4.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			8.0		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

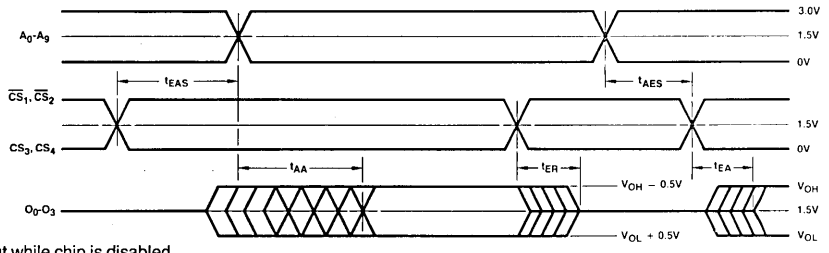
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY

Parameters	Description	Test Conditions		Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA1}	Address Access Time	t_{EAS} ≥ 25ns	AC Test Load Fig. 1-3, 5 (Notes 1, 5 & 6)	30	50	65	65	75	ns
t_{AA2}	Power Switched Address Access Time	t_{EAS} = 0ns		50	65	80	75	90	ns
t_{EA}	Enable Access Time	t_{AES} > 0ns		50	65	80	75	90	ns
t_{ER}	Enable Recovery Time			15	25	35	30	45	ns

Notes: 5. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
6. t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} −0.5V with S_1 open; LOW-to-high impedance tests are made to the V_{OL} +0.5V level with S_1 closed.

SWITCHING WAVEFORMS



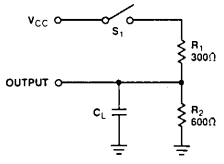
Note: Level on output while chip is disabled is determined externally.

Figure 1.

BPM-305

2

AC TEST LOAD



BPM-145

Figure 2.

KEY TO SWITCHING WAVEFORMS

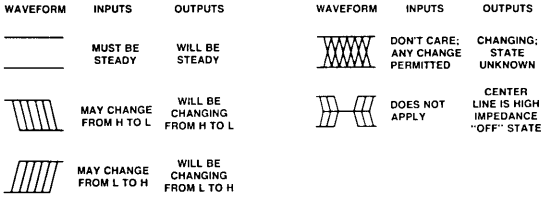


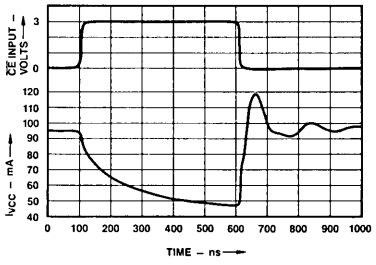
Figure 3.

NOTES ON POWER SWITCHING

The Am27PS181A/181 and Am27PS281A/281 are power switched devices. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to less than half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS181A/181 and Am27PS281A/281 are selected, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 24 to pin 12 at each device. (See Figure 4.)
2. Address access time (t_{AA}) can be optimized if a chip enable setup time (t_{EAS}) of greater than 25ns is observed. Negative setup times on chip enable ($t_{EAS} < 0$) should be avoided. (For typical and worse case characteristics, see Figure 5.)

Typical I_{VCC} Current Surge without 0.1μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)



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Typical I_{VCC} Current Surge with 0.1μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)

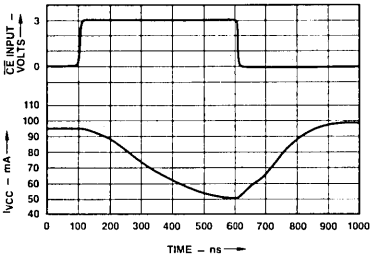

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Figure 4. I_{CC} Current

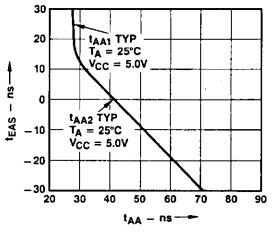

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Figure 5A. t_{AA} versus t_{EAS}

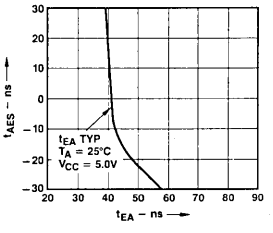

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Figure 5B. t_{EA} versus t_{AES}

PROGRAMMING

The entire Generic PROM Series is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the devices, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{CS}_1$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

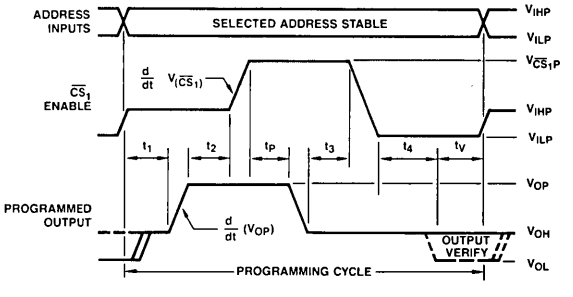
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{CS}_1P}$	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{CS}_1})/dt$	Rate of $\overline{CS}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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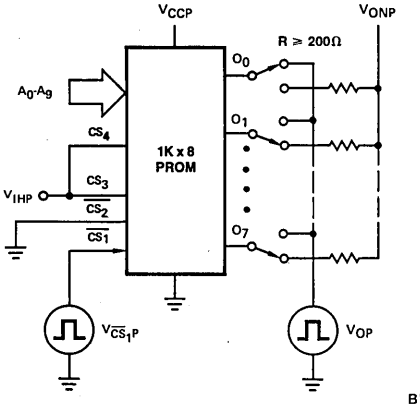
SIMPLIFIED PROGRAMMING DIAGRAM



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PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19 and 29	M900, M900B, M910, M920 and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H* Unipak Rev H* (Code 16 37)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27PS181A/ 181	715-1545-2	PA 24-13 and 1024 x 8(L)	IM 1024 x 8-24-AMD	SA 22-7 B 1024 x 8/24	DIS-137 AM	DA 61	AM100-6
Am27PS281A/ 281			IM 1024 x 8-24-27S280/281-AMD		DIS-214 AM	DA 60	

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
50ns	AM27PS181APC	P-24-1AC	C-1	COM'L
	AM27PS181APCB	P-24-1AC	B-1	
	AM27PS281APC	P-24-1AA (Note 4)	C-1	
	AM27PS281APCB	P-24-1AA (Note 4)	B-1	
	AM27PS181ADC	D-24-1AC	C-1	
	AM27PS181ADCB	D-24-1AC	B-1	
	AM27PS281ADC	D-24-1AA	C-1	
	AM27PS281ADCB	D-24-1AA	B-1	
	AM27PS181ALC	L-32-2	C-1	
	AM27PS181ALCB	L-32-2	B-1	
65ns	AM27PS181ADM	D-24-1AC	C-3	MIL
	AM27PS181ADMB	D-24-1AC	B-3	
	AM27PS281ADM	D-24-1AA	C-3	
	AM27PS281ADMB	D-24-1AA	B-3	
	AM27PS181AFM	F-24-1	C-3	
	AM27PS181AFMB	F-24-1	B-3	
	AM27PS181ALM	L-32-2	C-3	
	AM27PS181ALMB	L-32-2	B-3	
65ns	AM27PS181PC	P-24-1AC	C-1	COM'L
	AM27PS181PCB	P-24-1AC	B-1	
	AM27PS281PC	P-24-1AA (Note 4)	C-1	
	AM27PS281PCB	P-24-1AA (Note 4)	B-1	
	AM27PS181DC	D-24-1AC	C-1	
	AM27PS181DCB	D-24-1AC	B-1	
	AM27PS281DC	D-24-1AA	C-1	
	AM27PS281DCB	D-24-1AA	B-1	
	AM27PS181LC	L-32-2	C-1	
	AM27PS181LCB	L-32-2	B-1	
75ns	AM27PS181DM	D-24-1AC	C-3	MIL
	AM27PS181DMB	D-24-1AC	B-3	
	AM27PS281DM	D-24-1AA	C-3	
	AM27PS281DMB	D-24-1AA	B-3	
	AM27PS181FM	F-24-1	C-3	
	AM27PS181FMB	F-24-1	B-3	
	AM27PS181LM	L-32-2	C-3	
	AM27PS181LMB	L-32-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads. AC = 600 mil center package. AA = 300 mil center package.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. This package will be available soon. Consult factory.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27S184A • Am27S185A
Am27S184 • Am27S185

8192-Bit Generic Series Bipolar IMOX™ PROM
(2048 x 4 bits with ultra fast access time)

2

DISTINCTIVE CHARACTERISTICS

- Ultra fast access time "A" version (35ns max) – Fast access time Standard version (50ns max) – allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

These 8K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

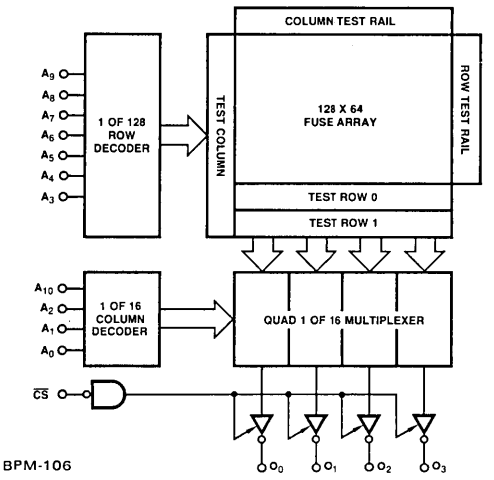
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX™. This advanced process permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

The Am27S184A and Am27S185A, Am27S184 and Am27S185 are high speed electrically programmable Schottky read only memories. Organized in 2048 x 4 configuration, they are available in both open collector (Am27S184A and Am27S184) and three-state (Am27S185A and Am27S185) output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_{10} and holding the chip select input, $\overline{CS}$ LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the OFF or high impedance state.

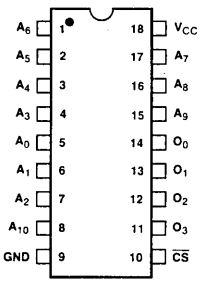
BLOCK DIAGRAM



BPM-106

CONNECTION DIAGRAMS – Top Views

DIP



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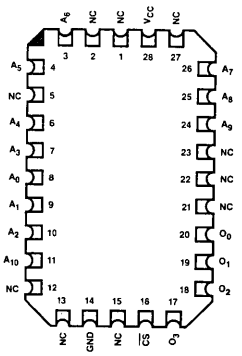
Chip-Pak™ L-28-2



Note: Pin 1 is marked for orientation. BPM-257

IMOX is a trademark of Advanced Micro Devices, Inc.
Chip-Pak is a trademark of Advanced Micro Devices, Inc.

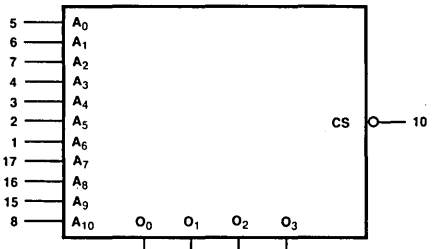
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

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ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)		−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX			105	150	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $V_{\overline{CS}}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)			8.0		

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

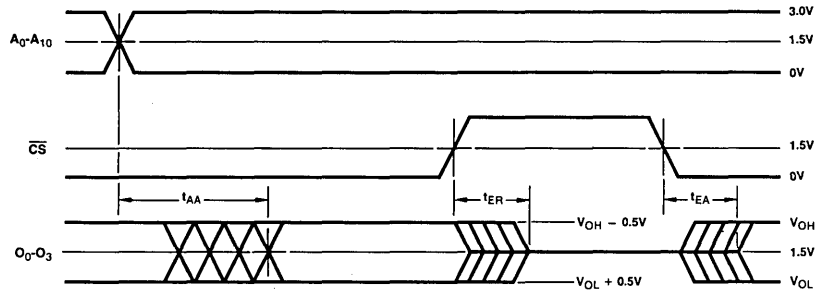
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	Typ 5V 25°C A	Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1, 2, 3)	28	30	35	50	45	55	ns
t_{EA}	Enable Access Time		10	10	25	25	30	30	ns
t_{ER}	Enable Recovery Time		10	10	25	25	30	30	ns

Notes:
1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three-state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

2

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

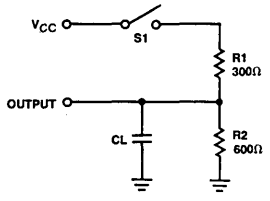
BPM-109

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-199

PROGRAMMING

This entire Generic PROM Series is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled, and the output level sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

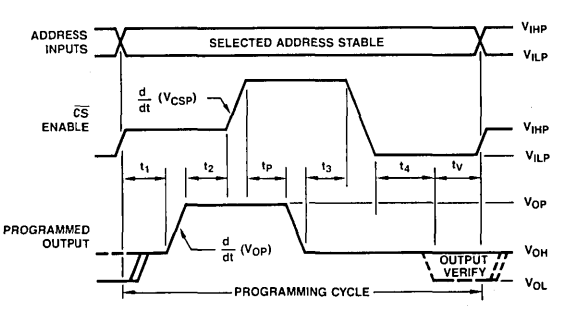
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CSP})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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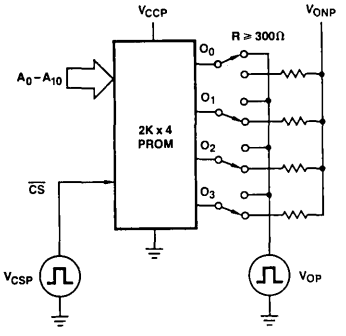
SIMPLIFIED PROGRAMMING DIAGRAM



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PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 & 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H* Unipak Rev H* (Code 1606)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S184A/185A Am27S184/185	715-1616	PA 18-8 and 2048 x 4(L)	IM 2048 x 4-18-AMD	SA 4-4 B 2048 x 4/18	DIS-211 AM	DA 23	AM 140-3

*Rev shown is minimum approved revision.

2

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM27S184APC	AM27S185APC	P-18-1	C-1	COM'L
	AM27S184APCB	AM27S185APCB	P-18-1	B-1	
	AM27S184ADC	AM27S185ADC	D-18-1	C-1	
	AM27S184ADCB	AM27S185ADCB	D-18-1	B-1	
	AM27S184ALC	AM27S185ALC	L-28-2	C-1	
	AM27S184ALCB	AM27S185ALCB	L-28-2	B-1	
45ns	AM27S184ADM	AM27S185ADM	D-18-1	C-3	MIL
	AM27S184ADMB	AM27S185ADMB	D-18-1	B-3	
	AM27S184ALM	AM27S185ALM	L-28-2	C-3	
	AM27S184ALMB	AM27S185ALMB	L-28-2	B-3	
	AM27S184AFM	AM27S185AFM	(Note 4)	C-3	
	AM27S184AFMB	AM27S185AFMB	(Note 4)	B-3	
50ns	AM27S184PC	AM27S185PC	P-18-1	C-1	COM'L
	AM27S184PCB	AM27S185PCB	P-18-1	B-1	
	AM27S184DC	AM27S185DC	D-18-1	C-1	
	AM27S184DCB	AM27S185DCB	D-18-1	B-1	
	AM27S184LC	AM27S185LC	L-28-2	C-1	
	AM27S184LCB	AM27S185LCB	L-28-2	B-1	
55ns	AM27S184DM	AM27S185DM	D-18-1	C-3	MIL
	AM27S184DMB	AM27S185DMB	D-18-1	B-3	
	AM27S184LM	AM27S185LM	L-28-2	C-3	
	AM27S184LMB	AM27S185LMB	L-28-2	B-3	
	AM27S184FM	AM27S185FM	(Note 4)	C-3	
	AM27S184FMB	AM27S185FMB	(Note 4)	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. Consult factory for flat package outline drawings.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27LS184 • Am27LS185

8192-Bit Generic Series Bipolar IMOX™ PROM
(2048 x 4 bits with low power dissipation)

DISTINCTIVE CHARACTERISTICS

- Excellent performance over the full military and commercial ranges
- Low power dissipation
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

These 8K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

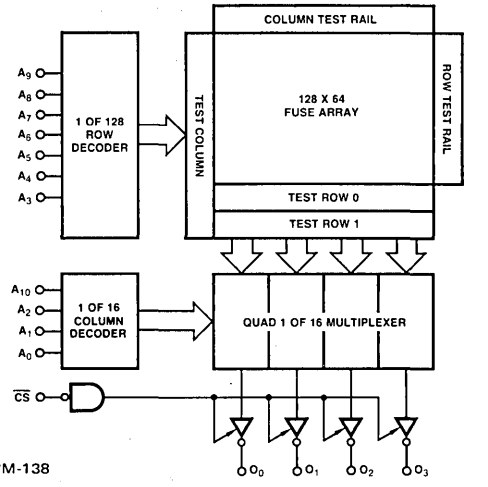
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX™. This advanced process permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

The Am27LS184 and Am27LS185 are high speed electrically programmable Low-Power Schottky read only memories. Organized in the industry standard 2048 x 4 configuration, they are available in both open collector Am27LS184 and three-state Am27LS185 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_{10} and holding the chip select input $\overline{CS}$ LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the off or high-impedance state.

BLOCK DIAGRAM



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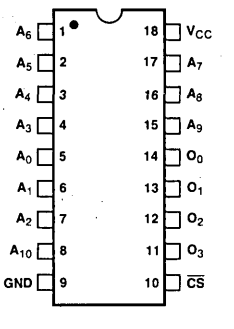
CONNECTION DIAGRAMS – Top Views

DIP



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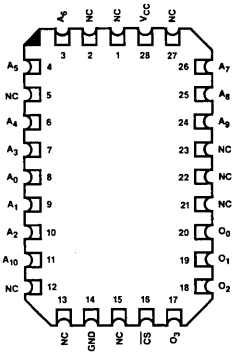
Chip-Pak™ L-28-2



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Note: Pin 1 is marked for orientation

IMOX is a trademark of Advanced Micro Devices, Inc.
Chip-Pak is a trademark of Advanced Micro Devices, Inc.

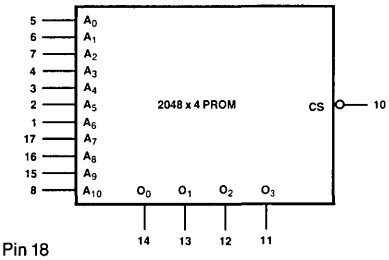
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

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ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)		−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX			80	125	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $\overline{CS}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)			5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)			8		

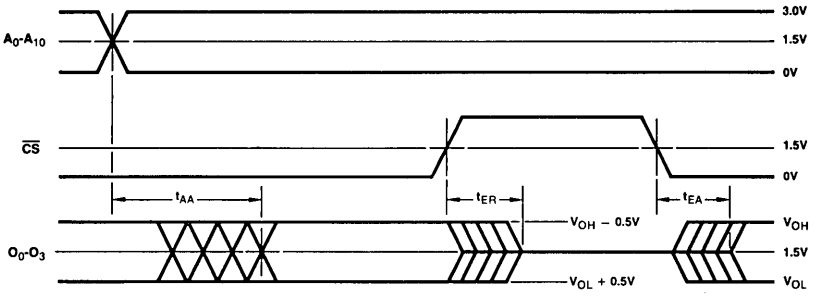
Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions	Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	40	60	65	ns
t_{EA}	Enable Access Time		10	25	30	ns
t_{ER}	Enable Recovery Time		10	25	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING CHARACTERISTICS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

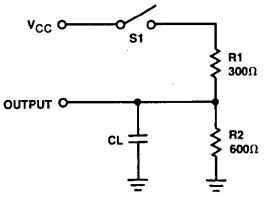
BPM-109

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
▨	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-110

PROGRAMMING

The Am27LS184 and Am27LS185 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

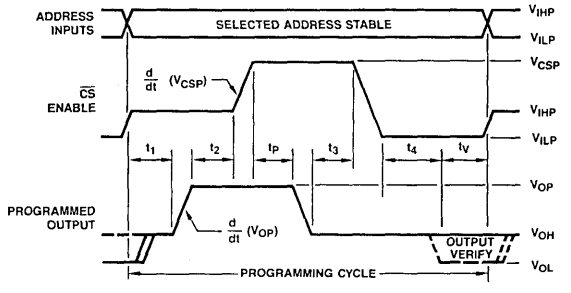
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CSP})/dt$	Rate of $\overline{CS}$, Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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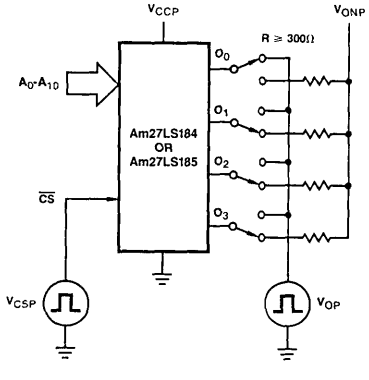
SIMPLIFIED PROGRAMMING DIAGRAM



BPM-112

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7 and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27LS184 Am27LS185	715-1616	PA 18-8 and 2048 x 4(L)	IM 2048 x 4-18-AMD	SA 4-4 B 2048 x 4/18	DIS-211 AM	DA 23	AM 140-3

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
60ns	AM27LS184PC	AM27LS185PC	P-18-1	C-1	COM'L
	AM27LS184PCB	AM27LS185PCB	P-18-1	B-1	
	AM27LS184DC	AM27LS185DC	D-18-1	C-1	
	AM27LS184DCB	AM27LS185DCB	D-18-1	B-1	
	AM27LS184LC	AM27LS185LC	L-28-2	C-1	
	AM27LS184LCB	AM27LS185LCB	L-28-2	B-1	
65ns	AM27LS184DM	AM27LS185DM	D-18-1	C-3	MIL
	AM27LS184DMB	AM27LS185DMB	D-18-1	B-3	
	AM27LS184LM	AM27LS185LM	L-28-2	C-3	
	AM27LS184LMB	AM27LS185LMB	L-28-2	B-3	
	AM27LS184FM	AM27LS185FM	(Note 4)	C-3	
	AM27LS184FMB	AM27LS185FMB	(Note 4)	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. Consult factory for flat package outline drawings.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27PS185

8192-Bit Generic Series Bipolar IMOX™ PROM (2048 x 4 bits with power-down via $\overline{CS}$)

DISTINCTIVE CHARACTERISTICS

- Fast access time (60ns max) allows system speed improvements
- 50% power savings on deselected parts – enhances reliability through total system heat reduction
- Plug in replacement for industry standard product – no board changes required
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test rows and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

The Am27PS185 is a member of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

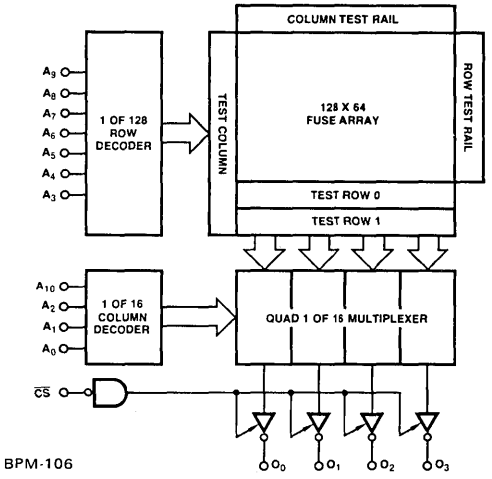
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX™. This advanced process permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

The Am27PS185 is a high speed electrically programmable Schottky read only memory. Organized in the industry standard 2048 x 4 configuration, it is available in the three-state (Am27PS185) output version. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_{10} and holding the chip select input $\overline{CS}$ LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the OFF or high-impedance state, and I_{CC} is reduced by 50%.

BLOCK DIAGRAM



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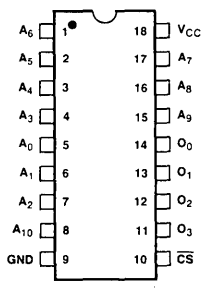
CONNECTION DIAGRAMS – Top Views

DIP



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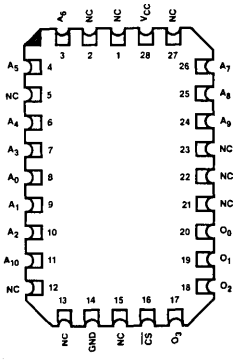
Chip-Pak™ L-28-2



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Note: Pin 1 is marked for orientation.

IMOX is a trademark of Advanced Micro Devices, Inc.
Chip-Pak is a trademerk of Advanced Micro Devices, Inc.

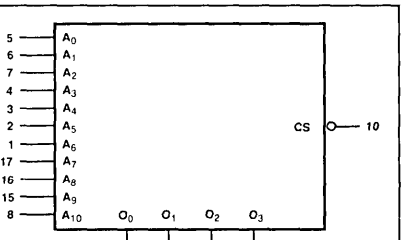
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 18 to Pin 9) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA, V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA, V_{IN} = V_{IH} or V_{IL}			0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V		−0.020	−.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}			40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	−15	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND		105	150	mA
		$\overline{CS}$ = 2.7V; All other inputs = GND		50	75	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS}}$ = 2.4V; V_O = V_{CC}			40	μA
		V_{CC} = MAX, $V_{\overline{CS}}$ = 2.4V; V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)		5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)		8		pF

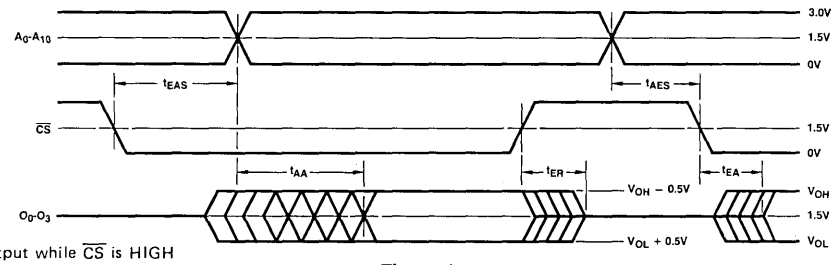
Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions		Typ 5V 25°C	Max COM'L	Max MIL	Units
t_{AA1}	Address Access Time	$t_{EAS} \geq$ 25ns	AC Test Load Fig. 1-3, 5 (Notes 1, 4 and 5)	28	50	55	ns
t_{AA2}	Power Switched Address Access Time	t_{EAS} = 0ns		41	60	65	ns
t_{EA}	Enable Access Time	$t_{AES} \geq$ 0ns		41	60	65	ns
t_{ER}	Enable Recovery Time			10	25	30	ns

Notes: 4. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
5. t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} −0.5V with S_1 open; LOW-to-HIGH impedance tests are made to the V_{OL} +0.5V level with S_1 closed.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

Figure 1.

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AC TEST LOAD

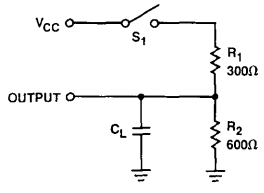


Figure 2.

BPM-145

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANYCHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

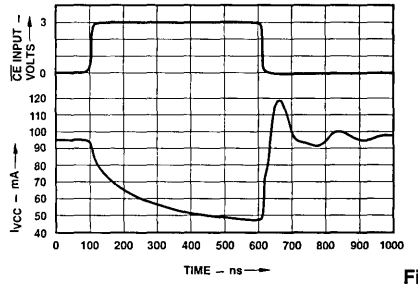
Figure 3.

POWER SWITCHING

The Am27PS185 is a power switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS185 is selected by a low level on $\overline{CS}$, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 18 to pin 9 at each device. (See Figure 4.)
2. Address access time (t_{AA}) can be optimized if a chip enable set-up time (t_{EAS}) of greater than 25ns is observed. Negative set-up times on chip enable ($t_{EAS} < 0$) should be avoided. (For typical and worse case characteristics see Figure 5.)

Typical I_{VCC} Current Surge without 0.1μf (I_{VCC} is Current Supplied by V_{CC} Power Supply)



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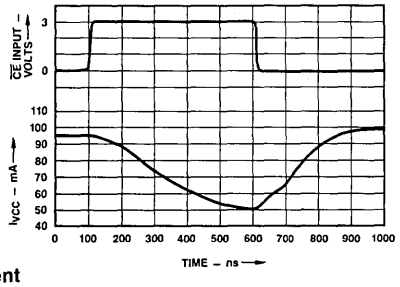
Typical I_{VCC} Current Surge with 0.1μf (I_{VCC} is Current Supplied by V_{CC} Power Supply)



BPM-147

Figure 4. I_{CC} Current

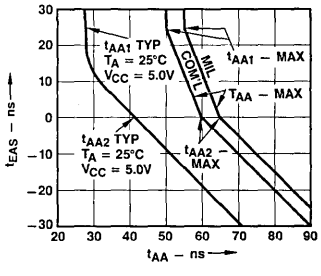


Figure 5A. T_{AA} versus T_{EAS}

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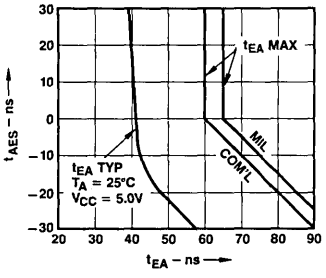


Figure 5B. T_{EA} versus T_{AES}

BPM-258

PROGRAMMING

The Am27PS185 is manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

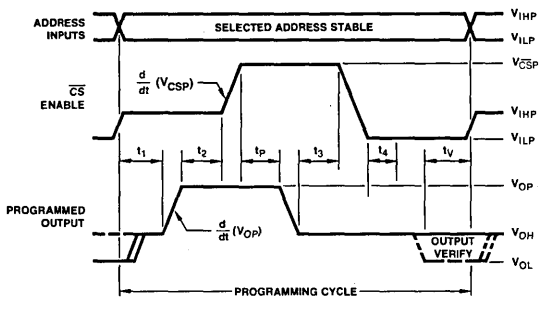
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CSP})/dt$	Rate of $\overline{CS}$, Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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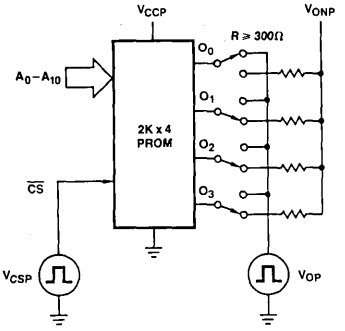
SIMPLIFIED PROGRAMMING DIAGRAM



BPM-260

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17 and 19	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H* Unipak (Code 1606)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27PS185	715-1616	PA 18-8 and 2048 x 4(L)	IM 2048 x 4-18-AMD	SA 4-4 B 2048 x 4/18	DIS-211 AM	DA 23	AM 140-3

*Rev shown is minimum approved revision.

2

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
t_{AA1} = 50ns t_{AA2} = 60ns	AM27PS185PC	P-18-1	C-1	COM'L
	AM27PS185PCB	P-18-1	B-1	
	AM27PS185DC	D-18-1	C-1	
	AM27PS185DCB	D-18-1	B-1	
	AM27PS185LC	L-28-2	C-1	
	AM27PS185LCB	L-28-2	B-1	
t_{AA1} = 55ns t_{AA2} = 65ns	AM27PS185DM	D-18-1	C-3	MIL
	AM27PS185DMB	D-18-1	B-3	
	AM27PS185LM	L-28-2	C-3	
	AM27PS185LMB	L-28-2	B-3	
	AM27PS185FM	(Note 4)	C-3	
	AM27PS185FMB	(Note 4)	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. Consult factory for flat package outline drawing.

This device is also available in die form selected to commercial and military specifications.
Pad layout and bonding diagram available upon request.

Am27S190A • Am27S191A
Am27S290A • Am27S291A

Ultra Fast Access Time

Am27S190 • Am27S191
Am27S290 • Am27S291

Fast Access Time
16,384-Bit Generic Series Bipolar IMOX™ PROM

DISTINCTIVE CHARACTERISTICS

Part Number	Package Width	Other Features
Am27S190A	24-Pin, Plug in Replacement for Industry Standard 600-mil Configuration No Board Changes Required	Ultra fast – 35ns max
Am27S191A		
Am27S190		Fast – 50ns max
Am27S191		
Am27S290A	New Space-Saving 24-Pin, THINDIP, 300-mil Configuration Increases Overall Board Density	Ultra fast – 35ns max
Am27S291A		
Am27S290		Fast – 50ns max
Am27S291		

IMOX is a trademark of Advanced Micro Devices, Inc.

DISTINCTIVE CHARACTERISTICS

- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Members of generic PROM series utilizing standard programming algorithm
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

These 16K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

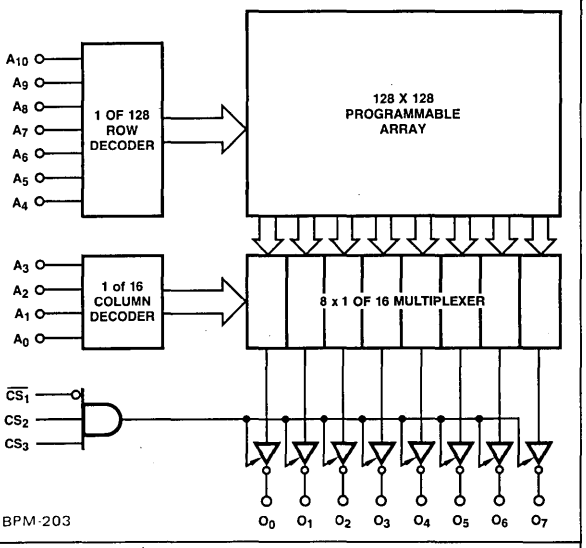
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

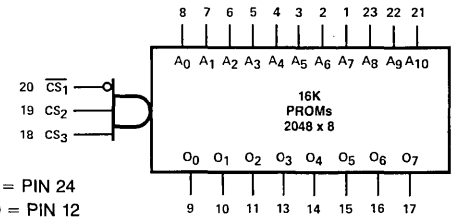
These 16K PROMs are high speed electrically programmable Schottky read only memories. Organized in the industry standard 2048 x 8 configuration, they are available in both open collector (Am27S190A/190 and Am27S290A/290) and three-state (Am27S191A/191 and Am27S291A/291) output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_{10} and holding $\overline{CS}_1$ LOW and CS_2 and CS_3 HIGH. All other valid input conditions on $\overline{CS}_1$, CS_2, and CS_3 place O_0-O_7 into the OFF or HIGH impedance state.

BLOCK DIAGRAM



BPM-203

LOGIC SYMBOL

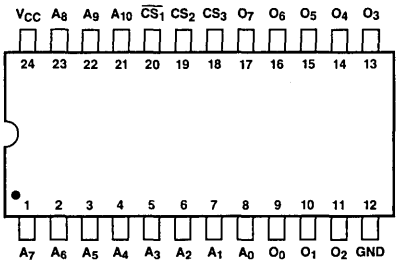


V_{CC} = PIN 24
GND = PIN 12

BPM-204

CONNECTION DIAGRAMS – Top Views

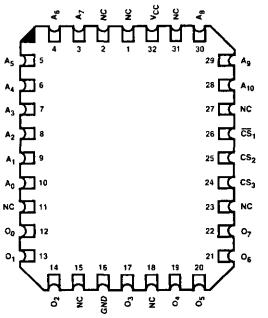
DIP



Note: Pin 1 is marked for orientation.

BPM-205

Chip-Pak™



BPM-206

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH} (TS Devices only)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC} (TS Devices only)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	COM'L	−20	−40	−90	mA
			MIL	−15	−40	−90	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX			115	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $V_{\overline{CS}_1}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			4.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			8.0		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

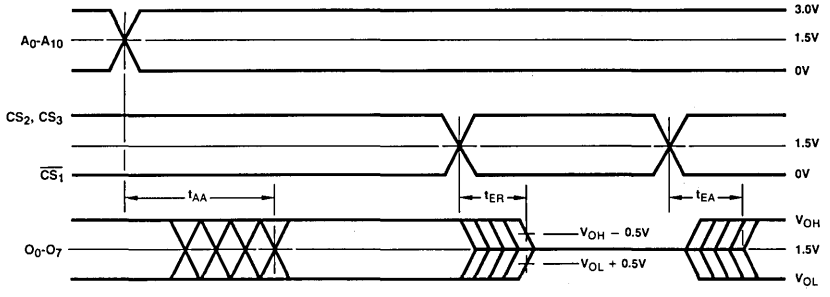
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	Typ		Max				Units
			5V 25°C		COM'L		MIL		
			A	STD	A	STD	A	STD	
t_{AA}	Address Access Time	AC Test Load (See Notes 1, 2, 3)	25	30	35	50	50	65	ns
t_{EA}	Enable Access Time		10	10	25	25	30	30	ns
t_{ER}	Enable Recovery Time		10	10	25	25	30	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested to the 1.5V output level with S_1 closed; C_L = 30pF.
3. For three-state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage to V_{OH} – 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} + 0.5V level with S_1 closed.

2

SWITCHING WAVEFORMS



Note: Level on output while chip is disabled is determined externally.

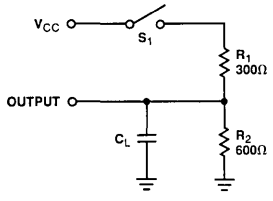
BPM-207

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-208

PROGRAMMING

The entire Generic PROM Series is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the devices, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

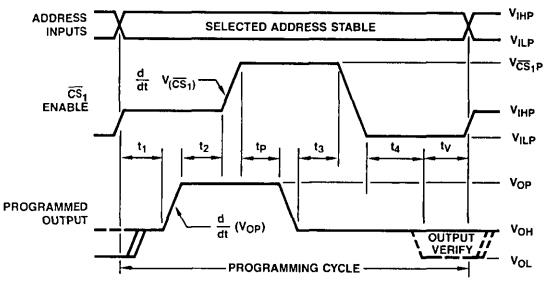
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{CS}_1P}$	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{CS}_1})dt$	Rate of $\overline{CS}_1$ Voltage Change	50	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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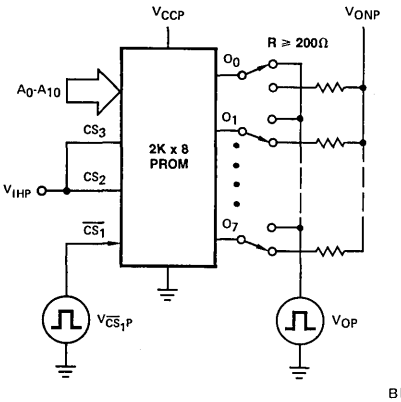
SIMPLIFIED PROGRAMMING DIAGRAM



BPM-210

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 3 Tevuot Haaretz St. Tel-Aviv, Israel		Stag Systems, Inc. 1120 San Antonio Rd. Palo Alto, CA 94303
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19 and 29	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H* Unipak Rev H* (Code 16 68)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S190A/191A Am27S190/191	715-1688-1	PA 24-17 and 2048 x 8(L)	IM 2048 x 8-24-AMD	SA 22-10 B 2048 x 8/24	DIS-151 AM	DA 61	AM100-5
Am27S290A/291A Am27S290/291	715-1688-2	PA 24-28 and 2048 x 8(L)	IM 2048 x 8-24-27S290/291-AMD	SA 29 B 2048 x 8/24	DIS-215 AM	DA 62	AM190-7

*Rev shown is minimum approved revision.

2

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 2048 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.5 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

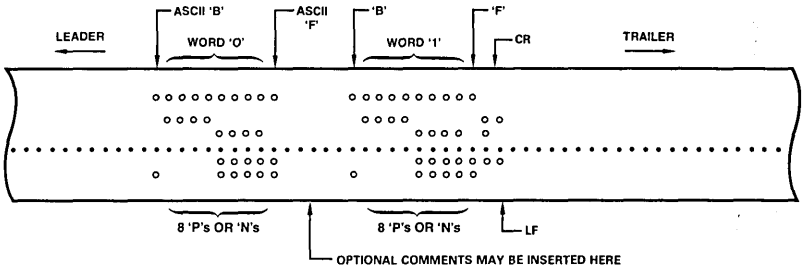
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
ØØ2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
ØØ4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
ØØ6   BPNNPPPNNF   HERE (R) (L)
 :    :::::::::::    :
2047  BNNNNPPPNF   END (R) (L)

(R) = CARRIAGE RETURN
(L) = LINE FEED
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS_1}$ LOW AND CS_2 CS_3 HIGH)

A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
						⋮								⋮				
H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



BPM-211

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM27S190APC	AM27S191APC	P-24-1AC	C-1	COM'L
	AM27S190APCB	AM27S191APCB	P-24-1AC	B-1	
	AM27S290APC	AM27S291APC	P-24-1AA (Note 4)	C-1	
	AM27S290APCB	AM27S291APCB	P-24-1AA (Note 4)	B-1	
	AM27S190ADC	AM27S191ADC	D-24-1AC	C-1	
	AM27S190ADCB	AM27S191ADCB	D-24-1AC	B-1	
	AM27S290ADC	AM27S291ADC	D-24-1AA	C-1	
	AM27S290ADCB	AM27S291ADCB	D-24-1AA	B-1	
	AM27S190ALC	AM27S191ALC	L-32-2	C-1	
	AM27S190ALCB	AM27S191ALCB	L-32-2	B-1	
50ns	AM27S190ADM	AM27S191ADM	D-24-1AC	C-3	MIL
	AM27S190ADMB	AM27S191ADMB	D-24-1AC	B-3	
	AM27S290ADM	AM27S291ADM	D-24-1AA	C-3	
	AM27S290ADMB	AM27S291ADMB	D-24-1AA	B-3	
	AM27S190AFM	AM27S191AFM	F-24-1	C-3	
	AM27S190AFMB	AM27S191AFMB	F-24-1	B-3	
	AM27S190ALM	AM27S191ALM	L-32-2	C-3	
	AM27S190ALMB	AM27S191ALMB	L-32-2	B-3	
50ns	AM27S190PC	AM27S191PC	P-24-1AC	C-1	COM'L
	AM27S190PCB	AM27S191PCB	P-24-1AC	B-1	
	AM27S290PC	AM27S291PC	P-24-1AA (Note 4)	C-1	
	AM27S290PCB	AM27S291PCB	P-24-1AA (Note 4)	B-1	
	AM27S190DC	AM27S191DC	D-24-1AC	C-1	
	AM27S190DCB	AM27S191DCB	D-24-1AC	B-1	
	AM27S290DC	AM27S291DC	D-24-1AA	C-1	
	AM27S290DCB	AM27S291DCB	D-24-1AA	B-1	
	AM27S190LC	AM27S191LC	L-32-2	C-1	
	AM27S190LCB	AM27S191LCB	L-32-2	B-1	
65ns	AM27S190DM	AM27S191DM	D-24-1AC	C-3	MIL
	AM27S190DMB	AM27S191DMB	D-24-1AC	B-3	
	AM27S290DM	AM27S291DM	D-24-1AA	C-3	
	AM27S290DMB	AM27S291DMB	D-24-1AA	B-3	
	AM27S190FM	AM27S191FM	F-24-1	C-3	
	AM27S190FMB	AM27S191FMB	F-24-1	B-3	
	AM27S190LM	AM27S191LM	L-32-2	C-3	
	AM27S190LMB	AM27S191LMB	L-32-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads. AC = 600 mil center package. AA = 300 mil center package.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. This package will be available soon. Consult factory.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27PS191A • Am27PS291A

Ultra Fast Access Time

Am27PS191 • Am27PS291

Fast Access Time

16,384-Bit Generic Series IMOX™ Bipolar PROM

2048 x 8 Bits with Power-Down Via $\overline{CS}$

2

DISTINCTIVE CHARACTERISTICS

Part Number	Package Width	Other Features
Am27PS191A	24-Pin, Plug in Replacement for Industry Standard 600-mil Configuration No Board Changes Required	Ultra fast – 50ns max
Am27PS191		Fast – 65ns max
Am27PS291A	New Space-Saving 24-Pin, THINDIP, 300-mil Configuration Increases Overall Board Density	Ultra fast – 50ns max
Am27PS291		Fast – 65ns max

IMOX is a trademark of Advanced Micro Devices, Inc.

DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts – enhances reliability through total system heat reduction
- Plug in replacement for industry standard product – no board changes required
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Rapid recovery from power-down state provides minimum delay
- Members of generic PROM series utilizing standard programming algorithm
- 100% processed to MIL-STD-883C
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

These 16K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

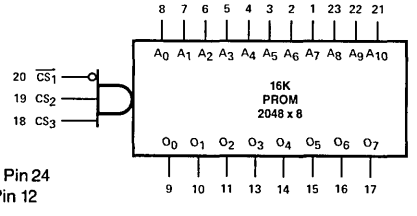
All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

LOGIC SYMBOL



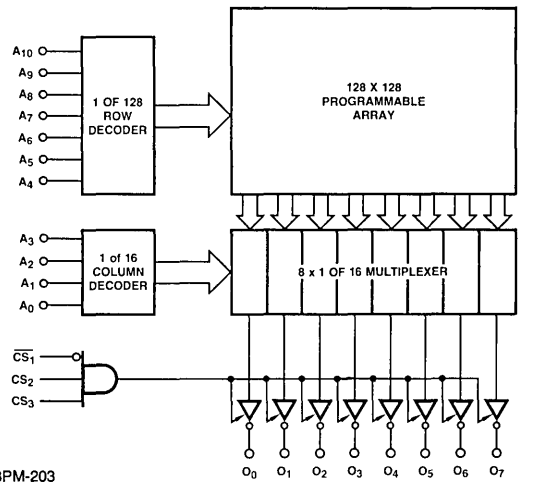
V_{CC} = Pin 24
GND Pin 12

BPM-204

FUNCTIONAL DESCRIPTION

These 16K PROMs are high speed electrically programmable Schottky read only memories. Organized in the industry standard 2048 x 8 configuration, they are available in both the standard 600-mil package (Am27PS191A/191) and the space-saving THINDIP, 300-mil package (Am27PS291A/291) versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_{10}$ and holding $\overline{CS}_1$ LOW and CS_2 and CS_3 HIGH. All other input combinations on $\overline{CS}_1$, CS_2, and CS_3 place $O_0 - O_7$ into the OFF or high impedance state and reduce I_{CC} by more than 50%.

BLOCK DIAGRAM



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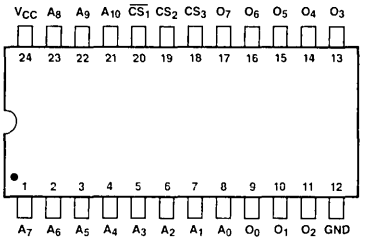
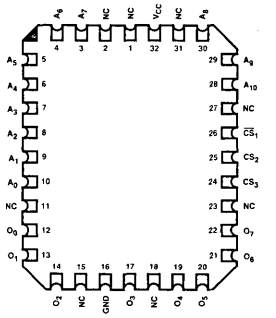
CONNECTION DIAGRAMS – Top Views

DIP



Note: Pin 1 is marked for orientation.

Chip-Pak™ L-32-2



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Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

2

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	COM'L	−20	−40	−90	mA
			MIL	−15	−40	−90	
I_{CC}	Power Supply Current	All inputs = GND			115	185	mA
I_{CCD}	Power Down Supply Current	$\overline{CS_1}$ = 2.7V	All other inputs = GND		50	80	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX	V_O = V_{CC}			40	μA
		$V_{\overline{CS_1}}$ = 2.4V	V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			4.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			8.0		

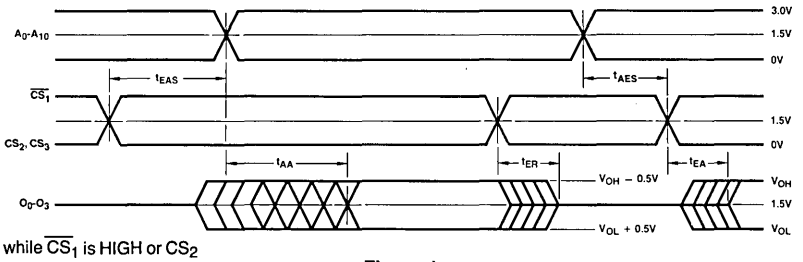
Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions		Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA1}	Address Access Time	$t_{EAS} \geq$ 25ns	AC Test Load Fig. 1-3, 5 (Notes 5 and 6)	30	50	65	65	75	ns
t_{AA2}	Power Switched Address Access Time	t_{EAS} = 0ns		50	65	80	75	90	ns
t_{EA}	Enable Access Time	t_{AES} > 0ns		50	65	80	75	90	ns
t_{ER}	Enable Recovery Time			15	25	35	30	45	ns

Notes: 5. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
6. t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} −0.5V with S_1 open; LOW-to-high impedance tests are made to the V_{OL} +0.5V level with S_1 closed.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS_1}$ is HIGH or CS_2 or CS_3 are LOW is determined externally.

Figure 1.

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AC TEST LOAD

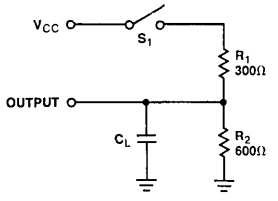

Figure 2.

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KEY TO SWITCHING WAVEFORMS

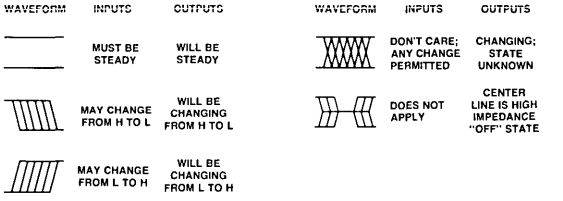


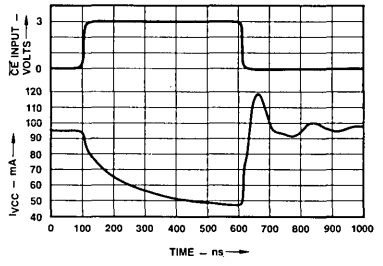
Figure 3.

NOTES ON POWER SWITCHING

The Am27PS191A/191 and Am27PS291A/291 are power switched devices. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to less than half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS191A/191 and Am27PS291A/291 are selected, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 24 to pin 12 at each device. (See Figure 4.)
2. Address access time (t_{AA}) can be optimized if a chip enable set-up time (t_{EAS}) of greater than 25ns is observed. Negative set-up times on chip enable ($t_{EAS} < 0$) should be avoided. (For typical and worse case characteristics, see Figure 5.)

Typical I_{VCC} Current Surge without 0.1μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)



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Typical I_{VCC} Current Surge with 0.1μF (I_{VCC} is Current Supplied by V_{CC} Power Supply)

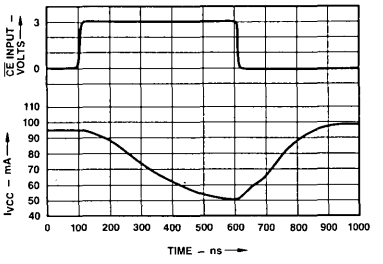

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Figure 4. I_{CC} Current

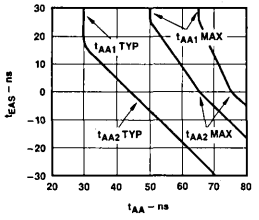

Figure 5A. t_{AA} vs t_{EAS} (Am27PS191A/291A)

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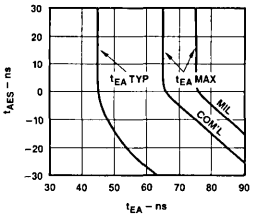

Figure 5B. t_{EA} vs t_{AES}

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PROGRAMMING

The entire Generic PROM Series is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the devices, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{CS}_1$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled and the output level is sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

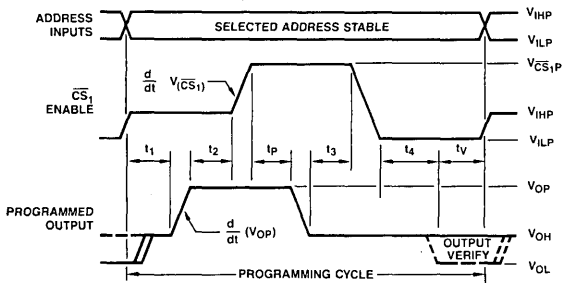
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{CS}_1P}$	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{CS}_1})/dt$	Rate of $\overline{CS}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_v, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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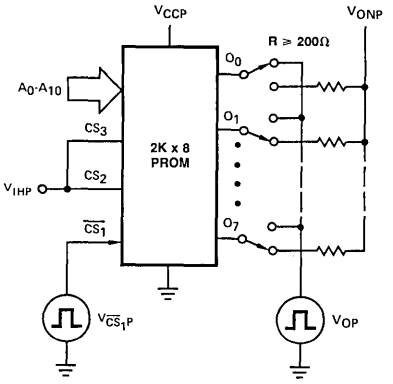
SIMPLIFIED PROGRAMMING DIAGRAM



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PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H* Unipak Rev H* (Code 16 68)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27PS191A/ 191	715-1688-1	PA 24-17 and 2048 x 8(L)	IM 2048 x 8-24-AMD	SA 22-10 B 2048 x 8/24	DIS-151 AM	DA 61	AM100-5
Am27PS291A/ 291	715-1688-2	PA 24-28 and 2048 x 8(L)	IM 2048 x 8-24-27S290/291-AMD	SA 29 B 2048 x 8/24	DIS-215 AM	DA 62	AM190-7

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
T_{AA1} = 50ns T_{AA2} = 65ns	AM27PS191APC	P-24-1AC	C-1	COM'L
	AM27PS191APCB	P-24-1AC	B-1	
	AM27PS291APC	P-24-1AA (Note 4)	C-1	
	AM27PS291APCB	P-24-1AA (Note 4)	B-1	
	AM27PS191ADC	D-24-1AC	C-1	
	AM27PS191ADCB	D-24-1AC	B-1	
	AM27PS291ADC	D-24-1AA	C-1	
	AM27PS291ADCB	D-24-1AA	B-1	
	AM27PS191ALC	L-32-2	C-1	
	AM27PS191ALCB	L-32-2	B-1	
T_{AA1} = 65ns T_{AA2} = 75ns	AM27PS191ADM	D-24-1AC	C-3	MIL
	AM27PS191ADMB	D-24-1AC	B-3	
	AM27PS291ADM	D-24-1AA	C-3	
	AM27PS291ADMB	D-24-1AA	B-3	
	AM27PS191AFM	F-24-1	C-3	
	AM27PS191AFMB	F-24-1	B-3	
	AM27PS191ALM	L-32-2	C-3	
	AM27PS191ALMB	L-32-2	B-3	
T_{AA1} = 65ns T_{AA2} = 80ns	AM27PS191PC	P-24-1AC	C-1	COM'L
	AM27PS191PCB	P-24-1AC	B-1	
	AM27PS291PC	P-24-1AA (Note 4)	C-1	
	AM27PS291PCB	P-24-1AA (Note 4)	B-1	
	AM27PS191DC	D-24-1AC	C-1	
	AM27PS191DCB	D-24-1AC	B-1	
	AM27PS291DC	D-24-1AA	C-1	
	AM27PS291DCB	D-24-1AA	B-1	
	AM27PS191LC	L-32-2	C-1	
	AM27PS191LCB	L-32-2	B-1	
T_{AA1} = 75ns T_{AA2} = 90ns	AM27PS191DM	D-24-1AC	C-3	MIL
	AM27PS191DMB	D-24-1AC	B-3	
	AM27PS291DM	D-24-1AA	C-3	
	AM27PS291DMB	D-24-1AA	B-3	
	AM27PS191FM	F-24-1	C-3	
	AM27PS191FMB	F-24-1	B-3	
	AM27PS191LM	L-32-2	C-3	
	AM27PS191LMB	L-32-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads. AC = 600 mil center package. AA = 300 mil center package.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. This package will be available soon. Consult factory.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27S45A • Am27S45
Am27S47A • Am27S47

16K-Bit (2048 x 8) Generic Series IMOX™
Bipolar High Performance Registered PROM with Programmable $\overline{\text{INITIALIZE}}$

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Member of AMD's Generic Family of 8-bit wide registered PROMs
- On-chip edge-triggered registers – ideal for pipelined microprogrammed systems
- User programmable for synchronous or asynchronous enable for simplified word expansion
- Versatile programmable register $\overline{\text{INITIALIZE}}$ either asynchronous (Am27S45A/45) or synchronous (Am27S47A/47)
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Fast standard version – 45ns max setup and 25ns max clock-to-output allows system speed improvements
- "A" version offers improved AC performance in critical paths (40ns max setup and 20ns max clock-to-output)
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ>98%)
- AC performance is factory tested utilizing programmed test words and columns
- 100% MIL-STD-883C processing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

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All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming algorithms (and common programming equipment) these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to insure extremely high field programming yields and produce excellent AC and DC parametric correlation.

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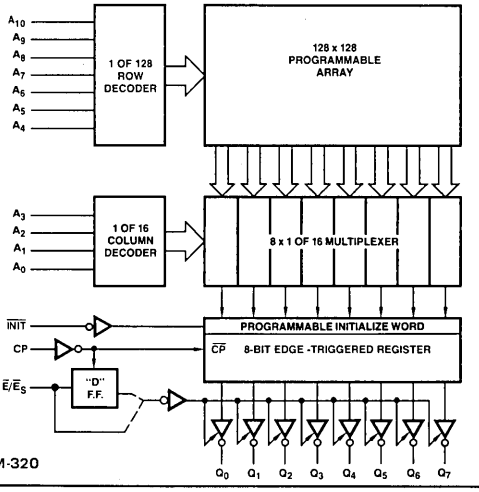
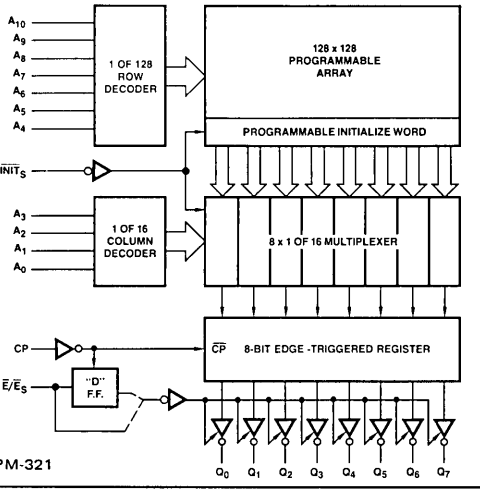
BLOCK DIAGRAMS

Am27S45A/45



BPM-320

Am27S47A/47



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IMOX is a trademark of Advanced Micro Devices, Inc.

FUNCTIONAL DESCRIPTION

The Am27S45A/45 and Am27S47A/47 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 2048-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S45A/45 and Am27S47A/47 also offer maximum flexibility for system design by providing either synchronous or asynchronous initialize, and sychronous or asynchronous output enable.

When V_{CC} power is first applied, the state of the ouputs will depend on whether the enable has been programmed to be a synchronous or asynchronous enable. If the synchronous enable ($\overline{E}_S$) is being used, the register will be in the set condition causing the outputs (Q_0 to Q_7) to be in the OFF or HIGH impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or HIGH impedance state only if the enable ($\overline{E}$) input is at a logic HIGH level. Reading data is accomplished by first applying the binary word address to the address inputs (A_0 through A_{10}) and a logic LOW to the enable input. During the address setup time, the stored data is accessed and loaded into the master flip-flops of the data register. Upon the next LOW-to-HIGH transition of the clock input (CP), data is transferred to the slave flip-flops which drive the output buffers, and the accessed data will appear at the outputs (Q_0 through Q_7). If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable back to the logic LOW state. For devices using the synchronous enable ($\overline{E}_S$), the outputs will go into the OFF or HIGH impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the next positive clock edge willl return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change, since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from the system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

These devices also contain a built-in initialize function. When activated, the initialize control input ($\overline{INIT}$) causes the contents of an additional (2049th) 8-bit word to be loaded into the on-chip register. This extra word is user programmable. Since each bit is individually programmable, the initialize function can be used to load any desired combination of HIGHs and LOWs into the register. In the unprogrammed state, activating $\overline{INIT}$ will perform a register CLEAR (all outputs LOW). If all bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

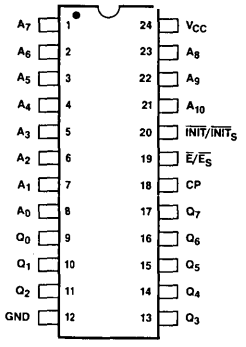
This ability to tailor the initialize outputs to the system requirements simplifies system design and enhances performance. The initialize function is useful during power up and timeout sequences. This flexible feature can also facilitate implementation of other sophisticated functions such as a built-in "jump-start" address.

The Am27S45A/45 has an asynchronous initialize input ($\overline{INIT}$). Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register independent of all other inputs (including CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

The Am27S47A/47 has a synchronous $\overline{INIT}_S$ input. Applying a LOW to the $\overline{INIT}_S$ input causes an immediate load of the programmed initialize word into the master flip-flops of the register only independent of all other inputs (including CP). To bring this data to the outputs of a device with a synchronous enable, the synchronous enable ($\overline{E}_S$) should be held LOW until the next LOW-to-HIGH transition of the clock (CP). For a device with an asynchronous enable, the data will appear at the device outputs after the next LOW-to-HIGH clock transition if the enable ($\overline{E}$) is held LOW.

CONNECTION DIAGRAMS
Top Views

DIP



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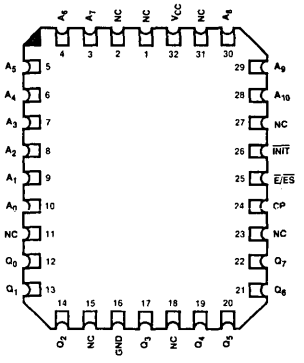
Chip-Pak™
L-32-2



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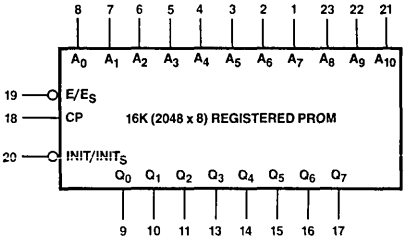
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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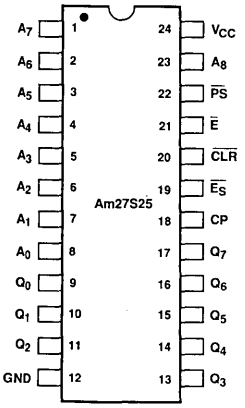
V_{CC}=Pin 24
GND=Pin 12

AMD's GENERIC FAMILY OF 8-WIDE REGISTERED PROMs



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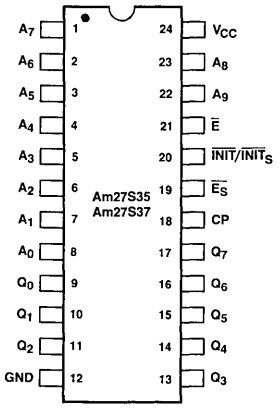
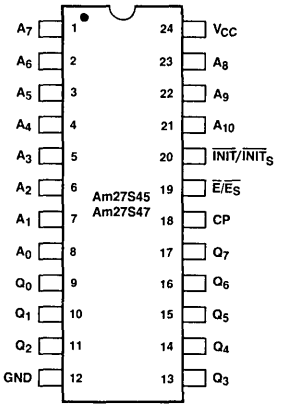
512 x 8



BPM-326

1024 x 8



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2048 x 8

Note: Pin 1 is marked for orientation.

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PRELIMINARY

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

2

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V				−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}					40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 3)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX				130	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX V_E = 2.4V	(Note 4)	V_O = V_{CC}			40	μA
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 5)				5		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 5)				12		

Notes: 1. Typical values are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. These parameters are not 100% tested, but are periodically sampled.

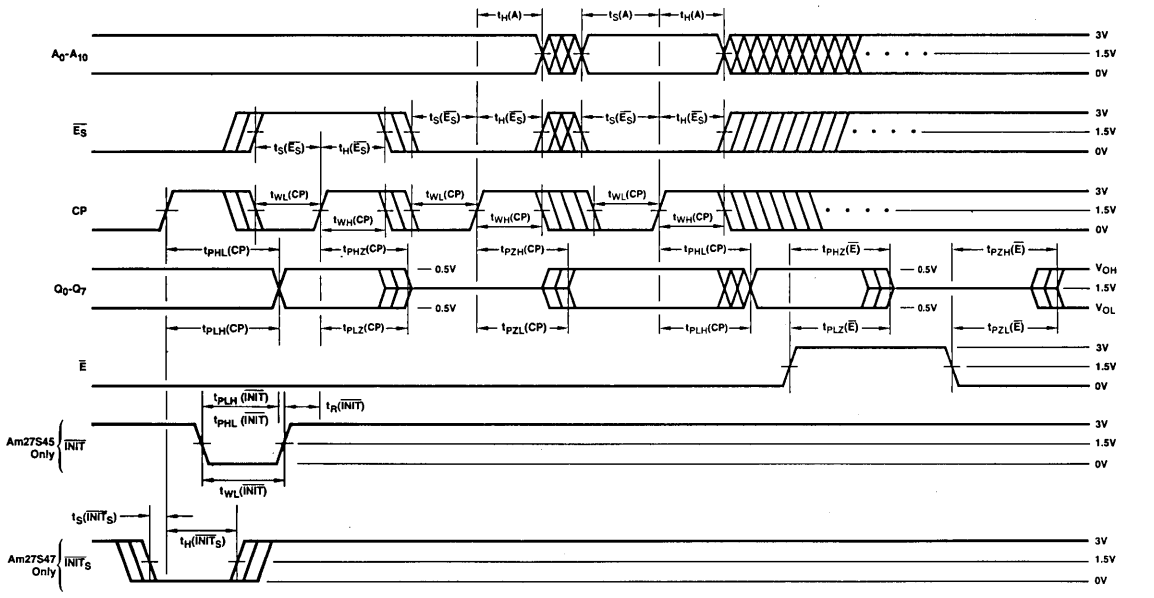
SWITCHING CHARACTERISTICS OVER OPERATING RANGE (See Notes on Testing)

PRELIMINARY

Parameters	Description		Typ (Note 1)	Am27S45A • Am27S47A COM'L Min	Am27S45A • Am27S47A COM'L Max	Am27S45A • Am27S47A MIL Min	Am27S45A • Am27S47A MIL Max	Am27S45 • Am27S47 COM'L Min	Am27S45 • Am27S47 COM'L Max	Am27S45 • Am27S47 MIL Min	Am27S45 • Am27S47 MIL Max	Units
$t_S(A)$	Address to CP (HIGH) Setup Time		25	40		45		45		50		ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−4	0		0		0		0		ns
$t_{PHL}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)	All Outputs Simlutaneous	13		20		25		25		30	ns
$t_{PLH}(CP)$		Single Output (Note 3)	11		18		21		20		23	
$t_{WH}(CP)$ / $t_{WL}(CP)$	CP Width (HIGH or LOW)		10	20		20		20		20		ns
$t_S(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Setup Time		5	15		15		15		15		ns
$t_H(\overline{E}_S)$	$\overline{E}_S$ to CP (HIGH) Hold Time		−2	5		5		5		5		ns
$t_{PHL}(\overline{INIT})$ / $t_{PLH}(\overline{INIT})$	Delay from $\overline{INIT}$ (LOW) to Outputs (LOW or HIGH) (Note 5)		20		30		35		35		40	ns
$t_R(\overline{INIT})$	$\overline{INIT}$ Recovery (Inactive) to CP (HIGH) (Note 5)		8	20		20		20		20		ns
$t_{WL}(\overline{INIT})$	$\overline{INIT}$ Pulse Width (Note 5)		10	25		30		25		30		ns
$t_S(\overline{INIT}_S)$	$\overline{INIT}_S$ to CP (HIGH) Setup Time (Note 6)		18	25		30		30		35		ns
$t_H(\overline{INIT}_S)$	$\overline{INIT}_S$ to CP (HIGH) Hold Time (Note 6)		−5	0		0		0		0		ns
$t_{PZL}(CP)$ / $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW) (Note 7)		15		25		30		30		35	ns
$t_{PLZ}(CP)$ / $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or High Impedance) (Notes 4 and 7)		15		25		30		30		35	ns
$t_{PZL}(\overline{E})$ / $t_{PZH}(\overline{E})$	Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) (Note 8)		15		25		30		30		35	ns
$t_{PLZ}(\overline{E})$ / $t_{PHZ}(\overline{E})$	Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or High Impedance) (Notes 4 and 8)		10		25		30		30		35	ns

Notes:
1. Typical values at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. Tests are performed with input 10 to 90% rise and fall times of 5ns or less.
3. Single register performance numbers provided for comparison with discrete register test data.
4. t_{PHZ} and t_{PLZ} are measured to the $V_{OH} - 0.5V$ and $V_{OL} + 0.5V$ output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
5. Applies only to the Am27S45A/45 (asynchronous $\overline{INITIALIZE}$ function).
6. Applies only to the Am27S47A/47 (synchronous $\overline{INITIALIZE}$ function).
7. Applies only when synchronous $\overline{ENABLE}$ function is used.
8. Applies only when asynchronous $\overline{ENABLE}$ function is used.

SWITCHING WAVEFORMS
(See Notes on Testing)



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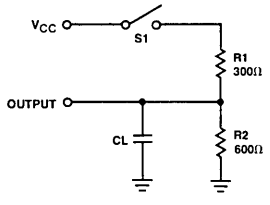
NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

AC TEST LOAD



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Notes: 1. C_L = 50pF for all switching characteristics except t_{PLZ} and t_{PHZ}.
2. C_L = 5pF for t_{PLZ} and t_{PHZ}.
3. S_1 is closed for all tests except for t_{PHZ} and t_{PZH}.
4. All device test loads should be located within 2" of device outputs.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

PROGRAMMING

These 16K registered PROMs are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. Programming each bit location (i.e. opening the fusible links) is accomplished by first applying a logic HIGH to the $\overline{E}/\overline{E}_S$ and $\overline{INIT}/\overline{INIT}_S$ inputs, followed by a LOW-to-HIGH clock transition in order to disable the outputs (although devices with an asynchronous $\overline{ENABLE}$ input do not require this clock pulse, it nevertheless may be included in the programming algorithm without affecting the programmability of the devices. This feature allows the use of a common generic programming algorithm for use on all registered PROMs). The output is then raised to 20 volts, and current from this 20 volt supply is then gated through the addressed fuse by raising the $\overline{E}/\overline{E}_S$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled and the CP input is clocked. Each data verification must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

The initialize word is programmed by setting the $\overline{INIT}/\overline{INIT}_S$ input to a logic LOW and programming the desired initialize word, output by output, in the same manner as any other address location. The address inputs may assume either logic state, but should not be left open, in order to avoid the possibility of oscillation. This is easily implemented by inverting the A_{11} address input from a PROM programmer and applying this signal to the $\overline{INIT}/\overline{INIT}_S$ input. Using this method the initialize word would be programmed as address 2048. When $\overline{INIT}/\overline{INIT}_S$ is asserted LOW the internal programming circuitry for all other addresses is deselected. Address A_0 must be LOW.

The enable input for these devices is shipped from the factory as an asynchronous enable ($\overline{E}$) and may be programmed to a synchronous enable ($\overline{E}_S$) by using the following programming procedure. To program the enable function to a synchronous enable the $\overline{INIT}/\overline{INIT}_S$ input must be set to a logic LOW, with address A_0 in a logic HIGH state. A standard programming pulse should then be applied to output Q_0. The remaining address inputs may assume either logic state, but should not be left open in order to avoid possibility of oscillation. This is easily implemented by inverting the A_{11} address from a PROM programmer and applying this signal to the $\overline{INIT}/\overline{INIT}_S$ input. Using this method the synchronous enable word would be treated as address 2049.

Typical current into an output during programming will be approximately 190mA until the fuse link is opened, after which the current drops to approximately 110mA. Current into the $\overline{E}/\overline{E}_S$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

It should be noted that when programming $\overline{E}_S$, the enable pin is changing from an asynchronous enable ($\overline{E}$) to a synchronous enable ($\overline{E}_S$). This is a functional change rather than a data change to the part. Therefore, verification that the programming event has taken place must be performed in a different manner.

The Am27S45/47 contains on-chip circuitry which when enabled will cause the $\overline{E}/\overline{E}_S$ fuse to appear as data on all outputs simultaneously; i.e. fuse intact = asynchronous enable = 00_{16} and fuse programmed = synchronous enable = FF_{16}. This verification circuitry is enabled by taking the A_0 input to a "zener high level" (14V. to 15V.). This "zener high level" should be used for read and verification cycles only (not programming) and preferably for the explicit address used for $\overline{E}/\overline{E}_S$ data only.

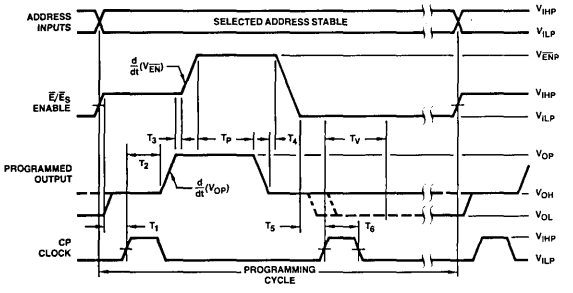
An alternative to using the on-chip verification circuitry would be for the programming equipment to utilize decision making capability in conjuction with clock and enable to determine in which functional mode the enable is operating.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{ENP}}$	$\overline{E}/\overline{E}_S$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{EN}})/dt$	Rate of $\overline{E}/\overline{E}_S$, Voltage Change	50	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_7 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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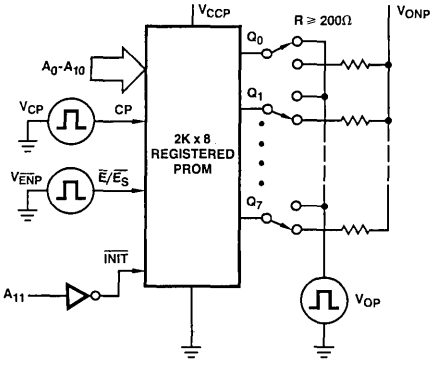
SIMPLIFIED PROGRAMMING DIAGRAM



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PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev J* 919-1286-1 Rev J*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Socket Adapters and Configurators							
Am27S45 Am27S47	715-1660	PA 24 and 2049 x 8(L)	IM 2048 x 8-27S45/ 47 AMD	SA 31 B 2048 x 8/24	DIS-217 AM	DA 64	

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

ORDERING INFORMATION

Speed Selection (Setup Time)	Order Code: Asynchronous $\overline{\text{INITIALIZE}}$	Order Code: Synchronous $\overline{\text{INITIALIZE}}$	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
40ns	AM27S45APC	AM27S47APC	P-24-1AA (Note 4)	C-1	COM'L
	AM27S45APCB	AM27S47APCB	P-24-1AA (Note 4)	B-1	
	AM27S45ADC	AM27S47ADC	D-24-1AA	C-1	
	AM27S45ADCB	AM27S47ADCB	D-24-1AA	B-1	
	AM27S45ALC	AM27S47ALC	L-32-2	C-1	
	AM27S45ALCB	AM27S47ALCB	L-32-2	B-1	
45ns	AM27S45ADM	AM27S47ADM	D-24-1AA	C-3	MIL
	AM27S45ADMB	AM27S47ADMB	D-24-1AA	B-3	
	AM27S45AFM	AM27S47AFM	F-24-1	C-3	
	AM27S45AFMB	AM27S47AFMB	F-24-1	B-3	
	AM27S45ALM	AM27S47ALM	L-32-2	C-3	
	AM27S45ALMB	AM27S47ALMB	L-32-2	B-3	
45ns	AM27S45PC	AM27S47PC	P-24-1AA (Note 4)	C-1	COM'L
	AM27S45PCB	AM27S47PCB	P-24-1AA (Note 4)	B-1	
	AM27S45DC	AM27S47DC	D-24-1AA	C-1	
	AM27S45DCB	AM27S47DCB	D-24-1AA	B-1	
	AM27S45LC	AM27S47LC	L-32-2	C-1	
	AM27S45LCB	AM27S47LCB	L-32-2	B-1	
50ns	AM27S45DM	AM27S47DM	D-24-1AA	C-3	MIL
	AM27S45DMB	AM27S47DMB	D-24-1AA	B-3	
	AM27S45FM	AM27S47FM	F-24-1	C-3	
	AM27S45FMB	AM27S47FMB	F-24-1	B-3	
	AM27S45LM	AM27S47LM	L-32-2	C-3	
	AM27S45LMB	AM27S47LMB	L-32-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.
4. This package will be available soon. Consult Factory.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27S40A • Am27S41A
Am27S40 • Am27S41

16,384-Bit Generic Series Bipolar IMOX™ PROM
(4096 x 4 bits with ultra fast access time)

DISTINCTIVE CHARACTERISTICS

- Ultra fast access time "A" version (35ns max) – Fast access time Standard version (50ns max) – allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

These 16K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

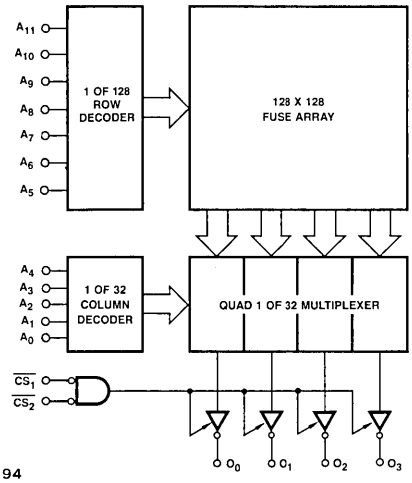
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX™. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

The Am27S40A, Am27S41A, Am27S40, and Am27S41 are high speed electrically programmable Schottky read only memories. Organized in 4096 x 4 configuration, they are available in both open collector (Am27S40A and Am27S40) and three-state (Am27S41A and Am27S41) output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_{11} and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, LOW. If either chip select input goes to a logic HIGH, O_0-O_3 go to the OFF or HIGH impedance state.

BLOCK DIAGRAM



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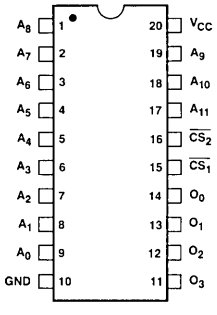
CONNECTION DIAGRAMS – Top Views

DIP



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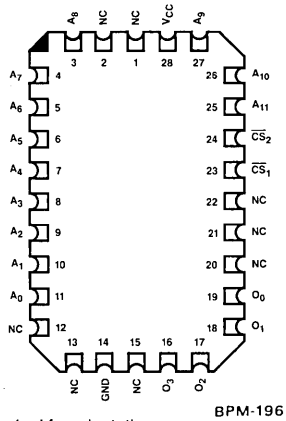
Chip-Pak™



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Note: Pin 1 is marked for orientation.

IMOX is a trademark of Advanced Micro Devices, Inc.
Chip-Pak is a trademark of Advanced Micro Devices, Inc.

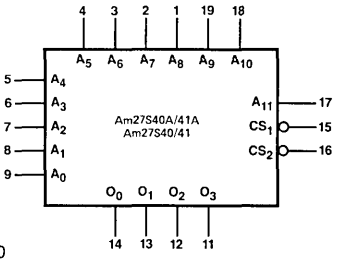
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Type (Note 1)	Max	Units
V_{OH} (TS Devices only)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}	COM'L			0.45	Volts
			MIL			0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC} (TS Devices only)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	COM'L	−20	−40	−90	mA
			MIL	−15	−40	−90	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	COM'L		110	165	mA
			MIL		110	170	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $V_{\overline{CS}_1}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			8.0		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

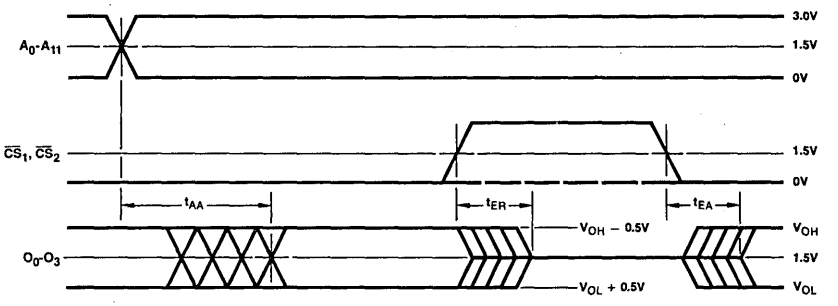
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	Typ 5V 25°C A	Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1, 2, 3)	25	30	35	50	50	65	ns
t_{EA}	Enable Access Time		10	10	25	25	30	30	ns
t_{ER}	Enable Recovery Time		10	10	25	25	30	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three-state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

2

SWITCHING CHARACTERISTICS



Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

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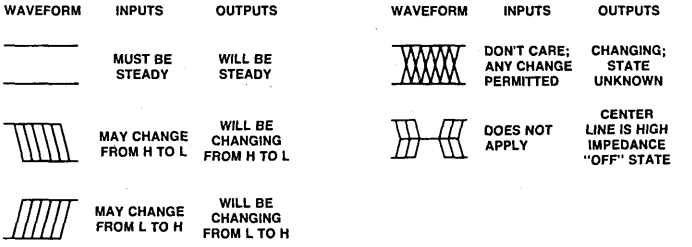
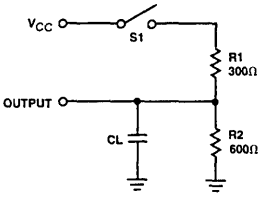
KEY TO TIMING DIAGRAM



AC TEST LOAD



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PROGRAMMING

This entire Generic PROM Series is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS_1}$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS_1}$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled, and the output level sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS_1}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

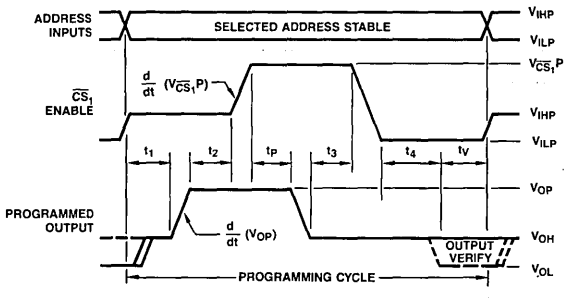
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{CS_1}P}$	$\overline{CS_1}$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{CS_1}})/dt$	Rate of $\overline{CS_1}$ Voltage Change	50	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_v, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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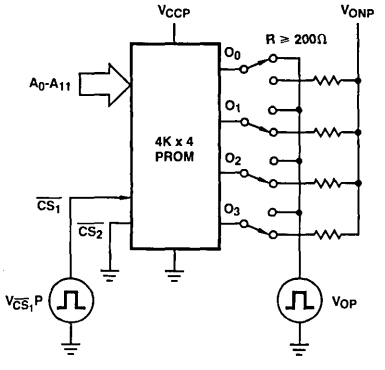
SIMPLIFIED PROGRAMMING DIAGRAM



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PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 3 Tevuot Haaretz St. Tel-Aviv, Israel		Stag Systems, Inc. 1120 San Antonio Rd. Palo Alto, CA 94303
Programmer Model(s)	Model 5, 7, and 9 Systems 17 and 19	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S40A/41A Am27S40/41	715-1282	PA 20-9 and 4096 x 4(L)	IM 4096 x 4-20-AMD	SA 30 B 4096 x 4/20	DIS-216 AM	DA 63	AM 120-6

*Rev shown is minimum approved revision.

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OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 4096 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.5 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

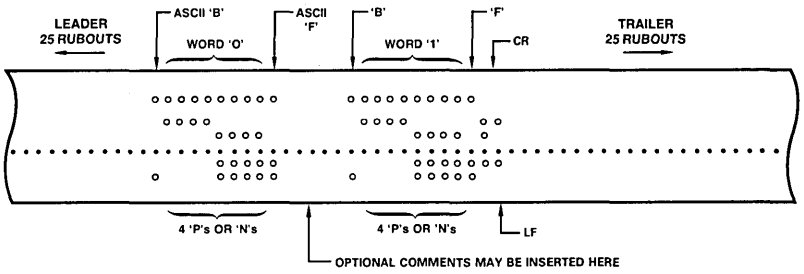
TYPICAL PAPER TAPE FORMAT

```
ØØØ   BNNNPF   WORD ZERO (R) (L)
      BPPNNF   COMMENT FIELD (R) (L)
ØØ2   BPPPNF   ANY (R) (L)
      BNNNNF   TEXT (R) (L)
ØØ4   BNNNPF   CAN (R) (L)
      BPPNNF   GO (R) (L)
ØØ6   BPPNNF   HERE (R) (L)
 .    ......    .
 .    ......    .
4095  BPPPNF   END (R) (L)
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS_1}$ AND $\overline{CS_2}$ = LOW)

A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	L	L	L	H	H	L	H	H	L	L
H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

ASCII PAPER TAPE



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ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM27S40APC	AM27S41APC	P-20-1	C-1	COM'L
	AM27S40APCB	AM27S41APCB	P-20-1	B-1	
	AM27S40ADC	AM27S41ADC	D-20-1	C-1	
	AM27S40ADCB	AM27S41ADCB	D-20-1	B-1	
	AM27S40ALC	AM27S41ALC	L-28-2	C-1	
	AM27S40ALCB	AM27S41ALCB	L-28-2	B-1	
50ns	AM27S40ADM	AM27S41ADM	D-20-1	C-3	MIL
	AM27S40ADMB	AM27S41ADMB	D-20-1	B-3	
	AM27S40ALM	AM27S41ALM	L-28-2	C-3	
	AM27S40ALMB	AM27S41ALMB	L-28-2	B-3	
50ns	AM27S40PC	AM27S41PC	P-20-1	C-1	COM'L
	AM27S40PCB	AM27S41PCB	P-20-1	B-1	
	AM27S40DC	AM27S41DC	D-20-1	C-1	
	AM27S40DCB	AM27S41DCB	D-20-1	B-1	
	AM27S40LC	AM27S41LC	L-28-2	C-1	
	AM27S40LCB	AM27S41LCB	L-28-2	B-1	
65ns	AM27S40DM	AM27S41DM	D-20-1	C-3	MIL
	AM27S40DMB	AM27S41DMB	D-20-1	B-3	
	AM27S40LM	AM27S41LM	L-28-2	C-3	
	AM27S40LMB	AM27S41LMB	L-28-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27PS41

16,384-Bit Generic Series Bipolar IMOX™ PROM
4096 x 4 Bits with Power-Down Via $\overline{CS}$

DISTINCTIVE CHARACTERISTICS

- Fast access time Standard version (50ns max) – allows tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

This 16K PROM is a member of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

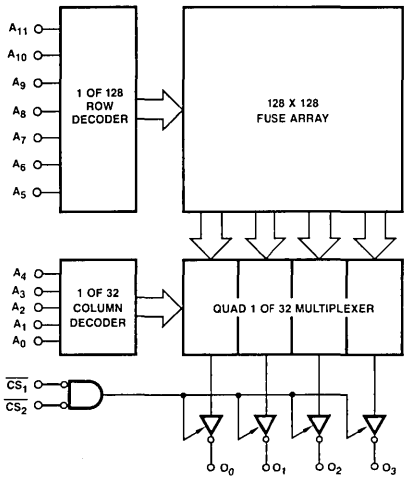
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

The Am27PS41 is a high speed electrically programmable Schottky read only memory. Organized in 4096 x 4 configuration, it is available in the three-state (Am27PS41) output version. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_{11} and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, LOW. If either chip select input goes to a logic HIGH, O_0-O_3 go to the OFF or HIGH impedance state.

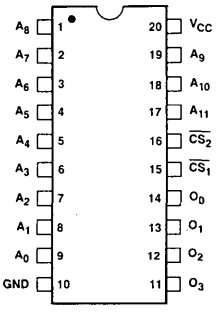
BLOCK DIAGRAM



BPM-194

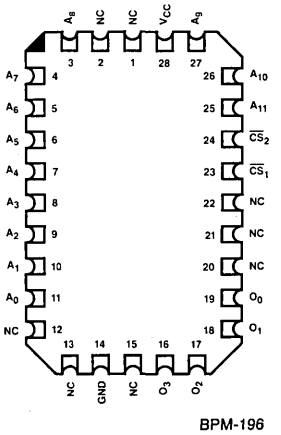
CONNECTION DIAGRAMS – Top Views

DIP



BPM-195

Chip-Pak™ L-28-2



BPM-196

Note: Pin 1 is marked for orientation.

IMOX is a trademark of Advanced Micro Devices, Inc.
Chip-Pak is a trademark of Advanced Micro Devices, Inc.

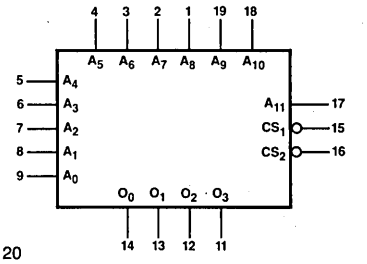
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA, V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA, V_{IN} = V_{IH} or V_{IL}	COM'L			0.45	Volts
			MIL			0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	COM'L	−20	−40	−90	mA
			MIL	−15	−40	−90	
I_{CC}	Power Supply Current	All inputs = GND			110	170	mA
		$\overline{CS}_1$ = 2.7V, All other inputs = GND			50	85	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS}_1}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			8.0		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

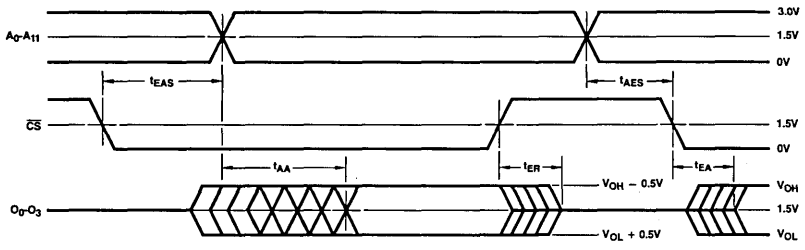
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions		Typ	Max		Units
				5V 25°C	COM'L	MIL	
t_{AA1}	Address Access Time	$t_{EAS} \geq 25ns$	AC Test Load (Notes 1 and 2)	30	50	65	ns
t_{AA2}	Power Switched Address Access Time	$t_{EAS} = 0ns$		50	70	85	ns
t_{EA}	Enable Access Time	$t_{AES} \geq 0ns$		50	70	85	ns
t_{ER}	Enable Recovery Time			10	25	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and $C_L = 30pF$. t_{EAS} is defined as chip enable setup time.
2. For the three-state output, t_{EA} is tested with $C_L = 30pF$ to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with $C_L = 5pF$. HIGH to high impedance tests are made with S_1 open to an output voltage of $V_{OH} - 0.5V$; LOW to high impedance tests are made with S_1 closed to the $V_{OL} + 0.5V$ level.

2

SWITCHING WAVEFORMS



Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

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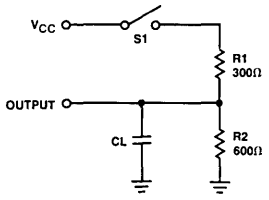
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



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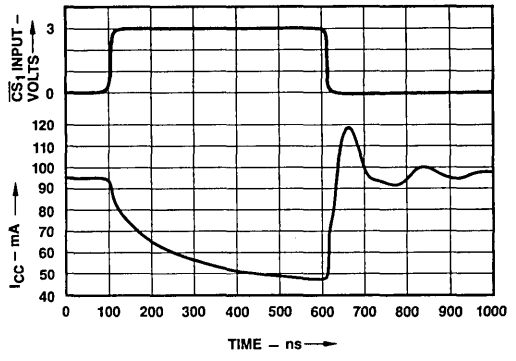
POWER SWITCHING

The Am27PS41 is a power switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS41 is selected by a low level on $\overline{CS}_1$, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μF ceramic capacitor be connected from pin 20 to pin 10 at each device. (See Figure 1.)
2. Address access time (t_{AA}) can be optimized if a chip enable set-up time (t_{EAS}) of greater than 25ns is observed. Negative set-up times on chip enable ($t_{EAS} < 0$) should be avoided. (For typical and worse case characteristics, see Figure 2.)

Typical I_{CC} Current Surge without 0.1μF (I_{CC} is Current Supplied by V_{CC} Power Supply)



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Typical I_{CC} Current Surge with 0.1μF (I_{CC} is Current Supplied by V_{CC} Power Supply)

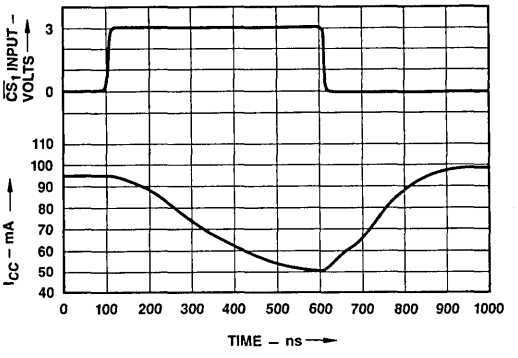

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Figure 1. I_{CC} Current

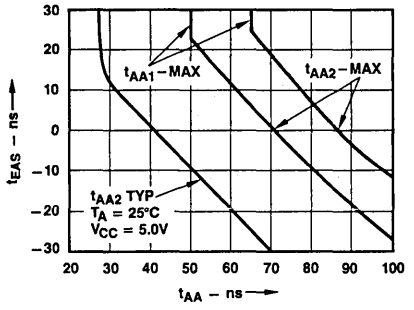

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Figure 2A. t_{AA} versus t_{EAS}

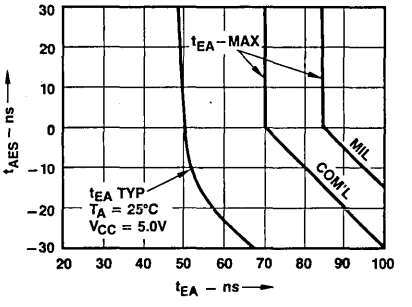

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Figure 2B. t_{EA} versus t_{AES}

PROGRAMMING

This entire Generic PROM Series is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled, and the output level sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

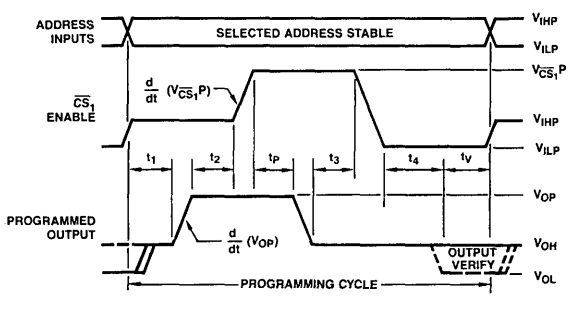
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{CS}_1P}$	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{CS}_1})/dt$	Rate of $\overline{CS}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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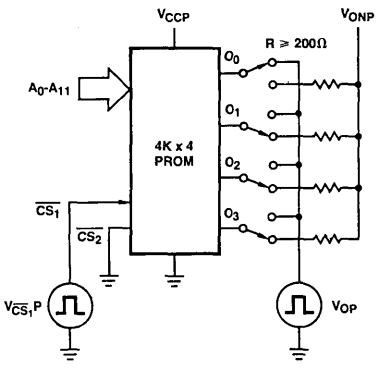
SIMPLIFIED PROGRAMMING DIAGRAM



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PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27PS41	715-1282	PA 20-9 and 4096 x 4(L)	IM 4096 x 4-20-AMD	SA 30 B 4096 x 4/20	DIS-216 AM	DA 63	AM 120-6

*Rev shown is minimum approved revision.

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
t_{AA1} = 50ns t_{AA2} = 70ns	AM27PS41PC	P-20-1	C-1	COM'L
	AM27PS41PCB	P-20-1	B-1	
	AM27PS41DC	D-20-1	C-1	
	AM27PS41DCB	D-20-1	B-1	
	AM27PS41LC	L-28-2	C-1	
	AM27PS41LCB	L-28-2	B-1	
t_{AA1} = 65ns t_{AA2} = 85ns	AM27PS41DM	D-20-1	C-3	MIL
	AM27PS41DMB	D-20-1	B-3	
	AM27PS41LM	L-28-2	C-3	
	AM27PS41LMB	L-28-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am27S43A • Am27S43

32,768-Bit Generic Series Bipolar IMOX™ PROM
(4096 x 8 bits with ultra fast access time)

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Ultra fast access time "A" version (40ns max) – Fast access time Standard version (55ns max) – allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123

GENERIC SERIES CHARACTERISTICS

These 32K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

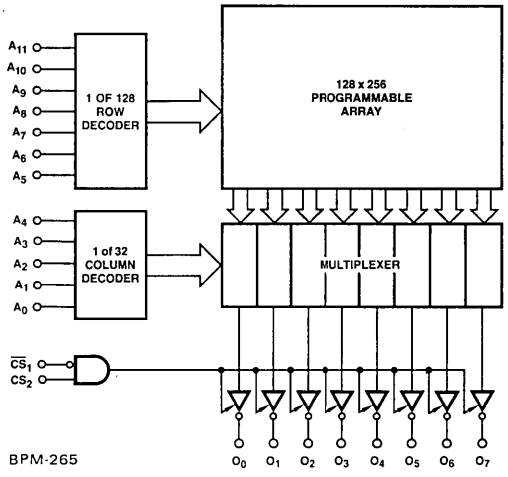
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX™. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

The Am27S43A and Am27S43 are high speed electrically programmable Schottky read only memories. Organized in 4096 x 8 configuration, they are available in three-state (Am27S43A and Am27S43) output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_{11} and holding the chip select inputs, $\overline{CS}_1$, LOW and CS_2, HIGH. If $\overline{CS}_1$ goes to logic HIGH or CS_2 goes to a logic LOW, O_0-O_7 go to the OFF or HIGH impedance state.

BLOCK DIAGRAM



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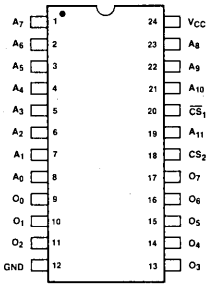
CONNECTION DIAGRAMS – Top Views

DIP



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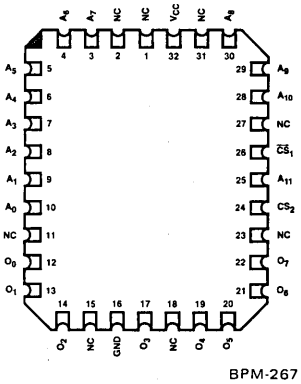
Chip-Pak™ L-32-2



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Note: Pin 1 is marked for orientation.

IMOX is a trademark of Advanced Micro Devices, Inc. Chip-Pak is a trademark of Advanced Micro Devices, Inc.

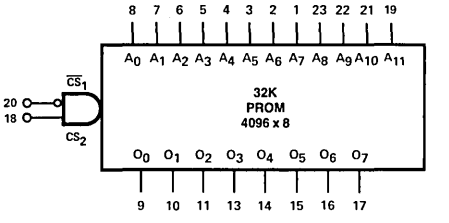
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max Duration of 1 sec)	250mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_C = −55 to +125°C

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

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ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

ADVANCED INFORMATION

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 3)		−15	−40	−100	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	COM'L		135	185	mA
			MIL		135	185	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX, $V_{\overline{CS}_1}$ = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 4)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 4)			8.0		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

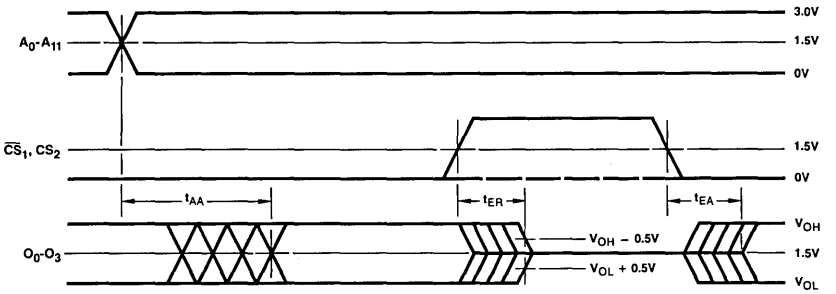
SWITCHING CHARACTERISTICS OVER OPERATING RANGE
ADVANCED INFORMATION

Parameters	Description	Test Conditions	Typ 5V 25°C A	Typ 5V 25°C STD	Max COM'L A	Max COM'L STD	Max MIL A	Max MIL STD	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1 and 2)	30	35	40	55	55	65	ns
t_{EA}	Enable Access Time		20	20	30	35	35	40	ns
t_{ER}	Enable Recovery Time		20	20	30	35	35	40	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For three-state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} −0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} +0.5V level.

2

SWITCHING CHARACTERISTICS



Note: Level on output while $\overline{CS}_1$ is HIGH or CS_2 is LOW is determined externally.

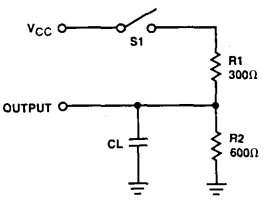
BPM-269

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



BPM-199

PROGRAMMING

The entire Generic PROM Series is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled, and the output level sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

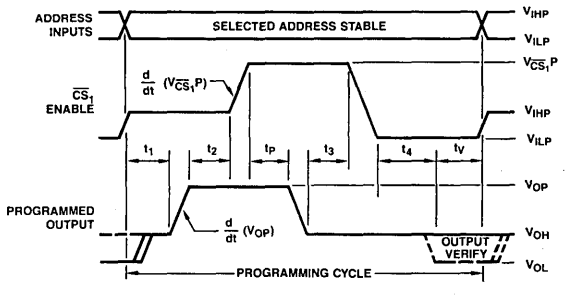
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameters	Description	Min	Max	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
$V_{\overline{CS}_1P}$	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP} + 0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{\overline{CS}_1})/dt$	Rate of $\overline{CS}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

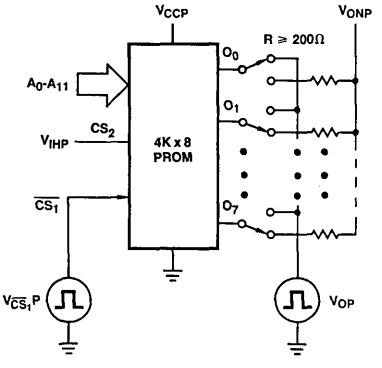
Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



BPM-200

SIMPLIFIED PROGRAMMING DIAGRAM



BPM-270

PROM PROGRAMMING EQUIPMENT INFORMATION

The PROM Programming Equipment from the following manufacturers has been evaluated and approved by AMD:

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 95603	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7, and 9 Systems 17, 19, 29 and 100	M900, M900B, M910, M920, and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 Rev H* 919-1286-1 Rev H*	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Am27S43A/43	715-1698-002		IM 4096 x 8-24-AMD				

*Rev shown is minimum approved revision.

2

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

ORDERING INFORMATION

Speed Selection	Order Code Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
40ns	AM27S43APC	P-24-1AC	C-1	COM'L
	AM27S43APCB	P-24-1AC	B-1	
	AM27S43ADC	D-24-1AC	C-1	
	AM27S43ADCB	D-24-1AC	B-1	
	AM27S43ALC	L-32-2	C-1	
	AM27S43ALCB	L-32-2	B-1	
55ns	AM27S43ADM	D-24-1AC	C-3	MIL
	AM27S43ADMB	D-24-1AC	B-3	
	AM27S43ALM	L-32-2	C-3	
	AM27S43ALMB	L-32-2	B-3	
55ns	AM27S43PC	P-24-1AC	C-1	COM'L
	AM27S43PCB	P-24-1AC	B-1	
	AM27S43DC	D-24-1AC	C-1	
	AM27S43DCB	D-24-1AC	B-1	
	AM27S43LC	L-32-2	C-1	
	AM27S43LCB	L-32-2	B-1	
65ns	AM27S43DM	D-24-1AC	C-3	MIL
	AM27S43DMB	D-24-1AC	B-3	
	AM27S43LM	L-32-2	C-3	
	AM27S43LMB	L-32-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Flat packages are available upon special request. Consult factory.

Technical Report

Reliability Report
Bipolar Generic PROM Series

ABSTRACT

This report is a review of the manufacturing process, the circuit design techniques, the testing, the fuse element, and the reliability of Advanced Micro Devices' Generic Bipolar PROM Series. Results indicate that platinum silicide forms a fuse with excellent reliability characteristics.

The purpose of this report is to present a description of Advanced Micro Devices' Bipolar PROM circuits, their manufacturing process and their reliability. Included is a discussion of the wafer fabrication in which an advanced, highly reliable platinum silicide fuse is utilized, a description of the circuits and their testing, an analysis of the fusing characteristics of platinum silicide and supportive reliability data.

The products evaluated in this report are members of a generic family of field programmable-read-only memories (PROMs) from 256 bits through 16384 bits. Advanced Micro Devices utilizes two manufacturing processes. The first is the platinum-silicide Schottky, washed emitter process described in this report. The second is the IMOX™ process. IMOX is the trademark name for a selective oxide isolation process which employs ion-implantation of various transistor elements. This improved process incorporates many of the technologies previously developed, such as platinum silicide fuses, dual layer metal, and platinum-silicide Schottkies. IMOX allows further reduction in chip size due to tighter device spacings and device dimensions. All new product developments for the PROM family use the IMOX process. This high density process allows Advanced Micro Devices to continue to supply very high speed, high performance products while increasing device complexity. The circuit design concepts are similar on each of the PROMs with the result that the products can be programmed using the same hardware. Only the socket adaptor required for the PROM configuration and pin count is different. The same programming algorithm is used for all devices with completely satisfactory results. The PROMs utilize a platinum Schottky diode structure with barrier metal. Dual-layer metallization is also employed to maximize speed and minimize chip size. All Advanced Micro Devices' circuits receive screening per MIL-STD-883, Method 5004 class C or better. Part of the 883 flow involves sample acceptance tests in which all temperature requirements are sampled to Lot Tolerance Percent Defective (LTPD) plans. A 5% LTPD corresponds to about a 0.65% Acceptance Quality Level (AQL). In early 1981 Advanced Micro Devices announced a new program that guarantees the highest quality levels for semiconductor devices in the industry. The new program is called INTERNATIONAL STANDARD 123. Under INT-STD-123 all Bipolar Memory PROMs are sampled to a 0.3% AQL. This is a direct statement of AMD's commitment to excellence.

Prepared by: Advanced Micro Devices Quality and Reliability Department in Conjunction with Bipolar Memory Engineering.

THE PROCESS TECHNOLOGY

Advanced Micro Devices has chosen a platinum silicide Schottky, washed emitter, dual-layer metal process for its bipolar PROMs. Platinum silicide has been chosen as the material to form the fuse for several reasons. First, it has been demonstrated to be an extremely reliable fuse material. It does not have the growback phenomenon common to nichrome technologies; it is not moisture sensitive in freeze-out tests; it is less fragile than nichrome, and it does not have mass transport problems associated with moderate current densities. Second, the manufacturing process is easily controlled with regard to reliability factors and fusing currents. Third, the fuses are quite easy to form during the manufacturing process without a substantial number of additional processing steps.

Figure 2 is a cross section of a transistor and a fuse. A heavily doped buried layer diffusion is first performed to allow for the fabrication of NPN transistors with low saturation resistances. A thin epitaxial layer is grown followed by isolation and base diffusions. The isolation and base are effectively self-aligned using a composite masking approach. A short series of steps results in the definition of polycrystalline silicon in the shape of the fuse.

A second composite mask now defines all the emitter, contact, Schottky diode and ohmic contact areas.

Following the emitter diffusion and the contact mask, platinum is sputtered over the entire wafer. Since all contacts, Schottkies, and fuses are exposed at this point, an alloying operation allows platinum silicide to form. The residual platinum is etched off the wafer leaving the silicide contacts, Schottkies, and fuses. After this step, the semiconductor elements of the circuit have been completely formed, and all that remains is the interconnect metallization.

To form the interconnects, aluminum is used as the primary conducting element. Aluminum has a very strong affinity for silicon, including that in platinum silicide. To retain the advantages of the very stable platinum silicide Schottky devices, it is necessary to sputter an inactive metal, tungsten, with a small amount of titanium as a bonding agent over the surface of the wafers to serve as a barrier to the diffusion or microalloying of the aluminum. Aluminum is now evaporated over the surface of the wafers and conventional masking and etching cycles are used to define the aluminum interconnections. Figure 3 shows the structure of this metal layer.

To complete the dual-layer metallization structure, silicon dioxide is chemically vapor deposited on the wafer and etched with interlayer metal contact openings (vias). A second layer of aluminum is then placed on top of the dielectric. This layer has a thickness substantially greater than the first one and is especially suited for power busses and output lines.

To complete the circuit, a passivation layer is deposited over the top of the wafers and etched at the appropriate locations to allow for bonding pad contact.

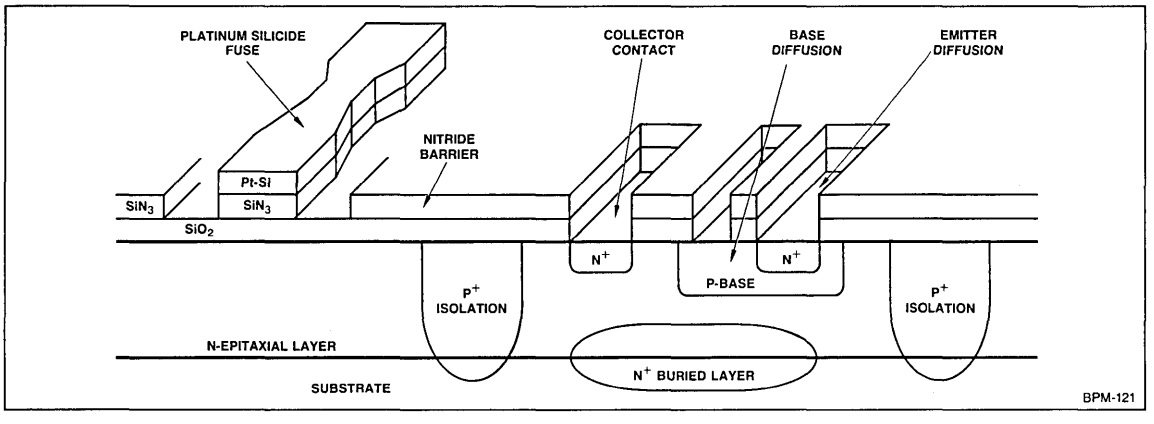


Figure 2. Transistor & Fuse Structures.

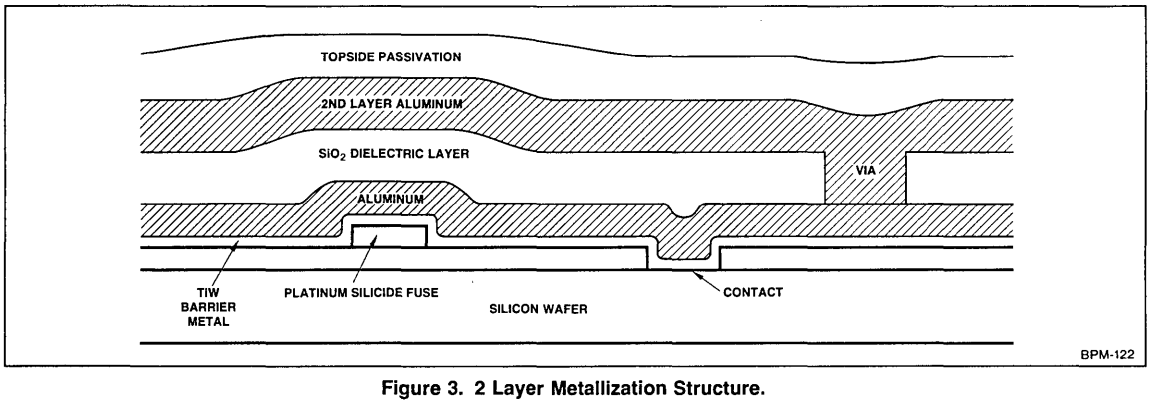


Figure 3. 2 Layer Metallization Structure.

PROGRAMMABLE READ-ONLY MEMORY CIRCUITRY

Advanced Micro Devices' bipolar PROM designs have the general configuration shown in Figure 4. Although the figure is for that of the Am27S20, the circuit techniques are the same for the entire generic family of PROMs.

Input, Memory & Output Circuitry

Two groups of input buffers and decoders called "X" and "Y" are used to drive word lines and columns respectively. The X-decode addresses (A_3-A_7) have Schottky clamp diode protected, PNP inputs for minimum loading. (Figure 5). The X-input buffers (A_3-A_7) provide A and $\overline{A}$ outputs to a Schottky decode matrix which selects one of 64 word drivers. The word line drivers are very fast high current, high voltage, non-saturating buffers providing voltage pull down to the selected word line.

The Y-decode address buffers (A_0-A_2) are also Schottky diode clamped, PNP inputs driving a Schottky diode matrix. However, this diode matrix selects one of eight columns on each of the four output bits. The selected column line drives the sense amplifier input to a high level in the case of a blown fuse, or current is shunted through an unblown fuse through the selected word driver to ground resulting in a "low" input to the sense amplifier.

The sense amplifier is a proprietary fast level shifter-inverter with temperature and voltage threshold sensitivities compensated for the driving circuitry. Each of the four sense amplifiers in this circuit provides active drive to an output buffer.

Each output buffer also contains a disable input, which is driven from the chip-enable buffer. The chip-enable buffer input is a Schottky diode clamped PNP buffered design with an active pull up and pull down to drive the output buffer. Additionally, the chip-enable gate contains circuitry to provide fuse control as described below.

Fusing Circuitry

Platinum silicide fuses as implemented in Advanced Micro Devices' PROMs have extremely high fuse current to sense current ratios. Sensing normally requires that only a few hundred microamps flow through the fuse, whereas absolute minimum requirements for opening the fuse are approximately 100 times that amount. This provides a significant safety margin for transient protection and long-term reliability.

High-yield fusing of platinum silicide fuses requires that a substantial current be delivered to each fuse. This current is sourced from the output terminals through darlingtons which can drive the column lines when enabled. These darlingtons are driven directly from the output and are selected by the Y-decode column select circuitry. Current during fusing flows from the output through the darlington directly to the fuse

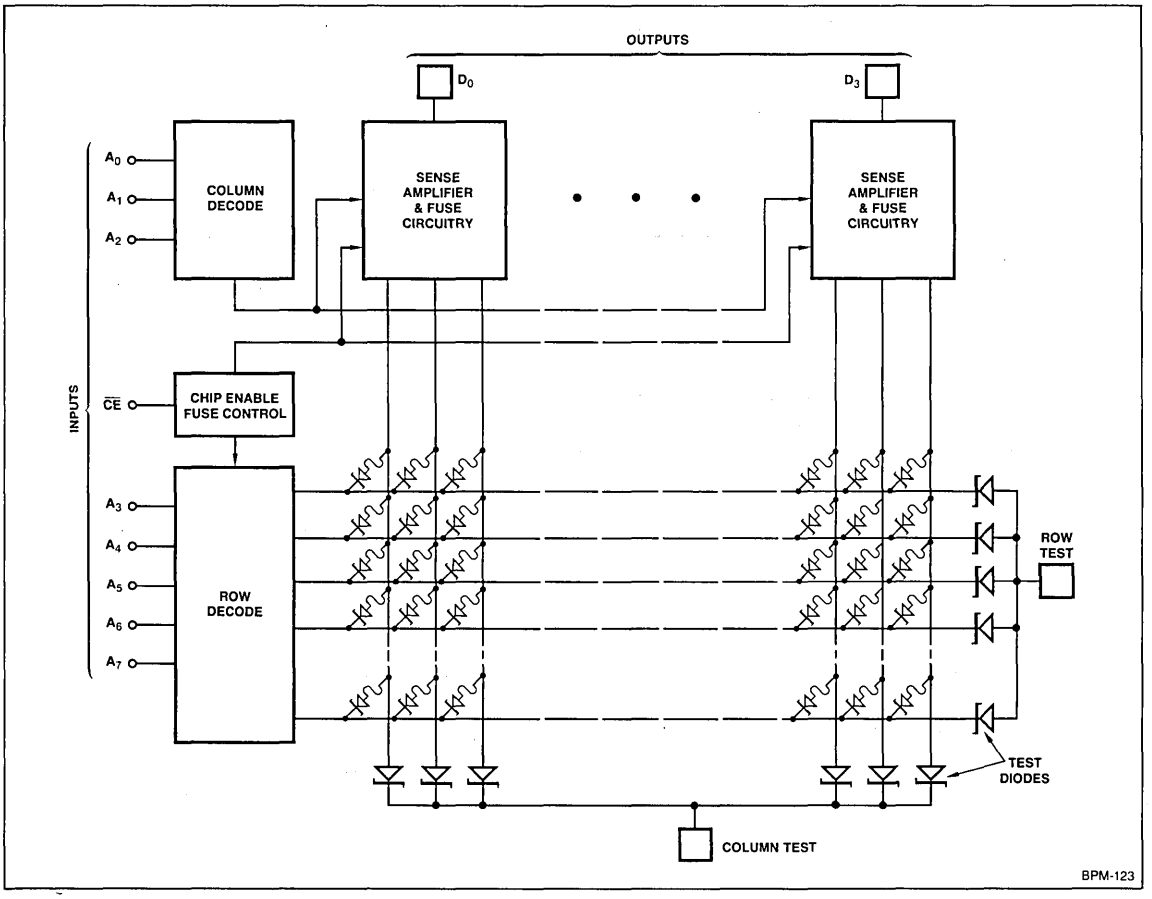


Figure 4. PROM Circuitry Block Diagram.

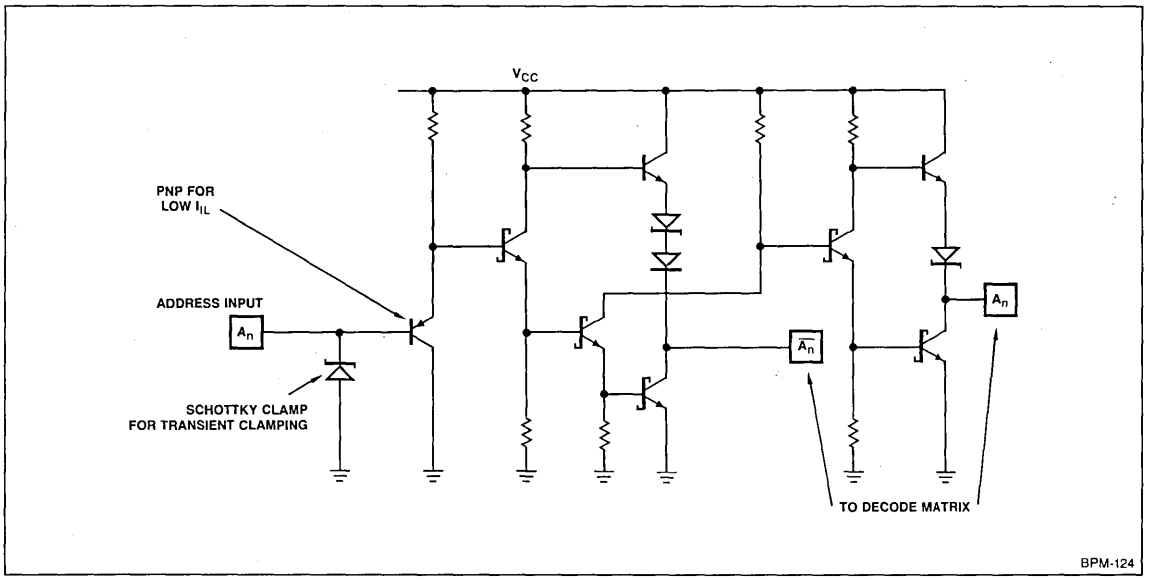


Figure 5. Input Buffer Schematic.

through the selected array Schottky and finally through the word-driver output transistor to ground. This path is designed for a very large fusing current safety margin.

The control circuitry works as follows: After V_{CC} is applied, the appropriate address is selected and the $\overline{CE}$ input is taken to a logic high, the programmer applies 20 volts to the bit output to be programmed. The application of the 20 volts simultaneously deselects the output buffer to prevent destructive current flow, and powers down internal circuitry unneeded during fusing to minimize chip heating.

It also enables the darlington base drive circuitry, makes power available to the darlington from the output and enables the fusing control circuitry. At this point, the PROM is ready for the control line at the chip-select pin to release the selected word driver to allow current flow through the fuse. This technique is particularly advantageous because the control signal does not supply the large fusing currents. They are supplied through the darlington from the output power supply. Some care must be taken to avoid excessive line inductance on the output line. Reasonable and normal amounts of care will reward the user with high-programming yields.

Special Test Circuitry

All Advanced Micro Devices PROMs include high-threshold voltage gates paralleling several address lines to allow the selection of special test words and the deselection of the columns to allow for more complete testing of the devices. Additionally, special test pads accessible prior to assembly allow for testing of some key attributes of the devices. The function of these special circuits will be described in more detail in the section, "Testing", later in this report.

THE PLATINUM SILICIDE FUSE

Fusing Technique

Advanced Micro Devices' PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer yet allows the circuit to fuse the platinum silicide links quickly and reliably. Specifically, the following sequence of events must take place:

1. V_{CC} power is applied to the chip;
2. The appropriate address is selected;
3. The chip is deselected;
4. The programming voltage is applied to one output;
5. The chip enable voltage is raised to enable high-threshold voltage gate. This action gates the current flow through the proper fuse resulting in an open fuse in a few microseconds;
6. The output voltage is lowered; the programming voltage is removed.
7. The device is enabled and the bit is sensed to verify that the fuse is blown. In the unusual event that the fuse does not verify as blown, a sequence of much longer pulses is applied to the fuse at a high duty cycle until the fuse opens; and,
8. The sequence of 2 through 7 is repeated for each bit which must be fused.

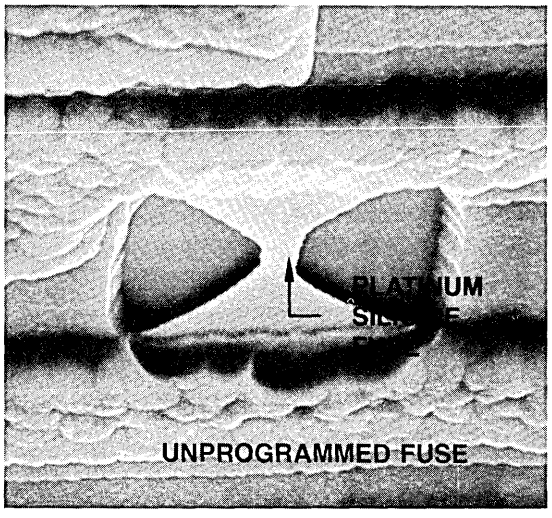
There are several advantages to this technique. First, the two high current power sources, V_{CC} and the voltage applied to the output do not have critical timing requirements. The low current chip select pin gates the fusing current into the circuit. Since it is generally desirable to gate the fusing current into the chip at relatively fast rates, the use of the chip select for this purpose avoids the speed trade-off which would exist using the output voltage as the control. The output voltage must not be raised too quickly to avoid breakdown and latchback conditions which might occur with sub-microsecond rise times on the output.

The second major advantage of this technique is that in the event that the fuse does not open during the first attempt to blow it, a near DC condition may be safely applied to it with no danger of developing a reliability problem such as that which occurs with nichrome fuses. This will be discussed in more detail later. The algorithm can therefore be designed first to minimize the time required to program the PROM, i.e. with a fast first pulse, and second, to maximize the probability that any circuit will program. Most PROMs do, of course, fuse satisfactorily with all short pulses. However, it is impossible for any manufacturer to guarantee absolutely that all fuses in all circuits receive 100 percent of the rated fusing current during programming.

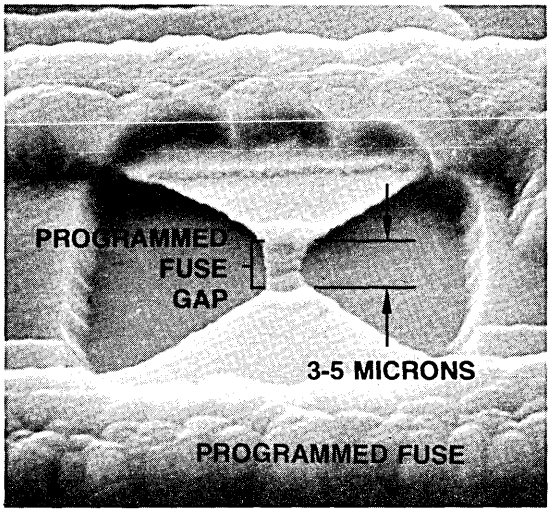
Circuit defects which may be resistant to pre-programming testing prevent such a guarantee. It is, therefore, quite important to have a fuse material insensitive to marginal conditions. Even the application of single, short pulses does not guarantee that no fuse received marginal amounts of current during fusing. The silicide fuse provides this safety margin and allows the programmer to maximize the possibility of fusing by applying near DC condition to the fuses.

Fuse Characteristics

When a fast (less than 500ns rise time) current pulse is applied to a fuse, the fuse voltage rises abruptly to a value approaching the level anticipated from calculations of the room temperature resistance. However, it quickly falls to a value of approximately two volts. This value is nearly independent of the applied current. During this period of time, typically, the fuse is molten. Very abruptly, the fuse current drops to zero indicating the separation of the platinum silicide into two distinct sections. Scanning Electron Microscope photographs of the resulting fuses (see Figure 6) indicate that the typical case is a sharp, clean separation in excess of a micron. This separation occurs in the center of the fuse because the bow-tie structure (see Figure 7) concentrates the energy density in the center away from the aluminum lines. The energy density in the center of the fuse is capable of creating temperatures substantially greater than required to melt the silicide. The very abrupt, high



Unprogrammed Fuse



Programmed Fuse

Figure 6.

power applied to the fuse melts the fuse center and results in a wicking of material on either side due to surface tension.

Reliability of Fuses Programmed Under Non-optimal Conditions

The marginally opened fuse has been studied in some detail even though it rarely occurs in practice. Under conditions where the fuse is purposely blown at much slower rates, it is possible for the fuse to assume a high impedance state which is sensed as an open fuse by the circuit. This occurs because the fuse cools before separation is achieved. Electrical and SEM studies of fuses blown with these characteristics indicate that a small conductive path of silicon remains of sufficiently high resistance to prevent appropriate power transfer required for complete opening on subsequent applications of power. Under these slow-blow conditions, the thermal conductivity of the silicon nitride pedestal on which the fuse rests, the silicon dioxode beneath that, and the silicon chip become factors because sufficient time exists for the heat flow to carry a significant amount of energy away from the fuse. This is extremely unusual in practice since it requires a rather narrow set of conditions. However, a number of PROMs have been specially programmed under these unusual conditions which can cause this type of fuse to occur. These devices have been life tested for over two thousand hours. No failures occurred in any of these circuits. It is clear from this study that partially opened platinum silicide fuses are stable. Although it is very rare to see such a fuse in a circuit which has been programmed under normal conditions, Advanced Micro Devices believes that such fuses do not represent a reliability hazard based on this study and the results of the other studies run on the programmable-read-only memories. It should be noted that most manufacturers carefully specify the conditions under which their devices *must* be programmed in order to avoid reliability problems. Reliability data available on these devices must be assumed to have been generated using optimally programmed devices. Advanced Micro Devices believes that the study described here and four billion fuse hours of data from many production lots of PROMs demonstrate the capability of the platinum slicide fuse under a wide variety of conditions.

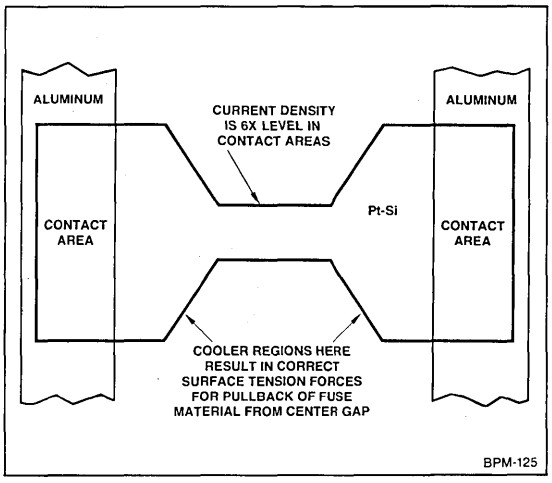


Figure 7. Bowtie Fuse Design.

FINAL TESTING OF ADVANCED MICRO DEVICES' MEMORIES

Wafer Level Tests

In addition to all the standard DC tests, Advanced Micro Devices performs a series of special tests to conform to the screening criteria of MIL-STD-883, Method 5004 3.3 and the 0.3% AQL INT-STD-123. Also, AMD performs special tests to increase the confidence level of unique address selection and to demonstrate fusing capability on all columns and word drivers. To accomplish this, diodes are connected from the column lines and the word lines to special test pads which are accessible only during wafer probing. (See Figure 4). Using these diodes, Advanced Micro Devices confirms that each word driver is capable of sinking sufficient current to blow fuses, has appropriate saturation characteristics for AC performance, and has sufficient voltage breakdown to withstand fusing voltages. In addition, using special software, a sequence of tests dramatically increases the confidence of unique address selection on the address decoding. All darlingtons are checked to confirm that sufficient current drive is available to blow fuses from any column. Schottky diode array leakage is also checked to affirm that it is sufficiently low so as not to overload the pull down circuitry during the high-voltage application of fusing. Finally, high voltages are applied to the inputs and outputs to remove potentially weak devices before the PROM's are assembled.

Test Fusing

Each PROM has two additional word drivers connected to special test fuses. These test words are valuable in demonstrating beyond reasonable doubt that the device is capable of opening fuses in all columns. They also increase the confidence level in unique addressing. Furthermore, the test words serve as correlatable measures of the access times that the user can expect from his devices after he has placed his own program in the memory. These test words are not visible to the user unless he applies special voltages to certain address pins. Figure 8 is a diagram of this input circuit. One hundred percent of the PROM devices shipped from Advanced Micro Devices have had AC testing for access and enable times at high-and low-power supply voltages to affirm their AC characteristics.

The result of this extensive testing at both the wafer and finished device level is a product with very high-programming yields and virtually guaranteed AC performance after the user places his program in the parts. Additionally, the high voltage tests provide an additional level of confidence that the oxide and junction integrity is excellent in each circuit and that the devices will be relatively insensitive to small transients common to programming equipment.

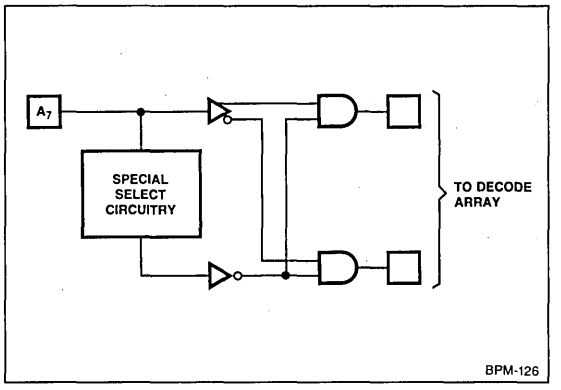


Figure 8. Special Input Circuit Used for Array Deselection and Test Word Check.

THE MANUFACTURING PROCESS

All products bearing the Advanced Micro Devices' logo will have screening meeting the requirements of the MIL-STD-883 Method 5004, for Class C microcircuits and INT-STD-123 Quality Levels. A summary of the standard processing is shown below. The presence of the Advanced Micro Devices' logo on the package is confirmation that the screening has been completed. The only exceptions to this procedure are special products revised by contract for a customer's lesser requirements and distinctly marked for that customer alone. Standard burn-in option B is available on standard product which allows the customer to upgrade to Class B microcircuits.

Assembly and Environmental Standard Processing

1. Die Visual Inspection	Method 2010 Condition B
2. Wire Bond	Method 2010 Condition B rebonds less than 10 percent
3. Internal Visual	Method 2010 Condition B
4. Seal	
5. High Temperature Storage	Method 1008 Condition C
6. Temperature Cycle	Method 1010 Condition C
7. Constant Acceleration	Method 2001 Condition E
8. Visual Inspection	Method 5004
9. Fine Leak	Method 1014 Condition A or B
10. Gross Leak	Method 1014 Condition C Step 2

Note: Steps 7-10 not required for solid packages.

Electrical Test through Shipping Standard Processing

1. Initial Electrical Test	Method 5004 to device specifications.
2. Group A Electrical	INT-STD-123 quality levels.
3. Mark	Per customer order or Advanced Micro Devices catalog identification.
4. External Visual	Method 2009
5. Sample Quality Inspection	Physical or electrical verification of product identity.

RELIABILITY TESTING

Advanced Micro Devices has an ongoing reliability program to evaluate its bipolar memory products. Reliability testing conforms to MIL-STD-883 Method 1005 Conditions C or D. Examples of the test circuits used are shown in Figure 9. Data has now been accumulated on the process described here in excess of ten thousand hours on some devices. Over forty billion fuse hours have been completed with no fuse oriented failures.

Advanced Micro Devices selects samples of its product stratified by product type at periodic intervals for this testing. Figure 10 is a tabulation of the results of the lots placed on test during this period of time. The data demonstrates a highly reliable process. The fuse has an immeasurably low contribution to the failure rate at this point in the reliability testing.

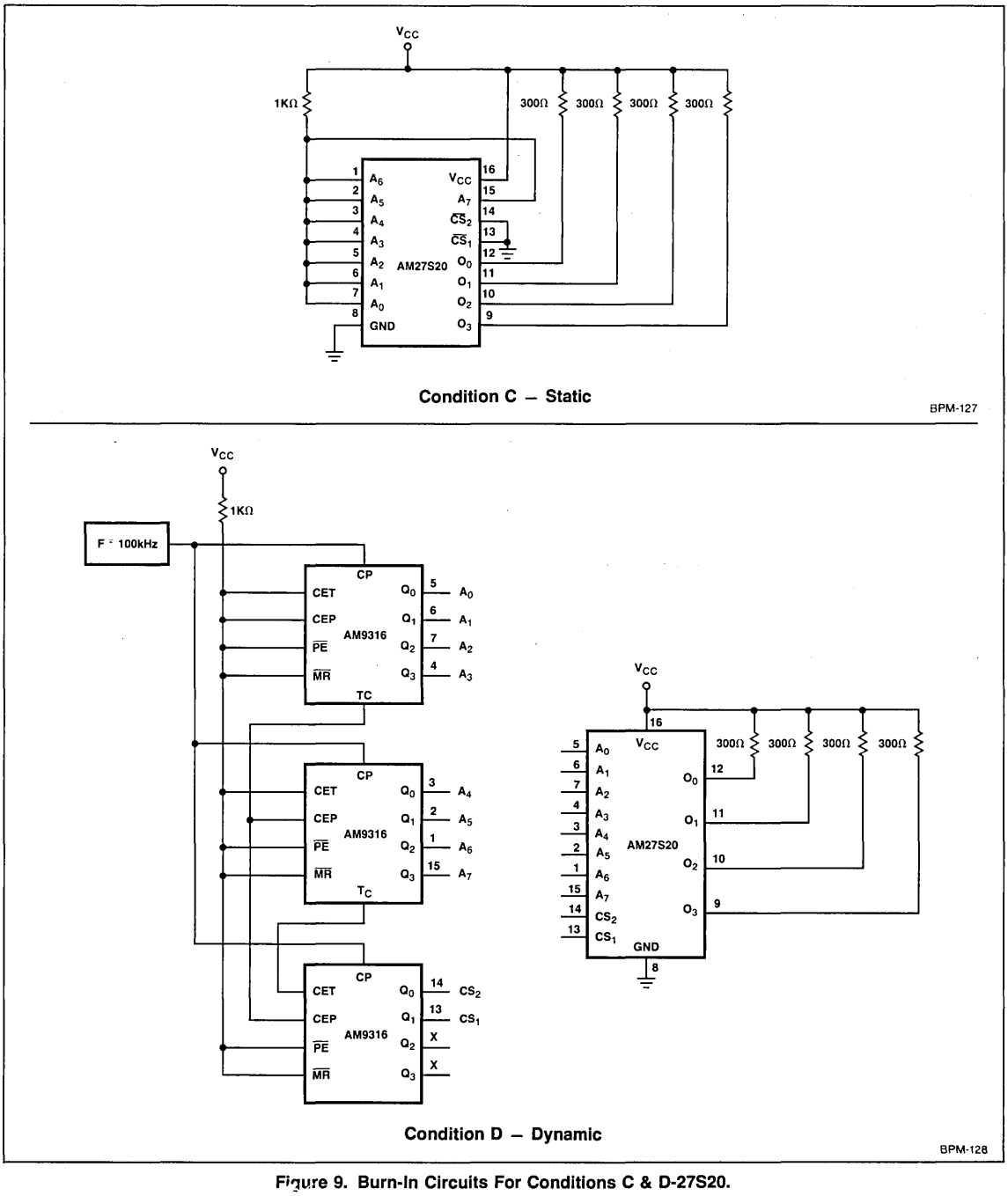


Figure 9. Burn-In Circuits For Conditions C & D-27S20.

BIPOLAR MEMORY RELIABILITY SUMMARY

Product	Production Lots	Units Tested	Total Unit Hours (thousands)	Total Fuse Hours (billions)	Unit Failures	Fuse Related Failures	Unit Failure Rate @ 60% Confidence %/1000 hrs at 125°C	Unit Failure Rate* @ 60% Confidence %/1000 hrs at 70°C
27S18/19 (256 bit PROM)	5	491	982	.251B	0	0	0.10	0.0010
27S20/21 (1K bit PROM)	16	1321	2207	2.260B	2**	0	0.01	0.0001
27S12/13 (2K bit PROM)	11	571	1840	3.768B	0	0	0.05	0.0005
27S15 27S27 27S28/29 27S32/33 (4K bit PROM)	24	1870	1408	5.767B	0	0	0.07	0.0007
27S180/181 (8K bit PROM)	12	463	926	7.586B	0	0	0.11	0.0010
27S184/185 IMOX (8K bit PROM)	15	556	1112	9.109B	0	0	0.09	0.0008
27S190/191 IMOX (16K bit PROM)	2	69	795	13.025B	0	0	0.12	0.0011
Totals for PROM products	85	5341	9270	41.766B	2**	0	0.02	0.0002

*Assuming on activation energy of 1.0 eV.
**Oxide failure.

Figure 10.

SUMMARY

The Advanced Micro Devices' bipolar memory process has been described with particular emphasis on programmable-read-only memories. An advanced form of the low-power Schottky process is used in conjunction with a highly reliable and stable platinum silicide fuse. Extensive testing and screening have been used to assure that the products will meet all specification after the user has placed his program into the device and that the circuit reliability will be outstanding.

Guide to the Analysis of Programming Problems

2

Advanced Micro Devices Bipolar Memory Product Engineering

INTRODUCTION

Advanced Micro Devices' Generic Series of Programmable Read Only Memory (PROM) circuits have been designed to provide extremely high programming yields. Available programming currents are over designed by a factor of four and special circuitry accessible only during testing is incorporated into each product to eliminate ordinarily difficult to detect shorts and opens in the array and decoders. As a result, unique decoding and very large fusing currents are virtually assured to the user. AMD PROMs have test fuses programmed prior to shipment as a further guarantee. The results of such extensive testing and design considerations are programming yields consistently in the 98% to 99.5% range.

Key to the achievement of such yields is a programmer properly calibrated to the AMD specification with good contactors, "clean" electrical wave forms and properly functioning subcircuits. In the event that your programming yields fall below 98%, you should investigate the characteristics of the failed devices to find a prominent failure mode, then use the attached information as a guide to resolving the problem. Simple problems can be very costly if not detected and corrected.

Should you continue to have trouble optimizing your programming yield, contact your AMD representative or local programmer manufacturer representative.

Guide to the Analysis of Programming Problems

Primary Symptom	Secondary Symptom	Possible Causes
I) Units fail to program all desired bits	A) Binary blocks of missing data	1) Address driver output which remains continuously low or continuously high. 2) Address driver with a "low" voltage greater than 0.5V or a "high" voltage less than 2.4V. 3) Poor, intermittent or no electrical contact to one or more address input pins. Any of the above may result in over programming half the array and not programming the other half.
	B) Random bits of missing data	1) Address driver with a "low" voltage greater than 0.5V or a "high" voltage less than 2.4V. 2) Poor electrical contact to address, chip enable and output pins. 3) Excessive transient noise on V_{CC}, output pin (> 20.5V), or ground pins. Check with a high speed storage oscilloscope for peak values during programming. Use transient suppression networks where appropriate. 4) Programmer does not comply with AMD Programming Specification. (See Programming Parameters.) Examples: – Output voltage during programming less than 19.5V – V_{CC} during programming less than 5.0V – $\overline{CS}$ voltage during programming less than 14.5V
	C) All data associated with a single output missing	1) Poor or no electrical contact to that output pin. 2) Defective current switch in programmer.
	D) No data change	1) Wrong device or programming socket. 2) Programmer does not comply with AMD's Programming Specifications. (See Programming Parameters.) Examples: – Output voltage during programming less than 19.5V – V_{CC} during programming less than 5.0V – $\overline{CS}$ voltage during programming less than 14.5V
II) Over-Programmed Devices	A) One output continuously at a Logic "1"	1) Programmer does not comply with AMD's Programming Specifications. (See Programming Parameters.) Examples: – Output voltage during programming greater than 20.5V – Programmer timing incorrect 2) Open outputs can appear to be programmed to Logic "1" with the presence of a pullup resistor even though the device has not actually been programmed. 3) Excessive voltage transients on output lines during programming. Be sure appropriate transient suppression networks are placed on the outputs. (See Figure 1.)
	B) All outputs continuously at a Logic "1"	1) No V_{CC} applied to device. 2) No ground applied to device. 3) Incorrect device type. 4) Incorrect programming socket. 5) Excessive voltage transients on output lines. Use transient suppression network shown in Figure 1.

DEFINITIONS

Fuse
– Conductive Platinum-Silicide link used as a memory element in Advanced Micro Devices' PROM circuits.

Unprogrammed Bit
– A conductive fuse.

Programmed Bit
– A nonconductive fuse, that is one which has been opened.

Output Low (Logic "0")
– An output condition created by an unprogrammed bit.

Output High (Logic "1")
– An output condition created by a programmed bit.

Failure to Program
– A device failure in which a fuse selected to be opened failed to open during the fusing operation.

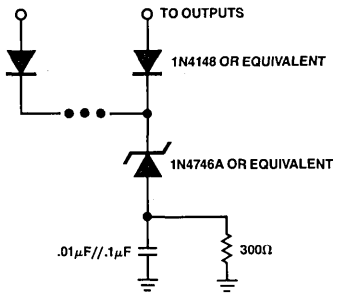
Over Programmed
– A device failure in which a fuse which was not selected to open nevertheless opened during the fusing operation.

Address Driver
– The voltage source which drives an individual address pin in the PROM. This source is part of the programmer and drives the address pin with "0"s (0 to .45V) and "1"s (2.4 to 5.5V) depending on instructions from the programmer control circuitry. There is a separate address driver for every PROM address pin.

Programmer
– A system capable of providing the appropriate array of signals to a PROM circuit to cause certain user controlled bits to be programmed (i.e., fuses opened) in the device. As a minimum it consists of a memory containing the pattern to be programmed, control circuitry to sequence the addressing and fusing control pulses, power supplies, and address drivers.

2

TRANSIENT SUPPRESSION NETWORK



Notes: 1. Clamp diodes should be connected to each output as close as physically possible to the device pin.
2. V_{CC} should be decoupled at the device pin using .01μF//.1μF capacitors.
3. AMD recommends that all address pins be decoupled using .001μF capacitors.

Figure 1.

PROM Programming Equipment Guide

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052		Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 93940	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7 and 9 Systems 17, 19, 29 and 100		M900, M900B, M910, M920 and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 919-1286-1 Rev H	Unipak Rev 003 (Family and Pin Code)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Socket Adapters and Configurators								
Am27S18/19 Am27LS18/19	715-1407-1	16 02	PA 16-6 and 32 x 8(L)	IM 32 x 8-16-AMD	SA 3-1 B 32 x 8/16	DIS-156 AM	DA 22	AM 110-2
Am27S20/21	715-1408-1	16 01	PA 16-5 and 256 x 4(L)	IM 256 x 4-16-AMD	SA 4-2 B 256 x 4/16	DIS-133 AM	DA 21	AM 130-2
Am27S12/13	715-1408-2	16 03	PA 16-5 and 512 x 4(L)	IM 512 x 4-16-AMD	SA 4-1 B 512 x 4/16	DIS-134 AM	DA 21	AM 130-3
Am27S15	715-1411-1	–	PA 24-14 and 512 x 8(L)	IM 512 x 8-24-27S15-AMD	SA 17-3 B 512 x 8/24	DIS-165 AM	DA 33	–
Am27S25	715-1617	62 65	PA 24-16 and 512 x 8(L)	IM 512 x 8-24-27S25-AMD	SA 31-2 B 512 x 8/24	DIS-213 AM	DA 31	AM 190-2
Am27S27	715-1412-2	–	PA 22-4 and 512 x 8(L)	IM 512 x 8-22-27S27-AMD	SA 18 B 512 x 8/22	DIS-168 AM	DA 28	–
Am27S28/29	715-1413	16 09	PA 20-4 and 512 x 8(L)	IM 512 x 8-20-AMD	SA 6 B 512 x 8/20	DIS-158 AM	DA 34	AM 120-3
Am27S30/31	715-1545	16 36	PA 24-13 and 512 x 8(L)	IM 512 x 8-24-AMD	SA 22-6 B 512 x 8/24	DIS-135 AM	DA 29	–
Am27S32/33	715-1414	16 38	PA 18-6 and 1024 x 4(L)	IM 1024 x 4-18-AMD	SA 24 B 1024 x 4/18	DIS-136 AM	DA 38	AM 170-2
Am27S35 Am27S37	715-1723	62 66	PA 24-18 and 1025 x 8(L)	IM 1024 x 8-27S35/37-AMD	SA 31-1 B 1024 x 8/24	DIS-218 AM	DA 65	AM 190-3
Am27S180/181 Am27PS181	715-1545-2	16 37	PA 24-13 and 1024 x 8(L)	IM 1024 x 8-24-AMD	SA 22-7 B 1024 x 8/24	DIS-137 AM	DA 29	AM 100-6
Am27S280/281 Am27PS281		16 37	–	IM 1024 x 8-24-27S280/281-AMD	–	DIS-214 AM	DA 60	–
Am27S184/185 Am27LS184/185 Am27PS185	715-1616	16 06	PA 18-8 and 2048 x 4(L)	IM 2048 x 4-18-AMD	SA 4-4 B 2048 x 4/18	DIS-211 AM	DA 23	AM 140-3
Am27S190/191 Am27PS191	715-1688-1	16 68	PA 24-17 and 2048 x 8(L)	IM 2048 x 8-24-AMD	SA 22-10 B 2048 x 8/24	DIS-151 AM	DA 61	AM 100-5
Am27S290/291 Am27PS291	715-1688-2	16 68	PA 24-28 and 2048 x 8(L)	IM 2048 x 8-24-27S290/291-AMD	SA 29 B 2048 x 8/24	DIS-215 AM	DA 62	AM 190-7
Am27S40/41 Am27PS41	715-1282	–	PA 20-9 and 4096 x 4(L)	IM 4096 x 4-20-AMD	SA 30 B 4096 x 4/20	DIS-216 AM	DA 63	AM 120-6
Am27S45 Am27S47	715-1660	–	–	IM 2048 x 8-24-27S45/47-AMD	SA 31 B 2048 x 8/24	–	DA 64	AM 170-3
Am27S43	715-1698-002	–	–	IM 4096 x 8-24-AMD	–	–	–	–

Bipolar Random Access Memories (RAM) Index

Am27S02A • Am27S03A
Am27S02 • Am27S03

Schottky 64-Bit Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit Low-power Schottky RAMs
- Ultra-Fast "A" Version: Address access time 25ns
- Standard Version: Address access time 35ns
- Low Power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with open collector outputs (Am27S02/02A) or with three-state outputs (Am27S03/03A)
- Pin compatible replacements for 3101A, 74S289, 93403, 6560 (use Am27S02A/02); for 74S189, 6561, DM8599 (use Am27S03A/03)
- 100% reliability assurance testing in compliance with MIL-STD-883
- Guaranteed to INT-STD-123

FUNCTIONAL DESCRIPTION

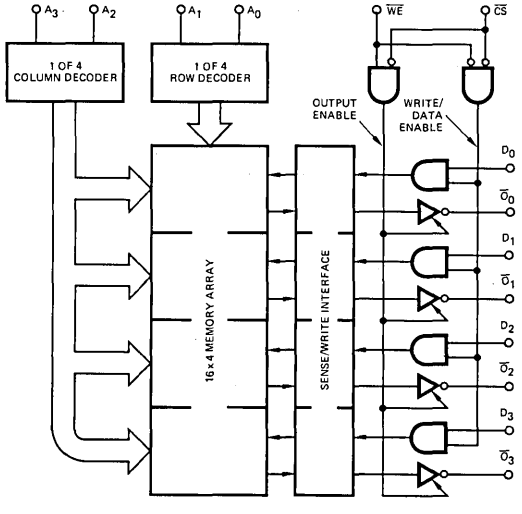
The Am27S02/02A and Am27S03/03A are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am27S02/02A) or three-state outputs (Am27S03/03A). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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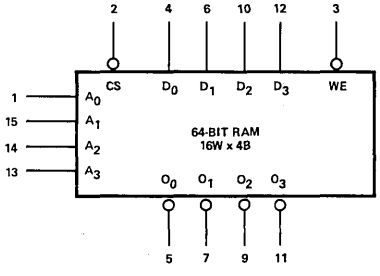
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

FUNCTION TABLE

Input		Function	Data Output Status
$\overline{CS}$	$\overline{WE}$		$\overline{O}_0-\overline{O}_3$
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word (Inverted)
High	Don't Care	Deselect	Output Disabled

DC CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA			0.350	0.45	Volts
			I_{OL} = 20mA			0.380	0.5	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Input (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3			−0.015	−0.25	mA
			$\overline{CS}$			−0.030	−0.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V				0.0	10	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)			−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX		COM'L		75	100	mA
				MIL		75	105	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4V		Am27S02A/03A Am27S02/03		0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.4V, V_{CC} = MAX		(Note 2)	−40	0		μA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

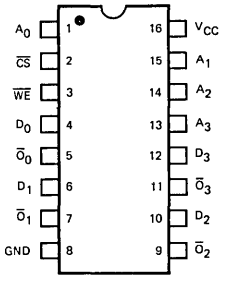
Test Conditions: See Figures 3 and 4 and Notes 3, 4, and 5

Parameters	Description		Am27S02A • Am27S03A					Am27S02 • Am27S03					Units
			Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	15		25		30	22		35		50	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2	10		15		20	14		17		25	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1	12		20		25	19		35		40	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 1	−6.0	0		0		−6.0	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1	−2.5	0		0		−2.5	0		0		ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 1	9.0	20		25		18	25		25		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1	−4.0	0		0		−4.0	0		0		ns
$t_{pw}(\overline{WE})$	MIN Write Enable Pulse Width to Insure Write	See Fig. 1	10	20		25		18	25		25		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2	10		15		20	13		17		25	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1	12		20		25	15		25		35	ns

Notes:
1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
3. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30pF$ with both input and output timing referenced to 1.5V.
4. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$ $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30pF$; and with both the input and output timing referenced to 1.5V.
5. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, $C_L = 30pF$ and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, $C_L = 30pF$ and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq 5pF$ and are measured between the 1.5V level on the input to the $V_{OH} - 500mV$ level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq 5pF$ and are measured between the 1.5V level on the input and the $V_{OL} + 500mV$ level on the output.

CONNECTION DIAGRAMS
Top Views

DIP



Note: Pin 1 is marked for orientation.

Chip-Pak™

BPM-240

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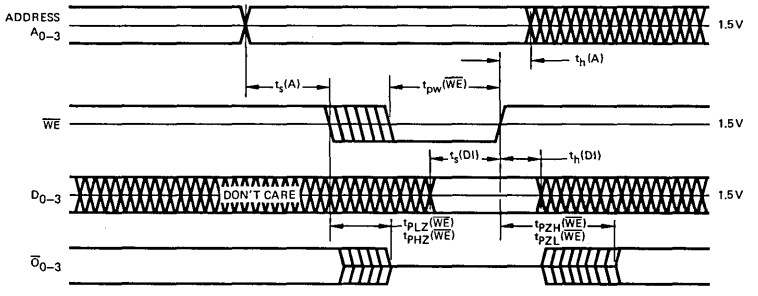
SWITCHING WAVEFORMS

WRITE MODE



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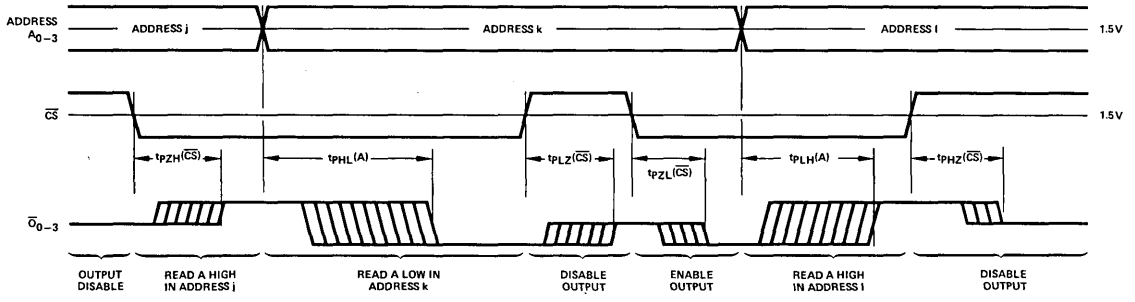
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S03A/03) while the write enable is ($\overline{WE}$) LOW.

Figure 1

READ MODE



Switching delays from address and chip select inputs to the data output. For the Am27S03A/03 disabled output is "OFF", represented by a single center line. For the Am27S02A/02, a disabled output is HIGH.

Figure 2

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AC TEST LOAD AND WAVEFORM

AC TEST LOAD

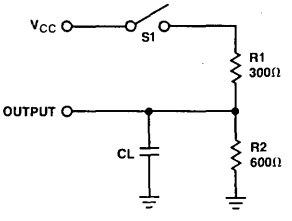

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Figure 3

INPUT PULSES

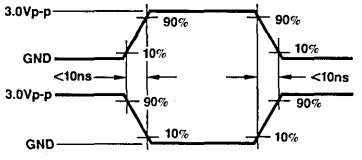


Figure 4

BPM-055

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: 3-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
25ns	AM27S02APC	AM27S03APC	P-16-1	C-1	COM'L
	AM27S02APCB	AM27S03APCB	P-16-1	B-1	
	AM27S02ADC	AM27S03ADC	D-16-1	C-1	
	AM27S02ADCB	AM27S03ADCB	D-16-1	B-1	
	AM27S02ALC	AM27S03ALC	Consult Factory	C-1	
	AM27S02ALCB	AM27S03ALCB	Consult Factory	B-1	
30ns	AM27S02ADM	AM27S03ADM	D-16-1	C-3	MIL
	AM27S02ADMB	AM27S03ADMB	D-16-1	B-3	
	AM27S02AFM	AM27S03AFM	F-16-1	C-3	
	AM27S02AFMB	AM27S03AFMB	F-16-1	B-3	
	AM27S02ALM	AM27S03ALM	Consult Factory	C-3	
	AM27S02ALMB	AM27S03ALMB	Consult Factory	B-3	
35ns	AM27S02PC	AM27S03PC	P-16-1	C-1	COM'L
	AM27S02PCB	AM27S03PCB	P-16-1	B-1	
	AM27S02DC	AM27S03DC	D-16-1	C-1	
	AM27S02DCB	AM27S03DCB	D-16-1	B-1	
	AM27S02LC	AM27S03LC	Consult Factory	C-1	
	AM27S02LCB	AM27S03LCB	Consult Factory	B-1	
50ns	AM27S02DM	AM27S03DM	D-16-1	C-3	MIL
	AM27S02DMB	AM27S03DMB	D-16-1	B-3	
	AM27S02FM	AM27S03FM	F-16-1	C-3	
	AM27S02FMB	AM27S03FMB	F-16-1	B-3	
	AM27S02LM	AM27S03LM	Consult Factory	C-3	
	AM27S02LMB	AM27S03LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See operating range table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am29702 • Am29703

Schottky 64-Bit RAM

Refer to

Am27S02 • Am27S03

Bipolar Memory RAM Product Specification

The Am29702 is replaced by the Am27S02 (open collector).

The Am29703 is replaced by the Am27S03 (three-state).

Am27LS02 • Am27LS03

Low-Power Schottky 64-Bit Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit Low-power Schottky RAMs
- Ultra-low power: I_{CC} typically 30mA
- High speed: Address access time typically 40ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (Am27LS03) or with open collector outputs (Am27LS02)
- Pin compatible replacements for DM74L89A, DM74LS289, L6560, 7489 (use Am27LS02), for DM86L99, DM74LS189, (use Am27LS03).
- 100% MIL-STD-883C assurance testing
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Guaranteed to INT-STD-123

FUNCTIONAL DESCRIPTION

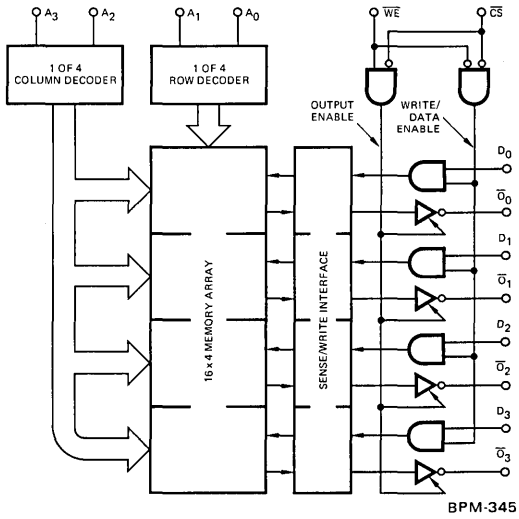
The Am27LS02 and Am27LS03 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications where power is at a premium. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am27LS02) or three-state outputs (Am27LS03). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74LS138.

An active LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW, the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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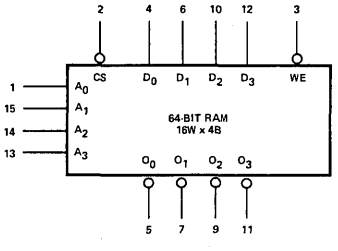
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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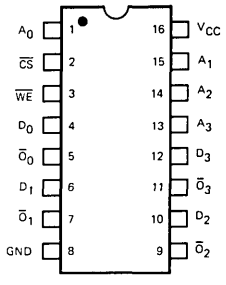
CONNECTION DIAGRAMS – Top Views

DIP



Note: Pin 1 is marked for orientation.

Chip-Pak™

TO BE DETERMINED

BPM-347

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	DC Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Am27LS03 only)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	COM'L	2.4	3.6		Volts
			I_{OH} = −2.0mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.280	0.45	Volts
			I_{OL} = 10mA			0.310	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3			−0.015	−0.250	mA
			$\overline{CS}$			−0.030	−0.250	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V				0	10	μA
I_{SC} (Am27LS03 only)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V			−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX		COM'L		30	35	mA
				MIL		30	38	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4V	Am27LS02/03			0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.4V, V_{CC} = MAX	Am27LS03		−40	0		μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots and undershoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

FUNCTION TABLE

Input		Function	Data Output Status $\overline{O}_{0\text{-}3}$
$\overline{CS}$	$\overline{WE}$		
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word (Inverted)
High	Don't Care	Deselect	Output Disabled

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

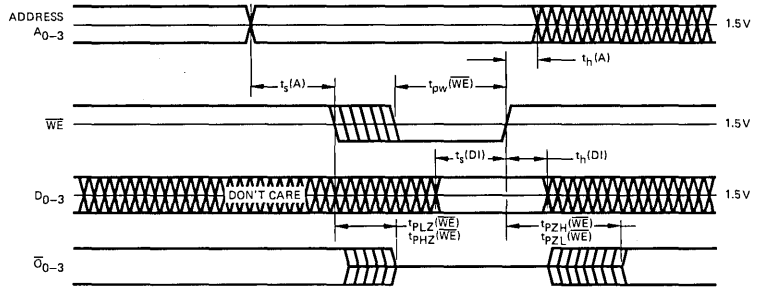
Parameters	Description		AC Test Conditions	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	Figure 3 Test Load and Figure 4 for Input Waveform Characteristics See Notes 3 and 4	40		55		65	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select to Active Output and Correct Data	See Fig. 2		18		30		35	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1		18		30		35	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 1		−17	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1		−6	0		0		ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 1		16	45		55		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1		−8	0		0		ns
$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	See Fig. 1		25	45		55		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select to Inactive Output (HI-Z)	See Fig. 2		18		30		35	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1		18		30		35	ns

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch)
3. For open collector Am27LS02, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CE}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$) are measured with S_1 closed and C_L = 30pF; and with both the input and output timing referenced to 1.5V.
4. For 3-state output Am27LS03, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the V_{OH} − 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the V_{OL} + 500mV level on the output.

SWITCHING WAVEFORMS

WRITE MODE

($\overline{CS}$ = LOW unless otherwise noted)



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
⧵⧵⧵	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
⧸⧸⧸	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
⧵⧸⧵⧸	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⧸⧵⧸⧵	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS03) while the write enable is LOW or the chip select is HIGH.

Figure 1.

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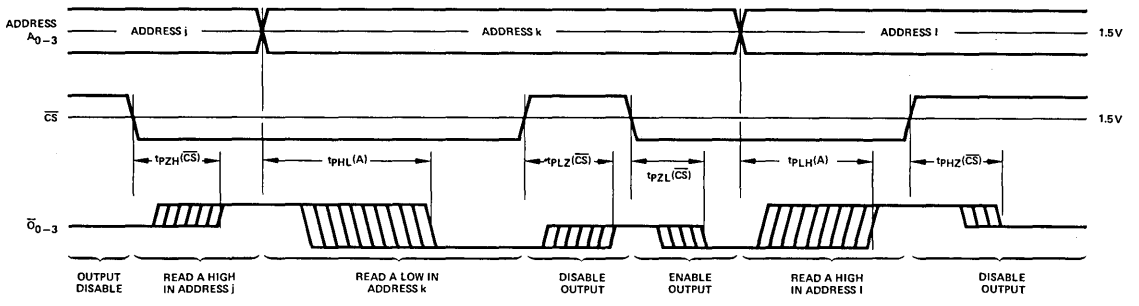
SWITCHING WAVEFORMS (Cont.)

READ MODE



Switching delays from address and chip select inputs to the data output. For the Am27LS03, disabled output is "OFF", represented by a single center line. For the Am27LS02, a disabled output is HIGH.

Figure 2.

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AC TEST LOAD AND WAVEFORM

AC TEST LOAD

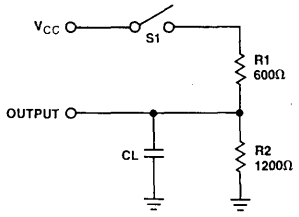

Figure 3.

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INPUT PULSES

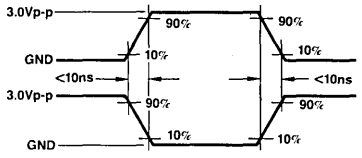

Figure 4.

See Notes 2, 3 and 4 of Switching Characteristics.

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ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
55ns	AM27LS02PC	AM27LS03PC	P-16-1	C-1	COM'L
	AM27LS02PCB	AM27LS03PCB	P-16-1	B-1	
	AM27LS02DC	AM27LS03DC	D-16-1	C-1	
	AM27LS02DCB	AM27LS03DCB	D-16-1	B-1	
	AM27LS02LC	AM27LS03LC	Consult Factory	C-1	
	AM27LS02LCB	AM27LS03LCB	Consult Factory	B-1	
65ns	AM27LS02DM	AM27LS03DM	D-16-1	C-3	MIL
	AM27LS02DMB	AM27LS03DMB	D-16-1	B-3	
	AM27LS02FM	AM27LS03FM	F-16-1	C-3	
	AM27LS02FMB	AM27LS03FMB	F-16-1	B-3	
	AM27LS02LM	AM27LS03LM	Consult Factory	C-1	
	AM27LS02LMB	AM27LS03LMB	Consult Factory	B-1	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

Am3101-1 • Am54/7489-1
Am3101 • Am54/7489

Schottky 64-Bit Write Transparent Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit Low-power write transparent Schottky RAMs
- Fast "−1" Version: Address access time 35ns
- Standard Version: Address access time 50ns
- Low Power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Available with open collector outputs
- Pin compatible replacements for 6560, 93403
- 100% reliability assurance testing in compliance with MIL-STD-883
- Guaranteed to INT-STD-123

FUNCTIONAL DESCRIPTION

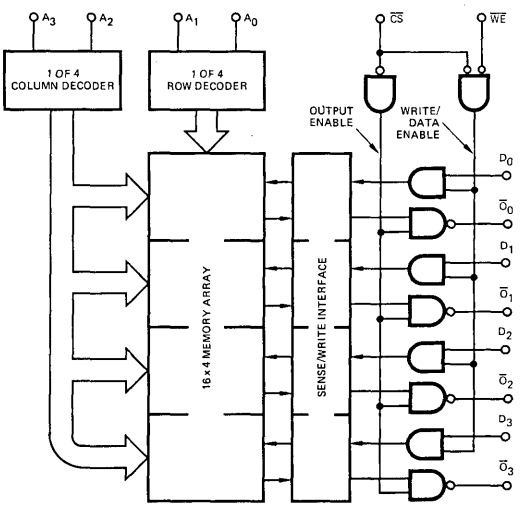
The Am3101-1/3101 and Am54/7489-1/Am54/7489 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs. Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word. During the write cycle, the outputs are active and invert the four data inputs, D_0 to D_3.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

When the chip select line is HIGH, the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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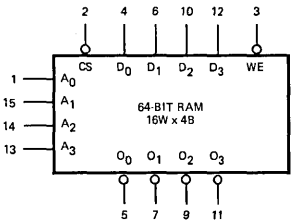
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

FUNCTION TABLE

Input		Function	Data Output Status
$\overline{CS}$	$\overline{WE}$		$\overline{O}_0-\overline{O}_3$
Low	Low	Write	D_0-D_3 (Inverted)
Low	High	Read	Selected Word (Inverted)
High	Don't Care	Deselect	Output and Write Disabled

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA		0.350	0.45	Volts
			I_{OL} = 20mA		0.380	0.5	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3		−0.015	−0.25	mA
			$\overline{CS}$		−0.030	−0.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V			0.0	10	μA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	COM'L		75	100	mA
			MIL		75	105	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA			−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH}, V_{OUT} = 2.4V, $V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}			0	40	μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

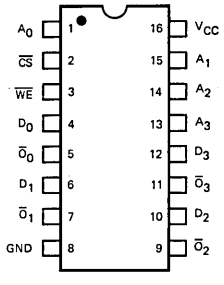
Test Conditions: See Figures 3 and 4 and Notes 3 and 4

Parameters	Description		Am3101-1 • Am54/7489-1					Am3101 • Am54/7489					Units
			Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	22		35		50	32		50		60	ns
$t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2	14		17		25	20		30		40	ns
$t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1	19		35		50	30		50		60	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 1	−6.0	0		0		−6.0	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1	−2.5	0		0		−2.5	0		0		ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 1	18	25		25		24	30		30		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1	−4.0	0		0		−4.0	0		0		ns
$t_{pw}(\overline{WE})$	MIN Write Enable Pulse Width to Insure Write	See Fig. 1	18	25		25		24	30		30		ns
$t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (Hi-Z)	See Fig. 2	13		17		25	20		30		40	ns
$t_{PLH}(DI)$ $t_{PHL}(DI)$	Delay Data Input to Correct Data Output ($\overline{WE} = \overline{CS} = V_{IL}$)	See Fig. 1	18		35		50	30		50		60	ns

Notes: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. Output is conditioned to data in (inverted) during write to insure correct data is present on all outputs during write and after write is terminated.
3. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30pF$ with both input and output timing referenced to 1.5V.
4. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30pF$; and with both the input and output timing referenced to 1.5V.

CONNECTION DIAGRAMS
Top Views

DIP



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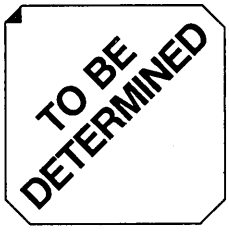
Note: Pin 1 is marked for orientation.

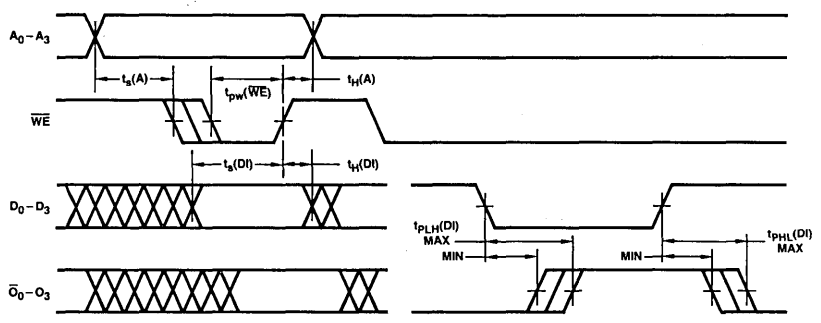
Chip-Pak™



Chip-Pak is a trademark of Advanced Micro Devices, Inc.

SWITCHING WAVEFORMS

WRITE MODE



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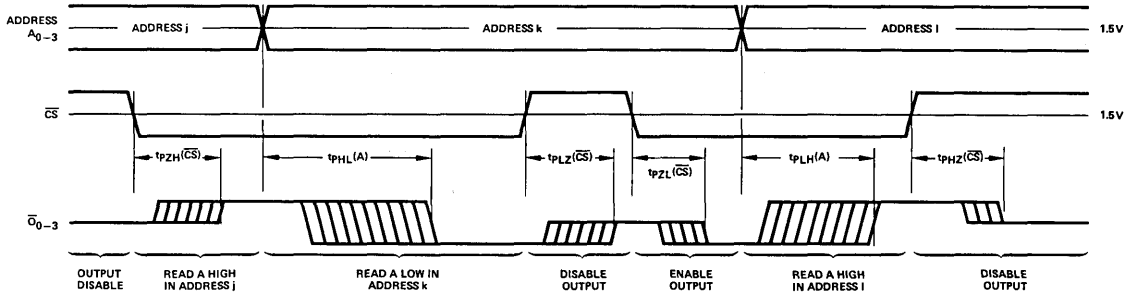
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be inactive while the write enable is ($\overline{WE}$) LOW.

Figure 1

READ MODE



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Switching delays from address and chip select inputs to the data output. A disabled output is HIGH.

Figure 2

AC TEST LOAD AND WAVEFORM

AC TEST LOAD

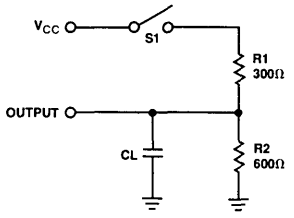

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Figure 3

INPUT PULSES

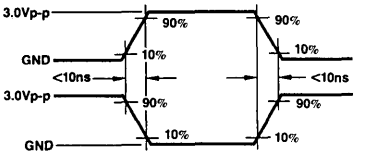

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Figure 4

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM3101-1PC	P-16-1	C-1	COM'L
	AM7489-1N	P-16-1	C-1	
	AM3101-1PCB	P-16-1	B-1	
	AM7489-1NB	P-16-1	B-1	
	AM3101-1DC	D-16-1	C-1	
	AM7489-1J	D-16-1	C-1	
	AM3101-1DCB	D-16-1	B-1	
	AM7489-1JB	D-16-1	B-1	
	AM3101-1LC	Consult Factory	C-1	
	AM7489-1LC	Consult Factory	C-1	
	AM3101-1LCB	Consult Factory	B-1	
	AM7489-1LCB	Consult Factory	B-1	
50ns	AM3101-1DM	D-16-1	C-3	MIL
	AM5489-1J	D-16-1	C-3	
	AM3101-1DMB	D-16-1	B-3	
	AM5489-1JB	D-16-1	B-3	
	AM3101-1FM	F-16-1	C-3	
	AM5489-1W	F-16-1	C-3	
	AM3101-1FMB	F-16-1	B-3	
	AM5489-1WB	F-16-1	B-3	
	AM3101-1LM	Consult Factory	C-3	
	AM5489-1LM	Consult Factory	C-3	
	AM3101-1LMB	Consult Factory	B-3	
	AM5489-1LMB	Consult Factory	B-3	
50ns	AM3101PC	P-16-1	C-1	COM'L
	AM7489N	P-16-1	C-1	
	AM3101PCB	P-16-1	B-1	
	AM7489NB	P-16-1	B-1	
	AM3101DC	D-16-1	C-1	
	AM7489J	D-16-1	C-1	
	AM3101DCB	D-16-1	B-1	
	AM7489JB	D-16-1	B-1	
	AM3101LC	Consult Factory	C-1	
	AM7489LC	Consult Factory	C-1	
	AM3101LCB	Consult Factory	B-1	
	AM7489LCB	Consult Factory	B-1	
60ns	AM3101DM	D-16-1	C-3	MIL
	AM5489J	D-16-1	C-3	
	AM3101DMB	D-16-1	B-3	
	AM5489JB	D-16-1	B-3	
	AM3101FM	F-16-1	C-3	
	Am5489W	F-16-1	C-3	
	AM3101FMB	F-16-1	B-3	
	AM5489WB	F-16-1	B-3	
	AM3101LM	Consult Factory	C-3	
	AM5489LM	Consult Factory	C-3	
	AM3101LMB	Consult Factory	B-3	
	AM5489LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am3101A • Am54S/74S289/ Am54S/74S189

Schottky 64-Bit Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit Low power Schottky RAMs
- Ultra-High speed: Address Access time 35ns
- Low Power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with open collector outputs (Am54S/74S289/Am3101A) or with three-state outputs (Am54S/74S189)
- Pin compatible replacements for Am27S02, 93403, 6560 (use Am54S/74S289/Am3101A); for Am27S03, 6561, DM8599 (use Am54S/74S189)
- 100% MIL-STD-883C assurance testing
- Guaranteed to INT-STD-123 quality levels

FUNCTIONAL DESCRIPTION

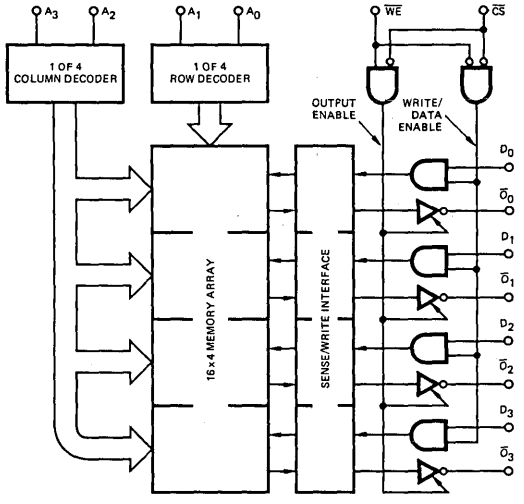
The Am3101A/Am54S/74S289 and Am54S/74S189 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am3101A/Am54S/74S289) or three-state outputs (Am54S/74S189). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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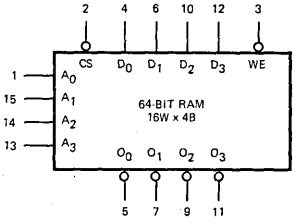
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

FUNCTION TABLE

Input		Function	Data Output Status $\overline{O}_0-\overline{O}_3$
$\overline{CS}$	$\overline{WE}$		
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word (Inverted)
High	Don't Care	Deselect	Output Disabled

3

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA			0.350	0.45	Volts
			I_{OL} = 20mA			0.380	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3			−0.015	−0.250	mA
			$\overline{CS}$			−0.030	−0.250	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V				0.0	10	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)			−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	COM'L			75	100	mA
			MIL			75	105	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4V				0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.4V, V_{CC} = MAX	(Note 2)		−40	0		μA

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

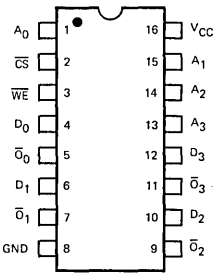
Test Conditions: See Figures 1 and 2 and Notes 3, 4, 5

Parameters	Description		Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	22		35		50	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2	14		17		25	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1	19		35		40	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 1	−6.0	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1	−2.5	0		0		ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 1	18	25		25		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1	−4.0	0		0		ns
$t_{pw}(\overline{WE})$	MIN Write Enable Pulse Width to Insure Write	See Fig. 1	18	25		25		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2	13		17		25	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1	15		25		35	ns

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
3. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and C_L = 30pF with both input and output timing referenced to 1.5V.
4. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}, $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and C_L = 30pF; and with both the input and output timing referenced to 1.5V.
5. For three-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the V_{OH} − 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the V_{OL} + 500mV level on the output.

CONNECTION DIAGRAMS
Top Views

DIP



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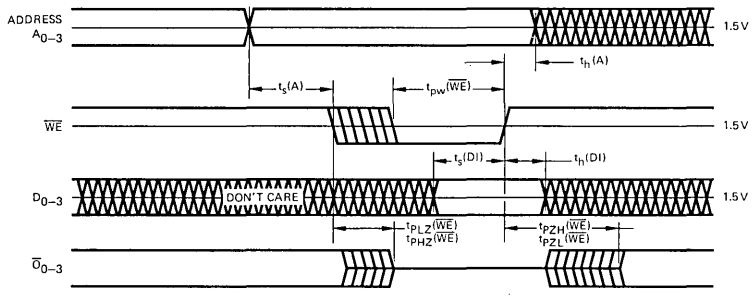
Note: Pin 1 is marked for orientation.

Chip-Pak™

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

SWITCHING WAVEFORMS

WRITE MODE



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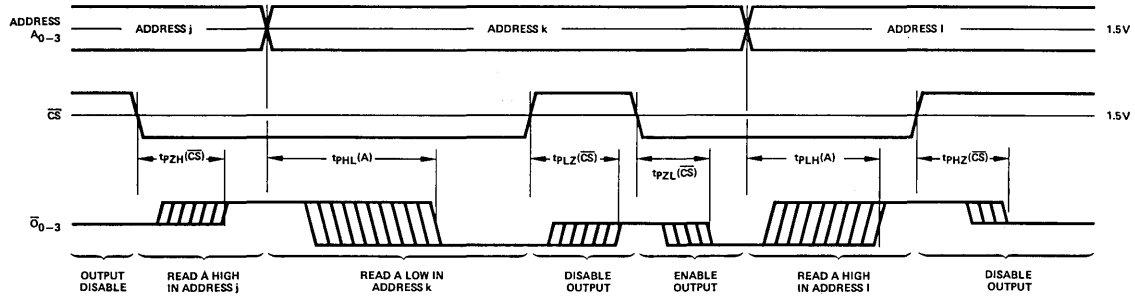
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) min must be allowed before the address may be changed again. The output will be inactive (floating for the Am54S/74S189) while the write enable is ($\overline{WE}$) LOW.

Figure 1

READ MODE



Switching delays from address and chip select inputs to the data output. For the Am54S/74S189 disabled output is "OFF", represented by a single center line. For the Am3101A/Am54S/74S289, a disabled output is HIGH.

BPM-254

Figure 2

AC TEST LOAD AND WAVEFORM

AC TEST LOAD

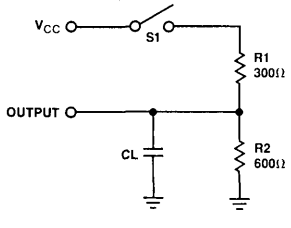


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Figure 3

INPUT PULSES

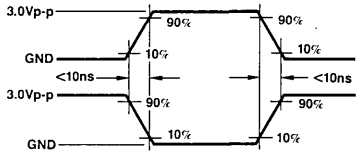

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Figure 4

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM74S289N	AM74S189N	P-16-1	C-1	COM'L
	AM3101APC		P-16-1	C-1	
	AM74S289NB	AM74S189NB	P-16-1	B-1	
	AM3101APCB		P-16-1	B-1	
	AM74S289J	AM74S189J	D-16-1	C-1	
	AM3101ADC		D-16-1	C-1	
	AM74S289JB	AM74S189JB	D-16-1	B-1	
	AM3101ADCB		D-16-1	B-1	
	AM74S289LC	AM74S189LC	Consult Factory	C-1	
	AM3101ALC		Consult Factory	C-1	
	AM74S289LCB	AM74S189LCB	Consult Factory	B-1	
	AM3101ALCB		Consult Factory	B-1	
50ns	AM54S289J	AM54S189J	D-16-1	C-3	MIL
	AM3101ADM		D-16-1	C-3	
	AM54S289JB	AM54S189JB	D-16-1	B-3	
	AM3101ADMB		D-16-1	B-3	
	AM54S289W	AM54S189W	F-16-1	C-3	
	AM3101AFM		F-16-1	C-3	
	AM54S289WB	AM54S189WB	F-16-1	B-3	
	AM3101AFMB		F-16-1	B-3	
	AM54S289LM	AM54S189LM	Consult Factory	C-3	
	AM3101ALM		Consult Factory	C-3	
	AM54S289LMB	AM54S189LMB	Consult Factory	B-3	
	AM3101ALMB		Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am31L01A • Am31L01

64-Bit Write Transparent Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16 word x 4-bit ultra low-power write transparent Schottky RAM
- High-Speed "A" version:
  Address access time typically 40ns
  Fast Standard version:
  Address access time typically 50ns
- Ultra Low Power: I_{CC} typically 30mA
- Internal ECL circuitry for optimum speed power performance over voltage and temperature
- Output reflects inverted input data during write cycle
- Electrically tested and optically inspected die are available for the assemblers of hybrid products
- 100% reliability assurance testing in compliance with MIL-STD-883
- Guaranteed to INT-STD-123

FUNCTIONAL DESCRIPTION

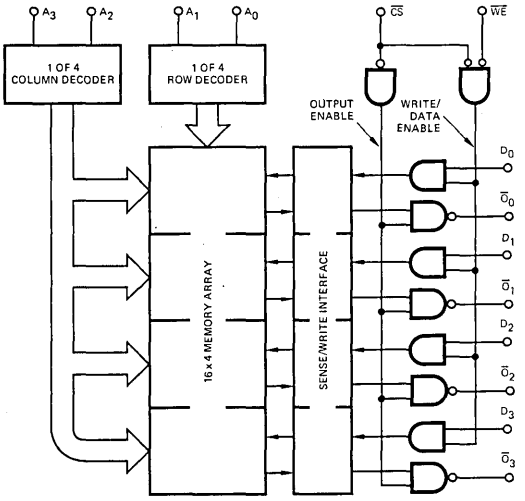
The Am31L01A and Am31L01 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs. Chip selection for large memory systems can be controlled by active LOW output decoders, such as the Am74LS138.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word. During the write cycle, the outputs are active and invert the four data inputs, D_0 to D_3.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

When the chip select line is HIGH, the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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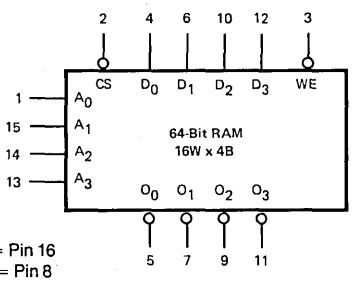
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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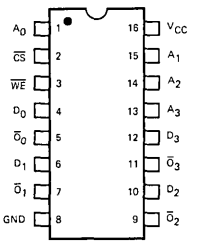
CONNECTION DIAGRAMS

Top Views

DIP



Chip-Pak™

BPM-245

Note: Pin 1 is marked for orientation.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_A = −55 to +125°C

FUNCTION TABLE

Input		Function	Data Output Status
$\overline{CS}$	$\overline{WE}$		$\overline{O_0}$-$\overline{O_3}$
Low	Low	Write	Data In (Inverted)
Low	High	Read	Selected Word (Inverted)
High	Don't Care	Deselect	Output and Write Disabled

DC CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA		0.280	0.45	Volts
			I_{OL} = 10mA		0.310	0.50	
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V			−0.030	−0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V			0.0	10	μA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	COM'L		25	35	mA
			MIL		25	38	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA			−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH}, V_{OUT} = 2.4V			0	40	μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

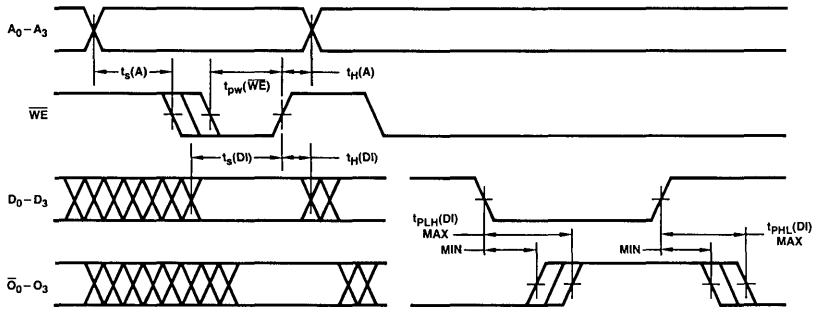
Test Conditions: See Figures 3 and 4 and Notes 3 and 4

Parameters	Description		Am31L01A Typ (Note 1)	Am31L01A COM'L Min	Am31L01A COM'L Max	Am31L01A MIL Min	Am31L01A MIL Max	Am31L01 Typ (Note 1)	Am31L01 COM'L Min	Am31L01 COM'L Max	Am31L01 MIL Min	Am31L01 MIL Max	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	40		55		65	50		80		90	ns
$t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2	18		30		35	18		60		70	ns
$t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1	18		30		35	18		80		100	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 1	−17	0		0		−17	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1	−6	0		0		−6	0		0		ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 1	16	45		55		16	60		80		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1	−8	0		0		−8	0		0		ns
$t_{pw}(\overline{WE})$	MIN Write Enable Pulse Width to Insure Write	See Fig. 1	25	45		55		25	60		80		ns
$t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HIGH-Z)	See Fig. 2	18		30		35	18		50		60	ns
$t_{PLH}(DI)$ $t_{PHL}(DI)$	Delay from Data Input to Correct Data Output ($\overline{WE} = \overline{CS} = V_{IL}$)	See Fig. 1	40		55		65	50		80		90	ns

Notes:
1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs during write and when write is terminated.
3. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30pF$ with both input and output timing referenced to 1.5V.
4. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30pF$; and with both the input and output timing referenced to 1.5V.

SWITCHING WAVEFORMS

WRITE MODE



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KEY TO TIMING DIAGRAM

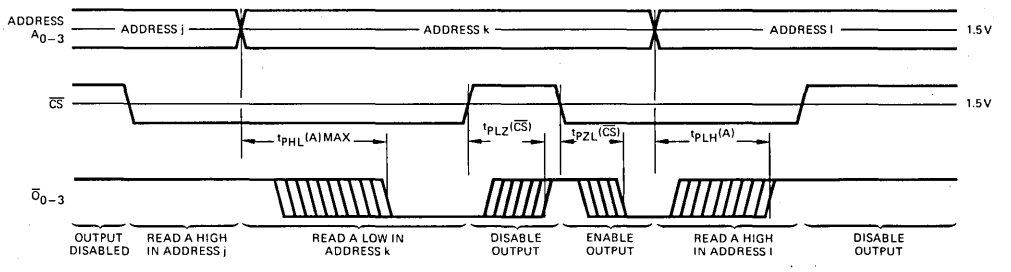
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be the complement of the Data Input while the write enable is LOW.

Figure 1.

SWITCHING WAVEFORMS (Cont.)

READ MODE



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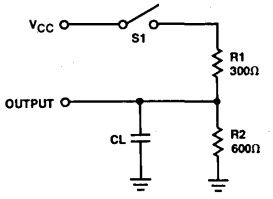
Switching delays from address and chip select inputs to the data output. For the Am31L01A and Am31L01, a disabled output is HIGH.

Figure 2.

AC TEST LOAD AND WAVEFORM

AC TEST LOAD



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INPUT PULSES

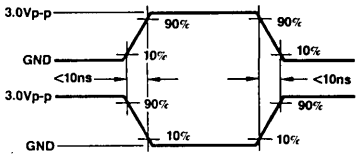

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Figure 3.

Figure 4.

See Notes 3 and 4 of Switching Characteristics.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
55ns	AM31L01APC	P-16-1	C-1	COM'L
	AM31L01APCB	P-16-1	B-1	
	AM31L01ADC	D-16-1	C-1	
	AM31L01ADCB	D-16-1	B-1	
	AM31L01ALC	Consult Factory	C-1	
	AM31L01ALCB	Consult Factory	B-1	
65ns	AM31L01ADM	D-16-1	C-3	MIL
	AM31L01ADMB	D-16-1	B-3	
	AM31L01AFM	F-16-1	C-3	
	AM31L01AFMB	F-16-1	B-3	
	AM31L01ALM	Consult Factory	C-3	
	AM31L01ALMB	Consult Factory	B-3	
80ns	AM31L01PC	P-16-1	C-1	COM'L
	AM31L01PCB	P-16-1	B-1	
	AM31L01DC	D-16-1	C-1	
	AM31L01DCB	D-16-1	B-1	
	AM31L01LC	Consult Factory	C-1	
	AM31L01LCB	Consult Factory	B-1	
90ns	AM31L01DM	D-16-1	C-3	MIL
	AM31L01DMB	D-16-1	B-3	
	AM31L01FM	F-16-1	C-3	
	AM31L01FMB	F-16-1	B-3	
	AM31L01LM	Consult Factory	C-3	
	AM31L01LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak.
Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

3

Am27S06A • Am27S07A
Am27S06 • Am27S07

Noninverting Schottky 64-Bit Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit low-power, noninverting Schottky RAMs
- Ultra-high speed "A" version:
  Address access time typically 15ns
  High speed standard version:
  Address access time typically 22ns
- Low power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am27S07A/07) or with open collector inputs (Am27S06A/06)
- 100% reliability assurance testing in compliance with MIL-STD-883
- Guaranteed to INT-STD-123 quality levels
- Electrically tested and optically inspected die are available for the assemblers of hybrid products

FUNCTIONAL DESCRIPTION

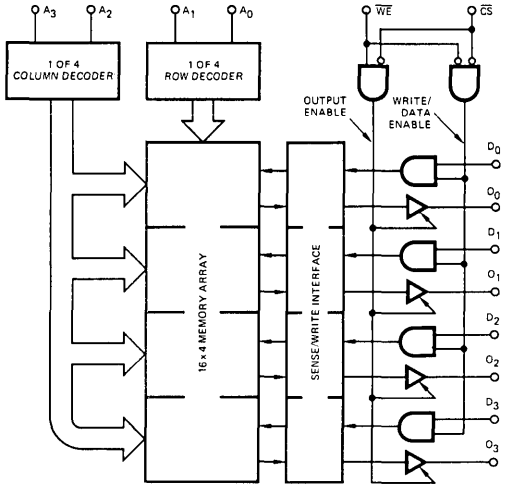
The Am27S06A/06 and Am27S07A/07 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am27S06A/06) or three-state outputs (Am27S07A/07). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four noninverting outputs O_0 to O_3.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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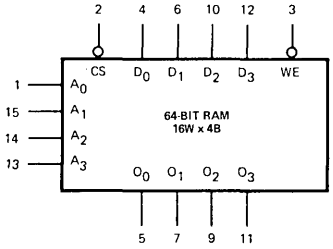
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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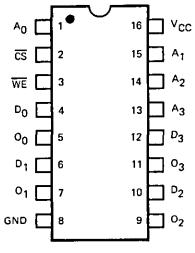
CONNECTION DIAGRAMS – Top Views

DIP



Note: Pin 1 is marked for orientation.

Chip-Pak™

BPM-354

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA			0.350	0.45	Volts
			I_{OL} = 20mA			0.380	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3			−0.015	−0.250	mA
			$\overline{CS}$			−0.030	−0.250	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V				0.0	10	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)			−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX	COM'L			75	100	mA
			MIL			75	105	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4V				0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4V, V_{CC} = MAX	(Note 2)		−40	0		μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

FUNCTION TABLE

Input		Function	Data Output Status O_{0-3}
$\overline{CS}$	$\overline{WE}$		
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word
High	Don't Care	Deselect	Output Disabled

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Test Conditions: See Figures 3 and 4 and Notes 3, 4, 5

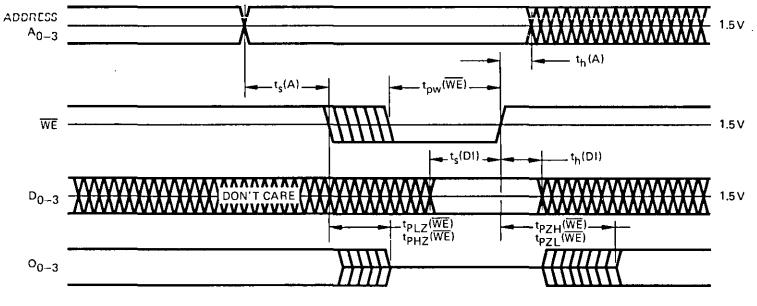
Parameters	Description		Am27S06A • Am27S07A Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Am27S06 • Am27S07 Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	15		25		30	22		35		50	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2	10		15		20	14		17		25	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1	12		20		25	19		35		40	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 1	−6.0	0		0		−6.0	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1	−2.5	0		0		−2.5	0		0		ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 1	9.0	20		25		18	25		25		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1	−4.0	0		0		−4.0	0		0		ns
$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	See Fig. 1	10	20		25		18	25		25		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (Hi-Z)	See Fig. 2	10		15		20	13		17		25	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (Hi-Z)	See Fig. 1	12		20		25	15		25		35	ns

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in (noninverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
3. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and C_L = 30pF with both input and output timing referenced to 1.5V.
4. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and C_L = 30pF and with both the input and output timing referenced to 1.5V.
5. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the V_{OH} − 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the V_{OL} + 500mV level on the output.

SWITCHING WAVEFORMS

WRITE MODE

($\overline{CS}$ = LOW unless otherwise noted)



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L-TO H
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S07A/07) while the write enable is LOW.

Figure 1.

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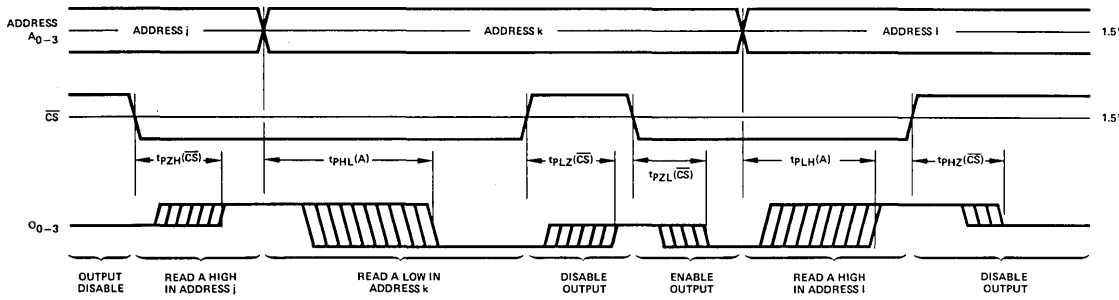
SWITCHING WAVEFORMS (Cont.)
READ MODE



Switching delays from address and chip select inputs to the data output. For the Am27S07A/07 disabled output is "OFF", represented by a single center line. For the Am27S06A/06 disabled output is HIGH.

Figure 2.

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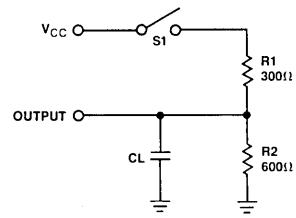
AC TEST LOAD



See Notes 3, 4, and 5 of Switching Characteristics.

Figure 3.

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INPUT PULSES

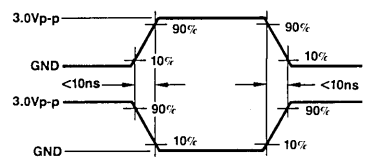

Figure 4.

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ORDERING INFORMATION

Speed Selection	Order Code		Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
	Open Collector	Three-State			
25ns	AM27S06APC	AM27S07APC	P-16-1	C-1	COM'L
	AM27S06APCB	AM27S07APCB	P-16-1	B-1	
	AM27S06ADC	AM27S07ADC	D-16-1	C-1	
	AM27S06ADCB	AM27S07ADCB	D-16-1	B-1	
	AM27S06ALC	AM27S07ALC	Consult Factory	C-1	
	AM27S06ALCB	AM27S07ALCB	Consult Factory	B-1	
30ns	AM27S06ADM	AM27S07ADM	D-16-1	C-3	MIL
	AM27S06ADMB	AM27S07ADMB	D-16-1	B-3	
	AM27S06AFM	AM27S07AFM	F-16-1	C-3	
	AM27S06AFMB	AM27S07AFMB	F-16-1	B-3	
	AM27S06ALM	AM27S07ALM	Consult Factory	C-3	
	AM27S06ALMB	AM27S07ALMB	Consult Factory	B-3	
35ns	AM27S06PC	AM27S07PC	P-16-1	C-1	COM'L
	AM27S06PCB	AM27S07PCB	P-16-1	B-1	
	AM27S06DC	AM27S07DC	D-16-1	C-1	
	AM27S06DCB	AM27S07DCB	D-16-1	B-1	
	AM27S06LC	AM27S07LC	Consult Factory	C-1	
	AM27S06LCB	AM27S07LCB	Consult Factory	B-1	
50ns	AM27S06DM	AM27S07DM	D-16-1	C-3	MIL
	AM27S06DMB	AM27S07DMB	D-16-1	B-3	
	AM27S06FM	AM27S07FM	F-16-1	C-3	
	AM27S06FMB	AM27S07FMB	F-16-1	B-3	
	AM27S06LM	AM27S07LM	Consult Factory	C-3	
	AM27S06LMB	AM27S07LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am29700 • Am29701

Noninverting Schottky 64-Bit RAM

Refer to

Am27S06 • Am27S07

Bipolar Memory RAM Product Specification

The Am29700 is replaced by the Am27S06 (open collector).

The Am29701 is replaced by the Am27S07 (three-state).

3

Am27LS06 • Am27LS07

Low Power, Noninverting 64-Bit Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit low power Schottky RAMs
- Ultra-low power: I_{CC} typically 30mA
- High-speed: Address access time typically 40ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (Am27LS07) or with open collector outputs (Am27LS06)
- 100% MIL-STD-883 assurance testing
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Guaranteed to INT-STD-123

FUNCTIONAL DESCRIPTION

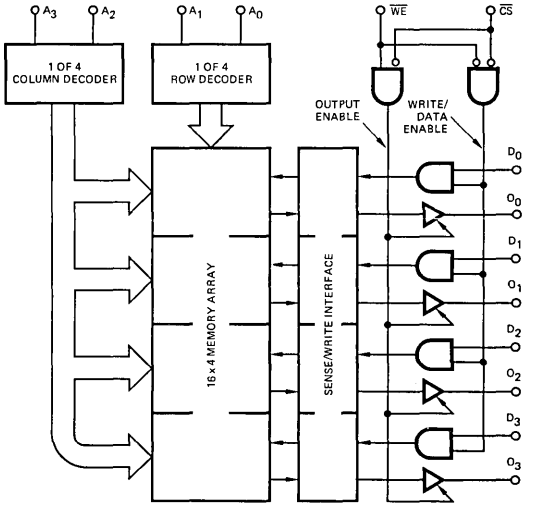
The Am27LS06 and Am27LS07 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am27LS06) or three-state outputs (Am27LS07). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74LS189.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four noninverting outputs O_0 to O_3.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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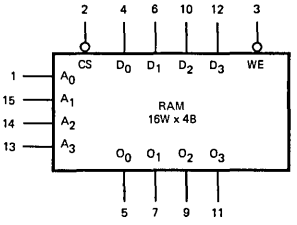
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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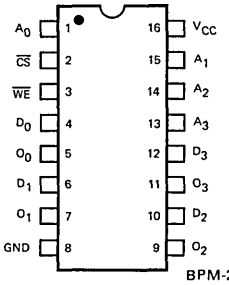
CONNECTION DIAGRAMS
Top Views

DIP



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Chip-Pak™

Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

FUNCTION TABLE

Input		Function	Data Output Status O_{0-3}
$\overline{CS}$	$\overline{WE}$		
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word (Not Inverted)
High	Don't Care	Deselect	Output Disabled

3

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	DC Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Am27LS07 only)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	COM'L	2.4	3.6		Volts
			I_{OH} = −2.0mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.280	0.45	Volts
			I_{OL} = 10mA			0.310	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3			−0.015	−0.250	mA
			$\overline{CS}$			−0.030	−0.250	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V				0	10	μA
I_{SC} (Am27LS07 only)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V			−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX		COM'L		30	35	mA
				MIL		30	38	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4V	Am27LS06/07			0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.4V, V_{CC} = MAX	Am27LS07		−40	0		μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots and undershoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

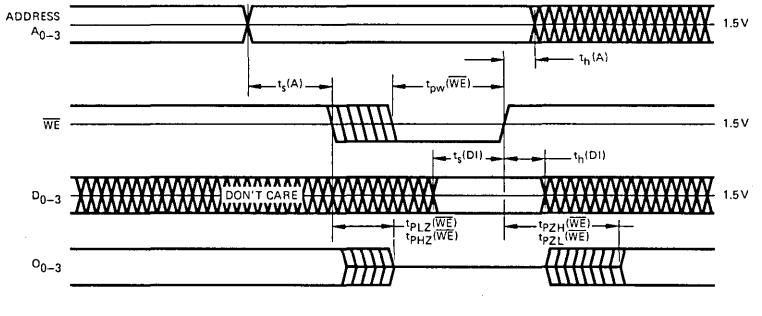
Parameters	Description		AC Test Conditions	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	Figure 3 Test Load and Figure 4 for Input Waveform Characteristics See Notes 3 and 4	40		55		65	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select to Active Output and Correct Data	See Fig. 2		18		30		35	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1		18		30		35	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 1		−17	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1		−6	0		0		ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 1		16	45		55		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1		−8	0		0		ns
$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	See Fig. 1		25	45		55		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select to Inactive Output (HI-Z)	See Fig. 2		18		30		35	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1		18		30		35	ns

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in (noninverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
3. For open collector Am27LS06, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (O_0-O_3), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and C_L = 30pF and with both the input and output timing referenced to 1.5V.
4. For 3-state output Am27LS07, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, C_L = 30pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the V_{OH} − 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the V_{OL} + 500mV level on the output.

SWITCHING WAVEFORMS

WRITE MODE

($\overline{CS}$ = LOW unless otherwise noted)



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KEY TO TIMING DIAGRAM

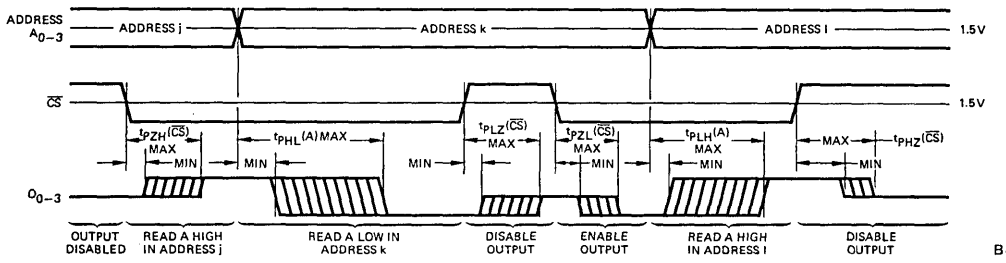
WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
⟋⟋⟋	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
⟋⟋⟋	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
⟋⟋⟋	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⟋⟋⟋	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS07) while the write enable is LOW or the chip select is HIGH.

Figure 1.

SWITCHING WAVEFORMS (Cont.)

READ MODE



Switching delays from address and chip select inputs to the data output. For the Am27LS07, disabled output is "OFF", represented by a single center line. For the Am27LS06, a disabled output is HIGH.

Figure 2.

AC TEST LOAD AND WAVEFORM

AC TEST LOAD

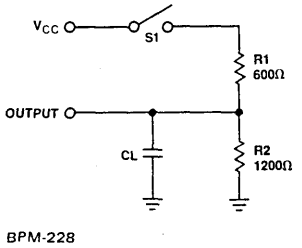


Figure 3.

INPUT PULSES

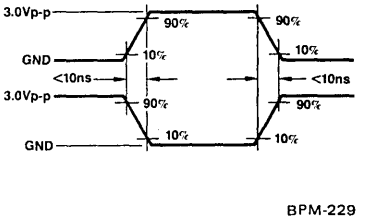


Figure 4.

See notes 2, 3 and 4 of Switching Characteristics.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
55ns	AM27LS06PC	AM27LS07PC	P-16-1	C-1	COM'L
	AM27LS06PCB	AM27LS07PCB	P-16-1	B-1	
	AM27LS06DC	AM27LS07DC	D-16-1	C-1	
	AM27LS06DCB	AM27LS07DCB	D-16-1	B-1	
	AM27LS06LC	AM27LS07LC	Consult Factory	C-1	
	AM27LS06LCB	AM27LS07LCB	Consult Factory	B-1	
65ns	AM27LS06DM	AM27LS07DM	D-16-1	C-3	MIL
	AM27LS06DMB	AM27LS07DMB	D-16-1	B-3	
	AM27LS06FM	AM27LS07FM	F-16-1	C-3	
	AM27LS06FMB	AM27LS07FMB	F-16-1	B-3	
	AM27LS06LM	AM27LS07LM	Consult Factory	C-3	
	AM27LS06LMB	AM27LS07LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

Am27LS00A • Am27LS01A
Am27LS00 • Am27LS01

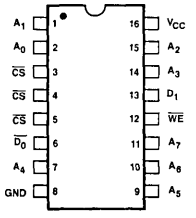
Low-Power Schottky 256-Bit Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 256-word x 1-bit low-power Schottky RAMs
- Low power dissipation:
  "A" version typically 80mA
  Standard version typically 55mA
- High-speed "A" version:
  Address access time typically 25ns
  Fast standard version:
  Address access time typically 35ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (Am27LS00A/00) or with open collector outputs (Am27LS01A/01)
- 100% MIL-STD-883C quality assurance testing
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Guaranteed to INT-STD-123

CONNECTION DIAGRAMS
Top Views

DIP



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Note: Pin 1 is marked for orientation.

Chip-Pak™

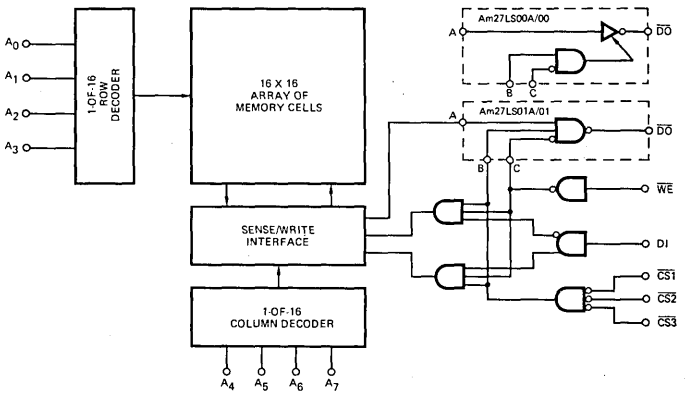
FUNCTIONAL DESCRIPTION

The Am27LS00A/00 and Am27LS01A/01 are fully decoded bipolar random access memories for use in high-speed buffer memories. The memories are organized 256-words by 1-bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am27LS00A/00) or open-collector output (Am27LS01A/01). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output floats allowing the data bus to be used by other memories or open-collector logic elements that are tied to the inverting data output. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

The chip is selected by three active LOW inputs all of which must be LOW in order for the data output to be active during the read operation and for data to be written into or read from the memory. These three active LOW chip select inputs permit MSI decoders to select memories in either a linear select, two or three dimensional mode of operation when large memory systems are being built. The delay from the chip select to the output is considerably faster than from the address inputs and extra delay can be tolerated in the chip select path without affecting system performance.

LOGIC DIAGRAM



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Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +V_{CC}
Output Current, Into Outputs	30mA
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_A = −55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

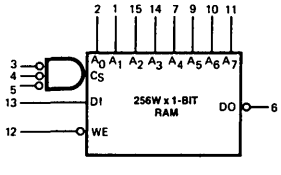
Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA			0.3	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V				0.030	0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				<1	20	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V			−20	−30	−60	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX		"A" version		80	115	mA
				Standard		55	70	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4V				0	30	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.4V, V_{CC} = MAX		(Note 2)	−30	0		μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

FUNCTION TABLE

Input			Function	Data Output Status
$\overline{CS}$	$\overline{WE}$	DI		$\overline{DO}$ (t_{n+1})
High	Don't Care	Don't Care	No Selection	Output Disabled
Low	Low	Low	Write '0'	Output Disabled
Low	Low	High	Write '1'	Output Disabled
Low	High	Don't Care	Read	Selected Bit (Inverted)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Test Conditions: See Figures 3 and 4 and Notes 3, 4 and 5

Parameters	Description		Am27LS00A • Am27LS01A					Am27LS00 • Am27LS01					Units
			Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 4	25		35		45	35		45		55	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 4	15		25		25	15		25		30	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data	See Fig. 3		5		5			5		5		ns
$t_{rec}(\overline{WE})$	Delay from Write Enable (HIGH) to Correct Output Data	See Fig. 3	25		35		45	35		45		55	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 3	0		0		5	−5		0		5	ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 3	0		0		5	−5		0		5	ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 3	25		25		30	25		30		55	ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 3	0		5		5	−5		0		5	ns
$t_{pw}(\overline{WE})$	MIN Write Enable Pulse Width to Insure Write	See Fig. 3	20	25		30		20	30		35		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 4	15		25		25	15		25		30	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 3	20		30		40	20		30		40	ns

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
3. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S closed and C_L = 50pF with both input and output timing referenced to 1.5V.
4. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed and C_L = 50pF; and with both the input and output timing referenced to 1.5V.
5. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S open, C_L = 50pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed, C_L = 50pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the V_{OH} − 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S closed and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the V_{OL} + 500mV level on the output.

AC TEST LOAD AND WAVEFORM

AC TEST LOAD

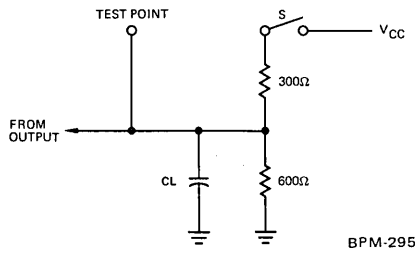


Figure 1.

INPUT PULSES

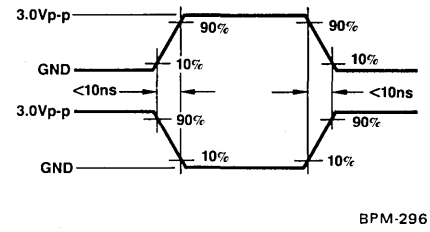
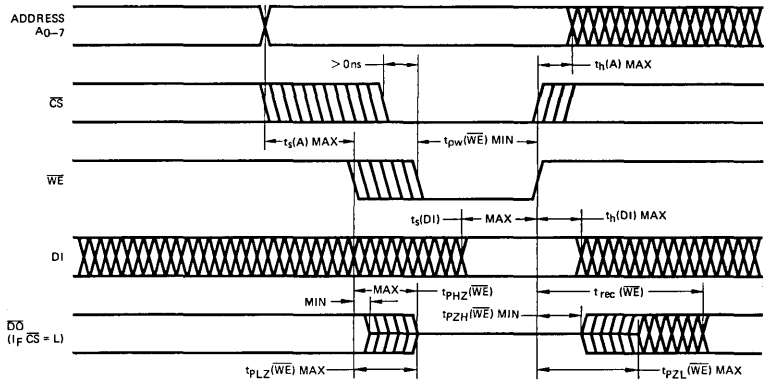


Figure 2.

See notes 3, 4 and 5 of Switching Characteristics.

SWITCHING WAVEFORMS

WRITE MODE



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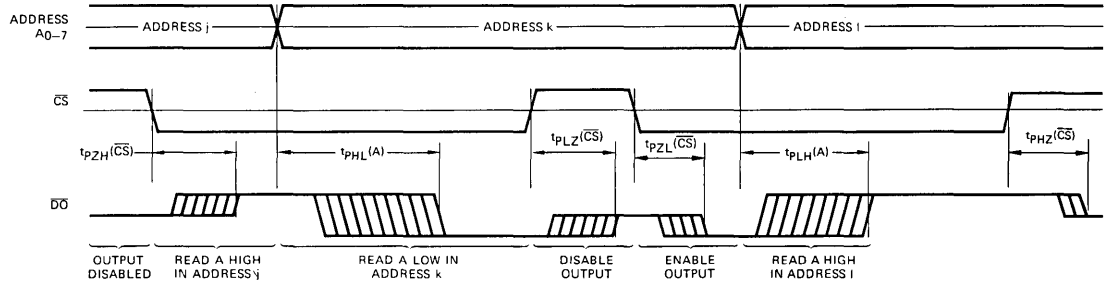
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_S(A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) max must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS00A/00) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

Figure 3.

READ MODE



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Switching delays from address and chip select inputs to the data output. For the Am27LS00A/00 disabled output is "OFF", represented by a single center line. For the Am27LS01A/01, a disabled output is HIGH.

Figure 4.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM27LS01APC	AM27LS00APC	P-16-1	C-1	COM'L
	AM27LS01APCB	AM27LS00APCB	P-16-1	B-1	
	AM27LS01ADC	AM27LS00ADC	D-16-1	C-1	
	AM27LS01ADCB	AM27LS00ADCB	D-16-1	B-1	
	AM27LS01ALC	AM27LS00ALC	Consult Factory	C-1	
	AM27LS01ALCB	AM27LS00ALCB	Consult Factory	B-1	
45ns	AM27LS01ADM	AM27LS00ADM	D-16-1	C-3	MIL
	AM27LS01ADMB	AM27LS00ADMB	D-16-1	B-3	
	AM27LS01AFM	AM27LS00AFM	F-16-1	C-3	
	AM27LS01AFMB	AM27LS00AFMB	F-16-1	B-3	
	AM27LS01ALM	AM27LS00ALM	Consult Factory	C-3	
	AM27LS01ALMB	AM27LS00ALMB	Consult Factory	B-3	
45ns	AM27LS01PC	AM27LS00PC	P-16-1	C-1	COM'L
	AM27LS01PCB	AM27LS00PCB	P-16-1	B-1	
	AM27LS01DC	AM27LS00DC	D-16-1	C-1	
	AM27LS01DCB	AM27LS00DCB	D-16-1	B-1	
	AM27LS01LC	AM27LS00LC	Consult Factory	C-1	
	AM27LS01LCB	AM27LS00LCB	Consult Factory	B-1	
55ns	AM27LS01DM	AM27LS00DM	D-16-1	C-3	MIL
	AM27LS01DMB	AM27LS00DMB	D-16-1	B-3	
	AM27LS01FM	AM27LS00FM	F-16-1	C-3	
	AM27LS01FMB	AM27LS00FMB	F-16-1	B-3	
	AM27LS01LM	AM27LS00LM	Consult Factory	C-3	
	AM27LS01LMB	AM27LS00LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am29720 • Am29721

Low-Power Schottky 256-Bit Random Access Memories

Refer to

Am27LS00 • Am27LS01

Bipolar Memory RAM Product Specification

The Am29720 is replaced by the Am27LS01 (open collector).

The Am29721 is replaced by the Am27LS00 (three-state).

3

Am27LS00-1A • Am27LS01-1A
Am27LS00-1 • Am27LS01-1

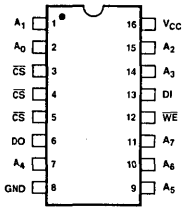
Low-Power Schottky (Noninverting) 256-Bit Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 256-word x 1-bit low-power Schottky RAMs
- Low-power dissipation:
  "A" version typically 80mA
  Standard version typically 55mA
- High-speed "A" version:
  address access time typically 25ns
  Fast standard version:
  address access time typically 35ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (Am27LS00-1A/00-1) or with open collector outputs (Am27LS01-1A/01-1)
- 100% MIL-STD-883C quality assurance testing
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Guaranteed to IND-STD-123

CONNECTION DIAGRAMS
Top Views

DIP



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Chip-Pak™

Note: Pin 1 is marked for orientation.

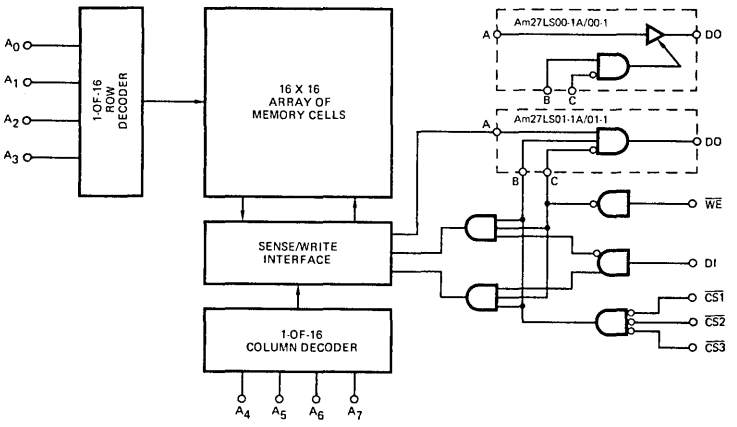
FUNCTIONAL DESCRIPTION

The Am27LS00-1A/00-1 and Am27LS01-1A/01-1 are fully decoded bipolar random access memories for use in high-speed buffer memories. The memories are organized 256-words by 1-bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am27LS00-1A/00-1) or open collector output (Am27LS01-1A/01-1). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output floats allowing the data bus to be used by other memories or open-collector logic elements that are tied to the inverting data output. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output noninverted.

The chip is selected by three active LOW inputs all of which must be LOW in order for the data output to be active during the read operation and for data to be written into or read from the memory. These three active LOW chip select inputs permit MSI decoders to select memories in either a linear select, two or three dimensional mode of operation when large memory systems are being built. The delay from the chip select to the output is considerably faster than from the address inputs and extra delay can be tolerated in the chip select path without affecting system performance.

LOGIC DIAGRAM



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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +V_{CC}
Output Current, Into Outputs	30mA
DC Input Current	−30 to +5mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	T_A = 0 to +75°C
MIL	4.5 to 5.5V	T_A = −55 to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

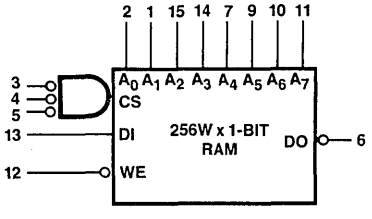
Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	COM'L	2.4	3.2		Volts
			I_{OH} = −2.0mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA			0.310	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 3)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 3)					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V				0.030	0.25	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				<1	20	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V			−20	−30	−60	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX		"A" version		80	115	mA
				Standard		55	70	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4V				0	30	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.4V, V_{CC} = MAX		(Note 2)	−30	0		μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

FUNCTION TABLE

Input $\overline{CS}$	Input $\overline{WE}$	Input DI	Function	Data Output Status DO
High	Don't Care	Don't Care	No Selection	Output Disabled
Low	Low	Low	Write "0"	Output Disabled
Low	Low	High	Write "1"	Output Disabled
Low	High	Don't Care	Read	Selected Word

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Test Conditions: See Figures 3 and 4 and Notes 3, 4 and 5

Parameters	Description		Am27LS00-1A • Am27LS01-1A					Am27LS00-1 • Am27LS01-1					Units
			Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 4	25		35		45	35		45		55	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 4	15		25		25	15		25		30	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data	See Fig. 3		5		5			5		5		ns
$t_{rec}(\overline{WE})$	Delay from Write Enable (HIGH) to Correct Output Data	See Fig. 3	25		35		45	35		45		55	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 3	0		0		5	−5		0		5	ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 3	0		0		5	−5		0		5	ns
$t_s(DI)$	Setup Time Data Input (Prior to Termination of Write)	See Fig. 3	25		25		30	25		30		55	ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 3	0		5		5	−5		0		5	ns
$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	See Fig. 3	20	25		30		20	30		35		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 4	15		25		25	15		25		30	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 3	20		30		40	20		30		40	ns

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
3. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S closed and C_L = 50pF with both input and output timing referenced to 1.5V.
4. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$ $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed and C_L = 50pF and with both the input and output timing referenced to 1.5V.
5. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S open, C_L = 50pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed, C_L = 50pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the V_{OH} − 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S closed and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the V_{OL} + 500mV level on the output.

AC TEST LOAD AND WAVEFORM

AC TEST LOAD

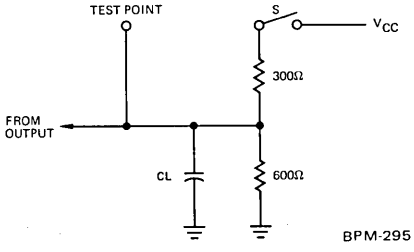


Figure 1.

INPUT PULSES

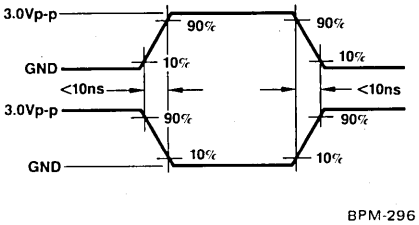
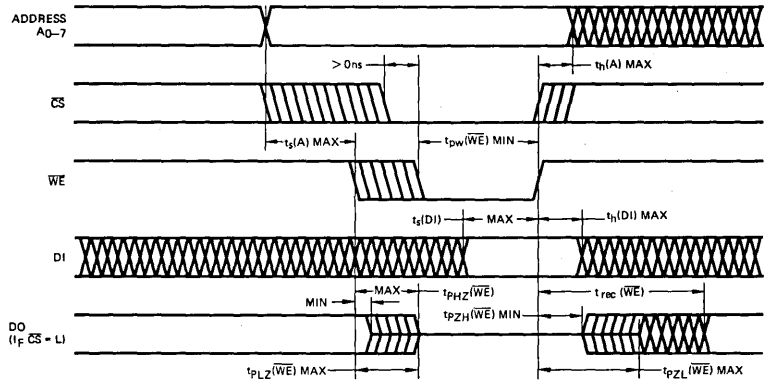


Figure 2.

See Notes 3, 4 and 5 of Switching Characteristics.

SWITCHING WAVEFORMS

WRITE MODE



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KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) max must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS00-1A/00-1) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

Figure 3.

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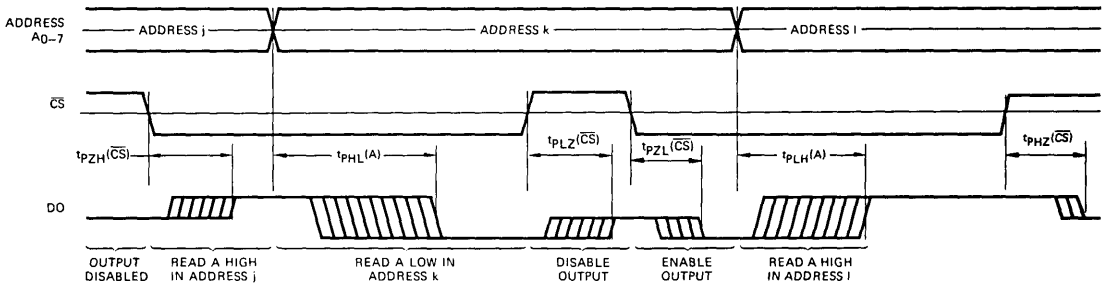
READ MODE



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Switching delays from address and chip select inputs to the data output. For the Am27LS00-1A/00-1 disabled output is "OFF," represented by a single center line. For the Am27LS01-1A/01-1, a disabled output is HIGH.

Figure 4.

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ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM27LS01-1APC	AM27LS00-1APC	P-16-1	C-1	COM'L
	AM27LS01-1APCB	AM27LS00-1APCB	P-16-1	B-1	
	AM27LS01-1ADC	AM27LS00-1ADC	D-16-1	C-1	
	AM27LS01-1ADCB	AM27LS00-1ADCB	D-16-1	B-1	
	AM27LS01-1ALC	AM27LS00-1ALC	Consult Factory	C-1	
	AM27LS01-1ALCB	AM27LS00-1ALCB	Consult Factory	B-1	
45ns	AM27LS01-1ADM	AM27LS00-1ADM	D-16-1	C-3	MIL
	AM27LS01-1ADMB	AM27LS00-1ADMB	D-16-1	B-3	
	AM27LS01-1AFM	AM27LS00-1AFM	F-16-1	C-3	
	AM27LS01-1AFMB	AM27LS00-1AFMB	F-16-1	B-3	
	AM27LS01-1ALM	AM27LS00-1ALM	Consult Factory	C-3	
	AM27LS01-1ALMB	AM27LS00-1ALMB	Consult Factory	B-3	
45ns	AM27LS01-1PC	AM27LS00-1PC	P-16-1	C-1	COM'L
	AM27LS01-1PCB	AM27LS00-1PCB	P-16-1	B-1	
	AM27LS01-1DC	AM27LS00-1DC	D-16-1	C-1	
	AM27LS01-1DCB	AM27LS00-1DCB	D-16-1	B-1	
	AM27LS01-1LC	AM27LS00-1LC	Consult Factory	C-1	
	AM27LS01-1LCB	AM27LS00-1LCB	Consult Factory	B-1	
55ns	AM27LS01-1DM	AM27LS00-1DM	D-16-1	C-3	MIL
	AM27LS01-1DMB	AM27LS00-1DMB	D-16-1	B-3	
	AM27LS01-1FM	AM27LS00-1FM	F-16-1	C-3	
	AM27LS01-1FMB	AM27LS00-1FMB	F-16-1	B-3	
	AM27LS01-1LM	AM27LS00-1LM	Consult Factory	C-3	
	AM27LS01-1LMB	AM27LS00-1LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Am93412A • Am93422A
Am93412 • Am93422

TTL 1024-Bit Bipolar IMOX™ RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 256-word x 4-bit RAMs
- High-speed "A" version:
  Address access time typically 25ns
  High-Speed Standard version:
  Address access time typically 30ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with 3-state outputs (Am93422A/422) or with open collector outputs (Am93412A/412)
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Plug-in replacement for Fairchild 93412/412A and 93422/422A
- Power dissipation decreases with increasing temperature
- Guaranteed to INT-STD-123 quality levels

FUNCTIONAL DESCRIPTION

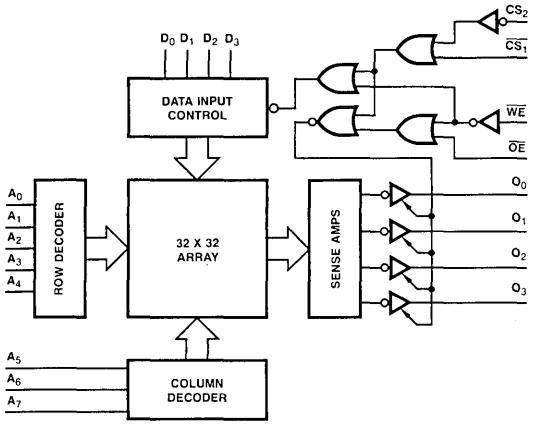
The Am93412A/412 and Am93422A/422 are 1024-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in high-speed control and buffer memory applications. Each memory is organized as a fully decoded 256-word memory of four bits per word. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) and an active HIGH chip select two (CS_2) as well as open collector OR tieable outputs (Am93412A/412) or 3-state outputs (Am93422A/422).

An active LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS}_1$) and write line ($\overline{WE}$) are LOW and chip select two (CS_2) is HIGH, the information on data inputs (D_0 through D_3) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS}_1$) LOW and the chip select two (CS_2) HIGH and the write line ($\overline{WE}$) HIGH and with the output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the noninverting outputs (O_0 through O_3).

The outputs of the memory go to an inactive high-impedance state whenever chip select one ($\overline{CS}_1$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

LOGIC BLOCK DIAGRAM



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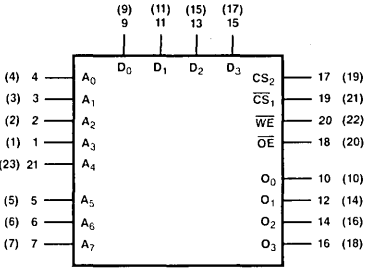
LOGIC SYMBOL



V_{CC} = Pin 22 (24)
GND = Pin 8 (8)

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Note: Pin numbers in parentheses "( )" indicate pinout for 24-pin flat package.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 8)	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs (Low)	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

FUNCTION TABLE

Inputs					Output	Mode
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	
L	X	X	X	X	*HIGH Z	Not Select
X	H	X	X	X	*HIGH Z	Not Select
H	L	H	H	X	*HIGH Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	*HIGH Z	Write "0"
H	L	L	X	H	*HIGH Z	Write "1"

H = High Voltage Level L = Low Voltage Level X = Don't Care

*High Z implies outputs are disabled or off. This condition is defined as a high impedance state for the Am93422A/422 and as an output high level for the Am93412A/412.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA		0.350	0.45	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs		2.1	1.6		Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs			1.5	0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V			−100	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 4.5V			1	40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)				−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	$T_A \geq 75°C$		100	130	mA
			T_A = 0°C			155	
			T_A = −55°C			170	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −10mA			−0.850	−1.5	Volts
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4V	Am93422A/422		0	50	μA
		V_{OUT} = 0.5V, V_{CC} = MAX	Am93422A/422	−50	0		
		V_{OUT} = 4.5V	Am93412A/412		0	100	
C_{IN}	Input Pin Capacitance	See Note 5			4		pF
C_{OUT}	Output Pin Capacitance	See Note 5			7		pF

Notes:
1. Typical characteristics are at V_{CC} = 5.0V and T_A = 25°C.
2. Applies only to the Am93422A and Am93422 with 3-state outputs.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Input and output capacitance measured on a sample basis @ f = 1.0MHz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

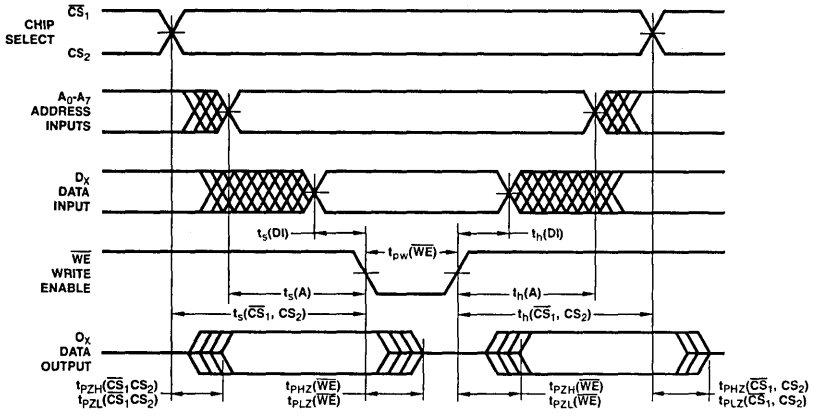
Test Conditions: See Figures 3 and 4 and Notes 3, 4 and 5 (below)

Parameters	Description	Am93412A • Am93422A					Am93412 • Am93422					Units
		Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	
t_{PLH}(A) (Note 3) t_{PHL}(A) (Note 3)	Delay from Address to Output (Address Access Time) (See Fig. 2)	25		35		45	30		45		60	ns
$t_{PZH}(\overline{CS_1}, CS_2)$ $t_{PZL}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Active Output and Correct Data (See Fig. 2)	15		25		35	15		30		45	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery) (See Fig. 1)	15		25		40	15		40		50	ns
$t_{PZH}(\overline{OE})$ $t_{PZL}(\overline{OE})$	Delay from Output Enable to Active Output and Correct Data (See Fig. 2)	10		25		35	10		30		45	ns
t_s(A)	Setup Time Address (Prior to Initiation of Write) (See Fig. 1)	−10	5		5		−10	10		10		ns
t_h(A)	Hold Time Address (After Termination of Write) (See Fig. 1)	−10	5		5		−10	5		5		ns
t_s(DI)	Setup Time Data Input (Prior to Initiation of Write) (See Fig. 1)	−10	5		5		−10	5		5		ns
t_h(DI)	Hold Time Data Input (After Termination of Write) (See Fig. 1)	−10	5		5		−10	5		5		ns
$t_s(\overline{CS_1}, CS_2)$	Setup Time Chip Select (Prior to Initiation of Write) (See Fig. 1)	−10	5		5		−10	5		5		ns
$t_h(\overline{CS_1}, CS_2)$	Hold Time Chip Select (After Termination of Write) (See Fig. 1)	−10	5		5		−10	5		5		ns
$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write (See Fig. 1)	15	20		35		15	30		40		ns
$t_{PHZ}(\overline{CS_1}, CS_2)$ $t_{PLZ}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Inactive Output (HIGH-Z) (See Fig. 2)	15		30		35	15		30		45	ns
$t_{PHZ}(\overline{WE})$ $t_{PLZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (HIGH-Z) (See Fig. 1)	15		30		40	15		35		45	ns
$t_{PHZ}(\overline{OE})$ $t_{PLZ}(\overline{OE})$	Delay from Output Enable to Inactive Output (HIGH-Z) (See Fig. 2)	15		30		35	15		30		45	ns

Notes:
1. Typical characteristics are at V_{CC} = 5.0V and T_A = 25°C.
2. Input and output capacitance measured on a sample basis @ f = 1.0MHz.
3. t_{PLH}(A) and t_{PHL}(A) are tested with S_1 closed and C_L = 15pF with both input and output timing referenced to 1.5V.
4. For open collector Am93412A/412, all delays from Write Enable ($\overline{WE}$) or selects ($\overline{CS_1}$, CS_2, $\overline{OE}$) inputs to the Data Output ($O_0 - O_3$) ($t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$, $t_{PLZ}(\overline{OE})$, $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}, CS_2)$ and $t_{PZL}(\overline{OE})$) are measured with S_1 closed and C_L = 15pF; and with both the input and output timing referenced to 1.5V.
5. For 3-state output Am93422A/422, $t_{PZH}(\overline{WE})$, $t_{PZH}(\overline{CS_1}, CS_2)$ and $t_{PZH}(\overline{OE})$ are measured with S_1 open, C_L = 15pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}, CS_2)$ and $t_{PZL}(\overline{OE})$ are measured with S_1 closed, C_L = 15pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$, $t_{PHZ}(\overline{CS_1}, CS_2)$ and $t_{PHZ}(\overline{OE})$ are measured with S_1 open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the V_{OH} −500mV level on the output. $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$ and $t_{PLZ}(\overline{OE})$ are measured with S_1 closed and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the V_{OL} + 500mV level on the output.

SWITCHING WAVEFORMS

WRITE MODE (WITH $\overline{OE}$ = LOW)



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L-TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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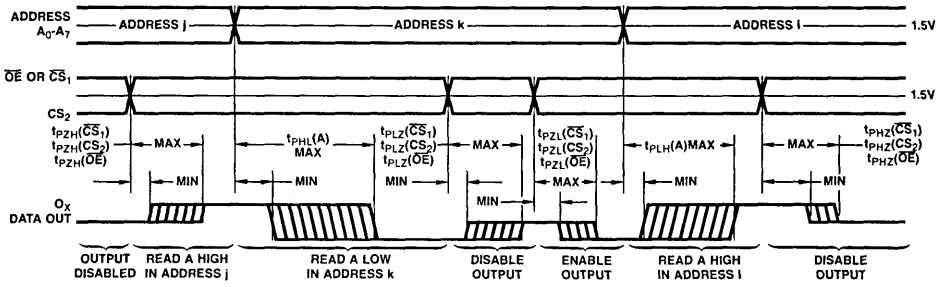
Figure 1.

READ MODE



Switching delays from address input, output enable input and the chip select inputs to the data output. For the Am93422A/422 disabled output is "OFF", represented by a single center line. For the Am93412A/412, a disabled output is HIGH.

Figure 2.

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AC TEST LOAD AND WAVEFORM

AC TEST LOAD

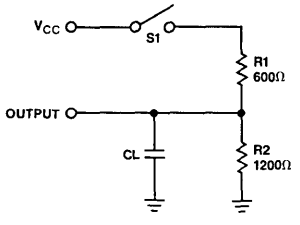

Figure 3.

INPUT PULSES

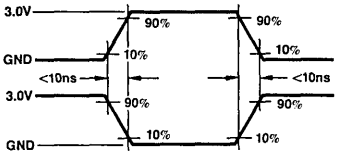

Figure 4.

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See Notes 3, 4 and 5 of Switching Characteristics.

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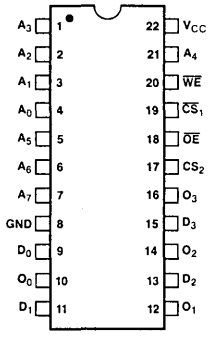
CONNECTION DIAGRAMS
Top Views

DIP



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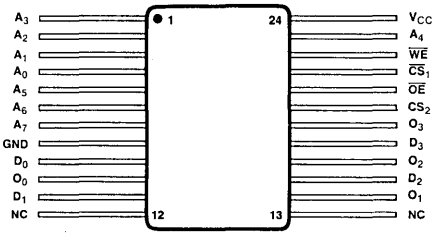
Flat Package



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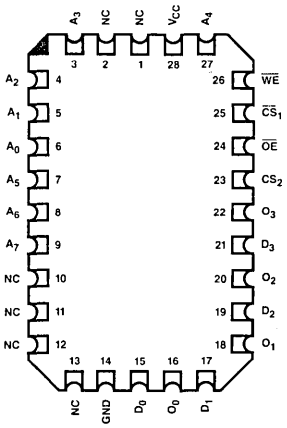
Chip-Pak™ L-28-2



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Note: Pin 1 is marked for orientation.

3

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
35ns	AM93412APC	AM93422APC	P-22-1	C-1	COM'L
	AM93412APCB	AM93422APCB	P-22-1	B-1	
	AM93412ADC	AM93422ADC	D-22-1	C-1	
	AM93412ADCB	AM93422ADCB	D-22-1	B-1	
	AM93412ALC	AM93422ALC	L-28-2	C-1	
	AM93412ALCB	AM93422ALCB	L-28-2	B-1	
45ns	AM93412ADM	AM93422ADM	D-22-1	C-3	MIL
	AM93412ADMB	AM93422ADMB	D-22-1	B-3	
	AM93412AFM	AM93422AFM	F-24-1	C-3	
	AM93412AFMB	AM93422AFMB	F-24-1	B-3	
	AM93412ALM	AM93422ALM	L-28-2	C-3	
	AM93412ALMB	AM93422ALMB	L-28-2	B-3	
45ns	AM93412PC	AM93422PC	P-22-1	C-1	COM'L
	AM93412PCB	AM93422PCB	P-22-1	B-1	
	AM93412DC	AM93422DC	D-22-1	C-1	
	AM93412DCB	AM93422DCB	D-22-1	B-1	
	AM93412LC	AM93422LC	L-28-2	C-1	
	AM93412LCB	AM93422LCB	L-28-2	B-1	
60ns	AM93412DM	AM93422DM	D-22-1	C-3	MIL
	AM93412DMB	AM93422DMB	D-22-1	B-3	
	AM93412FM	AM93422FM	F-24-1	C-3	
	AM93412FMB	AM93422FMB	F-24-1	B-3	
	AM93412LM	AM93422LM	L-28-2	C-3	
	AM93412LMB	AM93422LMB	L-28-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

Am93L412A • Am93L422A
Am93L412 • Am93L422

Low Power TTL 1024-Bit Bipolar IMOX™ RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 256-word x 4-bit RAMs
- High speed "A" version:
  Address access time typically 30ns
  Fast Standard version:
  Address access time typically 45ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with 3-state outputs (Am93L422A/L422) or with open collector outputs (Am93L412A/L412)
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Plug-in replacement for Fairchild 93L412A/L412 and 93L422A/L422
- Power dissipation decreases with increasing temperature
- Guaranteed to INT-STD-123 quality levels

FUNCTIONAL DESCRIPTION

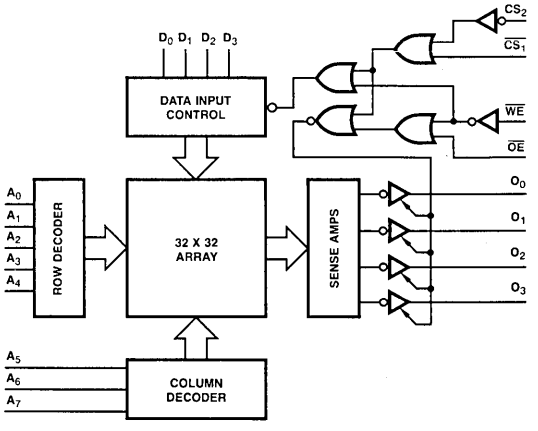
The Am93L412A/L412 and Am93L422A/L422 are 1024-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in high-speed control and buffer memory applications. Each memory is organized as a fully decoded 256-word memory of four bits per word. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) and an active HIGH chip select two (CS_2) as well as open collector OR tieable outputs (Am93L412A/L412) or 3-state outputs (Am93L422A/L422).

An active LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write line ($\overline{WE}$) are LOW and chip select two (CS_2) is HIGH, the information on data inputs (D_0 through D_3) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS_1}$) LOW and the chip select two (CS_2) HIGH and the write line ($\overline{WE}$) HIGH and with the output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the noninverting outputs (O_0 through O_3).

The outputs of the memory go to an inactive high-impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

LOGIC BLOCK DIAGRAM



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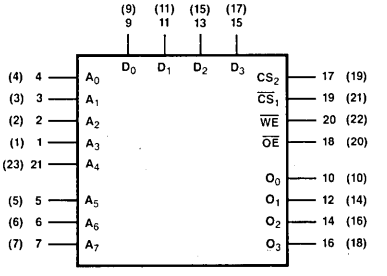
LOGIC SYMBOL



V_{CC} = Pin 22 (24)
GND = Pin 8 (8)

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Note: Pin numbers in parentheses "( )" indicate pinout for 24-pin flat package.

IMOX is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 8)	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs (Low)	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

FUNCTION TABLE

Inputs					Output	Mode
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	
L	X	X	X	X	*HIGH Z	Not Select
X	H	X	X	X	*HIGH Z	Not Select
H	L	H	H	X	*HIGH Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	*HIGH Z	Write "0"
H	L	L	X	H	*HIGH Z	Write "1"

H = High Voltage Level L = Low Voltage Level X = Don't Care

*High Z implies outputs are disabled or off. This condition is defined as a high impedance state for the Am93L422A/L422 and as an output high level for the Am93L412A/L412.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA		0.350	0.45	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs		2.1	1.6		Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs			1.5	0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V			−100	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 4.5V			1	40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 4)				−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	$T_A \geq 75°C$		55	75	mA
			T_A = 0°C			80	
			T_A = −55°C			90	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −10mA			−0.850	−1.5	Volts
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4V	Am93L422A/L422		0	50	μA
		V_{OUT} = 0.5V, V_{CC} = MAX	Am93L422A/L422	−50	0		
		V_{OUT} = 4.5V	Am93L412A/L412		0	100	
C_{IN}	Input Pin Capacitance	See Note 5			4		pF
C_{OUT}	Output Pin Capacitance	See Note 5			7		pF

Notes: 1. Typical characteristics are at V_{CC} = 5.0V and T_A = 25°C.
2. Applies only to the Am93L422A and Am93L422 with 3-state outputs.
3. *These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise.* Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Input and output capacitance measured on a sample basis @ f = 1.0MHz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

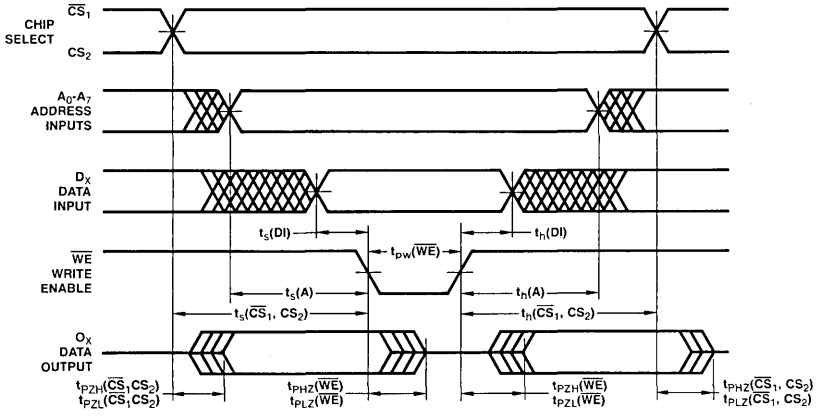
Test Conditions: See Figures 3 and 4 and Notes 3, 4 and 5 (below)

Parameters	Description	Am93L412A • Am93L422A					Am93L412 • Am93L422					Units
		Typ (Note 1)	COM'L		MIL		Typ (Note 1)	COM'L		MIL		
			Min	Max	Min	Max		Min	Max	Min	Max	
t_{PLH}(A) (Note 3) t_{PHL}(A) (Note 3)	Delay from Address to Output (Address Access Time) (See Fig. 2)	30		45		55	45		60		75	ns
$t_{PZH}(\overline{CS_1}, CS_2)$ $t_{PZL}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Active Output and Correct Data (See Fig. 2)	15		30		40	20		35		45	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery) (See Fig. 1)	25		40		45	25		45		50	ns
$t_{PZH}(\overline{OE})$ $t_{PZL}(\overline{OE})$	Delay from Output Enable to Active Output and Correct Data (See Fig. 2)	15		30		40	20		35		45	ns
t_s(A)	Setup Time Address (Prior to Initiation of Write) (See Fig. 1)	−5	5		10		−5	10		10		ns
t_h(A)	Hold Time Address (After Termination of Write) (See Fig. 1)	−5	5		5		−5	5		10		ns
t_s(DI)	Setup Time Data Input (Prior to Initiation of Write) (See Fig. 1)	−5	5		5		−5	5		5		ns
t_h(DI)	Hold Time Data Input (After Termination of Write) (See Fig. 1)	−5	5		5		−5	5		5		ns
$t_s(\overline{CS_1}, CS_2)$	Setup Time Chip Select (Prior to Initiation of Write) (See Fig. 1)	−5	5		5		−5	5		5		ns
$t_h(\overline{CS_1}, CS_2)$	Hold Time Chip Select (After Termination of Write) (See Fig. 1)	−5	5		5		−5	5		10		ns
$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write (See Fig. 1)	15	35		40		15	45		55		ns
$t_{PHZ}(\overline{CS_1}, CS_2)$ $t_{PLZ}(\overline{CS_1}, CS_2)$	Delay from Chip Select to Inactive Output (HIGH-Z) (See Fig. 2)	20		30		40	20		35		45	ns
$t_{PHZ}(\overline{WE})$ $t_{PLZ}(\overline{WE})$	Delay from Write Enable to Inactive Output (HIGH-Z) (See Fig. 1)	25		35		40	30		40		45	ns
$t_{PHZ}(\overline{OE})$ $t_{PLZ}(\overline{OE})$	Delay from Output Enable to Inactive Output (HIGH-Z) (See Fig. 2)	20		30		40	20		35		45	ns

Notes:
1. Typical characteristics are at V_{CC} = 5.0V and T_A = 25°C.
2. Input and output capacitance measured on a sample basis @ f = 1.0MHz.
3. t_{PLH}(A) and t_{PHL}(A) are tested with S_1 closed and C_L = 15pF with both input and output timing referenced to 1.5V.
4. For open collector Am93L412A/L412, all delays from Write Enable ($\overline{WE}$) or selects ($\overline{CS_1}$, CS_2, $\overline{OE}$) inputs to the Data Output ($O_0 - O_3$) ($t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$, $t_{PLZ}(\overline{OE})$, $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}, CS_2)$ and $t_{PZL}(\overline{OE})$) are measured with S_1 closed and C_L = 15pF; and with both the input and output timing referenced to 1.5V.
5. For 3-state output Am93L422A/L422, $t_{PZH}(\overline{WE})$, $t_{PZH}(\overline{CS_1}, CS_2)$ and $t_{PZH}(\overline{OE})$ are measured with S_1 open, C_L = 15pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}, CS_2)$ and $t_{PZL}(\overline{OE})$ are measured with S_1 closed, C_L = 15pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$, $t_{PHZ}(\overline{CS_1}, CS_2)$ and $t_{PHZ}(\overline{OE})$ are measured with S_1 open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the V_{OH} − 500mV level on the output. $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$ and $t_{PLZ}(\overline{OE})$ are measured with S_1 closed and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the V_{OL} + 500mV level on the output.

SWITCHING WAVEFORMS

WRITE MODE (WITH $\overline{OE}$ = LOW)



KEY TO TIMING DIAGRAM

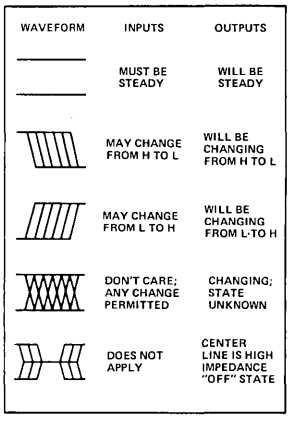


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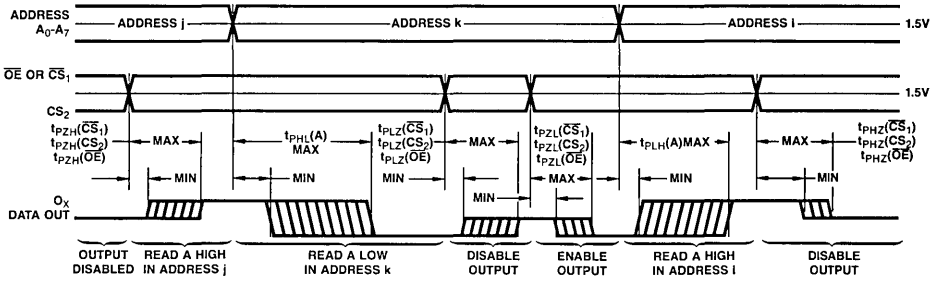
Figure 1.

3

READ MODE



Switching delays from address input, output enable input and the chip select inputs to the data output. For the Am93L422A/L422 disabled output is "OFF", represented by a single center line. For the Am93L412A/L412, a disabled output is HIGH.

Figure 2.

BPM-232

AC TEST LOAD AND WAVEFORM

AC TEST LOAD

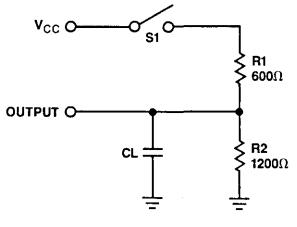


Figure 3.

INPUT PULSES

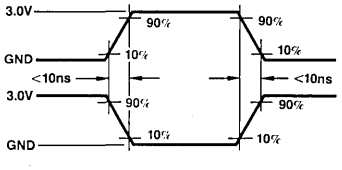


Figure 4.

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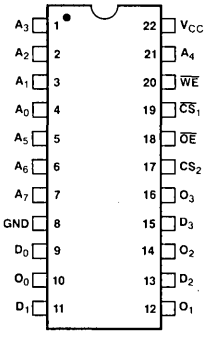
See Notes 3, 4 and 5 of Switching Characteristics.

BPM-234

CONNECTION DIAGRAMS
Top Views

DIP



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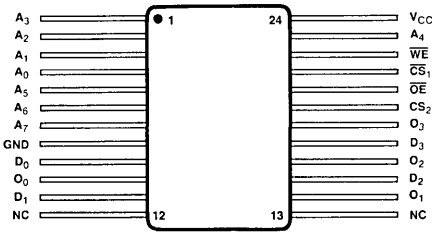
Flat Package



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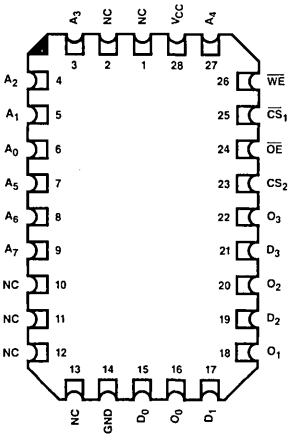

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Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
45ns	AM93L412APC	AM93L422APC	P-22-1	C-1	COM'L
	AM93L412APCB	AM93L422APCB	P-22-1	B-1	
	AM93L412ADC	AM93L422ADC	D-22-1	C-1	
	AM93L412ADCB	AM93L422ADCB	D-22-1	B-1	
	AM93L412ALC	AM93L422ALC	L-28-2	C-1	
	AM93L412ALCB	AM93L422ALCB	L-28-2	B-1	
55ns	AM93L412ADM	AM93L422ADM	D-22-1	C-3	MIL
	AM93L412ADMB	AM93L422ADMB	D-22-1	B-3	
	AM93L412AFM	AM93L422AFM	F-24-1	C-3	
	AM93L412AFMB	AM93L422AFMB	F-24-1	B-3	
	AM93L412ALM	AM93L422ALM	L-28-2	C-3	
	AM93L412ALMB	AM93L422ALMB	L-28-2	B-3	
60ns	AM93L412PC	AM93L422PC	P-22-1	C-1	COM'L
	AM93L412PCB	AM93L422PCB	P-22-1	B-1	
	AM93L412DC	AM93L422DC	D-22-1	C-1	
	AM93L412DCB	AM93L422DCB	D-22-1	B-1	
	AM93L412LC	AM93L422LC	L-28-2	C-1	
	AM93L412LCB	AM93L422LCB	L-28-2	B-1	
75ns	AM93L412DM	AM93L422DM	D-22-1	C-3	MIL
	AM93L412DMB	AM93L422DMB	D-22-1	B-3	
	AM93L412FM	AM93L422FM	F-24-1	C-3	
	AM93L412FMB	AM93L422FMB	F-24-1	B-3	
	AM93L412LM	AM93L422LM	L-28-2	C-3	
	AM93L412LMB	AM93L422LMB	L-28-2	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications. Pad layout and bonding diagram available upon request.

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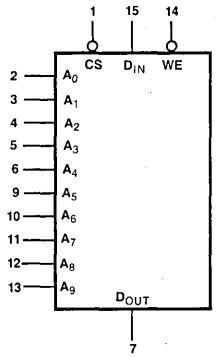
Am93415A • Am93425A
Am93415 • Am93425

TTL 1024-Bit Bipolar IMOX™ RAM

DISTINCTIVE CHARACTERISTICS

- Fully decoded 1024-word x 1-bit RAMs
- Ultra-high speed "A" version:
  Address Access time typically 22ns
  High Speed Standard version:
  Address Access time typically 30ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am93425A/425) or with open collector outputs (Am93415A/415)
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Plug in replacement for Fairchild 93415A/415 and 93425A/425
- Power dissipation decreases with increasing temperature
- Guaranteed to INT-STD-123 quality levels

LOGIC SYMBOL

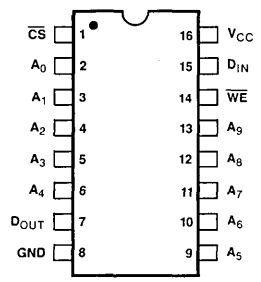


V_{CC} = Pin 16
GND = Pin 8

BPM-050

CONNECTION DIAGRAMS – Top Views

DIP



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Chip-Pak™

Note: Pin 1 is marked for orientation

FUNCTIONAL DESCRIPTION

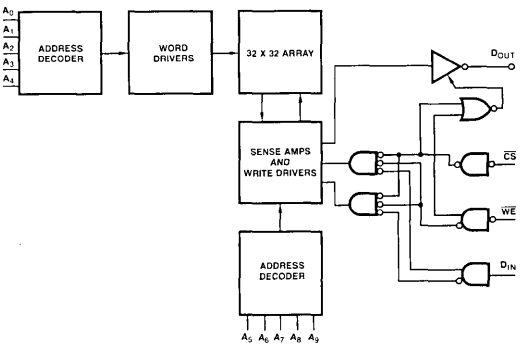
The Am93415A/415 and Am93425A/425 are 1024-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in high-speed control and buffer memory applications. Each memory is organized as a fully decoded 1024-word memory of 1 bit per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am93415A/415) or three-state outputs (Am93425A/425). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the data input (D_{IN}) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



BPM-049

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3

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5 to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
Output Current, Into Outputs (Low)	20mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
COM'L	4.75 to 5.25V	0 to +75°C
MIL	4.5 to 5.5V	−55 to +125°C

FUNCTION TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	*HIGH-Z	Not Selected
L	L	L	*HIGH-Z	Write "0"
L	L	H	*HIGH-Z	Write "1"
L	H	X	Selected Data	Read

H = High Voltage Level L = Low Voltage Level X = Don't Care

*HIGH-Z implies outputs are disabled or off. This condition is defined as a high impedance state for the Am93425A/425 and as an output high level for the Am93415A/415.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH} (Note 2)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −10.3mA	COM'L	2.4	3.6		Volts
			I_{OH} = −5.2mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA			0.350	0.45	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs			2.1	1.6		Volts
V_{IL}	Input LOW Level (Note 3)	Guaranteed input logical LOW voltage for all inputs				1.5	0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V				−180	−400	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 4.5V				1	40	μA
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V					−100	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	$T_A \geq 75°C$			95	110	mA
			T_A = 0°C				125	
			T_A = −55°C				145	
V_{CL}	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −10mA				−0.850	−1.5	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 2.4V	Am93415A/425A Am93415/425			0	100	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL}, V_{OUT} = 0.5V, V_{CC} = MAX	Am93425A Am93425		−50	0		
C_{IN}	Input Pin Capacitance	See Note 4				4		pF
C_{OUT}	Output Pin Capacitance	See Note 4				7		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. This applies only to the Am93425A/425 with three-state outputs.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Input and output capacitance measured on a sample basis using pulse technique.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

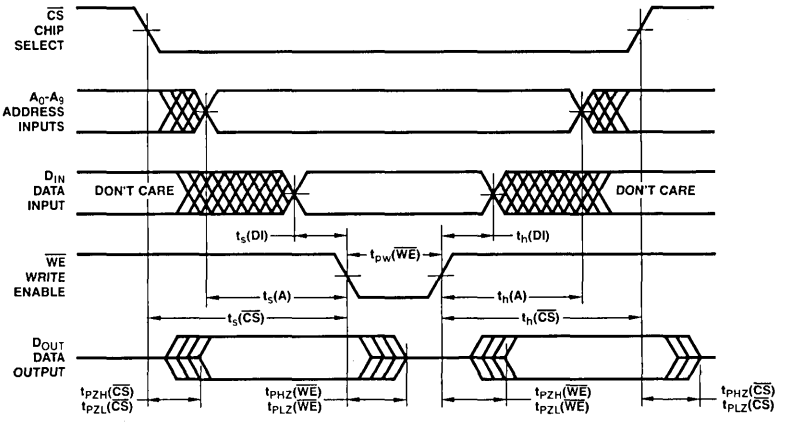
Test Conditions: See Figures 3 and 4 and Notes 2, 3, and 4 (below)

Parameters	Description		Am93415A • Am93425A					Am93415 • Am93425					Units
			Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output (Address Access Time)	See Fig. 2	22		30		40	30		45		60	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select to Active Output and Correct Data	See Fig. 2	10		20		30	15		35		45	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable to Active Output and Correct Data (Write Recovery)	See Fig. 1	10		25		35	15		40		50	ns
$t_s(A)$	Setup Time Address (Prior to Initiation of Write)	See Fig. 1	0	5		5		0	10		15		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1	0	5		5		0	5		5		ns
$t_s(DI)$	Setup Time Data Input (Prior to Initiation of Write)	See Fig. 1	0	5		5		0	5		5		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1	0	5		5		0	5		5		ns
$t_s(\overline{CS})$	Setup Time Chip Select (Prior to Initiation of Write)	See Fig. 1	0	5		5		0	5		5		ns
$t_h(\overline{CS})$	Hold Time Chip Select (After Termination of Write)	See Fig. 1	0	5		5		0	5		5		ns
$t_{pw}(\overline{WE})$	Min Write Enable Pulse Width to Insure Write	See Fig. 1	12	20		30		15	30		40		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select to Inactive Output (HIGH-Z)	See Fig. 2	10		20		30	15		35		50	ns
$t_{PHZ}(\overline{WE})$ $t_{PLZ}(\overline{WE})$	Delay from write Enable to Inactive Output (HIGH-Z)	See Fig. 1	10		20		30	15		35		35	ns

Notes:
1. Typical characteristics are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with S_1 closed and $C_L = 30pF$ with both input and output timing referenced to 1.5V.
3. For open collector Am93415A/415, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CE}$) inputs to the Data Output (D_{OUT}), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed and $C_L = 30pF$; and with both the input and output timing referenced to 1.5V.
4. For 3-state output Am93425A/425, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S_1 open, $C_L = 30pF$ and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S_1 closed, $C_L = 30pF$ and with both the input and output timing referenced to 1.5V. $t_{PZH}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S_1 open and $C_L \leq 5pF$ and are measured between the 1.5V level on the input to the $V_{OH} - 500mV$ level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with S_1 closed and $C_L \leq 5pF$ and are measured between the 1.5V level on the input and the $V_{OL} + 500mV$ level on the output.

SWITCHING WAVEFORMS

WRITE MODE



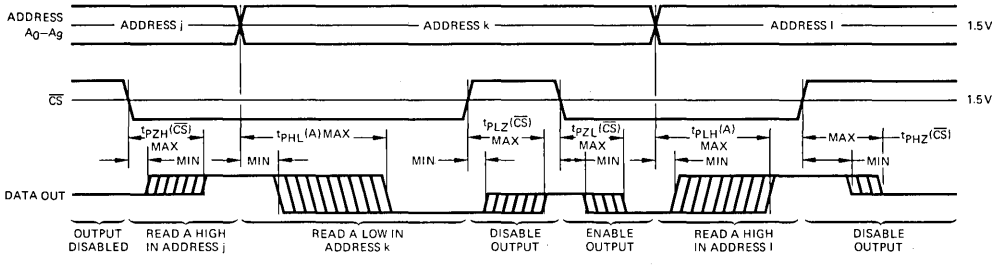
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

BPM-052

Figure 1.

READ MODE



Switching delays from address and chip select inputs to the data output. For the Am93425A/425 disabled output is "OFF", represented by a single center line. For the Am93415A/415 a disabled output is HIGH.

Figure 2.

BPM-053

AC TEST LOAD AND WAVEFORM

AC TEST LOAD

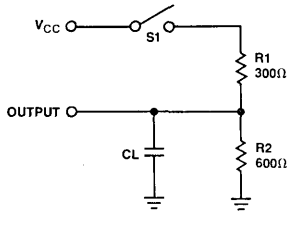


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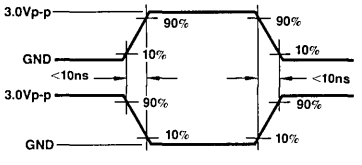
Figure 3.

INPUT PULSES



BPM-055

Figure 4.

See Notes 2, 3, and 4 of Switching Characteristics.

ORDERING INFORMATION

Speed Selection	Order Code: Open Collector	Order Code: Three-State	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
30ns	AM93415APC	AM93425APC	P-16-1	C-1	COM'L
	AM93415APCB	AM93425APCB	P-16-1	B-1	
	AM93415ADC	AM93425ADC	D-16-1	C-1	
	AM93415ADCB	AM93425ADCB	D-16-1	B-1	
	AM93415ALC	AM93425ALC	Consult Factory	C-1	
	AM93415ALCB	AM93425ALCB	Consult Factory	B-1	
40ns	AM93415ADM	AM93425ADM	D-16-1	C-3	MIL
	AM93415ADMB	AM93425ADMB	D-16-1	B-3	
	AM93415AFM	AM93425AFM	F-16-1	C-3	
	AM93415AFMB	AM93425AFMB	F-16-1	B-3	
	AM93415ALM	AM93425ALM	Consult Factory	C-3	
	AM93415ALMB	AM93425ALMB	Consult Factory	B-3	
45ns	AM93415PC	AM93425PC	P-16-1	C-1	COM'L
	AM93415PCB	AM93425PCB	P-16-1	B-1	
	AM93415DC	AM93425DC	D-16-1	C-1	
	AM93415DCB	AM93425DCB	D-16-1	B-1	
	AM93415LC	AM93425LC	Consult Factory	C-1	
	AM93415LCB	AM93425LCB	Consult Factory	B-1	
60ns	AM93415DM	AM93425DM	D-16-1	C-3	MIL
	AM93415DMB	AM93425DMB	D-16-1	B-3	
	AM93415FM	AM93425FM	F-16-1	C-3	
	AM93415FMB	AM93425FMB	F-16-1	B-3	
	AM93415LM	AM93425LM	Consult Factory	C-3	
	AM93415LMB	AM93425LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications.
Pad layout and bonding diagram available upon request.

Am10415SA • Am10415A • Am10415

ECL 1024 x 1 IMOX™ Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fast access time (10ns typ.) – improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL – no board changes required
- Internally voltage compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- 100% MIL-STD-883C screening and guaranteed to INT-STD-123 insures the highest reliability
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

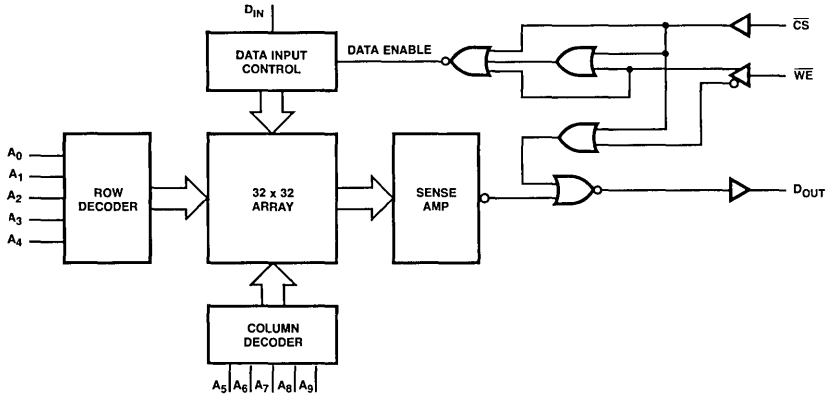
The Am10415SA, Am10415A and Am10415 are fully decoded 1024-bit ECL RAMs organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

BLOCK DIAGRAM



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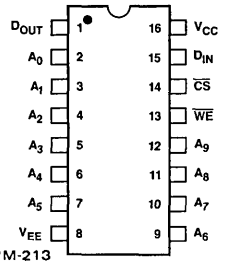
CONNECTION DIAGRAMS – Top Views

DIP



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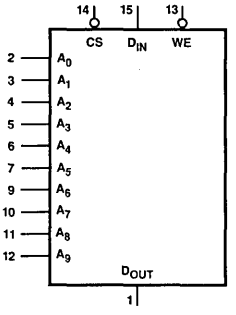
Chip-Pak™

TO BE DETERMINED

Note: Pin 1 is marked for orientation.
The flatpackage version has the same pinout as the dual in-line package.

LOGIC SYMBOL



BPM-214

V_{CC} = Pin 16
V_{EE} = Pin 8

IMOX is a trademark of Advanced Micro Devices, Inc.
Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
V_{EE} Pin Potential to GND Pin	−7.0 to +0.5V
Input Voltage (dc)	V_{EE} to +0.5V
Output Current (dc Output HIGH)	−30 to +0.1mA

OPERATING RANGE

Range	V_{EE}	Ambient Temperature
COM'L	−5.46 to −4.94V	0 to +75°C
MIL	−5.72 to −4.68V	−55 to +125°C

FUNCTION TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level ≃ −0.9V X = Don't Care
L = LOW Voltage Level ≃ −1.7V

DC CHARACTERISTICS (Commercial)

V_{EE} = −5.2V, V_{CC} = GND, Output Load = 50Ω and 30pF to −2.0V, T_A = 0 to +75°C (Note 2)

Parameters	Description	Test Conditions			B	Typ (Note 1)	A	Units
V_{OH}	Output Voltage HIGH	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50Ω to −2.0V	T_A = 0°C	−1000		−840	mV
				T_A = +25°C	−960		−810	
				T_A = +75°C	−900		−720	
V_{OL}	Output Voltage LOW			T_A = 0°C	−1870		−1665	mV
				T_A = +25°C	−1850		−1650	
				T_A = +75°C	−1830		−1625	
V_{OHC}	Output Voltage HIGH	V_{IN} = V_{IHB} or V_{ILA}		T_A = 0°C	−1020			mV
				T_A = +25°C	−980			
				T_A = +75°C	−920			
V_{OLC}	Output Voltage LOW			T_A = 0°C			−1645	mV
				T_A = +25°C			−1630	
				T_A = +75°C			−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		T_A = 0°C	−1145		−840	mV
				T_A = +25°C	−1105		−810	
				T_A = +75°C	−1045		−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		T_A = 0°C	−1870		−1490	mV
				T_A = +25°C	−1850		−1475	
				T_A = +75°C	−1830		−1450	
I_{IH}	Input Current HIGH	V_{IN} = V_{IHA}		T_A = 0 to +75°C			220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	V_{IN} = V_{ILB}		T_A = +25°C	0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 8)	All Inputs and Outputs Open		T_A = 0°C	−150	−105		mA
				T_A = +75°C		−90		

Notes: 1. Typical values are at V_{EE} = −5.2V, T_A = 25°C and maximum loading.
2. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical thermal resistance values of the package are:
θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
θ_{JC} (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification:
The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

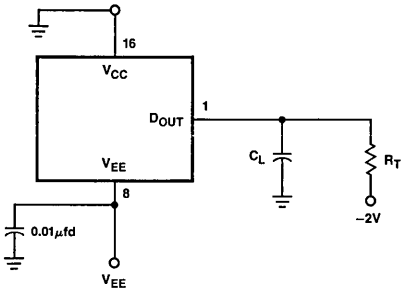
DC CHARACTERISTICS (Military)

V_{EE} = −5.2V, V_{CC} = GND, T_A = −55°C, and +125°C.

Parameters	Description	Test Conditions			B	Typ (Note 1)	A	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50Ω to −2.0V	T_A = −55°C	−1070		−860	mV
				T_A = +125°C	−860		−650	
V_{OL}	Output Voltage LOW			T_A = −55°C	−1900		−1690	mV
				T_A = +125°C	−1800		−1570	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		T_A = −55°C	−1090			mV
				T_A = +125°C	−880			
V_{OLC}	Output Voltage LOW			T_A = −55°C			−1670	mV
				T_A = +125°C			−1550	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		T_A = −55°C	−1215		−860	mV
				T_A = +125°C	−1005		−650	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		T_A = −55°C	−1900		−1515	mV
				T_A = +125°C	−1800		−1395	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$		T_A = −55°C			250	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	$V_{IN} = V_{ILB}$		T_A = −55°C	0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 8)	All Inputs and Outputs Open		T_A = −55°C	−165	−115		mA
				T_A = +125°C		−80		

AC TEST LOAD AND WAVEFORM

AC TEST LOAD



R_T = 50Ω TERMINATION OF MEASUREMENT SYSTEM
C_L = 30pF (INCLUDING STRAY JIG CAPACITANCE)

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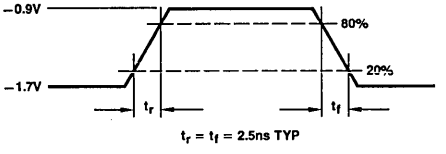
INPUT PULSES



$t_r = t_f$ = 2.5ns TYP

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AC CHARACTERISTICS (Commercial)

V_{EE} = −5.46 to −4.94V, Output Load = 50Ω, 30pF to −2.0V, T_A = 0 to +75°C

Parameters	Description	Test Conditions	Am10415SA Min	Am10415SA Typ (Note 1)	Am10415SA Max	Am10415A Min	Am10415A Typ (Note 1)	Am10415A Max	Am10415 Min	Am10415 Typ (Note 1)	Am10415 Max	Units
READ MODE												
t_{ACS}	Chip Select Access Time	Figure 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})		6	8		6	8		7	10	ns
t_{RCS}	Chip Select Recovery Time			5	8		5	8		7	10	ns
t_{AA}	Address Access Time			10	15		13	20		20	35	ns
WRITE MODE												
t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min)	10	6		12	9		25	15		ns
t_{WSD}	Data Setup Time Prior to Write		2	0		4	0		5	0		ns
t_{WHD}	Data Hold Time After Write		2	0		4	0		5	0		ns
t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min)	3	0		5	3		8	5		ns
t_{WHA}	Address Hold Time After Write		2	0		3	0		4	1		ns
t_{WSCS}	Chip Select Setup Time Prior to Write	Figure 1 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})	2	0		4	0		5	0		ns
t_{WHCS}	Chip Select Hold Time After Write		2	0		4	0		5	0		ns
t_{WS}	Write Disable Time			5	10		5	10		7	10	ns
t_{WR}	Write Recovery Time			6	12		10	15		14	20	ns
RISE TIME AND FALL TIME												
t_r	Output Rise Time	Measured between 20% and 80% points		5			5			5		ns
t_f	Output Fall Time			5			5			5		ns
CAPACITANCE												
C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique		4	5		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	pF

3

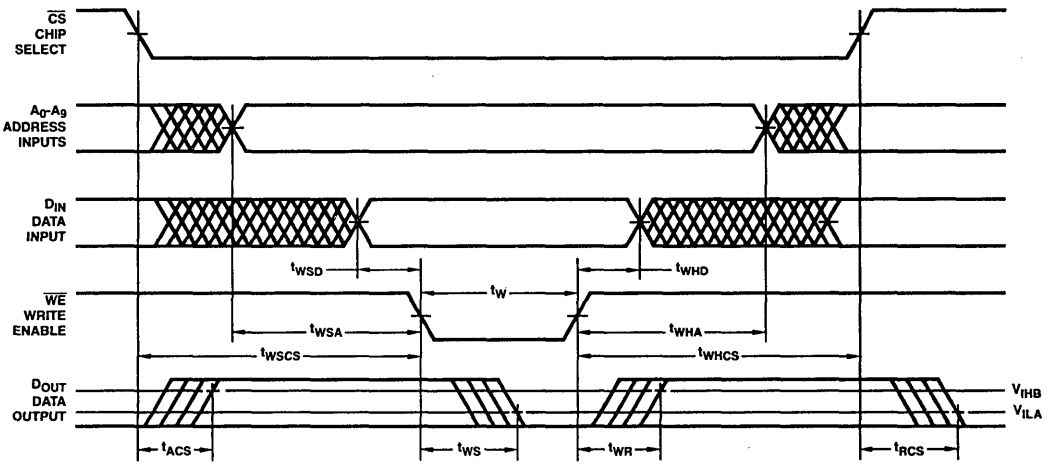
AC CHARACTERISTICS (Military)

V_{EE} = −5.72 to −4.68V, Output Load = 50Ω, 30pF to −2.0V, T_A = −55 to +125°C

Parameters	Description	Test Conditions	Am10415SA Min	Am10415SA Typ (Note 1)	Am10415SA Max	Am10415A Min	Am10415A Typ (Note 1)	Am10415A Max	Am10415 Min	Am10415 Typ (Note 1)	Am10415 Max	Units
READ MODE												
t_{ACS}	Chip Select Access Time	Figure 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})		6	10		6	12		7	15	ns
t_{RCS}	Chip Select Recovery Time			5	10		5	12		7	15	ns
t_{AA}	Address Access Time			10	20		13	25		20	40	ns
WRITE MODE												
t_W	Write Pulse Width	$t_{WSA} = t_{WSA}$ (Min)	13	6		16	9		25	15		ns
t_{WSD}	Data Setup Time Prior to Write		3	0		4	0		7	0		ns
t_{WHD}	Data Hold Time After Write		3	0		4	0		7	0		ns
t_{WSA}	Address Setup Time	$t_W = t_W$ (Min)	4	0		5	3		8	5		ns
t_{WHA}	Address Hold Time		3	0		4	0		7	1		ns
t_{WSCS}	Chip Select Setup Time	Figure 1 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})	3	0		4	0		7	0		ns
t_{WHCS}	Chip Select Hold Time		3	0		4	0		7	0		ns
t_{WS}	Write Disable Time			5	10		5	10		7	10	ns
t_{WR}	Write Recovery Time			6	12		10	15		14	20	ns
RISE TIME AND FALL TIME												
t_r	Output Rise Time	Measured between 20% and 80% points		5			5			5		ns
t_f	Output Fall Time			5			5			5		ns
CAPACITANCE												
C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique		4	5		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	pF

SWITCHING WAVEFORMS

WRITE MODE



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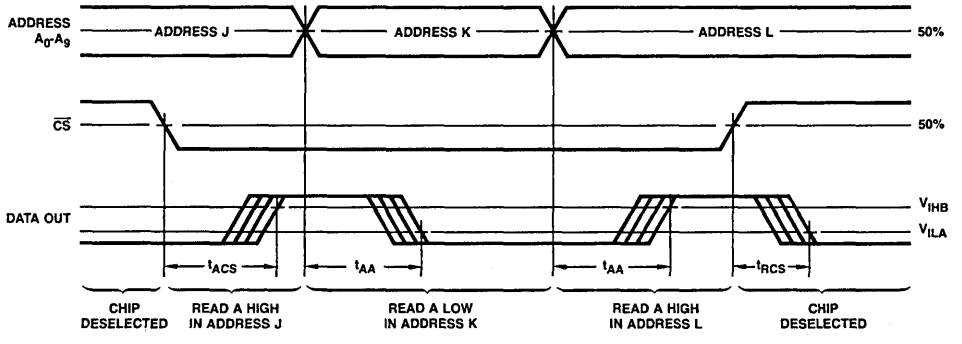
READ MODE



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KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▒▒▒	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▒▒▒	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
▒▒▒	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

ORDERING INFORMATION

Speed Selection	Order Code	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
15ns	AM10415SAPC	P-16-1	C-1	COM'L
	AM10415SAPCB	P-16-1	B-1	
	AM10415SADC	D-16-1	C-1	
	AM10415SADCB	D-16-1	B-1	
	AM10415SALC	Consult Factory	C-1	
	AM10415SALCB	Consult Factory	B-1	
20ns	AM10415SADM	D-16-1	C-3	MIL
	AM10415SADMB	D-16-1	B-3	
	AM10415SAFM	F-16-1	C-3	
	AM10415SAFMB	F-16-1	B-3	
	AM10415SALM	Consult Factory	C-3	
	AM10415SALMB	Consult Factory	B-3	
20ns	AM10415APC	P-16-1	C-1	COM'L
	AM10415APCB	P-16-1	B-1	
	AM10415ADC	D-16-1	C-1	
	AM10415ADCB	D-16-1	B-1	
	AM10415ALC	Consult Factory	C-1	
	AM10415ALCB	Consult Factory	B-1	
25ns	AM10415ADM	D-16-1	C-3	MIL
	AM10415ADMB	D-16-1	B-3	
	AM10415AFM	F-16-1	C-3	
	AM10415AFMB	F-16-1	B-3	
	AM10415ALM	Consult Factory	C-3	
	AM10415ALMB	Consult Factory	B-3	
35ns	AM10415PC	P-16-1	C-1	COM'L
	AM10415PCB	P-16-1	B-1	
	AM10415DC	D-16-1	C-1	
	AM10415DCB	D-16-1	B-1	
	AM10415LC	Consult Factory	C-1	
	AM10415LCB	Consult Factory	B-1	
40ns	AM10415DM	D-16-1	C-3	MIL
	AM10415DMB	D-16-1	B-3	
	AM10415FM	F-16-1	C-3	
	AM10415FMB	F-16-1	B-3	
	AM10415LM	Consult Factory	C-3	
	AM10415LMB	Consult Factory	B-3	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Cerpak.
Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications.
Pad layout and bonding diagram available upon request.

Am100415A • Am100415

ECL 1024 x 1 IMOX™ II Bipolar RAM

DISTINCTIVE CHARACTERISTICS

- Fast access time (10ns typ) – improves system cycle speeds
- Fully compatible with 100K series ECL logic – no board changes required
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- 100% MIL-STD-883C screening and guaranteed to INT-STD-123 insures the highest reliability
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

The Am100415A and Am100415 are fully decoded 1024-bit ECL RAMs organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

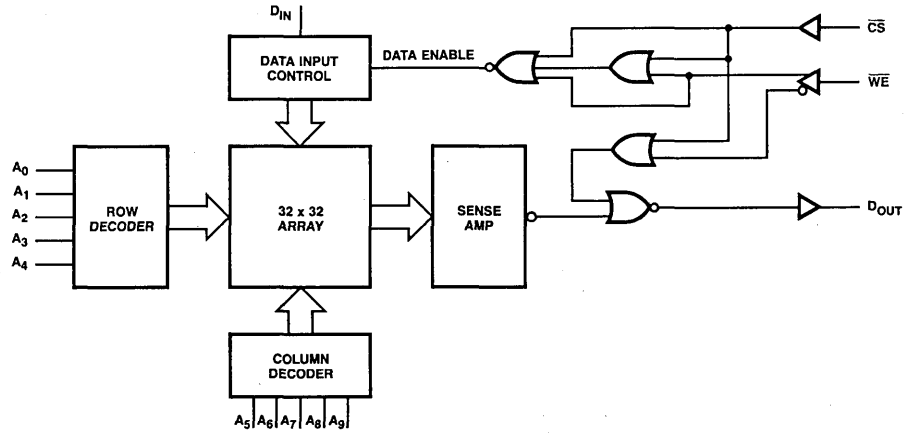
An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

3

LOGIC BLOCK DIAGRAM



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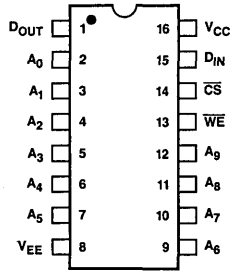
CONNECTION DIAGRAM – Top Views

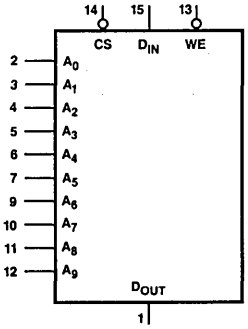
DIP



BPM-187 Note: Pin 1 is marked for orientation.

Chip-Pak™

LOGIC SYMBOL



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V_{CC} = Pin 16
V_{EE} = Pin 8

IMOX is a trademark of Advanced Micro Devices, Inc.
Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
V_{EE} Pin Potential to GND Pin	−7.0 to +0.5V
Input Voltage (dc)	V_{EE} to +0.5V
Output Current (dc Output HIGH)	−30 to +0.1mA

OPERATING RANGE

Part Number	V_{EE}	Ambient Temperature
Commercial	−5.7 to −4.2V	0 to +85°C

FUNCTION TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level = −0.9V
L = LOW Voltage Level = −1.7V
X = Don't Care

DC CHARACTERISTICS

V_{EE} = −4.5V, V_{CC} = GND, Output Load = 50Ω and 30pF to −2.0V, T_A = 0 to +85°C (Note 2)

Parameters	Description	Test Conditions		B	Typ (Note 1)	A	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50Ω to −2.0V	−1025	−955	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1715	−1620	mV
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		−1035			mV
V_{OLC}	Output Voltage LOW					−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for all inputs (Note 4)		−1165		−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for all inputs (Note 4)		−1810		−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$				220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	$V_{IN} = V_{ILB}$		0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 8)	All Inputs and Outputs Open		−150	−105		mA

Notes: 1. Typical values are at V_{EE} = −4.5V, T_A = 25°C and maximum loading.
2. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
θ_{JC} (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification:
The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC CHARACTERISTICS

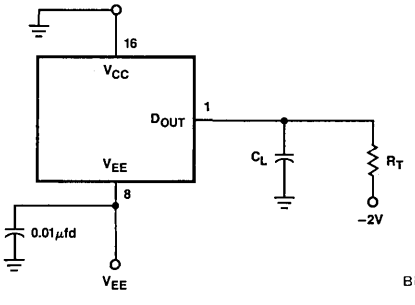
V_{EE} = −4.27V to −4.73V, Output Load = 50Ω, 30pF to −2.0V, T_A = 0 to +85°C

Parameters	Description	Test Conditions	Am100415A Min	Am100415A Typ (Note 1)	Am100415A Max	Am100415 Min	Am100415 Typ (Note 1)	Am100415 Max	Units
READ MODE									
t_{ACS}	Chip Select Access Time	Figure 1 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})		5	8		5	8	ns
t_{RCS}	Chip Select Recovery Time			5	8		5	8	ns
t_{AA}	Address Access Time			10	15		12	20	ns
WRITE MODE									
t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min)	10	6		12	9		ns
t_{WSD}	Data Setup Time Prior to Write		2	0		4	0		ns
t_{WHD}	Data Hold Time After Write		2	0		4	0		ns
t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min)	3	0		5	3		ns
t_{WHA}	Address Hold Time After Write		2	0		3	0		ns
t_{WSCS}	Chip Select Setup Time Prior to Write	Figure 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})	2	0		4	0		ns
t_{WHCS}	Chip Select Hold Time After Write		2	0		4	0		ns
t_{WS}	Write Disable Time			5	10		5	10	ns
t_{WR}	Write Recovery Time			6	12		7	15	ns
RISE TIME AND FALL TIME									
t_r	Output Rise Time	Measured between 20% and 80% points		5			5		ns
t_f	Output Fall Time			5			5		ns
CAPACITANCE									
C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8	pF

3

AC TEST LOAD AND WAVEFORM

AC TEST LOAD



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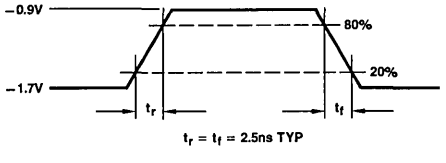
INPUT PULSES



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R_T = 50Ω TERMINATION OF MEASUREMENT SYSTEM
C_L = 30pF (INCLUDING STRAY JIG CAPACITANCE)

SWITCHING WAVEFORMS

READ MODE

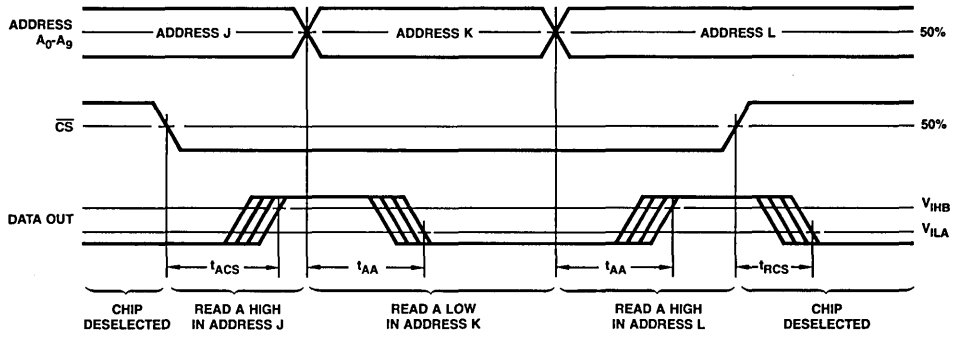


Figure 1.

BPM-191

WRITE MODE

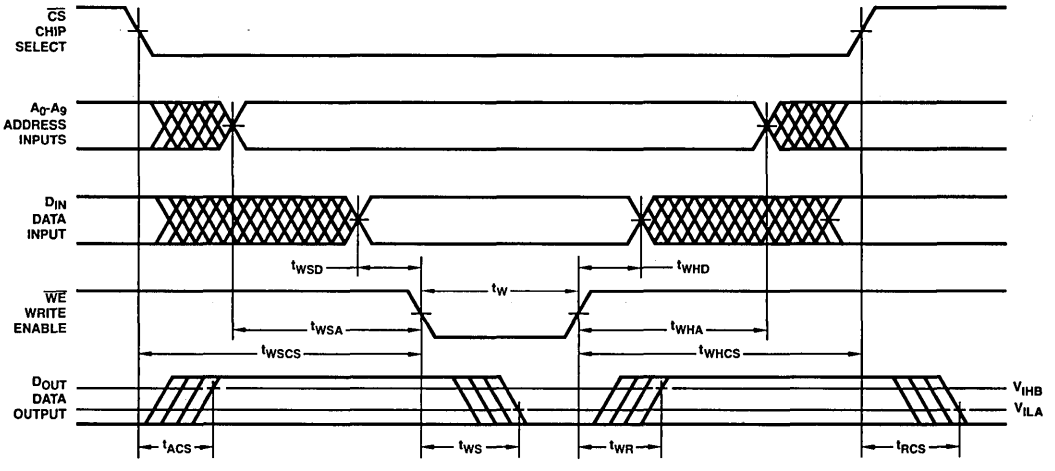


Figure 2.

BPM-192

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANYCHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L			
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

BPM-193

ORDERING INFORMATION

Speed Selection	Order Code	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
15ns	AM100415APC	P-16-1	C-1	COM'L
	AM100415APCB	P-16-1	B-1	
	AM100415ADC	D-16-1	C-1	
	AM100415ADCB	D-16-1	B-1	
	AM100415ALC	Consult Factory	C-1	
	AM100415ALCB	Consult Factory	B-1	
20ns	AM100415PC	P-16-1	C-1	COM'L
	AM100415PCB	P-16-1	B-1	
	AM100415DC	D-16-1	C-1	
	AM100415DCB	D-16-1	B-1	
	AM100415LC	Consult Factory	C-1	
	AM100415LCB	Consult Factory	B-1	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-123, Class C. Levels B-1 and B-3 conform to MIL-STD-123, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial specifications. Pad layout and bonding diagram available upon request.

3

Am10474SA • Am10474A
Am10474

ECL 1024 x 4 IMOX™ Bipolar RAM

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL – no board changes required
- Internally voltage and temperature compensated providing flat AC performance
- 100% MIL-STD-883C screening and guaranteed to INT-STD-123 insures the highest reliability
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

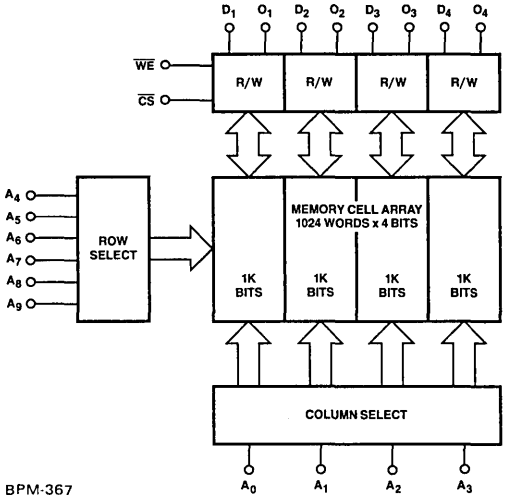
The Am10474SA, Am10474A and Am10474 are fully decoded 4096-bit ECL RAMs organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_1-D_4) are written into the addressed memory words.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting outputs D_1-D_4.

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

LOGIC BLOCK DIAGRAM



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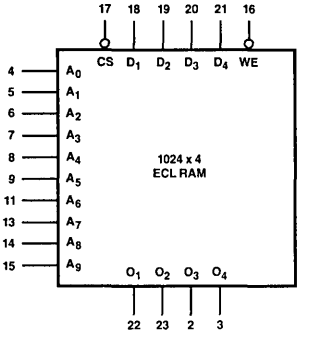
LOGIC SYMBOL



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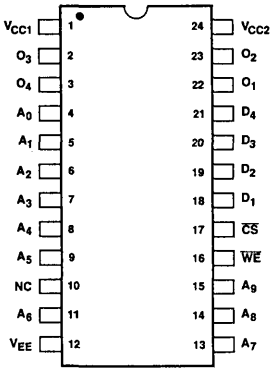
V_{CC2} = Pin 24
V_{EE} = Pin 12

CONNECTION DIAGRAMS – Top Views

DIP



Note: Pin 1 is marked for orientation.

Chip-Pak™

BPM-369

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Am100474SA • Am100474A
Am100474

ECL 1024 x 4 IMOX™ Bipolar RAM

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with 100K series ECL logic – no board changes required
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- 100% MIL-STD-883C screening and guaranteed to INT-STD-123 insures the highest reliability
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

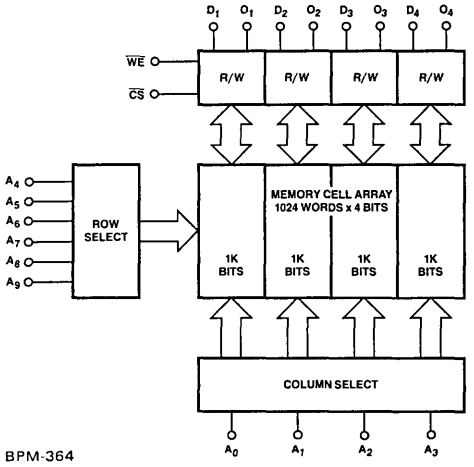
The Am100474SA, Am100474A and Am100474 are fully decoded 4096-bit ECL RAMs organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and unterminated OR tieable emitter follower outputs.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data inputs (D_1-D_4) are written into the addressed memory words.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed words is read out on the noninverting outputs O_1-O_4.

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

LOGIC BLOCK DIAGRAM



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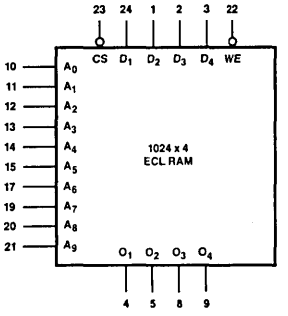
LOGIC SYMBOL



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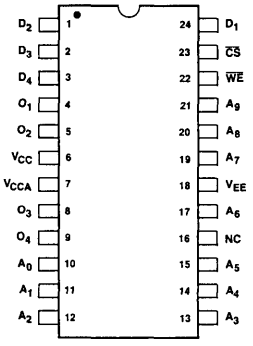
CONNECTION DIAGRAMS – Top Views

DIP



Note: Pin 1 is marked for orientation.

Chip-Pak™

TO BE DETERMINED

BPM-366

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Am10470SA • Am10470A • Am10470

ECL 4096 x 1 IMOX™ Bipolar RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL – no board changes required
- Internally voltage compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- 100% MIL-STD-883C screening and guaranteed to INT-STD-123 insures the highest reliability
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

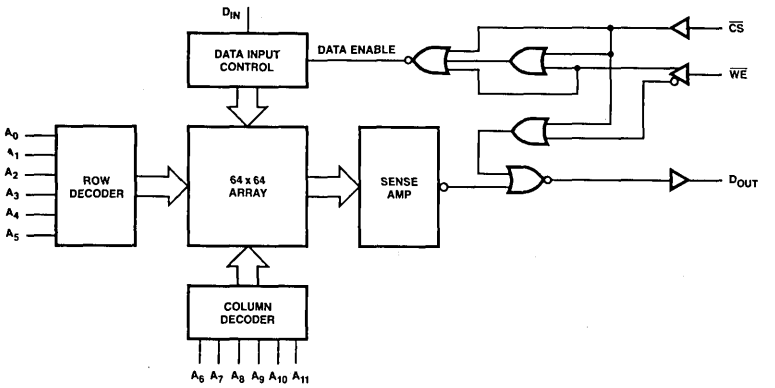
The Am10470SA, Am10470A and Am10470 are fully decoded 4096-bit ECL RAMs organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the 'write recovery glitch.'

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

BLOCK DIAGRAM



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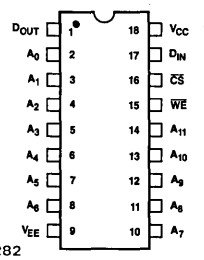
CONNECTION DIAGRAMS – Top Views

DIP



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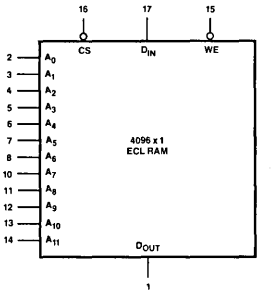
Chip-Pak™

TO BE DETERMINED

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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V_{CC} = Pin 18
V_{EE} = Pin 9

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
V_{EE} Pin Potential to GND Pin	−7.0 to +0.5V
Input Voltage (dc)	V_{EE} to +0.5V
Output Current (dc Output HIGH)	−30 to +0.1mA

OPERATING RANGE

Range	V_{EE}	Ambient Temperature
COM'L	−5.46 to −4.94V	0 to +75°C
MIL	−5.72 to −4.68V	−55 to +125°C

FUNCTION TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level = −0.9V
L = LOW Voltage Level = −1.7V
X = Don't Care

DC CHARACTERISTICS (Commercial)

V_{EE} = −5.2V, V_{CC} = GND, Output Load = 50Ω and 30pF to −2.0V, T_A = 0 to +75°C (Note 2)

Parameters	Description	Test Conditions			B	Typ (Note 1)	A	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50Ω to −2.0V	T_A = 0°C	−1000		−840	mV
				T_A = +25°C	−960		−810	
				T_A = +75°C	−900		−720	
V_{OL}	Output Voltage LOW			T_A = 0°C	−1870		−1665	mV
				T_A = +25°C	−1850		−1650	
				T_A = +75°C	−1830		−1625	
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		T_A = 0°C	−1020			mV
				T_A = +25°C	−980			
				T_A = +75°C	−920			
V_{OLC}	Output Voltage LOW			T_A = 0°C			−1645	mV
				T_A = +25°C			−1630	
				T_A = +75°C			−1605	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		T_A = 0°C	−1145		−840	mV
				T_A = +25°C	−1105		−810	
				T_A = +75°C	−1045		−720	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		T_A = 0°C	−1870		−1490	mV
				T_A = +25°C	−1850		−1475	
				T_A = +75°C	−1830		−1450	
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$		T_A = 0 to +75°C			220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	$V_{IN} = V_{ILB}$		T_A = +25°C	0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 9)	All Inputs and Outputs Open	Am10470A and Am10470	T_A = 0°C	−200	−160		mA
				T_A = +75°C		−145		
			Am10470SA	T_A = 0°C	−230	−180		

Notes: 1. Typical values are at V_{EE} = −5.2V, T_A = 25°C and maximum loading.
2. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical thermal resistance values of the package are:
θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
θ_{JC} (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification:
The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

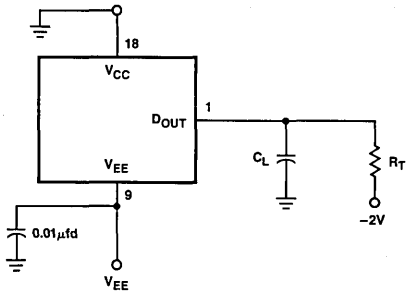
DC CHARACTERISTICS (Military)

V_{EE} = −5.2V, V_{CC} = GND, T_A = −55 to +125°C

Parameters	Description	Test Conditions			B	Typ (Note 1)	A	Units
V_{OH}	Output Voltage HIGH	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50Ω to −2.0V	T_A = −55°C	−1070		−860	mV
				T_A = +125°C	−860		−650	
V_{OL}	Output Voltage LOW			T_A = −55°C	−1900		−1690	mV
				T_A = +125°C	−1800		−1570	
V_{OHC}	Output Voltage HIGH	V_{IN} = V_{IHB} or V_{ILA}		T_A = −55°C	−1090			mV
				T_A = +125°C	−880			
V_{OLC}	Output Voltage LOW			T_A = −55°C			−1670	mV
				T_A = +125°C			−1550	
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for All Inputs (Note 4)		T_A = −55°C	−1215		−860	mV
				T_A = +125°C	−1005		−650	
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for All Inputs (Note 4)		T_A = −55°C	−1900		−1515	mV
				T_A = +125°C	−1800		−1395	
I_{IH}	Input Current HIGH	V_{IN} = V_{IHA}		T_A = −55°C			250	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	V_{IN} = V_{ILB}		T_A = −55°C	0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 9)	All Inputs and Outputs Open	Am10470A and Am10470	T_A = −55°C	−220	−175		mA
				T_A = +125°C		−160		
			Am10470SA	T_A = −55°C	−255	−200		

AC TEST LOAD AND WAVEFORM

AC TEST LOAD



R_T = 50Ω termination of measurement system
C_L = 30pF (including stray jig capacitance)

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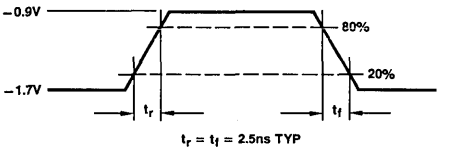
INPUT PULSES



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AC CHARACTERISTICS (Commercial)

V_{EE} = −5.46 to −4.94V, Output Load = 50Ω, 30pF to −2.0V, T_A = 0 to +75°C

PRELIMINARY

Parameters	Description	Test Conditions	Am10470SA Min	Am10470SA Typ (Note 1)	Am10470SA Max	Am10470A Min	Am10470A Typ (Note 1)	Am10470A Max	Am10470 Min	Am10470 Typ (Note 1)	Am10470 Max	Units
READ MODE												
t_{ACS}	Chip Select Access Time	Figure 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})		6	8		8	10		10	15	ns
t_{RCS}	Chip Select Recovery Time			6	8		8	10		10	15	ns
t_{AA}	Address Access Time			12	15		18	25		25	35	ns
WRITE MODE												
t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min)	15	8		20	10		25	15		ns
t_{WSD}	Data Setup Time Prior to Write		2	0		2	0		5	1		ns
t_{WHD}	Data Hold Time After Write		2	0		2	0		5	1		ns
t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min)	2	0		2	0		5	1		ns
t_{WHA}	Address Hold Time After Write		2	0		2	0		5	1		ns
t_{WSCS}	Chip Select Setup Time Prior to Write	Figure 1 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})	2	0		2	0		5	1		ns
t_{WHCS}	Chip Select Hold Time After Write		2	0		2	0		5	1		ns
t_{WS}	Write Disable Time			6	8		8	10		7	15	ns
t_{WR}	Write Recovery Time			6	8		8	10		10	20	ns
RISE TIME AND FALL TIME												
t_r	Output Rise Time	Measured between 20% and 80% points		3			3			3		ns
t_f	Output Fall Time			3			3			3		ns
CAPACITANCE												
C_{IN}	Input Pin Capacitance	Measured with a Pulse Technique on a Sample Basis.		4	5		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	pF

3

AC CHARACTERISTICS (Military)

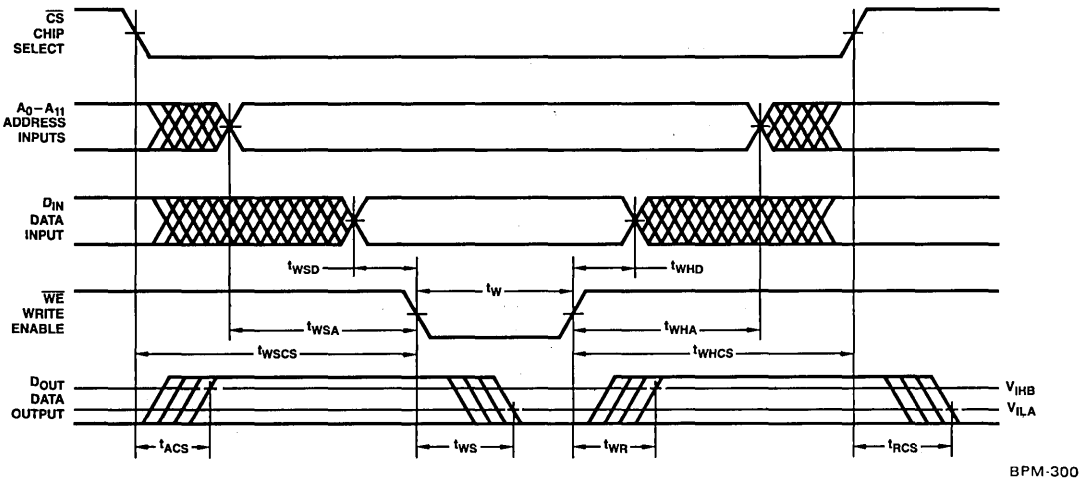
V_{EE} = −5.72 to −4.68V, Output Load = 50Ω, 30pF to −2.0V, T_A = −55 to +125°C

PRELIMINARY

Parameters	Description	Test Conditions	Am10470SA Min	Am10470SA Typ (Note 1)	Am10470SA Max	Am10470A Min	Am10470A Typ (Note 1)	Am10470A Max	Am10470 Min	Am10470 Typ (Note 1)	Am10470 Max	Units
READ MODE												
t_{ACS}	Chip Select Access Time	Figure 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})		8	10		10	15		15	20	ns
t_{RCS}	Chip Select Recovery Time			8	10		10	15		15	20	ns
t_{AA}	Address Access Time			17	20		20	30		30	40	ns
WRITE MODE												
t_W	Write Pulse Width	$t_{WSA} = t_{WSA}$ (Min)	18	14		22	17		25	20		ns
t_{WSD}	Data Setup Time Prior to Write		3	0		5	0		7	2		ns
t_{WHD}	Data Hold Time After Write		3	0		5	0		7	2		ns
t_{WSA}	Address Setup Time	$t_W = t_W$ (Min)	3	0		5	0		7	2		ns
t_{WHA}	Address Hold Time		3	0		5	0		7	2		ns
t_{WSCS}	Chip Select Setup Time	Figure 1 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})	3	0		5	0		7	2		ns
t_{WHCS}	Chip Select Hold Time		3	0		5	0		7	2		ns
t_{WS}	Write Disable Time			8	10		10	12		7	15	ns
t_{WR}	Write Recovery Time			8	10		10	12		10	20	ns
RISE TIME AND FALL TIME												
t_r	Output Rise Time	Measured between 20% and 80% points		3			3			3		ns
t_f	Output Fall Time			3			3			3		ns
CAPACITANCE												
C_{IN}	Input Pin Capacitance	Measured with a Pulse Technique on a Sample Basis.		4	5		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	pF

SWITCHING WAVEFORMS

WRITE MODE



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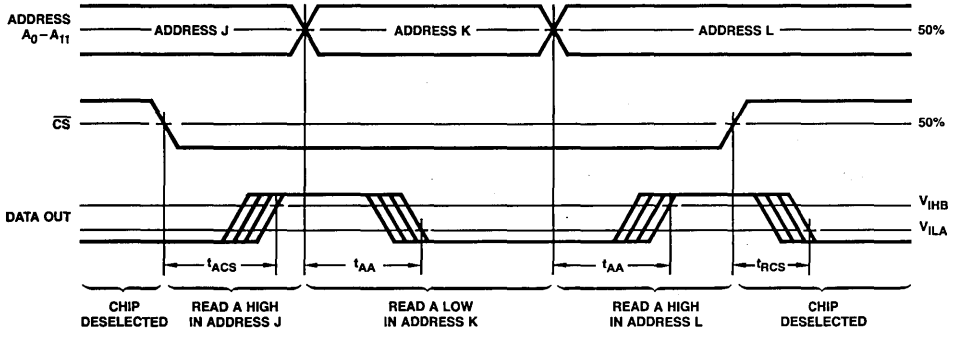
READ MODE



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KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
⟋⟋⟋	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
⟋⟋⟋	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
⟋⟍⟋⟍	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

ORDERING INFORMATION

Speed Selection	Order Code	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
15ns	AM10470SADC	D-18-1	C-1	COM'L
	AM10470SADCB	D-18-1	B-1	
	AM10470SALC	Consult Factory	C-1	
	AM10470SALCB	Consult Factory	B-1	
20ns	AM10470SADM	D-18-1	C-3	MIL
	AM10470SADMB	D-18-1	B-3	
	AM10470SAFM	Consult Factory	C-3	
	AM10470SAFMB	Consult Factory	B-3	
	AM10470SALM	Consult Factory	C-3	
	AM10470SALMB	Consult Factory	B-3	
25ns	AM10470ADC	D-18-1	C-1	COM'L
	AM10470ADCB	D-18-1	B-1	
	AM10470ALC	Consult Factory	C-1	
	AM10470ALCB	Consult Factory	B-1	
30ns	AM10470ADM	D-18-1	C-3	MIL
	AM10470ADMB	D-18-1	B-3	
	AM10470AFM	Consult Factory	C-3	
	AM10470AFMB	Consult Factory	B-3	
	AM10470ALM	Consult Factory	C-3	
	AM10470ALMB	Consult Factory	B-3	
35ns	AM10470DC	D-18-1	C-1	COM'L
	AM10470DCB	D-18-1	B-1	
	AM10470LC	Consult Factory	C-1	
	AM10470LCB	Consult Factory	B-1	
40ns	AM10470DM	D-18-1	C-3	MIL
	AM10470DMB	D-18-1	B-3	
	AM10470FM	Consult Factory	C-3	
	AM10470FMB	Consult Factory	B-3	
	AM10470LM	Consult Factory	C-3	
	AM10470LMB	Consult Factory	B-3	

Notes: 1. D = Hermetic DIP, L = Chip-Pak, F = Cerpak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Levels B-1 and B-3 conform to MIL-STD-883, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial and military specifications.
Pad layout and bonding diagram available upon request.

Am100470SA • Am100470A
Am100470

ECL 4096 x 1 IMOX™ Bipolar RAM

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with 100K series ECL logic – no board changes required
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- 100% MIL-STD-883C screening and guaranteed to INT-STD-123 insures the highest reliability
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

The Am100470SA, Am100470A and Am100470 are fully decoded 4096-bit ECL RAMs organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

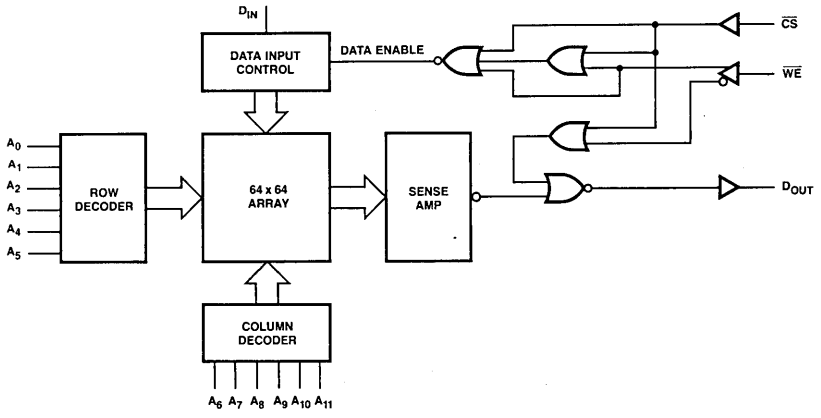
An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the 'write recovery glitch.'

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

3

LOGIC BLOCK DIAGRAM



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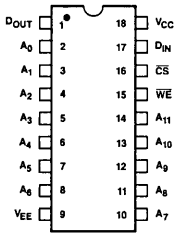
CONNECTION DIAGRAM – Top Views

DIP



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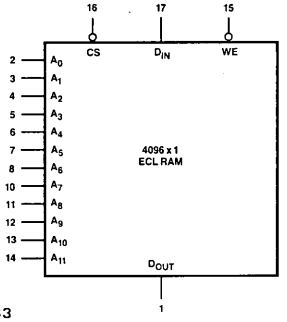
Chip-Pak™

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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V_{CC} = Pin 18
V_{EE} = Pin 9

IMOX is a trademark of Advanced Micro Devices, Inc.
Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
V_{EE} Pin Potential to GND Pin	−7.0 to +0.5V
Input Voltage (dc)	V_{EE} to +0.5V
Output Current (dc Output HIGH)	−30 to +0.1mA

OPERATING RANGE

Part Number	V_{EE}	Ambient Temperature
Commercial	−5.7 to −4.2V	0 to +85°C

FUNCTION TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level = −0.9V
L = LOW Voltage Level = −1.7V
X = Don't Care

DC CHARACTERISTICS

V_{EE} = −4.5V, V_{CC} = GND, Output Load = 50Ω and 30pF to −2.0V, T_A = 0 to +85°C (Note 2)

Parameters	Description	Test Conditions		B	Typ (Note 1)	A	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50Ω to −2.0V	−1025	−955	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1715	−1620	mV
V_{OHC}	Output Voltage HIGH	$V_{IN} = V_{IHB}$ or V_{ILA}		−1035			mV
V_{OLC}	Output Voltage LOW					−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH for all inputs (Note 4)		−1165		−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW for all inputs (Note 4)		−1810		−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IHA}$				220	μA
I_{IL}	Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs	$V_{IN} = V_{ILB}$		0.5 −50		170	μA
I_{EE}	Power Supply Current (Pin 9)	All Inputs and Outputs Open	Am100470A/Am100470	−195	−160		mA
			Am100470SA	−230	−180		

Notes: 1. Typical values are at V_{EE} = −4.5V, T_A = 25°C and maximum loading.
2. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
θ_{JC} (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification:
The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC CHARACTERISTICS (Commercial)

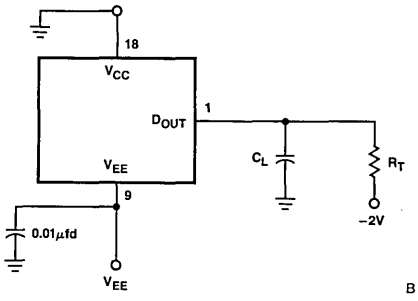
V_{EE} = −5.46 to −4.94V, Output Load = 50Ω, 30pF to −2.0V, T_A = 0 to +85°C

PRELIMINARY

Parameters	Description	Test Conditions	Am100470SA Min	Am100470SA Typ (Note 1)	Am100470SA Max	Am100470A Min	Am100470A Typ (Note 1)	Am100470A Max	Am100470 Min	Am100470 Typ (Note 1)	Am100470 Max	Units
READ MODE												
t_{ACS}	Chip Select Access Time	Figure 2 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})		6	8		8	10		10	15	ns
t_{RCS}	Chip Select Recovery Time			6	8		8	10		10	15	ns
t_{AA}	Address Access Time			12	15		18	25		25	35	ns
WRITE MODE												
t_W	Write Pulse Width (to Guarantee Writing)	$t_{WSA} = t_{WSA}$ (Min)	15			20			25	18		ns
t_{WSD}	Data Setup Time Prior to Write		2			2			5	1		ns
t_{WHD}	Data Hold Time After Write		2			2			5	1		ns
t_{WSA}	Address Setup Time Prior to Write	$t_W = t_W$ (Min)	3			3			10	5		ns
t_{WHA}	Address Hold Time After Write		2			2			5	1		ns
t_{WSCS}	Chip Select Setup Time Prior to Write	Figure 1 measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})	2			2			5	1		ns
t_{WHCS}	Chip Select Hold Time After Write		2			2			5	1		ns
t_{WS}	Write Disable Time			6	8		8	10		7	15	ns
t_{WR}	Write Recovery Time			6	8		8	10		10	20	ns
RISE TIME AND FALL TIME												
t_r	Output Rise Time	Measured between 20% and 80% points		2			2			2		ns
t_f	Output Fall Time			2			2			2		ns
CAPACITANCE												
C_{IN}	Input Pin Capacitance	Measured with a Pulse Technique on a Sample Basis.		4	5		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	pF

AC TEST LOAD AND WAVEFORM

AC TEST LOAD



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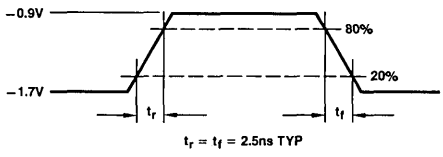
INPUT PULSES



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R_T = 50Ω termination of measurement system
C_L = 30pF (including stray jig capacitance)

SWITCHING WAVEFORMS
READ MODE

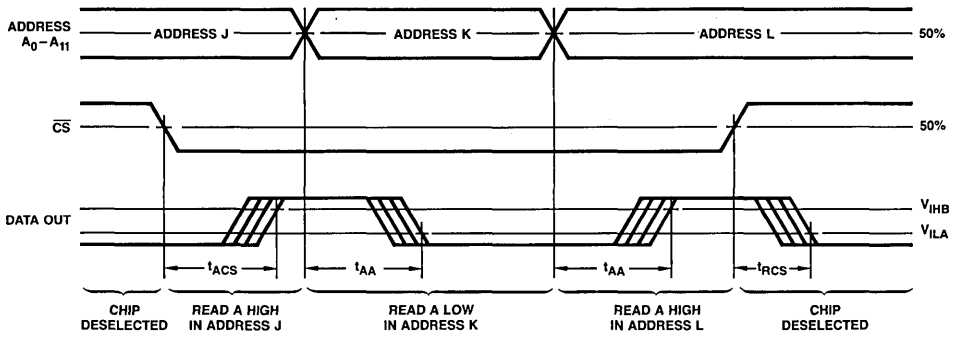

Figure 1.

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WRITE MODE

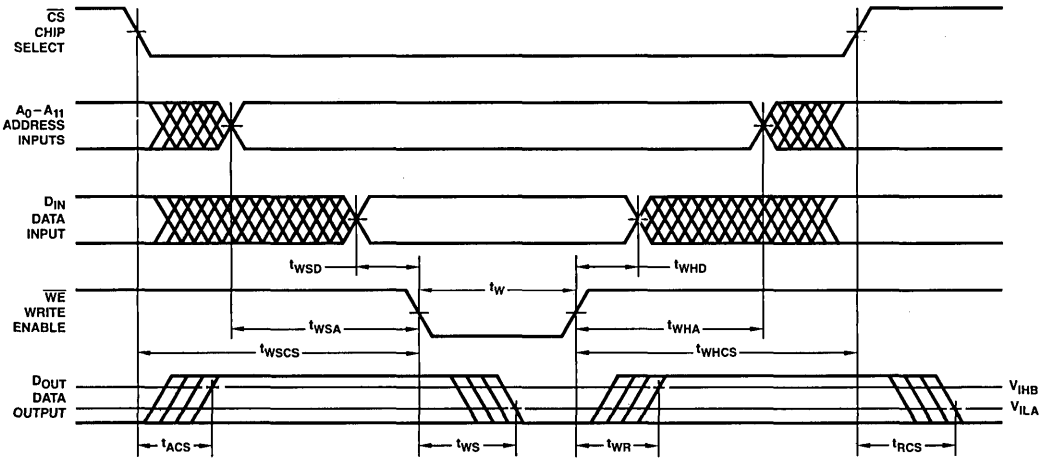

Figure 2.

BPM-285

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
▨	DOES NOT APPLY	CENTER *LINE IS HIGH* IMPEDANCE "OFF" STATE

BPM-193

ORDERING INFORMATION

Speed Selection	Order Code	Package Type (Note 1)	Screening Flow Code (Note 2)	Operating Range (Note 3)
15ns	AM100470SADC	D-18-1	C-1	COM'L
	AM100470SADCB	D-18-1	B-1	
	AM100470SALC	Consult Factory	C-1	
	AM100470SALCB	Consult Factory	B-1	
20ns	AM100470ADC	D-18-1	C-1	COM'L
	AM100470ADCB	D-18-1	B-1	
	AM100470ALC	Consult Factory	C-1	
	AM100470ALCB	Consult Factory	B-1	
35ns	AM100470DC	D-18-1	C-1	COM'L
	AM100470DCB	D-18-1	B-1	
	AM100470LC	Consult Factory	C-1	
	AM100470LCB	Consult Factory	B-1	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-123, Class C. Levels B-1 and B-3 conform to MIL-STD-123, Class B.
3. See Operating Range Table.

This device is also available in die form selected to commercial specifications. Pad layout and bonding diagram available upon request.

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MOS Random Access Memories (RAM) Index

Am9101/Am91L01/Am2101 Family

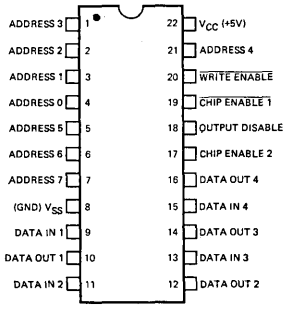
256 x 4 Static R/W Random Access Memories

Part Number	Am2101	Am2101-2	Am9101A Am91L01A Am2101-1	Am9101B Am91L01B	Am9101C Am91L01C	Am9101D
Access Time	1000ns	650ns	500ns	400ns	300ns	250ns

DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization
- Low operating power
  125mW typ; 290mW maximum – standard power
  100mW typ; 175mW maximum – low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive – two full TTL loads
- High noise immunity – full 400mV
- Single +5 volt power supply – tolerances ±5% commercial, ±10% military
- Uniform switching characteristics – access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Two chip enable inputs
- Output disable control
- Zero address setup and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MOS-344

FUNCTIONAL DESCRIPTION

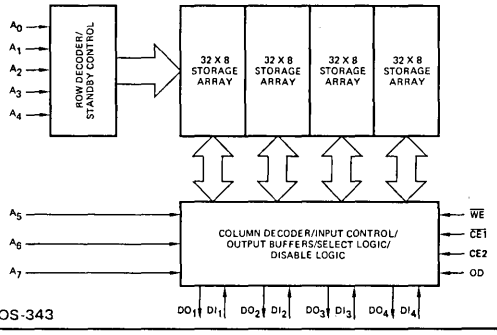
The Am9101/Am91L01 series of devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L01 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are fully static and no refresh operations, sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

Am9101 BLOCK DIAGRAM



MOS-343

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Power Type	Access Times					
			1000ns	650ns	500ns	400ns	300ns	250ns
0 to +70°C	Molded DIP	Standard	P2101	P2101-2	P2101-1 AM9101APC	AM9101BPC	AM9101CPC	AM9101DPC
		Low			AM91L01APC	AM91L01BPC	AM91L01CPC	
	Hermetic DIP	Standard	C2101	C2101-2	C2101-1 AM9101ADC	AM9101BDC	AM9101CDC	AM9101DDC
		Low			AM91L01ADC	AM91L01BDC	AM91L01CDC	
−55 to +125°C	Hermetic DIP	Standard			AM9101ADM	AM9101BDM	AM9101CDM	
		Low			AM91L01ADM	AM91L01BDM	AM91L01CDM	

4

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} With Respect to V_{SS}, Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS

Am9101PC, Am9101DC
Am91L01PC, Am91L01DC
Am2101

T_A = 0°C to +70°C
V_{CC} = +5.0V ±5%

Parameters	Description	Test Conditions			Am9101/ Am91L01 Family Min.	Am9101/ Am91L01 Family Max.	Am2101 Family Min.	Am2101 Family Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.		I_{OH} = −200μA	2.4				Volts
				I_{OH} = −150μA			2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN.		I_{OL} = 3.2mA		0.4			Volts
				I_{OL} = 2.0mA				0.45	
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.2	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.65	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., 0V ≤ V_{IN} ≤ 5.25V				10		10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}}$ = V_{IH}		V_{OUT} = V_{CC}		5.0		15	μA
				V_{OUT} = 0.4V		−10		−50	
I_{CC1}	Power Supply Current	Data out open V_{CC} = Max. V_{IN} = V_{CC}	T_A = 25°C	Am9101A/B		50		60	mA
				Am9101C/D/E		55			
				Am91L01A/B		31			
				Am91L01C		34			
I_{CC2}			T_A = 0°C	Am9101A/B		55		70	
				Am9101C/D/E		60			
				Am91L01A/B		33			
				Am91L01C		36			

ELECTRICAL CHARACTERISTICS

Am9101DM
Am91L01DM

T_A = −55°C to +125°C
V_{CC} = +5.0V ±10%

Parameters	Description	Test Conditions			Am9101/ Am91L01 Family Min.	Am9101/ Am91L01 Family Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −200μA		V_{CC} = 4.75V	2.4		Volts
				V_{CC} = 4.5V	2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., 0V ≤ V_{IN} ≤ 5.5V				10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}}$ = V_{IH}		V_{OUT} = V_{CC}		10	μA
				V_{OUT} = 0.4V		−10	
I_{CC1}	Power Supply Current	Data out open V_{CC} = Max. V_{IN} = V_{CC}	T_A = 25°C	Am9101A/B		50	mA
				Am9101C		55	
				Am91L01A/B		31	
				Am91L01C		34	
I_{CC3}			T_A = −55°C	Am9101A/B		60	
				Am9101C		65	
				Am91L01A/B		37	
				Am91L01C		40	

CAPACITANCE

Parameters	Description	Test Conditions		Typ.	Max.	Units
C_{IN}	Input Capacitance, V_{IN} = 0V	T_A = 25°C, f = 1MHz	Am2101	4.0	8.0	pF
			Am9101/Am91L01	3.0	6.0	
C_{OUT}	Output Capacitance, V_{OUT} = 0V		Am2101	8.0	12	pF
			Am9101/Am91L01	6.0	9.0	

SWITCHING CHARACTERISTICS over operating temperature and voltage range

Output Load = 1 TTL Gate + 100pF — T_A = 0 to 70°C — V_{CC} = +5V ±5%
Transition Times = 10ns — T_A = −55 to +125°C — V_{CC} = +5V ±10%
Input Levels, Output References = 0.8V and 2.0V

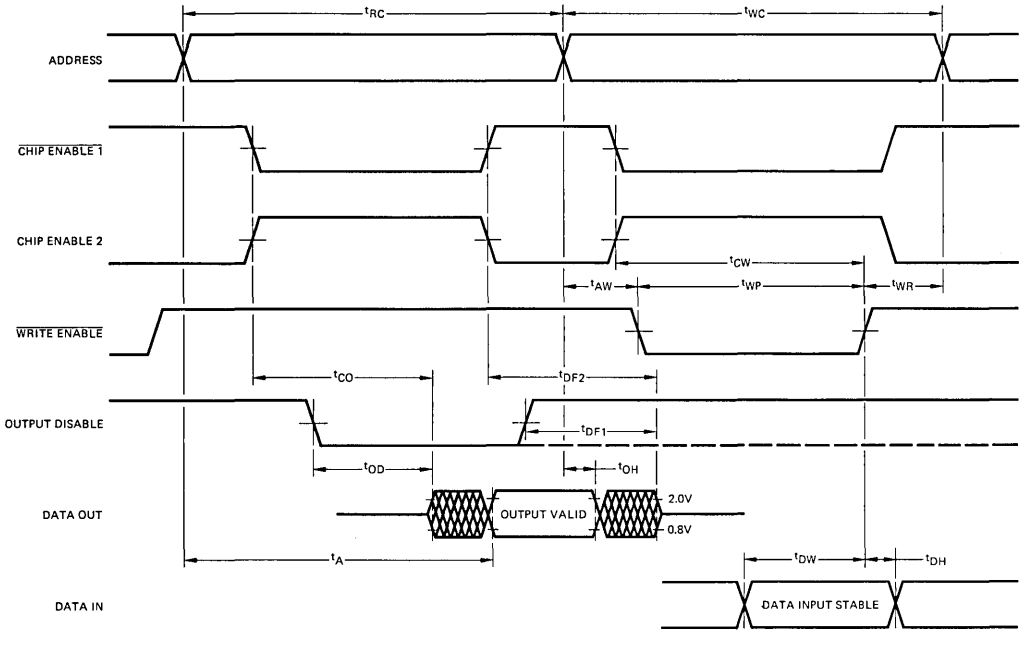
		2101		2101-2		2101-1		9101A 91L01A		9101B 91L01B		9101C 91L01C		9101D		
Parameters	**Description**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{RC}	Read Cycle Time	1000		650		500		500		400		300		250		ns
t_A	Access Time		1000		650		500		500		400		300		250	ns
t_{CO}	Chip Enable to Output ON Delay (Note 1)		800		400		350		200		175		150		125	ns
t_{OD}	Output Disable to Output ON Delay		700		350		300		175		150		125		100	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change	0		0		0		40		40		40		30		ns
t_{DF1}	Output Disable to Output OFF Delay	0	200	0	150	0	150	5.0	125	5.0	100	5.0	100	5.0	75	ns
t_{DF2}	Chip Enable to Output OFF Delay	0	200	0	150	0	150	10	125	10	125	10	100	10	100	ns
t_{WC}	Write Cycle Time	1000		650		500		500		400		300		250		ns
t_{AW}	Address Set-up Time	150		150		100		0		0		0		0		ns
t_{WP}	Write Pulse Width	750		400		300		175		150		125		100		ns
t_{CW}	Chip Enable Set-up Time (Note 1)	900		550		400		175		150		125		100		ns
t_{WR}	Address Hold Time	50		50		50		0		0		0		0		ns
t_{DW}	Input Data Set-up Time	700		400		280		150		125		100		85		ns
t_{DH}	Input Data Hold Time	100		100		100		0		0		0		0		ns

Note: 1. Both $\overline{CE1}$ and CE2 must be true to enable the chip.

4

SWITCHING WAVEFORMS

READ CYCLE — WRITE CYCLE



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DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE1}$, CE2 Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ is low and CE2 is high.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{OD} Output enable time. Delay time from falling edge of OD to output on.

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

t_{OH} Minimum time which will elapse between change of address and any change of the data output.

t_{DF1} Time delay between output disable HIGH and output data float.

t_{DF2} Time delay between chip enable OFF and output data float.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

t_{CW} Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

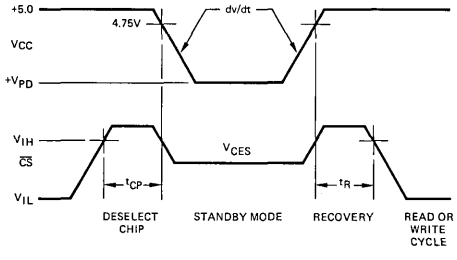
POWER DOWN STANDBY OPERATION

The Am9101/Am91L01 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

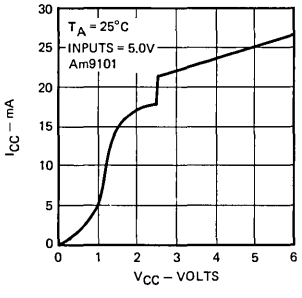
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

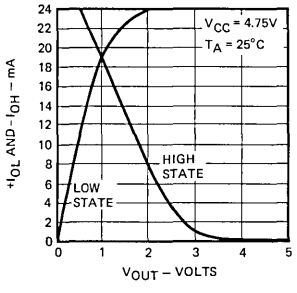
Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$ All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L01		11	25	mA
				Am9101		13	31	
			$V_{PD} = 2.0V$	Am91L01		13	31	
				Am9101		17	41	
		$T_A = -55°C$ All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L01		11	28	mA
				Am9101		13	34	
			$V_{PD} = 2.0V$	Am91L01		13	34	
				Am9101		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts



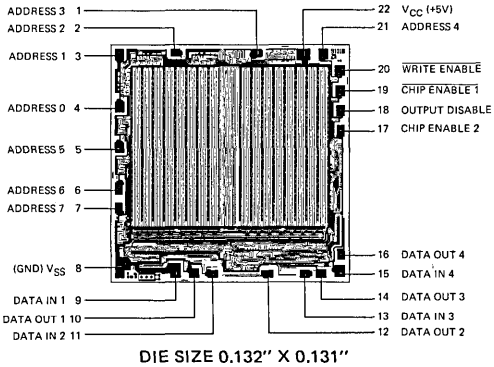
Typical Power Supply Current Versus Voltage



Typical Output Current Versus Voltage

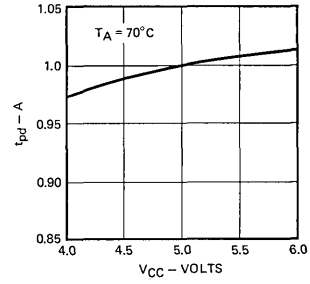


Metallization and Pad Layout

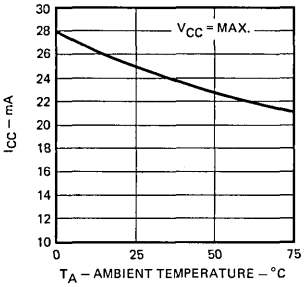


DIE SIZE 0.132" X 0.131"

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



Typical Power Supply Current Versus Ambient Temperature



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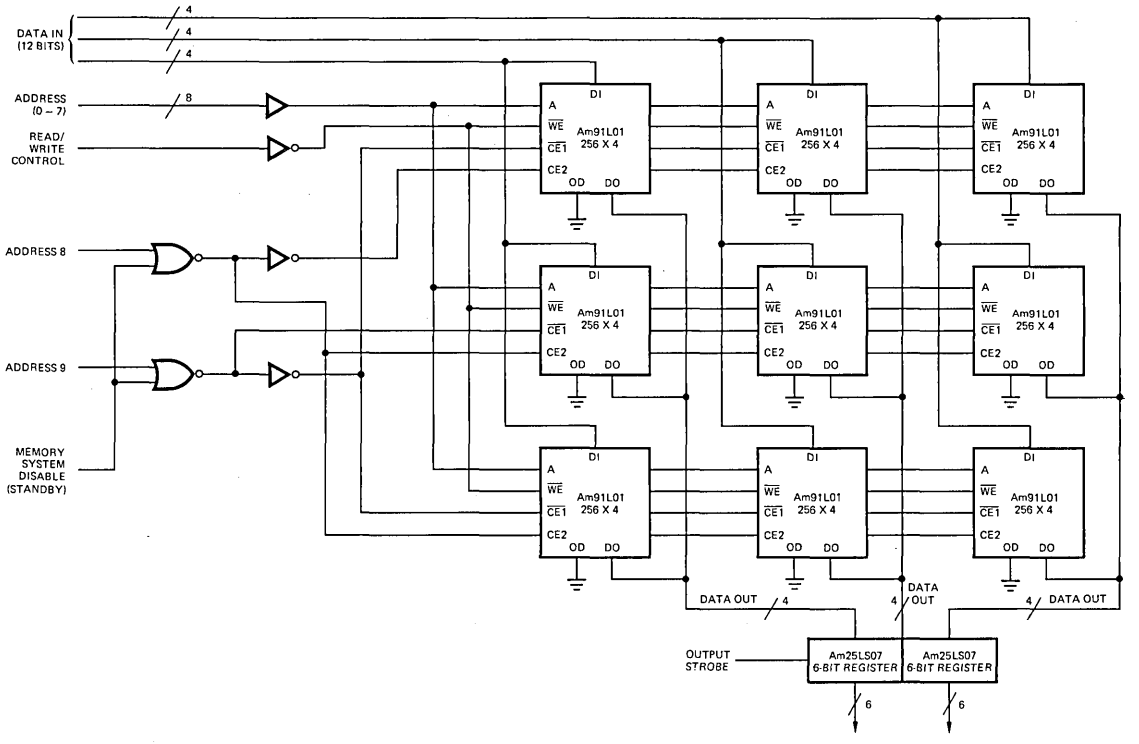
APPLICATIONS



MEMORY SYSTEM
768 WORDS BY 12 BITS PER WORD

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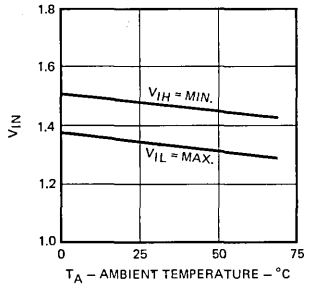
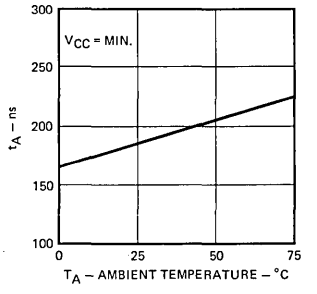
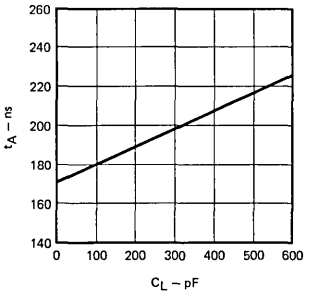
Typical V_{IN} Limits Versus Ambient Temperature



Typical t_A Versus Ambient Temperature



Typical t_A Versus C_L



MOS-349

Am9111/Am91L11/Am2111 Family

256 x 4 Static R/W Random Access Memories

Part Number	Am2111	Am2111-2	Am9111A Am91L11A Am2111-1	Am9111B Am91L11B	Am9111C Am91L11C	Am9111D
Access Time	1000ns	650ns	500ns	400ns	300ns	250ns

DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization for small memory systems
- Low operating power dissipation
  125mW typ; 290mW maximum – standard power
  100mW typ; 175mW maximum – low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive – two full TTL loads
- High noise immunity – full 400mV
- Single +5 volt power supply – tolerances ±5% commercial, ±10% military
- Uniform switching characteristics – access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Bussed input and output data on common pins
- Output disable control
- Zero address setup and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DESCRIPTION

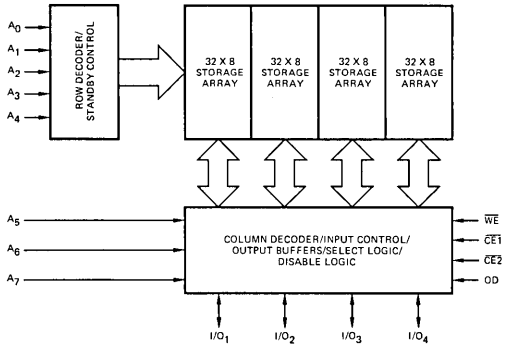
The Am9111/Am91L11 series of devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth. The input data and output data signals are bussed together to share common I/O pins. This feature not only decreases the package size, but also helps eliminate external logic in bus-oriented memory systems.

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L11 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are fully static and no refresh operations, sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

Am9111 BLOCK DIAGRAM



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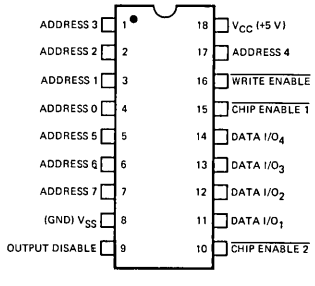
CONNECTION DIAGRAM
Top View



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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} With Respect to V_{SS}, Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS

Am9111PC, Am91L11PC, Am2111: T_A = 0°C to +70°C, V_{CC} = +5.0V ±5%

Parameters	Description	Test Conditions			Am9111/Am91L11 Family Min.	Am9111/Am91L11 Family Max.	Am2111 Family Min.	Am2111 Family Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.		I_{OH} = −200μA	2.4				Volts
				I_{OH} = −150μA			2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN.		I_{OL} = 3.2mA		0.4			Volts
				I_{OL} = 2.0mA				0.45	
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.2	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	−0.5	0.65	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., 0V ≤ V_{IN} ≤ 5.25V				10		10	μA
I_{LO}	I/O Leakage Current	$V_{\overline{CE}} = V_{IH}$		$V_{OUT} = V_{CC}$		5.0		15	μA
				V_{OUT} = 0.4V		−10		−50	
I_{CC1}	Power Supply Current	Data out open, V_{CC} = Max., $V_{IN} = V_{CC}$	T_A = 25°C	Am9111A/B		50		60	mA
				Am9111C/D/E		55			
				Am91L11A/B		31			
				Am91L11C		34			
I_{CC2}			T_A = 0°C	Am9111A/B		55		70	
				Am9111C/D/E		60			
				Am91L11A/B		33			
				Am91L11C		36			

ELECTRICAL CHARACTERISTICS

Am9111DM, Am91L11DM: T_A = −55°C to +125°C, V_{CC} = +5.0V ±10%

Parameters	Description	Test Conditions			Am9111/Am91L11 Family Min.	Am9111/Am91L11 Family Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −200μA		V_{CC} = 4.75V	2.4		Volts
				V_{CC} = 4.5V	2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., 0V ≤ V_{IN} ≤ 5.5V				10	μA
I_{LO}	Output Leakage Current	$V_{\overline{CE}} = V_{IH}$		$V_{OUT} = V_{CC}$		10	μA
				V_{OUT} = 0.4V		−10	
I_{CC1}	Power Supply Current	Data out open, V_{CC} = Max., $V_{IN} = V_{CC}$	T_A = 25°C	Am9111A/Am9111B		50	mA
				Am9111C		55	
				Am91L11A/Am91L11B		31	
				Am91L11C		34	
I_{CC3}			T_A = −55°C	Am9111A/Am9111B		60	
				Am9111C		65	
				Am91L11A/Am91L11B		37	
				Am91L11C		40	

CAPACITANCE

Parameters	Description	Test Conditions		Typ.	Max.	Units
C_{IN}	Input Capacitance, V_{IN} = 0V	T_A = 25°C, f = 1 mHz	Am2111	4.0	8.0	pF
			Am9111/Am91L11	3.0	6.0	
C_{OUT}	Output Capacitance, V_{OUT} = 0V		Am2111	10	15	pF
			Am9111/Am91L11	8.0	11	

SWITCHING CHARACTERISTICS over operating temperature and voltage range

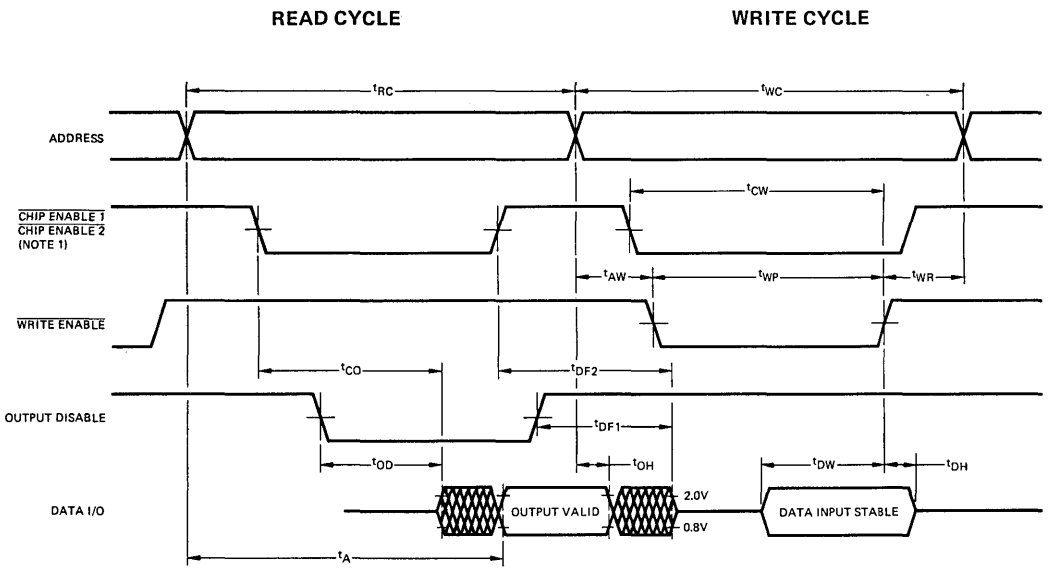
Output Load = 1 TTL Gate + 100pF T_A = 0 to 70°C V_{CC} = +5V ±5%
Transition Times = 10ns T_A = −55 to +125°C V_{CC} = +5V ±10%
Input Levels, Output References = 0.8V and 2.0V

		2111		2111-2		2111-1		9111A 91L11A		9111B 91L11B		9111C 91L11C		9111D		
Parameters	**Description**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{RC}	Read Cycle Time	1000		650		500		500		400		300		250		ns
t_A	Access Time		1000		650		500		500		400		300		250	ns
t_{CO}	Chip Enable to Output ON Delay (Note 1)		800		400		350		200		175		150		125	ns
t_{OD}	Output Disable to Output ON Delay		700		350		300		175		150		125		100	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change	0		0		0		40		40		40		30		ns
t_{DF1}	Output Disable to Output OFF Delay	0	200	0	150	0	150	5.0	125	5.0	100	5.0	100	5.0	75	ns
t_{DF2}	Chip Enable to Output OFF Delay	0	200	0	150	0	150	10	150	10	125	10	125	10	100	ns
t_{WC}	Write Cycle Time	1000		650		500		500		400		300		250		ns
t_{AW}	Address Set-up Time	150		150		100		0		0		0		0		ns
t_{WP}	Write Pulse Width	750		400		300		175		150		125		100		ns
t_{CW}	Chip Enable Set-up Time (Note 1)	900		550		400		175		150		125		100		ns
t_{WR}	Address Hold Time	50		50		50		0		0		0		0		ns
t_{DW}	Input Data Set-up Time	700		400		280		150		125		100		85		ns
t_{DH}	Input Data Hold Time	100		100		100		0		0		0		0		ns

Note: 1. Both $\overline{CE1}$ and $\overline{CE2}$ must be LOW to enable the chip.

4

SWITCHING WAVEFORMS



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DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE1}$, $\overline{CE2}$ Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ and $\overline{CE2}$ are LOW.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if WE is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{OD} Output enable time. Delay time from falling edge of OD to output on.

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

t_{OH} Minimum time which will elapse between change of address and any change of the data output.

t_{DF1} Time delay between output disable HIGH and output data float.

t_{DF2} Time delay between chip enable OFF and output data float.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

t_{CW} Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

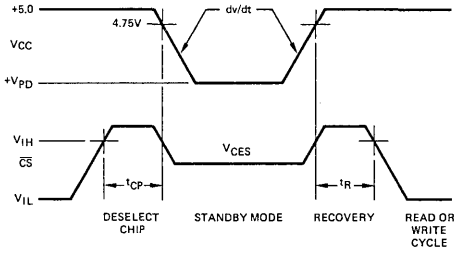
POWER DOWN STANDBY OPERATION

The Am9111/Am91L11 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

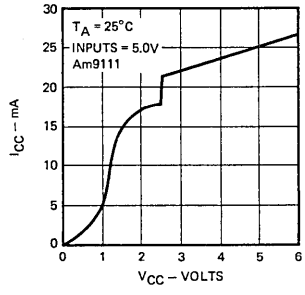
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

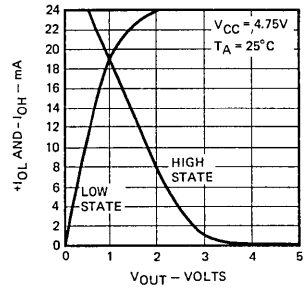
Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L11		11	25	mA
				Am9111		13	31	
			$V_{PD} = 2.0V$	Am91L11		13	31	
				Am9111		17	41	
		$T_A = -55°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L11		11	28	mA
				Am9111		13	34	
			$V_{PD} = 2.0V$	Am91L11		13	34	
				Am9111		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts



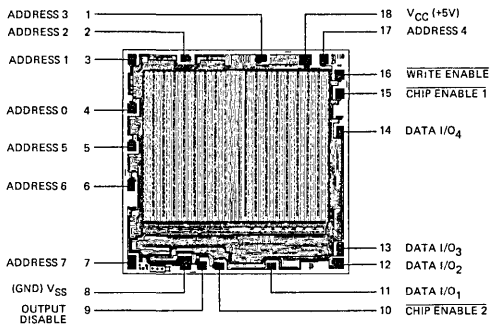
Typical Power Supply Current Versus Voltage



Typical Output Current Versus Voltage

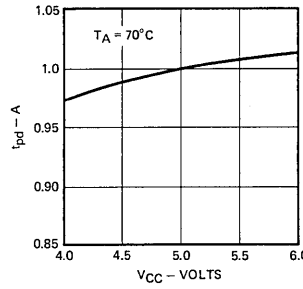


Metallization and Pad Layout

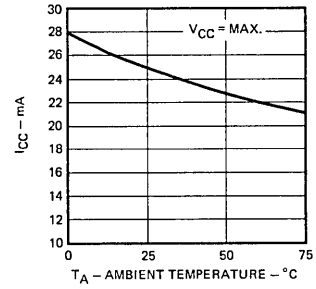


DIE SIZE: 0.132" X 0.131"

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



Typical Power Supply Current Versus Ambient Temperature



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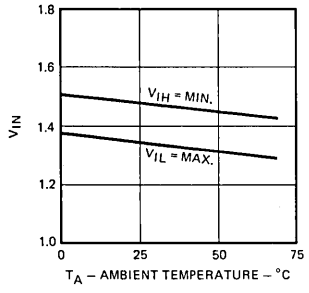
Am9111 FAMILY — APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9111 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

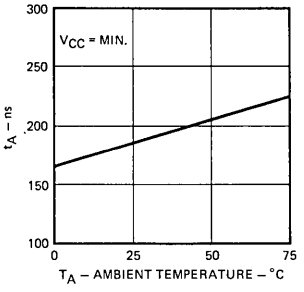
This bussed I/O approach cuts down the package pin count allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9111 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

The Output Disable control signal is provided to prevent signal contention for the bus lines, and to simplify tri-state bus control in the external circuitry. If the chip is enabled and the output is enabled and the memory is in the Read state, then the output buffers will be impressing data on the bus lines. At that point, if the external system tries to drive the bus with data, in preparation for a write operation, there will be conflict for domination of the bus lines. The Output Disable signal allows the user direct control over the output buffers, independent of the state of the memory. Although there are alternative ways to resolve the conflict, normally Output Disable will be held high during a write operation.

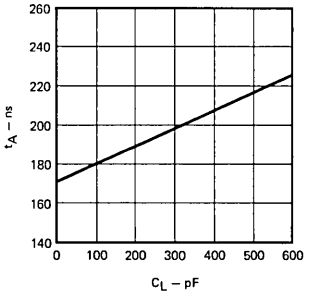
Typical V_{IN} Limits Versus Ambient Temperature



Typical t_A Versus Ambient Temperature



Typical t_A Versus C_L



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ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Power Type	Access Times					
			1000ns	650ns	500ns	400ns	300ns	250ns
0 to +70°C	Molded DIP	Standard	P2111	P2111-2	P2111-1 AM9111APC	AM9111BPC	AM9111CPC	AM9111DPC
		Low			AM91L11APC	AM91L11BPC	AM91L11CPC	
	Hermetic DIP	Standard	C2111	C2111-2	C2111-1 AM9111ADC	AM9111BDC	AM9111CDC	AM9111DDC
		Low			AM91L11ADC	AM91L11BDC	AM91L11CDC	
−55 to +125°C	Hermetic DIP	Standard			AM9111ADM	AM9111BDM	AM9111CDM	
		Low			AM91L11ADM	AM91L11BDM	AM91L11CDM	

Am9112/Am91L12 Family

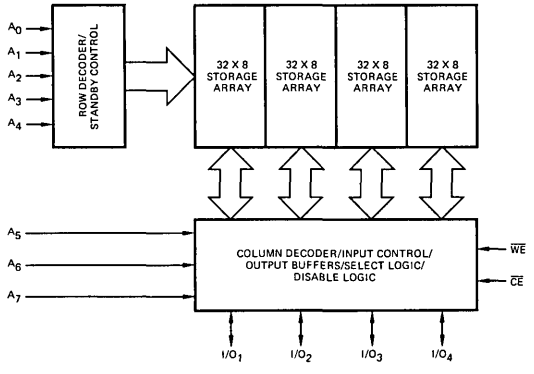
256 x 4 Static R/W Random Access Memories

Part Number	Am2112	Am2112-2	Am9112A Am91L12A	Am9112B Am91L12B	Am9112C Am91L12C	Am9112D
Access Time	1000ns	650ns	500ns	400ns	300ns	250ns

DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization
- 16-pin standard DIP
- Low operating power dissipation
  125mW typ; 290mW maximum – standard power
  100mW typ; 175mW maximum – low power
- DC standby mode reduces power up to 84%
  20mW Typ; 47mW maximum
- Logic voltage levels identical to TTL
- High output drive – two full TTL loads guaranteed
- High noise immunity – full 400mV
- Uniform switching characteristics – access times insensitive to supply variations, address patterns and data patterns
- Single +5V power supply – tolerances ±5% commercial, ±10% military
- Bus-oriented I/O data
- Zero address, setup and hold times guaranteed for simpler timing
- Direct plug-in replacement for 2112 type devices
- 100% MIL-STD-883 reliability assurance testing

Am9112 BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The Am9112/Am91L12 series of products are high performance, low power, 1024-bit, static read/write random access memories. They offer a range of speeds and power dissipations including versions as fast as 200ns and as low as 100mW typical.

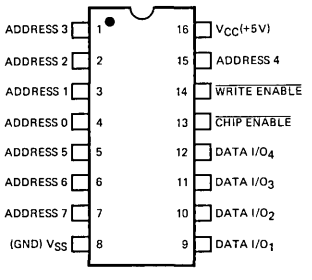
Each memory is implemented as 256 words by 4-bits per word. This organization allows efficient design of small memory systems and permits finer resolution of incremental memory word size relative to 1024 by 1 devices. The output and input data signals are internally bussed together and share 4 common I/O pins. This feature keeps the package size small and provides a simplified interface to bus-oriented systems.

The Am9112/Am91L12 memories may be operated in a DC standby mode for reductions of as much as 84% of the normal operating power dissipation. Though the memory cannot be operated, data can be retained in the storage cells with a power supply as low as 1.5 volts. The Am91L12 versions offer reduced power during normal operating conditions as well as even lower dissipation in standby mode.

The eight Address inputs are decoded to select 1-of-256 locations within the memory. The Chip Enable input acts as a high-order address in multiple chip systems. It also controls the write amplifier and the output buffers in conjunction with the Write Enable input. When $\overline{CE}$ is low and $\overline{WE}$ is high, the write amplifiers are disabled, the output buffers are enabled and the memory will execute a read cycle. When $\overline{CE}$ is low and $\overline{WE}$ is low, the write amplifiers are enabled, the output buffers are disabled and the memory will execute a write cycle. When $\overline{CE}$ is high both the write amplifiers and the output buffers are disabled.

These memories are fully static and require no refresh operations or sense amplifiers or clocks. All input and output voltage levels are identical to standard TTL specifications, including the power supply.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} With Respect to V_{SS}, Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

ELECTRICAL CHARACTERISTICS

Am9112PC, Am9112DC $T_A = 0°C$ to $+70°C$
Am91L12PC, Am91L12DC $V_{CC} = +5V \pm 5\%$

Parameters	Description	Test Conditions			Am9112/ Am91L12 Family Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -200\mu A$			2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., $0V \leq V_{IN} \leq 5.25V$				10	µA
I_{LO}	I/O Leakage Current	$V_{\overline{CE}} = V_{IH}$	$V_{OUT} = V_{CC}$			5.0	µA
			$V_{OUT} = 0.4V$			−10	
I_{CC1}	Power Supply Current	Data out open V_{CC} = MAX. $V_{IN} = V_{CC}$	$T_A = 25°C$	Am9112A/B		50	mA
				Am9112C/D/E		55	
				Am91L12A/B		31	
				Am91L12C		34	
I_{CC2}			$T_A = 0°C$	Am9112A/B		55	
				Am9112C/D/E		60	
				Am91L12A/B		33	
				Am91L12C		36	

ELECTRICAL CHARACTERISTICS

Am9112DM $T_A = -55°C$ to $+125°C$
Am91L12DM $V_{CC} = +5.0V \pm 10\%$

Parameters	Description	Test Conditions			Am9112/ Am91L12 Family Min.	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$		2.4		Volts
			$V_{CC} = 4.50V$		2.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	Volts
V_{IL}	Input LOW Voltage				−0.5	0.8	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., $0V \leq V_{IN} \leq 5.5V$				10	µA
I_{LO}	I/O Leakage Current	$V_{\overline{CE}} = V_{IH}$	$V_{OUT} = V_{CC}$			10	µA
			$V_{OUT} = 0.4V$			−10	
I_{CC1}	Power Supply Current	Data out open V_{CC} = MAX. $V_{IN} = V_{CC}$	$T_A = 25°C$	Am9112A/B		50	mA
				Am9112C		55	
				Am91L12A/B		31	
				Am91L12C		34	
I_{CC3}			$T_A = -55°C$	Am9112A/B		60	
				Am9112C		65	
				Am91L12A/B		37	
				Am91L12C		40	

CAPACITANCE

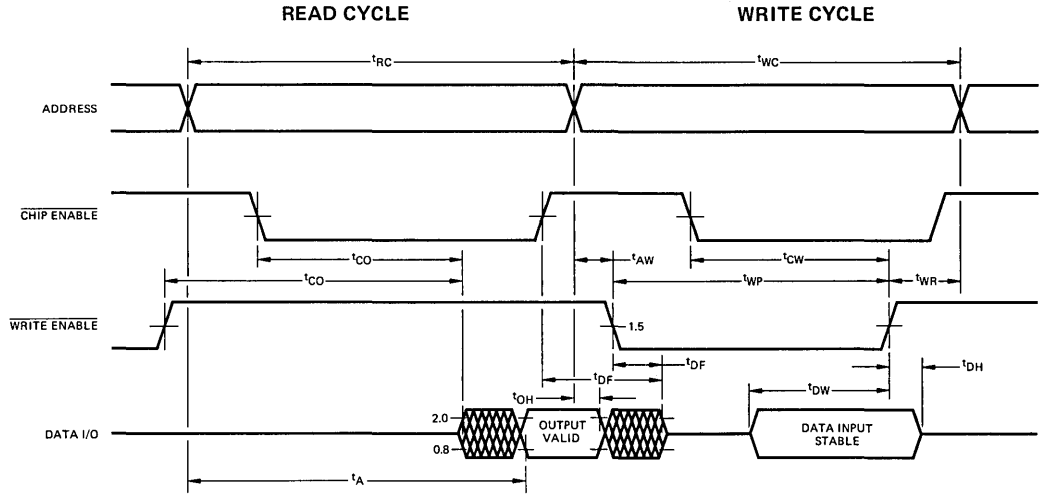
Parameters	Description	Test Conditions		Typ.	Max.	Units
C_{IN}	Input Capacitance, V_{IN} = 0V	$T_A = 25°C$, f = 1 mHz	Am2112	4.0	8.0	pF
			Am9112/Am91L12	3.0	6.0	
C_{OUT}	Output Capacitance, V_{OUT} = 0V		Am2112	10	18	pF
			Am9112/Am91L12	8.0	11	

SWITCHING CHARACTERISTICS over operating temperature and voltage range

Output Load = 1 TTL Gate +100pF
Transition Times = 10ns
Input Levels, Output References = 0.8V and 2.0V

Parameters	Description	Am9112A Am91L12A Min	Am9112A Am91L12A Max	Am9112B Am91L12B Min	Am9112B Am91L12B Max	Am9112C Am91L12C Min	Am9112C Am91L12C Max	Am9112D Min	Am9112D Max	Units
t_{RC}	Read Cycle Time	500		400		300		250		ns
t_A	Access Time		500		400		300		250	ns
t_{CO}	Output Enabled to Output ON Delay (Note 1)	5.0	175	5.0	150	5.0	125	5.0	100	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change	40		40		40		30		ns
t_{DF}	Output Disabled to Output OFF Delay (Note 2)	5.0	125	5.0	100	5.0	100	5.0	75	ns
t_{WC}	Write Cycle Time	500		400		300		250		ns
t_{AW}	Address Set-up Time	0		0		0		0		ns
t_{WR}	Address Hold Time	0		0		0		0		ns
t_{WP}	Write Pulse Width (Note 3)	175		150		125		100		ns
t_{CW}	Chip Enable Set-up Time	175		150		125		100		ns
t_{DW}	Input Data Set-up Time	150		125		100		85		ns
t_{DH}	Input Data Hold Time (Note 4)	0		0		0		0		ns

SWITCHING WAVEFORMS (Note 5)



Notes: 1. Output is enabled and t_{CO} commences only with both $\overline{CE}$ LOW and $\overline{WE}$ HIGH.
2. Output is disabled and t_{DF} defined from either the rising edge of $\overline{CE}$ or the falling edge of $\overline{WE}$.
3. Minimum t_{WP} is valid when $\overline{CE}$ has been HIGH at least t_{DF} before $\overline{WE}$ goes LOW. Otherwise $t_{WP(min.)} = t_{DW(min.)} + t_{DF(max.)}$.
4. When $\overline{WE}$ goes HIGH at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still LOW. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.
5. See "Application Information" section of this specification.

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4

DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE}$ Active LOW Chip Enable. Data can be read from or written into the memory only if $\overline{CE}$ is LOW.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Output Enable Time. The time during which $\overline{CE}$ must be LOW and $\overline{WE}$ must be HIGH prior to data on the output.

t_{OH} Minimum time which will elapse between change of address and any change on the data output.

t_{DF} Time which will elapse between a change on the chip enable or the right enable and on data outputs being driven to a floating status.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

t_{DW} Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

t_{CW} Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

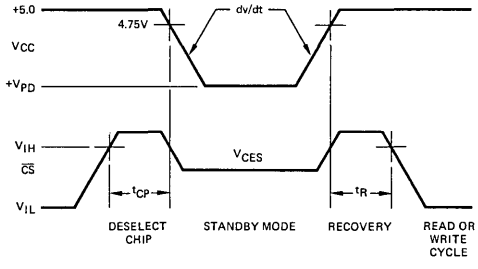
POWER DOWN STANDBY OPERATION

The Am9112/Am91L12 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

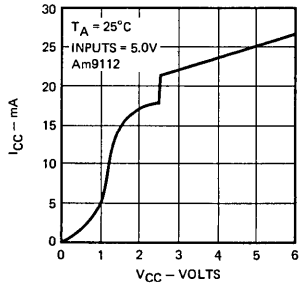
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at V_{IH} or V_{CES} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

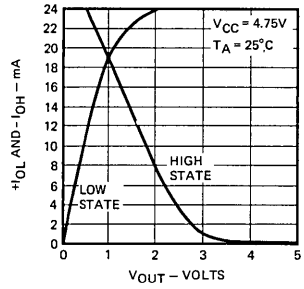
Parameters	Description	Test Conditions			Min.	Typ.	Max.	Units
V_{PD}	V_{CC} in Standby Mode				1.5			
I_{PD}	I_{CC} in Standby Mode	$T_A = 0°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L12		11	25	mA
				Am9112		13	31	
			$V_{PD} = 2.0V$	Am91L12		13	31	
				Am9112		17	41	
		$T_A = -55°C$, All Inputs = V_{PD}	$V_{PD} = 1.5V$	Am91L12		11	28	mA
				Am9112		13	34	
			$V_{PD} = 2.0V$	Am91L12		13	34	
				Am9112		17	46	
dv/dt	Rate of Change of V_{CC}						1.0	V/μs
t_R	Standby Recovery Time				t_{RC}			ns
t_{CP}	Chip Deselect Time				0			ns
V_{CES}	$\overline{CE}$ Bias in Standby				V_{PD}			Volts



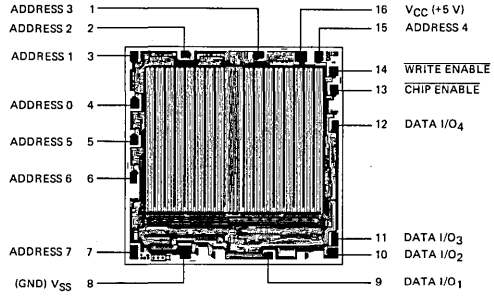
Typical Power Supply Current Versus Voltage



Typical Output Current Versus Voltage

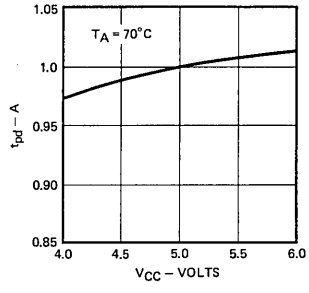


Metallization and Pad Layout

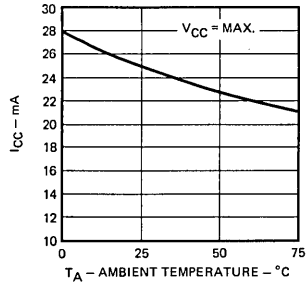


DIE SIZE 0.132" X 0.131"

Access Time Versus V_{CC} Normalized to V_{CC} = +5.0 Volts



Typical Power Supply Current Versus Ambient Temperature



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APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9112 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

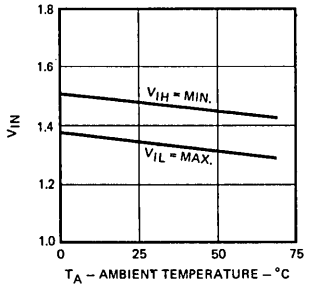
This bussed I/O approach keeps the package pin count low allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9112 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

If the chip is enabled ($\overline{CE}$ low) and the memory is in the Read state ($\overline{WE}$ high), the output buffers will be turned on and will be driving data on the I/O bus lines. If the external system tries to drive the bus with data, there may be contention for control of the data lines and large current surges can result. Since the condition can occur at the beginning of a write cycle, it is important that incoming data to be written not be entered until the output buffers have been turned off.

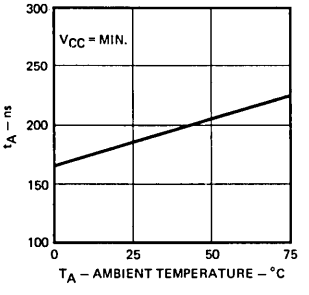
These operational suggestions for write cycles may be of some help for memory system designs:

1. For systems where $\overline{CE}$ is always low or is derived directly from addresses and so is low for the whole cycle, make sure t_{WP} is at least $t_{DW} + t_{DF}$ and delay the input data until t_{DF} following the falling edge of $\overline{WE}$. With zero address set-up and hold times it will often be convenient to make $\overline{WE}$ a cycle-width level ($t_{WP} = t_{WC}$) so that the only subcycle timing required is the delay of the input data.
2. For systems where $\overline{CE}$ is high for at least t_{DF} preceeding the falling edge of $\overline{WE}$, t_{WP} may assume the minimum specified value. When $\overline{CE}$ is high for t_{DF} before the start of the cycle, then no other subcycle timing is required and $\overline{WE}$ and data-in may be cycle-width levels.
3. Notice that because both $\overline{CE}$ and $\overline{WE}$ must be low to cause a write to take place, either signal can be used to determine the effective write pulse. Thus, $\overline{WE}$ could be a level with $\overline{CE}$ becoming the write timing signal. In such a case, the data set-up and hold times are specified with respect to the rising edge of $\overline{CE}$. The value of the data set-up time remains the same and the value of the data hold time should change to a minimum of 25ns.

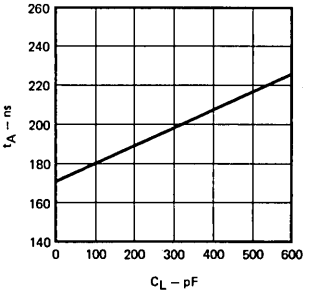
Typical V_{IN} Limits Versus Ambient Temperature



Typical t_A Versus Ambient Temperature



Typical t_A Versus C_L



MOS-360

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Power Type	Access Times					
			1000ns	650ns	500ns	400ns	300ns	250ns
0 to +70°C	Molded DIP	Standard	P2112	P2112-2	AM9112APC	AM9112BPC	AM9112CPC	AM9112DPC
		Low			AM91L12APC	AM91L12BPC	AM91L12CPC	
	Hermetic DIP	Standard	C2112	C2112-2	AM9112ADC	AM9112BDC	AM9112CDC	AM9112DDC
		Low			AM91L12ADC	AM91L12BDC	AM91L12CDC	
−55 to +125°C	Hermetic DIP	Standard			AM9112ADM	AM9112BDM	AM9112CDM	
		Low			AM91L12ADM	AM91L12BDM	AM91L12CDM	

Am9122/Am91L22

256 x 4 Static R/W RAMs

DISTINCTIVE CHARACTERISTICS

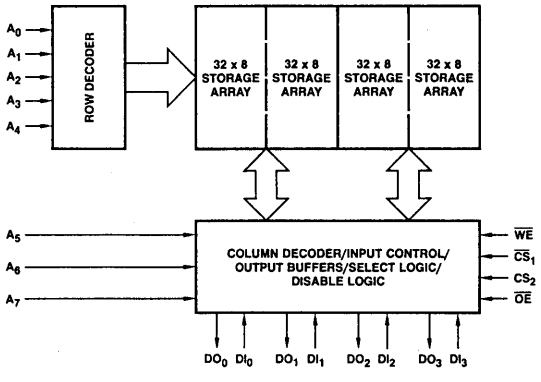
- High performance replacement for 93422/93L422
- 256 x 4 organization for small memory systems
- Fast access times – down to 25ns (Commercial)
  – down to 35ns (Military)
- Low operating power dissipation
  - Standard power: 660mW (Commercial)
    745mW (Military)
  - Low power: 248/440mW (Commercial)
    495mW (Military)
- Single 5 volt power supply – ±10% tolerance both commercial and military
- 100% MIL-STD-883 reliability assurance testing
- Guaranteed 0.1% AQL

FUNCTIONAL DESCRIPTION

The Am9122/Am91L22 series is a MOS pin-for-pin and functional replacement for the 93422/93L422 bipolar memories. These devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 25ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

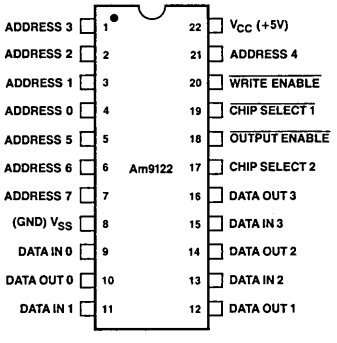
The Am9122/91L22 employs an output enable and two chip enable inputs to give the user better data control. High noise immunity, high output drive (4 TTL loads) and TTL logic voltage levels allow easy conversion from bipolar to MOS. 10% power supply tolerances give better margins in the memory system. As with all AMD MOS RAMs, the Am9122/91L22 is guaranteed to 0.1% AQL.

Am9122 BLOCK DIAGRAM



RAM-019

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

RAM-020

SELECTION GUIDE

		Am9122-25	Am9122-35	Am91L22-35	Am91L22-45	Am91L22-60
Maximum Access Time (ns)		25	35	35	45	60
Maximum Operating Current (mA)	0 to 70°C	120	120	80	80	45
	–55 to 125°C	N/A	135	N/A	90	N/A

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 10 to Pin 9) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs	−0.5 to +7.0V
DC Input Voltage	−0.5 to +7.0V
Power Dissipation	1.0W
DC Output Current	20mA

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}
Am9122 DC/PC Am91L22 DC/PC	$0°C \leq T_A \leq +70°C$	+5.0V ± 10%
Am9122 DM Am91L22 DM	$-55°C \leq T_A \leq +125°C$	+5.0V ± 10%

ELECTRICAL CHARACTERISTICS over the operating temperature range unless otherwise specified (Note 1)

Parameters	Description	Test Conditions		Am91L22-60 Min	Am91L22-60 Max	Am91L22-35 Am91L22-45 Min	Am91L22-35 Am91L22-45 Max	Am9122-25 Am9122-35 Min	Am9122-25 Am9122-35 Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = −5.2mA	2.4		2.4		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 8.0mA		0.4		0.4		0.4	Volts
V_{IH}	Input HIGH Voltage			2.1	V_{CC}	2.1	V_{CC}	2.1	V_{CC}	Volts
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = Gnd			10		10		10	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = V_{CC}			10		10		10	μA
V_{CD}	Input Diode Clamp Voltage				Note 4		Note 4		Note 4	Volts
I_{OFF}	Output Current (High-Z)	$V_{OL} \leq V_{OUT} \leq V_{OH}$ Output Disabled	T_A = Max	−50	50	−50	50	−50	50	μA
I_{OS}	Output Short Circuit Current Note 3	V_{CC} = Max, V_{OUT} = GND	Commercial		−70		−70		−70	mA
			Military		−80		−80		−80	mA
I_{CC}	Power Supply Current	V_{CC} = Max, I_{OUT} = 0mA	T_A = 70°C		40		70		110	mA
			T_A = 0°C		45		80		120	mA
			T_A = −55°C		N/A		90		135	mA

CAPACITANCE

Parameters	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance, V_{IN} = 0V	T_A = 25°C, f = 1MHz V_{CC} = 4.5V	3	5	pF
C_{OUT}	Output Capacitance, V_{OUT} = 0V		5	8	

Notes:
1. The temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. A two minute warm up period is required for −55°C operation.
2. t_w measured at t_{wsa} = min; t_{wsa} measured at t_w = min.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. The NMOS process does not provide a clamp diode. However, the Am9122/91L22 is insensitive to −3V DC input levels and −5V undershoot pulses of less than 10ns (measured at 50% point).
5. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30pF load capacitance as in Figure 1a.
6. Transition is measured at V_{OH} −500mV or V_{OL} +500mV levels on the output from 1.5V level on the input with load shown in Figure 1b.

SWITCHING CHARACTERISTICS over operating and voltage range (Note 5)

Parameters	Description	Test Conditions	Am9122-25 Min	Am9122-25 Max	Am91L22-35 Am9122-35 Min	Am91L22-35 Am9122-35 Max	Am91L22-45 Min	Am91L22-45 Max	Am91L22-60 Min	Am91L22-60 Max	Units
t_{ACS}	Chip Select Time			15		25		30		35	ns
t_{ZRCS}	Chip Select to High-Z	(Note 6)		20		30		30		35	ns
t_{AOS}	Output Enable Time			15		25		30		35	ns
t_{ZROS}	Output Enable to High-Z	(Note 6)		20		30		30		35	ns
t_{AA}	Address Access Time			25		35		45		60	ns
t_{ZWS}	Write Disable to High-Z	(Note 6)		20		30		35		40	ns
t_{WR}	Write Recovery Time			20		25		40		45	ns
t_W	Write Pulse Width	(Note 2)	15		25		30		40		ns
t_{WSD}	Data Setup Time Prior to Write		5		5		5		5		ns
t_{WHD}	Data Hold Time After Write		5		5		5		5		ns
t_{WSA}	Address Setup Time	(Note 2)	5		5		10		10		ns
t_{WHA}	Address Hold Time		5		5		5		5		ns
t_{WSCS}	Chip Select Setup Time		5		5		5		5		ns
t_{WHCS}	Chip Select Hold Time		5		5		5		5		ns

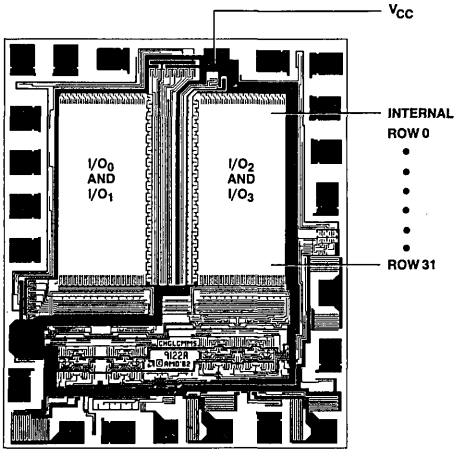
LOGIC TABLE

Inputs					Outputs	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	D_0-D_3		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	O_0-O_3	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled
H	L	H	L	L	High Z	Write "0" (Output Disabled)
H	L	H	L	H	High Z	Write "1" (Output Disabled)

Notes: H = HIGH Voltage
L = LOW Voltage
X = Don't Care (HIGH or LOW)
High Z = High Impedance

BIT MAP

Address Designators	
External	Internal
A_0	A_0
A_1	A_1
A_2	A_2
A_3	A_3
A_4	A_4
A_5	A_5
A_6	A_6
A_7	A_7



AC TEST LOADS AND WAVEFORMS

AC TEST LOADS

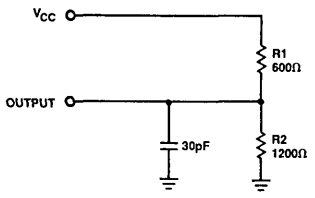


Figure 1a.

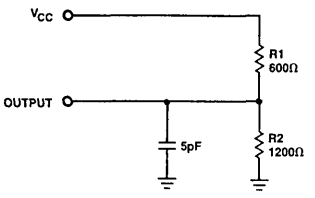


Figure 1b.

INPUT PULSES

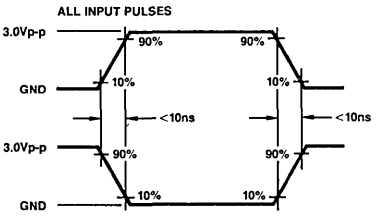
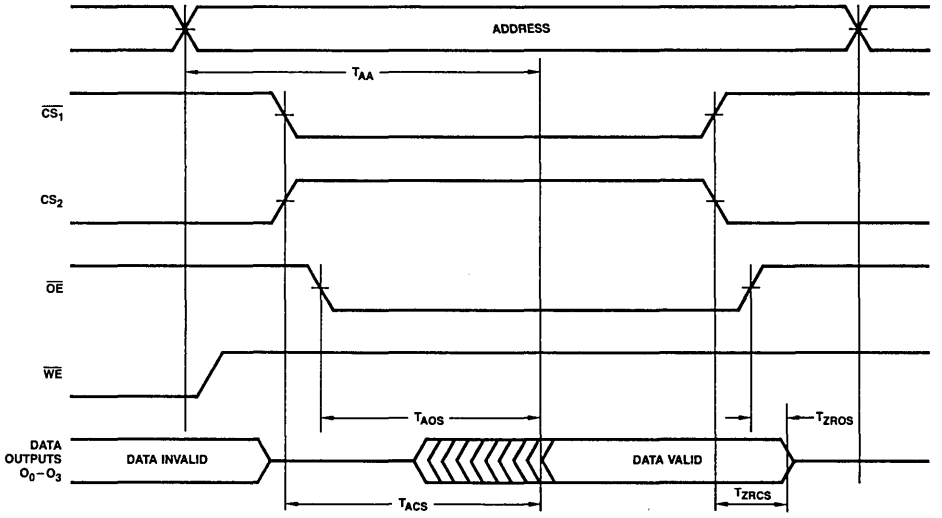


Figure 2.

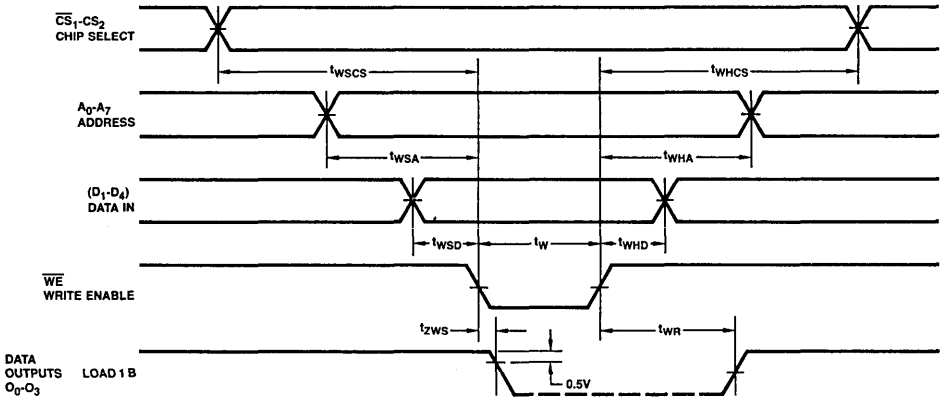
RAM-021

READ MODE



RAM-022

WRITE MODE



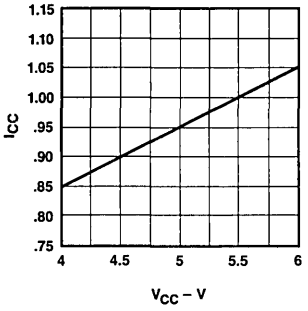
RAM-023

(All above measurements implemented to 1.5V unless otherwise stated.)

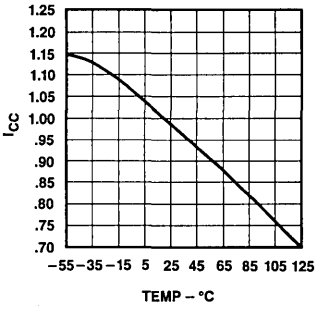
Note: Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed to in various applications as long as the worst case limits are not violated.

TYPICAL DC AND AC CHARACTERISTICS

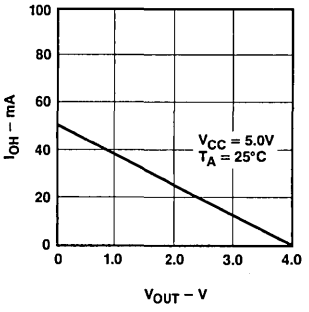
Normalized ICC versus Supply Voltage



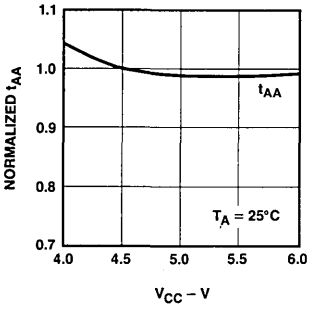
Normalized ICC versus Ambient Temperature



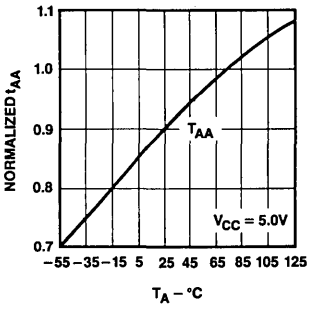
Output Source Current versus Output Voltage



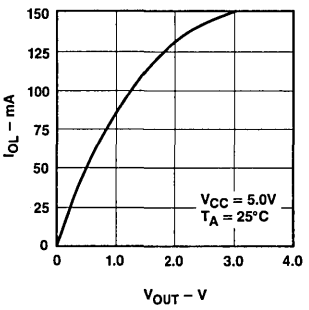
Normalized Access Time versus Supply Voltage



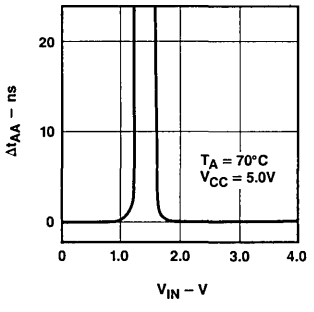
Normalized Access Time versus Ambient Temperature



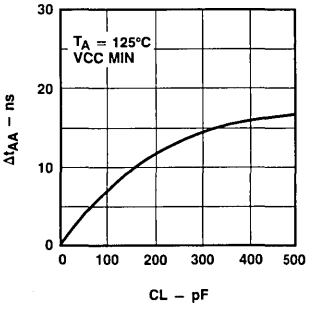
Output Sink Current versus Output Voltage



Access Time Change versus Input Voltage



Access Time Change versus Output Loading



RAM-024

ORDERING INFORMATION

9122-25 Order Code	9122-35 Order Code	91L22-35 Order Code	91L22-45 Order Code	91L22-60 Order Code	Package Type	Screening Level	Operating Range
Am9122-25PC	Am9122-35PC	Am91L22-35PC	Am91L22-45PC	Am91L22-60PC	P-22	C-1	C
Am9122-25DC	Am9122-35DC	Am91L22-35DC	Am91L22-45DC	Am91L22-60DC	D-22	C-1	C
N/A	Am9122-35DM	N/A	Am91L22-45DM	N/A	D-22	C-3	M

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pack. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
3. See Operating Range Table.

Am21L41

4096 x 1 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- 4K x 1 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Equal access and cycle times
- Automatic power-down when deselected
- Low power dissipation
  - Am21L41; 220mW active, 27.5mW power down
- Standard 18-pin, .300 inch dual in-line package
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- 100% MIL-STD-883 reliability assurance testing
- No power-on current surge
- Guaranteed 0.1% AQL

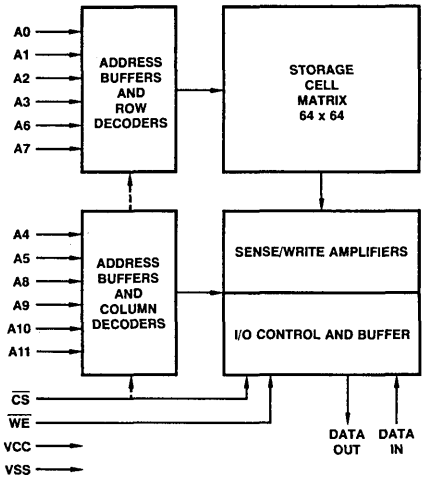
GENERAL DESCRIPTION

The Am21L41 is a high performance, 4096-bit, static, read/write, random access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard Schottky TTL loads or up to six standard TTL loads.

Only a single +5 volt power supply is required. When deselected ($\overline{CS} \geq VIH$), the Am21L41 automatically enters a power-down mode which reduces power dissipation by as much as 85%. When selected, the chip powers up again with no access time penalty.

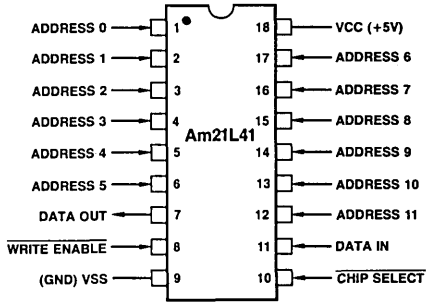
Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a 3-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

BLOCK DIAGRAM



RAM-037

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

RAM-038

PRODUCT SELECTIONS

	Am21L41-12	Am21L41-15	Am21L41-20	Am21L41-25
Max Access Time (ns)	120	150	200	250
Max Active Current (mA)	55	40	40	40
Max Standby Current (mA)	10	5	5	5

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	0 to 70°C
VCC with Respect to VSS	−0.5 to +7.0V
All Signal Voltages with Respect to VSS	−1.5 to +7.0V
Power Dissipation (Package Limitation)	1.2W
DC Output Current	20mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VSS	VCC
Am21L41 PC/DC	0°C ≤ T_A ≤ +70°C	0V	+5.0V ± 10%

ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameter	Description	Test Conditions		Am21L41-12 Min	Am21L41-12 Max	Am21L41-15 Am21L41-20 Am21L41-25 Min	Am21L41-15 Am21L41-20 Am21L41-25 Max	Units
IOH	Output High Current	VOH = 2.4V	VCC = 4.5V	−4		−4		mA
IOL	Output Low Current	VOL = 0.4V	T_A = 70°C	8		8		mA
VIH	Input High Voltage			2.0	6.0	2.0	6.0	Volts
VIL	Input Low Voltage			−3.0	0.8	−3.0	0.8	Volts
IIX	Input Load Current	VSS ≤ VI ≤ VCC			10		10	μA
IOZ	Output Leakage Current	GND ≤ VO ≤ VCC Output Disabled	T_A = 70°C	−10	10	−10	10	μA
IOS	Output Short Circuit Current	GND ≤ VO ≤ VCC (Note 2)	0 to +70°C	−120	120	−120	120	mA
CI	Input Capacitance (Note 1)	Test Frequency = 1.0MHz T_A = 25°C, All pins at 0V			5.0		5.0	pF
CO	Output Capacitance (Note 1)				6.0		6.0	
ICC	VCC Operating Supply Current	Max VCC, $\overline{CS}$ ≤ VIL	T_A = 0°C		55		40	mA
ISB	Automatic $\overline{CS}$ Power Down Current	Max VCC, ($\overline{CS}$ ≥ VIH) (Note 5)			10		5.0	mA

Notes:
1. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
2. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.5V and output loading of the specified IOL/IOH and C_L = 30pF load capacitance (reference Figure 1.).
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. A pull up resistor to VCC on the $\overline{CS}$ input is required to keep the device deselected during VCC power up otherwise ISB will exceed values given.
6. Chip deselected greater than 55ns prior to selection.
7. Chip deselected less than 55ns prior to selection.
8. At any given temperature and voltage condition, tHZ is less than tLZ for all devices. Transition is measured at VOH −500mV and VOL +500mV levels on the output from 1.5V level on the input with load shown in Figure 1 using CL = 5pF.
9. $\overline{WE}$ is high for read cycle.
10. Device is continuously selected, $\overline{CS}$ = VIL.
11. Address valid prior to or coincident with $\overline{CS}$ transition low.

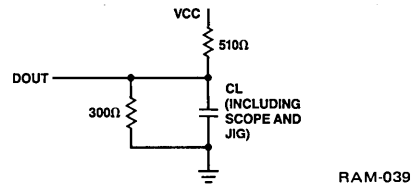


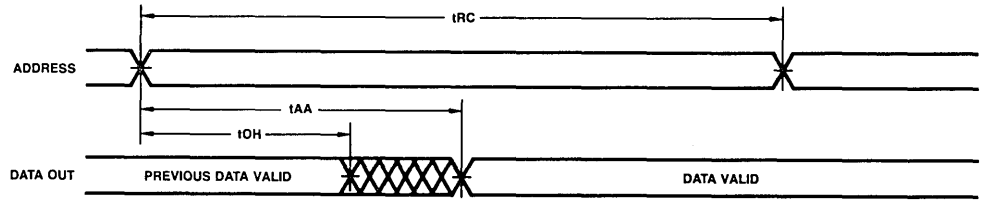
Figure 1. Output Load

SWITCHING CHARACTERISTICS over operating range (Note 3)

Parameter	Description		Am21L41-12 Min	Am21L41-12 Max	Am21L41-15 Min	Am21L41-15 Max	Am21L41-20 Min	Am21L41-20 Max	Am21L41-25 Min	Am21L41-25 Max	Units
Read Cycle											
tRC	Address Valid to Address Do Not Care Time (Read Cycle Time)		120		150		200		250		ns
tAA	Address Valid to Data Out Valid Delay (Address Access Time)			120		150		200		250	ns
tASC1	Chip Select Low to Data Out Valid	Note 6		120		150		200		250	ns
tASC2		Note 7		130		160		200		250	ns
tLZ	Chip Select Low to Data Out On	Note 8	10		10		10		10		ns
tHZ	Chip Select High to Data Out Off	Note 8	0	60	0	60	0	60	0	60	ns
tOH	Address Unknown to Data Out Unknown Time		10		10		10		10		ns
tPD	Chip Select High to Power Low Delay			60		60		60		60	ns
tPU	Chip Select Low to Power High Delay		0		0		0		0		ns
Write Cycle											
tWC	Address Valid to Address Do Not Care Time (Write Cycle Time)		120		150		200		250		ns
tWP	Write Enable Low to Write Enable High Time	Note 4	60		60		60		75		ns
tWR	Write Enable High to Address Do Not Care Time		10		15		20		20		ns
tWZ	Write Enable Low to Data Out Off Delay	Note 8	0	70	0	80	0	80	0	80	ns
tDW	Data in Valid to Write Enable High Time		50		60		60		75		ns
tDH	Write Enable Low to Data In Do Not Care Time		10		10		10		10		ns
tAS	Address Valid to Write Enable Low Time		0		0		0		0		ns
tCW	Chip Select Low to Write Enable High Time	Note 4	110		135		180		230		ns
tOW	Write Enable High to Output Turn On	Note 8	0		0		0		0		ns
tAW	Address Valid to End of Write		110		135		180		230		ns

SWITCHING WAVEFORMS

READ CYCLE NO. 1 (Notes 9, 10)



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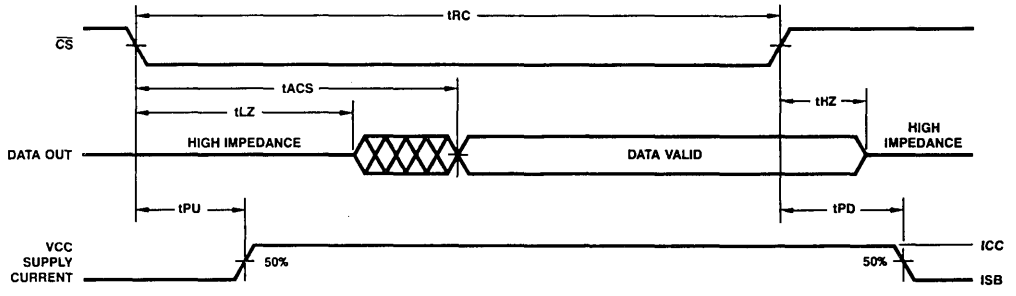
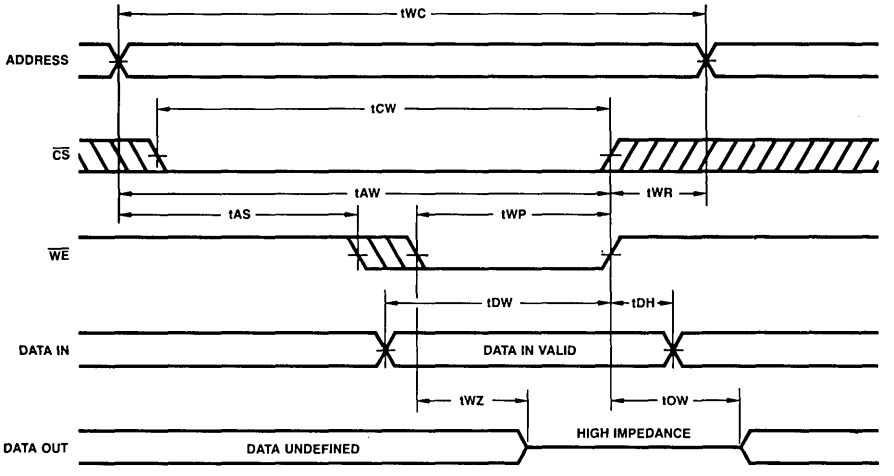
READ CYCLE NO. 2 (Notes 9, 11)



RAM-041

SWITCHING WAVEFORMS (Cont.)

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



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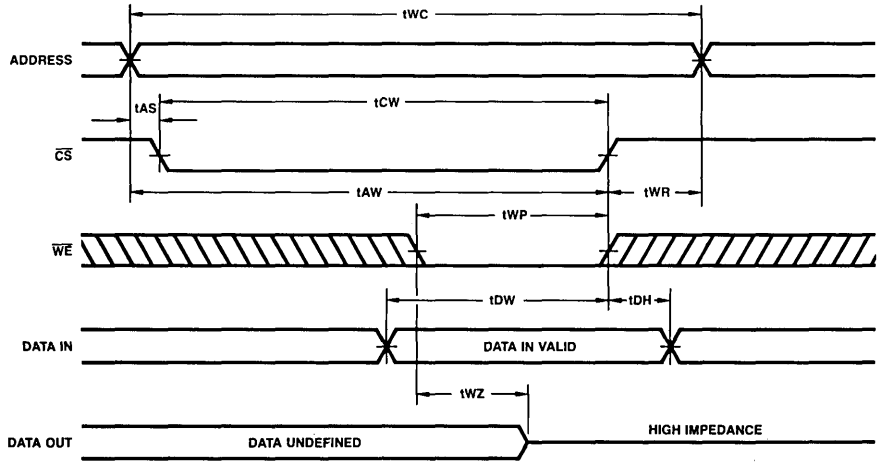
WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)

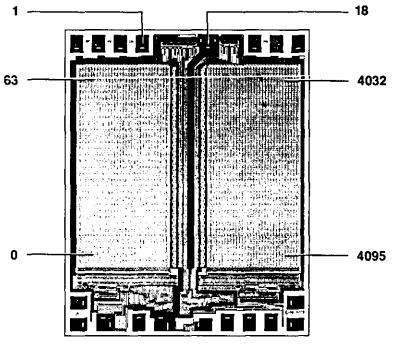


Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

RAM-043

BIT MAP

Address Designators	
External	Internal
A0	A2
A1	A5
A2	A4
A3	A3
A4	A8
A5	A7
A6	A1
A7	A0
A8	A11
A9	A9
A10	A10
A11	A6



DIE SIZE:
0.130 X 0.106

Figure 2. Bit Mapping Information

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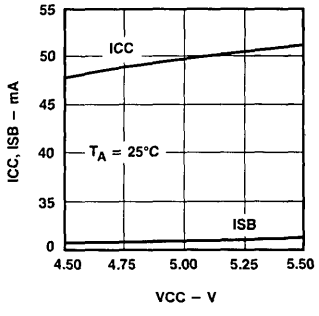
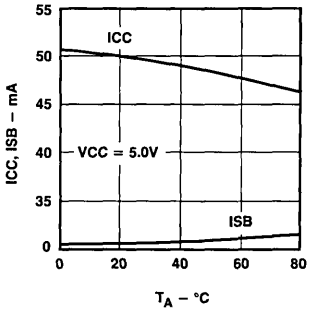
TYPICAL DC AND AC CHARACTERISTICS

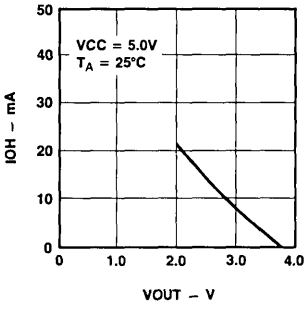
Supply Current Versus Supply Voltage



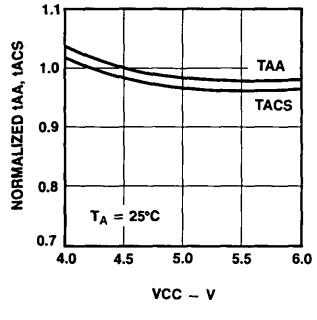
Supply Current Versus Ambient Temperature



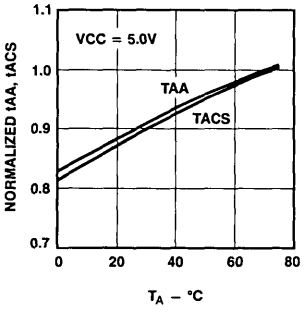
Output Source Current Versus Output Voltage



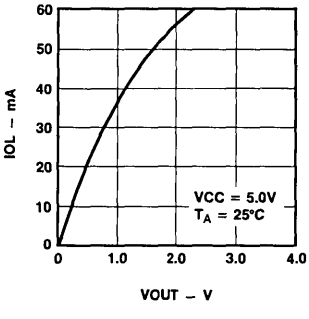
Normalized Access Time Versus Supply Voltage



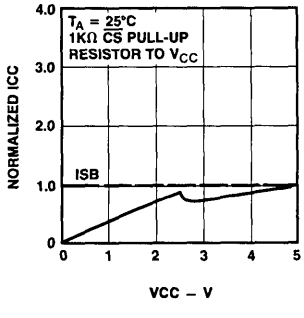
Normalized Access Time Versus Ambient Temperature



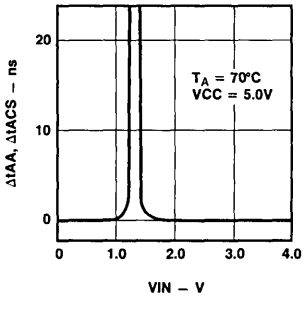
Output Sink Current Versus Output Voltage



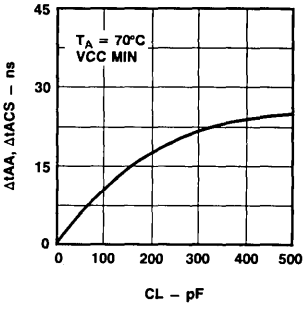
Typical Power-On Current Versus Power Supply



Access Time Change Versus Input Voltage



Access Time Change Versus Output Loading



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4

ORDERING INFORMATION

Am21L41-12 Order Code	Am21L41-15 Order Code	Am21L41-20 Order Code	Am21L41-25 Order Code	Package Type	Screening Level	Operating Range
Am21L41-12PC	Am21L41-15PC	Am21L41-20PC	Am21L41-25PC	P-18-1	C-1	C
Am21L41-12DC	Am21L41-15DC	Am21L41-20DC	Am21L41-25DC	D-18-1	C-1	C

Notes: 1. P = Molded DIP, D = Hermetic DIP. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
3. See Operating Range Table.

Am9044 • Am9244

4096 x 1 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- **LOW OPERATING POWER (MAX)**
  Am9044/Am9244 385mW (70mA)
  Am90L44/Am92L44 275mW (50mA)
- **LOW STANDBY POWER (MAX)**
  Am92L44 110mW (20mA)
- Access times down to 200ns (max)
- Military temperature range available to 250ns (max)
- Am9044 is a direct plug-in replacement for 4044
- Am9244 pin and function compatible with Am9044 and 4044 plus $\overline{CS}$ power down feature
- Fully static – no clocking
- Identical access and cycle time
- High output drive – 4.0mA sink current @ 0.4V
- TTL identical interface logic levels
- 100% MIL-STD-883 reliability assurance testing

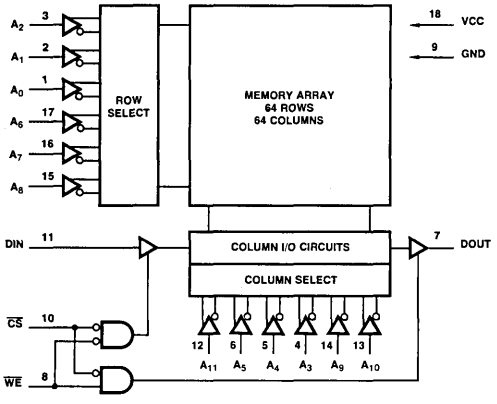
GENERAL DESCRIPTION

The Am9044 and Am9244 are high performance, static, N-Channel, read/write, random access memories organized as 4096 x 1. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of about 30%. The Am9044 and Am9244 are the same except that the Am9244 offers an automatic $\overline{CS}$ power down feature.

The Am9244 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am9244 power decreases from 385mW to 165mW in the standby mode, and the Am92L44 from 275mW to 110mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9044.

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9244 and Am9044 provide increased short circuit current for improved drive.

BLOCK DIAGRAM



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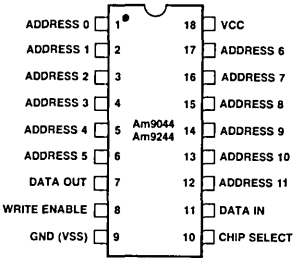
CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

MOS-257

ORDERING INFORMATION

Ambient Temperature	Package Type	ICC Current Level	Access Times							
			Am9044				Am9244			
			450ns	300ns	250ns	200ns	450ns	300ns	250ns	200ns
0°C ≤ T_A ≤ +70°C	Plastic	70mA	AM9044BPC	AM9044CPC	AM9044DPC	AM9044EPC	AM9244BPC	AM9244CPC	AM9244DPC	AM9244EPC
		50mA	AM90L44BPC	AM90L44CPC	AM90L44DPC		AM92L44BPC	AM92L44CPC	AM92L44DPC	
	Hermetic	70mA	AM9044BDC	AM9044CDC	AM9044DDC	AM9044EDC	AM9244BDC	AM9244CDC	AM9244DDC	AM9244EDC
		50mA	AM90L44BDC	AM90L44CDC	AM90L44DDC		AM92L44BDC	AM92L44CDC	AM92L44DDC	
−55°C ≤ T_A ≤ +125°C	Hermetic	90mA	AM9044BDM	AM9044CDM	AM9044DDM		AM9244BDM	AM9244CDM	AM9244DDM	
		60mA	AM90L44BDM	AM90L44CDM			AM92L44BDM	AM92L44CDM		

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	−0.5V to +7.0V
All Signal Voltages with Respect to VSS	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.0W
DC Output Current	10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VSS	VCC	Part Number	Ambient Temperature	VSS	VCC
Am9044DC/PC Am90L44DC/PC Am9244DC/PC Am92L44DC/PC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ±10%	Am9044DM Am90L44DM Am9244DM Am92L44DM	$-55°C \leq T_A \leq +125°C$	0V	+5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions			Am9244XX Am92L44XX Min.	Am9244XX Am92L44XX Typ.	Am9244XX Am92L44XX Max.	Am9044XX Am90L44XX Min.	Am9044XX Am90L44XX Typ.	Am9044XX Am90L44XX Max.	Units
IOH	Output High Current	VOH = 2.4V	VCC = 4.5V	70°C	−1.0			−1.0			mA
		VOH = 2.4V	VCC = 4.5V	125°C	−.4			−.4			
IOL	Output Low Current	VOL = 0.4V	$T_A = +70°C$		4.0			4.0			mA
			$T_A = +125°C$		3.2			3.2			
VIH	Input High Voltage				2.0		VCC	2.0		VCC	Volts
VIL	Input Low Voltage				−0.5		0.8	−0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ VI ≤ VCC					10			10	μA
IOZ	Output Leakage Current	0.4V ≤ VO ≤ VCC Output Disabled	$T_A = +125°C$		−50		50	−50		50	μA
			$T_A = +70°C$		−10		10	−10		10	
CI	Input Capacitance (Note 1)	Test Frequency = 1.0MHz $T_A = 25°C$, All pins at 0V				3.0	5.0		3.0	5.0	pF
CI/O	I/O Capacitance (Note 1)					5.0	6.0		5.0	6.0	

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am92L44 Typ.	Am92L44 Max.	Am9244 Typ.	Am9244 Max.	Am90L44 Typ.	Am90L44 Max.	Am9044 Typ.	Am9044 Max.	Units
ICC	VCC Operating Supply Current	Max. VCC $\overline{CS} \leq$ VIL for Am9244/92L44	$T_A = 0°C$		50		70		50		70	mA
			$T_A = -55°C$		60		80		60		80	
IPD	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC} ($\overline{CS} \geq V_{IH}$)	$T_A = 0°C$		20		30		–		–	mA
			$T_A = -55°C$		22		33		–		–	

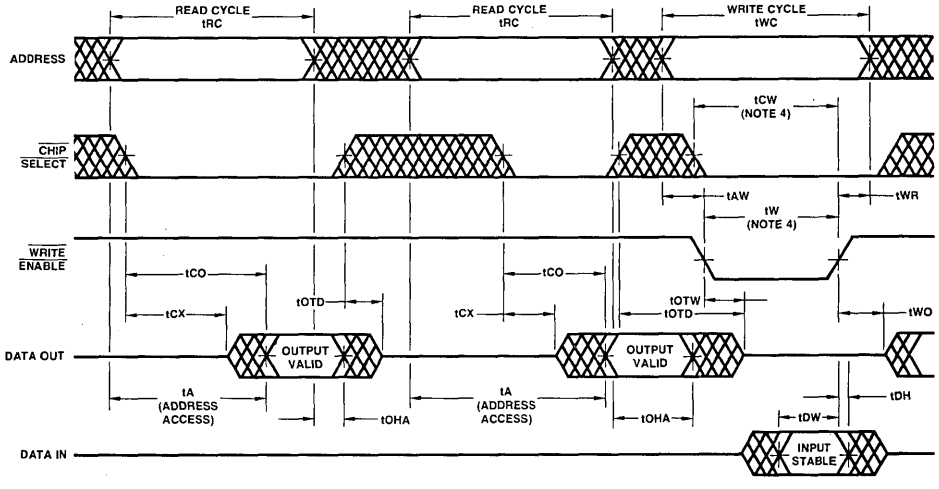
Notes:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time (t_{CO}) is longer for the Am9244 than for the Am9044. The specified address access time will be valid only when Chip Select is low soon enough for t_{CO} to elapse.

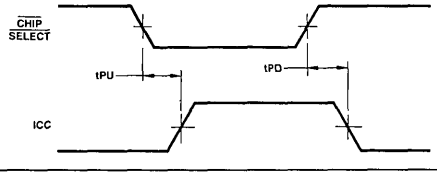
SWITCHING CHARACTERISTICS over operating range (Note 3)

Parameter	Description		Am9044B Am9244B Min.	Am9044B Am9244B Max.	Am9044C Am9244C Min.	Am9044C Am9244C Max.	Am9044D Am9244D Min.	Am9044D Am9244D Max.	Am9044E Am9244E Min.	Am9044E Am9244E Max.	Units
Read Cycle											
tRC	Address Valid to Address Do Not Care Time (Read Cycle Time)		450		300		250		200		ns
tA	Address Valid to Data Out Valid Delay (Address Access Time)			450		300		250		200	ns
tCO	Chip Select Low to Data Out Valid (Note 5)	Am9044		100		100		70		70	ns
		Am9244		450		300		250		200	ns
tCX	Chip Select Low to Data Out On		20		20		20		20		ns
tOTD	Chip Select High to Data Out Off			100		80		60		60	ns
tOHA	Address Unknown to Data Out Unknown Time		20		20		20		20		ns
Write Cycle											
tWC	Address Valid to Address Do Not Care Time (Write Cycle Time)		450		300		250		200		ns
tW	Write Enable Low to Write Enable High Time (Note 4)	Am9044	200		150		100		100		ns
		Am9244	250		200		150		150		ns
tWR	Write Enable High to Address Do Not Care Time		0		0		0		0		ns
tOTW	Write Enable Low to Data Out Off Delay			100		80		60		60	ns
tDW	Data In Valid to Write Enable High Time		200		150		100		100		ns
tDH	Write Enable Low to Data In Do Not Care Time		0		0		0		0		ns
tAW	Address Valid to Write Enable Low Time		0		0		0		0		ns
tPD	Chip Select High to Power Low Delay (Am9244 only)			200		150		100		100	ns
tPU	Chip Select Low to Power High Delay (Am9244 only)		0		0		0		0		ns
tCW	Chip Select Low to Write Enable High Time (Note 4)	Am9044	200		150		100		100		ns
		Am9244	250		200		150		150		ns
tWO	Write Enable High To Output Turn On			100		100		70		70	ns

SWITCHING WAVEFORMS



POWER DOWN WAVEFORM (Am9244 ONLY)



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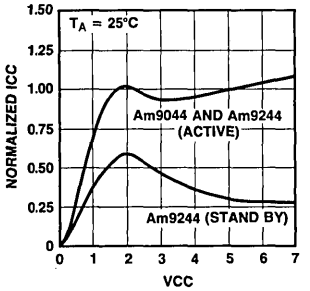
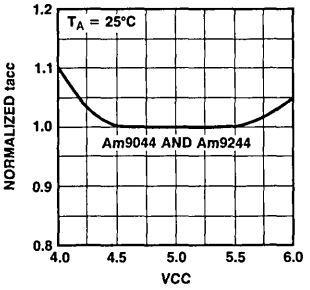
TYPICAL CHARACTERISTICS

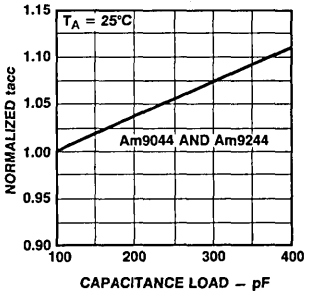
Typical ICC
Versus VCC Characteristics



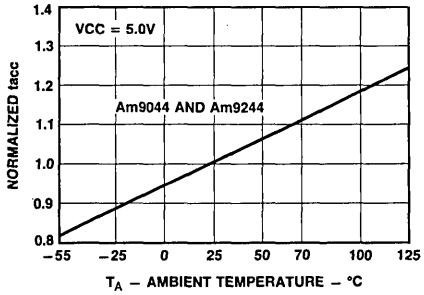
Typical tacc
Versus VCC Characteristics



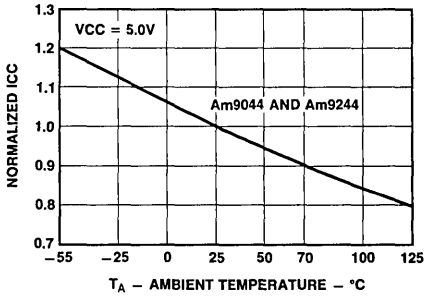
Typical C Load Versus
Normalized tacc Characteristics



Normalized tacc
Versus Ambient Temperature



Normalized ICC
Versus Ambient Temperature



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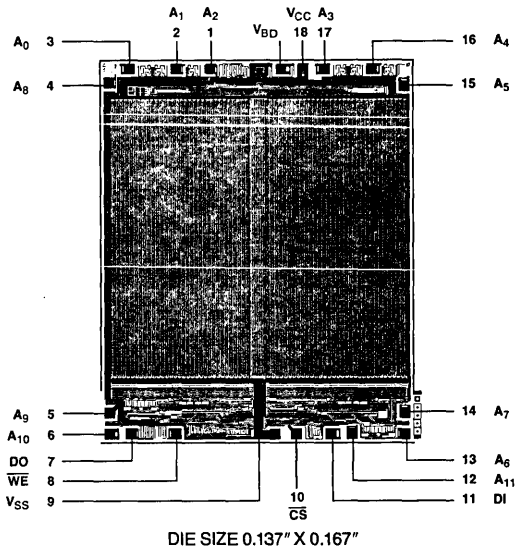
BIT MAP



DIE SIZE 0.137″ X 0.167″

Address Designators	
External	Internal
A0	A2
A1	A1
A2	A0
A3	A8
A4	A9
A5	A10
A6	A3
A7	A4
A8	A5
A9	A7
A10	A6
A11	A11

Figure 1. Bit Mapping Information.

Am9114 • Am9124

1024 x 4 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- **LOW OPERATING POWER (MAX)**
  Am9124/Am9114 368mW (70mA)
  Am91L24/Am91L14 262mW (50mA)
- **LOW STANDBY POWER (MAX)**
  Am9124 158mW (30mA)
  Am91L24 105mW (20mA)
- Access times down to 150ns (max)
- Military temperature range available to 300ns (max)
- Am9114 is a direct plug-in replacement for 2114
- Am9124 pin and function compatible with Am9114 and 2114, plus $\overline{CS}$ power down feature
- Fully static – no clocking
- Identical access and cycle time
- High output drive –
  4.0mA sink current @ 0.4V – 9124
  3.2mA sink current @ 0.4V – 9114
- TTL identical input/output levels
- 100% MIL-STD-883 reliability assurance testing
- Guaranteed 0.1% AQL

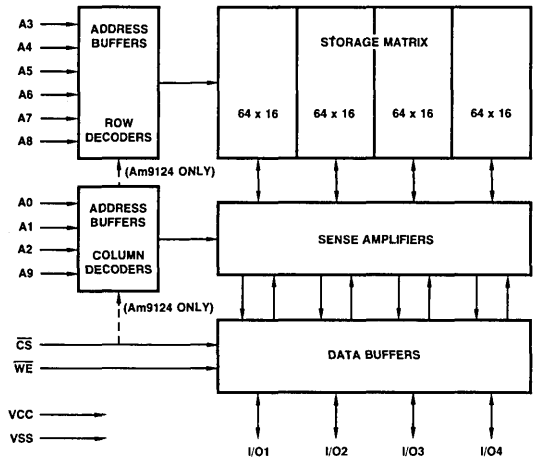
GENERAL DESCRIPTION

The Am9114 and Am9124 are high performance, static, N-Channel, read/write, random access memories organized as 1024 x 4. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of over 30%. The Am9114 and Am9124 are the same except that the Am9124 offers an automatic $\overline{CS}$ power down feature.

The Am9124 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am9124 power decreases from 368mW to 158mW in the standby mode, and the Am91L24 from 262mW to 105mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9114. (See Figure 1, page 4).

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9124 and 3.2mA for Am9114 provides increased short circuit current for improved capacitive drive.

BLOCK DIAGRAM



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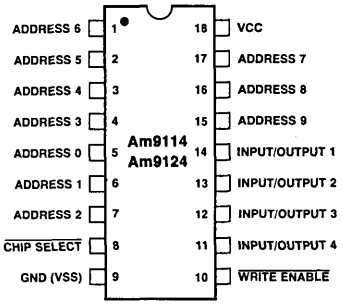
CONNECTION DIAGRAM



Top View
Pin 1 is marked for orientation.

MOS-067

ORDERING INFORMATION

Ambient Temperature	Package Type	ICC Current Level	Access Time					
			Am9114				Am9124 (Power Down Option)	
			450ns	300ns	200ns	150ns	450ns	300ns
0°C ≤ T_A ≤ 70°C	Plastic	70mA	Am9114BPC	Am9114CPC	Am9114EPC	Am9114FPC	Am9124BPC	Am9124CPC
		50mA	Am91L14BPC	Am91L14CPC	Am91L14EPC		Am91L24BPC	Am91L24CPC
	Hermetic	70mA	Am9114BDC	Am9114CDC	Am9114EDC	Am9114FDC	Am9124BDC	Am9124CDC
		50mA	Am91L14BDC	Am91L14CDC	Am91L14EDC		Am91L24BDC	Am91L24CDC
−55°C ≤ T_A ≤ +125°C	Hermetic	80mA	Am9114BDM	Am9114CDM	Am9114EDM		Am9124BDM	Am9124CDM
		60mA	Am91L14BDM	Am91L14CDM			Am91L24BDM	Am91L24CDM

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−3.0 to +7.0V
Power Dissipation (Package Limitation)	1.0W
DC Output Current	10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{CC}	Part Number	Ambient Temperature	V_{SS}	V_{CC}
Am9114DC/PC Am91L14DC/PC Am9124DC/PC Am91L24DC/PC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ± 10%	Am9114DM Am91L14DM Am9124DM Am91L24DM	$-55°C \leq T_A \leq +125°C$	0V	+5.0V ± 10%

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am9124XX Am91L24XX Min	Typ	Max	Am9114XX Am91L14XX Min	Typ	Max	Units
I_{OH}	Output High Current	V_{OH} = 2.4V	V_{CC} = 4.5V	−1.4			−1.0			mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	T_A = +70°C	4.0			3.2			mA
			T_A = +125°C	3.2			2.4			
V_{IH}	Input High Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input Low Voltage			−3.0		0.8	−3.0		0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$				10			10	µA
I_{OZ}	Output Leakage Current	$V_{SS} \leq V_O \leq V_{CC}$ Output Disabled	T_A = +125°C	−50		50	−50		50	µA
			T_A = +70°C	−10		10	−10		10	
I_{OS}	Output Short Circuit Current	(Note 2)	0 to +70°C			95			75	mA
			−55 to +125°C			115			75	
CI	Input Capacitance (Note 1)	Test frequency = 1.0MHz			3.0	5.0		3.0	5.0	pF
CI/O	I/O Capacitance (Note 1)	T_A = 25°C, all pins at 0V			5.0	6.0		5.0	6.0	

ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions		Am91L24 Typ.	Max.	Am9124 Typ.	Max.	Am91L14 Typ.	Max.	Am9114 Typ.	Max.	Units
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ for Am9124/91L24	T_A = 25°C	40		60		40		60		mA
			T_A = 0°C		50		70		50		70	
			T_A = −55°C		60		80		60		80	
I_{PD}	Automatic $\overline{CS}$ Power Down Current	Max. V_{CC} ($\overline{CS} \geq V_{IH}$)	T_A = 25°C	15		24			–		–	mA
			T_A = 0°C		20		30		–		–	
			T_A = −55°C		22		33		–		–	

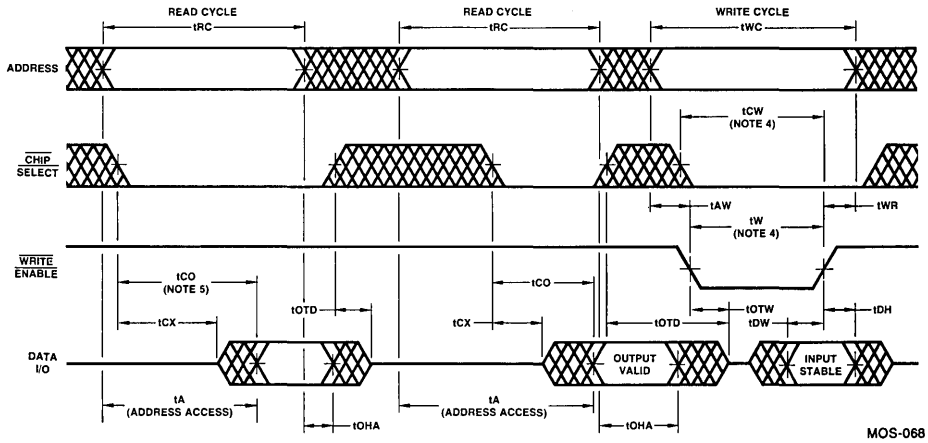
Notes:

1. Typical values are for T_A = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time (t_{CO}) is longer for the Am9124 than for the Am9114. The specified address access time will be valid only when Chip Select is low soon enough for t_{CO} to elapse.

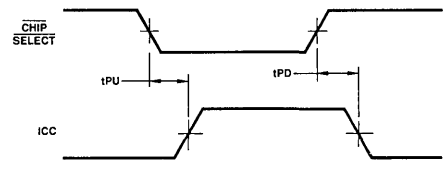
SWITCHING CHARACTERISTICS over operating range (Note 3)

Parameter	Description		Am9114B Am9124B Min	Am9114B Am9124B Max	Am9114C Am9124C Min	Am9114C Am9124C Max	Am9114E Min	Am9114E Max	Am9114F Min	Am9114F Max	Units
Read Cycle											
tRC	Address Valid to Address Do Not Care Time (Read Cycle Time)		450		300		200		150		ns
tA	Address Valid to Data Out Valid Delay (Address Access Time)			450		300		200		150	ns
tCO	Chip Select Low to Data Out Valid (Note 5)	Am9114		120		100		70		70	ns
		Am9124		420		280		NA		NA	ns
tCX	Chip Select Low to Data Out On		20		20		20		10		ns
tOTD	Chip Select High to Data Out Off			100		80		60		40	ns
tOHA	Address Unknown to Data Out Unknown Time		50		50		50		15		ns
Write Cycle											
tWC	Address Valid to Address Do Not Care Time (Write Cycle Time)		450		300		200		150		ns
tW	Write Enable Low to Write Enable High Time (Note 4)	Am9114	200		150		120		90		ns
		Am9124	250		200		NA		NA		ns
tWR	Write Enable High to Address Do Not Care Time		0		0		0		0		ns
tOTW	Write Enable Low to Data Out Off Delay			100		80		60		40	ns
tDW	Data in Valid to Write Enable High Time		200		150		120		90		ns
tDH	Write Enable Low to Data In Do Not Care Time		0		0	0	0		0		ns
tAW	Address Valid to Write Enable Low Time		0		0		0		0		ns
tPD	Chip Select High to Power Low Delay (Am9124 only)			200		150		100		NA	ns
tPU	Chip Select Low to Power High Delay (Am9124 only)		0		0		0		NA		ns
tCW	Chip Select Low to Write Enable High Time (Note 4)	Am9114	200		150		120		90		ns
		Am9124	250		200		NA		NA		ns

SWITCHING WAVEFORMS

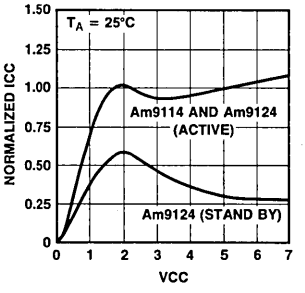


POWER DOWN WAVEFORM (Am9124 ONLY)

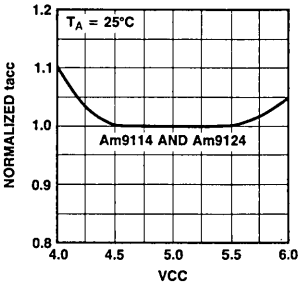


TYPICAL CHARACTERISTICS

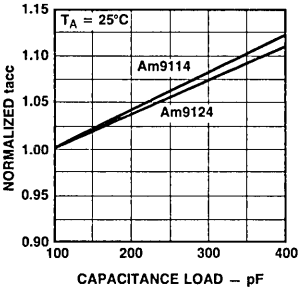
Typical ICC Versus VCC Characteristics



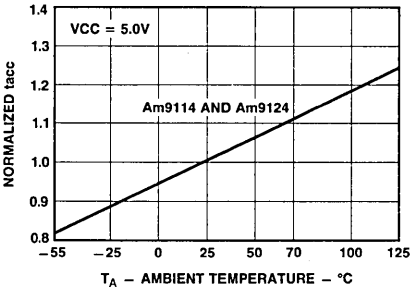
Typical tacc Versus VCC Characteristics



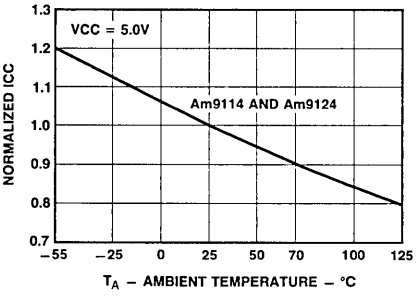
Typical C Load Versus Normalized tacc Characteristics



Normalized tacc Versus Ambient Temperature



Normalized ICC Versus Ambient Temperature



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Configuration	Part Number	Worst Case Current (mA at 0°C) 100% Duty Cycle	50% Duty Cycle
2K x 8	9114	280	280
	91L14	200	200
	9124	200	160
	91L24	140	110
4K x 12	9114	840	840
	91L14	600	600
	9124	480	420
	91L24	330	285
8K x 16	9114	2240	2240
	91L14	1600	1600
	9124	1120	1040
	91L24	760	700

Figure 1. Supply Current Advantages of Am9124.

BIT MAP

Address Designators	
External	Internal
A0	A9
A1	A8
A2	A7
A3	A0
A4	A1
A5	A2
A6	A3
A7	A4
A8	A5
A9	A6

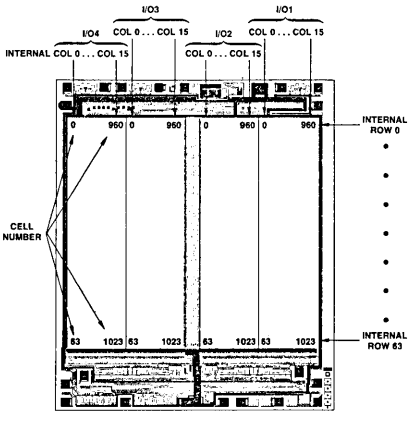


Figure 2. Bit Mapping Information.

Am2147

4096 x 1 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High speed – access times down to 35ns maximum
- 4K x 1 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Equal access and cycle times
- Automatic power-down when deselected
- Low power dissipation
  - Am2147: 990mW active, 165mW power down
  - Am21L47: 688mW active, 83mW power down
- Standard 18-pin, .300 inch dual in-line package
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- 100% MIL-STD-883 reliability assurance testing
- No power-on current surge

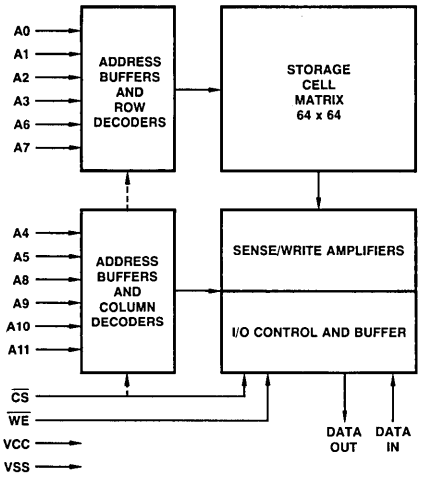
GENERAL DESCRIPTION

The Am2147 is a high performance, 4096-bit, static, read/write, random access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard TTL loads or up to six Schottky TTL loads.

Only a single +5 volt power supply is required. When deselected ($\overline{CS} \geq V_{IH}$), the Am2147 automatically enters a power-down mode which reduces power dissipation by more than 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a 3-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

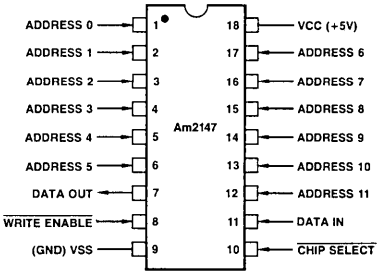
BLOCK DIAGRAM



RAM-001

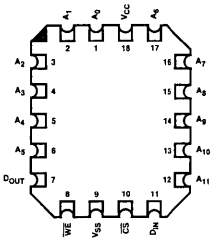
CONNECTION DIAGRAMS – Top Views

DIP



RAM-002

Chip-Pak™
L-18-2



Note: Pin 1 is marked for orientation.

RAM-036

PRODUCT SELECTIONS

	Am2147-35	Am2147-45	Am21L47-45	Am2147-55	Am21L47-55	Am2147-70	Am21L47-70
Maximum Access Time (ns)	35	45	45	55	55	70	70
Maximum Active Current (mA)	180	180	125	180	125	160(180 mil)	125
Maximum Standby Current (mA)	30	30	15	30	15	20(30 mil)	15
Full Military Operating Range Version		Yes		Yes		Yes	

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−55 to +125°C
V_{CC} with Respect to V_{SS}	−0.5 to +7.0V
All Signal Voltages with Respect to V_{SS}	−3.5 to +7.0V
Power Dissipation (Package Limitation)	1.2W
DC Output Current	20mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{CC}
Am2147DC/LC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ± 10%
Am21L47DC/LC			
Am2147DM/LM	$-55°C \leq T_A \leq +125°C$	0V	+5.0V ± 10%

ELECTRICAL CHARACTERISTICS over operating range (Note 4)

Parameter	Description	Test Conditions		Am2147-35 Am2147-45 Am2147-55 Min	Am2147-35 Am2147-45 Am2147-55 Max	Am21L47-45 Am21L47-55 Am21L47-70 Min	Am21L47-45 Am21L47-55 Am21L47-70 Max	Am2147-70 Min	Am2147-70 Max	Units
I_{OH}	Output High Current	V_{OH} = 2.4V	V_{CC} = 4.5V	−4		−4		−4		mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	T_A = 70°C	12		12		12		mA
			T_A = 125°C	8		N/A		8		
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	2.0	6.0	Volts
V_{IL}	Input Low Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$			10		10		10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ Output Disabled	T_A = −55 to +125°C	−50	50	−50	50	−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0MHz			5		5		5	pF
C_O	Output Capacitance	T_A = 25°C, All pins at 0V, V_{CC} = 5V			6		6		6	
I_{CC}	V_{CC} Operating Supply Current	Max V_{CC}, $\overline{CS} \leq$ V_{IL} Output Open	T_A = 70°C		155		105		135	mA
			T_A = 0°C		180		125		160	
			T_A = −55°C		180		N/A		180	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max V_{CC}, ($\overline{CS} \geq$ V_{IH}) (Note 3)	T_A = 0 to 70°C		30		15		20	mA
			T_A = −55 to +125°C		30		N/A		30	

Notes:

1. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30pF load capacitance. Output timing reference is 1.5V for 2147-35 and 0.8/2.0V for −45, −55 and −70 parts.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise I_{SB} will exceed values given.
4. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
5. Chip deselected greater than 55ns prior to selection.
6. Chip deselected less than 55ns prior to selection.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.
8. $\overline{WE}$ is high for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.

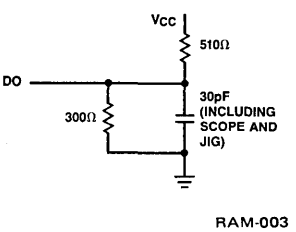


Figure 1. Output Load

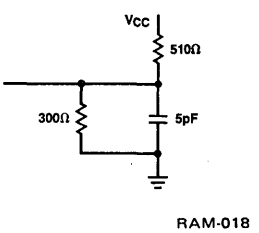


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

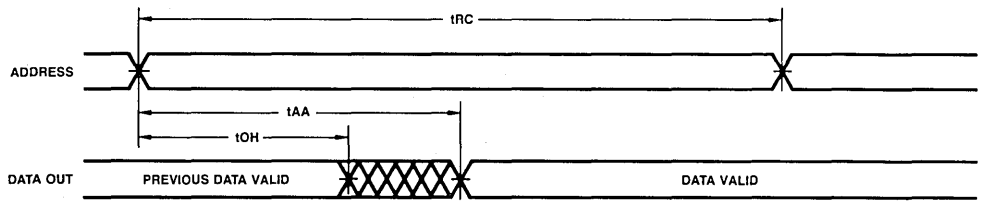
SWITCHING CHARACTERISTICS over operating range (Note 1)

Parameter	Description		Am2147-35 Min	Am2147-35 Max	Am2147-45 Am21L47-45 Min	Am2147-45 Am21L47-45 Max	Am2147-55 Am21L47-55 Min	Am2147-55 Am21L47-55 Max	Am2147-70 Am21L47-70 Min	Am2147-70 Am21L47-70 Max	Units
Read Cycle											
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		35		45		55		70		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			35		45		55		70	ns
t_{ACS1}	Chip Select Low to Data Out Valid	Note 5		35		45		55		70	ns
t_{ACS2}		Note 6		35		45		65		80	
t_{LZ}	Chip Select Low to Data Out On	Note 7	5		5(10*)		10		10		ns
t_{HZ}	Chip Select High to Data Out Off	Note 7	0	30	0	30	0	30	0	40	ns
t_{OH}	Address Unknown to Data Out Unknown Time		5		5		5		5		ns
t_{PD}	Chip Select High to Power Down Delay			20		20		20		30	ns
t_{PU}	Chip Select Low to Power Up Delay		0		0		0		0		ns
Write Cycle											
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		35		45		55		70		ns
t_{WP}	Write Enable Low to Write Enable High	Note 2	20		25		25		40		ns
t_{WR}	Write Enable High to Address		0		0		10		15		ns
t_{WZ}	Write Enable Low to Output in High Z	Note 6	0	20	0	25	0	25	0	35	ns
t_{DW}	Data In Valid to Write Enable High		20		25		25		30		ns
t_{DH}	Data Hold Time		10		10		10		10		ns
t_{AS}	Address Valid to Write Enable Low		0		0		0		0		ns
t_{CW}	Chip Select Low to Write Enable High	Note 2	35		45		45		55		ns
t_{OW}	Write Enable High to Output in Low Z	Note 6	0		0		0		0		ns
t_{AW}	Address Valid to End of Write		35		45		45		55		ns

*Military version only.

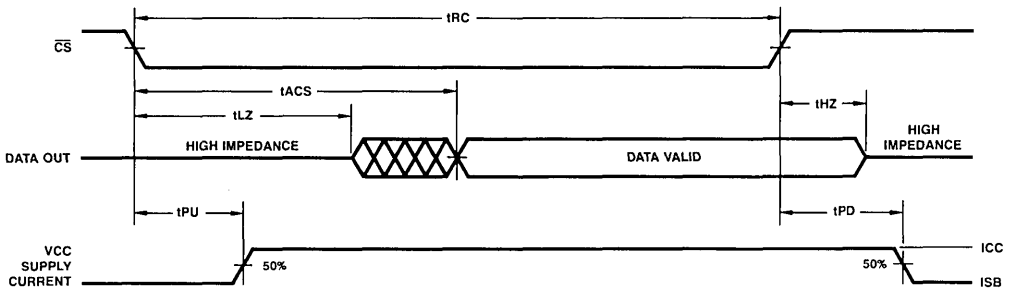
SWITCHING WAVEFORMS

READ CYCLE NO. 1 (Notes 8, 9)



RAM-004

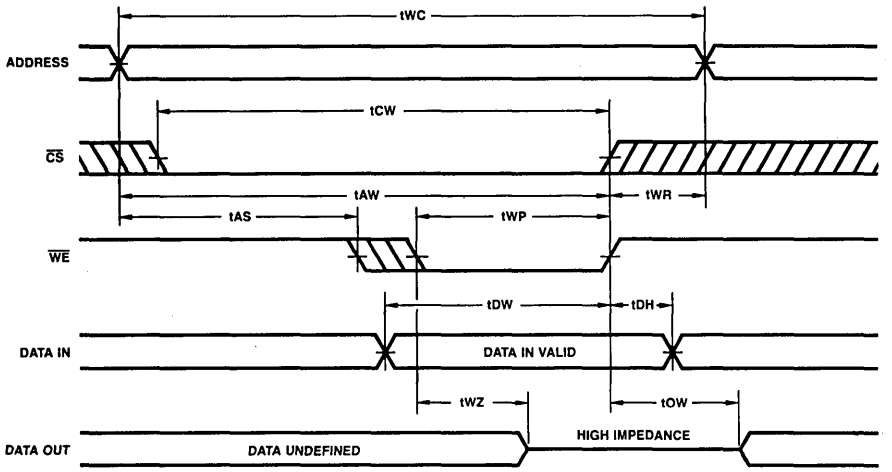
READ CYCLE NO. 2 (Notes 8, 10)



RAM-005

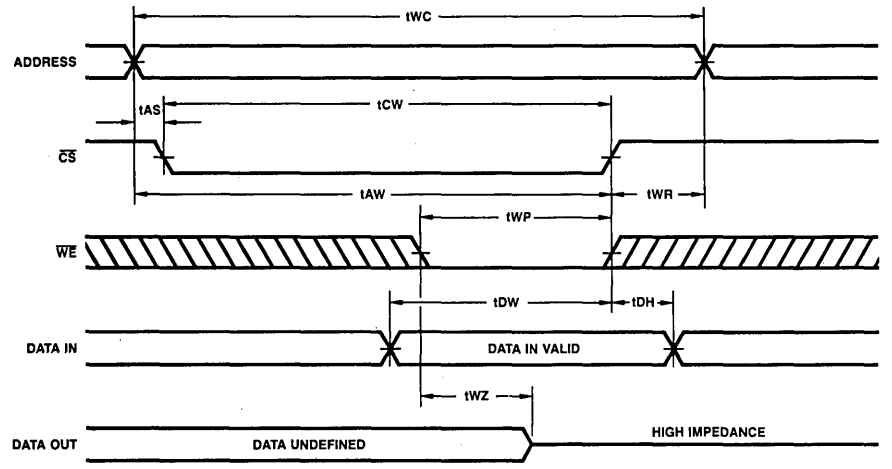
SWITCHING WAVEFORMS (Cont.)

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



RAM-006

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)

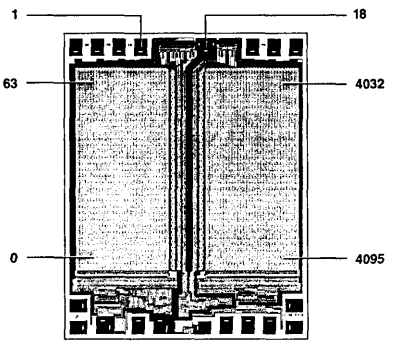


RAM-007

Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

BIT MAP

Address Designators	
External	Internal
A_0	A_2
A_1	A_5
A_2	A_4
A_3	A_3
A_4	A_8
A_5	A_7
A_6	A_1
A_7	A_0
A_8	A_{11}
A_9	A_9
A_{10}	A_{10}
A_{11}	A_6

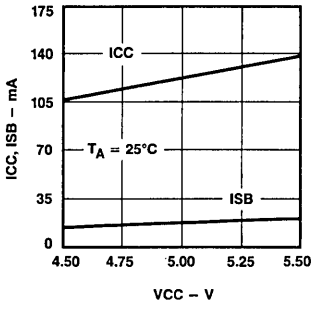


DIE SIZE:
0.130 X 0.106

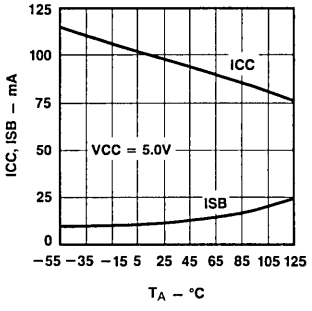
Figure 2. Bit Mapping Information

TYPICAL DC AND AC CHARACTERISTICS

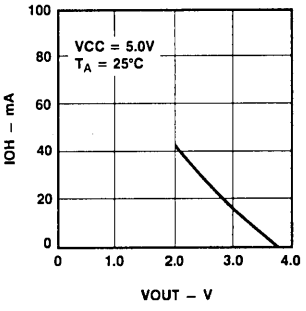
Supply Current Versus Supply Voltage



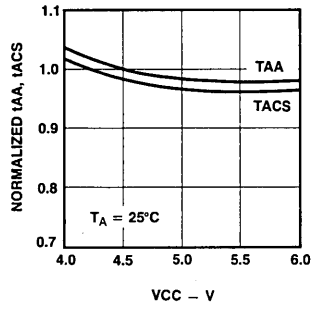
Supply Current Versus Ambient Temperature



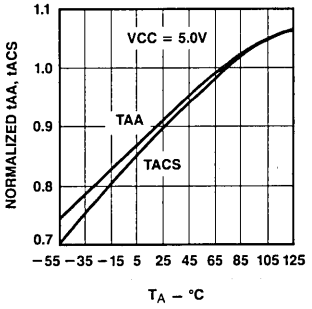
Output Source Current Versus Output Voltage



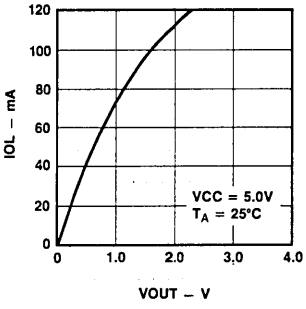
Normalized Access Time Versus Supply Voltage



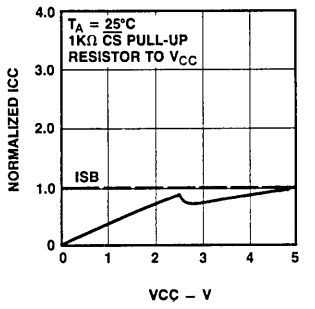
Normalized Access Time Versus Ambient Temperature



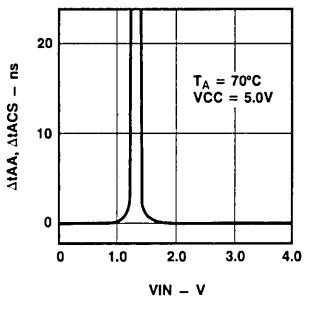
Output Sink Current Versus Output Voltage



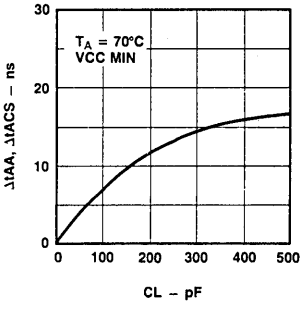
Typical Power-On Current Versus Power Supply



Access Time Change Versus Input Voltage



Access Time Change Versus Output Loading

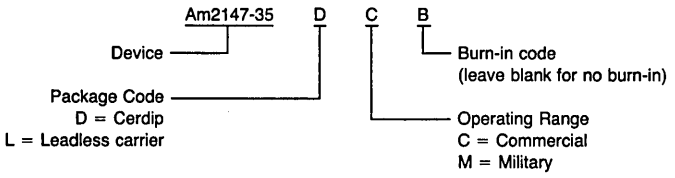


RAM-008

4

ORDERING INFORMATION

Ordering part numbers consist of the device, package, and operating range codes as shown.



Am2148 • Am2149

1024 x 4 Static R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High speed – access times down to 45ns maximum
- 1K x 4 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- Automatic power-down when deselected (Am2148)
- Low power dissipation
  - Am2148: 990mW active, 165mW power down
  - Am21L48: 688mW active, 110mW power down
- Standard 18-pin, .300 inch dual in-line package
- High output drive
  - Up to seven standard TTL loads
- Commercial and full military temperature ranges
- TTL compatible interface levels
- 100% MIL-STD-883 reliability assurance testing
- Guaranteed 0.1% AQL

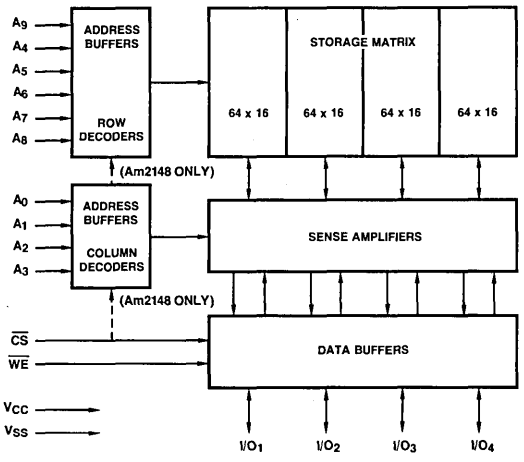
GENERAL DESCRIPTION

The Am2148 and Am2149 are high performance, static, N-Channel, read/write, random access memories organized as 1024 x 4. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. The Am2148 and Am2149 are the same except that the Am2148 offers an automatic $\overline{CS}$ power down feature.

The Am2148 remains in a low-power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am2148 power decreases from 990mW to 165mW in the standby mode. The $\overline{CS}$ input does not affect the power dissipation of the Am2149.

Data readout is not destructive and has the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied.

BLOCK DIAGRAM



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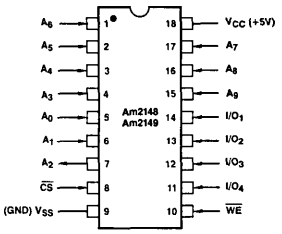
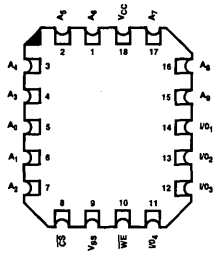
CONNECTION DIAGRAMS
Top Views

DIP



Chip-Pak™ L-18-2



Note: Pin 1 is marked for orientation.

RAM-034

PRODUCT SELECTIONS

		Am2148/9-45	Am21L48/9-45	Am2148/9-55	Am21L48/9-55	Am2148/9-70	Am21L48/9-70
Maximum Access Time (ns)		45	45	55	55	70	70
Max Active Current (mA)	0 to 70°C	180	125	180	125	N/A	125
Max Standby Current (mA)*	0 to 70°C	30	20	30	20	N/A	20
Max Active Current (mA)	−55 to 125°C	180	N/A	180	N/A	180	N/A
Max Standby Current (mA)*	−55 to 125°C	30	N/A	30	N/A	30	N/A

*Am2148 only

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MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−55 to +125°C
V_{CC} with Respect to V_{SS}	−0.5 to +7.0V
All Signal Voltages with Respect to V_{SS}	−3.5V to +7.0V
Power Dissipation (Package Limitation)	1.2W
DC Output Current	20mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{CC}
Am2148/9DC/LC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ± 10%
Am21L48/9DC/LC			
Am2148/9DM/LM	$-55°C \leq T_A \leq +125°C$	0V	+5.0V ± 10%

ELECTRICAL CHARACTERISTICS over operating range (Note 4)

Parameter	Description	Test Conditions		Am2148/9-45 Am2148/9-55 Am2148/9-70 Min	Max	Am21L48/9-45 Am21L48/9-55 Am21L48/9-70 Min	Max	Units
I_{OH}	Output High Current	V_{OH} = 2.4V	V_{CC} = 4.5V	−4		−4		mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	T_A = 70°C	8		8		mA
			T_A = 125°C	8		N/A		
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	Volts
V_{IL}	Input Low Voltage			−3.0	0.8	−3.0	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$			10		10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ Output Disabled	T_A = −55 to +125°C	−50	50	−50	50	μA
C_I	Input Capacitance	Test Frequency = 1.0MHz T_A = 25°C, All pins at 0V, V_{CC} = 5V			5		5	pF
$C_{I/O}$	Input/Output Capacitance				7		7	
I_{CC}	V_{CC} Operating Supply Current	Max V_{CC}, $\overline{CS} \leq V_{IL}$ Output Open	T_A = 0 to +70°C		180		125	mA
			T_A = −55 to +125°C		180		N/A	
I_{SB}	Automatic $\overline{CS}$ Power Down Current	Max V_{CC}, ($\overline{CS} \geq V_{IH}$) (Note 3)	T_A = 0 to +70°C		30		20	mA
			T_A = −55 to +125°C		30		N/A	
I_{OS}	Output Short Circuit Current	$GND \leq V_O \leq V_{CC}$ (Note 11)	T_A = 0 to +70°C		±275		±275	mA
			T_A = −55 to +125°C		±350		±350	

Notes:

1. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30pF load capacitance. Output timing reference is 1.5V.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise I_{SB} will exceed values given (Am2148 only).
4. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
5. Chip deselected greater than 55ns prior to selection.
6. Chip deselected less than 55ns prior to selection.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.
8. WE is high for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

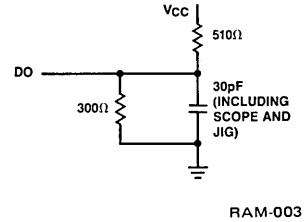


Figure 1. Output Load

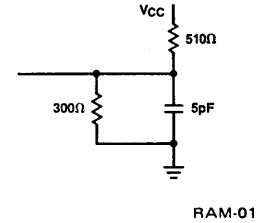


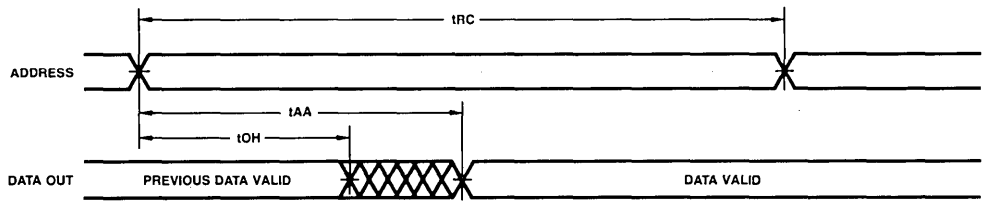
Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

SWITCHING CHARACTERISTICS over operating range (Note 1)

Parameter	Description			Am2148/9-45 Am21L48/9-45 Min	Am2148/9-45 Am21L48/9-45 Max	Am2148/9-55 Am21L48/9-55 Min	Am2148/9-55 Am21L48/9-55 Max	Am2148/9-70 Am21L48/9-70 Min	Am2148/9-70 Am21L48/9-70 Max	Units
Read Cycle										
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)			45		55		70		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)				45		55		70	ns
t_{ACS1}	Chip Select Low to Data Out Valid (Am2148 only)		Note 5		45		55		70	ns
t_{ACS2}			Note 6		55		65		80	
t_{ACS}	Chip Select Low to Data Out Valid (Am2149 only)				20		25		30	ns
t_{LZ}	Chip Select Low to Data Out On	Am2148	Note 7	20		20		20		ns
		Am2149		5		5		5		
t_{HZ}	Chip Select High to Data Out Off		Note 7	0	20	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time			5		5		5		ns
t_{PD}	Chip Select High to Power Down Delay	Am2148			30		30		30	ns
t_{PU}	Chip Select Low to Power Up Delay	Am2148		0		0		0		ns
Write Cycle										
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)			45		55		70		ns
t_{WP}	Write Enable Low to Write Enable High		Note 2	35		40		50		ns
t_{WR}	Write Enable High to Address			5		5		5		ns
t_{WZ}	Write Enable Low to Output in High Z		Note 7	0	15	0	20	0	25	ns
t_{DW}	Data In Valid to Write Enable High			20		20		25		ns
t_{DH}	Data Hold Time			0		0		0		ns
t_{AS}	Address Valid to Write Enable Low			0		0		0		ns
t_{CW}	Chip Select Low to Write Enable High		Note 2	40		50		65		ns
t_{OW}	Write Enable High to Output in Low Z		Note 7	0		0		0		ns
t_{AW}	Address Valid to End of Write			40		50		65		ns

SWITCHING WAVEFORMS

READ CYCLE NO. 1 (Notes 8, 9)



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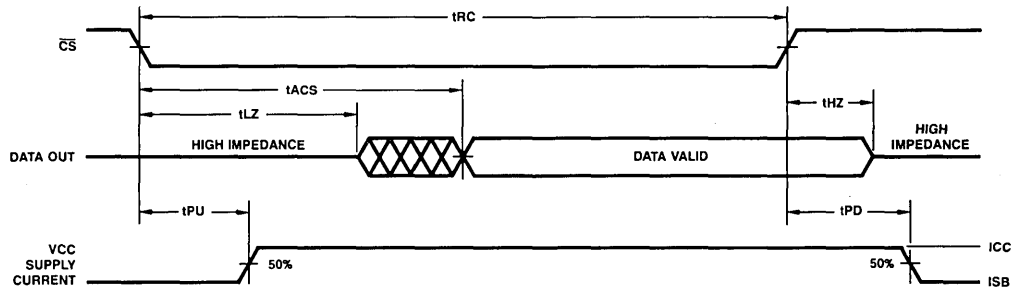
READ CYCLE NO. 2 (Notes 8, 10)



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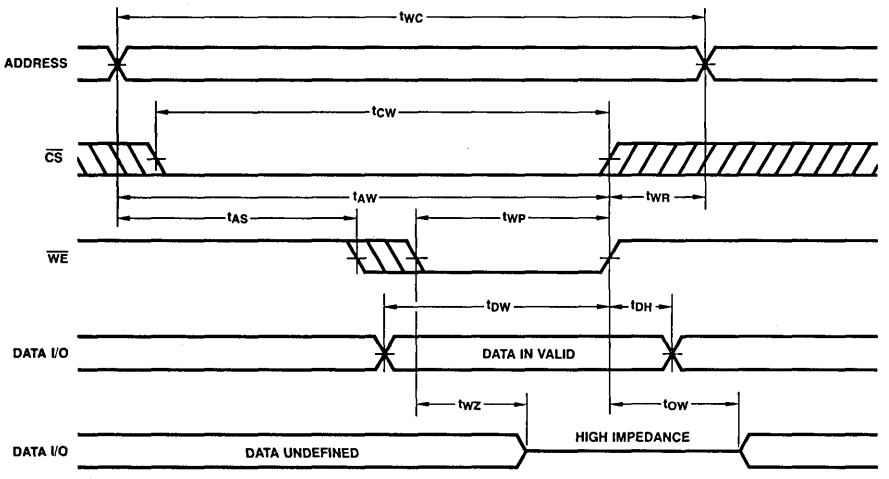
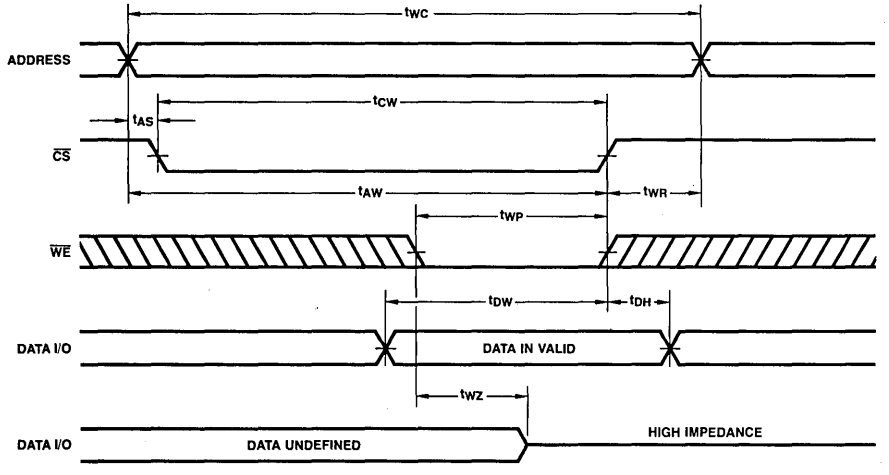
SWITCHING WAVEFORMS (Cont.)

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



MOS-573

WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



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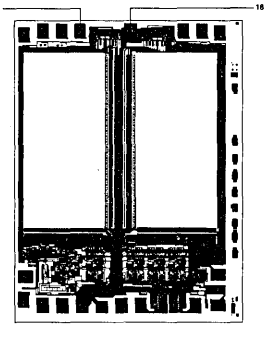
Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

BIT MAP

Address Designators	
External	Internal
A_0	A_7
A_1	A_8
A_2	A_9
A_3	A_6
A_4	A_5
A_5	A_4
A_6	A_3
A_7	A_2
A_8	A_1
A_9	A_0

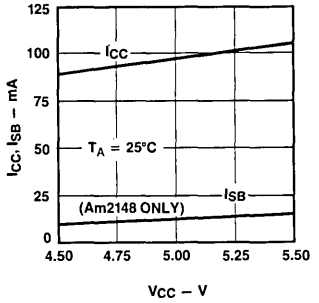


DIE SIZE: 0.107 x 0.145

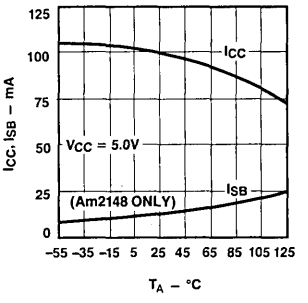
Figure 2. Bit Mapping Information.

TYPICAL DC AND AC CHARACTERISTICS

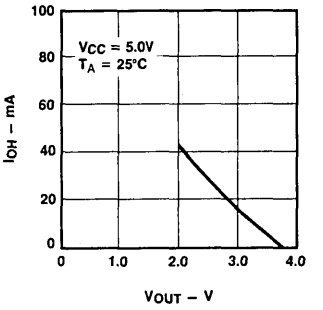
Supply Current Versus Supply Voltage



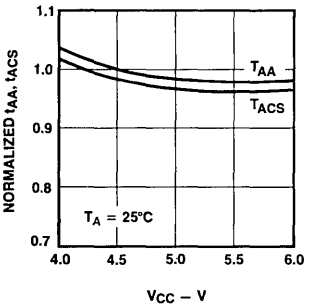
Supply Current Versus Ambient Temperature



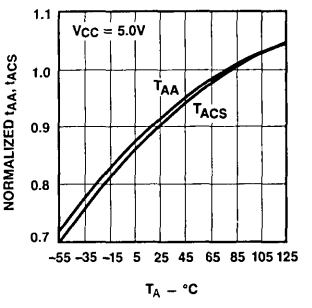
Output Source Current Versus Output Voltage



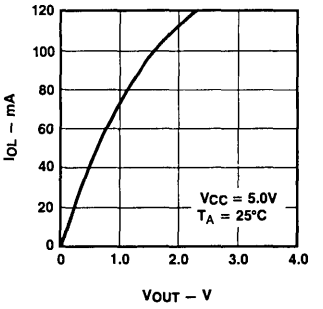
Normalized Access Time Versus Supply Voltage



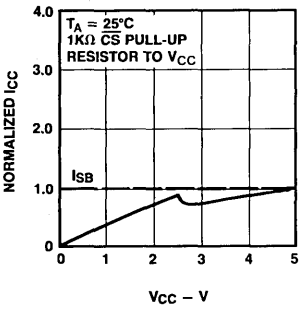
Normalized Access Time Versus Ambient Temperature



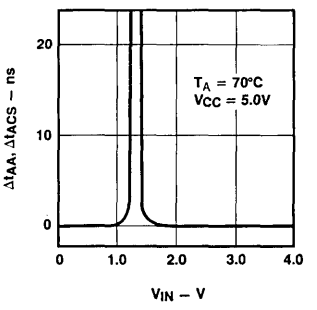
Output Sink Current Versus Output Voltage



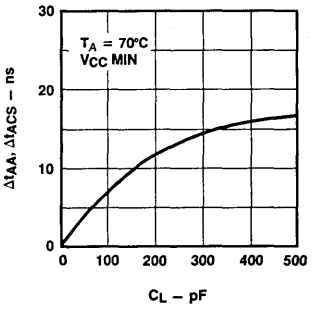
Typical Power-On Current Versus Power Supply Am2148



Access Time Change Versus Input Voltage



Access Time Change Versus Output Loading



RAM-035

4

ORDERING INFORMATION

Am2148-45 Am2149-45 Order Code	Am2148-55 Am2149-55 Order Code	Am2148-70 Am2149-70 Order Code	Am21L48-45 Am21L49-45 Order Code	Am21L48-55 Am21L49-55 Order Code	Am21L48-70 Am21L49-70 Order Code	Package Type	Screening Level	Operating Range
Am2148-45DC	Am2148-55DC	Am2148-70DC	Am21L48-45DC	Am21L48-55DC	Am21L48-70DC	D-18-1	C-1	C
Am2148-45DM	Am2148-55DM	Am2148-70DM	–	–	–	D-18-1	C-3	M
Am2148-45DMB	Am2148-55DMB	Am2148-70DMB	–	–	–	D-18-1	B-3	M
Am2148-45LC	Am2148-55LC	Am2148-70LC	Am21L48-45LC	Am21L48-55LC	Am21L48-70LC	L-18-2	C-1	C
Am2148-45LM	Am2148-55LM	Am2148-70LM	–	–	–	L-18-2	C-3	M
Am2148-45LMB	Am2148-55LMB	Am2148-70LMB	–	–	–	L-18-2	B-3	M
Am2149-45DC	Am2149-55DC	Am2149-70DC	Am21L49-45DC	Am21L49-55DC	Am21L49-70DC	D-18-1	C-1	C
Am2149-45DM	Am2149-55DM	Am2149-70DM	–	–	–	D-18-1	C-3	M
Am2149-45DMB	Am2149-55DMB	Am2149-70DMB	–	–	–	D-18-1	B-3	M
Am2149-45LC	Am2149-55LC	Am2149-70LC	Am21L49-45LC	Am21L49-55LC	Am21L49-70LC	L-18-2	C-1	C
Am2149-45LM	Am2149-55LM	Am2149-70LM	–	–	–	L-18-2	C-3	M
Am2149-45LMB	Am2149-55LMB	Am2149-70LMB	–	–	–	L-18-2	B-3	M

Notes: 1. D = Hermetic DIP, L = Leadless Chip Carrier. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C.
Level B-3 conforms to MIL-STD-883, Class B.
3. See Operating Range Table.

Am9128

2048 x 8 Static R/W Random Access Memory

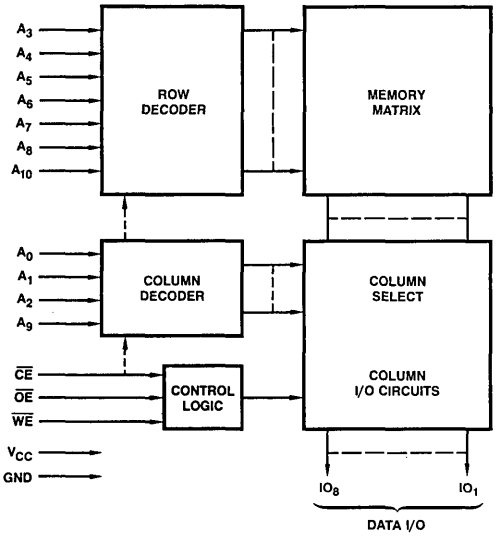
DISTINCTIVE CHARACTERISTICS

- 2,048 x 8-bit organization
- Standard 24-pin, 0.6″ wide DIP package
- Logic voltage levels compatible with TTL
- Three-state output buffers-common I/O
- Fully static; no clocks or refresh required
- Single +5V power supply ±10% tolerance
- MIL-STD-883 reliability assurance testing
- I_{CC} max down to 100mA
- T_{AA}/T_{ACS} down to 70ns
- Power down mode (I_{CC} standby max down to 15mA)
- Commercial and full military temperature ranges
- Guaranteed 0.1% AQL

GENERAL DESCRIPTION

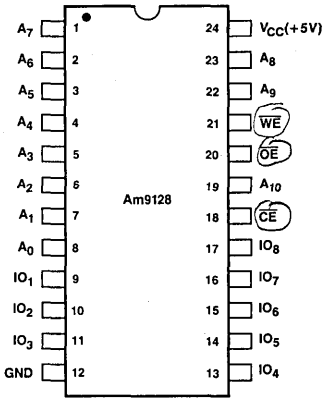
The Am9128 is a 16,384-bit static Random Access Read-write Memory organized as 2048 words of 8 bits. It uses fully static circuitry, requiring no clocks or refresh to operate. Directly TTL-compatible inputs and outputs and operation from a single +5V supply simplify system designs. Common data I/O pins using three-state outputs are provided. The Am9128 is available in an industry-standard 24-pin DIP package with 0.6-inch pin row spacing. The Am9128 uses the JEDEC standard pinout for byte-wide memories (compatible to 16K EPROM's).

BLOCK DIAGRAM



RAM-025

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

RAM-026

PRODUCT SELECTIONS

Part Number		Am9128-70	Am9128-10	Am9128-15	Am9128-20
Maximum Access Time (ns)		70	100	150	200
Maximum Operating Current (mA)	0° to 70°C	140	120	100	140
	−55° to 125°C	N/A	N/A	150	150
Maximum Standby Current (mA)	0° to 70°C	30	15	15	30
	−55° to 125°C	N/A	N/A	30	30

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−3.0V to +7.0V
Power Dissipation (Package Limitation)	1.0W
DC Output Current	10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{CC}
Am9128-10DC/PC Am9128-15DC/PC Am9128-20DC/PC Am9128-70DC/PC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ± 10%
Am9128-15DM Am9128-20DM	$-55°C \leq T_A \leq +125°C$	0V	+5V ± 10%

ELECTRICAL CHARACTERISTICS over operating range (Note 3)

Parameter	Description	Test Conditions		Am9128-10 Min	Am9128-10 Max	Am9128-15 Min	Am9128-15 Max	Am9128-70 Am9128-20 Min	Am9128-70 Am9128-20 Max	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4V	V_{CC} = 4.5V	−2		−2		−2		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4V		4		4		4		mA
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 1.0	2.0	V_{CC} + 1.0	2.0	V_{CC} + 1.0	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	−0.5	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$			10		10		10	μA
I_{OZ}	Output Leakage Current	GND ≤ $V_O \leq V_{CC}$ Output Disabled			10		10		10	μA
C_I	Input Capacitance	Test Frequency = 1.0MHz T_A = 25°C, All pins at 0V	V_{CC} = 5.0V		6		6		6	pF
$C_{I/O}$	Input/Output Capacitance				7		7		7	
I_{CC}	V_{CC} Operating Supply Current	Max V_{CC}, $\overline{CE} \leq V_{IL}$ Outputs Open	$T_A = -55°C$ to +125°C		N/A		150		150 (Note 11)	mA
			T_A = 0°C to +70°C		120		100		140	
I_{SB}	Automatic $\overline{CE}$ Power Down Current	Max V_{CC}, $\overline{CE} \geq V_{IH}$	$T_A = -55°C$ to +125°C		N/A		30		30 (Note 11)	mA
			T_A = 0°C to 70°C		15		15		30	
I_{PO}	Peak Power On Current	V_{CC} = GND to V_{CC} Max $\overline{CE} \geq V_{IH}$ (Note 2)	$T_A = -55°C$ to +125°C		N/A		30		30 (Note 11)	mA
			T_A = 0°C to 70°C		15		15		30	

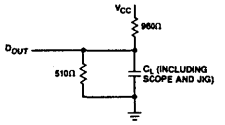
Notes:
1. The internal write time of the memory is defined by the overlap of $\overline{CE}$ Low and $\overline{WE}$ Low. Both signals must be Low to initiate a write and either signal can terminate a write by going High. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. A pull up resistor to V_{CC} on the $\overline{CE}$ input is required during power up to keep the device deselected, otherwise I_{SB} will exceed values given.
3. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
4. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices.
5. $\overline{WE}$ is High for read cycle.
6. Device is continuously selected, $\overline{CE} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CE}$ transition Low.
8. $\overline{OE} = V_{IL}$.
9. C_L = 100pF for Am9128-10/-15/-20. C_L = 30pF for Am9128-70.
10. Transition is measured at V_{OH} − 500mV and V_{OL} + 500mV. Levels on the output from 1.5V level on the input with load shown in Figure 1 using C_L = 5pF.
11. Am9128-20 only.

SWITCHING CHARACTERISTICS *over operating range unless otherwise specified*

Parameter	Description			Am9128-70 Min	Am9128-70 Max	Am9128-10 Min	Am9128-10 Max	Am9128-15 Min	Am9128-15 Max	Am9128-20 Min	Am9128-20 Max	Units
READ CYCLE												
t_{RC}	Read Cycle Time			70		100		150		200		ns
t_{ACC}	Address Access Time		Note 9		70		100		150		200	ns
t_{ACS}	Chip Select Access Time		Note 9		70		100		150		200	ns
t_{OE}	Output Enable Time	0°C to +70°C	Note 9		40		50		60		70	ns
		−55°C to +125°C			N/A		N/A		70		80	
t_{OH}	Output Hold Time from Address Change			10		10		10		10		ns
t_{CLZ}	Output in LOW-Z from $\overline{CE}$		Notes 4, 10	10		10		10		10		ns
t_{CHZ}	Output in HIGH-Z from $\overline{CE}$		Notes 4, 10		35		40		55		55	ns
t_{OLZ}	Output in LOW-Z from $\overline{OE}$		Notes 4, 10	5		5		5		5		ns
t_{OHZ}	Output in HIGH-Z from $\overline{OE}$		Notes 4, 10		30		35		50		50	ns
t_{PU}	Chip Selection to Power Up Time			0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time				40		50		60		60	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time			70		100		150		200		ns
t_{CW}	Chip Selection to End of Write	0°C to +70°C	Note 1	60		90		120		150		ns
		−55°C to +125°C		N/A		N/A		130		160		
t_{AS}	Address Setup Time			5		10		20		20		ns
t_{WP}	Write Pulse Width		Note 1	60		70		100		100		ns
t_{WR}	Write Recovery Time			5		5		5		5		ns
t_{DS}	Data Setup Time			30		40		50		60		ns
t_{DH}	Data Hold Time			5		5		5		5		ns
t_{WLZ}	Output in LOW-Z from $\overline{WE}$		Notes 4, 10	5		5		5		5		ns
t_{WHZ}	Output in HIGH-Z from $\overline{WE}$		Notes 4, 10		30		35		50		50	ns
t_{AW}				65		80		120		120		ns

AC TEST CONDITIONS

Input Pulse Levels	0 to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

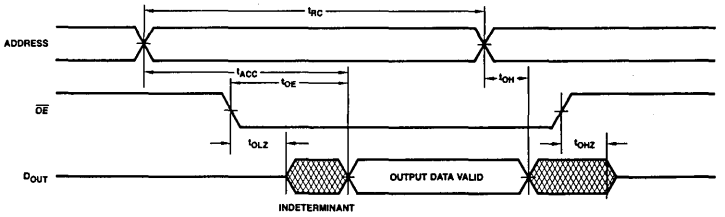


RAM-032

Figure 1. Output Load (Notes 9, 10)

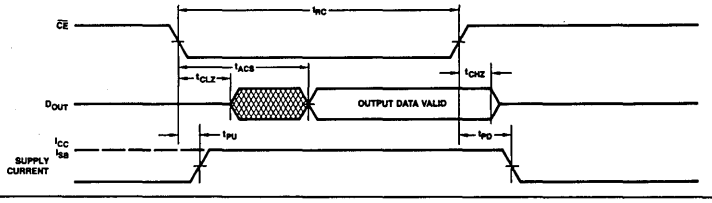
TIMING WAVEFORMS

READ CYCLE 1 (Notes 5, 6)



RAM-027

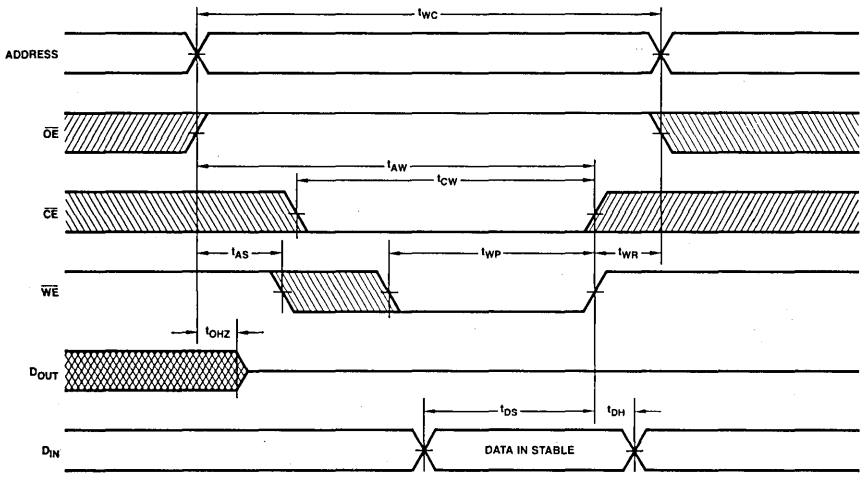
READ CYCLE 2 (Notes 5, 7, 8)



RAM-028

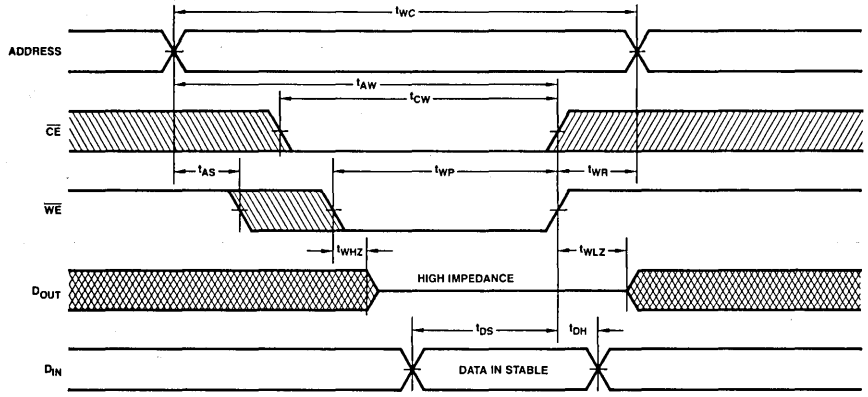
TIMING WAVEFORMS (Cont.)

WRITE CYCLE 1



RAM-029

WRITE CYCLE 2 (Notes 7, 8)



RAM-030

BIT MAP

Address Designators	
External	Internal
A_3	AX_0
A_4	AX_1
A_5	AX_2
A_6	AX_3
A_7	AX_4
A_8	AX_5
A_{10}	AX_6
A_0	AY_0
A_1	AY_1
A_2	AY_2
A_9	AY_3

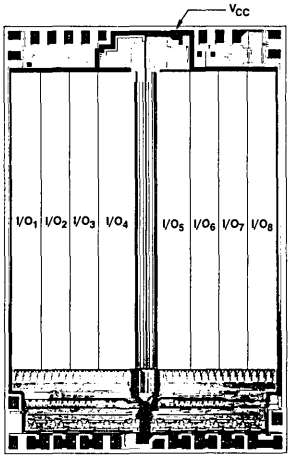
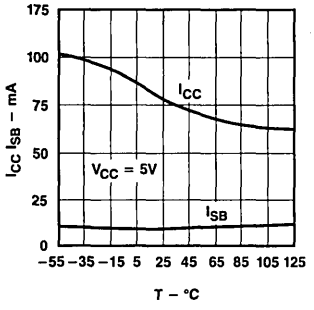


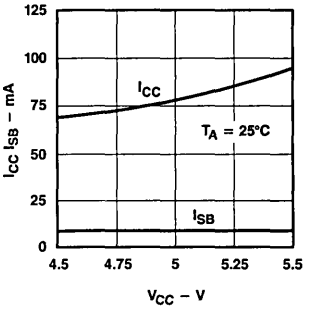
Figure 2. Bit Mapping Information

TYPICAL DC AND AC CHARACTERISTICS

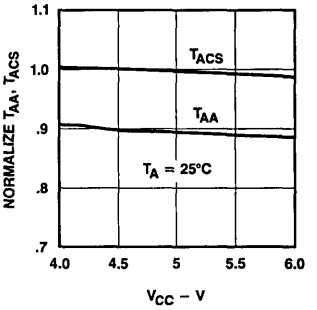
Supply Current Versus Ambient Temperature



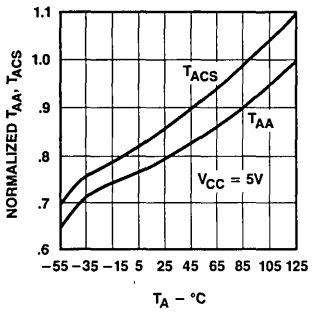
Supply Current Versus Supply Voltage



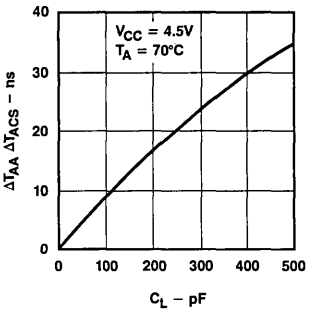
Normalized Access Time Versus Supply Voltage



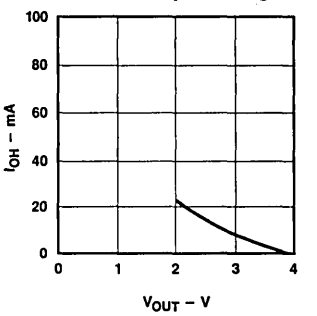
Normalized Access Time Versus Ambient Temperature



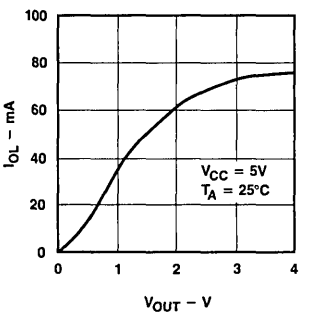
Access Time Change Versus Output Loading



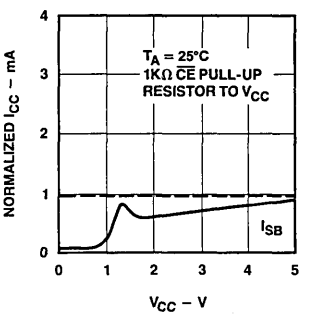
Output Source Current Versus Output Voltage



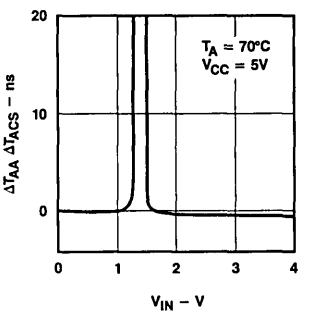
Output Sink Current Versus Output Voltage



Typical Power-On Current Versus Power Supply



Access Time Change Versus Input Voltage



RAM-031

4

ORDERING INFORMATION

Am9128-70 Order Code	Am9128-10 Order Code	Am9128-15 Order Code	Am9128-20 Order Code	Package Type	Screening Level	Operating Range
AM9128-70PC	AM9128-10PC	AM9128-15PC	AM9128-20PC	P-24-1	C-1	C
AM9128-70DC	AM9128-10DC	AM9128-15DC	AM9128-20DC	D-24-1	C-1	C
		AM9128-15DM	AM9128-20DM	D-24-1	C-3	M
		AM9128-15DMB	AM9128-20DMB	D-24-1	B-3	M

Notes: 1. P = Molded DIP, D = Hermetic DIP. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
3. See operating range table.

Am9167

16,384 x 1 Static R/W Random Access Memory

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- High speed – access times down to 45ns maximum
- 16K x 1 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Equal access and cycle times
- Automatic power down when deselected
- Low power dissipation
  - Am9167: 660mW active, 165mW power down
- Standard 20-pin, .300 inch dual-in-line package
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- 100% MIL-STD-883 reliability assurance testing
- No power-on current surge
- Guaranteed 0.1% AQL

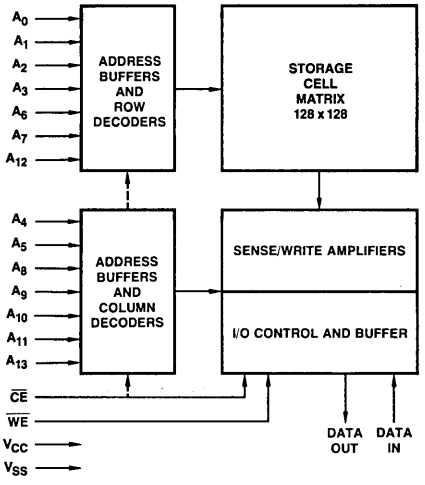
GENERAL DESCRIPTION

The Am9167 is a high performance, 16,384-bit, static, read/write, random access memory. It is organized as 16,384 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to six standard Schottky TTL loads or up to seven standard TTL loads.

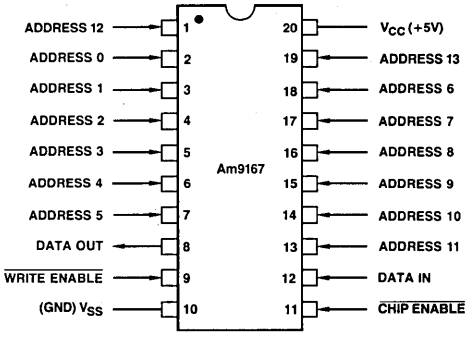
Only a single +5 volt power supply is required. When deselected ($\overline{CE} \geq V_{IH}$), the Am9167 automatically enters a power-down mode which reduces power dissipation by 75%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 20-pin package. Data Out is the same polarity as Data In. Data Out is a 3-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

PRODUCT SELECTIONS

	Am9167-45	Am9167-55	Am9167-70
Maximum Access Time (ns)	45	55	70
Maximum Active Current (mA)	120	120	120
Maximum Standby Current (mA)	30	30	30

Am9168 • Am9169

4096 x 4 Static R/W Random Access Memory

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- High speed – access times down to 45ns maximum
- 4K x 4 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Equal access and cycle times
- Automatic power down when deselected for Am9168
- Power dissipation
  - Am9168: 660mW active 165mW power down
    Am9169: 660mW
- Standard 20-pin, .300 inch dual-in-line package
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- 100% MIL-STD-883 reliability assurance testing
- Guaranteed 0.1% AQL

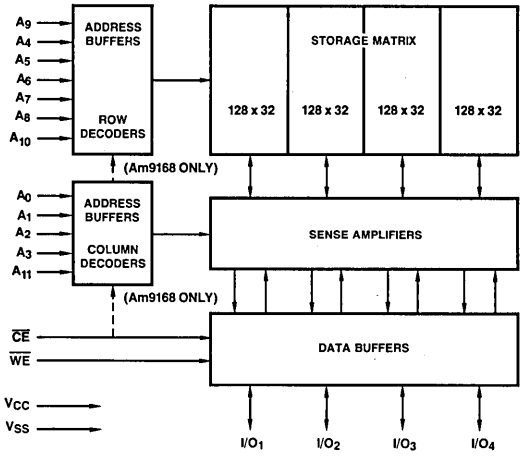
GENERAL DESCRIPTION

The Am9168 and Am9169 are high performance, static, N-Channel, read/write, random access memories organized as 4096 words of 4 bits. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. The Am9168 and Am9169 are the same except that the Am9168 offers an automatic $\overline{CE}$ power down feature.

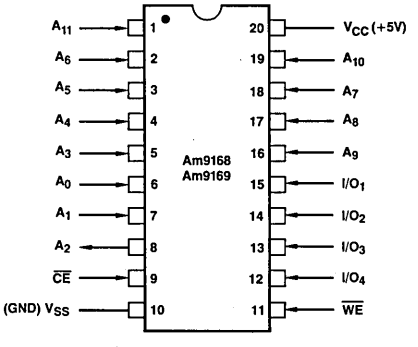
The Am9168 remains in a low-power standby mode as long as $\overline{CE}$ remains high, thus reducing its power requirements. The Am9168 power decreases from 660mW to 165mW in the standby mode. The $\overline{CE}$ input does not affect the power dissipation of the Am9169.

Data readout is not destructive and has the same polarity as data input. $\overline{CE}$ provides for easy selection of an individual package when the outputs are OR-tied.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

PRODUCT SELECTIONS

	Am9168-45	Am9169-45	Am9168-55	Am9169-55	Am9168-70	Am9169-70
Maximum Access Time (ns)	45	45	55	55	70	70
Maximum Active Current (mA)	120	120	120	120	120	120
Maximum Standby Current (mA)	30	N/A	30	N/A	30	N/A

Am9016

16,384 x 1 Dynamic R/W Random Access Memory
Advanced MOS/LSI

DISTINCTIVE CHARACTERISTICS

- High density 16K x 1 organization
- Replacement for MK4116
- Low maximum power dissipation – 462mW active, 20mW standby
- High-speed operation – 150ns access, 320ns cycle (COM'L)
  200ns access, 375ns cycle (MIL)
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- $\overline{RAS}$ only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual-in-line package
- JEDEC standard 18-pin, Chip-Pak™ leadless chip carrier
- Double poly N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing
- Extended ambient operating temperature (−55 to +85°C) available

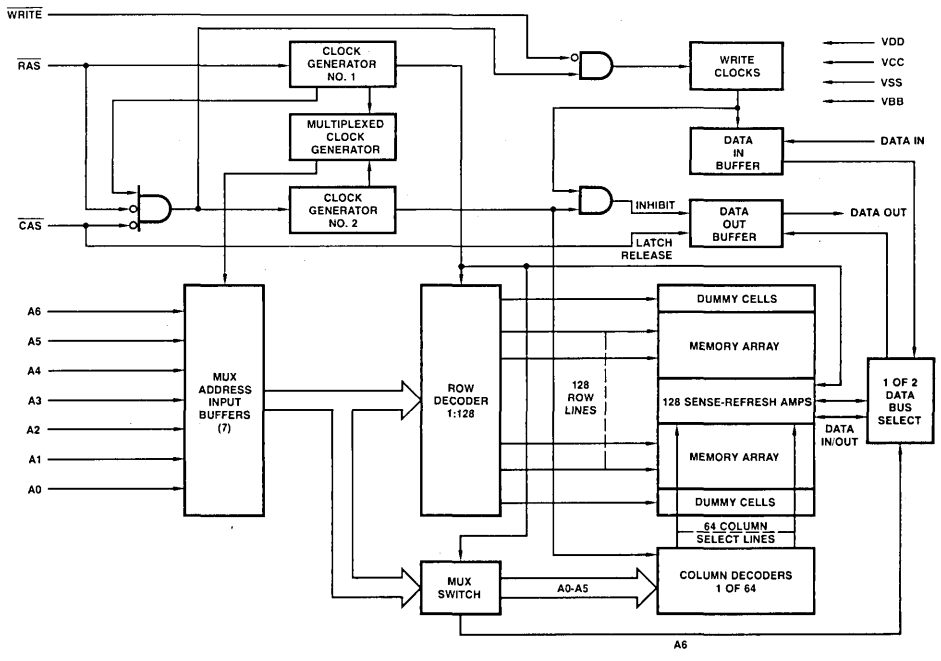
GENERAL DESCRIPTION

The Am9016 is a high-speed, 16K-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP or 18-pin leadless chip carrier. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share seven input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance and power dissipation.

The 3-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

BLOCK DIAGRAM



MOS-190

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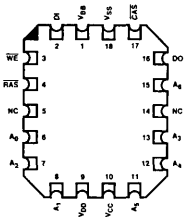
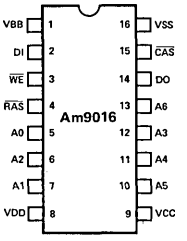
CONNECTION DIAGRAMS – Top Views

Chip-Pak
L-18-2



DIP



A0 – A6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
DI	DATA IN
DO	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
VDD	POWER (+12V)
VCC	POWER (+5V)
VSS	GROUND
VBB	POWER (–5V)
$\overline{WE}$	WRITE ENABLE

MOS-670

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	–65 to +150°C
Ambient Temperature Under Bias	–55 to +85°C
Voltage on Any Pin Relative to VBB	–0.5 to +20V
VDD and VCC Supply Voltages with Respect to VSS	–1.0 to +15.0V
VBB – VSS (VDD – VSS > 0V)	0V
Power Dissipation	1.0W
Short Circuit Output Current	50mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{DD}	V_{CC}	V_{SS}	V_{BB}
Am9016DC/PC/LC	$0°C \leq T_A \leq +70°C$	+12V ±10%	+5V ±10%	0	–5V ±10%
Am9016DL/LL	$-55°C \leq T_A \leq +85°C$	+12V ±10%	+5V ±10%	0	–5V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 9)

Parameters	Description		Test Conditions	Am9016 Min	Typ	Max	Units
VOH	Output HIGH Voltage		IOH = –5.0mA	2.4		VCC	Volts
VOL	Output LOW Voltage		IOL = 4.2mA	VSS		0.40	Volts
VIH	Input HIGH Voltage for Address, Data In			2.4		7.0	Volts
VIHC	Input HIGH Voltage for $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$			2.7		7.0	Volts
VIL	Input LOW Voltage			–1.0		0.80	Volts
IIX	Input Load Current		$VSS \leq VI \leq 7V$	–10		10	µA
IOZ	Output Leakage Current		$VSS \leq VO \leq VCC$, Output OFF	–10		10	µA
ICC	VCC Supply Current		Output OFF (Note 4)	–10		10	µA
IBB	VBB Supply Current, Average	$0°C \leq T_A \leq +70°C$	Standby, $\overline{RAS} \geq$ VIHC			100	µA
		$-55°C \leq T_A \leq +85°C$				200	
		$0°C \leq T_A \leq +70°C$	Operating, Minimum Cycle Time			200	
		$-55°C \leq T_A \leq +85°C$				400	
IDD	VDD Supply Current, Average	Operating IDD1	$\overline{RAS}$ Cycling, $\overline{CAS}$ Cycling, Minimum Cycle Times			35	mA
		Page Mode IDD4	$\overline{RAS} \leq$ VIL, $\overline{CAS}$ Cycling, Minimum Cycle Times			27	
		$\overline{RAS}$ Only Refresh IDD3	$\overline{RAS}$ Cycling, $\overline{CAS} \geq$ VIHC, Minimum Cycle Times			27	
	$0°C \leq T_A \leq +70°C$	Standby IDD2	$\overline{RAS} \geq$ VIHC			1.5	
	$-55°C \leq T_A \leq +85°C$		$\overline{RAS} \geq$ VIHC			2.25	
CI	Input Capacitance	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Inputs at 0V, f = 1MHz, Nominal Supply Voltages			10	pF
		Address, Data In				5.0	
CO	Output Capacitance		Output OFF			7.0	

SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5)

Parameters	Description		Am9016C Min	Am9016C Max	Am9016D Min	Am9016D Max	Am9016E Min	Am9016E Max	Am9016F Min	Am9016F Max	Units
tAR	$\overline{RAS}$ LOW to Column Address Hold Time		200		160		120		95		ns
tASC	Column Address Setup Time	0°C ≤ T_A ≤ +70°C	−10		−10		−10		−10		ns
		−55°C ≤ T_A ≤ +85°C	0		0		0		NA		ns
tASR	Row Address Setup Time		0		0		0		0		ns
tCAC	Access Time from $\overline{CAS}$ (Note 6)			185		165		135		100	ns
tCAH	$\overline{CAS}$ LOW to Column Address Hold Time		85		75		55		45		ns
tCAS	$\overline{CAS}$ Pulse Width	0°C ≤ T_A ≤ +70°C	185	10,000	165	10,000	135	10,000	100	10,000	ns
		−55°C ≤ T_A ≤ +85°C	185	5000	165	5000	135	5000	NA	NA	ns
tCP	Page Mode $\overline{CAS}$ Precharge Time		100		100		80		60		ns
tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0°C ≤ T_A ≤ +70°C	−20		−20		−20		−20		ns
		−55°C ≤ T_A ≤ +85°C	0		0		0		NA		ns
tCSH	$\overline{CAS}$ Hold Time		300		250		200		150		ns
tCWD	$\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)		145		125		95		70		ns
tCWL	$\overline{WE}$ LOW to $\overline{CAS}$ HIGH Setup Time		100		85		70		50		ns
tDH	$\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7)		85		75		55		45		ns
tDHR	$\overline{RAS}$ LOW to Data In Valid Hold Time		200		160		120		95		ns
tDS	Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Setup Time (Note 7)		0		0		0		0		ns
tOFF	$\overline{CAS}$ HIGH to Output OFF Delay		0	60	0	60	0	50	0	40	ns
tPC	Page Mode Cycle Time		295		275		225		170		ns
tRAC	Access Time from $\overline{RAS}$ (Note 6)			300		250		200		150	ns
tRAH	$\overline{RAS}$ LOW to Row Address Hold Time		45		35		25		20		ns
tRAS	$\overline{RAS}$ Pulse Width	0°C ≤ T_A ≤ +70°C	300	10,000	250	10,000	200	10,000	150	10,000	ns
		−55°C ≤ T_A ≤ +85°C	300	5000	250	5000	200	5000	NA	NA	ns
tRC	Random Read or Write Cycle Time		460		410		375		320		ns
tRCD	$\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6)		35	115	35	85	25	65	20	50	ns
tRCH	Read Hold Time		0		0		0		0		ns
tRCS	Read Setup Time		0		0		0		0		ns
tREF	Refresh Interval			2		2		2		2	ms
tRMW	Read Modify Write Cycle Time		600		500		405		320		ns
tRP	$\overline{RAS}$ Precharge Time		150		150		120		100		ns
tRSH	$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay		185		165		135		100		ns
tRWC	Read/Write Cycle Time		525		425		375		320		ns
tRWD	$\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)		260		210		160		120		ns
tRWL	$\overline{WE}$ LOW to $\overline{RAS}$ HIGH Setup Time		100		85		70		50		ns
tT	Transition Time		3	50	3	50	3	50	3	35	ns
tWCH	Write Hold Time		85		75		55		45		ns
tWCR	$\overline{RAS}$ LOW to Write Hold Time		200		160		120		95		ns
tWCS	$\overline{WE}$ LOW to $\overline{CAS}$ LOW Setup Time (Note 9)	0°C ≤ T_A ≤ +70°C	−20		−20		−20		−20		ns
		−55°C ≤ T_A ≤ +85°C	0		0		0		NA		
tWP	Write Pulse Width		85		75		55		45		ns

Notes:
1. All voltages referenced to VSS.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low read data. Access timing will depend on the relative positions of their falling edges. When tRCD is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When tRCD is more than the maximum value shown access time depends on $\overline{CAS}$ and tCAC governs. The

Notes (Cont.)

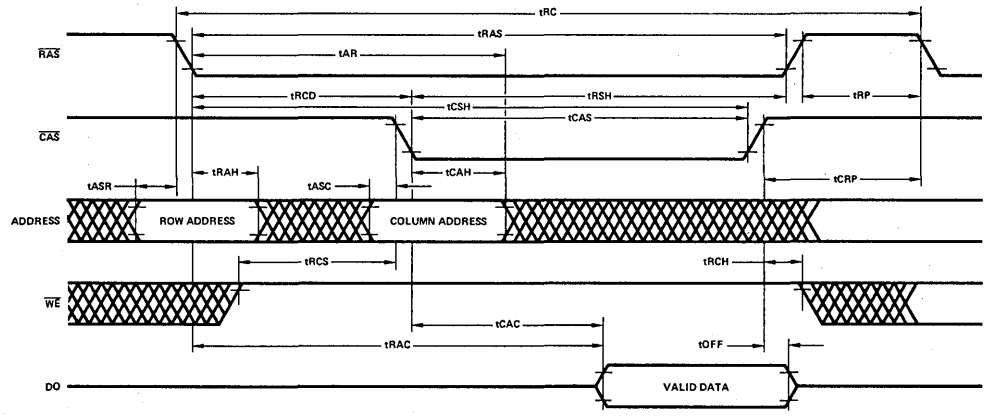
maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.

7. Timing reference points for data input setup and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least eight initialization cycles that exercise $\overline{RAS}$ should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part.

When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.

SWITCHING WAVEFORMS

READ CYCLE



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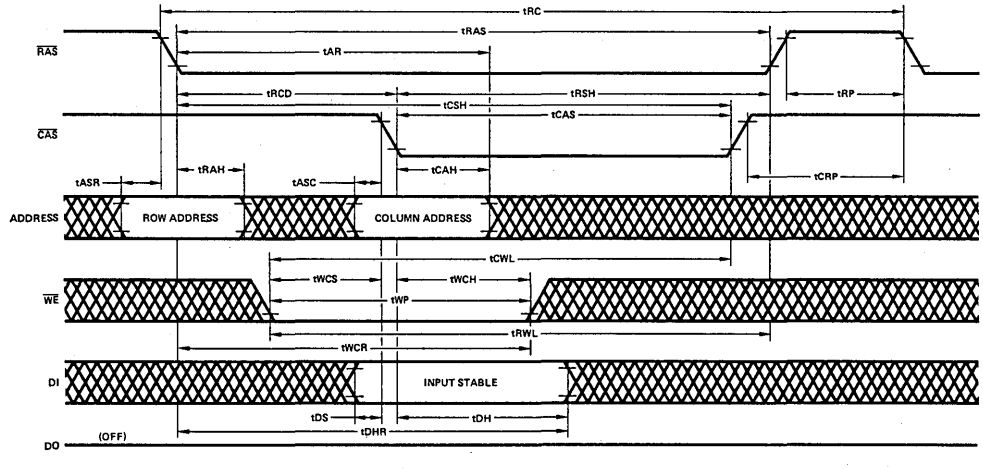
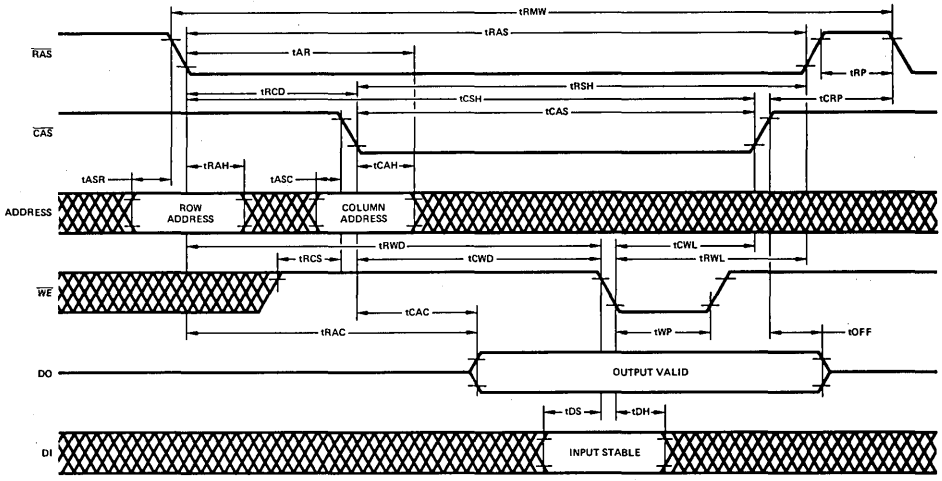
WRITE CYCLE (EARLY WRITE)



MOS-193

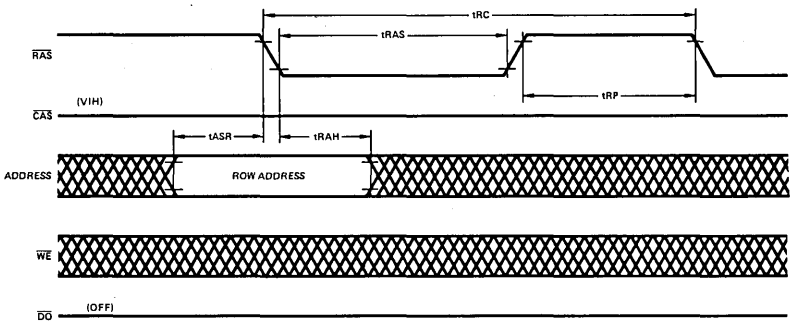
SWITCHING WAVEFORMS (Cont.)

READ-WRITE/READ-MODIFY-WRITE CYCLE



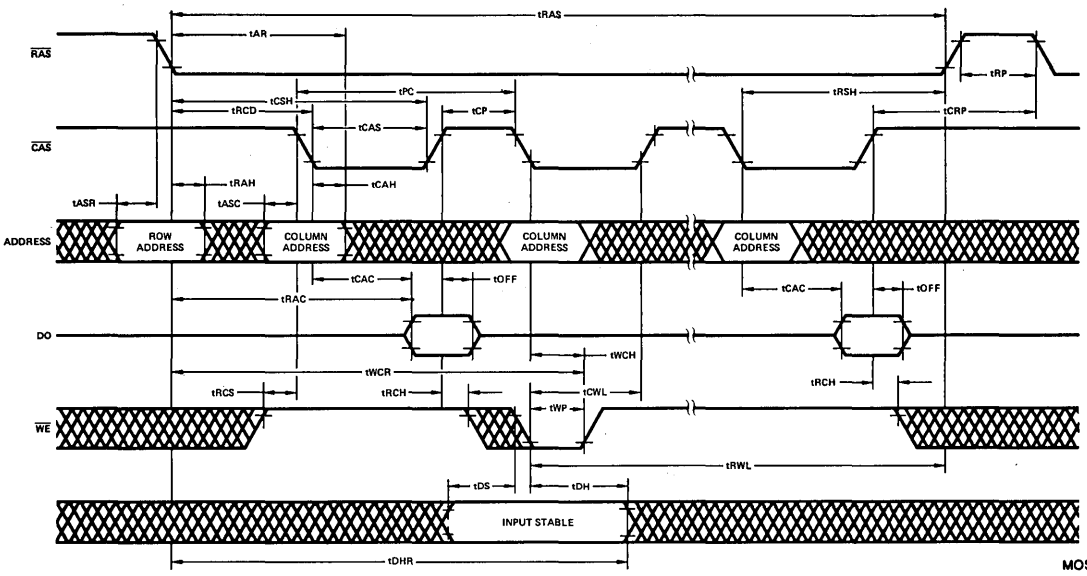
MOS-194

RAS ONLY REFRESH CYCLE



MOS-195

PAGE MODE CYCLE



MOS-196

APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4) $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise $\overline{RAS}$ before valid memory accesses are begun.

ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

DATA OUTPUT CONTROL

Any time $\overline{CAS}$ is high the data output will be off (after tOFF). The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

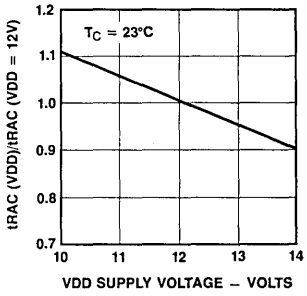
POWER CONSIDERATIONS

$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

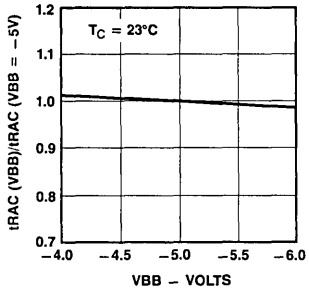
At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

TYPICAL CHARACTERISTICS

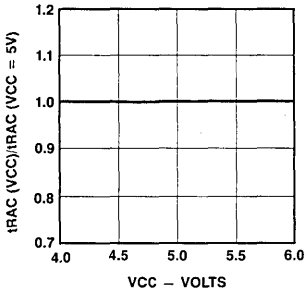
Typical Access Time (Normalized) tRAC Versus VDD



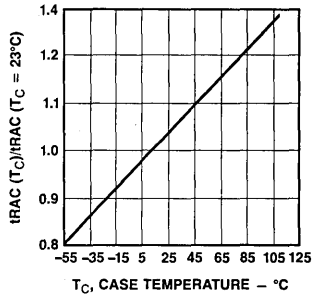
Typical Access Time (Normalized) tRAC Versus VBB



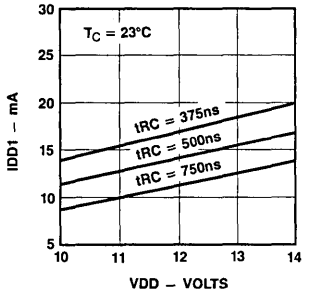
Typical Access Time (Normalized) tRAC Versus VCC



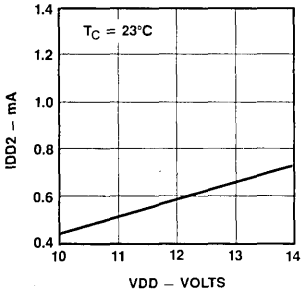
Typical Access Time (Normalized) tRAC Versus Case Temperature



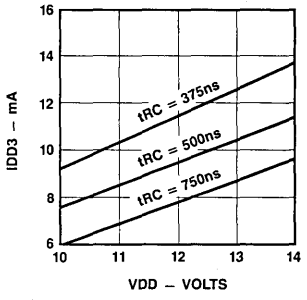
Typical Operating Current IDD1 Versus VDD



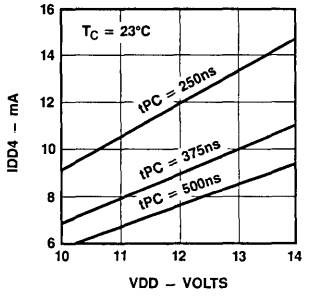
Typical Standby Current IDD2 Versus VDD



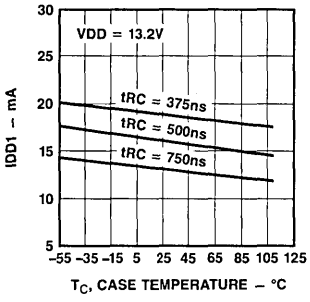
Typical Refresh Current IDD3 Versus VDD



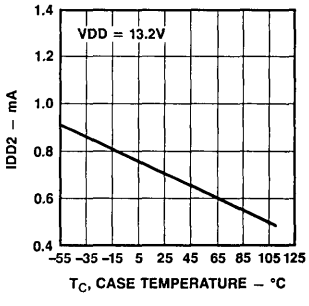
Typical Page Mode Current IDD4 Versus VDD



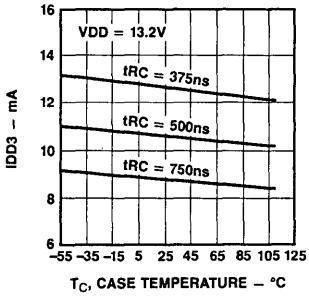
Typical Operating Current IDD1 Versus Case Temperature



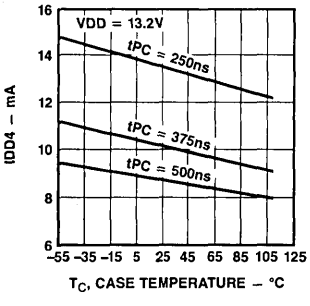
Typical Standby Current IDD2 Versus Case Temperature



Typical Refresh Current IDD3 Versus Case Temperature



Typical Page Mode Current IDD4 Versus Case Temperature



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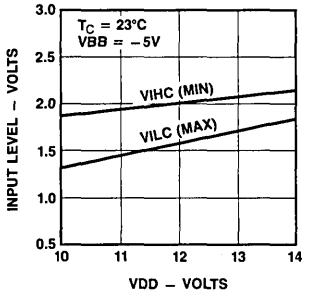
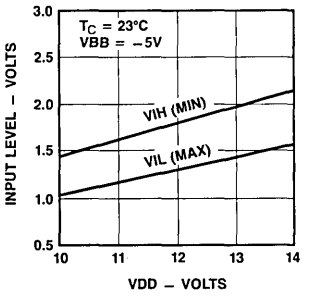
TYPICAL CHARACTERISTICS (Cont.)

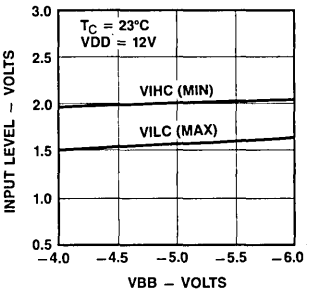
Input Voltage Levels Versus VDD



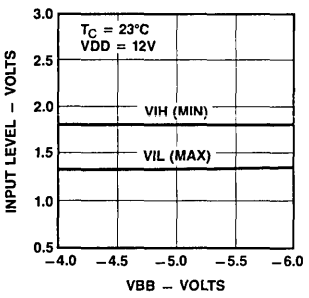
Input Voltage Levels Versus VDD



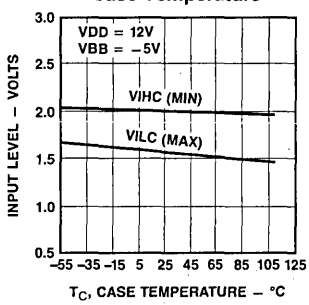
Input Voltage Levels Versus VBB



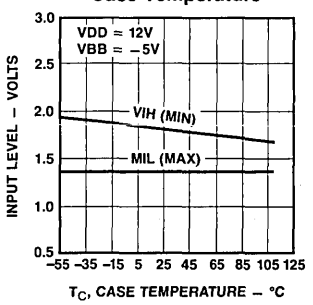
Input Voltages Levels Versus VBB



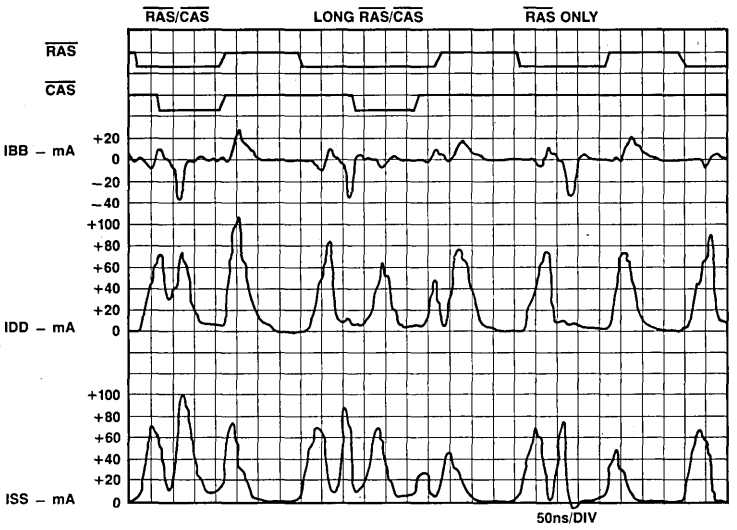
Input Voltage Levels Versus Case Temperature



Input Voltage Levels Versus Case Temperature



TYPICAL CURRENT WAVEFORMS



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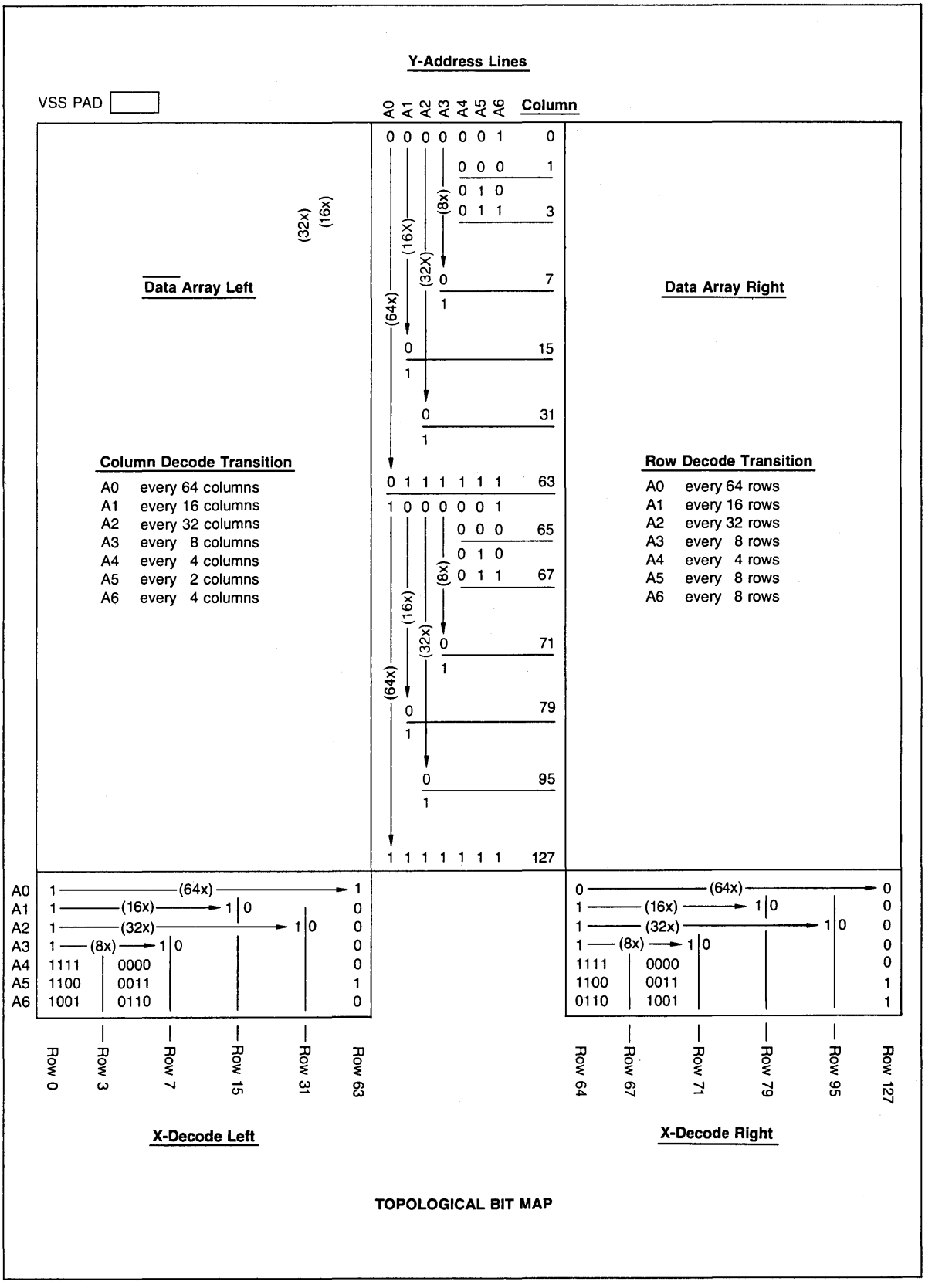
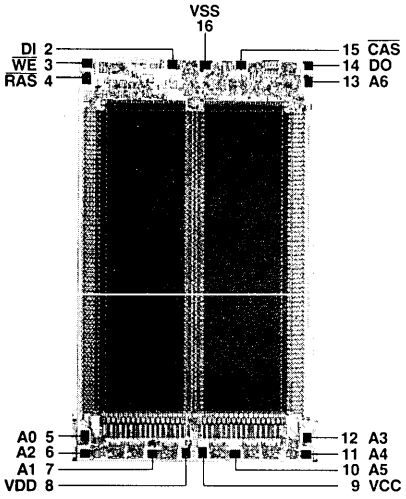


TOPOLOGICAL BIT MAP

ORDERING INFORMATION

Ambient Temperature	Package Type	Access Time			
		300ns	250ns	200ns	150ns
$0°C \leq T_A \leq +70°C$	Hermetic DIP	AM9016CDC	AM9016DDC	AM9016EDC	AM9016FDC
	Molded DIP	AM9016CPC	AM9016DPC	AM9016EPC	AM9016FPC
	Chip-Pak	AM9016CLC	AM9016DLC	AM9016ELC	AM9016FLC
$-55°C \leq T_A \leq +85°C$	Hermetic DIP	AM9016CDL	AM9016DDL	AM9016EDL	–
	Chip-Pak	AM9016CLL	AM9016DLL	AM9016ELL	–

Metallization and Pad Layout



DIE SIZE 0.107" X 0.205"

MOS Read Only Memories (ROM) Index

Am9218/8316E

2048 x 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- Plug-in replacement for 8316E
- Access times as fast as 350 ns
- Fully capacitive inputs – simplified driving
- 3 fully programmable Chip Selects – increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers – simplified expansion
- Drives two full TTL loads
- Single supply voltage – +5.0V
- Low power dissipation
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing
- Am2716 compatible

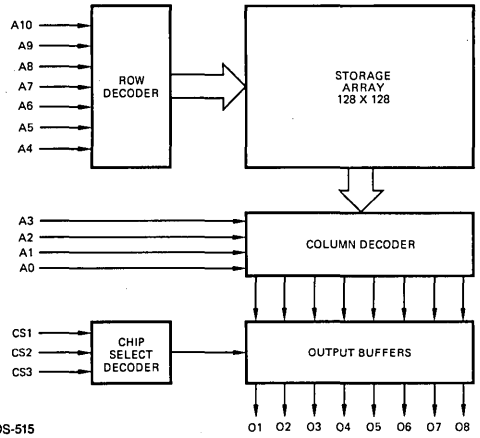
FUNCTIONAL DESCRIPTION

The Am9218 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 8 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9218 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

BLOCK DIAGRAM



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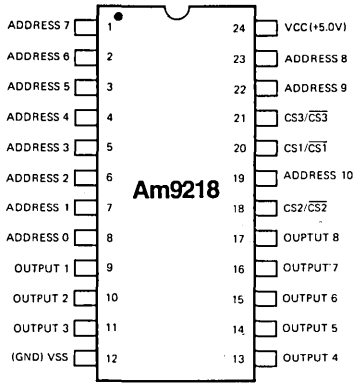
CONNECTION DIAGRAM



Top View

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Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		450ns	350ns
Molded	$0°C \leq T_A \leq 70°C$	AM9218BPC P8316E	AM9218CPC
Cerdip	$0°C \leq T_A \leq 70°C$	AM9218BCC	AM9218CCC
Side-Brazed Ceramic	$0°C \leq T_A \leq 70°C$	AM9218BDC C8316E	AM9218CDC
	$-55°C \leq T_A \leq +125°C$	AM9218BDM	

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	+7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

ELECTRICAL CHARACTERISTICS

Am9218BDC, Am9218CDC, C8316A: T_A = 0°C to +70°C; VCC = 5.0V ±5%

Parameters	Description	Test Conditions		Am9218XDC Min.	Am9218XDC Max.	C8316E Min.	C8316E Max.	Units
VOH	Output HIGH Voltage	9218	IOH = −200μA	2.4				Volts
		8316E	IOH = −100μA			2.4		
VOL	Output LOW Voltage	9218	IOL = 3.2mA		0.4			Volts
		8316E	IOL = 2.1mA				0.4	
VIH	Input HIGH Voltage			2.0	VCC + 1.0	2.0	VCC + 1.0	Volts
VIL	Input LOW Voltage			−0.5	0.8	−0.5	0.8	Volts
ILO	Output Leakage Current	Chip Disabled			10		10	μA
ILI	Input Leakage Current				10		10	μA
ICC	VCC Supply Current				70		95	mA

ELECTRICAL CHARACTERISTICS

Am9218BDM: T_A = −55°C to +125°C; VCC = 5.0V ±10%

Parameters	Description	Test Conditions	Am9218B Min.	Am9218B Max.	Units
VOH	Output HIGH Voltage	IOH = −200μA	2.2		Volts
VOL	Output LOW Voltage	IOL = 3.2mA		0.45	Volts
VIH	Input HIGH Voltage		2.0	VCC + 1.0	Volts
VIL	Input LOW Voltage		−0.5	0.8	Volts
ILO	Output Leakage Current	Chip Disabled		10	μA
ILI	Input Leakage Current			10	μA
ICC	VCC Supply Current			80	mA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

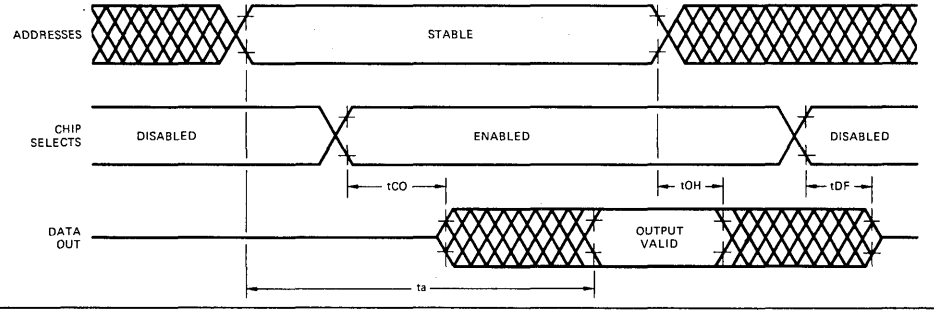
Am9218XDC/C8316E: T_A = 0°C to +70°C; VCC = 5.0V ± 5%

Am9218BDM: T_A = −55°C to +125°C; VCC = 5.0V ± 10%

Parameters	Description	Test Conditions	Am9218B Min.	Am9218B Max.	Am9218C Min.	Am9218C Max.	8316E Min.	8316E Max.	Units
ta	Address to Output Access Time	tr = tf = 20ns; Output Load: one standard TTL gate plus 100pF (Note 1)		450		350		450	ns
tCO	Chip Select to Output ON Delay			150		130		250	ns
tOH	Previous Read Data Valid with Respect to Address Change		20		20		–		ns
tDF	Chip Select to Output OFF Delay			150		130		250	ns
CI	Input Capacitance	T_A = 25°C, f = 1.0MHz; All pins at 0V		7.0		7.0		7.0	pF
CO	Output Capacitance			7.0		7.0		7.0	pF

Notes: 1. Timing reference levels: High = 2.0V, Low = 0.8V.

SWITCHING WAVEFORMS



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PROGRAMMING INSTRUCTIONS

CUSTOM PATTERN ORDERING INFORMATION

The Am9218 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.
Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0 V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	8316E or 9218
65 thru 72	Optional information

SECOND CARD

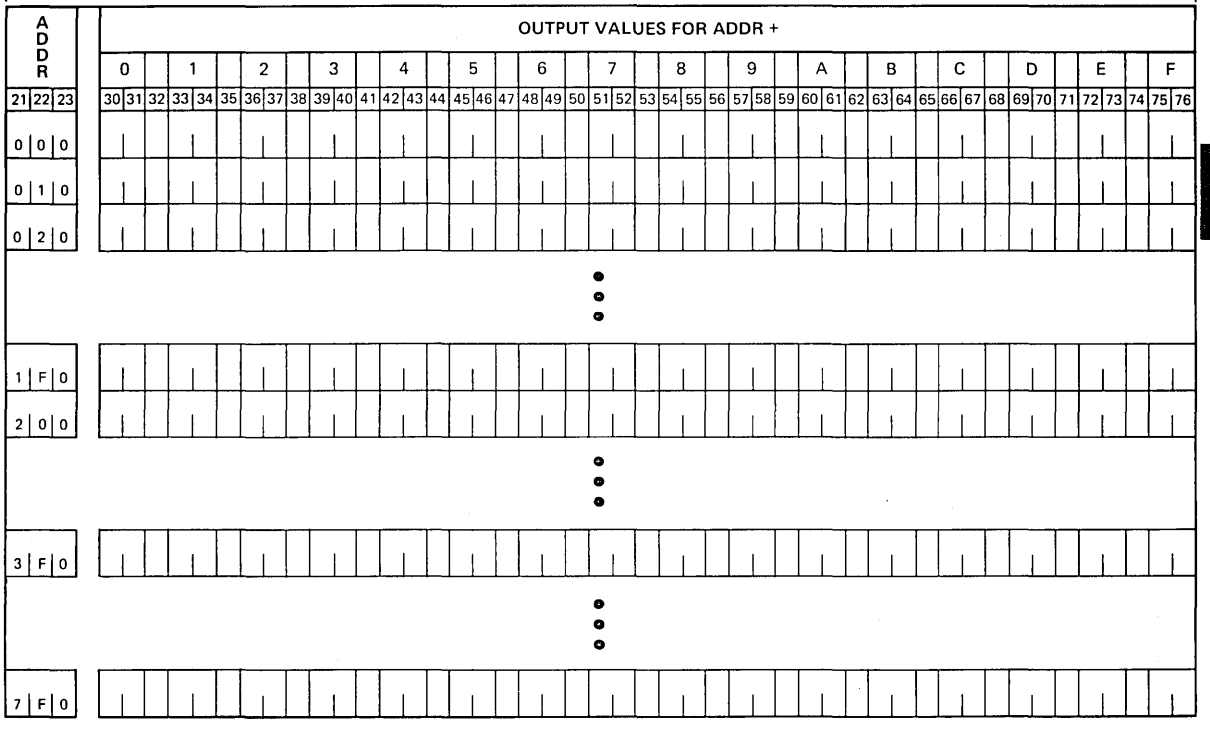
Column Number	Description
29	CS3 input required to select chip (0 or 1)
31	CS2 input required to select chip (0 or 1)
33	CS1 input required to select chip (0 or 1)

Two options are provided for entering the data pattern with the remaining cards.

OPTION 1 is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

Column Number	
10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30	Address input pattern with the most significant bit (A10) in column 10 and the least significant bit (A0) in column 30.
40, 42, 44, 46, 48, 50, 52, 54	Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

OPTION 2 is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.



Am9232 • Am9233

4096 x 8 Read Only Memory

DISTINCTIVE CHARACTERISTICS

- 4096 x 8 organization
- No clocks or refresh required
- Access time selected to 300ns
- Fully capacitive inputs – simplified driving
- Two mask programmable chip selects – increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers – simplified expansion
- Drives two TTL loads
- Single +5 volt power supply
- Two different pinouts for universal application
- Low power dissipation
- 100% MIL-STD-883 reliability assurance testing
- Non-connect option on chip selects

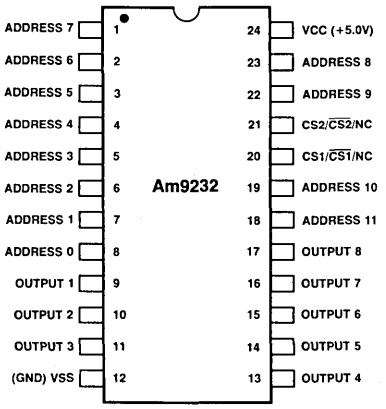
FUNCTIONAL DESCRIPTION

The Am9232/33 devices are high performance, 32,768-bit, static, mask programmed, read only memories. Each memory is implemented as 4096 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes of 4096 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9232/33 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

CONNECTION DIAGRAMS
Top Views



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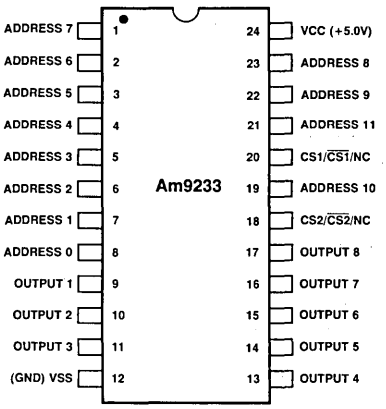

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Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time	
		450ns	300ns
Molded	$0°C \leq T_A \leq +70°C$	AM9232/33BPC	AM9232/33CPC
Cerdip	$0°C \leq T_A \leq +70°C$	AM9232/33BCC	AM9232/33CCC
Side-Brazed Ceramic	$-55°C \leq T_A \leq +125°C$	AM9232/33BDM	
	$0°C \leq T_A \leq +70°C$	AM9232/33BDC	AM9232/33CDC

MAXIMUM RATINGS beyond which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
VCC with Respect to VSS	+7.0V
DC Voltage Applied to Outputs	−0.5V to +7.0V
DC Input Voltage	−0.5V to +7.0V
Power Dissipation (Package Limitation)	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VCC	VSS
Am9232DC/PC/CC	$0°C \leq T_A \leq +70°C$	+5.0V ±5%	0V
Am9232/33DM	$-55°C \leq T_A \leq +125°C$	+5.0V ±10%	0V

ELECTRICAL CHARACTERISTICS over operating range

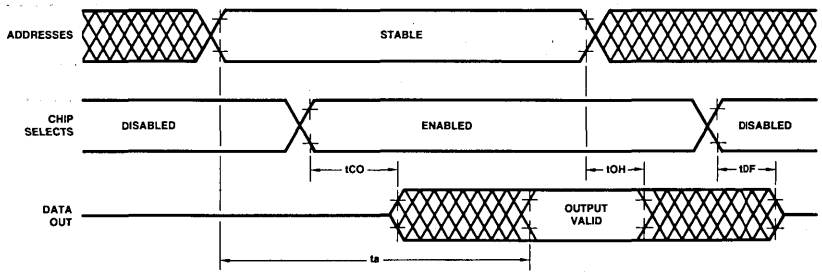
Parameter	Description	Test Conditions		Am9232/Am9233 Min.	Max.	Unit
VOH	Output HIGH Voltage	IOH = −200μA	VCC = 4.75	2.4		Volts
			VCC = 4.50	2.2		
VOL	Output LOW Voltage	IOL = 3.2mA			0.4	Volts
VIH	Input HIGH Voltage			2.0	VCC+1.0	Volts
VIL	Input LOW Voltage			−0.5	0.8	Volts
ILI	Input Load Current	VSS ≤ VI ≤ VCC			10	μA
ILO	Output Leakage Current	VSS ≤ VO ≤ VCC Chip Disabled	+70°C		10	μA
			+125°C (DM)		50	
ICC	VCC Supply Current		0°C		80	mA
			−55°C (DM)		100	
CI	Input Capacitance	T_A = 25°C, f = 1.0MHz All pins at 0V			7.0	pF
CO	Output Capacitance				7.0	pF

SWITCHING CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am9232/33B Min.	Am9232/33B Max.	Am9232/33C Min.	Am9232/33C Max.	Unit
ta	Address to Output Access Time	tr = tf = 20ns Output Load: one standard TTL gate plus 100pF (Note 1)		450		300	ns
tCO	Chip Select to Output ON Delay			150		120	ns
tOH	Previous Read Data Valid with Respect to Address Change		20		20		ns
tDF	Chip Select to Output OFF Delay			150		120	ns

Note 1. Timing reference levels: High = 2.0V, Low = 0.8V.

SWITCHING WAVEFORMS



MOS-105

PROGRAMMING INTRUCTIONS

CUSTOM PATTERN ORDERING INFORMATION

The Am9232 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.

Logic "1" = a more positive voltage (normally +5.0V)
Logic "0" = a more negative voltage (normally 0V)

FIRST CARD

Column Number	Description
10 thru 29	Customer Name
32 thru 37	Total number of "1's" contained in the data. This is optional and should be left blank if not used.
50 thru 62	9232 or 9233
65 thru 72	Optional information

SECOND CARD

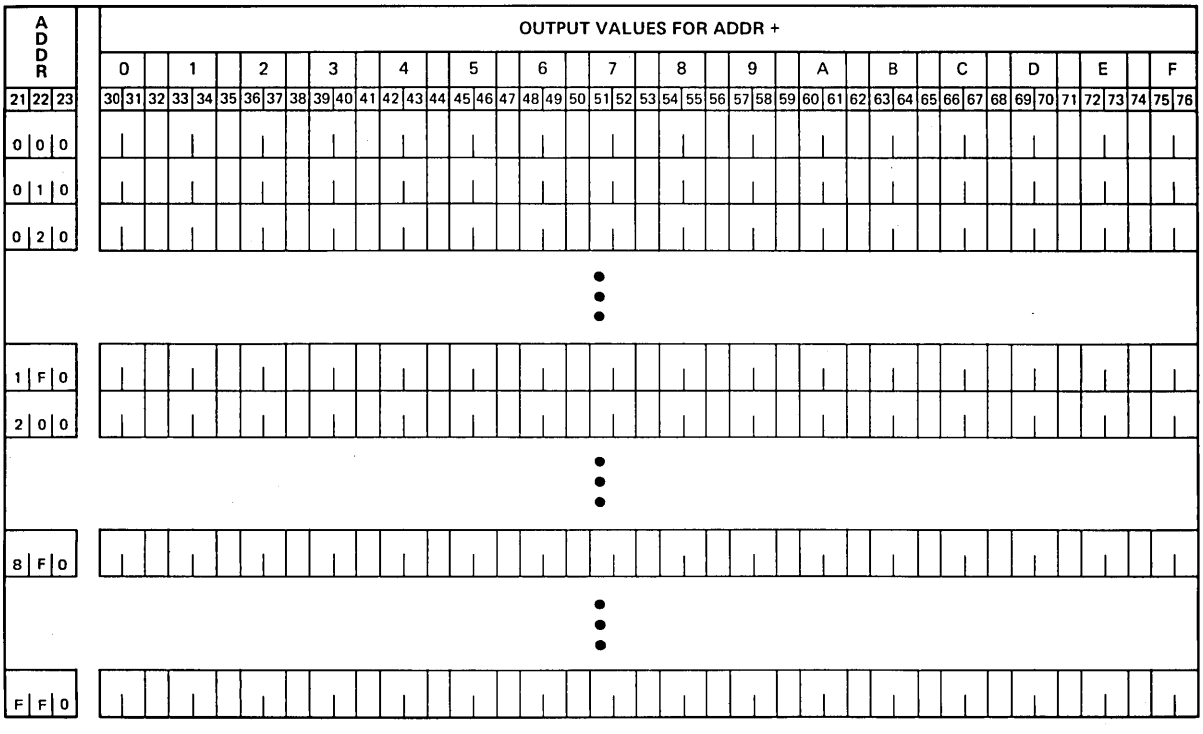
Column Number	Description
31	CS2 input required to select chip (0 or 1); If CS2 = NC, column 31 = 2.
33	CS1 input required to select chip (0 or 1); If CS1 = NC, column 33 = 2.

Two options are provided for entering the data pattern with the remaining cards.

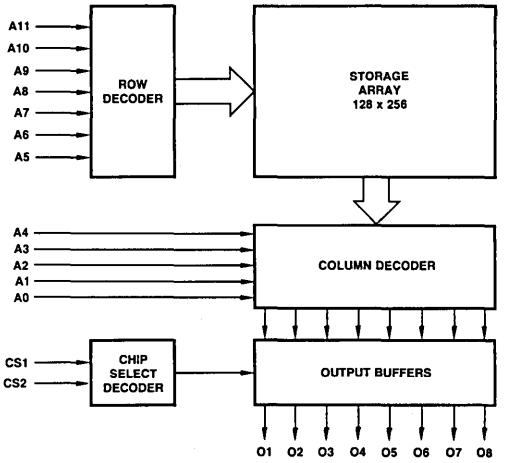
OPTION 1 is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 4096 data cards are required.

Column Number	
8, 10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30	Address input pattern with the most significant bit (A11) in column 8 and the least significant bit (A0) in column 30.
40, 42, 44, 46, 48 50, 52, 54	Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54.
73 thru 80	Coding these columns is not essential and may be used for card identification purposes.

OPTION 2 is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 256 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through FF:256 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.



Am9232/Am9233
BLOCK DIAGRAM



MOS-106

5

Am9264

64K (8192 x 8) Read Only Memory

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Enhanced manufacturability with post-metal programming
- Access time – 250ns (max)
- Single +5V ±10% power supply
- Fully static operation
- Completely TTL compatible
- Standard 24 pin DIP
- Pin compatible with 16K/32K/64K EPROMs/ROMs
- INT-STD-123 – guaranteed to 0.1%AQL
- Military version (−55 to +125°C) – Available – 450ns (max) access time

FUNCTIONAL DESCRIPTION

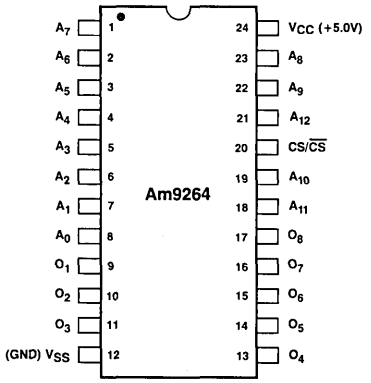
The Am9264 high performance read only memory is organized 8192 words by 8 bits with access times of less than 250ns. This organization simplifies the design of small memory systems and permits incremental memory sizes of 8192 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

The programmable chip select input signal is provided to control the output buffers. Chip Select Polarity may be provided by the customer thus allowing the addressing of 2 memory chips without external gating. The outputs of the unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9264 devices and other three state components.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) will result in faster turn around time for new or old patterns. This technique will allow us to test wafers before committing customer patterns to categorize speed and power dissipation requirements.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ROM-010

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time		
		450ns	300ns	250ns
Molded	$0°C \leq T_A \leq +70°C$	AM9264BPC	AM9264CPC	AM9264DPC
Cerdip	$0°C \leq T_A \leq +70°C$	AM9264BCC	AM9264CCC	AM9264DCC
Ceramic Side-Brazed	$0°C \leq T_A \leq +70°C$	AM9264BDC	AM9264CDC	AM9264DDC
	$-55°C \leq T_A \leq +125°C$	AM9264BDM		

MAXIMUM RATINGS beyond which the useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−55 to +125°C
V_{CC} with Respect to V_{SS}	+7.0V
DC Voltage Applied to Outputs	−0.5 to +7.0V
DC Input Voltage	−0.5 to +7.0V
Power Dissipation (Package Limitation)	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am9264DC/PC/CC	$0°C \leq T_A \leq +70°C$	+5.0V ±10%	0V
Am9264DM	$-55°C \leq T_A \leq +125°C$	+5.0V ±10%	0V

ELECTRICAL CHARACTERISTICS over operating range

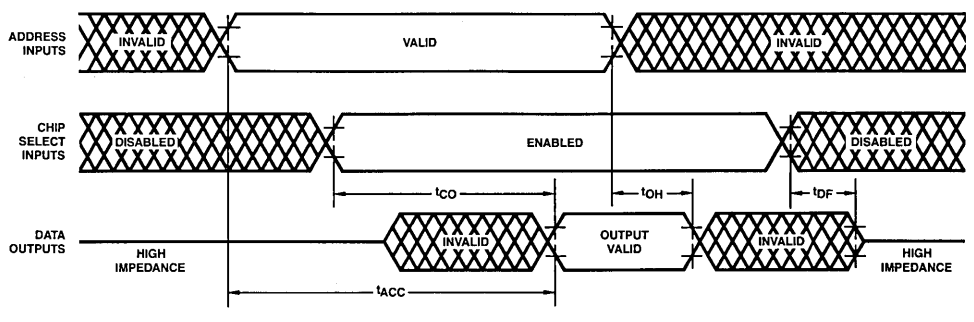
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$		2.4		Volts
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +1.0V	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	Volts
I_{LI}	Input Leakage Current	$V_{SS} \leq V_I \leq V_{CC}$			10	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_O \leq \leq V_{CC}$ Chip Disabled	+70°C		10	μA
			+125°C (DM)		50	
I_{CC}	V_{CC} Supply Current		0°C		80	mA
			−55°C (DM)		100	
C_I	Input Capacitance	$T_A = 25°C$, f = 1.0MHz			7.0	pF
C_O	Output Capacitance	All pins at 0V			7.0	

SWITCHING CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am9264B Min.	Am9264B Max.	Am9264C Min.	Am9264C Max.	Am9264D Min.	Am9264D Max.	Unit
T_A	Address to Output Access time	$t_r = t_f = 20ns$		450		300		250	ns
t_{CO}	Chip Select to Output on Delay	Output Load: one standard TTL gate plus 100pF (Note 1)		150		120		100	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change		20		20		20		ns
t_{DF}	Chip Select to Output OFF Delay			120		100		80	ns

Note 1: Timing reference levels: High = 2.0V. Low = 0.8V.

SWITCHING WAVEFORMS



ROM CODE DATA

EPROM

AMD's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs programmed with identical data should be submitted. AMD will read the programmed EPROM and generate an Intel Hex paper tape. The second EPROM is compared with Intel Hex paper tape to insure that both EPROMs have identical data. Then AMD generates a PG tape (Pattern Generation) which is used to make masks after customer gives a code approval. One of the EPROMs is erased and then it is programmed from AMD's data base. The AMD programmed EPROM is returned to the customer for code verification of the ROM program. Unless otherwise requested, AMD will not proceed until the customer verifies the program in the returned EPROM. AMD requests a written verification form (supplied by AMD with programmed EPROM) signed by customer before proceeding to any further work.

The following EPROMs should be used for submitting ROM CODE DATA:

ROM		EPROM	
		Preferred	Optional
Am9208	1K x 8	2708	—
Am9217/18	2K x 8	2716	2516/2-2708
Am9232/33	4K x 8	2732	2532/2-2716
Am9264	8K x 8	2764	4-2716/2-2732
Am9265	8K x 8	2764	4-2716/2-2732

If more than one EPROM is used to specify one ROM pattern, (i.e., 4 16K EPROMs or 2 32K EPROMs for one 64K ROM) two complete sets of programmed EPROMs should be submitted. In this instance, the programmed EPROMs must clearly state which of the two or four EPROMs is for lower and upper address locations in the ROM.

CARD FORMAT

If customer prefers to submit punch cards, be sure to provide the industry standard formats, such as:

AMD HEXADECIMAL (PREFERRED)
INTEL HEXADECIMAL
INTEL BPNF
MOTOROLA HEXADECIMAL
EA OCTAL
G.I. BINARY

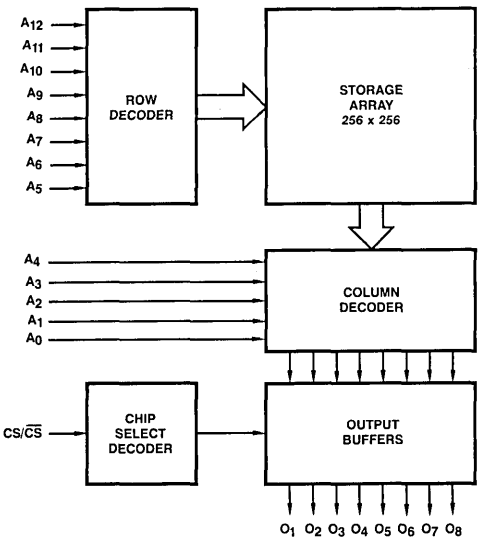
CHIP SELECT INFORMATION

Regardless of the method of submitting ROM CODE DATA (EPROM or CARDs), the chip select information must be specified at the time of customer input data. EPROMs do not have programmable chip selects and, therefore, cannot provide the required chip select information.

KEY POINTS

- Obtain AMD's 5 digit code number from product marketing
- Supply chip select information
- Supply customer part number and appropriate AMD part number
- Supply marking information
- Instruction on whether prototype approval is required prior to production or AMD is allowed to go straight to production (in case of code change or error, customer is liable for all products in line) after customer code approval.

BLOCK DIAGRAM



ROM-012

Am9265

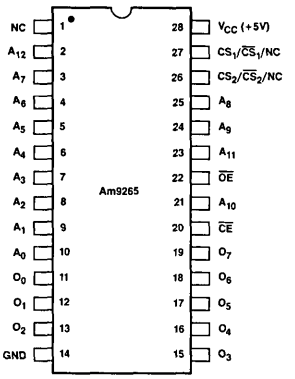
64K (8192 x 8) Read Only Memory

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Enhanced manufacturability with post metal programming
- Access time – 250ns (max)
- Fully static operation
- Single +5V ± 10% power supply
- Automatic power down feature controlled by separate $\overline{CE}$ pin.
  - 80mA max operating current
  - 20mA max standby current
- Separate $\overline{OE}$ pin for tri-state output control
- Two programmable chip selects with no-connect option
- Pin compatible with 28 pin 64K and higher density ROMs/EPROMs
- Completly TTL compatible
- Standard 28 pin DIP
- INT-STD-123 – guaranteed to 0.1% AQL.
- Military version (−55 to +125°C) – Available with 450ns (max) access time

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation ROM-001

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am9265DC/PC/CC	$0°C \leq T_A \leq +70°C$	+5.0V ±10%	0V
Am9265DM	$-55°C \leq T_A \leq +125°C$	+5.0V ±10%	0V

FUNCTIONAL DESCRIPTION

The Am9265 high performance read only memory is organized 8192 words by 8 bits with access times of less than 250ns. This organization simplifies the design of small memory systems and permits incremental memory sizes of 8192 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two programmable chip select inputs are provided to control the output buffers. Chip select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of the unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9265 devices and other three state components. No-connect option on chip selects can be provided if desired by the customer.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications. A separate $\overline{OE}$, output enable pin, controls outputs providing greater system flexibility and eliminating bus contention.

The Am9265 features an automatic stand-by mode. When deselected by $\overline{CE}$, the maximum supply current is reduced from 80mA to 20mA, a 75% reduction.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) results in faster turn around time for new or old patterns. This technique also allows testing of wafers to categorize speed and power dissipation before committing customer patterns.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time		
		450ns	300ns	250ns
Molded	$0°C \leq T_A \leq +70°C$	AM9265BPC	AM9265CPC	AM9265DPC
Cerdip	$0°C \leq T_A \leq +70°C$	AM9265BCC	AM9265CCC	AM9265DCC
Ceramic Side-Brazed	$0°C \leq T_A \leq +70°C$	AM9265BDC	AM9265CDC	AM9265DDC
	$-55°C \leq T_A \leq +125°C$	AM9265BDM		

MAXIMUM RATINGS beyond which the useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−55 to +125°C
V_{CC} with Respect to V_{SS}	+7.0V
DC Voltage Applied to Outputs	−0.5 to +7.0V
DC Input Voltage	−0.5 to +7.0V
Power Dissipation (Package Limitation)	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

ELECTRICAL CHARACTERISTICS over operating range

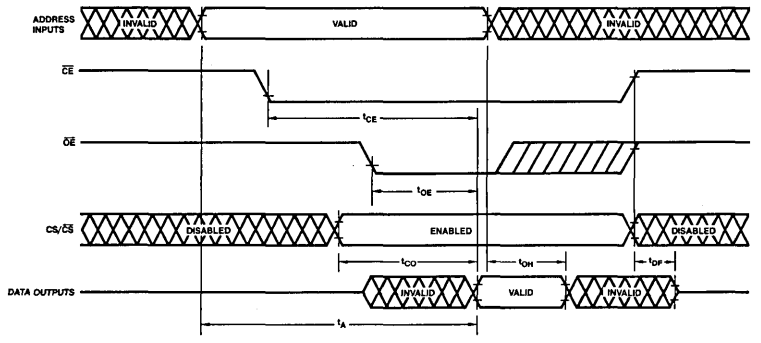
Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −400μA		2.4		Volts
V_{OL}	Ouput LOW Voltage	I_{OL} = 3.2mA			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +1.0V	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	Volts
I_{LI}	Input Leakage Current	$V_{SS} \leq V_I \leq V_{CC}$			10	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_O \leq V_{CC}$ Chip Disabled	+70°C		10	μA
			+125°C (DM)		50	
I_{CC1}	V_{CC} Standby Current		0°C		20	mA
			−55°C (DM)		25	
I_{CC2}	V_{CC} Operating Current		0°C		80	mA
			−55°C (DM)		100	
C_I	Input Capacitance	T_A = 25°C, f = 1.0MHz All pins at 0V			7.0	pF
C_O	Output Capacitance				7.0	pF

SWITCHING CHARACTERISTICS over operating range (see notes)

Parameter	Description	Test Conditions	Am9265B Min	Am9265B Max	Am9265C Min	Am9265C Max	Am9265D Min	Am9265D Max	Unit
t_A	Address to Output Access Time	tr = tf = 10ns Output Load One Standard TTL Gate Plus 100pF (Note 1)		450		300		250	ns
t_{CO}	Chip Select to Output ON Delay			150		120		100	ns
t_{OE}	Output Enable to Output ON Delay			150		120		100	ns
t_{CE}	$\overline{CE}$ to Output ON Delay			450		300		250	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change		20		20		20		ns
t_{DF}	Chip Select to Output OFF Delay			120		100		80	ns

Notes: 1. Timing reference levels: High = 2.0V Low = 0.8V.
2. t_{DF} is the worst case OFF delay. If $\overline{OE}$ occurs before $\overline{CE}$ and CS/$\overline{CS}$ are disabled, then t_{DF} is referenced to $\overline{OE}$ only. If $\overline{OE}$, CS/$\overline{CS}$ and $\overline{CE}$ are disabled simultaneously, then t_{DF} is referenced to all three.

SWITCHING WAVEFORMS



ROM-004

5

ROM CODE DATA

AMD's preferred method of receiving ROM code data is in EPROM. Two identically programmed EPROMs should be submitted for code verification purposes. AMD will read one of the EPROMs and store contents in a floppy disk. The contents of the second EPROM are compared with the stored data for consistency. The second EPROM is erased and then reprogrammed and submitted to the customer for verification of the ROM code, along with code listing. Unless otherwise requested, AMD will not proceed until production is authorized by means of a signed MOS ROM verification form (submitted with code verification data).

The following EPROMs should be used for submitting ROM code data:

ROM		EPROM	
		Preferred	Optional
Am9208	1K x 8	2708	–
Am9217/18	2K x 8	2716	2516/2-2708
Am9232/33	4K x 8	2732	2532/2-2716
Am9264	8K x 8	2764	4-2716/2-2732
Am9265	8K x 8	2764	4-2716/2-2732

If more than one EPROM is used to specify a ROM pattern, the upper and lower address locations must be clearly specified.

CARD FORMAT

If card decks are preferred as code inputs, the following industry standard formats are acceptable:

AMD HEXADECIMAL (PREFERRED)
INTEL HEXADECIMAL
INTEL BPNF
MOTOROLA HEXADECIMAL
EA OCTAL
GI BINARY

PAPER TAPE FORMAT

If punched paper tape is preferred as code input, most industry standard formats are acceptable. Verify with factory before submittal.

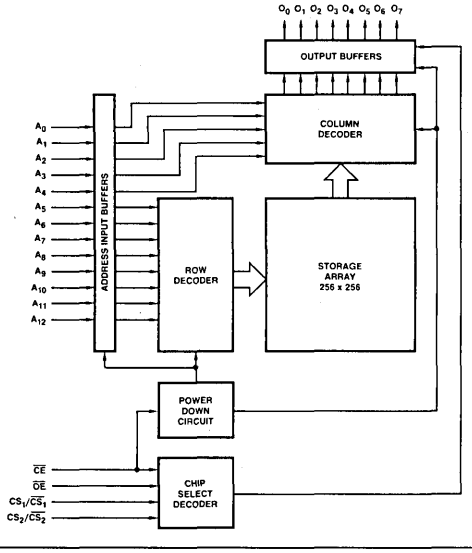
CHIP SELECT INFORMATION

Regardless of the method of submitting ROM code data, the chip select information must be specified at the time of customer input data. EPROMs do not have programmable chip selects and, therefore, cannot provide the required chip select information.

KEY POINTS

- Supply 2 sets of identically programmed EPROMs.
- Specify customer part number and appropriate AMD part number.
- Supply marking information.
- Identify upper and lower address location when more than one EPROM is used.
- Cover EPROM window with opaque material to prevent bit loss.

BLOCK DIAGRAM



ROM-003

Am92128

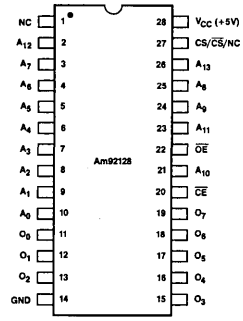
128K (16,384 x 8) Read Only Memory

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Enhanced manufacturability with post metal programming
- Access time – 250ns (max)
- Fully static operation
- Single +5V ± 10% power supply
- Automatic power down feature controlled by separate $\overline{CE}$ pin
  - 80mA max operating current
  - 25mA max standby current
- Separate $\overline{OE}$ pin for three-state output control
- Programmable chip select with no-connect option
- Pin compatible with 28-pin and high density ROMs/EPROMs
- TTL compatible
- Standard 28-pin DIP
- INT-STD-123 – guaranteed to 0.1% AQL
- Military version (−55 to +125°C) – Available with 450ns (max) access time

CONNECTION DIAGRAM
Top View



ROM-008

Note: Pin 1 is marked for orientation.

PIN NAMES

A_0-A_{13}	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5V
NC	No Connection	GND	Ground
CS/$\overline{CS}$	Chip Select	O_0-O_7	Data Outputs

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am92128 X PC/CC	$0°C \leq T_A \leq +70°C$	+5.0V ±10%	0V
Am92128BDM	$-55°C \leq T_A \leq +125°C$	+5.0V ±10%	0V

FUNCTIONAL DESCRIPTION

The Am92128 high performance read only memory is organized 16,384 words by 8 bits and has access times of less than 250ns. This organization simplifies the design of memory systems and permits incremental memory sizes of 16,384 bytes. The fast access times provided allow the ROM to service high performance microcomputer applications without inserting wait states.

One programmable chip select input is provided to control the output buffers. Chip select polarity may be specified by the customer thus allowing the addressing of 2 memory chips without external gating.The outputs of the unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am92128 devices and other three-state components. No-connect option on chip select can be provided if desired by the customer.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications. A separate $\overline{OE}$, output enable pin, controls outputs providing greater system flexibility and eliminating bus contention.

The Am92128 features an automatic stand-by mode. When deselected by $\overline{CE}$, the maximum supply current is reduced from 80mA to 25mA, a 70% reduction.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) results in faster turn around time for new or old patterns. This technique also allows testing of wafers to categorize speed and power dissipation before committing customer patterns.

TRUTH TABLE

$\overline{CS}$ or CS	$\overline{CE}$	$\overline{OE}$	Mode	Outputs	Power
H	L	L	X	Deselected	High-Z	Active
H	L	H	X	Deselected	High-Z	Standby
L	H	L	H	Inhibit	High-Z	Active
L	H	H	X	Deselected	High-Z	Standby
L	H	L	L	Read	D_{OUT}	Active

H = HIGH (≥ 2.0V)
L = LOW (≤ 0.8V)
X = Don't Care

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time 450ns	300ns	250ns
Molded	$0°C \leq T_A \leq +70°C$	Am92128BPC	Am92128CPC	Am92128DPC
Cerdip	$0°C \leq T_A \leq +70°C$	Am92128BCC	Am92128CCC	Am92128DCC
Side-Brazed	$+55°C \leq T_A \leq +125°C$	Am92128BDM		

5

MAXIMUM RATINGS beyond which the useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−55 to +125°C
V_{CC} with Respect to V_{SS}	+7.0V
DC Voltage Applied to Outputs	−0.5 to +7.0V
DC Input Voltage	−0.5 to +7.0V
Power Dissipation (Package Limitation)	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

ELECTRICAL CHARACTERISTICS over operating range

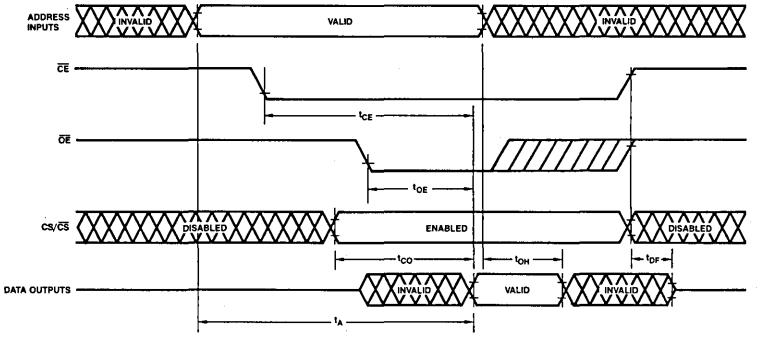
Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −400μA		2.4		Volts
V_{OL}	Ouput LOW Voltage	I_{OL} = 3.2mA			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +1.0V	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	Volts
I_{LI}	Input Leakage Current	$V_{SS} \leq V_I \leq V_{CC}$			10	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_O \leq V_{CC}$ Chip Disabled	+70°C		10	μA
			+125°C (DM)		50	
I_{CC1}	V_{CC} Standby Current		0°C		25	mA
			−55°C (DM)		30	
I_{CC2}	V_{CC} Operating Current		0°C		80	mA
			−55°C (DM)		100	
C_I	Input Capacitance	T_A = 25°C, f = 1.0MHz All pins at 0V			7.0	pF
C_O	Output Capacitance				7.0	pF

SWITCHING CHARACTERISTICS over operating range (see notes)

Parameter	Description	Test Conditions	Am92128B Min	Am92128B Max	Am92128C Min	Am92128C Max	Am92128D Min	Am92128D Max	Unit
t_A	Address to Output Access Time	tr = tf = 10ns Output Load One Standard TTL Gate Plus 100pF (Note 1)		450		300		250	ns
t_{CO}	Chip Select to Output ON Delay			150		120		100	ns
t_{OE}	Output Enable to Output ON Delay			150		120		100	ns
t_{CE}	$\overline{CE}$ to Output Delay			450		300		250	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change		20		20		20		ns
t_{DF}	Chip Select to Output OFF Delay			120		100		80	ns

Notes: 1. Timing reference levels: High = 2.0V Low = 0.8V.
2. t_{DF} is the worst case OFF delay. If $\overline{OE}$ occurs before $\overline{CE}$ and CS/$\overline{CS}$ are disabled, then t_{DF} is referenced to $\overline{OE}$ only. If $\overline{OE}$, CS/$\overline{CS}$, and $\overline{CE}$ are disabled simultaneously, then t_{DF} is referenced to all three.

SWITCHING WAVEFORMS



ROM-004

ROM CODE DATA

AMD's preferred method of receiving ROM code data is in EPROM. Two identically programmed EPROMs should be submitted for code verification purposes. AMD will read one of the EPROMs and store contents in a floppy disk. The contents of the second EPROM are compared with the stored data for consistency. The second EPROM is erased and then reprogrammed and submitted to the customer for verification of the ROM code, along with code listing. Unless otherwise requested, AMD will not proceed until production is authorized by means of a signed MOS ROM verification form (submitted with code verification data).

The following EPROMs should be used for submitting ROM code data:

ROM		EPROM	
		Preferred	Optional
Am9208	1K x 8	2708	–
Am9217/18	2K x 8	2716	2516/2-2708
Am9232/33	4K x 8	2732	2532/2-2716
Am9264	8K x 8	2764	4-2716/2-2732
Am9265	8K x 8	2764	4-2716/2-2732
Am92128	16K x 8	27128	2-2764

If more than one EPROM is used to specify a ROM pattern, the upper and lower address locations must be clearly specified.

CARD FORMAT

If card decks are preferred as code inputs, the following industry standard formats are acceptable:

AMD HEXADECIMAL (PREFERRED)
INTEL HEXADECIMAL
INTEL BPNF
MOTOROLA HEXADECIMAL
EA OCTAL
GI BINARY

PAPER TAPE FORMAT

If punched paper tape is preferred as code input, most industry standard formats are acceptable. Verify with factory before submittal.

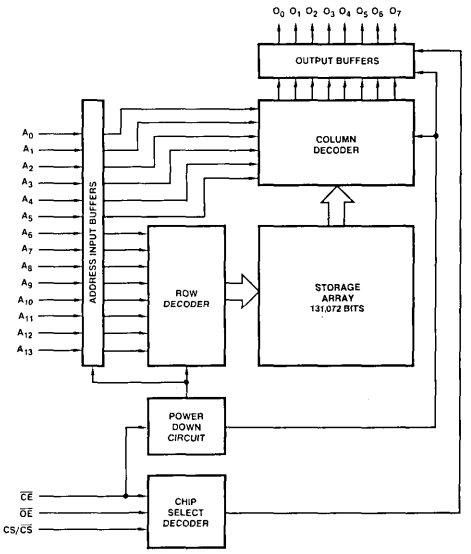
CHIP SELECT INFORMATION

Regardless of the method of submitting ROM code data, the chip select information must be specified at the time of customer input data. EPROMs do not have programmable chip selects and, therefore, cannot provide the required chip select information.

KEY POINTS

- Supply 2 sets of identically programmed EPROMs.
- Specify customer part number and appropriate AMD part number.
- Supply marking information.
- Identify upper and lower address location when more than one EPROM is used.
- Cover EPROM window with opaque material to prevent bit loss.

BLOCK DIAGRAM



ROM-009

Am92256

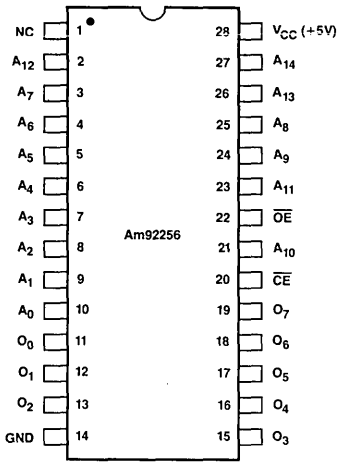
256K (32,768 x 8) Read Only Memory

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Enhanced manufacturability with post metal programming
- Access time – 250ns (max)
- Fully static operation
- Single +5V ± 10% power supply
- Automatic power down feature controlled by separate $\overline{CE}$ pin
  - 120mA max operating current
  - 30mA max standby current
- Separate $\overline{OE}$ pin for three-state output control
- Pin compatible with 28-pin high density ROMs/EPROMs
- TTL compatible
- Standard 28-pin DIP
- INT-STD-123 – guaranteed to 0.1% AQL

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation. ROM-005

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am92256PC/CC	$0°C \leq T_A \leq +70°C$	+5.0V ±10%	0V

FUNCTIONAL DESCRIPTION

The Am92256 high performance read only memory is organized 32,768 words by 8 bits and has access times of less than 250ns. This organization simplifies the design of memory systems and permits incremental memory sizes of 32,768 bytes. The fast access times provided allow the ROM to service high performance microcomputer applications without inserting wait states.

The Am92256 features an automatic stand-by mode. When deselected by $\overline{CE}$, the maximum supply current is reduced from 120mA to 30mA, a 75% reduction. The outputs of the deselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am92256 devices and other three-state components.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications. A separate $\overline{OE}$, output enable pin, controls outputs providing greater system flexibility and eliminating bus contention.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) results in faster turn around time for new or old patterns. This technique also allows testing of wafers to categorize speed and power dissipation before committing customer patterns.

PIN NAMES

$A_0 - A_{14}$	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5V
NC	No Connection	GND	Ground
		$O_0 - O_7$	Data Outputs

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	Mode	Outputs	Power
H	X	Deselect	High-Z	Standby
L	H	Inhibit	High-Z	Active
L	L	Read	D_{OUT}	Active

H = HIGH (≥ 2.0V)
L = LOW (≤ 0.8V)
X = Don't Care

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time		
		450ns	300ns	250ns
Molded	$0°C \leq T_A \leq +70°C$	Am92256BPC	Am92256CPC	Am92256DPC
Cerdip	$0°C \leq T_A \leq +70°C$	Am92256BCC	Am92256CCC	Am92256DCC

MAXIMUM RATINGS beyond which the useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−55 to +125°C
V_{CC} with Respect to V_{SS}	+7.0V
DC Voltage Applied to Outputs	−0.5 to +7.0V
DC Input Voltage	−0.5 to +7.0V
Power Dissipation (Package Limitation)	1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

ELECTRICAL CHARACTERISTICS over operating range

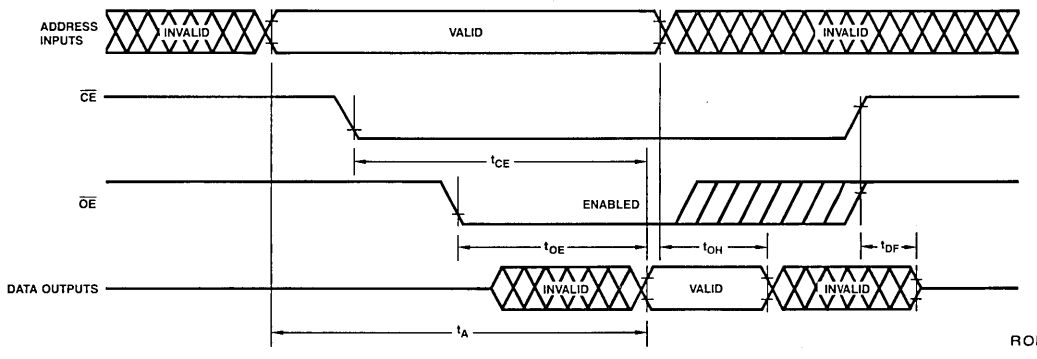
Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400\mu A$		2.4		Volts
V_{OL}	Ouput LOW Voltage	$I_{OL} = 3.2mA$			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +1.0V	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	Volts
I_{LI}	Input Leakage Current	$V_{SS} \leq V_I \leq V_{CC}$			10	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_O \leq V_{CC}$ Chip Disabled	+70°C		10	μA
I_{CC1}	V_{CC} Standby Current		0°C		30	mA
I_{CC2}	V_{CC} Operating Current		0°C		120	mA
C_I	Input Capacitance	$T_A = 25°C$, f = 1.0MHz All pins at 0V			7.0	pF
C_O	Output Capacitance				7.0	pF

SWITCHING CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am92256B Min	Am92256B Max	Am92256C Min	Am92256C Max	Am92256D Min	Am92256D Max	Unit
t_A	Address to Output Access Time	tr = tf = 10ns Output Load One Standard TTL Gate Plus 100pF (Note 1)		450		300		250	ns
t_{OE}	Output Enable to Output ON Delay			150		120		100	ns
t_{CE}	$\overline{CE}$ to Output ON Delay			450		300		250	ns
t_{OH}	Previous Read Data Valid with Respect to Address Change		20		20		20		ns
t_{DF}	Chip Select to Output OFF Delay			120		100		80	ns

Notes: 1. Timing reference levels: High = 2.0V Low = 0.8V.
2. t_{DF} is the worst case OFF delay. If $\overline{OE}$ occurs before $\overline{CE}$ is disabled, then t_{DF} is referenced to $\overline{OE}$ only. If $\overline{OE}$, and $\overline{CE}$ are disabled simultaneously, then t_{DF} is referenced to both.

SWITCHING WAVEFORMS



ROM-006

ROM CODE DATA

AMD's preferred method of receiving ROM code data is in EPROM. Two identically programmed EPROMs should be submitted for code verification purposes. AMD will read one of the EPROMs and store contents in a floppy disk. The contents of the second EPROM are compared with the stored data for consistency. The second EPROM is erased and then reprogrammed and submitted to the customer for verification of the ROM code, along with code listing. Unless otherwise requested, AMD will not proceed until production is authorized by means of a signed MOS ROM verification form (submitted with code verification data).

The following EPROMs should be used for submitting ROM code data:

ROM		EPROM	
		Preferred	Optional
Am9208	1K x 8	2708	–
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Am9232/33	4K x 8	2732	2532/2-2716
Am9264	8K x 8	2764	4-2716/2-2732
Am9265	8K x 8	2764	4-2716/2-2732
Am92128	16K x 8	27128	2-2764
Am92256	32K x 8	2-27128	4-2764

If more than one EPROM is used to specify a ROM pattern, the upper and lower address locations must be clearly specified.

CARD FORMAT

If card decks are preferred as code inputs, the following industry standard formats are acceptable:

AMD HEXADECIMAL (PREFERRED)
INTEL HEXADECIMAL
INTEL BPNF
MOTOROLA HEXADECIMAL
EA OCTAL
GI BINARY

PAPER TAPE FORMAT

If punched paper tape is preferred as code input, most industry standard formats are acceptable. Verify with factory before submittal.

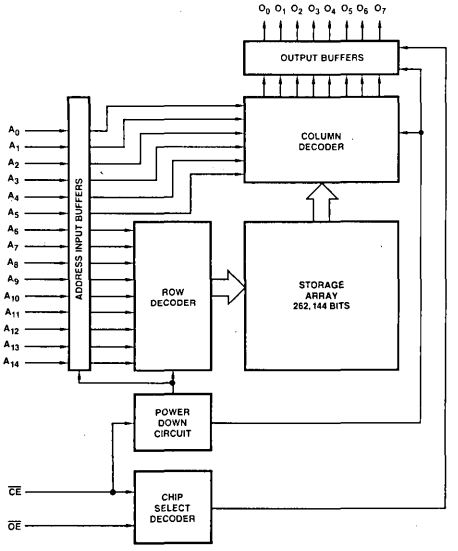
CHIP SELECT INFORMATION

Regardless of the method of submitting ROM code data, the chip select information must be specified at the time of customer input data. EPROMs do not have programmable chip selects and, therefore, cannot provide the required chip select information.

KEY POINTS

- Supply 2 sets of identically programmed EPROMs.
- Specify customer part number and appropriate AMD part number.
- Supply marking information.
- Identify upper and lower address location when more than one EPROM is used.
- Cover EPROM window with opaque material to prevent bit loss.

BLOCK DIAGRAM



ROM-007

MOS UV Erasable Programmable ROM (EPROM) Index

Am1702A

256-Word by 8-Bit Programmable Read Only Memory

DISTINCTIVE CHARACTERISTICS

- Field programmable 2048 bit ROM
- Access times down to 550 nanoseconds
- 100% tested for programmability
- Inputs and outputs TTL compatible
- Three-state output – wired-OR capability
- Typical programming time of less than 2 minutes/device
- Clocked VGG mode for lower power dissipation
- 100% MIL-STD-883 reliability assurance testing

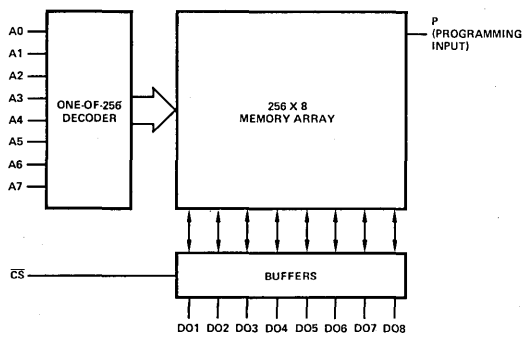
GENERAL DESCRIPTION

The Am1702A is a 2048-bit electrically programmable ultraviolet light erasable Read Only Memory. It is organized as 256 by 8 bits. It is packaged in a 24 pin dual in-line hermetic cerdip package with a foggy lid.

The transparent lid allows the user to erase any previously stored bit pattern by exposing the die to an ultraviolet (UV) light source. Initially, and after each erasure, all 2048 bits are in the zero state (output low). The data is selectively written into specified address locations by writing in ones.

A low power version, the Am1702AL, is available which permits the VGG input to be clocked for lower average power dissipation.

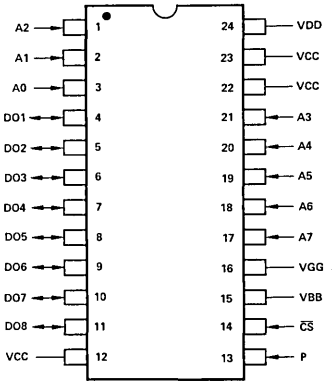
BLOCK DIAGRAM



MOS-372

CONNECTION DIAGRAM

Top View



Pin 1 is marked for orientation

MOS-373

ORDERING INFORMATION

Ambient Temperature Specification	Package Type	Clocked VGG	Access Time (ns)		
			1000	650	550
0°C to +70°C	Hermetic DIP Transparent Window	No	AM1702A	AM1702A-2	AM1702A-1
		Yes	AM1702AL	AM1702AL-2	AM1702AL-1
−55°C to +85°C	Hermetic DIP Transparent Window	No	AM9702AHDL	AM9702A-2HDL	AM9702A-1HDL
		Yes	AM9702ALHDL	AM9702AL-2HDL	AM9702AL-1DHL

6

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +85°C
Power Dissipation	1 W
Input and Supply Voltages (Operating)	VCC −20 V to VCC +0.5 V
Input and Supply Voltages (Programming)	−50 V

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE, Read Mode (Notes 1, 2)

Ambient Temperature	VCC	VDD	VGG	VBB
0°C to +70°C	+5.0V ±5%	−9.0V ±5%	−9.0V ±5%	+5.0V ±5%
−55°C to +85°C	+5.0V ±5%	−9.0V ±5%	−9.0V ±5%	+5.0V ±5%

ELECTRICAL CHARACTERISTICS over operating range (Note 3)

Parameter	Description	Test Conditions		Am1702A Am9702A Min.	Typ.	Max.	Am1702AL Am9702AL Min.	Typ.	Max.	Unit
ICF1	Output Clamp Current	T_A = 0°C, VO = −1.0V			8	14		5.5	8	mA
ICF2	Output Clamp Current	T_A = 25°C, VO = −1.0V				13		5	7	mA
IDD0	VDD Current (Note 4)	VGG = VCC, IOL = 0mA $\overline{CS}$ = VCC −2.0, T_A = 25°C						7	10	mA
IDD1		IOL = 0mA, $\overline{CS}$ = VCC −2.0, T_A = 25°C			35	50		35	50	mA
IDD2		IOL = 0mA, $\overline{CS}$ = 0, T_A = 25°C			32	46		32	46	mA
IDD3		IOL = 0mA, $\overline{CS}$ = VCC −2.0, T_A = 0°C			38	60		38	60	mA
IGG	VGG Current					1.0			1.0	μA
IL1	Input Leakage Current	VI = 0V				1.0			1.0	μA
ILO	Output Leakage Current	$\overline{CS}$ = VCC −2.0, VO = 0V				1.0			1.0	μA
IOH	Output Source Current	VO = 0V		−2.0			−2.0			mA
IOL	Output Sink Current	VO = 0.45V		1.6	4		2.0			mA
VIH	Input HIGH Level			VCC−2.0		VCC+0.3	VCC−2.0		VCC+0.3	Volts
VIL	Input LOW Level			−1.0		0.65	−1.0		0.65	Volts
VOH	Output HIGH Level	IOH = −200μA		3.5	4.5		3.5	4.5		Volts
VOL	Output LOW Level	IOL	1.6mA		−3.0	0.45				Volts
			2.0mA						0.4	

SWITCHING CHARACTERISTICS over operating range (Note 5)

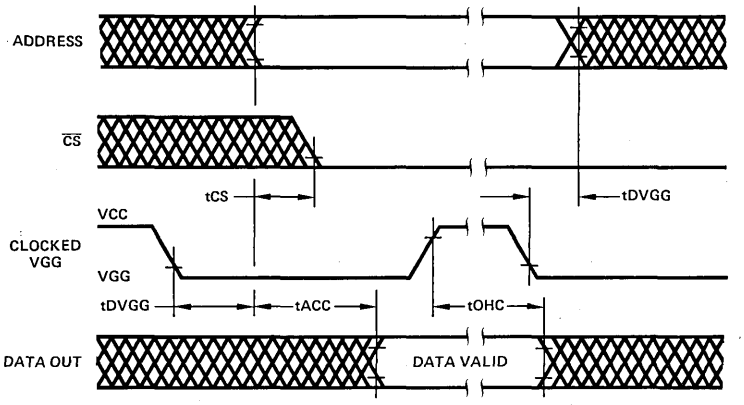
Parameter	Description	Am1702A-1 Am1702AL-1 Am9702A-1 Am9702AL-1 Min.	Max.	Am1702A-2 Am1702AL-2 Am9702A-2 Am9702AL-2 Min.	Max.	Am1702A Am1702AL Am9702A Am9702AL Min.	Max.	Unit
tACC	Address to Output Access Time		550		650		1000	ns
tCO	Output Delay from $\overline{CS}$		450		350		900	ns
t$\overline{CS}$	Chip Select Delay		100		300		100	ns
tDVGG	Set-up Time, VGG	0.3		0.3		0.4		μs
tOD	Output Deselect		300		300		300	ns
tDH	Previous Read Data Valid		100		100		100	ns
tOHC	Data Out Valid from VGG (Note 6)		5.0		5.0		5.0	μs
freq.	Repetition Rate		1.8		1.6		1.0	MHz

CAPACITANCE (Note 7)

Parameter	Description	Conditions	Typ.	Max.	Unit
CI	Input Capacitance	T_A = 25°C All unused pins are at VCC	8	15	pF
CO	Output Capacitance		10	15	pF
CVGG	VGG Capacitance			30	pF

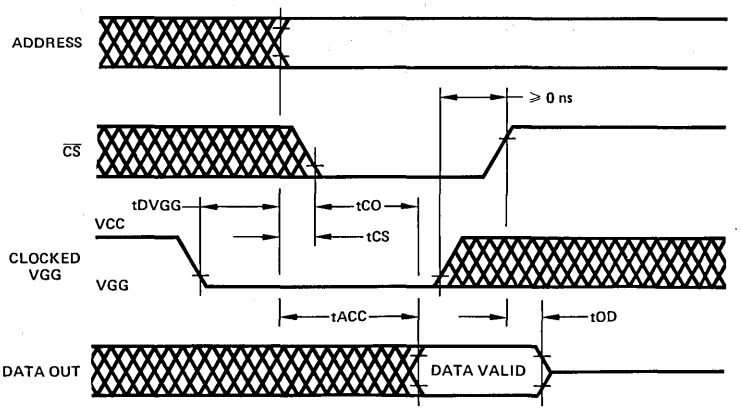
SWITCHING WAVEFORMS

READ OPERATION (Note 2)



MOS-374

DESELECTION



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CLOCKED VGG OPERATION (Note 1)

The VGG input may be clocked between +5V (VCC) and −9V to save power. To read the data, the chip select ($\overline{CS}$) must be low (≤ VIL) and the VGG level must be lowered to −9V at least tDVGG prior to the address selection. Once the data has appeared at the output and the access time has elapsed, VGG may be raised to +5V. The data output will remain stable for tOHC. To deselect the chip, $\overline{CS}$ is raised to ≥ VIH, and the output will go the high impedance state after tOD. The chip will be deselected when $\overline{CS}$ is raised to VIH whether the VGG is at +5V or at −9V.

6

PROGRAMMING THE Am1702A

Each storage node in the Am1702A consists of an MOS transistor whose gate is not connected to any circuit element. The transistors are all normally off, making all outputs LOW in an unprogrammed device. A bit is programmed to a HIGH by applying a large negative voltage to the MOS transistor; electrons tunnel through the gate insulation onto the gate itself. When the programming voltage is removed, a charge is left on the gate which holds the transistor on. Since the gate is completely isolated, there is no path by which the charge can escape, except for random high energy electrons which might retunnel through the gate insulation. Under ordinary conditions retunneling is not significant. The application of high energy to the chip through X-rays or UV light (via the quartz window) raises energy levels so that the charge can escape from the gate region, erasing the program and restoring the device to all LOW.

In order to program a specified byte, all 8 address lines must be in the binary complement of the address desired when pulsed VDD and VGG move to their negative level. The complemented address must be stable for at least tACW before VDD and VGG make their negative transitions. The voltage swing of the address lines during programming is between −47V ± 1V and 0V. The addresses must then make a transition to the true state at least tATW before the program pulse is applied. For good data retention, the addresses should be programmed in sequence from 0 to 255, a minimum of 32 times. DO1 through DO8 are used as the data inputs to program the desired pattern. A low level at the data input (−47V ± 1V) will program the selected bit to 1 and a high level (0V) will program it to a 0. All 8 bits addressed are programmed simultaneously.

Programming Boards are available for the Data I/O automatic programmer (part number 1010/1011), for the Spectrum Dynamics programmer (part number 434-549), and for the Pro-Log programmer (part number PM9001).

ERASING THE Am1702A

The Am1702A may be erased (restored to all LOW's) by exposing the die to ultraviolet light from a high intensity source. The recommended dosage is 6 W-sec/cm^2 at a wavelength of 2537 Å. The Ultraviolet Products, Inc., models UVS-54 or S-52 can erase the Am1702A in about 15 minutes, with the devices held one inch from the lamp. (Caution should be used when Am1702A's are inspected under fluorescent lamps after being programmed, as some fluorescent lamps may emit sufficient UV to erase or "soften" the PROM.)

CAUTION

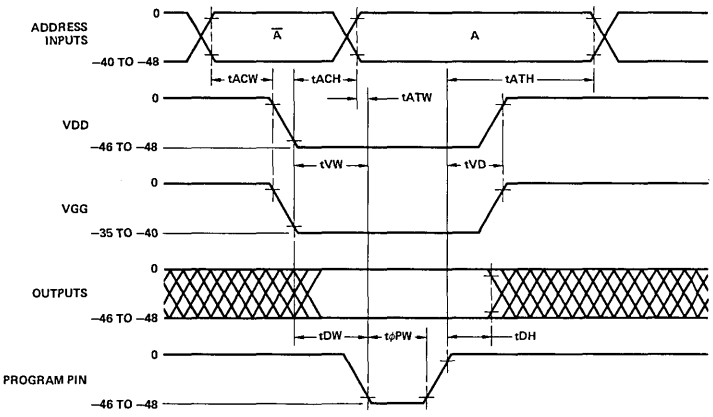
Ultraviolet radiation is invisible and can damage human eyes. Precautions should be taken to avoid exposure to direct or reflected ultraviolet radiation. It will often be convenient to fully enclose the ultraviolet source and the EROMs being erased to prevent accidental exposure.

Ultraviolet lamps can also ionize oxygen and create ozone which is harmful to humans. Erasing should be carried out in a well ventilated area in order to minimize the concentration of ozone.

PROGRAMMING REQUIREMENTS (Note 2)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
ILI1P	Input Current, Address and Data	VI = −48V			10	mA
ILI2P	Input Current, Program and VGG Inputs	VI = −48V			10	mA
IBB	VBB Current			0.05		mA
IDDP	IDD Current During Programming Pulse	VDD = VProg = −48V, VGG = −35V		200	Note 8	mA
VIHP	Input HIGH Voltage				0.3	Volts
VIL1P	Voltage Applied to Output to Program a HIGH		−46		−48	Volts
VIL2P	Input LOW Level on Address Inputs		−40		−48	Volts
VIL3P	Voltage Applied to VDD and Program Inputs		−46		−48	Volts
VIL4P	Voltage Applied to VGG Input		−35		−40	Volts
tϕPW	Programming Pulse Width	VGG = −35V, VDD = VProg = −48V			3.0	ms
tDW	Data Set-up Time		25			μs
tDH	Data Hold Time		10			μs
tVW	VGG and VDD Set-up Time		100			μs
tVD	VGG and VDD Hold Time		10		100	μs
tACW	Address Set-up Time (Complement)		25			μs
tACH	Address Hold Time (Complement)		25			μs
tATW	Address Set-up Time (True)		10			μs
tATH	Address Hold Time (True)		10			μs
	Duty Cycle				20	%

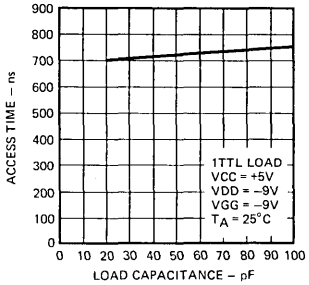
PROGRAMMING WAVEFORMS



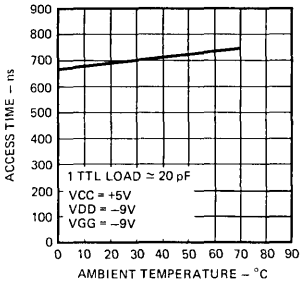
MOS-376

TYPICAL PERFORMANCE CURVES

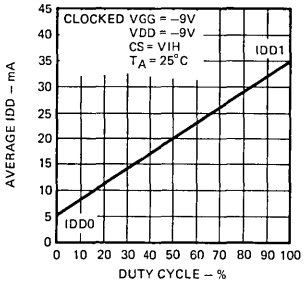
Access Time Versus Load Capacitance



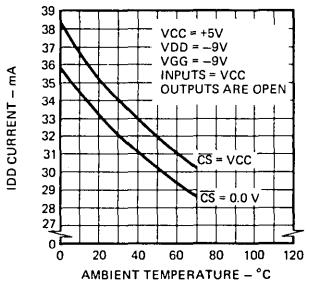
Access Time Versus Temperature



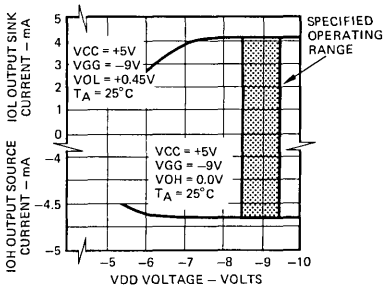
Average Current Versus Duty Cycle for Clocked VGG



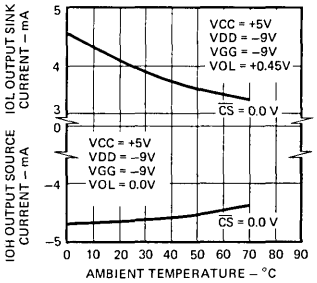
IDD Current Versus Temperature



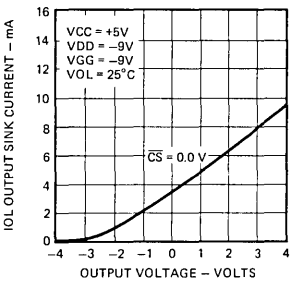
Output Current Versus VDD Supply Voltage



Output Current Versus Temperature



Output Sink Current Versus Output Voltage



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NOTES:

1. During read operations VGG may be clocked high to reduce power consumption. This involves swinging VGG up to VCC. See "Clocked VGG Operation". This mode is possible only with the Am1702AL.
2. During Read operations:
   Pins 12, 13, 15, 22, 23 = +5.0V ±5%
   Pins 16, 24 = −9.0V ±5%
   During Program operations:
   T_A = 25°C
   Pins 12, 22, 23 = 0V
   Pins 13, 24 are pulsed low from 0V to −47V ±1V
   Pin 15 = +12.0V ±10%
   Pin 16 is pulsed low from 0V to −37.5V ±2.5V
3. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
4. IDD may be reduced by pulsing the VGG supply between VCC and −9V. VDD current will be directly proportional to the VGG duty cycle. The data outputs will be unaffected by address or chip select changes while VGG is at VCC. For this option specify AM1702AL.
5. VIL = 0V, VIH = 4.0V, tr = tf ≤ 50ns, Load = 1 TTL gate.
6. The output will remain valid for tOHC after the VGG pin is raised to VCC, even if address change occurs.
7. These parameters are guaranteed by design and are not 100% tested.
8. Do not allow IDD to exceed 300mA for more than 100μsec.

Am9708/Am2708

1024 x 8 Erasable Read Only Memory

DISTINCTIVE CHARACTERISTICS

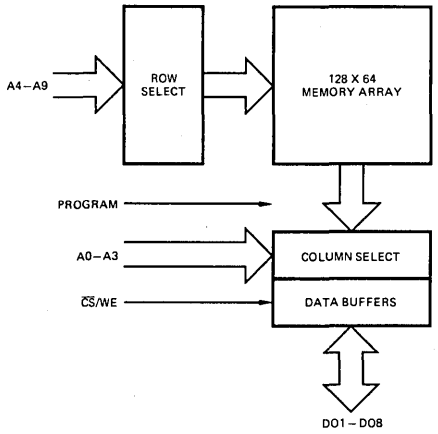
- Direct replacement for Intel 2708/8708
- Interchangeable with Am9208, Am9216 masked ROMs
- Full military temperature operation
- Fast programming time – typically 50sec
- TTL compatible interface signals
- Fully static operation – no clocks
- Fast access time – 350ns
- Three-state outputs
- Tested for 100% programmability
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am2708 is an 8,192-bit erasable and programmable MOS read-only memory. It is organized as 1024 words by 8 bits per word. Erasing the data in the EROM is accomplished by projecting ultraviolet light through a transparent window for a predetermined time period.

When the Chip Select/Write Enable input is at the high logic level, the device is unselected and the data lines are in their high impedance state. The device is selected when $\overline{CS}$/WE is at the low logic level. The contents of a particular memory location, specified by the 10 address lines, will be available on the data lines after the access time has elapsed. For programming, $\overline{CS}$/WE is connected to +12V and is used in conjunction with the Program input. The Address and Data lines are TTL compatible for all operating and programming modes.

BLOCK DIAGRAM



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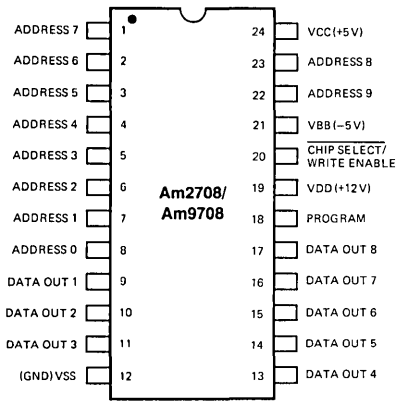
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Number
Hermetic DIP Transparent Window	$0°C \leq T_A \leq +70°C$	AM2708DC (450ns) AM2708-1DC (350ns)
Hermetic DIP Transparent Window	$-55°C \leq T_A \leq +125°C$	AM9708DM (480ns)

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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
All Signal Voltages, except Program and $\overline{CS}$/WE, with Respect to VBB	−0.3V to +15V
Program Input Voltage with Respect to VBB	−0.3V to +35V
$\overline{CS}$/WE Input with Respect to VBB	−0.3V to +20V
VCC and VSS with Respect to VBB	−0.3V to +15V
VDD with Respect to VBB	−0.3V to +20V
Power Dissipation	1.5W

The product described by this specification includes internal circuitry designed to protect input devices from excessive accumulation of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to any voltages that exceed the maximum ratings.

OPERATING RANGE

Ambient Temperature	VDD	VCC	VBB	VSS
0°C to +70°C	+12V ±5%	+5V ±5%	−5V ±5%	0V
−55°C to +125°C	+12V ±10%	+5V ±10%	−5V ±10%	0V

PROGRAMMING CONDITIONS

Ambient Temperature	VDD	VCC	VBB	VSS	$\overline{CS}$/WE	VIHP
+25°C	+12V ± 5%	+5V ± 5%	−5V ± 5%	0V	+12V ± 5%	26V ± 1V

READ OPERATION
ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 7)

Parameters	Description	Test Conditions		Min.	Typ.	Max.	Units
VIL	Input LOW Voltage			VSS		0.65	Volts
VIH	Input HIGH Voltage	T_A = 0°C to +70°C		3.0		VCC+1	Volts
		T_A = −55°C to +125°C		2.4		VCC+1	Volts
VOL	Output LOW Voltage	IOL = 1.6mA				0.45	Volts
VOH	Output HIGH Voltage	IOH = − 100μA		3.7			Volts
		IOH = −1.0mA		2.4			Volts
ILI	Address and Chip Select Input Load Current	VSS ≤ VIN ≤ VCC			1.0	10	μA
ILO	Output Leakage Current	VOUT = Worst Case $\overline{CS}$/WE = + 5.0V			1.0	10	μA
IDD	VDD Supply Current	All inputs HIGH. $\overline{CS}$/WE = +5.0V	T_A = 0°C		50	65	mA
			T_A = −55°C			80	
ICC	VCC Supply Current		T_A = 0°C		6.0	10	mA
			T_A = −55°C			15	
IBB	VBB Supply Current		T_A = 0°C		30	45	mA
			T_A = −55°C			60	
PD	Power Dissipation	T_A = 70°C				800	mW
CIN	Input Capacitance	T_A = 25°C f = 1MHz All pins at 0V			4.0	6.0	pF
COUT	Output Capacitance				8.0	12.0	pF

READ OPERATION
SWITCHING CHARACTERISTICS over operating range (Notes 2, 7)

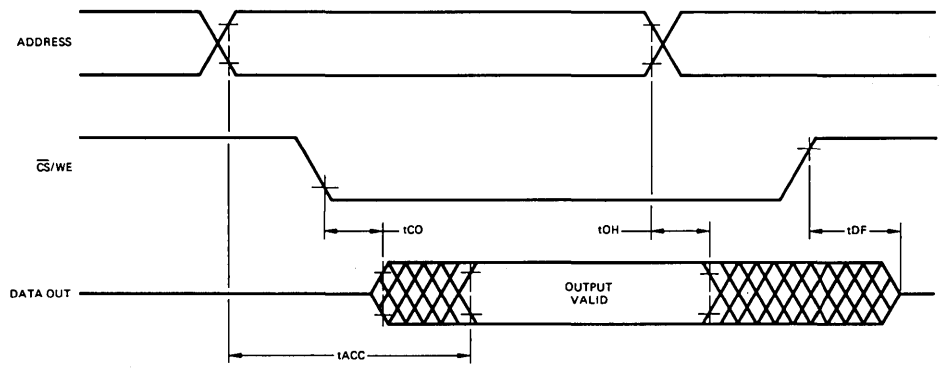
Parameters	Description	Test Conditions	0°C ≤ T_A ≤ 70°C Min.	0°C ≤ T_A ≤ 70°C Max.	−55°C ≤ T_A ≤ +125°C Min.	−55°C ≤ T_A ≤ +125°C Max.	Units
tACC	Address to Output Access Time (Note 3)	tr = tf ≤ 20ns Output Load: One Standard TTL Gate Plus 100pF		2708: 450 2708-1: 350		480	ns
tCO	Chip Select to Output on Delay (Note 4)			120		150	ns
tDF	Chip Select to Output OFF Delay		0	120	0	150	
tOH	Previous Read Data Valid with Respect to Address Change		0		0		

PROGRAMMING CHARACTERISTICS under programming conditions

Parameter	Description	Min.	Max.	Units
tAS	Address Set Up Time	10		μs
tCSS	$\overline{CS}$/WE Set Up Time	10		μs
tDS	Data Set Up Time	10		μs
tAH	Address Hold Time (Note 5)	1.0		μs
tCH	$\overline{CS}$/WE Hold Time (Note 5)	0.5		μs
tDH	Data Hold Time	1.0		μs
tDF	Chip Select to Output Off Delay	0	120	ns
tDPR	Program to Read Delay		10	μs
tPW	Program Pulse Width	0.1	1.0	ms
tPR, tPF	Program Pulse Transition Times	0.5	2.0	μs
VIHW	$\overline{CS}$/WE Input High Level	11.4	12.6	Volts
VIHP	Program Pulse High Level (Note 6)	25	27	Volts
VILP	Program Pulse Low Level (Note 6)	VSS	1.0	Volts

SWITCHING WAVEFORMS

READ CYCLE



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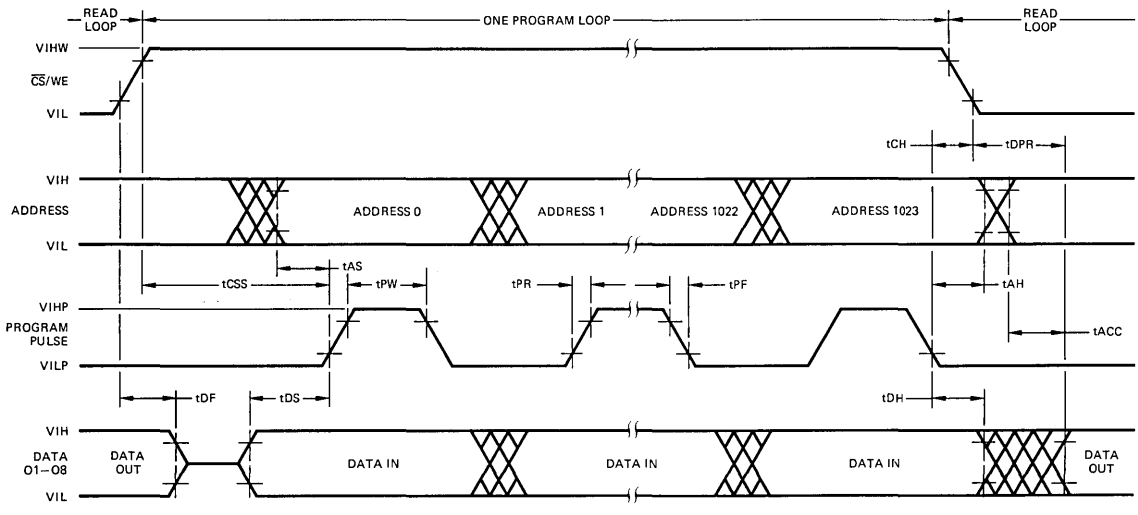
PROGRAM MODE (Note 5)



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PROGRAMMING THE Am2708

All 8192 bits of the Am2708 are in the logic HIGH state after erasure. When any of the output bits are programmed, the output state will change from HIGH to LOW. Programming of the device is initiated by raising the $\overline{CS}$/WE input to +12V. A memory location is programmed by addressing the device and supplying 8 data bits in parallel to the data out lines. When address and data bits are set up, a programming pulse is applied to the program input. All addresses are programmed sequentially in a similar manner. One pass through all 1024 addresses is considered one program loop. The number of program loops (N) required to complete the programming cycle is a function of the program pulse width (tPW) such that N $\geqslant$ 100ms/tPW requirement is met. Do not apply more than one program pulse per address without sequentially programming all other addresses. There should be N successive loops through all locations. The Program pin will source the IIPL current when it is low (VILP) and $\overline{CS}$/WE is high (VIHW). The Program pin should be actively pulled down to maintain its low level.

ERASING THE Am2708

The Am2708 can be erased by exposing the die to high-intensity, short-wave, ultra-violet light at a wavelength of 2537 angstroms through the transparent lid. The recommended dosage is ten watt-seconds per square centimeter. This erasing condition can be obtained by exposing the die to model S-52 ultraviolet lamp manufactured by Ultra-Violet Products, Inc. or Product Specialties, Inc. for approximately 20 to 30 minutes from a distance of about 2.5 centimeters above the transparent lid. The light source should not be operated with a short-wave filter installed. All bits will be in a logic HIGH state when erasure is complete.

CAUTION

Ultraviolet radiation is invisible and can damage human eyes. Precautions should be taken to avoid exposure to direct or reflected ultraviolet radiation. It will often be convenient to fully enclose the ultraviolet source and the EROMs being erased to prevent accidental exposure.

Ultraviolet lamps can also ionize oxygen and create ozone which can be harmful to humans. Erasing should be carried out in a well ventilated area in order to minimize the concentration of ozone.

NOTES:

1. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
2. Timing reference levels (Read) —
   Inputs: High = 2.8V (DC), 2.2V (DM); Low = 0.8V
   Outputs: High = 2.4V, Low = 0.8V
3. Typical access time is 280ns.
4. Typical chip select to output on delay is 60ns.
5. tAH must be greater than tCH.
6. VIHP – VILP $\geqslant$ 25 Volts.
7. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

Am2716/Am9716

2048 x 8-Bit UV Erasable PROM

MILITARY, INDUSTRIAL AND COMMERCIAL

DISTINCTIVE CHARACTERISTICS

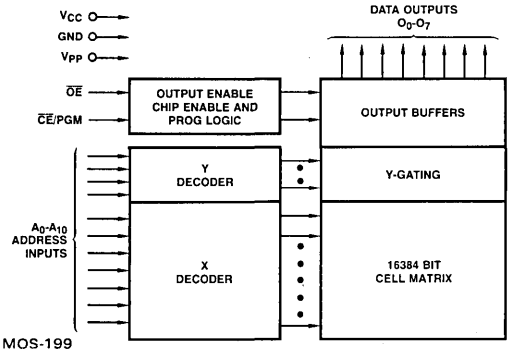
- 0.3% AQL guaranteed
- Direct replacement for Intel 2716
- Interchangeable with Am9218 – 16K ROM
- Single +5V power supply
- Fast access time – 450ns standard with 300ns, 350ns and 390ns options
- Low power dissipation
  - 525mW active
  - 132mW standby
- Fully static operation – no clocks
- Three-state outputs
- TTL compatible inputs/outputs
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am2716/Am9716 is a 16384-bit ultraviolet erasable and programmable read-only memory. It is organized as 2048 words by 8 bits per word, operates from a single +5V supply, has a static standby mode and features fast single address location programming.

Because the Am2716/Am9716 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 100 seconds.

BLOCK DIAGRAM



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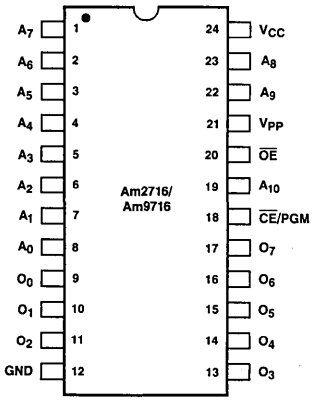
MODE SELECTION

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

CONNECTION DIAGRAMS – Top Views

DIP



Note: Pin 1 is marked for orientation

A_0-A_{10}: Addresses
O_0-O_7: Outputs
$\overline{CE}$/PGM: Chip Enable/Program
$\overline{OE}$: Output Enable

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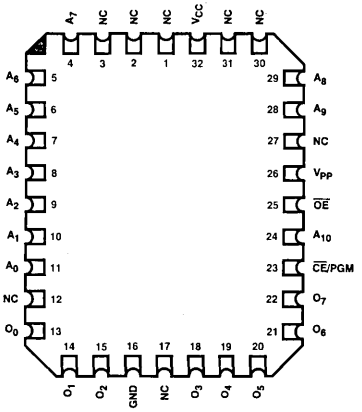
Chip-Pak™ L-32-2



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Chip-Pak is a trademark of Advanced Micro Devices, Inc.

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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−65 to +135°C
Voltage on All Inputs/Outputs (except V_{PP}) with Respect to GND	+6V to −0.3V
Voltage on V_{PP} During Program with Respect to GND	+26.5V to −0.3V

DC AND AC READ OPERATIONS CONDITIONS (Notes 1, 2)

	Temperature Range	V_{CC}	V_{PP}
AM2716DC/AM2716-2DC	0 to +70°C	5V ± 5%	V_{PP} (Note 2) = V_{CC} For all device types
AM9716DC/AM2716-1DC	0 to +70°C	5V ± 10%	
AM2716DI/AM2716-1DI	−40 to +85°C	5V ± 5%	
AM2716DL/AM2716-1DL	−55 to +100°C	5V ± 10%	
AM2716DM	−55 to +125°C	5V ± 10%	

DC CHARACTERISTICS

Parameters	Description	Test Conditions	Min Values	Maximum Values			Units
			All Types	DL/DM	DI	DC	
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ (Max) and $V_{IN} = 0$		10	10	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ (Max) and $V_{OUT} = 0$		10	10	10	μA
I_{PP1} (Note 2)	V_{PP} Current	$V_{PP} = V_{CC}$ (Max)		5	5	5	mA
I_{CC1} (Note 2)	V_{PP} Current (Standby)	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$		30	30	25	mA
I_{CC2} (Note 2)	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$		115	110	100	mA
V_{IL}	Input Low Voltage		−0.1	0.8	0.8	0.8	Volts
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V_{CC}+1	V_{CC}+1	Volts
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA @ V_{CC} (Min)		0.45	0.45	0.45	Volts
V_{OH}	Output High Voltage	I_{OH} = −400μA @ V_{CC} (Min)	2.4				Volts

AC CHARACTERISTICS

Parameters	Description	Test Conditions (Note 3)	Min Values	Maximum Values						Units
			All Types	9716 DC	2716-1 DC	2716-2 DC	2716 DC	2716-1 DI/DL	2716 DI/DL/DM	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		300	350	390	450	350	450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		300	350	390	450	350	450	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		120	120	120	120	150	150	ns
t_{DF}	Output Enable High to Output Float	$\overline{CE} = V_{IL}$	0	100	100	100	100	130	130	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0							ns

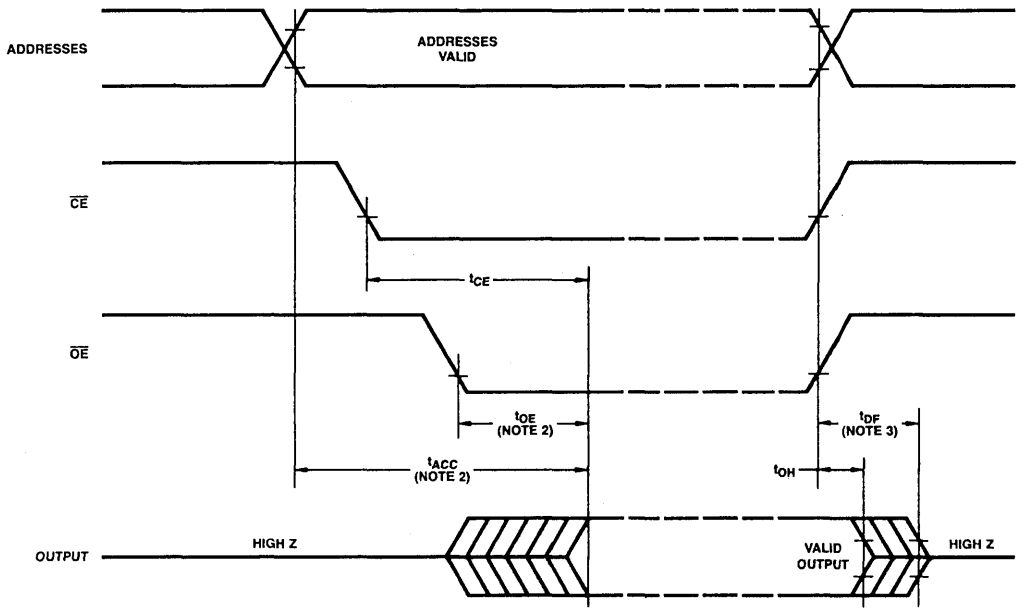
CAPACITANCE (Note 4)

T_A = +25°C, f = 1MHz

Parameters	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Other Test Conditions: a) Output Load: 1 TTL gate and C_L = 100pF
   b) Input Rise and Fall Times: ≤20ns
   c) Input Pulse Levels: 0.8 to 2.2V
   d) Timing Measurement Reference Level:
      Inputs: 1V and 2V
      Outputs: 0.8V and 2V
4. This parameter is only sampled and is not 100% tested.

AC WAVEFORMS (Note 1)



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Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

ORDERING INFORMATION

Ambient Temperature Specification	Order Number	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)
$0°C \leq T_A \leq 70°C$	AM9716DC	300	300	120
	AM9716LC			
	AM2716-1DC	350	350	120
	AM2716-1LC			
	AM2716-2DC	390	390	120
	AM2716-2LC			
	AM2716DC	450	450	120
	AM2716LC			
$-40°C \leq T_A \leq +85°C$	AM2716-1DI	350	350	150
	AM2716-1LI			
	AM2716DI	450	450	150
	AM2716LI			
$-55°C \leq T_A \leq +100°C$	AM2716-1DL	350	350	150
	AM2716-1LL			
	AM2716DL	450	450	150
	AM2716LL			
$-55°C \leq T_A \leq +125°C$	AM2716DM	450	450	150
	AM2716LM			

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PROGRAM OPERATION

DC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (Note 1) = 5V ±5%, V_{PP} (Notes 1, 2) = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
I_{LI}	Input Current	V_{IN} = 5.25/0.45V		10	μA
I_{PP1}	V_{PP} Supply Current	$\overline{CE}$/PGM = V_{IL}		5	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$/PGM = V_{IH}		30	mA
I_{CC}	V_{CC} Supply Current			100	mA
V_{IL}	Input Low Level		−0.1	0.8	Volts
V_{IH}	Input High Level		2.0	V_{CC}+1	Volts

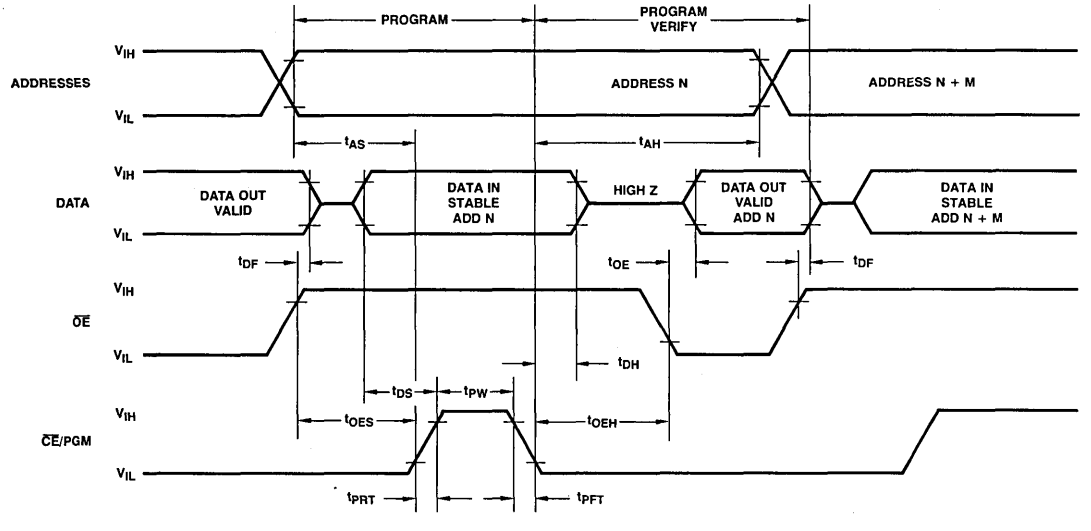
AC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (Note 1) = 5V ±5%, V_{PP} (Notes 1, 2) = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
t_{AS}	Address Set-up Time	Input t_R and t_F (10% to 90%) = 20ns Input Signal Levels = 0.8 to 2.2V Input Timing Reference Level = 1V and 2V Output Timing Reference Level = 0.8V and 2V	2		μs
t_{OES}	Output Enable Set-up Time		2		μs
t_{DS}	Data Set-up Time		2		μs
t_{AH}	Address Hold Time		2		μs
t_{OEH}	Output Enable Hold Time		2		μs
t_{DH}	Data Hold Time		2		μs
t_{DF}	Output Disable to Output Float Delay ($\overline{CE}$/PGM = V_{IL})		0	120	ns
t_{OE}	Output Enable to Output Delay ($\overline{CE}$/PGM = V_{IL})		–	120	ns
t_{PW}	Program Pulse Width		45	55	ms
t_{PRT}	Program Pulse Rise Time		5	–	ns
t_{PFT}	Program Pulse Fall Time		5	–	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} must not be greater than 26 volts including overshoot. Permanent device damage may occur if the device is taken out of or put into the socket when V_{PP} = 25 volts is applied. Also, during $\overline{OE}$ = $\overline{CE}$/PGM = V_{IH}, V_{PP} must not be switched from 5 volts to 25 volts or vice versa.

PROGRAMMING WAVEFORMS



MOS-202

ERASING THE Am2716/Am9716

In order to clear all locations of their programmed contents, it is necessary to expose the Am2716/Am9716 to an ultraviolet light source. A dosage of 15 Wseconds/cm^2 is required to completely erase an Am2716/Am9716. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å)] with intensity of 12000μW/cm^2 for 15 to 20 minutes. The Am2716/Am9716 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2716/Am9716, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to florescent light and sunlight will eventually erase the Am2716/Am9716, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING THE Am2716/Am9716

Upon delivery, or after each erasure the Am2716/Am9716 has all 16384 bits in the "1," or high state. "0s" are loaded into the Am2716/Am4716 through the procedure of programming.

The programming mode is entered when +25V is applied to the V_{PP} pin and when $\overline{OE}$ is at V_{IH}. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL high level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC level to the $\overline{CE}$/PGM input is prohibited when programming.

READ MODE

The Am2716/Am9716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}) for all devices. Data is available at the outputs 120ns or 150ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The Am2716/Am9716 has a standby mode which reduces the active power dissipation by 75%, from 525mW to 132mW (values for 0 to +70°C). The Am2716/Am9716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAM INHIBIT

Programming of multiple Am2716/Am9716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2716/Am9716s may be common. A TTL level program pulse applied to an Am2716/Am9716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that Am2716/Am9716. A low level $\overline{CE}$/PGM input inhibits the other Am2716/Am9716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at V_{CC}.

Am2732

4096 x 8-Bit UV Erasable PROM

Military, Industrial and Commercial

DISTINCTIVE CHARACTERISTICS

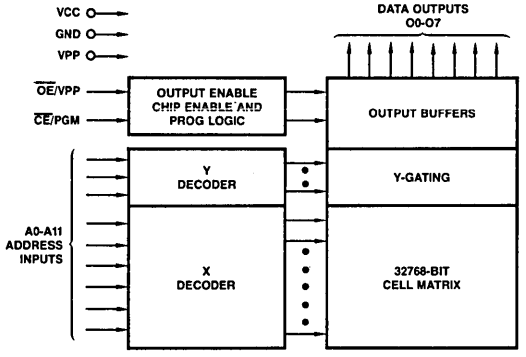
- 0.3% AQL guaranteed
- Direct replacement for Intel 2732
- Pin compatible with Am9233 – 32K ROM
- Single +5V power supply
- Fast access time – 350ns and 450ns
- Low power dissipation
  - –787mW active
  - –157mW standby
- Fully static operation – no clocks
- Three-state outputs
- TTL compatible inputs/outputs
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am2732 is a 32768-bit ultraviolet erasable and programmable read-only memory. It is organized as 4096 words by 8 bits per word, operates from a single +5V supply, has a static standby mode, and features fast single address location programming.

Because the Am2732 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 200 seconds.

BLOCK DIAGRAM



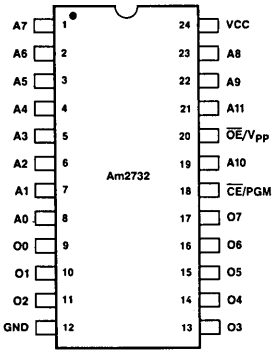
MOS-490

MODE SELECTION

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$/VPP (20)	VCC (24)	Outputs (9-11, 13-17)
Read	VIL	VIL	+5	DOUT
Standby	VIH	Don't Care	+5	High Z
Program	VIL	VPP	+5	DIN
Program Verify	VIL	VIL	+5	DOUT
Program Inhibit	VIH	VPP	+5	High Z

CONNECTION DIAGRAMS – Top Views

DIP

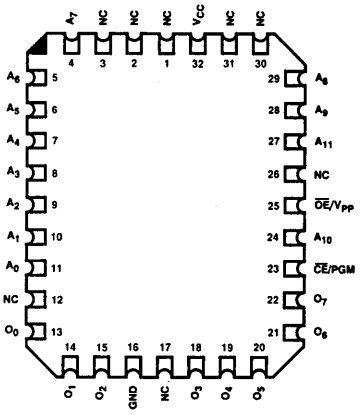


MOS-491

Pin 1 is marked for orientation.

A_0-A_{11}: Addresses
O_0-O_7: Outputs
$\overline{CE}$/PGM: Chip Enable/Program
$\overline{OE}$/VPP: Output Enable

Chip-Pak™ L-32-2



MOS-671

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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−65 to +135°C
Voltage on All Inputs/Outputs (Except $\overline{OE}$/VPP) with Respect to GND	+6 to −0.3V
$\overline{OE}$/VPP with Respect to GND	+26.5 to −0.3V

DC AND AC READ OPERATIONS CONDITIONS

	Temperature Range	V_{CC}
AM2732-1DC	0 to +70°C	5V ±10%
AM2732DC	0 to +70°C	5V ± 5%
AM2732DI	−40 to 85°C	5V ± 5%
AM2732DL	−55 to +100°C	5V ± 10%
AM2732DM	−55 to +125°C	5V ± 10%

DC CHARACTERISTICS

Parameters	Description	Test Conditions	Min Values	Maximum Values			Units
			All Types	2732 DL/DM	2732DI	2732DC/ -1DC	
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ (Max) and $V_{IN} = 0$		10	10	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ (Max) and $V_{IN} = 0$		10	10	10	μA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$		45	40	30	mA
I_{CC2} (Note 2)	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$		175	165	150	mA
V_{IL}	Input Low Voltage		−0.1	0.8	0.8	0.8	Volts
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V_{CC}+1	V_{CC}+1	Volts
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.45	0.45	0.45	Volts
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4				Volts

AC CHARACTERISTICS

Parameters	Description	Test Conditions		Min Values	Maximum Values			Units
				All Types	2732-1 DC	2732DC	2732DI/ DL/DM	
t_{ACC}	Address to Output Delay	Output Load: 1 TTL gate and C_L = 100pF Input Rise and Fall Times: ≤20ns Input Pulse Levels: 0.8 to 2.2V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V	$\overline{CE} = \overline{OE} = V_{IL}$		350	450	450	ns
t_{CE}	$\overline{CE}$ to Output Delay		$\overline{OE} = V_{IL}$		350	450	450	ns
t_{OE}	Output Enable to Output Delay		$\overline{CE} = V_{IL}$		120	120	150	ns
t_{DF}	Output Enable High to Output Float		$\overline{CE} = V_{IL}$	0	100	100	130	ns
t_{OH}	Address to Output Hold		$\overline{CE} = \overline{OE} = V_{IL}$	0				ns

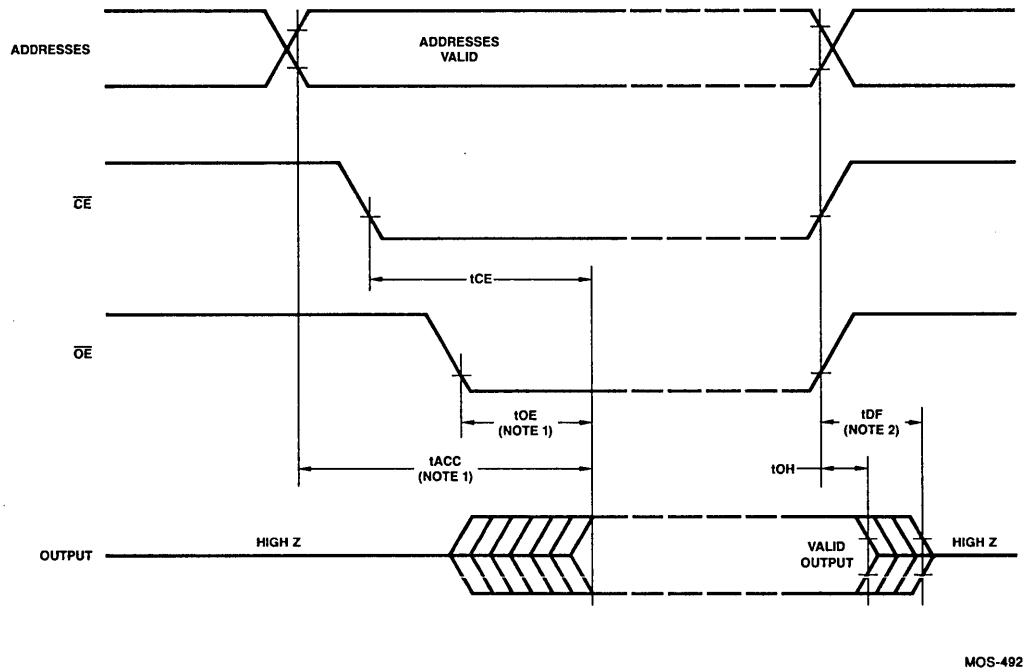
CAPACITANCE (Note 1)

T_A = +25°C, f = 1MHz

Parameters	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{IN2}	$\overline{OE}$/VPP Input Capacitance	V_{IN} = 0V		20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note 1. This parameter is only sampled and is not 100% tested.

AC WAVEFORMS (Note 1)



Notes: 1. OE may be delayed up to 330ns after the falling edge of $\overline{CE}$ without impact on t_{ACC}
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAM OPERATION

DC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (Note 1) = 5V ±5%, V_{PP} (Notes 1, 2) = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	μA
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1mA		0.45	Volts
V_{OH}	Output High Voltage During Verify	I_{OH} = −400μA	2.4		Volts
I_{CC}	V_{CC} Supply Current			150	mA
V_{IL}	Input Low Level (All Inputs)		−0.1	0.8	Volts
V_{IH}	Input High Level (All Inputs Except $\overline{OE}$/VPP)		2.0	V_{CC}+1	Volts
I_{PP}	VPP Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE}$ = VPP		30	mA

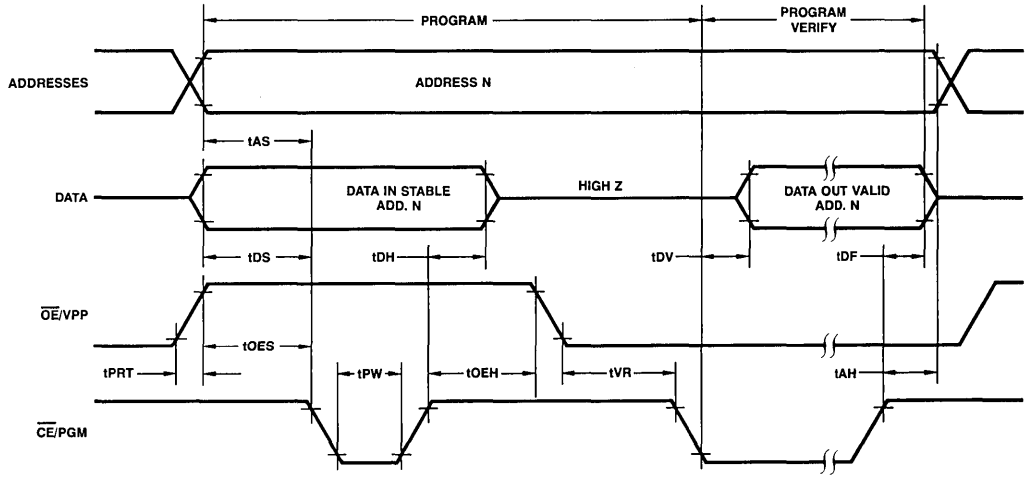
AC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (Note 1) = 5V ±5%, V_{PP} (Notes 1, 2) = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
t_{AS}	Address Set-up Time	Input tR and tF (10% to 90%) = 20ns Input Signal Levels = 0.8 to 2.2V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V	2		μs
t_{OES}	Output Enable Set-up Time		2		μs
t_{DS}	Data Set-up Time		2		μs
t_{AH}	Address Hold Time		2		μs
t_{OEH}	Output Enable Hold Time		2		μs
t_{DH}	Data Hold Time		2		μs
t_{DF}	Chip Enable to Output Float Delay		0	120	ns
t_{DV}	Data Valid From $\overline{CE}$ ($\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$)		–	1	ns
t_{PW}	Program Pulse Width		45	55	ms
t_{PRT}	Program Pulse Rise Time		50	–	ns
t_{VR}	VPP Recovery Time		2	–	ns

Note 1. When programming the Am2732, a 0.1μF capacitor is required across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device.

PROGRAMMING WAVEFORMS



MOS-493

ERASING THE Am2732

In order to clear all locations of their programmed contents, it is necessary to expose the Am2732 to an ultraviolet light source. A dosage of 15 Wseconds/cm^2 is required to completely erase an Am2732. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000μW/cm^2 for 15 to 20 minutes. The Am2732 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2732, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am2732, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING THE Am2732

Upon delivery, or after each erasure the Am2732 has all 32768 bits in the "1", or high state. "0"s are loaded into the Am2732 through the procedure of programming.

The programming mode is entered when +25V is applied to the $\overline{OE}$/VPP pin. A 0.1μF capacitor must be placed across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL low level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC low level to the $\overline{CE}$/PGM input is prohibited when programming.

READ MODE

The Am2732 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$/VPP) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs 120ns (tOE) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC − tOE.

STANDBY MODE

The Am2732 has a standby mode which reduces the active power dissipation by 80%, from 787mW to 157mW (values for 0 to +70°C). The Am2732 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAM INHIBIT

Programming of multiple Am2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2732s may be common. A TTL level program pulse applied to an Am2732's $\overline{CE}$/PGM input with VPP at 25V will program that Am2732. A high level $\overline{CE}$/PGM input inhibits the other Am2732 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$/VPP and $\overline{CE}$ at VIL. Data should be verified tDV after the falling edge of $\overline{CE}$.

ORDERING INFORMATION

Ambient Temperature Specification	Order Number	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)
0°C ≤ T_A ≤ 70°C	AM2732-1DC	350	350	120
	AM2732-1LC			
	AM2732DC	450	450	120
	AM2732LC			
−40°C ≤ T_A ≤ +85°C	AM2732DI	450	450	150
	AM2732LI			
−55°C ≤ T_A ≤ +100°C	AM2732DL	450	450	150
	AM2732LL			
−55°C ≤ T_A ≤ +125°C	AM2732DM	450	450	150
	AM2732LM			

Am2732A

4096 x 8-Bit UV Erasable PROM

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access times – 200ns, 250ns, 300ns
- Low power consumption
  - 785mW active
  - 184mW stand-by
- Single 5V power supply
- ±10% V_{CC} supply tolerance available
- TTL compatible inputs
- Three-state outputs
- 24-pin JEDEC approved 2732 pin-out
- Pin compatible with Am9233-32K-bit ROM
- Separate chip enable and output enable
- 100% MIL-STD-883 reliability testing

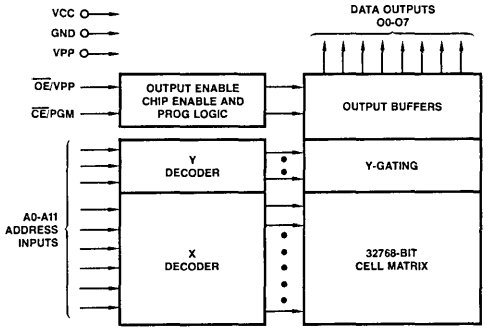
GENERAL DESCRIPTION

The Am2732A is a 32768-bit UV-light erasable and electrically pogrammable read-only memory. It is organized as 4096 words by 8-bits per word. The standard Am2732A offers an access time of 200ns, allowing operation with high-speed (≥8MHz) microprocessors without any WAIT state.

To eliminate bus contention in a multiple-bus microprocessor system, Am2732A offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random.

BLOCK DIAGRAM



MOS-490

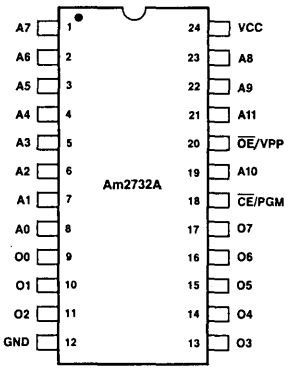
MODE SELECTION

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$/VPP (20)	VCC (24)	Outputs (9-11, 13-17)
Read	VIL	VIL	+5	DOUT
Standby	VIH	X	+5	High Z
Program	VIL	VPP	+5	DIN
Program Verify	VIL	VIL	+5	DOUT
Program Inhibit	VIH	VPP	+5	High Z

X can be either V_{IL} or V_{IH}

Figure 1.

CONNECTION DIAGRAM
Top View



MOS-669

Pin 1 is marked for orientation.

A0-A11: Addresses
O0-O7: Outputs
$\overline{CE}$/PGM: Chip Enable/Program
$\overline{OE}$/VPP: Output Enable

Figure 2.

Am2764

8192 x 8-Bit UV Erasable PROM

DISTINCTIVE CHARACTERISTICS

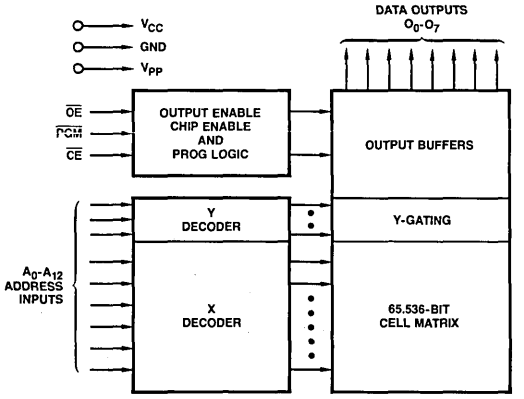
- 0.3% AQL guaranteed
- Fast access time – 200ns, 250ns, and 300ns
- Low power dissipation
  - –525mW active
  - –105mW standby
- ±10% power supply tolerance available
- 100% MIL-STD-883 reliability assurance testing
- Single +5V power supply
- 28-pin JEDEC approved 2764 pinout
- Pin compatible with Am9265 – 64K ROM
- Fully static operation – no clocks
- TTL compatible inputs/outputs

GENERAL DESCRIPTION

The Am2764 is a 65536-bit ultraviolet erasable and programmable read-only memory. It is organized as 8192 words by 8 bits per word, operates from a single +5V supply, has a static standby mode, and features fast single address location programming.

Because the Am2764 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 400 seconds.

BLOCK DIAGRAM



MODE SELECTION

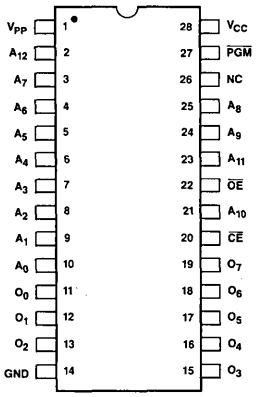
Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}

NVM-001

CONNECTION DIAGRAMS – Top Views

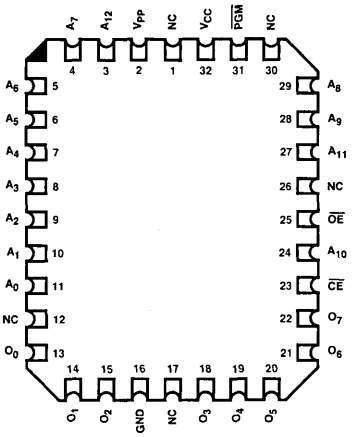
DIP



NVM-002

Pin 1 is marked for orientation.

Chip-Pak™ L-32-2



NVM-007

A_0-A_{12}:	Addresses	$\overline{OE}$:	Output Enable
O_0-O_7:	Outputs	$\overline{PGM}$:	Program
$\overline{CE}$:	Chip Enable	NC: :	No Connect

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MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65 to +125°C
Ambient Temperature Under Bias	−10 to +80°C
Voltage on All Inputs/Outputs with Respect to GND	+7 to −0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+22V to −0.6V

READ OPERATION[5]

DC CHARACTERISTICS $0°C \leq T_A \leq +70°C$, $V_{CC} = V_{PP} = 5V \pm 5\%$ (Notes 1, 2) ($V_{CC} = V_{PP} = 5V \pm 10\%$ for 2764-20, 2764-25, 2764-30 and 2764-45)

Parameters	Description	Test Conditions	Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0V$ to 5.5V		10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0V$ to 5.5V		10	μA
I_{PP1}	V_{PP} Current Read (Note 2)	$V_{PP} = 5.5V$		1	mA
I_{CC1}	V_{CC} Standby Current (Note 2)	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$		20	mA
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{OE} = \overline{CE} = V_{IL}$		100	mA
V_{IL}	Input Low Voltage		−0.1	+0.8	Volts
V_{IH}	Input High Voltage		2.0	V_{CC}+1	Volts
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$		0.45	Volts
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4		Volts

AC CHARACTERISTICS $0°C \leq T_A \leq 70°C$, $V_{CC} = V_{PP} = 5V \pm 5\%$ (Notes 1, 2)
($V_{CC} = V_{PP} = 5V \pm 10\%$ for 2764-20, 2764-25, 2764-30 and 2764-45)

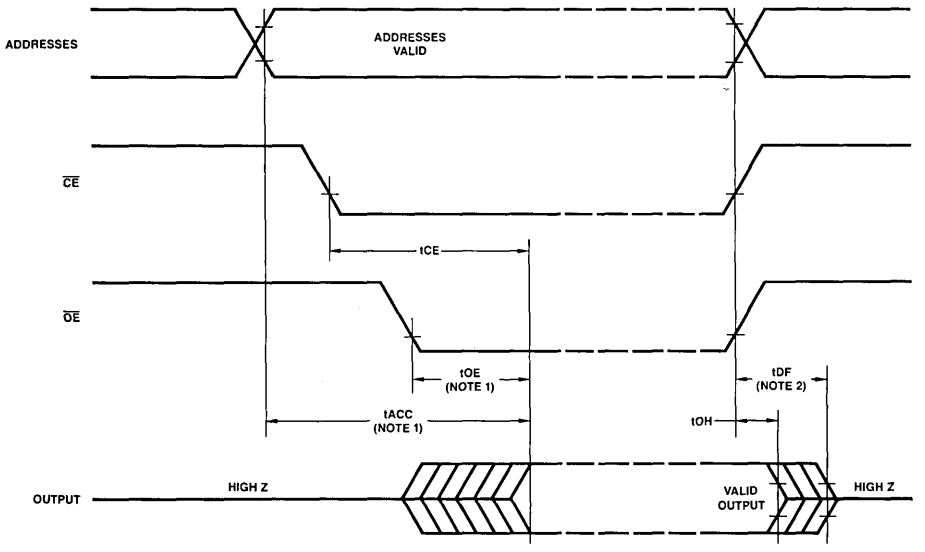
Parameters	Description	Test Conditions		Min Values	Maximum Values				Units
				All Types	2764-20 2764-2	2764-25 2764	2764-30 2764-3	2764-45 2764-4	
t_{ACC}	Address to Output Delay	Output Load: 1 TTL gate and C_L = 100pF Input Rise and Fall Times: ≤20ns Input Pulse Levels: .45 to 2.4V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V	$\overline{CE} = \overline{OE} = V_{IL}$		200	250	300	450	ns
t_{CE}	$\overline{CE}$ to Output Delay		$\overline{OE} = V_{IL}$		200	250	300	450	ns
t_{OE}	Output Enable to Output Delay		$\overline{CE} = V_{IL}$		75	100	120	150	ns
t_{DF}	Output Enable High to Output Float (Note 4)		$\overline{CE} = V_{IL}$	0	60	85	105	130	ns
t_{OH} (Note 4)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First		$\overline{CE} = \overline{OE} = V_{IL}$	0					ns

CAPACITANCE (Notes 3, 4)
$T_A = +25°C$, f = 1MHz

Parameters	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for nominal supply voltages.
4. This parameter is only sampled and not 100% tested.
5. Caution: The 2764 must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.

AC WAVEFORMS



Notes: 1. OE may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

NVM-003

PROGRAM OPERATION

DC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (See Note 1) = 5V ±5%, V_{PP} (See Notes 1, 2) = 21V ±0.5V

Parameters	Description	Test Conditions	Min	Max	Units
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	μA
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1mA		0.45	Volts
V_{OH}	Output High Voltage During Verify	I_{OH} = −400μA	2.4		Volts
I_{CC2}	V_{CC} Supply Current (Active)			100	mA
V_{IL}	Input Low Level (All Inputs)		−0.1	0.8	Volts
V_{IH}	Input High Level		2.0	V_{CC}+1	Volts
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL} = \overline{PGM}$		30	mA

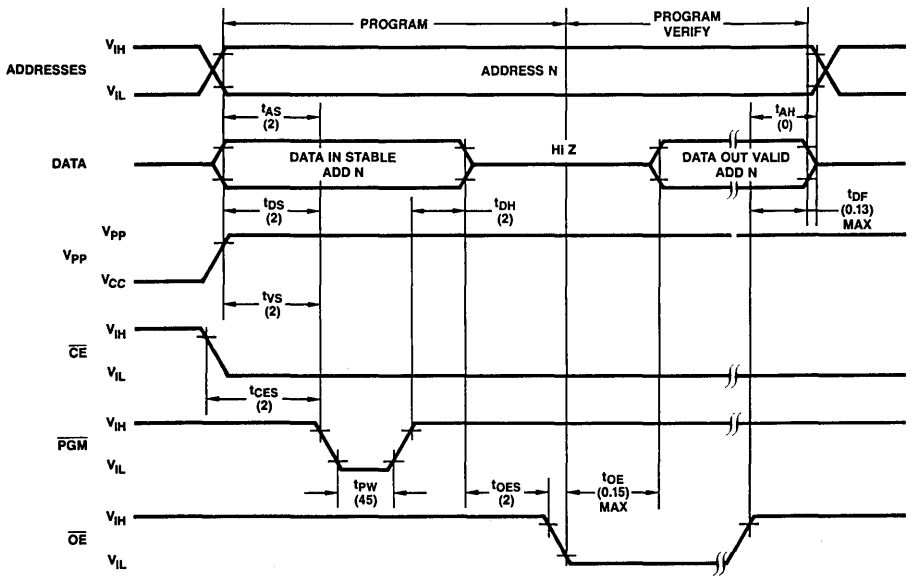
AC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (Note 1) = 5V ±5%, V_{PP} (Notes 1, 2) = 21V ±0.5V

Parameters	Description	Test Conditions	Min	Max	Units
t_{AS}	Address Set-up Time	Input tR and tF (10 to 90%) = 20ns Input Pulse Levels = 0.45 to 2.4V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V	2		μs
t_{OES}	Output Enable Set-up Time		2		μs
t_{DS}	Data Set-up Time		2		μs
t_{AH}	Address Hold Time		0		μs
t_{OEH}	Output Enable Hold Time		2		μs
t_{DH}	Data Hold Time		2		μs
t_{DF}	Chip Enable to Output Float Delay		0	130	ns
t_{VS}	V_{PP} Setup Time		2		μs
t_{PW}	$\overline{PGM}$ Pulse Width		45	55	ms
t_{CES}	$\overline{CE}$ Setup Time		2		μs
t_{OE}	Data Valid From $\overline{OE}$			150	ns

Notes: 1. *Caution: If V_{CC} is not applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}, the 2764 could be damaged.*
2. When programming the Am2764, a 0.1μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.

PROGRAMMING WAVEFORMS (Notes 1, 2 and 3)



Notes: 1. All times shown in ( ) are minimum and in μsec unless otherwise specified.
2. The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.
3. t_{OE} and t_{DF} are characteristics of the device but must be accomodated by the programmer.

NVM-004

ORDERING INFORMATION

Ambient Temperature Specification	Order Number	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}
$0C \leq T_A \leq 70°C$	AM2764-2DC	200	200	75	5V ± 5%
	AM2764-2LC				
	AM2764-20DC	200	200	75	5V ± 10%
	AM2764-20LC				
	AM2764DC	250	250	100	5V ± 5%
	AM2764LC				
	AM2764-25DC	250	250	100	5V ± 10%
	AM2764-25LC				
	AM2764-3DC	300	300	120	5V ± 5%
	AM2764-3LC				
	AM2764-30DC	300	300	120	5V ± 10%
	AM2764-30LC				
	AM2764-4DC	450	450	150	5V ± 5%
	AM2764-4LC				
	AM2764-45DC	450	450	150	5V ± 10%
	AM2764-45LC				

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ERASING THE Am2764

In order to clear all locations of their programmed contents, it is necessary to expose the Am2764 to an ultraviolet light source. A dosage of 15 Wseconds/cm^2 is required to completely erase an Am2764. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000μW/cm^2 for 15 to 20 minutes. The Am2764 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2764, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am2764, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

PROGRAMMING THE Am2764

Upon delivery, or after each erasure the Am2764 has all 65536 bits in the "1", or high state. "0"s are loaded into the Am2764 through the procedure of programming.

The programming mode is entered when +21V is applied to the VPP pin. A 0.1μF capacitor must be placed across VPP and ground to suppress spurious voltage transients which may damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL low level pulse is applied to the $\overline{PGM}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC low level to the $\overline{PGM}$ input is prohibited when programming.

READ MODE

The Am2764 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The Am2764 has a standby mode which reduces the active power dissipation by 80%, from 525mW to 105mW (values for 0 to +70°C). The Am2764 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAM INHIBIT

Programming of multiple Am2764s in parallel with different data is also easily accomplished. Except for $\overline{PGM}$, all like inputs (including $\overline{OE}$) of the parallel Am2764s may be common. A TTL level program pulse applied to an Am2764's $\overline{PGM}$ input with VPP at 21V will program that Am2764. A high level $\overline{PGM}$ input inhibits the other Am2764s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$ and $\overline{CE}$ at VIL. Data should be verified tOE after the falling edge of $\overline{OE}$.

SYSTEM APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage droop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

Am27128

16 384 x 8-Bit UV Erasable PROM

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast access time – 200ns, 250ns, 300ns, 450ns
- Low power consumption
  - 525mW active
  - 210mW stand-by
- Single 5V power supply
- ±10% V_{CC} supply tolerance available
- Fully static operation – no clocks
- Separate chip enable and output enable controls
- TTL compatible inputs/outputs
- 28-pin JEDEC approved 27128 pin-out
- Pin compatible to Am2764 EPROM and Am92128-128K ROM
- 100% MIL-STD-883 reliability testing

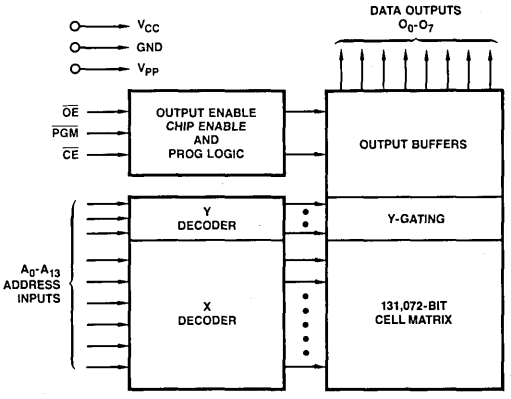
GENERAL DESCRIPTION

The Am27128 is a 131,072-bit UV-light erasable and electrically programmable read-only memory. It is organized as 16384 words by 8-bits per word. The standard Am27128 offers access time of 200ns, allowing operation with high-speed (≥8MHz) microprocessors without any WAIT state.

To eliminate bus contention in a multiple-bus microprocessor system, Am27128 offers separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random.

BLOCK DIAGRAM



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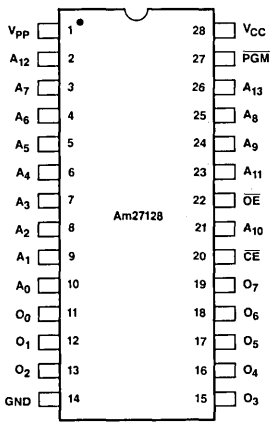
MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}

Figure 1.

CONNECTION DIAGRAM
Top View



NVM-006

Pin 1 is marked for orientation.

A_0-A_{13}:	Addresses	$\overline{OE}$:	Output Enable
O_0-O_7:	Outputs	$\overline{PGM}$:	Program
$\overline{CE}$:	Chip Enable		

Figure 2.

General Information Index

Advanced Micro Devices Commitment to Excellence

Product Assurance Programs for Military and Commercial Integrated Circuits

7

A COMMITMENT TO EXCELLENCE

Advanced Micro Devices was conceived on the premise that there was a place in the semiconductor community for a manufacturer dedicated to excellence.

In product assurance procedures, Advanced Micro Devices is unique. Only Advanced Micro Devices processes all integrated circuits, commercial as well as military, to the demanding requirements of MIL-STD-883. The Rome Air Development Center (RADC), which is the Air Force's principal authority on component reliability, has issued MIL-HDBK-217B which indicates that parts processed to Military Standard 883, Level C (Advanced Micro Devices' standard processing) yield a product nearly ten times better in failure rates than the industry commercial average.

Our Sunnyvale facility has been certified by the Defense Electronics Supply Center (DESC) to produce parts to JAN Class B and C under Military Specification MIL-M-38510. The National Aeronautics and Space Administration (NASA) has certified this production line for the manufacture of Class A products for programs requiring the highest levels of reliability. Advanced Micro Devices is the only integrated circuit company formed within the last ten years to achieve such line certification.

This brochure outlines Advanced Micro Devices' standard programs for Class B, C and A devices for military and commercial operating range applications. These will cover the majority of system requirements today. Alternative screening flows for specific user needs can be performed on request. Check with your local sales office for further information.

ADVANCED MICRO DEVICES' STANDARD PRODUCTS ARE MANUFACTURED TO MIL-STD-883 REQUIREMENTS

Advanced Micro Devices' product assurance programs are based on two key documents.

MIL-M-38510 – General Specification for Microcircuits

MIL-STD-883 – Test Methods and Procedures for Microelectronics

The screening charts in this brochure show that every integrated circuit shipped by Advanced Micro Devices receives the critical screening procedures defined in MIL-STD-883, Method 5004 for Class C product. This includes molded plastic devices.

In addition, documentation, design, processing and assembly workmanship guidelines are patterned after MIL-M-38510 specifications.

Commercial and industrial users receive the quality and reliability benefits of this aerospace-type screening and documentation at no additional cost.

STANDARD PRODUCT TESTING CATEGORIES

Advanced Micro Devices offers integrated circuits to three standard testing categories.

1. Commercial operating range product (typically 0 to 70°C)
2. Military operating range product (typically −55 to +125°C)
3. JAN qualified product

Categories 1 and 2 are available on most Advanced Micro Devices circuits. Category 3 is offered on a more limited line. Additional testing and screening services are available to special order. Check with your local sales office for details.

STANDARD PRODUCT ASSURANCE CATEGORIES

Devices produced to the above testing categories are available to the three standard classes of product assurance defined by MIL-STD-883. As a minimum, every device shipped by Advanced Micro Devices meets the screening requirements of Class C.

Class C – For commercial and ground-based military systems where replacement can be accomplished without difficulty.

According to MIL-HDBK-217B, this assures relative failure rates 9.4 times better than that of regular industry commercial product.

Class B – For flight applications and commercial systems where maintenance is difficult or expensive and where reliablity is vital.

Devices are upgraded from Class C to Class B by burn-in screening and additional testing.

According to MIL-HDBK-217B, Class B failure rate is improved 30 times over regular industry commercial product. Advanced Micro Devices Class B processing conforms to MIL-STD-883 requirements. MIL-HDBK-217B indicates that this may provide failure rates as much as two times better than some other manufacturers' "equivalent" or "pseudo" Class B programs.

Class S – For space applications where replacement is extremely difficult or impossible and reliability is imperative.

Class S screening includes x-ray and other special inspections tailored to the specific requirements of the user.

The 100% screening and quality conformance testing performed within these Advanced Micro Devices' programs is shown in TABLES I, II and III. A full description of the process flow is provided in Product Assurance Document 15-010, available on request.

CLASS C SCREENING FLOW FOR COMMERCIAL SYSTEMS AND GROUND BASED MILITARY SYSTEMS

TABLE I
CLASS C
INTEGRATED CIRCUITS

Screening Procedure per MIL-STD-883 Method 5004, Class C		COMMERCIAL OPERATING RANGE	MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES	HERMETIC PACKAGE ONLY	
Screen	Test Method	Flow C1 Commercial Product	Flow C3 Military Product	Flow C4 Jan Qualified Product
VISUAL AND MECHANICAL				
Internal visual	2010, Condition B	100%	100%	100%
High temperature storage	1008, Condition C, 24 hours	100%	100%	100%
Temperature cycle	1010, Condition C	100%	100%	100%
Constant acceleration	2001	100% (1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (1)	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(2)	–	–
Functional	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(2)	–	–
Switching (ac) or Dynamic	At 25°C, nominal power supply	(2)	–	–
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample
Sample Tests	Group B	–	–	Sample
	Group C	–	–	Sample
	Group D	–	–	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%

TABLE II
GROUP A QUALITY CONFORMANCE LEVELS

Advanced Micro Devices employs the military-recommended LTPD sampling system to assure quality. MIL-STD-883, Method 5005, TABLE I, Group A, subgroups 1 through 9 as appropriate to the device family are performed on every lot. Quality levels defined for Class B product are applied by Advanced Micro Devices to both Class B and Class C orders.

	LTPD	INITIAL SAMPLE SIZE
Subgroup 1 – Static tests at 25°C	5	45
Subgroup 2 – Static tests at maximum rated operating temperature	7	32
Subgroup 3 – Static tests at minimum rated operating temperature	7	32
Subgroup 4 – Dynamic tests at 25°C – LINEAR devices	5	45
Subgroup 5 – Dynamic tests at maximum rated operating temperature – LINEAR devices	7	32
Subgroup 6 – Dynamic tests at minimum rated operating temperature – LINEAR devices	7	32
Subgroup 7 – Functional tests at 25°C	5	45
Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 – Switching tests at 25°C – DIGITAL devices	7	32
Subgroup 10 – Switching tests at maximum rated operating temperatures – DIGITAL devices	*	
Subgroup 11 – Switching tests at minimum rated operating temperatures – DIGITAL devices	*	

*These subgroups, where applicable, are usually performed during initial characterization only for all except JAN Qualified product.

CLASS B SCREENING FLOW FOR HIGH RELIABILITY COMMERCIAL AND MILITARY SYSTEMS

TABLE III
CLASS B
INTEGRATED CIRCUITS
(Class C plus burn in screening and additional testing.)

Screening Procedure per MIL-STD-883 Method 5004, Class B		COMMERCIAL OPERATING RANGE	MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES	HERMETIC PACKAGE ONLY	
Screen	Test Method	Flow B1 Commercial Product	Flow B3 Military Product	Flow B4 Jan Qualified Product
VISUAL AND MECHANICAL				
Internal visual	2010, Condition B	100%	100%	100%
High temperature storage	1008, Condition C, 24 hours	100%	100%	100%
Temperature cycle	1010, Condition C	100%	100%	100%
Constant acceleration	2001	100% (1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (1)	100%	100%
BURN IN				
Interim (pre burn in) electricals	Per applicable device specification	100%	100%	100%
Burn in	1015, 160 hours at 125°C or equivalent.*	100% (3)	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(2) (3)	100%	100%
Functional	a) At 25°C, and power supply extremes	100%	100%	100%
	b) At temperature and power supply extremes	(2) (3)	100%	100%
Switching (ac) or Dynamic	At 25°C, nominal power supply	(2)	100%	100%
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample
Sample Tests	Group B	–	(4)	Sample
	Group C	–	(4)	Sample
	Group D	–	(4)	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%

Notes: 1. Not applicable to molded packages.
2. All MOS RAMs and many other MOS devices receive a.c. testing and 100% d.c. screening at high temperature and power supply extremes as standard. Other products sampled at Group A (Table II).
3. Am2900 LSI products receive a 96 hour burn-in, plus 100% d.c. screening at high temperature and power supply extremes.
4. Unless device data sheet specifies different limits.
5. Without optical aid for commercial devices.

*(Unless device data sheet specifies otherwise).

CLASS S
FOR AEROSPACE SYSTEMS. (FORMERLY CLASS A)

Advanced Micro Devices offers Class S programs based on screening defined in MIL-STD-883, Method 5004. Contact your local Advanced Micro Devices' sales office for more information.

Table IV – Class S Screening Flow

Screening Procedure Class S		MILITARY OPERATING RANGE HERMETIC PACKAGE ONLY	MILITARY OPERATING RANGE HERMETIC PACKAGE ONLY
Screen	Test Method	Flow S1 Basic S Flow	Flow S2 Extended Class S Processing
SEM			Contact Advanced Micro Devices Sales for Details
Scanning Electron Microscope	2018	Wafer Lot Sample	
ASSEMBLY			
Class S Process Monitors	–	Periodic sampling	
VISUAL AND MECHANICAL			
Internal Visual	2010, Condition A	100%	
High Temperature Storage	1008, Condition C, 24 hours	100%	
Temperature Cycle	1010, Condition C	100%	
Constant Acceleration	2001, Condition E	100%	
PIND			
Particle Impact Noise Detection	2020, Condition A or B	100% (Note 1)	
Serialization		100%	
X-RAY			
Radiographic	2012, Two views	100%	
BURN-IN			
Interim (Pre Burn-in) Electricals	Per applicable device specification	100% (Note 2)	
Burn-in	1015, 240 hours at 125°C or equivalent	100% (Note 3)	
Interim (Post Burn-in) Electricals	Per applicable device specification	100% (Note 2)	
FINAL ELECTRICAL TESTS		AMD Data Sheet	
Static (dc)	a) At 25°C, and power supply extremes	100%	
	b) At temperature and power supply extremes	100%	
Functional	a) At 25°C and power supply extremes	100%	
	b) At temperature and power supply extremes	100%	
Switching (ac) or Dynamic	At 25°C nominal power supply	100%	
SEAL			
Hermeticity, Fine and Gross	1014	100%	
QUALITY CONFORMANCE			
	5005, Group A (See Table II)	Sample	
Sample Tests	Group B	Sample (Note 4)	
	Group D	Sample (Note 4)	
EXTERNAL VISUAL	2009	100%	

Notes: 1. 100% screen, one pass.
2. Read and record requirements to be specified as applicable to particular device type.
3. Consult device data sheet.
4. Available to special order.

STANDARD PRODUCT
SCREENING SUMMARY AND ORDERING INFORMATION

1. COMMERCIAL PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic and molded packages.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class C and Class B options.

Class C

- Order standard AMD part number.
- Marked same as order number.

Examples: AM25LS374DC, SN74LS374J

Class B

- Burn in performed in AMD circuit condition.
- Order standard AMD part number, add suffix B (or /883B for 1, 2 and 300 Series Linear devices).
- Marked same as order number.

Examples: AM25LS374DC-B, SN74LS374J-B

2. MILITARY PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic package only.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class B and Class C options.

Class C

- Order standard AMD part number.
- Marked same as order number.

Examples: AM25LS374DM, SN54LS374J

Class B

- Burn in performed in AMD circuit condition.
- AC at 25°C, d.c. and functional testing at 25°C as well as temperature and power supply extremes performed on 100% of every lot.
- Quality conformance testing, Method 5005, Groups B, C and D available to special order.
- Order standard AMD part number, add suffix B.
- Marked same as order number.

Examples: AM25LS374DM-B, SN54LS374J-B

3. JAN QUALIFIED PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested to JAN detail specification (slash sheet).
- Manufactured in Defense Logistics Agency certified facility.
- Quality conformance testing, Method 5005, Groups A, B, C and D performed as standard and must be completed prior to shipment.
- It is a product for which AMD has gained QPL listing.*

Class B (Flow B4)

- Burn in performed in circuit condition approved for JAN devices.
- Order per military document.
- Marked per military document.

Example: JM38510/30106BEB

*In certain cases where JAN Qualified product is specified but is not available, Advanced Micro Devices can provide devices to the electrical limits and burn-in criteria of the slash sheet. This class of product has been called JAN Equivalent and marked M38510/ by some manufacturers. This identification is no longer permitted by DESC. Check with your local sales office for availability of specific device types.

Product Assurance

MIL-M-38510 • MIL-STD-883

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Two military documents provide the foundation for this program. They are:

MIL-M-38510 – General Specification for Microcircuits
MIL-STD-883 – Test Methods and Procedures for Microelectronics

MIL-M-38510 describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. All circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510.

MIL-STD-883 defines detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

Test Method 2010 defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Standard inspection at Advanced Micro Devices includes all the requirements of the latest revision of Method 2010, condition B.

Test Method 5004 defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

Class C – Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

Class B – Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 160-hour burn-in at 125°C followed by more extensive electrical measurements. All other screening requirements are the same.

Class S – Used where replacement is extremely difficult and reliability is imperative. Class S screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and tighter sampling inspection.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to MIL-STD-883, Class C. Molded integrated circuits receive Class C screening except that centrifuge and hermeticity steps are omitted.

Optional extended processing to MIL-STD-883, Class B is available for all AMD integrated circuits. Parts procured to this screening are marked with a "−B" following the standard part number, except that linear 100, 200 or 300 series are suffixed "/883B".

Test Method 5005 defines qualification and quality conformance procedures. Subgroups, tests and quality levels are given for Group A (electrical), Group B (mechanical quality related to the user's assembly environment), Group C (die related tests) and Group D (package related tests). Group A tests are always performed; Group B, C and D may be specified by the user.

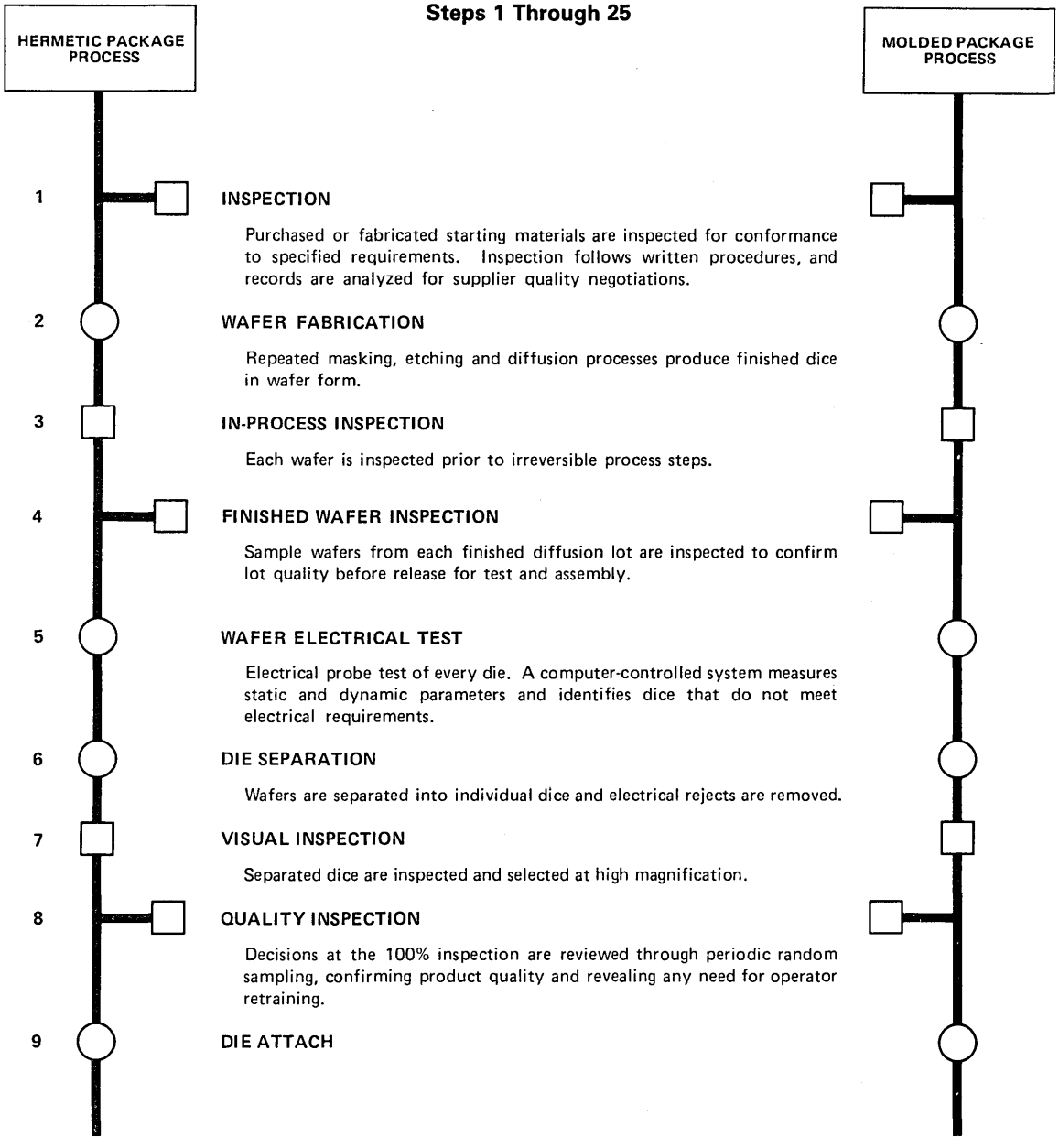
MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004, Class C; quality conformance inspection where required is performed to Class B quality levels on either Class B or Class C product.

All full-temperature-range (−55°C to +125°C) circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.

STANDARD PROCESSING CLASS C Steps 1 Through 25



10 **QUALITY INSPECTION**

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

11 **WIRE BOND**

Hermetic: Aluminum wires, ultrasonic bonding.
Molded: Gold wires, thermocompression bonding.

12 **QUALITY INSPECTION**

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

13 **INTERNAL VISUAL INSPECTION**

Assembled but unsealed units are individually inspected at low and high power.

QUALITY STANDARDS:

All devices – MIL-STD-883, Method 2010, Condition B (latest revision). Full temperature devices – MIL-M-38510, Para. 3.7 for workmanship (re-bonding limits).

14 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

15a **FINAL SEAL**

(Hermetic devices)

15b **ENCAPSULATE**

(Molded Devices)

16 **HIGH TEMPERATURE STORAGE**

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

17 **TEMPERATURE CYCLE**

MIL-STD-883, Method 1010, Cond. C: −65°C, +150°C, 10 cycles

18 **CENTRIFUGE**

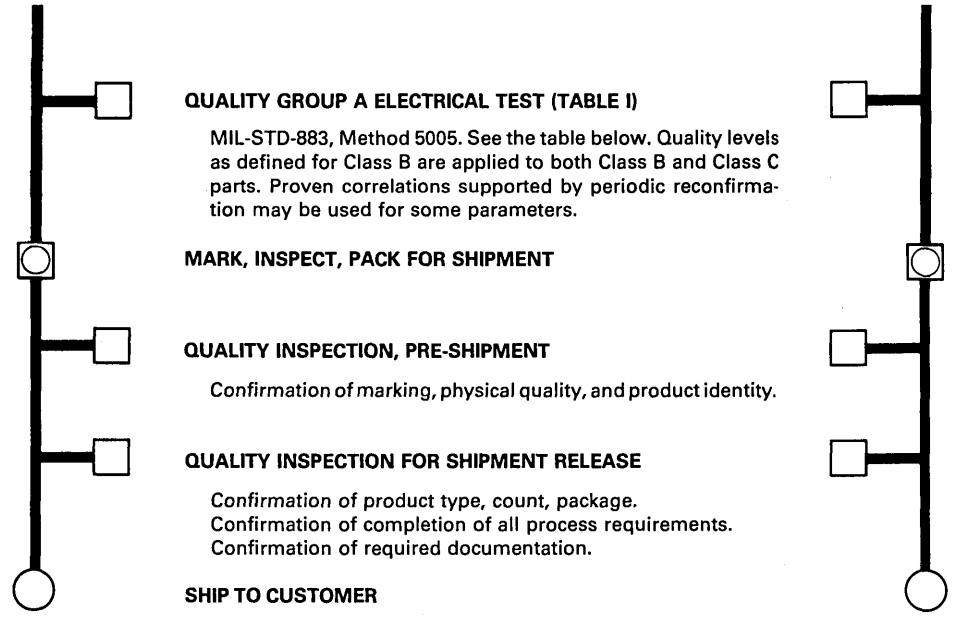
MIL-STD-883, Method 2001, Cond. E: 30,000 G

19 **SEAL (HERMETICITY) TEST**

MIL-STD-883, Method 1014, Cond. A or B: Fine Leak
MIL-STD-883, Method 1014, Cond. C: Gross Leak

20 **ELECTRICAL TEST**

MIL-STD-883, Method 5004, Para. 3.1.12: Static, dynamic, functional tests at 25°C or in certain products at the most critical extreme temperature to assure accuracy of device selection.



21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

MIL-STD-883, Method 5005. See the table below. Quality levels as defined for Class B are applied to both Class B and Class C parts. Proven correlations supported by periodic reconfirmation may be used for some parameters.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER**

This AMD standard product meets screening requirements of MIL-STD-883, Class C.

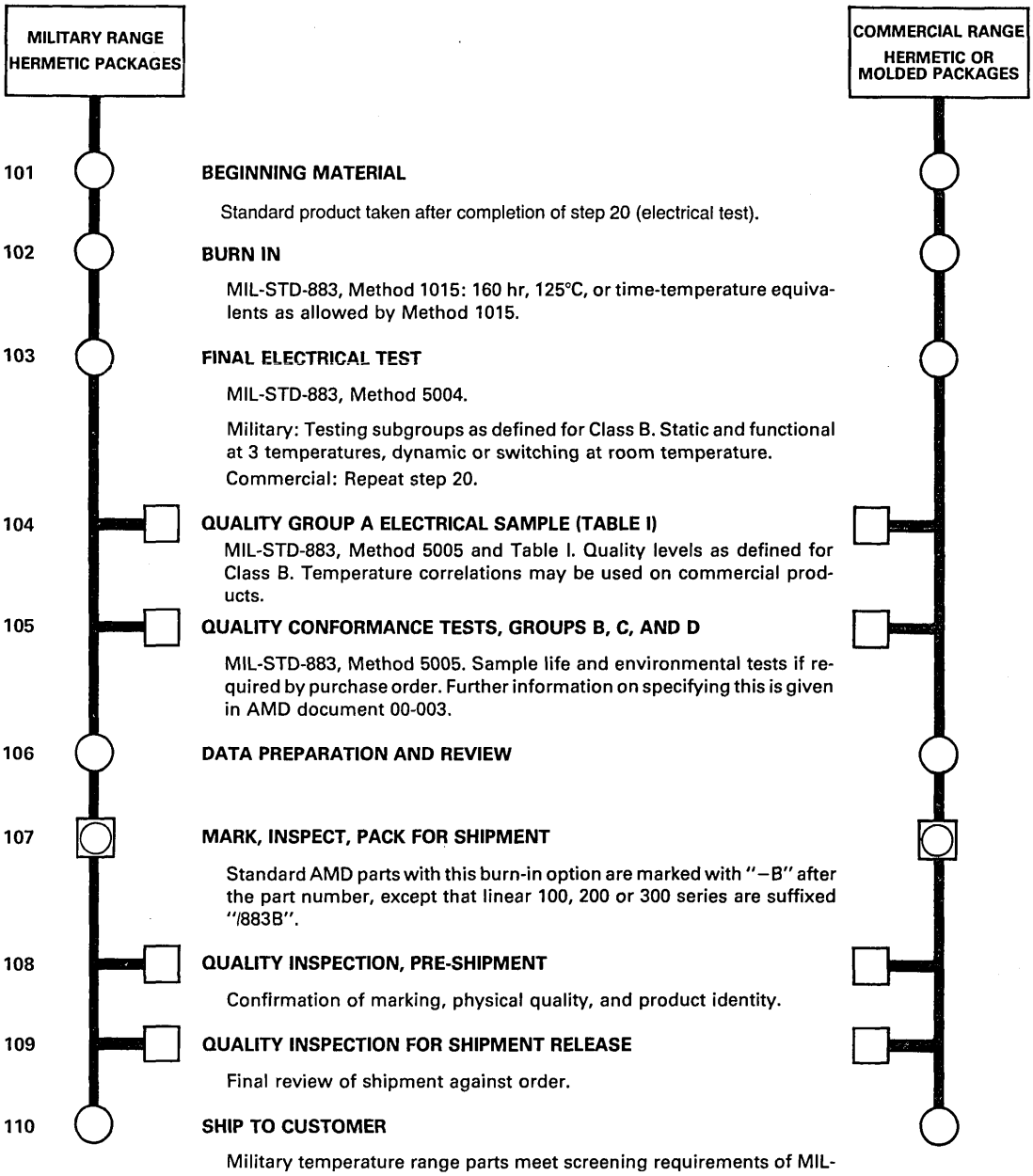
GROUP A ELECTRICAL TESTS
From MIL-STD-883, Method 5005, Table I

Subgroups	LTPD (Note 1)	Initial Sample Size
Subgroup 1 – Static tests at 25°C	5	45
Subgroup 2 – Static tests at maximum rated operating temperature	7	32
Subgroup 3 – Static tests at minimum rated operating temperature	7	32
Subgroup 4 – Dynamic tests at 25°C – Linear devices	5	45
Subgroup 5 – Dynamic tests at maximum rated operating temperature – Linear devices	7	32
Subgroup 6 – Dynamic tests at minimum rated operating temperature – Linear devices	7	32
Subgroup 7 – Functional tests at 25°C	5	45
Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 – Switching tests at 25°C – Digital devices	7	32
Subgroup 10 – Switching tests at maximum rated operating temperature – Digital devices (Note 2)	10	10
Subgroup 11 – Switching tests at minimum rated operating temperature – Digital devices (Note 2)	10	10

1. Sampling plans are based on LTPD tables of MIL-M-38510. The smaller initial sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to an acceptance number of 2. The minimum reject number in all cases is 3.
2. These subgroups are usually performed during initial device characterization only.

OPTIONAL EXTENDED PROCESSING
CLASS B
Steps 101 Through 110

Advanced Micro Devices offers several extended processing options to meet customer high-reliability requirements. These are defined in AMD document 00-003. The flow chart below outlines Option B, a 160-hr burn in. Military temperature range devices processed to this flow (in the left column) meet the screening requirements of MIL-STD-883, Class B.



OTHER OPTIONS

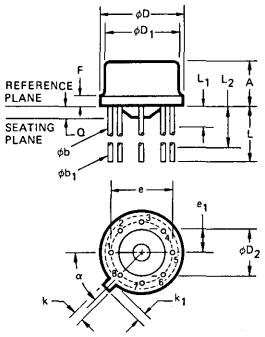
Document 00-003, "Extended Processing Options", further defines Option B as well as other screening or sampling options available or special order. Available options are listed here for reference.

Option	Description	Effect
A	Modified Class A screen (Similar to Class S screening)	Provides space-grade product, following most Class S requirements of MIL-STD-883, Method 5004.
B	160-hr operating burn in	Upgrades a part from Class C to Class B.
X	Radiographic inspection (X-ray)	Related to Option A. Provides limited internal inspection of sealed parts.
S	Scanning Electron Microscope (SEM) metal inspection	Sample inspection of metal coverage of die.
V	Preseal visual inspection to MIL-STD-883, Method 2010, Cond. A	More stringent visual inspection of assemblies and die surfaces prior to seal.
P	Particle impact noise (PIN) screen with ultrasonic detection.	Detects loose particles of approximately 0.5 mil size or larger, which could affect reliability in zero-G or high vibration applications.
Q	Quality conformance inspection (Group B, C and D life and environmental tests)	Samples from the lot are stressed and tested per Method 5005. The customer's order must state which groups are required. Group B destroys 16 devices; Group C, 92 devices; Group D, 60 devices.

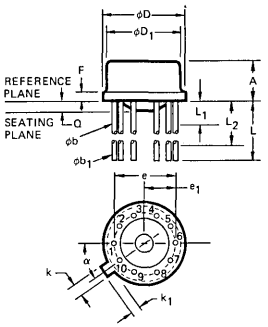
Package Outlines

METAL CAN PACKAGES

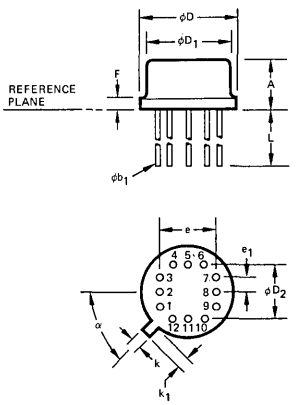
H-8-1



H-10-1



G-12-1



AMD Pkg.	H-8-1		H-10-1		G-12-1	
Common Name	TO-99 Metal Can		TO-100 Metal Can		TO-8 Metal Can	
38510 Appendix C	A-1		A-2		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.
A	.165	.185	.165	.185	.155	.180
e	.185	.215	.215	.245	.390	.410
e_1	.090	.110	.105	.125	.090	.110
F	.013	.033	.013	.033	.020	.030
k	.027	.034	.027	.034	.024	.034
k_1	.027	.045	.027	.045	.024	.038
L	.500	.570	.500	.610	.500	.600
L_1		.050		.050		
L_2	.250		.250			
α	45° BSC		36° BSC		45°	
ϕb	.016	.019	.016	.019		
ϕb_1	.016	.021	.016	.021	.016	.021
ϕD	.350	.370	.350	.370	.590	.610
ϕD_1	.305	.335	.305	.335	.540	.560
ϕD_2	.120	.160	.120	.160	.390	.410
Q	.015	.045	.015	.045		

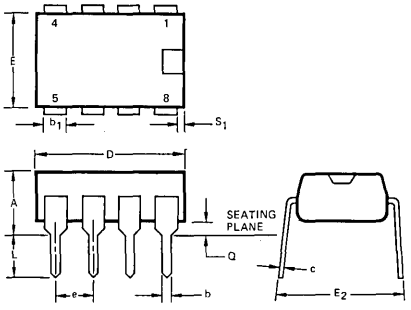
Notes: 1. Standard lead finish is bright acid tin plate or gold plate.
2. ϕb applies between L_1 and L_2. ϕb_1 applies between L_1 and 0.500" beyond reference plane.

7

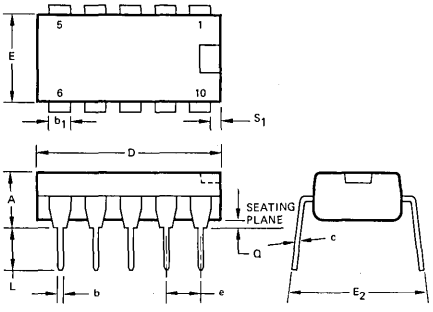
PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES

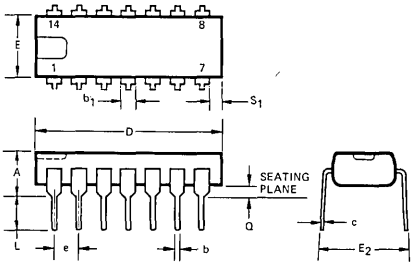
P-8-1



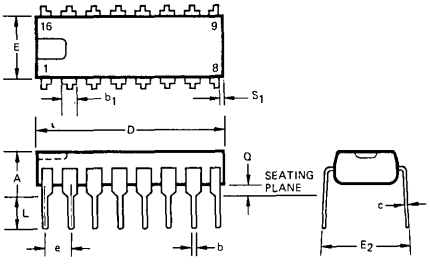
P-10-1



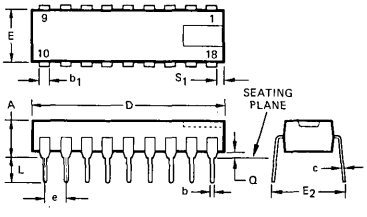
P-14-1



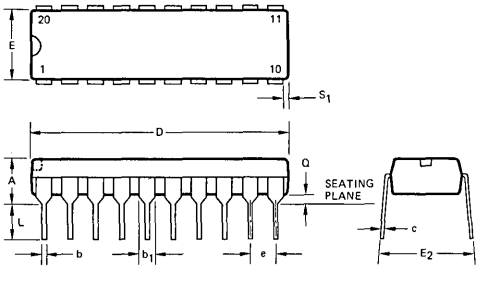
P-16-1



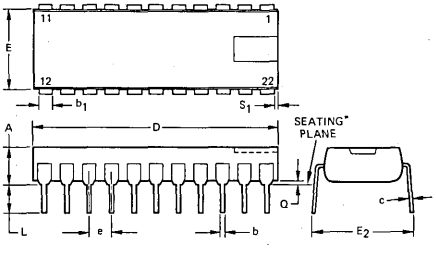
P-18-1



P-20-1



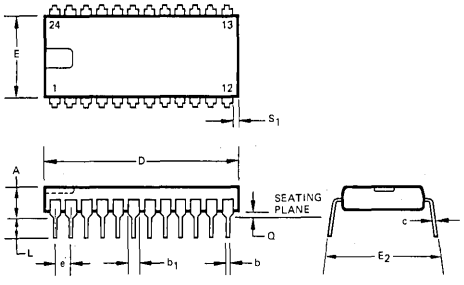
P-22-1



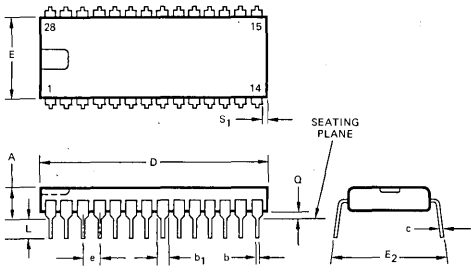
PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES (Cont.)

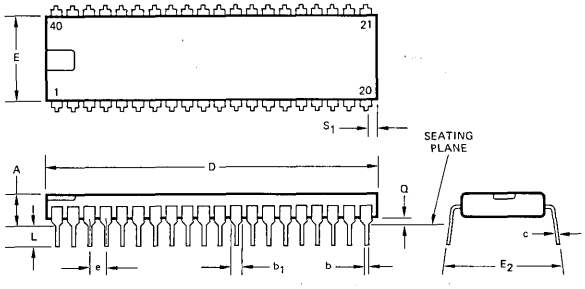
P-24-1



P-28-1



P-40-1



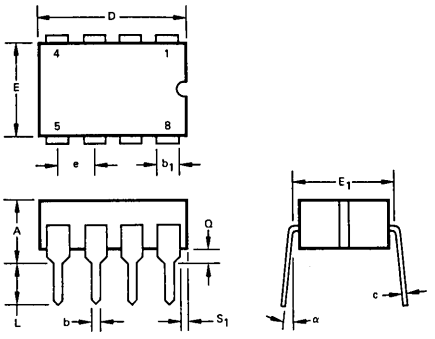
AMD Pkg.	P-8-1		P-10-1		P-14-1		P-16-1		P-18-1		P-20-1		P-22-1		P-24-1		P-28-1		P-40-1	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.150	.200	.150	.200	.150	.200	.150	.200	.150	.200	.150	.200	.150	.200	.170	.215	.150	.200	.150	.200
b	.015	.022	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020
b_1	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065
c	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011
D	.375	.395	.505	.550	.745	.775	.745	.775	.895	.925	1.010	1.050	1.080	1.120	1.240	1.270	1.450	1.480	2.050	2.080
E	.240	.260	.240	.260	.240	.260	.240	.260	.240	.260	.250	.290	.330	.370	.515	.540	.530	.550	.530	.550
E_2	.310	.385	.310	.385	.310	.385	.310	.385	.310	.385	.310	.385	.410	.480	.585	.700	.585	.700	.585	.700
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.125	.150	.125	.150	.125	.150	.125	.150	.125	.160	.125	.160	.125	.160	.125	.160
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S_1	.010	.030	.040	.070	.040	.065	.010	.040	.030	.040	.025	.055	.015	.045	.035	.065	.040	.070	.040	.070

Notes: 1. Standard lead finish is tin plate or solder dip.
2. Dimension E_2 is an outside measurement.

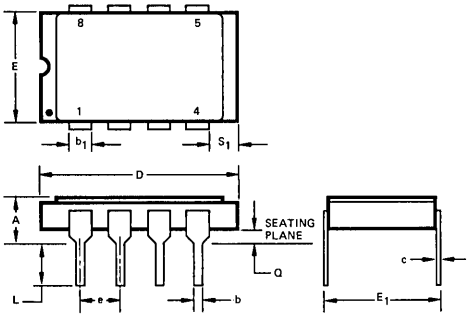
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES

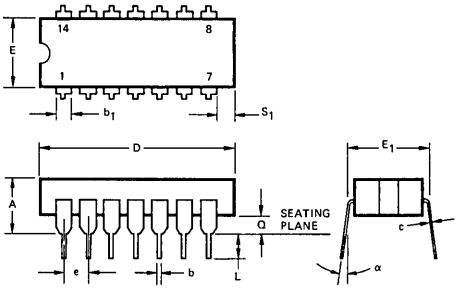
D-8-1



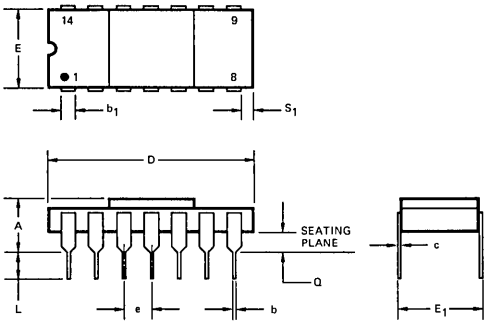
D-8-2



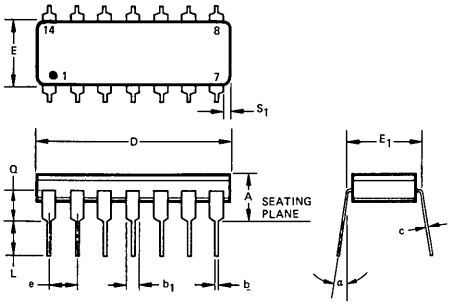
D-14-1



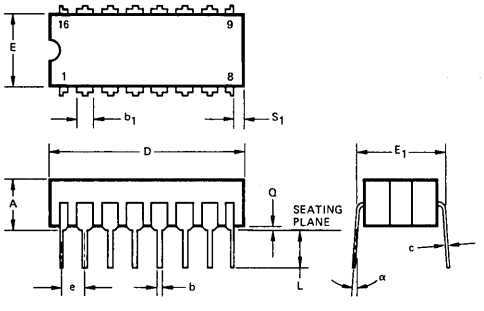
D-14-2



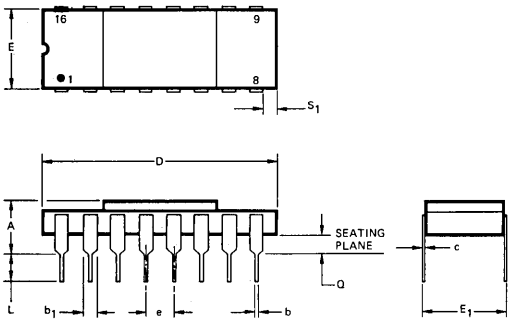
D-14-3



D-16-1



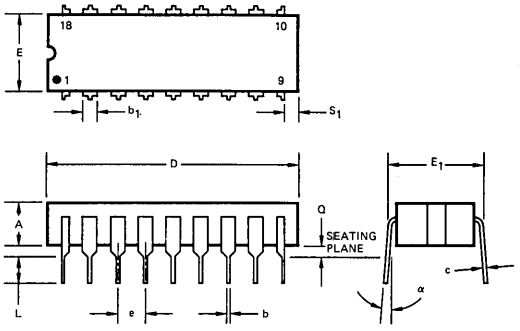
D-16-2



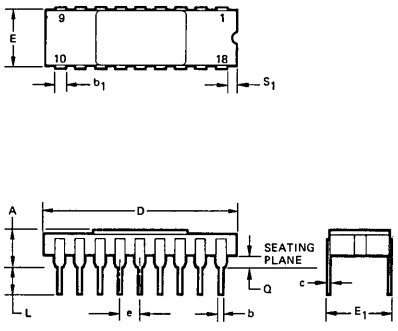
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

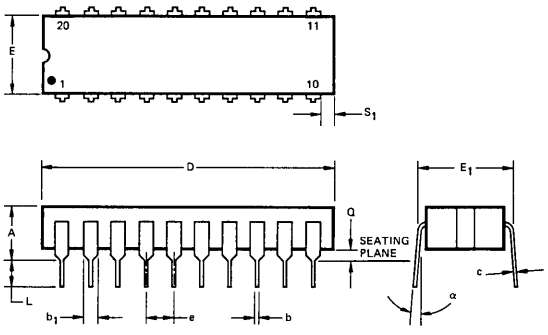
D-18-1



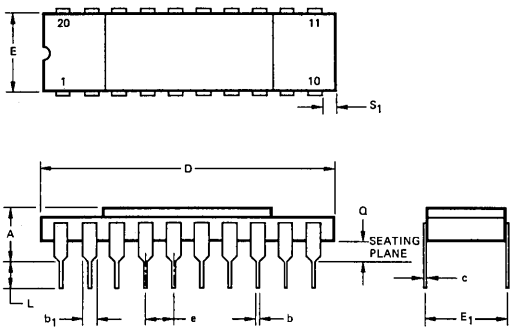
D-18-2



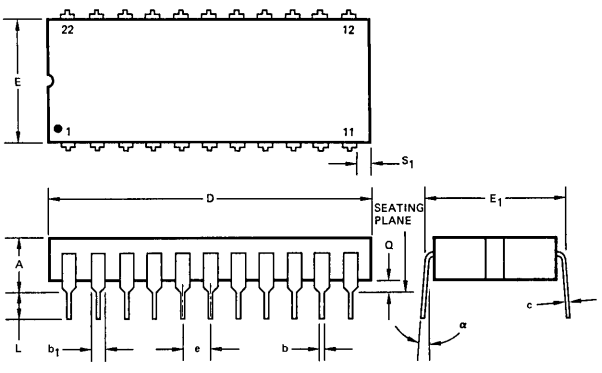
D-20-1



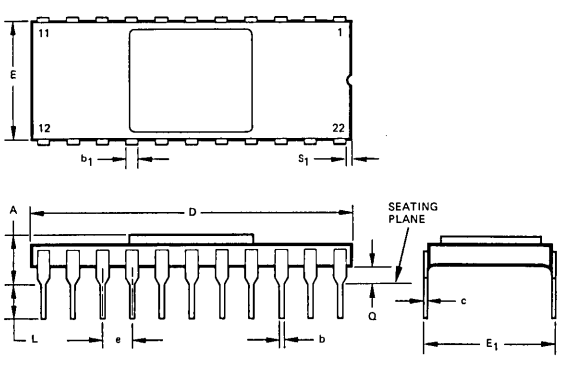
D-20-2



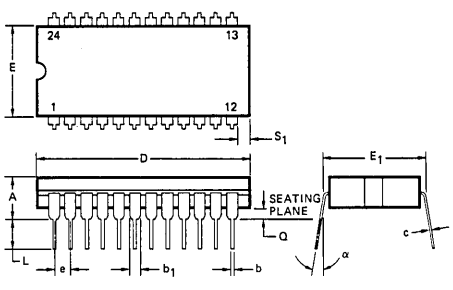
D-22-1



D-22-2



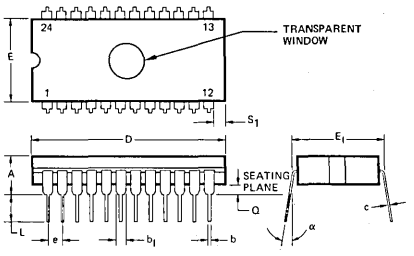
D-24-1 and D-24-4



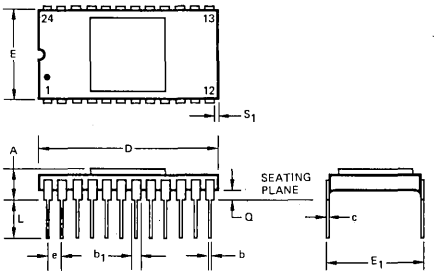
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

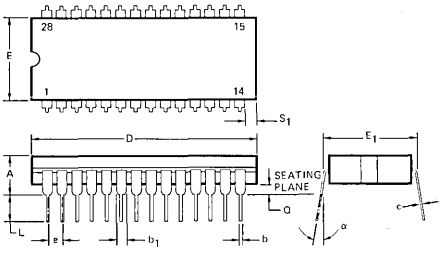
D-24-4*



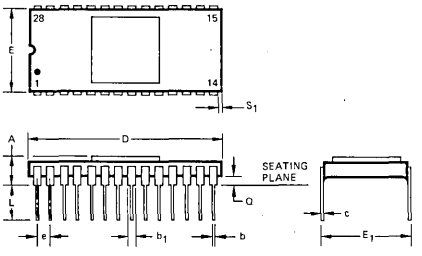
D-24-2



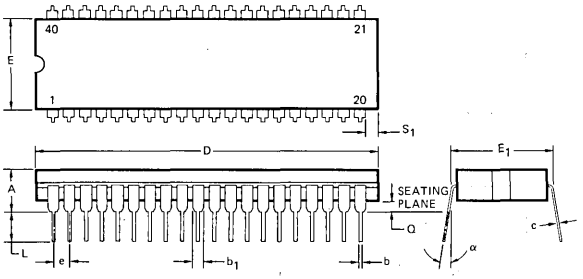
D-28-1



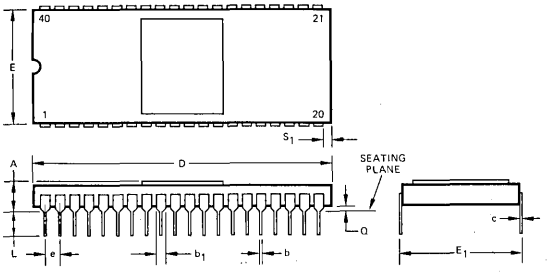
D-28-2



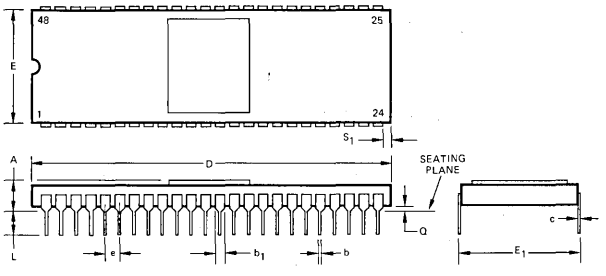
D-40-1



D-40-2



D-48-2



PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

AMD Pkg.	D-8-1		D-8-2		D-14-1		D-14-2		D-14-3 (Note 2)		D-16-1		D-16-2	
Common Name	CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		METAL DIP		CERDIP		SIDE-BRAZED	
38510 Appendix C	–		–		D-1(1)		D-1(3)		D-1(1)		D-2(1)		D-2(3)	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.130	.200	.100	.200	.130	.200	.100	.200	.100	.200	.130	.200	.100	.200
b	.016	.020	.015	.022	.016	.020	.015	.022	.015	.023	.016	.020	.015	.022
b_1	.050	.070	.040	.065	.050	.070	.040	.065	.030	.070	.050	.070	.040	.065
c	.009	.011	.008	.013	.009	.011	.008	.013	.008	.011	.009	.011	.008	.013
D	.370	.400	.500	.540	.745	.785	.690	.730	.660	.785	.745	.785	.780	.820
E	.240	.285	.260	.310	.240	.285	.260	.310	.230	.265	.240	.310	.260	.310
E_1	.300	.320	.290	.320	.290	.320	.290	.320	.290	.310	.290	.320	.290	.320
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.160	.125	.150	.125	.160	.100	.150	.125	.150	.125	.160
Q	.015	.060	.020	.060	.015	.060	.020	.060	.020	.080	.015	.060	.020	.060
S_1	.004		.005		.010		.005		.020		.005		.005	
α	3°	13°			3°	13°			3°	13°	3°	13°		
Standard Lead Finish	b		b or c		b		b or c		c		b		b or c	

AMD Pkg.	D-18-1		D-18-2		D-20-1		D-20-2		D-22-1		D-22-2		D-24-1	
Common Name	CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		CERDIP	
38510 Appendix C	–		–		–		–		–		–		D-3(1)	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.130	.200	.100	.200	.140	.220	.100	.200	.140	.220	.100	.200	.150	.225
b	.016	.020	.015	.022	.016	.020	.015	.022	.016	.020	.015	.022	.016	.020
b_1	.050	.070	.040	.065	.050	.070	.040	.065	.045	.065	.030	.060	.045	.065
c	.009	.011	.008	.013	.009	.011	.008	.013	.009	.011	.008	.013	.009	.011
D	.870	.920	.850	.930	.935	.970	.950	1.010	1.045	1.110	1.050	1.110	1.230	1.285
E	.280	.310	.260	.310	.245	.285	.260	.310	.360	.405	.360	.410	.510	.545
E_1	.290	.320	.290	.320	.290	.320	.290	.320	.390	.420	.390	.420	.600	.620
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.160	.125	.150	.125	.160	.125	.150	.125	.160	.120	.150
Q	.015	.060	.020	.060	.015	.060	.020	.060	.015	.060	.020	.060	.015	.060
S_1	.005		.005		.005		.005		.005		.005		.010	
α	3°	13°			3°	13°			3°	13°			3°	13°
Standard Lead Finish	b		b or c		b		b or c		b		b or c		b	

PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

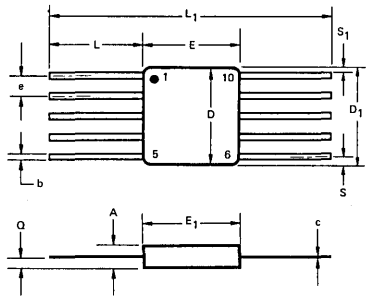
AMD Pkg.	D-24-2		D-24-4/D-24-4*		D-28-1		D-28-2		D-40-1		D-40-2		D-48-2	
Common Name	SIDE-BRAZED		CERVIEW		CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		SIDE-BRAZED	
38510 Appendix C	D-3(3)		–		–		–		D-5		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.100	.200	.150	.225	.150	.225	.100	.200	.150	.225	.100	.200	.100	.200
b	.015	.022	.016	.020	.016	.020	.015	.022	.016	.020	.015	.022	.015	.022
b_1	.030	.060	.045	.065	.045	.065	.030	.060	.045	.065	.030	.060	.030	.060
c	.008	.013	.009	.011	.009	.011	.008	.013	.009	.011	.008	.013	.008	.013
D	1.170	1.200	1.235	1.280	1.440	1.500	1.380	1.420	2.020	2.100	1.960	2.040	2.370	2.430
E	.550	.610	.510	.550	.510	.550	.560	.600	.510	.550	.550	.610	.570	.610
E_1	.590	.620	.600	.630	.600	.630	.590	.620	.600	.630	.590	.620	.590	.620
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.120	.160	.120	.150	.120	.150	.120	.160	.120	.150	.120	.160	.125	.160
Q	.020	.060	.015	.060	.015	.060	.020	.060	.015	.060	.020	.060	.020	.060
S_1	.005		.010		.005		.005		.005		.005		.005	
α			3°	13°	3°	13°			3°	13°				
Standard Lead Finish	b or c				b		b		b		b or c		b or c	

Notes: 1. Load finish b is tin plate. Finish c is gold plate.
2. Used only for LM108/LM108A.
3. Dimensions E and D allow for off-center lid, meniscus and glass overrun.

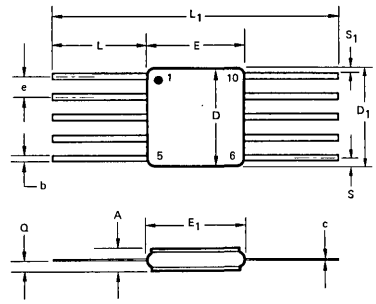
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES

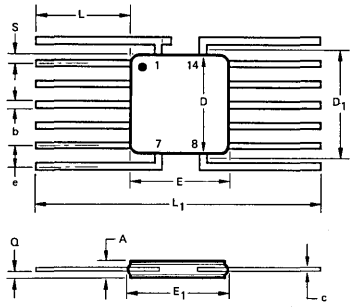
F-10-1



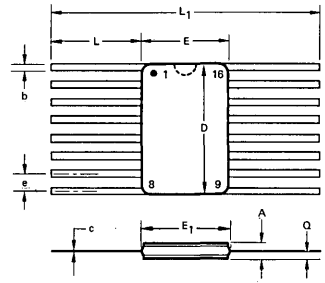
F-10-2



F-14-1 and F-14-2

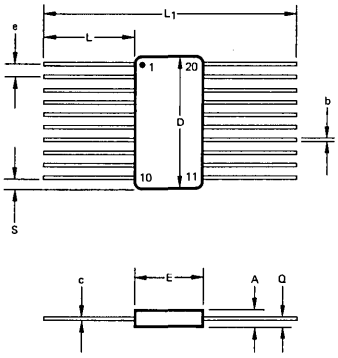


F-16-1 and F-16-2

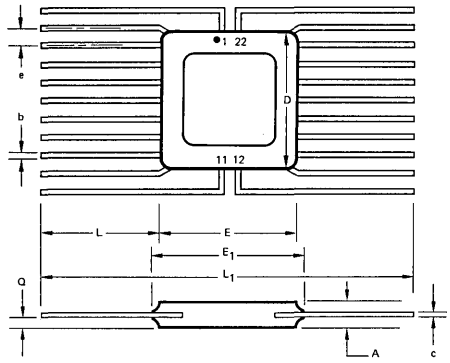


Note: Notch is pin 1 index on cerpack.

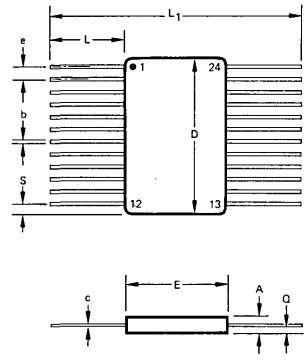
F-20-1



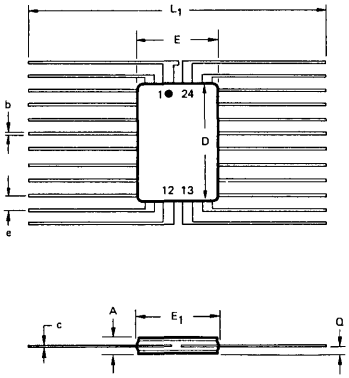
F-22-1



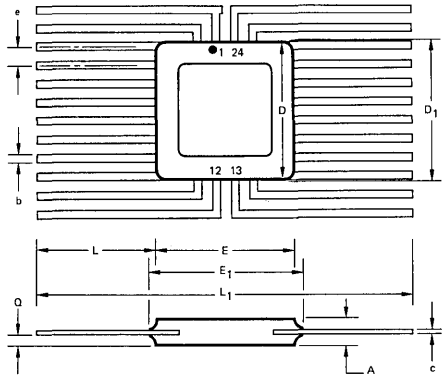
F-24-1



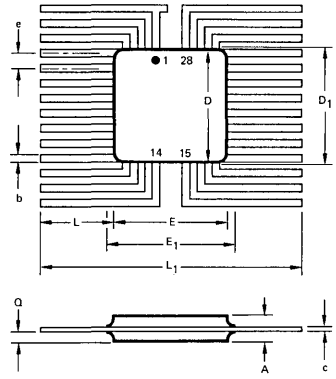
F-24-2



F-24-3



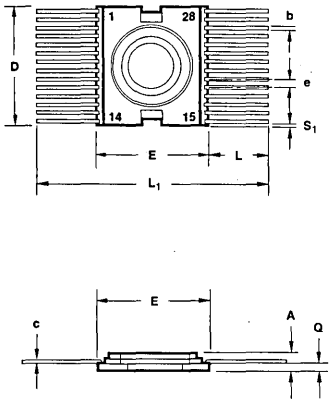
F-28-1



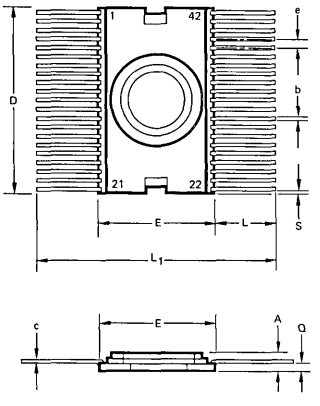
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES (Cont.)

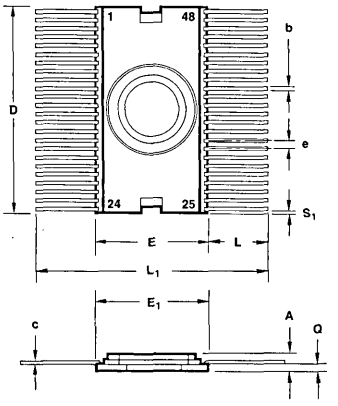
F-28-2



F-42-1



F-48-2

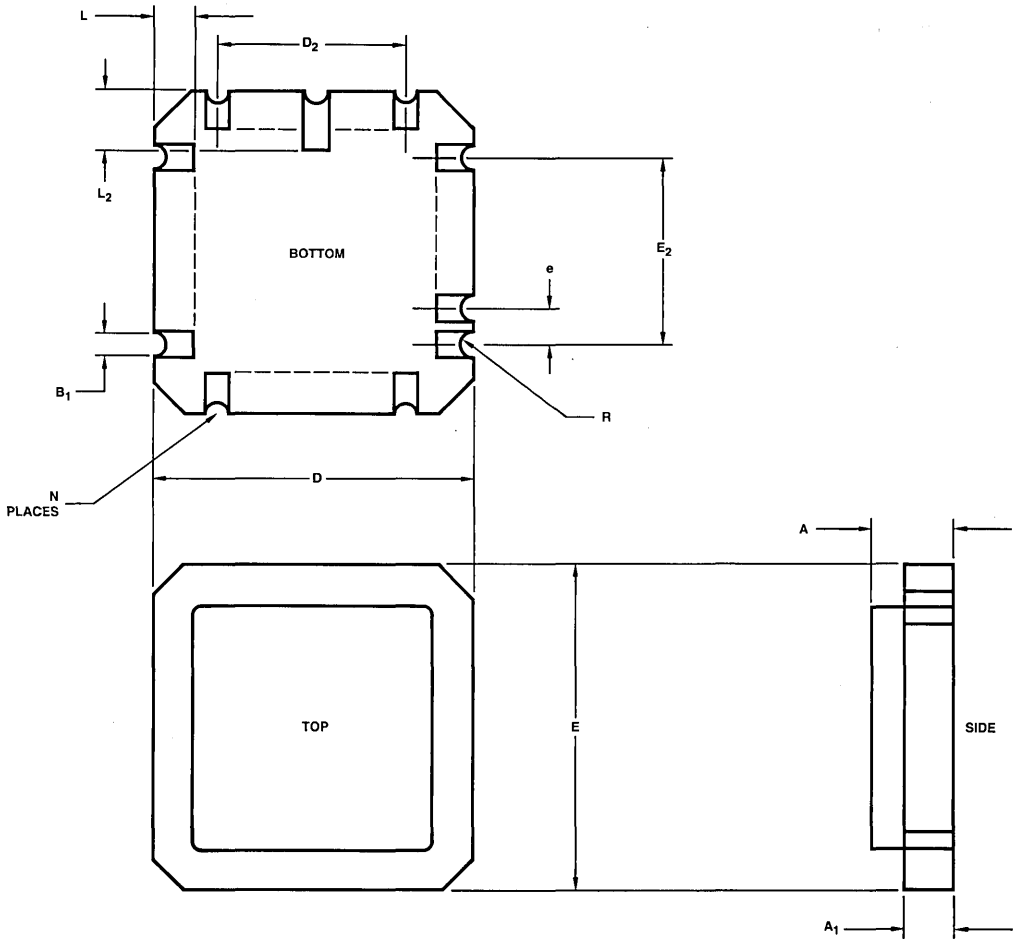


AMD Pkg.	F-10-1		F-10-2		F-14-1		F-14-2		F-16-1		F-16-2		F-20-1		F-22-1	
Common NAME	CERPACK		METAL FLAT PAK		CERPACK		METAL FLAT PAK		CERPACK		METAL FLAT PAK		CERPACK		METAL FLAT PAK	
38510 Appendix C	F-4		F-4		.F-1		F-1		F-5		–		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.045	.080	.045	.080	.045	.080	.045	.085	.045	.085	.045	.085	.045	.085	.045	.090
b	.015	.019	.012	.019	.015	.019	.012	.019	.015	.019	.015	.019	.015	.019	.015	.019
c	.004	.006	.003	.006	.004	.006	.003	.006	.004	.006	.003	.006	.004	.006	.003	.006
D	.230	.255	.235	.275	.230	.255	.230	.270	.370	.425	.370	.400	.490	.520	.380	.420
D_1				.275				.280				.410				.440
E	.240	.260	.240	.260	.240	.260	.240	.260	.245	.285	.245	.285	.245	.285	.380	.420
E_1		.275		.280		.275		.280		.290		.305		.290		.440
e	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055
L	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.250	.320
L_1	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980
Q	.010	.040	.010	.040	.010	.040	.010	.040	.020	.040	.010	.040	.020	.040	.010	.040
S_1	.005		.005		.005		.005		.005		.005		.005			
Standard Lead Finish	b		c		b		c		b		c		b		c	

AMD Pkg.	F-24-1		F-24-2		F-24-3		F-28-1		F-28-2		F-42-1		F-48-2	
Common Name	CERPACK		METAL FLAT PAK		METAL FLAT PAK		METAL FLAT PAK		CERAMIC FLAT PAK		CERAMIC FLAT PAK		CERAMIC FLAT PAK	
38510 Appendix C	F-6		F-8		–		–		–		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.050	.090	.045	.090	.045	.090	.045	.080	.065	.085	.070	.115	.070	.110
b	.015	.019	.015	.019	.015	.019	.015	.019	.016	.025	.017	.023	.018	.022
c	.004	.006	.003	.006	.003	.006	.003	.006	.007	.010	.006	.012	.006	.010
D	.580	.620	.360	.410	.380	.420	.360	.410	.700	.720	1.030	1.090	1.175	1.250
D_1				.420		.440		.410		.720		1.090		1.250
E	.360	.385	.245	.285	.380	.420	.360	.410	.625	.650	.620	.660	.615	.670
E_1		.410		.305		.440		.410		.650		.660		.670
e	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055
L	.265	.320	.300	.370	.250	.320	.270	.320	.415	.435	.320	.370	.320	.370
L_1	.920	.980	.920	.980	.920	.980	.955	1.000	1.475	1.500	1.300	1.370	1.310	1.365
Q	.020	.040	.010	.040	.010	.040	.010	.040	.017	.025	.020	.060	.020	.055
S_1	.005		.005		0		0		.005		.005		.015	
Standard Lead Finish	b		c		c		c		c		c		c	

Notes: 1. Lead finish b is tin plate. Finish c is gold plate.
2. Dimensions E_1 and D_1 allow for off-center lid, meniscus, and glass overrun.

SQUARE CHIP CARRIER FAMILY (L-XX-1)



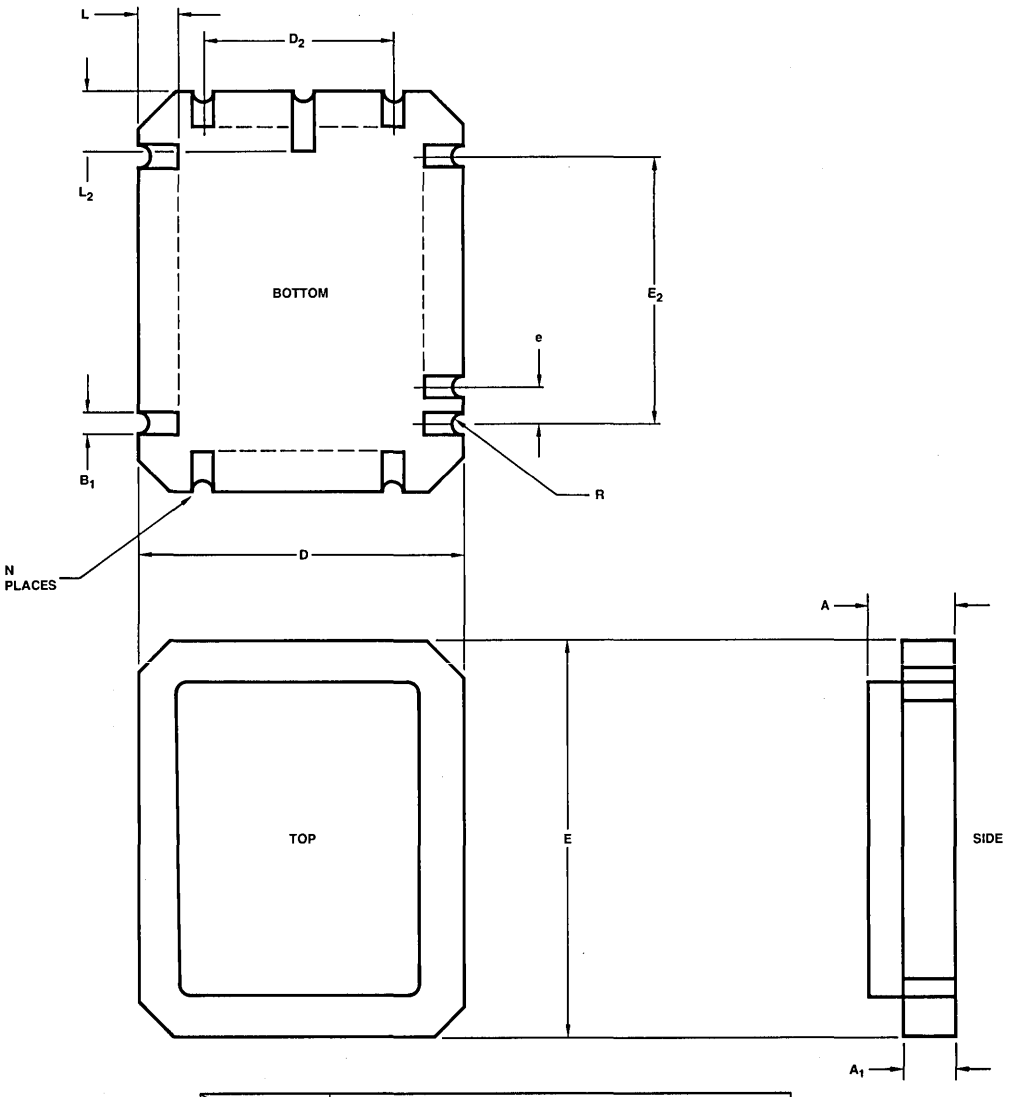
Limit / Symbol	Inches									
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	.064	.100	.064	.100	.064	.120	.082	.120		
A_1	.054	.088	.054	.088	.054	.088	.072	.088		
B_1	.022	.028	.022	.028	.022	.028	.022	.028		
D	.342	.358	.442	.458	.640	.660	.739	.761		
D_2	.190	.210	.290	.310	.490	.510	.590	.610		
E	.342	.358	.442	.458	.640	.660	.739	.761		
E_2	.190	.210	.290	.310	.490	.510	.590	.610		
e	.045	.055	.045	.055	.045	.055	.045	.055		
L	.045	.055	.045	.055	.045	.055	.045	.055		
L_2	.077	.093	.077	.093	.077	.093	.077	.093		
N	20 (5 x 5)		28 (7 x 7)		44 (11 x 11)		52 (13 x 13)		68	
R	.007	.011	.007	.011	.007	.011	.007	.011		
Outline	L-20-1		L-28-1		L-44-1		L-52-1		L-68-1	

TO BE DETERMINED

7

Package Outlines

RECTANGULAR CHIP CARRIER FAMILY (L-XX-2)



Limit / Symbol	Inches					
	Min	Max	Min	Max	Min	Max
A	.060	.120	.060	.120	.060	.120
A_1	.050	.088	.050	.088	.050	.088
B_1	.022	.028	.022	.028	.022	.028
D	.280	.305	.342	.358	.442	.458
D_2	.140	.160	.190	.210	.290	.310
E	.345	.365	.540	.560	.540	.560
E_2	.190	.210	.390	.410	.390	.410
e	.045	.055	.045	.055	.045	.055
L	.045	.055	.045	.055	.045	.055
L_2	.077	.093	.077	.093	.077	.093
N	18 (4 x 5)		28 (5 x 9)		32 (7 x 9)	
R	.007	.011	.007	.011	.007	.011
Outline	L-18-2		L-28-2		L-32-2	

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