BURR-BROWN®

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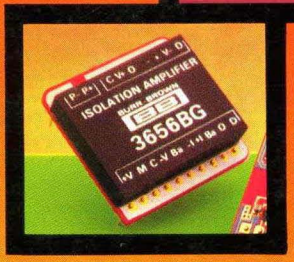
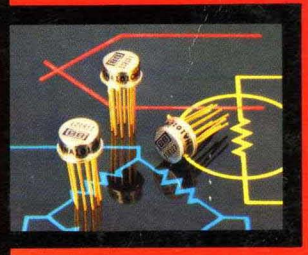
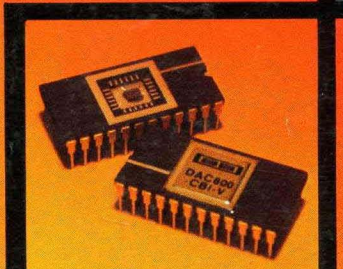






product data book

BURR-BROWN® product data book

MODEL INDEX

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734
Tel (602) 746-1111 - TWX: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PRODUCT DATA BOOK

LI-269

Printed in U.S.A. July, 1982

Building an Unequalled Reputation, Worldwide, for Quality, Performance, Reliability

Data acquisition, signal conditioning, and computer I/O components and systems from Burr-Brown are recognized and used worldwide. Over the past two decades these products have earned a reputation for superior quality, exceptional performance, and consistent reliability - perhaps the best reputation for workmanship in our industry.

Cost effectiveness of our products has been proven in a host of applications: in industrial and process control, test instrumentation, aerospace systems, environmental monitoring, medical-clinical, and analytical instrumentation.

We have built our credibility by being totally responsive to our customers' requirements. Knowing the problems encountered in the real world, we apply the best, most appropriate, and proven technologies to achieve practical solutions.

Our components have become more complex, more sophisticated as we continue to combine and vertically integrate multiple functions into smaller, space-saving packages. When you select these versatile "mini-systems" your design and assembly time is decreased while your products' performance and reliability are increased. And today you pay less, per function, as these microcircuits and subsystems work more efficiently for you.

At Burr-Brown, quality and reliability are built-in by conservative designs, carefully selected components and manufacturing processes, by intensive, thorough testing, and stringent quality control.

Customers also give Burr-Brown high marks for service and support. Our technical literature is among the best in the industry and our global applications and sales force is factory trained ... highly qualified to help you in product selection and use. Wherever in the world you contact us, you can be assured of prompt, courteous, efficient service - and superb product performance.

BURR-BROWN PRODUCT DATA BOOK

The Burr-Brown Product Data Book contains detailed product data sheets for our broad line of precision components for signal processing, data acquisition, and data transmission. In addition, it includes supplementary data for these components, such as screening programs available, a list of other technical literature that you may order, accessories, and information on how to interface with Burr-Brown.

To acquaint you with the full breadth of the Burr-Brown product line, we also include information on the products from our Industrial Systems Division. Additional detailed manuals are available for most of these products upon request. Contact your local Burr-Brown Sales Office listed inside the back cover.

For your convenience the Data Book is separated into twelve major sections: Operational Amplifiers, Instrumentation Amplifiers, Isolation Amplifiers, Fiber Optic Data Links, Analog Circuit Functions, Data Conversion and Acquisition, Military Products, Modular Power Supplies, Microcomputer I/O Systems, Data Entry and Display Terminals, Industrial Systems Products, and Accessories. Each page has a margin tab on the outer edge which indicates both product type and part number. The tab index on page V provides a visual guide to the major sections.

At the beginning of each product section, you will find explanatory material and a selection guide to assist you in selecting the products most suitable for your applications. The selection guide also contains page numbers for individual product data sheets.

An index of products in this Data Book, listed in alphanumeric order, is found on the inside of the front cover. A general table of contents appears on page IV.

TABLE OF CONTENTS

TAB INDEX

INTERFACING WITH BURR-BROWN

PLACING AN ORDER

Orders may be placed via mail, telephone, TWX or TELEX with any authorized Burr-Brown field sales office, sales representative, or our headquarters in Tucson. Our offices are listed inside the back cover of this Data Book. When placing your order, please provide complete information, including model number with all option designations, product description or name, quantity desired, and ship-to and bill-to addresses.

TECHNICAL ASSISTANCE

Burr-Brown has a large and competent field sales force, backed-up by an experienced staff of applications specialists. They will be most happy to assist you in selecting the right product for your application. This service is available, without charge, from all sales offices and from our headquarters in Tucson.

DATA SHEETS/LITERATURE

Product data sheets or manuals, similar to those in this Data Book but perhaps containing more recent revisions, are available for most of the products listed in this Data Book. Application Notes and other supporting literature are also available on request. If you wish a copy of any of these items simply contact your nearest Burr-Brown sales office or representative.

PRICES AND TERMS

Prices listed in this catalog, unless otherwise noted, apply only to domestic USA customers; all other customers should contact their local Burr-Brown representative for price information.

All prices are FOB Tucson, Arizona, USA, in U.S. dollars. Applicable federal, state, and local taxes are extra. Terms are net 30 days. Prices and specifications are subject to change without notice.

QUOTATIONS

Price quotations made by Burr-Brown or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement.

RETURNS AND WARRANTY SERVICE

When returning products for any reason, it is necessary to contact Burr-Brown, prior to shipping, for authorization and shipping instructions. In the U.S., contact our Tucson headquarters. In other countries, contact your nearest Burr-Brown field sales office or representative. Returned units should be shipped prepaid and must be accompanied by the original purchase order number and date, and an explanation of the malfunction. Upon receipt of the returned unit, Burr-Brown will verify the malfunction and will inform you of the warranty status, cost to repair or replace, credits, and status of replacement units where applicable.

STILL AVAILABLE...

The following list includes the more popular Burr-Brown models that are not listed elsewhere in this catalog. We realize that these models are "designed into" a great number of applications. We also realize that it is usually not economical for you to re-design in order to take advantage of newer products, even though they offer lower cost. Consequently, we want to assure you of the continuing availability of these older models.

However, we feel obligated to remind you that in many cases, these models may not be the best choices for your new designs. For your convenience, we have suggested newer models giving similar performance at lower cost.

Model Series	Nearest Equivalent	Model Series	Nearest Equivalent	Model Series	Nearest Equivalent	Model Series	Nearest Equivalent
ADC40	ADC80, ADC85	3016/25	3329/03	3421K	3523K	3600K	3606AG/BG
DAC12QZ	DAC80	3038/25	3581J, 3582J	3421L	3523L	3601J	3606AG/BG
DAC40	DAC80	3307/12C	3522K	3440J	3510BM	3601K	3606AG/BG
SDM850	SDM853	3308/12C	3522K	3440K	3510CM	3602J	3606AG/BG
SDM851	SDM853	3341/15C	3554BM	3440L	3510CM	3602K	3606AG/BG
SHC23	SHC80	3342/15C	3554AM	3460	3580J	3622	3620
SHM40	SHC85	3400	3554AM	3503A	3542J	3625	3626
SHM41	SHC85	3401	3550K	3503B	3522J	4095/15	4213
UAF15	UAF41	3402	3550K	3503R	3542S	4096/15	4213
UAF25	UAF41	3420J	3521J	3503S	3522S	4118/25	4301
501	553	3420K	3521K	3505J	3507J	4130	4341
1538A/25	3293	3420L	3521L	3506J	3508J	4131	4341
1541/25	3580J	3421J	3523J	3600J	3606AG/BG		

HIGH RELIABILITY PROGRAMS

Burr-Brown is committed to providing products of high quality and reliability. This is manifested by designing for conservative stress levels, careful selection of components and processes, comprehensive testing procedures, thorough quality control practices, and optional programs of military screening. The Burr-Brown Q-Progam, described below, is intended as a reliable enhancement of standard Burr-Brown products by subjecting them to a defined program of environmental stresses.

An even more comprehensive reliability program, aimed particularly at the needs of military customers, is the /MIL program which includes manufacturing procedures per MIL-M-38510 and screening procedures per MIL-STD-883. This program, and the products available under it, are described in section seven of this Data Book.

THE Q-PROGRAM

The Burr-Brown Q-Program is designed to further enhance the reliability of Burr-Brown microcircuits at a reasonable cost. The Q-Program is appropriate for some military and aerospece applications, industrial control systems, medical patient monitoring instrumentation, and other applications where failure may be expensive or where replacement of parts is difficult and incovenient. The Q-Program consists of the screening of standard Burr-Brown microcircuits in accordance with applicable test methods of MIL-STD-883. The screening sequences shown below identify the mechanical, electrical, and thermal stresses applied to all Q-Products.

Q-SCREENING SEQUENCE

STEP	SCREEN	PROCEDURE
Routinely performed 100% on all Burr-Brown products	INTERNAL VISUAL INSPECTION (precap)	Burr-Brown QC4118 (copies available on request)
	ELECTRICAL TEST, 100% (postcap)	Per appropriate Burr-Brown product data sheet
①	STABILIZATION BAKE	MIL-STD-883, Method 1008
②	TEMPERATURE CYCLING	MIL-STD-883, Method 1010
③	HERMETICITY, GROSS LEAK	MIL-STD-883, Method 1014
④	HERMETICITY, FINE LEAK	MIL-STD-883, Method 1014
⑤	BURN-IN	MIL-STD-883, Method 1015
⑥	CONSTANT ACCELERATION (centrifuge)	MIL-STD-883, Method 2001
⑦	FINAL ELECTRICAL TEST	Per appropriate Burr-Brown product data sheet

Explanation of Screening Steps...

- **INTERNAL VISUAL INSPECTION**

  This is a microscopic examination of the product performed prior to capping in order to verify conformance to Burr-Brown standards of quality for material, methods of construction, and workmanship. Its purpose is to detect and eliminate devices with internal defects which could lead to failures under the thermal, mechanical, and electrical stresses of extended operation.

- **100% ELECTRICAL TEST**

  Each product is tested in accordance with the appropriate Burr-Brown product data sheet. These tests will normally include static and dynamic tests at +25°C, as well as drift tests over the operating temperature range.

①STABILIZATION BAKE

In this step the product is stored at an elevated temperature without electrical stress applied. The purpose is to stabilize circuit parameters through accelerated aging.

②TEMPERATURE CYCLING

The product is alternately exposed to extremes of high and low temperature such as would be experienced when parts or equipment are transferred to and from heated shelters in arctic areas. The purpose is to check for permanent changes in operating characteristics and physical damage resulting principally from variation in dimensions and other physical properties.

③④HERMETICITY - GROSS AND FINE LEAK

The purpose of these two tests is to verify the hermeticity of the seal of integrated circuits having internal cavities whichare evacuated or filled with gas. The test is intended to determine those devices which, when exposed for long periode to atmosphere containing high concentration of water vapor or other gaseous contaminants, would degrade in performance and become latent failures.

⑤BURN-IN

During burn-in the device is subjected to a high temperature for an extended period of time, with power applied. The burn-in screen is performed in order to eliminate marginal devices with inherent defects. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions.

⑥CONSTANT ACCELERATION

This test subjects the product to a constant acceleration force in a centrifuge. The purpose is to detect and eliminate devices having structural and mechanical weaknesses that could lead to failure when subjected to mechanical stresses during application.

⑦FINAL ELECTRICAL TEST

This is a repetition of the 100% electrical test above. Devices which pass this test, after successfully passing the above screening test, are qualified as Q-parts.

HANDLING PROCEDURES FOR MICROCIRCUITS

In developing handling procedures for microcircuits it is well to keep in mind that virtually all semiconductor devices are vulnerable in some degree to damage from the discharge of electrostatic energy. This is due to the small dimensions involved. It should be noted that electrostatic damage (ESD) to semiconductor devices can cause effects ranging from a degradation in performance, to latent failure, or immediate failure, of the device involved.

We at Burr-Brown are directly concerned with this subject because our products are designed to achieve the highest performance and precision. Often, this depends upon a high degree of device matching or precision within the microcircuit and any degradation due to ESD is unacceptable. Accordingly, we have developed a set of guidelines that will minimize the exposure of our products to possible electrostatic damage during manufacturing and handling at Burr-Brown. We strongly recommend that our customers adopt similar procedures throughout their handling and utilization of these and other semiconductor products. These guidelines are summarized below:

GUIDELINES

1. Eliminate souces of ESD by removing static generating materials from all areas that handle products, by grounding all operators, equipment, and work stations where products are handled or stored, and by transporting and shipping products in static-free containers.
2. Shield products from potential damage by using a conductive Faraday shield where practical.
3. Shunt electrostatic charges and voltage potentials to zero where practical by connecting together all leads of each device by means of a conductive material.

ELIMINATE SOURCES OF ESD

It is highly desirable to eliminate static-generating materials from close proximity to products. This includes the elimination of all plastics, such as wrapping and packing materials, which have not been properly treated to achieve antistatic properties.

Antistatic is a term used to describe insulators which have been treated to reduce their very high surface resistance from a value in excess of a million meghoms to a value in the vicinity of one megohm.

The human body has been electrically characterized as a capacitor ranging from 100 to 200 picofarads and a resistance ranging from 500 ohms to several thousand ohms. As in electrical applications, the best way to prevent an accumulation of charge, or to drain the accumulation of existing charge on a capacitor, is to short the capacitor terminals together. The body is one plate of the capacitor with earth being the other. The only way to effectively short this capacitor is to connect the body to earth ground. For reasons of safety, this connection should include approximately one megohm of series resistance, or a ground fault interrupter. There should be periodic measurement to assure proper continuity all the way from the wrist strap connection to earth ground, and that the safety protection is operational. The wrist strap must have continuity to the skin in order to drain off the accumulated charge. Work station surfaces should be metallic or conductive plastic and should also be grounded through one megohm of series resistance, or have ground fault interrupters.

Static-free containers are important in storing and transporting product because the product could act as one plate of the capacitor and the container the other plate. Thus, it is possible to induce a charge, and therefore create a voltage, on the product without ohmic contact. Because of area and spacing considerations only unusual situations could cause damage, but it is nevertheless a possibility.

SHIELDING

In even the most optimum environments, there is always the potential for some accumulation of charge. The most positive control is to shield the product from potentially damaging electrostatic fields by use of a highly conductive (Faraday) shield. Antistatic enclosures or wrappers are only low enough in resistance to disperse accumulated charge. The Faraday shield must be low enough in resistance to completely conduct any electrostatic field around the product and prevent any field inside the enclosure. To be totally effective the Faraday shield must completely enclose the product. In addition, only antistatic materials may be used inside the container to assure that internal charge is not developed.

SHUNTING

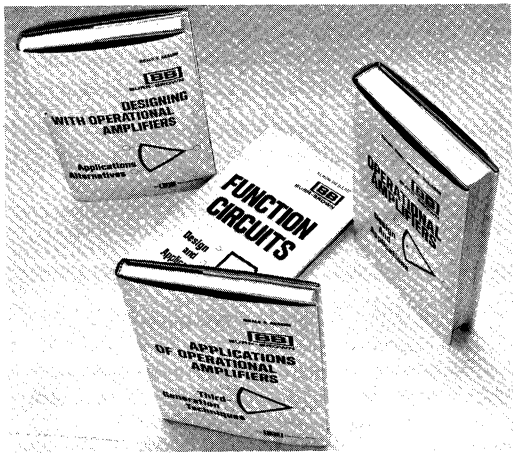
Shunting is one of the most cost-effective ways to protect products during assembly, testing, packing, unpacking, and handling. With a short circuit across sensitive terminals, it is nearly impossible to develop the voltages required for damage to occur. The limitation to this occurs when it is possible to induce large voltages internally in complex microcircuits. We can only shunt or short the exterior connections.

OTHER MEASURES

To help minimize the buildup of electrostatic charge it is desirable to control relative humidity to as high a value as practical (50% is recommended). In addition, where it is not possible to ground all surfaces, or where non-conducting surfaces cannot be completely eliminated, a good alternative may be the use of ionized air blowers.

BURR-BROWN TECHNICAL LIBRARY

The Burr-Brown engineering staff, in cooperation with McGraw-Hill have authored the world's most extensive and authoritative library dealing with the art of analog signal conditioning, conversion, and computation. These books, respected and referenced throughout the international engineering community, are available to you directly from Burr-Brown.



FUNCTION CIRCUITS

Design and Applications

This new volume in the growing Burr-Brown series is the first to deal with the multi-faceted area of analog function circuits. FUNCTION CIRCUITS explores in depth both the design theory and numerous applications for such analog functions as Multipliers, Dividers, Logarithmic Amplifiers, Exponentiators, RMS Converters, and Active Filters. It also shows clearly how to specify and test these functions, which are increasingly becoming available in the form of integrated circuits. As in previous Burr-Brown books, the emphasis is on practicality while maintaining a rigorous treatment of theory. Numerous graphs and formulas are presented to allow the user to obtain optimum circuit performance (over 300 pages and 200 illustrations).

DESIGNING WITH OPERATIONAL AMPLIFIERS

Applications Alternatives

This latest volume in Burr-Brown's well-known series on Operational Amplifiers presents a wealth of new applications and circuit techniques which have evolved since publication of the previous two books. The applications are presented in a manner that will aid the user in developing further circuits. In addition to providing completed designs, the applications include explanations of circuit operation. Practical limitations are discussed and pertinent design equations presented to allow adaptation to specific application requirements.

New applications include amplifier performance improvement techniques, signal analyzers, signal conditioners, absolute-value circuits, signal generators, computing circuits, data transmission circuits, and test an measurement circuits (approximately 270 pages and 200 illustrations).

OPERATIONAL AMPLIFIERS

Design and Applications

Covering basic theory, test methods, amplifier design techniques, and applications, this pioneer work provides *practical* information which can be directly applied to instrumentation design.

The book is divided into two principal parts and two appendices. Part I considers the design of operational amplifiers, offers insight into the factors determining performance characteristics, and outlines the techniques available for their control. Part II presents a wide range of practical operational amplifier applications, and provides sufficient descriptions of operation to permit design adaption from the specific circuits described. In Appendix A the basic theory of operational amplifiers is reviewed to provide an accompanying reference. Appendix B gives concise definitions of the performance parameters used to characterize operational amplifiers, and provides associated test circuits (over 470 pages and 300 illustrations).

APPLICATIONS OF OPERATIONAL AMPLIFIERS

Third Generation Techniques

This is the second volume in the operational amplifier series. More than just a collection of circuit or theoretical analysis, the book presents numerous applications of operational amplifiers in a variety of electronic equipment: specialized amplifiers, signal controls, processors, waveform generators, and special purpose circuits. It is a storehouse of detailed practical information, featuring numerous circuit diagrams, circuit values, pertinent design equations, error sources, and test-based comments on the efficiency of the arrangements and devices (over 230 pages and 170 illustrations).

BURR-BROWN UPDATE

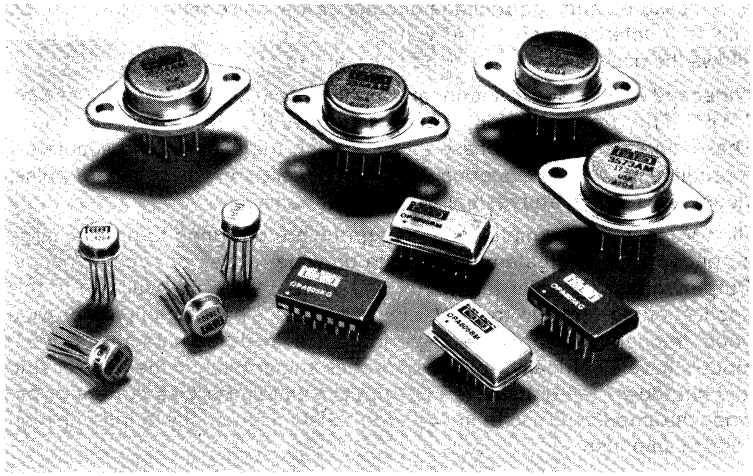
The Burr-Brown Update is published several times per year to keep our customers informed about new product developments, literature, and applications. If you would like to receive this publication on a regular basis, please contact your nearest Burr-Brown sales office or representative and ask to be put on our Update mailing list.

APPLICATION NOTES...

Burr-Brown engineers have compiled a library of Applications Notes to assist you in your designs. These notes are listed below and are available on request.

AN-58 "D/A Converter Differential Linearity Error - It Really Shows Up!"
AN-59 "Don't Forget D/A Converter Tempco!"
AN-60 "Protect Op Amps from Overloads"
AN-62 "Varying Comparator Hysteresis w/o Shifting Initial Trip Point"
AN-63 "Electronic Controller With An Equilibrium Sustaining Mode"
AN-64 "Combine Two Op Amps to Avoid the Speed Accuracy Compromise"
AN-68 "Using Op Amps in Low Noise Applications"
AN-70 "Analog Shaping"
AN-74 "Design of A Unique Precision Controlled Current Source"
AN-75 "Instrumentation Amplifiers"
AN-79 "Principles of Data Acquisition and Conversion"
AN-80 "Remote Multiplexing"
AN-83 "How to Determine What Heat Sink to Use"
AN-84 "Intrinsically Safe Data Acquisition"
AN-86 "Squeeze High Performance Out of Low Cost Hybrid Data Converters"
AN-87 "Analog I/O for Microprocessors Made Easy"
AN-88 "Software Conversion of Analog Outputs to Analog Inputs"
AN-89 "What Designers Should Know About Data Converter Drift"
AN-90 " Differential Optical Coupler Hits New High in Linearity, Stability"
AN-91 "Getting Transducers to Talk to Digital Computers"
AN-93 "Design and Application of Transformer-coupled Hybrid Isolation Amplifier Model 3656"
AN-94 "Programmable Handheld Calculator Computes Digital-to-Analog Converter Errors"
AN-95 "Using the MP8418 Microcomputer Analog I/O System"
AN-96 "Isolated Digital Input/Output Microcomputer Peripherals Solve Industrial Problems"
AN-97 "Mixed Data Link Extends Length, Reduces Cost"
AN-98 "Analog IC's Divided Accuracy to Conquer Computation Problems"
AN-99 "Static and Dynamic Testing of Digital-to-Analog Converters"
AN-100 "Testing of Analog-to-Digital Converters"
AN-101 "Correcting Errors Digitally in Data Acquisition and Control"
AN-102 "To Sidestep Track/Hold Pitfalls, Recognize Subtle Design Errors"
AN-103 "Instrumentation Amplifiers Sift Signals from Noise."
AN-105 "Advantages of ECL for High Speed, High Accuracy, D/A Conversion"
AN-106 "Diode-Connected FET Protects Op Amps."
AN-107 "Properly Designed Log Amplifiers Process Bipolar Input Signals"

OPERATIONAL AMPLIFIERS



Burr-Brown operational amplifiers are listed in eight applications groups and are described below. This enables the user to determine and select the best operational amplifier available for a design requirement. Instrumentation amplifiers and isolation amplifiers are described in sections 2 and 3 respectively

General Purpose - General purpose operational amplifiers are suited for a wide variety of applications. They give moderately good performance over a wide range of parameters at moderate cost. This applications group contains both FET and bipolar input models with frequency responses from 0.5mHz to 1.5MHz and offset voltages as low as 1mV.

Low Drift - Low Drift operational amplifiers are best suited for applications where accuracy must be preserved over a substantial temperature range. These amplifiers are optimized to minimize the initial input offset voltage and input offset voltage change with temperature. Input offset drifts from 0.1μV/°C to 10μV/°C are available within this group. Chopper-stabilized operational amplifiers represent the best available in overall accuracy and long term stability.

Low Bias Current - Low bias current operational amplifiers consist of a group of varactor diode and FET input designs. This group includes amplifiers with input bias currents from 0.01pA to 1nA. Applications with large feedback resistances or large source resistances (long time constants, integrators, current sources, etc.) and buffer applications will benefit by the use of low bias current amplifiers.

Low Noise - This group contains low noise FET input operational amplifiers. Burr-Brown units offer guaranteed noise spectral density, 100% tested. In applications like low noise signal conditioning, light measurements, radiation measurements, photodiode circuits or low noise data acquisition the fully characterized and tested voltage noise performance of these units allows the designer to truly bound noise errors.

Wideband - Wideband operational amplifiers have bandwidths greater than 10MHz. This group also contains fast settling and high slew rate amplifiers. These amplifiers reduce phase errors at high frequencies and accurately reproduce complex waveforms. These amplifiers are well suited for pulse, video, fast settling, and multiplexing applications.

High Voltage - The amplifiers in this group are designed to provide large output voltage swings and to operate on wide ranges of supply voltage. Output voltages greater than ±10V and up to ±145V are available in this applications group (up to 290V, single supply). These amplifiers provide good frequency response and performance in other parameters. Most models have electrically isolated packages and automatic thermal sensing and shutdown. All units have FET inputs to minimize bias current errors when the amplifier is used with the large resistances usually found with high voltage amplifiers.

High Current - These amplifiers provide output currents from ±10mA to ±2A (±5A peak). They are used with small load resistances, coax cable impedances, and with power booster applications. Many units have self-contained thermal sensing and shutdown to automatically protect the amplifiers from overheating and damage. All of these units have electrically isolated packages.

Unity-Gain Buffer (Power Booster) - Unity-gain buffer amplifiers have a wide variety of applications. They are used to boost the output current capability of another amplifier, to buffer an impedance that might load a critical circuit or to be an input impedance converter from an input which must not be loaded. These amplifiers may also be used inside the feedback loop of another operational amplifier to form a current-boosted, composite amplifier.

SELECTION GUIDE
Operational Amplifiers

GENERAL PURPOSE

These moderately priced FET and bipolar op amps offer good performance over a wide range of parameters. These are good options when a special function op amp is not required. Models 3500 and OPA103 are particularly worth consideration in general purpose designs.

These give moderately good performance over a wide range of parameters.

GENERAL PURPOSE															
		Offset Voltage		Bias	Open	Frequency Response		Rated Output					Price ($)		
		at 25°C	Temp Drift	Current	Loop										
		±mV	±μV/°C	nA (25°C)	Gain	Unity Gain	Slew Rate	±V	±mA	Temp					
Description	Model(1)	max	max	max	dB, min	MHz	V/μsec	min	min	Range(2)	Package	Unit	100's	Page
Bipolar	3500A	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99	9.60	5.95	1-62
	3500B	2	5	±20	93	1.5	0.8	10	10	Ind	TO-99	17.25	10.65	1-62
	3500C	1	3	±15	93	1.5	1.0	10	10	Ind	TO-99	22.00	13.90	1-62
	3500R, (Q)	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99	20.50	12.20	1-62
	3500S, (Q)	2	10	±20	93	1.5	0.8	10	10	Mil	TO-99	33.00	21.20	1-62
	3500T, (Q)	1	5	±15	93	1.5	1.0	10	10	Mil	TO-99	53.25	33.60	1-62
Military	3500/MIL Series	See Military Products												
Bipolar	3501A, (Q)	5	20	±15	93	0.5	0.1	10	5	Ind	TO-99	5.50	3.50	1-71
	3501B, (Q)	2	10	±7	93	0.5	0.1	10	5	Ind	TO-99	11.85	7.75	1-71
	3501C, (Q)	2	5	±3	93	0.5	0.1	10	5	Ind	TO-99	15.45	10.85	1-71
	3501R	5	20	±15	93	0.5	0.1	10	5	Mil	TO-99	17.00	11.35	1-71
	3501S	2	10	±7	93	0.5	0.1	10	5	Mil	TO-99	24.75	16.50	1-71
FET	OPA103AM	0.50	25	-0.002	106	1	1.3	10	5	Ind	TO-99	10.20	6.50	1-36
	OPA103BM	0.50	15	-0.001	106	1	1.3	10	5	Ind	TO-99	13.80	8.60	1-36
	OPA103CM	0.25	5	-0.001	106	1	1.3	10	5	Ind	TO-99	18.05	11.20	1-36
	OPA103DM	0.25	2	-0.001	106	1	1.3	10	5	Ind	TO-99	29.85	18.50	1-36
	3527AM	0.50	10	-0.005	100	1.0	0.6	10	10	Ind	TO-99	15.05	10.15	1-99
	3527BM	0.25	5	-0.002	100	1.0	0.6	10	10	Ind	TO-99	20.15	13.65	1-99
	3527CM	0.25	2	-0.005	100	1.0	0.6	10	10	Ind	TO-99	33.15	23.30	1-99
	3542J, (Q)	20	50	-0.025	88	1.0	0.5	10	10	Com	TO-99	9.75	6.50	1-109
	3542S, (Q)	20	50	-0.025	88	1.0	0.5	10	10	Mil	TO-99	15.80	12.65	1-109
Wide Temp Range	OPA11HT	5	5(3)	±25	94	12.0	7.0	10	15	-55°C to	TO-99	49.00	39.20	1-8
	OPA12HT	10	30(3)	+250	77	20, A = 10(4)	120	10	10	+200°C(5)	TO-99	59.00	47.20	1-12

NOTES: 1) "(Q)" indicates product also avaliable with screening for increased reliability. 2) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C. 3) Typical. 4) Gain-bandwidth product. 5) OPA12HT: -55°C to +175°C.

LOW NOISE

We now solve another designer's dilemma with this group of low noise FET op amps offering guaranteed noise spectral density, 100% tested. Until now the designer of low noise circuits had to rely on "typical" specifications for his FET amplifier designs. In applications for low noise signal conditioning, light measurements, radiation measurements, photodiode circuits, low noise data acquisition, etc., the fully characterized and tested voltage noise performance of the OPA101 or OPA102 allows the designer to truly bound noise errors.

LOW NOISE															
		Noise				Open	Frequency(2) Response								
		Voltage	Bias	Offset Voltage		Loop			Rated Output						
		nV/√Hz	Current	at 25°C	Temp Drift	Gain		Slew					Price ($)		
		at 10kHz	at 25°C	±mV	±μV/°C	dB	A-BW	Rate	±V	±mA	Temp				
Description	Model	max	max	max	max	min	MHz	V/μsec min	min	min	Range(1)	Package	Unit	100's	Page
†A_{CL} > 1V/V	OPA101AM	8	-15pA	±0.5	±10	94	20	5	12	12	Ind	TO-99	32.20	23.00	1-24
	OPA101BM	8	-10pA	±0.25	±5	94	20	5	12	12	Ind	TO-99	40.25	28.75	1-24
†A_{CL} > 3V/V	OPA102AM	8	-15pA	±0.5	±10	94	40	10	12	12	Ind	TO-99	32.20	23.00	1-24
	OPA102BM	8	-10pA	±0.25	±5	94	40	10	12	12	Ind	TO-99	40.25	28.75	1-24
Low Noise(2)	OPA27/37A	3, 8	±40nA	0.025	0.6	120	8, 40	2.8, 17	12	6	Mil	(3)	(4)		1-16
	OPA27/37E	3, 8	±40nA	0.025	0.6	120	8, 40	2.8, 17	12	6	Ind	(3)	(4)		1-16
	OPA27/37B	3, 8	±55nA	0.06	1.3	120	8, 40	2.8, 17	12	6	Mil	(3)	(4)		1-16
	OPA27/37F	3, 8	±55nA	0.06	1.3	120	8, 40	2.8, 17	12	6	Ind	(3)	(4)		1-16
	OPA27/37C	4, 5	±80nA	0.1	1.8	117	8, 40	2.8, 17	11, 5	5, 7	Mil	(3)	(4)		1-16
	OPA27/37G	4, 5	±80nA	0.1	1.8	117	8, 40	2.8, 17	11, 5	5, 7	Ind	(3)	(4)		1-16

† FET Input

NOTES: 1) Com = 0 to + 70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C. 2) OPA27 more heavily frequency compensated than OPA37. 3) Both OPA27 and OPA37 are available in TO-99 and 8-pin Hermetic DIP. 4) Advance information subject to change, contact Burr-Brown for price and availability.

LOW BIAS CURRENT

This group includes amplifiers with input bias currents from 0.01pA to 1nA. Applications with large feedback resistances or large source resistances (long time constants, integrators, current sources, etc.) and buffer applications will benefit by the use of low bias current amplifiers. Our many years of experience in designing, manufacturing, and testing FET amplifiers gives us unique abilities in providing low and ultra-low bias current op amps. Models OPA103 and OPA104 are noteworthy as they offer bias currents as low as 75fA (75×10^{-15} amps) and offset voltage drift as low as $2\mu V/°C$. With offset voltage laser-trimmed to as low as $250\mu V$, the need for expensive trim pot adjustment is eliminated.

0.01pA to 1nA bias current. — LOW BIAS CURRENT

Description	Model[1]	Offset Voltage at 25°C ±mV max	Offset Voltage Temp Drift ±µV/°C max	Bias Current pA (25°C) max	Open Loop Gain dB, min	Frequency Response Unity Gain MHz	Frequency Response Slew Rate V/µsec	Rated Output ±V min	Rated Output ±mA min	Temp Range[2]	Package	Price ($) Unit	Price ($) 100's	Page
Low Drift	OPA103AM	0.50	25	-2	106	1	1.3	10	5	Ind	TO-99	10.20	6.50	1-36
	OPA103BM	0.50	15	-1	106	1	1.3	10	5	Ind	TO-99	13.80	8.60	1-36
	OPA103CM	0.25	5	-1	106	1	1.3	10	5	Ind	TO-99	18.05	11.20	1-36
	OPA103DM	0.25	2	-1	106	1	1.3	10	5	Ind	TO-99	29.85	18.50	1-36
†Low Noise	OPA101AM	0.50	10	-15	94	10	6.5	12	12	Ind	TO-99	32.20	23.00	1-24
	OPA101BM	0.25	5	-10	94	10	6.5	12	12	Ind	TO-99	40.25	28.75	1-24
	OPA102AM	0.50	10	-15	94	40[3]	14	12	12	Ind	TO-99	32.20	23.00	1-24
	OPA102BM	0.25	5	-10	94	40[3]	14	12	12	Ind	TO-99	40.25	28.75	1-24
Ultra-Low Bias Current	OPA104AM	1.0	25	-0.300	106	1	2.2	10	5	Ind	TO-99	17.00	9.90	1-40
	OPA104BM	0.50	15	-0.150	106	1	2.2	10	5	Ind	TO-99	23.00	14.00	1-40
	OPA104CM	0.50	10	-0.075	106	1	2.2	10	5	Ind	TO-99	29.50	19.00	1-40
	3528AM, (Q)	0.50	15	-0.300	88	0.7	0.3	10	5	Ind	TO-99	18.60	12.10	1-103
	3528BM, (Q)	0.25	5	-0.150	92	0.7	0.3	10	5	Ind	TO-99	22.95	16.35	1-103
	3528CM, (Q)	0.50	10	-0.075	90	0.7	0.3	10	5	Ind	TO-99	29.35	21.25	1-103
	3523J, (Q)	1.0	50	-0.50	100	1	0.6	10	10	Com	TO-99	31.75	20.60	1-95
	3523K	0.50	25	-0.25	100	1	0.6	10	10	Com	TO-99	39.70	27.55	1-95
	3523L, (Q)	0.50	25	-0.10	100	1	0.6	10	10	Com	TO-99	47.60	31.80	1-95
Inverting Only	3430J	Adj. to 0	30	±0.01	100	2kHz	0.4V/msec	10	5	Com	Module	81.95	55.00	1-60
	3430K	Adj. to 0	10	±0.01	100	2kHz	0.4V/msec	10	5	Com	Module	104.00	[5]	1-60
Noninverting Only	3431J	Adj. to 0	30	±0.01	100	2kHz	0.4V/msec	10	5	Com	Module	81.95	55.00	1-60
	3431K	Adj. to 0	10	±0.01	100	2kHz	0.4V/msec	10	5	Com	Module	104.00	[5]	1-60
†Low Cost	3542J	20	50	-25	88	1	0.5	10	10	Com	TO-99	9.75	6.50	1-109
	3542S	20	50	-25	88	1	0.5	10	10	Mil	TO-99	15.80	12.65	1-109
Chopper-Stabilized	3291/14	0.02	0.1	±50	140	3	6	10	5	Ind	Module	109.00	77.50	1-52
	3292/14	0.05	0.3	±50	140	3	6	10	5	Ind	Module	80.60	56.10	1-52
	3293/14	0.10	1	±100	140	3	6	10	5	Ind	Module	70.35	46.00	1-52
	3271/25	0.05	1	±80	140	1	20	110	20	Ind	Module	244.00	172.50	1-50
†Wideband	OPA605H/A	1.0	25	-35	80	20	94	10	30	Com/Ind	DIP	49.00	34.50	1-44
	OPA605J/B	0.5	10	-35	80	20	94	10	30	Com/Ind	DIP	58.00	41.00	1-44
	OPA605K/C	0.5	5	-35	80	20	94	10	30	Com/Ind	DIP	73.00	51.00	1-44
	3554AM, (Q)	2	50	-50	100	1000[3]	1000	10	100	Ind	TO-3	73.20	47.70	1-125
	3554BM, (Q)	1	15	-50	100	1000[3]	1000	10	100	Ind	TO-3	83.80	56.15	1-125
	3554CM, (Q)	1	25	-50	100	1000[3]	1000	10	100	Mil	TO-3	97.60	66.30	1-125
†Buffer	3553AM, (Q)	50	300	-200	NA	300[4]	2000	10	200	Ind	TO-3	36.00	22.45	1-123
†High Current	3571AM, (Q)	2	40	-100	94	0.5	3	30	1A	Ind	TO-3	72.45	48.00	1-133
	3572AM	2	40	-100	94	0.5	3	30	2A	Ind	TO-3	83.00	54.50	1-133
†High Voltage	3580J	10	30	-50	86	5	15	30	60	Com	TO-3	62.00	41.00	1-143
	3581J	3	25	-20	94	5	20	70	30	Com	TO-3	93.45	61.00	1-143
	3582J, (Q)	3	25	-20	100	5	20	145	15	Com	TO-3	101.50	71.00	1-143
	3583AM, (Q)	3	25	-20	105	5	30	140	75	Ind	TO-3	111.20	79.00	1-147
	3583JM	3	25	-20	94	5	30	140	75	Com	TO-3	105.60	74.00	1-147
	3584JM, (Q)	3	25	-20	100	20[3]	150	145	15	Com	TO-3	107.00	79.00	1-147
General Purpose	3522J	1.0	50	-10	94	1	0.6	10	10	Com	TO-99	17.00	11.20	1-89
	3522K	0.50	10	-5	94	1	0.6	10	10	Com	TO-99	22.40	15.25	1-89
	3522L	0.50	25	-1	94	1	0.6	10	10	Com	TO-99	32.75	21.10	1-89
	3522S, (Q)	0.50	25	-5	94	1	0.6	10	10	Mil	TO-99	46.30	29.85	1-89
Ultra-Low Drift	3527AM, (Q)	0.50	10	-5	100	1	0.6	10	10	Ind	TO-99	15.05	10.15	1-99
	3527BM, (Q)	0.25	5	-2	100	1	0.6	10	10	Ind	TO-99	20.15	13.65	1-99
	3527CM, (Q)	0.25	2	-5	100	1	0.6	10	10	Ind	TO-99	33.15	23.30	1-99
	3521H	0.50	10	-20	94	1.5	0.6	10	10	Com	TO-99	22.80	14.90	1-89
	3521J, (Q)	0.25	5	-20	94	1.5	0.6	10	10	Com	TO-99	32.65	20.25	1-89
	3521K	0.25	2	-15	94	1.5	0.6	10	10	Com	TO-99	48.95	32.65	1-89
	3521L	0.25	1	-10	94	1.5	0.6	10	10	Com	TO-99	72.40	47.00	1-89
	3521R, (Q)	0.25	5	-20	94	1.5	0.6	10	10	Mil	TO-99	84.25	55.70	1-89

†FET Input *Varactor Input

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. 2) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C. 3) Gain-bandwidth product. 4) -3dB bandwidth. 5) Contact factory.

HIGH VOLTAGE - HIGH CURRENT

The high voltage amplifiers are designed to provide large output voltage swings (greater than ±10V, up to ±145V) and to operate on wide ranges of supply voltage. The high current amplifiers provide output currents greater than ±10mA to ±5A peak. All high voltage units have FET inputs to minimize bias current errors while many high current units have self-contained thermal sensing and shutdown to automatically protect the amplifiers from over heat-

Output voltages > ±10V to ±145V.		HIGH VOLTAGE												
		Rated Output		Offset Voltage at 25°C	Offset Voltage Temp Drift	Bias Current	Frequency Response		Open Loop					
		±V	±mA	±mV	±μV/°C	pA (25°C)	Unity-Gain	Slew Rate	Gain	Temp		Price ($)		
Description	Model(1)	min	min	max	max	max	MHz	V/μsec	dB	Range(2)	Package	Unit	100's	Page
FET	3584JM, (Q)	145	15	3	25	-20	20(3)	150	120	Com	TO-3	94.50	65.50	1-151
	3583AM, (Q)	140	75	3	25	-20	5	30	118	Ind	TO-3	100.00	70.00	1-147
	3583JM	140	75	3	25	-20	5	30	118	Com	TO-3	95.00	65.00	1-147
	3582J	145	15	3	25	-20	5	20	118	Com	TO-3	101.50	71.00	1-143
	3581J	70	30	3	25	-20	5	20	112	Com	TO-3	93.45	61.00	1-143
	3580J	30	60	10	30	-50	5	15	106	Com	TO-3	62.00	41.00	1-143
	3571AM, (Q)	30	1A(4)	2	40	-100	0.5	3	94	Ind	TO-3	72.45	48.00	1-133
	3572AM	30	2A(5)	2	40	-100	0.5	3	94	Ind	TO-3	83.00	54.50	1-133
	3573AM	20	2A(5)	10	65	40nA	1	2.6	94	Ind	TO-3	36.00	25.00	1-139
Chopper-Stabilized	3271/25	110	20	0.05	1	±80	1	20	140	Ind	Module	244.00	172.50	1-50

Output currents > ±15mA to ±2A		HIGH CURRENT												
High Power	3573AM	20	2A(5)	10	65	40nA	1	2.6	94	Ind	TO-3	36.00	25.00	1-139
	3572AM	30	2A(5)	2	40	-100	0.5	3	94	Ind	TO-3	83.00	54.50	1-133
	3571AM, (Q)	30	1A(4)	2	40	-100	0.5	3	94	Ind	TO-3	72.45	48.00	1-133
Wideband	3554AM, (Q)	10	100	2	50	-50	1700(3)	1200	100	Ind	TO-3	73.20	47.70	1-125
	3554BM, (Q)	10	100	1	15	-50	1700(3)	1200	100	Ind	TO-3	83.80	56.15	1-125
	3554SM, (Q)	10	100	1	25	-50	1700(3)	1200	100	Mil	TO-3	97.60	66.30	1-125
High Voltage	3584JM, (Q)	145	15	3	25	-20	20(3)	150	126	Com	TO-3	94.50	65.50	1-151
	3583AM	140	75	3	25	-20	5	30	118	Ind	TO-3	100.00	70.00	1-147
	3583JM	140	75	3	25	-20	5	30	118	Com	TO-3	95.00	65.00	1-147
	3582J	145	15	3	25	-20	5	20	118	Com	TO-3	101.50	71.00	1-143
	3581J	70	30	3	25	-20	5	20	112	Com	TO-3	93.45	61.00	1-143
	3580J	30	60	10	30	-50	5	15	106	Com	TO-3	62.00	41.00	1-143
Booster (Buffer)	3553AM, (Q)	10	200	50	300(6)	-200	300	2000	NA	Ind	TO-3	36.00	22.45	
	3329/03	10	100	50	--	Bipolar	5	--	NA	Ind	DIP	36.75	22.95	

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. 2) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C. 3) Gain-bandwidth product. 4) 2A peak. 5) 5A peak. 6) Typical.

WIDE BANDWIDTH

Wideband operational amplifiers have gain bandwidths (A BW) greater than 10MHz. This group also contains fast settling and high slew rate amplifiers. For pulse, video, fast settling and multiplexing applications, select from this group of amplifiers. Note Models 3554 and OPA605 which provide an excellent combination of wide bandwidth, settling time, and output current all at moderate cost.

		WIDE BANDWIDTH													
		Frequency Response		t_s		Rated Output		Offset Voltage		Open					
		A-BW	Slew Rate V/μsec	±0.1%	Com-	±V	±mA	at 25°C ±mV	Temp Drift ±μV/°C	Loop Gain	Temp		Price ($)		
Description	Model(1)	MHz	min	nsec	tion	min	min	max	max	dB	Range(2)	Package	Unit	100's	Page
Differential	3554AM, (Q)	1700, A = 1000	1000	120	ext.	10	100	2	50	100	Ind	TO-3	73.20	47.70	1-125
	3554BM, (Q)	1700, A = 1000	1000	120	ext.	10	100	1	15	100	Ind	TO-3	83.80	56.15	1-125
	3554SM, (Q)	1700, A = 1000	1000	120	ext.	10	100	1	25	100	Mil	TO-3	97.60	66.30	1-125
	3551J	50, A = 10	250(3)	400	ext.	10	10	1	50	100	Com	TO-99	31.80	21.45	1-117
	3551S, (Q)	50, A = 10	250(3)	400	ext.	10	10	1	50	100	Mil	TO-99	56.15	35.70	1-117
	3550J	10, A = 1	65	400	int.	10	10	1	50	100	Com	TO-99	31.20	21.45	1-113
	3550K	20, A = 1	100	400	int.	10	10	1	50	100	Com	TO-99	39.75	25.50	1-113
	3550S, (Q)	10, A = 1	65	400	int.	10	10	1	50	100	Mil	TO-99	57.80	35.70	1-113
	3508J	100, A = 100	20	--	ext.	10	10	5	30(3)	103	Com	TO-99	10.25	7.50	1-79
	3507J, (Q)	20, A = 10	80	200	ext.	10	10	10	30(3)	83	Com	TO-99	12.50	8.90	1-75
	OPA605H/A	200, A = 1000	300(3)	300	ext.	10	30	1	25	96	Com/Ind	DIP	49.00	34.50	1-44
	OPA605J/B	200, A = 1000	300(3)	300	ext.	10	30	0.5	10	96	Com/Ind	DIP	58.00	41.00	1-44
	OPA605K/C	200, A = 1000	300(3)	300	ext.	10	30	0.5	5	96	Com/Ind	DIP	73.00	51.00	1-44
Low Noise	OPA101AM	20, A = 100	5	2.5	int.	12	12	0.5	10	105	Ind	TO-99	32.20	23.00	1-24
	OPA101BM	20, A = 100	5	2.5	int.	12	12	0.25	5	105	Ind	TO-99	40.25	28.75	1-24
	OPA102AM	40, A = 100	10	1.5	int.	12	12	0.5	10	105	Ind	TO-99	32.20	23.00	1-24
	OPA102BM	40, A = 100	10	1.5	int.	12	12	0.25	5	105	Ind	TO-99	40.25	28.75	1-24
Military	OPA600/MIL Series	See Military Products													
Unity-Gain Buffer	3553AM, (Q)	32(4)	2000	--	--	10	200	50	300(3)	NA	Ind	TO-3	36.00	22.45	1-121
Wide Temp Range	OPA12HT	20, A = 10	80	200	ext.	10	10	10	30(3)	83	-55°C to	TO-99	59.00	47.20	1-12
	OPA11HT	12, A = 1	4	1500	int.	10	15	5	5(3)	98	+200°C(5)	TO-99	49.00	39.20	1-8

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. 2) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C. 3) Typical. 4) Full power bandwidth. 5) OPA12HT: -55°C to +175°C.

LOW DRIFT

For applications where accuracy must be preserved over a substantial temperature range, select operational amplifiers from this group of low drift operational amplifier. Sophisticated drift compensation techniques help provide low offset voltage drift versus temperature, in both the FET and the Bipolar input type operational amplifiers. Input offset drifts from 0.1μV/°C to 10μV/°C are available within this group. Models 3510 and OPA103 are particularly recommended because of their excellent specifications and low cost.

0.1μV/°C to 10μV/°C input offset voltage change with temperature.

LOW DRIFT

Description	Model(1)	Offset Voltage at 25°C ±mV max	Offset Voltage Temp Drift ±μV/°C max	Bias Current nA (25°C) max	Open Loop Gain dB, min	Frequency Response Unity Gain MHz	Frequency Response Slew Rate Vμsec	Rated Output ±V min	Rated Output ±mA min	Temp Range(2)	Package	Price ($) Unit	Price ($) 100's	Page
*Inverting Only	3291/14	0.02	0.10	±0.05	140	3	6	10	5	Ind	Module	109.00	77.50	1-52
	3292/14	0.05	0.30	±0.05	140	3	6	10	5	Ind	Module	80.60	56.10	1-52
	3293/14	0.10	1.0	±0.10	140	3	6	10	5	Ind	Module	70.35	46.00	1-52
FET	OPA103AM	0.50	25	-0.002	106	1	1.3	10	5	Ind	TO-99	10.20	6.50	1-36
	OPA103BM	0.50	15	-0.001	106	1	1.3	10	5	Ind	TO-99	13.80	8.60	1-36
	OPA103CM	0.25	5	-0.001	106	1	1.3	10	5	Ind	TO-99	18.05	11.20	1-36
	OPA103DM	0.25	2	-0.001	106	1	1.3	10	5	Ind	TO-99	29.85	18.50	1-36
	3521H	0.50	10	-0.02	94	1.5	0.6	10	10	Com	TO-99	22.80	14.95	1-89
	3521J	0.25	5	-0.02	94	1.5	0.6	10	10	Com	TO-99	32.65	20.25	1-89
	3521K	0.25	2	-0.015	94	1.5	0.6	10	10	Com	TO-99	48.95	32.65	1-89
	3521L	0.25	1	-0.01	94	1.5	0.6	10	10	Com	TO-99	72.40	47.00	1-89
	3521R	0.25	5	-0.02	94	1.5	0.6	10	10	Mil	TO-99	84.25	55.70	1-89
	3527AM, (Q)	0.50	10	-0.005	100	1	0.6	10	10	Ind	TO-99	15.05	10.15	1-99
	3527BM, (Q)	0.25	5	-0.002	100	1	0.6	10	10	Ind	TO-99	20.15	13.65	1-99
	3527CM, (Q)	0.25	2	-0.005	100	1	0.6	10	10	Ind	TO-99	33.15	23.30	1-99
	3528AM	0.50	15	-0.30pA	88	0.7	0.3	10	5	Ind	TO-99	18.60	12.10	1-103
	3528BM	0.25	5	-0.15pA	92	0.7	0.3	10	5	Ind	TO-99	22.95	16.35	1-103
	3528CM	0.50	10	-0.075pA	90	0.7	0.3	10	5	Ind	TO-99	29.35	21.25	1-103
Bipolar	3510AM	0.15	2	±35	120	0.4	0.5	10	10	Ind	TO-99	8.90	5.70	1-83
	3510BM	0.12	1	±25	120	0.4	0.5	10	10	Ind	TO-99	11.25	7.10	1-83
	3510CM	0.06	0.5	±15	120	0.4	0.5	10	10	Ind	TO-99	18.25	11.60	1-83
Military	3510VM/MIL, /883B	See Military Products												
Bipolar	3500B	2	5	±20	93	1.5	0.8	10	10	Ind	TO-99	17.25	10.65	1-62
	3500C	1	3	±15	93	1.5	1.0	10	10	Ind	TO-99	22.00	13.90	1-62
	3500R, (Q)	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99	20.50	12.20	1-62
	3500S, (Q)	2	10	±20	93	1.5	0.8	10	10	Mil	TO-99	33.00	21.20	1-62
	3500T, (Q)	1	3	±15	93	1.5	1.0	10	10	Mil	TO-99	53.25	33.60	1-62
	3500E	0.50	1	±50	100(4)	1.5	0.8	10	10	Ind	TO-99	36.25	22.25	1-62
	3500MP	0.20(3)	1(3)	±50	100(4)	1.5	0.8	10	10	Ind	TO-99	36.25	22.25	1-66
	3501A, (Q)	5	20	±15	93	0.5	0.1	10	5	Ind	TO-99	5.50	3.50	1-71
	3501B, (Q)	2	10	±7	93	0.5	0.1	10	5	Ind	TO-99	11.85	7.75	1-71
	3501C, (Q)	2	5	±3	93	0.5	0.1	10	5	Ind	TO-99	15.45	10.85	1-71
	3501R	5	20	±15	93	0.5	0.1	10	5	Mil	TO-99	17.00	11.35	1-71
	3501S	2	10	±7	93	0.5	0.1	10	5	Mil	TO-99	24.75	16.50	1-71
High Voltage	3271/25	0.05	1.0	±0.08	140	1	20	110	20	Ind	Module	244.00	172.00	1-50

*Chopper-stabilized

NOTES: 1) "(Q)" indicates product also avaliable with screening for increased reliability. 2) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C. 3) These specifications apply to the match between two devices. The 3500MP is a matched pair of amplifiers. 4) Typical.

UNITY-GAIN BUFFER (Power Booster)

These versatile amplifiers: boost the output current capability of another amplifier; buffer an impedance that might load a critical circuit; may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±100mA are available with speeds of 2000V/μsec.

UNITY-GAIN BUFFER

Description	Model	Rated Output ±V min	Rated Output ±mA min	Frequency Response -3dB MHz	Frequency Response Full Pwr BW MHz	Frequency Response Slew Rate V/μsec	Gain V/V	Input Impedance Ω	Open Loop Gain dB	Temp Range(1)	Package	Price ($) Unit	Price ($) 100's	Page
Noninverting	3553AM	10	200	300	32	2000	≈ 1	10^{11}	NA	Ind	TO-3	36.00	22.45	1-121
	3329/03	10	100	5	1	--	≈ 1	10k	NA	Ind	DIP	36.75	22.95	1-58

NOTES: 1) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C.

GLOSSARY OF TERMS AND DEFINITIONS
Operational Amplifiers

COMMON-MODE INPUT IMPEDANCE
The effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground terminal.

COMMON-MODE REJECTION (CMR)
When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$CMR \text{ (in dB)} = 20 \log_{10} CMV/\text{Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE VOLTAGE (CMV)
That portion of an input signal which is common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$CMV = (e_1 + e_2)/2$$

COMMON-MODE VOLTAGE GAIN
The ratio of the output signal voltage (ideally zero) to the common-mode input signal voltage.

COMMON-MODE VOLTAGE RANGE
The range of input voltage for linear, nonsaturated operation.

DIFFERENTIAL INPUT IMPEDANCE
The apparent impedance, resistance in parallel with capacitance, between the two input terminals.

FULL POWER FREQUENCY RESPONSE
The maximum frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN-BANDWIDTH PRODUCT
A product of small signal, open-loop gain and frequency at that gain.

INPUT BIAS CURRENT
The DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT VS SUPPLY VOLTAGE
The sensitivity of input bias current to the power supply voltages.

INPUT BIAS CURRENT VS TEMPERATURE
The sensitivity of input bias current to temperature.

INPUT CURRENT NOISE
The input current which would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are large.

INPUT OFFSET CURRENT
The difference of the two input bias currents of a differential amplifier.

INPUT OFFSET VOLTAGE
The DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT OFFSET VOLTAGE VS SUPPLY VOLTAGE I/PSRR
The sensitivity of input offset voltage to the power supply voltages. Both power supply magnitudes are changed in the same direction and over the operating voltage range.

INPUT OFFSET VOLTAGE VS TEMPERATURE (DRIFT)
The rate of change of input offset voltage with temperature. At Burr-Brown, this is the change in input offset voltage from 25°C to the maximum specification temperature, plus the change in input offset voltage from 25°C to the minimum specification temperature, this quantity divided by the specification temperature range.

INPUT OFFSET VOLTAGE VS TIME
The sensitivity of input offset voltage to time.

INPUT VOLTAGE NOISE
The differential input voltage which would produce, at the output of a noiseless amplifier, the same output as that produced by the inherent noise generated internally in the amplifier when the source resistances are small.

MAXIMUM SAFE INPUT VOLTAGE
The maximum, peak value, continuous voltage that may be applied at, or between, the inputs without damage.

OPEN-LOOP GAIN
The ratio of the output signal voltage to the differential input signal voltage.

OPERATING TEMPERATURE RANGE
The temperature range, ambient unless otherwise indicated, over which the amplifier may be safely operated.

OUTPUT RESISTANCE
The open-loop output source resistance with respect to ground.

POWER SUPPLY RATED VOLTAGE
The normal value of power supply voltage at which the amplifier is designed to operate.

POWER SUPPLY VOLTAGE RANGE
The range of power supply voltage over which the amplifier may be safely operated.

QUIESCENT CURRENT
The current required from the power supply to operate the amplfiier with no load and with the output at zero.

RATED OUTPUT
The peak output voltage and current which can be continuously, simultaneously supplied.

SETTLING TIME
The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

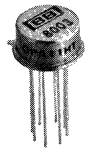
SLEW RATE
The maximum rate of charge of the output voltage when supplying rated output.

SPECIFICATION TEMPERATURE RANGE
The temperature range over which the "versus temperature" specifications are specified.

STORAGE TEMPERATURE RANGE
The temperature range over which the amplifier may be safely stored, unpowered.

UNITY-GAIN FREQUENCY RESPONSE
The frequency at which the open-loop becomes unity.

BURR-BROWN®



OPA11HT

Wide Temperature-Range General Purpose OPERATIONAL AMPLIFIER

FEATURES

- -55°C TO +200°C SPECIFICATIONS
- 30nA MAX, INPUT BIAS CURRENT AT +200°C
- ±6mV, MAX, INPUT OFFSET VOLTAGE AT +200°C
- ±5μV/°C TYP, INPUT OFFSET VOLTAGE COEFFICIENT
- 12MHz BANDWIDTH, TYPICAL
- HERMETIC PACKAGE WITH STANDARD PINOUT (741-TYPE)

DESCRIPTION

These specifications give you a versatile operational amplifier that will work in circuits that are subjected to extremely wide temperature ranges. Typical applications for OPA11HT include general purpose gain blocks, high-speed pulse amplifiers, audio amplifiers, high-frequency active filters, high-speed integrators, and photodiode amplifiers.

You're assured of this product's performance over the -55°C to +200°C range because we conduct 100% screening procedures in accordance with MIL-STD-883, method 5004, class B. Burn-in is performed at 200°C. Our sample and inspection procedures include both destructive and nondestructive bonding wire pull tests in accordance with Method 2011 of MIL-STD-883. The product is assembled in a clean-room environment.

Model OPA11HT is internally compensated for stability at all gains. Pins are available for special tailoring of the bandwidth compensation. Significant advantages in high gain, wide bandwidth, low-bias current, high output current and high common-mode rejection are provided by OPA11HT. Inputs are protected against common-mode voltages up to the value of the power supplies while the output is current limited to offer short circuited protection. TO-99 hermetic package has standard 741-type pinout arrangement.

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PDS-476

SPECIFICATIONS

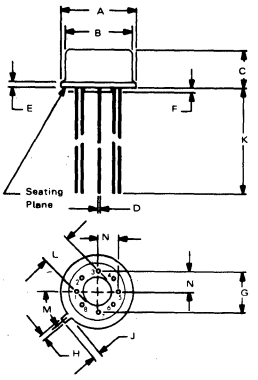
ELECTRICAL

Specifications at ±15VDC and T_A = +200°C unless otherwise noted.

MODEL		OPA11HT			
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
OPEN LOOP GAIN, DC, single-ended	A_V				
No load			103		dB
R_L= 2kΩ		94	100		dB
RATED OUTPUT					
Voltage, R_L= 2kΩ	V_{om}	±10	±12		V
Current (T_A = 25°C)	I_{om}	±15	±23		mA
DYNAMIC RESPONSE (T_A = 25°C)					
Small-Signal Bandwidth (0dB)			12		MHz
Full-Power Bandwidth, V_{OUT} = ±10V	BW_{fp}	50	75		kHz
Slew Rate, R_L = 2kΩ	SR	4	7		V/μsec
Settling Time (0.1%)			1.5		μsec
Rise Time (10% to 90%, small-signal)			30		nsec
INPUT OFFSET VOLTAGE	V_{io}				
Initial (without adj. at 25°C)			±1	±5	mV
Over Temperature					
T_A = +200°C				±6	mV
T_A = -55°C				±7	mV
Average V_{io} coefficient			±5		μV/°C
Average V_{io} coefficient vs supply voltage (T_A = 25°C)			±10	±200	μV/V
INPUT BIAS CURRENT	I_{ib}				
Initial at +25°C			±10	±25	nA
Over Temperature					
T_A = +200°C				±30	nA
T_A = -55°C				±40	nA
Average I_{ib} coefficient			±0.1		nA/°C
INPUT DIFFERENCE CURRENT	I_{io}				
Initial at +25°C			±10	±25	nA
Over Temperature					
T_A = +200°C				±30	nA
T_A = -55°C				±40	nA
Average I_{io} coefficient			±0.1		nA/°C
INPUT IMPEDANCE (T_A = 25°C)					
Differential	r_i	100	300		MΩ
	c_i		3		pF
Common Mode	$r_{i(CM)}$		1000		MΩ
	$c_{i(CM)}$		3		pF
INPUT VOLTAGE RANGE					
Common Mode				±11	V
Differential Mode				±12	V
Common-Mode Rejection	CMR	80	100		dB
Over Temperature (-55°C ≤ T_A ≤ +200°C)			100		dB
POWER SUPPLY (T_A = 25°C)					
Rated Voltage	V_{CC}			±15	V
Voltage Range, derated			±8 to ±22		V
Current, quiescent	I_q		±3	±3.7	mA
Over Temperature (-55°C ≤ T_A ≤ +200°C)			±3		mA
Power Supply Rejection Ratio (T_A = 200°C)	PS_{rr}	80	100		dB
TEMPERATURE RANGE					
Specification	-55°C ≤ T_A ≤ +200°C				
Operating	-55°C ≤ T_A ≤ +200°C				
Storage	-65°C ≤ T_A ≤ +250°C				

MECHANICAL

TO-99 PACKAGE

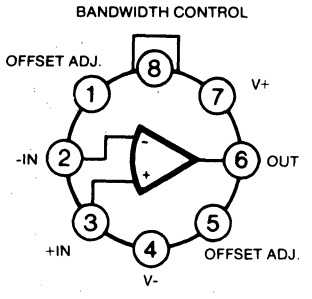


NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM



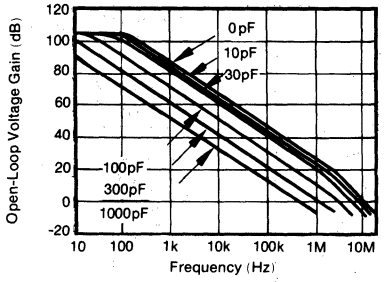
TOP VIEW

PIN 4 IS CONNECTED TO CASE.

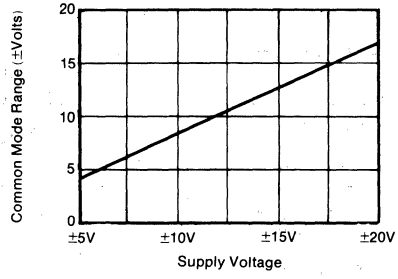
TYPICAL PERFORMANCE CURVES

(at ±15VDC and T_A = +25°C unless otherwise specified)

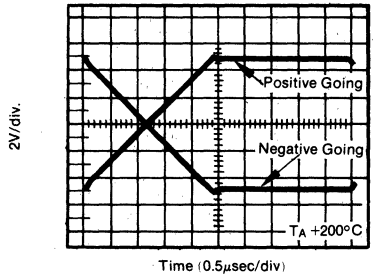
OPEN LOOP FREQUENCY RESPONSE[1]



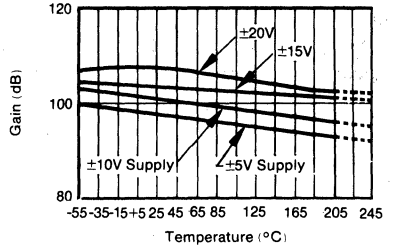
COMMON MODE VOLTAGE RANGE vs. SUPPLY VOLTAGE



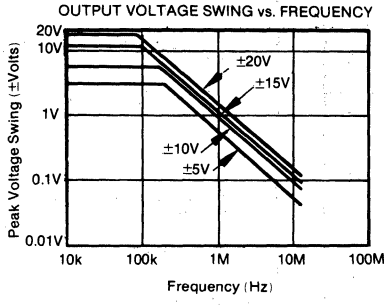
STEP RESPONSE IN FOLLOWER CONFIGURATION[2]



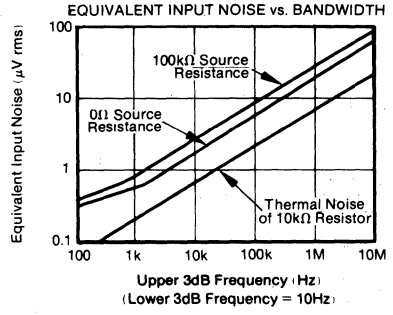
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



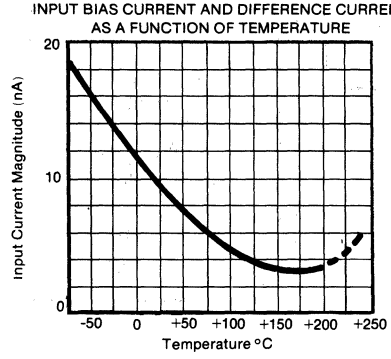
OUTPUT VOLTAGE SWING vs. FREQUENCY



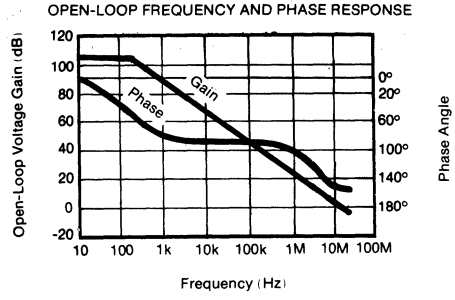
EQUIVALENT INPUT NOISE vs. BANDWIDTH



INPUT BIAS CURRENT AND DIFFERENCE CURRENT AS A FUNCTION OF TEMPERATURE



OPEN-LOOP FREQUENCY AND PHASE RESPONSE



1. Capacitance values shown are compensation from pin 8 to common. Not required for stability. See Figure 1. 2. See Figure 3.

APPLICATIONS

BANDWIDTH COMPENSATION

The frequency response of the OPA11HT can be adjusted by use of an external compensation capacitor from pin 8 to common as shown in Figure 1. The open-loop frequency response curves illustrate the effect of various values of capacitance. The OPA11HT is stable at any gain level without the use of compensation, provided that stray wiring capacitance and/or load capacitance are not excessive, and that moderate values of feedback resistance are used ($R_{FB} \leq 10k\Omega$). A load capacitance of $\approx$50pF is desirable in all feedback configurations.

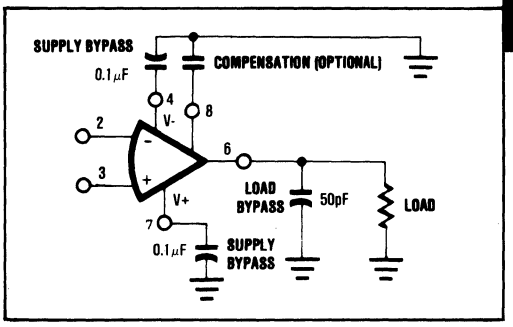


FIGURE 1. Compensated Amplifier with Supply Load Bypassing.

STABILITY

Because the OPA11HT is an extremely-fast amplifier with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly by passing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50pF capacitor, see Figure 1.

OFFSET VOLTAGE AND ADJUSTMENT

Although the offset voltage of these amplifiers is only a few millivolts, it may in some cases be desirable to null this offset. This is done by use of a 100kΩ potentiometer as shown in Figure 2.

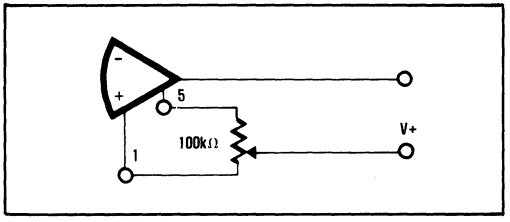


FIGURE 2. External Adjustment of Offset Voltage.

TEST CIRCUIT - DYNAMIC RESPONSE

The test circuit of Figure 3 is used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured for a small output signal (V_{OUT} = ±100mV). Slew rate and settling time are measured for a 10V, p-p, square wave.

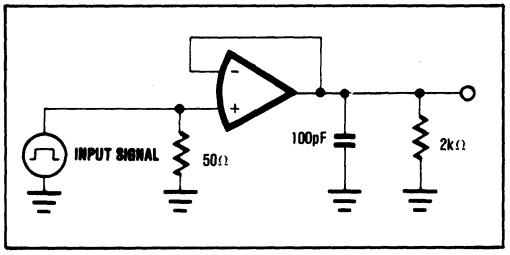


FIGURE 3. Dynamic Response Test Circuit.

VOLTAGE REGULATOR AT 200°C

In many applications, a regulated source of ±15V is needed. A voltage regulator that typically will operate up to +200°C is shown in Figure 4. This regulator accepts +16V to +30V at its input and provides +15V at 20mA at its output. A complementary version may be constructed to provide -15V by using the OPA11HT with a 2N1711 transistor. Short-circuit protection should be added if required.

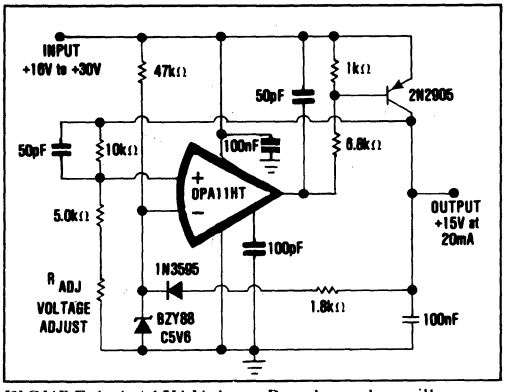


FIGURE 4. A +15V Voltage Regulator that will Operate at +200°C.

BURR-BROWN®

OPA12HT

Wide Temperature Range Fast-Slewing OPERATIONAL AMPLIFIER

FEATURES

- -55°C to +175°C SPECIFICATIONS
- 80V/μsec MIN SLEW RATE (120V/μsec, typ)
- 200nsec SETTLING TIME, typ
- HERMETIC PACKAGE WITH STANDARD PINOUT (741-type)

DESCRIPTION

If you need a fast transient-response circuit over wide -55°C to +175°C temperature range, you'll find the OPA12HT has the solution. Very-high speed pulse amplifiers, comparators, fast followers, and digital-to-analog converters are typical applications.

Performance over the temperature is assured because OPA12HT is subjected to 100% screening procedures in accordance with MIL-STD-883; method 5004, class B. Burn-in is performed at +175°C minimum. Sample and inspection procedures include both destructive and nondestructive wire bond pull tests in accordance with method 2011 of MIL-STD-883. The product is assembled in a clean-room environment.

OPA12HT is internally compensated to provide fast slewing and wide bandwidth for gains of 3 or more. At gains greater than 3, the gain rolloff is 6dB/ octave. Inputs are protected against common-mode voltages up to the value of the power supplies and the output can tolerate momentary short circuits to common. The TO-99 hermetic package offers standard 741-type pinout.

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PDS-477

SPECIFICATIONS

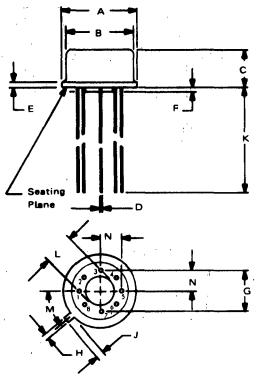
ELECTRICAL

Specifications at ±15VDC and +25°C unless otherwise noted.

MODEL		OPA12HT			
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
OPEN LOOP GAIN, DC, single-ended	A_{VS}				
No load			90		dB
$R_L = 2k\Omega$		77	83		dB
RATED OUTPUT					
Voltage, $R_L = 1k\Omega$	V_{om}	±10	±12		V
Current	I_{om}	±10	±20		mA
DYNAMIC RESPONSE					
Gain-Bandwidth Product ($A_{CL} = 10$)			20		MHz
Full-Power Bandwidth ($V_{OUT} = \pm 10V$, $R_L = 2k\Omega$, $A_{CL} = 3$)	BW_{fp}	1.2	1.6		MHz
Slew Rate ($R_L = 2k\Omega$, $A_{CL} = 3$)	SR	80	120		V/μsec
Settling Time (0.1%)			200		nsec
Rise Time (10% to 90%, small-signal)			25		nsec
INPUT OFFSET VOLTAGE	V_{io}				
Initial (without adj.) at 25°C			±5	±10	mV
Over Temperature (-55°C ≤ T_A ≤ +175°C)				±14	mV
Average V_{io} coefficient			±30		μV/°C
Average V_{io} coefficient vs supply voltage			±30	±200	μV/V
INPUT BIAS CURRENT	I_{ib}				
Initial at 25°C			+50	+250	nA
Over Temperature (-55°C ≤ T_A ≤ +175°C)				±1	μA
Average I_{ib} Coefficient			±2		nA/°C
INPUT DIFFERENCE CURRENT	I_{io}				
Initial at +25°C			±20	±50	nA
Over Temperature (-55°C ≤ T_A ≤ +175°C)				±300	nA
Average I_{io} Coefficient			1		nA/°C
INPUT IMPEDANCE					
Differential	r_i		100		MΩ
	c_i		3		pF
Common Mode	$r_{i(CM)}$		1000		MΩ
	$c_{i(CM)}$		5		pF
INPUT VOLTAGE RANGE					
Common Mode			±12	±10	V
Differential Mode				±15	V
Absolute Max (inputs common)				±Supply	V
Common Mode Rejection	CMR	74	90		dB
POWER SUPPLY					
Rated Voltage	V_{cc}			±15	V
Voltage Range, derated			±8 to ±20		V
Current, quiescent at 25°C	I_q		±4	±6	mA
Over Temperature (-55°C ≤ T_A ≤ + 175°C)			±5		mA
TEMPERATURE RANGE					
Specification		-55°C ≤ T_A ≤ +175°C			
Operating		-55°C ≤ T_A ≤ +175°C			
Storage		-65°C ≤ T_A ≤ +200°C			

MECHANICAL

TO-99 PACKAGE

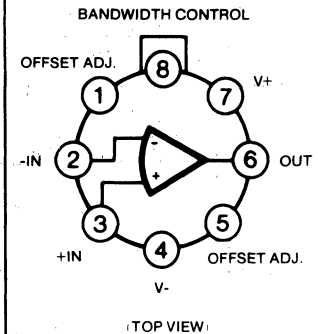


NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.7	---
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM



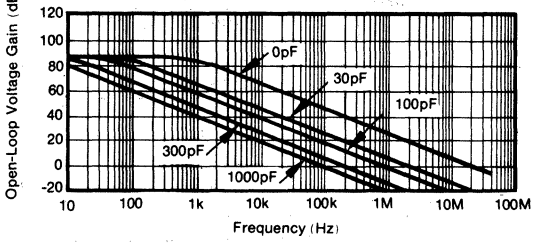
(TOP VIEW)

CASE IS ISOLATED FROM ALL PINS.

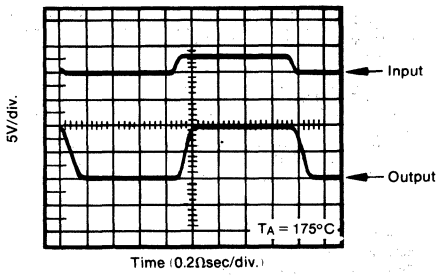
TYPICAL PERFORMANCE CURVES

(at ±15VDC and T_A = +25°C unless otherwise specified)

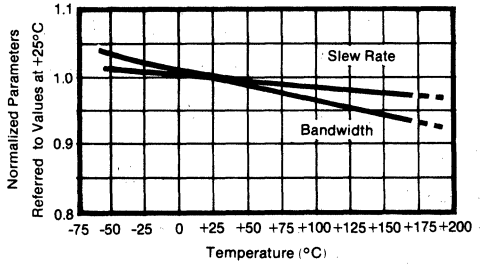
OPEN-LOOP FREQUENCY RESPONSE[1]



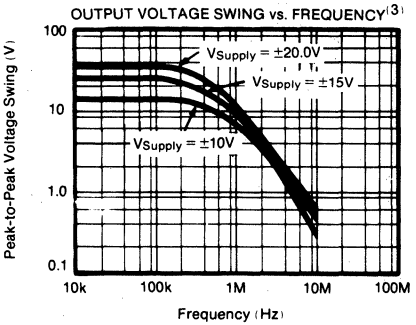
STEP RESPONSE[2]



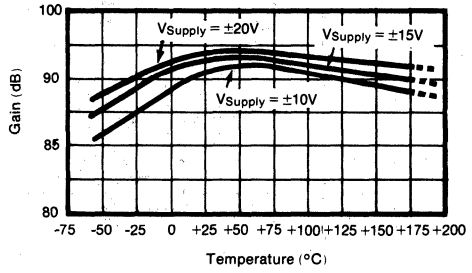
NORMALIZED AC PARAMETERS vs. TEMPERATURE



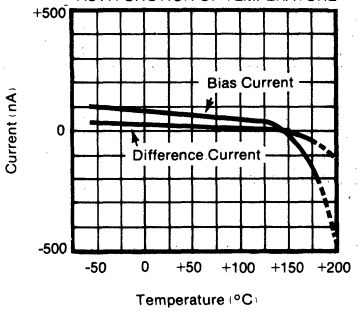
OUTPUT VOLTAGE SWING vs. FREQUENCY[3]



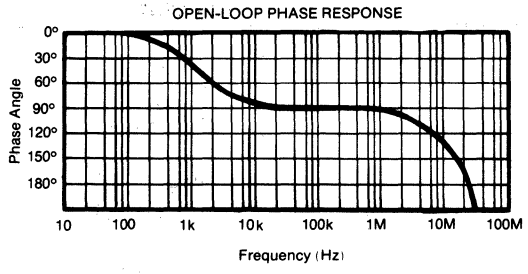
OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



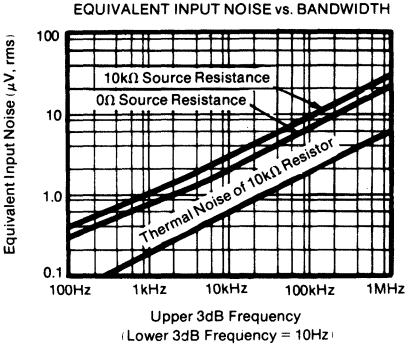
INPUT BIAS AND DIFFERENCE CURRENTS AS A FUNCTION OF TEMPERATURE



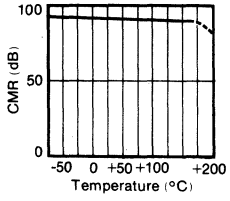
OPEN-LOOP PHASE RESPONSE



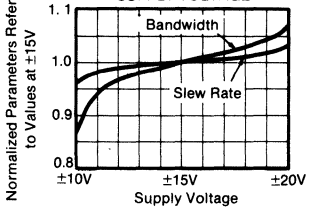
EQUIVALENT INPUT NOISE vs. BANDWIDTH



COMMON-MODE REJECTION RATIO vs. TEMPERATURE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



1. Capacitance values shown are external compensation from pin 8 to COMMON. See Figure 1.
2. Closed-Loop Gain = 3. See Figure 4.
3. With no external compensation capacitance.

APPLICATIONS

BANDWIDTH COMPENSATION

The frequency response of the OPA12HT can be adjusted by use of an external compensation capacitor from pin 8 to common, as shown in Figure 1. The open loop

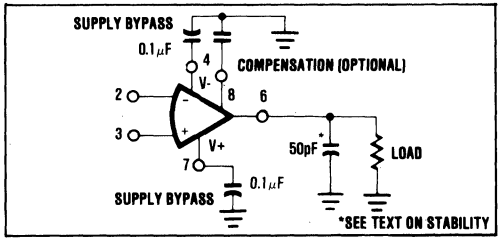


FIGURE 1. Compensated Amplifier with Supply and Load Bypassing.

frequency response curves of illustrate the effect of various values of capacitance. A load capacitance of ≈50pF is desirable in all feedback configurations. The OPA12HT is stable for gains of 3 or greater without external compensation (subject to limits on stray and load capacitance and resistance levels). A 20pF compensation capacitor will stabilize the OPA12HT for all values of gain, at the sacrifice of bandwidth and slew rate.

The circuit of Figure 2 illustrates another approach to compensation of the OPA12HT. This method yields unity gain stability without sacrificing slew rate.

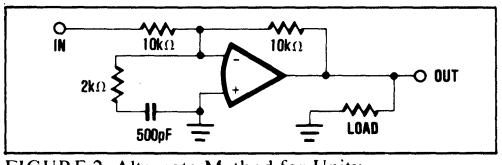


FIGURE 2. Alternate Method for Unity - Gain Compensation.

STABILITY

Because the OPA12HT is an extremely fast amplifier with high gain, stray wiring capacitance, and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly bypassing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50pF capacitor. (see Figure 1).

OFFSET VOLTAGE ADJUSTMENT

Although the offset voltage of these amplifiers is only a few millivolts, it may be desirable in some cases to null this offset. This is done by use of a 20kΩ potentiometer as shown in Figure 3.

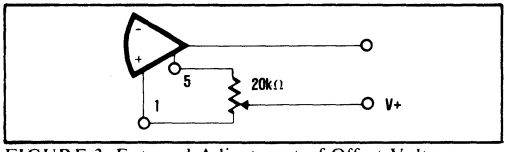


FIGURE 3. External Adjustment of Offset Voltage.

TEST CIRCUIT - DYNAMIC RESPONSE

The test circuits of Figure 4 is used for measurement of slew rate, settling time, and overshoot. Both rise time and overshoot are measured under small signal conditions (V_{OUT} = ±200mV). Slew rate and settling time are measured for a 10V, p-p, square wave.

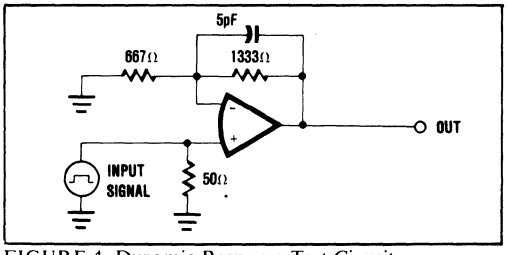
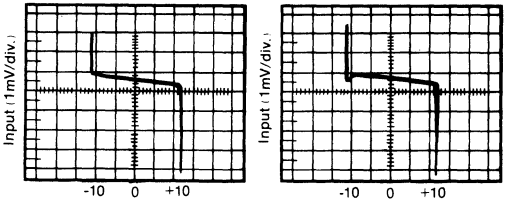


FIGURE 4. Dynamic Response Test Circuit.

HIGH TEMPERATURE LARGE-OUTPUT OPERATION

Figure 5 shows a typical transfer-function plot at +175°C for operation at no load and with a 2kΩload resistance. Distortion is just beginning to appear with the 2kΩload at -10V. This may be avoided by operating with a smaller negative output swing, by increasing the value of load resistance, or by reducing the temperature.

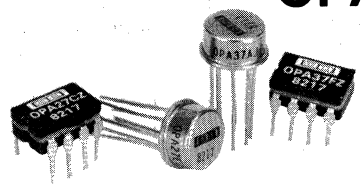


(a) T_A = +175°C, No load (b) T_A = +175°C, R_L = 2kΩ

FIGURE 5. Typical Open-Loop Transfer Function at +175°C.

BURR-BROWN®

OPA27/OPA37



Ultra-Low Noise Precision OPERATIONAL AMPLIFIERS

FEATURES

- EXTREMELY LOW NOISE
  - 3nV/$\sqrt{Hz}$ at 1kHz
  - 80nV, p-p from 0.1Hz to 10Hz
- LOW OFFSET VOLTAGE
  - 10μV
  - 0.2μV/°C
- HIGH SPEED
  - OPA27, 2.8V/μsec
  - OPA37, 17V/μsec
- EXCELLENT CMRR
  - 126dB over ±11V Input
- HIGH GAIN
  - 1800V/mV (125dB)
- FITS OP-07, OP-05, 725, AD510, AD517 SOCKETS

APPLICATIONS

- TRANSDUCER AMPLIFIER
- LOW NOISE INSTRUMENTATION AMPLIFIER
- DATA ACQUISITION PREAMPLIFIER
- PHONO AND TAPE PREAMPLIFIER
- FAST D/A CONVERTER OUTPUT
- WIDE BANDWIDTH INSTRUMENTATION AMPLIFIERS
- PRECISION COMPARATOR

DESCRIPTION

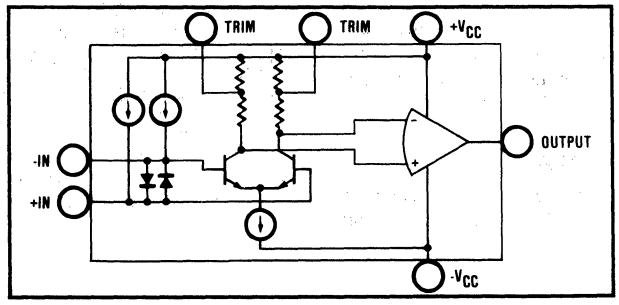
Low noise integrated processing, a unique circuit design, and advanced wafer level trimming techniques are combined in the OPA27/37 to produce an extremely-high performance "instrumentation grade" operational amplifier.

The OPA27/37 provide superior performance in three areas - low noise, excellent DC performance, and high speed (OPA37 is stable in gains > 5).

Noise is typically only 3nV/$\sqrt{Hz}$ at 1kHz with an exceptionally low 1/f corner frequency of 2.7Hz. Peak-to-peak noise is just 80nV in a 0.1Hz to 10Hz bandwidth.

Offset voltage is typically just 10μV and drift is only 0.2μV/°C. 125dB open-loop gain is matched with 125dB common-mode rejection ratio. Power consumption is only 3mA.

The same basic op amp comes in two frequency compensation versions. The OPA37 is lightly compensated and provides 17V/μsec slew rate and 63MHz gain-bandwidth product. The OPA27 is more heavily compensated for better frequency stability in low gain applications. It has a 2.8V/μsec slew rate and an 8MHz unity gain frequency.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-466

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

		OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			
PARAMETERS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INITIAL OFFSET VOLTAGE											
Initial Offset(1)	T_A = +25°C		10	25		20	60		30	100	µV
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C		30	60		50	200		70	300	µV
Average vs Temperature	A, B, C -55°C ≤ T_A ≤ +125°C(2)		0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C		20	50		40	140		55	22	µV
Average vs Temperature	E, F, G -25°C ≤ T_A ≤ +85°C(2)		0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Long Term Stability(3)			0.2	1.0		0.3	1.5		0.4	2.0	µV/mo
Offset Adjustment Range			±4			*			*		mV
INPUT OFFSET CURRENT											
Initial Offset	T_A = +25°C		7	35		9	50		12	75	nA
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C		15	50		22	85		30	135	nA
	E, F, G -25°C ≤ T_A ≤ +85°C		10	50		14	85		20	135	nA
INPUT BIAS CURRENT											
Initial Bias	T_A = +25°C		±10	±40		±12	±55		±15	±80	nA
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C		±20	±60		±28	±95		±35	±150	nA
	E, F, G -25°C ≤ T_A ≤ +85°C		±14	±60		±18	±95		±25	±150	nA
INPUT NOISE											
Voltage	0.1Hz to 10Hz(4)(5)		0.08	0.18		*	*		0.09	0.25	µV, p-p
Voltage Density	f_O = 10Hz(4)		3.5	5.5		*	*		3.8	8.0	nV $\sqrt{Hz}$
	f_O = 30Hz(4)		3.1	4.5		*	*		3.3	5.6	nV $\sqrt{Hz}$
	f_O = 1000Hz(4)		3.0	3.8		*	*		3.2	4.5	nV $\sqrt{Hz}$
Current Density	f_O = 10Hz(4)(6)		1.7	4.0		*	*		*		pA $\sqrt{Hz}$
	f_O = 30Hz(4)(6)		1.0	2.3		*	*		*		pA $\sqrt{Hz}$
	f_O = 1000Hz(4)(6)		0.4	0.6		*	*		*	*	pA $\sqrt{Hz}$
INPUT RESISTANCE											
Differential(7)		1.5	6		1.2	5		0.8	4		MΩ
Common-Mode			3			2.5			2		GΩ
INPUT VOLTAGE RANGE											
Initial Input Voltage	T_A = +25°C	±11.0	±12.3		*	*		*	*		V
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C	±10.3	±11.5		*	*		*	*		V
	E, F, G -25°C ≤ T_A ≤ +85°C	±10.5	±11.8		*	*		*	*		V
COMMON-MODE REJECTION RATIO											
Initial Rejection Ratio	V_{CM} = ±11V	114	126		106	123		100	120		dB
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C	108	122		100	119		94	116		dB
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C	110	124		102	121		96	118		dB
POWER SUPPLY REJECTION RATIO											
Initial Rejection Ratio	$\pm V_{CC}$ = 4V to 18V	100	120		*	*		94	118		dB
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C ($\pm V_{CC}$ = 4.5V to 18V)	96	116		94	114		86	110		dB
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C ($\pm V_{CC}$ = 4.5V to 18V)	97	118		96	116		90	114		dB
LARGE SIGNAL VOLTAGE GAIN(7)(8)											
Initial Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	1000	1800		*	*		700	1500		V/mV
	R_L ≥ 1kΩ, V_O = ±10V	800	1500		*	*			*		V/mV
	R_L ≥ 600Ω, V_O = ±1V, V_{CC} = ±4V	250	700		*	*		200	500		V/mV
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C (R_L ≥ 2kΩ, V_O = ±10V)	600	1200		500	1000		300	800		V/mV
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C (R_L ≥ 2kΩ, V_O = ±10V)	750	1500		700	1300		450	1000		V/mV
RATED OUTPUT											
Initial Voltage Swing	R_L ≥ 2kΩ	±12.0	±13.8		*	*		±11.5	±13.5		V
	R_L ≥ 600Ω	±10.0	±11.5		*	*		*	*		V
Over Temperature	A, B, C -55°C ≤ T_A ≤ +125°C (R_L ≥ 2kΩ)	±11.5	±13.5		±11.0	±13.2		±10.5	±13.0		V
Over Temperature	E, F, G -25°C ≤ T_A ≤ +85°C (R_L ≥ 2kΩ)	±11.7	±13.6		±11.4	±13.5		±11.0	±13.3		V
Output Resistance	Open Loop		70			*			*		Ω
DYNAMIC RESPONSE											
Slew Rate	OPA27	1.7	2.8		*	*		*	*		V/µsec
	OPA37	11	17		*	*		*	*		V/µsec
Gain-Bandwidth Product	OPA27	5	8		*	*		*	*		MHz
	OPA37		40			*			*		MHz

ELECTRICAL (CONT)

PARAMETERS	CONDITIONS	OPA27/37A, OPA27/37E			OPA27/37B, OPA27/37F			OPA27/37C, OPA27/37G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range		±4		±22	*		*		*	*	VDC
Current, Quiescent			±3	±4.7		*	*		±3.3	±5.7	mA
Power Comsumption			90	140		*	*		100	170	mW
TEMPERATURE RANGE											
Specification A, B, C		-55		+125	*		*	*		*	°C
E, F, G		-25		+85	*		*	*		*	°C
Operating A, B, C		-55		+125	*		*	*		*	°C
E, F, G		-25		+85	*		*	*		*	°C
Storage		-65		+150	*		*	*		*	°C

*Specification same as OPA27/37A and OPA27/37E.

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with R_P = 8kΩ to 20kΩ.
3. Long Term Input Offset Voltage Stability refers to average trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV (refer to Typical Performance Curves).
4. Parameter is not 100% tested; 90% of units meet this specification.
5. See Figures 1 and 2.
6. See Figure 1 for current noise measurement.
7. Parameter is guaranteed by design and is not tested.
8. Closed-loop gain ≥ 5 is required for stability in the OPA37. OPA27 is stable at unity gain.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Internal Power Dissipation(1) 500mW
Input Voltage(3) ..... ±22V
Output Short Circuit Duration ..... Indefinite
Differential Input Voltage(2) ..... ±0.7V
Differential Input Current(2) ..... ±25mA
Storage Temperature Range .... -65°C to +150°C
Operating Temperature Range
A, B, C ..... -55°C to +125°C
E, F, G ..... -25°C to +85°C
Lead Temperature Range
(Soldering, 60sec) ..... 300°C

NOTES:

1. Maximum Package Power Dissipation vs ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
8-Pin Heremetic Dip (Z)	75°C	6.7mW/°C

2. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

OPAXX Y Z

Basic Model Number
Performance Grade Code
A, B, C -55°C to +125°C
E, F, G -25°C to +85°C
Package Code
J TO-99
Z 8-Pin Hermetic DIP

TO-99 J SUFFIX		8-PIN HERMETIC DIP	
OPA27AJ	OPA27EJ	OPA27AZ	OPA27EZ
OPA27BJ	OPA27FJ	OPA27BZ	OPA27FZ
OPA27CJ	OPA27GJ	OPA27CZ	OPA27GZ
OPA37AJ	OPA37EJ	OPA37AZ	OPA37EZ
OPA37BJ	OPA37FJ	OPA37BZ	OPA37FZ
OPA37CJ	OPA37GJ	OPA37CZ	OPA37GZ

NOTE: All parts available with /883 screening.

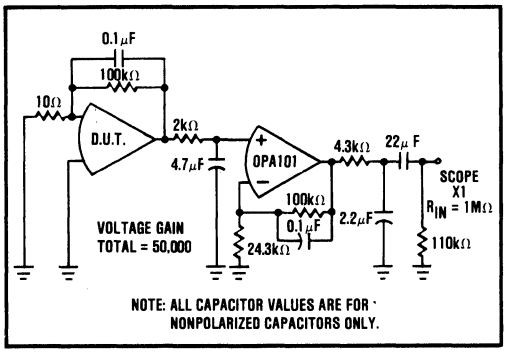


FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

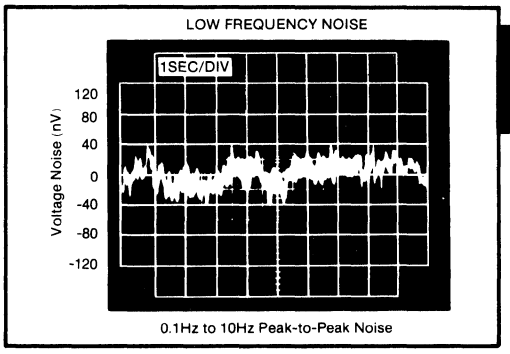
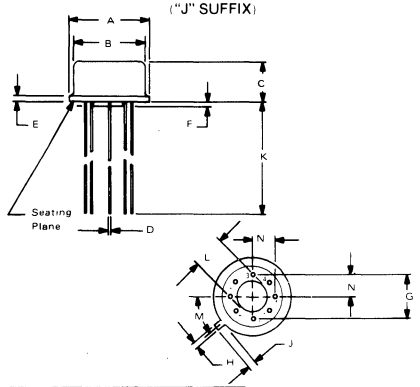


FIGURE 2. Low Frequency Noise.

MECHANICAL

TO-99 PACKAGE
("J" SUFFIX)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

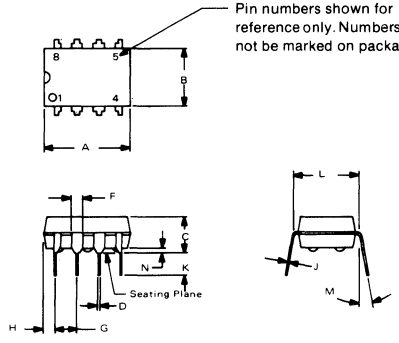
NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

The TO-99 can and leads are bright acid tin plated.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 except paragraph 3.2).

8-PIN HERMETIC DIP
("Z" SUFFIX)

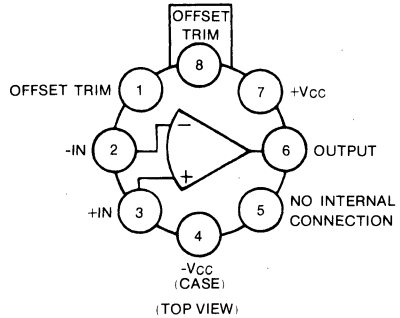


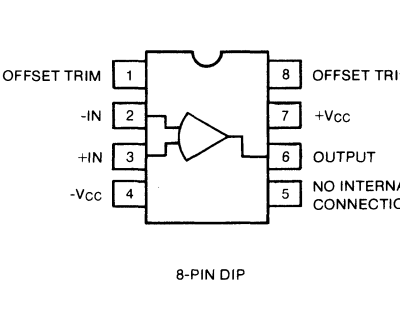
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.370	.400	9.40	10.16
B	.230	.290	5.84	7.37
C	.120	.200	3.05	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.050	0.76	1.27
J	.008	.015	0.20	0.38
K	.070	.135	1.78	3.43
L	.300 BASIC		7.62 BASIC	
M		10°		10°
N	.010	.030	0.25	0.76

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

PIN CONFIGURATION

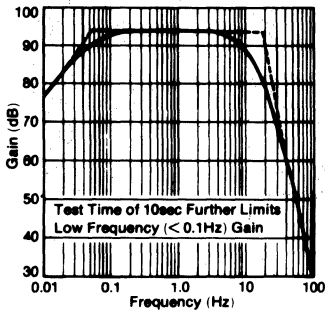




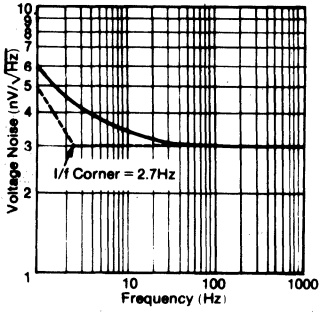
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted)

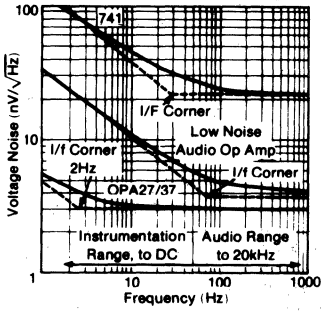
0.1Hz TO 10Hz, p-p NOISE TESTER FREQUENCY RESPONSE



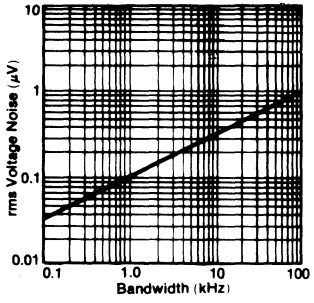
VOLTAGE NOISE VS FREQUENCY



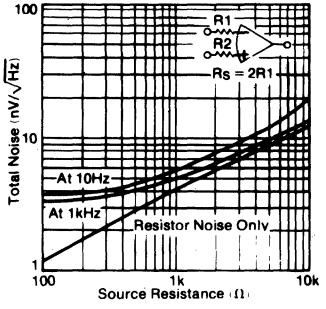
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRUMS



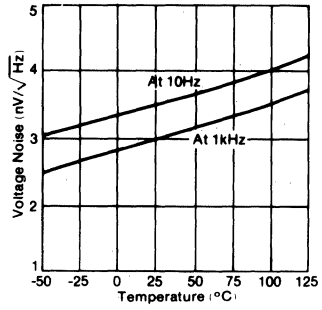
INPUT WIDEBAND VOLTAGE NOISE VS BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



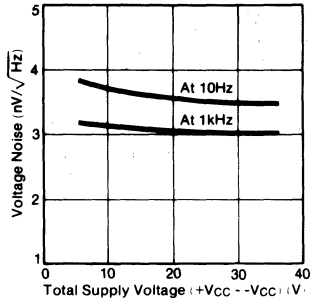
TOTAL NOISE VS SOURCE RESISTANCE



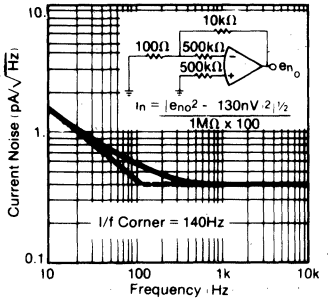
VOLTAGE NOISE VS TEMPERATURE



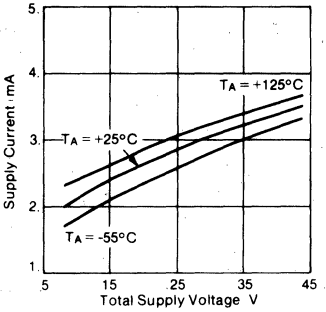
VOLTAGE NOISE VS SUPPLY VOLTAGE



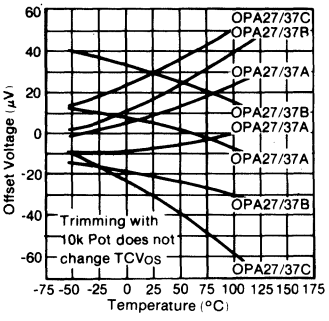
CURRENT NOISE VS FREQUENCY



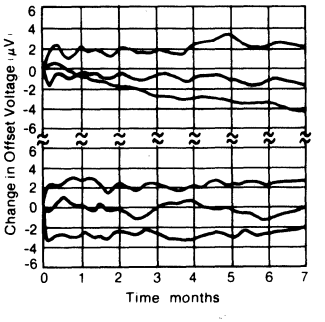
SUPPLY CURRENT VS SUPPLY VOLTAGE



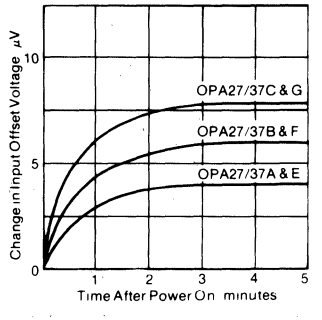
OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS



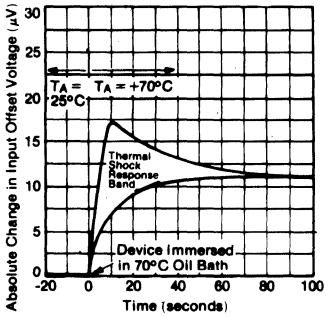
LONG TERM DRIFT OF REPESENTATIVE UNITS



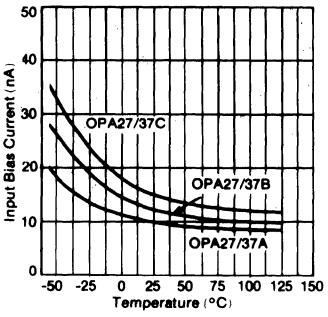
WARM-UP DRIFT



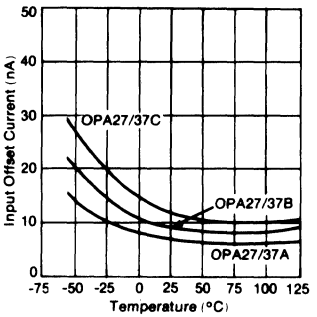
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



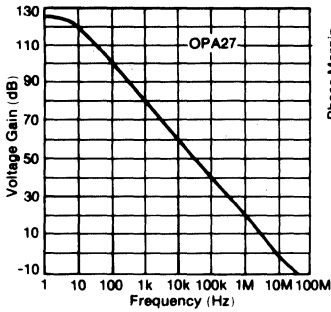
INPUT BIAS CURRENT VS TEMPERATURE



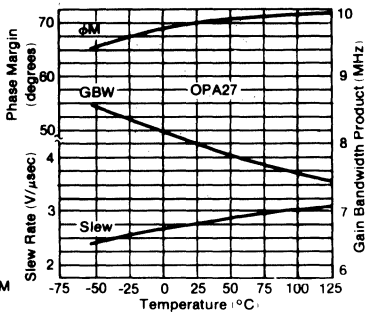
INPUT OFFSET CURRENT VS TEMPERATURE



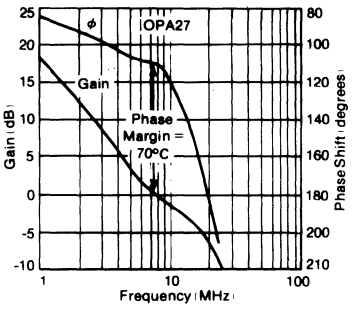
OPEN-LOOP GAIN VS FREQUENCY



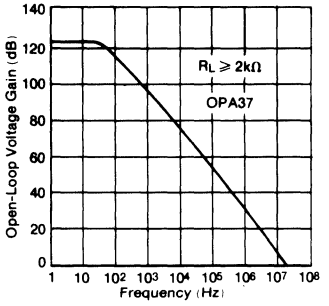
SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN VS TEMPERATURE



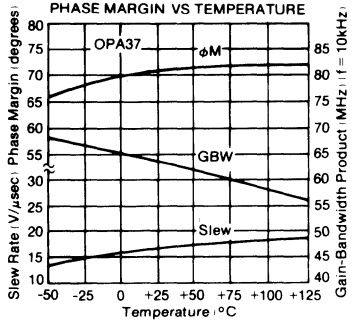
GAIN, PHASE SHIFT VS FREQUENCY



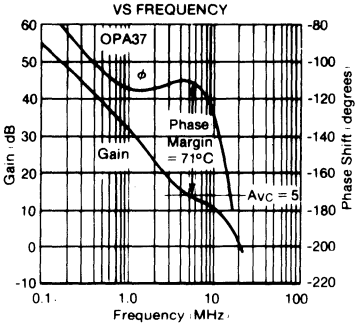
OPEN-LOOP GAIN VS FREQUENCY



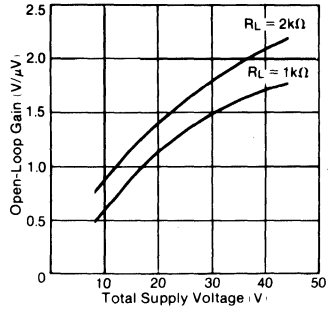
SLEW RATE, GAIN BANDWIDTH PRODUCT PHASE MARGIN VS TEMPERATURE



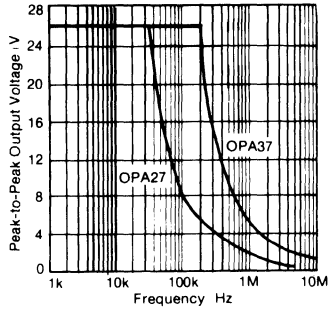
GAIN, PHASE VS FREQUENCY



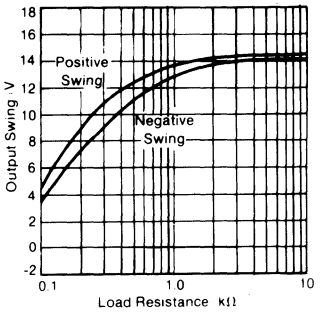
OPEN-LOOP VOLTAGE GAIN VS SUPPLY VOLTAGE



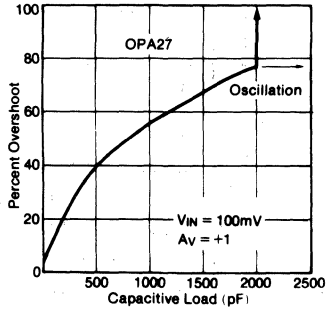
MAXIMUM UNDISTORTED OUTPUT VS FREQUENCY



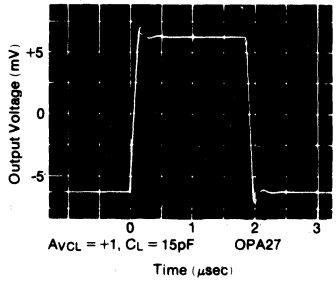
MAXIMUM OUTPUT SWING VS RESISTIVE LOAD



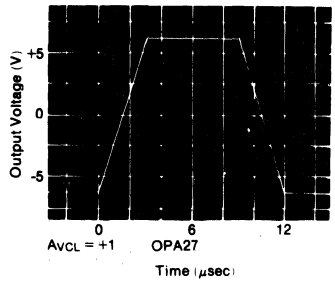
SMALL SIGNAL OVERSHOOT VS CAPACITIVE LOAD



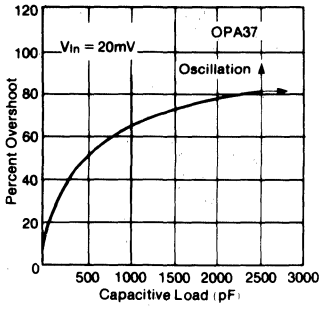
SMALL SIGNAL TRANSIENT RESPONSE



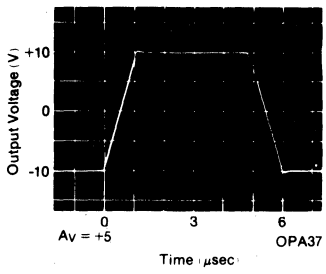
LARGE SIGNAL TRANSIENT RESPONSE



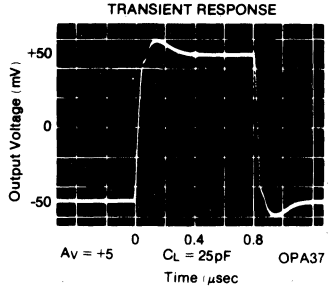
SMALL SIGNAL OVERSHOOT VS CAPACITIVE LOAD



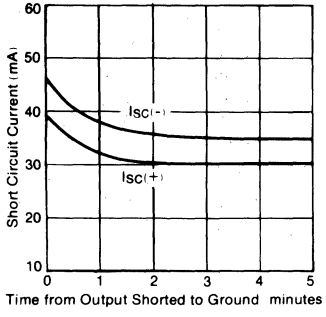
LARGE SIGNAL TRANSIENT RESPONSE



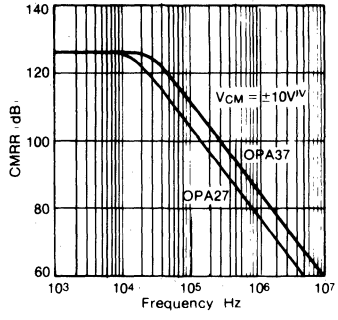
SMALL SIGNAL TRANSIENT RESPONSE



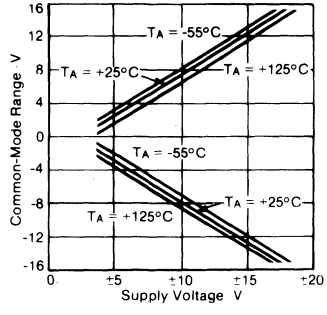
SHORT CIRCUIT CURRENT VS TIME



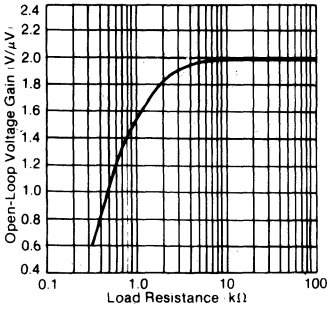
CMRR VS FREQUENCY



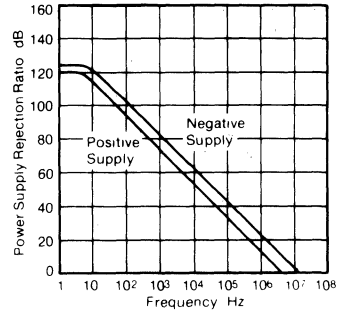
COMMON-MODE INPUT RANGE VS SUPPLY VOLTAGE



OPEN-LOOP VOLTAGE GAIN VS LOAD RESISTANCE



PSRR VS FREQUENCY



APPLICATION INFORMATION

OPA27/37 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, OPA27/37 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OPA27/37 operation. OPA27/37 offset voltage may be nulled to zero (or other desired setting) through use of a potentiometer (see Figure 3).

OPA27/37 provides stable operation with load capacitances up to 2000pF and ±10V swings; larger capacitances should be decoupled with 50Ω decoupling resistor.

The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferable close to the temperature of the device's package.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage and its drift with temperature of the OPA27/37 are permanently trimmed at wafer testing to a very-low level. However, if further adjustment of V_{OS} is necessary, nulling with a 10kΩ potentiometer will not degrade TCV_{OS} (see Figure 4). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of (V_{OS}/300) μV/°C, e.g., if V_{OS} is adjusted to 100μV, the change in TCV_{OS} will be 0.33μV/°C. The offset voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the sensitivity and/or resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors. For example, the network in Figure 3 will have a ±280μV adjustment range.

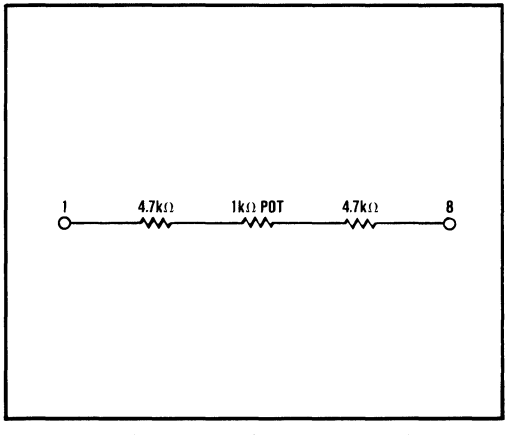


FIGURE 3. Higher Resolution Nulling Circuit.

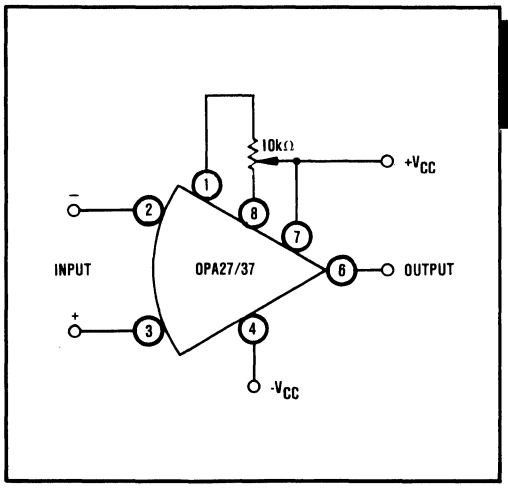


FIGURE 4. Offset Nulling Circuit.

UNITY GAIN BUFFER APPLICATIONS - OPA27.

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (> 1V), the output waveform will look as shown in Figure 4.

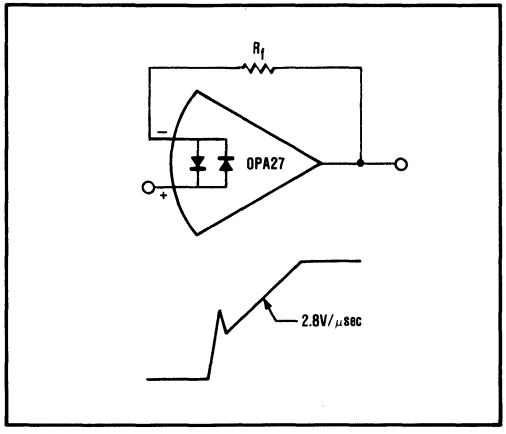


FIGURE 5. Pulsed Operation.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. This results in the waveform shown in Figure 5. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_f \leq 20$mA at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_f \geq 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance (8pF), creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_f will eliminate this problem.

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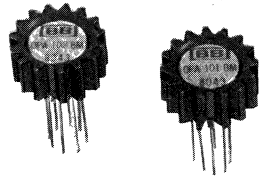


OPA101
OPA102

Low Noise - Wideband
PRECISION JFET INPUT OPERATIONAL AMPLIFIER

FEATURES

- GUARANTEED NOISE SPECTRAL DENSITY - 100% Tested
- LOW VOLTAGE NOISE - 8nV/$\sqrt{Hz}$ max at 10kHz
- LOW VOLTAGE DRIFT - 5μV/°C max (B grade)
- LOW OFFSET VOLTAGE - 250μV max (B grade)
- LOW BIAS CURRENTS - 10pA max at 25°C Ambient (B Grade)
- HIGH SPEED - 10V/μsec min (OPA102)
- GAIN BANDWIDTH PRODUCT - 40MHz (OPA102)

APPLICATIONS

- LOW NOISE SIGNAL CONDITIONING
- LIGHT MEASURMENTS
- RADIATION MEASUREMENTS
- PIN DIODE APPLICATIONS
- DENSITOMETERS
- PHOTODIODE/PHOTOMULTIPLIER CIRCUITS
- LOW NOISE DATA ACQUISITION

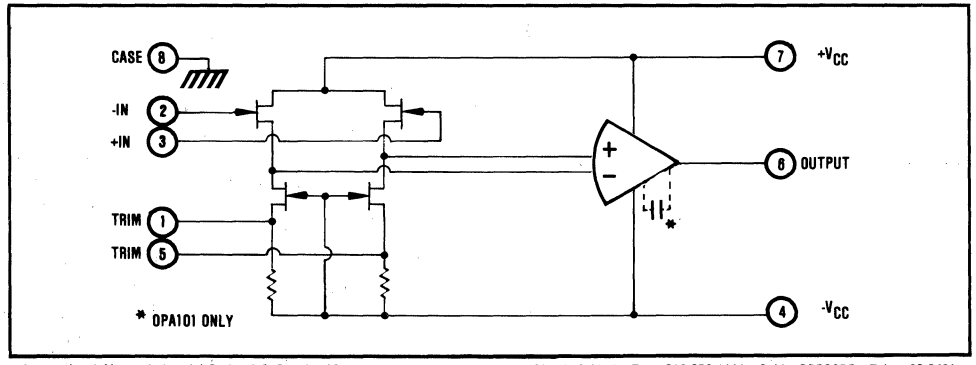
DESCRIPTION

The OPA101 and OPA102 are the first FET operational amplifiers available with noise characteristics (voltage spectral density) guaranteed and 100% tested.

The amplifiers have a complementary set of specifications permitting low errors in signal conditioning applications; low noise, low bias current, high open-loop gain, high common-mode rejection, low offset voltage, low offset voltage drift, etc.

In addition, the amplifiers have moderately high speed. The OPA101 is compensated for unity gain stability and has a slew rate of 5V/μsec, min. The OPA102 is compensated for gains of 3V/V and above and has a slew rate of 10V/μsec, min.

Each unit is laser-trimmed for low offset voltage and low offset voltage drift versus temperature. Bias currents are specified with the units fully warmed up at +25°C ambient temperature.



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PDS-434A

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT NOISE								
Voltage Noise Density	f_O = 1Hz(1)		100	200		80	100	$nV/\sqrt{Hz}$
	f_O = 10Hz		32	60		25	30	$nV/\sqrt{Hz}$
	f_O = 100Hz		14	30		11	15	$nV/\sqrt{Hz}$
	f_O = 1kHz		9	15		8	12	$nV/\sqrt{Hz}$
	f_O = 10kHz		7	8		7	8	$nV/\sqrt{Hz}$
	f_O = 100kHz		6.5	8		6.5	8	$nV/\sqrt{Hz}$
f_C; 1/f Corner Frequency			125			100		Hz
Voltage Noise	f_B = 0.1Hz to 10Hz(1)		1.3	2.6		1.0	1.3	µV, p-p
	f_B = 10Hz to 10kHz		1.0	1.2		0.8	1.0	µV, rms
	f_B = 10Hz to 100kHz		2.1	2.6		2.1	2.6	µV, rms
Current Noise Density	f_O = 0.1Hz thru 10kHz		2.0			1.4		$fA/\sqrt{Hz}$
Current Noise	f_B = 0.1Hz to 10Hz		38			26		fA, p-p
	f_B = 10Hz to 10kHz		200			140		fA, rms
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal							
OPA101			10			*		MHz
OPA102			Note 2			*		
Gain-Bandwidth Product	A_{CL} = 100							
OPA101			20			*		MHz
OPA102			40			*		MHz
Full Power Bandwidth	V_O = 20V, p-p; R_L = 1kΩ							
OPA101		80	100		*	*		kHz
OPA102		160	210		*	*		kHz
Slew Rate	V_O = ±10V; R_L = 1kΩ							
OPA101	A_{CL} = -1	5	6.5		*	*		V/µsec
OPA102	A_{CL} = -3	10	14		*	*		V/µsec
Settling Time (OPA101)	V_O = ±5V; A_{CL} = -1; R_L = 1kΩ							
ε = 1%			2			*		µsec
ε = 0.1%			2.5			*		µsec
ε = 0.01%			10			*		µsec
Settling Time (OPA102)	V_O = ±5V; A_{CL} = -3; R_L = 1kΩ							
ε = 1%			1			*		µsec
ε = 0.1%			1.5			*		µsec
ε = 0.01%			8			*		µsec
Small-Signal Overshoot	R_L = 1kΩ; C_L = 100pF							
OPA101	A_{CL} = +1		15			*		%
OPA102	A_{CL} = +3		20			*		%
Rise Time	10% to 90%, Small Signal							
OPA101			40			*		nsec
OPA102			30			*		nsec
Phase Margin	R_L = 1kΩ							
OPA101	A_{CL} = +1		60			*		Degrees
OPA102	A_{CL} = +3		45			*		Degrees
Overload Recovery(3)								
OPA101	A_{CL} = -1, 50% overdrive		1			*		µsec
OPA102	A_{CL} = -3, 50% overdrive		0.8			*		µsec
OPEN-LOOP GAIN, DC								
Full Load	V_O = ±10V; R_L = 1kΩ	94	105		*	*		dB
No Load	V_O = ±10V; R_L ≥ 10kΩ	96	108		*	*		dB
RATED OUTPUT								
Voltage	I_O = ±12mA	±12	±13		*	*		V
Current	V_O = ±12V	±12	±30		*	*		mA
Output Resistance	Open-Loop, f = DC		500			*		Ω
Short-Circuit Current			±45			*		mA
Capacitive Load Range	Phase Margin ≥ 25°							
OPA101	A_{CL} = +1		500			*		pF
OPA102	A_{CL} = +3		300			*		pF
INPUT OFFSET VOLTAGE								
Initial Offset	T_A = +25°C		±100	±500		±50	±250	µV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6	±10		±3	±5	µV/°C
vs Supply Voltage	±5VDC ≤ | V_{CC} | ≤ ±20VDC		±10	±50		*	*	µV/V
vs Time			±10			*		µV/mo.
Adjustment Range	Circuit in "Connection Diagram"		±1			*		mV
INPUT BIAS CURRENT								
Initial Bias	T_A = +25°C		-12	-15		-6	-10	pA
vs Temperature			Note 4			*		
vs Supply Voltage			Note 5			*		

ELECTRICAL (CONT)

MODEL		OPA101/102AM			OPA101/102BM			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT DIFFERENCE CURRENT								
Initial Difference	T_A = +25°C		±3	±6		±1.5	±4	pA
vs Temperature			Note 4			*		
vs Supply Voltage			Note 5			*		
INPUT IMPEDANCE								
Differential								
Resistance			10^{12}			*		Ω
Capacitance			1			*		pF
Common-mode								
Resistance			10^{13}			*		Ω
Capacitance			3			*		pF
INPUT VOLTAGE RANGE								
Common-mode Voltage Range	Linear Operation		±(| V_{CC} | -3)			*		V
Common-mode Rejection	f_o = DC, V_{CM} = ±10V	80	105		*	*		dB
POWER SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range	Derated Performance	±5		±20	*		*	VDC
Current, Quiescent			5.8	8		*	*	mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Operating	Derated Performance	-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

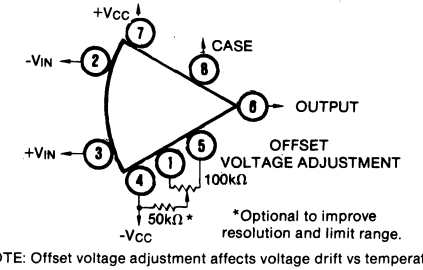
NOTES: *Specifications same as for OPA101/102AM.
1. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
2. Minimum stable gain for the OPA102 is 3V/V.
3. Time required for output to return from saturation to linear operation following the removal of an input overdrive signal.
4. Doubles approximately every 8.5°C.
5. See Typical Performance Curves.

ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	750mW
Differential Input Voltage(2)	±20VDC
Input Voltage, Either Input(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration(3)	60 seconds
Junction Temperature	+175°C

NOTES:
1. Package must be derated according to the details in the Application Information section.
2. For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage.
3. Short-circuit may be to ground only. See discussion of Thermal Model in the Application Information section.

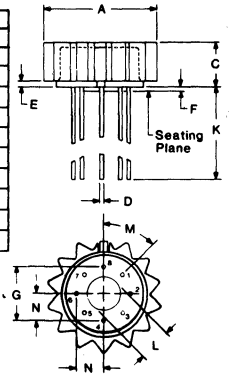
CONNECTION DIAGRAM



NOTE: Offset voltage adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted.

MECHANICAL SPECIFICATIONS

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.489	.522	12.42	13.26
C	.243	.307	6.17	7.80
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

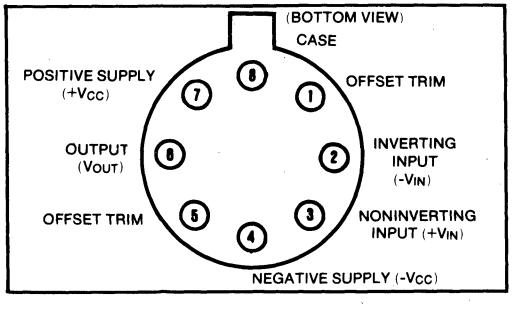


NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.
Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

Weight: 2 grams

Order Number:
OPA101AM OPA101BM
OPA102AM OPA102BM

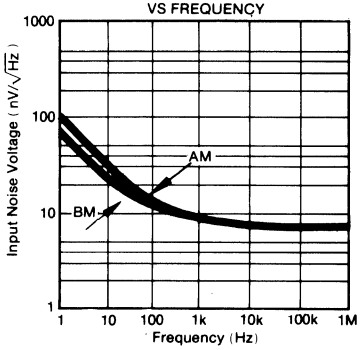
PIN CONFIGURATION



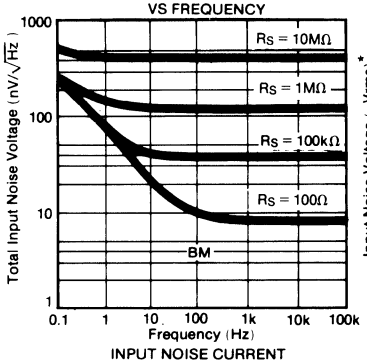
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = ±15VDC, unless otherwise noted. Performance curves apply to both OPA101 and OPA102 unless otherwise noted.)

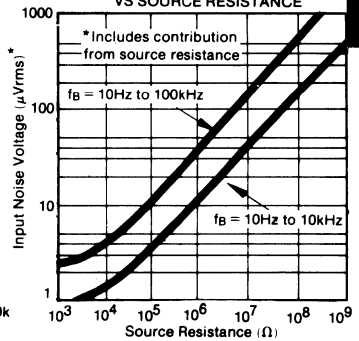
INPUT NOISE VOLTAGE VS FREQUENCY



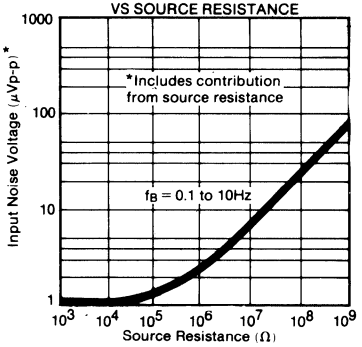
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



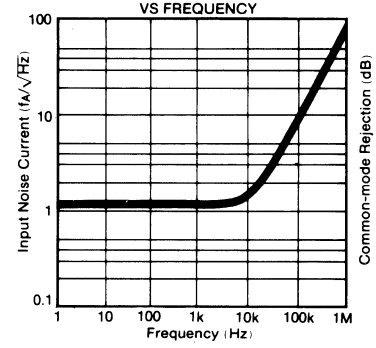
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



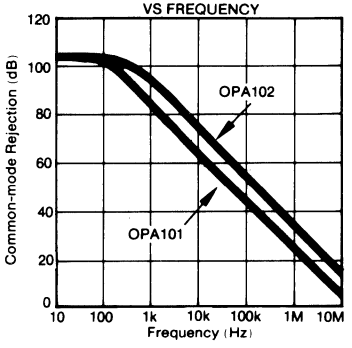
PEAK-TO-PEAK INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



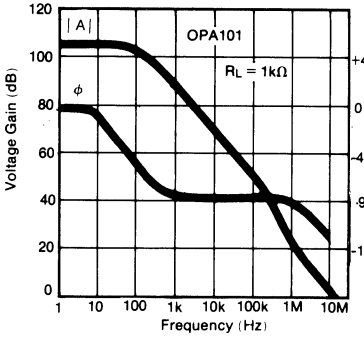
INPUT NOISE CURRENT VS FREQUENCY



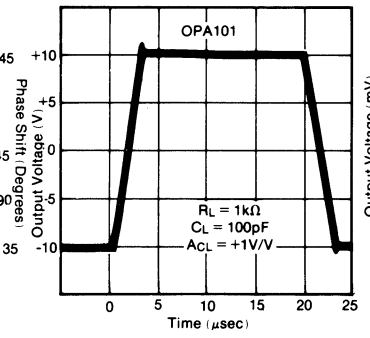
COMMON-MODE REJECTION VS FREQUENCY



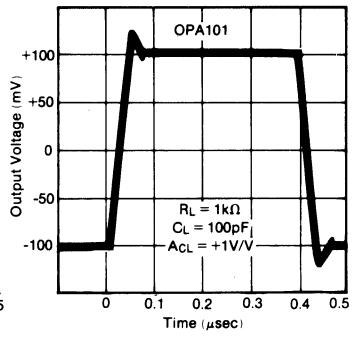
OPEN-LOOP FREQUENCY RESPONSE



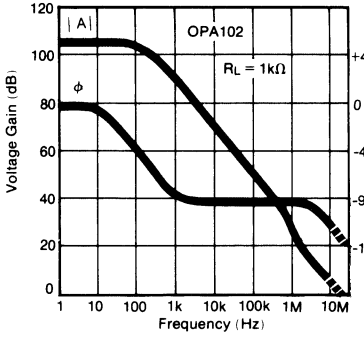
LARGE SIGNAL TRANSIENT RESPONSE



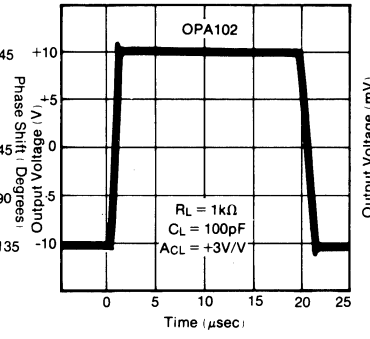
SMALL SIGNAL TRANSIENT RESPONSE



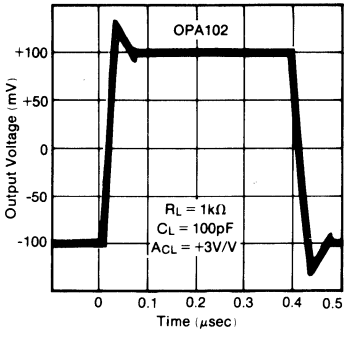
OPEN-LOOP FREQUENCY RESPONSE



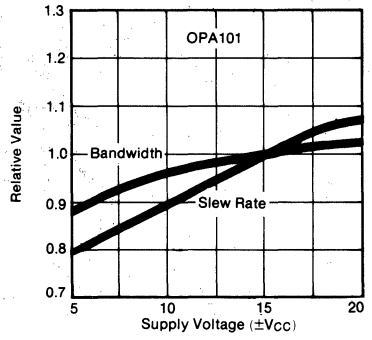
LARGE SIGNAL TRANSIENT RESPONSE



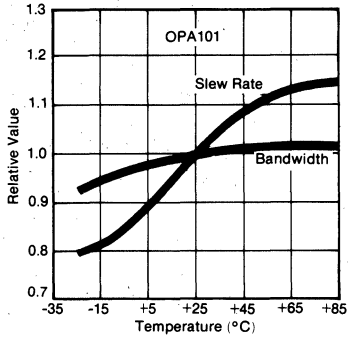
SMALL SIGNAL TRANSIENT RESPONSE



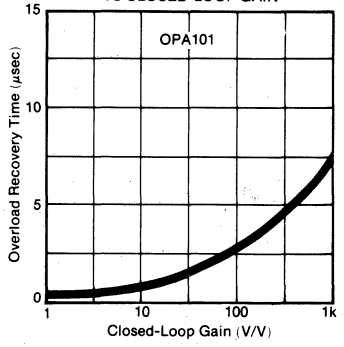
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



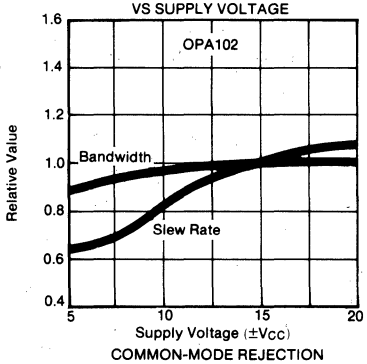
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



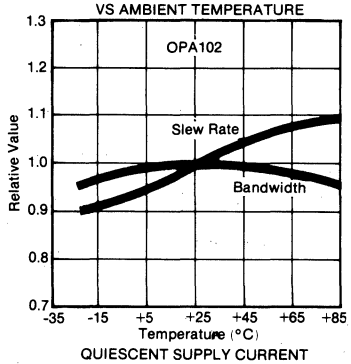
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



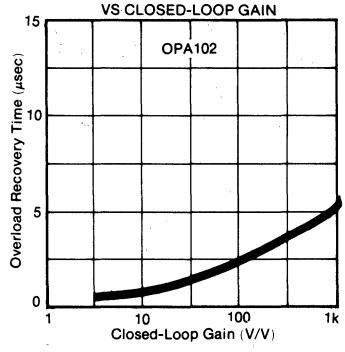
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



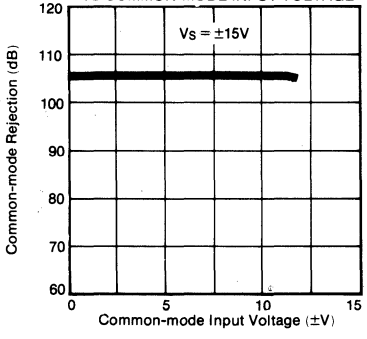
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



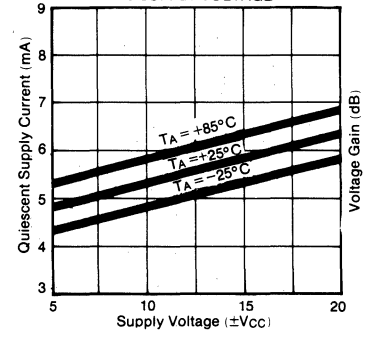
OVERLOAD RECOVERY TIME VS CLOSED-LOOP GAIN



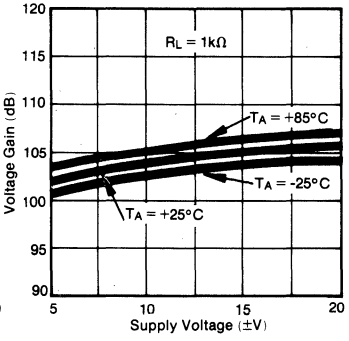
COMMON-MODE REJECTION VS COMMON-MODE INPUT VOLTAGE



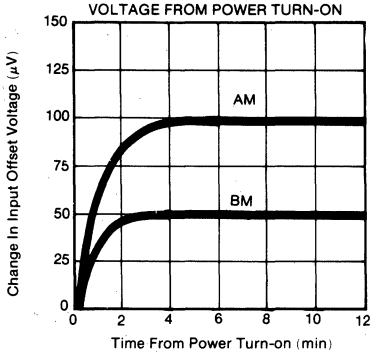
QUIESCENT SUPPLY CURRENT VS SUPPLY VOLTAGE



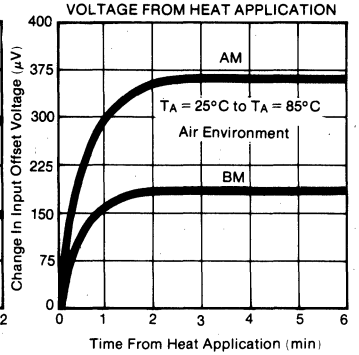
VOLTAGE GAIN VS SUPPLY VOLTAGE



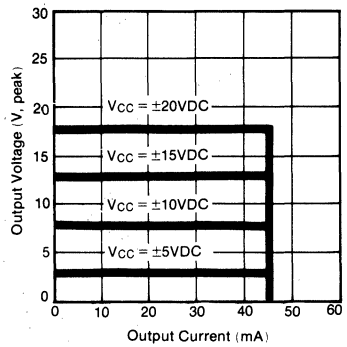
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



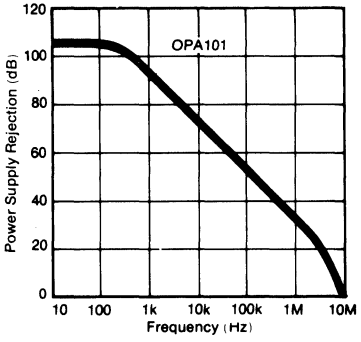
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



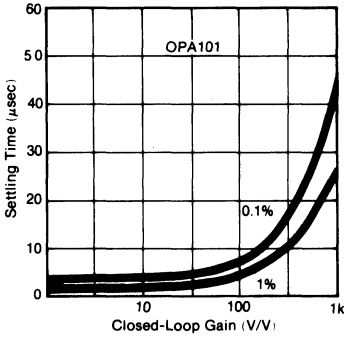
OUTPUT VOLTAGE VS OUTPUT CURRENT



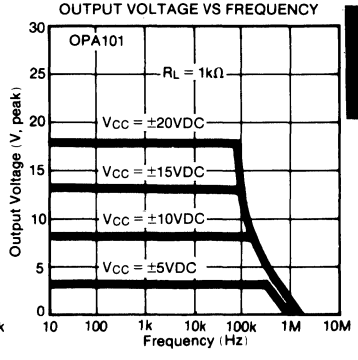
POWER SUPPLY REJECTION VS FREQUENCY



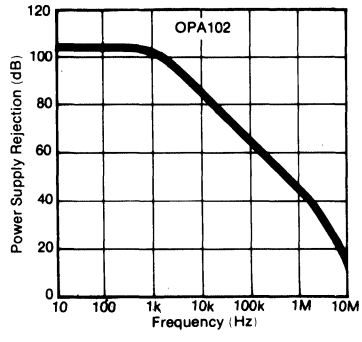
SETTLING TIME VS CLOSED-LOOP GAIN



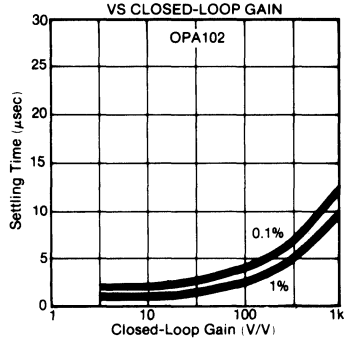
OUTPUT VOLTAGE VS FREQUENCY



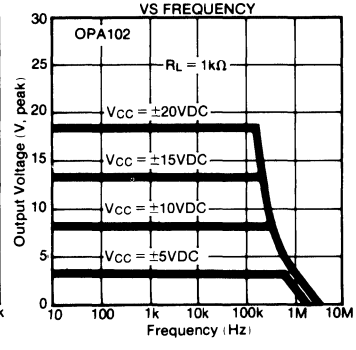
POWER SUPPLY REJECTION VS FREQUENCY



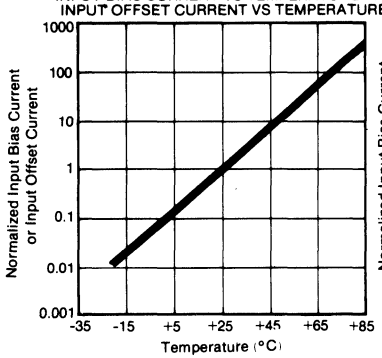
SETTLING TIME VS CLOSED-LOOP GAIN



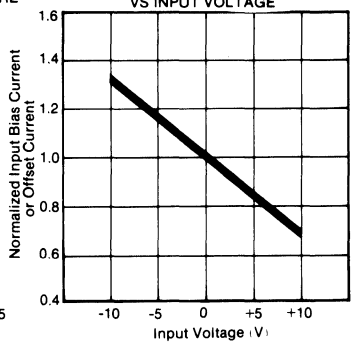
OUTPUT VOLTAGE VS FREQUENCY



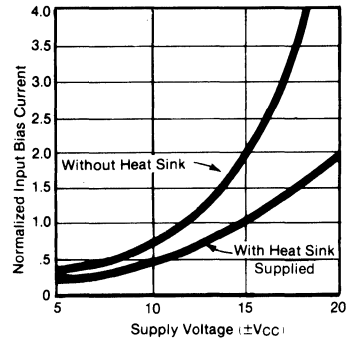
INPUT BIAS CURRENT VS TEMPERATURE AND INPUT OFFSET CURRENT VS TEMPERATURE



INPUT BIAS CURRENT VS INPUT VOLTAGE AND INPUT OFFSET CURRENT VS INPUT VOLTAGE



INPUT BIAS CURRENT VS SUPPLY VOLTAGE



APPLICATION INFORMATION

INTRODUCTION

The availability of detailed noise spectral density characteristics for the OPA101/102 amplifiers allows an accurate noise error analysis in a variety of different circuit configurations. The fact that the spectral characteristics are guaranteed maximums allows absolute noise errors to be truly bounded. Other FET amplifiers normally use simpler specifications of rms noise in a given bandwidth (typically 10Hz to 10kHz) and peak-to-peak noise (typically specified in the band 0.1Hz to 10Hz). These specifications do not contain enough information to allow accurate analysis of noise behavior in any but the simplest of circuit configurations.

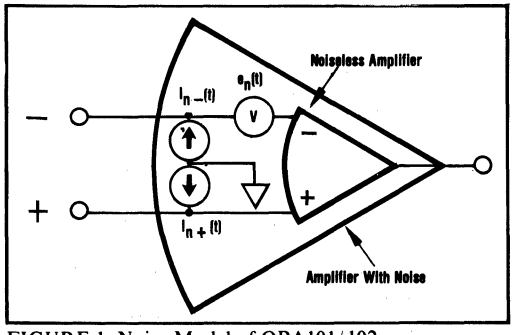


FIGURE 1. Noise Model of OPA101/102.

Noise in the OPA101/102 can be modeled as shown in Figure 1. This model is the same form as the DC model for offset voltage (E_{OS}) and bias currents (I_B). In fact, if the voltage $e_n(t)$ and currents $i_n(t)$ are thought of as general instantaneous error sources, then they could represent either noise or DC offsets. The error equations for the general instantaneous model are shown in Figure 2 below.

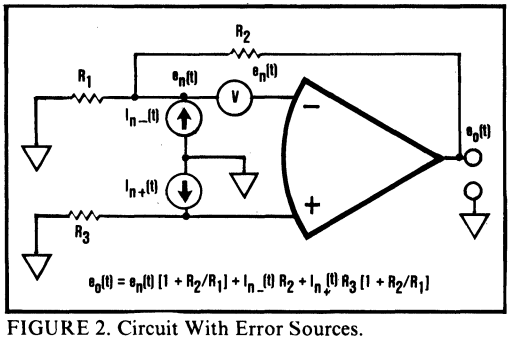


FIGURE 2. Circuit With Error Sources.

If the instantaneous terms represent DC errors (i.e., offset voltage and bias currents) the equation is a useful tool to compute actual errors. It is not, however, useful in the same direct way to compute noise errors. The basic problem is that noise cannot be predicted as a function of time. It is a random variable and must be described in probabilistic terms. It is normally described by some type of average - most commonly the rms value.

$$N_{rms} \triangleq \sqrt{1/T \int_0^T n^2(t)\,dt} \qquad (1)$$

where N_{rms} is the rms value of some random variable n(t). In the case of amplifier noise, n(t) represents either $e_n(t)$ or $i_n(t)$.

The internal noise sources in operational amplifiers are normally uncorrelated. That is, they are randomly related to each other in time and there is no systematic phase relationship. Uncorrelated noise quantities are combined as root-sum-squares. Thus, if $n_1(t)$, $n_2(t)$, and $n_3(t)$ are uncorrelated then their combined value is

$$N_{TOTAL_{rms}} = \sqrt{N_1^2{}_{rms} + N_2^2{}_{rms} + N_3^2{}_{rms}} \qquad (2)$$

The basic approach in noise error calculations then is to identify the noise sources, segment them into conveniently handled groups (in terms of the shape of their noise spectral densities), compute the rms value of each group, and then combine them by root-sum-squares to get the total noise.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

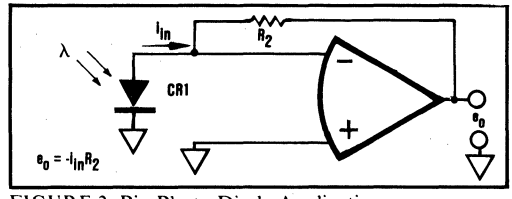


FIGURE 3. Pin Photo Diode Application.

CR1 is a PIN photo diode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{in} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 is what would be expected from stray capacitance with moderately careful layout (0.5pF to 2pF). A larger value of C_2 would normally be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

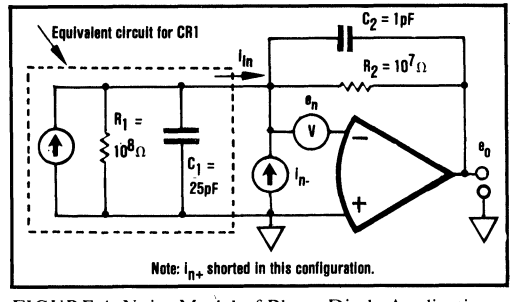


FIGURE 4. Noise Model of Photo Diode Application.

In Figure 4, e_n and i_n represent the amplifier's voltage and current spectral densities, $e_n(\omega)$ and $i_n(\omega)$ respectively. These are shown in Figure 5.

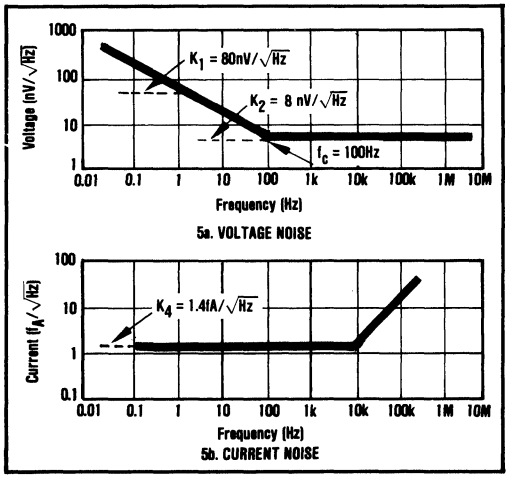


FIGURE 5. Noise Voltage and Current Spectral Density.

Figure 6 shows the desired "gain" of the circuit (transimpedance of $e_o/i_{in} = Z_2(s)$). It has a single-pole rolloff at $f_2 = 1/(2\pi R_2 C_2) = \omega_2/2\pi$. Output noise is minimized if f_2 is made smaller. Normally R_2 is chosen for the desired DC transimpedance based on the full scale input current (i_{in} full scale) and maximum output (e_o max). Then C_2 is chosen to make f_2 as small as possible consistent with the necessary signal frequency response.

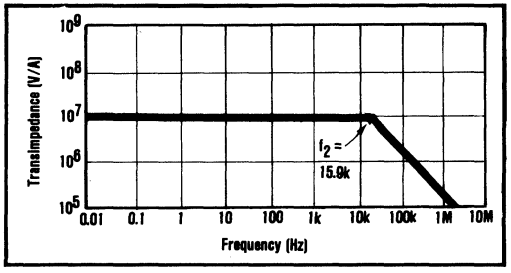


FIGURE 6. Transimpedance.

Voltage Noise

Figure 7 shows the noise voltage gain for the circuit in Figure 4. It is derived from the equation

$$e_o = e_n \left[\frac{A}{1 + A\beta} \right] = e_n \frac{1}{\beta} \left[\frac{1}{1 + \frac{1}{A\beta}} \right] \qquad (3)$$

where:

$A = A(\omega)$ is the open-loop gain

$\beta = \beta(\omega)$ is the feedback factor. It is the amount of output voltage feedback to the input of the op amp.

$A\beta = A(\omega)\,\beta(\omega)$ is the loop gain. It is the amount of the output voltage feedback to the input and then amplified and returned to the output.

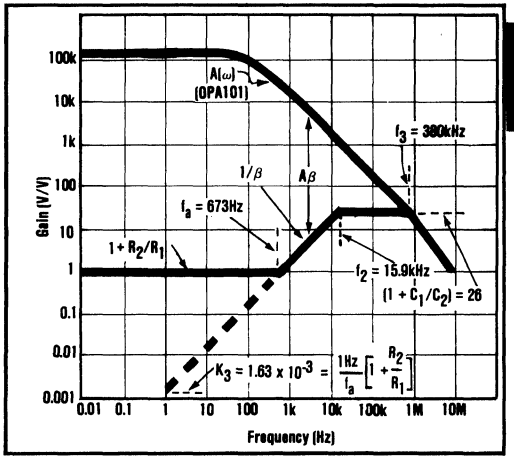


FIGURE 7. Noise Voltage Gain.

Note that for large loop gain ($A\beta >> 1$)

$$e_o \cong e_n \frac{1}{\beta} \cdot \qquad (4)$$

For the circuit in Figure 4 it can be shown that

$$\frac{1}{\beta} = 1 + \frac{R_2(R_1C_1s + 1)}{R_1(R_2C_2s + 1)} \qquad (5)$$

This may be rearranged to

$$\frac{1}{\beta} = \frac{R_2 + R_1}{R_1} \left[\frac{\tau_a s + 1}{\tau_2 s + 1} \right] \qquad (5a)$$

where $\tau_a = (R_1 \parallel R_2)(C_1 \parallel C_2)$ (5b)

$$= \left[\frac{R_1R_2}{R_1 + R_2} \right] (C_1 + C_2)$$

and $\tau_2 = R_2C_2$ · (5c)

Then, $f_a = \frac{1}{2\pi\tau_a}$ and $f_2 = \frac{1}{2\pi\tau_2}$ · (5d)

For very low frequencies ($f << f_a$), s approaches zero and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1} \cdot \qquad (6)$$

For very high frequencies ($f >> f_2$), s approaches infinity and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{C_1}{C_2} \cdot \qquad (7)$$

The noise voltage spectral density at the output is obtained by multiplying the amplifier's noise voltage spectral density (Figure 5a) times the circuits noise gain (Figure 7). Since both curves are plotted on log-log scales the multiplication can be performed by the addition of the two curves. The result is shown in Figure 8.

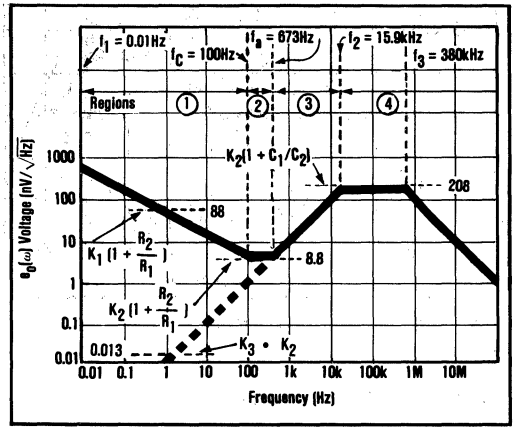


FIGURE 8. Output Noise Voltage Spectral Density.

The total rms noise at the amplifier's output due to the amplifier's internal voltage noise is derived from the $e_o(\omega)$ function in Figure 8 with the following expression:

$$E_{o\ rms} = \sqrt{\int_{-\infty}^{+\infty} e_o^2(\omega)\, d\omega} \qquad (8)$$

It is both convenient and informative to calculate the rms noise using a piecewise approach (region-by-region) for each of the four regions indicated in Figure 8.

Region 1; $f_l = 0.01Hz$ to $f_c = 100Hz$

$$E_{n1\ rms} = K_1 \left(1 + \frac{R_2}{R_1}\right) \sqrt{\ln(f_c/f_l)} \qquad (9)$$

$$= 80nV/\sqrt{Hz} \left(1 + \frac{10^7}{10^8}\right) \sqrt{\ln \frac{100}{0.01}} \qquad (9a)$$

$$= 2.67\mu V$$

This region has the characteristic of 1/f or "pink" noise (slope of -10dB per decade on the log-log plot of $e_n(\omega)$). The selection of 0.01Hz is somewhat arbitrary but it can be shown that for this example there would be only negligible additional contribution by extending f_l several decades lower. Note that $K_1(1 + R_2/R_1)$ is the value of e_o at f = 1Hz.

Region 2; $f_c = 100Hz$ to $f_a = 673Hz$

$$E_{n2\ rms} = K_2 \left(1 + \frac{R_2}{R_1}\right) \sqrt{f_a - f_c} \qquad (10)$$

$$= 8nV/\sqrt{Hz} \left(1 + \frac{10^7}{10^8}\right) \sqrt{673 - 100} \qquad (10a)$$

$$= 0.21\mu V$$

This is a region of "white" noise which leads to the form of equation (10).

Region 3; $f_a = 673Hz$ to $f_2 = 15.9kHz$

$$E_{n3\ rms} = K_2 \cdot K_3 \sqrt{\frac{f_2^3}{3} - \frac{f_a^3}{3}} \qquad (11)$$

$$= 8nV/\sqrt{Hz}\,(1.63 \times 10^{-3}) \sqrt{\frac{(15.9k)^3}{3} - \frac{(673)^3}{3}} \qquad (11a)$$

$$= 15.1\mu V$$

This is the region of increasing noise gain (slope of +20dB/decade on the log-log plot) caused by the lead network formed by the resistance $R_1 \| R_2$ and the capacitance $(C_1 + C_2)$. Note that $K_3 \cdot K_2$ is the value of the $e_o(\omega)$ function for this segment projected back to 1Hz.

Region 4; $f > 15.9kHz$

$$E_{n4\ rms} = K_2 \left(1 + \frac{C_1}{C_2}\right) \sqrt{\left[\frac{\pi}{2}\right] f_3 - f_2} \qquad (12)$$

$$= 8nV/\sqrt{Hz} \left(1 + \frac{25}{1}\right) \sqrt{\left[\frac{\pi}{2}\right] 380k - 15.9k} \qquad (12a)$$

$$= 158.5\mu V$$

This is a region of white noise with a single order rolloff at $f_3 = 380kHz$ caused by the intersection of the $1/\beta$ curve and the open-loop gain curve. The value of 380kHz is obtained from observing the intersection point of Figure 7. The $\pi/2$ applied to f_3 is to convert from a 3dB corner frequency to an effective noise bandwidth.

Current Noise

The output voltage component due to current noise is equal to:

$$E_{ni} = i_n \times Z_2(s) \qquad (13)$$

where $Z_2(s) = R_2 \| X_{C_2}$ (13a)

This voltage may be obtained by combining the information from figures 5 (b) and 6 together with the open loop gain curve of Figure 7. The result is shown in Figure 9 below.

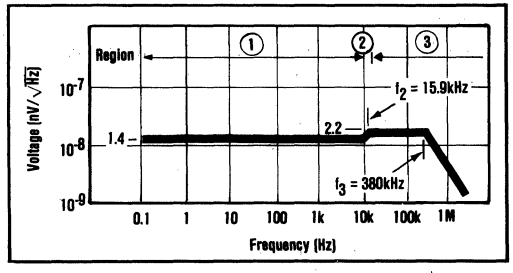


FIGURE 9. Output Voltage Due to Noise Current.

Using the same techniques that were used for the voltage noise:

Region 1; 0.1Hz to 10kHz

$$E_{ni1} = 1.4 \times 10^{-8} \sqrt{10k - 0.1} \quad (14)$$

$$= 1.4\mu V$$

Region 2; 10kHz to 15.9kHz

$$E_{ni2} = 1.4 \times 10^{-12} \sqrt{\frac{(15.9k)^3}{3} - \frac{(10k)^3}{3}} \quad (14a)$$

$$= 1.4\mu V$$

Region 3; f > 15.9kHz

$$E_{ni3} = 2.2 \times 10^{-8} \sqrt{\frac{\pi}{2} 380k - 15.9k} \quad (14b)$$

$$= 16.8\mu V$$

$$E_{ni\ total} = 10^{-6} \sqrt{(1.4)^2 + (1.4)^2 + (16.8)^2} \quad (14c)$$

$$= 16.9\mu V_{rms}$$

Resistor Noise

For a complete noise analysis of the circuit in Figure 4, the noise of the feedback resistor, R_2, must also be included. The thermal noise of the resistor is given by:

$$E_{R\ rms} = \sqrt{4kTRB} \quad (15)$$

K = Boltzmann's constant = 1.38×10^{-23} Joules/°Kelvin
T = Absolute temperature (degrees Kelvin)
R = Resistance (ohms)
B = Effective noise bandwidth (Hz) (ideal filter assumed)

At 25°C this becomes

E_R rms $\cong 0.13 \sqrt{RB}$
E_R rms in μV
R in MΩ
B in Hz

For the circuit in Figure 4

$R_2 = 10^7\Omega = 10M\Omega$

$$B = \frac{\pi}{2}(f_2) = \frac{\pi}{2}\ 15.9k$$

Then

$$E_R\ rms = (411nV/\sqrt{Hz})\sqrt{B}$$

$$= (411nV/\sqrt{Hz})\sqrt{\frac{\pi}{2}\ 15.9kHz}$$

$$= 64.9\mu V\ rms$$

Total Noise

The total noise may now be computed from

$$E_{n\ total} = \sqrt{E_{n1}^2 + E_{n2}^2 + E_{n3}^2 + E_{n4}^2 + E_{nR}^2 + E_{ni}^2} \quad (16)$$

$$= \sqrt{2.67^2 + 0.21^2 + 15.1^2 + 158.5^2 + 64.9^2 + 16.9^2} \quad (16a)$$

$$= \sqrt{7.1 + 0.04 + 228 + 25122 + 4212 + 286} \quad (16b)$$

$$= 173\mu V\ rms$$

Conclusions

Examination of the results in equation (16b) together with the curves in Figure 8 leads to some interesting conclusions. In this example 84% of the noise comes from E_{n4}. From Figure 8 it is seen that this is the area beyond the pole formed by R_2 and C_2.

The E_{n4} contribution could be reduced several ways. The most common method is to increase C_2. This reduces f_2 and the value of K2(1 + C1/C2) (see Figure 8). It also reduces the signal bandwidth (see Figure 6) and the final value of C_2 is normally a compromise between noise gain and necessary signal bandwidth.

It should be noted that increasing C_2 will also affect f_a since f_a is determined by $(C_1 + C_2)$ (see equation (5b)). Normally C_2 is larger than C_1 and f_2 will change more than f_a for a given change in C_2.

The other means of reducing the noise in region 4 involves changing amplifier parameters. For example, the use of a slower amplifier would move the open-loop gain curve to the left and decrease f_3. Of course, reducing the value of K_2, the noise floor, would also reduce the noise in this region.

The second largest component is the resistor noise E_{nR} (14% of the total noise). A lower resistor value decreases resistor noise as a function of $\sqrt{R}$, but it also lowers the desired signal gain as a direct function of R. Thus, lowering R reduces the signal-to-noise ratio at the output which shows that the feedback resistor should be as large as possible. The noise contribution due to R_2 can be decreased by raising the value of C_2 (lowering f_2) but this reduces signal bandwidth.

It is interesting to note that the current noise of the amplifier accounted for only 1% of the total E_n. This is different than would be expected when comparing the current and voltage spectral densities with the size of the feedback resistor. For example, if we define a characteristic value of resistance as

$$R_{characteristic} = \frac{e_n(\omega)}{i_n(\omega)} \text{ at } f = 10kHz \quad (17)$$

$$= \frac{8nV/\sqrt{Hz}}{1.4fA/\sqrt{Hz}}$$

$$= 5.7M\Omega$$

Thus, in simple transimpedance circuits with feedback resistors greater than the characteristic value, the amplifier's current noise would cause more output noise than the amplifier's voltage noise. Based on this and the 10MΩ feedback resistor in the example, the amplifier noise current would be expected to have a higher contribution than the noise voltage. The reason it does not in the example of Figure 4 is that the noise voltage has high gain at higher frequencies (Figure 7) and the noise current does not (Figure 6).

The fourth largest component of total noise comes from E_{n3} (0.8%). Decreasing C_1 will also lower the term $K_2(1 + C_1/C_2)$. In this case, f_2 will stay fixed and f_a will move to the right (i.e., the +20dB/decade slope segment will move

to the right). This can have a significant reduction on noise without lowering the signal bandwidth. This points out the importance of maintaining low capacitance at the amplifier's input in low noise applications.

Shielding and Guarding

The low noise, low bias current and high input impedance of the OPA101/102 are well suited to a number of precision applications. In order to fully benefit from the outstanding specifications of this unit, careful layout, shielding, and guarding are required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the OPA101/102.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the OPA101/102 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pickup.

Unless care is used, leakage currents across printed circuit boards can easily exceed the bias current of the OPA101/102. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the amplifier be wired to a Teflon standoff. If this is not done and instead the OPA101/102 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 10). The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents. In addition, noise pickup is also reduced.

Figures 11, 12, and 13 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two-part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.

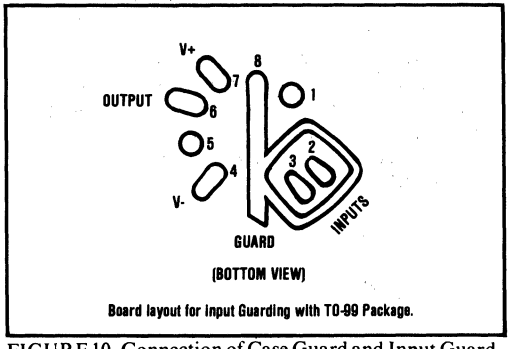


FIGURE 10. Connection of Case Guard and Input Guard.

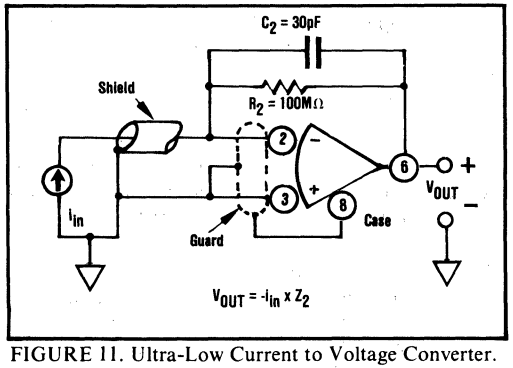


FIGURE 11. Ultra-Low Current to Voltage Converter.

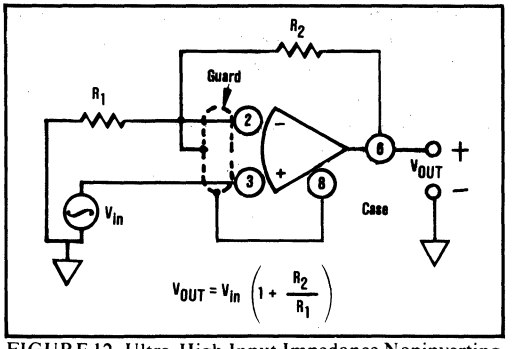


FIGURE 12. Ultra-High Input Impedance Noninverting Circuit.

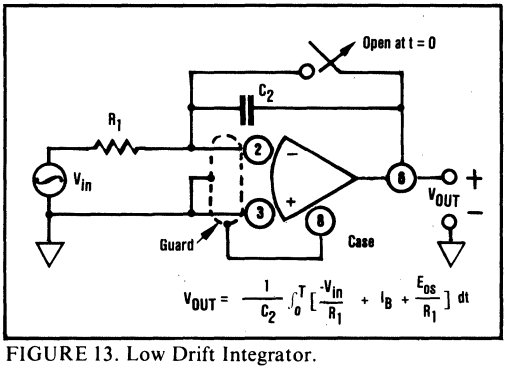


FIGURE 13. Low Drift Integrator.

Thermal Model

Figure 14 is the thermal model for the OPA101/102 where:

T_J = Junction temperature (output load)
T_J* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ_{CA} = Thermal resistance, case-to-ambient

θ_{HS} = Effective thermal resistance of the heat sink

P_{DQ} = Quiescent power dissipation

$|+V_{CC}|\ I_{+QUIESCENT} + |-V_{CC}|\ I_{-QUIESCENT}$

P_{DX} = Power dissipation in the output transistor

$= (V_{OUT} - V_{CC})\ I_{OUT}$

(In a complementary output stage only one output transistor is conducting current at a time.)

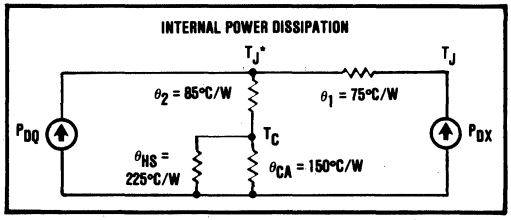


FIGURE 14. OPA101/102 Thermal Model

This model is obviously not the simple one-power source model used with most linear integrated circuits. It is, however, a more accurate model for multichip hybrid integrated circuits where the quiescent power is dissipated in the input stage and the internal power dissipation due to the load is dissipated in a somewhat physically separated output stage.

The model in Figure 14 must be used in conjunction with the OPA101/102's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem: Determine the output transistor junction temperature when the output has its maximum load resistance and is operated at the worst-case output voltage conditions. Assume $V_{CC} = \pm 15$VDC and $T_A = 25°C$.

Maximum P_{DX} occurs where $V_{OUT} = 1/2V_{CC}$. Then

$$P_{DX\ max} = \frac{(V_{CC})^2}{4R_{load}} \qquad (18)$$

$$T_j = T_A + P_{DQ}\,[\theta_2 + (\theta_{HS} \parallel \theta_{CA})] + P_{DX}\,[\theta_1 + \theta_2 + (\theta_{HS} \parallel \theta_{CA})] \qquad (19)$$

where $(\theta_{HS} \parallel \theta_{CA}) = \dfrac{\theta_{HS}\theta_{CA}}{\theta_{HS} + \theta_{CA}} = 90°C/W$

Substituting appropriate values yields

$$T_j = 25° + (30V \times 8mA)[85°C/W + 90°C/W] + \frac{(15V)^2}{4 \times 1k\Omega}\,[75°C/W + 85°C/W + 90°C/W]$$

$$= 25°C + 42°C + 14°C = T_A + 56°C$$

$$= 81°C$$

The conclusion is that under a worst-case output voltage condition and with a 1kΩ load the junction temperature rise is 56°C above ambient. Thus, under these conditions, the device could be operated in an ambient up to 119°C without exceeding the 175°C junction temperature rating.

A similar analysis for conditions of the output short-circuited to ground where

$$P_{DX\ SS} = V_{CC}\ I_{(output\ limit)} \qquad (20)$$

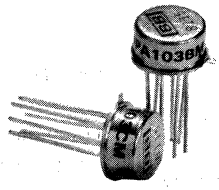
shows that the maximum junction temperature rating of 175°C is exceeded. Thus, the output should not be shorted to ground for sustained periods of time.

HEAT SINK

The heat sink used on the OPA101/102 should not be removed. It has the effect of reducing the package thermal resistance from 150°C/W to about 90°C per watt. Removing the heat sink would naturally increase the junction temperature of the amplifier which would in turn raise the input bias current. The change in thermal resistance also affects the noise performance. Removing the heat sink would increase the noise in the 1/f region.

BURR-BROWN®

OPA103



Low Drift - Low Bias Current FET Input OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, 1pA, max
- HIGH INPUT IMPEDANCE, $10^{13}\Omega$
- ULTRA-LOW DRIFT, $2\mu V/°C$, max
- LOW OFFSET VOLTAGE, 0.25mV, max
- LOW QUIESCENT CURRENT, 1.5mA, max
- HERMETICALLY SEALED TO-99 PACKAGE

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  - photo current detectors
  - pH electrodes
  - biological probes/transducers

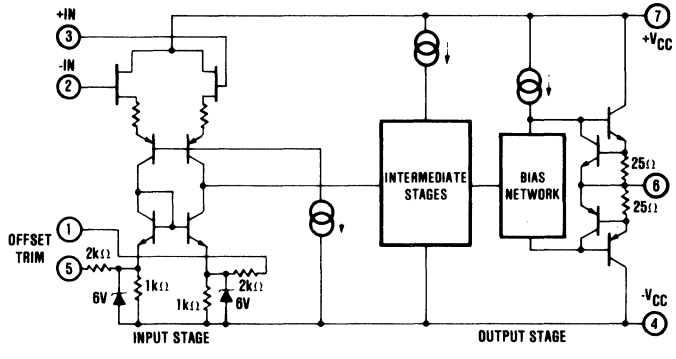
DESCRIPTION

The OPA103 is a precision low bias current operational amplifier. Guaranteed low initial offset voltage (0.25mV, max) and associated drift versus temperature ($2\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. This feature, and guaranteed low bias current (1pA, max), allow greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA103 include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA103 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



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PDS-444A

SPECIFICATIONS

ELECTRICAL

At T_A = 25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL	OPA103AM			OPA103BM			OPA103CM			OPA103DM			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OPEN-LOOP GAIN, DC, V_{OUT} = ±10V													
Rated Load, $R_L \geq 2k\Omega$	100	106		*	*		*	*		*	*		dB
$R_L \geq 10k\Omega$		112			*			*			*		dB
T_A = -25°C to +85°C, $R_L \geq 2k\Omega$	94	100		*	*		*	*		*	*		dB
RATED OUTPUT													
Voltage at R_L = 2kΩ, T_A = -25°C to +85°C	±10	±12		*	*		*	*		*	*		V
R_L = 10kΩ, T_A = -25°C to +85°C	±12	±13		*	*		*	*		*	*		V
Current, T_A = -25°C to +85°C	±5	±10		*	*		*	*		*	*		mA
Output Impedance		3			*			*			*		kΩ
Load Capacitance(1)	500	1000		*	*		*	*		*	*		pF
Short Circuit Current	10	25		*	*		*	*		*	*		mA
FREQUENCY RESPONSE													
Unity Gain, Small Signal		1			*			*			*		MHz
Full Power Response	14	20		*	*		*	*		*	*		kHz
Slew Rate	0.9	1.3		*	*		*	*		*	*		V/μsec
Settling Time (0.1%)		9			*			*			*		μsec
Settling Time (0.01%)		20			*			*			*		μsec
Overload Recovery(2), 50% overdrive		4	15		*	*		*	*		*	*	μsec
INPUT OFFSET VOLTAGE													
Initial Offset, T_A = +25°C		±200	±500		±200	±500		±100	±250		±100	±250	μV
vs Temperature, T_A = -25°C to +85°C		±15	±25		±10	±15		±3	±5		±1	±2	μV/°C
vs Supply Voltage, T_A = -25°C to +85°C		±20	±200		*	*		*	*		*	*	μV/V
vs Time		±20			*			*			*		μV/mo
INPUT BIAS CURRENT(3)													
Initial Bias, T_A = +25°C			-2			-1			-1			-1	pA
vs Supply Voltage		0.005			*			*			*		pA/V
INPUT DIFFERENCE CURRENT													
Initial Difference, T_A = +25°C		±0.3			±0.2			±0.2			±0.2		pA
INPUT IMPEDANCE													
Differential		10^{13} || 0.8			*			*			*		Ω || pF
Common-mode		10^{14} || 0.6			*			*			*		Ω || pF
INPUT NOISE													
Voltage, f_o = 10Hz		55			*			*			*		nV/√Hz
f_o = 100Hz		35			*			*			*		nV/√Hz
f_o = 1kHz		30			*			*			*		nV/√Hz
f_o = 10kHz		25			*			*			*		nV/√Hz
f_B = 0.1Hz to 10Hz		3.0			*			*			*		μV, p-p
Current, f_B = 0.1Hz to 10Hz		0.01			*			*			*		pA, p-p
f_B = 10Hz to 10kHz		0.03			*			*			*		pA, rms
f_o = 1kHz		0.6			*			*			*		fA/√Hz
INPUT VOLTAGE RANGE													
Differential	±20			*			*			*			V
Common-mode, T_A = -25°C to +85°C	±10	±12		*	*		*	*		*	*		V
Common-mode Rejection, V_{IN} = ±10V	76	86		*	*		*	*		*	*		dB
Maximum Safe Input Voltage		±Vs			*			*			*		V
POWER SUPPLY													
Rated Voltage		±15			*			*			*		VDC
Voltage Range, derated performance	±5		±20	*		*	*		*	*		*	VDC
Current, quiescent, T_A = -25°C to +85°C		1.0	1.5		*	*		*	*		*	*	mA
TEMPERATURE RANGE (ambient)													
Specification	-25		+85	*		*	*		*	*		*	°C
Operating	-55		+125	*		*	*		*	*		*	°C
Storage	-65		+150	*		*	*		*	*		*	°C
θ junction - ambient		235			*			*			*		°C/W

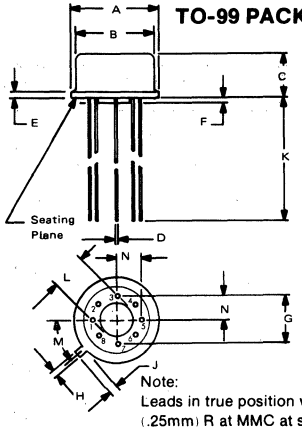
*Specifications same as for OPA103AM.

NOTES:

1. Stability guaranteed with load capacitance ≤ 500pF.
2. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
3. Bias current is tested and guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperature the bias current doubles every +10°C.

MECHANICAL

TO-99 PACKAGE



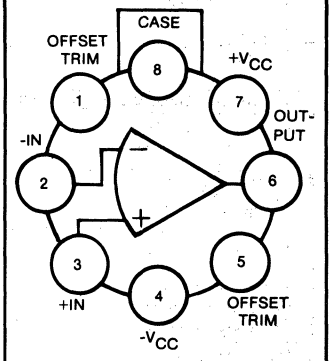
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Weight: 1 gram

Note:
Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.

The TO-99 can and leads are bright acid tin plated.
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

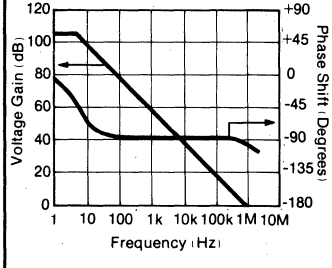
CONNECTION DIAGRAM



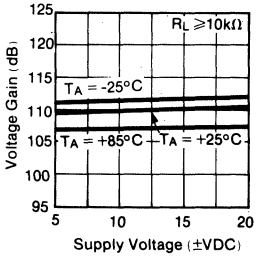
(TOP VIEW)

TYPICAL PERFORMANCE CURVES

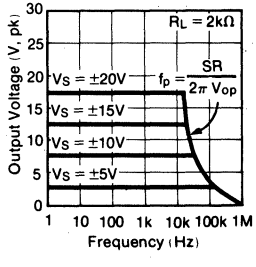
OPEN-LOOP FREQUENCY RESPONSE



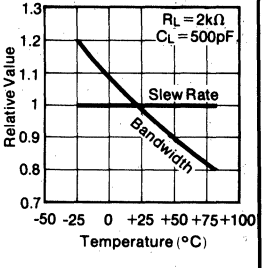
VOLTAGE GAIN



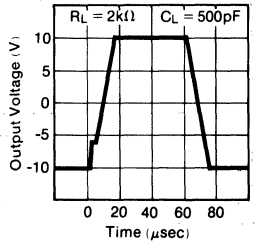
OUTPUT VOLTAGE vs FREQUENCY



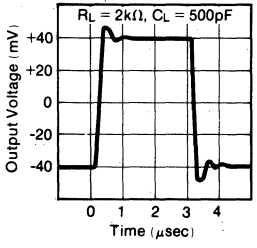
FREQUENCY CHARACTERISTICS



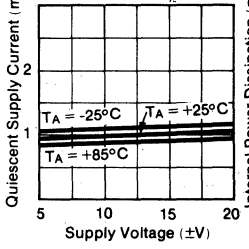
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



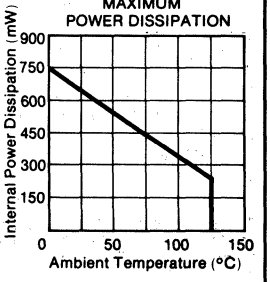
TRANSIENT RESPONSE



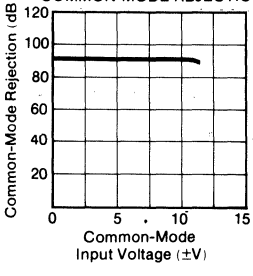
QUIESCENT SUPPLY CURRENT



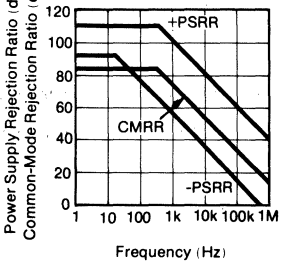
MAXIMUM POWER DISSIPATION



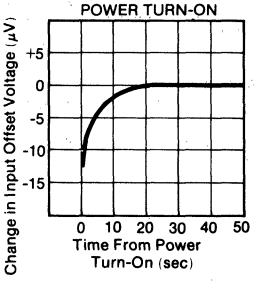
COMMON-MODE REJECTION



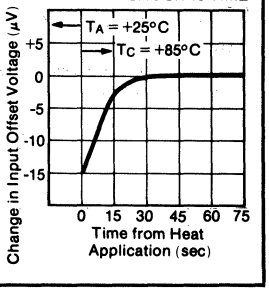
CMRR AND PSRR



STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



INPUT OFFSET VOLTAGE vs THERMAL SHOCK vs TIME



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the OPA103. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA103 is approximately 20 seconds (see Typical Performance Curves).

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the OPA103 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA103.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA103. To avoid leakage problems, it is recommended that the signal input lead of the OPA103 be wired to a Teflon standoff. If the OPA103 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard. The resistor R_3 shown in Figure 1 is optional. It may be used to compensate effects of very large source resistances. However, note that its use would also increase the noise due to the thermal noise of R_3.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA103 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C, for every 100μV of offset adjustment.

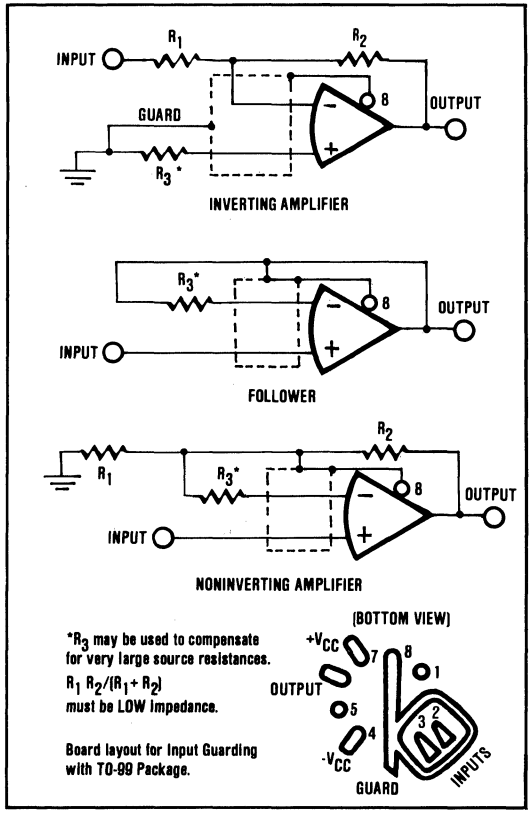


FIGURE 1. Connection of Input Guard.

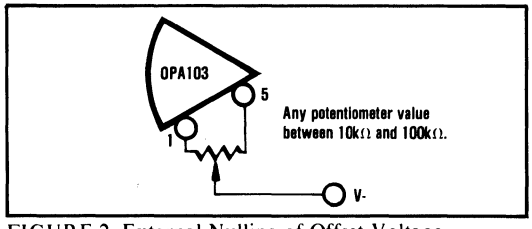


FIGURE 2. External Nulling of Offset Voltage.

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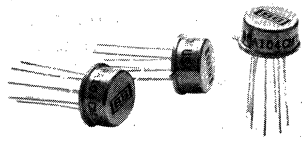
OPA104



Ultra-Low Bias Current Low Drift FET Input OPERATIONAL AMPLIFIER

FEATURES

- SPECIFICATIONS GUARANTEED OVER TEMPERATURE
- ULTRA-LOW BIAS CURRRENT, 75fA, max
- HIGH INPUT IMPEDANCE, $10^{15}\Omega$
- LOW DRIFT, $10\mu V/°C$, max
- LOW OFFSET VOLTAGE, 0.5mV, max
- LOW QUIESCENT CURRENT, 1.5mA, max

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  - photo current detectors
  - pH electrodes
  - biological probes/transducers

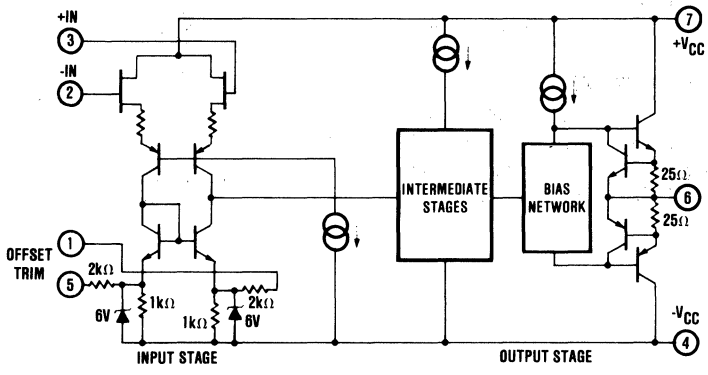
DESCRIPTION

The OPA104 is a precision low bias current operational amplifier. Guaranteed low initial offset voltage (0.5mV, max) and associated drift versus temperature ($10\mu V$ °C, max) is achieved by laser-adjusting the amplifier during manufacturing. The low offset, in addition to the guaranteed low bias current (75fA, max), allows greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA104 include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or ambient temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidently shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA104 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



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PDS-451

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

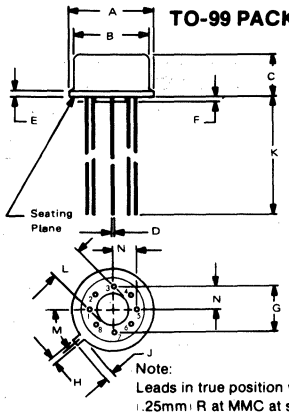
MODEL	OPA104AM			OPA104BM			OPA104CM			
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OPEN-LOOP GAIN, DC, V_{OUT} = ±10V										
Rated Load, $R_L \geq 2k\Omega$	100	106		•	•		•	•		dB
$R_L \geq 10k\Omega$	106	112		•	•		•	•		dB
T_A = -25°C to +85°C, $R_L \geq 2k\Omega$	92	100		•	•		•	•		dB
RATED OUTPUT										
Voltage at R_L = 2kΩ, T_A = -25°C to +85°C	±10	±12		•	•		•	•		V
R_L = 10kΩ, T_A = -25°C to +85°C	±12	±13		•	•		•	•		V
Current T_A = -25°C to +85°C	±5	±10		•	•		•	•		mA
Output Impedance		3			•			•		kΩ
Load Capacitance(1)	500	1000		•	•		•	•		pF
Short Circuit Current	10	25		•	•		•	•		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			•			•		MHz
Full Power Response	25	35		•	•		•	•		kHz
Slew Rate	1.6	2.2		•	•		•	•		V/µsec
Settling Time (0.1%), A_V = -1, V_O = 0 to ±10V		6			•			•		µsec
Settling Time (0.01%), A_V = -1, V_O = 0 to ±10V		18			•			•		µsec
Overload Recovery(2), 50% overdrive		4	15		•	•		•	•	µsec
INPUT OFFSET VOLTAGE										
Initial Offset, T_A = +25°C		±200	±1000		±200	±500		±200	±500	µV
vs Temperature, T_A = -25°C to +85°C		±15	±25		±10	±15		±5	±10	µV/°C
vs Supply Voltage, T_A = +25°C		±10	±100		•	•		•	•	µV/V
vs Supply Voltage, T_A = -25°C to +85°C		±20	±150		•	•		•	•	µV/V
INPUT BIAS CURRENT(3)										
Initial Bias, T_A = +25°C			-300			-150			-75	fA
vs Supply Voltage		1				•			•	fA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, T_A = +25°C		±80			±80			±40		fA
INPUT IMPEDANCE										
Differential		$10^{14} \parallel 0.5$			•			•		Ω || pF
Common-mode		$10^{15} \parallel 1.0$			•			•		Ω || pF
INPUT NOISE										
Voltage, f_o = 10Hz		75			•			•		$nV/\sqrt{Hz}$
f_o = 100Hz		55			•			•		$nV/\sqrt{Hz}$
f_o = 1kHz		35			•			•		$nV/\sqrt{Hz}$
f_o = 10kHz		35			•			•		$nV/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz		6			•			•		µV, p-p
Current, f_B = 0.1Hz to 10Hz		3			•			•		fA, p-p
f_B = 10Hz to 10kHz		10			•			•		fA, rms
f_o = 1kHz		0.25			•			•		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE										
Differential	±20			•			•			V
Common-mode, T_A = -25°C to +85°C	±10	±12		•	•		•	•		V
Common-mode Rejection at V_{IN} = ±10V	66	76		•	•		80	90		dB
Maximum Safe Input Voltage		±Vs			•			•		V
POWER SUPPLY										
Rated Voltage		±15			•			•		VDC
Voltage Range, derated performance	±5		±20	•		•	•		•	VDC
Current, quiescent T_A = -25°C to +85°C		1.0	1.5		•	•		•	•	mA
TEMPERATURE RANGE (ambient)										
Specification	-25		+85	•		•	•		•	°C
Operating	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C
θ junction - ambient		235			•			•		°C/W

*Specifications same as for OPA104AM.

NOTES:
1. Stability guaranteed with load capacitance ≤ 500pF.
2. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
3. Bias current is tested and guaranteed after 5 minutes of operation T_A = +25°C. For higher temperature the bias current doubles approximately every +10°C.

MECHANICAL

TO-99 PACKAGE



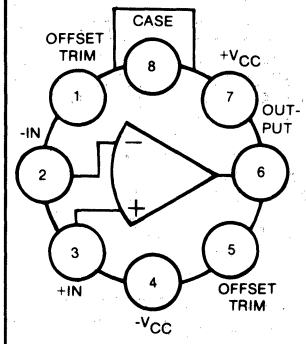
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Weight: 1 gram

Note:
Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package.

The TO-99 can and leads are bright acid tin plated.
Pin material and plating composition conform to Method 2003 (solderability of MIL-STD-883 (except paragraph 3.2).

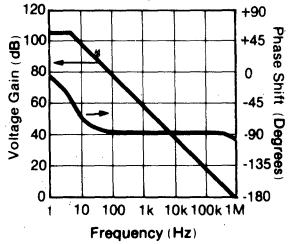
CONNECTION DIAGRAM



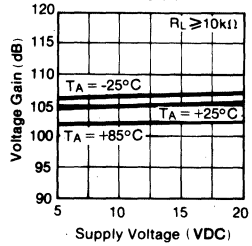
(TOP VIEW)

TYPICAL PERFORMANCE CURVES

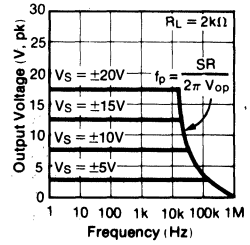
OPEN-LOOP FREQUENCY RESPONSE



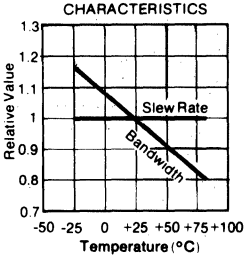
VOLTAGE GAIN



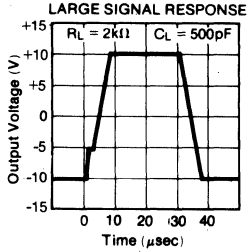
OUTPUT VOLTAGE vs FREQUENCY



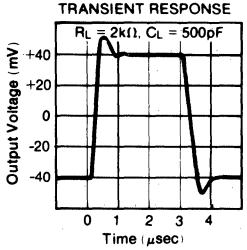
FREQUENCY CHARACTERISTICS



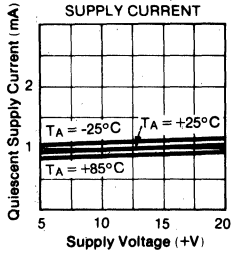
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



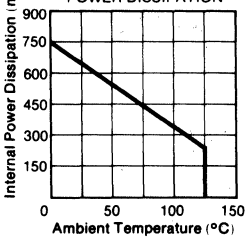
TRANSIENT RESPONSE



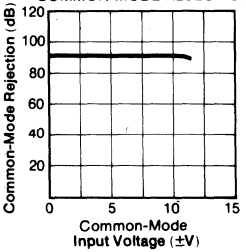
QUIESCENT SUPPLY CURRENT



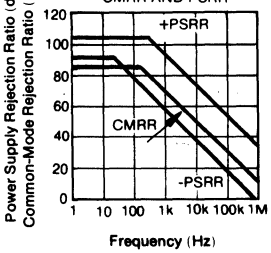
MAXIMUM POWER DISSIPATION



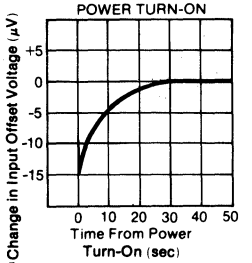
COMMON-MODE REJECTION



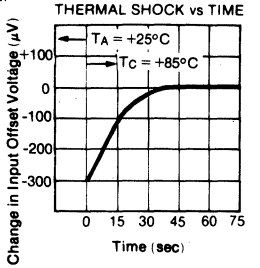
CMRR AND PSRR



STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



INPUT OFFSET VOLTAGE vs THERMAL SHOCK vs TIME



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the OPA104. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA104 is approximately 20 seconds (see Typical Performance Curves).

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the OPA104 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA104.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA104. To avoid leakage problems, it is recommended that the signal input lead of the OPA104 be wired to a Teflon standoff. If the OPA104 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA104 has a low initial offset voltage (500μV), some applications may require external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C, for every 100μV of offset adjustment.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

CR1 is a PIN photodiode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{in} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 (0.5pF to 2pF) is what would be typically required to compensate for the pole generated by the capacitance at the input node. A larger value of C_2 could be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

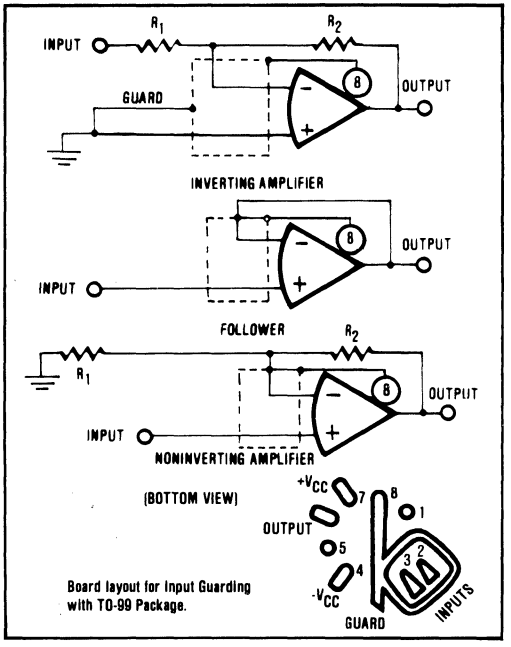


FIGURE 1. Connection of Input Guard.

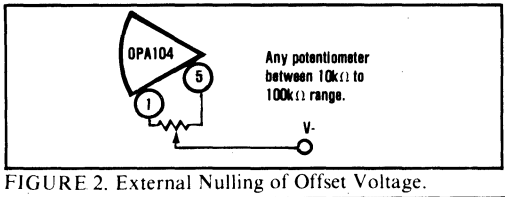


FIGURE 2. External Nulling of Offset Voltage.

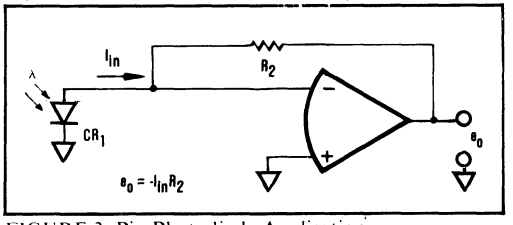


FIGURE 3. Pin Photodiode Application.

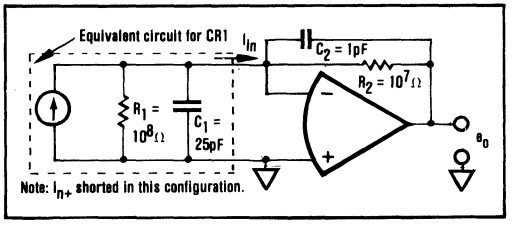


FIGURE 4. Model of Photodiode Application.

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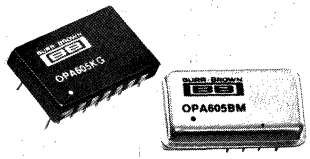
OPA605



Wideband - Fast Settling OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING - 500nsec max to 0.1%
- WIDE BANDWIDTH - 200MHz Gain - Bandwidth Product
- FAST SLEWING - 300V/μsec slew rate, $A_{CL} \geq 50$
- LARGE OUTPUT CURRENT - ±30mA min at ±10V
- HIGH GAIN - 80dB min at ±30mA output
- LOW VOLTAGE OFFSET AND DRIFT - 500μV max, 5μV/°C max

APPLICATIONS

- PULSE AMPLIFIERS
- FAST D/A CONVERTERS
- LINE DRIVERS
- WAVEFORM GENERATORS
- HIGH SPEED TEST EQUIPMENT

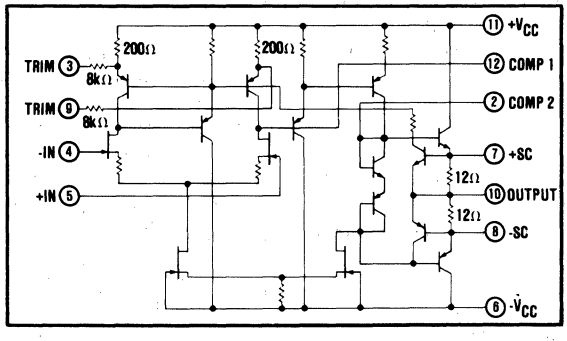
DESCRIPTION

The OPA605 is designed to offer a well balanced set of both AC and DC specifications. Versatility in fast settling, wideband and steady state AC applications is provided by the use of a single external compensation capacitor. This allows the user to optimize speed and stability for any particular application.

The full ±30mA guaranteed minimum output current (at ±10V) allows the user to realize the high speed features of the OPA605. Unlike most integrated circuit wideband amplifiers additional current booster circuitry is not needed for most applications.

The 500nsec max to 0.1% settling time specification is guaranteed with a load of 500Ω and 100pF. Also the open-loop gain is guaranteed at the full ±30mA output.

In addition to the excellent wideband and fast settling characteristics, the OPA605 also offers outstanding DC performance. Offset voltages are as low as 500μV max and offset voltage drift versus temperature of only 5μV/°C max is available.



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PDS-443

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL		OPA605H/OPA605A			OPA605J/OPA605B			OPA605K/OPA605C			
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OPEN-LOOP GAIN, DC											
Full Load	V_O = ±10V; R_L = 330Ω	80	96		*	*		*	*		dB
No Load	V_O = ±10V; $R_L \geq$ 10kΩ		102			*			*		dB
RATED OUTPUT											
Voltage	I_O = ±30mA	±10	±12		*	*		*	*		V
Current	V_O = ±10V	±30	±50		*	*		*	*		mA
Output Resistance	Open Loop		200			*			*		Ω
Short Circuit Current	Internal Limits(1)	±30	±50	±80	*	*	*	*	*	*	mA
Capacitive Load(2)	A_{CL} = -1, C_C = 20pF	500			*			*			pF
DYNAMIC RESPONSE											
Gain-Bandwidth Product											
A_{CL} = 1000, C_C = 0			200			*			*		MHz
A_{CL} = -1, C_C = 20pF			20			*			*		MHz
Slew Rate	R_L = 330Ω, V_O = 0 to +10V,										
$A_{CL} \geq$ 50, C_C = 0	0 to -10V		300			*			*		V/μsec
A_{CL} = -1, C_C = 20pF		80	94		*	*		*	*		V/μsec
Full Power Bandwidth	R_L = 330Ω, V_O = ±10V,	1.3	1.5		*	*		*	*		MHz
	A_{CL} = -1, C_C = 20pF										
Settling Time, A_V = -1(3)	C_C = 20pF, R_L = 500Ω,										
	C_L = 100pF, V_O = 0 to +10V,										
	0 to -10V										
ε = 1%			200			*			*		nsec
ε = 0.1%			300	500		*	*		*	*	nsec
ε = 0.01%			400			*			*		nsec
Small-Signal Overshoot	A_V = -1, C_C = 20pF, R_L = 500Ω		0	20		*	*		*	*	%
	C_L = 100pF										
INPUT OFFSET VOLTAGE											
Initial Offset	T_A = +25°C		±0.25	±1.0		*	±0.5		*	±0.5	mV
vs Temperature	T_L to T_H			±25			±10			±5	μV/°C
vs Supply Voltage			±30	±200		*	*		*	*	μV/V
Adjustment Range(4)	Circuit in		±9			*			*		mV
	"Connection Diagram"										
INPUT BIAS CURRENT											
Initial Bias	T_A = +25°C, V_{CM} = 0		-10	-35		*	*		*	*	pA
vs Temperature	T_L to T_H		Note 5			*			*		
vs Supply Voltage			0.2			*			*		pA/V
vs V_{CM}			Note 6			*			*		
INPUT DIFFERRENCE CURRENT											
Initial Difference	T_A = +25°C, V_{CM} = 0		±2			*			*		pA
vs Temperature			Note 5			*			*		
vs Supply Voltage			0.05			*			*		pA/V
VOLTAGE NOISE DENSITY $R_S \leq$ 100Ω											
	f_O = 10Hz		80			*			*		nV/√Hz
	f_O = 100Hz		30			*			*		nV/√Hz
	f_O = 1kHz		20			*			*		nV/√Hz
	f_O = 10kHz		12			*			*		nV/√Hz
	f_O = 100kHz		12			*			*		nV√Hz
INPUT IMPEDANCE											
Differential											
Resistance			10^{11}			*			*		Ω
Capacitance			3			*			*		pF
Common-Mode											
Resistance			10^{11}			*			*		Ω
Capacitance			3			*			*		pF
INPUT VOLTAGE RANGE											
Common-Mode Voltage	Linear Operation										
Range		±10	±12		*	*		*	*		V
Common-Mode Rejection		70	90		80	90		80	90		dB
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range	Derated Performance	±5		±18	*		*	*		*	VDC
Current, Quiescent			±7.2	±9		*	*		*	*	mA
TEMPERATURE RANGE											
Specification											
H, J, K Grades	T_L to T_H	0		+70	*		*	*		*	°C
A, B, C Grades	T_L to T_H	-25		+85	*		*	*		*	°C
Operating	Derated Performance	-55		+125	*		*	*		*	°C
Storage		-65		+150	*		*	*		*	°C

NOTES:
*Specifications same as for OPA605H/OPA605A. 1. Current limit may be increased with external resistors. 2. Allowable capacitive load depends on several factors. See Compensation section. 3. Settling Time measured in circuit of Figure 4. 4. Adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted. 5. Doubles approximately every 8.5°C 6. See Typical Performance Curves.

ABSOLUTE MAXIMUM RATINGS

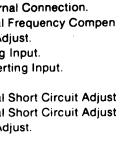
Supply	±20VDC
Internal Power Dissipation	(1)
Differential Input Voltage(2)	±20VDC
Input Voltage, Either Input(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-Circuit Duration(3)	Continuous
Junction Temperature	+175°C

NOTES:
1. Package must be derated according to details in the Applications Information section.
2. For supply voltages less than ±20VDC, the absolute maximum input is equal to the supply voltage.
3. Short circuit to ground only. See Short Circuit Protection discussion in the Application Information section.

PIN CONFIGURATION

1. No Internal Connection.
2. Optional Frequency Compensation.
3. Offset Adjust.
4. Inverting Input.
5. Noninverting Input.
6. -Vcc.
7. Optional Short Circuit Adjust.
8. Optional Short Circuit Adjust.
9. Offset Adjust.
10. Output
11. +Vcc.
12. Frequency Compensation.
13. No Internal Connection*.
14. No Internal Connection.

*Case on metal package

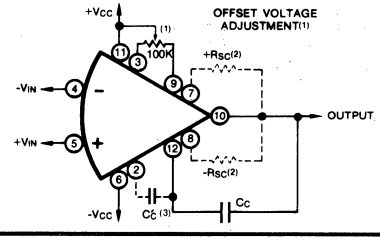


Bottom View

Pin numbers shown for reference only. Numbers are not marked on package.

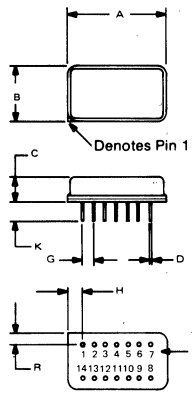
Pin 13 is case on metal unit.

CONNECTION DIAGRAM



NOTES:
1. Offset voltage adjustment affects voltage drift vs temperature by approximately ±0.3μV/°C for each 100μV of offset adjusted.
2. Optional resistors to increase current limits. See Application Information.
3. Optional frequency compensation. See Applications Information.

MECHANICAL "M" PACKAGE

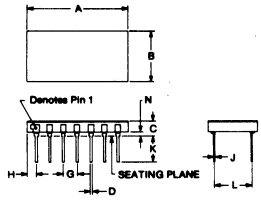


NOTES:
1. Leads in true position within .010" (.25mm) R at MMC at seating plane.
2. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

MECHANICAL "G" PACKAGE



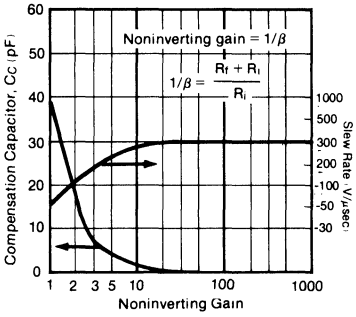
NOTES:
1. Leads in true position within .010" (.25mm) R at MMC at seating plane.
2. Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.770	.810	19.56	20.57
B	.480	.500	12.19	12.70
C	.155	.215	3.94	5.46
D	.016	.020	.41	.51
G	.100 BASIC		2.54 BASIC	
H	.080	.110	2.03	2.79
J	.009	.012	.23	.30
K	.150	.210	3.81	5.33
L	.300 BASIC		7.62 BASIC	
N	.015	.035	.38	.89

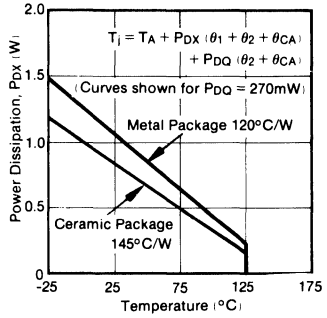
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)

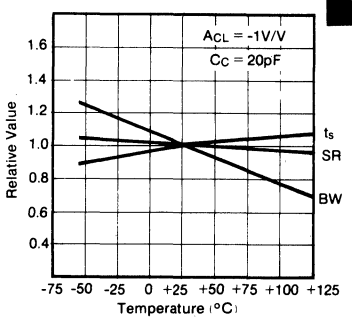
COMPENSATION CAPACITANCE AND SLEW RATE VS NONINVERTING GAIN



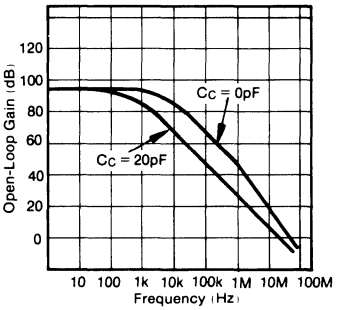
POWER DERATING



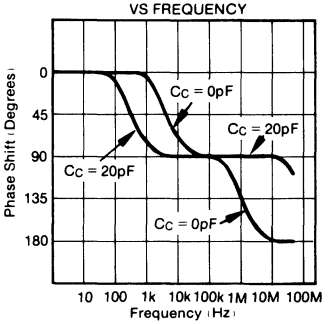
AC PARAMETERS VS TEMPERATURE



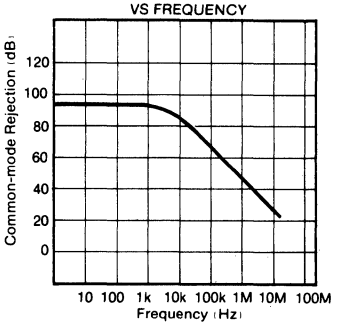
OPEN-LOOP GAIN VS FREQUENCY



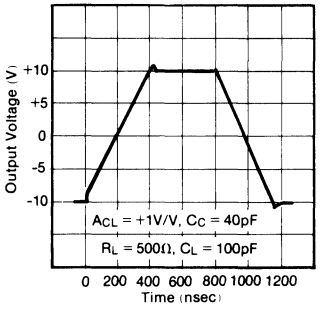
OPEN-LOOP PHASE SHIFT VS FREQUENCY



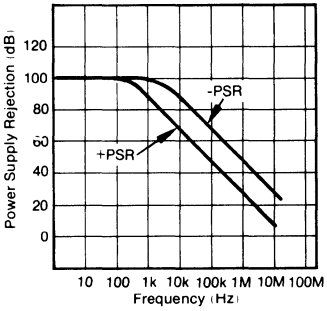
COMMON-MODE REJECTION VS FREQUENCY



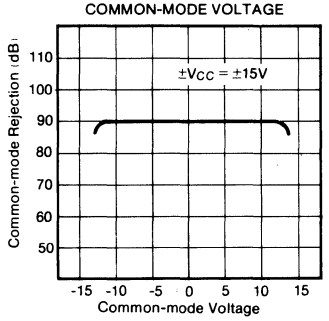
LARGE SIGNAL TRANSIENT RESPONSE



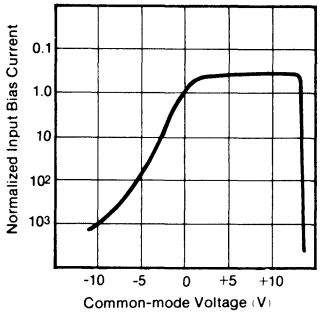
POWER SUPPLY REJECTION VS FREQUENCY



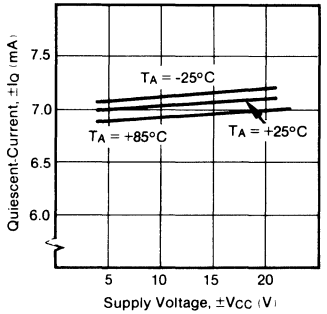
COMMON-MODE REJECTION VS COMMON-MODE VOLTAGE



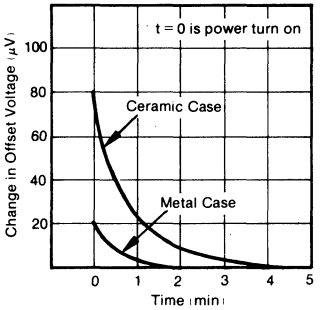
BIAS CURRENT VS COMMON-MODE VOLTAGE



QUIESCENT CURRENT VS SUPPLY VOLTAGE



OFFSET VOLTAGE VS TIME



APPLICATION INFORMATION

SLEW RATE

Slew rate is a large signal output parameter. It is primarily dependent on the compensation capacitor value (C_C) and has almost no dependence on changes in the closed loop gain or bandwidth. Typical values of slew rate versus compensation capacitor value are shown in the Typical Performance Curves. Decreasing the compensation capacitance increases the slew rate but reduces the frequency stability of the closed-loop circuit. Stray circuit capacitances may appear as added compensation to the amplifier. Therefore, stray capacitances should be minimized to avoid limiting slew rate performance.

BANDWIDTH

The closed-loop bandwidth is a small signal parameter. It is dependent on the open-loop frequency response of the op amp (which is determined by the value of the compensation capacitor, C_C) and the external closed-loop circuitry applied to the amplifier. Requirements for increased bandwidth and more frequency stability result in opposing constraints on the circuitry and generally the final selection of circuit values represents a compromise between the two needs.

SETTLING TIME

Settling time is defined as the total time required, measured from the input signal step, for the output to settle to within the specified error band around the final value. The error band is expressed as a percent of the full scale output voltage (10V) and the output transition is from 0V to +10V or 0V to -10V.

Settling time depends on slew rate (discussed above) and the time to reach the final value after the slew portion of the transition is complete. The latter is a function of the closed-loop bandwidth (discussed above) and the closed-loop gain. Thus, settling time is a function of both the open-loop frequency compensation (value of C_C) and the particular closed-loop circuit configuration. The best settling time is generally obtained at low gains.

COMPENSATION

The OPA605 uses external frequency compensation which allows the user to optimize slew rate, bandwidth and settling time for a particular application. As mentioned previously, compensation is normally a compromise between the desired speed and the necessary frequency stability - the higher the speed the lower the value of C_C and the less stable the circuit. Several of the Typical Performance Curves provide information to aid in the selection of the correct value of compensation capacitor. In addition, several typical circuits show recommended compensation in different applications.

The value of compensation capacitor required for stability is a function of the amount of negative feedback used in the particular application. This is characterized as $1/\beta$, where β is the "feedback factor". $1/\beta$ is also equal to the gain in noninverting configurations (see figures 2 and 3).

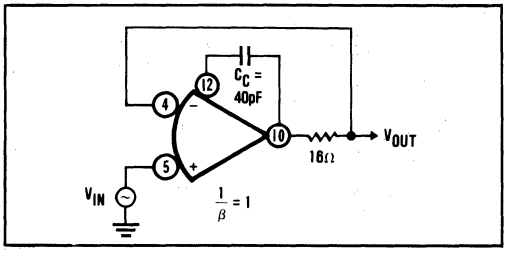


FIGURE 1. Unity Gain Follower.

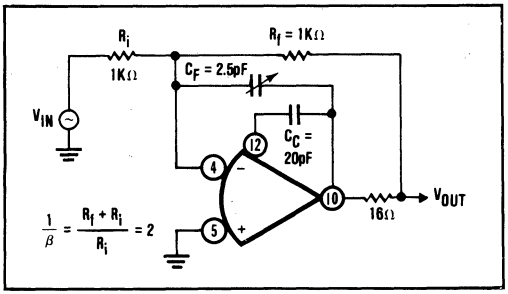


FIGURE 2. Unity Gain Inverting.

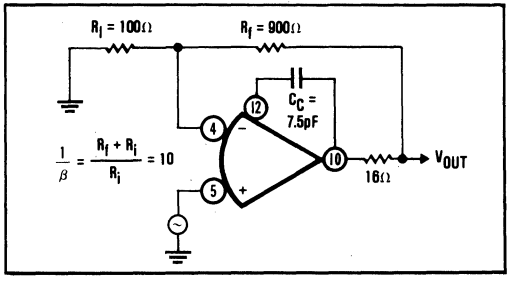


FIGURE 3. Gain of +10V.

The OPA605 may be compensated in either one of two ways. In the primary compensation method, C_C is connected between pins 10 and 12. Alternately the amplifier may be compensated with C_C' between pins 12 and 2 (see Connection Diagram). Normally the use of C_C is recommended. The use of C_C' will give lower output impedance at higher frequencies. This can be an advantage in some applications, but the effects are subtle and must be determined empirically.

Improved stability with larger capacitive loads may be obtained by connecting a small resistor (a value of 16Ω is recommended) in series with the output (see figures 2 through 4).

Flat high frequency closed-loop frequency response may be preserved and any high frequency peaking reduced by connecting a small capacitor (C_F in the examples) in parallel with the feedback resistor. This capacitor will compensate for the high frequency closed-loop transfer function zero formed by the capacitance at the amplifier's input and the input and feedback resistors. C_F may be a trimmer capacitor, a fixed capacitor or a planned printed circuit board capacitance. Typical values range from 0pF to 5pF.

WIRING PRECAUTIONS

Of all the wiring precautions, grounding is the most important. A good ground plane and good grounding practices should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns.

If point-to-point wiring is used (no ground plane), single point grounding should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins.

All printed circuit board conductors should be wide to provide low resistance, low inductance connections, and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitance should be minimized especially at high impedance nodes. Pin 4, the inverting input is especially sensitive to capacitance and all connections to that point must be short.

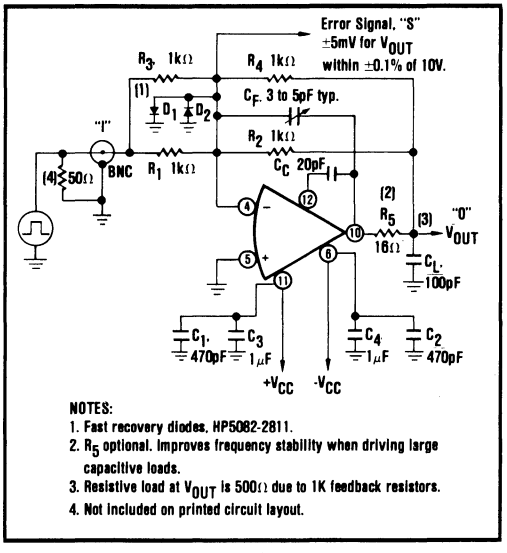


FIGURE 4. Dynamic Test Circuit.

Input and feedback resistors should be kept as small in value as practical; values less than 5.6kΩ are recommended. This will minimize performance limitations caused by the time constants formed by these resistors and circuit capacitances.

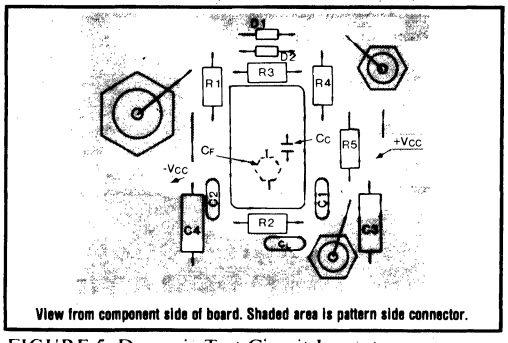


FIGURE 5. Dynamic Test Circuit Layout.

SHORT CIRCUIT PROTECTION

Short circuit protection to common is provided by internal current limiting resistors. (Output shorts to either supply can destroy the device.) The current limits may be increased by paralleling the internal resistors with external resistors, R_{EXT} connected between pins 7 and 10 and pins 8 and 10. The short-circuit current is then $I_{SC} \approx 0.05 + 0.6/R_{EXT}$ (in amps). The power derating constraints must be observed when modifying the current limits. Details are given by the thermal model.

THERMAL MODEL

Figure 6 is the thermal model for the OPA605 where:

T_J = Junction temperature (output load)
T_J^* = Junction temperature (no load)
T_C = Case temperature
T_A = Ambient temperature
θ_{CA} = Thermal resistance, case-to-ambient
P_{DQ} = Quiescent power dissipation
$= |+V_{CC}| I_{Q\,(+)} + |-V_{CC}| I_{Q\,(-)}$
P_{DX} = Power dissipation in the output transistor
$= (V_{OUT} - V_{CC}) I_{OUT}$

(In a complementary output stage only one output transistor is conducting current at a time.)

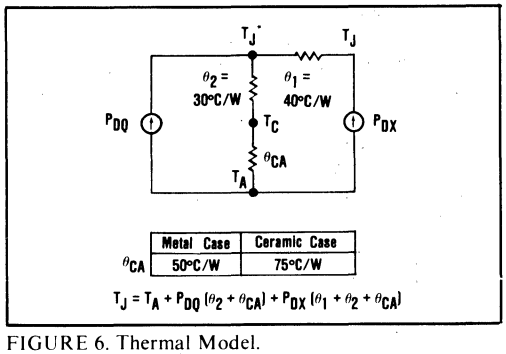
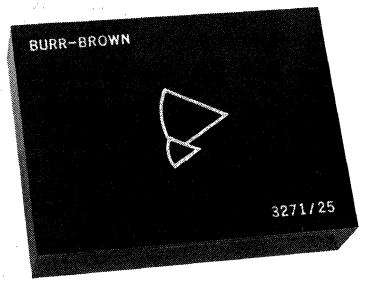


FIGURE 6. Thermal Model.

This model yields a Power Derating curve which is a function of P_{DQ}. See Typical Performance Curves.

BURR-BROWN®



3271/25

High Voltage - Chopper-stabilized OPERATIONAL AMPLIFIERS

FEATURES

- LOW DRIFT
- OPERATES OVER WIDE SUPPLY RANGE
- HIGH OUTPUT VOLTAGE UP TO 110V
- SMALL, ENCAPSULATED PACKAGE
- ALL SOLID-STATE DESIGN

DESCRIPTION

The Model 3271/25 is a high voltage, chopper-stabilized operational amplifier in a small, encapsulated package. The module can be soldered directly on a circuit board, or may be plugged into a 1500MC connector for chassis mounting. The epoxy encapsulation insures ruggedness and resistance to environmental stresses, while the all-solid-state design, including self-contained MOSFET chopper and driver, guarantees reliable operation.

The amplifier is designed for operation on external supplies ranging anywhere from ±60VDC to ±120VDC. Output voltage range depends on the supply voltages. A low-noise chopping technique insures ultra-low DC drift as a function of temperature and time, while eliminating the noise spikes usually associated with chopper amplifiers.

The 3271/25 has input protection up to the value of supply voltage. The output stage may be shorted to common without damage to the amplifier. These features are particularly desirable when the amplifier is used in a patchable simulator.

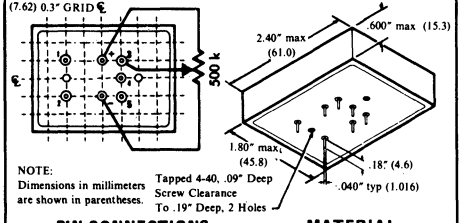
The open-loop gain exhibits a high frequency rolloff of approximately 6dB/octave, which insures stability at all feedback gain levels, or when driving capacitive loads. At the same time, the fast slewing rate and relatively wide bandwidth guarantee fast step response, with low overshoot, and low phase shift, when the 3271/25 is used as an inverter or summing amplifier.

APPLICATIONS

Typical areas of application for the 3271/25 are: integrators, summing amplifiers, inverters, sample/hold units, D/A converters, precision function generation, data amplifiers, and DC preamplifiers. The wide supply voltage tolerance and stable design enable the 3271/25 to be used as a replacement for vacuum tube amplifiers and older, solid-state amplifiers in simulators, data acquisition systems, and other systems where it is desired to increase reliability and improve performance at modest cost.

Because of the rugged construction techniques and use of silicon semiconductors, the 3271/25 is not limited to laboratory applications, but may also be used in relatively severe environments. Examples are shipboard, airborne, high vibration industrial, and remote monitoring stations.

MODEL 3271/25 ENCAPSULATED PACKAGE



NOTE:
Dimensions in millimeters are shown in parentheses.

PIN CONNECTIONS

Pin 1	Inverting Signal Input
Pin 2	Common
Pin 4	Signal Output
(+)	Positive Power
(-)	Negative Power
Pin 3	External Zero Control
Pin 5	Overload Signal

MATERIAL

Case - Black Epoxy
Pins - Gold-Flashed
Header - Alum., Hard Black Anodized
Mating Connector
Model 1500MC

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

LI-227-2D

SPECIFICATIONS

Performance at 25°C and ±120 VDC supply unless otherwise noted.

* See discussion of output characteristics below.
Operating Temperature Range, -25°C to +85°C; Storage - 55°C to +100°C.

MODEL	RATED OUTPUT		DC GAIN	BANDWIDTH		SLEW RATE	INPUT OFFSET VOLTAGE					INPUT BIAS CURRENT				INPUT NOISE	OPEN LOOP IMPEDANCES		POWER SUPPLY	
	V_o	I_o		Unity Gain	Full Power		At +25°C	Over Range -25°C to +85°C	Versus Temp.	Versus Supply	Versus Time	At 25°C	Over Range -25°C to 85°C	Versus Temp.	Versus Supply	10Hz to 10kHz	Input	Output	Range	Quies. Current
	Volts min	mA min	dB min	MHz min	kHz min	V/μs min	μV max	μV max	μV/°C max	μV/V max	μV/mo typ	pA max	pA max	pA/°C max	pA/V max	μV rms max	MΩ typ	kΩ typ	Volts	mA max
3271/25	Supply less ±10V	±20	140	1.0	30*	20	±50	±110	1.0	1.0	+1	±80	±200	±2	±10	25 10(typ)	0.5	25	±60 to ±120	±20mA @±120VDC

OPEN-LOOP RESPONSE

The DC gain of the amplifier is typically 160dB because of the additional gain contributed by the DC chopper channel. This chopper channel gain rolls off at very-low frequency after which the amplifier gain is determined by the AC channel. The high frequency gain decreases at very nearly 6dB/octave. Figure 1 illustrates the open-loop gain response of a typical unit.

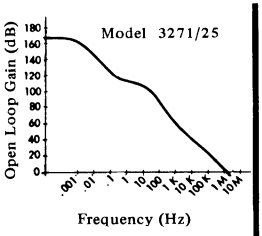


FIGURE 1. Open Loop Gain vs. Frequency.

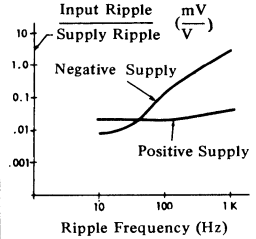


FIGURE 2. Supply Ripple Rejection vs. Frequency.

OUTPUT CHARACTERISTICS

The output stage of the amplifier is a balanced class B design which insures a minimum of quiescent drain from the power supply. The output current rating is +20mA and -20mA, regardless of the power supply level. Rated output voltage swing in either direction is 10V less than the supply voltage of the same polarity, whether equal or unequal values of supply voltage are used. For example, supply voltages of +75VDC and -90VDC could legitimately be used. The output voltage rated swing in the positive direction would be +(75-10) = +65V, while the negative rated output voltage would be -(90-10) = -80V. Full power frequency is measured with ±100V swing and ±20mA of output current, on ±120VDC supplies.

POWER SUPPLY CONSIDERATIONS

The 3271/25 will operate quite satisfactorily over a range of power supply voltages from ±60VDC to ±120VDC. In addition the supplies may have unequal values, so long as each is between 60V and 120V. Amplifier noise and drift will be minimized if the power supplies are balanced, well regulated, and have low output ripple. High frequency performance will be best, and crosstalk between adjacent amplifier channels will be least, if the supply impedance at the amplifier pins is low at all frequencies from DC to above 100kHz. If the supplies incorporate provisions for remote voltage sensing, the sense leads should be connected to the positive and negative supply buses as close as possible to the amplifier pins. The common lead should be as short as possible. Heavy gauge bus wire should be used if long supply and common leads are necessary. The addition of bypass capacitors from the supply bus to common, at the amplifier pins, will reduce the equivalent supply impedance and may be required if supply leads are long. Figure 2 illustrates the ripple induced at the amplifier input as a result of supply ripple.

INSTALLATION RECOMMENDATIONS

The input lead to the amplifier summing junction should be shielded to avoid pickup of spurious signals, particularly signals at the chopper drive frequency of 100Hz. In integrator applications, a shielded wire may be used to connect the feedback or integrating capacitor to the amplifier input terminals. The center conductor should be connected to the amplifier input, while the shield is connected to the amplifier output. The lead employed should have high insulation resistance to prevent capacitor discharge.

OFFSET VOLTAGE ZERO CONTROL

The Model 3271/25 operates with low DC input offset voltage, without the use of a zero control. An optional external zero control may be employed to accurately null the amplifier offset. This control is shown in the package drawing.

EXTERNAL OVERLOAD INDICATOR

Electrical overload signals may be detected in the chopper stabilizing channel and applied through pin 5 to an external overload indicating circuit. In the suggested circuit of Figure 3, D1 and D2 are silicon diodes; Q1 is an NPN silicon switching transistor while Q2 is a PNP silicon switch. Lamp DS1 is a 10V, 15mA indicator, G.E. #1869 or equivalent. The circuit may be adapted for latching operation by including the 100kΩ resistor and the reset switch shown in dotted lines. The indicator will then remain lighted, after the amplifier comes out of saturation, until the reset switch is closed.

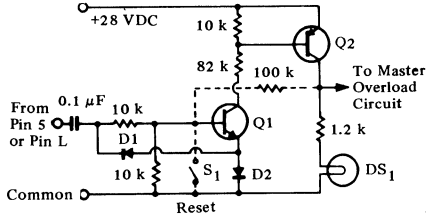
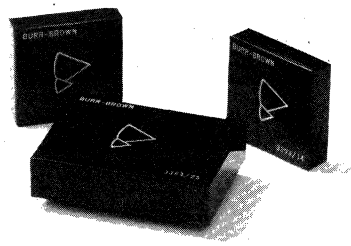


FIGURE 3. Overload Indicating Circuit.

BURR-BROWN®



3291
3292
3293
3354
3355
3356

Chopper-Stabilized OPERATIONAL AMPLIFIERS

FEATURES

- DIFFERENTIAL INPUT OR SINGLE-ENDED
- VOLTAGE DRIFT AS LOW AS 0.1μV/°C
- CURRENT DRIFT AS LOW AS 0.5pA/°C

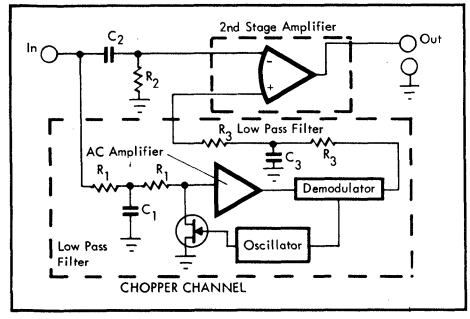


FIGURE 1. Single-ended Chopper-stablized Amplifier.

DESCRIPTION

Chopper-stabilized amplifiers achieve their ultra-low DC offset voltage and bias current by "chopping" the low frequency component of the input signal, amplifying this chopped signal in an AC amplifier and then demodulating the output of the AC amplifier. This output is then further amplified in a second stage of DC amplification. High frequency signals, which are filtered out at the input of the chopper channel, are coupled directly into the second stage amplifier. The net result of this technique is to reduce the DC offsets and drift of the second amplifier by a factor equal to the gain of the chopper channel. The AC amplifier introduces no offsets. Minor offsets and bias currents exist due to imperfect chopping, but these are extremely small.

The great strength of the chopper-stabilized amplifier is its insensitivity to component changes due to aging, temperature change, power supply variation or other environmental factors. Thus it is usually the best choice where both offset voltage and bias current must be small over long periods of time, or under significant environmental changes, and where external adjustment of offsets is undersirable or impossible. Both bias current and offset voltage can be nulled, if desired, by optional external controls. Figure 1 shows a simplified diagram of a single-ended chopper-stabilized op amp. Since the chopper channel, including switches and switch-driving oscillator, is built into the amplifier, only the DC power is supplied externally.

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PDS-235E

ELECTRICAL SPECIFICATIONS

SPECIFICATIONS Typical at 25°C and rated supply unless otherwise noted.		MODELS	RATED OUTPUT		DC GAIN	BANDWIDTH		SLEW RATE	INPUT NOISE			
			V_o	I_o		Unity Gain	Full Power		Voltage		Current	
									0.01 Hz to 10 Hz	10 Hz to 10 kHz	0.01 Hz to 10 Hz	10 Hz to 10 kHz
			Volts min	mA min	dB min	MHz min	kHz min	V/μsec min	μV p-p	μV rms	pA p-p	pA rms
	Low Cost Inverting Only	3291/14 3292/14 3293/14	±10	±5	140	3 typ	100	6.0	2	3	10	80
	Differential Input	3354/25 3355/25 3356/25	±10	±5	140	3	100	6.0	8	2	30	400

DIFFERENTIAL INPUT TYPES

Until the introudction of Burr-Brown Models 3354/25, 3355/25, and 3356/25, high performance chopper-stabilized operational amplifiers were always single-ended. In other words, they could only be used in inverting circuits. Now, with these units, the same ultra-low drift and low offset characteristics can be obtained for noninverting amplifiers, differential feedback amplifiers, sample/hold circuits, peak/hold circuits and many other applications where the amplifier must function with both differential and common-mode signals. These amplifiers are ideal for amplification of low level signals since the low drift and noise result in low input signal uncertainty. In addition, the gain and common-mode rejection ratio are very high, insuring excellent linearity of feedback gain (CMR for common-mode voltage of ±10V is typically 140dB at DC and 100dB up to 100Hz).

When the amplifier is used as a buffer for high impedance signal sources, the $10^{13}\Omega$ common-mode input impedance results in negligible loading of the source. Also, this causes the small DC input bias current to be virtually independent of input voltage - a very desirable characteristic for buffering of the memory capacitor in sample/hold and peak/hold circuits.

In general, these differential chopper-stabilized units can be used anywhere that a differential op amp would normally be used - but where both voltage and current drift must be very low.

LOW COST SINGLE-ENDED TYPES

For most inverting applications, Models 3291/14, 3292/14, or 3293/14 will be found to be the best choice. These units represent the state-of-the-art in single-ended chopper-stabilized amplifiers, featuring the lowest drift, lowest noise, lowest profile (1.5″ x 1.5″ x 0.4″), and the lowest prices available. Frequency response and slew rate are more than adequate for most applications.

Typical applications for these single-ended amplifiers are integrators, precision reference sources, D/A and A/D converters of high accuracy, precision comparators, current to voltage converters and high gain amplifiers for low level, low impedance signal sources.

Where a differential input is not required, these are the units to use for those applications where both low voltage drift and low bias current drift are required.

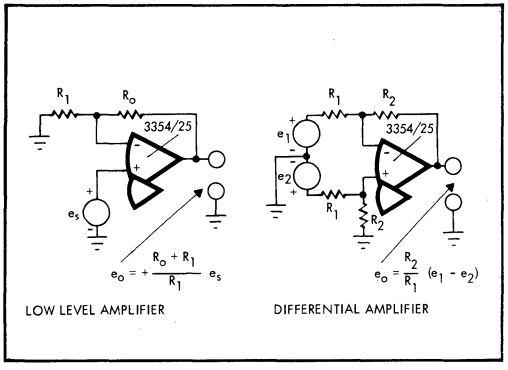


FIGURE 2. Typical Applications of Differential Chopper-stabilized Amplifiers.

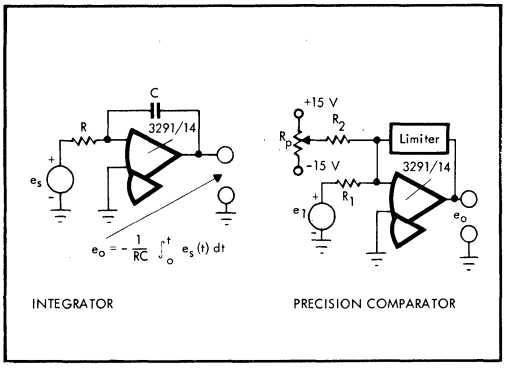


FIGURE 3. Typical Applications of Single-ended Chopper-stabilized Amplifiers.

INPUT OFFSET VOLTAGE		INPUT VOLTAGE DRIFT			INPUT BIAS CURRENT		BIAS CURRENT DRIFT		OPEN LOOP IMPEDANCES			POWER SUPPLY			PKG. DWG.
At 25°C	Over Range -25°C to +85°C	Versus Temp. -25°C to +85°C	Versus Supply	Versus Time	At 25°C	Over Range -25°C to +85°C	Versus Temp. -25°C to +85°C	Versus Supply	Input Diff.	Input CM	Output	Nom. Rated	Range	Quies. Current	See Page 1-57
µV max	µV max	µV/°C max	µV/V	µV/day	pA max	pA max	pA/°C max	pA/V	MΩ	Ω	kΩ	Volts	Volts	mA max	
±20 ±50 ±100	±26 ±68 ±160	±0.1 ±0.3 ±1.0	±5	1 µV/mo	±50 ±50 ±100	±80 ±110 ±220	±0.5 ±1.0 ±2.0	±10	0.5	-	1.5	±15	±12 to ±18	±10	/14
±30 ±50 ±100	±36 ±80 ±160	±0.1 ±0.25 ±1.0	±10	1 µV/mo	±20 ±50 ±50	doubles / +10°C		±1	1.0	$10^{13}\Omega$	2.0	±15	±12 to ±18	±10	/25

INSTALLATION, OPERATION AND APPLICATIONS INFORMATION

DRIFT CONSIDERATIONS

The best overall drift performance of an amplifier circuit will be achieved by minimizing impedance levels in the feedback network. The effect on output offset and drift of feedback and source impedances is illustrated in Figure 4. For very large resistances, input bias current becomes the major contributor to output voltage offset and drift. Where high input impedance and high gain are needed simultaneously, it may, therefore, not be feasible to use a single-ended inverting chopper-stabilized amplifier, because of this bias current factor. The differential input chopper-stabilized amplifier, used in the noninverting mode, then becomes the best choice. This allows the use of low impedance feedback networks while still retaining very high input impedance to prevent source loading. Note that input bias current doubles (approximately) for every +10°C temperature rise for these units.

The circuit of Figure 5 illustrates the effects of offset voltage and input bias current on integrator performance. Both parameters cause output errors which increase at a constant rate as a function of time. Additional offset voltage and input bias current caused by temperature drift will cause the output rate errors to increase with temperature. Note that the output rate error due to bias current diminishes as capacitance, C_F, increases. Usually, however, there is not much point in going beyond 10µF because of capacitor dielectric leakage. Also, as C_F is increased, R_i must decrease to maintain a given $R_i C_F$ product and there will usually be a lower limit on desirable values of R_i, since this represents the input impedance of the integrator. Also, R_i determines the amount of input and feedback current flowing for a given input level. The amplifier, and the signal source, must be capable of supplying this current. Thus a compromise set of R_i and C_F can usually be reached which takes into account these factors.

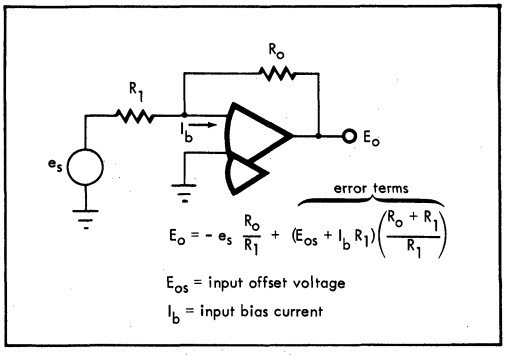


FIGURE 4. Output Drift Components.

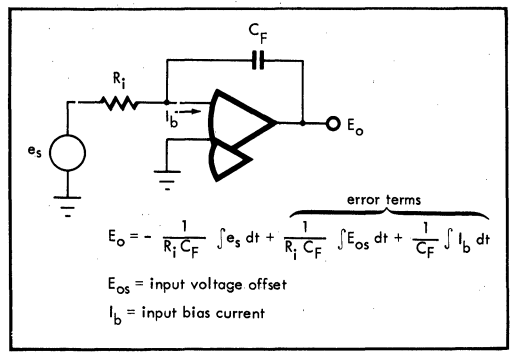


FIGURE 5. Integrator Errors Due to Offset Voltage and Bias Current.

NOISE CONSIDERATIONS

Because of the extremely low DC offset and DC drift associated with the chopper-stabilized amplifier, noise is often found to be the remaining limit on signal resolution. Thus it is desirable to design the feedback networks and external wiring to minimize the total circuit noise. This includes the proper grounding and noise decoupling as described under Wiring Recommendations. In addition it is desirable to minimize the levels of feedback impedance as a means of reducing noise "pickup" and the effects of amplifier current noise. When the full bandwidth of the amplifier is not required, it is recommended that a feedback capacitor be used to

limit the overall bandwidth and eliminate as much high frequency noise as possible.

When one of the differential input, chopper-stabilized amplifiers is used with a high impedance source, the input current noise will be the limiting factor on signal resolution. For source impedances of 1kΩ or greater it is recommended that a compensating resistance, R_C, be inserted in series with the inverting input (see Figure 6). This resistor will minimize the effect of current noise at the chopper frequency.

Shielding of feedback components is desirable and may be necessary in electrically noisy environments. Use of shielded wire for summing junction leads is also

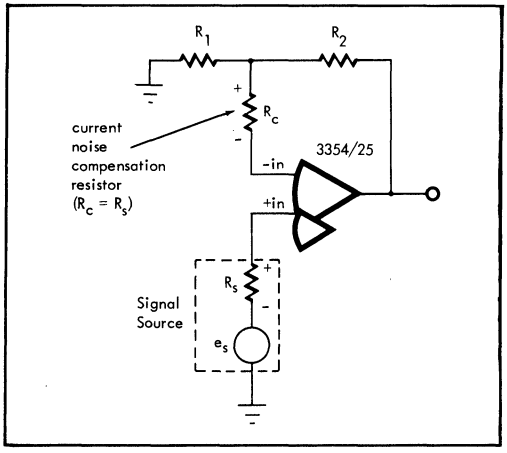


FIGURE 6. Use of a Current Noise Compensating Resistor with Differential Chopper-stabilized Operational Amplifier.

recommended in high noise environments. The shield should then be connected to the output terminal of the amplifier.

POWER SUPPLY REQUIREMENTS

The amplifiers described in this brochure are specified for operation on the rated supply voltages (±1%). They will operate with some degradation over the specified range

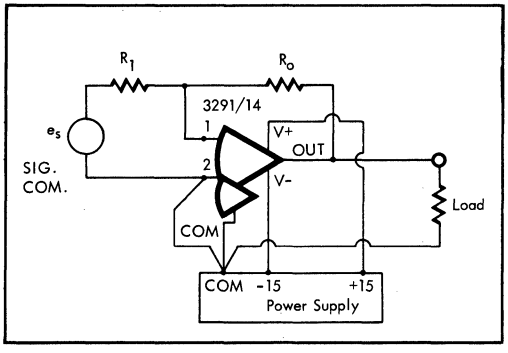


FIGURE 7. Proper Grounding of Models 3291/14, 3292/14 and 3293/14.

of supply voltages (±12VDC to ±18VDC for ±10V amplifiers).

Supply drain current is specified under quiescent conditions (no output current from the amplifier). When the amplifier is supplying current to a load, this current must be added to the quiescent current of the proper supply to determine total supply current.

WIRING RECOMMENDATIONS

Models 3291/14, 3292/14 and 3293/14 are designed with separate pins for power supply command and signal common. The diagram of Figure 7 illustrates the proper grounding techniques for these amplifiers. It is important that the signal common and power common leads be connected only at pin 2 of the amplifier. A separate lead is required from the power supply common to the COM pin of the amplifier.

Figure 8 illustrates proper grounding for noninverting circuits using the differential amplifiers (3354/25, 3355/25, 3356/25).

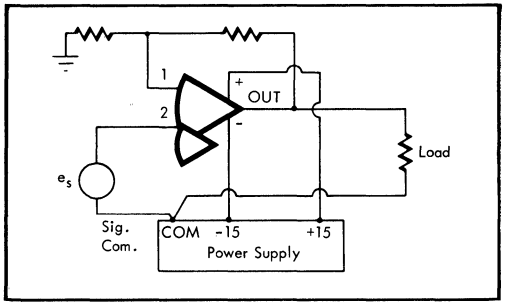


FIGURE 8. Proper Grounding of Differential Models (Noninverting Mode).

OVERLOAD CHARACTERISTICS

Because the chopper-stabilized amplifier consists of two amplifying channels, one fast and the other very slow, the overload behavior is different from that of nonchopper-stabilized op amps. If the chopper channel becomes overloaded due to a large error voltage at the summing junction, recovery may require as much as a few seconds. There are three ways in which such overloads may occur - output voltage saturation, output current limiting, and transient overload induced when power supply voltages are applied. The first of these three possible conditions arises when the amplifier output voltage is driven to its limits. When the output voltage can no longer follow the input signal, the summing junction voltage rises from its virtual ground potential. This relatively large potential is then amplified by the high gain of the chopper channel to a level of several volts, a much larger value than is encountered in the chopper channel during normal operation. Because of the very large time constants of the chopper channel filters, decay of this overvoltage, and consequently amplifier recovery, may take several seconds after removal of the overdrive signal. When the

amplifier reaches one of its output current limits, under the proper combination of loading and signal, a condition much like that of voltage saturation occurs. The output voltage fails to follow the input signal and chopper channel overload occurs.

In general, the amplifier will recover quickly from transient or short duration overloads since the relatively slow chopper channel will not become charged to high levels.

Overloads due to output voltage limiting (not current limiting) may be prevented by use of a feedback limiter such as that of Figure 9. Because the amplifier summing junction is always held at virtual ground, even when the limiter is active, the chopper channel does not overload and recovery from limiting is very rapid (1.0μsec or less is typical). The limits must, of course, be set below the output saturation levels of the amplifier itself.

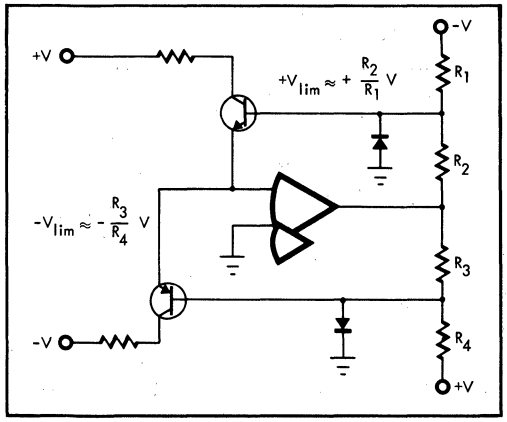


FIGURE 9. Feedback Limiter Circuit.

Overloads which occur during the application of DC power to the amplifier are a result of transient imbalances within the circuit. Recovery time from this type of overload is a function of circuit design. Where rapid recovery from such initial overloads is important, Models 3354/25, 3355/25 and 3356/25 are the best choices. These amplifiers typically recover to specified operation in less than one second. They recover equally fast from extended overload due to signal overdrive conditions for simple resistive feedback.

DC NULLING TECHNIQUES

The proper connections for nulling of the DC offset voltage are shown in the Mechanical Specifications. Note that in all cases these offset controls are optional and need not be used if the small offset voltage of the amplifier can be tolerated. The differential chopper-stabilized models (3354/25, 3355/25 and 3356/25) can be nulled as shown in Figure 10. However, the inherent offset voltage of these amplifiers is acceptably low (typically less than 10μV) for many applications and the null control may be unnecessary.

The input current of the amplifier may be nulled as in Figure 11 (for inverting circuits).

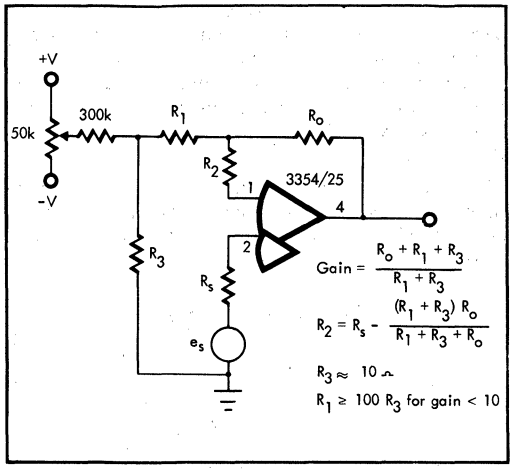


FIGURE 10. Offset Voltage Adjustment for Noninverting Circuits.

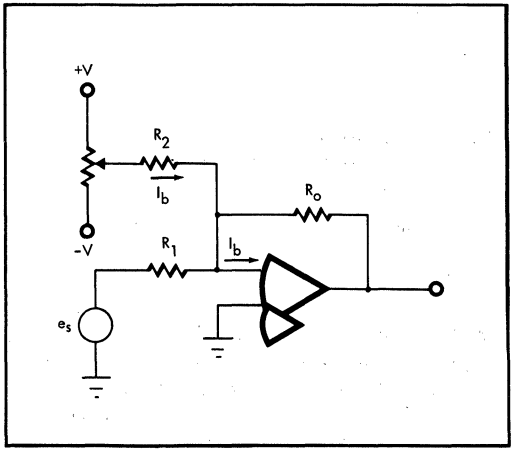


FIGURE 11. Null Adjustment of Input Current.

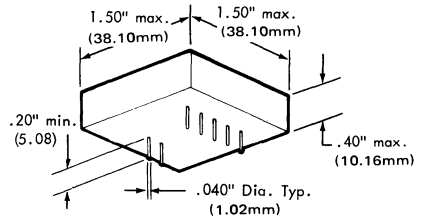
INPUT/OUTPUT PROTECTION

The various amplifiers described here are designed such that any voltage up to the value of power supply voltage may be applied directly to the amplifier input pin without damage to the amplifier.

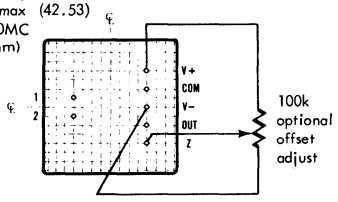
Output stages of the amplifiers are current limited to prevent damage should the output pin be shorted to common. Permanent damage to the amplifier may occur, however, if the output pin is connected to a voltage of the same order of magnitude as the supply voltages.

MECHANICAL SPECIFICATIONS

/14 MODULES



PIN - Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATERIAL - Black Epoxy
WEIGHT - 1.50 oz. max (42.53)
CONNECTOR - 1400MC
GRID - 0.1" (2.54mm)

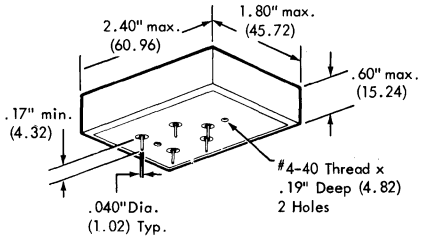


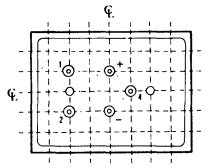
PIN CONNECTIONS - are as follows unless otherwise noted.

Pin	Connection
1	inverting input
2	signal common or noninverting input
3	(not used)
4 (OUT)	output
5	(not used)
+ (V+)	positive supply
- (V-)	negative supply
COM	power common
Z	optional offset adjust

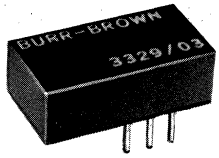
/25 MODULES

PIN - Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATERIAL - Black Epoxy
WEIGHT - 4.00 oz. max (113.40)
CONNECTOR - 1500MC
GRID - 0.3" (7.6)





BURR-BROWN®

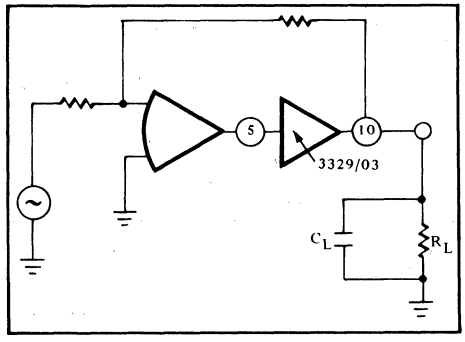


3329/03

HYBRID IC POWER BOOSTER

FEATURES

- ±100mA OUTPUT
- SHORT CIRCUIT PROTECTED
- NO HEAT SINK REQUIRED
- DUAL-IN-LINE PACKAGE



DESCRIPTION

The Model 3329/03 is a power booster amplifier designed for use in cascade with IC or discrete component operational amplifiers inside the feedback loop. Current output of up to ±100mA at ±10VDC is provided without the need for a heat sink. The unit is short circuit protected over the full temperature range of -40°C to +85°C. Output current is limited to ±150mA by internal circuitry. No external components are required. The high full power frequency (1MHz) and small signal bandwidth of 5MHz insure that the unit will not degrade the frequency response of the operational amplifier used.

The class B output stage provides high output current with a minimum of quiescent power supply drain. The low open loop output impedance (10Ω) insures stable operation with large capacitive loads, and virtually eliminates the closed loop gain loading effect of low impedance loads such as 50Ω terminated lines. Because of the 10kΩ input impedance of the booster, the current output requirements of the operational amplifier are minimal.

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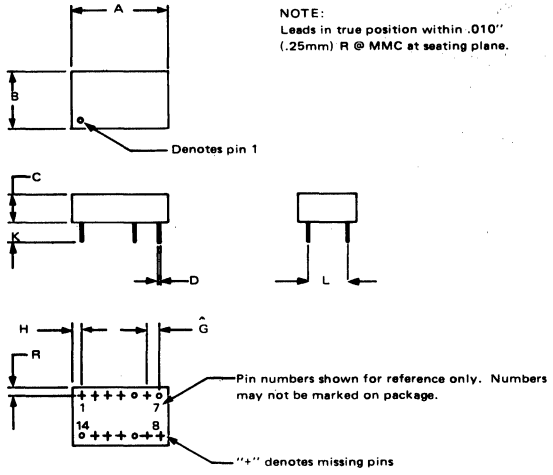
PDS-225E

MECHANICAL SPECIFICATIONS



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

APPLICATIONS INFORMATION

Power Supply Requirements

The Model 3329/03 is designed to operate over a power supply range of ±12 VDC to ±18 VDC. Output voltage swing is guaranteed to be in excess of ±10 volts at full load, when operating on supplies of ±15 VDC. For other values of supply voltage, the output swing varies in proportion.

Gain and Stability

The voltage gain of the 3329/03 is approximately 1.0. The accuracy of this gain is relatively unimportant, since the booster is used inside the feedback loop of an operational amplifier. The booster by itself is completely stable under all conditions of capacitive loading. Because of it's very low output impedance, the 3329/03 tends to isolate the associated operational amplifier from the effects of capacitive load.

The input impedance of the booster is approximately equal to 100 x (load impedance). Thus, for a 100 ohm load, the input impedance is approximately 10 k ohms. The effective output impedance of the booster is approximately equal to the output impedance of the operational amplifier, divided by 100.

For most general purpose operational amplifiers the dynamic output impedance is on the order of 1 kΩ. When a low impedance load (e.g. 50Ω) is being driven, a severe loading effect occurs which greatly reduces the effective open loop gain and bandwidth. Effectively, the unloaded gain and bandwidth of the operational amplifier would be multipled by the loading factor $\frac{50}{1050} \approx .05$, if the load is 50Ω.

When the 3329/03 booster is used, however, the effective open loop output impedance is 10Ω. The loading factor now is $\frac{50}{60} = .866$, and the gain and bandwidth are reduced only slightly by this loading.

Input and Output Protection

The output stage of the 3329/03 is current limited to insure survival of the booster if the output is shunted to ground. The unit is safe even under continuous short circuit at +85°C. No heat sink is required.

The input circuitry will withstand overvoltage up to the value of supply voltage.

Temperature Range

The 3329/03 will operate over the -40°C to +85°C temperature range. Storage temperature range may vary from -55°C to +100°C.

3329/03 POWER BOOSTER SPECIFICATIONS

Rated Output		Full Power Response	-3dB Response	Input Signal Range	Input Offset Voltage	Input Impedance	Output Impedance	Power Supply Requirements		
V_o Volts (min)	I_o mA (min)	kHz (min)	MHz (min)	Volts (min)	mVolts (max)	kΩ (typ.)	Ω (typ.)	Nom. Rated Volts	Range Volts	Quies. Current mA (max)
±10	±100	1000	5	±10	±50	10	10	±15	±12 to ±18	±15

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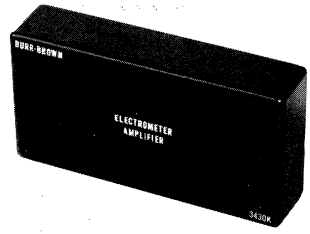

3430
3431

ELECTROMETER AMPLIFIERS

FEATURES

- ULTRA-LOW INPUT CURRENT, .01pA, max
- LOW INPUT CURRENT NOISE, .001pA, p-p
- HIGH INPUT IMPEDANCE, $10^{14}\Omega$
- INVERTING OR NONINVERTING OPERATION

DESCRIPTION

Models 3430 and 3431 are designed to minimize input bias current and input noise current through the use of a varactor diode bridge technique. Models 3430J and 3430K are intended for meaurement of very-low-level currents, long-term integrators and analog memory applications. The 3431J and 3431K are designed for measurement of sub-millivolt signals from very high source impedances such as pH and other electrochemical cells, and in long-term track/hold applications where charge stored on a capacitor is the input signal source.

The varactor bridge technique uses the voltage variable capacitance and extremely low leakage current of the two zero-biased varactor diodes to achieve input bias current and input current noise 10 to 100 times less than that of FET amplifiers.

The 3430 and 3431 out-perform amplifiers that use electrometer tubes or MOSFET input stages. Primary areas of advantage over these other devices are in voltage drift, common-mode rejection, and lower cost. An additional advantage over MOSFET's is the inherent input protection of the varactor bridge input configuration.

Operation of the 3430 and 3431 are simply explained. The amplifier input voltage, e_{in}, varies the capacitance of the varactor diodes, causing a bridge unbalance and developing a bridge output signal at the carrier frequency. This carrier frequency signal, which is proportional in amplitude to the input signal level, is amplified by the low-noise AC amplifier, phase-sensitivity demodulated to restore correct polarity and filtered to eliminate the carrier components. Additional amplification is provided by a conventional DC amplifier stage. The output is equal to the product of input signal and open-loop gain.

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SPECIFICATIONS

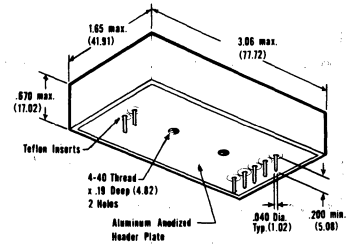
(Typical @ 25°C and ±15 VDC unless otherwise noted)

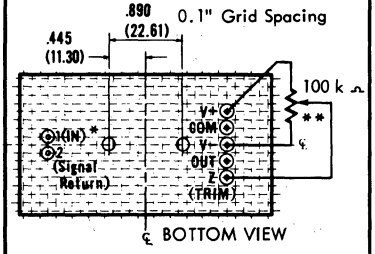
MODEL	3430J/K	3431J/K
OPEN LOOP GAIN		*
2 k Ω load, min.	100 dB	
RATED OUTPUT		*
Voltage, min	±10 V	
Current, min	±5 mA	
Load Capacitance	0 to .01 μF	
Output Impedance @ DC	2 k Ω	
FREQUENCY RESPONSE		
Unity gain, small signal	2 kHz	*
Full power response, min	7 Hz	
Slewing rate, min	0.4 V/ms	
Overload recovery	10 ms	
INPUT OFFSET VOLTAGE		
External trim pot	100 k Ω	*
Avg. vs. temp (10°C to 70°C) max	±30 μV/°C (J) ±10 μV/°C (K)	±30 μV/°C (J) ±10 μV/°C (K)
vs. supply voltage	±500 μV/V	*
vs. time	±100 μV/mo.	*
Warm-up drift	75 μV (15 min)	*
INPUT BIAS CURRENT		
Initial bias, 25°C, max		
Inverting input	±0.01 pA	±1 nA
Non-inverting input	±1 nA	±0.01 pA
Avg. vs. temp (signal input only)**	x2/10°C	*
vs. supply voltage (signal input only)	±0.01 pA/V	*
INPUT IMPEDANCE		
Differential	-	3×10^{11} Ω || 30 pF
Inverting input (to common)	3×10^{11} Ω || 30 pF	10^9 Ω || .02 μF
Non-inverting input (to common)	-	10^{14} Ω || 35 pF
INPUT NOISE		*
Voltage, .01 to 1 Hz, p-p	10 μV	
1 to 100 Hz rms	5 μV	
Current, .01 to 1 Hz, p-p	.001 pA	
1 to 100 Hz, rms	.002 pA	
COMMON MODE CHARACTERISTICS		
Max safe input voltage	±300V	±300V
Max common mode	NA	±200V
Common mode rejection @ ±25V	NA	100 dB
POWER SUPPLY		*
Voltage, rated specification	±15V	
Voltage, operating	±(12 to 18)V	
Current, quiescent	+15, -6 mA	
TEMPERATURE RANGE		*
Operating, rated specifications	0° to +70°C	
Operating, derated specifications	-25° to +85°C	
Storage	-55° to +85°C	
MECHANICAL		*
Case style	28	
Mating connector	2800MC	
Weight	6 oz.	

* Specification same as 3430.
** Negative input for Model 3430; positive input for Model 3431.

PACKAGE CONFIGURATION

NOTE: Dimensions in millimeters are shown in parentheses.

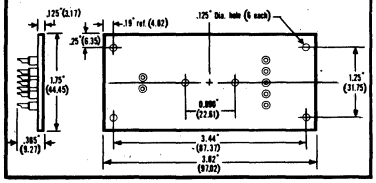




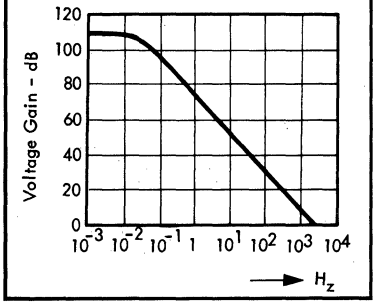
*-IN, 3430 **Optional Offset Adjust
+IN, 3431

PINS - Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATERIAL - Aluminum Case
Aluminum Anodized Header
WEIGHT - 6 oz max (170)

2800MC



OPEN LOOP FREQUENCY RESPONSE



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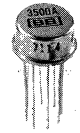


3500 SERIES

Low Bias Current OPERATIONAL AMPLIFIERS

FEATURES

- LOW BIAS CURRENT, ±15nA, max
- LOW DRIFT, ±1μV/°C, max
- LOW NOISE, 1.4μV, p-p
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- REPLACES 741 TYPE AMPLIFIERS

APPLICATIONS

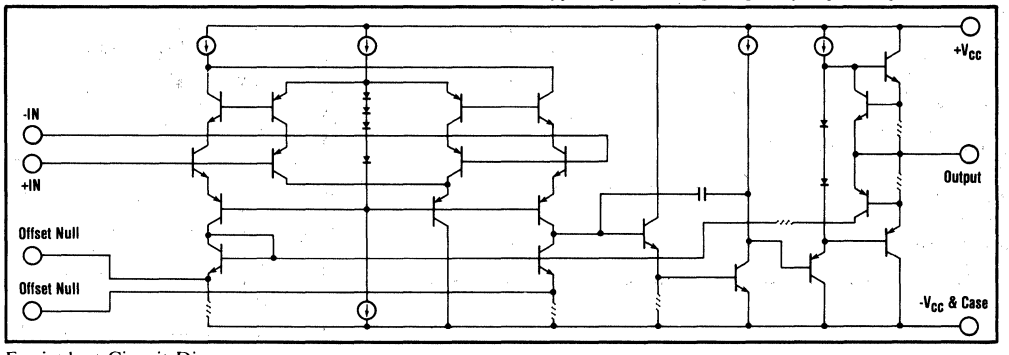
- GENERAL PURPOSE AMPLIFIER
- ANALOG COMPUTATION
- PRECISION BUFFER
- LOW DRIFT INTEGRATOR
- BRIDGE AMPLIFIER
- STABLE REFERENCE CIRCUITS

DESCRIPTION

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high impedance, both differential and common-mode. The amplifier maintains internal current levels essentially constant over the full range of power supply voltages. Thus the offset voltage and drift remain low for all combinations of supply voltage.

Both military and industrial temperature range versions are offered. Drift selected units are offered at ±1, ±3, ±5, ±10, and ±20μV/°C, max. The 3500 is also a low noise IC op amp, as illustrated by the typical performance curves. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30 volts, thus the amplifier can be used as a sensitive comparator. The output stage is internally current-limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.



Equivalent Circuit Diagram

PDS-471

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL	3500 SERIES			
	3500A 3500R	3500B 3500S	3500C 3500T	3500E
OPEN-LOOP GAIN, DC, no load, min	93dB	*	*	100dB**
RATED OUTPUT				
Voltage, min	±10V	*	*	*
Current, min	±10mA	*	*	*
Output Impedance	2kΩ	*	*	1kΩ
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1.5MHz	*	*	*
Full Power Sine Wave, min	10kHz	12kHz	15kHz	12kHz
Slew Rate, min	0.6V/μsec	0.8V/μsec	1.0V/μsec	0.8V/μsec
INPUT OFFSET VOLTAGE				
Initial Offset at 25°C, max	±5mV	±2mV	±1mV±500μV	±500μV
Avg. vs Temp. (-25°C to +85°C) max	±20μV/°C (A)	±5μV/°C (B)	±3μV/°C (C)	+1μV/°C
(-55°C to +125°C) max	±20μV/°C (R)	±10μV/°C (S)	±5μV/°C (T)	--
vs Supply Voltage	±40μV/V	*	*	*
vs Time	±2μV/day	*	*	±5μV/mo
INPUT BIAS CURRENT				
At 25°C (either input), max	±30nA	±20nA	±15nA	±50nA
Avg. vs Temp. (-25°C to +85°C) max	±1.0nA/°C (A)	±0.5nA/°C (B)	±0.3nA/°C (C)	±0.5nA/°C
(-55°C to +125°C) max	±1.5nA/°C (R)	±1.0nA/°C (S)	±0.5nA/°C (T)	--
vs Supply Voltage	±0.2nA/V	*	*	*
INPUT DIFFERENCE CURRENT				
At 25°C	±15nA	±10nA	±7nA	±30nA, max
Avg. vs Temp. (-25°C to +85°C)	±0.5nA/°C (A)	±0.2nA/°C (B)	±0.1nA/°C (C)	±0.3nA/°C, max
(-55°C to +125°C)	±0.7nA/°C (R)	±0.5nA/°C (S)	±0.2nA/°C (T)	--
vs Supply Voltage	±0.1nA/V	*	*	*
INPUT IMPEDANCE				
Differential	$10^7\Omega$ || 3pF	*	*	*
Common Mode	5 x $10^9\Omega$ || 3pF	*	*	*
INPUT NOISE				
Voltage, 0.01Hz to 10Hz, p-p	2.0μV	*	*	*
10Hz to 10kHz, rms	1.4μV	*	*	*
Current, 0.01Hz, p-p	200pA	*	*	*
10Hz to 10kHz, rms	35pA	*	*	*
INPUT VOLTAGE RANGE				
Common-mode Voltage, min	±11V	*	*	*
Common-mode Rejection at ±10V	100dB	*	*	*
Maximum Safe Input Voltage***	±V_{CC}	*	*	*
POWER SUPPLY				
Voltage, rated specification	±15V	*	*	*
Operating Range	±3V to ±20V	*	*	*
Current, quiescent, max	±3.5mA	*	*	*
TEMPERATURE				
Operating, Rated Specs A, B, C	-25°C to +85°C	*	*	*
R, S, T	-55°C to +125°C	*	*	--
Storage	-65°C to +150°C	*	*	*

*Specifications the same as the 3500A or 3500R. **Typical.

***If signal voltage is applied to the input in the absence of power supply voltage, series resistance should be used to limit input current to 20mA.

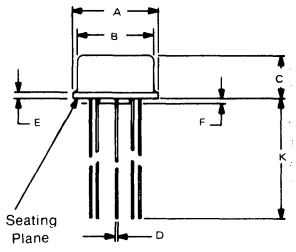
ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65° C to +150° C
Operating Temperature Range	-55° C to +125° C
Lead Temperature - Soldering, 10 seconds	+300° C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+150° C

NOTES:
1. Package must be derated based on: θ_{JC} = 45°C/W or θ_{JA} = 150°C/W.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to power supply common only. Rating applies to +85°C ambient.

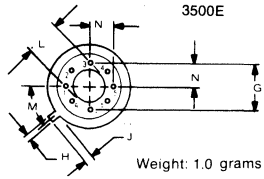
MECHANICAL

TO-99



Order Number:

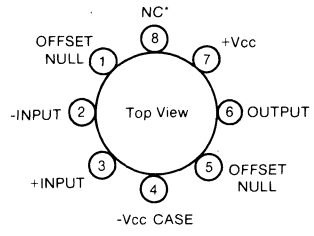
3500A
3500B
3500C
3500R
3500S
3500T
3500E



Weight: 1.0 grams

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

PIN CONFIGURATION

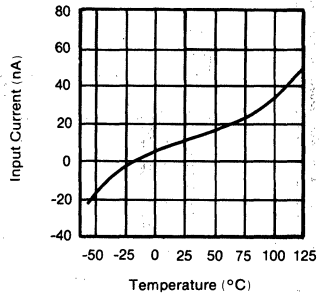


*No Internal Connection

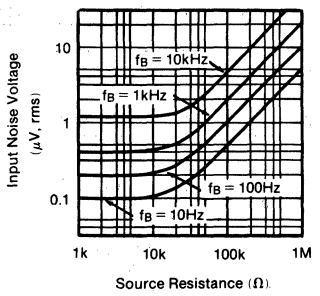
TYPICAL PERFORMANCE CURVES

(At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise specified)

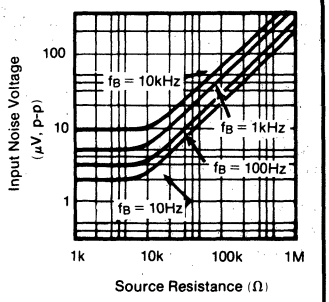
INPUT BIAS CURRENT VS TEMPERATURE



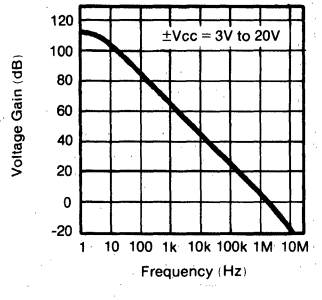
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



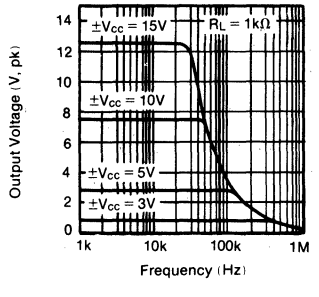
P-P INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



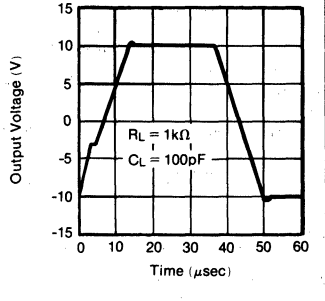
OPEN-LOOP FREQUENCY RESPONSE



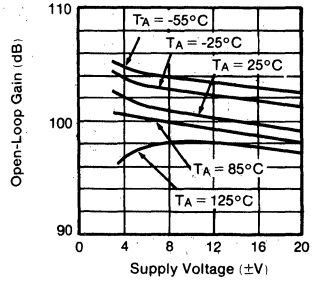
OUTPUT VOLTAGE VS FREQUENCY



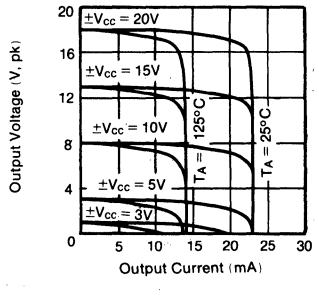
VOLTAGE FOLLOWER STEP RESPONSE



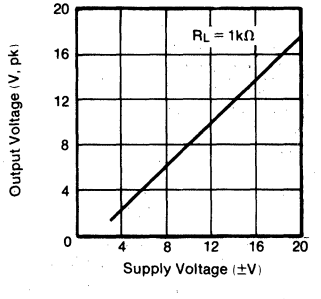
VOLTAGE GAIN VS SUPPLY VOLTAGE



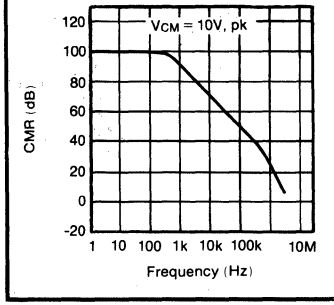
OUTPUT VOLTAGE VS OUTPUT CURRENT



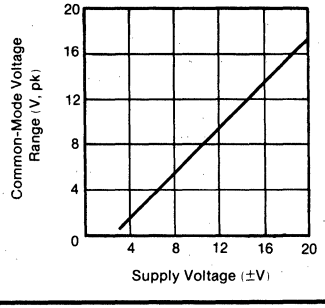
OUTPUT VOLTAGE VS SUPPLY VOLTAGE



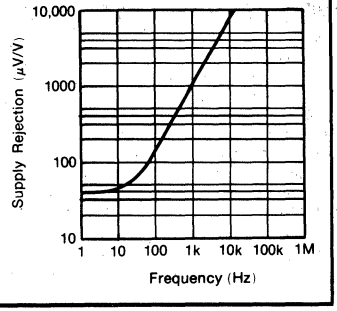
COMMON-MODE REJECTION VS FREQUENCY



COMMON-MODE RANGE VS SUPPLY VOLTAGE



POWER SUPPLY REJECTION VS FREQUENCY



APPLICATIONS INFORMATION

OFFSET ADJUSTMENT

The input offset voltage of the Model 3500 may be adjusted to zero by connecting a 50kΩ potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 1a). This provides an adjustment range of approximately ±10mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the 3500 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3μV/°C change of drift for each 1.0mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers, such as the 3500C and 3500T, this effect must be considered. By use of a transistor as in Figure 1 the effect of offset adjustment on drift can be substantially reduced (by approximately a factor of six).

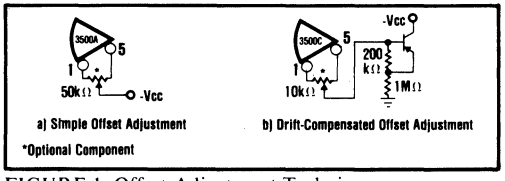


FIGURE 1. Offset Adjustment Techniques.

BIAS CURRENT EFFECTS

Input bias current of the amplifier creates additional offset voltages by flowing in the impedances of the signal source and the feedback network. Although the bias currents of the 3500 are quite small, their effects may be appreciable when these impedances are large. The bias currents at the two inputs tend to be equal and the difference current smaller than either. Thus equalizing the resistance from each input to common, as in Figure 2, is an effective means of reducing DC offset due to bias current.

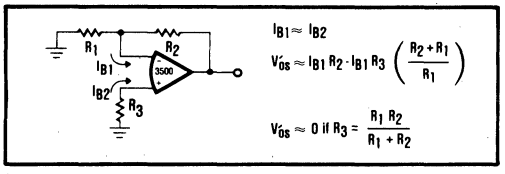


FIGURE 2. Minimization of Bias Current Effects.

OPERATION ON A SINGLE SUPPLY

Although virtually any op amp can be operated on a single supply if input and output voltage limitations are observed, the Model 3500 is particularly suitable for such use. Its wide supply range of ±3VDC to ±20VDC translates to a single supply operating range of 6VDC to 40VDC, plus or minus. Two possible modes of operation on a single supply are shown in Figure 3. The following conditions must be observed to keep the amplifier within its linear region of operation.

1) $+2 < V_O < (V_{CC} - 2)$

2) $+3 < V_{IN} < (V_{CC} - 3)$, Figure 3b

When operating on a single supply ($+V_{CC}$), shorting the output to common is equivalent to a short to supply and the internal power dissipation is approximately twice that which occurs for a short to common with balanced supplies of $\pm\frac{V_{CC}}{2}$. This dissipation may exceed safe limits for single supply voltages greater than 20V and must be prevented by use of a series limiting resistor or other device, if short circuit protection is desired.

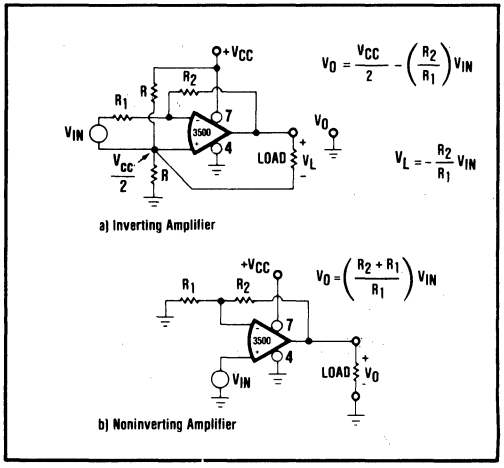
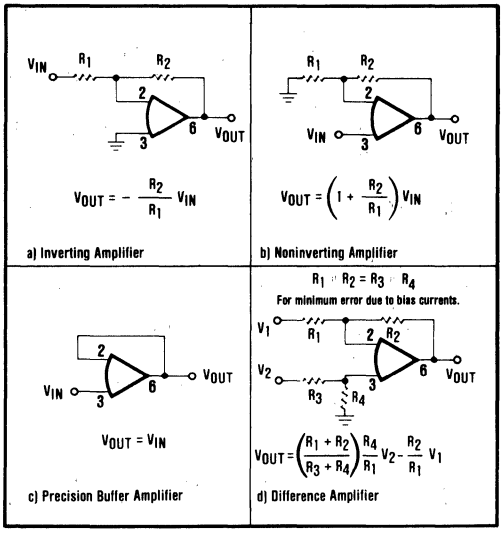


FIGURE 3. Operation on a Single Supply.

WIRING PRECAUTIONS

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 0.001μF ceramic capacitor from pins 7 and 4 to the power supply common.

TYPICAL APPLICATIONS



BURR-BROWN®

3500MP

Matched Low Bias Current IC OPERATIONAL AMPLIFIERS

FEATURES

TWO MONOLITHIC OP AMPS WITH ...

- MATCHED OFFSET VOLTAGES - △ Vos = 200μV max
- MATCHED DRIFT, △Vos vs Temp. = 1μV/°C max
- LOW NOISE, 1.4μV p-p
- LOW BIAS CURRENT, 50nA max
- INTERNAL COMPENSATION
- WIDE POWER SUPPLY RANGE

APPLICATIONS

- INSTRUMENTATION AMPLIFIERS
- MULTISTAGE ACTIVE FILTERS WITH LOW OUTPUT OFFSET
- LOW DRIFT SINGLE-ENDED AMPLIFIERS WITH LOW NOISE
- DUAL CHANNEL AMPLIFIERS WITH MATCHED DRIFT

DESCRIPTION

Close process control and careful grading by Burr-Brown make possible a new dimension in IC op amps - drift matched pairs. Drifts as low as 1μV/°C may be obtained using the 3500MP op amps. The 3500MP IC's are selected from Burr-Brown's 3500 series of op amps, thus all the features of the 3500 series are automatically found in the 3500MP. This enables the 3500MP to provide very-low drift (1μV/°C) with very-low noise (1.4μV p-p) without sacrificing speed. (Slew rate 0.8V/μsec min.)

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high input impedance, both differential and common-mode.

All units of the 3500E series are 100% temperature tested for voltage and current drift. The 3500 is also one of the lowest noise IC op amps yet produced, as illustrated by the curves on page 1-68. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30V. The output stage is internally current limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.

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PDS-264E

SPECIFICATIONS

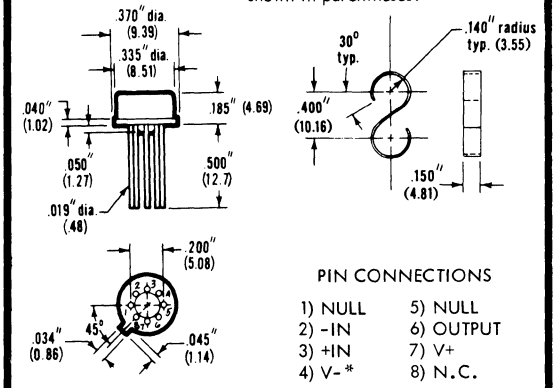
Specifications typical at 25°C and ±15 Vdc power supply unless otherwise noted.
(Two matched operational amplifiers Burr-Brown 3500 type)

MODEL	3500MP (Both Units)
OPEN LOOP GAIN	100 dB
RATED OUTPUT	
Voltage	±10 V, min.
Current	±10 mA, min.
Output Impedance	1 kΩ
FREQUENCY RESPONSE	
Unity Gain, Small Signal	1.5 MHz
Full Power Sine Wave	12 kHz, min.
Slew Rate	0.8 V/μsec, min.
INPUT OFFSET VOLTAGE V_{os1}, V_{os2}	
Initial Offset @ 25°C	±2 mV, max.
Avg. vs. Temp. (-25 to +85°C) max.	±5 μV/°C
vs. Supply Voltage	±40 μV/V
vs. Time	±5 μV/mo
DIFFERENTIAL INPUT OFFSET VOLTAGE $\Delta V_{os} = \lvert V_{os1} - V_{os2} \rvert$	
Initial Offset @ 25°C	±200 μV, max.
Avg. vs. Temp. (-25 to +85°C) max.	±1.0 μV/°C
INPUT BIAS CURRENT	
@ 25°C (either input)	±50 nA, max.
Avg. vs. Temp. (-25°C to +85°C) max.	±0.5 nA/°C
vs. Supply Voltage	±0.2 nA/V
INPUT DIFFERENCE CURRENT	
@ 25°C	±25 nA
Avg. vs. Temp. (-25°C to +85°C)	±0.25 nA/°C
vs. Supply Voltage	±0.1 nA/V
INPUT IMPEDANCE	
Differential	10^7 Ω || 3 pF
Common Mode	5×10^9 Ω || 3 pF
INPUT NOISE	
Voltage, 0.01 Hz to 10 Hz, p-p	2.0 μV
10 Hz to 10 kHz, rms	1.4 μV
Current, 0.01 Hz to 10 Hz, p-p	200 pA
10 Hz to 10 kHz, rms	35 pA
INPUT VOLTAGE RANGE	
Common Mode Voltage	±11 V, min.
Common Mode Rejection @ ±10 V	100 dB
Maximum Safe Input Voltage *	± supply
POWER SUPPLY	
Voltage, Rated Specification	±15 V
Operating Range	±3 to ±20 V
Current, Quiescent	±3.5 mA, max
TEMPERATURE RANGE	
Operating Ambient	-25 to +85°C
Storage	-65 to +125°C

* If signal voltage is applied to the input in the absence of power supply voltage, series resistance should be used to limit input current to 20 mA.

TO-99 PACKAGE

Dimensions in millimeters are shown in parentheses.



PIN CONNECTIONS

1) NULL	5) NULL
2) -IN	6) OUTPUT
3) +IN	7) V+
4) V- *	8) N.C.

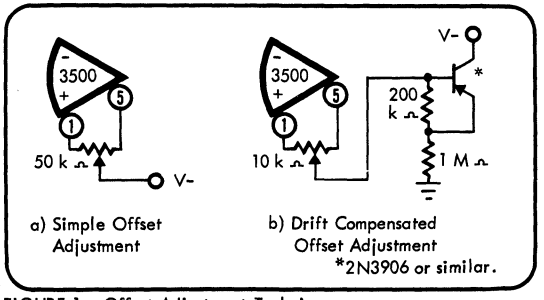
*Pin 4 is connected to case. NC is no internal connection

OFFSET ADJUSTMENT

The input offset voltage of the Model 3500 may be adjusted to zero by connecting a 50 kΩ potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 1a). This provides an adjustment range of approximately ±10 mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the Model 3500 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3 μV/°C change of drift for each 1.0 mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers this effect must be considered. By use of a transistor as in Figure 1b the effect of offset adjustment on drift can be substantially reduced (by approximately a factor of six).

Whenever possible adjust V_{os1} to equal V_{os2} (zero differential offset). Do not adjust $V_{os1} = 0 = V_{os2}$ unless absolutely necessary. If both V_{os1} and V_{os2} are adjusted to zero, the drift compensated adjustment technique (Figure 1b) must be used or the ΔV_{os} drift of 1 μV/°C will be adversely affected.



a) Simple Offset Adjustment

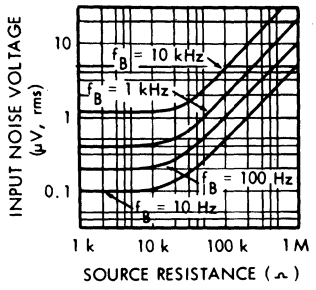
b) Drift Compensated Offset Adjustment
*2N3906 or similar.

FIGURE 1. Offset Adjustment Techniques.

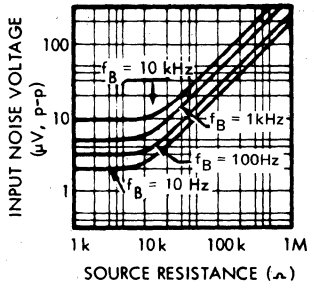
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

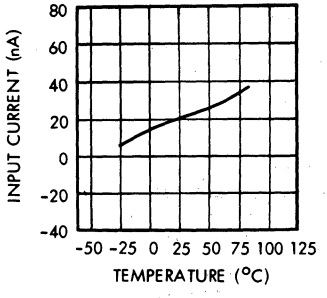
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



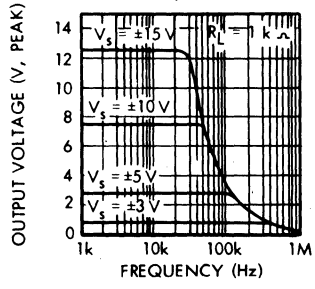
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



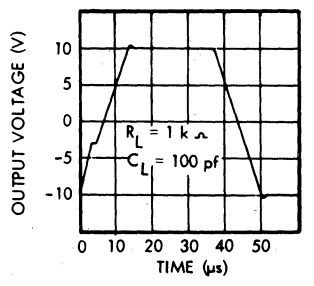
INPUT BIAS CURRENT vs. TEMPERATURE



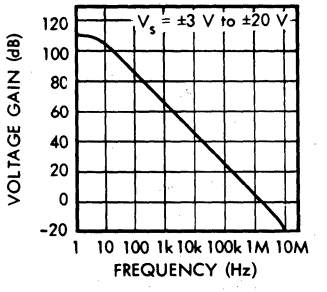
OUTPUT VOLTAGE vs. FREQUENCY



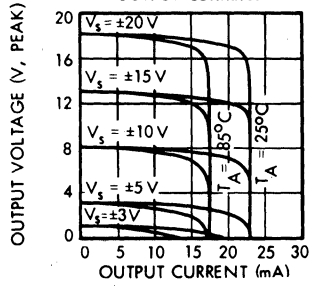
VOLTAGE FOLLOWER STEP RESPONSE



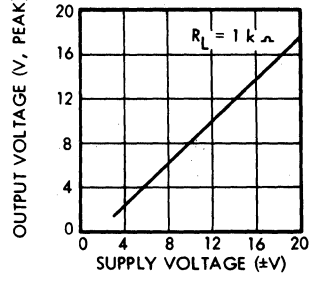
OPEN LOOP FREQUENCY RESPONSE



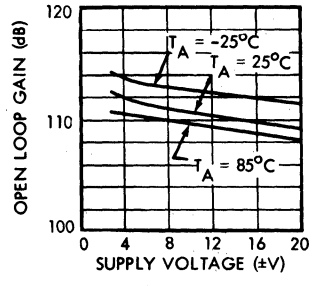
OUTPUT VOLTAGE vs. OUTPUT CURRENT



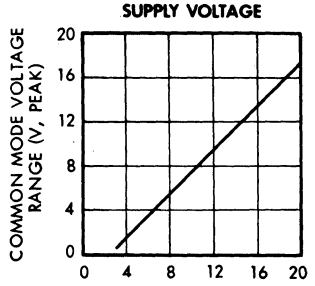
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



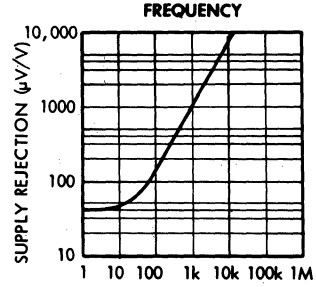
VOLTAGE GAIN vs. SUPPLY VOLTAGE



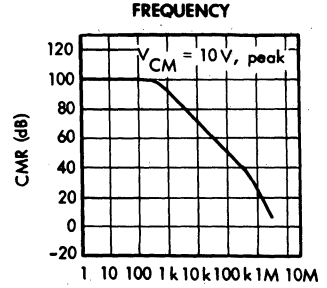
COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



COMMON MODE REJECTION vs. FREQUENCY



BIAS CURRENT EFFECTS

Input bias current of an amplifier can generate additional small offset voltages by flowing through the equivalent input source resistances. Although the bias currents for the 3500MP are quite small, the current-generated offset voltages may be significant for source resistances greater than 1 kΩ. When using the matched 3500MP amplifiers to obtain offset voltage drifts on the order of 1 μV/°C particular attention must be given to the input bias currents. Because of the great number of circuit configurations involving two operational amplifiers, it is only possible to give some general guidelines for minimizing bias current effects.

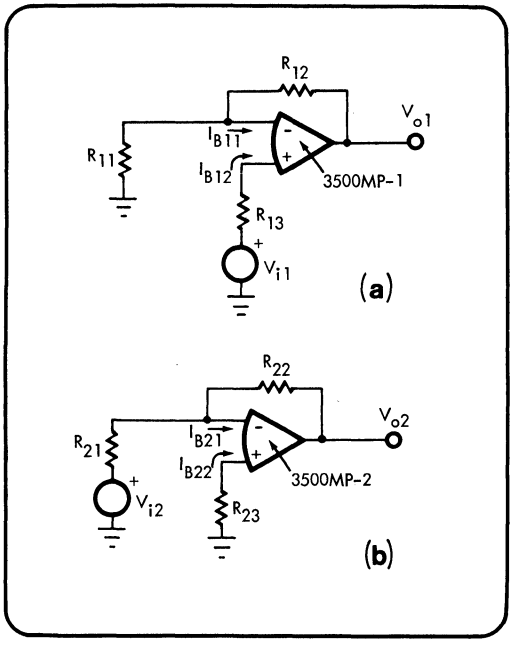


FIGURE 2. Bias Current Effects.

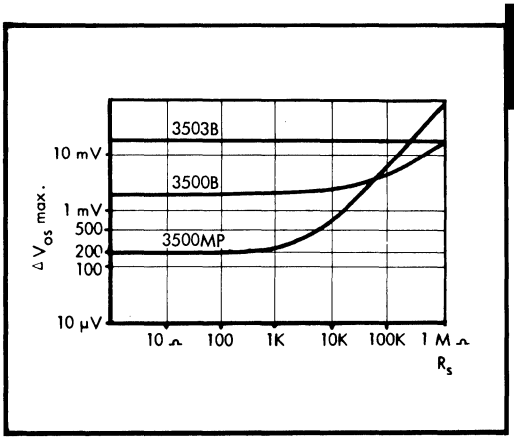


FIGURE 3. ΔV_{os} vs. Source Resistance.

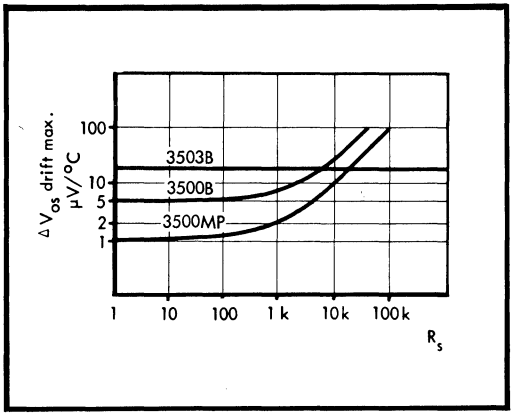


FIGURE 4. ΔV_{os} Drift vs. Source Resistance.

Bias currents generate offset voltages in two ways. If $I_{B11} = I_{B12}$ (see Figure 2a) no offset will be generated by I_{B11} and I_{B12}

$$\text{if } R_{13} = \frac{R_{11}R_{12}}{R_{11}+R_{12}}$$

However, in general, $I_{B11} = I_{B12} + I_{os1}$ where I_{os1} is the input offset current of op amp 1. I_{os} will vary from unit to unit and I_{os} is also subject to drift with time and temperature. Fortunately I_{os} is normally much less than I_{B11}. Therefore we may minimize effects of bias current by making the Thevenin equivalent input resistances equal (i.e. $R_{13} = \frac{R_{11}R_{12}}{R_{11}+R_{12}}$) and the effects of I_{os} may be minimized by making the equivalent source resistances small. Keep in mind that in some two amplifier circuits the "differential" bias current ($\Delta I_B = I_{B11} - I_{B12}$) will generate the predominate source of bias current errors.

Similarly for the circuit configuration of Figure 2b bias current effects are minimized by setting

$$R_{23} = \frac{R_{21}R_{22}}{R_{21}+R_{22}}$$

The effect of offset currents are summarized in Figures 3 and 4 which plot offset voltage (ΔV_{os}) between the two amplifiers and ΔV_{os} drift as a function of source resistance (R_s). Curves for a single 3500B type amplifier and an FET input 3503B) amplifier are included for comparison. Note that a 3500MP provides superior performance for low source resistance.

THERMAL CONSIDERATIONS

The very low ΔV_{os} drift specification for the 3500MP assumes both integrated circuits have the same "chip" temperature. A metal clip is furnished with the 3500MP to provide close thermal matching between the two device cases. However, care should be taken to see that each op amp drives approximately the same load or thermal offsets will result due to internal self heating. In any case thermal offsets are much less critical with the 3500MP than with matched transistors. A 1°C temperature offset will cause a voltage offset in a matched pair of transistors of about 2.5 mV but the ΔV_{os} of a 3500MP will be only 5 μV for 1°C temperature offset.

APPLICATIONS

COMPOSITE LOW DRIFT OP AMP

The two matched op amps in the 3500MP may be connected to simulate a single op amp with very low initial offset voltage and drift. The circuit shown in Figure 5a may be used in any conventional op amp circuit to obtain low drift. A typical feedback circuit with an inverting gain of 100 is shown in Figure 5c. Note the addition of R_3, R_4, and R_5 to minimize bias current effects on the offset voltage.

The composite op amp will be stable in circuits with voltage gains greater than about three. For lower voltage gains the compensation shown in Figure 5b may be used if required. For unity gain non-inverting operation, the compensation technique of Figure 5b will not decrease the composite amplifier bandwidth below the bandwidth of the individual op amps.

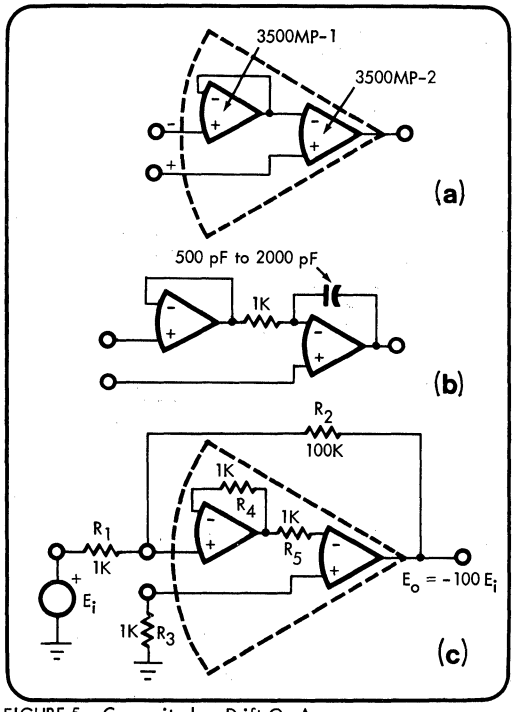


FIGURE 5. Composite low Drift Op Amp.

HIGH INPUT IMPEDANCE DIFFERENTIAL AMPLIFIER

The circuit in Figure 7 acts as a high input impedance differential amplifier provided $R_1 / R_2 = R_4 / R_3$. A mismatch of resistance ratios results in a common mode gain A_C as shown below. In addition to finite common mode gain, a resistance mismatch causes a differential gain error equal to A_C/A_D. Notice that the output offset error is proportional to ΔV_{os} which is made very small by the matching of the two op amps. (In most practical cases $A_D \Delta V_{os} >> A_C (V_{os1} + V_{os2}) / 2$.)

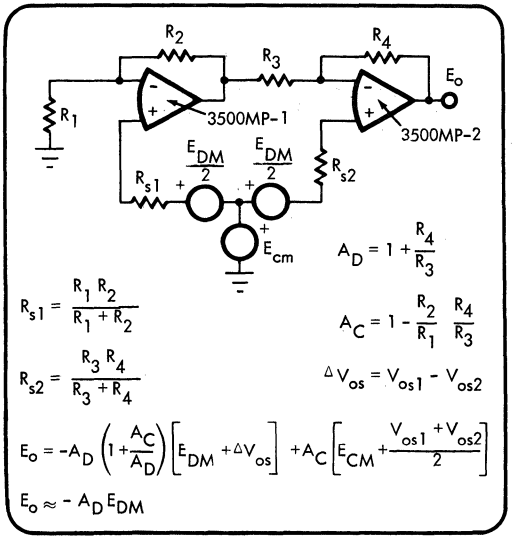


FIGURE 7. Differential Amplifier.

LOW PASS FILTER WITH LOW DC ERROR

Multistage low pass active filters often have large amounts of d.c. offset and drift because the offsets of the op amps used tend to add. The inverting synthesis technique shown in Figure 6 to realize each pole pair causes the amplifier offset voltages to cancel if they are matched. The net offset error without trimming will be less than 400 μV and the total drift of the filter is less than 2 μV/°C. The output d.c. error is made essentially independent of bias current effects by choosing small resistor values. However the small resistance values limit the maximum output voltage to about 1.0 V p-p and $R_L > 125\ \Omega$.

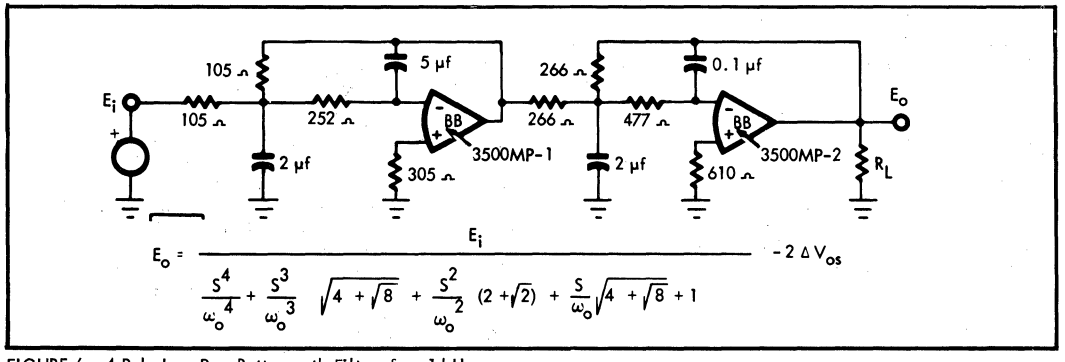
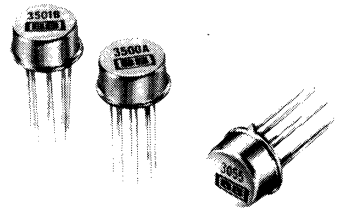


FIGURE 6. 4 Pole Low Pass Butterworth Filter; f_o = 1 kHz.

BURR-BROWN®



3501

Low Bias Current OPERATIONAL AMPLIFIERS

FEATURES

- LOW BIAS CURRENT, ±3nA, max
- LOW DRIFT, ±5μV/°C, max ±30pA/°C, max
- LOW NOISE, 0.8μV, p-p 30pA, p-p
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- REPLACES 108 AND 741 TYPE AMPLIFIERS

DESCRIPTION

The 3501 series is designed to minimize input voltage drift and input bias current, without resorting to exotic processing. The low input bias current is achieved by a current cancellation technique developed by Burr-Brown's IC Engineering Group. The same input circuitry gives the 3501 very-high input impedance, both differential and common-mode. Internal current levels of the amplifier are maintained essentially constant over the full range of supply voltages by relying on basic semiconductor properties and device matching. The result is that major performance parameters - open-loop gain, bias current, voltage drift, slew rate and output current - are affected only slightly by wide variations of supply voltage. Quiescent power drain is quite low over the supply voltage range.

The 3501 is internally compensated for unconditional stability in all feedback configurations, even with capacitive loads. Thus it is interchangeable with both 741 and 108 type amplifiers (eliminating the external frequency compensation required of 108 type amplifiers).

Because of the unique input stage design of the 3501, its common-mode rejection is very-high (100dB). The result is excellent linearity (.01% or better) as a noninverting buffer. Also the input stage exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high for input voltages up to the value of the supply voltages.

The output stage is internally current limited to provide protection against continuous circuits.

All units of the 3501 series are 100% tested to all min/max specifications - including voltage and current drift versus temperature. Units are drift selected with maximum specifications at ±5μV/°C, ±10μV/°C and ±20μV/°C. Both military and industrial temperature range versions are offered.

The 3501 is also a very-low noise amplifier. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually dictate against the use of utility op amps, such as the 741, for low-level signal processing.

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PDS-249E

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

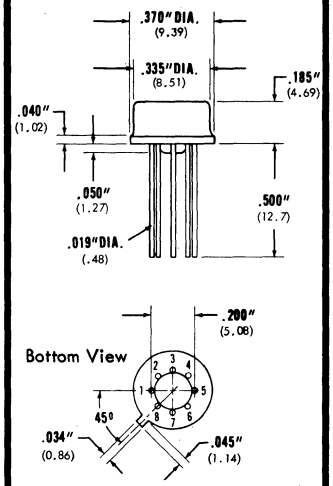
Typical at 25°C and ±15 Vdc unless otherwise noted.

MODEL	3501A 3501R	3501B 3501S	3501C
OPEN LOOP GAIN, dc, no load	93 dB, min	*	*
RATED OUTPUT		*	*
Voltage	±10V, min		
Current	±5 mA, min		
Capacitive Load Range	0 to 1000 pF		
Output Impedance	2 kΩ		
FREQUENCY RESPONSE		*	*
Unity Gain, Open Loop	0.5 MHz		
Full Power Sine Wave	1.6 kHz, min		
Slew Rate	0.1 V/μsec, min		
INPUT OFFSET VOLTAGE			
Initial Offset @ 25°C	±5 mV, max	±2 mV, max	±2 mV, max
Avg. vs. Temp. (-25° to +85°C) max	±20 μV/°C (A)	±10μV/°C (B)	±5 μV/°C (C)
(-55° to +125°C) max	±20 μV/°C (R)	±10 μV/°C (S)	
vs. Supply Voltage	±40 μV/V	*	*
vs. Time	±2 μV/day	*	*
INPUT BIAS CURRENT			
@ 25°C	±15 nA, max	±7 nA, max	±3 nA, max
Avg. vs. Temp. (-25° to +85°C) max	±0.2 nA/°C (A)	±0.15 nA/°C(B)	±0.1 nA/°C(C)
(-55° to +125°C) max	±0.2 nA/°C (R)	±0.15 nA/°C(S)	
vs. Supply Voltage	±30 pA/V	*	*
INPUT DIFFERENCE CURRENT			
@ 25°C	±5 nA	±3 nA	±2 nA
Avg. vs. Temp. (-25° to +85°C)	±0.1 nA/°C (A)	±0.05 nA/°C(B)	±0.03nA/°C(C)
(-55° to +125°C	±0.1 nA/°C (R)	±0.05 nA/°C(S)	
vs. Supply Voltage	±10 pA/V	*	*
INPUT IMPEDANCE		*	*
Differential	$5 \times 10^7\ \Omega$ ‖ 3 pF		
Common Mode	$10^{10}\ \Omega$ ‖ 3 pF		
INPUT NOISE		*	*
Voltage, .01 Hz to 10 Hz, p-p	2 μV		
10 Hz to 10 kHz, rms	1.4 μV		
Current, .01 Hz to 10 Hz, p-p	66 pA		
10 Hz to 10 kHz, rms	12 pA		
INPUT VOLTAGE RANGE		*	*
Common Mode Voltage	±11 V, min		
Common Mode Rejection @ ±10V	100 dB		
Max. Safe Input Voltage	±supply**		
POWER SUPPLY		*	*
Voltage, rated specification	±15 Vdc		
Operating Range	±3V to ±20V		
Absolute Max	±22 Vdc		
Current, quiescent	±1.5 mA, max.		
TEMPERATURE RANGE			
Operating, Rated Specs A, B, C	-25° to +85°C	*	*
R, S	-55° to +125°C	*	*
Storage	-65° to +150°C	*	*

* Specifications same for all models. ** If input voltage is applied in the absence of power supply voltage, series resistance should be added to limit current flow to ±20 mA.

TO-99 PACKAGE

Specify 3501A, etc.



Note: Dimensions in millimeters are shown in parentheses.

PIN CONNECTIONS

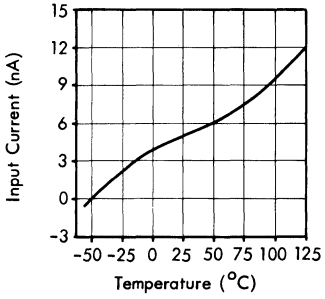
1) NULL	5) NULL
2) -IN	6) OUTPUT
3) +IN	7) V+
4) V-*	8) N.C.

*Pin 4 connected to case

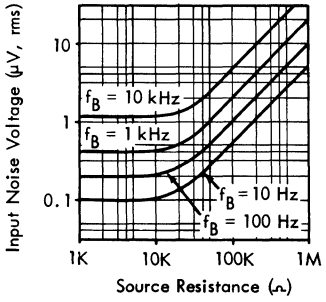
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

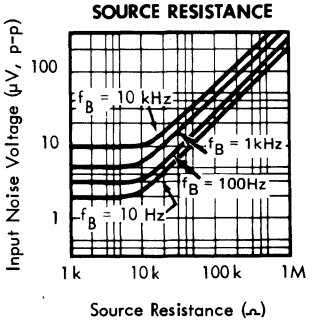
INPUT BIAS CURRENT vs. TEMPERATURE



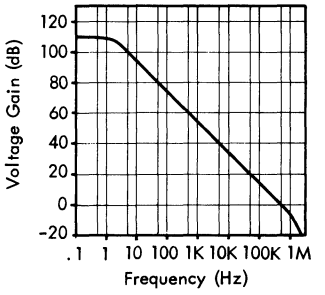
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



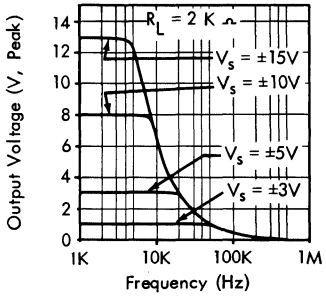
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



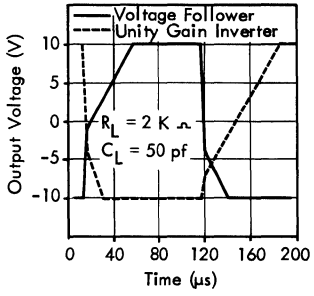
OPEN LOOP FREQUENCY RESPONSE



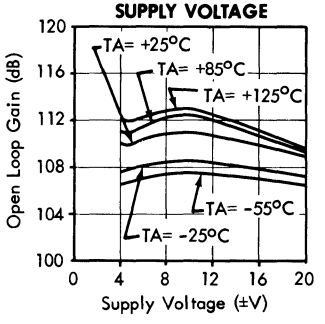
OUTPUT VOLTAGE vs. FREQUENCY



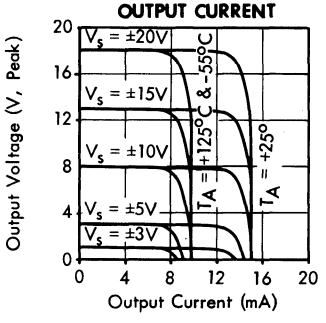
LARGE SIGNAL STEP RESPONSE



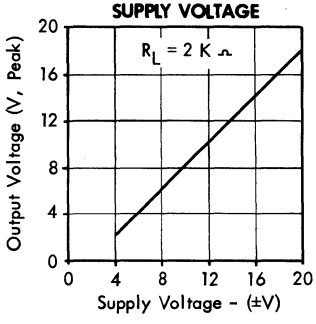
VOLTAGE GAIN vs. SUPPLY VOLTAGE



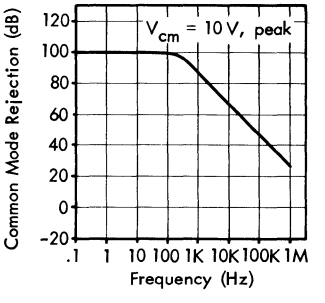
OUTPUT VOLTAGE vs. OUTPUT CURRENT



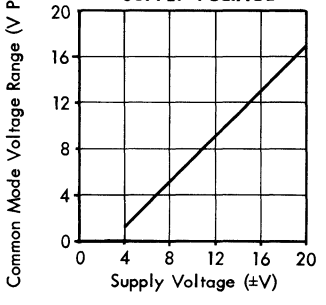
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



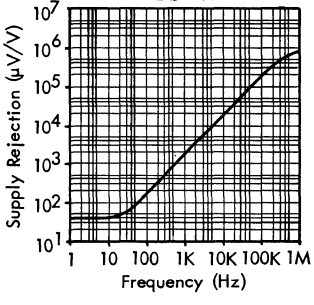
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



APPLICATIONS INFORMATION

OFFSET ADJUSTMENT

The input offset voltage of the Model 3501 may be adjusted to zero by connecting a 50 k Ω potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 1a). This provides an adjustment range of approximately ±10 mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the 3501 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3 μV/°C change of drift for each 1.0 mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers, such as the 3501C, this effect must be considered. By use of a transistor as in Figure 1 the effect of offset adjustment on drift can be substantially reduced (by approximately a factor of six).

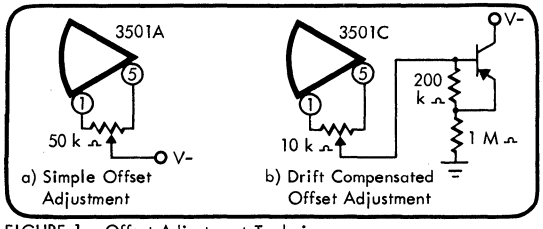


FIGURE 1. Offset Adjustment Techniques.

BIAS CURRENT EFFECTS

Input bias current of the amplifier creates additional offset voltages by flowing in the impedances of the signal source and the feedback network. Although the bias currents of the 3501 are quite small, their effects may be appreciable when these impedances are large. The bias currents at the two inputs tend to be equal and the difference current smaller than either. Thus equalizing the resistance from each input to common, as in Figure 2, is an effective means of reducing DC offset due to bias current.

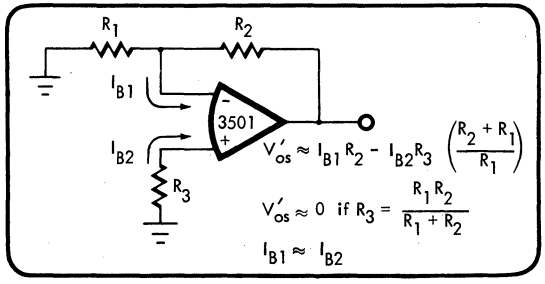


FIGURE 2. Minimization of Bias Current Effects.

OPERATION ON A SINGLE SUPPLY

Although virtually any op amp can be operated on a single supply if input and output voltage limitations are observed, the Model 3501 is particularly suitable for such use. It's wide supply range of ±3 to ±20 Vdc translates to a single supply operating range of 6 to 40 Vdc, plus or minus. Two possible modes of operation on a single supply are shown in Figure 3. The following conditions must be observed to keep the amplifier within its linear region of operation.

1) $+2 < e_o < (V_s - 2)$

2) $+3 < e_s < (V_s - 3)$, Figure 3b

When operating on a single supply (V_s), shorting the output to common is equivalent to a short to supply and the internal power dissipation is approximately twice that which occurs for a short to common with balanced supplies of $\pm \frac{V_s}{2}$. This dissipation may exceed safe limits for single supply voltages greater than 20 volts and must be prevented by use of a series limiting resistor or other device, if short circuit protection is desired.

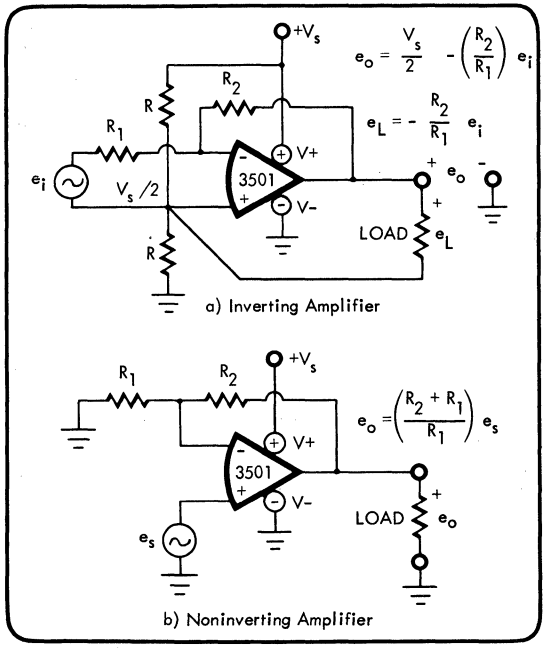


FIGURE 3. Operation on a Single Supply.

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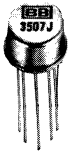

3507J

Fast-Slewing OPERATIONAL AMPLIFIER

FEATURES

- 120V/μsec SLEW RATE
- 20MHz GAIN-BANDWIDTH PRODUCT
- INTERCHANGEABLE WITH 741 TYPES

DESCRIPTION

Burr-Brown model 3507J is intended for use in circuits requiring fast transient response-pulse amplifiers, D/A converters, comparators, fast followers, etc. Key parameters such as slew rate, settling time and bandwidth are orders of magnitude better than for most other IC op amps.

The 3507J is compensated to allow faster slewing and greater bandwidth for gains of 3 or more. For gains greater than 3, the gain rolloff is 6dB/octave. By use of a single external 20pF compensation capacitor the 3507J can be stabilized at all gains including unity. In addition, by use of an alternate compensation technique, it is possible to stabilize the 3507J at unity gain without sacrificing its faster slew rate.

The 3507J is pin-compatible with other standard IC op amps while offering greater speed and higher output current. It also is input- and output-protected to prevent damage if the output is shorted to common, or the input is shorted to supply voltage.

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PDS-297B

SPECIFICATIONS

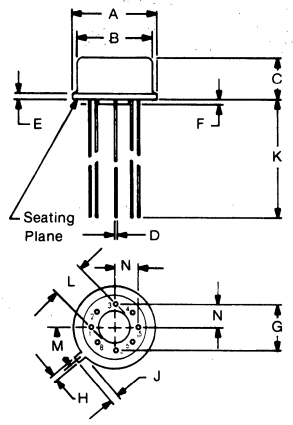
ELECTRICAL

Typical at ±15VDC and +25°C unless otherwise noted.

MODEL	3507J	
	TYPICAL	GUARANTEED
OPEN-LOOP GAIN, DC		
No Load	90dB	
2kΩLoad	83dB	77dB
RATED OUTPUT		
Voltage (1kΩ load)	±12V	±10V
Current	±20mA	±10mA
DYNAMIC RESPONSE		
Small Signal Bandwidth (0dB)	--	
Gain-Bandwidth Product (A_{CL} = 10)	20MHz	
Full Power Bandwidth	1.6MHz	1.2MHz
Slew Rate	120V/μsec	80V/μsec
Settling Time (0.1%)	200nsec	
Rise Time (10-90%, small signal)	25nsec	50nsec
Overshoot	--	--
INPUT OFFSET VOLTAGE		
Initial (without adjust) at +25°C	±5mV	±10mV
Over Temperature		±14mV
(avg. 0°C to +70°C)	±30μV/°C	
vs Supply Voltage	±30μV/V	200μV/V
vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at +25°C	+50nA	+250nA
Over Temperature		+500nA
(avg. 0°C to +70°C)	±0.5nA/°C	
INPUT DIFFERENCE CURRENT		
Initial at +25°C	±20nA	±50nA
Over Temperature		±100nA
(avg. 0°C to +70°C)	±0.1nA/°C	
INPUT IMPEDANCE		
Differential	100MΩ ‖ 3pF	40MΩ
Common-Mode	1000MΩ ‖ 3pF	
INPUT VOLTAGE RANGE		
Common-Mode (linear operation)	±12V	±10V
Differential (between inputs)		±15V
Absolute Max (either input)		±Supply
Common-Mode Rejection	90dB	74dB
POWER SUPPLY		
Rated Voltage		±15VDC
Voltage Range, derated	±8V to ±20V	
Current, quiecscent	±4mA	±6mA
TEMPERATURE RANGE		
Specifications		0°C to +70°C
Operating		-25°C to +85°C
Storage		-65°C to +150°C

MECHANICAL

TO-99 PACKAGE

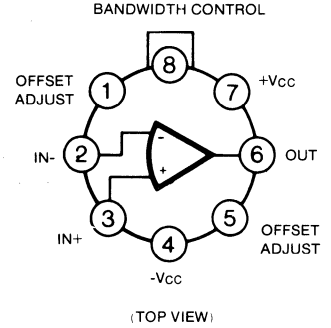


NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM

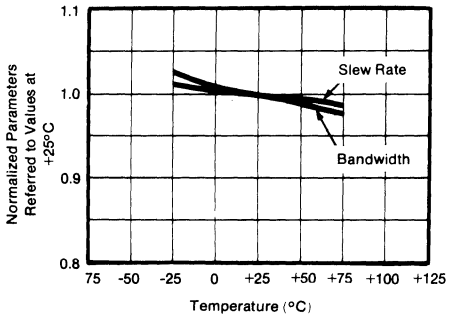


(TOP VIEW)

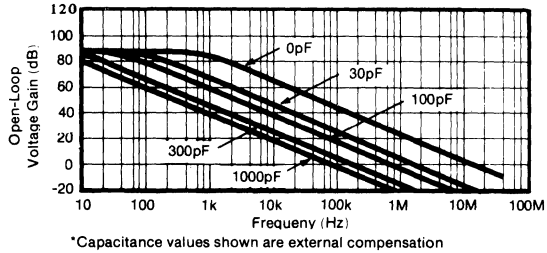
TYPICAL PERFORMANCE CURVES

(At +25°C and ±15VDC, unless otherwise specified)

NORMALIZED AC PARAMETERS
VS TEMPERATURE

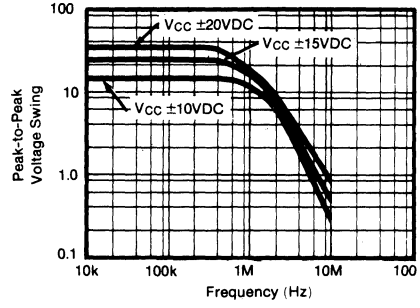


OPEN-LOOP FREQUENCY RESONSE*



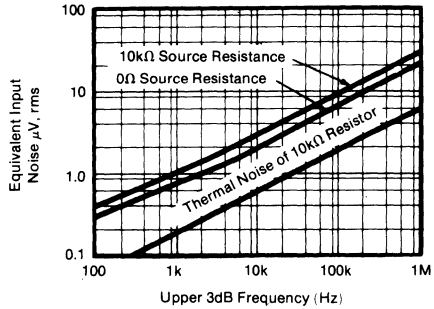
*Capacitance values shown are external compensation from pin 8 to Common.

OUTPUT VOLTAGE SWING
VS FREQUENCY*

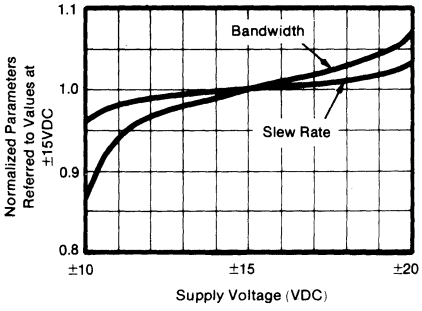


*With no external compensation capacitance.

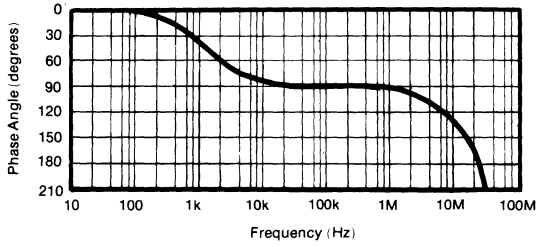
EQUIVALENT INPUT NOISE
VS BANDWIDTH



NORMALIZED AC PARAMETERS
VS SUPPLY VOLTAGE AT +25°C



OPEN-LOOP PHASE RESPONSE



APPLICATIONS

BANDWIDTH COMPENSATION

The frequency response of the 3507J can be adjusted by use of an external compensation capacitor from pin 8 to common, as shown in Figure 1. The open-loop frequency response curves illustrate the effect of various values of capacitance. The 3507J is stable for gains of 3 or greater without external compensation (subject to the same limits on stray and load capacitance and resistance levels). A 20pF compensation capacitor will stabilize the 3507J for all values of gain, at the sacrifice of bandwidth and slew rate.

The circuit of Figure 2 illustrates another approach to compensation of the 3507J. This method yields unity gain stability without sacrificing slew rate.

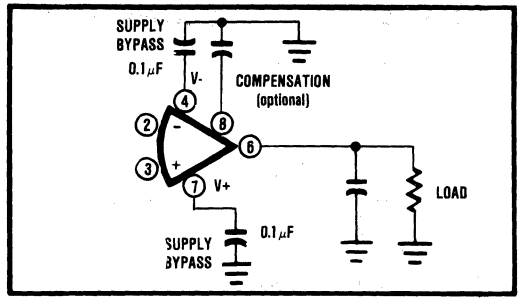


FIGURE 1. Compensated Amplifier with Supply and Load Bypassing.

STABILITY

Because the 3507J is an extremely fast amplifier with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly by-passing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50pF capacitor; see Figure 1.

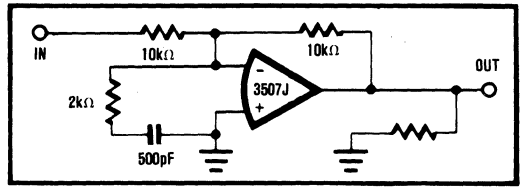


FIGURE 2. Alternate Method for Unity - Gain Compensation of 3507J.

OFFSET VOLTAGE ADJUSTMENT

Although the offset voltage of this amplifier is only a few millivolts, it may be desirable in some cases to null this offset. This is done by use of a 20kΩ potentiometer as shown in Figure 3.

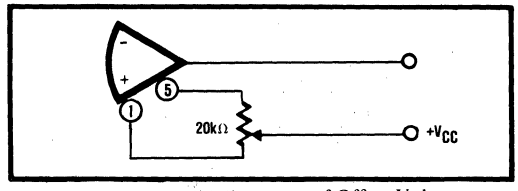


FIGURE 3. External Adjustment of Offset Voltage.

TEST CIRCUIT - DYNAMIC RESPONSE

The test circuits of Figure 4 are used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured under small signal conditions (V_{OUT} = ±200mV). Slew rate and settling time are measured for a 10V, p-p, square wave.

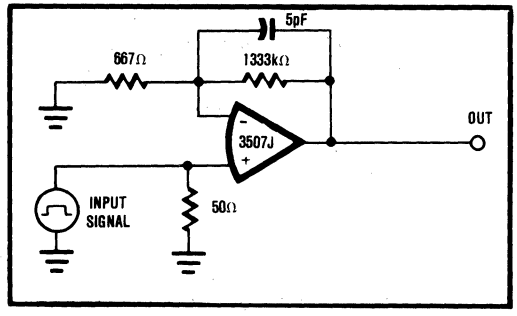


FIGURE 4. Dynamic Response Test Circuits.

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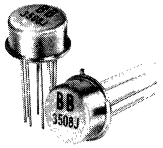

3508J

Wideband OPERATIONAL AMPLIFIER

FEATURES

- 100mHz GAIN BANDWIDTH PRODUCT
- 5nA INPUT BIAS CURENT
- 103dB OPEN-LOOP GAIN
- INTERCHANGEABLE WITH 741 TYPES

DESCRIPTION

Burr-Brown model 3508J is a wideband operational amplifier intended for use in circuits requiring extended bandwidth and high gain. Typical examples of applications are: RF signal amplifiers, fast recovery voltage references, high speed integrators, high frequency active filters, and photodiode amplifiers.

Model 3508J is internally compensated for stability at gains greater than five. The 3508J can be externallv compensated by use of a single capacitor, and can thus be stabilized at any value of gain. By use of an alternate compensation scheme the 3508J can be stabilized at unity gain without sacrificing slew rate.

In addition to its wide bandwidth and high gain the amplifier has a number of other significant advantages over other IC op amps; low bias current, high output current, and high common-mode rejection. Inputs are protected against voltages up to the value of the power supplies. The output is current-limited to provide short-circuit protection.

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PDS-298B

SPECIFICATIONS

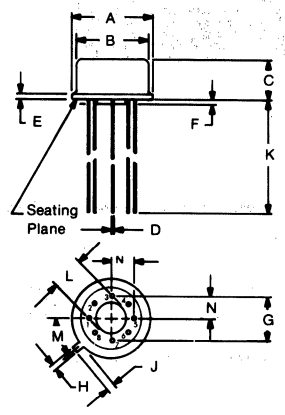
ELECTRICAL

Typical at ±15VDC and +25°C unless otherwise noted.

MODEL	3508J	
	TYPICAL	GUARANTEED
OPEN-LOOP GAIN, DC		
No Load	106dB	
2kΩLoad	103dB	98dB
RATED OUTPUT		
Voltage	±12V	±10V
Current	±18mA	±10mA
DYNAMIC RESPONSE		
Small Signal Bandwidth (0dB)	--	
Gain-Bandwidth Product (A_{CL} = 10)	100MHz	
Full Power Bandwidth	600kHz	320kHz
Slew Rate	35V/μsec	20V/μsec
Settling Time (0.1%)	--	--
Rise Time (10-90%, small signal)	17nsec	45nsec
Overshoot	--	--
INPUT OFFSET VOLTAGE		
Initial (without adjust) at +25°C	±3mV	±5mV
Over Temperature		±7mV
(avg. 0°C to +70°C)	±30μV/°C	
vs Supply Voltage	±30μV/V	200μV/V
vs Time	±50μV/mo	
INPUT BIAS CURRENT		
Initial at +25°C	+15nA	+25nA
Over Temperature		+40nA
(avg. 0°C to +70°C)	±0.5nA/°C	
INPUT DIFFERENCE CURRENT		
Initial at +25°C	±5nA	±25nA
Over Temperature		±40nA
(avg. 0°C to +70°C)	±0.2nA/°C	
INPUT IMPEDANCE		
Differential	300MΩ || 3pF	40MΩ
Common-Mode	1000MΩ || 3pF	
INPUT VOLTAGE RANGE		
Common-Mode (linear operation)	±13V	±11V
Differential-Mode (between inputs)		±12V
Absolute Max (either input)		±Supply
Common-Mode Rejection	100dB	74dB
POWER SUPPLY		
Rated Voltage		±15VDC
Voltage Range, derated	±8V to ±22V	
Current, quiecscent	±3mA	±4mA
TEMPERATURE RANGE		
Specifications		0°C to +70°C
Operating		-25°C to +85°C
Storage		-65°C to +150°C

MECHANICAL

TO-99 PACKAGE

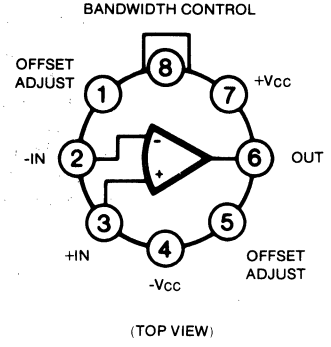


NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM

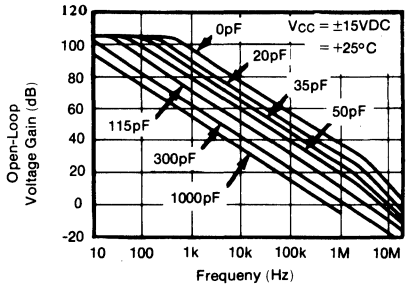


(TOP VIEW)

TYPICAL PERFORMANCE CURVES

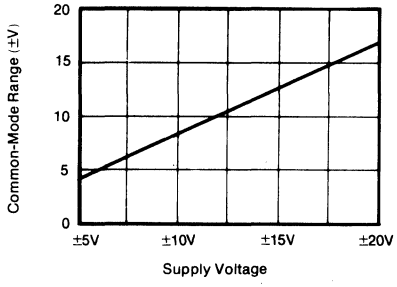
(At +25°C and ±15VDC, unless otherwise specified)

OPEN-LOOP FREQUENCY RESONSE*

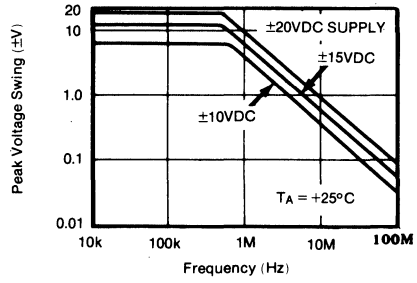


*Capacitance values shown are external compensation from pin 8 to Common.

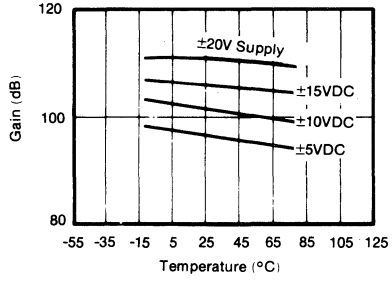
COMMON-MODE VOLTAGE RANGE VS SUPPLY VOLTAGE



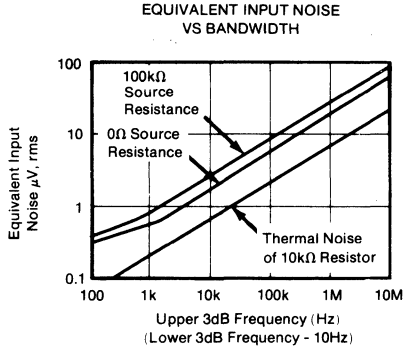
OUTPUT VOLTAGE SWING VS FREQUENCY*



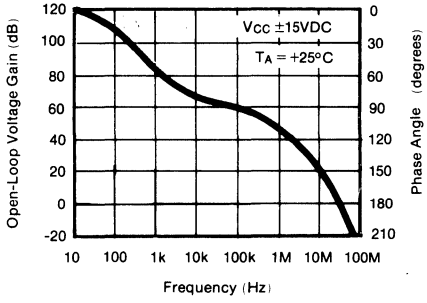
OPEN-LOOP VOLTAGE GAIN VS TEMPERATURE



EQUIVALENT INPUT NOISE VS BANDWIDTH



OPEN-LOOP GAIN AND PHASE ANGLE VS FREQUENCY



APPLICATIONS

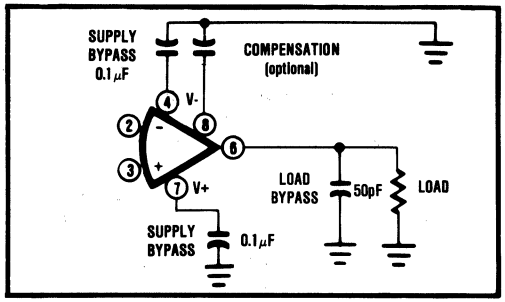


FIGURE 1. Compensated Amplifier with Supply and Load Bypassing.

BANDWIDTH COMPENSATION

The frequency response of the 3508J can be adjusted by use of an external compensation capacitor from pin 8 to common as shown in Figure 1. The open-loop frequency response curves included in the Typical Performance Curves illustrate the effect of various values of capacitance. The 3508J is stable for gains of 5 or greater without external compensation (subject to the same limits on stray and load capacitance and resistance levels). A 20pF compensation capacitor will stabilize the 3508J for all values of gain, at the sacrifice of bandwidth and slew rate.

The circuit of Figure 2 illustrates another approach to compensation of the 3508J. This method yields unity gain stability without sacrificing slew rate.

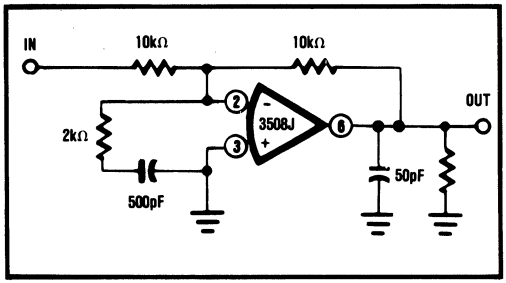


FIGURE 2. Alternate Method for Unity - Gain Compensation of 3508J.

STABILITY

Because the 3508J is an extremely fast amplifier with high gain, stray wiring capacitance and inductance in power supply leads can cause circuit oscillation. This can be prevented by proper circuit layout (all leads or patterns as short as possible) and by properly bypassing the power supply lines to common at points close to the amplifier. In addition, it is recommended that the load be bypassed by a 50pF capacitor; (see Figure 1).

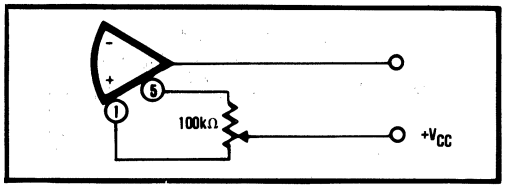


FIGURE 3. External Adjustment of Offset Voltage.

OFFSET VOLTAGE ADJUSTMENT

Although the offset voltage of this amplifier is only a few millivolts, it may be desirable in some cases to null this offset. This is done by use of a 100kΩ potentiometer as shown in Figure 3.

TEST CIRCUIT - DYNAMIC RESPONSE

The test circuits of Figure 4 are used for measurement of slew rate, settling time, rise time and overshoot. Both rise time and overshoot are measured for a small output signal ($V_{OUT} = \pm 100mV$). Slew rate and settling time are measured for a 10V, p-p, square wave.

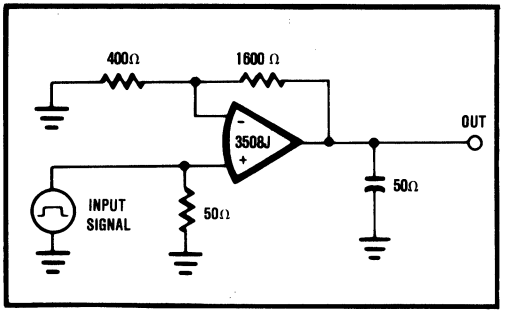


FIGURE 4. Dynamic Response Test Circuits.

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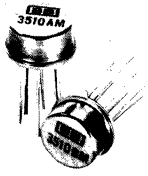


3510

Very-Low Drift - Precision OPERATIONAL AMPLIFIER

FEATURES

- VERY-LOW DRIFT - ±0.5µV/°C max
- VERY-LOW OFFSET - ±60µV max
- LOW BIAS CURRENT - ±15nA max
- HIGH OPEN-LOOP GAIN - 120dB min
- HIGH CMR - 110dB min
- VERY-LOW THERMAL FEEDBACK - ±0.1µV/V

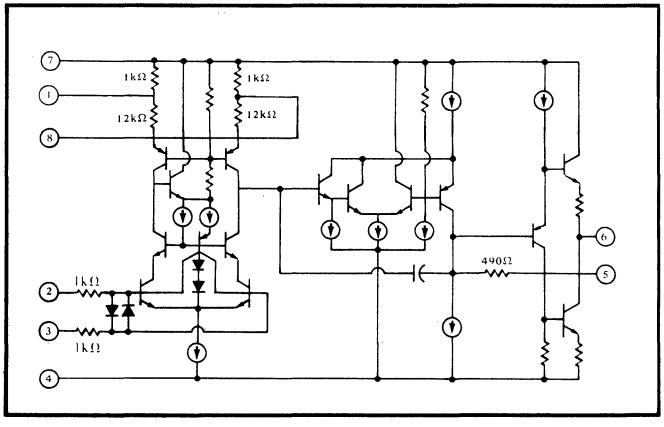
DESCRIPTION

High overall accuracy is offered by Burr-Brown's 3510 Operational Amplifier. It's designed expressly for use in high gain analog circuits where very-low drift and high accuracy are essential requirements.

This precision instrumentation grade op amp provides an economical method to maintain high circuit accuracy and reliability over temperature ranges from -25°C to +85°C, surpassing competitive units rated for only 0°C to +70°C.

Additional performance features of the 3510 include high open-loop gain, extremely-low initial offset voltage, high CMR, very-low thermal feedback, low input bias current and very-low voltage drift vs temperature.

Burr-Brown's rigid control of monolithic processing and its rigid quality control standards result in very-low voltage and current noise in the 3510. It's specifically designed for use in low level analog signal processing. Performance specifications are met exactly by precision trimming at the wafer level with complete testing before shipment. Performance of the 3510 significantly exceeds that of Burr-Brown's popular 3500 op amp.



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PDS-374B

ELECTRICAL SPECIFICATIONS

Specifications at T_A = 25°C and ±15VDC, unless otherwise noted. Standard specifications after warm-up.

MODELS	3510AM			3510BM/3510SM			3510CM			UNITS
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN, DC										
2kΩ Load	120			*			*			dB
RATED OUTPUT										
Voltage	±10			*			*			V
Current	±10			*			*			mA
Output Resistance		300			*			*		Ω
Load Capacitance		1000			*			*		pF
FREQUENCY RESPONSE										
Unity Gain, Open Loop, Small Signal C_c = 4700pF		0.4			*			*		MHz
Closed Loop Gain, C_c = 0, Stable Operation		≥10			*			*		V/V
Full Power Response, C_c = 0, A_{CL} = 10	7	12		*	*		*	*		kHz
Slew Rate, C_c = 0, A_{CL} = 10	0.5	0.8		*	*		*	*		V/μs
INPUT OFFSET VOLTAGE										
Initial Offset, 25°C			150			120			60	μV
vs Temp[1] - unnulled V_{os}			2.0			1.0			0.5	μV/°C
vs Temp[1] - nulled V_{os}			2.5			1.4			0.7	μV/°C
vs Time		0.2			*			*		μV/mo
Power Supply Rejection	110	130		*	*		*	*		dB
Thermal Feedback, R_L = 2kΩ, f = 1Hz		±0.1			*			*		μV/V
INPUT BIAS CURRENT										
Initial Bias, 25°C			±35			±25			±15	nA
vs Temp[1]			±0.6			±0.4			±0.25	nA/°C
vs Supply Voltage		±0.1			*			*		nA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, 25°C			±20			±15			±10	nA
vs Temp[1]			±0.4			±0.25			±0.15	nA/°C
vs Supply Voltage		±10			*			*		pA/V
INPUT IMPEDANCE										
Differential		1 ‖ 3			*			*		MΩ ‖ pF
Common-mode		10 ‖ 3			*			*		GΩ ‖ pF
INPUT NOISE										
Voltage, 0.1Hz to 10Hz		0.8			*			*		μV, p-p
f_o = 10 Hz		14			*			*		nV/√Hz
f_o = 100 Hz		12			*			*		nV/√Hz
f_o = 1 kHz		12			*			*		nV/√Hz
Current, 0.1 Hz to 10 Hz		50			*			*		pA, p-p
f_o = 10 Hz		0.8			*			*		pA/√Hz
f_o = 100 Hz		0.46			*			*		pA/√Hz
f_o = 1 kHz		0.35			*			*		pA/√Hz
INPUT VOLTAGE RANGE										
Common-mode Voltage Range, linear operation		±(V_{cc}-3)		*			*			V
Common-mode Rejection at ±10V	110			*			*			dB
Maximum Safe Input Voltage		±V_{cc}			*			*		V
POWER SUPPLY										
Rated Voltage		±15			*			*		V
Voltage Range, derated performance	±3		±20	*		*	*		*	V
Quiescent Current		±2.5	±3.5		*	*		*	*	mA
TEMPERATURE RANGE										
Specification, (A, B, C)	-25		+85	*		*	*		*	°C
, (S)				-55		+125				°C
Operating, derated performance	-55		+125	*		*	*		*	
Storage	-65		+150	*		*	*		*	°C
θ junction-case		40			*			*		°C/W
θ junction-ambient		150			*			*		°C/W

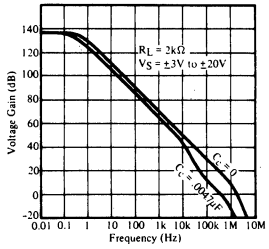
*Specification limits same as 3510AM.

(1) Temperature coefficient specifications: -25°C to +85°C for AM, BM, CM
-55°C to +125°C for SM

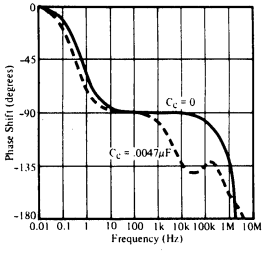
TYPICAL PERFORMANCE CURVES

Typical at T_A = 25°C and ±15VDC, unless otherwise noted.

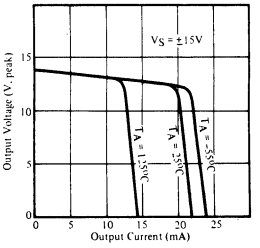
OPEN LOOP FREQUENCY RESPONSE



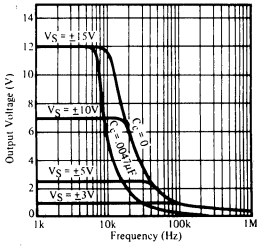
OPEN LOOP PHASE RESPONSE



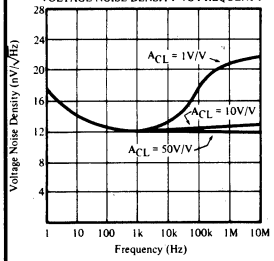
OUTPUT VOLTAGE VS OUTPUT CURRENT



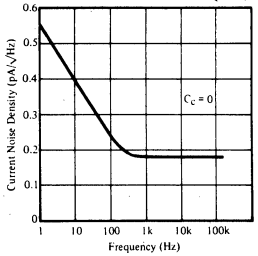
OUTPUT VOLTAGE VS FREQUENCY



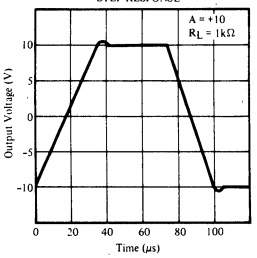
VOLTAGE NOISE DENSITY VS FREQUENCY



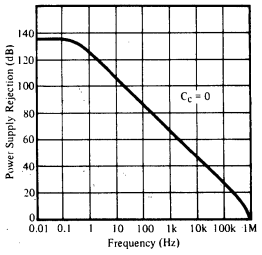
CURRENT NOISE DENSITY VS FREQUENCY



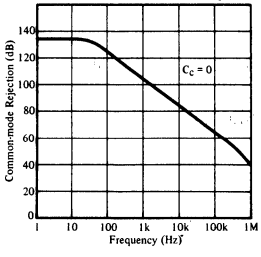
STEP RESPONSE



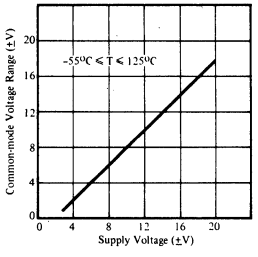
POWER SUPPLY REJECTION VS FREQUENCY



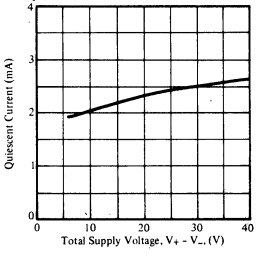
COMMON-MODE REJECTION VS FREQUENCY



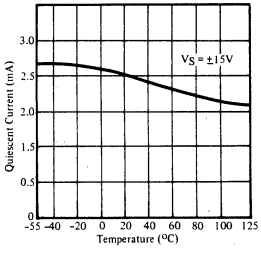
COMMON-MODE RANGE VS SUPPLY VOLTAGE



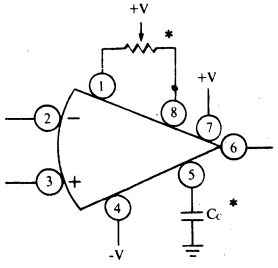
QUIESCENT CURRENT VS SUPPLY VOLTAGE



QUIESCENT CURRENT VS TEMPERATURE

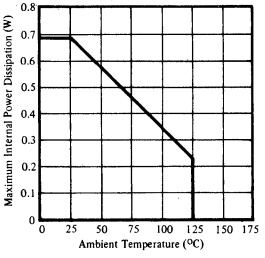


Amplifier Connections

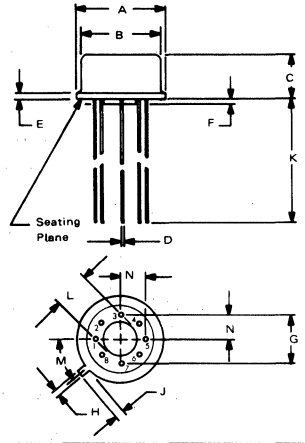


* Optional
See applications information

MAXIMUM POWER DISSIPATION VS. TEMPERATURE



MECHANICAL SPECIFICATIONS



TO-99

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Notes:
1. There is no case connection
2. The case is metalic and is conductive
3. The case and leads are bright acid tin plated

APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT, NULLING AND DRIFT

Unlike some competitive models it is not necessary to null the offset voltage of the 3510 to achieve minimum voltage drift versus temperature. Drift of the 3510 is specified both nulled and unnulled.

In this op amp, the input offset voltage and the input offset voltage drift versus temperature are trimmed, at the wafer level, during manufacture. This feature, combined with the op amp's electrical design and high quality, closely controlled processing produce the low offset voltages and drifts indicated in the specifications. These figures are 100% guaranteed.

Should it be necessary to null the offset voltage to the lowest possible value this can be accomplished by inserting a potentiometer between pins 1 and 8. See "Alternate Nulling Techniques" for other methods. Nulling ultra-low offset amplifiers may, however, be undesirable when these factors are considered:

Cost of potentiometer and labor to install and null.

Decreased reliability through introduction of additional components.

Possible degradation of overall performance due to temperature coefficients of external nulling resistors (not true with 3510).

Nulling the offset voltage of most modern op amps will minimize offset voltage drift. In the 3510, an ultra low offset amplifier, a major portion of the offset voltage is trimmed during manufacture. Additional trimming by the user may increase the voltage drift slightly. Drift changes 0.33μV/°C for each 100μV of offset voltage nulled. Due to second order effects, the point of minimum voltage drift does not occur at the point of zero offset voltage in approximately 25% of the cases. In these instances, nulling the offset voltage may cause a slight increase in voltage drift, but not beyond the guaranteed nulled voltage drift specified. Nulling the offset voltage will decrease the voltage drift in approximately 75% of cases.

ALTERNATE NULLING TECHNIQUES

When it is essential to null offset voltage and achieve the lowest guaranteed voltage drift specifications, the following methods can be used:

Burr-Brown recommends nulling in a following stage as shown in Figure 1.

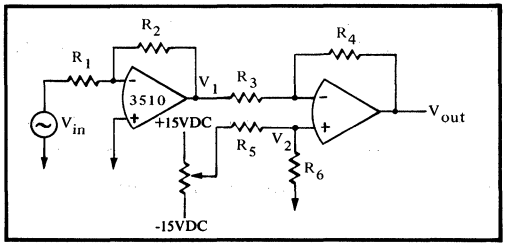


Figure 1. Multistage Nulling Circuit.

In this circuit, with $V_{in} = 0$, V_1 will be due to E_{os} and I_{bias} of 3510. The component of V_{out} due to V_1 is $\frac{V_1 R4}{R3}$. Resistors R_5 and R_6 are selected so that the component of V_{out} due to V_2 will cancel the component of V_{out} due to V_1. The specific values of R_5 and R_6 are selected to provide the desired range and resolution and will depend upon the model of the 3510 involved and the gain in each stage.

When only a single stage of amplification is used the following circuits could be employed.

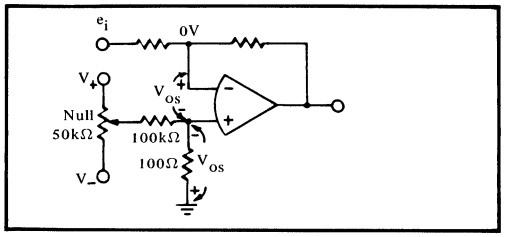


FIGURE 2. Inverting Amplifier

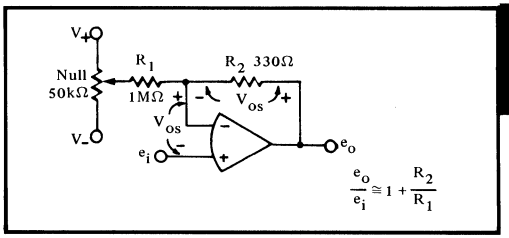


FIGURE 3. Non-Inverting Amplifier

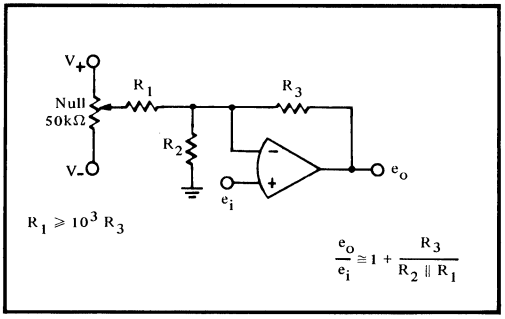


FIGURE 4. Follower Amplifier

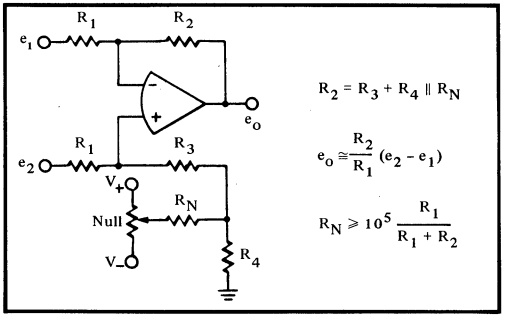


FIGURE 5. Difference Amplifier

RESOLUTION OF NULLING POTENTIOMETER

One of the advantages of the 3510 is the ease of nulling the offset voltage, even with a low cost, single turn potentiometer. A single turn linear potentiometer can be used with good resolution. Unlike some competitive, low offset op amps, the 3510 does not require multiturn pots or fixed resistors padded with a pot to produce a high level of trim resolution.

Resolution and range of the offset trim potentiometer at various resistance values are shown in Table I.

Potentiometer Value	Offset Adjustment Range		Resolution at Pot Center	Sensitivity of $\Delta V_{os}/\Delta T$ to Potentiometer (1) T.C.R. (2)
	10% - 90% Rotation	0% - 100% Rotation		
*100kΩ	±170μV	±2mV	1μV/% rotation	10^{-4}μV/ppm/°C
20kΩ	±600μV	±2mV	3.5μV/% rotation	10^{-4}μV/ppm/°C
10kΩ	±800μV	±2mV	6μV/% rotation	10^{-4}μV/ppm/°C

* Recommended offset adjustment potentiometer.

(1) T.C.R. = temperature coefficient of resistance

(2) Sensitivity after nulling ±120μV of V_{os}; typically the sensitivity is one-half the value shown.

TABLE I. Offset Potentiometer Effects

POTENTIOMETER

Because the external offset 100kΩ potentiometer parallels two internal 1kΩ resistors, the temperature coefficient of the potentiometer will affect the offset voltage temperature drift of the 3510 to a very small degree. In addition, the potentiometer halves have the same temperature coefficient, therefore the percent rotation does not drift. Sensitivity of the offset voltage to the external potentiometer is very low, only 10^{-4}μV/ppm/°C and must be added to the amplifier's drift. However, even when using a 100ppm industrial pot, this figure is ±0.01μV/°C and can be ignored.

THERMAL FEEDBACK

When an amplifier achieves the high performance levels of the 3510 some effects previously masked by larger error terms (and now reduced by the 3510's high accuracy, high performance and low error terms) may become observable. This situation exists with a condition referred to as thermal feedback.

Thermal feedback is an error generating condition which can be caused by the power dissipation and resultant temperature rise of the amplifier's output stage. This error is fed back to a previous stage of the amplifier and alters its usual operation. Normally the input stage is affected. This error is described as a change in input offset voltage per volt of output voltage change. When the 3510 has a 2kΩ load the specification is ±0.1μV/V.

This phenomena is most noticeable at frequencies below a few hertz and most easily observed on an oscilloscope. Thermal feedback can add a small error term to the "average" temperature effects normally described as input offset voltage drift versus temperature and input bias current versus temperature.

To minimize the effect of thermal feedback, the 3510 circuits are carefully laid out and thermally balanced to minimize thermal feedback.

THERMAL RESPONSE TIME

In low drift operational amplifiers like the 3510, thermal response time is an important performance parameter. In precision applications the response of the amplifier to warm-up or environmental change should be considered.

Figure 5 and 7 show typical thermal response of the 3510. Note that the offset voltage does not overshoot and that the response time is very short - less than three minutes. Some competitive low drift operational amplifiers require 15 minutes to warm up.

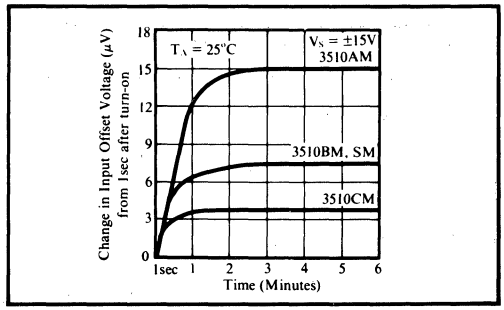


FIGURE 6. Warm-up Drift.

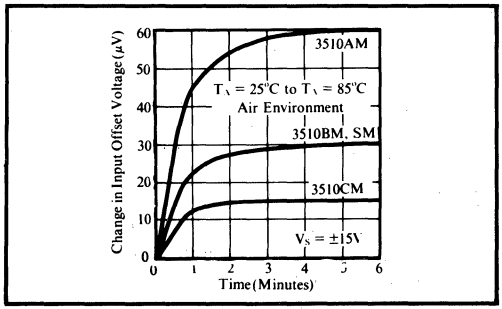


FIGURE 7. Offset Response to an Environmental Change.

NOISE

In a high performance amplifier such as the 3510, noise may well be the final and limiting criteria for system accuracy. See specifications and performance curves.

While the 3510 noise is very acceptable in low and mid-frequencies, it is fairly large above 100kHz. Whether or not this unique characteristic will cause user problems depends on the application of the 3510 and steps taken to reduce high frequency noise effects.

If circuitry following the 3510 does not respond to noise above 100kHz, no corrective steps need to be taken. This situation is common in applications where a 0.5V/μs amplifier is satisfactory. When high frequency noise must be reduced, a low pass filter should be installed in a stage following the 3510 (filtering at the 3510 itself has little effect).

Two high frequency filtering approaches are shown in Figures 8 and 9.

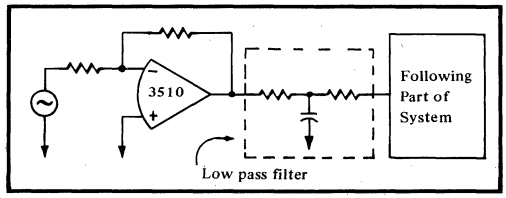


FIGURE 8. High Frequency Filter For Single Stage Amplifier.

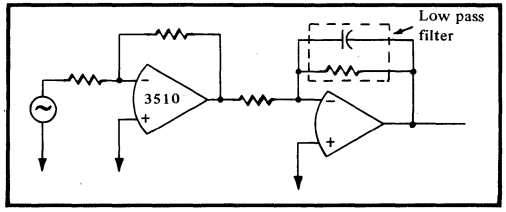


FIGURE 9. High Frequency Filter For Multi-stage Amplifier

COMPENSATION

At closed loop gains above 10V/V, the 3510 op amp is stable without additional frequency compensation. The amplifier is compensated as shown in Figure 10 for gains below 10V/V.

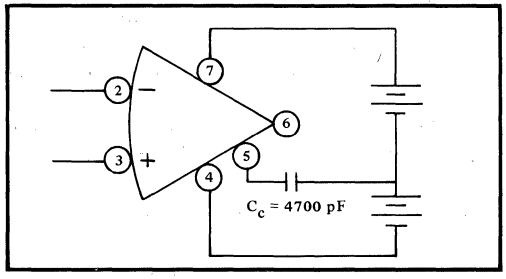


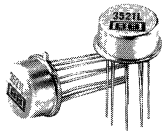
FIGURE 10. Amplifier Compensation Circuit

Alternately, the capacitor may be connected between pin 5 and $+V_{cc}$ (pin 7) if the supply is well bypassed to ground.

SHORT CIRCUIT PROTECTION

The 3510 may be short circuited to ground continuously without damage. Output shorts other than to ground may be tolerated if the "Maximum Power Dissipation vs Temperature" ratings given in the performance curves are not exceeded. Power dissipation can be determined as the product of $(V_{cc} - V_{out})$ X I_{out}. I_{out} under current limit conditions is specified in the "Output Voltage vs Output Current" performance curve.

BURR-BROWN®



3521 SERIES
3522 SERIES

Ultra-Low Drift - FET Input OPERATIONAL AMPLIFIERS

FEATURES

- **ULTRA-LOW DRIFT, 1μV/°C max**
- **LOW INITIAL OFFSET VOLTAGE, 250μV, max**
- **LOW BIAS CURRENT, 1pA, max**
- **LOW NOISE**
- **HIGH COMMON-MODE REJECTION, 90dB, typ**
- **WIDE POWER SUPPLY RANGE, ±5VDC to ±20VDC**

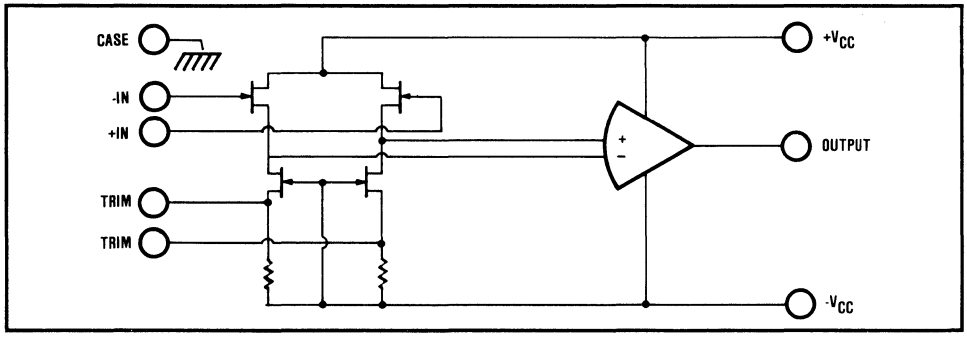
DESCRIPTION

With input offset voltage drifts as low as 1μV/°C, the Burr-Brown 3521 IC Operational Amplifier provides FET input performance combined with drift equal to the best bipolar IC's (e.g., BB3500E). The spectacular performance is achieved through truly state-of-the-art hybrid design and manufacturing, including monolithic FET pairs and active laser-trimming.

The 3521 and 3522 have an exceptionally fast thermal response. This fast warm-up is achieved without any heat-sinking.

While low drift and FET input impedance are the outstanding features of the 3521 and 3522 other specifications have not been compromised. They are internally compensated for unity-gain configuration and the initial voltage offset is guaranteed less than 250μV so for most applications the 3521 is ready to "plug-in and go." Like other low drift IC's from Burr-Brown the 3521 and 3522 have ample speed and bandwidth for most any application. (Slew rate = 0.6V/μsec). The high common-mode rejection ratio (90dB, typ.) enables them to be used as a 0.01% accurate buffer with low drift and extremely-high input impedance. The 3521/3522 also have very-low input noise to complement the low drift. The output is current limited to provide protection for continuous output shorts to common.

The 3521/3522 are pin-compatible with 741-type amplifiers, but provide FET input performance with ultra-low drift while exceeding all other specifications for general purpose operational amplifiers of the 741-type. Burr-Brown tests and guarantees all units to meet all max/min specifications.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-472

SPECIFICATIONS

ELECTRICAL

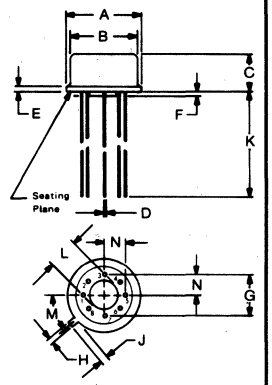
Typical at +25°C and ±15VDC power supply unless otherwise noted.

MODELS	3521H	3521J	3521K	3521L	3521R
OPEN-LOOP GAIN, DC					
Rated Load, min	94dB	*	*	*	*
RATED OUTPUT					
Voltage, min	+10V	*	*	*	*
Current, min	±10mA	*	*	*	*
Output Impedance	100Ω	*	*	*	*
FREQUENCY RESPONSE					
Unity Gain, Open-Loop	1.5MHz	*	*	*	*
Full Power Response, min	10kHz	*	*	*	*
Slew Rate, min	0.6V/μsec	*	*	*	*
INPUT OFFSET VOLTAGE					
Initial Offset, 25°C, max	±500μV	250μV	250μV	250μV	250μV
vs Temp (0°C to +70°C), **max	±10μV/°C	±5μV/°C	2μV/°C	±1μV/°C	±5μV/°C
vs Temp (-25°C to +85°C)	±15μV/°C	±8μV/°C	±4μV/°C	±2μV/°C	±2μV/°C
vs Supply Voltage	±25μV/V	*	*	*	*
vs Time	5μV/mo	*	*	*	*
INPUT BIAS CURRENT					
Initial Bias, 25°C, max	-20pA	*	-15pA	-10pA	*
(doubles every +10°C)					
vs Supply Voltage	1pA/V	*	*	*	*
INPUT DIFFERENCE CURRENT					
Initial difference, 25°C	±2pA	*	*	*	*
INPUT IMPEDANCE					
Differential	$10^{11}\Omega$	*	*	*	*
Common-mode	$10^{12}\Omega$	*	*	*	*
INPUT NOISE					
Voltage, 0.01Hz - 10Hz, p-p	4μV	*	*	*	*
Voltage, 10Hz - 1kHz, rms	2μV	*	*	*	*
Current, 0.01Hz - 10Hz, p-p	0.3pA	*	*	*	*
Current, 10Hz - 1kHz, rms	0.6pA	*	*	*	*
INPUT VOLTAGE RANGE					
Common-mode Voltage	±10V	*	*	*	*
Common-mode Rejection	90dB	*	*	*	*
Max. Safe Input Voltage	±Supply	*	*	*	*
POWER SUPPLY					
Rated Voltage	±15VDC	*	*	*	*
Voltage Range, derated	±5 to ±20VDC	*	*	*	*
Current, quiescent	±4mA	*	*	*	*
TEMPERATURE RANGE					
Specification	0°C to +70°C	*	*	*	-55°C to +125°C
Operating	-25°C to +85°C	*	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*	*

*Specification same as for 3521H.
**-55°C to +125°C for 3521R.

MECHANICAL

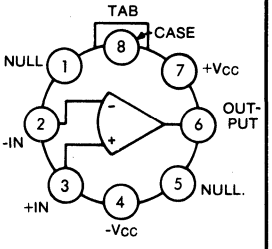
(TO-99 PACKAGE)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

CONNECTION DIAGRAM

(TOP VIEW)



ELECTRICAL (CONT)

Typical at +25°C and ±15VDC power supply unless otherwise noted.

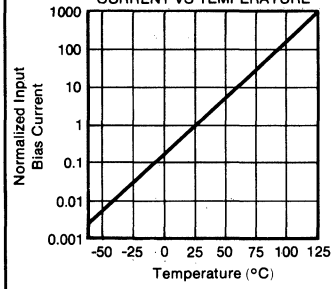
MODELS	3522J	3522K	3522L	3522S
OPEN-LOOP GAIN, DC				
Rated Load, min	94dB	*	*	*
RATED OUTPUT				
Voltage, min	±10V	*	*	*
Current, min	±10mA	*	*	*
Output Impedance	100Ω	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Open-loop	1MHz	*	*	*
Full Power Response, min	10kHz	*	*	*
Slew Rate, min	0.6V/μsec	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, 25°C, max	±1mV	±500μV	±500μV	±500μV
vs Temp (0°C to +70°C), max	±50μV/°C	±10μV/°C	±10μV/°C	
(-55°C to +125°C), max				±25μV/°C
vs Supply Voltage	±25μV/mo	*	*	*
vs Time	±10μV/mo	*	*	*
INPUT BIAS CURRENT**				
Input Bias, 25°C, max	-10pA	-5pA	-1pA	-5pA
(doubles every +10°C)				
vs Supply Voltage	±0.1pA/V	*	*	*
INPUT DIFFERENCE CURRENT				
Initial Difference, +25°C	±2pA	±1pA	±0.5pA	±1pA
INPUT IMPEDANCE				
Differential	$10^{11}\Omega$	*	*	*
Common-mode	$10^{12}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.01Hz to 10Hz, p-p	4μV	*	*	*
Voltage, 10Hz to 1kHz, rms	2μV	*	*	*
Current, 0.01Hz to 10Hz, p-p	0.3pA	*	*	*
Current, 10Hz to 1kHz, rms	0.6pA	*	*	*
INPUT VOLTAGE RANGE				
Common-mode Voltage	±10V	*	*	*
Common-mode Rejection	90dB	*	*	*
Max. Safe Input Voltage	±Supply	*	*	*
POWER SUPPLY				
Rated Voltage	±15VDC	*	*	*
Voltage Range, derated	±5VDC to ±20VDC	*	*	*
Current, quiescent	±4mA	*	*	*
TEMPERATURE RANGE				
Specification	0°C to +70°C	*	*	-55°C to +125°C
Operating	-25°C to +85°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*

*Specification same as for 3522J.
**After Warm-Up.

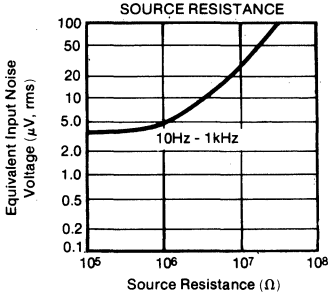
TYPICAL PERFORMANCE CURVES

(At +25°C and ±15VDC unless otherwise specified)

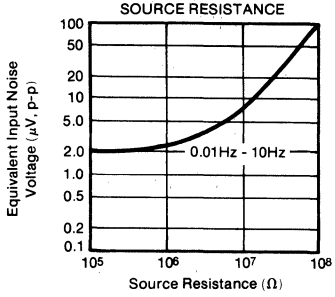
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



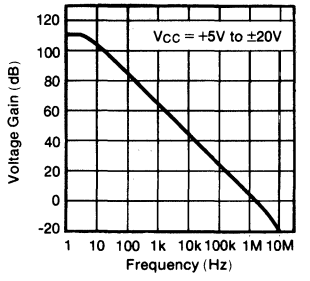
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



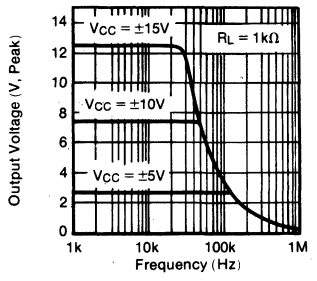
P-P INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



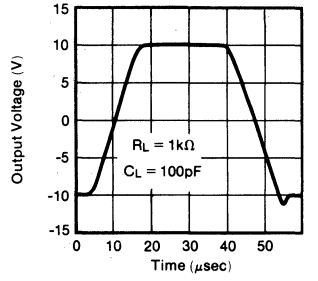
OPEN-LOOP FREQUENCY RESPONSE



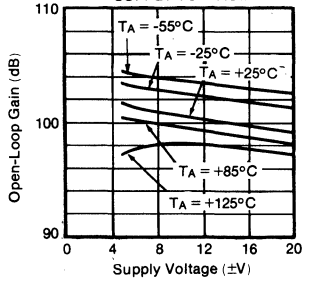
OUTPUT VOLTAGE VS FREQUENCY



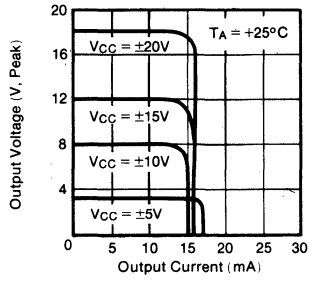
VOLTAGE FOLLOWER STEP RESPONSE



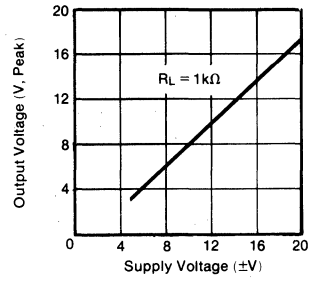
VOLTAGE GAIN VS SUPPLY VOLTAGE



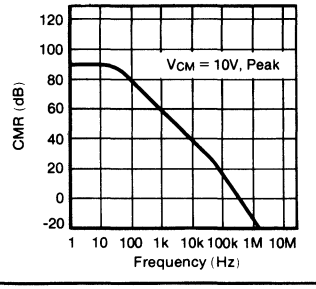
OUTPUT VOLTAGE VS OUTPUT CURRENT



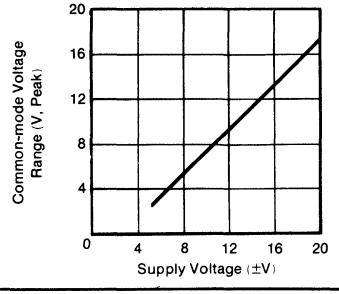
OUTPUT VOLTAGE VS SUPPLY VOLTAGE



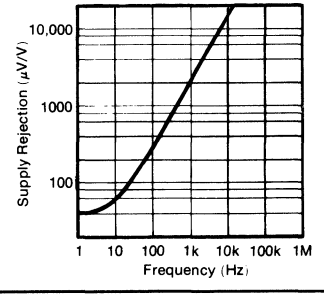
COMMON-MODE REJECTION VS FREQUENCY



COMMON-MODE RANGE VS SUPPLY VOLTAGE



POWER SUPPLY REJECTION VS FREQUENCY



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the 3521/3522. A low drift specification would be of little value if the amplifier took several hours to stabilize after turn-on or ambient temperature change. The TO-99 packaging is particularly well suited for devices requiring fast thermal response. Figure 1 shows the typical warm-up drift of the 3521. Note that the offset voltage has stabilized in less than 4 minutes. Similar warm-up times for some discrete low drift operational amplifiers range from 7 to 15 minutes.

Offset voltage response to thermal shock can provide some real suprises, particularly for amplifiers packaged in discrete modules. Again the TO-99 package proves superior. Figure 2 shows that the response to thermal shock settles very quickly. The 3521/3522 quickly and smoothly assumes a new value of offset voltage as dictated by the drift specification.

BIAS CURRENT EFFECTS

The low bias currents and offset currents of FET input stages overcome most of the source resistance limitations of bipolar operational amplifiers. However, for very large source resistances or large unbalances in source resistance (5MΩ and up) the input offset voltage and drift will be affected as shown in Figures 3 and 4.

COMMON-MODE PROPERTIES

The input stage of the 3521 is a monolithic FET pair, which affords very good matching between the two input transistors. This close matching makes the 90dB common-mode rejection ratio (CMRR) possible. Because of its excellent common-mode properties the 3521 may be used as a 0.01% accurate buffer amplifier for inputs between ±10V. Figure 5 below illustrates typical common-mode performance of the 3521.

POWER SUPPLIES AND DRIFTS

Note that a power supply change of 40mV will typically introduce an input offset voltage change of 1μV. Since power supply drift will have the same effect as offset voltage drift, the power supply temperature coefficients of ±15V supplies should be about 0.1%/°C for optimum drift performance of the 3521L.

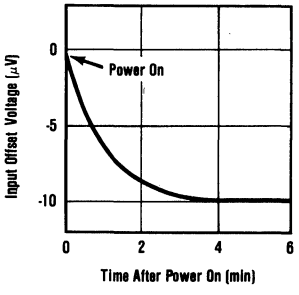


FIGURE 1. Typical Warm-up Drift.

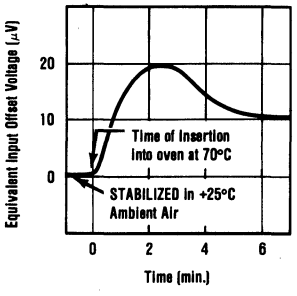
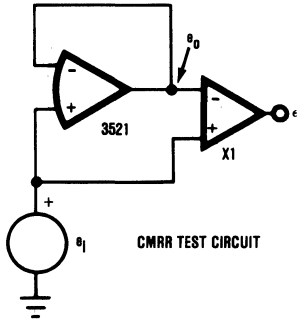


FIGURE 2. Effect of Thermal Shock on Offset Voltage.



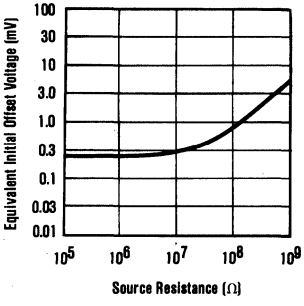


FIGURE 3. Typical Effects of Source Resistance on Initial Offset Voltage.

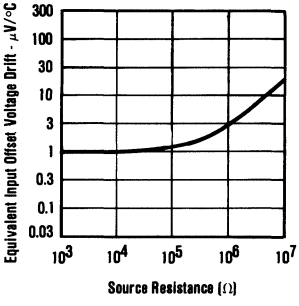


FIGURE 4. Typical Effects of Source Resistance on Equivalent Input Offset Voltage Drift.

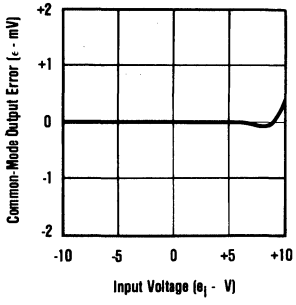


FIGURE 5. Common-Mode Performance.

WIRING CONSIDERATIONS (Shielding and Guarding)

The ultra-low drift, very-low bias current and high input impedance make the 3521/3522 well suited to a number of unique applications. However, careless signal wiring can degrade "system" performance several orders of magnitude below the 3521/3522 capability.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large value feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the units. Perhaps more important, unbalanced leakage paths (when is leakage ever balanced?) can generate significant input offset voltages when large source impedances (100kΩ and up) are involved. To avoid leakage problems, it is recommended that the inputs of the 3521 be wired to teflon standoffs. If the unit must be soldered directly into a printed circuit board, utmost care should be used in designing the board layout. A "guard" pattern should completely surround the two input leads and be connected to a low impedance point at the common-mode input voltage. Figure 6 shows suggested guard connections for various amplifier feedback configurations. The amplifier case should be connected to any input shield or guard via pin 8.

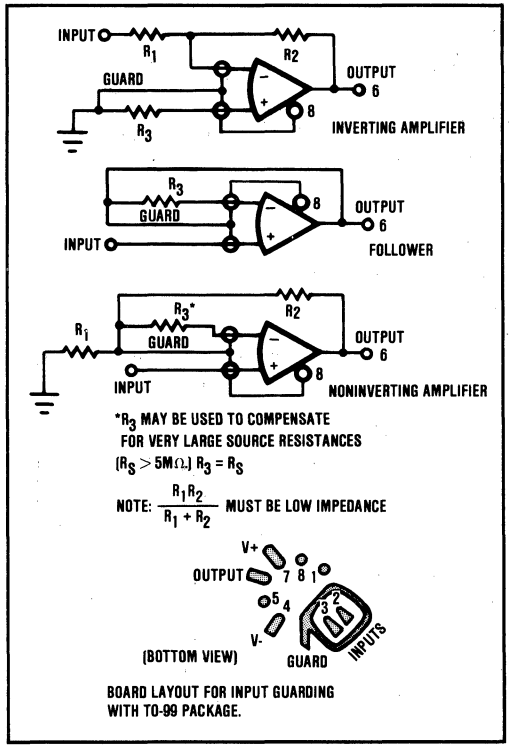


FIGURE 6. Connection of Input Guard.

OFFSET VOLTAGE ADJUSTMENT

The 3521 has a low initial offset (250μV) compatible with its low drift. However, some high accuracy applications may require external nulling of even this small initial offset voltage. Virtually any offset voltage adjustment method can increase offset voltage drift unless some care is used. For example, the initial offset voltage of most monolithic op amps (BB 3500, 741-types, 101, etc.) may be nulled using a single potentiometer, but offset voltage drift is typically increased by about 3μV/°C for each mV of offset voltage adjust. This same relationship will also hold for the 3521.

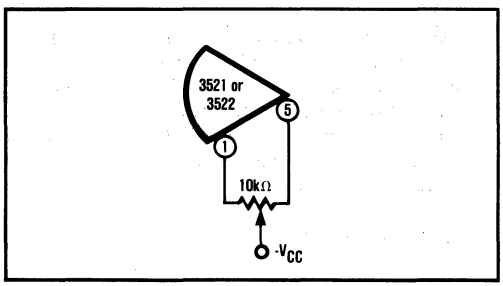


FIGURE 7. Single Potentiometer Adjust at Op Amp Trim Terminals.

Advantages:

1. Simplest circuit.
2. Compatible with most IC op amps.

Disadvantages:

1. Drift increased by circuit about 0.75μV/°C for 3521.

TEMPERATURE COMPENSATED POTENTIOMETER OFFSET VOLTAGE ADJUST

If the circuit in Figure 7 is replaced with a circuit which "drifts" with temperature, nulling the offset voltage will not increase the drift by so large an amount. The circuit shown in Figure 8 may be used to null initial offset voltage and drift will increase only about 0.5μV/°C for each mV of offset adjust. In the case of the 3521, this zeroing circuit will typically add at most 0.14μV/°C.

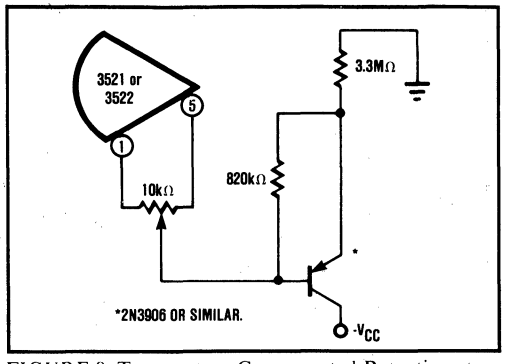
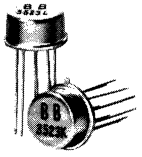


FIGURE 8. Temperature Compensated Potentiometer Null.

BURR-BROWN®

3523 SERIES



Ultra-Low Bias Current FET OPERATIONAL AMPLIFIERS

FEATURES

- BIAS CURRENT, 0.1pA, max
- OFFSET VOLTAGE, 500μV, max
- VOLTAGE DRIFT, 25μV/°C, max
- INPUT IMPEDANCE, $10^{13}\Omega$
- Noise (10Hz), 0.003pA, p-p

DESCRIPTION

The Burr-Brown 3523 Series amplifiers are the first IC operational amplifiers to achieve sub-picoampere input currents without exhibiting excessive offset voltage, voltage drift and voltage noise. The high common-mode rejection, ultra-low bias current, and $10^{13}\Omega$ input impedance of the 3523 make it the best choice for a variety of buffer and electrometer applications. These include pH measurement, photocurrent amplification, long term integration, and low droop sample/hold or track/hold applications. Because its input offset voltage is laser-trimmed to less than 500μV, the 3523 can usually be used without offset nulling. This is a distinct advantage in applications where it is desired to locate the 3523 near the signal source (e.g., in a signal probe).

The package of the 3523 is designed to preserve its ability to measure ultra-low currents and to avoid noise pickup. The case guard (pin no. 8) may be connected to a point which is at signal potential. This minimizes leakage current input from pins to case. Also, it shields the amplifier's sensitive input circuitry from power line frequency "hum", switching transients, and other sources of electrical noise.

Bias current specifications of the 3523 are guaranteed after warm-up in ambient air with no heat sink. Thus, the ultra-low bias current specifications become even more significant since internal power dissipation can easily raise case temperature by 20°C in many applications.

The bias current on many FET amplifiers is a strong function of applied common-mode voltage. This is not the case with the 3523. The input stage design of the 3523 make the input bias current virtually independent of the common-mode voltage over its full range.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-309C

SPECIFICATIONS

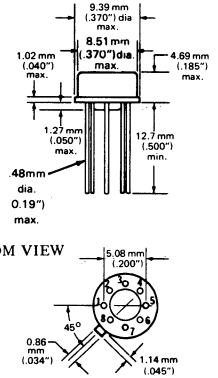
Specifications typical at 25°C and ±15 Vdc Power Supply unless otherwise noted.

ELECTRICAL

MODELS	3523J	3523K	3523L
OPEN LOOP GAIN, dc no load		100 dB	
1 kΩ, load, min		94 dB	
RATED OUTPUT			
Voltage, min		±10 V	
Current min		±10 mA	
Output Impedance		100 Ω	
FREQUENCY RESPONSE			
Unity Gain, Open Loop		1 MHz	
Full Power Response, min		10 kHz	
Slew Rate, min		0.6 V/μsec	
INPUT OFFSET VOLTAGE			
Initial Offset, 25°C, max	±1 mV	±500 μV	±500 μV
vs. Temp (0° to 70°C), max	±50 μV/°C	±25 μV/°C	±25 μV/°C
vs. Supply Voltage		±25 μV/V	
vs. Time		±5 μV/mo	
INPUT BIAS CURRENT			
Initial bias, 25°C, max	-0.5 pA	-0.25 pA	-0.1 pA
(doubles every +10°C)			
vs. Supply Voltage		±0.01 pA/V	
INPUT DIFFERENCE CURRENT			
Initial difference, 25°C	±0.2 pA	±0.1 pA	±0.05 pA
INPUT IMPEDANCE			
Differential		10^{12} Ω	
Common Mode		10^{13} Ω	
INPUT NOISE			
Voltage, .01 Hz - 10 Hz, p-p		4 μV	
10 Hz - 10 kHz, rms		2 μV	
Current, .01 Hz - 10 Hz, p-p		.003 pA	
10 Hz - 10 kHz, rms		0.01 pA	
INPUT VOLTAGE RANGE			
Common Mode Voltage		±(|V_S|-2) V	
Common Mode Rejection @ 10V		80 dB	
Max. Safe Input Voltage		± Supply	
POWER SUPPLY			
Rated Voltage		±15 Vdc	
Voltage Range, derated		±5 to ±20 Vdc	
Current, quiescent		±4 mA	
TEMPERATURE RANGE			
Specification		0° to +70°C	
Operating		-55° to +125°	
Storage		-65° to +150°C	

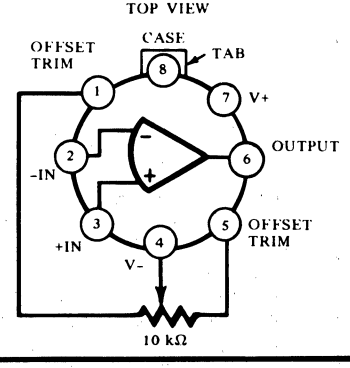
MECHANICAL

TO-99

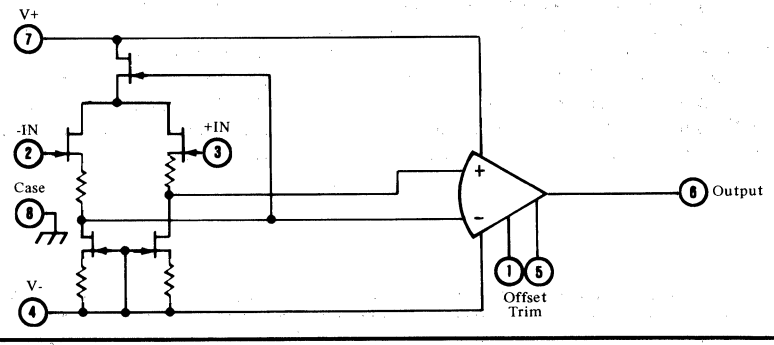


Dimensions in inches are in parentheses. Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

CONNECTION DIAGRAM



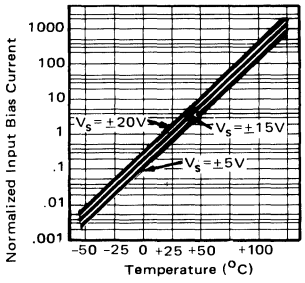
SIMPLIFIED SCHEMATIC



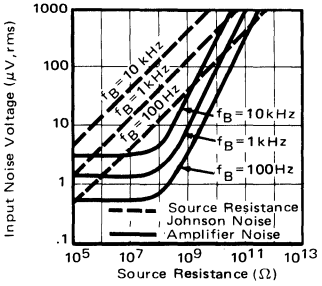
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

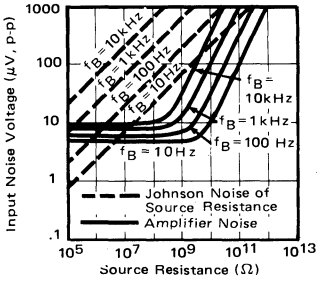
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



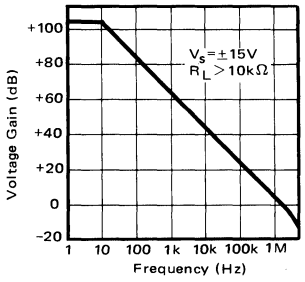
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



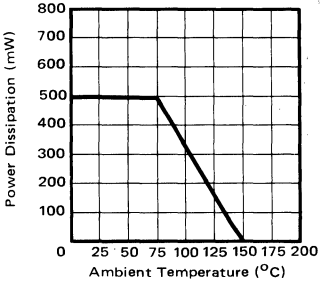
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



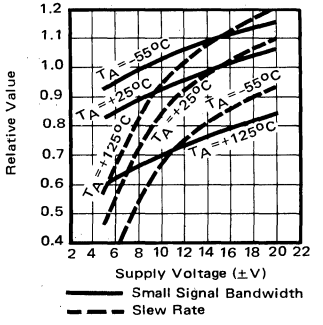
OPEN LOOP FREQUENCY REPONSE



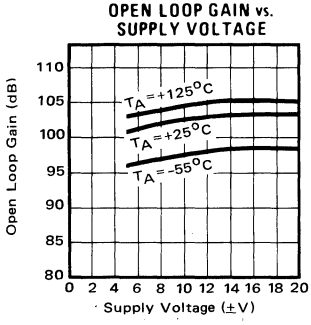
MAXIMUM POWER DISSIPATION



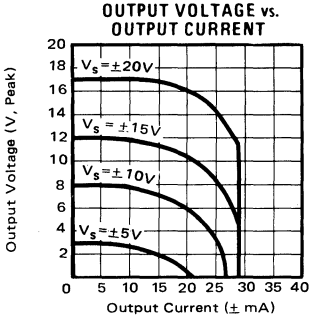
FREQUENCY CHARACTERISTICS vs. SUPPLY VOLTAGE



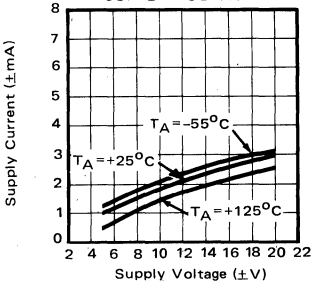
OPEN LOOP GAIN vs. SUPPLY VOLTAGE



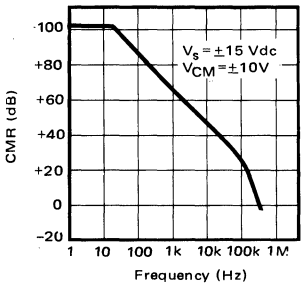
OUTPUT VOLTAGE vs. OUTPUT CURRENT



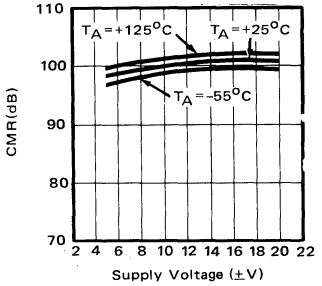
SUPPLY CURRENT vs. SUPPLY VOLTAGE



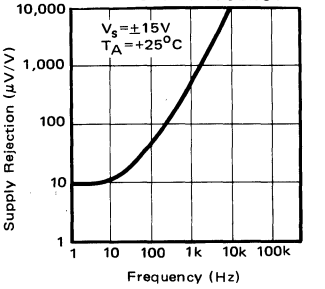
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE REJECTION vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



APPLICATION CONSIDERATIONS

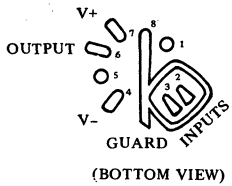
The ultra-low bias current and high input impedance of the 3523 are well suited to a number of challenging applications. In order to fully benefit from the outstanding specifications of this unit careful layout, shielding and guarding is required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the 3523.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the 3523 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pick-up.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3523. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the 3523 be wired to a Telfon standoff. If this is not done and instead the 3523 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential. (See Figure 1) The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents.

Figures 2, 3, and 4 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in ultra low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.



Board layout for Input Guarding with Guarded TO-99 Package.

FIGURE 1. Connection of Case Guard and Input Guard.

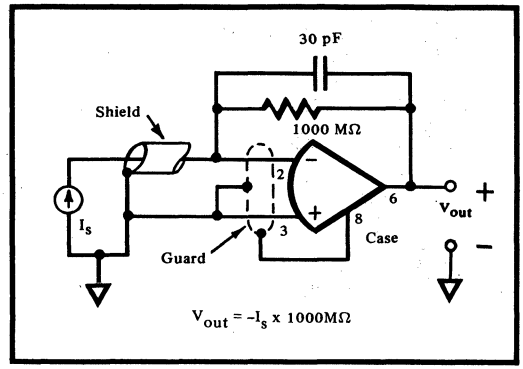


FIGURE 2. Ultra Low Current to Voltage Converter.

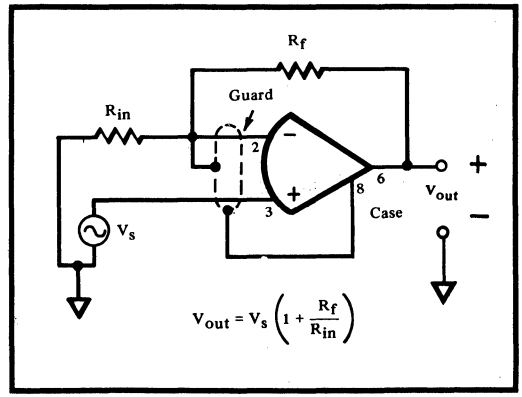


FIGURE 3. Ultra High Input Impedance Noninverting Circuit.

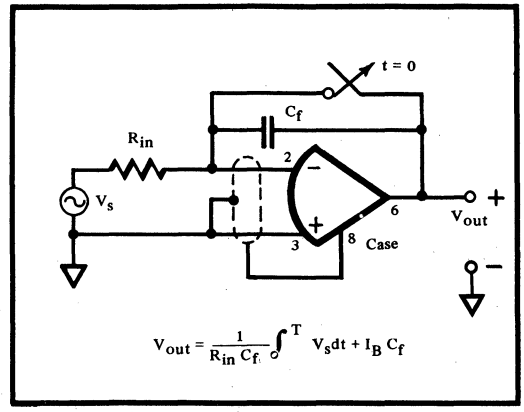
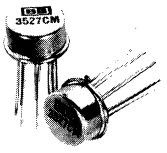


FIGURE 4. Ultra Low Drift Integrator.

BURR-BROWN®

3527



Low Drift - Low Bias Current FET Input OPERATIONAL AMPLIFIER

FEATURES

- LOWER PRICED
- ULTRA-LOW DRIFT, 2μV/°C, max
- LOW INITIAL OFFSET VOLTAGE, 250μV, max
- LOW BIAS CURRENT, 2pA, max
- LOW NOISE

DESCRIPTION

The Burr-Brown 3527 is a precision operational amplifier. It offers spectacular performance at moderate cost through the use of hybrid construction, monolithic ICs, matched FETs, thin-film resistors, and active laser trimming.

The 3527 low, initial offset voltage (250μV, max) allows higher design accuracy at lower installed cost. Costly pots and external nulling of the offset voltage is not required for most applications. Also, higher system reliability is achieved by using fewer parts.

The offset voltage temperature drift of the 3527 is exceptionally low (2μV/°C, max) and is compatible with the best bipolar amplifiers (BB3500E). It is achieved by laser-adjusting the offset during manufacture and means that high system accuracy is maintained over the temperature range.

The low bias current (guaranteed 2pA, max) allows the use of larger feedback resistor values, and smaller bias current errors are realizable.

Of course, all the other desirable features of high quality op amps are engineered into the 3527. It has low input noise, is free from latch-up, is short-circuit-protected for continuous output shorts to common, is internally compensated for unity-gain stability, and is pin-compatible with 741 amplifiers. Guarding is achieved by the pin 8 case connection.

For increased reliability screening, consult Burr-Brown.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-370

SPECIFICATIONS

ELECTRICAL

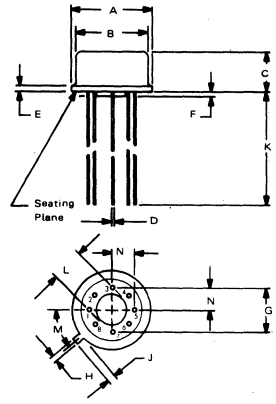
Specifications typical at T_A = 25°C and ±15VDC supplies, unless otherwise noted.

MODELS	3527AM			3527BM			3527CM			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN, DC					*			*		
No Load		112								dB
R_L = 2kΩ	100	108								dB
RATED OUTPUT					*			*		
Voltage	±10	±12								V
Current	±10	±20								mA
Output Impedance		600								Ω
Load Capacitance		1000								pF
FREQUENCY RESPONSE					*			*		
Unity Gain, Open Loop		1								MHz
Full Power Response	10	14								kHz
Slew Rate	0.6	0.9								V/μsec
Settling Time (0.01%)		45								μsec
INPUT OFFSET VOLTAGE										
Initial Offset, 25°C		±200	±500		±100	±250		±100	±250	μV
vs. Temp. (-25°C to +85°C		±5	±10		±2	±5		±1	±2	μV/°C
vs. Supply Voltage		±75			*			*		μV/V
vs. Time		±20			*			*		μV/mo
INPUT BIAS CURRENT										
Initial Bias, 25°C		-2	-5		-0.7	-2		-2	-5	pA
vs. Temp		**			**			**		
vs. Supply Voltage		±5			*			*		pA/V
INPUT DIFFERENCE CURRENT					*			*		
Initial Difference, 25°C		±0.3								pA
INPUT IMPEDANCE					*			*		
Differential		10^{12}								Ω
Common-mode		10^{15}								Ω
INPUT NOISE					*			*		
Voltage, f_o = 10Hz		75								nV/√Hz
f_o = 100Hz		35								nV/√Hz
f_o = 1kHz		30								nV/√Hz
f_o = 10kHz		25								nV/√Hz
0.3Hz to 10Hz, p-p		2.6								μV
10Hz to 10kHz, rms		3								μV
Current, 0.3Hz to 10Hz, p-p		15								fA
10Hz to 10kHz, rms		60								fA
INPUT VOLTAGE RANGE					*			*		
Common-mode Voltage Range		±(|Vs|-3								V
Common-mode Rejection at ±10V		76								dB
Max. Safe Input Voltage		±Vs								VDC
POWER SUPPLY					*		*	*		
Rated Voltage		±15								VDC
Voltage Range, derated performance	±5		±20							VDC
Current, quiescent		2.6	4							mA
TEMPERATURE RANGE (ambient)					*		*		*	
Specification	-25		+85							°C
Operating	-55		+125							°C
Storage	-65		+150							°C
θ junction-ambient		235								°C/W

*Specifications same as for 3527AM.
**Doubles every +10°C.

MECHANICAL TO-99 PACKAGE

Order Number: 3527AM, 3527BM, 3527CM Weight: 1 gram



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

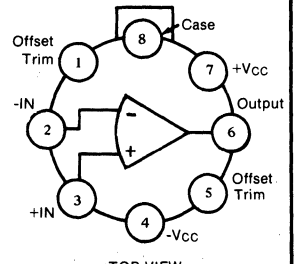
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

The TO-99 can and leads are bright acid tin plated.

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CONNECTION DIAGRAM

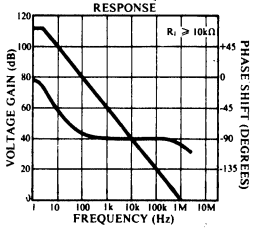


(TOP VIEW)

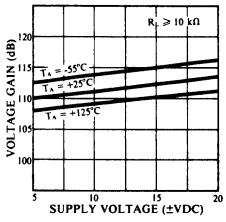
TYPICAL PERFORMANCE CURVES

at T_A = +25°C and ±15VDC unless otherwise noted.

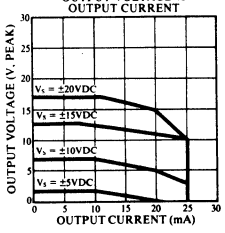
OPEN LOOP FREQUENCY RESPONSE



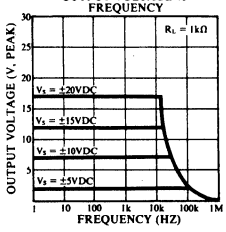
VOLTAGE GAIN



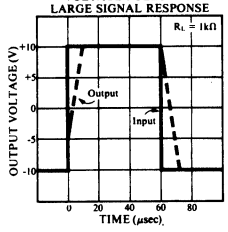
OUTPUT VOLTAGE vs OUTPUT CURRENT



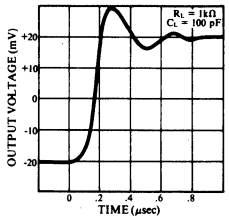
OUTPUT VOLTAGE vs FREQUENCY



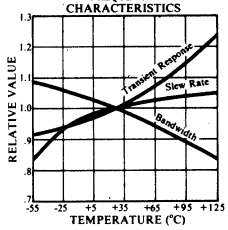
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



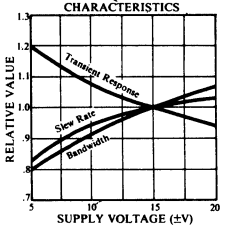
TRANSIENT RESPONSE



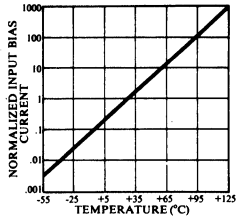
FREQUENCY CHARACTERISTICS



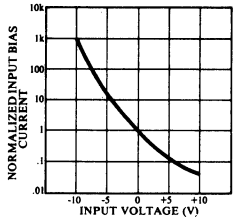
FREQUENCY CHARACTERISTICS



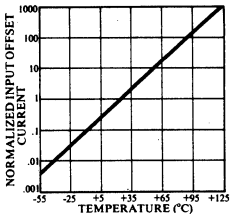
INPUT BIAS CURRENT



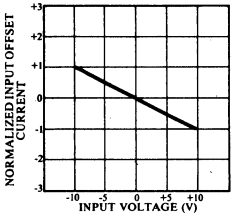
INPUT BIAS CURRENT



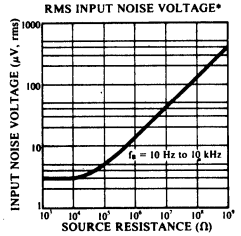
INPUT OFFSET CURRENT



INPUT OFFSET CURRENT

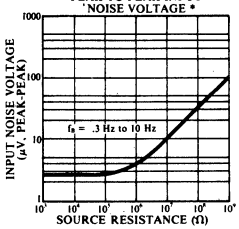


RMS INPUT NOISE VOLTAGE*

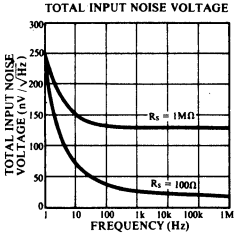


* Includes contribution from source resistance.

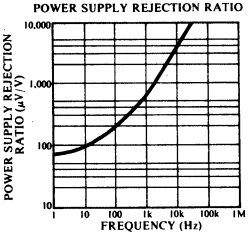
PEAK-TO-PEAK INPUT NOISE VOLTAGE *



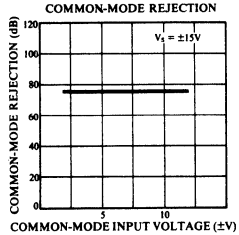
TOTAL INPUT NOISE VOLTAGE



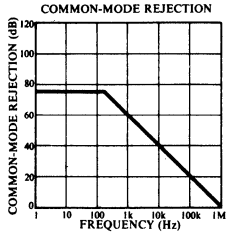
POWER SUPPLY REJECTION RATIO



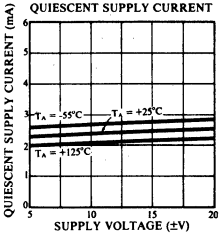
COMMON-MODE REJECTION



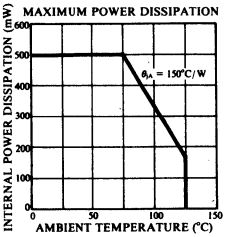
COMMON-MODE REJECTION



QUIESCENT SUPPLY CURRENT



MAXIMUM POWER DISSIPATION



APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the 3527. A low drift specification would be of little value if the amplifier took several hours to stabilize after turn-on or ambient temperature change. The TO-99 packaging is particularly well suited for devices requiring fast thermal response. Figure 1 shows the typical warm-up drift of the 3527. Note that the offset voltage has stabilized in less than 1 minute. Similar warm-up times for some low drift operational amplifiers range from 2 to 15 minutes.

Offset voltage response to thermal shock can provide some real surprises, particularly for amplifiers packaged in discrete modules. Again the 3527 TO-99 package proves superior. Figure 2 shows that the response to thermal shock settles very quickly. The 3527 quickly and smoothly assumes a new value of offset voltage as dictated by the drift specification.

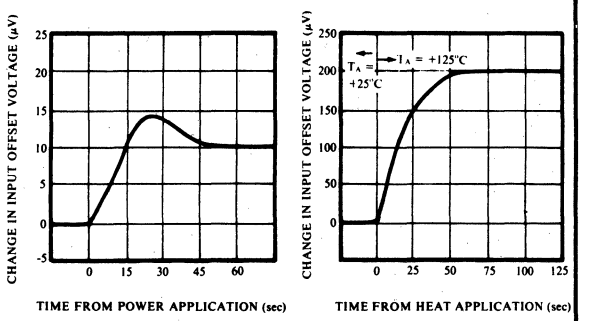


FIGURE 1. Typical Warmup Drift.

FIGURE 2. Effect of Thermal Shock on Offset Voltage.

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the 3527 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the 3527.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3527. To avoid leakage problems, it is recommended that the signal input lead of the 3527 be wired to a Teflon standoff. If the 3527 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 3 illustrates the use of the guard.

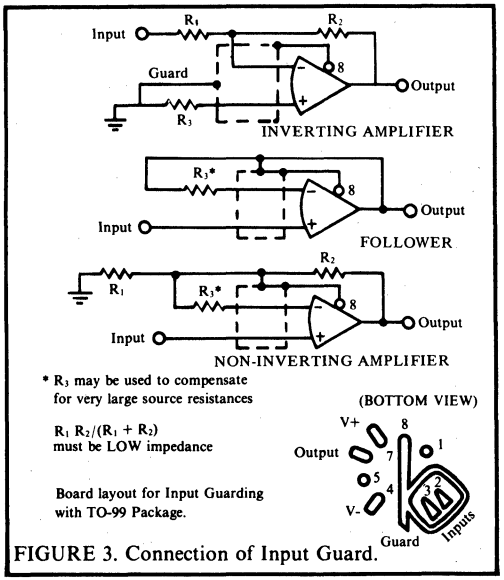


FIGURE 3. Connection of Input Guard.

OFFSET VOLTAGE ADJUSTMENT

Although the 3527 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. For each microvolt of offset adjusted, an additional drift of ±0.002 μV/°C is induced.

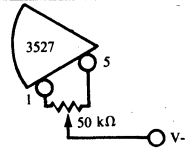


FIGURE 4. External Nulling of Offset Voltage.

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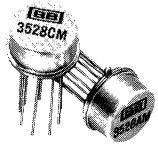
3528



Ultra Low Bias Current FET OPERATIONAL AMPLIFIER

FEATURES

- 75fA MAX INPUT BIAS CURRENT
- 250μV MAX OFFSET VOLTAGE
- 5μV/°C MAX OFFSET VOLTAGE DRIFT

APPLICATIONS

- PHOTODIODE AMPLIFIER
- PHOTOMULTIPLIER TUBE AMPLIFIER
- LOW DRIFT INTEGRATOR
- CURRENT-TO-VOLTAGE CONVERTER

DESCRIPTION

An excellent combination of specifications for applications requiring ultra low input bias currents are provided by the 3528 amplifier family. These applications include photometers, selective ion detectors, long term integrators and low-droop sample hold circuits.

The 3528 is unique in that in addition to providing bias currents as low as 75fA (3528CM) it also provides very low offset voltage drift (5μV/°C max, 3528BM) and offset voltage (250μV, 3528BM). Thus, user trimming offset voltage with an external potentiometer is usually avoided.

The output is protected from damage due to short circuits to ground or either supply and the unit is specified over the full -25°C to +85°C temperature range rather than the more limited 0°C to 70°C range.

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PDS-389

ELECTRICAL SPECIFICATIONS

At T_A = 25°C and $\pm V_{cc}$ = ±15VDC unless otherwise noted.

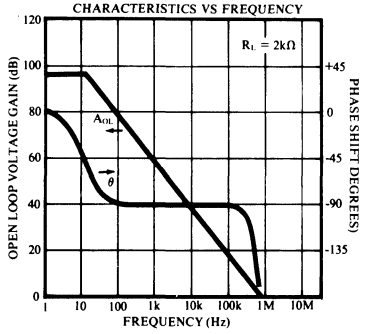
PARAMETER	CONDITIONS	3528AM MIN	3528AM TYP	3528AM MAX	3528BM MIN	3528BM TYP	3528BM MAX	3528CM MIN	3528CM TYP	3528CM MAX	UNITS
OPEN LOOP GAIN, DC											
$R_L \geq 2k$	V_o = 20V p-p	88	93		92	95		90	93		dB
$R_L \geq 10k$	V_o = 20V p-p	94	114		100	*		98	*		
RATED OUTPUT											
Voltage	$R_L = 2k\Omega$	±10	±12		*	*		*	*		V
	R_L = 10k	±12	±13		*	*		*	*		V
Current	V_o = ±10V	±5	±10		*	*		*	*		mA
Output Resistance Open Loop	f = DC		1.5	3		*	*		*	*	kΩ
Short Circuit Current	$R_L = 0\Omega$		19			*			*		mA
DYNAMIC RESPONSE											
Bandwidth, Unity Gain	Small Signal		0.7			*			*		MHz
Full Power Bandwidth	$R_L = 2k\Omega$	5	11		*	*		*	*		kHz
Slew Rate	$R_L = 2k\Omega$	0.3	0.7		*	*		*	*		V/μsec
Settling time	to 1%		30			*			*		μs
	to 0.1%		150			*			*		μs
	to 0.01%		1			*			*		ms
INPUT OFFSET VOLTAGE											
Initial Offset	T_A = 25°C		±200	±500		±100	±250		±200	±500	μV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±5	±15		±2	±5		±5	±10	μV/°C
vs Supply Voltage	$\pm V_{CC}$ = 15V to 20V, to 5V		±25	±100		*	*		*	*	μV/V
vs Time			20			*			*		μV/mo
INPUT BIAS CURRENT											
Initial	T_A = 25°C			-300			-150			±75	fA
at Temperature	at T_A = 85°C		-40	-60		-20	-30		-10	-15	pA
vs Supply Voltage			1			*			*		fA/V
INPUT DIFFERENCE CURRENT											
Initial	T_A = 25°C		±80			±40			±20		fA
at Temperature	at T_A = 85°C		±8			±4			±2		pA
INPUT IMPEDANCE											
Differential			$10^{13} \parallel 0.8$			*			*		Ω ‖ pF
Common-mode			$10^{15} \parallel 1$			*			*		Ω ‖ pF
INPUT NOISE											
Voltage Noise Density	f_o = 1Hz		475			*			*		nV/√Hz
	f_o = 10Hz		120			*			*		nV/√Hz
	f_o = 100Hz		55			*			*		nV/√Hz
	f_o = 1kHz		40			*			*		nV/√Hz
	f_o = 10kHz		40			*			*		nV/√Hz
Voltage Noise	f_B = 0.3Hz to 10Hz		6			*			*		μV, p-p
	f_B = 10Hz to 10kHz		4			*			*		μV, rms
Current Noise Density	f_o = 1Hz		0.25			0.2			0.15		fA/√Hz
	f_o = 10Hz		0.25			0.2			0.15		fA/√Hz
	f_o = 100Hz		0.25			0.2			0.15		fA/√Hz
	f_o = 1kHz		0.25			0.2			0.15		fA/√Hz
Current Noise	f_B = 0.3Hz to 10Hz		7			5			4		fA, p-p
	f_B = 10Hz to 10kHz		26			20			15		fA, rms
INPUT VOLTAGE RANGE											
Common-mode Voltage Range	Linear Operation		$\pm(\lvert V_{cc}\rvert - 3)$			*			*		V
Common-mode Rejection	f = DC, V_{CM} = ±10V	66	74		80	86		70	86		dB
Max. Safe Input Voltage			$\pm V_{cc}$			*			*		V
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range, derated performance		±5		±20	*		*	*		*	V
Current, quiescent			1	1.5		*	*		*	*	mA
TEMPERATURE RANGE (ambient)											
Specification		-25		+85	*		*	*		*	°C
Operating, derated performance		-55		+125	*		*	*		*	°C
Storage		-65		+150	*		*	*		*	°C

TABLE I. Electrical Specifications

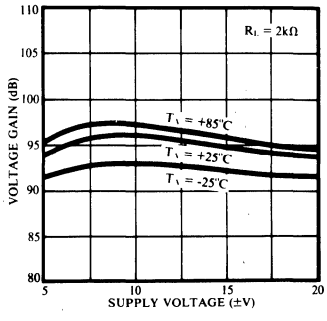
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted)

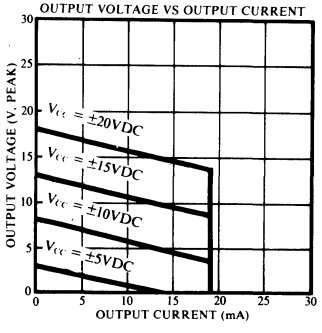
OPEN LOOP TRANSFER CHARACTERISTICS VS FREQUENCY



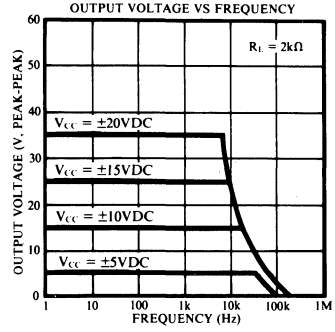
VOLTAGE GAIN VS SUPPLY VOLTAGE



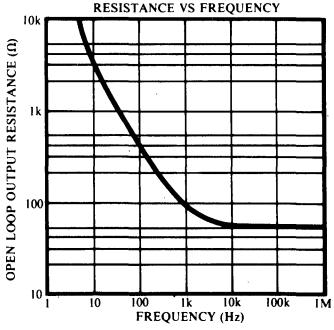
OUTPUT VOLTAGE VS OUTPUT CURRENT



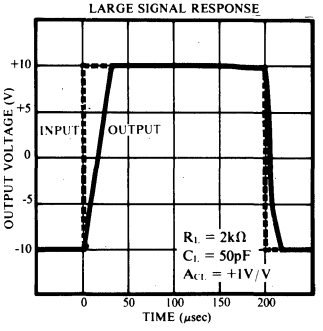
OUTPUT VOLTAGE VS FREQUENCY



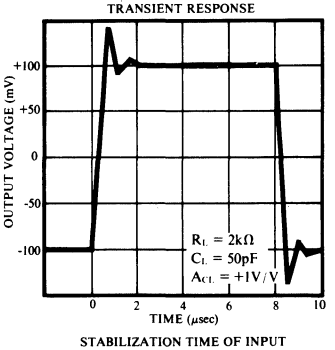
OPEN LOOP OUTPUT RESISTANCE VS FREQUENCY



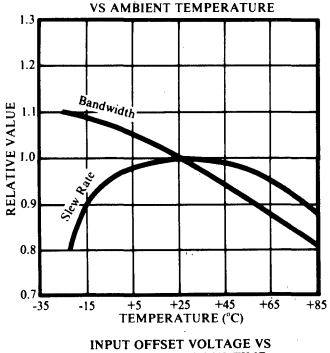
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



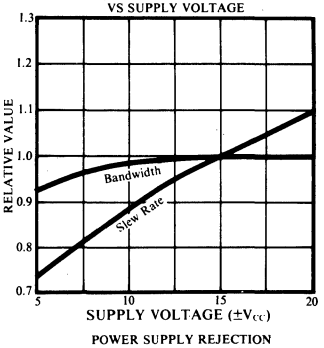
TRANSIENT RESPONSE



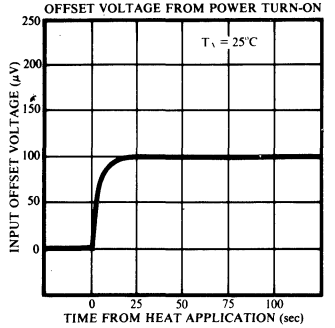
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



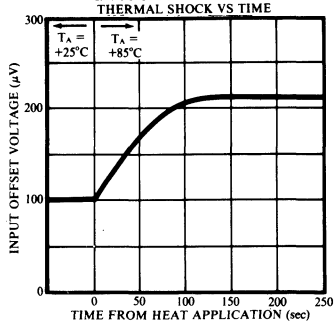
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



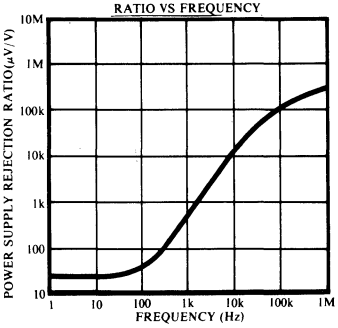
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



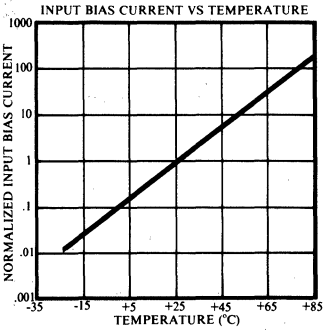
INPUT OFFSET VOLTAGE VS THERMAL SHOCK VS TIME



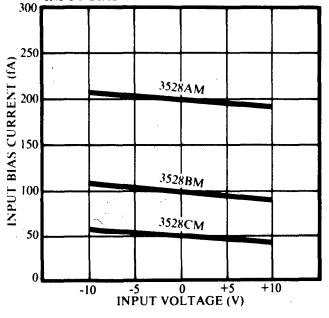
POWER SUPPLY REJECTION RATIO VS FREQUENCY



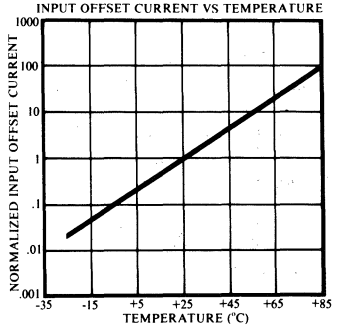
INPUT BIAS CURRENT VS TEMPERATURE



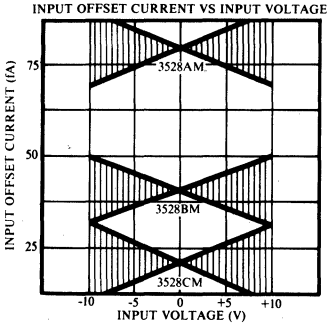
INPUT BIAS CURRENT VS INPUT VOLTAGE



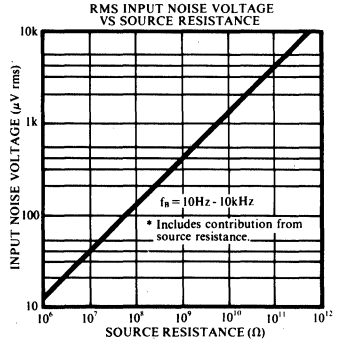
INPUT OFFSET CURRENT VS TEMPERATURE



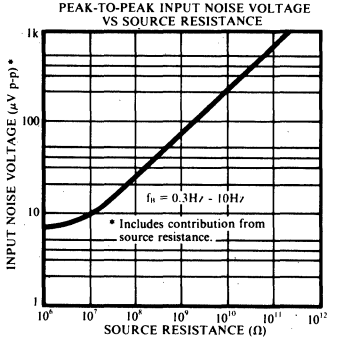
INPUT OFFSET CURRENT VS INPUT VOLTAGE



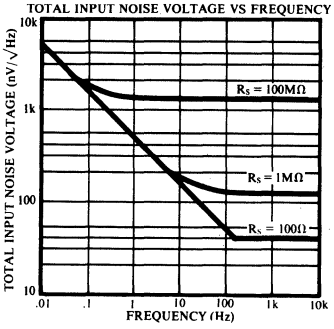
RMS INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



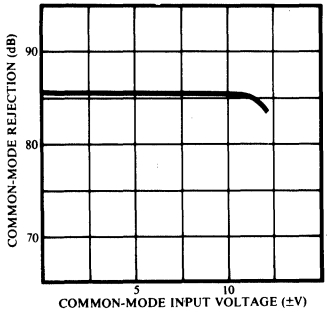
PEAK-TO-PEAK INPUT NOISE VOLTAGE VS SOURCE RESISTANCE



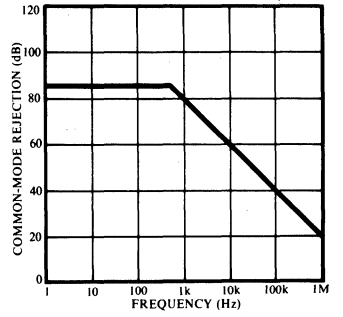
TOTAL INPUT NOISE VOLTAGE VS FREQUENCY



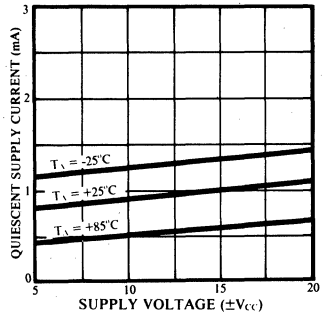
COMMON-MODE REJECTION VS COMMON MODE INPUT VOLTAGE



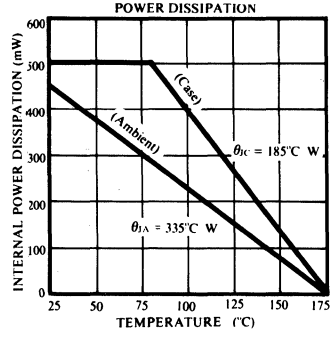
COMMON-MODE REJECTION VS FREQUENCY



QUIESCENT SUPPLY CURRENT VS SUPPLY VOLTAGE



POWER DISSIPATION



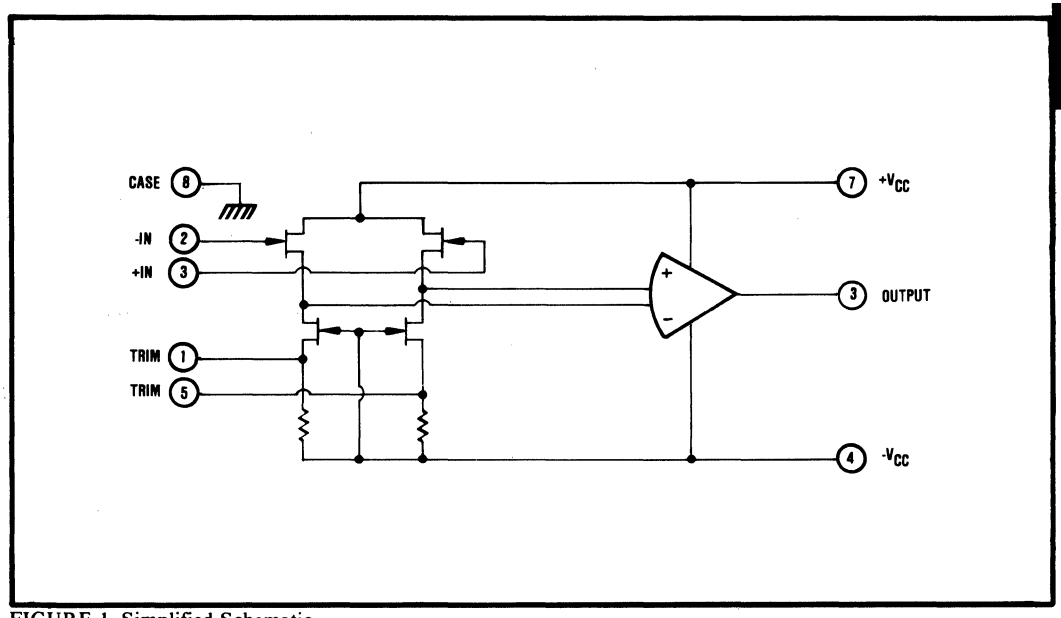


FIGURE 1. Simplified Schematic

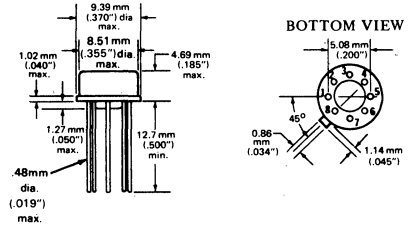
ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation (note 1)	500mW
Differential Input Voltage (note 2)	±40VDC
Input Voltage Range (note 2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	300°C
Output Short - Circuit Duration (note 3)	Continuous
Junction Temperature	T_j = +175°C

NOTES:

1. Package must be derated based on a junction to ambient thermal resistance of 335°C/W.
2. For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +115°C case temperature or +75°C. ambient temperature.

TO-99 PACKAGE



Dimensions in inches are in parentheses. Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883

FIGURE 2. Mechanical Specifications

CONNECTION DIAGRAM

TOP VIEW

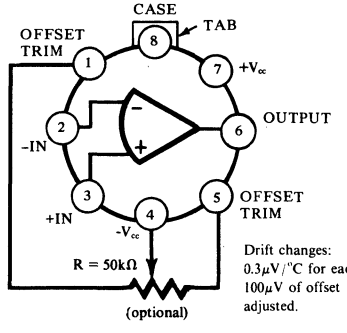


FIGURE 3. Pin Connections

APPLICATION CONSIDERATIONS

The ultra-low bias current and high input impedance of the 3528 are well suited to a number of challenging applications. In order to fully benefit from the outstanding specifications of this unit careful layout, shielding and guarding is required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the 3528.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the 3528 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pick-up.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3528. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the 3528 be wired to a Teflon standoff. If this is not done and instead the 3528 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 4). The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents.

Figures 5, 6, and 7 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in ultra-low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.

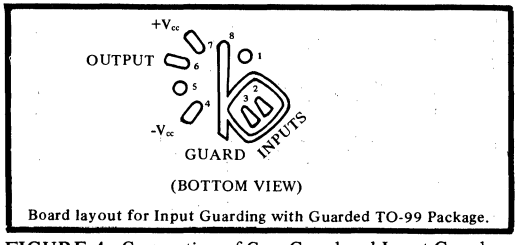


FIGURE 4. Connection of Case Guard and Input Guard.

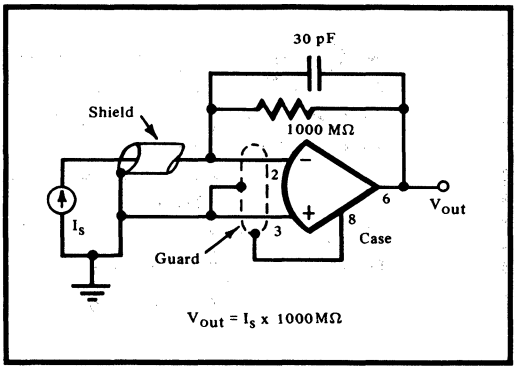


FIGURE 5.Ultra Low Current to Voltage Converter.

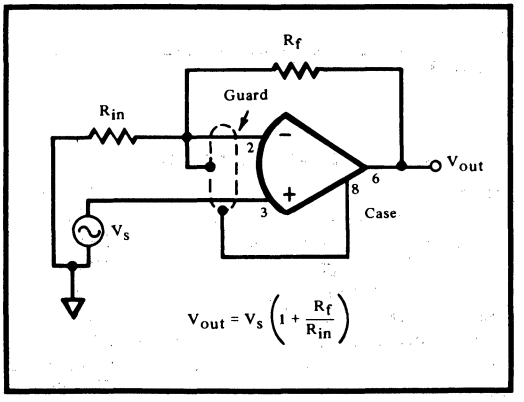


FIGURE 6. Ultra High Input Impedance Noninverting Circuit.

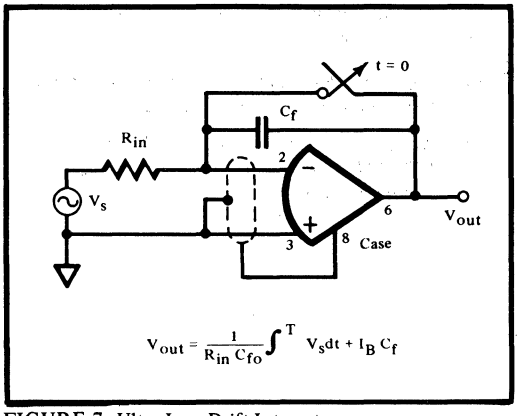


FIGURE 7. Ultra Low Drift Integrator.

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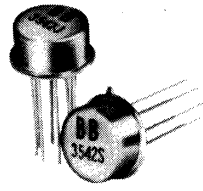

3542 SERIES

FET Input OPERATIONAL AMPLIFIERS

FEATURES

- HIGH INPUT IMPEDANCE, $10^{11}\ \Omega$
- LOW NOISE, 2μV, p-p
- HIGH CMR, 80dB
- WIDE SUPPLY RANGE, ±5VDC to ±20VDC
- INTERNAL FREQUENCY COMPENSATION
- INDUSTRIAL AND MILITARY VERSIONS

DESCRIPTION

These FET amplifiers offer excellent input characteristics at low cost through the use of monolithic chips and thin film hybrid technology. Unlike other FET op amps of comparable cost, they have low input noise and moderate voltage drift. Thus they are suitable for a number of applications where previous hybrid or monolithic FET op amps were, at best marginal.

In addition, the 3542 series are extremely stable amplifiers having internal frequency compensation. Other built-in features are output short-circuit protection, input protection to supply voltage, and operation over a wide range of supply voltages.

The pin configuration of the 3542 is conventional (same as 741 type amplifiers) except for pin 8, which is connected to the case. In the usual IC operational amplifier, the case is connected to the negative supply voltage. However, in FET amplifiers it is often desirable to connect the case to a low impedance "guard" potential. This aids in eliminating noise "pickup" in high impedance circuits and preserves the low input currents of the amplifier.

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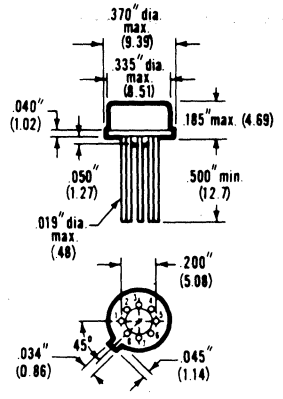
PDS-293D

SPECIFICATIONS

Specifications typical at 25°C and ±15 Vdc Power Supply unless otherwise noted.

MODEL	3542J	3542S
OPEN LOOP GAIN, dc rated load, min.	88 dB	
RATED OUTPUT Voltage, min. Current, min. Output Impedance	±10V ±10 mA 75 Ω	
FREQUENCY RESPONSE Unity Gain, Open Loop Full Power Response Slew Rate	1 MHz 8 kHz 0.5 V/μsec	
INPUT OFFSET VOLTAGE Initial Offset, 25°C, max. vs. Temp (0° to 70°C) vs. Supply Voltage vs. Time	±20 mV ±10μV/°C, typ; ±50μV/°C, max ±50μV/V typ ±100 μV/mo	
INPUT BIAS CURRENT Initial bias, 25°C (doubles every +10°C) vs. Supply Voltage	-10 typ, -25 max. pA 1 pA/V	
INPUT DIFFERENCE CURRENT Initial difference, 25°C	±2 pA	
INPUT IMPEDANCE Differential Common Mode	10^{11} Ω 10^{11} Ω	
INPUT NOISE Voltage, .01 Hz - 10 Hz, p-p 10 Hz - 1 kHz, rms Current, .01 Hz - 10 Hz, p-p 10 Hz - 1 kHz, rms	2 μV 3 μV 0.3 pA 0.6 pA	
INPUT VOLTAGE RANGE Common Mode Voltage Common Mode Rejection Max. Safe Input Voltage	±($\|V_S\|$ -5 V) 80dB typ $\pm V_S$	
POWER SUPPLY Rated Voltage Voltage Range, derated Current, quiescent	±15 VDC ±5 to ±20 VDC ±4 mA	
TEMPERATURE RANGE Specification Operating Storage	0° to +70°C -25° to +85°C -65° to +150°C	-55° to +125°C -55° to +125°C

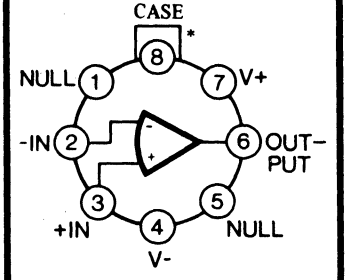
TO-99 PACKAGE



(BOTTOM VIEW)

CONNECTION DIAGRAM

(TOP VIEW)

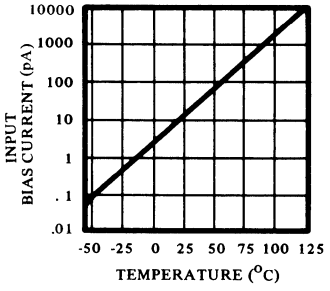


*Pin 8 is connected to case

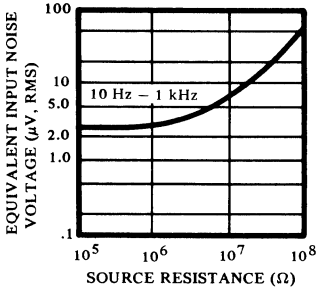
TYPICAL PERFORMANCE CURVES

(@ +25°C and ±15 Vdc unless otherwise specified)

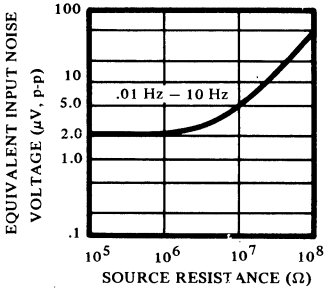
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



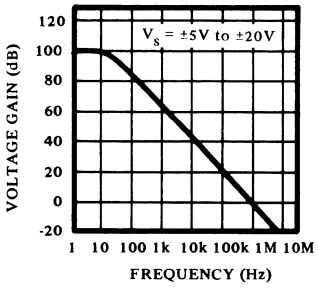
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



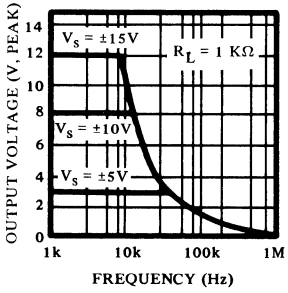
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



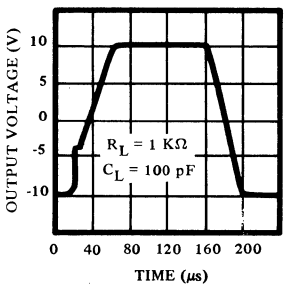
OPEN LOOP FREQUENCY RESPONSE



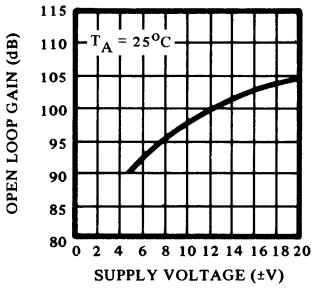
OUTPUT VOLTAGE vs. FREQUENCY



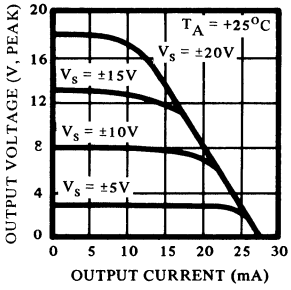
VOLTAGE FOLLOWER STEP RESPONSE



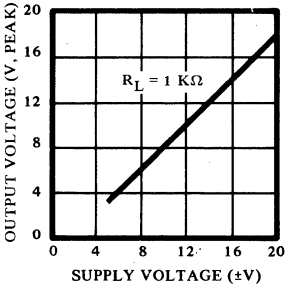
VOLTAGE GAIN vs. SUPPLY VOLTAGE



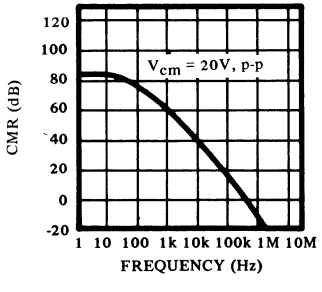
OUTPUT VOLTAGE vs. OUTPUT CURRENT



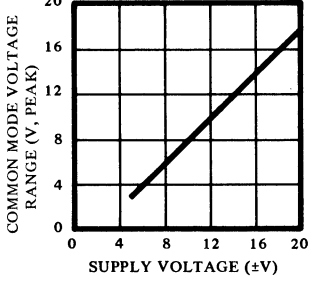
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



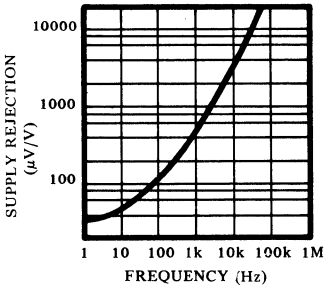
COMMON MODE REJECTION vs. FREQUENCY



COMMON MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



WIRING CONSIDERATIONS

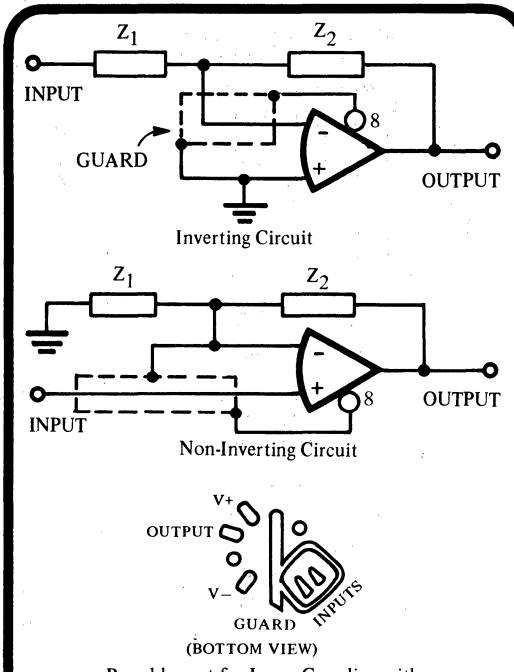
SHIELDING AND GUARDING

The low bias current and high input impedance of the 3542 are well-suited to a number of stringent applications. However, careless signal wiring or printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the 3542.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the 3542. To avoid leakage problems, it is recommended that the signal input lead of the 3542 be wired to a Teflon standoff. If the 3542 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard for both inverting and non-inverting circuits.



Board layout for In Guarding with Guarded TO-99 Package.

FIGURE 1. Connection of Case Guard and Input Guard.

OFFSET VOLTAGE ADJUSTMENT

Although the 3542 has a moderately low initial offset voltage (5 mV, typ) compatible with it's moderate voltage drift, some applications may require external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage.

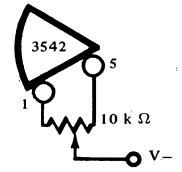


FIGURE 2. External Nulling of Offset Voltage.

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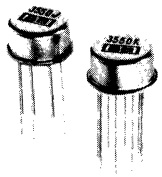

3550 SERIES

Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- SETTLING TIME (0.01%), 600ns, max
- TRUE DIFFERENTIAL INPUT
- SLEW RATE, 100V/μs, min
- FULL POWER, 1.5MHz, min
- INPUT IMPEDANCE, $10^{11}\Omega$
- INTERNALLY COMPENSATED
- STABLE OPERATION, 1000pF, typ

DESCRIPTION

The 3550 is specifically designed for fast transient applications such as D/A and A/D conversion, sample/hold, multiplexer buffering and pulse amplification where the primary amplifier requirements are fast settling, good accuracy, and high input impedance.

Because the 3550 is internally compensated, elaborate compensation schemes requiring external components are not necessary. The smooth 6dB/octave rolloff of open-loop gain and the low output impedance provides the excellent step response and smooth settling without sacrificing frequency stability (no oscillations even with 1000pF of capacitive load)! A 10 to 1 improvement in settling time with large capacitive loads can be obtained with the addition of a single capacitor.

Unlike many wideband and fast settling amplifiers the 3550 has a true differential input. This means it can provide its excellent transient performance in the inverting, non-inverting, current to voltage, and difference configurations.

The 3550J and S have identical specifications except for temperature range: The 3550J is specified for 0°C to +70°C and the 3550S is specified for -55°C to +125°C. The 3550K has improved dynamic specifications and is specified over the 0°C to +70°C temperature range.

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PDS-302

SPECIFICATIONS

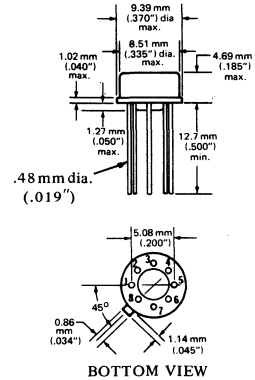
ELECTRICAL

Specifications typical at 25°C and ±15 Vdc Power Supply unless otherwise noted.

MODELS	3550J	3550K	3550S
OPEN LOOP GAIN, dc			
no load		100 dB	
1 kΩ, load min		88 dB	
RATED OUTPUT			
Voltage, min		±10 V	
Current, min		±10 mA	
Open loop Output Resistance		100 Ω @ 1 MHz	
DYNAMIC RESPONSE			
Bandwidth (0 dB, small signal)	10 MHz	20 MHz	10 MHz
Full Power Response, min	1.0 MHz	1.5 MHz	1.0 MHz
Slew Rate, min	65 V/μs	100 V/μsec	65 V/μs
Settling Time (0.01%), max	1 μs	0.6 μs	1 μs
INPUT OFFSET VOLTAGE			
Initial Offset, 25°C, max		±1 mV	
vs. Temp		±50 μV/°C	
vs. Supply Voltage		±500 μV/V	
vs. Time		±100 μV/mo	
INPUT BIAS CURRENT			
Initial Bias, 25°C, max		-400pA (after full warm-up)	
vs. Temperature		doubles every 10°C	
vs. Supply Voltage		±1 pA/V	
INPUT DIFFERENCE CURRENT			
Initial Difference, 25°C		±10 pA	
INPUT IMPEDANCE			
Differential		10^{11} Ω ‖ 3 pF	
Common Mode		10^{11} Ω ‖ 3 pF	
INPUT NOISE			
Voltage, .01 Hz - 10 Hz, p-p		20 μV	
10 Hz - 10 kHz, rms		4 μV	
Current, .01 Hz - 10 Hz, p-p		0.2 pA	
10 Hz - 10 kHz, rms		1.5 pA	
INPUT VOLTAGE RANGE			
Common Mode Voltage		±(|V_S| -5) V	
Common Mode Rejection		70 dB @ +5 V, -10V	
Max. Safe Input Voltage		±Supply	
POWER SUPPLY			
Rated Voltage		±15 Vdc	
Voltage Range, derated		±5 to ±20 Vdc	
Current, quiescent	(1)	11 mA	
TEMPERATURE RANGE			
Specification		0° to +70°C	-55° to +125°C
Operating		-55°C to +125°C	-55° to +125°C
Storage		-65° to +150°C	

(1) The use of a finned heatsink is recommended.

MECHANICAL TO-99

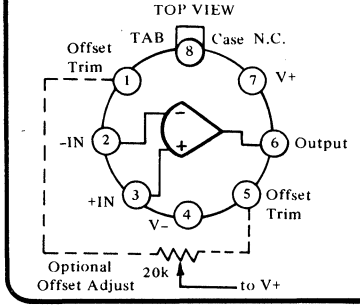


BOTTOM VIEW

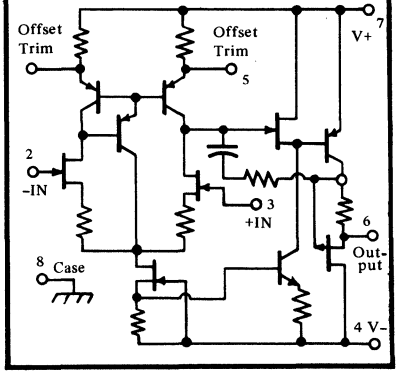
Dimensions in inches are in parentheses.

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM



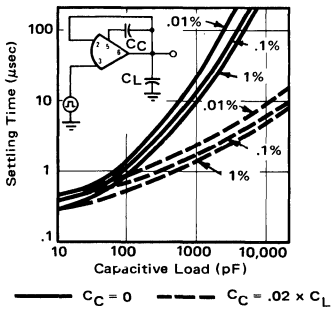
Simplified Schematic



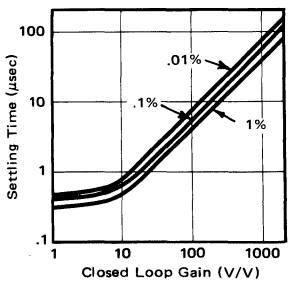
TYPICAL PERFORMANCE CURVES

$T_A = 25^oC$ $V_S = \pm 15$ Vdc unless otherwise indicated.

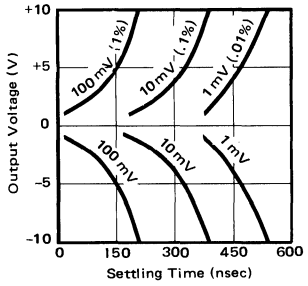
SETTLING TIME vs. CAPACITIVE LOAD



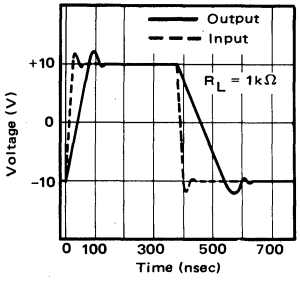
SETTLING TIME vs. CLOSED LOOP GAIN



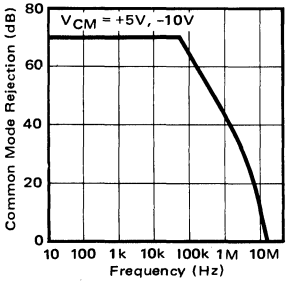
SETTLING TIME vs. OUTPUT VOLTAGE CHANGE



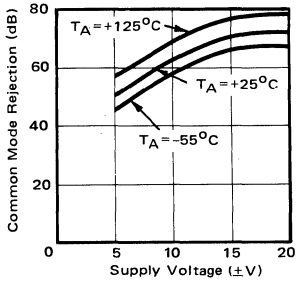
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



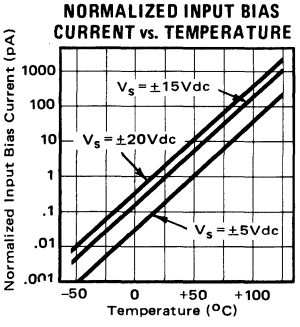
COMMON MODE REJECTION vs. FREQUENCY



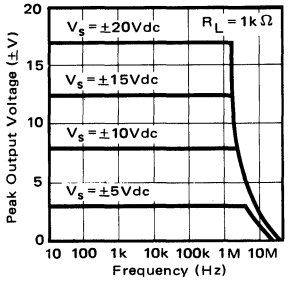
COMMON MODE REJECTION vs. SUPPLY VOLTAGE



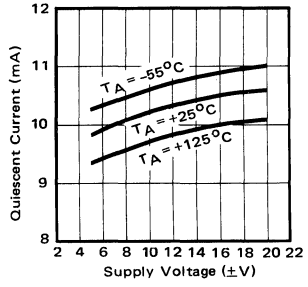
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



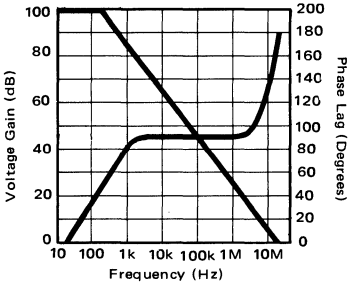
OUTPUT VOLTAGE vs. FREQUENCY



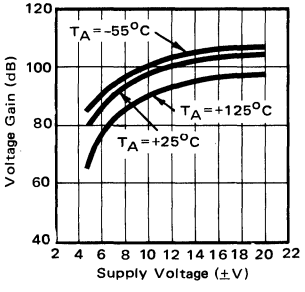
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



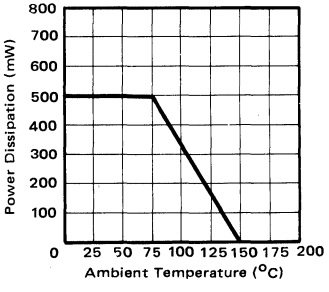
OPEN LOOP RESPONSE



OPEN LOOP GAIN vs. SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

SETTLING TIME

Settling time of an amplifier is defined (see Figure 1) as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition. A recommended test circuit for settling time is shown in Figure 2. The output error signal appears, attenuated by a factor of two, at point A and may be observed at this point with the aid of an oscilloscope. The diodes act as limiters to prevent overloading the oscilloscope during the fast leading edge of the input signal. All resistors should be 2 kΩ or less to eliminate degradation of performance due to stray capacitance. A typical measurement desired is the settling time to .01% for a 10 volt step input. This is the time required for the signal at point A to decrease to 0.5 mV or less and remain below this level.

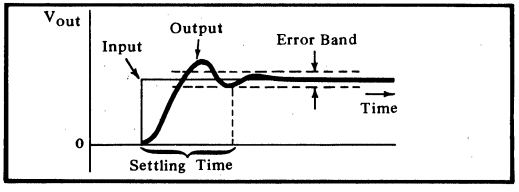


FIGURE 1. Concept of Settling Time.

Settling time for noninverting circuits can also be measured but requires the use of ultra-fast differential amplifier test fixtures. For the 3550 settling time is equal for inverting or noninverting circuits of equal gain.

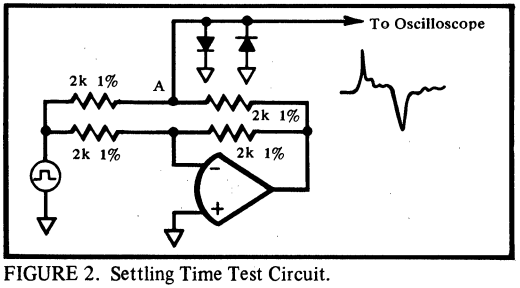


FIGURE 2. Settling Time Test Circuit.

Because settling time is affected by bandwidth which in turn is dependent upon closed-loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling time vs. gain curves on page 1-115 illustrate this effect for the 3550 at several levels of settling accuracy.

The 3550 is remarkably tolerant of load capacitance because of its stable, 6 dB/octave gain rolloff and low output impedance. Settling time vs. load capacitance curves show this characteristic for the unity-gain configuration. For larger values of load capacitance the compensation technique of Figure 3 may be used to optimize the response. The slight negative feedback provided by C_C tends to reduce any ringing at the top of the output voltage waveform without significantly affecting the slew rate. See the settling time vs. load capacitance curves for typical improvements in settling time.

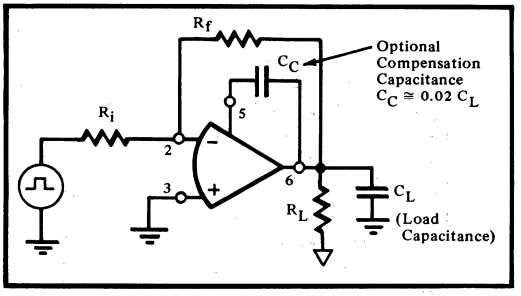


FIGURE 3. Compensation for Load Capacitance.

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3550, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the output to noninverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedances. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

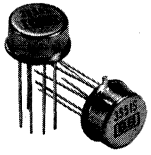
In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10 μf tantalum capacitor in parallel with a 0.001 μf ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3550 is specified for best operation on power supply voltage of ±15 Vdc, it will operate with minor performance changes over a power supply voltage range of ±5VDC to ±20VDC. Many of the curves on page 1-115 show performance of the 3550 when operated from supplies other than ±15 Vdc.

BURR-BROWN®

3551 SERIES



Wideband and Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- **REDUCES WIDEBAND ERRORS**
  - **50MHz Gain-bandwidth product (ACL ≥10)**
  - **250V/μs slew rate (Cf = 0)**
- **VERSATILE**
  - **Single compensation capacitor allows optimum response**
  - **True differential input**
- **PRESERVES DC ACCURACY**
  - **Bias current, 100pA, max**
  - **Laser-trimmed offset voltage**

DESCRIPTION

The 3551 is designed to offer the user versatility in wideband steady state and fast transient applications. The use of a single external compensation capacitor allows the user to optimize frequency response for maximum bandwidth for a variety of closed loop-gains and capacitive loads. The amplifier is stable at closed-loop gains of greater than 20V/V, with no external compensation and may be stablized at all gains with the single 10pF compensation capacitor.

In addition to the excellent dynamic response characteristics, the 3551 also has good DC properties. The use of a monolithic FET input stage gives the 3551 very low input bias and offset currents. This is in contrast to the high input currents usually associated with fast amplifiers having bipolar input stages. Also, the input offset voltage and offset voltage drift are low as a result of Burr-Brown's laser-trimming techniques.

Unlike many wideband and fast settling amplifiers, the 3551 has a true differential input. This means it can provide its excellent wideband response in the inverting, noninverting, current-to-voltage and difference configurations.

The 3551 is an excellent choice for applications such as fast D/A and A/D converters, high speed comparators and fast sampling circuits, to name just a few.

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PDS-301A

SPECIFICATIONS

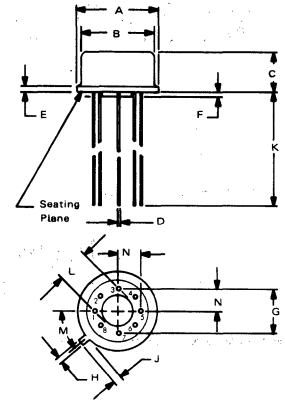
ELECTRICAL

Specifications typical at 25°C and ±15VDC Power Supply unless otherwise noted.

MODELS	3551J	3551S
OPEN LOOP GAIN, DC		
No Load	100dB	
1kΩ, Load min	88dB	
RATED OUTPUT		
Voltage, min	±10V	
Current, min	±10mA	
Open Loop Output Resistance	100Ω at 1MHz	
DYNAMIC RESPONSE		
Gain-Bandwidth Product		
Gain = 1000	50MHz	
Gain = 10	50MHz	
Slew Rate (C_f = 0)	250V/μsec	
INPUT OFFSET VOLTAGE		
Initial Offset, 25°C, max	±1mV	
vs. Temp(1)	±50μV/°C	
vs. Supply Voltage	±500μV/V	
vs. Time	±100μV/mo	
INPUT BIAS CURRENT		
Initial Bias, 25°C, max	-400pA (after full warm-up)	
vs. Temperature	doubles every 10°C	
vs. Supply Voltage	±1pA/V	
INPUT DIFFERENCE CURRENT		
Initial Difference, 25°C	±10pA	
INPUT IMPEDANCE		
Differential	$10^{11}\Omega$ || 3pF	
Common-mode	$10^{11}\Omega$ || 3pF	
INPUT NOISE		
Voltage, 0.01Hz to 10Hz, p-p	20μV	
Voltage, 10Hz to 10kHz, rms	4μV	
Current, 0.01Hz to 10Hz, p-p	0.2pA	
Current, 10Hz to 10kHz, rms	1.5pA	
INPUT VOLTAGE RANGE		
Common-mode Voltage	±(|V_{CC}|-5)V	
Common-mode Rejection	70dB at +5V, -10V	
Max. Safe Input Voltage	±Supply	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range, derated	±5VDC to ±20VDC	
Current, quiescent(1)	11mA	
TEMPERATURE RANGE		
Specification	0°C to +70°C	-55°C to +125°C
Operating	-55°C to +125°C	-55°C to +125°C
Storage	-65°C to +150°C	

NOTE:
1. The use of a finned heat sink is recommended.

MECHANICAL TO-99



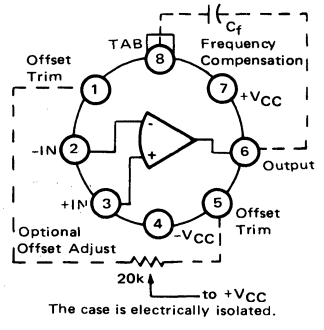
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	---	12.7	---
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

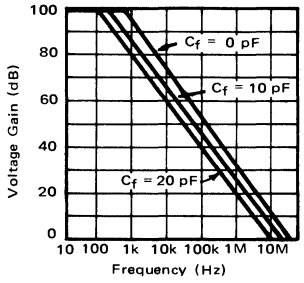


The case is electrically isolated.

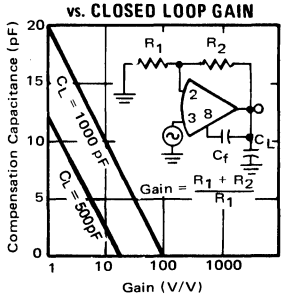
TYPICAL PERFORMANCE CURVES

T_A = 25°C, V_S = ±15VDC unless otherwise indicated.

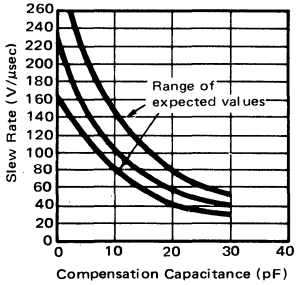
OPEN LOOP RESPONSE



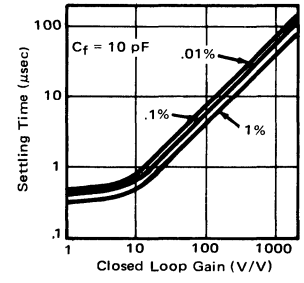
RECOMMENDED VALUES OF FREQUENCY COMPENSATION CAPACITANCE vs. CLOSED LOOP GAIN



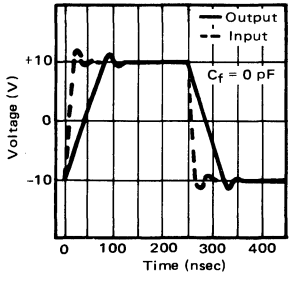
SLEW RATE vs. COMPENSATION CAPACITANCE



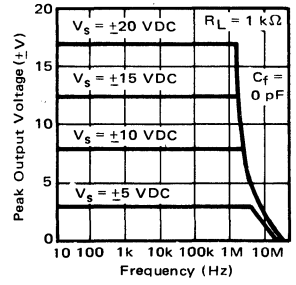
SETTLING TIME vs. CLOSED LOOP GAIN



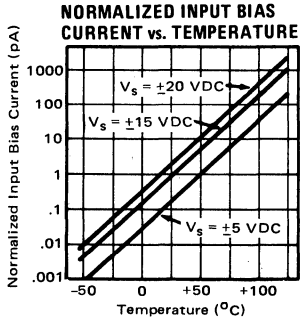
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



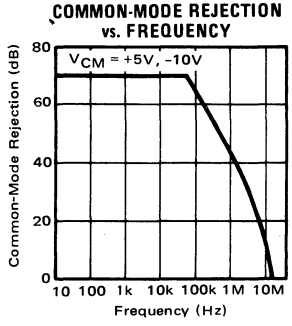
OUTPUT VOLTAGE vs. FREQUENCY



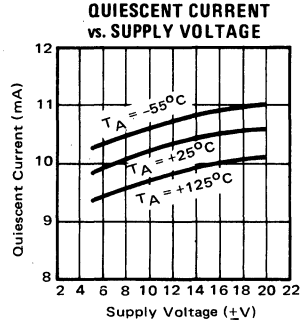
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



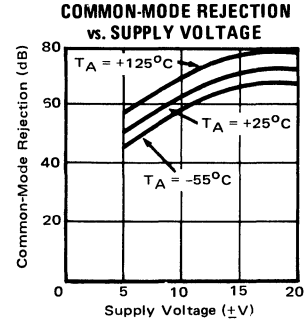
COMMON-MODE REJECTION vs. FREQUENCY



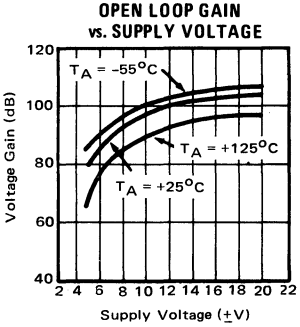
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



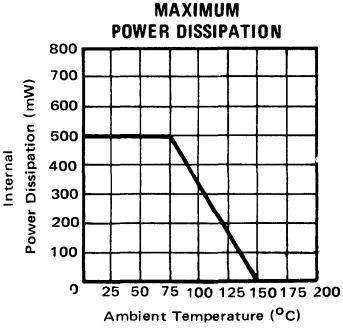
COMMON-MODE REJECTION vs. SUPPLY VOLTAGE



OPEN LOOP GAIN vs. SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3551, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the output to noninverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedances. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

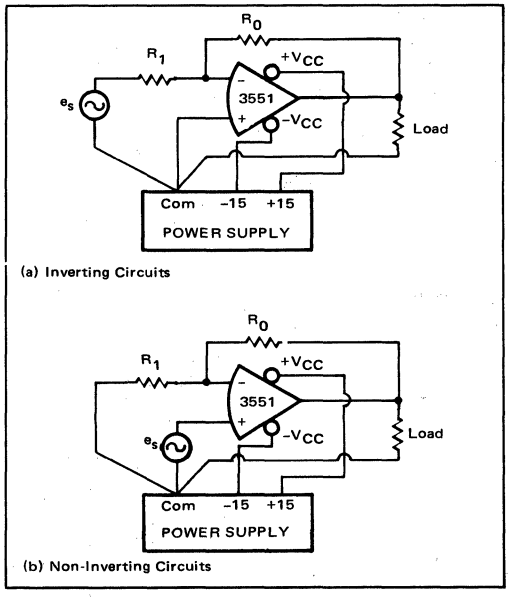


FIGURE 1. Proper Grounding Methods

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10 μf tantalum capacitor in parallel with a 0.001 μf ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3551 is specified for best operation on power supply voltage of ±15 VDC, it will operate with minor performance changes over a power supply voltage range of ±5 VDC to ±20 VDC. Many of the performance curves show performance of the 3551 when operated from supplies other than ±15 VDC.

INPUT/OUTPUT PROTECTION

All of the amplifiers listed in the specification table are designed to withstand input voltages as high as the supply voltage, without damage to the amplifier. Thus, inputs may be subjected to either supply voltage, in any combination, without damage.

Output stages are internally current limited and will withstand short-circuit-to-ground conditions. However, application of nonzero potential to the output pin may cause permanent damage and should be prevented by the proper precautions.

SETTLING TIME

Settling time of an amplifier is defined as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition.

Because settling time is affected by bandwidth which in turn is dependent upon closed loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling time vs. gain curves illustrate this effect for the 3551 at several levels of settling accuracy.

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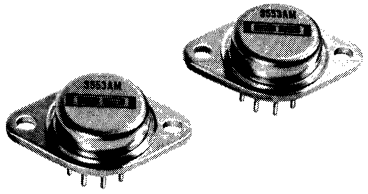

3553

Wideband - Fast-Slewing BUFFER AMPLIFIER

FEATURES

- GAIN = .99V/V
- OUTPUT CURRENT, ±200mA
- BANDWIDTH, 300MHz
- SLEW RATE, 2000V/μsec
- ELECTRICALLY ISOLATED CASE
- EXTENDS OP AMP DRIVING CAPABILITY WHILE PRESERVING BANDWIDTH & SETTLING TIME

DESCRIPTION

The 3553 is a unity-gain amplifier designed to be used either as a signal buffer, or as the power output stage for an operational amplifier. Because of its wideband response (300MHz, -3dB bandwidth) and fast slewing capability (2000V/μsec) the 3553 is capable of following very fast signals. When used inside the feedback loop of an operational amplifier, these high speed characteristics are essential in order to preserve the performance and stability of the feedback amplifier circuit.

With its ±200mA of output current capability, the 3553 is capable of driving a signal of ±10V into a 50Ω load. This power capability, coupled with its extremely high speed and wide bandwidth, makes the 3553 ideally suited for line driving applications where fast pulses or wideband signals are involved.

In addition to its fast/wideband characteristics and high output current, the 3553 has low input offset voltage and drift. This adds to its versatility, particularly in stand-alone buffer amplifier applications.

The 3553 is packaged in a reliable hermetically sealed TO-3 package for environmental ruggedness. The metal case is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated.

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PDS-329B

Printed in U.S.A. July, 1978

SPECIFICATIONS

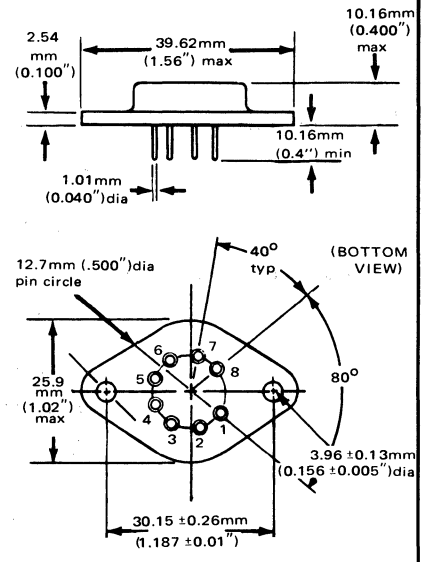
Specifications are typical at +25°C Case Temperature and ± 15 VDC power supply unless otherwise noted.

ELECTRICAL

MODEL	3553AM
GAIN, DC	
No Load	0.98 V/V
50 Ω Load, min	0.92 V/V
RATED OUTPUT	
Voltage, min	±10 V
Current, min	±200 mA
Output Resistance	1 Ω
DYNAMIC RESPONSE	
Slew Rate, min	2000 V/μsec
Full Power Bandwidth, min	32 MHz
Small Signal -3dB Bandwidth	300 MHz
Settling Time to 1%	7.2 nsec
to .01%	14.5 nsec
INPUT PARAMETERS	
Input Voltage, linear range	±10 V
Input Voltage, absolute, max	±Supply Voltage
Input Impedance	10^{11} Ω
Input Bias Current @ +25°C (doubles/+10°C)	-200 pA
OUTPUT OFFSET VOLTAGE	
Initial Offset @ +25°C, max	±50 mV
vs. Temperature (average) -25°C to +85°C	±300 μV/°C
POWER SUPPLY	
Rated Voltage	±15 VDC
Voltage Range, derated	±5 VDC to ±20 VDC
Current, Quiescent, max	±80 mA
typ	±50 mA
TEMPERATURE RANGE (Case)	
Specification	-25°C to +85°C
Operation (derate above +120°C Case)	-55°C to +125°C
Storage	-65°C to +150°C
θ_{JC} Thermal Resistance, junction to case	6°C/W
θ_{JA} Thermal Resistance, junction to ambient	33°C/W

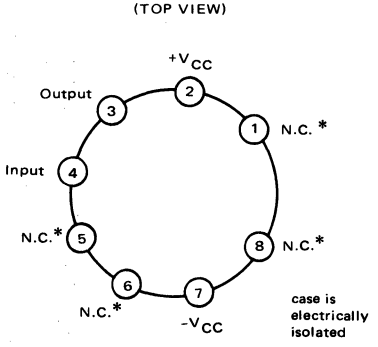
MECHANICAL

M PACKAGE (TO-3)



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

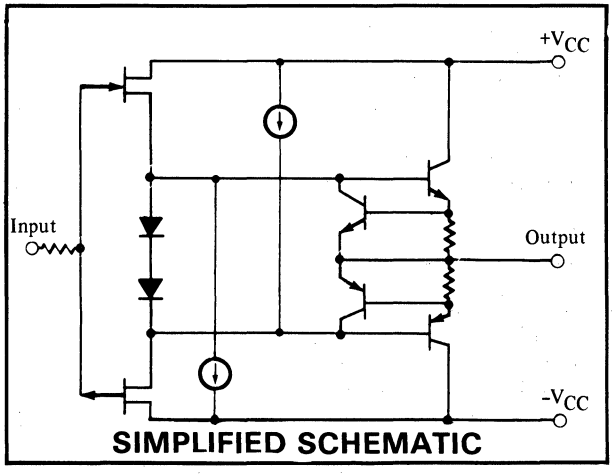
CONNECTION DIAGRAM



*No internal connection

CONNECTOR: 0803MC

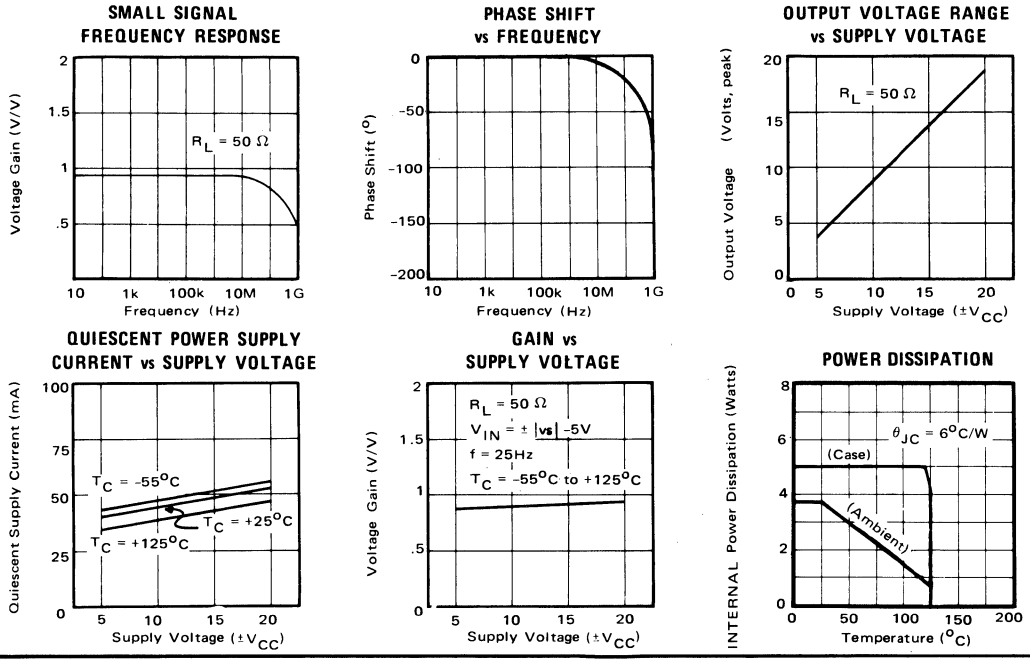
HEATSINKS: 0803HS 12°C/W
0804HS 4.2°C/W
0805HS 3°C/W



SIMPLIFIED SCHEMATIC

TYPICAL PERFORMANCE CURVES

Typical at 25°C and rated supply voltage unless otherwise noted.



APPLICATION INFORMATION

BOOSTER AMPLIFIER

One of the primary applications for the 3553 is that of a current booster for an operational amplifier. The circuit of Figure 1 is typical of such applications. Note that the 3553 is used inside the feedback loop and becomes, effectively, the output stage of the composite amplifier. Because the 3553 has unity voltage gain, wideband response, fast slewing rate, and very little phase delay, the dynamic response of the operational amplifier is virtually unaffected by the addition of the booster.

The already low offset voltage of the 3553 is effectively reduced by a factor equal to the open loop gain of the operational amplifier and becomes a negligible factor in total offset error of the circuit.

Input impedance of the 3553 is extremely high, thus requiring almost no drive current from the operational amplifier. On the other hand, the presence of the 3553 in the circuit increases the output current capability to ±200 mA, drastically lowers the output impedance of the loop, and permits the driving of low impedance loads such as a terminated 50Ω coaxial line.

Capacitive loads, often a source of instability and oscillations in operational amplifier circuits, are buffered by the presence of the 3553. In driving heavily capacitive loads the slew rate of the 3553 will be seen to decrease. This is due simply to the large currents required by fast voltage slewing in a capacitive load,

$$I_c = C_{load} \frac{dV}{dt}.$$

The internal current limit of the 3553 (approximately 600 mA) places a limit on the slewing rate under such conditions.

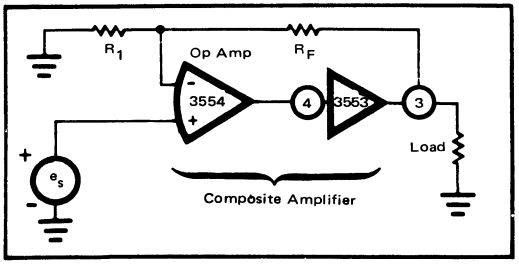


FIGURE 1. Model 3553 as a power booster.

BUFFER AMPLIFIER

The 3553 may also be used, as shown in Figure 2, as a unity gain buffer amplifier. No operational amplifier is required in this mode of operation. Since the 3553 is then operated without feedback, it's offset voltage and drift are translated to the output. While the gain is not precisely unity in this mode, the accuracy is adequate for many applications.

INPUT/OUTPUT PROTECTION

The output stage of the 3553 is current limited at approximately 600 mA. This will provide a measure of output short circuit protection for the amplifier for a period of time as determined by the heatsinking used, the amplifier's thermal resistance, the ambient temperature, etc. The amplifier's output stage transistors should not be allowed to exceed 150°C (175°C absolute max).

The input stage is designed to allow the application of either supply voltage without damage to the amplifier.

POWER DISSIPATION

The power dissipation capability of the 3553 varies with ambient temperature and with the type of heat sink used. A heat sink may be used to increase the dissipation capability or to achieve a given dissipation capability at higher temperature. The power derating curve is given in the typical performance curves on page 1-123.

WIRING RECOMMENDATIONS

No special wiring techniques are necessary with the 3553. However, it is recommended, as a good engineering practice, that the power supply lines be bypassed to common at a point near the amplifier. (A 1.0 μF electrolytic in parallel with a 1000 pF ceramic is recommended.) If the 3553 is used with a wideband operational amplifier, all leads must be kept as short as possible to minimize stray capacitance and unwanted feedback paths.

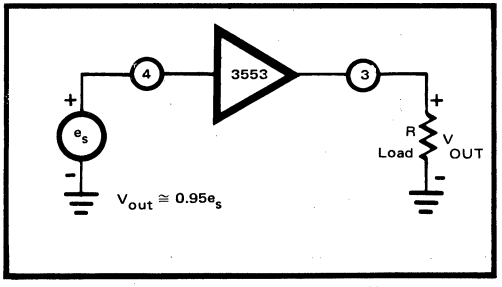
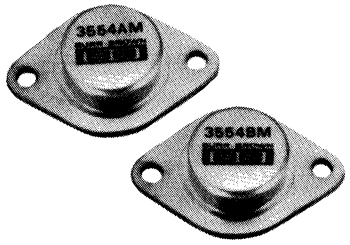


FIGURE 2. Model 3553 as a unity gain buffer.

BURR-BROWN®



3554

Wideband - Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- SLEW RATE, 1000V/μsec
- FAST SETTLING, 150nsec, max (to ±.05%)
- GAIN-BANDWIDTH PRODUCT, 1.7GHz
- FULL DIFFERENTIAL INPUT

APPLICATIONS

- PULSE AMPLIFIERS
- TEST EQUIPMENT
- WAVEFORM GENERATORS
- FAST D/A CONVERTERS

DESCRIPTION

The 3554 is a full differential input, wideband operational amplifier. It is designed specifically for the amplification or conditioning of wideband data signals and fast pulses. It features an unbeatable combination of gain-bandwidth product, settling time and slew rate. It uses hybrid construction. On the beryllia substrate are matched input FETs, thin-film resistors and high speed silicon dice. Active laser trimming and complete testing provide superior performance at a very moderate price.

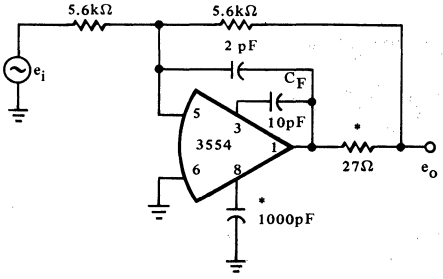
The 3554 has a slew rate of 1000V/μsec and will output ±10V and ±100mA. When used as a fast settling amplifier, the 3554 will settle to ±0.05% of the final value within 150nsec. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate or settling time in the particular application.

The 3554 is reliable and rugged and addresses almost any application when speed and bandwidth are serious considerations. It is particularly a good choice for use in fast settling circuits, fast D/A converters, multiplexer buffers, comparators, waveform generators, integrators, and fast current amplifiers. It is available in several grades to allow selection of just the performance required.

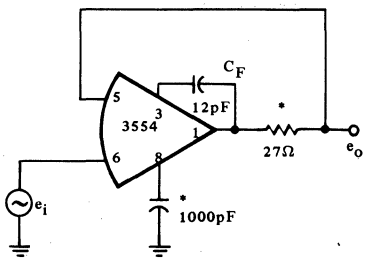
International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-331A

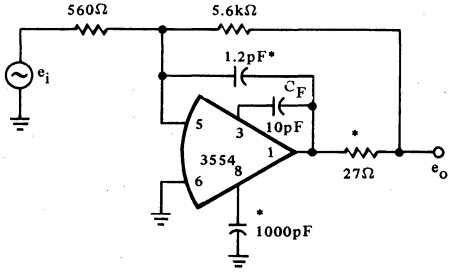
TYPICAL CIRCUITS



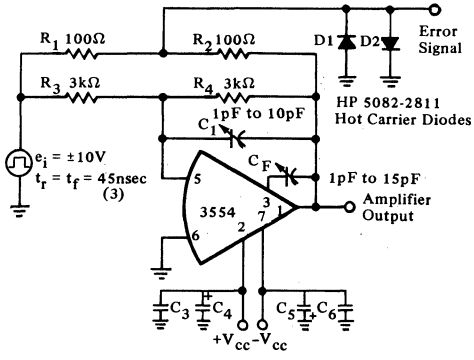
X1 Inverters



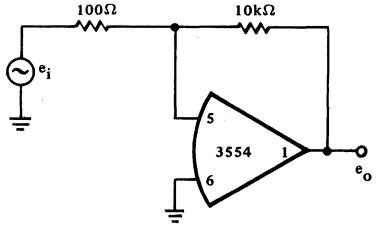
X1 Non-Inverter



X10 Inverter

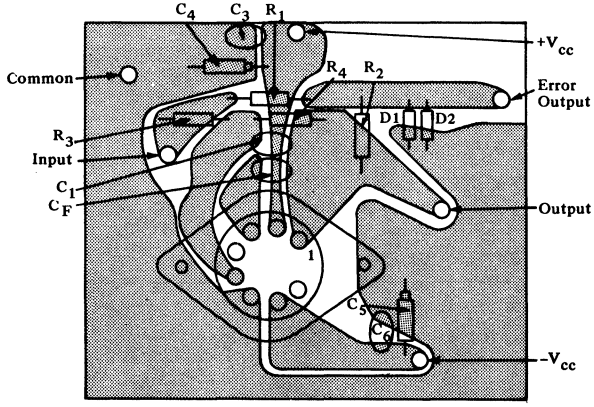


Settling Time Test Circuit Schematic



X100 Inverter

View from Component Side.
Shaded area is the pattern side conductor.



Settling Time Test Circuit Layout

NOTES:

1. These circuits are optimized for driving large capacitive loads (to 470pF).
2. The 3554 is stable at gains of greater than 55 ($C_L \leq 100pF$) without any frequency compensation.
3. 45nsec is optimum. Very fast rise times (10-20nsec) may saturate the input stage causing less than optimum settling time performance.

*Indicates component that may be eliminated when large capacitive loads are not being driven by the device.

ELECTRICAL SPECIFICATIONS

At T_{CASE} = 25°C and ±15VDC, unless otherwise noted.

PARAMETERS	CONDITIONS	3554AM			3554BM			3554SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN LOOP GAIN,DC					*	*	*	*	*	*	
No Load		100	106								dB
Rated Load	R_L = 100Ω	90	96								dB
RATED OUTPUT					*	*	*	*	*	*	
Voltage	I_O = ±100mA	±10	±11								V
Current	V_O = ±10V	±100	±125								mA
Output Resistance, open loop	f = 10MHz		20								Ω
DYNAMIC RESPONSE					*	*	*	*	*	*	
Bandwidth (0dB, small signal)	C_F = 0	70†	90								MHz
Gain-bandwidth Product	C_F = 0, G = 10 V/V	150	225								MHz
	C_F = 0, G = 100 V/V	425	725								MHz
	C_F = 0, G = 1000 V/V	1000	1700								MHz
Full Power Bandwidth	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	16	19								MHz
Slew Rate	C_F = 0, V_o = 20Vp-p, R_L = 100Ω	1000	1200								V/μsec
Settling Time to ±1%	A = -1		60								nsec
to ±.1%	A = -1		120								nsec
to ±.05%	A = -1		140	150							nsec
to ±.01%	A = -1		200	250							nsec
INPUT OFFSET VOLTAGE											
Initial offset, T_A = 25°C			±0.5	±2		±0.2	±1		±0.2	±1	mV
vs. Temp (T_A = -25°C to +85°C)			±20	±50		±8	±15				μV/°C
vs. Temp (T_A = -55°C to +125°C)									±12	±25	μV/°C
vs. Supply Voltage			±80	±300		*	*		*	*	μV/V
INPUT BIAS CURRENT					*	*	*	*	*	*	
Initial bias, 25°C		0	-10	-50							pA
vs. Temp			**								
vs. Supply Voltage			±1								pA/V
INPUT DIFFERENCE CURRENT					*	*	*	*	*	*	
Initial difference, 25°C			±2	±10							pA
INPUT IMPEDANCE						*			*		
Differential			10^{11} || 2								Ω || pF
Common-mode			10^{11} || 2								Ω || pF
INPUT NOISE					*	*	*	*	*	*	
Voltage, f_o = 1Hz	R_S = 100Ω		125	450†							nV/√Hz
f_o = 10 Hz	R_S = 100Ω		50	160†							nV/√Hz
f_o = 100 Hz	R_S = 100Ω		25	90†							nV/√Hz
f_o = 1 kHz	R_S = 100Ω		15	50†							nV/√Hz
f_o = 10 kHz	R_S = 100Ω		10	35†							nV/√Hz
f_o = 100 kHz	R_S = 100Ω		8	25†							nV/√Hz
f_o = 1 MHz	R_S = 100Ω		7	25†							nV/√Hz
f_B = .3 Hz to 10 Hz	R_S = 100Ω		2	7†							μV, p-p
f_B = 10 Hz to 1 MHz	R_S = 100Ω		8	25							μV, rms
Current, f_B = .3 Hz to 10 Hz	R_S = 100Ω		45								fA, p-p
f_B = 10 Hz to 1 MHz	R_S = 100Ω		2								pA, rms
INPUT VOLTAGE RANGE					*	*	*	*	*	*	
Common-mode Voltage Range	Linear Operation		±(V_{CC}-4)								V
Common-mode Rejection	f = DC, V_{CM} = +7V, -10V	44	78								dB
Max. Safe Input Voltage			±Supply								V
POWER SUPPLY					*	*	*	*	*	*	
Rated Voltage			±15								VDC
Voltage Range, derated performance		±5		±18							VDC
Current, quiescent		±17	±35	±45							mA
TEMPERATURE RANGE (ambient)											
Specification		-25		+85	-25		+85	-55		+125	°C
Operating, derated performance		-55		+125	-55		+125	-55		+125	°C
Storage		-65		+150	-65		+150	-65		+150	°C
θ junction-case			15			15			15		°C/W
θ junction-ambient			45			45			45		°C/W

* Specifications same as for 3554AM

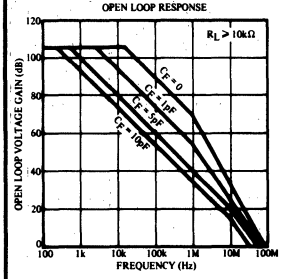
** Doubles every +10°C

† This parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.

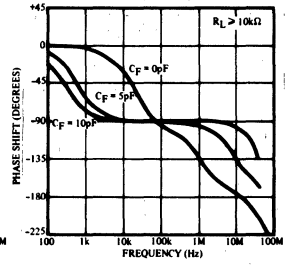
TYPICAL PERFORMANCE CURVES

at T_C = +25°C and ±15VDC unless otherwise noted.

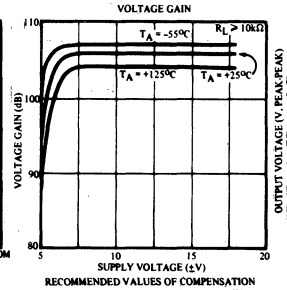
OPEN LOOP RESPONSE



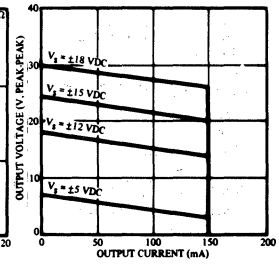
OPEN LOOP RESPONSE



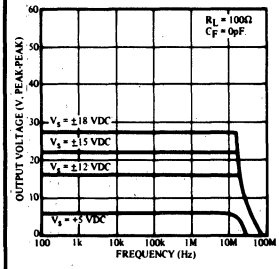
VOLTAGE GAIN



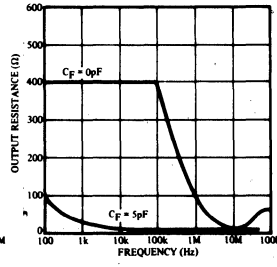
OUTPUT VOLTAGE VS OUTPUT CURRENT



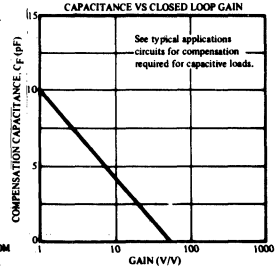
OUTPUT VOLTAGE



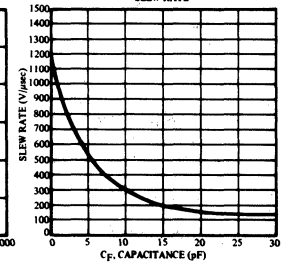
OPEN LOOP OUTPUT RESISTANCE VS FREQUENCY



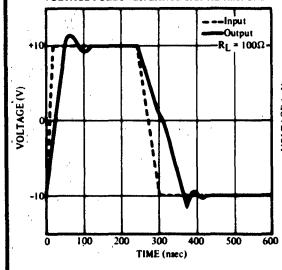
RECOMMENDED VALUES OF COMPENSATION CAPACITANCE VS CLOSED LOOP GAIN



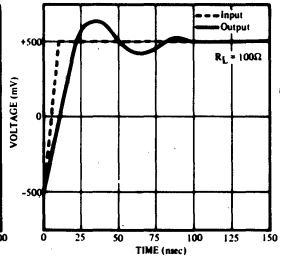
SLEW RATE



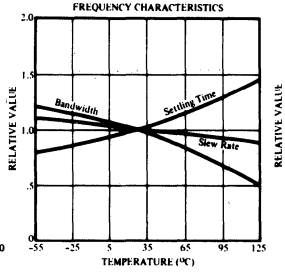
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



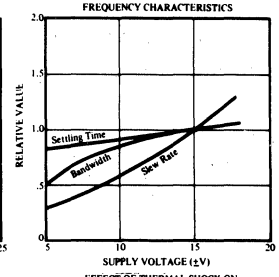
VOLTAGE FOLLOWER TRANSIENT RESPONSE



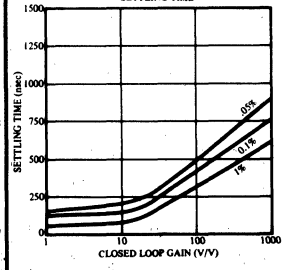
FREQUENCY CHARACTERISTICS



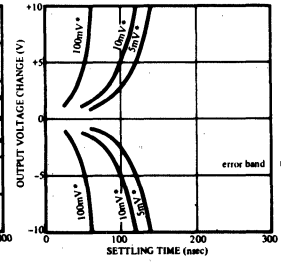
FREQUENCY CHARACTERISTICS



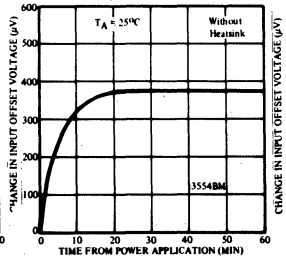
SETTLING TIME



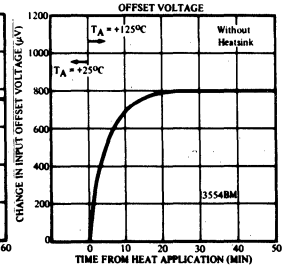
SETTLING TIME VS OUTPUT VOLTAGE CHANGE



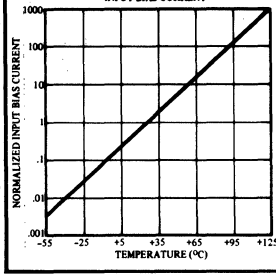
WARMUP DRIFT



EFFECT OF THERMAL SHOCK ON OFFSET VOLTAGE



INPUT BIAS CURRENT



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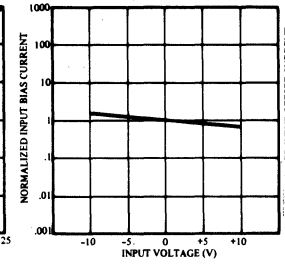
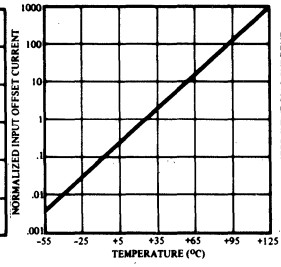
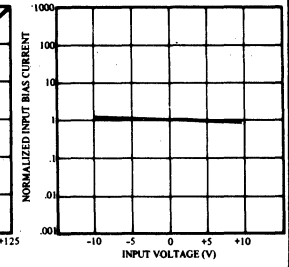
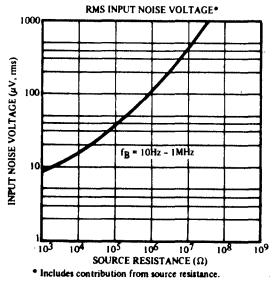


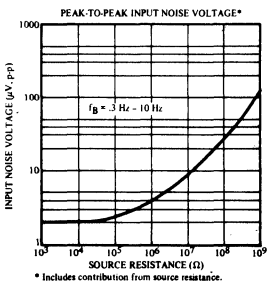
INPUT OFFSET CURRENT

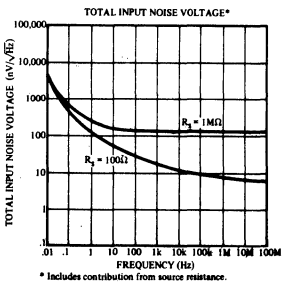


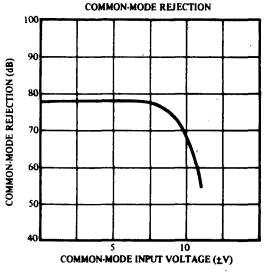
INPUT OFFSET CURRENT

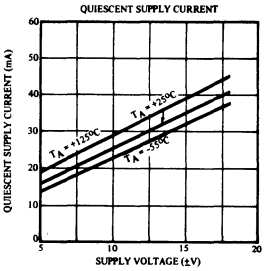


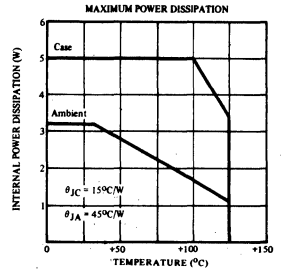




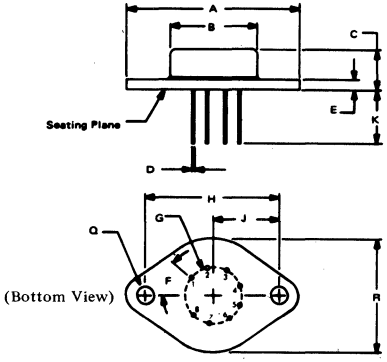








MECHANICAL



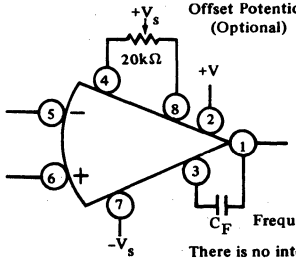
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

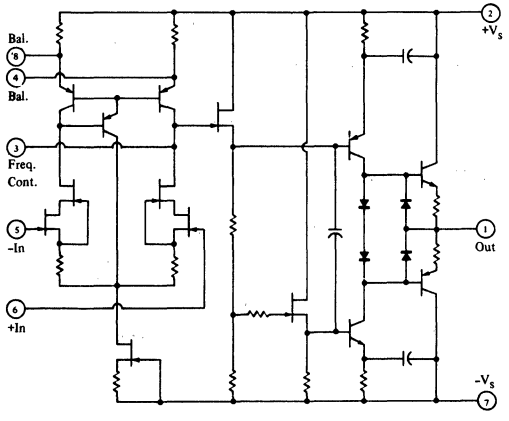
Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

AMPLIFIER CONNECTIONS





APPLICATIONS INFORMATION

WIRING PRECAUTIONS

The 3554 is a wideband, high frequency operational amplifier that has a gain-bandwidth product exceeding 1 Gigahertz. The full performance capability of this amplifier will be realized by observing a few wiring precautions and high frequency techniques.

Of all the wiring precautions, grounding is the most important and is described in an individual section. The mechanical circuit layout also is very important. All circuit element leads should be as short as possible. All printed circuit board conductors should be wide to provide low resistance, low inductance connections and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitances should be minimized especially at high impedance nodes such as the input terminals of the amplifier. Pin 5, the inverting input, is especially sensitive and all associated connections must be short. Stray signal coupling from the output to the input or to pin 8 should be minimized. A recommended printed circuit board layout is shown with the TYPICAL CIRCUITS. It also may be used for test purposes as described below.

When designing high frequency circuits low resistor values should be used; resistor values less than 5.6kΩ are recommended. This practice will give the best circuit performance as the time constants formed with the circuit capacitances will not limit the performance of the amplifier.

GROUNDING

As with all high frequency circuits a ground plane and good grounding techniques should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pick up. An example of an adequate ground plane and good high frequency techniques is the Settling Time Test Circuit Layout shown with the TYPICAL CIRCUITS.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A combination of a 1μF tantalum capacitor in parallel with a 470pF ceramic capacitor is a suitable bypass.

In inverting applications it is recommended that pin 6, the non-inverting input, be grounded rather than being connected to a bias current compensating resistor. This assures a good signal ground at the non-inverting input. A slight offset error will result; however, because the resistor values normally used in high frequency circuits are small and the bias current is small, the offset error will be minimal.

If point to point wiring is used or a ground plane is not, single point grounding should be used. The input signal return and the load signal return and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

It is recommended that the case of the 3554 not be grounded during use (it may, if desired). A grounded case will add a slight capacitance to each pin. To an already functional circuit grounding the case will probably require slight compensation readjustment and the compensation capacitor values will be slightly different from those recommended in the typical performance curves. There is no internal connection to the case.

Proper grounding is the single most important aspect of high frequency circuitry.

GUARDING

The input terminals of the 3554 may be surrounded by a guard ring to divert leakage currents from the input terminals. This technique is particularly important in low bias current and high input impedance applications. The guard, a conductive path that completely surrounds the two amplifier inputs, should be connected to a low impedance point which is at the input signal potential. It blocks unwanted printed circuit board leakage currents from reaching the input terminals. The guard also will reduce stray signal coupling to the input.

In high frequency applications guarding may not be desirable as it increases the input capacitance and can degrade performance. The effects of input capacitance, however, can be compensated by a small capacitor placed across the feedback resistor. This is described further in the COMPENSATION section.

COMPENSATION

The 3554 uses external frequency compensation so that the user may optimize the bandwidth or slew rate or settling time for his particular application. Several typical performance curves are provided to aid in the selection of the correct compensation capacitance value. In addition several typical circuits show recommended compensation in different applications.

The primary compensation capacitor, C_F, is connected between pins 1 and 3. As the performance curves show, larger closed loop gain configurations require less capacitance and an improved gain-bandwidth product will be realized. Note that no compensation capacitor is required for closed loop gains above 55 V/V and when the load capacitance is less than 100 pF.

When driving large capacitive loads, 470 pF and greater,

an additional capacitor, C_8, is connected between pin 8 and ground. This capacitor is typically 1000 pF. It is particularly necessary in low closed loop voltage gain configurations. The value may be varied to optimize performance and will depend upon the load capacitance value. In addition, the performance may be optimized by connecting a small resistance in series with the output and a small capacitor from pin 1 to 5. See the TYPICAL CIRCUITS for the X10 Inverter.

The flat high frequency response of the 3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2 pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin. Resistor values less than 5.6kΩ are recommended. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed loop gain. It will typically be 2 pF for a clean layout using low resistances (1kΩ) and up to 10 pF for circuits using larger resistances.

SETTLING TIME

Settling time is truly a complete dynamic measure of the 3554's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open loop gain. The settling time may be optimized for the particular application by selection of the closed loop gain and the compensation capacitance. The best settling time is observed in low closed loop gain circuits. A performance curve shows the settling time to three different error bands.

Settling time is defined as the total time required, from the signal input step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed loop gain or the bandwidth, per se. It is dependent upon compensation. Decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve. Stray capacitances may appear to the amplifier as compensation. To avoid limiting the slew rate performance, stray capacitances should be minimized.

CAPACITIVE LOADS

The 3554 will drive large capacitive loads (up to 1000 pF) when properly compensated. See the APPLICATIONS INFORMATION section on COMPENSATION. The effect of a capacitive load is to decrease the phase margin of the amplifier. With compensation the amplifier will provide stable operation even with large capacitive loads.

The 3554 is particularly well suited for driving 50Ω loads connected via coaxial cables due to its ±100mA output drive capability.The capacitance of the coaxial cable, 29 pF/foot of length for RG-58, does not load the amplifier when the coaxial cable or transmission line is terminated in the characteristic impedance of the transmission line.

OFFSET VOLTAGE ADJUSTMENT

The offset voltage of the 3554 may be adjusted to zero by connecting a 20kΩ linear potentiometer between pins 4 and 8 with the wiper connected to the positive supply. A small, non-inductive potentiometer is recommended. The leads connecting the potentiometer to pins 4 and 8 should be no longer than 6 inches to avoid stray capacitance and stray signal pickup. Stray coupling from the output, pin 1, to pin 4 (negative feedback) or to pin 8 (positive feedback) should be avoided.

The potentiometer is optional and may be omitted when the guaranteed offset voltage is considered sufficiently low for the particular application.

For each microvolt of offset voltage adjusted, the offset voltage temperature drift will change by ±0.004 μV/°C.

HEATSINKING

The 3554 does not require a heatsink for operation in most environments. The use of a heatsink, however, will reduce the internal thermal rise and will result in cooler operating temperatures. At extreme temperature and under full load conditions a heatsink will be necessary as indicated in the MAXIMUM POWER DISSIPATION curve. A heatsink with 8 holes for the 8 amplifier pins should be used. Burr-Brown has heatsinks available in three sizes – 3°C/W, 4.2°C/W and 12°C/W. A separate product data sheet is available upon request.

When heatsinking the 3554, it is recommended that the heatsink be connected to the amplifier case and the combination not connected to the ground plane. For a single sided printed circuit board, the heatsink may be mounted between the 3554 and the non-conductive side of the PC board, and insulating washers, etc., will not be required. The addition of a heatsink to an already functional circuit will probably require slight compensation readjustment for optimum performance due to the change in stray capacitances. The added stray capacitance from the heatsink to each pin will depend on the thickness and type of heatsink used.

SHORT CIRCUIT PROTECTION

The 3554 is short circuit protected for continuous output shorts to common. Output shorts to either supply will destroy the device, even for momentary connections. Output shorts to other potential sources are not recommended as they may cause permanent damage.

TESTING

The 3554 may be tested in conventional operational amplifier test circuits; however, to realize the full performance capabilities of the 3554, the test fixture must not limit the full dynamic performance capability of the amplifier. High frequency techniques must be employed. The most critical dynamic test is for settling time. The 3554 Settling Time Test Circuit Schematic and a test circuit layout is shown with the "Typical Circuits." The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. The layout exemplifies the high frequency considerations that must be observed. The layout also may be used as a guide for other test circuits. Good grounding, truly square drive signals, minimum stray coupling and small physical size are important.

Every 3554 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

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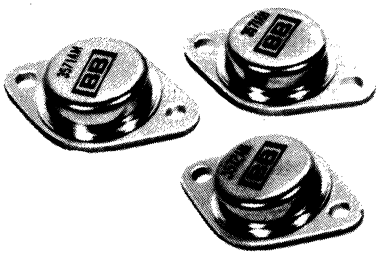

3571
3572

OPERATIONAL AMPLIFIERS

FEATURES

- HIGH CURRENT
  Up to 5A peak, 2A continuous
- EASY TO USE
  Adjustable current limits
  Electrically isolated case
  Small size - 8-pin TO-3 package
- HIGH VOLTAGE
  Up to 70V p-p output
- SELF-PROTECTED
  Self-contained automatic thermal sensing and shutdown
- HIGH POWER
  Delivers up to 70W to load

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PDS-334C

DESCRIPTION

The 3571AM and 3572AM are high output current integrated circuit operational amplifiers. Their performance, ease of use and compact size make them ideal to use in a variety of high current applications. They are especially well suited for driving permanent magnet DC servo and torque motors.

The equivalent circuit for the 3571AM and 3572AM is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

The input offset voltage at 25°C and the input offset voltage drift versus temperature are compensated by state-of-the-art laser trimming techniques. The offset voltage is low enough so that trimming will not be required in most applications. The excellent input characteristics and the high gain available mean that the use of a preamplifier, sometimes required with other servo type amplifiers, will not be necessary with the 3571AM and 3572AM.

The output stage is a class AB design which provides low distortion and minimizes quiescent current drain. The output circuitry provides for external current limiting resistors for both positive and negative output currents. This allows the user to select the current limit value suited to his particular application. This is especially desirable for driving permanent magnet motors where the high current seen during direction reversal (plugging) can demagnetize the motor.

The 3571AM and 3572AM have been designed to operate over a relatively wide supply range (±15VDC to ±40VDC) while still maintaining the high output current capability. This allows the user a wide range for the selection of the proper output voltage and current and makes the amplifiers useful for many different types of loads.

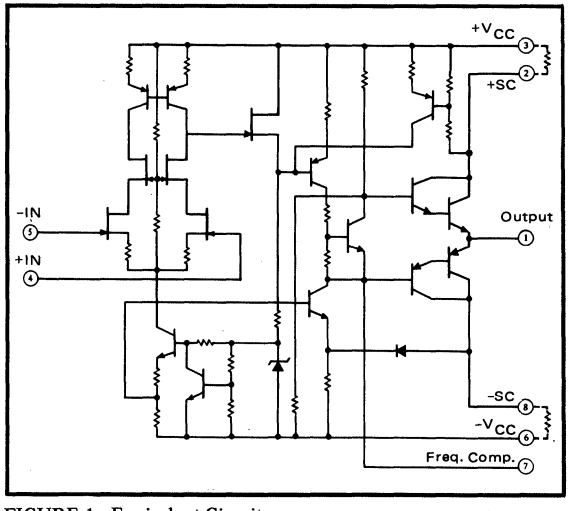


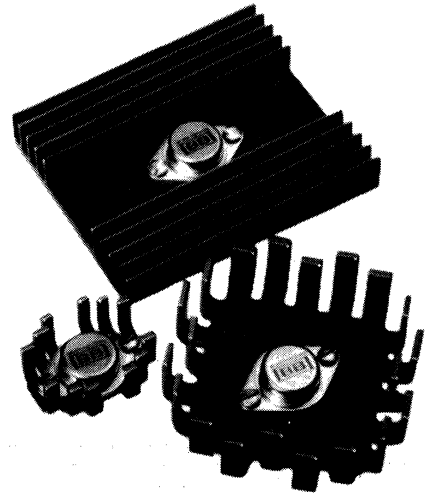
FIGURE 1. Equivalent Circuit.

The output circuit has a unique protection feature which is only practical in integrated circuit amplifiers – self-contained automatic thermal sensing and shut off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the amplifiers biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current may remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

Internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see POWER DERATING CURVE, page 1-136). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the SAFE OPERATING AREA curves (see page 1-136) must still be observed.

The 3571AM and 3572AM have several other features that improve their utility. For instance, the metal case of the units is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better than discrete component amplifiers. The small package size makes mounting more convenient.

Burr-Brown offers three heat sinks as accessories; 0803HS with a thermal resistance of 12°C/watt, 0804HS at 5.2°C/watt, and 0805HS at 3°C/watt. A convenient mating connector, 0803MC is also available.



SPECIFICATIONS

Typical @ T_{case} = 25°C and $\pm V_{CC}$ = ±35 VDC max unless otherwise noted.

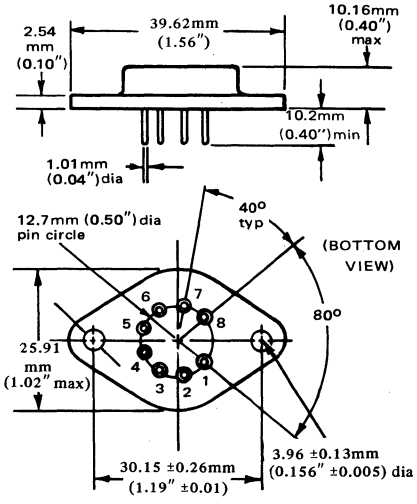
ELECTRICAL

MODELS	3571AM	3572AM
RATED OUTPUT (to load)		
Power to Load		
Continuous, min(1)	30 Watts	60 Watts
Peak, min(1)	60 Watts	150 Watts
Output Voltage, ±(|V_{CC}|-5)V		
Continuous, min(1)	±30V @ ±1A	±30V @ ±2A
Peak, min(1)	±30V @ 2A	±30V @ 5A
Load Capacitance	3300 pF	
DISSIPATION RATING		
at 25°C Case Temperature	33 Watts	50 Watts
Derating Above 25°C	See typical performance curves	
Thermal Resistance, Case to Free Air	30°C/Watt	
Thermal Time Constant (No heat sink)	2 minutes	
Thermal Resistance, Junction to Case	2.5°C/W	
POWER SUPPLY		
Voltage, $\pm V_{CC}$	±15 to ±40 VDC	
Quiescent Current, max	±35 mA	
OPEN LOOP		
Gain min, at R_{load} = 30Ω (3572AM) R_{load} = 60Ω (3571AM)	94 dB	
Output Impedance	2.5 Ω	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	500 kHz	
Full Power Bandwidth	16 kHz @ Vpk = 30 V	
Slew Rate, C_C = 1000 pF	3V/μs	
INPUT OFFSET VOLTAGE		
Initial @ 25°C, max	±2mV	
Drift vs. Temp., max	±40 μV/°C	
Drift vs. Supply Voltage	±100 μV/V	
Drift vs. Time	50 μV/mo	
Drift vs. Power Dissipation (T_C constant)	20 μV/Watt	
INPUT BIAS CURRENT		
Initial @ 25°C, max	-100 pA	
Drift vs. Temp.	doubles every 10°C	
Drift vs. Supply Voltage	0.5 pA/V	
INPUT OFFSET CURRENT		
Initial @ 25°C	±50 pA	
Drift vs. Temp.	doubles every 10°C	
Drift vs. Supply Voltage	0.5 pA/V	
INPUT IMPEDANCE		
Differential	10^{11} Ω‖10 pF	
Common-Mode	10^{11}Ω	
INPUT NOISE		
Voltage 0.01 Hz to 10 Hz, p-p	4 μV	
10 Hz to 1 kHz, RMS	3 μV	
Current 0.01 Hz to 10 Hz, p-p	1 pA	
10 Hz to 1 kHz, RMS	0.1 pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage	(+V_{CC} + | -V_{CC} |)	
Max Safe Common-Mode Voltage	+V_{CC} to -V_{CC}	
Common-Mode Voltage, Linear Operation	±(|V_{CC}|-10)V	
Common-Mode Rejection	80 dB min., 90 dB, typ.	
TEMPERATURE RANGE (Case)		
Specification	-25°C to +85°C	
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	
ACCESSORIES		
Heat Sink	0803HS (12°C/W)	
	0804HS (5.2°C/W)	
	0805HS (3°C/W)	
Connector	0803MC	

(1) SAFE OPERATING AREA and POWER DERATING limitations must be observed.

MECHANICAL

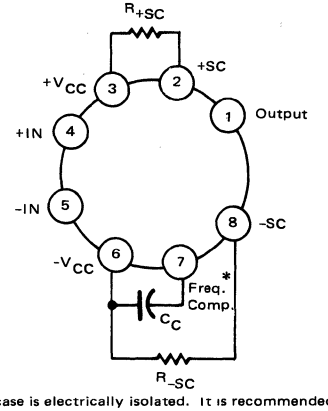
"M" PACKAGE (TO-3)



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std 883 [except paragraph 3.2.].

Connection Diagram

(TOP VIEW)



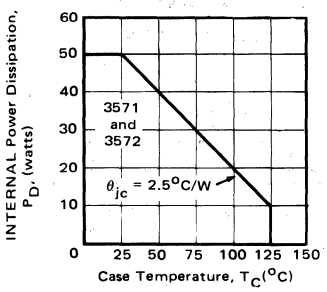
The case is electrically isolated. It is recommended that the case be grounded during use.

* A 1000 pF ±20% ceramic capacitor is recommended for all circuit configurations and at all amplifier gains. The capacitor's lead lengths should be short. For gains above 10 V/V, C_c is not absolutely required.

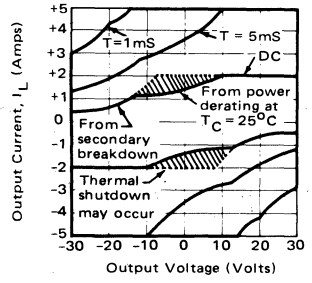
TYPICAL PERFORMANCE CURVES

(Typical T_{case} = 25°C and $\pm V_{CC}$ = ±35 VDC unless otherwise noted.)

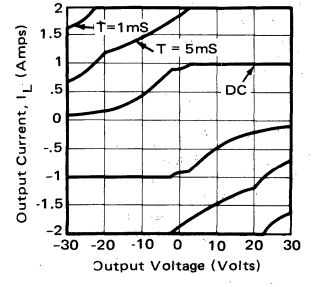
POWER DERATING



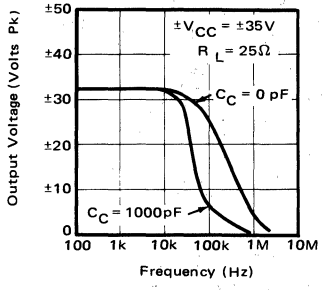
3572 SAFE OPERATING AREA



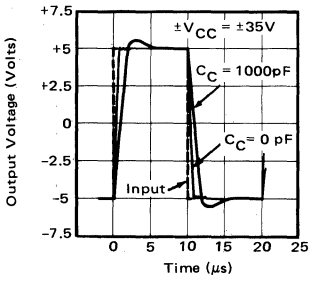
3571 SAFE OPERATING AREA



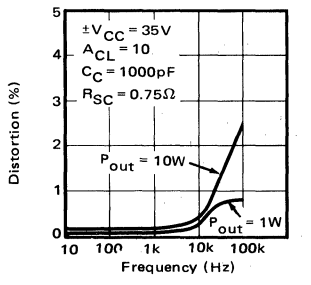
OUTPUT VOLTAGE VS. FREQUENCY



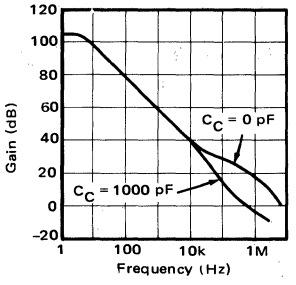
VOLTAGE FOLLOWER PULSE RESPONSE



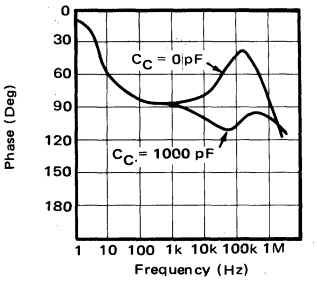
DISTORTION VS. FREQUENCY



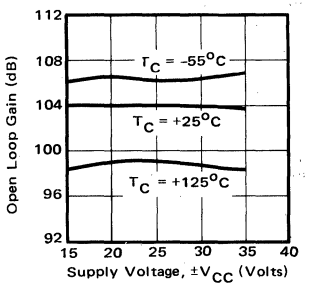
OPEN LOOP GAIN VS. FREQUENCY



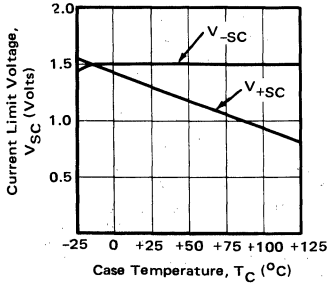
OPEN LOOP PHASE



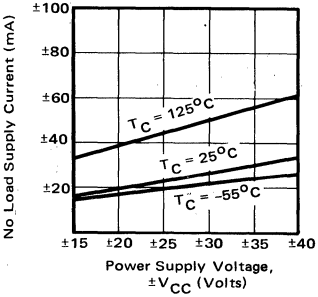
OPEN LOOP GAIN VS. SUPPLY VOLTAGE



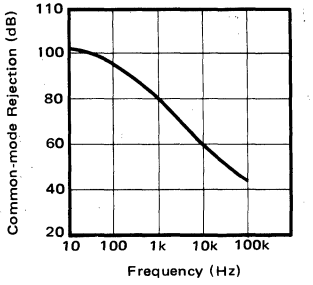
CURRENT LIMIT VOLTAGE VS. TEMPERATURE



QUIESCENT CURRENT VS. SUPPLY VOLTAGE



COMMON-MODE REJECTION VS. FREQUENCY



INSTALLATION and OPERATING INSTRUCTIONS

General Precautions

CURRENT LIMITING

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250 mA ($R_{SC} \cong 5.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

MINIMUM HEAT SINK

The 3571AM and 3572AM require a minimum heat sink of 16°C/watt or lower in order to insure thermal stability (mounting on a 3″ x 3″ x 0.06″ piece of 80% copper-clad printed circuit board material will be sufficient). Normally this will not be a consideration since a larger heat sink will be used to provide the proper power dissipation as described in the THERMAL CONSIDERATIONS section which follows.

PROPER GROUNDING & POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground loop errors. Figure 2 illustrates proper connections.

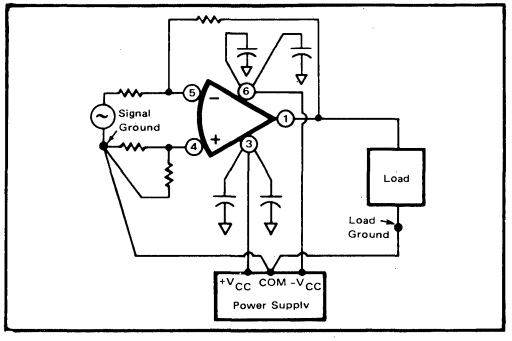


FIGURE 2. Proper power supply connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power supply bypassed with 50 μF tantalum capacitors connected in parallel with 0.01 μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

Current Limits

The amplifiers are designed so that both the positive and negative load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equations:

$$R_{+SC} = \frac{1.3\ (\text{volts})}{I_{+\text{limit}}(\text{amps})}, \quad R_{-SC} = \frac{1.5\ (\text{volts})}{I_{-\text{limit}}(\text{amps})}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{SC}(I_{limit})^2$. The current limits determined by the equations above are accurate to about ±10%. The variation of I_{limit} vs. temperature is shown in the Typical Performance Curves. Both $+V_{CC}$ and $-V_{CC}$ must be on for the current limits to function.

To avoid introducing unwanted inductance into the current limit circuitry, which may introduce oscillations and permanent damage, both current limit resistors must be non-inductive. Do not use wire wound resistors. Carbon composition resistors are preferred and paralleling them can provide a wide current limit range at the wattage needed.

The maximum value of the negative current limit resistor is 15 ohms (100 mA, minimum). Exceeding this value, or an open circuit, could permanently damage the internal 75Ω, thin-film resistor which parallels R_{-SC}.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

Thermal Considerations

The 3571AM and 3572AM are rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.5°C per watt. The corresponding Power Derating Curve is given in the Typical Performance Curves section.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DL}$ where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipated in the output stage due to the load. (For $\pm V_{CC} = \pm 40V$, $P_{DQ} = 80 \times 0.035 = 2.8$ watts max) For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{out}$) the maximum value of P_{DL} occurs at $\pm V_{out} = \frac{\pm V_{CC}}{2}$ and is equal to $P_{DL_{max}} = \frac{(\pm V_{CC})^2}{4R_L}$. Figure 3 shows P_D as function of the output voltage with the load resistance as a running parameter.

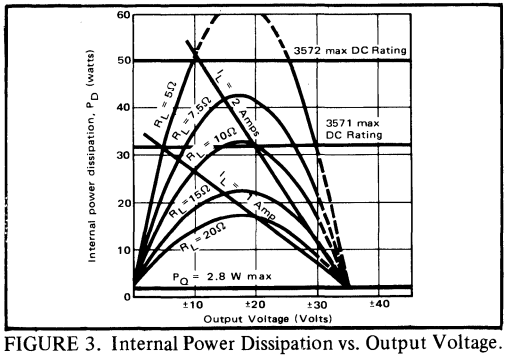


FIGURE 3. Internal Power Dissipation vs. Output Voltage.

P_{DL} for any other value of V_{out} can be computed from $P_{DL} = (\pm V_{CC} - \pm V_{out}) \cdot I_L = (\pm V_{CC} - \pm V_{out})\left(\frac{\pm V_{out}}{R_L}\right)$.

The use of an adequate heat sink is mandatory and thermal resistance of the heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = \frac{T_J - T_A}{P_D} - \theta_{jc}$$

where T_J is the desired amplifier junction temperature (+150°C max), T_A is the ambient temperature, P_D is the amplifiers dissipation, $P_D = P_{DO} + P_{DL}$, and θ_{jc} is the junction to case thermal resistance of the amplifier. Burr-Brown Application Note AN-83 entitled, "How to Determine What Heatsink to Use", is available for additional information.

The electrically isolated case of the 3571AM and 3572AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

SAFE OPERATING AREA

There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the SAFE OPERATING AREA CURVES in the Typical Performance Curves.

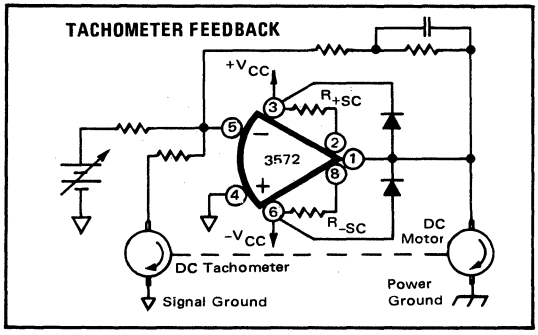
APPLICATION CONSTRAINT

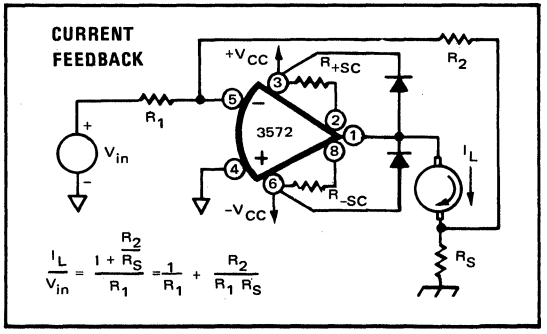
Because of the possibility of damaging the output stage if frequency instability (oscillations) occurs, applications with an inductive load which will activate the current limit of the amplifier, are constrained to have a load impedance phase angle of less than 60° leading, over the frequency band of 10kHz to 100kHz. Increasing the load's series resistance will decrease the phase angle, if necessary. Larger inductive loads may be applied if current limit is not activated.

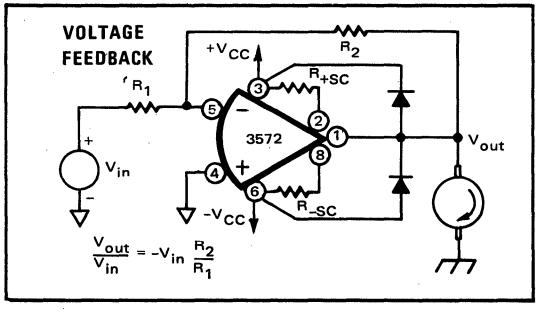
FREQUENCY COMPENSATION

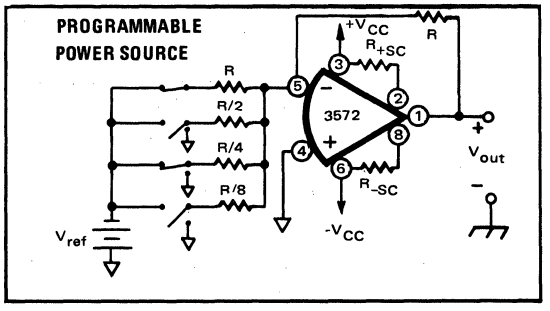
The optimum value of the compensation capacitor is 1000 pF. A ±20% tolerance ceramic capacitor is recommended. The compensation capacitor should be used with all circuit configurations and at all amplifier gains.

TYPICAL APPLICATIONS



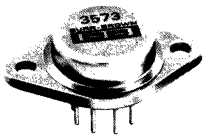






BURR-BROWN®

3573



High Current - High Power OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT POWER
  100 Watts Peak
  40 Watts Continuous
- WIDE SUPPLY RANGE
  ±10 to ±34 Volts
- HIGH OUTPUT CURRENT
  ±5 Amps Peak
  ±2 Amps Continuous
- SMALL SIZE: TO-3 PACKAGE
- LOW COST

APPLICATIONS

- DC MOTORS
- AC MOTORS
- ACTUATORS
- ELECTRONIC VALVES
- SYNCROS

DESCRIPTION

If you need to supply 100 watts peak or 40 watts continuous, yet must choose a small, easy to use op amp, you'll find the 3573 a logical solution. This hybrid IC delivers ±5A peak minimum at ±20V minimum to the load when operated from ±28V power supplies. The design of this op amp has been optimized for low cost while preserving moderately good input and distortion characteristics.

Output circuitry provides for external current limiting resistors for both positive and negative currents. This allows current limits to be set to values dictated by the op amp's application. 3573 is internally frequency compensated and is unconditionally stable with capacitive loads to 3300pF.

Housed in a small, rugged, hermetically sealed 8-lead TO-3 package, 3573 will withstand severe environments far better than discrete component amplifiers. The metal case is completely electrically isolated from the amplifier circuitry. Thus, mounting is easier (no isolation washers or spacers) and the hazards of a case connected to the output or supply voltage is eliminated.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-393

ELECTRICAL SPECIFICATIONS

At T_{case} = 25°C and $\pm V_{CC}$ = ±28VDC unless otherwise noted.

PARAMETER	CONDITIONS	3573AM MIN	3573AM TYP	3573AM MAX	UNITS
OPEN LOOP GAIN, DC	$R_L \geq 30\Omega$	94	115		dB
RATED OUTPUT					
Power to Load[1]					
Continuous		40			W
Peak		100			W
Output Current					
Continuous		±2			A
Peak		±5			A
Output Voltage	I_{out} = ±5A[4]	±20	±23		V
DYNAMIC RESPONSE					
Bandwidth, Unity Gain	Small Signal		1		MHz
Full Power Bandwidth		15	23		kHz
Slew Rate		1.5	2.6		V/µs
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±10	mV
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±10	±65	µV/°C
vs Supply Voltage			±35		µV/V
INPUT BIAS CURRENT					
Initial	T_{case} = 25°C		15	40	nA
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±0.05		nA/°C
vs Supply Voltage			±0.02		nA/V
INPUT DIFFERENCE CURRENT					
Initial	T_{case} = 25°C		±5	±10	nA
vs Temperature	-25°C ≤ T_{case} ≤ 85°C		±0.01		nA/°C
INPUT IMPEDANCE					
Differential			10		MΩ
Common-mode			250		MΩ
INPUT NOISE					
Voltage Noise	f_n = 0.3Hz to 10Hz		3		µV p-p
	f_n = 10Hz to 10kHz		5		µVrms
Current Noise	f_n = 0.3Hz to 10Hz		20		pA p-p
	f_n = 10Hz to 10kHz		4.5		pA rms
INPUT VOLTAGE RANGE					
Common-mode Voltage	Linear Operation	±($\lvert V_{CC}\rvert$-6)	±($\lvert V_{CC}\rvert$-3)		V
Common-mode Rejection	f = DC, V_{CM} = ±22	70	110		dB
POWER SUPPLY					
Rated Voltage			±28		V
Voltage Range, derated		±10		±34	V
Current, quiescent			±2.6	±5	mA
TEMPERATURE RANGE					
Operating	T_{case}	-25		+85	°C
Storage		-65		+150	°C

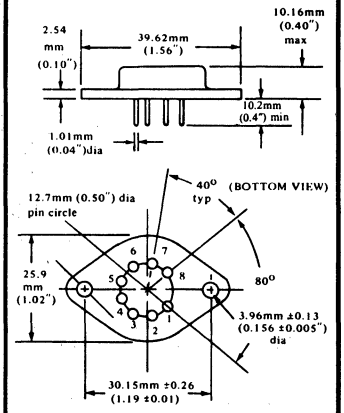
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	±34VDC
Internal Power Dissipation[1]	45W
Differential Input Voltage[2]	±62VDC
Input Voltage Range[2]	±31VDC
Storage Temperature Range	-65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Output Short-Circuit Duration[3]	Continuous
Junction Temperature	150°C

1. Package must be derated based on a junction to case thermal resistance of 2.8°C/W, or a junction to ambient thermal resistance of 30°C/W.
2. For supply voltages less than ±34VDC, the absolute maximum voltage is three volts less than supply voltage.
3. Safe Operating Area and Power Derating Curves must be observed.
4. With R±SC = 0.

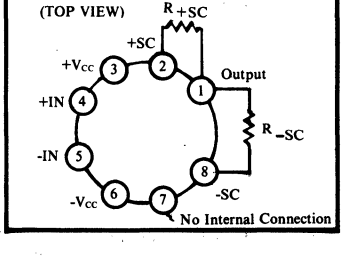
MECHANICAL

TO-3



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

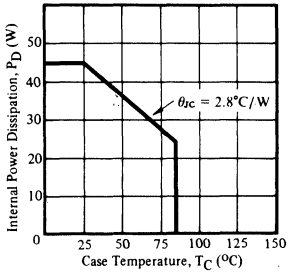
CONNECTION DIAGRAM



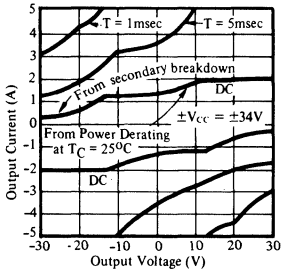
TYPICAL PERFORMANCE CURVES

(Typical at 25°Case and $\pm V_{CC} = \pm 28$ VDC unless otherwise noted.)

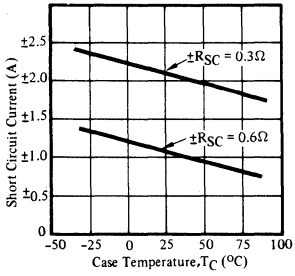
POWER DERATING CURVE



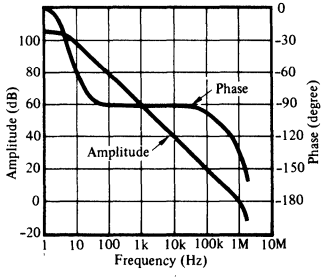
SAFE OPERATING AREA



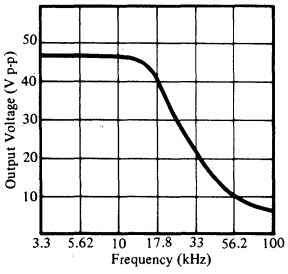
CURRENT LIMITING



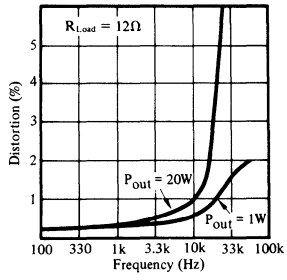
OPEN LOOP FREQUENCY RESPONSE



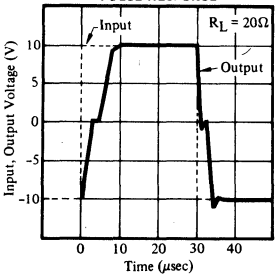
OUTPUT VOLTAGE VS FREQUENCY



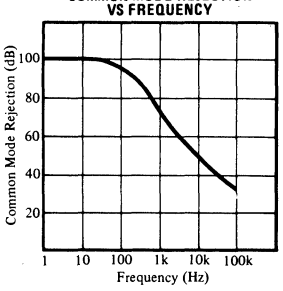
HARMONIC DISTORTION



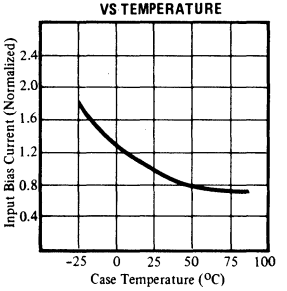
VOLTAGE FOLLOWER PULSE RESPONSE



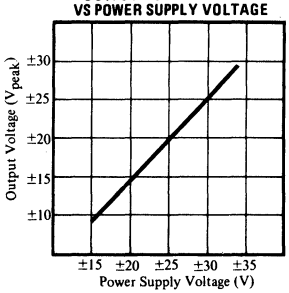
COMMON MODE REJECTION VS FREQUENCY



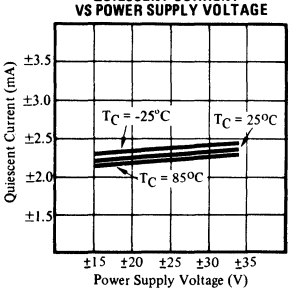
INPUT BIAS CURRENT VS TEMPERATURE



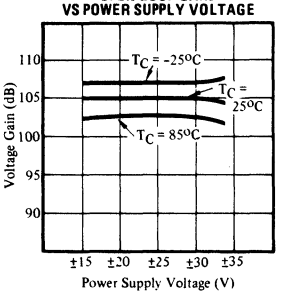
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



QUIESCENT CURRENT VS POWER SUPPLY VOLTAGE



OPEN LOOP GAIN VS POWER SUPPLY VOLTAGE



INSTALLATION AND OPERATING INSTRUCTIONS

GENERAL PRECAUTIONS

CURRENT LIMITING

It is recommended that during initial amplifier setup, particularly in breadboarding and when a lack of familiarity with the amplifier exists, that the current limit be set at about 250mA ($R_{SC} \cong 2.6\Omega$). This will allow verification of the circuit and will minimize the possibility of damaging the amplifier. Later, when the circuit configuration and connections have been proven, the current limits can be raised to the desired value.

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Particular attention should be given to proper grounding practices because the large output currents can cause significant ground loop errors. Figure 1 illustrates proper connections.

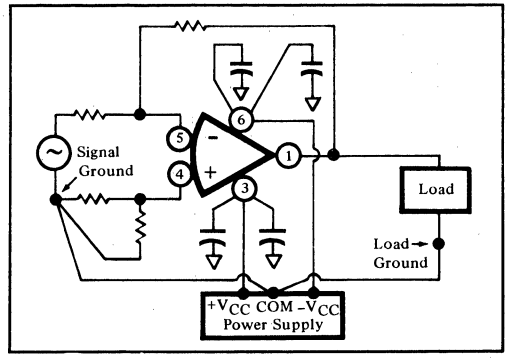

FIGURE 1. Proper Power Supply Connections.

Note that the connections are such that the load current does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power supply bypassed with 50μF tantalum capacitors connected in parallel with 0.01 μF ceramic capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The amplifier is designed so that both the positive and negtive load current limits can be adjusted with external resistors, R_{+SC} and R_{-SC} respectively. The value of the resistors are given by the following equation:

$$R_{SC} = \frac{0.65 \text{ (volts)}}{I_{limit} \text{ (amps)}}$$

I_{limit} is the desired maximum current. The maximum power dissipation of the resistors is $P_{max} = R_{SC} (I_{limit})^2$. The current limits determined by the equations above are accurate to about ±10%. The variation of I_{limit} vs temperature is shown in the Typical Performance Curves.

The amplifier should be used with as low a current limit as possible for the particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and increase reliability by limiting the internal power dissipation of the amplifier.

THERMAL CONSIDERATIONS

The 3573AM is rated for 150°C maximum junction temperature. The thermal resistance from junction to case (θ_{jc}) is 2.8°C/W per watt. The corresponding Power Derating Curve is given in the Typical Performance Curves section.

The internal power dissipation of the amplifier is given by the equation $P_D = P_{DQ} + P_{DL}$ where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipated in the output stage due to the load.

The thermal resistance of the required heat sink (θ_{hs}) can be determined from the equation:

$$\theta_{hs} = \frac{T_J - T_A}{P_D} - \theta_{jc}$$

where T_J is the desired amplifier junction temperature (+150°C max), T_A is the ambient temperature, P_D is the amplifier's dissipation, $P_D = P_{DQ} + P_{DL}$, and θ_{jc} is the junction to case thermal resistance of the amplifier.

The electrically isolated case of the 3573AM simplifies mounting the amplifiers to the heat sink (and the heat sink to any other assemblies) since there is no need for electrical insulation. Thermal joint compound and lock washers should be used to prevent mechanical relaxation due to thermal stresses.

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There are additional constraints on the output voltage and current other than those just due to the maximum internal power dissipation of the amplifiers. These are related to the prevention of secondary breakdown in the output stage transistors. These restrictions are shown in the SAFE OPERATING AREA CURVES in the Typical Performance Curves.

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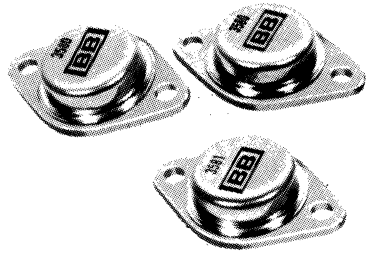

3580
3581
3582

High Voltage OPERATIONAL AMPLIFIERS

FEATURES

- HIGH OUTPUT SWINGS, up to ±145V (3582)
- LARGE LOAD CURRENTS, up to ±60mA (3580)
- DIFFICULT TO DAMAGE, automatic thermal shutoff
- REDUCES SOURCE LOADING, 10^{11} Ω Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA bias current

DESCRIPTION

The 3580 series is the first family of Integrated Circuit operational amplifiers which will provide output voltage swings of up to ±145V.

The monolithic FET input stage has low bias currents (20pA) which minimized the offset voltages caused by the bias current and the large resistance normally associated with high voltage circuits.

The 3580 series is packaged in a TO-3 package which will dissipate over 3W of power without a heat sink and 4.5W with a suitable heat sink.

The input stage is protected against overvoltages and the output stage is protected against short-circuits-to-ground. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

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PDS-313A

THEORY OF OPERATION

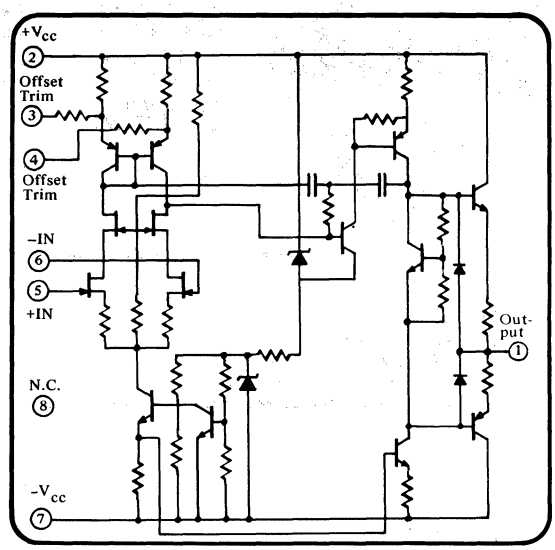


FIGURE 1. Simplified Schematic of 3580.

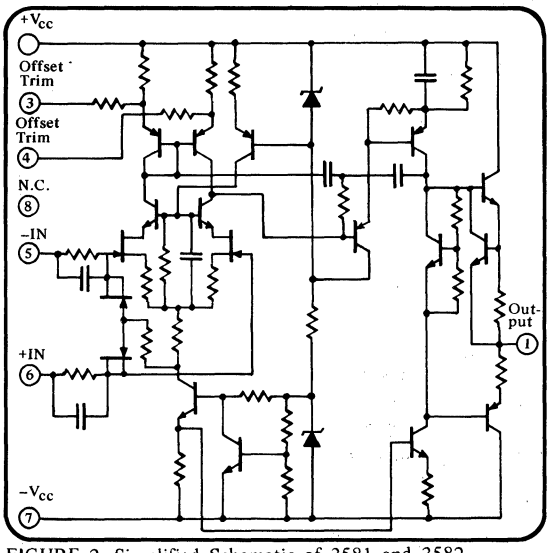


FIGURE 2. Simplified Schematic of 3581 and 3582.

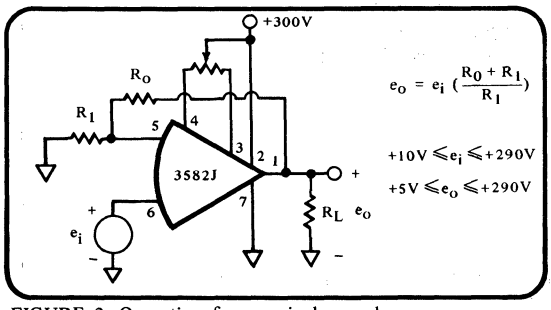


FIGURE 3. Operation from a single supply.

The 3580 family of integrated circuit high voltage amplifiers provides performance which previously was only available in bulky modular packages. In addition to the smaller size and inherent reliability, the integrated circuit construction offers other advantages not normally available in modular or discrete component units. The amplifiers have thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating the input stage current source when the temperature reaches a critical level. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases.

If the cause of the abnormal power dissipation is continuous (such as a short circuit across the load) the output current may remain at a low value or oscillate between 2 values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will allow the use of a smaller heat sink than would otherwise be required. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormal conditions.

Another unique feature of the 3580 family is the thorough testing the unit receives. In addition to the normal tests, all amplifiers are 100% tested for input protection at its full rated differential voltage ($+V_{CC}$-V_{CC}). Each unit is also 100% tested for output short circuit to common at maximum supply voltage.

The 3581 and 3582 have an unique feature that is important in many high voltage applications. In these two models the input bias current is virtually independent of the applied common mode voltage. This is accomplished by the true cascode input stage which keeps the drain to source voltage of the input transistors constant as the common mode voltage changes.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 3 illustrates a typical application.

Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the 3581 and 3582 amplifiers are operated from a single supply, the output stage, which is still short circuit current limited and thermally protected, is not protected against short circuits to ground (the 3580 will still be short circuit protected under these conditions). When the amplifiers are operated from a single supply, the voltage across one of the output transistors is high enough that secondary breakdown is a consideration. The output current must be limited in order to prevent damage. This can be done by keeping the load resistor larger than 5k ohms for the 3582 and greater than 1k ohm for the 3581.

SPECIFICATIONS

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

ELECTRICAL

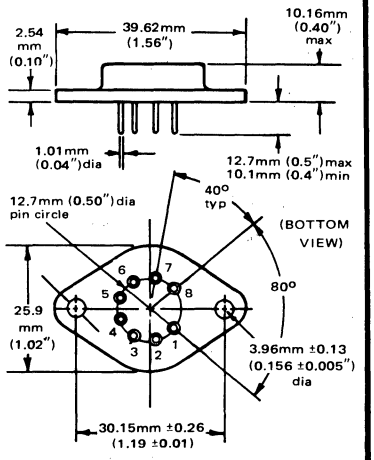
MODELS	3580J	3581J	3582J
POWER SUPPLY			
Voltage, $\pm V_{cc}$	±15 to ±35 Vdc	±32 to ±75 Vdc	±70 to ±150 Vdc
Quiescent Current, max	±10 mA	±8 mA	±6.5 mA
RATED OUTPUT			
Voltage, $\pm(\lvert V_{cc}\rvert -5)$Vdc, min	±10 to ±30 Vdc	±27 to ±70 Vdc	±65 to ±145 Vdc
Current, min	±60 mA	±30 mA	±15 mA
Current, Short Circuit	±100 mA	±50 mA	±25 mA
Load Capacitance, max	*	10 nF	*
OPEN LOOP GAIN			
No Load, dc	106 dB	112 dB	118 dB
Rated Load, dc , min	86 dB	94 dB	100 dB
FREQUENCY RESPONSE			
Unity Gain Bandwidth, Small Signal	*	5 MHz, min	*
Full Power Bandwidth	100 kHz	60 kHz	30 kHz
Slew Rate	15 V/μs	20V/μs	20 V/μs
Settling Time, 0.1%	*	12 μs	*
INPUT OFFSET VOLTAGE			
Initial @ 25°C, max	±10 mV	±3 mV	±3 mV
Drift vs Temp, max	±30 μV/°C	±25 μV/°C	±25 μV/°C
Drift vs Supply Voltage	100 μV/V	20 μV/V	20 μV/V
Drift vs Time	100 μV/mo	50 μV/mo	50 μV/mo
INPUT BIAS CURRENT			
Initial @ 25°C, max	-50 pA	-20 pA	-20 pA
Drift vs Temp		doubles every 10°C	
Drift vs Supply Voltage	0.5 pA/V	0.2 pA/V	0.2 pA/V
INPUT OFFSET CURRENT			
Initial @ 25°C	*	±20 pA	*
Drift vs Temp	*	doubles every 10°C	*
Drift vs Supply Voltage	0.5 pA/V	0.2 pA/V	0.2 pA/V
INPUT IMPEDANCE			
Differential	*	$10^{11}\ \Omega \parallel 10$ pF	*
Common Mode	*	$10^{11}\ \Omega$	*
INPUT NOISE			
Voltage 0.01 Hz to 10 Hz p-p	*	5μV	*
10 Hz to 1 kHz rms	1 μV	1.7μV	1.7μV
Current 0.01 Hz to 10 Hz p-p	1 pA	0.3 pA	0.3 pA
INPUT VOLTAGE RANGE			
Max Safe Differential Voltage (1)	*	$(+V_{cc} + \lvert -V_{cc}\rvert)$	*
Max Safe Common Mode Voltage	*	$+V_{cc}$ to $-V_{cc}$	*
Common Mode Voltage, Linear Operation	$\pm(\lvert V_{cc}\rvert -8)$V	$\pm(\lvert V_{cc}\rvert -10)$V	$\pm(\lvert V_{cc}\rvert -10)$V
Common Mode Rejection	86 dB	110 dB	110 dB
TEMPERATURE RANGE (Case)			
Specification	*	0°C to 70°C	*
Operating	*	-55°C to +125°C	*
Storage	*	-55°C to +150°C	*

*Specifications same for all models.

(1) On Models 3581 and 3582 the inputs may be damaged by pulses at pins 5 or 6 with $dV/dt \geq 1V/ns$. Any possible damage can be eliminated by limiting the input current to 150 mA with external resistors in series with those pins. No external protection is needed for slower voltage.

MECHANICAL

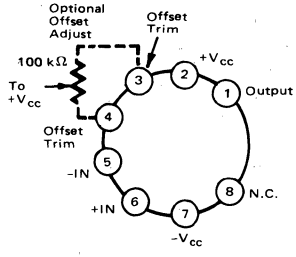
TO-3



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

CONNECTION DIAGRAM

(TOP VIEW) *



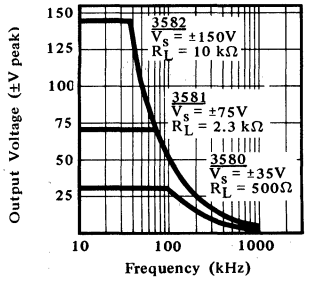
Connector: 0803MC
Heat sink: 0803HS
0804HS
0805HS

* The case is electrically isolated. It is recommended that the case be grounded during use.

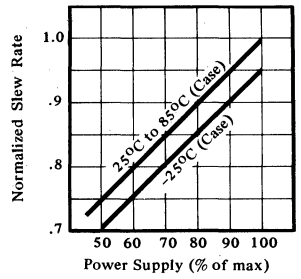
TYPICAL PERFORMANCE CURVES

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

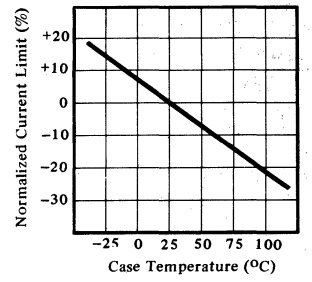
OUTPUT VOLTAGE vs FREQUENCY



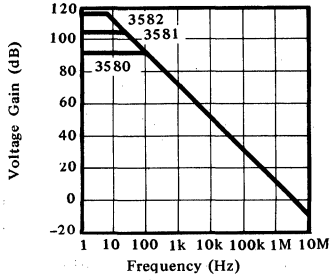
SLEW RATE vs SUPPLY VOLTAGE @ FULL LOAD



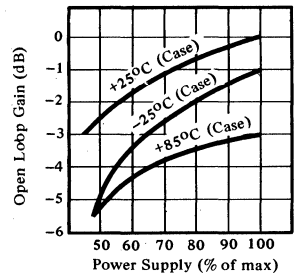
CURRENT LIMIT vs TEMPERATURE



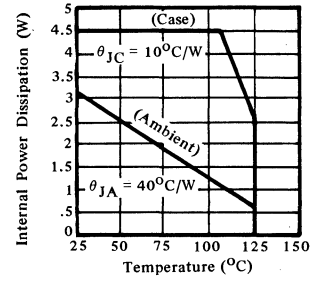
OPEN LOOP FREQUENCY RESPONSE–FULL LOAD



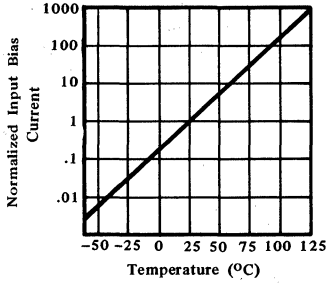
OPEN LOOP GAIN vs SUPPLY VOLTAGE @ MAX LOAD



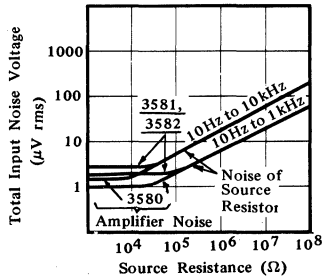
MAXIMUM POWER DISSIPATION



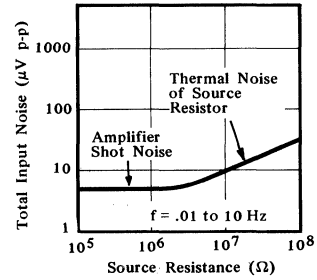
NORMALIZED INPUT BIAS CURRENT vs TEMPERATURE



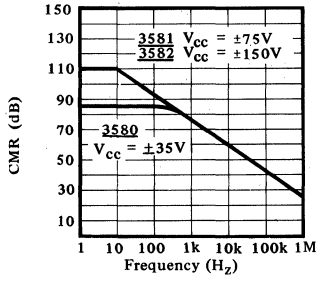
TOTAL INPUT NOISE VOLTAGE vs SOURCE RESISTANCE



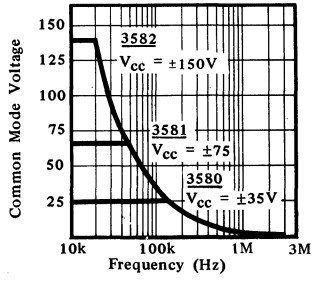
TOTAL LOW FREQUENCY INPUT NOISE vs SOURCE RESISTANCE



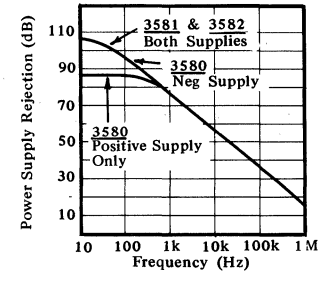
COMMON MODE REJECTION vs FREQUENCY



MAXIMUM COMMON MODE VOLTAGE vs. FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY



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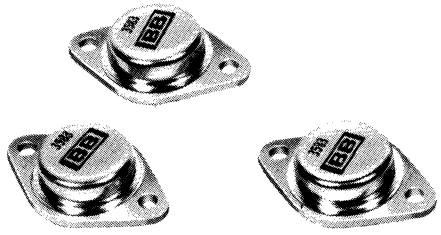

3583

High Voltage - High Current OPERATIONAL AMPLIFIER

FEATURES

- HIGH OUTPUT SWINGS, up to ±140V
- LARGE LOAD CURRENTS, ±75mA
- PROTECTED OUTPUT STAGE, automatic thermal shutoff
- REDUCES SOURCE LOADING, $10^{11}\Omega$ Input Z
- PRESERVES SYSTEM ACCURACY, 110dB CMR 20pA bias current

DESCRIPTION

The 3583 is the first integrated circuit operational amplifier to provide output voltage swings of ±140V with currents as high as ±75mA.

The amplifier operates over a wide supply range (±50VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV E_{OS}, 25μV/°C $\Delta E_{OS}/\Delta T$).

The monolithic FET input stage has low bias current (20pA) which minimizes the offset voltages caused by the bias current and the large resistances normally associated with high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short circuits to ground for supply voltages below ±100VDC. A special thermal sensing circuit prevents damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

Two temperature ranges are available: 0°C to +70°C (3583JM) and -25°C to +85°C (3583AM).

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PDS-343A

DESCRIPTION

The 3583 is a high, voltage high output current integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage applications.

The equivalent circuit for the 3583 is shown in Figure 1. The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage at 25°C and the drift versus temperature are compensated by state-of-the-art laser trimming techniques. They are low enough so that user trimming will not be required in most applications. The high input impedance provides negligible source impedance loading errors when the noninverting circuit configuration is used. The low bias currents minimize offset errors when large values of source and feedback resistors are used.

A true cascode input stage is used together with considerable protection circuitry. There are voltage limiting transistors to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150 and -150V) but typically will withstand a 50% overvoltage without damage.

The unit operates over a wide supply range (±50V to ±150V) with outstanding common-mode rejection (110dB). It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. The output circuit has a unique protection feature which is only practical in integrated circuit amplifiers - self contained automatic thermal sensing and shut off circuitry which automatically turns the amplifier off when the internal temperature reaches approximately 150°C.

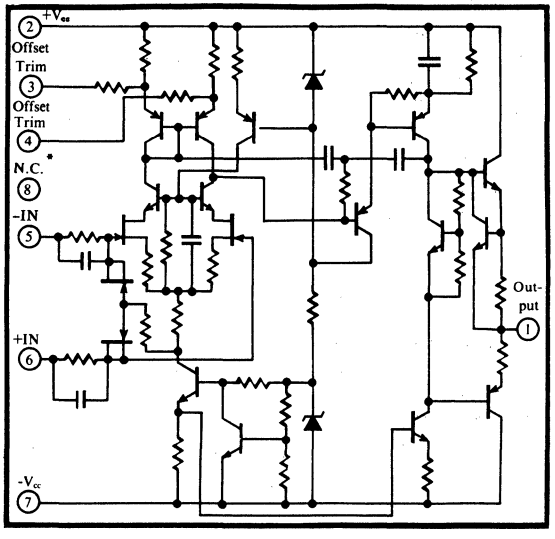


FIGURE 1. 3583 Equivalent Circuit.
(* N.C. = No internal connection.)

This is accomplished by sensing the subtrate temperature and deactivating the amplifiers biasing network when the temperature reaches 150°C. As this happens, the output load current limits at a safe value and the amplifier's quiescent current decreases. The output current will remain at a low value or oscillate between two values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal load condition is removed.

Internal thermal protection removes some of the constraints of power derating for abnormal operating conditions. The amplifier will protect itself for many conditions of excess power dissipation (see POWER DERATING CURVE, page 1-150). This allows the use of a smaller heat sink to protect against abnormal output conditions since the amplifier has its own internal protection for many conditions of excess power dissipation. The output constraints of the SAFE OPERATING AREA CURVES (page 1-150) must still be observed.

The 3583 has several other features that improve its utility. For instance, the metal case of the unit is completely electrically isolated. (This can be contrasted to most power semiconductors where the case is connected to the collector of the device.) This simplifies mounting and reduces cost since the need for insulating spacers and bushings is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better than discrete component amplifiers. The small package size reduces weight and makes mounting more convenient.

SPECIFICATIONS

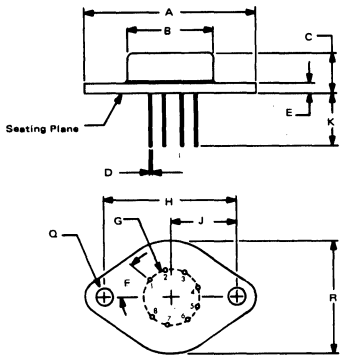
ELECTRICAL

Specifications typical at T_{CASE} = +25°C and $\pm V_{CC}$ = 150VDC unless otherwise noted.

MODELS	3583AM	3583JM
POWER SUPPLY		
Voltage, $\pm V_{CC}$	±50VDC to ±150VDC	
Quiescent Current, max	8.5mA	
RATED OUTPUT		
Voltage, $\pm(\lvert V_{CC}\rvert - 10)$VDC, min	±40VDC to ±140VDC	
Current, min	±75mA	
Current, Short Circuit	±100mA	
Load Capacitance, max	10nF	
OPEN-LOOP GAIN		
No Load, DC	118dB	
Rated Load, DC	94dB, min; 105dB, typ	
FREQUENCY RESPONSE		
Unity Gain Bandwidth, Small Signal	5MHz	
Full Power Bandwidth, R_L = 10kΩ	60kHz	
Slew Rate	30V/µsec	
Settling Time, 0.1%	12µsec	
INPUT OFFSET VOLTAGE T_A = +25°C		
Initial at 25°C, max	±3mV	
Drift vs Temp, max	±23µ/°C	
Drift vs Supply Voltage	±20µV/V	
Drift vs Time	±50µV/mo	
INPUT BIAS CURRENT		
Initial at 25°C, max	-20pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0.2pA/V	
INPUT OFFSET CURRENT		
Initial at 25°C	±20pA	
Drift vs Temp	doubles every 10°C	
Drift vs Supply Voltage	0.2pA/V	
INPUT IMPEDANCE		
Differential	$10^{11}\Omega \parallel 10$pF	
Common-mode	$10^{11}\Omega$	
INPUT NOISE		
Voltage 0.01Hz to 10Hz, p-p	5µV	
10Hz to 1kHz, rms	1.7µV	
Current 0.01Hz to 10Hz, p-p	0.3pA	
INPUT VOLTAGE RANGE		
Max Safe Differential Voltage(1)	$\lvert +V_{CC} + \lvert -V_{CC}\rvert\rvert$	
Max Safe Common-mode Voltage	$+V_{CC}$ to $-V_{CC}$	
Common-mode Voltage, Linear Operation	$\pm(\lvert V_{CC}\rvert - 10)$V	
Common-mode Rejection	110dB	
TEMPERATURE RANGE (Case)		
Specification	-25°C to +85°C	0°C to 70°C
Operating	-55°C to +125°C	
Storage	-55°C to +125°C	

NOTES:
1. The inputs may be damaged by pulses at pins 5 or 6 with dV/dt ≥ 1V/nsec. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage changes.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

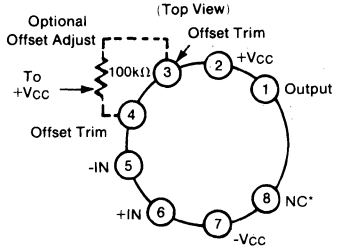
ORDER NUMBER:
3583AM 3583JM

WEIGHT:
15.1 Grams

MATING CONNECTOR:
0803MC

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

CONNECTION DIAGRAM

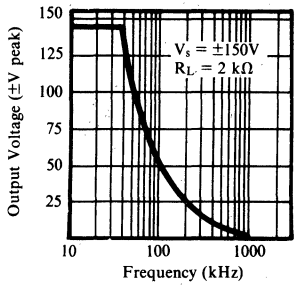


* No internal connection.
The metal case is electrically isolated. It is recommended that the case be grounded during use.

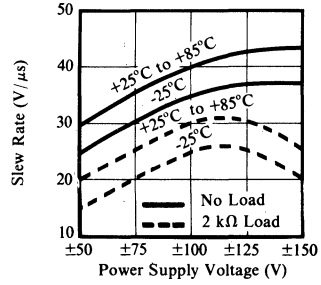
TYPICAL PERFORMANCE CURVES

Typical at 25°C case and $\pm V_{cc}$ max unless otherwise noted.

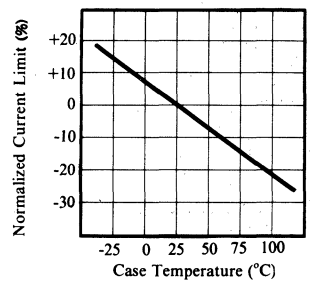
OUTPUT VOLTAGE vs. FREQUENCY



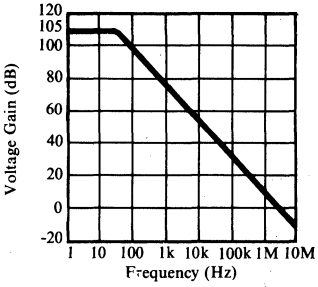
SLEW RATE vs. SUPPLY VOLTAGE



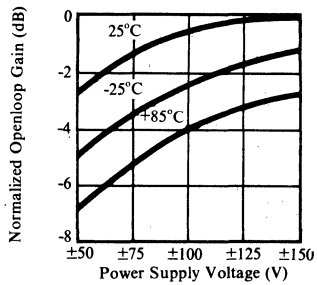
CURRENT LIMIT vs. TEMPERATURE



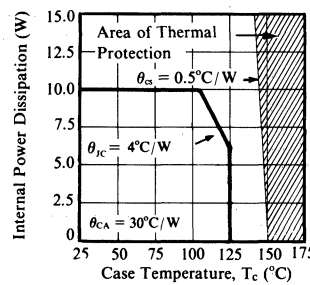
OPEN LOOP FREQUENCY RESPONSE—FULL LOAD



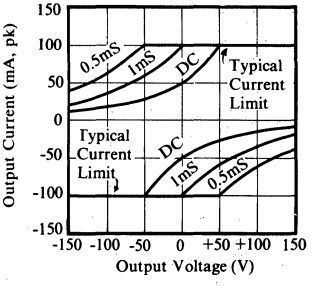
OPEN LOOP GAIN vs. SUPPLY VOLTAGE @ FULL LOAD



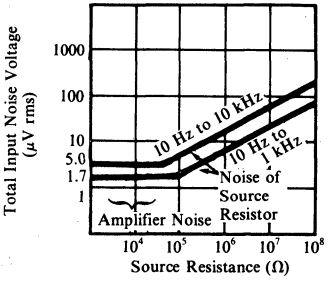
RECOMMENDED POWER DERATING



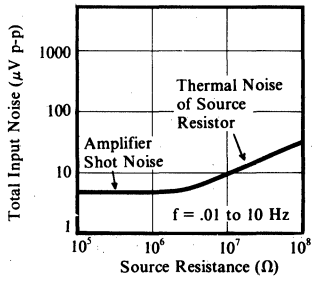
RECOMMENDED SAFE OPERATING AREA (Secondary Breakdown)



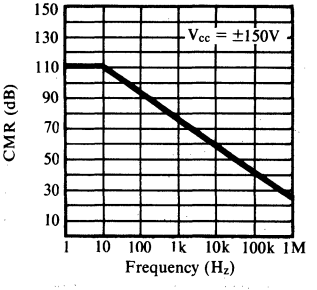
TOTAL INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



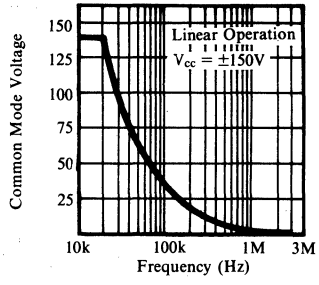
TOTAL LOW FREQUENCY INPUT NOISE vs. SOURCE RESISTANCE



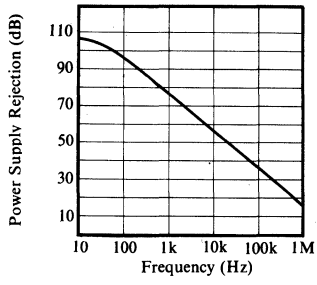
COMMON-MODE REJECTION vs. FREQUENCY



COMMON-MODE VOLTAGE vs. FREQUENCY



POWER SUPPLY REJECTION vs. FREQUENCY



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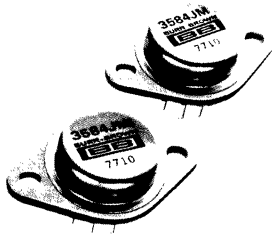


3584

High Voltage OPERATIONAL AMPLIFIER

FEATURES

- TYPICAL GAIN-BANDWIDTH, 50MHz
- OUTPUT, +145V
- PROTECTED OUTPUT, automatic thermal shutoff
- BIAS CURRENT, -20pA
- CMR, 110dB
- SLEW RATE, 150V/usec

APPLICATIONS

- ANALOG SIMULATORS
- DIGITALLY-CONTROLLED POWER SUPPLIES
- CRT DEFLECTION
- ELECTROSTATIC TRANSDUCERS

DESCRIPTION

The 3584 is a high voltage, integrated circuit operational amplifier that will provide up to ±145V output.

The amplifier will provide a gain-bandwidth product of 20MHz minimum, 50MHz typical. The amplifier uses external frequency compensation (one R and one C) so that the user may optimize the bandwidth and slew rate for his particular application.

The amplifier operates over a wide supply range (±70VDC to ±150VDC) and has excellent input characteristics (110dB CMR, 3mV E_{os}, and 25μV/°C E_{os} Drift). The input stage is a FET. The low -20pA bias current minimizes the offset errors caused by the large value resistors normally used in high voltage circuits.

The input stage is protected against overvoltages and the output stage is protected against short circuits to ground. A special thermal sensing circuit helps to prevent damage to the amplifier by automatically shutting the amplifier down when too much power is being dissipated.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-376A

DISCUSSION

The 3584 is a high voltage, integrated circuit operational amplifier. Its ease of use, compact size, and excellent input and output specifications makes it well suited for a wide variety of high voltage and high speed applications.

The design uses a monolithic FET input stage for high input impedance, low bias current, and low voltage drift versus temperature. The offset voltage and the drift are laser trimmed. They are low enough so that user trimming will not be required in most applications.

To achieve the high common-mode voltage capability and rejection a true cascode input stage is used together with considerable protection circuitry. There are voltage limiting diodes to prevent damage due to reverse bias breakdown of the input pair and current limiting resistors to limit the steady state input current to 1mA with the inputs at ±150 volts. The units are conservatively rated (and 100% tested) at full rated differential voltage (+150 and -150V) but typically will withstand a 50% overvoltage without damage.

It also has another feature which is important in many high voltage applications. The input bias current is virtually independent of applied common-mode voltage. This is a benefit of the true cascode input stage which keeps the drain to source voltage of the input transistors constant as the common-mode voltage changes.

The amplifier contains automatic thermal sensing and shut-off circuitry which automatically turns the amplifier off when the internal (substrate) temperature reaches approximately 150°C. This is accomplished by sensing the substrate temperature and deactivating all current sources when the temperature reaches a critical level. As this happens, the output current gradually decreases to zero. The output current may remain at a low value or oscillate between 2 values depending on the amount of power being dissipated and the heat sink conditions seen by the amplifier. In either case, the amplifier will not sustain internal damage and will return to normal operation within a few seconds after the abnormal condition is removed.

The incorporation of thermal sensing and shut-off in the amplifier will require a smaller heat sink than normal. This is due to the fact that the amplifier will protect itself and does not require a massive heat sink for protection under abnormally high power dissipation.

The 3584 has several other features that improve its utility. The metal case of the unit is completely electrically isolated. This simplifies mounting and reduces cost since the need for insulating spacers is eliminated. The hermetically sealed package improves reliability and will withstand severe environments better. And the small package size reduces weight and makes mounting more convenient.

OPERATION FROM A SINGLE SUPPLY

It may be desirable in some applications to operate the amplifiers from a single supply. The circuit in Figure 1 illustrates a typical application. Note that there are restrictions on the input and output voltages (e_i and e_o) which are necessary in order to keep the amplifier circuits operating in a linear manner.

It should be noted that when the amplifier is operated from a single supply, the output stage, which is still short circuit current limited and thermally protected, is not protected for short circuits to ground under all operating conditions. Consult the safe operating area curve.

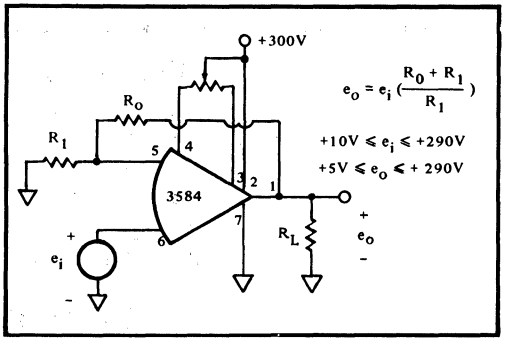


FIGURE 1. Operation from a single supply.

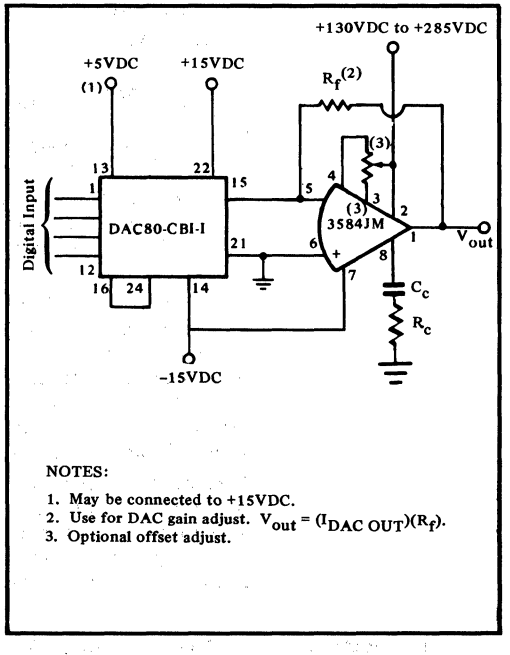


FIGURE 2. High Speed, High Voltage DAC.

SPECIFICATIONS

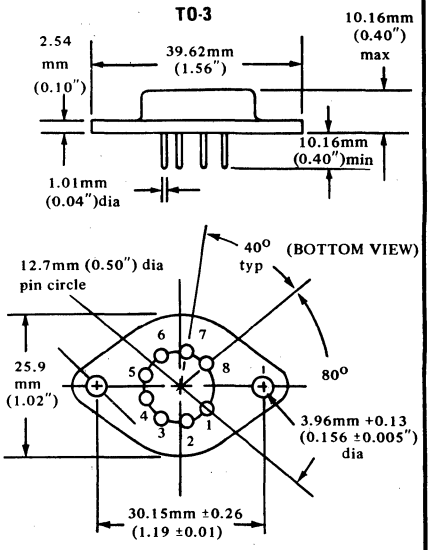
ELECTRICAL

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

MODELS	3584JM
POWER SUPPLY	
Voltage, $\pm V_{cc}$	±70 to ±150 VDC
Quiescent Current, max	±6.5mA
RATED OUTPUT	
Voltage, ± (| V_{cc} | -5)VDC, min	±65 to ±145 VDC
Current, min	±15mA
Current, Short Circuit	±25mA
Load Capacitance, max	10 nF
OPEN LOOP GAIN	
No Load, DC	120 dB
Rated Load, DC, min	100dB
FREQUENCY RESPONSE	
Unity Gain Bandwidth, Small Signal	7 MHz
Gain-bandwidth Product, f = 1 kHz, G = 100	20 MHz, min
Full Power Bandwidth, G = 100	135 kHz
Slew Rate, G = 100	150 V/μs
Settling Time, 0.1%, G = 100	12 μs
INPUT OFFSET VOLTAGE	
Initial @ 25°C, max	3 mV
Drift vs Temp, max	25 μV/°C
Drift vs Supply Voltage	20 μV/V
Drift vs Time	50 μV/mo
INPUT BIAS CURRENT	
Initial @ 25°C, max	-20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT OFFSET CURRENT	
Initial @ 25°C	±20 pA
Drift vs Temp	doubles every 10°C
Drift vs Supply Voltage	0.2 pA/V
INPUT IMPEDANCE	
Differential	10^{11} Ω || 10 pF
Common Mode	10^{11} Ω
INPUT NOISE	
Voltage 0.01 Hz to 10 Hz p-p	5 μV
10 Hz to 1 kHz rms	1.7 μV
Current 0.01 Hz to 10 Hz p-p	0.3 pA
INPUT VOLTAGE RANGE	
Max Safe Differential Voltage(1)	(+V_{cc} + | -V_{cc} |)
Max Safe Common Mode Voltage	+V_{cc} to -V_{cc}
Common Mode Voltage, Linear Operation	±(| V_{cc} | -10)V
Common Mode Rejection	110dB
TEMPERATURE RANGE (Case)	
Specification:	0°C to 70°C
Operating	-55°C to +125°C
Storage	-55°C to +150°C

(1) The inputs may be damaged by pulses at pins 5 or 6 with $dV/dt \geq 1$ V/ns. Any possible damage can be eliminated by limiting the input current to 150mA with external resistors in series with those pins. No external protection is needed for slower voltage changes.

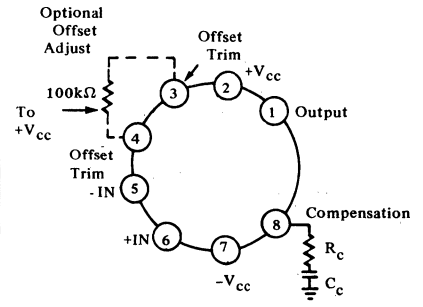
MECHANICAL



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]

CONNECTION DIAGRAM

(TOP VIEW)



Connector: 0803MC
Heatsinks: 0803HS, 0804HS, or 0805HS

Compensation		
Gain	C_C	R_C
1	10 nF	200Ω
10	500 pF	2kΩ
100	50 pF	20kΩ
1000	not required	

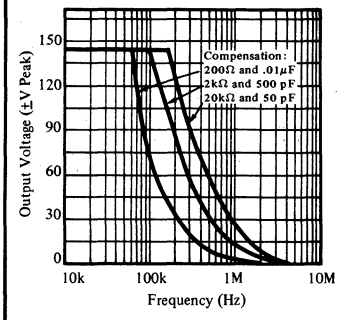
For intermediate values of gain, R and C values may be interpolated.

The case is electrically isolated. It is recommended that the case be grounded during use.

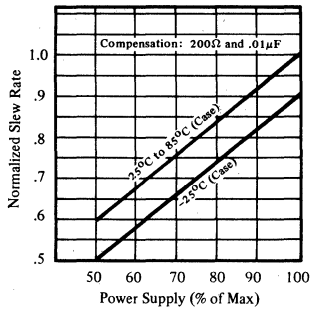
TYPICAL PERFORMANCE CURVES

Typical at 25°C and $\pm V_{cc}$ max unless otherwise noted.

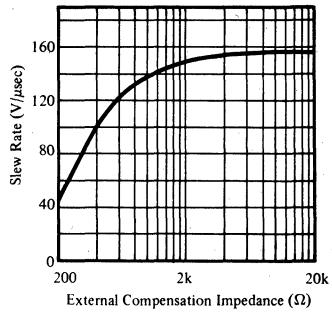
OUTPUT VOLTAGE vs FREQUENCY



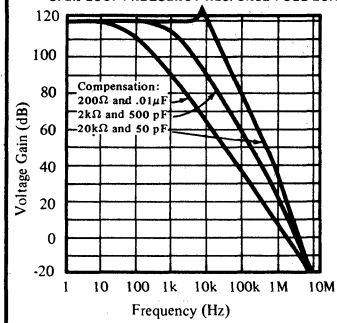
SLEW RATE vs SUPPLY VOLTAGE @ FULL LOAD



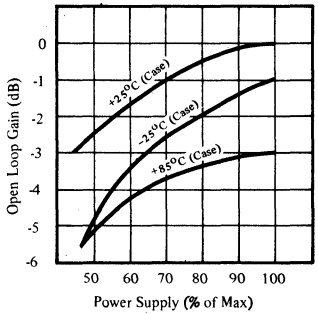
SLEW RATE vs COMPENSATION



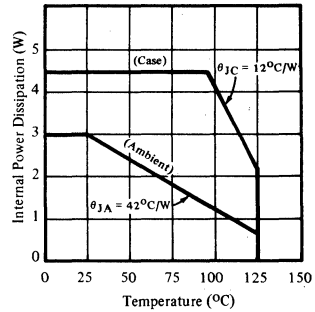
OPEN LOOP FREQUENCY RESPONSE FULL LOAD



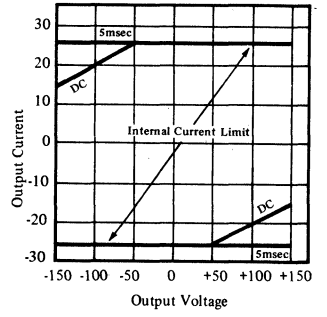
OPEN LOOP GAIN vs SUPPLY VOLTAGE @ MAX LOAD



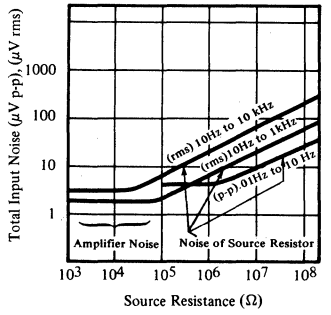
POWER DISSIPATION



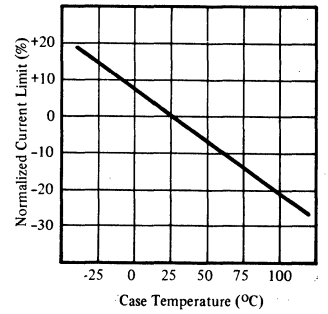
SAFE OPERATING AREA (Secondary Breakdown)



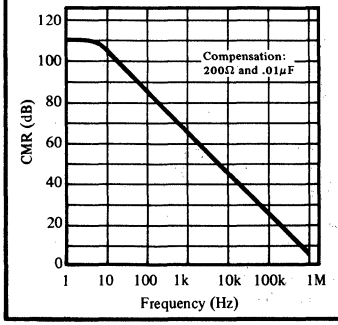
NOISE vs SOURCE RESISTANCE



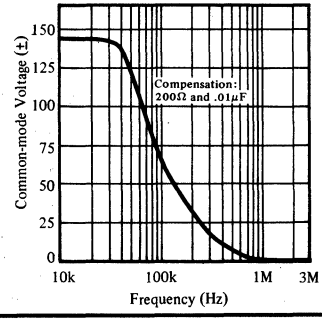
CURRENT LIMIT vs TEMPERATURE



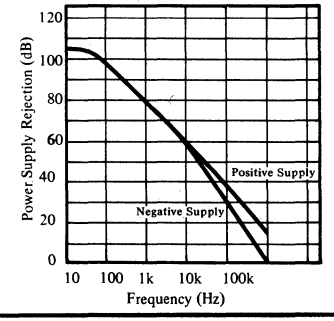
COMMON-MODE REJECTION



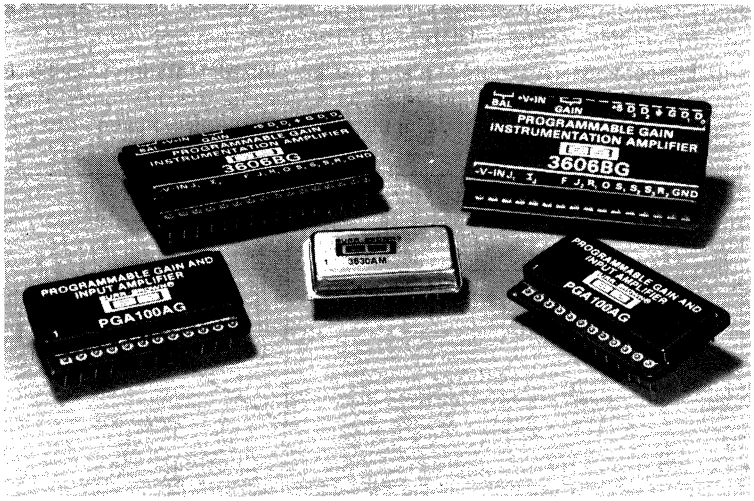
MAXIMUM COMMON-MODE VOLTAGE vs FREQUENCY



POWER SUPPLY REJECTION



INSTRUMENTATION AMPLIFIERS



WHAT IS AN INSTRUMENTATION AMPLIFIER?

An instrumentation amplifier is a closed-loop, differential input gain block. It is a committed circuit with the primary function of accurately amplifying the voltage applied to its inputs.

Ideally, the instrumentation amplifier responds only to the difference between the two input signals and exhibits extremely-high impedances between the two input terminals, and from each terminal to ground. The output voltage is developed single-ended with respect to ground and is equal to the product of amplifier gain and the difference of the two input voltages (see Figure 1).

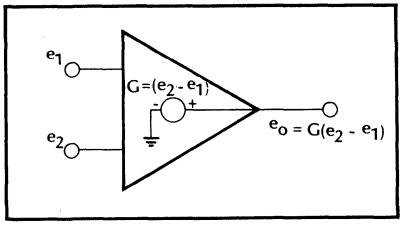


FIGURE 1. Idealized Model of an Instrumentation Amplifier.

The amplifier gain G is normally set by the user with a single external resistor. The properties of this model may be summarized as infinite input impedance, zero output impedance, the output voltage proportional to only the difference voltage ($e_2 - e_1$), a precisely known gain constant (implying no nonlinearity), and unlimited bandwidth. This amplifier would completely reject signal components common to both inputs (common-mode rejection) and would exhibit no DC offset voltage or drift.

CHARACTERISTICS OF INSTRUMENTATION AMPLIFIERS

It is desirable to achieve, as close as possible, the characteristics of the ideal instrumentation amplifier. The following paragraphs are a discussion of the, other-than-ideal, characteristics of the instrumentation amplifiers.

Input Impedance - A simple model of realistic instrumentation amplifier is shown in Figure 2. The impedance Z_{id} represents the differential input impedance. The common-mode input impedance Z_{icm} is represented as two

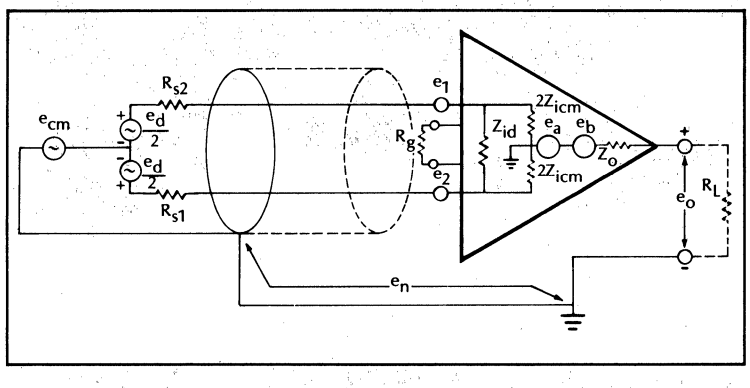


FIGURE 2. Simple Model of an Instrumentation Amplifier Shown in a Typical Application Configuration.

equal components, $2Z_{icm}$, *from each input to ground. These finite resistances contribute an effective gain error due to loading of the source resistance. The instrumentation amplifier provides a load on the source of* $Z_i = Z_{id} \parallel Z_{icm}$. If source impedance is $R_S = R_{s1} + R_{s2}$, the gain error caused by this loading is:

$$\text{Gain Error} = 1 - \frac{Z_i}{Z_i + R_s} = \frac{R_s}{Z_i + R_s} \cong \frac{R_s}{Z_i} \text{ if } Z_i \gg R_s$$

If R_s is 10kΩ and Z_i is 10MΩ,

$$\text{Gain Error} \cong \frac{10 \times 10^3}{10 \times 10^6} = 0.1\%$$

The DC common-mode input impedance Z_{icm} will be independent of gain. The DC differential input impedance Z_{id} may vary as a function of gain. Specifications give the worst-case value. The nonzero output impedance of the amplifier will also create a gain error, the value of which depends on the load resistance.

Nonlinearity - The linearity of gain is possibly of more importance than the gain accuracy, since the value of the gain can be adjusted to compensate for simple gain errors. The nonlinearity is specified to be the peak deviation from a "best fit" straightline, expressed as a percent of peak-to-peak full scale output.

Common-mode Rejection - As illustrated in Figure 2, the output voltage has two components. One component is proportional to the differential input voltage $e_d = (e_2 - e_1)$. The second component is proportional to the common-mode input voltage. The common-mode voltage which appears at the amplifier's input terminals is defined as $E_{cm} = e_2 + e_1/2$. This may consist of some common-mode voltage in the source itself, e_{cm}, (such as bridge excitation) plus any noise voltage, e_n, between the source common and the amplifier common. As shown in Figure 2, the constant G represents the

differential amplifier gain factor (fixed by the external gain-setting resistor). The constant (G/CMRR) represents the commo-mode signal gain of the amplifier. The CMRR (common-mode rejection ratio) is the ratio of differential gain to common-mode gain. Thus CMRR is proportional to the differential gain and CMRR increases as the differential (gain G) increased. Hence, CMRR is usually specified for the maximum and the minimum values of gain of the amplifier. The common-mode rejection may be expressed in dB as - CMRR (dB) = 20 $\log_{10}$ CMRR.

For an ideal instrumentation amplifier the output voltage component due to common-mode voltage should be zero. For a realistic instrumentation amplifier, the CMRR though very high, is still not infinite and so will cause an error voltage of E_{cm}/CMRR x G to appear at the output.

Source Impedance Unbalance - If the source impedances are unbalanced the source voltages ($e_{cm} + e_n$) are divided unequally upon the common-mode impedances and a differential signal is developed at the amplifier's input. This error signal cannot be separated from the desired signal. In the circuit in Figure 2 if $R_{s2} = 0$, $R_{s1} = 1k\Omega$, $e_{cm} + e_n = 10V$, and $Z_{cm} = 100M\Omega$, then the effect of unbalance is to generate a voltage.

$$e_2 - e_1 = 10V - 10V\frac{10^8}{10^8 + 10^3} = 10V\frac{10^3}{10^8 + 10^3} \cong \frac{10V}{10^5} = 0.1mV$$

If e_d full scale is 10mV then this error is:

$$\text{Error} = \frac{0.1mV}{10mV} = 1\% \text{ of full scale.}$$

Offset Voltage and Drift - Most instrumentation amplifiers are two stage devices - they have a variable gain input stage and a fixed gain output stage. If V_i and V_o are the offset voltages of the input and output stages respectively, then the amplifiers total offset voltage referred to the input (RTI) = $V_i + V_o/G$ where G is the amplifier's gain. [Note that E_{os} (RTI) x G.]

The initial offset voltage is usually adjustable to zero and therefore, the voltage drift is the more significant term since it cannot be nulled. The offset voltage drift also has two components - one due to the input stage of the amplifier and the other due to the output stage. When the amplifier is operated at high gain, the drift of the input stage predominates. At low values of gain, the drift of the output stage will be the major component of drift. When the total output drift is referred to the input, the effective input voltage drift is largest for low values of gain. Output voltage drift will always be lowest at low gains. If $\Delta V_i/\Delta T = 2\mu V/°C$ and $\Delta V_o/\Delta T = 500\mu V/°C$ and the amplifier in a gain of 1000V/V is nulled at 25°C, then at 65°C the offset voltage will be:

$$E_{os}\,(RTI)_{65°} = 40°C\,[2\mu V/°C + (500\mu V/°C/1000V/V)]$$
$$= 40°C\,(2.5\mu V/°C) = 100\mu V = 0.1mV$$

If the full scale input is 10mV then the error due to voltage drift is:

$$\text{Error} = 0.1mV/10mV = 1\% \text{ of full scale.}$$

Input Bias and Offset Currents - The input bias currents are the currents that flow out of (or into) either of the two inputs of the amplifier. They are the base currents for bipolar input stages and the JFET leakage currents for FET input stage. Offset currents are the difference of the two bias currents.

The bias currents flowing into the source resistances will generate offset voltages of $E_{os2} = 1_{B2} \times R_{s2}$ and $E_{os1} = 1_{B1} \times R_{s1}$. If $R_{s1} = R_{s2} = R_s/2$ the offset voltage at the input is $E_{os2} - E_{os1} = I_{os} \times R_x/2$. This input referred offset error may be compared directly with the input voltage to compute percent error. (Note that the source must be returned to power supply common or R_s will be infinite and the amplifier will saturate.)

APPLICATIONS OF INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are generally used in applications where extracting and accurately amplifying low level differential signals riding on high common-mode voltages (±10V) is very important. Such applications require high input impedance, high CMRR, low input noise, and excellent DC levels stability (low offset voltage drift).

Instrumentation amplifiers are used as transducer amplifiers for various types of transducers such as strain gage bridges, load cells, thermistor networks, thermocouples, current shunts, biological probes, weather gauges and so forth. Other applications include recorder preamplifiers, multiplexer buffers, servo error amplifiers, current sensors, signal conditioners in process control and data acquisition systems, and in general measurements of small differential signals riding on common-mode voltages.

The small size, low cost, and high performance of these amplifiers offer an attractive approach for data acquisition applications, that is, assigning a fixed-gain amplifier to each transducer and locating the amplifier physically near the transducer. This approach largely eliminates common-mode noise pickup problems since a high level signal (rather than a low level transducer signal) is then retransmitted to the data gathering station. The result is a higher signal/noise ratio at the output. Using one amplifier per point may well be more economical, as well as offering better peformance and flexibility, than the approach of using low level multiplexers.

SELECTION GUIDE
Instrumentation Amplifiers

INSTRUMENTATION AMPLIFIERS													
						Input Parameters					Price ($)		
Description	Model	Range	Gain Accuracy G=100, 25°C max	Gain Drift G = 100 ppm/°C	Non-Linearity G = 100 max	CMR, DC to 60Hz, G = 10 1kΩ, Unbal...min	Voltage vs. Temp. max (μV/°C)	Dynamic Response G = 100 ±3dB BW	Temp. Range[1]	Package	Unit	100's	Page
Very-High Accuracy	INA101AM	1-1000[2]	0.03	22[5]	±0.007%	96dB	±(2 + 20/G)	25kHz	Ind	TO-100	13.20	9.90	2-7
	INA101BM	1-1000[2]	0.03	22[5]	±0.004%	96dB	±(0.75 + 10/G)	25kHz	Ind	TO-100	16.00	12.00	2-7
	INA101CM	1-1000[2]	0.03	22[5]	±0.004%	96dB	±(0.25 + 10/G)	25kHz	Ind	TO-100	18.40	13.80	2-7
	INA101SM	1-1000[2]	0.03	22[5]	±0.004%	96dB	±(0.25 + 10/G)	25kHz	Mil	TO-100	19.50	14.40	2-7
	3630AM	1-1000[2]	0.1	125[5]	±0.007%	96dB	±(2 + 20/G)	25kHz	Ind	DIP	44.00	28.00	2-56
	3630BM	1-1000[2]	0.05	125[5]	±0.003%	96dB	±(0.75 + 10/G)	25kHz	Ind	DIP	62.25	41.15	2-56
	3630CM	1-1000[2]	0.05	125[5]	±0.003%	96dB	±(0.25 + 10/G)	25kHz	Ind	DIP	95.00	64.50	2-56
	3630SM	1-1000[2]	0.05	125	±0.003%	96dB	±(0.75 + 10/G)	25kHz	Ind	DIP	95.00	64.50	2-56
General Purpose	3626AP	5-1000[2]	0.5	35[5]	±0.05%	74dB	±(6 + 10/G)	14kHz	Ind	DIP	30.50	18.90	2-42
	3626BP	5-1000[2]	0.5	35[5]	±0.04%	80dB	±(3 + 5/G)	14kHz	Ind	DIP	32.55	20.50	2-42
	3626CP	5-1000[2]	0.5	35[5]	±0.04%	80dB	±(1 + 5/G)	14kHz	Ind	DIP	39.40	26.50	2-42
	3629AM	5-1000[2]	0.1	45[5]	±0.007%	106dB[3]	±(3 + 10/G)	30kHz	Ind	DIP	29.60	20.90	2-50
	3629AP	5-1000[2]	0.1	45[5]	±0.007%	106dB[3]	±(3 + 10/G)	30kHz	Ind	DIP	26.50	19.40	2-50
	3629BM	5-1000[2]	0.1	45[5]	±0.004%	106dB[3]	±(1.5 + 7.5/G)	30kHz	Ind	DIP	35.90	23.92	2-50
	3629BP	5-1000[2]	0.1	45[5]	±0.004%	106dB[3]	±(1.5 + 7.5/G)	30kHz	Ind	DIP	33.80	20.80	2-50
	3629CM	5-1000[2]	0.1	45[5]	±0.004%	106dB[3]	±(0.75 + 5/G)	30kHz	Ind	DIP	44.15	29.15	2-50
	3629CP	5-1000[2]	0.1	45[5]	±0.004%	106dB[3]	±(0.75 + 5/G)	30kHz	Ind	DIP	39.40	26.50	2-50
	3629SM	5-1000[2]	0.1	45[5]	±0.004%	106dB[3]	±(1.5 + 7.5/G)	30kHz	Ind	DIP	44.15	26.15	2-50
Buffer, Unity-Gain Differential	3627AM	1V/V, fixed	0.01	5	±0.001%[4]	90dB	30	800kHz[4]	Ind	TO-99	12.50	9.15	2-46
	3627BM	1V/V, fixed	0.01	5	±0.001%[4]	100dB	20	800kHz[4]	Ind	TO-99	16.75	11.25	2-46
PROGRAMMABLE GAIN AMPLIFIERS													
Noninverting Multiplexed Input	PGA100AG	Gain set with 4-bit word 1,2,4 8,...128	0.05	10	±0.01	NA	6[6]	5MHz	Ind	DIP	57.00	43.00	2-15
	PGA100BG		0.02	10	±0.005	NA	6[6]	5MHz	Ind	DIP	63.00	47.00	2-15
Differential Input	3606AG	Gain set with 4-bit word 1,2,4, 8,...1024	0.05	10	0.004%	90dB, G = 1	±(3 + 50/G)	40kHz	Ind	DIP	93.40	63.75	2-34
	3606AM		0.05	10	0.004%	90dB, G = 1	±(3 + 50/G)	40kHz	Ind	DIP	110.00	80.30	2-34
	3606BG		0.02	10	0.004%	90dB, G = 1	±(1 + 20/G)	40kHz	Ind	DIP	124.95	86.70	2-34
	3606BM		0.02	10	0.004%	90dB, G = 1	±(1 + 20/G)	40kHz	Ind	DIP	152.00	106.00	2-34

PRECISION TWO-WIRE TRANSMITTER													
	Span			Input Parameters			Output Parameters						
Model	Un-trimmed error max	Non-Linearity max	Temp. Drift ppm%/°C	Offset Voltage max	Offset Voltage vs Temp. max. μV/°C	CMR DC, min	Current Range mA	Offset Current error μA, max	Full Scale Output Current error μA, max	Temp. Range[1]	Package	Price	Page
XTR100AM/AP	-3%	0.01%	±100	±50μV	±1	90dB	4 - 20	±4	±20	Mil/Ind	DIP	[6]	2-23
XTR100BM/BP	-3%	0.01%	±100	±25μV	±0.5	90dB	4 - 20	±4	±20	Mil/Ind	DIP	[6]	2-23

NOTES: 1) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C. 2) Set with external resistor. 3) DC only. 4) Unity-gain. 5) Typical. 6) Advance information subject to change, contact Burr-Brown for price and availability.

GLOSSARY OF TERMS & DEFINITIONS
Instrumentation Amplifiers

COMMON-MODE INPUT IMPEDANCE
The effective impedance (resistance in parallel with capacitance) between either input of an amplifier and its common, or ground, terminal.

COMMON-MODE REJECTION (CMR)
When both inputs of a differential amplifier experience the same common-mode voltage (CMV), the output should, ideally, be unaffected. CMR is the ratio of the common-mode input voltage change to the differential input voltage (error voltage) which produces the same output change.

$$\text{CMR (in dB)} = 20 \log_{10} \text{CMV/Error Voltage}$$

Thus a CMR of 80dB means that 1V of common-mode voltage will cause an error of 100μV (referred to input).

COMMON-MODE REJECTION RATIO (CMRR)
The ratio of the differential voltage gain of an amplifier to its common-mode voltage gain.

COMMON-MODE VOLTAGE (CMV)
That portion of an input signal which is common to both inputs of a differential amplifier. Mathematically it is defined as the average of the signals at the two inputs:

$$\text{CMV} = e_1 + e_2/2$$

FEEDBACK
The return of a portion of the output signal from a device to the input of the device.

FULL POWER FREQUENCY RESPONSE
The maximum sinewave frequency at which a device can supply its peak-to-peak rated output voltage and current, without introducing significant distortion.

GAIN
The ratio of the output signal to the associated input signal of a device.

GAIN ERROR
The difference between the actual gain of an amplifier and the one predicted by the ideal gain expression.

INPUT BIAS CURRENT
The DC input current required at each input of an amplifier to provide zero output voltage when the input signal and input offset voltage are zero. The specified maximum is for each input.

INPUT BIAS CURRENT DRIFT
The rate of change of input bias current with temperature or time.

INPUT GUARDING
The use of an input shield that is sometimes driven to follow the voltage level of the input signal and, thereby, remove leakage and loss-inducing voltage differences between the input signal path and surrounding stray conduction paths.

INPUT OFFSET CURRENT
The difference of the two input bias currents in a differential amplifier.

INPUT OFFSET VOLTAGE
The DC input voltage required to provide zero voltage at the output of an amplifier when the input signal and input bias currents are zero.

INPUT PROTECTION
A means of protecting an input of a device from damage due to the application of excessive input voltage.

INSTRUMENTATION AMPLIFIER
A closed-loop differential input gain block exhibiting high input impedance and high common-mode rejection. Its primary function is to accurately amplify the voltage applied to its inputs.

NONLINEARITY
The peak deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

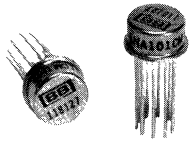
OVERLOAD RECOVERY TIME
The time required for the output of an amplifier to return from saturation to linear operation, following the removal of an input overdrive signal.

SETTLING TIME
The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE
The maximum rate of change of an output voltage when supplying the rated output.

BURR-BROWN®

INA101



Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C
- LOW OFFSET VOLTAGE - 25μV
- LOW NONLINEARITY - 0.002%
- LOW NOISE - 13nV/√Hz at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS
- MEDICAL INSTRUMENTATION

DESCRIPTION

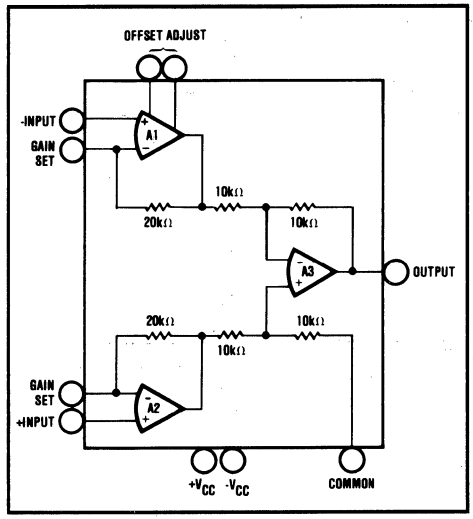
The INA101 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired. All circuits, including the interconnected thin-film resistors, are integrated on a single monolithic substrate.

A multiamplifier design is used to provide the highest performance and maximum versatility with monolithic construction for low cost. The input stage uses Burr-Brown's ultra-low drift, low noise technology to provide exceptional input characteristics.

Gain accuracy is achieved with precision nichrome resistors. This provides high initial accuracy, low TCR (temperature coefficient of resistance) and TCR matching, with outstanding stability as a function of time.

State-of-the-art wafer-level laser-trimming techniques are used for minimizing offset voltage and offset voltage drift versus temperature. This advanced technique also maximizes common-mode rejection and gain accuracy.

The INA101 introduces premium instrumentation amplifier performance and with the lower cost makes it ideal for even higher volume applications.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

MODEL	INA101AM			INA101BM, INA101SM			INA101CM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN										
Range of Gain	1		1000	*		*	*		*	V/V
Gain Equation		G = 1 + (40k/R_G)			*			*		V/V
Error From Equation, DC(1)		±(0.04±0.000016G - 0.02/G)	±(0.1±0.0003G - 0.05/G)		*	*		*	*	% of FS
Gain Temp. Coefficient(2)										
G = 1		2	5		*	*		*	*	ppm/°C
G = 10		20	100		*	*		*	*	ppm/°C
G = 100		22	110		*	*		*	*	ppm/°C
G = 1000		22	110		*	*		*	*	ppm/°C
Nonlinearity, DC		±(0.002 + 10^{-5}G)	±(0.005 + 2 x 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)	% of p-p FS
RATED OUTPUT										
Voltage	±10	±12.5		*	*		*	*		V
Current	±5	±12.5		*	*		*	*		mA
Output Impedance		0.01			*			*		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at +25°C(3)		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	µV
vs. Temperature			±2 ±20/G			±0.75 ±10/G			±0.25 ±10/G	µV/°C
vs. Supply		±(1 + 20/G)			*			*		µV/V
vs. Time		±(1 + 20/G)			*			*		µV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input)		±15	±30		±10	±30		±5	±20	nA
vs. Temperature		±0.2			*			*		nA/°C
vs Supply		±0.1			*			*		nA/V
Initial Offset Current		±15	±30		±10	±30		±5	±20	nA
vs. Temperature		±0.5			*			*		nA/°C
INPUT IMPEDANCE										
Differential		10^{10} ‖ 3			*			*		Ω ‖ pF
Common-mode		10^{10} ‖ 3			*			*		Ω ‖ pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10	±12		*	*		*	*		V
CMR with 1kΩ Source Imbal.										
DC to 60Hz, G = 1	80	90		*	*		*	*		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		dB
INPUT NOISE										
Input Voltage Noise										
f_B = 0.01Hz to 10Hz		0.8			*			*		µV, p-p
Density, G = 1000										
f_o = 10Hz		18			*			*		nV/√Hz
f_o = 100Hz		15			*			*		nV/√Hz
f_o = 1kHz		13			*			*		nV/√Hz
Input Current Noise										
f_B = 0.01Hz to 10Hz		50			*			*		pA, p-p
Density										
f_o = 10Hz		0.8			*			*		pA/√Hz
f_o = 100Hz		0.46			*			*		pA/√Hz
f_o = 1kHz		0.35			*			*		pA/√Hz
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness										
G = 1		300			*			*		kHz
G = 10		140			*			*		kHz
G = 100		25			*			*		kHz
G = 1000		2.5			*			*		kHz
Small Signal, ±1% Flatness										
G = 1		20			*			*		kHz
G = 10		10			*			*		kHz
G = 100		1			*			*		kHz
G = 1000		200			*			*		Hz
Full Power, G = 1 - 100		6.4			*			*		kHz
Slew Rate, G = 1 - 100	0.2	0.4		*	*		*	*		V/µsec
Settling Time (0.1%)										
G = 1		30	40		*	*		*	*	µsec
G = 100		40	55		*	*		*	*	µsec
G = 1000		35	470		*	*		*	*	µsec
Settling Time (0.01%)										
G = 1		30	45		*	*		*	*	µsec
G = 100		50	70		*	*		*	*	µsec
G = 1000		500	650		*	*		*	*	µsec

ELECTRICAL (CONT)

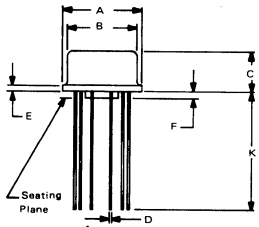
MODEL	INA101AM			INA101BM, INA101SM			INA101CM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY										
Rated Voltage		±15			*			*		V
Voltage Range	±5		±20	*		*	*		*	V
Current, Quiescent		±6.7	±8.5		*	*		*	*	mA
TEMPERATURE RANGE										
Specification[4]	-25		+85	*		*	*		*	°C
Operation	-55		+125	*		*	*		*	°C
Storage	-65		+150	*		*	*		*	°C

*Specifications same as for INA101AM.

NOTES:
1. Typically the tolerance of R_G will be the major source of gain error. 2. Not including the TCR of R_G.
3. Adjustable to zero at any one gain. 4. -55°C to +125°C for INA101SM.

MECHANICAL

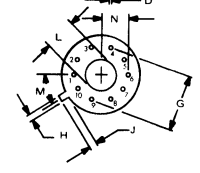
TO-100



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

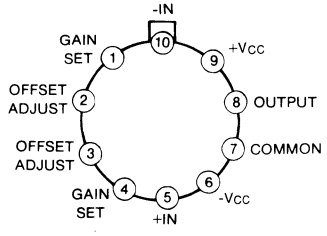
Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05



BOTTOM VIEW

CONNECTION DIAGRAM



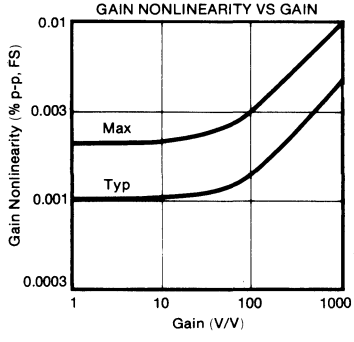
TOP VIEW

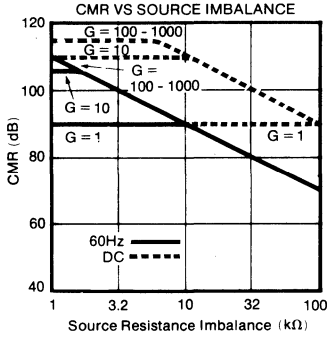
ABSOLUTE MAXIMUM RATINGS

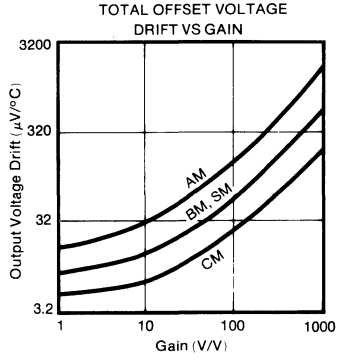
Supply	±20V
Internal Power Dissipation	600mW
Input Voltage Range	±V_{CC}
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground

TYPICAL PERFORMANCE CURVES

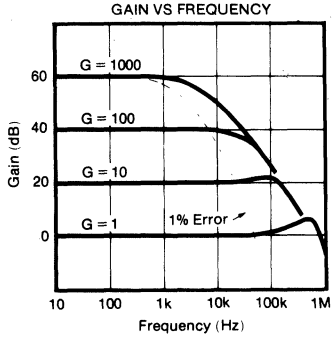
At +25°C and in circuit of Figure 2 unless otherwise noted.

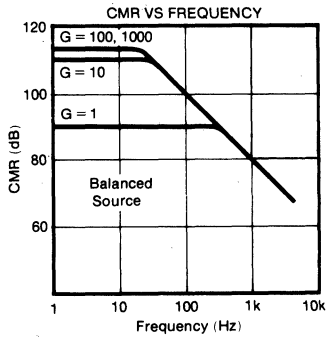


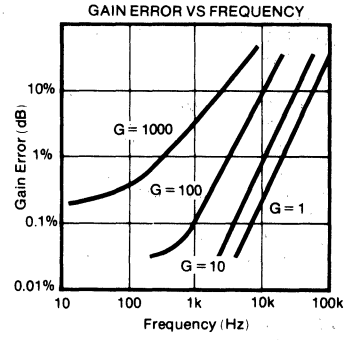


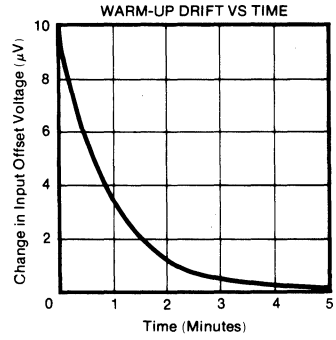


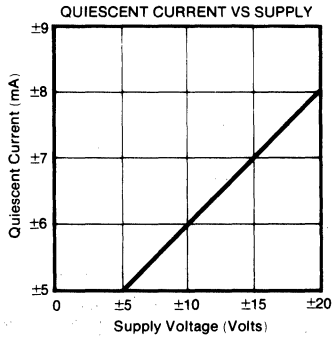
TYPICAL PERFORMANCE CURVES (CONT)

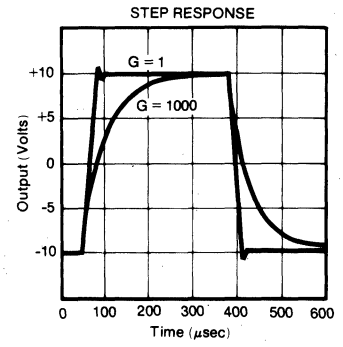


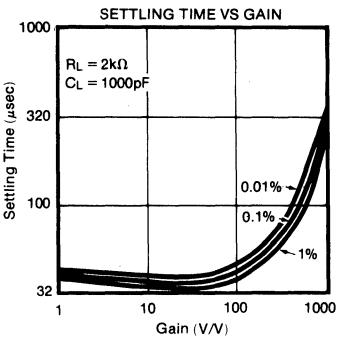


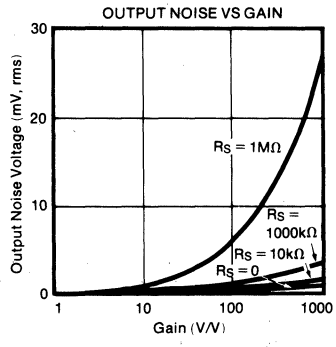


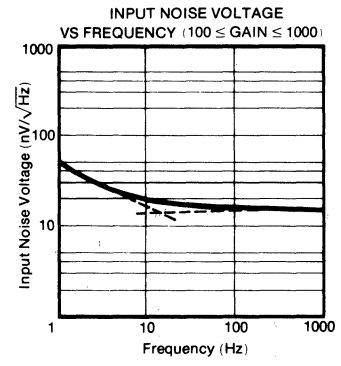












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are differential input closed-loop gain blocks whose committed circuit accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is very difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances. Figure 1 shows a simplified model of an instrumentation amplifier that eliminates most of the problems.

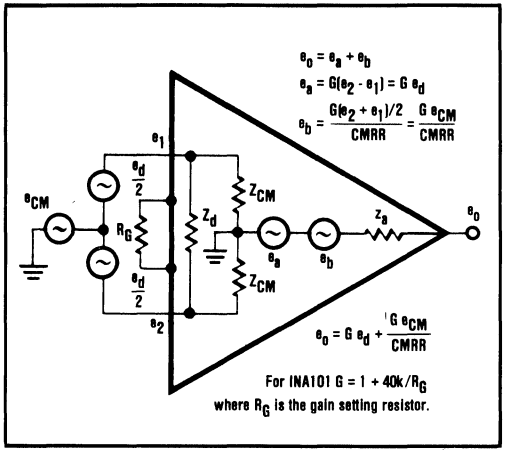


FIGURE 1. Model of an Instrumentation Amplifier.

THE INA101

A simplified schematic of the INA101 is shown on the first page of this data sheet. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found on integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA101 is operated over wide temperature ranges.

USING THE INA101

Figure 2 shows the simplest configuration of the INA101. The gain is set by the external resistor, R_G with a gain equation of $G = 1 + (40K/R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally between pins 1 and 4. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect.

The optional offset null capability is shown in Figure 2. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately $0.31\mu V/^{\circ}C$ per $100\mu V$ of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset. Output offsetting can be accomplished in Figure 3 by applying a voltage to the Common (pin 7) through a buffer amplifier. This limits the resistance in series with pin 7 to minimize CMR error. Resistance above 0.1Ω will cause the common-mode rejection to fall below 106dB. Be certain to keep this resistance low.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA101 is shown in Figure 2. The output voltage is a function of the differential input voltage times the gain.

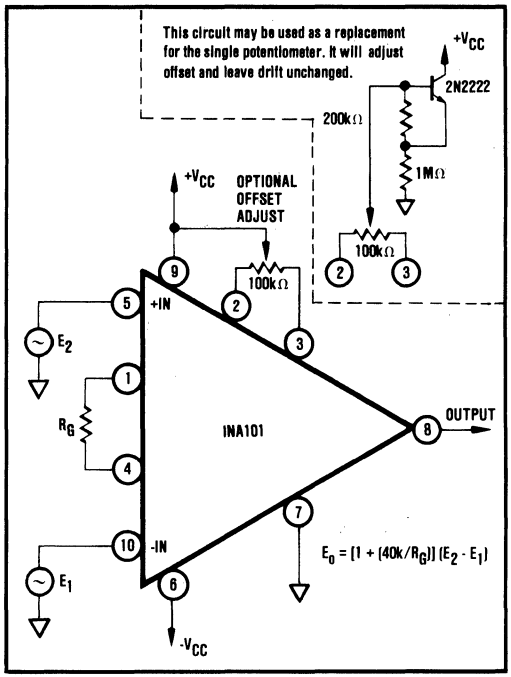


FIGURE 2. Basic Circuit Connection for the INA101 Including Optional Input Offset Null Potentiometer.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component of offset (Figure 2) and occasionally that of the output (Figure 3). The quality of the potentiometer will affect the

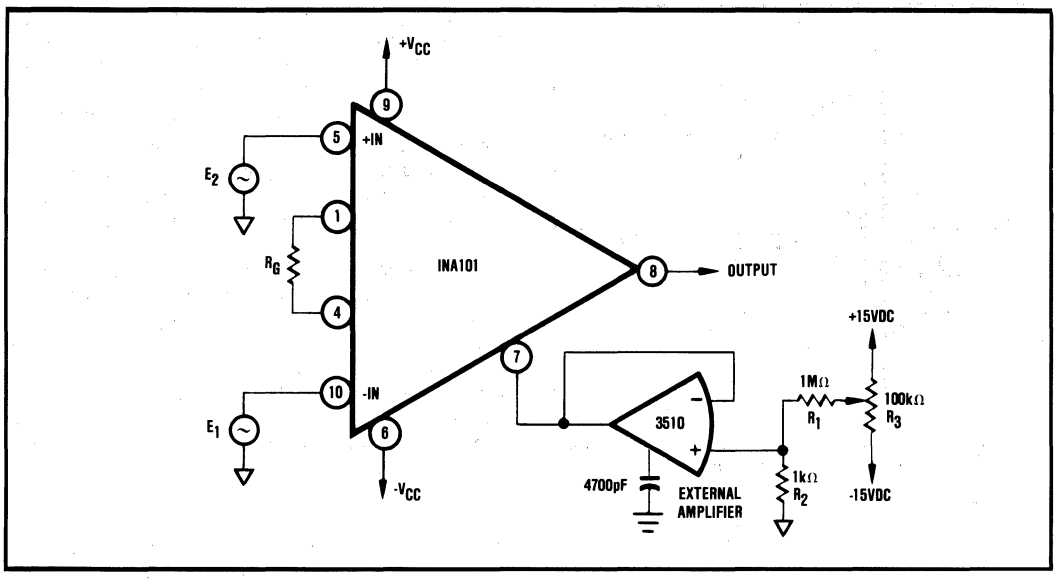


FIGURE 3. Optional Output Offset Nulling or Offsetting Using External Amplifier (Low Impedance to Pin 7).

results, therefore, choose one with good temperature and mechanical-resistance stability. The procedure is as follows:

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return path exists to the input).
2. Set the gain to the desired value by choosing R_G.
3. Adjust to 100kΩ potentiometer in Figure 2 until the output reads 0V ±1mV or desired setting. Note that the offset will change when the gain is changed. If the output component of offset is to be removed or if it is desired to establish an intentional offset, adjust the 100kΩ potentiometer in Figure 3 until the output reads 0V ±1mV or desired setting. Note that the offset will not change with gain, but be sure to use a stable external amplifier with good DC characteristics. The range of adjustment is ±15mV as shown. For larger ranges change the ratio of R_1 to R_2.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low level differential signals from bridges and transducers such as strain gages, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise, see Figure 1), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA101 accomplishes all of these with high precision.

Figures 4 through 9 show some typical applications circuits.

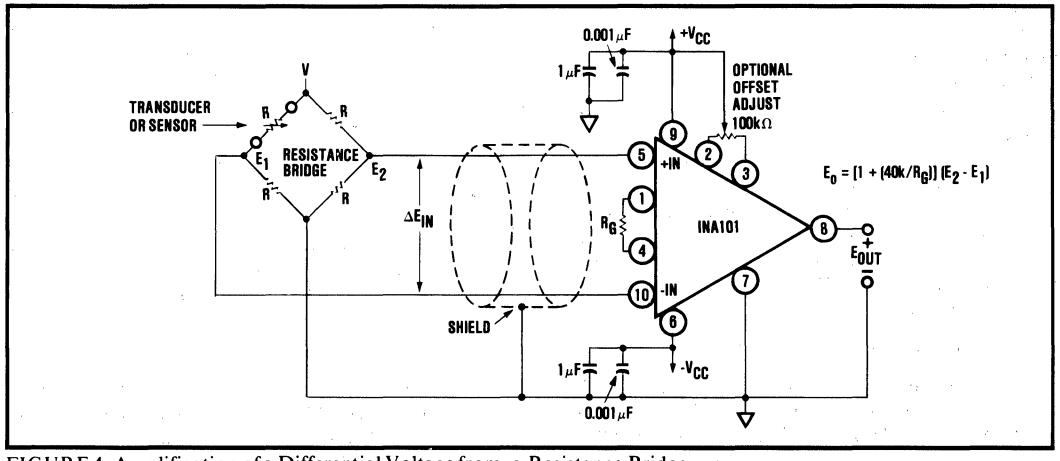


FIGURE 4. Amplification of a Differential Voltage from a Resistance Bridge.

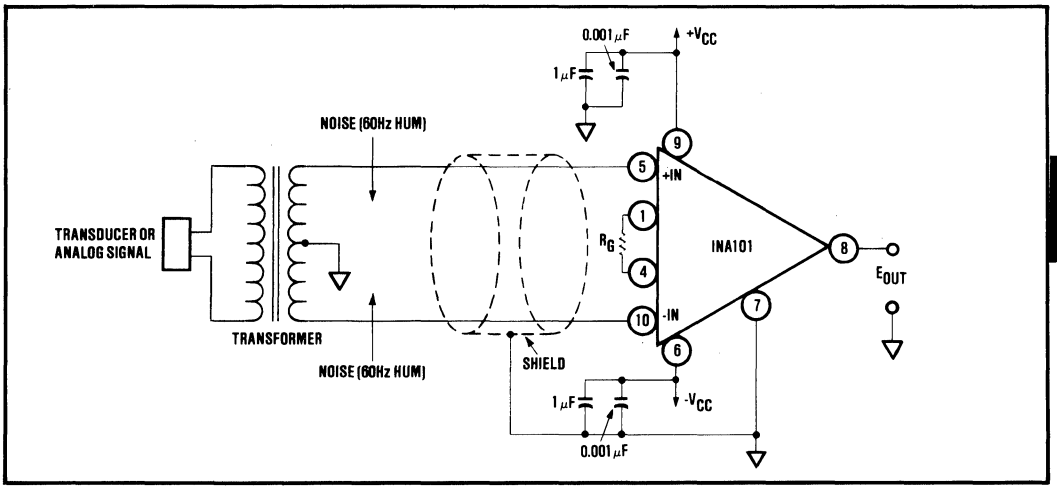


FIGURE 5. Amplification of a Transformer Coupled Analog Signal.

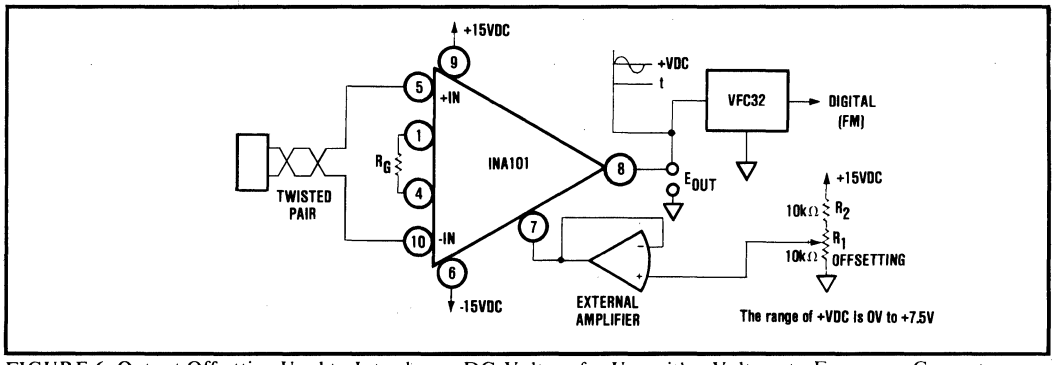


FIGURE 6. Output Offsetting Used to Introduce a DC Voltage for Use with a Voltage-to-Frequency Converter.

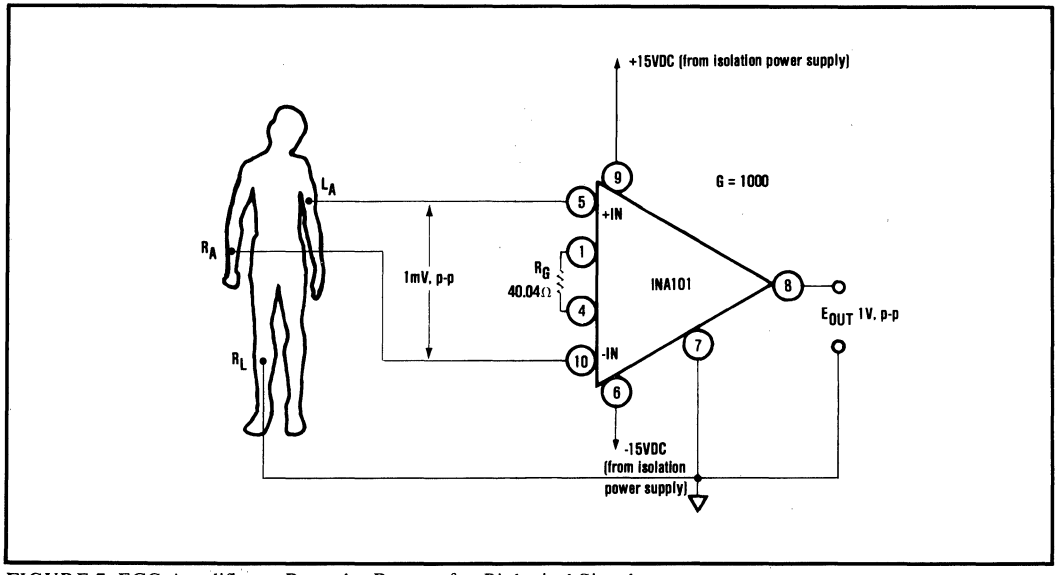


FIGURE 7. ECG Amplifier or Recorder Preamp for Biological Signals.

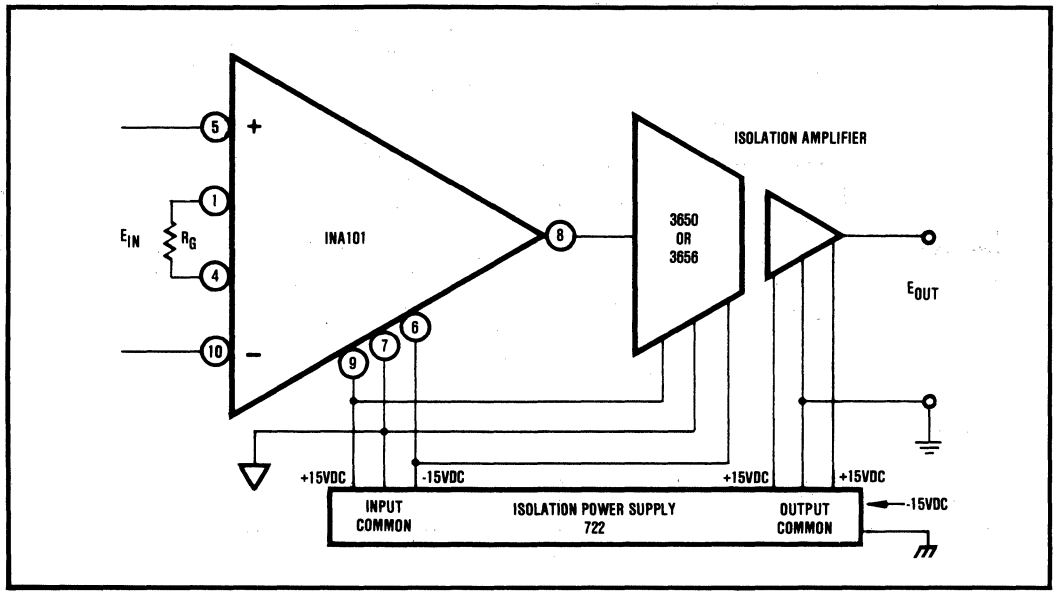


FIGURE 8. Precision Isolated Instrumentation Amplifier.

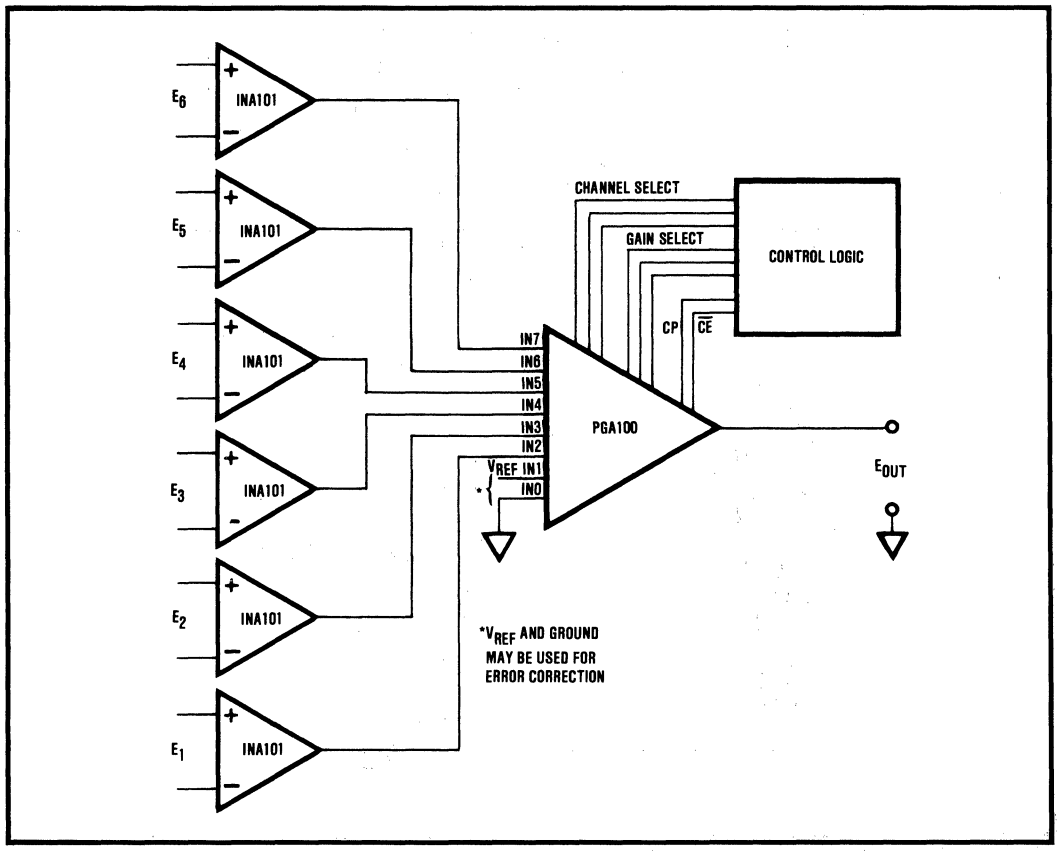


FIGURE 9. Multiple Channel Precision Instrumentation Amplifier.

BURR-BROWN®

PGA100

Digitally-Controlled Programmable Gain/Multiplexed Input OPERATIONAL AMPLIFIER

FEATURES

- HIGH GAIN ACCURACY, ±0.02%, max (B grade)
- LOW NONLINEARITY, ±0.005%, max (B grade)
- FAST SETTLING, 5μsec to 0.01%
- LOW CHANNEL-TO-CHANNEL CROSSTALK, ±0.003%
- INPUT PROTECTION, ±20V, max above $\pm V_{CC}$
- 8 ANALOG INPUT CHANNELS WITH HIGH Z_{IN}, $10^{11}\Omega$
- 8 BINARY GAINS 1, 2, 4, 8, 16, 32, 64, 128 (V/V)
- FULLY MICROPROCESSOR-COMPATIBLE

APPLICATIONS

- DATA ACQUISITION SYSTEM AMPLIFIER
- SOFTWARE ERROR CORRECTION
- AUTO-ZEROING CAPABILITY
- DIGITALLY-CONTROLLED AUTORANGING SYSTEM
- TEST EQUIPMENT
- REMOTE INSTRUMENTATION SYSTEM
- SYSTEM DYNAMIC RANGE AND RESOLUTION IMPROVEMENT

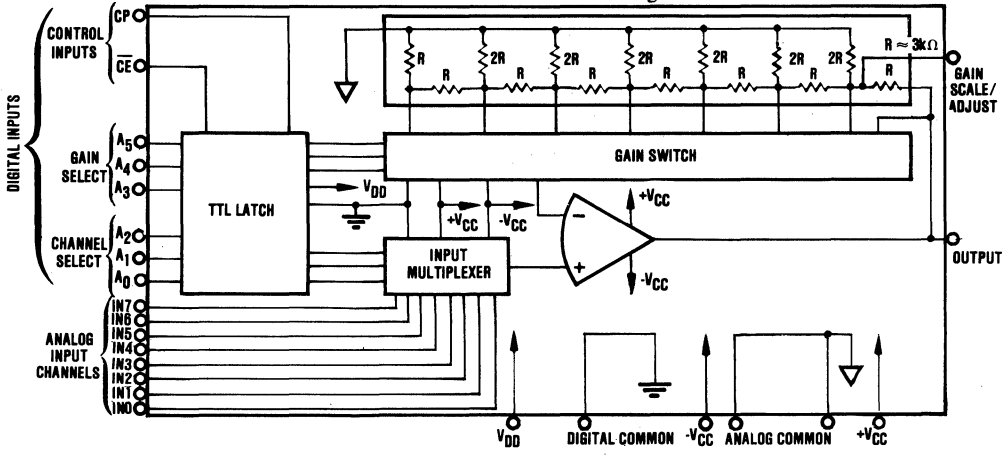
DESCRIPTION

The PGA100 is a precision, digitally-programmable-gain multiplexed-input amplifier. The user can select any one of eight analog input channels simultaneously with any one of eight noninverting binarily weighted gain steps from 1 to 128 (V/V). The digital gain and channel select are latchable for microprocessor interface. Also, the fast 5μsec settling time is ideal for rapid channel scanning in data acquisition systems.

Precision laser-trimming of both offset voltage and gain accuracy, with good temperature tracking of feedback resistor ratios, permits direct use without adjustments. However, hardware or software correction of errors is readily achievable.

In addition, gain scaling to gains other than 1 to 128V/V can easily be accomplished.

Microcircuit construction and the use of laser-trimmed thin-film feedback resistors achieve high accuracy, small size, and low cost not obtained with discrete designs.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-457

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC unless otherwise noted.

PARAMETER	CONDITIONS	PGA100AG			PGA100BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
GAIN, G								
Inaccuracy(1)	G = 1 to 128, I_O = 1mA		±0.01	±0.05		±0.005	±0.02	%
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±5	±10		*	*	ppm/°C
vs Time			±0.001			*		%/1000 hrs.
Nonlinearity(3)	G = 1 to 128, I_O = 1mA		±0.004	±0.01		±0.002	±0.005	% of FS
vs Temperature(2)	-25°C ≤ T_A ≤ +85°C		±2	±5		*	*	ppm/°C
vs Time			±0.001			*		%/1000 hrs.
Warm-up Time		1			*			min
RATED OUTPUT								
Voltage	I_O = ±2mA	±10			*			V
Current	V_O = ±10V	±2			*			mA
Output Resistance	G ≤ 128		0.05			*		Ω
Short Circuit Current			±15			*		mA
Capacitive Load Range	Phase Margin ≥ 25°		1000			*		pF
INPUT OFFSET VOLTAGE								
Initial	T_A = +25°C		±0.1	±1		±0.05	±0.5	mV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±6			*		µV/°C
vs Supply Voltage	±8VDC ≤ | V_{CC} | ≤ ±18VDC		±10	±80		*	*	µV/V
vs Time			±15			*		µV/mo.
INPUT BIAS CURRENT								
Initial	T_A = +25°C							
"OFF" Channel			±10			*		pA
"ON" Channel			±0.1			*	±1	nA
vs Temperature			Note 4			*		
INPUT DIFFERENCE CURRENT, BETWEEN CHANNELS								
Initial	T_A = +25°C							
"OFF" Channel			±20			*		pA
"ON" Channel			±0.2			*	±2	nA
vs Temperature			Note 4			*		
ANALOG INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±(|V_{CC}|+20)			*	V
Input Voltage Range	Linear operation	±10			*			V
Input Impedance								
"OFF" Channel			10^{12} || 5			*		Ω || pF
"ON" Channel			10^{11} || 25			*		Ω || pF
INPUT NOISE								
Voltage Noise Density	f_O = 1Hz		200			*		nV/√Hz
	f_O = 10Hz		60			*		nV/√Hz
	f_O = 100Hz		25			*		nV/√Hz
	f_O = 1kHz		18			*		nV/√Hz
	f_O = 10kHz		18			*		nV/√Hz
	f_O = 100kHz		18			*		nV/√Hz
Voltage Noise	f_B = 0.1Hz to 10Hz		2.6			*		µV, p-p
Current Noise Density	f_O = 0.1Hz thru 8kHz		6			*		fA/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		115			*		fA, p-p
DYNAMIC RESPONSE								
Gain Bandwidth Product			5			*		MHz
Full Power Bandwidth	G = 1, V_O = 20V, p-p, R_L = 5kΩ		220		80	*		kHz
Slew Rate	G = 1, V_O = ±10V, R_L = 5kΩ		14		5	*		V/µsec
Settling Time(5)	G = 1, V_O = ±10V, R_L = 5kΩ							
ε = 1%			2.5			*		µsec
ε = 0.1%			3			*		µsec
ε = 0.01%			5			*		µsec
Rise Time	10% to 90%, small signal		70			*		nsec
Phase Margin	G = 1, R_L = 5kΩ		60			*		Degrees
Overload Recovery (6)	G = 1, 50% overdrive		2			*		µsec
Crosstalk, RTI(5)(7)	20V, p-p, 1kHz sine, R_S = 1kΩ on all OFF channels		±0.003			*		%
DIGITAL INPUT(8)								
Input "Low" Threshold, V_{IL}				0.8			*	V
Input "High" Threshold, V_{IH}		2.0			*			V
f_{max}, Maximum Clock Frequency		30			*			MHz
t_{WL}, Clock Pulse Width (Low)	Figure 1	20			*			nsec
t_{s_1}, Setup Time (Data to CP)	Figure 1	20			*			nsec
t_{h_1}, Hold Time (Data to CP)	Figure 1	5			*			nsec
t_{s_2}, Setup Time ($\overline{CE}$ to CP)	Figure 1	25			*			nsec
t_{h_2}, Hold Time ($\overline{CE}$ to CP)	Figure 1	5			*			nsec

ELECTRICAL (CONT)

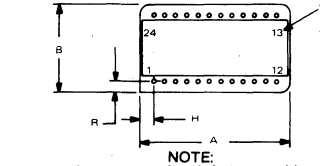
PARAMETER	CONDITIONS	PGA100AG			PGA100BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SUPPLY								
Rated Voltage			±15			"		VDC
Voltage Range	Derated performance	±8		±18	"		"	V
Positive Quiescent Current			+20	+27		+15	+20	mA
Negative Quiescent Current			-10	-16		-7.5	-12	mA
DIGITAL SUPPLY								
Rated Voltage			+5			"		VDC
Voltage Range		+4.75		+5.25	"		"	V
Quiescent Current	V_{DD} = +5.25V		15	27		"	"	mA
TEMPERATURE RANGE								
Specification		-25		+85	"		"	°C
Operating	Derated performance	-55		+125	"		"	°C
Storage		-55		+125	"		"	°C

*Specifications same as PGA100AG.

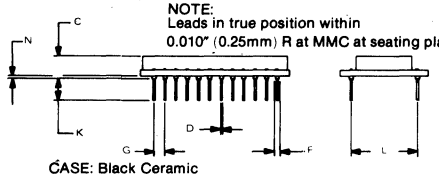
NOTES:
1. Inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero.
2. Parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
3. Nonlinearity is the maximum peak deviation from a "best straight line" (curve fitting on input-output graph) expressed as a percent of the full scale peak-to-peak output. Gain constant, V_{OUT} ranges from -10V to +10V.
4. Doubles approximately every 10°C.
5. See Typical Performance Curves.
6. Time required for the output to return from saturation to linear operation following the removal of an input overdrive signal.
7. Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is expressed as a percent of the signal applied to all OFF channels.
8. All digital inputs are one 74LSTTL load.

MECHANICAL

Pin numbers shown for reference only.
Numbers may not be marked on package.



NOTE:
Leads in true position within
0.010" (0.25mm) R at MMC at seating plane.



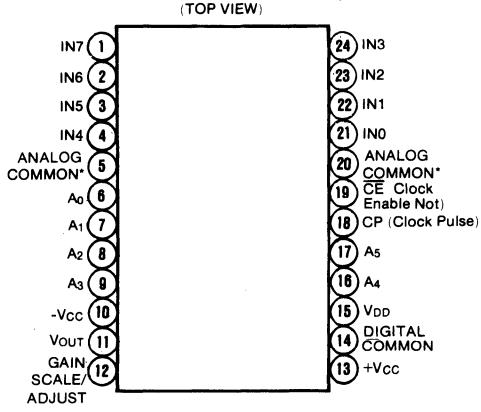
CASE: Black Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 6.3 grams (0.225 oz.)
HERMETICITY: Conform to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

ABSOLUTE MAXIMUM RATINGS

Analog Supply	±18V
Digital Supply	+7V
Input Voltage Range, Analog	±(|Vcc| +20)V
Input Voltage Range, Digital	+7V
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

PIN DESIGNATIONS

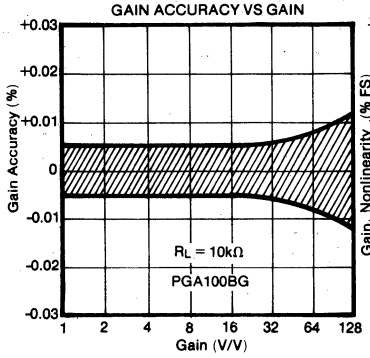


*Connected internally. Use pin 20 as the primary analog common.

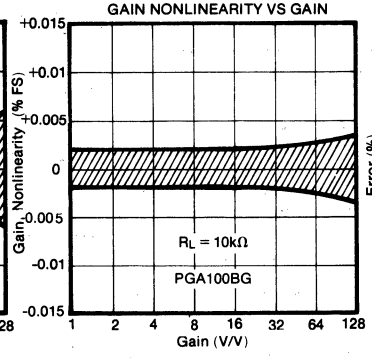
TYPICAL PERFORMANCE CURVES

(T_A = +25°C. ±V_{CC} = 15VDC, V_{DD} = +5VDC, unless otherwise noted.)

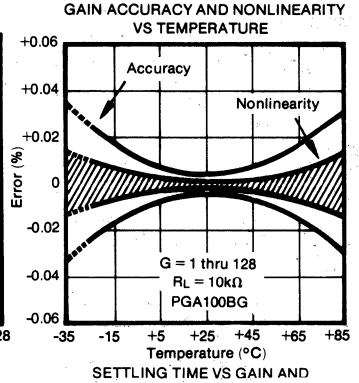
GAIN ACCURACY VS GAIN



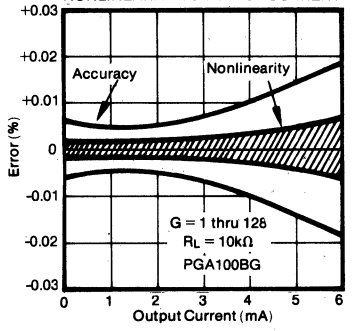
GAIN NONLINEARITY VS GAIN



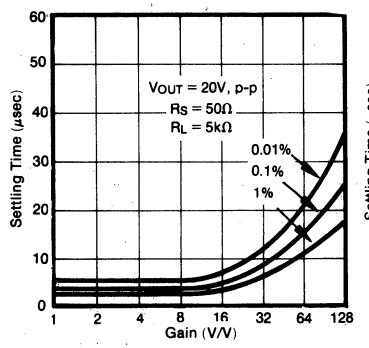
GAIN ACCURACY AND NONLINEARITY VS TEMPERATURE



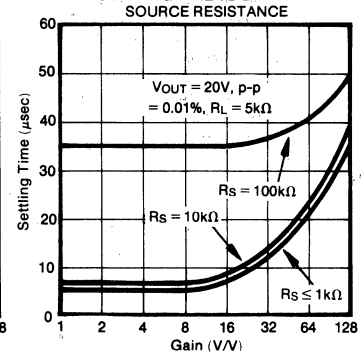
GAIN ACCURACY AND NONLINEARITY VS OUTPUT CURRENT



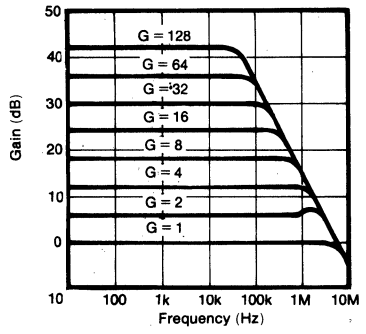
SETTLING TIME VS GAIN



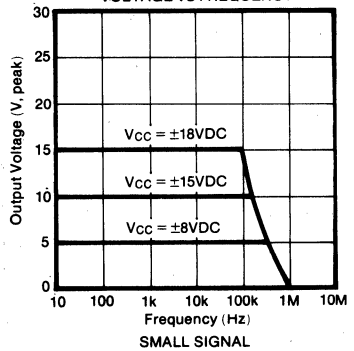
SETTLING TIME VS GAIN AND SOURCE RESISTANCE



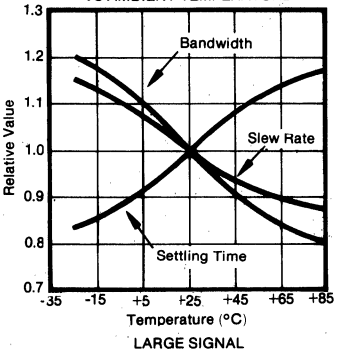
SMALL SIGNAL FREQUENCY RESPONSE



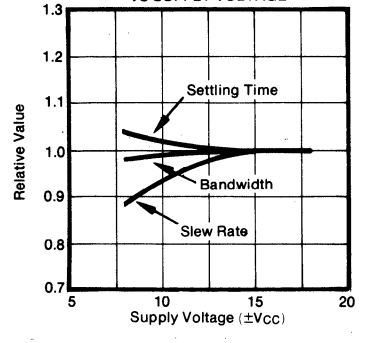
LARGE SIGNAL OUTPUT VOLTAGE VS FREQUENCY



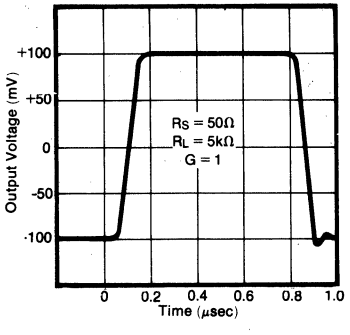
FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE



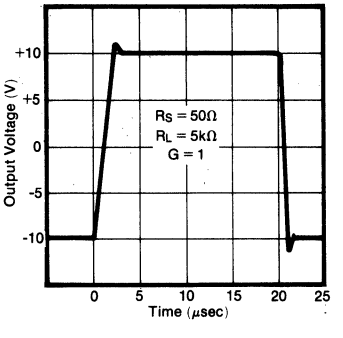
FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE



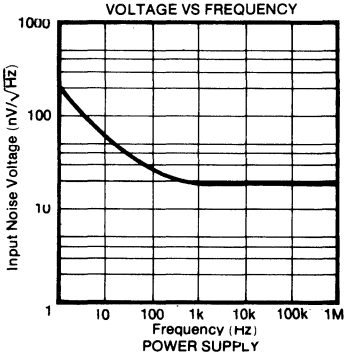
SMALL SIGNAL TRANSIENT RESPONSE



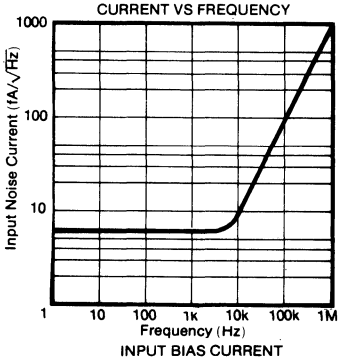
LARGE SIGNAL TRANSIENT RESPONSE



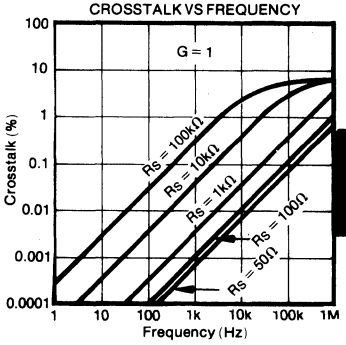
INPUT NOISE VOLTAGE VS FREQUENCY



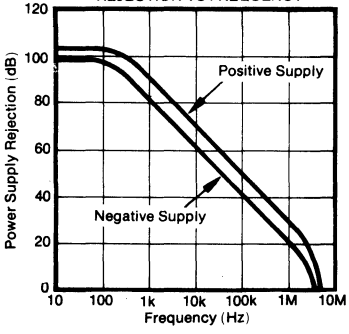
INPUT NOISE CURRENT VS FREQUENCY



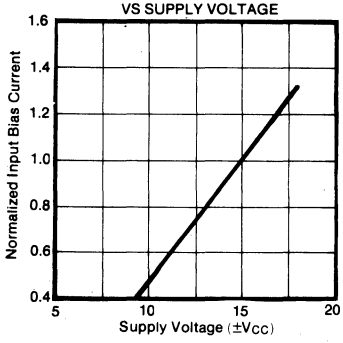
CHANNEL-TO-CHANNEL CROSSTALK VS FREQUENCY



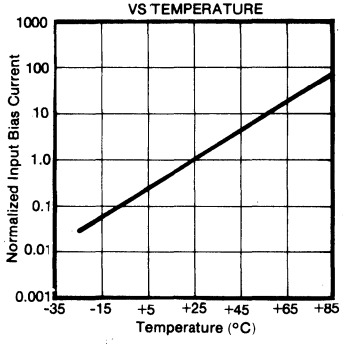
POWER SUPPLY REJECTION VS FREQUENCY



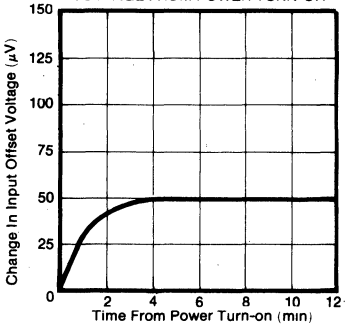
INPUT BIAS CURRENT VS SUPPLY VOLTAGE



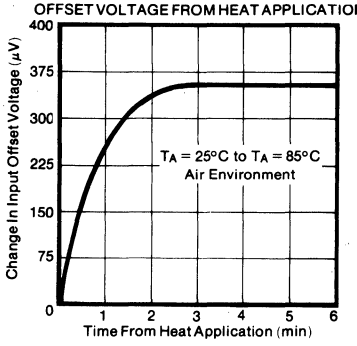
INPUT BIAS CURRENT VS TEMPERATURE



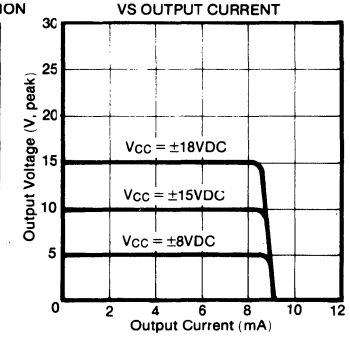
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



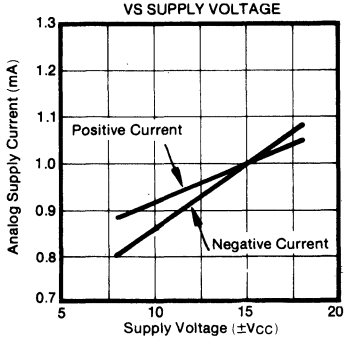
THERMAL RESPONSE TIME OF INPUT OFFSET VOLTAGE FROM HEAT APPLICATION



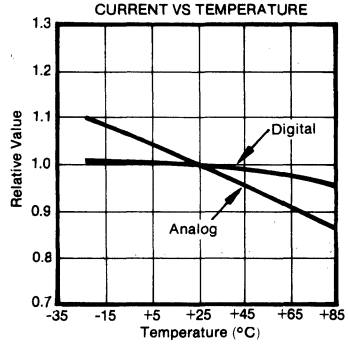
OUTPUT VOLTAGE VS OUTPUT CURRENT



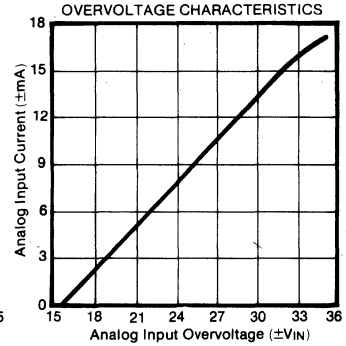
ANALOG SUPPLY CURRENT VS SUPPLY VOLTAGE



QUIESCENT SUPPLY CURRENT VS TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



DISCUSSION OF PERFORMANCE

The PGA100 is a self-contained programmable-gain amplifier whose gain can be changed in 8 binarily weighted steps from 1 to 128 or as scaled externally through the gain scale/adjust pin. The gain control is accomplished by the gain switch (break-before-make) whose position is determined by the 3-bit TTL address, A_3, A_4, and A_5. When selected, 1 of 8 positions connects the thin-film resistor network to the feedback loop of the op amp. This establishes the desired gain. (See Installation and Operating Instructions for gain scaling.)

Similarly, the 8 analog input channels are switched by the input multiplexer (break-before-make) whose position is determined by the 3-bit TTL address, A_0, A_1, and A_2. Gain and channel selection appear in Table I. 64-channel/gain combinations are possible.

The digital inputs are latched by the positive transition of the clock pulse, pin 18, when the clock enable, pin 19, is low. The relative set up and holding times specified in the Electrical Specifications are shown in Figure 1. The internal latch is similar to the industry standard 74LS378. Figure 2 shows a timing diagram for selected addresses indicating: the enable function, changing channel and gain, changing channel/constant gain, and constant channel/changing gain.

TABLE I. Gain and Channel Select Truth Table.

GAIN SELECT			GAIN	CHANNEL SELECT			CHANNEL
A_5	A_4	A_3		A_2	A_1	A_0	
0	0	0	1	0	0	0	IN0
0	0	1	2	0	0	1	IN1
0	1	0	4	0	1	0	IN2
0	1	1	8	0	1	1	IN3
1	0	0	16	1	0	0	IN4
1	0	1	32	1	0	1	IN5
1	1	0	64	1	1	0	IN6
1	1	1	128	1	1	1	IN7

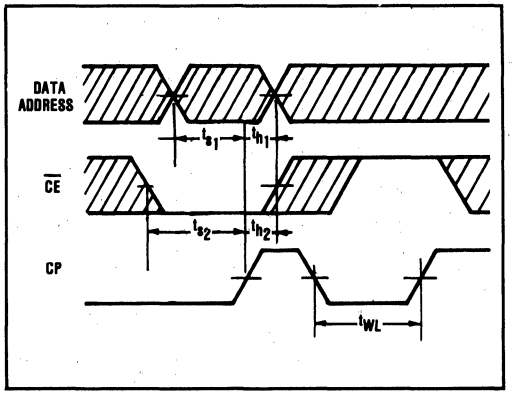


FIGURE 1. Data Address and Clock Enable Setup and Hold Times.

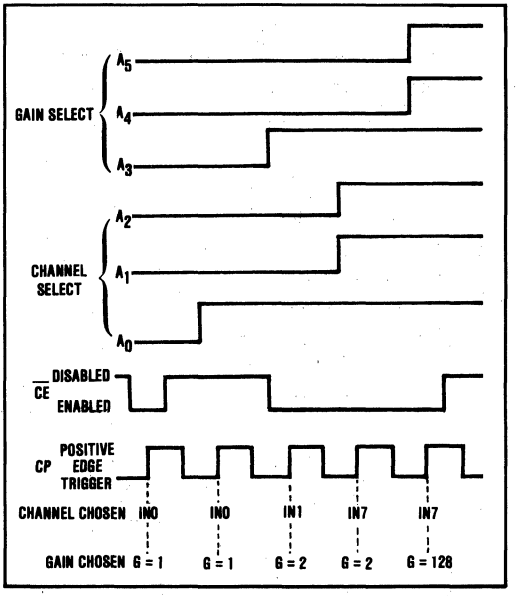


FIGURE 2. Timing Diagram for Selected Addresses.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY AND SIGNAL CONNECTIONS

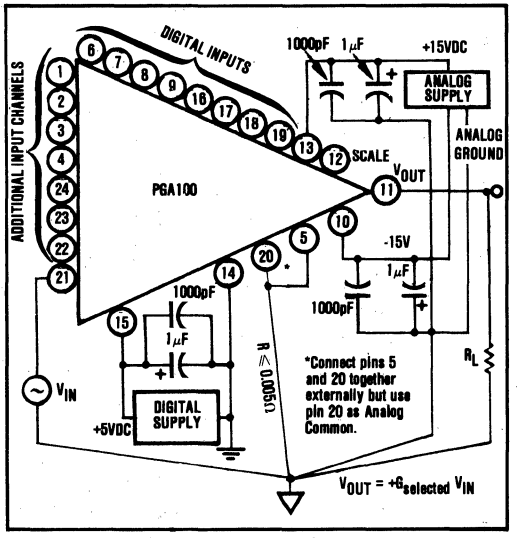


FIGURE 3. Basic Power Supply, Ground, and Signal Connections.

Figure 3 shows the proper analog and digital power supply connections. The supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. To avoid gain errors connect grounds as indicated being sure to minimize ground resistance. Note that a resistance of greater than

0.005Ω in series with the analog common will degrade the specified gain accuracy. IMPORTANT: Normally the digital ground is brought in from the digital power supply on a separate line. However, the analog and digital commons must be connected together somewhere in the system.

OPTIONAL GAIN SCALE/ADJUST

The gain scale/adjust pin is shown in Figure 4. When no connection is made, gains appear as in Table I. At least two functions can be performed. First, the gain range can be scaled to gains other than 1 to 128, for example, 1 to 100 or 1 to 1024. Gain steps, however, retain binary weighting. Some examples are: (1, 1, 2, 4, 8, 16, 32, 64 with pins 11 and 12 connected together), (1, 1.5625, 3.125, 6.25, 12.5, 25, 50, 100), (1, 12.5, 25, 50, 100, 200, 400, 800), and (1, 16, 32, 64, 128, 256, 512, 1024). Scaling is accomplished by using a potentiometer, R_1, shown in Figure 4. Be certain to use a potentiometer of good mechanical and thermal stability. Additional gain drift with temperature should be minimal since it depends on the thermal tracking of the resistance ratio, R_A to R_B, set by the potentiometer.

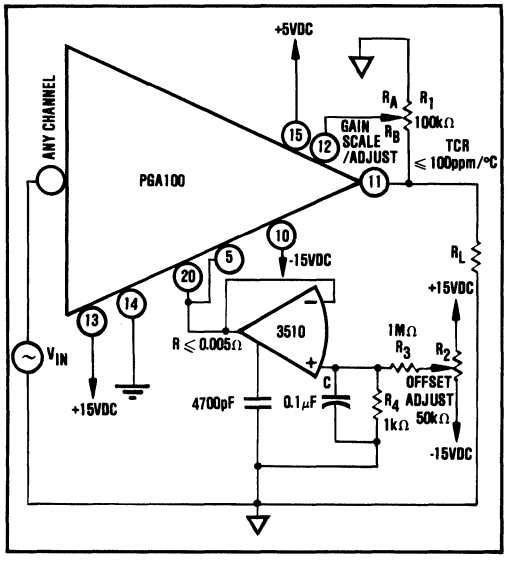


FIGURE 4. External Gain and Offset Adjustment.

Second, the gain inaccuracy, remaining after laser trimming at the factory, can be adjusted to zero at any gain other than unity. To improve resolution and limit adjustment range, a resistor may be added in series with the wiper of the potentiometer and pin 12. This will, however, increase gain drift. Figure 5 shows the effect of gain adjustment. R_1 does not affect gain linearity.

OPTIONAL OFFSET ADJUSTMENT

Figure 4 also illustrates a technique for offset adjustment. This adjustment has no effect at unity gain. R_2 will trim the offset to zero and have neglible effect on the gain accuracy. For best results, trim the offset at the highest

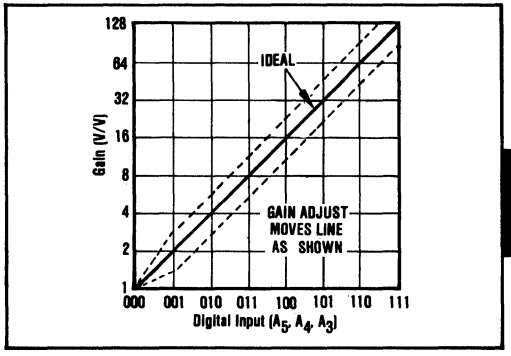


FIGURE 5. Effect of Gain Adjustment.

gain. If R_3 is made smaller, output offsetting can be accomplished. This can be used to introduce an intentional DC voltage at the output. The external amplifier used will add to the input noise, therefore, use one with a noise level of at least three times lower than that specified for the PGA100.

LAYOUT CONSIDERATIONS

Proper attention to layout is necessary to achieve the specified performance of the PGA100. Major goals are to reduce crosstalk, noise pickup, noise coupled from the power supply, and gain errors.

Be certain to separate analog and digital runs to avoid coupling of digital transients. To reduce gain errors, connect analog grounds with a ground plane or a low resistance star configuration as shown in Figure 3. Analog and digital commons must be connected at some point in the system to insure proper operation.

GAIN INACCURACY AND NONLINEARITY

As shown in Figure 3, connect pins 5 and 20 directly together at the unit and use pin 20 as the primary analog common. Ground resistance in series with pin 20 also appears in series with the internal gain-setting resistors and will decrease the magnitude of all gains except unity. The resulting accuracy error varies nonlinearly with the gain selected and therefore cannot be externally adjusted to zero for more than one gain at a time. Gain linearity is not affected by external ground resistance (see Performance Curves.)

CROSSTALK

Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is expressed as a percent of the input signal applied to all OFF channels. For example, the 0.003% specification indicates that 0.6mV, p-p, out of a 20V, p-p, 1kHz sine wave (applied to 7 OFF channels) will appear at the noninverting input of the internal op amp. Note that crosstalk increases with high frequencies due to the capacitive coupling between ON and OFF channels. It also increases with greater source resistance. However, because both the input signal and crosstalk noise are amplified equally, the resulting output signal-to-noise

ratio is independent of gain. Unused input channels should be grounded in order to reduce crosstalk and extraneous noise pickup. (See Performance Curves.)

SETTLING TIME

Settling time is the time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value. It is a very important consideration since ' s will be the limiting parameter in determining the maximum channel scanning or throughput rate. The PGA100 specification includes the effects of both the multiplexer and amplifier. Note that settling time increases with increasing source resistance and gain. Minimum settling time is achieved by choosing a low source resistance, for example, $R_S \leq 10k\Omega$ and gains ≤ 16. (See Performance Curves.)

INPUT OVERVOLTAGE PROTECTION

The PGA100 provides input overvoltage protection of 20V in excess of either power supply voltage expressed as $\pm(|V_{CC}|+20)$. This is achieved in the dielectrically isolated analog multiplexer which will withstand overvoltage even when the power supplies are off. As a consequence the PGA100 is protected against high input levels and brief transient spikes of up to several hundred volts that can result from signals originating from outside the system. (See Performance Curves.)

TYPICAL APPLICATIONS

The PGA100 is ideal for a variety of applications, especially where low channel-to-channel crosstalk is required. In many applications the PGA100 will not require trimming of offset and gain errors. However, these can be minimized utilizing hardware or software error correction techniques. Figures 6 and 7 show applications of the PGA100 separately and in a data acquisition system.

Figure 7 shows a Data Acquisition System. In this system the PGA100 allows the user to deal with signals of wide dynamic range while maintaining high system resolution. For example: When used with a 12-bit A/D converter in a "floating point" system, the 2^7 gain range of the PGA100 plus the 2^{12} range of the converter produces a total system resolution of 2^{19} (524,000 to 1).

Also the user can modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated amplifiers are not required for various input channels, the PGA100 also saves space and overall system costs. Software correction virtually eliminates system offset and gain errors over both time and temperature.

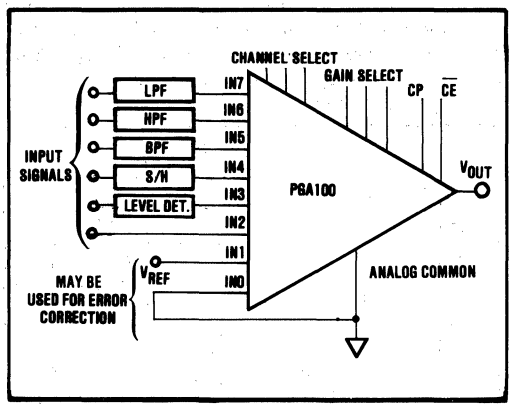


FIGURE 6. Digitally Selectable Function Amplifier.

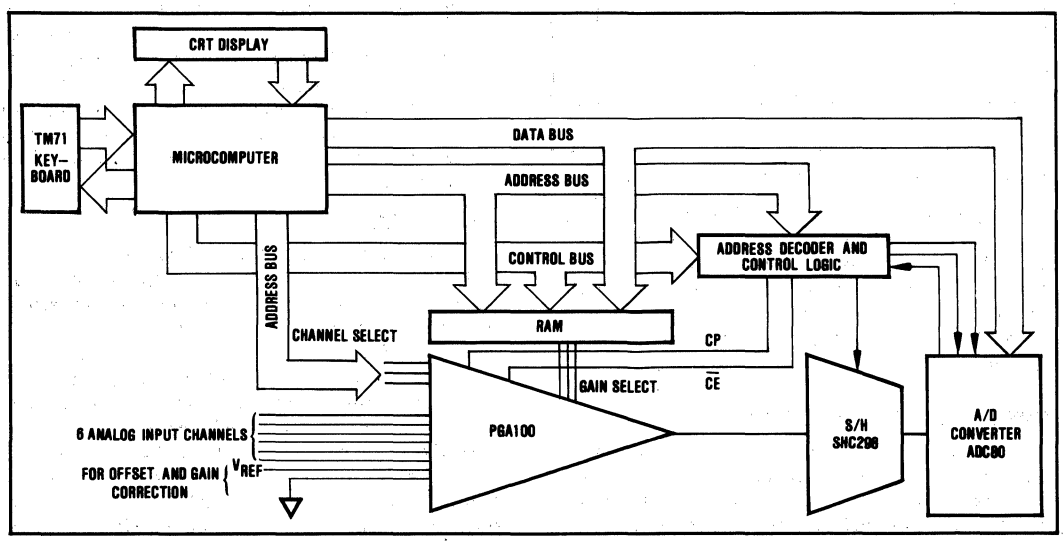


FIGURE 7. Use of PGA100 in a Data Acquisition System with Software Auto-zero and Gain Calibration.

BURR-BROWN®

XTR100

ADVANCE INFORMATION
Subject to Change

Precision, Low Drift 4mA to 20mA TWO-WIRE TRANSMITTER

FEATURES

- INSTRUMENTATION AMPLIFIER INPUT
  - Low Offset Voltage, 25μV max
  - Low Voltage Drift, 0.5μV/°C max
  - Low Nonlinearity, 0.01% max
- TRUE TWO-WIRE OPERATION
  - Power and Signal on One Wire Pair
  - Current Mode Signal Transmission
  - High Noise Immunity
- DUAL MATCHED CURRENT SOURCES
- WIDE SUPPLY RANGE, 11.6V to 40V
- -40°C TO +70°C SPECIFICATION RANGE
- SMALL 14-PIN DIP PACKAGE

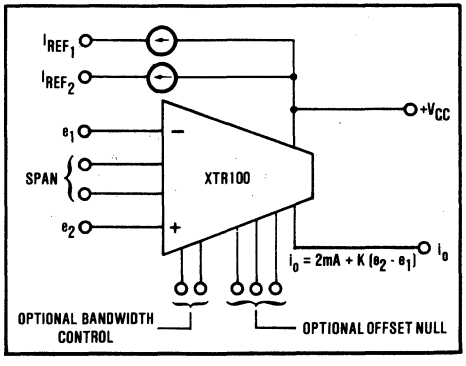
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  - Pressure Transmitters
  - Temperature Transmitters
  - Millivolt Transmitters
- RESISTANCE BRIDGE INPUTS
- THERMOCOUPLE INPUTS
- RTD INPUTS
- CURRENT SHUNT (mV) INPUTS
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR100 is a microcircuit, 4mA to 20mA, two-wire transmitter containing a high accuracy instrumentation amplified (IA), a voltage controlled output current source, and dual-matched precision current references. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTD's, thermistors, and strain gauge bridges. State-of-the art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers. Also, the XTR100 is generally very useful for low noise, current-mode signal transmission.



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PDS-467

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{CC}$ = 24VDC, R_L = 100Ω unles otherwise noted.

PARAMETER	CONDITIONS/DESIGNATION	XTR100AM/AP MIN	XTR100AM/AP TYP	XTR100AM/AP MAX	XTR100BM/BP MIN	XTR100BM/BP TYP	XTR100BM/BP MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS								
Current	Linear Operating Region	4		20	*		*	mA
Current	Derated Performance	3.8		22	*		*	mA
Current Limit	I_O min		28	38		*	*	mA
Offset Current Error	I_{OS}, I_O = 4mA			±4			*	µA
Offset Current Error vs Temp.	$\Delta I_{OS}/\Delta T$			±10			*	ppm, FS/°C
Full Scale Output Current Error	Full Scale = 20mA			±20			*	µA
Power Supply Rejection		120			*			dB
Power Supply Voltage	V_{CC}, pins 7 & 8, compliance(1)	+11.6		+40	*		*	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			*	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			*	Ω
SPAN								
Equation	R_S in Ω, e_1 and e_2 in V	$i_O = 4mA + [(0.016mA/mV + (40/R_S)](e_2 - e_1)$						
Untrimmed Error(2)	ϵ_{SPAN}	-3		0	*		*	%
Nonlinearity	$\epsilon_{NONLINEARITY}$			0.01			*	%
Hysteresis			0			*		%
Dead Band			0			*		%
Temperature Effects				±100			*	ppm %/°C
INPUT CHARACTERISTICS								
Impedance								
Differential			0.4 || 0.047			*		GΩ || µF
Common-Mode			10 || 180			*		GΩ || pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$(3)	0		1	*		*	V
Offset Voltage	V_{OS}			±50			±25	µV
vs Temperature	$\Delta V_{OS}/\Delta T$			±1			±0.5	µV/°C
Bias Current	I_B			150			*	nA
vs Temperature	$\Delta I_B/\Delta T$			1			*	nA/°C
Offset Current	I_{OSI}			±30			*	nA
vs Temperature	$\Delta I_{OSI}/\Delta T$			0.3			*	nA/°C
Common-Mode Rejection(4)	DC	90			*		*	dB
Common-Mode Range	e_1 and e_2 with respect to pin 7	4		6	*		*	V
CURRENT SOURCES								
Magnitude			1			*		mA
Accuracy	V_{CC} = 24V, $V_{PIN\ 8}$ to $V_{PIN\ 10, 11}$ = 14V, R_2 = 5k, Fig. 3			±0.05			*	%
vs Temperature				±30			*	ppm/°C
vs Time			±8			*		ppm/mo.
Ratio Match	Tracking							
Accuracy	1 - I_{REF1}/I_{REF2}			±0.01			*	%
vs Temperature				±10			*	ppm/°C
vs Time			±1			*		ppm/mo.
Output Impedance		10			*			MΩ
TEMPERATURE RANGE								
Specification		-40		+85	*		*	°C
Operating (AM, BM)		-55		+125	*		*	°C
(AP, BP)		-40		+85	*		*	°C
Storage (AM, BM)		-55		+165	*		*	°C
(AP, BP)		-40		+85	*		*	°C

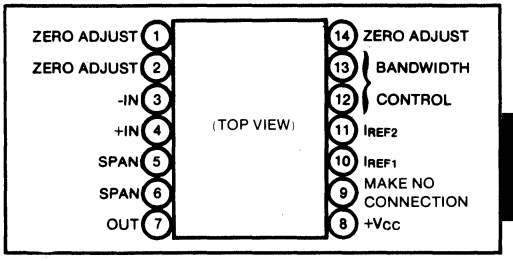
*Same as XTR100AM/AP.

NOTES:
1. See Typical Performance Curves.
2. Span error shown is untrimmed and may be adjusted to zero.
3. e_1 and e_2 are signals on the -IN and +IN terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR100A and XTR100B grades respectively.
4. Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Applications Information section.

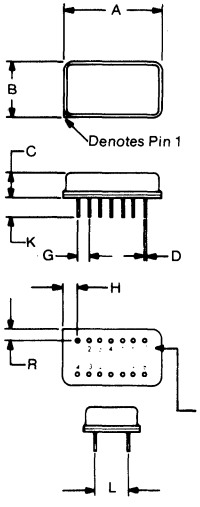
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC}	40V
Input Voltage, e_1, or e_2	$\geq V_{OUT}$, $\leq +V_{CC}$
Storage Temperature Range, metal	-55°C to +165°C
Storage Temperature Range, plastic	-40°C to +85°C
Lead Temperature (soldering 10 seconds)	300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	+165°C

PIN DESIGNATIONS



MECHANICAL

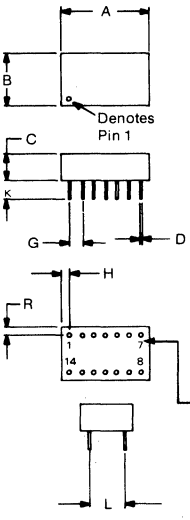


XTR100AM/BM (Metal)

NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

Pin numbers shown for reference only. Numbers are not marked on package.



XTR100AP/BP (Plastic)

NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

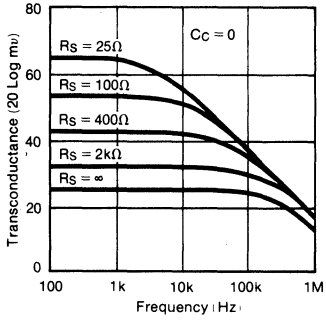
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

Pin numbers shown for reference only. Numbers are not marked on package.

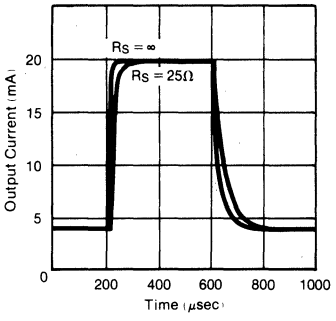
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, $+V_{CC}$ = 24VDC unless otherwise noted)

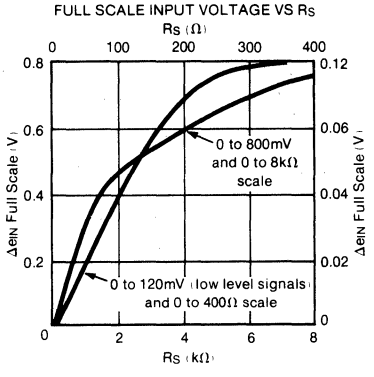
SPAN VS FREQUENCY

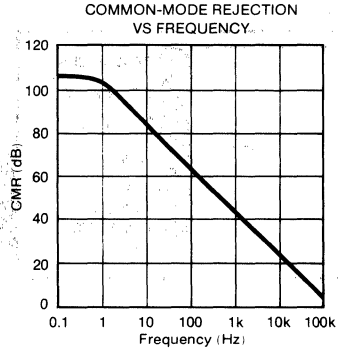


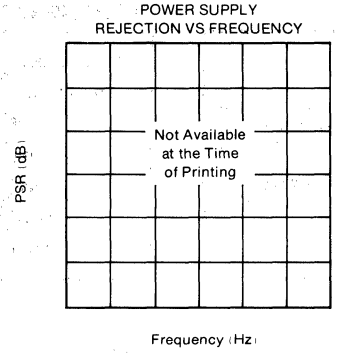
STEP RESPONSE

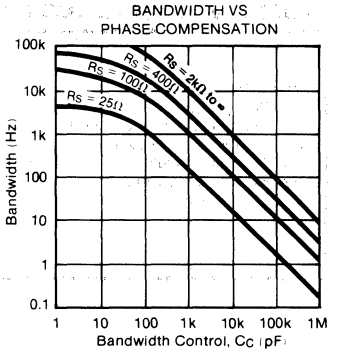


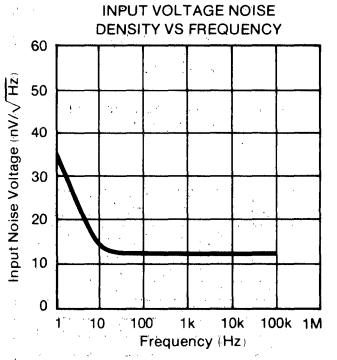
FULL SCALE INPUT VOLTAGE VS RS

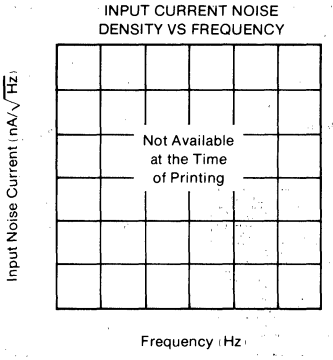


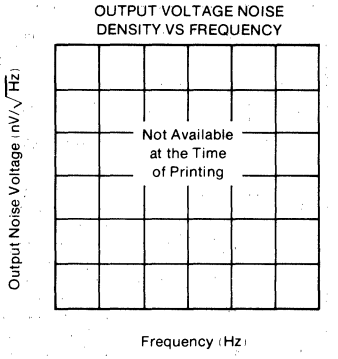












THEORY OF OPERATION

A simplified schematic of the XTR100 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as an instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016mA/mV + 40/R_S)(e_{IN}$ full scale$) = 16mA$. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geqslant e_1$ or $e_{IN} \geqslant 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

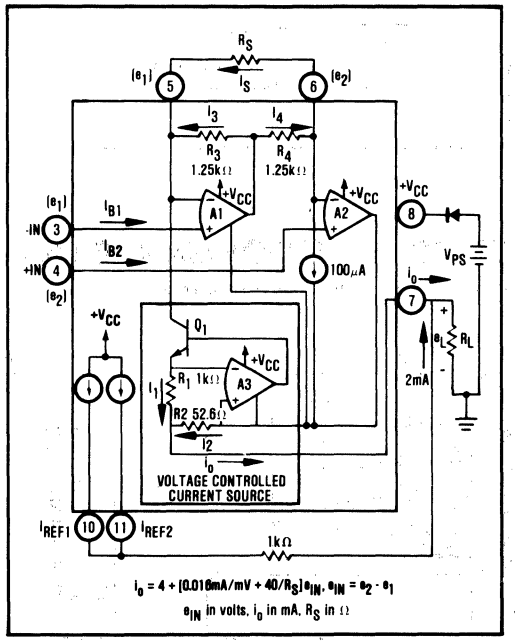


FIGURE 1. Simplified Schematic of the XTR100.

INSTALLATION AND OPERATING INSTRUCTIONS

Major points to consider when designing with the XTR100:

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a $0.01\mu F$ capacitor as close to the unit at possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation;
   $4V \leqslant e_1 \leqslant 6V$
   $4V \leqslant e_2 \leqslant 6V$
   (e_1 and e_2 measured with respect to pin 7)
4. The maximum input signal level ($e_{IN_{FS}}$) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation connect them together and through a $1k\Omega$ resistor to pin 7. Each reference must have between +1V and $+(V_{CC} - 4V)$ with respect to pin 7.
6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4mA to 20mA range (see Figure 2).
7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR100 caused by momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.

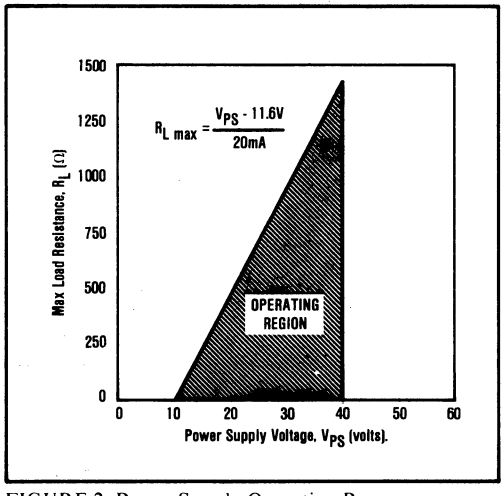


FIGURE 2. Power Supply Operating Range.

SELECTING R_S

R_{SPAN} is chosen so that a given full scale input span $e_{IN_{FS}}$ will result in the desired full scale output span of $\Delta I_{O_{FS}}$, 16mA $[(0.016mA/mV) + (40/R_S)]\ \Delta e_{IN} = \Delta I_O$.

Solving for R_S;

$$R_S = \frac{40}{\Delta I_O/\Delta e - 0.016\ \frac{mA}{mV}} \qquad (1)$$

where R_S is in Ω
ΔI_O is in mA
Δe_{IN} in mV

For example, if $\Delta e_{IN_{FS}} = 100mV$ for $\Delta I_{O_{FS}} = 16mA$

$$R_S = \frac{40}{(16/100) - 0.016} = \frac{40}{0.16 - 0.016} = \frac{40}{0.144} = 278\Omega$$

See Typical Performance Curves for a plot of R_S vs $\Delta e_{IN_{FS}}$. Note that in order not to exceed the 20mA upper range limit e_{IN} must be less than 1V when $R_S = \infty$ and proportionately smaller as R_S decreases.

BIASING THE INPUTS

The internal circuitry of the XTR100 is such that both e_1 and e_2 must be kept approximately 5V above the voltage at pin 7. This is easily done by using one or both current sources and an external resistor R_2. Figure 3 shows the simplest case - a floating voltage source e'_2. The 2mA from the current sources flows through the $2.5k\Omega$ value of R_2 and both e_1 and e_2 are raised by the required 5V with respect to pin 7. For linear operation the constraint is

$+4V \leqslant e_1 \leqslant +6V$
$+4V \leqslant e_2 \leqslant +6V$

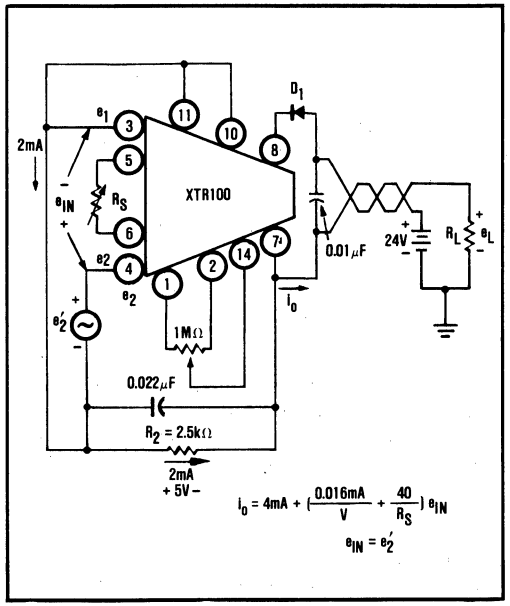


FIGURE 3. Basic Connection for Floating Voltage Source.

Figure 4 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources.

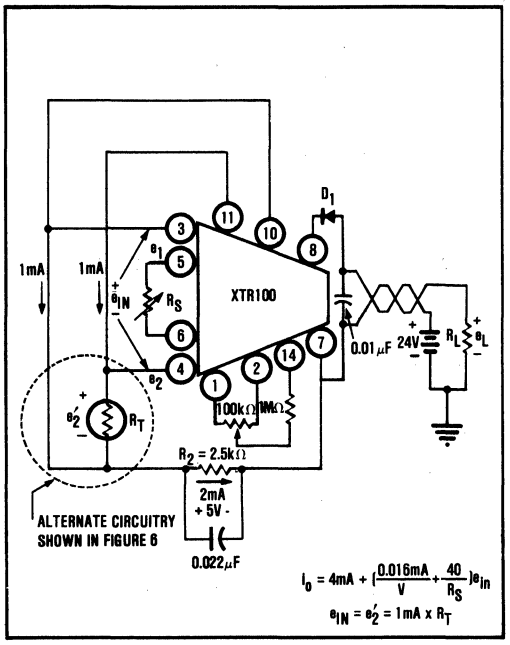


FIGURE 4. Basic Connection for Resistive Source.

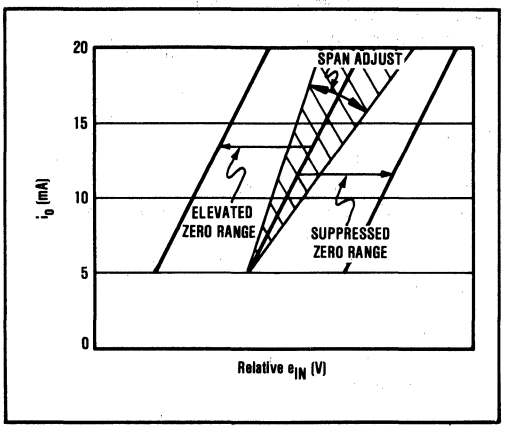


FIGURE 5. Elevation and Suppression Graph.

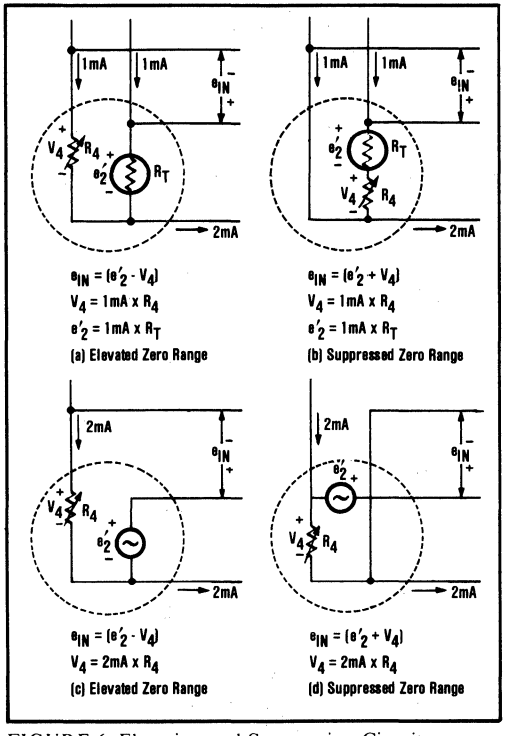


FIGURE 6. Elevation and Suppression Circuits.

CMV AND CMR

Thus the XTR100 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications. If the inputs are biased at some other CMV then an input offset error term is (CMV - 5)/CMRR; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR100 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 5 and 6(a). In this example the sensor voltage is derived from R_T (a thermistor, RTD or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 6(b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2, and 14) for elevation/suppression. This trim capability is used only to null the amplifiers input offset voltage. In many applications the already low offset voltage (typically 20μV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3μV/°C per 100μV of induced offset.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR100 ideal for a variety of two-wire transmitter applications. It can be used by OEM's producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise

interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR100 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1 - RTD Transducer shown in Figure 7. Given a process with temperature limits of + 25°C and +150°C, configure the XTR100 to measure the temperature with a Platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

Computing R_S.

The sensitivity of the RTD is $\Delta R/\Delta T = 100\Omega/266°C$. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span) the span of e_{IN} is 1mA x (100Ω/266°C) x 125°C = 47mV = Δe_{IN}.

$$\text{From equation 1, } R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{in}} - \frac{0.016mA}{mV}}$$

$$R_S = \frac{40}{\frac{16mA}{47mV} - \frac{0.016mA}{mV}} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

Computing R_4:

$$\text{At } 25°C,\ e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 25°C)]$$
$$= 1mA \times 109.4\Omega$$
$$= 109.4mV$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA the input circuitry shown in Figure 7 is used.

e_{IN} is made 0 at 25°C
or $e'_{2\,25°C} - V_4 = 0$
thus, $V_4 = e'_{2\,25°C} = 109.4mV$

$$R_4 = \frac{V_4}{1mA} = \frac{109.4mV}{1mA} = 109.4\Omega$$

Computing R_2 and checking CMV:

At 25°C, $e'_2 = 109.4mV$

$$\text{At } 150°C,\ e'_2 = 1mA \times [100\Omega + (\frac{100\Omega}{266°C} \times 150°C)]$$
$$= 156.4mV$$

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage they may be ignored in computing R_2 as long as the CMV is met.

$R_2 = 5V/2mA = 2.5k\Omega$

e_2 min = 5V + 0.1094V
e_2 max = 5V + 0.1564V
e_1 = 5V + 0.1094V

The +4V to +6V CMV requirement is met.

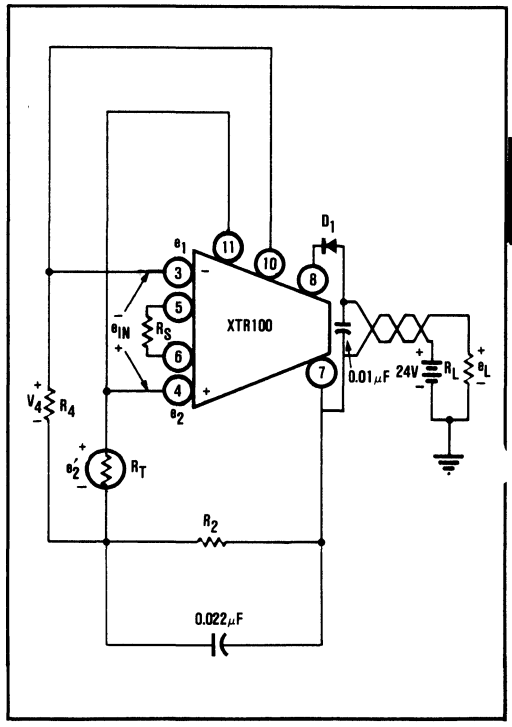


FIGURE 7. Circuit for Example 1.

EXAMPLE 2 - Thermocouple Transducer shown in Figure 9. Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR100 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.

Establishing R_S:

The input full scale span is 58mV ($\Delta e_{IN_{FS}} = 58mV$).

R_S is found from equation (1)

$$R_S = \frac{40}{\frac{\Delta I_O}{\Delta e_{IN}} \quad \frac{0.016mA}{mV}}$$

$$= \frac{40}{\frac{16mA}{58mV} - \frac{0.016mA}{mV}} = \frac{40}{0.2599}$$

$R_S = 153.9\Omega$

Cold Junction Compensation:

The temperature reference circuit is shown in Figure 8.

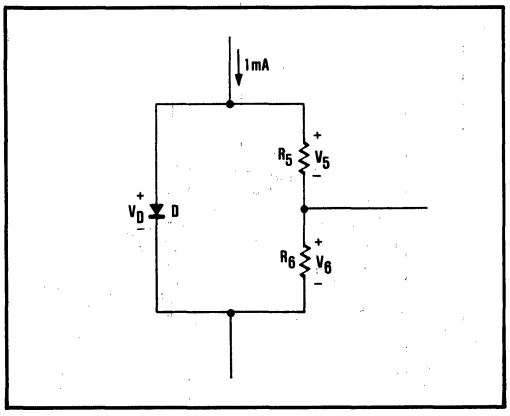


FIGURE 8. Cold Junction Compensation Circuit.

The diode voltage has the form

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at $T_2 = 25°C$, $V_D = 0.6V$ and $\Delta V_D/\Delta T = -2mV/°C$. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta V_D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At 25°C this is approximately 52·V/°C (obtained from standard thermocouple table) therefore,

$$\Delta V_{TC}/\Delta T = \Delta V_D/\Delta T \left(\frac{R_6}{R_5 + R_6}\right)$$

$$52\mu V/°C = 2000\mu V/°C \left(\frac{R_6}{R_5 + R_6}\right) \qquad (2)$$

R_5 is chosen as 2kΩ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

Selecting R_4:

R_4 is chosen to make the output 4mA at $T_{TC} = 0°C$ ($V_{TC} = -1.28mV$) and $T_D = 25°C$ ($V_D = 0.6V$). A circuit is shown in Figure 9.

V_{TC} will be -1.28mV when $T_{TC} = 0°C$ and the reference junction is at +25°C. e_1 must be computed for the condition of $T_D = +25°C$ to make $e_{IN} = 0V$.

$V_{D_{25°C}}$ = 600mV.
$e_{1_{25°C}}$ = 600mV x 51/205 = 14.9mV
e_{IN} = $e_2 - e_1 = +V_{TC} + V_4 - e_1$
with e_{IN} = 0 and $V_{TC} = -1.28mV$
V_4 = $e'_T + e_{IN} - V_{TC} = 14.9mV + 0V - (-1.28mV)$
1mA x R_4 = 16.18mV
R_4 = 16.18Ω

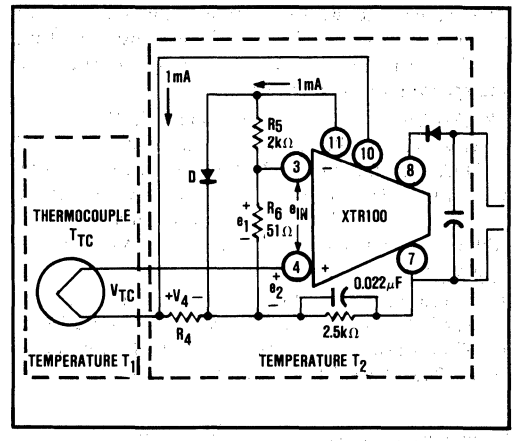


FIGURE 9. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typicaly done by forcing the two-wire transmitter current to either limit when the thermocouple impedance goes very high. The circuits of Figures 14 and 15 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the +input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 16 should be used. When the TC opens the output will go to its upper range limit value (about 38mA).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR100 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltage (25μV max for the B grade, 50μV max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2, and 14 as shown in Figures 3 and 4. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering can be done by either one of two techniques shown in Figure 10. C_2 connected to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by

$$f_{CO} = \frac{1.59 \times 10}{(R_1 + R_2 + R_3 + R_4)(C_2 + 0.047\mu F)}$$

with f_{CO} in Hz, all R_S in Ω and C_2 in μF. This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1 will use smaller values of capacitance and is not a function of the input resistors. It is however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

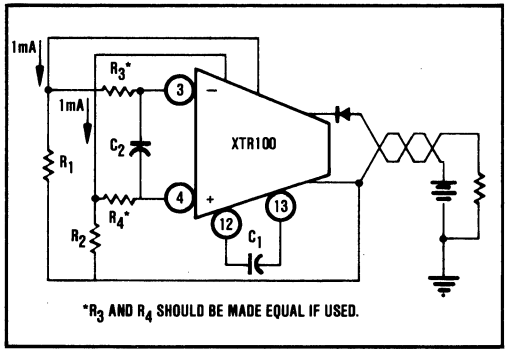


FIGURE 10. Optional Filtering.

APPLICATION CIRCUITS

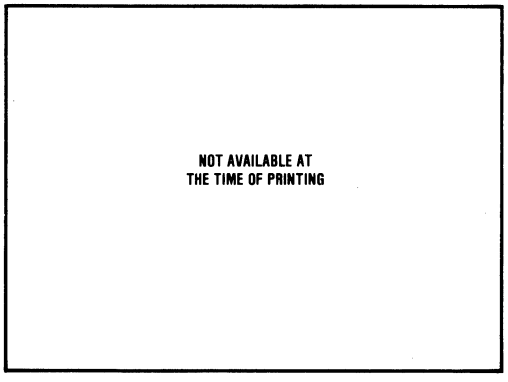


FIGURE 11.

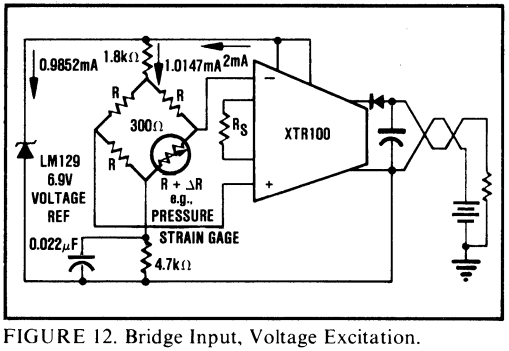


FIGURE 12. Bridge Input, Voltage Excitation.

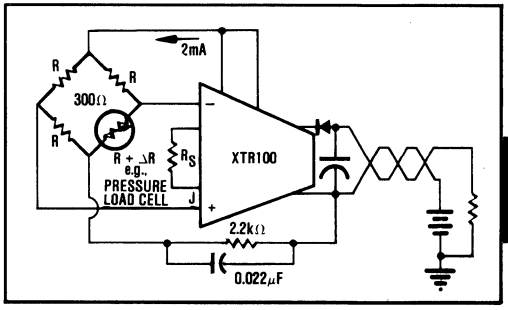


FIGURE 13. Bridge Input, Current Excitation.

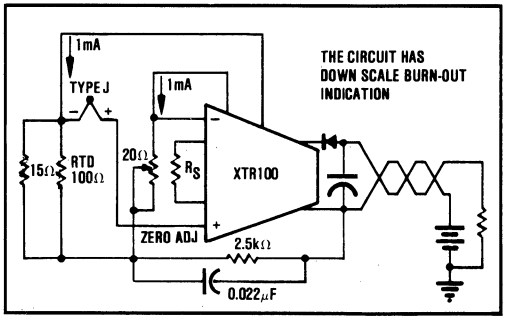


FIGURE 14. Thermocouple Input with RTD Cold Junction Compensation.

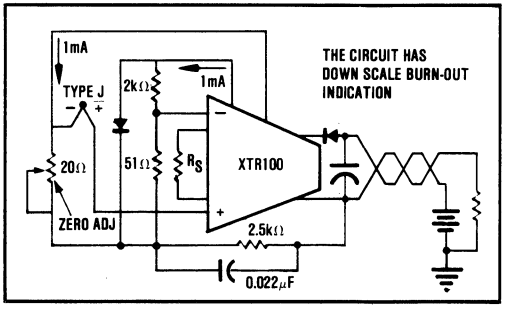


FIGURE 15. Thermocouple Input with Diode Cold Junction Compensation.

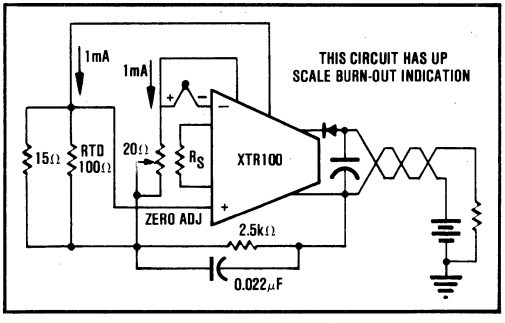


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O\ IDEAL} = 4mA + K\ e_{IN} \quad (3)$$

K is the span (gain) term, $(0.016mA/mV) + (40/R_S)$

The nature of the XTR100 circuit is such that there are three major components of error

σ_O = error associated with the output stage.
σ_S = errors associated with span adjustment.
σ_I = errors associated with input stage.

The transfer function including these errors is

$$I_{O\ ACTUAL} = (4mA + \sigma_O) + K\ (1 + \sigma_S)(e_{IN} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms ($\sigma_S\ \sigma_I$) dropped, and terms collected, the result is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ e_{IN}\ \text{“}K\sigma_I + K\sigma_S\ e_{IN} \quad (5)$$

The error in the output current is $i_{O\ ACTUAL} - i_{O\ IDEAL}$ and can be found by subtracting equations (5) and (3).

$$i_{O\ ERROR} = \sigma_O + K\sigma_S + K\ \sigma_S\ e_{IN} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR100 and the particular circuit in which it is applied. The circuit of Figure 7 will be used to illustrate the principles.

$$\sigma_O = I_{OS_{RTO}} \quad (7)$$

$I_{OS_{RTO}}$* = the output offset error current.

For the circuit of Figure 7,

$$\sigma_I = V_{OSI} + [I_{B1}\ R_T - I_{B2}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR} \quad (8)$$

The term in brackets maybe written in terms of offset current and resistor mismatches as $I_{B1}\ \Delta R + I_{OS}'\ R_4$.

V_{OSI}* = input offset voltage
I_{B1},* I_{B2}* = input bias current
I_{OSI}* = input offset current
$\Delta R = R_T - R_4$ = mismatch in resistor
ΔV_{CC} = change supply voltage between pins 7 and 8 away from 24V nomimal
PSRR* = power supply rejection ratio
CMRR* = common-mode rejection ratio
$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
ϵ_{NONLIN}* = span nonlinearity
ϵ_{SPAN}* = span equation error. Untrimmed error = 3% max. May be trimmed to zero.

*Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

Given the circuit in Figure 7 with the XTR100B specifications and the following conditions: R_T = 109.4Ω at 25°C, R_T = 156.4Ω at 150°C, I_o = 4mA at 25°C, I_o = 20mA at 150°C, R_S = 123.3Ω, R_4 = 109Ω, R_L = 250Ω, R_{LINE} = 100Ω, V_{D1} = 0.6V, V_{PS} = 24V ±0.5%. Determine the % error at the upper and lower range values.

A. At the lower range value (T = 25°C).

$$\sigma_O = I_{OS_{RTO}} = \pm 4\mu A$$

$$\sigma_I = V_{OSI} + [I_{B1}\ \Delta R + I_{OSI}\ R_4] + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5}{CMRR}$$

$$\Delta R = R_{T_{25°C}} - R_4 = 109.4 - 109 \approx 0$$

$$\Delta V_{CC} = 24 \times 0.005 + 4mA\ (250\Omega + 100\Omega) + 0.6V = 120mV + 1400mV + 600mV = 2120mV$$

$$e_1 = (2mA \times 2.5k\Omega) + (1mA \times 109\Omega) = 5.109V$$

$$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 109.4\Omega) = 5.1094V$$

$$(e_1 + e_2)/2 - 5 \approx 0$$

$PSRR = 3.16 \times 10^{-6}$ for 130dB
$CMRR = 31.6 \times 10^{3}$ for 90dB

$$\sigma_I = 25\mu V + (150nA \times 0 + 30nA \times 109\Omega) + \frac{2120mV}{3.16 \times 10^6} + \frac{0}{31.6 \times 10^3}$$

$$= 25\mu V + 3.27\mu V + 0.067\mu V + 0 = 28.3\mu V \quad (9)$$

$\sigma_S = \epsilon_{NONLIN} + \epsilon_{SPAN}$
$= 0.0001 + 0$ (assumes trim of R_S)
i_O error $= \sigma_O + K\ \sigma_I + K\ \sigma_S\ e_{IN}$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} = 0.341\upsilon$$

$e_{IN} = e_2' - V_4 = I_{REF1}\ R_{T_{25°C}} - I_{REF2}\ R_4$
since $R_{T\ 25°C} = R_4$
$e_{IN} = (I_{REF1} - I_{REF2})\ R_4 = 0.1\mu A \times 109\Omega = 10.9\mu V$

Since the maximum mismatch of the current references is 0.01% of 1mA = 0.1μA

$$i_O \text{ error} = 4\mu A + (0.34\upsilon \times 28.9\mu V) + (0.341 \times 0.0001) \times 10.9\mu V = 4\mu A + 9.85\mu A + 0.0004\mu A = 13.9\mu A$$

$$\%\text{error} = \frac{13.9\mu A}{4mA} \times 100\% = 0.35\% \text{ at lower range value.}$$

B. At the upper range value (T = 150°C)

$$\Delta R = R_{T\ 150°C} - R_4 = 156.4 - 109.4 = 47\Omega$$

$$\Delta V_{CC} = 24 \times 0.005 + 20mA\ (250\Omega + 100\Omega) + 0.6 = 7720mV$$

$e_1 = 5.109V$

$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 156.4\Omega) = 5.156V$

$(e_1\ e_2)/2 - 5V \approx 0$

$\Delta R = -R_{T\ 150°C} + R_4 = 156.4 - 109 = 47\Omega$

$\sigma_O = 4\mu A$

$\sigma_1 = 25\mu V + (150nA \times 47\Omega + 30nA \times 109\Omega)$

$$+ \frac{7720mV}{3.16 \times 10^6} + \frac{0}{31.6 \times 10^3}$$

$= 25\mu V + 10.33\mu V) + 0.25\mu V\ F0 = 35.58\mu V$

$\sigma_S = 0.0001$

$e_{IN} = e_2' - V_4 = I_{REF1}\ R_{T\ 150°C} - I_{REF2}\ R_4$

$= 1mA \times 156.4\Omega - 1mA\ 109\Omega$

$= 47mV.$

$i_{O\ ERROR} = \sigma_O + K\ \sigma_1 + K\ \sigma_S \times e_{IN}$

$= 4\mu A + 0.341\upsilon \times 39.9\mu V + 0.341\upsilon \times 0.0001 \times 47000\mu V$

$= 4 \times 12.1 + 1.6 = 17.7\mu A \qquad (10)$

$$\% \text{ error} = \frac{17.7}{20mA} \times 100\% = 0.088\% \text{ at upper}$$

range value or % of FS.

CONCLUSIONS

From equation (9) it is observed that the predominant error term is the input offset voltage (25μV for the B grade). This is of little consequence in many applications. $V_{OS\ RTI}$ can, however, be nulled using the pot shown in Figures 3 and 4. From equation (10), the predominant errors are $I_{OS\ RTI}$ (4μA), $V_{OS\ RTI}$ (25μV), and I_B (150nA).

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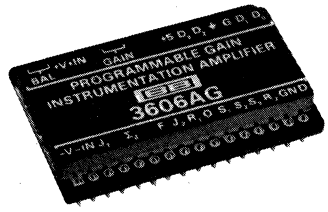
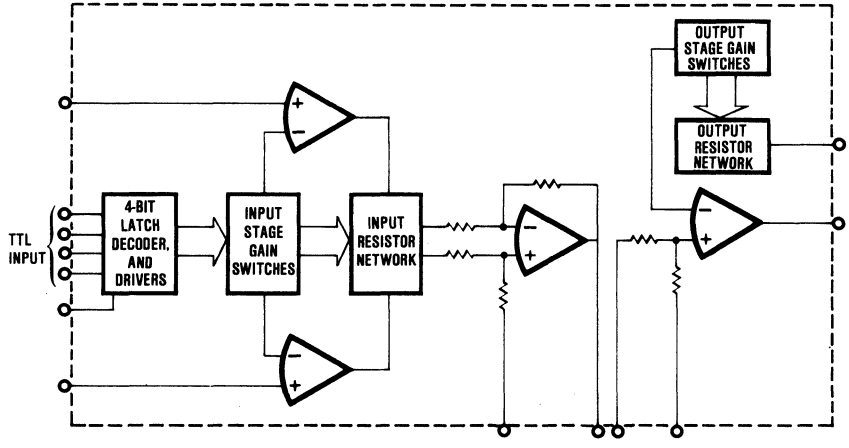


3606

Digitally Controlled Programmable Gain INSTRUMENTATION AMPLIFIER

FEATURES

- 11 BINARY GAINS - 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024V/V
- 4-BIT TTL GAIN CONTROL
- EXCELLENT GAIN NONLINEARITY 0.01% max at G = 1024V/V
- LOW GAIN ERRORS - 0.02% max
- LOW GAIN DRIFT - 10ppm/°C max
- LOW VOLTAGE DRIFT 1μV/°C max RTI, G = 1024V/V
- HIGH CMR - 110dB min, G = 1024V/V
- HIGH INPUT IMPEDANCE - 10 x $10^9\Omega$
- LOW OFFSET VOLTAGE 22μV max RTI, G = 1024V/V 2mV max RTI, G = 1V/V



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PDS-388A

DESCRIPTION

The 3606 is a self-contained, Programmable Gain Instrumentation Amplifier (PGIA) whose gain can be changed in 11 binary weighted steps from 1 to 1024V/V. The gain control is accomplished through a 4-bit TTL input.

The PGIA function allows the user to deal with wide dynamic range signals while maintaining high system resolution. For example: when used with a 10-bit A to D converter in a "floating point" system, the 2^{10} gain range of the 3606, plus the 2^{10} range of the converter produces a total system resolution of 2^{20} (|| 1,000,000:1).

Desirable characteristics of a high performance instrumentation amplifier are offered by the 3606: high input impedance (10GΩ), excellent gain nonlinearity (0.01% max, G = 1024V/V; 0.02% max, G = 1V/V), high common-mode rejection (100dB min, G≥ 4V/V), low gain error (0.02% max with no trimming required), low gain temperature coefficient (10ppm/°C max), and low offset voltage drift vs temperature (1μV/°C max, RTI, G = 1024).

Added to these outstanding instrumentation amplifier characteristics is the ability to change 3606's gain under control of a 4-bit TTL input word. An important characteristic of the 3606 PGIA is its low change in offset plus laser trimming minimized this change to a maximum of ±25mV with no external adjustments. With two simple offset adjustments the change can be limited to less than 2mV (1mV typ) at the output over the entire 1V/V to 1024V/V gain range.

A simplified schematic of the 3606 is shown in Figure 1. The circuit consists of a variable gain high input impedance voltage follower input stage (A1 and A2) followed by a unity gain difference amplifier (A3) with a variable gain output stage (A4).

Common-mode voltage is derived for active guard drive to improve system common-mode rejection. Two-pole, low-pass filtering can easily be implemented on the output stage to reduce noise bandwidth and improve system signal-to-noise operation. A latch function is provided to inhibit gain changes while the digital gain control input is changed.

Burr-Brown's instrumentation grade monolithic operational amplifiers, high stability precision thin-film resistor networks and advanced laser-trimming techniques are used by the 3606 to achieve a performance, size and cost combination never before achieved in a PGIA. It is available in a 32-pin dual-in-line package in either ceramic or metal (hermetic) configurations.

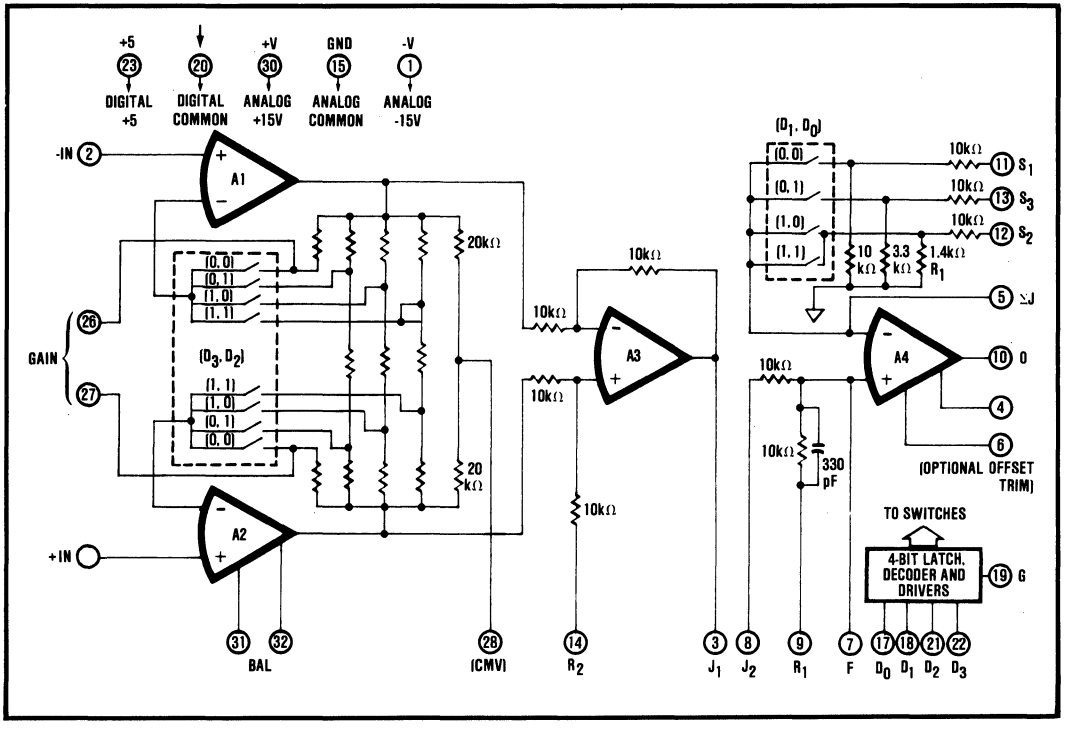


FIGURE 1. Simplified Schematic.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	3606A[7] MIN	3606A[7] TYP	3606A[7] MAX	3606B[7] MIN	3606B[7] TYP	3606B[7] MAX	UNITS
GAIN, G[1]								
Inaccuracy	G = 1 to 1024, I_O = 1mA		±0.02	±0.05		±0.01	±0.02	%
Nonlinearity[2]	G = 1 to 16		0.001	0.002		*	*	%[5]
	G = 32 to 128		0.003	0.004		*	*	%
	G = 256 to 1024		0.005	0.01		*	*	%
Drift vs Temperature	G = 1 to 1024		±5	±10		*	*	ppm/°C
vs Time	G = 1 to 1024		±0.01					%/1000 hrs
RATED OUTPUT								
Voltage	I_O = ±5mA	±10	±12		*	*		V
Current	V_O = ±10V	±5	±10		*	*		mA
Impedance			0.05			*		Ω
INPUT CHARACTERISTICS								
Absolute Max Voltage	No damage			±Vcc			*	V
Common-Mode Voltage Range	Linear operation	±10	±10.5		*	*		V
Differential Impedance			10 || 3			*		$10^9\Omega$ || pF
Common-Mode Impedance			10 || 3			*		$10^9\Omega$ || pF
OFFSET VOLTAGE, RTO[3]								
Initial at 25°C[4]			±(0.02G +1)	±(0.04G +2)		±(0.01G +1)	±(0.02G +2)	mV
vs Temperature	-25°C to +85°C		(±0.0015G ±0.03G_2)	(±0.003G ±0.05G_2)		(±0.0005G ±0.01G_2)	(±0.001G ±0.02G_2)	mV/°C
vs Time			(±0.001G ±0.01G_2)			*		mV/mo
vs Supply			(±0.002G ±0.04G_2)			*		mV/V
vs Gain[5]	With trimming		±1	±2		*	*	mV
INPUT BIAS CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	-25°C to +85°C		±0.3			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	+25°C		±15	±50		±5	±20	nA
vs Temperature	-25°C to +85°C		±0.5			*		nA/°C
vs Supply Voltage			±0.1			*		nA/V
INPUT NOISE								
Voltage	$R_{SOURCE} \leq 5k\Omega$							
0.01Hz to 10Hz	G = 1024		1.4			*		μV, p-p
10Hz to 1kHz			1.0			*		μV, rms
Current								
0.01Hz to 10Hz			70			*		nA, p-p
10Hz to 1kHz			20			*		nA, rms
COMMON-MODE REJECTION								
DC, 1kΩ Source Imbalance								
G = 1, 2		80	90		90	100		dB
G = 4 to 6		90	100		100	110		dB
G = 32 to 1024		100	114		110	114		dB
60Hz, 1kΩ Source Imbalance								
G = 1, 2		80	86		*	*		dB
G = 4 to 16		90	96		*	*		dB
G = 32 to 1024		100	106		*	*		dB
DYNAMIC RESPONSE								
±3dB Response	Small Signal							kHz
G = 1			100			*		kHz
G = 32 to 128			40			*		kHz
G = 256 to 1024			10			*		kHz
±1% Response	Small Signal							
G = 1			40			*		kHz
G = 32 to 128			8			*		kHz
G = 256 to 1024			3			*		kHz
Slew Rate	G = 1	0.2	0.5			*		V/μsec
Settling Time	G = 128							
to 1%			75			*		μsec
to 0.1%			100			*		μsec
to 0.01%			200			*		μsec

ELECTRICAL (CONT)

Typical at +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	3606A(7) MIN	3606A(7) TYP	3606A(7) MAX	3606B(7) MIN	3606B(7) TYP	3606B(7) MAX	UNITS
LOGIC VOLTAGES								
"0" Level(6)			0	+0.4		*	*	V
"1" Level(6)		+2.4	+5.0		*	*		V
Absolute Max	No damage			+7				V
ANALOG SUPPLY								
Rated Voltage			±15			*		VDC
Voltage Range, Derated Performance		±8		±18	*		*	VDC
Current, quiescent			±10	±20		*	*	mA
DIGITAL SUPPLY								
Rated Voltage			+5			*		VDC
Voltage Range		+4.5		+5.5	*		*	VDC
Current, quiescent			10			*		mA
TEMPERATURE RANGE								
Specification		-25		+85	*		*	°C
Storage		-40		+100	*		*	°C

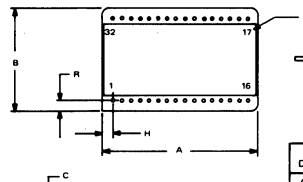
*Specifications same as 3606A.

NOTES:

1. $G = G_1 \times G_2$.
2. Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.
3. "RTO = Referred To Output. May be referred to input by dividing by gain G.
4. May be adjusted to zero.
5. Trimmed according to Figure 8.
6. All digital inputs are 1 TTL unit load.
7. Specify 3606AG or 3606BG for ceramic package and 3606AM or 3606BM for metal package - see below.

MECHANICAL

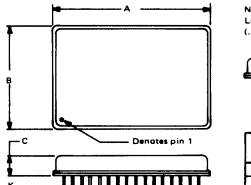
"G" PACKAGE



NOTE:
LEADS IN TRUE POSITION WITHIN .010" (.25mm)R @ MMC AT SEATING PLANE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

"M" PACKAGE



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

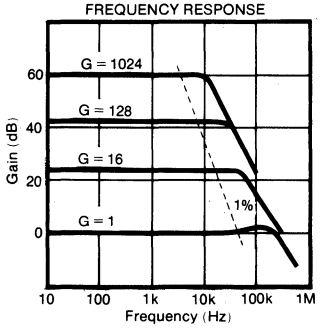
PIN DESIGNATIONS

PIN NO.	DESIG.	FUNCTION	PIN NO.	DESIG.	FUNCTION
1	-V	-15V Analog Supply	17	D_0	Digital Input, LSB
2	-IN	Inverting Input	18	D_1	Digital Input, next LSB
3	J_1	Output of A_3	19	G	Latch
4	(None)	Optional A_4 Offset Trim	20	⏚	Digital Common
5	ΣJ	Summing Junction of A_4	21	D_2	Digital Input, next MSB
6	(None)	Optional A_4 Offset Trim	22	D_3	Digital Input, MSB
7	F	Low-Pass Filter Pin	23	+5	+5 Digital Supply
8	J_2	Input to A_4	24	(None)	No Internal Connection
9	R_1	Output Reference	25	(None)	No Internal Connection
10	O	Output	26	Gain	Optional External Gain
11	S_1	Sense G = 1	27	Gain	Optional External Gain
12	S_2	Sense G = 4	28	(None)	Input CMV
13	S_3	Sense G = 2	29	+IN	Noninverting Input
14	R_2	Output Reference	30	+V	+15V Analog Supply
15	GND	Analog Common	31	BAL	Optional Input Stage
16	(None)	No Internal Connection	32	BAL	Offset Null

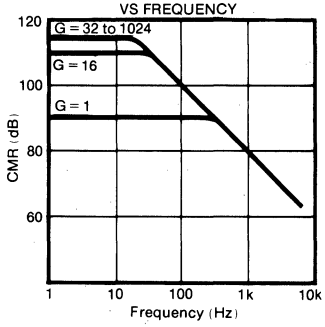
TYPICAL PERFORMANCE CURVES

Typical at +25°C unless otherwise noted.

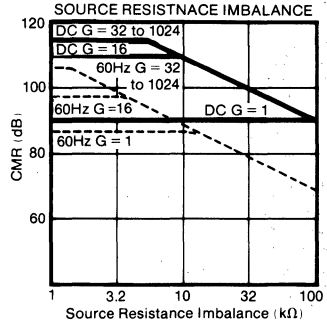
SMALL SIGNAL FREQUENCY RESPONSE



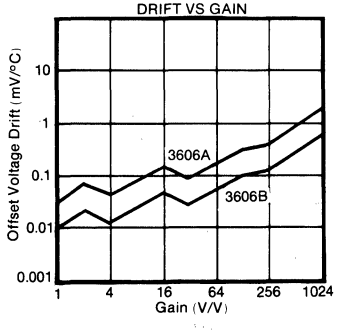
COMMON-MODE REJECTION VS FREQUENCY



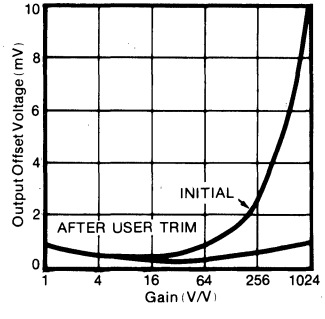
COMMON-MODE REJECTION VS SOURCE RESISTNACE IMBALANCE



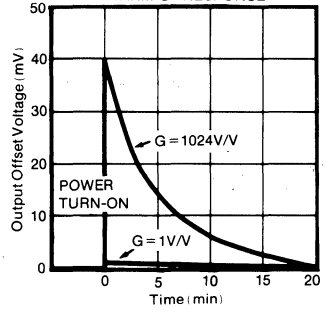
OUTPUT OFFSET VOLTAGE DRIFT VS GAIN



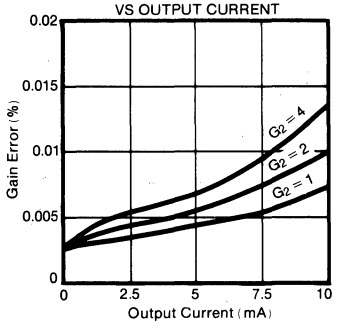
OUTPUT OFFSET VOLTAGE GAIN



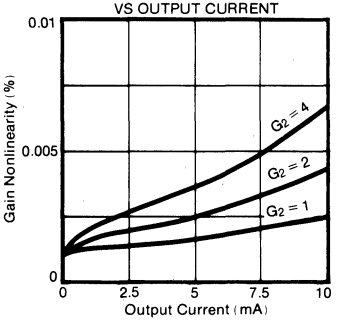
WARM-UP RESPONSE



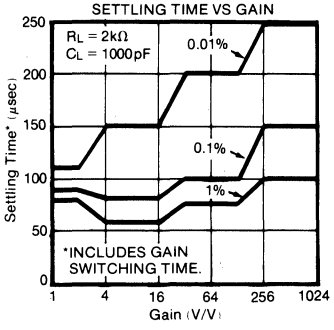
OUTPUT STAGE GAIN ERROR VS OUTPUT CURRENT



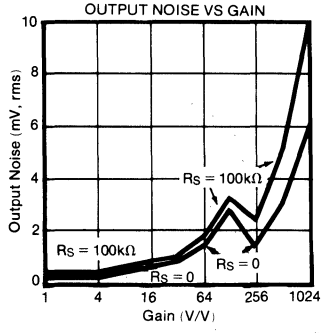
OUTPUT STAGE GAIN NONLINEARITY VS OUTPUT CURRENT



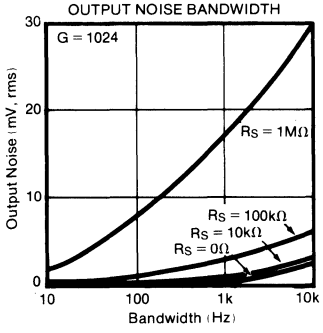
SETTLING TIME VS GAIN



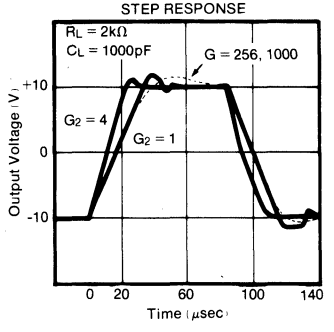
WIDEBAND OUTPUT NOISE VS GAIN



OUTPUT NOISE BANDWIDTH



STEP RESPONSE



INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Figure 2 shows the proper analog and digital power supply connections. The analog supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible. Because the amplifier is direct-coupled it must have a ground return path for the bias currents associated with the amplifier inputs at pins 2 and 29. If the ground return path is not inherent in the signal source (floating source) it must be provided externally. The ground return resistance (R_{GR}) should be kept as low as practical. An upper limit of approximately 50MΩ is established by the input bias currents of the amplifier and its common-mode voltage.

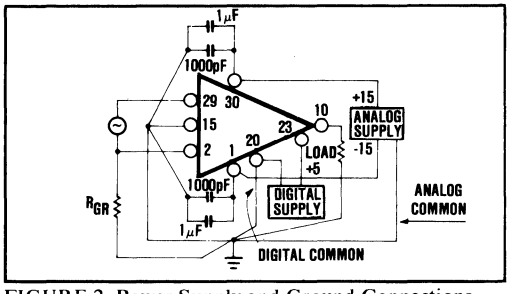


FIGURE 2. Power Supply and Ground Connections.

SIGNAL CONNECTIONS

Basic signal connections are shown in Figure 3. The connection to pin 14 completes the difference amplifier of A_3 (see Figure 1). The 3 to 8 jumper connects the output stage. The pin 9 connection provides a divide-by-two attenuator for the A_4 stage. This is necessary to limit the signal on the output stage switches to maintain signal linearity. The pin 11, 12 and 13 connections to pin 10 close the feedback loop around A_4.

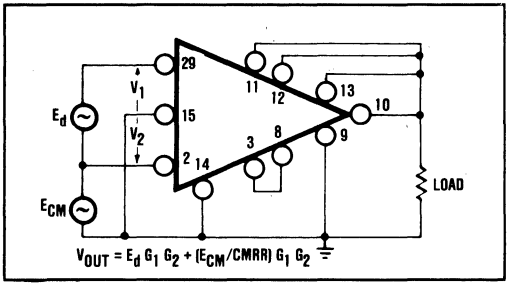


FIGURE 3. Basic Signal Connections.

In the equation shown in Figure 3, G_1 is the input stage gain and G_2 is the output stage gain. CMRR is the common-mode rejection ratio [CMR (in dB) = 20 log CMRR (in V/V)]. Common-mode voltage shown as E_{CM} is actually the average of the two voltages appearing at the two inputs (pins 29 and 2) with respect to pin 15 (V_1 and V_2).

GAIN SETTING

Gain is determined by a 4-bit digital word applied to the input D_0 through D_3 (see Figure 1). Pin 19 provides a latch function for the inputs. When pin 19 is a logic 0, changes on the D_0 through D_3 inputs are inhibited. Pin 19 should be at +5V if the latch is not used.

A gain state truth table is shown in Table I. Gains are determined by the resistor networks shown in Figure 1. For the state D_3, D_2 = 0, 0, the input stage gain is a function of the gain setting resistor R_G connected between pins 26 and 27. If gains of 1, 2 and 4 are desired, no connection should be made to pins 26 and 27 and the resistance across these pins should be kept high with respect to 40kΩ (> 400MΩ).

Gain accuracy is established by laser-trimming the thim-film resistor networks during assembly. No external, user trimming is required.

OUTPUT OFFSET

Output offset may be varied by either of two methods shown in Figure 4. Sources at pin 9 and pin 14 apply voltages to the noninverting inputs of A_4 and A_3 respectively (see Figure 1). Since the output stage gain occurs after these points, the output voltage bias established with V_{R1} and V_{R2} will vary with the output gain, G_2. Sources connected at pins 9 and 14 must have resistances low with respect to 10kΩ in order not to disturb gain accuracy and common-mode rejection.

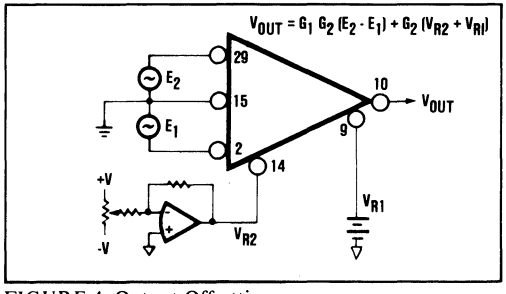


FIGURE 4. Output Offsetting.

LOW-PASS FILTER

For low frequency signals, system performance may be improved by reducing noise bandwidth in the amplifier. This may be accomplished with the addition of one or two external capacitors as shown in Figure 5. C_2 is connected to a 10k/10k attenuator and C_1 is connected as a feedback element across A4 (see Figures 1 and 5). The transfer function is:

$$\frac{V_O}{V_{IN}} = \left[\frac{10 \times 10^3}{100 \times 10^6\, S\,(C_2 + 330 \times 10^{-12}) + 20 \times 10^3}\right]\left[1 + \frac{10 \times 10^3}{10 \times 10^3\, R_1\, SC_1 + R_1}\right]$$

TABLE I. Gain State Truth Table.

Digital Inputs (G_1) D_1	D_2	(G_2) D_1	D_0	G_1 (A_1 and A_2) (Pins 2 & 29 to 3)	G_2 (A_4) (Pin 8 to Pin 10)	$G_1 \cdot G_2$ (R_G* = ∞)	$G_1 \cdot G_2$ (R_G* ≠ ∞)
0	0	0	0	1 + 40k/R_G	1	1	1(1 + 40k/R_G)
0	0	0	1		2	2	2(1 + 40k/R_G)
0	0	1	0		4	4	4(1 + 40k/R_G)
0	0	1	1		4	4	4(1 + 40k/R_G)
0	1	0	0	4	1	4	4
0	1	0	1		2	8	8
0	1	1	0		4	16	16
0	1	1	1		4	16	16
1	0	0	0	32	1	32	32
1	0	0	1		2	64	64
1	0	1	0		4	128	128
1	0	1	1		4	128	128
1	1	0	0	256	1	256	256
1	1	0	1		2	512	512
1	1	1	0		4	1024	1024
1	1	1	1		4	1024	1024

*R_G connected between pins 26 and 27.

The first term is a first order filter. The second term is more complex. R_1 varies with the output stage gain -1.4k for $G_2 = 4$ (see Figure 1). The "1 + ..." nature of the transfer function prevents a true first order filter rolloff.

For most applications, the first order low-pass filter obtained by C_2 provides sufficient filtering. The value C_2 required for a desired cutoff frequency (f_2 in Hz) is obtained by the equation shown in Figure 5.

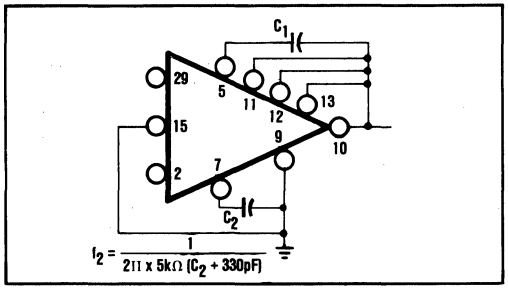


FIGURE 5. Low-Pass Filter Connections.

LARGER OUTPUT CURRENT

The output current rating of the 3606 is a minimum of ±5mA. The linearity of the gain is affected by output current. See Typical Performance Curves. Optimum linearity is achieved with $I_O \leq$ 1mA, $I_O \leq$ 5mA is acceptable. Above 5mA it may be desirable to use a power or current booster as shown in Figure 6. Burr-Brown's 3329 will provide ±100mA output while Burr-Brown's 3553 will supply ±200mA. When either booster is placed inside the feedback loop as shown, the booster's offset voltage produces no significant errors since it is divided by the open-loop gain of the output stage.

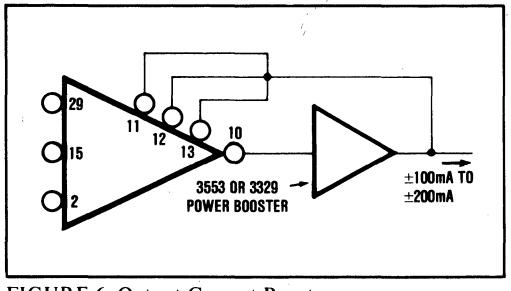


FIGURE 6. Output Current Booster.

GUARD DRIVE CONNECTIONS

Use of the guard drive connection shown in Figure 7 can improve system common-mode rejection when the distributed capacitance of the input lines is significant. The common-mode voltage which appears on the input lines and on pins 29 and 2 is computed by the 3606 [(V_1 + V_2)/2] and appears at pin 28. It is then fed back to the shield so that the voltage across the distributed capacitances is minimized. This reduces the common-mode current and improves common-mode rejection. The operational amplifier in the voltage follower configuration is used to supply more current than can be obtained from the 20k resistors connected internally to pin 28 (see Figure 1).

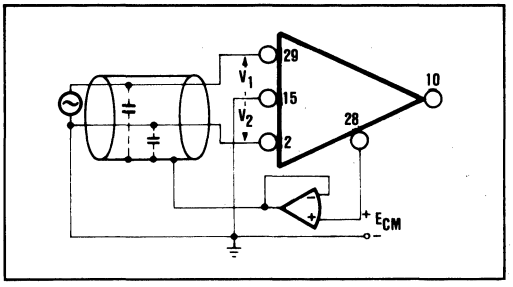


FIGURE 7. Guard Drive Connections.

OFFSET TRIM

Offset voltages of the 3606 are reduced by laser-trimming during assembly. This reduces the initial offset voltage and the offset voltage change with gain change to levels that are acceptable for most applications. For more critical applications the offset voltages can be externally

nulled to zero. The following steps should be followed (see Figure 8).

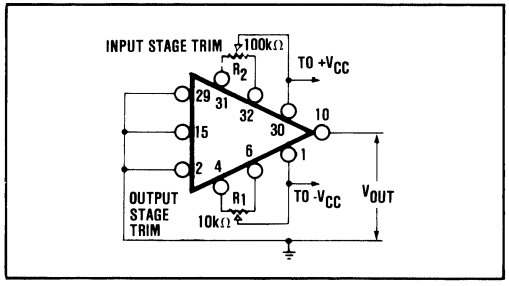


FIGURE 8. Optional Offset Trim.

1. Adjust both R_1 and R_2 to mid-range.
2. Set the gain to minimum (1V/V).
3. Adjust R_1 to make V_{OUT} equal zero.
4. Set the gain to maximum (1024V/V).
5. Adjust R_2 to make V_{OUT} equal zero.

By using this technique, the change in output offset voltage caused by a gain change of 1V/V to 1024V/V may be reduced to, typically 1mV instead of 10mV with no external trimming. Trimming may cause the offset voltage drift vs temperature to increase slightly.

APPLICATIONS

A typical application of 3606 in a microcomputer based data acquisition system is shown in the block diagram below.

The purpose of this system is to be able to acquire data from a specific analog input channel, suitably condition it (amplify it and convert it to digital form) and store it or transmit it for further processing.

Initially the Microcomputer loads the RAM (random access memory) with the required coding for various desired gains via Data Bus. The coding associates the gain state truth table for 3606 with corresponding address locations in the computer memory. So when the computer puts out an instruction to multiplex a specific analog input channel through the multiplexer via the Address Bus, the RAM also receives the same address information and puts out corresponding gain code to the PGIA 3606. The 3606 amplifies the multiplexed signal by the programmed gain value, and outputs it to S/H (sample and hold). The S/H holds the output value when it receives the control signal from the computer and the A/D converts it and outputs it to the computer via the Data Bus under computer control.

The PGIA 3606 allows the system user to modify and reprogram gain values for different analog input channels merely by changing the software computer program. Since different dedicated instruments are not required for various input channels, the PGIA also saves space and overall system costs.

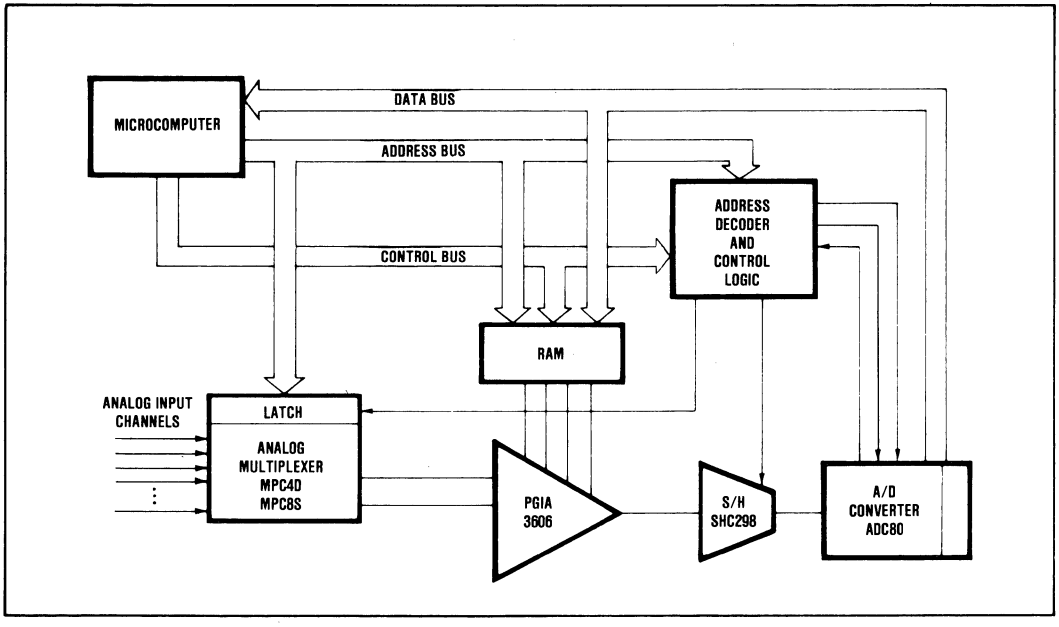


FIGURE 9. Use of 3606 in Data Acquisition System.

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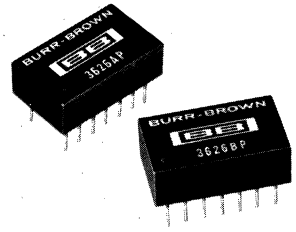

3626

Low Drift INSTRUMENTATION AMPLIFIER

FEATURES

- LOW VOLTAGE DRIFT @ LOW GAIN
  2μV/°C @ G = 5 (3626CP)
- LOW NOISE - 2μV p-p
- HIGH CMR - > 80dB @ = 1000
- LOW COST
- SMALL SIZE - DIP Package

DESCRIPTION

The 3626 is an integrated circuit instrumentation amplifier designed for amplifying low-level signals in the presence of high common-mode voltages. Its low drift, high input impedance ($5 \times 10^9\Omega$), easy gain adjustment (5V/V to 1000V/V) and high common-mode rejection eliminate the problems and compromises associated with using operational amplifiers to realize the same gain function.

Compared to other integrated circuit instrumentation amplifiers it has the unique feature of having low voltage drift versus temperature at low gains.

The 3626 offers many benefits to the user for his instrumentation applications:

Low voltage drift reduces temperature errors

High common-mode rejection preserves system accuracy

High input impedance prevents errors due to source loading and source impedance imbalance

Small, dual-in-line package conserves board space

Laser-trimmed offset requires no nulling

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DISCUSSION

An instrumentation amplifier is basically a closed-loop gain block that exhibits high input impedance and high common-mode rejection. Instrumentation amplifiers are committed devices with differential inputs and accurately predicatable input-to-output relationships – all necessary feedback networks are contained in the circuit package. These characteristics distinguish instrumentation amps from operational amplifiers – open-loop devices whose closed-loop performance depends upon the external networks supplied by the user.

In instrumentation amps parameters such as input and output impedances, frequency response, offset voltage drift and common-mode rejection are specified for the closed-loop, committed configuration. One of the few parameters that the user can vary is gain (by choosing the external gain-setting resistor value). Another important difference between an op amp and instrumentation amp is that the instrumentation amp has no summing junction available; you cannot make a summing amplifier or integrator out of an instrumentation amp.

In the past few years, choices in instrumentation amplifier designs have grown from a number of discrete modular units to include monolithic and hybrid integrated circuit versions which offer high performance at lower cost – and in smaller packages. Monolithic IC's were the first to break the price and performance barrier. Hybrid IC's, such as the 3626, are more expensive than monolithic IC's but they give better performance for the money.

Instrumentation amps normally require at least one external resistor – the gain-setting resistor R_G. Monolithic units usually require two additional – the output feedback resistor and a resistor between feedback common and ground. Since temperature coefficient differences between these two resistors will cause output offset voltage drift, they must be matched to meet the desired drift specification. Hybrid units, such as the 3626, have the advantage that all resistors except the gain-setting R_G can be included in the package.

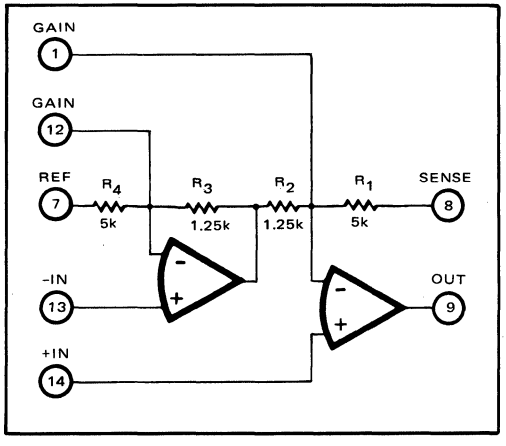


FIGURE 1. Simplified Circuit Diagram.

A simplified circuit diagram of the 3626 is shown in Figure 1. The circuit uses Burr-Brown's high performance bipolar integrated circuit amplifiers and a laser trimmed thin-film resistor network. The excellent initial matching and temperature tracking of these components provide a level of performance difficult to obtain with even expensive discrete amplifiers and resistors. The gain accuracy, linearity and temperature coefficient are particularly attractive.

One of the most outstanding features of the 3626 is its low voltage drift, especially at low and medium gains. Figure 2 shows the drift performance of the 3626 series comapred to monolithic integrated circuit instrumentation amplifiers. The guaranteed voltage drift performance is almost two orders of magnitude better at low gains.

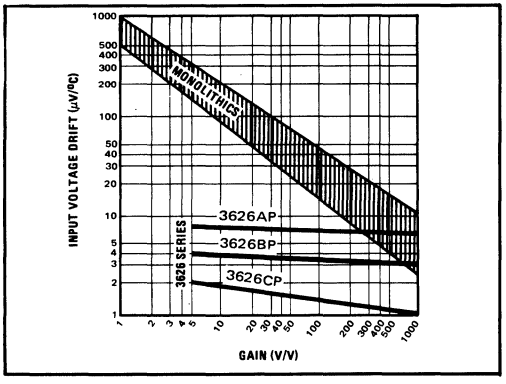


FIGURE 2. Input Offset Drift vs Gain.

The design of the 3626 is such that output biasing is easily accomplished. See Figure 3 for proper connections. The impedance of the reference source should be low compared to 5kΩ. A current booster such as the 3329 (100 mA) or 3553 (200 mA) can conveniently be used with the 3626 to increase its output current driving capability.

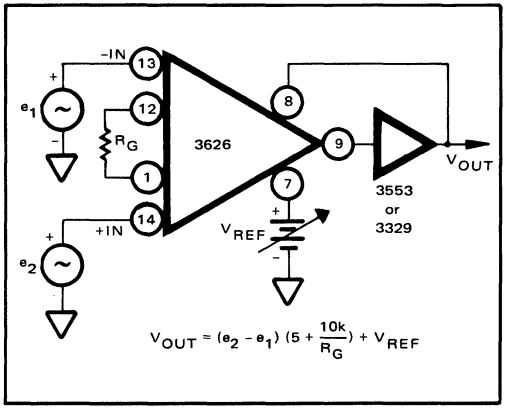


FIGURE 3. Output Offsetting and Power Boosting.

SPECIFICATIONS

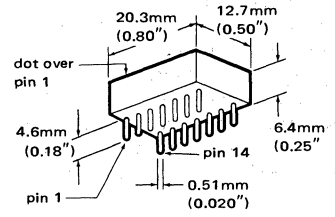
ELECTRICAL

Specifications typical at 25°C and ±15 VDC Power Supply Unless Otherwise Noted.

MODELS	3626AP	3626BP	3626CP
GAIN			
Gain Equation	$G = 5 + \frac{10\ k\Omega}{R_G}$		
Error from Equation (1)	(±0.25 - 0.003G)%		
Range of Gain, min	5 to 1000		
Gain Temp. Coefficient:			
G = 5	2ppm/°C		
G = 10	25ppm/°C		
G = 100	35ppm/°C		
G = 1000	50ppm/°C		
Nonlinearity, max (%) (2)	±(0.02 +0.0003G)	±(0.01 + 0.0003G)	±(0.01 +0.003G)
OUTPUT			
Rated Output, min	±10V @ ±5mA		
Output Impedance, G = 100	2Ω		
INPUT			
Input Impedance, Diff. & CM	$5 \times 10^9\ \Omega \parallel 3$ pF		
Input Voltage Range, min			
Differential	±10V		
Common-mode	±6V		
CMR, DC to 60Hz	with 1kΩ source unbalance		
G = 5, min	68dB	74dB	74dB
G = 10 to 1000, min	74dB	80dB	80dB
INPUT OFFSET VOLTAGE			
Initial Offset, max (1)	$\pm(0.4 + \frac{0.4}{G})$mV	$\pm(0.2 + \frac{0.2}{G})$mV	$\pm(0.2 + \frac{0.2}{G})$mV
vs. Temperature, max	$\pm(6 + \frac{10}{G})\mu$V/°C	$\pm(3 + \frac{5}{G})\mu$V/°C	$\pm(1 + \frac{5}{G})\mu$V/°C
vs. Supply	40μV/V		
vs. Time	3μV/mo.		
INPUT BIAS CURRENTS			
Initial Bias Current, max	±50nA (either input)		
vs. Temperature, max	±0.7nA/°C		
vs. Supply	±0.1nA/V		
INPUT NOISE			
Voltage, p-p, 0.01Hz–10Hz	2μVp-p		
RMS, 10Hz - 10kHz	2μV RMS		
Current, p-p, 0.01Hz - 10Hz	150 pA p-p		
RMS, 10Hz - 10kHz	50 pA RMS		
DYNAMIC RESPONSE			
Small Signal, ±3dB Flatness:			
G = 5	400kHz		
G = 10	160kHz		
G = 100	14kHz		
G = 1000	1.4kHz		
Small Signal, ±1% Flatness;			
G = 5	76kHz		
G = 10	27kHz		
G = 100	2.1 kHz		
G = 1000	250 Hz		
Full Power, G = 5 - 100	19 kHz		
Slew Rate, G = 5 - 100	1.2 V/μs		
Settling Time (0.1%):			
G = 5	0.02 ms		
G = 10	0.03 ms		
G = 100	0.1 ms		
G = 1000	12 ms		
POWER SUPPLY			
Rated Voltage	±15 VDC		
Voltage Range	±5 to ±20 VDC		
Quiescent Supply Current	±6 mA, max		
TEMPERATURE RANGE			
Specifications, min	-25°C to +85°C		
Operation	-55°C to +125°C		
Storage	-65°C to +150°C		

(1) May be trimmed to zero.
(2) Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.

MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 0145MC (14-pin DIP)

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

Pin Connections

1.	Gain	8.	Sense
2.	} No Internal	9.	Out
3.	} Connection	10.	$+V_{CC}$
4.	V_{OS}	11.	No Internal Connection
5.	V_{OS}	12.	Gain
6.	$-V_{CC}$	13.	-In
7.	Ref	14.	+In

Connection Diagram

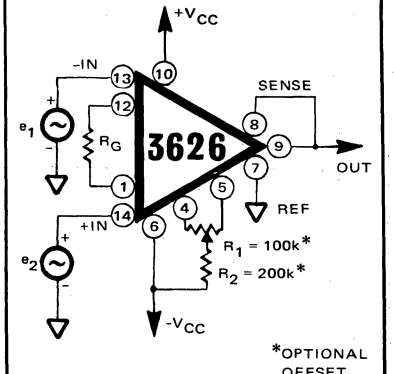
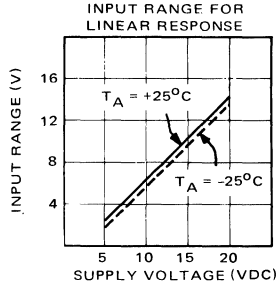
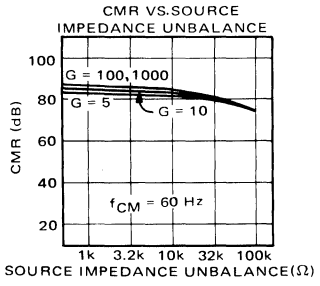


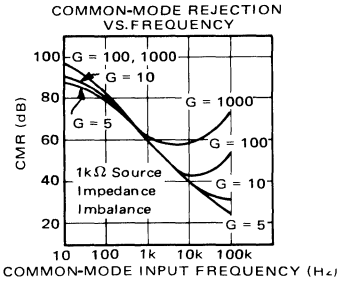
FIGURE 4

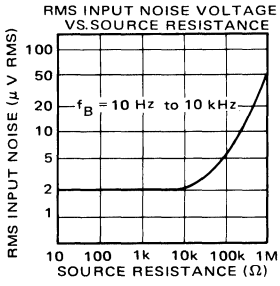
TYPICAL PERFORMANCE CURVES

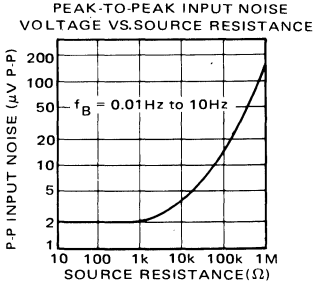
(TYPICAL @ 25°C and ±15 VDC POWER SUPPLIES UNLESS OTHERWISE NOTED)

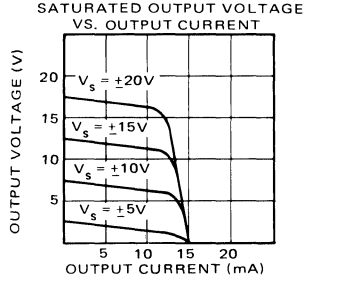


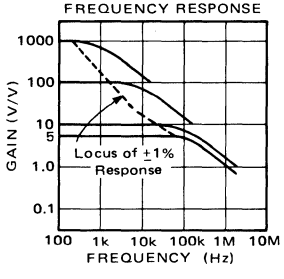


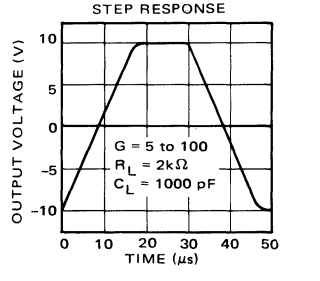


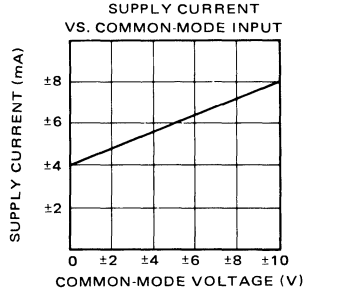












INSTALLATION AND OPERATING INSTRUCTIONS

SETTING THE GAIN

Figure 3 shows the normal operating connections for the 3626. The differential gain, G, is determined according to the equation

$$G = 5 + \frac{10k\Omega}{R_G}$$

where R_G is the resistor shown in Figure 4. This gain equation is typically accurate to 0.25%. The temperature coefficient of R_G will directly affect the stability of G. For high gains, R_G will be quite small (R_G = 10Ω for G = 1000); thus, the wiring impedance between pins 12 and 1 should be kept as low as possible. (Trimming of R_G will eliminate the effects of wiring impedances so long as this impedance is constant.) Also, note that V_{ref} source needs to be low impedance so as not to significantly affect the gain equation.

CMR TRIM

The 3626 meets its CMR specifications without additional trimming; however, for improved CMR in special situations (such as imbalanced source impedances), the circuit in Figure 5 may be used. In this circuit, R_1 is added to intentionally imbalance the inverting and noninverting gains of the amplifier. R_2 is then used to rebalance them, which overcomes the effects of any residual CMR degradation due to source impedance imbalance, etc. An improvement of approximately 6 to 10 dB can be typically realized at low gains.

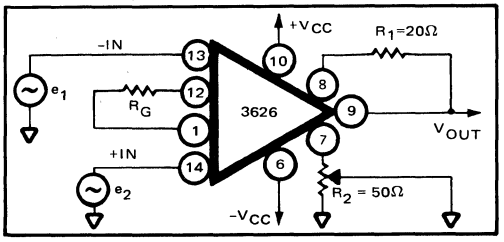
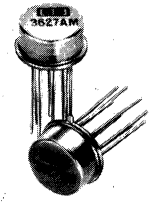


FIGURE 5. CMR Trim.

BURR-BROWN®

3627



High Accuracy Unity-Gain DIFFERENTIAL AMPLIFIER

FEATURES

- LOW COST
- EASY TO USE
- COMPLETELY SELF-CONTAINED
- HIGH ACCURACY
  - Gain Error, 0.005%
  - Nonlinearity, 0.0005%
  - CMR, 106dB
- NO TRIMMING REQUIRED

DESCRIPTION

The 3627 is a high accuracy committed-gain differential amplifier. It consists of a high quality monolithic operation amplifier, a low drift thin-film resistor network and laser-trimmed offset circuitry - all inside a single integrated circuit package.

The fact that the 3627 is completely self-contained in a TO-99 package has several user benefits:

The total performance is guaranteed as a single component.

No gain adjustments are required.

No offset trimming is required.

The whole circuit, including the gain setting resistors and offset trim circuitry, is protected by the environmentally rugged hermetically sealed package.

The total amplifier function is very small in size (0.108 square inches of area and 0.025 cubic inches of volume).

The 3627 is offered in two grades: the 3627AM and the 3627BM. They differ only in common-mode rejection (94dB typ. vs 106dB typ.) and offset voltage drift (15μV/°C typ. vs 10μV/°C typ.).

The 3627 offers excellent total performance with no fuss and a very-low total installed cost.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DISCUSSION

The 3627 is a new and unique approach to a widely occurring problem-how to get excellent performance at a low cost in a unity gain differential amplifier circuit. Burr-Brown's solution to this problem uses its wide range of integrated circuit expertise; a high quality monolithic amplifier, low drift high stability thin-film resistor network and state-of-the-art laser-trimming techniques. The result is a completely self-contained amplifier with total guaranteed 25°C accuracy of less than ±0.015% (gain error, nonlinearity, offsets and common-mode rejection).

The simplicity of the unity gain differential amplifier circuit may be deceiving when one considers an error analysis. Consider, for example, gain and common-mode rejection errors. The gain is determined by the ratio of R1 and R2 and the ratio of R3 and R4. The common-mode rejection of the total circuit is a function of the CMR of the operational amplifier and the matching of the resistors R1 to R3 and R2 to R4. Even if the operational amplifier is perfect (infinite CMR), in order to guarantee 100dB common-mode rejection would require resistor match of approximately 0.0005% (5ppm).

This matching (and especially maintaining the match over temperature) can be difficult and expensive to achieve. Packaged matched and tracking resistor networks are available but they are fairly expensive compared to the cost of the complete 3627 amplifier. Of course, matching can be obtained by trimming or padding some of the resistors, but this is difficult to do since each resistor effects both gain accuracy and common-mode rejection simultaneously. Unless care is used in choosing the trimming sequence a frustrating iterative trimming process can be encountered.

With the 3627 these problems no longer exist for the user. They are solved inside the package by Burr-Brown and the user has a completely self-contained plug-in-and-go amplifier to use. The excellent gain accuracy and common-mode rejection is obtained by using laser-trimming of a thin-film resistor network (R1 through R4). The outstanding gain and common-mode rejection temperature coefficients are a result of the excellent TCR tracking properties inherent in Burr-Brown's thin-film resistor networks.

The offset voltage is also laser-trimmed to a very low 250μV max value (100μV typical). This low value of offset eliminates the need for external offset adjust potentiometers which reduces cost and improves reliability.

The basic approach of the 3627 as a completely self-contained amplifier has several cost saving implications. It reduces design, purchasing and inventory cost. It reduces labor costs because the gain setting resistors do not require installation and adjustment. Also, no potentiometers are required.

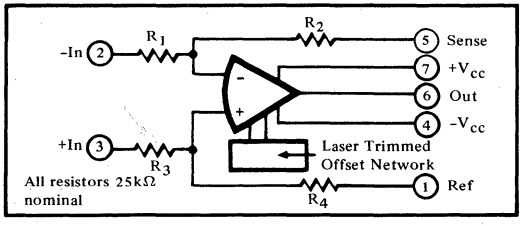
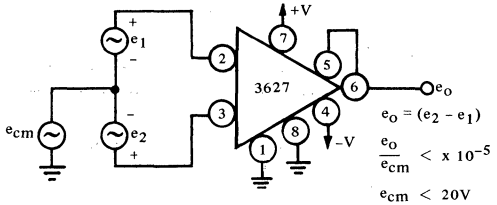
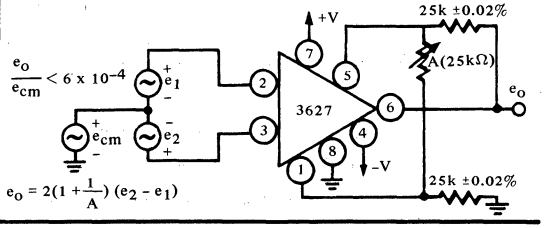


FIGURE 1. Simplified Circuit Diagram.

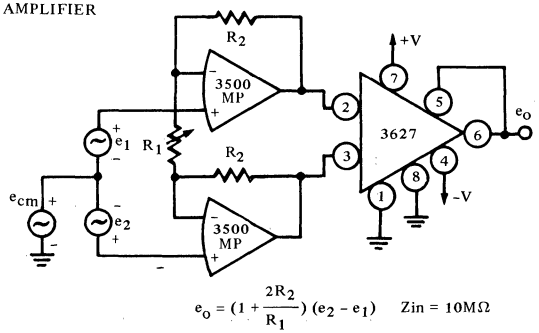
UNITY GAIN DIFFERENCE AMPLIFIER



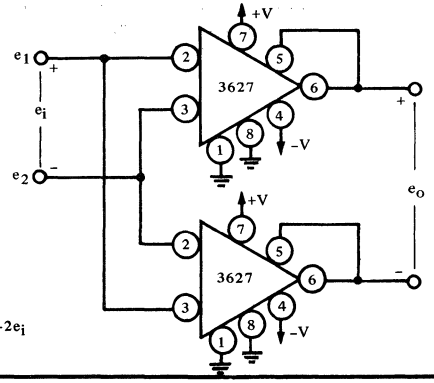
VARIABLE GAIN DIFFERENTIAL AMPLIFIER



HIGH INPUT IMPEDANCE, VARIABLE GAIN, INSTRUMENTATION AMPLIFIER



DIFFERENTIAL IN - DIFFERENTIAL OUT AMPLIFIER



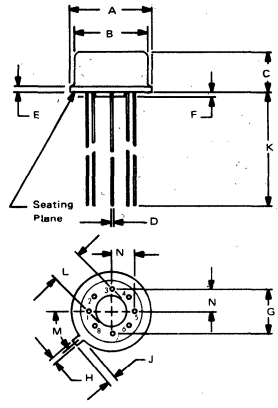
ELECTRICAL SPECIFICATIONS

Specifications typical at 25°C and ±15VDC power supply unless otherwise noticed.

MODELS	3627AM	3627BM
GAIN		
Gain Equation	G = 1V/V[1]	
Gain Error	±0.01%, max (±0.005% typ)	
Gain Nonlinearity[2]	±0.001%, max (±0.0005% typ)	
Gain Temp. Coefficient, max	±0.0005%/°C (5ppm/°C)	
Gain Temp. Coefficient, typ	±0.0002%/°C (2ppm/°C)	
OUTPUT		
Rated Output, min	±10V at ±5mA	
Rated Output, typ	±12V at ±10mA	
Output Impedance	0.01Ω	
INPUT		
Input Impedance		
Differential	50kΩ	
Common-mode	50kΩ	
Input Voltage Range, Linear Operation		
Differential	±10V	
Common-mode	±20V	
Common-mode Rejection, DC to 60Hz		
CMR, at 25°C	90dB, min (94dB, typ)	100dB, min (106dB, typ)
CMR, -25°C to +85°C	80dB, min (90dB, typ)	86dB, min (94dB, typ)
OFFSET AND NOISE		
Offset Voltage, RTO[4][5]		
at 25°C	250μV (100μV, typ)	
vs Temperature, μV/°C	30, max (15, typ)	20, max (10, typ)
vs Supply	20μV/V	
vs Time	20μV/mo	
Noise Voltage, RTO[4][6]		
0.01Hz to 10Hz	2μV, p-p	
10Hz to 100Hz	1.5μV, rms	
DYNAMIC RESPONSE		
Small Signal, ±1% Flatness	5kHz min (8kHz, typ)	
Small Signal, ±3dB Flatness	0.8MHz min (1.2MHz, typ)	
Full Power Bandwidth	14kHz min (18kHz, typ)	
Slew Rate	0.6V/μs min (1V/μs, typ)	
Settling Time, 0.1% (±10mV)	20μsec	
Settling Time, 0.01% (±1mV)	50μsec	
POWER SUPPLY		
Rated Voltage	±15VDC	
Voltage Range	±5VDC to ±18VDC	
Quiescent Supply Current	±2mA	
TEMPERATURE RANGE		
Specifications, min	-25°C to +85°C	
Operation	-55°C to ±125°C	
Storage	C to +150°C	

1. Connected as unity-gain amplifier. Several other configurations ar possible. See the figures in Discussion and Typical Applications.
2. Nonlinearity is the maximum peak deviation from the best straightline as a percent of full scale peak-to-peak output.
3. With zero source impedance unbalance.
4. Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifiers offset voltage and noise voltage.
5. Includes effects of amplifiers' input bias currents.
6. Includes effects of amplifiers' input current noise.

MECHANICAL

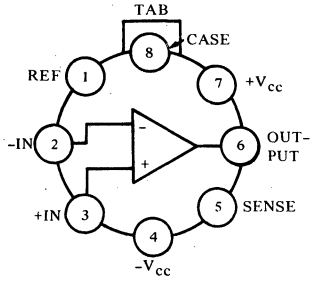


NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

CONNECTION DIAGRAM

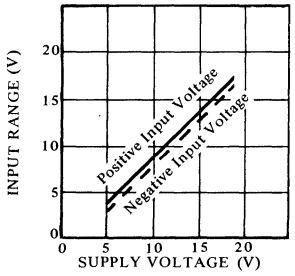


See Figure 1 for circuit diagrams.

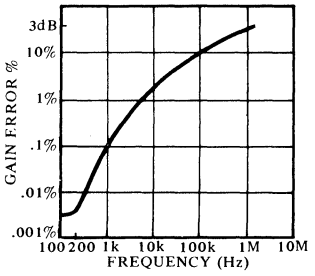
TYPICAL PERFORMANCE CURVES

(Typical at 25°C and ±15 VDC Power Supplies unless otherwise noted.)

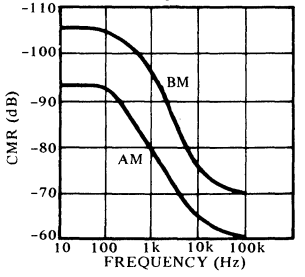
INPUT RANGE FOR LINEAR RESPONSE



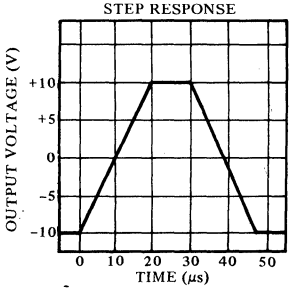
GAIN ERROR VS FREQUENCY



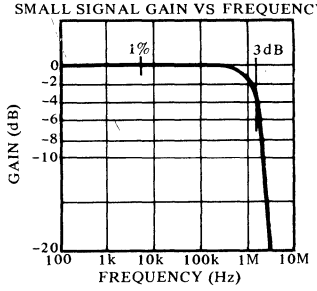
COMMON-MODE REJECTION VS FREQUENCY



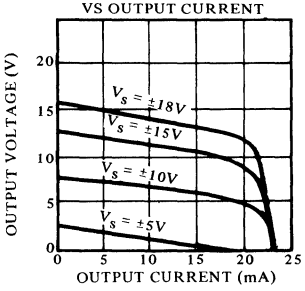
STEP RESPONSE



SMALL SIGNAL GAIN VS FREQUENCY

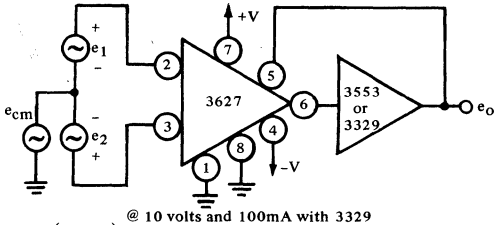


MAXIMUM OUTPUT VOLTAGE VS OUTPUT CURRENT



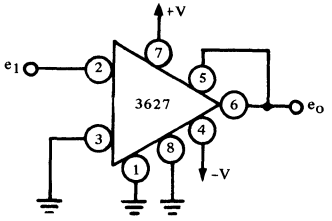
TYPICAL APPLICATIONS

HIGH POWER DIFFERENTIAL AMPLIFIER



$e_o = (e_2 - e_1)$ @ 10 volts and 100mA with 3329
@ 10 volts and 200mA with 3553

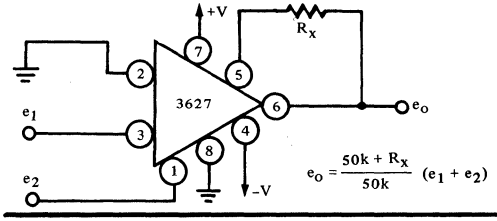
HIGH ACCURACY, LOW DRIFT, LOW OFFSET-UNIT GAIN INVERTER



$e_o = -e_1$

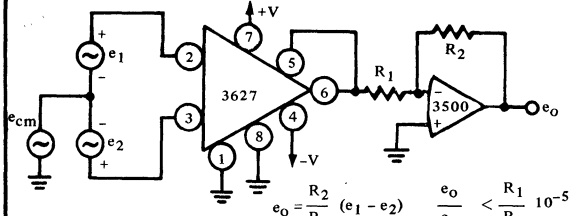
Accuracy .01%
Linearity .001%
Offset < 250μV at output
Offset Drift < 20μV/°C at output

NON-INVERTING SUMMER



$e_o = \frac{50k + R_X}{50k} (e_1 + e_2)$

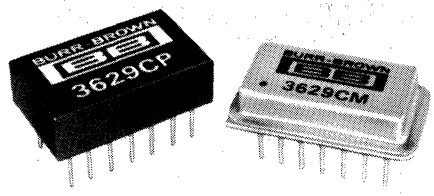
HIGHER GAIN DIFFERENCE AMPLIFIER



$e_o = \frac{R_2}{R_1} (e_1 - e_2)$ $\frac{e_o}{e_{cm}} < \frac{R_1}{R_2} 10^{-5}$

BURR-BROWN®

3629



Low Drift INSTRUMENTATION AMPLIFIER

FEATURES

- VERY-LOW VOLTAGE DRIFT 0.75μV/°C
- HIGH CMR - 90dB @ 60Hz
- LOW BIAS CURRENT - 20nA
- LOW NOISE - 1.2μV p-p
- SMALL SIZE - DIP Package

DESCRIPTION

Offering very-low voltage drift versus temperature even at low gains, the 3629 meets critical instrumentation requirements when amplifying low level signals in the presence of high common-mode voltages. This precision integrated circuit instrumentation amplifier offers low bias current and high input impedance ($10^{10}\Omega$). A single resistor sets gain from 5V/V to 1000V/V.

The 3629 exceeds the performance of other IC instrumentation amplifiers and offers many benefits for instrumentation applications:

Low voltage drift to reduce temperature errors
High common-mode rejection to preserve system accuracy
High input impedance to minimize errors caused by source loading and source impedance imbalance
Small, dual-in-line plastic or hermetically sealed metal package to conserve board space
Laser-trimmed offset to eliminate nulling

Use the 3629 to eliminate problems and compromises that arise when attempting to use operational amplifiers to achieve the same gain function.

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DISCUSSION

Instrumentation amplifiers are closed loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high input impedances.

Figure 1 represents a simplified circuit diagram of the 3629. The circuit employs high performance bipolar IC amps and a laser trimmed thin-film resistor network.

The 3629 offers excellent performance. Its low voltage drift reduces temperature errors, especially at low and medium gains. Figure 2 illustrates the drift performance of the 3629 compared with competitive monolithic IC instrumentation amplifiers. Note that the drift does not increase at lower gains. Compare the 3629's input offset voltage drift vs temp at 1.75μV/°C with monolithic IC instrumentation amps in the range of 100μV/°C.

Because of its design, output biasing of the 3629 is easily accomplished. See Figure 3 for connections. The impedance of the reference source should be low compared to 10kΩ. Figure 3 also shows a current booster, such as Burr-Brown's 3329 (100mA) or 3553 (200mA), used with the 3629 to increase its output current driving capability while retaining its 5-1000 V/V gain characteristics. If power boosting is not required, connect pin 8 to pin 9.

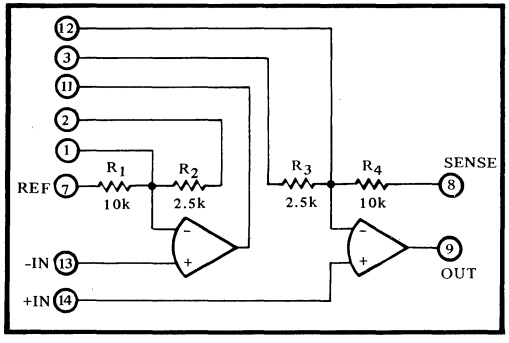


FIGURE 1. Simplified Circuit Diagram.

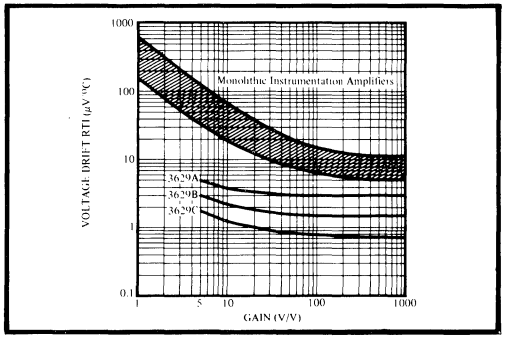


FIGURE 2. Input Offset Drift vs Gain.

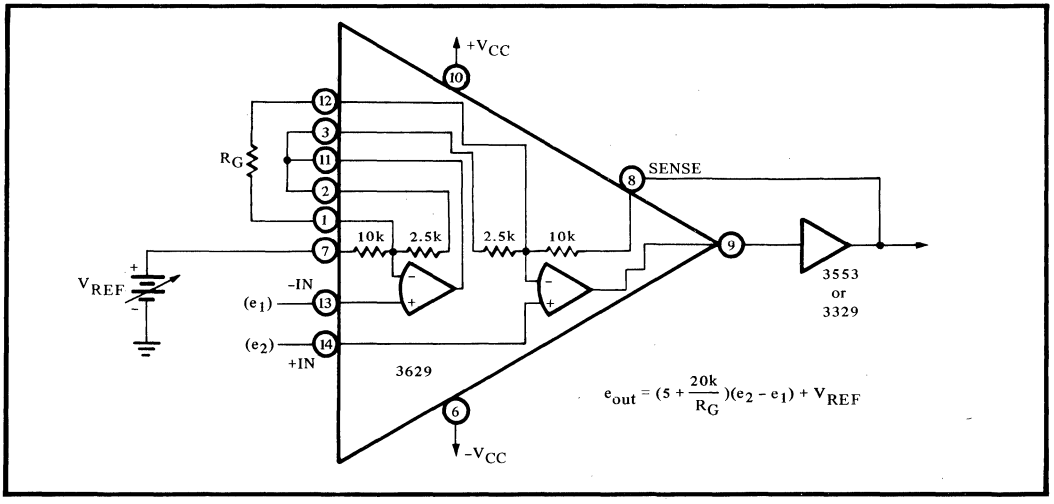


FIGURE 3. Output Biasing and Power Boosting.

DESIGN VERSATILITY

The 3629 offers additional application versatility. Its matched pair of amplifiers can be used as two independent, uncommitted op amps with a laser trimmed thin-film network present in one package.

When amplification must be extended to gains below 5, a 3629 used with a unity gain instrumentation amplifier (Burr-Brown's 3627) is recommended. This connection is shown in Figure 4.

DESIGN ALTERNATIVES

To amplify signals in the presence of common-mode voltages and noise while maintaining high input impedance, you can: 1) design and build an op amp circuit with a differential input configuration; 2) design and build an instrumentation amplifier made up of multiple op amps or; 3) purchase a ready-to-install, committed instrumentation amplifier. Only the third option provides an immediate solution with the elimination of in-house design, assembly and tuning steps. The growing range of lower cost, high quality IC instrumentation amps available has answered the build or buy question.

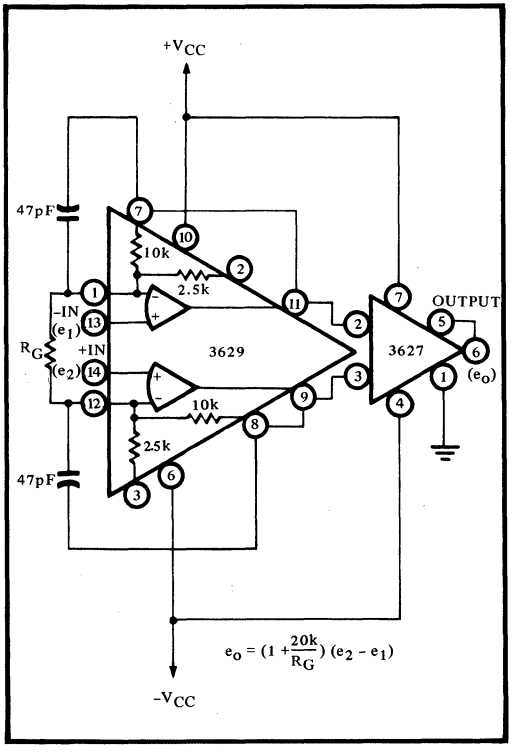


FIGURE 4. 3629 In A Composite Instrumentation Amplifier.

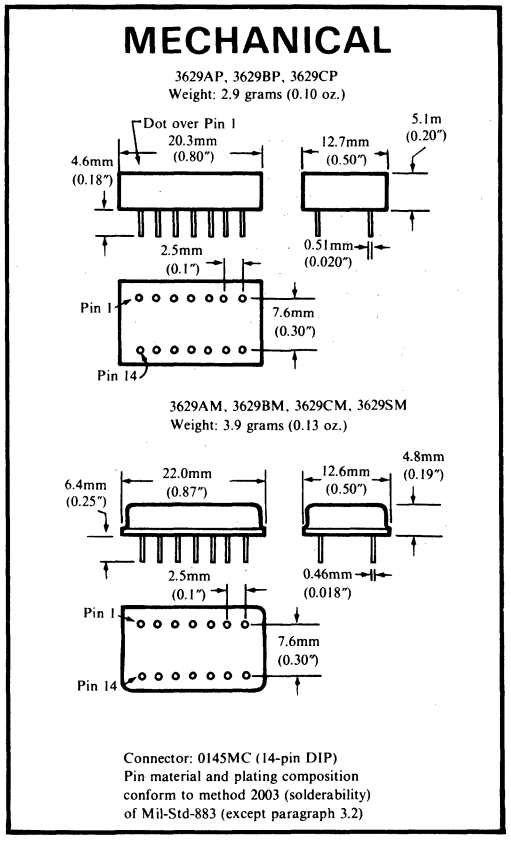


FIGURE 5. Mechanical Specifications

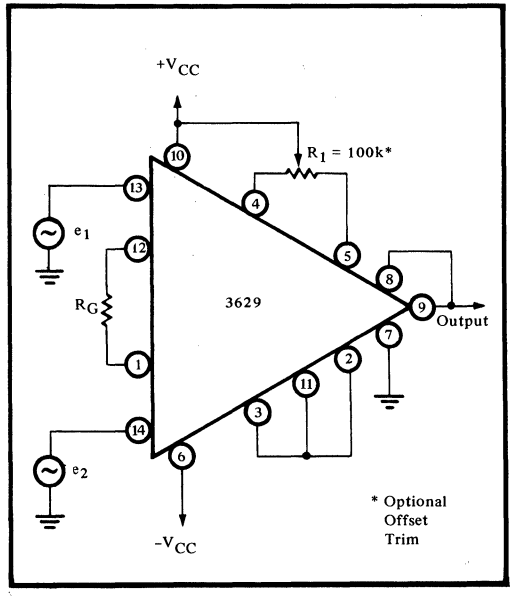


FIGURE 6. Connection Diagram

ELECTRICAL SPECIFICATIONS

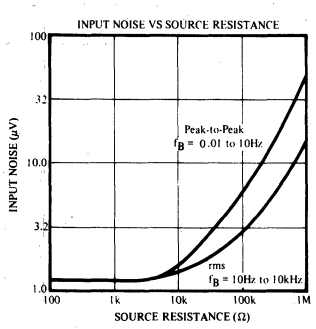
Specifications typical at 25°C with ±15VDC power supply unless otherwise noted.

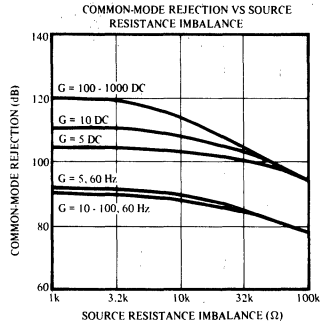
MODEL	3629AP, 3629AM			3629BP, 3629BM, 3629SM			3629CP, 3629CM			UNITS
	min	typ	max	min	typ	max	min	typ	max	
GAIN										
Range of Gain	5		1000	•		•	•		•	V/V
Gain Equation		G = 5 + 20k/R_G			•			•		V/V
Error From Equation, DC			(1)			•			•	
Gain Temp. Coefficient										
G = 5		2	5		•	•		•	•	ppm/°C
G = 10		12	25		•	•		•	•	ppm/°C
G = 100		20	45		•	•		•	•	ppm/°C
G = 1000		25	50		•	•		•	•	ppm/°C
Nonlinearity, DC		±(0.002 + 10^{-4}G)	±(0.005 + 2 x 10^{-4}G)		±(0.001 +10^{-4}G)	±(0.003 + 10^{-4}G)		±(0.001 + 10^{-4}G)	±(0.003 + 10^{-4}G)	% p-p FS
RATED OUTPUT										
Voltage	±10	±12.5		•	•		•	•		V
Current	±10	±12.5		•	•		•	•		mA
Output Impedance G = 100		0.01			•			•		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at 25°C		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	μV
vs. Temp.			±3 ±10/G			±1.5 ±7.5/G			±0.75 ±5/G	μV/°C
vs. Supply		5	10		•	•		•	•	μV/V
vs. Time		±0.4			•			•		μV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input)		±15	±35		±10	±25		±5	±20	nA
vs. Temp.		±0.30	±0.60		•	•		•	•	nA/°C
vs. Supply		±0.1	±0.2		•	•		•	•	nA/V
Initial Offset Current		±15	±50		±10	±30		±5	±20	nA
vs. Temp.		±0.6	±1.2		•	•		•	•	nA/°C
INPUT IMPEDANCE										
Differential		10 ‖ 3			•			•		GΩ‖pF
Common-mode		10 ‖ 3			•			•		GΩ‖pF
INPUT VOLTAGE RANGE										
Differential	±10			•			•			V
Common-mode	±6			•			•			V
CMR w/ 1kΩ Source Imbalance										
DC, G = 5	100	104		•	•		•	•		dB
, G = 10	106	110		•	•		•	•		dB
, G = 100 to 1000	110	120		•	•		•	•		dB
60 Hz All Gains	90	92		•	•		•	•		dB
INPUT NOISE										
Voltage, p-p, 0.01Hz - 10Hz		1.2			•			•		μV p-p
rms, 10Hz - 1.0 kHz		1.0			•			•		μV rms
Current, p-p, 0.01Hz - 10Hz		70			•			•		pA p-p
rms, 10Hz - 1.0kHz		20			•			•		pA rms
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness,										
G = 5		90			•			•		kHz
G = 10		60			•			•		kHz
G = 100		30			•			•		kHz
G = 1000		3.5			•			•		kHz
Small Signal, ±1% Flatness,										
G = 5		7.2			•			•		kHz
G = 10		3.8			•			•		kHz
G = 100		0.33			•			•		kHz
G = 1000		30			•			•		Hz
Full Power, G = 5 - 100		7.5			•			•		kHz
Slew Rate, G = 5 - 100	0.2	0.45		•	•		•	•		V/μsec
Settling Time (0.1%)										
G = 5		35			•			•		μsec
G = 100		85			•			•		μsec
G = 1000		350			•			•		μsec
Settling Time (.01%)										
G = 5		40			•			•		μsec
G = 100		120			•			•		μsec
G = 1000		400			•			•		μsec
POWER SUPPLY										
Rated Voltage		±15			•			•		V
Voltage Range	±5		±20	•		•	•		•	V
Current, Quiescent		±5	±7		•	•		•	•	mA
TEMPERATURE RANGE										
Specification [2]	-25		+85	•		•	•		•	°C
Operation	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C

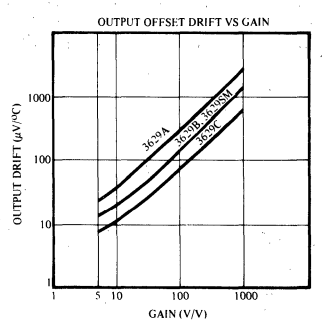
* Specifications same as for 3629AP/AM. (1) See Typical Performance Curves. (2) -55°C to +125°C for 3629SM.

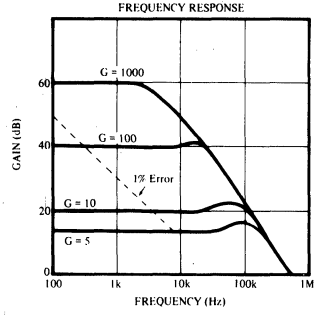
TABLE I.

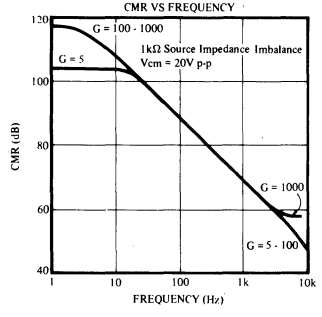
TYPICAL PERFORMANCE CURVES

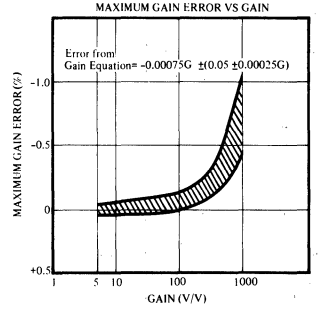


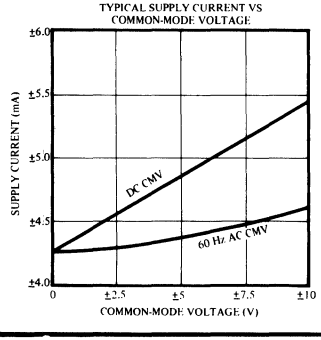


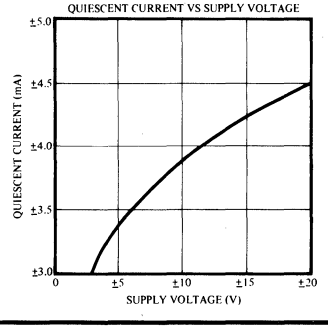


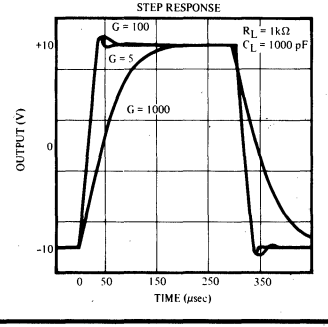












INSTALLATION AND OPERATING INSTRUCTIONS

OFFSET VOLTAGE ADJUSTMENT

Initial offset of the 3629 is trimmed to a very low value during production. In most applications further nulling will not be required. If it is necessary to null offset to the lowest possible value, a low cost single turn potentiometer can be connected between pins 4 and 5 as shown in Figure 6. Drift changes 0.33μV/°C for each 100μV of offset voltage nulled. Due to second order effects, the point of minimum offset drift does not occur at the point of zero offset voltage in approximately 25% of the cases. In these instances nulling the offset voltage may cause a slight increase in voltage drift.

A following stage should be used if large system offsets must be nulled. This method results in the lowest possible drift. In the circuit shown in Figure 7, the offset component of V_{OUT} due to V_1 is V_1R_2/R_1. Resistors R_1 through R_4 are selected to provide system scaling and to make the offset component of V_{OUT} due to V_2 cancel the component of V_{OUT} due to V_1.

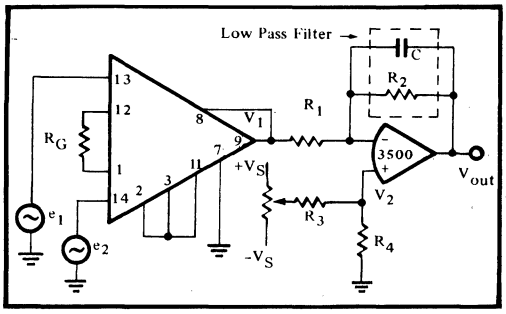


FIGURE 7. Multi-stage Amplifier For Offset Null and High Frequency Filtering.

NOISE

The 3629 offers very low noise at low and mid-frequencies. See specifications and performance curves. At frequencies above 100kHz, noise increases and may cause errors if the following circuitry responds to higher frequencies. When high frequency noise must be reduced, a low pass filter should be installed in a stage following the 3629. Figures 7 and 8 illustrate two high frequency filtering approaches.

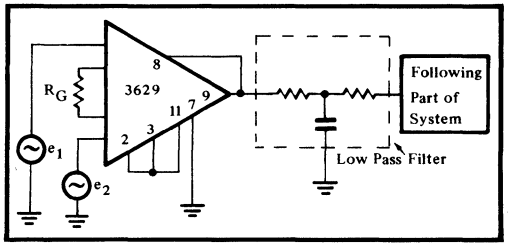


FIGURE 8. High Frequency Filter For Single Stage Amplifier.

APPLICATIONS

TRANSDUCER APPLICATION

A bridge transducer, Figure 9, with a 0 to 0.1V output requires amplification to interface with a 0 to 10V range system. The bridge introduces a 100Ω source imbalance and 0.25V of 60Hz noise is present on the ground return. Operating temperature range is 10°C to 50°C.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources are tabulated in Table II as a % of Full Scale.

	Absolute Error		Resolution Error	
	Max	Typ	Max	Typ
Gain Nonlinearity	0.004%	0.002%	0.004%	0.002%
CMR	0.008%	0.0063%	0.008%	0.0063%
Noise 0.1 to 100Hz	0.0012%	0.0012%	0.0012%	0.0012%
Voltage Offset Drift	0.032%	0.020%		
Offset Current Drift	0.0048%	0.0024%		
Gain Drift	0.20%	0.08%		
TOTAL	0.230%	0.1119%	0.0132%	0.0095%

TABLE II. Transducer Application Error Analysis.

The 3629 Instrumentation Amplifier is, therefore, capable of 1/2LSB resolution in a 12 bit system over a 10°C to 50°C range and will produce 8 bit accuracy over the full temperature range.

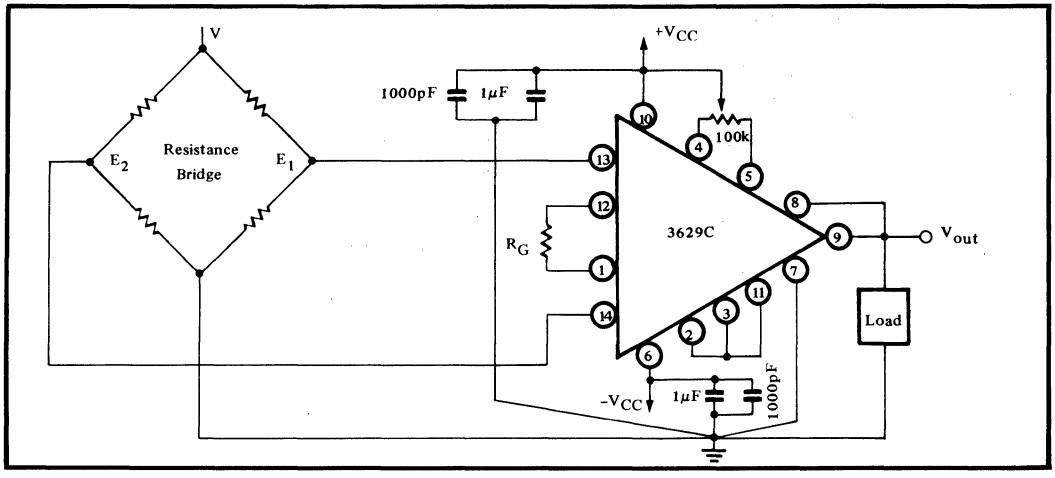


FIGURE 9. 3629 Used In A Transducer Application.

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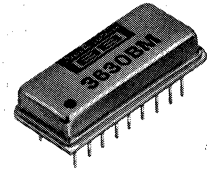
3630



Very High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- ULTRA LOW VOLTAGE DRIFT - 0.25µV/°C
- LOW BIAS CURRENT - 20nA
- LOW NOISE - 1.2µV p-p
- HIGH INPUT IMPEDANCE - 10 x $10^9\Omega$
- HIGH CMR - 106dB @ 60Hz
- LOW OFFSET VOLTAGE - 25µV
- LOW NONLINEARITY - 0.002%

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:

  Strain Gages
  Thermocouples
  RTDs
- REMOTE TRANSDUCERS
- LOW LEVEL SIGNALS

DESCRIPTION

The 3630 is a high accuracy, multi-stage, integrated circuit instrumentation amplifier designed for signal conditioning requirements where very high performance is desired.

A multi-stage design is used to provide excellent specifications and maximum versatility at reasonable cost. The input stage uses Burr-Brown's ultra-low drift low noise monolithic operational amplifiers to provide outstanding input characteristics.

All resistors are on a single network of Nichrome deposited on silicon. This provides high initial accuracy low TCR (temperature coefficient of resistance) and TCR matching, and outstanding stability as a function of time.

State-of-the-art laser-trimming techniques are used for reduction of offset voltage, offset voltage drift versus temperature, and for maximizing common-mode rejection.

In addition to providing an outstanding set of specifications, the 3630 offers convenience and ease of use in providing the following features: single capacitor active low pass filtering; easy output biasing (zero suppression and elevation); common-mode voltage generation for active guard drive; conveniently increased output current capability.

The unit is packaged in an 18-pin metal hermetic dual-in-line package which provides shielding, ease of installation, and environmental ruggedness.

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DISCUSSION

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are closed loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open loop, uncommitted device that requires external networks to close the loop. While op amps can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using op amps often leads to design trade-offs when it is necessary to amplify low-level signals in the presence of common-mode voltages while maintaining high input impedances.

THE 3630

A simplified schematic of the 3630 is shown in Figure 1. It is a three-stage device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found on integrated circuit instrumentation amplifiers.

The input stage (A1 and A2) consists of two of Burr-Brown's premium grade high accuracy bipolar operational amplifiers. They are connected in the noninverting configuration to provide the high input impedance (10 x $10^9\Omega$) desirable in the instrumentation amplifier function. The inherent low offset voltage and low offset voltage drift versus temperature of these amplifiers is improved even further by the state-of-the-art laser-trimming techniques.

The second stage (A3) consists of a high quality operational amplifier connected in a unity gain difference amplifier configuration. A critical part of this stage is the matching of the four 10k ohm resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to maintain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the resistors shown in Figure 1 are part of a single thin-film network of Nichrome deposited on a passivated silicon substrate. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. The single network approach provides the excellent TCR (temperature coefficient of resistance) and TCR tracking desirable to provide gain accuracy and common-mode rejection when the 3630 is operated over wide temperature ranges.

The third stage (A4) of the 3630 adds a great deal of versatility and convenience to the amplifier. Its use allows easy implementation of active low pass filtering, output offsetting, and additional gain generation. The pin connections make the use of this stage optional but the effects are included in electrical specifications.

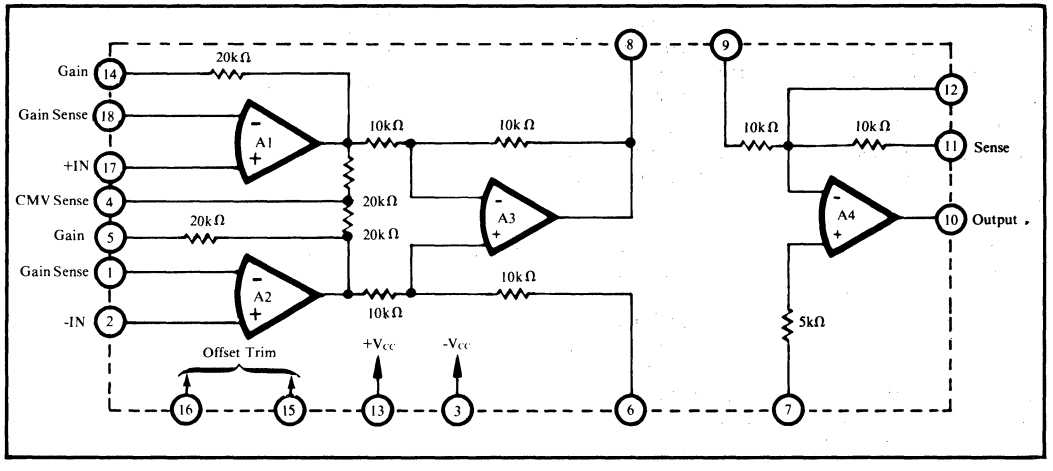


FIGURE 1. Simplified Schematic

USING THE 3630

Figure 2 shows the simplest configuration of the 3630. The gain is set by the external resistor R_G with a gain equation $G = 1 + 40k/R_G$. A low TCR resistor should be used for R_G since it contributes directly to the gain accuracy.

Pins 1, 5, 14 and 18 are accessible so that a four terminal connection can be made to R_G. (Pins 1 and 18 are the voltage sense terminals since no signal current flows into the operational amplifiers' inputs.) This may be useful at high gains where the value of R_G becomes small.

The optional offset null capability is shown in Figure 4. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be effected by approximately $0.33\mu V/°C$ per $100\mu V$ of input offset voltage nulled.

Output offsetting ("zero suppression" or "zero elevation") may be more easily accomplished with the 3630 than with most other IC instrumentation amplifiers.

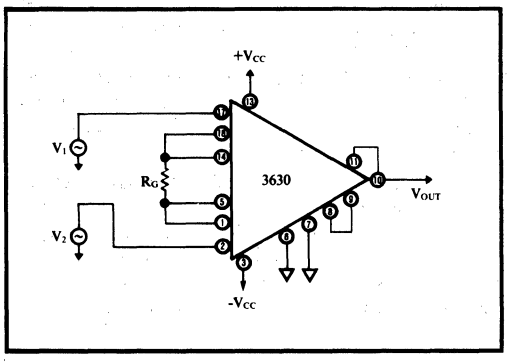


FIGURE 2. Basic Connections

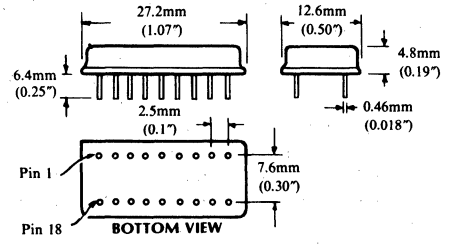
Figure 5 shows how this is done. The use of the noninverting input of the output stage means that CMR of the second stage is not disturbed and that any convenient value of variable resistor can be used.

The output stage also allows active low pass filtering to be implemented conveniently with a single capacitor. The effect this filtering has on noise reduction can be seen in the Typical Performance Curves.

The input stage contains extra resistors for the computation of input common-mode voltage. Figure 7 shows how this voltage, available at pin 4, can be used to drive the shield of the input cable. Since the cable is driven at the common-mode voltage the effects of distributed capacitance is reduced and the AC system common-mode rejection may be improved. Amplifier A1 is a buffer to supply larger currents than can be supplied by the 20kΩ resistors internally connected to pin 4.

Figure 8 shows how the output stage may be used to provide additional gain. If gains greater than 1000V/V are desired it is better to obtain them from the output stage than the input stage due to the low values of R_G required ($R_G < 40\Omega$ for $(1 + 40k/R_G) > 1000$).

MECHANICAL



Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).

FIGURE 3. Mechanical Specifications

PIN DESIGNATIONS

1. Gain Sense
2. Inverting Input
3. Negative Supply
4. Common-mode Voltage Sense
5. Gain
6. Ground
7. Reference
8. Output of A_3
9. Input to A_4
10. Output
11. Sense
12. Summing Junction of A_4
13. Positive Supply
14. Gain
15. Offset Trim
16. Offset Trim
17. Noninverting Input
18. Gain Sense

ELECTRICAL SPECIFICATIONS

Specifications typical at 25°C with ±15VDC power supply and in circuit of Figure 2 unless otherwise noted.

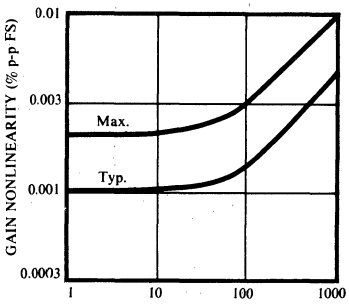
MODEL	3630AM			3630BM, 3630SM			3630CM			Units
	min	typ	max	min	typ	max	min	typ	max	
GAIN										
Range of Gain	1		1000	*		*	*		*	V/V
Gain Equation		G = 1 + 40k/R_G			*			*		V/V
Error From Equation, DC		(±0.05 ±0.0001G)	(±0.1 ±0.0002G)		(±0.02 ±0.00005G)	(±0.05 ±0.0001G)		(±0.02 ±0.00005G)	(±0.05 ±0.0001G)	%
Gain Temp. Coefficient [1]										
G = 1		8	20		*	*		*	*	ppm/°C
G = 10		45	115		*	*		*	*	ppm/°C
G = 100		50	125		*	*		*	*	ppm/°C
G = 1000		50	125		*	*		*	*	ppm/°C
Nonlinearity, DC		±(0.002 + 10^{-5}G)	±(0.005 + 2 x 10^{-5}G)		±(0.001 + 4 x 10^{-6}G)	±(0.002 + 10^{-5}G)		±(0.001 +4 x 10^{-6}G)	±(0.002 + 10^{-5}G)	% of p-p FS
RATED OUTPUT										
Voltage	±10	±12.5		*	*		*	*		V
Current	±5	±12.5		*	*		*	*		mA
Output Impedance		0.01			*			*		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at 25°C [2]		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	μV
vs. Temperature			±2 ±20/G			±0.75 ±10/G			±0.25 ±10/G	μV/°C
vs. Supply		±(1 + 20/G)			*			*		μV/V
vs. Time		±(1 + 20/G)			*			*		μV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input)		±15	±50		±10	±30		±5	±20	nA
vs. Temperature		±0.3			*			*		nA/°C
vs. Supply		±0.1			*			*		nA/V
Initial Offset Current		±15	±50		±10	±30		±5	±20	nA
vs. Temperature		±0.5			*			*		nA/°C
INPUT IMPEDANCE										
Differential		10 x 10^9 || 3			*			*		Ω || pF
Common-mode		10 x 10^9 || 3			*			*		Ω || pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10	±12		*	*		*	*		V
CMR w/ 1kΩ Source Imbal.										
DC to 60Hz, G = 1	80	90		*	*		*	*		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		dB
INPUT NOISE										
Voltage, p-p, 0.01Hz - 10Hz		1.2			*			*		μV p-p
rms, 10Hz - 1.0kHz		1.0			*			*		μV rms
Current, p-p, 0.01Hz - 10Hz		70			*			*		pA p-p
rms, 10Hz - 1.0kHz		20			*			*		pA rms
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness,										
G = 1		150			*			*		kHz
G = 10		90			*			*		kHz
G = 100		25			*			*		kHz
G = 1000		2.5			*			*		kHz
Small Signal, ±1% Flatness,										
G = 1		20			*			*		kHz
G = 10		10			*			*		kHz
G = 100		1			*			*		kHz
G = 1000		200			*			*		Hz
Full Power, G = 1 - 100		7.5			*			*		kHz
Slew Rate, G = 1 - 100	0.2	0.5		*	*		*	*		V/μsec
Settling Time (0.1%)										
G = 1		60			*			*		μsec
G = 100		100			*			*		μsec
G = 1000		500			*			*		μsec
Settling Time (.01%)										
G = 5		100			*			*		μsec
G = 100		150			*			*		μsec
G = 1000		1000			*			*		μsec
POWER SUPPLY										
Rated Voltage		±15			*			*		V
Voltage Range	±5		±20	*		*	*		*	V
Current, Quiescent		±8	±14		*	*		*	*	mA
TEMPERATURE RANGE										
Specification [3]	-25		+85	*		*	*		*	°C
Operation	-55		+125	*		*	*		*	°C
Storage	-65		+150	*		*	*		*	°C

NOTES:
1. With R_G TCR = 0 ppm/°C
2. Trimmable to zero at any one gain.
3. -55°C to +125°C for 3630SM.

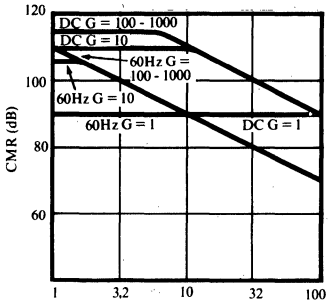
*Specifications same as for 3630AM

TYPICAL PERFORMANCE CURVES

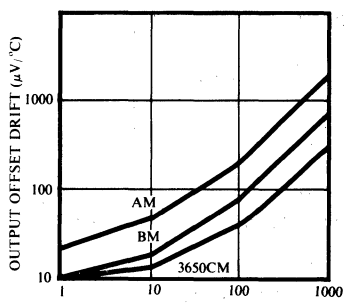
At 25°C and in circuit of Figure 2 unless otherwise noted.



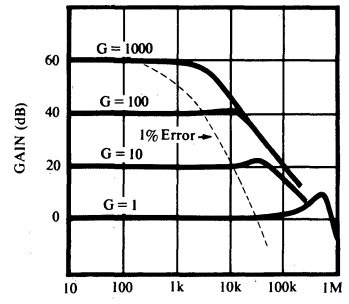
GAIN NONLINEARITY VS GAIN



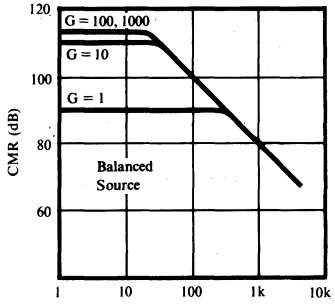
CMR VS SOURCE IMBLANCE



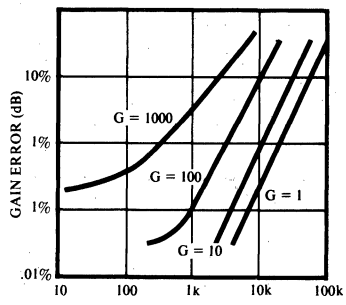
OUTPUT OFFSET DRIFT VS GAIN



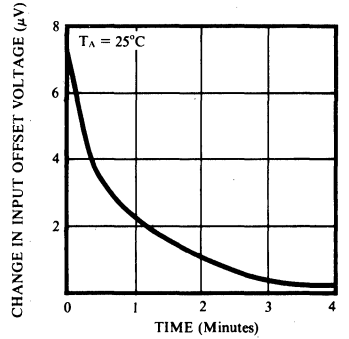
GAIN VS FREQUENCY



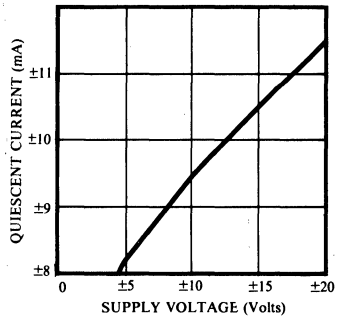
CMR VS FREQUENCY



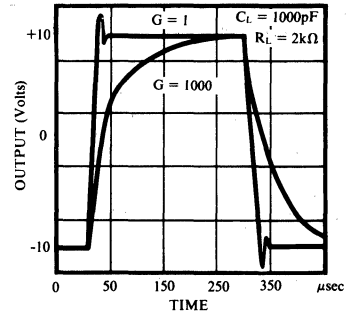
GAIN ERROR VS FREQUENCY



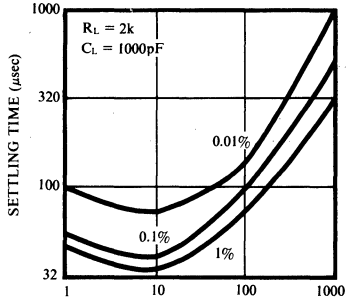
WARM-UP DRIFT VS TIME



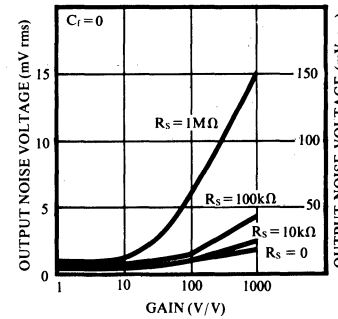
QUIESCENT CURRENT VS SUPPLY



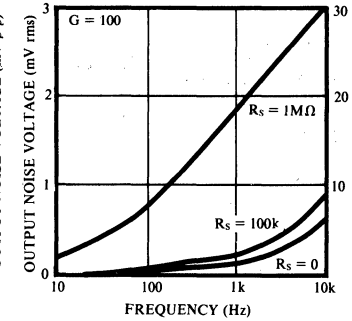
STEP RESPONSE



SETTLING TIME VS GAIN



OUTPUT NOISE VS GAIN



OUTPUT NOISE VS 3dB FREQUENCY

APPLICATIONS

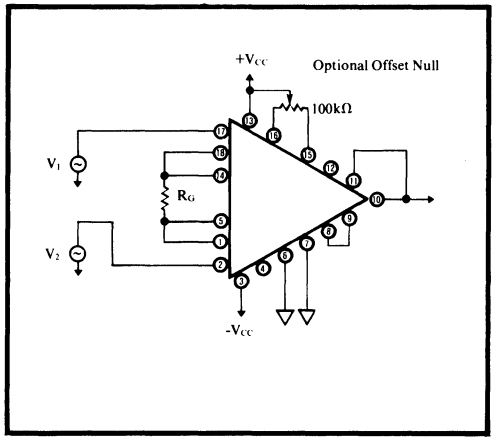


FIGURE 4. Optional Offset Null

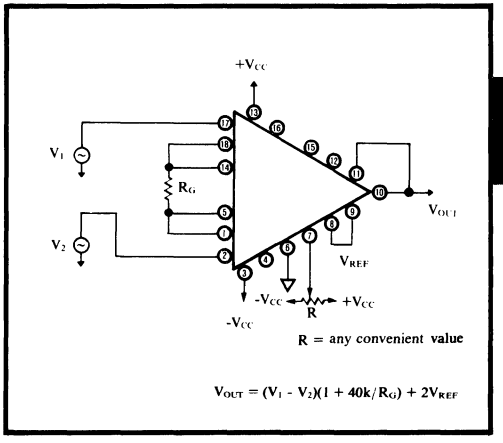


FIGURE 5. Output Offsetting

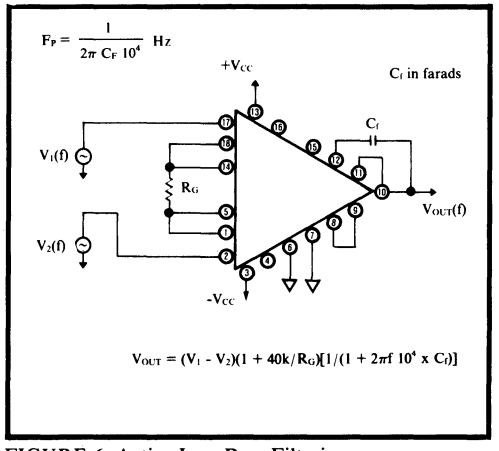


FIGURE 6. Active Low Pass Filtering

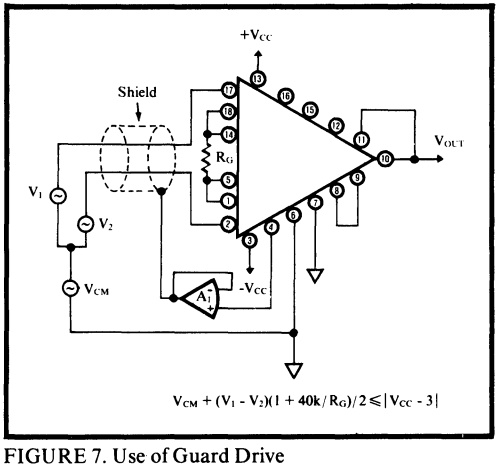


FIGURE 7. Use of Guard Drive

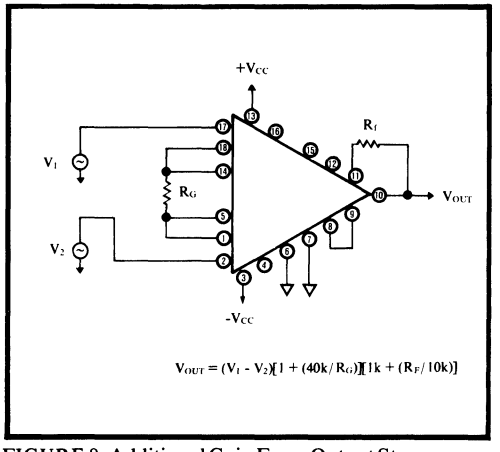


FIGURE 8. Additional Gain From Output Stage

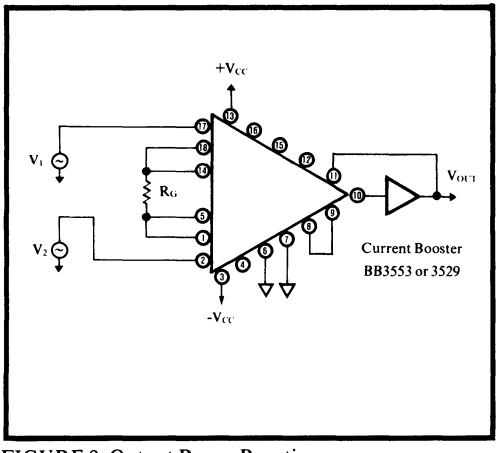
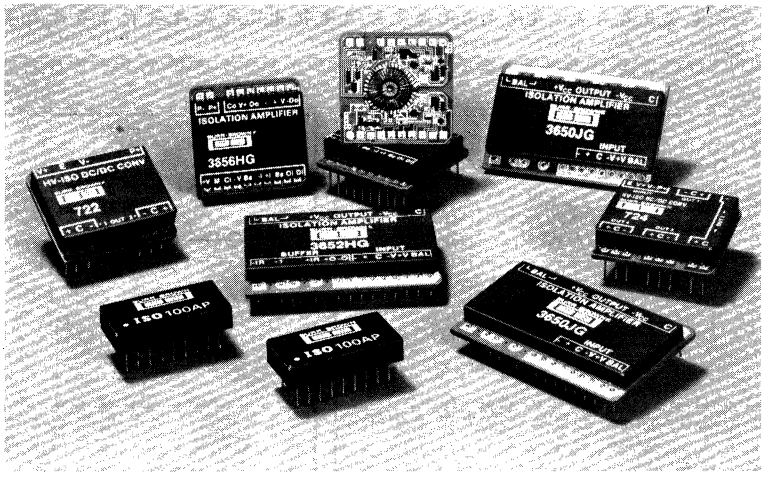


FIGURE 9. Output Power Boosting

ISOLATION AMPLIFIERS



WHAT IS AN ISOLATION AMPLIFIER?

An isolation amplifier is a device with the primary function of providing ohmic isolation (break the ohmic continuity of electrical signal) between the input signal/circuitry and the output of the amplifiers. It usually consists of an input operational amplifier or instrumentation amplifier followed by a unity-gain isolation stage. The sole purpose of the unity-gain isolation stage is to completely isolate the input from the output of the device. Ideally, the ohmic continuity of the input signal is broken (at the isolation barrier) yet accurate signal transfer without any attenuation is achieved across the unity-gain isolation stage. An important feature of an isolation amplifier is that it has a completely floating input which helps eliminate cumbersome connections to source ground in several applications.

Figures 1 and 2 show typical isolation amplifier applications. The isolation-mode voltage V_{iso} is the voltage which exists across the isolation barrier. The contribution of the output referred error caused by V_{iso} is (V_{iso}/IMRR) x Gain where IMRR is the Isolation Mode Rejection Ratio. V_{sig} is the differential input signal and V_{cm} is the common-mode voltage. The "Leakage Current" is the current which flows across the isolation barrier with some specified isolation voltage applied between the input and the output.

CHARACTERISTICS OF ISOLATION AMPLIFIERS

The following is a discussion of some of the characteristics and terms unique to isolation amplifiers.

Common-mode Voltage and Isolation Voltage - Some manufacturers (other than Burr-Brown) treat common-mode voltage and isolation voltages synonymously in describing the use and/or specifications of isolation amplifiers. It is important to understand the significance of these terms and the difference between them.

When the input common is grounded, the input signal V_d (see Figure 1) can be floated by the amount V_{cm} above the input ground. V_{cm} is the common-

mode voltage (CMV) and is generally ±10V, limited by the CMV rating of the input stage amplifier. In applications involving higher systems common-mode voltages, input common terminal is not grounded and the common-mode voltages are referenced across the isolation barrier to the output common terminal.

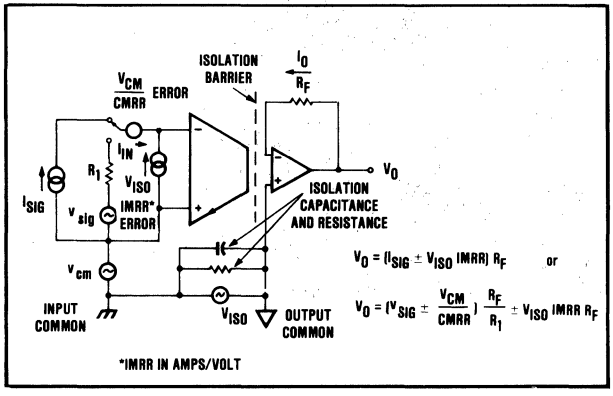


FIGURE 1. Typical Isolation Amplifier, Current (Input) Mode.

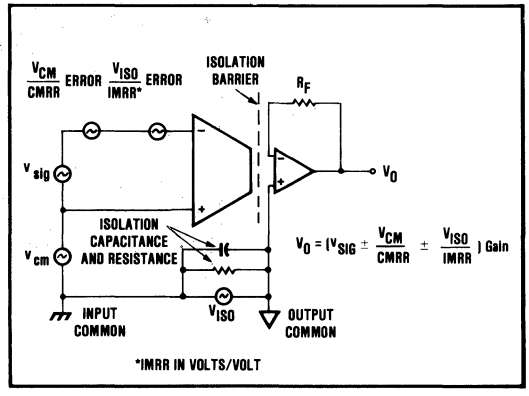


FIGURE 2. Typical Isolation Amplifier, Voltage (Input) Mode.

The isolation voltage V_{iso} as shown in Figure 1 is the potential difference between the input common and the output common terminals. The isolation voltage rating describes the amount of voltage that the isolation barrier can withstand without breakdown. This feature of the isolation amplifier allows two distinct ground connections to be made when necessary. It allows the isolation amplifier to be used in applications involving very-high common-mode voltages and in applications of breaking ground loops.

Many applications involve a large "system common-mode voltage." In such applications, the isolation amplifier's input common terminal is not connected to any ground but the output common terminal is connected to the system ground. In such a case, the term V_{cm} shown in Figures 1 and 2 becomes negligible and V_{iso} determines the safe limit for the system common-mode voltage. In this manner, the isolation amplifier can accommodate common-mode voltages of 2000V or more.

Common-mode Rejection and Isolation Rejection - Isolation-mode rejection (IMR) is another term which some other manufacturers refer to as common-mode rejection (CMR). The above discussion on the common-mode voltage and isolation voltage helps recognize the difference between CMR and the IMR. The CMR is the measure of the input stage amplifier's ability to reject common-mode input signals (common-mode with reference to the output common) while transmitting the differential signal across the isolation barrier. The isolation-mode rejection ratio (IMRR) is defined by the equation shown in Figures 1 and 2. Thus, understanding the IMR capability of isolation amplifiers allows their meaningful use in applications requiring very high common-mode rejection ratios such as 100dB to 140dB.

Isolation Voltage Ratings, Test Voltage - It is important to understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. For most isolation amplifiers, Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may chose to use a less conservative derating to establish a specification from the test voltage.

APPLICATIONS OF ISOLATION AMPLIFIERS

When one or more of the following conditions/requirements are present in an application, an isolation amplifier would generally be the right choice as a signal conditioning device:

- When ohmic isolation between the signal source and the output is a requirement (isolation impedance between the input and the output $>$ 10MΩ).
- When excellent common-mode noise and voltage rejection is a requirement (CMR $>$ 100dB).
- When it is necessary to process signals in the presence of, or riding on, high common-mode voltages (CMV $\gg$ 10V).

In general, most applications can be broadly categorized into the following four types:

- Amplifying and measuring low level signals in the presence of high common-mode voltages.
- Breaking ground loops and/or eliminating source ground connections. The isolation amplifier provides full floating input, eliminating the need for connections to source ground, and thus allows two-wire hook-up to the signal sources.
- Providing an interface between medical patient monitoring equipment and the transducer/devices which may be in physical contact with the patients. Such applications require high isolation voltage levels and very-low leakage currents.
- Providing isolation protection to electronic instruments/equipment. Large common-mode voltages occasionally cause hazardous electronic faults. Low leakage currents and high isolation voltage capability of isolation amplifiers help protect instruments against damage caused by such faults.

Isolation amplifier performance requirements vary significantly, depending on the type of requirement. In applications where bandwidth and speed of response are more important than gain accuracy and linearity, the optically-coupled amplifiers will be the best choice. For applications where gain accuracy and linearity are key parameters, Burr-Brown's family of transformer-coupled amplifiers are the suitable choice.

*Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

SELECTION GUIDE
Isolation Amplifiers

TRANSFORMER COUPLED AMPLIFIERS

Description	Model	Isolation Voltage: Continuous (Vpeak)	Isolation Voltage: Pulse/Test (Vpeak)	Isolation Mode Rejection, min: DC (dB)	Isolation Mode Rejection, min: 60Hz (dB)	Leakage Current at Test Voltage (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Gain Nonlinearity: max (%)	Gain Nonlinearity: typ (%)	Input Offset Volt. Drift (±μV/°C) max	Bias Current max	±3dB Freq kHz	External Isolation Power Required	Temp. Range[1]	Package	Price $: Unit	Price $: 100's	Page
Low Drift[2]	3450	±500	±2000	160	120	1	10^{12}	16	±0.005	±0.0015	1 + (100/G_1)	50nA	1.5	No	Com	Module	229.50	149.00	3-19
Low Bias FET	3491	±500	±2000	160	120	1	10^{12}	16	±0.025	±0.005	50 + (100/G_1)	25pA	2.5	No	Com	Module	121.50	88.00	3-19
	3452	±2000	±5000	160	120	1	10^{12}	16	±0.025	±0.005	5 + (100/G_1)	20pA	2.5	No[4]	Com	Module	162.50	117.50	3-19
	3455	(3)	(3)	160	120	(3)	10^{12}	16	±0.025	±0.005	5 + (100/G_1)	20pA	2.5	No[4]	Com	Module	172.50	127.50	1-19
True 3-wire Inst. Amp	3456A	±2000	±5000	160	130	25	10^{12}	14	±0.02	±0.01	2 + (150/G_1)	50nA	2.5	No	Com	Module	148.00	117.25	3-26
	3456B	±2000	±5000	160	130	25	10^{12}	14	±0.08	±0.03	1 + (75/G_1)	50nA	2.5	No	Com	Module	168.50	133.65	3-26
Highest Isolation Voltage	3656AG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	25 + (500/G_1)	100nA	30	No	Ind	DIP	82.25	55.10	3-40
	3656BG	±3500	±8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5 + (350/G_1)	100nA	30	No	Ind	DIP	101.60	74.15	3-40
	3656HG	±3500	±8000	160	125	0.5	10^{12}	6	±0.15	±0.03	200 + (1000/G_1)	100nA	30	No	Com	DIP	72.60	48.65	3-40
	3656JG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	50 + (750/G_1)	100nA	30	No	Com	DIP	77.40	51.90	3-40
	3656KG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	10 + (350/G_1)	100nA	30	No	Com	DIP	95.15	63.75	3-40

OPTICALLY COUPLED AMPLIFIERS

Description	Model	Isolation Voltage: Continuous (Vpeak)	Isolation Voltage: Pulse/Test (Vpeak)	Isolation Mode Rejection, min: DC (dB)	Isolation Mode Rejection, min: 60Hz (dB)	Leakage Current at Test Voltage (μA)	Isolation Impedance (Ω)	Isolation Impedance (pF)	Gain Nonlinearity: max (%)	Gain Nonlinearity: typ (%)	Input Offset Volt. Drift (±μV/°C) max	Bias Current max	±3dB Freq kHz	External Isolation Power Required	Temp Range[1]	Package	Price $: Unit	Price $: 100's	Page
Balanced Current Input	3650HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	25 + (900/G_1)	10nA	15	Yes[6]	Ind	DIP	51.00	30.60	3-32
	3650JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.03	10 + (450/G_1)	10nA	15	Yes[6]	Ind	DIP	66.30	42.30	3-32
	3650KG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.05	±0.02	5 + (300/G_1)	10nA	15	Yes[6]	Ind	DIP	80.60	59.00	3-32
	3650MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100 + (900/G_1)	10nA	15	Yes[6]	Ind	DIP	44.90	29.10	3-32
Balanced FET Input	3652HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	50 + (900/G_1)	50nA	15	Yes[6]	Ind	DIP	66.30	42.30	3-32
	3652JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.05	25 + (450/G_1)	50nA	15	Yes[6]	Ind	DIP	80.60	58.00	3-32
	3652MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100 + (900/G_1)	50nA	15	Yes[6]	Ind	DIP	52.00	38.80	3-32
Miniature Isolation Amplifier	ISO100AP	750	1000	5pA/V typ.[8]	400 pA/V typ.[8]	0.3	10^{12}	2.5	0.4	--	5 + (5/G_1)	10nA[7]	60	Yes	Ind	DIP	(9)	--	3-6
	ISO100BP	750	1000			0.3	10^{12}	2.5	0.07	--	2 + (2/G_1)	10nA[7]	60	Yes	Ind	DIP	(9)	--	3-6
	ISO100CP	750	1000			0.3	10^{12}	2.5	0.03	--	1 + (1/G_1)	10nA	60	Yes	Ind	DIP	(9)	--	3-6

NOTES: 1) Com = 0°C to +70°C; Ind = -25°C to +85°C. 2) Bipolar. 3) Isolation voltage tested at 2500V, rms, 60Hz; leakage current tested for 2μA max at 240V, rms, 60Hz. 4) ±15V at ±15mA isolated power available to power external circuitry. 5) At 240V/60Hz. 6) Models 722 or 724. 7) For ISO100 values shown are I_{OS}. 8) See product data sheet for detailed discussion. 9) Advance Information, subject to change, contact Burr-Brown for price and delivery.

GLOSSARY OF TERMS & DEFINITIONS
Isolation Amplifiers

ISOLATION AMPLIFIER

A device which provides ohmic isolation (breaks ohmic continuity of an electric signal) between the input and the output of the device. Method of coupling may be thermal, magnetic, optical, or any means other than direct ohmic coupling. Such a device allows the input circuit to be referenced separately and independent of the output circuitry.

ISOLATION BARRIER

A barrier or region between the input and the output stage of an isolation amplifier, where signal transfer is achieved between the input and the output.

ISOLATION IMPEDANCE

The effective impedance between the input common terminal and the output common terminal. It is the impedance of the isolation barrier. (It is usually specified as a typical parameter. Leakage current is related to isolation impedance and is usually specified with a maximum limit.)

ISOLATION-MODE REJECTION (IMR)

The IMR is the measure of an isolation amplifier's ability to reject common-mode input signals (common-mode with reference to the output common), while transmitting the differential signal across the isolation barrier. It is the voltage or current that must be applied to the input to force the output to zero when V_{iso} is present.

For voltage input mode:

$$IMRR = \frac{V_{o\ error\ ISO}/G}{V_{iso}} \text{ with } V_o = 0$$

For current input mode:

$$IMRR = \frac{I_{o\ error\ ISO}}{V_{iso}} \text{ with } V_o = 0\ (I_o = 0)$$

ISOLATION VOLTAGE

The potential difference between the input stage common and output stage common terminals of an isolation amplifier.

ISOLATION VOLTAGE RATING

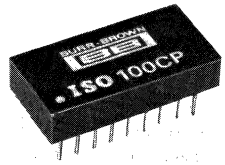
The amount of voltage that can be impressed between the input common and the output common terminals (across the isolation barrier) without resulting in breakdown.

LEAKAGE CURRENT

The current that flows between the input common terminal and the output common terminal (across the isolation barrier) with a specified voltage applied across it. (It is usually 100% tested and specified with a maximum limit.)

BURR-BROWN®

ISO100



ADVANCE INFORMATION
Subject to Change

Miniature Low Drift - Wide Bandwidth ISOLATION AMPLIFIER

FEATURES

- EASY TO USE, SIMILAR TO AN OP AMP
  $V_{OUT}/I_{IN} = R_F$, Current Input
  $V_{OUT}/V_{IN} = R_F/R_{IN}$, Voltage Input
- KEY PARAMETERS TESTED AT 1000V
- ULTRA-LOW LEAKAGE, 0.3μA, max, at 240V/60Hz
- WIDE BANDWIDTH, 60kHz
- LOW COST
- 18-PIN DIP PACKAGE

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
  Transducer sensing
  (thermocouple, RTD, pressure bridges)
  4mA to 20mA loops
  Motor and SCR control
  Ground loop elimination
- BIOMEDICAL MEASUREMENTS
- TEST EQUIPMENT
- DATA ACQUISITION

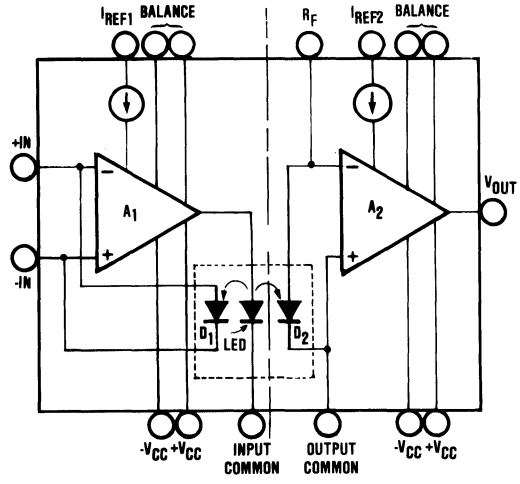
DESCRIPTION

The ISO100 is a miniature low cost optically-coupled isolation amplifier. High accuracy, linearity, and time-temperature stability are achieved by coupling light from an LED back to the input (negative feedback) as well as forward to the output. Optical components are carefully matched and the amplifier is actively laser-trimmed to assure excellent tracking and low offset errors.

The circuit acts as a current-to-voltage converter with a minimum of 750V (2500V test) between input and output terminals. It also effectively breaks the galvanic connection between input and output commons as indicated by the ultra-low 60Hz leakage current of 0.3μA at 240V. Voltage input operation is easily achieved by using one external resistor.

Versatility along with outstanding DC and AC performance provide excellent solutions to a variety of challenging isolation problems. For example, the ISO100 is capable of operating in many modes, including: noninverting (unipolar and bipolar) and inverting (unipolar and bipolar) configurations. Two precision current sources are provided to accomplish bipolar operation. Since these are not required for unipolar operation, they are available for external use (see Applications section).

Designs using the ISO100 are easily accomplished with relatively few external components. Since V_{OUT} of the ISO100 is simply $I_{IN}R_{OUT}$, gains can be changed by altering one resistor value. In addition, the ISO100 has sufficient bandwidth (DC to 60kHz) to amplify most industrial and test equipment signals.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

PARAMETER	CONDITIONS	ISO100AP			ISO100BP			ISO100CP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Rated Continuous, DC		750			*			*			VDC
Test, Parametric(1)		1000			*			*			VDC
Test, Breakdown	10sec	2500			*			*			VDC
Rejection(2) DC			5			*			*		pA/V
	R_{IN} =10kΩ, Gain = 100		146			*			*		dB
AC	60Hz, 480V, R_F = 1MΩ		400			*			*		pA/V
	R_{IN} = 10kΩ, Gain = 100		108			*			*		dB
Resistance || Capacitance			10^{12} || 2.5			*			*		Ω || pF
Leakage Current	240V, rms, 60Hz			0.3			*			*	μA, rms
OFFSET VOLTAGE (RTI)											
Input Stage (V_{OSI})											
Initial Offset(1)				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Input Power Supplies(1)				105			*			*	dB
vs Time			1			*			*		μV/kHr
Output Stage (V_{OSO})											
Initial Offset(1)				500			300			200	μV
vs Temperature				5			2			2	μV/°C
vs Output Power Supplies(1)				105			*			*	dB
vs Time			1			*			*		μV/kHr
Common-Mode Rejection Ratio(2)	60Hz, R_F = 1MΩ		3			*			*		nA/V
	R_{IN} = 10kΩ, Gain = 100		90			*			*		dB
Common-Mode Range	±10				*			*			V
REFERENCE CURRENT SOURCES											
Magnitude											
Nominal		10.5	12	12.5	*	*	*	*	*	*	μA
vs Temperature				400			175			175	ppm/°C
vs Power Supplies			0.3	3		*	*		*	*	nA/V
Matching											
Nominal			50			*			*		nA
vs Temperature			150			*			*		ppm/°C
vs Power Supplies			0.3			*			*		nA/V
Compliance Voltage	-10			+15	*		*	*		*	V
Output Resistance			2 x 10^9			*			*		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	Gain = 1V/μA		60			*			*		kHz
Full Power Bandwidth	Gain = 1V/μA, V_O = ±10V		6			*			*		kHz
Slew Rate(1)			0.4			*			*		V/μsec
Settling Time	0.1%		100			*			*		μsec
TEMPERATURE RANGE											
Specification		-25		+85	*		*	*		*	°C
Operating		-40		+100	*		*	*		*	°C
Storage		-55		+100	*		*	*		*	°C

UNIPOLAR OPERATION

GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-20		-0.02	*		*	*		*	μA
Without Damage		-1		+1	*		*	*		*	mA
Input Impedance			0.1			*			*		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	-10		0	*		*	*		*	V
Output Impedance	DC		1200			*			*		Ω
GAIN	$V_O = R_F (I_{IN})$										
Initial Error (Adjustable To Zero)(1)			2	5		1	2		1	2	% FS
vs Temperature			0.03	0.06		0.01	0.04		0.005	0.03	%/°C
vs Time			0.05			*			*		%/kHr
Nonlinearity(1)(3)			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE	I_{IN} = 0.2μA										
0.01Hz to 10Hz			20			*			*		pA, p-p
10Hz			1			*			*		pA/$\sqrt{Hz}$
100Hz			0.7			*			*		pA/$\sqrt{Hz}$
1kHz			0.65			*			*		pA/$\sqrt{Hz}$
INPUT OFFSET CURRENT (I_{OS})											
Initial Offset			1	10		*	*		*	*	nA
vs Temperature			0.01	0.05		*	*		*	*	nA/°C
vs Power Supplies			0.1			*			*		nA/V
vs Time			100			*			*		pA/kHr

ELECTRICAL (CONT)

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

PARAMETER	CONDITIONS	ISO100AP MIN	ISO100AP TYP	ISO100AP MAX	ISO100BP MIN	ISO100BP TYP	ISO100BP MAX	ISO100CP MIN	ISO100CP TYP	ISO100CP MAX	UNITS
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	I_{IN} = -0.02μA		±1.1	±2		*	*		*	*	mA
	I_{IN} = -20μA		+8, -1.1	+13, -2		*	*		*	*	mA
Output Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	V_O = 0		±1.1	±2		*	*		*	*	mA
Short Circuit Current Limit(1)				±40			*			*	mA

BIPOLAR OPERATION

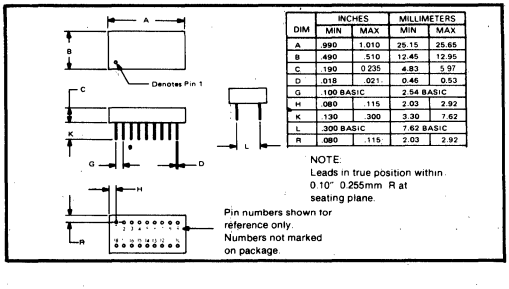
GENERAL PARAMETERS											
Input Current Range											
Linear Operation		-10		+10	*		*	*		*	μA
Without Damage		-1		+1	*		*	*		*	mA
Input Impedance			0.1			*			*		Ω
Output Voltage Swing	R_L = 2kΩ, R_F = 1MΩ	-10		+10	*		*	*		*	mA
Output Impedance			1200			*			*		* Ω
GAIN	$V_O = R_F (I_{IN})$										
Initial Error (Adjustable To Zero)(1)			2	5		1	2		1	2	% of FS
vs Temperature			0.03	0.06		0.01	0.04		0.005	0.03	%/°C
vs Time			0.05			*			*		%/kHr
Nonlinearity(1)(3)			0.1	0.4		0.03	0.1		0.02	0.07	%
CURRENT NOISE	I_{IN} = 0.2μA										
0.01Hz to 10Hz			1.5			*			*		nA, p-p
10Hz			17			*			*		pA/√Hz
100Hz			7			*			*		pA/√Hz
1kHz			6			*			*		pA/√Hz
INPUT OFFSET CURRENT (I_{OS}, bipolar)(4)											
Initial Offset(1)			40	200		20	70		10	35	nA
vs Temperature				3			1.3			0.8	nA/°C
vs Power Supplies				0.7			*			*	nA/V
vs Time			250			*			*		pA/kHr
POWER SUPPLIES											
Input Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	I_{IN} = +10μA		+2, -1.1	+3,-2		*	*		*	*	mA
	I_{IN} = -10μA		+8, -1.1	+13,-2		*	*		*	*	mA
Output Stage											
Voltage (rated performance)			±15			*			*		V
Voltage (derated performance)		±7		±18	*		*	*		*	V
Supply Current	V_O = 0		±1.1	±2		*	*		*	*	mA
Short Circuit Current Limit(1)				±40			*			*	mA

* Same as ISO100AP.

NOTES:

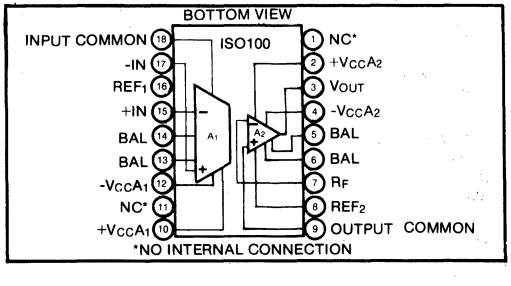
1. These parameters are tested during the 1000V stress test.
2. See Theory of Operation section for definitions. For dB see Ex. 2, CM and HV errors.
3. Nonlinearity is the peak deviation from a "best fit" straight line expressed as a percent of full scale output.
4. Bipolar offset current includes effects of reference current mismatch and unipolar offset current.

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.990	1.010	25.15	25.65
B	.490	.510	12.45	12.95
C	.190	0.235	4.83	5.97
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

PIN CONFIGURATION



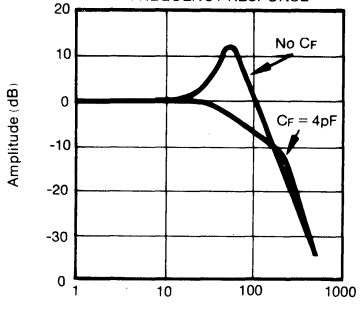
ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±18V
Isolation Voltage	2500V
Input Current	±1mA
Storage Temperature Range	-55°C to +100°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground

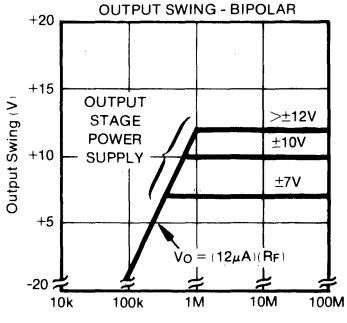
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted)

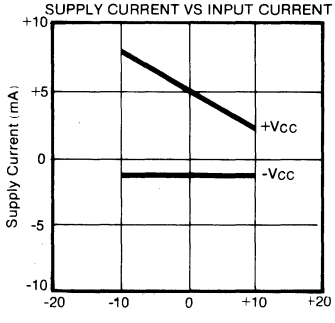
SMALL SIGNAL FREQUENCY RESPONSE



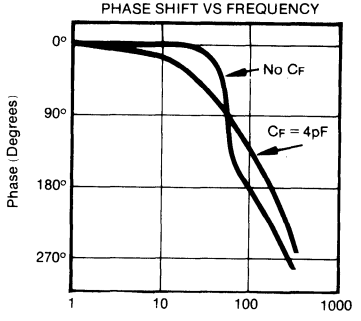
OUTPUT SWING - BIPOLAR



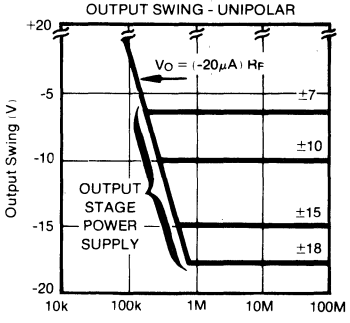
BIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



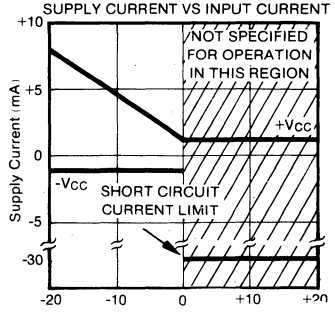
PHASE SHIFT VS FREQUENCY



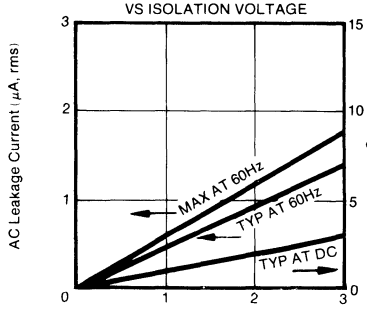
OUTPUT SWING - UNIPOLAR



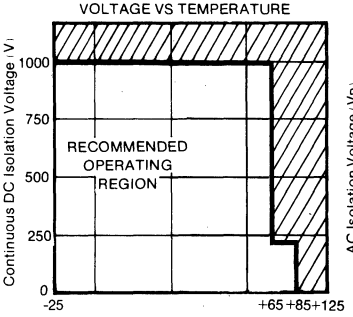
UNIPOLAR INPUT STAGE SUPPLY CURRENT VS INPUT CURRENT



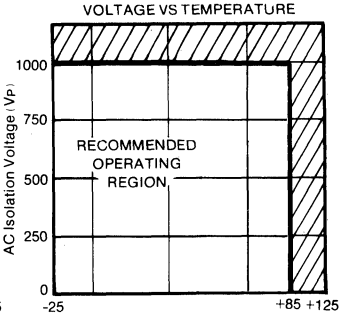
ISOLATION LEAKAGE CURRENT VS ISOLATION VOLTAGE

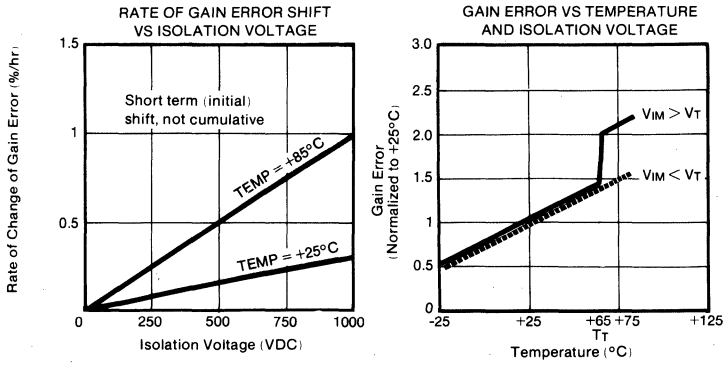


CONTINUOUS DC ISOLATION VOLTAGE VS TEMPERATURE



AC ISOLATION VOLTAGE VS TEMPERATURE





NOTES:
V_T and T_T approximate the threshold for the indicated gain shift. This is caused by the properties of the optical cavity.

$T_T \approx +65°C$, $V_T \approx 200VDC$. Shift does not occur for AC voltages.

V_{IM} = Isolation-mode Voltage
V_T = Threshold Voltage
T_T = Threshold Temperature

THEORY OF OPERATION

The ISO100 is fundamentally a unity gain current amplifier intended to transfer small signals between electrical circuits separated by high voltages or different references. In most applications an output voltage is obtained by passing the output current through the feedback resistor (R_F).

The ISO100 uses a single light emitting diode (LED) and a pair of photodiode detectors, coupled together, to isolate the output signal from the input.

Figure 1 shows a simplified diagram of the amplifier. I_{REF1} and I_{REF2} are required only for bipolar operation, to generate a midscale reference. The LED and photodiodes (D1 and D2) are arranged such that the same amount of light falls on each photodiode. Thus, the currents generated by the diodes match very closely. As a result, the transfer function depends upon optical match, rather than absolute performance. Laser-trimming of the components improves matching and enhances accuracy, while negative feedback improves linearity. Negative feedback around A1 occurs through the optical path formed by the LED and D1. The signal is transferred across the isolation barrier by the matched light path to D2.

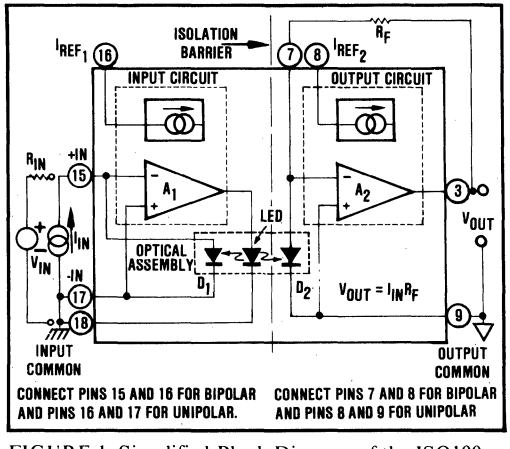


FIGURE 1. Simplified Block Diagram of the ISO100.

The overall ISO amplifier is noninverting (a positive going input produces a positive going output).

INSTALLATION AND OPERATING INSTRUCTIONS

UNIPOLAR OPERATION

In Figure 1, assume a current, I_{IN}, flows out of the ISO100 (I_{IN} must be negative in unipolar operation). This causes the voltage at pin 15 to decrease. Because the amplifier is inverting, the output of A1 increases, driving current through the LED. As the LED light output increases, D1 responds by generating an increasing current. The current increases until the sum of the currents in and out of the input node (-Input to A_1) is zero. At that point the negative feedback through D1 has stabilized the loop, and the current I_{D1} equals the input current plus the bias current. As a result no bias current flows in the source. Since D1 and D2 are matched ($I_{D1} = I_{D2}$), I_{IN} is replicated at the output via D2. Thus, A1 functions as a unity-gain current amplifier, and A2 is a current-to-voltage converter, as described below.

Current produced by D2 must either flow into A2 or R_F. Since A2 is designed for low bias current ($\approx$10nA) almost all of the current flows through R_F to the output. The output voltage then becomes;

$V_O = (I_{D2})\ R_F = (I_{D1} \pm I_{OS})\ R_F \approx -(-I_{IN})\ R_F = I_{IN}R_F$, (1)

where, I_{OS} is the difference between A1 and A2 bias currents. For input voltage operation I_{IN} can be replaced by a voltage source (V_{IN}) and series resistor (R_{IN}) since the summing node of the op amp is essentially at ground. Thus, $I_{IN} = V_{IN}/R_{IN}$.

Unipolar operation does have some constraints, however. In this mode the input current must be negative so as to produce a positive output voltage from A1 to turn the LED on. A current more negative than 20nA is necessary to keep the LED turned on and the loop stabilized. When this condition is not met the output may be indeterminant. Many sensors generate unidirectional signals, e.g., photoconductive and photodiode devices, as well as some applications of thermocouples. However, other applications do require bipolar operation of the ISO100.

BIPOLAR OPERATION

To activate the bipolar mode, reference currents as shown in Figure 1, are attached to the input nodes of the op amps. The input stage stabilizes just as it did in unipolar operation. Assuming $I_{IN} = 0$, the photodiode has to supply all the I_{REF1} current. Again, due to symmetry, $I_{D1} = I_{D2}$. Since the two references are matched, the current generated by D2 will equal I_{REF2}. This results in no current flow in R_F, and the output voltage will be zero. When I_{IN} either adds or substracts current from the input node, the current D1 will adjust to satisfy $I_{D1} = I_{IN} + I_{REF1}$. Because I_{REF1} equals I_{REF2} and I_{D1} equals I_{D2}, a current equal to I_{IN} will flow in R_F. The output voltage is then $V_O = I_{IN}R_F$. The range of allowable I_{IN} is limited. Positive I_{IN} can be as large as I_{REF1} (10.5μA, min). At this point, D1 supplies no current and the loop opens. Negative I_{IN} can be as large as that generated by D1 with maximum LED output (recommended 10μA, max).

DC ERRORS

Errors in the ISO100 take the form of offset currents and voltages plus their drifts with temperature. These are shown in Figure 2.

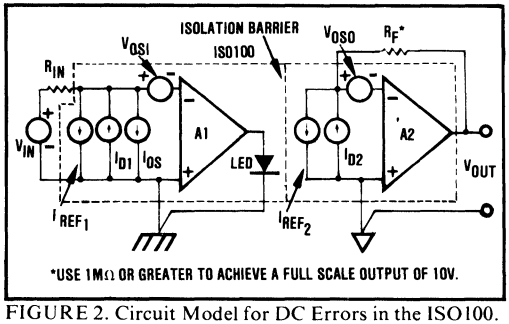


FIGURE 2. Circuit Model for DC Errors in the ISO100.

A1 and A2: are assumed to be ideal amplifiers.

V_{OSO} and V_{OSI}: are the input offset voltages of the output and input stage, respectively. V_{OSO} appears directly at the output, but, V_{OSI} appears at the output as

$$V_{OSI}\frac{R_F}{R_{IN}},$$

see equation (2).

I_{OS}: is the offset current. This is the current at the input necessary to make the output zero. It is equal to the combined effect of the difference between the bias currents of A1 and A2 and the matching errors in the optical components, in the unipolar mode.

I_{REF} and I_{REF2}: are the reference currents that, when connected to the inputs, enable bipolar operation. The two currents are trimmed, in the bipolar mode, to minimize the $I_{OS\ bipolar}$ error.

I_{D1} and I_{D2}: are the currents generated by each photodiode in response to the light from the LED.

A_e: is the gain error.

$$A_e = |\text{Ideal gain}/\text{Actual gain}| - 1$$

The output then becomes:

$$V_{OUT} = R_F\left[\left(\frac{V_{IN} \pm V_{OSI}}{R_{IN}} - I_{REF} \pm I_{OS}\right)(1 + A_e) + I_{REF2}\right] \pm V_{OSO} \quad (2)$$

The total input referred offset voltage of the ISO100 can be simplified by assuming that $A_e = 0$ and $V_{IN} = 0$:

$$V_{OUT} \approx R_F\left[\frac{\pm V_{OSI}}{R_{IN}} \pm I_{OS} \pm \Delta I_{REF}\right] \pm V_{OSO} \quad (3)$$

where, $\Delta I_{REF} = I_{REF1} - I_{REF2}$.

This voltage is then referred back to the input by dividing by R_F/R_{IN}.

Letting $\Delta I_{REF} - I_{OS} = I_{OS\ bipolar}$,

$$V_{OS(RTI)} = (\pm V_{OSI}) \pm R_{IN}(I_{OS\ bipolar}) + V_{OSO}/(R_F/R_{IN}) \quad (4)$$

Example 1: (Refer to Figure 2 and Electrical Specifications Table)

Given: $R_{IN} = 100k\Omega$, $R_F = 1M\Omega$ (gain = 10),
$V_{OSI} = +200\mu V$.
$I_{OS\ bipolar} = +35nA$, $V_{OSO} = +200\mu V$

Find: The total offset voltage error referred to the input and output when $V_{IN} = 0V$

V_{OS} total RTI $= \pm V_{OS}I \pm R_{IN}(I_{OS\ bipolar}), \pm V_{OSO}(R_F/R_{IN})$
$= +200\mu V + 100k\Omega\ (35nA) + 200\mu V/(1M\Omega/100k\Omega)$
$= 0.2mV + 3.5mV + 0.02mV$
$= 3.72mV$

V_{OS} total RTO = V_{os} total RTI x RF/RIN
$= 3.72mV \times 10$
$= 37.2mV$

(Note: This error is dominated by $I_{OS\ bipolar}$)

COMMON-MODE AND HIGH VOLTAGE ERRORS

Figure 3 shows a model of the ISO100 that can be used to analyze common-mode and high voltage behavior.

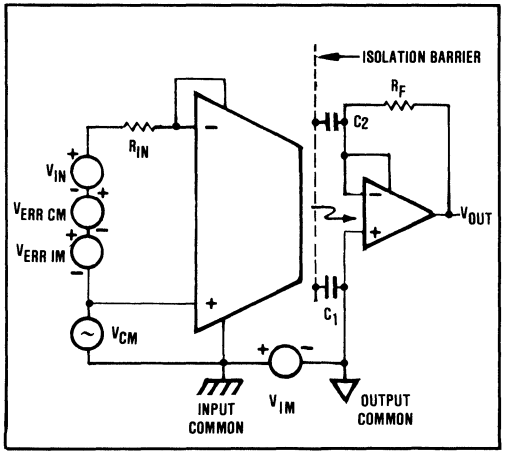


FIGURE 3. High Voltage Error Model.

ISO100

Definitions of CMR and IMR

I_{OS} is defined as the input current required to make the ISO100's output zero. CMRR and IMRR in the ISO100 are expressed as conductances. CMRR defines the relationship between a change in the applied common-mode voltage (V_{CM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

$$\text{CMRR (I-mode)} = \Delta I_{OS}/\Delta V_{CM} \text{ in nA/V} \quad (5)$$

$$\text{CMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{CM}}\right] R_{IN} = \frac{\Delta V_{ERR\ CM}}{\Delta V_{CM}} \text{ in V/V} \quad (6)$$

IMRR defines the relationship between a change in the applied isolation mode voltage (V_{IM}) and the change in I_{OS} required to maintain the amplifier's output at zero:

$$\text{IMRR (I-mode)} = \frac{\Delta I_{OS}}{\Delta V_{CM}} \text{ in pA/V} \quad (7)$$

$$\text{IMRR (V-mode)} = \left[\frac{\Delta I_{OS}}{\Delta V_{IM}}\right] R_{IN} = \frac{\Delta V_{ERR\ IM}}{\Delta V_{IM}} \text{ in V/V} \quad (8)$$

CMRR & IMRR in V/V are a function of R_{IN}.

V_{IM} is the voltage between input common and output common.

V_{CM} is the common-mode voltage (noise that is present on both input lines, typically 60Hz).

V_{ERR} is the equivalent error signal, applied in series with the input voltage, which produces an output error identical to that produced by application of V_{CM} and V_{IM}.

CMRR and IMRR are the common-mode and isolation-mode rejection ratios, respectively.

TOTAL CAPACITANCE (C_1 and C_2) is distributed along the isolation barrier. Most of the capacitance is coupled to low impedance or noncritical nodes and affects only the leakage current. Only a small capacitance (C_2) couples to the input of the second stage, and contributes to IMRR.

Example 2: Refer to Figure 3 and Electrical Specification Table)

Given: V_{CM} = 1V_{AC} peak at 60Hz, V_{IM} = 200VDC, CMRR = 3nA/V, IMRR = 5pA/V, R_{IN} = 100kΩ, R_F = 1MΩ (Gain = 10)

Find: The error voltage referred to the input and output when V_{IR} = 0V

$$V_{ERR\ RTI} = (V_{CM})(CMRR)(R_{IN}) + (V_{IM})(IMRR)(R_{IN})$$
$$= 1V\ (3nA/V)\ (100k\Omega) + 200V\ (5pA/V)(100k\Omega)$$
$$= 0.3mV + 0.1mV$$
$$= 0.4mV$$

$$V_{ERR\ RTO} = V_{ERR\ RTI}\ (R_F/R_{IN})$$
$$= 0.4mV\ (10)$$
$$= 4mV \text{ (with DC IMRR)}$$

(Note: This error is dominated by the CMRR term)

For purposes of comparing CMRR and IMRR directly with dB specifications, the following calculations can be performed:

$$\text{CMRR in V/V} = \text{CMRR (I-mode)}(R_{IN}) = 3nA/V(100k) = 0.3mV/V$$

$$\text{CMR} = 20 \text{ LOG } (0.3mV/V) = -70dB \text{ at } 60Hz$$

$$\text{IMRR in V/V} = \text{IMRR (I-mode)}(R_{IN}) = 5pA/V\ (100k) = 0.5\mu V/V$$

$$\text{IMR} = 20 \text{ LOG } (0.5 \times 10^{-6} V/V) = -126dB \text{ at DC}$$

Example 3:

In Example 2, V_{IM} is an AC signal at 60Hz and

$$\text{IMRR} = \frac{400pA}{V}$$

$$V_{ERR\ RTI} = V_{ERR}\ CM + V_{ERR\ IM}$$
$$= 0.3mV + 200V\ (400pA/V)(100k\Omega)$$
$$= 83mV$$

$V_{ERR\ RTO}$ = 83mV (with AC IMRR)

Example 4:

Given: Total error RTO from Examples 1 and 3 as 120.2mV (with AC IMRR)

Find: Percent error of +10V full scale output

$$\%\ \text{Error} = \frac{V_{ERR\ total}}{V_{FS}} \times 100$$
$$= \frac{120.2mV}{10V} \times 100$$
$$= 1.2\%$$

NOISE ERRORS

Noise errors in the unipolar mode are due primarily to the optical cavity. When the full 60kHz bandwidth is not needed, the output noise of the ISO100 can be limited by either a capacitor, C_F, in the feedback loop or by a low-pass filter following the output. This is shown in Figure 4. Noise in the bipolar mode is due primarily to the reference current sources, and can be reduced by the low-pass filters shown in Figure 5.

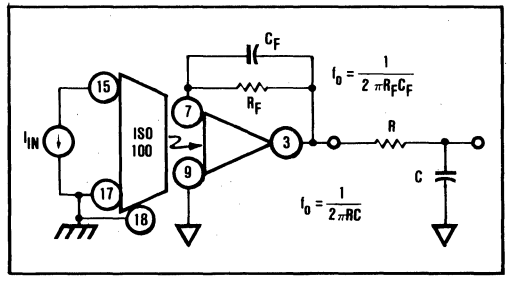


FIGURE 4. Two Circuit Techniques for Reducing Noise in the Unipolar Mode.

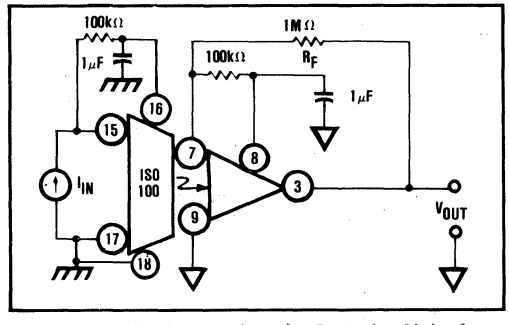


FIGURE 5. Circuit Technique for Reducing Noise from The Current Sources in the Bipolar-Mode.

OPTIONAL ADJUSTMENTS

The offset voltage of the input and output amplifiers generally need no adjustment. However, V_{OSI} and V_{OSO} can be adjusted independently using external potentiometers. An example is shown in Figure 15. Note that V_{OSO} (500μV, max) appears directly at the output, but V_{OSI} causes an error in the input current which is negligible for high source impedances. In general one pot, usually at the input is sufficient.

Adjustment Procedures: In the bipolar mode, remove I_{IN} and adjust the offset potentiometer for a zero output voltage. In the unipolar mode, set I_{IN} to the lowest expected input current, for example 20nA, and adjust the offset potentiometer for an output voltage equal to I_{IN} x R_F.

BASIC CIRCUIT CONNECTIONS

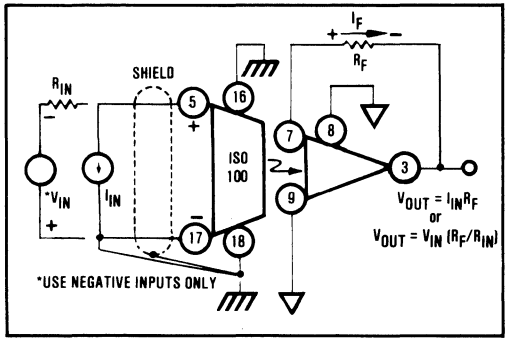


FIGURE 6. Unipolar Noninverting.

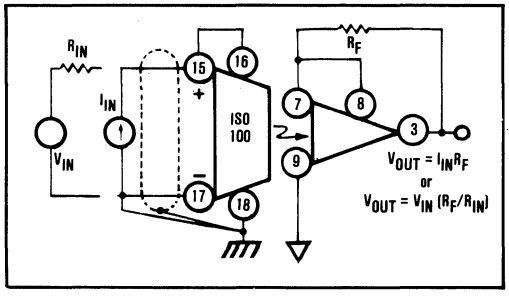


FIGURE 7. Bipolar Noninverting.

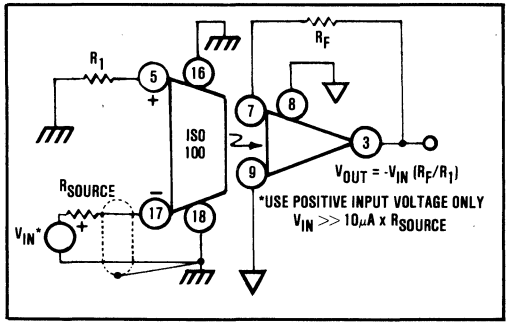


FIGURE 8. Unipolar Inverting.

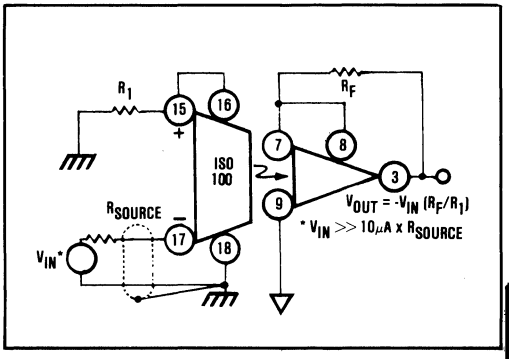


FIGURE 9. Bipolar Inverting.

APPLICATION INFORMATION

The small size, low offset and drift, wide bandwidth, ultra-low leakage, and low cost, make the ISO100 ideal for a variety of isolation applications. The basic mode of operation of the ISO100 will be determined by the type of signal and application.

Major points to consider when designing circuits with the ISO100.

1. Input Common (pin 18) and -IN (pin 17) should be grounded through separate lines. The Input Common can carry a large DC current and may cause feedback to the signal input
2. Use shielded or twisted pair cable at the input, for long lines.
3. Care should be taken to minimize external capacitance across the isolation barrier.
4. The distance across the isolation barrier, between external components, and conductor patterns, should be maximized to reduce leakage and arcing.
5. Although not an absolute requirement, the use of conformally-coated printed circuit boards is recommended.
6. When in the unipolar mode, the reference currents (pins 8 and 16) must be terminated.
7. The noise contribution of the reference currents will cause the bipolar mode to be noisier than the unipolar mode.
8. The maximum output voltage swing is determined by I_{IN} and R_F.

$$V_{SWING} = I_{IN_{max}} \times R_F$$

9. A capacitor (about 3pF) can be connected across R_F to compensate for peaking in the frequency response. The peaking is caused by the pole generated by R_F and the capacitance at the input of the output amplifier.

Figures 10 through 16 show applications of the ISO100.

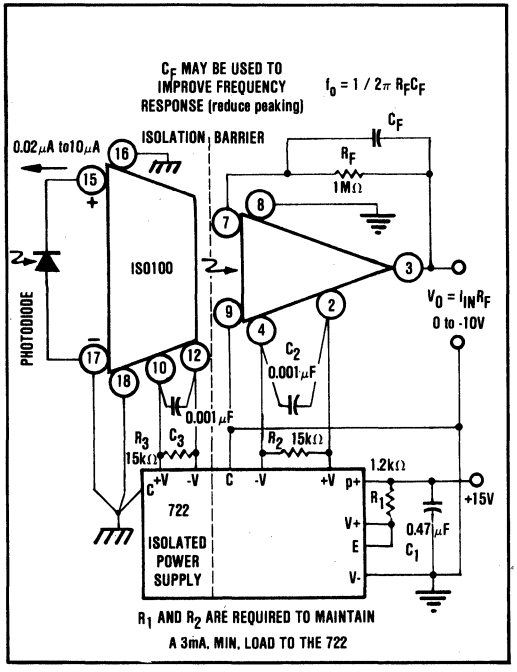


FIGURE 10. Two-Port Isolation Photodiode Amplifier (Unipolar).

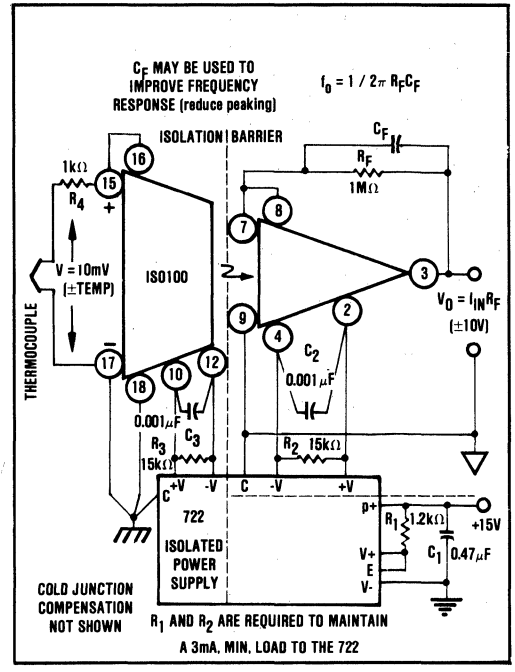
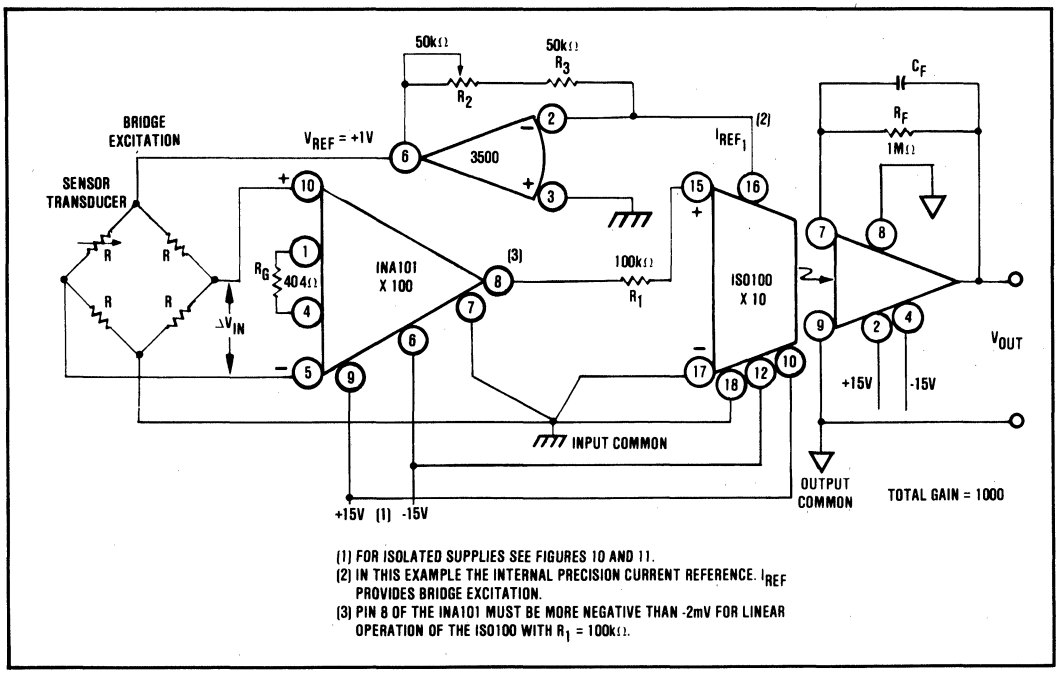


FIGURE 11. Three-Port Isolation Thermocouple Amplifier (Bipolar).



(1) FOR ISOLATED SUPPLIES SEE FIGURES 10 AND 11.
(2) IN THIS EXAMPLE THE INTERNAL PRECISION CURRENT REFERENCE. I_{REF} PROVIDES BRIDGE EXCITATION.
(3) PIN 8 OF THE INA101 MUST BE MORE NEGATIVE THAN -2mV FOR LINEAR OPERATION OF THE ISO100 WITH R_1 = 100kΩ.

FIGURE 12. Precision Bridge Isolation Amplifier (Unipolar).

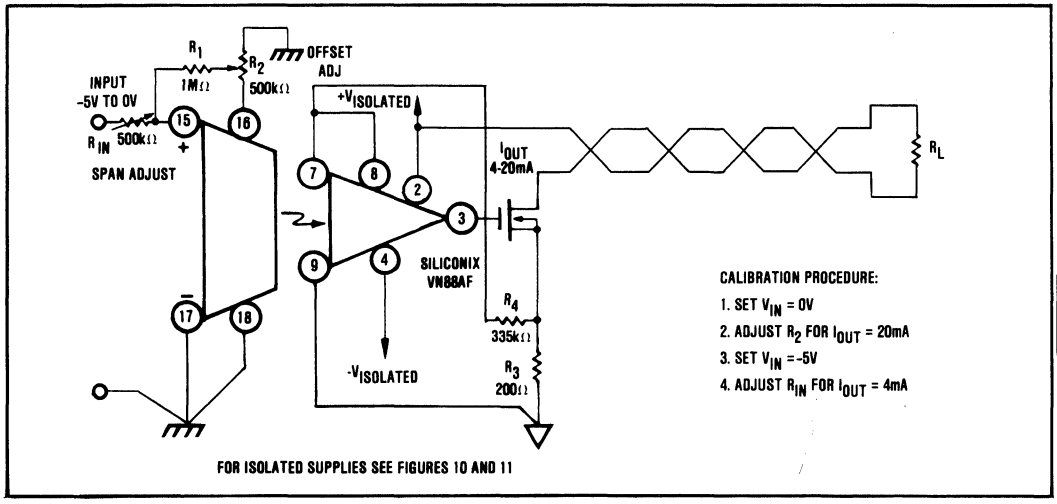


FIGURE 13. Isolated 4mA to 20mA Transmitter (Example of an isolated voltage controlled current source).

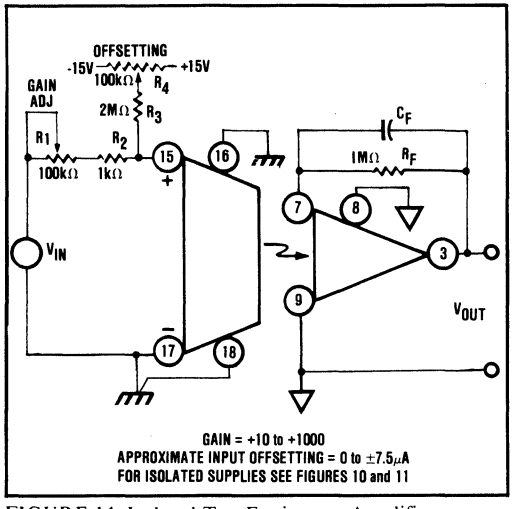


FIGURE 14. Isolated Test Equipment Amplifier (Unipolar with Offsetting).

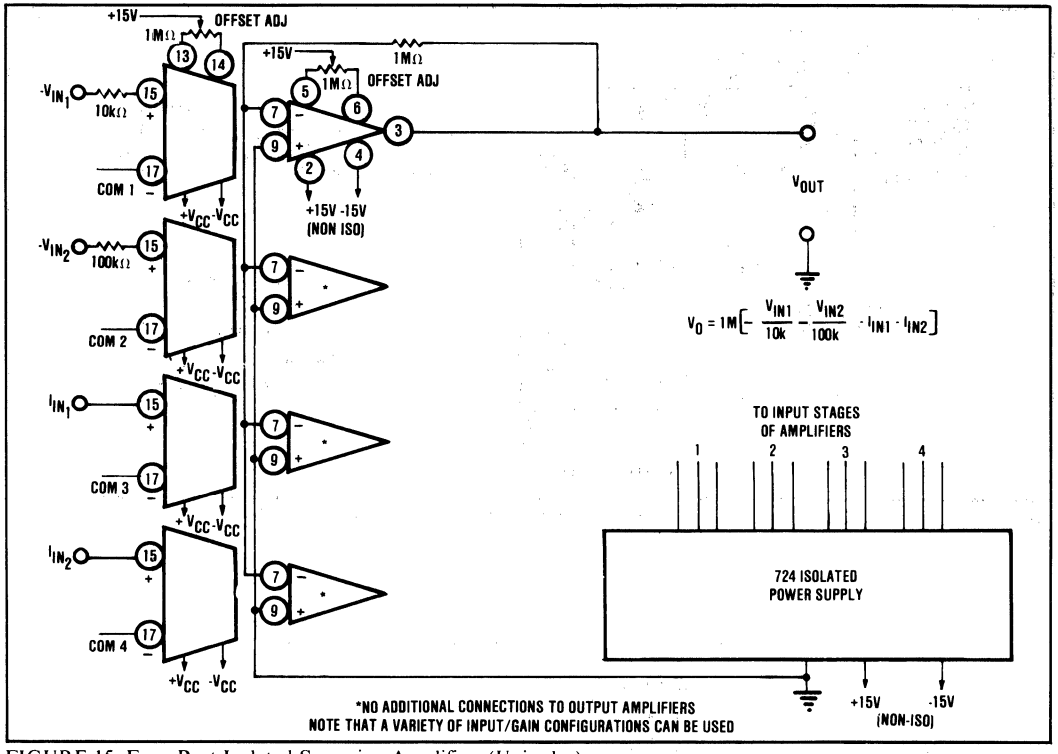


FIGURE 15. Four-Port Isolated Summing Amplifier (Unipolar).

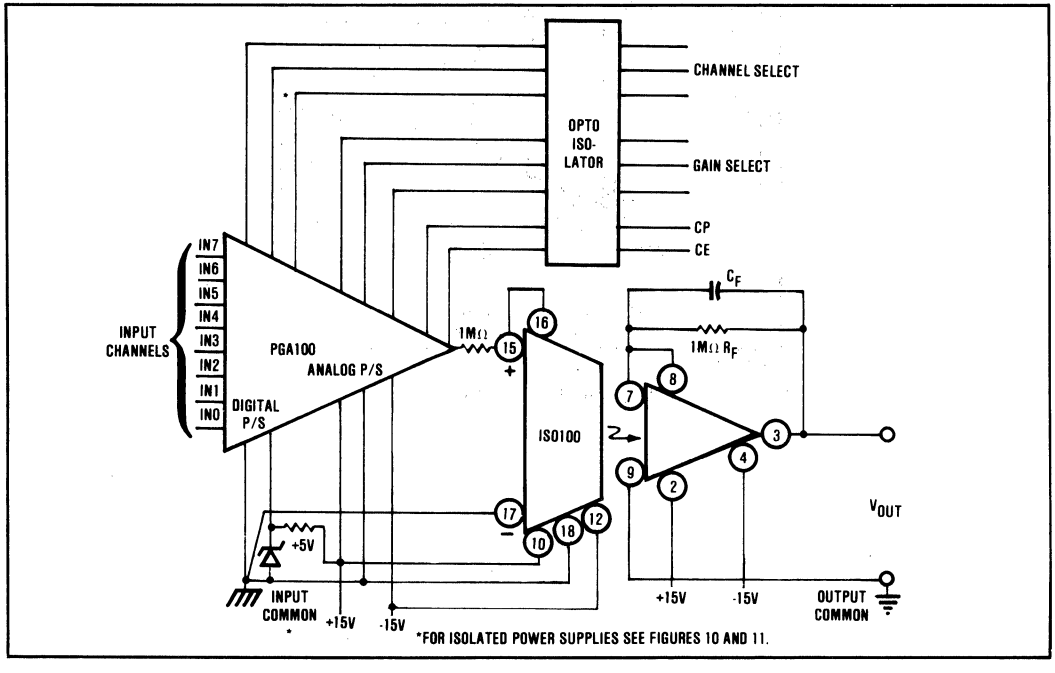
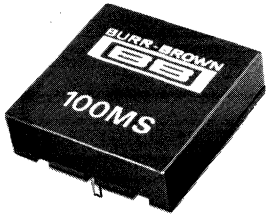


FIGURE 16. Multiple Channel Isolation Amplifier (Bipolar) with Programmable Gain (Useful in Data Acquisition Systems).

BURR-BROWN



100MS

EMI SHIELD

DESCRIPTION

The 100MS is an epoxy encapsulated electromagnetic electrostatic interference (EMI) shield for use with circuits where sensitivity to EMI is critical. It was designed to attenuate EMI by converting electromagnetic field energy into heat that is absorbed by the shield and by shunting electrostatic fields to common. The 100MS may be used in applications to either confine or exclude EMI. Its cavity was designed for 28.45mm x 28.45mm x 7.24mm, 20-pin hybrid packages. The shields in the cover and base plate are in two separate halves to maintain the electrical isolation between the adjacent rows of pins of the module it encloses. Because of the spacing between the shield halves and the epoxy flow holes, the 100MS provides a partial, but adequate low reluctance path for electromagnetic flux. The 100MS is well suited for use with isolation modules such as the Burr-Brown 3656, 722, and 724.

ASSEMBLY INSTRUCTIONS

Assemble the base plate to the module by pushing the pins of the module through the beveled holes in the base plate until the base plate and bottom of the module are in contact with each other. Place the cover over the module so the tabs are aligned and fit into the slots in the base plate. Bend the four wide shield soldering tabs protruding from the cover to make contact with the bare metal on the base plate. Solder these four tabs to insure the integrity of their connection to the base plate.

The 100MS and the module it contains are mounted and secured to a printed circuit board (PCB) by soldering the two narrow PCB solder tabs to the appropriate common. The PCB solder tab closest to the input side of the module should be soldered to the input common. The other tab should be soldered to the output common. Figure 2 illustrates the assembly of the 100MS.

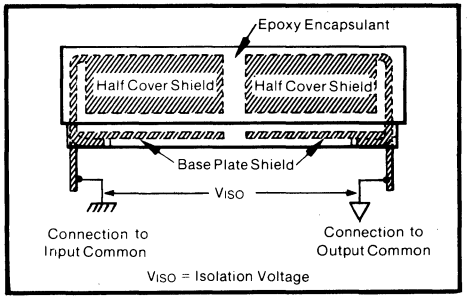


FIGURE 1. Cross-Sectional Side View of 100MS.

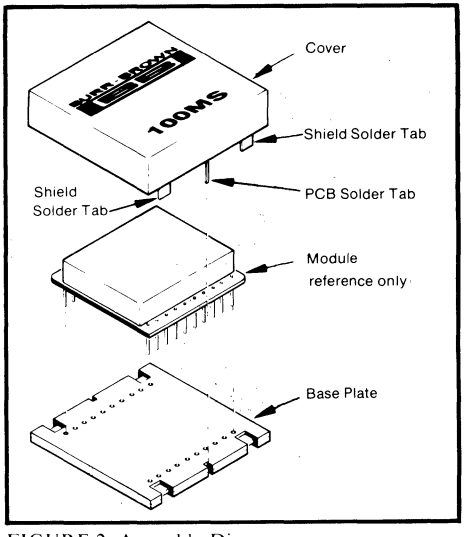


FIGURE 2. Assembly Diagram.

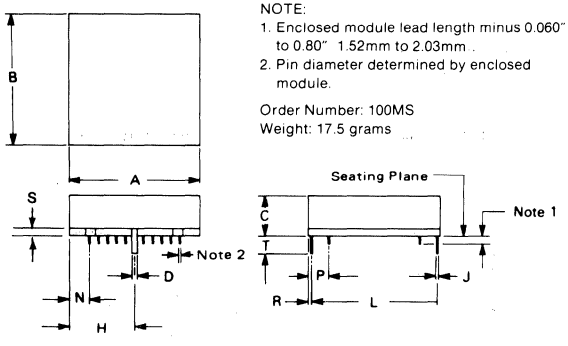
International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL - Specifications apply between solder tabs.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Isolation Voltage					
Rated Continuous, DC		3500			VDC
Rated Continuous, AC		2000			V, rms
Test	10 seconds	8000			VDC
Capacitance			5		pF
Resistance			10^{10}		Ω
Leakage Current	120V, 60Hz		0.23		μA

MECHANICAL



NOTE:
1. Enclosed module lead length minus 0.060" to 0.80" 1.52mm to 2.03mm.
2. Pin diameter determined by enclosed module.

Order Number: 100MS
Weight: 17.5 grams

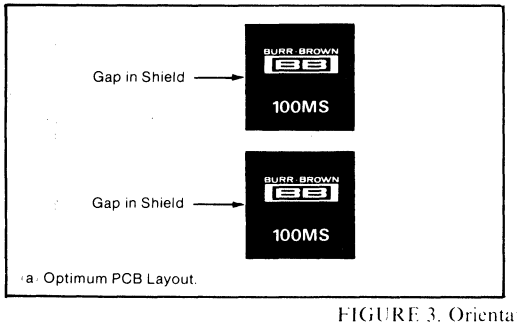
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.320	1.380	33.53	35.05
B	1.320	1.380	33.53	35.05
C	.350	.450	8.89	11.43
D	.040	.060	1.02	1.52
H	.600	.700	15.24	17.78
J	.015	.025	0.38	0.64
L	1.180	1.280	29.97	32.51
N	.150	.250	3.81	6.35
P	.150	.250	3.81	6.35
R	.015	.055	0.38	1.40
T	.130	.230	3.30	5.84
S	.060	.080	1.52	2.03

APPLICATIONS INFORMATION

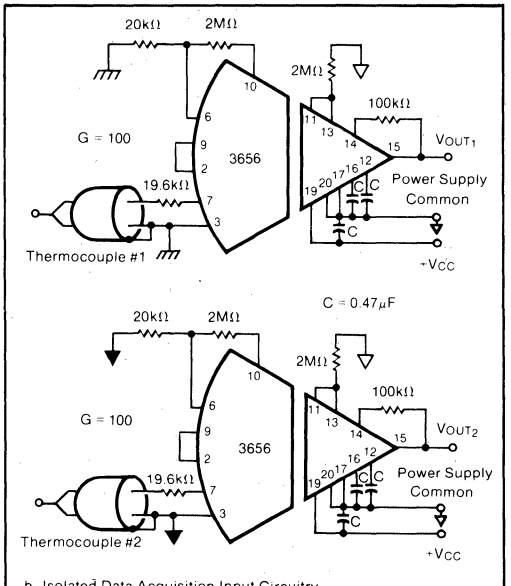
MULTIPLE DEVICE ORIENTATION

A typical application for the 100MS is shown in Figure 3. Using multiple devices within 30mm of each other can cause them to interact by forming beat frequency interference outputs. The 100MS can reduce this interference by as much as a factor of 200:1 depending on the distance between the devices and their relative orientation.

Minimum EMI results when the gaps of both shields are paralleled as in Figure 3a.



a. Optimum PCB Layout.



b. Isolated Data Acquisition Input Circuitry.

FIGURE 3. Orientation for Minimum EMI.

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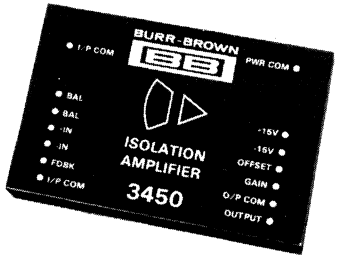


3450
3451
3452
3455

Precision Linear ISOLATION AMPLIFIERS

FEATURES

- 2000V ISOLATION (3452)
- 160dB ISOLATION-MODE REJECTION
- DIFFERENTIAL INPUT
- 0.005% GUARANTEED GAIN LINEARITY (3450)
- 1μV/°C INPUT VOLTAGE DRIFT (3450)
- 20pA INPUT BIAS CURRENT (3452)
- PRECISION WIRE-WOUND RESISTORS FOR LONG TERM STABILITY
- LOW INTERFERENCE PICKUP-PW MODULATION

DESCRIPTION

The Models 3450, 3451 and 3452 are operational amplifiers with the unique feature of having the output completely isolated from the input. This is accomplished by a high accuracy modulation/demodulation stage which isolates the input from the output by $10^{12}\Omega$ in parallel with 12 pF of coupling capacitance and provides gain linearity and stability far superior to that offered by ordinary isolation amplifiers.

These devices differ from other isolation amplifiers in several respects. They are true differential input operational amplifiers where as other commercially available isolation amplifiers are simple unity-gain isolators or are capable of a few fixed gains. Thus they can be connected in all of the common op amp feedback circuits such as summing, inverting, differentiating, etc.

The 3452 differs from the 3450 and 3451 in that it has higher isolation voltage (2000 volts vs 500 volts) and has isolated ± 15 Vdc power available at the input.

The 3450 and 3451 differ from each other primarily in their input stage characteristics. The 3450 has a low drift (1 μV/°C) bipolar transistor input stage while the 3451 has a low bias current (25 pA) FET transistor input stage. The 3455 is identical to the 3452 except for additional isolation specifications more well suited for medical applications.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

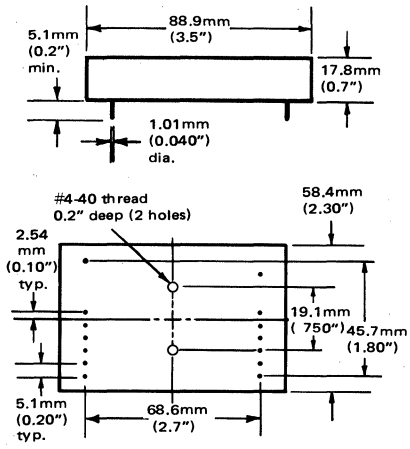
SPECIFICATIONS

Typical at 25°C and ±15 Vdc unless otherwise noted.

ELECTRICAL

MODEL		3450	3451	3452/3455(6)
INPUT STAGE SPECIFICATIONS (1)				
Open Loop Gain	dB, Min.	94	88	94
Input Offset Voltage @ 25°C(4)	mV, Max.	±0.55	±20	±0.30
vs. Temp.	µV/°C Max.	±1.0	±50	±5.0
vs. Supply	µV/V	±50	±50	±25
vs. Time	µV/mo	±10	±100	
Input Bias Current @ 25°C	Max.	±50 nA	−25 pA	−20 pA
vs Temp.	Max.	±0.5 nA/°C	doubles/10°C	
vs. Supply		±0.2 nA/V	±1 pA/V	
Input Offset Current @ 25°C		±30 nA Max.	±2 pA	
vs. Temp.	Max.	±0.3 nA/°C	doubles/10°C	
vs. Supply		±0.1 nA/V	±0.5 pA/V	
Input Impedance				
Differential		$10^7\Omega$	$10^{11}\Omega$	
Common Mode (2)		$5\times10^9\Omega \parallel 10pF$	$10^{11}\Omega \parallel 10pF$	
Input Noise				
Voltage, .01 Hz - 10 Hz	µV, p-p	0.8	2	4
10 Hz - 1 kHz	µV rms	1.2	3	2
Current, .01 Hz - 10 Hz	pA, p-p	30	0.3	0.3
10 Hz - 1 kHz	pA, rms	50	0.6	0.6
Input Voltage Range				
Common Mode (2) (operating)	V, Min.		±10	
Differential (w/o damage)	V, Min.		±15	
Common Mode (2) Rejection	dB @ 10V	100	80	90
Isolated Power Available				
Voltage		—	—	±15V +0 −10%
Current,	Max.	—	—	±10mA
Ripple @ 100 kHz		—	—	100 mV p-p
ISOLATION STAGE SPECIFICATIONS				
Gain (without trimming) (4)	1 V/V, ±Max	±0.1%	±0.5 %	
vs. Temp.	ppM/°C Max	±10	±50	
Nonlinearity(7) @ ±10V % Max/typ		±.005/±0.0015	±0.025/±.005	±0.025/±.005
Frequency Response, -3 dB (See Fig. 9)		1.5 kHz	2.5 kHz	
Settling Time				
to 0.01%			5 msec	
to 0.1%			1 msec	
Isolation Impedance(3)			$10^{12}\Omega \parallel 16$ pf	
Isolation Leakage Current at 240V/60Hz			2.5µA max(6)	
Isolation Mode(3) Rejection, G = 10				
DC			160 dB Min.	
60Hz			120 dB Min.	
Isolation(3) Voltage				
Rated, continuous, (min.)		±500 V Peak		±2000Vpk
Test voltage(5)		±2000V Peak		±5000Vpk(6)
Output Voltage			±10 V Min.	
Output Current			±5 mA Min.	
Output Impedance, DC			0.2 Ω	
Output Noise				
.01 Hz to 10 Hz			7 µV p-p	
10 Hz to 1 kHz			25 µV rms	
Output Offset Voltage @ 25°C(4)	mV, Max.	±2	±5	±5
vs. Temp.			±100µV/°C Max.	
vs. Supply			±500µV/V	
vs. Time			±100µV/Mo	
Input Power Requirements				
Voltage			±14 to ±16 VDC	
Current, quiescent			+30/-5 mA Max.	
, full load, max.		+35/-10mA		+55/-10mA(8)
TEMPERATURE RANGE				
Specification			-25°C to +85°C	
Storage			-55°C to +95°C	
Operating			-25°C to +85°C	

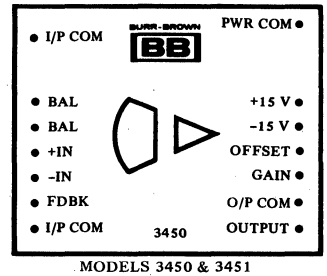
MECHANICAL



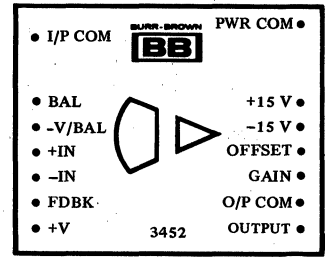
MATERIAL - Black Plastic
WEIGHT - 100g (3.5 oz)
PINS - Pin material and plating composition meet method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2]
Mating Connector - 4400MC,

PIN CONNECTIONS

(TOP VIEW)



MODELS 3450 & 3451



MODEL 3452 & 3455

1) For 3450 and 3451 current drawn from FDBK pin must be ≤ 5mA. For 3452 the sum of the current drawn from FDBK pin and either "-V/Bal" or "+V" pins (i.e., + or - isolated current) must be ≤ 11mA.
2) Common-mode parameters are measured at the +IN and -IN pins with respect to the I/P COM pin.
3) Isolation mode parameters are measured at the I/P COM pin with respect to the PWR COM pin and O/P COM pin.
4) Errors may be trimmed to zero.
5) All units 100% tested for 1µA max leakage current at test voltage.
6) The 3455 is identical to the 3452 except for two additional specifications. Each unit is tested to withstand a 2500V rms, 60 Hz sinewave isolation voltage (Ref. Dielectric Withstand Voltage, paragraph 31.11 of UL 544). Each unit is specified at a maximum leakage current of 2µA with 240V rms, 60 Hz isolation voltage (Ref. Leakage Current, paragraph 27.5 of UL 544).
7) Nonlinearity is specified to be the peak deviation from a best straightline expressed as a percent of peak-to-peak full scale output.
8) Includes fully loaded input power.

CIRCUIT DESCRIPTION

The 3450,3451 and 3452 operate on the same principle, basically that of an operational amplifier followed by a high accuracy isolation stage (Figure 1a). The high accuracy of the isolation stage is achieved by use of a proprietary feedback technique in combination with high-stability components.

Isolated DC power for the input amplifier is provided by an internal DC-DC converter which derives its power from the external +15 Vdc supply.

Although a DC-DC converter and modulation techniques are used, the output noise is typically less than 1 mV (peak) as a result of careful design, internal filtering, and a shielded package. The frequency of this noise is approximately 100 kHz which makes it insignificant for many applications. Pulse width modulation minimizes pickup from adjacent units. The symbol shown in Figure 1b is used to represent the complete isolated operational amplifier.

The O/P COM pin must be connected to the PWR COM pin. Figure 10a shows the power supply connections and the optional offset and gain trims.

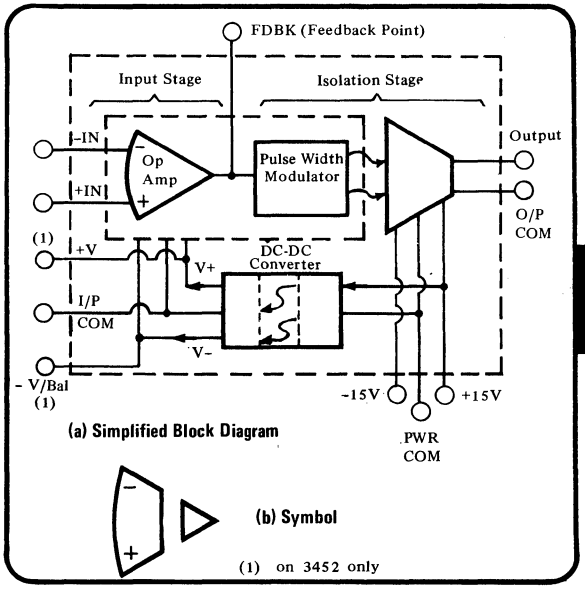


FIGURE 1. Block Diagram and Symbol

APPLICATIONS

The isolation amplifiers may be used in the same manner as any operational amplifier except that the feedback signal is taken from the FDBK pin rather than from the output pin. No connection is required or would normally be made from input common (I/P COM) to either the power common (PWR COM) or output signal ground pins. Some typical circuit applications are shown in the following.

NONINVERTING CIRCUITS

One of the most useful applications of these amplifiers is impedance buffering and pre-amplification of low-level signals. Such signals may be "riding" on several hundred volts of common mode potential or they may simply have a significant amount of common mode noise (power line "pickup," etc).

Figure 2 illustrates the correct signal and feedback connections for such noninverting circuits.

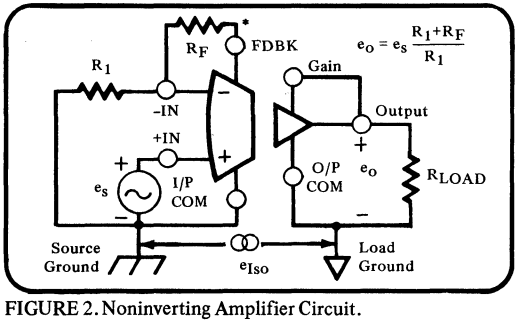


FIGURE 2. Noninverting Amplifier Circuit.

*See note (1) under Electrical Specifications.

For signal sources of millivolt levels and low internal impedance, the 3450 will usually be the best choice. Signal sources of this type include thermocouples, thermistors, etc. The 3451 will generally be the best choice for signal sources having large values of internal impedance. The pH cell is an example of this type of signal source.

INVERTING CIRCUITS

The isolation amplifiers can be used for a variety of inverting circuit applications. Figure 3 illustrates the proper circuit connections for summing a number of signals which are all at the same common mode level. An example of the use of such an amplifier is the computation of a weighted average of several temperature inputs.

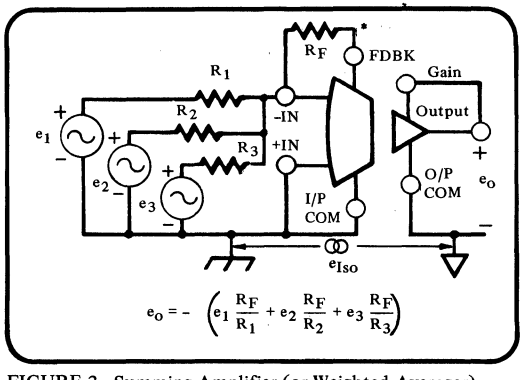


FIGURE 3. Summing Amplifier (or Weighted Averager).

DIFFERENTIAL INPUT CIRCUIT

The isolated operational amplifier can be operated in a fully differential mode as shown in Figure 4. The input impedance of the differential amplifier circuit is $2R_1$ and may cause undesirable loading of the signal source unless R_1 is much greater than the impedance of the signal sources.

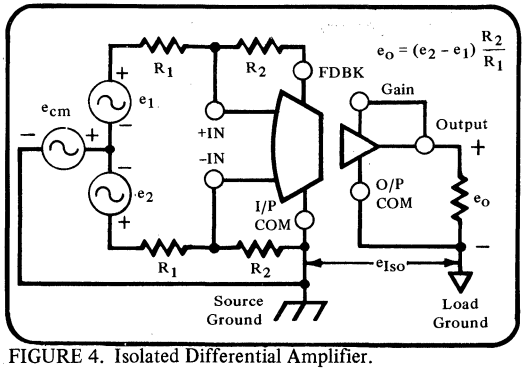


FIGURE 4. Isolated Differential Amplifier.

CURRENT AMPLIFIER

As with nonisolated operational amplifiers, the isolation amplifiers can be used to convert current source or convert current signals to output voltage. However, with these amplifiers the input signal may have a large voltage associated with it which can be completely isolated from output ground. The circuit of Figure 5 illustrates this technique.

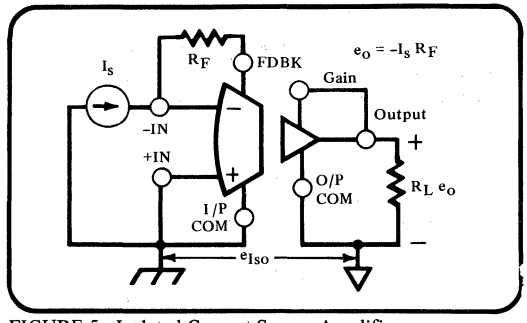


FIGURE 5. Isolated Current Source Amplifier.

BRIDGE AMPLIFIER

The circuit in Figure 6 illustrates a method of amplifying a signal from a balanced bridge which cannot be conveniently used with a nonisolated amplifier. The circuit shown provides a high input impedance so that the bridge is not loaded. The common mode rejection of the bridge excitation voltage is not degraded by the external gain setting resistors as it would be with a difference amplifier. The gain can be changed conveniently by adjusting a single resistor (R_2). Also, the whole bridge circuit may be floated with respect to the output by a voltage equal to the isolation mode voltage specification without creating troublesome ground loop current.

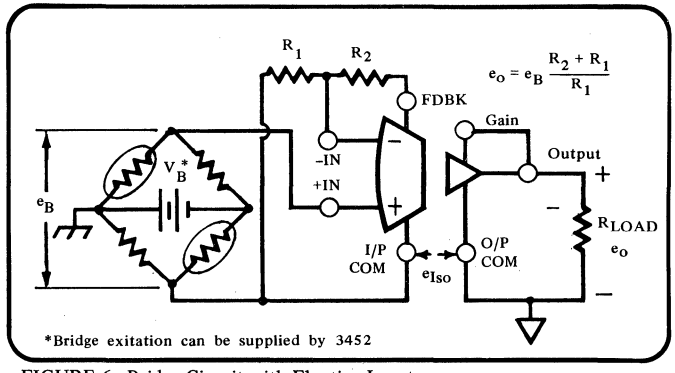


FIGURE 6. Bridge Circuit with Floating Input.

ISOLATION AMPLIFIERS USED IN MEDICAL APPLICATIONS

When isolation amplifiers are used in patient monitoring medical application the considerations of 1) patient safety and 2) protection of the amplifier against defibrillator voltages require the use of additional circuitry.

The input resistors must be kept large in order to limit the leakage current in the event of a component failure in the input stage of the amplifier. The 1.2meg. ohm resistors will limit the current to 12.5μA (Figure 7).

The amplifier must be protected in two areas against possible damage from defibrillator over voltages. Diodes D_1 through D_4 protect the input stage from excessive voltages and currents. The gas filled surge voltage protection (SVP in Figure 7) will protect the isolation barrier of the amplifier from breakdown. A Siemens part number B2-B470 will limit the voltage across the isolation barrier to 470V and has high isolation resistance and low leakage capacitance characteristics.

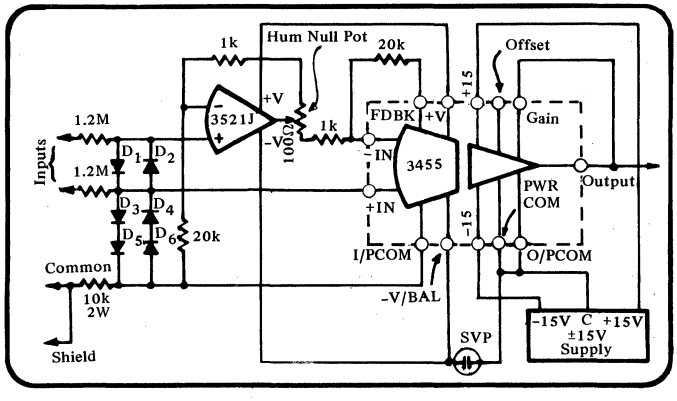


FIGURE 7. High Performance ECG Amplifier Gain = 20V/V

PERFORMANCE

OFFSET VOLTAGE and NOISE

The total error at the output of the isolation amplifiers may be computed by treating it as two amplifier stages in cascade. One stage (the input stage) has variable gain (G_1) and the other stage (the isolation stage) has a fixed gain of 1 V/V.

When this concept is applied to the circuit in Figure 2 as a typical example we see that the total DC offset voltage error at the isolation amplifier output is given by

$$V_{OS} = V_{OS_1} \times G_1 + I_B R_1 \times G_1 + V_{OS_2}$$

where V_{OS} = total offset voltage, referred to output (RTO)
V_{OS_1} = offset voltage of input stage
V_{OS_2} = offset voltage of isolation stage
I_B = input bias current
R_1 = input impedance
G_1 = gain of input stage, $\frac{R_1 + R_F}{R_1}$

A similiar expression may be used to compute the total offset voltage drift, RTO.

Total output noise may be calculated in much the same way.

$$E_N\,(\text{rms}) = \sqrt{(E_{N1} \times G_1)^2 + (I_N R_1 \times G_1)^2 + (E_{N2})^2}$$

where E_N (rms) = total noise, RTO
E_{N1} = rms voltage noise of input stage
I_N = rms current noise of input stage
E_{N2} = rms voltage noise of output stage

The rms noise specifications shown in the Electrical Specifications are for a frequency band of 10Hz - 1kHz. If the bandwidth is reduced by filtering the noise will be decreased.

FREQUENCY RESPONSE

Because the isolation amplifiers are two stage amplifiers, the frequency response of both stages in cascade must be considered in determining the overall response. The curves of Figure 9 show the frequency response of each stage. Note that the frequency response of the input stage is shown under open loop conditions: As with conventional operational amplifiers, the actual closed loop response depends on the feedback network used.

GAIN ACCURACY and STABILITY

The overall gain accuracy of the isolation amplifier is determined by the gain accuracies of its two stages. The input stage accuracy is determined by the open loop gain and the feedback network (i.e. the loop gain) as with a conventional operational amplifier. The untrimmed accuracy of the isolation stage is given in the Electrical Specifications. Since these can be trimmed to zero the fundamental limitation on gain accuracy is the linearity and gain drift. When these limitations are considered the isolation amplifiers are quite capable of achieving gain accuracies of 0.01% and 0.1%. The achievement of such accuracies, as always, requires the use of high quality feedback components (such as wire-wound resistors) and careful calibration techniques (see Calibration Adjustments).

COMMON MODE REJECTION and ISOLATION MODE REJECTION

The use of the common mode rejection (CMR) and isolation mode rejection (IMR) specifications to calculate their respective error contribution is illustrated in Figure 8.

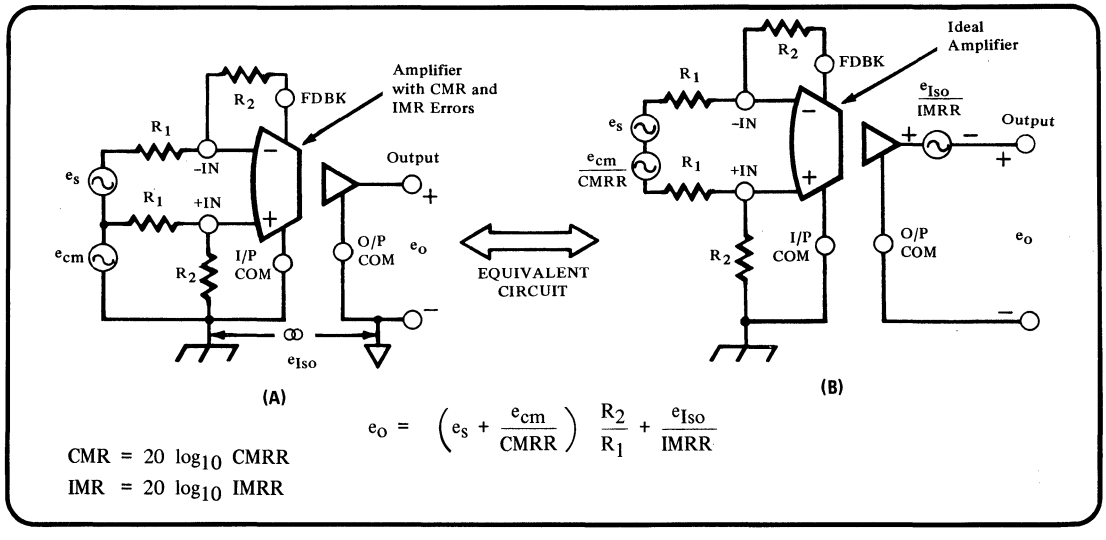


FIGURE 8. Common Mode and Isolation Mode Voltage Errors.

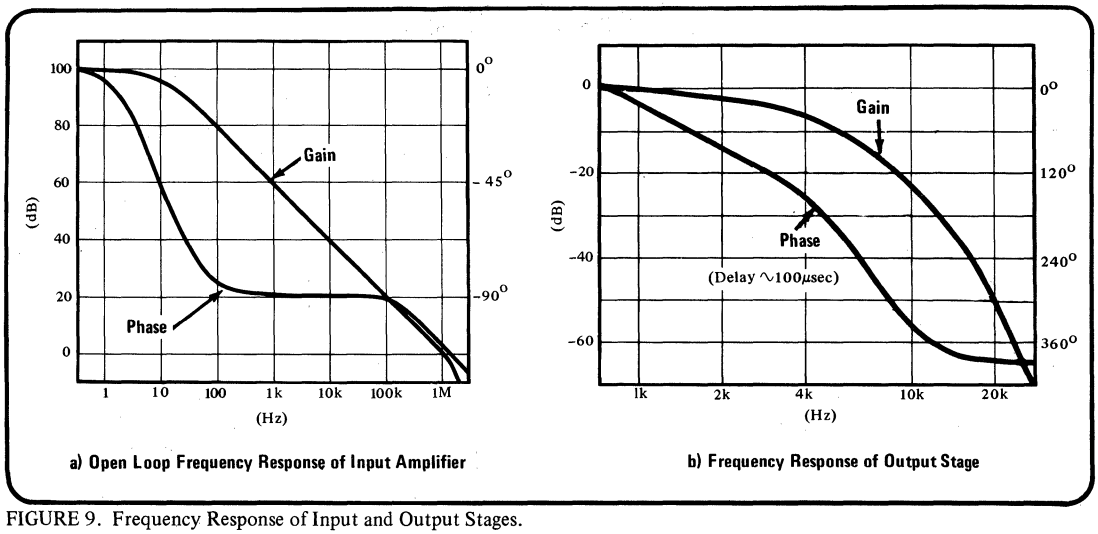


FIGURE 9. Frequency Response of Input and Output Stages.

INSTALLATION and OPERATING INSTRUCTIONS

MOUNTING

The isolation amplifiers are plastic cased modules suitable for soldering directly on to a printed circuit board. Alternatively they may be plugged into the 4400 MC mating connector which may be mounted on a panel or chassis.

POWER SUPPLY REQUIREMENTS

The isolation amplifiers have no unusual power supply requirements. A standard low-cost power supply such as the Burr-Brown 551 is recommended. The necessary isolated power for the input stage of the amplifier is derived internally by a DC-DC Converter operating from the externally applied +15VDC power.

CALIBRATION ADJUSTMENTS

Gain of the isolation amplifiers is determined primarily by the operational amplifier input stage. This allows a wide range of possible gains with the accuracy determined primarily by the feedback networks and the open loop gain of the operational amplifiers. $R_F \geq 10$ k is recommended for best linearity. The gain of the isolation stage is nominally unity but may be trimmed over a limited range to allow easy calibration.

Offset voltages of both input and output stages are adjustable by use of external components.

Figure 10 illustrates a typical amplifier circuit where gain and offset voltages are adjusted. Proper calibration procedure for this circuit would normally be as follows:

ISOLATION STAGE OFFSET VOLTAGE NULL

Set input signal to zero (connect +IN to I/P Com) connect I/P Com to O/P Com and measure the voltage between the FDBK and OUTPUT pins with a floating DVM. Null this voltage by adjusting R4. Remove the connection between I/P Com and O/P Com.

INPUT STAGE OFFSET VOLTAGE NULL

With the input signal set to zero, adjust R5 such that the voltage between the FDBK and I/P Com pins is zero. (This is best done at a high gain value i.e. $\frac{R_G + R_F}{R_G} \cong 1000$).

OVERALL GAIN ACCURACY

With R_F and R_G at the proper values to produce the desired gain $G = \frac{R_G + R_F}{R_G}$, apply a known calibration voltage V_R as the input signal. Adjust R_3 for the desired output $V_O = V_R \times G$.

If it is unnecessary to adjust offset voltage of the output stage, R_1 and R_4 may be omitted. If no adjustment of input stage offset voltage is desired, omit R_5 and R_6. If the specified gain accuracy (see spec table) is adequate without further adjustment, both R_2 and R_3 may be omitted. The OUTPUT pin must then be connected to the GAIN pin for an output stage gain of unity. Omit R_7 if R_1 through R_4 omitted.

For all applications other than unity gain noninverting, R_2 is unnecessary and only R_3 is needed to trim the gain. However, it is then necessary to set the first stage gain slightly below the desired overall value and then use R_3 for the gain calibration.

For fixed gain applications it may be unnecessary to null offset voltage for both input and output stages. The offset voltage of the output stage, for instance, may be used to compensate for the input stage offset, thus giving an overall null. However, if gain is to be varied over a wide range it will usually be necessary to null both offset voltages.

Appropriate safety precautions should be taken when adjusting input stage offset voltage or gain. These points will be "floating" at the isolation mode voltage and appropriate precautions must be taken if this is a high voltage. In particular, any adjustment potentiometers used for input stage adjustment should have insulated shafts with voltage ratings in excess of any expected common mode potential.

The output stage can be adapted to drive capacitive load of up to 10,000 pF without sacrificing DC gain accuracy. Add R_8 = 100Ω as shown in Figure 10b; otherwise, R_8 = 0Ω.

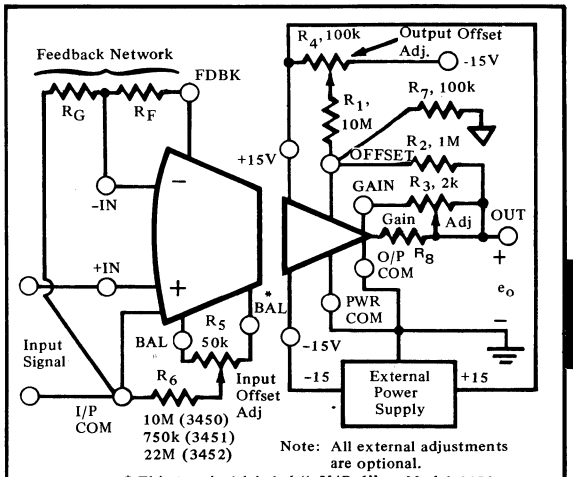


FIGURE 10a. External Connections for 3450, 3451 and 3452

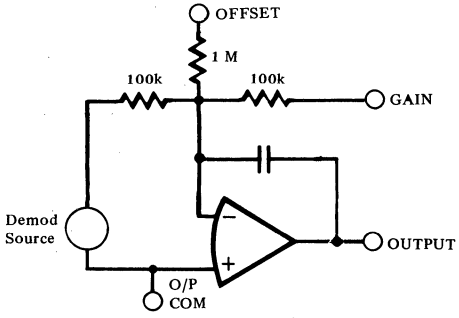


FIGURE 10b. Equivalent Circuit of O/P Stage.

WIRING SHIELDING and ISOLATION MODE REJECTION

The capacitive coupling from input common (I/P COM) to output common (O/P COM) for the isolation amplifiers is extremely low. This is an essential element in achieving the isolation mode rejection specifications. Therefore it is essential that care be used in wiring and printed circuit card layout to minimize stray capacitance between input and output circuits.

Proper shielding of input leads is also essential in preserving isolation mode rejection. When shielded cable is used the shield should be connected to the common mode potential at the signal-source.

Isolation mode rejection at high frequencies will be degraded by resistance in series between the signal source and the I/P COM pin (e.g. wire resistance). Figure11 illustrates the mechanism by which such degradation occurs. The isolation mode voltage "divides" across R_W and C_C creating an isolation mode error voltage Δe_{Iso} which appears as an unwanted differential input voltage adding to e_s. Note that this error occurs even if R_N and R_W are equal because the stray capacitance C_C exists only from the I/P COM pin to O/P COM. If this degradation of the isolation mode rejection becomes significant (for R_W = 1 kΩ and f = 60 Hz, the CMR is still in excess of 97 dB) a capacitance from the +IN pin to O/P COM will compensate the effect. A capacitor used in this manner must withstand whatever isolation mode potential exists.

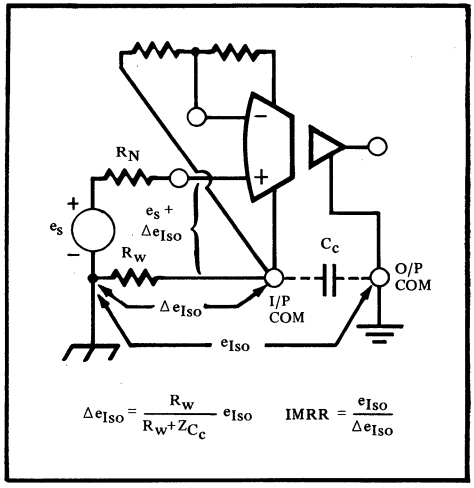


FIGURE 11. Degradation of Isolation Mode Rejection due to Wiring Impedance and Coupling Capacitance.

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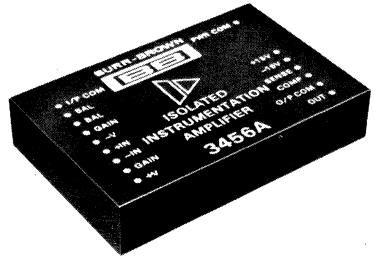

3456

ISOLATED INSTRUMENTATION AMPLIFIER

FEATURES

- TRUE 3-WIRE INSTRUMENTATION AMPLIFIER INPUT
- TRUE INSTRUMENTATION GRADE ISOLATION AMPLIFIER
- 1μV/°C INPUT VOLTAGE DRIFT
- ADJUSTABLE GAIN, 1 to 1000
- LOW NONLINEARITY, 0.02% max
- ISOLATION VOLTAGE, 2000V PEAK RATED CONTINUOUS
- 160dB ISOLATION-MODE REJECTION
- ±20mA, VOLTAGE OR CURRENT PROGRAMMABLE OUTPUT
- 2.5kHz, FREQUENCY RESPONSE
- LOW INTERFERENCE PICKUP-PW. MODULATION
- FULLY SELF-CONTAINED

APPLICATIONS

- ISOLATED THERMOCOUPLE & RTD SENSING
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT AND INSTRUMENTS
- HIGH VOLTAGE INSTRUMENTATION AMPLIFIER
- CURRENT SHUNT MEASUREMENTS
- GROUND-LOOP ELIMINATION
- BIOMEDICAL PATIENT MONITORING

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PDS-377

DESCRIPTION

The Models 3456A and 3456B are high performance instrumentation amplifiers which have their outputs completely isolated from the input. The front end of the unit is a high performance, DC differential-input instrumentation amplifier stage, designed for data acquisition and instrumentation use. The low drift, low noise and high CMR make it possible to accurately amplify microvolt-level signals with gains of up to 1000. The input stage is followed by a high accuracy unity gain, pulse width modulation/demodulation isolation stage. This isolation stage isolates its input from the output by $10^{12}\Omega$|| 14 pF impedance. The 3456A and 3456B differ from other isolation amplifiers in several respects. They are true instrumentation amplifiers as opposed to differential input op amps or fixed gain isolators. They offer both, the single resistor programmable gain range as well as the true 3 wire instrumentation amplifier input.

THEORY OF OPERATION

Figure 1 shows block diagram of 3456. The true 3 wire instrumentation amplifier input section shown needs only one resistor to set the required gain level. It has high input impedance, high CMR and low bias current and allows the use of inverting, non-inverting and differential input configurations. The input offset adjustment shown is optional.

Isolated DC power for the input stage is provided by an internal DC/DC converter which derives its power from the external +15 VDC supply. The isolated power is also made available (on +V and -V pins) for external use.

The modulation/demodulation stage isolates the input from the output by $10^{12}\Omega$ in parallel with 14 pF of coupling capacitance. Pulse width modulation technique is used to minimize pickup from adjacent units. This technique combined with the use of wirewound and laser trimmed thin-film resistors provides high overall accuracy and excellent drift characteristics.

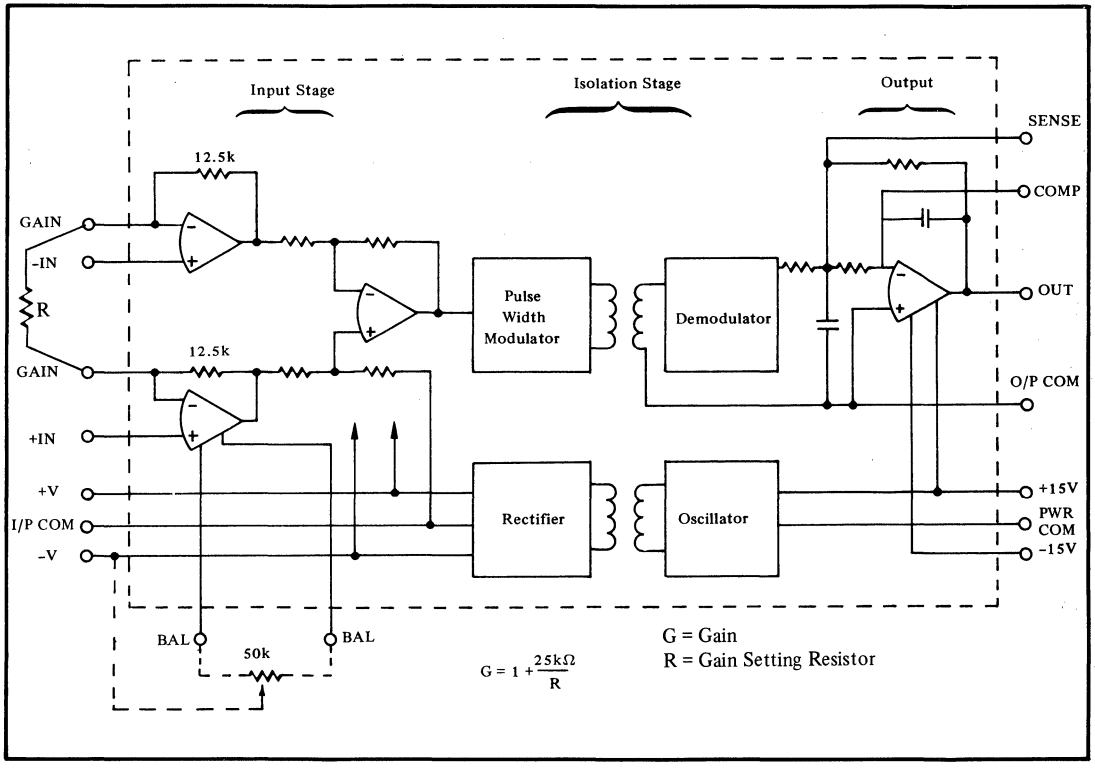


FIGURE 1. 3456 BLOCK DIAGRAM

SPECIFICATIONS

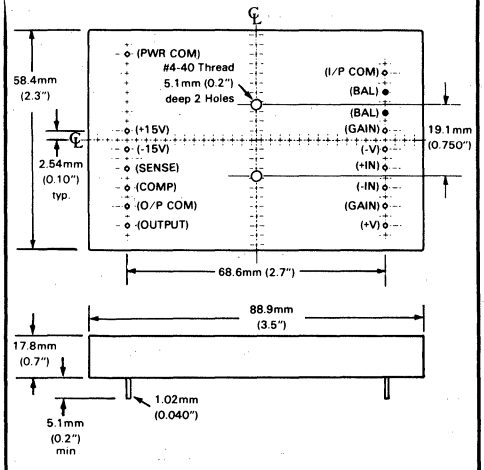
Typical at 25°C and ±15VDC supply voltage unless otherwise noted.

ELECTRICAL

MODEL	3456A	3456B
GAIN		
Gain Equation	$G = 1 + \frac{25k\Omega}{R}$	
Range of Gain	1 - 1000	
Gain Nonlinearity at G ⩽ 100	±0.01% typ., ±0.02% max	
⩽ 1000	±0.03% typ., ±0.08% max	
Gain Accuracy at G ⩽ 100	±0.2% max	
G ⩽ 1000	±0.5% typ.	
Gain vs Temperature at G ⩽ 100	10 ppm/°C	
at G = 1000	50 ppm/°C	
INPUT		
Input Impedance - Differential	$10^7\Omega$ ‖ 3 pF	
Common-mode	$5 \times 10^9\Omega$ ‖ 3 pF	
Input Voltage Range[1]	±10V	
Absolute max	±Isolated Supply	
Common-mode Rejection, DC-100Hz		
at G = 1.5kΩ source unbal.	80dB, min	
at G = 100, 0Ω balanced source	110dB	
Input Bias Current, Initial	±50nA, max	
vs Temperature	0.3nA/°C typ, 0.6nA/°C, max	
vs Supply	±0.2nA/V	
Input Noise		
Voltage, 0.01Hz - 10 Hz	1.5μ p-p	
10Hz - 1.0kHz	1.4μV rms	
Current, 0.01Hz - 10Hz	200pA p-p	
10Hz - 1.0kHz	50pA rms	
ISOLATED POWER		
Voltage - No load	±15.3V, max	
Voltage - ±10mA	±13.5V, min	
Current	±10mA, max	
Ripple at 100kHz	100mV, p-p	
TOTAL OFFSET VOLTAGE		
Initial[2]	±(0.5 + 5/G)mV max	±(0.25 + 2/G)mV max
vs Temperature	±(2 + 150/G)μV/°C max	±(1 + 75/G)μV/°C max
vs Supply	±(30 + 500/G)μV/V	
vs Time	±(3 + 100/G)μV/mo	
ISOLATION		
Isolation Impedance[3]	$10^{12}\Omega$ ‖ 14 pF	
Isolation Mode Rejection, DC	160dB + I/P Gain (dB)	
,60Hz	130dB + I/P Gain (dB), min	
Isolation Voltage, Rated Continuous	±2000V Peak	
Test Voltage[4]	±5000V Peak	
FREQUENCY RESPONSE		
-3dB Response at G ⩽ 400	2.5kHz	
-3dB Response for 400 ⩽ G ⩽ 1000	2.5kHz to 1kHz	
Setting Time to 0.01%	5msec	
to 0.1%	1msec	
OUTPUT		
Output Voltage	±10V at ±20mA, min	
Output Impedance, DC	0.04Ω	
Short Circuit Current, Duration	40mA, unlimited	
Output Noise, 0.01Hz - 10Hz	15μV p-p	
1Hz - 1kHz	25μV rms	
POWER SUPPLY		
Voltage	±14 to ±16VDC	
Current, Quiescent	+40/-8mA, max	
Full Load[5]	+85/-30mA, max	
TEMPERATURE RANGE		
Specification	-25°C to +85°C	
Operating	-25°C to +85°C	
Storage	-55°C to +95°C	

MECHANICAL

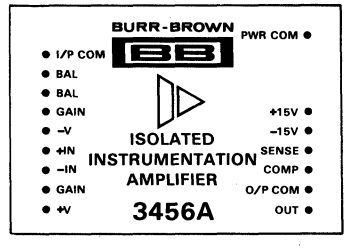
(BOTTOM VIEW)



MATERIAL: Black Plastic
WEIGHT: 100 grams (3.5 oz.)
PINS: Pin material and plating composition meet method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 4400MC

PIN CONNECTIONS

(TOP VIEW)



NOTES:
1. The ±10V input range is subject to the limitation that $|V_{common\ mode}| + |\text{Gain} \times V_{diff}/2| \leqslant 10V$.
2. Both the components (input and output) of the offset voltage may be trimmed to zero.
3. Isolation mode parameters are measured at the I/P COM pin with respect to the PWR COM pin.
4. All units are 100% tested for 25μA maximum leakage at test voltage.
5. Includes full isolated power supply.

VOLTAGE OUTPUT CONFIGURATION

The 3456, when connected as shown in Figure 2, will provide output signal capable of driving up to ±20mA load. Refer to the block diagram shown in Figure 2. Notice that the demodulated signal is referenced to the O/P COM pin. The O/P COM pin is connected to the output ground (PWR COM) for voltage output configuration as is shown in Figure 2. So with this configuration, the demodulated voltage signal is fully applied across the load impedance Z_L.

If roll-off at a lower frequency (lower than 2.5kHz) is desired, an optional compensation capacitor C_C may be connected as shown between the COMP pin and the OUT pin. See Figure 4 for the selection of C_C. The output offset controls shown in Figure 2 and Figure 3 are optional. They provide approximately ±15mV offset control at the output.

The SENSE and COMP pins are subject to electrostatic noise pick-up via stray capacitance. To minimize this noise pick-up these pins and connected circuits should be shielded. If these controls are not used, we recommend the unused pins be cut off flush to the 3456 surface. This would help minimize the degradation of Isolation Mode Rejection.

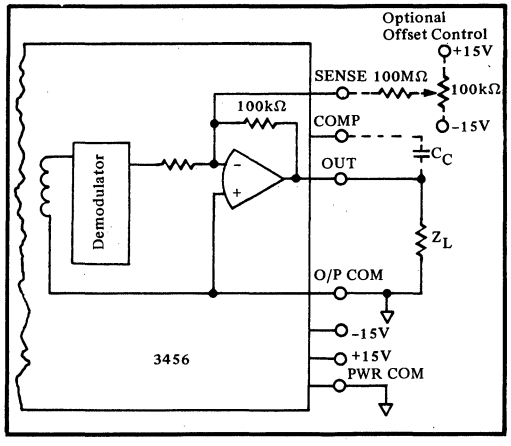


FIGURE 2. Voltage Output Configuration With Simplified Block Diagram.

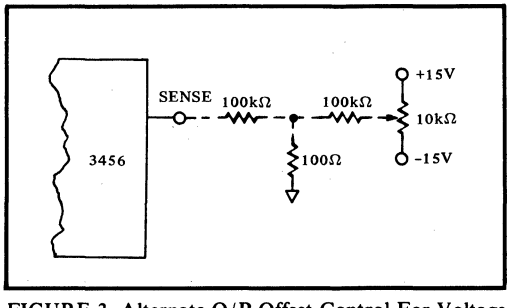


FIGURE 3. Alternate O/P Offset Control For Voltage Output Configuration.

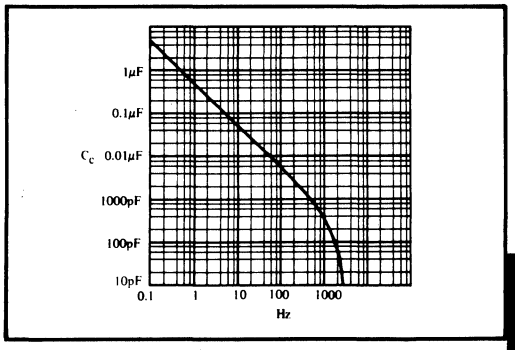


FIGURE 4. -3dB Frequency Vs C_C (Voltage Output).

ALTERNATE GAIN ADJUSTMENT

The gain adjustments are normally made by varying the gain setting resistor at the input. Since voltages at high potential may be present at the input side of the isolation barrier, some applications may require that gain adjustments or gain trimming be done at the output side of the isolation amplifier. For the voltage output configuration, such gain trimming can be done at the output. Figure 5 shows a recommended gain adjustment method. This method would provide a ±1% gain trim at the output.

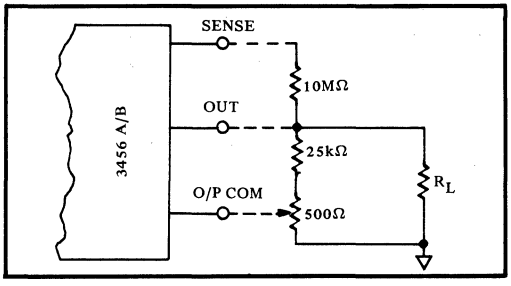


FIGURE 5. Alternate Gain Adjustment Method For Voltage Output Configuration.

CURRENT OUTPUT CONFIGURATION

Current output configuration is a configuration which gives an output current proportional to the input signal. The 3456 should be connected as shown in Figure 6 for current output configuration. In this configuration, the O/P COM pin is not connected to the output ground (PWR COM). The O/P COM pin is connected to R_L. The demodulated signal (voltage between the OUT pin and O/P COM pin) is thus applied across R_S. With a given demodulated signal and known feedback for the output amplifier, the voltage across R_S can be calculated. With known value of this voltage, the value of R_S can be fixed to give the desired output current to the load resistor R_L. The output current is thus programmed by R_S. It does not change with changes in the load resistor R_L. The feedback resistor R_F paralleled with the internal 100kΩ resistor (see Figure 6) helps achieve the required voltage rescaling at the output (the OUT pin).

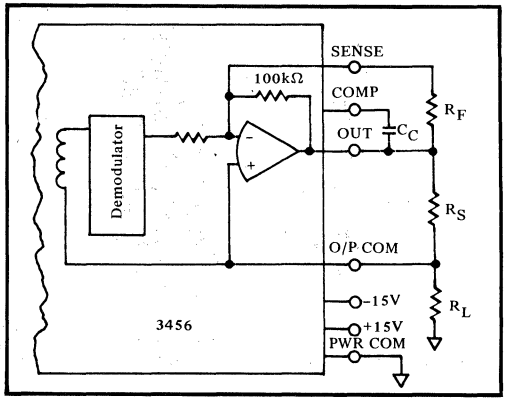


FIGURE 6. Current Output Configuration With Simplified Block Diagram

PROGRAMMING FOR CURRENT OUTPUT

The selection criteria discussed below is based on 3456 being gain programmed for ±10V full scale signal at the OUT pin (the signal as referenced to the PWR COM pin). With ±10V full scale signal, best overall accuracy is achieved.

R_L is defined as the maximum load impedance in ohms and I_o as the maximum peak output current in amperes. The common-mode voltage (an error producing term) is directly proportional to R_L. So, it is desirable to keep R_L to as minimum a value as is consistent with desired application's requirements.

Determine first the value of I_o and R_L suitable for the desired application. The values of R_S and R_F in ohms can be obtained by the expressions,

$$R_S = \frac{10 - I_o R_L}{I_o}$$

and

$$R_F = \frac{10^5 (I_o R_S 10^4 - R_S)}{10^5 - I_o R_S . 10^4 + R_S}$$

C_C, expressed in pF, can be calculated by the expression

$$C_C = \frac{220 . 10^5}{R_F}$$

where R_F is in ohms.

The above calculated value of C_C would maintain the -3dB frequency response at 2.5kHz. Roll-off at a frequency lower than 2.5kHz can be achieved by increasing the value of C_C.

The maximum allowable voltage across $R_S + R_L$ to maintain the specified accuracy, also known as "compliance" is limited to ±10V by the output swing capability of the output amplifier.

The current output configuration contains all error elements of the voltage output configuration plus additional common-mode errors introduced by raising the demodulated signal reference from output ground to the voltage developed across R_L. Hence, as discussed earlier, consistent with the requirements of desired application, it is best to keep the R_L to as minimum a value as is possible. Figure 7 shows the maximum additional peak nonlinearity errors in the current output configuration expressed as a percent of full scale peak to peak output (40mA) vs R_L/R_S.

The values of R_S and R_F as calculated above, would program the unit for the desired full scale output current I_o when the gain of 3456 is scaled for ±10V full scale ouptut. With these values of R_S and R_F the unit would comply with the performance curves shown in Figures 7, 8 and 9. Deviation from this selection procedure could result in degraded performance.

Due to the output amplifier bias currents and the demodulator currents, we recommend that the full scale output current value be ±1mA or higher (up to ±20mA).

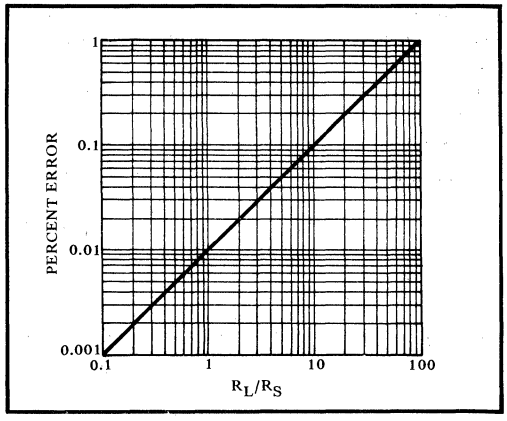


FIGURE 7. Maximum Additional Peak Nonlinearity Errors in Current Output Configuration Expressed as Percent of p-p Output Current Vs R_L/R_S.

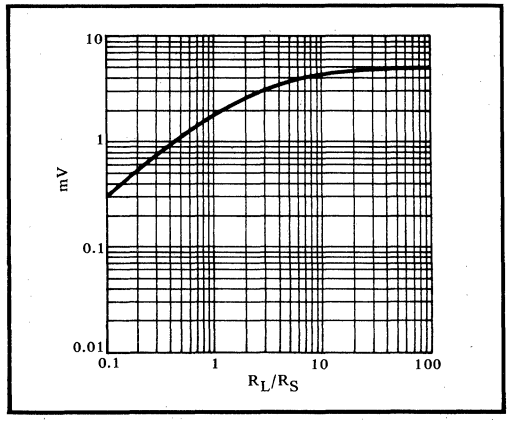


FIGURE 8. Typical Additional Offset in Current Output Configuration Vs R_L/R_S.

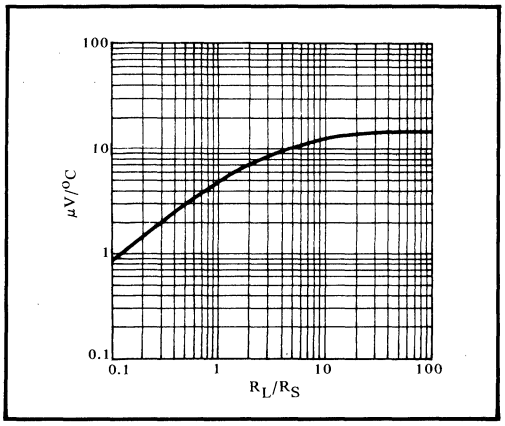


FIGURE 9. Typical Additional Temperature Drift in Current Output Configuration Vs R_L/R_S.

SPECIFICATIONS FOR CURRENT OUTPUT

When the above discussed current output configuration procedure is followed for selection of R_F, R_S, C_C and R_L, the following performance standards would be met by the configuration.

Gain accuracy would be maintained within a maximum of 0.1% above that specified for voltage output configuration. Gain nonlinearity would not exceed the voltage output specification by more than the value indicated in Figure 7.

Current output offset and temperature drift are specified as a voltage quantity appearing across R_S. These parameters each contain two terms. The first term is the total offset voltage RTI (referred to input) specification for voltage output mode multiplied by the input gain setting, multiplied by $\frac{R_S}{R_S + R_L}$. The second term is the value found from Figure 8 for the offset voltage and from Figure 9 for the offset voltage drift. Adding these two terms would give the offset voltage and the offset voltage drift values appearing across the scaling resistor R_S. To obtain these parameters in terms of the offset current and the offset current drift, they have to be divided by R_S. In short,

$$\left(\begin{matrix}\text{Voltage Output Mode}\\ \text{Specification}\end{matrix}\right)\left(\begin{matrix}\text{Input}\\ \text{Gain}\end{matrix}\right)\left(\frac{R_S}{R_S + R_L}\right)+\left(\begin{matrix}\text{Value from}\\ \text{Fig. 8 or Fig. 9}\end{matrix}\right)$$
$$=\left(\begin{matrix}\text{Current Output Mode}\\ \text{Specification}\end{matrix}\right)$$

To obtain the offset or drift in units of current, divide the above equation by R_S.

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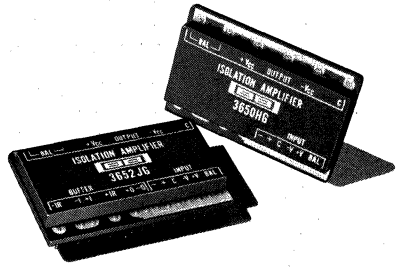


3650
3652

Optically-Coupled Linear ISOLATION AMPLIFIERS

FEATURES

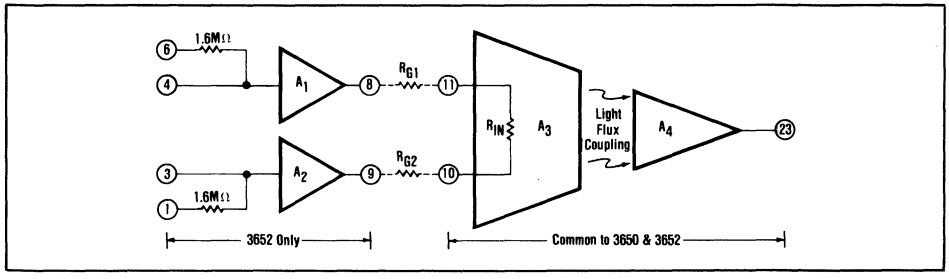
- BALANCED INPUT
- LARGE COMMON-MODE VOLTAGES
  ±2000V Continuous
  140dB Rejection
- ULTRA LOW LEAKAGE
  0.25μA max at 240V/60Hz
  1.8pF Leakage Capacitance
- EXCELLENT GAIN ACCURACY
  0.05% Linearity
  0.05%/1000Hours Stability
- WIDE BANDWIDTH
  15kHz ±3dB
  1.2V/μsec Slew Rate

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- DATA ACQUISITION
- INTERFACE ELEMENT
- BIOMEDICAL MEASUREMENTS
- PATIENT MONITORING
- TEST EQUIPMENT
- CURRENT SHUNT MEASUREMENT
- GROUND-LOOP ELIMINATION
- SCR CONTROLS

DESCRIPTION

The 3650 and 3652 are optically coupled integrated circuit isolation amplifiers. Prior to their introduction commercially available isolation amplifiers had been modular or rack mounted devices using transformer coupled modulation/demodulation techniques. Compared to these earlier isolation amplifiers the 3650 and 3652 have the advantage of smaller size, lower cost, wider bandwidth and integrated circuit reliability. Also, because they use a DC analog modulation technique as opposed to a carrier type technique, they avoid the problems of electromagnetic interference (both transmitted and received) that most of the modular isolation amplifiers exhibit.



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SPECIFICATIONS

ELECTRICAL

Typical at 25°C and ±15VDC supply voltages unless otherwise noted.

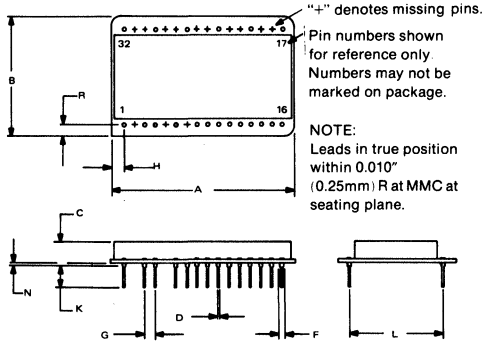
MODEL	3650MG/HG[1]	3650JG	3650KG	3652MG/HG[1]	3652JG
ISOLATION					
Isolation Voltage Rated Continuous, (min) Test Voltage, (min) 10sec duration	2000Vp or VDC 5000Vp				
Isolation-Mode Rejection, G = 10 DC 60Hz, 5000Ω source unbalance Leakage Current, 240V/60Hz Isolation Impedance Capacitance Resistance	140dB 120dB 0.25μA, max 1.8pF $10^{12}\Omega$				
GAIN					
Gain Equation for current sources for voltage sources	$G_I = 10^6$ Volt/Amp $G_V = \frac{10^6}{R_{G1} + R_{G2} + R_{IN}}$ V/V			$G_I = 1.0057 \times 10^6$ Volt/Amp[2] $\frac{10^6}{R_{G1} + R_{G2} + R_{IN} + R_O}$ V/V	
Input Resistance, R_{IN}, max Buffer Output Impedance, R_O Gain Equation Error, max[3] Gain Nonlinearity Gain vs Temperature Gain vs Time	25Ω Not applicable 1.5% ±0.05% typ. ±0.2% max 300ppm/°C	0.5% ±0.03% typ. ±0.1% max 100ppm/°C ±0.05%/1000hrs.	0.5% ±0.02% typ. ±0.05% max 50ppm/°C	25Ω 90Ω ±30Ω 1.5%[4] ±0.05% typ. ±0.2% max 300ppm/°C[4]	0.5%[4] ±0.05% typ. ±0.1% max 200ppm/°C[4] ±0.05%/1000hrs.
Frequency Response Slew Rate ±3dB Frequency Settling Time to ±0.01% to ±0.1%	0.7V/μsec min, 1.2V/μsec typ. 15kHz 400μsec 200μsec				
INPUT STAGE[5]					
Input Offset Voltage at 25°C, max[3] vs Temperature, max vs Supply vs Time	±5mV ±25μV/°C	±1mV ±10μV/°C 100μV/V 50μV/1000 hrs.	±0.5mV ±5μV/°C	±5mV ±50μV/°C 100μV/V 100μV/1000 hrs.	±2mV ±25μV/°C
Input Bias Current at 25°C vs Temperature vs Supply	10nA typ, 40nA max 0.3nA/°C 0.2nA/V			10pA typ, 50pA max doubles every +10°C 1pA/V	
Input Offset Current vs Temperature vs Supply	effects included in output offset			10pA doubles every 10°C 1pA/V	
Input Impedance Differential Common-mode	"R_{IN}" = 25Ω max $10^9\Omega$			$10^{11}\Omega$ $10^{11}\Omega$	
Input Noise Voltage, 0.05Hz to 100Hz 10Hz to 10kHz	8μV, p-p 4μV, rms			4μ, p-p 5μV, rms	
Input Voltage Range Common-mode, linear operation, w/o damage, at +,- at +I, -I at +IR, -IR	±(|V| -5)V ±V Not applicable Not applicable			±(|V| -5) ±V ±300V for 10msec[6] ±3000V for 10msec[6]	
Differential, w/o damage, at +, - Differential, w/o damage, at +I, -I Differential, w/o damage, at +IR, -IR	±V Not applicable Not applicable			±V ±600V for 10msec[6] ±6000V for 10msec[6]	
Common-mode Rejection, 60Hz	90dB at 60Hz, 5kΩ imbalance			80dB at 60Hz, 5kΩ imbalance	
Power Supply (Input Stage Only) Voltage (at "+V" and "-V" Current Quiescent with ±10V output[7]	±8V to±18V ±1.2mA[7] +6.5mA or -6.5mA, typ +12mA or -12mA, max			±8V to ±18V ±3mA[7] +8.5mA or -8.5mA, typ +16mA or -16mA, max	

ELECTRICAL (cont)

MODEL	3650MG/HG(1)	3650JG	3650KG	3652MG/HG(1)	3652JG
OUTPUT STAGE					
Output Voltage, min		±10V		±10V	
Output Current, min		±5mA		±5mA	
Output Offset Voltage					
at 25°C max(3)	±25mV	±10mV	±10mV	±25mV	±10mV
vs Temperature, max	±900μV/°C	±450μV/°C	±300μV/°C	±900μV/°C	±450μV/°C
vs Supply		±500μV/V		±500μV/V	
vs Time		±1mV/1000hrs		±1mV/1000hrs	
Output Noise Voltage					
0.05Hz to 100Hz		50μV, p-p		50μV, p-p	
10Hz to 1kHz		65μV, rms		65μV, rms	
Power Supply (Output Stage Only)					
Voltage ("+V_{CC}" and "-V_{CC}")		±8V to ±18V			
Current					
Quiescent		±2.3mA typ, ±6mA max			
with ±5mA output, max		±11mA			
TEMPERATURE(8)					
Specification		0°C to 85°C			
Operating		-40°C to +100°C			
Storage		-55°C to +125°C			

1. All electrical and mechanical specifications of the 3650MG and 3652MG are identical to the 3650HG and 3652HG, respectively, except that the following specifications apply to the 3650MG and 3652MG: (a) Isolation test voltage duration increased from 10sec minimum to 60sec minimum; (b) Input Offset voltage at 25°C max: ±10mV; vs. temp. max: ±100μV/°C; (c) Output offset voltage at 25°C max: ±50mV; vs temp. max: ±1.8mV/°C.
2. If used as 3650, see Installation and Operating Instructions.
3. Trimmable to zero.
4. Gain error terms specified for inputs applied through buffer amplifiers (i.e., ±I or ±IR pins).
5. Input stage specifications at +I and -I inputs for 3652 unless otherwise noted.
6. Continuous rating is 1/3 pulse rating.
7. Load current is drawn from one supply lead at a time other supply current at quiescent level, for 3652 add 0.2mA/V of pos CMV.
8. dT/dt > 1°C/minute below 0°C, and long-term storage above 100°C is not recommended. Also limit the repeated thermal cycles to be within the 0°C to 85°C temperature range.

MECHANICAL



"+" denotes missing pins.

Pin numbers shown for reference only. Numbers may not be marked on package.

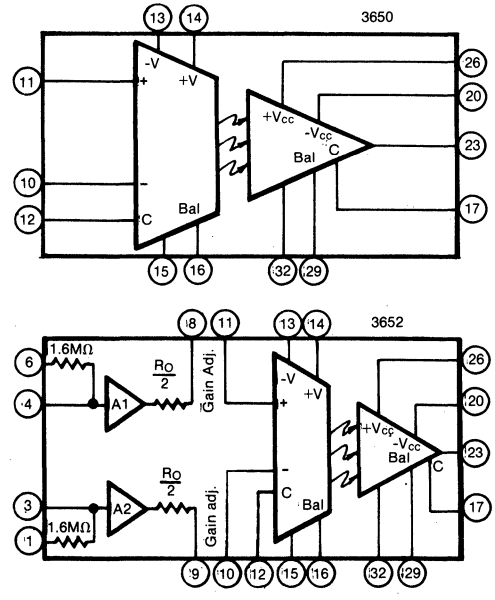
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

ORDER NUMBER:
3650MG 3652MG
3650HG 3652HG
3650JG 3652JG
3650KG

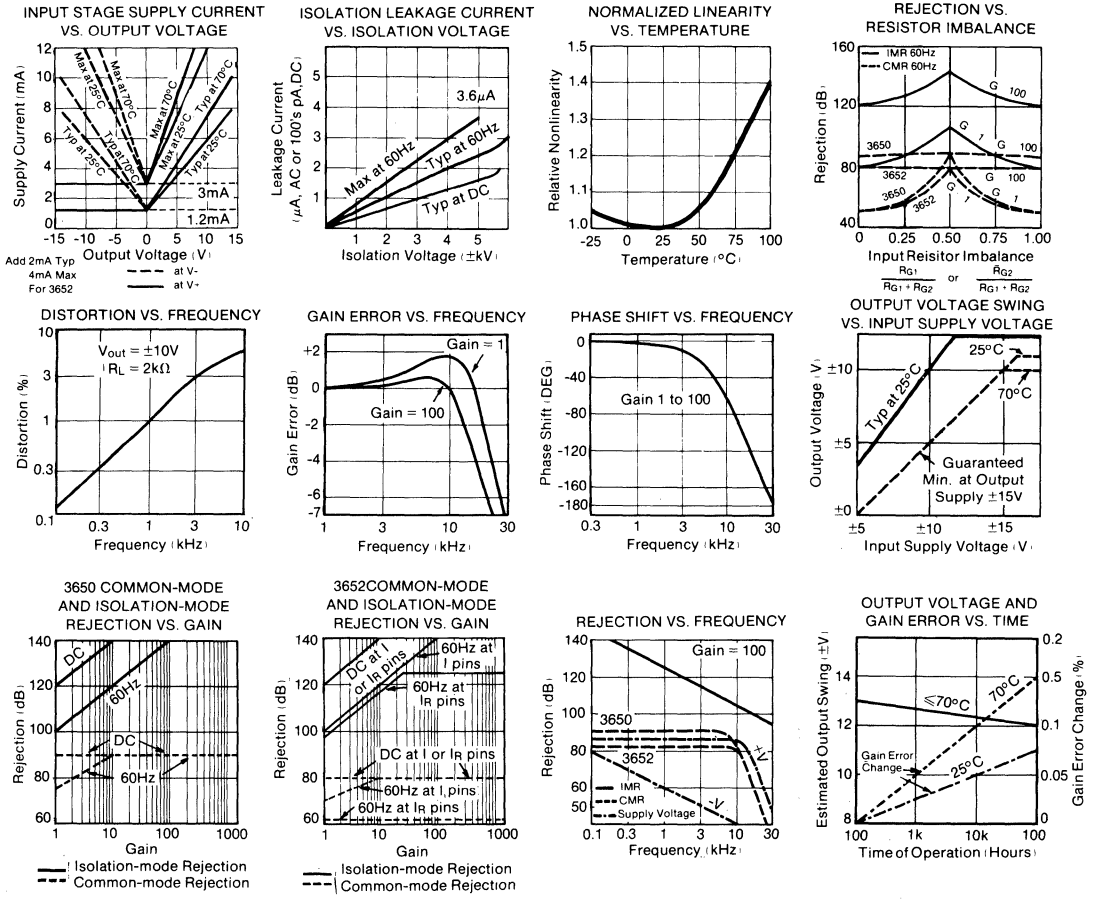
MATERIAL: Alumina (ceramic)
WEIGHT: 14 grams (0.5 oz)
MATING CONNECTOR: 2302MC (set of two, 16-pin strips)

PIN CONNECTIONS



TYPICAL PERFORMANCE CURVES

Typical at 25°C and ±15VDC power supplies unless otherwise noted.



DEFINITIONS

ISOLATION-MODE VOLTAGE, V_{ISO}

The isolation-mode voltage is the voltage which appears across the isolation barrier, i.e., between the input common and the output common. (See Figure 1.)

Two isolation voltages are given in the electrical specifications; "rated continuous" and "test voltage". Since it is impractical on a production basis to test a "continuous" voltage (infinite test time is implied), it is generally accepted practice to test at a significantly higher voltage for some reasonable length of time. For the 3650 and the 3652 the "test voltage" is equal to 1000V plus two times the "rated continuous" voltage. Thus, for a continuous rating of 2000V each unit is tested at 5000V. Specifically, each unit is tested with a 60Hz 5000V peak sine wave with

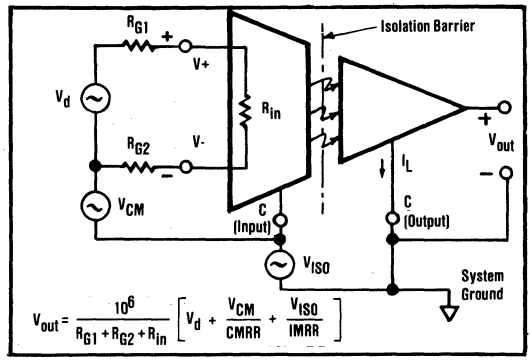


FIGURE 1. Illustration of Isolation-mode and Common-mode Specifications.

an acceptance criteria of 3.7μA maximum leakage current I_L (equivalent to 0.25μA at 240V/60Hz).

COMMON-MODE VOLTAGE, V_{CM}

The common-mode voltage is the voltage midway between the two inputs of the amplifier measured with respect to input common. It is the algebraic average of the voltage applied at the amplifiers' input terminals. In the circuit in Figure 5, $(V_+ + V_-)/2 = V_{CM}$. (Note: Many applications involve a large system "common-mode voltage." Usually in such cases the term defined here as "V_{CM}" is negligible and the system "common-mode voltage" is applied to the amplifier as "V_{ISO}" in Figure 1.)

ISOLATION-MODE REJECTION

The isolation-mode rejection is defined by the equation in Figure 1. The isolation-mode rejection is not infinite because there is some leakage across the isolation barrier due to the isolation resistance and capacitance.

NONLINEARITY

Nonlinearity is specified to be the peak deviation from a best straightline, expressed as a percent of peak-to-peak full scale output (i.e., ±10mV at 20V p-p ≈ 0.05%).

THEORY OF OPERATION

Prior to the introduction of the 3650 family optical isolation had not been practical in linear circuits. A single LED and photodiode combination, while useful in a wide range of digital isolation applications, has fundamental limitations - primarily nonlinearity and instability as a function of time and temperature.

The 3650 and 3652 use a unique technique to overcome the limitations of the single LED and photodiode isolator. Figure 2 is an elementary equivalent circuit for the 3650 which can be used to understand the basic operation without consideration the cluttering details of offset adjustment and biasing for bipolar operation.

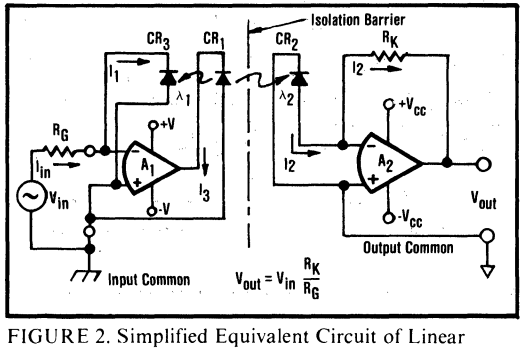


FIGURE 2. Simplified Equivalent Circuit of Linear Isolator.

Two matched photodiodes are used--one in the input (CR_3) and one in the output stage (CR_2) - - to greatly reduce nonlinearities and time - temperature instabilities. Amplifier A_1, LED CR_1, and photodiode CR_3 are used in a negative feedback configuration such that $I_1 = I_{in} / R_G$ (where R_G is the user supplied gain setting resistor). Since CR_2 and CR_3 are closely matched and since they receive equal amounts of light from the LED CR_1 (i.e., $\lambda_1 = \lambda_2$), $I_2 = I_1 = I_{in}$. Amplifier A_2 is connected as a current-to-voltage converter with $V_{out} = I_2 R_K$ where R_K is an internal 1MΩ scaling resistor. Thus the overall transfer function is:

$$V_{out} = V_{in} \frac{10^6}{R_G}, \ (R_G \text{ in ohms})$$

This improved isolator circuit overcomes the primary limitations of the single LED and photodiode combination. The transfer function is now virtually independent of any degradation in the LED output as long as the two photodiodes and optics are closely matched*. Linearity is now a function of the accuracy of the matching and is further enhanced by the use of negative feedback in the input stage. Advanced laser trimming techniques are used to further compensate for residual matching errors.

*The only effect of decreased LED output is a slight decrease in full scale swing capability. See Typical Performance Curves.

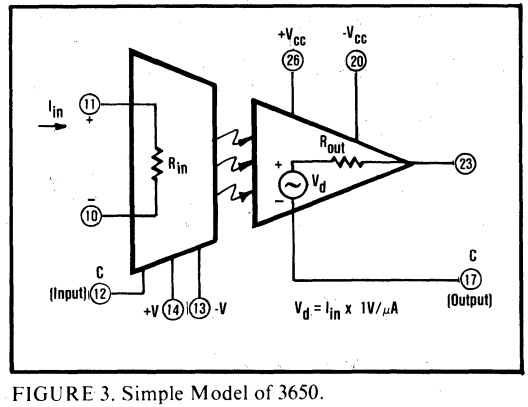


FIGURE 3. Simple Model of 3650.

A model of the 3650 suitable for simple circuit analysis is shown in Figure 3. The output is a current dependent voltage source, V_d, whose value depends on the input current. Thus, the 3650 is a transconductance amplifier with a gain of one volt per microamp. When voltage sources are used the input current is derived by using gain setting resistors in series with the voltage source (see Installation and Operating Instructions for details). R_{in} is the differential input impedance. The common-mode and isolation impedances are very high and are assumed to be infinite for this model.

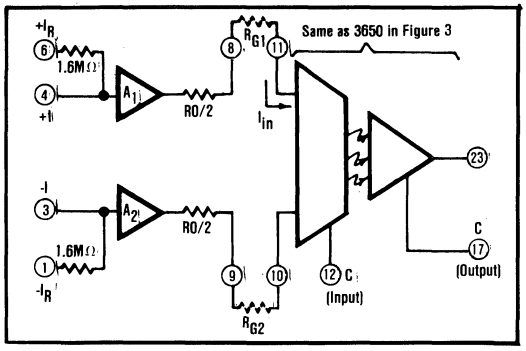


FIGURE 4. Simple Model of 3652.

A simplified model of the 3652 is shown in Figure 4. The isolation and output stages are identical to the 3650. Additional input circuitry consisting of FET buffer amplifiers and input protection resistors have been added to give higher differential and common-mode input impedance ($10^{11}\Omega$), lower bias currents (50pA) and overvoltage protection. The +IR and -IR inputs have a 10msec pulse rating of 6000V differential and 3000V common-mode (see Definitions for a discussion of common-mode and isolation-mode voltages.) The addition of the buffer amplifiers also creates a voltage-in voltage-out transfer function with the gain set by R_{G1} and R_{G2}.

INSTALLATION & OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

The power supply connections for the 3650 and 3652 are shown in Figure 5. When a DC/DC converter is used for isolated power it is placed in a parallel with the isolation barrier of the amplifier. This can lower the isolation impedance and degrade the isolation-mode rejection of the overall circuit. Therefore, a high quality, low leakage DC/DC converter such as the Burr-Brown Model 722 should be used.

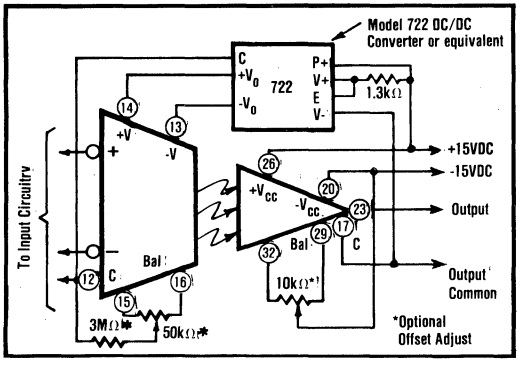


FIGURE 5. Power and Offset Adjust Connections.

OFFSET VOLTAGE ADJUSTMENTS

The offset nulling circuits are identical for the 3650 and 3652 and are shown in Figure 5. The offset adjust circuitry is optional and the units will meet the stated specifications with the BAL terminals unconnected. Provisions are available to null both the input and output stage offsets. If the amplifier is operated at a fixed gain, normally only one adjustment will be used; the output stage (10kΩ adjustment) for low gains and the input stage (50kΩ adjustment) for high gains.(>10).

Use the following procedure if it is desired to null both input and output components (for example, if the gain of the amplifier is to be switched). The input stage offset is first nulled (50kΩ adjustment) with the appropriate input signal pins connected to input common and the amplifier set at its maximum gain. The gain is then set to its minimum value and the output offset is nulled (10kΩ adjustment).

INPUT CONFIGURATIONS

Some possible input configurations for the 3650 and 3652 are shown in Figures 6a, 6b, 6c. Differential input sources are used in these examples. For situations with non-differential inputs the appropriate source term should be set to zero in the gain equations and replaced with a short in the diagrams.

Figure 6a shows the 3650 connected as a transconductance amplifier with input current sources. Voltage sources are shown in Figure 6b. In this case the voltages are converted to currents by R_{G1} and R_{G2}. As shown by the equations, they perform as gain setting resistors in the voltage transfer function. When a single voltage source is used it is recommended (but not essential) that the gain setting resistor remain split into two equal halves in order to minimize errors due to bias currents and common-mode rejection (see Typical Performance Curves).

Figure 6c illustrates the connections for the 3652 when the FET buffer amplifiers A_1 and A_2 are used. This configuration provides an isolation amplifier with high input impedance (both common-mode and differential) and good common-mode and isolation-mode rejection. It is a true isolated instrumentation amplifier which has many benefits for noise rejection when source impedance imbalances are present.

In the 3652 the voltage gain of the buffer amplifiers is slightly less than unity, but the gain of the output stage has been raised to compensate for this so that the overall transfer function from the ±I or ±IR inputs to the output is correct. It should be noted that A_1 and A_2 are buffer amplifiers. No summing can be done at the ±I or ±IR inputs. Figure 6c shows the +I and -I inputs used. If more input voltage protection is desired, then the +IR and −IR inputs should be used. This will increase the input noise due to the contribution from the 1.6MΩ resistors, but will provide additional differential and common-mode protection (10msec rating of 3kV).

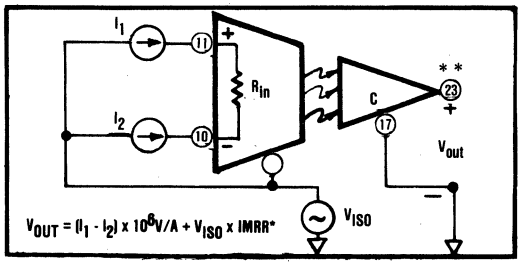


FIGURE 6a. 3650 With Differential Current Sources.

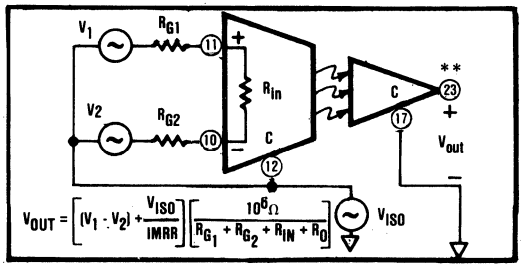


FIGURE 6b. 3650 With Differential Voltage Source.

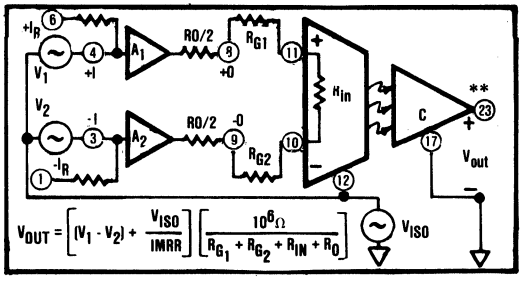


FIGURE 6c. 3652 with Differential Voltage Source.

*IMRR here is in pA/V, typically 5pA/V at 60Hz and 1pA/V at DC.
**The offset adjustment circuitry and power supply connections have been omitted for simplicity. Refer to Figure 5 for details.

ERROR ANALYSIS

A model of the 3650 suitable for DC error analysis of offset voltage, voltage drift versus temperature, bias current, etc., is shown in Figure 7.

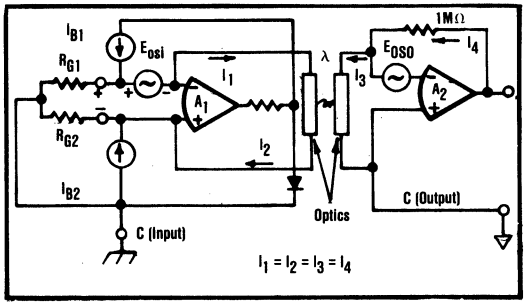


FIGURE 7. DC Error Analysis Model for 3650.

A_1 and A_2, the input and output stage amplifiers, are considered to be ideal. Separate external generators are used to model the offset voltages and bias currents. R_{in} is assumed to be small relative to R_{G1} and R_{G2} and is therefore omitted from the gain equation. The feedback configuration, optics and component matching are such that $I_1 = I_2 = I_3 = I_4$. A simple circuit analysis gives the following expression for the total output error voltage due to offset voltages and bias currents.

$$V_{out\text{-}total} = \frac{10^6}{R_{G1} + R_{G2}} \left[E_{osi} + (I_{B1} R_{G1} - I_{B2} R_{G2})\right] + E_{oso} \quad (1)$$

Offset current is defined as the difference between the two bias currents I_{B1} and I_{B2}. If $I_{B1} = I_B$ and $I_{B2} = I_B + I_{os}$, then, for $R_{G1} = R_{G2}$, $V_{out} - I_B = \frac{10^6 \cdot I_{os}}{2}$.

This component of error is not a function of gain and is therefore included as a part of E_{oso} specifications. The output errors due to the output stage bias current are also included in E_{oso}. This results in a very simple equation for the total error:

$$V_{out\text{-}total} = \frac{10^6 E_{osi}}{2R_{G1}} + E_{oso} \text{ (for } R_{G1} = R_{G2}). \quad (2)$$

In summary it should be noted that equation (2) should be used only when $R_{G1} = R_{G2}$. When $R_{G1} \neq R_{G2}$, equation (1) applies.

The effects of temperature may be analyzed by replacing the offset terms with their corresponding temperature gradient terms:

$V_{out} \rightarrow \Delta V_{out}/\Delta T$, $E_{osi} \rightarrow \Delta E_{osi}/\Delta T$, etc.

For a complete analysis of the effects of temperature, gain variations must also be considered.

OUTPUT NOISE

The total output noise is given by

$$E_n\,(RMS) = \sqrt{(E_{nI}\,G)^2 + (E_{nO})^2}$$

where E_n (RMS) = total output noise
E_{nI} = RMS noise of the input stage
E_{nO} = RMS noise of the output stage
$G = 10^6 / (R_{G1} + R_{G2})$

E_{nO} includes the noise contribution due to the optics and the noise currents of the output stage. Errors created by the noise current of the input stage are insignificant compared to other noise sources and are therefore omitted.

COMMON-MODE and ISOLATION-MODE REJECTION

The expression for the output error due to common-mode and isolation mode voltage is:

$$V_{out} = G \cdot \frac{V_{cm}}{CMRR} + \frac{V_{iso}}{IMRR}.$$

GUARDING & PROTECTION

To preserve the excellent inherent isolation characteristics of these amplifiers, the following recommended practice should be noted:

1. Use shielded, twisted pair of cable at the input as with any instrumentation amplifier;
2. Care sould be taken to minimize external capacitance. A symmetrical layout of external components to achieve balanced capacitance from the input terminals to output common will preserve high IMR;
3. External components and conductor patterns should be at a distance equal to or greater than the distance between the input and output terminals, to prevent HV breakdown.
4. Though not an absolute requirement, the use of laminated or conformally coated printed circuit boards is recommended.

APPLICATIONS

Figure 8 shows a system where isolation amplifiers (3650) are used to measure the armature current and the armature voltage of a motor.

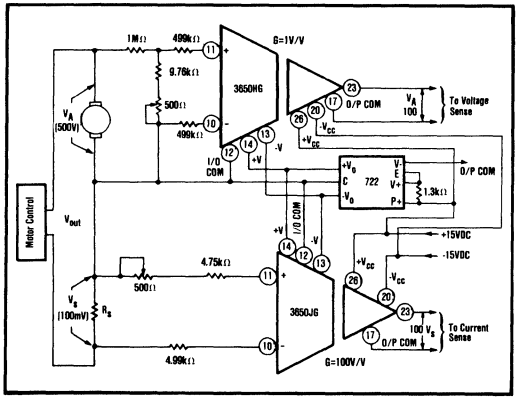


FIGURE 8. Isolated Armature Current and Voltage Sensor.

The armature current of the motor is converted to a voltage by the calibrated shunt R, and then amplifier (adjustable gain) and isolated by the 3650.

The armature voltage is sensed by the voltage divider (adjustable) shown and then amplified and isolated by the 3650.

The 3650 provides the advantage of accurate current measurement in the presence of high common-mode voltage. Both 3650's provide the advantage of isolating the motor ground from the control system ground. Isolated power is provided by an isolated DC/DC converter (BB Model 722 or equivalent).

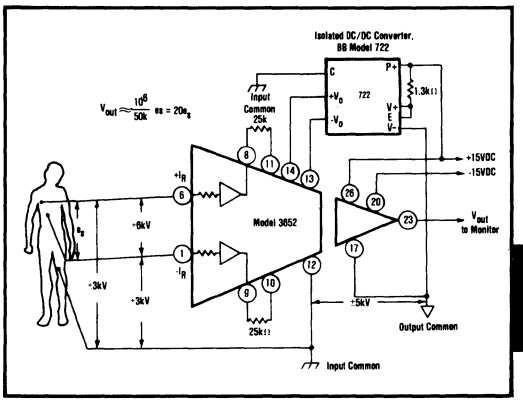


FIGURE 9. 3652 Used in Patient Monitoring Application (ECG, VCG, EMG Amplifier).

The 3652 is ideally suited for patient monitoring applications as shown in Figure 9. The fact that it is a true balanced input instrumentation amplifier with very high differential and common-mode inpedance means that it can greatly reduce the common-mode noise pick up due to imbalance in lead impedances that often appear in patient monitoring situations. The 3kV and 6kV shown in Figure 9 are the 10msec pulse ratings of the +IR and -IR inputs for the common-mode and differential input voltages with respect to input common. The rating of the isolation barrier is 2000V, pk continuous. The non-recurrent pulse rating of the isolation barrier is 5000V, pk since each unit is factory tested at 5000V, pk. If the isolation barrier is to be subjected to higher voltages a gas filled surge voltage protection device can be used. For multichannel operation, two 3562's can be powered by one Model 722 isolated DC/DC converter. The total leakage current for both channels at 240V/60Hz would still be less than 2μA.

The block diagram in Figure 10 shows the use of isolation amplifiers in SCR control application.

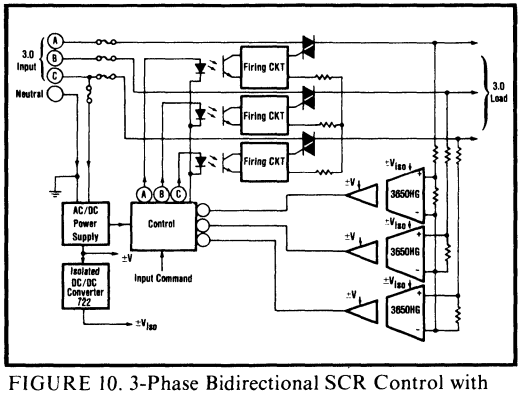
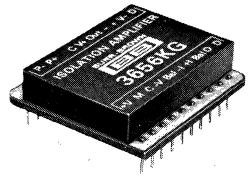


FIGURE 10. 3-Phase Bidirectional SCR Control with Voltage Feedback.

BURR-BROWN®

3656



Integrated Circuit - Transformer Coupled ISOLATION AMPLIFIER

FEATURES

- INTERNAL ISOLATED POWER
- 8000V ISOLATION TEST VOLTAGE
- 0.5μA MAX LEAKAGE AT 120V, 60Hz
- 3-PORT ISOLATION
- 125dB REJECTION AT 60Hz
- 1" x 1" x 0.25" CERAMIC PACKAGE

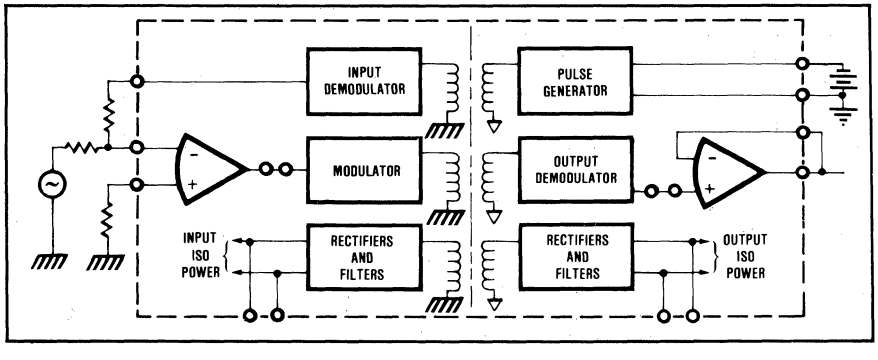
APPLICATIONS

- MEDICAL
  Patient monitoring and diagnostic instrumentation
- INDUSTRIAL
  Ground loop elimination and off-ground signal measurement
- NUCLEAR
  Input/output/power isolation

DESCRIPTION

The 3656 is the first amplifier to provide a total isolation function ... both signal and power isolation ... in integrated circuit form. This remarkable advancement in analog signal processing capability is accomplished by use of a patented modulation technique and minature hybrid transformer.

Versatility and performance are outstanding features of the 3656. It is capable of operating with three completely independent grounds (three-port isolation). In addition, the isolated power generated is available to power external circuitry at either the input or output. The uncommitted op amps at the input and the output allow a wide variety of closed-loop configurations to match the requirements of many different types of isolation applications.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

THEORY OF OPERATION

Details of the 3656 design are shown in Figure 1. The external connections shown, place it in its simplest gain configuration - unity gain, noninverting. Several other amplifier gain configurations and power isolation configurations are possible. See Installation and Operating Instructions and Applications sections for details.

Isolation of both signal and power is accomplished with a single miniature toroid transformer with multiple windings. A pulse generator operating at approximately 750kHz provides a two-part voltage waveform to transformer T1. One part of the waveform is rectified by diodes D_1 through D_4 to provide the isolated power to the input and output stages (+V, -V and V+, V-). The other part of the waveform is modulated with input signal information by the modulator operating into the W_2 winding of the transformer.

The modulated signal is coupled by windings W_6 and W_7 to two matched demodulators - one in the input stage and one in the output stage - which generate identical voltages at their outputs, pins 10 and 11 (voltages identical with respect to their respective commons, pins 3 and 17). In the input stage the input amplifier A1, the modulator and the input demodulator are connected in a negative feedback loop. This forces the voltage at pin 6 (connected as shown in Figure 1) to equal the input signal voltage applied at pin 7. Since the input and the output demodulators are matched and produce identical output voltages, the voltage at pin 11 (referenced to pin 17, the output common) is equal to the voltage at pin 10 (referenced to pin 3, the input common). In the output stage, output amplifier A_2 is connected as a unity gain buffer, thus the output voltage at pin 15 equals the output demodulator voltage at pin 11. The end result is an isolated output voltage at pin 15 equal to the input voltage at pin 7 with no galvanic connection between them.

Several amplifier and power connection variations are possible:

1. The input stage may be connected in various operational amplifier gain configurations.
2. The output stage may be operated at gains above unity.
3. The internally generated isolated voltages which provide power to A_1 and A_2 may be overridden and external supply voltages used instead.

Versatility and its three independent isolated grounds allow simple solutions to demanding analog signal conditioning problems. See the Installation and Operating Instructions and Applications sections for details.

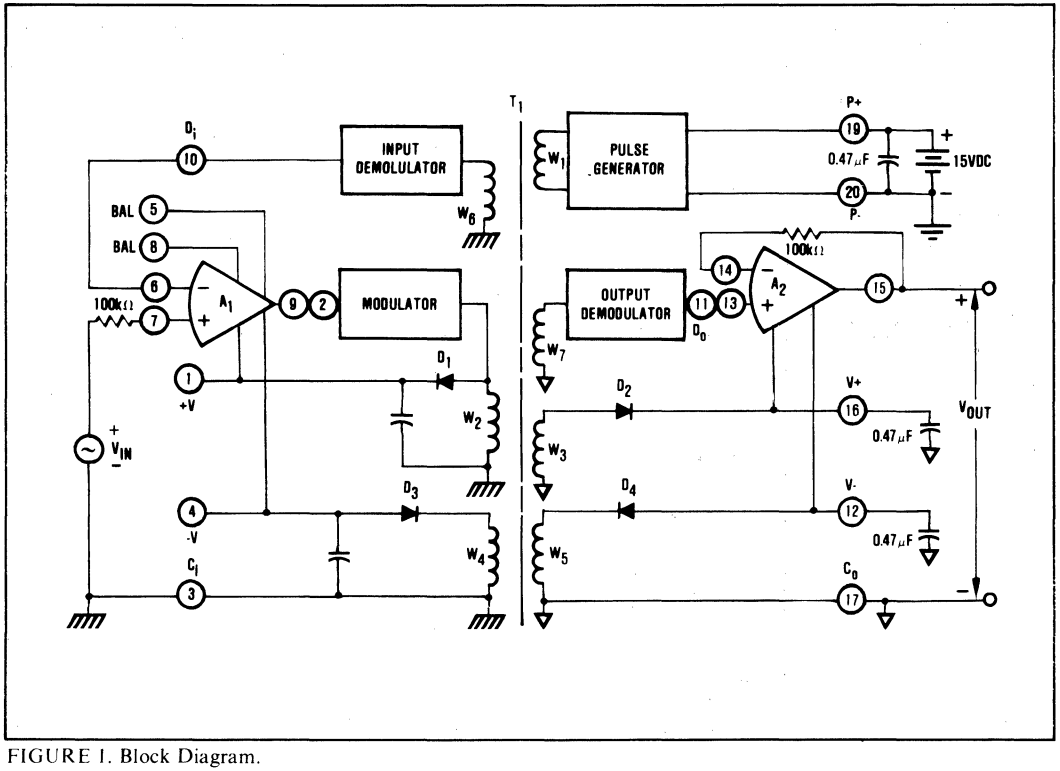


FIGURE 1. Block Diagram.

SPECIFICATIONS
ELECTRICAL

At 25°C, V± = ±15V and 15V between P+ and P-, unless otherwise noted.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
ISOLATION					
Voltage					
Rated Continuous(1), DC		3500 (1000)			VDC
Rate Continuous(2), AC		2000 (700)			V, rms
Test, 10sec(1)		8000 (3000)			VDC
Rejection	G_1 = 10V/V				
DC			160		dB
60Hz, < 100Ω in I/P Com(2)			125		dB
60Hz, 5kΩ in I/P Com(2)					
3656HG		108			dB
3656AG, BG, JG, KG		112			dB
Capacitance(1)			6.0 (6.3)		pF
Resistance(1)			10^{12} (10^{12})		Ω
Leakage Current	120V, 60Hz		0.28	0.5	μA
GAIN					
Equations	See Text				
Accuracy of Equations					
Initial(3) 3656HG	G < 100V/V			1.5	%
3656AG, JG, KG				1.0	%
3656BG				0.3	%
vs. Temperature 3656HG				480	ppm/°C
3656AG, JG				120	ppm/°C
3656BG, KG				60	ppm/°C
vs. Time			0.02 (1 + log khrs.)		%
Nonlinearity	$R_A + R_F = R_B \geq 2M\Omega$				
External Supplies used at					
pins 12 and 16, 3656HG	Unipolar or Bipolar Output			±0.15	%
3656AG, JG, KG				±0.1	%
3656BG				±0.05	%
Internal Supplies used for	Bipolar Output Voltage				
Output Stage	Swing, Full Load(4)		±0.15		%
OFFSET VOLTAGE(5)	RTI				
Initial(3), 3656HG	15V_P between P+ and P-			±(4 + 40/G_1)]	mV
3656AG, JG				±(2 + (20/G_1)]	mV
3656BG, KG				±(1 + (10/G_1)]	mV
vs. Temperature, 3656HG				±(200 + (1000/G_1)]	μV/°C
3656JG				±(50 + (750/G_1)]	μV/°C
3656AG				±(25 + (500/G_1)]	μV/°C
3656KG				±(10 + (350/G_1)]	μV/°C
3656BG				±(5 + (350/G_1)]	μV/°C
vs. Supply Voltage	Supply between P+ and P-				
3656HG				±(0.6 + (3.5/G_1)]	mV/V
3656AG, BG, JG, KG				±(0.3 + (2.1/G_1)]	mV/V
vs. Current(6)			±(0.1 + (10/G_1)]	±(0.2 + (20/G_1)]	mV/mA
vs. Time			±(10 + (100/G_1)] x (1 + log khrs.)		μV
AMPLIFIER PARAMETERS	Apply to A1 and A2				
Bias Current(7)					
Initial				100	nA
vs. Temperature			0.5		nA/°C
vs. Supply			0.2		nA/V
Offset Current(7)			5	20	nA
Impedance	Common-mode		100 || 5		MΩ || pF
Input Noise Voltage	f_B = 0.05Hz to 100Hz		5		μV, p-p
	f_B = 10Hz to 10kHz		5		μV, rms
Input Voltage Range(8)					
Linear Operation	Internal Supply			±5	V
	External Supply			Supply -5V	V
Without Damage	Internal Supply			±8	V
	External Supply			Supply	V
Output Current	V_{OUT} = ±5V				
	±15V External Supply	±5			mA
	Internal Supply	±2.5			mA
	V_{OUT} = ±10V				
	±15V External Supply	±2.5			mA
	V_{OUT} = ±2V, $V_{P+, P-}$ = 8.5V				
	Internal Supply		±1		mA
Quiescent Current			150	450	μA

ELECTRICAL (CONT)

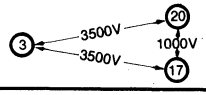
At 25°C, V+ = ±15V and 15V between P+ and P-, unless otherwise noted.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG			UNITS
		MIN	TYP	MAX	
FREQUENCY RESPONSE					
±3dB Response	Small Signal		30		kHz
Full Power			1.3		kHz
Slew Rate	Direction measured at output	+0.1, -0.04			V/μsec
Settling Time	to 0.05%		500		μsec
OUTPUT					
Noise Voltage (RTI)	f_B = 0.05Hz to 100Hz		$\sqrt{.5^2 + (22/G_1)^2}$		μV, p-p
	f_B = 10Hz to 10kHz		$\sqrt{.5^2 + (11/G_1)^2}$		μV, rms
Residual Ripple(9)				5	mV, p-p
POWER SUPPLY IN,	at P+, P- pins 19 and 20				
Rated Performance			15		VDC
Voltage Range(10)	Derated Performance	8.5		16	VDC
Ripple Current(9)			10	25	mA, p-p
Quiescent Current(11)	Average		14	18	mA, DC
Current vs. Load Current(12)	vs. Currents from +V, -V, V+, V-		0.7		mA/mA
ISOLATED POWER OUT	at +V, -V, V+, V- pins				
Voltage, no load	15V between P+ and P-	8.5	9.0	9.5	V
Voltage, full load	±5mA (10mA sum) load (12)	7.0	8.0	9.0	V
Voltage vs. Power Supply	vs. Supply between P+ and P-		0.66		V/V
Ripple Voltage(9)					
No load			40		mV, p-p
Full load	±5mA load		80	200	mV, p-p
TEMPERATURE RANGE					
Specification 3656AG, BG		-25		+85	°C
3656HG, JG, KG		0		+70	°C
Operation(10)		-55		+100	°C
Storage(13)		-65		+125	°C

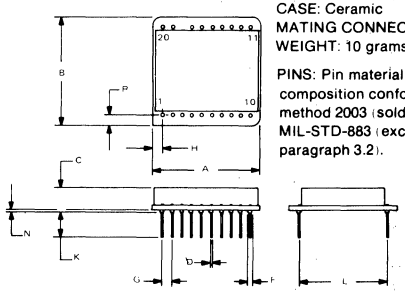
NOTES:

1. Ratings in parenthesis and between P- (pin 20) and O/P Com (pin 17). Other isolation ratings are between I/P Com and O/P Com or I/P Com and P-.

An example of the ratings for 3-port continuous isolation.



MECHANICAL



CASE: Ceramic
MATING CONNECTOR: None
WEIGHT: 10 grams (0.35 oz.)

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.285	5.97	7.24
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	

NOTE:
An accessory part which provides both magnetic and electrostatic shielding is available.
Order Number: 100MS
Size: 1.2" x 1.2" x 0.6"
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

2. May be improved with proper shielding. See Performance Curves.
3. May be trimmed to zero.
4. If output swing is unipolar, or if the output is not loaded, specification same as if external supply were used.
5. Includes effects of A_1 and A_2 offset voltages and bias currents if recommended resistors used.
6. Versus the sum of all external currents drawn from V+, V-, +V, -V (=I_{ISO}).
7. Effects of A_1 and A_2 bias currents and offset currents are included in Offset Voltage specifications.
8. With respect to I/P Com (pin 3) for A_1 and with respect to O/P Com (pin 17) for A_2. CMR for A_1 and A_2 is 100dB, typical.
9. In configuration of Figure 3. Ripple frequency approximately 750kHz. Measurement bandwidth is 10MHz.
10. Decrease linearly from 16VDC at 85°C to 12VDC at 100°C.
11. Instantaneous peak current required from pins 19 and 20 at turn-on is 100mA for slow rising voltages (50msec) and 300mA for fast rises (50μsec).
12. Load current is sum drawn from +V, -V, V+, V- (=I_{ISO}).
13. Isolation ratings may degrade if exposed to 125°C for more than 1000 hours or 90°C for more than 50,000 hours.

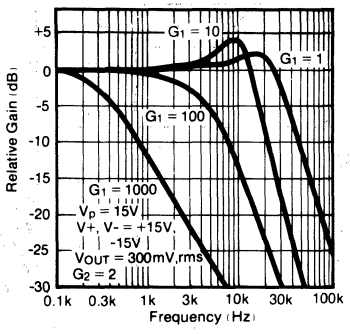
PIN DESIGNATIONS

1	+V	11	OUTPUT DEMOD
2	MOD INPUT	12	V-
3	INPUT DEMOD COM	13	A_2 NONINVERTING INPUT
4	-V	14	A_2 INVERTING INPUT
5	BALANCE	15	A_2 OUTPUT
6	A_1 INVERTING INPUT	16	V+
7	A_1 NONINVERTING INPUT	17	OUTPUT DEMOD COM
8	BALANCE	18	NO PIN
9	A_1 OUTPUT	19	P+
10	INPUT DEMOD	20	P-

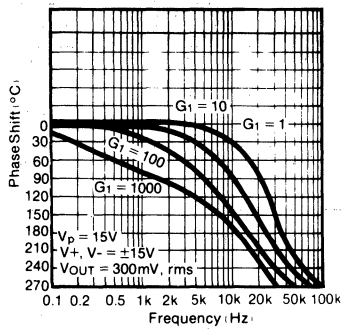
TYPICAL PERFORMANCE CURVES

All specifications typical at 25° C unless otherwise noted.

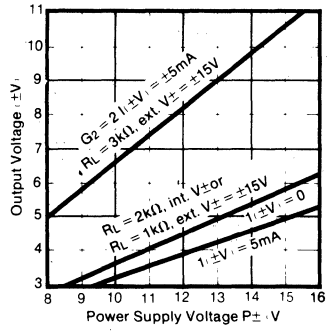
SMALL SIGNAL FREQUENCY RESPONSE



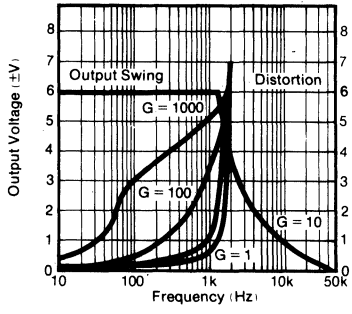
PHASE RESPONSE



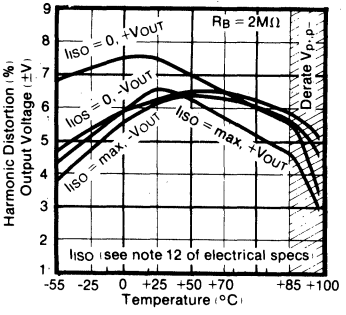
OUTPUT SWING VS SUPPLY VOLTAGE



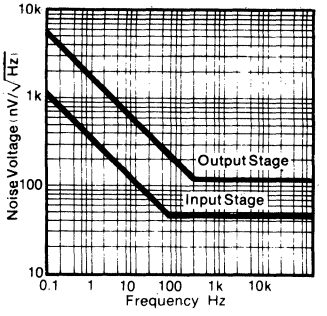
OUTPUT SWING AND DISTORTION VS FREQUENCY



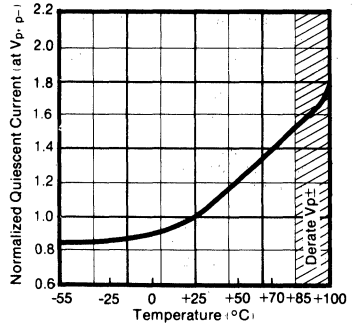
OUTPUT VOLTAGE SWING VS TEMPERATURE AND ISOLATED SUPPLY LOAD



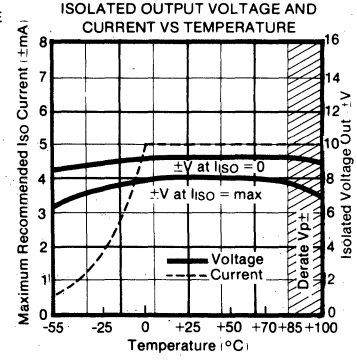
NOISE VOLTAGE VS FREQUENCY



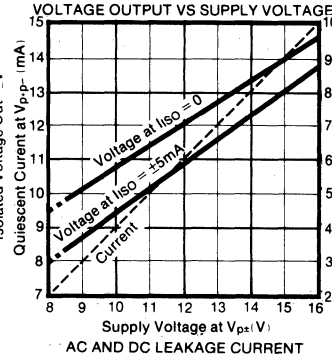
QUIESCENT CURRENT VS TEMPERATURE



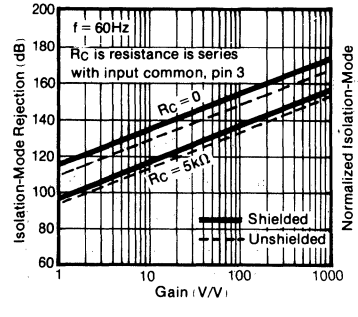
ISOLATED OUTPUT VOLTAGE AND CURRENT VS TEMPERATURE



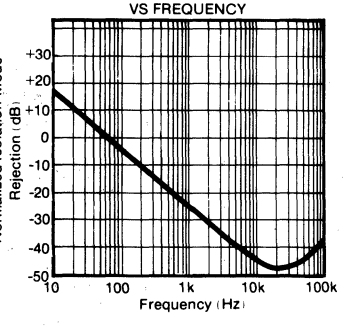
QUIESCENT CURRENT AND ISOLATED VOLTAGE OUTPUT VS SUPPLY VOLTAGE



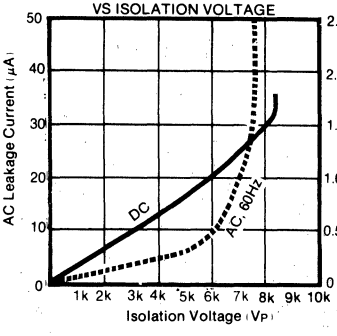
ISOLATION-MODE REJECTION VS GAIN



ISOLATION-MODE REJECTION VS FREQUENCY



AC AND DC LEAKAGE CURRENT VS ISOLATION VOLTAGE



INSTALLATION AND OPERATING INSTRUCTIONS

The 3656 is a very versatile device capable of being used in a variety of isolation and amplification configurations. There are several fundamental considerations that determine configuration and component value constraints:

1. Consideration must be given to the load placed on the resistance (pin 10 and pin 11) by external circuitry. Their output resistance is 100kΩ and a load resistor of 2MΩ or greater is recommended to prevent a voltage divider loading effect in excess of 5%.
2. Demodulator loadings should be closely matched so their output voltages will be equal. (Unequal demodulator output voltages will produce a gain error.) At the 2MΩ level, a matching error of 5% will cause an additional gain error of 0.25%.
3. Voltage swings at demodulator outputs should be limited to 5V. The output may be distorted if this limit is exceeded. This constrains the maximum allowed gains of the input and output stages. Note that the voltage swings at demodulator outputs are tested with 2MΩ load for a minimum of 5V.
4. Total current drawn from the internal isolated supplies must be limited to less than ±5mA per supply and limited to a total of 10mA. In other words, the combination of external and internal current drawn from the internal circuitry which feeds the +V, -V, V+ and V- pins should be limited to 5mA per supply (total current to +V, -V, V+ and V- limited to 10mA). The internal filter capacitors for ±V are 0.01μF. If more than 0.1mA is drawn to provide isolated power for external circuitry (see Figure 12), additional capacitors are required to provide adequate filtering. A minimum of 0.1μF/mA is recommended.
5. The input voltage at pin 7 (noninverting input to A_1) must not exceed the voltage at pin 4 (negative supply voltage for A_1 in order to prevent a possible lockup condition. A low leakage diode connected between pins 7 and 4, as shown in Figure 2, can be used to limit this input voltage swing.
6. Impedances seen by each amplifier's + and - input terminals should be matched to minimize offset voltages caused by amplifier input bias currents. Since the demodulators have a 100kΩ output resistance, the amplifier input not connected to the demodulator should also see 100kΩ.
7. All external filter capacitors should be mounted as close to the respective supply pins as is possible in order to prevent excessive ripple voltages on the supplies or at the output. (Optimum spacing is less than 0.5". Ceramic capacitors recommended.)

POWER AND SIGNAL CONFIGURATIONS

NOTE: Figures 2, 3 and 4 are used to illustrate both signal and power connection configurations. In the circuits shown, the power and signal configurations are independent so that any power configuration could be used with any signal configuration.

ISOLATED POWER CONFIGURATIONS

The 3656 is designed with isolation between the input, the output, and the power connections. The internally generated isolated voltages supplied to A_1 and A_2 may be overridden with external voltages greater than the internal supply voltages. These two features of 3656 provide a great deal of versatility in possible isolation and power supply hook-ups. When external supplies are applied, the rectifying diodes (D_1 through D_4) are reverse biased and the internal voltage sources are decoupled from the amplifiers (see Figure 1). Note that when external supplies are used, they must never be lower than the internal supply voltage.

Three-Port

The power supply connections in Figure 2 show the full three-port isolation configuration. The system has three separate grounds with no galvanic connections between them. The two external 0.47μF capacitors at pins 12 and 16 filter the rectified isolated voltage at the output stage. Filtering on the input stage is provided by internal capacitors. In this configuration continuous isolation voltage ratings are: 3500V between pins 3 and 17; 3500V between pins 3 and 19; 1000V between pins 17 and 19.

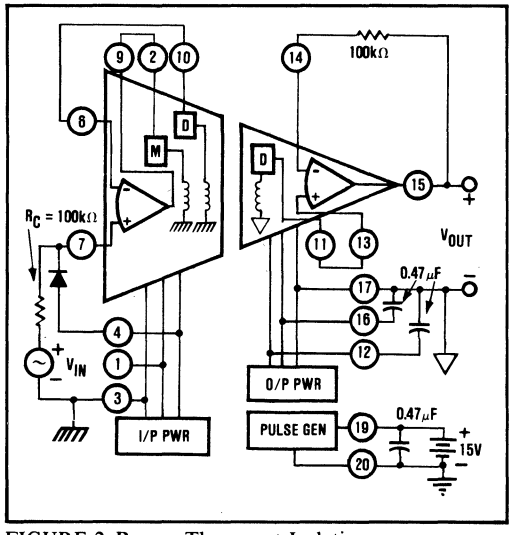


FIGURE 2. Power: Three-port Isolation; Signal: Unity-gain Noninverting.

Two-Port - Bipolar Supply

Figure 3 shows two-port isolation which uses an external bipolar supply with its common connected to the output stage ground (pin 17). One of the supplies (either + or - could be used) provides power to the pulse generator (pins 19 and 20). The same sort of configuration is possible with the external supplies connected to the input stage. With the connection shown, filtering at pins 12 and 16 is not required. In this configuration continuous isolation voltage rating is: 3500VDC between pins 3 and 17; not applicable between pins 17 and 19; 3500VDC between pins 3 and 19.

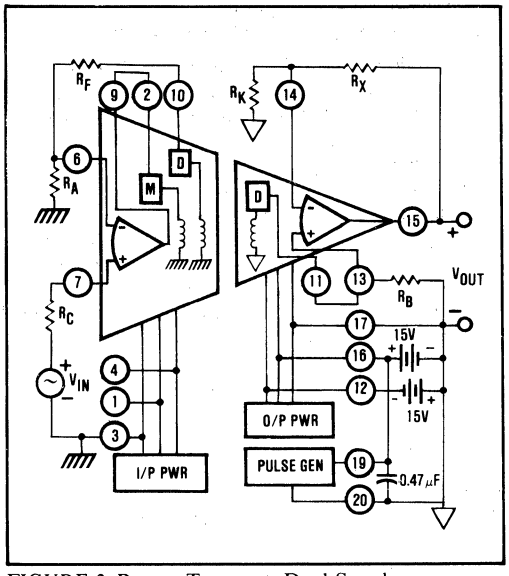


FIGURE 3. Power: Two-port, Dual Supply; Signal: Noninverting Gain.

Two-Port - Single Supply

Figure 4 demonstrates two-port isolation using a single polarity supply connected to the output common (pin 17). The other polarity of supply for A_2 is internally generated (thus the filtering at pin 12). This isolated power configuration could be used at the input stage as well and either polarity of supply could be employed. In this configuration continuous isolation voltage rating is: 3500V between pins 3 and 17; 3500V between pins 3 and 19; not applicable between pins 17 and 19.

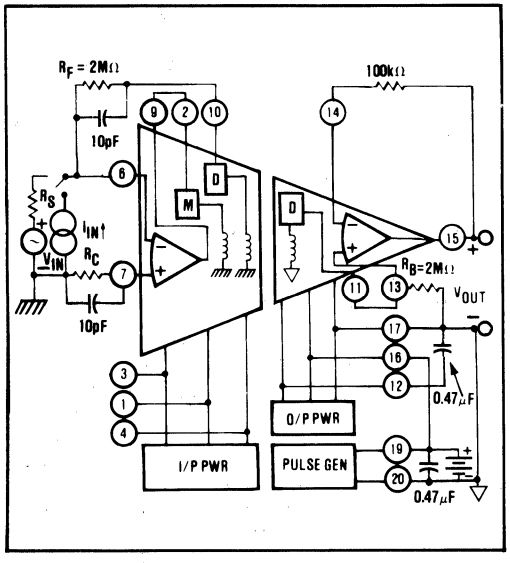


FIGURE 4. Power: Two-port, Single Supply; Signal: Inverting Gains.

SIGNAL CONFIGURATIONS

Unity Gain Noninverting

The signal path portion of Figure 2 shows the 3656 in its simplest gain configuration: unity gain noninverting. The two 100kΩ resistors provide balanced resistances to the inverting and noninverting inputs of the amplifiers. The diode prevents latch up in case the input voltage goes more negative than the voltage at pin 4.

Noninverting With Gain

The signal path portion of Figure 3 demonstrates two additional gain configurations: gain in the output stage and noninverting gain in the input stage. The following equations apply:

Total amplifier gain:

$$G = G_1 \cdot G_2 = V_{OUT}/V_{IN} \quad (1)$$

Input Stage:

$G_1 = 1 + (R_F/R_A)$ (Select G_1 to be less than 5V/full scale V_{IN} to limit demodulator output to 5V) (2)

$R_A + R_F \geq 2M\Omega$ (Select to load input demodulator with at least 2MΩ) (3)

$$R_C = R_A \parallel (R_F + 100k\Omega) = \frac{R_A (R_F + 100k\Omega)}{R_A + R_F + 100k\Omega}$$

(Balance impedances seen by the + and - inputs of A_1 to reduce input offset caused by bias current) (4)

Output Stage:

$G_2 = 1 + (R_X/R_K)$ (Select ratio to obtain V_{OUT} between 5V and 10V full scale with V_{IN} at its maximum) (5)

$R_X \parallel R_K = 100k\Omega$ (Balance impedances seen by the + and - inputs of A_2 to reduce effect of bias current on the output offset) (6)

$R_B = R_A + R_F$ (Load output demodulator equal to input demodulator) (7)

Inverting Gain, Voltage or Current Input

The signal portion of Figure 4 shows two possible inverting input stage configurations: current input and voltage input.

Input Stage:

For the voltage input case:

$G_1 = -R_F/R_S$ (Select G_1 to be less than 5V/full scale V_{IN} to limit the demodulator output voltage to 5V) (8)

$R_F = 2M\Omega$ (Select to load the demodulator with at least 2MΩ) (9)

$$R_C = R_S \parallel (R_F + 100k\Omega) = \frac{R_S (R_F + 100k\Omega)}{R_S + R_F + 100k\Omega}$$

(Balance the impedances seen by the + and - inputs of A_1.) (10)

For the current input case:

$$V_{OUT} = -I_{IN} R_F \cdot G_2 \quad (11)$$

$$R_C = R_F \quad (12)$$

R_F may be made larger than 2MΩ if desired. The 10pF capacitors are used to compensate for the input capacitance of A_1 and to insure frequency stability.

Output Stage:

The output stage is the same as shown in equations (5), (6), and (7).

Illustrative Calculations:

The maximum input voltage is 100mV. It is desired to amplify the input signal for maximum accuracy. Noninverting output is desired.

Input Stage:

Step 1

G_1 max = 5V/Max Input Signal = 5V/0.1V = 50V/V

With the above gain of 50V/V, if the input ever exceeds 100mV, it would drive the output to saturation. Therefore, it is good practice to allow reasonable input overrange.

So, to allow for 25% input overrange without saturation at the output, select

$$G_1 = 40V/V$$

$$G_1 = 1 + (R_F/R_A) = 40$$

$$\therefore R_F/R_A = 39 \quad (13)$$

Step 2

$R_A + R_F$ forms a voltage divider with the 100kΩ output resistance of the demodulator. To limit the voltage divider loading effect to no more than 5%, $R_A + R_F$ should be chosen to be at least 2MΩ. For most applications, the 2MΩ should be sufficiently large for $R_A + R_F$. Resistances greater than 2MΩ may help decrease the loading effect, but would increase the offset voltage drift.

The voltage divider with $R_A + R_F = 2M\Omega$ is 2MΩ/ (2MΩ + 100kΩ) = 2/(2 + 0.1) = 95.2%, i.e., the percent loading is 4.8%

Choose $R_A + R_F = 2M\Omega$ (14)

Step 3

Solving equations (13) and (14)

$R_A = 50k\Omega$ and $R_F = 1.95M\Omega$

Step 4

The resistances seen by the + and - input terminals of the input amplifier A1 should be closely matched in order to minimize offset voltage due to bias currents.

$$\therefore R_C = R_A \parallel (R_F + 100k\Omega)$$
$$= 50k\Omega \parallel (1.95M\Omega + 100k\Omega)$$
$$\cong 49k\Omega$$

Output Stage:

Step 5

$$V_{OUT} = V_{IN\ MAX} \cdot G_1 \cdot G_2$$

As discussed in Step 1, it is good practice to provide 25% input overrange.

So we will calculate G_2 for 10V output and 125% of the maximum input voltage.

$$\therefore V_{OUT} = (1.25 \times 0.1)(G_1)(G_2)$$
i.e., $10V = 0.125 \times 40 \times G_2$
$$\therefore G_2 = 10V/5V = 2V/V$$

Step 6

$$G_2 = 1 + (R_X/R_K) = 2.0$$
$$\therefore R_X/R_K = 1.0$$
$$\therefore R_X = R_K \quad (15)$$

Step 7

The resistance seen by the + input terminal of the output stage amplifier A_2 (pin 13) is the output resistance 100kΩ of the output demodulator. The resistance seen by the - input terminal of A_2 (pin 14) should be matched to the resistance seen by the + input terminal.

The resistance seen by pin 14 is the parallel combination of R_X and R_K.

$$\therefore R_X \parallel R_K = 100k\Omega$$
i.e., $(R_X \cdot R_K/(R_X + R_K) = 100k\Omega$
i.e., $R_K/[1 + (R_K/R_X)] = 100k\Omega \quad (16)$

Step 8

Solving equations (15) and (16) $R_K = 200k\Omega$ and $R_X = 200k\Omega$.

Step 9

The output demodulator must be loaded equal to the input demodulator.

$$\therefore R_B = R_A + R_F = 2M\Omega$$

(See equation (14) above in Step 2)

Use the resistor values obtained in Steps 3, 4, 8 and 9, and connect the 3656 as shown in Figure 3.

OFFSET TRIMMING

Figure 5 shows an optional offset voltage trim circuit. It is important that $R_A + R_F = R_B$.

CASE 1: Input and output stages in low gain, use output potentiometer (R_2) only. Input potentiometer (R_1) may be disconnected. For example, unity gain could be obtained by setting $R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_1 = 0$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 2: Input stage in high gain and output stage in low gain, use input potentiometer (R_1) only. Output potentiometer (R_2) may be disconnected. For example, $G_T = 100$ could be obtained by setting $R_F = 2M\Omega$, $R_B = 2M\Omega$ returned to pin 17, $R_A = 20k\Omega$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 3: When it is necessary to perform a two-stage precision trim (to maintain a very small offset change under conditions of changing temperature and changing gain in A_1 and A_2), use step 1 to adjust the input stage and step 2 for the output stage. Carbon composition resistors are acceptable but potentiometers should be stable.

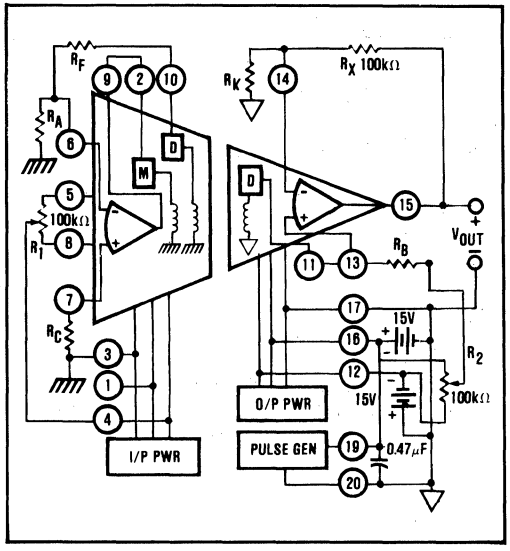


FIGURE 5. Optional Offset Voltage Trim.

Step 1: Input stage trim ($R_A = R_C = 20k\Omega$, $R_F = R_B = 20M\Omega$, $R_X = 100k\Omega$, $R_K = \infty$, R_2 disconnected); A_1 high, A_2 low gain. Adjust R_1 for 0V ±5mV or desired setting at V_{OUT}, pin 15.

Step 2: Output stage trim ($R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, $R_K = \infty$, R_1 and R_2 connected); A_1 low, A_2 low gain. Adjust R_2 for 0V ±1mV or desired setting at V_{OUT}, pin 15 (±110mV approximate total range).

Note: Other circuit component values can be used with valid results.

APPLICATIONS

ECG AMPLIFIER

Although the features of the circuit shown in Figure 6 are important in patient monitoring applications, they may also be useful in other applications. The input circuitry uses an external, low quiescent current op amp (OPA21 type) powered by the isolated power of the input stage to form a high impedance instrumentation amplifier input (true three-wire input). R_3 and R_4 give the input stage amplifier of the 3656 a noninverting gain of 10 and an inverting gain of -9. R_1 and R_2 give the external amplifier a noninverting gain of 1 + 1/9. The inputs are applied to the noninverting inputs of the two amplifiers and the composite input stage amplifier has a gain of 10.

The 330kΩ, 1W, carbon resistors and diodes D_1 - D_4 provide protection for the input amplifiers from defibrillation pulses.

The output stage in Figure 6 is configured to provide a bandpass filter with a gain of 22.7 (68MΩ/3MΩ). The high-pass section (0.05Hz cutoff) is formed by the 1μF capacitor and 3MΩ resistor which are connected in series between the output demodulator and the inverting input of the output stage amplifier. The low-pass section (100Hz cutoff) is formed by the 68MΩ resistor and 22pF capacitor located in the feedback loop of the output stage. The diodes provide for quick recovery of the high-pass filter to overvoltages at the input. The 100kΩ pot and the 100MΩ resistor allow the output voltage to be trimmed to compensate for increased offset voltage caused by unbalanced impedances seen by the inputs of the output stage amplifier.

In many modern electrocardiographic systems, the

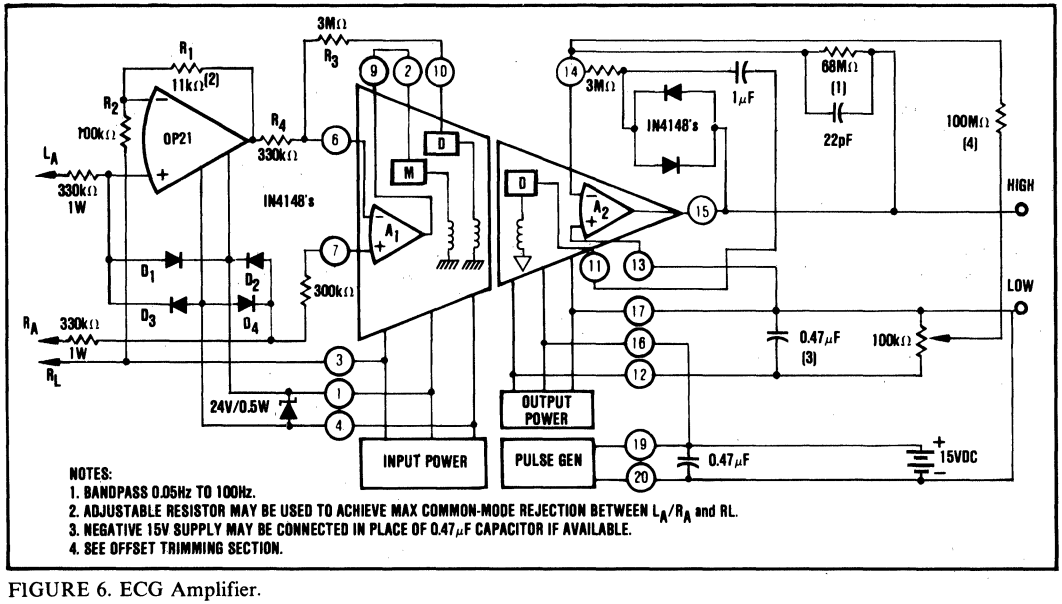


FIGURE 6. ECG Amplifier.

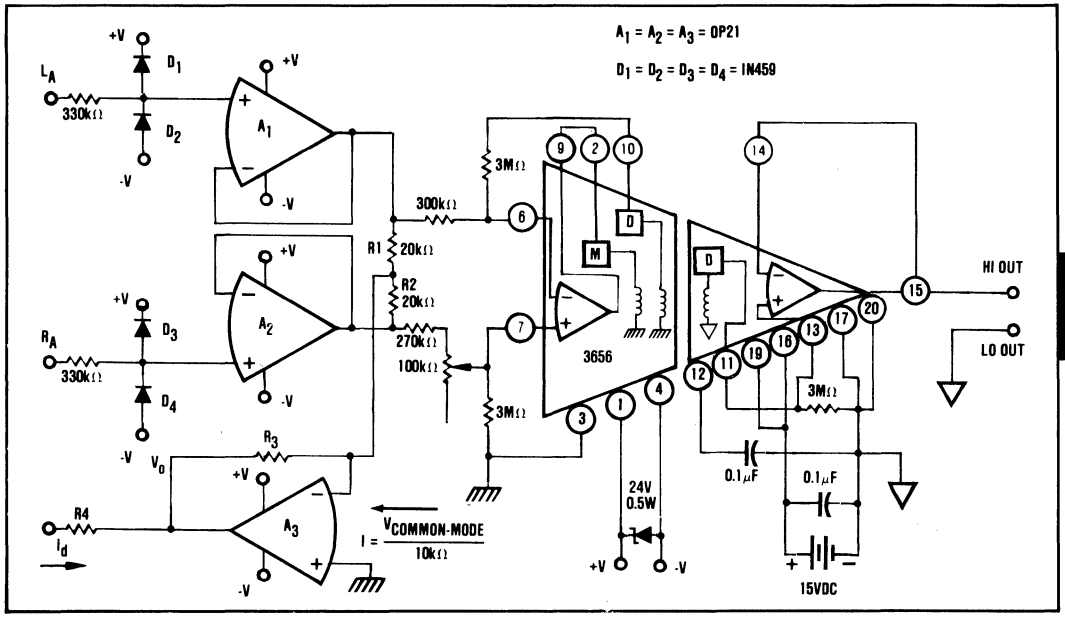


FIGURE 7. Driven Right-Leg ECG Amplifier.

patient is not grounded. Instead, the right-leg electrode is connected to the output of an auxiliary operational amplifier as shown in Figure 7. In this circuit, the common-mode voltage on the body is sensed by the two averaging resistors R_1 and R_2, inverted, amplified, and fed back to the right-leg through resistor R_4. This negative feedback drives the common-mode voltage to a low value. The body's displacement current i_d does not flow to ground, but rather to the output circuit of A_3. This reduces the pickup as far as the ECG amplifier is concerned and effectively grounds the patient.

The value of R_4 should be as large as practical to isolate the patient from ground. The resistors R_3 and R_4 may be selected by these equations:

$$R_3 = (R_1/2)\,(V_o/V_{CM}) \text{ and } R_4 = (V_{CM} - V_o)/i_d$$

$$(-10V \leq V_o \leq +10V \text{ and } -10V \leq V_{CM} \leq +10V)$$

where V_o is the output voltage of A_3 and V_{CM} is the common-mode voltage between the inputs LA and RA and the input common at pin 3 of the 3656.

This circuit has the added benefit of having higher common-mode rejection than the circuit in Figure 6 (approximately 10dB improvement).

BIPOLAR CURRENT OUTPUT

The three-port capability of the 3656 can be used to implement a current output isolation amplifier function, usually difficult to implement when grounded loads are involved. The circuit is shown in Figure 8 and the following equations apply:

$$G = I_{OUT}/V_{IN} = 1 + \frac{R_F}{R_A} \times \frac{R_2}{(R_1 + R_2) \cdot R_S}$$

$$I_{OUT} \leq \pm 2.5mA$$

$$V_L \leq \pm 4V \text{ (compliance)}$$

$$R_L \leq 1.6k\Omega$$

$$R_F + R_A = R_1 + R_2 \geq 2M\Omega$$

CURRENT OUTPUT - LARGER UNIPOLAR CURRENTS

A more practical version of the current output function is shown in Figure 9. If the circuit is powered from a source greater than 15V as shown, a three-terminal regulator should be used to provide 15V for the pulse generator (pins 19 and 20). The input stage is configured as a unity gain buffer, although other configurations such as current input could be used. The circuit uses the isolation feature between the output stage and the primary power supply to generate the output current configuration that can work into a grounded load. Note that the output transistors can only drive positive current into the load. Bipolar current output would require a second transistor and dual supply.

ISOLATED 4mA TO 20mA OUTPUT

Figure 10 shows the circuit of an expanded version of the isolated current output function. It allows any input voltage range to generate the 4mA to 20mA output excursion and is also capable of zero suppression. The "span" (gain) is adjusted by R_2 and the "zero" (4mA output for minimum input) is set by the 200kΩ pot in the output stage. A three-terminal 5V reference is used to provide a stable 4mA operating point. The reference is

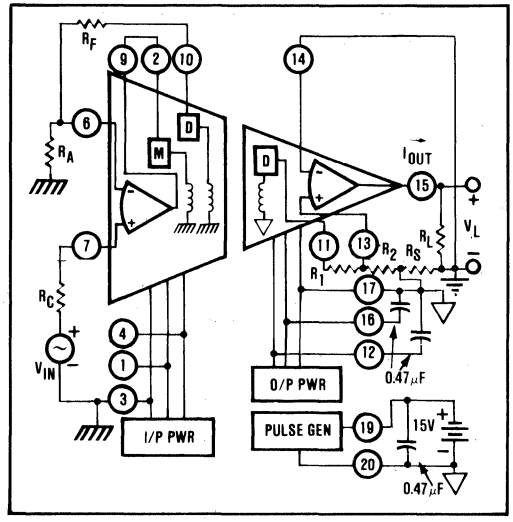


FIGURE 8. Bipolar Current Output.

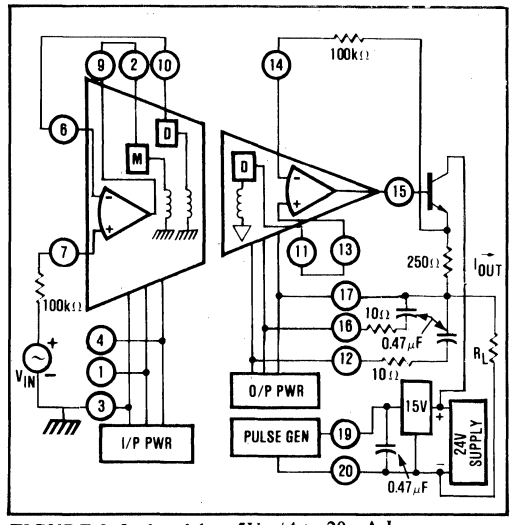


FIGURE 9. Isolated 1 to $5V_{IN}/4$ to 20mA I_{OUT}.

connected to insert an adjustable bias between the demodulator output and the noninverting input of the output stage amplifier.

DIFFERENTIAL INPUT

Figure 11 shows the proper connections for differential input configuration. The 3656 is capable of operating in this input configuration only for floating loads (i.e., the source V_{IN} has no connection to the ground reference established at pin 3). For this configuration the usual 2MΩ resistor used in the input stage is split into two halves, R_F and R_{F-}. The demodulator load (seen by pin 10 with respect to pin 3) is still 2MΩ for the floating load as shown. Notice pin 19 is common in Figure 11 whereas pin 20 is common in previous figures.

SERIES STRING SOURCE

Figure 12 shows a situation where a small voltage, which is part of a series string of other voltages, must be measured. The basic problem is that the small voltage to be measured is 500V above the system ground (i.e., a system common-mode voltage of 500V exists). The circuit converts this system CMV to an amplifier isolation mode voltage. Thus, the isolation voltage ratings and isolation-mode rejection specifications apply.

IMPROVED INPUT CHARACTERISTICS

In situations where it is desired to have better DC input amplifier characteristics than the 3656 normally provides it is possible to add a precision operational amplifier as shown in Figure 13. Here the instrumentation grade Burr-Brown 3510 is supplied from the isolated power of the input stage. The 3656 is configured as a unity-gain buffer. The gain of the 3510 stage must be chosen to limit its full scale output voltage to 5V and avoid overdriving the 3656's demodulators. Since the 3656 draws a

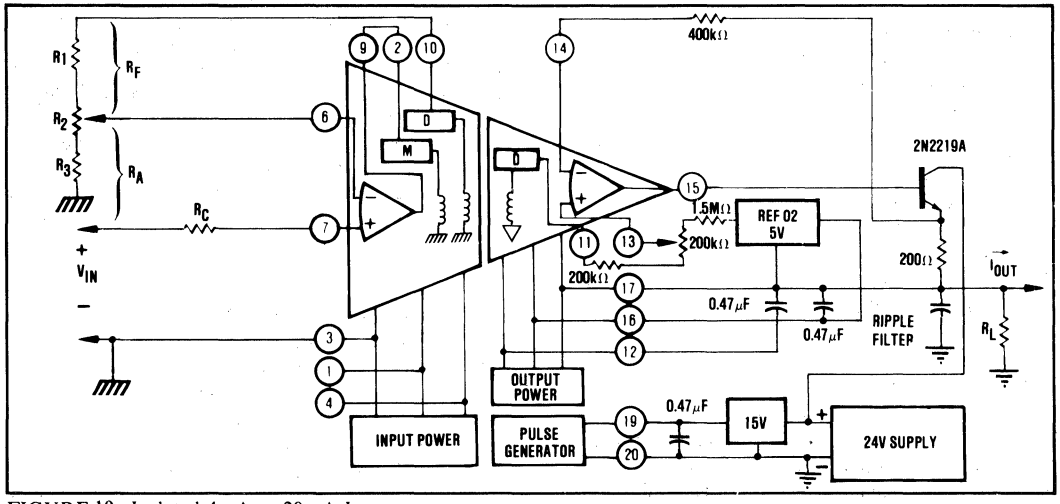


FIGURE 10. Isolated 4mA to 20mA I_{OUT}.

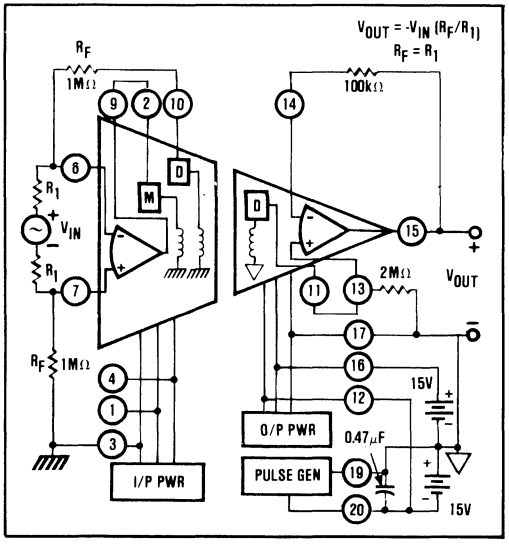


FIGURE 11. Differential Input, Floating Source.

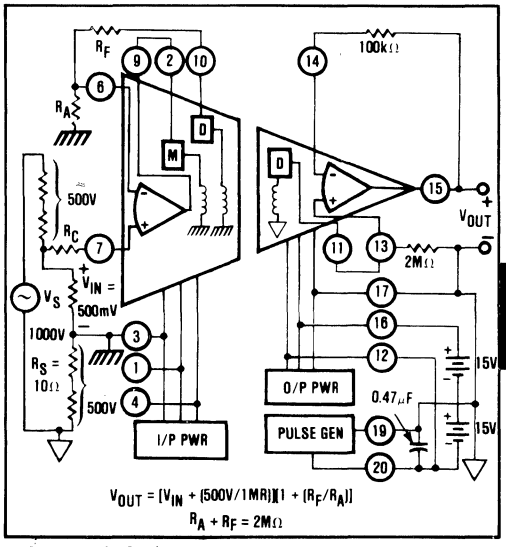


FIGURE 12. Series Source.

significant amount of supply current, extra filtering for the input supply is required as shown (2 x 0.47μF).

ELECTROMAGNETIC RADIATION

The transformer coupling used in the 3656 for isolation makes the 3656 a source of electromagnetic radiation unless it is properly shielded. Physical separation between the 3656 and sensitive components may not give sufficient attenuation by itself. In these applications the use of an electromagnetic shield such as the Burr-Brown 100MS is a must. This shield is especially designed for use with the 3656 package. It provides shielding in all directions. Note that the offset voltage appearing at pin 15 may change by 4mV to 12mV with use of the shield; however, this can be trimmed (see Offset Trimming Section).

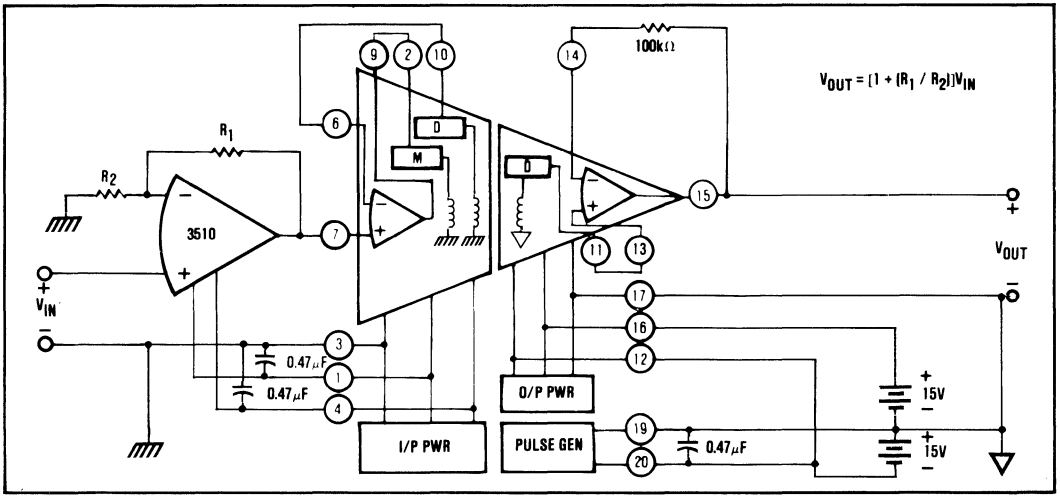


FIGURE 13. Isolator for Low-Level Signals.

FIBER OPTIC DATA LINKS

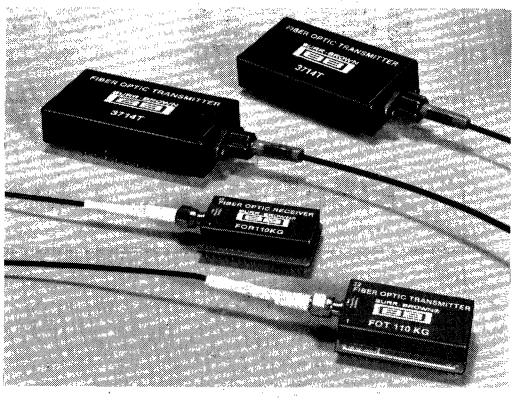
Total noise immunity and electrical isolation are provided by these fiber optic data links designed to convert TTL or analog input signals to output light signals and transmit data - with maximum accuracy -through severe electrical environments.

These DC-coupled links are data pattern independent. Special coding is not required and asynchronous data can be accepted.

3714T is a self-contained transmitter whose output is a train of light pulses whose frequency is directly proportional to the magnitude of an analog input signal. It's capable of transmitting analog signals as small as 10mV FS up to 1.7km with a linearity error of ±0.005%.

FOT110 transmitter/FOR110 receiver are compact IC packages (2.1" x 1.2" x 0.4" / 43.1mm x 27.9mm x 10.1mm) that transmit TTL inputs at data data rates of 0 to 2M bits at distances up to 7.4km without repeaters.

They also can transmit analog signals as amplitude modulation of the light output in a 10Hz to 1MHz bandwidth.



SPECIAL OFFER* - COMPLETE DATA LINK

Here is an easy and inexpensive way to evaluate fiber optics in your application. Each FODL (Fiber Optic Data Link) contains a transmitter, receiver, two electrical sockets and factory terminated fiber optic cable. Apply power and you have a complete functioning link ready for experimentation in your own application. FODL-K1, $99; FODL-K2, $125; FODL-K3, $155; FODL-K4, $143.

*Limit one of each link per customer.

4

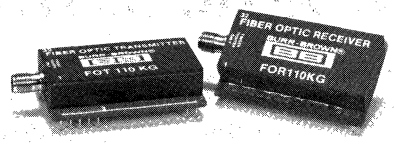
SELECTION GUIDE

FIBER OPTICS											
Transmitter/Receiver	Input	Output	Data Rate	Wavelength	Link Length(1)	Auto-Threshold™	Adjustable Light Output	Price(2) $ Units	Price(2) $ 100's	FODL(3) Number	Page
FOT110KG/FOR110KG	TTL	TTL	0 to 2M bits	665nm	1900M(4)	Yes	Yes	218.00	143.00	FODL-K4	4-2
FOT110KG-IR/FOR110KG	TTL	TTL	0 to 1M bit	880nm	7400M(5)	Yes	Yes	225.00	147.50	--	4-2
3712T/3712R	TTL	TTL	0 to 25k bits	670nm	2290M(6)	Yes	No	153.00	118.00	FODL-K1	4-14
3713T/3713R	TTL	TTL	0 to 250k bits	660nm	2500M(6)	Yes	Yes	193.00	153.00	FODL-K2	4-22
3714T/3713R	Analog	TTL(7)	0 to 10kHz	660nm	2500M(6)	Yes	Yes	270.00	208.75	FODL-K3	4-30

FIBER OPTIC CABLE ASSEMBLIES							
Model	Conditions	Core Material	Attenuation	Numerical Aperature	Rise Time	Price	Page
OCA100	λ = 660nm	Plastic	1300dBm/km	0.53	--	$1.60/m + $20 Cable Term.	4-10
OCA101	λ = 660nm	Plastic	360dBm/km	0.53	5.5nsec/km	$4.80/m + $20 Cable Term.	4-10
OCA102	λ = 660nm	Silica	33dBm/km	0.40	3.8nsec/km	$6.40/m + $20 Cable Term.	4-10

NOTES: 1) Without repeaters. 2) Transmitter and receiver may be purchased separately. 3) See "Special Offer" above. 4) 200μM core dia., 12dB/km attenuation. 5) 63μM core dia., 2dB/km attenuation. 6) 200μM core dia., 8dB/km attenuation. 7) May be converted to analog with a Voltage-to-Frequency converter.

BURR-BROWN®



FOT110
FOR110

High Performance Digital/Analog FIBER OPTIC TRANSMITTER AND RECEIVER

FEATURES

- HIGH SENSITIVITY
- INTERNAL SQUELCH
- TTL (0 to 2M baud, typ) AND LINEAR AMPLITUDE MODULATION (1MHz, typ)
- TRUE DC RESPONSE (data pattern independent)
- LOW BIT ERROR RATE (to 10^{-14})
- AUTO THRESHOLD™
- LINK MONITORING
- UP TO 7KM IN SILICA OR 100 METERS IN ALL-PLASTIC FIBERS
- IMMUNE TO EMI AND ELECTRICALLY ISOLATED

APPLICATIONS

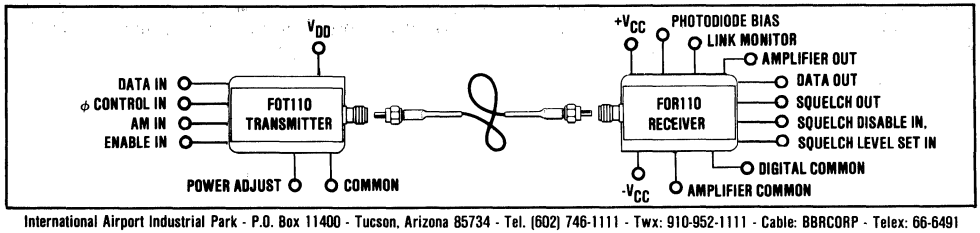
- INDUSTRIAL/PROCESS CONTROL
- REMOTE INSTRUMENTATION SYSTEMS
- NUCLEAR POWER PLANT CONTROL
- TRANSFER OF FACTORY COMPUTER DATA
- MULTIPLEXED DATA LINK (TDM or FDM)
- DIGITAL PHONE SYSTEM (standard T1)
- HIGH VOLTAGE TRANSMISSION LINE MONITORING
- LIGHTNING IMMUNE SYSTEM
- SYSTEMS REQUIRING INTRINSIC SAFETY

DESCRIPTION

The FOT/FOR110 fiber optic transmitter and receiver, together with a suitable fiber optic cable, form a versatile digital data and analog signal link. TTL data (up to 2M baud NRZ) applied to the transmitter input is converted to an optical signal. This is accepted by the receiver and reproduced as TTL data at its output. The receiver has Auto Threshold™ adjustment including a squelch function. True DC response is achieved, and the recovery scheme is independent of the data pattern, for example, Manchester coding is not required. An analog signal (10Hz to 1MHz) can also be transmitted with high linearity. No external adjustments are necessary and link lengths greater than 1.7km can be attained with silica fibers. Longer lengths, up to 7km without repeaters, are possible with the infrared (IR) transmitter version. In addition, the hybrid package permits mounting on printed circuit boards.

The FOT110 is a hybrid fiber optic transmitter capable of 0 to 2M baud data rate. Although most applications will have separate functions, it can uniquely transmit an analog signal by amplitude modulation (AM) simultaneously with a digital TTL signal over one cable. Pin-selectable LED phasing may be used to generate biphase data through the link if desired. Transmitter optical output is specified as actual power launched and is adjustable allowing very-short links without receiver overload. The LED color is bright red, making troubleshooting easier without expensive test or image converter scopes. The IR transmitter offers higher power for longer link lengths, although the light is not visible.

The FOR110 is a very-high sensitivity hybrid fiber optic receiver capable of 0 to 2M baud NRZ data rate, typical. The Auto Threshold™ circuit continuously sets the Data Out threshold for maximum noise immunity. A single external capacitor can reduce bandwidth. This lowers the bit error rate and increases sensitivity for lower baud rate applications.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-455

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C, V_{DD} = +5VDC for transmitter and ±V_{CC} = 15VDC for receiver unless otherwise noted.

RECEIVER					
			FOR110KG(1)		
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
AMPLIFIER SECTION					
Responsivity (665nm to 880nm)	200µm, NA ≤ 0.5		1		V/µW
Fiber Pigtail Core Diameter			375		µm
Fiber Pigtail NA	-10dB	0.5	0.66		
Output Signal (max undistorted)	R_L = ≤50kΩ	5	7.5		V_{PEAK}
Output Noise	No signal, C_{BW} = 47pF, BW = 10Hz to 2MHz		0.8	2.5	mV, rms
Output Bandwidth	Bias = 0V, -3dB	DC to 0.5	DC to 1		MHz
Output Offset	Input and Bias = 0 (dark)		1	5	mV
Power Supply Rejection, Amplifier Output	ΔVCC = ±1VDC		60		dB
DIGITAL SECTION					
Bit Rate(2)	NRZ, Bias = 0	0 to 1M	0 to 2M		Baud
Duty Cycle(3)		0		100	%
Sensitivity(4)	BER = 10^{-9}, Bias = 0V*	32	15		nW
		-45	-48		dBm
Propagation Delay	50% In/Out		0.8		µsec
Fan Out, Data Out	Without external pull-up resistor	2	4		Unit Loads
TTL Output "High"	I_O = 200µA	2.4	3.2		V
TTL Output "Low"	I_O = 6.4mA		0.3	0.5	V
Logic Polarity, Data Out	No Input		Low		
Squelch Out, Data Out	I_O = 10mA		0.25		V
POWER SUPPLY					
Voltage		±11.5	±15	±16	VDC
Current	±V_{CC} = 15VDC		±37	±46	mA DC
TEMPERATURE RANGE		0		+70	°C

TRAMSMITTER								
		FOT110KG			FOT110KG-IR			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OPTICAL OUTPUT SECTION								
Baud Rate	NRZ, P_O max	0 to 2M	0 to 4M		0 to 0.75M	0 to 1M		Baud
Output Power, into fiber(5)	200µm, NA = 0.48	5	10		50	90		µW
		-23	-20		-13	-10.5		dBm
Power Adjustment Range	Maximum to Minimum	16	23		16	23		dB
Wavelength of LED, λ peak(6)	P_O max	650	665	680	850	880	910	nm
Spectral Width of LED(6)	-3dB from P_O max		25			80		nm
Fiber Pigtail Core Diameter			375			375		µm
Fiber Pigtail NA	-10dB		0.66			0.66		
T_R, T_F (rise and fall times)	10% to 90%; P_O max		150	250		600	850	nsec
T_P (propagation delay)	100KB/sec; 50% In/Out; P_O max		120			480		nsec
T_E (enable delay)	100KB/sec; 50% In/Out; P_O max		120			480		nsec
DIGITAL TTL INPUT								
Input "High" Voltage	T_A = 0 to +70°C	2			2			V
Input "Low" Voltage	T_A = 0 to +70°C			0.8			0.8	V
Input "High" Current	V_S = +5.25V; V_{IN} = +2.7V; 0 to +70°C			-40			-40	µA
Input "Low" Current	V_S = +5.25V; V_{IN} = +0.4V; 0 to +70°C			-0.8			-0.8	mA
ANALOG AM INPUT								
Input Impedance	Input, Enable and ϕ = High, f = 1kHz		100			100		Ω
Input Sensitivity	Input, Enable and ϕ = High, f = 1kHz, AM = 100%		1.1			1.1		V, p-p
AM Bandwidth	Input = 1V, p-p, Output at -3dB, P_O max	1	2.5		0.3	1		mHz
AM Distortion (total harmonic distortion)	Mod = 50%, f = 1kHz, P_O max		1.3			0.6		%
POWER SUPPLY								
Voltage		4.75	5	5.25	4.75	5	5.25	V
Current (LED off)	V_{DD} = +5.0V		10.5	17		10.5	17	mA
Current (LED on)	V_{DD} = +5.0V		118	135		118	135	mA
TEMPERATURE RANGE		0		+70	0		+70	°C

* 665nm (1MB/sec); 880nm (0.8MB/sec).

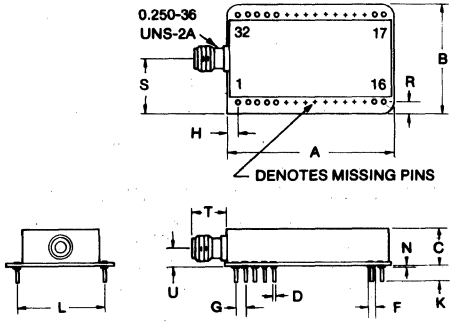
NOTES
1. FOR110KG operates with FOT110KG or FOT110KG-IR.
2. See Theory of Operation and Application sections regarding operation of Automatic Threshold circuit. For baud rates less than 2, use squelch function to eliminate unwanted error due to noise.
3. Input should be limited to 1μW to avoid duty cycle distortion.
4. May be improved with external threshold voltage trim and bandwidth limiting capacitor (C_{BW}). See Theory of Operation and Application sections.
5. Optical output power is adjustable. See Application Information section. Optical power is measured into an exit numerical aperture (NA) of 0.48 and a core diameter of 200μm. For other cable core diameters and NA see Typical Performance Curves and Cable Selection section.
6. The IR version offers increased optical output power and longer links with a decrease in bandwidth.

ABSOLUTE MAXIMUM RATINGS

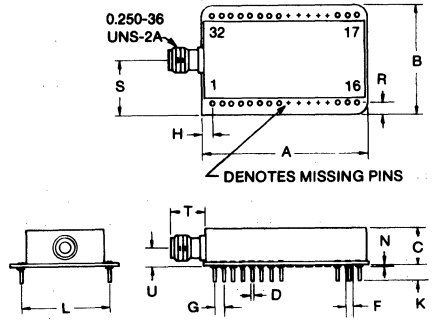
TRANSMITTER		RECEIVER	
$+V_{DD}$	+5.25V	$\pm V_{CC}$	±16V
Data In, Enable In, and ϕ Control In	+5.25V	Squelch Disable Input	+5.25V
AM In	+1.2Vp	Squelch and Data Out Pull-Up Voltage	+30V
Storage Temperature Range	-55°C to +85°C	Squelch Level Set	+5V
Operating Temperature Range	-40°C to +70°C	Photodiode Bias	+30V, max; 0V, min
Lead Temperature (soldering 10sec)	+300°C	Storage Temperature Range	-55°C to +85°C
		Operating Temperature Range	-40°C to +70°C
		Lead Temperature (soldering 10sec)	+300°C

MECHANICAL

FOT110 (TRANSMITTER)



FOR110 (RECEIVER)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.710	1.750	43.43	44.45
B	1.106	1.140	28.09	28.96
C	.370	.430	9.40	10.92
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30
S	.530	.590	13.46	14.99
T	.345	.355	8.76	9.02
U	.192	.220	4.88	5.59

NOTES:
1. Leads in true position within 0.10" (0.25MM) R at MMC at seating plane.
2. Pin numbers shown for reference only. Numbers may not be marked on package.
3. Maximum optical connector torque - 5in/oz.
4. Connector compatible with Amphenol 905 and 906 series or other similar SMA series.

PIN CONFIGURATION, TRANSMITTER

1. Package Shield
2. AM In
3. Data In
4. ϕ Control In*
5. *
15. Power Adj.
16. Common and package shield
17. Package Shield
18. V_{DD}
28. Enable In**
29. **
30. **
31. **
32. Package Shield

*These pins are connected together internally.
**These pins are connected together internally.

PIN CONFIGURATION, RECEIVER

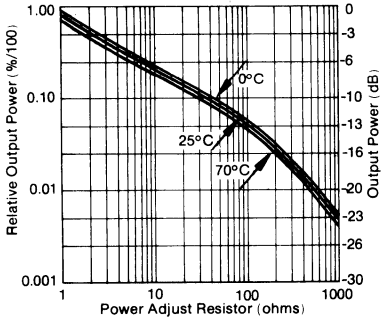
1. Package Shield
2. Data Out
3. Digital Common
4. $+V_{CC}$
5. $-V_{CC}$
6. Link Monitor
7. Amplifier Common
8. Amplifier Out
14. NC*
15. NC*
16. Package Shield
17. Package Shield
18. Photodiode Bias
19. NC*
25. NC*
26. NC*
27. NC*
28. Squelch Disable In
29. Squelch Out
30. Squelch Level Set In
31. NC*
32. Package Shield

*No internal connection.

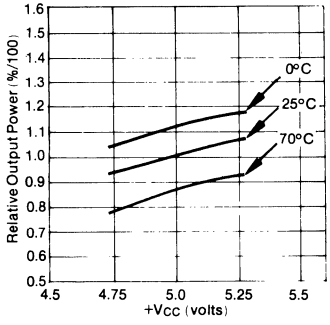
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, V_{DD} = +5VDC, ±V_{CC} = 15VDC, unless otherwise noted)

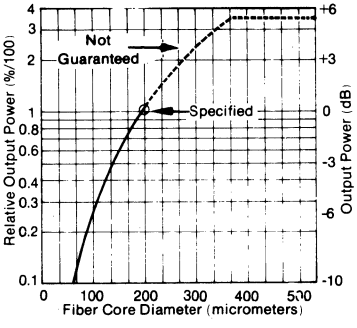
TRANSMITTER OPTICAL OUTPUT POWER VS POWER ADJUST RESISTOR AND TEMPERATURE



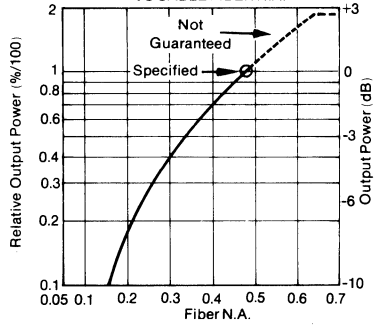
OPTICAL OUTPUT POWER VS AMBIENT TEMPERATURE AND +Vcc



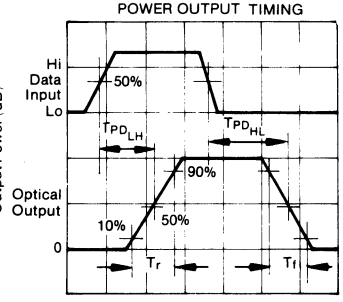
LAUNCHED OUTPUT POWER VS CABLE CORE DIAMETER



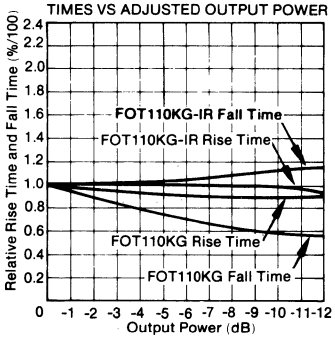
LAUNCHED OUTPUT POWER VS CABLE FIBER N.A.



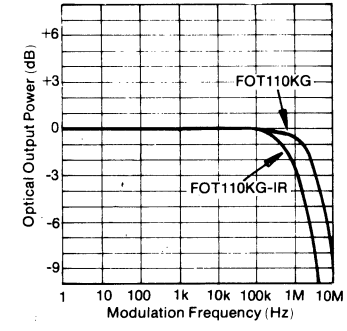
DATA INPUT AND OPTICAL POWER OUTPUT TIMING



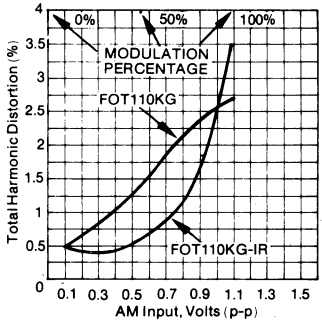
OPTICAL OUTPUT RISE AND FALL TIMES VS ADJUSTED OUTPUT POWER



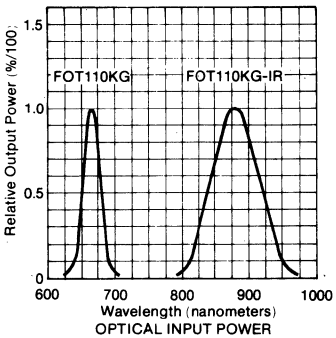
OUTPUT POWER VS MODULATION FREQUENCY, TYPICAL AT 25°C



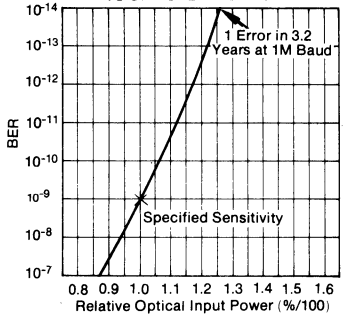
TOTAL HARMONIC DISTORTION VS AM INPUT, TYPICAL AT 25°C



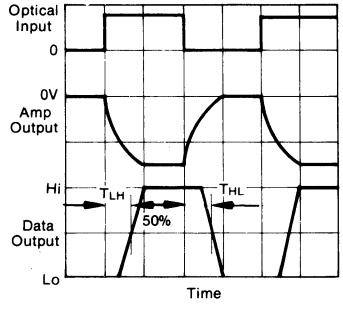
TRANSMITTER SPECTRAL OUTPUT



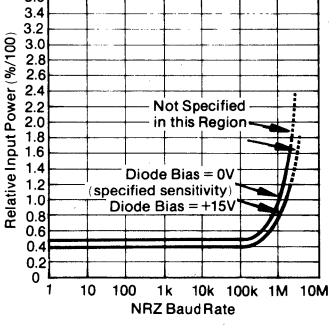
BIT ERROR RATE VS OPTICAL INPUT POWER



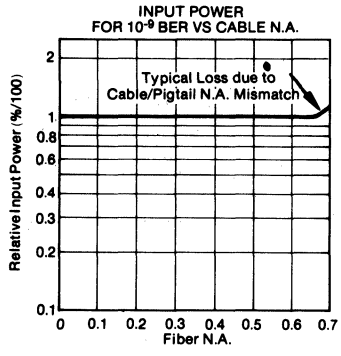
PROPAGATION DELAY VS TIME

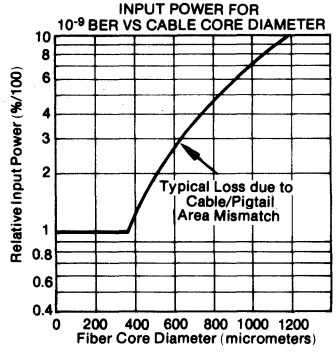


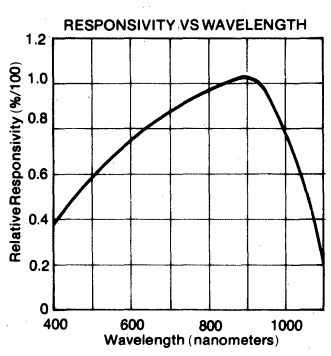
OPTICAL INPUT POWER FOR 10^{-9} BER VS BAUD RATE



FOT110







THEORY OF OPERATION

TRANSMITTER

The FOT110 transmitter, shown in Figure 1, consists of digital input gates, a current mirror, and an LED. The open-collector exclusive OR gates are lower power Schottky TTL.

This circuit can transmit a data rate of at least 2M baud (0.75M baud FOT110KG-IR).

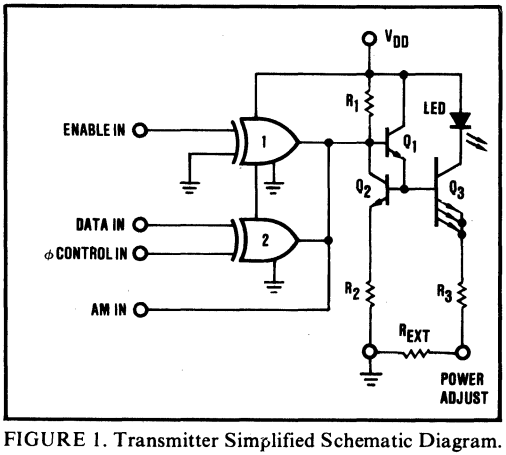


FIGURE 1. Transmitter Simplified Schematic Diagram.

When the Enable In is high ("1"), the Data In will control the state of the LED. The data-LED phase relationship is controlled by applying a "1" or "0" to the ϕ Control In, as shown in Table I.

TABLE I. Transmitter Truth Table.

ENABLE IN	DATA IN	ϕ CONTROL IN	LED
0	X	X	Off
1	0	0	Off
1	1	0	On
1	0	1	On
1	1	1	Off

X = Don't Care

Biphase modulated data can be generated by applying a clock signal to the ϕ Control In and clock-synchronized data to the Data In. This technique reduces the baud rate, but is useful for generating an AC signal. Figure 2 shows a timing diagram.

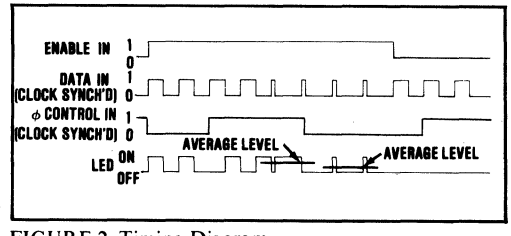


FIGURE 2. Timing Diagram.

The LED is driven by a ratioed current mirror as shown in Figure 1. When the voltage at the base of Q_1 is high ($\geq 2V_{BE}$), the LED is on. With $R_{EXT} = 0$, the LED is at the maximum current of 108mA. Increasing the value of R_{EXT} reduces the LED current and output power. This will reduce power consumption and extend LED lifetime. This also allows operation over very short links without receiver overload. For selection of R_{EXT} see Typical Performance Curves.

The LED can also be intensity modulated directly by the voltage level at the Amplitude Modulation (AM) input. The AM signal can be audio or low frequency RF (up to 1MHz). It should be capacitively-coupled to the input to prevent DC levels from disturbing the transistor bias voltage. In effect, the AM input voltage modulates the LED current causing intensity modulation. A 1.1Vp-p signal through a capacitor to the AM input will provide 100% modulation.

RECEIVER

The FOR110 receiver, shown in Figure 3, consists of a PIN photodiode and transimpedance amplifier, followed by two comparators, one for data and one for squelch. The photodiode converts the incident light signal from the optical fiber to a current corresponding to the received power. Sensitivity and bandwidth can be improved by biasing the photodiode to $+V_{CC}$. However, at temperatures greater than +50°C, sensitivity will be reduced due to photodiode dark current (see Typical

Performance Curves). The current is converted to a voltage by a low noise, high speed, transimpedance amplifier. This voltage, appearing in Figure 4 as an eye

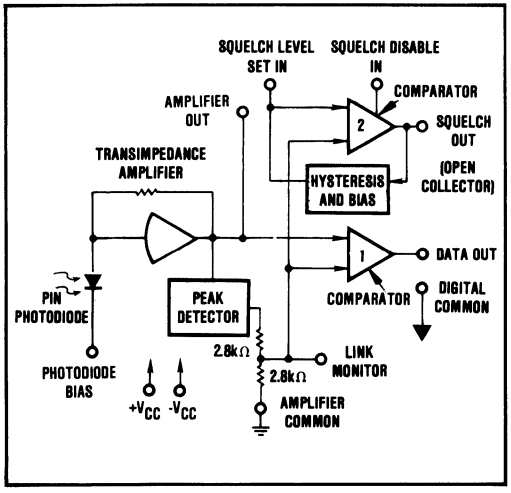


FIGURE 3. Receiver Simplified Schematic.

diagram, will be reconstructed into a TTL output through comparator 1. If the transmitter is amplitude modulated, then the AM signal can be obtained at the amplifier output.

The reference of the comparators is automatically set by the Auto Threshold™ peak detector. This threshold voltage, at the Link Monitor output, is equal to one-half of the amplifier peak output level. This assures that comparator 1 will always switch with maximum noise immunity. Unlike fixed-threshold receivers, this circuit maintains symmetry over a wide dynamic range. In

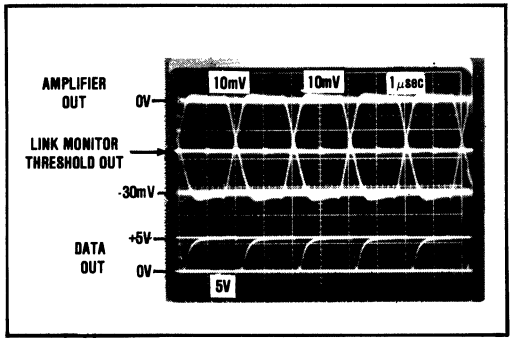


FIGURE 4. Amplifier Output (Eye Diagram) and TTL Data Out. (500k Baud, Diode Bias = 0V, C_{BW} = 47pF, Receiver Input 25nW$_{PEAK}$, λ = 665nm).

addition, it provides improved bit error rate with larger input signals. Since the FOR110 is DC coupled, it allows far greater noise immunity than "edge-triggered" systems. Improved sensitivity can be achieved in lower speed applications by adding an external capacitor between the amplifier output and common. Its value is determined by the following relationship:

$$C_{BW} = \frac{1}{2\pi\ (2.5)\ F_C}$$

where F_C is the 3dB cut-off frequency in kHz and C_{BW} is in microfarads.

The squelch function allows the data output to be cut off by comparators when the optical input power falls below a preset level. This is accomplished by strapping the Squelch Out to the Data Out. With no external connection to the Squelch Level Set In, the squelch level will be approximately 20nW. Squelch can be turned off with "1" applied to the Squelch Disable In. The Link Monitor output can be used to monitor the continuity of the link. The load impedance should be greater than 100kΩ.

CABLE SELECTION

The FOT/FOR110 connector is compatible with Amphenol 905 and 906 series or similar SMA connectors and can be used with a wide variety of cable types. The choice of a cable type depends on the particular application.

The visible (665nm) output of the FOT110KG is well matched for use with low cost all-plastic cable as well as glass and silica fibers. The high power infrared (880nm) output of the FOT110KG-IR provides improved performance with glass and silica fibers. However, use with plastic fibers is severely limited due to high attenuation of these materials in the infrared.

The operating temperature range and mechanical integrity of fiber optic cables varies widely. Consult manufacturers' specifications for specific information; some are shown in Table II. Table III contains calculated link performance for selected fiber optics cables. Performance is based on best available data from fiber optic cable manufacturers at time of printing.

TABLE II. FOT/FOR110 Compatible Cable Manufacturers.

Maxlite Fiber Optic Div. Raychem Corp. of Arizona 3035 N. 33rd Drive Phoenix, AZ 85017 (602) 269-8387	Siecor Optical Cables, Inc. P.O. Box 489 Hickory, NC 28601 (704) 322-3740
E.I.DuPont de Nemours & Company,Inc. DuPont Building D-13121-5 Polymer Products Dept. Wilmington, DE 19898 (302) 774-6339	Telecommunication Products Corning Glass Works Corning, NY 14831 (607) 974-4411
Quartz Products Corporation 688 Somerset St. P.O. Box 1347 Plainfield, NJ 07061 (201) 757-4545	Nissho-Iwai American Corp. Broadway Plaza Suite 1900 700 South Flower Street Los Angeles, CA 90017 (213) 688-0684

TABLE III. Calculated Link for Selected Cables (at +25°C).[1]

TRANSMITTER	CABLE TYPE	FIBER CORE DIAMETER (μm)	FIBER EFFECTIVE[2] NA	FIBER LOSS[2] dB/km		LINK LENGTH m	
				TYP	MAX	WORST CASE[3]	TYPICAL
FOT110KG (Red LED)	All Plastic[4]	368	0.42	260	270	75	118
	Glass/Glass[5]	200	0.38	80	85	219	311
	Plastic Clad Silica[6]	200	0.34	12	15	1203	2028
	Telecom Silica[7]	50	0.20	NOT RECOMMENDED			
	Telecom Silica[8]	100	0.28	9	12	871	1861
	Light Duty Plastic[9]	400	0.5	380	720	34	83
FOT110KG-IR (IR LED)	All Plastic[4]	368	0.42	800	850	42	69
	Glass/Glass[5]	200	0.35	35	45	636	948
	Plastic Clad Silica[10]	200	0.33	15	20	1402	2259
	Telecom Silica[7]	50	0.20	2	2.5	4533	8588
	Telecom Silica[8]	100	0.27	4.5	7	2873	5767

NOTES:
(1) Lengths can be determined on the basis of power launched, losses, and receiver sensitivity for bit error rate. (2) Best estimate of NA at this length. Manufacturer's loss data (could be typical) on fiber. (3) Typical fiber loss, worst case = FOT110 min output power, FOR110 worst case sensitivity. (4) Dupont PIFAX PIR-140. (5) Siecor 155 Super Fat. (6) Maxlite MSC200A. (7) Corning 2510F. (8) Corning LCF. (9) Burr-Brown OCA-201-XX terminated cable assembly. (10) Maxlite MSC200B.

The transmitter output power is specified as the power coupled into a 200μm core diameter fiber with an NA of 0.48. Larger NA (up to 0.66) couples more power, and smaller NA less power. Larger core diameter (up to 375μm) couples more power, and smaller core diameter couples less power.

Power coupled into various cables can be calculated as follows:

Power coupled into cable =

$$\left(\frac{\text{Dia}}{200\mu\text{m}}\right)^2 \text{x} \left(\frac{\text{NA}}{0.48}\right)^2 \text{x} \left(\frac{1 - 0.48^2}{1 - \text{NA}^2}\right) \text{x} \text{FOT110 Rated Output Power}$$

where

Dia = cable fiber core Dia (μm) up to 375μm max.

NA = effective cable NA up to 0.66 max (effective NA depends on cable length, decreasing with increased length to a "steady state" value). Coupling into graded index fiber results in additional 3dB loss.

See Typical Performance Curves for Launched Output Power vs Core Diameter and vs Numerical Aperture.

BASIC CIRCUIT CONNECTIONS

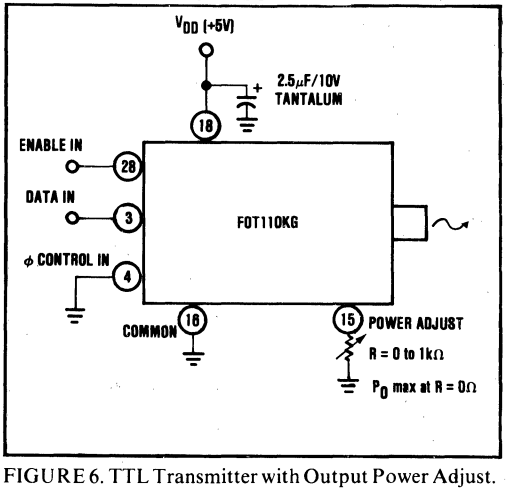


FIGURE 6. TTL Transmitter with Output Power Adjust.

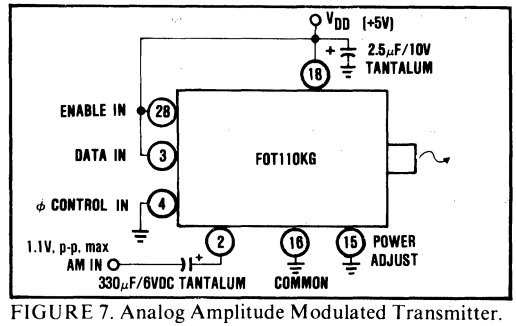


FIGURE 7. Analog Amplitude Modulated Transmitter.

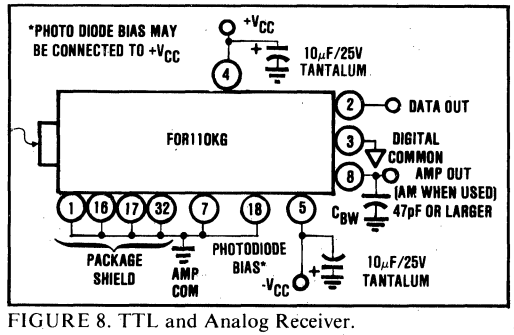


FIGURE 8. TTL and Analog Receiver.

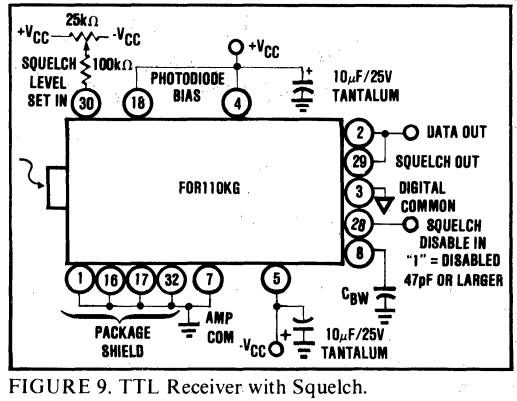


FIGURE 9. TTL Receiver with Squelch.

TYPICAL APPLICATIONS

The FOT/FOR110 Fiber Optic Data Link solves such data transmission problems as crosstalk, ringing, and echos. Electromagnetic radiation interference is avoided when using a fiber optic data link in high noise environments. Lightning damage to cables and connected equipment can be eliminated where fiber optic cables replace metallic conductors. In refineries and chemical plants which have explosive atmospheres, sparks from shorted electrical cables are eliminated by the fiber optic cable - an inherent safety feature. Figures 10 thru 14 illustrate the use of the FOT/FOR transmitter and receiver to replace conventional metal conductor cables.

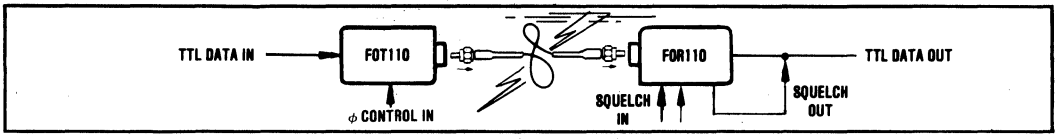


FIGURE 10. TTL Transparent Data Link with Squelch.

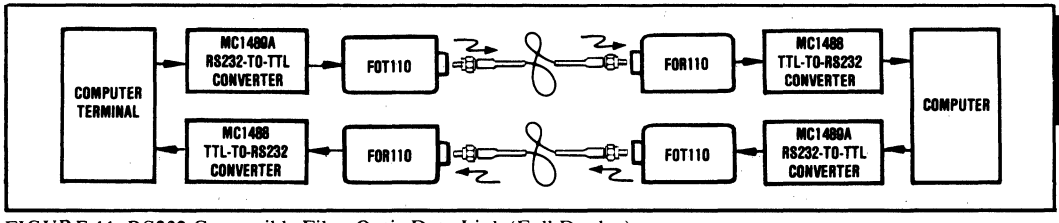


FIGURE 11. RS232 Compatible Fiber Optic Data Link (Full Duplex).

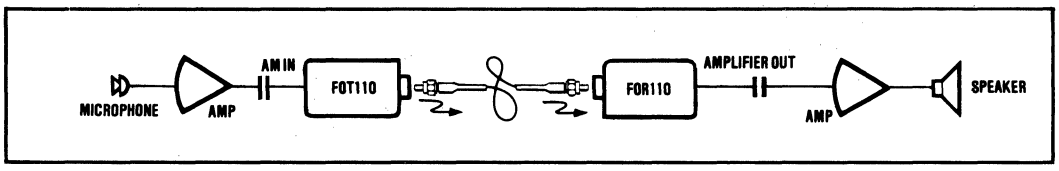


FIGURE 12. Fiber Optic Voice Link (Optical Intercom).

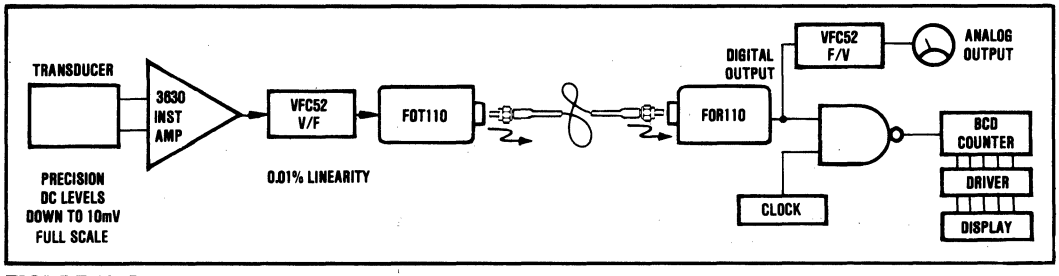


FIGURE 13. Remote Transducer Readout.

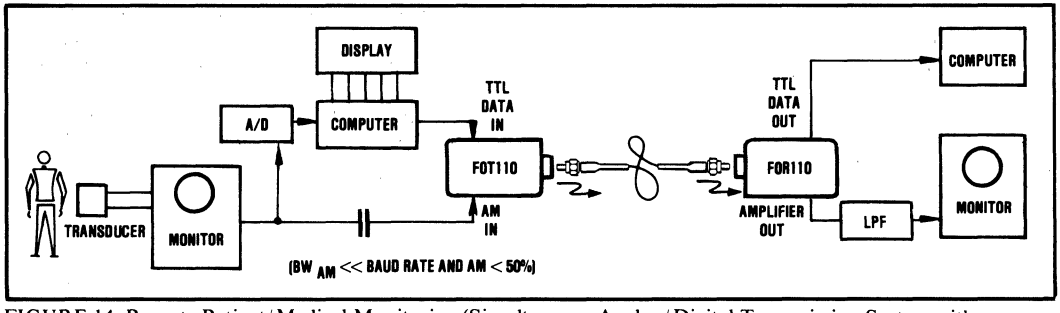
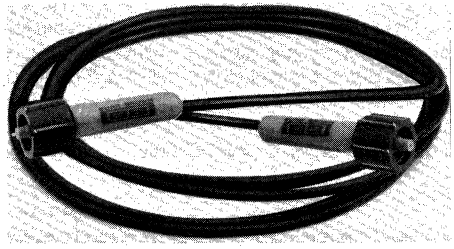


FIGURE 14. Remote Patient/Medical Monitoring (Simultaneous Analog/Digital Transmission System with Megavolts of Isolation).

BURR-BROWN®



OCA100
OCA101
OCA102

Step-Index
FIBER OPTIC CABLE ASSEMBLIES

FEATURES

- FACTORY-INSTALLED CONNECTORS
- USER-SPECIFIED LENGTH - No Minimum Order
- IMMUNITY FROM EMI AND RFI
- NO RADIATED RF
- ELIMINATES GROUND LOOPS AND SHORT CIRCUITS
- ELIMINATES EXPLOSION AND FIRE HAZARD
- GUARANTEED COMPATIBILITY WITH 3712T/R AND 3713T/R

APPLICATIONS

- INDUSTRIAL/PROCESS CONTROL SYSTEMS IMMUNITY TO NOISY ENVIRONMENTS
- REMOTE INSTRUMENTATION SYSTEMS
- POWER PLANT CONTROL
- HIGH VOLTAGE OR ELECTROMAGNETIC FIELD RESEARCH
- FACTORY DATA COLLECTION
- SECURITY SYSTEMS
- INTRINSIC SAFETY
- MACHINE TOOL CONTROL
- SHIPBOARD AND AIRCRAFT CABLES

GENERAL DESCRIPTION

The OCA100 Series Fiber Optic Cable Assemblies are factory terminated cables. They use the AMP™ Optimate Single Position Fiber Optic Cable Connector System and Single, Step-Index Optical Fibers. These cable assemblies are individually tested to insure their compatibility with Burr-Brown's 3712 and 3713 fiber optic transmitters and receivers.

The OCA100 is an inexpensive, high loss cable assembly suitable for general purpose applications. This plastic core, plastic clad fiber optic cable offers the best price versus performance trade-offs for short lengths.

The OCA101 is a single-channel, plastic core, plastic clad fiber optic cable assembly. This cable is reinforced with Kevlar® 49 aramid fiber. The outer protective jacket is of Hytrel® polyester elastomer. The plastic core is well centered within a thin cladding to which a connector is crimped directly. The OCA101 is the most rugged cable of this series of cable assemblies. Its large core diameter and large numerical aperture make possible run lengths of up to 90 meters.

The OCA102 is a plastic clad silica fiber optic cable assembly. Its single fiber is protected by two jackets of Hytrel® polyester elastomer and Kevlar® aramid reinforcing fibers to give this cable outstanding strength and ruggedness. The low attenuation of the OCA102 permits run lengths of over 850 meters (over 1/2 mile) when it is used with the 3713T transmitter and 3712R receiver mixed data link.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

OPTICAL - Typical specifications at +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OCA100	OCA101	OCA102	UNITS
Attenuation	λ = 660nm λ = 670nm	1300 1300	360 500	33 33	dB/km dB/km
Material Numerical Aperture		0.53	0.53	0.40	
Rise Time	10% to 90%	--	5.5	3.8	nsec/km

MECHANICAL - Typical specifications at +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OCA100	OCA101	OCA102	UNITS
Core Material		Plastic	Plastic	Silica	
Core Diameter		1013	368	200	μm
Fiber Diameter		1016	400	600	μm
Reinforcing Fibers	Kevlar® 49	No	Yes	Yes	
Cable Diameter		2.2	1.9	2.4	mm
Cable Weight		4	4	6	kg/km
Minimum Cable Breaking Strength	1 meter test length. Ends wrapped around 1.6cm radius mandrel.	--	25	65	kg
Minimum Bend Radius	Short Term	--	1	1.5	mm
Cable Elongation	Tensile Force = 15kgf	--	1.2	1	%
Flex Resistance	DOD-STD-1678-Method 2010	--	--	10,000	Cycles
Operating Temperature (without Tensile Load)	Minimum Maximum	-20 +70	-20 +70	-20 +70	°C °C
AMP™ Connector		530530-2	530530-9	1-530530-2	

ORDERING INFORMATION

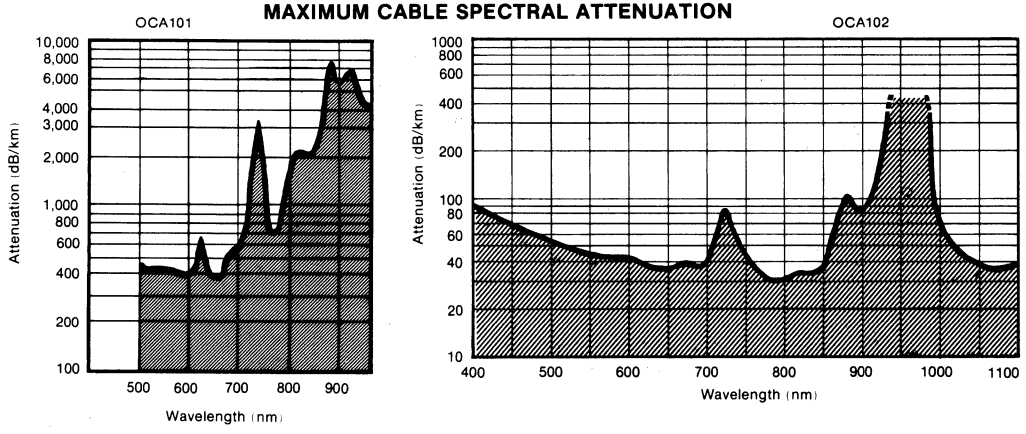
To order, specify cable part number (OCA100, OCA101, or OCA102) and desired length to the nearest tenth of a meter.

SAFETY

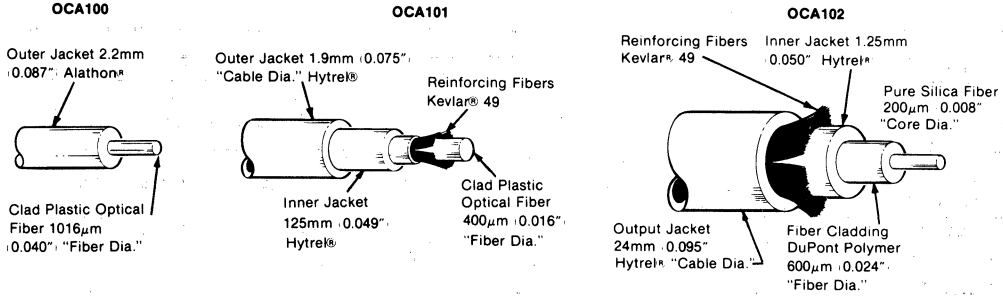
Do not look at the output end of the fiber optic cable because high radiance LEDs or lasers can inject sufficient power into optical fibers to injure the eye.

Reasonable precaution should be observed to avoid undue skin contact when handling the OCA101 and prolonged contact with the cable should be avoided. The jacketing materials of the OCA101 have been specially treated with additives which inhibit the propagation of flame along the cable. Wash hands before smoking or eating. Gloves are recommended for extensive handling.

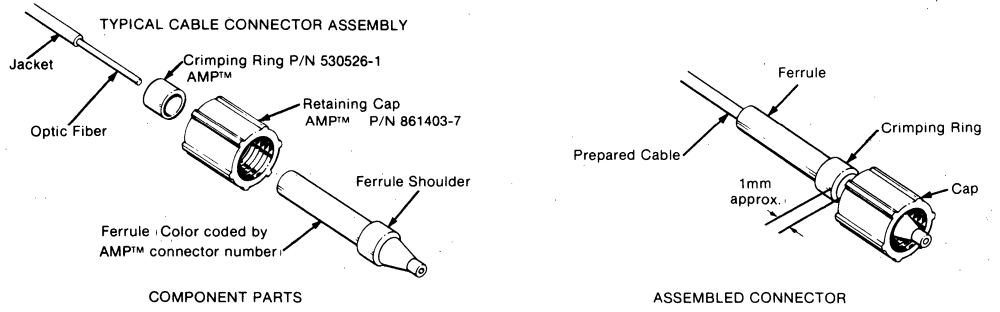
MAXIMUM CABLE SPECTRAL ATTENUATION



CABLE CONSTRUCTION



CABLE CONNECTOR CONSTRUCTION



APPLICATIONS INFORMATION

CABLE TERMINATION

For splicing a damaged cable the following procedure may be used. These procedures will cause an additional loss of about -2dB with the OCA100, -4dB with the OCA101, and -5dB with the OCA102 due to coupling losses at the splice.

1. Clean ferrules ultrasonically in isopropyl alcohol. Allow to dry 24 hours at +25°C or bake at +50°C for 30 minutes.
2. Strip off 2cm of the outside jacket from the cable. This may be done by using an AWG stripper blade #17 for the OCA100, a #22 for the OCA101, or a #16 for the OCA102.
3. For the OCA101 or OCA102, cut back Kevlar® strength fibers to 1cm using sharp scissors.
4. For the OCA102, strip exposed inner jacket to the Kevlar® using a #22 AWG stripper blade.
5. Clean stripped cable end ultrasonically in isopropyl alcohol. At least 10cm of the cable should be cleaned from its end. Wipe dry with a clean wiping tissue and allow to dry for one hour.
6. Apply an epoxy such as TRA-BOND BA-2114 to the inside of the ferrule. Thoroughly coat the small hole in the end of the ferrule. Wipe off any spilled epoxy from the outside of the ferrule.
7. Slip the brass crimping ring and the retaining cap (in that order) over the end of the cable. The open threaded-end of the retaining cap should be facing the end of the cable.
8. On the OCA101 or OCA102. fold back the Kevlar®.
9. Dip the end of the fiber into the epoxy adhesive. Coat between 1cm and 2cm with epoxy.
10. Insert cable into ferrule as far as it will go. Do not smear adhesive on the outside of the ferrule.
11. Slide retaining cap and then crimping ring over the ferrule. Position crimp ring about 1mm behind cap to allow it to rotate freely when installed. Crimp with AMP™ tool number 90364-1.
12. Allow epoxy to cure 18 hours.
13. Cleave and polish fiber as described in the following sections.

FIBER CLEAVING

NOTE: Reasonable precautions should be observed when terminating the OCA102 (silicia core cable). Eye protection is recommended to protect against injury from fragments of silicia core. Avoid skin punctures.

Procedure for cleaving OCA100 or OCA101:

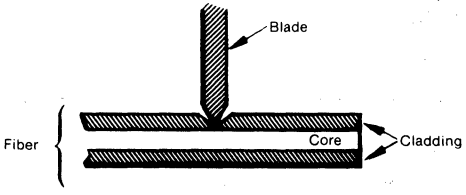
1. Cut the fiber completely through with a sharp razor blade so that it protrudes about 1mm from the end of the ferrule.

Procedure for cleaving OCA102:

1. Using a sharp silicon carbide razor blade cut through the cladding and just barely nick the silica core. Do not saw back and forth or allow the fiber to rotate. Do not cut through the fiber. If the fiber is cut all the way through, a crack could propagate into the core

which could result in reterminating the cable.

2. Bend the fiber at the scribe. A clean cleave should result.
3. Examine the end with a magnifier. If the cleave is smooth, the core should appear darkened when viewed at a 45° angle. If a crack did progagate into the core, the core should appear white - consider recleaving.

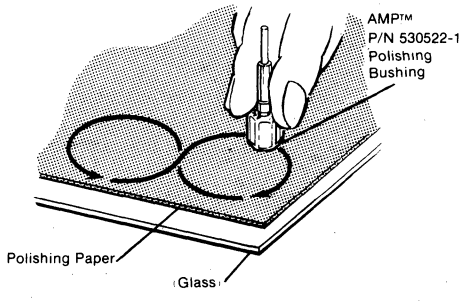


FIBER POLISHING

NOTE: Fine silica powder produced in polishing the OCA102 may be hazardous if inhaled.

Procedure:

1. Screw polishing bushing into retaining cap until ferrule is firmly bottomed.
2. Take connector between thumb and forefinger as if it were a pencil.



3. Use a figure 8 pattern when polishing the end of the fiber. The polishing paper should be thoroughly wet with water before beginning. Clean the end of the polishing bushing in isopropyl alcohol after each polishing step and before going to finer paper.
4. Polish very lightly with 600-A type silicon carbide paper until polishing lines from fiber are no longer visible.
5. Next polish with 3 micron silicon carbide lapping film. Note: Lapping film must be kept free of dust particles. Accumulated dust and dirt on the surface of the film will act as an undesirable abrasive.
6. Polish with 0.3 micron aluminum oxide lapping film.
7. The polishing is complete when the surface of the polishing bushing immediately surrounding the ferrule is polished to a glossy finish.
8. Remove and discard the polishing bushing - do not reuse.
9. Clean connector in isopropyl alcohol.

MINIMIZING SPLICE LOSSES

Losses due to lateral misalignment of the optical fibers inside the splicing bushing can be minimized as follows:

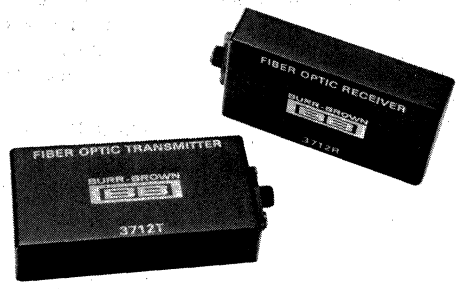
1. Connect the spliced cable to a working fiber optic data link. Loosen the retaining caps of the cable.
2. If a 3712 or 3713 data link is used, monitor the analog output of the fiber optic receiver. Rotate one of the cables inside the splicing bushing to get a maximum signal from the analog output. Tighten the retaining caps of the cable.
3. If a data link other than a 3712 or 3713 is used, monitor the optical power out of the spliced cable using a radiometer. Rotate one of the cables inside the splicing bushing to get a maximum signal at the radiometer. Tighten the retaining cap.

MATERIAL SUPPLIERS

This is a representative list of suppliers for some of the materials mentioned in this product data sheet:

1. Wire Strippers:
   Ideal Industries, Inc.
   Sycamore, IL 60178
2. Silicon Carbide Blades:
   Deane Carbide Co.
   P.O. Box 118
   Trevose, PA 19047
   (215) 673-2121
3. Shears for Cutting Kevlar®:
   Technology Associates, Inc.
   P.O. Box 7163
   Wilmington, DE 19803
   (302) 475-6219
4. Polishing Materials:
   Glennel Corp.
   Rt. 100 S. or Rt. 141
   Chester Springs, PA 19425
   (215) 458-8901
5. Epoxy Adhesive:
   TRA-CON, Inc.
   55 North Street
   Medford, MA 02155
   (617) 391-5550
6. Connectors & Splicing Bushings:
   AMP, Inc.
   449 Eisenhower Blvd.
   Harrisburgh, PA 17105
   (717) 564-0101

BURR-BROWN®



3712T
3712R

High Sensitivity - Low Speed FIBER OPTIC TRANSMITTER AND RECEIVER

FEATURES

- LOW COST
- HIGH SENSITIVITY
- TTL INPUT/OUTPUT
- IMMUNITY TO ELECTROMAGNETIC INTERFERENCE
- NO EXTERNALLY RADIATED SIGNAL
- ELECTRICAL ISOLATION
- DUTY CYCLE INDEPENDENT
- 0°C TO 70°C OPERATION

APPLICATIONS

- INDUSTRIAL/PROCESS CONTROL
- REMOTE INSTRUMENTATION SYSTEMS
- POWER PLANT CONTROL
- HIGH VOLTAGE OR ELECTROMAGNETIC FIELD RESEARCH
- FACTORY DATA COLLECTION
- SECURITY SYSTEMS
- INTRINSIC SAFETY

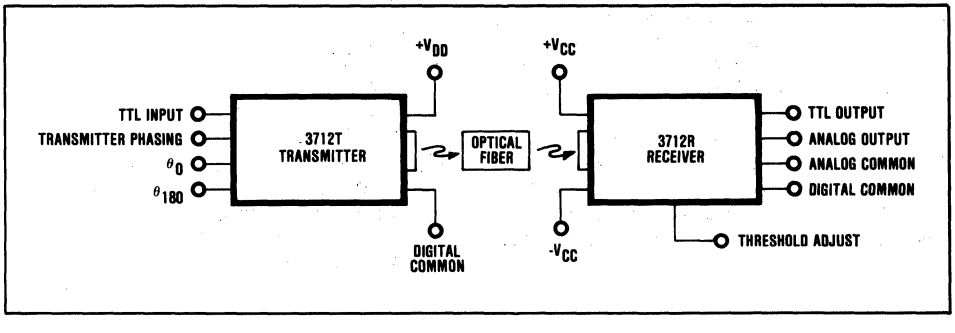
DESCRIPTION

The 3712T and 3712R when connected by a suitable fiber optic cable form a 25k baud NRZ fiber optic data link capable of operation to 1.5km.

The 3712T fiber optic transmitter is an electrical-to-optical transducer designed for digital data transmission over single fiber channels. Transmitter circuitry converts TTL level inputs to optical pulses at data rates from DC to 2M baud NRZ.

The 3712R fiber optic receiver is an optical-to-electrical transducer designed for reception of digital data over single fiber channels. The receiver circuitry converts optical pulses to TTL level outputs with a receiver sensitivity of a mere 2nW and data rates to 25k baud NRZ.

An integral optical connector, on both the 3712T and 3712R, allows easy interfacing between modules and optical fiber without problems of source/fiber/detector alignment. The metal packages of the 3712T and 3712R provide immunity to electromagnetic radiation and direct printed circuit board mounting with no additional heat sink required.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

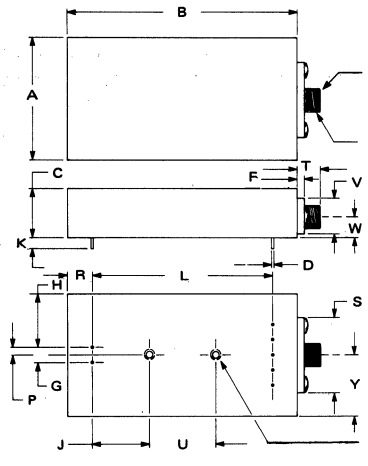
ELECTRICAL

Specifications at T_A = +25°C, $+V_{DD}$ = 5VDC, $\pm V_{CC}$ = 15VDC and no threshold trim unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER, 3712T					
Output Power	Coupled into:				
	1016μm, 0.53NA Fiber	2.5	3.5		μW
	368μm, 0.53NA Fiber	0.33	0.46		μW
	200μm, 0.40NA Fiber	0.10	0.14		μW
Wavelength			670		nm
Rise Time	10% to 90%		120		nsec
Fall Time	90% to 10%		50		nsec
Bit Rate			0 to 2M		Baud
DIGITAL TTL INPUT					
Input "High" Threshold		1.4	1.6	1.9	V
Input "Low" Threshold		0.5	0.8	1.0	V
POWER SUPPLY ($+V_{DD}$)					
Voltage		4.75	5.00	5.25	VDC
Current					
Emitter On		35	46	60	mADC
Emitter Off		4	8	16	mADC
TEMPERATURE RANGE					
Operating		0		70	°C
RECEIVER, 3712R					
ANALOG SECTION					
Responsivity	λ = 940nm	-6.7	-11		mV/nW
	λ = 900nm	-6.9	-11.3		mV/nW
	λ = 670nm	-3.6	-6		mV/nW
Detector Active Area			1.7		mm^2
Noise Equivalent Power	λ = 900nm, F = 1kHz, BW = 1Hz		5.2×10^{-14}	8.2×10^{-14}	$W/\sqrt{Hz}$
Output Noise	10Hz to 10MHz		0.35		mV, rms
Bandwidth	-3dB	DC to 15	DC to 20		kHz
Output Offset	Total Darkness				
25°C			0.2	0.5	mVDC
70°C			0.65	1.3	mVDC
Output Voltage	R_L = 2kΩ	-10	-12		V
DIGITAL SECTION (P_{IN} = 5nW at 670nm)					
Bit Rate(1)	NRZ coding	0 to 20k	0 to 25k		Baud
Duty Cycle(1)		0		100	%
Sensitivity(2)(3)	BER = 10^{-9}, 1kB/Sec,λ = 670nm, 0°C to 70°C	5	2		nW
Propagation Delay	Light In, Digital Out		20	30	μsec
Output Rise Time	Without external pull-up resistor		1		μsec
Output Fall Time	Without external pull-up resistor		0.15		μsec
Fan Out	Without external pull-up resistor	2	4		Unit loads
TTL Out "High"	Without external pull-up resistor	2.4	3.2		V
TTL Out "Low"	Without external pull-up resistor		0.2	0.4	V
Logic Polarity	No Light		Low		
POWER SUPPLY ($\pm V_{CC}$)					
Voltage		±11.5	±15	±18	VDC
Current	±15VDC		+20, -17		mADC
TEMPERATURE					
Operating		0		70	°C

NOTES:
1. See "Applications Information" section regarding operation of Automatic Threshold Circuit.
2. May be improved with external threshold voltage trim.
3. Input should be limited to 0.2μW to avoid duty cycle distortion.

MECHANICAL



Order Number:
3712T
3712R

AMP™ Optimate Single Position Fiber Optic Connector P/N 530570-1

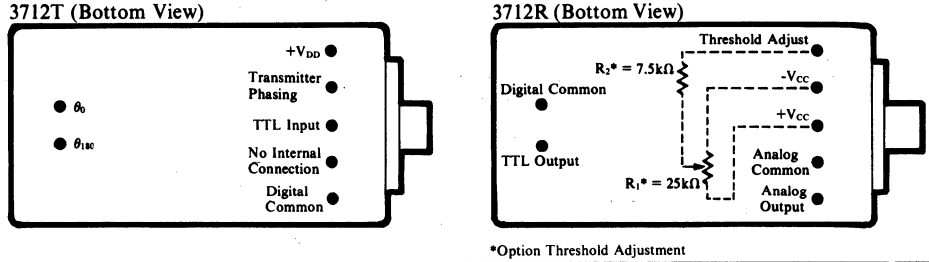
5/16 - 32 NEF - 2A thread.

NOTE:
Leads in true position within .015" (.38mm)R at MMC at seating plane.

4-40 thread, .150" (3.81mm) min. depth, 2 places in true position within .015" (.38mm)R at MMC.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.610	1.650	40.89	41.91
B	3.020	3.060	76.71	77.72
C	.640	.680	16.26	17.27
D	.038	.042	0.97	1.07
F	.075	.095	1.91	2.41
G	.200 BASIC		5.08 BASIC	
H	.670	.770	17.02	19.56
J	.755 BASIC		19.18 BASIC	
K	.250	.350	6.35	8.89
L	2.200 BASIC		55.88 BASIC	
P	.100 BASIC		2.54 BASIC	
R	.275	.375	6.99	9.53
S	.980	1.020	24.89	25.91
T	.275	.315	6.99	8.00
U	.890 BASIC		22.61 BASIC	
V	.460	.500	11.68	12.70
W	.260	.300	6.60	7.62
Y	.795	.835	20.19	21.21

PIN CONFIGURATION



*Option Threshold Adjustment

APPLICATIONS INFORMATION

THEORY OF OPERATION

Transmitter Operation

A simplified block diagram of the 3712T transmitter is shown in Figure 1. The input stage uses a Schmitt Trigger EXCLUSIVE OR Gate G_1 for noise immunity, and its logic is configured so the phasing of the transmitter is pin-programmable. When the transmitter phasing pin is connected to θ_0 the light output is in-phase with the digital input signal - the LED is on when the TTL input is high. Connecting the transmitter phasing pin to θ_{180} causes the reverse to happen - the LED is on for a digital low. Operating the 3712T with the transmitter phasing to θ_{180} makes it possible to detect a break in the fiber optic cable when the data link is idle. This may be particularly useful in the transmission of asynchronous data with an idle state of a TTL low. Programming the phase of the 3712T is discussed more in "Receiver Operation".

Amplifier A_1 and the current switch drive a light emitting diode (LED).

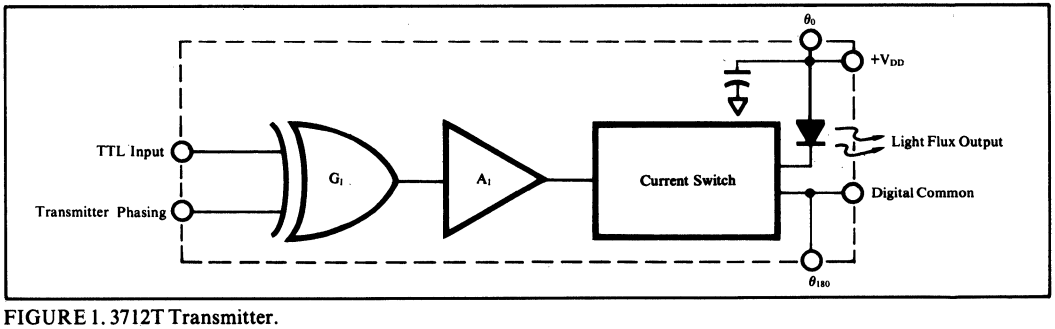


FIGURE 1. 3712T Transmitter.

Receiver Operation

A simplified block diagram of the 3712R receiver is shown in Figure 2. Input light is converted to a current by the PIN photodiode CR1 which is connected in the photovoltaic mode for maximum sensitivity. A low bias current FET input current-to-voltage converter tranforms diode current into a voltage (V_A) which is further amplified by A_2 and presented to comparator A_3 as V_B where it is compared to the threshold voltage V_T.

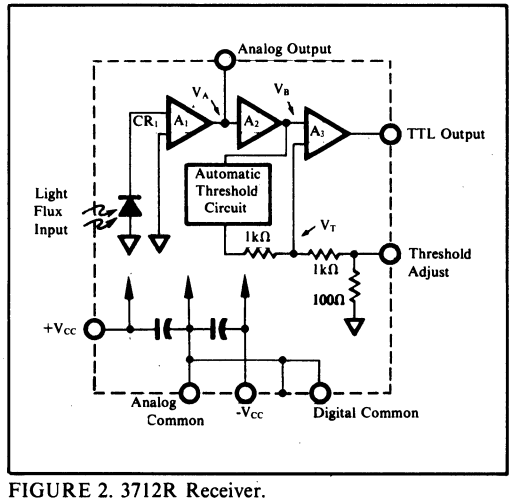


FIGURE 2. 3712R Receiver.

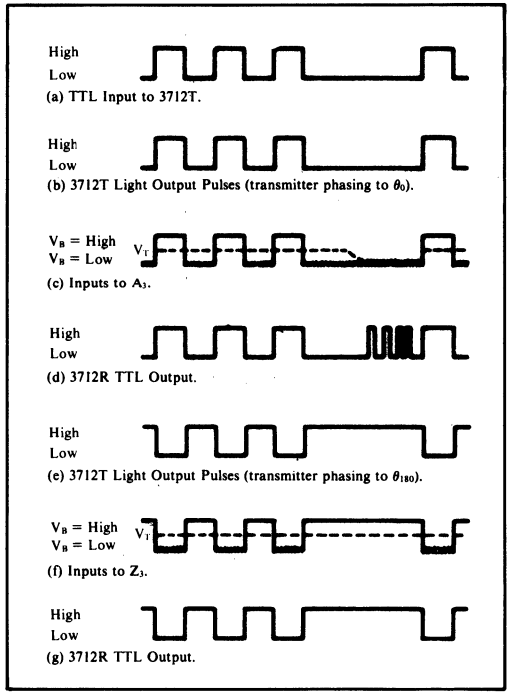


FIGURE 3. Transmitter Phasing for Improved Noise Immunity.

For maximum noise immunity it is desirable to have the threshold voltage set to a value corresponding to a level halfway between the high value and low value of input regardless of the actual light level at the input as shown in Figure 3c. In the 3712R this is accomplished by a peak detector type Automatic Threshold Circuit. A pulse of light input causes a voltage pulse at V_B which is stored in the Automatic Threshold Circuit, divided in half, and supplied to the comparator as the threshold input V_T. Thus, V_T is a voltage corresponding to the midpoint of the Light and No Light conditions of the diode.

Since the Automatic Threshold Circuit uses a capacitive hold technique the threshold voltage V_T is subject to decay, as in Figure 3c, when light is removed from CR_1. A No Light condition of approximately 1/2 second duration (a 1 baud data rate) can be used with no significant effect on noise immunity.

If the light is left off indefinitely, the voltage at V_T will drop to the noise floor and the TTL Output will be subject to normal noise pulse outputs, as illustrated in Figure 3d. The first light pulse received will then activate the Automatic Threshold Circuit. The initial transition at the TTL output may be uncertain for this first pulse, but after the first pulse activates the Automatic Threshold Circuit there will be no uncertainty in the TTL output.

It should be noted that the polarity of the transmitter is pin-programmable. Thus, in an application where there are idle states that exceed 1/2 second (such as ASCII data transmission) the transmitter may be programmed such that the idle state corresponds to a Light On condition (see Figure 3e). This will keep the automatic threshold activated and there will be no first pulse ambiguity as shown in Figures 3f and 3g. Connecting the transmitter phasing to θ_{180} has the disadvantage of keeping the LED on during idle periods. LED optical output is a function of operating time as shown in Figure 4.

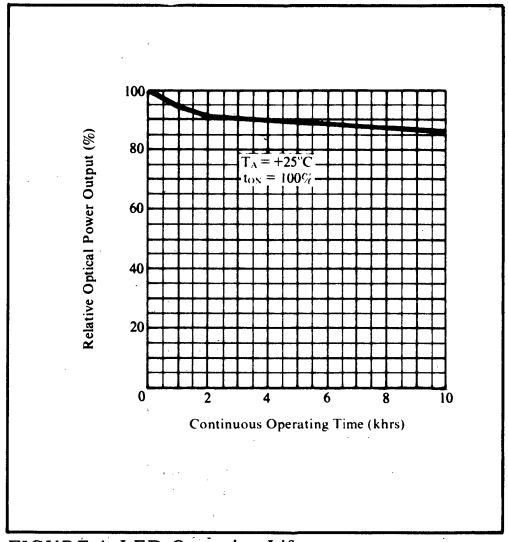


FIGURE 4. LED Operating Life.

Figure 5 shows the spectral response of the receiver.

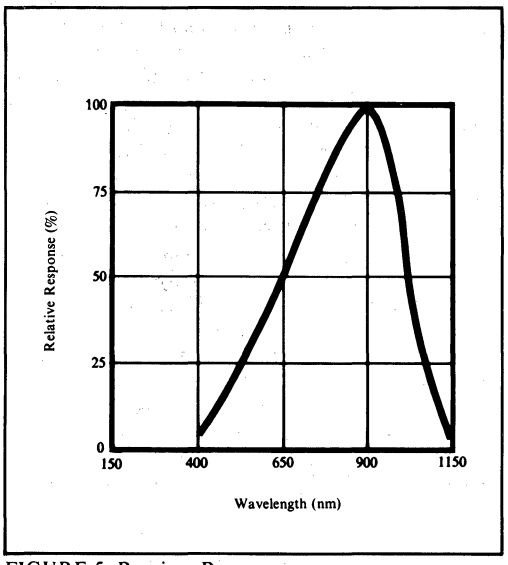


FIGURE 5. Receiver Response.

The Analog Output terminal of the 3712R is the output of the linear amplifier A_1. The voltage at this pin is a function of the input power to the receiver. As such, it makes an excellent diagnostic point for testing the fiber optic cable. Monitoring the Analog Output terminal gives a relative measure of cable loss at the transmitted wavelength and a direct measurement of receiver signal-to-noise ratio when the transmitter is off.

Optional Receiver Threshold Adjustment

The circuit in Figure 6 is used to add a DC bias voltage to the comparator A_3. This bias voltage may be used to:

a) Adjust the receiver for maximum sensitivity, or

b) Eliminate spurious outputs when the transmitter is idle for long periods of time and the threshold voltage decays to the noise floor of the receiver.

Adjustment procedure for maximum receiver sensitivity:

1. Provide a No Light input condition to the receiver. (This may be done with a cable connected to an OFF transmitter or by using an opaque cap and no cable.) The TTL Out may now be changing state due to normal receiver noise.
2. Adjust R_1 for an equal number of high and low states at the TTL Out. This may be done by observing the TTL Out on an oscilloscope or an AC voltmeter. When the voltmeter is used adjust R_1 for a peak reading.

Adjustment procedure to eliminate spurious outputs:

1. Provide a No Light input condition as previously described.
2. Adjust R_1 until the voltage at the TTL Output remains at a low state. (Note: More offset gives better BER, but requires a higher input level to the receiver.)

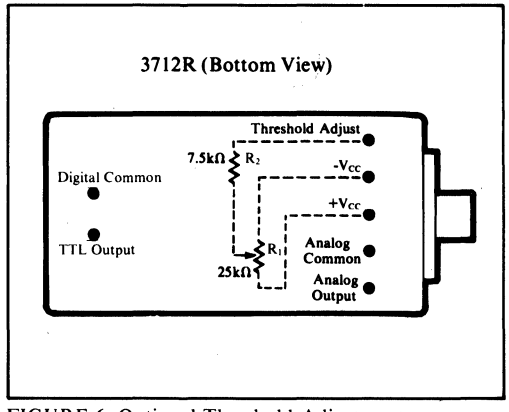


FIGURE 6. Optional Threshold Adjustment.

CABLE SELECTION

The 3712T and 3712R with the AMP Optimate Single Position Fiber Optic Cable Connector System can be used with a wide variety of cable types. The choice of a cable type for a particular application of course depends upon the details of that application such as link environment, link length, cable performance characteristics, and cable cost.

ENVIRONMENTAL CONSIDERATIONS

The mechanical stresses, environmental temperature extremes, and exposure to harsh chemicals must be considered when choosing a particular cable. Such things as jacketing method and the type of added strength members, see Figure 7, determine a cable's mechanical

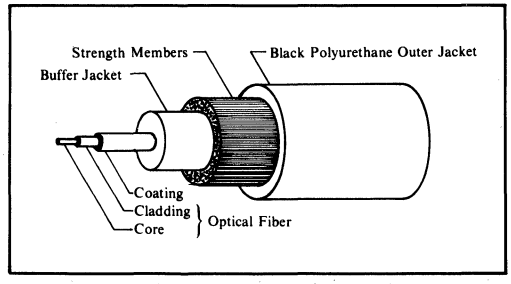


FIGURE 7. Typical Step Index Fiber Optic Cable Construction.

and environmental capabilities. Table I is a list of representative cable manufacturers who make cables compatible with the 3712T/R. See Table II for details of cable performance.

TABLE I. Representative Cable Manufacturers.

AMP (CONNECTORS)
(717)564-0101
AMP, Inc.
449 Eisenhower Blvd.
Harrisburgh, PA 17105

BELDEN
(312)232-8900
Belden Corp.
2000 South Batavia
Geneva, Il 60134

DUPONT (CROFON)
(302)774-6595
E.I. DuPont De Nemours
PP & R Dept., Room D-12086
Crofon Fiber Optics Group
Wilmington, DE 19898

DUPONT (PIFAX)
(302)774-7850
(302)774-6339
E.I. DuPont De Nemours
Plastic Products & Resins
Wilmington, DE 19898

GALILEO
(617)347-9191
Galileo Electro-Optics
Galileo Park
Sturbridge, MA 01518

MAXLIGHT
(602)269-8387
Maxlight
Optical Waveguides, Inc.
3035 N. 33rd Drive
Phoenix, AZ 85017

VALTEC
(617)835-6082
Valtec Corp.
Fiber Optics Div.
West Boylston, MA 01583

DETERMINING CABLE TYPE

There are three types of optical fibers to choose from: Step Index, Single-Mode, and Graded Index. Each type specifies the profile or variation of the fiber's index of refraction as a function of radial distance from the fiber's center. In a fiber with a step-index profile, the refractive index undergoes an abrupt change (step) in value. This step is caused by the sudden change in the index of refraction between the fiber's core and a surrounding annular cladding, as shown in Figure 8.

Step-index fiber with a core diameter of 200μm or larger is recommended for use with the 3712T and 3712R. Step-index fiber offers the best compromise between core diameter, bandwidth, coupling loss, and cost. Single-mode and graded-index fiber is not recommended due to their small core diameter. The wide bandwidth characteristics of these cables are not needed.

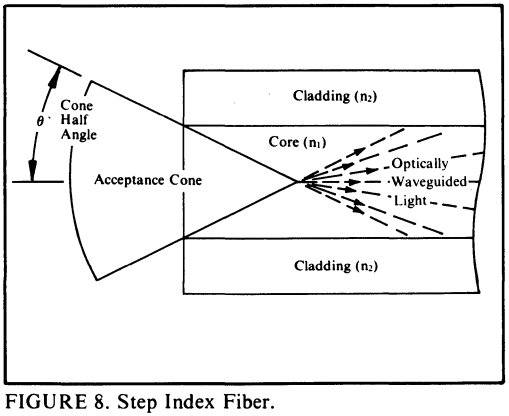


FIGURE 8. Step Index Fiber.

DETERMINING LAUNCHED POWER

Once the mechanical characteristics and cable type have been chosen, it becomes necessary to analyze link performance with various cables. First, analyze the power launched into a particular cable from the transmitter.

An advantage of the 3712T over most other fiber optic transmitters is the way output power has been specified. The 3712T specifies the actual power launched into the cable. Thus such complicated effects as LED output power and emission profile, cable numerical aperture (NA), and spacing between the LED transmitter and the cable have all been taken into consideration for the user. For cable other than those specified in the Electrical Specifications Table, the power launched may be determined by:

$$P_L \text{ (Fiber 2)} = P_L \text{ (Fiber 1)}[(D_2)^2/(D_1)^2],$$

where P_L (Fiber 2) is the power launched into the unspecified cable whose core diameter is D_2 and P_L (Fiber 1) is 2.5μW, minimum, (3.5μW, typical) the core diameter D_1 of Fiber 1 is 1016μm.

NUMERICAL APERTURE

Numerical aperture differences between fibers will somewhat modify the results obtained by the equation just discussed (e.g., higher NA will increase coupling efficiency, thus increasing the power launched into the cable). However, this effect is minimum for the 3712T because of the physical relationship between the LED transmitter and the fiber optic cable.

DETERMINING MAXIMUM CABLE LENGTH

Once P_L and Lλ are known, the maximum cable length may be determined. First the loss margin is found,

$$LM(dB) = 10 \log (P_L/P_{In\ min}).$$

For the 3712T with CROFON 1040 1016μm fiber, P_L = 2.5μW and for the 3712R, $P_{In\ min}$ = 5nW worst case for 10^{-9} BER. Thus,

$$LM = 10 \log (2.5\mu W/5nW) = 10 \log 500 = 27dB.$$

Then X_{max}, the maximum cable length that will just present $P_{In\ min}$ to the transmitter is found

$$X_{max} = [LM(dB)]/[L\lambda(dB/m)].$$

For CROFON 1040 at λT = 670nm, Lλ = 1300dB/km

X_{max} = 27dB/1.3dB(m) = 21 meters.

If this length is too short, a cable with a larger diameter (larger P_L) or less attenuation (smaller Lλ) must be used.

Table II shows the link performance for several different cables.

DETERMINING MINIMUM CABLE LENGTH

Short cable lengths with large core diameter fibers may cause some receiver slew rate limit which will appear as duty cycle distortion. Limiting the power coupled into the receiver from the cable will prevent this from occurring.

The minimum cable length may be determined for a

TABLE II. Link Performance vs Various Cable Types.

Cable Manufacturer and Part Number	Cable Characteristics					Link Performance						Recommended AMP™ Connector
	Core Dia. (μm)	Fiber(1) Dia. (μm)	Cable Dia. (mm)	Lλ (2) at 670nm (dB/km)	Material NA	P_L (μW)		LM (dB)		X_{Max} (meters)		
						min	typ	min	typ	min	typ	
BELDEN												
220001	200	400	3.8	12	0.35	0.10	0.14	12.9	18.3	1073	1526	Contact Belden
221001	300	440	3.8	12	0.35	0.22	0.31	16.4	21.8	1366	1820	Contact Belden
DUPONT												
Crofon 1040	1016	1016	2.2	1300	0.53	2.50	3.50	27.0	32.4	21	25	530530-2
PIFAX-P140	368	400	1.9	500	0.53	0.33	0.46	18.2	23.6	36	47	530530-9
PIFAX-PIR140	368	400	1.9	330	0.53	0.33	0.46	18.2	23.6	55	72	530530-9
PIFAX-S120	200	600	2.4	43	0.4	0.10	0.14	12.9	18.3	299	426	1-530530-2
PIFAX-S120 (type 30)	200	600	2.4	33	0.4	0.10	0.14	12.9	18.3	390	555	1-530530-2
GALILEO												
3000LC-P	204	245	2.2	100	0.48	0.10	0.14	13.0	18.5	130	185	530530-9
MAXLIGHT												
KSC200A	200	300	2.4	8	0.39	0.10	0.14	12.9	18.3	1609	2289	(3)
KSC200B	200	300	2.4	27	0.39	0.10	0.14	12.9	18.3	477	678	(3)
VALTEC												
MD-PC100	250	430	4.1	14	0.30	0.15	0.21	14.8	20.3	1058	1447	530530-9

1) Fiber Diameter = Core Diameter plus Cladding. 2) Conversion Factors: 100μm = 0.003937 in; 1000m = 3281 ft. 3) Sold as terminated cable.

specific cable by calculating the power launched into it as previously done using:

$$P_L \text{ (Fiber 2)} = P_L \text{ (Fiber 1)} [(D_2)^2/(D_1)^2].$$

The typical value of P_L (Fiber 1) should be used since this will give the most power into the receiver and result in the desired minimum cable length.

For example, consider a cable with a 368μm core diameter and a cable loss of 330dB/km. The power launched into the cable by the transmitter is:

$$P_L \text{ (Fiber 2)} = 3.5\mu W [(368\mu m)^2/(1016\mu m)^2]$$

$$P_L \text{ (Fiber 2)} = 0.46\mu W.$$

The minimum loss margin is found using the typical power launched into the cable and the maximum input to the receiver which is 0.2μW for the 3712R.

$$LM = 10 \log [(P_L \text{ (Fiber 2)}/P_{In\ max})]$$

$$LM = 10 \log [(0.46\mu W/0.2\mu W)] = 3.6dB.$$

The minimum cable length for the specific cable in this example is: $X_{min} = LM_{min}/L\lambda$

$$X_{min} = 3.6dB/0.33dB/m = 11 \text{ meters.}$$

If this minimum cable length is not short enough for a particular application, use a smaller core diameter cable or a cable with higher loss.

DEFINITION OF TERMS

ACCEPTANCE ANGLE

The critical angle, measured from the core centerline, above which light will not enter the fiber. It is equal to the half-angle of the acceptance cone.

BAUD

The number of signaling elements or data bits per second.

BIT ERROR RATE

The ratio of incorrect bits to total bits in a received data stream.

CLADDING

A sheathing or cover of a lower refractive index material in intimate contact with the core of a higher refractive index material. It serves to provide optical insulation and protection to the total reflection surface.

CORE

The high refractive index central material of an optical fiber through which a light is propagated.

FIBER

The material path along which light propagates; a single discrete optical transmission element consisting of the core and its cladding.

Lλ

Attenuation of a fiber at a specific wavelength.

LM

Loss margin. This is the difference in transmitted power and received power in decibels.

NUMERICAL APERTURE (NA)

See text.

NRZ

Nonreturn-to-zero is the term for a transmission code in which the signal does not periodically return to zero.

P_L

Actual power launched into a specific cable.

RZ

Return-to-zero. Transmission code for a signal which periodically returns to zero.

RESPONSIVITY

The spectral response of the receiver at the output of the radiant flux-to-voltage converter. Given in millivolts per nanowatts.

TYPICAL APPLICATIONS

The 3712T/R Fiber Optic Data Link solves such data transmission problems as crosstalk, ringing, and echos. Electromagnetic radiation interference is avoided when using a fiber optic data link in high noise environments. Lightning damage to cables and connected equipment can be eliminated where fiber optic cables replace metallic conductors. In refineries and chemical plants which have explosive atmospheres, sparks from shorted electrical cables are eliminated by the fiber optic cable - an inherent safety feature. Figures 9 thru 11 illustrate the use of the 3712 transmitter and receiver to replace conventional metal conductor cables.

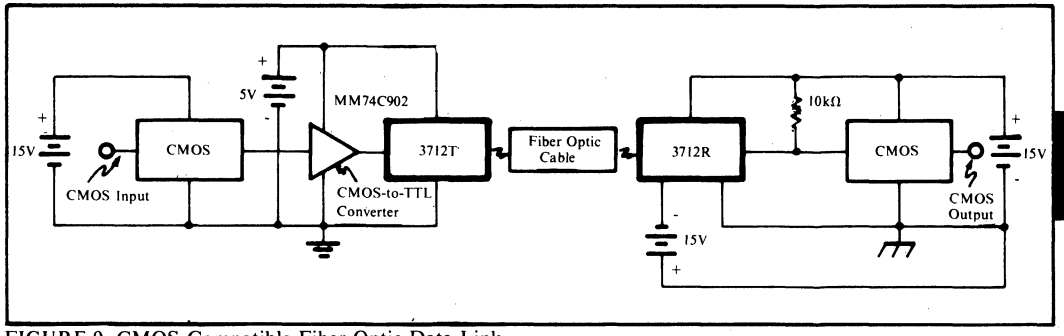


FIGURE 9. CMOS Compatible Fiber Optic Data Link.

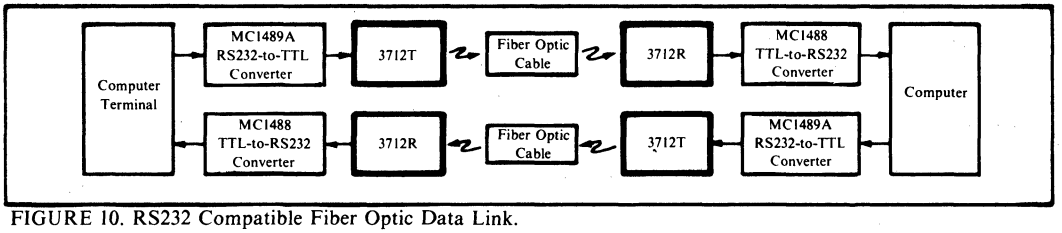


FIGURE 10. RS232 Compatible Fiber Optic Data Link.

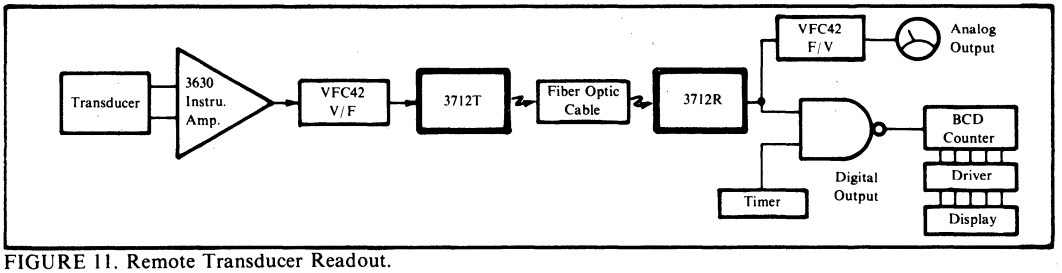
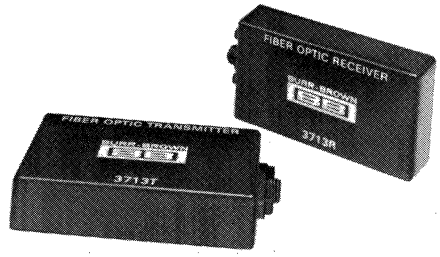


FIGURE 11. Remote Transducer Readout.

BURR-BROWN®



3713T
3713R

High Sensitivity - Medium Speed FIBER OPTIC TRANSMITTER AND RECEIVER

FEATURES

- LOW COST
- HIGH SENSITIVITY
- TTL INPUT/OUTPUT
- IMMUNITY TO ELECTROMAGNETIC INTERFERENCE
- NO EXTERNALLY RADIATED SIGNAL
- ELECTRICAL ISOLATION
- DUTY CYCLE INDEPENDENT
- 0°C TO 70°C OPERATION

APPLICATIONS

- INDUSTRIAL/PROCESS CONTROL
- REMOTE INSTRUMENTATION SYSTEMS
- POWER PLANT CONTROL
- HIGH VOLTAGE OR ELECTROMAGNETIC FIELD RESEARCH
- FACTORY DATA COLLECTION
- SECURITY SYSTEMS
- INTRINSIC SAFETY

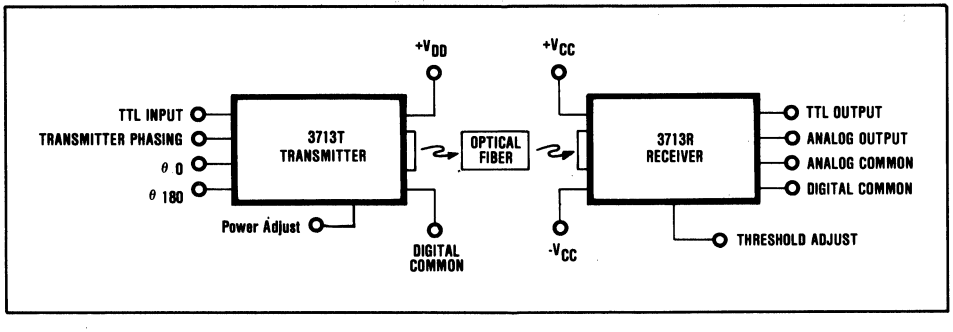
DESCRIPTION

The 3713T and 3713R when connected by a suitable fiber optic cable form a 250k baud NRZ fiber optic data link capable of operation to 1.7km.

The 3713T fiber optic transmitter is an electrical to optical tranducer designed for digital data transmission over single fiber channels. Transmitter circuitry converts TTL level inputs to optical pulses at data rates from DC to 2M baud NRZ.

The 3713R fiber optic receiver is an optical to electrical transducer designed for reception of digital data over single fiber channels. The receiver circuitry converts optical pulses to TTL level outputs with a receiver sensitivity of 15nW and data rates to 250k baud NRZ.

An integral optical connector on both the 3713T and 3713R allows easy interfacing between modules and optical fiber without problems of source/fiber/detector alignment. The metal packages of the 3713T and 3713R provide immunity to electromagnetic radiation and direct printed circuit board mounting with no additional heat sink required.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

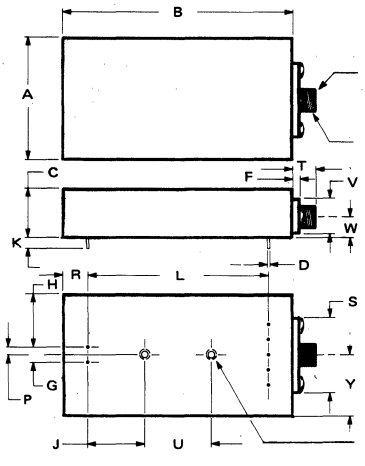
ELECTRICAL

Specifications at T_A = +25°C, $+V_{DD}$ = 5VDC, $\pm V_{CC}$ = 15VDC and no threshold trim unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER, 3713T					
OPTICAL OUTPUT					
Output Power, with maximum output power(1)	Coupled into:				
	1016μm, 0.53NA Fiber	10	15		μW
	368μm, 0.53NA Fiber	1.5	3.5		μW
	200μm, 0.4NA Fiber	0.7	1.5		μW
Output Power Adjustment Range(1)			20		dB
Wavelength			660		nm
Rise Time	10% to 90%		40		nsec
Fall Time	90% to 10%		75		nsec
Bit Rate			0 to 2M		Baud
DIGITAL TTL INPUT					
Input "High" Threshold		1.4	1.6	1.9	V
Input "Low" Threshold		0.5	0.8	1.0	V
POWER SUPPLY					
Voltage		4.75	5.00	5.25	VDC
Current					
Emitter On, with maximum output power			46	60	mADC
Emitter On, with minimum output power			16		mADC
Emitter Off		4	8	16	mADC
TEMPERATURE RANGE					
Operating		0		70	°C
RECEIVER, 3713R					
ANALOG SECTION					
Responsivity	λ = 940nm	-1.6	-2.6		mV/nW
	λ = 900nm	-1.6	-2.7		mV/nW
	λ = 660nm	-0.8	-1.4		mV/nW
Detector Active Area			1.7		mm^2
Noise Equivalent Power	λ = 900nm, F = 10kHz, BW = 1Hz		1.2×10^{-13}	1.7×10^{-13}	$W/\sqrt{Hz}$
Output Noise	10Hz to 10MHz		1.3		mV, rms
Bandwidth	-3dB	DC to 100	DC to 125		kHz
Output Offset	Total Darkness				
25°C			0.7	2.2	mVDC
70°C			1.6		mVDC
Output Voltage	R_L = 2kΩ	-10	-12		V
DIGITAL SECTION (P_{IN} = 50nW at 660nm)					
Bit Rate(2)	NRZ coding	0 to 200k	0 to 250k		Baud
Duty Cycle(2)		0		100	%
Sensitivity(3)(4)	BER = 10^{-9}, 100kB/Sec, λ = 660nm, 25°C	30	15		nW
	BER = 10^{-9}, 100kB/Sec, λ = 660nm, 0°C to 70°C	40	20		nW
Propagation Delay	Light In, Digital Out		8	10	μsec
Output Rise Time	Without external pull-up resistor		1		μsec
Output Fall Time	Without external pull-up resistor		0.15		μsec
Fan Out	Without external pull-up resistor	2	4		Unit Loads
TTL Out "High"	Without external pull-up resistor	2.4	3.2		V
TTL Out "Low"	Without external pull-up resistor		0.2	0.4	V
Logic Polarity	No Light		Low		
POWER SUPPLY					
Voltage		±11.5	±15	±18	VDC
Current	±15VDC		+25, -22		mADC
TEMPERATURE					
Operating		0		70	°C

NOTES:
1. Optical output power is adjustable. See "Applications Information" section. Optical output power is measured into an exit NA of 0.24.
2. See "Applications Information" section regarding operation of Automatic Threshold Circuit.
3. May be improved with external threshold voltage trim. See "Applications Information" section.
4. Input should be limited to 1μW to avoid duty cycle distortion.

MECHANICAL



Order Number:
3713T
3713R

AMP™ Optimate Single Position Fiber Optic Connector P/N 530570-1

5/16 - 32 NEF - 2A thread.

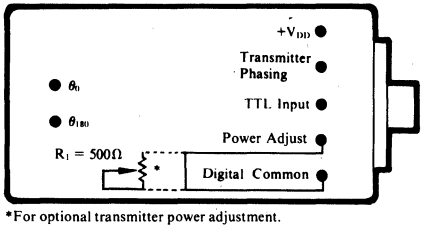
NOTE:
Leads in true position within .015" (.38mm)R at MMC at seating plane.

4-40 thread, .150" (3.81mm) min. depth, 2 places in true position within .015" (.38mm)R at MMC.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.610	1.650	40.89	41.91
B	3.020	3.060	76.71	77.72
C	.640	.680	16.26	17.27
D	.038	.042	0.97	1.07
F	.075	.095	1.91	2.41
G	.200 BASIC		5.08 BASIC	
H	.670	.770	17.02	19.56
J	.755 BASIC		19.18 BASIC	
K	.250	.350	6.35	8.89
L	2.200 BASIC		55.88 BASIC	
P	.100 BASIC		2.54 BASIC	
R	.275	.375	6.99	9.53
S	.980	1.020	24.89	25.91
T	.275	.315	6.99	8.00
U	.890 BASIC		22.61 BASIC	
V	.460	.500	11.68	12.70
W	.260	.300	6.60	7.62
Y	.795	.835	20.19	21.21

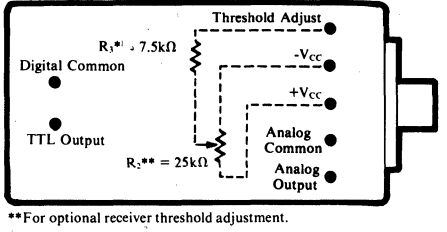
PIN CONFIGURATION

3713T (Bottom View)



*For optional transmitter power adjustment.

3713R (Bottom View)



**For optional receiver threshold adjustment.

APPLICATIONS INFORMATION

THEORY OF OPERATION

Transmitter Operation

A simplified block diagram of the 3713T transmitter is shown in Figure 1. The input stage uses a Schmitt Trigger EXCLUSIVE OR Gate G_1 for noise immunity, and its logic is configured so the phasing of the transmitter is pin-programmable. When the transmitter phasing terminal is connected to θ_0 the light output is in-phase with the digital input signal - the LED is on when the TTL Input is high. Connecting the transmitter phasing terminal to θ_{180} causes the reverse to happen - the LED is on for a digital low. Operating the 3713T with the transmitter phasing to θ_{180} makes it possible to detect a break in the fiber optic cable when the data link is idle. This may be particularly useful in the transmission of asynchronous data with an idle state of a TTL low. Programming the phase of the 3713T is discussed more in the "Receiver Operation" section.

Amplifier A_1 and the current switch drive a light emitting diode (LED).

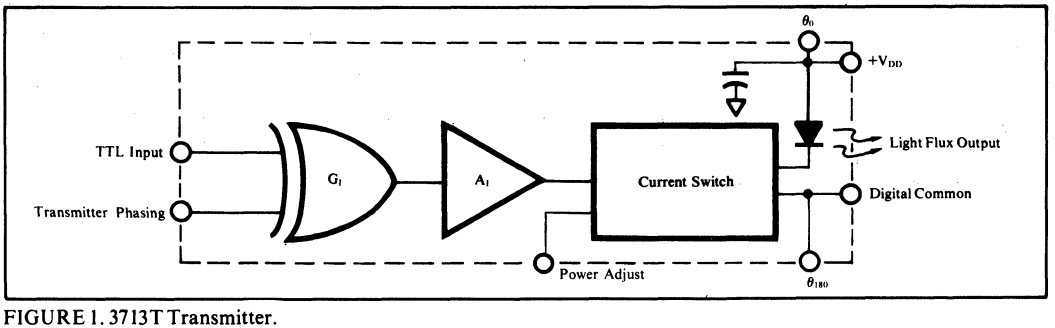


FIGURE 1. 3713T Transmitter.

Optional Transmitter Power Adjustment

The optical power output of the 3713T transmitter may be adjusted by controlling the resistance between the Power Adjust pin and Ground (see Figure 2). This controls the peak or "on" current in the LED as described by the equation $I_{LED} \approx 0.65 \div [1k\Omega \parallel (22\Omega + R_1)]$. Excessive lead length should be avoided when using the external resistor, R_1.

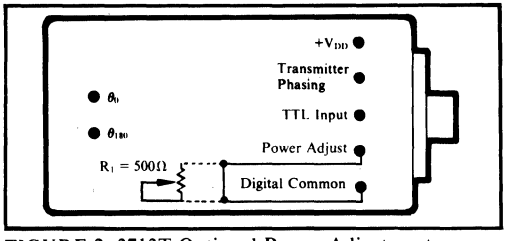


FIGURE 2. 3713T Optional Power Adjustment.

When the resistor is minimum the LED output is maximum and as the resistance is increased the LED output asymptotically approaches a minimum value. The relationships are shown in Table I.

TABLE I. Transmitter Performance vs Optical Power Adjustment.

R_1 (Ω)	I_{LED} (mA)	% max Power	Reduction (dB)
0	30	100	0
10	20	67	-1.7
25	15	50	-3
50	10	33	-5
100	6	20	-7
500	1.9	6	-12
1000	1.3	4	-14
∞	0.65	2	-17

Normally a link would be operated with $R_1 = 0$. For short lengths where the cable loss is low, the LED current may be reduced to extend the LED's life.

Receiver Operation

A simplified block diagram of the 3713R receiver is shown in Figure 3. Input light is converted to a current by the PIN photodiode CR1 which is connected in the photovoltaic mode for maximum sensitivity. A low bias current FET input current-to-voltage converter transforms the diode current into a voltage (V_A) which is further amplified by A_2 and presented to comparator A_3 as V_B where it is compared to the threshold voltage V_T. For maximum noise immunity it is desirable to have the threshold voltage set to a value corresponding to a level halfway between the high value and low value of input regardless of the actual light level at the input as shown in Figure 4c. In the 3713R this is accomplished by a peak detector type Automatic Threshold Circuit. A pulse of light input causes a voltage pulse at V_B which is stored in the Automatic Threshold Circuit, divided in half, and supplied to the comparator as the threshold input V_T. Thus, V_T is a voltage corresponding to the midpoint of the Light and No Light conditions of the diode.

Since the Automatic Threshold Circuit uses a capacitive

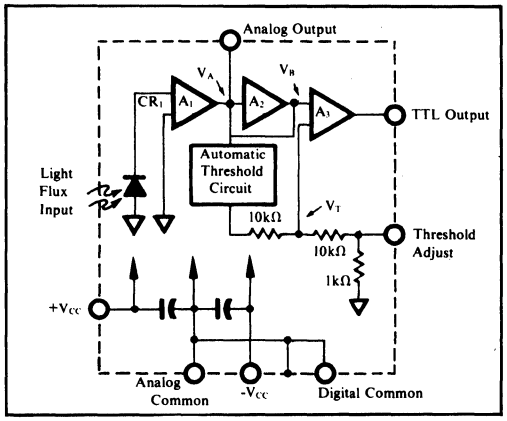


FIGURE 3. 3713R Receiver.

hold technique the threshold voltage V_T is subject to decay, as in Figure 4c, when light is removed from CR1. A No Light condition of approximately 1/2 second duration (a 1 baud data rate) can be used with no significant effect on noise immunity.

If the light is left off indefinitely, the voltage at V_T will drop to the noise floor and the TTL Output will be subject to normal noise pulse outputs, as illustrated in Figure 4d. The first light pulse received will then activate the Automatic Threshold Circuit. The initial transition at the TTL output may be uncertain for this first pulse, but after the first pulse activates the Automatic Threshold Circuit there will be no uncertainty in the TTL output.

It should be noted that the polarity of the transmitter is pin-programmable. Thus, in an application where there are idle states that exceed 1/2 second (such as ASCII data transmission) the transmitter may be programmed such that the idle state corresponds to a Light On condition, see Figure 4e. This will keep the automatic threshold activated and there will be no first pulse ambiguity, as shown in Figures 4f and 4g. Connecting the transmitter phasing to θ_{180} has the disadvantage of keeping the LED on during idle periods. LED optical output is a function of operating time as shown in Figure 5.

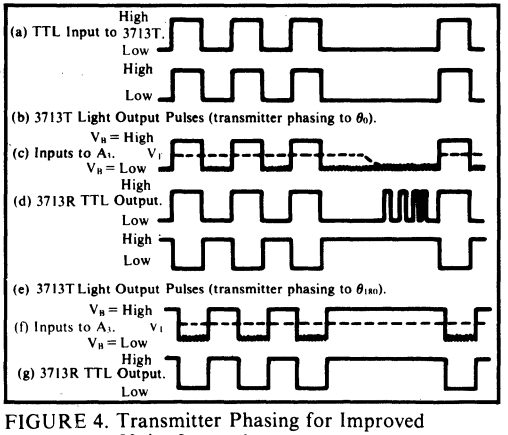


FIGURE 4. Transmitter Phasing for Improved Noise Immunity.

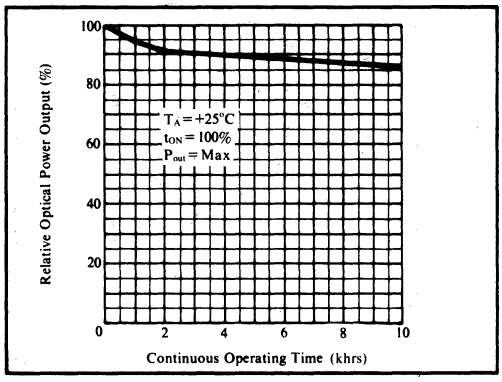


FIGURE 5. LED Operating Life.

Figure 6 shows the spectral response of the receiver.

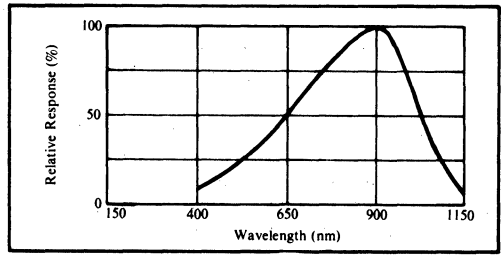


FIGURE 6. Receiver Response.

The Analog Output terminal of the 3713R is the output of the linear amplifier A_1. The voltage at this terminal is a function of the input power to the receiver. As such, it makes an excellent diagnostic point for testing the fiber optic cable. Monitoring the Analog Output terminal gives a relative measure of cable loss at the transmitted wavelength and a direct measurement of receiver signal-to-noise ratios when the transmitter is off.

Optional Receiver Threshold Adjustment

The circuit in Figure 7 is used to add a DC bias voltage to the comparator A_3. This bias voltage may be used to:

a) Adjust the receiver for maximum sensitivity, or
b) Eliminate spurious outputs when the transmitter is idle for long periods of time and the threshold voltage decays to the noise floor of the receiver.

Adjustment procedure for maximum receiver sensitivity:

1. Provide a No Light input condition to the receiver. (This may be done with a cable connected to an OFF transmitter or by using an opaque cap and no cable.) The TTL Out may now be changing state due to normal receiver noise.
2. Adjust R_1 for an equal number of high and low states at the TTL Out. This may be done by observing the TTL Out on an oscilloscope or an AC voltmeter. When the voltmeter is used adjust R_1 for a peak reading.

Adjustment procedure to eliminate spurious outputs:

1. Provide a No Light input condition as previously described.
2. Adjust R_1 until the voltage at the TTL Output remains at a low state. Note: More offset gives better BER, but requires a higher input level to the receiver.

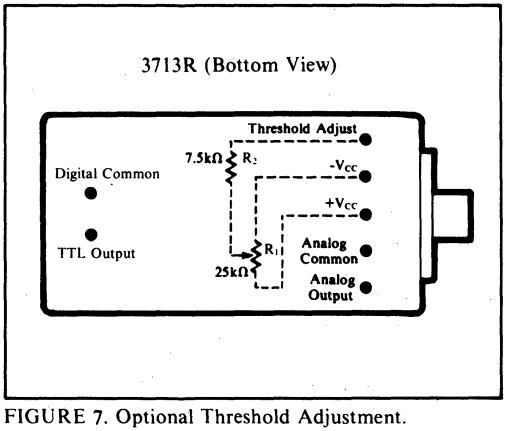


FIGURE 7. Optional Threshold Adjustment.

CABLE SELECTION

The 3713T and 3713R with the AMP Optimate Single Position Fiber Optic Cable Connector System can be used with a wide variety of cable types. The choice of a cable type for a particular application, of course, depends upon the details of that application; link environment, link length, cable performance characteristics, and cable cost.

ENVIRONMENTAL CONSIDERATIONS

The mechanical stresses, environmental temperature extremes, and exposure to harsh chemicals must be considered when choosing a particular cable. Such things as jacketing material and the type of added strength members, see Figure 8, determine a cable's mechanical and environmental capabilities. Table II is a list of representative cable manufacturers who make cable compatible with the 3713T/R. See Table III for details of cable performance.

TABLE II. Representative Cable Manufacturers.

AMP (CONNECTORS)
(717)564-0101
AMP, Inc.
449 Eisenhower Blvd.
Harrisburgh, PA 17105

BELDEN
(312)232-8900
Belden Corp.
2000 South Batavia
Geneva, Il 60134

DUPONT (CROFON)
(302)774-6595
E.I. DuPont De Nemours
PP & R Dept., Room D-12086
Crofon Fiber Optics Group
Wilmington, DE 19898

DUPONT (PIFAX)
(302)774-7850
(302)774-6339
E.I. DuPont De Nemours
Plastic Products & Resins
Wilmington, DE 19898

GALILEO
(617)347-9191
Galileo Electro-Optics
Galileo Park
Sturbridge, MA 01518

MAXLIGHT
(602)269-8387
Maxlight
Optical Waveguides, Inc.
3035 N. 33rd Drive
Phoenix, AZ 85017

VALTEC
(617)835-6082
Valtec Corp.
Fiber Optics Div.
West Boylston, MA 01583

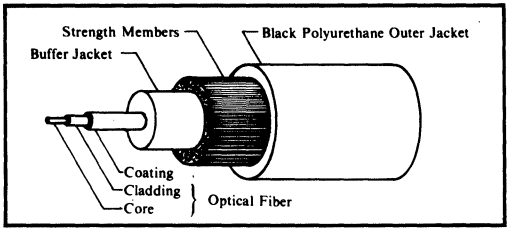


FIGURE 8. Typical Step Index Fiber Optic Cable Construction.

DETERMINING CABLE TYPE

There are three basic types of optical fibers to choose from: Step-Index, Single-Mode, and Graded-Index. Each type specifies the profile or variation of the fiber's index of refraction as a function of radial distance from the fiber's center. In a fiber with a step-index profile, the refractive index undergoes an abrupt change (step) in value. This step is caused by the sudden change in the index of refraction between the fiber's core and a surrounding annular cladding, as shown in Figure 9.

Step-index fiber with a core diameter of 200μm or larger is recommended for use with the 3713T and 3713R. Step-index fiber offers the best compromise between core diameter, bandwidth, coupling loss, and cost. Single-mode and graded-index fibers are not recommended due to their small core diameter. The wide bandwidth characteristics of these cables are not needed.

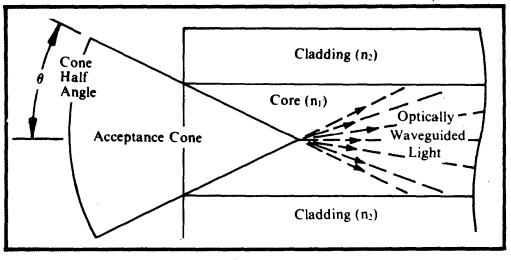


FIGURE 9. Step Index Fiber.

DETERMINING LAUNCHED POWER

Once the mechanical characteristics and cable type have been chosen, it becomes necessary to analyze link performance with various cables. The first analysis to make is the power launched into a particular cable from the transmitter.

An advantage of the 3713T over many other fiber optic transmitters is the way output power has been specified. The 3713T specifies the actual power launched into the cable. Thus, such complicated effects as LED output power and emission profile, cable numerical aperture (NA), and spacing between the LED transmitter and the cable have all been taken into consideration for the user. For cables other than those specified in the Electrical Specification Table, the power launched may be determined from the curve in Figure 10.

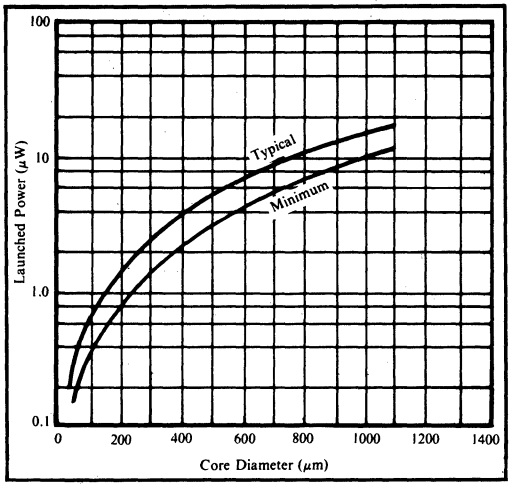


FIGURE 10. Launched Power vs Core Diameter.

DETERMINING MAXIMUM CABLE LENGTH

Once P_L and Lλ are known, the maximum cable length may be obtained. First the loss margin is found by,

$$LM(dB) = 10 \log (P_L / P_{In\ min}).$$

For the 3713T with CROFON 1040 1016μm fiber, P_L = 10μW and for the 3713R, $P_{In\ min}$ = 30nW worst case for 10^{-9} BER. Thus,

$$LM = 10 \log (10\mu W / 30nW) = 10 \log 333 = 25dB.$$

Then X_{Max}, the maximum cable length that will just present $P_{In\ min}$ to the transmitter is found by,

$$X_{Max} = [LM(dB)]/[L\lambda(dB/m)].$$

For CROFON 1040 at λT = 670nm, Lλ = 1300dB/km

$$X_{Max} = 25dB/1.3dB(m) = 19 \text{ meters}.$$

If this length is too short, a cable with a larger diameter (larger P_L) or less attenuation (smaller Lλ) must be used.

Table III shows the link performance for several different cables.

DETERMINING MINIMUM CABLE LENGTH

Short cable lengths with large core diameter fibers may

cause some receiver slew rate limit which will appear as duty cycle distortion. Limiting the power coupled into the receiver from the cable will prevent this from occurring.

The minimum cable length may be determined for a specific cable by calculating the power launched into it as previously done using the typical curve from Figure 10. The typical value of launched power should be used since this will give the most power into the receiver, resulting in the desired minimum cable length.

As an example, consider a cable with a 368μm core diameter and a cable loss of 330dB/km. The typical power launched into the cable from Figure 10 is 3.5μW.

The minimum loss margin is found using the typical power launched into the cable and the maximum input to the receiver which is 1μW for the 3713R.

$$LM = 10 \log (P_L / P_{In\ max})$$

$$LM = 10 \log (3.5\mu W / 1\mu W) = 5.4dB.$$

The minimum cable length for the specific cable in this example is:

$$X_{Min} = LM_{Min} / L\lambda$$

$$X_{Min} (5.4dB / 0.33dB/m) = 16 \text{ meters.}$$

If this minimum cable length is too long for a particular application, use a smaller core diameter cable, a cable with higher loss, or the power launched into the cable may be reduced as described in the "Optional Transmitter Power Adjustment" section.

TABLE III. Link Performance vs Various Cable Types.

Cable Manufacturer and Part Number	Cable Characteristics					Link Performance						Recommended AMP™ Connector
	Core Dia. (μm)	Fiber(1) Dia. (μm)	Cable Dia. (mm)	Lλ (2) at 660nm (dB/km)	Material NA	P_L (μW)		LM (dB)		X_{Max} (meters)		
						min	typ	min	typ	min	typ	
BELDEN												
220001	200	400	3.8	12	0.35	0.7	1.5	14	20	1140	1667	Contact Belden
221001	300	440	3.8	12	0.35	1.1	2.6	16	22	1304	1866	Contact Belden
DUPONT												
Crofon 1040	1016	1016	2.2	1300	0.53	10	15	25	30	19	23	530530-2
PIFAX-P140	368	400	1.9	500	0.53	1.5	3.5	17	24	34	47	530530-9
PIFAX-PIR140	368	400	1.9	330	0.53	1.5	3.5	17	24	51	72	530530-9
PIFAX-S120	200	600	2.4	43	0.4	0.7	1.5	14	20	318	465	1-530530-2
PIFAX-S120 (type 30)	200	600	2.4	33	0.4	0.7	1.5	14	20	415	606	1-530530-2
GALILEO												
3000LC-P	204	245	2.2	100	0.48	0.7	1.5	14	20	137	200	530530-9.
MAXLIGHT												
KSC200A	200	300	2.4	8	0.39	0.7	1.5	14	20	1710	2500	(3)
KSC200B	200	300	2.4	27	0.39	0.7	1.5	14	20	507	741	(3)
VALTEC												
MD-PC100	250	430	4.1	14	0.30	0.9	2.0	15	21	1055	1518	530530-9

1) Fiber Diameter = Core Diameter plus Cladding. 2) Conversion Factors: 100μm = 0.003937 in; 1000m = 3281 ft. 3) Sold as terminated cable.

DEFINITION OF TERMS

ACCEPTANCE ANGLE

The critical angle, measured from the core centerline, above which light will not enter the fiber. It is equal to the half-angle of the acceptance cone.

BAUD

The number of signaling elements or data bits per second.

BIT ERROR RATE

The ratio of incorrect bits to total bits in a received data stream.

CLADDING

A sheathing or cover of a lower refractive index material in intimate contact with the core of a higher refractive index material. It serves to provide optical insulation and protection to the total reflection surface.

CORE

The high refractive index central material of an optical fiber through which a light is propagated.

FIBER

The material path along which light propagates; a single discrete optical transmission element consisting of the core and its cladding.

Lλ

Attenuation of a fiber at a specific wavelength.

LM

Loss margin. This is the difference in transmitted power and received power in decibels.

NRZ

Nonreturn-to-zero is the term for a transmission code in which the signal does not periodically return to zero.

P_L

Actual power launched into a specific cable.

RZ

Return-to-zero. Transmission code for a signal which periodically returns to zero.

RESPONSIVITY

The spectral response of the receiver at the output of the radiant flux-to-voltage converter. Given in millivolts per nanowatts.

TYPICAL APPLICATIONS

The 3713T/R Fiber Optic Data Link solves such data transmission problems as crosstalk, ringing, and echos. Electromagnetic radiation interference is avoided when using a fiber optic data link in high noise environments. Lightning damage to cables and connected equipment can be eliminated where fiber optic cables replace metallic conductors. In refineries and chemical plants which have explosive atmospheres, sparks from shorted electrical cables are eliminated by the fiber optic cable - an inherent safety feature. Figures 11 thru 13 illustrate the use of the 3713 transmitter and receiver to replace conventional metal conductor cables.

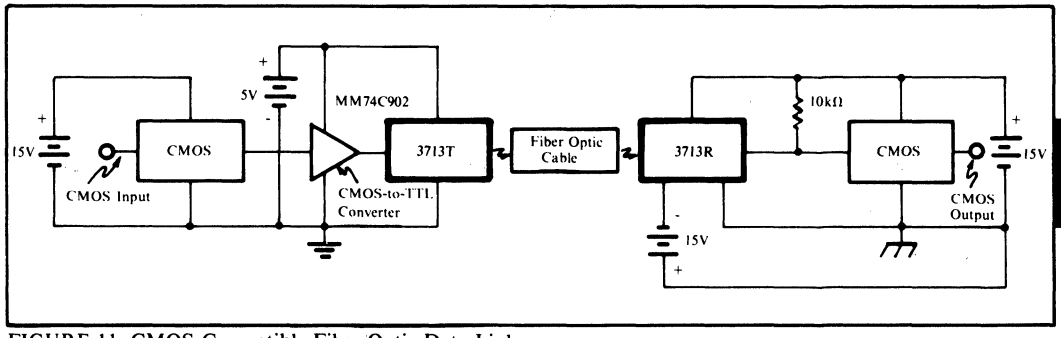


FIGURE 11. CMOS Compatible Fiber Optic Data Link.

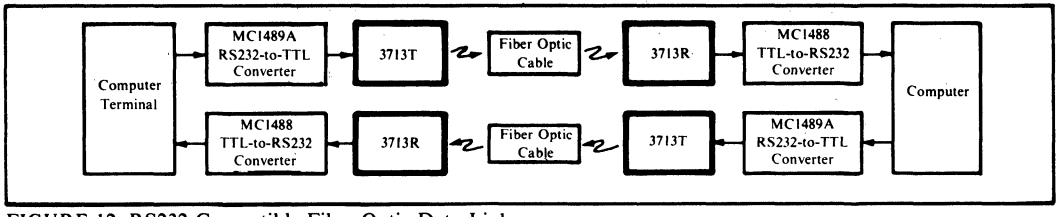


FIGURE 12. RS232 Compatible Fiber Optic Data Link.

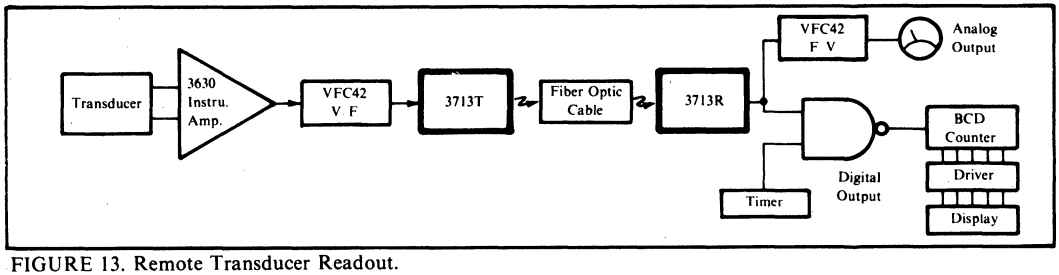
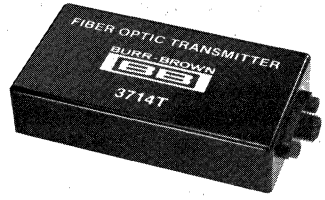


FIGURE 13. Remote Transducer Readout.

BURR-BROWN®

3714T



Analog Input Voltage-to-Frequency FIBER OPTIC TRANSMITTER

FEATURES

- ANALOG SIGNAL CONDITIONING
  - Instrumentation amplifier input
  - CMR of 106dB min at G = 1000
  - Input impedance of $10^{10}\Omega$
- EXCELLENT DC LINEARITY (±0.05% max of FSR)
- LONG DISTANCE OPERATION (up to 1.7km)
- FREQUENCY MODULATED TRANSMISSION
- IMMUNITY TO ELECTROMAGNETIC INTERFERENCE
- NO EXTERNAL RADIATED SIGNAL
- ELECTRICAL ISOLATION
- SELF-CONTAINED

APPLICATIONS

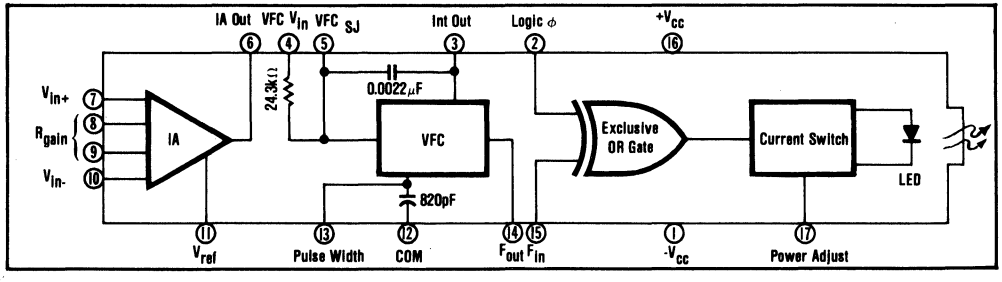
- REMOTE INSTRUMENTATION SYSTEMS FROM LOW LEVEL SENSORS
- INDUSTRIAL PROCESS CONTROL
- POWER PLANT CONTROL
- MEDICAL MONITORING
- HIGH VOLTAGE OR ELECTROMAGNETIC FIELD RESEARCH
- LOW COST ANALOG-TO-DIGITAL CONVERSION
- FACTORY DATA COLLECTION
- SECURITY SYSTEMS
- INTRINSIC SAFETY

DESCRIPTION

The 3714T is a versatile, self-contained, analog input fiber optic transmitter module. When connected to a suitable fiber optic cable and receiver, it is capable of transmitting analog input signals as small as 10mV full scale for a distance up to 1.7km with a typical linearity error of ±0.005%. In addition, it will transmit a CMOS logic signal at data rates from DC to 2M baud NRZ. The 3714T contains a precision instrumentation amplifier (IA), voltage-to-frequency converter (VFC), and fiber optic transmitter section (FOT).

The IA provides high input impedance of $10^{10}\Omega$, CMR of 106dB, programmable gain up to 1000V/V, and level shifting for ±5V max bipolar signals. The VFC linearly converts input voltages between 0 and +10V to an adjustable pulse train ranging from 0 to 50kHz. A DC input produces a fixed frequency output and a dynamic analog input produces a frequency modulated output. The FOT drives the output LED at a resistor programmable power level.

An AMP™ optimate optical connector on the metal case (EMI shielding) allows easy interfacing to a fiber optic cable without alignment difficulty.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

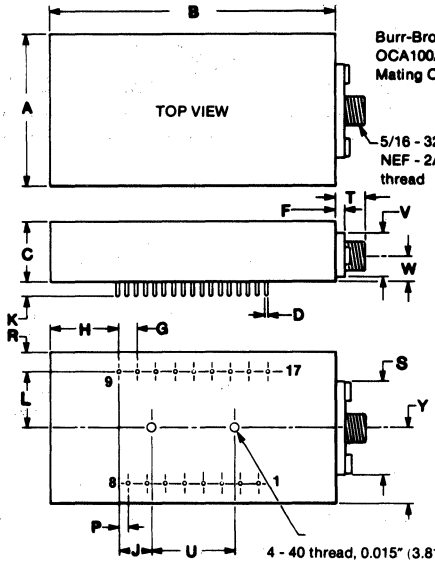
ELECTRICAL

Specifications at T_A = +25°C, $\pm V_{CC}$ = 15VDC

MODEL		TRANSMITTER 3714T			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSFER FUNCTION(1)	$G_T = G_{IA} \times G_{VFC}$ in Hz/V				
INSTRUMENTATION AMPLIFIER SECTION					
Transfer Function	$G_{IA} = IA_{out}/(V_{in+} - V_{in-}) = 1 + (40k/R_G)$ in V/V				
Input(2)					
Unipolar		0		10	V
Bipolar		-5		+5	V
Gain Range		1		1000	V/V
Input Impedance					
Differential			$10^{10} \parallel 3$		Ω || pF
Common-mode			$10^{10} \parallel 3$		Ω || pF
Input Offset Voltage			$\pm 25 \pm (200/G)$	$\pm 50 \pm (400/G)$	µV
Input Offset Drift				$\pm 2 \pm (20/G)$	µV/°C
Bias Current			±10	±30	nA
Bias Drift			±0.3		nA/°C
Offset Current			±10	±30	nA
Linearity			$\pm 0.002 + 10^{-5}G$		% of p-p FS
Settling Time(3) to .01% of FSR	G = 5		100		µsec
	G = 100		150		µsec
	G = 1000		1000		µsec
CMR w/1kΩ source imbalance	DC to 60Hz, G = 1	80	90		dB
	DC to 60Hz, G = 10	96	106		dB
	DC to 60Hz, G = 1000	106	110		dB
VOLTAGE-TO-FREQUENCY CONVERTER SECTION					
Transfer Function	$G_{VFC} = (120 \times 10^{-3})/(C_1 + 820 \times 10^{-12})(R_2 + 24.3 \times 10^3)$ in Hz/V				
Gain Error (adjustable to zero)				±5	% of FSR
Linearity	0.01Hz ≤ F ≤ 10kHz		±0.002	±0.01	% of FSR
	0.1Hz ≤ F ≤ 50kHz		±0.005	±0.05	% of FSR
Offset Error				±0.05	% of FSR
Power Supply Sensitivity			0.01		% of FSR/%
Gain Drift			±75	±175	ppm/°C
Offset Drift			±1	±4	ppm/°C
Settling Time	to within linearity spec		1 pulse of new frequency plus 1µsec		
Overload Recovery Time					
OPTICAL OUTPUT (FIBER OPTIC TRANSMITTER) SECTION					
Output Power(4)(5)	1016µm, 0.53NA	10	15		µW
(Adj. for Max)	368µm, 0.53NA	1.5	3.5		µW
	200µm, 0.4NA	0.7	1.5		µW
Output Power Adjust Range(5)			17		dB
Wavelength	30nm spectral half width		660		nm
Rise Time	10% to 90%		50		nsec
Fall Time	90% to 10%		80		nsec
Bit Rate(6)	Transmitter only		0 to 2M		baud
DIGITAL CMOS INPUT					
Input "High" Threshold		70			%V_{CC}
Input "Low" Threshold				30	%V_{CC}
POWER SUPPLY					
Voltage		±10	±15	±17	V
Current	LED on, max power		+60, -17		mADC
	LED on, min power		+25, -17		mADC
	LED off		+19, -17		mADC
TEMPERATURE					
Operating		0		+70	°C
Storage		-25		+85	°C

NOTES:
1. Total Transfer Function is adjustable and is nominally 5kHz/volt.
2. IA capable of ±10V input. VFC limited to 0 to +10V input. To convert bipolar inputs to unipolar the IA reference is shifted.
3. For low IA gains VFC is predominant for settling.
4. Output power specified is that coupled into three cables shown. Optical output power is measured into an exit Numerical Aperture (NA) of 0.24.
5. Output is adjustable, see Application Information section.
6. Bit rate refers to speed of the transmitter in response to a digital input.

MECHANICAL



Burr-Brown Terminated Fiber Optic Cables OCA100/101/102 and Burr-Brown Electrical Mating Connector 2801MC may be used.

5/16 - 32 NEF - 2A thread

AMP™ Optimate Fiber Optic Connector

NOTE:
1. Leads in true position within 0.015" (38mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

4 - 40 thread, 0.015" (3.81 mm) min. depth 2 places in true position within 0.015" (38mm) R at MMC.

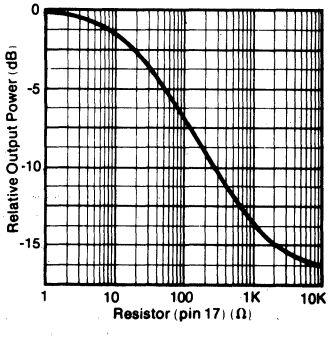
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.610	1.650	40.89	41.91
B	3.020	3.060	76.71	77.72
C	.640	.680	16.26	17.27
D	.038	.042	0.97	1.07
F	.075	.095	1.91	2.41
G	.200 BASIC		5.08 BASIC	
H	.670	.770	17.02	19.56
J	.355 BASIC		9.02 BASIC	
K	.250	.350	6.35	8.89
L	.600 BASIC		15.24 BASIC	
P	.100 BASIC		2.54 BASIC	
R	.165	.265	4.19	6.73
S	.980	1.020	24.89	25.91
T	.275	.315	6.99	8.00
U	.890 BASIC		22.61 BASIC	
V	.460	.500	11.68	12.70
W	.260	.300	6.60	7.62
Y	.795	.835	20.19	21.21

PIN DESIGNATIONS

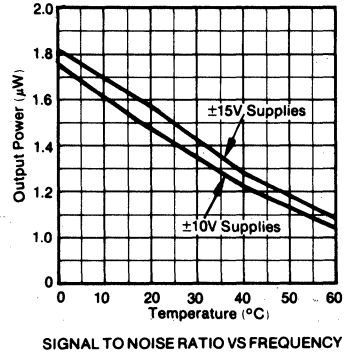
1. $-V_{CC}$	7. $+V_{in}$	13. Pulse width
2. Logic ϕ	8. R_G	14. F_{out}
3. Int Out	9. R_G	15. F_{in}
4. VFC_{in}	10. $-V_{in}$	16. $+V_{CC}$
5. $VFC_{S.J.}$	11. V_{ref}	17. Pwr Adj
6. IA_{out}	12. Common	

TYPICAL PERFORMANCE CURVES

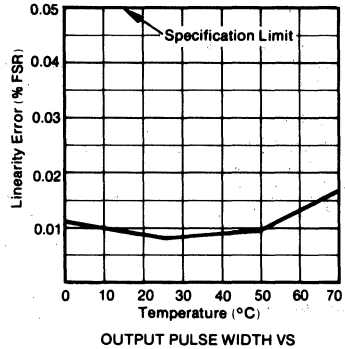
RELATIVE OUTPUT POWER VS CURRENT SETTING RESISTOR



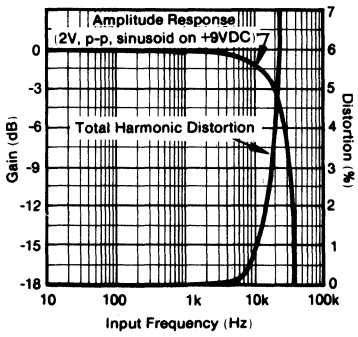
OUTPUT POWER VS TEMPERATURE (launched into 0.25NA, 200μm fiber)



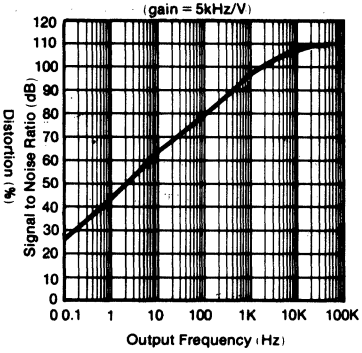
LINEARITY ERROR VS TEMPERATURE



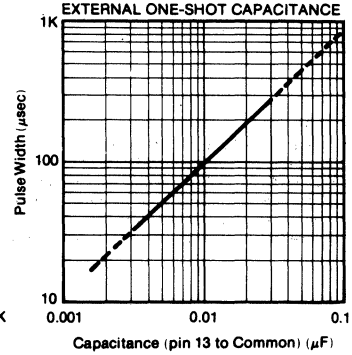
BANDWIDTH AND DISTORTION OF VFC



SIGNAL TO NOISE RATIO VS FREQUENCY (gain = 5kHz/V)



OUTPUT PULSE WIDTH VS EXTERNAL ONE-SHOT CAPACITANCE



THEORY OF OPERATION

The block diagram of the 3714T is on the front page of this data sheet. All circuits are pretested and compatible. The precision instrumentation amplifier will accept a differential analog signal input through pins 7 and 10 and produce a single-ended output at pin 6. This section contains low drift, low noise, monolithic operational amplifiers in a three-stage arrangement. The instrumentation amplifier has the advantages of high input impedance ($10^{10}\Omega$ || 3pF), high common-mode rejection (106dB at G = 1000), low offset voltage (25μV), adjustable gain up to 1000, and adjustable reference to handle unipolar and bipolar inputs. For further detail see the data sheet on the Burr-Brown 3630AM.

The VFC section is a monolithic voltage-to-frequency converter which produces a digital pulse train output at pin 14 with a repetition rate directly proportional to the analog input voltage level at pin 4. The output frequency is initially set at 50kHz full scale by an 820pF capacitor and can be decreased by adding capacitance at pin 13 to Common, pin 12. This capacitor changes the pulse width of a one-shot which controls the direction and duration of a ramping voltage (see Typical Performance Curves). The ramp is produced by an operational amplifier integrator with a nominal capacitor of 0.002μF. The rise and fall depends on this capacitor in addition to the resistor connected between pin 4 and pin 6 in series with the internal 24.3kΩ resistor. An external capacitor can be added between the Integrator Output, pin 3, and the operational amplifier Summing Junction, pin 5, to lower the ramp. The VFC has the advantages of high linearity (±0.05% of FSR max at 50kHz full scale), good stability, and frequency modulated output. For further detail see the data sheet on the Burr-Brown VFC32BM.

The Transmitter section consists of an Exclusive OR gate which drives a current switch to power the LED. The logic phase input at pin 2 determines whether or not the logic level input at pin 15 will be inverted through the gate. The LED light output intensity (power) can be increased by connecting resistance between pin 17 and Common, pin 12. Shorter cable links require less light power to prevent receiver input saturation. This also prolongs LED lifetime and reduces power consumption in the transmitter (see Typical Performance Curves).

In the fundamental configuration, the optical signal is frequency modulated. It radiates no external energy, is immune to interference, and is electrically isolated.

The fiber optic connector is aligned at the factory for optimum performance. This alignment will be disturbed if the connector mounting screws are loosened.

POWER SUPPLY CONNECTIONS

The 3714T requires ±15V supplies only. For optimum performance and noise rejection, all required supply bypassing capacitors are internal. A low resistance external ground return path must be provided for the IA input bias currents (pins 7 and 10). This lowers DC offset errors. Figure 1 shows a configuration with minimal connections and external components for a usable transmitter circuit.

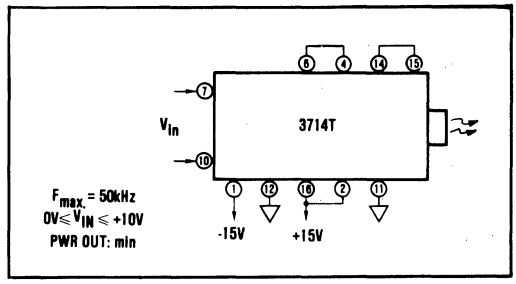


FIGURE 1. Minimal Connections.

OPTICAL POWER ADJUSTMENT

The optical power of the 3714T may be adjusted by controlling the resistance between the Power Adjust, pin 17 and Common, pin 12. The following equation shows LED current.

$$I_{LED} \approx 0.65 \div [1k\Omega \parallel (22 + R_1)] \quad (1)$$

where R_1 is the external resistor shown in Figure 2.

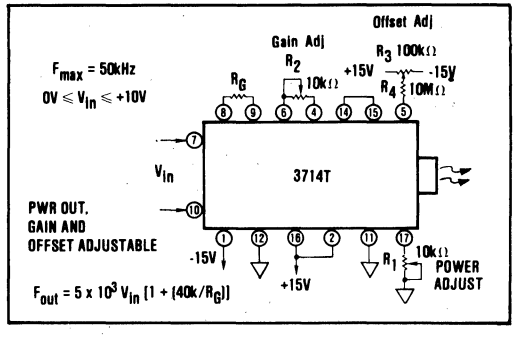


FIGURE 2. Typical Connections.

The leads on R_1 should be kept short. When the resistor is minimum the LED output is maximum, and as R_1 is increased, the output asymptotically approaches a minimum value. This is shown in the performance curve "Relative Output Power vs Current Setting Resistor". LED power should be no greater than that required by the cable and receiver (3713R). See Cable Selection section for details.

FULL SCALE FREQUENCY ADJUSTMENT

The full scale frequency of the 3714T may be reduced for use with lower speed receivers. Two external capacitors shown in Figure 3 are chosen as follows.

$$C_1 = (4.1 \times 10^{-5}) / f_{max} - 8.20 \times 10^{-10} \text{ farads} \quad (2)$$

Select the closest standard value to the capacitance given by the equation. A low drift capacitor such as an NPO ceramic or silver mica type is recommended. The initial tolerance is not critical since R_2 will be adjusted to remove initial gain errors.

$$C_2 = (10^{-4} \cdot f_{max}) - 2.2 \times 10^{-9} \text{ farads} \quad (3)$$

Select one for low leakage and low dielectric absorption. A mylar or polycarbonate type is recommended.

VFC OFFSET ADJUSTMENT

The offset may be adjusted by injecting a small current into the Summing Junction (SJ) of the VFC. This can be accomplished by connecting a 10kΩ to 100kΩ potentiometer, R_3, and 10MΩ resistor to pin 5 as shown in Figure 2. 1A V_{ref} at pin 11 can also be used (see Bipolar Operation). Establish the offset by: (1) applying a DC input voltage at pins 7 and 10 to produce an output frequency of 0.001 x full scale and (2) adjusting R_3 for proper output frequency at pin 14.

GAIN ADJUSTMENT

Overall gain is defined in terms of frequency out divided by voltage in. The general transfer function of Figure 3 is:

$$G_T = \frac{F_{out}}{F_{in}} = \frac{120 \times 10^{-3}[1 + (40 + 10^3/R_G)]}{(C_1 + 820 \times 10^{-12})(R_2 + 24.3 \times 10^3)} \text{ in Hz/V} \quad (4)$$

where,

$[1 + (40 \times 10^3/R_G)] = G_{1A}$ = Instrumentation Amplifier Gain

$(C_1 + 820 + 10^{-12})$ = VFC total one-shot capacitance

$(R_2 + 24.3 \times 10^3)$ = VFC total gain setting resistance

R_G = external 1A gain setting resistor in ohms between pins 8 and 9.

C_1 = external one-shot capacitor in farads between pins 3 and 5.

R_2 = external VFC gain setting resistor in ohms between pins 6 and 4.

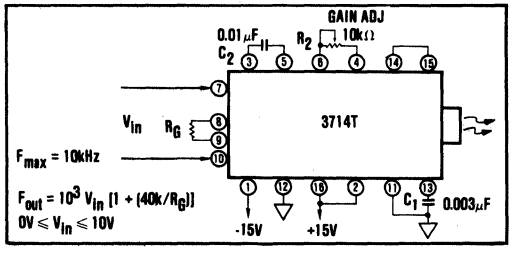


FIGURE 3. 10kHz Full Scale Connection.

The nominal value of R_2 is 5kΩ, but a 10kΩ potentiometer with a TCR of 100ppm/°C can be used to minimize gain error. Set gain by: (1) Applying desired full scale DC input voltage at pins 7 and 8 and (2) adjusting R_2 for desired frequency at pin 14.

Once the gain error is zeroed, 1A gain may be changed while maintaining a very high overall gain accuracy. R_G then sets the gain according to the equation:

$$G_{1A} = 1 + (40k/R_G) \quad (5)$$

for calibration of the basic circuit (Figure 2). This involves an iteration between VFC Offset adjustment and Gain adjustment.

Example: $0V \leq V_{in} \leq +10V$

$0Hz \leq F_{out} \leq 50Hz$

$G_T = F_{out}/V_{in} \approx 4.994kHz/V$ calculated

(1) Set V_{in} = +10mV ±0.1mV and adjust R_3 for 50Hz ±1Hz at F_{out}, pin 14.

(2) Set V_{in} = +10V ±1mV and adjust R_2 for 50kHz ±1Hz at F_{out}, pin 14.

(3) Iterate as necessary.

CURRENT INPUT CONNECTION

A current input connection can also be achieved by injecting a current into the VFC Summing Junction at pin 5. This is shown in Figure 4.

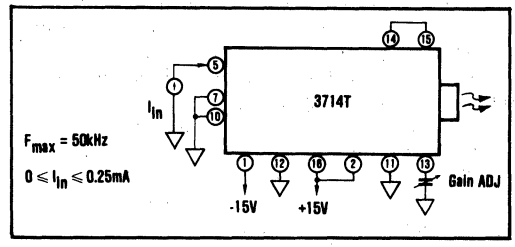


FIGURE 4. Current Input Connection.

BIPOLAR INPUT OPERATION

A bipolar input can be accommodated by offsetting the 1A output at the V_{ref}, pin 11. Figure 5 shows how this is done. The offsetting is necessary because the VFC can only accept positive inputs. The effective offset is twice the voltage applied to pin 11. V_{ref} source impedance should be less than 10kΩ.

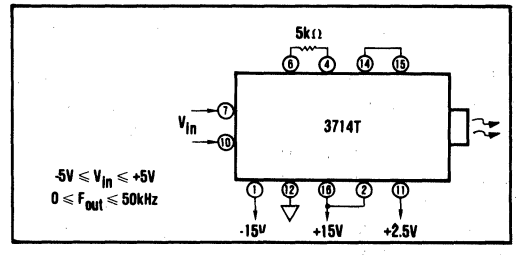


FIGURE 5. Bipolar Input Connection.

LOGIC ϕ SELECTION

When Logic ϕ, pin 2, is +15V, the LED is on for a logic high at F_{in}, pin 15. It is opposite when pin 2 is 0V. This helps detect cable breaks with idle data inputs, and permits optimizing response of receivers using peak detection for automatic threshold adjustment.

LOGIC INPUT OPERATION

Figure 6 shows a CMOS Logic Input connection.

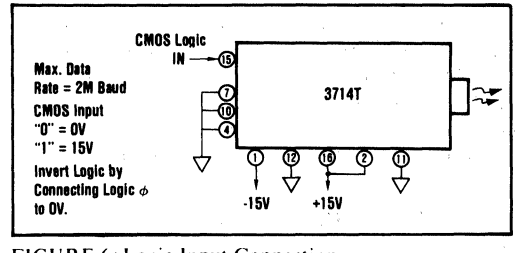


FIGURE 6. Logic Input Connection.

COMPATIBLE FIBER OPTIC RECEIVER

The 3712R and 3713R are compatible receivers for the 3714T transmitter. As shown in Figure 10, Application Information section, the recovered FM digital 3713R

output can be demodulated by a frequency-to-voltage converter to obtain an analog signal. An inexpensive analog-to-digital converter is also shown in Figure 10 by using a gate and counter to record pulse over a fixed time period.

CABLE SELECTION

The 3714T and 3713R with the AMP™ Optimate Single Position Fiber Optic Cable Connector System can be used with a wide variety of cable types. The choice of a cable type for a particular application, of course, depends upon the details of that application: link environment, link length, cable performance characteristics, and cable cost.

ENVIRONMENTAL CONSIDERATIONS

The mechanical stresses, environmental temperature extremes, and exposure to harsh chemicals must be considered when choosing a particular cable. Such things as jacketing material and the type of added strength members, see Figure 7, determine a cable's mechanical and environmental capabilities. Table I is a representative list of cable manufacturers who make cable compatible with the 3714T. See Table II for details of cable performance.

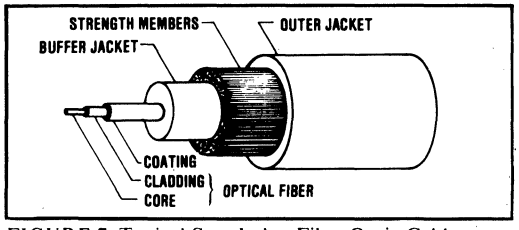


FIGURE 7. Typical Step Index Fiber Optic Cable Construction.

TABLE I. 3714T Compatible Cable Manufacturers.

AMP (CONNECTORS)
(717) 546-0101
AMP, Inc.
499 Eisenhower Blvd.
Harrisburg, PA 17105

DUPONT (CROFON)
(302) 774-6595
E.I. Dupont De Nemours
PP & R Dept., Room D-12086
Crofon Fiber Optics Group
Wilmington, DE 19898

GALILEO
(617) 347-9191
Galileo Electro-Optics
Galileo Park
Sturbridge, MA 01518

VALTEC
(617) 835-6082
Valtec Corp.
Fiber Optics Div.
West Boylston, MA 01583

BELDEN
(312) 232-8900
Belden Corp.
2000 South Batavia
Geneva, Il 60134

DUPONT (PIFAX)
(302) 774-7850
(302) 774-6339
E.I. Dupont De Nemours
Plastic Products & Resins
Wilmington, DE 19898

MAXLIGHT
(602) 269-8387
Maxlight
Optical Waveguides, Inc.
3035 N. 33rd Drive
Phoenix, AZ 85017

DETERMINING CABLE TYPE

There are three basic types of optical fibers to choose from: Step-Index, Single-Mode, and Graded-Index. Each type specifies the profile or variation of the fiber's index of refraction as a function of radial distance from the fiber's center. In a fiber with a step-index profile, the refractive index undergoes an abrupt change (step) in value. This step is caused by the sudden change in the index of refraction between the fiber's core and a surrounding annular cladding, as shown in Figure 8.

Step-index fiber with a core diameter of 200μm or larger is recommended for use with the 3714T and 3713R. Step-index fiber offers the best compromise between core diameter, bandwidth, coupling loss, and cost. Single-mode and graded-index fibers are not recommended due to their small core diameter. The wide bandwidth characteristics of these cables are not needed.

TABLE II. Link Performance vs Various Cable Types.

Cable Manufacturer and Part Number	Cable Characteristics					Link Performance						Recommended AMP™ Connector
	Core Dia. (μm)	Fiber(1) Dia. (μm)	Cable Dia. (mm)	LA(2) at 660nm (dB/km)	Material NA	PL (μW)		LM (dB)		XMAX (meters		
						min	typ	min	typ	min	typ	
BELDEN												
220001	200	400	3.8	12	0.35	0.7	1.5	14	20	1140	1667	Contact Belden
221001	300	440	3.8	12	0.35	1.1	2.6	16	22	1304	1866	Contact Belden
DUPONT												
Crofon 1040*	1016	1016	2.2	1300	0.53	10	15	25	30	19	23	530530-2
PIFAX-P140**	368	400	1.9	360	0.53	1.5	3.5	17	24	34	47	530530-9
PIFAX-PIR140	368	400	1.9	330	0.53	1.5	3.5	17	24	51	72	530530-9
PIFAX-S120	200	600	2.4	43	0.4	0.7	1.5	14	20	318	465	1-530530-2
PIFAX-S120*** (type 30)	200	600	2.4	33	0.4	0.7	1.5	14	20	415	606	1-530530-2
GALILEO												
3000LC-P	204	245	2.2	100	0.48	0.7	1.5	14	20	137	200	530530-9,
MAXLIGHT												
KSC200A	200	300	2.4	8	0.39	0.7	1.5	14	20	1710	2500	(3)
KSC200B	200	300	2.4	27	0.39	0.7	1.5	14	20	507	741	(3)
VALTEC												
MD-PC100	250	430	4.1	14	0.30	0.9	2.0	15	21	1055	1518	530530-9

1) Fiber Diameter = Core Diameter plus Cladding. 2) Conversion Factors: 100μm = 0.003937 in; 1000m = 3281 ft. 3) Sold as terminated cable.
*Same as Burr-Brown OCA100. **Same as Burr-Brown OCA101. ***Same as Burr-Brown OCA102.

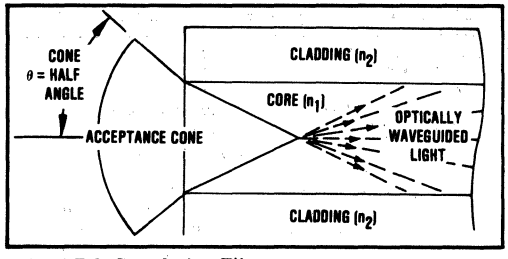


FIGURE 8. Step Index Fiber.

DETERMINING LAUNCHED POWER

Once the mechanical characteristics and cable type have been chosen, it becomes necessary to analyze link performance with various cables. The first analysis to make is the power launched into a particular cable from the transmitter.

An advantage of the 3714T over many other fiber optic transmitters is the way output power has been specified. The 3714T specifies the actual power launched into the cable. Thus, such complicated effects as LED output power and emission profile, cable numerical aperture (NA), and spacing between the LED transmitter and the cable have all been taken into consideration for the user. For cables other than those specified in the Electrical Specification Table, the power launched may be determined from the curve in Figure 9.

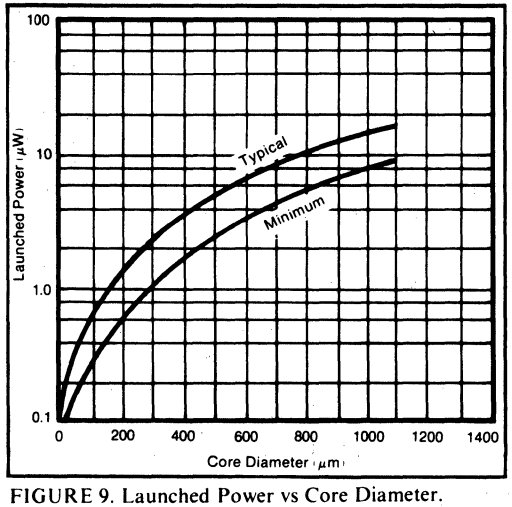


FIGURE 9. Launched Power vs Core Diameter.

DETERMINING MAXIMUM CABLE LENGTH

Once P_L and $L\lambda$ are known, the maximum cable length may be obtained. First the loss margin is found by,

$$LM(dB) = 10 \log (P_L / P_{in\ min}). \quad (6)$$

For the 3714T with CROFON 1040 1016μm fiber, P_L = 10μW and for the 3713R, $P_{in\ min}$ = 30nW worst-case for 10^{-9} BER. Thus,

$$LM = 10 \log (10\mu W / 30nW) = 10 \log 333 = 25dB.$$

Then X_{max}, the maximum cable length that will just present $P_{in\ min}$ to the transmitter is found by,

$$X_{max} = [LM(dB)]/[L\lambda(dB/m)].$$

For CROFON 1040 at λT = 670nm, $L\lambda$ = 1300dB/km

$$X_{max} = 25dB/(1.3dB/m) = 19 \text{ meters.}$$

If this length is too short, a cable with a larger diameter (larger P_L) or less attenuation (smaller $L\lambda$) must be used.

Table II shows the link performance for several different cables.

DETERMINING MINIMUM CABLE LENGTH

Short cable lengths with large core diameter fibers may cause some receiver slew rate limit which will appear as duty cycle distortion. Limiting the power coupled into the receiver from the cable will prevent this from occurring.

The minimum cable length may be determined for a specific cable by calculating the power launched into it as previously done using the typical curve from Figure 9. The typical value of launched power should be used since this will give the most power into the receiver, resulting in the desired minimum cable length.

As an example, consider a cable with a 368μm core diameter and a cable loss of 330dB km. The typical power launched into the cable from Figure 9 is 3.5μW.

The minimum loss margin is found using the typical power launched into the cable and the maximum input to the receiver which is 1μW for the 3713R.

$$LM = 10 \log (P_L\ P_{in\ max})$$

$$LM = 10 \log (3.5\mu W\ \ 1\mu W) = 5.4dB.$$

The minimum cable length for the specific cable in this example is:

$$X_{min} = LM_{min}\ \ L\lambda$$

$$X_{min}\ (5.4dB/0.33dB\ \ m) = 16 \text{ meters.}$$

If this minimum cable length is too long for a particular application, use a smaller core diameter cable, a cable with higher loss, or the power launched into the cable may be reduced as described in the Optical Power Adjustment section.

APPLICATION INFORMATION

Parameters of the OCA100 101 102 fiber optic cables appear in the Cable Selection section. The 3712R or 3713R are compatible receivers. The 2801MC is an electrical mating connector.

PRECAUTIONS

The 3714T contains protected CMOS circuitry; however, to prevent failures, anti-static handling procedures should be observed and the F_{in} and Logic ϕ inputs must be committed to either 0V or +15V prior to turn-on and during operation. Loosening of the cable connector can cause misalignment of the LED and fiber.

RECEIVERS

The 3713R will operate over the full 50kHz bandwidth of the 3714T. However, the 3712R will allow longer link lengths, but at a lower bit rate of 20k bits sec (10kHz). In this case the full scale frequency of the 3714T should be set to 10kHz (see Figure 3).

APPLICATION CIRCUITS

The 3714T Fiber Optic Data Link solves such data transmission problems as crosstalk, ringing, and echos. Electromagnetic radiation interference is avoided when using a fiber optic data link in high noise environments.

Lightning damage to cables and connecting equipment can be eliminated where fiber optic cables replace metalic conductors. In refineries and chemical plants which have explosive atmospheres, sparks from shorted electrical cables are eliminated by the fiber optic cable - an inherent safety feature. The unique features of the 3714T allow it to be used directly with transducers requiring high sensitivity and linearity. Also, an inexpensive analog-to-digital converter can readily be constructed. Figures 10 thru 13 illustrate the use of the 3714T transmitter and 3713R reciever.

One major application of the 3714T is a Remote Transducer Readout, Figure 10. This arrangement utilizes the key features of sensitivity and linearity. The transducer can be connected directly to the 3714T input eliminating the requirement for an external precision instrumentation amplifier. Recovery of the analog signal can be achieved by a frequency-to-voltage converter such as the VFC42. A digital display can easily be produced by counting the TTL pulses from the output of the 3713R. In Figure 12, voice can be amplitude modulated and a sensor can be frequency modulated over the same cable. Also, two-channel multiplexing is possible as shown in Figure 13.

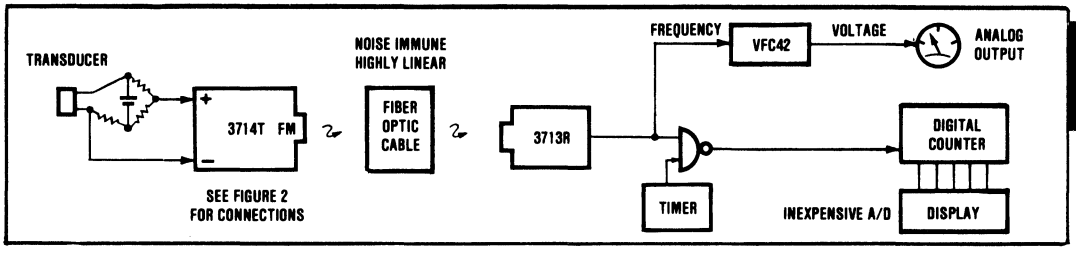


FIGURE 10. Remote Transducer Readout.

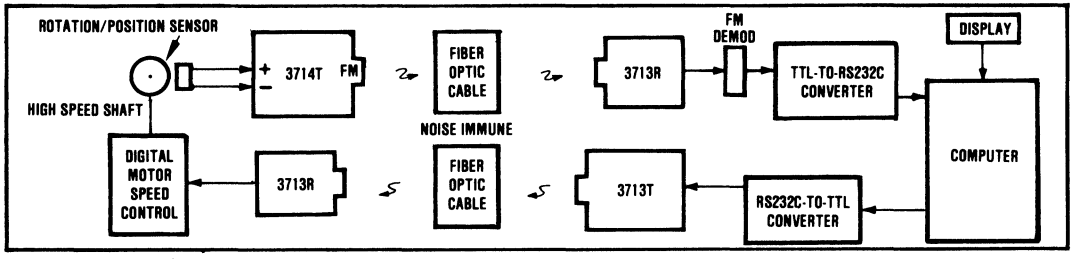


FIGURE 11. Monitor and Control System Using a High Speed Rotation Position Sensor.

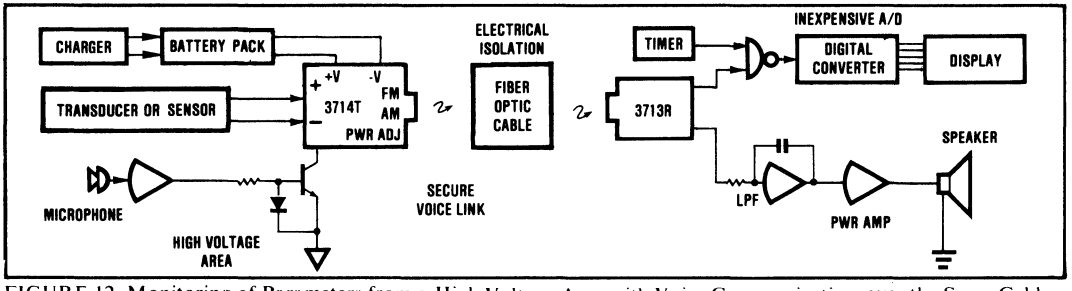


FIGURE 12. Monitoring of Parameters from a High Voltage Area with Voice Communication over the Same Cable.

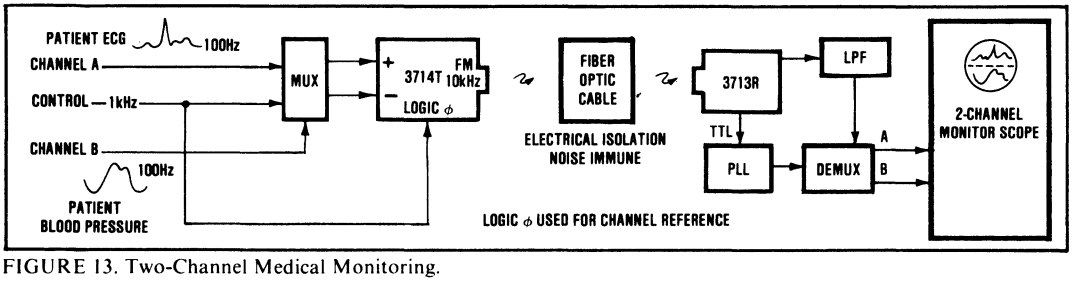
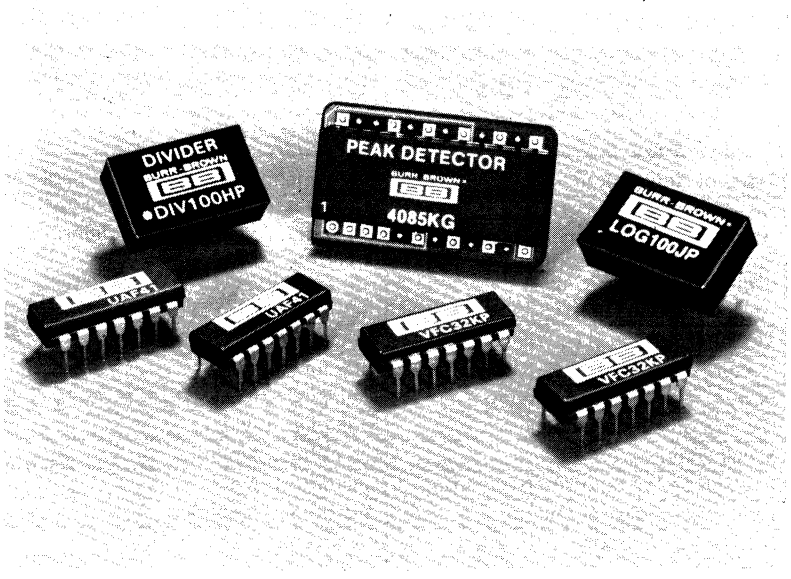


FIGURE 13. Two-Channel Medical Monitoring.

ANALOG CIRCUIT FUNCTIONS



5

Analog circuits act as building blocks with which to perform a variety of instrumentation, computation, and control functions. They provide a broad range of versatile, proven, and ready to use computational function circuits for the designer to use in developing simple or complex systems. The analog circuit functions include multipliers, dividers, multifunction converters, true rms-to-DC converters, logarithmic amplifiers, voltage and window comparators, peak detectors, precision oscillators, and filters. The multifunction converter also provide multiply, divide, square root, exponentiate, roots, sine, cosine, arctangent, vector magnitude RMS-to-DC and logarithmic amplifier functions.

The availability of these relatively complex functions as precise, versatile, easy-to-use, low-cost building blocks has broadened the scope of practical analog circuit systems and greatly simplified analog circuit designs. The names of most analog circuit functions are self-explanatory and describe the main functions they perform.

The functions are used mostly for processing (handing) and/or conditioning of analog signals, and usually (though not always) for simulation of algebraic and/or trigonometrically expressed analog computations. The variety of applications these functions are effectively used for, are limited only by the designer's creative imagination. Some of the interesting applications where analog circuit functions have found wide acceptance are listed in the table on the following page.

Types of Applications	Recommended Analog Circuit Function
Analog simulation. Algebraic and trigonometric computations. Power series approximation, function fitting and linearizing Analog wave shaping.	Multiplier, Divider, Multifunction Converter, Logarithmic Amplifier, Oscillator.
VCO and AGC applications.	Multiplier, Divider.
Vector computation.	Multifunction Converter, Multiplier.
Power and energy measurements.	Multiplier, RMS-to-DC Converter.
Moduation and demodulation.	Multiplier, Divider.
Signal compression.	Logarithmic Amplifier.
Log-antilog-log ratio computations.	Logarithmic Amplifier.
Light-related measurements.	Logarithmic Amplifier.
Analog signal conditioning.	All circuit functions.
Instrumentation and control systems.	All circuit functions.
Variety of test equipment.	All circuit functions.
Transducer excitation	Oscillator.
Signal reference.	Oscillator.
Alarm circuits.	Voltage and Window Comparators.
Bang-bang control applications.	Voltage and Window Comparators.
Control of limit stops.	Voltage and Window Comparators.
Analog memory and peak detection.	Peak Detection.
Fixed-frequency tuned filters.	ATF-76 Filters.

SELECTION GUIDE
Analog Circuit Functions

These circuits offer a broad range of versatile, proven and ready-to-use analog computational functions designed to work in simple and complex instrumentation and control systems. Primarily they process and/or condition analog signals - usually for simulation of algebraic or trigonometric computations. Burr-Brown has the widest selection of such functions available in the industry. How you apply these circuits is limited only by your creative imagination!

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% to 2% max from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy - no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

MULTIPLIERS/DIVIDERS

Model(1)	Transfer Function	Accuracy max at 25°C %, max	Temperature Coefficient %/°C	Feed-through mV	Offset Voltage mV	1% Bandwidth kHz	Temp Range(2)	Package	Price ($) Unit	Price ($) 100's	Page
4203J	XY/10	2	0.04	50	20	40	Com	TO-100	35.20	19.00	5-41
4203K	*	1	0.04	50	20	40	Com	TO-100	48.20	33.80	5-41
4203S, (Q)	*	1	0.04	50	20	40	Mil	TO-100	77.00	--	5-41
4204J	*	0.5	0.01	10	15	32	Ind	DIP	68.00	51.00	5-43
4204K	*	0.5	0.01	5	5	33	Ind	DIP	88.75	64.50	5-43
4204S, (Q)	*	0.25	0.02	5	5	33	Mil	DIP	101.00	82.00	5-43
4205J	$(X_1 - X_2)(Y_1 - Y_2)/10$	2	0.04	50	20	40	Com	TO-100	31.00	19.40	5-41
4205K	*	1	0.04	50	20	40	Com	TO-100	45.15	29.35	5-41
4205S, (Q)	*	1	0.04	50	20	40	Mil	TO-100	64.50	38.80	5-41
4206J	XY/10	0.5	0.01	10	15	33	Com	DIP	47.00	29.35	5-49
4206K	*	0.25	0.01	5	5	33	Com	DIP	66.80	41.00	5-49
4213AM, (Q)	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.008	30	10	70	Ind	TO-100	29.35	18.90	5-55
4213BM	*	0.5	0.008	30	7	70	Ind	TO-100	42.50	28.30	5-55
4213SM	*	0.5	0.008	30	7	70	Mil	TO-100	55.00	37.75	5-55
4213/MIL Series				See Military Products							
4214AP	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.02	30	10	70	Ind	DIP	24.50	16.30	5-62
4214BP	*	0.5	0.02	30	7	70	Ind	DIP	36.70	26.50	5-62
4214RM	*	1	0.02	30	10	70	Ind	DIP	29.60	22.65	5-62
4214SM	*	0.5	0.02	30	7	70	Ind	DIP	47.95	35.70	5-62

*Same as model above. NOTES: 1) "(Q)" indicates product also available with screening for increased reliability.
2) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C.

DIVIDERS

The use of a special log/antilog committed divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS

Model	Transfer Function	Input Range	Accuracy, max D = 250mV %	Temperature Coefficient %/°C	0.5% Bandwidth kHz	Rated Output, min	Temp Range(1)	Package	Price ($) Unit	Price ($) 100's	Page
DIV100HP	N/D 10	250mV	1.0	0.2	15	±10V, ±5mA	Ind	DIP	28.75	17.25	5-6
DIV100JP	*	to	0.5	0.2	15	±10V, ±5mA	Ind	DIP	40.25	26.45	5-6
DIV100KP	*	10V	0.25	0.2	15	±10V, ±5mA	Ind	DIP	57.50	40.25	5-6

*Same as model above. NOTES: 1) Ind = -25°C to +85°C.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems.

Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

Model	Function	Description	Comments	Temp Range(1)	Package	Price ($) Unit	Price ($) 100's	Page
4301 4302	Multifunction Converter	$Y(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	4301 is hermetically sealed and shielded in a metal package. 4302 is in a plastic package. Both units are pin-for-pin compatible.	Ind Ind	DIP DIP	90.75 50.00	64.70 30.60	5-66 5-68
LOG100JP	Log Ratio Amplifier	$K \text{ Log } (I_1/I_2)$ Can provide log and log ratio of current or voltage inputs. Also forms antilog.	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA). 55mV total error; 0.25% log conformity.	Com	DIP	36.00	25.00	5-14
4127JG 4127KP	Logarithmic Amplifier	$K \text{ Log } (I_1/I_{REF})$	A more versatile part which contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com Com	DIP DIP	46.00 53.00	31.10 39.80	5-34 5-34
4340	$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	True rms-to-DC conversion based on a log-antilog computational approach.	Laser-trimmed, requires no external trimming for rated accuracy. Hermetically sealed in a metal package.	Ind	DIP	90.75	64.20	5-74
4341	$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2 dt}$	True rms-to-DC conversion based on a log-antilog computational approach.	Some external trimming required. Lower cost in plastic package. Pin compatible with 4340.	Ind	DIP	27.00	16.85	5-78
4085BM 4085KG 4085SM	Peak Detector	These are analog memory circuits which hold and provide read-out of a DC voltage equal to peak value of a complex input waveform.	Digital mode control provides reset capability and allows selection of peaks within a desired time interval. May be used to make peak-to-peak detector.	Com Ind Mil	DIP DIP DIP	78.00 67.65 103.00	56.00 47.05 71.90	5-26 5-26 5-26
4115/04	Window Comparator	4115/04 provides a window or dual limit for comparison. Unit has 3 inputs; one for a voltage that sets upper limit, one for a voltage that sets lower limit, and one for a signal input.	The 3 outputs are capable of sinking up to 200mA of current, indicating if the input voltage is above, below, or in the window.	Com	Module	66.30	46.00	5-32
4082/03	Level Comparator	Compares input voltage with user set limit. Provides 2-state logic output that indicates whether one analog voltage is > or < another.	Adjustable hysteresis uncommitted collector output can sink up to 100mA.	Ind	DIP	48.25	31.00	5-24

NOTE: 1) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attenuation. Both fixed frequency and user selected frequency units are available.

Model	Function	Description	Comments	Temp Range(1)	Package	Prices ($) Unit	Prices ($) 100's	Page
4023/25	Oscillator	Fixed-frequency (customer-specified, 10Hz to 20kHz) provides low distortion, stable amplitude sine wave output.	Frequency stability vs temperature: 0.04%/°C max. Amplitude stability vs temperature: 0.02%/°C max.	Ind	Module	199.50	148.00	5-22
4423	Oscillator	Very-low cost in plastic package. Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available).	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP	19.90	13.50	5-82
UAF41 UAF31 UAF21 UAF21H,Q UAF11 UAF11H,Q	Universal Active Filter	These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass and bandpass outputs are available.	Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.	Ind Ind Ind Ind Ind Ind	DIP DIP DIP DIP DIP DIP	18.25 28.95 74.00 81.00 46.35 54.00	9.40 16.00 46.00 56.00 22.75 33.50	5-109 5-101 5-93 5-93 5-93 5-93
ATF76 Series	Fixed-Frequency Active Filter	Over 60 different types of filters are available from combinations of filter type, number of poles and type of response.	Low-pass, bandpass and band reject. Butterworth, Chebyschev and Bessel. 2 to 8 poles.	Ind	DIP	102.00 to 192.00	49.00 to 140.00	5-86

NOTE: 1) Com = 0 to +70°C; Ind = -25°C to +85°C.

GLOSSARY OF TERMS & DEFINITIONS
Analog Circuit Functions

ABSOLUTE-VALUE CIRCUIT
A circuit that produces a unipolar output signal equal to the magnitude or absolute value of a bipolar input signal.

ACCURACY
The deviation from the ideal output voltage defined as a percent of full scale output voltage.

COMPARATOR
A device with two stable output states which signal if an input current or voltage has crossed a threshold. The threshold may be set by one or more other currents or voltages, either fixed or variable.

CREST FACTOR
The ratio of the peak value of a time-varying signal to its rms value.

CURRENT LIMITING
Limiting the output current supplied by a circuit for protection purposes.

FEEDBACK
The return of a portion of the output signal from a device to the input of the device.

FEEDTHROUGH
The input offset parameter applicable to multipliers. It is the output voltage when voltage is applied to one input of the multiplier and the other input is at zero.

FULL POWER FREQUENCY RESPONSE
The maximum frequency at which the output will swing full scale peak-to-peak voltage into a rated load without significant distortion of the output.

HYSTERESIS
The transfer response lag of comparators controlled by positive feedback and resulting in different trip points for the two directions of output transition.

LOGARITHMIC AMPLIFIER
An amplifier which develops an output voltage that is proportional to the logarithm of the input signal.

OUTPUT OFFSET
The output voltage when the inputs are grounded.

RMS
The root-mean-square value of a time-varying signal E(t) over a time period of T is

$$E_{rms} = \sqrt{1/T \int_o^t [E(t)]^2 \, dt}$$

RMS CONVERTER
A circuit that develops a DC output voltage equal in rms value to an input signal of arbitrary waveform.

SETTLING TIME
The time required for the output to respond to a step input and to settle within some specified error band around the output final value.

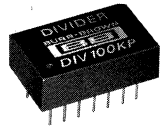
SLEW RATE
The maximum rate of change of an output voltage when supplying the rated output.

SMALL SCALE FREQUENCY RESPONSE
The -3dB output frequency for a small AC signal (normally 1V, p-p) input. For multipliers, one input may be held at +10VDC or -10VDC and the other input held at small AC signal.

WINDOW COMPARATOR
A compartor that detects levels within a set range or window rather than simply distinguishing between levels above and below a set point.

BURR-BROWN®

DIV100



ANALOG DIVIDER

FEATURES

- **HIGH ACCURACY**
  0.25% maximum error, 40:1 denominator range
- **TWO-QUADRANT OPERATION**
  Dedicated log-antilog technique
- **EASY TO USE**
  Laser-trimmed to specified accuracy - no external resistors needed
- **LOW COST**
- **DIP PACKAGE**

APPLICATIONS

- **DIVISION**
- **SQUARE ROOT**
- **RATIOMETRIC MEASUREMENT**
- **PERCENTAGE COMPUTATION**
- **TRANSDUCER AND BRIDGE LINEARIZATION**
- **AUTOMATIC LEVEL - AND GAIN - CONTROL**
- **VOLTAGE CONTROLLED AMPLIFIERS**
- **ANALOG SIMULATION**

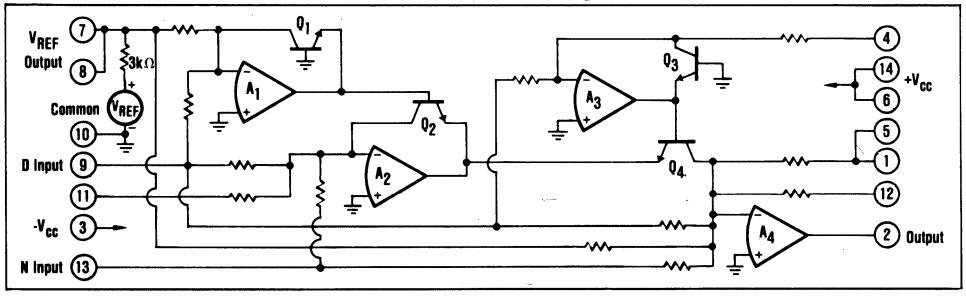
DESCRIPTION

The DIV100 is a precision two-quadrant analog divider offering superior performance over a wide range of denominator input. Its accuracy is nearly two orders of magnitude better than multipliers used for division. It consists of four operational amplifiers and logging transistors integrated into a single monolithic circuit and a laser-trimmed, thin-film resistor network. The electrical characteristics of these devices offer the user guaranteed accuracy without the need for external adjustment - the DIV100 is a complete, single package analog divider.

For those applications requiring higher accuracy than the DIV100 specifies the capability for optional adjustment is provided. These adjustments allow the user to set scale factor, feedthrough, and output-referred offsets for the lowest total divider error.

The DIV100 also gives the user a precision, temperature-compensated reference voltage for external use.

Designers of industrial process control systems, analytical instruments, or biomedical instrumentation will find the DIV100 easy to use and also a low cost, but highly accurate solution to their analog divider applications.



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SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL		DIV100HP			DIV100JP			DIV100KP			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSFER FUNCTION			V_O = 10N/D			*			*		
ACCURACY	$R_L \geq 10k\Omega$										
Total Error											
Initial	$0.25V \leq D \leq 10V, N \leq \lvert D \rvert$		0.7	1.0		0.3	0.5		0.2	0.25	% FSO(1)
vs. Temperature	$1V \leq D \leq 10V, N \leq \lvert D \rvert$		0.02	0.05(2)		*	*		*	*	% FSO/°C
	$0.25V \leq D \leq 1V, N \leq \lvert D \rvert$		0.06	0.2(2)		*	*		*	*	% FSO/°C
vs. Supply	$0.25V \leq D \leq 10V, N \leq \lvert D \rvert$		0.15			*			*		% FSO/%
Warm-up time to rated performance			5			*			*		Minutes
AC PERFORMANCE	D = +10V										
Small-Signal Bandwidth	-3dB		350			*			*		kHz
0.5% Amplitude Error	Small-Signal		15			*			*		kHz
0.57° Vector Error	Small-Signal		1000			*			*		Hz
Full-Power Bandwidth	$V_O = \pm 10V$, $I_O = \pm 5mA$		30			*			*		kHz
Slew Rate	$V_D = \pm 10V$, $I_O = \pm 5mA$		2			*			*		V/μsec
Settling Time	ϵ = 1%, ΔV_O = 20V		15			*			*		μsec
Overload Recovery	50% Output Overload		4			*			*		μsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Numerator	$N \leq \lvert D \rvert$	±10			*			*			V
Denominator	$D \geq +250mV$	+10			*			*			V
Input Resistance	Either Input		25			*			*		kΩ
OUTPUT CHARACTERISTICS											
Full-Scale Output (FSO)		±10			*			*			V
Rated Output											
Voltage	$I_O = \pm 5mA$	±10			*			*			V
Current	$V_O = \pm 10V$	±5			*			*			mA
Current Limit											
Positive			15	20(2)		*			*		mA
Negative			19	23(2)		*			*		mA
OUTPUT NOISE VOLTAGE	N = 0V										
f_B = 10Hz to 10kHz											
D = +10V			370			*			*		μV, rms
D = +250mV			1			*			*		mV, rms
REFERENCE VOLTAGE CHARACTERISTICS	$R_L \geq 10M\Omega$										
Output Voltage											
Initial	At +25°C	6.3(2)	6.6	6.9(2)	*	*	*	*	*	*	V
vs. Supply			±25			*			*		μV/V
Temperature Coefficient			±50			*			*		ppm/°C
Output Resistance			3			*			*		kΩ
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*			*		VDC
Operating Range	Derated Performance	±12		±20	*		*	*		*	VDC
Quiescent Current											
Positive Supply			5	7(2)		*	*		*	*	mA
Negative Supply			8	10(2)		*	*		*	*	mA
AMBIENT TEMPERATURE RANGE											
Specification		0		+70	*		*	*		*	°C
Operating Range	Derated Performance	-25		+85	*		*	*		*	°C
Storage		-55		+125	*		*	*		*	°C

*Same as DIV100H.

NOTES:
1. FSO is the abbreviation for Full Scale Output.
2. This parameter is untested and is not guaranteed. This specification is established to a 90% confidence level.
3. See General Information section for discussion.
4. For supply voltages less than ±20VDC, the absolute maximum input voltage is equal to the supply voltage.
5. Short-circuit may be to ground only. Rating applies to an ambient temperature of +38°C at rated supply voltage.

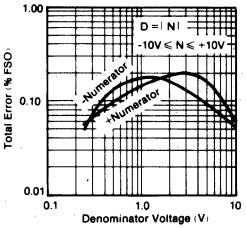
ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(3)	600mW
Input Voltage Range(4)	±20VDC
Storage Temperature Range	-55°C to +125°C
Operating Temperature Range	-25°C to +85°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-Circuit Duration(3)(5)	Continuous
Junction Temperature	175°C

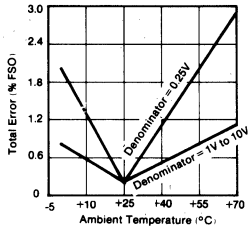
TYPICAL PERFORMANCE CURVES

(TA = +25°C, VCC = ±15VDC unless otherwise noted.)

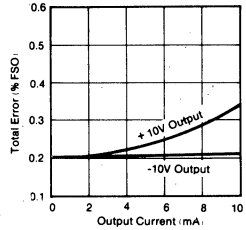
TOTAL ERROR VS DENOMINATOR VOLTAGE



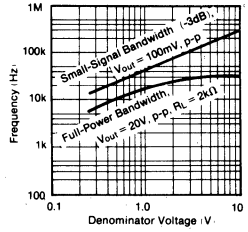
TOTAL ERROR VS AMBIENT TEMPERATURE



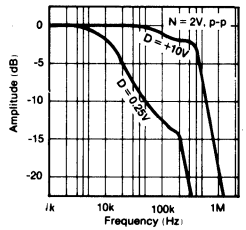
TOTAL ERROR VS OUTPUT CURRENT



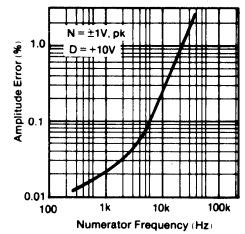
FREQUENCY RESPONSE VS DENOMINATOR VOLTAGE



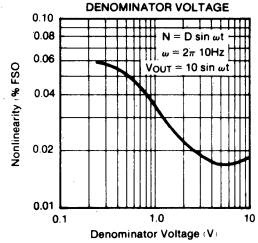
SMALL-SIGNAL FREQUENCY RESPONSE



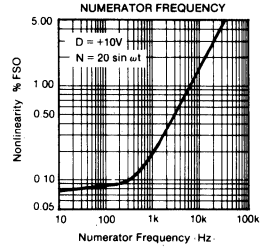
AMPLITUDE ERROR VS NUMERATOR FREQUENCY



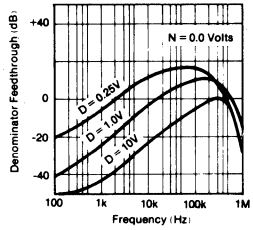
NONLINEARITY VS DENOMINATOR VOLTAGE



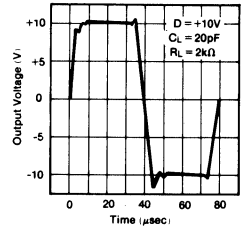
NONLINEARITY VS NUMERATOR FREQUENCY



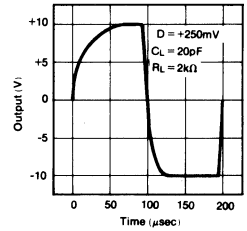
DENOMINATOR FEEDTHROUGH VS DENOMINATOR FREQUENCY



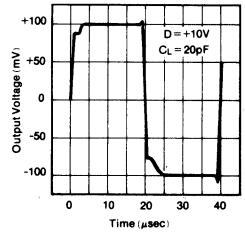
LARGE SIGNAL STEP RESPONSE



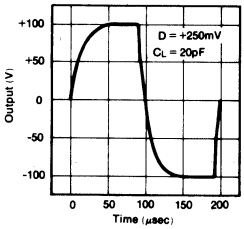
LARGE SIGNAL STEP RESPONSE



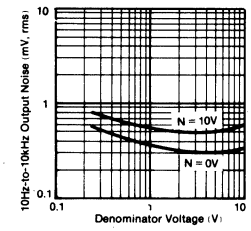
TRANSIENT RESPONSE



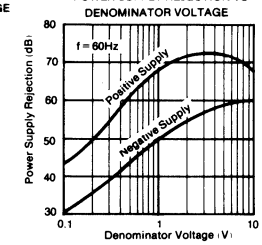
TRANSIENT RESPONSE



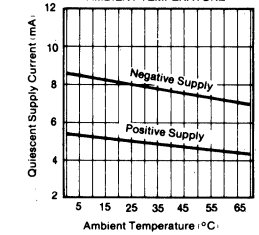
OUTPUT NOISE VS DENOMINATOR VOLTAGE



POWER SUPPLY REJECTION VS DENOMINATOR VOLTAGE

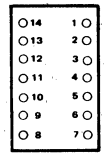


QUIESCENT CURRENT VS AMBIENT TEMPERATURE



PIN CONFIGURATION

1. Gain Error Adjust
2. Output
3. -VCC
4. D Input Offset Adjust
5. Internally Connected to Pin 1
6. Internally Connected to Pin 14
7. Internally Connected to Pin 8
8. Reference Voltage
9. Denominator (D) Input
10. Common
11. N Input Offset Adjust
12. Output Offset Adjust
13. Numerator (N) Input
14. +VCC



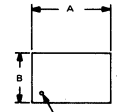
(Bottom View)

MECHANICAL

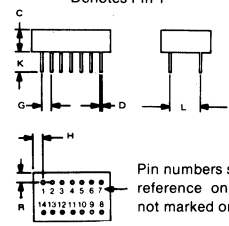
ORDER NUMBER: DIV100HP, DIV100JP, DIV100KP

CASE: Epoxy
WEIGHT: 2.7 Grams
CONNECTOR: 0145MC

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



Pin numbers shown for reference only. Numbers are not marked on package.

DEFINITIONS

TRANSFER FUNCTION

The ideal transfer function for the DIV100 is:

$V_{out} = 10\ N/D$

where: N = Numerator input voltage
D = Denominator input voltage
10 = Internal scale factor

Figure 1 shows the operating region over the specified numerator and denominator ranges. Note that below the minimum denominator voltage (250mV) operation is undefined.

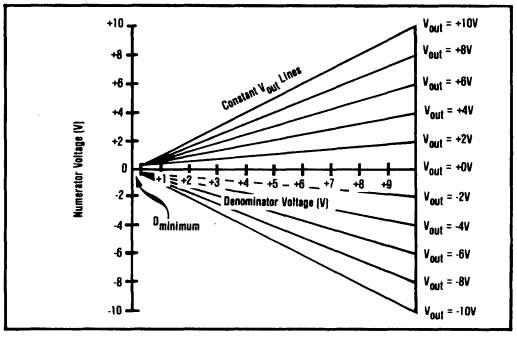


FIGURE 1. Operating Region.

ACCURACY

Accuracy is specified as a percentage of full-scale output (FSO). It is derived from the total error specification.

TOTAL ERROR

Total error is the deviation of the actual output from the ideal quotient 10N/D expressed in percent of FSO(10V); e.g., for the DIV100K:

$V_{out\ (actual)} = V_{out\ (ideal)} \pm$ total error,

where: Total error = 0.25% FSO = 25mV.

It represents the sum of all error terms normally associated with a divider: numerator nonlinearity, denomimator nonlinearity, scale-factor error, output-referred numerator and denominator offsets, and the offset due to the output amplifier. Individual errors are not specified because it is their sum that affects the user's application.

SMALL-SIGNAL BANDWIDTH

Small-signal bandwidth is the frequency the output drops to 70% (-3dB) of its DC value. The input signal must be low enough in amplitude to keep the divider's output from becoming slew-rate limited. A rule-of-thumb is to make the output voltage 100mV, p-p, when testing this parameter. Small-signal bandwidth is directly proportional to denominator magnitude as described in the Typical Performance Curves.

0.5% AMPLITUDE ERROR

At high frequencies the input-to-output relationship is a complex function that produces both a magnitude and vector error. The 0.5% amplitude error is the frequency at which the magnitude of the output drops 0.5% from its DC value.

0.57° VECTOR ERROR

The 0.57° vector error is the frequency at which a phase error of 0.01 radians occurs. This is the most sensitive measure of dynamic error of a divider.

LINEARITY

Defining linearity for a nonlinear device may seem unnecessary; however, by keeping one input constant the output becomes a linear function of the remaining input. The denominator is the input that is held fixed with a divider. Nonlinearities in a divider add harmonic distortion to the output in the amount of:

$$\text{Percent Distortion} \approx \frac{\text{Percent Nonlinearity}}{\sqrt{2}}$$

FEEDTHROUGH

Feedthrough is the signal at the output for any value of denominator within its rated range, when the numerator input is zero. Ideally the output should be zero under this condition.

GENERAL INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the DIV100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 1000pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the DIV100's output.

OVERLOAD PROTECTION

The DIV100 can be protected against accidental power supply reversal by putting a diode(1N4001, type) in series with each power supply line as shown in Figure 2. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off.

If this protection circuit is used, the accuracy of the DIV100 will be degraded by the power supply sensitivity specification. No other overload protection circuit is necessary. Inputs are internally protected against overvoltages and they are current-limited by at least a 10kΩ series resistor. The output is protected against short circuits to power supply common only.

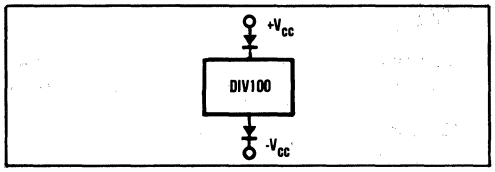


FIGURE 2. Overload Protection Circuit.

STATIC SENSITIVITY

No special handling is required. The DIV100 does not use MOS-type transistors. Furthermore, all external leads are protected by resistors against low energy electrostatic discharge (ESD).

INTERNAL POWER DISSIPATION

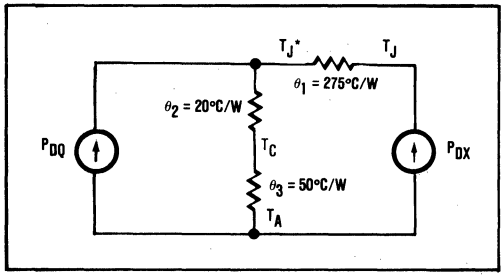


FIGURE 3. DIV100 Thermal Model.

Figure 3 is the thermal model for the DIV100 where:

P_{DQ} = Quiescent Power Dissipation
= $|+V_{CC}| I_{+QUIESCENT} + |-V_{CC}| I_{-QUIESCENT}$

P_{DX} = Worst case power dissipation in the output transistor
= $V_{CC}^2/4R_{LOAD}$ (for normal operation)
= $V_{CC} I_{(output\ limit)}$ (for short-circuit)

T_J = Junction Temperature (output loaded)
T_J* = Junction Temperature (no load)
T_C = Case Temperature
T_A = Ambient Temperature
θ = Thermal Resistance

This model is obviously not the simple one power source model that most linear device manufacturers give. It is, however, a more accurate model for a multidevice monolithic or hybrid integrated circuit.

The model in Figure 3 must be used in conjunction with the DIV100's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem:

Determine the highest ambient temperature at which the DIV100 may be operated with a continuous short circuit to ground. $V_{CC} = \pm 15VDC$.

$P_{D(max)} = 600mW$. $T_{J(max)} = +175°C$.

$T_A = T_{J(max)} - P_{DQ}(\theta_2 + \theta_3) - P_{DX(short=circuit)}(\theta_1+\theta_2+\theta_3)$
$= 175°C - 18°C - 119°C = 38°C$

$P_{D(actual)} = P_{DQ} + P_{DX(short=circuit)} \leq P_{D(max)}$
$= 255mW + 345mW = 600mW$

The conclusion is that the device will withstand a short-circuit up to $T_A = +38°C$ without exceeding either the 175°C or 600mW absolute maximum limits.

LIMITING OUTPUT VOLTAGE SWING

The negative output voltage swing should be limited to ±11V, maximum, to prevent polarity inversion and possible system instability. This should be done by limiting the input voltage range.

THEORY OF OPERATION

The DIV100 is a log-antilog divider consisting of four operational amplifiers and four logging transistors integrated into a single monolithic circuit. Its basic principal of operation can be seen by an analysis of the circuit in Figure 4.

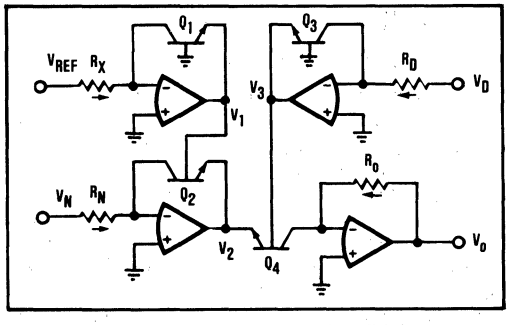


FIGURE 4. One-Quadrant Log-Antilog Divider.

The logarithmic equation for a biopolar transistor is:

$$V_{BE} = V_T \ln (I_c/I_s), \quad (1)$$

where: $V_T = kT/q$
k = Boltzmann's constant = 1.381×10^{-23}
T = Absolute temperature in degrees Kelvin
q = Electron charge = 1.602×10^{-19}
I_c = Collector current
I_s = Reverse saturation current

Applying equation (1) to the four logging transistors gives:

For Q_1:
$V_{BE} = V_B - V_E = V_T[\ln(V_{REF}/R_X - \ln I_s]$

This leads to:
$V_1 = -V_T[\ln(V_{REF}/R_X - \ln I_s]$

For Q_2:
$V_1 - V_2 = V_T[\ln(V_N/R_N) - \ln I_S]$

For Q_3:
$V_3 = -V_T[\ln (V_D/R_D) - \ln I_S]$

We have now taken the logarithms of the input voltage V_{REF}, V_N, and V_D. Applying equation (1) to Q_4 gives:
$V_3 - V_2 = V_T [\ln (V_o/R_o) - \ln I_s]$.

Assume V_T and I_s are the same for all four transistors (a reasonable assumption with a monolithic IC). Solving

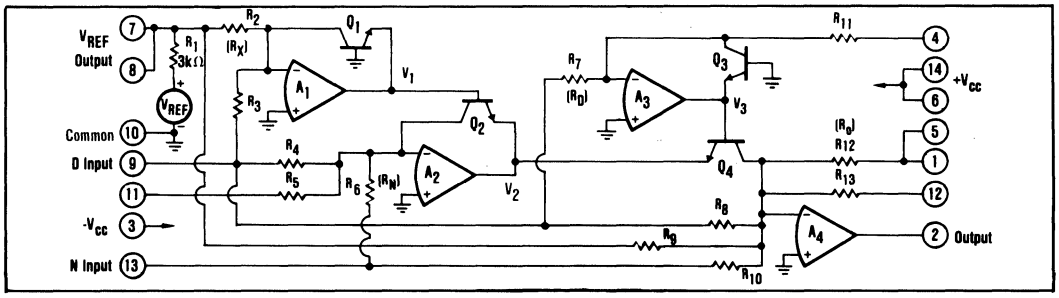


FIGURE 5. DIV100 Two-Quadrant Log-Antilog Circuit.

this last equation in terms of the previously defined variables and taking the antilogarithm of the result yields:

$$V_o = \frac{V_{REF}\, V_N\, R_o\, R_D}{V_D\, R_X\, R_N} \qquad (2)$$

In the DIV100 $V_{REF} = 6.6V$, $R_o = R_X = R_D$, and R_X is such that the transfer function is:

$$V_o = 10\ N\ D \qquad (3)$$

where: N = Numerator Voltage
D = Denominator Voltage

Figure 5 is a more detailed circuit diagram for the DIV100. In addition to the circuitry included in Figure 3, it also shows the resistors (R_3, R_4, R_8, R_9, and R_{10}) used for level-shifting. This converts the DIV100 to a two-quadrant divider.

The implementation of the transfer function is equation (3) is done using devices with real limitations. For example, the value of the D input must always be positive. If it isn't, Q_3 will no longer conduct, A_3 will become open loop, and its output and the DIV100 output will saturate. This limitation is further restricted in that if the D input is less than +250mV the errors will become substantial. It will still function, but its accuracy will be less.

Still another limitation is the value of the N input must always be equal to or less than the absolute value of the D input. From equation (3) it can be seen that if this limitation is not met V_o will try to be greater than the 10V output voltage limit of A_4.

A limitation that may not be obvious is the effect of source resistance. If the numerator or denominator inputs are driven from a source with more than 10Ω of output resistance, the resultant voltage divider will cause a significant output error. This voltage divider is formed by the source resistance and the DIV100 input resistance. With $R_{SOURCE} = 10\Omega$ and $R_{INPUT\ (DIV100)} = 25k\Omega$ an error of 0.04% results. This means that the best performance of the DIV100 is obtained by driving its inputs from operational amplifiers.

Note that the reference voltage is brought out to pins 7 and 8. This gives the user a precision, temperature-compensated reference for external use. Its open-circuit voltage is +6.6VDC, ±0.075V, typically. Its Thevenin equivalent resistance is 3kΩ. Since the output resistance is a relatively high value, an operational amplifier is necessary to buffer this source as shown in Figure 6. The external amplifier is necessary because current drawn through the 3kΩ resistor will effect the DIV100 scale factor.

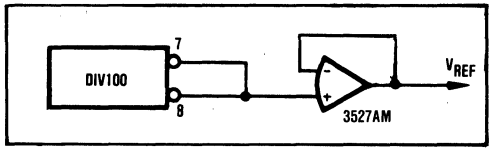


FIGURE 6. Buffered Precision Voltage Reference.

OPTIONAL ADJUSTMENTS

Figure 7 shows the connections to make to adjust the DIV100 for significantly better accuracy over its 40-to-1 denominator range.

The adjustment procedure is:

1. Begin with R_1, R_2, and R_3 set to their mid-position.
2. With N = D = 10.000V, ±1mV, adjust R_1 for V_o = +10.000V, ±1mV. This sets the scale factor.
3. Set D to the minimum expected denominator voltage. With N = D, adjust R_2 for V_o = -10.000V. This adjusts the output referred denominator offset errors.
4. With D still at its minimum expected value make N = +D. Adjust R_3 for V_o = 10.000V. This adjusts the output referrred numerator offset errors.
5. Repeat steps 2 - 4 until the best accuracy is obtained.

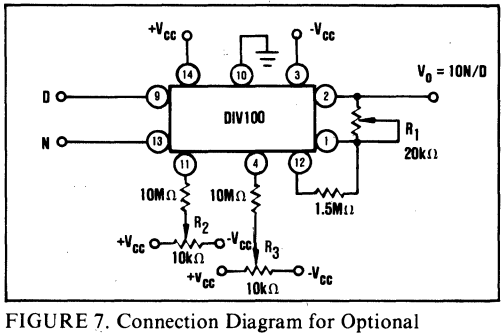


FIGURE 7. Connection Diagram for Optional Adjustments.

TYPICAL APPLICATIONS

CONNECTION DIAGRAM

Figure 8 is applicable to each application discussed in this section, except the square root mode.

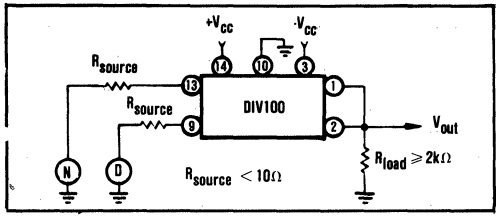


FIGURE 8. Connection Diagram - Divide Mode.

RATIOMETRIC MEASUREMENT

The DIV100 is useful for ratiometric measurements such as efficiency, elasticity, stress, strain, percent distortion, impedance magnitude, and fractional loss or gain. These ratios may be made for instantaneous, average, RMS, or peak values.

The advantage of using the DIV100 can be illustrated from the example shown in Figure 9.

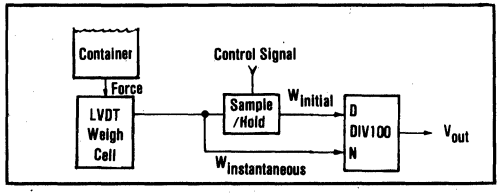


FIGURE 9. Weighing System - Fractional Loss.

The LVDT (Linear Variable Differential Transformer) weigh cell measures the force exerted on it by the weight of the material in the container. Its output is a voltage proportional to:

$$W = \frac{Fg}{a}$$

where: W = Weight of material
F = Force
g = Acceleration due to gravity
a = Acceleration (acting on body of weight W)

In a fractional loss weighing system the initial value of the material can be determined by the volume of the container and the density of the material. If this value is then held on the D-input to the DIV100 for some time interval, the DIV100 output will be a measure of the instantaneous fractional loss:

$$\text{Loss (L)} = W_{INSTANTANEOUS} / W_{INITIAL}$$

Note that by using the DIV100 in this application the common physical parameters of g and a have been eliminated from the measurement, thus eliminating the need for precise system calibration.

The output from a ratiometric measuring system may also be used as a feedback signal in an adaptive process control system. A common application in the chemical industry is in the ratio control of a gas and liquid flow as illustrated in Figure 10.

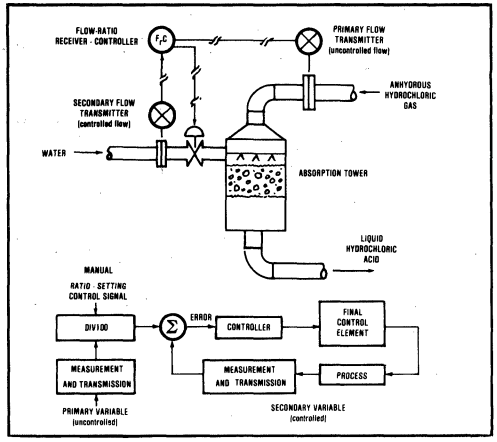


FIGURE 10. Ratio Control of Water to Hydrochloric Gas

PERCENTAGE COMPUTATION

A variation of the direct ratiometric measurements previously discussed is the need for percentage computation. In Figure 11 the DIV100 output varies as the percent deviation of the measured variable to the standard.

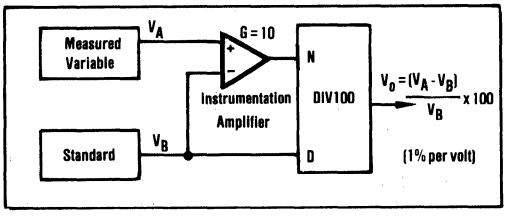


FIGURE 11. Percentage Computation.

TIME AVERAGING

The circuit in Figure 12 overcomes the fixed averaging interval and crude approximation of more conventional time averaging schemes.

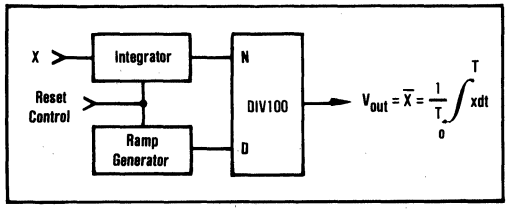


FIGURE 12. Time Averaging Computation Circuit.

BRIDGE LINEARIZATION

The bridge circuit in Figure 13 is fundamental to pressure, force, strain and electrical measurements. It can have one or more active arms whose resistance is a function of the physical quantity, property, or condition that is being measured; e.g., force of compression. For the sake of explanation the bridge in Figure 13 has only one active arm.

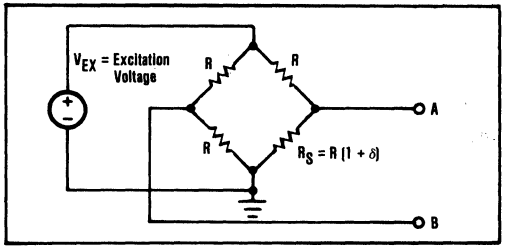


FIGURE 13. Bridge Circuit.

The differential output voltage V_{BA} is:

$$V_{BA} = V_B - V_A \quad \frac{-V_{EX}\delta}{2(2+\delta)},$$

a nonlinear function of the resistance change in the active arm. This nonlinearity limits the useful span of the bridge to perhaps ±10% variation in the measured parameter.

Bridge linearization is accomplished using the circuit in Figure 14. The instrumentation amplifier converts the differential output to a single-ended voltage needed to drive the divider. The voltage-divider string makes the numerator and denominator voltages:

$$N = \frac{-V_{EX}\delta\ R_{iN}}{(2R_1 + 3R_{in})(2+\delta)}, \text{and,}$$

$$D = \frac{2\ V_{EX}\ R_{iD}}{(2R_1 + 3R_{iD})(2+\delta)}, \text{ respectively,}$$

where: R_{iN} = DIV100 numerator input resistance
R_{iD} = DIV100 denominator input resistance

Applying these voltages to the DIV100 transfer function gives:

$$V_o = 10N\ D = \frac{(2R_1 + 3R_{iD})(R_{iN}\delta)\ 10}{(2R_1 + 3R_{iN})(2R_{iD})},$$

which reduces to:

$V_o = -5\delta$

if the divider's input resistances are equal.

The nonlinearity of the bridge has been eliminated and the circuit output is independent of variations in the excitation voltage.

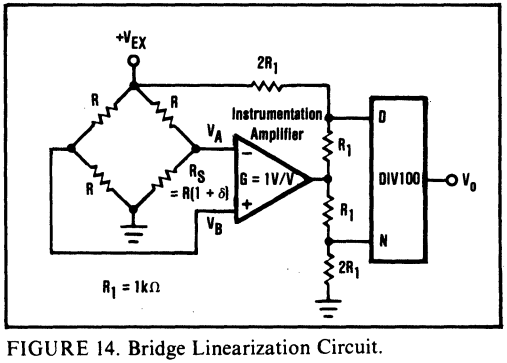


FIGURE 14. Bridge Linearization Circuit.

AUTOMATIC GAIN CONTROL

A simple AGC circuit using the DIV100 is shown in Figure 15. The numerator voltage may vary both positive and negative. The divider's output is half-wave rectified and filtered by D_1, R_3, and C_2. It is then compared to the DC reference voltage. If a difference exists the integrator sends a control signal to the denominator input to maintain a constant output, thus compensating for input voltage changes.

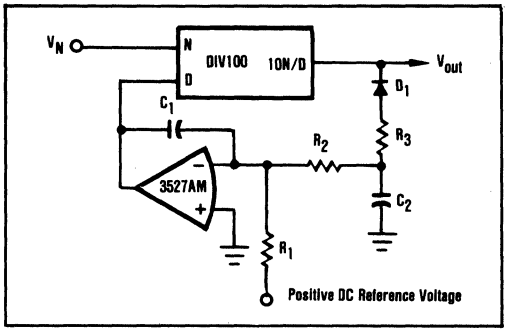


FIGURE 15. Automatic Gain Control Circuit.

VOLTAGE-CONTROLLED FILTER

Figure 16 shows how to use the DIV100 in the feedback loop of an integrator to form a voltage-controlled filter. The transfer function is:

$$\frac{V_{out(S)}}{V_{in(S)}} = \frac{K}{\tau S + 1}$$

where: $K = -R_2/R_1$

$$\tau = \frac{10\ R_2\ C}{V_{CONTROL}}$$

This circuit may be used as a single-pole low-pass active filter whose cutoff frequency is linearily proportional to the circuit's control voltage.

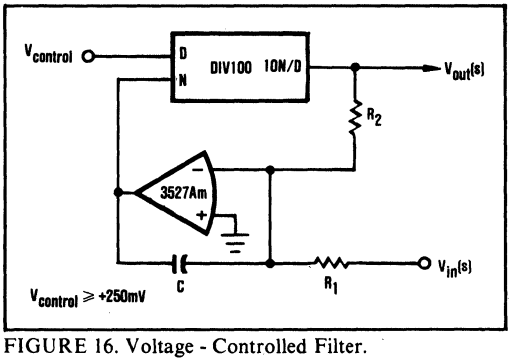


FIGURE 16. Voltage - Controlled Filter.

SQUARE ROOT

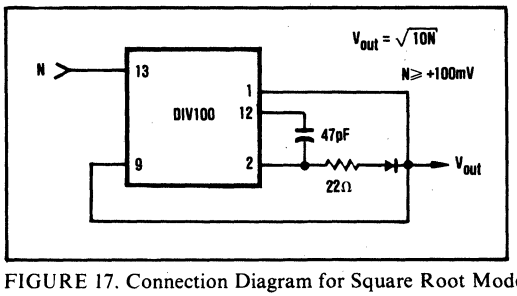


FIGURE 17. Connection Diagram for Square Root Mode.

BURR-BROWN

LOG100

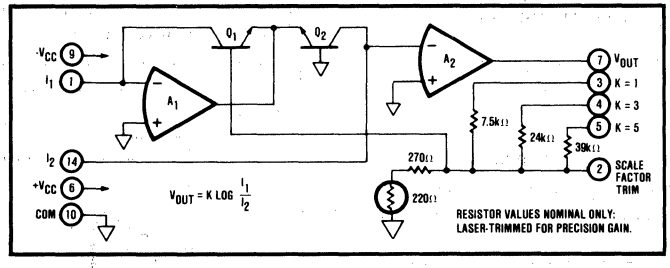
Precision LOGARITHMIC AND LOG RATIO AMPLIFIER

FEATURES

- HIGH ACCURACY
  0.37% FSO max Total Error
  over 5 decades
- GOOD LINEARITY
  0.1% max Log Conformity
  over 5 decades
- EASY TO USE
  Pin-selectable Gains
  Internal Laser-trimmed Resistors
- WIDE INPUT DYNAMIC RANGE
  6 Decades, 1nA to 1mA

APPLICATIONS

- LOG, LOG RATIO AND ANTILOG COMPUTATIONS
- ABSORBANCE MEASUREMENTS
- DATA COMPRESSION
- OPTICAL DENSITY MEASUREMENTS
- DATA LINEARIZATION
- CURRENT AND VOLTAGE INPUTS



DESCRIPTION

The LOG100 uses advanced integrated circuit technologies to achieve high accuracy, ease of use, low cost, and small size. It is the logical choice for your logarithmic-type computations. The amplifier has guaranteed maximum error specifications over the full six-decade input range (1nA to 1mA) and for all possible combinations of I_1 and I_2. Total error is guaranteed so that involved error computations are not necessary.

The circuit uses a specially designed compatible thin-film monolithic integrated circuit which contains amplifiers, logging transistors, and low drift thin-film resistors. The resistors are laser-trimmed for maximum precision. FET input transistors are used for the amplifiers whose low bias currents (1pA typical) permit signal currents as low as 1nA while maintaining guaranteed total errors of 0.37% FSO maximum.

Because scaling resistors are self-contained, scale factors of 1V, 3V or 5V per decade are obtained simply by pin selections. No other resistors are required for log ratio applications. The LOG100 will meet its guaranteed accuracy with no user trimming. Provisions are made for simple adjustments of scale factor, offset voltage, and bias current if enhanced performance is desired.

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ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSFER FUNCTION			V_{OUT} = K Log (I_1/I_2)		
Log Conformity Error(1)	Either I_1 or I_2				
Initial	1nA to 100µA (5 decades)		0.04	0.1	%
	1nA to 1mA (6 decades)		0.15	0.25	%
Over Temperature	1nA to 100µA (5 decades)		0.002		%/°C
	1nA to 1mA (6 decades)		0.001		%/°C
K Range(2)			1, 3, 5		V/decade
Accuracy			0.3		%
Temperature Coefficient			0.03		%/°C
ACCURACY					
Total Error(3)	K = 1,(4) Current Input Operation				
Initial	I_1, I_2 = 1mA			±55	mV
	I_1, I_2 = 100µA			±30	mV
	I_1, I_2 = 10µA			±25	mV
	I_1, I_2 = 1µA			±20	mV
	I_1, I_2 = 100nA			±25	mV
	I_1, I_2 = 10nA			±30	mV
	I_1, I_2 = 1nA			±37	mV
vs Temperature	I_1, I_2 = 1mA		±0.20		mV/°C
	I_1, I_2 = 100µA		±0.37		mV/°C
	I_1, I_2 = 10µA		±0.28		mV/°C
	I_1, I_2 = 1µA		±0.033		mV/°C
	I_1, I_2 = 100nA		±0.28		mV/°C
	I_1, I_2 = 10nA		±0.51		mV/°C
	I_1, I_2 = 1nA		±1.26		mV/°C
vs Supply	I_1, I_2 = 1mA		±4.3		mV/V
	I_1, I_2 = 100µA		±1.5		mV/V
	I_1, I_2 = 10µA		±0.37		mV/V
	I_1, I_2 = 1µA		±0.11		mV/V
	I_1, I_2 = 100nA		±0.61		mV/V
	I_1, I_2 = 10nA		±0.91		mV/V
	I_1, I_2 = 1nA		±2.6		mV/V
INPUT CHARACTERISTICS (of amplifiers A_1 and A_2)					
Offset Voltage					
Initial			±0.7	±5	mV
vs Temperature			±80		µV/°C
Bias Current					
Initial			1	5(5)	pA
vs Temperature			doubles every 10°C		
Voltage Noise	10Hz to 10kHz, RTI		3		µV, rms
Current Noise	10Hz to 10kHz, RTI		0.5		pA, rms
AC PERFORMANCE					
3dB Response(6), I_2 = 10µA					
1nA	C_C = 4500pF		0.11		kHz
1µA	C_C = 150pF		38		kHz
10µA	C_C = 150pF		27		kHz
1mA	C_C = 50pF		45		kHz
Step Response(6)					
Increasing	C_C = 150pF				
1µA to 1mA			11		µsec
100ΩA to 1µA			7		µsec
10nA to 100nA			110		µsec
Decreasing	C_C = 150pF				
1mA to 1µA			45		µsec
1µA to 100nA			20		µsec
100nA to 10nA			550		µsec
OUTPUT CHARACTERISTICS					
Full Scale Output (FSO)		±10			V
Rated Output					
Voltage	I_{OUT} = ±5mA	±10			V
Current	V_{OUT} = ±10V	±5			mA
Current Limit					
Positive			12.5		mA
Negative			15		mA
Impedance			0.05		Ω
POWER SUPPLY REQUIREMENTS					
Rated Voltage			±15		VDC
Operating Range	Derated Performance	±12		±18	VDC
Quiescent Current			±7	±9	mA

ELECTRICAL (CONT'D)

Specifications at T_A = +25°C and $\pm V_{CC}$ = ±15V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AMBIENT TEMPERATURE RANGE					
Specification	Derated Performance	0		+70	°C
Operating Range		-55		+125	°C
Storage		-55		+125	°C

NOTES:
1. Log Conformity Error is the peak deviation from the best-fit straight line of the V_{OUT} vs log I_{IN} curve expressed as a percent of peak-to-peak full scale output.
2. May be trimmed to other values. See Applications section.
3. The worst-case Total Error for any ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.
4. Total Error at other values of K is K times Total Error for K = 1.
5. Guaranteed by design. Not directly measurable due to amplifier's committed configuration.
6. **3dB and transient response are a function of both the compensation capacitor and the level of input current. See Performance Curves.**

ABSOLUTE MAXIMUM RATINGS

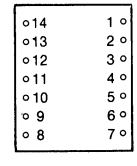
Supply	±18V
Internal Power Dissipation	600mV
Input Current	10mA
Input Voltage Range	±18V
Storage Temperature Range	-55°C to +125°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground
Junction Temperature	175°C

SCALE FACTOR PIN CONNECTIONS

K, V/decade	Connections
5	5 to 7
3	4 to 7
1.9	4 and 5 to 7
1	3 to 7
0.85	3 and 5 to 7
0.77	3 and 4 to 7
0.68	3 and 4 and 5 to 7

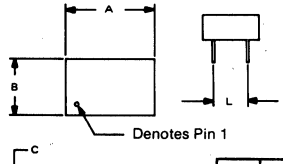
PIN CONFIGURATION

1. I_1 INPUT
2. SCALE FACTOR TRIM
3. K = 1
4. K = 3
5. K = 5
6. $+V_{CC}$
7. OUTPUT
8. NO INTERNAL CONNECTION
9. $-V_{CC}$
10. COMMON
11. NO INTERNAL CONNECTION
12. NO INTERNAL CONNECTION
13. NO INTERNAL CONNECTION
14. I_2 INPUT



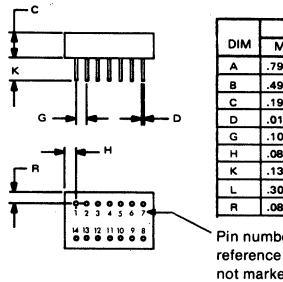
(Bottom View)

MECHANICAL



ORDER NUMBER: LOG100JP
CASE: Epoxy
WEIGHT: 2.7 grams
CONNECTOR: 0145MC

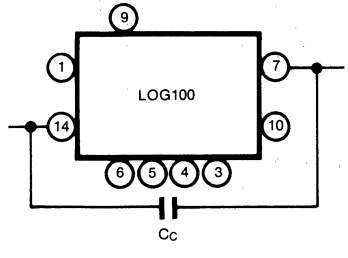
NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

Pin numbers shown for reference only. Numbers are not marked on package.

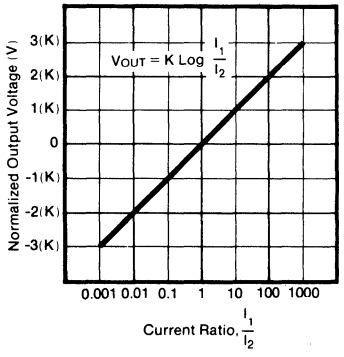
FREQUENCY COMPENSATION



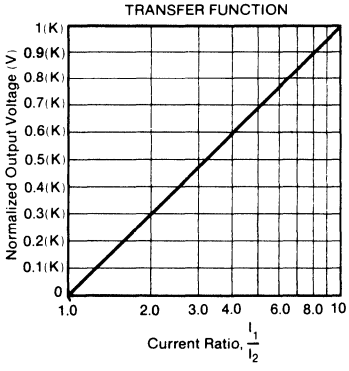
PERFORMANCE CURVES

(Typical at T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.)

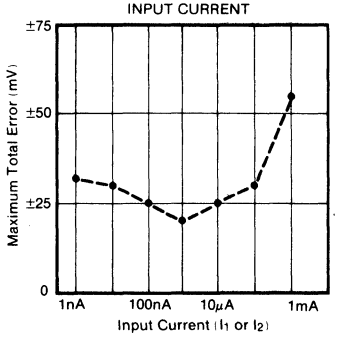
NORMALIZED TRANSFER FUNCTION



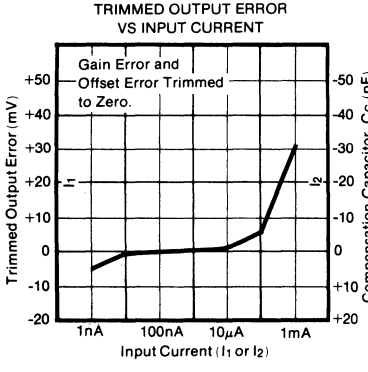
ONE CYCLE OF NORMALIZED TRANSFER FUNCTION



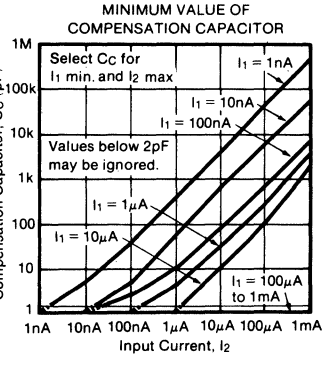
TOTAL ERROR VS INPUT CURRENT



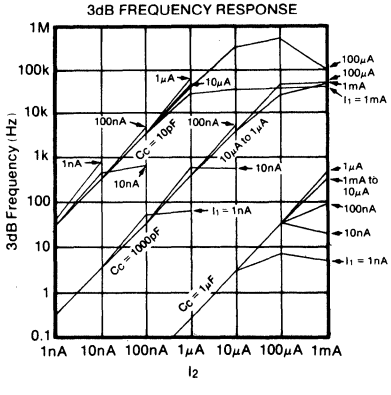
TRIMMED OUTPUT ERROR VS INPUT CURRENT



MINIMUM VALUE OF COMPENSATION CAPACITOR



3dB FREQUENCY RESPONSE



LOG100

THEORY OF OPERATION

The base-emitter voltage of a bipolar transistor is

$$V_{BE} = V_T \ln \frac{I_c}{I_s} \quad \text{where:} \quad V_T = \frac{KT}{q} \tag{1}$$

K = Boltzman's constant = 1.381 x 10^{-23}

T = Absolute temperature in degrees Kelvin

q = Electron charge = 1.602 x 10^{-19} Coulombs

I_c = Collector current

I_s = Reverse saturation current

From the circuit in Figure 1, we see that

$$V_{OUT}' = V_{BE_1} - V_{BE_2} \tag{2}$$

Substituting (1) into (2) yields

$$V_{OUT}' = V_{T_1} \ln \frac{I_1}{I_{s_1}} - V_{T_2} \ln \frac{I_1}{I_{s_2}} \tag{3}$$

If the transistors are matched and isothermal and $V_{T_1} = V_{T_2}$, then (3) becomes

$$V_{OUT}' = V_T \left[\ln \frac{I_1}{I_s} - \ln \frac{I_2}{I_s} \right] \tag{4}$$

$$V_{OUT}' = V_T \ln \frac{I_1}{I_2} \quad \text{and since} \tag{5}$$

$$\ln X = 2.3 \log_{10} X \tag{6}$$

$$V_{OUT}' = n\, V_T \log \frac{I_1}{I_2} \tag{7}$$

where $n = 2.3$ (8)

also

$$V_{OUT} = V_{OUT}' \frac{R_1 + R_2}{R_1} \tag{9}$$

$$= \frac{R_1 + R_2}{R_1} n\, V_T \log \frac{I_1}{I_2} \tag{10}$$

or

$$V_{OUT} = K \log \frac{I_1}{I_2} \tag{11}$$

It should be noted that the temperature dependance associated with $V_T = KT/q$ is compensated by making R_1 a temperature sensitive resistor with the required positive temperature coefficient.

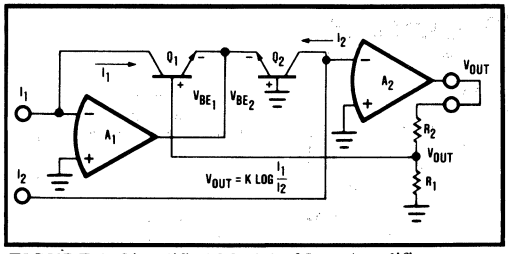


FIGURE 1. Simplified Model of Log Amplifier.

DEFINITION OF TERMS

TRANSFER FUNCTION

The ideal transfer function is $V_{OUT} = K \log \frac{I_1}{I_2}$

where

K = the scale factor with units of volts/decade

I_1 = numerator input current

I_2 = denominator input current.

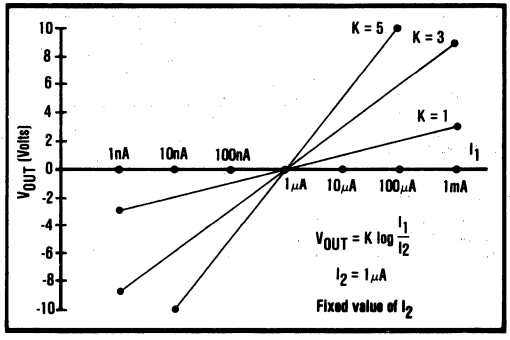


FIGURE 2. Transfer Function with Varying K and I_1.

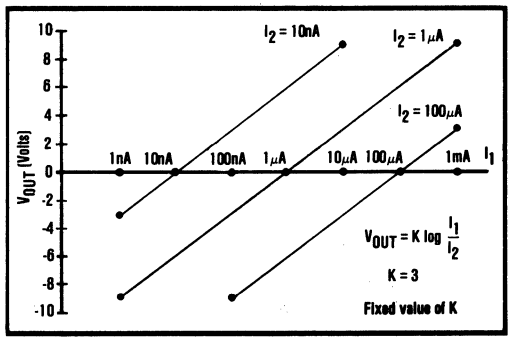


FIGURE 3. Transfer Function with Varying I_2 and I_1.

ACCURACY

Accuracy considerations for a log ratio amplifier are somewhat more complicated than for other amplifiers. The reason is that the transfer function is nonlinear and has two inputs, each of which can vary over a wide dynamic range. The accuracy for any combination of inputs is determined from the total error specification.

TOTAL ERROR

The total error is the deviation (expressed in mV) of the actual output from the ideal output of $V_{OUT} = K \log (I_1/I_2)$. Thus,

$V_{OUT\ (ACTUAL)} = V_{OUT\ (IDEAL)} \pm$ Total Error.

It represents the sum of all the individual components of error normally associated with the log amp when operated in the current input mode. The worst-case error for any given ratio of I_1/I_2 is the largest of the two errors when I_1 and I_2 are considered separately.

Example

I_1 varies over a range of 10nA to 1μA and I_2 varies from 100nA to 10μA. What is the maximum error?

Table I shows the maximum errors for each decade combination of I_1 and I_2.

TABLE I. I_1/I_2 and Maximum Errors.

I_2 (max error)* \ I_1 (max error)*	10nA (30mV)	100nA (25mV)	1μA (20mV)
100nA (25mV)	0.1 (30mV)	1 (25mV)	10 (25mV)
1μA (20mV)	0.01 (30mV)	0.1 (25mV)	1 (20mV)
10μA (25mV)	0.001 (30mV)	0.01 (25mV)	0.1 (25mV)

*Maximum errors are in parenthesis.

Since the largest value of I_1/I_2 is 10 and the smallest is 0.001, K is set at 3V per decade so the output will range from +3V to -9V. The maximum total error occurs when I_1 = 10nA and is equal to K x 30mV. This represents a 0.75% of peak-to-peak FSO error $\frac{(3 \times 0.030)}{12} \times 100\% =$ 0.75% where the full scale output is 12V (from +3V to -9V).

ERRORS RTO AND RTI

As with any transfer function, errors generated by the function itself may be Referred-to-Output (RTO) or Referred-to-Input (RTI). In this respect log amps have a unique property:

Given some error voltage at the log amp's output, that error corresponds to a constant percent of the input regardless of the actual input level.

Refer to: Yu Jen Wong and William E. Ott, "Function Circuits: Design & Applications", McGraw-Hill Book, 1976.

LOG CONFORMITY

Log conformity corresponds to linearity when V_{OUT} is plotted versus I_1/I_2 on a semilog scale. In many applications log conformity is the most important specification. This is true because bias current errors are negligible (1pA compared to input currents of 1nA and above) and the scale factor and offset errors may be trimmed to zero or removed by system calibration. This leaves log conformity as the major source of error.

Log conformity error is defined as the peak deviation from the best-fit straight line of the V_{OUT} versus log (I_1/I_2) curve. This is expressed as a percent of peak-to-peak full scale output. Thus, the nonlinearity error expressed in volts over m decades is

$$V_{OUT\ (NONLIN.)} = K\ 2Nm \text{ volts} \quad (12)$$

where N is the log conformity error, in percent.

INDIVIDUAL ERROR COMPONENTS

The ideal transfer function with current input is

$$V_{OUT} = K \text{ Log } \frac{I_1}{I_2} \quad (13)$$

The actual transfer function with the major components of error is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{I_1 - I_{B_1}}{I_2 - I_{B_2}} \pm K\ 2Nm \pm V_{OS\ OUT} \quad (14)$$

The individual component of error is

ΔK = scale factor error (0.3%, typ)

I_{B_1} = bias current of A_1 (1pA, typ)

I_{B_2} = bias current of A_2 (1pA, typ)

N = log conformity error (0.05%, 0.1%, typ)

$V_{OS\ OUT}$ = output offset voltage (1mV, typ)

m = no. of decades over which N is specified: 0.05% for m = 5, 0.1% for m = 6

Example: what is the error with K = 3 when

$I_1 = 1\mu A$ and $I_2 = 100nA$

$$V_{OUT} = 3(1 \pm 0.003) \log \frac{10^{-6} - 10^{-12}}{10^{-7} - 10^{-12}} \pm 3(2)(0.0005)\ 5 \pm 1mV \quad (15)$$

$$\approx 3.009 \log \frac{10^{-6}}{10^{-7}} + 0.015 + 0.001 \quad (16)$$

$$= 3.009\ (1) + 0.015 + 0.001 \quad (17)$$

$$= 3.025 \text{ volts} \quad (18)$$

Since the ideal output is 3.000V the error as a percent of reading is

$$\%\ \text{error} = \frac{0.025}{3} \times 100\% = 0.83\% \quad (19)$$

For the case of voltage inputs, the actual transfer function is

$$V_{OUT} = K(1 \pm \Delta K) \log \frac{\frac{V_1}{R_1} - I_{B_1} \pm \frac{E_{OS_1}}{R_1}}{\frac{V_2}{R_2} - I_{B_2} \pm \frac{E_{OS_2}}{R_2}} \pm K\ 2Nm \pm V_{OS\ OUT} \quad (20)$$

FREQUENCY RESPONSE

The 3dB frequency response of the LOG100 is a function of the magnitude of the input current levels and of the value of the frequency compensation capacitor. See Performance Curves for details.

The frequency response curves are shown for constant DC I_1 and I_2 with a small signal AC current on one of them.

The transient response of the LOG100 is different for increasing and decreasing signals. This is due to the fact that a log amp is a nonlinear gain element and has different gains at different levels of input signals. Frequency response decreases as the gain increases.

GENERAL INFORMATION

INPUT CURRENT RANGE

The stated input range of 1nA to 1mA is the range for specified accuracy. Smaller or larger input currents may be applied with decreased accuracy. Currents larger than 1mA result in increased nonlinearity. The 10mA absolute maximum is a conservative value to limit the power dissipation in the output stage of A_1 and the logging transistor. Currents below 1nA will result in increased errors due to the input bias currents of A_1 and A_2 (1pA typical). These errors may be nulled. See Optional Adjustments section.

FREQUENCY COMPENSATION

Frequency compensation for the LOG100 is obtained by connecting a capacitor between pins 7 and 14. The size of the capacitor is a function of the input currents as shown in the Performance Curves. For any given application the smallest value of the capacitor which may be used is determined by the maximum value at I_2 and the minimum value of I_1. Larger values of C_C will make the LOG100 more stable, but will reduce the frequency response.

SETTING THE REFERENCE CURRENT

When the LOG100 is used as a straight log amplifier I_2 is constant and becomes the reference current in the expression

$$V_{OUT} = K \log \frac{I_1}{I_{REF}}. \quad (21)$$

I_{REF} can be derived from an external current source (such as shown in Figure 4) or it may be derived from a voltage source with one or more resistors.

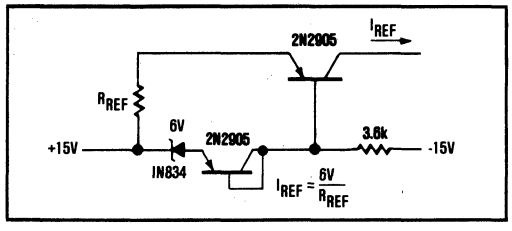


FIGURE 4. Temperature-Compensated Current Reference.

When a single resistor is used the value may be quite large when I_{REF} is small. If I_{REF} is 10nA and +15V is used

$$R_{REF} = \frac{15V}{10\,nA} = 1500M\Omega.$$

A voltage divider may be used to reduce the value of the resistor. When this is done one must be aware of possible errors caused by the amplifier's input offset voltage. This is shown in Figure 5.

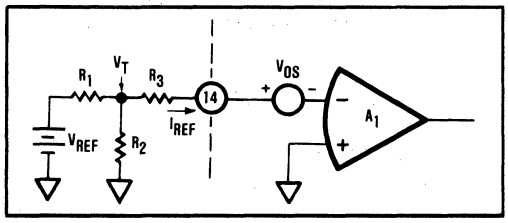


FIGURE 5. "T" Network for Reference Current.

In this case the voltage at pin 14 is not exactly zero, but is equal to the value of the input offset voltage of A_2 which ranges from zero to ±5mV. V_T must be kept much larger than 5mV in order to make this effect negligible. This concept also applies to pin 1.

OPTIONAL ADJUSTMENTS

The LOG100 will meet its specified accuracy with no user adjustments. If improved performance is desired the following optional adjustments may be made.

INPUT BIAS CURRENT

The circuit in Figure 6 may be used to compensate for the input bias currents of A_1 and A_2. Since the amplifiers have FET inputs with the characteristic bias current doubling every 10°C this nulling technique is practical only where the temperature is fairly stable.

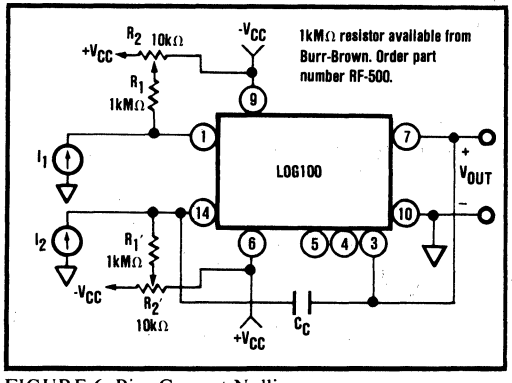


FIGURE 6. Bias Current Nulling.

OUTPUT OFFSET

The output offset may be nulled with the circuit in Figure 7. I_1 and I_2 are set equal at some convenient value in the range of 100nA to 100μA. R_1 is then adjusted for zero output voltage.

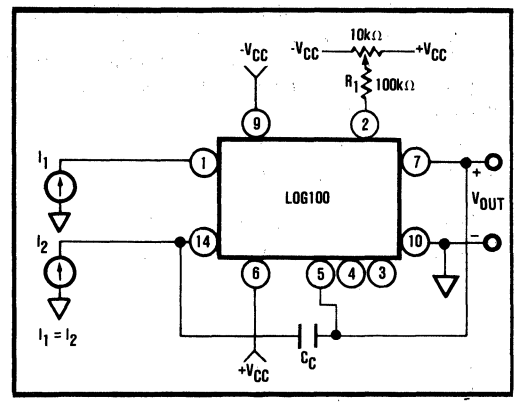


FIGURE 7. Output Offset Nulling.

ADJUSTMENTS OF SCALE FACTOR K

The value of K may be changed by increasing or decreasing the voltage divider resistor normally connected to the output, pin 7. To increase K put resistance in series between pin 7 and the appropriate scaling resistor pin (3, 4 or 5). To decrease K place a parallel resistor between pin 2 and either pin 3, 4 or 5.

APPLICATION INFORMATION

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins to the power supply common. The connection of these capacitors should be as close to the LOG100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 100pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the LOG100's output. This resistor will, of course, form a voltage divider with other resistive loads.

CIRCUIT PROTECTION

The LOG100 can be protected against accidental power supply reversal by putting a diode (1N4001 type) in series with each power supply line as shown in Figure 8. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off. If this protection circuit is used, the accuracy of the LOG100 will be degraded slightly by the voltage drops across the diodes as determined by the power supply sensitivity specification.

The LOG100 uses small geometry FET transistors to achieve the low input bias currents. Normal FET handling techniques should be used to avoid damage caused by low energy electrostatic discharge (ESD).

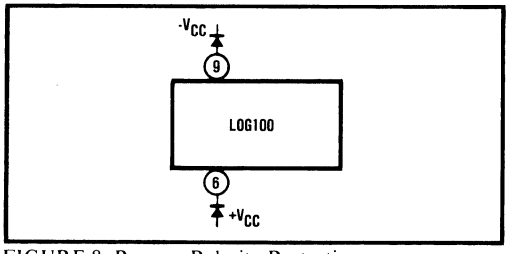


FIGURE 8. Reverse Polarity Protection.

LOG RATIO

One of the more common uses of log ratio amplifiers is to measure absorbance. A typical application is shown in Figure 9.

Absorbance of the sample is: $A = \log \frac{\lambda_2'}{\lambda_1}$ (22)

If $\lambda_2 = \lambda_1$ and D_1 and D_2 are matched $A \propto K \log \frac{I_1}{I_2}$. (23)

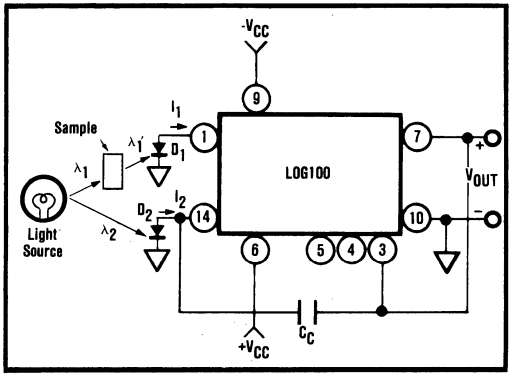


FIGURE 9. Absorbance Measurement.

DATA COMPRESSION

In many applications the compressive effects of the logarithmic transfer function is useful. For example, a LOG100 preceding an 8-bit analog-to-digital converter can replace a more expensive 20-bit converter.

SELECTING OPTIMUM VALUES OF I_2 AND K

In straight log applications (as opposed to log ratio) both K and I_2 are selected by the designer. In order to minimize errors due to output offset and noise it is normally best to scale the log amp to use as much of the ±10V output range as possible. Thus, with the range of I_1 from $I_{1\,MIN}$ to $I_{1\,MAX}$;

For $I_{1\,MAX}$ $+10V = K \log I_{1\,MAX}/I_2$ (24)

For $I_{1\,MIN}$ $-10V = K \log I_{1\,MIN}/I_2$ (25)

Addition of these two equations and solving for I_2 shows that its optimum value, $I_{2\,OPT}$, is the geometric mean of $I_{1\,MAX}$ and $I_{1\,MIN}$.

$$I_{2\,OPT} = \sqrt{I_{1\,MAX} \times I_{1\,MIN}} \quad (26)$$

$$K_{OPT} = \frac{10}{\log \frac{I_{1\,MAX}}{I_{2\,OPT}}} \quad (27)$$

Since K is selectable in discrete steps, use the largest value of K available which does not exceed K_{OPT}.

NEGATIVE INPUT CURRENTS

The LOG100 will function only with positive input currents (conventional current flow into pins 1 and 14). Some current sources (such as photomultiplier tubes) provide negative input currents. In such situations the circuit in Figure 10 may be used.*

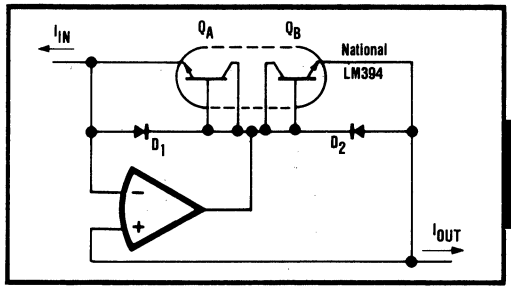


FIGURE 10. Current Inverter.

VOLTAGE INPUTS

The LOG100 gives the best performance with current inputs. Voltage inputs may be handled directly with series resistors, but the dynamic input range is limited to approximately three decades of input voltage by voltage noise and offsets. The transfer function of equation (20) applies to this configuration.

ANTILOG CONFIGURATION (an implicit technique)

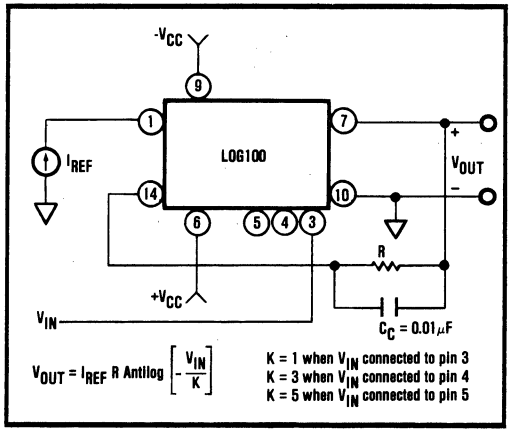


FIGURE 11. Connections for Antilog Function.

BURR-BROWN®

4023/25

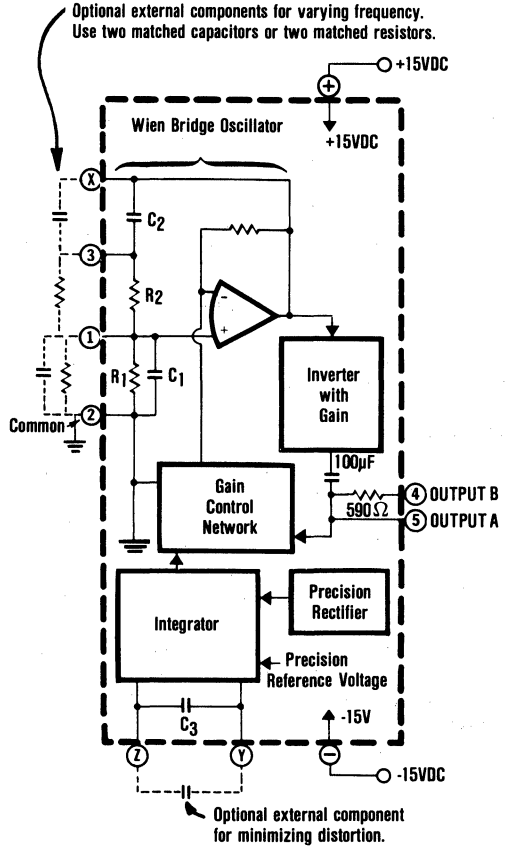
PRECISION OSCILLATOR

FEATURES

- FIXED FREQUENCY - 10Hz to 20kHz
- STABLE AMPLITUDE
- SINE WAVE OUTPUT
- LOW DISTORTION

DESCRIPTION

Model 4023/25 is an all solid-state, ultra-stable sine-wave oscillator. Both output amplitude and frequency are constant, and the stability of both with time and temperature variations is excellent. Internal high-performance Burr-Brown IC operational amplifiers are used to form a Wien bridge oscillator circuit and to regulate the output amplitude. The frequency of oscillation is within ±1% of the customer-specified value. If desired, external components may be added to trim the frequency to an exact value. Adding two external resistors will raise the output frequency and adding two external capacitors will lower the output frequency. With its small size, low distortion, and excellent frequency and amplitude stability, the Model 4023/25 is ideal for use as a reference oscillator in airborne or mobile equipment, special-purpose test equipment, and in telemetry systems. To order, specify Model 4023/25 and frequency.



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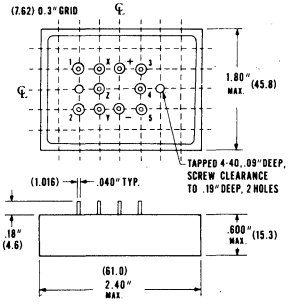
ELECTRICAL SPECIFICATIONS

Typical performance at 25°C and with rated supply unless otherwise noted.

FREQUENCY	
Range (1)	Customer specified, may be any value from 10 Hz to 20 kHz.
Accuracy	±1%, (May be trimmed by the user to less than ±1%)
Stability vs. Temperature	0.04%/°C (max.)
OUTPUT (3)	
Amplitude - Output A	6 Vrms
- Output B	3 Vrms (with 600 Ω load)
Amplitude Accuracy	±2%
Impedance - Output A	1 Ω
- Output B	600 Ω
Rated Load - Output A	1.2 kΩ
- Output B	600 Ω
Distortion (max.)	0.1%
AMPLITUDE STABILITY	
vs. Temperature (max.)	0.02%/°C
Noise and Jitter (max.)	0.02%
Long Term (max.)	0.1%
TEMPERATURE RANGE	
Operating, Rated Specifications	-25°C to +85°C
Storage	-55°C to +100°C
POWER REQUIREMENTS	
Rated Supply	±15 Vdc
Voltage Range at 25°C (2)	±12 Vdc to ±18 Vdc
Supply Drain (max.)	±40 mA

(1) To order, specify Model 4023/25 and frequency.
(2) The positive and negative supplies must be balanced within 2% of each other.
(3) The output may be taken from either Output A or Output B (not both).

MECHANICAL SPECIFICATIONS



Dimensions in millimeters are shown in parentheses.

Weight: 4 oz. maximum (120 grams)

Mating Connector: 1500MC (Optional)

OPERATING INSTRUCTIONS

With $R_1 = R_2$ and $C_1 = C_2$, the Wien-Bridge oscillator will provide a sine-wave oscillation of frequency:

$f_o = 1/2\pi RC$, where $R = R_1 = R_2$ and $C = C_1 = C_2$.

The frequency of oscillation, f_o, will be within ±1% of the nominal value specified by the customer. The frequency may be lowered by externally paralleling the internal capacitors C_1 and C_2; and the frequency may be raised by paralleling the internal resistors R_1 and R_2. The nominal values of C_1 and C_2 will be as follows:

Frequency f_o	C_1 and C_2
10Hz to 100Hz	0.1μF
101Hz to 1000Hz	0.01μF
1001Hz to 20kHz	0.001μF

It is important to pad both R_1 and R_2 or C_1 and C_2 by an equal amount to keep distortion within specifications.

If the frequency is lowered by a significant amount, it may be necessary to externally parallel the integrator capacitor C_3 to lower distortion of the output.

The range of frequency adjustment is approximately 2 decades (within 10kHz and 20kHz). For example, a 10Hz unit may be trimmed for a frequency of up to 1kHz or a 10kHz unit may be varied down to 100Hz. However, the distortion and amplitude stability specifications are guaranteed and tested only for the nominal frequency of oscillation. In general, the degradation in distortion and amplitude stability as the frequency is varied over a wide range is very small.

INSTALLATION

The Model 4023/25 is designed for installation on a flat mounting surface such as a chassis or printed circuit board. The gold-flashed pins may be hand or dip soldered; for plug-in installation, the Model 1500MC mating connector may be installed on the chassis. The unit may be secured to the mounting surface by means of two 4-40 machine screws inserted through the mounting surface not more than 3/16" into the tapped holes in the bottom.

Pin 1 and pin 3 must be shielded from external sources of electrical noise. The module is particularly sensitive to periodic noise near the resonant frequency. Also, if external bridge components are added to the Wien bridge terminals they must be physically near the 4023/25 module.

EXTERNAL CONNECTIONS

External connections are made to the gold-flashed pins on the unit. These connections include the Wien bridge, integrator feedback, output, and power supply termination and are made as follows:

Pin 1 Pin 2 Common Pin 3 Pin X	Wien Bridge Terminals
Pin 4	Output B
Pin 5	Output A
Pin Y Pin Z	Integrator Feedback Terminals
(+)	Positive Power, +15VDC
(-)	Negative Power, -15VDC

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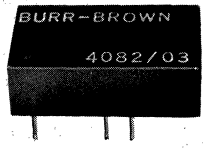

4082/03

GENERAL PURPOSE COMPARATOR

FEATURES

- **RELAY AND LAMP-DRIVING CAPABILITY Up to 100mA LOAD**
- **TRANSIENT PROTECTION TO 400mA**
- **RESPONSE TIME AND HYSTERESIS ADJUST**

DESCRIPTION

Model 4082/03 is a low cost hybrid integrated circuit comparator in a dual-in-line package. It combines a low-cost differential input comparator with an open collector transistor output stage capable of sinking 100mA. With transient protection of 400mA, this unit is an excellent choice to drive lamps, relays, and other devices with high transient requirements. In addition, the open collector output will accept up to +30VDC making the 4082/03 compatible with MOS circuitry and high noise immunity logic as well as TTL and DTL devices. The 4082/03 operates from ±15VDC power. Additional outputs are provided for response time control and hysteresis feedback.

OPERATION

Model 4082/03 will function when power is applied and the output load is connected between Pin 9 and Pin 13. The load may be resistor, lamp, or relay. A simplified diagram in shown in Figure 1.

Either input may be connected to common or to some reference voltage. Whenever the (+In) input is positive with respect to the (-In) input, the output transistor is switched ON. The load power ($+V_R$) may be any voltage up to +30VDC.

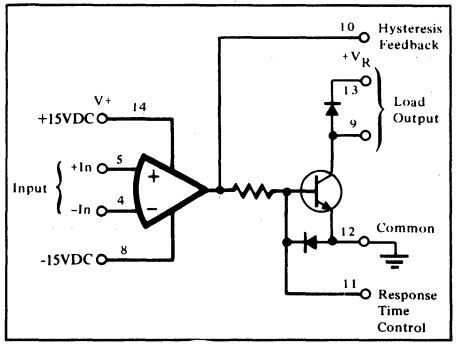

FIGURE 1. Simplified Diagram of Model 4082/03 Comparator.

HYSTERESIS

Hysteresis may be added by means of positive feedback as shown in Figure 2. The amount of hysteresis is approximately:

$$\text{Hysteresis} \approx 26V\ R_o/R_f + R_o,\ R_f \geq 10k\Omega$$

Adding hysteresis provides better noise immunity, but at the price of decreased switching resolution.

RESPONSE TIME

Response time can be decreased if desired by adding capacitance between Pin 11 and Pin 12 (common). This will limit the rise and fall times of the output voltage, which in turn limits turn-on surge currents when driving lamps.

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ELECTRICAL SPECIFICATIONS

Typical performance at 25°C and with rated supplies unless otherwise noted.

MODEL	4082/03	Units
INPUT		
Signal Levels		
Either (or both) Inputs	±10	V
Absolute Maximum	±15	V
Impedance (both Inputs)		
Differential, small signal	300	kΩ
Differential, large signal	10	kΩ
Common-mode	100	MΩ
Bias Current at 25°C	400	nA
Over Temperature Range, (max)	700	nA
Differential Offset Current at 25°C	±30	nA
Over Temperature Range, (max)	±80	nA
OUTPUT		
Switched Current Sink		
Impedance to common from output		
OFF state	1	MΩ
ON state	3	Ω
Load Voltage Supply (V_R)	0 to +30	V
Load Current (sinking)	Up to +100	mA
Transient (absolute maximum)	+400	mA
ACCURACY		
Sensitivity, (min)	±0.1	mV
Offset		
Over Temperature (max)[1]	±12	mV
at 25°C	±3	mV
vs Power Supply	±50	μV/V
FREQUENCY RESPONSE		
Total Switching Time[2]		
at 20mV Step Input	7	μsec
TEMPERATURE RANGE		
Operating, Rated Specification	-25 to +85	°C
Operating, Derated Performance	-40 to +85	°C
Storage	-55 to +100	°C
POWER SUPPLY REQUIREMENTS		
(-V and +V)		
Rated Supply Voltage	±15	V
Voltage Range	-14 to +16	V
Supply Drain, (max)	±12	mA

1. This offset is referred to the input and includes offset due to common-mode effects.
2. With load supply of +15VDC and with output load of 300Ω. Total switching time includes delay time and rise time. The input E_{IN} is a sine wave of frequency f_S.

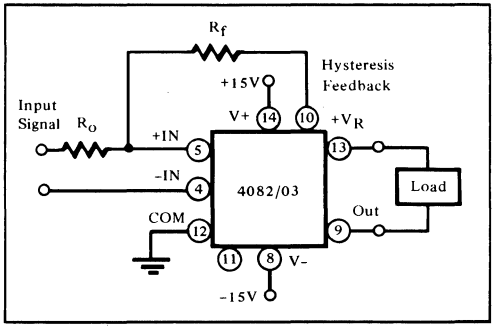
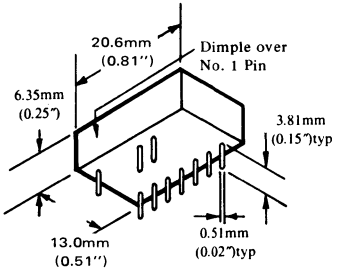
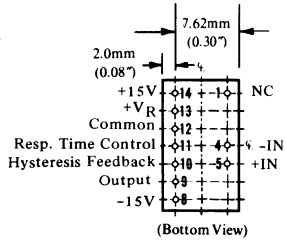


FIGURE 2. Connections for Adding Hysteresis.

MECHANICAL SPECIFICATIONS

MODEL 4082/03





WEIGHT: 0.12 oz. (3.40 grams)
GRID SPACING: 0.1" (2.5)
MATERIAL: Black Epoxy
PIN: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
CONNECTOR: Standard 14 pin DIP socket

BURR-BROWN®

4085

HYBRID MICROCIRCUIT PEAK DETECTOR

FEATURES

- STORES TRANSIENT VOLTAGES
- COMPLETELY SELF-CONTAINED
- ACCURATE TO ±0.01%
- LOW DROOP ERRORS
- SMALL DIP PACKAGE

DESCRIPTION

The 4085 is a specialized sample/hold amplifier that tracks an input signal until a maximum amplitude is reached. That maximum value is held at the analog output, and the digital STATUS output indicates that a peak has been detected. The unit can then be commanded to hold that value, ignoring additional peaks, or reset to a user-specified reference voltage. The 4085 detects positive-going peaks from -10V to +10V and is available in a hermetic metal package and a low-cost ceramic package. Three models are available, specified for temperature ranges 0 to +70°C (4085KG), -25 to +85°C (4085BM), and -55 to +125°C (4085SM).

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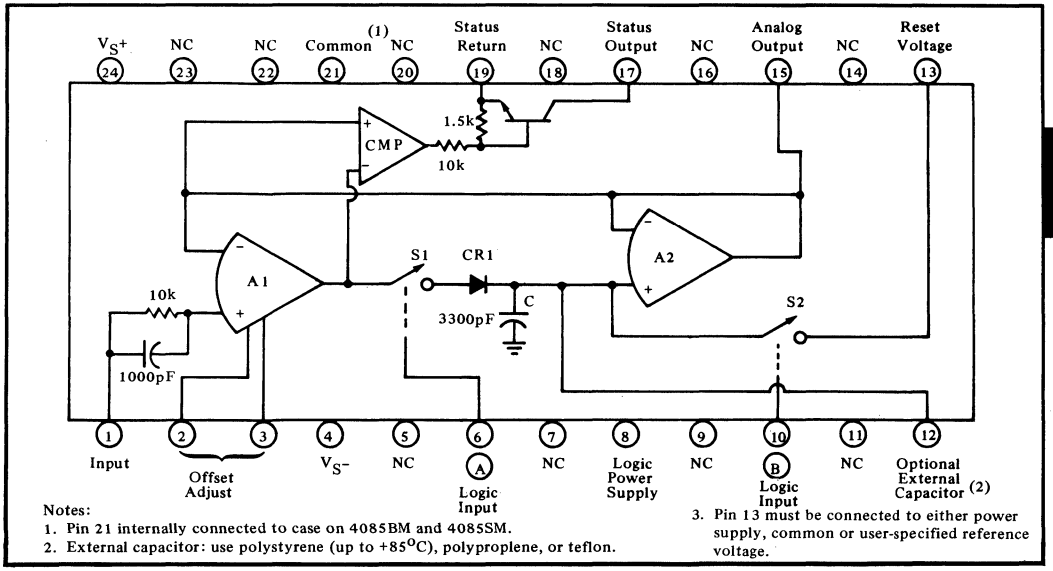
THEORY OF OPERATION

In the PEAK DETECT mode (S1 closed, S2 open), the analog output tracks the analog input until a peak value is reached. When the input voltage falls below the magnitude of the peak voltage, CR1 becomes reversed biased, and the feedback loop between A1 and A2 is broken. At this point, the status output transistor turns on and the magnitude of the peak voltage is held on the analog output. In the HOLD mode (S1 open, S2 open), the current charging path from the output of A1 to the capacitor is opened. The output voltage is equal to the voltage stored in the capacitor even though the input voltage may become larger than the peak voltage. In the RESET mode (S1 open, S2 closed), the voltage on the capacitor will charge to whatever voltage is applied to the RESET voltage input. If both S1 and S2 are closed at the same time, the output of A1 will be connected to the reset voltage input through a low impedance. This represents an illegal mode of operation, but will cause no damage to the unit.



Notes:
1. Pin 21 internally connected to case on 4085BM and 4085SM.
2. External capacitor: use polystyrene (up to +85°C), polyproplene, or teflon.
3. Pin 13 must be connected to either power supply, common or user-specified reference voltage.

FIGURE 1. 4085 Functional Diagram and Pin Configuration.

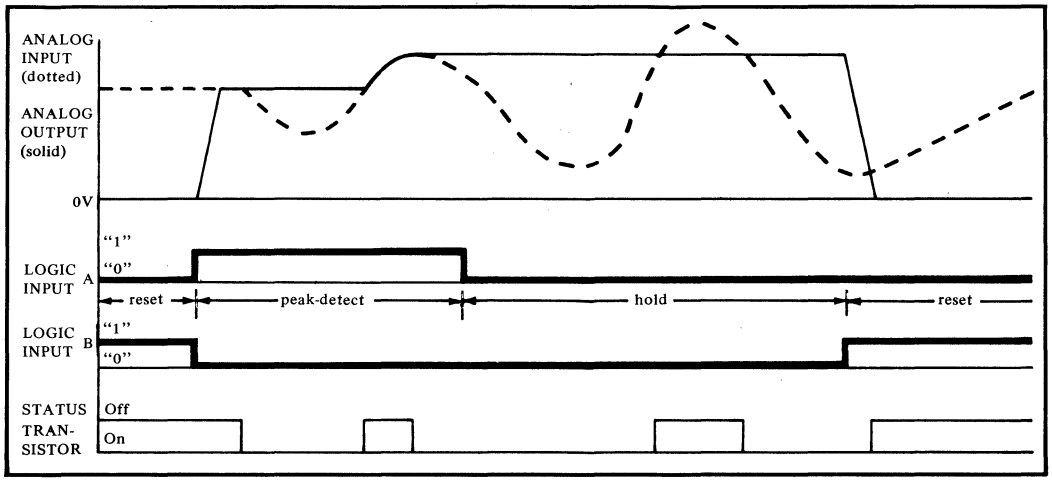


FIGURE 2. Timing Diagram For Peak-Detect Operation

ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C and ±15VDC and +5VDC power supplies unless otherwise noted.

MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG INPUT				
Signal Inputs				
Operating Range	±10	|V_S| -3		V
Absolute Maximum Range			±Supply	V
Input Offset Voltage (adjustable to zero)			2	mV
Input Offset Voltage Drift		15	50	µV/°C
Input Bias Current		15	50	pA
Input Resistance		1		GΩ
Input Capacitance		8		pF
DIGITAL INPUT				
Logic Levels				
Logic "1"	+2.4 at 50nA max			V
Logic "0"			+0.8 at 100µA max	V
Truth Table	Logic Input A		Logic Input B	
Peak Detect Mode	1		0	
Hold Mode	0		0	
Reset	0		1	
TRANSFER CHARACTERISTICS				
Voltage Gain		1.0		V/V
ACCURACY				
DC Voltage Gain Error			±0.01	% of FSR[3]
Dynamic Accuracy to 300Hz		±0.01	±0.02	% of FSR
100Hz			±0.01	% of FSR
Temperature Coefficient of Gain Error		±3		ppm/°C
Feedthrough			±0.05	% of Step
Droop (all units at T_A = +25°C)[5]			±0.06	mV/ms
T_A = +70°C, 4085KG			±0.5	mV/ms
T_A = +85°C, 4085BM			±1.2	mV/ms
T_A = +125°C, 4085SM			±12.0	mV/ms
Power Supply Sensitivity, ±V_S			±0.005	%/% Supply Variation
Logic Supply			±0.005	%/% Supply Variation
DYNAMIC PERFORMANCE				
Acquisition Time (BM, SM)			500	µsec
(KG)			800	µsec
Slew Rate		0.5		V/µsec
Charge Offset[4]		0.5	1	mV
Status Delay at 500Hz		0.7	1	ms
at 100Hz		1.2	2	ms

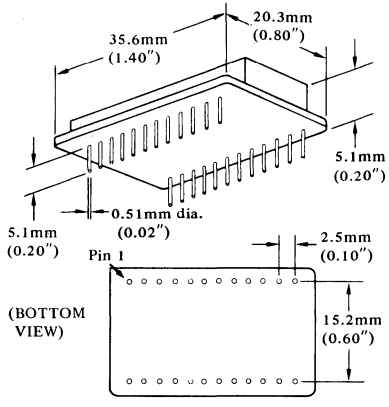
MODEL	4085 MIN	4085 TYP	4085 MAX	UNITS
ANALOG OUTPUT				
Voltage Range	±10	|V_S| -3		V
Output Current	5			mA
Output Resistance		0.2	0.5	Ω
Output Noise 10Hz to 100kHz		30		µV rms
Output Load Capacitance	50	100		pF
STATUS OUTPUT				
Collector-emitter Voltage			+30	V
Collector Current			20	mA
DC Current Gain	50	100		mA/mA
V_{BE}		0.65		V
RESET VOLTAGE				
Operating Range	±10	|V_S| -3		V
Absolute Maximum Range			±Supply	V
Discharge Current[1]	5		30	mA
POWER SUPPLY REQUIREMENTS				
Rated Voltage		±15		V
Operating Range	±8		±18	V
Current Drain (i_{out} = 0)			±20	mA
Rated Logic Supply Voltage[2]		+5.0 ±0.5		V
Logic Supply Current				
(Logic A & B high)		3.0 ±0.3		mA
(Logic A & B = 0V)		4.4 ±0.5		mA
TEMPERATURE RANGE				
Specification				
4085KG	0		+70	°C
4085BM	-25		+85	°C
4085SM	-55		+125	°C
Operating				
4085KG	-25		+85	°C
4085BM	-55		+90	°C
4085SM	-55		+125	°C
Storage				
4085KG	-30		+90	°C
4085BM	-60		+100	°C
4085SM	-60		+150	°C

Notes:

1. Any circuitry connected to the reset pin should be capable of sinking the desired discharge current of the internal 3300pF holding capacitor plus any external capacitor. The discharge current range is the current limit imposed by an internal FET switch. It does not imply that the I_{DSS} of external circuitry must be designed to limit current to this range.
2. Logic Supply, pin 8, may be connected to higher supply voltages for operation with MOS or CMOS logic. Refer to OPERATING INSTRUCTIONS.
3. FSR = Full Scale Range, 20V for the 4085.
4. Charge Offset is the charge transferred from the holding capacitor when the 4085 is switched to the hold mode.
5. Equation for droop: $\text{Droop (mV/ms)} = \frac{100\text{pA} \times 2^{\left(\frac{T - 25^{\circ}C}{11}\right)}}{3300\text{pF} + C_{ext}\,(\text{pF})}$

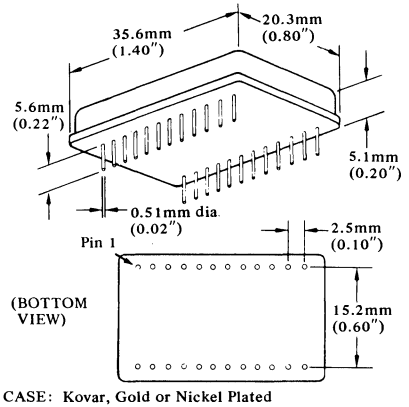
MECHANICAL SPECIFICATIONS

CERAMIC PACKAGE 4085KG



CASE: Black Ceramic (alumina)
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to Mil-Std-883, method 1014. Gross leak (condition C, step 1, Fluorocarbon).

METAL PACKAGE 4085BM, 4085SM



CASE: Kovar, Gold or Nickel Plated
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to Mil-Std-883, method 1014. Gross leak (condition C, step 1, Fluorocarbon) Fine leak (condition A, Helium, 5×10^{-7} cc/sec).

TYPICAL PERFORMANCE CURVES

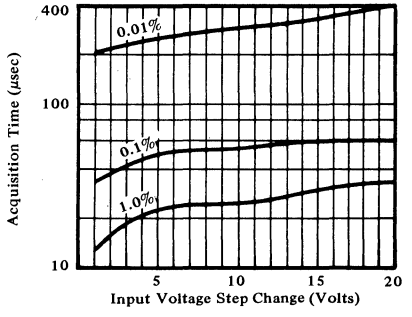


FIGURE 3. Acquisition Time

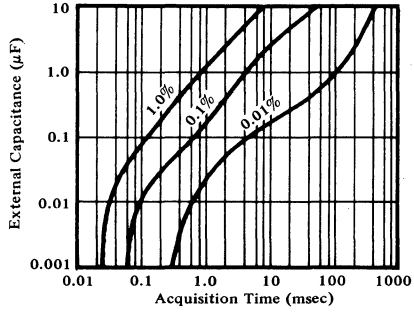


FIGURE 4. Acquisition Time

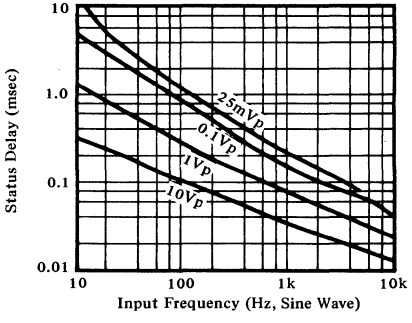


FIGURE 5. Status Output Delay

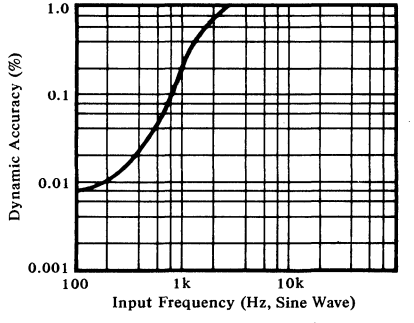


FIGURE 6. Dynamic Accuracy

OPERATING INSTRUCTIONS

OFFSET VOLTAGE ADJUSTMENT

The ±2mV input offset voltage of the 4085 may be nulled to zero by using the circuit shown in Figure 7. With the 4085 in the PEAK DETECT mode (logic input A = "1", logic input B = "0") apply zero volts to pin 1. Adjust the potentiometer until the output voltage is zero volts. Disconnect pin 12 after adjustment is made.

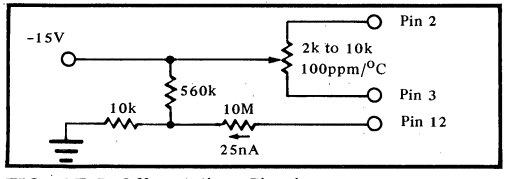


FIGURE 7. Offset Adjust Circuit

POWER SUPPLY CONSIDERATIONS

The 4085 will operate as specified with power supplies from ±8VDC to ±18VDC. To minimize noise pickup, the supply inputs should be decoupled with 1μF tantalum capacitors located physically close to the unit.

DIGITAL INPUTS AND LOGIC SUPPLY

The digital inputs may be driven with TTL or CMOS logic. Pin 8 should be tied to the logic supply. The logic supply voltage (V_L) may also be provided by connecting pin 8 through a resistor of value R(kohms) = 1.67 (V_S - V_L)/V_L to the +V_S supply ($V_S \geq V_L$). The logic threshold voltage is equal to 0.4 V_L - 0.7 volts.

INPUT FREQUENCY BANDWIDTH LIMITING

It is recommended that the input bandwidth be limited as much as possible by an RC section such as that shown in Figure 8. This is to limit noise spikes at the input that may cause erroneous readings. If detecting large pulse heights, a 5 μsecond time constant should be used. This will not degrade acquisition time or tracking accuracy for frequencies up to 500 Hz. For input frequencies greater than 500 Hz, a smaller time constant may be used.

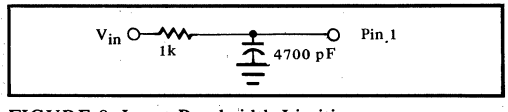


FIGURE 8. Input Bandwidth Limiting

STATUS OUTPUT CHARACTERISTICS

The open-collector, open-emitter output transistor is a small signal, medium speed switching transistor similar to a 2N2222. To facilitate driving a variety of devices, the configuration of the status output has been left to the user's discretion.

The internal comparator shown in the block diagram (Figure 1) has an output characteristic as follows. Input signal track: $Z_{out} \approx \infty$; peak hold: V_{out} = +V_S - 0.5 volts. Several configurations are illustrated in Figures 9 through 11. "Inverting" means logic "0" = peak has been detected, "Noninverting" means logic "1" = peak has been detected.

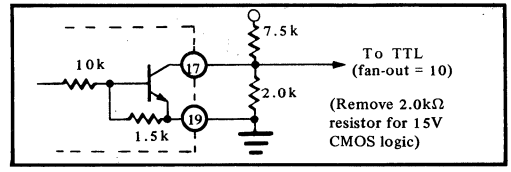


FIGURE 9. Inverting TTL (CMOS) STATUS Output.

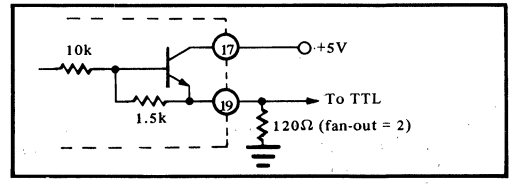


FIGURE 10. Noninverting TTL STATUS Output.

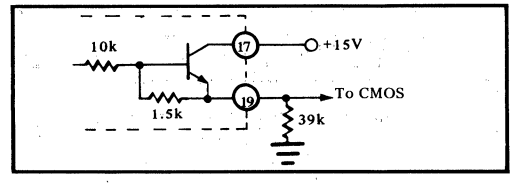


FIGURE 11. Noninverting CMOS STATUS Output

DESIGNING IN HYSTERESIS

It may be desirable in some situations to have hysteresis in the circuit such that small peaks will not be detected, eliminating jitter in the STATUS output. This is possible through external components connected as shown in Figure 12. After a peak is detected, the input voltage must be slightly greater (determined by R1/R2) than the previous peak to cause the output to resume tracking the input. This hysteresis voltage is expressed by:

$$V_H = \frac{(V_{in} - V_E - 0.9V)\ R1}{R1 + R2}$$

The emitter voltage of the status transistor should be tied to a voltage sufficiently lower than the lowest expected peak to allow proper operation.

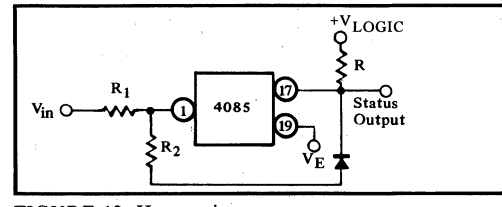


FIGURE 12. Hysteresis

APPLICATIONS

PEAK CATCHER

This circuit detects and holds the first peak it encounters. After the first peak is detected, it automatically is switched to the hold mode. To reset the circuit for catching another peak, a 10 μsec or longer positive logic pulse should occur at the "RELEASE" input. This will reset the peak detector to the desired voltage and put it in the peak-detect mode.

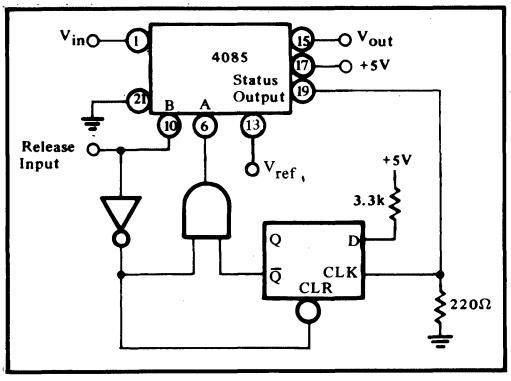


FIGURE 13. Peak Catcher

NO-RIPPLE, FAST SETTLING RMS-DC CONVERTER

If a waveform is known, the RMS value of the signal may be computed from the peak value. In this circuit, the RMS value is computed by the output amplifier from the peak value held by the 4085. The output in the circuit shown is updated manually. It may be updated automatically by replacing the switch circuit with an oscillator plus timing logic.

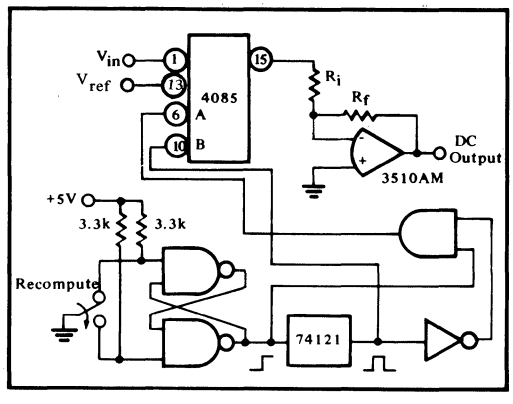


FIGURE 14. RMS-DC Converter

INTERFACING TO A/D CONVERTER

Interfacing to an A/D converter is straightforward. The gating of the A/D converter command allows a conversion only if a peak has been detected and permits completion of each conversion. If a peak occurs while the A/D is converting, it will not be detected.

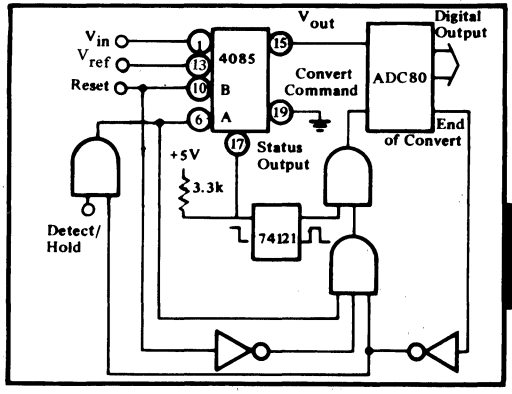


FIGURE 15. A/D Converter Interface

PEAK-TO-PEAK DETECTOR

Figure 16 shows a circuit that will display the peak-to-peak voltage of an input waveform. The STATUS output indicates that both positive and negative peaks have been detected and that the output is valid. The resistors around A3 should be matched to insure good common-mode rejection.

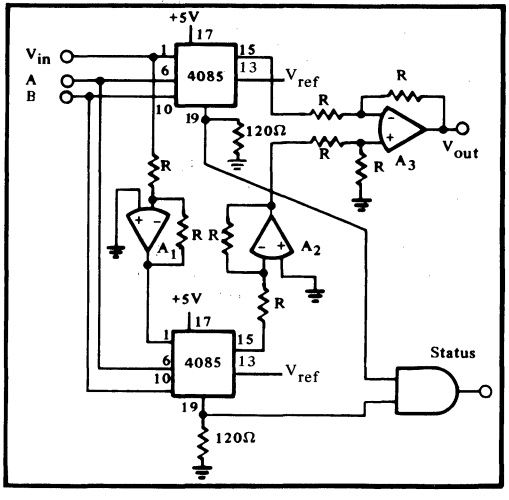


FIGURE 16. Peak-to-Peak Detector

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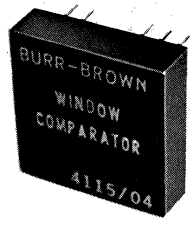


4115/04

WINDOW COMPARATOR

FEATURES

- ADJUSTABLE LIMITS FOR "HIGH", "LOW", AND "GO"
- UP TO 200mA LOAD CAPABILITY (each output)
- INPUT PROTECTION

APPLICATIONS

- PRODUCTION LINE TESTING
- TEMPERATURE CONTROLS
- INDUSTRIAL ALARMS
- LEVEL DETECTORS/CONTROLS

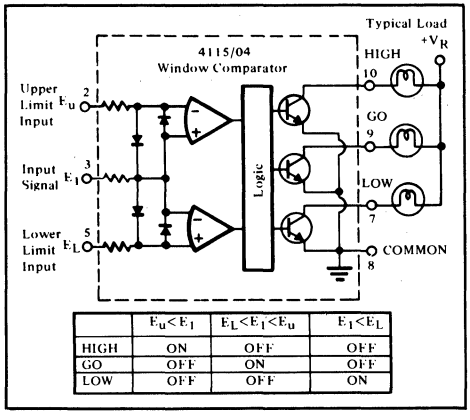
DESCRIPTION

Model 4115/04 is a hybrid IC window comparator in a double width DIP. The unit has three inputs - one for a voltage that sets the upper limit, another for a voltage that sets the lower limit, and a signal input. There are three mutually exclusive outputs - HIGH, LOW and GO. When an output is ON it will sink up to 200mA of current. This input diode protected device is designed to work with input voltages of up to ±10V, and will not be harmed by voltages to ±15V. The 4115/04 will drive a variety of loads including lamps, relays, MOS circuitry, and high noise immunity logic as well as DTL and TTL devices.

INSTALLATION

Separate connections should be made from each power supply common (+15VDC, -15VDC and V_R) to the 4115/04 common (pin 8).

To avoid unwanted pickup or chattering it may be necessary to include bypass capacitors from the ±15V supply pins (13 and 14) to the module common pin (8).



	$E_u<E_I$	$E_L<E_I<E_u$	$E_I<E_L$
HIGH	ON	OFF	OFF
GO	OFF	ON	OFF
LOW	OFF	OFF	ON

Model 4115/04 Transfer Characteristics.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

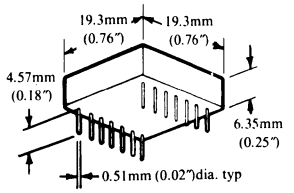
ELECTRICAL SPECIFICATIONS

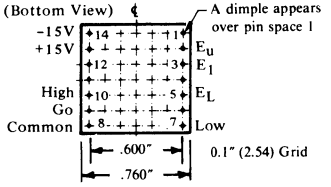
Typical performance at 25°C and with rated supply unless otherwise noted.

MODEL	4115 04	Units
INPUT		
All Inputs	±10V into 6kΩ (min)	
Maximum Safe Input	±15	V
ACCURACY		
D.C. Resolution (min)	±0.2	mV
Voltage Offset (referred to input)		
at 25°C (max)	±2	mV
vs Temperature (max)	±30	μV °C
Over Temperature Range (max)	±7	mV
vs Power Supply	±50	μV V
Switching Speed		
Total Switching Time at 30mV Overdrive	300	μsec
OUTPUT		
Impedance to COMMON from all Outputs		
OFF state	> 1	MΩ
ON state	3	Ω
Load Supply Voltage (V_R)	0 to +30	V
Load Current		
Steady State	+200	mA
Transient (absolute maximum)		
1 Second Duration	+400	mA
Saturation Voltage (V_{CE}) (max)		
at 200mA	0.7	V
TEMPERATURE RANGE		
Rated Specifications	-25 to +85	°C
Derated Performance	-40 to +85	°C
Storage	-55 to +100	°C
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltage	±15	VDC
Derated Performance	-12 to ±18	VDC
Quiescent Drain (max)	±15	mA

To achieve best results use stable quiet reference sources and drive signal input from low impedance source. Noise and drift in input sources readily masks the inherently high resolution of the device.

MECHANICAL SPECIFICATIONS





WEIGHT: 0.24 oz. (6.80 grams)
MATERIAL: Black Exoxy
PIN: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
CONNECTOR: Fits any commercial dual-in-line connector.

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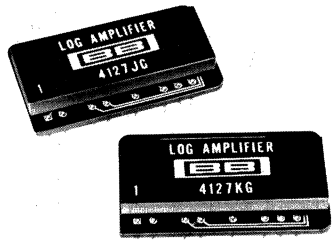


4127

LOGARITHMIC AMPLIFIER

FEATURES

- **ACCEPTS INPUT VOLTAGES OR CURRENTS OF EITHER POLARITY**
- **WIDE INPUT DYNAMIC RANGE**
  6 Decades of current
  4 Decades of voltage
- **VERSATILE**
  Log, antilog, and log ratio capability
- **SMALL SIZE**
  Doublewide DIP
- **LOW COST**

DESCRIPTION

Packaged in a ceramic doublewide DIP, the 4127 is the first hybrid logarithmic amplifier that accepts input signals of either polarity from current or voltage sources. A special purpose monolithic chip, developed specifically for logarithmic conversions, functions accurately for up to six decades of input current and four decades of input voltage. In addition, a newly-developed current inverter and a precise internal reference allow pin programming of the 4127 as a logarithmic, log ratio, or antilog amplifier.

To further increase its versatility and reduce your system cost the 4127 has an uncommitted operational amplifier in its package that can be used as a buffer, inverter, filter, or gain element.

The 4127 is available with initial accuracies (log conformity) of 0.5% and 1.0%, and operates over an ambient temperature range of -10°C to +70°C.

With its versatility and high performance, the 4127 has many applications in signal compression, transducer linearization, and phototube buffering. Manufacturers of medical equipment, analytical instruments, and process control instrumentation will find the 4127 a low-cost solution to many signal processing problems.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

GENERAL DESCRIPTION

The 4127 is a complete logarithmic amplifier that can be pin-programmed to accept input currents or voltages of either polarity. By making use of the internal current inverter, reference current generator, log ratio element, and uncommitted op amp, you can generate a variety of logarithmic functions, including the log ratio of two signals, the logarithm of an input signal, or the antilog of an input signal. The unique FET-input current-inverting element removes the polarity limitations present in most conventional log amplifiers.

Utilizing the inherent exponential characteristics of transistor functions, the 4127 calculates accurate log functions for input currents from 1 nA to 1 mA or input voltages from 1 mV to 10 V. Carefully-matched monolithic quad transistors and temperature sensitive gain elements are used to produce a log amplifier with excellent temperature characteristics.

THEORY OF OPERATION

A functional diagram of the 4127 circuit is shown in Figure 1. Besides the basic log amplifier, the 4127 contains a separate internal current source, a current inverter, and an uncommitted operational amplifier. The current inverter accurately converts negative input current to a positive current of equal magnitude.

The 4127 is capable of accurately logging input current over a 120dB range, but to use this full range good shielding practice must be followed. A current source input is, by definition, a high impedance source, and is therefore subject to electrostatic pickups.

The input op amps A_1 and A_3 have FET input stages for low noise and very low input bias current. The op amp A_1 will make the collector current of Q_1 equal to the signal input current I_S, and the collector current of Q_2 will be the reference input current I_R.

From the semiconductor junction characteristics, the base-to-emitter voltage will be

$$V_{BE} \approx \frac{m K T}{q} \ln \frac{I_C}{I_L}$$, where I_C = Collector current
I_L = Reverse saturation current
q, m, K = Constants
T = Absolute temperature

$$\text{So } E_1 = -\frac{m K T_1}{q} \ln \frac{I_S}{I_{L1}} \quad \text{and } E_2 - E_1 = \frac{m K T_2}{q} \ln \frac{I_R}{I_{L2}}$$

If the transistors Q_1 and Q_2 are at the same temperature and have matched characteristics then

$$E_2 = \frac{m K T}{q} \left[\ln \frac{I_R}{I_L} - \ln \frac{I_S}{I_L} \right]$$

$$E_2 = \frac{-m K T}{q} \ln \frac{I_S}{I_R}$$

The output op amp A_2 provides a voltage gain of approximately $(R_T + R_2)/R_T$, and the value of m K T/q is about 26mV at room temperature. Since resistor R_T varies with temperature to compensate for gain drift, the output voltage E_o expressed as a log will be

$$E_o = -A \log_{10} \frac{I_S}{I_R}$$

$$\text{where } A \approx \frac{R_T + R_2}{R_T} (26 \text{ mV}) \frac{1}{0.434}, \quad R_T \approx 520\Omega$$

The external resistor R_1 sets the reference current I_R and resistor R_2 sets the scale-factor "A". The two resistors must be trimmed to the desired values, but graphs in Figures 2 and 3 show the approximate relationships.

Figures 4 and 5 illustrate the relationship between the input current I_S and the output voltage E_o in terms of the externally adjusted parameters I_R and "A". This relationship is, of course, restricted to values of I_S between 1 nA to 1 mA and output voltages of less than ±10V.

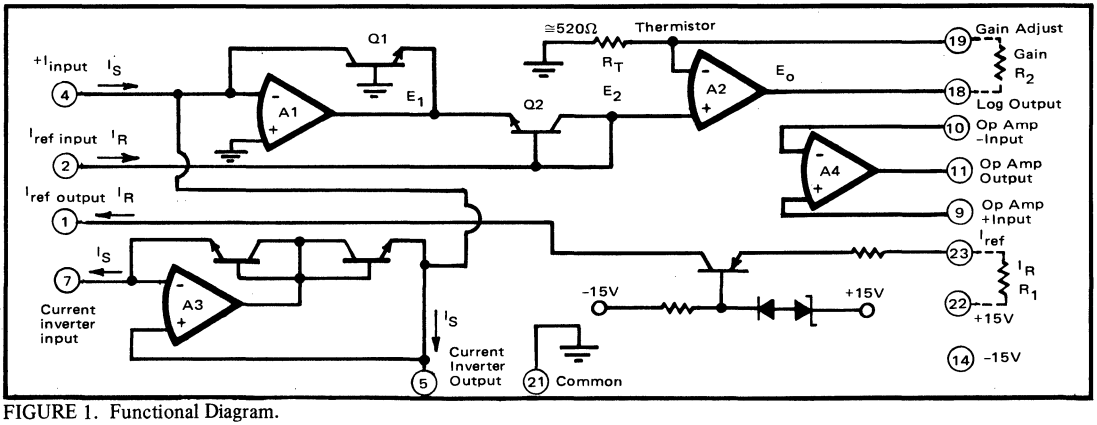


FIGURE 1. Functional Diagram.

SPECIFICATIONS

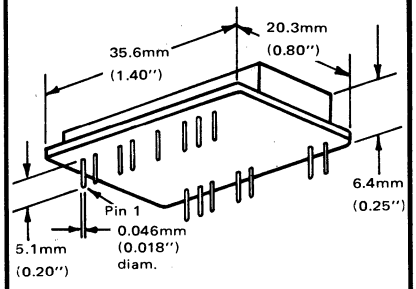
Typical specifications at +25°C with rated supplies unless otherwise specified.

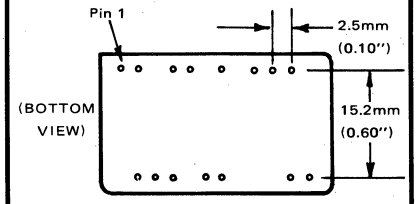
ELECTRICAL

	4127KG	4127JG
ACCURACY, (1) % of FSR		
Current Source Input: 1nA to 1mA	0.5% max	1% max
Voltage Input: 1mV to 10V	0.5% max	1% max
INPUT		
Current Source Input, Pin 4	+1nA to +1mA	
Pin 7	-1nA to -1mA	
Reference Current Input, Pin 2	+1μA to +1mA	
Absolute Maximum Inputs	±10mA or ±Supply Volts	
OUTPUT		
Voltage	±10V	
Current	±5mA	
Impedance	10 Ω	
FREQUENCY RESPONSE		
-3dB Small Signal at Current Input		
of 100μA	90kHz	
10μA	50kHz	
1μA	5kHz	
100nA	250Hz	
10nA	80Hz	
Step Response to within ±1% of Final Value (I_R = 1μA, A = 5)	10msec	
STABILITY		
Scale Factor Drift (Δ A/°C)	±0.0005A/°C	
Reference Current Drift (Δ I_R/°C)	±0.001 I_R/°C for $I_R \geq 1\mu A$	
	±0.003 I_R/°C for 400nA < I_R < 1μA	
Input Offset Current Drift (Δ I_S/°C)	10pA at +25°C, Doubles Every 10°C	
Input Offset Voltage Drift	±10μV/°C	
Accuracy vs. Supply Variation		
Reference Current	±0.001 I_R/V	
Input Offset Voltage	±300μ V/V	
Input Noise - Current Input	1pA RMS, 10Hz to 10kHz	
Voltage Input	10μV RMS, 10Hz to 10kHz	
UNCOMMITTED OP AMP CHARACTERISTICS		
Input Offset Voltage	5mV	
Input Bias Current	40nA	
Input Impedance	1MΩ	
Large Signal Voltage Gain	85dB	
Output Current	5mA	
TEMPERATURE RANGE		
Specification	0°C to +60°C	
Operating	-10°C to +70°C	
Storage	-55°C to +125°C	
POWER SUPPLY REQUIREMENTS		
Rated Supply Voltages	±15VDC	
Supply Voltage Range	±14VDC to ±16VDC	
Supply Current Drain		
at Quiescent (max.)	±20mA	
at Full Load (max.)	±26mA	

(1) Log conformity at 25°C

MECHANICAL





CASE: Black Ceramic
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
WEIGHT: 56 grams, (2 oz.)

PIN DESIGNATIONS

1. I_{REF} Output
2. I_{REF} Input
3. No Pin Present
4. +I Input
5. Current Inverter Output
6. No Pin Present
7. Current inverter Input
8. No Pin Present
9. Op Amp +Input
10. Op Amp -Input
11. Op Amp Output
12. No Pin Present
13. Make No Connection
14. Negative Supply
15. No Pin Present
16. No Pin Present
17. No Pin Present
18. Log Output
19. Gain Adjust
20. No Pin Present
21. Common
22. Positive Supply
23. I_{REF} Bias
24. No Pin Present

NOTE: Pin 4 is internally connected to pin 5.

TYPICAL PERFORMANCE CURVES

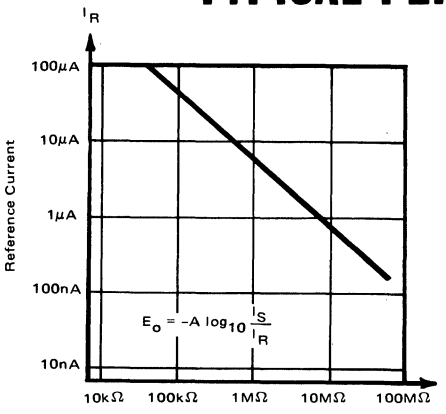


FIGURE 2. Relationship of Reference Current I_R and external resistor R_1.

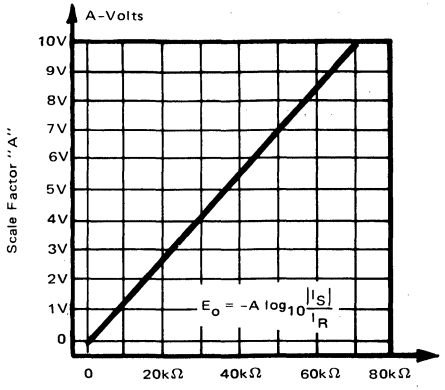


FIGURE 3. Relationship of scale factor "A" to gain-setting resistor R_2.

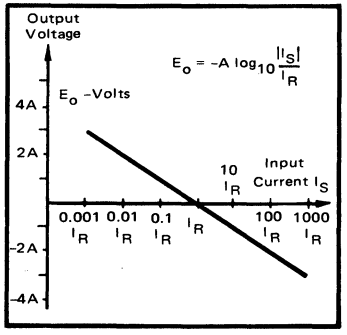


FIGURE 4. Log Relationship of $\frac{|I_S|}{I_R}$ and output voltage in terms of "A".

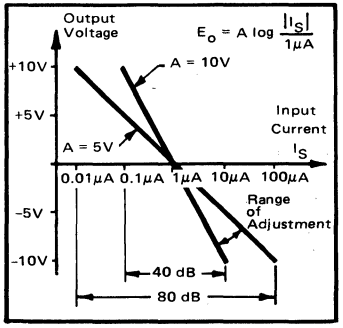


FIGURE 5. Relationship of $\frac{|I_S|}{I_R}$ to output voltage for I_R = 1μA and A = 5V and 10V.

4127

DISCUSSION OF SPECIFICATIONS

ACCURACY

The deviation from the ideal output voltage defined as a percent of the full scale output voltage.

INPUT/OUTPUT RANGE

The log relationships of $-A \log \frac{I_S}{I_R}$ and $-A \log \frac{E_S}{I_R R}$ are subject to the constraints specified. The 4127 can be operated with inputs lower than those given, but the accuracy will be degraded.

FREQUENCY RESPONSE

The small-signal frequency response varies considerably with signal level and scaling, so the frequency response is specified under several different operating conditions.

STABILITY

The use of a monolithic transistor quad and low-drift op amps minimizes drift, but some drift remains in the scale-factor, reference current, and input offset. Input offset consists of a bias current plus the op amp input voltage offset divided by the signal source resistance. Also, there is some slight drift in conformity to the log function and in output amplifier offset, but this is generally negligible.

SCALE FACTOR A AND REFERENCE CURRENT I_R.

Refer to CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.

CHOOSING THE OPTIMUM SCALE FACTOR AND REFERENCE CURRENT

To minimize the effects of output offset and noise, it is usually best to use the full ±10V output range. Once an output range of ±10V has been chosen, then "A" and I_R can be determined from the min/max of the input current I_S.

$$E_o = -A \log \frac{I_S}{I_R}, \text{ where } I_{min} < I_S < I_{max}$$

The output range of ±10V for an input range of I_{min} to I_{max} means that

$$+10 = -A \log \frac{I_{min}}{I_R} \text{ and } -10 = -A \log \frac{I_{max}}{I_R}$$

Adding these two equations together

$$\log \frac{I_{max} I_{min}}{I_R^2} = 0, \text{ or } I_R = \sqrt{I_{max} I_{min}}$$

The value for A can be found from:

$$10 = A \log \frac{I_{max}}{\sqrt{I_{max}\, I_{min}}}$$

In terms of the input current range for I_S, the values for I_R and A that will provide a full ±10V output swing are:

$$I_R = \sqrt{I_{max} I_{min}} \text{ and } A = \frac{10}{\log \frac{I_{max}}{I_R}}$$

Example: Assume that I_{min} is +10nA and I_{max} is +100μA.

This is an 80 dB range.

$$I_R = \sqrt{I_{max} I_{min}} = \sqrt{(10^{-4})\ (10^{-8})} = 10^{-6}, \text{ or } 1\mu A.$$

$$\frac{I_{max}}{I_R} = \frac{10^{-4}}{10^{-6}} = 100$$

$$\log \frac{I_{max}}{I_R} = 2 \quad \text{So } A = 5$$

For an I_R of 1μA and A of 5,

$$E_o = -5 \log \frac{I_S}{1\mu A}$$

*Single resistor recommended. Voltage divider network difficult to use due to amplifier offset voltage. RF500-108, 1k meg resistor available from Burr-Brown.

CONNECTION DIAGRAMS

If current inverter is not used leave pin 7 open.

Transfer function is $E_o = -A \log \frac{I_1}{I_R}$ where I_1 is a positive input current and I_R is the resistor-programmed internal reference current.

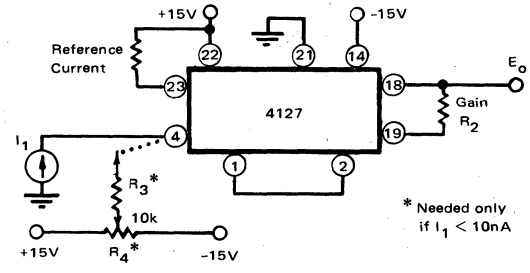


FIGURE 6.

ADJUSTMENT PROCEDURE

1. Refer to top of page for choosing optimum scale factor and reference current.
2. Apply $I_1 = I_R$, adjust R_1 such that $E_o = 0$.
3. Apply $I_1 = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $I_{1min} \geq 10nA$. Otherwise, apply $I_1 = 1nA$, make $R_3 = 1k\Omega$* and adjust R_4 for the proper output voltage.

Transfer function is $E_o = -A \log \frac{|I_1|}{I_R}$ where I_1 is a negative input current and I_R is the resistor-programmed internal reference current.

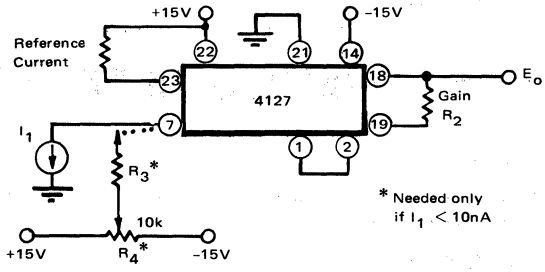


FIGURE 7.

ADJUSTMENT PROCEDURE

1. Refer to top of page for choosing optimum scale factor and reference current.
2. Apply $|I_1| = I_R$ adjust R_1 such that $E_o = 0$.
3. Apply $|I_1| = I_{max}$, adjust R_2 for the proper output voltage.
4. Repeat steps 2 and 3 if necessary.
5. Ignore this step if $|I_{1min}| \geq 10nA$. Otherwise, apply $|I_1| = 1nA$, make $R_3 = 1k\Omega$* and adjust R_4 for the proper output voltage.

CONNECTION DIAGRAMS

Transfer function is $E_0 = -A \log \frac{E_1}{R_4 I_R}$, where E_1 is a positive input voltage and I_R is the resistor-programmed internal reference current.

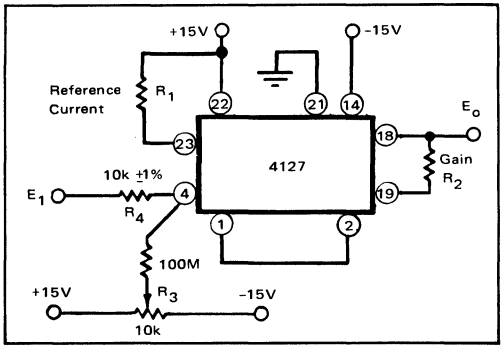


FIGURE 8.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. Apply $E_1 = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $E_1 = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $E_1 = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

NOTE: If lockup occurs at low input levels, pin 4 should be connected to pin 5.

Transfer function is $E_0 = -A \log \frac{|E_1|}{R_4 I_R}$, where E_1 is a negative input voltage and I_R is the resistor-programmed internal reference current.

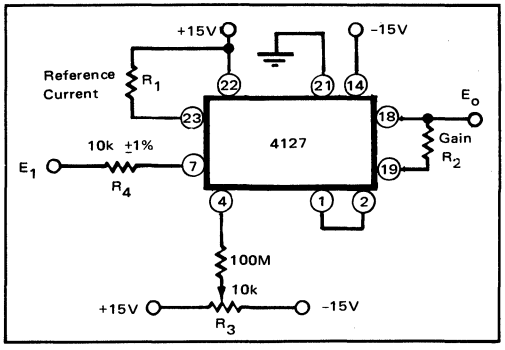


FIGURE 9.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. Apply $|E_1| = I_R$ (10kΩ), adjust R_1 such that $E_0 = 0$.
3. Apply $|E_1| = E_{max}$, adjust R_2 for the proper output voltage.
4. Apply $|E_1| = E_{min}$, adjust R_3 for the proper output.
5. Repeat steps 2 through 4 if necessary.

Transfer function is $E_0 = -A \log \frac{|I_1|}{|I_2|}$ with I_1 and I_2 negative; $|I_1| \geq 1nA, |I_2| \geq 1\mu A$.

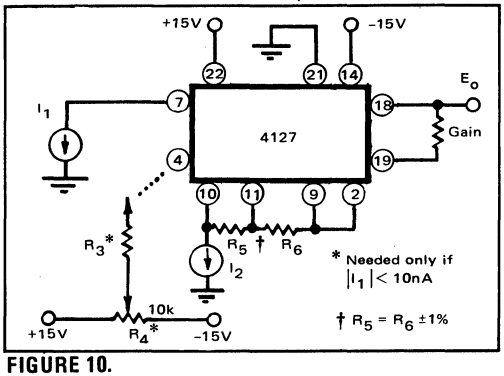


FIGURE 10.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. No further adjustment is necessary if I_1 min ≥ 10nA, otherwise connect the R_3 and R_4 network, with R_4 = 10k and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of ±5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_0 = -A \log \frac{|I_1|}{I_2}$ with I_1 negative, I_2 positive; $|I_1| \geq 1nA$, $I_2 \geq 1\mu A$.

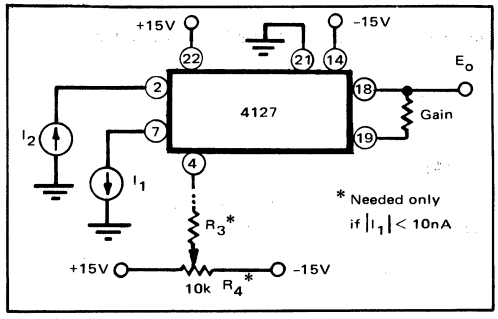


FIGURE 11.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. No further adjustment is necessary if $|I_1|$min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with R_4 = 10k and $R_3 = 10^9\Omega$. Adjust R_4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

Transfer function is $E_0 = -A \log \frac{I_1}{I_2}$ with I_1 and I_2 positive; $I_1 \geq 1nA$, $I_2 \geq 1\mu A$.

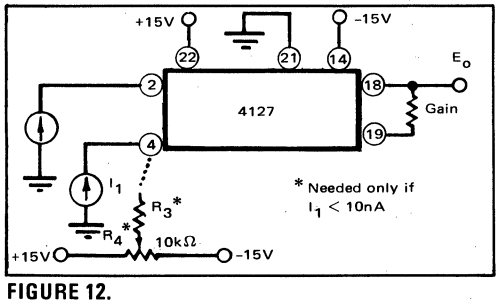


FIGURE 12.

ADJUSTMENT PROCEDURE

1. Refer to CHOOSING OPTIMUM SCALE FACTOR AND REFERENCE CURRENT.
2. No further adjustment is necessary if I_1 min $\geq$ 10nA, otherwise connect the R_3 and R_4 network, with R_4 = 10k and $R_3 = 10^9\Omega$. Adjust R4 for proper output voltage after adjusting gain errors. Since the voltage at pin 4 is in the range of $\pm$5mV, it is not practical to use a T - network to replace R_3.

ANTILOG OPERATION

The 4127 can also perform the antilog function. The output is connected through a resistor R_0 into the current input, pin 4. The input signal is connected through a gain resistor to pin 19 as shown in Figure 13.

These connections form an implicit loop for computing the antilog function. From the block diagram of Figure 1, the voltage at the inverting input of the output amplifier A2 must equal E_2, so

$$E_2 \approx \frac{R_T}{R_T + R_2} E_S, \quad R_T \cong 520\Omega$$

Since the output is connected through R_0 to pin 4, the current I_S will equal E_0/R_0 and E_2 will be

$$E_2 = -\frac{m K T}{q} \ln \frac{E_0}{R_0 I_R}$$

Combining expressions for E_2 gives the relationship

$$\frac{R_T}{R_T + R_2} E_S = -\frac{m K T}{q} \ln \frac{E_0}{R_0 I_R}$$

$$-\frac{E_S}{A} = \log \frac{E_0}{R_0 I_R}$$

where

$$A \approx \frac{R_T + R_2}{R_T} (26mV) \frac{1}{0.434}$$

$$E_0 = R_0 I_R \text{ Antilog} - \frac{E_S}{A}$$

Setting R_0 and I_R will set the scale factor. For example, an R_0 of 1MΩ and I_R of 1μA will give a scale factor of unity and

$$E_0 = \text{Antilog} - \frac{E_S}{A}$$

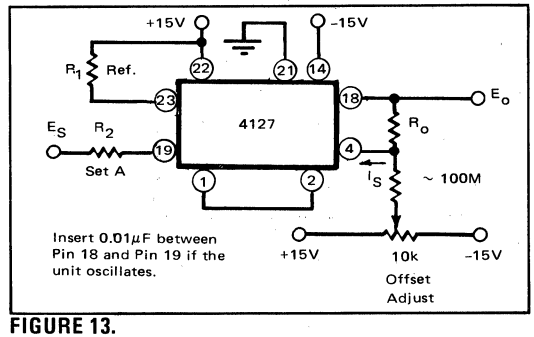


FIGURE 13.

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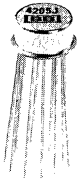

4203
4205

Integrated Circuit
MULTIPLIER-DIVIDERS

FEATURES

- LASER-TRIMMED
  Requires No Adjustment
- GUARANTEED ACCURACY - 1% or 2%
- SELF-CONTAINED
  No Additional Amplifiers
- FAST SLEWING - 25V/μsec
- SMALL PACKAGE - TO-100

APPLICATIONS

- MULTIPLICATION, DIVISION, SQUARING, SQUARE ROOTS
- RMS MEASUREMENTS
- FREQUENCY DOUBLER
- BALANCED MODULATOR AND DEMODULATOR
- ELECTRONIC GAIN CONTROL
- FUNCTION GENERATOR AND LINEARIZING CIRCUITS
- PROCESS CONTROL SYSTEMS

DESCRIPTION

Burr-Brown Models 4203 and 4205 are integrated circuit multipliers designed for general purpose usage. In addition to four-quadrant multiplication they also perform division and square rooting of analog signals, requiring no additional amplifiers in performing the above functions. They are laser-trimmed prior to final packaging and are guaranteed to their rated accuracy with no external components. This is a distinct advantage from the standpoints of cost and reliability.

These multipliers contain their own zener-regulated references and, as a result, are much less sensitive to supply voltage variation than were earlier IC multipliers. The fast (25V/μsec) slew rate and 1MHz bandwidth are key performance factors for applications where delay phase shift must be minimized. Harmonic distortion of the 4203 and 4205 remain low for frequencies well above 100kHz, an important asset in modulation applications.

Other desirable features are hermetic TO-100 package (10-pin version of TO-99) and wide temperature range of operation. The 4203S and 4205S are specified for operation over the full MIL temperature range.

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PDS-473

SPECIFICATIONS

ELECTRICAL

Typical at +25°C with rated power supplies unless otherwise noted.
Percent specifications refer to % of full scale (10V).

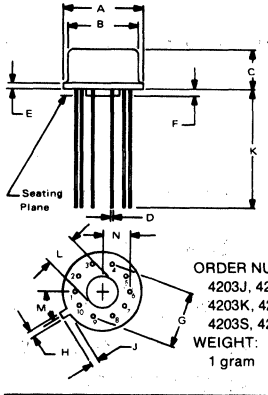
MODEL	4203J/4205J	4203K/4205K	4203S/4205S
OUTPUT FUNCTION 4203		XY/10	
4205		$(X_1 - X_2)(Y_1 - Y_2)/10$	
TOTAL ERROR*			
Internal Trim	2%, max	1%, max	1%, max
External Trim	1%	0.6%	0.6%
vs Temperature		0.04%/°C	
vs Supply		0.2%/%	
INDIVIDUAL ERRORS			
Output Offset at +25°C (X = Y = 0)		20mV, max	
vs Temperature (Operating Range)		0.4mV/°C	
vs Supply		10mV/%	
Scale Factor Error	1%	0.6%	0.6%
vs Temperature (Operating Range)		0.04%/°C	
vs Supply		0.1%/%	
Nonlinearity			
X(X = 20V, p-p; Y = ±10VDC)	0.8%	0.5%	0.5%
Y(Y = 20V, p-p; X = ±10VDC)		0.2%	
Feedthrough at 50Hz			
X = 0, Y = 20V, p-p (Internal Trim)		50mV, p-p	
(External Trim)		20mV, p-p	
vs Temperature		1mV, p-p/°C	
Y = 0, X = 20V, p-p (Internal Trim)		50mV, p-p	
(External Trim)		20mV, p-p	
vs Temperature		2mV, p-p/°C	
AC PERFORMANCE			
Slew Rate		25V/μsec	
-3dB Small Signal Bandwidth		1MHz	
1% Amplitude Error		40kHz	
1% Vector Error (0.57° phase shift)		10kHz	
Settling Time (2% of final value, 20V, step)		1μsec	
Overload Recovery Time		3μsec	
OUTPUT NOISE (X = Y = 0)			
10kHz to 10MHz		3mV, rms	
10Hz to 10kHz		600μV, rms	
INPUT CHARACTERISTICS			
Input Voltage Range			
Rated Operation		±10V	
Absolute Max		±15V	
Input Impedance, X		10MΩ	
Y		10MΩ	
Z		36kΩ	
OUTPUT CHARACTERISTICS			
Rated Output		±10V at ±5mA	
Output Impedance		1Ω	
POWER SUPPLY REQUIREMENTS			
Rated Voltage		±15VDC	
Operating Range		±12VDC to ±18VDC	
Quiescent Current		±4.5mA	
TEMPERATURE RANGE			
Operating, Rated Performance	0°C to 70°C		-55°C to +125°C
Storage		-65°C to +150°C	

*Total error is a tested maximum at +25°C and represents the maximum allowed value for the sum of the individual errors.

MECHANICAL

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

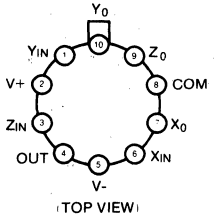
Pin numbers shown for reference only.
Numbers may not be marked on package.



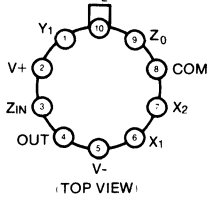
ORDER NUMBER:
4203J, 4205J
4203K, 4205K
4203S, 4205S
WEIGHT:
1 gram

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

CONNECTION DIAGRAM



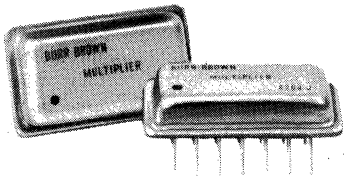
(TOP VIEW)
4203



(TOP VIEW)
4205

BURR-BROWN®

4204



ANALOG MULTIPLER-DIVIDER

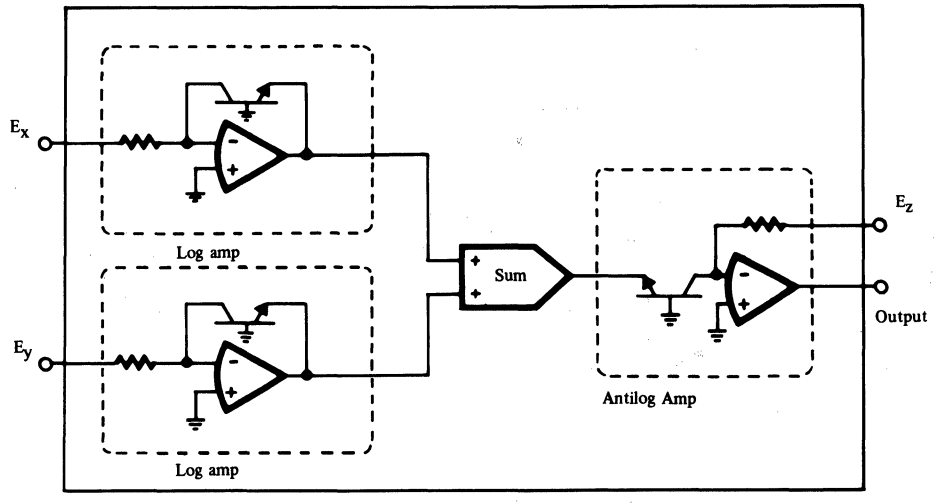
FEATURES

IMPROVE SYSTEM ACCURACY
±0.25% and ±0.5% units

LOW COST
0.5% accuracy

IMPROVE ACCURACY
OVER TEMPERATURE - ±0.02%/°C max

SIMPLIFY ASSEMBLY
Laser-trimmed at the factory
No external components required



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DESCRIPTION

The 4204 is an internally trimmed four quadrant analog multiplier/divider using the log/antilog technique. This method yields excellent accuracy, low noise and moderate bandwidth–at low cost. No external components or amplifiers are required with the 4204. Accuracy specifications are guaranteed without external adjustments and are verified at Burr-Brown by an automatic tester which scans the X-Y plane. Maximum error at any point in the plane is required to be less than the specified values.

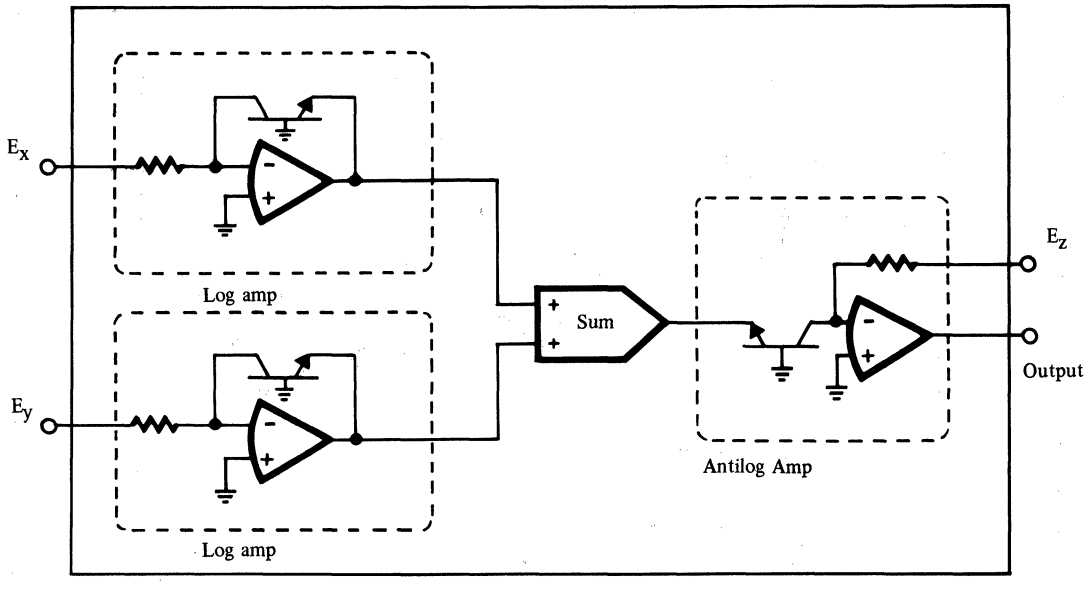
The laser trimmed 4204 is the first high accuracy hybrid IC multiplier/divider ever offered. Just as Burr-Brown was first to offer internally laser trimmed IC multipliers with accuracies of 1% and 2% (Model 4203), we have now extended this money saving technology into the accuracy areas where only higher priced modules were previously available. The excellent tracking characteristics of adjacent monolithic transistors is a key element in maintaining the 4204's high accuracy performance over the temperature range. By variation of external pin connections, the 4204 may be used as a divider or square rooter. No external amplifiers are required for either operation.

THEORY OF OPERATION

The 4204's log-antilog multiplication technique is based upon the logarithmic voltage-current relationship in a semiconductor junction. This action is shown by this simplified equation: $V_{be} = (\frac{KT}{q})(\ln I_C - \ln I_S)$

where V_{be} is the transistor's emitter base voltage, I_C is the transistor collector current, I_S is the collector saturation current, K is Boltzmann's constant, q is the charge of one electron and T is the absolute temperature in degrees Kelvin. As can be seen from the equation, the logarithmic function is extremely temperature sensitive. The 4204, however, has excellent temperature characteristics because the log and antilog circuitry have equal and opposite temperature drifts which cancel to a first order approximation. The log and antilog circuits will compensate each other to the extent that the various logging transistors are matched to each other. In the 4204 these transistors are placed adjacently on a monolithic chip to obtain the best possible matching and so the best possible performance.

BLOCK DIAGRAM



Functional Diagram of Model 4204.

SPECIFICATIONS

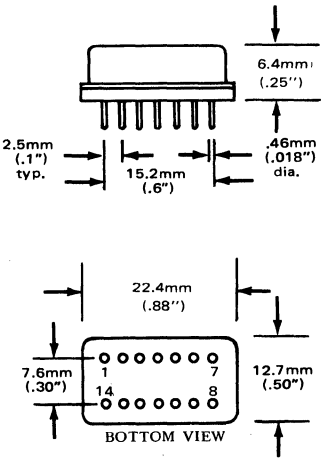
Typical performance at +25°C with rated power supplies unless otherwise noted.
Per cent specifications refer to % of full scale (10V).

ELECTRICAL

MODEL	4204J	4204K	4204S
OUTPUT FUNCTION	$\frac{E_x E_y}{10}$	*	*
TOTAL ERROR**			
Internal trim †	0.5% max	0.25% max	0.25%,max
External trim, typ	0.2%	0.1%	0.1%
vs. Temperature	0.01%/°C	*	0.02%/°C,max
vs. Supply	0.02%/%	*	*
INDIVIDUAL ERRORS			
Output Offset X=Y=0	15 mV	5 mV	5 mV
Scale Factor Error	0.2%	0.1%	0.1%
Non-Linearity			
X = 20 V, p-p Y = −10 VDC Y = 20 V, p-p X = −10 VDC	0.005%	*	*
X = 20 V, p-p Y = +10 VDC Y = 20 V, p-p X = +10 VDC	0.05%	*	*
Feedthrough @ 50 Hz			
X = 20 V, p-p Y = 0	10 mV p-p	5 mV p-p	5 mV p-p
Y = 20 V, p-p X = 0	10 mV p-p	5 mV p-p	5 mV p-p
AC PERFORMANCE		*	*
Slew Rate	1 V/μsec		
−3 dB Small Signal Bandwidth	250 kHz		
1% Amplitude Error	33 kHz		
1% Vector Error (0.57° phase shift)	2.5 kHz		
Full Power Response	20 kHz		
OUTPUT NOISE X = Y = 0.0V		*	*
DC to 10 kHz	300 μV rms		
INPUT CHARACTERISTICS		*	*
Input Voltage			
Maximum for Rated Specifications X,Y,Z	±10 V		
Maximum Safe Level X,Y,Z	±Supply		
Input Impedance X/Y/Z	25kΩ/25kΩ/100kΩ		
OUTPUT CHARACTERISTICS		*	*
Rated Output			
Voltage, min	±10 V		
Current, min	±5 mA		
Output Impedance	1 Ω		
POWER SUPPLY REQUIREMENTS		*	*
Rated Supply	±15 VDC		
Operating Range	±14 to ±16 V		
Quiescent Current	+15 mA, −8.5 mA		
TEMPERATURE RANGE		*	
Specification	-25°C to +85°C		-55°C to +125°C
Operating	-55°C to +125°C		*
Storage	-65°C to +125°C		*

*Same as for 4204J.
** Total error is a tested maximum and does not represent a sum of the maximum individual errors as the maximum individual errors do not occur at the same X, Y operating point.
† With output loading of 10 kΩ or less.

MECHANICAL



PIN 1 IS IDENTIFIED BY A BLACK DOT ON THE TOP SURFACE

Pin material and plating composition meet Method 2003 (solderability) of Mil-Std-883 [except for paragraph 3.2.]

PIN CONNECTIONS

1	E_z
2	Output
3	$-V_s$
4	Feedthrough Adj.
5	Make No Connection
6	Make No Connection
7	E_x
8	Internal Reference
9	Make No Connection
10	Ground
11	Feedthrough Adj.
12	Offset Adj.
13	E_y
14	$+V_s$

TYPICAL PERFORMANCE CURVES

Typical Performance @25°C and ±15 VDC

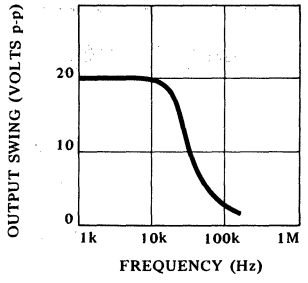


FIGURE 1. Large Signal Frequency Response

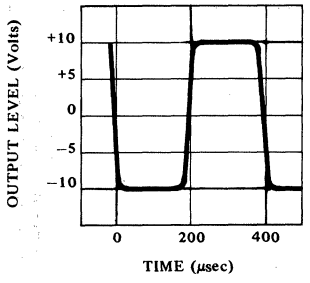


FIGURE 2. Step Response

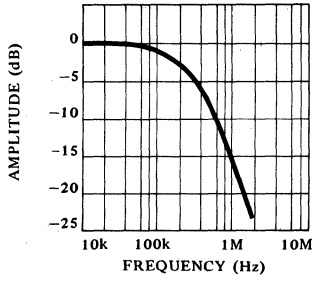


FIGURE 3. Small Signal Frequency Response

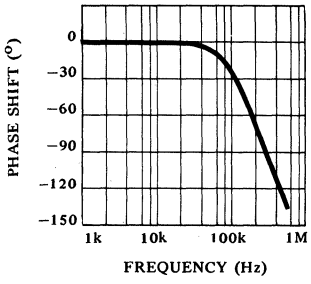


FIGURE 4. Small Signal Frequency Response

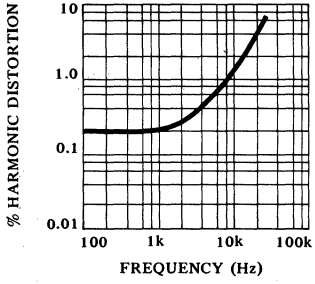


FIGURE 5. Output Distortion vs. Frequency

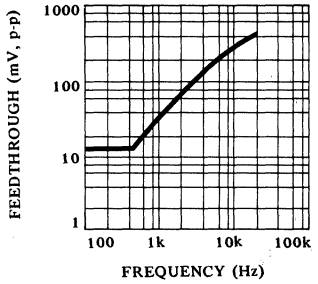


FIGURE 6. AC Feedthrough vs. Frequency

DISCUSSION OF PERFORMANCE CURVES

LARGE SIGNAL FREQUENCY RESPONSE

This response curve describes the output voltage capability of the 4204 as a function of frequency. The measurement is made with one input at +10 or −10 VDC, and with a sine wave applied at the other input. An output distortion of 0.5% is allowed.

STEP RESPONSE

Step response is measured with one input at +10 or −10VDC and with a 20 volt p-p square wave applied at the other input.

SMALL SIGNAL FREQUENCY RESPONSE

These curves are the amplitude and phase response of the 4204's transfer function, when one input is held at +10 or −10 VDC. A sine wave signal is applied to the other input. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

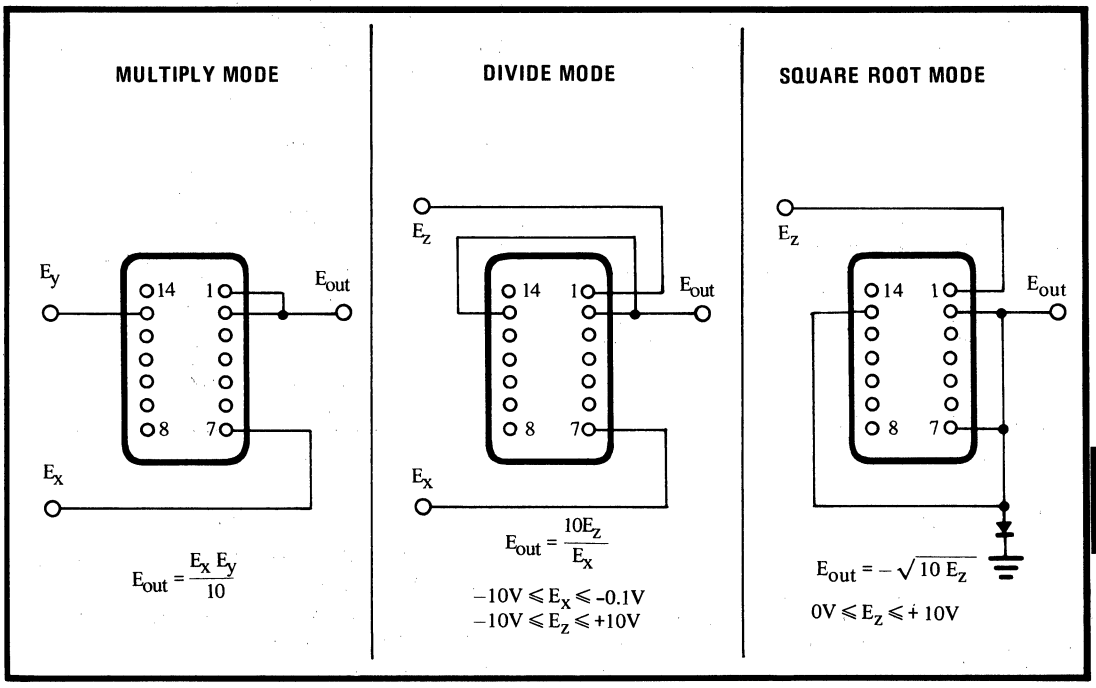
OUTPUT DISTORTION

The output distortion of the 4204 is of most interest in modulator applications. The curve of Figure 5 characterizes this distortion with one input of the 4204 held at +10 or −10 VDC. A sine wave is applied to the other input. The sine wave amplitude is held constant at 20 volts p-p while frequency is varied.

AC FEEDTHROUGH

The variation of feedthrough as a function of frequency is illustrated by Figure 6. One of the inputs is a zero while a 20 volt p-p sine wave is applied at the other input. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

OPERATING MODES



4204

ADJUSTMENTS

Although the 4204 will achieve specified performance in the multiply mode with no external trimming, optimized performance can be achieved with external adjustments. The proper connections and the trim procedures are explained below.

The 4204 will operate within specification with any combination of input signals. The best performance, however, will be obtained in the 2nd, 3rd and 4th quadrants. That is if four quadrant operations are not needed, the performance of the 4204 can be optimized by constraining operation to quadrants 2, 3 and 4 rather than 1.

MULTIPLICATION

MULTIPLICATION TRIM PROCEDURE (FIG. 7)

1) Set E_X = 0 and apply a 10 volt peak-peak sine wave (50 Hz) to E_Y: Adjust R_1 for minimum output.
2) Set E_Y = 0 and apply a 10 volt peak-to-peak sine wave (50 Hz) to E_X: Adjust R_2 for minimum output.
3) Set $E_X = E_Y$ = 0: Adjust R_3 for E_{out} = 0.000 V.
4) Set $E_X = E_Y$ = +10.000 V ±1 mV: Adjust R_4 for E_{out} = +10.000 V ±2 mV.

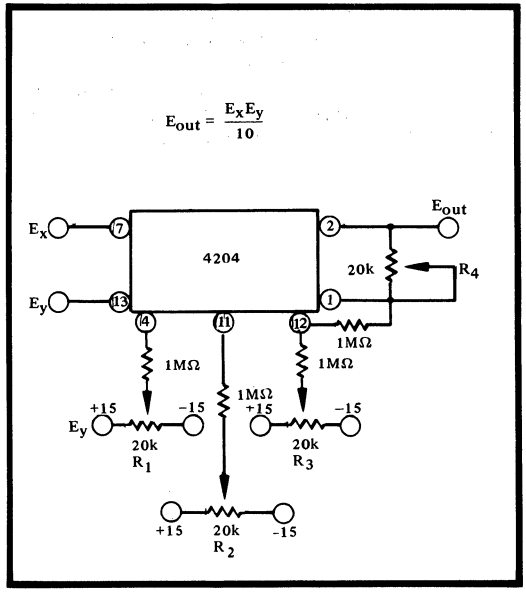


FIGURE 7. Multiplication Trim Procedure.

DIVISION

The 4204 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that the maximum output error is approximately given by

$$\text{divider error} \approx \frac{10\epsilon_m}{Ex}$$

where ϵ_m is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of E_X. A 10:1 denominator range is usually the practical limit. If more accurate division is required over wide range of denominator voltages, the Burr-Brown model DIV100 is recommended (0.25% max error over 40:1 range).

DIVISION TRIM PROCEDURE (FIG. 8)

1) Set all potentiometers @ about mid-scale.
2) Set E_Z = 0 volt, $E_X \approx -10$ V, adjust R_2 such that E_O = 0.000 V ±2 mV.
3) Set $E_X = E_Z = -10.000$VDC ±2 mV, adjust R_3 such that $E_O = +10.000$VDC ±2 mV.
4) Set $E_X = E_Z \approx$ minimum value required by application, adjust R_1 such that $E_O = +10.000$VDC ±5 mV.
5) Repeat steps (2) through (4) if necessary.

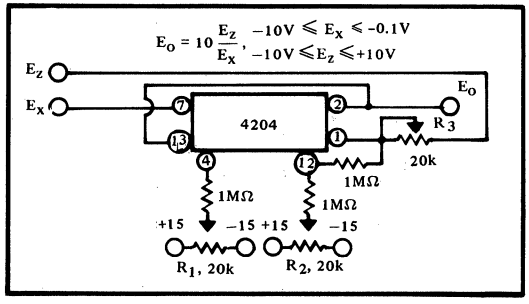


FIGURE 8. Division Trim Procedure.

SQUARE ROOT

The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node. Errors in the Square Root mode of operation become troublesome for small values of E_Z. However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of E_Z is given approximately by

$$E_{out} \approx -\sqrt{10E_Z + 10\epsilon_m}$$

where ϵ_m is the total error specified for Multiply mode. This equation can be used to determine the feasibility of using the 4204 as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, the Model 4302 multifunction converter is recommended.

SQUARE ROOT TRIM PROCEDURE (FIG. 9)

1) Set E_Z = +10.000VDC ±2 mV, adjust R_2 such that E_O = -10.000VDC ±2 mV.
2) Set $E_Z \approx$ minimum value required by application (E_{Zm}) adjust R_1 such that $E_O = -\sqrt{10\,E_{Zm}}$ ±2 mV.
3) Repeat steps (1) and (2) if necessary.

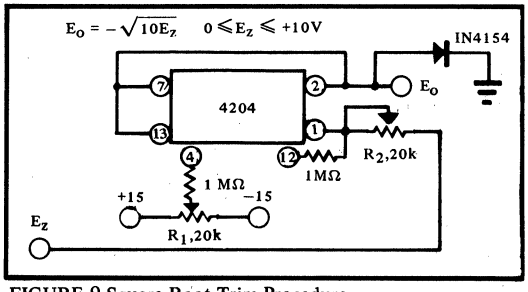
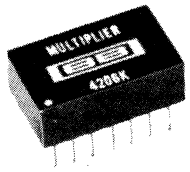


FIGURE 9. Square Root Trim Procedure.

BURR-BROWN®

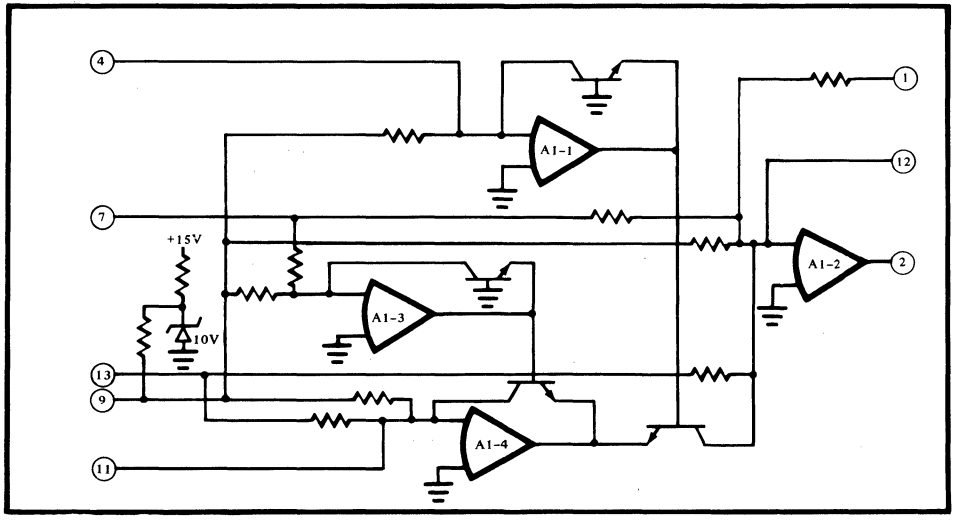
4206



ANALOG MULTIPLIER-DIVIDER

FEATURES

- HIGH TOTAL ACCURACY
  0.25% and 0.5% max, no external trims
  0.1% and 0.2% typ. with external trims
- LOW TEMPERATURE DRIFT
  100ppm/°C from 0°C to +70°C
- SMALL PACKAGE
  Dual-in-line saves board space
- LOW COST



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PDS-330B

DESCRIPTION

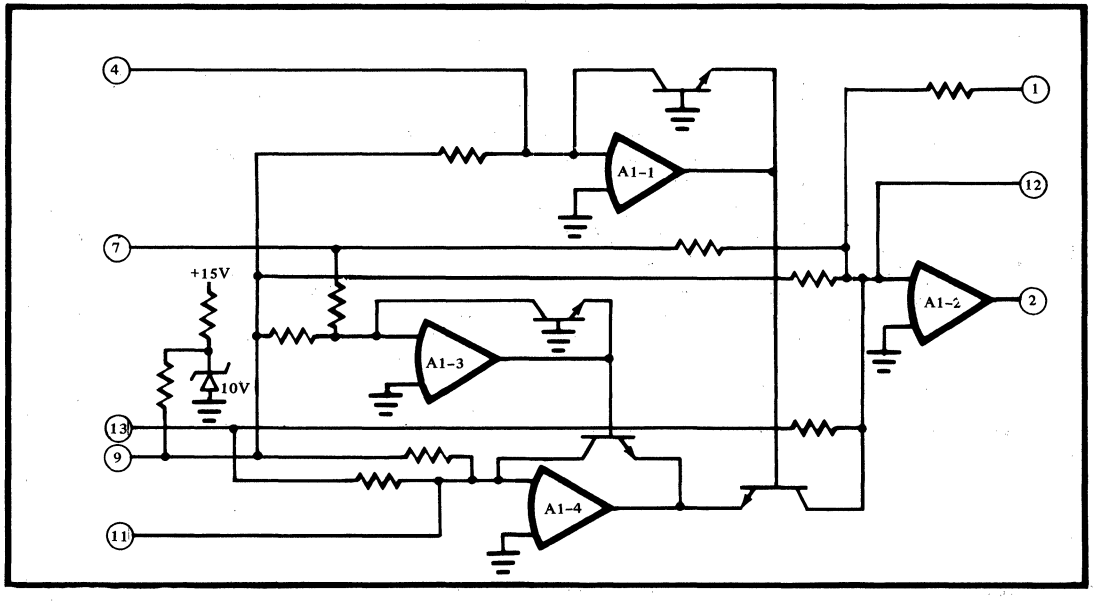
The 4206 is a four-quadrant analog multiplier offering high accuracy, low noise, and moderate bandwidth at low cost. It uses the log/antilog technique and is internally laser-trimmed and multiply mode accuracies of 0.25% and 0.5% max, are guaranteed with no external components. By following the external trim procedure described in Multiplication section, accuracies can be improved to 0.1% and 0.2% typ. Accuracy specifications are verified at Burr-Brown by an automatic tester which scans the X-Y plane. Maximum error at any points in the plane is required to be less than the specified values.

The 4206 also performs the divide function in two quadrants and the square root function in one quadrant with no external components required. Detailed instructions for these operations are given on the last page.

THEORY OF OPERATION

The 4206's log-antilog multiplication technique is based upon the logarithmic voltage-current relationship in a semiconductor junction. This action is shown by the simplified equation: $V_{be} = (\frac{KT}{q})(\ln I_c - \ln I_s)$

where V_{be} is the transistor's emitter-base voltage, I_c is the transistor collector current, I_s is the collector saturation current, K is Bolzmann's constant, q is the charge of one electron and T is the absolute temperature in degrees Kelvin. As can be seen from the equation, the logarithmic function is extremely temperature sensitive. The 4206, however, has excellent temperature characteristics because the log and antilog circuitry have equal and opposite temperature drifts which cancel to a first order approximation. The log and antilog circuits will compensate each other to the extent that the various logging transistors are matched to each other. In the 4206 these transistors are placed adjacently on a monolithic chip to obtain the best possible matching and so the best possible performance.



SPECIFICATIONS

Typical performance at +25°C with rated power supplies unless otherwise noted.
Per cent specifications refer to % of full scale (10V).

ELECTRICAL

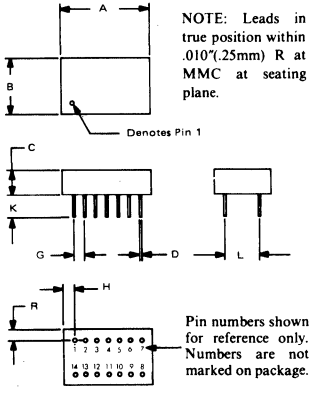
MODEL	4206J	4206K
OUTPUT FUNCTION	$\frac{E_x E_y}{10}$	*
TOTAL ERROR (Multiply Mode)**		
Internal trim, max †	0.5% max	0.25% max
External trim, typ	0.2%	0.1%
vs. Temperature	0.01%/°C	*
vs. Supply	0.02%/%	*
INDIVIDUAL ERRORS (Multiply Mode)		
Output Offset X=Y=0	15 mV	5 mV
Scale Factor Error	0.2%	0.1%
Non-Linearity		
X = 20 V, p-p Y = −10 VDC Y = 20 V, p-p X = −10 VDC	0.005%	*
X = 20 V, p-p Y = +10 VDC Y = 20 V, p-p X = +10 VDC	0.05%	*
Feedthrough @ 50 Hz		
X = 20 V, p-p Y = 0	10 mV p-p	5 mV p-p
Y = 20 V, p-p X = 0	10 mV p-p	5 mV p-p
AC PERFORMANCE		*
Slew Rate	1 V/μsec	
−3 dB Small Signal Bandwidth	250 kHz	
1% Amplitude Error	33 kHz	
1% Vector Error (0.57° phase shift)	2.5 kHz	
Full Power Response	20 kHz	
OUTPUT NOISE X = Y = 0.0V		*
DC to 10 kHz	300 μV rms	
INPUT CHARACTERISTICS		*
Input Voltage		
Maximum for Rated Specifications X,Y,Z	±10 V	
Maximum Safe Level X,Y,Z	±Supply	
Input Impedance X/Y/Z	25kΩ/25kΩ/100kΩ	
OUTPUT CHARACTERISTICS		*
Rated Output		
Voltage, min	±10 V	
Current, min	±5 mA	
Output Impedance	1 Ω	
POWER SUPPLY REQUIREMENTS		*
Rated Supply	±15 VDC	
Operating Range	±14 to ±16 V	
Quiescent Current	+15 mA, −8.5 mA	
TEMPERATURE RANGE		*
Specification	0°C to +70°C	
Operating	-25°C to +85°C	
Storage	-55°C to + 125°C	

* Same as for 4206J

** Total error is a tested maximum and does not represent a sum of the maximum individual errors as the maximum individual errors do not occur at the same X, Y operating point.

† With output loading of 10kΩ or less.

MECHANICAL



NOTE: Leads in true position within .010"(.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

PIN SPACING: 2.5mm (0.1") ROW SPACING: 7.6mm (0.300") WEIGHT: 3.4 grams (0.12 oz.) CONNECTOR: 14-pin DIP 0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

PIN CONNECTIONS

1 E_Z
2 Output
3 $-V_S$
4 Feedthrough Adj.
5 Make No Connection
6 Make No Connection
7 E_X
8 Internal Reference
9 Make No Connection
10 Ground
11 Feedthrough Adj.
12 Offset Adj.
13 E_Y
14 $+V_S$

TYPICAL PERFORMANCE CURVES

Typical Performance @25°C and ±15 VDC

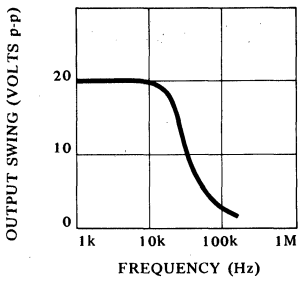


FIGURE 1. Large Signal Frequency Response

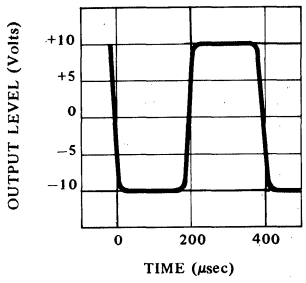


FIGURE 2. Step Response

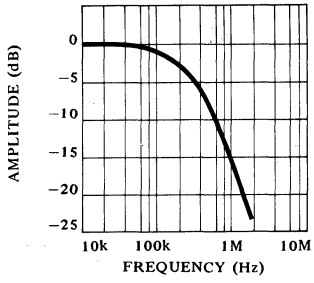


FIGURE 3. Small Signal Frequency Response

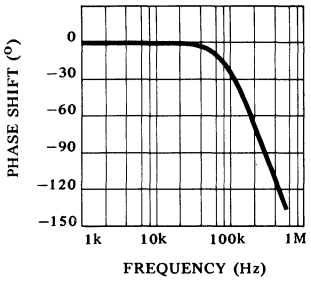


FIGURE 4. Small Signal Frequency Response

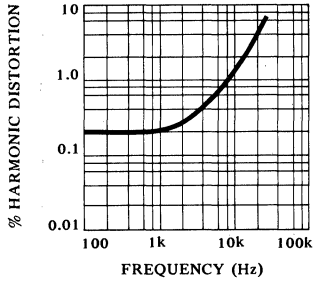


FIGURE 5. Output Distortion vs. Frequency

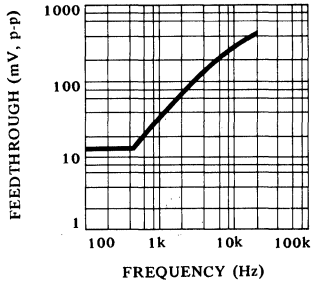


FIGURE 6. AC Feedthrough vs. Frequency

DISCUSSION OF PERFORMANCE CURVES

LARGE SIGNAL FREQUENCY RESPONSE

This response curve describes the output voltage capability of the 4206 as a function of frequency. The measurement is made with one input at +10 or −10 VDC, and with a sine wave applied at the other input. An output distortion of 0.5% is allowed.

STEP RESPONSE

Step response is measured with one input at +10 or −10VDC and with a 20 volt p-p square wave applied at the other input.

SMALL SIGNAL FREQUENCY RESPONSE

These curves are the amplitude and phase response of the 4206's transfer function, when one input is held at +10 or −10 VDC. A sine wave signal is applied to the other input. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

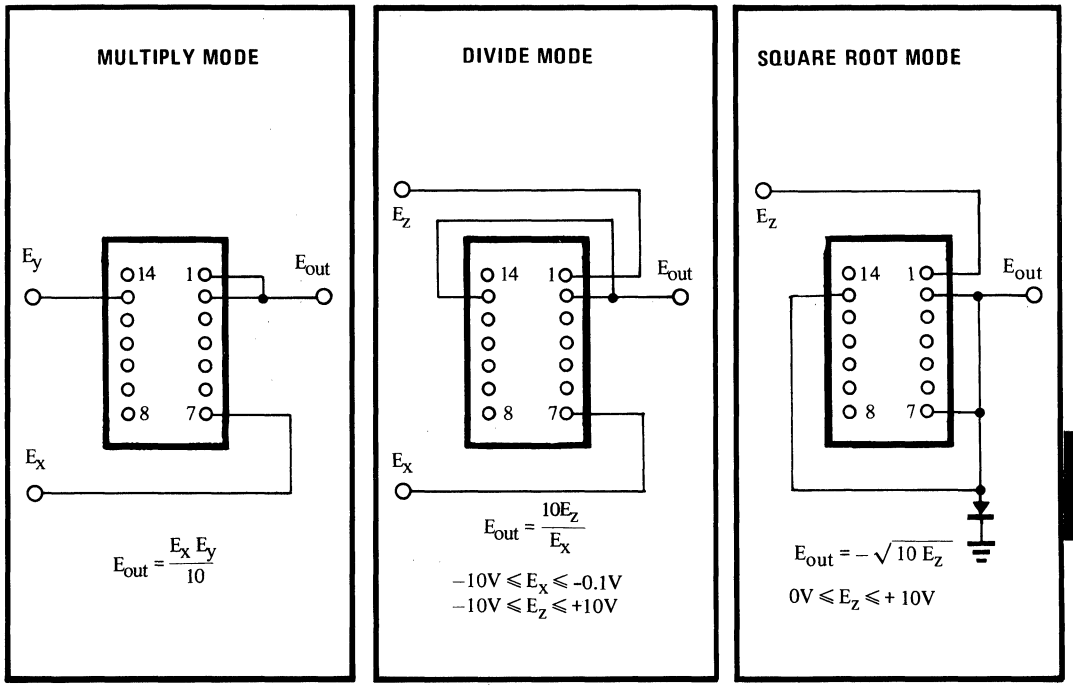
OUTPUT DISTORTION

The output distortion of the 4206 is of most interest in modulator applications. The curve of Figure 5 characterizes this distortion with one input of the 4206 held at +10 or −10 VDC. A sine wave is applied to the other input. The sine wave amplitude is held constant at 20 volts p-p while frequency is varied.

AC FEEDTHROUGH

The variation of feedthrough as a function of frequency is illustrated by Figure 6. One of the inputs is a zero while a 20 volt p-p sine wave is applied at the other input. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

OPERATING MODES



4206

ADJUSTMENTS

Although the 4206 will achieve specified performance in the multiply mode with no external trimming, optimized performance can be achieved with external adjustments. The proper connections and the trim procedures are explained below.

The 4206 will operate within specification with any combination of input signals. The best performance, however, will be obtained in the 2nd, 3rd and 4th quadrants. That is if four quadrant operations are not needed, the performance of the 4206 can be optimized by constraining operation to quadrants 2, 3 and 4 rather than 1.

MULTIPLICATION

MULTIPLICATION TRIM PROCEDURE (FIG. 7)

1) Set $E_x = 0$ and apply a 10 volt peak-peak sine wave (50 Hz) to E_y: Adjust R_1 for minimum output.
2) Set $E_y = 0$ and apply a 10 volt peak-to-peak sine wave (50 Hz) to E_x: Adjust R_2 for minimum output.
3) Set $E_x = E_y = 0$: Adjust R_3 for $E_{out} = 0.000$ V.
4) Set $E_x = E_y = +10.000$ V ± 1 mV: Adjust R_4 for $E_{out} = +10.000$ V ± 2 mV.

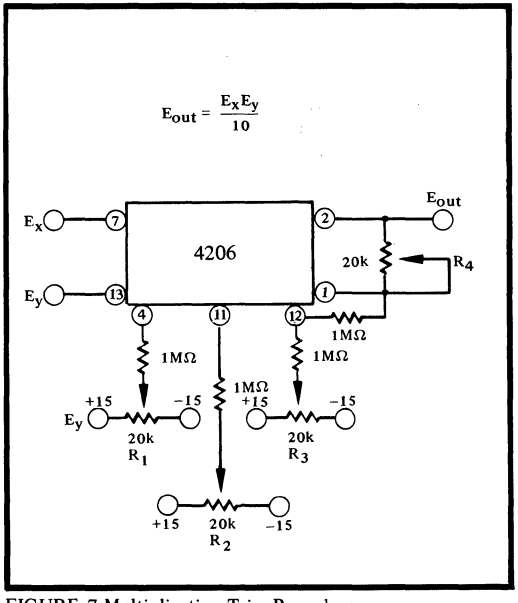


FIGURE 7 Multiplication Trim Procedure

DIVISION

The 4206 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that the maximum output error is approximately given by

$$\text{divider error} \approx \frac{10\epsilon_m}{Ex}$$

where ϵ_m is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of E_X. A 10:1 denominator range is usually the practical limit. If accurate division is required over a wide dynamic range of denominator voltage, the Burr-Brown model DIV100 is recommended (0.25%, max., over a 40:1 range).

DIVISION TRIM PROCEDURE (FIG. 8)

1) Set all potentiometers near mid-scale.
2) Set E_Z = 0 volt, $E_X \approx -10$ V, adjust R_2 such that E_O = 0.000 V ±2 mV.
3) Set $E_X = E_Z$ = -10.000VDC ±2 mV, adjust R_3 such that E_O = +10.000VDC ±2 mV.
4) Set $E_X = E_Z \approx$ minimum value required by application, adjust R_1 such that E_O = +10.000VDC ±5 mV.
5) Repeat steps (2) through (4) if necessary.

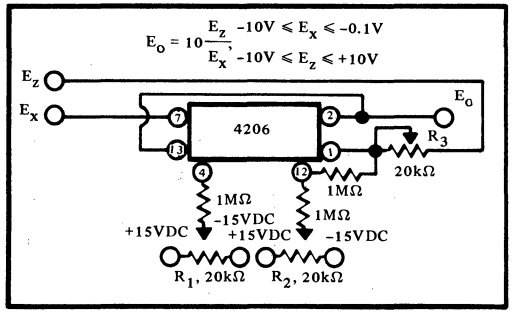


FIGURE 8 Division Trim Procedure

SQUARE ROOT TRIM PROCEDURE (FIG. 9)

1) Set E_Z = +10.000VDC ±2 mV, adjust R_2 such that E_O = +10.000VDC ±2 mV.
2) Set $E_Z \approx$ minimum value required by application (E_{Zm}) adjust R_1 such that $E_O = -\sqrt{10\,E_{Zm}}$ ±2 mV.
3) Repeat steps (1) and (2) if necessary.

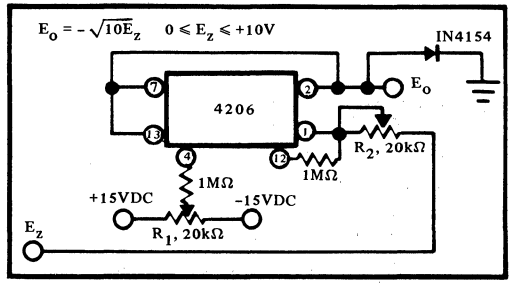


FIGURE 9 Square Root Trim Procedure

SQUARE ROOT

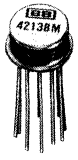
The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node. Errors in the Square Root mode of operation become troublesome for small values of E_Z. However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of E_Z is given approximately by

$$E_{out} \approx -\sqrt{10E_Z + 10\epsilon_m}$$

where ϵ_m is the total error specified for Multiply mode. This equation can be used to determine the feasibility of using the 4206 as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, the Model 4302 multifunction converter is recommended.

BURR-BROWN®

4213



MULTIPLIER-DIVIDER

FEATURES

- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- LOW NOISE
  120μV, rms, 10Hz to 10kHz
- SELF-CONTAINED
  No additional amplifiers
- SMALL SIZE
  Hermetic TO-100 package
- WIDE TEMPERATURE OPERATION

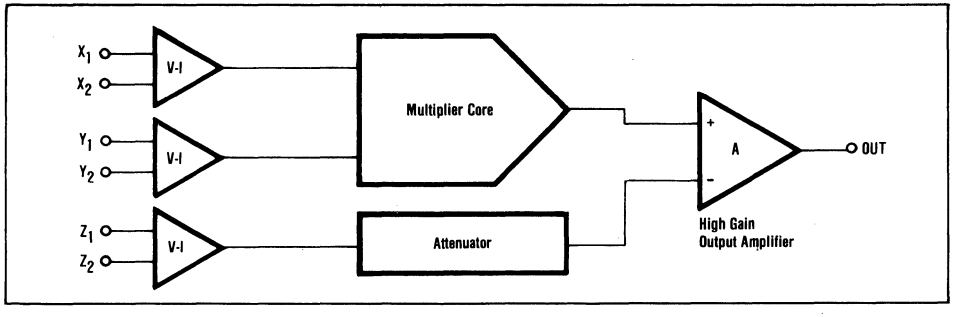
APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The 4213 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers. The 4213 is laser-trimmed to guarantee its rated accuracy with no external components. The internal zener regulated references make the 4213 much less sensitive to supply variation than earlier IC multipliers. Hermetic TO-100 package, wide operating temperature range, low output noise, and low cost are some of the desirable features of this versatile device.

4213 FUNCTIONAL DIAGRAM



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PDS-366D

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

MODEL		4213AM			4213BM			4213SM			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
MULTIPLIER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$			*			*		
Total Error	-10V ≤ X, Y ≤ 10V										
Initial	T_A = +25°C			±1.0			±0.5			±0.5	% FSR
vs Temperature	-25°C ≤ T_A ≤ +85°C		±0.008	±0.02		*	*		--	--	% FSR/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--	--		--	--		±0.025	±0.05	% FSR/°C
vs Supply			±0.05			*			*		% FSR/%
Individual Errors											
Output Offset											
Initial	T_A = +25°C		±10	±50		±7	±25		±7	±25	mV
vs Temperature	-25°C ≤ T_A ≤ +85°C		±0.7	±2.0		±0.3	±0.7		--	--	mV/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--	--		--	--		±0.3	±0.7	mV/°C
vs Supply			±0.25			*			*		mV/%
Scale Factor Error											
Initial	T_A = +25°C		±0.12			*			*		% FSR
vs Temperature	-25°C ≤ T_A ≤ +85°C		±0.008			*			--		% FSR/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--			--			±0.008		% FSR/°C
vs Supply			±0.05			*			*		% FSR/%
Nonlinearity											
X Input	X = 20V, p-p; Y = ±10VDC		±0.08			*			*		% FSR
Y Input	Y = 20V, p-p; X = ±10VDC		±0.01			*			*		% FSR
Feedthrough	f = 50Hz										
X Input	X = 20V, p-p; Y = 0		30			*			*		mV, p-p
Y Input	Y = 20V, p-p; X = 0		6			*			*		mV, p-p
vs Temperature	-25°C ≤ T_A ≤ +85°C		0.1			*			--		mV, p-p/°C
vs Temperature	-55°C ≤ T_A ≤ +125°C		--			--			0.1		mV, p-p/°C
vs Supply			0.15			*			*		mV, p-p/%
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$		$\frac{10(Z_1 - Z_2)}{(X_1 - X_2)} + Y_2$			*			*		
Total Error (with external adjustments)	X = -10V										
	-10V ≤ Z ≤ +10V		±0.75			±0.35			±0.35		% FSR
	X = -1V										
	-1V ≤ Z ≤ +1V		±2.0			±1.0			±1.0		% FSR
	-10V ≤ X ≤ -0.2V										
	-10V ≤ Z ≤ +10V		±5.0			±1.0			±1.0		% FSR
SQUARER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)^2}{10} + Z_2$			*			*		
Total Error	-10V ≤ X ≤ +10V		±0.6			±0.3			±0.3		% FSR
SQUARE-ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$		$+\sqrt{10(Z_2 - Z_1)}$			*			*		
Total Error	1V ≤ Z ≤ 10V		±1			±0.5			±0.5		% FSR
AC PERFORMANCE											
Small-Signal Bandwidth	±3dB		550			*			*		kHz
1% Amplitude Error	Small Signal		70			*			*		kHz
1% (0.57°) Vector Error	Small Signal		5			*			*		kHz
Full Power Bandwidth	$\|V_o\|$ = 10V, R_L = 2kΩ		320			*			*		kHz
Slew Rate	$\|V_o\|$ = 10V, R_L = 2kΩ		20			*			*		V/μsec
Settling Time	ε = ±1%, ΔVo = 20V		2			*			*		μsec
Overload Recovery	50% Output Overload		0.2			*			*		μsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Rated Operation		±10			*			*			V
Absolute Maximum				±V_{CC}			*			*	V
Input Resistance	X, Y, Z(1)		10			*			*		MΩ
Input Bias Current	X, Y, Z		1.4			*			*		μA
OUTPUT CHARACTERISTICS											
Rated Output											
Voltage	I_o = ±5mA	±10			*			*			V
Current	V_o = ±10V	±5			*			*			mA
Output Resistance	f = DC		1.5			*			*		Ω
OUTPUT NOISE VOLTAGE	X = Y = 0										
f_o = 1Hz			40			*			*		μV/√Hz
f_o = 10kHz			1.0			*			*		μV/√Hz
1/f Corner Frequency			1060			*			*		Hz
f_B = 10Hz to 10kHz			125			*			*		μV, rms
f_B = 10Hz to 10MHz			3			*			*		mV, rms
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*			*		VDC
Operating Range	Derated Performance	±8.5		±20	*		*	*		*	VDC
Quiescent Current			±5.5			*			*		mA

ELECTRICAL (CONT)

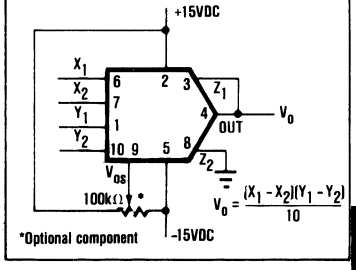
MODEL		4213AM			4213BM			4213SM			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE (Ambient)											
Specification	Derated Performance	-25		+85	*		*	-55		+125	°C
Operating Range		-55		+125	*		*	*		*	°C
Storage		-65		+150	*		*	*		*	°C

NOTES:

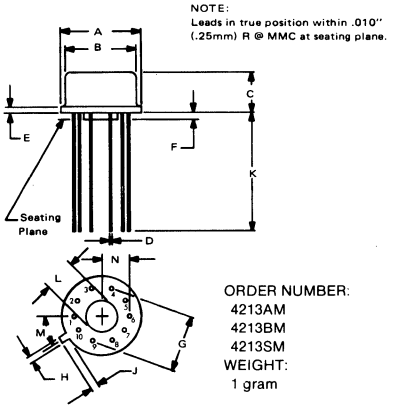
1. Z_2 input resistance is 10MΩ, typical, with Pin 9 open. If Pin 9 is grounded or used for optional offset adjustment, the Z_2 input resistance may be as low as 25kΩ.

*Same as 4213AM specification.

CONNECTION DIAGRAM



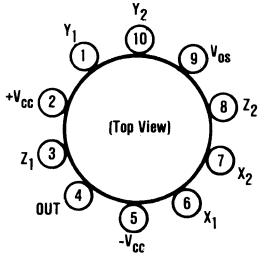
MECHANICAL



ORDER NUMBER:
4213AM
4213BM
4213SM
WEIGHT:
1 gram

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

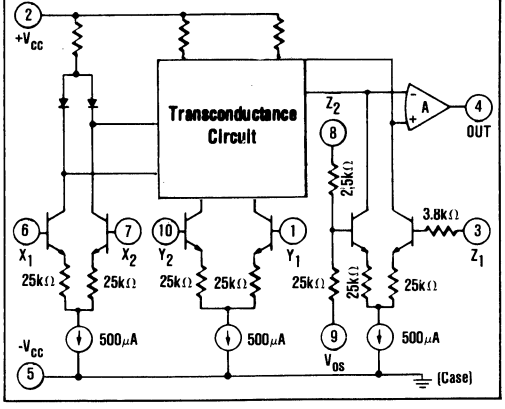
PIN CONFIGURATION



NOTES:

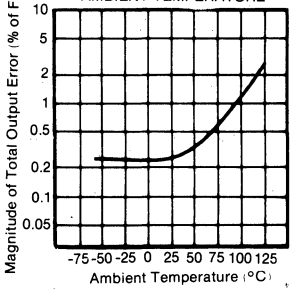
1. V_{OS} adjustment optional not normally recommended. V_{OS} pin may be left open or grounded.
2. All unused input pins should be grounded.
3. Pin 5 is connected to the case.

SIMPLIFIED SCHEMATIC

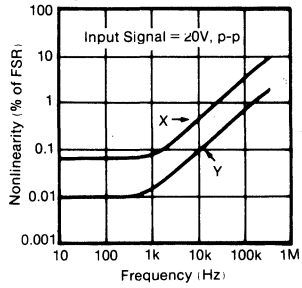


TYPICAL PERFORMANCE CURVES

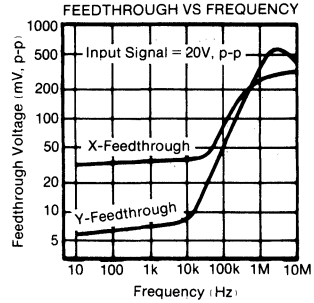
TOTAL ERROR VS AMBIENT TEMPERATURE



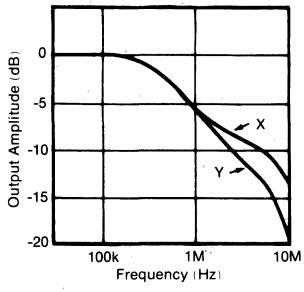
NONLINEARITY VS FREQUENCY



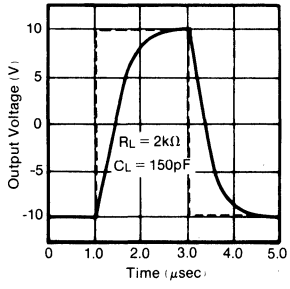
FEEDTHROUGH VS FREQUENCY



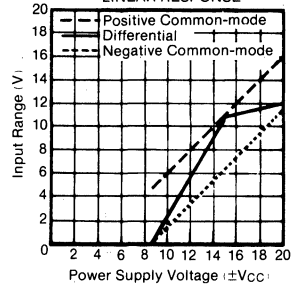
OUTPUT AMPLITUDE VS FREQUENCY



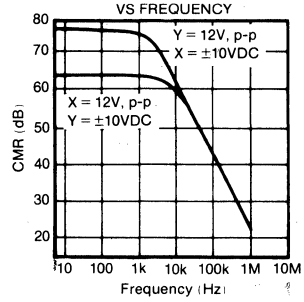
LARGE SIGNAL RESPONSE



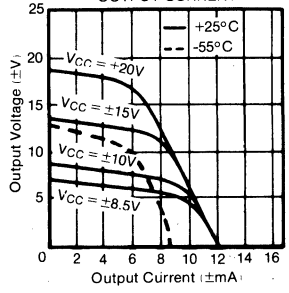
INPUT VOLTAGE FOR LINEAR RESPONSE



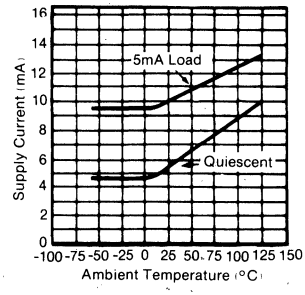
COMMON-MODE REJECTION VS FREQUENCY



OUTPUT VOLTAGE VS OUTPUT CURRENT



SUPPLY CURRENT VS AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-circuit Duration(3)	Continuous
Junction Temperature	+150°C

NOTES:
1. Package must be derated based on: θ_{JC} = 55°C/W and θ_{JA} = 165°C/W.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground only. Rating applies to +85°C ambient.

DEFINITIONS

TOTAL ERROR (Accuracy)

Total error is the actual departure of the multiplier output voltage from the ideal product of its input voltages. It includes the sum of the effects of input and output DC offsets, gain error and nonlinearity.

OUTPUT OFFSET

Output offset is the output voltage when both inputs V_X and Y_Y are zero volts.

SCALE FACTOR ERROR

Scale factor error is the difference between the actual scale factor and the ideal scale factor.

NONLINEARITY

Nonlinearity is the maximum deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

FEEDTHROUGH

Feedthrough is the signal at the output for any value of V_X or V_Y within the rated range, when the other input is zero.

SMALL SIGNAL BANDWIDTH

Small signal bandwidth is the frequency at which the output is down 3dB from its low frequency value for a nominal output amplitude of 10% of full scale.

1% AMPLITUDE ERROR

The 1% amplitude error is the frequency the output amplitude is in error by 1%, measured with an output amplitude of 10% of full scale.

1% VECTOR ERROR

The 1% vector error is the frequency at which a phase error of 0.01 radians (0.57°) occurs. This is the most sensitive measure of dynamic error of a multiplier.

APPLICATIONS INFORMATION

MULTIPLICATION

Figure 1 shows the basic connection for four-quadrant multiplication.

The 4213 meets all of its specifications without trimming. Accuracy can, however, be improved by nulling the output offset voltage using the 100kΩ optional balance potentiometer shown in Figure 1.

AC feedthrough may be reduced to a minimum by applying an external voltage to the X or Y input as shown in Figure 2.

Z_2, the optional summing input, may be used to sum a voltage into the output of the 4213. If not used, this terminal, as well as the X and Y input terminals, should be grounded. All inputs should be referenced to power supply common.

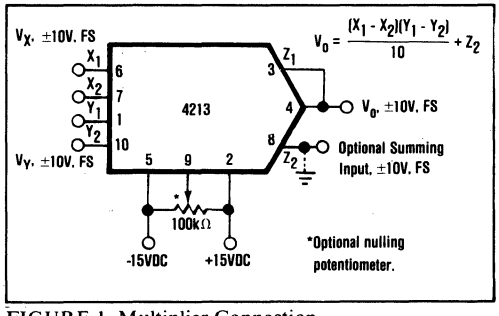


FIGURE 1. Multiplier Connection.

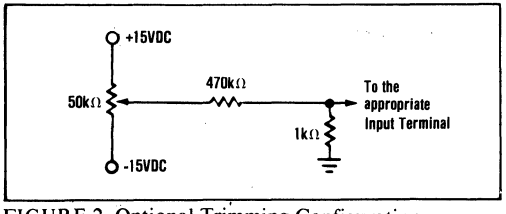


FIGURE 2. Optional Trimming Configuration.

Figure 3 shows how to achieve a scale factor larger than the nominal 0.1. In this case, the scale factor is unity which makes the transfer function

$$V_o = KV_XV_Y = K(X_1 - X_2)(Y_1 - Y_2)$$
$$K = [1 + (R_1/R_2)]/10$$
$$0.1 \leq K \leq 1$$

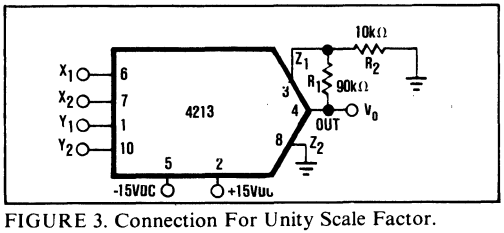


FIGURE 3. Connection For Unity Scale Factor.

This circuit has the disadvantage of increasing the output offset voltage by a factor of 10 which may require the use of the optional balance control for some applications. In addition, this connection reduces the small signal bandwidth to about 50kHz.

DIVISION

Figure 4 shows the basic connection for two-quadrant division. This configuration is a multiplier-inverted analog divider, i.e., a multiplier connected in the feedback loop of an operational amplifier. In the case of the 4213 this operational amplifier is the output amplifier of the multiplier itself.

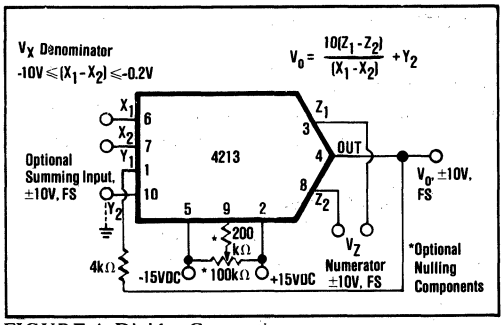


FIGURE 4. Divider Connection.

The divider error with a multiplier-inverted analog divider is approximately

$$\epsilon_{divider} = 10\,\epsilon_{multiplier}/(X_1 - X_2).$$

It is obvious from this error equation that divider error becomes excessively large for small values of $X_1 - X_2$. A 10-to-1 denominator range is usually the practical limit. If more accurate division is required over a wide range of denominator voltages, an externally generated voltage may be applied to the unused X-input (see Optional Trim Configuration). To trim, apply a ramp of +100mV to +1V at 100Hz to both X_1 and Z_1 if X_2 is used for offset adjustment, otherwise reverse the signal polarity, and adjust the trim voltage to minimize the variation in the output. An alternative to this procedure would be to use the Burr-Brown DIV100, a precision log-antilog divider.

SQUARING

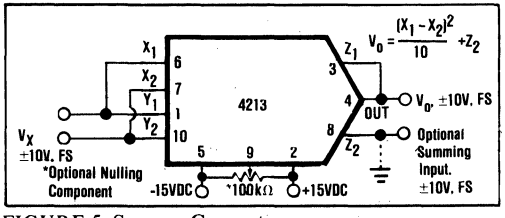


FIGURE 5. Squarer Connection.

SQUARE ROOT

Figure 6 shows the connection for taking the square root of the voltage V_Z. The diode prevents a latching condition which could occur if the input momentarily changed polarity. This latching condition is not a design flaw in the 4213, but occurs when a multiplier is connected in the feedback loop of an operational amplifier to perform square root functions.

The load resistance R_L must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$. This resistance must be in the circuit as it provides the current necessary to operate the diode.

The output offset should be nulled for optimum performance by allowing the input to be its smallest expected value and adjusting R_1 for the proper output voltage.

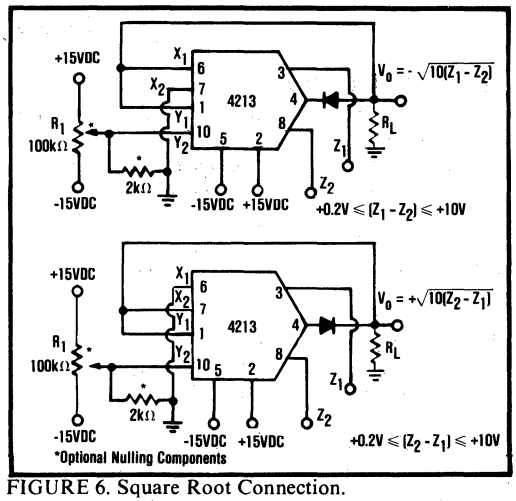


FIGURE 6. Square Root Connection.

This will improve the square root mode accuracy to about that of the multiply mode.

BRIDGE LINEARIZATION

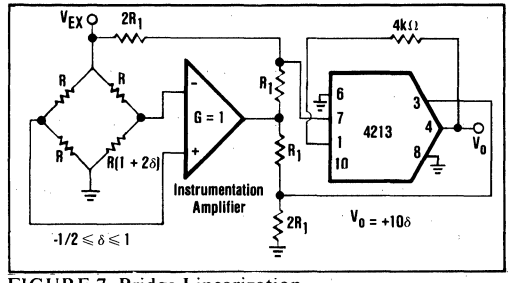


FIGURE 7. Bridge Linearization.

The use of the 4213 and the instrumentation amplifier to linearize the output from a bridge circuit makes the output V_O independent of the bridge supply voltage.

TRUE RMS-TO-DC CONVERSION

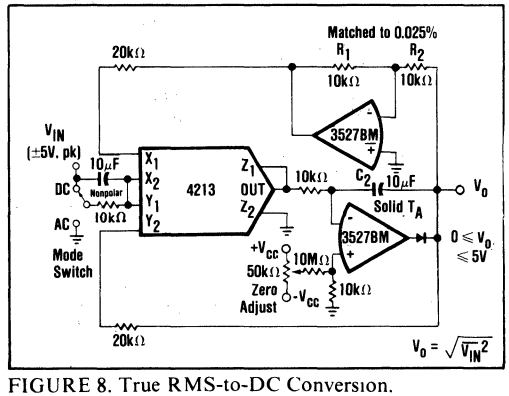


FIGURE 8. True RMS-to-DC Conversion.

The RMS-to-DC conversion circuit of Figure 8 gives greater accuracy and bandwidth but with less dynamic range than most rms-to-DC converters.

PERCENTAGE COMPUTATION

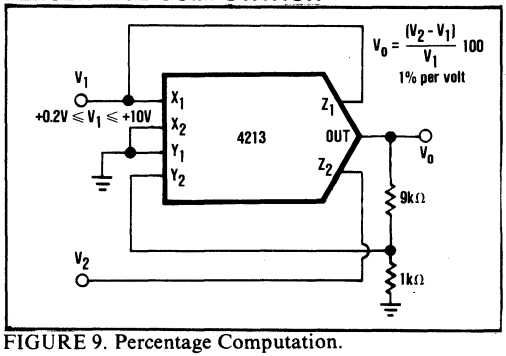


FIGURE 9. Percentage Computation.

The circuit of Figure 9 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1.

SINE FUNCTION GENERATOR

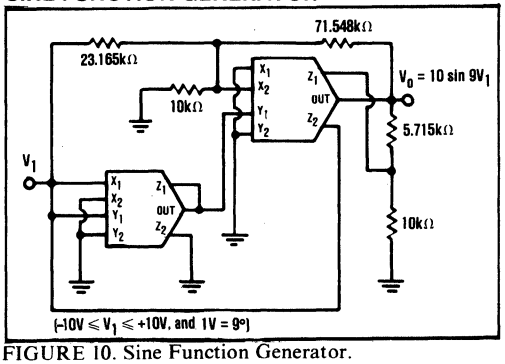


FIGURE 10. Sine Function Generator.

The circuit in Figure 10 uses implicit feedback to implement the following sine function approximation:

$$V_o = (1.5715V_1 - 0.004317V_1^3)/(1 + 0.001398V_1^2)$$
$$= 10 \sin (9V_1).$$

SINGLE-PHASE POWER MEASUREMENT

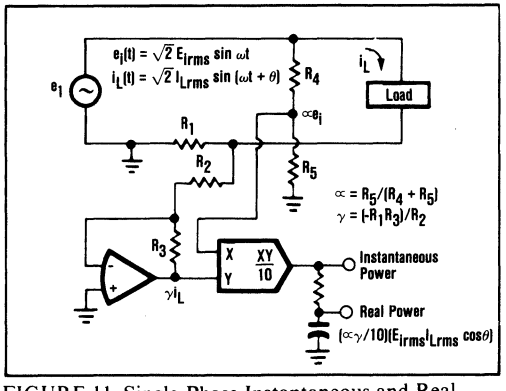


FIGURE 11. Single-Phase Instantaneous and Real Power Measurement.

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins of the 4213 to the power supply common. The connection of these capacitors should be as close to the 4213 as practical.

CAPACITIVE LOADS

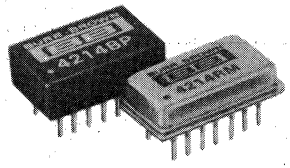
Stable operation is maintained with capacitive loads to 1000pF in all modes typically, except the square root mode for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the 4213's output.

MORE CIRCUITS

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the Burr-Brown/ McGraw Hill book "FUNCTION CIRCUITS - Design and Applications."

BURR-BROWN®

4214



MULTIPLIER - DIVIDER

FEATURES

- DIFFERENTIAL INPUTS
- LASER-TRIMMED
- GUARANTEED ACCURACY
  0.5% and 1%
- SELF-CONTAINED
  No additional parts required
- LOW NOISE
  120μV rms, 10Hz - 10kHz
- DIP PACKAGES

APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOTING
- ADAPTIVE CONTROL
- ALGEBRAIC COMPUTATION
- POWER COMPUTATION

DESCRIPTION

The 4214 family of multipliers are low cost integrated circuit multiplier/dividers designed for general purpose usage. In addition to four quadrant multiplication, they also perform division and square rooting of analog signals. They do not require use of additional amplifiers to perform these functions. The 4214 is laser-trimmed prior to final packaging and is guaranteed to its rated accuracy with no external components - a distinct advantage from standpoints of cost and reliability.

4214 contains its own zener regulated references and, as a result is much less sensitive to supply voltage variation than were earlier IC multipliers. The multipliers' output noise is only 120μV rms in a 10Hz to 10kHz bandwidth.

The unit is available in two 14 pin DIP packages. The plastic version ("P" package) is offered for minimum cost and is specified over the -25°C to +85°C range. The hermetic metal package ("M" package option) provides operation over the full -55°C to +125°C temperature range.

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PDS-395

ELECTRICAL SPECIFICATIONS

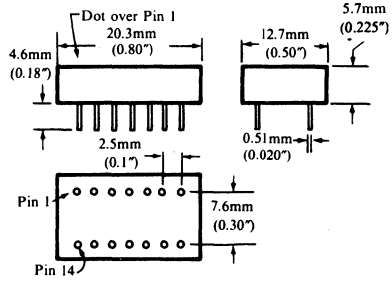
Typical performance at +25°C with rated power supplies unless otherwise noted.

MODEL	4214AP/RM	4214BP/SM
OUTPUT FUNCTION	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$	
TOTAL ERROR[1]		
Without Trimming	1% max	0.5% max
Error vs Temperature (-25°C to +85°C), (AP and BP)	0.008%/°C typ., 0.02%/°C max	
(-55°C to +125°C), (RM and SM)	0.025%/°C typ., 0.05%/°C max	
Error vs Supply	0.05%/%	
INDIVIDUAL ERRORS		
Output Offset	10mV typ	7mV typ
	50mV max	25mV max
vs Temperature	0.7mV/°C typ	0.3mV/°C typ
	2mV/°C max	0.7mV/°C max
vs Supply	0.25mV/%	
Scale Factor Error	0.12%	
vs Temperature	0.008%/°C	
vs Supply	0.05%/%	
Nonlinearity		
X(X = 20V p-p, Y = ±10VDC)	±0.08%	
Y(Y = 20V p-p, X = ±10VDC)	±0.01%	
Feedthrough at 50 Hz		
X = 20V p-p, Y = 0	30mV p-p	
Y = 20V p-p, X = 0	6mV p-p	
vs Temperature	0.1mV p-p/°C	
vs Supply	0.15mV p-p/%	
AC PERFORMANCE		
Small Signal ±3dB Flatness	550kHz	
Small Signal ±1% Flatness	70kHz	
Small Signal ±1% Vector Error (0.57° Phase Shift)	5kHz	
Full Power Bandwidth	320kHz	
Slew Rate	20V/μs	
Settling Time to 1% (20V step)	2/μs	
OUTPUT NOISE (X = Y = 0)		
10 Hz to 10 kHz	120μV rms	
10 Hz to 10 MHz	700μV rms	
INPUT CHARACTERISTICS		
Input Voltage Range		
Rated Operation, min.	±10V	
Absolute max	±V$_s$	
Input Impedance, X, Y, Z[2]	10 MΩ	
Input Bias Current, X, Y, Z	1.4μA	
OUTPUT CHARACTERISTICS		
Rated Output	±10V at ±5mA min	
Output Impedance	1.5Ω	
POWER SUPPLY REQUIREMENTS		
Rated Voltage	±15V	
Operating Range	±8.5VDC to ±20VDC	
Quiescent Current	±5.5mA	
TEMPERATURE RANGE	AP and BP	-25°C to +85°C
Rated Performance (specification)	RM and SM	-55°C to +125°C
Operation		-55°C to +125°C
Storage		-65°C to +150°C

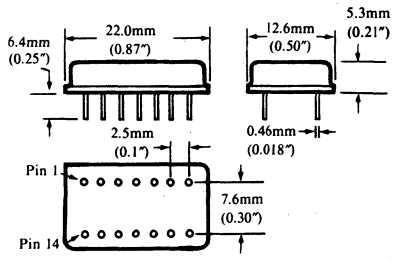
1. Total error is the maximum allowed value of the sum of the individual errors.
2. Z_2 input impedance is 10 MΩ typ with Pin 11 open circuit. If Pin 11 is grounded or used for optional offset adjustment the Z_2 input impedance may become as low as 25kΩ.

MECHANICAL

4214AP, 4214BP
Weight: 2.9 grams (0.10 oz.)

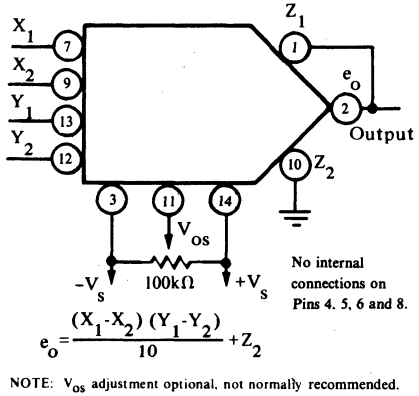


4214RM, 4214SM
Weight: 3.9 grams (0.13 oz.)



Connector: 0145MC (14-pin DIP)
Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

CONNECTION DIAGRAM



No internal connections on Pins 4, 5, 6 and 8.

$$e_o = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$$

NOTE: V_{os} adjustment optional, not normally recommended. Pin 11 may be left open or grounded.

4214

TYPICAL PERFORMANCE CURVES

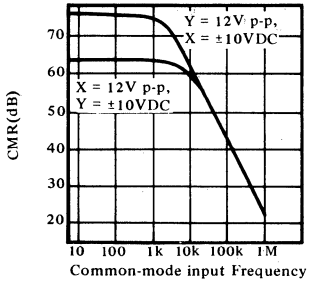


FIGURE 1. Common-mode Rejection vs. Frequency.

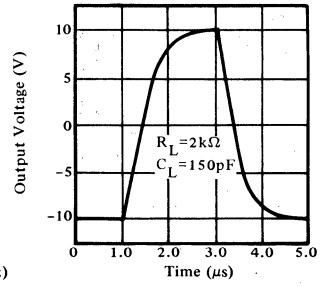


FIGURE 2. Step Response.

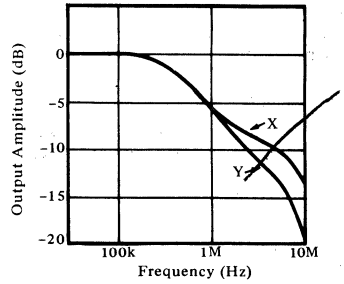


FIGURE 3. Small-signal Frequency Response.

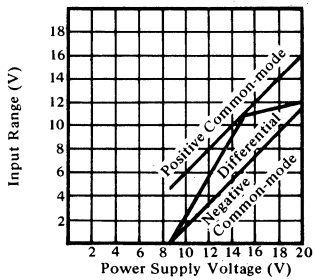


FIGURE 4. Input Range for Linear Response.

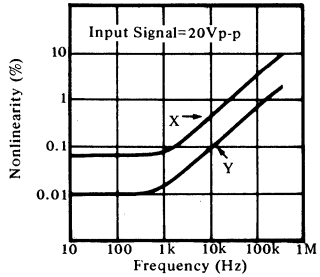


FIGURE 5. Nonlinearity vs. Frequency.

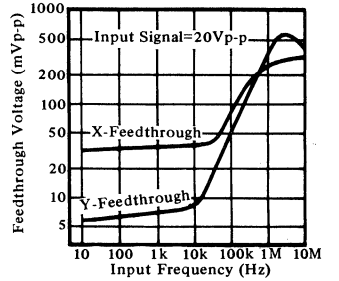


FIGURE 6.Feedthrough vs. Frequency.

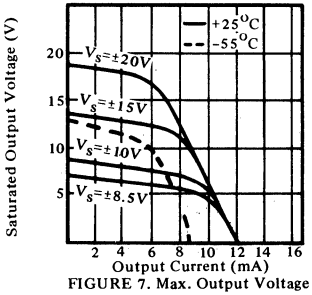


FIGURE 7. Max. Output Voltage vs. Output Current.

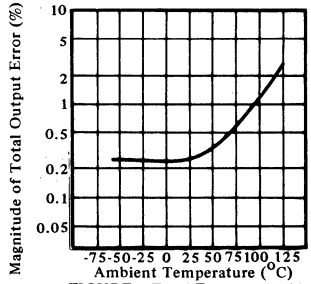


FIGURE 8.Total Error vs. Ambient Temperature.

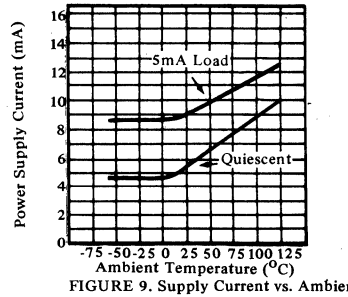


FIGURE 9. Supply Current vs. Ambient Temperature.

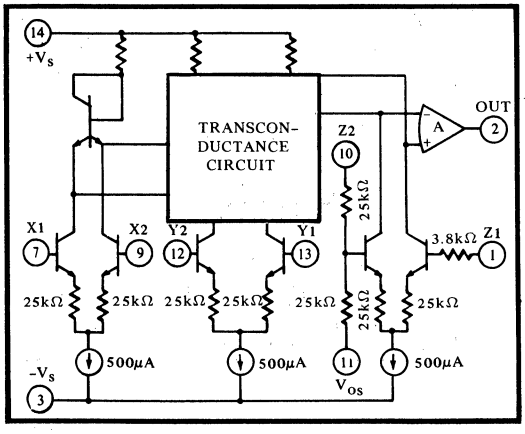


FIGURE 10. Simplified Equivalent Circuit.

OPERATING MODES MULTIPLICATION

The 4214 is a general purpose multiplier/divider with three sets of differential inputs viz. X, Y, and Z. Its open-loop transfer function is

$$e_o = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2)\right]$$

where, A is the open-loop gain of the internal output amplifier (see the simplified equivalent circuit, Figure 10). Due to very high gain ($A \rightarrow \infty$) of the output amplifier the feedback from the output to any of the inputs will establish the relationship

$$Z_1 - Z_2 = (X_1 - X_2)(Y_1 - Y_2)/10$$

Taking output at Z_1 the multiplication mode transfer function is obtained and is expressed as

$$e_o = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2.$$

This connection of 4214 is shown on the previous page.

DIVISION

The 4214 may be used as a two quadrant divider, without the need for an external op amp. Note that the maximum output error in the divide mode is given approximately by,

$$\text{Divider error} \simeq \frac{10 \in m}{X_1 - X_2}, \text{ where } \in m \text{ is}$$

the total error specified for the multiply mode. The divider error, as shown above, becomes excessively large for small values of $(X_1 - X_2)$. A 10:1 denominator range is usually the practical limit. This is true for all such units, where a multiplier is used in voltage feedback mode to generate "divide" function.

If more accurate division is required over wide range of denominator voltages, the Burr-Brown model DIV100 is recommended (0.25% max error over 40:1 range).

For optimum performance, the Z offset should be nulled by letting the input be zero and adjusting R_1 for zero output. This offset adjustment will improve the divider error to about $\frac{3 \in m}{(X_1 - X_2)}$ for $(X_1 - X_2)$ much less than 10V.

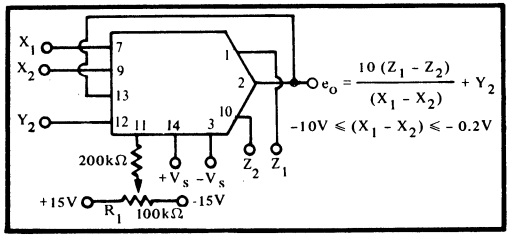


FIGURE 11. Divide Mode Connections - 4214.

SQUARE ROOT

By applying feedback from the output to both the X and Y inputs, the square root function can be obtained. The errors in the square root mode become large for small values of Z input. The actual output is approximately

$$\text{Square root output } e_o = \sqrt{10 (Z_1 - Z_2) + 10 \in m}$$

where $\in m$ is the total error for the multiply mode.

Burr-Brown's multifunction converter model 4302 is recommended for applications requiring more accuracy over wider dynamic range.

The output offset should be nulled for optimum performance by allowing the input to be its smallest expected value and adjusting R_1 for the proper output voltage.

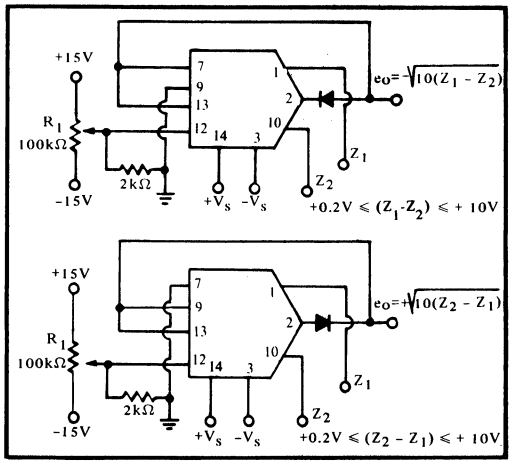


FIGURE 12. Square Root Mode Connections - 4214.

SINE FUNCTION GENERATOR

Two 4214's can be connected with implicit feedback as shown in Figure 13 to implement the following sine function approximation.

$$e_o = \frac{1.5715\, e_i - 0.004317\, e_i^3}{1 + 0.001398\, e_i^2} = 10 \text{ Sin } 9\, e_i$$

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the new Burr-Brown/McGraw Hill book "FUNCTION CIRCUIT - Design and Applications."

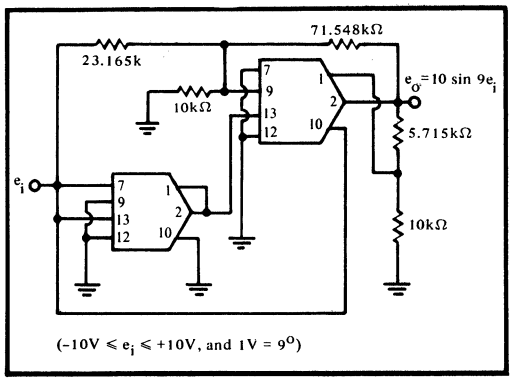
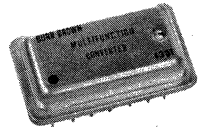


FIGURE 13. Sine Function Connections - 4214.

BURR-BROWN®

4301



Low Cost MULTIFUNCTION CONVERTER

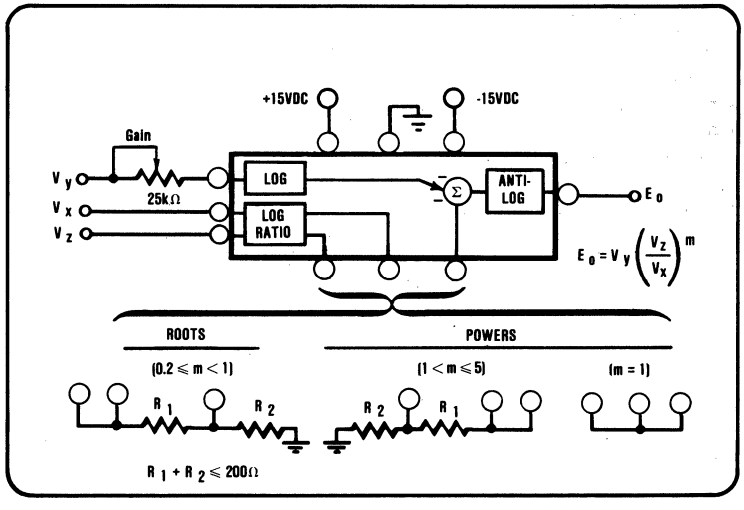
FEATURES

- LOW COST
- SMALL PACKAGE - Dual-in-line
- HERMETIC, SHIELDED PACKAGE
- UNIVERSAL CONVERTER

FUNCTIONS	ACCURACY
MULTIPLY	±0.25%
DIVIDE	±0.25%
SQUARE	±0.03%
SQUARE ROOT	±0.07%
EXPONENTIATE	±0.15% (m = 5)
ROOTS	±0.2% (m = 0.2)
SINE θ	±0.5%
COSINE θ	±0.8%
TAN^{-1} (Y/X)	±0.6%
$\sqrt{X^2 + Y^2}$	±0.07%

DESCRIPTION

Burr-Brown's multifunction converter model 4301 is a low-cost solution to many analog conversion needs. Much more than just another multiplier/divider, the 4301 out performs many analog circuit functions with a very-high degree of accuracy at a very-low total cost to the user.



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PDS-307G

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and with rated supply unless otherwise noted.

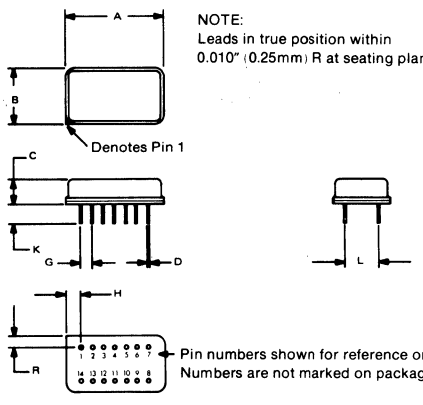
MODEL	4301
TRANSFER FUNCTION	$E_O = V_Y (V_Z/V_X)^m$
RATED OUTPUT	
Voltage	+10.0V
Current	5mA
INPUT	
Signal Range	$0 \le (V_X, V_Y, V_Z) \le +10V$
Absolute Maximum	$(V_X, V_Y, V_Z) \le \pm 18V$
Impedance (X/Y/Z)	100kΩ/90kΩ/100kΩ
EXPONENT RANGE(1)	
Roots ($0.2 \le m < 1$)	$m = \lvert R_2/(R_1 + R_2)\rvert$
Powers ($1 < m \le 5$)	$m = \lvert(R_1 + R_2)/R_2\rvert$
Powers ($m = 1$)	$R_1 = 0\Omega$, R_2 not used
POWER REQUIREMENTS	
Rated Supply	±15VDC
Range	±12VDC to ±18VDC
Quiescent Current	±10mA
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-25°C to +85°C

NOTE: 1. Refer to Figure 1.

General specifications for the Model 4301 Multifunction Converter are shown above; Figure 1 is a functional diagram. These specifications characterize the 4301 as a versatile three input multifunction converter.

Applications information to help you apply the 4301 to your particular need is shown in the product data sheet for model 4302. The dedicated circuit configurations needed to produce the multiplication, division, exponentiation, square rooting, squaring, sine, cosine, arctangent, and vector algebraic functions are shown along with information for model 4302.

MECHANICAL

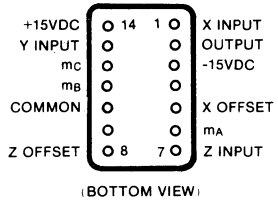


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

CASE: Kovar or equiv.
WEIGHT: 0.15 oz. (3.4 grams)
CONNECTOR: 14-pin DIP connector
Burr-Brown Model No. 0145MC)

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

PIN CONNECTIONS



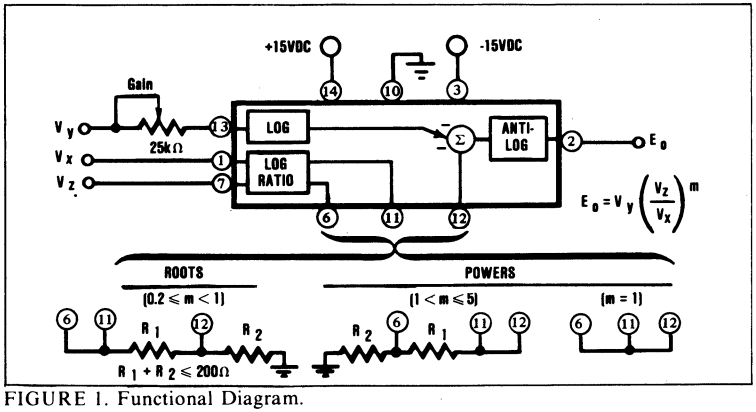


FIGURE 1. Functional Diagram.

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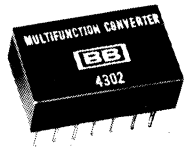

4302

Low Cost MULTIFUNCTION CONVERTER

FEATURES

- LOW COST
- SMALL PACKAGE - Dual-in-line
- RELIABLE HYBRID CONSTRUCTION
- VERSATILE

FUNCTIONS	ACCURACY
MULTIPLY	±0.25%
DIVIDE	±0.25%
SQUARE	±0.03%
SQUARE ROOT	±0.07%
EXPONENTIATE	±0.15% (m = 5)
ROOTS	±0.2% (m = .2)
SINE θ	±0.5%
COSINE θ	±0.8%
TAN $^{-1}$ (Y/X)	±0.6%
$\sqrt{X^2 + Y^2}$	±0.07%

Typical accuracies expressed as a % of output full scale (+10VDC) at 25°C.

DESCRIPTION

Burr-Brown's multifunction converter model 4302 is a low cost solution to many analog conversion needs. Much more than just another multiplier/divider, the 4302 out performs many analog circuit functions with a very high degree of accuracy at a very low total cost to the user.

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PDS-326C

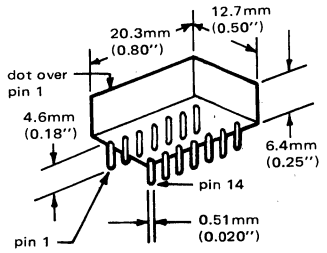
SPECIFICATIONS

Performance typical at 25°C and with rated supply unless otherwise noted.

ELECTRICAL

MODEL	4302
TRANSFER FUNCTION	$E_O = V_Y (\frac{V_Z}{V_X})^m$
RATED OUTPUT	
Voltage	+10.0 V
Current	5 mA
INPUT	
Signal Range	$0 \leq (V_X, V_Y, V_Z) \leq +10$ V
Absolute Maximum	$(V_X, V_Y, V_Z) \leq \pm 18$ V
Impedance (X/Y/Z)	100 kΩ/90 kΩ/100 kΩ
EXPONENT RANGE	
Roots ($0.2 \leq m < 1$)	$m = \frac{R_2}{R_1 + R_2}$ Refer to Functional Diagram below
Powers ($1 < m \leq 5$)	$m = \frac{R_1 + R_2}{R_2}$
($m = 1$)	$R_1 = 0\ \Omega$, R_2 not used
POWER REQUIREMENTS	
Rated Supply	±15 VDC
Range	±12 to ±18 VDC
Quiescent Current	±10 mA
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +125°C

MECHANICAL

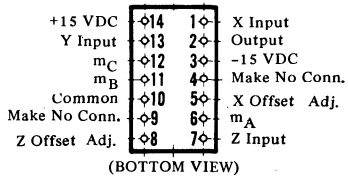


Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

4302

PIN CONNECTIONS



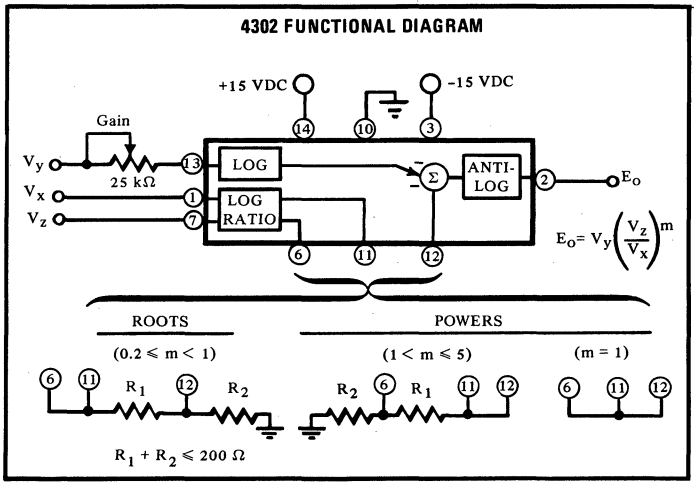
(BOTTOM VIEW)

General specifications for the Model 4302 Multifunction Converter are presented on this page. These specifications characterize the 4302 as a versatile three input multifunction converter.

The following pages are applications oriented to help you apply the 4302 to your particular circuit function need. These pages contain dedicated circuit configurations in order to produce the functions of: multiplication, division, exponentiation, square rooting, squaring, sine, cosine, arctangent, and vector algebra.

It is the purpose of this product data sheet to enable you to apply the 4302 to your analog conversion needs quickly and efficiently.

4302 FUNCTIONAL DIAGRAM



Many of the following circuit configurations using the 4302 require a reference voltage for scaling purposes. The reference voltage is shown to be +15 VDC (+15 VDC REF.) since in most cases the +15 VDC power source for the 4302 has sufficient time and temperature related stability to achieve the specified typical accuracies.

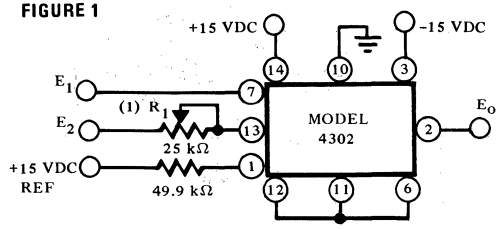
If the particular supplies which are available for powering the 4302 do not have the necessary stability for the required conversion accuracy, an additional +15 VDC precision supply may be required.

MULTIPLIER/DIVIDER FUNCTIONS

MULTIPLIER

In multiplier applications the 4302 provides high accuracy at a low cost. The 4302 accepts inputs up to +10 VDC and provides a typical accuracy of ±0.25% of full scale.

FIGURE 1



(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_o = +10.00$ VDC.

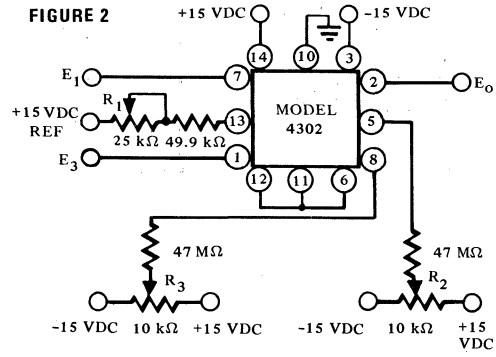
Transfer Function	$E_o = +\frac{E_1 E_2}{10}$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for input range)	$\begin{cases} 0.03V \leq E_1^* \leq 10\ V \\ 0.01\ V \leq E_2 \leq 10\ V \end{cases}$
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = E_2 = 0$)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±0.2 mV/°C
NOISE (10 Hz to 1 kHz)	100 μV rms
BANDWIDTH (E_1, E_2)	
Small Signal (-3 dB)	500 kHz
Full Output	60 kHz

DIVIDER

As a divider, the 4302 outperforms many of the multiplier/dividers on the market at a much lower cost. In the divider configuration the 4302 boasts a typical conversion accuracy of ±0.25% of full scale.

Transfer Function	$E_o = +10\ (E_1/E_3)$
ACCURACY	
Total Errors	
Typical at +25°C	±25 mV
Maximum at +25°C	±50 mV
(for $E_1 \leq E_3$ and input range)	$\begin{cases} 0.03V \leq E_1^* \leq 10\ V \\ 0.1\ V \leq E_3 \leq 10\ V \end{cases}$
vs. Temperature	±1 mV/°C
Offset Errors ($E_1 = 0$, $E_3 = +10$ V)	
Output Offset (at 25°C)	±10 mV
vs. Temperature	±1 mV/°C
NOISE (10 Hz to 1 kHz)	
$E_3 = +10$ V	100 μV rms
$E_3 = +0.1$ V	300 μV rms
BANDWIDTH (E_1, E_3)	
Small Signal (-3 dB)	500 kHz
Full Output ($E_3 = +10$ V)	60 kHz

FIGURE 2



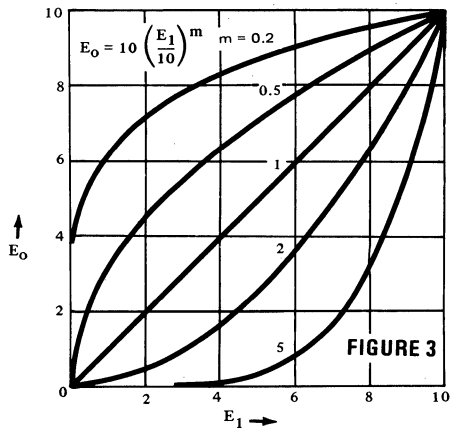
NOTES:
(1) Set R_1 so that with $E_1 = E_3 = +10.00$ VDC, $E_o = +10.00$ VDC.
(2) Set R_2 so that with $E_1 = E_3 = +0.10$ VDC, $E_o = +10.00$ VDC.
(3) Set R_3 so that with $E_1 = +0.01$ VDC and with $E_3 = +0.10$ VDC, $E_o = +1.00$ VDC.
(4) Repeat steps 1 through 3 as necessary to achieve the specified output voltages.

* The input voltage may be extended below 0.03V by connecting a 0.047 μF capacitor between pins 11 and 5, causing a slight reduction in bandwidth. (Multiply and Divide Modes).

EXPONENTIAL FUNCTIONS

Model 4302 may be used as exponentiator over a range of exponents from 0.2 to 5. The exponents 0.5 and 2, square rooting and squaring respectively, are often used functions and are treated below. Other values of exponents (m) may be useful in terms of linearization of nonlinear functions or simply for producing the mathematical conversions. Characteristics of m = 0.2 and m = 5 are presented on the right. For other values of m the curves presented in Figure 3 may be used to interpolate the error for a nonspecified value of m.

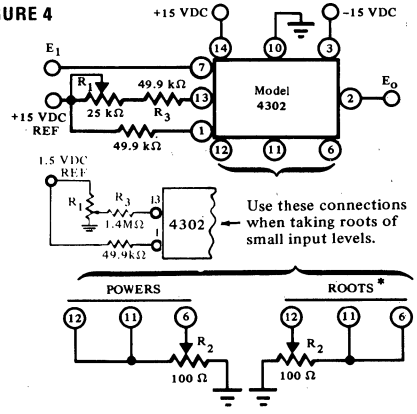
Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^m$
Total Conversion Error (typical)	
m = 0.2	
0.5 VDC < $E_1 \leq$ 10 VDC	±2 m VDC
0.1 VDC < $E_1 \leq$ 0.5 VDC	±25 m VDC
m = 5	
1.0 VDC < $E_1 \leq$ 10 VDC	±15 m VDC
Exponent Range (continuous)	$0.2 \leq m \leq 5$
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC



Exponentiator Transfer Characteristics

NOTES:
(1) Connect a 100 Ω potentiometer as shown in Figure 4 for either roots ($0.2 \leq m < 1$) or powers ($1 < m \leq 5$).
(2) Set R_1 so that with E_1 = +10.00 VDC, E_o = +10.00 VDC.
(3) Select a + DC voltage level (E_1) such that the output voltage (E_o), as acted upon by the desired exponent, will not exceed +10.00 VDC. A level which is mid-range for input values of interest is an appropriate one to use. Set R_2 so that the output voltage (E_o) is the value expected for the chosen values of input (E_1) and exponent (m).

FIGURE 4



(4) Repeat steps (2) through (4) as necessary.

* When taking roots of smaller input levels, a modified transfer equation [$E_o = (10E_1)^m$] will provide improved conversion accuracy. To achieve this transfer function: 1) apply a +1.5 VDC REF in place of the +15 VDC REF shown in Figure 4., 2) make R_3 a 1.40 MΩ resistor, and rearrange R_1 and R_3 as 1.5VDC REF and 3) follow all notes except in note (2) apply +0.10VDC to pin 7 to set R_1 to E_o = +1.00VDC.

4302

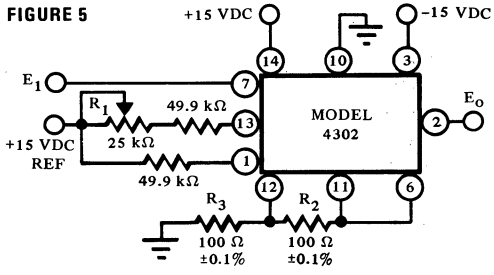
SQUARE ROOT

As a Square Rooter (m = 0.5), the 4302 provides a typical total conversion accuracy of ±0.07%. Refer to Figure 5 and notes for connections and adjustments respectively.

Transfer Function	$E_o = 10\sqrt{\frac{E_1}{10}}$
Total Conversion Error (Typical)	
0.5 VDC < E_1 ≤ 10 VDC	±7 mV
0.02 VDC < E_1 ≤ 0.5 VDC	±55 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Connect pins 12, 11, and 6 together. Set R_1 such that with E_1 = +10.00 VDC; E_o = +10.00 VDC.
(2) Connect 100 Ω resistors as shown in Figure 5.
(3) For greater conversion accuracy, R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 5



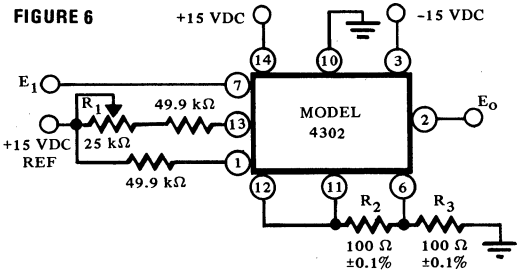
SQUARE

Configured as a Square Function Converter (m = 2), the 4302 produces high conversion accuracies of typically 0.03%. Please refer to Figure 6 and accompanying notes.

Transfer Function	$E_o = 10\left(\frac{E_1}{10}\right)^2$
Total Conversion Error (typical)	
0.1 VDC ≤ E_1 ≤ 10 VDC	±3 mV
Input Voltage Range	0 to +10 VDC
Output Voltage Range	0 to +10 VDC

NOTES:
(1) Set R_1 such that with E_1 = +10.00 VDC, E_o = +10.00 VDC.
(2) Connect 100 Ω resistors as shown in Figure 6.
(3) For greater conversion accuracy R_2 & R_3 may be replaced by a potentiometer as shown in Figure 4.

FIGURE 6



TRIGONOMETRIC FUNCTIONS

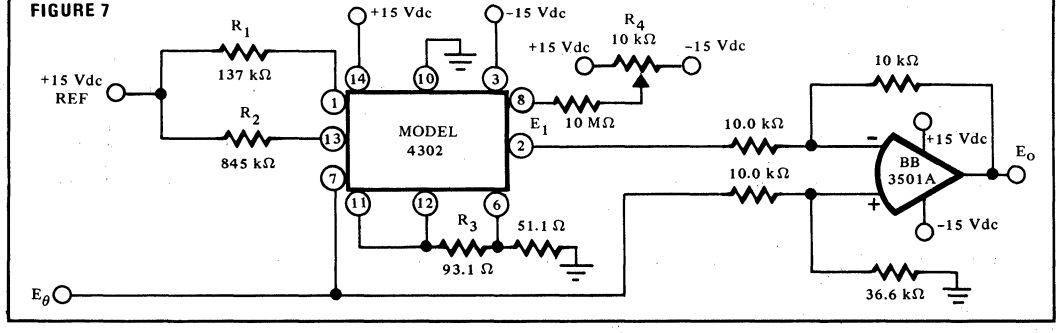
SINE

Sine functions can be accurately generated from input voltage levels representing angular displacement from 0 to 90°. Model 4302 configured as in Figure 7 will produce the sine power series approximations with modified coefficients to typically better than ±0.5% of full scale. In this circuit, the 4302 is scaled so that when $\theta = 0$, $E_O = 0$ VDC, and when $\theta = 90$, $E_O = 10$ VDC.

NOTES:
(1) Adjust R_4 if needed so that $E_1 < 1$ m VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_1 = +0.8045$ VDC when $E_\theta = +5.00$ VDC.
(3) Adjust R_3 so that $E_1 = +5.709$ VDC when $E_\theta = +10.00$ VDC.
(4) Repeat steps (2) and (3) as necessary.

Transfer Function	$E_O = 10 \text{ Sin } 9E_\theta$
Power Series Approximation: $E_O = 1.5708E_\theta - 1.5924\left(\frac{E_\theta}{6.366}\right)^{2.827}$	
Total Conversion Error (typical)	±50 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 to +10 VDC
Output Voltage Range ($0 \leq \sin\theta \leq 1$)	0 to +10 VDC

FIGURE 7



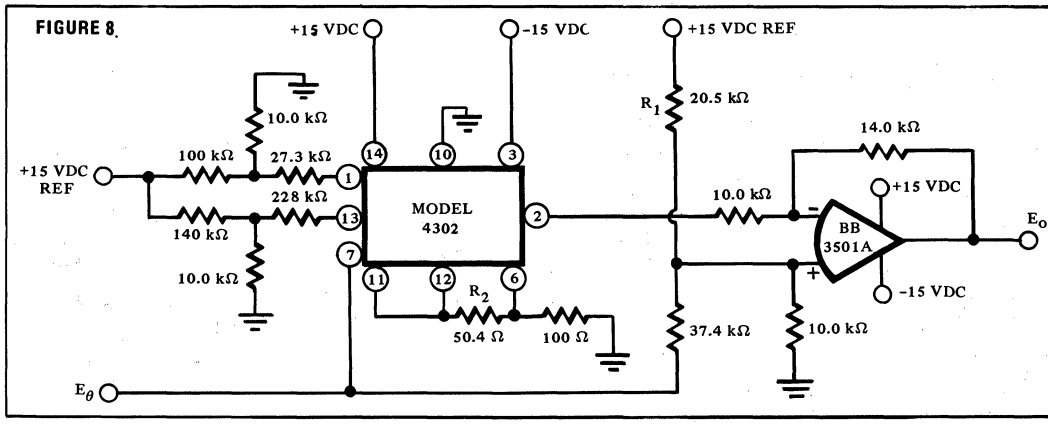
COSINE

Connected as in Figure 2, the Model 4302 will generate a cosine function of the input voltage. Typical accuracies of ±0.8% can be expected from this configuration.

NOTES:
(1) Adjust R_1 so that $E_O = +10.00$ VDC when $E_\theta = 0$.
(2) Adjust R_2 so that $E_O = 0$ when $E_\theta = +10.00$ VDC.

Transfer Function	$E_O = 10 \cos 9E_\theta$
Power Series Approximation: $E_O = 10 + 0.3652\,E_\theta - 0.4276E^{1.504}$	
Total Conversion Error (typical)	±80 mV
Input Voltage Range ($0 \leq \theta \leq 90^o$)	0 VDC to +10 VDC
Output Voltage Range ($1 \leq \cos\theta \leq 0$)	+10 VDC to 0 VDC

FIGURE 8



ARCTANGENT

Model 4302 and the associated circuitry shown below will produce the inverse tangent of a ratio. This application is particularly well suited to conversion from rectangular coordinates to polar coordinates where

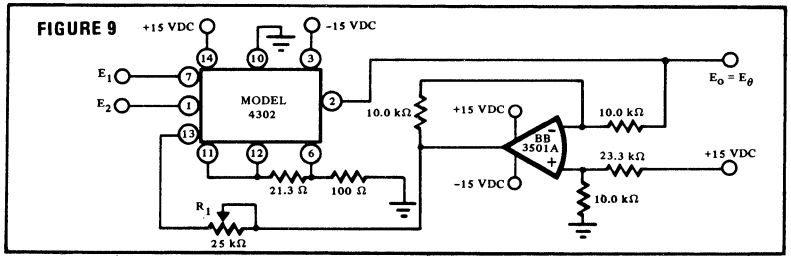
$$E_\theta = \tan^{-1}\frac{E_y}{E_x}$$

The accuracy of conversion depends upon the levels of the input signals. Please refer to table at right.

Transfer Function	$E_o = \tan^{-1}\left(\frac{\lvert E_1\rvert}{\lvert E_2\rvert}\right)$
Power Series Approximation	$E_o = \frac{\left(\frac{\lvert E_1\rvert}{\lvert E_2\rvert}\right)^{1.2125}}{1+\left(\frac{\lvert E_1\rvert}{\lvert E_2\rvert}\right)^{1.2125}}(90^o)$
Total Conversion Error $2 < E_1, E_2 \leq 10$ VDC $0.1 < E_1, E_2 \leq 2$ VDC $0.03 < E_1, E_2 \leq 0.1$ VDC Input Voltage Range (E_1, E_2) Output Voltage Range $0 \leq E_\theta \leq 90^o$	 ±55 m VDC ±65 m VDC ±340 m VDC +0.01 VDC to +10 VDC 0 VDC to +9 VDC

NOTE:
(1) Set R_1 so that with $E_1 = E_2 = +10.00$ VDC, $E_o = +4.500$ VDC ±1 mVDC.

FIGURE 9



VECTOR MAGNITUDE FUNCTION

The model 4302 will produce the square root of the sum of the squares of two inputs. This function is companion to the arctangent of a ratio for the conversion of rectangular to polar coordinates.

Transfer Function	$E_o = \sqrt{E_1^2 + E_2^2}$
Input Voltage Range E_1 E_2	0 to +10VDC -10VDC to +10VDC
(refer to notes 1 and 2)	
Output Voltage Range	0 to +10VDC
Conversion Error	±7m VDC

NOTES:

1. Figure 10 shows one practical way to implement the transfer function $E_o = \sqrt{E_1^2 + E_2^2}$ using 4302. It shows use of model 3501A op amp. Model 3501's rated output is ±10V. This limits the range of E_1 and E_2, such that the conditions $E_1 \leq \sqrt{100 - E_2}$ and $|E_2| \leq (5 - E_1^2/20)$ and $\sqrt{E_1^2 + E_2^2} \leq 10$ are always satisfied.
   (a) The above conditions imply, $0V \leq E_1 \leq 10V$ and $-5V \leq E_2 \leq 5V$.
   (b) The above conditions also imply that for applications where $E_1 = |E_2|$ the range would be limited to 4.142V max.
2. Use of model 3627 as shown in Figure 11 would directly substitute the eight 10kΩ resistors and the two model 3501A op amps. This would reduce the number of components needed to implement vector magnitude function and reduce overall cost.

FIGURE 10

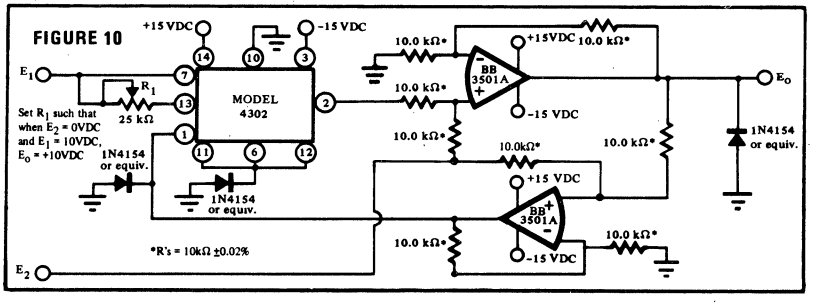
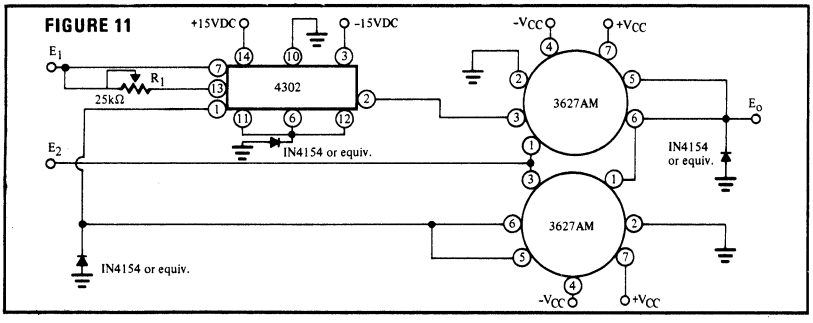
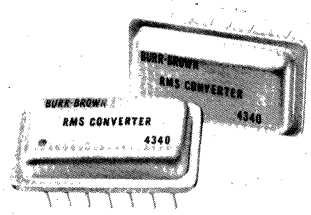


FIGURE 11



BURR-BROWN®

4340



TRUE RMS-TO-DC CONVERTER

FEATURES

- LOW COST
- HIGH ACCURACY
  ±0.3mV ±0.1% Rdg.
- HIGH INPUT IMPEDANCE - 5kΩ
- HERMETIC METAL PACKAGE

DESCRIPTION

The Burr-Brown Model 4340 is a True RMS-to-DC Converter featuring high performance, low cost, and a small hermetic package. The 4340 will compute the True RMS value of a variety of signals applied to the input. The input signal may consist of complex AC waveforms as well as a DC voltage level. The output of the 4340 is a DC voltage, the amplitude of which is equal to the RMS value of the input voltage.

The 4340 will accept input voltages from 0 to ±10V over a wide input frequency range. The conversion accuracy of the 4340 is specified in terms of error in millivolts (mV) plus a percent of reading, as a function of input signal level over an input frequency range.

The 4340 has an input impedance of 5kΩ and an output impedance of 1Ω. This product will supply up to 5mA of output current at a voltage of +10VDC. The input is fully protected for conditions of overvoltage up to the supply voltage. The output will withstand short-circuit to power supply common for an indefinte period of time.

The specified unadjusted performance characteristics of the 4340 are shown in the ELECTRICAL SPECIFICATIONS. Provision for the external adjustment of: gain, voltage offset, DC reversal error, and frequency response performance allow the user to improve upon the specified conversion accuracies to the degree required by the user's application.

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SPECIFICATIONS

ELECTRICAL

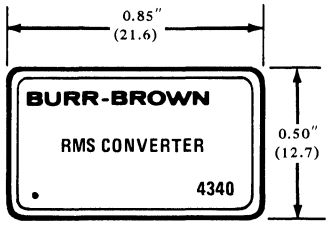
(Typical at 25°C with rated power supplies unless otherwise noted).

MODEL	4340
TRANSFER FUNCTION	E_O (d.c.) = $\sqrt{\overline{E_{IN}^2}}$
INPUT	
Peak Voltage	±10 Vdc
Absolute Maximum Voltage	± Supply
Impedance	5 kΩ
OUTPUT	
Voltage	0 to +10 Vdc
Current (min)	+5 mA
Impedance	1 Ω
CONVERSION ACCURACY	
Total Unadjusted Error (max)	
Input: 10 mV rms to 7.0 rms, 100 Hz to 10 kHz sine wave*	±2 mV ±0.2% Reading
Total Adjusted Error**	
Input: 10 mV rms to 7 V rms, 50 Hz to 20 kHz*	±0.3 mV ±0.1% Reading
STABILITY	
Accuracy vs Temperature	±0.001% of FS plus ±0.01% of reading per °C
Accuracy vs Supply	±0.001% of FS plus ±0.01% of reading per %ΔV
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +125°C
POWER REQUIREMENTS	
Rated Voltage	±15 Vdc
Voltage Range	±14 Vdc to ±16 Vdc
Quiescent Current	±12 mA

* Model 4340 will convert d.c. inputs. Lower frequency a.c. input signals will require the addition of external capacitors to preserve the accuracy.

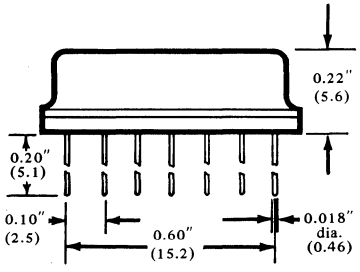
** Performance with external trims and $C_L \geq 3\ \mu F$ and $20\ pF \leq C_H \leq 100\ pF$.

MECHANICAL



(TOP VIEW)

Dimensions in millimeters are shown in parentheses.

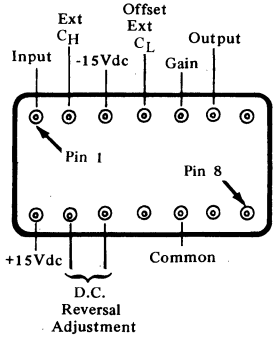


(SIDE VIEW)

Row Spacing: 0.30" (7.6)

Pin material and plating composition meet Method 2003 (solderability) of Mil-Std-883 [except for paragraph 3.2.]

PIN CONNECTIONS



(BOTTOM VIEW)

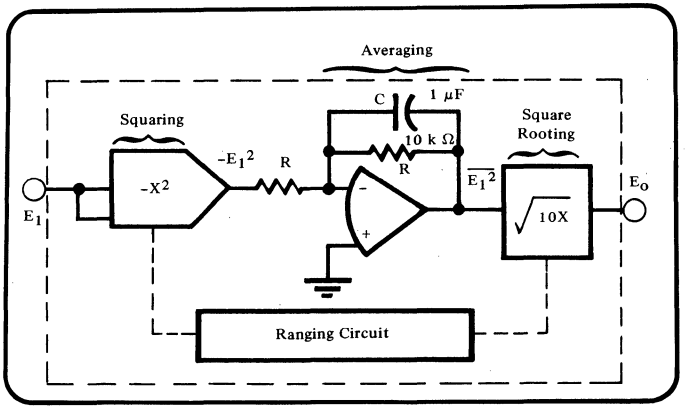


FIGURE 1. Functional Block Diagram of Model 4340.

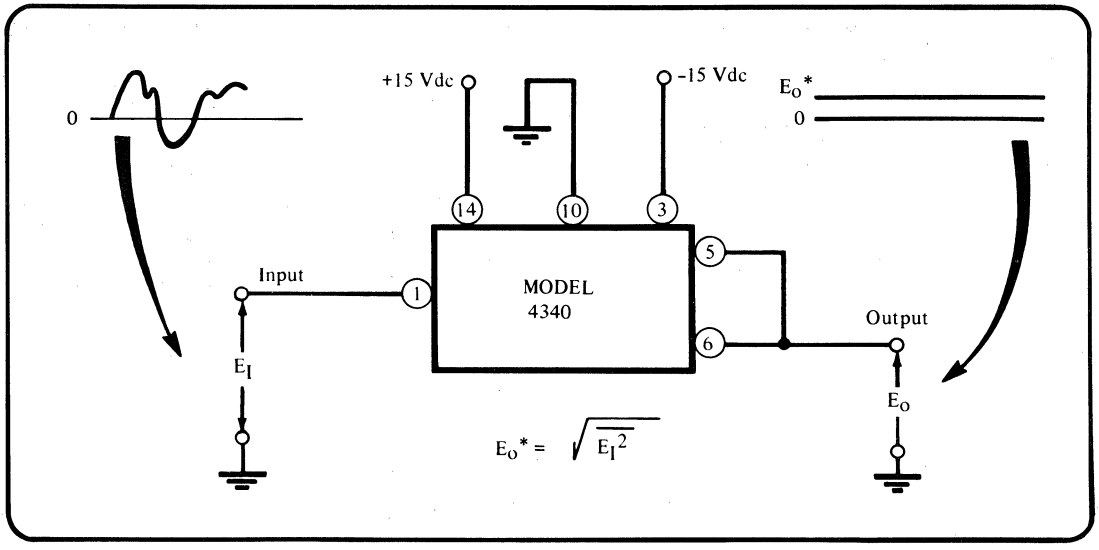


FIGURE 2. Model 4340 RMS Converter – Connected to produce specified unadjusted accuracy.

OPTIONAL EXTERNAL ADJUSTMENTS

Although the unadjusted performance of the 4340 is quite high for most applications, optimized performance can be achieved with external adjustments. The following paragraphs and figures will demonstrate the techniques for external adjustments of gain, voltage offset, d.c. reversal error, and frequency response. The unity gain adjustment should be made first, then the offset voltage adjustment. The unity gain adjustment should then be repeated for best results.

UNITY GAIN

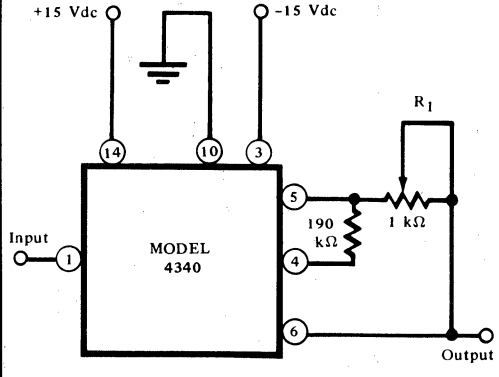


FIGURE 3. Unity Gain Adjustment – Apply +5 V rms Sine Wave to Input. Adjust R_1 for +5 Vdc at Output.

OFFSET VOLTAGE

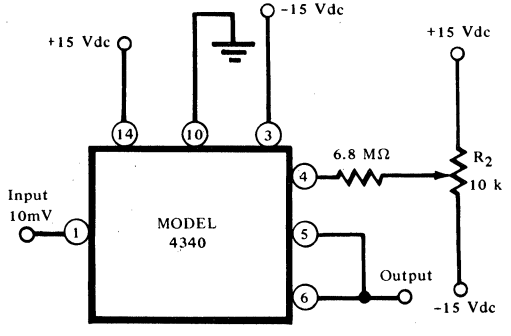


FIGURE 4. Offset Voltage Adjustment – Adjust R_2 for 10mVdc at Output.

FREQUENCY RESPONSE

The conversion accuracy of the 4340 over a broad range of input frequencies can be enhanced by the addition of one or more externally connected capacitors. Refering to Figure 5, C_H will improve the high frequency performance and C_L will extend the low frequency response.

HIGH FREQUENCY RESPONSE COMPENSATION

The upper limit of frequency response of the 4340 may be extended to meet the adjusted conversion accuracy specification by the proper selection of C_H.

Sweep a 1.0 V rms signal from 10 kHz to 20 kHz, measure the output voltage change from 1.0 Vdc. Select a value for C_H that minimizes the change in output voltage over 10 kHz to 20 kHz frequency range.

* C_H may be selected from 22 pF, 33 pF, 47 pF, or 100 pF.

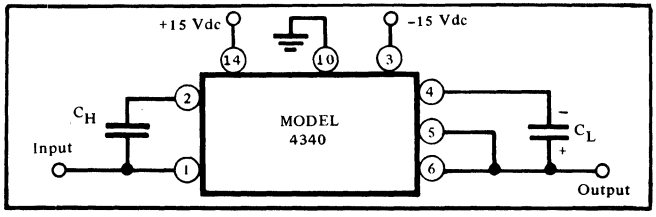


FIGURE 5. Frequency Response Adjustments – C_H* = 22 pF to 100 pF and $C_L \geq 3.0\ \mu F$ for "adjusted" frequency response range.

LOW FREQUENCY RESPONSE EXTENSION

In the 4340, a single-pole, low pass filter provides the averaging function. The time constant of this filter (To) is selected to be 0.005 seconds. Larger time constants should be selected in order to achieve the Conversion Accuracy at frequencies lower than 100 Hz.

The external capacitor can be 100's of microfarads, but the shunt resistance of the capacitor must be very large in order to maintain gain accuracy. The best value of C_L is inherently a compromise – the larger the capacitor the lower the ripple, but the response time is increased. Calculating the proper C_L for a given waveform can be done, but is tedious. The fastest method of choosing C_L is to apply a representative input signal, and observe the ripple at the output. Select various values of C_L until the ripple is attenuated sufficiently. The amount of allowable output ripple depends upon the application. For example, if the output is being read by an integrating DVM, then output ripple won't be critical.

ADDITIONAL ADJUSTMENTS

NON-UNITY GAIN

The 4340 may be adjusted to achieve a non-unity gain transfer function: $E_O = A\sqrt{E_{IN}^2}$ for $1 < A \leq 10$. Figure 6 illustrates the technique to achieve this gain change.

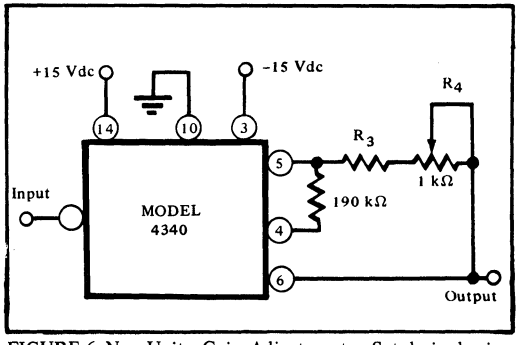


FIGURE 6. Non-Unity Gain Adjustment – Set desired gain by selecting R_3 such that $R_3 = (A^2 - 1) \times 10k\Omega$. Apply appropriate mid-scale d.c. level to Input and adjust R_4 for output equal to $A \times V_{Input}$ (Vdc).

D.C. REVERSAL ERROR

When the 4340 is utilized with D.C. inputs and a high degree of conversion accuracy is required, a correction for d.c. reversal error may be required. Figure 7 illustrates the method to accomplish this adjustment.

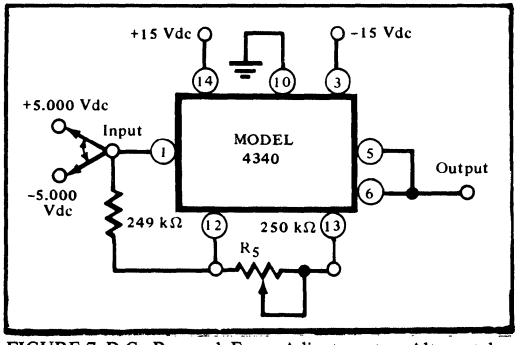
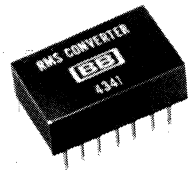


FIGURE 7. D.C. Reversal Error Adjustment – Alternately switch the input between +5.000 Vdc and -5.000 Vdc, adjust R_5 so that the output error voltage from +5.000 Vdc is the same for both input polarities.

NOTE: Some minor interaction may be experienced between the various adjustments requiring repeating of these adjustments for lowest total error.

BURR-BROWN®

4341



Low Cost
TRUE RMS-TO-DC CONVERTER

FEATURES

- **LOW COST**
- **HIGH ACCURACY**
  ±0.2% ±2mV
- **HIGH RELIABILITY**
  Hybrid construction

DESCRIPTION

The Burr-Brown Model 4341 RMS-to-DC Converter features low cost without sacrificing performance. The 4341 computes a DC voltage proportional to the true rms value of signals which may be complex waveforms, DC levels, or a combination of both.

The input and output are fully protected against overvoltages and short circuits. Provisions for the external adjustment of gain, offset voltage, DC-reversal error, and frequency response make the 4341 versatile enough to fill the majority of your applications.

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PDS-323A

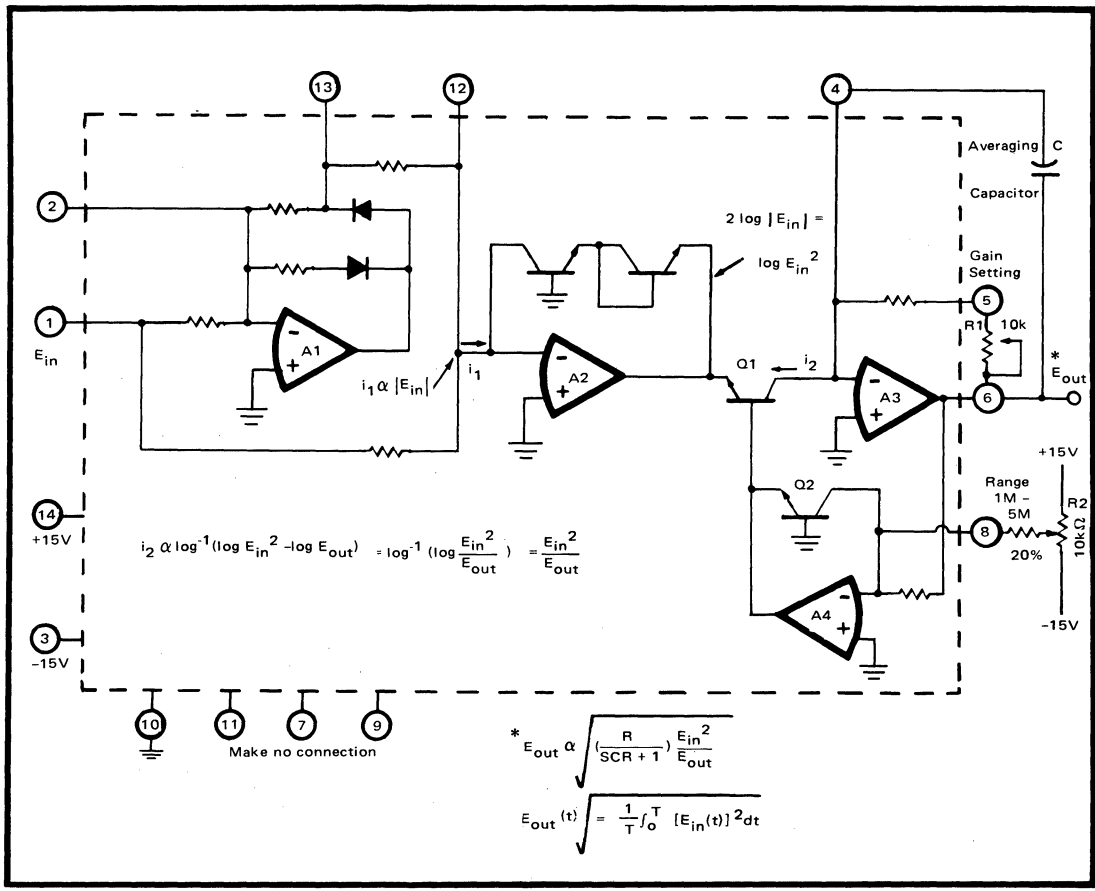


FIGURE 1. Simplified Schematic.

THEORY OF OPERATION

The true RMS value of a time-varying signal E (t) over a time period T is

$$E_{RMS} = \sqrt{\frac{1}{T} \int_0^T [E(t)]^2 \, dt}$$

The required operations are squaring, averaging and square rooting. A simplified schematic diagram of the 4341 is shown in Figure 1. The A1 circuit produces a current i_1 which is proportional to the rectified input voltage. The A2 circuit is a logarithmic amplifier which produces a voltage proportional to 2 log E_{in} or log E_{in}^2. The logarithmic gain of the A2 circuit is derived from the inherent exponential characteristics of transistor junctions. By using proprietary monolithic components, the circuit provides an accurate log function over many decades which is relatively insensitive to temperature variations. Amplifier A4 uses the same techniques as A2 to generate log E_{out}.

Transistor Q1 produces a collector current i_2 proportional to the antilog of its base-emitter voltage, such that

$$i_2 \alpha \log^{-1}(\log E_{in}^2 - \log E_{out}) = \log^{-1}\left(\log \frac{E_{in}^2}{E_{out}}\right) = \frac{E_{in}^2}{E_{out}}$$

The A3 circuit which contains the external capacitor takes the time average of the i_2 signal and produces E_{out} which is directly proportional to the RMS value of E_{in}.

Figures 2 and 3 show the effects of the external filter capacitor on ripple magnitude and response time. As the frequency of the input approaches DC, the 4341 begins to act like a full wave rectifier such that the output is the absolute value of the input. While the 4341 will accurately convert dc input voltages, the averaging capacitor must be made very large to minimize ripple at low frequencies.

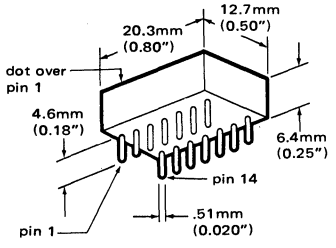
SPECIFICATIONS

(Typical at 25°C with rated supply voltages, unless otherwise noted.)

ELECTRICAL

MODEL	4341
TRANSFER FUNCTION	$E_{out}(DC) = \sqrt{\frac{1}{T}\int_0^T E_{in}^2(t)\,dt}$
INPUT	
Peak Operating Voltage	±10V
Absolute Maximum Voltage	±Supply
Impedance	5 kΩ
OUTPUT	
Voltage	0 to +10V
Current	+5mA, min
Resistance	1 Ω, max
BANDWIDTH	
±1% of Theoretical Output	80 kHz
-3 dB	450 kHz
CONVERSION ACCURACY(2)	
Input: 500 mV RMS to 5.0 V RMS DC to 10 kHz Sine Wave	±0.5% of Reading, max(1)
Input: 10 mV RMS to 7 V RMS DC to 20 kHz	±2 mV ±0.2% Reading
STABILITY	
Accuracy vs. Temperature	±0.1 mV ±0.01% of Reading/°C
Accuracy vs. Supply Voltage	±0.1 mV ±0.01% of Reading/% of Supply Voltage Change
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +125°C
POWER REQUIREMENTS	
Rated Voltage	±15 VDC
Voltage Range	±14 VDC to ±16 VDC
Quiescent Current	±12 mA, typ./±24 mA, max

MECHANICAL



Row Spacing: 7.6mm (0.300")
Weight: 3.4 grams (0.12 oz.)
Connector: 14-Pin DIP
0145MC

Pin material and plating composition conform to Method 208 (solderability) of Mil-Std-202.

(1) After standard trim procedure (see below).
(2) Model 4341 will convert DC inputs. Lower frequency AC inputs require a large value of averaging capacitor to minimize ripple at output. (See Figure 2)

STANDARD TRIM PROCEDURE

If the 4341 is used to measure sine waves or distorted sine waves, only two trims are needed to achieve an accuracy of ±0.5% of reading from 500 mV RMS to 5 V RMS up to 10 kHz. Refer to Figure 1.

1. Set E_{in} = 5.000 V RMS ±0.02% and adjust R1 such that E_o = 5.000 VDC ±2 mV.
2. Set E_{in} = 500 mV RMS ±0.02% and adjust R2 such that E_o = 500 mVDC ±0.2 mV.
3. Repeat Step 1.

CHOOSING THE AVERAGING CAPACITOR

A single-pole low-pass RC filter provides the averaging function. The time constant is 1/2 RC where R is 10kΩ when the 4341 is adjusted for unity gain. To select the best value of C, make a tradeoff between output ripple and response time. Figure 2 shows the ripple magnitude vs. frequency for several typical values of capacitor. Response time vs. capacitor value is shown in Figure 3. (Note that rise times and fall times are different for the same value of capacitor).

While the ripple magnitude for signals other than sine waves can be analytically determined, it is tedious. The fastest method of choosing C is to apply a representative input signal and observe the output for various value of C. C can be 100's of microfarads, but should have a leakage current less than 0.1μA to minimize gain errors. With very large values of C, the input signals with frequencies approaching DC level could be averaged. Since the output is always a positive voltage, C can be polar capacitor.

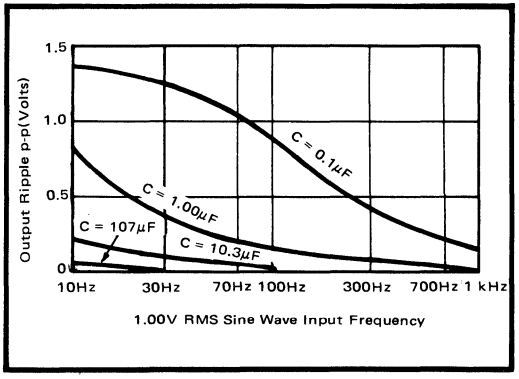


FIGURE 2. Output Ripple Magnitude vs. Input Signal Frequency.

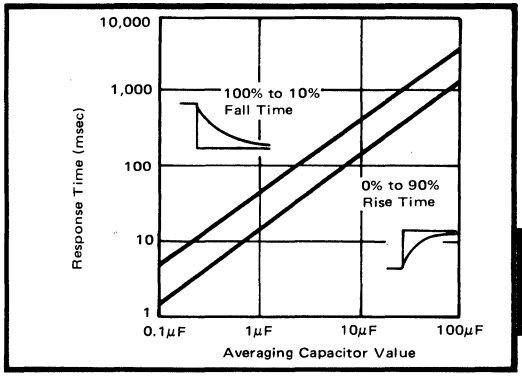


FIGURE 3. Response Time vs. Value of Averaging Capacitor.

EXPANDED TRIM PROCEDURE FOR GREATER ACCURACY

If the 4341 is used in applications to measure complex waveforms, the following expanded trim procedure is recommended. (Refer to Figure 4).

First set all potentiometers at mid turn position.

1. DC Reversal Error - Apply +10.000V ±1mV and -10.000V ±1mV to E_{in} alternatively, adjust R5 such that E_o readings are the same ±2mV.
2. Gain Adjustment - Apply E_{in} = +10.000VDC ±1mV, adjust R1 such that E_o = +10.000VDC ±1mV.
3. Input Offset - Apply +10.0mV ±0.1mV and -10.0mV ±0.1mV to E_{in}, adjust R4 such that E_o readings are the same ±0.1mV.
4. Offset - Ground E_{in}, adjust R3 such that E_o = 0 ±0.1mV. Repeat Step (3).
5. Low Level Accuracy - Apply E_{in} = +10.0mV ±0.1mV, adjust R2 such that E_o = +10.0mV ±0.1mV.

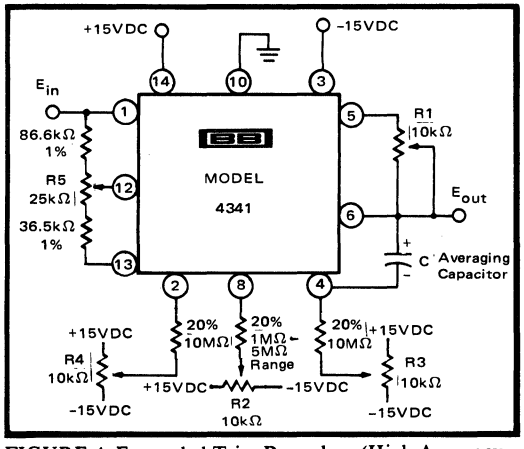


FIGURE 4. Expanded Trim Procedure (High Accuracy Applications).

NONUNITY GAINS

Gain values greater than unity can be achieved by inserting resistor R_x between pin 5 and pin 6. $R_x \simeq (A^2 - 1) \times 10k + 2k$ where A is the desired value of gain ($1 < A \leq 10$). (R_x is in ohms).

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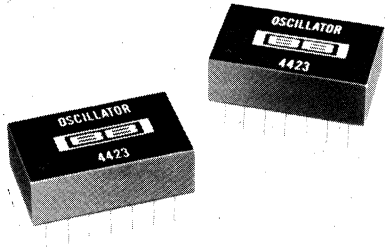

4423

PRECISION QUADRATURE OSCILLATOR

FEATURES

- SINE AND COSINE OUTPUTS
- RESISTOR PROGRAMMABLE FREQUENCY
- WIDE FREQUENCY RANGE
  0.002Hz to 20kHz
- LOW DISTORTION
  0.2% max up to 5kHz
- EASY ADJUSTMENTS
- SMALL SIZE
- LOW COST

DESCRIPTION

The Model 4423 is a precision quadrature oscillator. It has two outputs 90 degrees out of phase with each other, thus providing sine and cosine wave outputs available at the same time. The 4423 is resistor programmable and is easy to use. It has low distortion (0.2% max up to 5 kHz) and excellent frequency and amplitude stability.

The Model 4423 also includes an uncommitted operational amplifier which may be used as a buffer, a level shifter or as an independent operational amplifier. The 4423 is packaged in a versatile, small, low cost DIP package.

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PDS-365A

SPECIFICATIONS

Specifications typical at 25°C and ±15VDC
Power Supply Unless Otherwise Noted.

ELECTRICAL

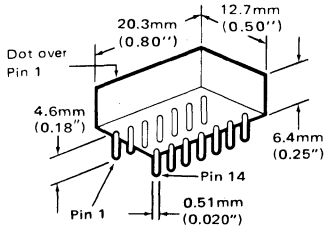
	MIN	TYP	MAX	UNITS
FREQUENCY				
Initial Frequency (no adjustments)	20.0k	21.0k	22.0k	Hz
Frequency Range (using 2 R's only)	2k		20k	Hz
Frequency Range (using 2 R's and 2 C's)	0.002		20k	Hz
Accuracy of Frequency Equation*		±1	±5	%
Stability vs Temperature		±50	±100	ppm/°C
Quadrature Phase Error		±0.1		degree
DISTORTION				
Sine Output (pin 1)				
0.002Hz to 5kHz			0.2	%
5kHz to 20kHz			0.5	%
Cosine Output (pin 7)				
0.002Hz to 5kHz		0.2		%
5kHz to 20kHz		0.8		%
Distortion vs Temperature		0.015		%/°C
OUTPUT				
Amplitude (Sine)				
At 20 kHz	6.5	7	7.5	V rms
vs Temperature		0.05		%/°C
vs Supply		0.4		V/V
Output Current	1.5	5		mA
Output impedance			1	Ω
UNCOMMITTED OP AMP				
Input Offset Voltage		1.5		mV
Input Bias Current		275		nA
Input Impedance		1		MΩ
Open Loop Gain		90		dB
Output Current	5			mA
POWER SUPPLY				
Rated Supply Voltage		±15		VDC
Supply Voltage Range	±12		±18	VDC
Quiescent Current		±9	±18	mA
TEMPERATURE RANGE				
Specifications	0		+70	°C
Operation	-25		+85	°C
Storage	-55		+125	°C

* May be trimmed for better accuracy.

PIN CONNECTIONS

1. E_1, Sine Output
2. Frequency Adjustment
3. Frequency Adjustment
4. +In, Uncommitted Op Amp
5. -In, Uncommitted Op Amp
6. Output, Uncommitted Op Amp
7. E_2, Cosine Output
8. Frequency Adjustment
9. $-V_{CC}$, -15VDC
10. $+V_{CC}$, +15VDC
11. Common
12. Frequency Adjustment
13. Frequency Adjustment
14. Frequency Adjustment

MECHANICAL



ROW SPACING - 7.6 (0.300")
WEIGHT - 3.4 gms (0.12 oz)
CONNECTOR - 14 pin DIP connector
(145 MC)

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

4423

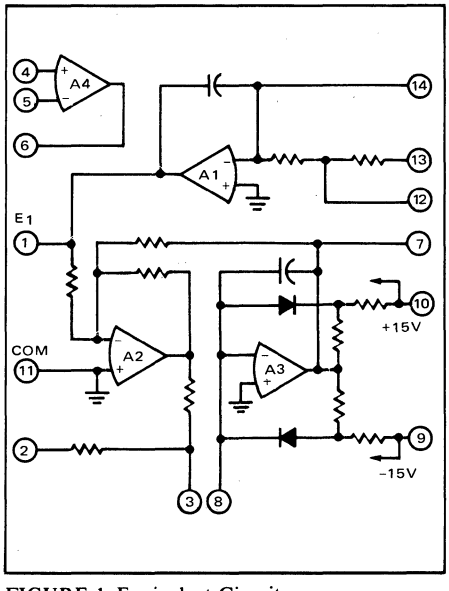


FIGURE 1. Equivalent Circuit.

TYPICAL PERFORMANCE CURVES

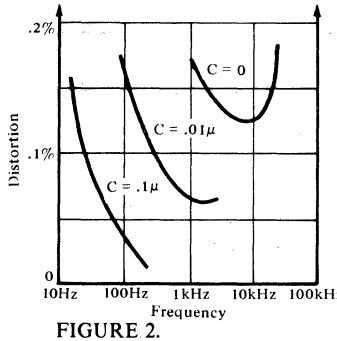


FIGURE 2.

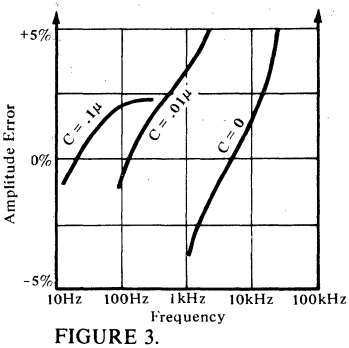


FIGURE 3.

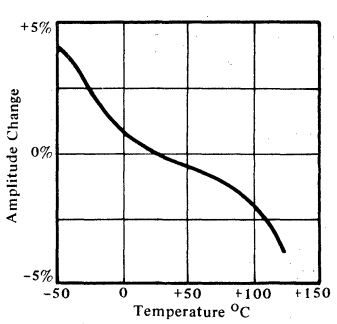


FIGURE 4.

EXTERNAL CONNECTIONS

1. 20 kHz Quadrature Oscillator

The 4423 does not require any external component to obtain a 20 kHz quadrature oscillator. The connection diagram is as shown in Figure 5.

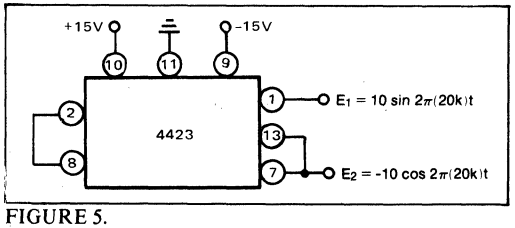


FIGURE 5.

2. Resistor Programmable Quadrature Oscillator

For resistor programmable frequencies in the 2 kHz to 20 kHz frequency range, the connection diagram is shown in Figure 6. Note that only two resistors of equal value are required. The resistor R can be expressed by,

$$R = \frac{3.785f}{42.05 - 2f}$$, R in kΩ, f in kHz

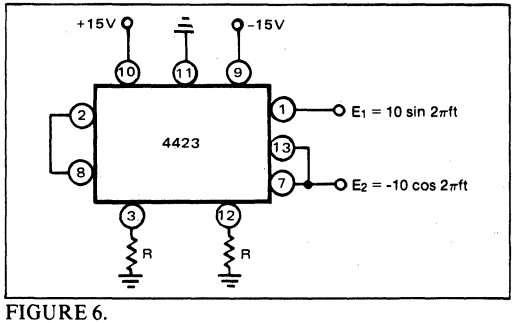


FIGURE 6.

3. Quadrature Oscillator Programmable to 0.002 Hz

For oscillator frequencies below 2000 Hz, use of two capacitors of equal value and two resistors of equal value as shown in Figure 7 is recommended. Connections shown in Figure 7 can be used to get oscillator frequency in the 0.002 Hz to 20 kHz range.

The frequency f can be expressed by:

$$f = \frac{42.05\ R}{(C + 0.001)\ (3.785 + 2R)}$$

where, f is in Hz
C is in μF
and R is in kΩ

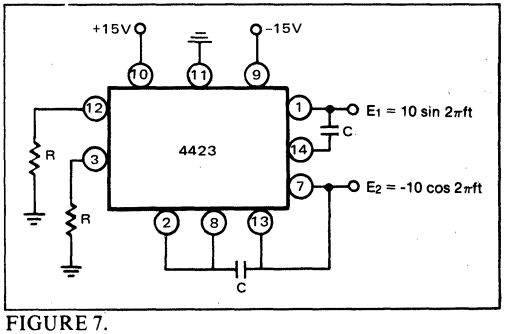


FIGURE 7.

For best results, the capacitor values shown in Table I should be selected with respect to their frequency ranges.

	f	20 kHz to 2 kHz	2 kHz to 200 Hz	200 Hz to 20 Hz
	C	0	0.01μF	0.1μF
f	20 Hz to 2 Hz	2 Hz to 0.2 Hz	0.2 Hz to 0.02 Hz	0.02 Hz to 0.002 Hz
C	1μF	10μF	100μF	1000μF

TABLE I.

After selecting the capacitor for a particular frequency the value of the required resistor can be obtained by using the resistor selection curve shown in Figure 8 or by the expression:

$$R = \frac{3.785f\ (C + 0.001)}{42.05 - 2f\ (C + 0.001)}$$

where,
R is in kΩ
f is in Hz
and C is in μF

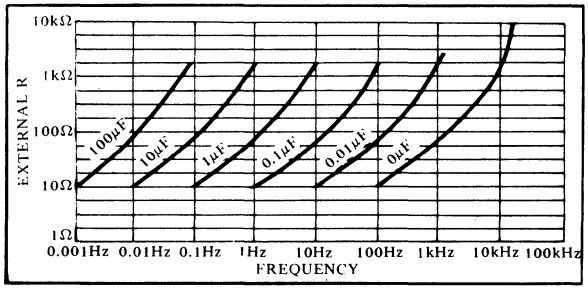


FIGURE 8.

The curves shown in Figure 8 are provided only as a nomographic design aid. The selection of capacitor values is not limited to the values shown in Figure 8. Any suitable combination of R and C values which satisfies the expression relating R, F and C as shown above, would work satisfactorily with the 4423.

NOTES ON TYPES OF CAPACITORS TO USE:

There are various kinds of capacitors available for use. There are polarized, also known as DC capacitors and non-polarized, also known as AC capacitors available. Of these two types, the polarized capacitors cannot be used with 4423 to set the frequencies.

Commonly available non-polarized capacitors include NPO ceramic, silver mica, teflon, polystyrene, polycarbonate, mylar, ceramic disc etc. A comparison is shown in Table II.

	Capacitance Range (μF)	Temperature Coefficients ppm/°C	Dissipation Factor (%)
NPO Ceramic	5pF - 0.1 μF	30	0.05
Silver Mica	5pF - 0.047 μF	60	0.05
Teflon	0.001 - 100 μF	200	0.01
Polystyrene	0.001 - 500 μF	100	0.03
Polycarbonate	0.001 - 1000 μF	90	0.08
Metalized Teflon	0.001 - 100 μF	60	0.1
Metalized Polycarbonate	0.001 - 1000 μF	10	0.4
Mylar	0.001 - 1000 μF	700	0.7
Metalized Mylar	0.001 - 2000 μF	700	1
Ceramic Disc	5pF - 0.5 μF	10,000	3

TABLE II.

For use with the 4423 oscillator, the choice of capacitors depends mainly on the user's application, error budget and cost budget. Note that the specifications of 4423 do not include the error contribution of the external components. The errors sourced by external components normally have to be added to the 4423 specifications.

As a general selection criteria we recommend the use of the above table. Start from the top of the list in the above table. If the capacitor is found unsuitable due to it being too large in size, too expensive, or is not easily available, then move down in the list for the next best selection. In any case do not choose or use any capacitors with dissipation factors greater than 1%. Such a capacitor would stop 4423 oscillation.

DISSIPATION FACTOR (DF)

A capacitor can be modeled by an ideal capacitor in parallel with an internal resistor whose value depends on its dissipation factor (DF). Mathematically, the internal resistor R is given by,

$$R = \frac{1}{2\pi f\, C(DF)}$$

where R is in Ω, f is the Hz, and C is in farads.

For example, the DF of ceramic disc capacitors is of the order of 3%, which for a 0.01 μF capacitor would look like having an internal resistor of 530kΩ at 1 kHz. The 530 kΩ value resistor is small enough to stop the 4423 oscillator from oscillating.

Some capacitor manufacturers use the terms "Power Factor" (PF) or "Q Factor" (Q) instead of the term "Dissipation Factor". These terms are similar in meaning and are mathematically related by,

$$(PF) = \frac{(DF)}{\sqrt{1 + (DF)^2}} \quad ; \quad Q = \frac{1}{(DF)}$$

OSCILLATION AMPLITUDE

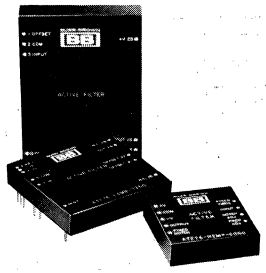
It takes a finite time to build up the amplitude of the oscillation to its final full scale value. There is a relationship between the amplitude build-up time and the frequency. The lower the frequency, the longer the amplitude build-up time. For example, typically it takes 250 seconds at 1 Hz, 30 seconds at 10 Hz, 4 seconds at 100 Hz, 400 milliseconds at 1 kHz, and 40 milliseconds at 10 kHz oscillator frequencies.

There are two methods available to shorten this normal amplitude build-up time. But there is also a relationship between the amplitude build-up time and distortion at final amplitude value. When the amplitude build-up time is shortened, the distortion can get worse.

One method to shorten the amplitude build-up time is to connect a resistor between pin 3 and pin 14. The lower this resistor is the shorter will be the time to build up amplitude of the oscillation, and worse will be the distortion of the output waveform. For example, a 100kΩ resistor would shorten the amplitude build up time from 15 seconds to 1 second at 20 Hz frequency, but the distortion could be degraded from tpically 0.05% to 0.5%.

The other method is to momentarily insert a 1kΩ resistor via a reset switch betwen pin 3 and pin 14. The amplitude of oscillation is built up instantaneously when the reset switch is pushed. There will be no degradation of distortion with this method since the 1kΩ resistor does not remain in the circuit continuously.

BURR-BROWN®



ATF76

ACTIVE FILTERS

FEATURES

- LOW PROFILE PACKAGE
- FACTORY TUNED
- NO EXTERNAL COMPONENTS REQUIRED
- WIDE TEMPERATURE RANGE

DESCRIPTION

Burr-Brown's standard series of fixed-frequency active filters is available with a wide range of transfer characteristics and resonant frequencies. These modular units are pre-tuned at Burr-Brown to the response you specify and they require no external components or adjustments. The ATF76 series includes Bessel, Butterworth, Chebyschev, band pass and band reject filters with up to eight poles. You can save hours of design and analysis, especially when your application requires a complex transfer function.

These units have applications in communications equipment, servo systems, and process controllers as well as test equipment. All filters are completely tested at the factory, and all give you the reliability you expect from Burr-Brown.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

FIXED FREQUENCY ACTIVE FILTERS

Burr-Brown's standard catalog active filters, the ATF76 series, are available with low pass, band pass, and band reject characteristics. The filters in this series are packaged in space-saving 0.4" high modules ranging in size from 1.5" x 1.5" for 2 pole low pass and notch models to only 2.1" x 3.0" for 8 pole low pass models. All filters are complete units that are factory tuned with no external components required. All standard active filters operate from ±15 VDC power over a -25°C to +85°C temperature range.

Specifications typical at 25°C and rated supply voltage unless otherwise noted.

MODEL(1)	BAND PASS SINGLE TUNED				
	ATF76-B1*M	ATF76-B1*N	ATF76-B1*P	ATF76-B1*Q	ATF76-B1*R
FILTER ORDER No. of Poles	2				
INPUT					
Voltage Range	±10 V, min				
Impedance	100 kΩ, min				
FREQUENCY (f_c)					
Range	1 to 20kHz				
Accuracy	±1%				
Temp. Coeff.	±0.03%/°C				
Adj. Range	±3%				
GAIN	(inverting)				
Pass Band	0 ±0.5 dB				
SELECTIVITY (Q)					
Value	2	5	10	20	50
Tolerance	±10%				
OUTPUT					
Noise(2)	100 μV				
Impedance	10 Ω				
Current	±5 mA				
POWER SUPPLY CURRENT					
±15 VDC @ Quiescent(6)	±10 mA				
PACKAGE DWG.(See page 5-92)	#23	2" x 2" x 0.4"			

ATF76

Specifications typical at 25°C and rated supply voltage unless otherwise noted.

MODEL(1)	LOW PASS BUTTERWORTH				LOW PASS BESSEL (Linear Phase)			
	ATF76-L2*B	ATF76-L4*B	ATF76-L6*B	ATF76-L8*B	ATF76-L2*L	ATF76-L4*L	ATF76-L6*L	ATF76-L8*L
FILTER ORDER No. of Poles	2	4	6	8	2	4	6	8
INPUT								
Voltage Range	±10 V min				±10 V min			
Impedance(5)	30 kΩ, min				30 kΩ, min			
FREQUENCY								
Range	1 to 20kHz				1 to 20kHz			
Accuracy	±2%				±2%			
Temp. Coeff.	±0.05%/°C				±0.05%/°C			
GAIN(9)	(non-inverting)				(non-inverting)			
Pass Band	0 dB, nom				0 dB, nom			
DC Accuracy	±0.05 dB, max				±0.05 dB, max			
Q-FACTOR	N/A				N/A			
OUTPUT								
Noise(2)	50 μV, RMS				50 μV, RMS			
Output Impedance	1Ω				1Ω			
Rated Current	±5 mA				±5 mA			
Offset at 25°C(8)	±2 mV				±2 mV			
Offset Drift -25°C to +85°C	±25 μV/°C		±50 μV/°C		±25 μV/°C		±50 μV/°C	
POWER SUPPLY CURRENT ±15 VDC @ Quiescent (7)	±6 mA	±10 mA	±14 mA	±18 mA	±6 mA	±10 mA	±14 mA	±18 mA
PACKAGE DWG.(See page 5-92)	#14 1.5" x 1.5" x 0.4"	#23 2" x 2" x 0.4"	#33 3" x 2.1" x 0.4"		#14 1.5" x 1.5" x 0.4"	#23 2" x 2" x 0.4"	#33 3" x 2.1" x 0.4"	

*Insert L or M, depending on frequency required.
(1) See below for ordering information.
(2) 10 Hz to 50 kHz with input grounded.
(3) -40 dB notch attenuation, minimum.
(4) ±3% f_c adjustment and notch depth adjustment.

ORDERING INFORMATION

ATF76 - B 2 M

- ATF76 — (Designates Series)
- DEFINES FILTER TYPE — L = Low Pass; B = Band Pass; N = Notch
- DESIGNATES NO. OF POLES OR POLE PAIRS OR ZERO PAIRS — Low Pass: 2 = 2 poles, 4 = 4 poles, 6 = 6 poles, 8 = 8 poles; Band Pass: 1 = 1 pole pair, 2 = 2 pole pairs; Notch: 1 = zero pair
- GROSS FREQUENCY RANGE — L < 10 Hz; M ⩾ 10 Hz

BAND PASS STAGGER TUNED				
ATF76-B2 *K	ATF76-B2 *M	ATF76-B2 *N	ATF76-B2 *P	ATF76-B2 *Q
4				
±10 V, min 100 kΩ, min				
1 to 20kHz ±1% ±0.03%/°C				
— (non-inverting) 0 ±0.5 dB				
1	2	5 ±10%	10	20
100 μV 10 Ω ±5 mA				
±20 mA				
#33	3" x 2.1" x 0.4"			

Prices and specifications are subject to change without notice.

LOW PASS CHEBYSCHEV (±0.4 dB Ripple)				LOW PASS CHEBYSCHEV (±1.6 dB Ripple)				BAND-REJECT (NOTCH)		
ATF76-L2 *C	ATF76-L4 *C	ATF76-L6 *C	ATF76-L8 *C	ATF76-L2 *D	ATF76-L4 *D	ATF76-L6 *D	ATF76-L8 *D	ATF76-N1 *M	ATF76-N1 *N	ATF76-N1 *P
2	4	6	8	2	4	6	8	2	2	2
±10V 30 kΩ, min				±10V 30 kΩ, min				±10V 30 kΩ, min		
1 to 20kHz ±2% ±0.05%/°C				1 to 20kHz ±2% ±0.05%/°C				1 to 20kHz ±2%(4) ±0.03%/°C		
(non-inverting) 0 dB, nom -0.4 dB, max				(non-inverting) 0 dB, nom -1.6 dB, max				(inverting) 0 dB, nom(3) ±0.05 dB, max		
N/A				N/A				2 ± 10%	5 ± 10%	10 ± 10%
50 μV, RMS 1 Ω ±5 mA ±2 mV				50 μV, RMS 1 Ω ±5 mA ±2 mV				200 μV, RMS 1 Ω ±5 mA ±2 mV		
±25 μV/°C		±50 μV/°C		±25 μV/°C		±50 μV/°C		±25 μV/°C		
±6 mA	±10 mA	±14 mA	±18 mA	±6 mA	±10 mA	±14 mA	±18 mA	±10 mA		
#14 1.5" x 1.5" x 0.4"	#23 2" x 2" x 0.4"	#33 3" x 2.1" x 0.4"		#14 1.5" x 1.5" x 0.4"	#23 2" x 2" x 0.4"	#33 3" x 2.1" x 0.4"		#14 1.5" x 1.5" x 0.4"		

(5) For models with higher input impedance contact Burr-Brown or your local representative.
(6) ±9 to ±18 VDC power may be used.
(7) ±12 to ±18 VDC power may be used.
(8) The offset may be trimmed to zero.
(9) All filters have noninverting outputs except the single tuned band pass and band reject filter which have inverting outputs.

M – 58RO

TYPE OF FILTER RESPONSE

Low Pass	Band Pass	S - Special Order	Notch
B = Butterworth	K for Q = 1(2 pole pairs only)	indicate Q on order for	M for Q = 2
C = Chebyschev	M for Q = 2	2 pole pairs 1 ⩽ Q ⩽ 20	N for Q = 5
0.4 dB nom ripple	N for Q = 5	1 pole pair 2 ⩽ Q ⩽ 50	P for Q = 10
D = Chebyschev -	P for Q = 10		S for Q = Special
1.6 dB nom ripple	Q for Q = 20		(indicate Q on order,
L = Bessel	R for Q = 50 (1 pole pair only)		2 ⩽ Q ⩽ 10)

CUTOFF OR CENTER FREQUENCY

For frequencies less than 100 Hz, use "R" to indicate decimal point. For frequencies greater than 100 Hz, the last digit indicates number of zeros following first 3 digits of frequency. For example: 58 Hz = 58RO, 580 Hz = 5800, 5800 Hz = 5801

Definition of Filter Responses

LOW PASS FILTERS

BUTTERWORTH

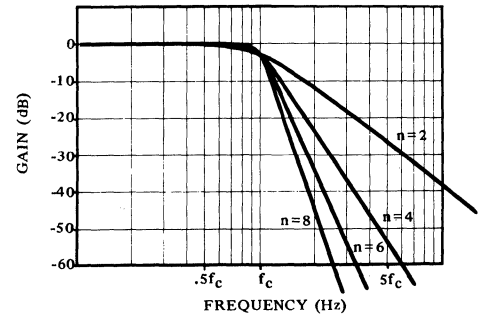
The Butterworth is a "maximally flat" amplitude response filter. Butterworth filters are used for filtering signals in data acquisition systems to prevent aliasing errors in sampled-data applications and for general purpose low-pass filtering.

The cutoff frequency, f_c, is the frequency at which the amplitude response is down 3 dB. The attenuation rate beyond the cutoff frequency is -n6 dB per octave of frequency where n is the order (number of poles) of the filter.

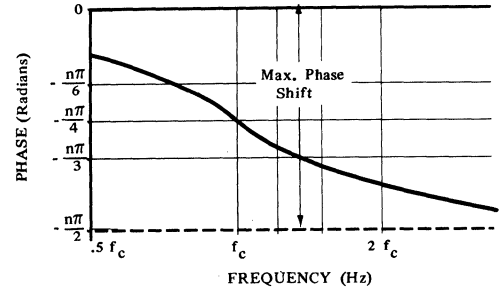
Other characteristics:

- Flattest possible amplitude response
- Excellent gain accuracy at low frequency end of passband.

AMPLITUDE RESPONSE



PHASE RESPONSE



ATF76

BESSEL

The Bessel is a type of "linear phase" filter. Because of their linear phase characteristics, these filters approximate a constant time delay over a limited frequency range. Bessel filters pass transient waveforms with a minimum of distortion. They are also used to provide time delays for low pass filtering of modulated waveforms and as a "running average" type filter.

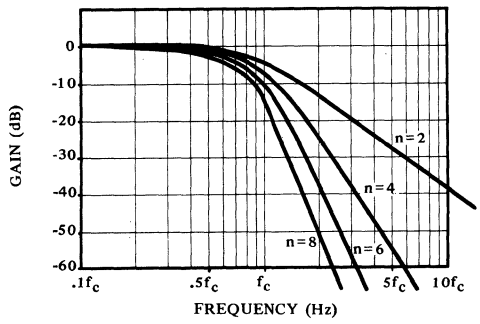
The maximum phase shift is $\frac{-n\pi}{2}$ radians where n is the order (number of poles) of the filter. The cutoff frequency, f_c, is defined as the frequency at which the phase shift is one half of this value. For accurate delay, the cutoff frequency should be twice the maximum signal frequency. The following table can be used to obtain the -3 dB frequency of the filter.

	2 pole	4 pole	6 pole	8 pole
3 dB Frequency	.77 f_c	.67 f_c	.57 f_c	.50 f_c

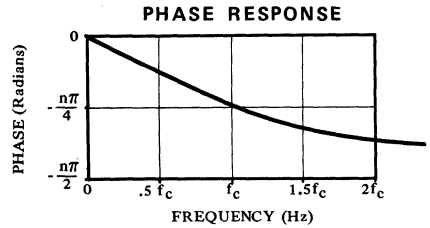
Other characteristics:

- Selectivity not as great as Chebyschev or Butterworth
- Very little overshoot response to step inputs
- Fast rise time

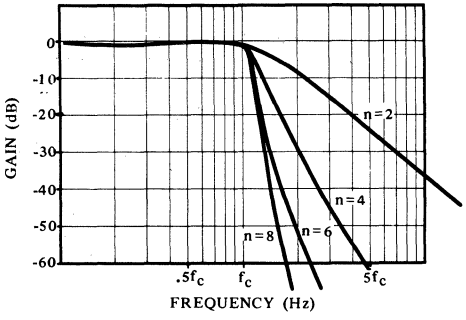
AMPLITUDE RESPONSE



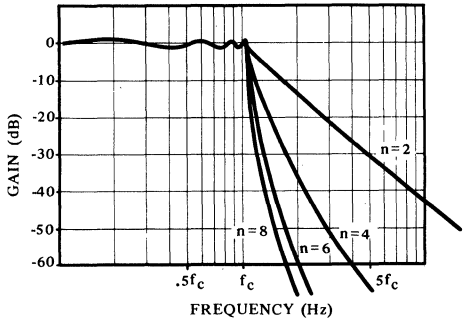
PHASE RESPONSE



C MODEL AMPLITUDE RESPONSE
(± 0.4 dB Ripple)



D MODEL AMPLITUDE RESPONSE
(± 1.6 dB Ripple)



CHEBYSCHEV

Chebyschev filters have greater selectivity than either the Bessel or Butterworth at the expense of ripple in the passband.

Burr-Brown offers Chebyschev filters with peak to peak ripple design values of ±0.25 dB and ±1.0 dB in the passband. Due to parameter tolerances the actual ripple is allowed to go to ±0.4 and ±1.6 dB; however the rolloff in the stopband will closely approximate the design response. Increased ripple in the passband allows increased attenuation past the cutoff frequency. The filter is designed so that the passband ripples equally about 0 dB.

The cutoff frequency is defined as the frequency at which the amplitude response passes through the specified maximum ripple band and enters the stop band.

Other characteristics:

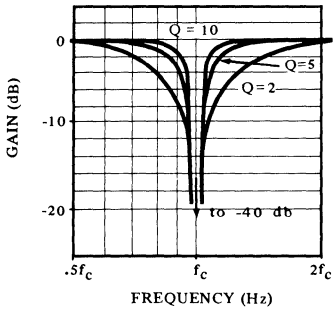
- Greatest selectivity
- Very nonlinear phase response
- High overshoot response to step inputs

The table below shows the typical overshoot and settling time response of the low pass filters to a step input.

	NUMBER OF POLES	PEAK OVERSHOOT	SETTLING TIME (% of final value)		
		% Overshoot	±1%	±0.1%	±0.01%
BUTTERWORTH	2	4	$1.1/f_c$ sec.	$1.7/f_c$ sec.	$1.9/f_c$ sec.
	4	11	$1.7/f_c$	$2.8/f_c$	$3.8/f_c$
	6	14	$2.4/f_c$	$3.9/f_c$	$5.0/f_c$
	8	16	$3.1/f_c$	$5.1/f_c$	$7.1/f_c$
BESSEL	2	0.4	$0.8/f_c$	$1.4/f_c$	$1.7/f_c$
	4	0.8	$1.0/f_c$	$1.8/f_c$	$2.4/f_c$
	6	0.6	$1.3/f_c$	$2.1/f_c$	$2.7/f_c$
	8	0.3	$1.6/f_c$	$2.3/f_c$	$3.2/f_c$
CHEBYSCHEV (C Model)	2	11	$1.1/f_c$	$1.6/f_c$	-
	4	18	$3.0/f_c$	$5.4/f_c$	-
	6	21	$5.9/f_c$	$10.4/f_c$	-
	8	23	$8.4/f_c$	$16.4/f_c$	-
CHEBYSCHEV (D Model)	2	21	$1.6/f_c$	$2.7/f_c$	-
	4	28	$4.8/f_c$	$8.4/f_c$	-
	6	32	$8.2/f_c$	$16.3/f_c$	-
	8	34	$11.6/f_c$	$24.8/f_c$	-

BAND REJECT FILTERS

AMPLITUDE RESPONSE



Burr-Brown's band reject filters have steep attenuation skirts and a minimum of 40 dB attenuation at f_c. Although f_c is factory adjusted to ±1%, an external trim potentiometer allows adjustment of f_c within a ±3% range allowing the user to obtain the exact frequency desired. A notch adjustment trimmer may also be used to provide a minimum of 40 dB attenuation at any point within the ±3% f_c adjustment range.

The frequencies below and above f_c where the amplitude response is down by 3 dB are referred to as f_1 and f_2 respectively. The selectivity of the filter is defined as: $Q = f_c / (f_2 - f_1)$.

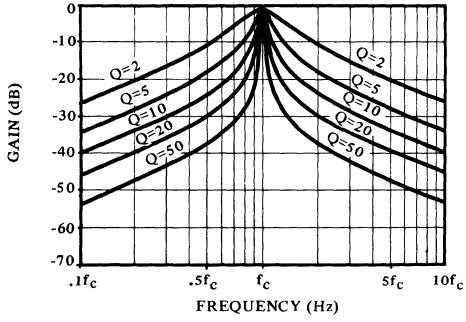
BAND PASS FILTERS

Burr-Brown makes both single-tuned (2 pole) and stagger-tuned (4 pole) bandpass filters. The center frequency, f_c, of single tuned filters can be user adjusted over a ±3% range. Stagger tuned filters are maximally flat in the passband and have steeper attenuation rolloffs than single tuned filters of comparable Q.

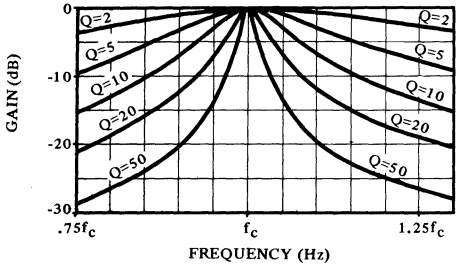
The 3 dB frequencies below and above f_c are f_1 and f_2. The selectivity, Q, is defined as: $Q = f_c / (f_2 - f_1)$. f_c itself is defined as: $f_c = \sqrt{f_1 f_2}$.

SINGLE-TUNED

AMPLITUDE RESPONSE

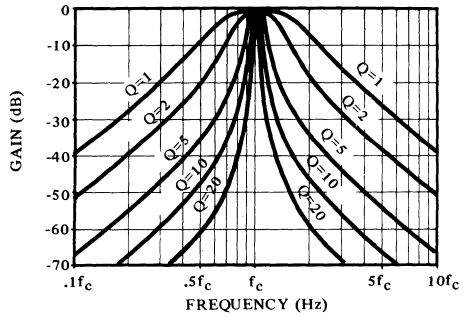


AMPLITUDE RESPONSE EXPANDED SCALE

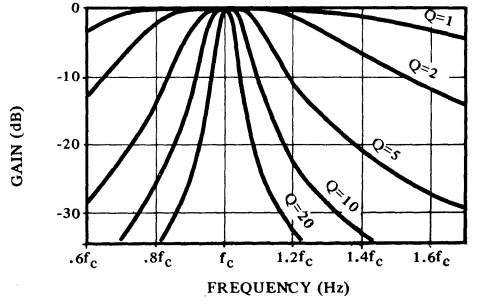


STAGGER-TUNED

AMPLITUDE RESPONSE

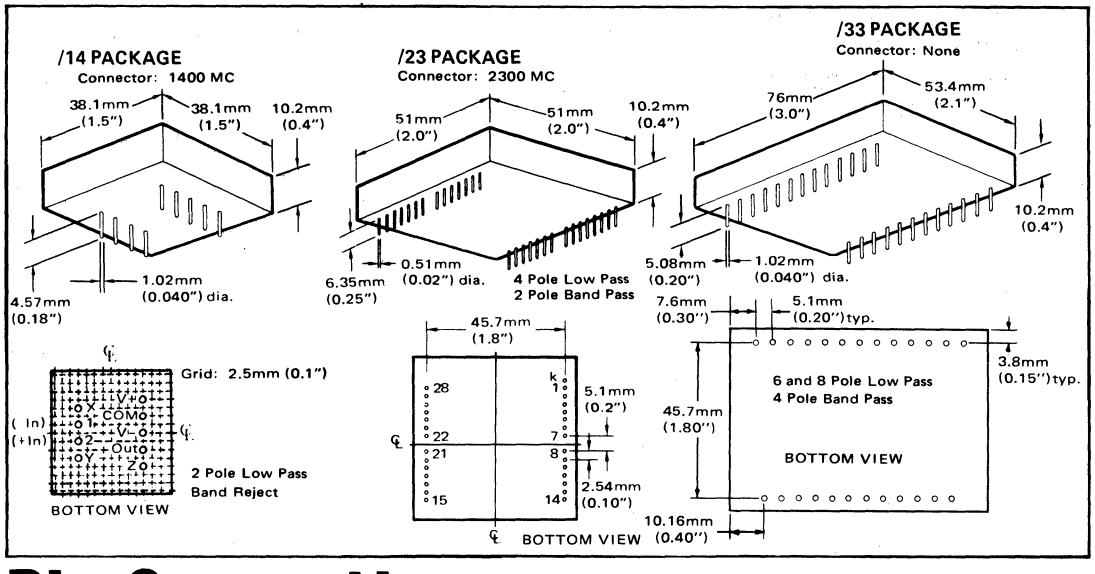


AMPLITUDE RESPONSE EXPANDED SCALE



Mechanical Specifications

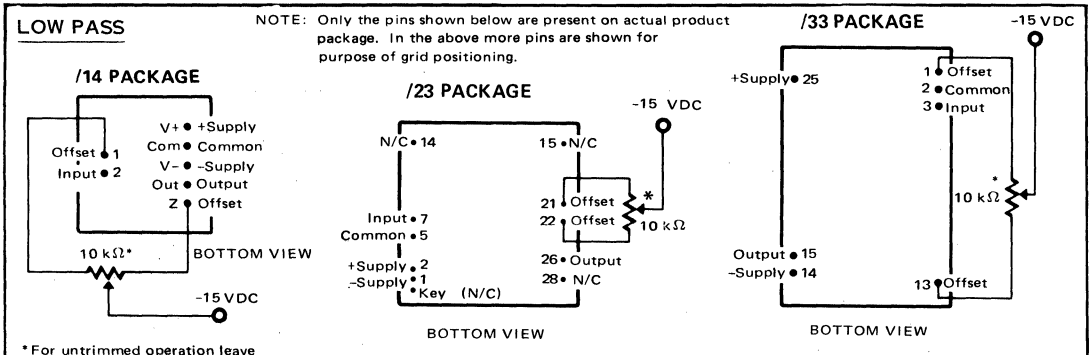
Dimensions in millimeters are shown in parentheses.



Pin Connections

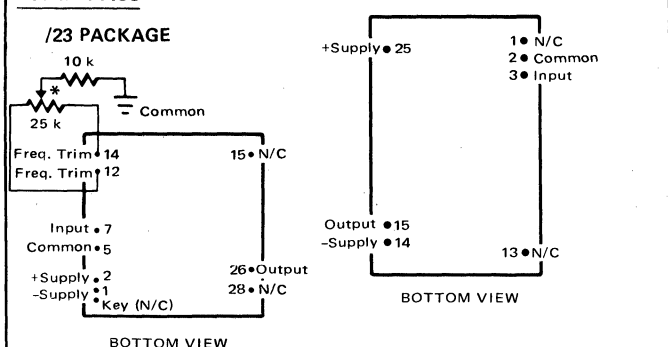
LOW PASS

NOTE: Only the pins shown below are present on actual product package. In the above more pins are shown for purpose of grid positioning.



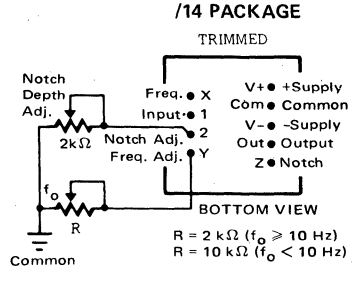
*For untrimmed operation leave adjustment pins open.

BAND PASS



*For untrimmed operation leave adjustment pins open.

BAND REJECT



For untrimmed operation, leave pin 2 and pin Y open while tying pin X and pin Z to ground. When using trimpots leave pins X and Z open.

BURR-BROWN®

UAF11
UAF21

UNIVERSAL ACTIVE FILTERS

FEATURES

- **SAVES DESIGN TIME**
  - User-tuneable frequency, Q-factor, gain
  - Calculate only three resistance values
  - Design directly from this data sheet
  - Completely characterized parameters
- **IMPROVED PERFORMANCE**
  - Wide frequency ranges
  - UAF11 - 0.001Hz to 20kHz
  - UAF21 - 0.001Hz to 200kHz
  - 1% frequency accuracy
  - -55° to +125°C temperature range
  - Q range of 0.5 to 500
  - Reliable hybrid construction
  - NPO capacitors and thin-film resistors

APPLICATIONS

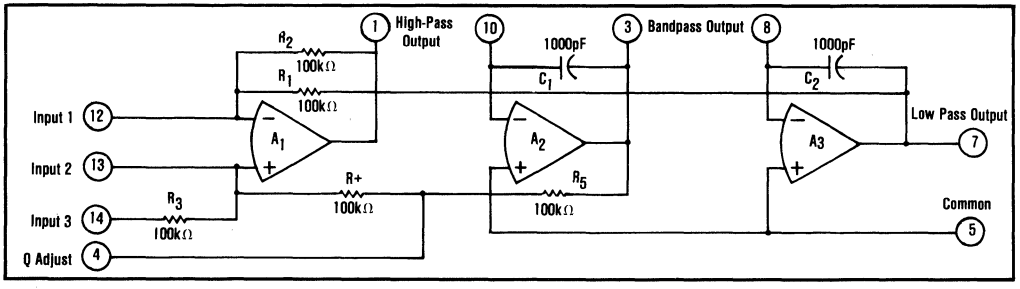
- **FILTER CONFIGURATIONS**
  - Butterworth
  - Bessel
  - Chebyschev
- **FILTER FUNCTIONS**
  - Low pass
  - High pass
  - Bandpass
  - Band reject

DESCRIPTION

The UAF11's and UAF21's are low cost universal active filters. These versatile units can easily be tailored to any active filter application using the extensive information provided in this data sheet. UAF's are excellent choices for use in communications equipment, test equipment (engine analyzers, aircraft and automotive test, medical test, etc.), servo systems, process control equipment, sonar and many others.

The UAF11's and UAF21's are complete two-pole active filters with the addition of four external resistors that provide the user easy control of the Q-factor, resonant frequency and gain. Any complex filter response can be obtained by cascading these units. Three separate outputs provide low-pass, high-pass, and bandpass transfer functions. A band-reject (notch) transfer function may be realized simply by summing the high-pass and low-pass outputs.

Since these UAF's are so versatile and flexible, they can be stocked by the user in quantity for use as building blocks whenever the requirement arises. This means instant availability and the UAF purchases may be made in volume to take advantage of quantity price discounts.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-295G

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and with rated supply unless otherwise noted.

MODEL	UAF11	UAF21(1)	UNITS
INPUT			
Input Bias Current	±100	±15	nA
Input Voltage Range	±10	±10	V
Input Resistance	100k	100k	Ω
TRANSFER CHARACTERISTICS			
Frequency Range (f_o)	0.001 to 20k	0.001 to 200k	Hz
f_o Accuracy(2)	±1/±5	±1/±5	%
f_o Stability(3) (over temp. range)	±0.005	±0.005	%/°C
Q Range(4)	0.5 to 500	0.5 to 500	--
Q Stability(5)			
at f_o Q ≤ 10^4	±0.025	±0.01	%/°C
at f_o Q ≤ 10^5	±0.1	±0.025	%/°C
Gain Range	0.1 to 50	0.1 to 50	--
OUTPUT			
Slew Rate	0.6	6.0	V/μsec
Peak-to-Peak Output Swing(6)			
f_o ≤ 10kHz	20	20	V
f_o ≤ 20kHz	10	20	V
f_o ≤ 100kHz	2	20	V
Output Offset			
(at low-pass output with unity gain)	±10	±10	mV
Output Impedance	2	10	Ω
Noise(7)	200	200	μV, rms
Output Current(8)	10	10	mA
POWER SUPPLIES			
Rated Power Supplies	±15	±15	V
Power Supply Range(9)	±5 to ±18	±5 to ±18	V
Supply Current at ±15V (Quiescent)	±12, max	±12, max	mA
TEMPERATURE RANGE			
Specification Temperature Range			
Epoxy	-25 to +85	-25 to +85	°C
Hermetic	-55 to +125	-55 to +125	°C
Storage Temperature Range	-55 to +125	-55 to +125	°C

NOTES

1. The UAF21 includes two internal 0.002μF power supply capacitors.
2. Repeatability of f_o using 0.1% frequency determining resistors.
3. T.C.R. of external frequency determining resistors must be added to this figure.
4. Derated 50% from maximum - see Typical Performance Curves.
5. Q stability varies with both the value of Q and the resonant frequency f_o.
6. Low-pass output - see Typical Performance Curves.
7. Measured at the bandpass output with Q = 50 over DC to 50kHz.
8. The current required to drive R_{F1} and R_{F2} (external) as well as C_1 and C_2 must come from this current.
9. For supplies below ±10V, Q max will decrease slightly; filters will operate below ±5V.

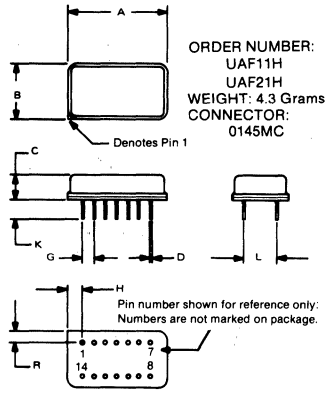
PIN CONNECTIONS

Pin 1. High-Pass Output	Pin 8. Frequency Adjust
Pin 2. Optional Pin	Pin 9. -Supply
Pin 3. Bandpass Output	Pin 10. Frequency Adjust
Pin 4. Q Adjust Point	Pin 11. Optional Pin
Pin 5. Common	Pin 12. Input 1
Pin 6. +Supply	Pin 13. Input 2
Pin 7. Low-Pass Output	Pin 14. Input 3

MECHANICAL

HERMETIC METAL PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMR at seating plane.



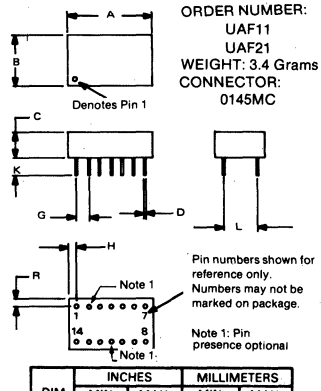
ORDER NUMBER:
UAF11H
UAF21H
WEIGHT: 4.3 Grams
CONNECTOR:
0145MC

Pin number shown for reference only. Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.860	.880	21.84	22.35
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

EPOXY PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.



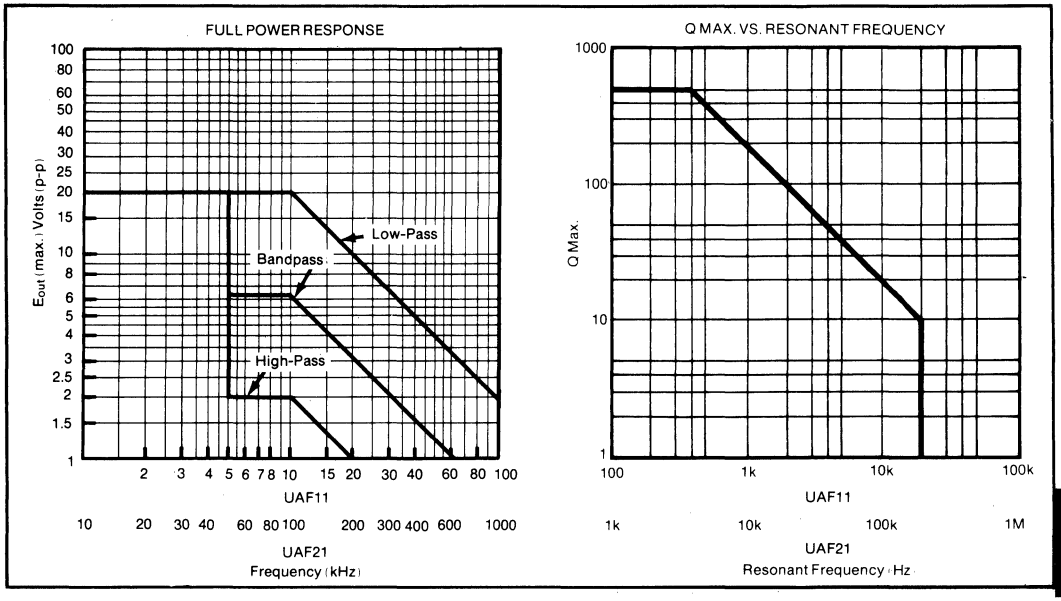
ORDER NUMBER:
UAF11
UAF21
WEIGHT: 3.4 Grams
CONNECTOR:
0145MC

Pin numbers shown for reference only. Numbers may not be marked on package.

Note 1: Pin presence optional

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.790	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

TYPICAL PERFORMANCE CURVES



APPLICATIONS INFORMATION

TRANSFER FUNCTION

The UAF21 uses the state variable technique to produce a basic second order transfer function. The equation describing the three outputs available are:

$$T(\text{Low-Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Bandpass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High-Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $\omega_o = 2\pi f_o$.

To obtain band reject characteristics the low-pass and high-pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band-Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

where $A_{LP} = A_{HP} = A$.

The state variable approach uses two op amp integrators and a summing amplifier to provide simultaneous low-pass, bandpass and high-pass responses. One UAF is required for each two poles of low-pass or high-pass filters and for each pole-pair of bandpass or band-reject filters.

DESIGN PROCEDURE SUMMARY

These procedures give the design steps for the proper application of a UAF and for the selection of the external components. More detailed information on filter theory pertinent to some of the steps can be found in the reference sources listed in Table I.

TABLE I. Useful References.

1. Tobey, Gene, et al, Operational Amplifiers: Design and Applications, Chapter 8, McGraw-Hill Book Company, 1971.
2. Wong, Yu Jen, and William Ott: Function Circuits: Design and Applications, Chapter 6, McGraw-Hill Book Company, 1976.
3. Daniels, Richard W.: Approximation Methods for Electronic Filter Design, McGraw-Hill Book Company, 1974.
4. Zyerev, Anatol I.: Handbook of Filter Synthesis, John Wiley and Sons, 1967.
5. Temes, Gabor C., and Sanjit K. Mitra: Modern Filter Theory and Design, John Wiley and Sons, 1973.

Burr-Brown also manufactures a line of completely self-contained active filters called the ATF76 series. These are available in most popular transfer functions with from 2- to 8-pole responses. They contain all necessary components and do not require any user design effort.

DESIGN STEPS

1. Choose the type of function (low-pass, bandpass, etc.), type of response (Butterworth, Bessel, etc.), number of poles, and cutoff frequency based on the particular application.

   If the transfer function is band-reject see Band-Reject Transfer Function before proceeding to step 2.
2. Determine the normalized low-pass filter parameters (f_n and Q) based on the type of response and number of poles selected in step 1. See Normalized Low-Pass Parameters.
3. If the actual response desired is low-pass go to step 4. For other responses a transformation of variables must be made (low-pass to bandpass or low-pass to high-pass). See Low-Pass Transformation.

4. Determine the actual (denormalized) cutoff frequency, f_o, by multiplying f_n by the actual desired cutoff frequency. See Denormalization of Parameters.
5. Pick the desired UAF configuration (noninverting, inverting or bi-quad). See Configuration Selection Guide and UAF Configurations and Design Equations.
6. Decide whether to use design equations "A" or "B". See Design Equations "A" and "B".
7. Calculate R_{F1} and R_{F2}. See Natural Frequency and UAF Configurations and Design Equations.
8. Determine Q_P. See Q_P Procedure.
9. Select the desired gain for each UAF and calculate the corresponding R_G and R_Q. See Gain (A) and UAF Configurations and Design Equations.

BAND-REJECT TRANSFER FUNCTION

The band-reject is achieved by summing the high-pass and low-pass UAF outputs. Either of the configurations in Figures 2 and 3 can be used to provide the band-reject function if they are used as shown in Figure 1.

The 15kΩ resistor is adjusted for maximum rejection. The circuit in Figure 3 is applicable when using design equations "A" ($A_{LP} = A_{HP}$). When design equations "B" are used ($A_{LP} = 10A_{HP}$), the resistor at pin 7 must be 10 times the resistor at pin 1 to obtain equal pass-band gains above and below f_n.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the band-reject filter desired and for A_{LP} to equal the desired pass-band gain. An input constraint is that the input voltage times A_{BP} must not exceed the rated peak-to-peak voltage of the bandpass output, or clipping will result.

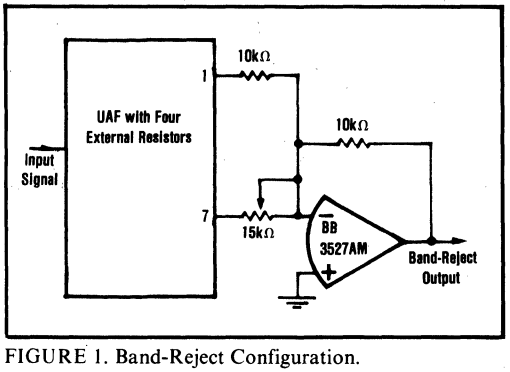


FIGURE 1. Band-Reject Configuration.

NORMALIZED LOW-PASS PARAMETERS

Usual active filter design procedure involves using normalized low-pass parameters. Table II is provided to assist in this step for the more common filter responses. Table III is a FORTRAN program which allows f_n and Q to be calculated for any desired ripple and number of poles for the Chebyschev response. Program inputs are the number of poles (N) and the peak-to-peak ripple (R). Program outputs are f_n and Q, which are used exactly as the values taken from Table II.

TABLE II. Low-Pass Filter Parameters.

Number	Butterworth		Bessel		Chebysev 0.5 dB Ripple		Chebysev 2 dB Ripple	
of Poles	f_n(1)	Q	f_n(1)	Q	f_n(2)	Q	f_n(2)	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	--	1.32475	--	0.626456	--	0.368911	--
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	--	1.50470	--	0.362320	--	0.218308	--
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	--	1.68713	--	0.256170	--	0.155410	--
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67658	0.237699	0.89236
	1.0	0.60134	1.85314	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5308	0.990142	18.6873

1. -3dB frequency.
2. Frequency at which amplitude response passes through the ripple band.

TABLE III. Low-Pass Chebyschev Program.

```
      PI=3.1415926536
      COMPLEX P(10)
      READ 5, N, R
    5 FORMAT (I2,F8.6)
      A=SQRT(EXP(R/4.3429448)-1.)
      B=1./A
      AN=ALOG(B+SQRT(B**2.1.))
      AN=AN/FLOAT(N)
      J=MOD(N, 2)+N/2
      DO 10K=1, J
      RP=SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT (2*N))
      XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
      WN=SQRT(RP**2+XIP**2)
      Q=-WN/(2*RP)
      P(K)=CMPLX(WN,Q)
      IF(MOD(N,2).NE.0.AND K.EQ.J)GO TO 15
      PRINT 20, P(K)
      GO TO 10
   15 F=REAL(P(K))
      PRINT 30, F
   10 CONTINUE
   20 FORMAT (2X"FN="E20.8"Q="E20.8)
   30 FORMAT (2X"FN = "E20.8)
      STOP
      END
```

NOTE: Language variations between computers may require modification of this program.

Note that for bandpass and high-pass filters complex conjugate pole pairs in the actual filter correspond to single poles in the normalized low-pass model. Thus four poles in Table II would correspond to four-pole pairs in a bandpass or high-pass filter.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents a simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. An external op amp and RC network can be used for this purpose.

The cutoff frequency determined by the Table II filter parameters is (1) the -3dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band (to enter the stop band).

LOW-PASS TRANSFORMATION

Low-Pass to High-Pass

The following simple transformation may be used for high-pass filters:

f_n (high-pass) = $\frac{1}{f_n \text{ (low-pass)}}$

Q (high-pass) = Q (low-pass)

Low-Pass to Bandpass

The low-pass to bandpass transformation to generate f_n (bandpass) and Q (bandpass) is much more complicated. It is tedious to do by hand but can be accomplished with the FORTRAN program given in Table IV. This program automates the tranformation

$s = p/2 \pm \sqrt{(p/2)^2 - 1.}$

TABLE IV. Low-Pass to Bandpass Transformation Program.

```
      COMPLEX P,S,U
      READ 5, FN, Q, QBP
    5 FORMAT (3F12.5)
      Y=FN*SQRT(1.-1(./(Q*2.))**2)
      X=-FN/Q*2.)
      P=CMPLX(X,Y)
      U=CONJG(P)
      DO 30 I=1,2
      S=P/(2*QBP)
      P=S**2-1.
      T=ATAN2(AIMAG(P),REAL(P))
      IF (T.GE.0.)GO TO 10
      T=2.*3.14159+T
   10 T=T/2.
      A=SQRT(CABS(P))*COS(T)
      B=SQRT(CABS(P))*SIN(T)
      S=S+CMPLX(A,B)
      FN=CABS(S)
      Q=-FN/(2.*REAL(S))
      PRINT 20,FN,Q
   20 FORMAT (2X"FN="F12.5"Q="F12.5)
      IF(AIMAG(U).EQ.0.)GO TO 40
   30 P=U
   40 STOP
      END
```

NOTE: Language variations between computers may require modification of this program.

Program Inputs

1. f_n - From Table II for the low-pass filter of interest
2. Q - From Table II
3. Q_{BP} - Desired Q of the bandpass filter

For filters with an odd number of poles a Q of 0.5 should be used where Q is not given in Table II. Enter 10^5 for Q when transforming zeros on the imaginary axis.

The program transforms each low-pass pole into a bandpass pole pair. Thus a three-pole low-pass input, would result in the pole positions for a three-pole pair bandpass filter requiring three UAF stages.

DENORMALIZATION OF PARAMETERS

Table II shows filter parameters for many 2- to 8-pole normalized low-pass filters. The Q and the normalized undamped natural frequency, f_n for each two-pole section are shown. The Q values do not have to be denormalized and may be used directly as described in the Design Procedure Summary. f_n must be denormalized by multiplying it by the desired cutoff frequency of the actual overall filter to obtain the required frequency, f_o for the design formulas. As an example, consider a 4-pole low-pass Bessel filter with a cutoff frequency of 1000Hz. The first stage would be designed to an $f_o$of 1432.41Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94Hz and Q of 0.80554. To combine the two stages into the composite filter the low-pass output of the first stage (pin 9) would be connected to the input resistors (R_G) of the second stage.

CONFIGURATION SELECTION GUIDE

It is possible to configure the UAF three different ways. Each configuration produces features that may or may not be desirable for a specific application. The selection guide in Table V is given to assist in determining the most advantageous configuration for a particular application.

UAF CONFIGURATIONS AND DESIGN EQUATIONS

Noninverting Configuration

For applications requiring a bandpass gain of 1V/V, the internal resistor R_F may be used (input at pin 14) as the gain resistor R_G; thus, only three external resistors are needed to configure the filter.

To use equations "B" connect an 11kΩ resistor between pins 12 and 1. Use equations "B" for frequencies above 8kHz or when R_Q from equations "A" becomes a negative value.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5$kHz (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $A_{BP} = QA_{LP} = QA_{HP}$
3. $R_Q = 10^5/(2Q_p - A_{BP} - 1)$
4. $R_G = (2Q_p - A_{BP} + 1)\ 10^5/A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5$kHz (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $A_{BP} = Q/3.16\ A_{LP} = 3.16Q\ A_{HP}$
3. $R_Q = 10^5/(3.48Q_p - A_{BP} - 1)$
4. $R_G = (3.48Q_p - A_{BP} + 1)\ 10^5/A_{BP}$

Inverting Configuration

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5$kHz (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $A_{BP} = Q\ A_{LP} = Q\ A_{HP}$
3. $R_G = 10^5\ Q_P/A_{BP}$
4. $R_Q = 2 \times 10^5/(2Q_P + A_{BP} - 1)$

	NONINVERTING INPUT	INVERTING INPUT	BI-QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Inverted Outputs	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant bandwidth
Other Advantages	May be used with only three external resistors (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2Q_P - A_{BP} > 1$ ($f_o < 8kHz$) $3.48Q_P - A_{BP} > 1$ ($f_o > 8kHz$)	$2Q_P + A_{BP} > 1$ ($f_o < 8kHz$) $3.48Q_P + A_{BP} > 1$ ($f_o > 8kHz$)	None

Summary: The Bi-Quad filter is particularly useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a bandpass or maintaining constant response of a low-pass or high-pass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than R_G and R_Q of the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 100k\Omega$; therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q).

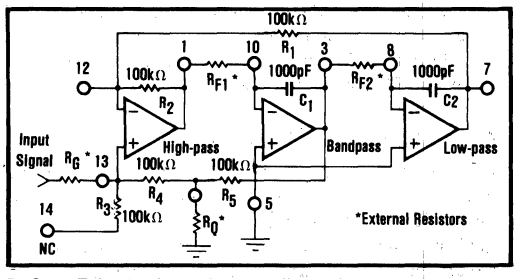


FIGURE 2. Noninverting Configuration.

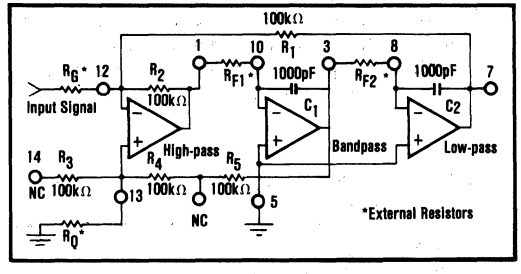


FIGURE 3. Inverting Configuration.

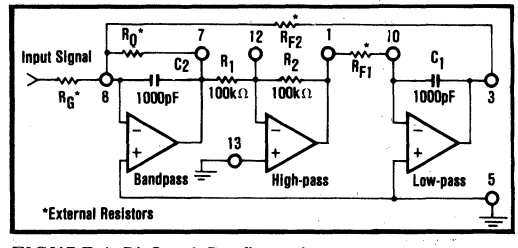


FIGURE 4. Bi-Quad Configuration.

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $A_{BP} = Q_P/3.16 = 3.16 Q_P A_{HP}$
3. $R_G = 3.16 \times 10^4 Q_P/A_{BP}$
4. $R_Q = 2 \times 10^5/(3.48Q_P + A_{BP} - 1)$

Bi-Quad Configuration

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 10^9/\omega_o = 1.59 \times 10^8/f_o$
2. $Q A_{LP} = A_{BP}$
3. $R_Q = Q_P R_{F1}$
4. $R_G = R_Q/A_{BP}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o > 5kHz$ (UAF11) or 50kHz (UAF21)

1. $R_{F1} = R_{F2} = 3.16 \times 10^8/\omega_o = 5.03 \times 10^7/f_o$
2. $Q A_{LP} = A_{BP}$
3. $R_Q = 3.16 Q_P R_{F1}$
4. $R_G = R_Q/A_{BP}$

Design Equations "A" and "B"

1. For f_o below 8kHz, either of equations "A" or "B" may be used.
2. For f_o above 8kHz, equations "B" must be used. If equations "A" were used above 8kHz, the filter could become unstable.
3. Equations "A" are for the UAF as it is supplied. When using equations "B", a 11kΩ resistor must be placed in parallel with R_2 (between pins 12 and 1).
4. The values of R_{F1} and R_{F2} calculated with equations "B" are approximately one-third of those calculated with equations "A". Thus there may be an advantage in using equations "B" at low frequencies. Using equations "B" would require use of one more resistor, but that would not alter or affect filter performance in any manner.
5. Using the negative gain values for A_{LP} or A_{HP} or A_{BP} could result in the negative values for resistors R_G and R_Q. So the absolute value of the gain should always be used in the equations.
6. Under some circumstances the value of R_Q using equations "A" will be negative. If this occurs, use design equations "B".

Natural Frequency (f_o)

1. f_o for each one pole-pair bandpass filter is the center frequency (f_C). f_C is defined as $f_C = \sqrt{f_1 f_2}$ where f_1 is the lower -3dB point and f_2 is the upper -3dB point of the pole-pair response.

2. To obtain f_o below 100Hz using practical resistor values, capacitors may be paralleled with C1 and C2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}\text{ (new)} = R_{F2}\text{ (new)} = R_{F1}\text{ (old)}\ \frac{1000pF}{C + 1000pF}$$

where R_F (new) is the new lower value frequency resistor, C is the value of the two external capacitors placed across C1 and C2 (between pins 10 and 3 and pins 8 and 7 and R_{F1} (old) is the value calculated in the simplified design equations.

Q-Factor

1. For bandpass filters $Q = \frac{f_o}{3dB\text{ bandwidth}}$
2. When designing low-pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.

Qp Procedure

1. If the "f_o times Q" product is greater than 10^4 (or 10^5 for the UAF21), it is possible for the measured filter Q to be different from the calculated value of Q. This effect is the result of nonideal characteristics of operational amplifiers. It can be compensated for by introducing the parameter Q_P into the design equations.
2. Calculate the f_o Q product for the filter. If the product is above 10^4Hz (or 10^5 for the UAF21), locate the corresponding f_oQ_P product on the curve in Figure 5. Divide f_oQ_P by f_o to obtain Q_P. Use Q_P as indicated in the design equations. For f_oQ products below 10^4Hz (or 10^5 for the UAF21), $Q_P = Q$.

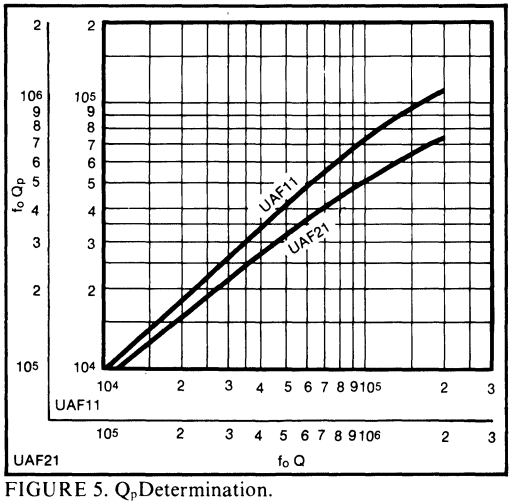


FIGURE 5. Q_PDetermination.

Gain (A)

1. The gain (V/V) of each filter section is:
   A_{LP} - for low-pass output - gain at DC
   A_{BP} - for bandpass output - gain at f_o
   A_{HP} - for high-pass output - gain at high frequencies.
2. Refer to the Typical Performance Curves for full power response. When selecting the gain, insure the limits of the curve are not exceeded for the desired voltage range.

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF filter components. They are not required for the regular design procedure but could be used if a detailed analysis is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = R_2 (R_1 R_{F1} C_1 R_{F2} C_2)$
2. $Q = 1 + \left(\frac{R_1}{R_{F1}}\right)\left(\frac{R_F}{R_1 + R_2}\right)(1 + 10^5 R_Q)\sqrt{\frac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2}}$
3. $R_F = 10^5 + 10^5 R_Q\ (10^5 + R_Q)$
4. $Q\ A_{LP} = Q\ A_{HP}\ R_1\ R_2 = A_{BP}\sqrt{R_1 R_{F1} C_1\ (R_2 R_{F2} C_2)}$
5. $A_{BP} = 10^5 (2 + 10^5 R_Q)\ R_G$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = R_2 (R_1 R_{F1} C_1 R_{F2} C_2)$
2. $Q = R_p (1 + 2 \times 10^5 R_Q)\sqrt{R_{F1} C_1\ (R_1 R_2 R_{F2} C_2)}$
3. $Q\ A_{LP} = Q\ R_1\ A_{HP}\ R_2 = A_{BP}\sqrt{R_1 R_{F1} C_1\ (R_2 R_{F2} C_2)}$
4. $A_{BP} = \sqrt{R_1 R_2 R_{F2} C_2\ (R_{F1} C_1)}\ Q\ R_G$
5. $1\ R_p = 1\ R_1 + 1\ R_2 + 1\ R_G$

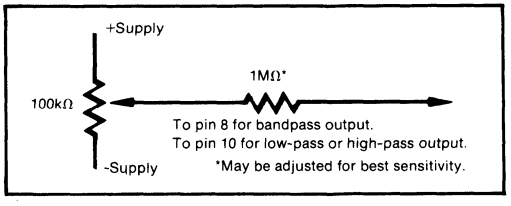
BI-QUAD CONFIGURATION

1. $\omega_o^2 = R_2 (R_1 R_{F1} C_1 R_{F2} C_2)$
2. $Q = R_Q C_2\ \omega_o$
3. $Q\ A_{LP}\ (\omega_o R_1 C2) = A_{HP} = R_Q\ R_G$

Offset Error Adjustment

DC offset errors will be minimized by grounding pin 5 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}. The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



Design Example

It is desired to design a 5-pole Bessel, Low-Pass Filter with $f_o = 3.3$kHz and $A_{LP} = 1$. We will use the UAF11 to implement this filter.

From Table II the following values of f_n and Q are obtained.

Complex Poles:
$f_n = 1.55876$
$Q = 0.56354$
$f_n = 1.75812$
$Q = 0.91652$
Simple Pole:
$f_n = 1.50470$

Using the above shown values of f_n and Q, we now will proceed to design the three stages of filter separately.

Any one of the three configurations can be used. We will select inverting configuration.

For Stage 1.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.55876 = 5144Hz$

Since $f_o > 5kHz$, equations "B" would be used, thus an 11kΩ resistor must be connected between pins 12 and 1.

$$R_{F1} = R_{F2} = \frac{5.03 \times 10^7}{5144} = 9778\Omega$$

$$f_oQ = 5144 \times 0.56354 = 2.9 \times 10^3$$

$f_oQ < 10^4$, $\therefore Q_P = Q = 0.56354$

$$A_{BP} = \frac{Q_P}{3.16} \quad A_{LP} = \frac{0.56354}{3.16} \times 1 = 0.17834$$

$$R_G = \frac{3.16 \times 10^4 Q_P}{A_{BP}} = \frac{3.16 \times 10^4 \times 0.56354}{0.17834} = 99.85k\Omega$$

$$R_Q = \frac{2 \times 10^5}{3.48Q_P + A_{BP} - 1} = \frac{2 \times 10^5}{3.48 \times 0.56354 + 0.17834 - 1} = 175.52k\Omega$$

For Stage 2.

$f_o = 3.3kHz \times f_n = 3.3kHz \times 1.75812 = 5802Hz$

Since $f_o > 5kHz$, equations "B" would again be used, and an 11kΩ resistor would be connected between pins 12 and 1 of the second UAF stage.

$$R_{F1} = R_{F2} = \frac{5.03 \times 10^7}{5802} = 8669\Omega$$

$$f_oQ = 5802 \times 0.91652 = 5.32 \times 10^3$$

$f_oQ < 10^4$, $\therefore Q_P = Q = 0.91652$

$$A_{BP} = \frac{Q_P}{3.16} \quad A_{LP} = \frac{0.91652}{3.16} \times 1 = 0.29004$$

$$R_G = \frac{3.16 \times 10^4 Q_P}{A_{BP}} = \frac{3.16 \times 10^4 \times 0.91652}{0.29004} = 99.86k\Omega$$

$$R_Q = \frac{2 \times 10^5}{(3.48Q_P + A_{BP} - 1)} = \frac{2 \times 10^5}{(3.48 \times 0.91652 + 0.29004 - 1)} = 80.66k\Omega$$

For Stage 3.

$f = 3.3kHz \times f_n = 3.3kHz \times 1.50470 = 4966Hz$

For the simple pole,

$$RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 4966} = 3.2049 \times 10^{-5}$$

3300pF (or any convenient value)

$$R = \frac{3.2049 \times 10^{-5}}{3300 \times 10^{-12}} = 9.71k\Omega$$

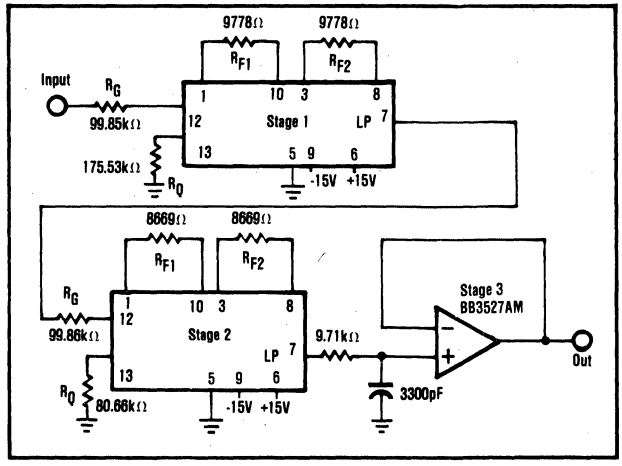


FIGURE 6. Overall Circuit.

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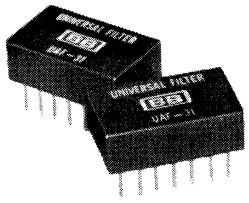
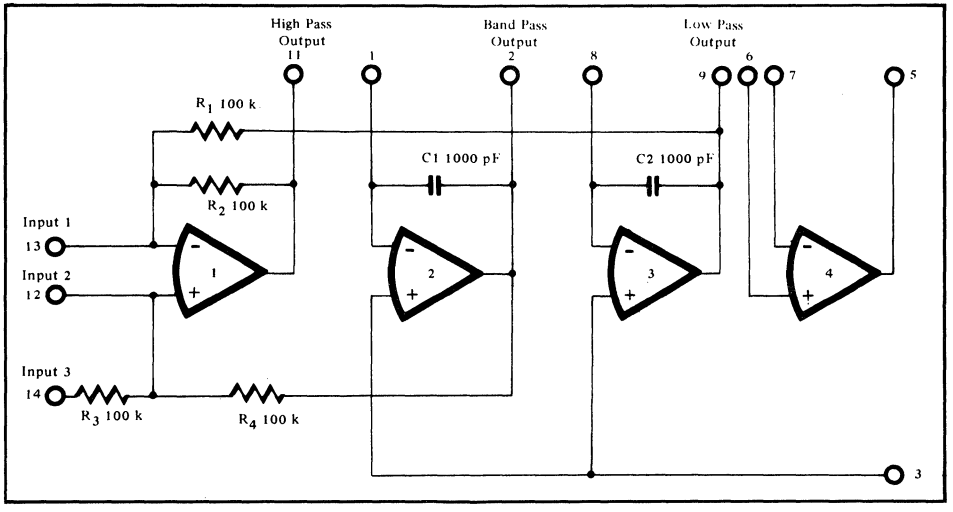


UAF31

UNIVERSAL ACTIVE FILTER



FEATURES

- **LOW COST**
- **SAVES DESIGN TIME**
  - **Calculate only three resistance values**
  - **Design directly from this data sheet**
  - **Completely characterized parameters**
- **IMPROVED PERFORMANCE**
  - **1% frequency accuracy**
  - **Uncommitted op amp included**
  - **Q range of 0.5 to 500**
  - **Reliable hybrid construction**
  - **NPO capacitors and thin-film resistors**

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PDS-318B

DESCRIPTION

The UAF31 is a versatile 2-pole active filter which, with the addition of three or four external resistors, provides the user easy control of the Q-factor, resonant frequency and gain. Any complex filter response can be obtained by cascading units. The UAF31 is an ideal building block that can be purchased and stocked in quantity to be used whenever the requirement for a filter arises. In this way filters are available immediately and may be purchased in volume to take advantage of quantity price discounts.

Three separate outputs provide low pass, high pass, and band pass transfer functions. A band reject (notch) transfer function may be realized simply by summing the high pass and low pass outputs. The UAF31 also includes an uncommitted op amp that may be used as an input or output buffer or to add an additional one-pole response to the filter.

TRANSFER FUNCTION

The UAF31 uses the state variable technique to produce a basic second order transfer function. The equations describing the three outputs available are:

$$T(\text{Low Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\, s + \omega_o^2}$$

$$T(\text{Band Pass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)\, s + \omega_o^2}$$

$$T(\text{High Pass}) = \frac{A_{HP}\, s^2}{s^2 + (\omega_o/Q)\, s + \omega_o^2}$$

To obtain band reject characteristics the low pass and high pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2+(\omega_o/Q)\, s + \omega_o^2} \text{ where } A_{LP}=A_{HP}=A.$$

The state variable approach uses two op amp integrators (#2 and #3 in the simplified schematic below) and a summing amplifier (#1) to provide simultaneous low pass, band pass and high pass responses. One UAF31 is required for each two poles of low pass or high pass filters and for each pole-pair of band pass or band reject filters.

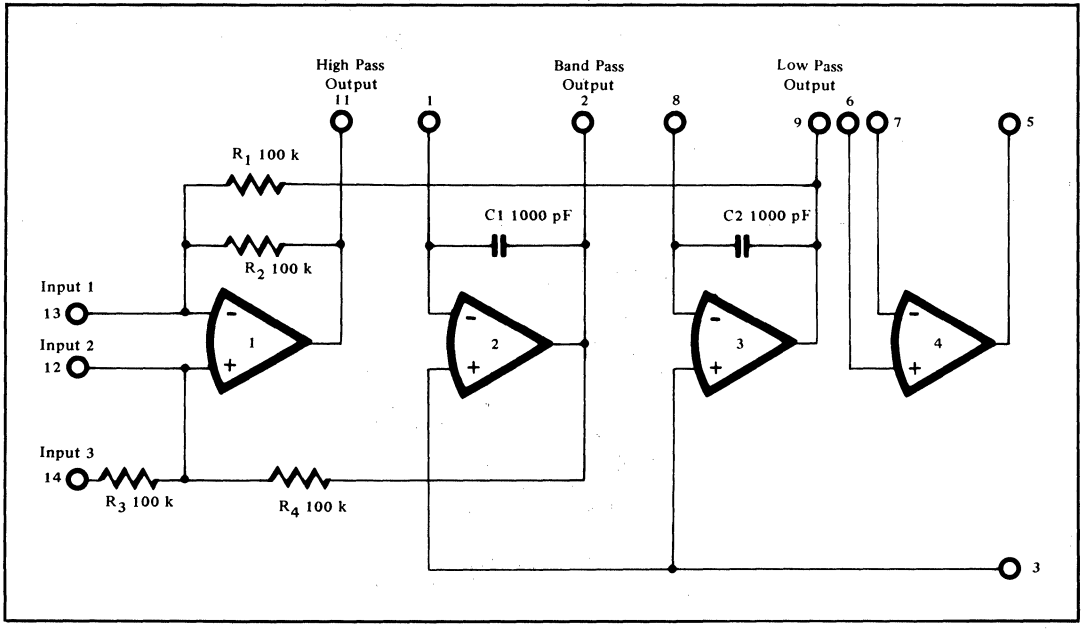


FIGURE 1. UAF31 Schematic.

SPECIFICATIONS

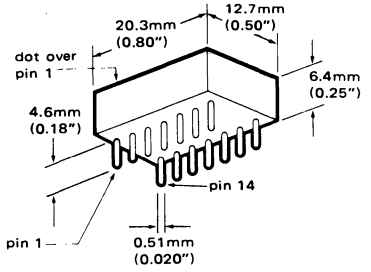
ELECTRICAL

Typical at 25°C and with rated supply unless otherwise noted.

MODEL	UAF31
INPUT	
Input Bias Current	±40 nA
Input Voltage Range	±10 V
Input Resistance	100 kΩ
TRANSFER CHARACTERISTICS	
Frequency Range (f_o)	0.001 to 25 kHz
f_o Accuracy(1), max	±1%
f_o Stability(2)	±0.002%/°C
Q Range(3)	0.5-500
Q Stability(4)	
@f_o Q ≤ 10^4	±0.01%/°C
@f_o Q ≤ 10^5	±0.025%/°C
Q Repeatability	±10%
Gain Range	0.1 to 50V/V
OUTPUT	
Peak to Peak Output Swing(5)	20 V
Output Offset	
(at L.P. output with unity gain)	±20 mV
Output Impedance	1 Ω
Noise(6)	200 μV (rms)
Output Current(7)	5 mA
UNCOMMITTED AMP CHARACTERISTICS	
Input Offset Voltage	5 mV
Input Bias Current	40 nA
Input Impedance	1 MΩ
Large Signal Voltage Gain	85 dB
Output Current	5 mA
POWER SUPPLIES	
Rated Power Supplies	±15 V
Power Supply Range(8)	±5 to ±18 V
Supply Current @ ±15 V(Quiescent), max	12 mA
TEMPERATURE RANGE	
Specification Temperature Range	-25 to +85°C
Storage Temperature Range	-25 to +85°C

(1) The tolerance of external frequency determining resistors must be added to this figure.
(2) T.C.R. of external frequency determining resistors must be added to this figure.
(3) See figure 3 for Q vs. F curve.
(4) Q stability varies with both the value of Q and the resonant frequency f_o.
(5) See figure 2 for full power response curve.
(6) Measured at the band pass output with Q @ 50 over DC to 50 kHz.
(7) The current required to drive R_{F1} and C_1 and C_2 must come from this current.
(8) For supplies below ±10 V, Q max will decrease slightly; filters will operate below ±5 V.

MECHANICAL



ROW SPACING—7.6 (0.300")
WEIGHT—.12 oz. (3.4)
CONNECTOR—14 pin DIP connector

Pin material and plating composition conform to method 208 (solderability) of MIL-STD-202.

PIN CONNECTIONS

Pin 1—Frequency Adjust
Pin 2—Band pass Output
Pin 3—Common
Pin 4—Positive Supply
Pin 5—Auxiliary Amp. Output
Pin 6—Auxiliary Amp + Input
Pin 7—Auxiliary Amp - Input
Pin 8—Frequency Adjust
Pin 9—Low Pass Output
Pin 10—Negative Supply
Pin 11—High Pass Output
Pin 12—Filter Input 2
Pin 13—Filter Input 1
Pin 14—Filter Input 3

TYPICAL PERFORMANCE CURVES

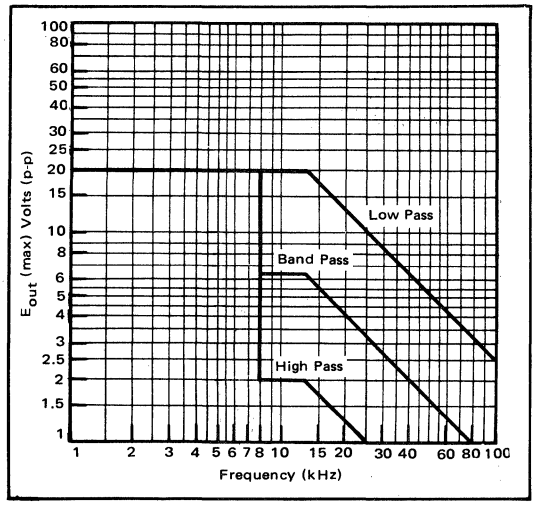


FIGURE 2. Full Power Response

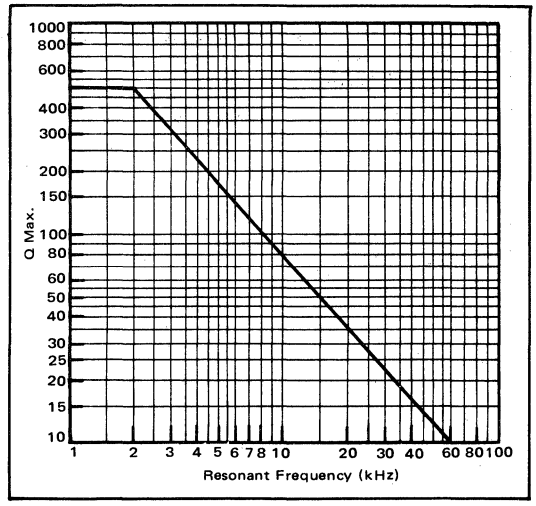


FIGURE 3. Q Max. vs. Resonant Frequency

ACTIVE FILTER DESIGN PROCEDURE

To design filters using the circuits shown on the following pages, these six design steps should be followed:

1. Determine f_o, the natural frequency of the pole pair.
2. Determine A, the gain of the filter section (V/V).
3. Determine the Q factor.
4. Calculate Q_p as shown in the Q factor design notes to compensate for amplifier phase shift errors.
5. Determine the filter configuration that will be used (see configuration selection guide on the opposite page for recommendations).
6. Calculate the resistance values required using the design equations for the filter configuration selected.

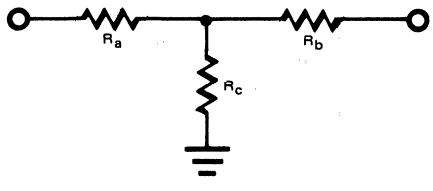
NATURAL FREQUENCY (f_o) DESIGN NOTES

f_o values for many low pass and high pass filters are given in the filter parameter table on page 5-107.

f_o for each one pole-pair band pass filter is the center frequency (f_c). f_c is defined as $f_c = \sqrt{f_1 f_2}$ when f_1 is the lower 3 dB point and f_2 is the upper 3 dB point of the filter.

To use the UAF31 with f_o above 8 kHz, an 11 kΩ resistor must be placed in parallel with R_2 (between pins 13 and 11). For the higher frequencies where an 11 kΩ resistor is required, use simplified design equations "B". For operation below these frequencies; use simplified design equations "A" or "B".

To obtain f_o below 100 Hz using practical resistor values, T-networks may be used for the frequency determining resistors (R_{F1} and R_{F2}).



The equivalent resistance if inserted between pins 1 and 11 or pins 2 and 8 is

$$R = \frac{R_a R_b}{R_c} + R_a + R_b$$

Capacitors may also be paralleled with C_1 and C_2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}(\text{new}) = R_{F2}(\text{new}) = R_{F1}(\text{old}) \frac{1000\ \text{pF}}{C + 1000\ \text{pF}}$$

where R_F(new) are the new lower value frequency resistors, C is the value of the two external capacitors placed across C_1 and C_2 (between pins 1 and 2 and pins 8 and 9), R_{F1} (old) is the value calculated in the simplified design equations.

GAIN (A) DESIGN NOTES

The gain (V/V) of the filter section is:

A_{LP} - for low pass output - gain at DC.

A_{BP} - for band pass output - gain at f_o.

A_{HP} - for high pass output - gain at high frequencies.

Q FACTOR DESIGN NOTES

For band pass filters $Q = \frac{f_o}{3\text{ dB bandwidth}}$

Q values for many low pass and high pass filters are given in the pole position table on page 5-107.

A FORTRAN computer program to transform low pass pole positions to band pass pole positions is given on page 5-108.

When designing low pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.

Q repeatability (Q change from unit-to-unit) is typically ±5% at f_oQ products less than 10^4. The Q repeatability error increases as the f_oQ product increases, to approximately ±20% for f_oQ products near 10^6.

Calculate the f_o times Q product of the filter. If the product is above 10^4 Hz, locate the corresponding f_oQ_p product in Figure 4. Divide f_oQ_p by f_o to obtain Q_p. Use Q_p as indicated in the equations on page 5-106 to correct for amplifier phase shift errors. For f_oQ products below 10^4 Hz, simply use Q. As can be seen in Figure 4, the amplifier phase shift errors cause Q to rise with increasing f_oQ products.

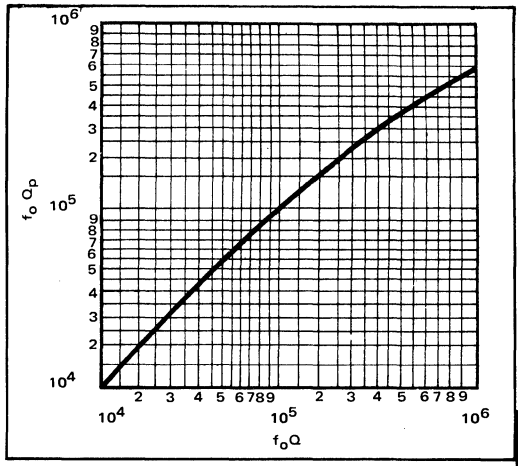


FIGURE 4. Qp Determination

NOTE: For more comprehensive detailed design procedure and illustrated examples of filter design using the Universal Active Filters, please refer to PDS-359, product data sheet for Burr-Brown model No. UAF41.

CONFIGURATION SELECTION GUIDE

	NONINVERTING INPUT	INVERTING INPUT	BI-QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Inverted Outputs	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant bandwidth
Other Advantages	May be used with only three external resistors (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2Q_p - A_{BP} > 1$ ($f_o < 8$ kHz) $3.48Q_p - A_{BP} > 1$ ($f_o > 8$ kHz)	$2Q_p + A_{BP} > 1$ ($f_o < 8$ kHz) $3.48Q_p + A_{BP} > 1$ ($f_o > 8$ kHz)	NONE

Summary: The Bi-Quad filter is particularly useful as a bandpass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a band pass or maintaining a constant response of a lowpass or highpass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than R_G and R_Q of the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 100$ k therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q).

NONINVERTING INPUT CONFIGURATION

For applications requiring a band pass gain of 1 (V/V), the internal resistor R_3 may be used (input at pin 14) as the gain resistor R_G. Thus only three external resistors are needed to configure the filter.

SIMPLIFIED DESIGN EQUATIONS "A"

$f_o < 8$ kHz

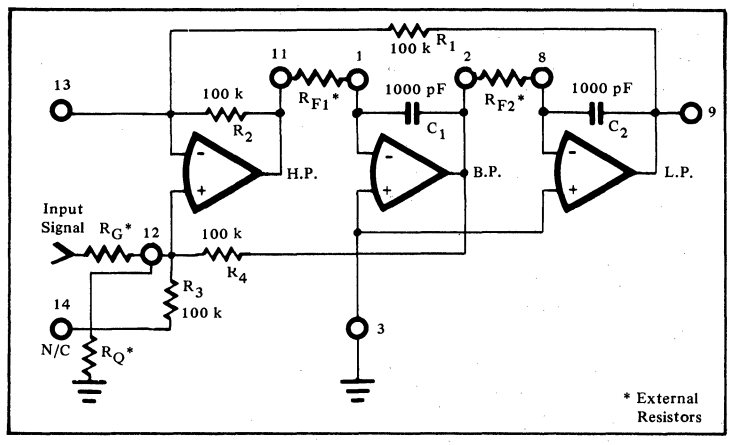
1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q\,A_{LP} = Q\,A_{HP}$
3. $R_G = \frac{10^5}{A_{BP}}\,\frac{Q}{Q_P}$
4. $R_Q = \frac{10^5}{2Q_P - \frac{A_{BP}\,Q_P}{Q} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = \frac{Q}{3.16}\,A_{LP} = 3.16\,Q\,A_{HP}$
3. $R_G = \frac{10^5}{A_{BP}}\,\frac{Q}{Q_P}$
4. $R_Q = \frac{10^5}{3.48\,Q_P - A_{BP}\,Q_P/Q - 1}$

* To use equations "B" connect an 11 k resistor between pins 11 and 13. Equations "B" are also valid for frequencies below 8 kHz.



INVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

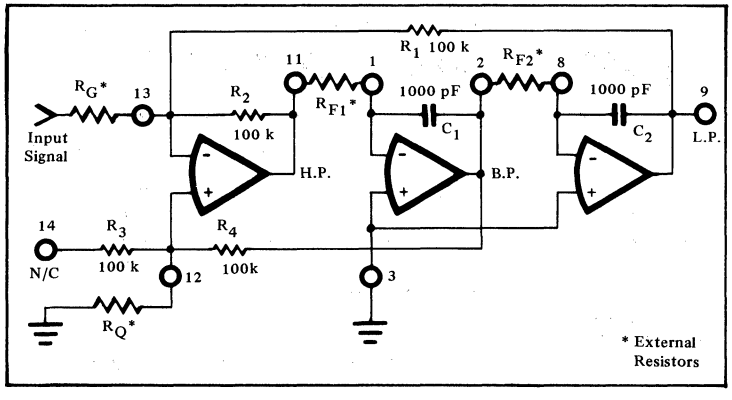
$f_o < 8$ kHz

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q_P\,A_{LP} = Q_P\,A_{HP}$
3. $R_G = \frac{10^5\,Q_P}{A_{BP}}$
4. $R_Q = \frac{10^5}{2Q_P + A_{BP} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = \frac{Q_P}{3.16}\,A_{LP} = 3.16\,Q_P\,A_{HP}$
3. $R_G = \frac{3.16 \times 10^4\,Q_P}{A_{BP}}$
4. $R_Q = \frac{10^5}{3.48\,Q_P + A_{BP} - 1}$



BI-QUAD CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

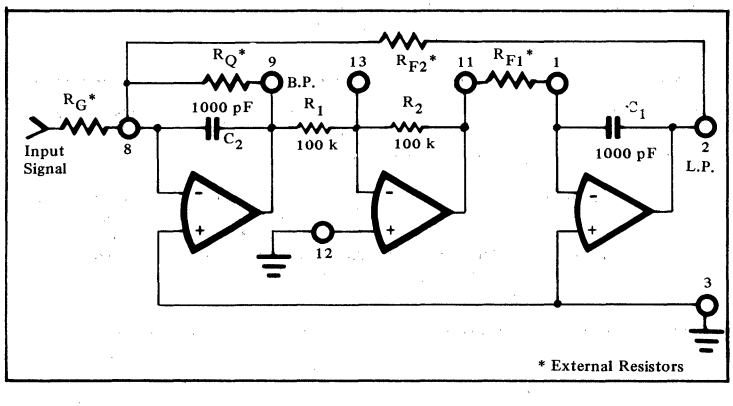
$f_o < 8$ kHz

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$
2. $A_{BP} = Q\,A_{LP}$
3. $R_Q = Q_P\,R_{F1}$
4. $R_G = \frac{R_Q}{A_{BP}}$

SIMPLIFIED DESIGN EQUATIONS "B"

$f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$
2. $A_{BP} = 3.16\,Q\,A_{LP}$
3. $R_Q = 3.16\,Q_P\,R_{F1}$
4. $R_G = \frac{R_Q}{A_{BP}}$



BAND REJECT

The band reject configuration is achieved by summing the high pass and low pass UAF outputs. The circuits shown in Figures 5 and 6 can be used to provide the band reject function if they are connected as shown in Figure 8. The Figure 8 circuit is applicable when using simplified design equations "A" ($A_{LP} = A_{HP}$), but when operating with an 11 kΩ resistor between pins 13 and 11 ($A_{LP} = 10\ A_{HP}$), the resistor at pin 9 must be 10 times the resistor at pin 11 to obtain equal passband gains above and below f_O.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_O and Q of the band reject filter desired and for A_{LP} to equal the desired passband gain. An input constraint: the input voltage times A_{BP} must not exceed the rated peak-to-peak output voltage of the band pass output, or clipping and distortion will result.

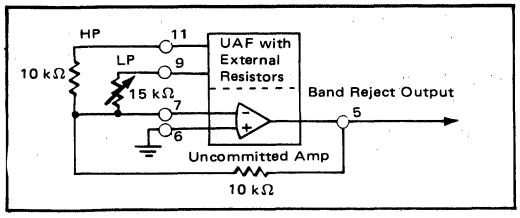


FIGURE 8. Band Reject Output

FILTER PARAMETERS

LOW PASS AND HIGH PASS

Table 1 shows filter parameters for many 2 to 8 pole low pass filters. The Q and the normalized undamped natural frequency, f_n, for each two-pole section are shown. The Q values should be used with Figure 4 and in the design formulas on page 5-106 and f_n must be multiplied by the desired cutoff frequency of the overall filter to obtain the required frequency, f_o, for the design formulas. As an example, consider a 4-pole low pass Bessel filter with a cutoff frequency of 1000Hz. The first stage would be designed to an f_o of 1432.41Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94Hz and a Q of 0.80554. The low pass output of the first stage (pin 9) should be connected to the input resistor (R_G) of the second stage.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents the simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. The uncommitted internal op amp should be used as a buffer to isolate the RC network so that the UAF input resistor will not affect the cutoff frequency of the RC network.

The cutoff frequency determined by the Table 1 filter parameters is (1) the 3 dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band and enters the stop band.

To obtain high pass pole positions, the low pass to high pass transformation may be used:

$$f_n\ (\text{high pass}) = \frac{1}{f_n\ (\text{low pass})}$$

$$Q\ (\text{high pass}) = Q\ (\text{low pass})$$

The low pass to band pass transformation is much more complicated, but it can be done using the low pass to band pass conversion program (Table III).

NUMBER OF POLES	BUTTERWORTH		BESSEL		CHEBYSCHEV 0.5 dB RIPPLE		CHEBYSCHEV 2 dB RIPPLE	
	f_n	Q	f_n	Q	f_n	Q	f_n	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	----------	1.32475	----------	0.626456	----------	0.368911	----------
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	----------	1.50470	----------	0.362320	----------	0.218308	----------
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	----------	1.68713	----------	0.256170	----------	0.155410	----------
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67657	0.237699	0.89236
	1.0	0.60134	1.83514	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5305	0.990142	18.6873

TABLE 1. Low Pass Filter Parameters

LOW PASS CHEBYSCHEV

Table II details a FORTRAN program to determine f_n and Q for a Chebyschev low pass filter. The only inputs required are the number of poles and the peak to peak ripple (dB) of the desired filter. The program outputs are treated exactly as the values on the pole position table (Table 1).

BAND PASS

Table III details a FORTRAN program that may be used to transform low pass pole positions into the equivalent band pass pole positions.

Program Inputs:

1. f_n—From Table I for the low pass filter of interest.
2. Q From Table I.
3. Q_{BP}—Desired Q of the band pass filter.

For filters with an odd number of poles a Q of .5 should be used where Q is not given in Table I. The program transforms each low pass pole into a band pass pole pair. That is, using the two-pole low pass pole positions would result in the pole positions for a two pole pair, band pass filter, requiring two UAF stages. Enter 10^6 for Q when transforming zeros on the imaginary axis. This program automates the transformation $s = p/2 \pm (p/2)^2 - 1$.

```
   PI=3.1415926536
   COMPLEX P(10)
   READ 5,N,R
5 FORMAT(I2,F8.6)
   A=SQRT(EXP(R/4.3429448)-1.)
   B=1./A
   AN=ALOG(B+SQRT(B**2+1.))
   AN=AN/FLOAT(N)
   J=MOD(N,2)+N/2
   DO 10 K=1,J
   RP=SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
   XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
   WN=SQRT(RP**2+XIP**2)
   Q=-WN/(2.*RP)
   P(K)=CMPLX(WN,Q)
   IF(MOD(N,2).NE.0.AND.K.EQ.J) GO TO 15
   PRINT 20,P(K)
   GO TO 10
15 F=REAL(P(K))
   PRINT 30,F
10 CONTINUE
20 FORMAT(2X"FN="E20.8" Q = "E20.8)
30 FORMAT(2X"FN="E20.8)
   STOP
   END
```

OFFSET ERROR ADJUSTMENT

DC offset errors will be minimized by grounding pin 3 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}.

The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.

```
   COMPLEX P,S,U
   READ 5, FN, Q, QBP
5  FORMAT (3F12.5)
   Y=FN*SQRT(1.-(1./(Q*2.))**2)
   X=-FN/(Q*2.)
   P=CMPLX(X,Y)
   U=CONJG(P)
   DO 30 I=1,2
   S=P/(2.*QBP)
   P=S**2-1.
   T=ATAN2(AIMAG(P),REAL(P))
   IF(T.GE.0.) GO TO 10
   T=2.*3.14159+T
10 T=T/2.
   A=SQRT(CABS(P))*COS(T)
   B=SQRT(CABS(P))*SIN(T)
   S=S+CMPLX(A,B)
   FN=CABS(S)
   Q=-FN/(2.*REAL(S))
   PRINT 20,FN,Q
20 FORMAT (2X"FN = "F12.5" Q = "F12.5)
   IF(AIMAG(U).EQ.0.) GO TO 40
30 P=U
40 STOP
   END
```

TABLE III. Low Pass to Band Pass Transformation Program

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF31 filter components. They should be used if a detailed analysis, not covered in the simplified equations, is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \dfrac{1 + \frac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \frac{R_2}{R_1}} \left(\dfrac{R_2}{R_1} \dfrac{R_{F1} C_1}{R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{1 + \frac{R_1}{R_2}}{R_G\left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{1 + \frac{R_2}{R_1}}{R_G\left(\frac{1}{R_G} + \frac{1}{R_Q} + \frac{1}{R_4}\right)}$

6. $A_{BP} = \dfrac{R_4}{R_G}$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \left(1 + \dfrac{R_4}{R_Q}\right) \left(\dfrac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}}\right) \left(\dfrac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{R_1}{R_G}$

5. $A_{HP} = \dfrac{R_2}{R_1} A_{LP} = \dfrac{R_2}{R_G}$

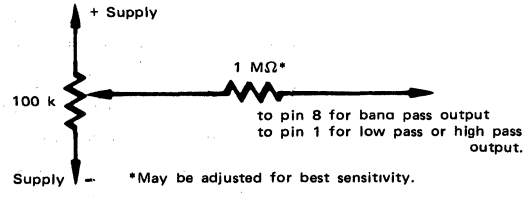
6. $A_{BP} = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{R_G\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_G}\right)}$

BI-QUAD CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} C_1 R_{F2} C_2}$

2. $Q = R_Q C_2 \omega_o$

3. $A_{BP} = \dfrac{Q A_{LP}}{\omega_o R_{F2} C_2} = \dfrac{R_Q}{R_G}$



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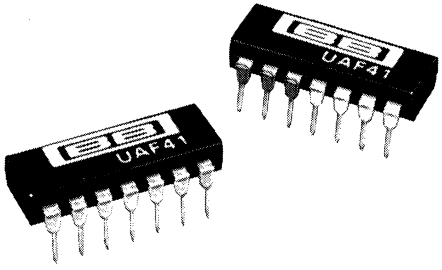

UAF41

UNIVERSAL ACTIVE FILTER

FEATURES

- LOW COST
- SMALL SIZE
  Single wide DIP package
- FULLY CHARACTERIZED PARAMETERS
- HYBRID CONSTRUCTION
- IMPROVED PERFORMANCE
  1% frequency accuracy
  Q range of 0.5 to 500
  NPO capacitors and thin-film resistors
  Uncommitted op amp included

BENEFITS

- SAVES PRINTED CIRCUIT BOARD SPACE
- SAVES DESIGN TIME
  Calculate only four resistance values
  Design directly from this data sheet
  Versatile building block for filter design
- HIGH RELIABILITY
- HIGH STABILITY

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PDS-359 Printed in U.S.A. July, 1978

DESCRIPTION

The UAF41 is a versatile 2-pole active filter. It uses a three operational amplifier double integrater feedback loop to generate a complex pole pair (two conjugate poles). The location of the poles in the complex plane (and thus the natural frequency and Q) are determined by external, user supplied resistors. Either 3 or 4 resistors are used depending on the particular configuration chosen.

The UAF41 produces three transfer functions simultaneously - low pass, high pass, and band pass - which are available at three separate outputs. The fourth basic transfer function - the band reject or notch - can be obtained simply by summing the high pass and low pass outputs using the uncommitted amplifier (A4) contained in the UAF41. The uncommitted op amp can also be used to add a single pole response for complex filters requiring an odd number of poles.

More complex higher order filters can readily be obtained by cascading UAF's. This is easily done with the UAF41 since the high input impedance and low output impedance associated with the operational amplifiers used prevents the series connected stages from interacting (e.g., no frequency pull due to following stage loading). This data sheet contains the design procedures for an easy selection of resistor values for the stagger tuning of cascaded stages.

The versatility of the UAF41 makes it a general purpose building block for a wide variety of active filter applications. Its universal nature, ease of use, small size and low cost allows the user the convenience of keeping units on hand for immediate use whenever a filter requirement arises.

TRANSFER FUNCTION

The UAF41 uses the state variable technique to produce a basic second order transfer function. The equations describing the three outputs available are:

$$T(\text{Low Pass}) = \frac{A_{LP}\omega_o^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{Band Pass}) = \frac{A_{BP}(\omega_o/Q)s}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

$$T(\text{High Pass}) = \frac{A_{HP}\,s^2}{s^2 + (\omega_o/Q)\,s + \omega_o^2}$$

To obtain band reject characteristics the low pass and high pass outputs are summed to form a pair of $j\omega$ axis zeros:

$$T(\text{Band Reject}) = \frac{A\,(s^2 + \omega_o^2)}{s^2+(\omega_o/Q)\,s + \omega_o^2}$$

where $A_{LP}=A_{HP}=A$.

The state variable approach uses two op amp integrators (A2 and A3 in the simplified schematic below) and a summing amplifier (A1) to provide simultaneous low pass, band pass and high pass responses. One UAF41 is required for each two poles of low pass or high pass filters and for each pole-pair of band pass or band reject filters.

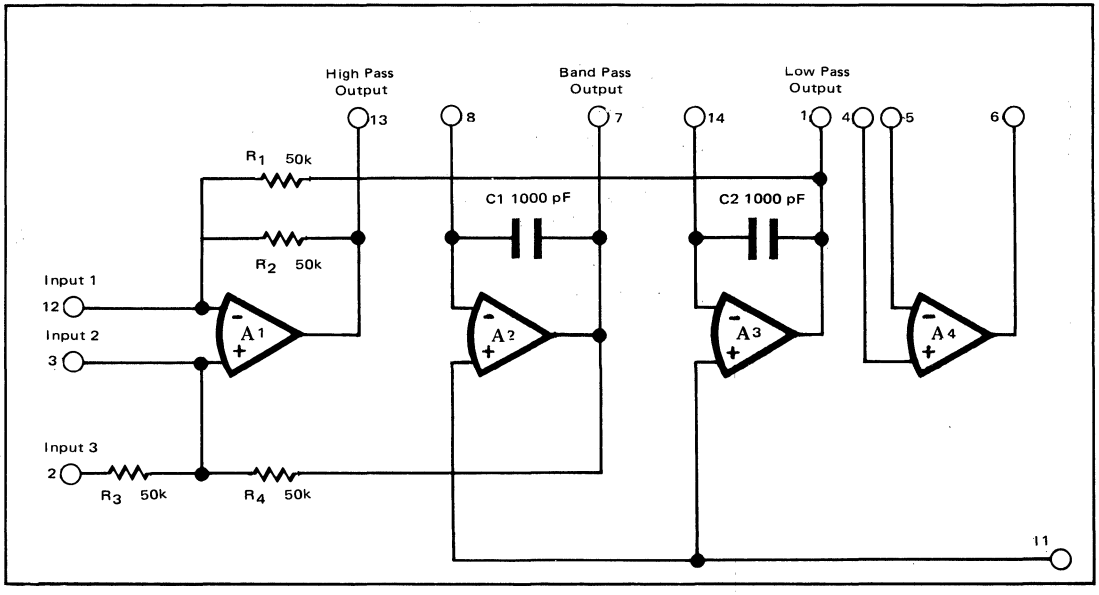


FIGURE 1. UAF41 Schematic.

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and with rated supply unless otherwise noted.

MODEL	UAF41
INPUT	
Input Bias Current	±40 nA
Input Voltage Range	±10 V
Input Resistance (1)	50 kΩ
TRANSFER CHARACTERISTICS	
Frequency Range (f_o)	0.001 to 25 kHz
f_o Accuracy(2), max	±1%
f_o Stability(3)	±0.002%/°C
Q Range(4)	0.5-500
Q Stability(5)	
@f_o Q ≤ 10^4	±0.01%/°C
@f_o Q ≤ 10^5	±0.025%/°C
Q Repeatability at f_o Q ≤ 10^5	±10%
Gain Range	0.1 to 50V/V
OUTPUT	
Peak to Peak Output Swing(6)	20 V
Output Offset(7)	
(at L.P. output with unity gain)	±20 mV
Output Impedance	1 Ω
Noise(8)	200 μV (rms)
Output Current(9)	5 mA
UNCOMMITTED AMP CHARACTERISTICS	
Input Offset Voltage	5 mV
Input Bias Current	40 nA
Input Impedance	1 MΩ
Large Signal Voltage Gain	85 dB
Output Current	5 mA
POWER SUPPLIES	
Rated Power Supplies	±15 V
Power Supply Range(10)	±5 to ±18 V
Supply Current @ ±15 V(Quiescent), max	7 mA
TEMPERATURE RANGE	
Specification Temperature Range	-25 to +85°C
Storage Temperature Range	-25 to +85°C

(1) For noninverting input configuration with A_{BP} = 1.

(2) The tolerance of external frequency determining resistors must be added to this figure.

(3) T.C.R. of external frequency determining resistors must be added to this figure.

(4) See Figure 3 for Q_{max} vs F curve.

(5) Q stability varies with both the value of Q and the resonant frequency f_o.

(6) See Figure 2 for full power response curve.

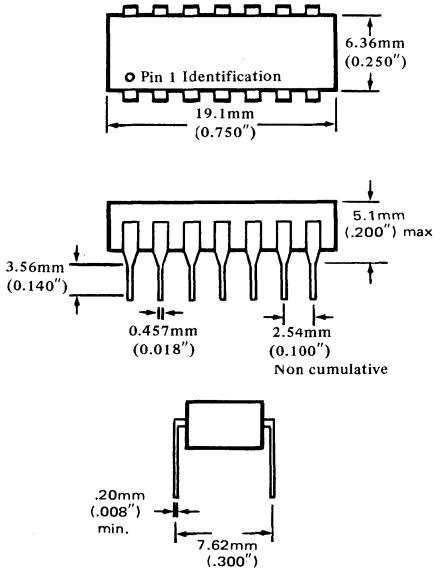
(7) $R_{F1} = R_{F2} < 100k\Omega$ at L.P. output with unity gain.

(8) Measured at the band pass output with Q @ 50 over DC to 50 kHz.

(9) The current required to drive R_{F1} and R_{F2} (external) as well as C_1 and C_2 must come from this current.

(10) For supplies below ±10V, Q_{max} will decrease slightly; filters will operate below ±5V.

MECHANICAL



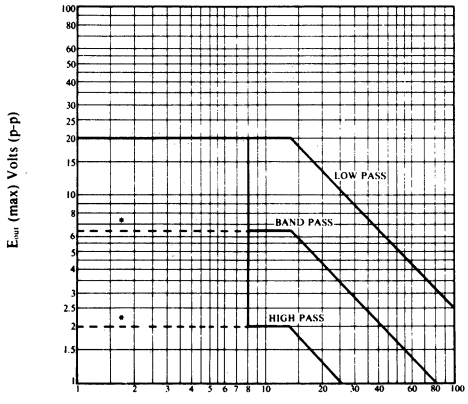
ROW SPACING - 7.63mm (0.300")
WEIGHT - 1.1gms max
CONNECTOR - 14 pin DIP connector

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

PIN CONNECTIONS

Pin 1 - Low Pass Output
Pin 2 - Filter Input 3
Pin 3 - Filter Input 2
Pin 4 - Auxiliary Amp + Input
Pin 5 - Auxiliary Amp - Input
Pin 6 - Auxiliary Amp Output
Pin 7 - Band Pass Output
Pin 8 - Frequency Adjust
Pin 9 - Negative Supply
Pin 10 - Positive Supply
Pin 11 - Common
Pin 12 - Filter Input 1
Pin 13 - High Pass Output
Pin 14 - Frequency Adjust

TYPICAL PERFORMANCE CURVES



*If Equations "B" used below 8 kHz.

FIGURE 2. Full Power Response.

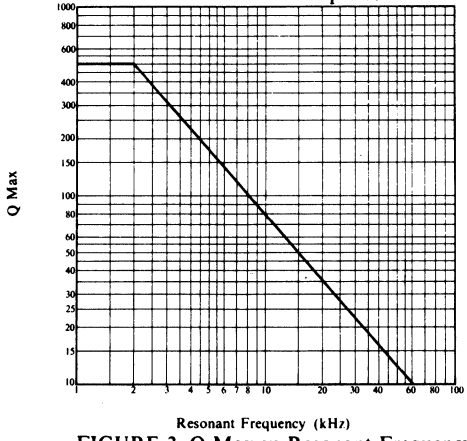


FIGURE 3. Q Max vs Resonant Frequency.

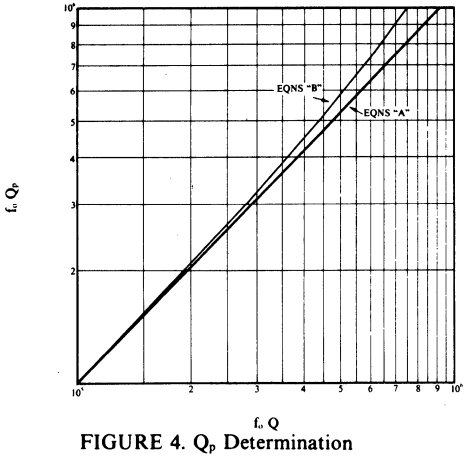


FIGURE 4. Q_p Determination

DESIGN PROCEDURE SUMMARY

This summary gives the design steps for the proper application of UAF41s and for the selection of the external components. More detailed information on filter theory pertinent to some of the steps can be found in the reference sources listed under USEFUL REFERENCES.

Burr-Brown also manufactures a line of completely self-contained active filters called the ATF76 series. These are available in most popular transfer functions with from 2 to 8 pole responses. They contain all necessary components and do not require any user design effort.

DESIGN STEPS:

1. Choose the type of transfer function (low pass, band pass, etc.), type of response (Butterworth, Bessel, etc.), number of poles, and cutoff frequency based on the particular application.

   If the transfer function is band reject see BAND REJECT TRANSFER FUNCTION, before proceeding to step 2.

2. Determine the normalized low pass filter parameters (f_n and Q) based on the type of response and number of poles selected in step 1. See NORMALIZED LOW PASS PARAMETERS.

3. If the actual response desired is low pass go to step 4. For other responses a transformation of variables must be made (low pass to band pass or low pass to high pass). See LOW PASS TRANSFORMATION.

4. Determine the actual (denormalized) cutoff frequency, f_o, by multiplying f_n by the actual desired cutoff frequency. See DENORMALIZATION OF PARAMETERS.

5. Pick the desired UAF configuration (noninverting, inverting or bi-quad) see CONFIGURATION SELECTION GUIDE, and UAF41 CONFIGURATIONS AND DESIGN EQUATIONS.

6. Decide whether to use design equations "A" or "B". See DESIGN EQUATIONS "A" AND "B".

7. Calculate R_{F1} and R_{F2}. See NATURAL FREQUENCY, and UAF CONFIGURATIONS AND DESIGN EQUATIONS.

8. Determine Q_P. See Q_P PROCEDURE.

9. Select the desired gain for each UAF and calculate the corresponding R_G and R_Q. See GAIN (A), and UAF41 CONFIGURATIONS AND DESIGN EQUATIONS.

NORMALIZED LOW PASS PARAMETERS

Usual active filter design procedure involves using normalized low pass parameters. Table I is provided to assist in this step for the more common filter responses. Table II is a FORTRAN program which allows f_n and Q to be calculated for any desired ripple and number of poles for the Chebyschev response. Consult the USEFUL REFERENCES for other information.

Note that for band pass and high pass filters complex conjugate pole pairs in the actual filter correspond to single poles in the normalized low pass model. Thus four poles in Table I would correspond to four pole pairs in a band pass or high pass filter.

Filters with an odd number of poles show one f_n with no corresponding Q value. This represents a simple RC network that is required for odd pole filters. This RC network with a cutoff frequency equal to f_n times the overall filter cutoff frequency should be placed in series with the first UAF two-pole section. The uncommitted internal op amp with an external RC network can be used for this purpose.

The cutoff frequency determined by the Table I filter parameters is (1) the -3dB frequency of the Butterworth response and of the Bessel response and (2) the frequency at which the amplitude response of the Chebyschev filters passes through the maximum ripple band (to enter the stop band).

NUMBER OF POLES	BUTTERWORTH		BESSEL		CHEBYSCHEV 0.5dB RIPPLE		CHEBYSCHEV 2dB RIPPLE	
	fn(1)	Q	fn(1)	Q	fn(2)	Q	fn(2)	Q
2	1.0	0.70711	1.2742	0.57735	1.23134	0.86372	0.907227	1.1286
3	1.0	----	1.32475	----	0.626456	----	0.368911	----
	1.0	1.0	1.44993	0.69104	1.068853	1.7062	0.941326	2.5516
4	1.0	0.54118	1.43241	0.52193	0.597002	0.70511	0.470711	0.9294
	1.0	1.3065	1.60594	0.80554	1.031270	2.9406	0.963678	4.59388
5	1.0	----	1.50470	----	0.362320	----	0.218308	----
	1.0	0.61805	1.55876	0.56354	0.690483	1.1778	0.627017	1.77509
	1.0	1.61812	1.75812	0.91652	1.017735	4.5450	0.97579	7.23228
6	1.0	0.51763	1.60653	0.51032	0.396229	0.68364	0.31611	0.9016
	1.0	0.70711	1.69186	0.61120	0.768121	1.8104	0.730027	2.84426
	1.0	1.93349	1.90782	1.0233	1.011446	6.5128	0.982828	10.4616
7	1.0	----	1.68713	----	0.256170	----	0.155410	----
	1.0	0.55497	1.71911	0.53235	0.503863	1.0916	0.460853	1.64642
	1.0	0.80192	1.82539	0.66083	0.822729	2.5755	0.797114	4.11507
	1.0	2.2472	2.05279	1.1263	1.008022	8.8418	0.987226	14.2802
8	1.0	0.50980	1.78143	0.50599	0.296736	0.67657	0.237699	0.89236
	1.0	0.60134	1.83514	0.55961	0.598874	1.6107	0.571925	2.5327
	1.0	0.89998	1.95645	0.71085	0.861007	3.4657	0.842486	5.58354
	1.0	2.5629	2.19237	1.2257	1.005984	11.5305	0.990142	18.6873

(1) -3 dB Frequency
(2) Frequency at which amplitude response passes through the ripple band.

TABLE I. Low Pass Filter Parameters.

NORMALIZED LOW PASS CHEBYSCHEV

Table II gives a FORTRAN program for the determination of f_n and Q for a general normalized Chebyschev low pass filter of any ripple and number of poles. Program inputs are the number of poles (N) and the peak-to-peak ripple (R). Program outputs are f_n and Q, which are used exactly as the values taken from Table I.

```
      PI=3.1415926536
      COMPLEX P(10)
      READ 5, N,R
    5 FORMAT (12, F8, 6)
      A=SQRT (EXP(R/4.3429448)-1)
      B=1./A
      AN=ALOG(B+SQRT(B**2+1.))
      AN=AN/FLOAT(N)
      J=MOD(N,2)+N/2
      DO 10 K=1, J
      RP=SINH(AN)*SIN(PI*FLOAT(2*K-1)/FLOAT(2*N))
      XIP=COSH(AN)*COS(PI*FLOAT(2*K-1)/FLOAT(2*N))
      WN=SQRT(RP**2+XIP**2)
      Q=-WN/(2.*RP)
      P(K)=CMPLX(WN,Q)
      IF(MOD(N,2).NE.0 AND.K.E Q.J)GO TO 15
      PRINT 20, P(K)
      GO TO 10
   15 F=REAL(P(K))
      PRINT 30, F
   10 CONTINUE
   20 FORMAT(2X"FN="E20.8"Q="E20.8)
   30 FORMAT(2X"FN="E20.8)
      STOP
      END
```

TABLE II. Low Pass Chebyschev Program

BAND REJECT TRANSFER FUNCTION

The band reject is achieved by summing the high pass and low pass UAF outputs. Either of the configurations in Figures 6 and 7 can be used to provide the band reject function if they are used as shown in Figure 5.

The 15kΩ resistor is adjusted for maximum rejection. The circuit in Figure 5 is applicable when using design equations "A" ($A_{LP} = A_{HP}$). When design equations "B" are used ($A_{LP} = 10A_{HP}$), the resistor at pin 1 must be 10 times the resistor at pin 13 to obtain equal pass band gains above and below f_n.

In either case, the four external UAF resistors (R_G, R_Q, R_{F1} and R_{F2}) should be calculated for f_o and Q of the band reject filter desired and for A_{LP} to equal the desired passband gain. An input constraint is that the input voltage times A_{BP} must not exceed the rated peak-to-peak voltage of the band pass output, or clipping will result.

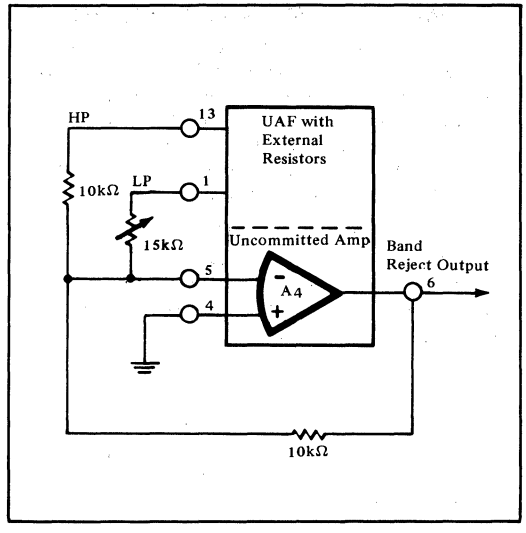


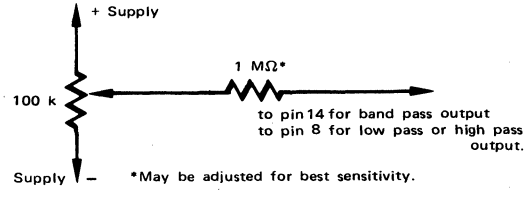
FIGURE 5. Band Reject Configuration.

OFFSET ERROR ADJUSTMENT

DC offset errors will be minimized by grounding pin 3 through a resistor equal to 1/2 the value of R_{F1} or R_{F2}.

The DC offset adjustment shown here may be used if required.

Offset errors will increase with increases in R_F.



LOW PASS TRANSFORMATION

LOW PASS TO HIGH PASS

The following simple transformation may be used for high pass filters:

$$f_n \text{ (high pass)} = \frac{1}{f_n \text{ (low pass)}}$$

$$Q \text{ (high pass)} = Q \text{ (low pass)}$$

LOW PASS TO BAND PASS

The low pass to band pass transformation to generate f_n (band pass) and Q (band pass) is much more complicated. It is tedious to do by hand but can be accomplished with the FORTRAN program given in Table III. This program automates the transformation

$$s = p/2 \pm \sqrt{(p/2)^2 - 1}.$$

```
      COMPLEX P,S,U
      READ 5, FN, Q, QBP
    5 FORMAT (3F12.5)
      Y=FN*SQRT(1.-(1./(Q*2.))**2)
      X=-FN/(Q*2)
      P=CMPLX(X,Y)
      U=CONJG(P)
      DO 30 I=1,2
      S=P/(2.*QBP)
      P=S**2-1.
      T=ATAN2(AIMAG(P),REAL(P))
      IF(T.GE.0) GO TO 10
      T=2.*3.14159+T
   10 T=T/2
      A=SQRT(CABS(P))*COS(T)
      B=SQRT(CABS(P))*SIN(T)
      S=S+CMPLX(A,B)
      FN=CABS(S)
      Q=-FN/(2.*REAL(S))
      PRINT 20, FN,Q
   20 FORMAT (2X"FN = "F12.5" Q = "F12.5)
      IF(AIMAG(U).EQ.0) GO TO 40
   30 P=U
   40 STOP
      END
```

TABLE III. Low Pass to Band Pass Transformation Program

PROGRAM INPUTS:

1. f_n - From Table I for the low pass filter of interest
2. Q - From Table I
3. Q_{BP} - Desired Q of the band pass filter

For filters with an odd number of poles a Q of 0.5 should be used where Q is not given in Table I. Enter 10^5 for Q when transforming zeros on the imaginary axis.

The program transforms each low pass pole into a band pass pole pair. Thus a three-pole low pass input, would result in the pole positions for a three pole pair band pass filter requiring three UAF stages.

DENORMALIZATION OF PARAMETERS

Table I shows filter parameters for many 2 to 8 pole normalized low pass filters. The Q and the normalized undamped natural frequency, f_n for each two-pole section are shown. The Q values do not have to be denormalized and may be used directly as described in the DESIGN PROCEDURE SUMMARY. f_n must be denormalized by multiplying it by the desired cutoff frequency of the actual overall filter to obtain the required frequency, f_o for the design formulas. As an example, consider a 4-pole low pass Bessel filter with a cutoff frequency of 1000 Hz. The first stage would be designed to an f_o of 1432.41 Hz and a Q of 0.52193 while the second stage would have an f_o of 1605.94 Hz and a Q of 0.80554. To combine the two stages into the composite filter the low pass output of the first stage (pin 1) would be connected to the input resistors (R_G) of the second stage.

DESIGN EQUATIONS "A" AND "B"

1. For f_o below 8 kHz, either of equations "A" or "B" may be used.

2. For f_o above 8 kHz, equations "B" must be used. If equations "A" were used above 8 kHz, the filter could become unstable.

3. Equations "A" are for the UAF as it is supplied. When using equations "B", a 5.49kΩ resistor must be placed in parallel with R_2 (between pins 12 and 13).

4. The values of R_{F1} and R_{F2} calculated with equations "B" are approximately one-third of those calculated with equations "A". Thus there may be an advantage in using equation "B" at low frequencies. Using equation "B" would require use of one more resistor, but that would not alter or affect filter performance in any manner.

5. Using the negative gain values for A_{LP} or A_{HP} or A_{BP} could result in the negative values for resistors R_G and R_Q. So the absolute value of the gain should always be used in the equations.

GAIN (A)

1. The gain (V/V) of each filter section is:
   A_{LP} - for low pass output - gain at DC
   A_{BP} - for band pass output - gain at f_0
   A_{HP} - for high pass output - gain at high frequencies.
2. Refer to Figure 2 for full power response. When selecting the gain, insure that the limits of the curve are not exceeded for the desired voltage range.

NATURAL FREQUENCY (f_o)

1. f_o for each one pole-pair band pass filter is the center frequency (f_C). f_C is defined as $f_C = \sqrt{f_1 f_2}$ where f_1 is the lower -3 dB point and f_2 is the upper -3 dB point of the pole pair response.
2. To obtain f_o below 100 Hz using practical resistor values, capacitors may be paralleled with C_1 and C_2 to reduce the size of R_{F1} and R_{F2}. If capacitors are added in parallel,

$$R_{F1}\text{ (new)} = R_{F2}\text{ (new)} = R_{F1}\text{ (old)}\ \frac{1000\text{ pF}}{C + 1000\text{ pF}}$$

where R_F (new) is the new lower value frequency resistor, C is the value of the two external capacitors placed across C_1 and C_2 (between pins 7 and 8 and pins 1 and 14 and R_{F1} (old) is the value calculated in the simplified design equations.

Q-FACTOR

1. For band pass filters $Q = \frac{f_o}{3\text{ dB bandwidth}}$.

2. When designing low pass filters of more than two poles, best results will be obtained if the two pole sections with lower Q are followed by the sections with higher Q. This will eliminate any possibility of clipping due to high gain ripple in high Q sections.
3. Q repeatability (Q change from unit-to-unit) is typically ±5% for f_oQ products less than 10^4. The Q repeatability error increases as the f_oQ product increases to approximately ±10% for f_oQ products near 10^5.

Q_P PROCEDURE

1. If the "f_o times Q" product is greater than 10^5, it is possible for the measured filter Q to be different from the calculated value of Q. This effect is the result of non-ideal characteristics of operational amplifiers. It can be compensated for by introducing the parameter Qp into the design equations.
2. Calculate the f_oQ product for the filter. If the product is above 10^5 Hz, locate the corresponding f_oQ_P product in Figure 4. Divide f_oQ_P by f_o to obtain Q_P. Use Q_P as indicated in the design equations. For f_oQ products below 10^5 Hz, $Q_P = Q$.

CONFIGURATION SELECTION GUIDE

It is possible to configure the UAF41 three different ways. Each configuration produces features that may or may not be desirable for a specific application. This selection guide is given to assist in determining the most advantageous configuration for a particular application.

	NONINVERTING INPUT	INVERTING INPUT	BI QUAD
Outputs Available	BP, LP and HP	BP, LP and HP	BP and LP
Outputs Inverted with respect to the Input	BP	HP and LP	BP and LP
Q & Gain Independent of Frequency Resistors?	Yes	Yes	No
Type of Q Variation With Changes in R_F	Constant Q	Constant Q	Constant Bandwidth
Other Advantages	May eliminate one external resistor (use internal R_3 as R_G)		R_G and R_Q are small at high frequencies
Parameter Limitations	$2Q_p - A_{BP} > 1$ (Eqns. "A") $3.48Q_p - A_{BP} > 1$ (Eqns. "B")	$2Q_p + A_{BP} > 1$ (Eqns. "A") $3.48Q_p + A_{BP} > 1$ (Eqns. "B")	No HP Output

Summary: The Bi-Quad filter is particularly useful as a band pass filter if the filter bandwidth must be kept constant as the center frequency is varied. If Q must be kept constant (i.e., constant Q of a band pass or maintaining a constant response of a low pass or high pass) one of the other two configurations should be used. The Bi-Quad also has the advantage that R_G and R_Q are smaller than with the other two configurations (this is especially useful at high frequencies). The noninverting input configuration has the advantage that for $A_{BP} = 1$, $R_G = 50k\Omega$; therefore R_3 (internal) may be used so that only three external resistors are needed (R_{F1}, R_{F2}, R_Q).

UAF41 CONFIGURATIONS AND DESIGN EQUATIONS

NONINVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q\,A_{LP} = Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q}{A_{BP}\,Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{2Q_P - \frac{A_{BP}\,Q_P}{Q} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = \frac{Q}{3.16} A_{LP} = 3.16\,Q\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q}{A_{BP}\,Q_P}$

4. $R_Q = \frac{5.0 \times 10^4}{3.48Q_p - \frac{A_{BP}\,Q_P}{Q} - 1}$

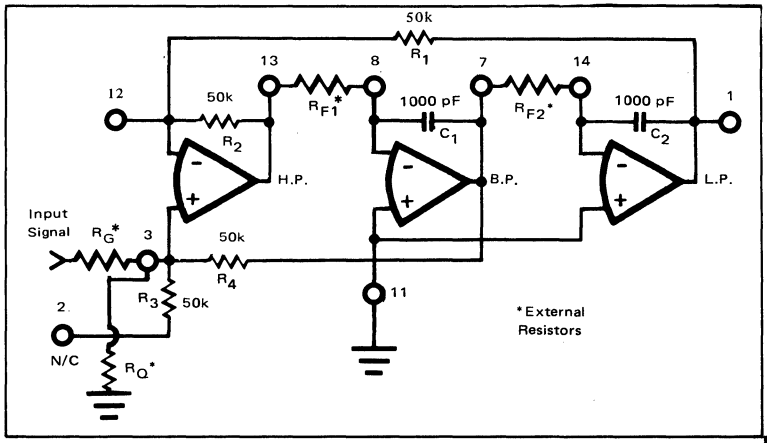


FIGURE 6. Noninverting Input Configuration.

INVERTING INPUT CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q_P\,A_{LP} = Q_P\,A_{HP}$

3. $R_G = \frac{5.0 \times 10^4\,Q_P}{A_{BP}}$

4. $R_Q = \frac{5.0 \times 10^4}{2Q_P + A_{BP} - 1}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = \frac{Q_P}{3.16} A_{LP} = 3.16\,Q_P\,A_{HP}$

3. $R_G = \frac{1.58 \times 10^4\,Q_P}{A_{BP}}$

4. $R_Q = \frac{5.0 \times 10^4}{3.48\,Q_P + A_{BP} - 1}$

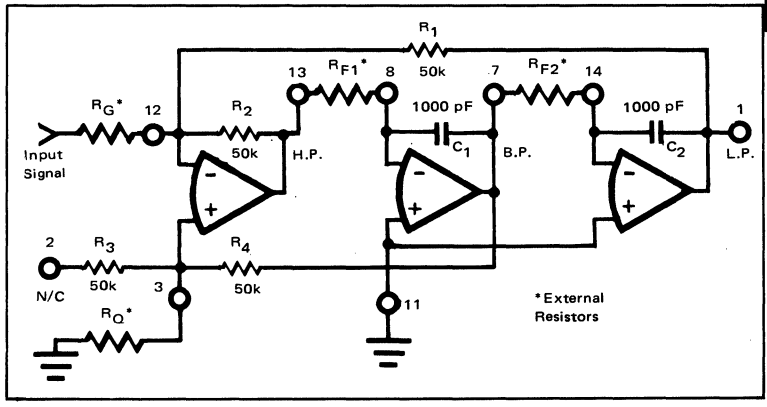


FIGURE 7. Inverting Input Configuration.

BI-QUAD CONFIGURATION

SIMPLIFIED DESIGN EQUATIONS "A"

1. $R_{F1} = R_{F2} = \frac{10^9}{\omega_o} = \frac{1.592 \times 10^8}{f_o}$

2. $A_{BP} = Q\,A_{LP}$

3. $R_Q = Q_P\,R_{F1}$

4. $R_G = \frac{R_Q}{A_{BP}}$

SIMPLIFIED DESIGN EQUATIONS "B" †

Must be used for $f_o \geq 8$ kHz

1. $R_{F1} = R_{F2} = \frac{\sqrt{10} \times 10^8}{\omega_o} = \frac{5.033 \times 10^7}{f_o}$

2. $A_{BP} = 3.16\,Q\,A_{LP}$

3. $R_Q = 3.16\,Q_P\,R_{F1}$

4. $R_G = \frac{R_Q}{A_{BP}}$

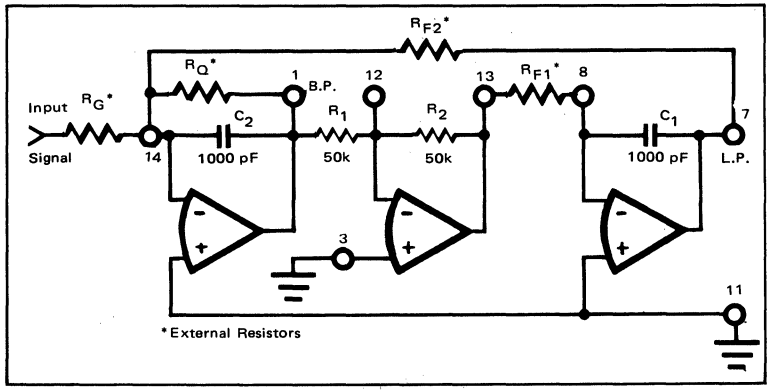


FIGURE 8. Bi-Quad Configuration.

† To use equations "B" connect a 5.49k resistor between pins 12 and 13.
Equations "B" are also valid for frequencies below 8kHz.

DETAILED TRANSFER FUNCTION EQUATIONS

The following equations show the action of all the internal and external UAF41 filter components. They are not required for regular design procedure, but could be used if a detailed analysis is required.

NONINVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \dfrac{1 + \dfrac{R_4 (R_G + R_Q)}{R_G R_Q}}{1 + \dfrac{R_2}{R_1}} \left(\dfrac{R_2 R_{F1} C_1}{R_1 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{1 + \dfrac{R_1}{R_2}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4}\right)}$

5. $A_{HP} = \dfrac{R_2}{R_1} \quad A_{LP} = \dfrac{1 + \dfrac{R_2}{R_1}}{R_G \left(\dfrac{1}{R_G} + \dfrac{1}{R_Q} + \dfrac{1}{R_4}\right)}$

6. $A_{BP} = \dfrac{R_4}{R_G}$

INVERTING INPUT CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = \left(1 + \dfrac{R_4}{R_Q}\right) \left(\dfrac{1}{\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_G}}\right) \left(\dfrac{R_{F1} C_1}{R_1 R_2 R_{F2} C_2}\right)^{1/2}$

3. $Q A_{LP} = Q A_{HP} \left(\dfrac{R_1}{R_2}\right) = A_{BP} \left(\dfrac{R_1 R_{F1} C_1}{R_2 R_{F2} C_2}\right)^{1/2}$

4. $A_{LP} = \dfrac{R_1}{R_G}$

5. $A_{HP} = \dfrac{R_2}{R_1} \quad A_{LP} = \dfrac{R_2}{R_G}$

6. $A_{BP} = \left(1 + \dfrac{R_4}{R_Q}\right) \dfrac{1}{R_G \left(\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_G}\right)}$

BI-QUAD CONFIGURATION

1. $\omega_o^2 = \dfrac{R_2}{R_1 R_{F1} R_{F2} C_1 C_2}$

2. $Q = R_Q C_2 \omega_o$

3. $A_{BP} = \dfrac{Q A_{LP}}{\omega_o R_{F2} C_2} = \dfrac{R_Q}{}$

ACTIVE FILTER DESIGN EXAMPLES USING THE DESIGN PROCEDURE OUTLINED IN DESIGN STEPS SECTION.

Example 1.

It is desired to design a 3 pole, 0.5dB ripple, Chebyschev High Pass Filter; the cut off frequency $f_c = 2$ kHz, Gain $A_{HP} = +1$.

Step 1.

The type of transfer function (high pass), the type of response (Chebyschev), number of poles (3), and the cut off frequency (f_c) are chosen depending upon the particular application and are stated in the example.

Step 2.

Normalized low pass filter parameters f_n and Q are obtained from Table I (or from program shown in Table II).

Complex Poles:

$f_n = 1.068853$
$Q = 1.7062$

Simple Pole:

$f_n = 0.626456$

Step 3.

Now, since the actual response desired is high pass,the low pass to high pass transformation must be made as shown in LOW PASS TRANSFORMATION.

f_n (high pass) $= \dfrac{1}{f_n \text{ (low pass)}}$, $Q_{HP} = Q_{LP}$

$\therefore$ For Complex Poles:

$f_n = \dfrac{1}{1.068853} = 0.935582$

and $Q = 1.7062$

For Simple Pole: $f_n = \dfrac{1}{0.626456} = 1.596281$

Step 4.

Now, determine the actual (denormalized) frequency.

$f_o = f_c \times f_n = 2 \text{ kHz} \times 0.935582$

$= 1871.2$ Hz

Step 5.

Refer to the CONFIGURATION SELECTION GUIDE. Since the gain required is positive, the HP output is not inverted with respect to the input. Therefore, the noninverting input configuration must be selected. Note that the HP output is not available with the Bi-Quad configuration.

Step 6.

Since $f_o < 8$ kHz, Equations "A" would be used.

Step 7.

For the Complex Poles Stage of the filter, using the equations "A",

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{1871.2} = 85.08\ k\Omega$$

Step 8.

$f_o Q = 1871.2 \times 1.7062 = 3.19 \times 10^3$

$\therefore f_o Q < 10^5$

$\therefore Q_P = Q = 1.7062$

Step 9.

$A_{BP} = Q_P \times A_{HP} = 1.7062 \times 1 = 1.7062$

$$R_G = \frac{5.0 \times 10^4 \times 1.7062}{1.7062 \times 1.7062} = 29.3\ k\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{2 \times 1.7062 - 1.7062 - 1} = 70.8k\Omega$$

The above obtained resistor values are for the complex pole pair of the first stage of the required active filter. The simple pole obtained as outlined below, using the uncommitted op amp in the UAF41 makes the second stage of the required filter.

For the simple pole f_n was obtained in the step 3.

$f_n = 1.596281$

The actual (denormalized) frequency = $f_c \times f_n$

$= 2\ kHz \times 1.596281 = 3192.6\ Hz$

$$\text{Now, } f = \frac{1}{2\pi RC}$$

$$\therefore RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 3192.6} = 4.9851 \times 10^{-5}$$

Choosing C = 2200 pF (or any convenient value),

$$R = \frac{4.9851 \times 10^{-5}}{2200 \times 10^{-12}} = 22.66\ k\Omega$$

Note:

R and/or C may be chosen in any convenient manner to obtain the desired RC product.

The overall circuit for the requried filter is shown below:

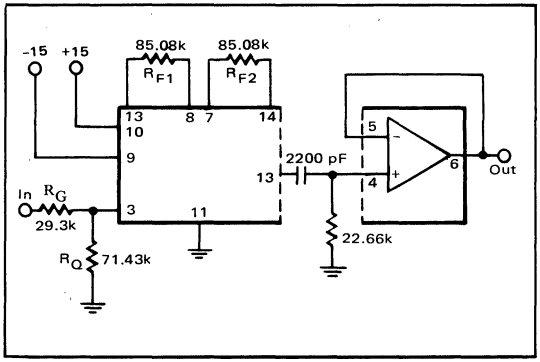


FIGURE 9. Overall Circuit - Example 1.

Example 2.

It is desired to design a 4 pole Butterworth, Band Pass Filter, with Q = 25, f_c = 19 kHz and A_{BP} = 1.

Using the computer program shown in Table III, the following values of f_n and Q are obtained.

$f_n = 1.0142435$, $Q = 35.36541$

and $f_n = 0.9859565$, $Q = 35.35886$

Using the above shown values of Q and f_n, we now will proceed to design the two stages of filter separately.

Any one of the three configurations shown in the CONFIGURATION SELECTION GUIDE can be used. We will select the noninverting input configuration.

For Stage 1

$f_o = 19\ kHz \times f_n = 19\ kHz \times 1.0142435$

$= 19270.6\ Hz$

Since $f_o > 8$ kHz, equations "B" would be used.

$$R_{F1} = R_{F2} = \frac{5.033 \times 10^7}{19270.6} = 2.6118\ k\Omega$$

$f_o Q = 19270.6 \times 35.36541 = 6.815136 \times 10^5$

Since $f_o Q > 10^5$, locate the corresponding $f_o Q_P$ from Figure 4.

Divide $f_o Q_P$ by f_o to obtain Q_P.

Thus $Q_P = 48.78$

$$R_G = \frac{5.0 \times 10^4 \times 35.36541}{1 \times 48.78} = 36.25k\Omega$$

$$R_Q = \frac{5.0 \times 10^4}{3.48 \times 48.78 - \frac{48.78}{35.37} - 1} = 298.7\Omega$$

For Stage 2.

Following the same procedure as shown for Stage 1 above, the values shown below are obtained.

$f_o Q = 6.624 \times 10^5$, Using Figure 4, $Q_P = 48.04$

$R_{F1} = R_{F2} = 2.6867\ k\Omega$

$R_G = 36.8\ k\Omega$

and $R_Q = 303.4\ \Omega$

The overall circuit for the required filter is shown below.

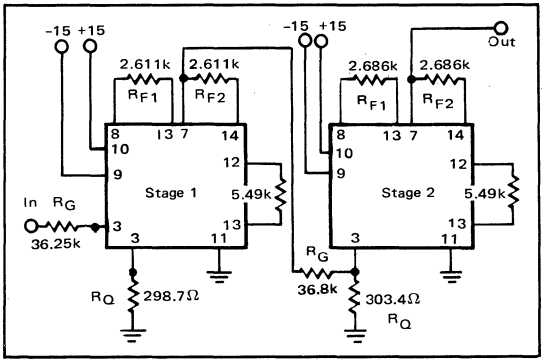


FIGURE 10. Overall Circuit - Example 2.

Example 3.

It is desired to design a 5 pole Bessel, Low Pass Filter with $f_c = 3.3$ kHz and $A_{LP} = 1$.

From Table I, the following values of f_o and Q are obtained.

Complex Poles:

$f_n = 1.55876$
$Q = 0.56354$
$f_n = 1.75812$
$Q = 0.91652$

Simple Pole:

$f_n = 1.50470$

Using the above shown values of f_n and Q, we now will proceed to design the three stages of filter separately.

Any one of the three configurations can be used. We will select inverting configuration.

For Stage 1.

$f_o = 3.3$ kHz x $f_n = 3.3$ kHz x $1.55876 = 5144$ Hz

Since $f_o < 8$ kHz, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5144} = 30.95\ k\Omega$$

$f_o Q = 5144 \times 0.56354 = 2.9 \times 10^3$

$f_o Q < 10^5$, $\therefore Q_P = Q = 0.56354$

$A_{BP} = Q_P A_{LP} = 0.56354 \times 1 = 0.56354$

$$R_G = \frac{5 \times 10^4 \times 0.56354}{0.56354} = 50\ k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.56354 + 0.56354 - 1} = 72.4\ k\Omega$$

For Stage 2.

$f_o = 3.3$ kHz x $f_n = 3.3$ kHz x $1.75812 = 5802$ Hz

Since $f_o < 8$ kHz, equations "A" would be used.

$$R_{F1} = R_{F2} = \frac{1.592 \times 10^8}{5802} = 27.44\ k\Omega$$

$f_o Q = 5802 \times 0.91652 = 5.32 \times 10^3$

$f_o Q < 10^5$, $\therefore Q_P = Q = 0.91652$

$A_{BP} = Q_P A_{LP} = 0.91652 \times 1 = 0.91652$

$$R_G = \frac{5 \times 10^4 \times 0.91652}{0.91652} = 50\ k\Omega$$

$$R_Q = \frac{5 \times 10^4}{2 \times 0.91652 + 0.91652 - 1} = 28.58\ k\Omega$$

For Stage 3.

$f = 3.3$ kHz x $f_n = 3.3$ kHz x $1.50470 = 4966$ Hz

For the simple pole,

$$RC = \frac{1}{2\pi f} = \frac{1}{2\pi \times 4966} = 3.2049 \times 10^{-5}$$

3300 pF (or any convenient value)

$$R = \frac{3.2049 \times 10^{-5}}{3300 \times 10^{-12}} = 9.71\ k\Omega$$

The overall circuit is shown below.

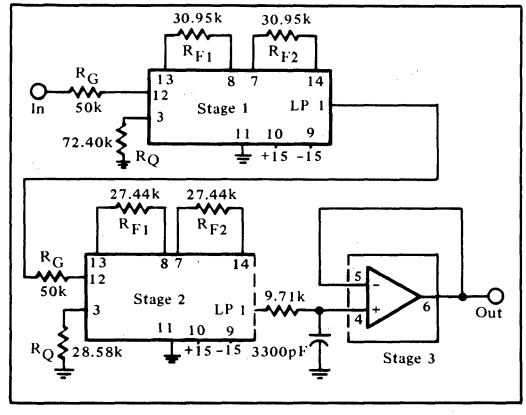
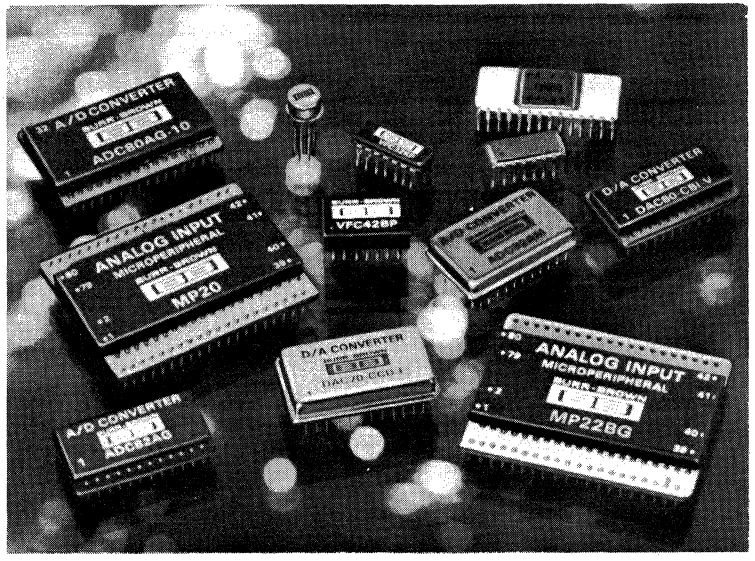


FIGURE 11. Overall Circuit - Example 3.

USEFUL REFERENCES

1. G.E. Tobey, J.G. Graeme and L.P. Huelsman, Operational Amplifiers: Design and Applications, (Chapter 8) McGraw Hill Book Co., 1971.
2. Yu Jen Wong, William E. Ott, Function Circuits: Design and Applications, (Chapter 6) McGraw Hill Book Co., 1976.
3. Richard W. Daniels, Approximation Methods for Electronic Filter Design, McGraw Hill Book Co., 1974.
4. Anatol I. Zverev, Handbook of Filter Synthesis, John Wiley and Sons Inc., New York, N.Y., 1967.
5. Gabor C. Temes, Sanjit K. Mitra, Modern Filter Theory and Design, John Wiley and Sons, New York, N.Y., 1973.

DATA CONVERSION AND ACQUISITION



6

The Burr-Brown data conversion and acquisition product line includes components necessary to multiplex and convert signals from analog-to-digital form and digital-to-analog form. These components are produced in four product types: digital-to-analog converters, analog-to-digital converters, sample/hold circuits, and multiplexers.

These products were designed to make their applications easy. Most units are complete, requiring no external components. All D/A converters include an internal reference and most have an output voltage amplifier. A/D converters come with internal clock, reference, and comparator. Many sample/hold circuits have an internal holding capacitor. The multiplexers contain input protection circuitry to prevent damage from input overvoltages.

If your system requires data acquisition and conversion, you will want to consider one of our predesigned System Data Modules (SDM). Each contains a multiplexer, instrumentation amplifier, sample/hold circuit, A/D converter, and timing and control logic. The microperipheral components are SDM's that have address decoding and specialized control logic making them compatible with most of the available microprocessors. These subsystems, tested at the factory, have a proven record of reliability.

True 16-bit accuracy performance will soon be available in the ADC73, an advanced design successive approximation A/D converter, guaranteed to have no more than ±0.00075% linearity error. Introduction is planned for 2nd quarter 1982.

Burr-Brown data acquisition components - quality and reliability at low cost.

SELECTION GUIDE
Data Conversion and Acquisition

Operating temperature range 0°C to 70°C, and parameters are typical unless otherwise noted.

ANALOG-TO-DIGITAL CONVERTERS

Description	Model(1)	Resolution (Bits)	Linearity, max (% of FSR)	Conversion Time, max (µsec)	Accy. Drift Bipolar, max (ppm FSR/°C)	Input Range (V)	Temp Range(2)	Package	Price $ Units	Price $ 100's	Page
Low Cost	ADC80AG-10(3)	10	±0.048	21	±23	±2.5, ±5, ±10, +5, +10	Ind	DIP	85.00	46.00	6-48
	ADC80AG-12(3)	12	±0.012	25	±23		Ind	DIP	87.00	48.00	6-48
Low Cost, High Speed	ADC82AG	8	±0.2	2.8	±75	±2.5, ±5, ±10 +5, +10, +20	Ind	DIP	69.00	48.00	6-56
	ADC82AM, (Q)	8	±0.2	2.8	±75		Ind	DIP	93.80	62.60	6-56
	ADC84KG-10	10	±0.048	6	±23	±2.5, ±5, ±10, +5, +10	Com	DIP	105.00	72.00	6-64
	ADC84KG-12	12	±0.012	10	±23		Com	DIP	119.00	75.00	6-64
Low Drift, High Speed	ADC85C-10	10	±0.048	6	±53		Com	DIP	119.00	99.00(7)	6-64
	ADC85-10	10	±0.048	6	±28		Ind	DIP	143.00	120.00(7)	6-64
	ADC85C-12, (Q)	12	±0.012	10	±30		Com	DIP	132.00	108.00(7)	6-64
	ADC85-12, (Q)	12	±0.012	10	±19		Ind	DIP	172.00	129.00(7)	6-64
High Resolution	ADC71JG	16	±0.006	50	±25	±2.5, ±5, ±10, 0 to +5, 0 to +10, 0 to +20	Com	Ceramic 32-pin DIP	168.00	122.00	6-24
	ADC71KG	16	±0.003	50	±25		Com		210.00	152.00	6-24
	ADC72AM	16	±0.006	50	±25		Ind	Metal Hermetic 32-pin DIP	269.00	194.00	6-32
	ADC72BM	16	±0.003	50	±25		Ind		295.00	213.00	6-32
	ADC72JM	16	±0.006	50	±30		Com		225.00	162.00	6-32
	ADC72KM	16	±0.003	50	±30		Com		265.00	191.00	6-32
	ADC76JG	16	±0.006	15	±30		Com	Ceramic 32-pin DIP	229.00	165.00	6-40
	ADC76KG	16	±0.003	15	±30		Com		265.00	191.00	6-40
Very-Wide Temp Range	ADC10HT	12	±0.012	50	±34	±5, ±10	-55°C to +200°C	Ceramic 28-pin DIP	485.00	395.00	6-8
	ADC10HT-1	12	±0.048	50	±63	±5, ±10			448.00	365.00	6-8
Very-High Speed	ADC60-08	8	±0.195	0.88	±20	±2.5, ±5	Com	Module	285.00	207.00	6-18
	ADC60-10	10	±0.0488	1.88	±20	±10, +5	Com	Module	316.00	228.00	6-18
	ADC60-12	12	±0.0244	3.50	±15	+10, +20	Com	Module	326.00	235.00	6-18
Military	ADC87/MIL Series	See Military Products									
High Resolution	ADC100-SMD	4 digit + sign	±0.005	30msec	±5	±10	Com	Module	376.00	285.00(7)	6-72

PCM ANALOG-TO-DIGITAL CONVERTERS FOR AUDIO

Description	Model	Resolution (Bits)	Total Harmonic Distortion (max)	Conversion Time (max)	Input Range (V)	Temp Range(2)	Dynamic Range	Price ($) Units	Price ($) 100's	Page
Audio Converter(4)	PCM75KG	16	0.02% at -15dB	17µsec(6)	±2.5, ±5, ±10	Com	90dB	249.00	189.00	6-298
	PCM75JG	14(5)	0.05% at -15dB	15µsec(6)	±2.5, ±5, ±10	Com	90dB	198.00	145.00	6-298

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. 2) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C. 3) "Z" models operate from ±12VDC supply. 4) Internal 16-bit DAC available to user. 5) Can be operated at 16-bits. 6) Can be reduced to 8µsec. 7) 25 - 99 quantity.

DIGITAL-TO-ANALOG CONVERTERS

Description	Model[1]	Resolution (Bits)	Linearity max (% of FSR)	Accy. Drift, Bipolar max (ppm of FSR/°C)	Output Ranges	Settling Time (FSR, ±1/2LSB)	Temp Range[2]	Package	Price ($) Units	Price ($) 100's	Page
Monolithic[3] 12-Bit	DAC800-CBI-I	12	±0.012	±25[5]	±1, -2mA	300nsec	Com	24-pin DIP	**23.95**	**15.95**	6-183
	DAC800-CBI-V	12	±0.012	±25	±2.5, ±5, ±10V +5, +10V	3μsec	Com		29.95	19.50	6-183
	DAC850-CBI-I	12	±0.012	±17[5]	±1, -2mA,	300nsec	Ind	Hermetic 24-pin DIP	**39.00**	**28.00**	6-190
	DAC850-CBI-V	12	±0.012	±17	±2.5, ±5, ±10, +5, +10V	3μsec	Ind		**47.00**	**34.00**	6-190
	DAC851-CBI-I	12	±0.012	±30[5]	±1, -2mA,	300nsec	Mil	Hermetic 24-pin DIP	105.00	69.00	6-190
	DAC851-CBI-V	12	±0.012	±30	±2.5, ±5, ±10, +5, +10V	3μsec	Mil		120.00	79.00	6-190
Low Cost	DAC80-CBI-I[4]	12	±0.012	±25[5]	±1.0, -2mA	300nsec	Com	DIP	**34.25**	**22.00**	6-152
	DAC80-CBI-V[4]	12	±0.012	±25	±2.5, ±5, ±10 +5, +10V	3μsec	Com	DIP	**36.50**	**22.95**	6-152
	DAC80-CCD-I[4]	3 digits	±0.025	±25[5]	0 to -2mA	300nsec	Com	DIP	34.50	22.00	6-152
	DAC80-CCD-V[4]	3 digits	±0.025	±25	0 to +10V	3μsec	Com	DIP	36.50	22.95	6-152
Low Drift	DAC85-CBI-I, (Q)	12	±0.012	±20[5]	±1.0, -2mA	300nsec	Ind	Metal Hermetic 24-pin DIP	104.00	84.50[6]	6-170
	DAC85-CBI-V, (Q)	12	±0.012	±20	±2.5, ±5, ±10 +5, +10V	3μsec	Ind		107.00	86.50[6]	6-170
	DAC85C-CBI-I, (Q)	12	±0.012	±30[5]	±1.0, -2mA	300nsec	Com		77.00	66.00[6]	6-170
	DAC85C-CBI-V, (Q)	12	±0.012	±30	±2.5, ±5, ±10 +5, +10V	3μsec	Com		79.00	68.00[6]	6-170
	DAC85LD-CBI-V	12	±0.012	±5	±2.5, ±5, ±10 +5, +10V	3μsec	Ind		142.75	129.50[6]	6-170
High Resolution	DAC70-CSB-I	16	±0.003	±9[5]	0 to -2mA	50μsec	Ind	Metal Hermetic 24-pin DIP	177.50	140.75[6]	6-101
	DAC70-COB-I, (Q)	16	±0.003	±9[5]	±1mA	50μsec	Ind		177.50	140.75[6]	6-101
	DAC70C-CSB-I	16	±0.005	±21[5]	0 to -2mA	50μsec	Com		**124.25**	**98.53[6]**	6-101
	DAC70C-COB-I	16	±0.005	±21[5]	±1mA	50μsec	Com		**124.25**	**98.53[6]**	6-101
	DAC70-CCD-I	4 digits	±0.003	±9[5]	0 to -2mA	50μsec	Ind		177.50	140.75[6]	6-101
	DAC70C-CCD-I	4 digits	±0.005	±21[5]	0 to -2mA	50μsec	Com		**124.25**	**98.53[6]**	6-101
	DAC71-CSB-I	16	±0.003	±15[5]	0 to -2mA	1μsec	Com	DIP	62.00	46.00	6-109
	DAC71-COB-I	16	±0.003	±15[5]	±1mA	1μsec	Com	DIP	62.00	46.00	6-109
	DAC71-CCD-I	4 digits	±0.005	±15[5]	0 to -2mA	1μsec	Com	DIP	62.00	46.00	6-109
	DAC71-CSB-V	16	±0.003	±15	0 to +10V	10μsec	Com	DIP	65.00	52.00	6-109
	DAC71-COB-V	16	±0.003	±15	±10V	10μsec	Com	DIP	65.00	52.00	6-109
	DAC71-CCD-V	4 digits	±0.005	±15	0 to +10V	10μsec	Com	DIP	65.00	52.00	6-109
	DAC72C-CSB-I	16	±0.003	±15[5]	0 to -2mA	1μsec	Com	Metal Hermetic 24-pin DIP	79.00	52.00	6-119
	DAC72C-COB-I	16	±0.003	±15[5]	±1mA	1μsec	Com		79.00	52.00	6-119
	DAC72C-CCD-I	4 digits	±0.005	±15[5]	0 to -2mA	1μsec	Com		79.00	52.00	6-119
	DAC72C-CSB-V	16	±0.003	±15	0 to +10V	10μsec	Com		87.00	58.00	6-119
	DAC72C-COB-V	16	±0.003	±15	±10V	10μsec	Com		87.00	58.00	6-119
	DAC72C-CCD-V	4 digits	±0.005	±15	0 to +10V	10μsec	Com		87.00	58.00	6-119
	DAC72-CSB-I	16	±0.003	±8[5]	0 to -2mA	1μsec	Ind	Metal Hermetic 24-pin DIP	89.00	60.00	6-119
	DAC72-COB-I	16	±0.003	±8[5]	±1mA	1μsec	Ind		89.00	60.00	6-119
	DAC72-CCD-I	4 digits	±0.005	±8[5]	0 to -2mA	1μsec	Ind		89.00	60.00	6-119
	DAC72-CSB-V	16	±0.003	±8	0 to +10V	10μsec	Ind		101.00	67.00	6-119
	DAC72-COB-V	16	±0.003	±8	±10V	10μsec	Ind		101.00	67.00	6-119
	DAC72-CCD-V	4 digits	±0.005	±8	0 to +10V	10μsec	Ind		101.00	67.00	6-119
High-Resolution Highly Accurate	DAC73J	16	±0.0015	±18	±2.5, ±5, ±10 +5V, +10V	50μsec	Com	Module	242.00	193.00	6-129
	DAC73K	16	±0.00075	±10.5		50μsec	Com	Module	286.00	228.00	6-129
	DAC736J	16	±0.0015	±18	0 to -2mA	50μsec	Com	Module	220.00	175.00	6-129
	DAC736K	16	±0.00075	±10.5	±1mA	50μsec	Com	Module	260.00	206.00	6-129
Very-Wide Temperature Range	DAC10HT	12	±0.012	±20	±2.5, ±5, ±10, +5, +10	200nsec	-55°C to +200°C	Ceramic 24-pin DIP	295.00	165.00	6-80
	DAC10HT-1	12	±0.048	±50		200nsec			273.00	150.00	6-80
Very-High Speed	DAC60-10	10	±0.048	±15[5]	0 to -5mA	40nsec	Com	Module	158.00	106.00	6-88
	DAC60-12	12	±0.012	±15[5]	±2.5mA	150nsec	Com	Module	172.00	114.00	6-88
Ultra-High Speed	DAC63BG	12	±0.012	±40	±5, -10mA	35nsec	Ind	Ceramic 24-pin DIP	108.00	83.00	6-93
	DAC63CG	12	±0.012	±30	±5, -10mA	35nsec	Ind		119.00	92.00	6-93

DIGITAL-TO-ANALOG CONVERTERS (continued)											
Description	Model(1)	Resolution (Bits)	Linearity max (% of FSR)	Accy. Drift, Bipolar max (ppm of FSR/°C)	Output Ranges	Settling Time FSR, ±1/2LSB	Temp Range(2)	Package	Price ($) Units	Price ($) 100's	Page
Military	DAC87/MIL Series	See Military Products									
Low Cost	DAC82KG	8	±0.16	±50	±2.5, ±5, ±10 +5, +10, ±0.8, 0 to -1.6mA	2.5µsec	Com	DIP	33.90	22.70	6-163
Monolithic 8-Bit	DAC90BG, (Q)	8	±0.2	±75(5)	±1, -2mA	200nsec	Ind	DIP	19.40	13.00	6-178
	DAC90SG, (Q)	8	±0.2	±75(5)	±1, -2mA	200nsec	Mil	DIP	26.50	17.70	6-178
PCM Audio Converter	PCM50KG	See PCM Digital-to-Analog Converters for Audio									

PCM DIGITAL-TO-ANALOG CONVERTERS FOR AUDIO										
Description	Model	Resolution (Bits)	Total Harmonic Distortion max	Settling Time	Output Range V	Temp Range(2)	Dynamic Range	Price ($) Units	Price ($) 100's	Page
PCM-Audio D/A Converter	PCM50KG	16	0.02% at -15dB	5µsec	±10, ±5	Com	96dB	75.00	49.75	6-281
	PCM51JG	16	0.04% at -15dB	5µsec	±10, ±5	Com	96dB	Contact factory		6-289

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. 2) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C. 3) In -V models the output op amp is on a second chip. 4) "Z" models operate from ±12VDC supply. 5) When used with an external op amp which uses the internal feedback resistor. 6) 25 - 99 quantity.

SELF-CALIBRATING DIGITAL-TO-ANALOG CONVERTER								
Description	Model	Resolution	Total Accuracy +15 to +45°C	Output Ranges	Calibration Time	Package	Price $ Units	Page
Precision, High-Resolution	DAC74	16-bits	±0.0015%, max	0 to +10V ±10V	2.5 sec	7" x 5" x 0.6" metal	$1495.00	6-137

POWER DACS									
Description	Model	Input Coding	Accuracy	Tempco (ppm FSR/°C)	Output Voltage (V)	Output Current (mA)	Package	Price ($) Units	Price ($) 25-99	Page
Low Cost, Open PC Card	4804	12-bit binary	±0.05% of reading	50, max	User-selected to ±30	±2000	PC card	259.00	182.00	6-381

V/F CONVERTERS										
Description	Model(1)	Frequency Range (kHz)	V_{IN} Range V	Linearity % of FSR max	Tempco ppm of FSR/°C max	Temp Range(2)	Package	Price $ Units	Price $ 100's	Page
Low Drift, Complete	VFC12	0 to 10	0 to +10	±0.01	50	Ind	Module	54.50	36.50	6-360
	VFC15	0 to 20	0 to +20	±0.01	50	Ind	Module	57.75	38.65	6-360
Very-Low Drift, Complete	VFC12LD	0 to 10	0 to +10	±0.005	10	Ind	Module	83.50	56.75	6-360
	VFC15LD	0 to 20	0 to +20	±0.005	10	Ind	Module	85.50	59.00	6-360
Low Cost, Monolithic	VFC32KP	User-selected,		±0.01 at 10kHz	±150	Com	DIP	10.15	6.15	6-367
	VFC32BM, (Q)	500kHz, max	User-selected	±0.05 at 100kHz	±150	Ind	TO-100	14.90	8.35	6-367
	VFC32SM, (Q)			±0.2 at 500kHz	±150	Mil	TO-100	19.70	11.85	6-367
Military	VFC32/MIL Series	See Military Products								
Low Cost, Complete, Hybrid	VFC42BP	0 to 10	0 to +10	±0.01	±100	Ind	DIP	19.75	14.50	6-375
	VFC42SM	0 to 10	0 to +10	±0.01	±100	Mil	DIP	33.40	22.75	6-375
	VFC52BP	0 to 100	0 to +10	±0.05	±150	Ind	DIP	19.75	14.50	6-375
	VFC52SM	0 to 100	0 to +10	±0.05	±150	Mil	DIP	33.40	22.75	6-375

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. 2) Com = 0 to +70°C; Ind = -25°C to +85°C; Mil = -55°C to +125°C.

DATA ACQUISITON SYSTEMS

Description	Model	Channels	Resolution Bits	Throughput Accuracy % of FSR	Throughput Rate kHz	Package	Price $ Units	Price $ 100's	Page
Modular	SDM853	16 single-ended 8 differential	12	±0.025	30(1)	Module	365.00	256.00 (3)	6-308
Low Level	SDM858	16 single-ended 8 differential	12	±0.025(2)	8(1)	Module	369.00	265.00 (3)	6-336
Hybrid ±10V Input	SDM854AG SDM854BG	16 single-ended 8 differential	12 12	±0.048 ±0.024	40 29	QIP QIP	220.00 246.00	165.00 185.00	6-314 6-314
Hybrid	SDM856JG SDM856KG	16 single-ended 8 differential	12 12	±0.048 ±0.024	33 25	QIP QIP	174.00 219.00	125.00 158.00	6-330 6-330
Hybrid Low Level	SDM857JG SDM857KG	16 single-ended 8 differential	12 12	±0.048 ±0.024	25 18	QIP QIP	194.00 242.00	130.00 162.00	6-330 6-330

NOTES: 1) Can be increased if short-cycled to 8- or 10-bit resolution. 2) At gain = 100. 3) 50 - 99.

MICROPROCESSOR INTERFACED ANALOG INPUT SYSTEMS

Description	Model	Channels	Resolution	Accuracy % of FSR max	Tempco ppm/°C max	Package	Price $ Units	Price $ 100's	Page
8080- SC/MP-Compatible	MP20	8 differential 16 single-ended	8 bits	±0.8, high ±0.4, low	±40	QIP	280.00	222.00(2)	6-205
6800-, 6502-Compatible	MP21	8 differential 16 single-ended	8 bits	±0.8, high ±0.4, low	±40	QIP	280.00	222.00(2)	6-217
Universal	MP22BG	8 differential 16 single-ended	12 bits	±0.4, high ±0.1, low	±25(1)	QIP	324.00	241.00(2)	6-229
High-Accuracy	MP32BG MP32CG	8 differential 16 single-ended	12 bits 12 bits	±0.05 ±0.025	±60 ±60	QIP QIP	339.00 429.00	267.00 286.00	6-237

MICROPROCESSOR INTERFACED ANALOG OUTPUT SYSTEMS

Description	Model	Channels	Resolution	Accuracy % of FSR max	Tempco ppm/°C max	Package	Price $ Units	Price $ 100's	Page
8080-, SC/MP-Compatible	MP10	2	8 bits	±0.4	±80	DIP	141.00	94.00	6-197
6800-, 6502-Compatible	MP11	2	8 bits	±0.4	±80	DIP	141.00	94.00	6-197

NOTES: 1) Unipolar, excluding IA. 2) 25 - 99 quantity.

MULTIPLEXERS

Description	Model	Channels	Input Range (V)	On Resistance max	Crosstalk % of OFF Channel Signal	Settling Time to 0.01%	Package	Price $ Units	Price $ 100's	Page
Protected Inputs	MPC8S	8 single	±15	1.8kΩ	0.005	5μsec	DIP	12.97	9.50	6-267
	MPC4D	4 differential	±15	1.8kΩ	0.005	5μsec	DIP	12.97	9.50	6-267
	MPC16S	16 single	±15	1.8kΩ	0.005	7μsec	DIP	23.21	17.00	6-274
	MPC8D	8 differential	±15	1.8kΩ	0.005	7μsec	DIP	23.21	17.00	6-274
High Speed	MPC800KG	16 single or	±15	750Ω	0.004	800nsec	DIP	30.71	22.50	6-253
	MPC800SG	8 differential	±15	750Ω	0.004	800nsec	DIP	61.43	45.00	6-253
	MPC801KG	8 single or	±15	750Ω	0.004	800nsec	DIP	16.00	11.72	6-260
	MPC801SG	4 differential	±15	750Ω	0.004	800nsec	DIP	33.12	24.26	6-260

SAMPLE/HOLD CIRCUITS

Description	Model(1)	Gain/Offset Error (%) (mV)	Charge Offset (mV)	Droop Rate (mV/msec	Tempco ppm of 20V/°C	Acquisition Time μsec (2)	Package	Price $ Units	Price $ 100's	Page
Low Cost, Complete	SHC80KP	±0.01, ±2 max	±2 max	0.5 max	3	10 max	DIP	51.00	34.10	6-342
High Speed, Complete	SHC85, (Q)	±0.01, ±2 max	±2 max	0.5 max	3	4.5 max	DIP(3)	95.00	75.90(5)	6-346
	SHC85ET, (Q)	±0.01, ±2 max	±2 max	0.5 max	3	4.5 max	DIP(3)	129.00	106.00(5)	6-346
Low Cost, Monolithic	SHC298AM	±0.01, ±7 max	±25 max	10 max(4)	4	10 max	TO-99(3)	6.95	4.50	6-350
Very-High Speed	SHM60	±0.01, ±1.5	±1.5	5	2	1 max	Module	154.00	104.00	6-356

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. 2) 10V step to 0.01% of final value. 3) Hermetic. 4) With 1000pF external holding capacitor. 5) 25 - 99 quantity.

GLOSSARY OF TERMS & DEFINITIONS
Data Conversion and Acquisition

ACQUISITION TIME

The time the output of a sample/hold circuit takes to change from its previous value to a new value when the circuit is switched from the hold mode to sample mode. It includes the slew time and settling time to within a certain error band of the final value and is usually specified for a full-scale change.

APERTURE TIME

When a sample/hold circuit is switched from sample to hold, a finite amount of time is required for the internal electronics to turn off. Aperture time is the time between the sample-to-hold command transition and the point at which the output ceases to follow the input.

APERTURE TIME UNCERTAINTY

The possible deviation in aperture time from one sample-to-hold transition to the next.

COMPLIANCE VOLTAGE

Some D/A converters have an output current proportional to the input digital code. The compliance voltage is that voltage which may be impressed on the output current pin without degrading the specified accuracy of the converter.

CONVERSION SPEED

The measure of how long it takes an A/D converter to arrive at the proper output code. It is the time between the edge of the convert command pulse that starts conversion and the rising edge of the end-of-convert signal that indicates the conversion is complete.

CHARGE OFFSET

During the sample-to-hold transition of a sample/hold circuit, a small amount of charge is transferred to the holding capacitor because of the switching process. This is known as the charge offset and is usually expressed in millivolts.

CROSSTALK

The measure of effect an off-channel signal has on the on-channel signal in a multiplexer, expressed in terms of dB of attenuation of the off-channel signal.

DIFFERENTIAL LINEARITY

The measure of the linearity from one digital state to the next. It applies to A/D and D/A converters. If the differential linearity is specified as +1/2LSB, the step size from one state to the next may be from 1/2 to 3/2 of an ideal 1LSB step.

DROOP RATE

A sample/hold circuit in the hold mode has a charge stored on a capacitor that is proportional to the input voltage at the time it was switched to the hold mode. Charge leaks off the capacitor because of the bias current of the buffer amplifier and switch leakage current. The droop rate is an expression of how fast the charge leaks off the capacitor and is given as a voltage per-unit-of-time.

FEEDTHROUGH

The measure of the change of the output voltage of a sample/hold in the hold mode due to a voltage change in the input, expressed as dB of attenuation.

GAIN ERROR

The error in the input-to-output ratio, usually expressed in percent. It is manifest as a rotation about the most negative full scale point of the transfer function curve. It is nulled in A/D, D/A, or V/F converters after the offset error is nulled by setting the input for a full-scale output and adjusting an external trim pot for the correct output.

LEAKAGE CURRENT

Multiplexer input current that does not flow through to the output but is shunted internally. It is also current that flows from OFF channels into the ON channel. In a current output D/A converter, there is a digital input code that ideally yields zero output current. If current flows with that input code, it is called leakage current. It is analogous to output voltage offset in a voltage-output D/A converter.

LEAST SIGNIFICANT BIT (LSB)

The lowest-order bit or the bit with the least weight.

LINEARITY

The maximum deviation of an actual output from an ideal output defined by a straight-line drawn through the end points of the transfer function. This is the error that remains after offset and gain errors have been nulled. It applies to A/D, D/A, and V/F converters. Linearity can be expressed in terms of percent of full scale range or fractions of a least significant bit (LSB). A converter must be linear to within ±1/2LSB to be accurate to its full resolution.

MONOTONICITY

In a D/A converter, if the output analog signal either increases or stays the same for an increase in input digital code, it is said to be monotonic. In an A/D converter, if

the output digital code increases or stays the same for a 1LSB increase in input voltage, it is said to be monotonic. If the differential linearity is within ±1LSB, the device will be monotonic. Monotonicity is especially important in control loops where convergence is necessary.

MOST SIGNIFICANT BIT (MSB)

The highest-order bit or the bit with the greatest weight.

NO MISSING CODES

This is a property of an A/D converter that is related to, but is more stringent than, monotonicity. If a converter is guaranteed to have no missing codes, there will be no output digital state that will be skipped when the input voltage is varied over the entire range.

OFFSET ERROR

This is an error in the reference point of the transfer function. It appears as a constant amplitude error signal at a D/A output or A/D input. It also appears as a constant frequency shift in the output of a V/F converter. It is nulled prior to adjusting gain error by setting the input to the most-negative input and adjusting the output to the proper value.

POWER SUPPLY REJECTION RATIO

The measure of output signal change due to power supply voltage change. It is expressed as dB of attenuation or % output change per % supply change.

QUANTIZING ERROR

In an A/D converter, there is an infinite number of possible input voltages, but only 2^n output codes (n = number of bits). Therefore, there will be an error as great as 1/2LSB because of this quantizing effect and the greatest error will occur at the transition voltage where the output changes state.

RESOLUTION

The number of bits on the input or output of an A/D or D/A converter. The number of discrete steps or states is equal to 2^n where n is the resolution of the converter, however, n bits of resolution does not guarantee n bits of accuracy.

SETTLING TIME

The time delay between a change of input signal value and the effected change in the output signal. It is usually expressed in terms of how long it takes the output to arrive at, and remain within, a certain error band around the final value and is often given for several different magnitudes of input step change.

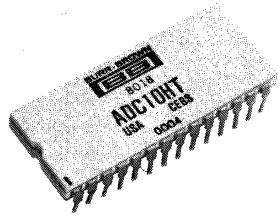
SWITCHING TIME

The time it takes for a multiplexer to change from one channel to the next with the new output signal being within a certain percentage of its final value. It is expressed for a maximum voltage transition.

THROUGHPUT RATE

An A/D converter or a data acquisition system has a finite number of points that it can convert in any given time. Throughput rate is an expression of that quantity. It is dependent on the time it takes to make a conversion and the time required to set up to make the next conversion. In a data acquisition system this time includes the composite delay due to switching and settling times of the mux, settling time of the amplifier and acquisition time of the sample-and-hold.

BURR-BROWN®



ADC10HT

Wide Temperature Range General Purpose 12-Bit ANALOG-TO-DIGITAL CONVERTER

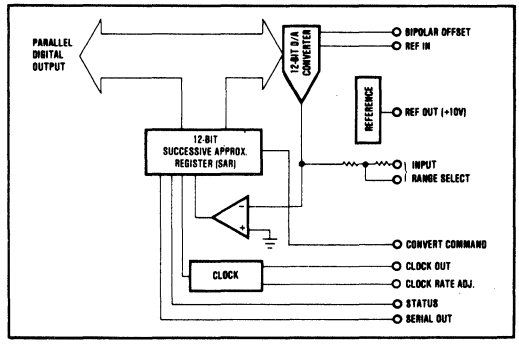
FEATURES

- -55°C to +200°C SPECIFICATIONS
- FULL 12-BIT RESOLUTION
- 50μsec MAX CONVERSION TIME
- NO MISSING CODES OVER FULL TEMPERATURE RANGE
- COMPLETE WITH INTERNAL CLOCK AND REFERENCE VOLTAGE
- SERIAL OUTPUT DATA AVAILABLE
- TTL AND +5V CMOS COMPATIBLE
- DUAL-WIDTH HERMETIC CERAMIC PACKAGE
- LOW POWER OPERATION WITH EXTERNAL REFERENCE (250mW)

DESCRIPTION

You'll find this general purpose, 12-bit, successive approximation A/D converter ideally qualified for circuits that must operate over wide temperature ranges. The ADC10HT incorporates state-of-the-art IC and laser-trimmed thin-film components. It is complete with an internal clock and reference voltage. Internal scaling resistors allow bipolar input voltage ranges of ±5V and ±10V. A pin is provided for serial output data. The ADC10HT is contained in a compact, dual width, 28-pin ceramic DIL package.

To assure consistent performance, 100% screening procedures are conducted on the ADC10HT at key points during its manufacture. Burn-in and temperature cycling are examples. A clean-room environment is maintained for assembly operations.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at rated power supply voltages and T_A = +25°C unless otherwise noted.

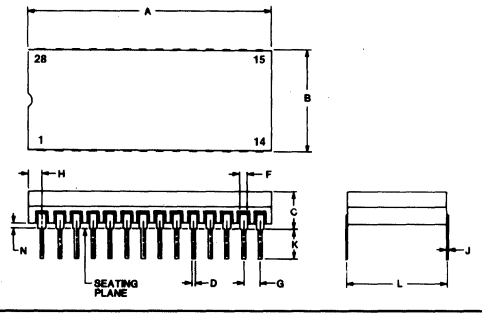
MODEL	ADC10HT			ADC10HT-1			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION	12			12			Bits
INPUT							
ANALOG							
Voltage Ranges							
Unipolar		0 to +10, 0 to +20			0 to +10, 0 to +20		V
Bipolar		±5, ±10			±5, ±10,		V
Impedance (direct input)							
0 to +10V, ±5V		2			2		kΩ
0 to +20V, ±10V		4			4		kΩ
DIGITAL(1)							
Convert Command Logic Loading		1			1		CMOS Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(2)		±0.05	±0.2		±0.05	±0.2	%
Offset Error(2)							
Unipolar		±0.05	±0.2		±0.05	±0.2	% of FSR(3)
Bipolar		±0.05	±0.2		±0.05	±0.2	% of FSR
Linearity Error			±0.012			±0.048	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error			±0.012			±0.048	% of FSR
Total Unadjusted Error(4)							
+25°C		±0.10	±0.40		±0.15	±0.40	% of FSR
-55°C to +200°C		±0.30	±1.00		±0.80	±1.50	% of FSR
Total Adjusted Error(5)							
+25°C		±0.006	±0.012		±0.024	±0.048	% of FSR
-55°C to +200°C		±0.20	±0.60		±0.50	±1.10	% of FSR
Total Unadjusted Error(6)							
Exclusive of Reference							
+25°C		±0.10	±0.40		±0.15	±0.45	% of FSR
-55°C to +200°C		±0.20	±0.80		±0.50	±1.10	% of FSR
Total Adjusted Error(7)							
Exclusive of Reference							
+25°C		±0.006	±0.012		±0.024	±0.048	% of FSR
-55°C to +200°C		±0.15	±0.40		±0.40	±0.75	% of FSR
CONVERSION TIME		30	50		30	50	µsec
DRIFT (-55°C ≤ T_A ≤ +200°C)							
Gain							
With Internal Reference		±15	±35		±25	±100	ppm/°C
Exclusive of Reference		±5	±10		±10	±20	ppm/°C
Offset							
Unipolar		±1	±2		±2	±10	ppm of FSR/°C
Bipolar							
With Internal Reference		±10	±35		±25	±100	ppm of FSR/°C
Exclusive of Reference		±4	±10		±8	±20	ppm of FSR/°C
Linearity		±0.5	±1		±1	±3	ppm of FSR/°C
No Missing Codes (Temp. Range							
-55°C to +200°C)	12			10			Bits
OUTPUT							
DIGITAL DATA							
Parallel							
Output Codes(8)							
Unipolar		SB			SB		
Bipolar(9)		OB, TC			OB, TC		
Output Drive	1			1			LSTTL Loads
Serial Data Code (NRZ) - SB, OB		SB, OB			SB, OB		
Output Drive	1			1			LSTTL Loads
Status	Logic "1" During Conversion			Logic "1" During Conversion			
Status Output Drive	1			1			LSTTL Loads
Internal Clock							
Output Drive	1			1			LSTTL Loads
Frequency		400			400		kHz

SPECIFICATIONS

MODEL	ADC10HT			ADC10HT-1			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLIES AND REFERENCE							
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain, +15VDC(10)		+15			+15		mA
-15VDC(10)		-30			-30		mA
+5VDC		+16			+16		mA
Power Supply Sensitivity							
±15VDC		0.01			0.01		% of FSR/%V_S
+5VDC		0.01			0.01		% of FSR/%V_S
Internal Reference Voltage	9.990	10.0	10.010	9.990	10.0	10.010	V
Max External Current with							
no Degradation of Specs		2			2		mA
Temperature Coefficient		±10			±10		ppm/°C
TEMPERATURE RANGE							
Specification	-55		+200	-55		+200	°C
Operating	-55		+200	-55		+200	°C
Storage	-65		+210	-65		+210	°C

NOTES:
1. +5V CMOS compatible. Input current (low to high state) = 1μA max. Use pull-up resistor when driving convert command from TTL.
2. Adjustable to zero (see Table II and Figures 5 and 6).
3. FSR means Full Scale Range. For example, unit connected for ±10V has a 20V FSR.
4. Includes Gain, Offset, and Linearity Errors (Bipolar Mode).
5. Gain and Offset Errors removed at +25°C (Bipolar Mode).
6. Includes Gain, Offset, and Linearity Errors with external +10.0V ±1mV reference, does not include Reference Drift Bipolar Mode.
7. Gain and Offset Errors removed at +25°C with external +10.0V ±1mV reference, does not include Reference Drift (Bipolar Mode.
8. See Table I. SB - Straight Binary, OB - Offset Binary, TC - Two's Complement.
9. TC coding obtained by using $\overline{MSB}$ (pin 13) instead of MSB (pin 12).
10. May be reduced. See Low Power Operation, pages 6-16 and 6-17.

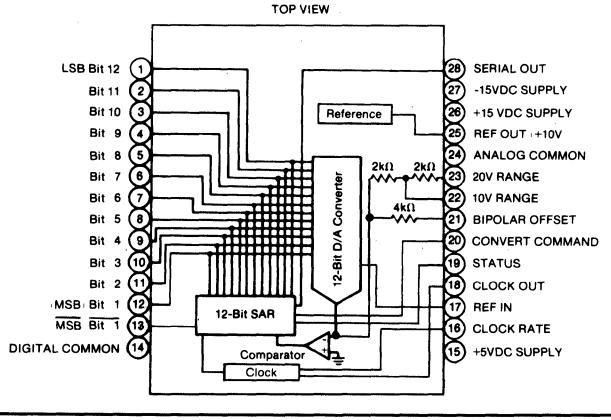
MECHANICAL



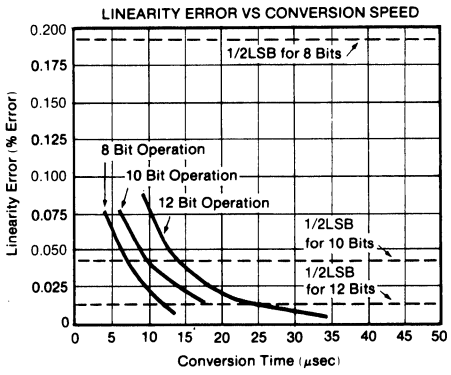
NOTES:
1. Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
2. Pin numbers shown for reference only. Numbers may not be marked on package.

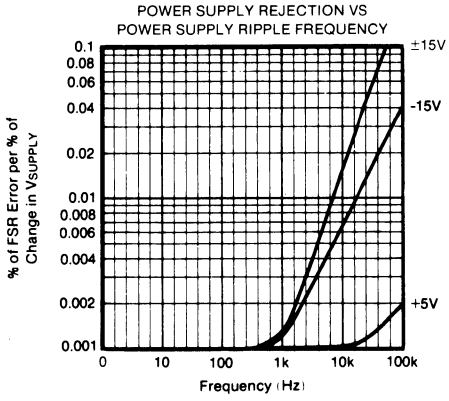
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	.610 BASIC		15.49 BASIC	
C	.160	.205	4.06	5.21
D	.015	.019	.38	.48
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.055	.095	1.40	2.41
J	.009	.012	.23	.30
K	.155	.195	3.94	4.95
L	.600 BASIC		15.24 BASIC	
N	.020	.030	.51	.76

CONNECTION DIAGRAM



TYPICAL PERFORMANCE CURVES





DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over range of the A/D converter is 1LSB, ±1/2LSB.

The ADC10HT is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also specifies that this converter will have no missing codes over the full operating temperature range.

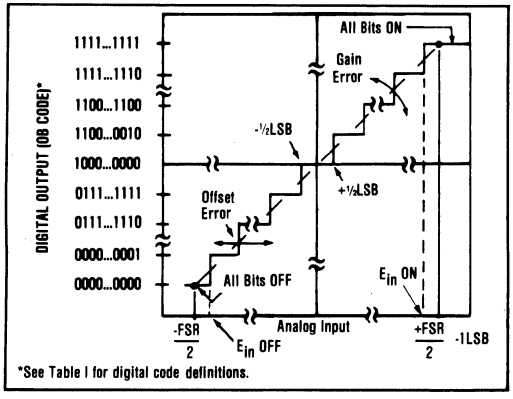


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 0110 0111 0110 exists.

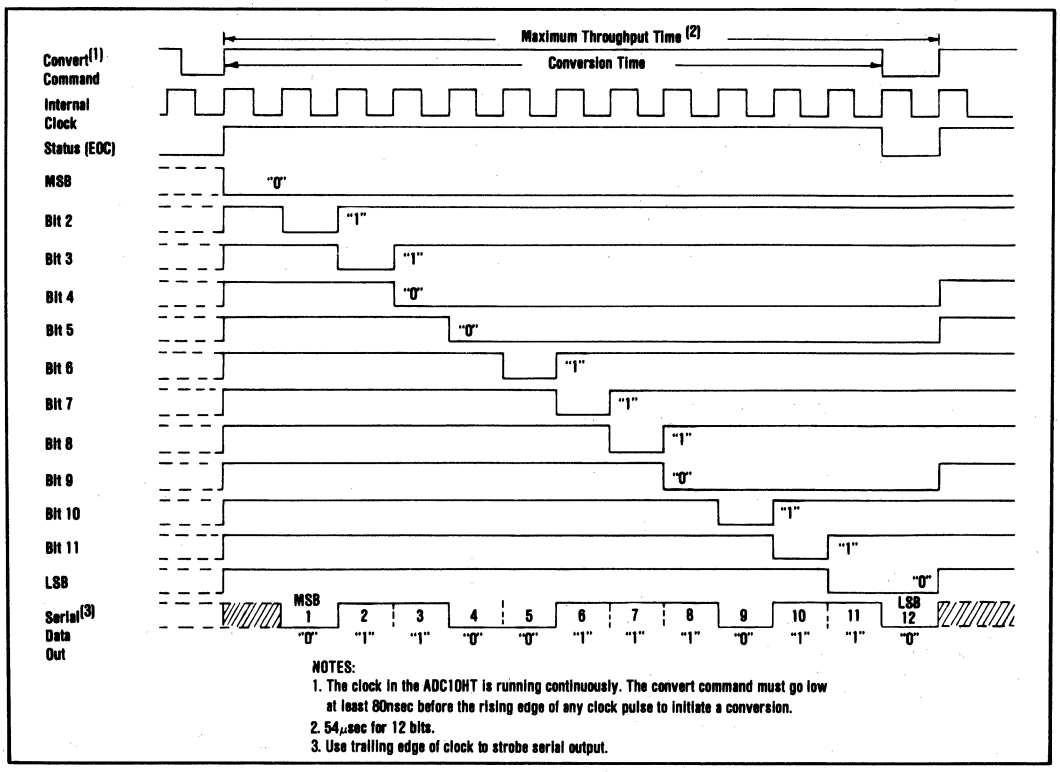


FIGURE 2. ADC10HT Timing Diagram.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC10HT parallel output; they are straight binary (SB) for unipolar input signal ranges and offset binary (OB) for bipolar input signal ranges. Two's complement (TC) may be obtained by using $\overline{\text{MSB}}$ (pin 13).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 8-, 10- and 12-bit resolutions. Figure 3 shows the connections for 12-bit resolution, parallel data output, with ±10V input.

SERIAL DATA

Two straight binary codes are available on the serial output line; they are SB and OB. The serial data is available only during conversion and appears with the MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the TC code.

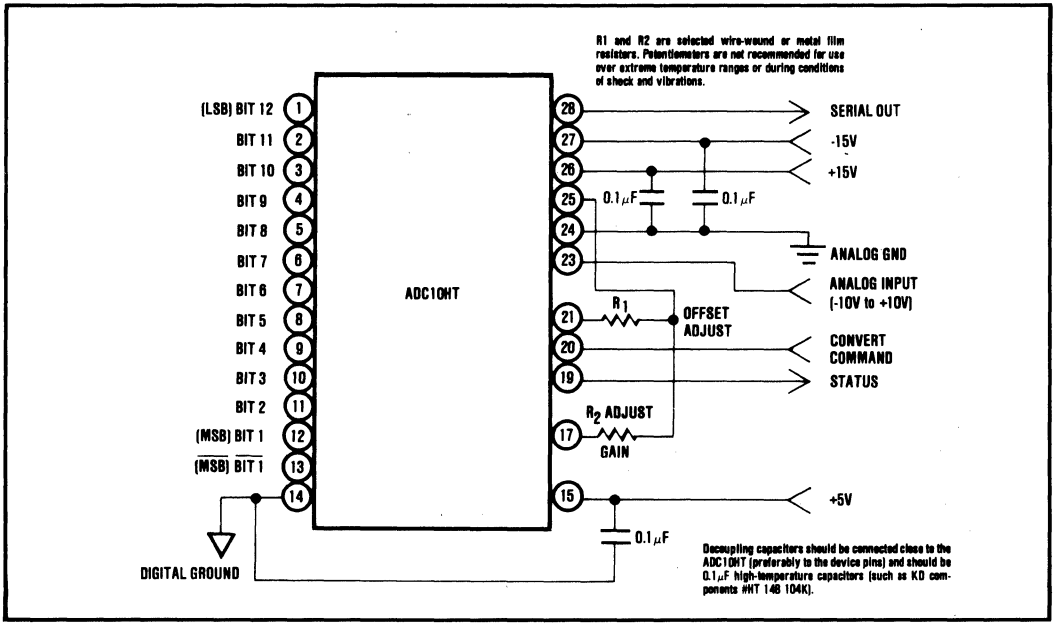


FIGURE 3. ADC10HT Connections for ±10V Analog Input, 12-Bit Resolution, and Serial or Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined As:	±10V	±5V	0 to +10V	0 to +20V
Code Designation		OB(1) or TC(2)	OB(1) or TC(2)	SB(3)	SB(3)
One Least Significant Bit (LSB)	$FSR/2^n$	$20V/2^n$	$10V/2^n$	$10V/2^n$	$20V/2^n$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 10	19.53mV	9.77mV	9.77mV	19.53mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Transition Values					
MSB LSB					
111...111(4)	+Full Scale	+10V - 3/2LSB	+5V - 3/2LSB	+10V - 3/2LSB	+20V - 3/2LSB
100...000	Mid Scale	0	0	+5V	+10V
000...001	-Full Scale	-10V + 1/2LSB	-5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

NOTES:
(1)OB = Offset Binary
(2)TC = Two's Complement - obtained by inverting the most significant bit. $\overline{MSB}$ (pin 13)
(3)SB = Straight Binary
(4)Voltages given are the nominal value for transition to the code specified

DISCUSSION OF SPECIFICATIONS

The ADC10HT is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion-speed effects on accuracy. This ADC is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.05% of FSR at 25°C. These errors may be trimmed to zero as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC10HT power supply sensitivity is specified for ±0.01% of FSR / $\%V_S$ for ±15V supplies and ±0.01% of FSR / $\%V_S$ for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC10HT but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with high temperature mica or teflon capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC.

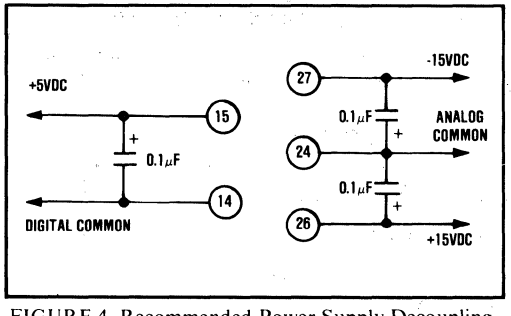


FIGURE 4. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

TABLE II. ADC10HT Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 21 To Pin	Connect Pin 23 To	Connect Input Signal To Pin
±10V	OB or TC*	25**	Input Sig.	23
±5V	OB or TC*	25**	Open	22
0 to +10V	SB	Open	Open	22
0 to +20V	SB	Open	Input Sig.	23

*Obtained by using $\overline{MSB}$ (pin 13)

** If optional offset adjustment is not used connect a 25Ω ±0.1% resistor from pin 21 to pin 25 to obtain specified gain and offset errors.

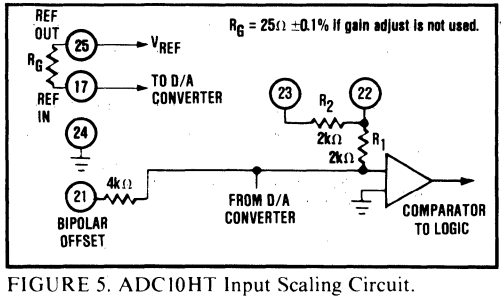


FIGURE 5. ADC10HT Input Scaling Circuit.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

A connection diagram for the ADC10HT in the ±10V input bipolar mode of operation is shown in Figure 3. The gain and offset adjustment resistors (R1 and R2) should be selected discrete metal-film or wirewound resistors and not potentiometers if optimum performance is required under high shock and vibration levels. The internal gain and offset errors are laser trimmed to within a maximum error of ±0.2% with 25Ω, 0.1% resistors in place of R1 and R2. Another possible approach in many applications is to simply remove the offset and gain errors with digital techniques after the A/D conversion has taken place. This approach can virtually eliminate the need for initial gain and offset adjustment and even the effects of gain and offset drift with time and temperature can often be removed. In some cases it may be desirable to use potentiometers.

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer or resistance substitution boxes as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits off E_{IN}^{OFF}.

Adjust the Offset potentiometer or resistor substitution boxes until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

GAIN - Connect the Gain adjust potentiometer or resistor substitution boxes as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

It is also possible to make the adjustments just described with potentiometers and then replace the resistive arms with discrete metal film or wire-wound resistors in order to make a system more rugged before subjecting it to harsh environments.

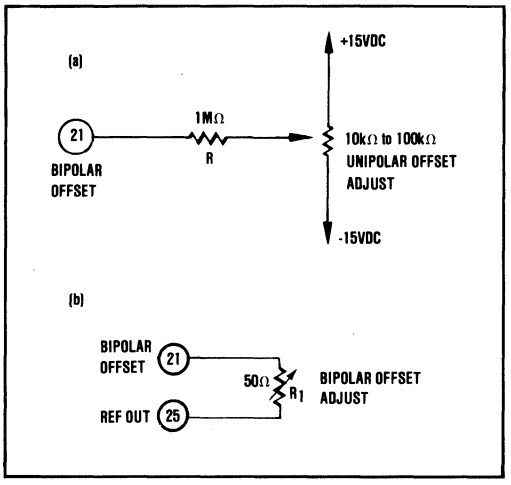


FIGURE 6. Optional Unipolar and Bipolar Offset Adjust Circuitry with ±0.4% of FSR Range of Adjustment.

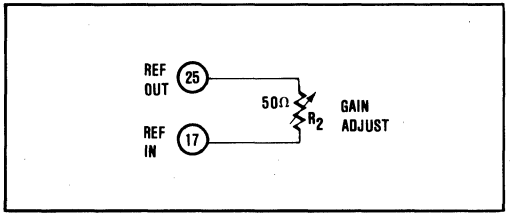


FIGURE 7. Optional Gain Adjust with ±0.4% Range of Adjustment.

CLOCK RATE CONTROL (OPTIONAL)

Faster Conversion

If adjustment of the clock rate is desired for faster conversion times, a resistor may be connected between Clock Rate (pin 16) and Clock Out (pin 18) as shown in Figure 8.

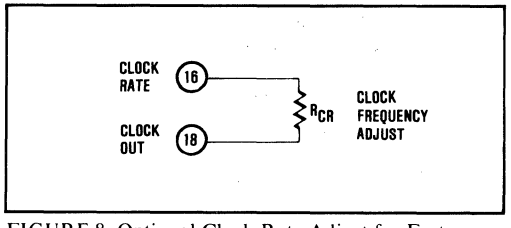


FIGURE 8. Optional Clock Rate Adjust for Faster Conversion Times.

Figure 9 shows the effect of clock rate control resistor (R_{CR}) on clock frequency. Figure 9 is based on a typical initial clock frequency of about 400kHz (conversion time of 30μsec for 12 bits). To determine the required clock frequency:

$$f_{clock} = \frac{\text{Bit Resolution}}{\text{Conversion Time}}$$

For example, if the ADC10HT is short cycled to 10-bit operation and a conversion time of 20μsec is required, then

$$f_{clock} = \frac{10}{20\mu\text{sec}} = 500\text{kHz}$$

from Figure 9 a clock rate resistor (R_{CR}) of about 40kΩ is required.

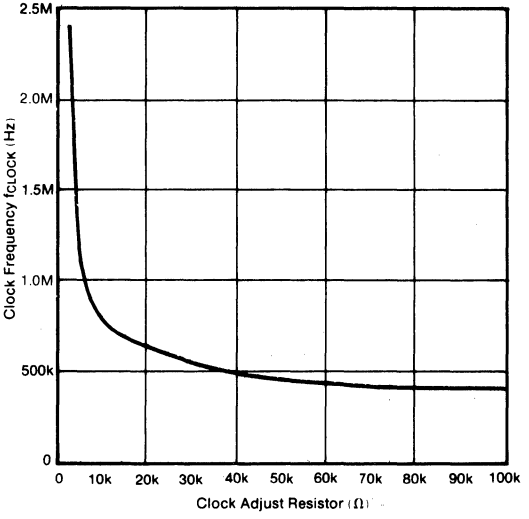


FIGURE 9. Clock Frequency vs Clock Rate Control Resistor (R_{CR}).

Slower Conversion

The conversion time can be decreased by connecting a capacitor from the Clock Rate pin to Digital Common (see Figure 10).

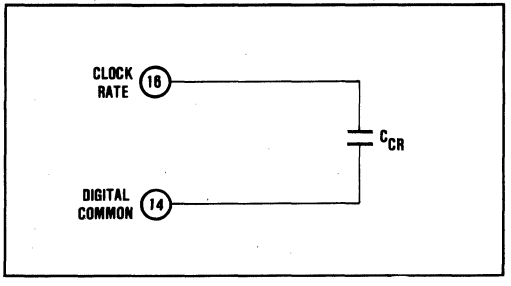


FIGURE 10. Optional Clock Rate Adjust for Slower Conversion Times.

Figure 11 shows the effect of the clock rate control capacitor on the clock frequency.

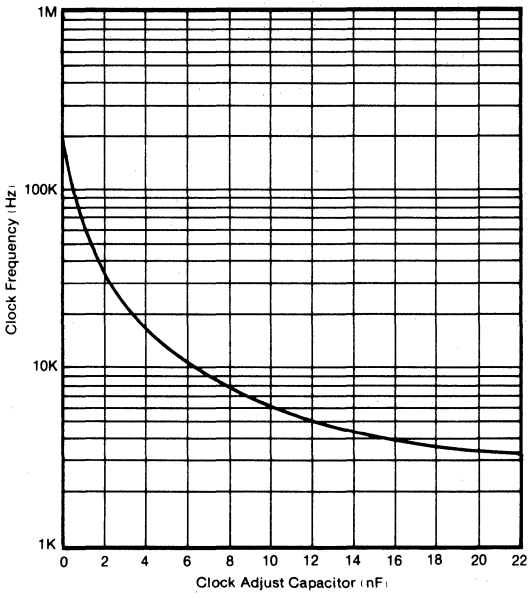


FIGURE 11. Clock Frequency vs. Clock Rate Control Capacitor (C_{CR}).

The serial output data (pin 28) is synchronous with the internal clock. In some applications the clock frequency must be lowered to 3kHz or 4kHz so that the data can be transmitted over long distances. If 12-bit resolution is required, the conversion time for 4kHz is

$$\text{conversion time} = \frac{12 \text{ bits}}{4\text{kHz}} = 3\text{msec}$$

From Figure 11, a clock rate control capacitor, C_{CR}, of approximately 16nF is required.

In applications requiring such a slow conversion time, a low-pass filter should be used at the analog input to the ADC10HT.

SHORT-CYCLE AND CONTINUOUS CONVERSION OPERATION.

The ADC10HT may be operated at faster speeds for resolutions less than 12 bits by using the clock rate control feature. The conversion time can be further increased by using the short cycle circuit shown in Figure 12. Without this circuit, the status signal (pin 19) will always remain high for 13 clock pulses even if only 8 bits are being used. By connecting the short cycle input of the NAND gate to the n + 1 bit (connect to bit 9 for 8-bit operation, for example) the conversion will be completed and the status signal will go low after n + 1 clock pulses (9 pulses for 8-bit operation). It should be noted that with the circuit shown in Figure 12, the ADC10HT will operate in a continuous conversion mode, i.e., a new conversion will start on the n + 2 clock pulse without the need for an external convert command.

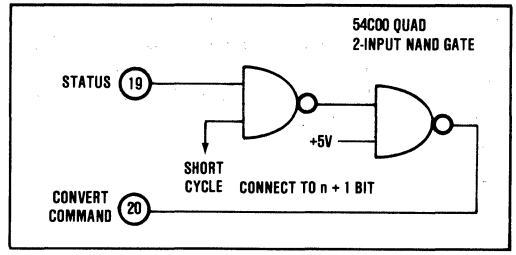


FIGURE 12. Short-Cycle Circuit which Provides for Lower Resolutions than 12 Bits with Faster Conversion Times and Continuous Conversions.

Table III indicates where to connect the short cycle input for 8-bit and 10-bit resolution and gives possible conversion time(s) obtainable by using this feature along with the clock rate pin.

TABLE III. Short Cycle Connections and Specifications for 8 to 12 Bit Resolutions.

Resolution (Bits)		12	10	8
Connect SHORT CYCLE to:		N/A	Pin 2	Pin 4
Conversion Time (μsec)(1)		24	10	6
Nonlinearity at +25°C (% of FSR)	ADC10HT	±0.012	±0.048	±0.1
	ADC10HT-1	±0.048	±0.048	±0.1

NOTE: (1) Adjust Conversion Time with Clock Rate Control resistor as shown in Figures 8 and 9.

For 12-bit operation and continuous conversion, simply connect status (pin 19) directly to convert command (pin 20).

OUTPUT DRIVE

Normally the ADC10HT logic outputs will drive two low power TTL loads or one LSTTL load. If long digital lines must be driven, external logic buffers are recommended. The digital outputs are connected directly to the internal CMOS successive-approximation-register and can drive +5V CMOS without the need for pull-up resistors.

HEAT DISSIPATION

The ADC10HT dissipastes approximately 750mW and the package has a case-to-case ambient thermal resistance (θ_{CA}) of 35°C/W. For optimum performance at +200°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the package can be achieved by using a silicone heat-sink compound.

LOW POWER OPERATION

The typical supply currents required by the ADC10HT under normal operating conditions are 15mA (+15V), 30mA (-15V), and 16mA (+5V). The average power required (P_D) is therefore

$P_D = |15\text{mA} \times 15\text{V}| + |30\text{mA} \times -15\text{V}| + |16\text{mA} \times 5\text{V}| = 755\text{mW}$.

Under certain operating conditions this power consumption can be reduced to as little as 250mW.

The ADC10HT is completely self-contained with an internal +10V reference voltage. The +15V supply is used only to supply power for the op amp current source and zener diode used in this reference. If an external reference is available, the +15V supply is not required and it can be removed. This reduces the P_D by 15mA x 15V = 225mW. The average P_D for the ADC10HT is therefore reduced to 530mW.

The major contributor to the power consumption is the -15V supply. As long as a +10V reference is used, the V- supply voltage must be between -13V and -16V. If, however, a lower voltage reference is used, this V- supply voltage can be reduced considerably which greatly reduces the power consumption. Lowering the reference voltage will, of course, lower the full scale input voltage by a proportional amount. For example, if the reference voltage is +5V, the full scale input voltage for the 10V range input (pin 22) will be +5V, instead of +10V with a +10V reference, in the unipolar mode of operation. Table IV indicates the minimum supply voltages and the typical power consumption obtained when using these supply voltages for various values of V_{REF}.

TABLE IV. Minimum Power Supply Voltages and Typical Power Consumption for Operation with External V_{REF}. (Note: +15V is not required if internal V_{REF} is not used.)

External V_{REF}	$+V_{LOGIC}$ (Pin 15)	-Vs (Pin 27) (Minimum)	Total Power Consumption (Typical)
+10V	+5V	-13V	470mW
+6.3V	+5V	-10V	300mW
+5V	+5V	-8V	250mW

LOW-POWER EXTERNAL REFERENCE

A simple external reference voltage can be made with a single resistor and a zener diode as shown in Figure 13. The power consumed by the reference is only about 75mW with $+V_S = +10V$. The power supply sensitivity of this reference is approximately ±0.02% of FSR/%V_S.

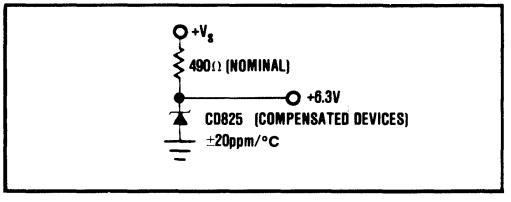


FIGURE 13. Simple +6.3V External Reference That Requires Only 75mW.

A very simple procedure can be used to obtain the lowest possible drift with this reference. First, vary the zener current from about 4mA to 11mA by changing either the bias voltage, $+V_S$, or bias resistor, R_B, and plot V_Z versus I_Z as shown in Figure 14. Next, heat the zener (the exact temperature is not important, but it should be near the desired operating temperature), and repeat the procedure. The point where the two curves cross is the zero-temperature-coefficient bias current. $+V_S$ and/or R_B should then be adjusted accordingly for this optimum operating current.

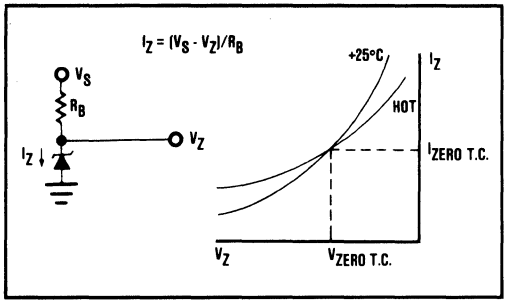


FIGURE 14. Simple Techniques for Obtaining a Low Drift Reference Voltage.

This procedure is also discussed in a Burr-Brown Application Note: "Squeeze High Performance out of Low-Cost Hybrid Data Converters, AN-86.

Other Application Notes

Burr-Brown also has other Application Notes of interest to the converter user. In particular:

"What Designers Should Know About Data Converter Drift," AN-89.

"Correcting Errors Digitally in Data Acquisition and Control," AN-101.

OPERATION WITH EXTERNAL CLOCK

Figure 15 shows the internal clock circuit of the ADC10HT. To operate with an external clock, first connect the Clock Rate Control (pin 16) to ground. This will shut off the internal clock and also turn off the open collector output transistor of the LM119 comparator. The Clock Out (pin 18) will then be in a "high" state (+5V) because of the 2kΩ pull-up resistor to +5V. Now simply use the Clock Out pin for the external clock input. Note that the external clock must have the capability of sinking 2.5mA when it is in the low state due to the 2kΩ pull-up resistor.

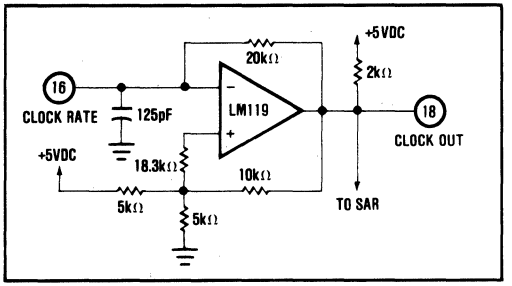


FIGURE 15. ADC10HT Internal Clock.

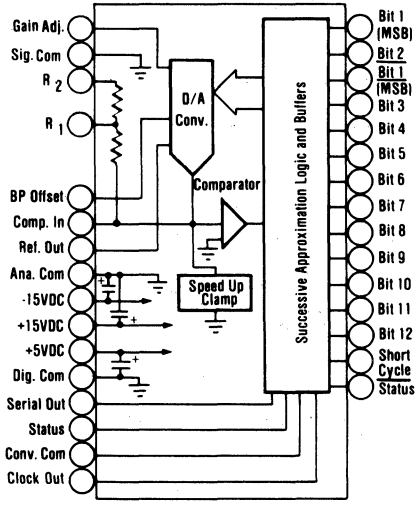
BURR-BROWN®

ADC60

High Speed ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **FAST CONVERSION SPEED:**
  12-bits - 3.5μsec, max
  10-bits - 1.88μsec, max
  8-bits - 0.88μsec, max
  Throughput sampling rates from 250kHz (12-bits) to 1MHz (8-bits) can be attained
- **PIN-PROGRAMMABLE UNIPOLAR OR BIPOLAR**
- **ANALOG SIGNALS**
- **SERIAL AND PARALLEL DATA OUTPUTS**
- **SELF-CONTAINED WITH INTERNAL CLOCK & REFERENCE**
  Simplifies system design and reduces cost
- **±1/2LSB LINEARITY**
  Provides accurate conversion
- **NO MISSING CODES**



DESCRIPTION

The Model ADC60 is a very high speed, successive approximation A/D converter than is designed for applications requiring system throughput sampling rates from 250kHz to 1MHz. The fast conversion speed is accomplished with proprietary fast settling circuits which preserve linearity and drift while permitting conversion speeds up to 100nsec/bit.

Available in 8-, 10-, and 12-bit resolutions the ADC60 contains an internal reference and clock. Internal components are provided for pin-programmable analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Digital data is available in both serial and parallel, binary form with corresponding timing signals. All digital input and output signals are DTL/TTL-compatible.

The ADC60 operates from ±15VDC and +5VDC power, and is housed in a 2" x 4" x 0.75" module with screened-on pin function identification.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-319A

THEORY OF OPERATION

Upon receipt of an external Convert Command, the previous data sample is cleared from the output register. Each bit is then successively compared against the amplitude of the input signal, and is either held as a "0" or turned on as a "1" until all bits have been tried. The parallel data output is not available for transfer to external devices until the Status output changes from logic "1" to logic "0".

Serial data is only available during conversion, and must be transferred to external devices with the Clock and Status signals beginning with the first clock pulse following a change in Status from logic "0" to logic "1".

TIMING CONSIDERATIONS

Data is available in both serial and parallel form. Timing signals are available for the transfer of data to external devices. For parallel data transfer, Status and its compliment Status indicate when the conversion is complete. For serial data transfer, the Clock Out signal starts on the trailing edge of the Convert Command; and serial data is valid before the positive going edge of the Clock Out signal. The Clock ceases operation when the conversion is complete. There will be one more clock pulse than the number of bits converted (resolution). Figure 1 shows the timing details of the ADC60.

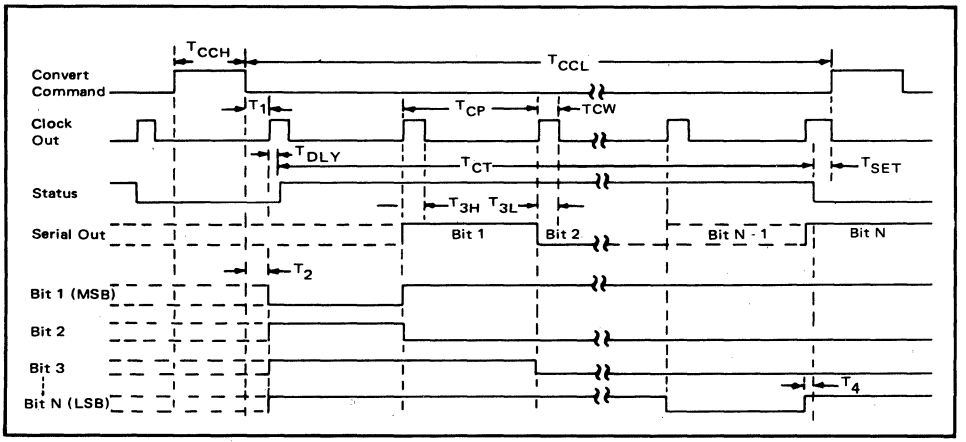


FIGURE 1. ADC60 Timing Diagram.

TABLE I. Switching Characteristics.

SYMBOL	PARAMETER DESCRIPTION	MIN.	TYP.	MAX.	UNITS
T_{CT}	Conversion Time - 12 Bit	2.50	3.45	3.50	µsec
	10 Bit	1.20	1.83	1.88	µsec
	8 Bit	0.80	0.84	0.88	µsec
T_{CCH}	Width of Convert Command Pulse	30	---	---	nsec
T_{CCL}	Internal Between Convert Command Pulses – ($T_{CT} + T_1 + T_{DLY}$)		(1)		
T_1	Delay From Trailing Edge of Conv. Command To Leading Edge of Clock Out	30	41	60	nsec
T_2	Delay from Conv. Command To Reset	26	40	68	nsec
T_{3H}	Delay From Valid High Output To Trailing Edge of Clock Out	22	43	70	nsec
T_{3L}	Delay From Valid Low Output To Trailing Edge of Clock Out	30	51	72	nsec
T_4	Delay From Valid Data to STATUS LOW	12	18	37	nsec
T_{DLY}	Delay From Clock Out to STATUS HIGH	22	44	60	nsec
T_{SET}	Setup Time from Status to Conv. Command - (2)	0	---	---	nsec
T_{CW}	Clock Out Width	40	50	60	nsec
T_{CP}	Clock Out Period - (3) 12 Bit	192	265	270	nsec
	10 Bit	104	165	171	nsec
	8 Bit	88	95	98	nsec

NOTES: 1. ADC60 internal clock may be inhibited by returning the convert command to "1". By this technique, the converter may be cycled through an entire conversion one clock pulse at a time. This technique allows the conversion time to be extended to virtually any conversion time.

2. The convert command may rise as soon as the last clock out pulse rises.
3. The clock period for ADC60 is not necessarily constant throughout the conversion time.

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

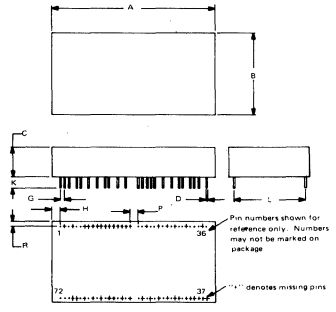
MODEL	ADC60-08	ADC60-10	ADC60-12	UNITS
RESOLUTION	8	10	12	Bits
INPUT				
ANALOG INPUTS				
Voltage Ranges, Bipolar	±2.5, ±5, ±10			V
Voltage Ranges, Unipolar	0 to +5, 0 to +10, 0 to +20			V
Impedance	0.2			kΩ/V FSR
DIGITAL INPUTS(1)				
Convert Command	Positive Pulse 30nsec wide (min. Trailing edge ("1" to "0" initiates conversion.			
Logic Loading	2			TTL Loads
TRANSFER CHARACTERISTICS				
ERROR(2)				
Gain Error	±0.2	±0.1	±0.1	% of FSR(3)
Offset Error	±0.2	±0.1	±0.1	% of FSR
Linearity Error, max	±0.195	±0.0488	±0.0244	% of FSR
Inherent Quantization Error	±0.19	±0.048	±0.012	% of FSR
Differential Linearity Error, max	±0.27	±0.068	+0.024, -0.019	% of FSR
Monotonicity	•	Guaranteed	•	
No Missing Codes	•	Guaranteed	•	
Power Supply Sensitivity	•	±0.002	•	% of FSR/%
DRIFT				
0°C to +70°C, max	±20	±20	±15	ppm/°C
-25°C to +85°C, max	±40	±40	±30	ppm/°C
CONVERSION SPEED, max	0.88	1.88	3.5	μsec
OUTPUT(4)				
DIGITAL DATA				
Parallel				
Output Codes, Unipolar	USB (straight binary)			
Output Codes, Bipolar	BOB (offset binary) and BTC (Two's Complement)			
Output Drive	6			TTL Loads
Serial Data Output Drive	6			TTL Loads
Status	"1" During Conversion			
$\overline{\text{Status}}$	"0" During Conversion			
Output Drive of Status and $\overline{\text{Status}}$	6			TTL Loads
Clock	A Positive Pulse Train Used for Strobing Serial Data into an External Register.			
Clock Output Drive	9			TTL Loads
INTERNAL REF. VOLTAGE	6.3			V
Max External Current with no degradation of Specifications	200			μA
POWER REQUIREMENTS				
Rated Voltages	±15 and +5			V
Range for Rated Accuracy	±14.5 to ±15.5 and +4.75 to +5.25			V
Supply Drain +15V	+50			mA
Supply Drain -15V (max)	-50			mA
Supply Drain +5V	+270			mA
PACKAGE	2" x 4" x 0.75"			
TEMPERATURE RANGE				
Specification	0 to +70			°C
Operating (reduced drift specs - see above)	-25 to +85			°C
Storage	-55 to +100			°C

NOTES:
1. All digital inputs in the ADC60 are TTL compatible (i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V, min.
2. Gain and Offset Errors may be adjusted to zero with external trimming.
3. FSR means Full Scale Range.
4. TTL compatible, Logic "0" = +0.4V, max, Logic "1" = +2.4V, min.

*Specifications same for all models.

MECHANICAL

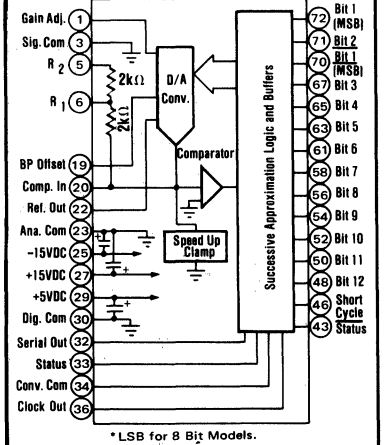
NOTE:
Leads in true position within .015" (.38mm) R @ MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.950	2.010	49.53	51.05
B	1.950	2.010	49.53	51.05
C	.350	4.10	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.300	6.35	7.62
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	.050	.150	1.27	3.81

Material: Case - Diallyl Phthalate Shell.
Weight: 5 oz.
Mating Connector: 2400MC - PC Card & Terminals
2401MC - Set of four 18-pin connector strips.
Pin spacing located on 2.54mm (0.10") grid. Allow 5.08mm (0.20") between pins 18-19 and 54-55. Pin material and plating composition meet method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

CONNECTION DIAGRAM



*LSB for 8 Bit Models.
**LSB for 10 Bit Models.
***LSB for 12 Bit Models.

DISCUSSION OF PERFORMANCE

ACCURACY

A/D converter error contributors are Quantization Error, Linearity Error, Drift, Gain and Offset errors. Figure 2 shows the transfer function of an ideal bipolar A/D converter, and describes the quantization and linearity error bands at a single temperature. Initial gain and offset errors are trimmed to zero. Gain drift rotates the line about the minus full scale point (or around zero for a unipolar A/D converter). Offset drift contributes an offset shift to the transfer function over the operating temperature range.

LINEARITY ERROR

Linearity Error is measured as the difference, in LSB, between the actual input voltage signal and the ideal transition voltage as shown in Figure 2. This measurement is made with Gain and Offset errors adjusted to zero. Thus, the Linearity Error, neglecting Quantizing Error, expresses the true accuracy of an A/D converter relative to the reading.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error is defined as the difference between actual adjacent transition values and an ideal 1LSB step. A Differential Linearity Error of 1/2LSB means that the size of a horizontal step can range from 1/2LSB to 3/2LSB. The size of the smallest step must be greater than 0.2LSB to guarantee no missing codes in an A/D converter. Expressed mathematically, Differential Linearity (D.L.)

$$\triangleq[(V_{j+1} - V_j) - \text{LSB}/\text{LSB}] \text{ where LSB} \triangleq V_{j+1} - V_j.$$

MONOTONICITY

An A/D converter is monotonic when the digital output code increases or remains the same for increasing analog input signals. The ADC60 is monotonic over the full scale range.

DIGITAL OUTPUT CODES

Three binary digital codes may be derived from the ADC60. They are Unipolar Straight Binary (USB) for unipolar analog input signals, and Bipolar Offset Binary (BOB) and Bipolar Two's Complement (BTC) for bipolar analog input signals. These codes are defined below in Table II.

A more detailed discussion of these and other A/D converters specifications is given in a separate Burr-Brown Application Note - AN53.

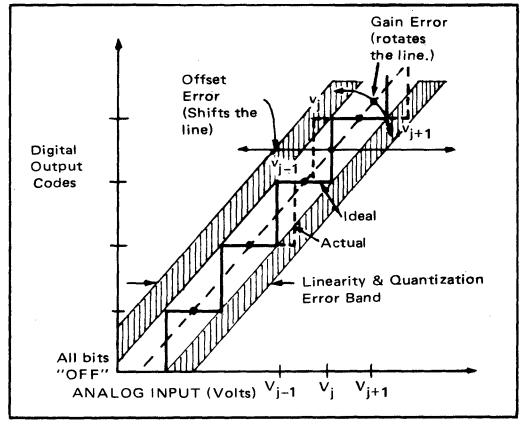


FIGURE 2. A/D Converter Definition of Specifications.

DEFINITION OF DIGITAL CODES

Three binary codes are available on the ADC60 parallel output; these are USB for unipolar input signals, and BOB or BTC for bipolar input signals. The LSB values and code definitions for each analog input signal range are shown below.

TABLE II. Input Voltages, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Signal Range	Defined As:	±10V	±5V	±2.5V	0 to +20V	0 to +10V	0 to +5V
Code Designation		BOB or BTC*	BOB or BTC*	BOB or BTC*	USB**	USB**	USB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	78.13mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	19.53mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	4.88mV	2.44mV	1.22mV
MSB LSB							
111....111***	+Full Scale	+10V -½LSB	+5V -½LSB	+2.5V -½LSB	+20V -½LSB	+10V -½LSB	+5V -½LSB
100....000	Mid Scale	0	0	0	+10V	+5V	+2.5V
000....001	-Full Scale	-10V +½LSB	-5V +½LSB	-2.5V +½LSB	0 +½LSB	0 +½LSB	0 +½LSB

*BOB = Bipolar Offset Binary
**USB = Unipolar Straight Binary
BTC = Bipolar Two's complement - obtained by using the complement of the most significant bit (MSB). MSB is available on pin 70 of the module.
*** Voltages given are the nominal value for transition to the code specified.

INSTALLATION AND OPERATING INSTRUCTIONS

The ADC60 is available with binary code resolutions of 8, 10 and 12 bits. Six input signal ranges are pin-programmable over the following ranges: 0 to +5V, +20V, +10V, ±2.5V, ±5V and ±10V.

Single polarity binary ranges are designated USB and dual polarity binary ranges are designated BOB or BTC. Connections for specific codes are detailed in Table III.

OPTIONAL GAIN AND OFFSET ADJUST

Although Gain and Offset are factory trimmed to ±0.1%, these parameters may be trimmed to zero error using external trim adjustments as shown in Figure 3. Due to component aging, these external adjustments may be required later on to recalibrate the ADC60 after 3 to 6 months.

To avoid interaction between adjustments, the offset should be adjusted first. Use multiturn potentiometers with TCR of 150ppm °C or better.

Offset is adjusted by sweeping the input through the end point transition voltage that causes an output transition to "all bits Off". Adjust the Offset potentiometers until the actual end point transition voltage occurs at the value shown in Table II.

Gain is adjusted by sweeping the input voltage through the end point transition that causes an output digital code of "all bits On". See Table I for end point transition values.

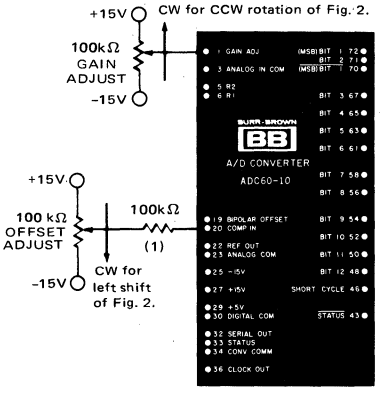


FIGURE 3. ADC60 Installation Diagram.

NOTE:
1. If Gain and/or Offset trim adjustments are not used simply leave pin 1 and/or pin 20 open. The minimum range of adjustment for OFFSET is ±0.25% of full scale range; for GAIN it is ±0.3% of full scale range. Locate the 100kΩ resistor as close as possible to pin 20..

GENERAL NOTES:
- If an input buffer amplifier is required, the BB3550 is recommended.
- Use BB SHM60 Sample/Hold if a Sample/Hold is required (1μsec acquisition time).

INPUT SCALING

To utilize the maximum resolution of the ADC60, the input FSR must be selected to match the expected full scale range of the input signal. Figure 4 and TableIII show the connections required for input scaling.

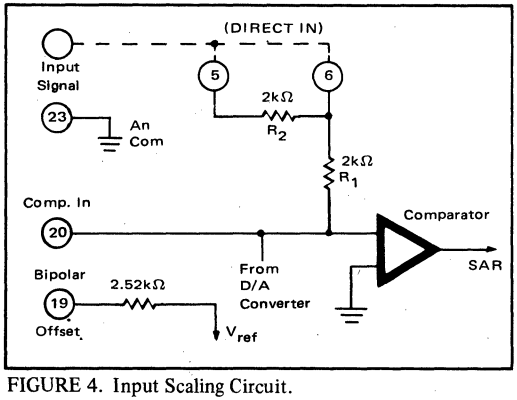


FIGURE 4. Input Scaling Circuit.

TABLE III. ADC60 Input Scaling Connections.

INPUT SIGNAL RANGE	DIGITAL OUTPUT CODE	CONNECT PIN 19 TO	CONNECT PIN 5 TO	CONNECT INPUT SIGNAL TO
±2.5V	BOB or BTC	PIN 20	PIN 20	PIN 6
0 to +5V	USB	PIN 23	PIN 20	PIN 6
±5V	BOB or BTC	PIN 20	OPEN	PIN 6
0 to +10V	USB	PIN 23	OPEN	PIN 6
0 to +20V	USB	PIN 23	INPUT	PIN 5
±10V	BOB or BTC	PIN 20	INPUT	PIN 5

INSTALLATION AND OPERATING INSTRUCTIONS (CONT)

SYSTEM TIMING

The basic system timing diagram is shown in Figure 1.

CONVERT COMMAND

A pulse of at least 30nsec duration (positive going) is required at pin 34 to start each conversion. Conversion starts after the Negative Going edge of the Convert Command.

STATUS

The Status output switches to a logical "1" on the Negative Edge of the Convert Command pulse. It returns to a logical "0" at the end of the conversion. The $\overline{\text{Status}}$ output leads Status by one normal gate delay (10nsec).

SHORT CYCLE

The ADC60 may be short-cycled for obtaining lower resolutions and corresponding faster conversion speeds. Connect "Short Cycle" (pin 46) of the ADC60 to bit N + 1 as shown in Table IV.

The Short Cycle feature must be used for the 8- and 10-bit models as outlined in Table IV. For 12-bit models, the Short Cycle is not used and may be left open; however, in a high noise environment, the Short Cycle input, pin 46, should be tied to +5V (pin 29) through a 1000Ω resistor.

TABLE IV. Short Cycle Connections for ADC60 and Corresponding Conversion Speeds.

RESOLUTION (BITS)	CONNECT PIN 46 TO PIN	MAXIMUM CONVERSION TIME (μSEC)		
		MODEL		
		8	10	12
12	N/A	–	–	3.50
11	48	–	–	3.24
10	50	–	1.88	2.97
9	52	–	1.71	2.70
8	54	0.88	1.53	2.43
7	56	0.79	1.37	2.16
6	58	0.69	1.20	1.89
5	61	0.59	1.03	1.62
4	63	0.49	0.85	1.35

ADC60

APPLICATION NOTE

HIGH SPEED DATA ACQUISITION SYSTEM

A high speed 16-channel data acquisition system with up to 625kHz system sampling rate is shown below. (If the ADC60 is used without a multiplexer or sample/hold for single channel applications, sampling rates up to 1MHz are possible.)

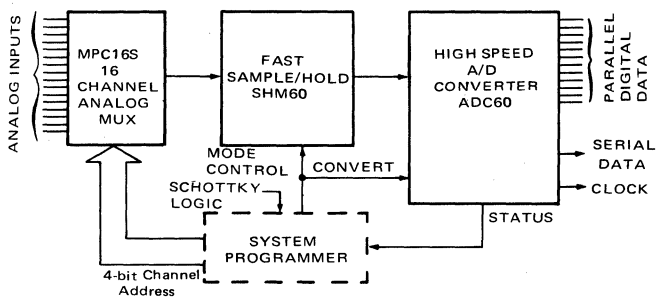


TABLE V. Typical System Characteristics.

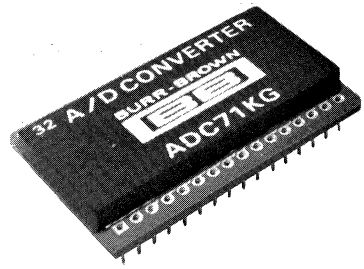
RESOLUTION (BITS)	INPUT SIGNAL RANGE (volts)	SYSTEM THROUGHPUT SAMPLING RATE (max)	TYPICAL SYSTEM ACCURACY *RSS
12	±10	200kHz	±0.04%
12	0 to +10	220kHz	±0.04%
10	±10	325kHz	±0.125%
10	0 to +10	370kHz	±0.125%
8	±10	530kHz	±0.25%
8	0 to +10	625kHz	±0.25%

*RSS = Root Sum Squared.

The system shown uses an overlapped mode programmer to eliminate or reduce the settling effects of the multiplexer and sample/hold and maximizes system throughput speed.

Typical system sampling speeds for the input signal ranges using these components are shown in Table V.

BURR-BROWN®



ADC71

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES:

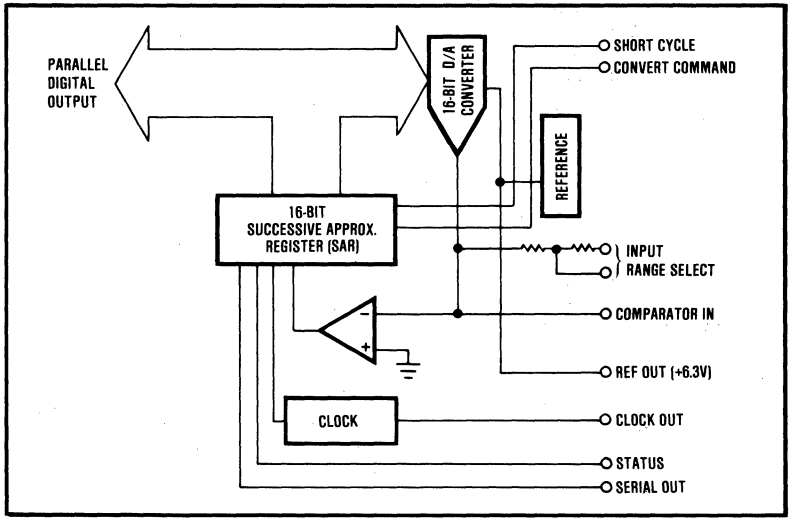
- 16-BIT RESOLUTION
- LINEARITY ERROR ±0.003%
- COMPACT DESIGN
  32-Pin Ceramic Package
- FAST CONVERSION SPEED
- LOW COST

DESCRIPTION

The ADC71 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The ADC71 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a convenient 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, and thin-film scaling resistors, which allows selection of analog input ranges of ±2.5V, ±5.0V, ±10.0V, 0 to +5.0V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are DTL/TTL compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

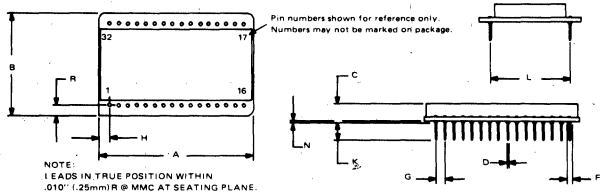
Typical at +25°C and rated power supplies unless otherwise noted.

MODEL	ADC71KG			ADC71JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL INPUTS(1)							
Convert Command	Positive pulse 50nsec wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1			1	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0.1(2)	±0.2		±0.1(2)	±0.2	%
Offset							
Unipolar		±0.05(2)	±0.1		±0.05(2)	±0.1	% of FSR(3)
Bipolar		±0.1(2)	±0.2		±0.1(2)	±0.2	% of FSR
Linearity Error			±0.003			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%V_S
+5VDC		0.001			0.001		% of FSR/%V_S
CONVERSION TIME(4) (14 Bits)			50			50	μsec
WARM-UP TIME	5			5			min
DRIFT							
Gain			±15			±15	ppm/°C
Offset							
Unipolar		±2	±4		±2	±4	ppm of FSR/°C
Bipolar			±10			±10	ppm of FSR/°C
Linearity		±2	±3		±2	±3	ppm of FSR/°C
No Missing Codes Temp Range							
KG (14-bit)	+10		+40				°C
JG (13-bit)				0		50	°C
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes(5)			CSB				
Unipolar			COB, CTC(6)				
Bipolar			2				TTL Loads
Output Drive			CSB, COB				
Serial Data Code (NRZ)			2				TTL Loads
Output Drive			Logic "1" during conversion				
Status			2			2	TTL Loads
Status Output Drive							
Internal Clock			2			2	TTL Loads
Clock Output Drive		280			280		kHz
Frequency							
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with No Degradation of Specs			±200			±200	μA
Temp Coefficient			±10			±10	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		1.55			1.55		W
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+45			+45		mA
Supply Drain -15VDC		-35			-35		mA
Supply Drain +5VDC		+70			+70		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (derated specs)	-25		+85	-25		+85	°C
Storage	-55		+125	-55		+125	°C

NOTES:
1. DTL/TTL compatible, i.e., Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max. Logic "1" = 2.4V, min.
2. Adjustable to zero.
3. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR.
4. Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section.
5. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
6. CTC coding obtained by inverting MSB (Pin 1).

MECHANICAL

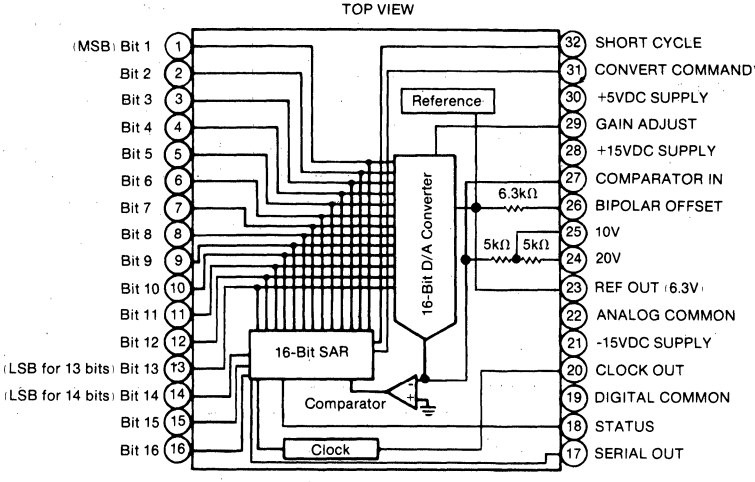
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30



NOTE:
LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.

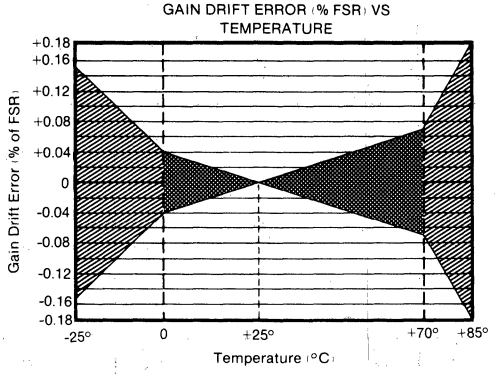
CASE: Ceramic
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0.46 oz.)

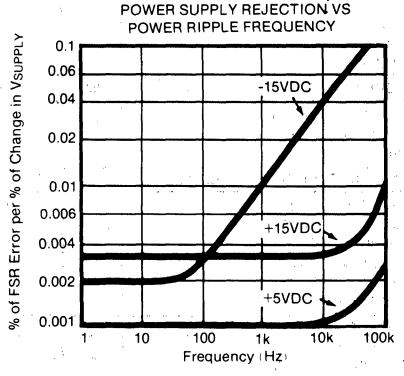
CONNECTION DIAGRAM



*If an external clock is used, connect the clock to pin 31 (CONVERT COMMAND).

TYPICAL PERFORMANCE CURVES





DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2 LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC71 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation.

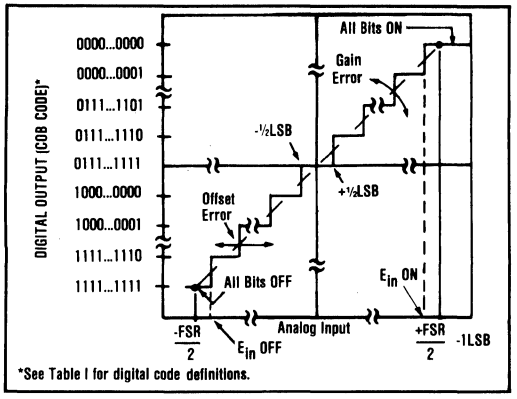


FIGURE 1. Input vs Output for an Ideal Bipolar A D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output).

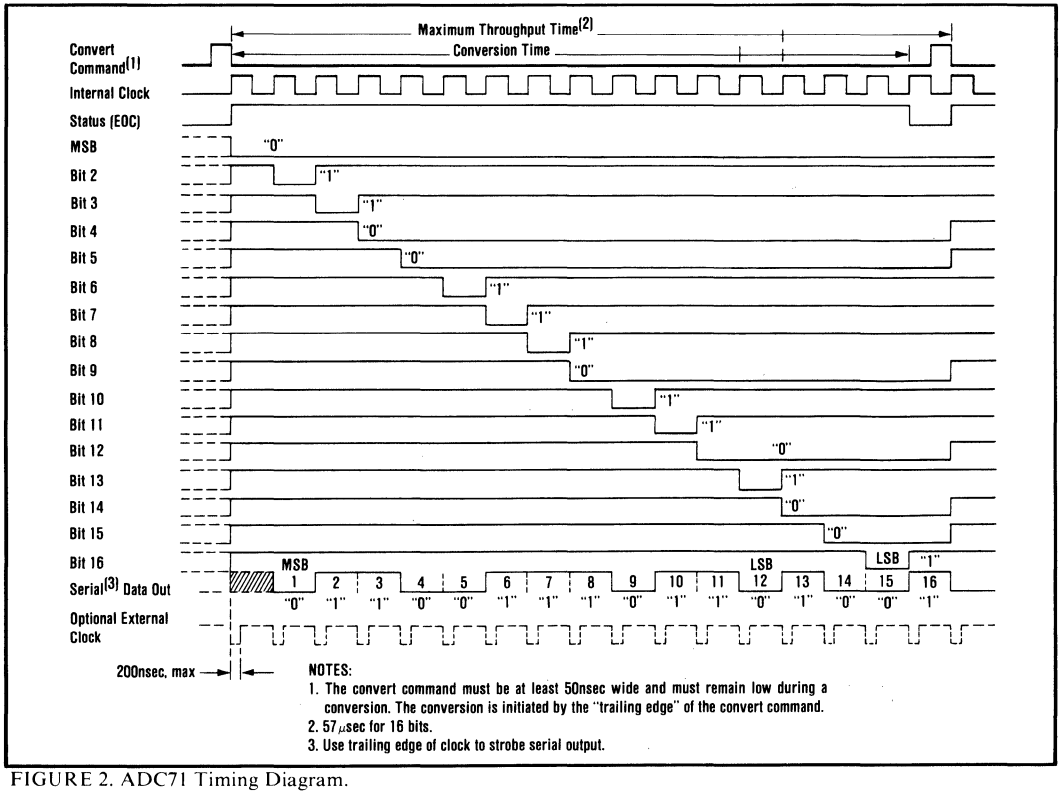


FIGURE 2. ADC71 Timing Diagram.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Two binary codes are available on the ADC71 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with the MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

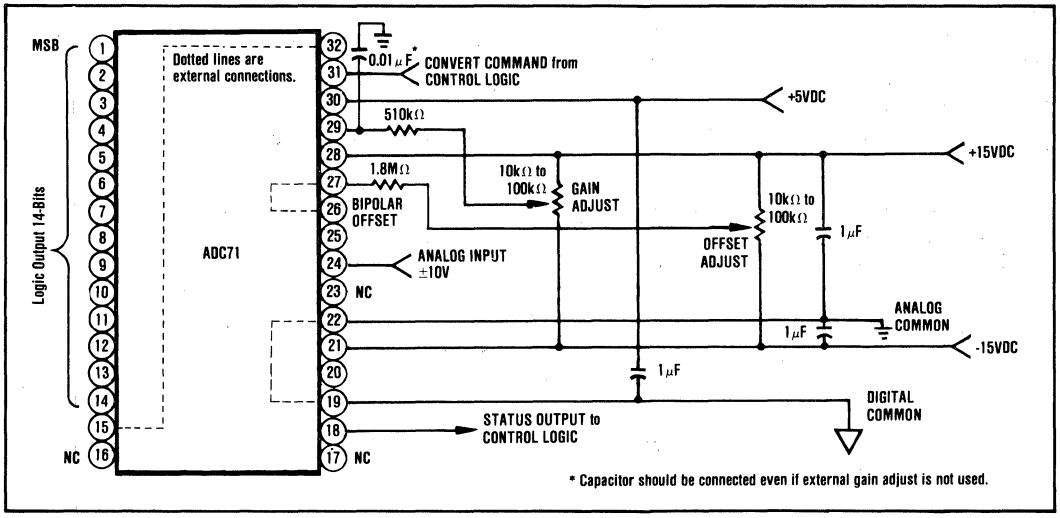


FIGURE 3. ADC71 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary
**CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB (Pin 1)
***CSB = Complementary Straight Binary
****Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC71 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC71 power supply sensitivity is specified for ±0.003% of FSR/%V, for ±15V supplies and ±0.0015% of FSR/%V, for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC71 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

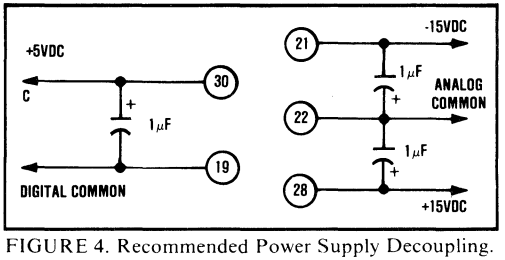


FIGURE 4. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

TABLE II. ADC71 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (Pin 1).

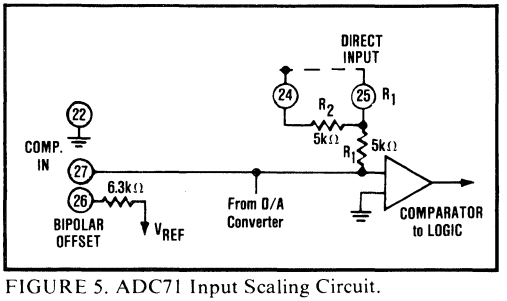


FIGURE 5. ADC71 Input Scaling Circuit.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 6. Sweep the input through the end point transition voltage

that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

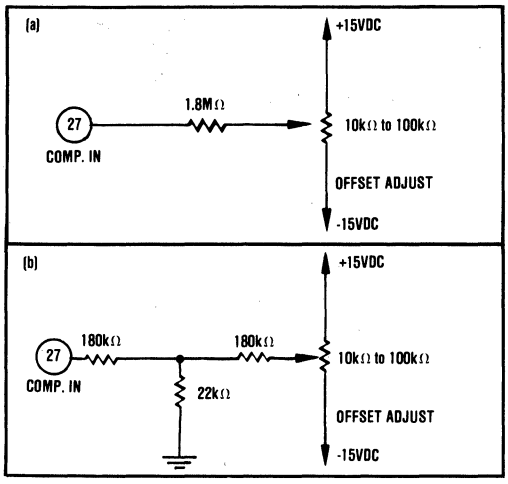


FIGURE 6. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

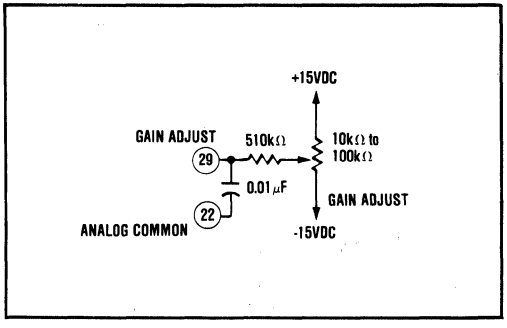


FIGURE 7. Connecting Optional Gain Adjust with a 0.6% Range of Adjustment.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to convert command, pin 31. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start on the first falling edge of the external clock following the completion of conversion. The clock out signal will remain as shown in Figure 2 even if an external clock is used. The external clock pulse must be a negative going pulse with a width between 100nsec and 200nsec as shown in Figure 2, and must be at a lower frequency than the internal clock.

ADDITIONAL CONNECTIONS REQUIRED

The ADC71 may be operated at faster speeds for resolutions less than 14 or 13 bits, depending on the model selected, by connecting the Short Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

TABLE III. Short Cycle Connections and Specifications for 12- to 14-Bit Resolutions.

Resolution - Bits	14	13	12
Connect Pin 32 to	Pin 15	Pin 14	Pin 13
Maximum Conversion Speed - μsec (1)	50	46.5	43
Maximum Nonlinearity at 25°C - % of FSR	0.003(2)	0.006(3)	0.006(3)

NOTES:
1. Max. conversion time to maintain specified nonlinearity error.
2. ADC71KG only.
3. ADC71KG or ADC71JG.

OUTPUT DRIVE

Normally all ADC71 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC71 dissipates approximately 1.55 watts (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C W. For operation above 70°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 8 for θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square inch (min.) area, this technique will allow operation to 85°C.

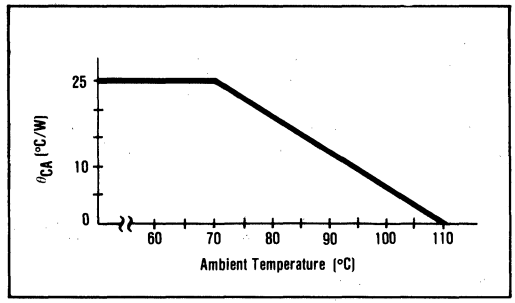


FIGURE 8. θ_{CA} Requirement Above 70°C.

ORDERING INFORMATION

MODEL	TEMPERATURE	PACKAGE
ADC71KG	0°C to +70°C	Ceramic
ADC71JG	0°C to +70°C	Ceramic

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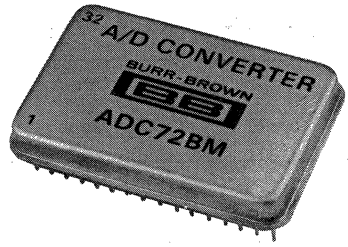


ADC72

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES:

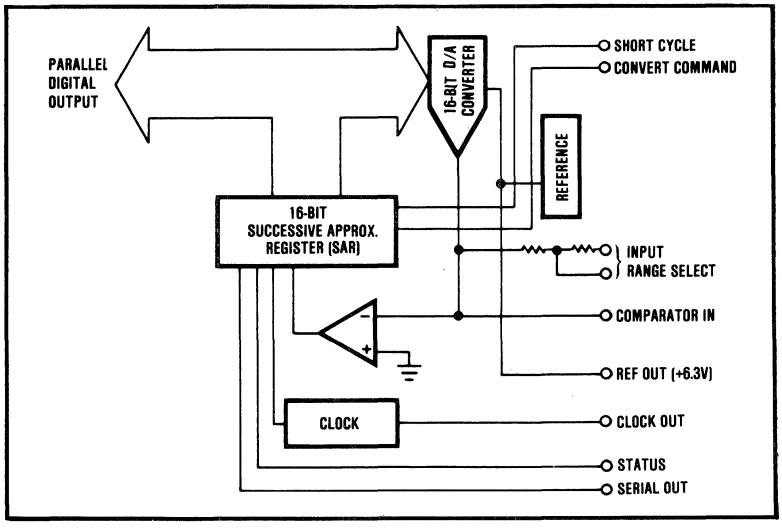
- 16-BIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- COMPACT DESIGN
  32-Pin Hermetic Metal Package
- FAST CONVERSION SPEED
  50μsec Maximum
- LOW COST

DESCRIPTION

The ADC72 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. It uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a compact 32-pin metal dual-in-line package. The converter is complete with internal reference, clock, comparator, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are DTL/TTL compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-432A

SPECIFICATIONS

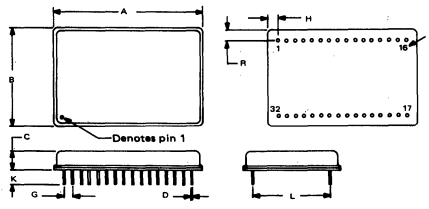
Typical at +25°C and rated power supplies unless otherwise noted.

MODEL	ADC72JM, KM			ADC72AM, BM			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
INPUT							
ANALOG							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL(1)							
Convert Command	Positive pulse 50nsec wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading		1				1	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(2)		±0.1	±0.2		±0.1	±0.2	%
Offset Gain(2)							
Unipolar		±0.05	±0.1		±0.05	±0.1	% of FSR(3)
Bipolar		±0.1	±0.2		±0.1	±0.2	% of FSR
Linearity Error KM, BM			±0.003			±0.003	% of FSR
JM, AM			±0.006			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		±0.003			±0.003		% of FSR/%ΔVs
+5VDC		±0.001			±0.001		% of FSR/%ΔVs
CONVERSION TIME(4) (14 Bits)			50			50	μsec
WARM-UP TIME	10			10			min
DRIFT							
Gain		±10	±20		±7	±15	ppm/°C
Offset							
Unipolar		±2	±4			±2	ppm of FSR/°C
Bipolar		±8	±10		±5	±10	ppm of FSR/°C
Linearity		±2	±3			±2	ppm of FSR/°C
No Missing Codes Temp Range							
JM, AM (13 bits)	0		+50	0		+50	°C
KM, BM (14 bits)	+10		+40	+10		+40	°C
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes(5)							
Unipolar			CSB				
Bipolar			COB, CTC(6)				
Output Drive			2				TTL Loads
Serial Data Code (NRZ)			CSB, COB				
Output Drive			2				TTL Loads
Status			Logic "1" during conversion				
Status Output Drive			2			2	TTL Loads
Internal Clock							
Clock Output Drive			2			2	TTL Loads
Frequency		280			280		kHz
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Max External Current with No Degradation of Specs			±200			±200	μA
Temp Coefficient			±10			±5	ppm/°C
POWER SUPPLY REQUIREMENTS							
Power Consumption		1.3			1.3		W
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+45			+45		mA
Supply Drain -15VDC		-35			-35		mA
Supply Drain +5VDC		+70			+70		mA
TEMPERATURE RANGE							
Specification	0		+70	-25		+85	°C
Operating (derated specs)	-25		+85	-55		+85	°C
Storage	-55		+125	-55		+125	°C

NOTES:
1. DTL/TTL compatible, i.e., Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V, max. Logic "1" = 2.4V, min.
2. Adjustable to zero.
3. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR.
4. Conversion time may be shortened with "Short Cycle" set for lower resolution, see "Additional Connections Required" section.
5. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
6. CTC coding obtained by inverting MSB (Pin 1).

MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

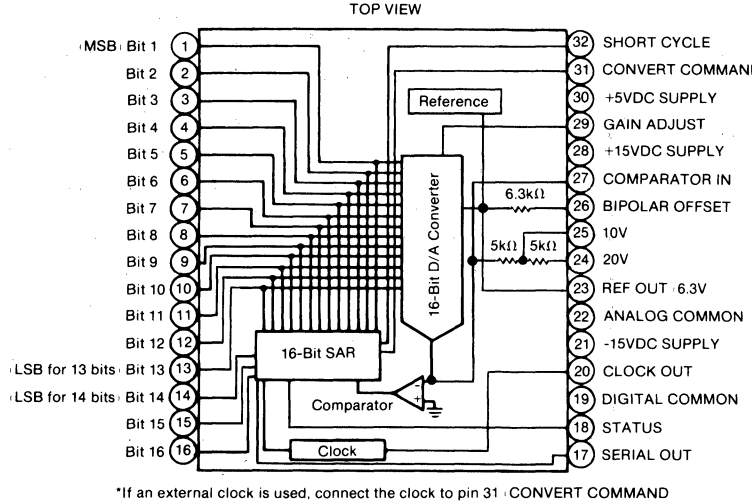


NOTE:
Leads in true position within .010" (.255mm) R at MMC at seating plane.

Pin numbers shown for reference only.
Numbers may not be marked on package.

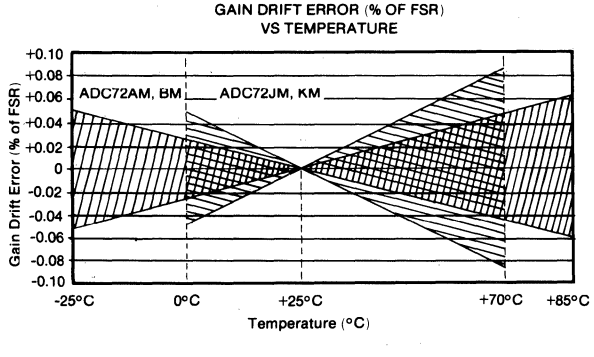
CASE: Nickel-plated kovar
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0.46 oz.)

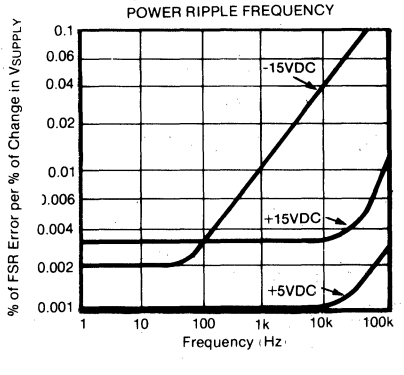
CONNECTION DIAGRAM



*If an external clock is used, connect the clock to pin 31 (CONVERT COMMAND)

TYPICAL PERFORMANCE CURVES





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The ADC72 is also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperature range when short-cycled for 14-bit operation.

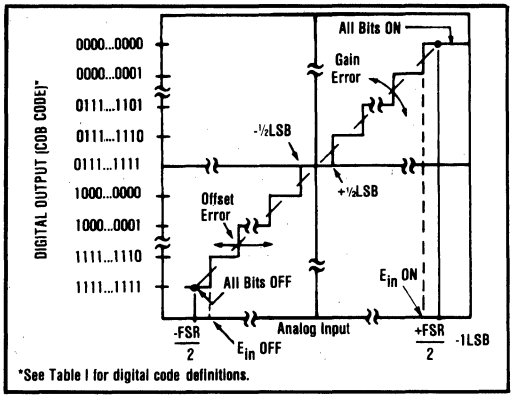

FIGURE 1. Input vs Output for an Ideal Bipolar A D Converter.

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The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output).

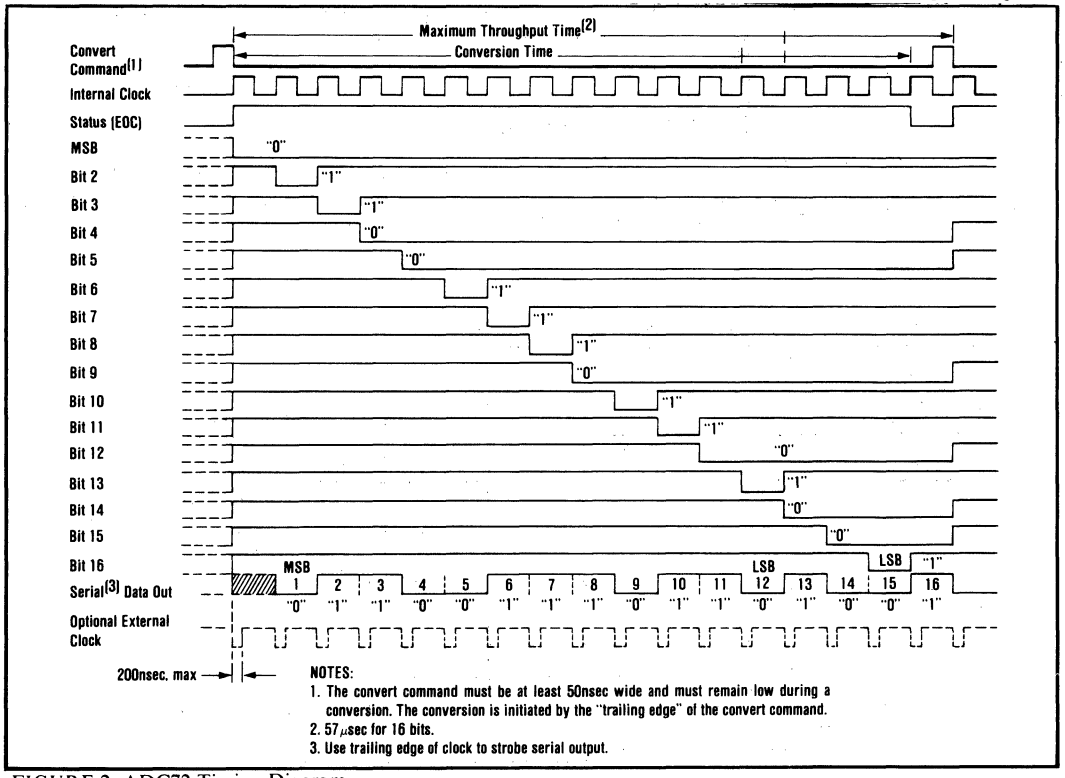

FIGURE 2. ADC72 Timing Diagram.

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Two binary codes are available on the ADC72 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (Pin 1).

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SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line CSB and COB. The serial data is available only during conversion and appears with the MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

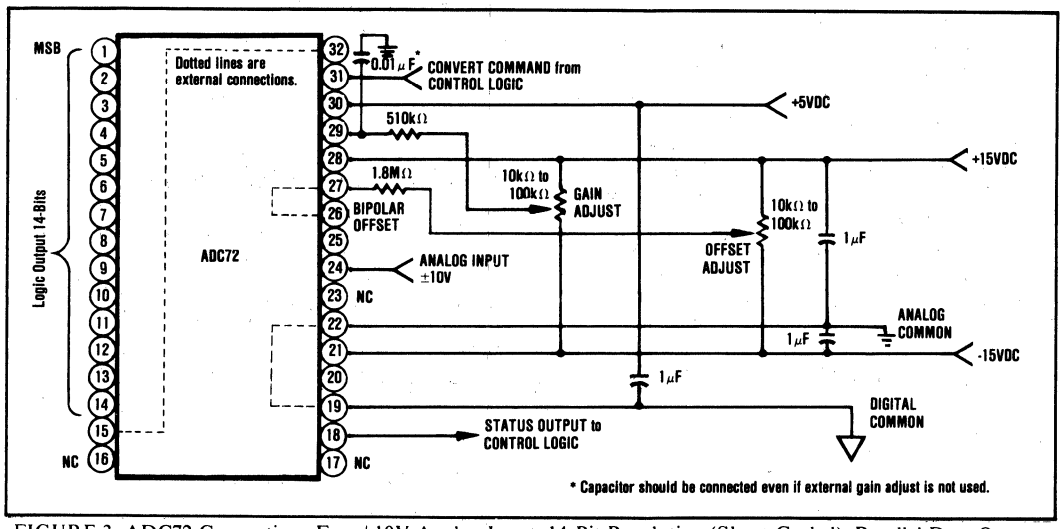


FIGURE 3. ADC72 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

(1) COB = Complementary Offset Binary
(2) CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB (Pin 1)
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC72 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC72 power supply sensitivity is specified for ±0.003% of FSR/%ΔV_S for ±15V supplies and ±0.001% of FSR/%ΔV_S for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling and Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECATUIONS

Analog and digital common are not connected internally in the ADC72 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF non-polarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (Pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 4 to obtain noise free operation. These capacitors should be located close to the ADC. Bypass 1μF electrolytic type capacitors with 0.01μF ceramic capacitors for improved high frequency performance.

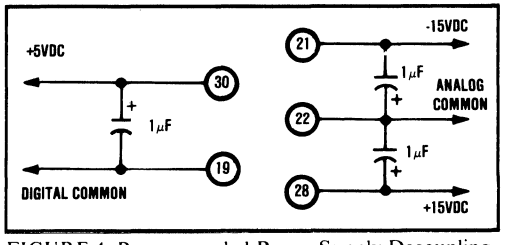


FIGURE 4. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 5 for circuit details.

TABLE II. ADC72 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (Pin 1).

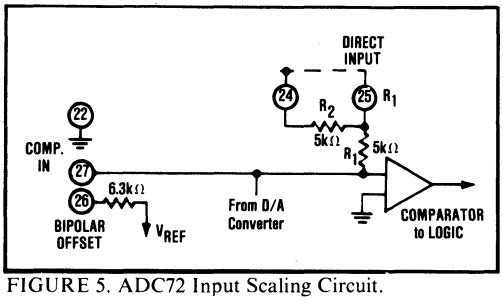


FIGURE 5. ADC72 Input Scaling Circuit.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 6 and 7. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and Pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all bits Off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

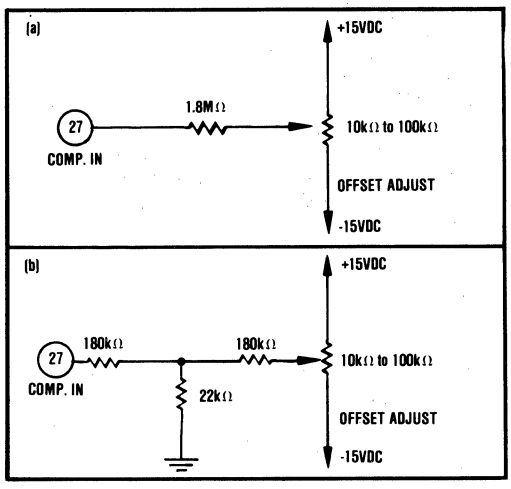


FIGURE 6. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 7. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

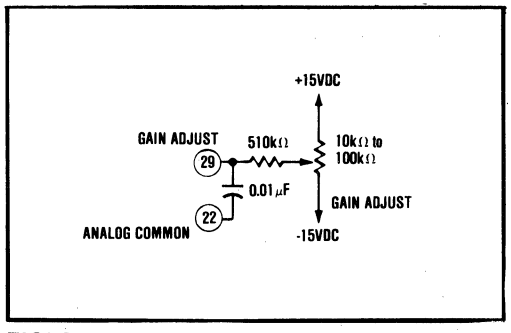


FIGURE 7. Connecting Optional Gain Adjust with a 0.6% Range of Adjustment.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to convert command, pin 31. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start on the first falling edge of the external clock following the completion of conversion. The clock out signal will remain as shown in Figure 2 even if an external clock is used.

The external clock pulse must be a negative-going pulse with a width between 100nsec and 200nsec as shown in Figure 2, and must be at a lower frequency than the internal clock.

ADDITIONAL CONNECTIONS REQUIRED

The ADC72 may be operated at faster speeds for resolutions less than 14 or 13 bits, depending on the model selected, by connecting the Short-Cycle Input, pin 32, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

TABLE III. Snort-Cycle Connections and Specifications for 12- to 14-Bit Resolutions.

Resolution (Bits)	14	13	12
Connect Pin 32 to	Pin 15	Pin 14	Pin 13
Maximum Conversion Speed (μsec) (1)	50	46.5	43
Maximum Nonlinearity at 25°C (% of FSR)	0.003 (2)	0.006	0.006

NOTES:
1. Max. conversion time to maintain specified nonlinearity error.
2. BM and KM models only.

OUTPUT DRIVE

Normally all ADC72 logic outputs will drive 2 standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC72 dissipates approximately 1.3 watts (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above 70°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 8 for θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square inch (min.) area, this technique will allow operation to 85°C.

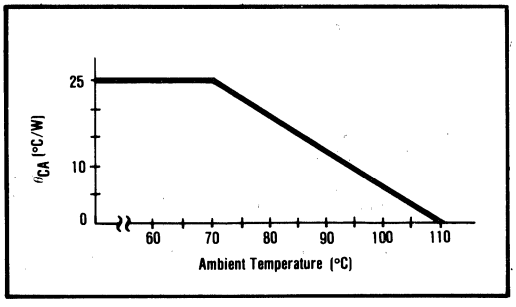


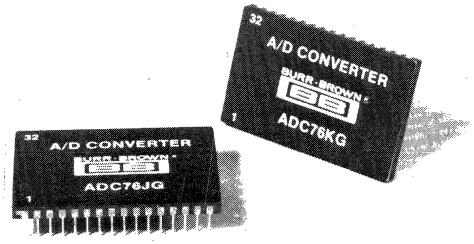
FIGURE 8. θ_{CA} Requirement Above 70°C.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	NONLINEARITY
ADC72JM	0°C to +70°C	±0.006% FSR
ADC72KM	0°C to +70°C	±0.003% FSR
ADC72AM	-25°C to +85°C	±0.006% FSR
ADC72BM	-25°C to +85°C	±0.003% FSR

BURR-BROWN®

ADC76



16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

FEATURES

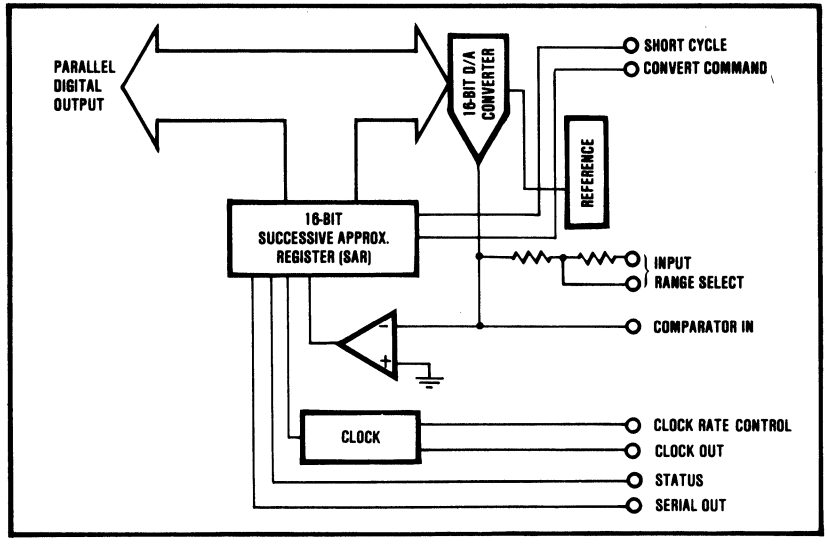
- 16-BIT RESOLUTION
- LINEARITY ERROR ±0.003% MAX (KG)
- COMPACT DESIGN
  32-Pin Ceramic Package
- LOW COST
- 15μsec CONVERSION TIME (14-BIT)

DESCRIPTION

The ADC76 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a convenient 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, and thin-film scaling resistors, which allows selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are DTL/TTL compatible.

Power supply voltages are ±15VDC and +5VDC.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

The ADC76 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation.

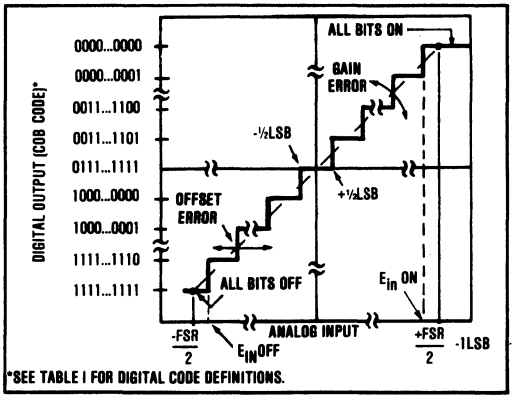


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output).

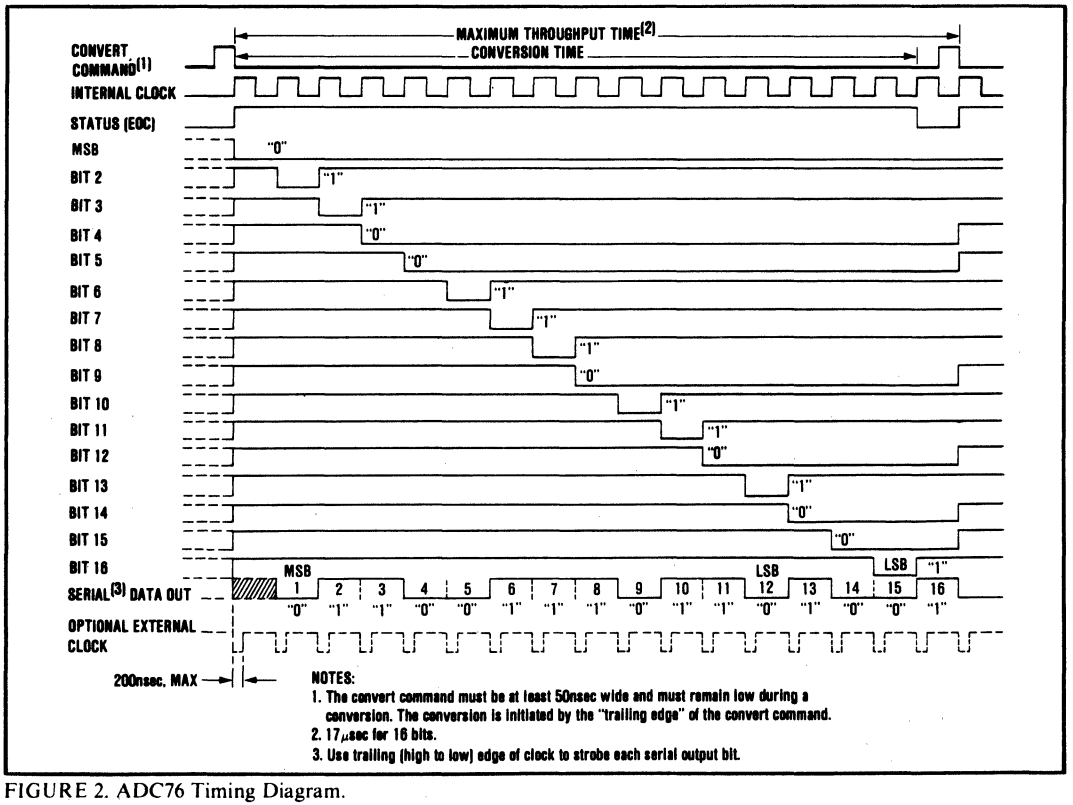


FIGURE 2. ADC76 Timing Diagram.

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC76 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

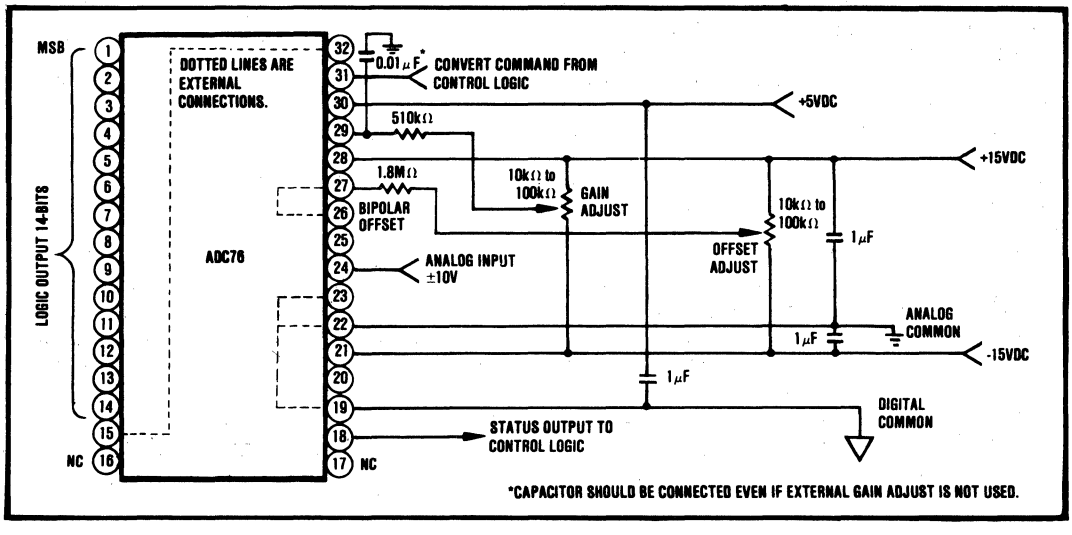


FIGURE 3. ADC76 Connections For: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

(1)COB = Complementary Offset Binary

(2)CTC = Complementary Two's Complement - obtained by inverting the most significant bit. MSB (pin 1).

(3)CSB = Complementary Straight Binary

(4)Voltages given are the nominal value for transition to the code specified.

SPECIFICATIONS

ELECTRICAL

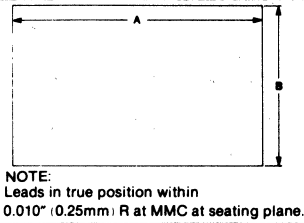
At +25°C and rated power supplies unless otherwise noted.

MODEL	ADC76KG			ADC76JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
ANALOG INPUTS							
Voltage Ranges							
Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Unipolar		0 to +5, 0 to +10, 0 to +20			0 to +5, 0 to +10, 0 to +20		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5.0V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL INPUTS(1)							
Convert Command	Positive pulse 50nsec wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1			1	TTL Load
External Clock	Negative pulse 100-200nsec wide. Frequency < internal clock(2)						
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(3)		+0.1	±0.2		±0.1	±0.2	%
Offset Error							
Unipolar(3)		±0.05	±0.1		±0.05	±0.1	% of FSR(4)
Bipolar(3)		±0.1	±0.2		±0.1	±0.2	% of FSR
Linearity Error			±0.003			±0.006	% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
Differential Linearity Error		±0.003			±0.003		% of FSR
Noise (3σ, p-p)		±0.003			±0.003		% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%Vs
+5VDC		0.001			0.001		% of FSR/%Vs
CONVERSION TIME(5) (14 Bits)			15			15	µsec
WARM-UP TIME	5			5			min
DRIFT							
Gain			±15			±15	ppm/°C
Offset							
Unipolar		±2	±4		±2	±4	ppm of FSR/°C
Bipolar			±10			±10	ppm of FSR/°C
Linearity		±2	±3		±2	±3	ppm of FSR/°C
No Missing Codes Temp Range							
KG (14-bit)	+10		+40				°C
JG (13-bit)				0		50	°C
OUTPUT							
DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes(6)							
Unipolar		CSB			CSB		
Bipolar		COB, CTC(7)			COB, CTC(7)		
Output Drive			2			2	TTL Loads
Serial Data Code (NRZ)		CSB, COB			CSB, COB		
Output Drive			2			2	TTL Loads
Status	Logic "1" during conversion			Logic "1" during conversion			
Status Output Drive			2			2	TTL Loads
Internal Clock							
Clock Output Drive			2			2	TTL Loads
Frequency(8)	933		1400	933		1400	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		1.55			1.55		W
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+45			+45		mA
Supply Drain -15VDC		-35			-35		mA
Supply Drain +5VDC		+70			+70		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (derated specs)	-25		+85	-25		+85	°C
Storage	-55		+125	-55		+125	°C

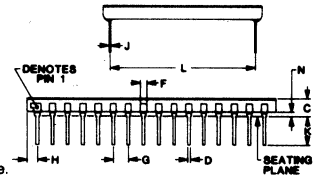
NOTES:
1. DTL/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1" = 2.4V, min.
2. See External Clock operating instructions.
3. Adjustment to zero. See "Optional External Gain and Offset Adjustment" section.
4. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR.
5. Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor.
6. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
7. CTC coding obtained by inverting MSB (pin 1).
8. Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 12 and 13 and Table III.

MECHANICAL

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	180	210	4.57	5.33
D	016	020	41	51
F	045	055	1.14	1.40
G	100 BASIC		2.54 BASIC	
H	089	106	2.26	2.69
J	009	012	23	30
K	200	210	5.08	5.33
L	900 BASIC		22.86 BASIC	
N	015	035	38	89

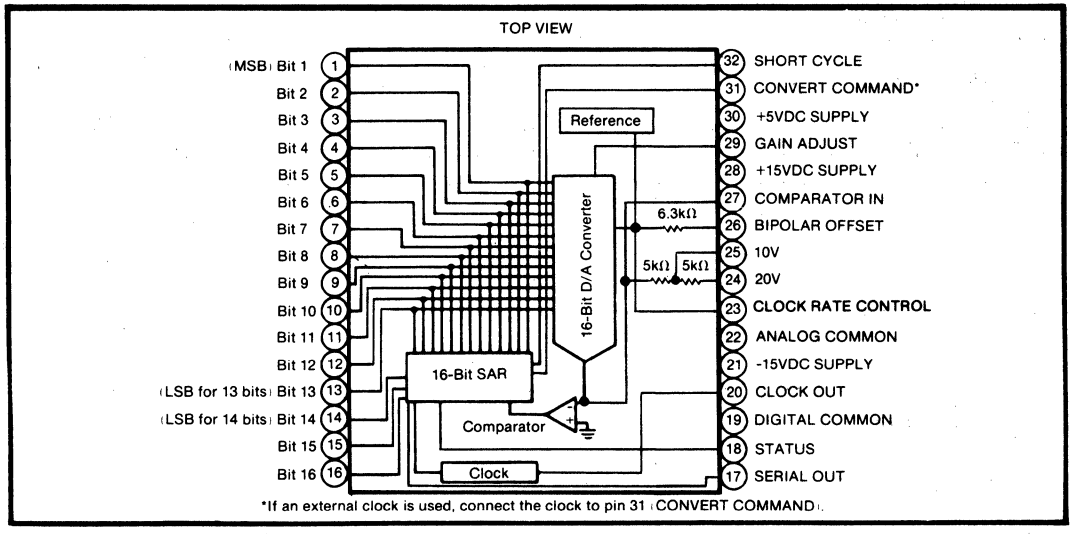


NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



CASE: Ceramic
MATING CONNECTOR: 2302MC
WEIGHT: 13 grams (0.46 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

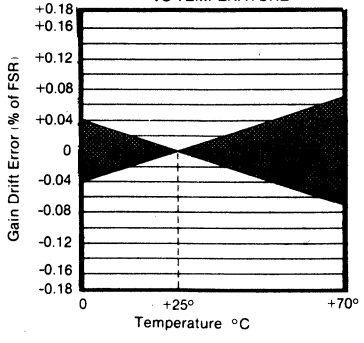
CONNECTION DIAGRAM



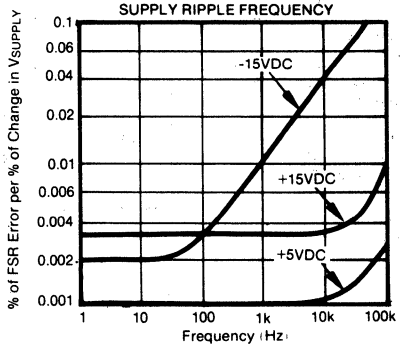
*If an external clock is used, connect the clock to pin 31 (CONVERT COMMAND).

TYPICAL PERFORMANCE CURVES

GAIN DRIFT ERROR (% OF FSR) VS TEMPERATURE



POWER SUPPLY REJECTION VS SUPPLY RIPPLE FREQUENCY



DISCUSSION OF SPECIFICATIONS

The ADC76 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 7 and 8.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. The ADC76 power supply sensitivity is specified at ±0.003% of FSR/%V_S for the ±15V supplies and ±0.0015% of FSR/%V_S for the +5V supply. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 5.

LINEARITY ERROR

Linearity error is not adjustable and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential linearity describes the step size between transition values. A differential linearity error of ±0.003% of FSR indicates that the size of any step may not vary from the ideal step size by more than 0.003% of Full Scale Range.

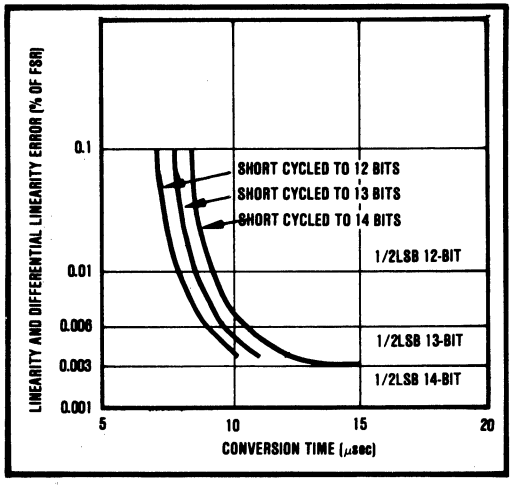


FIGURE 4. Linearity and Differential Linearity Versus Conversion Time.

ACCURACY VERSUS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC76 are shown in Figure 4.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC76, but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 5 to obtain noise free operation. These capacitors should be located close to the ADC.

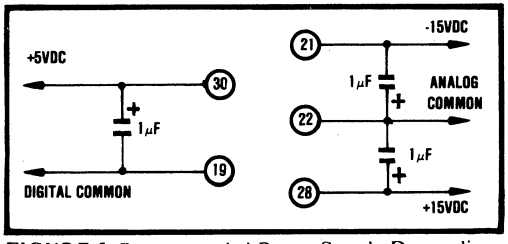


FIGURE 5. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 6 for circuit details.

TABLE II. ADC76 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (pin 1).

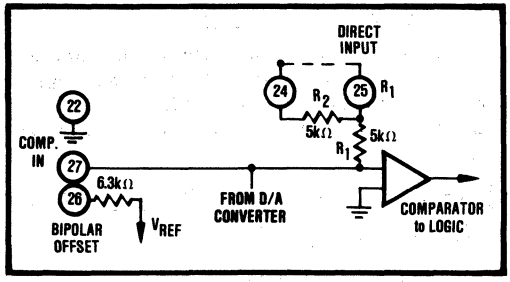


FIGURE 6. ADC76 Input Scaling Circuit.

OUTPUT DRIVE

Normally all ADC76 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

INPUT IMPEDANCE

The input signal to the ADC76 should be a low impedance, such as the output of an op amp to avoid any errors due to the relatively low input impedance of the ADC76.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the ADC76 as shown in Figure 7.

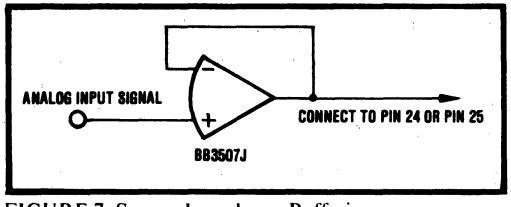


FIGURE 7. Source Impedance Buffering.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 8 and 9. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

Offset - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 8. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain - Connect the Gain adjust potentiometer as shown in Figure 9. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

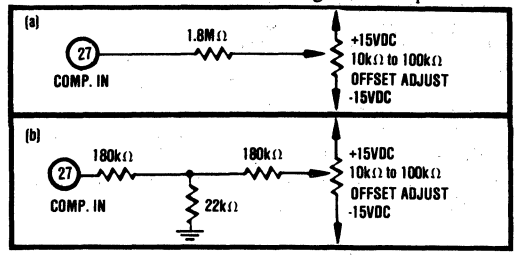


FIGURE 8. Two Methods of Connecting Optional Offset Adjust With a 0.4% of FSR Range of Adjustment.

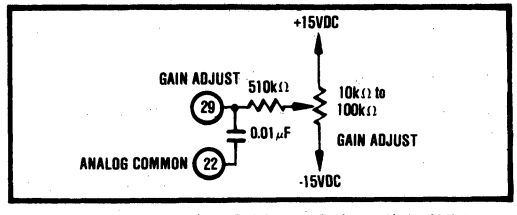


FIGURE 9. Connecting Optional Gain Adjust With a 0.6% Range of Adjustment.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to Convert Command, pin 31. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start on the first falling edge of the external clock following the completion of conversion. The clock out signal will remain as shown in Figure 2 even if an external clock is used. The external clock pulse must be a negative going pulse with a width between 100nsec and 200nsec as shown in Figure 2, and must be at a lower frequency than the internal clock. The circuit in Figure 10 shows a simple technique for generating a clock signal with the required duty cycle from an external clock with an arbitrary duty cycle. The external clock must operate at a lower frequency than the internal clock for proper operation. This should not present a problem since the frequency of the internal clock can be increased to any desired value by using the Clock Rate Control, pin 23. Figure 11 shows a conversion using a continuous external clock.

OPTIONAL CONVERSION TIME ADJUSTMENT

The ADC76 may be operated with faster conversion times for resolutions less than 14 bits by connecting the Clock Rate Control (pin 23) and the Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle and Clock Rate Control Connections for 12- to 16-Bit Resolutions.

Resolution (Bits)	16	15	14	13	12
Connect Pin 32* to	Open	Pin 16	Pin 15	Pin 14	Pin 13
Connect Pin 23 to	Pin 19	Pin 19	Pin 19	Pin 30	Pin 30
Typical Conversion Time	17μsec	16μsec	15μsec	10μsec	8μsec

*For resolutions less than 16 bits also connect a 2kΩ resistor from +5V to pin 32.

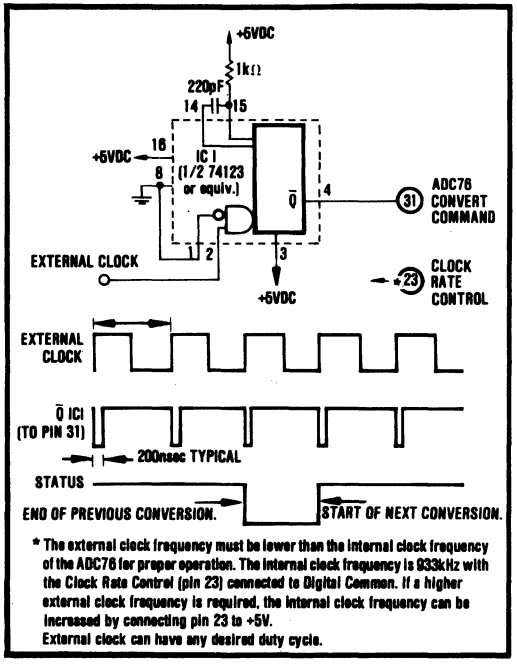


FIGURE 10. Continuous Conversion Using External Clock With Arbitrary Duty Cycle.

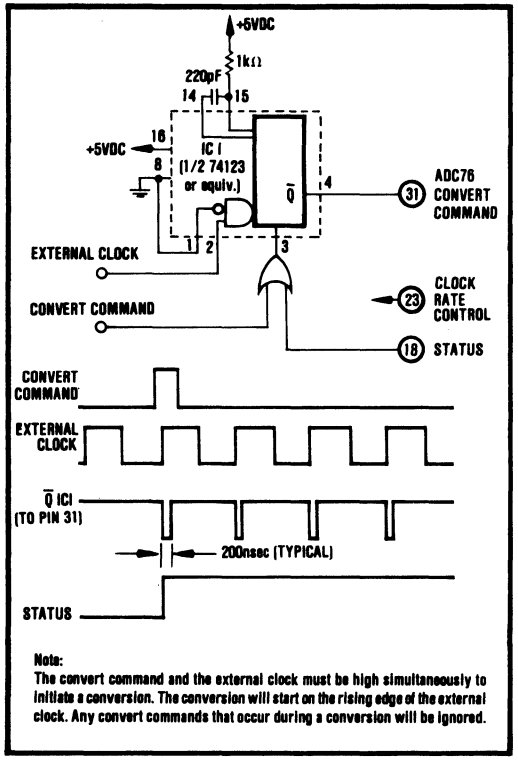


FIGURE 11. Conversion Initiated by Convert Command Using Continuous External Clock.

If a more precise adjustment of conversion time is desired than can be obtained by simply connecting the Clock Rate Control (pin 23) to Digital Common or +5V, as indicated in Table III, the Clock Rate Control may be connected to an external multiturn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figure 12. The typical conversion time versus the Clock Rate Control voltage is shown in Figure 13. The effect of

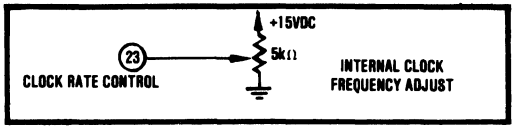


FIGURE 12. Clock Rate Control, Optional Fine Adjust.

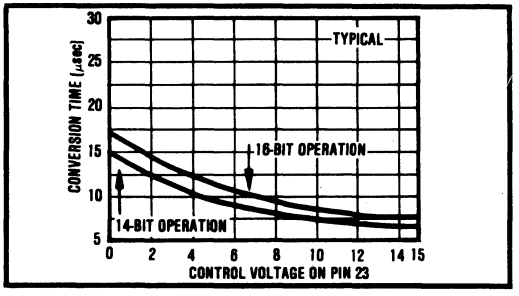


FIGURE 13. Conversion Time vs Clock Rate Control Voltage.

varying the conversion time and the resolution on Linearity Error and Differential Linearity Error is shown in Figure 4.

HEAT DISSIPATION

The ADC76 dissipates approximately 1.8 watts (typical) and the packages have a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above 70°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 14 for θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16 square inch (minimum) area, this technique will allow operation to +85°C.

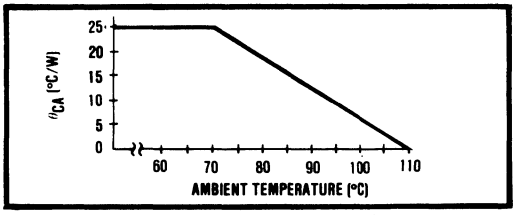


FIGURE 14. θ_{CA} Requirement Above 70°C.

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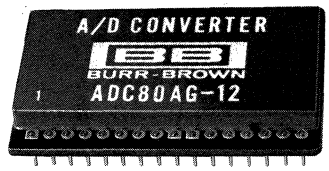


ADC80

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPACT DESIGN** - Self-contained with internal clock, comparator, and reference

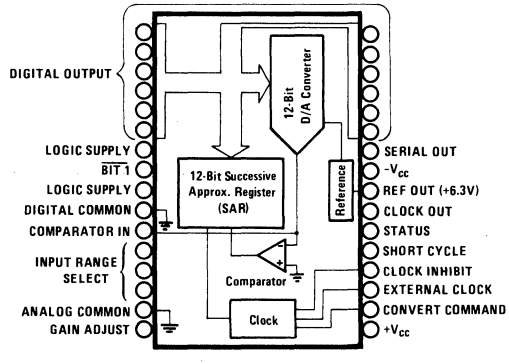
  32-pin ceramic package

- **FAST CONVERSION SPEEDS**
  Provide fast signal sampling rates
  12-bits - 25μsec, 10-bits - 21μsec
  Faster conversion speeds obtainable with "Short-Cycling" and optional external clock

- **LOW COST**

- **WIDE SUPPLY RANGE** - Will operate with ±10.8V to ±16V supplies (Z models)

FUNCTIONAL DIAGRAM



DESCRIPTION

The Model ADC80AG-10 and ADC80AG-12 are 10- and 12-bit successive approximation A/D converters. They utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a compact 32-pin ceramic package.

Complete with internal reference, the ADC80 offers versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V.

Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.0122% (±1/2LSB). The model ADC80 is specified for -25°C to +85°C operation.

The fast conversion speeds of 25μsec for 12-bit and 21μsec for 10-bit resolution make the ADC80 excellent for a wide range of applications where system throughput sampling rates from 40kHz to 47kHz are required. In addition, the ADC80 may be short cycled and an external clock may be used to obtain faster conversion speeds at lower resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Two power supply ranges are available: ±15V and ±12V (Z models). A +5V logic supply is also required.

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DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent QUANTIZATION ERROR of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including GAIN, OFFSET, LINEARITY, DIFFERENTIAL LINEARITY and POWER SUPPLY SENSITIVITY. Initial GAIN and OFFSET errors may be adjusted to zero. GAIN drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and OFFSET drift shifts the line left or right over the operating temperature range. LINEARITY error is unadjustable and is the most meaningful indicator of A/D converter accuracy. LINEARITY error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A DIFFERENTIAL LINEARITY error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC80 is also MONOTONIC, assuring that the output digital code either increases or remains the same for increasing analog input signals. A monotonic converter can have missing codes; therefore, Burr-Brown specifies no missing codes over a temperature range.

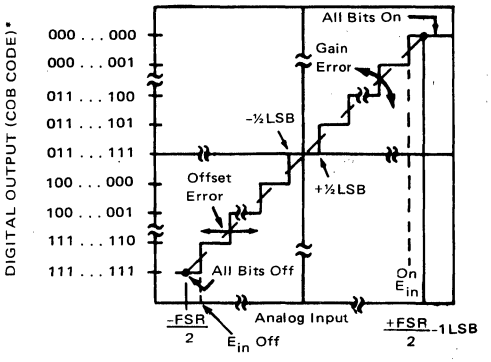


FIGURE 1. Input vs output for an ideal bipolar A/D converter.
*See Table I for digital code definitions.

TIMING CONSIDERATIONS

The timing diagram of the ADC80 (Figure 2) assumes an analog input such that the positive true digital word 10011000-1001 exists. The output will be complementary as shown in Figure 2 (011001110110 is the digital output).

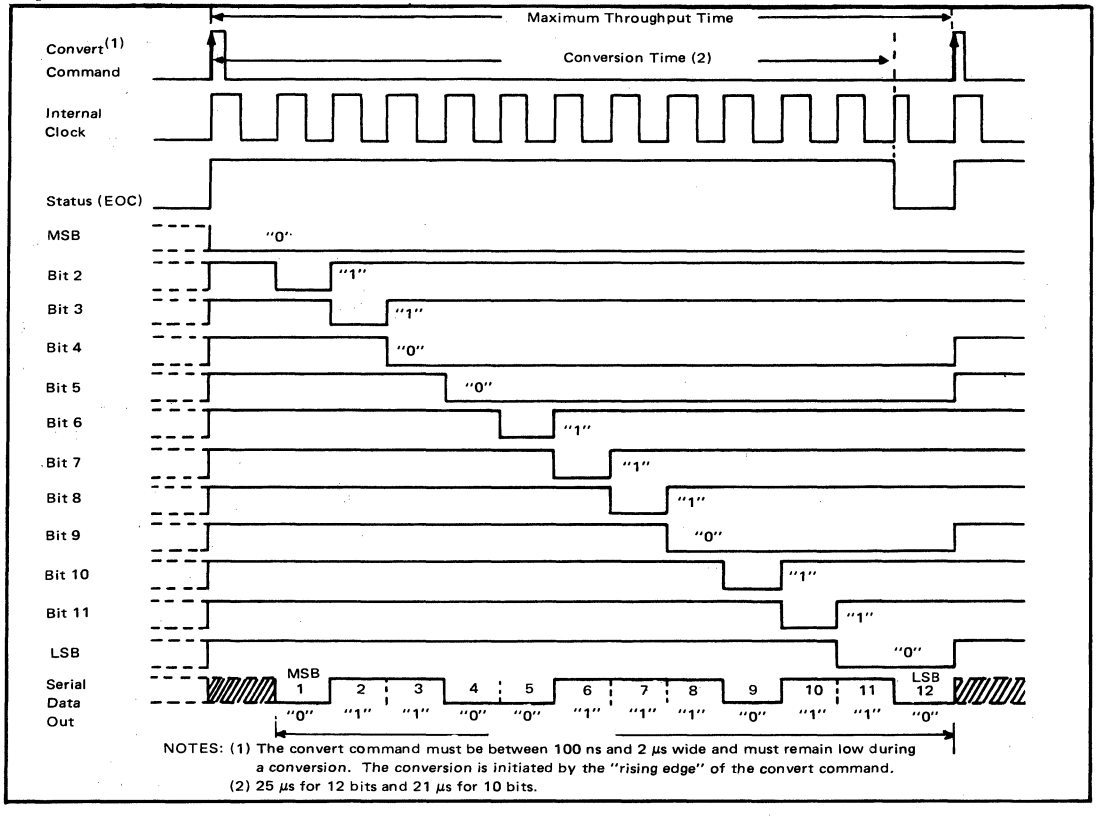


FIGURE 2. ADC80 Timing Diagram.

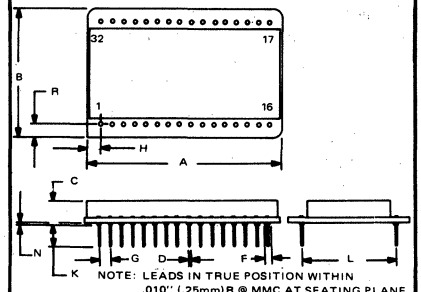
ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	ADC80AGZ-12 ADC80AG-12	ADC80AGZ-10 ADC80AG-10	Units
RESOLUTION	12	10	Bits
INPUT			
ANALOG INPUTS			
Voltage Ranges - Bipolar	±2.5, ±5, ±10		V
- Unipolar	0 to +5, 0 to +10		V
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5		kΩ
0 to +10V, ±5V	5		kΩ
±10V	10		kΩ
DIGITAL INPUTS[1]			
Convert Command	Positive Pulse 100ns Wide (min) 2μsec Wide (max).		
Logic Loading	1		TTL Load
External Clock	1		TTL Load
TRANSFER CHARACTERISTICS			
ERROR			
Gain Error[3]	±0.1		%
Offset Error[3] - Unipolar	±0.05		% of FSR[2]
- Bipolar	±0.1		% of FSR
Linearity Error (max)[4]	±0.012	±0.048	% of FSR
Inherent Quantization Error	±1/2		LSB
Differential Linearity Error	±1/2		LSB
No Missing Codes Temp. Range	0 to +70	0 to +70	°C
Power Supply Sensitivity			
±15V	±0.0030		% of FSR/%V,
+5V	±0.0015		% of FSR/%V,
DRIFT			
Specification Temperature Range	-25 to +85		°C
Total accuracy, bipolar (max)[8]	±23		ppm/°C
Gain, (max)	±30		ppm/°C
Offset - Unipolar	±3		ppm of FSR/°C
- Bipolar, (max)	±15		ppm of FSR/°C
Linearity, (max)	±3		ppm of FSR/°C
Monotonicity	GUARANTEED		
CONVERSION SPEED(max)[5]	25	21	μsec
OUTPUT			
DIGITAL DATA			
(all codes complementary)			
Parallel			
Output Codes[6] - Unipolar	CSB		
- Bipolar	COB, CTC		
Output Drive	2		TTL Loads
Serial Data Codes (NRZ)	CSB, COB		
Output Drive	2		TTL Loads
Status	Logic "1" during conversion		
Status Output Drive	2		TTL Loads
Internal Clock			
Clock Output Drive	2		TTL Loads
Frequency[7]	500		kHz
INTERNAL REF. VOLTAGE	6.3		V
Max. External Current (with no degradation of specifications)	200		μA
Tempco of Drift (max)	±20		ppm/°C
POWER REQUIREMENTS			
Rated Voltages	±15, +5		V
Z models	±12, +5		V
Range for Rated Accuracy	4.75 to 5.25 and ±14.0 to ±16.0		V
Z models	4.75 to 5.25 and ±10.8 to ±16.0		V
Supply Drain +15V or +12V	+20		mA
-15V or -12V	-20		mA
+5V	+70		mA
TEMPERATURE RANGE			
Specification	-25 to +85		°C
Operating (derated spec)	-55 to +100		°C
Storage	-55 to +125		°C

1. DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for inputs and for digital outputs. Logic "0" = +0.4V max and "1" = 2.4V min.
2. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
3. Adjustable to zero with external trimpots.
4. Error shown is the same as ±1/2 LSB max for resolution of A/D converter.
5. Conversion time with internal clock.
6. See Table I. CSB - Complementary Straight Binary.
   COB - Complementary Offset Binary.
   CTC - Complementary Two's Complementary.
7. For conversion speeds specified.
8. Includes drift due to linearity, gain, and offset drifts.

MECHANICAL



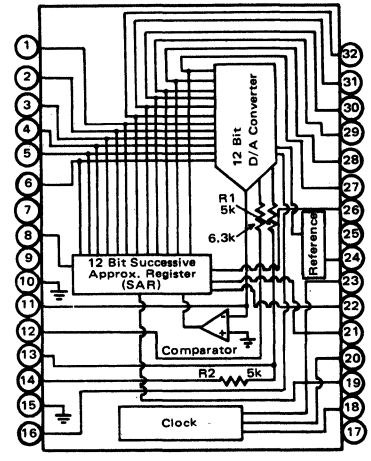
NOTE: LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

PINS: Pin material and plating composition conform to method 2003 (Solderability) of Mil-Std-883 (except paragraph 3.2).
CASE: Ceramic
MATING CONNECTOR: 2302MC - Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz).

Connection Diagram

TOP VIEW



PIN CONNECTIONS

1 Bit 6	32 Bit 7
2 Bit 5	31 Bit 8
3 Bit 4	30 Bit 9
4 Bit 3	29 Bit 10 (LSB-10 Bits)
5 Bit 2	28 Bit 11
6 Bit 1 (MSB)	27 Bit 12 (LSB-12 Bits)
7 +5V Analog Supply	26 Serial Out
8 Bit 1 (MSB)	25 -15V or -12V (Z Models)
9 +5V Digital Supply	24 Ref Out (+6.3V)
10 Digital Common	23 Clock Out
11 Comparator IN	22 Status
12 Bipolar Offset	21 Short Cycle
13 R1 10V Range	20 Clock Inhibit
14 R2 20V Range	19 External Clock
15 Analog Common	18 Convert Command
16 Gain Adjust	17 +15V or +12V (Z Models)

TYPICAL PERFORMANCE CURVES

FIGURE 3. Linearity error vs conversion time.

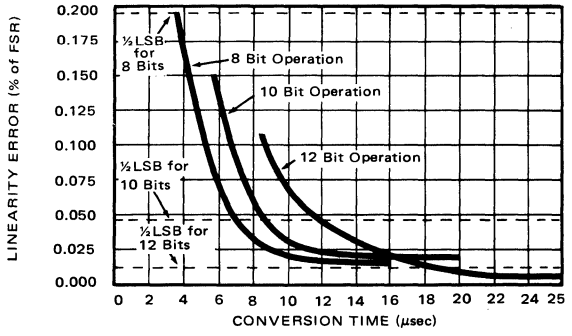


FIGURE 4. Differential linearity error vs conversion time.

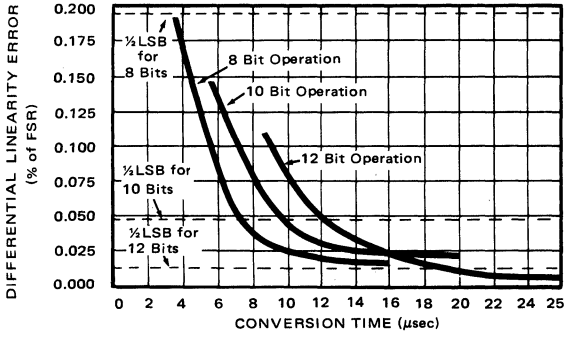


FIGURE 5. Gain drift error (% of FSR) vs temperature.

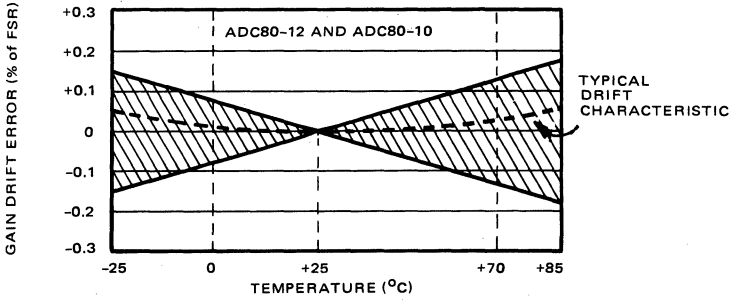
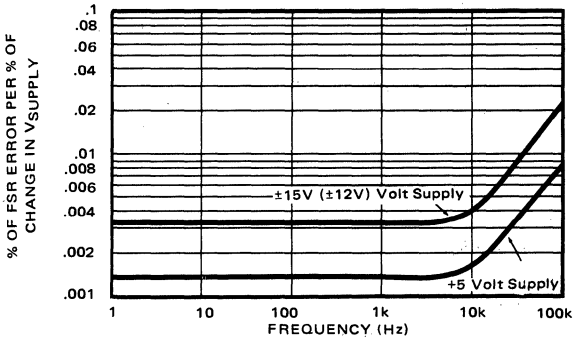


FIGURE 6. Power supply rejection vs power supply ripple frequency.



DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC80 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible ADC80 analog input signal range for 8, 10 and 12 bit resolutions.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line of the ADC80; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occuring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES					
Analog Input Voltage Range	Defined As:	±10V	+5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000...000***	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V
111...110	-Full Scale	-10V +½LSB	-5V +½LSB	-2.5V +½LSB	0 + ½LSB	0 +½LSB

* COB = Complementary Offset Binary
** CSB = Complementary Straight Binary
*CTC = Complementary Two's complement - obtained by using the complement of the most significant bit (MSB). MSB is available on pin 8.
*** Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

DISCUSSION OF SPECIFICATIONS

The ADC80 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors and conversion speed effects on accuracy. The ADC80 is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial GAIN and OFFSET errors are factory trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown on page 6-53.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\in g^2 + \in o^2 + \in e^2}$$

where $\in g$ = gain drift error (ppm/°C)
$\in o$ = offset drift error (ppm of FSR/°C)
$\in e$ = linearity error (ppm of FSR/°C)

For unipolar operation, the total RSS drift is ±30.3ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC80 are shown in Figures 3 and 4.

The ADC80 conversion speeds are specified for a maximum linearity error of ±½LSB and a differential linearity error of ±½LSB with the internal clock. Faster conversion speeds up to 23μs for 12 bits, 12μsec for 10 bits and 6μs for 8 bits are possible with an external clock (see page 6-54).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect the accuracy of the ADC80. The ADC80 power supply sensitivity is specified for ±0.003% of FSR/%Vs for ±15V (±12V) supplies and ±0.0015% of FSR/%Vs for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the ADC80. See layout precautions and power supply decoupling on page 6-53.

LAYOUT and OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC80 but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC80. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. Analog and digital +5 volt supplies are also not connected internally; they should be connected together at the unit as shown below in Figure 7 (Pins 7 and 9).

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC80. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

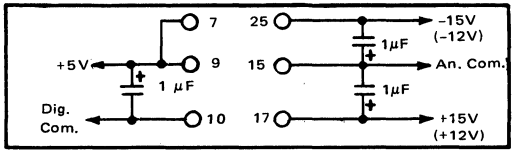


FIGURE 7. Recommended power supply decoupling.

INPUT SCALING

The ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

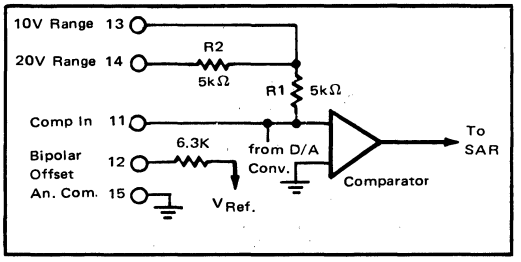


FIGURE 8. ADC80 Input scaling circuit.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

TABLE II. ADC80 Input scaling connections.

ADC80

Optional External Gain and Offset Adjustments

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC80 as shown in Figures 9 and 10. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10 kΩ to 100 kΩ. All resistors should be 20% carbon or better. Pin 16 (Gain Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the OFFSET potentiometer as shown in Figure 9. Sweep the input through the end point transition voltage that should cause an output transition to all ones.

Adjust the OFFSET potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

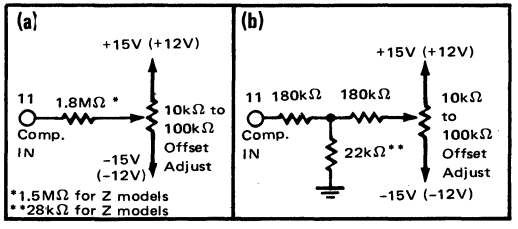


FIGURE 9. Two methods of connecting optional offset adjust with a 0.4% of FSR range of adjustment.

GAIN - Connect the GAIN adjust potentiometer as shown in Figure 10. Sweep the input through the end point transition voltage that should cause an output transition to all zeros.

Adjust the GAIN potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.
Table I details the transition voltage levels required.

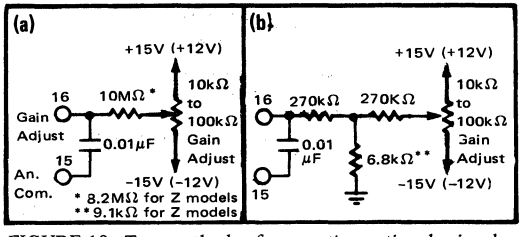


FIGURE 10. Two methods of connecting optional gain adjust with a 0.6% range of adjustment.

Clock Options

The ADC80 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with nothing more than an inexpensive quad 2-input NAND gate (7400) as shown in Figures 11 through 14.

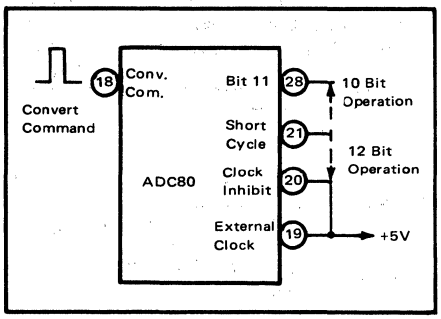


FIGURE 11. INTERNAL CLOCK – NORMAL OPERATING MODE. Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.

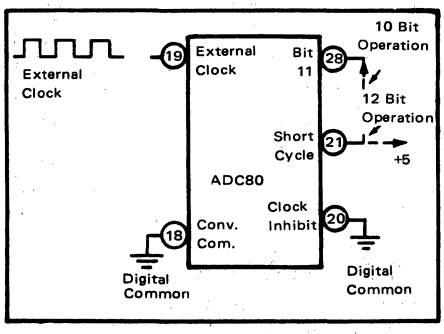


FIGURE 12. CONTINUOUS CONVERSION WITH EXTERNAL CLOCK. Conversion is initiated by 14th clock pulse. Clock runs continuously.

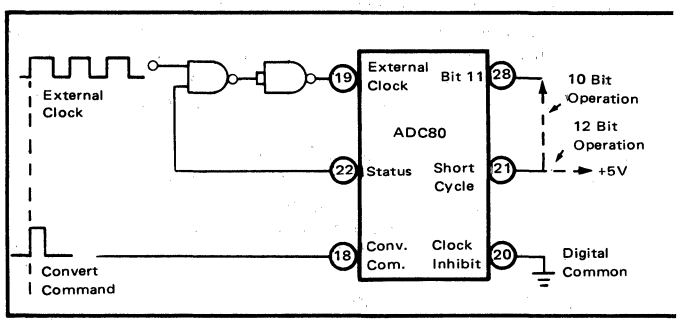


FIGURE 13. CONTINUOUS EXTERNAL CLOCK. Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.

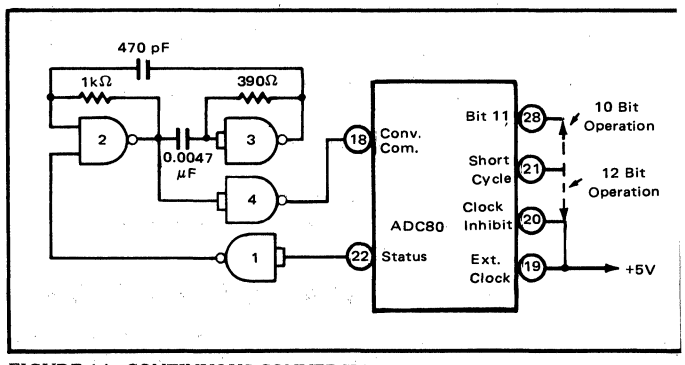


FIGURE 14. CONTINUOUS CONVERSION WITH INTERNAL CLOCK. Conversion is initiated by the 14th clock pulse. Clock runs continuously. The oscillator formed by gates 2 and 3 insures that the conversion process will start when logic power is first turned on.

Short Cycle Feature

The ADC80 may be operated at faster speeds for resolutions less than 10 or 12 bits, depending on the model selected, by connecting the short cycle pin, pin 21, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

RESOLUTION (BITS)	12	10	8
Connect Pin 21 to	Pin 9	Pin 28	Pin 30
Maximum Conversion Time(1)			
Internal Clock (μsec)	25	22	18
External Clock (μsec)	23	12	6
Maximum Nonlinearity At +25°C (% of FSR)	0.012(2)	0.048(3)	0.20(3)
NOTES: (1) Max conversion time to maintain ±½LSB Nonlinearity error. (2) 12 Bit Models only. (3) 10 or 12 Bit Models.			

TABLE III. Short cycle connections and resolutions for 8 to 12 bit resolutions - ADC80.

Output Drive

Normally all ADC80 logic outputs will drive 2 standard TTL loads; however if long digital lines must be driven, external logic buffers are recommended.

APPLICATIONS

LOW COST
DATA ACQUISITION
SYSTEM

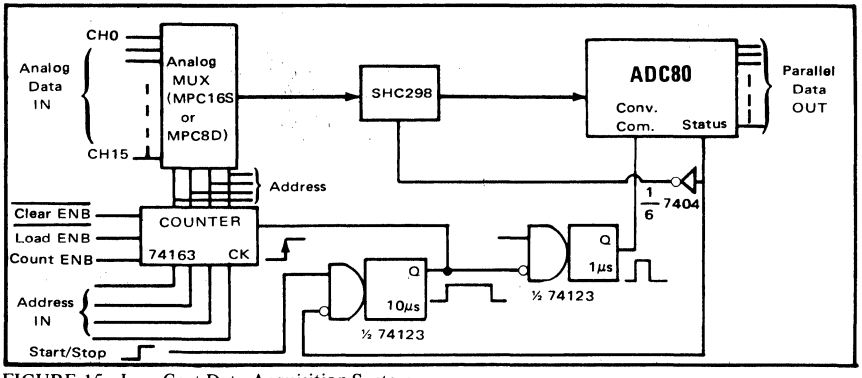


FIGURE 15. Low Cost Data Acquisition System.

ZERO DROOP SAMPLE/HOLD

A zero droop - infinite hold sample/hold can be constructed with the ADC80 with the circuit shown in Figure 16. A sample command will cause the relay to switch the analog input to the ADC80 input and also generate a convert command to the ADC80. The sample pulse width (T_A) should be greater than the combined switching and settling time of the relay and driver circuit and the ADC80 conversion time.

In the HOLD mode, the analog value can be held indefinitely with zero droop. The period of the first one-shot multivibrator must be equal to or greater than T_R, the switching time of the relay.

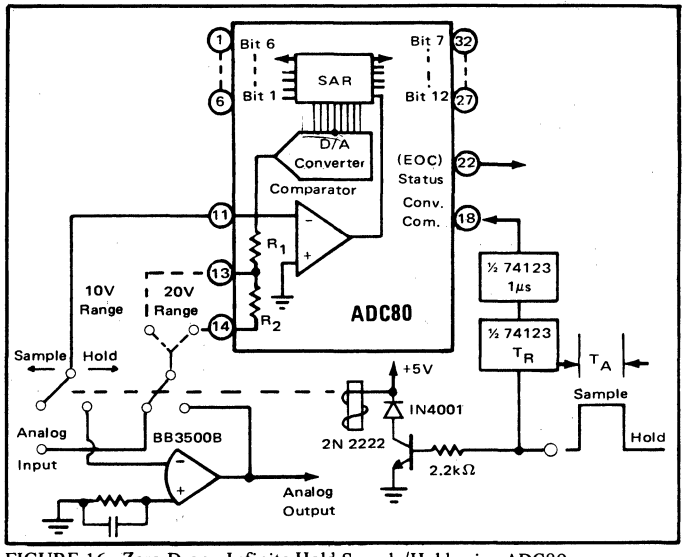


FIGURE 16. Zero Droop Infinite Hold Sample/Hold using ADC80 and a few external components.

ORDERING INFORMATION

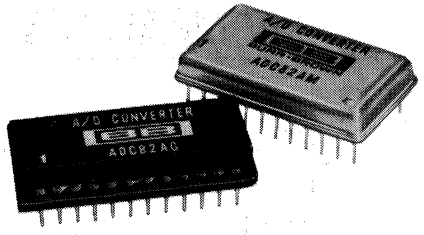
ADC80AG – XX

A/D Converter family
A = -25°C to +85°C
G = Ceramic Package

Blank - ±14.0V to ±16.0V supply range
Z - ±10.8V to ±16.0V Supply range

Resolution (No. of Bits)
10 = 10 Bits
12 = 12 Bits

BURR-BROWN®



ADC82

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **ABSOLUTE ACCURACY - No external gain or offset adjustments are required for 0 to +10V or ±10V signal ranges**
- **PRECISION - ±1/2LSB maximum nonlinearity error**
- **COMPACT DESIGN - 24-pin ceramic or metal dual-in-line package**
- **LOW COST - Ceramic packaged ADC82AG**
- **FAST CONVERSION SPEED - 2.8μsec, max Throughput sampling rates of over 300kHz Faster conversion speeds obtainable with optional external clock**
- **COMPLETELY SELF-CONTAINED - Internal clock, comparator, and reference**

DESCRIPTION

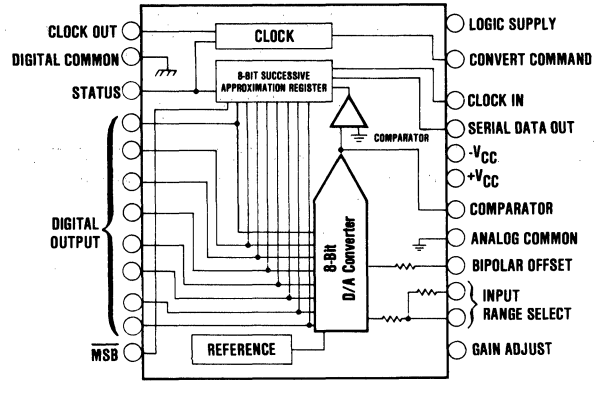
The model ADC82AG and ADC82AG are high-speed, 8-bit successive-approximation A/D converters designed for applications requiring system throughput sampling rates of over 300kHz. They utilize state-of-the-art IC and laser-trimmed thin-film components and are packaged in a 24-pin ceramic (ADC82AG) or metal (ADC82AM) package.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.25V, ±5V, ±10V, 0 to +5, 0 to +10V, or 0 to +20V.

No external adjustments are required to obtain initial absolute accuracies of better than ±1LSB for the 0 to +10V or ±10V signal ranges. Gain and offset errors may be externally trimmed to zero to obtain even greater accuracy.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Power supply voltages are ±15VDC and +5VDC.

FUNCTIONAL DIAGRAM



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PDS-351C

DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors, including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC82 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. A monotonic converter can have missing codes; therefore, Burr-Brown specifies no missing codes over a temperature range.

TIMING CONSIDERATIONS

The timing diagram of the ADC82 (see Figure 2) assumes an analog input such that the positive true digital word 10011000 exists. The output will be complementary as shown in Figure 2 (01100111 is the digital output).

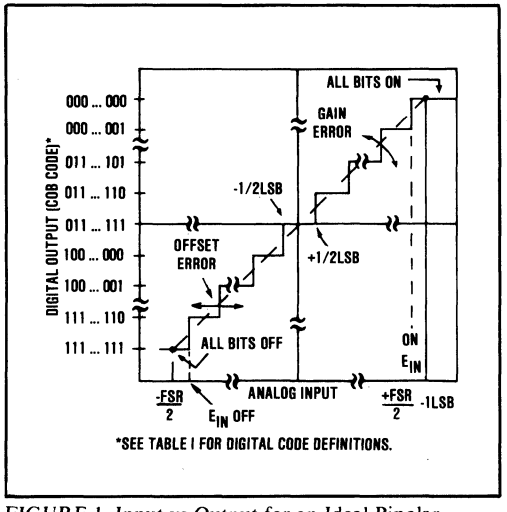


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

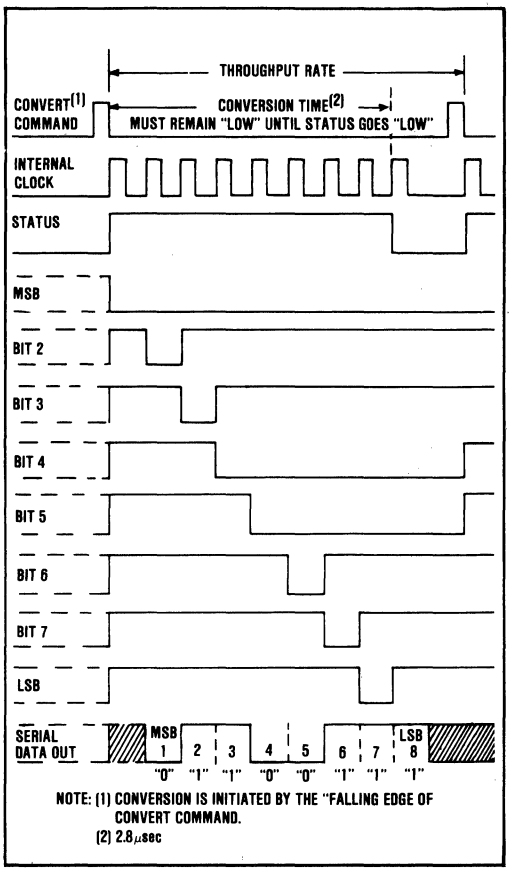


FIGURE 2. ADC82 Timing Diagram.

SPECIFICATIONS

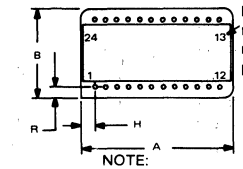
ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise noted.

MODEL	ADC82AG ADC82AM	UNITS
RESOLUTION	8	Bits
INPUT		
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5, ±5, ±10	V
Unipolar	0 to +5, 0 to +10, 0 to +20	V
Impedance (Direct Inputs)		
0 to +5V, ±2.5V	3.125	kΩ
0 to +10V, ±5V	6.25	kΩ
0 to +20V, ±10V	12.50	kΩ
DIGITAL INPUTS(1)		
Convert Command	Positive pulse 50nsec wide (min) trailing edge ("1" to "0") initiates conversion	
Logic Loading	1	TTL Load
External Clock	1	TTL Load
TRANSFER CHARACTERISTICS		
ERROR		
Total Accuracy Error, max	±1	LSB
Gain Error(2)	±0.1	%
Offser Error(2)		
Unipolar	±0.05	% of FSR(3)
Bipolar	±0.05	% of FSR
Linearity Error, max(4)	±0.2	% of FSR
Inherent Quantization Error	±1/2	LSB
Differential Linearity Error	±1/2	LSB
No Missing Codes Temp. Range	0 to 70	°C
Power Supply Sensitivity		
+15V	±0.02	% of FSR/%Vs
+5V and -15V	±0.006	% of FSR/%Vs
DRIFT		
Specification Temp. Range	-25 to +85	°C
Gain, max	±40	ppm/°C
Offset		
Unipolar	±20	ppm of FSR°C
Bipolar, max	±35	ppm of FSR°C
Linearity, max	±20	ppm of FSR/°C
Monotonicity	Guaranteed	
CONVERSION SPEED, max(5)	2.8	μsec
OUTPUT		
DIGITAL DATA(All codes complementary)		
Parallel		
Output Codes(6)		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	5	TTL Loads
Serial Data Codes (NRZ)	CSB, COB	
Output Drive	5	TTL Loads
Status	Logic "1" during conversion	
Status Output Drive	5	TTL Loads
Internal Clock		
Clock Output Drive	4	TTL Loads
Frequency(7)	2.85	MHz
POWER REQUIREMENTS		
Rated Voltages	±15, +5	VDC
Range for Rated Accuracy(8)	+4.75 to +5.25, ±14.5 to ±15.5	VDC
Supply Drain, +15VDC	+20	mA
-15VDC	-20	mA
+5VDC	+80	mA
TEMPERATURE RANGE		
Specification	-25 to +85	°C
Operating (derated specs)	-55 to +100	°C
Storage	-55 to +125	°C

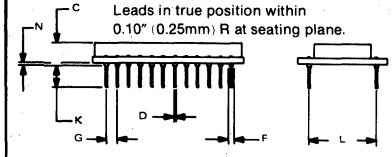
MECHANICAL

ADC82AG



Pin numbers shown for reference only. Numbers may not be marked on package.

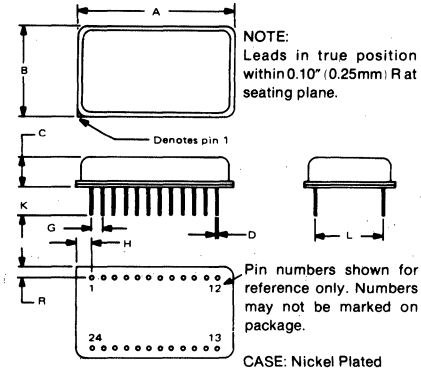
NOTE:
Leads in true position within 0.10" (0.25mm) R at seating plane.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	0.85	.105	2.16	2.67

CASE: Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 7 grams, (0.25 oz).

ADC82AM



NOTE:
Leads in true position within 0.10" (0.25mm) R at seating plane.

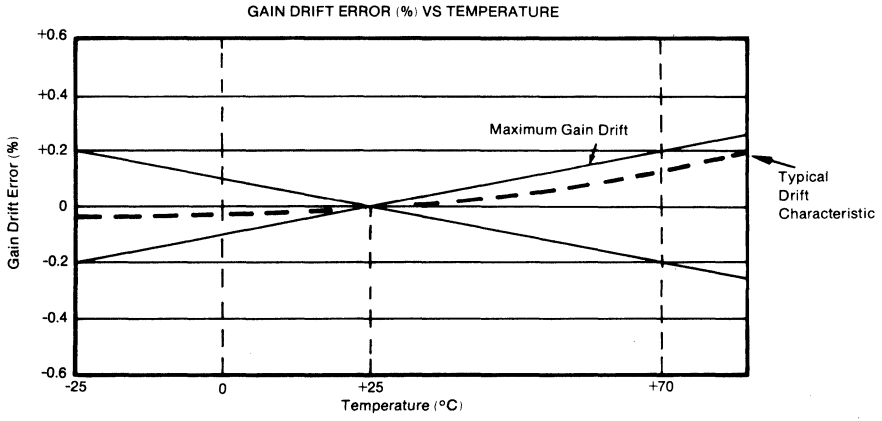
Pin numbers shown for reference only. Numbers may not be marked on package.

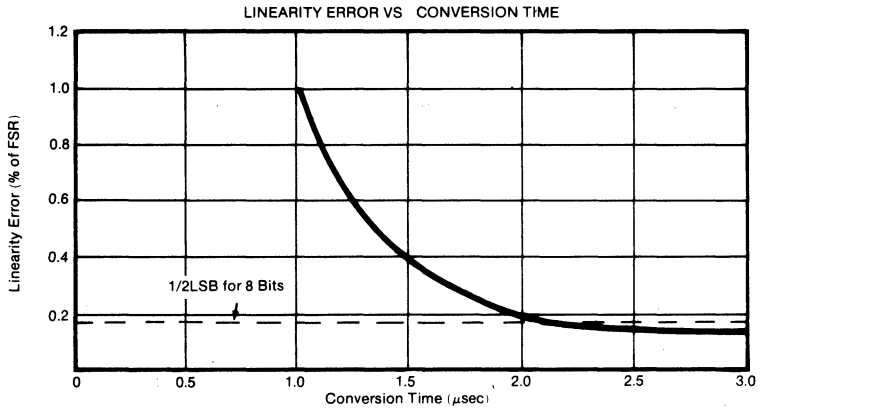
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

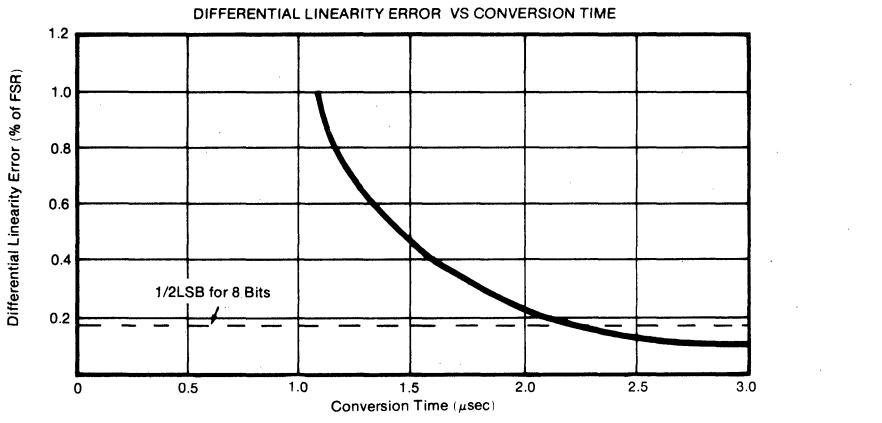
CASE: Nickel Plated
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 7 grams, (0.25 oz).

NOTES:
1. DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min.
2. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
3. Adjustable to zero with external trimpots.
4. Error shown is the same as ±1/2LSB max for resolution of A/D converter.
5. Conversion time with internal clock.
6. See Table I. CSB - Complementary Binary.
   COB - Complementary Offset Binary.
   CTC - Complementary Two's Complement.
7. For conversion speeds specified.
8. ±14.0V to ±16.0V for ±1-1/4LSB total accuracy error.

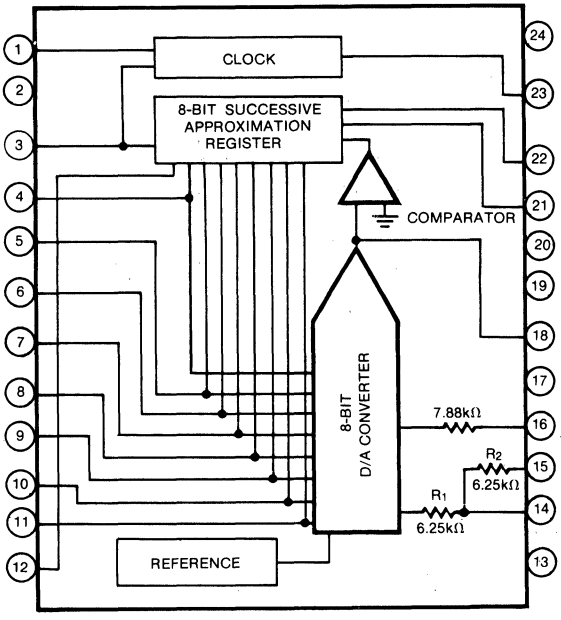
TYPICAL PERFORMANCE CURVES







CONNECTION DIAGRAM



PIN ASSIGNMENTS

1. Clock Out
2. Digital Common*
3. Status
4. Bit 8 (LSB)
5. Bit 7
6. Bit 6
7. Bit 5
8. Bit 4
9. Bit 3
10. Bit 2
11. Bit 1 (MSB)
12. $\overline{\text{Bit 1}}$ ($\overline{\text{MSB}}$)
13. Gain Adjust
14. R_1 (10V Range)
15. R_2 (20V Range)
16. Bipolar Offset
17. Analog Common
18. Comparator Input
19. +15
20. -15V
21. Serial Out
22. Clock In
23. Convert Command
24. +5V

*Internally connected to case on ADC82AM.

DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC82 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible ADC82 analog input signal range.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line of the ADC82; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTD code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Analog Input Voltage Ranges	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**	CSB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$ n = 8	$\frac{20V}{2^n}$ 78.13mV	$\frac{10V}{2^n}$ 39.06mV	$\frac{5V}{2^n}$ 19.53mV	$\frac{10V}{2^n}$ 39.06mV	$\frac{5V}{2^n}$ 19.53mV	$\frac{20V}{2^n}$ 78.13mV
Transition Values MSB LSB							
000 ... 00Ø***	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5 -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 11Ø	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

* COB = Complementary Offset Binary
**CSB = Complementary Straight Binary
*CTC = Complementary Two's complement - obtained by using the complement of the most-significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is avaliable on pin-12.
***Ø is the Transition Bit. Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC82 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. The ADC82 is factory trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial gain and offset errors are factory trimmed to ±0.05% of FSR at +25°C for both the 0 to +10 and ±10V ranges. No external adjustment is required to obtain initial absolute accuracies of ±1LSB. When using one of the other input signal ranges or when even greater initial accuracy is desired these errors may be trimmed to zero by connecting external potentiometers as shown in Figures 9 and 10.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\epsilon_g^2 + \epsilon_o^2 + \epsilon_e^2}$$

Where ϵ_g = gain drift error (ppm/°C)
ϵ_o = offset drift error (ppm of FSR/°C)
ϵ_e = Linearity error (ppm of FSR/°C)

For unipolar operation, the total RSS drift is ±49.0ppm/°C and for bipolar operation, the total RSS drift is ±56.8 ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC82 are shown in Typical Performance Curves.

The ADC82 conversion speeds are specified for a maximum linearity error of ±1/2LSB and a differential linearity error of ±1/2LSB with the internal clock. Faster conversion speeds are possible with an external clock (see Figures 6 and 7.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect the accuracy of the ADC82. The ADC82 power supply sensitivity is specified for ±0.006% of FSR/%V_S for -15V and +5V supplies and ±0.02% of FSR/%V_S for +15V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the ADC82. See layout precautions and power supply decoupling below.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC82 but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC82. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 3 to obtain noise free operation. These capacitors should be located close to the ADC82. 1μF electrolytic type capacitors should by bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

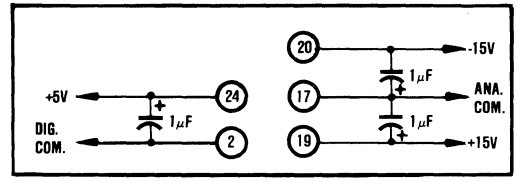


FIGURE 3. Recommended Power Supply Decoupling.

INPUT SCALING

The ADC82 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 4 for circuit details.

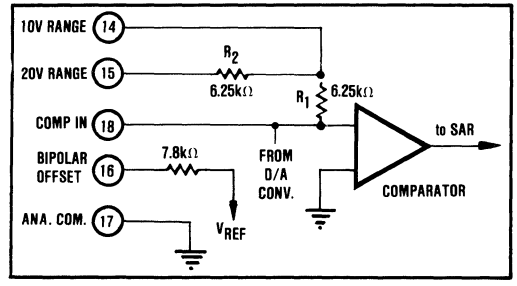


FIGURE 4. ADC82 Input Scaling Circuit.

TABLE II. ADC82 Input Scaling Connection.

Input Signal Range	Output Code	Connect Pin 16 To Pin	Connect Pin 15 To	Connect Input Signal To
±10V	COB or CTC	18	Input Signal	15
±5V	COB or CTC	18	Open	14
±2.5V	COB or CTC	18	Pin 18	14
0 to +5V	CSB	17	Pin 18	14
0 to +10V	CSB	17	Open	14
0 to +20V	CSB	17	Input Signal	15

CLOCK OPTIONS

The ADC82 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with nothing more than an inexpensive quad 2-input NAND Gate (7400) as shown in Figure 5 through 8.

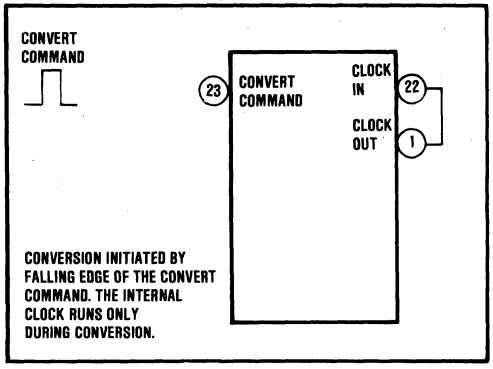


FIGURE 5. Internal Clock-Normal Operating Mode.

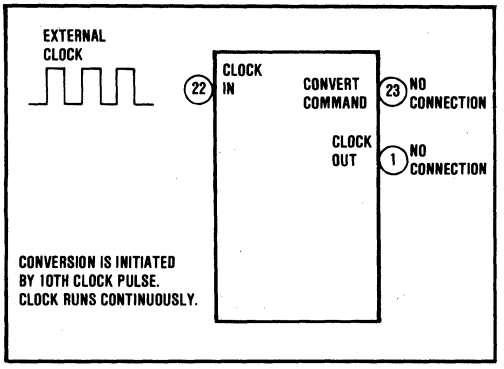


FIGURE 6. Continuous Conversion with External Clock.

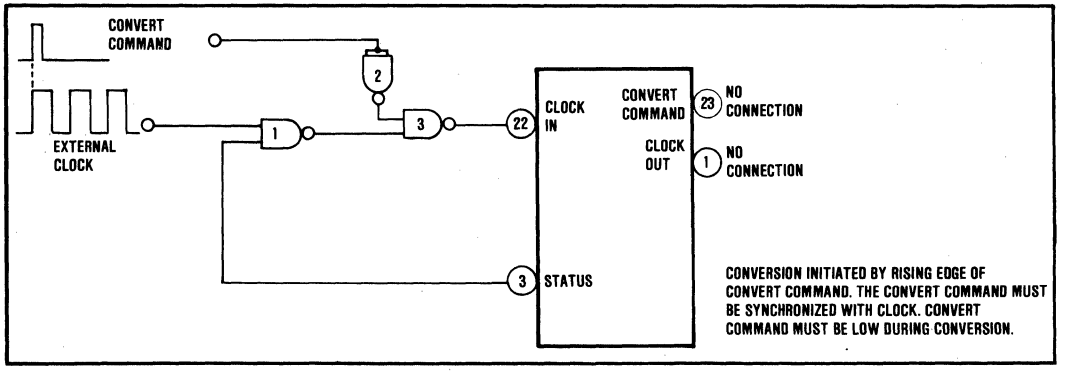


FIGURE 7. Continuous External Clock.

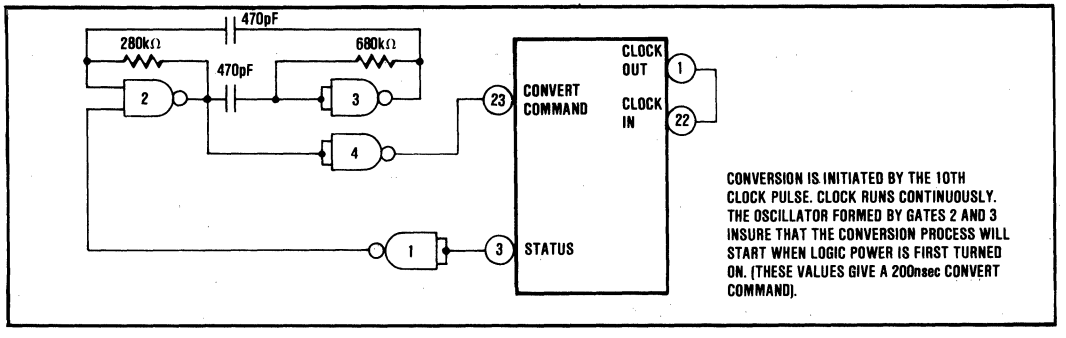


FIGURE 8. Continuous Conversion with Internal Clock.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC82 as shown in Figures 9 and 10. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 13 (Gain Adjust) may be left open if no external adjustment is required.

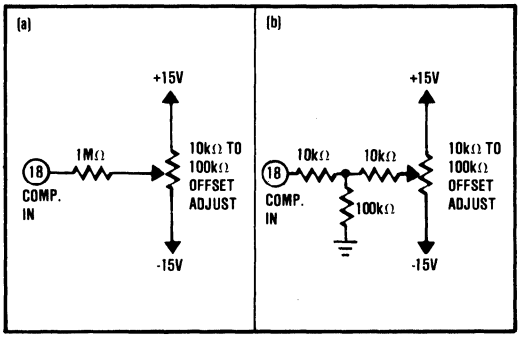


FIGURE 9. Two methods of Connecting Optional Offset Adjust with a ±1.0% of FSR Range of Adjustment.

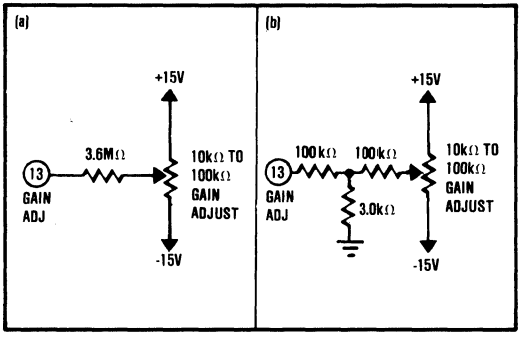


FIGURE 10. Two Methods of Connecting Optional Gain Adjust with a ±10% Range of Adjustment.

ADJUSTMENT PROCEDURE

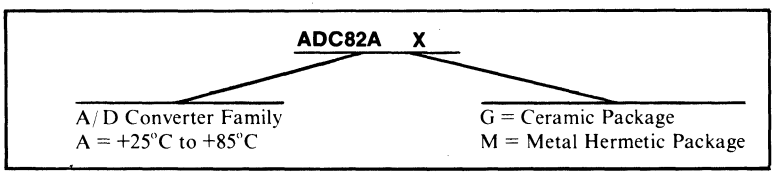
Offset - Connect the Offset potentiometer as shown in Figure 9. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

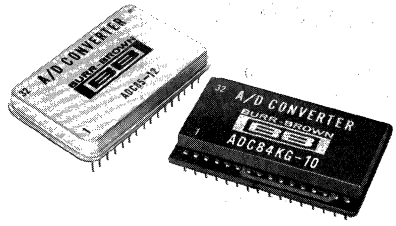
Gain - Connect the Gain adjust potentiometer as shown in Figure 10. Sweep the input through the end point transition voltage that should cause output transitions to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

ORDERING INFORMATION



BURR-BROWN®



ADC84
ADC85

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPACT DESIGN - Self-contained with internal clock, comparator, reference, and input buffer amplifier 32-pin ceramic or hermetic metal package**
- **FAST CONVERSION SPEEDS**
  Provide Fast Signal Sampling Rates
  12-bits - 10μsec, 10-bits - 6μsec
  Faster conversion speeds obtainable with "Short-Cycling" and adjustable clock rate
- **LOW COST - ADC84KG-12**

DESCRIPTION

The ADC84 and ADC85 families of 10- and 12-bit analog-to-digital converters utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a compact 32-pin dual-in-line packages.

Complete with internal reference and input buffer amplifier, they offer versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V. Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.012% (±1/2LSB).

The fast conversion speeds of 10μsec for 12-bit and 6μsec for 10-bit resolution make these ADC's excellent for a wide range of applications where system throughput sampling rates from 100kHz to 120kHz are required. In addition, they may be short cycled and the clock rate control may be used to obtain faster conversion speeds at low resolutions.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Power supply voltages are ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-355C

DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC84 and ADC85 are also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown also guarantees that these converters will have no missing codes over a specified temperture range.

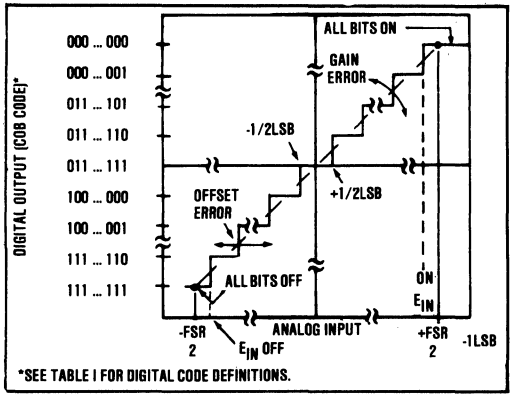


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram of the ADC's (see Figure 2) assumes an analog input such that the positive true digital word 100110001001 exists. The output will be complementary as shown in Figure 2 (011001110110 is the digital output).

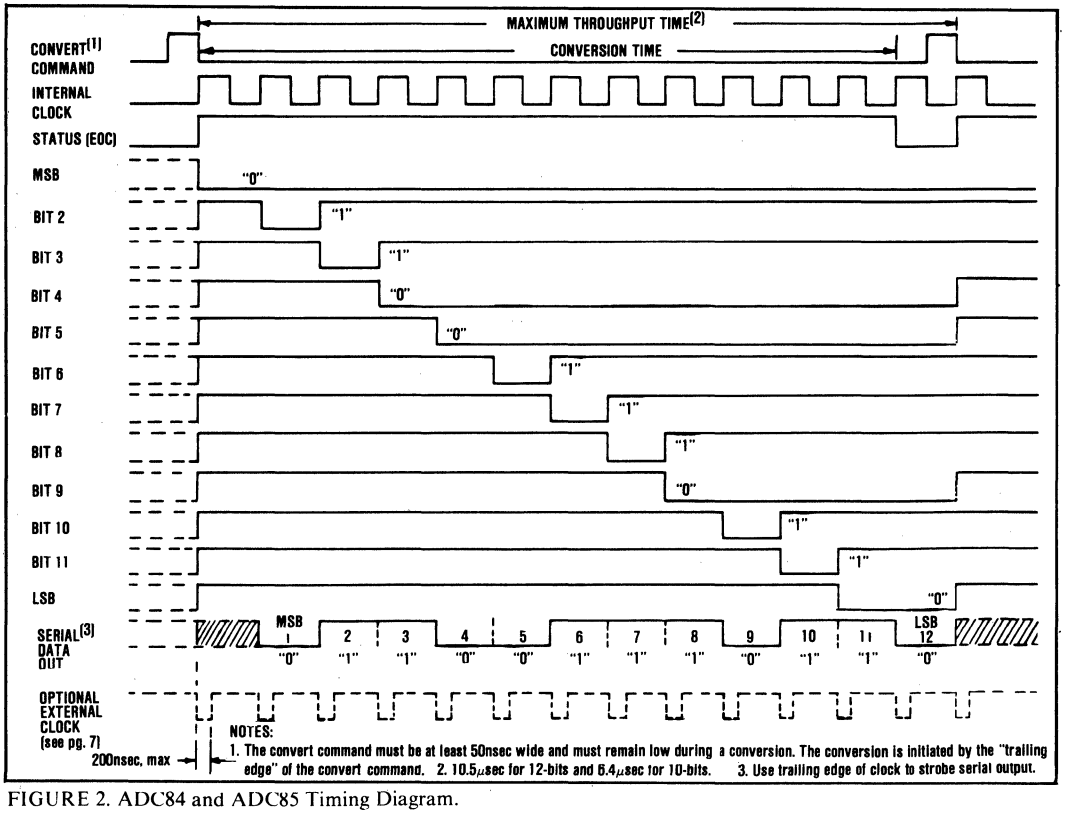


FIGURE 2. ADC84 and ADC85 Timing Diagram.

SPECIFICATIONS

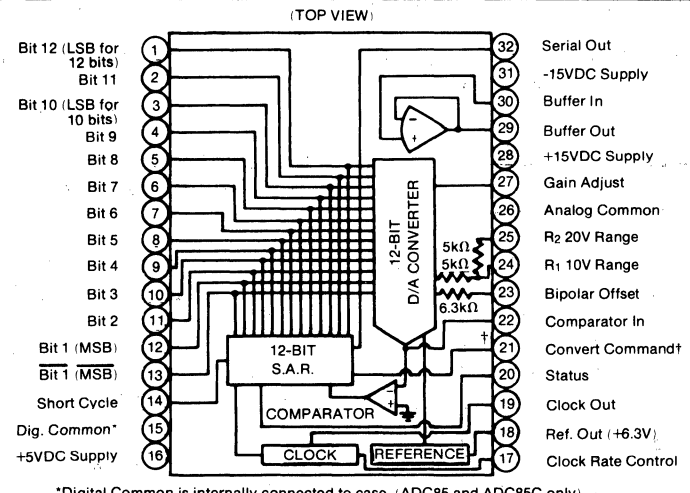
ELECTRICAL

Typical at +25°C and rated power supplies otherwise noted.

MODEL	ADC85		ADC85C		ADC84KG		UNITS
RESOLUTION	**10**	**12**	**10**	**12**	**10**	**12**	**BITS**
INPUT							
ANALOG INPUTS							
Voltages Ranges							
Bipolar	±2.5, ±5, ±10						V
Unipolar	0 to +5, 0 to +10						V
Impedance (Direct Input)							
0 to +5V, ±2.5V	2.5						kΩ
0 to +10V, ±5V	5						kΩ
±10V	10						kΩ
Buffer Amplifier							
Impedance, min	100						MΩ
Bias Current	50						nA
Settling Time							
to 0.01% for 20V step(1)	2						µsec
DIGITAL INPUTS(2)							
Convert Command	Positive pulse 50nsec wide, min. Trailing Edge ("1" to "0" initiates conversion)						
Logic Loading	1						TTL Load
External Clock	See External Clock paragraph						
TRANSFER CHARACTERISTICS							
ERROR							%
Gain Error	±0.1 (Adjustable to zero)						
Offset Error	Adjustable to zero						% of FSR(3)
Unipolar	±0.05						% of FSR
Bipolar	±0.1						% of FSR
Linearity Error, max(4)	±0.048	±0.012	±0.048	±0.012	±0.048	±0.012	LSB
Inherent Quantization Error	±1/2						LSB
Differential Linearity Error	±1/2						LSB
No Missing Codes	-25 to +85	0 to +70	0 to +70	0 to +70	0 to +70	0 to +70	°C
Power Supply Sensitivity							
±15VDC	±0.004						% of FSR/%Vs
+5VDC	±0.001						% of FSR/%Vs
DRIFT							
Specification Temperature Range	-25 to +85		0 to +70		0 to +70		°C
Gain, max	±20	±15	±40	±25		±30	ppm/°C
Offset							
Unipolar	±3	±3	±3	±3	±3	±3	ppm of FSR/°C
Bipolar	±10	±7	±20	±12	±15	±15	ppm of FSR/°C
Linearity, max	±3	±2	±3	±3	±3	±3	ppm of FSR/°C
Monotonicity	Guaranteed						
CONVERSION SPEED (max)(5)(6)	6	10	6	10	6	10	µsec
OUTPUT							
DIGITAL DATA							
All codes complementary							
Parallel							
Output Codes(7)							
Unipolar	CSB						
Bipolar	COB, CTC						
Output Drive	2						TTL Loads
Serial Data Codes (NRZ)	CSB, COB						
Output Drive	2						TTL Loads
Status	Logic "1" during conversion						
Status Output Drive	2						TTL Loads
Internal Clock							
Clock Output Drive	2						TTL Loads
Frequency(6)	1.9	1.35	1.9	1.35	1.9	1.35	MHz
INTERNAL REF. VOLTAGE	6.3						V
Max External Current With no degradation of Specifications	200						µA
Tempco of Drift, max	±5	±5	±10	±10	±20	±20	ppm/°C
POWER REQUIREMENTS							
Rated Voltages	±15, +5						V
Range for Rated Accuracy	4.75 to 5.25 and ±14.5 to ±15.5						V
Supply Drain +15VDC	+45				+45		mA
-15VDC	-35				-35		mA
+5VDC	+120				+70		mA
TEMPERATURE RANGE							
Specification	-25 to +85		0 to +70		0 to +70		°C
Operating (derated specs)	-55 to +85 (110°C case Temp.						°C
Storage	-55 to +125		-55 to +125		-55 to +125		°C
PACKAGE (see Mechanical Specifications)	Metal (Hermetic)				Ceramic		

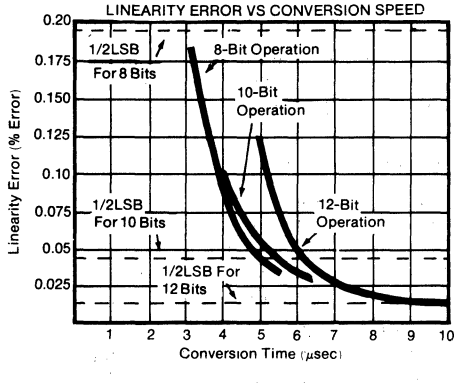
NOTES:
1. This settling time adds to conversion speed when buffer is connected to input.
2. DTL/TTL compatible; i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V, min for inputs. For digital outputs, Logic "0" = +0.4V max, Logic "1" = 2.4V, min.
3. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
4. Error shown is the same as ±1/2LSB max linearity error in % of FSR.
5. Conversion time may be shortened with "short cycle" set for lower resolution.
6. Internal Clock is externally adjustable.
7. See Table II. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.

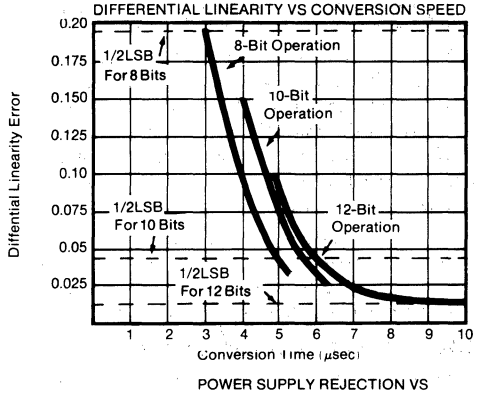
CONNECTION DIAGRAM

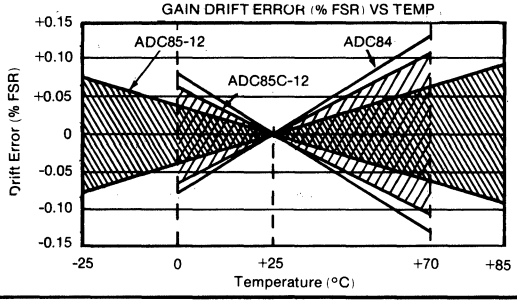


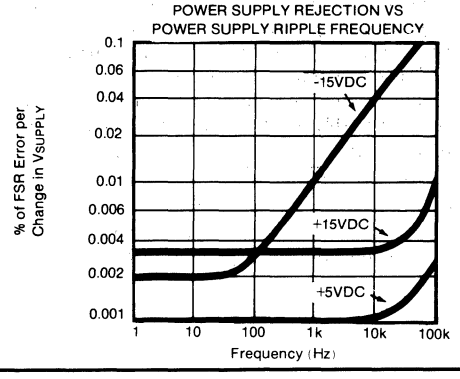
*Digital Common is internally connected to case. (ADC85 and ADC85C only)
† If an external clock is used, connect the clock to Pin-21 (conv. command). (See Figure 2 and External Clock paragraph).

TYPICAL PERFORMANCE CURVES









DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC84 and ADC85 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input singal ranges.

Table I describes the LSB, transition values and code definitions for each possible analog input signal range for 8-, 10-, and 12-bit resolutions.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES					
Analog Input Voltage Ranges	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB* or CTC***	COB* or CTC***	COB* or CTC***	CSB**	CSB**
One Least Significant Bit (LSB)	FSR 2^n	20V 2^n	10V 2^n	5V 2^n	10V 2^n	5V 2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 ... 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5 -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 ... 111	MIL Scale	0	0	0	+5V	+2.5V
111 ... 110	-Full Scale	-10V +1/2LSB	-5V + 1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 + 1/2LSB

*COB = Complementary Offset Binary
**CSB = Complementary Straight Binary
***CTC = Complementary Two's complement - obtained by using the complement of the most-significant bit (MSB). MSB is available on pin-13.
****Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC84 and ADC85 are specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors and conversion speed effects on accuracy. These ADC's are factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown on next page.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst-case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1σ errors as follows:

$$RSS = \sqrt{\epsilon g^2 + \epsilon o^2 + \epsilon e^2}$$

where ϵg = gain drift error (ppm/°C)
ϵo = offset drift error (ppm of FSR/°C)
ϵe = linearity error (ppm of FSR/°C)

For the ADC85-12 operating in the unipolar mode the total RSS drift is ±15.42ppm/°C and for bipolar operation the total RSS drift is ±16.7ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC84 and ADC85 are shown in Typical Performance Curves.

The conversion speeds are specified for a maximum linearity error of ±1/2LSB with the internal clock. Faster conversion speeds are possible (see Clock Rate Control Alternate Connections).

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The ADC84 and the ADC85 power supply sensitivity is specified for ±0.003% of FSR/%V_S for ±15VDC supplies and ±0.0015% of FSR/%V_S for +5VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with these ADC's. See Layout Precautions and Power Supply Decoupling on next page.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC84 and ADC85, but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 3 to obtain noise free operation. These capacitors should be located close to the ADC. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

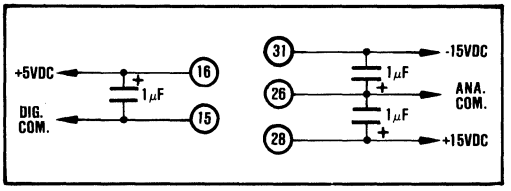


FIGURE 3. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 4 for circuit details.

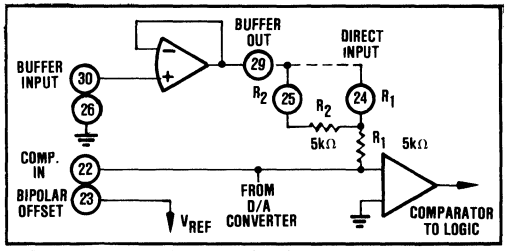


FIGURE 4. Input Scaling Circuit - ADC84 and ADC85.

TABLE II. ADC84 and ADC85 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Buffered Input* Connect Pin 29 To Pin	For Direct Input (see note) Connect Input Signal To Pin
			Input		
±10V	COB or CTC	22	Signal**	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0 to +5V	CSB	26	Pin 22	24	24
0 to +10V	CSB	26	Open	24	24

*Connect to Pin 29 or input signal as shown in next two columns.
**The input signal is connected to Pin 30 if the buffer amplifier is used.
NOTE: If the buffer amplifier is not used, the input Pin 30 must be grounde (Pin 26).

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 5 and 6. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 27 (Gain Adjust) and Pin 22 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

Offset - Connect the Offset potentiometer as shown in Figure 5. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

Gain - Connect the Gain adjust potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition voltage to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

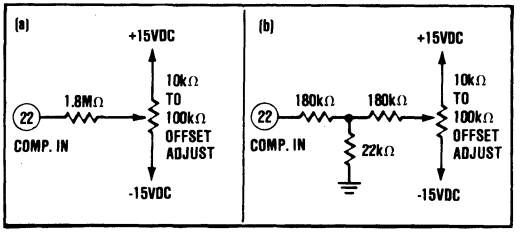


FIGURE 5. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range of Adjustment.

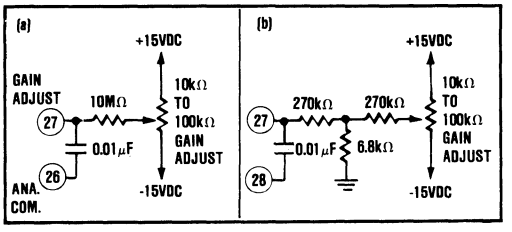


FIGURE 6. Two Methods of Connecting Optional Gain Adjust with a 0.6% Range of Adjustment.

CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the Clock Rate is desired for faster conversion speeds, the Clock Rate Control may be connected to an external multiturn trim potentiometer with TCR of ±100ppm/°C or less as shown in Figures 7A and 7B. If the potentiometer is connected to -15VDC, conversion time can be increased as shown in Figure 8. If these adjustments are used, delete the connections shown in Table III for pin 17. See Typical Performance Curves for nonlinearity error vs. clock frequency, and Figure 8 for the effect of the control voltage on clock speed.

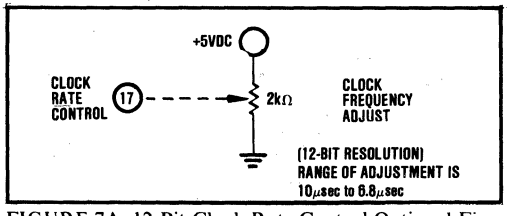


FIGURE 7A. 12-Bit Clock Rate Control Optional Fine Adjust.

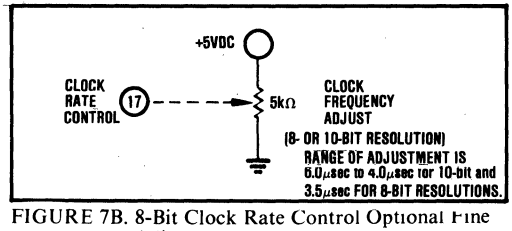


FIGURE 7B. 8-Bit Clock Rate Control Optional Fine Adjust.

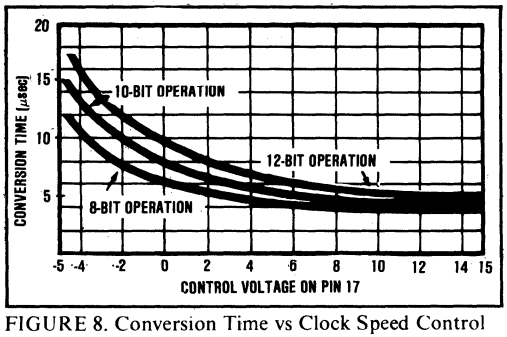


FIGURE 8. Conversion Time vs Clock Speed Control Voltage.

EXTERNAL CLOCK

If an external clock is used, connect the external clock to convert command, pin 21. The convert command shown in Figure 2 is not used. After each conversion is completed, a new conversion cycle will automatically start of the first falling edge of the external clock following the completion of conversion. The clock-out signal will remain as shown in Figure 2 even if an external clock is used. The external clock pulse must be a negative going pulse with a width between 100nsec and 200nsec as shown in Figure 2.

ADDITIONAL CONNECTIONS REQUIRED

The ADC84 and ADC85 may be operated at faster speeds for resolutions less than 12 or 10 bits depending on the model selected, by connecting the Short Cycle input, pin-14, as shown in Table III. Conversion speeds, linearity and resolutions are shown for reference.

TABLE III. Short Cycle Connections and Specifications for 8- to 12-Bit Resolution.

RESOLUTION (Bits)	12	10	8
Connect Pin 17 to (1)	Pin 15	Pin 16	Pin 28
Connect Pin 14 to	Pin 16	Pin 2	Pin 4
Maximum Conversion Speed (μsec)(2)	10	6	4
Manimum Nonlinearity at 25°C (% of FSR)	0.012(3)	0.048(4)	0.20(4)

NOTES:
1. Connect only if clock rate control is not used.
2. Max. conversion speeds to maintain ±1/2LSB nonlinearity error.
3. 12-bit models only.
4. 10- or 12-bit models.

OUTPUT DRIVE

Normally all ADC84 and ADC85 logic outputs will drive 2 standard TTL-loads; however, if long digital lines must be driven, external logic buffers are recommended.

HEAT DISSIPATION

The ADC84 and ADC85 dissipate approximately 1.2W and the packages have a case-to-ambient thermal resistance (Θ_{CA} should be lowered by a heat-sink or by forced air over the surface of the package). See Figure 9 for Θ_{CA} requirement above 70°C. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the case can be achieved using a silicone heat-sink compound. On a 0.062-inch thick PC card with 16 square-inch minimum area, this technique will allow operation to 85°C.

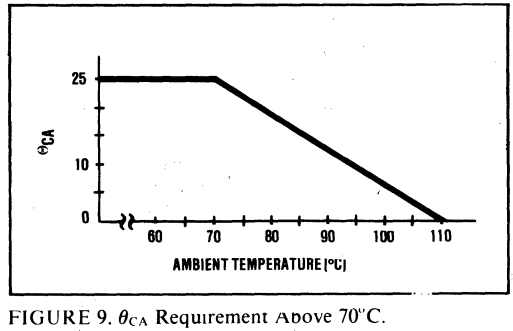


FIGURE 9. θ_{CA} Requirement Above 70°C.

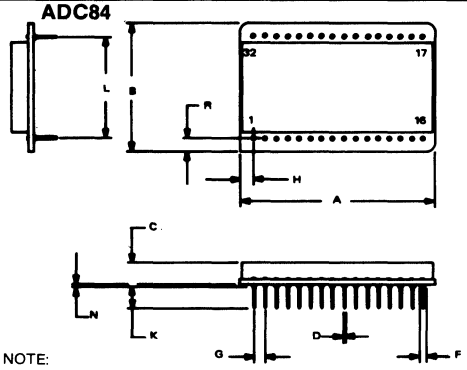
HIGH RELIABILITY A/D CONVERTERS

Each of the ADC85 models are available screened to the requirements of the Burr-Brown Q-Program, which consists of a sequence of thermal and mechanical stress procedures, plus a verification of package hermeticity. The diagram below illustrates the screening sequence which is applied to 100% of the Q-Screened A/D converters.

High Temp. Storage (MIL-STD-883)	Temperature Cycling (MIL-STD-883)	Hermeticity Gross Leak (MIL-STD-883)	Hermiticity Fine Leak (MIL-STD-883)	Burn-In (MIL-STD-883)	Centrifuge (MIL-STD-883)
Method 1008 Condition B +125°C 24 Hours	Method 1010 Condition B -55 to +25°C 10 Cycles	Method 1014 Condition C Step 1 Fluorocarbon	Method 1014 Condition A Helium 5 x 10^{-7}cc/sec	Method 1015 Condition D 168 Hours +70°C (ADC85C) +85°C (ADC85)	Method 2001 2,000 G Y_1 Axis

MECHANICAL

ADC84

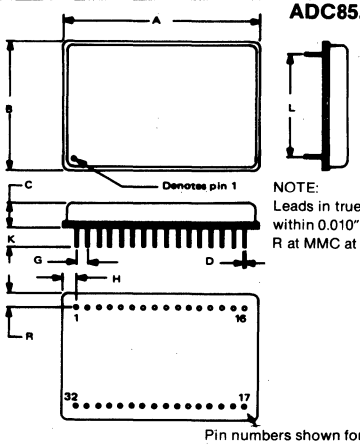


NOTE:
Leads in true position within 0.010" (0.255mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.016	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Ceramic
MATING CONNECTOR: 2302MC Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

ADC85. ADC85C



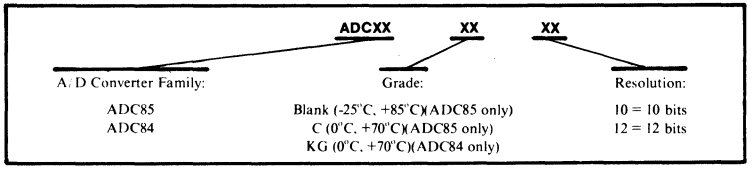
NOTE:
Leads in true position within 0.010" (0.255mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

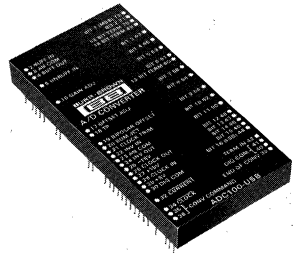
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Kovar, Nickel plated
MATING CONNECTOR: 2302MC Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

ORDERING INFORMATION



BURR-BROWN®



ADC100

High Resolution - Integrating ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 16-BIT RESOLUTION
- SELF-CONTAINED MODULAR PACKAGE
- LOW DRIFT
- USER-ADJUSTABLE LINEARITY
- EXPANDABLE TO 5-DIGIT BCD RESOLUTION

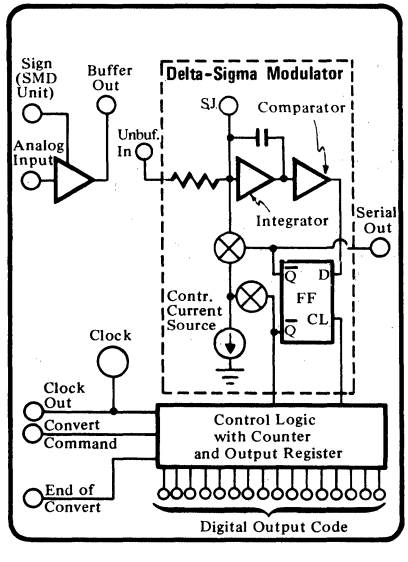
DESCRIPTION

The Burr-Brown Model ADC100 A/D Converter is an integrating A/D Converter that utilizes the delta sigma modulation principle. The digital equivalent of analog signals is developed by counting a number of pulses whose average repetition rate is proportional to the amplitude of the input signal over a fixed integration period. The internal clock is externally-adjustable to provide integration periods which are integral multiples of 50Hz or 60Hz periods for maximum powerline noise rejection. The closed conversion loop assures linear performance of ±0.005% ±1 count that is independent of clock frequency deviations over the specified temperature range of 0°C to ±70°C.

The ADC100 is housed in a 2" x 4" x 0.4" module and operates from ±15VDC and +5VDC power. All digital input and output signals are TTL-compatible.

Four basic models are offered: Unipolar 4-digit BCD, 4-digit plus sign BCD, unipolar and bipolar 16-bit binary. The binary units are pin-programmable for 12-, 14-, or 16-bit resolution.

The ADC100 is excellent for applications which require good accuracy and high resolution, but where speed is not too important. Conversion speeds range from 12msec for 12-bit binary to 30msec for 4-digit plus sign BCD codes.

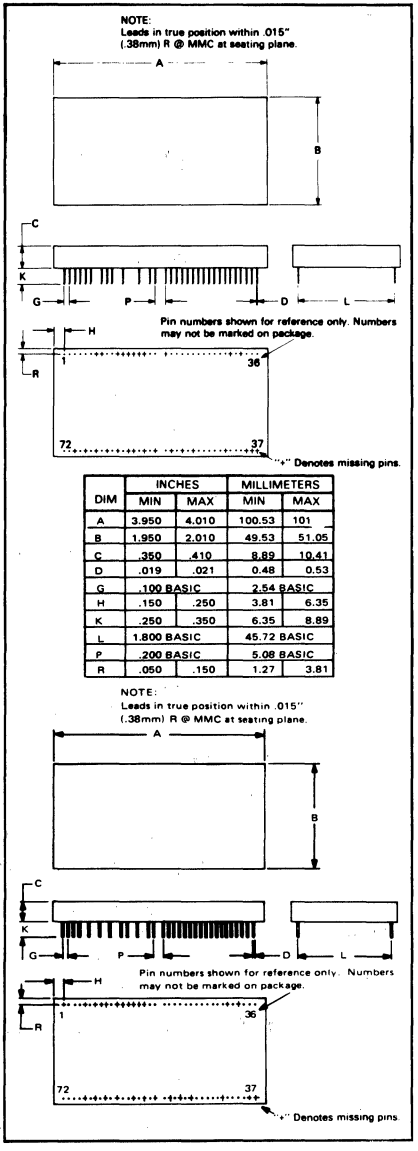


International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

Typical at 25°C and rated power supply unless otherwise noted.

ELECTRICAL					
MODEL	**DECIMAL**		**BINARY**		
ADC100	**BCD**	**SMD**	**Unipolar USB**	**Bipolar BOB**	**UNITS**
RESOLUTION	4 digits	4 digits + sign	14 or 16 bits	14 or 16 bits	
INPUT					
ANALOG INPUT					
Voltage Range	0 to +10	±10	0 to +10	±10	V
Maximum Safe Input Signal	±25V or supply voltage, whichever is less				
Input Bias Current typ max	20				nA
Impedance	200				nA
Buffered	200	200	200	200	MΩ
Unbuffered	10	10(1)	10	25	kΩ
Settling Time (to 0.003%) FSR(2) step					
Buffered, max	25	50	25	50	μsec
Unbuffered, max	1	1	1	1	μsec
DIGITAL INPUT					
Convert Command	TTL/DTL Compatible Logical "1" for at least one clock period @ 2 TTL Loads (Approximately 3μsec with internal clock)				
External Clock	See "Clock Operation"				
TRANSFER CHARACTERISTICS					
ACCURACY(3)					
Gain Error	.05	.05	.05	.05	% of FSR
Offset Error	.02	.02	.02	.05	% of FSR
Linearity Error, max(4)	±0.005	±0.005	±0.005	±0.005	% of FSR(2)
Quantizing Error	±1 count				
ACCURACY DRIFT					
Temperature Coefficient (max)	±10	±5	±10	±10	ppm of FSR/°C
POWER SUPPLY SENSITIVITY					
Power Supply Sensitivity, max					
±15VDC	±0.007	±0.004	±0.0002	±0.0002	% of FSR/% of P.S. Voltage(15V)
+5VDC	±0.002	±0.001	±0.002	±0.001	% of FSR/% of P.S. Voltage(5V)
CONVERSION TIME					
(maximum with Internal Clock)	30	30	For 12 bits - 12.5 14 bits - 50 16 bits - 200		msec
OUTPUT					
DIGITAL OUTPUTS	TTL/DTL Compatible All digital outputs will drive 6 TTL loads except the sign bit (for SMD units) which will drive 4 TTL loads.				
End of Conversion	"0" during conversion				
TEMPERATURE					
Specification	0 to +70				°C
Operating (reduced specs)	-25 to +85				°C
Storage	-55 to +100				°C
POWER SUPPLY					
Rated Voltage	±15 and +5				V
Range (max)	±14.5 to ±15.5 and +4.75 to +5.25				V
Supply Drain					
+15VDC	25	25	25	25	mA
-15VDC	20	20	15	15	mA
+5VDC	300	300	300	300	mA



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.950	4.010	100.53	101
B	1.950	2.010	49.53	51.05
C	.350	.410	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	.050	.150	1.27	3.81

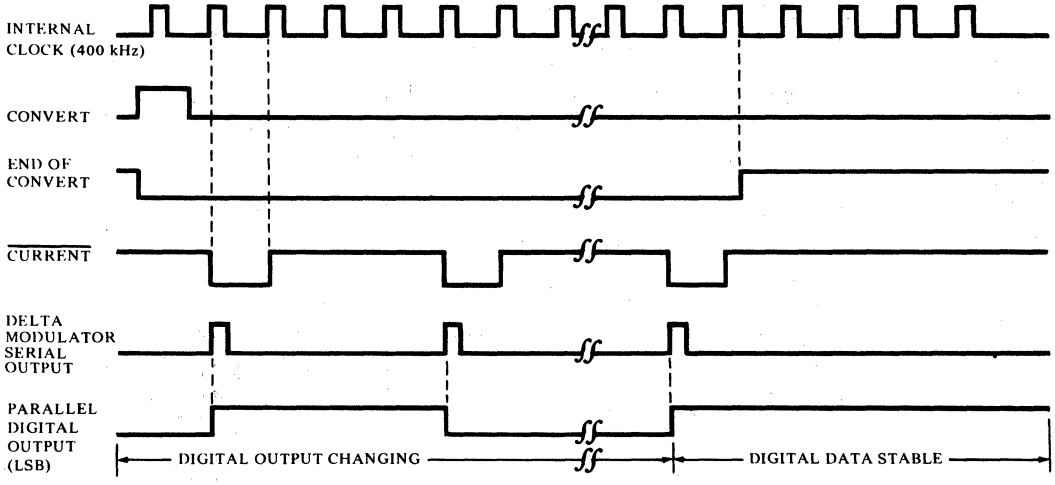
1) The internal buffer may be bypassed by connecting the input directly to unbuffered inputs. For SMD units this connection bypasses the sign magnitude circuitry and results in a unipolar BCD unit.
2) F S R is Full Scale Range; 10V for unipolar, 20V for bipolar converters.
3) Gain and Offset Error may be externally adjusted to zero.
4) Linearity is factory adjusted for 4 digit or 14 bit operation and is user adjustable to typically 0.002%.

Case: Diallyl Phthalate shell
Pins: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].
Weight: 4 oz (114 grams)
Actual pin assignments not shown on this diagram.
Mating Connectors: 2400MC - P.C. Card with solder terminals or 2401MC - Set of 4 - 18 pin connector strips

Method of Conversion

DELTA-SIGMA MODULATION

The Burr-Brown Model ADC100 A/D Converter utilizes the delta-sigma conversion technique which produces a train of pulses whose rate is proportional to the amplitude of the input analog signal. For a given internal clock frequency (400 kHz) the delta-sigma modulator output is a train of pulses whose average frequency varies from zero to 400 kHz. The width of these pulses are constant, but the number of pulses varies in relation to input signal amplitude. These pulses are counted in a binary (or BCD) counter over the integration interval resulting in a direct digital output that is equivalent to the analog input. The ADC100 timing diagram is shown in Figure 1.



DISCUSSION OF SPECIFICATIONS

ANALOG INPUT SETTLING TIME is the time required after a F.S.R. input step for the converter's input circuitry to settle to specified accuracy. The CONVERT COMMAND should be delayed by this period of time after any large input voltage change to preserve the converter's accuracy.

ACCURACY - The basic accuracy of the ADC100 is defined by linearity and quantizing errors. When gain and offset errors are adjusted as described on page 6-77, the accuracy of the ADC100 is 0.005% ±1 count.

LINEARITY ERROR is a measure of the deviation of the converter's actual transfer characteristic from the ideal. It is defined as the maximum deviation of the actual converter transfer function from the best fit straight line through it. If the linearity error is also adjusted (see page 6-78) the accuracy will typically be 0.002% ±1 count.

QUANTIZING ERROR is inherent in any A/D converter simply because a converter's analog input is continuous while its digital output must be discrete codes. The ADC 100 is designed such that increased resolution may be obtained by interpolation of several successive conversions of the same input voltage. For example, if the output code is zero for three conversions and one LSB for one conversion, the actual input voltage is one quarter of an LSB.

ACCURACY DRIFT is the maximum change with temperature of any point on the converter's transfer characteristic.

OFFSET ERROR is the deviation from the ideal input required to produce an output of all logical zeroes (all bits OFF). GAIN ERROR is the deviation from the ideal input required to produce an output of all logical ones (all bits ON) with the offset error adjusted to zero.

SERIAL OUTPUT

The serial output of the ADC100 may be used to transmit data remotely over a single line. Details for implementing this method of data transmission are shown on page 6-79 of this data sheet.

DIGITAL OUTPUT CODES

For unipolar analog input signals, 4 digit BCD or 16 bit straight binary (USB) digital output codes are offered; for bipolar analog input signals, 4 digit plus sign BCD (SMD) or 16 bit offset binary (BOB) digital output codes are offered. The LSB & full scale analog values and equivalent digital codes are shown in Table I.

ORDERING INFORMATION

The ADC 100 may be ordered by using the ordering code below.

ADC100 – XXX

ADC100 – Converter Family

XXX – OUTPUT CODE
BCD - Binary Coded Decimal
SMD - Sign Magnitude BCD
USB - Unipolar Straight Binary
BOB - Bipolar Offset Binary

INSTALLATION and OPERATING INSTRUCTIONS

CLOCK OPERATION

The ADC100 may be operated from the internal clock, or from a user supplied external clock.

A clock period faster than 2.5 μseconds or slower than 25μseconds will degrade the performance of the ADC100. 50 Hz or 60 Hz rejection may be achieved by adjusting the clock frequency such that the CONVERT COMPLETE pulse is an integral number of 50 or 60 Hz periods (i.e., a multiple of 16.67 ms for 60 Hz rejection or 20.00 ms for 50 Hz rejection). For example, SMD or BCD units convert in 30 millisec with a clock period of 3 μsec. The closest multiple for 60 Hz rejection is 33.33 ms integration time.

EXTERNAL CLOCK

An external clock may be used by leaving CLOCK OUT, pin 26, open and connecting the external clock to CLOCK IN, pin 28. The duty cycle of the external clock should be 80% to 90% as shown in Figure 3.

INTERNAL CLOCK

If the internal clock is used, CLOCK OUT, pin 26, and CLOCK IN, pin 28, must be connected together.

The approximate period of the internal clock is 3 μseconds.

The internal clock frequency may be adjusted using the circuit shown in Figure 5 over a range of approximately 2.5 μsec to 25 μsec. If the clock frequency is not adjusted, pin 21 should simply be left open.

CONNECTION DIAGRAMS

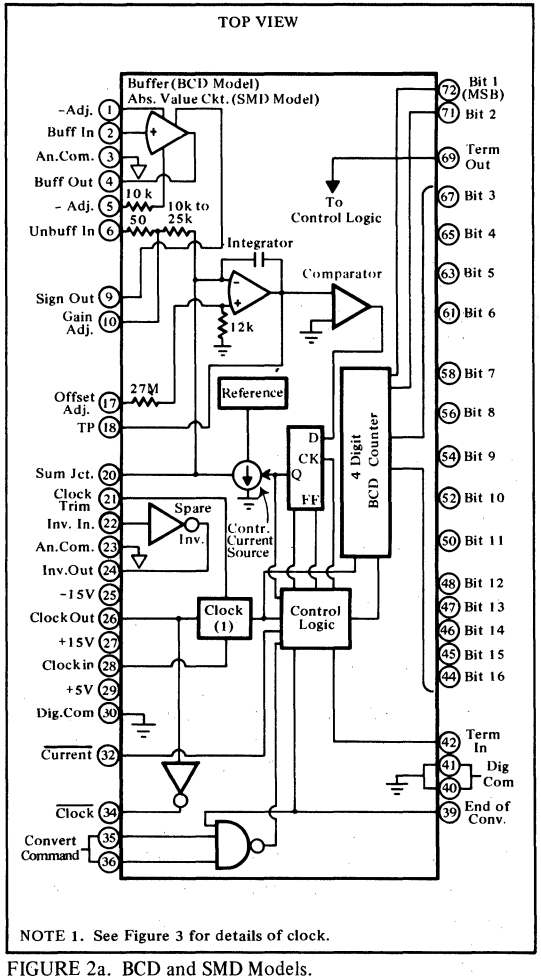


FIGURE 2a. BCD and SMD Models.

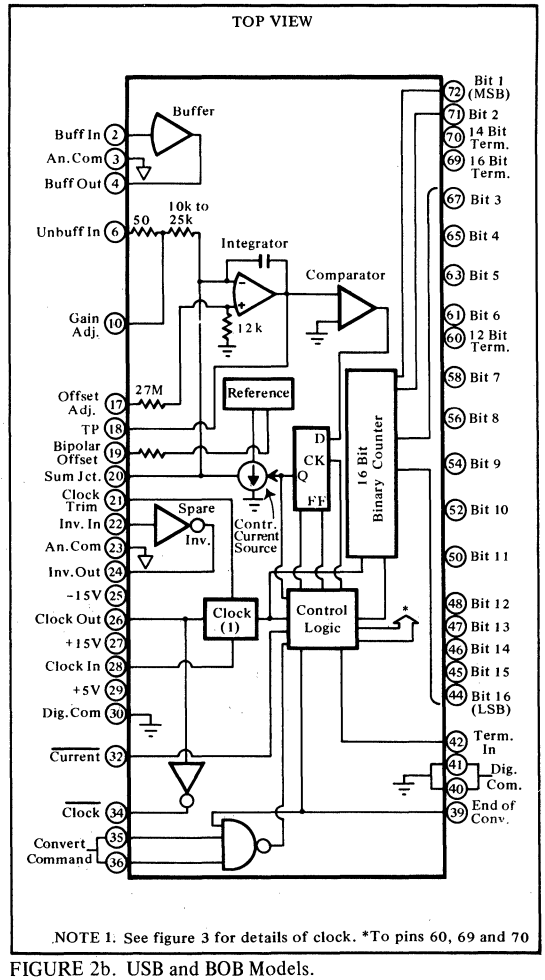


FIGURE 2b. USB and BOB Models.

ANALOG COMMON, pins 3 and 23, are connected together internally as are DIGITAL COMMON, pins 30, 40 and 41. Digital and Analog Common are not connected internally; but they should be tied together at some point in the system as close as possible to the ADC100 to prevent any difference voltage between them.

All units have available a spare inverter (SN7404) whose input is pin 22 and output is pin 24.

USB and BOB units are marked as shown in Figure 3, the BOB units only will have a connection for BIPOLAR OFFSET, pin 19. The BOB units must have pin 19 externally connected by the user to SUMMING JUNCTION, pin 20.

For USB and BOB units, either 16-BIT TERMINATE, pin 69, 14-BIT TERMINATE, pin 70, or 12-BIT TERMINATE, pin 60, must be connected to TERMINATE IN, pin 42. The LSB will always be on pin 44, the MSB for 16 bits is on pin 72, for 14 bits is on pin 67, for 12 bits is on pin 63.

BCD and SMD units are marked as shown in Figure 4, the SMD units only will have connections for ADJ, pin 1 and pin 5, and SIGN OUT, pin 9.

For BCD and SMD units, TERMINATE OUT, pin 69, should be connected to TERMINATE IN, pin 42, for 4-digit operation (see page 6-79 for increased resolution).

NOTE:

For SMD units, the output sign bit operates continuously. That is, the sign bit output will change with the input voltage polarity even though the end of conversion output is "high". Therefore an output flip flop (such as the 7474 IC shown on page 6-77) may be used to store the sign bit at the end of conversion. (The PC mount option includes this flip-flop).

CONNECTIONS FOR INPUT SIGNAL, EXTERNAL GAIN and OFFSET TRIM

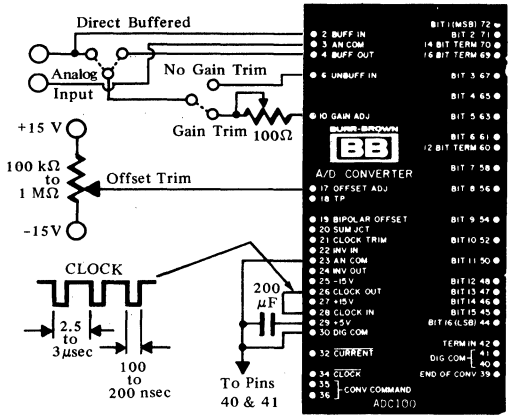


FIGURE 3. GAIN and OFFSET Adjustments for all Converters.

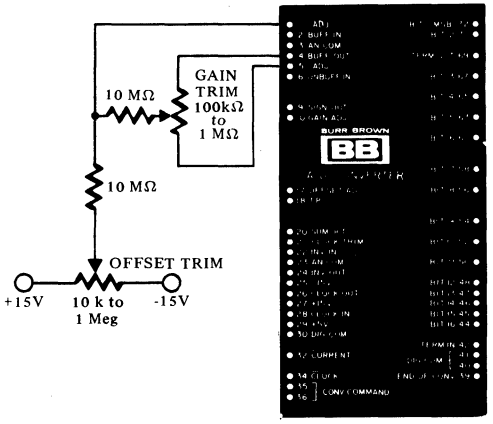


FIGURE 4. Additional NEGATIVE GAIN and OFFSET Adjustments required for SMD Converters.

The connections shown in Figure 3 illustrate various input and trim connection options; it is not necessary to include switches or jumpers as indicated unless that level of flexibility is desired. If linearity is not externally adjusted, the transfer characteristic of the ADC100 can be adjusted for minimum errors using only the GAIN and OFFSET adjustments. Table I shows the input voltage and respective output codes for these adjustments.

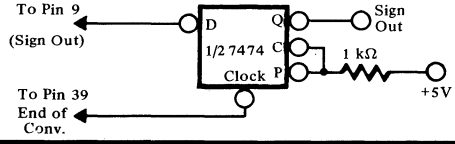
BCD and USB MODELS

Adjust to the proper output code with an input of +2.5000 volts using the OFFSET adjustment; then adjust to the proper output code with +7.5000 volts input using the GAIN adjustment (see Figure 3 for circuitry and Table I for input/output values). Repeat until both are optimum.

SMD MODELS

Adjust to the proper output codes as described above for BCD and USB models at 2.500 and +7.500 volts; then use the negative OFFSET adjustment (as shown in Figure 4) to provide the proper output code with -10 mV input and the negative GAIN adjustment (also in Figure 4) to provide the proper output code with -9.9900 volts input (see Table I).

SMD SIGN BIT STORAGE (see note on page 6-76).



BOB MODELS

Using the OFFSET adjustment, adjust to the output code of 0100 . . . . 00 with an input of -5.0000 volts; then find the input voltage, (near +5.00 volts), that causes an output code of 1100 . . . 000. Set the input voltage to a point halfway between e and 5.0000 volts. Use the GAIN adjustment to provide an output of 1100 . . . 000. Repeat the OFFSET adjustment at -5.0000 volts and check to see that an input of +5.00000 volts produces an output code of 1100 . . . 000. (See Table I). Repeat until both are optimum.

WIRING PRECAUTIONS

All connections between the ADC100 and external components should be as short as possible to minimize coupling effects and noise pickup. The +5V logic supply must be bypassed with a 100 to 200 µF tantalum capacitor to digital common to preserve ADC100 linearity, particularly near mid-scale. Experimenting by setting full scale and zero exactly correct and checking at or near mid-scale while varying the power supply decoupling will demonstrate the quality of the bypassing. This should be done first without any of the clock and/or linearity adjust circuitry, and then with the circuitry if it is to be used.

UNUSED ADJUSTMENTS

All unused adjustments should be left open except OFFSET adjust which should be grounded.

CODE		One LSB (mV)	1/4 Scale OFFSET Adjust		3/4 Scale GAIN Adjust	
			Input Voltage	OUTPUT CODE	Input Voltage	OUTPUT CODE
	BCD 4 digit	1.00	+2.5000	MSB LSB 0010 0101 0000 0000	+7.5000	MSB LSB 0111 0101 0000 0000
USB	12 bits	2.44	+2.5000	010000000000	+7.5000	110000000000
	14 bits	0.61	+2.5000	01000000000000	+7.5000	11000000000000
	16 bits	0.15	+2.5000	0100000000000000	+7.50000	1100000000000000
SMD	Positive	1.00	+2.5000	1 0010 0101 0000 0000	+7.5000	1 0111 0101 0000 0000
	Negative		-0.0100	0 0000 0000 0001 0000	-9.9900	0 1001 1001 1001 0000
BOB	12 bits	4.88	-5.0000	010000000000	+5.0000	110000000000
	14 bits	1.22	-5.0000	01000000000000	+5.0000	11000000000000
	16 bits	0.31	-5.00000	0100000000000000	+5.00000	1100000000000000

NOTE: Negative full scale is 0.000V for unipolar and -10.000V for bipolar models. Positive full scale is +10.000V -1 LSB.

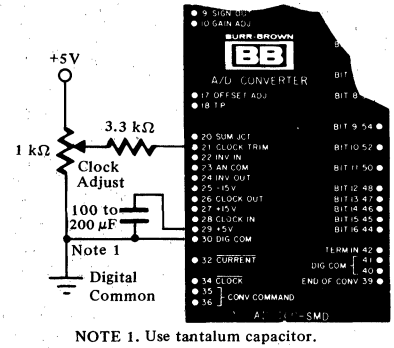
TABLE 1. GAIN and OFFSET Adjustments without LINEARITY Trim.

CLOCK and LINEARITY ADJUSTMENTS

CLOCK ADJUST

It may be necessary to adjust the clock frequency if optimum noise rejection to 50 or 60 Hz power line frequency is desired, or else a specific conversion period is desired. Otherwise, an external clock adjustment is not required. The CLOCK ADJUST trim circuitry shown in Figure 5 may affect linearity, particularly where there is already a bypassing problem with the 5 volt logic supply. If clock trim is employed, it may also be necessary to perform the linearity adjustment described below. The external wiring at pin 21 should be as short as possible to minimize this problem.

NOTE: The 400 kHz clock frequency will vary up to 1% per degree Centigrade. This will have a very small affect on the accuracy of the ADC100, but it can cause problems in some systems applications since the total conversion time will vary inversely with this frequency.



NOTE 1. Use tantalum capacitor.

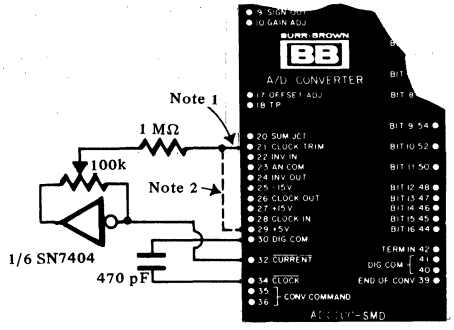
FIGURE 5. CLOCK ADJUST Circuit.

LINEARITY ADJUSTMENT

Linearity errors can typically be adjusted to less than 0.002% with the circuitry shown in Figure 6. This adjustment can be done only when the internal clock is used.

If the LINEARITY adjust circuitry is used, the OFFSET adjustment should be made near negative full scale, the GAIN adjustment should be made near positive full scale, and linearity adjusted near mid-scale. See Table II for the proper input voltages and output codes.

With GAIN and OFFSET adjusted per above, the linearity error should be adjusted to zero near mid-scale. Supply the ADC100 input with the mid-scale voltage shown in Table II and adjust the linearity potentiometer to obtain the output code also specified in Table II.



NOTES:
1. This wire should be as short as possible
2. This connection required only when external clock is used.

FIGURE 6. LINEARITY Adjustment Circuit.

CODE	OFFSET Adjustment		GAIN Adjustment		Mid-Scale LINEARITY Adjust	
	Input Voltage	Output Code	Input Voltage	Output Code	Input Voltage	Output Code
BCD 4 digit	+0.0100	MSB LSB 0000 0000 0001 0000	+9.9900	MSB LSB 1001 1001 1001 0000	+5.010	MSB LSB 0101 0000 0001 0000
USB 12 bits 14 bits 16 bits	 +0.00976 +0.00976 +0.00976	 000000000100 00000000010000 0000000001000000	 +9.9878 +9.9896 +9.9901	 111111111011 11111111101111 1111111110111111	 +5.00488 +5.00488 +5.00488	 100000000010 10000000001000 1000000000100000
SMD Positve Negative	 +0.0100 -0.0100	 1 0000 0000 0001 0000 0 0000 0000 0001 0000	 +9.9900 -9.9900	 1 1001 1001 1001 0000 0 1001 1001 1001 0000	 +5.010 – –	 1 0101 0000 0001 0000 – –
BOB 12 bits 14 bits 16 bits	 -9.99024 -9.99024 -9.99024	 000000000010 00000000001000 000000000010000	 +9.9854 +9.9890 +9.9898	 111111111101 11111111110111 1111111111011111	 +0.00976 +0.00976 +0.00976	 100000000010 10000000001000 1000000000100000

TABLE II. GAIN and OFFSET Adjustments with LINEARITY Trim.

APPLICATIONS

VOLTAGE TO FREQUENCY CONVERTER

The $\overline{\text{CURRENT}}$ output, pin 32, and the $\overline{\text{CLOCK}}$ output, pin 34, may be used to provide a continuous serial output pulse train whose average repetition rate is proportional to the analog input voltage. This circuitry is shown in solid lines in Figure 8. The END OF CONVERSION output, pin 39, can be gated with the serial output using the additional circuitry shown with dotted lines. The gated output pulse train is available only during conversion and the number of pulses in that period is proportional to the input voltage, as shown in Figure 7.

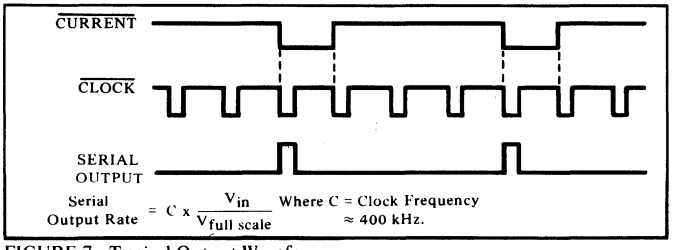


FIGURE 7. Typical Output Waveforms.

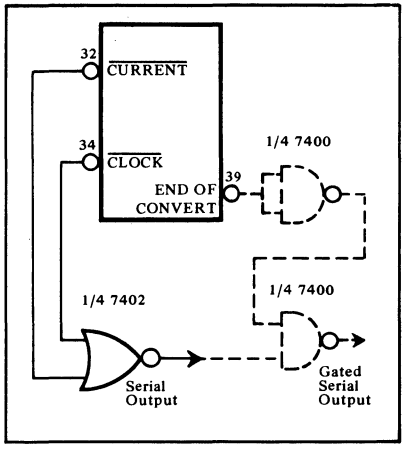


FIGURE 8. Voltage to Frequency Converter

5 DIGIT ADC100

The resolution of BCD and SMD models may be expanded to 4-1/2 or 5 digits with a minimum of external circuitry. Expansion to 4-1/2 digits will double the conversion time to about 60 milliseconds while 5 digit conversion will require 300 milliseconds. Figure 9 shows the application of two SN 7490 decade counters to provide an extra digit output.

If the ADC100 is used for five digit operation, it is recommended that the linearity adjustment circuitry shown on page 6-78 be used to provide accuracy consistent with the resolution. With five digit operation, the positive full scale input voltage is +9.99990 volts while the negative full scale input is 0.00000 volts (BCD) or -9.99990 (SMD). A good mid-scale input voltage to use for the linearity adjustment is 5.00500 volts (output code 0101 0000 0000 0101 0000).

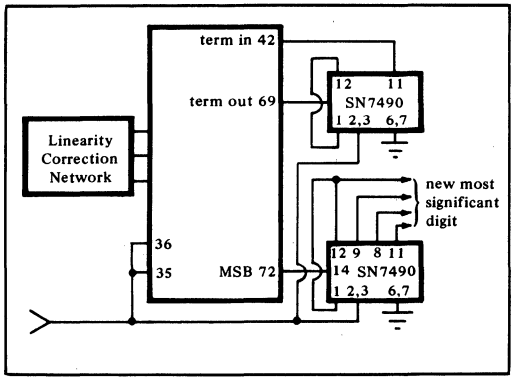


FIGURE 9. Extending ADC100 to 5 Digits.

The ADC100 may be used as the heart of a 5 digit DPM with accuracy much better than that of any moderately priced digital panel meters at a lower cost.

The components required in addition to the ADC100 are:

(1) Two decade counters (such as TI's SN7490)
(2) Five BCD to seven segment decoders (such at TI's SN7447A)
(3) A display (such as RCA's DR2100 Numitron series)
(4) Power Supplies, ±15 volts and +5 volts (such as Burr-Brown's Model 551 and Model 562).

ADC100 PREAMPLIFIER

An instrumentation amplifier may be used as the input to the ADC100. An input instrumentation amplifier such as Burr-Brown's 3625 will provide differential inputs with common mode rejection as well as gain. The circuitry shown below will provide a gain of 10 (i.e., 1 volt instead of 10 volt input range) and 74 dB CMR.

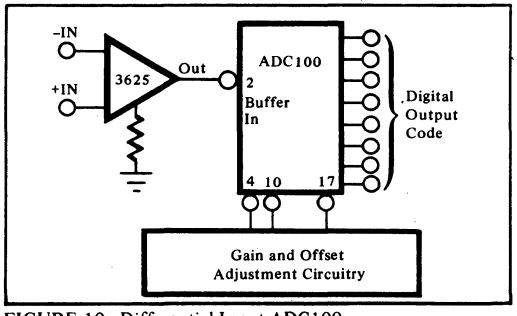
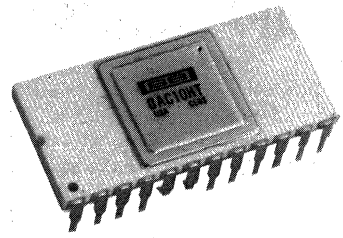


FIGURE 10. Differential Input ADC100.

The offset adjustment of the ADC100 has enough range to compensate for the small output offset of the 3625 and its' gain adjustment can compensate for the gain errors of the 3625

The 3625B will add no more than 10 ppm/°C gain drift and 1 ppm/°C offset drift while contributing only 0.002% linearity errors.

BURR-BROWN®



DAC10HT

Wide Temperature Range General Purpose 12-Bit DIGITAL-TO-ANALOG CONVERTER

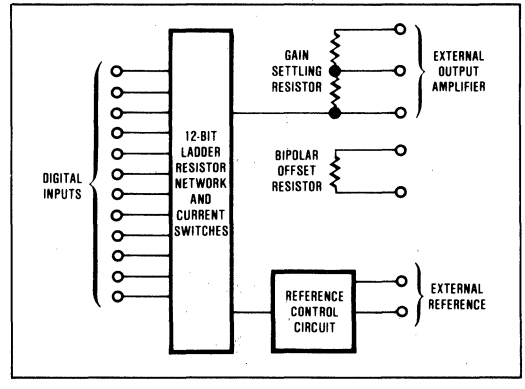
FEATURES

- -55°C to +200°C SPECIFICATIONS
- FULL 12-BIT RESOLUTION
- 200nsec SETTLING TIME, TYPICAL
- MONOTONIC OVER FULL TEMPERATURE RANGE
- TTL AND CMOS COMPATIBLE
- HERMETIC DUAL-WIDTH CERAMIC PACKAGE

DESCRIPTION

Designed for use in circuits that operate over a wide temperature range, DAC10HT is a general purpose, 12-bit D/A converter. The design uses state-of-the-art integrated circuit and laser-trimmed thin-film techniques for maximum accuracy. Compatible with TTL and CMOS logic, DAC10HT is monotonic over the full -55°C to +200°C temperture range. Special design techniques minimize output glitches. The package is compact, dual-width, 24-pin ceramic DIL.

100% screening operations are conducted at key manufacturing steps. Burn-in and temperature cycling are examples, and the product is assembled in a clean-room environment.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-475

SPECIFICATIONS

ELECTRICAL

Specifications at V_{CC} = +15VDC, V_{EE} = -15VDC, Reference = +10VDC, and T_A = +25°C unless otherwise noted.

MODEL	DAC10HT			DAC10HT-1			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
DIGITAL INPUTS							
Resolution	12			12			Bits
TTL-Logic "1" at 100nA, max	2.0			2.0			V
Logic "0" at -100μA, max			0.8			0.8	V
CMOS(1)-Logic "1" at 100nA, max	70% V_{CC}			70% V_{CC}			V
Logic "0" at -100μA, max			30% V_{CC}			30% V_{CC}	V
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at +25°C							
12-Bit		±1/4	±1/2				LSB
10-Bit					±1/4	±1/2	LSB
at -55°C to +200°C							
12-Bit			±2				LSB
10-Bit						±2	LSB
Gain Error(2)		0.05	0.2		0.05	0.2	%
Bipolar Offset Error (input all 0's)(2)		0.05	0.2		0.05	0.2	% of FSR
Unipolar Offset Error (input all 0's)(2)			0.2			0.2	% of FSR
Monotonic Temperature Range							
12-Bit	-55		+200				°C
10-Bit				-55		+200	°C
Differential Linearity Error							
12-Bit		±1/2	±1				LSB
10-Bit					±1/2	±1	LSB
Total Unadjusted Error(3)							
+25°C		±0.1	±0.4		±0.15	±0.45	% of FSR
-55°C to +200°C		±0.3	±0.8		±0.90	±1.30	% of FSR
Total Adjusted Error(4)							
+25°C		±0.006	±0.012		0.024	±0.048	% of FSR
-55°C to +200°C		±0.015	±0.40		±0.40	±0.90	% of FSR
CONVERSION SPEED							
Settling Time to 1/2LSB (+FS change)(5)		200			200		nsec
Major Carry Glitch Duration (to 90% complete)		35			35		nsec
DRIFT (-55°C to +200°C)							
Gain (exclusive of reference drift)		±2	±10		±5	±25	ppm/°C
Bipolar Offset		±2	±10		±5	±25	ppm of FSR/°C
Unipolar Offset		±0.5	±1		±2	±5	ppm of FSR/°C
Differential Linearity		±2	±3		±3	±4	ppm of FSR/°C
OUTPUT							
Current - Unipolar (±10%)		0 to 5			0 to 5		mA
Current - Bipolar (±10%)		-2.5 to +2.5			-2.5 to +2.5		mA
Selectable Ranges(6)		0 to +5, 0 to +10, -2.5 to +2.5, -5 to +5, -10 to +10			0 to +5, 0 to +10, -2.5 to +2.5 -5 to +5, -10 to +10		V
Resistance		1.0			1.0		kΩ
Capacitance		20			20		pF
Compliance Voltage	-3		+10	-3		+10	V
EXTERNAL ADJUSTMENTS							
Gain Adjust Range		±0.25			±0.25		% of FSR
Bipolar Offset Adjust Range		±0.25			±0.25		% of FSR
Unipolar Offset Adjust Range		±0.25			±0.25		% of FSR
NOISE (0.1Hz to 10Hz, all "1"s)		30			30		μV, p-p
MULTIPLYING MODE PERFORMANCE							
Number of Quadrants(7)			2			2	
Reference Voltage Range	0		+10.24	0		+10.24	V
Accuracy(8)	±0.05			±0.05			% of FSR
Feedthrough(9)		±0.02			±0.02		% of FSR
Output Slew Rate(10)		6			6		mA/μsec
Output Settling Time (to 0.01% of FS)(10)		3			3		μsec
Control Amplifier BW (small-signal, closed-loop)		10			10		MHz
POWER SUPPLIES AND REFERENCE							
Reference Input Impedance		8 ±10%			8 ±10%		kΩ
Reference Voltage Range	0		+10.24	0		+10.24	V
Power Supply, Voltage - V_{CC}	+4.75		+15.0	+4.75		+15.0	VDC
Voltage - V_{EE}	-13.5	-15	-16.5	-13.5	-15	-16.5	VDC
Current - V_{CC}		+9	+15.0		+9		mA
Current - V_{EE}		-28	-40.0		-28		mA
Power Supply Sensitivity							
V_{CC} at +5VDC		1	5		1	5	ppm/%ΔV
V_{EE} at -15VDC		3	10		3	10	ppm/%ΔV

SPECIFICATIONS

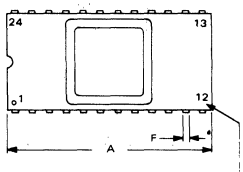
MODEL	DAC10HT			DAC10HT-1			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE							
Specification	-55		+200	-55		+200	°C
Operating	-55		+200	-55		+200	°C
Storage	-65		+210	-65		+210	°C

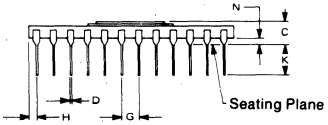
NOTES:
1. +4.75V < V_{CC} < +15.0V and pin 2 tied to pin 1.
2. Adjustable to zero (see Figures 4 and 5).
3. Includes Gain, Offset, and Linearity Errors with external +10.0V ±1mV reference. Does not include Reference Drift.
4. Gain and Offset Errors removed at +25°C with external +10.0V ±1mV reference. Does not include Reference Drift.
5. Current settling into short circuit.
6. Using internal scaling resistors and OPA11HT output op amp.
7. Bipolar operation at digital inputs only.
8. For 1VDC reference voltage (see Figure 2). Full Scale Range = 1V.
9. Voltage at reference input: 0 to +10V. 2kHz sine wave (see Figure 3).
10. All "1"s. 10V step on reference input.

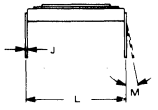
PIN DESIGNATIONS

$+V_{CC}$	1	24	BIT 1 (MSB)
LOGIC THRESHOLD	2	23	BIT 2
V_{REF} INPUT (LO)	3	22	BIT 3
N/C	4	21	BIT 4
V_{REF} INPUT (HI)	5	20	BIT 5
$-V_{EE}$	6	19	BIT 6
BIPOLAR OFFSET	7	18	BIT 7
BIPOLAR OFFSET	8	17	BIT 8
CURRENT OUTPUT	9	16	BIT 9
10V RANGE	10	15	BIT 10
20V RANGE	11	14	BIT 11
COMMON	12	13	BIT 12 (LSB)

MECHANICAL







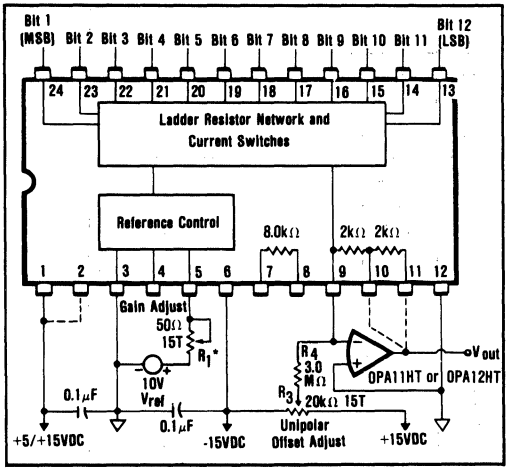
Pin numbers shown for reference only.
Numbers may not be marked on package.

NOTE:
Leads in true position within 0.010" (0.25mm)R at MMC at seating plane.

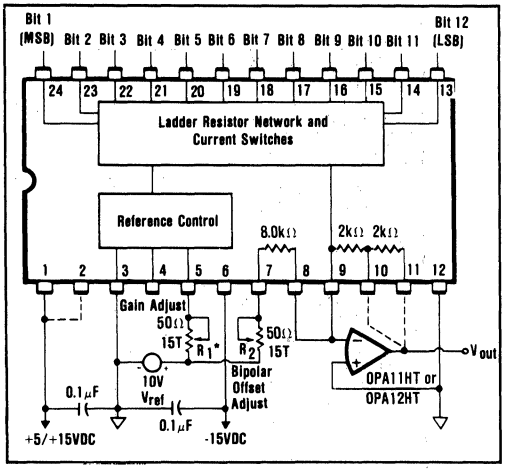
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	— —	10°	— —	10°
N	.025	.060	0.64	1.52

CASE: Ceramic with hermetic seal

CONNECTION DIAGRAM - UNIPOLAR



CONNECTION DIAGRAM - BIPOLAR



*In high temperature environments with high levels of shock and vibration it is recommended that discrete wirewound or metal film resistors be used instead of potentiometers.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

DAC10HT accepts a positive-true straight binary (BIN) input code. Offset-binary code is created by offsetting the output amplifier with the DAC reference. Two's complement code is obtained from offset binary by inverting bit 1 (the most significant bit) externally. See Table I.

ACCURACY

Linearity of the DAC10HT is guaranteed to be within the specification over its temperature range. This is the measure of the deviation of the actual transfer curve from the ideal transfer curve expressed graphically as a straight line drawn between the end-point values. For the DAC10HT the maximum deviation is ±1/2LSB at 25°C and ±1LSB over the full specification temperature range from -55°C to +200°C.

Differential Linearity error is the deviation from an ideal 1LSB output voltage change from one adjacent state to the next. An error specification of ±1/2LSB indicates that output voltage step size can range from 1/2LSB to 3/2LSB between adjacent states.

Monotonicity is an important property for a D/A converter, especially one used in a closed control loop. A converter is monotonic if the output signal increases or remains the same for an increase in digital input. A converter's differential linearity determines whether or not it is monotonic. If differential linearity is <±1LSB, the converter will be monotonic. Monotonicity is guaranteed over the entire specified temperature range for the DAC10HT.

Leakage Current is measured at the converter output with logic 0 on all digital inputs. It appears as part of offset error, both at room temperature and over the specified temperature range. In the unipolar configuration, virtually all offset error is due to leakage current.

DRIFT

Gain Drift is a measure of the change in the full scale range output due to a change in temperature and is expressed in parts per million per °C (ppm/°C). It is calculated by determining the full scale range value at high temperature, then at low temperature. The difference in the two values is divided by the difference in the two temperatures.

Offset Drift is a measure of the actual change in output over the specified temperature range with logic 0 on all digital inputs. It is calculated by measuring offset voltage at the temperature extremes. The maximum change referred to the offset voltage at +25°C is divided by the temperature excursion from +25°C. Offset drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

Differential Linearity Drift (the change in differential linearity over the specified temperature range) is calculated in a manner similar to offset drift and is expressed in ppm of FSR/°C.

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES				
	ANALOG OUTPUT			
LOGIC INPUTS	VOLTAGE*		CURRENT	
Binary	0 to +10V	-10V to +10V	0 to -2mA	-1mA to +1mA
111111111111	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
100000000000	+5.0000V	0.0000V	-1.0000mA	0.0000mA
011111111111	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
000000000000	0.0000V	-10.0000V	0.0000mA	+1.0000mA
Binary Two's Complement**				
011111111111		+9.9951V		-0.9995mA
000000000000		0.0000V		0.0000mA
111111111111		-0.0049V		+0.0005mA
100000000000		-10.000V		+1.0000mA
1LSB (BIN)	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.
**MSB must be inverted externally for this code.

CONVERSION SPEED

Settling Time is the time required for the output to enter and remain within an error band of the final value measured from the time the digital input is changed.

The settling time for a 1LSB change at the input is naturally less than for a full scale change. It is greatest at the major carry point (the point at which all of the bits change states) due to nonuniform switching times of the internal current switches. For a 1LSB change at the major carry point, settling time to within 0.01% will typically be 200nsec.

COMPLIANCE VOLTAGE

This is the maximum voltage which can be impressed on the current output node and still remain within the specified accuracy. These voltages are -3.0V and +10V.

POWER SUPPLY SENSITIVITY

This measure of the effect of a power supply voltage change on the D/A converter output is defined as a percent of FSR/percent of change in either the +5V, +15V or -15V power supplies about the nominal supply voltages. Figure 1 shows power supply rejection vs frequency.

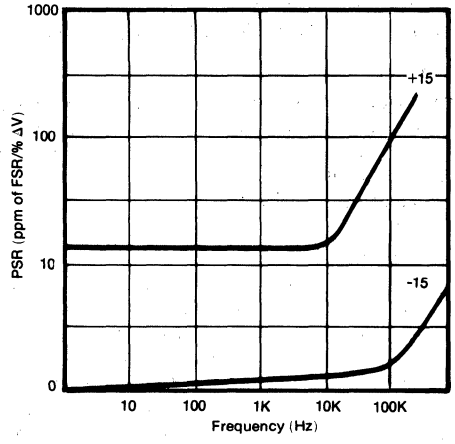


FIGURE 1. Power-Supply Rejection vs Power-Supply Ripple Frequency.

MULTIPLYING MODE PERFORMANCE

The output of the DAC10HT is the product of the reference input and digital input values. The reference may be an AC signal and can vary from 0 to +10 volts. This is useful in applications where digitally programmed attenuation of a signal is desired. Bcause the reference voltage input must be positive, the DAC10HT multiplies in two quadrants only. For highest accuracy the input reference voltage should be as high as possible (see Figure 2).

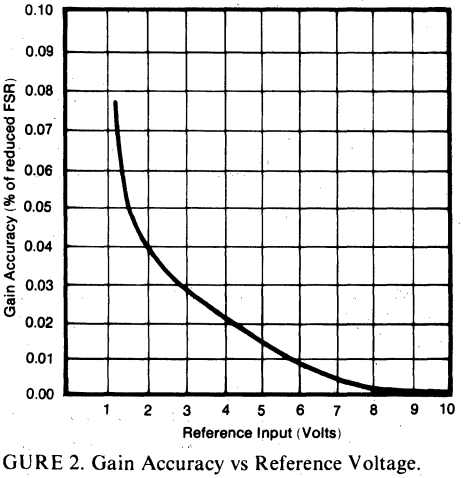


FIGURE 2. Gain Accuracy vs Reference Voltage.

Feedthrough of the DAC10HT is the amount of reference signal that appears at the output when all digital inputs are logic 0. Expressed in % of FSR, it increases with increasing reference frequency (see Figure 3).

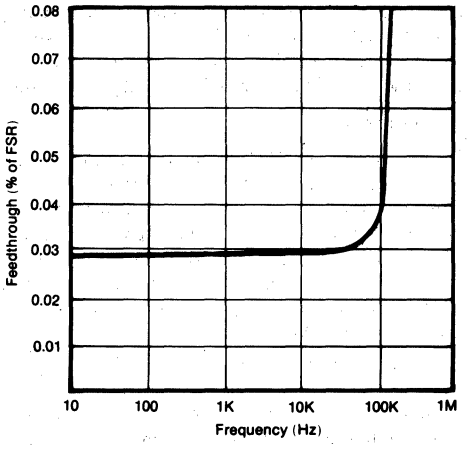


FIGURE 3. Feedthrough Voltage vs Power-Supply Ripple Frequency (Unipolar Mode).

OPERATING INSTRUCTIONS

INPUT LOGIC LEVELS

Inputs of the DAC10HT are either TTL or CMOS logic compatible. For TTL, connect +5V to pin 1 (pin 2 open). For +5V CMOS, connect +5V to pins 1 and 2. For +15V CMOS compatibility, connect +15V to pins 1 and 2.

In circuits where pin 2 is used to determine the digital threshold level, the following application tip may be helpful. If the analog system ground (to which the DAC10HT is referred) is separate from the digital driving logic ground, the threshold voltage input (at pin 2) may be driven from an external voltage source to keep the threshold at proper value. Threshold voltage will always be at one-half the voltage applied to pin 2 ($+1.4V < \text{pin } 2 < +15V$).

POWER SUPPLIES

Each power supply should be bypassed to ground with a 0.1μF capacitor as shown in the Connection Diagrams. Locate the capacitors as close as possible to the DAC10HT.

GAIN AND OFFSET ADJUSTMENTS

(Voltage Output Configuration)

Initial gain and offset errors of the DAC10HT circuit may be trimmed out using the following procedures.

Unipolar configuration - input all 0's and null offset error by adjusting R_3 until output voltage equals zero. Input all 1's and adjust R_1 until the output voltage is +FS -1LSB (see Table I and Connection Diagram).

Bipolar configuration - input all 0's and null offset error by adjusting R_2 until output voltage equals -FS. Input all 1's and adjust R_1 until the output voltage is +FS - 1LSB (see Table I and Connection Diagram).

To obtain specified gain and offset errors, replace the 50Ω potentiometers (R_1 and R_2) shown in the Connection Diagrams with 25Ω 0.1% fixed resistors.

SELECTING AN EXTERNAL REFERENCE

DAC10HT is configured to use a +10V reference. An internal 8kΩ resistor in series with an external 50Ω adjust potentiometer sets the current into the reference input at 1.25mA (see Figure 4).

Temperature drift of the reference increases drift of the entire circuit. In unipolar configurations the drift specification adds directly to the total circuit drift. In the bipolar configuration some drift cancelling effects take place. One-half of the reference drift added to the total DAC drift will give total circuit drift.

If a reference voltage other than +10V is required, use the circuit shown in Figure 5.

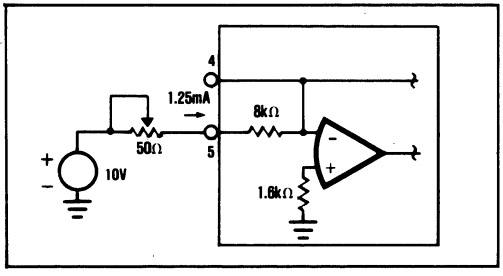


FIGURE 4. Using a +10V Reference.

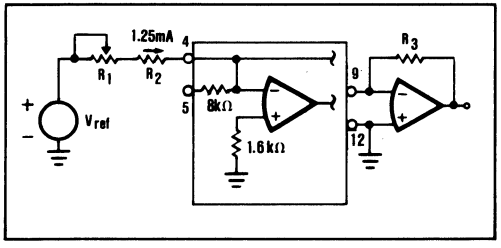


FIGURE 5. Using a Voltage Reference Other Than +10V.

The equation $V_{REF}/(R_2 + 1/2R_1) = 0.5mA$ should be used to select R_1 and R_2. The ratio of R_2 and R_1 should be approximately 200:1 for proper gain adjust range. To achieve good low drift performance over temperature with this method, R_2 and R_3 should track each other to within 5ppm/°C.

SELECTING AN EXTERNAL REFERENCE

Building An External +10V 200°C Reference

The DAC10HT requires an external +10V reference for normal operation. A circuit for obtaining this reference voltage that will operate at +200°C is shown in Figure 6. The value of R_1 or R_2 should be adjusted to provide a reference voltage of 10V ±1mV due to the tolerance of the zener voltage. With no adjustment to the zener current for optimum zero T.C. point (see page 10), this reference will have an average temperature coefficient of about ±20ppm/°C over -55°C to +200°C.

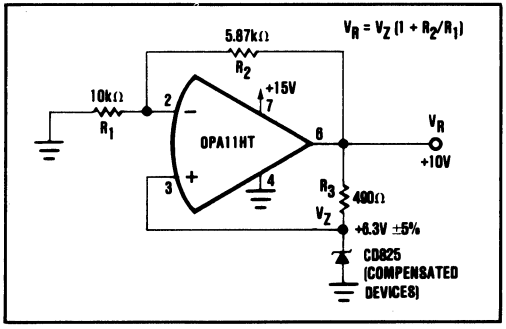


FIGURE 6. +10V Reference That Will Operate At +200°C.

LOW POWER OPERATION

The typical supply currents required by the DAC10HT under normal operating conditions are 9mA (V_{CC}) and 28mA (V_{EE}). The average power required (P_D) is therefore

$$P_D = |V_{CC} \times 9mA| + |V_{EE} \times 28mA|$$
$$= 555mW \ (+V_S = 15V, -V_S = 15V), \text{ or}$$
$$= 465mW \ (+V_S = 5V, -V_S = 15V).$$

Under certain operating conditions this power consumption can be reduced to as little as 245mW.

The major contributor to the power consumption is the -15V supply. As long as a +10V reference is used, V_{EE} must be between -13.5V and -16.5V. If, however, a lower reference voltage is used, V_{EE} can be reduced considerably and this greatly reduces the power consumption. Lowering the reference voltage will, of course, lower the full scale output voltage by a proportional amount. For example, if the reference voltage is +5V, the full scale output voltage when using the 10V range pin (pin 10) will be +5V instead of +10V with a +10V reference in the unipolar mode of operation. Table II indicates the minimum supply voltages and the power consumption obtained when using these supply voltages for various values of V_{REF}. See also page 10 for a discussion of how to build a low power voltage reference circuit.

TABLE II. Minimum Power Supply Voltages and Typical Power Consumption for Operation with Various Values of V_{REF}.

External V_{REF}	+Vcc (Pin 1)	-VEE (Pin 6)	Total Power Consumption (Typical)
+10V	+5V	-13V	409mW
+6.3V	+5V	-10V	275mW
+5V	+5V	-8V	235mW

SELECTING AN OUTPUT AMPLIFIER

The most important characteristics of the output amplifier are input offset voltage drift, input bias (or difference) current drift, and settling time. Specifications over the full operating temperature range are very important. Initial input offset voltage and bias current effects will be trimmed out, but bias errors will be introduced as these parameters drift with temperature changes. Errors introduced will appear as offset in the D/A circuit output.

Table III provides the equations used to convert these amplifier errors to D/A output errors.

TABLE III. Computing DAC Error Contributed by External Amplifier.

PARAMETER	UNIPOLAR CONFIGURATION	BIPOLAR CONFIGURATION
I_{Bias}	$\frac{I_B \times R_F}{FSR} \times 100$	$\frac{I_B \times R_F}{FSR} \times 100$
V_{os}	$\frac{V_{os}\left(1 + \frac{R_F}{1k\Omega}\right)}{FSR} \times 100$	$\frac{V_{os}\left(1 + \frac{R_F}{0.8k\Omega}\right)}{FSR} \times 100$
FSR = Full scale range (-2.5V to +2.5V is a 5V FSR, etc.). Results are in % of FSR; to get ppm of FSR, multiply by 10^4. R_F is the value of the feedback resistor. R_{F_1} and R_{F_2} are options shown in Figure 7.		

Example:

If V_{os} drift and I_{bias} drift of the output amplifier are $10\mu V/°C$ and $0.5nA/°C$, respectively, in a D/A converter with -10V to +10V output, the output drift due to these effects would be computed in this manner.

$$V_{os}: \frac{(10 \times 10^{-6})\left(1 + \frac{10k\Omega}{4.0k\Omega}\right)}{20} \times 100 = 0.00018\% \text{ of FSR}/°C$$

or 1.8ppm of FSR/°C

$$I_{Bias}: \frac{0.5 \times 10^{-9} \times (10k\Omega)}{20} \times 100 = 0.00003\% \text{ of FSR}/°C$$

or 0.3ppm of FSR/°C

Total error contribution of amplifier = 1.8 + 0.3 = 2.1ppm of FSR/°C

Effects of input bias current drift may be reduced approximately by a factor of 5 by placing a resistor in series with the positive input lead of the amplifier as shown in Figure 7.

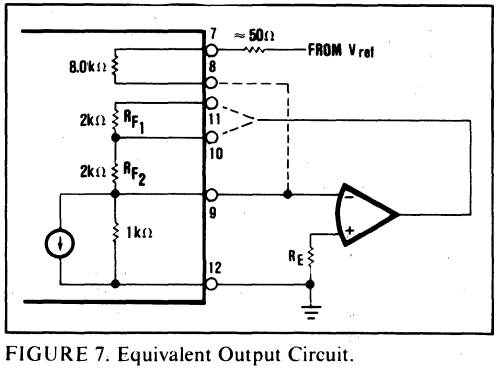


FIGURE 7. Equivalent Output Circuit.

This balances the offset created by bias currents and the error is reduced to the difference in bias currents in the positive and negative inputs. (Substitute I_{offset} in equations in Table III).

The value of this resistor is shown in Table IV for different output ranges.

TABLE IV. R_E Values.

Output Range	±2.5V	±5V	±10V	0 to +5V	0 to +10V
R_E Value	470Ω	615Ω	727Ω	500Ω	800Ω

Settling time of the DAC10HT is less than 400nsec for an FSR change to within 0.01% of final value. The output amplifier's dynamic characteristics should be compatible with this performance. Burr-Brown's OPA12HT fast-settling amplifier is recommended for use up to 175°C. The OPA11HT is recommended for operation at +200°C.

CURRENT OUTPUT OPERATION

DAC10HT can be connected to produce a bipolar voltage output without the use of external components by connecting the internal resistors as shown in Figure 8. Output voltage range of this circuit is approximately ±2.25V.

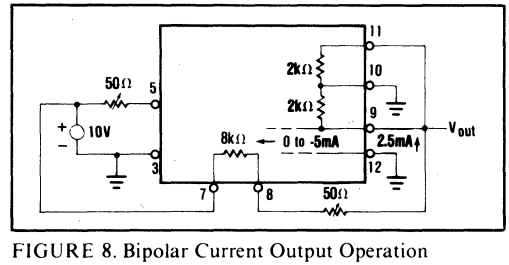


FIGURE 8. Bipolar Current Output Operation Utilizing Internal Resistors.

Gain and offset adjustments are made as described previously except the "+FS" and "-FS" are interchanged and "-FS + 1LSB substituted for +FS -1LSB.

Unipolar and other bipolar ranges may be selected by using an external load resistor as long as the compliance voltage limits, -3.0V to +10V, are observed. To minimize temperature drift when using an external load resistor, (R_2 in Figure 9), an external reference-current-setting resistor should also be used. These two resistors should track over temperature as explained in the section on selecting an external reference on the previous page.

MULTIPLYING MODE OPERATION

DAC10HT can be used as a two-quadrant multiplying D/A converter by applying the analog signal to be processed through a 100Ω potentiometer to the reference voltage input, pin 5. The analog signal must be between 0

and +10V. The output will be an analog signal equal to the product of the input analog signal and the input digital code. DC error of the output signal is less than 0.05% for a reference voltage range of +1V to +10V. For voltages near zero, the error can be quite large (see Figure 2).

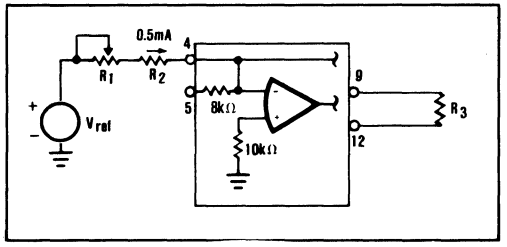
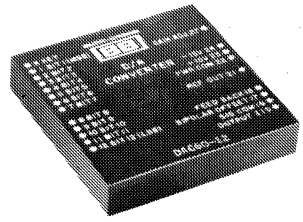


FIGURE 9. Using an External Load Resistor.

HEAT DISSIPATION

The DAC10HT dissipates approximately 430mW (with +5V and -15V power supplies) and the package has a case-to-ambient thermal resistance (θ_{CA}) of 34°C/W. For optimum performance at +200°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. If the converter is mounted on a PC card, improved thermal contact with the copper ground plane under the package can be achieved by using a silicone heat-sink compound.

BURR-BROWN®



DAC60

Ultra-high Speed DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 40nsec SETTLING TIME
- 10- AND 12-BITS
- LOW COST
- MONOTONIC
- 1/2LSB DIFFERENTIAL LINEARITY

DESCRIPTION

The DAC60 is a high speed digital-to-analog converter designed for high speed display applications, for use in high speed A/D converters, and for use as a high speed, precision waveform generator. The DAC60 is available in 10- and 12-bit accuracy. The extremely high speed of the DAC60 is accomplished with low impedance current switching techniques. The typical settling time to 0.05% for an LSB step is 25nsec. The maximum settling time for the major carry or for a full scale transition is only 40nsec to 0.05%. (The major carry is the LSB transition from 011 ... 11 to 100 ... 00).

The DAC60 produces a current output proportional to the digital input. The most significant bit (MSB) produces an output of -2.5mA. The DAC60 is pin-programmable to obtain unipolar or bipolar output signals. The current output may be fed directly into the summing junction of an external high speed operational amplifier, or onto an external summing resistor. An internal 2kΩ feedback resistor is included in the DAC60 for use with an external operational amplifier. This resistor provides voltage output ranges of 0 to +10V or ±5V and compensates for temperature drift of the DAC60.

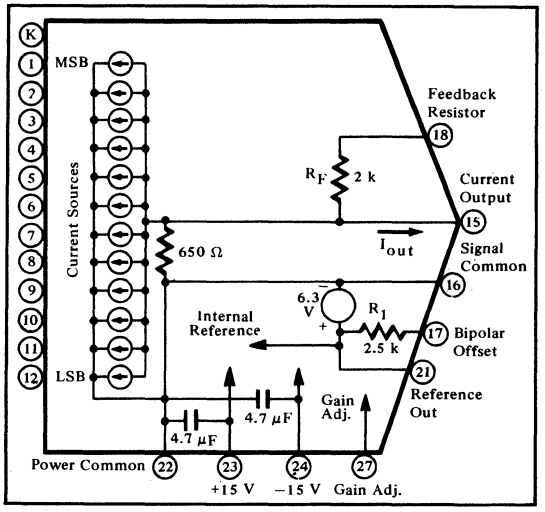
International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

Specifications typical at 25°C and with rated supply unless otherwise noted.

ELECTRICAL

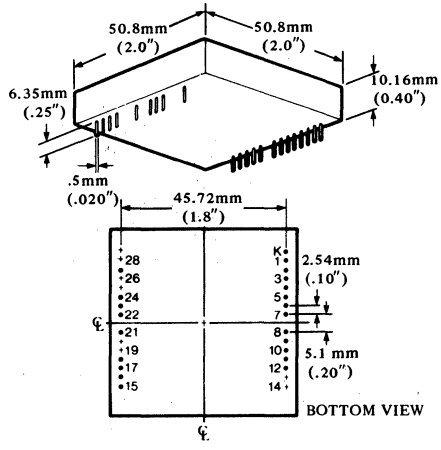
MODEL	DAC60
DIGITAL INPUTS	**10 Bits and 12 Bits**
Data Input Codes	TTL/DTL Compatible Complementary Logic
TRANSFER CHARACTERISTICS	
ACCURACY	
Linearity Error	±1/2 LSB
Differential Linearity Error (max)	±1/2 LSB
Gain Error (adjustable to zero)	±0.05% of FSR (3)
Offset Error (adjustable to zero)	
Unipolar	±0.001% of FSR
Bipolar	±0.05% of FSR
ACCURACY DRIFT	
Voltage Output (1)	±15 ppm/°C
Current Output	±30 ppm/°C
Differential Linearity Error (0° to +70°C)	
10 bits	±1/2 LSB
12 bits	±1 LSB
Monotonicity (0° to +70°C)	Guaranteed
CONVERSION SPEED	
Settling Time for 1 LSB Change (2)	
to 0.05%	25 ns
to 0.0125%	40 ns
for full scale change or major carry change	
to 0.05% (max)	40 ns
to 0.0125%	150 ns
POWER SUPPLY SENSITIVITY (4)	
±15 Volt Supply	±0.002 %/% P.S. Change
OUTPUT	
Unipolar Output Range (5)	0 to -5 mA
Compliance	3.2 V
Output Impedance	650 Ω
Bipolar Output Range (5)	±2.5 mA
Compliance	0.70 V
Output Impedance	516 Ω
POWER SUPPLY REQUIREMENTS	
Rated Power Supplies	±15 V
Power Supply Range	±14.5 to ±15.5 V
Supply Drain (max)	+45 mA, -35 mA
TEMPERATURE RANGE	
Specification	0° to +70°C.
Operating (reduced specs)	-25°C to +85°C
Storage	-55°C to +100°C



Simplified DAC60 Schematic.

MECHANICAL

Dimensions in parentheses are in inches.



Material
Case - Diallyl Phtalate Shell
"Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)."
Connector - 2301MC
or - 2302MC

(1) When in the voltage output mode using an external op amp and the internal feedback resistor as shown in figure 1.
(2) For any data change not involving the four most significant bits.
(3) FSR is Full Scale Range (5 mA).
(4) The percent change in the output level with a one percent change in power supply voltage.
(5) The unipolar output may be fed into a resistive load providing a 3.2 volt or less swing. It is recommended that the bipolar output be fed into the summing junction of an op amp or a resistive load low enough to limit the swing to less than 100 mV.

DEFINITION OF SPECIFICATIONS

DIFFERENTIAL LINEARITY ERROR

The differential linearity of the DAC60 is ±1/2 LSB. This means that any 1 LSB digital input change will produce an output change of 1 LSB ±1/2 LSB (1/2 LSB to 3/2 LSB). This specification is especially important in CRT display systems because the eye is sensitive to differential linearity errors greater than ±1/2 LSB.

LINEARITY ERROR

Linearity error is the deviation of any output state from an ideal straight line drawn between the end points (all bits ON and all bits OFF)

MONOTONICITY

The DAC60 is guaranteed to be monotonic over 0 to 70°C. This means that the output will never decrease for an increase in the digital input.

COMPLIANCE

The compliance voltage of the DAC60 is the maximum voltage swing allowed on the current output node in order to maintain the specified accuracy; it is 0.70 volts for the bipolar current range of ±2.5 mA and is 3.6 volts for the unipolar current range of 0 to -5 mA. The maximum safe voltage swing allowed with no damage to the DAC60 output is ±5 volts.

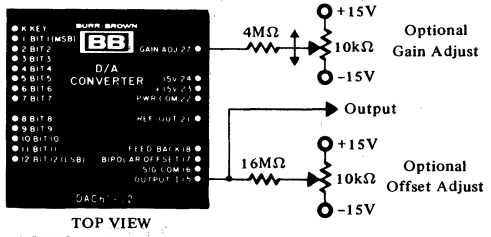
DEFINITION OF DIGITAL INPUT CODES

The DAC60 is available with complementary binary coding. The user may pin strap the output for bipolar complementary offset binary or unipolar complementary straight binary.

INPUT		OUTPUT CURRENT(1)		OUTPUT VOLTAGE(2)		OUTPUT VOLTAGE(3) when driving 50 Ω
MSB	LSB	BIPOLAR	UNIPOLAR	BIPOLAR	UNIPOLAR	UNIPOLAR
111 ...	111	+2.5 mA	0 mA	-5.0 V	0.0 V	0.00 mV
011 ...	111	0 mA	-2.5 mA	0.0 V	+5.0 V	-116.07 mV
000 ...	000	-(2.5 mA -1 LSB)	-(5 mA -1 LSB)	+5.0V -1 LSB	+10.0V -1 LSB	-(232.14 mV -1 LSB)
One LSB						
10 bits		4.88 μA	4.88 μA	9.76 mV	9.76 mV	0.227 mV
12 bits		1.22 μA	1.22 μA	2.44 mV	2.44 mV	0.057 mV

(1) Short circuit current
(2) Op-Amp output when driving summing junction and using the internal R_F (see Figure 1)
(3) See Figures 2 and 3.

INSTALLATION AND OPERATING INSTRUCTIONS



TOP VIEW
Optional GAIN and OFFSET Adjustments

- BIPOLAR OFFSET, pin 17, should be connected to I OUTPUT, pin 15, for bipolar operation or to POWER COMMON, pin 22, for unipolar operation.
- GAIN Adjustment Range: ±0.15% of FSR
- Offset Adjustment Range: ±0.15% of FSR
- If the GAIN ADJUST is not used, leave pin 27 open.
- REF OUT, pin 21 may be used to provide a low drift (5 ppm/°C) reference for external circuitry as long as less than ±100 μA is drawn from it.
- Internal 4.7 μF bypass capacitors between the ±15 Vdc power inputs and ground are included so that the DAC60 does not require external bypass capacitors.
- Both the DAC60-10 and DAC60-12 provide 12 digital inputs. Digital inputs that are not used should be tied to "1" (+5 volts). (Bits 11 and 12 on the DAC60-10 should be tied to +5 V if not used.)

INTERNAL FEEDBACK RESISTOR

Burr-Brown includes a 2 kΩ feedback resistor in the high speed resistor network (pin 18). The feedback resistor's temperature coefficient of resistance (TCR) is matched with that of the resistor network. Since the TCR of the resistor network contributes much of the current output drift of the DAC60, use of the feedback resistor with an external op amp reduces the effective drift of the voltage output. This is why the voltage output drift in the electrical specifications table is significantly better than the current output drift.

OPTIONAL OPERATING CONFIGURATIONS

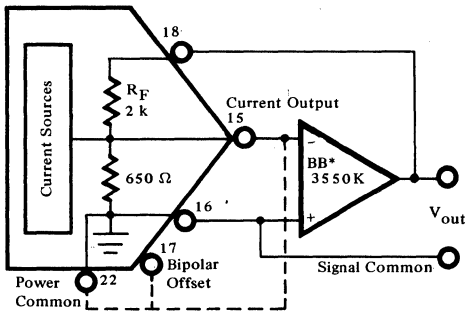
DRIVING AN OP AMP SUMMING JUNCTION

The DAC60 will drive the summing junction of an op amp (op amp being used as a current to voltage converter) to produce an output voltage:

$$V_{OUT} = -(I_{OUT})(R_F)$$

where I_{OUT} is the DAC60 short circuit output current and R_F is the op amp feedback resistor. Use of the internal feedback resistor (pin 18) will result in a 0 to +10 volt or ±5 volt output range. A 16 kΩ feedback resistor would produce output ranges of 0 to +50 volts or ±25 volts.

Use of the internal 2 kΩ feedback resistor will result in output voltage drifts as indicated in the specification table because the internal R_F drift is matched to that of the current sources. When using external feedback resistors, their temperature coefficient of resistance (TCR) should be directly added to the current output drift of the DAC60 to obtain the drift of the voltage output.



* Burr-Brown's 3400, 3401 and 3402 may also be used.

FIGURE 1. Driving an op amp summing junction.

DRIVING A RESISTIVE LOAD

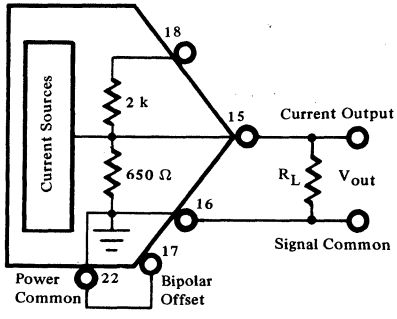


FIGURE 2. Driving a resistive load.

When driving a resistive load, the voltage output of the DAC60 is the short circuit output current times the equivalent load resistance. The DAC60 output impedance is approximately 650 ohms (in parallel with the load resistance, R_L). The output voltage is:

$$V_{OUT} = (I_{OUT})\left(\frac{R_L \times 650\ \Omega}{R_L + 650\ \Omega}\right)$$

With an R_L of 100 kΩ or higher, the full scale output voltage will be approximately 3.2 volts. An R_L of 300 ohms will provide a full scale output voltage of approximately 1 volt.

NOTE: For bipolar use, the output voltage should be less than 700 mV for acceptable output accuracy.

DRIVING A CABLE

The DAC60 can drive long lengths of cable with a circuit as shown in Figure 3. With just the 93 ohm terminating resistor used, the full scale output will be approximately 500 mV. The 120 ohm resistor across pins 15 and 16 will minimize output re-reflections due to mismatches between the characteristic impedance of the cable and the output impedance of the DAC60. The reflection factor of a cable is $\frac{Z_O - Z_t}{Z_O + Z_t}$ where Z_O is the characteristic impedance of the cable and Z_t is the termination resistance. A 1% mismatch between Z_O and Z_t will reflect back 1% of the output voltage to the cable input where the termination resistance normally seen is the 650 ohm output impedance of the DAC60. The reflection factor at the cable input would then be .75. The 120 ohm resistor reduces this reflection factor to 0.06 and significantly reduces glitches caused by reflections. Of course the 120 ohm resistor will reduce the full scale output voltage to about 250 mV.

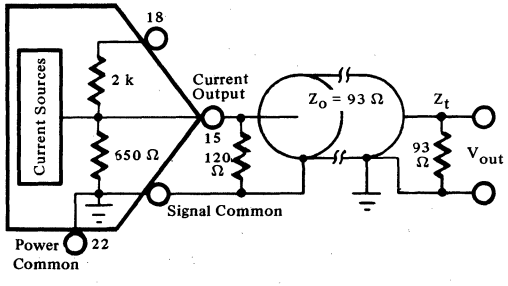


FIGURE 3. Driving a cable.

APPLICATIONS

DEGLITCHED VOLTAGE OUTPUT

Output transients when switching from one state to another are always a problem with high speed D/A converters. These transients, sometimes called glitches, are the result of unequal turn on and turn off times of the digital and analog components. A major contributor to glitch amplitude for the DAC 60 is the data skew of the digital inputs. Data skew is the time difference between the time one bit input changes state to the time other bit inputs change state. With data skew of less than 2 nanoseconds the DAC60 glitch area will typically be 25 picoamp seconds.

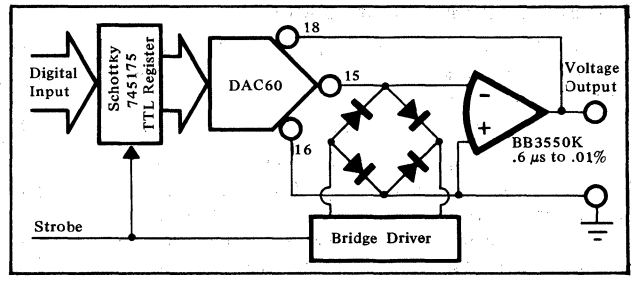


FIGURE 4. Deglitcher on DAC60 Output.

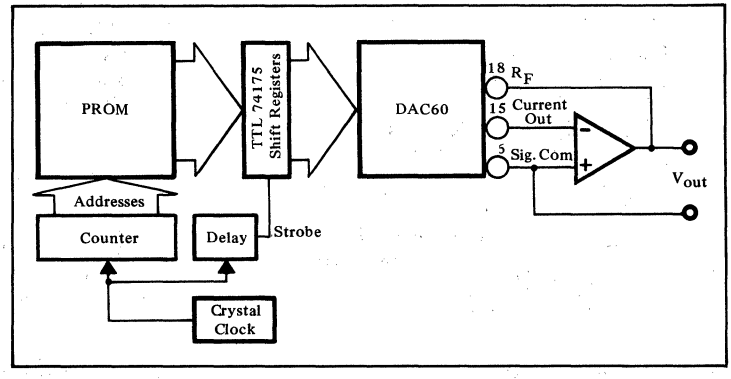
If a high speed amplifier, such as BB Model 3550 is used on the DAC60 output, a bridge clamping circuit on the summing junction will reduce the glitch amplitude. The deglitching bridge and bridge driver should be connected as shown in Figure 4. A high speed Schottky digital storage buffer should be used to reduce skew to 2 nanoseconds or less.

The deglitcher performance depends on the switching speed and matching of the bridge diodes. The bridge essentially clamps the summing junction near ground, preventing voltage glitches from appearing at the amplifier output. This technique can essentially eliminate or significantly reduce glitch amplitudes to 5 LSB or less at the output.

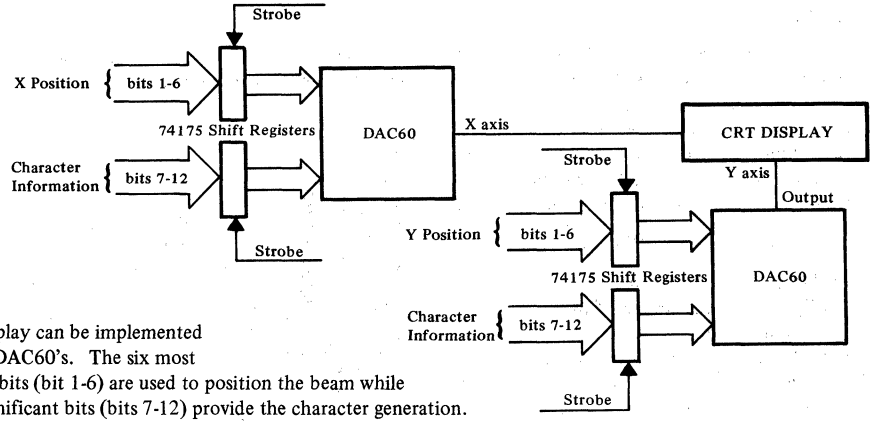
WAVEFORM GENERATORS

The DAC60 may be used as a high speed, precision signal generator with the help of a programmable read-only memory.

The counter updates the PROM addresses once each clock cycle. The delay provides a strobe pulse for the shift register when the PROM outputs have settled to a new word. This circuitry may be programmed to provide almost any complex, high speed waveform with up to 0.01% accuracy.

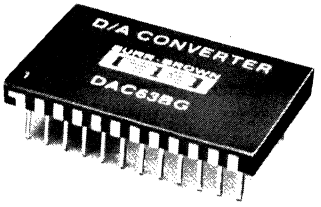


CRT DISPLAY CHARACTER GENERATOR



A CRT display can be implemented using two DAC60's. The six most significant bits (bit 1-6) are used to position the beam while the less significant bits (bits 7-12) provide the character generation.

BURR-BROWN®



DAC63

Ultra-High Speed DIGITAL-TO-ANALOG CONVERTER

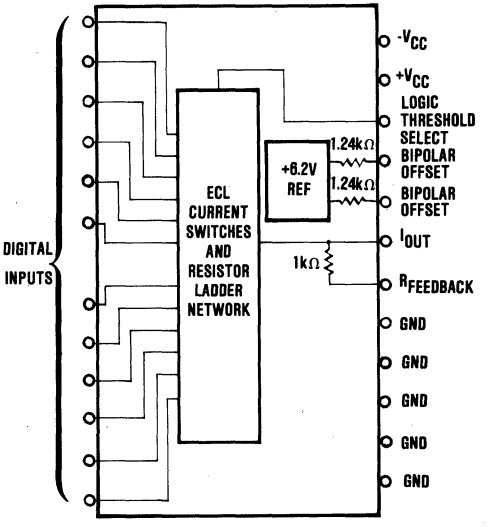
FEATURES

- 12-BIT RESOLUTION AND ACCURACY
- 35nsec SETTLING TIME
- ECL-COMPATIBLE INPUTS
- LOW GLITCH ENERGY
- ±30ppm/°C MAX GAIN DRIFT
- LINEARITY ERROR LESS THAN ±1/2LSB OVER SPECIFIED TEMP RANGE
- ADJUSTABLE LOGIC THRESHOLD FOR IDEAL SWITCHING
- INTERNALLY-BYPASSED SUPPLY LINES TO MINIMIZE SETTLING TIME
- INTERNAL FEEDBACK RESISTOR FOR EXCELLENT THERMAL TRACKING

DESCRIPTION

The DAC63 is an ultra-fast-settling 12-bit current output D/A converter in a 24-pin dual-in-line ceramic bottom-brazed package. The inputs are ECL-compatible and the output settles in 35nsec, typ (45nsec, max) to within ±0.012% of full scale range. The DAC63 utilizes a monolithic 12-bit switch chip and a stable thin-film-on-sapphire resistor network to achieve fast settling time and excellent stability over temperature and time. Because of the close thermal tracking of the current-switching transistors (all on one monolithic chip) the possibility of thermal-tail settling time problems is eliminated. An internal applications resistor for use with an external output op amp is included to convert the output current into a voltage. It is on the same chip as the ladder network to insure excellent tracking and therefore lower drift. The linearity is guaranteed to be within ±1/2LSB over the specified temperature range of -25°C to +85°C. Gain drift is ±30ppm/°C max and bipolar offset drift is ±10ppm of FSR/°C max (CG model). Also included internally is a +6.2V reference. An output voltage compliance range of +2.0V to -0.5V allows the generation of an output voltage without using an external output amplifier.

FUNCTIONAL DIAGRAM



DAC63

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

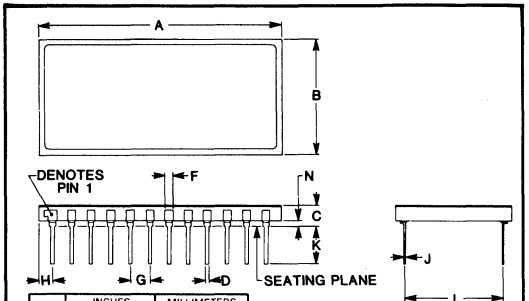
At +25°C and rated supplies unless otherwise noted.

MODEL	DAC63CG			DAC63BG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			12			12	Bits
Logic Inputs(1)		ECL-compatible			ECL-compatible		
Logic "1", Voltage	-0.78	-0.90	-0.96	-0.78	-0.90	-0.96	V
Current	6.0		33.0	6.0		33.0	µA
Logic "0", Voltage	-1.62	-1.75	-1.85	-1.62	-1.75	-1.85	V
Current		10.0			10.0		nA
Logic Threshold, Voltage	-1.20	-1.33	-1.40	-1.20	-1.33	-1.40	V
Current			0.25			0.25	mA
TRANSFER CHARACTERISTICS							
ACCURACY(2)							
Linearity Error			±0.012			±0.012	% of FSR(3)
Differential Linearity Error			±0.012			±0.012	% of FSR
Gain Error		±0.02	±0.1		±0.02	±0.1	%
Offset Error, Unipolar		±0.01	±0.04		±0.01	±0.04	% of FSR
Bipolar		±0.02	±0.1		±0.02	±0.1	% of FSR
Monotonicity Temp. Range (min)	-25		+85	-25		+85	°C
CONVERSION SPEED(4)							
Settling Time to ±1/2LSB into 150Ω							
For FSR Change		35	45		35	45	nsec
For 1LSB Change		20			20		nsec
Glitch Energy(5)		250			250		LSB-nsec
DRIFT(-25°C to +85°C)							
Gain		±15	±30		±20	±40	ppm/°C
Offset, Unipolar		±0.3	±0.6		±0.5	±1	ppm/°C
Bipolar			±10			±15	ppm/°C
Total Linearity Error	±0.012 over -25°C to +85°C			±0.025 over -25°C to +85°C			% of FSR
Total Differential Linearity Error	±0.025 over -25°C to +85°C			±0.05 over -25°C to +85°C			% of FSR
Drift (long term, linearity)		±2			±2		ppm/month
OUTPUT							
ANALOG OUTPUT							
Output Current		0 to -10, ±5			0 to -10, ±5		mA
Output Voltage Ranges							
with External Op Amp		0 to +10, ±5			0 to +10, ±5		V
without External Op Amp		0 to+1.5,±0.5			0 to +1.5, ±0.5		V
Output Impedance							
without External Op Amp							
Unipolar, Positive		150			150		Ω
Negative		200			200		Ω
Bipolar		170			170		Ω
Compliance Voltage	-0.5		+2.0	-0.5		+2.0	V
POWER SUPPLIES AND REFERENCE							
Internal Reference Voltage		+6.2			+6.2		V
Internal Reference Drift		±15			±15		ppm/°C
Power Supply Voltages	±13	±15	±18	±13	±15	±18	V
Power Supply Current							
+15V		26	31		26	31	mA
-15V		38	46		38	46	mA
Power Supply Sensitivity							
+15V		±0.0035			±0.0035		%/%ΔV
-15V		±0.0004			±0.0004		%/%ΔV
Power Dissipation		960	1160		960	1160	mW
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification	-25		+85	-25		+85	°C
Operating (derated specs)	-55		+100	-55		+100	°C
Storage	-55		+125	-55		+125	°C
PACKAGE	24-pin DIP bottom-brazed ceramic						

NOTES:

1. Logic input voltages and currents are dependent on the logic threshold voltage. The logic input values given in each column are correct for the logic threshold voltage given in that column.
2. When used with an external output op amp.
3. FSR is Full Scale Range, which is 10mA for both the DAC63BG and DAC63CG.
4. Refer to description of settling time measurement.
5. Refer to Output Glitch section.

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.280	1.310	32.51	33.27
B	.780	.800	19.81	20.32
C	.153	.207	3.89	5.26
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.087	.091	2.21	2.31
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.600 BASIC		15.24 BASIC	
N	.015	.035	.38	.89

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (.25MM) R@MMC AT SEATING PLANE

PIN ASSIGNMENTS

Pin No.	Function
1	Bit 1 (MSB)
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7
8	Bit 8
9	Bit 9
10	Bit 10
11	Bit 11
12	Bit 12 (LSB)
13	GND
14	GND
15	GND
16	GND
17	GND
18	Feedback Resistor Connection
19	Current Output
20	Bipolar Offset
21	Bipolar Offset
22	Logic Threshold
23	+15VDC
24	-15VDC

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a D/A converter is one of the true measures of its performance. The linearity error of the DAC63 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB (±1LSB for the BG model), from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of -25°C to +85°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a -25°C to +85°C and -55°C to +125°C range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for the DAC63 at T_{min}, +25°C, and T_{max}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications (includes internal reference).

Offset Drift is a measure of the actual change in output around zero over the specified temperature range. The offset is measured at T_{min}, +25°C, and T_{max}. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of the DAC63 is +2.0V and -0.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages. To insure precision operation, each supply lead should be bypassed to ground as close to the unit as possible with a 1μF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC63 (pins 13, 14, 15, 16, and 17). In order to preserve the stated linearity and accuracy specifications it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these five pins and the actual ground reference point will degrade the performance of the DAC63. To achieve fast settling performance it is recommended that pins 13 through 17 be returned directly to a ground plane (see Figure 1). The

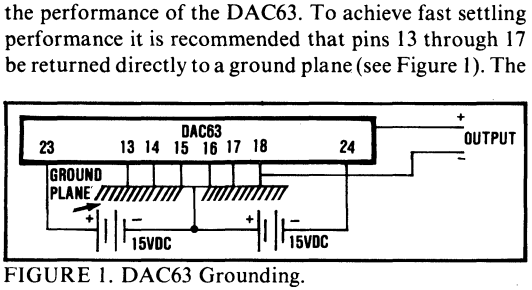


FIGURE 1. DAC63 Grounding.

analog ground should be located as close to the DAC63 as possible. Otherwise, the accuracy will be degraded by the voltage drop in the ground lines.

DIGITAL INTERFACE, LOGIC THRESHOLD, AND NOISE IMMUNITY

The DAC63 is compatible with conventional ECL logic families such as ECL 10,000. The circuit diagram shows that the equivalent circuit of each DAC63 digital input is the base of one side of a differential amplifier. The logic 1 input voltage is -0.85V with a typical input current of 8μA. The logic 0 input voltage is -1.75V with an input current of less than 8nA.

The Logic Threshold function of the DAC63 is very important in dealing with noise in the ECL input-driving circuitry. The ECL 10,000 logic family has a noise immunity of 125mV maximum. It has a temperature coefficient of -1.4mV/°C and a power supply sensitivity of 16mV/%ΔV. With a realistic condition of a 5% power supply variation and a 25°C temperature change, the noise immunity would be degraded to 10mV. In addition, a precision D/A converter is more susceptible to noise than is the ECL logic. Noise at levels acceptable to the logic can couple through the D/A resulting in an unacceptably noisy output.

Through the logic threshold input, the threshold voltage of the DAC63 is dynamically adjusted as the temperature and power supplies vary to give maximum noise immunity at the analog output over a wide range of conditions.

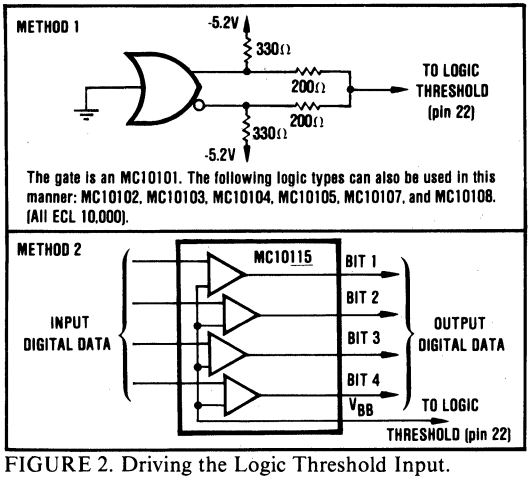


FIGURE 2. Driving the Logic Threshold Input.

If an MC10115 line receiver (or similar logic function) is used to drive the DAC63 input, the logic threshold pin can be driven by the V_{BB} output of the ECL gate. Refer to an ECL 10,000 data book for more detail. Figure 2 shows alternate methods for generating the drive signal for logic threshold, pin 22.

SETTLING TIME

Settling time for the DAC63 is the total time required for the output to settle within an error band around its final value after a digital input change. This time includes the digital delay of the internal switches.

The settling time of the DAC63 is determined indirectly because of the effect of test equipment error on the final measurement. The test equipment must be "calibrated" by measuring the settling time of the instrumentation using a pair of hot carrier diodes in place of the DAC63. The switching time of the hot carrier diodes is negligible and therefore the settling time of the instrumentation can be observed. The settling time measurement is made by amplifying the output of the DAC63 and displaying the output on a sampling scope. The settling time of the

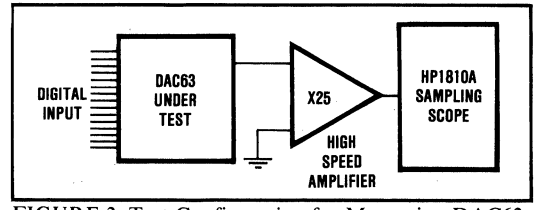


FIGURE 3. Test Configuration for Measuring DAC63 Settling Time.

DAC63 is determined mathematically in the following way:

$$t_{DAC} = \sqrt{(t_{measured})^2 - (t_{instrumentation})^2}$$

where

$t_{instrumentation}$ = settling time observed using hot carrier diodes in place of DAC63

$t_{measured}$ = settling time observed with the DAC63

t_{DAC} = actual settling time of the DAC63

A typical example of this settling time measurement procedure follows. A test configuration shown in the block diagram of Figure 3 is used. The high speed amplifier has a gain of 25. The amplifier schematic is shown in Figure 4.

The settling time of the amplifier is determined to be 20nsec which is reasonably in agreement with its bandwidth characteristic -- a 3-pole response with a -3dB point at 120MHz. After making the measurements, the DAC63 settling time is determined.

$t_{instrumentation}$ = 20nsec

$t_{measured}$ = 40nsec

$t_{DAC} = \sqrt{(40)^2 - (20)^2}$

= 35nsec

Figure 5 shows a typical settling time curve of the DAC63 versus output error. This curve is for full-scale digital code changes. Figures 6 and 7 are photographs showing typical measured settling time characteristics of the DAC63. This is the "$t_{measured}$" as given above.

In order to achieve a clean response it is necessary to observe the following good high frequency construction techniques:

1. The power supplies, including the logic threshold input (pin 22), should be bypassed by 1μF CS-type tantulum capacitors.
2. Use a ground plane to connect common ground points.
3. Remove the ground plane from underneath signal lines where it would add capacitance.

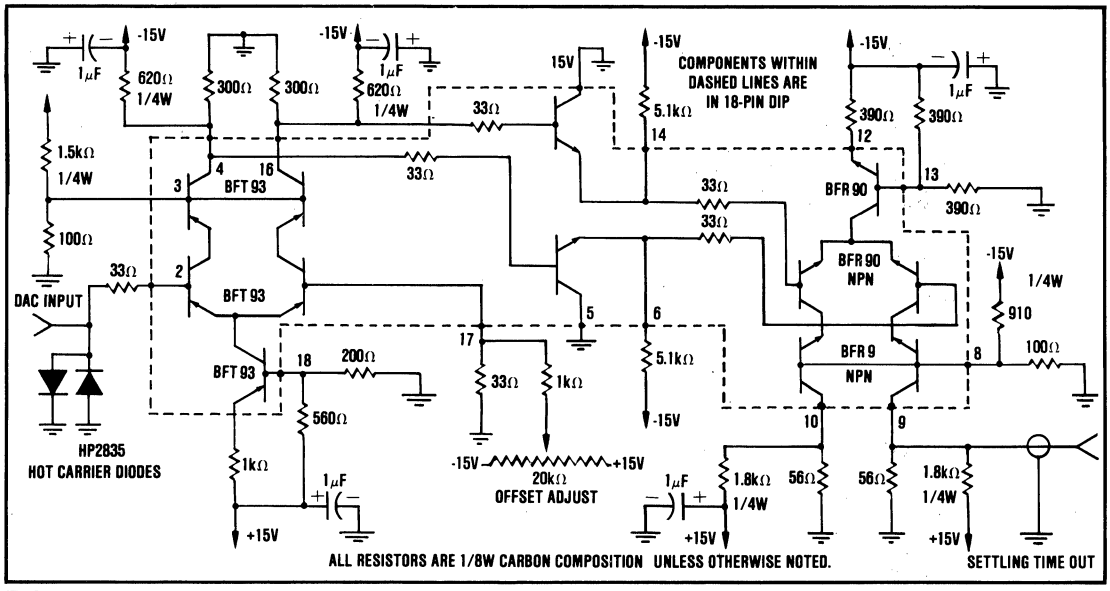


FIGURE 4. Schematic of Fast Settling Time Amplifier.

4. Separate analog and digital signal leads to avoid coupling of the digital signal into the analog paths.
5. Bring the source of the digital driving signal as close to the inputs of the DAC63 as possible. If the digital inputs are not clean it will be necessary to reshape them using registers or line drivers. Figure 9 shows how to interface the DAC63 to an input register. It is recommended that the logic power line be bypassed near the digital logic circuitry as a further measure to achieve clean signals.
6. If possible, the DAC63 should be soldered directly into the printed circuit board since connector lead length will cause ringing in the output.

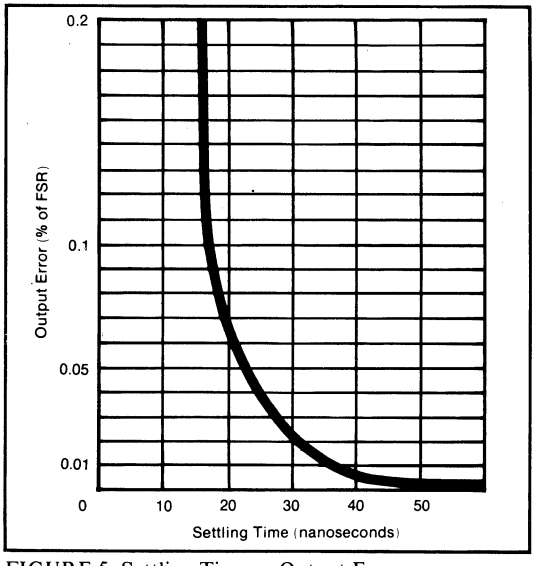


FIGURE 5. Settling Time vs Output Error.

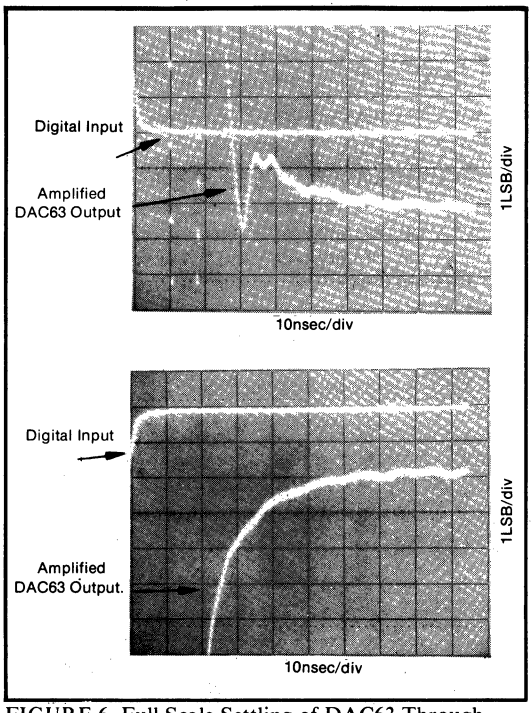


FIGURE 6. Full Scale Settling of DAC63 Through Amplifier.

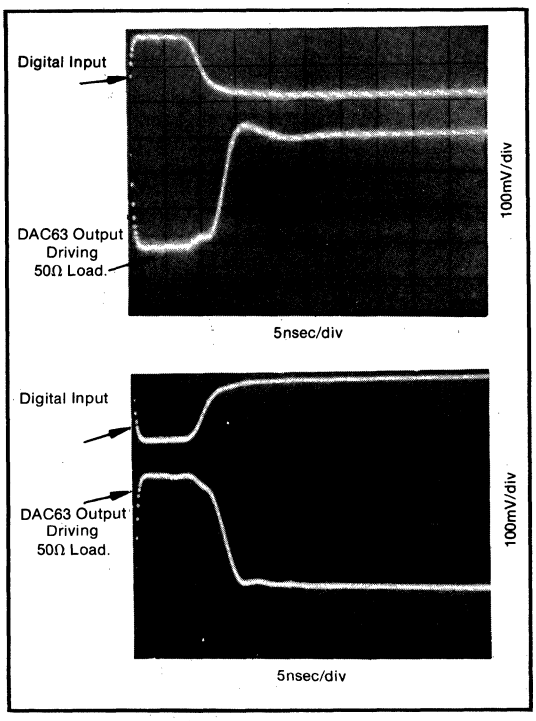


FIGURE 7. Full Scale Settling of DAC63 into 50Ω Load.

OUTPUT GLITCH

"Glitch" is defined as the difference in the waveforms at the output of the DAC if there is data skew and if there is not. The measurement of glitch is accomplished by measuring the area between these two waveforms.

An output glitch of less than 250LSB-nsec is achievable with the DAC63 because it employs ECL circuitry with current switches that have virtually identical delay times for logic signals making either positive or negative transitions. A glitch results when the digital data changes from one code to the next and the bits do not all switch at the same time. The delay time between the earliest and latest switching bits is called skew time. Typically during the skew time of the digital data, which includes the DAC switching, the digital code is undefined and the DAC output can go to any voltage between the full scale extremes. The glitch creates a noisy output which can be troublesome in some applications such as precision displays and complex waveform generation. Figure 8 is a photograph of a scope trace of the DAC output with a glitch occurring at the major carry transition.

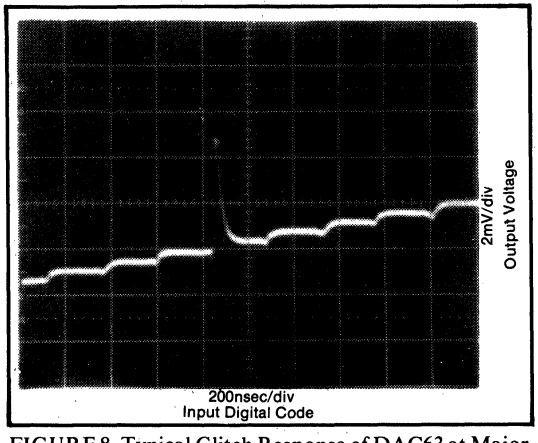


FIGURE 8. Typical Glitch Response of DAC63 at Major Carry Transition with a 1.6V Full Scale Range.

The DAC63 design has been optimized for low glitch energy. However, a further reduction in the output glitch can be achieved by adjusting the skew of the higher order bits of the driving circuitry and by adjusting the logic threshold. This can be done by connecting a variable capacitor from the data lines to ground on each of the first three significant bits (more than three lines may be adjusted if desired). Refer to Figure 9. It will be necessary to create a driving digital code pattern that causes a major carry transistion around these bits. It is convenient to use a digital ramp from a counter for this purpose. Initially set the logic threshold exactly half-way between logic 1 and a logic 0. This will be about -1.3V. Then examine the major carry transition associated with bit 3 and adjust the capacitor for minimum glitch. Make the same adjustment to bit 2 and then to bit 1. If done in this order, interactions will be minimized. Finally, fine tune the response by adjusting the logic threshold voltage (pin 22) for minimum glitch. It may be necessary to repeat this procedure once or twice for complete optimization.

OUTPUT CONFIGURATIONS AND APPLICATIONS INFORMATION

The DAC63 contains two 1.24kΩ resistors for generating the bipolar offset current and a 1kΩ resistor which is primarily used as the feedback resistor when used with an external op amp. This thin-film network is constructed on sapphire to provide excellent temperature tracking capability inherent in thin-film networks. These internal resistors along with other internal resistors cause the DAC63 output, in any mode, to be a ratiometric product of the reference. The feedback resistor has very low power sensitivity so that linearity is maintained independent of digital code changes. Because this resistor is constructed on a sapphire network it is possible to have both superior tracking and low capacitance. Figure 10 shows the DAC63 connected to an external op amp in unipolar and bipolar modes. When the op amp is a Burr-Brown model OPA600 it is possible to achieve settling times to ±0.01% accuracy in 150nsec. Many of the output accuracy and linearity specifications are given when connected to an external op amp.

For highest speed operation, the DAC63 should be used without an external op amp. Figures 11 and 12 show how to connect the DAC63 for bipolar and positive unipolar

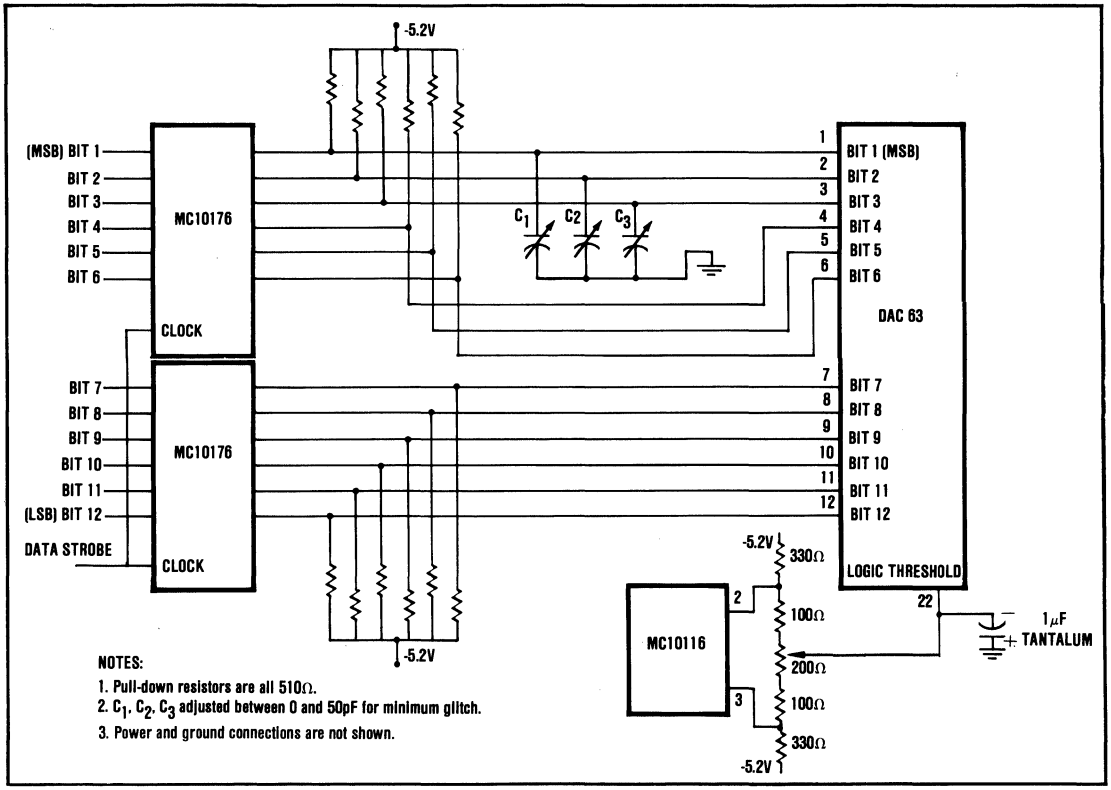
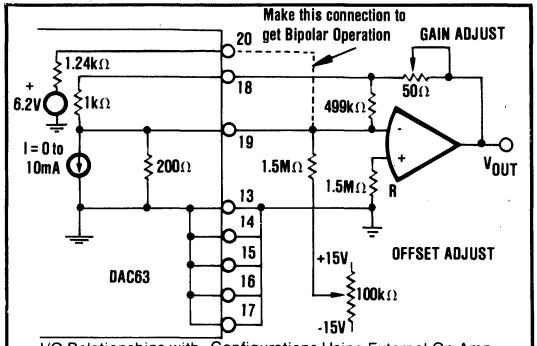


FIGURE 9. Glitch Adjustment.

operation. Figure 13 illustrates how to connect the DAC63 to construct a fast A/D converter. The ADC attempts to create a null at the DAC output, so it is possible to clamp the output voltage with a pair of diodes, thereby avoiding the negative compliance limit.



I/O Relationships with Configurations Using External Op Amp

		Unipolar	Bipolar
Digital Codes vs Output Voltage	111111111111	0.0000V	-5.0000V
	011111111111	5.0000V	0.0000V
	000000000000	9.9976V	4.9976V
R Value	R	169Ω	147Ω
Pin 20 Connection		Open	Connect to Pin 19

FIGURE 10. Bipolar and Unipolar Output Connections when Used with External Op Amp.

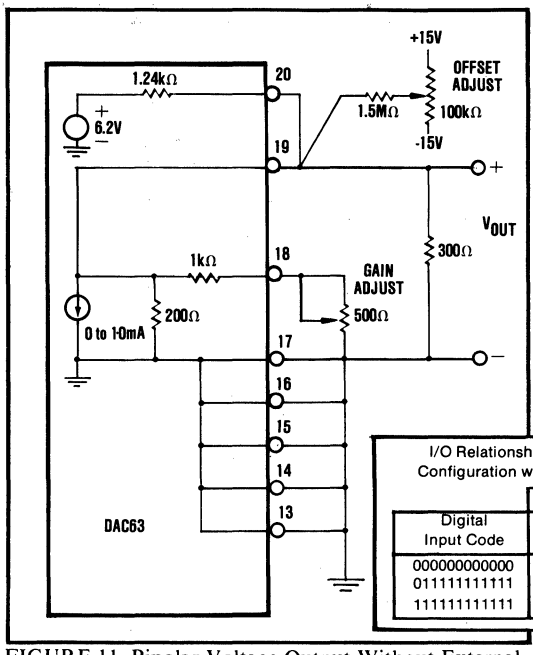


FIGURE 11. Bipolar Voltage Output Without External Op Amp.

I/O Relationships for Voltage Output Configuration without External Op Amp

Digital Input Code	Output Voltage: Positive Unipolar	Output Voltage: Bipolar
000000000000	0.0000V	-0.500V
011111111111	0.7500V	0.000V
111111111111	1.4996V	0.500V

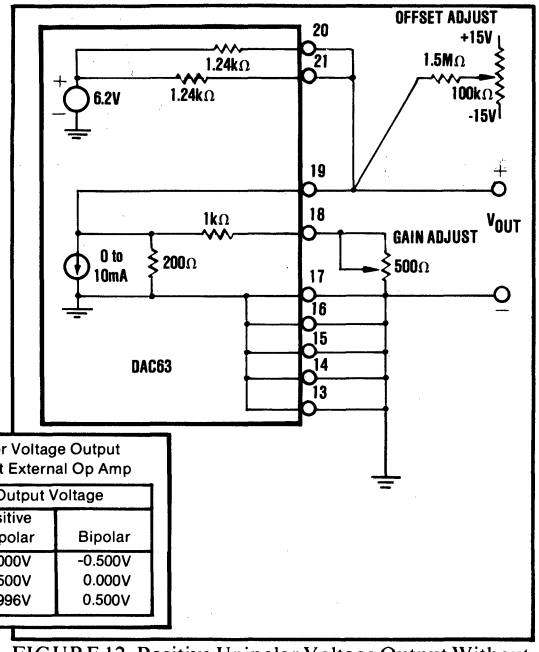


FIGURE 12. Positive Unipolar Voltage Output Without External Op Amp.

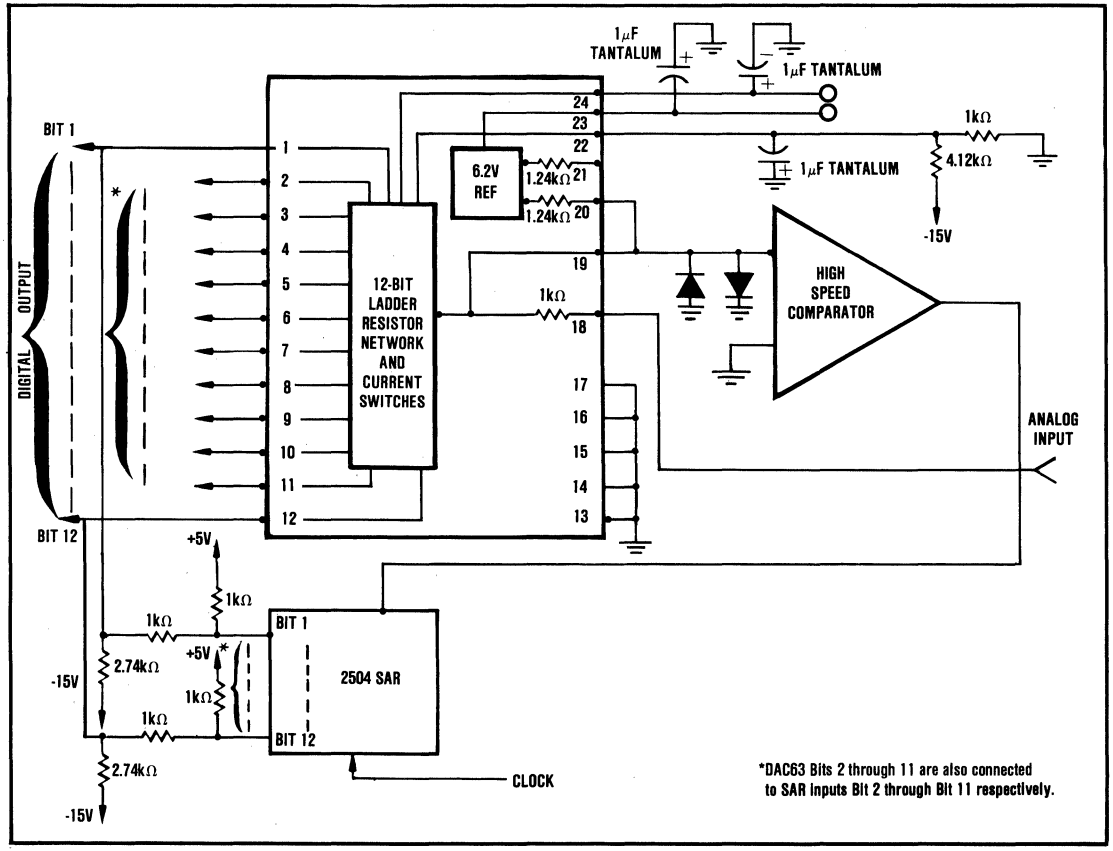
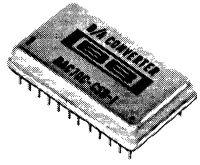


FIGURE 13. DAC63 Used in a Fast A/D Converter.

BURR-BROWN®



DAC70

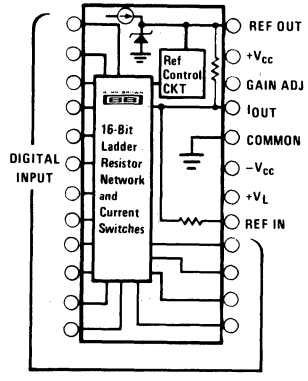
High Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

PROVIDES ACCURATE ANALOG SIGNALS
- EXCELLENT FOR CALIBRATION STANDARD AND HIGH RESOLUTION APPLICATIONS
  - 16-bit resolution
  - Laser-trimmed to ±0.003% maximum nonlinearity
  - Ultra-low drift - ±4ppm/°C, max

SMALL SIZE SAVES SPACE AND WEIGHT
- Hermetic Dual-in-line Package
- Low Cost

FUNCTIONAL DIAGRAM



DESCRIPTION

The DAC70 is a high quality 16-bit hybrid IC D/A converter in a 24-pin DIP-compatible hermetic metal package. Constructed with laser-trimmed and drift-matched thin-film resistor network and fast-settling bipolar IC current switches, the DAC70 settles in 50μsec to a maximum nonlinearity of ±0.003% of full scale range (FSR) and has a very low maximum gain drift of ±4ppm/°C over 15°C to 50°C. Three basic models accept complementary unipolar or bipolar 16-bit binary or complementary 4-digit BCD TTL-compatible input codes. Each model is available in two grades of drift, linearity and operating temperature range. The Model DAC 70 (-25°C to +85°C) offers ±0.003% of FSR maximum nonlinearity and ±7ppm/°C maximum gain drift. The Model DAC70C (0°C to +70°C) offers ±0.005% of FSR maximum nonlinearity and ±14ppm/°C maximum gain drift.

These units provide output current signals of ±1mA or 0 to -2mA, and contain the scaling resistors for connecting an external amplifier to provide 0 to +10V (CSB, CCD) or ±10V (COB) output voltage ranges. Input power is ±15VDC and +5VDC.

Excellent stability, long life and quality product performance is assured because each DAC70 is burned-in for 96 hours at +100°C. Calibration equipment used to test the DAC70 is traceable to the National Bureau of Standards.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-332C

SPECIFICATIONS

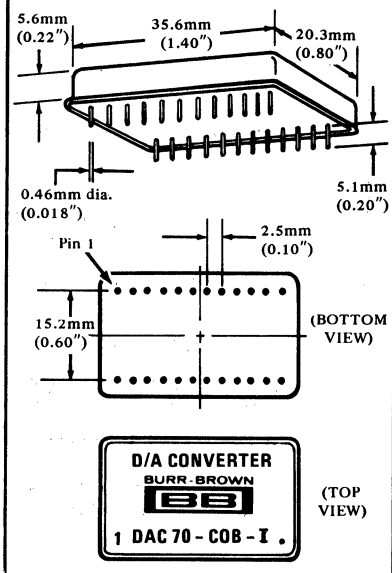
ELECTRICAL

(Typical at 25°C with rated power supplies unless otherwise noted.)

MODEL	DAC70	DAC70C	UNITS
INPUT			
DIGITAL INPUTS	TTL/DTL Compatible		
Data Input Codes	Complementary: 16 bit Binary/ 4 digit BCD		
Logic Levels(1)			
Logic "1"(2)	$+2.4 < e_d < +5.0$		V
Logic "0"(3)	$0 < e_d < +0.4$ max @ 1.0mA sink		V
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Linearity Error (max)	±0.003	±0.005	% of FSR(4)
Gain Error, (max)(5)	±0.05		%
Offset Error, (max)(5)	±0.05		% of FSR
Monotonicity Guaranteed (10°C to 40°C)	14	13	bits
DRIFT(4)			
Gain (max) (0°C to +70°C)	---	±14	ppm/°C
(max) (-25°C to +85°C)	±7	--	ppm/°C
(max) (+15°C to 50°C)	±4	±8	ppm/°C
Offset			
Unipolar	±1		ppm of FSR/°C
Bipolar (max)	±5	±10	ppm of FSR/°C
Linearity (max)	±2	± 2	ppm of FSR/°C
SETTLING TIME (6) (to 0.003% FSR)			
Voltage Output(5) (max) 20 V step	100		µsec
.6 mV step	50		µsec
Current Output 2 mA step	50		µsec
Output Switching Transient	500		mV
Slew Rate	1		V/µsec
POWER SUPPLY SENSITIVITY			
Unipolar Offset			
±15 V	±1		ppm of FSR/%
+5 V	±0.1		ppm of FSR/%
Bipolar Offset			
±15 V	±4		ppm of FSR/%
+5 V	±1		ppm of FSR/%
Gain			
±15 V	±10		ppm/%
+5 V	±5		ppm/%
OUTPUT			
ANALOG OUTPUT			
Voltage Mode(7)			
CSB and CCD Models	0 to +10		V
COB Model	±10		V
Output Current (min)	5		mA
Output Impedance (DC)	0.05		Ω
RMS Noise (10 Hz to 10 kHz)	0.003		% FSR
Current Mode			
CSB and CCD Models	0 to -2		mA
COB Model	±1		mA
Compliance(8)	±2.5		V
Output Impedance (DC)			
Bipolar	4.4		kΩ
Unipolar	15		kΩ
INTERNAL REFERENCE VOLTAGE (V_r)	6.3		V
Maximum External Current(9)	200		µA
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15 and +5		V
Range	±14.5 to ±15.5 & +4.75 to +5.25		V
Supply Drain			
±15 V (including 5 mA load)	30		mA
+5 V	25		mA
TEMPERATURE RANGE			
Specification	-25 to +85	0 to +70	°C
Operating (Double above drift specs)	-55 to +100	-25 to +85	°C
Storage	-55 to +125		°C

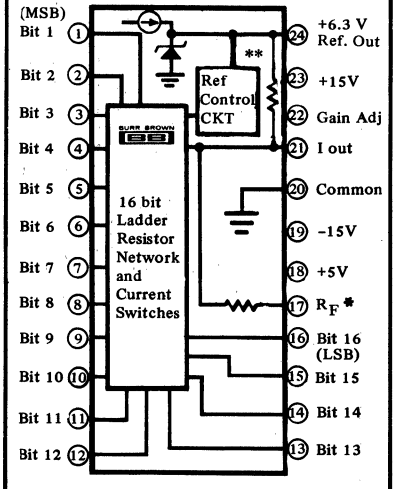
(1) It is recommended that the digital input lines to the DAC70 be drawn from TTL devices (inverters or registers) that drive only the DAC to obtain the specified accuracy.
(2) Logic "1" current = +40µA max at V_{in} = +5.0V.
(3) Logic "0" current = -1.6mA max at V_{in} = +0.4V.
(4) FSR means full scale range and is 20V for ±10V range, 10V for 0 to +10V range, etc.
(5) Gain and offset are externally adjustable to zero (see page 5-52).
(6) Worse case conditions measured at the worst case major carry (mid-scale).
(7) With external Burr-Brown Model 3500C op amp or equivalent, using internal feedback resistors.
(8) The current output should be connected to the virtual ground of an amplifier summing junction to obtain specified accuracy.
(9) With no degredation of specifications.

MECHANICAL



CASE: Kovar
Mating Connector 245MC
PIN: Pin material and plating composition conform to method 2003 (solderabiltiy) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 9 grams (.32 oz)

CONNECTION DIAGRAM



* R_F = 5k (CSB) 10k (COB) 8k (CCD)
** 6.3k Bipolar Offset Resistor (COB only)

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC70 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The COB model may be user connected for either complementary offset binary (COB) or complementary two's complement (CTC) codes as shown in Table I.

DIGITAL INPUT CODES					
	Logic Inputs		CSB	COB	CTC*
	MSB	LSB	Compl. Straight Binary	Compl. Offset Binary	Compl. Two's Complement
CBI Models	All bits OFF	0000 ... 000	+Full Scale	+Full Scale	-1 LSB
	Mid Scale	0111 ... 111	+½Full Scale	Zero	-Full Scale
	All bits ON	1111 ... 111	Zero	-Full Scale	Zero
		1000 ... 000	Mid Scale -1 LSB	-1 LSB	+Full Scale
CCD Models			CCD (Complementary Coded Decimal) 4 Digits		*Invert the MSB of the COB code with an external inverter to obtain CTC code.
	F.S. bits OFF	0110 ... 0110	+Full Scale		
	All bits ON	1111 ... 1111	Zero		

TABLE I. Digital Input Codes.

ACCURACY†

LINEARITY

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.003% of FSR max (DAC 70) or ±0.005% of FSR max (DAC70C) from a straight line drawn through the end points (all bits ON and all bits OFF) at 25°C.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can be anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

MONOTONICITY

Monotonicity over 10 to +40°C is guaranteed in the DAC70. This insures that the analog output will increase or remain the same for increasing 14 bit input digital codes. It is 13 bits over the same temperature range for the DAC70C.

DRIFT†

GAIN DRIFT is a measure of the change in the full scale range analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at -25°C or 0°C, +25°C and +70°C or +85°C for each model and calculating the GAIN ERROR with respect to the 25°C value and dividing by the temperature change. This specification is expressed in ppm/°C and is shown in Figure 1.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in the output with all bits OFF $\left(V_{OUT}^{OFF}\right)$ over the specified temperature range. V_{OUT}^{OFF} is measured at -25°C or 0°C, +25°C and +70°C or +85°C. The maximum charge in OFFSET is referenced to the OFFSET at 25°C divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME†

The settling time for each model DAC70 is the total time (including slew time) for the output to settle to within an error band about its final value after a change in the input. Two settling times are specified to ±0.003% of full scale range (FSR); one for a maximum full scale range change of 20V and also for a 1 LSB change. The 1 LSB change is measured at the major carry (0111 ... 11 to 1000 ... 00) since this is the point where the worst case settling time occurs. This measurement is made with an external BB3500C op amp. (See Figure 3.)

OUTPUT SIGNAL RANGES

For optimum operation and performance to specification, an external operational amplifier (BB Model 3500C) should be used with the DAC70. A laser trimmed low-drift thin film feedback resistor (R_F) is provided in each DAC70 to provide an output voltage range of ±10V for the COB model or 0 to +10V for the CSB or CCD models. The internal feedback resistor must be used to obtain low gain drift.

COMPLIANCE

The compliance voltage of the DAC70 is the maximum voltage swing allowed on the current output mode in order to maintain the specified accuracy; it is ±2.5V and is compatible with an external op amp summing junction. The maximum safe voltage swing allowed with no damage to the DAC70 output is ±5 volts.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of power supply voltage change on the D/A converter output. It is defined as ppm of FSR per percent of change in either the +15 volt or - 15 volt and +5 power supplies about the nominal power supply voltages. Figure 2 shows Power Supply rejection vs. Frequency.

[† All specifications are tested with a BB3500C operational amplifier connected to the DAC70 output.]

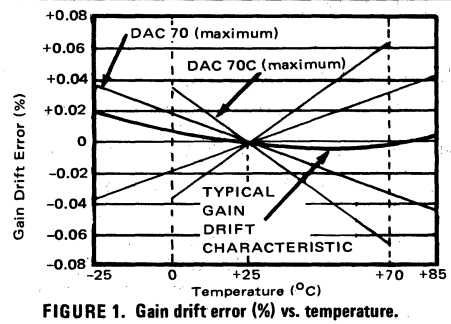


FIGURE 1. Gain drift error (%) vs. temperature.

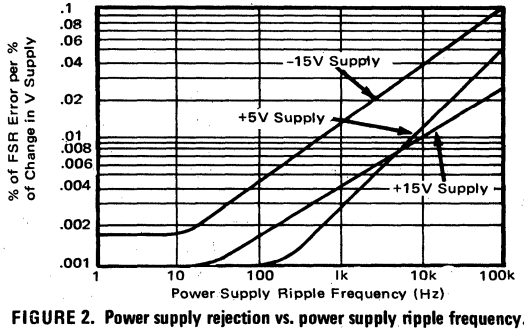


FIGURE 2. Power supply rejection vs. power supply ripple frequency.

TYPICAL PERFORMANCE CURVES

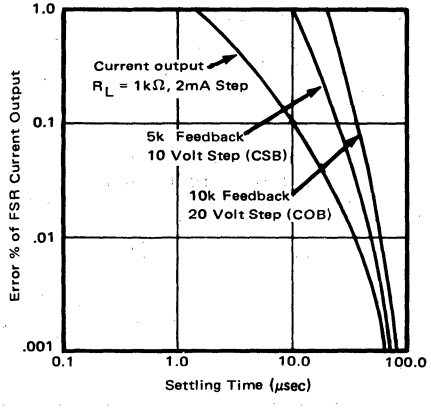


FIGURE 3. Full scale range settling time vs. accuracy.

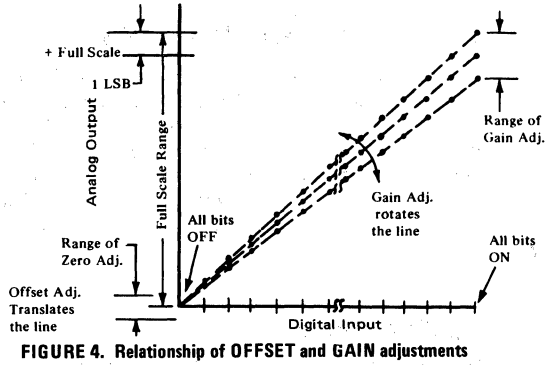


FIGURE 4. Relationship of OFFSET and GAIN adjustments for a UNIPOLAR D/A converter.

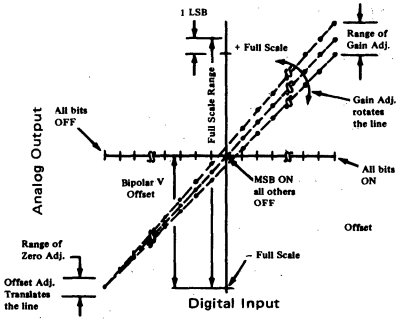


FIGURE 5. Relationship of OFFSET and GAIN adjustments for a BIPOLAR D/A converter.

DIGITAL INPUT AND ANALOG OUTPUT RELATIONSHIPS

DIGITAL INPUT CODE	OUTPUT CODE			
	VOLTAGE		CURRENT	
	16 Bit Resolution	14 Bit Resolution	16 Bit Resolution	14 Bit Resolution
Complementary Unipolar Straight Binary (CSB) 0 to +10V or 0 to -2mA				
One LSB	+153μV	+610μV	0.031mA	0.122μA
All Bits off	+9.99985V	+9.99939	-1.99997mA	-1.99988mA
All Bits on	Zero	Zero	Zero	Zero
Complementary Bipolar Offset Binary (COB) ±10V or ±1mA				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits off	+9.99969V	+9.99878V	-0.99997mA	-0.99988mA
All Bits on	-10.0000V	-10.0000V	+1.0000mA	+1.0000mA
Complementary Binary Coded Decimal (CCD) 0 to +10V or 0 to -1.25mA	4 Digit Resolution	N/A	4 Digit Resolution	N/A
One LSB	+1.0mV		0.125μA	
F.S. Bits off	+9.999V		-1.24987mA	
All Bits on	Zero		Zero	

TABLE II. Ideal output voltage and current.

INSTALLATION CONSIDERATIONS

The DAC70 is laser trimmed to 14 bit linearity. The design of the device makes the 16 bit resolution available on binary units. If 16 bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5 V through a single 1 k Ω resistor.

Due to the extremely high resolution and linearity of the DAC70, system design problems such as grounding and contact resistance become very important. For a 16 bit converter with a +10 volt full scale range, one LSB is 153μV. With a load current of 5 mA and series wiring and connector resistance of only 30 mΩ, the output will be in error by 1 LSB. To understand what this means in terms of a system layout, the impedance of #18 wire is about 0.064 Ω/ft. Neglecting contact resistance, less than 6 inches of wire will produce a 1 LSB error in the analog output voltage! Although the problems involved seem enormous, care in the installation planning can minimize the potential causes of error.

The output can be made essentially independent of lead resistance by sensing the output at the load itself as shown in Figure 6. The lead and contact resistance, Z_i, is reduced by the loop gain to acceptable values.

The DAC70 and the wiring to its connector should be located so as to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pick-up is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pick-up in the circuit. The metal case of the unit is internally connected to the common pin to further minimize pick-up. The DAC70 case is made of gold plated Kovar which also provides some electromagnetic shielding.

NOTE:

It is recommended that the digital input lines of the DAC70 be driven from inverters of TTL input registers to obtain specified accuracy.

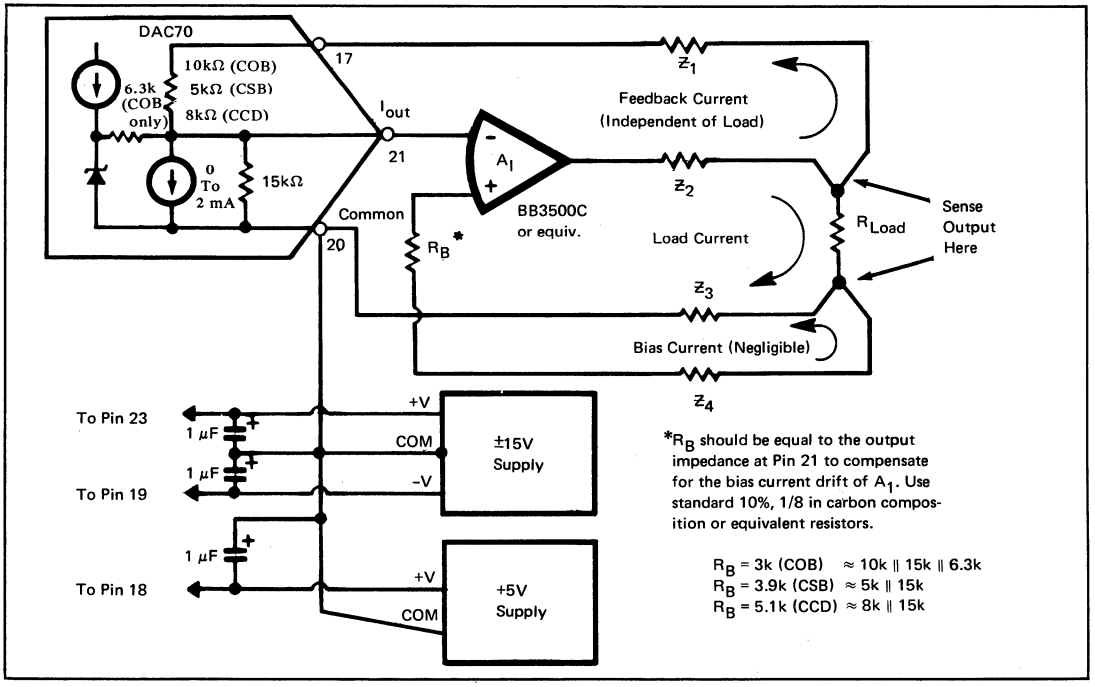


FIGURE 6. Output CIRCUIT for making LOAD VOLTAGE essentially independent of LEAD RESISTANCE.

SUPPLY DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 6. These capacitors should be located close to the DAC70 and should be tantalum or electrolytic types bypassed with a 0.01μF ceramic capacitor for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJ.

Offset and gain may be trimmed by the user with externally connected offset and gain potentiometers. Connection of these potentiometers and the method of adjustment is outlined below. In each case a simplified schematic of the DAC 70 as seen from the adjustment point is given to assist the user in designing his own adjustment networks. Adjust offset first and then gain to avoid interaction (see Figures 4 and 5).

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) D/A converters, apply the digital input code that should give zero volts output and adjust the offset potentiometer for zero volts output. For bipolar (COB) D/A converters, apply the digital input code that should give minus full scale (-10 volts) and adjust the offset potentiometer for an output voltage of -10 volts. Two methods of offset adjustment are shown in Figures 7 & 8.

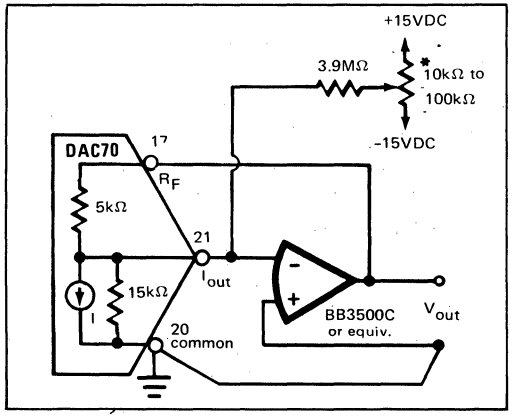


FIGURE 7. Offset adjustment with ±0.2% of FSR range of adjustment. DAC70–CSB–I with external op amp.

In some applications the use of such a large offset adjustment resistor might be undesirable. An alternative method of offset adjustment is shown in Figure 8:

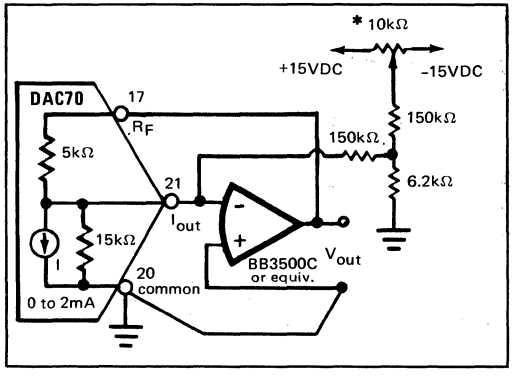


FIGURE 8. Alternative method of offset adjustment with ±0.2% of FSR range of adjustment for DAC70-CSB-I with external op amp.

GAIN ADJUSTMENT

For either unipolar (CSB, CCD) or bipolar (COB) models, apply the digital input that should give the maximum positive current or voltage output. Adjust the gain potentiometer for this full scale value. The positive full scale voltage and currents for the DAC70 are given in Table II.

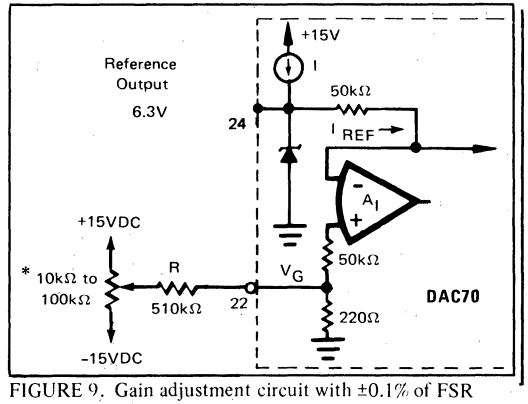


FIGURE 9. Gain adjustment circuit with ±0.1% of FSR range of adjustment.

Figure 9 shows how the gain adjust works on the DAC70. The gain of the DAC70 is determined by the reference current I_{ref}. Due to the high gain and low bias current of A_1, the voltage at the positive input of A_1 is approximately equal to the voltage at the gain adjust pin V_G. Therefore, the reference current is

$$I_{REF} = \frac{6.3\ V - V_G}{50\ k}$$

Since V_G is approximately equal to zero initially, a simple formula for determining the voltage range necessary at the gain adjust pin for a given percentage change in gain is

$$\Delta V_G = \frac{\%\ Gain\ Change}{100} \times 6.3\ volts$$

The full scale output voltage of the DAC70 with an external output amplifier and internal feedback resistor is laser trimmed to less than ±0.05% of FSR.

REFERENCE SUPPLY

All DAC70 and DAC70C models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a gain drift of typically ±3 ppm/°C and is burned in for a total of 160 hours for guaranteed reliability.

This reference may also be used externally but the current drain is limited to 200 μA. An external buffer amplifier is recommended if the DAC70 internal reference will be used externally in order to supply a constant load to the reference supply output.

NOTE: An external reference cannot be used. The DAC70 internal reference must be used.

* High quality multi-turn (10 turns if possible) potentiometers with less than 100 ppm/°C, T.C.R. should be used.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP

The DAC70 is a current output device and will drive the summing junction of an op amp to produce an output voltage (see Figure 10). The op amp output voltage is:

$$V_{out} = -I_{out} R_f$$

Where I_{out} is the DAC70 output current and R_f is the feedback resistor. Use of the internal feedback resistor (Pin 17) is required to obtain specified gain accuracy and low gain drift.

The DAC70 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±25 ppm/°C. The resistors in the DAC70 are chosen for ratio tracking of ±1 ppm/°C and not absolute T.C.R. (which may be as high as ±25 ppm/°C).

An alternative method of scaling the output voltage of the DAC70 and preserving the low gain drift is shown in Figure 11.

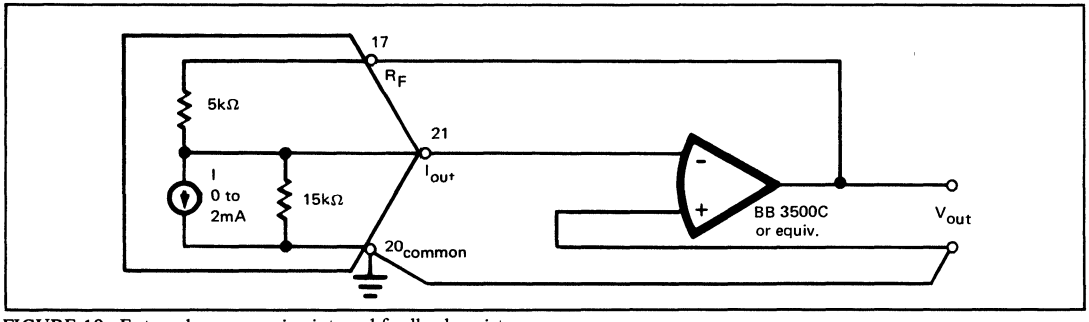


FIGURE 10. External op amp using internal feedback resistors.

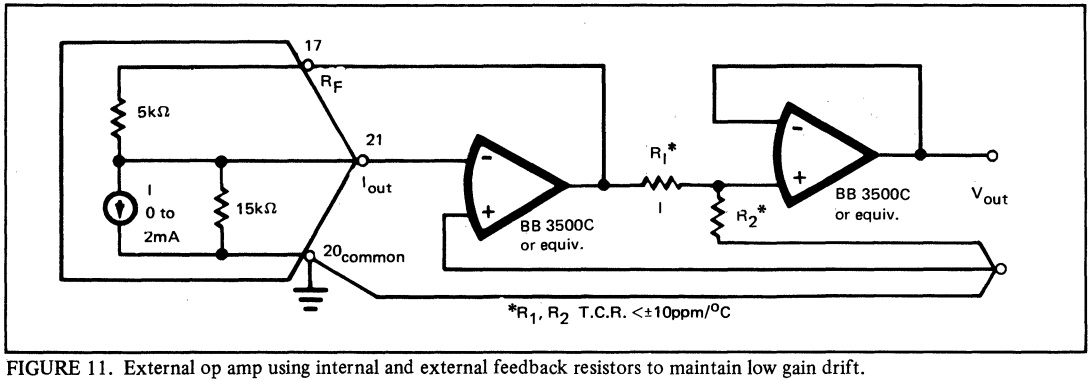


FIGURE 11. External op amp using internal and external feedback resistors to maintain low gain drift.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{out} values of ±1 mA for bipolar voltage ranges and -2 mA for unipolar voltage ranges (see Figure 12). Use protection diodes when a high voltage op amp is used.

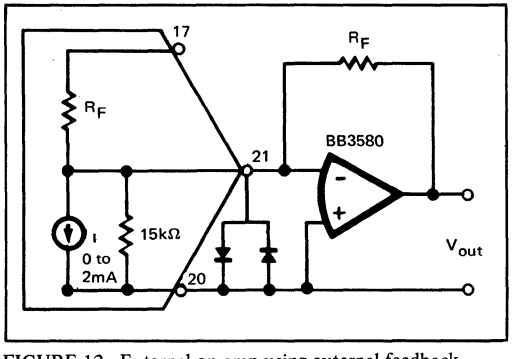
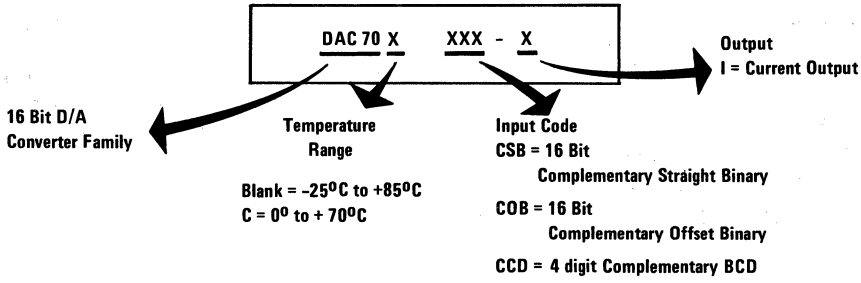


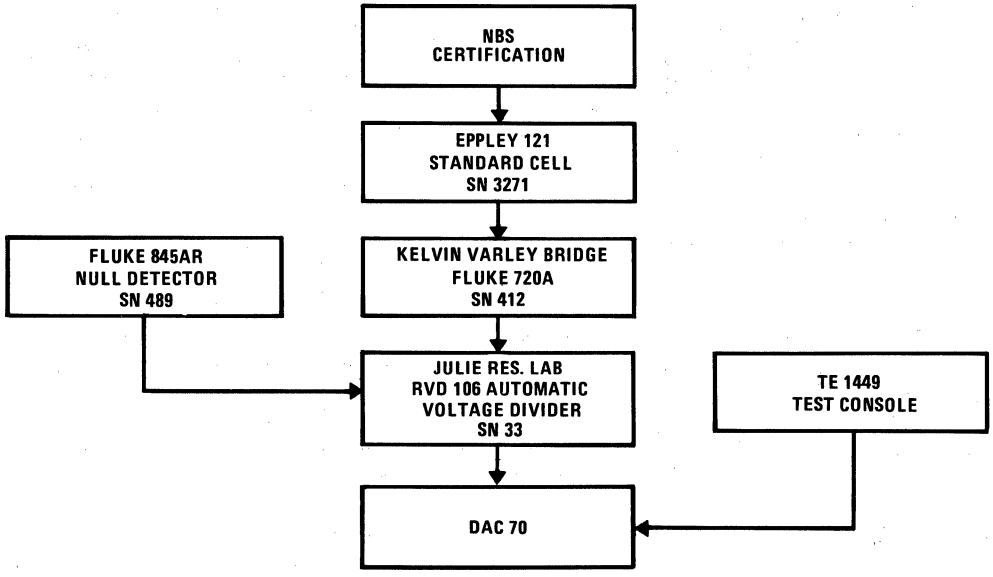
FIGURE 12. External op amp using external feedback resistors.

ORDER INFORMATION

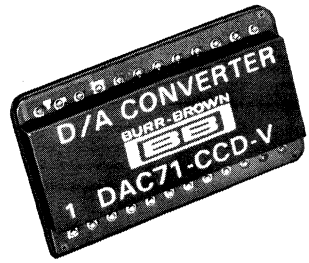


NBS TRACEABILITY

The reference zener is burned-in for a total of 160 hours. The entire unit is burned-in for 96 hours at +100°C to age and stabilize the components and insure long life, excellent stability, and high quality performance.



BURR-BROWN®

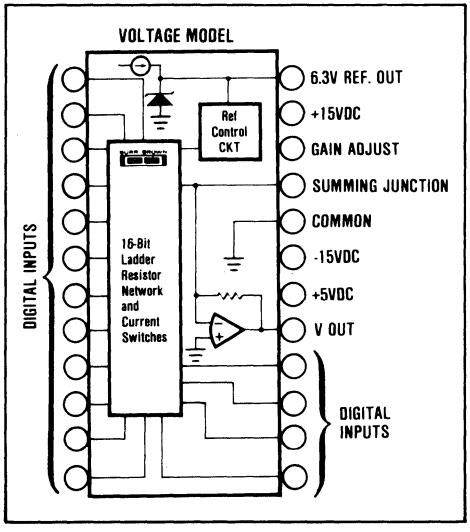


DAC71

High Resolution 16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT, 4-DIGIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±7ppm/°C, (TYPICAL)
- CURRENT AND VOLTAGE MODELS
- LOW COST



DESCRIPTION

The DAC71 is a high quality 16-bit hybrid IC D/A converter available in a 24-pin dual-in-line ceramic package.

The DAC71 with internal reference and optional output amplifier offers a maximum linearity error of ±0.003% of FSR at room temperature and a maximum gain drift of ±15ppm/°C over a temperature range of 0°C to +70°C.

Three basic models accept complementary 16-bit binary or complementary 4-digit BCD TTL-compatible input codes.

Packaged within the DAC71 are fast-settling switches and stable laser-trimmed thin-film resistors that let you select output voltages 0 to +10V (CSB and CCD) or ±10V (COB) and output currents of ±1mA or 0 to -2mA. Input power is ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-430

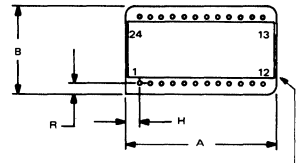
SPECIFICATIONS

ELECTRICAL

Typical at $T_A = 25°C$ and rated power supplies unless otherwise noted.

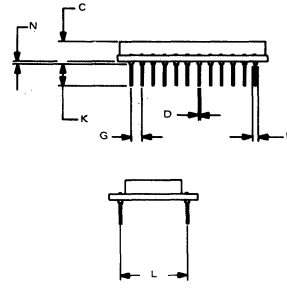
MODEL	DAC71 MIN	DAC71 TYP	DAC71 MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution, CCD		4		Digits
CSB, COB		16		Bits
Logic Levels (TTL-Compatible)(1)				
Logical "1" (at +40μA)	+2.4		+5.5	VDC
Logical "0" (at -1.6mA)	0		+0.4	VDC
TRANSFER CHARACTERISTICS				
ACCURACY				
Linearity Error at 25°C, CCD			±0.005	% of FSR(2)
COB, CSB			±0.003	% of FSR
Gain Error,(3) Voltage		±0.01	±0.1	%
Current		±0.05	±0.25	%
Offset Error,(3) Voltage, Unipolar		±0.1	±2	mV
Voltage, Bipolar			±5	mV
Current, Unipolar			±1	μA
Current, Bipolar			±5	μA
Monotonicity Temperature Range (14 bits)	0		+50	°C
DRIFT Over specified temp. range				
Total Bipolar Drift (includes gain, offset, and linearity drift),(4) Voltage		±7	±15	ppm of FSR/°C
Current		±15	±50	ppm of FSR/°C
Total Error over Temperature Range(5)				
Voltage, Unipolar			±0.083	% of FSR
Bipolar			±0.071	% of FSR
Current, Unipolar			±0.23	% of FSR
Bipolar			±0.23	% of FSR
Gain, Voltage			±15	ppm/°C
Current			±45	ppm/°C
Offset				
Voltage, Unipolar		±1	±2	ppm of FSR/°C
Bipolar			±10	ppm of FSR/°C
Current, Unipolar			±1	ppm of FSR/°C
Bipolar			±40	ppm of FSR/°C
Differential Linearity over Temperature			±2	ppm of FSR/°C
Linearity Error over Temperature			±2	ppm of FSR/°C
SETTLING TIME				
Voltage Models to ±0.003% of FSR				
Output: 20V Step		5	10	μsec
1LSB Step(6)		3	5	μsec
Slew Rate		20		V/μsec
Current Models (to ±0.003% of FSR)				
Output: 2mA step 10Ω to 100Ω Load			1	μsec
1kΩ Load			3	μsec
Switching Transient		500		mV
OUTPUT				
ANALOG OUTPUT				
Voltage Models				
Ranges - CSB, CCD		0 to +10		V
COB		±10		V
Output Current	±5			mA
Output Impedance DC		0.05		Ω
Short Circuit Duration		Indefinite to Common		
Current Models				
Ranges - CSB, CCD		0 to -2		mA
COB		±1		mA
Output Impedance - Unipolar		15		kΩ
Bipolar		4.4		kΩ
Compliance		±2.5		V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	V
Maximum External Current(7)			±200	μA
Temperature Coefficient of Drift			±10	ppm/°C

MECHANICAL



NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	0.85	.105	2.16	2.67

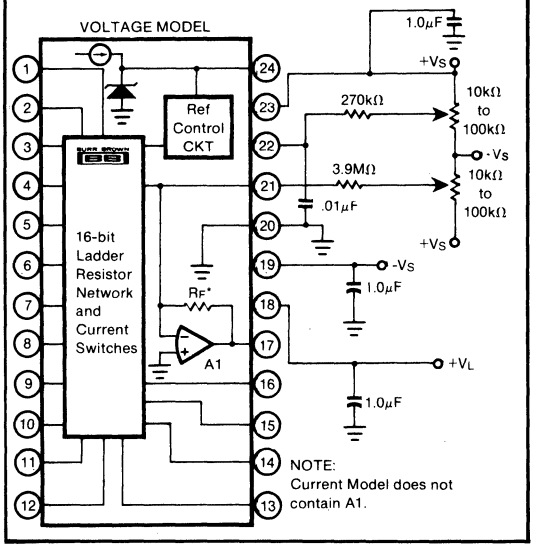
CASE: Black Ceramic
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

MODEL	DAC71			UNITS
	MIN	TYP	MAX	
POWER SUPPLY SENSITIVITY				
Unipolar Offset				
±15VDC		±0.0001		% of FSR/%V_S
+15VDC		±0.0001		% of FSR/%V_S
Bipolar Offset				
±15VDC		±0.0004		% of FSR/%V_S
+5VDC		±0.0001		% of FSR/%V_S
Gain				
±15VDC		±0.001		% of FSR/%V_S
+5VDC		±0.0005		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS				
Voltage	±14.5, +4.75	±15, +5	±15, +5.25	VDC
Supply Drain, ±15VDC (no load)		±25	±35	mA
+5VDC (logic supply)		+20	+35	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating (double above Drift Specs)	-25		+85	°C
Storage	-55		+100	°C

NOTES:

1. Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output (ΔV_O) as logic 0 varies from 0.0V to +0.4V and logic 1 changes from +2.4V to +5.0V on all inputs is less than 0.006% of FSR.
2. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
3. Adjustable to zero with external trim potentiometer.
4. See "Computing Total Accuracy over Temperature".
5. With gain and offset errors adjusted to zero at 25°C.
6. LSB is for 14-bit resolution.
7. Maximum with no degradation of specifications.

CONNECTION DIAGRAM



PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6.3V REF. OUT	24	6.3V REF. OUT

*R_F = 5kΩ (CSB), 10kΩ (COB), 8kΩ (CCD).

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC71 accepts complementary digital input codes in either binary (CSB, COB) or decimal (CCD) format. The COB model may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

	DIGITAL INPUT CODES			
	MSB ↓ LSB ↓	CSB	COB	CTC*
CSB, COB MODELS		Compl. Straight Binary	Compl. Offset Binary	Compl. Two's Complement
	All bits ON 0000...000	+Full Scale	+Full Scale	-1LSB
	Mid Scale 0111...111	+1/2 Full Scale	Zero	-Full Scale
	All bits OFF 1111...111	Zero	-Full Scale	Zero
	1000...000	Mid Scale -1LSB	-1LSB	+Full Scale
CCD MODELS		CCD Complementary Coded Decimal 4 Digits		*Invert the MSB of the COB code with an external inverter to obtain CTC code.
	F.S. bits ON 0110...0110	+Full Scale		
	All Bits OFF 1111...1111	Zero		

ACCURACY

LINEARITY

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.003% max (CSB, COB) or ±0.005% max (CCD) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can be anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

MONOTONICITY

Monotonicity over 0°C to +50°C is guaranteed. This insures that the analog output will increase or remain the same for increasing 14-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (see Figure 1). Gain Drift is established by: 1) testing the end point differences for each DAC71 model at +25°C and the appropriate specification temperature extremes; 2) calculating the gain error with respect to the +25°C value; and 3) dividing by the temperature change. This is expressed in ppm/°C.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

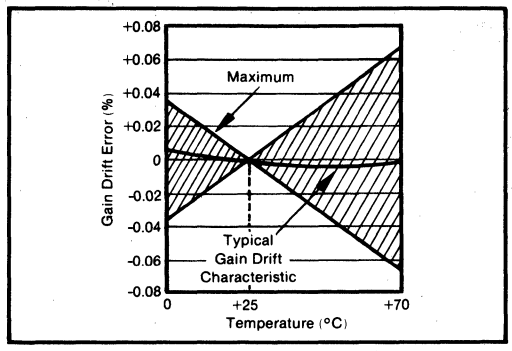


FIGURE 1. Gain Drift Error (%) vs Temperature.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC71 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

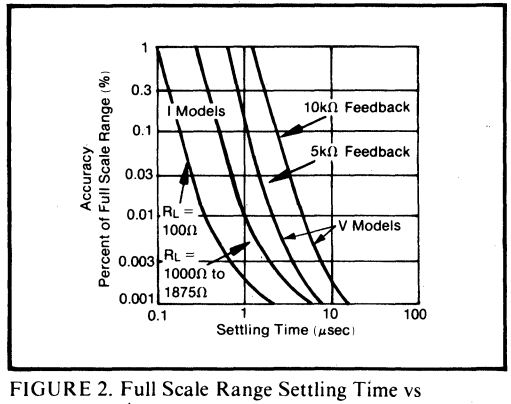


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

VOLTAGE OUTPUT MODELS

Settling times are specified to ±0.003% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

CURRENT OUTPUT MODELS

Two settling time are specified to ±0.003% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω.

COMPLIANCE

Compliance voltage is the maximum voltage swing

allowed on the output of the current models while maintaining specified accuracy. The typical compliance voltage of all current output models is ±2.5V and maximum safe voltage swing permitted without damage is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 3).

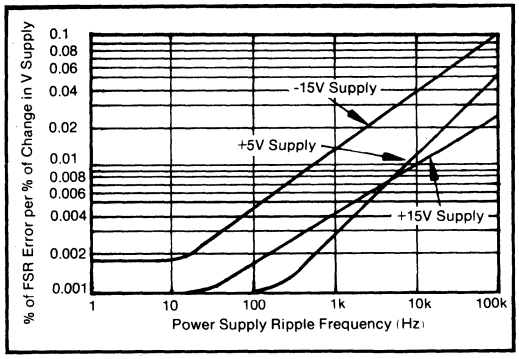


FIGURE 3. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All DAC71 models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±3ppm/°C and is burned-in for a total of 168 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 200μA. An external buffer amplifier is recommended if the DAC71 internal reference is used externally in order to provide a constant load to the reference supply output.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC71. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC71 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to Figures 5 and 6 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

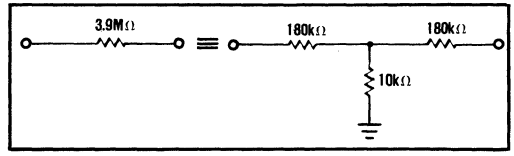


FIGURE 4. Equivalent Resistances.

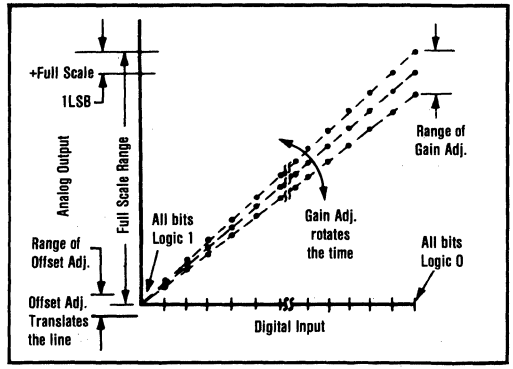


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

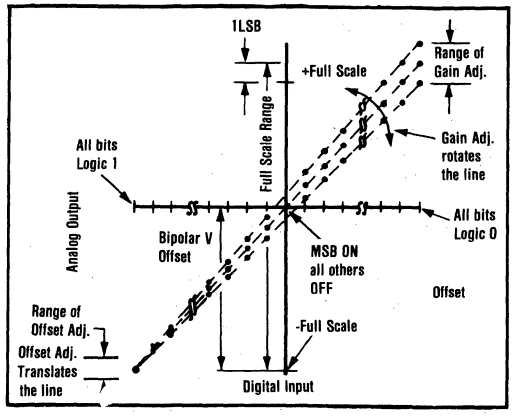


FIGURE 6. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential

output and adjust the offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. The COB model is internally connected for a 20V FSR range where the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

TABLE II. Digital Input and Analog Output Relationships.

DIGITAL INPUT CODE	OUTPUT CODE			
	VOLTAGE		CURRENT	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Unipolar Straight Binary CSB 0 to +10V or 0 to -2mA*				
One LSB	+153μV	+610μV	0.031μA	0.122μA
All Bits ON 00...00	+9.99985V	+9.99939V	-1.99997mA	-1.99988mA
All Bis OFF 11...11	Zero	Zero	Zero	Zero
Complementary Bipolar Offset Binary COB ±10V or ±1mA*				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits ON 00...00	+9.99969V	+9.99878V	-0.99997mA	-0.99988mA
All Bits OFF 11...11	-10.0000V	-10.0000V	+1.0000mA	+1.0000mA
Complementary Binary Coded Decimal CCD 0 to +10V or 0 to -1.25mA	4-Digit Resolution	N/A	4-Digit Resolution	N/A
One LSB	+1.0mV		0.125μA	
Full Scale 0110...0110	+9.999V		-1.24987mA	
All Bits OFF 1111...1111	Zero		Zero	

* To obtain values for other binary CBI ranges: 0 to +5V range, divide 0 to +10V range by 2; ±5V range, divide ±10V range by 2; ±2.5V range, divide ±10V range by 4.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

The DAC71 is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available on binary units. If 16-bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5VDC through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the DAC71, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ, the output will be in error by 1LSB. To understand what this means in terms of a system layout, the impedance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 6 inches of wire will produce a 1LSB error in the analog output voltage! Although the problems involved seem enormous, care in the installation planning can minimize the potential causes of error.

Figure 7 shows the connection diagram for a voltage output DAC71. Lead and contact resistances are represented by R_1 through R_5. As long as the load resistance (R_L) is constant. R_2 simply introduces a gain error than can be removed during initial calibration. R_3 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the DAC71 for optimum performance.

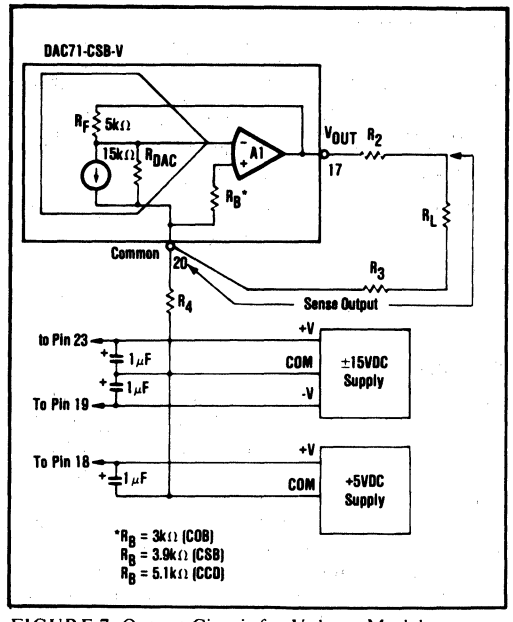


FIGURE 7. Output Circuit for Voltage Models.

Figures 8 and 9 show two methods of connecting current model DAC71's with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A1 at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_1 and can be eliminated during initial calibration. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at Common (pin 20), then the differential output circuit shown in Figure 9 is recommended. In this circuit the output voltage is sensed at the load common and not at the DAC common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible the circuit of Figure 9 can be reduced to the one shown in Figure 8 because $R_B = (R_7 + R_5) \parallel R_6$. In all three circuits the effect of R_4 is negligible.

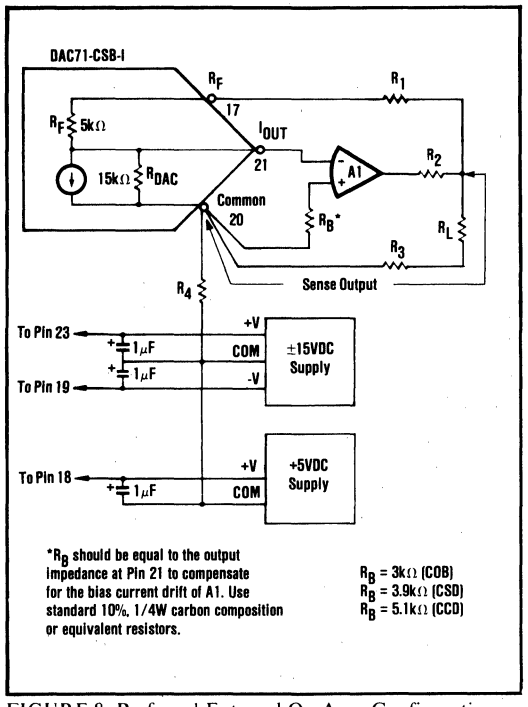


FIGURE 8. Preferred External Op Amp Configuration.

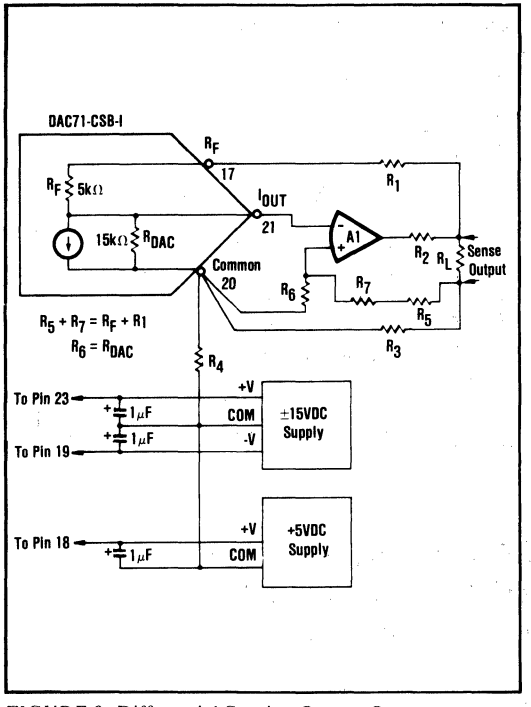


FIGURE 9. Differential Sensing Output Op Amp Configuration.

The DAC71 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

NOTE: It is recommended that the digital input lines of the DAC71 be driven from inverters or buffers of TTL input registers to obtain specified accuracy.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, R_L, with the current output model connected as shown in Figure 10, will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA[(15k\Omega \times R_L)/(15k\Omega + R_L)]$$

Where R_L max = 1.36kΩ

and V_{OUT} max = -2.5V

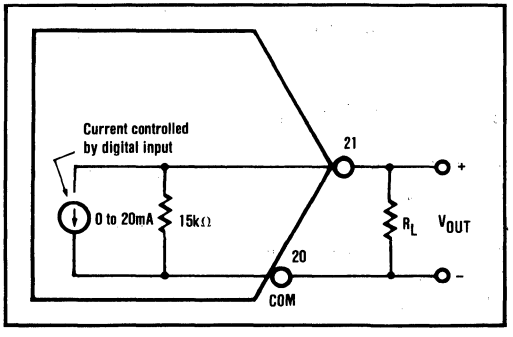


FIGURE 10. Equivalent Circuit DAC71-CSB-I Connected for Unipolar Voltage Output with Resistive Load.

Add an external low T.C. (<10ppm/°C) resistor (R_1) as shown in Figure 11 to obtain a 0 to -2V full scale output voltage range for CCD input codes.

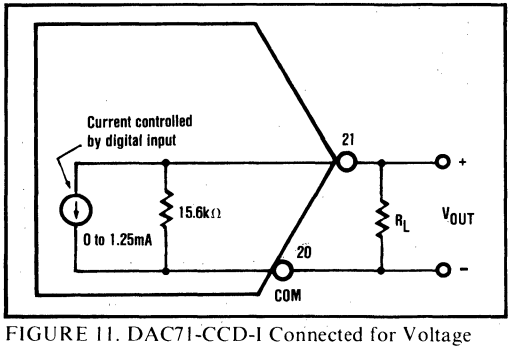


FIGURE 11. DAC71-CCD-I Connected for Voltage Output with Resistive Load.

$V_{OUT} = -1.25mA[(15.6k\Omega \times R_L)/(15.6k\Omega + R_L)]$
Where R_L max = 1.79kΩ
and V_{OUT} max = -2.01V

DRIVING A RESISTIVE LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12. V_{OUT} is determined by:

$V_{OUT} = \pm 1mA[(4.44k\Omega \times R_L)/(4.44k\Omega + R_L)]$
Where R_L max = 5.72kΩ
and V_{OUT} max = ±2.5V

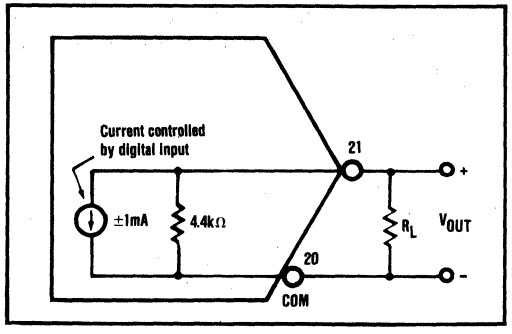


FIGURE 12. DAC71-COB-I Connected for Bipolar Output Voltage with Resistive Load.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DAC

The DAC71-(CSB, COB, CCD)-I are current output devices and will drive the summing junction of an op amp to produce an output voltage (see Figure 13). The op amp output voltage is:

$$V_{OUT} = -I_{OUT} R_F$$

where I_{OUT} is the DAC71 output current and R_F is the feedback resistor. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

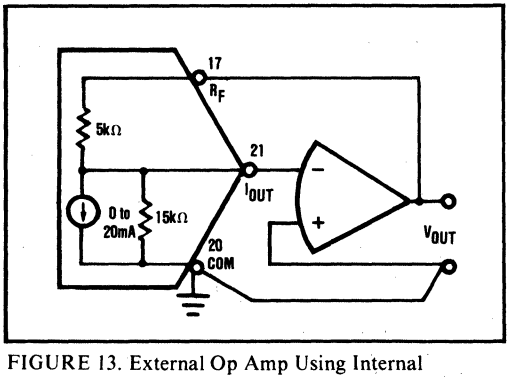


FIGURE 13. External Op Amp Using Internal Feedback Resistors.

The DAC71 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±25ppm/°C. The resistors in the DAC71 are chosen for ratio tracking of ±1ppm/°C and not absolute TCR (which may be as high at ±25ppm/°C.)

An alternative method of scaling the output voltage of the DAC71 and preserving the low gain drift is shown in Figure 14.

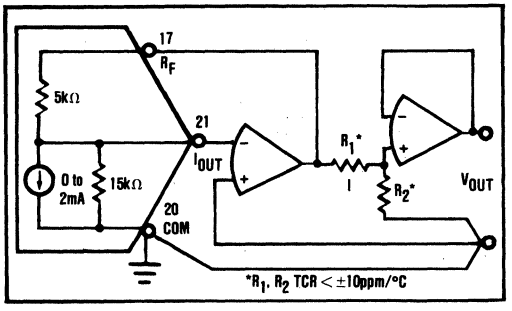


FIGURE 14. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

OUTPUTS LARGER THAN 20-VOLT RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges (see Figure 15). Use protection diodes when a high voltage op amp is used.

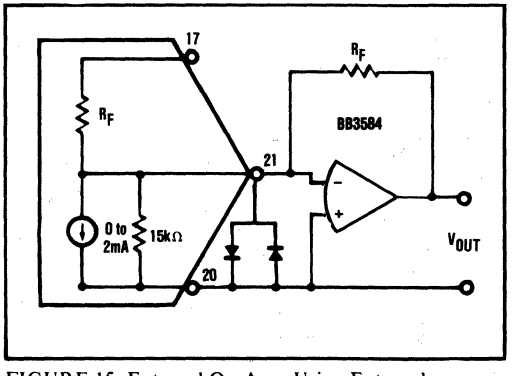


FIGURE 15. External Op Amp Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC71 consists of three primary components: gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the

worst-case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst-case accuracy drift for a DAC71 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately.

In the unipolar mode of operation, offset drift (±1ppm/°C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±5ppm/°C due to ratio drift of current switch V_{BE} to the reference transistor, 2)±10ppm/°C due to the zener reference and, 3) ±2ppm/°C linearity drift due to ratio drift of current weighting resistors and V_{BE} of the quad current switches. The sum of these three components, ±17ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst-case accuracy drift in the unipolar mode is simply the sum of the components, or ±18ppm/°C.

In the bipolar mode the major portion of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 16 shows a simplified circuit diagram of a DAC71-COB-V with all bits off. The current switch leakage current is negligible, so

$$V_{-FULL\ SCALE} = (-R_F/R_{BPO}) \cdot V_{REF}$$
$$= (-10k\Omega/6.3k\Omega) \cdot 6.3V = -10V$$

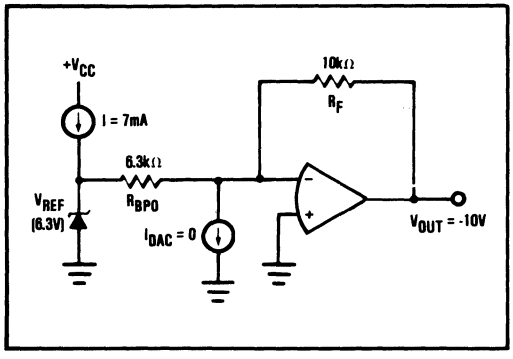


FIGURE 16. Simplified Diagram of DAC71-COB-V with "All Bits Off" (±10V Range).

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is +10ppm/°C, this equivalent to (+10ppm/°C) x (+6.3V) = +63μV/°C. This will result in a voltage drift at the amplifier output of

$$\Delta V_{-FS}/\Delta T = -(R_F/R_{BPO}) \cdot (\Delta V_{REF}/\Delta T)$$
$$= -(10k\Omega/6.3k\Omega) \cdot (63\mu V/°C) = -100\mu V/°C.$$

Since the DAC71-COB-V is operating in the ±10V range this equivalent to (-100μV/°C) ÷ (20V range) = -5ppm of FSR/°C.

Now consider the effect of reference changes on gain drift. When all of the bits are turned on it can be shown that:

$$\Delta V_{+FULL\ SCALE}/\Delta T = +(R_F/R_{BPO}) \cdot (\Delta V_{REF}/\Delta T)$$
$$= +(10k\Omega/6.3k\Omega) \cdot (63\mu V/°C) = +100\mu V/°C.$$

and (+100μV/°C) 20V Range = +5ppm/°C of FSR.

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the opposite direction of, the drift of the plus full scale voltage and that zener reference variations have virtually no effect on the zero point (see Figure 17). This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm/°C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

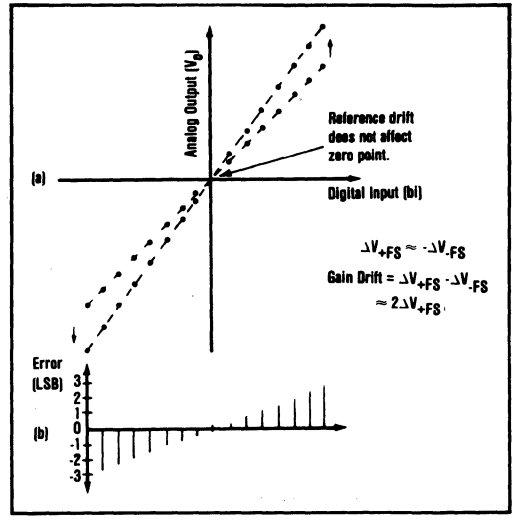


FIGURE 17. (a) Effect of a Positive Reference Drift on the Ideal D/A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC71.

Using this relationship, the worst-case accuracy drift for a DAC71-COB-V can be computed. The maximum TCR of the zener reference is ±10ppm/°C. The gain drift due to the reference then is also ±10ppm/°C. The full scale drift and bipolar offset drift are each half that amount or ±5ppm/°C. The maximum gain and offset drifts of the DAC71, exclusive of the reference, are ±5 and ±3ppm/°C respectively. Adding this to the full scale drift due to the reference plus the linearity drift of ±2ppm/°C gives a worst-case total accuracy drift of ±15ppm/°C. (Random drifts, which these are, can be in the same direction so they add directly.) This is much less than the total drift obtained by simply adding the maximum gain, bipolar offset, and linearity drifts (±27ppm/°C). The maximum

zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±5.5ppm of FSR/°C.

The DAC71 is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

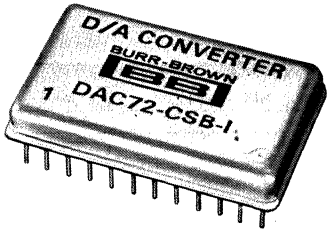
total worst-case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.003% + ±15ppm/°C (45°) (100)
= ±0.07%

total worst-case bipolar zero point error
= Bipolar zero drift x ΔT
= ±5.5ppm of FSR% (45°C) (100)
= ±0.025%

ORDERING INFORMATION

MODEL	INPUT CODE
CURRENT MODELS	
DAC71-COB-I	Complementary Offset Binary
DAC71-CSB-I	Complementary Straight Binary
DAC71-CCD-I	Complementary Coded Decimal
VOLTAGE MODELS	
DAC71-COB-V	Complementary Offset Binary
DAC71-CSB-V	Complementary Straight Binary
DAC71-CCD-V	Complementary Coded Decimal

BURR-BROWN®

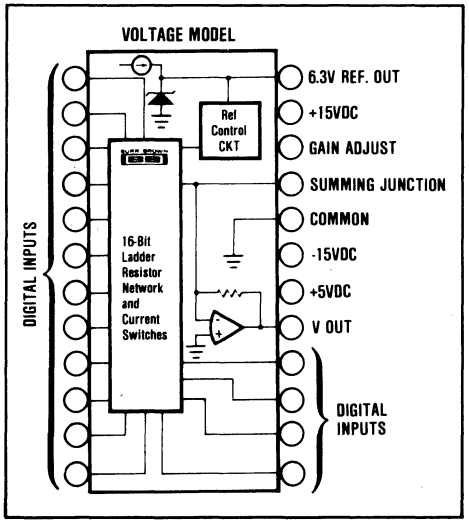


DAC72

High Resolution
16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT, 4-DIGIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±5ppm/°C, TYPICAL
- AVAILABLE IN TWO TEMPERATURE RANGES:
  0°C to +70°C
  -25°C to +85°C
- CURRENT AND VOLTAGE MODELS
- LOW COST
- METAL HERMETIC PACKAGE



DESCRIPTION

The DAC72 is a high quality 16-bit hybrid IC D/A converter in a 24-pin dual-in-line metal package.

The DAC72C with internal reference and optional output amplifier offers a maximum linearity error of ±0.003% of FSR at room temperature and a maximum gain drift of ±15ppm/°C over a temperature range of 0°C to +70°C. The DAC72 offers a maximum linearity error of ±0.003% of FSR at room temperature and a gain drift of ±7ppm/°C from +25°C to +85°C and ±15ppm/°C from -25°C to +25°C.

Three basic models accept complementary 16-bit binary or complementary 4-digit BCD TTL-compatible input codes.

Packaged within the DAC72 are fast-settling switches and stable laser-trimmed thin-film resistors that let you select output voltages 0 to +10V (CSB and CCD) or ±10V (COB) and output currents of ±1mA or 0 to -2mA. Input power is ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

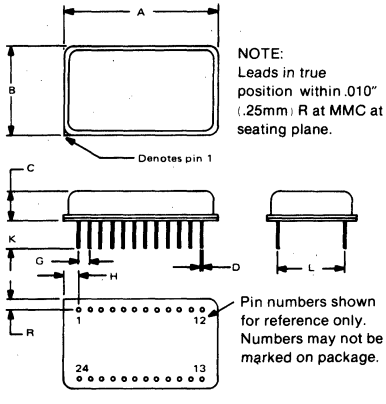
MODEL	DAC72C			DAC72			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution, CCD		4			4		Digits
CSB, COB		16			16		Bits
Logic Levels (TTL-Compatible)(1)							
Logical "1" (at +40µA)	+2.4		+5.5	+2.4		+5.5	VDC
Logical "0" (at -1.6mA)	0		+0.4	0		+0.4	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at 25°C, CCD			±0.005			±0.005	% of FSR(2)
COB, CSB			±0.003			±0.003	% of FSR
Gain Error(3), Voltage		±0.05	±0.15		±0.05	±0.15	%
Current		±0.05	±0.25		±0.05	±0.25	%
Offset Error(3), Voltage, Unipolar		±0.1	±2		±0.1	±2	mV
Voltage, Bipolar			±10			±10	mV
Current, Unipolar			±1			±1	µA
Current, Bipolar			±5			±5	µA
Monotonicity Temp. Range (14-bits)	0		+50	0		+70	°C
DRIFT (Over specified temp. range)							
Total Bipolar Drift (includes gain, offset, and linearity drift)(4), Voltage (hot/cold)(5)		±7	±15		±5	±11/±19	ppm of FSR/°C
Current		±15	±50		±10	±40	ppm of FSR/°C
Total Error over Temp. Range(6)							
Voltage, Unipolar (hot/cold)(5)			±0.083			±0.072/±0.10	% of FSR
Bipolar (hot/cold)(5)			±0.071			±0.072/±0.10	% of FSR
Current, Unipolar			±0.23			±0.24	% of FSR
Bipolar			±0.23			±0.24	% of FSR
Gain, Voltage (hot/cold)(5)			±15		±5	±7/±15	ppm/°C
Current			±45			±35	ppm/°C
Offset							
Voltage, Unipolar		±1	±2		±1	±2	ppm of FSR/°C
Bipolar			±10			±8	ppm of FSR/°C
Current, Unipolar			±1			±1	ppm of FSR/°C
Bipolar			±40			±35	ppm of FSR/°C
Differential Linearity over Temperature			±2			±1	ppm of FSR/°C
Linearity Error over Temperature			±2			±1	ppm of FSR/°C
SETTLING TIME							
Voltage Models (to ±0.003% of FSR)							
Output: 20V Step		5	10		5	10	µsec
1LSB Step(7)		3	5		3	5	µsec
Slew Rate		20			20		V/µsec
Current Models (to ±0.003% of FSR							
Output: 2mA step 10Ω to 100Ω Load			1			1	µsec
1kΩ Load			3			3	µsec
Switching Transient		500			500		mV
OUTPUT							
ANALOG OUTPUT							
Voltage Models							
Ranges - CSB, CCD		0 to +10			0 to +10		V
COB		±10			±10		V
Output Current	±5			±5			mA
Output Impedance DC		0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
Current Models							
Ranges - CSB, CCD		0 to -2			0 to -2		mA
COB		±1			±1		mA
Output Impedance - Unipolar		15			15		kΩ
Bipolar		4.4			4.4		kΩ
Compliance		±2.5			±2.5		V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Maximum External Current(8)			±200			±200	µA
Temp. Coeff. of Drift			±10			±5	ppm/°C

MODEL	DAC72C			DAC72			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY SENSITIVITY							
Unipolar Offset							
±15VDC		±0.0001			±0.0001		% of FSR/% Vs
+15VDC		±0.0001			±0.0001		% of FSR/% Vs
Bipolar Offset							
±15VDC		±0.0004			±0.0004		% of FSR/% Vs
+5VDC		±0.0001			±0.0001		% of FSR/% Vs
Gain							
±15VDC		±0.001			±0.001		% of FSR/% Vs
+5VDC		±0.0005			±0.0005		% of FSR/% Vs
POWER SUPPLY REQUIREMENTS							
Voltage	±14.5, +4.75	±15, +5	±15.5, +5.25	±14.5, +4.75	±15, +5	±15.5, +5.25	VDC
Supply Drain, ±15VDC (no load)		±25	±35		±25	±35	mA
+5VDC (logic supply)		+20	+35		±20	+35	mA
TEMPERATURE RANGE							
Specification	0		+70	-25		+85	°C
Operating (double above Drift Specs)	-25		+85	-55		+100	°C
Storage	-55		+100	-55		+110	°C

NOTES:

1. Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output (ΔVO) as logic 0 varies from 0.0V to 0.4V and (logic 1 changes from +2.4V to +5.0V on all inputs is less than 0.006% of FSR.
2. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
3. Adjustable to zero with external trim potentiometer.
4. See "Computing Total Accuracy over Temperature".
5. Hot ≡ +25°C to +85°C; Cold ≡ -25°C to +25°C for DAC72.
6. With gain and offset errors adjusted to zero at 25°C.
7. LSB is for 14-bit resolution.
8. Maximum with no degradation of specifications.

MECHANICAL



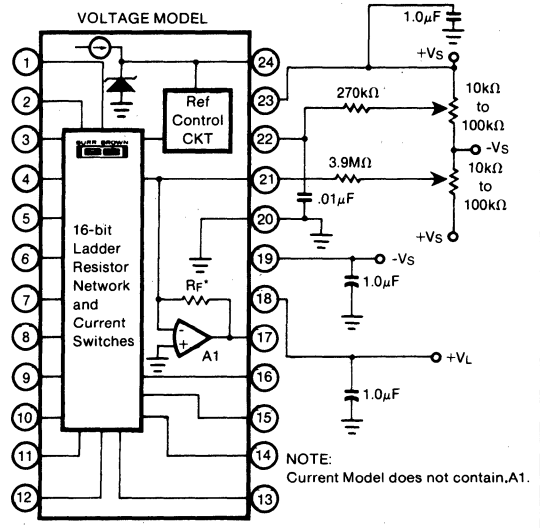
NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

CASE: Nickel Plated Steel
MATING CONNECTOR:245MC
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

CONNECTION DIAGRAM



*RF = 5kΩ (CSB), 10kΩ (COB), 8kΩ (CCD).

PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6.3V REF. OUT	24	6.3V REF. OUT

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC72 accepts complementary digital input codes in either binary (CSB, COB) or decimal (CCD) format. The COB model may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

	DIGITAL INPUT CODES				
			CSB	COB	CTC*
CSB, COB MODELS		MSB LSB	Compl. Straight Binary	Compl. Offset Binary	Compl. Two's Complement
	All bits ON	0000...000	+Full Scale	+Full Scale	-1LSB
	Mid Scale	0111...111	+1/2 Full Scale	Zero	-Full Scale
	All bits OFF	1111...111	Zero	-Full Scale	Zero
		1000...000	Mid Scale -1LSB	-1LSB	+Full Scale
CCD MODELS			CCD Complementary Coded Decimal 4 Digits		*Invert the MSB of the COB code with an external inverter to obtain CTC code.
	F.S. bits ON	0110...0110	+Full Scale		
	All Bits OFF	1111...1111	Zero		

ACCURACY

LINEARITY

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.003% max (CSB, COB) or ±0.005% max (CCD) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can be anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

MONOTONICITY

Monotonicity over 0°C to +50°C (DAC72C) and 0°C to +70°C (DAC72) is guaranteed. This insures that the analog output will increase or remain the same for increasing 14-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (see Figure 1). Gain Drift is established by: 1) testing the end point differences for each DAC72 model at +25°C and the appropriate specification temperature extremes; 2) calculating the gain error with respect to the +25°C value; and 3) dividing by the temperature change. This is expressed in ppm/°C.

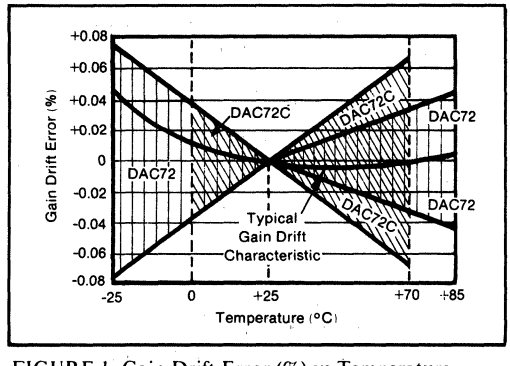


FIGURE 1. Gain Drift Error (%) vs Temperature.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC72 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

VOLTAGE OUTPUT MODELS

Settling times are specified to ±0.003% of FSR; one for maximum full scale range changes of 20V and one for a

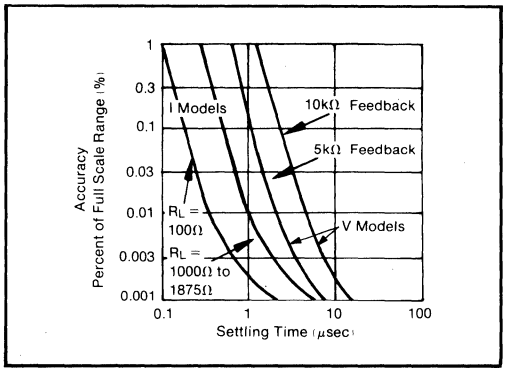


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

CURRENT OUTPUT MODELS

Two settling times are specified to ±0.003% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the output of the current models while maintaining specified accuracy. The typical compliance voltage of all current output models is ±2.5V and maximum safe voltage swing permitted without damage is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 3).

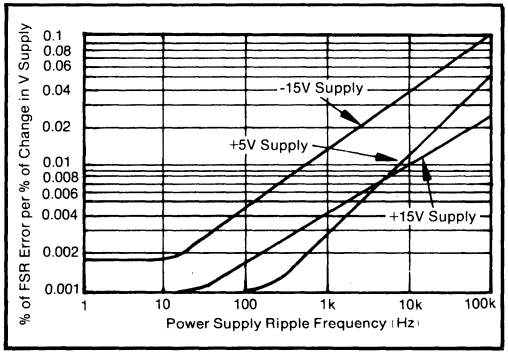


FIGURE 3. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All DAC72 models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±3ppm °C and is burned-in for a total of 168 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 200μA. An external buffer amplifier is recommended if the DAC72 internal reference is used externally in order to provide a constant load to the reference supply output.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC72. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC72 to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic

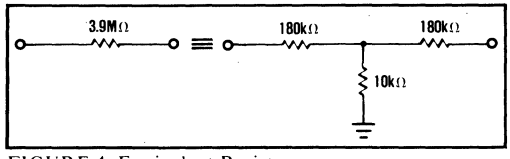


FIGURE 4. Equivalent Resistances.

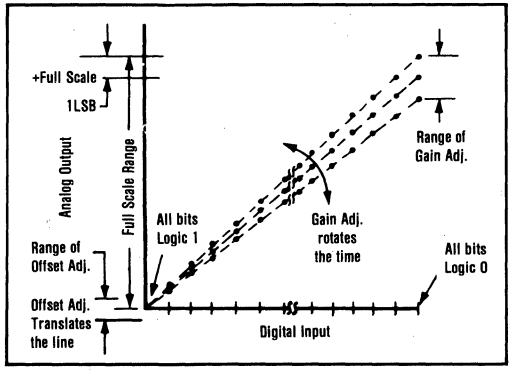


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to Figures 5 and 6 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

If the full (absolute) accuracy capability of the DAC72 is required, recalibration of gain and offset every 2 months is recommended.

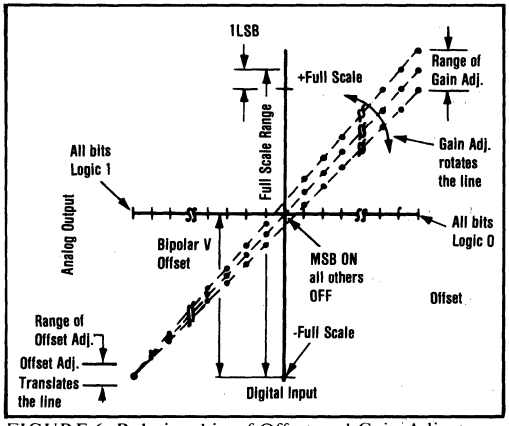


FIGURE 6. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. The COB model is internally connected for a 20V FSR range where the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

TABLE II. Digital Input and Analog Output Relationships.

DIGITAL INPUT CODE	OUTPUT CODE			
	VOLTAGE		CURRENT	
	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Unipolar Straight Binary (CSB)				
0 to +10V or 0 to -2mA*				
One LSB	+153μV	+610μV	0.031μA	0.122μA
All Bits ON (00...00)	+9.99985V	+9.99939V	-1.99997mA	-1.99988mA
All Bis OFF (11...11)	Zero	Zero	Zero	Zero
Complementary Bipolar Offset Binary (COB)				
±10V or ±1mA*				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits ON (00...00)	+9.99969V	+9.99878V	-0.99997mA	-0.99988mA
All Bits OFF (11...11)	-10.0000V	-10.0000V	+1.0000mA	+1.0000mA
Complementary Binary Coded Decimal (CCD)	4-Digit Resolution	N/A	4-Digit Resolution	N/A
0 to +10V or 0 to -1.25mA				
One LSB	+1.0mV		0.125μA	
Full Scale (0110...0110)	+9.999V		-1.24987mA	
All Bits OFF (1111...1111)	Zero		Zero	

* To obtain values for other binary (CBI) ranges; 0 to +5V range, divide 0 to +10V range by 2; ±5V range, divide ±10V range by 2; ±2.5V range, divide ±10V range by 4.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

The DAC72 is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available on binary units. If 16-bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5VDC through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the DAC72, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ, the output will be in error by 1LSB. To understand what this means in terms of a system layout, the impedance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 6 inches of wire will produce a 1LSB error in the analog output voltage! Although the problems involved seem enormous, care in the installation planning can minimize the potential causes of error.

Figure 7 shows the connection diagram for a voltage output DAC72. Lead and contact resistances are represented by

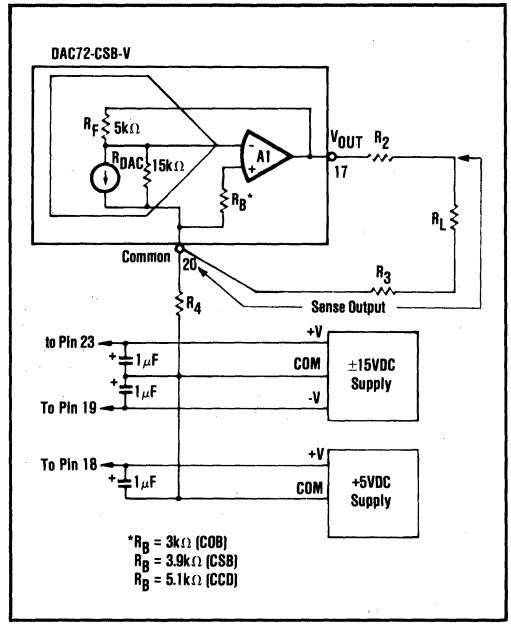


FIGURE 7. Output Circuit for Voltage Models.

R_1 through R_5. As long as the load resistance (R_L) is constant, R_2 simply introduces a gain error that can be removed during initial calibration. R_3 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable then R_2 should be less than 1LSB. For example, if $R_{L,min}$ is 5kΩ then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the DAC72 for optimum performance.

Figures 8 and 9 show two methods of connecting current model DAC72's with external precision output op amps. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A1 at R_L) the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but it is independent of the value of R_L and can be eliminated during initial calibration. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at Common (pin 20), then the differential output circuit shown in Figure 9 is recommended. In this circuit the output voltage is sensed at the load common and not at the DAC common as in the previous curcuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible the circuit of Figure 9 can be reduced to the one shown in Figure 8 because $R_B = (R_7 + R_5) \parallel R_6$. In all three circuits the effect of R_4 is negligible.

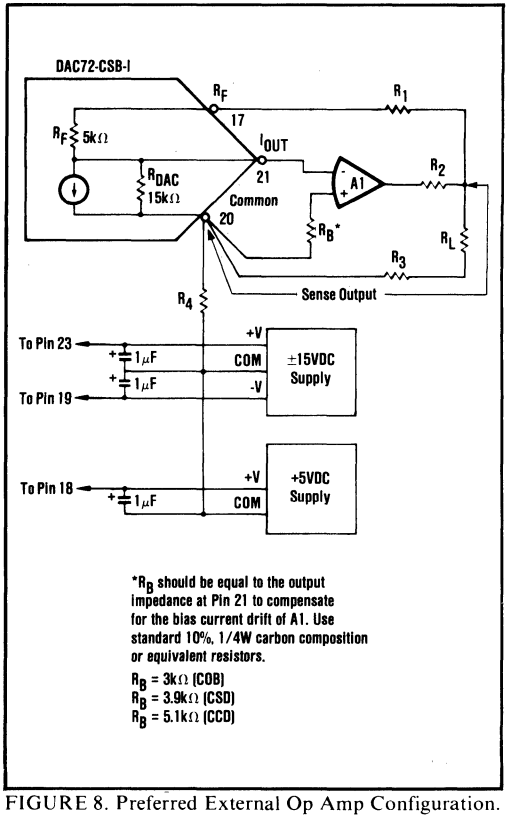


FIGURE 8. Preferred External Op Amp Configuration.

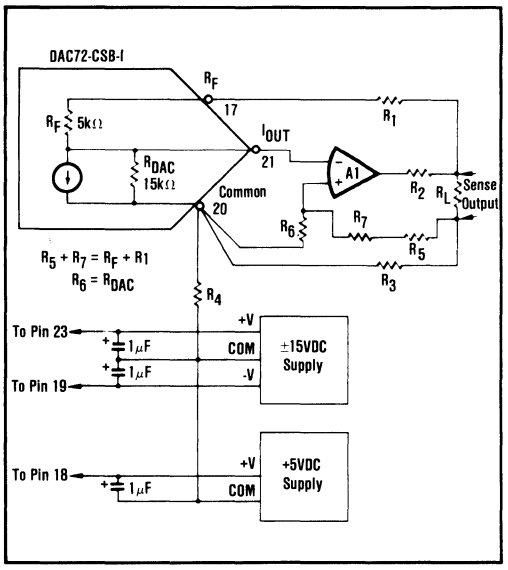


FIGURE 9. Differential Sensing Output Op Amp Configuration.

The DAC72 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit. The metal case of the DAC72 is internally connected to the common pin to further minimize pickup. The DAC72 is made of nickel plated steel which also provides some electromagnetic shielding.

NOTE: It is recommended that the digital input lines of the DAC72 be driven from inverters or buffers of TTL input registers to obtain specified accuracy.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, R_L, with the current output model connect as shown in Figure 10, will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA[(15k\Omega \times R_L)/(15k\Omega + R_L)]$$

Where R_L max = 1.36kΩ

and V_{OUT} max = -2.5V

Add an external low T.C. (<10ppm °C) resistor (R_L) as shown in Figure 11 to obtain a 0 to -2V full scale output voltage range for CCD input codes.

$$V_{OUT} = 1.25mA\ [(15.6k\Omega \times R_L)/(15.6k\Omega + R_L)]$$

Where R_L max = 1.79kΩ

and V_{OUT} max = -2.01V

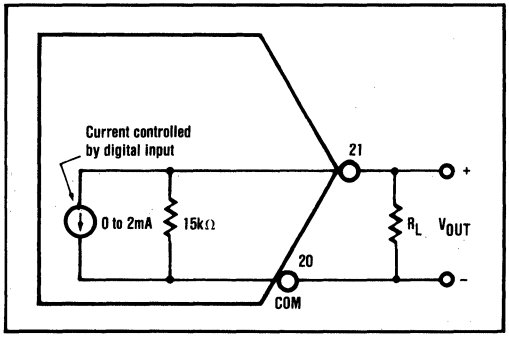


FIGURE 10. Equivalent Circuit DAC72-CSB-I Connected for Unipolar Voltage Output with Resistive Load.

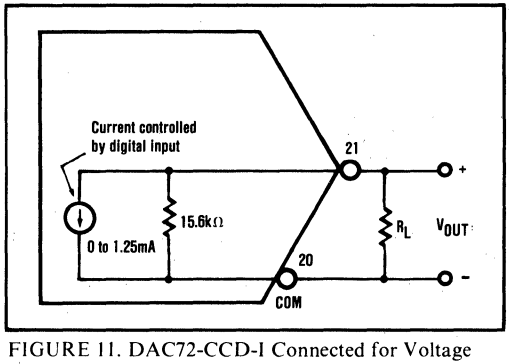


FIGURE 11. DAC72-CCD-I Connected for Voltage Output with Resistive Load.

DRIVING A RESISTIVE LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(4.44k\Omega \times R_L)/(4.44k\Omega + R_L)]$$

Where R_L max = 5.72kΩ
and V_{OUT} max = ±2.5V

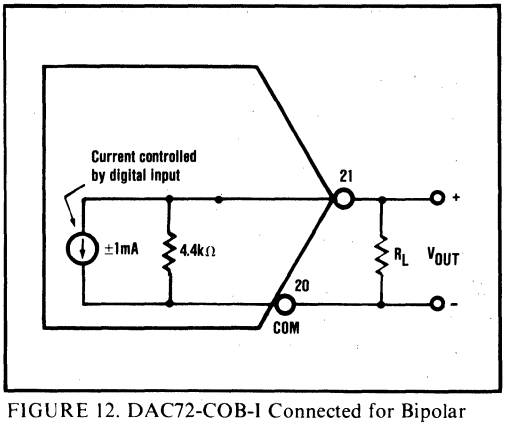


FIGURE 12. DAC72-COB-I Connected for Bipolar Output Voltage with Resistive Load.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DAC

The DAC72-(CSB, COB, CCD)-I are current output devices and will drive the summing junction of an op amp to produce an output voltage (see Figure 13). The op amp output voltage is:

$$V_{OUT} = -I_{OUT}\ R_F$$

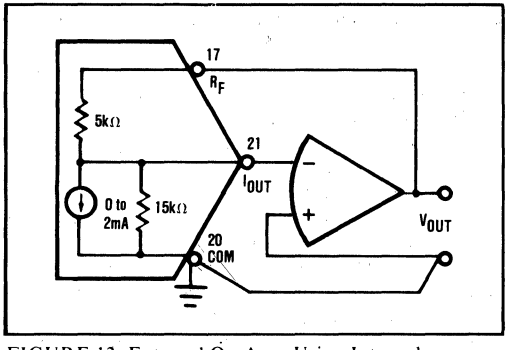


FIGURE 13. External Op Amp Using Internal Feedback Resistors.

Where I_{OUT} is the DAC72 output current and R_F is the feedback resistor. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

The DAC72 can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±25ppm/°C. The resistors in the DAC72 are chosen for ratio tracking of ±1ppm/°C and not absolute TCR (which may be as high at ±25ppm/°C.)

An alternative method of scaling the output voltage of the DAC72 and preserving the low gain drift is shown in Figure 14.

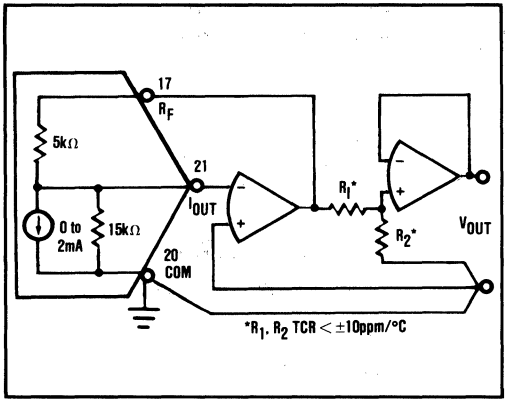


FIGURE 14. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

OUTPUTS LARGER THAN 20-VOLT RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges (see Figure 15). Use protection diodes when a high voltage op amp is used.

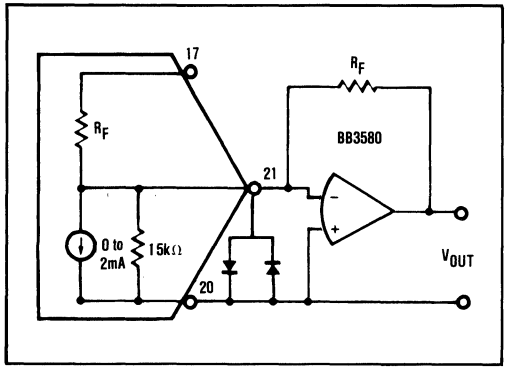


FIGURE 15. External Op Amp Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC72 consists of three primary components: gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the worst-case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst-case accuracy drift for a DAC72 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately. The following analysis is for the DAC72C although it applies to both models by simply substituting the proper temperature coefficients from the electrical specifications.

In the unipolar mode of operation, offset drift (±1ppm/°C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±5ppm/°C due to ratio drift of current switch V_{BE} to the reference transistor, 2) ±10ppm/°C due to the zener reference and, 3) ±2ppm/°C linearity drift due to ratio drift of current weighting resistors and V_{BE} of the quad current switches. The sum of these three components, ±17ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst-case accuracy drift in the unipolar mode is simply the sum of the components, or ±18ppm/°C.

In the bipolar mode the major portion of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 16 shows a simplified circuit diagram of a DAC72C-COB-V with all bits off. The current switch leakage current is negligible, so

$$V_{-FULL\ SCALE} = (-R_F / R_{BPR}) \cdot V_{REF}$$
$$= (-10k\Omega / 6.3k\Omega) \cdot 6.3V = -10V$$

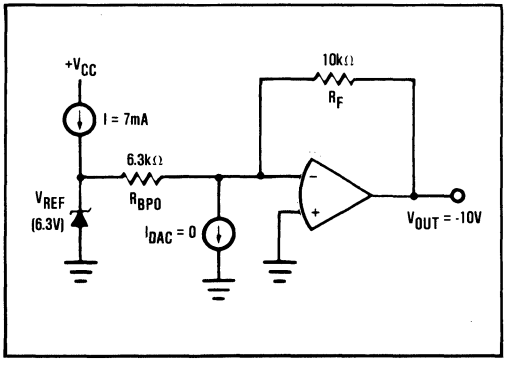


FIGURE 16. Simplified Diagram of DAC72C-COB-V with "All Bits Off" (±10V Range).

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is +10ppm/°C, this is equivalent to (+10ppm/°C) x (+6.3V) = +63V/°C. This will result in a voltage drift at the amplifier output of

$$\Delta V_{-FS} / \Delta T = -(R_F / R_{BPO}) \cdot (\Delta V_{REF} / \Delta T)$$
$$= -(10k\Omega / 6.3k\Omega) \cdot (63\mu V / °C) = -100\mu V / °C.$$

Since the DAC72C-COB-V is operating in the ±10V range this is equivalent to (-100μV/°C) ÷ (20V range) = -5ppm of FSR/°C.

Now consider the effect of reference changes on gain drift. When all of the bits are turned on it can be shown that:

$$\Delta V_{+FULL\ SCALE} / \Delta T = +(R_F / R_{BPO}) \cdot (\Delta V_{REF} / \Delta T)$$
$$= +(10k\Omega / 6.3k\Omega) \cdot (63\mu V / °C) = +100\mu V / °C$$

and (+100μV/°C) 20V Range = +5ppm/°C of FSR.

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the oppposite direction of, the drift of the plus full scale voltage and that zener reference variations have virtually no effect on the zero point (see Figure 17). This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm/°C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

Using this relationship, the worst-case accuracy drift for a DAC72C-COB-V can be computed. The maximum TCR of the zener reference is ±10ppm/°C. The gain drift due to the reference then is also ±10ppm/°C. The full scale drift and bipolar offset drift are each half that amount or

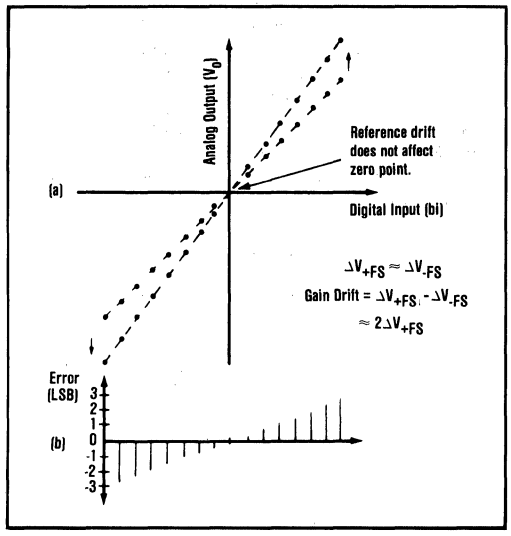


FIGURE 17. (a) Effect of a Positive Reference Drift on the Ideal D/A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC72.

±5ppm/°C. The maximum gain and offset drifts of the DAC72C, exclusive of the reference, are ±5 and ±3ppm/°C respectively. Adding this to the full scale drift due to the reference plus the linearity drift of ±2ppm/°C gives a worst-case total accuracy drift of ±15ppm/°C. (Random drifts, which these are can be in the same direction, so they add directly.) This is much less than the total drift obtained by simply adding the maximum gain, bipolar offset, and linearity drifts (±27ppm/°C). The maximum zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±5.5ppm of FSR/°C.

The DAC72C is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

total worst-case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.003% + ±15ppm/°C (45°) (100)
= ±0.07%

total worst-case bipolar zero point error
Bipolar zero drift x ΔT
= ±5ppm of FSR% (45°C) (100)
= ±0.025%

ORDERING INFORMATION

MODEL	TEMP RANGES	PKG	INPUT CODE
CURRENT MODELS			
DAC72C-COB-I	0°C to +70°C	Metal	Compl. Offset Binary
DAC72C-CSB-I	0°C to +70°C	Metal	Compl Straight Binary
DAC72C-CCD-I	0°C to +70°C	Metal	Compl. Coded Decimal
DAC72-COB-I	-25°C to +85°C	Metal	Compl. Offset Binary
DAC72-CSB-I	-25°C to +85°C	Metal	Compl. Straight Binary
DAC72-CCD-I	-25°C to +85°C	Metal	Compl. Coded Decimal
VOLTAGE MODELS			
DAC72C-COB-V	0°C to +70°C	Metal	Compl. Offset Binary
DAC72C-CSB-V	0°C to +70°C	Metal	Compl. Straight Binary
DAC72C-CCD-V	0°C to +70°C	Metal	Compl. Coded Decimal
DAC72-COB-V	-25°C to +85°C	Metal	Compl. Offset Binary
DAC72-CSB-V	-25°C to +85°C	Metal	Compl. Straight Binary
DAC72-CCD-V	-25°C to +85°C	Metal	Compl. Coded Decimal

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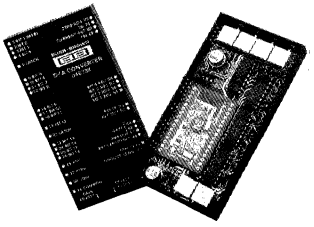
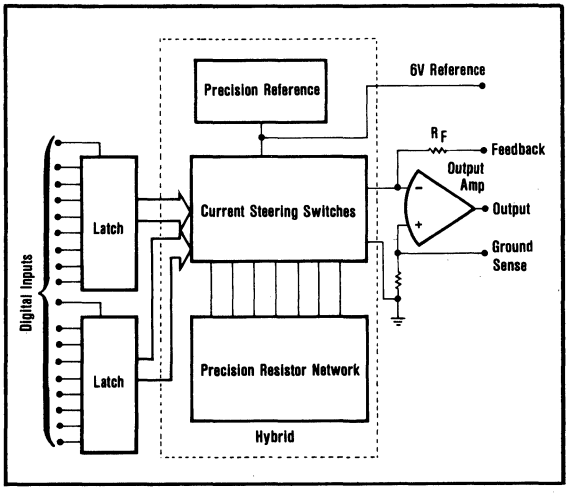


DAC73
DAC736

High Resolution
16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY
- LOW DRIFT
- CURRENT OR VOLTAGE OUTPUT
- INTERNAL GAIN, OFFSET, AND LINEARITY ADJUSTMENT
- LATCHED INPUTS (DAC73)
- LOW COST



DESCRIPTION

The DAC73 is a 16-bit modular high performance digital-to-analog converter in a 2" x 4" x 0.4" (50.8mm x 101.6mm x 10.2mm) package. The low drift and ultra-high linearity of the DAC73 provide voltage or current output signals that are accurate to ±0.00075% of full scale input range at 25°C ambient.

The critical components including the current steering switches, the temperature-compensated zener reference, and the precision laser-trimmed bit resistor network are contained in a single ceramic hybrid package.

The feedback and reference resistors are laid out for maximum stability with low current density and ±10ppm/°C maximum temperature coefficient with ±1ppm/°C tracking. This insures very-low superposition errors and low temperature coefficient of gain.

The inputs are TTL-compatible CMOS and contain level triggered latches in an 8-bit format for microprocessor data bus compatibility. No external components are required to achieve full 16-bit accuracy. Gain and offset potentiometers are also included in the DAC73.

The DAC736 has electrical specifications identical to the DAC73, but it is pin-compatible with the AD1136. The input latches, bit adjust pins, ground sense pin, and internal offset adjust pot are not included.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-419

SPECIFICATIONS

ELECTRICAL

T_A = 25°C and rated power supplies unless otherwise noted.

MODEL	DAC73J/DAC736J MIN	DAC73J/DAC736J TYP	DAC73J/DAC736J MAX	DAC73K/DAC736K MIN	DAC73K/DAC736K TYP	DAC73K/DAC736K MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution - CSB, COB			16			16	Bits
Logic Levels (TTL-Compatible CMOS)							
Logical "1" (at +1.0μA)	+3.5		+5.5	+3.5		+5.5	VDC
Logical "0" (at -0.5mA)	-0.5		+1.5	-0.5		+1.5	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at 25°C			±0.0015			±0.00075	% of FSR(1)
Gain Error,(2) Voltage CSB		±0.005	±0.02		±0.005	±0.02	%
COB		±0.01	±0.05		±0.01	±0.05	%
Current		±0.05	±0.25		±0.05	±0.25	%
Offset Error,(2) Voltage, Unipolar			±0.8			±0.8	mV
Bipolar			±10			±10	mV
Current, Unipolar			±1			±1	μA
Bipolar			±5			±5	μA
Monotonicity Temp. Range 16 Bits for K, 15 Bits for J		±15		+5		+35	°C
DRIFT (Over specified temp. range)							
Total Drift (includes gain, offset, and linearity drift)							
CSB		±9.5	±24		±9.5	±24	ppm of FSR/°C
COB		±9	±22		±9	±22	ppm of FSR/°C
Total Error over Temp. Range(3)							
Voltage, Unipolar 0°C to 70°C		±0.043	±0.108		±0.043	±0.108	% of FSR
Bipolar		±0.040	±0.099		±0.040	±0.099	% of FSR
Voltage, Unipolar 15°C to 35°C		±0.010	±0.024		±0.010	±0.024	% of FSR
Bipolar		±0.009	±0.022		±0.009	±0.022	% of FSR
Gain (Exclusive of reference drift)		±4	±10		±4	±10	ppm/°C
Offset (Exclusive of reference drift)							
Unipolar		±0.5	±2		±0.5	±2	ppm of FSR/°C
Bipolar		±2	±5		±2	±5	ppm of FSR/°C
Differential Linearity over Temperature		±1	±2		±1	±2	ppm of FSR/°C
Linearity Error over Temperature		±1	±2		±1	±2	ppm of FSR/°C
SETTLING TIME							
Voltage (to ±0.00075% of FSR)							
Output: 20V Step			50			50	μsec
1LSB Step(4)		6	10		6	10	μsec
Slew Rate		18			18		V/μsec
Current (to ±0.00075% of FSR)							
Output: 2mA Step		6			6		μsec
COB Switching Transient Magnitude		4.5			4.5		V
COB Switching Transient Energy		5			5		nJ
OUTPUT							
ANALOG OUTPUT							
Voltage Output							
Ranges - CSB		0 to +5			0 to +5		V
		0 to +10			0 to +10		V
COB		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Output Current - Unipolar			+4			+4	mA
Bipolar			±2			±2	mA
Output Impedance (DC)		0.03	0.05		0.03	0.05	Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
Current Output							
Ranges - CSB		0 to -2			0 to -2		mA
COB		±1			±1		mA
Output Impedance - Unipolar		15			15		kΩ
Bipolar		4.4			4.4		kΩ
Compliance		-1.5 to +10			-1.5 to +10		V
INTERNAL REFERENCE VOLTAGE	5.990	6.000	6.010	5.990	6.000	6.010	V
Maximum External Current(5)			+4			+4	mA
Temp. Coeff.		±4	±10		±4	±10	ppm/°C
OUTPUT NOISE							
Current, COB							
0.1Hz to 10Hz		1			1		nA, p-p
10Hz to 100kHz		4			4		nA, rms
Voltage, COB, ±10V Range							
0.1Hz to 10Hz		10			10		μV, p-p
10Hz to 100kHz		70			70		μV, rms

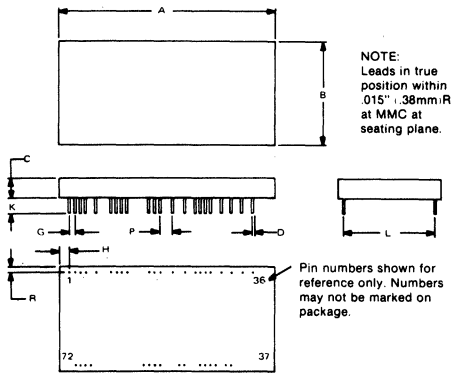
ELECTRICAL (CONT)

MODEL	DAC73J/DAC736J MIN	DAC73J/DAC736J TYP	DAC73J/DAC736J MAX	DAC73K/DAC736K MIN	DAC73K/DAC736K TYP	DAC73K/DAC736K MAX	UNITS
STABILITY, LONG TERM							
Gain (Exclusive of reference)		±30			±30		ppm/103hr
Offset COB (Exclusive of reference)		±30			±30		ppm of FSR/ 103hr
CSB		±5			±5		ppm of FSR/ 103hr
Linearity		±0.25			±0.25		LSB/103hr
Reference		±10			±10	±20	ppm/103hr
POWER SUPPLY SENSITIVITY							
Unipolar Offset							
±15VDC		±0.0001			±0.0001		% of FSR/% Vs
+5VDC		±0.0001			±0.0001		% of FSR/% Vs
Bipolar Offset							
±15VDC		±0.0004			±0.0004		% of FSR/% Vs
+5VDC		±0.0001			±0.0001		% of FSR/% Vs
Gain							
±15VDC		±0.001			±0.001		% of FSR/% Vs
+5VDC		±0.0005			±0.0005		% of FSR/% Vs
POWER SUPPLY REQUIREMENTS							
Rated Voltage		±15, +5			±15, +5		VDC
Range	±14.5, +4.75	±15, +5	±15.5, +5.25	±14.5, +4.75	±15, +5	±15.5, +5.25	VDC
Supply Drain, ±15VDC (no load		+35, -45	+50, -60		+35, -45	+50, -60	mA
+5VDC (logic supply		9			9		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Storage	-55		+100	-55		+100	°C

NOTES:
1. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
2. Adjustable to zero with internal trim potentiometer (offset adjustment external on DAC736).
3. With gain and offset errors adjusted to zero at 25°C.
4. LSB is for 16-bit resolution.
5. Maximum with no degradation of specifications.

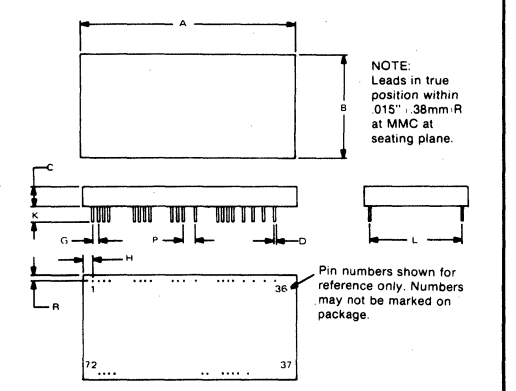
MECHANICAL

DAC73

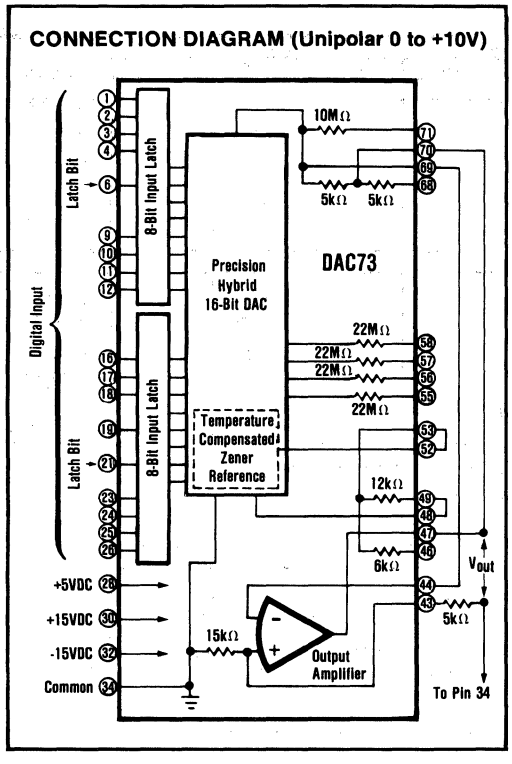


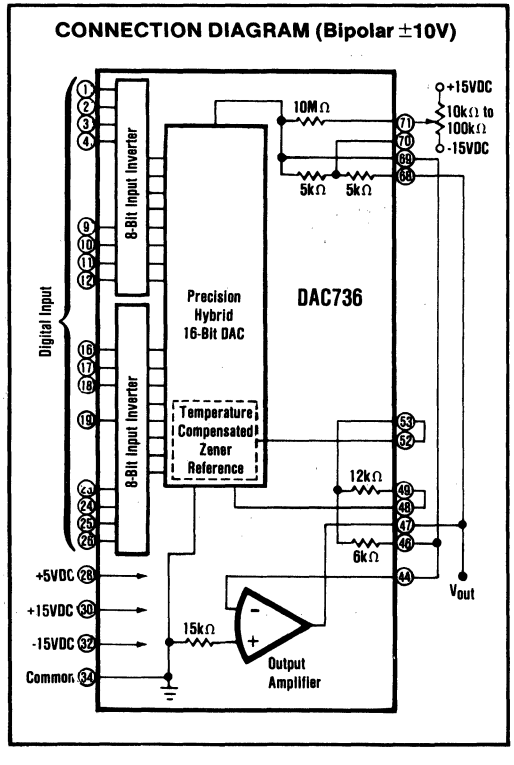
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.950	4.010	100.33	101.85
B	1.950	2.010	49.53	51.05
C	.350	.410	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	0.50	.150	1.27	3.81

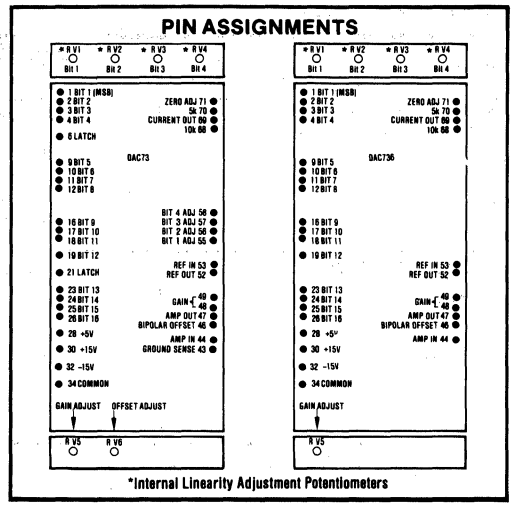
DAC736



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	3.950	4.010	100.33	101.85
B	1.950	2.010	49.53	51.05
C	.350	.410	8.89	10.41
D	.019	.021	0.48	0.53
G	.100 BASIC		2.54 BASIC	
H	.150	.250	3.81	6.35
K	.250	.350	6.35	8.89
L	1.800 BASIC		45.72 BASIC	
P	.200 BASIC		5.08 BASIC	
R	0.50	.150	1.27	3.81







DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC73/736 accepts complementary digital input codes in CSB or COB format. The COB model may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

	DIGITAL INPUT CODES			
CSB, COB MODELS	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Complement
All bits ON	0000...000	+Full Scale	+Full Scale	-1LSB
Mid Scale	0111...111	+1/2 Full Scale	Zero	-Full Scale
All Bits OFF	1111...111	Zero	-Full Scale	Zero
	1000...000	Mid Scale-1LSB	-1LSB	+Full Scale

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

INPUTS

Each bit input of the DAC73 consists of a buffered CMOS D type latch (see Figure 1). Bits 1 (MSB) through 8 are latched by a low level on pin 6. Bits 9 through 16 (LSB) are latched by a low level on pin 21. The latch inputs may be left open for transparent transfer of data.

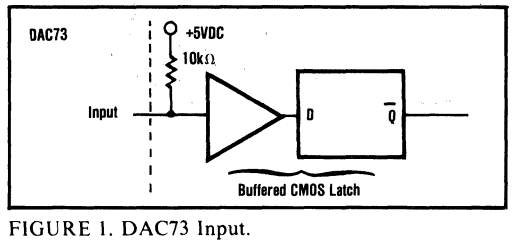


FIGURE 1. DAC73 Input.

The DAC736 inputs are CMOS inverters with 10kΩ pull-up resistors (see Figure 2).

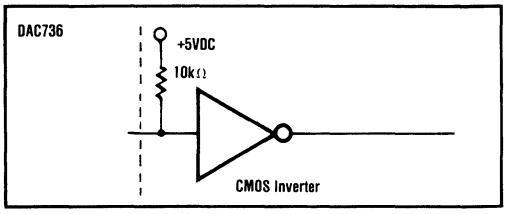


FIGURE 2. DAC736 Input.

The DAC73 and DAC736 can be driven directly by open collector or totem pole TTL logic.

ACCURACY

Linearity

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.00075% max (CSB, COB) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C (see Figure 3).

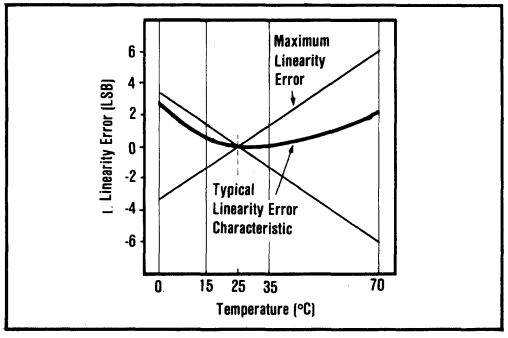


FIGURE 3. Nonlinearity vs Temperature.

Differential Linearity

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means than the output voltage step sizes can be anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

Monotonicity

Monotonicity over a ±5°C range for the DAC73 and DAC736 is guaranteed when ambient linearity is calibrated. This insures that the analog output will increase or remain the same for increasing 16-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in LSB's per °C (see Figure 4). Gain Drift is established by: 1) testing the end point differences for each DAC73 model at +25°C and the appropriate specification temperature extremes; 2) calculating the gain error with respect to the +25°C value; and 3) dividing by the temperature change. This is expressed in ppm/°C.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range.

The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

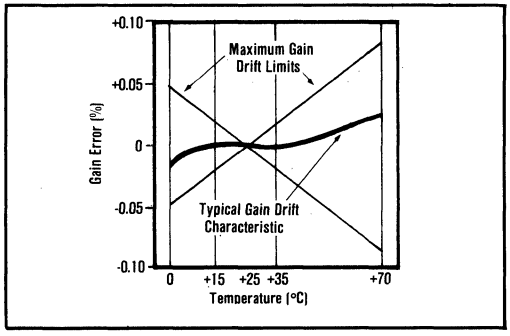


FIGURE 4. Gain Drift Error (%) vs Temperature.

SETTLING TIME

Settling time for each DAC73/736 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 5).

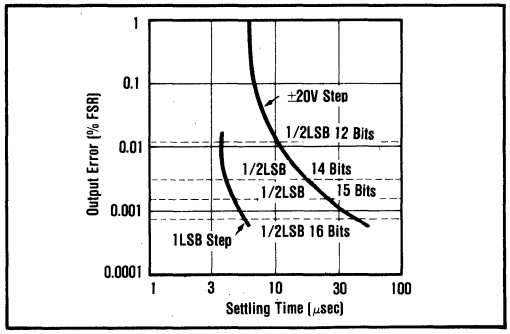


FIGURE 5. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.00075% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output while maintaining

specified accuracy. The maximum compliance voltage is -1.5V to +10V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 6).

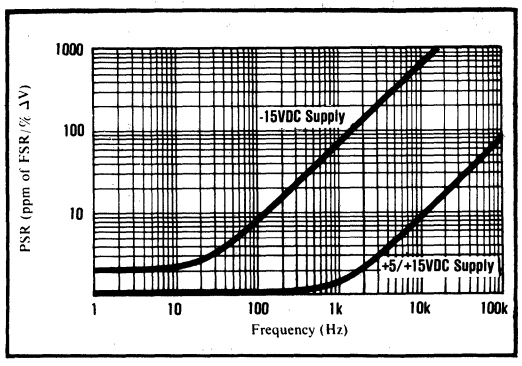


FIGURE 6. Power Supply Rejection vs Power Supply Ripple Frequency.

REFERENCE SUPPLY

All models are supplied with an internal +6V reference voltage supply. This reference voltage (pin 52) has a tolerance of ±0.05% and is connected internally for specified operation. The zener is selected for a Gain Drift of typically ±4ppm/°C and is burned-in for a total of 48 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 4mA and constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection the DAC73/736 decoupling capacitors are included internally. Refer to Figure 13 for correct grounding connections.

OFFSET AND GAIN ADJUSTMENT

Before taking measurements or making adjustments, the DAC73/736 should be warmed up for at least 25 minutes. The DAC73 has internal gain and offset potentiometers that are connected to an internal regulated supply. In most applications no external adjustment will be required.

External offset and gain adjustment of the DAC736, or DAC73 if the application requires, maybe accomplished as shown in Figures 7 and 8. These external circuits could be used in an application using both unipolar and bipolar modes. Refer to Figures 9 and 10 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters. The internal potentiometers could be used to null the unipolar gain and offset, and the external null could be switched in by relays to null bipolar gain and offset. An alternate offset adjustment is shown on the DAC736 connection diagram.

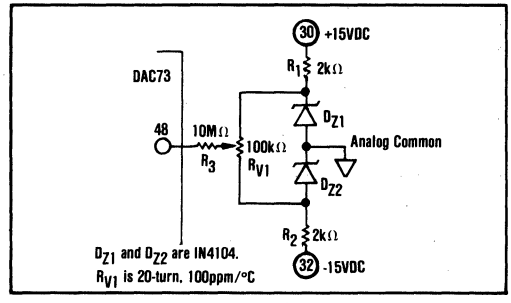


FIGURE 7. External Gain Adjustment.

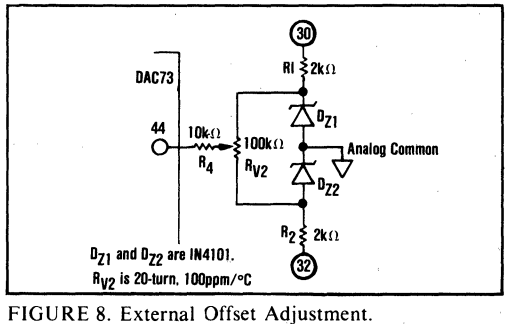


FIGURE 8. External Offset Adjustment.

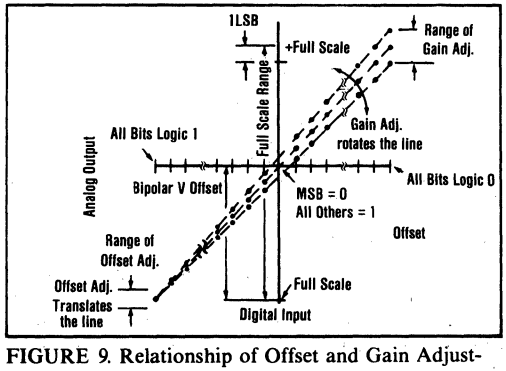


FIGURE 9. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

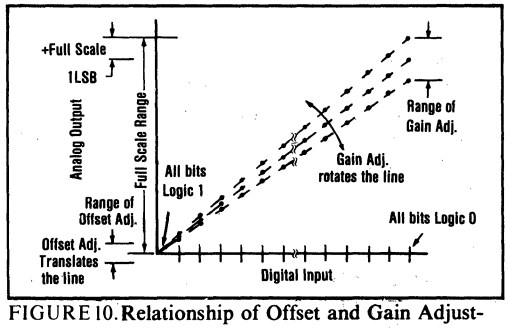


FIGURE 10. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors in the DAC73/736 provide a wide range of output voltage range connections. These internal resistors may be connected to provide three bipolar output voltage ranges of ±10V, ±5V, or ±2.5V or two unipolar voltage ranges of 0 to +5V or 0 to +10V. Since the internal scaling resistors are an integral part of the DAC73/736, gain and offset drift are minimized by their use. Connections for DAC73/736 are shown in Table II. Figure 11 is a connection diagram.

TABLE II. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 47 to	Connect Pin 46 to	Connect Pin 44 to	Connect Pin 68 to
±10V	COB	68	44	69	47
±5V	COB	70	44	69	NC
±2.5V	COB	70	44	69	69
0 to +10V	CSB	70	NC	69	NC
0 to +5V	CSB	70	NC	69	69

In all cases pins 52 and 53 and pins 48 and 49 should be shorted together with low resistance, capacitance connections.

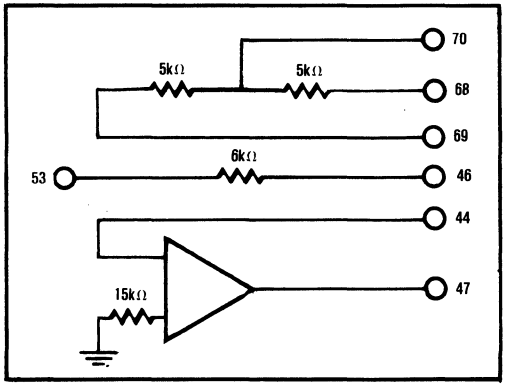


FIGURE 11. Output Amplifier Voltage Range Scaling Circuit.

LINEARITY ADJUSTMENT

Internal

If it becomes necessary to adjust the linearity of the DAC73 or DAC736 after an extended time period or for operation under temperature extremes, the 4MSB's may be user-adjusted. For optimum operation the unit should be calibrated in its operating environment. Calibration is performed by a differential linearity adjustment at the first four major carries. This method of calibration is possible since the DAC73 and DAC736 have almost no superposition error. The calibration procedure including gain, offset, and linearity adjustment is outlined in Table III. Steps 1 and 10 may be omitted for linearity adjustment only.

External (DAC73 only)

The linearity adjustment of the first 4MSB's of the DAC73 may be accomplished externally either with potentiometers or with D/A converters. Using a DAC to adjust linearity will allow computer controlled accuracy adjustments of the DAC thus giving the capability of maintaining 16-bit accuracy over all environmental variations. Gain and offset may also be adjusted in this manner.

Eight-bit bipolar voltage output DAC's can be used for all of the adjustments. Each circuit is shown in Figure 12.

INSTALLATION CONSIDERATIONS

To maintain the extremely-high accuracy of the DAC73 and DAC736 when installed in a system environment, careful attention must be paid to grounding and to connection resistances. Figures 13 and 14 are examples of correct connection configurations to yield maximum accuracy. The effects of various wiring and contact resistances R_1, R_2, R_3, and R_4 are reduced or eliminated as follows.

R_1 appears in series with the feedback resistance and therefore introduces only a gain error that can be nulled during calibration.

R_2 is inside the output amplifier feedback loop and its effect will be reduced by the loop gain.

In Figure 13 for the DAC736, R_3 is in series with the load

TABLE III. Calibration Procedure.

STEP	HEX INPUT CODE	ADJUST POTENTIOMETER(1)	DVM READING: UNIPOLAR MODE	DVM READING: ±10 VOLT BIPOLAR MODE	DESCRIPTION
1	FFFF	R_{V6}(2)	0.0V	-10.0000V	Null Offset
2	F000	N/A	V_4	V_4	Read Output Voltage
3	EFFF	R_{V4}	$V_4 + 153\mu V$	$V_4 + 305\mu V$	Adjust R_{V4} until DVM reads $V_4 + 1LSB$
4	E000	N/A	V_3	V_3	Read Output Voltage
5	DFFF	R_{V3}	$V_3 + 153\mu V$	$V_3 + 305\mu V$	Adjust R_{V3} until DVM reads $V_3 + 1LSB$
6	C000	N/A	V_2	V_2	Read Output Voltage
7	BFFF	R_{V2}	$V_2 + 153\mu V$	$V_2 + 305\mu V$	Adjust R_{V2} until DVM reads $V_2 + 1LSB$
8	8000	N/A	V_1	V_1	Read Output Voltage
9	7FFF	R_{V1}	$V_1 + 153\mu V$	$V_1 + 305\mu V$	Adjust R_{V1} until DVM reads $V_1 + 1LSB$
10	0000	R_{V5}	+9.999847V	+9.999695V	Adjust Gain

NOTES: 1. For potentiometer location see Pin Assignments. 2. External offset adjustment on DAC736.

resistor and will cause an error in the voltage across R_L. One-half LSB error would result at full load for R_3 = 0.02Ω. Therefore, if possible, sense the output voltage to include R_3.

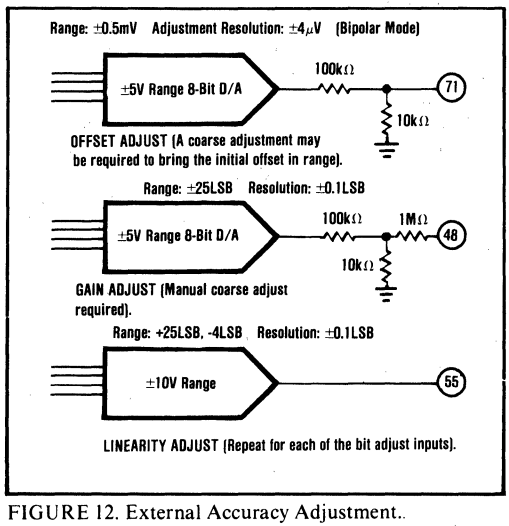


FIGURE 12. External Accuracy Adjustment..

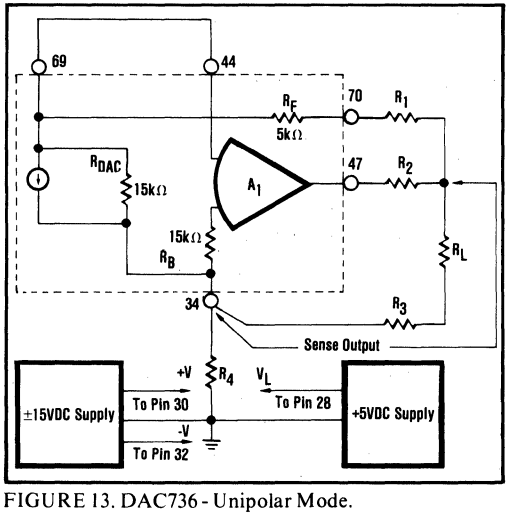


FIGURE 13. DAC736 - Unipolar Mode.

Figure 14 illustrates the optimum connection made possible by the ground sense pin on the DAC73. In the configuration shown $R'_F = R_F$ and $R'_B \parallel R_B = R_{DAC} \parallel R_{BPO}$. This causes any signal developed across R_3 to be rejected as a common-mode input, and R_3 will not affect the voltage across R_L. This configuration will also reject noise present on the system common.

R_4 is negligible in both circuits when ground connections are made as shown.

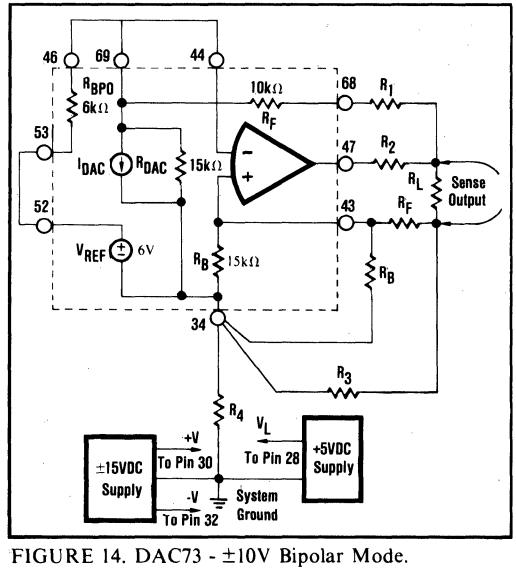


FIGURE 14. DAC73 - ±10V Bipolar Mode.

The DAC73/736 and the wiring to their connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area. Therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field.

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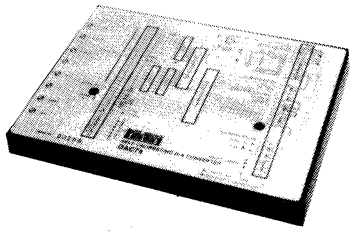


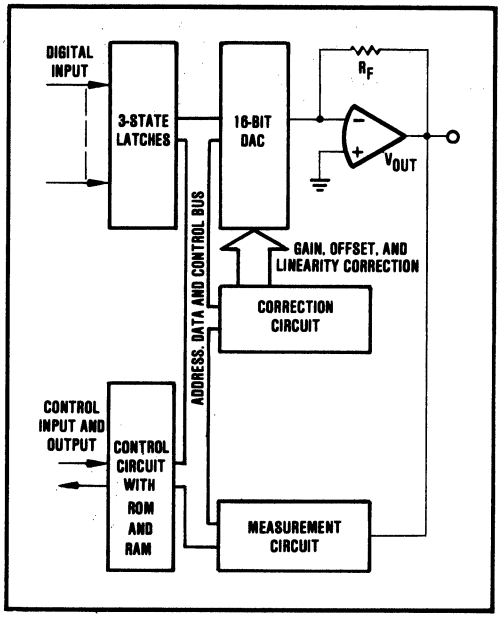
DAC74

Self-Calibrating High Resolution True 16-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT RESOLUTION
- SELF-CALIBRATION MAINTAINS ACCURACY OF
  - ±1/2LSB NONLINEARITY
  - ±0.00035% GAIN ERROR
  - ±40μV OFFSET

  } +15°C TO +45°C
- UNIPOLAR OR BIPOLAR VOLTAGE OUTPUT
- DOUBLE BUFFERED FOR AN 8- OR 16-BIT BUS



DESCRIPTION

The DAC74 is a self-contained true 16-bit Digital-to-Analog converter designed for applications requiring high resolution and accuracy such as displays, frequency synthesizers, automated test equipment, analytical instruments, and high resolution controllers. Furthermore, in applications where equipment is inaccessible or frequent calibration is impractical the DAC74 is ideal because the self-calibration accuracy depends only on the long term stability of a heated zener reference diode.

Using self-calibration circuits, the DAC74 maintains typically ±1LSB total error over +15°C to +45°C! Compare this with other high resolution converters which can only maintain this accuracy over a ±2°C or ±3°C range. A patented microprocessor-controlled differential measurement technique is the key contributor to the DAC74's drift performance. This technique allows use of low cost hybrid and monolithic circuits to remove linearity, gain, and offset errors resulting from ambient temperature variations, component aging, and varying load conditions.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-442

SYSTEM DESCRIPTION

The DAC74 is a self-calibrating, 16-bit digital-to-analog converter in a 5" x 7" x 0.6" (127mm x 178mm x 15.2mm) package. This D/A converter provides either a unipolar or a bipolar voltage output that is linear to within ±1/2LSB of the Full Scale Range (FSR). The FSR in the unipolar mode is set by the internal +10V reference. The FSR in the bipolar mode is set by the difference between the +10V and the -10V references. With respect to the internal references, the offset and gain errors are also less than ±1/2LSB. The settling time to ±1/2LSB is typically 6μsec for a 1LSB step.

A microprocessor-controlled calibration circuit retrims the D/A converter to this accuracy in the face of drift over temperature and time. The absolute accuracy of the calibration is dependent upon the accuracy of the internal voltage references. The drift of the reference is typically ±0.5ppm/°C.

The linearity and accuracy of the DAC74 versus temperature is illustrated in Figures 1 and 2. The calibration was performed at 5°C intervals. It can be seen that the calibration greatly increases the useful temperature range of the D/A converter.

The DAC74 (see Figure 3) consists of (1) a 16-bit, latched input main D/A converter, which performs the digital-to-analog conversion, (2) a stable, temperature-compensated voltage reference, (3) an error-measuring circuit which compares the D/A converter output to known references, and (4) a microcomputer-based controller that stores the output of the error measuring circuit and calculates correction factors for offset, gain, and linearity. The controller stores these correction factors in RAM and these are used to adjust errors when an input data word selected by the user is presented at the input to the main D/A converter.

The critical components, including the current steering switches and the laser-trimmed resistor network, are contained in a single ceramic hybrid package for improved thermal tracking. The zener reference is maintained at a constant temperature to reduce drift due to ambient temperature fluctuations.

The DAC74 is housed in a steel package which provides excellent electromagnetic shielding. The package can be mounted from either side for socket mounting or for use of ribbon cable connectors.

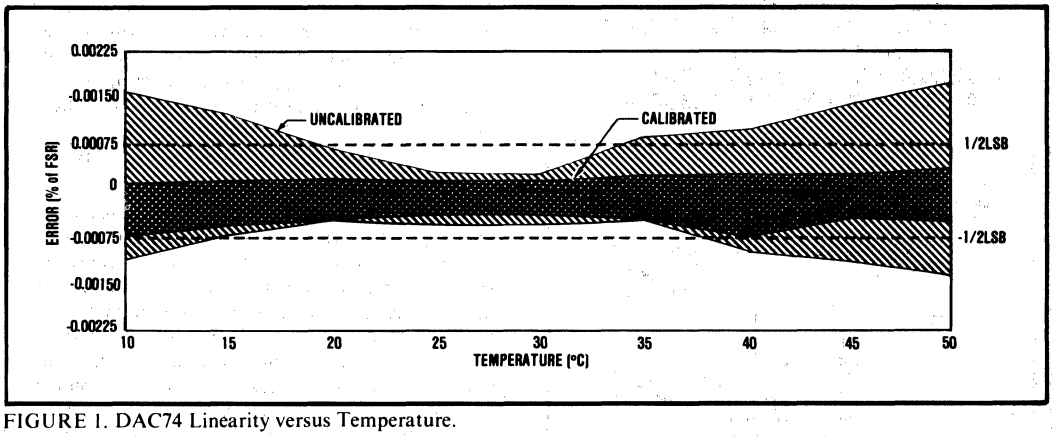


FIGURE 1. DAC74 Linearity versus Temperature.

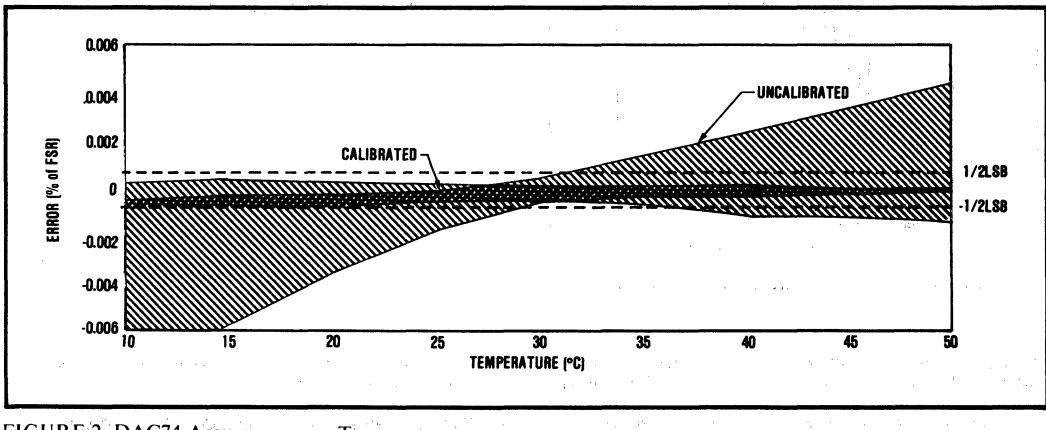


FIGURE 2. DAC74 Accuracy versus Temperature.

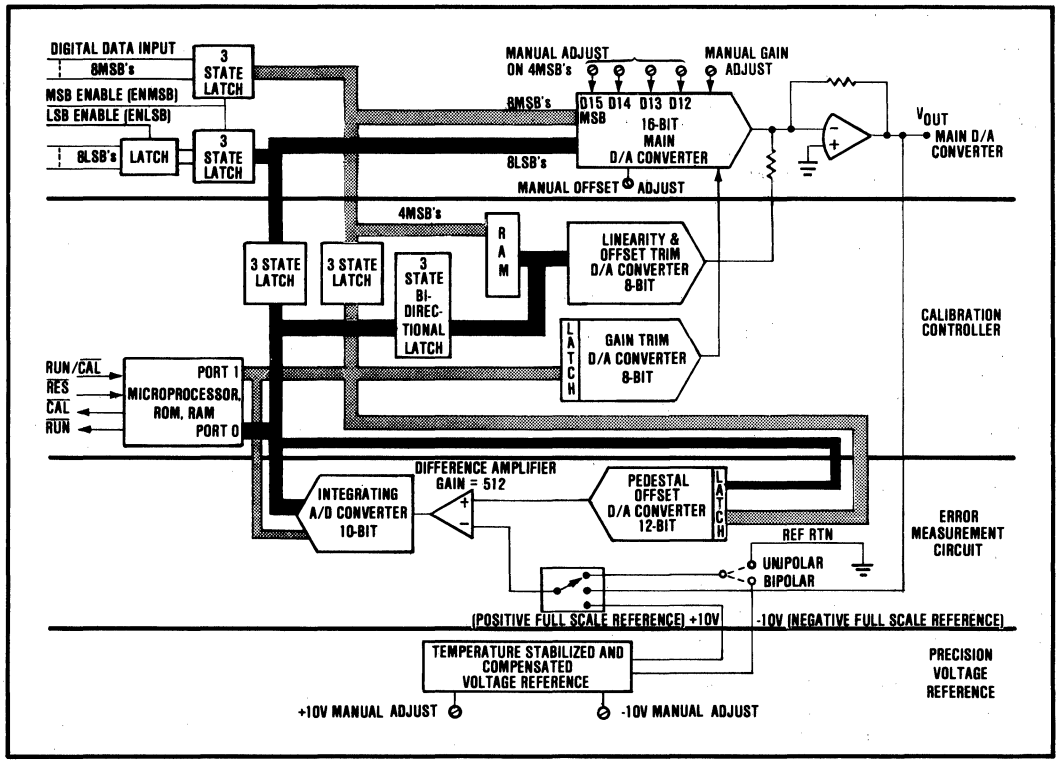


FIGURE 3. DAC74 Block Diagram.

A user initiates a calibration by applying a negative pulse to the reset input $\overline{RES}$ with the RUN/$\overline{CAL}$ input held low. After an initial system check, the $\overline{CAL}$ status goes low and a 2.5 second calibration cycle is started. During calibration, the external inputs are disabled and the $\overline{RUN}$ status is high. The D/A converter returns to the RUN mode at the end of the calibration cycle. $\overline{CAL}$ remains low in the RUN mode if the calibration was successful. The $\overline{RUN}$ status output is low during normal D/A converter operation; in this state, the external digital data inputs are routed to the main D/A converter.

THE MAIN D/A CONVERTER

The 16 data inputs to the main D/A converter are buffered by two octal latches that are enabled by a high input to ENMSB. In addition, the 8LSB's are double buffered by a latch with an enable input labeled ENLSB. This arrangement allows transparent operation, a 16-bit interface, or an 8-bit interface. The data inputs are positive true. The MSB is labeled D15 and the LSB is labeled D0. Both latches transfer their inputs to the output when the enable is high. The input data is held in the latch when the enable is low.

Four potentiometers adjust the bit currents for the 4MSB's. Two more potentiometers allow the Offset and Gain to be adjusted manually. After a calibration period of 1 year, these potentiommeter adjustments may be required to trim the D/A converter to within the error range which can be trimmed by the self-calibration circuits. The procedure is given in the Manual Calibration section.

The output operational amplifier converts the 0 to 2mA current from the bit switches into a voltage output. A 5-wire output connection to the main D/A converter is described in the Installation section. All five wires MUST be installed to the load as indicated to obtain the full specified accuracy.

The output connection diagrams for 0 to +10V unipolar operation or ±10V bipolar operation are shown in the Installation section. Jumpers must be installed to configure the main D/A converter and the calibration circuits for each of these output configurations.

PRECISION VOLTAGE REFERENCES

The +10V and -10V references, shown in Figure 3, supply the voltage standards for calibrating the main D/A converter. The -10V reference is required only for bipolar operation. The ±10V references derive their outputs from a heated zener reference diode. In addition, both reference circuits are temperature compensated to cancel variations caused by drift in the other components of the reference. The accuracy of these references over temperature and time determine the accuracy of the D/A converter after calibration. These reference voltages are available for external use but the load must remain constant. Alternatively, external +10V and -10V references may be used with the DAC74.

ERROR MEASUREMENT CIRCUIT

The error measurement circuit of the DAC74 includes an analog switch, differential instrumentation amplifier, pedestal offset D/A converter, and an analog-to-digital converter. The circuit measures a sequence of voltage pairs. The error of the main D/A converter trim is derived from the differences in each pair of voltages. For instance, the Offset error is the difference between the minus full scale D/A converter output and the minus full scale reference (RTN for unipolar and -10V for bipolar). The Gain error is the difference between the plus full scale D/A converter output and the +10V reference less 1LSB.

The analog switch selects one of three sources as the input to the instrumentation amplifier. These sources are the main D/A converter output, minus full scale reference, and the plus full scale reference. The analog switch is controlled by the calibration controller.

The difference amplifier derives one of its inputs from a pedestal offset D/A converter which provides a voltage roughly comparable to the other input. The other input comes from the analog switch. During any pair of measurements, the pedestal offset D/A converter output remains the same. Since the gain of the instrumentation amplifier is 512, small differences (20μV) in the voltage pair are detected by the analog-to-digital converter connected to the output of the difference amplifier. The input to the pedestal offset D/A converter is set to the same value as that sent to the main D/A converter so that the high gain difference amplifier will stay within its linear range. The accuracy of the pedestal offset D/A converter does not affect the calibration accuracy.

The 10-bit analog-to-digital converter translates the output of the difference amplifier into a digital code for the microcomputer-based controller. Only the difference in the readings between a pair of measurements is used by the controller. The Gain and Offset of this 10-bit analog-to-digital converter are preset at the factory. The control signals to the A/D converter are generated by the controller during a calibration cycle.

CALIBRATION CONTROLLER

The Calibration Controller consists of a microcomputer which has three functions; (1) interpret commands from the control inputs and terminal interface, (2) conduct measurements by sending control signals to the error measurement subsystem, and (3) calculate the trims to be sent to the trim D/A converters. In the RUN mode, the microcomputer is idle; in fact, it can be turned off to reduce noise by asserting the MPUOFF control input high or leaving it open. The user may initiate a calibration cycle with a negative pulse to the $\overline{RES}$ control input with the MPUOFF and the RUN/$\overline{CAL}$ control inputs both low. At the end of the pulse to $\overline{RES}$, the $\overline{RUN}$ status output goes high indicating the main D/A converter is no longer under user control. As discussed in the Manual Calibration section, the $\overline{CAL}$ output goes low indicating that the calibration process is underway. At the end of the calibation, the $\overline{RUN}$ status will return low. If and only if the calibration succeeds, the $\overline{CAL}$ status will remain low.

The two status outputs $\overline{RUN}$ and $\overline{CAL}$ are open-collector TTL outputs (7406) which can drive an LED indicator directly. At the end of the calibration, the controller automatically returns to the RUN mode and control of the main D/A converter inputs is returned to the user.

The Offset is first adjusted with respect to the minus full scale reference. Then a sequence of four differential linearity measurements are conducted on the four MSB's of the D/A converter. Starting with the LSB of these four bits, each bit is trimmed to be linear with respect to all the lesser significant bits. After the linearity is established, a final gain correction is made with respect to the full scale reference. If the calibration fails, either a component has failed, or the internal drift of the system has exceeded the range of the trim circuit. If calibration under normal operating conditions fails, adjustments of eight potentiometers must be made to restore the D/A converter to its original accuracy. A detailed description of the calibration procedure is contained in the Manual Calibration section.

The trim circuits of the DAC74 consist of 16 RAM locations, Linearity/Offset trim D/A converter, and a Gain trim D/A converter. As shown in the block diagram, the RAM address inputs are taken from either a latch connected to the controller bus or from the four MSB's of the data input to the main D/A converter. In the RUN mode, the four inputs from the main D/A converter select one of 16 digital codes. The 8-bit code selected by the address inputs constitutes the sum of the corrections for the Offset error and the sum of the bit errors for those bits of the upper four which are logic ones. For instance, the RAM location 0 contains the digital code for just the Offset correction since none of the upper four bits are turned on. The RAM location 8 contains the digital code for the sum of the Offset correction and the correction for the MSB error. During calibration, the controller addresses the RAM. It first zeros the RAM and then adds the correction for the Offset error to all the RAM locations. Then the corrections for the bit errors are added to those locations which have that bit turned on. For instance, the correction for the MSB is added to all locations whose address starts with one (1XXX). The 8-bit digital code from the RAM is the input to the Offset/Linearity trim D/A converter. The output of the trim D/A converter makes a slight adjustment in the total current of the main D/A converter (one part in 2048). The maximum trim in the unipolar mode is ±2.44lmV. With an 8-bit resolution trim D/A converter, the minimum possible trim is 1/8LSB or 0.019mV at the main D/A converter output.

A final Gain trim is made by sending a separate 8-bit trim word to the Gain D/A converter. The Gain error is the deviation of the full scale output from the full scale reference (+10V -1LSB). The maximum and minimum correction range in the full scale output are the same as the linearity/offset maximum and minimum, 2.441mV.

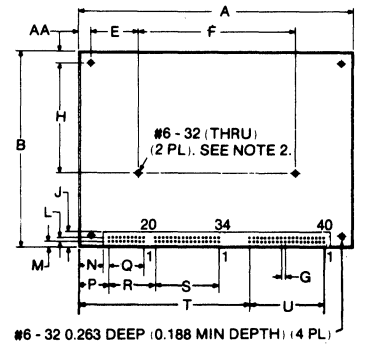
SPECIFICATIONS

ELECTRICAL

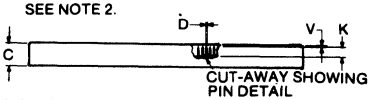
T_A = 25°C, rated power supplies and after 30 minute warm-up unless otherwise noted.

MODEL	DAC74			
	MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Resolution			16	Bits
Voltage Levels				
Logic 1, V_{IH}	+2		+5.5	VDC
Logic 0, V_{IL}	0		+0.8	VDC
Current				
D0-D15, ENLSB, ENMSB (SN74LS373)				
I_{IH}, V_I = 2.7V			20	µA
I_{IL}, V_I = 0.4V			-0.4	mA
$\overline{RES}$, RUN/$\overline{CAL}$, $\overline{UNIPOLAR\ CAL}$				
I_{IH}, V_I = 2.4V			40	µA
I_{IL}, V_I = 0.4V			-1.6	mA
MPUOFF (inc. 10kΩ pullup)				
I_{IH}, V_I = 2.4V			-0.3	mA
I_{IL}, V_I = 0.4V			-2.1	mA
ANALOG OUTPUT				
Ranges, Unipolar		0 to +10		V
Bipolar		±10		V
Output Impedance (DC)		0.03	0.05	Ω
Short Circuit to Common (Duration)		Indefinite		
Load Current	±5			mA
Settling Time (to ±1/2LSB)				
20V Step		20	50	µsec
1LSB Step(1)			10	µsec
Slew Rate		18		V/µsec
Noise				
Voltage, Bipolar				
0.1Hz to 10Hz		10		µV, p-p
10Hz to 100Hz		70		µV, rms
DIGITAL OUTPUT				
Open Collector (SN7406) (with 10kΩ Pullup)				
Voltage Levels				
Logic 1	+2.4			V
Logic 0			+0.4	V
Current (with 10kΩ Pullup)				
$\overline{CAL}$, $\overline{RUN}$				
I_{OH}			1	mA
I_{OL}			-15	mA
TRANSFER CHARACTERISTICS AFTER SELF-CALIBRATION CYCLE				
Accuracy(2)				
Total Error				
Unipolar			±0.0015	% of FSR(3)
Bipolar			±0.0015	% of FSR
Linearity Error			±1/2	LSB
Gain, Error, Unipolar			±0.00035	% of output
Bipolar			±0.00035	% of output
Offset Error, Unipolar			±40	µV
Bipolar			±80	µV
Monotonicity after Calibration, 16 bits		Guaranteed		
DRIFT				
Total Error Drift (includes gain, offset and linearity drift(4))				
Unipolar		±4	±9	ppm of FSR/°C
Bipolar		±5	±11	ppm of FSR/°C
Total Error over Temp Range				
Voltage, Unipolar (0°C to 70°C)			±0.06	% of FSR
Bipolar			±0.06	% of FSR
Voltage, Unipolar (+15°C to +45°C)			±0.013	% of FSR
Bipolar			±0.013	% of FSR
Gain (exclusive of reference drift)		±2	±5	ppm/°C
Offset (exclusive of reference drift)				
Unipolar		±0.5	±1	ppm of FSR/°C
Bipolar		±2	±3	ppm of FSR/°C
Differential Linearity over Temperature		±1	±2	ppm of FSR/°C
Linearity Error over Temperature		±1	±2	ppm of FSR/°C
PRECISION 10V REFERENCES				
Voltage(5)	±9.9995	±10.00	±10.0005	V
Drift vs Temperature		±0.5	±1	ppm/°C
External Current(6)			±4	mA

MECHANICAL



#6 - 32 0.263 DEEP (0.188 MIN DEPTH) (4 PL)
SEE NOTE 2.

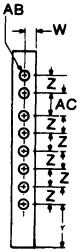


CUT-AWAY SHOWING
PIN DETAIL

NOTES:
1. Leads in true position within 0.015" (0.38mm) R at MMC at seating plane.
2. Holes in true position within 0.015" (0.38mm) R at MMC.

CASE MATERIAL: Epoxy coated steel
LABEL: Metal foil
WEIGHT: 20oz. (257gm.) max.
PIN: Gold Flashed
Mating Connectors
shipped with DAC74:

AMP86418-1	20 pin, P1 Test Interface
AMP1-86418-8	34 pin, P2 Digital
AMP86418-2	40 pin, P3 Analog

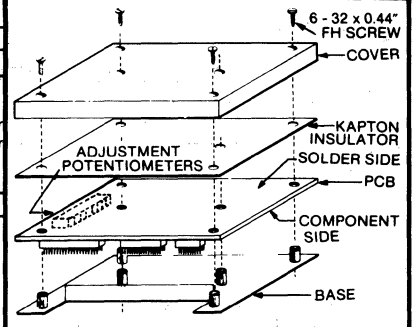


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	6.980	7.020	177.29	178.31
B	4.980	5.020	126.49	127.51
C	.550	.600	13.97	15.24
D	.022	.028	.56	.71
E	1.112 BASIC		28.24 BASIC	
F	4.150 BASIC		105.41 BASIC	
G	.100 BASIC		2.54 BASIC	
H	2.837 BASIC		71.98 BASIC	
J	.353	.373	8.97	9.47
K	.308	.328	7.82	8.33
L	.100 BASIC		2.54 BASIC	
M	.143	.183	3.63	4.65
N	.573	.613	14.55	15.57
P	.730	.770	18.54	19.56
Q	.900 BASIC		22.86 BASIC	
R	1.200 BASIC		30.48 BASIC	
S	1.600 BASIC		40.64 BASIC	
T	3.600 BASIC		91.44 BASIC	
U	1.900 BASIC		48.26 BASIC	
V	.020	.040	.51	1.02
W	.267	.287	6.78	7.29
Y	.831	.851	21.11	21.62
Z	.430	.470	10.92	11.94
AA	.293	.333	7.44	8.46
AB	.240	.260	6.10	6.60
AC	.565	.585	14.35	14.86

ELECTRICAL (CONT)

MODEL	DAC74			
	MIN	TYP	MAX	UNITS
STABILITY, LONG TERM				
Gain (exclusive of reference)		±30		ppm/10³ hr
Offset (exlusive of reference)				
Unipolar		±5		ppm of FSR/10³ hr
Bipolar		±30		ppm of FSR/10³ hr
Linearity		±0.25	±0.5	LSB/10³ hr
Precision 10V References		±20		ppm/10³ hr
POWER SUPPLY SENSITIVITY				
Unipolar Offset				
+15V and -15V Supplies		±0.0001		% of FSR/%Vs
+5V Supply		±0.0001		% of FSR/%Vs
Bipolar Offset				
+15V and -15V Supplies		±0.0004		% of FSR/%Vs
+5V Supply		±0.0001		% of FSR/%Vs
Gain				
+15V and -15V Supplies		±0.001		% of FSR/%Vs
+5V Supply		±0.0005		% of FSR/%Vs
POWER SUPPLY REQUIREMENTS				
Range	±14.5, +4.75	±15, +5	±15.5, +5.25	V V
Supply Drain, ±15VDC (not including output load)			200	mA
Current Surge, +15V Supply(7)			400	mA
+5VDC Supply			800	mA
TEMPERATURE RANGE				
Self-calibration Operation	+15		±45	°C
Drift Specification	0		+70	°C
Storage	-55		+100	°C
TIMING SPECIFICATIONS				
Control and Status Timing(8)				
t_{on}	50			msec
t_{RES}	14			µsec
t_{IN}			500	µsec
td_0		100		µsec
td_1		100		µsec
t_{RUN} (self-cal mode)		2.5	3	sec
t_{RUN} (service mode)		300	350	msec
Data Input Timing				
$t_{ENLSB, ENMSB}$ (pulse width t_W)	15			nsec
t_{su} (data input setup time)	20			nsec
t_h (data input hold time)	10			nsec

MECHANICAL (CONT)



Screws holding the package together are covered by the top label (not shown). If the package must be opened, the top label must be peeled back at the corners. The package is mounted through inserts in the corners when the connectors are mounted pins-down or through the two holes in the center of the package when the connectors are mounted pins-up.

Manual calibration potentiometers are located on one end of the package. The potentiometers are accessed by peeling off the label on the edge of the package.

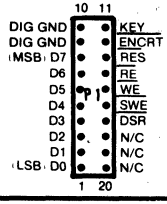
NOTES:

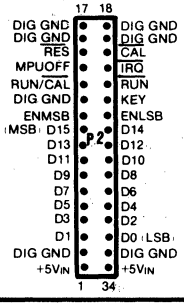
1. 1LSB at 16 bits = 0.00152% of FSR, = 15.2ppm of FSR, 152µV unipolar, 304µV bipolar.
2. Self-calibration can operate over +15°C to +45°C. DAC74 meets these specifications after the calibration cycle. These assume that the ±10V references have been adjusted to ±10.0000V ±10µV after 30-minute warm-up.
3. FSR means Full Scale Range and is 20V for bipolar and 10V for unipolar.
4. DAC74 will operate as a D/A converter over 0°C to +70°C. Self-calibration feature may be out of correctable range over a temperature range wider than +15°C to +45°C.
5. Manually adjustable to +10.00000 and -10.00000 after 30-minute warm-up.
6. Maximum with constant load for no degradation of specifications.
7. The heater current of the heated zener reference momentarily causes the initial power-up current of the +15V supply to approach 400mA. The +15V supply current then tapers to less than 200mA within 3 seconds.
8. See Operation section for timing diagrams.

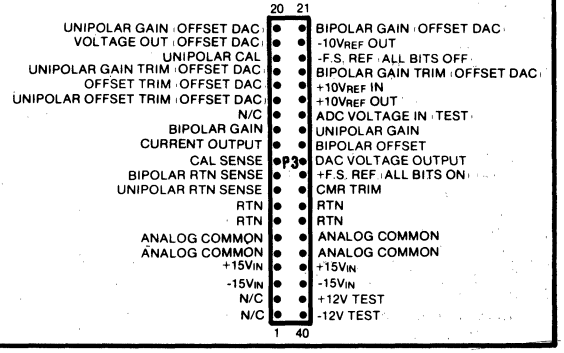
PIN CONFIGURATION

Connector P1 is a special service and test connector used by the factory. P2 is the Digital I/O connector containing the 16 input lines to the D/A converter, the control and status signals, and the +5V supply pins. Connector P3 contains all analog function pins for output, output sense, references, options, analog test points, and ±15V power supply input.

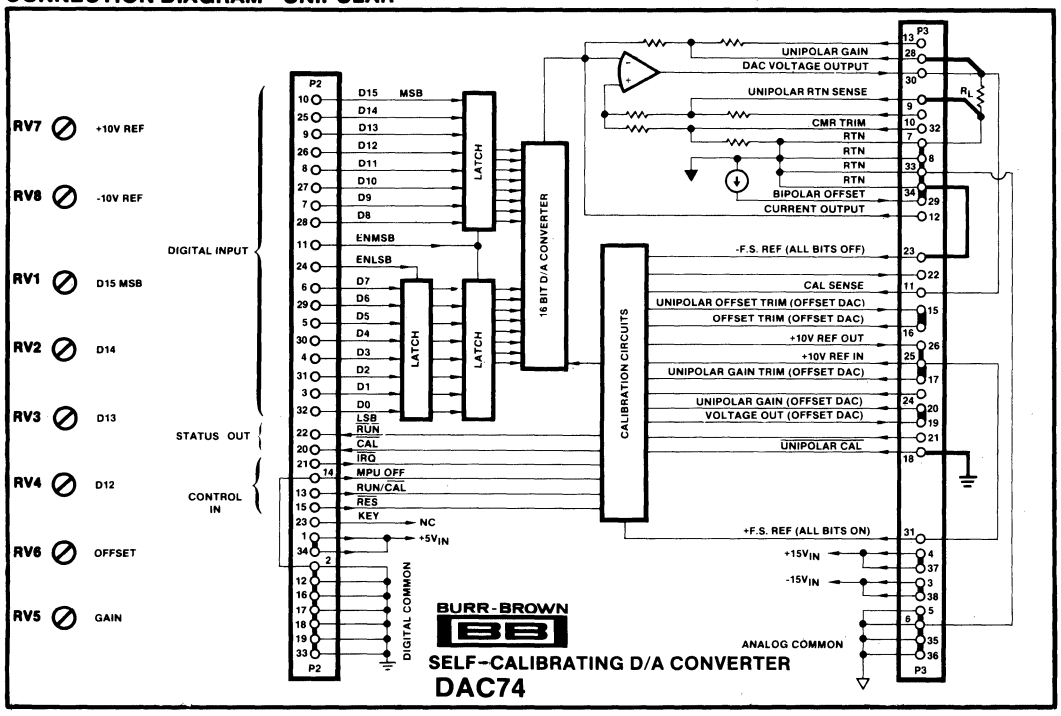
The DAC74 is delivered complete with mating connectors for printed circuit mounting.



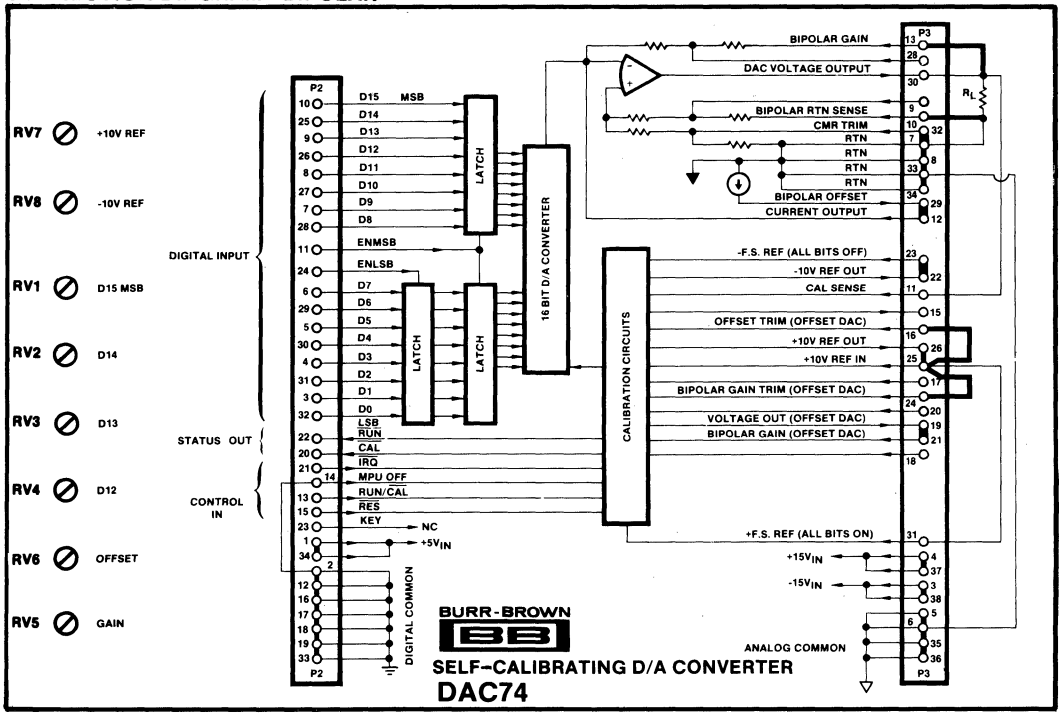




CONNECTION DIAGRAM - UNIPOLAR



CONNECTION DIAGRAM - BIPOLAR



DESCRIPTION OF PIN FUNCTIONS

CONNECTOR P1

Connector P1 is a test connector used by the factory. It is not described in this data sheet.

CONNECTOR P2 (Digital Signal Connector)

Pin No.	Designation	Function
1	$+5V_{IN}$	+5V supply input. Connected internally to pin 34.
2	DIGITAL COMMON	+5V supply return. Connected internally to pins 12, 16, 17, 18, 19, 33.
3 through 10	D1, D3, D5, D7, D9, D11, D13, D15	Data input to the Main D/A. D15 is the MSB. Logic 1 is a high input logic level.
11	ENMSB	Enable for the data input latches. Controls the MSB byte latch and the 2nd latch in the double-buffered LSB byte. Level triggered on high level.
12	DIGITAL COMMON	+5V supply return.
13	RUN/$\overline{CAL}$	Control input. Low input for SELF-CALIBRATION mode. High input for SERVICE, the manual calibration mode.
14	MPU OFF	Controls microprocessor oscillator. Low - ON, High - OFF. Must be low for 50msec before $\overline{RES}$ is asserted.
15	$\overline{RES}$	Control input. Resets the DAC74 controller and subsequently causes the RAM to be cleared and "calibration" or "service" to begin. Input is a logic 0 (low) pulse with 14μsec minimum width.
16, 17, 18, 19	DIGITAL COMMON	+5V supply return.
20	$\overline{CAL}$	Status Output. Informs the user if calibration failed. Logic low means calibration successful.
21	$\overline{IRQ}$	An internal microprocessor control input. Not used by user.
22	$\overline{RUN}$	Status Output. This is high during the time the calibration controller has control of the main D/A converter.
23	KEY	This pin may be used to key the module to protect against incorrect plug-in alignment.
24	ENLSB	Enable input for LSB byte latch. Level triggered on high level.
25 through 32	D14, D12, D10, D8, D6, D4, D2, D0	Data input to the main D/A. D0 is the LSB. Logic 1 is high logic level.
33	DIGITAL COMMON	+5V supply return.
34	$+5V_{IN}$	+5V supply input.

CONNECTOR P3 (Analog Connector)

Pin No.	Designation	Function
1, 2	NC	No connection.
3	$-15V_{IN}$	-15V supply input. Connected internally to pin 38.
4	$+15V_{IN}$	+15V supply input. Connected internally to pin 37.
5, 6	ANALOG COMMON	Return for ±15V supply. Connected internally to pins 35 and 36.
7, 8	RTN	Analog return for the analog output. Connected internally to pins 33 and 34.
9	UNIPOLAR RTN SENSE	Unipolar Return Sense. Analog load sense for unipolar output configuration.
10	BIPOLAR RTN SENSE	Bipolar Return Sense. Analog load sense for bipolar output configuration.
11	CAL SENSE	Calibration Sense. A connection to sense the D/A output at the load and provide an input to the error measurement circuit.
12	CURRENT OUTPUT	A connection to the current output of the bit switches. Used to connect Bipolar Offset, pin 29.
13	BIPOLAR GAIN	Connection to scale the output amplifier for bipolar output range (-10 to +10V) and to provide a sense input from the load.
14	NC	No connection.
15	UNIPOLAR OFFSET TRIM (OFFSET DAC)	Connects an internal trim network to pin 16 for unipolar operation. This network is factory set.
16	OFFSET TRIM (OFFSET DAC)	Offset trim input connection to the pedestal offset D/A converter.
17	UNIPOLAR GAIN TRIM (OFFSET DAC)	Gain trim input connection to the pedestal offset D/A converter for unipolar operation.
18	UNIPOLAR CAL	A digital option line selecting the software routine calibrating the main D/A converter for the bipolar or unipolar configuration.
19	VOLTAGE OUT (OFFSET DAC)	Analog output of the pedestal offset D/A converter.
20	UNIPOLAR GAIN (OFFSET DAC)	Connects the pedestal offset D/A converter for 0 to +10V output range. Connect to pin 19.
21	BIPOLAR GAIN (OFFSET DAC)	Connects the pedestal offset D/A converter for -10V to +10V output range. Connect to pin 19.
22	$-10V_{REF}$ OUT	-10V precision reference output.
23	-F.S. REF (ALL BITS OFF)	Minus Full Scale input to analog switch of error measurement circuit. Connect to pins 7, 8, 33, 34 for unipolar. Connect to pin 22 for bipolar.
24	BIPOLAR GAIN	Gain trim input connection to the pedestal offset D/A converter for bipolar operation. Connect to pin 25.

25	$+10V_{REF}$ IN	Connection to provide precision +10V reference to the D A converter circuits. Connect to pin 26.
26	$+10V_{REF}$ OUT	+10V precision reference output.
27	ADC VOLTAGE IN (TEST)	The analog output of the difference amplifier in the error measurement circuit.
28	UNIPOLAR GAIN	Connection to scale the output amplifier for unipolar output range (0 to +10V) and to provide a sense input from the load.
29	BIPOLAR OFFSET	Connects the bipolar offset current source to the current output of the main D A converter to provide bipolar offset. Connect to pins 7, 8, 33, 34 for unipolar. Connect to pin 12 for bipolar.
30	DAC VOLTAGE OUTPUT	Analog voltage output of the main D A converter.
31	+F.S. REF (ALL BITS ON)	Plus Full Scale input to analog switches of the error measurement circuit. Connect to pin 25.
32	CRM TRIM	Common-mode rejection trim for the output amplifier for bipolar operation only. Connect to pins 7, 8, 33, 34 for unipolar. Connect to pin 12 for bipolar.
33, 34	RTN	Analog return for the analog output. Also connected internally to pins 7 and 8.
35, 36	ANALOG COMMON	Return for ±15V supplies. Connected internally to pins 5 and 6.
37	$+15V_{IN}$	+15V supply input. Connected internally to pin 4.
38	$-15V_{IN}$	-15V supply input. Connected internally to pin 3.
39	+12V TEST	Test pin for internal +12VDC.
40	-12V TEST	Test pin for internal -12VDC.

INSTALLATION

The three connectors described in the previous section have three separate functions; analog interface, digital interface, and the terminal interface. The terminal interface is used only for factory test. Connection to a printed circuit board can be made using female printed-circuit-mounted connectors supplied with the DAC74. They should be positioned relative to the four internally-threaded mounting holes at the corners of the DAC74 as shown in Figure 4. Mount the DAC74 with four #6 external tooth lockwashers and four #6-32 screws using 0.156" diameter holes. Be sure to leave clearance for screwdriver adjustment of the trim potentiometers.

Alternatively, the DAC74 can be mounted on a chassis with the connectors facing upward using two #6 lockwashers and two #6-32 screws by means of the two internally-threaded holes near the center of the DAC74 as shown in Figure 4. In this orientation, connection to ribbon cable can be made with mass terminated, female, flat cable connectors (3M, 3421-0000, 3414-0000, 3417-0000). Individual wires may also be connected to the DAC74 in this orientation using female wire-applied connectors (AMP 1-87456-6, 3-87456-0, 3-87456-6 housings plus appropriate crimp snap-in pins). In either case, the jumpers for the unipolar or the bipolar configuration should be made right at the analog connector P2 as described in the following paragraph. The potential drops due to long jumpers cause a degradation in the accuracy of the calibration circuit.

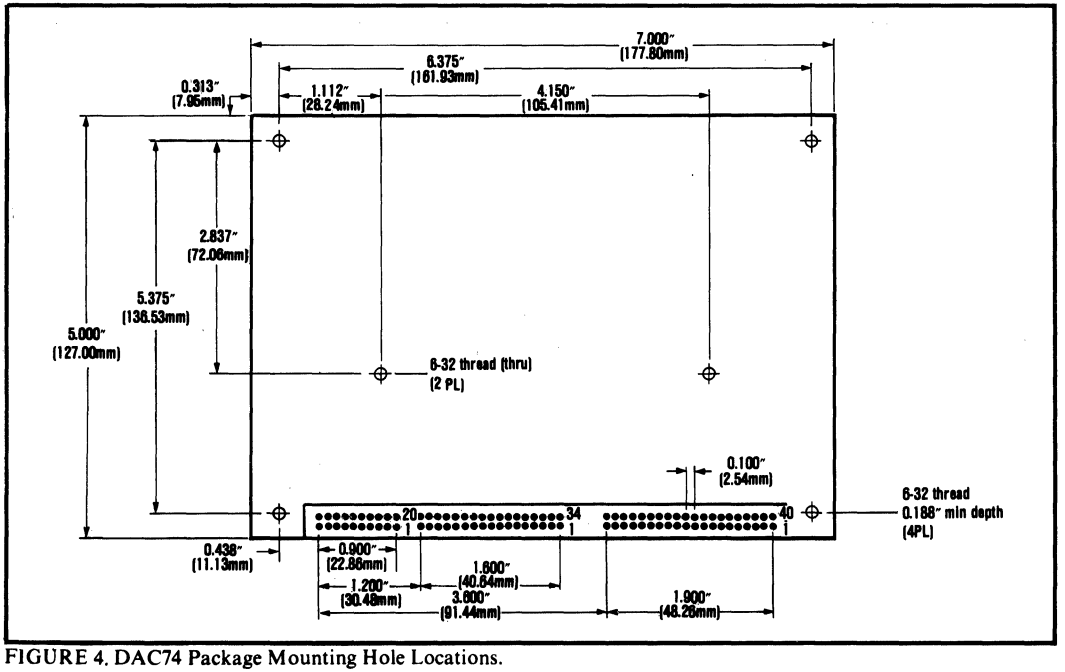


FIGURE 4. DAC74 Package Mounting Hole Locations.

POWER SUPPLY CONNECTIONS

A typical configuration is shown in Figure 5. Regardless of the local grounding, bring two separate return lines from the common near the power supplies to the DAC74. Connect one to Digital Common and the other to Analog Common. The load return line should be connected only to RTN (pins 7, 8, 33, 34) on P3 as shown in the unipolar and bipolar Connection Diagrams. Other connections to local grounds should be made with caution as they may cause ground loops which induce undesirable voltages at the common return points. The case is tied internally to Analog Common. Normally it should not be connected to any local grounds. Besides the power supply connections, other connections to the DAC74 should be limited to the digital inputs with a single digital current return and the 5-wire connection to the load. The external connections should be made so as to minimize the conduction paths to external noise sources. Internal bypass capacitors are included in the DAC74; no other bypass is needed nor recommended.

The power supply voltages may be sequenced on or off in any order provided that the power supply inputs have no transient voltages of polarity opposite to the normal DC input with respect to Analog or Digital Common.

The power supply requirements are listed below. During power-up, an initial surge of 400mA is required by the +15V supply input.

Input Voltage	+5V	+15V	-15V
Current, max	800mA	200mA	200mA
typ	500mA	150mA	150mA

Precautions

1. Provide all three grounds before applying voltage to either the power supply inputs or the signal inputs.
2. Avoid static discharge during handling and installation. Store the DAC74 in a conductive package.
3. Use short pairs of wire close together to minimize electromagnetic pickup.

In very noisy environments, separate floating supplies may be needed to power the DAC74. These supplies and their common returns should be connected only to the DAC74. Some experimentation with extra shielding and alternative return configurations may be necessary in extreme circumstances.

OUTPUT CONNECTION

The output connection for unipolar and bipolar operation are shown in the Connection Diagrams. For either unipolar or bipolar, it is very important to provide both a current-carrying wire and a sense wire to both sides of the load in order to minimize the errors caused by induced potentials and losses in the wiring to the load. The fifth wire, CAL SENSE, returns the output voltage at the load to the error measurement circuit. In a noisy environment these wires should be enclosed in a shield that is connected only to the RTN pins of the DAC74. The return line from the load to the RTN pin of the DAC74 must be separate from other grounds in order to avoid potential drops due to shared current paths. The resistance of this path must be low so that the voltage drop is less than 20μV. For example, at 5mA one foot of 16-guage copper wire (4Ω/1000ft.) produces a 20μV drop.

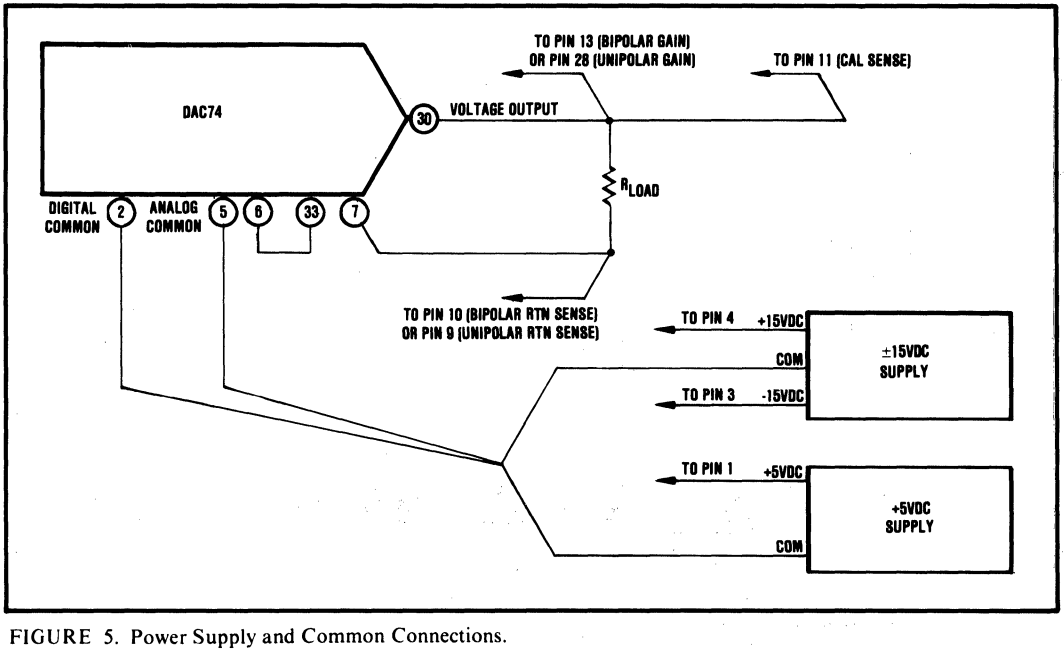


FIGURE 5. Power Supply and Common Connections.

Unipolar Connection. The output connections and jumpers are listed below. The pin numbers refer to the analog connector P3. The first five connections constitute the 5-wire connection to the load.

Connection	Purpose
30 to load (top)	DAC VOLTAGE OUTPUT Output connection to the load.
28 to load (top)	UNIPOLAR GAIN Output sense to the inverting input of the output amplifier. Sets unipolar range.
7 to load (bottom)	RTN Current return from the load. This return impedance must be low - equivalent of 16-gauge wire.
9 to load (bottom)	UNIPOLAR RETURN SENSE Return sense to the noninverting input of the output amplifier.
11 to load (top)	CAL SENSE Input to the error measurement circuit from the load.
33 to 6	RTN TO ANALOG COMMON Connect common returns. This jumper is essential to prevent damage to the internal reference.
23 to 34	-F.S. REF (ALL BITS OFF) Set minus full scale to 0 volts. Keep as short as possible.
29 to 34	BIPOLAR OFFSET TO RTN Maintain the same current drain on the +10 volt reference as bipolar connection.
26 to 25	+10V REF OUT TO +10V REF IN Keep as short as possible.
15 to 16	UNIPOLAR OFFSET TRIM TO OFFSET TRIM Connect offset trim to offset adjust input of the pedestal offset D/A converter.
17 to 25	UNIPOLAR GAIN TRIM (OFFSET DAC) to +10 VOLT REF Connect the full scale gain reference of pedestal offset D/A converter.
19 to 20	VOLTAGE OUT (OFFSET DAC) output to UNIPOLAR GAIN (OFFSET DAC) Return sense to inverting input of the pedestal offset D/A converter.
18 to digital common	UNIPOLAR CAL to DIGITAL COMMON Set software to unipolar mode.
31 to 25	+F.S. REF to +10V REF IN.

Bipolar Connection. The output connections and jumpers for bipolar operation are listed below. The pin numbers refer to the analog connector P3. The first five connections constitute the 5-wire connection to the load.

Connection	Purpose
30 to load (top)	DAC VOLTAGE OUTPUT Output connection to the load.
13 to load (top)	BIPOLAR GAIN Sense to the inverting input of the output amplifier. Sets bipolar range.
7 to load (bottom)	RTN Current return from the load. This return impedance must be low - equivalent of 1 foot 16-guage wire for 5mA output.
10 to load (bottom)	BIPOLAR RETURN SENSE Return sense to the noninverting input of the output amplifier.
11 to load (top)	CAL SENSE Input to the error measuring circuit from the load.
32 to 7	CMR to RTN Match the equivalent impedance to RTN for both inputs of output amplifier for the bipolar configuration.
7, 8, 33, 34	RTN Tied together internally.
33 to 6	RTN to ANALOG COMMON Connect common returns. This jumper is essential to prevent damage to the internal references

Connection	Purpose
23 to 22	-F.S. REF (ALL BITS OFF) to -10V REF OUT Set minus Full Scale to -10 volts. Keep as short as possible.
29 to 12	BIPOLAR OFFSET to CURRENT OUTPUT Bipolar offset for output amplifier.
26 to 25	+10V REF OUT to +10V REF IN Keep as short as possible.
16 to 25	OFFSET TRIM (OFFSET DAC) to +10V REFERENCE IN Connect bipolar offset of the pedestal offset D/A converter to +10V REF.
24 to 25	BIPOLAR GAIN TRIM (OFFSET DAC) to +10V REF Connect the Full Scale gain reference of the pedestal offset D/A converter.
19 to 21	VOLTAGE OUTPUT (OFFSET DAC) to BIPOLAR GAIN (OFFSET DAC) Return sense to inverting input of the pedestal offset D/A converter.
31 to 25	+F.S. REF to +10V REF IN.

Internally Connected Pins. The following pins are connected internally:

Function	Pin No.
DIGITAL COMMON	2, 12, 16, 17, 18, 19, 33
$+5V_{IN}$	1, 34
ANALOG COMMON	5, 6, 35, 36
$+15V_{IN}$	4, 37
$-15V_{IN}$	3, 38
RTN	7, 8, 33, 34

DIGITAL INPUTS

Data inputs D0 - D15 and enable inputs, ENMSB and ENLSB, are low power Schottky (74LS373). Control inputs $\overline{RES}$, RUN/$\overline{CAL}$ and $\overline{UNIPOLAR\ CAL}$ are standard TTL inputs. MPUOFF is a standard TTL input with a 10kΩ pullup resistor connected to +5V volts.

Timing specifications on the digital inputs are listed in the Specifications table and discussed in the Operation section.

OPERATION

DAC74 data inputs, control signals, and status lines are shown in Figure 6. MPUOFF will usually be tied to DIGITAL COMMON permitting the internal crystal ocsillator to run continuously. However, one may wish to control the oscillator to remove all possible sources of noise during D/A converter operation. MPUOFF must be asserted low 50msec before the $\overline{RES}$ pulse is asserted.

The $\overline{RES}$ line resets the calibration controller and starts controller operation when it returns high after being asserted low for at least 14μsec.

RUN/$\overline{CAL}$ is a mode control line. When high, RUN/$\overline{CAL}$ enables the controller to set up the SERVICE mode. In this mode, the user performs a coarse manual adjustment of the D/A converter. When RUN/$\overline{CAL}$ is low, the controller is informed to set up the SELF-CALIBRATION mode, the normal mode of operation.

Data input latches are level-triggered by ENSMB and ENLSB. These are used to strobe-in data from an 8-bit bus with D0 through D7 connected to D8 through D15 respectively. For 16-bit bus operation ENLSB can be permanently connected to +5V. Since all three latches are octal transparent latches (74LS373), their inputs may be transferred directly to their outputs by setting their respective enable inputs high. The table below indicates four common interfaces. A high input refers to a logic 1 input (2V to 3.5V) and a low input refers to a logic 0 input (0V to 0.8V).

Mode	ENMSB	ENLSB	Description
Transparent	High	High	Inputs are transferred directly to the MAIN D/A converter.
16-bit interface	Positive Pulse	High	All 16 bits are latched at the end of the ENMSB pulse.
8-bit interface	Low	Positive Pulse	Capture 8LSB's from the data bus in low byte buffer.
8-bit interface	Positive Pulse		Transfer 8MSB's from the data bus and transfer latched 8LSB's to the MAIN D/A converer at the end of the pulse.

The three-state output in the second rank of latches is disabled by $\overline{RUN}$, a status output signal, during the time the calibration controller has control of the main D/A converter.

INITIAL SETUP

It is necessary to trim the +10V and -10V reference as close to 10V as possible using the potentiometers located at the edge of the module. The procedure is described in Manual Calibration section.

It should not be necessary to manually adjust OFFSET, GAIN, and LINEARITY on units received from the factory. However, after a year or more of operation it may be necessary to adjust these parameters to within the range which can be trimmed by the self-calibration circuits. The manual adjustment procedure is described in the Manual Calibration section. It is important that either the load be connected or that a dummy load be switched in during calibration or adjustment.

Self-Calibration Mode

After power-up, a 1/2-hour warm-up period must be allowed. This permits the heated zener reference and other critical circuits to stabilize.

The next step is to initiate the SELF-CALIBRATION routine. Self-calibration is initiated by providing a pulse (low, 14μsec min) from the host equipment to the $\overline{\text{RES}}$ line. Self-calibration typically takes 2-1/2 seconds. $\overline{\text{CAL}}$ and $\overline{\text{RUN}}$ inform the user on the internal status of the calibration controller. The operation of these is best explained by a timing diagram, Figure 7.

Upon application of the reset pulse, $\overline{\text{CAL}}$ goes (or remains) low and goes high about 100μsec after $\overline{\text{RES}}$ is returned high. $\overline{\text{CAL}}$ remains high for 500μsec maximum. If it remains high, self-calibration has failed. If it goes low, self-calibration will be successful. The fact that calibration has failed means that either a noise transient has interferred with system operation or that the maximum correction factors have been used and that the main D/A converter connot be corrected to within specification. However, the converter will still operate. It will be necessary to perform manual adjustments described in the Manual Calibration section.

$\overline{\text{RUN}}$ goes high about 100μsec after the $\overline{\text{RES}}$ pulse returns high and remains high until all calibration controller operations are complete and control of the main D/A converter is returned to the digital data inputs. It is important to be aware of two facts during self-calibration: (1) the main D/A converter is being exercised, its output is moving and changing the voltage on the load; and (2) the three-state output enable of the main D/A converter input latches is held high by $\overline{\text{RUN}}$ thereby disconnecting the data inputs from the main D/A converter.

Service Mode

Before one can manually adjust the GAIN, OFFSET and LINEARITY of the DAC74, it must be put in a mode called the SERVICE mode. This is accomplished by switching RUN/$\overline{\text{CAL}}$ high and asserting a pulse on the $\overline{\text{RES}}$ line. The result of going into this mode is that all corrections in the RAM are set to zero before control is returned to the user data input lines.

The timing is illustrated in Figure 7. $\overline{\text{CAL}}$ does not return low as it did in the SELF-CALIBRATION mode but remains high. $\overline{\text{RUN}}$ returns low indicating that control has been returned to the data inputs. $\overline{\text{RUN}}$ time is about 300msec. Manual calibration may proceed as described in the Manual Calibration section.

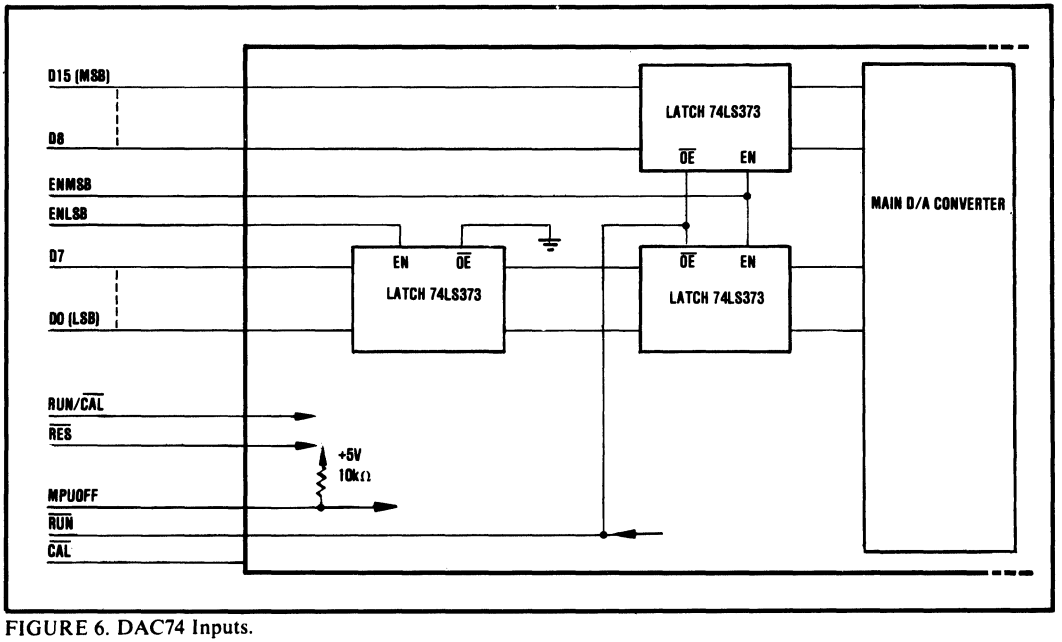


FIGURE 6. DAC74 Inputs.

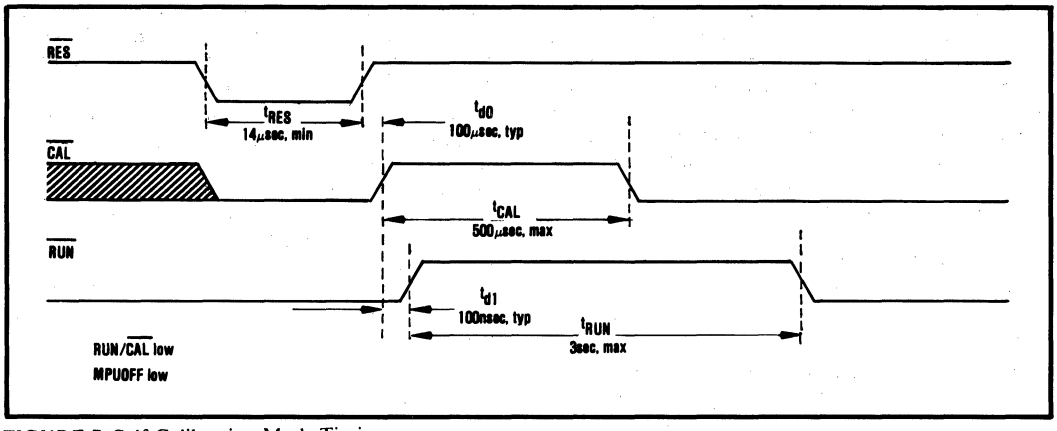


FIGURE 7. Self-Calibration Mode Timing.

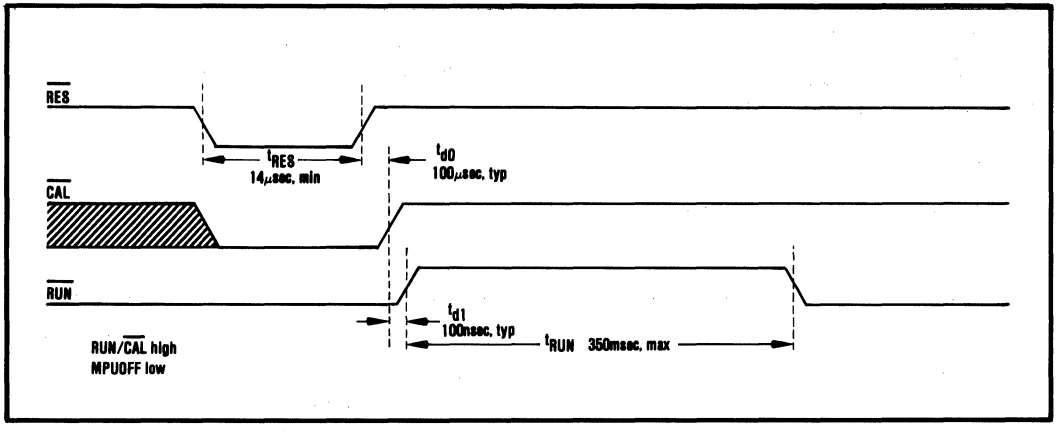


FIGURE 8. Service Mode Timing.

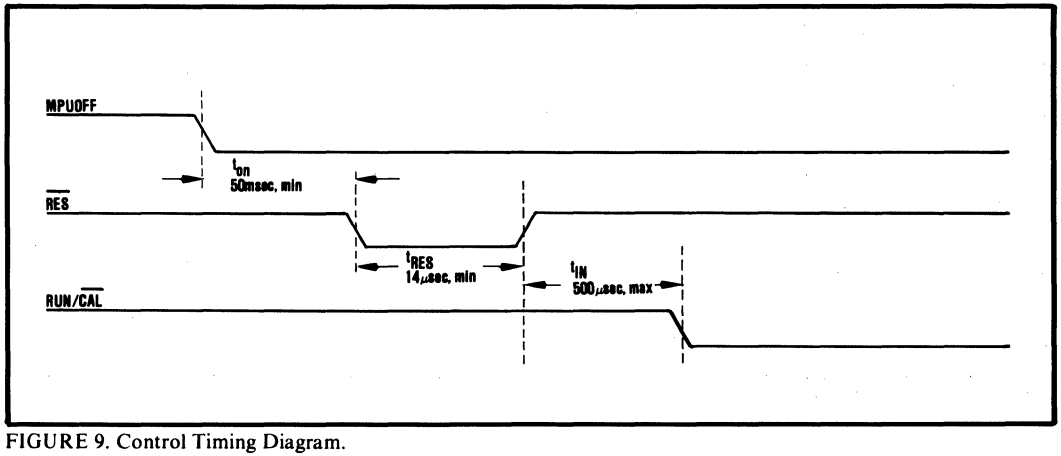


FIGURE 9. Control Timing Diagram.

Full Automatic Control

If the user wishes to automatically control the total operation of the DAC74 including the SERVICE mode as well as the SELF-CALIBRATION mode, additional timing considerations apply. An additional timing diagram is shown in Figure 8. Note that the MPUOFF must be asserted low 50msec before $\overline{RES}$ is asserted and the RUN/$\overline{CAL}$ must be asserted within 500μsec of the time that the $\overline{RES}$ pulse returns high.

MANUAL CALIBRATION

Manual adjustment of the DAC74 is accomplished by eight potentiometers located at one end of the package. Space for screwdriver access must be provided on the mounting surface. A label marked "REFER TO MANUAL BEFORE REMOVING LABEL" must be removed from the end of the package to access the potentiometers.

10V Reference Adjustment

After the DAC74 has been installed, the load connected, and a 1/2-hour warm-up period has elapsed, the references may be adjusted. The reference voltages should be set to 10V, ±10μV.

A 6-1/2 digit voltmeter, which has been calibrated as accurately as possible may be used to adjust the reference and coarse calibrate the D/A converter.

ADJUSTMENT PROCEDURE

1. Connect the voltmeter between the +10V REF OUT pin (26) and an ANALOG COMMON pin (5, 6, 35, 36). Adjust the +10V REF potentiometer to obtain a reading of 10.00000V, ±10μV.
2. Connect the voltmeter to the -10V REF OUT pin (22) and adjust the -10V REF potentiometer to read -10.00000V, ±10μV. Needed for bipolar only.

Note: If these reference voltages are to be used to provide references to other circuits, those loads must be connected before the above adjustments are made. External reference loads must remain constant for accurate operation of the DAC74.

Coarse Calibration of the Main D/A Converter.

The self-calibration controller can correct main D/A errors within a limited range. If the gain, offset or linearity shift due to initial installation environment, such as load return wire voltage drops, power supply voltage line regulation, or component aging, a manual coarse adjustment will be necessary. These six adjustments are made using potentiometers at the edge of the DAC74 package.

Coarse adjustments bring the errors of the DAC74 to within the operating range of the self-calibration circuit. It is sufficient to adjust the DAC74 output to within norminal values.

ADJUSTMENT PROCEDURE

After the DAC74 had been installed, the load connected, a 1/2-hour warm-up period has elapsed, and the reference voltages have been set, manual calibration may proceed. Put the DAC74 into the SERVICE mode as described in the Service Mode section.

Adjustments will be made in the following order: OFFSET, preliminary GAIN, 4MSB's (LINEARITY), and final GAIN. Output voltage readings will be different for bipolar and unipolar configurations. Table I shows the data word to be strobed into DAC74, the potentiometer to be adjusted, and the output reading to be attained for unipolar and bipolar configurations.

After these adjustments are made, put the DAC74 in the SELF-CALIBRATION mode as described in the Self-Calibration Mode section. The DAC74 is now ready for normal operation.

TABLE I. Calibration Voltages.

Step	Data Input Word (hex)	Adjust Poteniometer	D/A Output Reading	
			Unipolar	Bipolar
1	0000	OFFSET	0.0000V,±50μV	-10.0000V,±100μV
2	0800	GAIN	0.3125V,±50μV	-9.3750V,±100μV
3	1000	D12	0.6250V,±50μV	-8.7500V,±100μV
4	2000	D13	1.2500V,±50μV	-7.5000V,±100μV
5	4000	D14	2.5000V,±50μV	-5.0000V,±100μV
6	8000	D15	5.0000V,±50μV	0.0000V,±100μV
7	FFFF	GAIN	9.99985V,±50μV	-9.9997V,±100μV

OPERATIONAL CHECKLIST

1. Be sure that all pins and jumpers are connected properly as discussed and illustrated in the Installation section. Careful layout and shielding is necessary to keep digital noise out of the analog circuits.
2. The load return line from the load to RTN (pin 7, P3) must have less than 20μV voltage drop across its length for proper operation. See Installation section.
3. Be sure and wait about 1/2-hour for warm-up.
4. Check power supply voltages at the module pins.
   +15V and -15V, ±0.5V
   +5V, ±0.25V
5. Check +12V and -12V voltages generated internally.
   +12V, ±0.6V pin 39, P3
   -12V, ±0.6V pin 40, P3
6. Check +10V and -10V references. The D/A converter accuracy is directly dependent on these voltages. See Adjustment Procedure in the Manual Calibration section.
   +10.00000V, ±10μV pin 26, P3
   -10.00000V, ±10μV pin 22, P3
7. Check MPUOFF (pin 14, P3) to be sure it is low. It must be low for at least 50msec before attempting self-calibration.
8. Be sure $\overline{UNIPOLAR\ CAL}$ (pin 18, P3) is high for bipolar operation or low for unipolar operation.
9. $\overline{RES}$ pulse must be at least 14μsec wide.
10. If $\overline{CAL}$ status does not return low during an automatic self-calibration, the D/A converter may be out of tolerance. Adjust it using the procedure in the Manual Calibration section. An unsuccessful self-calibration can result from a voltage or current transient in the D/A converter system. Attempt a second self-calibration.

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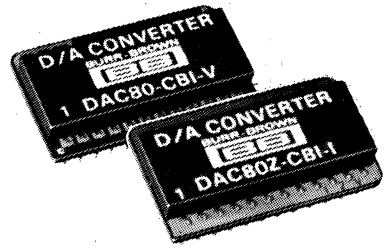


DAC80

IC DIGITAL-TO-ANALOG CONVERTER

FEATURES

- WIDE POWER SUPPLY RANGE MODELS AVAILABLE (Z MODELS)
- 12-BIT, 3 DIGIT RESOLUTION
- ±½LSB MAXIMUM NONLINEARITY
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT AMPLIFIER (V MODELS)
- FAST SETTLING - 300nsec to ±.01% (I MODELS)
- CERAMIC DUAL-IN-LINE PACKAGE
- LOW COST

DESCRIPTION

Use this popular 12 bit digital-to-analog converter for low cost precision performance applications.

DAC80, with internal reference and optional output amplifier, offers a maximum nonlinearity error of ±0.012%, ±30ppm/°C maximum gain drift, and monotonicity - all over a 0 to 70°C operating range. In the bipolar configuration, total accuracy drift is guaranteed to be less than ±25ppm/°C. Select TTL compatible complementary 12 bit binary (CBI) or 3 digit BCD (CCD) input codes.

Packaged within DAC80's 24 pin dual-in-line ceramic case are fast settling switches and stable, laser trimmed thin-film resistors that let you select output voltage ranges of ±2.5, ±5, ±10, 0 to +5, 0 to +10 volts (V models) or output current ranges of ±1mA or 0 to -2mA (I models). Voltage output models settle to ±0.01% of FSR in 3 microseconds for a 10 volt step change.

By specifying the new DAC80Z model with a supply range of ±11.4 to ±16.0 volts, you can use this proven D/A converter in microprocessor and semiconductor memory systems.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-322E

Printed in U.S.A. July, 1978

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC80-CBI			DAC80-CCD			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUT							
Resolution			12				Bits
						3	Digits
Logic Levels (TTL/Compatible)[1]							
Logic "1" (at +40μA)[2]	+2		+5.5	+2		+5.5	VDC
Logic "0" (at -1.0mA)[3]	0		+0.8	0		+0.8	VDC
ACCURACY							
Linearity Error at 25°C		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	+1, -3/4		±1/4	±1/2	LSB
Gain Error[4]		±0.1	±0.3		±0.1	±0.3	%
Offset Error[4]		±0.05	±0.15		±0.05	±0.15	% of FSR[5]
Monotonicity Temp. Range, min	0		+70	0		+70	°C
DRIFT[6] (0°C to +70°C)							
Total bipolar drift, max (includes gain, offset, and linearity drifts)[7]			±25			±25	ppm of FSR/°C
Total error over 0°C to +70°C[8]							
Unipolar		±0.08	±0.15		±0.08	±0.15	% of FSR
Bipolar		±0.06	±0.12		±0.06	±0.12	% of FSR
Gain		±15	±30		±15	±30	ppm/°C
Exclusive of internal reference			±10			±10	ppm/°C
Unipolar Offset		±1	±3		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, -7/8		±1/2	+1, -7/8	LSB
Linearity Error 0°C to +70°C			±1/2			±1/2	LSB
CONVERSION SPEED/V models							
Settling Time to ±0.01% of FSR For FSR Change							
with 10kΩ Feedback[9]		5			5		μsec
with 5kΩ Feedback		3			3		μsec
For 1 LSB Change		1.5			1.5		μsec
Slew Rate	10	20		10	20		V/μsec
CONVERSION SPEED/I models - of FSR							
Settling Time to ±0.01% For FSR Change							
10 to 100Ω Load		300			300		nsec
1kΩ Load		1			1		μsec
ANALOG OUTPUT/V models							
Ranges[6]	±2.5, ±5, ±10, 0 to +5, 0 to +10				0 to +10		Volts
Output Current	±5			±5			mA
Output Impedance (DC)		0.05			0.05		ohms
Short Circuit Duration	Indefinite to Common						
ANALOG OUTPUT/I models							
Ranges		±1, 0 to -2			0 to -2		mA
Output Impedance - Bipolar		4.4			4.4		kΩ
Output Impedance - Unipolar		15			15		kΩ
Compliance			±2.5			±2.5	Volts
INTERNAL REFERENCE VOLTAGE		+6.3			+6.3		Volts
Maximum External Current[10]			±200			±200	μA
Tempco of Drift, max		±10	±20		±10	±20	ppm/°C
POWER SUPPLY SENSITIVITY							
+15V Supply		±0.02			±0.02		% of FSR/% V_S
-15 and +5V Supplies		±0.002			±0.002		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS							
DAC80	±14, +4.75	±15, +5	±16, +16	±14, +4.75	±15, +5	±16, +16	VDC
DAC80Z[6]	±11.4, +4.75	±12, +5	±16, +16	±11.4, +4.75	±12, +5	±16, +16	VDC
Supply Drain							
±15/±12V (including 5mA load)		±25	±35		±25	±35	mA
+5V (logic supply)		+20	±30		+20	±30	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (double above specs)	-25		+85	-25		+85	°C
Storage	-55		+100	-55		+100	°C

TABLE I. Electrical Specifications

NOTES:

1. Adding external CMOS hex buffers CD 4009A will provide CMOS input compatibility.
2. Logic "1" current = 40μA max at V_{IN} = +5.0V
3. Logic "0" current = -1.6mA max at V_{IN} = +0.4V.
4. Adjustable to zero with external trim potentiometer.
5. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
6. To maintain drift spec internal feedback resistors must be used for current output models.
7. See discussion on page 6-161.
8. With gain and offset errors adjusted to zero at 25°C. See discussion on page 6-162
9. DAC80Z supply range is ±12.0V min to ±16.0V max for 0 to +10V and ±10V.
10. Maximum with no degradation of specifications.

CONNECTION DIAGRAM

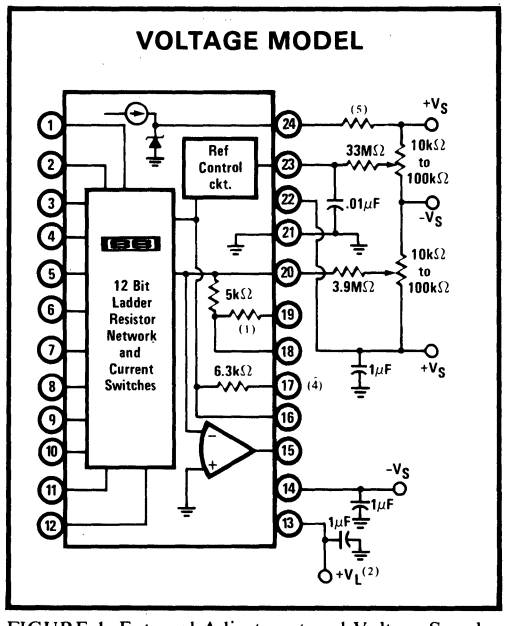


FIGURE 1. External Adjustment and Voltage Supply Connection Diagram, Voltage Model.

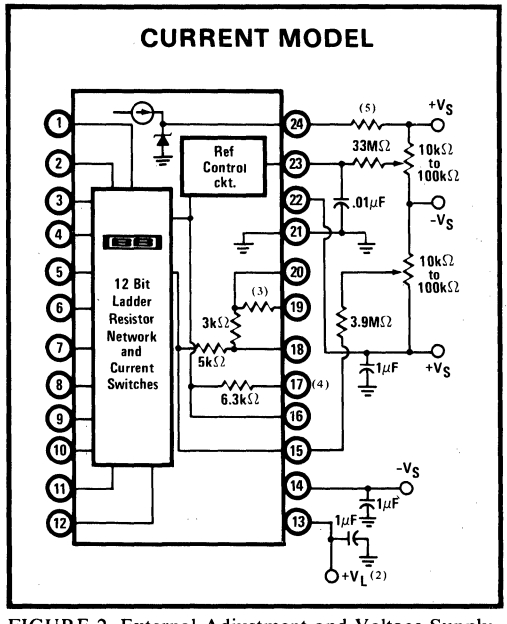


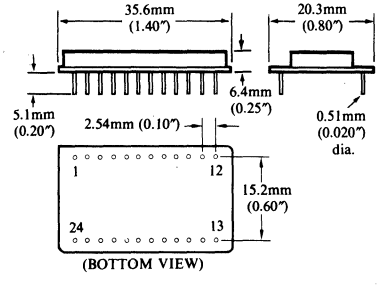
FIGURE 2. External Adjustment and Voltage Supply Connection Diagram, Current Model.

NOTES:
1. 3kΩ for CCD models, 5kΩ for CBI models.
2. If connected to $+V_S$, which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model,OΩ and pin 20 has no internal connection.
4. 6.3kΩ resistor internally grounded on CCD models.
5. Resistor required only for Z models, see page 6-156. Make no connection to power supply for regular models.

PIN ASSIGNMENTS

I Models	Pin #	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
Logic Supply	13	Logic Supply
$-V_S$	14	$-V_S$
I_{OUT}	15	V_{OUT}
Ref. Input	16	Ref. Input
Bipolar Offset	17	Bipolar Offset
Scaling Network	18	10V Range
Scaling Network	19	20V Range
Scaling Network	20	Summing Junction
Common	21	Common
$+V_S$	22	$+V_S$
Gain Adjust	23	Gain Adjust
6.3V Ref. Out	24	6.3V Ref. Out

MECHANICAL



CASE: Black Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of Mil-Std-883 (gross leak).

FIGURE 3. Mechanical Specifications

DISCUSSION

DIGITAL INPUT CODES

The DAC80 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, CTC or COB.

	DIGITAL INPUT	ANALOG OUTPUT		
	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+1/2 Full Scale	Zero	-Full Scale
	100000000000	Mid-scale -1LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE II. Digital Input Codes

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2 LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0 to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0 to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the specification table both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in OFFSET is referenced to the OFFSET at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0111 ... 11 to 1000 ... 00), the point at which the worst case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage range of ±1V and 0 to -2V. See Table V.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC80 is ±5V.

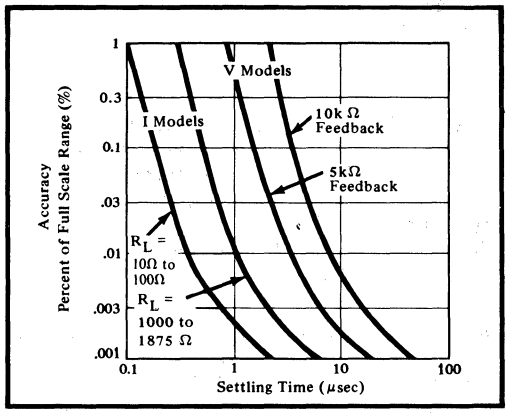


FIGURE 4. Full Scale Range Settling Time vs Accuracy

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive, negative, or logic supplies about the nominal power supply voltages. See Figure 5.

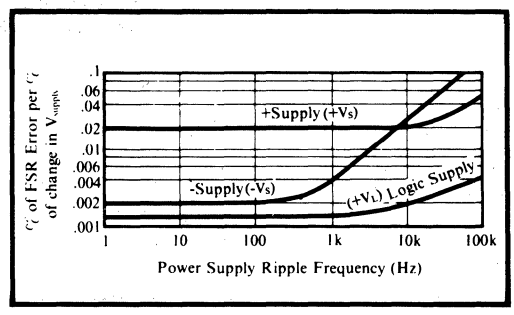


FIGURE 5. Power Supply Rejection vs Power Supply Ripple

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) has a tolerance of ±5% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 200μA. An external buffer amplifier is recommended if this reference will be used to drive other system components.

OPERATING INSTRUCTIONS

±12 VOLT SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. For operation with supplies less than ±14V an external resistor must be connected between the positive supply and pin 24. This provides additional current required by the internal reference. The required resistor value for supply voltages of ±11.4 to ±12.6V is 2.0kΩ and for supplies of ±12.6 to ±14V is 3.9kΩ.

It is recommended that output voltage ranges -10 to +10V and 0 to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{supply}| - |V_{out}\ max| <$ 2.0V. This applies to units with both CBI and CCD input codes. Except for operation at lower supply voltages, the DAC80Z and DAC80 operation is identical.

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the connection diagrams, Figures 1 and 2. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. If gain and offset adjust circuits are not used, pins 15, 20 and 23 should be connected as described in other sections herein. (Do not ground.) Connect the potentiometers as shown in Figure 1 and Figure 2 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 33MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pick-up. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a .001μF to .01μF ceramic capacitor should be connected from this pin to common to prevent noise pick-up. Refer to Figure 7 and 8 for relationship of OFFSET and GAIN adjustments to unipolar and bipolar D/A converters.

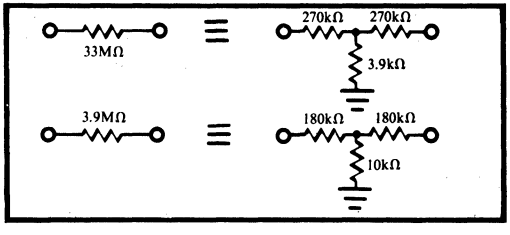


FIGURE 6. Equivalent Resistances.

Offset Adjustment: For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table III for corresponding codes and the block diagram on page 6-154 for offset adjustment connections.

Gain Adjustment: for either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table III for positive full scale voltages and the block diagrams for gain adjustment connections.

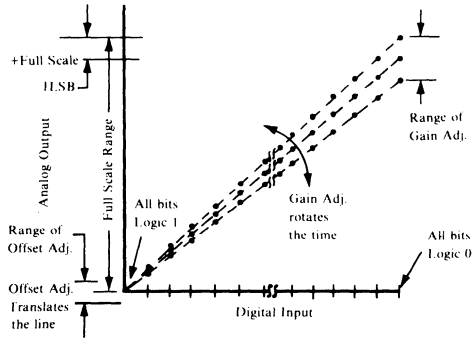


FIGURE 7. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

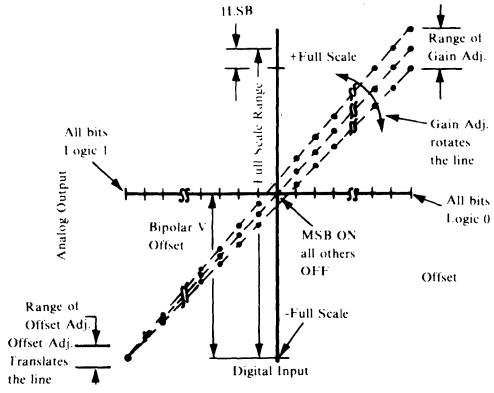


FIGURE 8. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter

	DIGITAL INPUT	ANALOG OUTPUT			
		VOLTAGE*		CURRENT	
		0 to +10V	±10V	0 to -2mA	±1mA
CBI Models	12 Bit Resolution MSB LSB				
	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
	One LSB	2.44mV	4.88mV	0.488μA	0.488μA
CCD Models	3 Digital Resolution MSB LSB				
	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	One LSB	10.00mV	N/A	1.25μA	N/A

** Normal full scale range with correct codes; output can go higher if illegal codes are applied.
* To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE III. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10*, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V.* See Figure 9.

*Refer to ±12V supply operation discussion, page 6-156.

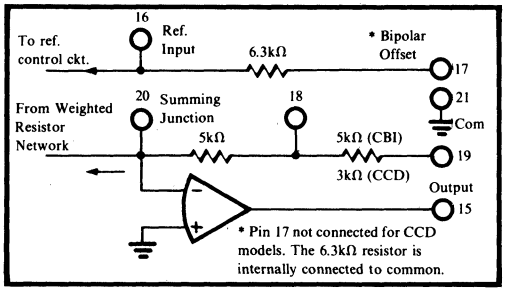


FIGURE 9. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized in the DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table IV. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

TABLE IV. Output Voltage Range Connections - Voltage Model DAC80.

CURRENT OUTPUT MODELS

The equivalent output circuit and resistive scaling network of the current model differ from the voltage model and are shown in Figures 10 and 11. Instructions for using the DAC80-XXX-I with a resistor or an external op amp follow. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100 ppm/°C or less to maintain the DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25 ppm/°C or less to minimize drift. This will typically add ±50 ppm/°C + the TCR of R_L (or R_F) to the total drift.

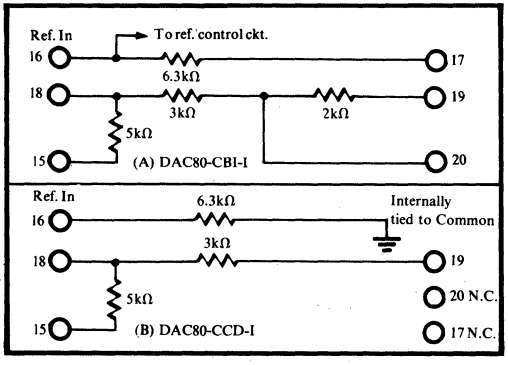


FIGURE 10. Internal Scaling Resistors

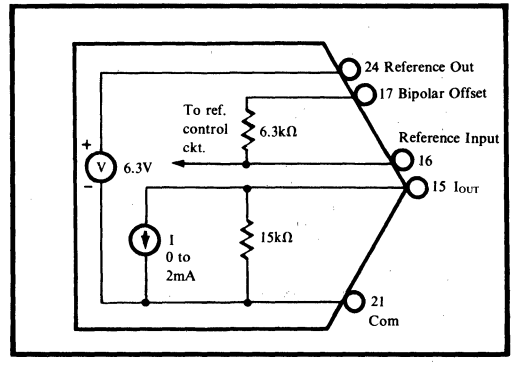


FIGURE 11. DAC80 Current Model Equivalent Output Circuit.

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	R_{LP}	R_{LI} Connections Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Reference Connect Pin 16 to	Bipolar Offset Connect Pin 17 to	R_{LS}	R_{LP}
CSB	0 to -2V	0.968kΩ	105Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	1.875kΩ	N/A	36.5kΩ	19	Com (21)	N.C.	24	N.C.	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	90.9Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

TABLE V. DAC80-XXX-I Resistive Load Connections.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 12 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{15k \times R_L}{15k + R_L}\right)$$

Where R_L max = 1.36kΩ
and V_{OUT} max = -2.5V

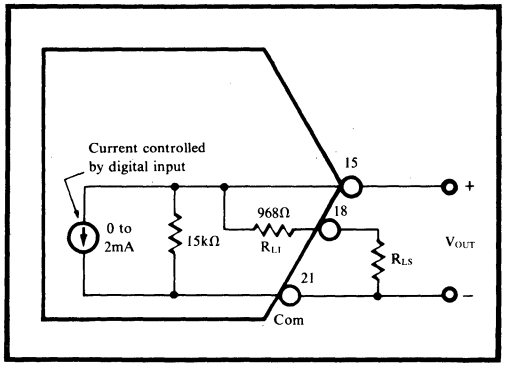


FIGURE 12. Equivalent Circuit DAC80-CBI-I connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table V to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With $R_{LS} = 0$, $V_{OUT} = -1.82V$.

CCD Input Code: Connect the internal scaling resistors as shown in Table V and add an external metal film resistor (R_{LP}) in parallel as shown in Figure 13 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes.

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}},$$

$$V_{OUT} = -1.25mA \left(\frac{15.6k \times R_L}{15.6k + R_L}\right)$$

If $R_{LP} = \infty$, $V_{OUT} = -2.08V$

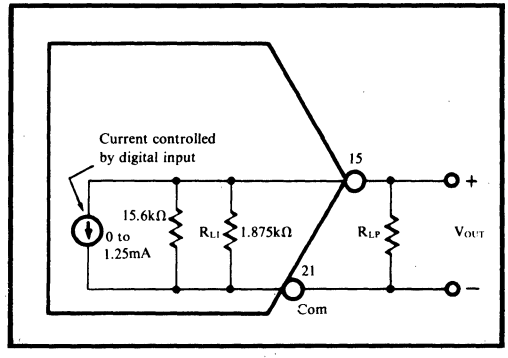


FIGURE 13. DAC80-CCD-I Connected for Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 14, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 4.44k}{R_L + 4.44k}\right)$$

Where R_L max = 5.72kΩ
V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table V for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V.

With $R_{LS} = 0$, $V_{OUT} = \pm 0.944V$.

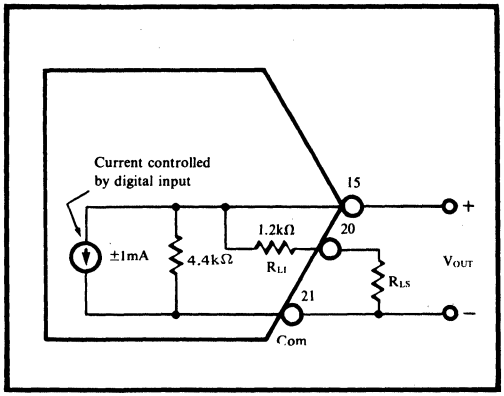


FIGURE 14. DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load.

DRIVING AN EXTERNAL OP AMP

The current model DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 15.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table VI.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Conect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	Ⓐ	24

TABLE VI. Voltage Range of Current Output DAC80.

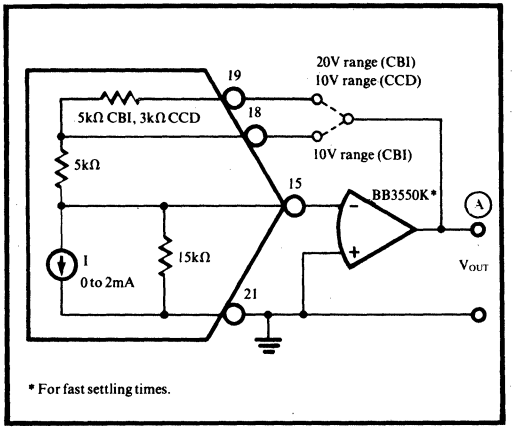


FIGURE 15. External Op Amp - Using Internal Feedback Resistors.

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges. See Figure 16. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

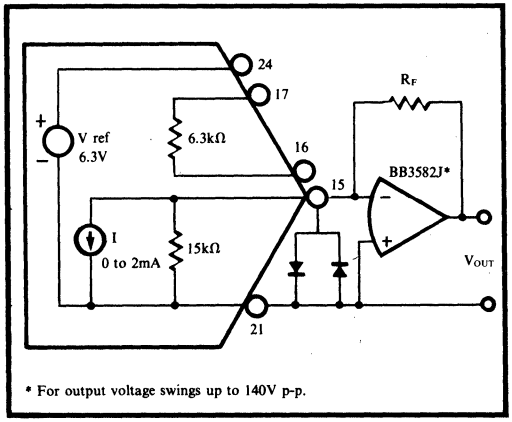


FIGURE 16. External Op Amp - Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC80 consists of three primary components: Gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the worst case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst case accuracy drift for a DAC80 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately. Note that the linearity drift of both modes is negligible. (Total linearity error is less than ±1/2 LSB over 0°C to +70°C.)

In the unipolar mode of operation, offset drift (±1 ppm/°C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±10 ppm/°C due to ratio drift of current weighting resistors to the reference resistor and current switch V_{BE} to the reference transistor (refer to Model 4550 data sheet); and 2) ±20 ppm/°C due to the zener reference. The sum of these two components, ±30 ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst case accuracy drift in the unipolar mode is simply the sum of the components, or ±31 ppm/°C.

In the bipolar mode the major portion (67%) of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 17 shows a simplified circuit diagram of a DAC80 operating in the bipolar mode with all bits off. The current switch leakage current is negligible, so

$$V_{-FULL\ SCALE} = -\frac{RF}{R_{BPO}} \cdot V_{REF}$$

$$= -\frac{10k}{6.3k} \cdot 6.3V = -10 \text{ volts}$$

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is

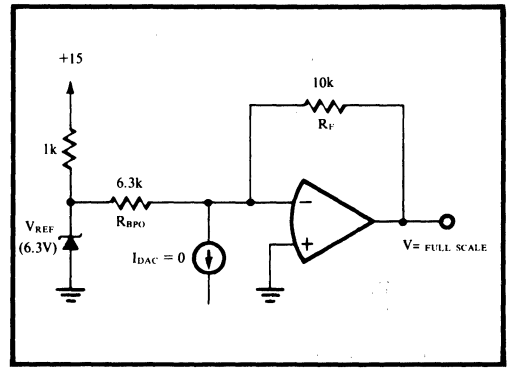


FIGURE 17. Simplified Diagram of DAC80 with "All Bits Off" Operating in Bipolar ±10V Range.

+20 ppm/°C, this is equivalent to (+20 ppm/°C) x (+6.3V) = +126μV/°C. This will result in a voltage drift at the amplifier output of

$$\frac{\Delta V_{-FS}}{\Delta T} = -\frac{R_F}{R_{BPO}} \cdot \frac{\Delta V_{REF}}{\Delta T}$$

$$= -\frac{10k}{6.3k} \cdot 126\mu V/^{o}C = -200\mu V/^{o}C.$$

Since the DAC80 is operating in the ±10V range this is equivalent to (-200μV/°C) ÷ (20V range) = -10 ppm of FSR/°C.

Now consider the effect of reference changes on gain drift. When all of the bits are turned on it can be shown that:

$$\frac{\Delta V_{+FULL\ SCALE}}{\Delta T} = +\frac{R_F}{R_{BPO}} \cdot \frac{V_{REF}}{\Delta T}$$

$$= +\frac{10k}{6.3k} \cdot 126\mu V/^{o}C = +200\mu V/^{o}C$$

$$\text{and } \frac{+200\mu V/^{o}C}{20V \text{ Range}} = +10 \text{ppm}/^{o}C \text{ of FSR.}$$

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the opposite direction of, the drift of the plus full scale voltage and that

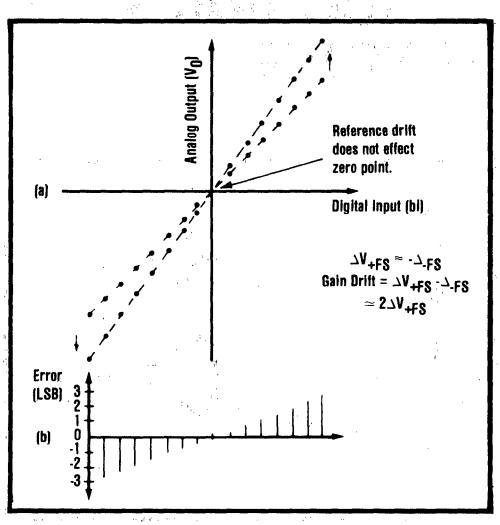


FIGURE 18. (a) Effect of a Positive Reference Drift on the Ideal D/A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC80.

zener reference variations have virtually no effect on the zero point. (See Figure 18) This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm/°C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

Using this relationship, the worst case accuracy drift for a bipolar DAC80 can be computed. The maximum TCR of the zener reference is ±20ppm/°C. The gain drift due to the reference then is also ±20ppm/°C. The full scale drift and bipolar offset drift are each half that amount or ±10ppm/°C. The maximum gain and offset drifts of the DAC80, exclusive of the reference, are ±10 and ±5ppm/°C respectively. Adding this to the full scale drift due to the reference gives a worst case total accuracy drift of ±25ppm/°C. (Random drifts, which these are, can be in the same direction, so they add directly.) This is much less that the total drift obtained by simply adding the maximum gain and bipolar offset drifts (±45ppm/°C). The maximum zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±10ppm of FSR/°C.

The DAC80 is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

total worst case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.01% + ±25ppm/°C (45°C) (100)
= ±0.12%;

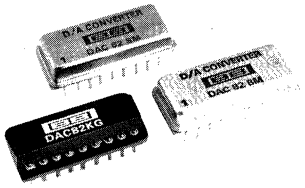
total worst case bipolar zero point error
= Bipolar zero drift x ΔT
= ±10ppm of FSR% (45°C) (100)
= ±0.045%

ORDERING INFORMATION

DAC80	X	–	XXX	–	X
Low Cost 12 Bit D/A Converter Family Example: DAC80-CBI-V Binary DAC80 with voltage output	Z = Wide Supply Range Blank = Standard		INPUT CODE CBI = Complementary 12 bit binary CCD = Complementary 3 digit BCD		OUTPUT V = Voltage I = Current

BURR-BROWN®

DAC82



8-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

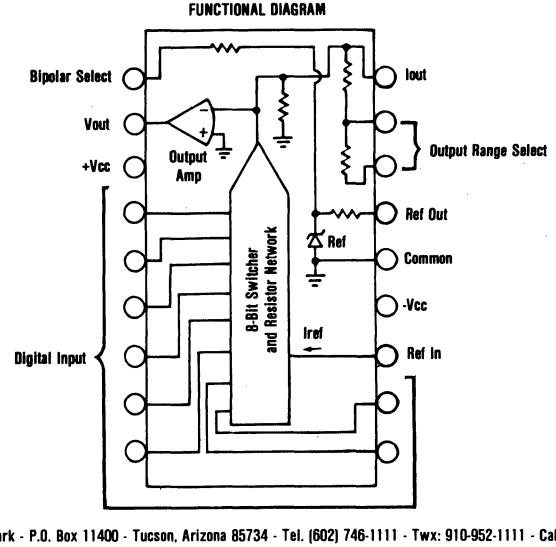
- 8-BIT RESOLUTION/LINEARITY
- NO EXTERNAL ADJUSTMENTS REQUIRED FOR ±1LSB ACCURACY
- INTERNAL REFERENCE AND SCALING RESISTORS
- 2-QUADRANT MULTIPLYING WITH EXTERNAL REFERENCE
- HERMETIC, DUAL-IN-LINE PACKAGE
- OPERATION OVER -55°C/+125°C

DESCRIPTION

The DAC82 is an 8-bit digital-to-analog converter with voltage and current outputs. Packaged in an 18-pin metal DIP, it is complete with its own internal reference and scaling resistors. When used with a variable, external reference, the DAC82 will multiply in two quadrants. Two versions are available: the DAC82BM (-25°C to +85°C) and the DAC82SM (-55°C to +125°C). Both offer ±1LSB absolute accuracy at room temperature with no external adjustments required and nonlineaity is guaranteed to be within ±1/2LSB over the specified temperature ranges. The small size of the DAC82 makes it an ideal choice for applications where space or weight is at a premium such as aircraft instrumentation, portable instruments, or CRT displays.

DAC82

FUNCTIONAL DIAGRAM



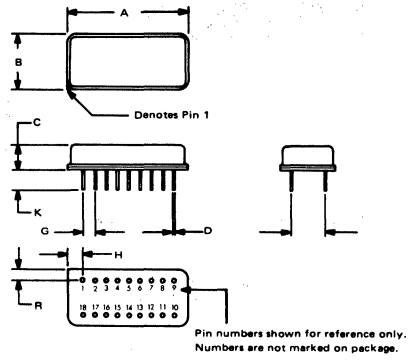
International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

ELECTRICAL SPECIFICATIONS

MODEL	DAC82KG DAC82BM	DAC82SM	UNITS
DIGITAL INPUT			
Resolution	8	8	Bits
Logic Levels (TTL compatible)			
Logic "1"	$+2 < e_d < +5.5$ at $+40\mu A$		V
Logic "0"	$0 < e_d < +0.8$ at -1.0mA		V
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error at 25°C (max)	±0.16	±0.16	% of FSR
-25°C to +85°C (max)	±0.2		% of FSR
-55°C to +125°C (max)		±0.2	% of FSR
Differential Linearity Error	±0.5	±0.5	LSB
Gain Error	±0.1	±0.1	%
Offset Error	±0.05	±0.05	% of FSR
Total Accuracy Error (max)	±1	±1	LSB
Monotonicity Temp Range	-25 to +85	-55 to +125	°C
DRIFT			
Gain (max)			
-25°C to +85°C	±50		ppm/°C
-55°C to +125°C		±35	ppm/°C
Offset			
Unipolar			
-25°C to +85°C	±1		ppm of FSR/°C
-55°C to +125°C		±1	ppm of FSR/°C
Bipolar (max)			
-25°C to +85°C	±20		ppm of FSR/°C
-55°C to +125°C		±15	ppm of FSR/°C
CONVERSION SPEED			
Voltage Output			
Settling time to ±0.2% of FSR			
For FSR change			
with 10kΩ Feedback	2.5		µsec
with 5kΩ Feedback	2.0		µsec
For 1 LSB change	0.5		µsec
Slew Rate	20		V/µsec
Current Output			
Settling time to ±0.2%			
For FSR change			
10 to 100Ω load	250		nsec
1kΩ load	350		nsec
OUTPUT			
ANALOG OUTPUT			
Voltage Output			
Ranges	±2.5, ±5, ±10, +5, +10		Volts
Output Current, min	±5		mA
Output Impedance (DC)	0.05		Ω
Current Output			
Ranges	±0.8, 0 to -1.6		mA
Output Impedance - Bipolar	1.8		kΩ
Unipolar	2.0		kΩ
Compliance	±4.0V		Volts
INTERNAL REFERENCE VOLTAGE			
Magnitude	+6.3		Volts
Tempco of Drift, max	±20		ppm/°C
POWER SUPPLY SENSITIVITY			
+15VDC Supply	±0.02		% of FSR/%Vs
-15VDC Supply	±0.002		% of FSR/%Vs
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15		Volts
Range	±14.0 to ±16.0		Volts
Supply Drain (No load)			
+15VDC	15		mA
-15VDC	10		mA
TEMPERATURE RANGE			
Specification	-25 to +85	-55 to +125	°C
Operating (double above drift specs)	-55 to +125	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C

MECHANICAL

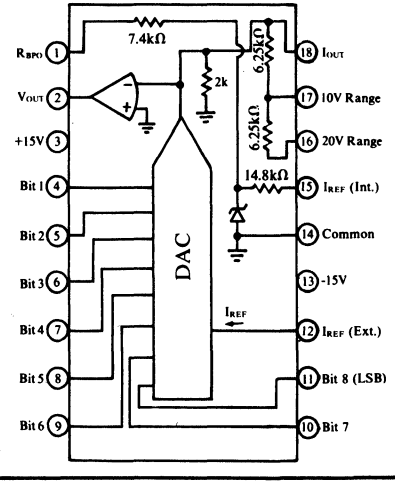
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.



CONNECTOR: None
CASE: Metal (BM, SM) Ceramic (KG)
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
HERMETICITY: Gross Leak (fluorocarbon) Fine Leak (helium, 5 x 10^{-7}cc/sec) (BM, SM only)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.060	1.080	26.92	27.43
B	.490	.510	12.45	12.95
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.115	.155	2.92	3.94
K	.150	.300	3.81	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.120	2.03	3.05

CONNECTION DIAGRAM



DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC82 accepts digital inputs in complementary binary (CBI) format and may be connected for complementary straight binary (CSB) or complementary offset binary (COB) operation. By using one external inverter, the user can operate the DAC82 in the complementary two's complement (CTC) mode.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
	0 to +10V	±10V	0 to 1.6mA	±0.8mA
MSB LSB				
0 0 0 0 0 0 0 0	+9.961V	+9.922V	-1.594mA	-0.794mA
0 1 1 1 1 1 1 1	+5.000V	0.000V	-0.800mA	0.000mA
1 0 0 0 0 0 0 0	+4.961V	-78.12mV	-0.792mA	+6.248μA
1 1 1 1 1 1 1 1	0.000V	-10.000V	0.000mA	+0.800mA
one LSB	39.06mV	78.12mV	6.248μA	6.248μA

* To obtain values for other binary (CBI) ranges:
0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE I. Digital Input and Analog Output Relationship.

ACCURACY

LINEARITY

The LINEARITY of a D/A converter is the true measure of its performance. The DAC82 analog output will not vary by more than ±1/2 LSB from an ideal straight line drawn between the end points (all 1's and all 0's) over the specified temperature range.

DIFFERENTIAL LINEARITY

The DIFFERENTIAL LINEARITY error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A DIFFERENTIAL LINEARITY error specification of ±1/2 LSB means that the output voltage can change anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent digital state to the next.

DRIFT

GAIN DRIFT

GAIN DRIFT is a measure of the change in the analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at the high and low temperature extremes and at 25°C for each model, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in output voltage at zero volts output over the specified temperature range. The offset voltage is measured at the temperature extremes, and the maximum change referenced to 25°C is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the time required for the output to enter and remain in an error band equal to ±0.2% of full scale range measured from the time the digital input is changed. Typical settling time values for full scale changes are a function of the load resistor and are shown in the figure below.

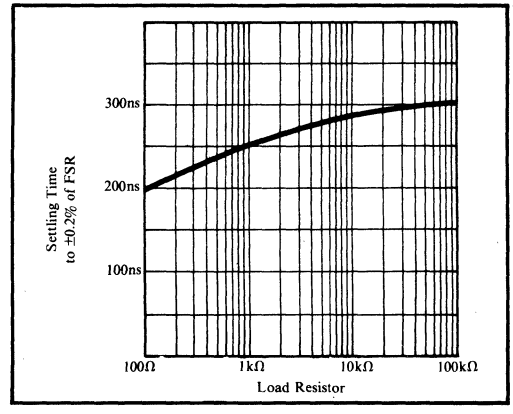


FIGURE 1. Settling Time for FSR Change vs Load.

COMPLIANCE

The COMPLIANCE VOLTAGE of the DAC82 is the maximum voltage swing allowed on the current output in order to maintain the specified accuracy. It is -4.0 to +4.0 volts for the unipolar and bipolar current ranges.

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR/percent of change in either the +15 volt or -15 volt power supplies about the nominal power supply voltages. Figure 2 shows Power Supply Rejection vs Frequency.

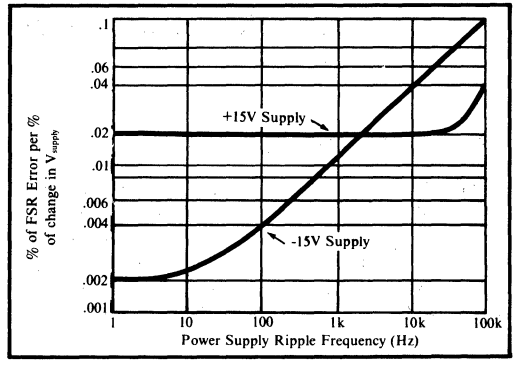


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC82 and should be tantalum or electrolytic types bypassed with a 0.01 μF ceramic capacitor for best high frequency performance.

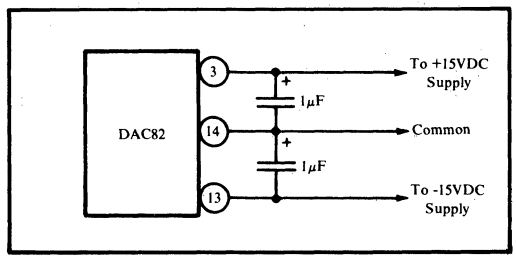


FIGURE 3. Recommended Power Supply Decoupling.

OPERATION IN THE CURRENT OUTPUT MODE

On the current output pin, the DAC82 provides a unipolar output current of 0 to -1.6mA and a bipolar output current of ±0.8mA. Refer to Figure 4 and Table II for proper connections. In applications requiring the use of the DAC82 in the current output mode, such as an A/D converter, the internal scaling resistors should be used to generate currents corresponding to analog input voltages.

OUTPUT RANGE	CONNECT PIN 1 TO:
0 to -1.6mA	N.C.
±0.8mA	Pin 18

TABLE II. Connections for Current Output Mode.

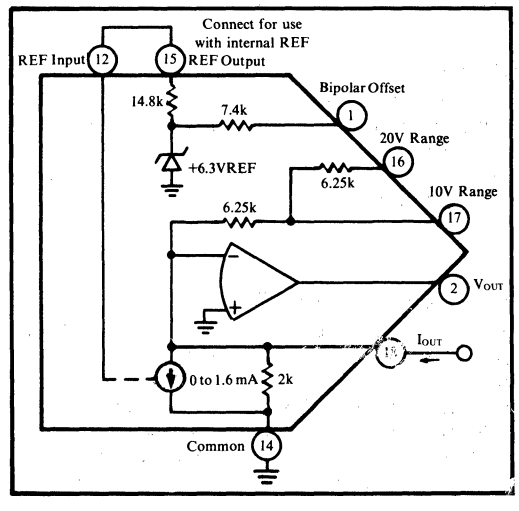


FIGURE 4. Current Output Mode Connection Diagram

DRIVING AN EXTERNAL OP AMP

UNIPOLAR OR BIPOLAR - UP TO 20V OUTPUT RANGE

The DAC82 will drive the summing junction of an op amp (the op amp being used as a current to voltage converter) to produce an output voltage (see Figure 5).

$$V_{OUT} = -I_{OUT} \times R_F$$

where I_{OUT} is the DAC82 output current and R_F is the feedback resistor. The internal feedback resistors should be used to maintain the temperature drift specification. Refer to Table III and Figure 5 for proper connections.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT Ⓐ TO	CONNECT PIN 1 TO	CONNECT PIN 16 TO
±10V	COB or CTC	16	18	Ⓐ
±5V	COB or CTC	17	18	N.C.
±2.5V	COB or CTC	17	18	18
0 to +10V	CSB	17	Common	N.C.
0 to +5V	CSB	17	Common	18

TABLE III. Voltage Ranges of Current Output DAC82 with External Op Amp.

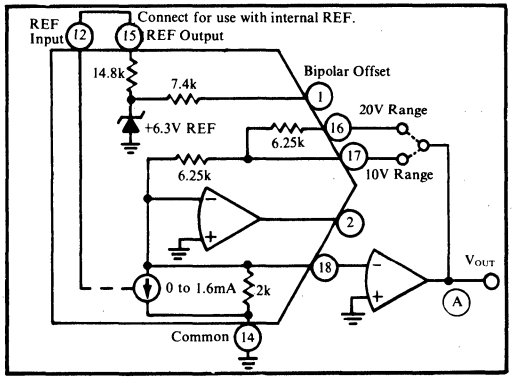


FIGURE 5. External Op Amp - Using Internal Feedback Resistors.

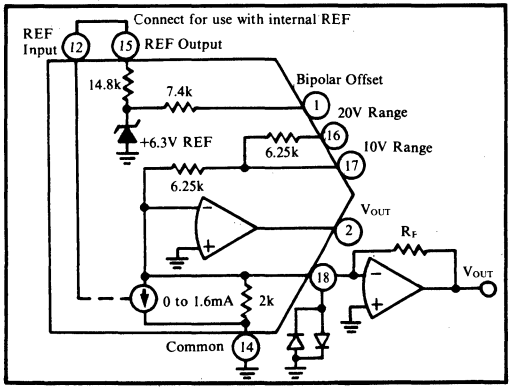


FIGURE 6. External Op Amp - Using External Feedback Resistors.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±0.8mA for bipolar voltage ranges, and 0 to -1.6mA for unipolar voltage ranges (see Figure 6). Use protection diodes when a high voltage op amp is used.

VOLTAGE OUTPUT OPERATION USING INTERNAL AMPLIFIER

The DAC82 contains internal scaling resistors to provide a wide range of output voltage ranges. These resistors may be connected to provide 3 bipolar output ranges of ±10, ±5, or ±2.5 volts or two unipolar output voltage ranges of 0 to +5 or 0 to +10 volts. Gain and offset drift errors are minimized since these scaling resistors are an integral part of the DAC. Connections for DAC82 output voltage ranges are shown in Table IV and Figure 7 below.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 2 TO	CONNECT PIN 1 TO	CONNECT PIN 16 TO
±10V	COB or CTC	16	18	2
±5V	COB or CTC	17	18	N.C.
±2.5V	COB or CTC	17	18	18
0 to +10V	CSB	17	Common	N.C.
0 to +5V	CSB	17	Common	18

TABLE IV. Voltage Ranges of Current Output DAC82 with External Op Amp.

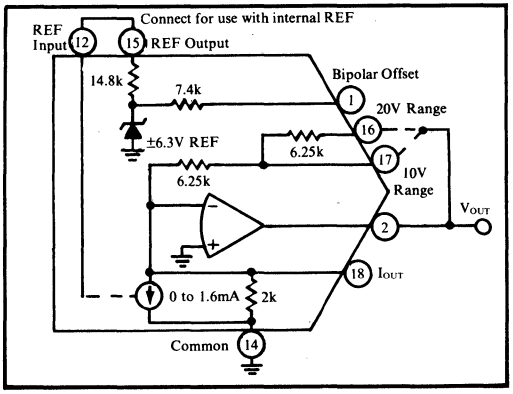


FIGURE 7. Voltage Output Using Internal Amplifier.

OPERATION AS MULTIPLYING DAC

By using an external voltage reference, the DAC82 can be connected as a multiplying DAC, such that the analog output represents the product of the digital input and the analog reference input. To operate the DAC82 as a two quadrant MDAC, connect the unit as shown in Figure 8. If R2, the bipolar offset resistor, is replaced with an open circuit, the DAC will operate in one quadrant. Table V below shows the digital input and analog output relationships for one quadrant and two quadrant multiplication and Figure 8 shows the connection for output voltage or output current. Since the absolute temperature coefficient of the internal feedback resistors (6.25k) is typically 30 ppm/°C, improved temperature stability can be achieved by using an external 13.5k resistor connected between pins 2 and pins 18, making no connection to pins 16 or 17.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
MSB LSB	0 to +10V	±10V	0 to -1.6mA	±0.8mA
00000000	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.9961)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.9922)$	$\frac{(4\ V_R)}{(R_1)}(0.9961)$	$\frac{(4\ V_R)}{(R_1)}(0.9922)$
0111111	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.5000)$	0.0000	$\frac{(4\ V_R)}{(R_1)}(0.5000)$	0.0000
10000000	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.4961)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(-0.0078)$	$\frac{(4\ V_R)}{(R_1)}(0.4961)$	$\frac{(4\ V_R)}{(R_1)}(-0.0078)$
1111111	0.0000	$\frac{(4\ V_R)(R_F)}{(R_1)}(-1)$	0.0000	$\frac{(4\ V_R)}{(R_1)}(-1)$
1 LSB	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.0039)$	$\frac{(4\ V_R)(R_F)}{(R_1)}(0.0078)$	$\frac{(4\ V_R)}{(R_1)}(0.0039)$	$\frac{(4\ V_R)}{(R_1)}(0.0078)$

TABLE V. Digital Input and Analog Output Relationship for Multiplying Configuration.

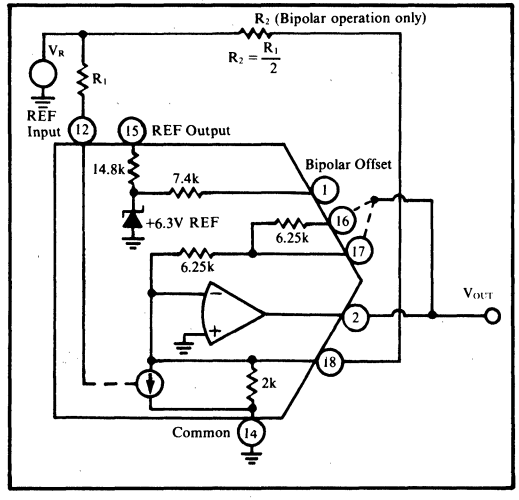


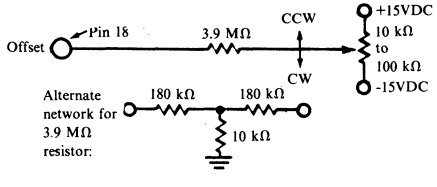
FIGURE 8. Connection for Multiplying Mode.

OPTIONAL EXTERNAL OFFSET AND GAIN ADJUSTMENTS

The DAC82 has been laser trimmed at the factory to insure absolute accuracy of 1 LSB at +25°C. However, externally connected offset and gain potentiometers may be used to null these error components to zero. If these adjustments are not used, simply leave the pins open. Adjustment networks should be located physically closed to the DAC82 to minimize signal pickup.

OFFSET ADJUSTMENT

For unipolar operation, apply the digital input code that should give zero volts output and adjust the OFFSET potentiometer for zero volts output. For bipolar operation, apply the digital input code that should give the maximum negative voltage output. Example: If the FULL SCALE RANGE is connected for 20 volts, then the maximum negative voltage output is -10 volts. See Table I for corresponding codes.



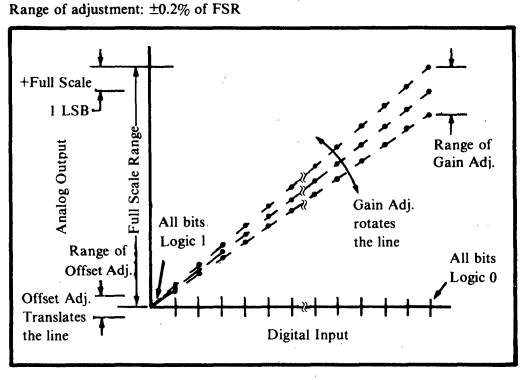
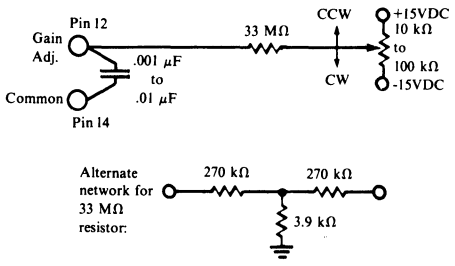


FIGURE 9. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar D/A converters, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. The positive full scale voltages for the DAC82 are given in Table V.



Range of Offset Adjustment: ±0.2% of FSR

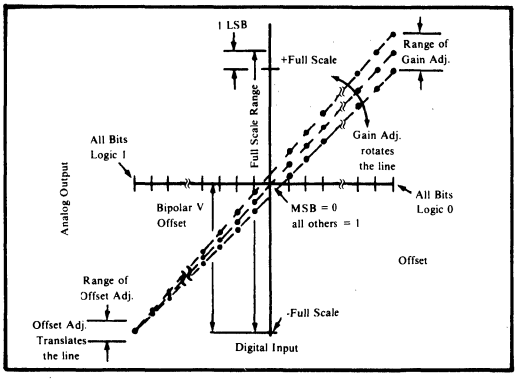


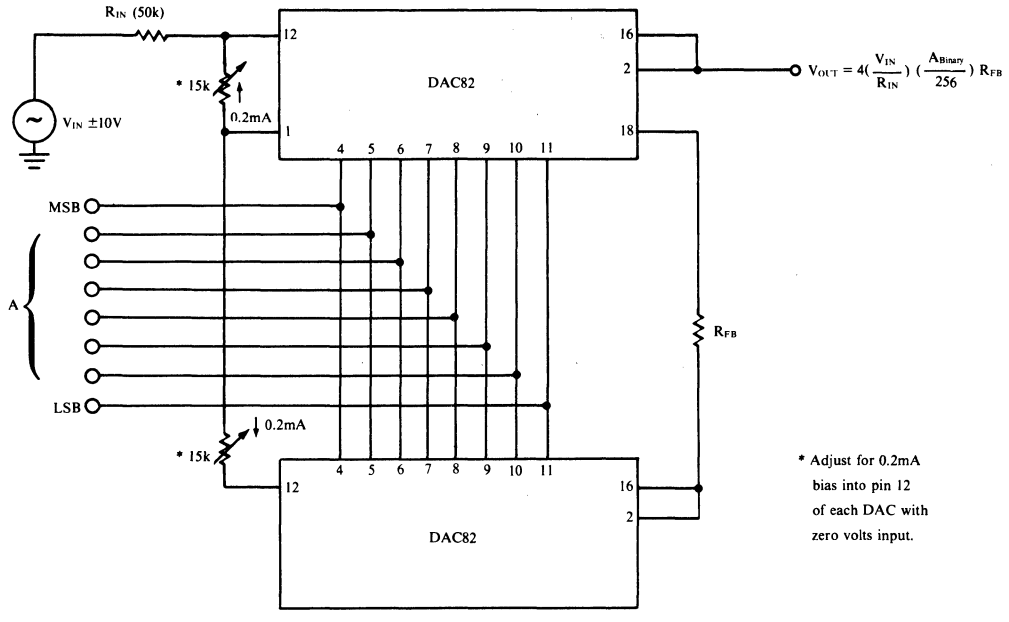
FIGURE 10. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter.

APPLICATIONS

Two DAC82's can be connected as shown to construct a digitally-controlled attenuator which will accept bipolar input voltages. Since the input to the DAC is a summing junction (pin 12), input voltages greater than ±10V can be used if R_{IN} is increased proportionately. The transfer function is:

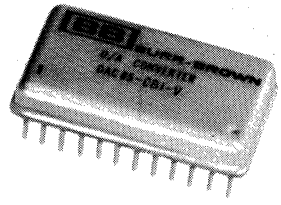
$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{4\ R_{FB}}{R_{IN}}\right)\left(\frac{A_{BINARY}}{256}\right)$$

To remove initial gain errors, the two 15k resistors should be adjusted such that 0.2 mA flows into pin 12 of each DAC82 when $V_{IN} = 0$.



DIGITALLY CONTROLLED ATTENUATOR WITH BIPOLAR INPUT

BURR-BROWN®



DAC85

Hybrid Microcircuit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 12-BIT RESOLUTION
- LASER-TRIMMED TO ±1/2LSB LINEARITY
- CURRENT OR VOLTAGE OUTPUT
- FAST SETTLING - 300nsec to ±.01% (Current Output Model)
- HERMETIC DUAL-IN-LINE PACKAGE
- LOW COST

DESCRIPTION

The DAC85 12-bit D/A converter offers quality performance usually found in larger modular units. Housed in a 24-pin dual-in-line metal case, this D/A converter is complete with internal reference and output amplifier and is engineered to preserve the performance normally found only in much larger, higher cost modular units, while providing sealed protection from rugged environments.

Highly stable laser-trimmed thin-film resistors and our Model 4550 quad current switches provide low nonlinearities of ±0.012% over 0°C to 70°C (DAC85C) and ±0.012% over -25°C to +85°C (DAC85 and DAC85LD) operating temperature ranges. Current output models settle to ±0.01% in 300nsec while voltage output models settle to ±0.01% in 5μsec, permitting throughput rates as high as 3MHz for full scale range changes.

The small size of the DAC85 makes it an ideal choice as the heart of your A/D converter design or for applications where space or weight is at a premium, such as CRT displays, aircraft instrumentation and portable instruments. The wide choice of performance models allows you to choose the right unit for your application and budget.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

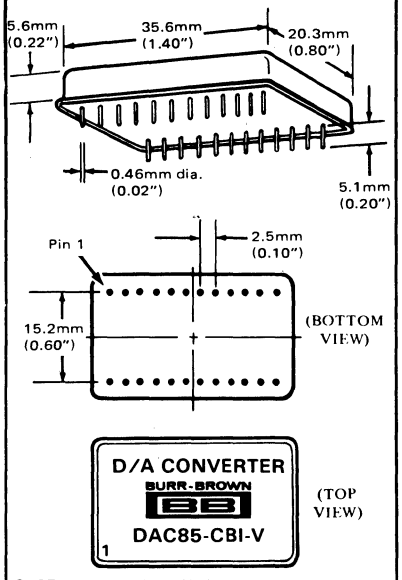
SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC85C		DAC85		DAC85LD	Units
Binary	CBI		CBI		CBI	
Decimal		CCD		CCD		
INPUT						
DIGITAL INPUT						
Resolution	12	3	12	3	12	Bits Digits
Logic Levels (TTL compatible)						
Logic "1"(1)	+2 < e_d < +5.5 at +40 μA					V
Logic "0"(2)	0 < e_d < +0.8 at -1.0 mA					V
TRANSFER CHARACTERISTICS						
ACCURACY						
Linearity Error @ 25°C (max)	±1/2	±1/4	±1/2	±1/4	±1/2	LSB
0°C to +70°C (max)	±1/2	±1/2				LSB
-25°C to +85°C (max)			±1/2	±1/2	±1/2	LSB
Differential Linearity Error	±1/2					LSB
Gain Error(3)	±0.1					%
Offset Error(3)	±0.05					% of FSR(4)
Minimum Temperature Range for Guaranteed Monotonicity	0 to +70		-25 to +85			°C
DRIFT(5)						
Gain						
0°C to +70°C (max)	±20		±20		±10	ppm/°C
-25°C to +85°C (max)	—		±20		±10	ppm/°C
Offset						
Unipolar 0°C to +70°C	±1					ppm of FSR/°C
-25°C to +85°C			±1		±1	ppm of FSR/°C
Bipolar 0°C to +70°C (max)	±10					ppm of FSR/°C
-25°C to +85°C(max)			±10		±5	ppm of FSR/°C
CONVERSION SPEED						
Voltage Models						
Settling time to ±0.01% of FSR for FSR change						
with 10 kΩ Feedback	5					μsec
with 5 kΩ Feedback	3					μsec
for 1 LSB change	1.5					μsec
Slew Rate	20					V/μsec
Current Models						
Settling time to ±0.01% of FSR for FSR change						
10 to 100 Ω load	300					nsec
1 kΩ load	1					μsec
OUTPUT						
ANALOG OUTPUT						
Voltage Models						
Ranges — CBI Units	±2.5, ±5, ±10, +5, +10					V
CCD Units	+10					V
Output Current (min)	±5					mA
Output Impedance (dc)	0.05					Ω
Current Models						
Ranges	±1, -2					mA
Output Impedance - Bipolar	4.4					kΩ
Unipolar	15					kΩ
Compliance	±2.5					V
Internal Reference Voltage (V_f)	6.3					V
Max. External Current(6)	200					μA
Tempco of Drift (max)	±10	±10	±10	±10	±5	ppm of V_f/°C
POWER SUPPLY SENSITIVITY						
+15V Supply	±0.02					% of FSR/%Vs
-15 and +5V Supplies	±0.002					% of FSR/%Vs
POWER SUPPLY REQUIREMENTS						
Rated Voltage	±15 and +5					V
Range	±14.5 to ±15.5 and +4.75 to +15.5(7)					V
Supply Drain						
±15 V (including 5 mA load)	±25					mA
+5 V	+20					mA
TEMPERATURE RANGE						
Specification	0 to +70		-25 to +85			°C
Operating(double above drift specs)	-25 to +85		-25 to +85			°C
Storage	-55 to +100		-55 to +100			°C

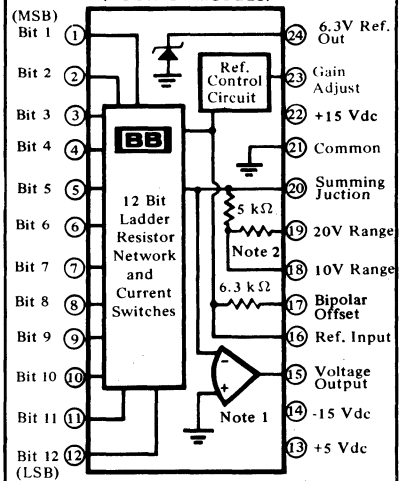
1. Logic "1" current = 40μA max at V_{IN} = +5.0V
2. Logic "0" current = -1.6mA max at V_{IN} = +0.4V
3. Adjustable to zero with external trim potentiometer.
4. FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range etc.
5. To maintain drift spec internal feedback resistors must be used for current output models.
6. With no degradation of specifications.
7. Operating logic supply at +15.5V increases power dissipation 200mW.

MECHANICAL



CASE: Kovar, Gold or Nickel Plated
MATING CONNECTOR 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
WEIGHT: 8.4 grams (0.3 oz.)

CONNECTION DIAGRAM



Note 1: Amplifier not included in current output models.
Note 2: 3 kΩ for CCD models
5 kΩ for CBI models

DAC85

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC85 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be user connected for any one of three complementary binary codes: CSB, CTC, or COB.

	DIGITAL INPUT	ANALOG OUTPUT		
	MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	000000000000	+Full Scale	+Full Scale	-LSB
	011111111111	+1/2 Full Scale	Zero	-Full Scale
	100000000000	Mid Scale -1 LSB	-1 LSB	+Full Scale
	111111111111	Zero	-Full Scale	Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110	+Full Scale		
	1111 1111 1111	Zero		

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE 1. Digital Input Codes.

ACCURACY

LINEARITY

The linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC85 and DAC-85C is specified over the entire specification temperature ranges. The definition of this specification means that the analog output will not vary by more than ±1/2LSB from an ideal straight line drawn between the end points (all bits ON and all bits OFF) over the specified operating temperature range.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage can change anywhere from 1/2 LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

DRIFT

GAIN DRIFT

GAIN DRIFT is a measure of the change in the full scale range analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at -25°C or 0°C, +25°C and +70°C or +85°C for each model and calculating the GAIN ERROR with respect to the 25°C value and dividing by the temperature change. This specification is expressed in ppm/°C.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in the output with all bits OFF (V_{OUT}^{OFF}) over the specified temperature range. V_{OUT}^{OFF} is measured at -25°C or 0°C, +25°C and +70°C or +85°C. The maximum change in OFFSET is referenced to the OFFSET at 25°C divided by the temperature range. This drift is expressed in parts per million of full scale range per °C. (ppm of FSR/°C).

SETTLING TIME

The settling time for each model DAC85 is the total time (including slew time) for the output to settle to within an error band about its final value after a change in the input.

VOLTAGE OUTPUT MODELS

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V and 10V and also for a 1 LSB change. The 1 LSB change is measured at the major carry (0111 ... 11 to 1000 ... 00) since this is the point where the worst case settling time occurs.

CURRENT OUTPUT MODELS

Two settling times are specified for current output models; each specified settling time to ±0.01% of FSR is given for the DAC85 current models connected with two different resistive loads – i.e., 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 ohms to 1800 ohms for output voltage ranges of ±1 volt and 0 to -2 volts. (See Table 4)

COMPLIANCE

The compliance voltage of the DAC85 is the maximum voltage swing allowed on the current output mode in order to maintain the specified accuracy; it is ±2.5 volts for the bipolar current range of ±1.0 mA and is -2.5 volts for the unipolar current range of 0 to -2 mA. The maximum safe voltage swing allowed with no damage to the DAC85 output is ±5 volts for current output models.

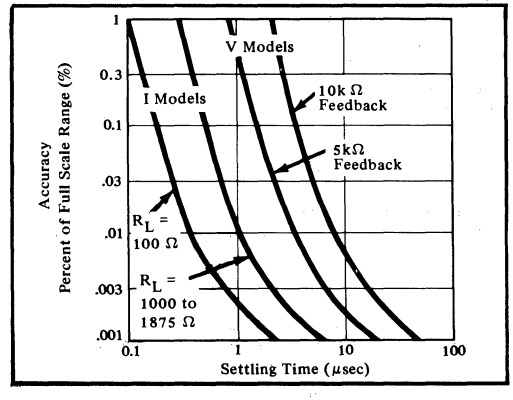


FIGURE 1. Full Scale Range Settling Time vs. Accuracy.

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the +15 volt or -15 volt and +5 power supplies about the nominal power supply voltages. Figure 2 shows Power Supply rejection vs. frequency.

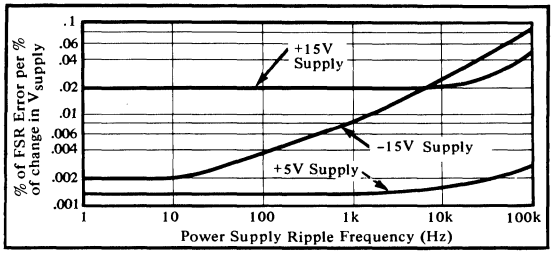


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

REFERENCE SUPPLY

All DAC85 models are supplied with an internal 6.3 volt reference voltage supply. This reference voltage (pin 24) has a tolerance of ±5%, and must be connected to the Reference Input (pin 16) for specified operation.

This reference may also be used externally, but the current drain is limited to 200 μA. An external buffer amplifier is recommended if the DAC85 internal reference will be externally used in order to provide a constant load to the reference supply output.

ORDERING INFORMATION

DAC85 XX – XXX – X

- DAC85: 12-Bit D/A Converter Family
- XX: C = 0 to +70°C Model; LD = Low drift -25°C to +85°C Model; Leave blank for -25°C to +85°C Model
- XXX: INPUT CODE — CBI = Complementary 12-bit binary; CCD = Complementary 3-digit BCD (not available for DAC85LD)
- X: OUTPUT — V = Voltage; I = Current (not available for LD model)

Example: DAC85-CBI-V DAC85 with voltage output, Binary code and -25°C to +85°C temp. range.

OPERATING INSTRUCTIONS

DIGITAL INPUT AND ANALOG OUTPUT RELATIONSHIP

Digital Input Codes	Output Range			
	Voltage *		Current	
	0 to +10V	±10V	0 to -2mA	±1mA
Binary (CBI)				
12 bit resolution				
One LSB	+2.44mV	4.88mV	0.488μA	0.488μA
All bits ON	+9.9976V	+9.9951V	−1.9995mA	-0.9995mA
All bits OFF	Zero	−10.000V	Zero	+1.0000mA
Decimal (CCD)				
3 digit resolution				
One LSB	10 mV		1.25μA	
+ FS bits ON	+9.99V†	N/A	−1.249mA	N/A
All bits OFF	Zero		Zero	

TABLF 2. Ideal Output Voltage and Current.

†Normal full scale range with correct codes; output can go to +12 volts if illegal codes are applied.

*To obtain values for other binary (CBI) ranges:

0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

POWER SUPPLY CONNECTIONS

DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC85 and should be tantalum or electrolytic types bypassed with a 0.01 μF ceramic capacitor for best high frequency performance.

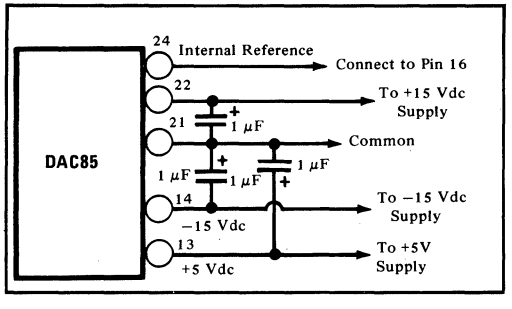


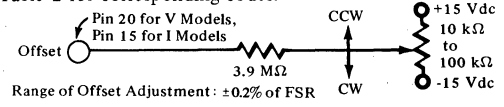
FIGURE 3. Recommended Power Supply Decoupling.

EXTERNAL OFFSET and GAIN ADJUSTMENT

Offset and gain may be trimmed externally by the user with externally connected OFFSET and GAIN potentiometers. If gain and offset adjust circuits are not used, pins 15, 20, and 23 should be connected as described in other sections herein. (Do not ground.) Connection of the potentiometers and the methods of adjutments is as outlined below. Potentiometer resistance values indicated are range of values. Potentiometers should have TCR of 100ppm/°C or less. The 3.9MΩ and 18MΩ resistors can be 20% carbon composition or better. These two resistors should be located close to the DAC85 to prevent signal pickup.

OFFSET ADJUSTMENT

For unipolar (CSB, CCD) D/A converters, apply the digital input code that should give zero volts output and adjust the OFFSET potentiometer for zero volts output. For bipolar (COB, CTC) D/A converters, apply the digital input code that should give the maximum negative voltage output. Example: If the FULL SCALE RANGE is connected for 20 volts, then the maximum negative voltage output is -10 volts. See Table 2 for corresponding codes.



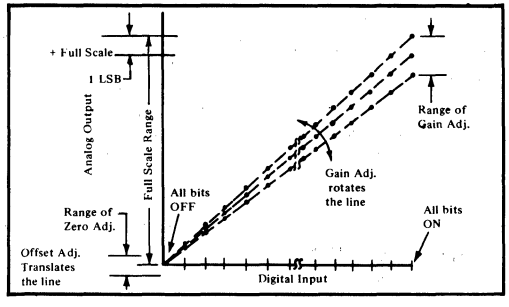
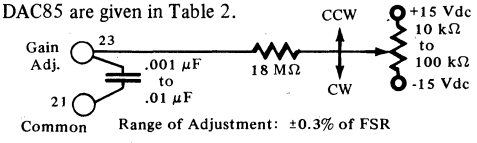


FIGURE 4. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar D/A converters, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. The positive full scale voltages for the DAC85 are given in Table 2.



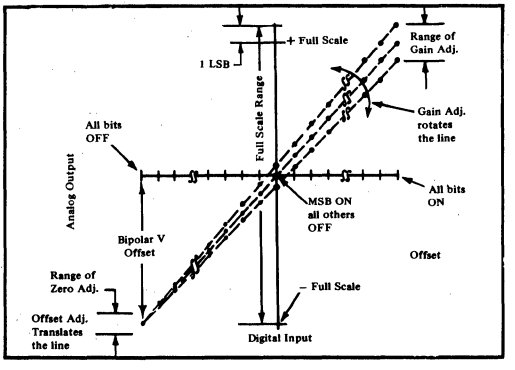


FIGURE 5. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter.

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

Internal scaling resistors are provided in the DAC85 to provide a wide range of output voltage range connections. These internal resistors may be connected to provide three bipolar output voltage ranges of ±10, ±5 or ±2.5 volts or two unipolar output voltage ranges of 0 to +5 or 0 to +10 volts. Since these internal scaling resistors are an integral part of the DAC85, gain and offset drift is minimized. Connections for DAC85 output voltage ranges are shown in Table 3.

Settling time for these voltage ranges is specified for a full scale range change, and is 5 microseconds for 8 kΩ or 10 kΩ and 3 microseconds for a 5 kΩ feedback resistor.

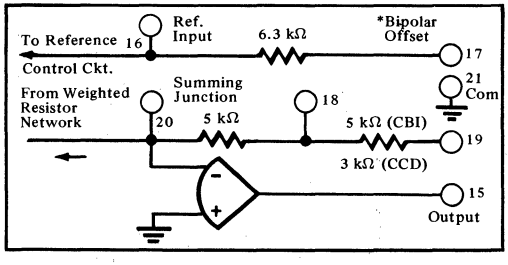


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.
*pin 17 not connected for CCD models. The 6.3 kΩ resistor is internally connected to common.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

TABLE 3. Output Voltage Range Connections – Voltage Model DAC85.

CURRENT OUTPUT MODELS

Internal resistors are provided either for scaling an external op amp to the same voltage ranges as the voltage model DAC85 or for configuring a resistive load to provide two output voltage ranges of ±1 volt or 0 to -2 volts. These internal resistors (R_{LI}) are an integral part of the DAC85 design, and are required to maintain the gain and bipolar offset drift specifications of the DAC85. If the internal resistors are not used, external R_L or R_F resistors should have ±25 ppm/°C or less temperature coefficient to minimize drift.

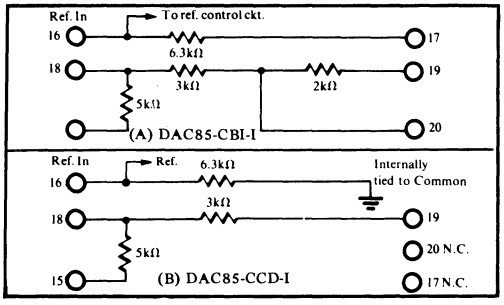


FIGURE 7. Internal Scaling Resistors.

The current model DAC85 equivalent output circuit and resistive scaling network is different from the voltage model DAC85, and is shown in Figure 7 and 8 for reference.

Instructions for using the DAC85-xxx-I with either a resistive load or an external op amp are on the following pages. External R_{LS} or R_{LP} resistors are required to give exactly 0 to -2V or ±1V output range. These resistors should have a TCR of ±100 ppm/°C or less. If these exact output ranges are not required, R_{LS} (or R_{LP}) need not be used as discussed below.

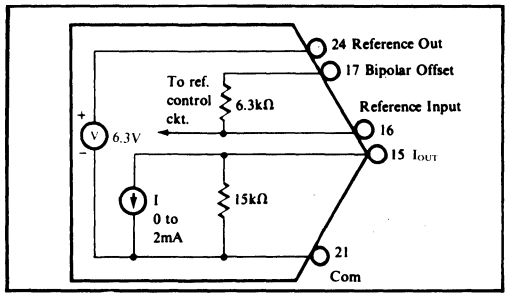


FIGURE 8. DAC85 Current Model Equivalent Output Circuit.

Voltage Output Using Resistive Load

UNIPOLAR

BINARY INPUT CODE (CSB)

A load resistance R_L connected to the output as shown in Figure 9, will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2\ mA \left(\frac{15\ k \times R_L}{15\ k + R_L} \right)$$

where R_L max = 1.36 kΩ
and V_{OUT} max = -2.5 volts

For minimum drift as specified, the internal scaling resistor (R_{LI}) should be connected as shown in Table 4 for the CSB code with a series connected external metal film full scale trim resistor (R_{LS}) to provide a full scale output voltage range of 0 to -2 volts. With R_{LS} = 0, V_{OUT} = -1.82V.

BCD INPUT CODE (CCD)

Connect the internal scaling resistors as shown in Table 4, and add an external parallel connected metal film resistor (R_{LP}) as shown in Figure 10 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes. With R_{LP} = ∞, V_{OUT} = -2.08V.

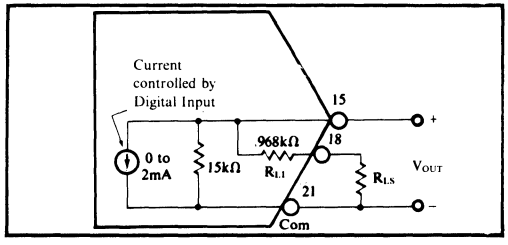


FIGURE 9. Equivalent Circuit DAC85-CBI-I connected for Unipolar Voltage Output with Resistive Load.

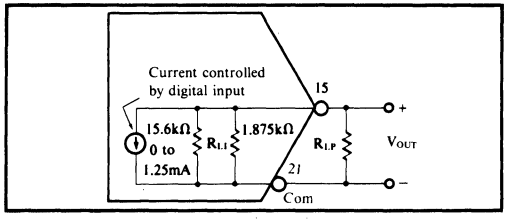


FIGURE 10. DAC85-CCD-I Connected for Voltage Output with Resistive Load.

Input Code	Output Voltage Range	Internal Resistance R_{LI}	1% Metal Film External Resistor R_{LS}	1% Metal Film External Resistor R_{LP}	R_{LI} Connections: Connect Pin 15 to	R_{LI} Connections: Connect Pin 18 to	R_{LI} Connections: Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	Bipolar Offset: R_{LS}	Bipolar Offset: R_{LP}
CSB	0 to -2V	0.968 kΩ	105 Ω	N/A	20	19 & R_{LS}	15	24	21 (Com)	Between pin 18 & 21	N/A
CCD	0 to -2V	1.875 kΩ	N/A	36.5 kΩ	19	21 (Com)	N.C.	24	N.C.	N/A	Between pin 15 & 21
COB or CTC	±1V	1.2 kΩ	90.9 Ω	N/A	18	19	R_{LS}	24	15	Between pin 20 & 21	N/A

TABLE 4. DAC85X - XXX - I Resistive Load Connections.

BIPOLAR

COB and CTC INPUT CODES

The equivalent output circuit for a bipolar output voltage range is shown in Figure 11. V_{OUT} is determined by:

$$V_{OUT} = \pm 1 \text{ mA} \times \left(\frac{R_L \times 4.44\text{ k}}{R_L + 4.44\text{ k}} \right)$$

where R_L max = 5.72 kΩ
V_{OUT} max = ±2.5 volts

For minimum drifts (as specified) the internal scaling resistors (R_{LI}) are connected as shown in Table 4 for the COB or CTC codes and an external series connected metal film resistor (R_{LS}) is added to obtain a full scale output voltage range of ±1 volt. With R_{LS} = 0, V_{OUT} = ±0.944V.

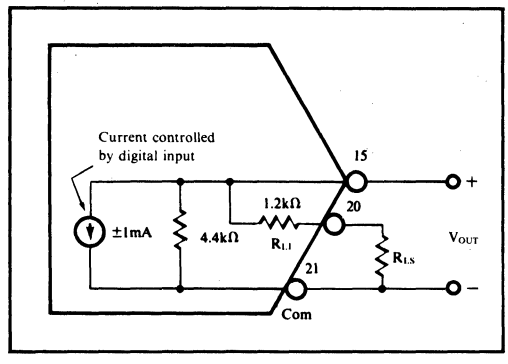


FIGURE 11. DAC85-CBI-I Connected for Bipolar Output Voltage with Resistive Load.

SETTLING TIME

The current output DAC85 models have a specified settling time of 300 nanoseconds with a 100 ohm load. Settling time increases as the load resistance increases due to the RC time constant of R_L and the summing junction capacitance.

Driving an External Op Amp

UNIPOLAR or BIPOLAR – Up to 20V Output Range

The current model DAC85 will drive the summing junction of an op amp (the op amp being used as a current to voltage converter) to produce an output voltage (see Figure 12):

$$V_{OUT} = -I \times R_F$$

where I_{OUT} is the DAC85 output current and R_F is the feedback resistor. Use of the internal feedback resistors of the DAC85 will provide the same output voltage ranges as the voltage model DAC85. Table 5 must be used for connecting the external op amp to obtain the desired output voltage range.

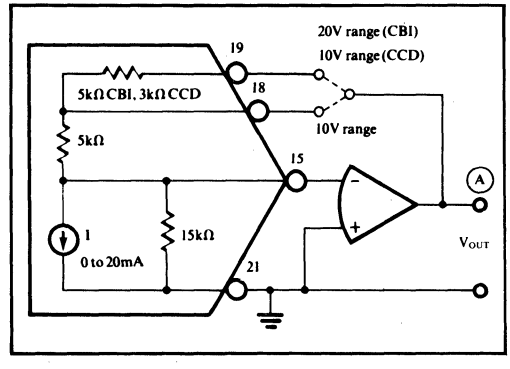


FIGURE 12. External Op Amp - Using Internal Feedback Resistors.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	Ⓐ	24

TABLE 5. Voltage Ranges of Current Output DAC85 with External Op Amp.

OUTPUTS LARGER THAN 20 VOLT RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1 mA for bipolar voltage ranges, and -2 mA for unipolar voltage ranges (see Figure 13). Use protection diodes when a high voltage op amp is used.

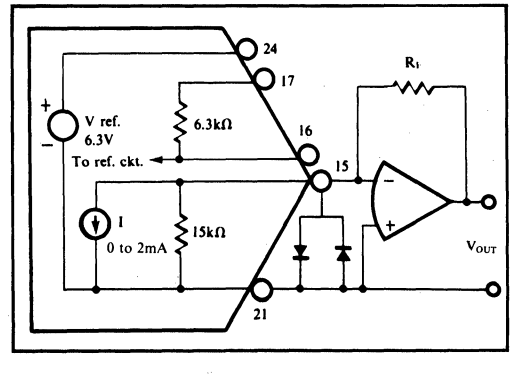


FIGURE 13. External Op Amp - Using External Feedback Resistors.

BUILDING AN A/D CONVERTER

The small size and good performance of the DAC85 makes it an excellent component for building A/D converters. The most popular medium speed (1 μsec/bit to 10 μsec/bit) A/D converter is the successive approximations type, in which the digital output equivalent of the analog input is formed by comparing a programmed D/A converter output with the analog input. The digital output is successively compared one bit at a time until the final comparison is within ± 1/2 bit of the resolution of the D/A converter.

The conversion speed of a successive approximation A/D converter constructed around a DAC85 is determined by the settling speed to ±1/2 LSB, the speed of the comparator, and the switching speed of the successive approximations logic. The A/D converter shown in Figure 14 will convert at speeds in excess of 60 kHz for 12 bits and near 80 kHz for 10 bits.

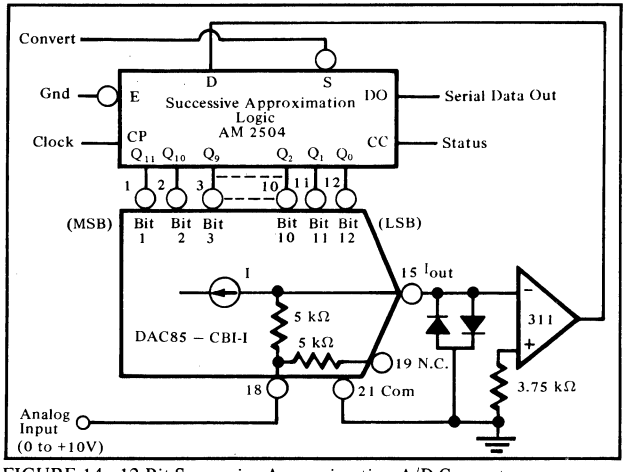
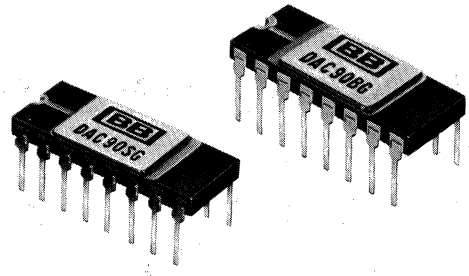


FIGURE 14. 12-Bit Successive Approximation A/D Converter.

BURR-BROWN®



DAC90

Monolithic Microcircuit DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 8-BIT RESOLUTION
- CURRENT OUTPUT
- FAST SETTLING
  200nsec to ±0.2%
- HERMETIC DUAL-IN-LINE PACKAGE
- LOW COST
- INTERNAL REFERENCE AND SCALING RESISTORS

DESCRIPTION

The DAC90 is an 8-bit D/A Converter that offers performance usually found only in larger, modular units. Housed in a 16-pin ceramic dual-in-line package, the DAC90 is complete with its own internal reference and scaling resistors.

Two versions are available: the DAC90BG (-25°C to +85°C) and DAC90SG (-55°C to +125°C) both offer ±0.2% nonlinearity over their respective temperature ranges. Settling time to ±0.2% is typically 200nsec.

The small size of the DAC90 makes it an ideal choice as the heart of your A/D converter design or for applications where space or weight is at a premium, such as CRT displays, aircraft instrumentation, and portable instruments.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-347B

Printed in U.S.A. July, 1978

SPECIFICATIONS

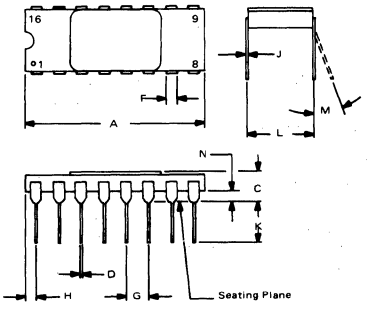
Typical at 25°C and rated power supplies unless otherwise noted.

ELECTRICAL

MODEL	DAC90BG	DAC90SG	UNITS
DIGITAL INPUT			
Resolution	8	8	Bits
Logic Levels (TTL-compatible)			
Logic "1"	$+2 < e_d < +5.5$ at $+40\mu A$		V
Logic "0"	$0 < e_d < +0.8$ at -1.0mA		V
TRANSFER CHARACTERISTICS			
ACCURACY			
Linearity Error at 25°C, max	±1/2	±1/2	LSB
-25°C to +85°C, max	±1/2		LSB
-55°C to +125°C, max		±1/2	LSB
Differential Linearity Error	±1/2	±1/2	LSB
Gain Error (1)	5	5	%
Offset Error (1)	1	1	% of FSR (2)
Minimum Temperature Range for Guaranteed Monotonicity	-25 to +85	-55 to +125	°C
DRIFT (3)			
Gain			
-25°C to +85°C	±50		ppm/°C
-55°C to +125°C		±50	ppm/°C
Offset			
Unipolar			
-25°C to +85°C	±1		ppm of FSR/°C
-55°C to +125°C		±1	ppm of FSR/°C
Bipolar			
-25°C to +85°C	±50		ppm of FSR/°C
-55°C to +125°C		±50	ppm of FSR/°C
CONVERSION SPEED			
Settling time to ±0.2% of FSR for FSR change			
10Ω to 100Ω load	200		nsec
1kΩ load	300		nsec
ANALOG OUTPUT			
Ranges	±1, 0 to -2		mA
Output Impedance – Bipolar	1.8		kΩ
Unipolar	2		kΩ
Compliance	-4 to +4		V
Internal Reference Voltage (V_r)	7.6		V
Tempco of Drift	±50	±50	ppm of V_r/°C
POWER SUPPLY SENSITIVITY			
+15VDC	±0.02		% of FSR/%Vs
-15VDC	±0.002		% of FSR/%Vs
POWER SUPPLY REQUIREMENTS			
Rated Voltage	±15		VDC
Range	±14.5 to ±15.5		VDC
Supply Drain ±15VDC	7		mA
TEMPERATURE RANGE			
Specification	-25 to +85	-55 to +125	°C
Operating	-55 to +125	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C

1. Adjustable to zero with external trim potentiometer.
2. FSR means "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.
3. To maintain drift spec internal feedback resistors must be used.
4. **Connect to ground if gain adjust circuit is not used.**

MECHANICAL

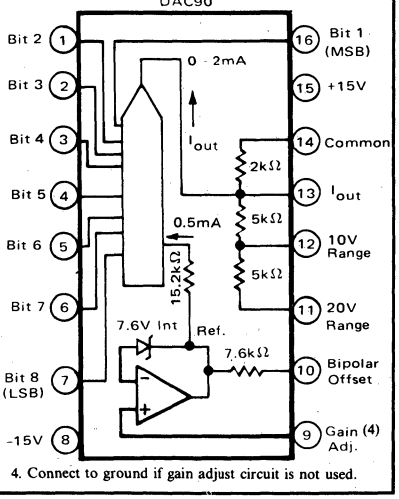


NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.790	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.048	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

CONNECTOR: None CASE: Ceramic, with hermetic seal. PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2) HERMETICITY: Fluoro-carbon (gross leak) and Helium 5 x 10^{-7}cc/sec (fine leak).

CONNECTION DIAGRAM



4. Connect to ground if gain adjust circuit is not used.

DAC90

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC90 accepts digital inputs in complementary binary (CBI) format and may be connected for complementary straight binary (CSB) or complementary offset binary (COB) operation (see Table I). By using one external inverter, the user can operate the DAC90 in the complementary two's complement (CTC) mode.

DIGITAL INPUT CODES	OUTPUT RANGE			
	VOLTAGE*		CURRENT	
	0 to +10V	±10V	0 to -2mA	±1mA
MSB LSB				
0 0 0 0 0 0 0 0	+9.961V	+9.922V	-1.992mA	-0.992mA
0 1 1 1 1 1 1 1	+5.000V	0.000V	-1.000mA	0.0000mA
1 0 0 0 0 0 0 0	+4.961V	-78.12mV	-0.99mA	+7.81μA
1 1 1 1 1 1 1 1	0.000V	-10.000V	0.000mA	+1.000mA
one LSB	39.06mV	78.12mV	7.81μA	7.81μA

* Requires external amplifier. To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE I.Digital Input and Analog Output Relationship.

ACCURACY

LINEARITY

The LINEARITY of a D/A converter is the true measure of its performance. The DAC90 analog output will not vary by more than ±1/2LSB from an ideal straight line drawn between the end points (all 1's and all 0's) over the specified temperature range.

DIFFERENTIAL LINEARITY

DIFFERENTIAL LINEARITY error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A DIFFERENTIAL LINEARITY error specification of ±1/2LSB means that the output voltage can change anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent digital state to the next.

DRIFT

GAIN DRIFT

GAIN DRIFT is a measure of the change in the analog output over temperature expressed in parts per million per °C (ppm/°C). The GAIN DRIFT is determined by testing the end point differences at the high and low temperature extremes and at 25°C for each model, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change.

OFFSET DRIFT

OFFSET DRIFT is a measure of the actual change in output voltage (using an external amplifier) at zero volts output over the specified temperature range. The offset voltage is measured at the temperature extremes, and the maximum change referenced to 25°C is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the time required for the output to enter and remain in an error band equal to ±0.2% of full scale range measured from the time the digital input is changed. Typical settling time values for full scale changes are a function of the load resistor and are shown in the figure below.

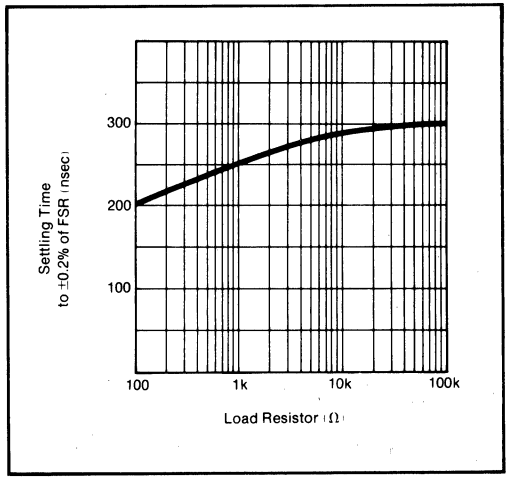


FIGURE 1. Settling Time for FSR Change vs Load.

COMPLIANCE

The COMPLIANCE VOLTAGE of the DAC90 is the maximum voltage swing allowed on the current output in order to maintain the specified accuracy; it is -4.0V to +4.0V for the unipolar and bipolar current ranges. The maximum safe voltage swing allowed with no damage to the DAC90 output is -4.0V to +15.0V.

POWER SUPPLY SENSITIVITY

POWER SUPPLY SENSITIVITY is a measure of the effect of a power supply voltage change on the D/A converter output. It is defined as a percent of FSR/percent of change in either the +15 volt or -15 volt power supplies about the nominal power supply voltages. Figure 2 shows Power Supply Rejection vs Frequency.

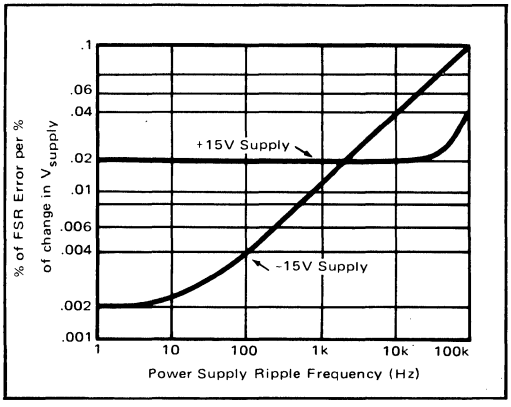


FIGURE 2. Power Supply Rejection vs. Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

DECOUPLING

For best performance and noise rejection, power supply decoupling capacitors should be connected as shown in Figure 3. These capacitors should be located close to the DAC90 and should be tantalum or electrolytic types bypassed with a 0.01 μF ceramic capacitor for best high frequency performance.

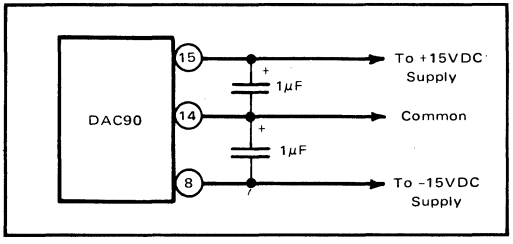


FIGURE 3. Recommended Power Supply Decoupling.

OPERATION IN THE CURRENT OUTPUT MODE

In the current output mode, the DAC90 provides a unipolar output current of 0 to -2mA and a bipolar output current of ±1mA. Refer to Figure 4 and Table II for proper connections. In applications requiring the use of the DAC90 in the current output mode, such as an A/D converter, the internal scaling resistors should be used to generate currents corresponding to analog input voltages.

Output Range	Connect Pin (13) to:
0 to -2mA	N.C.
±1mA	Pin 10

TABLE II. Connections for Current Output Mode.

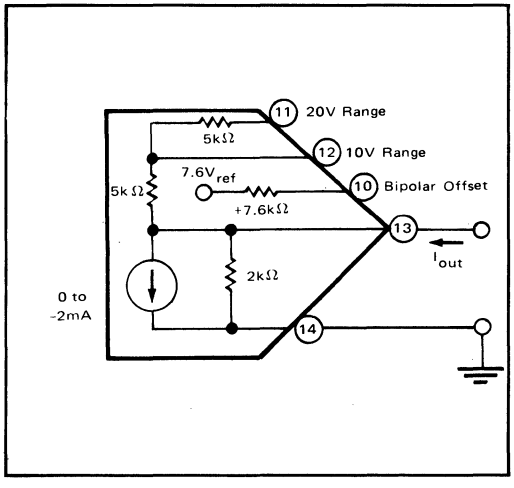


FIGURE 4. Current Output Mode Connection Diagram.

VOLTAGE OUTPUT using an EXTERNAL OP AMP

UNIPOLAR OR BIPOLAR OPERATION

The DAC90 wil drive the summing junction of an op amp (the op amp being used as a current-to-voltage converter) to produce an output voltage.

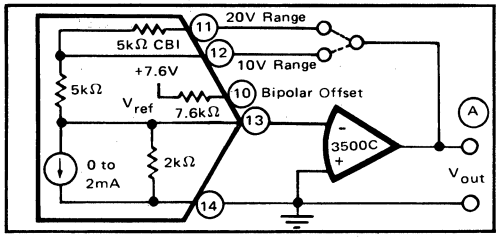


FIGURE 5. External Op Amp Using Internal Feedback Resistors.

$$V_{OUT} = -I \times R_F$$

where I_{OUT} is the DAC90 output current and R_F is the feedback resistor. Refer to Table III and Figure 5.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin (13) to
±10V	COB	11	10
±5V	COB	12	10
±2.5V	COB	12	10,11
0 to +10V	CSB	12	N.C.
0 to +5V	CSB	12	11

TABLE III. Voltage Ranges of Current Output DAC90 With External Op Amp.

EXTERNAL OFFSET and GAIN ADJUSTMENT

Initial offset and gain errors may be trimmed by the user with externally connected OFFSET and GAIN potentiometers and an operational amplifier. Refer to Figures 5 and 6 for proper connections. The adjustment procedures are described below. Potentiometer resistances are shown as a range of values and should have a temperature drift coefficient of 100 ppm/°C or less. The trimming networks should be located as close to the DAC90 as possible to minimize noise pickup. The ceramic capacitor shown in Figure 6 will further reduce noise pickup at the gain adjust point.

OFFSET ADJUSTMENT

Offset adjustment should be made prior to gain adjustment. Connect the unit as shown in Figure 5 for the desired output range and add the offset adjust network shown in Figure 6. Offset adjustment is the same procedure for either bipolar or unipolar operation. Apply the digital input code which should give zero volts output and adjust the offset potentiometer for zero volts output. See Table I for the corresponding codes.

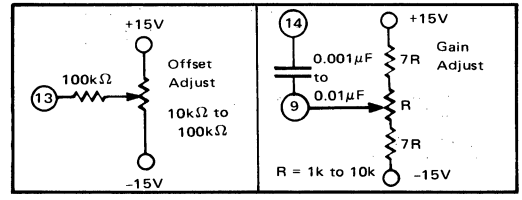


FIGURE 6. Connections for OFFSET and GAIN Adjustment.

GAIN ADJUSTMENT

The gain adjust procedure is the same for either bipolar or unipolar operation. An external amplifier should be connected as shown in Figure 5. Connect the unit for the desired output range and add the gain adjust network shown in Figure 6. Apply the digital input code which should give the maximum positive output voltage and adjust the gain potentiometer for the correct output. Refer to Table I for the corresponding codes.

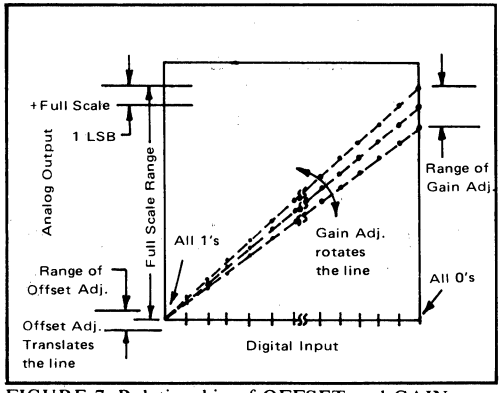


FIGURE 7. Relationship of OFFSET and GAIN Adjustment for a UNIPOLAR D/A Converter.

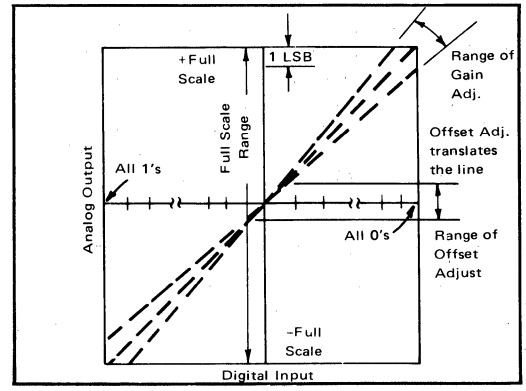
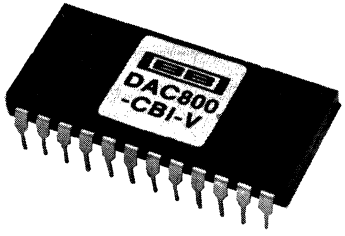


FIGURE 8. Relationship of OFFSET and GAIN Adjustments for BIPOLAR D/A Converter.

BURR-BROWN®

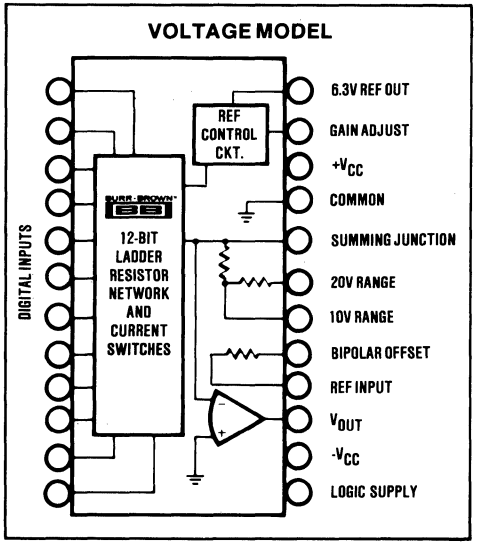


DAC800

Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST HIGH RELIABILITY SINGLE-CHIP REPLACEMENT FOR INDUSTRY-STANDARD DAC80
- 12-BIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY, 0°C TO +70°C
- GUARANTEED MONOTONICITY, 0°C TO +70°C
- DUAL-IN-LINE PACKAGE WITH INDUSTRY-STANDARD (DAC80) PINOUT



DESCRIPTION

The DAC800 is a third-generation monolithic Integrated Circuit that is a pin-for-pin equivalent to the industry-standard DAC80 first introduced by Burr-Brown. It has all of the functions of its predecessor plus faster settling time and enhanced reliability because of its monolithic construction.

The current output model of the DAC800 is a single-chip integrated circuit containing a subsurface zener reference diode, high speed current switches, and laser-trimmed thin-film resistors. The DAC800 provides output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V (V models) or output current ranges of ±1mA or 0 to -2mA (I models).

This high accuracy converter offers a maximum nonlinearity error of ±1/2LSB, ±30ppm/°C maximum gain drift and guaranteed monotonicity, all over 0°C to 70°C. In the bipolar configuration total drift is guaranteed to be less than 25ppm of FSR/°C.

The DAC800 is packaged in a 24-pin dual-in-line package with the popular DAC80 pinout.

For designs that require a wide temperature range and a hermetically sealed package see Burr-Brown models DAC850 and DAC851.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-440

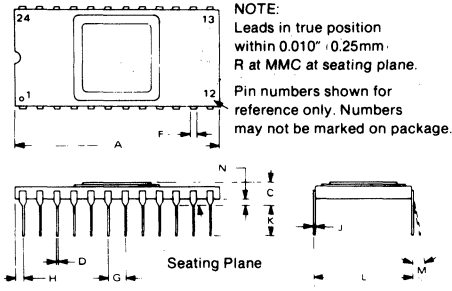
SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	DAC800-CBI			UNITS
	MIN	TYP	MAX	
DIGITAL INPUT				
Resolution			12	
Logic Levels (over spec. temp range)(1)				
V_{IH} (Logic "1")	+2		16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20	µA
I_{IL} (V_{IN} = +0.4V)			-0.36	mA
ACCURACY				
Linearity Error at 25°C		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	+1, -3/4	LSB
Gain Error(2)		±0.1	±0.2	%
Offset Error(2)		±0.05	±0.15	% of FSR(3)
Monotonicity Temp. Range, min	0		+70	°C
DRIFT(4) (0°C to +70°C)				
Bipolar Drift, (±full scale drift for the bipolar connection),		±10	±25	ppm of FSR/°C
Total error over 0°C to +70°C(5)				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.05	±0.12	% of FSR
Gain		±10	±30	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, -7/8	LSB
Linearity Error 0°C to +70°C			±1/2	LSB
CONVERSION SPEED/V models				
Settling Time to ±0.01% of FSR For FSR Change				
20 volt range, 2kΩ load		3	5	µsec
10 volt range, 2kΩ load		2.5	4	µsec
For 1LSB Change, Major Carry, 2kΩ load		1.5		µsec
Slew Rate, 2kΩ load	10	15		V/µsec
CONVERSION SPEED/I models				
Settling Time to ±0.01% of FSR For FSR Change				
10Ω to 100Ω load		300		nsec
1kΩ load		1		µsec
ANALOG OUTPUT/V models				
Ranges	±2.5, ±5, ±10, 0 to +5, 0 to +10			V
Output Current	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit to Common, Duration		Indefinite		
ANALOG OUTPUT/I models				
Ranges - Bipolar	±0.88	±1.175,	±1.47	mA
Unipolar	0 to -1.76	0 to -2.35	0 to -2.94	mA
Output Impedance - Bipolar		3.1		kΩ
Output Impedance - Unipolar		7.2		kΩ
Compliance	-2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
Current (for external loads), Source	1.5	2.5		mA
Tempco of Drift		±10	±30	ppm/°C
POWER SUPPLY SENSITIVITY				
+15V and +5V Supplies		±0.0001	±0.001	% of FSR/% V_{CC}
-15V Supply		±0.003	±0.006	% of FSR/% V_{CC}
POWER SUPPLY REQUIREMENTS				
$\pm V_{CC}$	±13.5	±15	+16.5	VDC
V_{DD}(6)	+4.5	+5.0	+16.5	VDC
Supply Drain				
+15V, -15V (no load		+8, -20	+12, -25	mA
+5V (logic supply)		+7	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	-25		+85	°C
Storage	-60		+100	°C

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	–	10°		10°
N	.025	.060	0.64	1.52

NOTE:
Metal Lid connected to -V_{CC} internally.

CASE: Ceramic
MATING CONNECTOR: 0245MC
WEIGHT: 8.4 grams (0.3oz.)

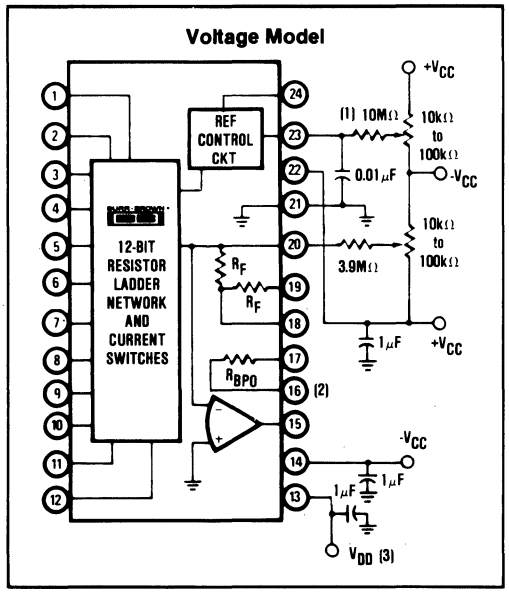
PIN ASSIGNMENTS

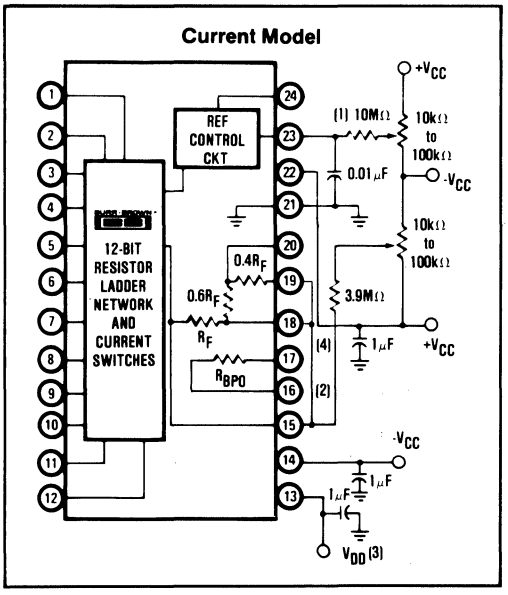
I MODELS	PIN NO.	V MODELS
MSB BIT 1	1	BIT 1 MSB
BIT 2	2	BIT 2
BIT 3	3	BIT 3
BIT 4	4	BIT 4
BIT 5	5	BIT 5
BIT 6	6	BIT 6
BIT 7	7	BIT 7
BIT 8	8	BIT 8
BIT 9	9	BIT 9
BIT 10	10	BIT 10
BIT 11	11	BIT 11
LSB BIT 12	12	BIT 12 LSB
LOGIC SUPPLY, V_{DD}	13	LOGIC SUPPLY, V_{DD}
-V_{CC}	14	-V_{CC}
I_{OUT}	15	V_{OUT}
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
+V_{CC}	22	+V_{CC}
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

NOTES:

1. Refer to Logic Input Compatibility section.
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
4. To maintain drift spec internal feedback resistors must be used for current output models.
5. Includes the effects of gain, offset and linearity drift. Gain and offset errors are adjusted to zero at +25°C.
6. Power dissipation is an additional 100mW, max, when V_{DD} is operated at +15V.

CONNECTION DIAGRAMS





NOTES:

1. DAC80 which may be replaced by DAC800 requires a 33MΩ resistor. DAC800 requires a 10MΩ resistor. DAC80's may also be operated with a 10MΩ resistor resulting in increased trim range.
2. Pin 16 of DAC800 is used only to connect the bipolar offset resistor. An external reference voltage may not be used with DAC800 as is possible with DAC80.
3. If connected to +VCC, which is permissible, power dissipation increases 75mW typ, 100mW max.
4. For fastest settling time connect pins 19, 18, and 15 together.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC800 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes; CSB, CTC, or COB.

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-1LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	1/2 Full Scale -1LSB	-1LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC800 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC800 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain Drift is established by: 1) testing the end point differences for each DAC800 model at 0°C, +25°C and +70°C; 2) calculating the gain change with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C.

Offset Drift is a measure of the change in output with all "1"s on the inputs over the specified temperature range. The Offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

Bipolar Drift is a measure of the change in plus or minus full scale output over the specification temperature range for the bipolar connection. Because Bipolar Offset Drift and Gain Drift have canceling interactions, Bipolar Drift is not simply the sum of the two. Total bipolar error over temperature is calculated using Bipolar Drift, then adding ±1/2LSB of linearity error.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

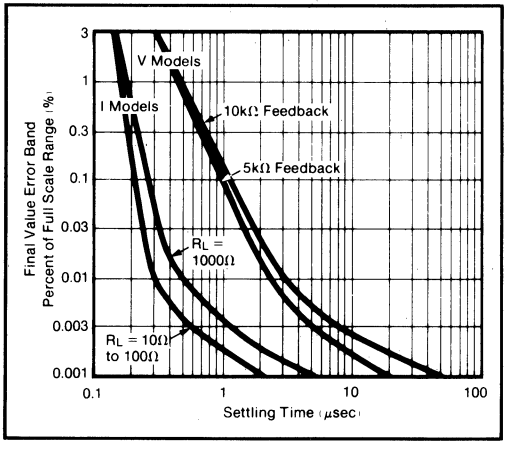


FIGURE 1. Full Scale Range Settling Time vs Final Value Error Band.

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω. Internal resistors are provided for connecting a nominal load resistance of approximately 1000Ω for output voltage ranges of ±1V and 0 to -2V.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is -2.5V to +2.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

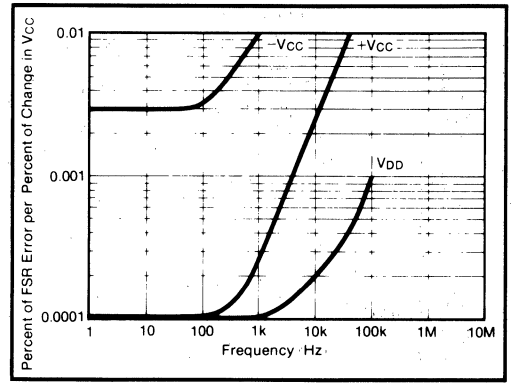


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC800 models have an on-chip +6.3 volt reference. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. Pin 16 is used only to connect the bipolar offset resistor. An external reference may not be used with DAC800. See Connection Diagrams. The reference voltage may be used to supply external circuits with 2.5mA of current in addition to the 1mA required by the bipolar offset circuit.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC800. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance. The metal lid on the top of the package is connected internally to -V_{CC}.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20%

carbon or better) should be located close to the DAC800 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. The Gain

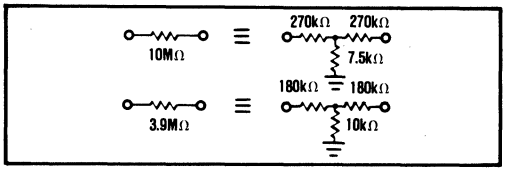


FIGURE 3. Equivalent Resistances.

Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to reduce noise pickup. Figures 4 and 5 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

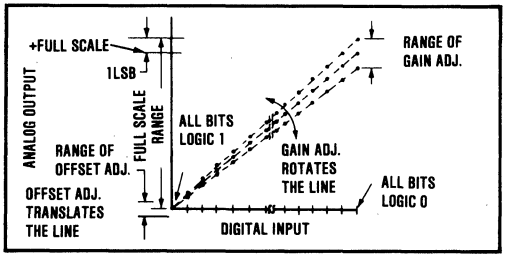


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

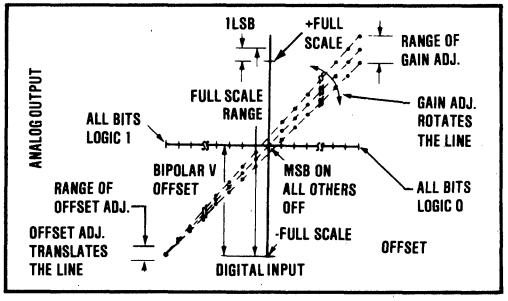


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

VOLTAGE OUTPUT MODEL

Output Range Connections

Internal scaling resistors provided in the DAC800 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full scale range change is specified as 3μsec for the 20 volt range and 2.5μsec for the 10 volt range.

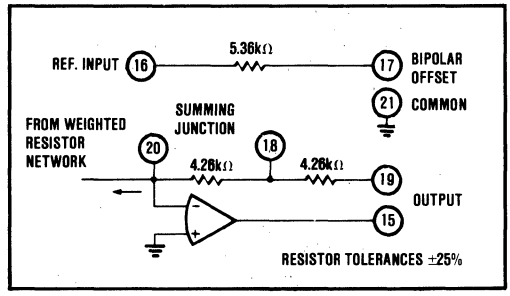


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE II. Digital Input / Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE*		CURRENT	
	0 to +10V	±10V	0 to -2mA	±1mA
12-Bit Resolution MSB LSB				
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges: 0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE III. Output Voltage Range Connections - Voltage Model DAC800.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODEL

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8. It is important to note

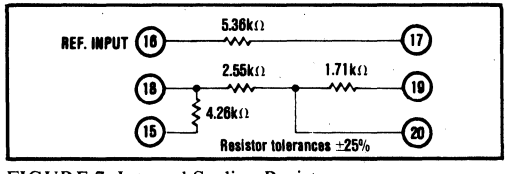


FIGURE 7. Internal Scaling Resistors.

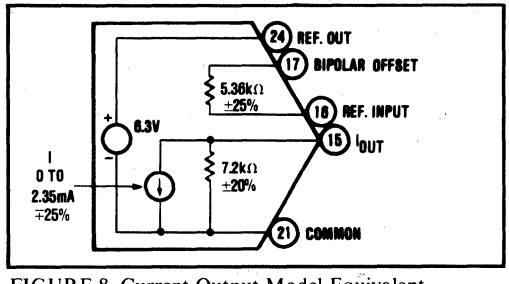


FIGURE 8. Current Output Model Equivalent Output Circuit.

that there is a relationship between the tolerances of the current source and the scaling resistors. The magnitude of the tolerance tracks very closely but with opposite sign. The tolerance of the internal resistance of the converter (7.2kΩ unipolar, 3.07kΩ bipolar) tracks the tolerance of the scaling resistors in sign and approximately proportionately in magnitude. That is, if the scaling resistors are high by 10%, the internal impedance is high by about 8%. An external resistor is required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the DAC800 output specifications. If exact output ranges are not required, the external resistors are not needed.

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors are an integral part of the DAC800 and maintain gain and bipolar offset drift specifications.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2.35mA \left(\frac{R_L \times 7.2k\Omega}{R_L + 7.2k\Omega} \right)$$

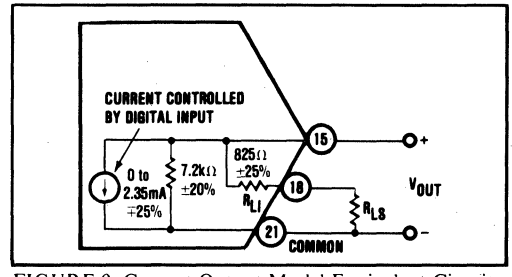


FIGURE 9. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift. Tolerances on internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 10, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1.175mA \left(\frac{R_L \times 3.07k\Omega}{R_L + 3.07k\Omega} \right)$$

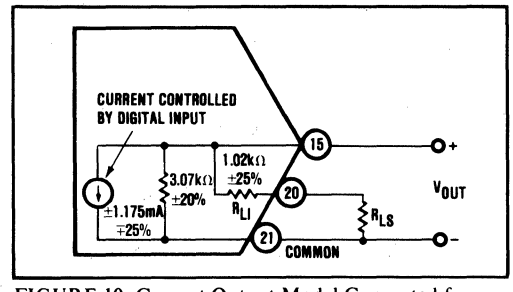


FIGURE 10. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

To achieve specified drift, connect 1.71kΩ and 2.55kΩ internal scaling resistors in parallel (R_{LI}) and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. The tolerances on the internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving An External Op Amp

The current output model DAC800 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 11.

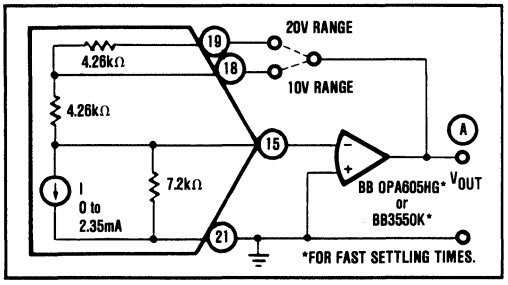


FIGURE 11. External Op Amp - Using Internal Feedback Resistors.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC800 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model DAC800 provides output voltage ranges the same as the voltage model DAC800. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

TABLE IV. Voltage Range of Current Output DAC800.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1.175mA ±25% for bipolar voltage ranges and -2.35mA ±25% for unipolar voltage ranges. See Figure 12. Use protection diodes when a high voltage op amp is used.

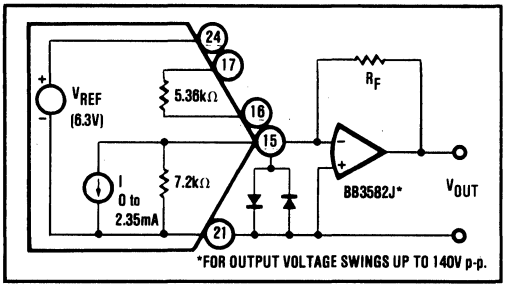


FIGURE 12. External Op Amp - Using External Feedback Resistors.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

LOGIC INPUT COMPATIBILITY

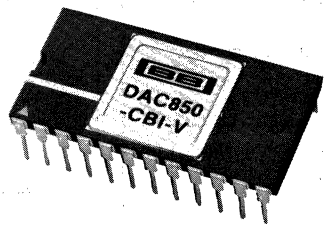
DAC800 digital inputs are TTL, LSTTL and 54/74HC CMOS compatible over the operating range of V_{DD}, +5 to +15 volts. The input switching threshold remains at the TTL threshold over supply range of V_{DD}, +5 to +15V.

Logic "0" input current over temperture is low enough to permit driving DAC800 directly from outputs of 4000B and 54/74C CMOS devices over the logic power supply range of +5 to +15 volts.

ORDERING INFORMATION

DAC800	-XXX	-X
Low Cost 12-Bit D A Converter Family	INPUT CODE	OUTPUT
Example: DAC800-CBI-V	CBI = Complementary Binary	V = Voltage
Complementary Binary DAC800 with voltage output		I = Current

BURR-BROWN®

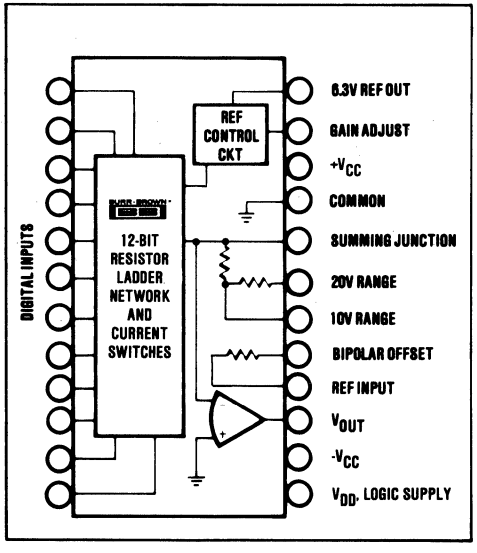


DAC850
DAC851

Integrated Circuit
DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW COST HIGH RELIABILITY SINGLE-CHIP REPLACEMENT FOR DAC85 AND DAC87
- 12-BIT RESOLUTION
- HIGH ACCURACY
  ±1/2LSB max nonlinearity -25°C to +85°C (DAC850)
  -55°C to +125°C (DAC851)
- GUARANTEED MONOTONICITY
- DUAL-IN-LINE HERMETIC PACKAGE WITH SIDE-BRAZED PINS



DESCRIPTION

The DAC850 and DAC851 are 12-bit single-chip (current output model) digital-to-analog converters for use in wide temperature high reliability applications.

The DAC850 and DAC851 are packaged in a hermetically-sealed package with side-brazed pins. The DAC850 is specified with a linearity error of ±1/2LSB over -25°C to +85°C and the DAC851 has a linearity error of ±1/2LSB over -55°C to +125°C. Both converters have guaranteed monotonicity over their specification temperature range. The current output configuration of these D/A converters is a single-chip integrated circuit containing a subsurface zener reference diode, high-speed current switches, and laser-trimmed thin-film resistors.

The DAC850 and DAC851 provide output voltage ranges of ±2.5V, ±5V, ±10V, 0 to +5 and 0 to +10V (V models) or output current ranges of ±1.175mA or 0 to -2.35mA (I models).

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PDS-453

SPECIFICATIONS

ELECTRICAL

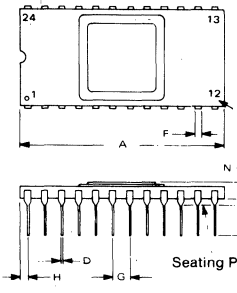
At 25°C and rated power supplies unless otherwise noted.

MODEL	DAC850-CBI MIN	DAC850-CBI TYP	DAC850-CBI MAX	DAC851-CBI MIN	DAC851-CBI TYP	DAC851-CBI MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution			12			12	Bits
Logic Levels (LSTTL Compatible)(1)							
Logic "1" (at +20μA)	+2		+5.5	+2		+5.5	VDC
Logic "0" (at -0.36mA)	0		+0.8	0		+0.8	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error		±1/4	±1/2		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	+1, -3/4		±1/2	+1, -3/4	LSB
Gain Error(2)		±0.1	±0.2		±0.1	±0.2	%
Offset Error(2)		±0.05	±0.15		±0.05	±0.15	% of FSR(3)
Monotonicity Temp. Range, min	-25		+85	-55		+125	°C
DRIFT(4) (over spec. temp. range)							
Bipolar Drift (±full scale drift for the bipolar connection)		±5	±17		±15	±30	ppm of FSR/°C
Total Error(5)							
Unipolar		±0.1	±0.20		±0.15	±0.30	% of FSR
Bipolar		±0.06	±0.12		±0.15	±0.30	% of FSR
Gain		±10	±20		±10	±25	ppm/°C
Offset, Unipolar		±1	±3		±1	±3	ppm of FSR/°C
Bipolar		±5	±10		±5	±15	ppm of FSR/°C
Differential Linearity (over spec. temp. range)		±1/2	±1		±1/2	±1	LSB
Linearity Error (over spec. temp. range)			±1/2			±1/2	LSB
CONVERSION SPEED							
V Model (settling time to ±0.01% of FSR)							
For FSR Change, 20V Range, 2kΩ Load		3	5		3	5	μsec
10V Range, 2kΩ Load		2.5	4		2.5	4	μsec
For 1LSB Change, Major Carry, 2kΩ Load		1.5			1.5		μsec
Slew Rate, 2kΩ Load	10	15		10	15		V/μsec
I Model (settling time to ±0.01% of FSR)							
For FSR Change, 10Ω to 100Ω Load		300			300		nsec
1kΩLoad		1			1		μsec
OUTPUT							
ANALOG OUTPUT							
V Model							
Ranges	±2.5, ±5, ±10, 0 to +5, 0 to +10			±2.5, ±5, ±10, 0 to +5, 0 to +10			V
Output Current	±5			±5			mA
Output Impedance (DC)		0.05			0.05		Ω
Short Circuit to Common, Duration	Indefinite						
I Model							
Ranges		±1.175, 0 to -2.35			±1.175, 0 to -2.35		mA
Output Impedance, Bipolar	2.5	3.1	3.7	2.5	3.1	3.7	kΩ
Unipolar	5.8	7.2	8.6	5.8	7.2	8.6	kΩ
Compliance	-2.5		+2.5	-2.5		+2.5	V
POWER SUPPLIES AND REFERENCE							
Reference Voltage Output	+6.23	+6.3	+6.37	+6.23	+6.3	+6.37	V
Current (for external loads), Source	1.5	2.5		1.5	2.5		mA
Temperature Coefficient of Drift		±10	±20		±10	±25	ppm/°C
Power Supply Sensitivity							
+15V and +5V Supplies		±0.0001	±0.001		±0.0001	±0.001	% of FSR/%V_{CC}
-15V Supply		±0.003	±0.006		±0.003	±0.006	% of FSR/%V_{CC}
Power Supply Requirements							
$\pm V_{CC}$	±13.5	±15	±16.5	±13.5	±15	±16.5	VDC
V_{DD}(6)	+4.5	+5	+16.5	+4.5	+5	+16.5	VDC
Power Supply Drain							
$\pm V_{CC}$ (no load)		+8, -20	+12, -25		+8, -20	+12, -25	mA
V_{DD} (logic supply)		+7	+10		+7	+10	mA
PHYSICAL CHARACTERISTICS							
TEMPERATURE RANGE							
Specification	-25		+85	-55		+125	°C
Storage	-60		+150	-60		+150	°C
PACKAGE	24-pin hermetic DIP side-brazed ceramic						

NOTES:

1. Adding external CMOS hex buffers CD 4049A/4050A will provide CMOS input compatibility. Refer to Logic Input Compatibility section.
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
4. To maintain drift spec internal feedback resistors must be used for current output models.
5. Includes the effects of gain, offset and linearity drift. Gain and offset errors are adjusted to zero at +25°C.
6. Power dissipation is an additional 100mW, max, when V_{DD} is operated at +15V.

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.185	1.215	30.10	30.86
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°		10°
N	.025	.060	0.64	1.52

NOTE:
Metal Cap connected to -V_{CC} internally.

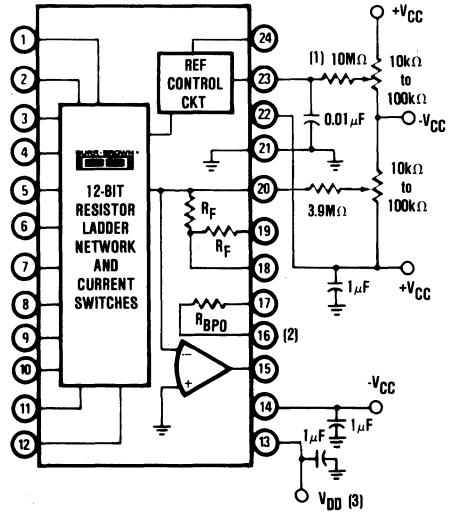
CASE: Ceramic
MATING CONNECTOR: 0245MC
WEIGHT: 8.4 grams (0.3oz.)

PIN ASSIGNMENTS

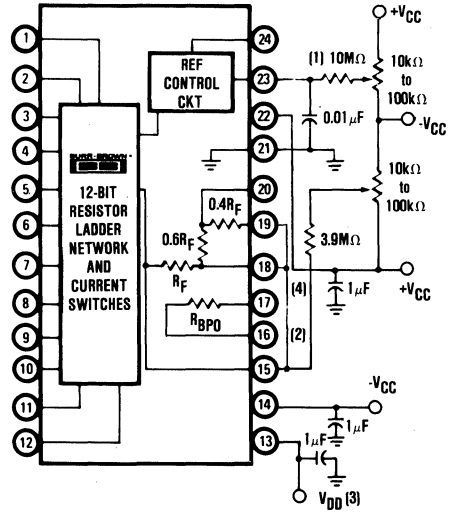
I MODELS	PIN NO.	V MODELS
(MSB) BIT 1	1	BIT 1 (MSB)
BIT 2	2	BIT 2
BIT 3	3	BIT 3
BIT 4	4	BIT 4
BIT 5	5	BIT 5
BIT 6	6	BIT 6
BIT 7	7	BIT 7
BIT 8	8	BIT 8
BIT 9	9	BIT 9
BIT 10	10	BIT 10
BIT 11	11	BIT 11
(LSB) BIT 12	12	BIT 12 (LSB)
LOGIC SUPPLY, V_{DD}	13	LOGIC SUPPLY, V_{DD}
-V_{CC}	14	-V_{CC}
I_{OUT}	15	V_{OUT}
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
+V_{CC}	22	+V_{CC}
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

CONNECTION DIAGRAMS

Voltage Model



Current Model



NOTES:

1. **DAC850/851 use a 10MΩ resistor. These models can replace the DAC85 which uses an 18MΩ resistor and the DAC87 which uses a 33MΩ resistor.**
2. **Pin 16 of DAC850/851 is used only to connect the bipolar offset resistor. An external reference voltage may not be used with DAC850/851.**
3. **If connected to +V_{CC}, which is permissible, power dissipation increases 75mW typ., 100mW max.**
4. **For fastest settling time connect pins 19, 18, and 15 together.**

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC850 and DAC851 accept complementary binary digital input codes. They may be connected by the user for any one of three complementary codes; CSB, CTC, or COB (see Table I).

TABLE I. Digital Input Codes.

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
000000000000	+Full Scale	+Full Scale	-LSB
011111111111	+1/2 Full Scale	Zero	-Full Scale
100000000000	Midscale -1LSB	-1LSB	+Full Scale
111111111111	Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specification temperature range is guaranteed to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences at -25°C, +25°C, and +85°C for the DAC850 and at -55°C, +25°C, and +125°C for the DAC851; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This is expressed in ppm/°C.

Offset drift is a measure of the actual change in output with all "1"s on the input over the specification temperature range. The offset is measured at -25°C, +25°C, and +85°C for the DAC850 and at -55°C, +25°C, and +125°C for the DAC851. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

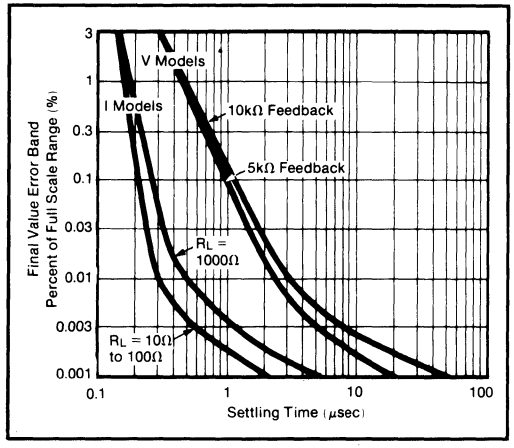


FIGURE 1. Full Scale Range Settling Time vs Final Value Error Band.

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω. Internal resistors are provided for connecting a nominal load resistance of approximately 1000Ω for output voltage ranges of ±1V and 0 to -2V.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is +2.5V to -2.5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

REFERENCE SUPPLY

All models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also. The external current drain is limited to sourcing 2.5mA up to +85°C and 1mA up to +125°C not including current required by the bipolar offset circuit.

An external buffer amplifier is recommended if this reference will be used to drive other system components because variations in a load driven from the reference will result in bipolar offset variations of the D/A converter. Gain and bipolar offset adjustments should be made under constant load conditions.

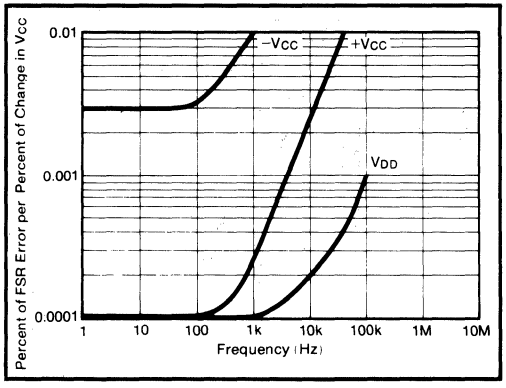


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the case. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance. The metal cap on the top of the package is connected internally to -V_{CC}.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the case to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. Figures 4 and 5 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

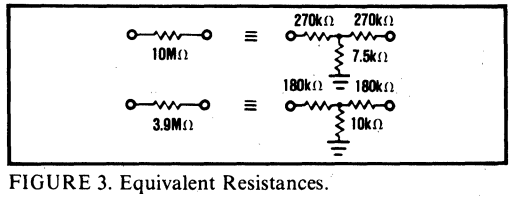


FIGURE 3. Equivalent Resistances.

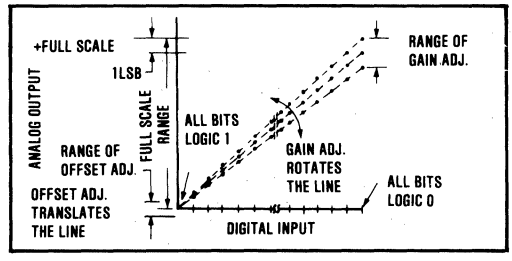


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

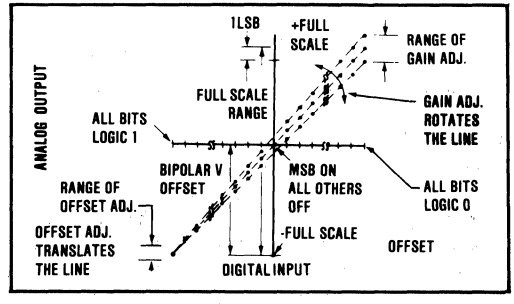


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

Offset Adjustment: For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full scale voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections.

TABLE II. Digital Input/Analog Output.

DIGITAL INPUT	ANALOG OUTPUT			
	VOLTAGE*		CURRENT	
MSB ↓ LSB ↓	0 to +10V	±10V	0 to -2mA	±1mA
000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
011111111111†	+5.0000V	0.0000V	-1.0000mA	0.0000mA
100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488μA	0.488μA

*To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC850 may be connected to produce bipolar output voltage ranges of ±10V, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

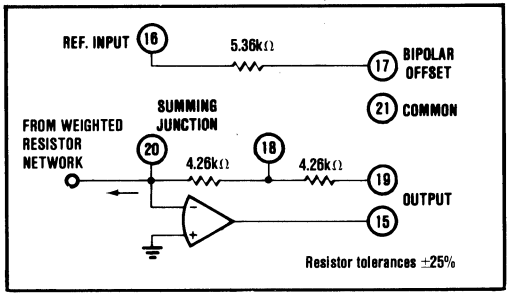


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full scale range change is specified as 3μsec for the 20 volt range and 2.5μsec for the 10 volt range.

TABLE III. Output Voltage Range Connections - Voltage Model.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

CURRENT OUTPUT MODELS

The equivalent output circuit and resistive scaling network of the current model differ from the voltage model and are shown in Figures 7 and 8.

An external R_{LS} resistor is required to produce exactly 0 to -2V or ±1V output. TCR of this resistor should be ±100ppm/°C or less to maintain the output specifications. If exact output ranges are not required, the external resistor is not needed.

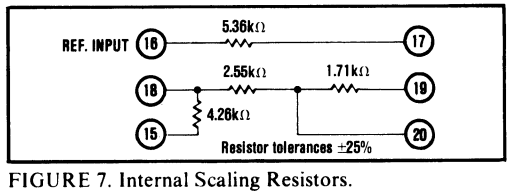


FIGURE 7. Internal Scaling Resistors.

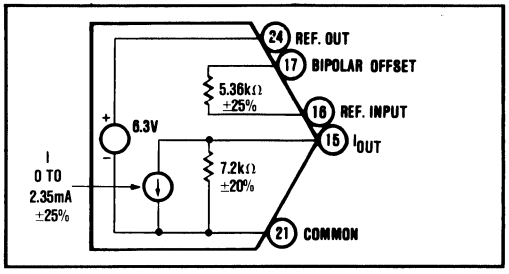


FIGURE 8. Current Output Model Equivalent Output Current.

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the DAC850/851 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2.35mA \left(\frac{R_L \times 7.2k\Omega}{R_L + 7.2k\Omega} \right)$$

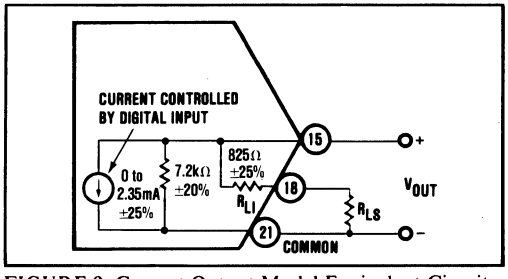


FIGURE 9. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. Tolerances on internal equivalent resistors are wide. R_{LS} will have to be selected for each unit.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 10, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1.175mA\left(\frac{R_L \times 3.17k\Omega}{R_L + 3.17k\Omega}\right)$$

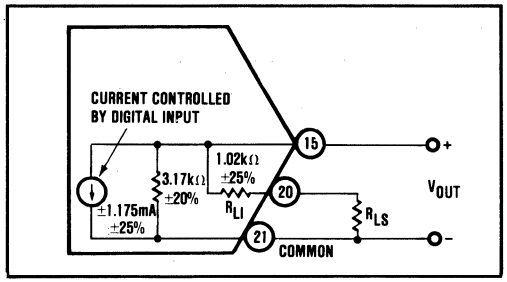


FIGURE 10. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

To achieve specified drift, connect the 1.71kΩ and 2.55kΩ internal scaling resistors in parallel (R_{LI}) and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. The tolerances on the equivalent internal resistors are wide. R_{LS} will have to be selected for each unit.

Driving An External Op Amp

The current output model will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage (see Figure 11).

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the output current and R_F is the feedback resistor. Using the internal feedback resistors of the current output model provides output voltage ranges the same as the voltage model. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

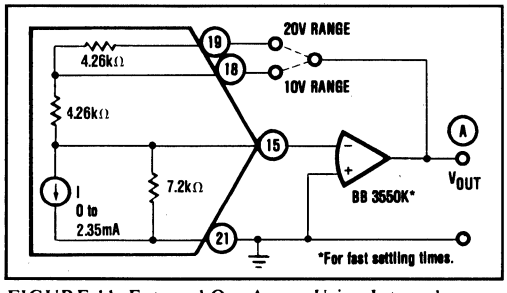


FIGURE 11. External Op Amp - Using Internal Feedback Resistors.

TABLE IV. Voltage Range of Current Output D/A Converter.

Output Range	Digital Input Codes	Connect (A) to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	(A)	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1.175mA for bipolar voltage ranges and -2.35mA for unipolar voltage ranges (see Figure 12). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.

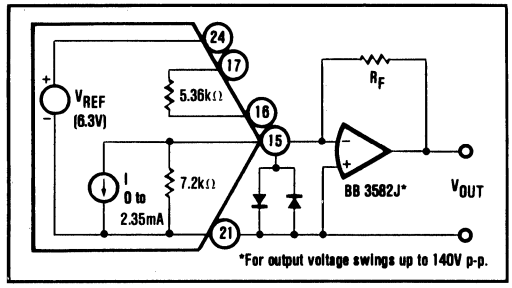


FIGURE 12. External Op Amp - Using External Feedback Resistors.

LOGIC INPUT COMPATIBILITY

DAC850 and DAC851 digital inputs are LSTTL compatible as shown in the specification table when V_{DD} is operated over 4.5 to 16.5 volts.

Figure 13 illustrates using CMOS hex buffers with DAC850 to provide CMOS input compatibility. This combination will operate together over a wide range of logic power supply voltages.

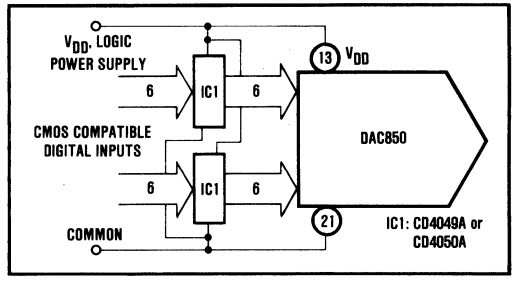
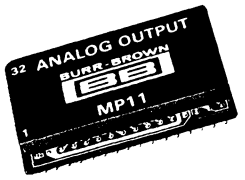


FIGURE 13. Using DAC850/851 with CMOS Hex Buffers Over a Wide Range of Logic Power Supply Voltages.

ORDERING INFORMATION

DAC850 DAC851	-XXX -XXX	-X -X
D/A Converter Family Example: DAC851-CBI-V	Input Code CBI= Complimentary 12-Bit Binary	Output V = Voltage I = Current

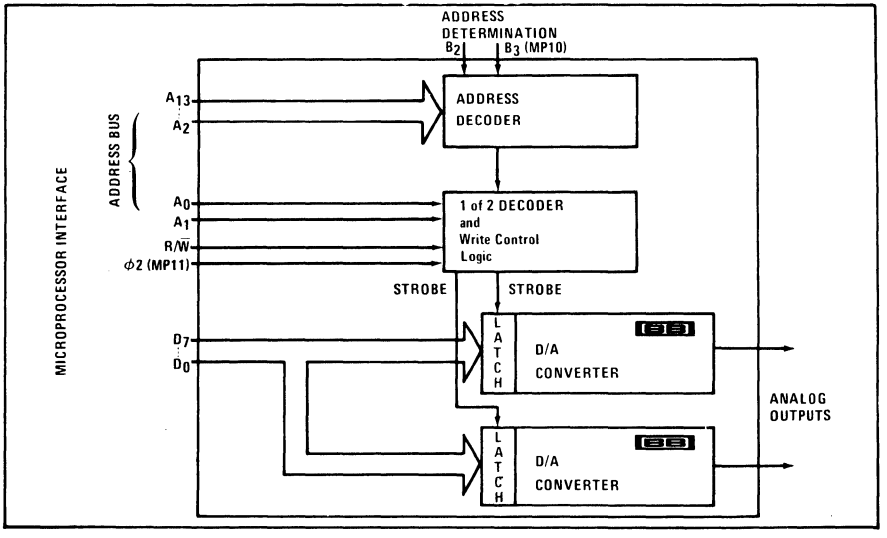
BURR-BROWN®



MP10
MP11

Microprocessor-Interfaced 8-BIT ANALOG OUTPUT SYSTEM

MP10, MP11 BLOCK DIAGRAM



FEATURES

- USE AS ANALOG INPUT AND OUTPUT
- EASY TO USE
  - Completely compatible with most microprocessors
  - No external logic required
  - Timing compatible
  - Memory-mapped
- SAVES DEVELOPMENT MONEY AND TIME
- COMPLETELY SELF-CONTAINED
- COMPATIBLE WITH:
  - 8080 (Intel)
  - 9080A (AMD)
  - Z-80 (Zilog)
  - 6800 (Motorola)
  - 8008 (Intel)
  - F-8 (Fairchild)
  - SC/MP (National)
  - 650X (MOS Technology)

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-363A

DESCRIPTION

These microprocessor peripherals provide an analog interface compatible with most microprocessors. The MP10 and MP11 are electrically and functionally microprocessor-compatible in static or dynamic situations.

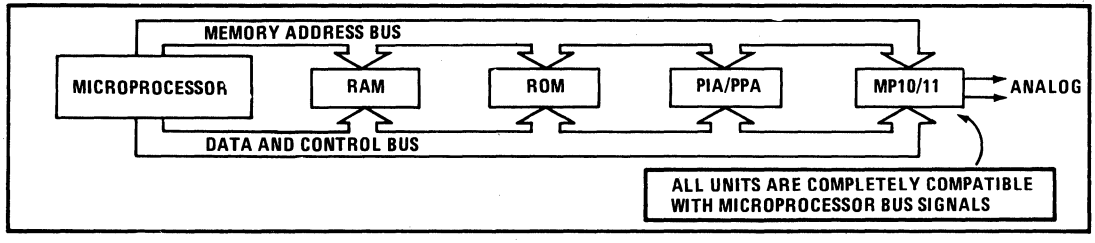
These units are complete analog systems packaged in 32-pin triple-wide dual-in-line packages. They contain two 8-bit D/A converters which are internally trimmed for gain and offset so that no external trimming is required. All necessary interface, timing and address decoding logic is also included.

The MP10 is designed to be used with 8080A and 8008 type microprocessors. It can be used with SC/MP if pull-up resistors are added to the address bus, with the F-8 Dynamic or Static memory interface chip if the RAM WRITE signal is a minimum of 430nsec and with the Z-80 if t_w (ϕH) = t_w (ϕL) = 500nsec. The MP11 is designed to be used with 6800 and 650X type microprocessors.

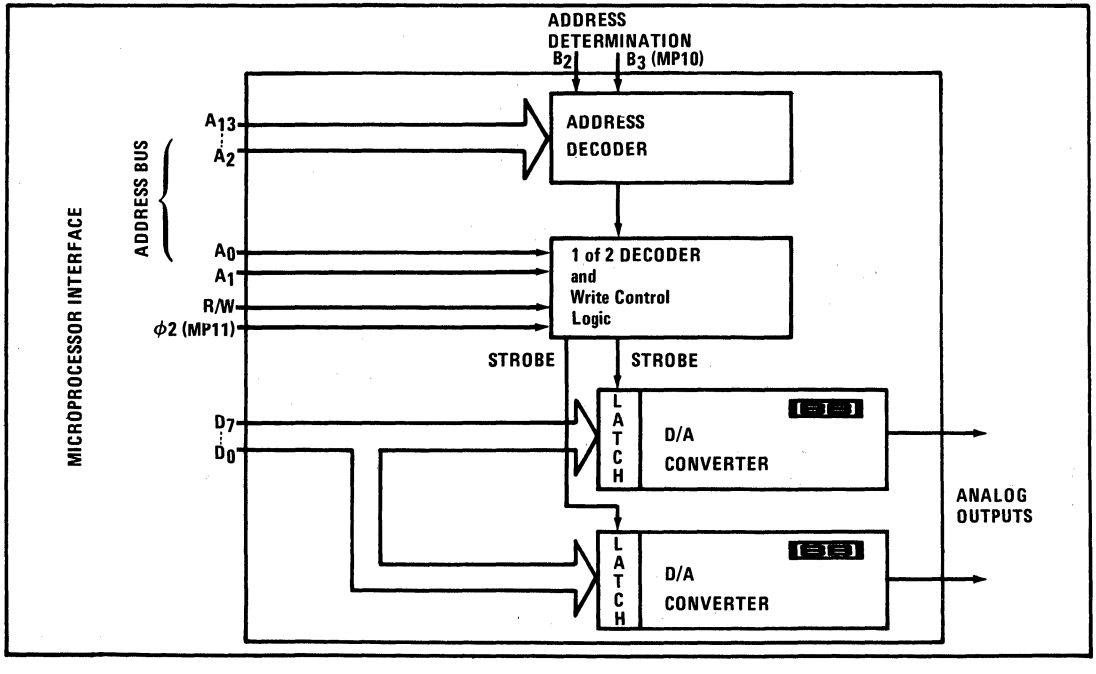
The address lines A_2 through A_{13}, B_2 and B_3 of the MP10 are CMOS compatible so that they can be directly connected to the address bus of an 8080 or 8008. All other input lines require standard TTL voltages. The address lines A_2 through A_{13} and B_2 of the MP11 are LSTTL compatible so they can be directly connected to the address bus of a 6800 or 650X. All other input lines require standard TTL voltages but are high impedance and require only microamp drive currents.

THEORY OF OPERATION

When programming these peripherals, the user treats them as memory. Because the D/A converter input is an 8 bit word, one 8 bit memory location is required for each channel. Since these units are treated as memory, a single instruction is all that's needed to write to an output channel. For instance, when the MP10 is used with an 8080, a single instruction, SHLD, can be used to output data to both D/A converter channels from the H and L register pair. Likewise, when the MP11 is used with the 6800 or 650X, a single STX instruction can be used to output data to both D/A converter channels from the index register. The MP10 and the MP11 require an initialization as would any programmable peripheral.



MP10, MP11 BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

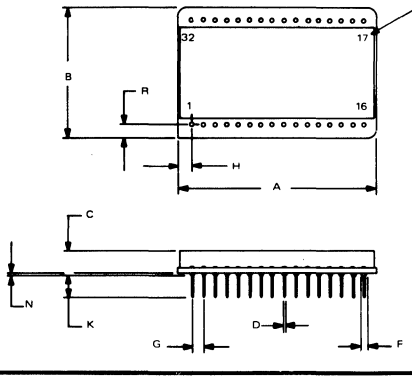
(Typical at 25°C and rated supplies unless otherwise noted.)

	MP10/MP11
ANALOG OUTPUT	
Number of analog outputs	2
Output voltage range	±10V
Output impedance	1Ω
Output settling time	25μsec
TRANSFER CHARACTERISTICS	
Resolution	8 bit binary (complementary binary)
One LSB	78.1mV
Throughput accuracy (max)	±0.4% FSR[1,2]
Throughput accuracy (typical)	±0.25% FSR
Temperature coefficient of accuracy	±0.008% FSR/°C

	MP10/MP11
DIGITAL INPUT/OUTPUT	
All signals compatible with the microprocessor bus	
An analog output channel selected by:	A0
Input data bits read by:	D0 - D7
POWER REQUIREMENTS	
	+5VDC ±5% at 90 mA +15V ±3% at 30 mA -15V ±3% at 30 mA
TEMPERATURE RANGE	
Operating temperature range	0°C to 70°C
Storage temperature range	-55°C to +85°C

1. FSR is Full Scale Range = 20V.
2. Accuracy components are: Linearity Error = ±0.2% FSR; Gain Error = ±0.1% FSR, Offset Error = ±0.1% FSR.

MECHANICAL SPECIFICATIONS



NOTE:
LEADS IN TRUE POSITION WITHIN
.010" (.25mm) R @ MMC AT SEATING PLANE.

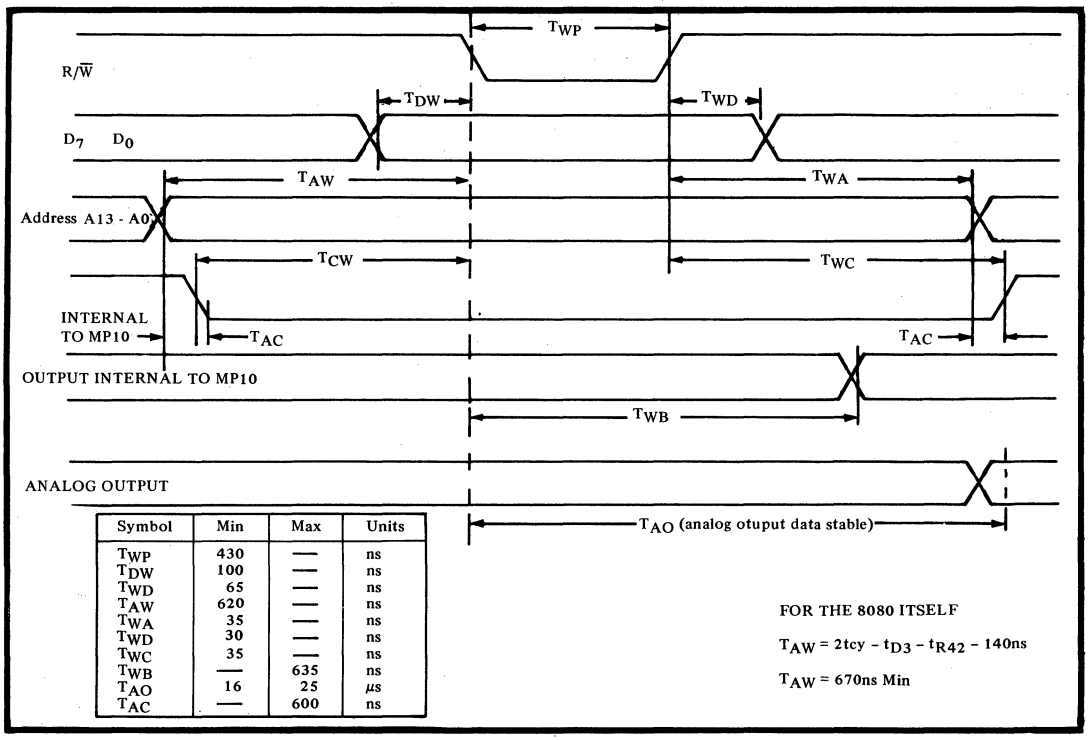
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

MATERIAL: Ceramic
WEIGHT: 14 grams (0.5 oz)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
MATING CONNECTOR: 2302MC (Set of two, 16-pin strips)

PIN CONNECTIONS

8080 Pin Connections					8080 Pin Connections
1	1	A10	A11	32	40
2	2	Common	A13	31	38
3	3	D4	A12	30	37
4	4	D5	A 9	29	35
5	5	D6	A 8	28	34
6	6	D7	A 7	27	33
7	7	D3	A 6	26	32
8	8	D2	A 5	25	31
9	9	D1 MP10	A 4	24	30
10	10	D0	A 3	23	29
12	11	Reset	A 2	22	27
18	12	R/$\overline{W}$	B 2	21	—
26	13	A1	B 3	20	—
25	14	A0	+5V	19	20
—	15	+15VDC	Out 1	18	—
—	16	-15VDC	Out 2	17	—

6800 Pin Connections					6800 Pin Connections
—	1	Output 1	-15VDC	32	—
—	2	Output 2	+15VDC	31	—
8	3	+5VDC	R/$\overline{W}$	30	34
37	4	Enable	$\overline{Reset}$	29	40
9	5	A0	D0	28	33
10	6	A1	D1	27	32
11	7	A2	D2	26	31
12	8	A3	D3	25	30
13	9	A4 MP11	D4	24	29
14	10	A5	D5	23	28
15	11	A6	D6	22	27
16	12	A7	D7	21	26
17	13	A8	Common	20	21
18	14	A9	B2	19	—
19	15	A10	A13	18	23
20	16	A11	A12	17	22



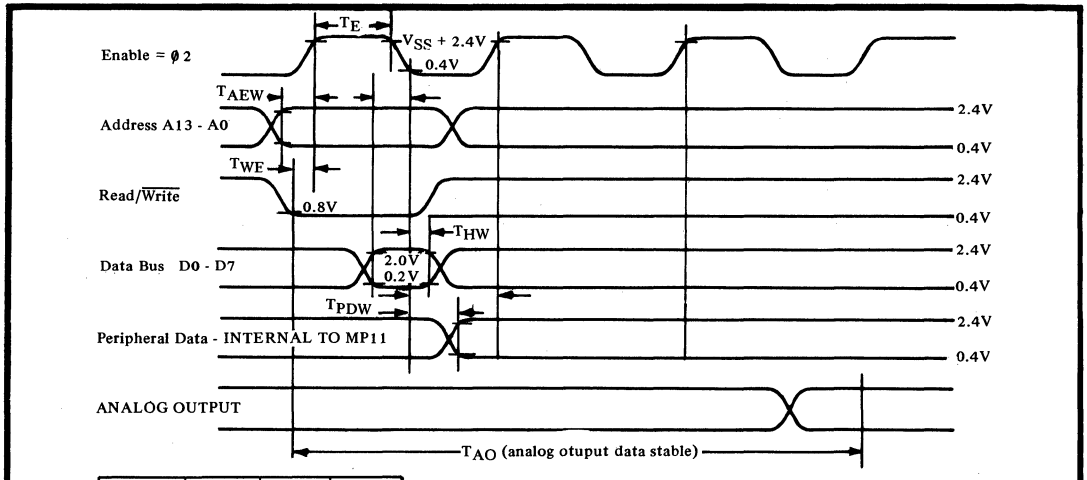
Symbol	Min	Max	Units
T_{WP}	430	—	ns
T_{DW}	100	—	ns
T_{WD}	65	—	ns
T_{AW}	620	—	ns
T_{WA}	35	—	ns
T_{WD}	30	—	ns
T_{WC}	35	—	ns
T_{WB}	—	635	ns
T_{AO}	16	25	μs
T_{AC}	—	600	ns

FOR THE 8080 ITSELF

$T_{AW} = 2tcy - t_{D3} - t_{R42} - 140ns$

$T_{AW} = 670ns$ Min

FIGURE 1. MP10 Timing Diagram.



Symbol	Min	Max	Unit
T_E	0.450	25	μs
T_{AEW}	180	—	ns
T_{DSU}	300	—	ns
T_{WE}	130	—	ns
T_{HW}	10	—	ns
T_{PDW}	—	1.0	μs
T_{AO}	17	25	μs

FIGURE 2. MP11 Timing Diagram.

PROGRAMMING

These units are easily programmed since all are treated as memory locations. They use any memory reference instruction that can write data from internal registers or the accumulator. A single instruction can be used to write data to one or both channels. When the MP10 is used with an 8080, a single SHLD instruction referenced to the lower of the two addresses will automatically transfer the data in the H register to DAC1 and the data in the L register to DAC2. An STA instruction will transfer the data in the accumulator to either DAC. When the MP11 is used with a 6800, a single STX instruction referenced to the lower of the two addresses will automatically transfer the eight upper bits of the index register to DAC1 and the eight lower bits to DAC2. An STAA instruction will transfer the contents of the accumulator to either DAC. Of course, if direct addressing is not desired, MOV instructions may be used to transfer data from internal registers to a specific DAC memory location. As with any programmable peripheral, the MP10 and MP11 must be initialized.

MP10 INITIALIZATION

The RESET input controls the status of the control register of the MP10. An active high on this line will reset the control register to all "zeros".

The MP10 will require initialization every time RESET is activated. If RESET is connected to ground, the MP10 must be initialized only once before output of the data.

MP10 INITIALIZATION SEQUENCE:

1. Load initialization address
2. Load initialization data

MP10 INITIALIZATION ADDRESS:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	1	1	1	1	1	1	1	1	1	1	a	a	1	1
												User Defined			

X = don't care, not connected to MP10
1 = True

MP10 INITIALIZATION DATA

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	0	0	$= 80_{16}$

For 8080 the sequence may look as follows:

LXI H, ADDR; ADDR = Initialization address
Loads H & L registers with initialization address

MVI M, DATA; DATA = 80
Loads initialization data (80_{16}) to initialization address

The initialization sequence assigns internal registers to function as input registers for the D/A converters. Now data can be written into the MP10. This is accomplished by outputting the correct MP10 address:

A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	1	1	1	1	1	1	a	a	0	0	
										User Defined				OUTPUT 1
1	1	1	1	1	1	1	1	1	1	a	a	0	1	
										User Defined				OUTPUT 2

The B_2 and B_3 inputs determine the address to which the MP10 will respond. The four memory locations which are possible are outlined below:

B_2	B_3	A_2	A_3
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

At the time that the address appears on the address bus, data will appear on the data bus and a R/$\overline{W}$ pulse will be generated by the microprocessor. After 25μsec, the analog voltage will be stable at the selected output. Timing requirements shown in Figure 1 must be satisfied in order for the MP10 to be initialized and operate correctly. These timing requirements are completely compatible with the 8080.

MP11 INITIALIZATION

The $\overline{\text{RESET}}$ input controls the status of the control and peripheral registers of the MP11. The initialization sequence will differ if $\overline{\text{RESET}}$ is connected to a master reset line of a microprocessor or if it is hard-wired to V_{cc}. The MP11 will require initialization every time the $\overline{\text{RESET}}$ line is activated low. If the $\overline{\text{RESET}}$ line is hard wired to V_{cc}, the MP11 must be initialized only once before output of the data is attempted.

MP11 ADDRESS STRUCTURE

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
X	X	1	1	1	1	1	1	1	1	1	1	0	a	Y	Y

A_{15}, A_{14} - don't care, not connected to MP11
A_2 - Address is user selectable
A_0, A_1 - Addresses control the initialization sequence

Initialization sequence when $\overline{\text{RESET}}$ is hard wired to V_{cc}:

1. Load accumulator with "zeros"
2. Store accumulator at memory locations:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	0	Address of Control register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	1	Address of Control register B

3. Load accumulator with "ones"
4. Store accumulator at memory locations:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	0	Address of Peripheral register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	1	Address of Peripheral register B
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	0	Address of Control register A
X	X	1	1	1	1	1	1	1	1	1	1	0	a	1	1	Address of Control register B

For the 6800 this sequence can be written as follows:

	LDAA	"zeros"	Loads Zeros in accumulator
	STAA	Address of control register A	Stores zero's in C.R.A.
	STAA	Address of control register B	Stores zero's in C.R. B
	LDAA	"ones"	Loads one's in accumulator
	STAA	Address of peripheral register A	Stores one's in P.R.A
	STAA	Address of peripheral register B	Stores one's in P.R.B.
	STAA	Address of control register A	Stores one's in C.R.A
	STAA	Address of control register B	Stores one's in C.R.B
Or as:	LDX	# $0000	Loads zero's in index register
	STX	$ Address control register A	Stores zero's in C.R. A and B
	LDX	# $1111	Loads one's in index register
	STX	$ Address peripheral register A	Stores one's in P.R. A and B
	STX	$ Address control register A	Stores one's in C.R. A and B

Initialization sequence when $\overline{\text{RESET}}$ line is connected to master reset (control registers A and B are always set to zero after master reset and only ones need to be stored in the registers):

LDAA	"ones"
STAA	Address Peripheral register A
STAA	Address Peripheral register B
STAA	Address Control register A
STAA	Address Control register B

or as:

LDXX	# $1111
STX	$ Address Peripheral register A
STX	$ Address Control register A

Now data can be written into MP11. This is accomplished by outputting the correct MP11 address:

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	0	OUTPUT 1
X	X	1	1	1	1	1	1	1	1	1	1	0	a	0	1	OUTPUT 2

At the time that the address appears on the address bus, data will appear on the data bus, and if the R/W and Enable pulses are correctly timed, 25μsec from the true address the analog voltage will be stable at the selected output.

Timing requirements shown in Figure 1 must be satisfied for the MP11 to be initialized and operate correctly. All timing requirements are completely compatible with 6800 microprocessors. User definable address line A_2 used in conjunction with the B_2 input allows the user to place the MP11 in two different memory locations or use two different MP11's in order to expand the analog system to four outputs. When B_2 is wired to logical 1, the MP11 responds to an A_2 address of 0 and when B_2 is wired to a logical 0, the MP11 responds to an A_2 address of 1.

TEST PROGRAMS

The test circuit and test programs following allow the user to test the operation of the MP10 or MP11. The test may be conducted by setting up the MP10/MP11 as shown in Figure 3. The microprocessor system should have a teletype/CRT terminal interface. The programs will step through several output voltage levels for each DAC output (see Figure 4). Notice how the software is different for the two test programs to illustrate two software approaches.

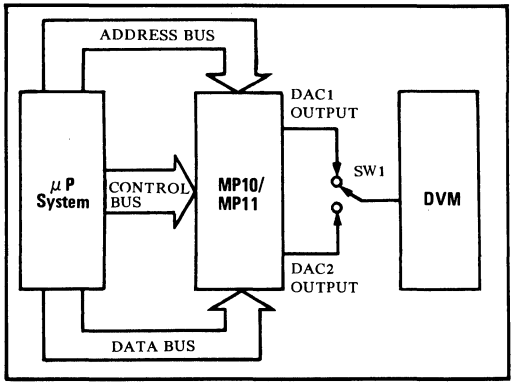


FIGURE 3. Test Circuit for MP10/MP11.

MP10 Test Program

```
                    Initialize MP10
        LXI H ADDR X        Address of the first
                            byte of data.
LOOP 1  MOV A, M            Load ACC with first byte
                            of data.
        STA ADDR2           Output to MP10 DAC1
        INX H               Increment ADDR1
        CALL CI             Call Input routine
        CPI                 Wait for any character
        8D                  except carriage return
        JNZ LOOP1
        LXI ADDR X
LOOP 2  MOV A, M
        STA ADDR3           Output to MP10 DAC2
        INX H               Increment ADDR1
        CALL CI
        CPI                 Wait for any character
        8D                  except carriage return
        JNZ LOOP2
        RET
```

The MP10 test program will output five different voltages from DAC1 and then from DAC2 (see Figure 4). DAC1 will initially output -10V. To step through the other values for DAC1 enter any character other than carriage return (CR). To transfer control to DAC2, enter CR. DAC2 will output -10V. To step through the other values for DAC2 enter any character except CR. To exit the test program, enter CR.

Store the following codes in memory beginning with location ADDR X:

ADDR X ← FF
ADDR X + 1 ← BF
ADDR X + 2 ← 7F
ADDR X + 3 ← 3F
ADDR X + 4 ← 00

ADDR 2 is the address of output 1, ADDR 3 is the address of output 2:

MP11 Test Program

```
                        Initialize MP11
        LDX  # $ FFFF;  Load index register
        STX  ADDR 1;    Store FF in each DAC
        JSR  INP
        LDX  # $ BFBF;  Load index register
        STX  ADDR 1;    Store BF in each DAC
        JSR  INP
        LDX  # $ 7F7F;  Load index register
        STX  ADDR 1;    Store 7F in each DAC
        JSR  INP
        LDX  # $ 3F3F;  Load index register
        STX  ADDR 1;    Store 3F in each DAC
        JSR  INP
        LDX  # $ 0000;  Load index register
        STX  ADDR 1;    Store 00 in each DAC
        JSR  INP
INP     LDAA ADDR X     Load Status of ACIA   } Wait for
        Bit A  #01                            } TTY
        BEQ  INP                              } input
        LDA A ADDR X + 1 Load Data From ACIA  }
        CMP  A                                } Jump back
        8D                                    } to test
        BNE  Back                             } program or
        JMP  Return                           } return to
BACK RTS                                      } main program
```

The MP11 test program will output -10V from both DAC1 and DAC2 then wait for an input from the TTY. Any character except CR will advance both DAC's of the MP11 to the next value as defined in Figure 4. CR terminates test program by jumping to RETURN.

ADDR 1 is the address of output 1, ADDR X is the address of the ACIA.

Step	Ideal Output	Actual Output Limits
1	-10V	-9.922V to -10.078V
2	-5.0V	-4.922 to -5.078
3	0.000V	-0.078 to +0.078
4	+5.0V	+4.972 to +5.078
5	+9.922V	+9.844 to +10.000

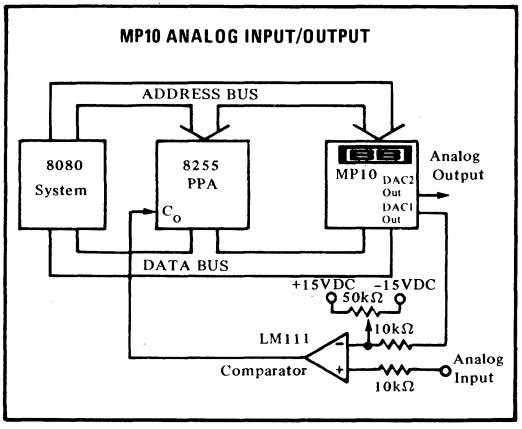
FIGURE 4. Output Voltages for Test Programs.

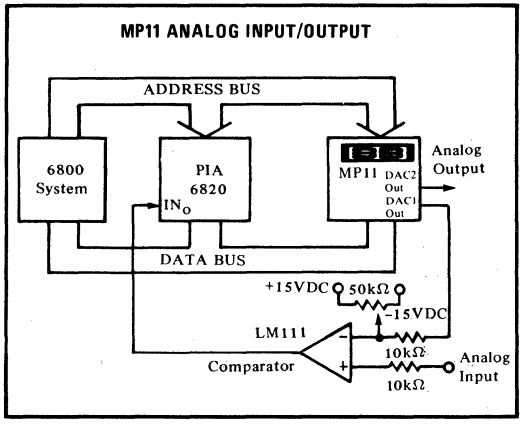
APPLICATIONS

ANALOG INPUT AND ANALOG OUTPUT

Although the MP10 and MP11 are analog output peripherals, they can be easily adapted to provide both analog inputs and outputs.

With the addition of a few external components, these units can each provide one analog input and one analog output for your system as shown below:

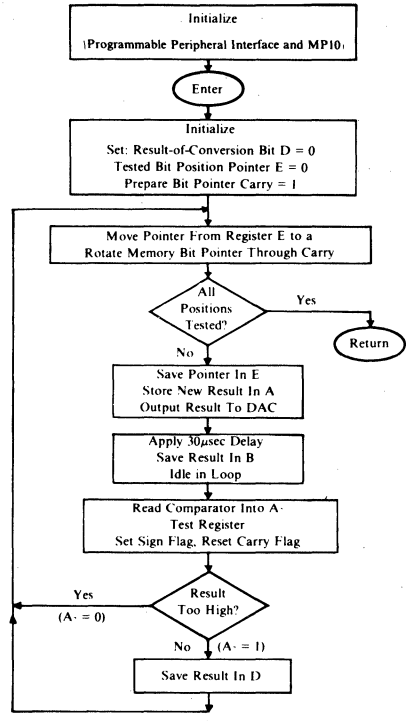




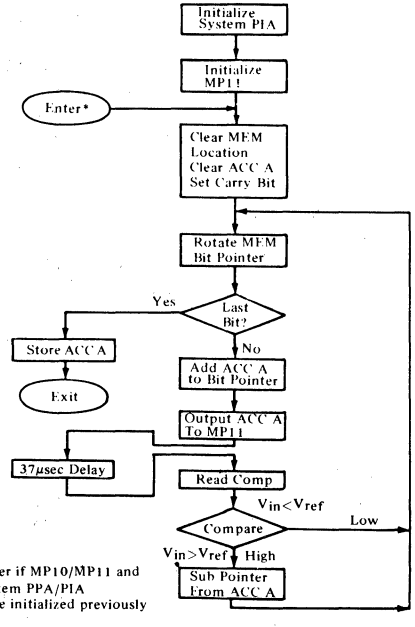
These systems use the microcomputer system to perform the logic of a successive approximation A/D converter, using one channel of the MP10 or MP11 to provide the D/A converter reference function required. In a successive approximation converter, the analog input is compared to known outputs of a D/A converter. First, the microcomputer turns the MSB on, waits for the settling time of the MP10 or MP11, and the switching time of the comparator, then reads the status. If the comparator indicates that the MSB voltage is smaller than the analog input, the MSB input to the MP10/MP11 stays "on" and the next most significant bit is turned on. If the comparator indicates that the MSB value is larger than the analog input, the microcomputer will turn the MSB "off" and turn "on" the next most significant bit. In this way all 8 bits of the D/A converter are tested. When the conversion is complete, the input of the D/A converter will be a digital representation of the analog input. This value will also be stored in the microprocessor's accumulator (complementary binary).

The A/D conversion will require approximately 900 microseconds when performed in this manner. Burr-Brown will shortly have available a detailed application note describing this process including all software required.

FLOWCHART USING 8080 and MP10



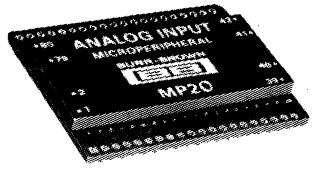
FLOWCHART USING 6800 and MP11



* Enter if MP10/MP11 and system PPA/PIA were initialized previously

BURR-BROWN®

MP20



Microprocessor-Interfaced 8-BIT DATA ACQUISITION SYSTEM

FEATURES

- COMPATIBLE WITH:
  - 8080A
  - 8085
  - 8008
  - 8048
  - Z-80
  - SC/MP
- EASY TO PROGRAM
  - Choice of ways to interface:
    - Memory-mapped or I/O mapped
    - Only one instruction to acquire data
- EASY TO USE
  - Completely compatible with 8080A microprocessors
  - PPA is not needed
  - No external logic needed
  - No external adjustments
  - Low or high level analog inputs
  - Unlimited expansion
- COMPLETELY SELF-CONTAINED
- LOW COST
- SAVES DEVELOPMENT TIME AND MONEY

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

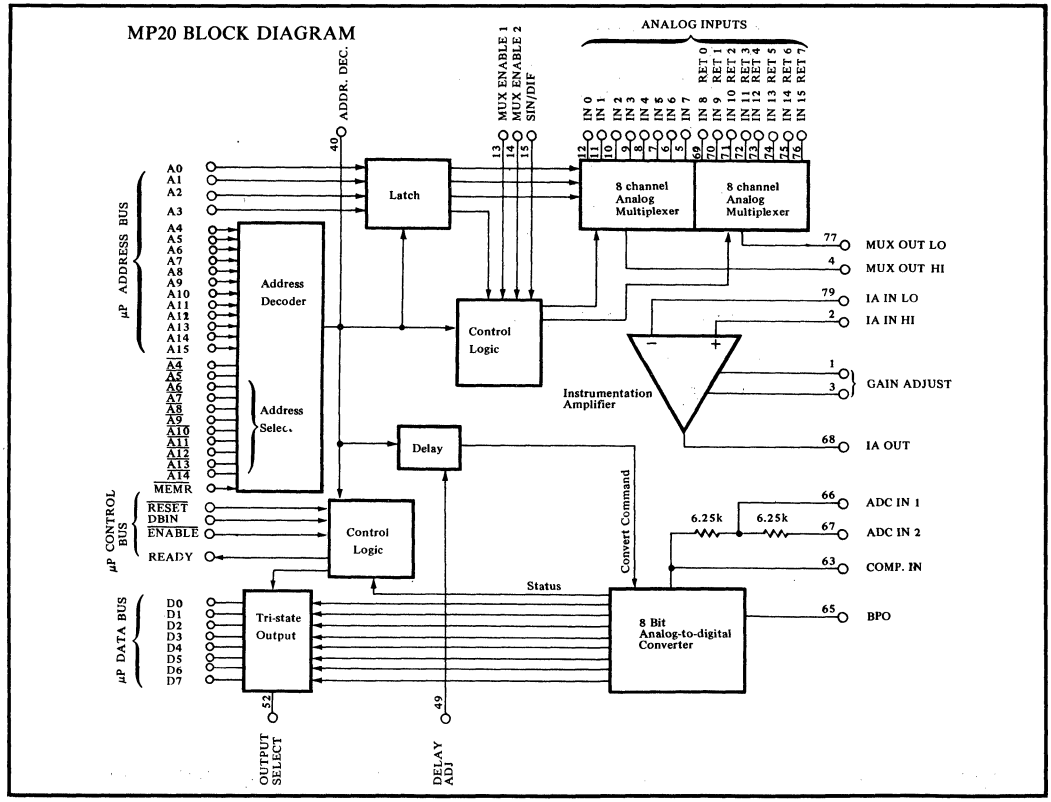
DESCRIPTION

The MP20 is a complete analog input system packaged in an 80-pin quad-in-line package. It is completely compatible with 8080A and 8008 microprocessors. It is also compatible with SC/MP and with the Z-80. The MP20 contains a high speed 8-bit A/D converter, an instrumentation amplifier, an input multiplexer that can accept up to 16 single-ended signals or 8 differential signals as well as interface, timing and address decoding logic. The gain and offset are internally laser trimmed so that no external adjustments are required on the ±5V or 0 to +5V input range to obtain an absolute accuracy of better than ±0.4% (1 LSB). The system can digitize low level or high level analog signals. The gain of the internal instrumentation amplifier can be programmed with a single external resistor to allow input signal ranges as low as ±10 mV. This means that the MP20 can be connected to low level sensors such as thermocouples and strain gauges without external signal amplification.

The address lines A0 through A15 are low power Schottky TTL compatible and can be connected directly to the address bus of an 8080A or 8008. All digital input lines require standard LSTTL voltages.

PROGRAMMING

When programming these peripherals, the user treats them as memory. Each analog input channel occupies one memory location. Any memory reference instruction can be used. Since most microprocessors have been optimized for memory usage, memory reference instructions are the most powerful instructions in a microprocessor's repertoire. The MP20 is treated as memory to simplify software and allow an almost unlimited number of systems to be connected to a single processor. Pins $\overline{A4}$ to $\overline{A14}$ are made available so that the microperipheral address can be hardwired for almost any possible memory location. Since these units are treated as memory, a single instruction is all that's needed to read an input channel. For instance, when the MP20 is used with an 8080A, a single instruction, LHLD, can be used to input data to the H and L registers from two consecutive analog inputs. Likewise, a single LDA or MOV instruction will input data from one channel to the CPU.



SPECIFICATIONS

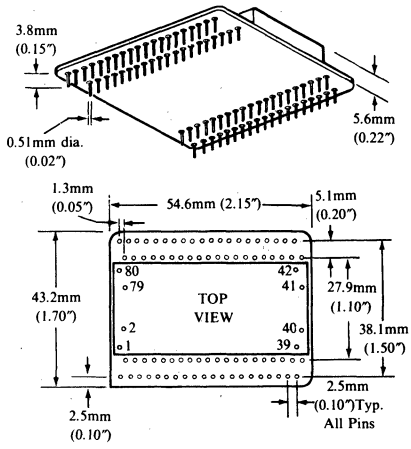
(Typical at 25°C unless otherwise noted.)

ELECTRICAL

TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
Number of channels	16 single-ended/8 differential
Throughput rate[1] (max)	40 μsec/channel
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	2 to 250
Amplifier gain equation	$G = 2 + 50k\Omega/R_{EXT}$[2]
Max input voltage without damage[3]	±20 volts
Max input voltage for multiplexer operation	±6 volts
Input impedance	$5 \times 10^9\Omega$ || 10 pF - OFF channel
	$5 \times 10^9\Omega$ || 100 pF - ON channel
Bias current 25°C	100 nA
0 - 70°C	200 nA
Amplifier output noise	
Gain = 100, R_S = 500 Ω	400 μV rms (10 Hz to 10 kHz)
Amplifier input offset voltage (max)	±1 mV
Amplifier offset voltage drift	±(6 + 50 G) μV/°C
Amplifier settling time (to .1% FSR)	
G = 2	20 μs
G = 10	25 μs
G = 50	50 μs
G = 100	100 μs
G = 200	200 μs
CMRR (for differential inputs) G = 2	70 dB (DC to 60 Hz)
ACCURACY	
Throughput accuracy	
±5V range (max)[4]	±0.4% of FSR[5]
0-5V range (max)[4]	±0.4% of FSR
±50 mV range (max)[6]	±0.8% of FSR
0-50 mV range (max)[6]	±0.8% of FSR
Linearity (max)[4]	±0.2% of FSR
Differential linearity[4]	±0.2% of FSR
Quantizing error	±1/2 LSB
Gain error[4]	±0.1%
Offset error[4]	±0.1% of FSR
Power supply sensitivity	
±15V	$\pm 0.02\%/\%\Delta V_{CC}$
+5V	$\pm 0.002\%/\%\Delta V_{CC}$
STABILITY OVER TEMPERATURE	
System accuracy drift[7] (max)	±40 ppm/°C
Linearity (max)	±20 ppm/°C
Monotonicity (0°C to +70°C)	Guaranteed
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microprocessor bus	
Output coding	Binary or Binary two's complement
Logic loading	All digital inputs are one LSTTL load
Output drive (D0 - D7)	5 TTL loads or 20 LSTTL loads
An analog input channel is selected by:	A0 - A3
The output data bits are read into:	D0 - D7
POWER REQUIREMENTS	
Rated voltages	±15V, +5V
Range for rated accuracy	4.75 to 5.25 and ±14.5 to ±15.5V
Supply drain ±15V	±30 mA
+5V	+90 mA
TEMPERATURE RANGE	0°C to +70°C

(1) Includes 35μsec for mux and amplifier settling time and 5μsec for ADC conversion time.
(2) R_{EXT} is the resistance between pins 1 and 3.
(3) With power applied.
(4) Gain = 2, with no external adjustments.
(5) FSR is Full Scale Range (FSR is 10V for ±5V range).
(6) Gain = 100 with external gain and offset trim.
(7) Includes gain drift, offset drift and linearity drift.

MECHANICAL



MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20 pin strips)

PIN CONNECTIONS

Pin 1	IA GAIN ADJUST	Pin 41	A14
2	IA IN HI	42	$\overline{A14}$
3	IA GAIN ADJUST	43	A15
4	MUX OUT HI	44	$\overline{MEMR}$
5	IN 7	45	$\overline{DBIN}$
6	IN 6	46	$\overline{ENABLE}$
7	IN 5	47	$\overline{RESET}$
8	IN 4	48	READY
9	IN 3	49	DELAY ADJ
10	IN 2	50	+5V
11	IN 1	51	DIG. COM
12	IN 0	52	OUTPUT SELECT
13	MUX ENABLE 1	53	D7 (MSB)
14	MUX ENABLE 2	54	D6
15	SIN. DIF	55	D5
16	A0	56	D4
17	A1	57	D3
18	A2	58	D2
19	A3	59	D1
20	A4	60	D0 (LSB)
21	$\overline{A4}$	61	-15V
22	A5	62	+15V
23	$\overline{A5}$	63	COMP IN
24	A6	64	ANA. COM
25	$\overline{A6}$	65	BPO
26	A7	66	R2
27	$\overline{A7}$	67	R1
28	A8	68	IA OUT
29	$\overline{A8}$	69	IN 8 RET 0
30	A9	70	IN 9 RET 1
31	$\overline{A9}$	71	IN 10 RET 2
32	A10	72	IN 11 RET 3
33	$\overline{A10}$	73	IN 12 RET 4
34	A11	74	IN 13 RET 5
35	$\overline{A11}$	75	IN 14 RET 6
36	A12	76	IN 15 RET 7
37	$\overline{A12}$	77	MUX OUT LO
38	A13	78	OFFSET NULL
39	$\overline{A13}$	79	IA IN LO
40	ADDR DECODE OUT	80	OFFSET NULL

PIN FUNCTIONS

IA GAIN ADJUST (Optional). Pin 1 and Pin 3. By connecting a resistor between pin 1 and 3 the gain of the internal instrumentation amplifier can be varied as follows:

$$\text{Gain} = 2 + 50\text{k}\Omega/R$$

where R is the gain setting resistor. The IA is factory adjusted for a gain of 2 without any external resistor.

Important: If a gain greater than 10 is required an external capacitor must be connected from "DELAY" (pin 49) to +5V. This increases an internal delay to allow for the increased settling time of the instrumentation amplifier.

IA IN HI Pin 2. This is the positive input of the internal instrumentation amplifier. This should be connected to pin 4 (MUX OUT HI) for normal operation.

MUX OUT HI Pin 4. This is the high output of the analog input multiplexer. This is connected to pin 2 (IA IN HI) for differential operation. It is connected to pin 77 (MUX OUT LO) and pin 2 for single-ended input operation.

IN7 - IN0 Pins 5 - 12. The first 8 (of 16) analog inputs for single-ended operation or the 8 positive inputs for 8 channel differential input operation.

MUX ENABLE 1 Pin 13. Leave open for single-ended input operation. Connect to pin 14 (MUX ENABLE 2) for differential input operation.

MUX ENABLE 2 Pin 14. Connect to pin 15 (SIN/DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.

SIN/DIF Pin 15. Single/Differential input operation connect to pin 14 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.

A0 - A3 Pin 16 - 19. Address lines that select one of 16 analog input signals (IN0 - IN15). 0000 selects channel 0 and 1111 selects channel 15 when the correct address is presented to the MP20. Connect A3 to ground for 8 channel differential operation.

A4 - A15 Address lines. Pins 20, 22, 24, 26, 28 30, 32, 34, 36, 38, 41, and 43. When the proper address is presented to the MP20 in addition to the $\overline{\text{MEMR}}$ (pin 44) pulse, the conversion is initiated.

$\overline{\text{A4}}$ - $\overline{\text{A14}}$ Address select lines. Pin 21, 23, 25, 27, 29, 31, 33, 35, 37, 39 and 42. By connecting these lines to DIG COM or +5 volts (through a 1kΩ resistor) almost any address can be assigned to the MP20. For example if $\overline{\text{A4}}$ is connected to GND., the correct (valid) address for A4 is a "1" (> + 2.0).

ADDR DEC Pin 40. A positive pulse will appear when a valid address appears on the MP20 address lines and $\overline{\text{MEMR}}$ (pin 44) is low. The rising edge of this pulse strobes the input channel select information (A0 - A3) into a latch. It can also be used for external purposes.

$\overline{\text{MEMR}}$ Pin 44. Memory read. A "Low" pulse on this line along with a correct address will enable D0 - D7 (data lines). Also used to initiate a conversion.

DBIN Pin 45. Connect to DBIN on 8080.

$\overline{\text{ENABLE}}$ Pin 46. Enables MP20 output. Connect to ground for normal operation (see figure 7).

$\overline{\text{RESET}}$ Pin 47. A "Low" on this line is required to RESET the MP20. Connect to RESIN input of the system's 8224 or invert 8080's RESET input.

READY Pin 48. When the MP20 is "Read" by the microprocessor, the READY line will go "Low" until conversion is complete. If the READY line is used to halt the CPU, the 8080 will enter a "Wait" state (T_w) until the multiplexer, instrument amp, and A/D converter have completed converting the analog data to a binary 8 bit code (40 μsec with gain ≤ 10). The READY line will then return to its "High" state which releases the processor from the T_w state. The output data appears on the data bus (D0 - D7) during the T_3 state.

DELAY ADJ Pin 49. When the MP20 is addressed, an internal delay of approximately 35μsec is initiated to allow for multiplexer and instrumentation amplifier settling time. When the IA is operated with gain > 10 this delay must be increased (see figure 4 and figure 5) to allow for the increased settling time of the IA.

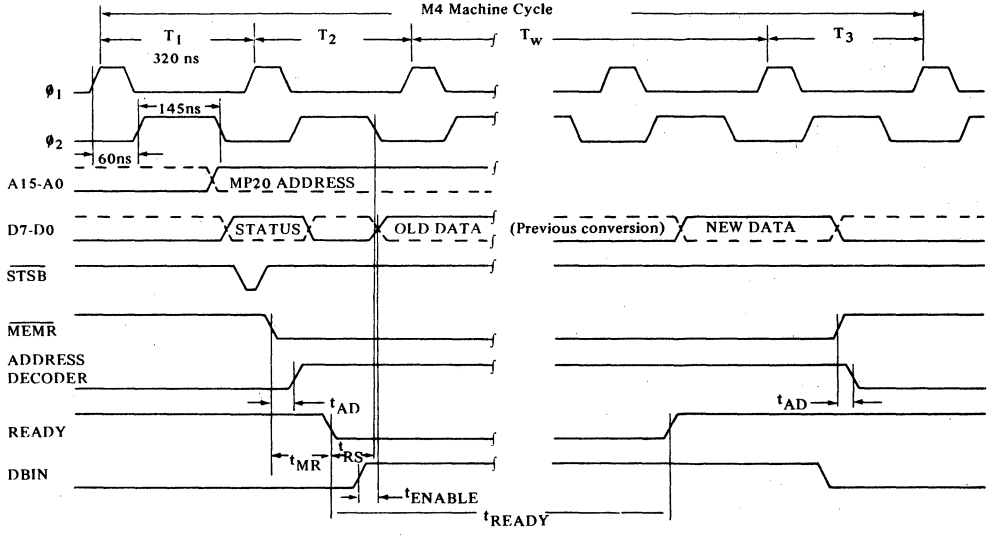
+5V Pin 50. +5 volt at 140 mA maximum, 90 mA typical.

DIG COM Pin 51. Digital common. This pin should be connected to analog common (pin 64) as close to the MP20 as possible for optimum performance.

OUTPUT SELECT Pin 52. This pin should be connected to DIG COM to obtain binary data at D0 - D7. To obtain two's complement data (bipolar mode) connect pin 52 to +5V through a 1kΩ resistor.

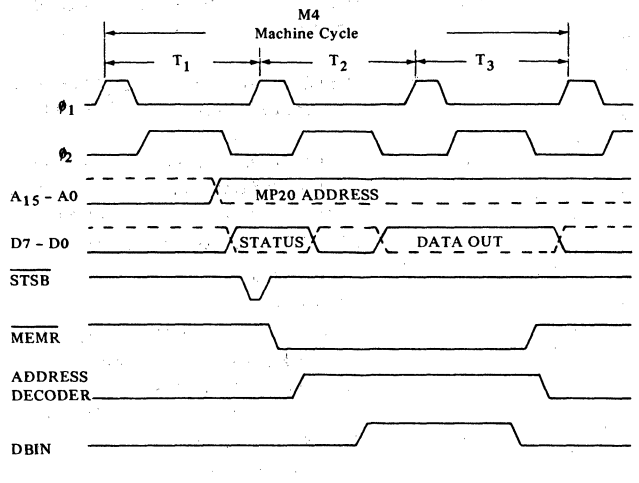
D7 - D0 Pin 53 - 60. 8 bit data bus. Tri-state low power Schottky TTL compatible.

-15V	Pin 61. -15 volt at 30 mA typical.
+15V	Pin 62. +15 volt at 30 mA typical.
COMP IN	Pin 63. Comparator input of 8 bit A/D converter (successive-approximation). Leave open for unipolar operation or connect to "BPO" (pin 65) for bipolar operation. NOTE: This point is extremely sensitive to noise. Any connection to this line should be as short as possible and shielded by ANA COM or ±15 volt supply patterns.
ANA COM	Pin 64. Analog common should be connected to digital common (pin 51) as close to the MP20 as possible for optimum performance.
BPO	Pin 65. A/D converter bipolar offset. It should be connected to ANA COM (pin 64) for unipolar operation of COMP IN (pin 63) for bipolar operation.
R2	Pin 66. A/D converter input resistor. Connect to IA OUT (pin 68) for 0 to +5V input unipolar operation or ±2.5V input bipolar operation. Leave open for ±5V input bipolar operation.
R1	Pin 67. A/D converter input resistor. Connect to IA OUT for ±5 volt operation.
IA OUT	Pin 68. Instrumentation amplifier output. Connect to R1 (pin 67) or R2 (pin 66) for normal operation.
IN8 - IN15 RET0-RET7	Pin 69 - 76. Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
MUX OUT LO	Pin 77. Multiplexer output for IN8 – IN15 RET0 – RET7 Connect to "MUX OUT HI" (pin 4) and "IA IN HI" (pin 2) for single-ended input operation or connect to "IA IN LO" (pin 79) for differential input operation.
OFFSET NULL	Pin 78, 80. Optional instrumentation amplifier offset adjust (see figure 1).
IA IN LO	Pin 79. Negative input of instrumentation amplifier. Connect to ANA COM (pin 64) for single-ended input operation or "MUX OUT LO" (pin 77) for differential input operation.



All waveforms shown are for an 8080A - 1 microprocessor operating at:
CLOCK PERIOD (t_{CY}) = 320 ns
INSTRUCTION CYCLE = 1.3 μs
ϕ_1 and ϕ_2 clock signals are shown for reference only. They are not required for operation of MP20.

MP20 Timing Diagram Normal Operation (LDA Instruction using READY to stop microprocessor during conversion).



SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AD}	Delay from $\overline{MEMR}$ to ADDR. DEC.	-	25	ns
t_{MR}	Delay from $\overline{MEMR}$ and correct address to READY	-	100	ns
t_{RS}	Delay from READY to ϕ_2.	-	90	ns
t_{ENABLE}	Output Data Stable from DBIN	-	40	ns
t_{READY}	Conversion time (READY low)	-	40	μs

The LDA Instruction will READ the data from the previous conversion and start a new conversion. The new data can be read in 40 μs (max).
CAUTION: Do not read the MP20 while a conversion is in progress or an erroneous output may result.

MP20 Timing Diagram (LDA Instruction without stopping microprocessor during conversion).

OPERATING INSTRUCTIONS

PROGRAMMING

The MP20 is easily programmed since it is treated as memory. It uses any memory reference instruction that can read data. A single instruction can read data from one channel (LDA) or two adjacent channels (LHLD).

Example: MP20 used with an 8080. MP20 base address - FF70; acquire data from channels FF70 through FF72. Normal operation.

```
LHLD FF70    Acquires data and transfers channel 0
             (FF70) data to L register and channel 1
             (FF71) data to H register.
LDA FF72     Acquires data from channel 2 (FF72) and
             transfers to the accumulator.
```

The MP20 may be operated in several programming modes. The minimum software approach (i.e., one instruction to acquire data as described above) is to halt the CPU during conversion (40 μsec). This mode of operation is effected by connecting the READY line (pin 48) of the MP20 to the 8080's READY input. The MP20 may also be operated without halting the CPU. In this mode of operation conversion may be initiated by a memory read instruction referenced to the proper channel. When the conversion is complete, the data value may be acquired by another read instruction. The second read instruction can be referenced to any channel address of the MP20. This instruction should be addressed to the next channel to be acquired since it will start a conversion cycle.

Example: MP20 used with an 8080. MP20 base address - FF70; acquire data from channels FF70 through FF72. Do not halt CPU.

```
LDA FF70     Starts conversion of channel 0 (FF70).
  :          At least 40 microseconds of software here to
  :          insure that conversion is complete.
LDA FF71     Transfers conversion data from channel 0
  :          (FF70) to accumulator and starts conversion
  :          of channel 1 (FF71).
  :          At least 40 microseconds of software.
LDA FF72     Transfers conversion data from channel 1
  :          (FF71) to accumulator and starts conversion
  :          of channel 2 (FF72).
  :          At least 40 microseconds of software.
LDS FF7X     Transfers conversion data from channel 2
             (FF72) to accumulator and starts conversio
             of any other channel of data.
```

The time required for conversion may be between 40 and 200 microseconds depending upon the gain of the internal instrumentation amplifier. Therefore, the 40 microsecond time between LDA instructions shown above could be as long as 200 microseconds for a system used in the highest gain mode. If desired, the READY line may be polled to determine that conversion is complete and the data output valid. Of course, if direct addressing is not desired, MOV instructions may also be used.

Example: MP20 used with an 8080. MP20 base address FF70. Normal Operation. Read and Print the value of all 16 input channels and then stop.

```
CROUT   EQU 01F3H (01EEH)
NMOUT   EQU 02C2H (02C3H)
        LXI SP 3FFF H (13EDH)
        LXI H 0FF70 H    :Address for channel zero
BEG 1:  MOV D, M         :Read data from board
        CALL CROUT       :Print CR & LF
        MOV A, D
        CALL NMOUT       :Print data
```

```
        INX H           :Next channel
        MOV A, L
        CPI 10          :Have all 16 channels
                         been read?
        JZ WHOA
        JMP BEG 1
WHOA:   HLT
```

This program assumes that the system is under the control of the SBC80/10 prototype package monitor (M80P, version 1.0, March 1, 1976). The locations in parenthesis are used with the MCS-80 system design kit.

The base address of the MP20 is set by inputs $\overline{A4}$ through $\overline{A14}$. Address lines A4 through A14 respond to the inverse of inputs $\overline{A4}$ through $\overline{A14}$. For instance, if $\overline{A6}$ is grounded, A6 will respond to a "high" input. A15 is internally connected to respond to a "high" input.

ANALOG INPUT RANGE SELECTION

The MP20 may be set for any range between ±5V and ±10 mV. Table I shows the pin connections for the various high level ranges available.

MP20 Input Range	Gain	ADC Range	Pin Connections
±5V	2	±10V	65 to 63; 66 open; 67 to 68
±2.5V	2	±5V	65 to 63; 66 to 68; 67 open
±1.25V	2	±2.5V	65 to 63; 66 to 68; 63 to 67
0 - 5V	2	0 - 10V	65 to 64; 66 to 68; 67 open
0 - 2.5V	2	0 - 5V	65 to 64; 66 to 68; 63 to 67

Table I. Analog Input Range Pin Connections

The MP20 may be set to output data with straight binary coding (pin 52 grounded) or two's complement coding (pin 52 to +5VDC through a 1 kΩ resistor). Straight binary coding is typically used with unipolar input ranges and two's complement coding with bipolar input ranges. Table II describes the coding.

The internal instrumentation amplifier is factory set for a gain of 2. This gain can be increased to 250 by adding an external resistance (R_{ext}) between pins 1 and 3. R_{ext} should be a stable resistor (10 ppm/°C) since this temperature drift will add to the accuracy temperature coefficient. The gain of the amplifier can be determined by this formula:

$$\text{Gain} = 2 + \frac{50k}{R_{ext}}$$

With pins 1 and 3 open, the gain is 2.

Since the amplifier input offset will be multiplied by the amplifier gain, an offset adjust may be required (see figure 1b).

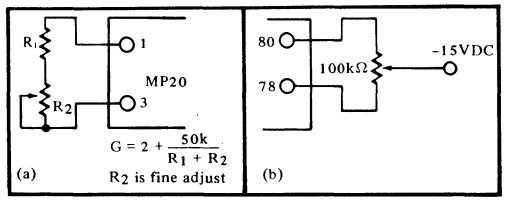


FIGURE 1. (a) MP20 Gain Adjust; (b) Offset Adjust

SINGLE ENDED VS. DIFFERENTIAL INPUTS

The MP20 analog inputs may be connected as single-ended, differential or pseudo-differential. Single-ended operation may be used for high level (over one volt full scale) signals in low noise environments (Figure 3). Differential operation will reject common-mode noise appearing on both inputs (Figure 2). It should be used in noisy environments or with any low level signal (less than one volt). In the pseudo-differential mode, the MP20 is connected as for the single-ended mode in Figure 3 except the I.A. low input, pin 79, is not grounded. Pin 79 is connected to an external ground that is common to all of the analog inputs. In cases with a noisy remote ground where little noise will be picked up between sensor and MP20, the pseudo-differential mode may be used.

The MP20 is set for single-ended operation when wired as shown in Figure 3. The microprocessor address lines are connected as indicated in the Pin Connections table on page 6-207. Differential operation occurs when the unit is connected as in Figure 2. However, address line A3 (Pin 19) should be grounded and A3 on the microprocessor connected to A4 on the MP20. The remainder of the higher ordered microprocessor address bits should be connected to the next higher bit on the MP20.

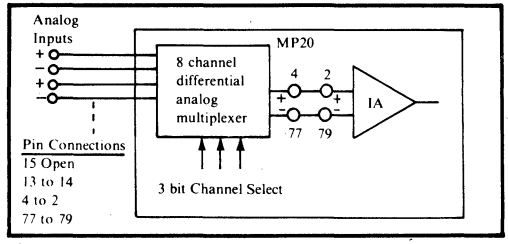


FIGURE 2. Differential Input Connections

	DIGITAL OUTPUT		ANALOG INPUT		
Straight Binary Code	Two's Complement Code		±5V	0 to +5V	±10mV
1111 1111 (FF_{16})	0111 1111 ($7F_{16}$)	+Full Scale	+4.961V	+4.980V	+9.92mV
1000 0000 (80_{16})	0000 0000 (00_{16})	Mid-Scale	0.000V	2.500V	0.000V
0000 0000 (00_{16})	1000 0000 (80_{16})	-Full Scale	-5.000V	0.000V	-10.00mV
		One LSB	39mV	19.5mV	78μV

TABLE II. Analog Input Values

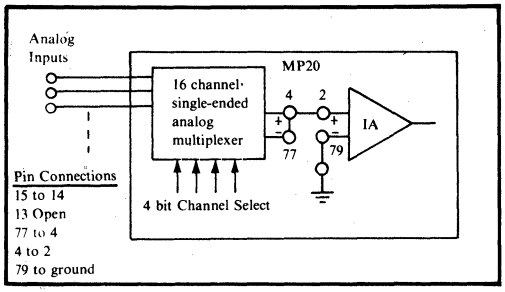


FIGURE 3. Single-ended Input Connections

DELAY TIMING

A delay time between channel selection and start of conversion is built into the MP20 to allow the analog multiplexer and instrumentation amplifier (I.A.) time to settle before starting the A/D converter. As the gain of the amplifier is increased, the settling time required increases. The factory set delay time (35 μsec) is sufficient for gains of up to 10. At higher gains, a capacitor must be added from pin 49 to the +5 VDC supply to increase the delay time. Figure 4 shows the settling time of the MP20 vs. gain. Figure 5 shows the value of capacitance required to increase the delay.

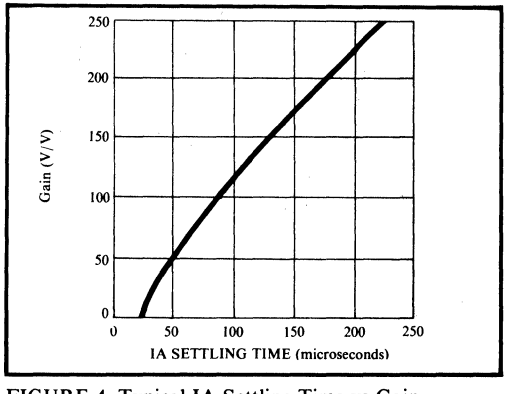


FIGURE 4. Typical IA Settling Time vs Gain (Output Settling to ±0.1%)

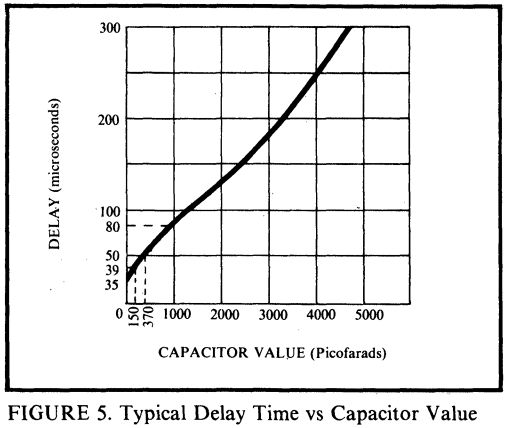


FIGURE 5. Typical Delay Time vs Capacitor Value

The only external factor, other than gain, that effects the MP20 settling time is the impedance of the source connected to a channel. Figure 6 shows a circuit model of an "ON" channel.

The signal at the output of the multiplier must be allowed to settle to ±0.1% (six time constants) to maintain the full accuracy of the system. The multiplexer time constant can be calculated with the formula: $\tau = (R_S + R_{ON})\,C_o$. For R_S = 1 kΩ and C_o = 50 pF, τ = (1.5 + 1) kΩ x 50 pF = 125ns. Thus 0.75 μs is needed to settle to ±0.1%. For high input impedances requiring more than 10 microseconds for mulitplexer settling time, the required delay time may be calculated with this formula: $T_D = \sqrt{T^2_{mux} + T^2_{IA}}$, where T_{mux} is the settling time of the multiplexer and T_{IA} is the settling time of the instrumentation amplifier as shown in Figure 4. If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitance across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5μF is sufficient. For such a capacitance the multiplexer time constant becomes 80 ns.

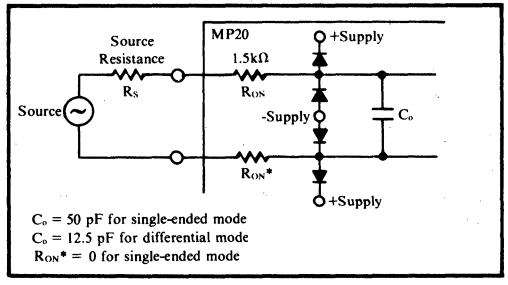


FIGURE 6. "ON" Channel Circuit Model

INPUT OVERVOLTAGE PROTECTION

As shown in Figure 6, the analog inputs have reverse biased diode circuits which protect from damage by overvoltage (such as static). It is still reasonable to take precautions against static discharge. The same circuitry protects the inputs from steady-state overvoltage damage during operation. The MP20's overvoltage protection can be increased by adding series resistors at each input. The input resistance must limit the current flowing through the input protection diodes to 10 mA. For instance, if 15 kΩ resistors are added to each input, the protection is increased to 165V (16.5kΩ x 10mA). Increased input resistance will, of course, increase the amount of time necessary for the multiplexer to settle as described in the previous section.

OUTPUT ENABLE

The circuitry used to enable the tristate output lines (D7 - D0) on the MP20 can be connected in such a way as to meet a wide variety of timing requirements. The output is enabled only when the address decoder output (pin 40) is high, DBIN (pin 45) is high, and $\overline{\text{ENABLE}}$ (pin 46) is low. Any other combination of digital signals on these lines will result in D7 - D0 being in a high impedance state (see Figure 7).

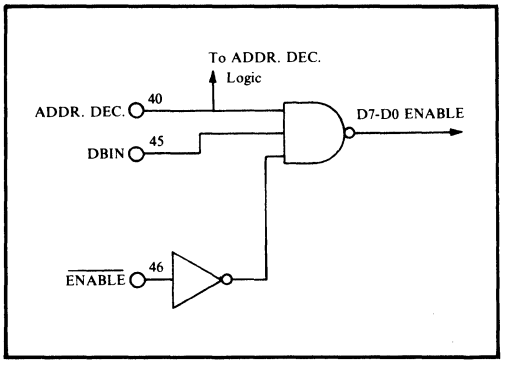


FIGURE 7. Output Enable Circuitry

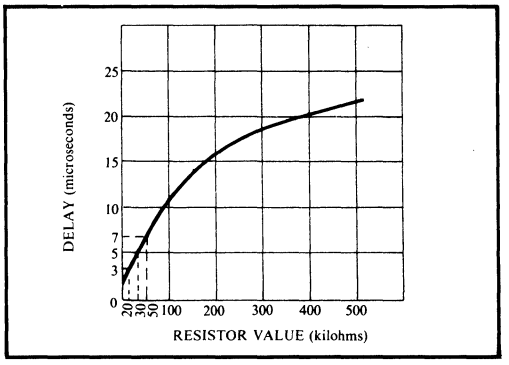


FIGURE 8. Typical Resistor Value to decrease Delay Time

The combination of a correct address and a memory read ($\overline{\text{MEMR}}$ - pin 44) command will cause the address decoder output to go high. If $\overline{\text{ENABLE}}$ is not used it should be connected to DIG COM. If DBIN is not used it should be connected to +5 volts through a 1kΩ resistor. Most applications will only require the use of one of these lines.

RESET

It is important to reset the MP20 on start up with a low pulse on the $\overline{\text{RESET}}$ line (pin 47) if the READY line (pin 48) is being used to halt the processor. The reset pulse simply clears an internal flip-flop and guarantees that on start up the READY line will go high thereby not halting CPU.

If the MP20 conversion cycle is being timed out by software control, a reset pulse is not necessary. If the $\overline{\text{RESET}}$ line is not used it should be connected to +5 volts.

HIGHER SPEED OPERATION

The MP20's internal instrumentation amplifier requires 35 microseconds to allow for settling time. If this internal amplifier is not used, substantial improvements in throughput rate can be obtained. This is easily done since neither the inputs or the output of the instrument amplifier are internally connected.The total delay time necessary may be calculated by this formula:

$$T_D = \sqrt{T^2_{MUX} + T^2_{IA}},$$

where T_{MUX} is the settling time of the multiplexer (750ns) and T_{IA} is the settling time of the instrument amplifier. For a T_{IA} of 1 μsec we have $T_D = 1.3$ μsec. Using 3μsec for the delay time to allow for unit to unit variation, the total throughput time will be 8 μsec (including 5 microseconds for ADC conversion time) or 125 kHz. A resistor between pin 49 and +5 VDC will reduce the delay time from the factory set value of 35 microseconds (see figure 8).

CALIBRATION

The MP20 is laser trimmed at the factory to ±0.4% accuracy when using the ±5V or 0 to +5V ranges. If one of these ranges is used, no adjustments are required. If the ±2.5V, ±1.25V or 0 to +2.5V ranges are used, an offset adjust only is required. For other ranges, both the gain and offset must be adjusted. Figure 1 shows the adjustment connections. The gain adjustment should be made such that the transition to a full scale output (1111 1110 to 1111 1111 for straight binary) occurs with an input of positive full scale less 1 and 1/2 LSB's. One least significant bit (LSB) is the full scale range (FSR) divided by 2^n where n is the number of bits of the A/D converter. For the MP20, one LSB is $FSR/2^8 = FSR/256$. The offset adjustment should be made such that the transition to minus full scale output (0000 0001 to 0000 0000 for straight binary) occurs with an input of negative full scale plus one half LSB. For a range of ±50 mV, one LSB = 100 mV/256 = 0.39 mV. The gain adjustment should be made at +50 mV - (1.5)(0.39 mV) = +49.42 mV. The offset adjustment should be made at -50 mV + (0.5)(0.39mV) = 49.80 mV. Table III shows offset and gain calibration values for typical ranges.

MP20 Input Range	Instrument Amp Gain	ADC Range	Calibration Values	
			Offset	Gain
±5V	2	±10V	-4.980V	+4.941V
0 to +5V	2	0 to +10V	+9.8mV	+4.971V
±2.5V	2	±5V	-2.490V	+2.471V
0 to +2.5V	2	0 to +5V	+4.9mV	+2.485V
±1.25V	2	±2.5V	-1.245V	+1.235
0 - 50mV	100	0 to +5V	+98 μV	+49.7mV
±25mV	100	±2.5V	-24.9mV	+24.7mV
0 - 25mV	200	0 to +5V	+49 μV	+24.9mV

Table III. Calibration Values.

The following program may be used to adjust gain and offset.

```
REF     EQU  00H              Offset Ref =00H
                              Full Scale Ref = FFH

CO      EQU  01E8H(01E3H)     Monitor routines

CROUT   EQU  01F3H(01EEH)
```

```
NMOUT  EQU   02C2H(02C3H)
       ;
       ORG   3C50H
       ;
       LX1   H, 0FF7ØH        Initialize
       LX1   SP,3FFFH(13EDH)
BEG1:  MVI   E,10H
BEG2:  LXI   B, 0
CLP:   MOV   A, M             ;Read data from
                               board
       SUI   REF               ;Increment data
                               count if data =
                               REF
       JNZ   NEQ
       INR   B
NEQ:   INR   C                 ;Have 100
                               conversions
                               been made?
       MVI   A, 64H
       SUB   C
       JNZ   CLP
       MOV   A, B              ;Yes, Print data
                               count
       CALL  NMOUT
       MVI   C,20H             ;Print a space
       CALL  CO
       DCR   E                 ;Full line been
                               printed?
       JNZ   BEG2
       CALL  CROUT             ;Yes, Print CR
                               & LF
       JMP   BEG1
       END
```

This program assumes that the system is under the control of the SBC80/10 prototype package monitor (M80P, version 1.0, March 1, 1976). The locations in parenthesis are used to allow the program to work with the MCS-80 system design kit. It may be used for both offset and gain calibration. The system offset should be adjusted first, followed by the gain adjustment.

The address of channel zero is assumed to be FF7Ø. If it is not, the LXI H instruction should reflect that change. The reference values on the first line assume straight binary coding. For offset binary coding, Offset Ref = 80 and Full Scale Ref = 7F.

A G3C50 monitor command will begin program execution. After 100 conversions have been made, the value (in hex) of the B register will be printed. This value represents the number of times the data read from the board was equal to "REF" (00 for offset; FF for gain).

Calibration is performed by connecting a voltage source capable of 0.01% accuracy to input channel zero (this could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.01% DVM).

The offset adjustment is made first by using the appropriate offset calibration voltage. Run the calibration program and adjust the on board offset potentiometer until the B register contains a value between $1E_{16}$ and 46_{16} (30_{10} and 70_{10}).

To perform the gain adjustment change the data labeled "REF" in the calibration program from 00 to FF, set the input voltage to the correct value as shown in Figure 8 and adjust the on board gain potentiometer in the same manner as described for offset.

If the SBC80 monitor is available, the substitute (S) command can be used to interrogate an input channel.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70 $\mu V/^{\circ}C$ and operating ranges of minus hundreds to plus thousands of degrees centigrade. When the MP20 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60 Hz or higher frequencies. When the MP20 is used as an eight channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices cannot always be observed, a differential RC filter may be used. Figure 9 shows such a system.

The 10 kΩ resistors and 10 μF capacitor provide low pass filtering (f_c = 0.8 Hz) while the optional 1 MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the $\pm$5 volt range of the multiplexer. If the sensor is earth grounded, the 1 MΩ resistors are not required. The 1 MΩ resistors do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias current of each input. See the overvoltage protection section for a discussion of the effects of the 10 kΩ in the input filter. The 1 MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10 k resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 9 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2 mV/°C.

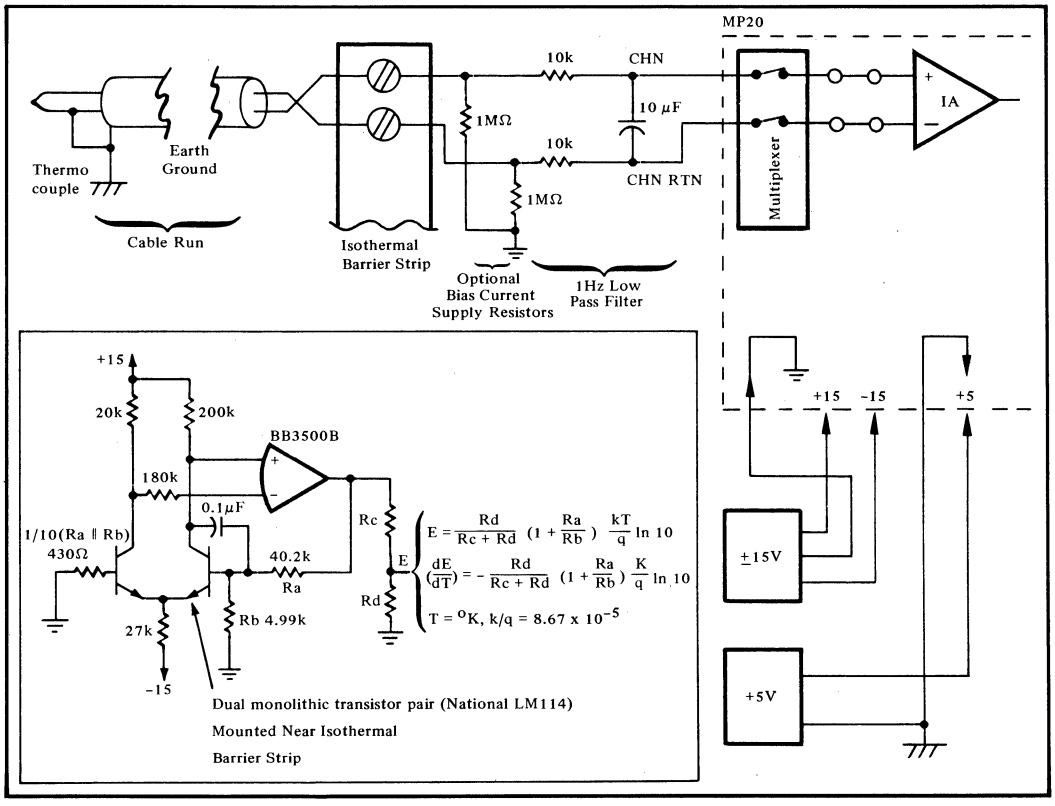


FIGURE 9. Thermocouple Input System Using MP20

PIN CONNECTION SUMMARY

	JUMPER		JUMPER
Single-ended Multiplexer	4 to 2; 4 to 77; 79 to 64; 15 to 14; 13 open	Address Bus (A0-A15)	Connect to 8080's address bus A0-A15
Differential Multiplexer	4 to 2; 77 to 79; 13 to 14; 15 open	Address Select ($\overline{A4}$-$\overline{A14}$)	Connect to +5V* or Ground
Amplifier	1 and 3 open for G = 2; R_{ext} between 1 and 3 for G≠2.	Control Bus	44 to 8228's $\overline{MEMR}$ output (pin 24) 45 to 8080's DBIN output (pin 17) 46 to ground 47 to 8224's $\overline{RESIN}$ input (pin 23) for normal operation 48 open for operation without halting CPU.
Input Range ±5V ±2.5V ±1.25V 0 - 5V 0 - 2.5V	 65 to 63; 66 open; 67 to 68 65 to 63; 66 to 68; 67 open 65 to 63; 66 to 68; 63 to 67 65 to 64; 66 to 68; 67 open 65 to 64; 66 to 68; 63 to 67		
Output Coding	52 to 51 for binary; 52 to 50* for two's complement.	Data Bus (D0 - D7)	Connect to 8080's data bus.

* Through a 1kΩ resistor

MICROPROCESSOR INTERCONNECTION

The following diagrams show interconnections of the MP20 (described in this data sheet) and also of Burr-Brown's MP10 analog output microperipheral (PDS-363) with Intel's 8080, National's SC/MP and Zilog's Z-80.

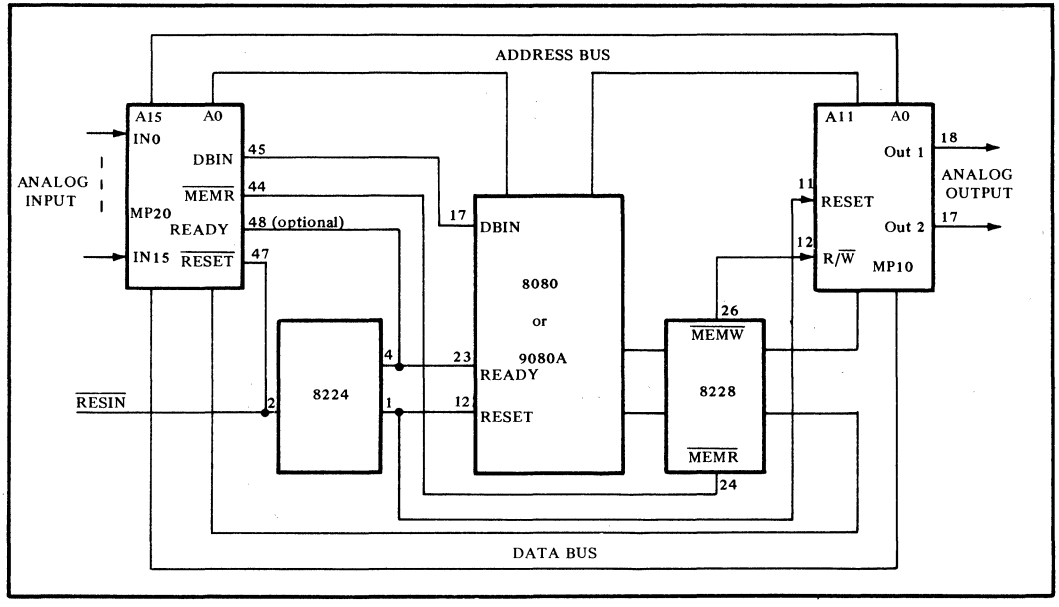


FIGURE 10. MP10 and MP20 Used With the 8080

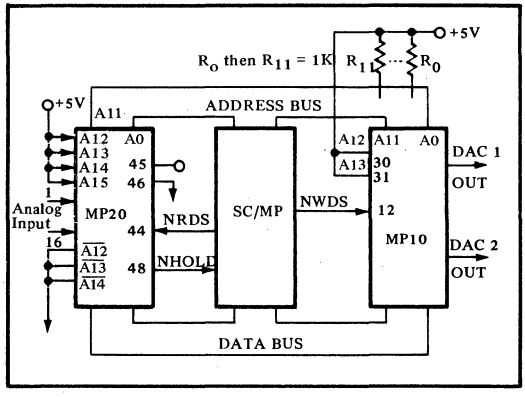


FIGURE 11. MP10 and MP20 Used With the SC/MP

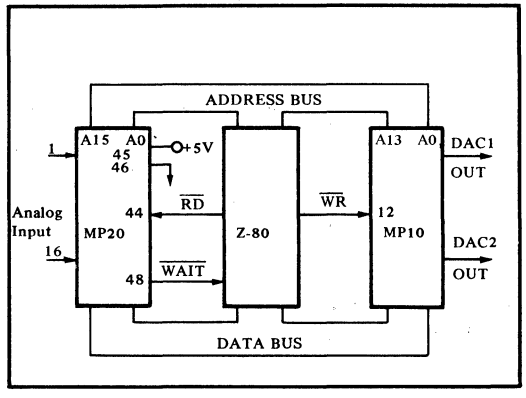
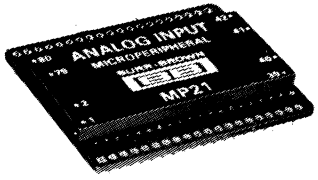


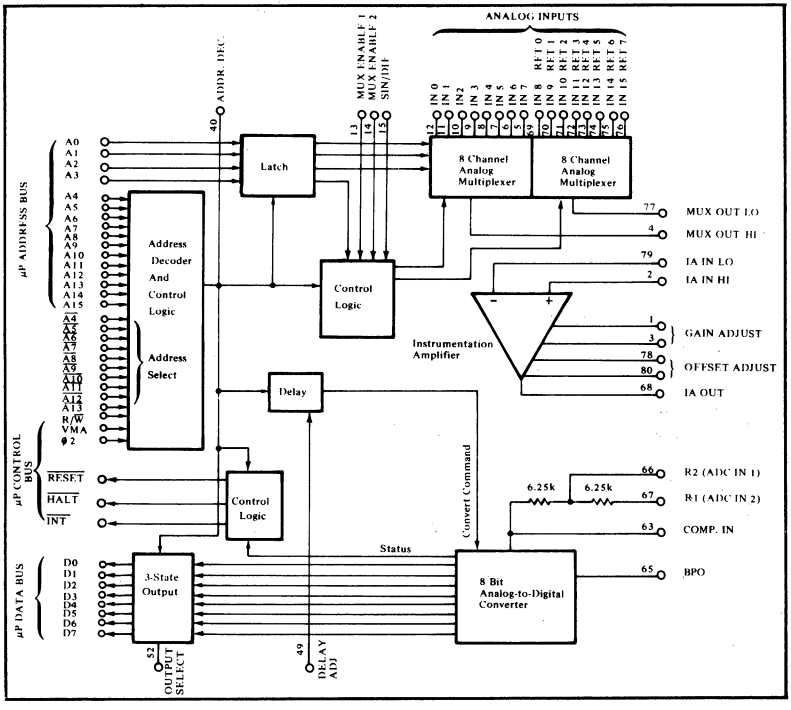
FIGURE 12. MP10 and MP20 Used With the Z-80

BURR-BROWN®

MP21



Microprocessor-Interfaced 8-BIT ANALOG INPUT SYSTEM



FEATURES

- COMPATIBLE WITH:
  - 6800
  - 650X
  - F-8
- EASY TO PROGRAM
  - Choice of ways to interface:
    - Memory-mapped
    - Interrupt capability
- SAVES DEVELOPMENT TIME AND MONEY
- EASY TO USE
  - PIA is not needed
  - No external logic needed
  - No external adjustments
  - Low or high level analog inputs
  - Unlimited expansion
- COMPLETELY SELF-CONTAINED
- LOW COST

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PDS-375

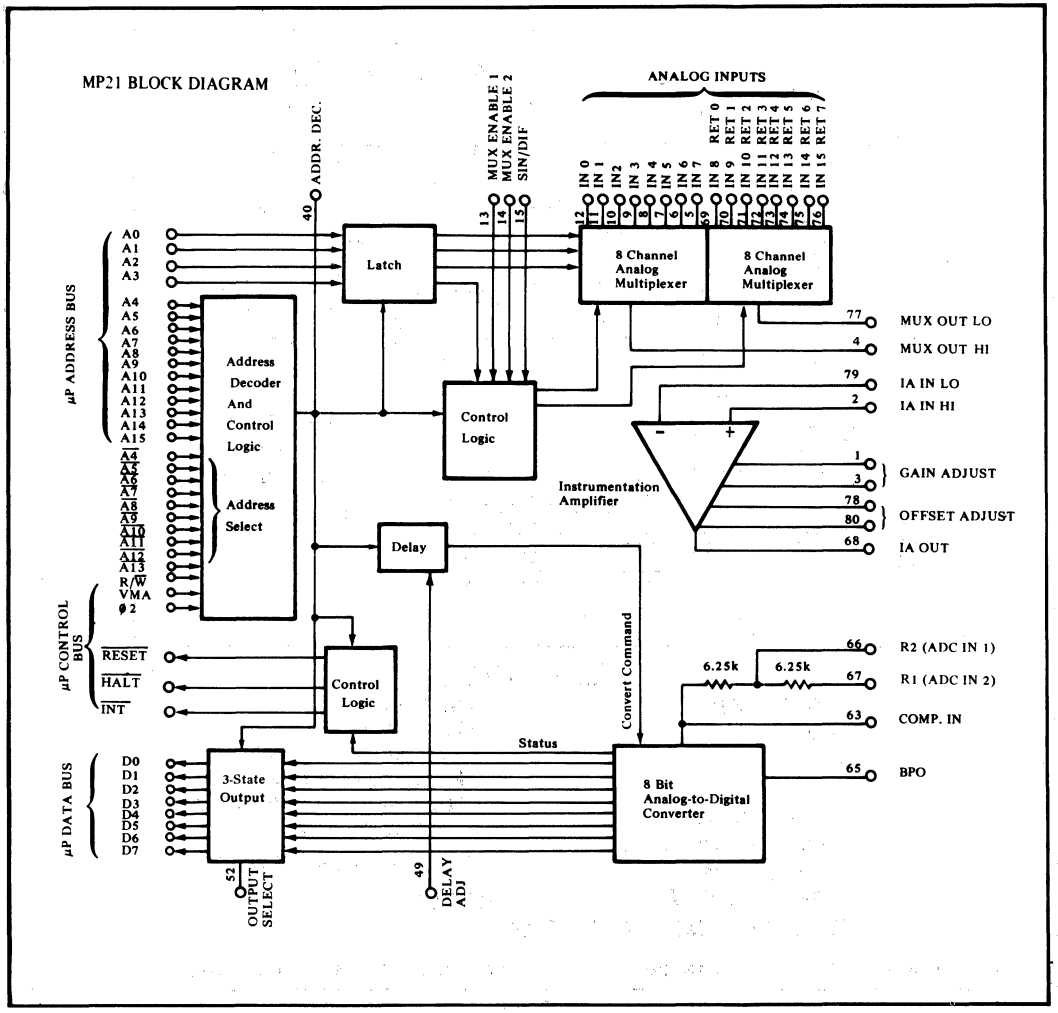
DESCRIPTION

The MP21 is a complete analog input system packaged in a 80-pin quad-in-line package. It is completely compatible with 6800 microprocessors. It is also compatible with the 650X and with the F-8. The MP21 contains a high speed 8-bit A/D converter, an instrumentation amplifier, an input multiplexer that can accept up to 16 single-ended signals or 8 differential signals as well as interface, timing and address decoding logic. The gain and offset are internally laser trimmed so that no external adjustments are required on the ±5V or 0 to +5V input range to obtain an absolute accuracy of better than ±0.4% (1 LSB). The system can digitize low level or high level analog signals. The gain of the internal instrumentation amplifier can be programmed with a single external resistor to allow input signal ranges as low as ±10 mV. This means that the MP21 can be connected to low level sensors such as thermocouples and strain gauges without external signal amplification.

All control lines are fully compatible with the microprocessor bus and operate at low power Schottky TTL levels. The MP21 input lines present one LS TTL load while all outputs can drive up to 20 LS TTL loads.

PROGRAMMING

When programming these peripherals, the user treats them as memory. Each analog input channel occupies one memory location. Any memory reference instruction can be used. Pins $\overline{A4}$ to $\overline{A13}$ are made available so that the microperipheral address can be hardwired for any of 1024 possible memory location bands. Since these units are treated as memory, a minimum of instructions are needed to read an input channel. The MP21's versatile memory mapped operation allows it to be used with or without halting the CPU or in the interrupt mode.



SPECIFICATIONS

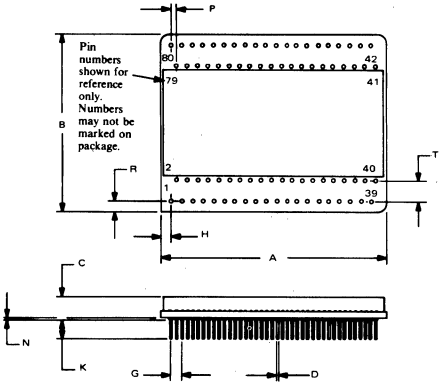
Typical at 25°C unless otherwise noted.

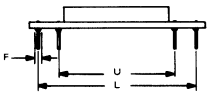
ELECTRICAL

TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
Number of channels	16 single-ended/8 differential
Throughput rate[1] (max)	40μsec/channel
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	2 to 250
Amplifier gain equation	$G = 2 + 50k\Omega/R_{ext}$[2]
Max input voltage without damage[3]	±23 volts
Max input voltage for multiplexer operation	±6 volts
Input impedance	$5 \times 10^9\Omega$ || 10 pF - OFF channel $5 \times 10^9\Omega$ || 100 pF - ON channel
Bias current 25°C	100 nA
0 - 70°C	200 nA
Amplifier output noise	
Gain = 100, $R_S = 500\Omega$	400μV rms (10 Hz to 10 kHz)
Amplifier input offset voltage (max)	±1 mV
Amplifier offset voltage drift	±(6 + 50/G)μV/°C
Amplifier settling time (to .1% FSR)	
G = 2	20μs
G = 10	25μs
G = 50	50μs
G = 100	100μs
G = 200	200μs
CMRR (for differential inputs) (G = 2)	70 dB (DC to 60 Hz)
ACCURACY	
Throughput accuracy	
±5V, ±2.5V, ±1.25V range (max)[4]	±0.4% of FSR[5]
0-5V, 0-2.5V range (max)[4]	±0.4% of FSR
±50 mV range (max)[6]	±0.8% of FSR
0-50 mV range (max)[6]	±0.8% of FSR
Linearity (max)[4]	±0.2% of FSR
Differential linearity[4]	±0.2% of FSR
Quantizing error	±1/2 LSB
Gain error (max)[4]	±0.1%
Offset error (max)[4]	±0.1% of FSR
Power supply sensitivity	
±15V	$\pm0.02\%/\%\Delta V_{CC}$
+5V	$\pm0.002\%/\%\Delta V_{CC}$
STABILITY OVER TEMPERATURE	
System accuracy drift[7] (max)	±40 ppm/°C
Linearity (max)	±20 ppm/°C
Monotonicity (0°C to +70°C)	Guaranteed
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microprocessor bus	
Output coding	Binary or Binary two's complement
Logic loading	All digital inputs are one LSTTL load
Output drive (D0 - D7)	5 TTL loads or 20 LSTTL loads
An analog input channel is selected by:	A0 - A3
The output data bus are read into:	D0 - D7
POWER REQUIREMENTS	
Rated voltages	±15V, +5V
Range for rated accuracy	4.75 to 5.25 and ±14.5 to ±15.5V
Supply drain ±15V	±30 mA
+5V	+90 mA
TEMPERATURE RANGE	0°C to +70°C

(1) Includes 35μsec for mux and amplifier time and 5μec for ADC conversion time.
(2) R_{ext} is an external resistor connected between pins 1 and 3.
(3) With power applied.
(4) With no external adjustments.
(5) FSR is Full Scale Range (FSR is 10V for ±5V range).
(6) Gain = 100 with external gain and offset trim.
(7) Includes gain drift, offset drift and linearity drift.

MECHANICAL





DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

NOTE: LEADS IN TRUE POSITION WITHIN .015" (.38mm) R AT MMC AT SEATING PLANE.

MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz) PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2) MATING CONNECTOR: 2350MC (Set of four 20 pin strips)

PIN CONNECTIONS

Pin		Pin	
1	IA GAIN ADJUST	41	A14
2	IA IN HI	42	R/$\overline{W}$
3	IA GAIN ADJUST	43	A15
4	MUX OUT HI	44	$\overline{INT}$
5	IN 7	45	VMA
6	IN 6	46	ϕ2
7	IN 5	47	$\overline{RESET}$
8	IN 4	48	HALT
9	IN 3	49	DELAY ADJ
10	IN 2	50	+5V
11	IN 1	51	DIG COM
12	IN 0	52	OUTPUT SELECT
13	MUX ENABLE 1	53	D7 (MSB)
14	MUX ENABLE 2	54	D6
15	SIN/DIF	55	D5
16	A0	56	D4
17	A1	57	D3
18	A2	58	D2
19	A3	59	D1
20	$\overline{A4}$	60	D0 (LSB)
21	$\overline{A4}$	61	-15V
22	$\overline{A5}$	62	-15V
23	$\overline{A5}$	63	COMP IN
24	$\overline{A6}$	64	ANA COM
25	$\overline{A6}$	65	BPO
26	$\overline{A7}$	66	R2 (ADC IN 1)
27	$\overline{A7}$	67	R1 (ADC IN 2)
28	$\overline{A8}$	68	IA OUT
29	$\overline{A8}$	69	IN 8 REF 0
30	$\overline{A9}$	70	IN 9 REF 1
31	$\overline{A9}$	71	IN 10 REF 2
32	$\overline{A10}$	72	IN 11 REF 3
33	$\overline{A10}$	73	IN 12 REF 4
34	$\overline{A11}$	74	IN 13 REF 5
35	$\overline{A11}$	75	IN 14 REF 6
36	$\overline{A12}$	76	IN 15 REF 7
37	$\overline{A12}$	77	MUX OUT LO
38	$\overline{A13}$	78	OFFSET NULL
39	$\overline{A13}$	79	IA IN LO
40	ADDR DECODE OUT	80	OFFSET NULL

PIN FUNCTIONS

IA GAIN ADJUST (Optional). Pin 1 and Pin 3. By connecting a resistor between pin 1 and 3 the gain of the internal instrumentation amplifier can be set as follows:

$$\text{Gain} = 2 + 50k\Omega/R_{ext}$$

Where R_{ext} is the gain setting resistor. The IA is factory adjusted for a gain of 2 without any external resistor.

Important: If a gain greater than 10 is required an external capacitor must be connected from "DELAY" (pin 49) to +5V. This increases an internal delay to allow for the increased settling time of the instrumentation amplifier. (See page 6-224)

IA IN HI Pin 2. This is the positive input of the internal instrumentation amplifier. This should be connected to pin 4 (MUX OUT HI) for normal operation.

MUX OUT HI Pin 4. This is the output of the analog input multiplexer. This is connected to pin 2 (IA IN HI) for differential operation. It is connected to pin 77 (MUX OUT LO) and pin 2 for single-ended input operation.

IN7 - IN0 Pins 5 - 12. The first 8 (of 16) analog inputs for single-ended operation or the 8 positive inputs for 8 channel differential input operation.

MUX ENABLE 1 Pin 13. Leave open for single-ended input operation. Connect to pin 14 (MUX ENABLE 2) for differential input operation.

MUX ENABLE 2 Pin 14. Connect to pin 15 (SIN/DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.

SIN/DIF Pin 15. Single/Differential input operation connect to pin 14 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.

A0 - A3 Pin 16 - 19. Address lines that select one of 16 analog input signals (IN0 - IN15). 0000 selects channel 0 and 1111 selects channel 15 when the correct address is presented to the MP21. Note: A3 should be connected to DIG COM for 8 channel differential input operation.

A4 - A15 Address lines. Pins 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 41, and 43. Connect to A4 - A15 of the 6800.

$\overline{A4}$ - $\overline{A13}$ Address select lines. Pin 21, 23, 25, 27, 29, 31, 33, 35, 37, and 39. By connecting these lines to DIG COM or +5 volts (through a 1kΩ resistor) any of 1024 address bands can be assigned to the MP21. For example, if $\overline{A4}$ is connected to GND., the correct (valid) address for A4 is a "1" (> + 2.4V).

ADDR DEC Pin 40. A positive pulse will appear when a valid address appears on the MP21 address lines and when R/$\overline{W}$ (pin 42), and $\phi 2$ (pin 46) and VMA (pin 45) are high. The rising edge of this pulse strobes the input channel select information (A0 - A3) into a latch. It can also be used for external purposes.

R/$\overline{W}$ Pin 42. Read/Write control line. Connect to R/$\overline{W}$ of 6800.

$\overline{INT}$ Pin 44. Interrupt output. Connect to $\overline{IRQ}$ or $\overline{NMI}$ of the 6800 if interrupt operation is desired. When conversion has been completed, a 10μsec pulse (negative) is generated on this line. (Not an open collector output.)

VMA Pin 45. Connect to VMA on 6800.

$\phi 2$ Pin 46. Connect to $\phi 2$ on 6800.

$\overline{RESET}$ Pin 47. A "Low" on this line is required to reset the MP21. Connect to the $\overline{RESET}$ input of the 6800.

$\overline{HALT}$ Pin 48. When the MP21 is "Read" by the microprocessor via any memory reference instruction the $\overline{HALT}$ line will go "Low" until conversion is complete. If the $\overline{HALT}$ line is used to halt the CPU, the 6800 will halt upon completion of the next instruction. When the multiplexer, instrument amp, and A/D converter have completed converting the analog data to a binary 8 bit code (40μsec with gain ≤ 10) the $\overline{HALT}$ line will then return to its "High" state which releases the processor. The output data can then be read with a second memory reference instruction. (Not an open collector output.)

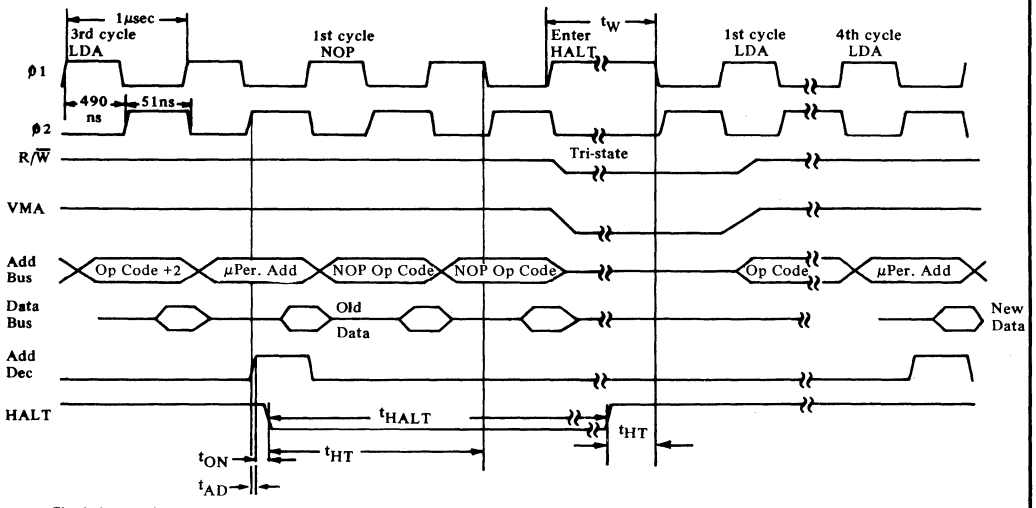
DELAY ADJ Pin 49. When the MP21 is addressed, an internal delay of approximately 35μsec is initiated to allow for multiplexer and instrumentation amplifier settling time. When the IA is operated with gain > 10 this delay must be increased (see Figure 4) to allow for the increased settling time of the IA. This is done by adding a capacitor between pin 49 and +5V. (See Figure 5)

+5V Pin 50. +5 volt at 140 mA maximum, 90 mA typical.

DIG COM Pin 51. Digital common. This pin should be connected to analog common (pin 64) as close to the MP21 as possible for optimum performance.

OUTPUT SELECT Pin 52. This pin should be connected to DIG COM to obtain binary data at D0 - D7. To obtain two's complement data (bipolar mode) connect pin 52 to +5V through a 1kΩ resistor.

D7 - D0	Pin 53 - 60. 8 bit data bus. 3-state low power Schottky TTL compatible.
-15V	Pin 61. -15 volt at 30 mA typical.
+15V	Pin 62. +15 volt at 30 mA typical.
COMP IN	Pin 63. Comparator input of 8 bit A/D converter (successive-approximation). Leave open for unipolar operation or connect to "BPO" (pin 65) for bipolar operation. NOTE: This point is extremely sensitive to noise. Any connection to this line should be as short as possible and shielded by ANA COM or ±15 volt supply patterns.
ANA COM	Pin 64. Analog common should be connected to digital common (pin 51) as close to the MP21 as possible for optimum performance.
BPO	Pin 65. A/D converter bipolar offset. It should be connected to ANA COM (pin 64) for unipolar operation or COMP IN (pin 63) for bipolar operation.
R2	Pin 66. A/D converter input resistor. Connect to IA out (pin 68) for 0 to +5V input unipolar operation or ±2.5V input bipolar operation. Leave open for ±5V input bipolar operation.
R1	Pin 67. A/D converter input resistor. Connect to IA out for ±5 volt operation. Connect to Pin 63 for 0 to +2.5V and ±1.25V ranges.
IA OUT	Pin 68. Instrumentation amplifier output. Connect to R1 (pin 67) or R2 (pin 66) for normal operation.
IN8-IN15 RET0-RET7	Pin 69-76. Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
MUX OUT LO	Pin 77. Multiplexer output for IN8-IN15 or RET0-RET7. Connect to "MUX OUT HI" (pin 4) and "IA IN HI" (pin 2) for single-ended input operation or connect to "IA IN LO" (pin 79) for differential input operation.
OFFSET NULL	Pin 78, 80. Optional instrumentation amplifier offset adjust (see Figure 1).
IA IN LO	Pin 79. Negative input of instrumentation amplifier. Connect to ANA COM (pin 64) for single-ended input operation or "MUX OUT LO" (pin 77) for differential input operation.



Clock freq. = 1 Mhz

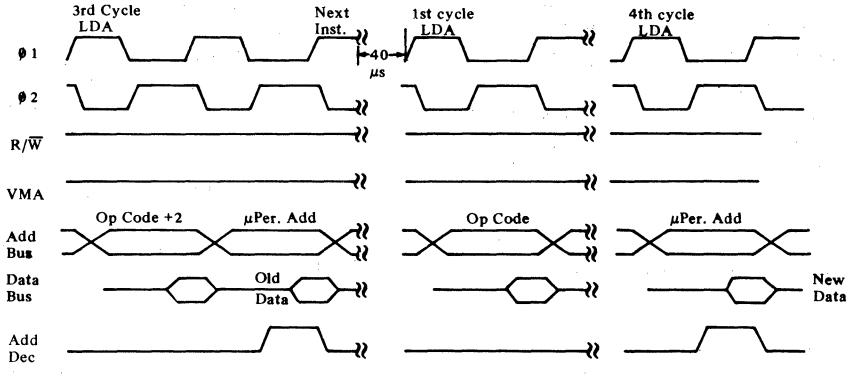
t_{HT} = 200ns min before falling edge of ϕ1

t_{HALT} = 40μsec (max)

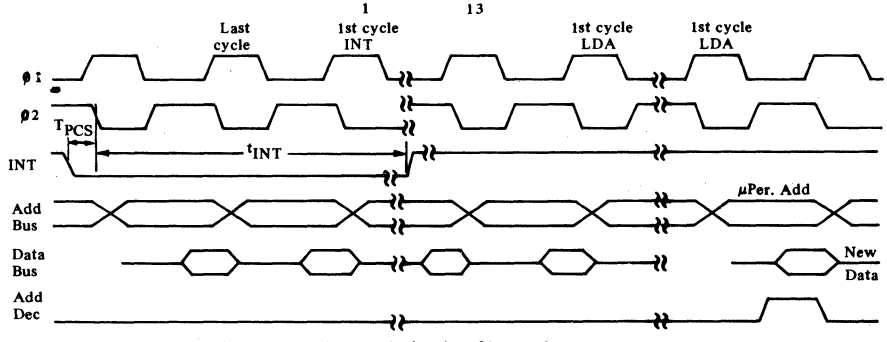
t_{ON} = 70nsec (max)

t_{AD} = 30nsec (max)

MP21 Timing Diagram (using HALT to stop microprocessor during conversion).



MP21 Timing Diagram (without stopping microprocessor during conversion).



t_{PCS} = 200ns min before falling edge of next to last φ2 clock pulse of instruction

t_{INT} = 12μsec (max)

MP21 Timing Diagram (using Interrupt).

OPERATING INSTRUCTIONS

PROGRAMMING

The MP21 is easily programmed since it is treated as memory. It uses any memory reference instruction that can read data.

The MP21 can be operated in four modes:

1) Start data conversion, halting the microprocessor for the 40μsec* conversion time. This is the simplest approach. It should be used if 40μsec of software time is available. (MP21's $\overline{\text{HALT}}$ line, pin 48, connected to the 6800's $\overline{\text{HALT}}$ input, pin 2.)

Example: LDA XXXX starts conversion of channel at location XXXX
NOP CPU halts at the end of this instruction
LDA XXXX transfers data from channel at location XXXX to accumulator

2) Start data conversion, then go to a different part of the program. When 40μsec* or more have passed, come back to the MP21 to read the converted data. This mode uses the least amount of time; it should be used when software time is at a minimum. (MP21's $\overline{\text{HALT}}$ line, pin 48, is open.)

Example: LDA XXXX starts conversion of the channel at location XXXX
•
•
• } at least 40μsec* of software here
LDA XXXX transfers data from channel at location XXXX to accumulator

* The conversion time of the MP21 may be between 40 and 200 microseconds depending upon the gain of the internal instrumentation amplifier. See Figure 4.

3) Start data conversion, then go to a different part of the program. Periodically, check the MP21's $\overline{\text{HALT}}$ line (pin 48) to detect if conversion is complete. This mode should

be used if a positive check of a complete conversion is needed. (MP21's $\overline{\text{HALT}}$ line, pin 48, could be interfaced to a 6820 PIA for instance.)

Example: LDA $XXXX starts conversion of channel at location XXXX

•
•
• } other software

LDA $YYYY } loop to determine if conversion is complete
AA ANDA $ZZ } YYYY is location of 6820 PIA with $\overline{\text{HALT}}$ information; ZZ is mask used for determining if end of conversion bit is set
BEQ AA
LDA $XXXX transfers data from channel at location XXXX to accumulator

4) Start conversion, then go to a different part of the program. The MP21 will interrupt at the end of conversion. The interrupt mode is very useful when the MP21 is at high gains with conversion times longer than 40μsec, see Figure 4.(MP21's $\overline{\text{INT}}$ line, pin 44, connected to the 6800's $\overline{\text{IRQ}}$ line, pin 4.)

Example: MP21 used with a 6800. MP21 base address 92E0. Processor halted operation. Read and Print the value of all 16 input channels and then stop.

```
                        NAM    MP21
     E0BF    OUT2H      EQU    $E0BF
     F1D1    OUTEEE     EQU    $E1D1
     E1AC    INEEE      EQU    $E1AC
0100                    ORG    $100
0100 CE 92E0 START      LDX    #$92E0    Base address for MP21
0103 5F                 CLR B            Clear Counter
0104 A6 00   CONV       LDA A,X          Initiate Conversion
0106 01 01              NOP
0107 A6 00              LDA A, X         Read Data
0109 FF 0137            STX    STRE1     Store Index Reg.
010C F7 0139            STA B  STRE2     Store Counter
010F B7 013B            STA A  STRE3     Store Data
0112 CE 013B            LDX    #STRE3
0115 BD E0BF            JSR    OUT2H     Print Data
0118 86 0D              LDA A  #$0D
011A BD E1D1            JSR    OUTEEE
011D 86 0A              LDA A  #$0A
011F BD E1D1            JSR    OUTEEE
0122 F6 0139            LDA B  STRE2
0125 FE 0137            LDX    STRE1
0128 5C                 INC B            Next Channel
0129 C1 10              CMP B  #$10      Have 16 channels been
                                         read?
012B 27 04              BEQ    STOP      Yes
012D 08                 INX
012E 7E 0104            JMP    CONV      Do another conversion
0131 BD E1AC STOP       JSR    INEEE     Input character
                                         to begin again
0134 7E 0100            JMP    START
0137 0002    STRE1      RMB    2
0139 0001    STRE2      RMB    1
013A 0001    STRE3      RMB    1
                        END
```

This program assumes that the system is under the control of the MIK BUG monitor, Revision 9. To read and print the value of all 16 channels again, input any character from the keyboard.

ADDRESS SELECTION

The base address of the MP21 is set by inputs $\overline{\text{A4}}$ through $\overline{\text{A13}}$. Address lines A4 through A13 respond to the inverse of inputs $\overline{\text{A4}}$ through $\overline{\text{A13}}$. For instance, if $\overline{\text{A6}}$ is grounded, A6 will respond to a "High" input. A14 and A15 are internally connected to respond to a "High" input.

ANALOG INPUT RANGE SELECTION

The MP21 may be set for any range between ±5V and ±10 mV. Table I shows the pin connections for the various high level ranges available.

MP21 Input Range	Gain	ADC Range	Pin Connections
±5V	2	±10V	65 to 63; 66 open; 67 to 68
±2.5V	2	±5V	65 to 63; 66 to 68; 67 open
±1.25V	2	±2.5V	65 to 63; 66 to 68; 63 to 67
0 - 5V	2	0 - 10V	65 to 64; 66 to 68; 67 open
0 - 2.5V	2	0 - 5V	65 to 64; 66 to 68; 63 to 67

Table I. Analog Input Range Pin Connections

The MP21 may be set to output data with straight binary coding (pin 52 grounded) or two's complement coding (pin 52 to +5VDC through a 1kΩ resistor). Straight binary coding is typically used with unipolar input ranges and two's complement coding with bipolar input ranges. Table II describes the coding.

The internal instrumentation amplifier is factory-set for a gain of 2. This gain can be increased to 250 by adding an external resistor (R_{ext}) between pins 1 and 3. R_{ext} should be a stable resistor (10 ppm/°C) since this temperature drift will add to the accuracy temperature coefficient. The gain of the amplifier can be determined by this formula: $\text{Gain} = 2 + \frac{50\text{k}\Omega}{R_{ext}}$. With pins 1 and 3 open, the gain is 2.

Since the amplifier input offset will be multiplied by the amplifier gain, an offset adjust may be required at high gains (see Figure 1b).

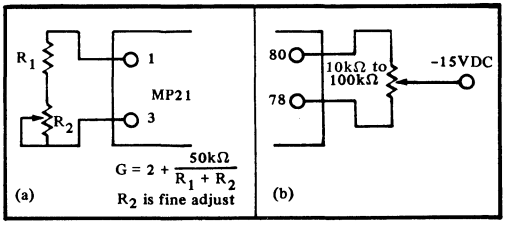


FIGURE 1. (a) MP21 Gain Adjust; (b) Offset Adjust

SINGLE-ENDED VS. DIFFERENTIAL INPUTS

The MP21 analog inputs may be connected as single-ended, differential or pseudo-differential. Single-ended operation may be used for high level (over one volt full scale) signals in low noise environments (Figure 3). Differential operation will reject common-mode noise appearing on both inputs (Figure 2). It should be used in noisy environments or with any low level signal (less than one volt). In the pseudo-differential mode, the MP21 is

	DIGITAL OUTPUT		ANALOG INPUT		
Straight Binary Code	Two's Complement Code		±5V	0 to +5V	±10mV
1111 1111 (FF_{16})	0111 1111 ($7F_{16}$)	+Full Scale	+4.961V	+4.980V	+9.92mV
1000 0000 (80_{16})	0000 0000 (00_{16})	Mid-Scale	0.000V	2.500V	0.000V
0000 0000 (00_{16})	1000 0000 (80_{16})	-Full Scale	-5.000V	0.000V	-10.00mV
		One LSB	39mV	19.5mV	78μV

TABLE II. Analog Input Values

connected as for the single-ended mode in Figure 3 except the IA low input, pin 79, is not grounded. Pin 79 is connected to an external ground that is common to all of the analog inputs. In cases with a noisy remote ground where little noise will be picked up between sensor and MP21, the pseudo-differential mode may be used.

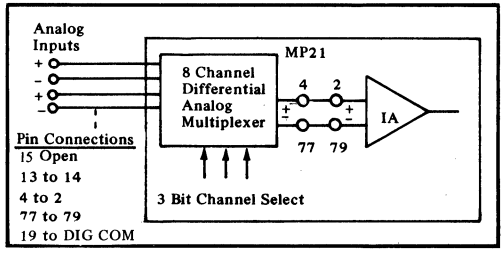


FIGURE 2. Differential Input Connections

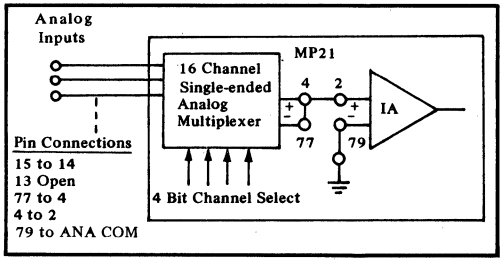


FIGURE 3. Single-ended Input Connections

DELAY TIMING

A delay time between channel selection and start of conversion is built into the MP21 to allow the analog multiplexer and instrumentation amplifier (IA) time to settle before starting the A/D converter. As the gain of the amplifier is increased, the settling time required increases. The factory set delay time (35μsec) is sufficient for gains of up to 10. At higher gains, a capacitor must be added from pin 49 to the +5 VDC supply to increase the delay time. Figure 4 shows the settling time of the MP21 vs. gain. Figure 5 shows the value of capacitance required to increase the delay.

The only external factor, other than gain, that affects the MP21 settling time is the impedance of the source connected to a channel. Figure 6 shows a circuit model of an "ON" channel.

The signal at the output of the multiplexer must be allowed to settle to ±0.1% (six time constants) to maintain the full accuracy of the system. The multiplexer time constant can be calculated with the formula: $\tau = (R_s + R_{on} + R_{on}^*)C_o$. For $R_s = 1k\Omega$ and $C_o = 50pF$, $\tau = (1.5+1)$ $k\Omega \times 50pF = 125ns$ (single-ended operation). Thus 0.75μs is needed to settle to ±0.1%. For high input impedances requiring more than 10 microseconds for multiplexer settling time, the required delay time may be calculated with this formula: $T_D = \sqrt{T^2_{mux} + T^2_{IA}}$, where T_{mux} is the settling time of the multiplexer and T_{IA} is the settling time of the instrumentation amplifier as shown in Figure 4. If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitance across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5μF is sufficient. For such a capacitance the multiplexer time constant becomes 80ns.

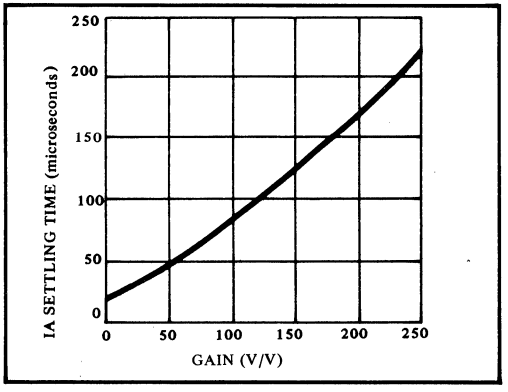


FIGURE 4. Typical IA Settling Time vs. Gain (Output Settling to ±0.1%).

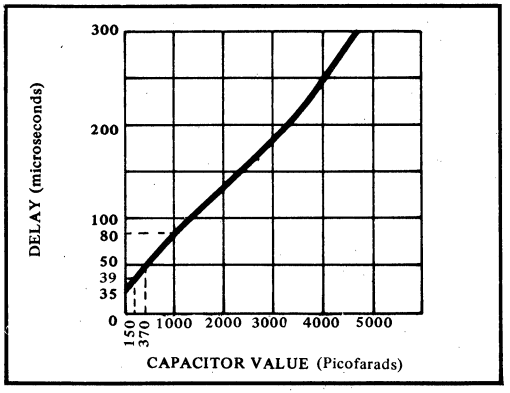


FIGURE 5. Typical Delay Time vs. Capacitor Value.

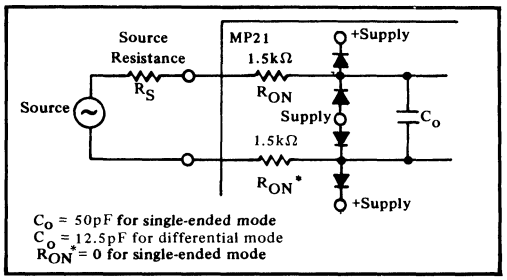


FIGURE 6. "ON" Channel Circuit Model.

INPUT OVERVOLTAGE PROTECTION

As shown in Figure 6, the analog inputs have reverse biased diode circuits which protect from damage by overvoltage (such as static). It is still advisable to take precautions against static discharge. The same circuitry protects the inputs from steady-state overvoltage damage during operation. The MP21's overvoltage protection can be increased by adding series resistors at each input. The input resistance must limit the current flowing through the input protection diodes to 10mA. For instance, if 15kΩ resistors are added to each input, the protection is increased to 165V (16.5kΩ x 10mA). Increased input resistance will, of course, increase the amount of time necessary for the multiplexer to settle as described in the previous section and increase the offset voltage by the drop caused when the bias current passes through this resistance.

NON 6800 OPERATION

The circuitry used to enable the 3-state output lines (D7 - D0) and begin conversion on the MP21 can be connected in such a way as to meet a wide variety of timing requirements. The output is enabled only when a valid address appears on the address inputs and when VMA (pin 45), R/$\overline{W}$ (pin 42), and ϕ2 (pin 46) are high. Any other combination of digital signals on these lines will result in D7 - D0 being in a high impedance state (see Figure 7).

All that is required to use the MP21 with a system other than a 6800, is that these signals be brought to their active levels. When this occurs, operation begins as previously described. Applications using the MP21 with other processors are shown in Figure 10 and 11.

RESET

It is important to reset the MP21 on startup with a low pulse on the $\overline{\text{RESET}}$ line (pin 47). The reset pulse clears an internal flip-flop and guarantees that the next read instruction to the unit will start a conversion. Thereafter, every other read instruction will initiate a conversion as previously described.

HIGHER SPEED OPERATION

The MP21's internal instrumentation amplifier requires 35 microseconds to allow for settling time. If this internal amplifier is not used, substantial improvements in throughput rate can be obtained. This is easily done since neither the inputs nor the output of the instrument amplifier are internally connected. The total delay time necessary may be calculated by this formula:

$$T_D = \sqrt{T^2_{MUX} + T^2_{IA}},$$

where T_{MUX} is the settling time of the multiplexer (750ns) and T_{IA} is the settling time of the instrument amplifier. For a T_{IA} of 1μsec we have T_D = 1.3μsec. Using 3μsec for the delay time to allow for unit to unit variation, the total throughput time will be 8μsec (including 5 microseconds for ADC conversion time) or 125 kHz. A resistor between pin 49 and +5 VDC will reduce the delay time from the factory set value of 35 microseconds (see Figure 8).

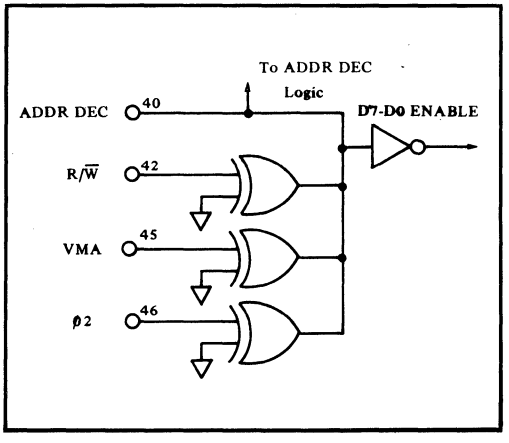


FIGURE 7. Output Enable Circuitry

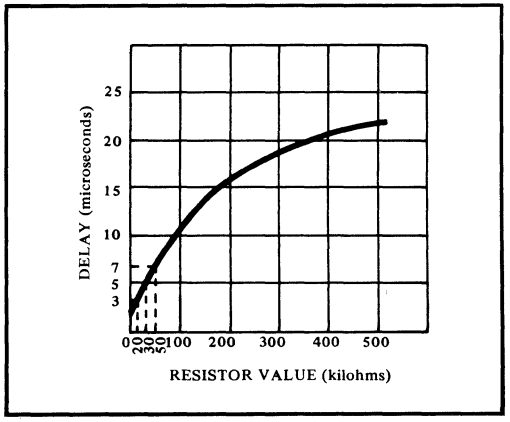


FIGURE 8. Typical Resistor Value to Decrease Delay Time.

CALIBRATION

The MP21 is laser trimmed at the factory to ±0.4% accuracy when using the ±5V, ±2.5V, ±1.25V, 0 to +2.5V or 0 to +5V ranges. If one of these ranges is used, no adjustments are required. For other ranges ($G \neq 2$), both the gain and offset must be adjusted. Figure 1 shows the adjustment connections. The offset adjustment should be made such that the transition to minus full scale output (0000 0001 to 0000 0000 for straight binary) occurs with an input of negative full scale plus 1/2 LSB. One least significant bit (LSB) is equal to the full scale range (FSR) divided by 2^n where n is the number of bits of the A/D converter. For the MP21, 1 LSB is $FSR/2^8 = FSR/256$. The gain adjustment should be made such that the transition to a full scale output (1111 1110 to 1111 1111 for straight binary) occurs with an input of positive full scale less 1/2 LSB. Since 128 states are used for negative inputs and one state is used for zero, only 127 states are available for the remaining positive range. Thus the positive full scale voltage is 1 LSB less than nominal full scale. For a range of ±50 mV, 1 LSB = 100 mV/256 = 0.39 mV. The gain adjustment should be made at +49.61mV* -(0.5)(0.39 mV) = +49.42 mV. The offset adjustment should be made at -50 mV + (0.5)(0.39mV) = -49.80 mV. Table III shows offset and gain calibration values for typical ranges.

* (50mV - 1 LSB = 49.61mV)

MP21 Input Range	Instrument Amp Gain	ADC Range	Calibration Values	
			Offset	Gain
±5V	2	±10V	-4.980V	+4.941V
0 to +5V	2	0 to +10V	+9.8mV	+4.971V
±2.5V	2	±5V	-2.490V	+2.471V
0 to +2.5V	2	0 to +5V	+4.9mV	+2.485V
±1.25V	2	±2.5V	-1.245V	+1.235
0 - 50mV	100	0 to +5V	+98μV	+49.7mV
±25mV	100	±2.5V	-24.9mV	+24.7mV
0 - 25mV	200	0 to +5V	+49μV	+24.9mV

Table III. Calibration Values.

The following program may be used to adjust gain and offset.

```
                        ORG  $100
START   0100    86      LDA A #$64
                64
        0102    B7      STA A COUNT
                01
                1A
        0105    4F      CLR A           Clear Accumulators.
        0106    5F      CLR B
CONV    0107    B6      LDA A $92 E0    Begin Conversion.
                92
                E0
        010A    01      NOP
        010B    B6      LDA A $92 E0    Read Data.
                92
                E0
        010E    81      CMP A #REF      Is Data = REF?
                REF
        0110    26      BNE AA          No. Do not count.
                01
        0112    5C      INC B           Yes. Do count.
AA      0113    7A      DEC COUNT       Have 100 conversions
                                        been done.
                01
                1A
        0116    26      BNE CONV        No. Do another.
                EF
        0118    20      BRA START       Yes. Begin next run.
                E6
COUNT   011A            RMB  1
                        END
```

This program assumes that the program is under control of the Motorola EXORciser EXbug monitor. If the Mikbug monitor is available, the following printout software may be added by using it to replace all codes starting from location 0118. In addition the references to count at 0104 and 0115 must be replaced with 2E.

```
OUT 2H  EQU  $E0   BF
OUT EEE EQU  $E1   D1

0118 F7     STA  B  STR0
     01
     2E
011B    CE     LDX  #STR0
        01
        2E
011E    BD     JSR  OUT 2H  Print no. of true conversions.
        E0
        BF
0121    86     LDA A  #0D
        0D
0123    BD     JSR  OUTEEE
        E1
        D1
012E           RMB  1          COUNT
012F           RMB  1          STR0
               END
```

This program may be used for both offset and gain calibration. The system offset should be adjusted first, followed by the gain adjustment.

The address of channel zero is assumed to be 92EO. If it is not, the LDA instructions should reflect that change. The reference values for Ref assume straight binary coding, Offset Ref = 00 and Gain Full Scale Ref = FF. For two's complement binary coding, Offset Ref = 80 and Gain Full Scale Ref = 7F.

A 100;G command to Exbug will begin program execution. For Mikbug the user's stack must be loaded with 1ØØ and then a G command executed to begin program execution. For those applications not using the printer portion of the program insert a breakpoint via a 118;V command. After 100 conversions have been made, the value (in hex) of the B accumulator will be printed if using Mikbug program. This value represents the number of times the data read from the board was equal to "REF" (00 for offset; FF for gain).

Calibration is performed by connecting a voltage source capable of 0.01% accuracy to input channel zero (this could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.01% DVM).

The offset adjustment is made first by using the appropriate offset calibration voltage and REF value. Run the calibration program and adjust the offset potentiometer until the B register contains a value between $1E_{16}$ and 46_{16} (30_{10} and 70_{10}).

To perform the gain adjustment, change the data labeled "REF" in the calibration program to its correct gain value. Set the input voltage to the correct value as shown in Figure 8 and adjust the gain potentiometer in the same manner as described for offset.

If EXbug is used the program will halt and the B accumulator can be examined from the program register display produced by the breakpoint.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the MP21 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60 Hz or higher frequencies. When the MP21 is used as an eight channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule, an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices cannot always be observed, a differential RC filter may be used. Figure 9 shows such a system.

The 10 kΩ resistors and 10μF capacitor provide low pass filtering (f_c = 0.8 Hz) while the optional 1 MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±5 volt range of the multiplexer. If the sensor is earth grounded, the 1MΩ resistors are not required. The 1 MΩ resistors do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias current of each input. See the overvoltage protection section for a discussion of the effects of the 10kΩ resistors in the input filter. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 9 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2 mV/°C.

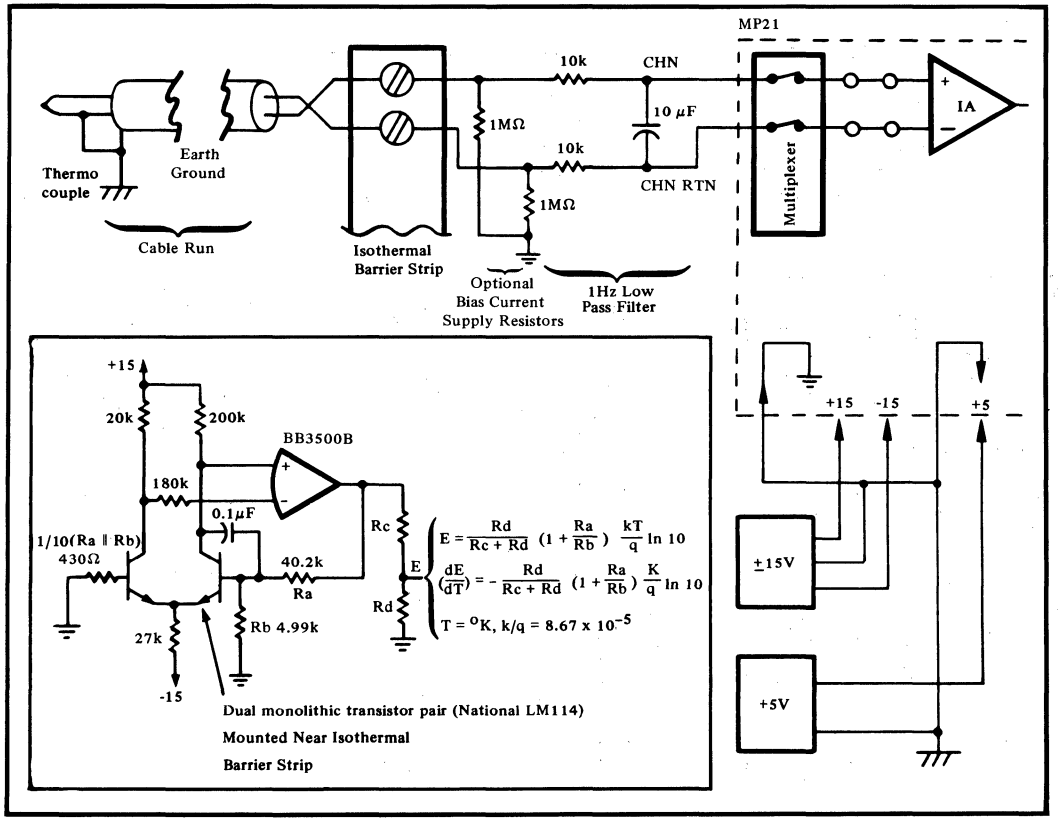


FIGURE 9. Thermocouple Input System Using MP21.

PIN CONNECTION SUMMARY

	JUMPER		JUMPER
Single-ended Multiplexer	4 to 2; 4 to 77; 79 to 64; 15 to 14; 13 open	Address Bus (A0 - A15)	Connect to 6800's address bus A0 - A15
Differential Multiplexer	4 to 2; 77 to 79; 13 to 14; 15 open	Address Select ($\overline{A4}$ - $\overline{A13}$)	Connect to +5V* or Ground
Amplifier	1 and 3 open for G = 2; R_{ext} between 1 and 3 for G ≠ 2.	Control Bus	42 to 6800's R/$\overline{W}$ (pin 39) 44 optionally to 6800's IRQ (pin 4) 45 to 6800's VMA (pin 5) 46 to 6800's Ø2 (pin 37) 47 to 6800's $\overline{RESET}$ (pin 40) 48 to 6800's $\overline{HALT}$ (pin 2) open for operation without halting CPU.
Input Range ±5V ±2.5V ±1.25V 0 - 5V 0 - 2.5V	 65 to 63; 66 open; 67 to 68 66 to 63; 66 to 68; 67 open 65 to 63; 66 to 68; 63 to 67 65 to 64; 66 to 68; 67 open 65 to 64; 66 to 68; 63 to 67		
Output Coding	52 to 51 for binary; 52 to 50* for two's complement.	Data Bus (D0 - D7)	Connect to 6800's data bus.

* Through a 1kΩ resistor.

MICROPROCESSOR INTERCONNECTION

The following diagrams show interconnections of the MP21 (described in this data sheet) and also of Burr-Brown's MP10 and MP11 analog output microperipherals (PDS-363) with Motorola's 6800, MOS Technology's 650X, and Fairchild's F-8. Although Burr-Brown's analog microperipherals are optimized for 8 bit microprocessors, with the addition of a few external components, they can be used with any 4 through 16 bit microprocessors.

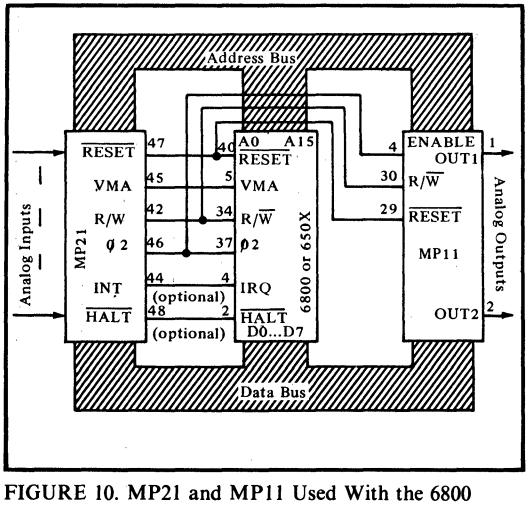


FIGURE 10. MP21 and MP11 Used With the 6800 or 650X.

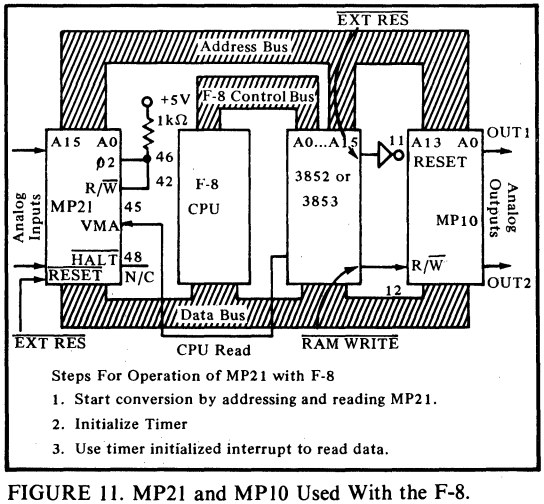
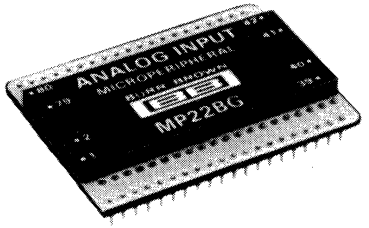


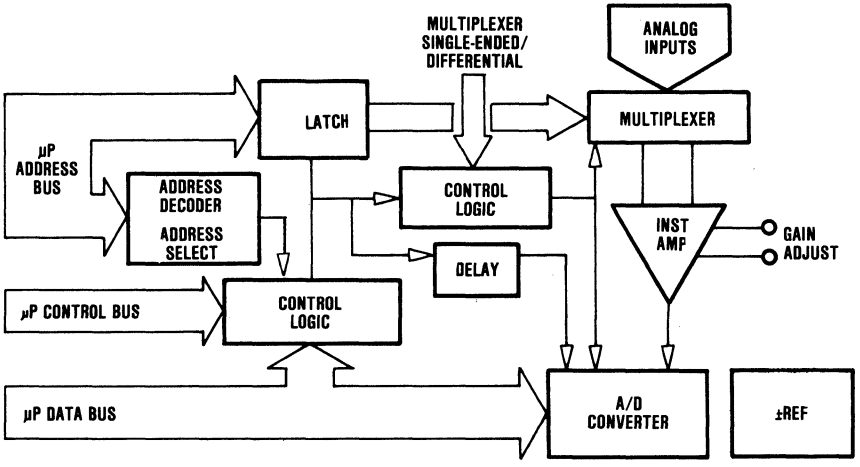
FIGURE 11. MP21 and MP10 Used With the F-8.

BURR-BROWN®



MP22BG

Microprocessor-Interfaced 12-BIT DATA ACQUISITION SYSTEM



FEATURES

- **INTERFACES WITH 8080A, 8048, Z-80, SC/MP MICROPROCESSORS WITHOUT ADDITIONAL COMPONENTS**
- **INTERFACES WITH 6800, 650X, F8, 8085 MICROPROCESSORS WITH MINIMAL EXTERNAL LOGIC**
- **EASY TO PROGRAM**
  One instruction acquires data as a memory mapped device
  Two instructions acquire data as an accumulator I/O device
- **COMPATIBLE WITH PDP-8, PDP-11, NOVA, ECLIPSE MINICOMPUTERS**

DESCRIPTION

A complete analog input system, the MP22 interfaces to most microprocessors without requiring additional external components. Contained in an 80-pin quad-in-line package, it includes a 12-bit CMOS A/D converter, instrumentation amplifier, input multiplexer that accepts up to 16 single-ended signals or 8 differential signals, an address decoder and control logic. Logic to generate interrupt, halt and direct memory access request signals are also included.

The system can digitize low level or high level analog signals. Gain of the internal instrumentation amplifier can be programmed with a single external resistor allowing input ranges as low as ±5mV.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-387A

Printed in U.S.A. July, 1978

ANALOG MULTIPLEXERS

Two 8-channel CMOS analog multiplexers are used on the input which permits selection of 16 single-ended or 8 differential inputs. A pseudo 16 channel differential mode of operation can also be achieved by connecting the amplifier's inverting input to a common, remote signal ground. Channels are addressed by the address decoder which is connected directly to the microprocessor address bus. The number of input channels can be expanded without limit using external multiplexers.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity and gain programming with an external resistor. Gain may be selected from unity to 500.

ANALOG-TO-DIGITAL CONVERTER

The 12-bit A/D converter is a CMOS, successive approximation device with 45μsec conversion time and three-state outputs. Laser-trimmed, compatible thin-film networks are used to assure linearity and stability over wide temperature ranges.

ADDRESS DECODER

Typical microprocessor systems have several thousand memory locations, teletype or CRT terminals, and possibly several MP22s. By using 12 address lines the microprocessor can communicate with as many as 2^{12} or 4096 memory locations or peripheral devices, with each having its own unique address.

The MP22's address decoder is made up of exclusive-or gates which have open collector outputs so that the outputs of several gates may be connected together through a single pull-up resistor. The address of the MP22 is determined by wiring the address select lines to either ground or +5 volts. Only when all of the address lines (A inputs) are in opposite states of their respective address select lines ($\overline{A}$ inputs) will the address decoder output go high.

DELAY TIMER

A time delay between channel selection and start of conversion is built into the MP22. This allows the analog multiplexer and the instrumentation amplifier time to settle before starting the A/D converter. As amplifier gain increases, settling time increases. See Figure 8. Factory set delay time (15μsec) is sufficient for gains from unity to 50. At higher gains a capacitor must be added between pins 49 and 50 to increase delay. Figure 7 indicates the capacitance required to increase delay time.

CONTROL LOGIC

The control logic generates signals to halt or interrupt the CPU while conversion takes place and to signal the CPU when conversion is complete and data can be read. Enable signals are also generated to gate the data onto the data bus.

REFERENCE

The internal voltage reference of the MP22 has been optimized for stable outputs with respect to temperature. Output current up to 2mA can be drawn externally from the reference outputs.

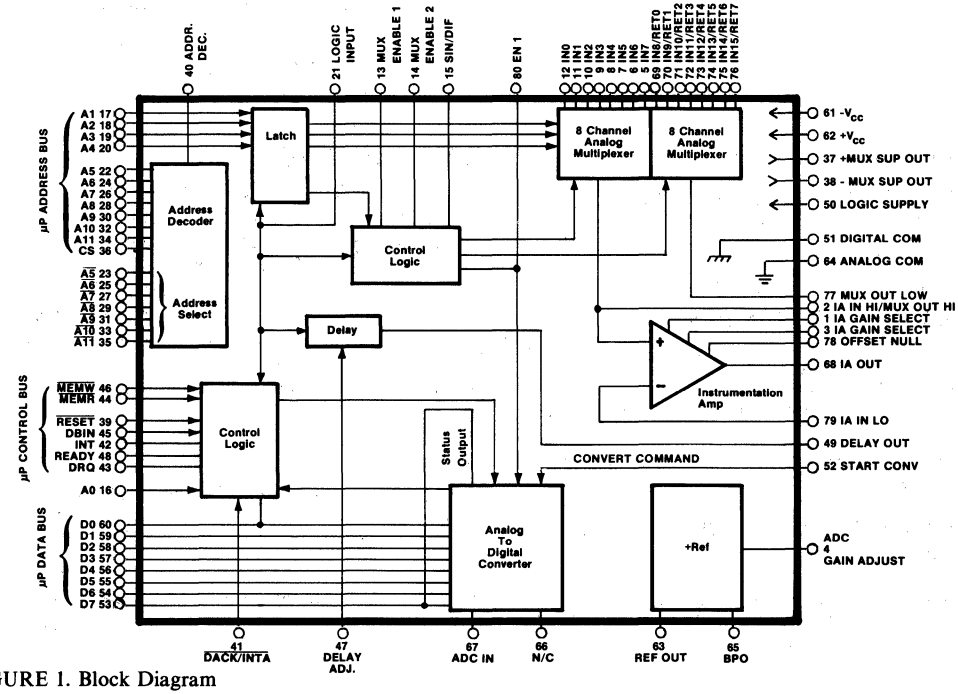
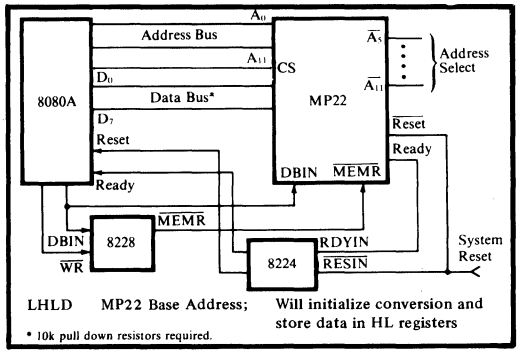


FIGURE 1. Block Diagram

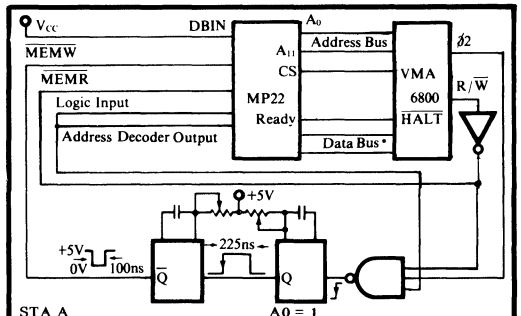
MICROPROCESSOR CONNECTION DIAGRAMS



LHLD MP22 Base Address; Will initialize conversion and store data in HL registers

* 10k pull down resistors required.

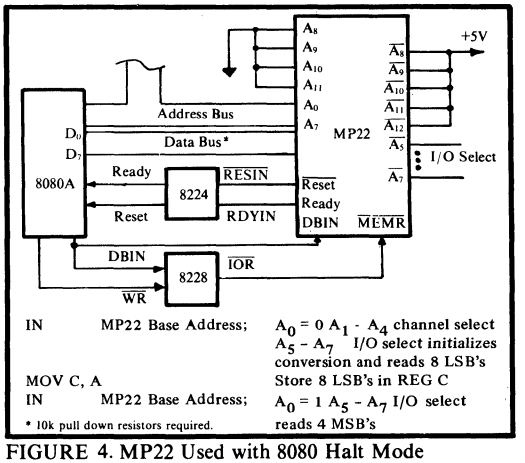
FIGURE 2. MP22 Used with 8080 Halt Mode Memory Mapped



STA A	A0 = 1	
Destination Address	D0 = 0	Starts conversion
NOP		Halt
LDA		
Destination Address	A0 = 0	8 LSB's, Resets MP22
LDA		
Destination Address	A0 = 1	4 MSB's

* 10k pull down resistors required.

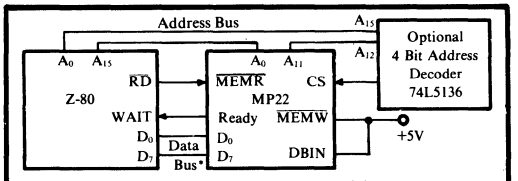
FIGURE 3. MP22 Used with 6800



IN	MP22 Base Address;	$A_0 = 0$ A_1 - A_4 channel select
		A_5 - A_7 I/O select initializes conversion and reads 8 LSB's
MOV C, A		Store 8 LSB's in REG C
IN	MP22 Base Address;	$A_0 = 1$ A_5 - A_7 I/O select reads 4 MSB's

* 10k pull down resistors required.

FIGURE 4. MP22 Used with 8080 Halt Mode Accumulator I/O



Program to READ and STORE 16 channels of data using Block Transfer Instruction.

LD HL, NN	NN points to channel 0 MP22
LD DE, MM	MM points to the first location of the destination
LD BC, 0100_H	byte counter (2 bytes/channel x 16) = 32_{10}
LDI	Load and increment

Total Execution Time with tcy = .4μs and conversion rate 40μs is T = 3 (4μs) + 16 (6.4 + 40μs) = 754.4μs.

* 10k pull down resistors required.

FIGURE 5. MP22 Used with Z-80 (Halt Mode)

DELAY TIME COMPONENT SELECTION CURVES

FIGURE 6. Typical Resistor Value to Decrease Delay Time

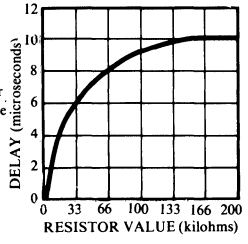
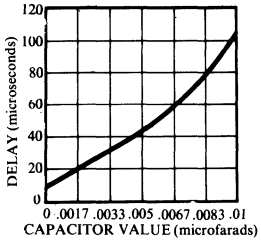


FIGURE 7. Typical Delay Time vs Capacitor Value



TYPICAL PERFORMANCE CURVES

FIGURE 8. Differential Amplifier Settling Time vs Gain

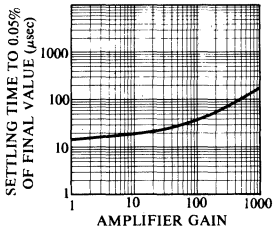
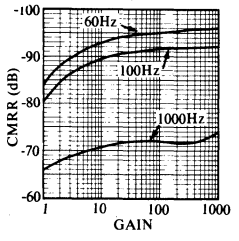


FIGURE 9. Differential Amplifier Common-mode Rejection vs Gain



ELECTRICAL SPECIFICATIONS

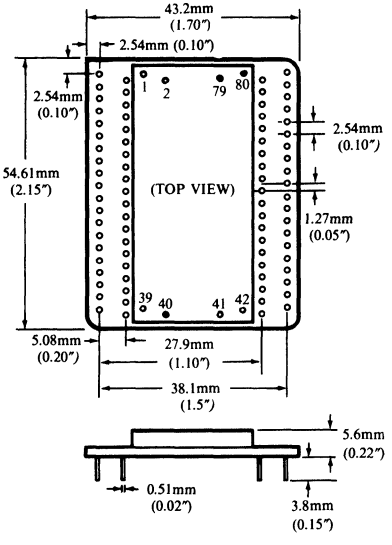
Typical at +25°C and rated supplies unless otherwise noted.

MODEL	MP22BG Min	MP22BG Typ	MP22BG Max	Units
TRANSFER CHARACTERISTICS				
Resolution[1]	12	12	12	Bits
Number of Channels		16 Single-Ended/8 Differential		
Throughput Rate[1] at G = 1	40	45	55	µs/Channel
ANALOG INPUTS				
ADC Gain Ranges				
Bipolar[3]		±5		Volts
Unipolar[1]		0-5		Volts
Amplifier Gain Range		1 to 500		
Gain Equation		$\left(1+\frac{25k\Omega}{R_{EXT}}\right)$		
Input Voltage Without Damage			±16	Volts
Input Voltage for Multiplexer Operation			±6.0	Volts
Input Impedance				
Off Channel		$5 \times 10^9\Omega$ || 10pF		
On Channel		$5 \times 10^9\Omega$ || 100pF		
Bias Current				
25°C			300	nA
0°C to +70°C			400	nA
Amplifier Output Noise G = 100, R_S = 1500		1.2		mV, rms
		7.0		mV, p-p
Amplifier Input Offset		±0.5	±7.0	mV
Amplifier Offset Drift (R_{max} = 1.5k)		±(7 + 90/G)	±(26 +190/G)	µV/°C
Amplifier Gain Drift, (R_{EXT} ≤10 ppm/°C)				
G = 1			10	ppm/°C
G = 10			110	ppm/°C
G = 100			120	ppm/°C
G = 1000			120	ppm/°C
Amplifier Settling Time to ±0.05% of FSR				
G = 1[1]			15	µs
G = 10		20		µs
G = 100		25		µs
G = 500		100		µs
CMRR for Differential Inputs Dc to 60Hz	74	84		dB
ACCURACY				
System RSS Accuracy[2] at 25kHz Throughput				
G = 1			±0.1	% FSR
Linearity			±0.05	% FSR
Differential Linearity		±0.05		% FSR
Gain Error		Adjustable to Zero		
Offset Error		Adjustable to Zero		
System RSS Accuracy at Gain = 500 and 1kHz Throughput			±0 39	% FSR
ADC Accuracy Drift				
Linearity			±3	ppm/°C
Gain			±10	ppm/°C
Reference Drift				
Ref Out (Pin 63)			±15	ppm/°C
BPO (Pin 65)			±25	ppm/°C
System Accuracy Drift (Excluding I.A.)				
Unipolar			±25	ppm/°C
Bipolar			±60	ppm/°C
Monotonicity (-25 to +85°C)		Guaranteed		
No Missing Codes (-25 to +85°C) (10 bits only)		Guaranteed		
Power Supply Sensitivity (Excluding I.A.)				
±V_{CC}			±0.008	% FSR/%ΔV
Logic Supply			±0.0002	% FSR/%ΔV
Instrumentation amplifier				
Power Supply Sensitivity			(1+2/G)10^{-4}	% FSR/%ΔV

MODEL	MP22BG Min	MP22BG Typ	MP22BG Max	Units
DIGITAL INPUT/OUTPUT				
Bipolar Code		Bipolar Offset Binary		
Unipolar Code		Unipolar Straight Binary		
Logic Loading Pin (21)			3LSTTL	
Pin (60)			2LSTTL	
Output Drive	1 TTL Load			
Analog Input Channels Selected By:		A1-A4		
Output Data:		D0-D7		
POWER REQUIREMENTS				
Rated Voltages[1]		±15, +5		Volts
Range for Rated Accuracy (Logic Supply, $\pm V_{cc}$)		4.75 to 5.25 and ±11.4 to ±15.75		Volts
$\pm V_{cc}$ Operating Range	±10		±18	Volts
Supply Drain				
$+V_{cc}$		10	20	mA
$-V_{cc}$		15	20	mA
Logic Supply		80	160	mA
Power Dissipation ($\pm V_{cc}$ = ±12V)		700	1300	mW
TEMPERATURE RANGE				
Specification	-25		+85	°C
Operating	-40		+100	°C
Storage	-55		+125	°C

NOTES: 1. These parameters are 100% tested.
2. Gain and offset adjusted to zero.
3. External amplifier required.

MECHANICAL



MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz.)
PINS: Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20 pin strips)
HERMETICITY: Fluorocarbon (gross leak)

PIN CONNECTIONS

Pin 1	IA GAIN SELECT	Pin 41	$\overline{\text{DACK/INTA}}$
2	IA IN HI/MUX OUT HIGH	42	INT
3	IA GAIN SELECT	43	$\overline{\text{DRQ}}$
4	ADC GAIN ADJUST	44	$\overline{\text{MEMR}}$
5	IN7	45	$\overline{\text{DBIN}}$
6	IN6	46	$\overline{\text{MEMW}}$
7	IN5	47	DELAY ADJ.
8	IN4	48	READY
9	IN3	49	DELAY OUTPUT
10	IN2	50	+5V LOGIC SUPPLY
11	IN1	51	DIG. COMMON
12	IN0	52	START CONV.
13	MUX ENABLE 1	53	D7 (MSB)
14	MUX ENABLE 2	54	D6
15	SIN/DIF	55	D5
16	A0	56	D4
17	A1	57	D3
18	A2	58	D2
19	A3	59	D1
20	A4	60	D0 (LSB)
21	LOGIC INPUT	61	-V_{cc}
22	A5	62	+V_{cc}
23	$\overline{\text{A5}}$	63	REF OUT
24	$\overline{\text{A6}}$	64	ANA. COMMON
25	$\overline{\text{A6}}$	65	BPO
26	A7	66	NO CONNECTION
27	$\overline{\text{A7}}$	67	ADC IN
28	A8	68	IA OUT
29	$\overline{\text{A8}}$	69	IN8 RET0
30	A9	70	IN9 RET1
31	$\overline{\text{A9}}$	71	IN10 RET2
32	A10	72	IN11 RET3
33	$\overline{\text{A10}}$	73	IN12 RET4
34	A11	74	IN13 RET5
35	$\overline{\text{A11}}$	75	IN14 RET6
36	CHIP SELECT (CS)	76	IN15 RET7
37	+MUX SUPPLY OUTPUT	77	MUX OUT LOW
38	-MUX SUPPLY OUTPUT	78	OFFSET NULL
39	$\overline{\text{RESET}}$	79	IA IN LO
40	ADDR DECODE	80	EN1

OPERATING INSTRUCTIONS

The MP22 is designed to be used as a memory-mapped or an accumulator I/O. Since there are many powerful memory reference instructions, the MP22 is used most efficiently as a memory-mapped device. Pins $\overline{A5}$ through $\overline{A11}$ are provided so that the microperipheral can be hardwired for any base address within a 4096 word block of the memory field. The address decoder output is available and can be easily expanded to 16 bits.

If used as a memory-mapped microperipheral, the MP22 can provide three modes of operation: HALT Mode, INTERRUPT Mode and DMA Mode.

More detailed application instructions are given in the operating manual, available upon request.

HALT MODE

After power up (or manual) reset, the MP22 is automatically set for operation in the HALT Mode. This mode requires minimum software to acquire data. To use the MP22 in the HALT Mode connect the MP22 READY line to the 8080 READY input (see Figure 2). When a memory reference instruction such as LHLD is executed, the READY line goes low, halting the CPU for the duration of the data conversion (45 μsec, gain = 1). When the conversion is complete the READY line goes high, signaling the CPU exit the wait state and enter the T_3 state to read the 8 LSB's. After reading the 8 LSB's, the CPU increments the memory address register and reads the 4 MSB's. When the most significant data byte has been read, the internal logic resets and the MP22 is ready for the next conversion.

Example:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	1	1	1	1	1	0	1	1	1	0	0	1	0
			MP22 Base Address								Channel Select				

MP22 used with 8080; read MP22 base address: $1F72_H$ channel 10.

LHLD $1F72_H$ acquires and transfers data to CPU from channel 10.

The 8 LSB's (at location $1F72_H$) are transferred to register L and the 4 MSB's (at location $1F73_H$) are transferred to register H.

Total time: 16 tcy + 40μsec = 47.8μsec (for tcy = 488 nsec [8080A]).

INTERRUPT MODE

To use the MP22 in the INTERRUPT Mode connect the INT and $\overline{DACK}/\overline{INTA}$ lines to the 8080's INT input and INTA output respectively. Conversion is initiated by writing D0 = 0 into the MP22. When the conversion is complete the MP22 generates an INT signal which will remain low until INTA is received from the 8080.

Example: MP22 base address $1F72_H$.

```
MVIA   00H                 START conversion
STA    1F72H
 .
 .                         Continue with program. INT will
 .                         arrive 40 µsec after start of conversion.
INCA
                           INT arrives here
CPIA                       User will jam RST instruction which
                           will provide address of an interrupt hand-
                           ling routine and store program counter.
INTERRUPT Subroutine:
        PUSH PSW           Store Acc. and Flags
        PUSH H  }
        PUSH D  }          Store reg. if necessary
        PUSH B  }
        EI                 Enable interrupt
        LHLD 1F72H         READ DATA from MP22
                           Channel 10 L = 8 LSB's
                                      H = 4 MSB's
                           Process data
        POP B   }
        POP D   }          Restore registers and flags
        POP H   }
        POP PSW            Restore program counter
        RET
```

The user must supply an instruction op code to the processor during the next DBIN time after the $\overline{INTA}$ status appears. This is usually done through use of an RST instruction.

DIRECT MEMORY ACCESS MODE

To use the MP22 in the DMA Mode connect the MP22 to the DMA controller. The controller is initialized by the CPU before reading data from the MP22. To accomplish a block move the CPU loads the 8257 with the starting address of the source block (the MP22 location) with A0 = 0 and the length of the block (L = 1) into channel 0. Channel 1 is programmed with the starting location of the destination block and the length (L = 1).

Next, start conversion by writing D0 = 0 into the MP22. When the conversion is complete, the MP22 will generate a DRQ request on channels 0 and 1. The 8257 is initialized to the rotating priority mode, therefore the first DMA cycle is from channel 0 which latches data from the first location of the source block into the 8212. The second cycle will be from channel 1 which will store the latched data in the first location of the destination block. The next cycle will return to channel 0 and the sequence will start over again until the terminal count is reached. When the terminal count for channel 1 is reached, $\overline{\text{DACK1}}$ and TC signals are generated and MP22 DRQ line is reset.

ANALOG INPUT RANGE SELECTION

The MP22 may be set for any range between ±5V and ±10mV. Pin connections for the high level ranges available are shown in Table I.

MP22 Input Range	Gain	ADC Range	Pin Connections
±5V	1	±5V	See bipolar operation
0 - 5V	1	0-5V	65, 63 open; connect 67 to 68

TABLE I. Analog Input Range Pin Connections

In the unipolar mode the MP22 output data is straight binary. In the bipolar mode it is bipolar offset binary. If two's complement output is needed an external three-state inverting buffer is required.

Gain of the internal instrumentation amplifier (without external gain adjust) is 1.0. This gain can be increased to any value between 1.0 and 500 by adding an external resistor between pins 1 and 3. This external resistor (R) should be stable (10 ppm/°C or better) because its drift will add to the system accuracy temperature coefficient. Gain of the amplifier is determined by this formula:

External resistor R_{ext} connected: Gain = $1 + 25k\Omega / R_{ext}$

Pins 1 and 3 open: Gain = 1.0 ±0.02%

OPERATION WITH BIPOLAR INPUT VOLTAGES

To operate the MP22 with bipolar input voltages of ±5V, connect the unit as shown in Figure 10. Amplifier A1 divides the magnitude of the input by two, and the connection of a 12.5kΩ resistor between pin 63 (ref out) and pin 78 (offset null) offsets the signal such that the A/D converter sees a unipolar voltage from 0 to +5V.

To null the gain and offset errors of this circuit, follow this procedure:

1. Input - 5.0000V to any MP22 channel.
2. Adjust R1 until a digital output of all zeros is obtained.
3. Input +4.99817V to that MP22 channel.
4. Adjust R2 until a digital output of $0FFF_H$ is obtained.

POWER SUPPLY CONSIDERATIONS

For best performance and noise rejection, power supplies should be decoupled with 1.0μf tantalum or electrolytic capacitors in parallel with 0.01μF ceramic capacitors. To insure proper power supply sequencing, a diode should be connected between the pins 50 and 62 with the anode connected to pin 50.

A 0.1μF ceramic capacitor is required on each of the lines +MUX SUPPLY OUT (pin 37) and -MUX SUPPLY OUT (pin 38). Each is tied from the respective pin to ground.

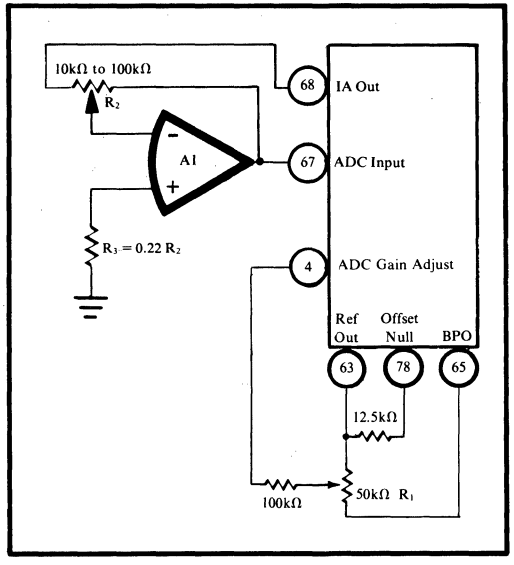


FIGURE 10. Connection for ±5V Input

	ANALOG INPUT			DIGITAL OUTPUT		
	±5V	0 to +5V	±5mV	OFFSET BINARY	STRAIGHT BINARY	TWO'S COMPLEMENT
+Full Scale	4.9975V	4.9988 V	4.9975 mV	FFF_H	FFF_H	$7FF_H$
Mid Scale	0.0000V	2.5000 V	0.0000	800_H	800_H	000_H
-Full Scale	-5.0000V	0.0000 V	-5.0000 mV	000_H	000_H	800_H
One LSB	2.44mV	1.22mV	2.44μV			

TABLE II. Analog Input, Digital Output Relationship

APPLICATIONS

DATA ACQUISITION FROM THERMOCOUPLE INPUTS

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of 10 to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the MP22 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60 Hz or higher frequencies. When the MP22 is used as an eight channel differential input system, the high common-mode rejection of the instrument amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule, an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices cannot always be observed, a differential RC filter may be used. Figure 11 shows such a system.

The 10 kΩ resistors and 10μF capacitor provide low pass filtering (f_c = 0.8 Hz) while the optional 1 MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the ±5 volt range of the multiplexer. If the sensor is earth grounded, the 1MΩ resistors are not required. The 1 MΩ resistors do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias currents of the two inputs. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 11 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2 mV/°C.

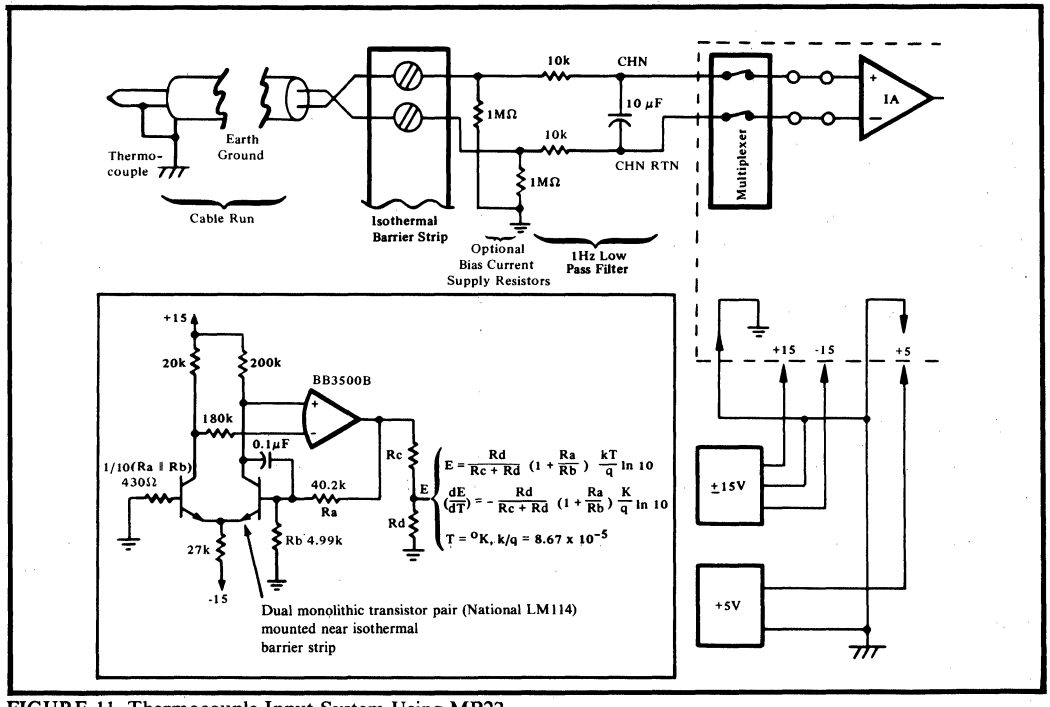
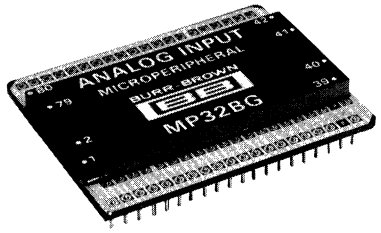


FIGURE 11. Thermocouple Input System Using MP22

BURR-BROWN®



MP32

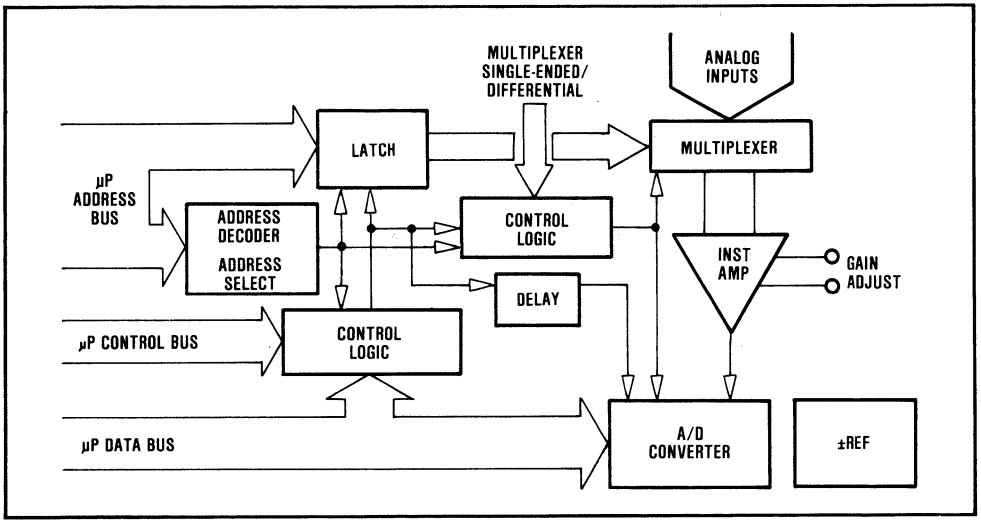
Microprocessor-Interfaced 12-BIT DATA ACQUISITION SYSTEM

FEATURES

- INTERFACES WITH 8080A, 8048, Z-80, SC/MP MICROPROCESSOR WITHOUT ADDITIONAL COMPONENTS
- INTERFACES WITH 6800, 650X, F8, 8085 MICROPROCESSORS WITH MINIMAL EXTERNAL LOGIC
- COMPATIBLE WITH PDP-8, PDP-11, NOVA, ECLIPSE MINICOMPUTERS
- EASY TO PROGRAM
  - One instruction acquires data as a memory-mapped device
  - Two instructions acquire data as an accumulator I/O device

DESCRIPTION

The MP32 is a complete analog input system and interfaces to many microprocessors without additional external components. Contained in an 80-pin quad-in-line package, it includes a 12-bit CMOS A/D converter, instrumentation amplifier, input multiplexer that accepts up to 16 single-ended signals or 8 differential signals, an addess decoder, and control logic. Logic to generate interrupt, halt, and direct memory access request signals is also included. The system can digitize low level or high level analog signals. Gain of the internal instrumentation amplifier can be programmed with a single external resistor allowing input ranges as low as ±10mV.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-424A

DESCRIPTION (CONT)

ANALOG MULTIPLEXERS

Two 8-channel CMOS analog multiplexers are used on the input which permits selection of 16 single-ended or 8 differential inputs. A 16-channel pseudo-differential mode of operation can also be achieved by connecting the amplifier's inverting input to a common, remote signal ground. Channels are addressed by the address decoder which is connected directly to the microprocessor address bus. The number of input channels can be expanded without limit using external multiplexers.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity and gain programming with an external resistor. Gain may be selected from unity to 500.

ANALOG-TO-DIGITAL CONVERTER

The 12-bit A/D converter is a CMOS, successive approximation device with 40μsec conversion time and three-state outputs. Laser-trimmed, compatible thin-film networks are used to assure linearity and stability over wide temperature ranges.

ADDRESS DECODER

The 12-bit address decoder has been included in the MP32 so the device can be uniquely specified within 4k bands of the address field. If further decoding is required, the chip select (CS) pin can provide a 13th bit or the output of an external decoder can be connected to the internal address decoder output "wired-AND" node.

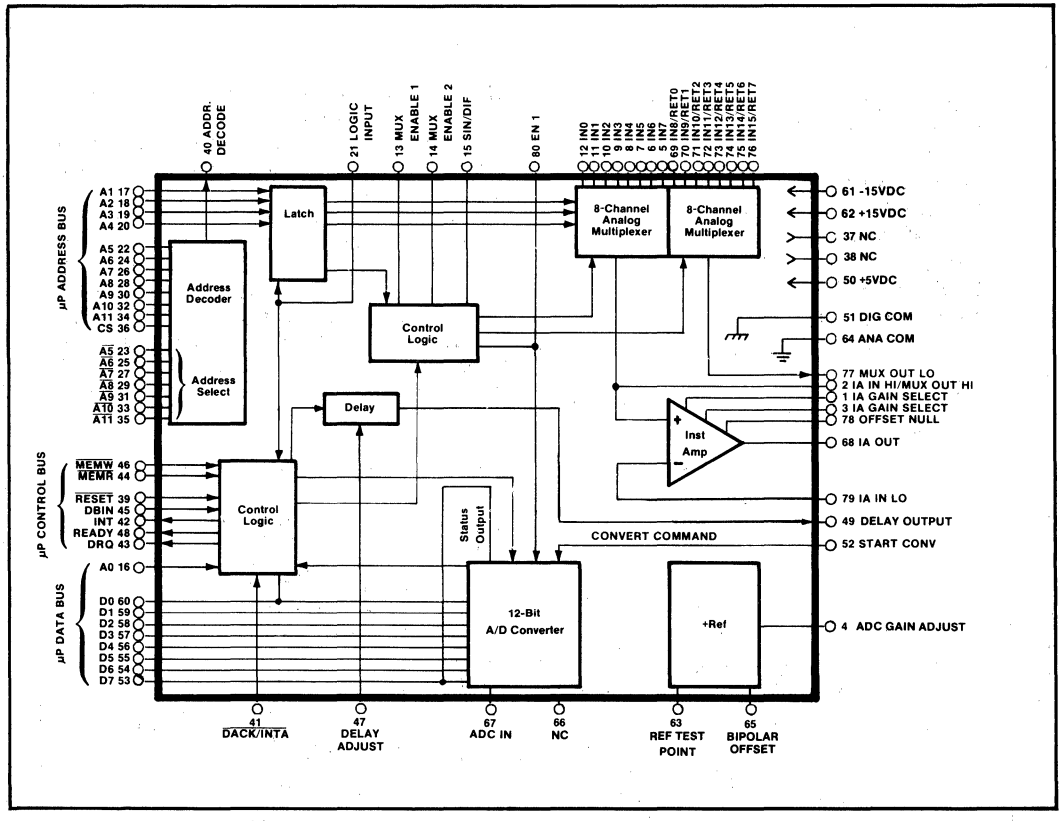


FIGURE 1. System Block Diagram.

DELAY TIMER

A time delay between channel selection and start of conversion is built into the MP32 and is described in detail in the Analog Input Configuration section.

CONTROL LOGIC

The control logic generates signals to halt or interrupt the CPU while conversion takes place and to signal the CPU when conversion is complete and data can be read. Enable signals are also generated to gate the data onto the data bus.

REFERENCE

The internal voltage reference of the MP32 has been optimized for stable outputs with respect to temperature. Output current up to 2mA can be drawn externally from the reference outputs.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated supplies unless otherwise noted.

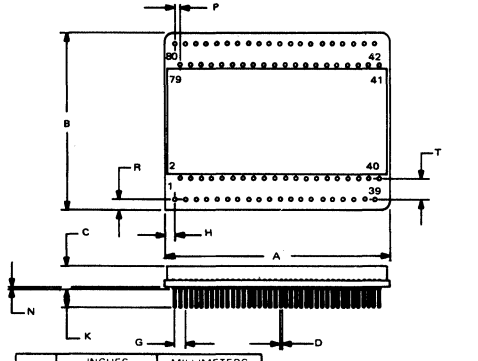
MODEL	MP32BG AND MP32CG MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS				
Resolution(1)	12	12	12	Bits
Number of Channels		16 Single-ended/8 Differential		
Throughput Rate(1) at G = 1	50	70	80	µsec/Channel
ANALOG INPUT/OUTPUT				
ADC Voltage Input Ranges(2)				
Bipolar(3)		±10		V
Unipolar(1)		0 to +10		V
Amplifier Gain Range		1 to 500		V/V
Gain Equation		1 + (25kΩ/R_{EXT})		
Input Voltage Without Damage			±35	V
Input Voltage for Multiplexer Operation			±10	V
Input Impedance				
Off Channel			10^{18}	Ω
On Channel		1.5	1.8	kΩ
Bias Current				
+25°C			300	nA
0°C to +70°C			400	nA
Amplifier Output Noise G = 100, R_S = 1500Ω		1.2		mV, rms
		7.0		mV, p-p
Amplifier Input Offset		±0.5	±7.0	mV
Amplifier Input Offset Drift (R_{source} = 1.5kΩ max)		±[7 + (90/G)]	±[26 + (190/G)]	µV/°C
Amplifier Gain Drift, (R_{EXT} ≤ 10ppm/°C)				
G = 1			±10	ppm/°C
G = 10			±110	ppm/°C
G = 100			±120	ppm/°C
G = 500			±120	ppm/°C
Amplifier Settling Time to ±0.01% of FSR				
G = 1(1)			15	µsec
G = 10		20		µsec
G = 100		25		µsec
G = 500		100		µsec
CMRR for Differential Inputs DC to 60Hz	80	84		dB
Instrumentation Amplifier				
Power Supply Sensitivity			[1 + (2/G)] 10^{-4}	% FSR/%ΔV
ACCURACY				
System RSS Accuracy(4) at 25kHz Throughput				
G = 1, BG			±0.05	
CG			±0.025	
Linearity, BG			±0.025	% FSR
CG			±0.0125	% FSR
Differential Linearity, BG		±0.025		% FSR
CG		±0.0125		% FSR
Gain Error		Adjustable to Zero		
Offset Error		Adjustable to Zero		
System RSS Accuracy at 1kHz Throughput				
G = 500			±0.39	%FSR
ADC Accuracy Drift				
Linearity			±3	ppm/°C
Gain			±10	ppm/°
Reference Drift				
Ref Out (Pin 63)			±15	ppm/°C
Bipolar Offset (Pin 65)			±25	ppm/°C
System Accuracy Drift (Excluding IA)				
Unipolar			±25	ppm/°C
Bipolar			±60	ppm/°C
No Missing Codes (-25°C to +85°C)(Bits 1 thru 12)CG		Guaranteed		
(Bits 1 thru 11)BG		Guaranteed		

ELECTRICAL (CONT)

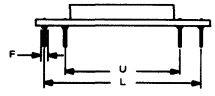
MODEL	MP32BG AND MP32CG			
	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (Excluding IA)				
±15VDC			±0.008	% FSR/%ΔV
+5VDC			±0.0002	% FSR/%ΔV
DIGITAL INPUT/OUTPUT				
Biopolar Code		Bipolar Offset Binary		
Unipolar Code		Unipolar Straight Binary		
Logic Loading Pin (21)			3LSTTL	
Logic Loading Pin (60)			2LSTTL	
All Other Digital Inputs			1LSTTL	
Output Drive	1TTL Load			
Analog Input Channels Selected By:		A1-A4		
Output Data		D0-D7		
POWER REQUIREMENTS				
Rated Power Supply Voltages(1)		±15, +5		VDC
Power Supply Ranges for Rated Accuracy		+4.75 to +5.25 and ±11.4 to ±15.75		VDC
Power Supply Operating Range (±15VDC only)	±10		±18	VDC
Supply Drain				
+15VDC		10	20	mA
-15VDC		15	20	mA
+5VDC		80	160	mA
Power Dissipation (at rated supplies)		700	1300	mW
TEMPERATURE RANGE				
Specification	-25		+85	°C
Operating	-40		+100	°C
Storage	-55		+125	°C

NOTES:
1. These parameters are 100% tested. 2. Input voltage must be kept 2V below supply voltage. 3. External amplifier required. 4. Gain and offset adjust to zero.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	



NOTE:
LEADS IN TRUE POSITION WITHIN 0.015" (0.38mm) R @ MMC AT SEATING PLANE.

Pin numbers shown for reference only. Numbers may not be marked on package.

MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz.)
MATING CONNECTOR: 2350MC (set of four 20 pin strips)

PIN ASSIGNMENTS

	Pin No.		
IA GAIN SELECT	1	41	$\overline{\text{DACK/INTA}}$
IA IN HI/MUX OUT HI	2	42	$\overline{\text{INT}}$
IA GAIN SELECT	3	43	$\overline{\text{DRQ}}$
ADC GAIN ADJUST	4	44	$\overline{\text{MEMR}}$
IN7	5	45	$\overline{\text{DBIN}}$
IN6	6	46	$\overline{\text{MEMW}}$
IN5	7	47	DELAY ADJUST
IN4	8	48	READY
IN3	9	49	DELAY OUTPUT
IN2	10	50	+5VDC
IN1	11	51	DIG COM
IN0	12	52	START CONV
MUX ENABLE 1	13	53	D7 (MSB
MUX ENABLE 2	14	54	D6
SIN/DIF	15	55	D5
A0	16	56	D4
A1	17	57	D3
A2	18	58	D2
A3	19	59	D1
A4	20	60	D0 (LSB
LOGIC INPUT	21	61	-15VDC
$\overline{\text{A5}}$	22	62	+15VDC
$\overline{\text{A5}}$	23	63	REF TEST POINT
$\overline{\text{A6}}$	24	64	ANA COM
$\overline{\text{A6}}$	25	65	BIPOLAR OFFSET
$\overline{\text{A7}}$	26	66	NC
$\overline{\text{A7}}$	27	67	ADC IN
$\overline{\text{A8}}$	28	68	IA OUT
$\overline{\text{A8}}$	29	69	IN8/RET0
$\overline{\text{A9}}$	30	70	IN9/RET1
$\overline{\text{A9}}$	31	71	IN10/RET2
$\overline{\text{A10}}$	32	72	IN11/RET3
$\overline{\text{A10}}$	33	73	IN12/RET4
$\overline{\text{A11}}$	34	74	IN13/RET5
$\overline{\text{A11}}$	35	75	IN14/RET6
CHIP SELECT ($\overline{\text{CS}}$)	36	76	IN15/RET7
NC	37	77	MUX OUT LO
$\overline{\text{NC}}$	38	78	OFFSET NULL
$\overline{\text{RESET}}$	39	79	IA IN LO
ADDR DECODE	40	80	EN1

DESCRIPTION OF PIN FUNCTIONS

NUMBER	DESIGNATION	DESCRIPTION
Pins 1 and 3	IA GAIN SELECT	(Optional). By connecting a resistor between pins 1 and 3, the gain of the internal instrumentation amplifier can be varied as follows: Gain = 1 + (25kΩ/R) where R is the gain setting resistor. Gain can be set from 1 to 500. Important: If a gain greater than 50 is required, an external capacitor must be connected from DELAY ADJUST (pin 47) to +5VDC (pin 50). This increases an internal delay to allow for the increased settling time required by the instrumentation amplifier.
Pin 2	IA IN/HI MUX OUT HI	This is the positive input of the internal instrumentation amplifier, and the "high side" of the multiplexer. For differential operation this pin is left open. For single-ended operation connect pin 2 to pin 77 and pin 79 to pin 64.
Pin 4	ADC GAIN ADJUST	This pin is used to adjust gain of the ADC (see Figures 6 and 7). If no external gain adjustment is needed, this pin is left open.
Pins 5 thru 12	IN7-IN0	The first 8 (of 16) analog inputs for single-ended operation or the 8 positive inputs for 8-channel differential input operation.
Pin 13	MUX ENABLE 1	Leave open for single-ended operation. Connect to MUX ENABLE 2 (pin 14) for differential input operation.
Pin 14	MUX ENABLE 2	Connect to SIN/DIF (pin 15) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.
Pin 15	SIN/DIF	Connect to MUX ENABLE 2 (pin 14) for single-ended operation. Leave open for differential input operation.
Pin 16	A0	In the Halt Mode A0 = "0" and $\overline{\text{MEMR}}$ = "0" will start conversion and enable 8LSB's; A0 = "1" enables 4MSB's. At the start of conversion, the output registers are not cleared.
Pins 17 thru 20	A1-A4	Address lines that select one of 16 analog input signals (IN0-IN15). 0000 selects channel 0 and 1111 selects channel 15 when the correct address is presented to the MP32. A4 is connected to DIG COM (pin 51) for differential operation.
Pin 21	LOGIC INPUT	Connect to pin 40. See signal description under pin 40.
Pins 22,24,26, 28, 30, 32, 34, 36	A5-A11, CS	Address lines. When the proper address is presented to the MP32, the internal logic is enabled for conversion or data output. CS is used as a chip select or the most significant address bit. It must be "1" to enable the unit.
Pins 23, 25, 27, 29, 31, 33, 35	$\overline{\text{A5-A11}}$	Address select lines. These lines are used to program the address decoder to respond to a particular address. This is done by connecting these pins to +5VDC or ground such that the bit pattern is the complement of the desired address that appears on the corresponding bit lines.
Pin 37	NC	No connection.
Pin 38	NC	No connection.
Pin 39	$\overline{\text{RESET}}$	A "low" on this line is required to RESET the MP32. Connect to system reset line.
Pin 40	ADDR DECODE	A positive pulse will appear when a valid address appears on the MP32 address lines. This pin is usually connected to LOGIC INPUT (pin 21). The rising edge of this pulse strobes the input channel select information (A1-A4) into an internal latch. It can also be used by the user for other system timing.
Pin 41	$\overline{\text{DACK/INTA}}$	In the Interrupt Mode, this pin is connected to the microprocessor interrupt acknowledge pin. This is an active low signal. If not used, connect to +5VDC through a 1kΩ resistor.
Pin 42	INT	In the Interrupt Mode, this signal is connected to the microcomputer system interrupt. Once the conversion is completed the MP32 generates an INT signal which will remain high until an $\overline{\text{INTA}}$ signal is received from the microcomputer. This is an open-collector LSTTL signal and must be pulled up with an external resistor.
Pin 43	DRQ	In the DMA Mode, this pin is connected to the direct memory access request line of the microcomputer system. Once conversion is complete, the MP32 will generate a DRQ signal which will remain high until $\overline{\text{DACK}}$ is received.
Pin 44	$\overline{\text{MEMR}}$	Memory read. A "low" pulse on this line is used to start a conversion in the Halt Mode. If not used, connect to +5VDC through a 1kΩ resistor.
Pin 45	DBIN	Connect the DBIN on 8080A. If used with any other microprocessor, connect through 1kΩ resistor to +5VDC.
Pin 46	$\overline{\text{MEMW}}$	Memory write. A "low" pulse on this line along with D0 = 0 will start conversion in the Interrupt or DMA Modes provided that LOGIC INPUT (pin 21) is "1". If not used, connect to +5VDC through a 1kΩ resistor.
Pin 47	DELAY ADJUST	When the IA is operated with gain greater than 50, the delay time must be increased (see Figure 11) to allow for the increased settling time of the IA.
Pin 48	READY	In the Halt Mode connect this output signal to the input that will cause the microprocessor to enter the "Wait" state (such as the READY input on the 8080). A logic "0" causes the microprocessor to halt to allow time for the analog circuitry to settle and the conversion to be completed (70μsec with gain ≤ 50). After conversion, the READY line will return to logic "1" which releases the microprocessor from the "Wait" state. The output data then appears on the data bus.
Pin 49	DELAY OUTPUT	When the MP32 is addressed, an internal delay of approximately 15μsec is initiated to allow for multiplexer and instrumentation amplifier settling time. Pin 49 must be connected to START CONV (pin 52). This point may be connected to a sample/hold control input if an external S/H is used.
Pin 50	+5VDC	+5VDC at 160mA, max.
Pin 51	DIG COM	Digital commmon. This pin should be connected to ANA COM (pin 64) as close to the MP32 as possible for optimum performance.
Pin 52	START CONV	This pin should be connected to DELAY OUTPUT (pin 49).
Pins 53 thru 60	D7-D0	8-bit data bus. Tri-state low power Schottky TTL-compatible.
Pin 61	-15VDC	-15VDC at 20mA, max.
Pin 62	+15VDC	+15VDC at 20mA, max.
Pin 63	REF TEST POINT	Test point for reference testing.
Pin 64	ANA COM	Analog common. This should be connected to DIG COM (pin 51) as close to the MP32 as possible for optimum performance.
Pin 65	BIPOLAR OFFSET	+5VDC voltage reference output. 2mA can be supplied from this pin without degradation.

DESCRIPTION OF PIN FUNCTIONS (CONT)

NUMBER	DESIGNATION	DESCRIPTION
Pin 66	NC	No connection.
Pin 67	ADC IN	A/D converter input. Connect to IA OUT (pin 68). If external S/H used, connect to S/H output.
Pin 68	IA OUT	Instrumentation amplifier output. Connect to ADC IN (pin 67) for normal operation. If external S/H used, connect to S/H input.
Pins 69 thru 76	IN8/RET0 -IN15/RET7	Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
Pin 77	MUX OUT LO	Multiplexer output for IN8/RET0 - IN15/RET7. Connect to IA IN HI/MUX OUT HI (pin 2) for single-ended input operation or connect to IA IN LO (pin 79) for differential input operation.
Pin 78	OFFSET NULL	Instrumentation amplifier offset adjust (see Figures 5, 6, and 7).
Pin 79	IA IN LO	Negative input of the instrumentation amplifier. Connect to ANA COM (pin 64) for single-ended input operation or MUX OUT LO (pin 77) for differential input operation.
Pin 80	ENI	Output signal which enables 4MSB's. See Figure 14 for utilization to obtain two's complement. For a straight binary output this pin is left open.

OPERATING INSTRUCTIONS

ADDRESSING MODES

In the memory-mapped addressing mode, the MP32 is regarded as a block of memory locations, each with its own unique address. Since the output data word is 12 bits long, it requires two address locations for each word.

The MP32 is connected to the microprocessor just as though it were memory, using the memory control lines. The address word format is illustrated in Figure 2. Address bits A5 through A12 (A12 is connected to CS, or CS can be used as a chip select) identify a particular MP32 unit. The bit pattern of A5 through A12 is selected by the user by connecting inputs $\overline{A5}$ through $\overline{A12}$ to logic 1 or logic 0. A1 through A4 select the particular analog input channel. A0 is used as a byte select (see Description of Pin Functions). The byte select bit is sequenced as specified in the discussion on operational modes. The advantage of using memory-mapped addressing is the flexibility of programming. All of the many memory reference instructions can be used to control MP32 operation.

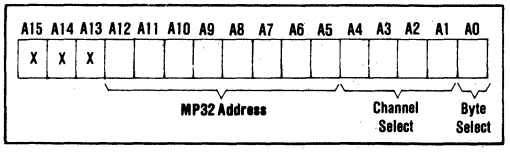


FIGURE 2. Address Word Format

Input/Output Addressing

Input/output addressing is accomplished by considering the MP32 as an input/output or peripheral device. Thus the I/O control signals are used to operate the unit. The addressing scheme is the same as that described in the Memory-Mapped Addressing section. The user may be forced to use I/O addressing if all of the available memory addresses have been taken up with memory or other memory-mapped devices.

Address Expansion

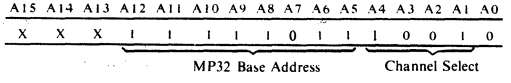
The 8-bit MP32 base address (A5 through A11 and CS) enables one of 256 bands of locations in the address field. The top 3 bits of the 16-bit microprocessor address bus are not used by the MP32. If it is necessary to expand the addressing capability to include these 3 additional bits, the output of an external 3-bit address decoder can be used in conjunction with the ADDR DECODE signal output of the MP32, to provide the LOGIC INPUT signal required by the MP32.

OPERATIONAL MODES (Memory-Mapped)

Halt Mode

After powerup (or manual) reset, the MP32 is automatically set for operation in the Halt Mode. This mode requires minimum software to acquire data. To use the MP32 in the Halt Mode connect the MP32 READY line to the 8080 READY input (see Figure 15). When a memory reference instruction such as LHLD is executed, the READY line goes low, halting the CPU for the duration of the data conversion (50μsec, gain = 1). When the conversion is complete the READY line goes high, signaling the CPU to exit the wait state and enter the T_3 state to read the 8LSB's. After reading the 8LSB's, the CPU increments the memory address register and reads the 4MSB's. When the most significant data byte has been read the internal logic resets and the MP32 is ready for the next conversion.

Example:



MP32 used with 8080; read MP32 base address: 1F72H channel 9.
LHD 1F72H acquires and transfers data to CPU from channel 9.
The 8LSB's (at location 1F72H) are transferred to register L and the 4MSB's (at location 1F73H) are transferred to register H.
Total time: 16tcy + 50μsec = 57.8μsec (for tcy = 488nsec 8080 A)

Interrupt Mode

To use the MP32 in the Interrupt Mode connect the INT and $\overline{DACK}$/INTA lines to the 8080's INT input and

$\overline{\text{INTA}}$ output respectively (see Figure 16). Conversion is initiated by writing D0 = into the MP32. When the conversion is complete the MP32 generates an INT signal which will remain low until $\overline{\text{INTA}}$ is received from the 8080.

Example: MP32 base address 1F72H

```
MVI A,0H    00H
STA         1F72H       START conversion
 .
 .                       Continue with program. INT will
 .                       arrive 50μsec after start of conversion.
 .                       INT arrives here
 .                       User will generate RST instruction
 .                       (usually done with an 8227) which
 .                       will provide the address of an
 .                       interrupt handling routine and store
 .                       program counter.
INTERRUPT Handler:
    PUSH PSW            Store acc. and flags
    PUSH H  }
    PUSH D  }           Store reg. if necessary
    PUSH B  }
    EI                  Enable interrupt
    LHLD 1F72H          READ DATA from MP32
                        Channel 10 L = 8LSB's
                                   H = 4MSB's
                        Process data
    POP B   }
    POP D   }           Restore registers and flags
    POP H   }
    POP PSW             Restore program counter
    RET
```

Polled Mode

The electrical connections for the Polled Mode are the same as that for the Halt Mode, except that the MP32 READY line is not connected.

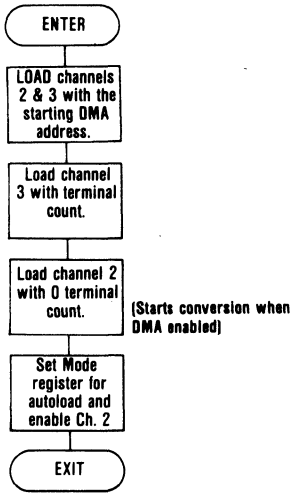
Programming in the Polled Mode is also similar to that of the Halt Mode except that after starting the conversion with a memory reference instruction, the program continues to run. After sufficient time has elapsed for the completion of the conversion, the most significant data byte is read. If the MSB is set, the conversion is still in progress. When it has been determined that the conversion has been completed, the least significant, and then the most significant data bytes are read. Reading of the data will begin a new conversion which may either be ignored or it can access the next analog channel of interest. In either case, the data from the first conversion will not be affected.

Direct Memory Access Mode

Data from the MP32 can be updated automatically and stored in a dedicated part of system memory by using the Direct Memory Access (DMA) mode of operation. Figure 3 illustrates the DMA connection for an 8080 microprocessor. Since the MP32 address decoder is not needed for this mode of operation it can be used to provide address selection for the DMA controller (model 8257). This interface is designed to operate on the I/O bus.

The following program can be used to operate the DMA interface. Any number of adjacent MP32 channels can be cycled repeatedly by inserting the desired memory starting address and the terminal count into the program.

Programming For DMA Operation




```
ENTER:  MVI A, XX   ;Load Channel 2 with DMA Starting Address
        OUT X4H
        MVI A, YY
        OUT X4H
        MVI A, XX   ;Load Channel 3 with DMA Starting Address
        OUT X6H
        MVI A, YY
        OUT X6H
        MVI A, XX   ;Load Channel 3 with Terminal Count
        OUT X7H
        MVI A, 0
        OUT X7H
        MVI A, 0    ;Load Channel 2 with 0 Terminal Count
        OUT X5H
        MVI A, 0
        OUT X5H
        MVI A, 84H  ;Set Mode Reg. for Autoload and enable Channel 2
        OUT X8H
```

The interface is designed to always start on analog input channel 0. The interface requires one pass through all channels to intialize. The data put in memory through this initial pass will most likely be erroneous and should be disregarded.

OPERATIONAL MODES (Input/Output)

Each memory-mapped operational mode can also be used on the I/O bus. When used with the I/O bus the appropriate address lines and timing signals (i.e., $\overline{\text{I/OR}}$ instead of $\overline{\text{MEMR}}$) must be applied. In addition, the appropriate READ and WRITE instructions must be used. For the 8080 this would mean substituting the following sequence for LHLD XXXXH:

```
IN XXH
MOV L, A
IN XX+1H
MOV H, A
```

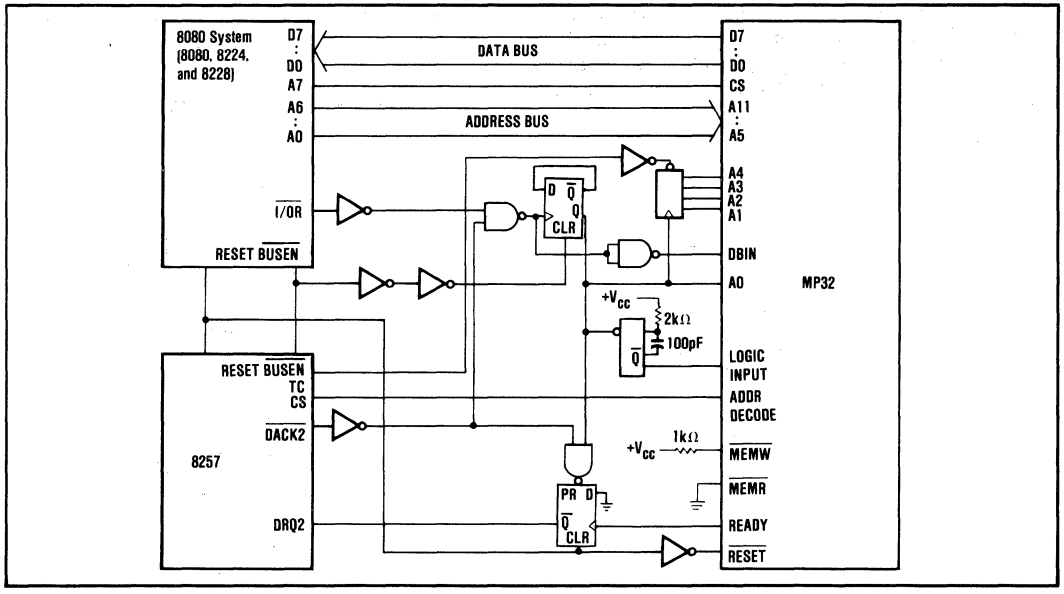


FIGURE 3. MP32 / 8080 Connection for DMA Operation (I/O Mapped).

TIMING

The internal timing diagram and timing constraints of the MP32 are shown in Figure 4 and Table I. The MP32 is compatible with any digital system that can operate within the timing constraints shown.

ANALOG INPUT CONFIGURATION

UNIPOLAR AND BIPOLAR OPERATION

The MP32 will convert either unipolar or bipolar voltage inputs. Unipolar input ranges vary from +10mV to +10V (full scale). Bipolar ranges are from ±10mV to ±10V. For bipolar input signal ranges from ±5V to ±10V, an external amplifier is used to divide the input signal by 2 and an offset is introduced to give a 0 to +5V input to the ADC. Use the connection diagram shown in Figure 5. For bipolar input signal ranges of ±5V down to ±10mV, the external amplifier is not used. Use the connection diagram shown in Figure 6.

TABLE I. MP32BG/CG Timing Diagram Parameters.

Symbol	Parameter	Min	Max	Unit
t_{ad}	Delay - Valid Addr. to Addr. Decoder Out		30	nsec
t_{rr}	Delay - $\overline{MEMW}$ to DELAY Out		128	nsec
t_{rr}	Delay - $\overline{MEMR}$ to DELAY Out		98	nsec
t_{delay}	Analog Settling Time	10	1000	µsec
t_R	Delay - DELAY to READY Out		52	nsec
$t_{conversion}$	Total Channel Conversion Time	45	55	µsec
t_D	Delay - End of Conversion to DRQ		25	nsec
t_I	Delay - End of Conversion to INT		70	nsec
t_{Da}	Delay - $\overline{DACK/INTA}$ to DRQ Out		60	nsec
t_{Ia}	Delay - $\overline{DACK/INTA}$ to INT Out		75	nsec

The unipolar input connection diagram is shown in Figure 7. Table II gives a summary of circuit configurations for several input ranges.

TABLE II. Analog Input Configurations.

Input Range	IA Gain	Circuit Configuration	Delay Adjust Required
±10V	1	Figure 5	No
±7.5V	1.33	Figure 5	No
±5V	1	Figure 6	No
±1.0V	5	Figure 6	No
±100mV	25	Figure 6	No
±20mV	250	Figure 6	Yes
0 to +10V	1	Figure 7	No
0 to +5V	2	Figure 7	No
0 to +20mV	500	Figure 7	Yes

INSTRUMENTATION AMPLIFIER GAIN SELECTION

The internal instrumentation amplifier gain may be set to any value between 1 and 500 by connecting an external gain resistor between pins 1 and 3. With the pins open the gain is 1 ±0.02%. The gain of the amplifier is determined by: $G = 1 + (25k\Omega/R_{ext})$, where R_{ext} is the gain resistor value. The external resistor should be stable (10ppm/°C or beter) since its drift will add to the gain temperature coefficient.

SINGLE-ENDED VERSUS DIFFERENTIAL INPUTS

The MP32 analog inputs may be connected in single-ended, differential, or pseudo-differential configurations. Single-ended operation may be used for high level (over 1V full scale) signals in low noise environments (see Figure 8). Differential operation will reject common-mode noise that appears on both inputs (see Figure 9). It should be used in noisy environments or with any low level signal (less than 1V). In the pseudo-differential mode, the MP32 is connected the same as single-ended

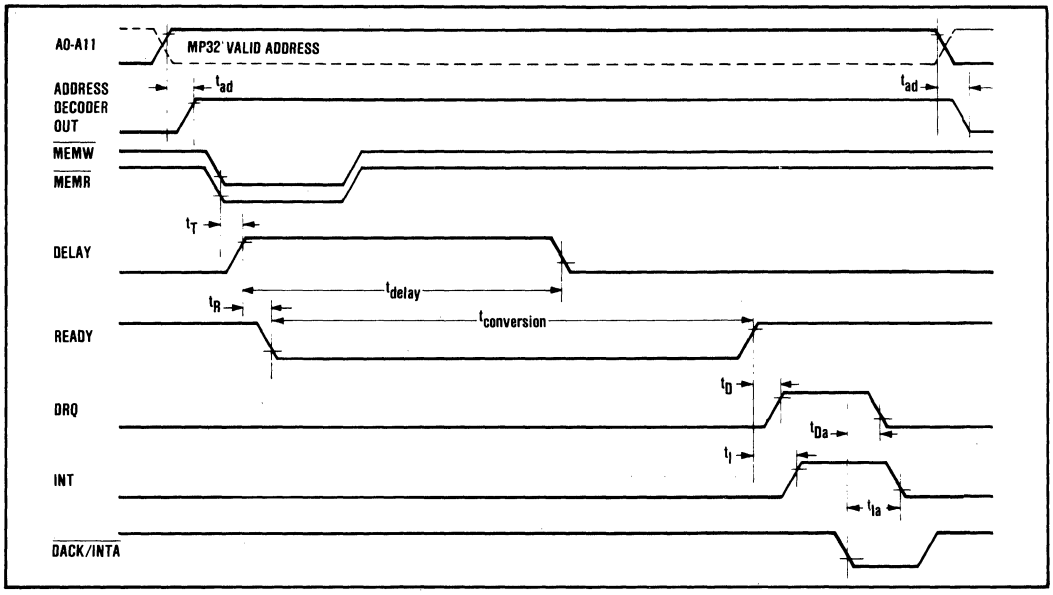


FIGURE 4. MP32 Timing Diagram.

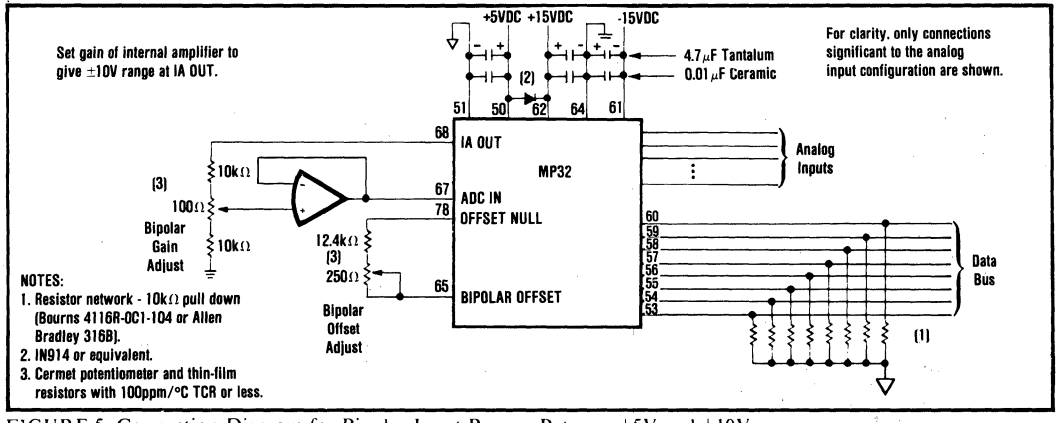


FIGURE 5. Connection Diagram for Bipolar Input Ranges Between ±5V and ±10V.

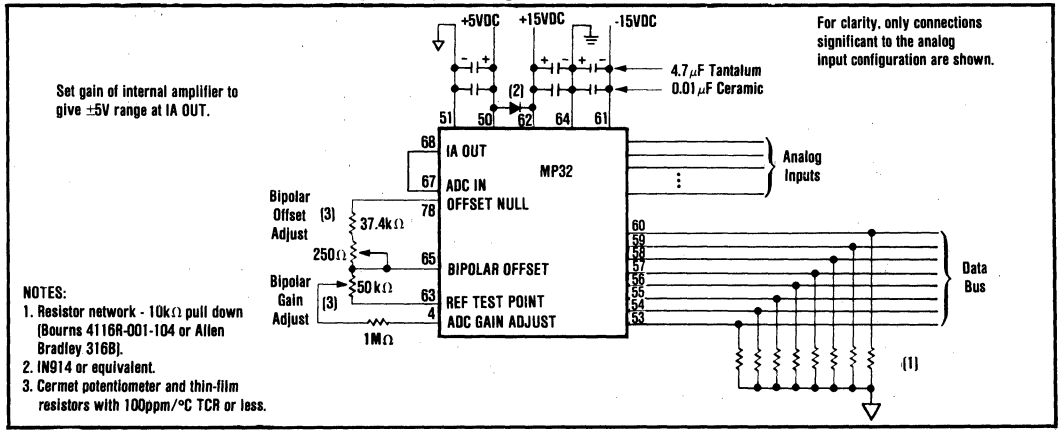


FIGURE 6. Connection Diagram for Bipolar Input Ranges of ±5V or Less.

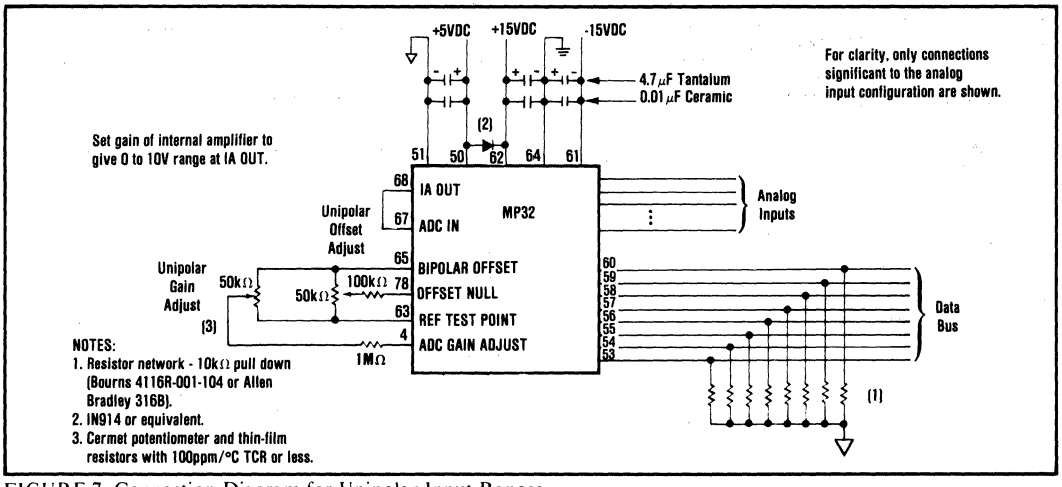


FIGURE 7. Connection Diagram for Unipolar Input Ranges.

mode except the IA low input (pin 79) is connected to a remote ground that is common to the analog inputs.

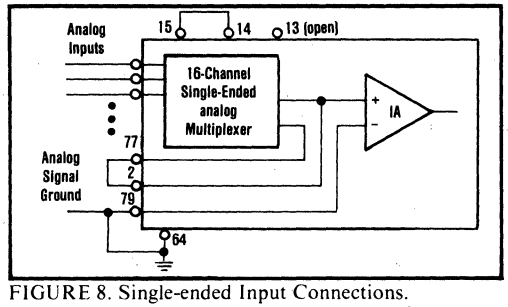


FIGURE 8. Single-ended Input Connections.

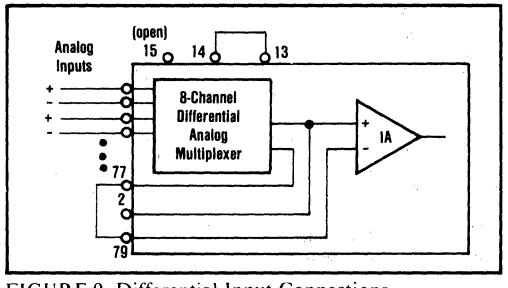


FIGURE 9. Differential Input Connections.

INPUT OVERVOLTAGE PROTECTION

As shown in Figure 10, the analog inputs have reverse biased diode circuits which protect them from damage by overvoltage (such as static). It is still reasonable to take precautions against static discharge. The same circuitry protects the inputs during operation against damage by steady-state differential or common-mode overvoltage. The MP32 overvoltage protection can be increased by adding series resistors at each input. The input resistance must limit the current flowing through the input protection diodes to 10mA. For instance, if 15kΩ resistors are added to each input, the protection is increased to 165V (16.5kΩ x 10mA). Care should be taken to insure safe power dissipation in these resistors. In this case, the power dissipated is 1.65 watts. Increased input resistance will, of course, increase the amount of time necessary for the multiplexer to settle as described in the following section.

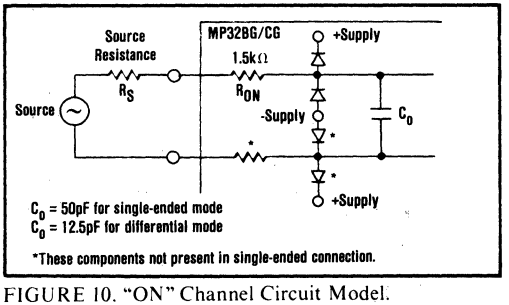


FIGURE 10. "ON" Channel Circuit Model.

SETTLING TIME AND DELAY TIME ADJUST

A delay time between channel selection and start of conversion is built into the MP32 to allow the analog multiplexer and instrumentation amplifier time to settle before starting the A/D converter. As the gain of the amplifier is increased, the settling time required increases (see Figure 11). The factory-set delay time (15μsec) is sufficient for gains of up to 50. At higher gains, a capacitor must be connected between pin 47 and pin 50 to increase the delay time. Figure 12 shows the value of capacitance required to increase the delay.

The only external factor, other than gain, that affects the MP32 settling time is the impedance of the source connected to a channel. Figure 10 shows a circuit model of an "ON" channel.

The signal at the output of the multiplexer must be allowed to settle to ±0.01% (9.2 time constants) to maintain the full accuracy of the system. The multiplexer

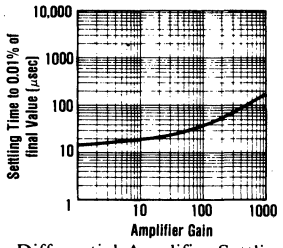


FIGURE 11. Differential Amplifier Settling Time vs Gain.

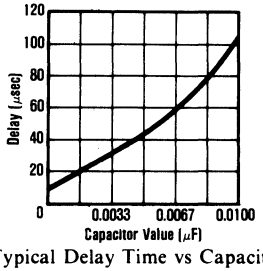


FIGURE 12. Typical Delay Time vs Capacitor Value.

time constant can be calculated with the formula:

$$\tau = (R_S + R_{ON})C_o.$$

For R_S = 1kΩ and C_o = 50pF, $\tau = (1.5 + 1)k\Omega \times 50pF$ = 125nsec. The 1.5μsec is needed to settle to ±0.01%. For high input impedances requiring more than 10μsec for multiplexer settling time, the required delay time may be calculated with this formula:

$$T_D = \sqrt{T^2_{mux} + T^2_{IA}},$$

where T_{mux} is the settling time of the multiplexer and T_{IA} is the settling time of the instrumentation amplifier as shown in Figure 11. If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitance across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5μF is sufficient. For such a capacitance the multiplexer time constant becomes 80nsec.

For switching of large signals it must be remembered that the "ON" resistance is the channel resistance of a FET which is a nonlinear function of the applied voltage. As a result the previous calculations are only an approximation derived from a linearized model. Another factor not considered is the addressing delay of the multiplexer. This is typically 250nsec and is additive to the above calculated times.

For differential units the same considerations apply. Even though two input circuits are involved there is sufficient component matching within the multiplexer to prevent measurable differences in the transfer functions for each half of the signals. Therefore, the time constant for only one circuit can be considered the time constant for the entire channel.

The MP32 internal instrumentation amplifier requires 15μsec to 100μsec for settling time. If this internal amplifier is not used, improvements in throughput rate can be obtained. This is easily done since neither the inputs nor the outputs of the instrumentation amplifier are internally connected. For instance, Burr-Brown's model 3507J high speed op amp may be used, with a settling time of 1μsec for gains of up to 100.

For a T_{IA} of 1μsec we have T_D = 1.3μsec. Using 3μsec for the delay time to allow for unit-to-unit variation, the total throughput time will be 18μsec (including the delay time from the factory-set value of 15μsec (see Figure 13).

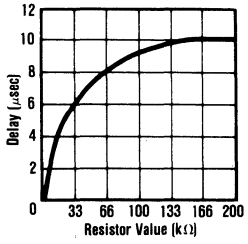


FIGURE 13. Typical Resistor Value to Decrease Delay Time.

DATA OUTPUT CODING

Table III gives the relationship of various input voltage levels to corresponding output digital words. The coding for unipolar input ranges is called Unipolar Straight Binary; bipolar input ranges yield Bipolar Offset Binary codes. Another popular output code used with bipolar input is Two's Complement. It is identical to the Bipolar Offset Binary except the MSB is inverted.

TABLE III. Voltage Input/Digital Output Relationship.

Analog Input			Digital Output
Unipolar Straight Binary	Bipolar Offset Binary	Bipolar Two's Complement	MSB LSB
+Full Scale -1LSB	+Full Scale -1LSB	-1LSB	111111111111
+1/2 Full Scale	Zero	-Full Scale	100000000000
+1/2 Full Scale -1LSB	-1LSB	+Full Scale -1LSB	011111111111
Zero	-Full Scale	Zero	000000000000

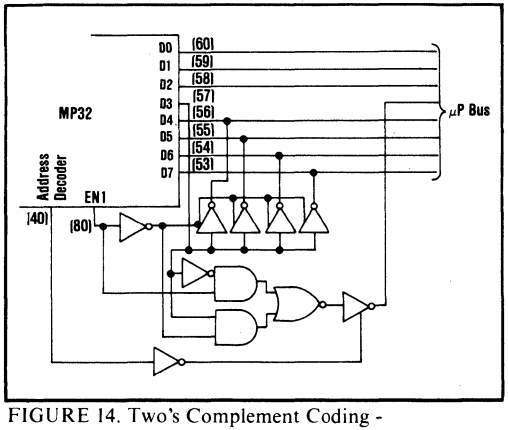


FIGURE 14. Two's Complement Coding - Output Circuit.

The two's complement output code may be obtained by software programming or by hardware, using a 4-bit

tri-state inverter as shown in Figure 14. The EN1 (pin 80) signal is used to gate $\overline{MSB}$ on the microprocessor bus during the time when the second byte of data is enabled. Thus $\overline{MSB}$ replaces $\overline{MSB}$ in this byte. The top four bits (D4-D7), normally not used in the second byte, are made equal to MSB to make two's complement addition easier.

SETUP AND CALIBRATION

RESET

It is important to reset the MP32 on start-up with a low pulse on the $\overline{RESET}$ line (pin 39). The reset pulse clears internal control logic and guarantees that at start-up all control lines are in the proper state.

GAIN AND OFFSET ADJUST CIRCUITS

The components required to null gain and offset errors for unipolar and bipolar inputs are shown in Figure 5, 6, and 7.

The offset is adjusted at the lowest input voltage transition point. (The input voltage at which the output code changes from 000000000000 to 000000000001.) The gain is adjusted at the highest input voltage transition point. Offset is adjusted first, then gain.

CALIBRATION WHEN USED WITH INTEL MODEL 8080

Before calibration, the MP32 should be allowed to warm up for 15 minutes (power applied). Calibration is performed by connecting a precision voltage source (capable of 0.005% accuracy) to an input channel. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.005% DVM.) The offset and gain adjustments on the MP32 are made while applying the voltages shown in Table IV.

The following program is used to calibrate:

```
        ORG     10H
AD:     LXI     B0          ;Clear B and C Reg. pair
AC:     LHLD    1F70H       ;Read data from
        MOV     A, L        ;Is Data = Low Ref?
        SUI     XXXX*
        JZ      AA
        INR     C           ;No. Increment count
        JMP     AB
AA:     INR     B           ;Yes. Increment count
AB:     MOV     A, B        ;Have 100 conversions
                            ; been made
        ADD     C
        CPI     64H
        JNZ     AC
AE:     JMP     AD          ;Yes. Begin program again
        END
```

*XXXX is 0000 for offset, 0FFF for gain.

The program assumes that the MP32 is wired for channel 0 located at 1F70H. If the MP32 is wired for a different address, the address associated with the LHLD instruction AC must reflect this change.

After assembling and loading the program, set a breakpoint at AE. The program is then started using a G10 Command. After 100 conversions, the breakpoint will be reached and control will return to the monitor. The B and C registers are then examined for an approximately equal count (within 10_{16} of each other). Both the Offset and Gain adjustments require that this process be repeated until the approximately equal count is reached.

CALIBRATION WHEN USED WITH MOTOROLA MODEL 6800

The procedure is the same in concept as that described in the 8080 calibration procedure. Again the unit should be allowed to warm up (power applied) for 15 minutes. The MP32 is connected as shown in Figure 21.

The 6800 calibration program is:

```
        ORG $100
START   LDAA #$64       86
                        64
        STAA COUNT      B7
                        01
                        21
        CLRA            4F      Clear accumulators
        CLRB            5F
CONV    LDX #0000       CE
                        00
                        00
        STX $1F70       FF      Begin conversion
                        1F
                        70
        NOP             01
        LDX $1F70       FE      Read data
                        1F
                        70
        CPX #$XXXX*     8C      Is Data = Low Ref
                        00
                        00
        BEQ AA          27
                        03
        INCB            5C      No. Increment count
        BRA AB          20
                        01
AA      INCA            4C      Yes. Increment count
AB      DEC COUNT       7A      Have conversions reached 100?
                        01
                        21
        BNE CONV        26      No. Do another conversion
                        F0
        BRA START       20      Yes. Begin next run
                        DF
COUNT
        END
```

*XXXX is 0000 for offset, 0FFF for gain.

The program assumes that the MP32 is set for channel located at $1F70_{16}$ and $1F71_{16}$. If the MP32 has been reprogrammed for some other address this value should be reflected in the program's STX instructions that refer to the MP32.

After assembling and loading, insert a breakpoint at location 11C via a "V" command.

Calibration is performed by connecting a precision voltage source capable of 0.005% accuracy to CH0. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a 0.005% DVM.) The offset adjustment is made first by using the appropriate offset calibration voltage. The calibration program is then run and after 100 conversions will halt at the breakpoint. Control will return to the monitor which will then print the contents of all of the program registers at the time of the breakpoint. The contents of each accumulator should be compared for approximately equal values. If a difference of more than 10_{16} is present, slightly readjust the offset control and restart the program with a ;P command. Repeat this procedure until the accumulators' contents are within 10_{16} of each other.

TABLE IV. Calibration Input Voltages.

	Input Voltage Range(1)	Full Scale Range	LSB Value	V_{in} for Offset Adjustment	V_{in} for Gain Adjustment
Unipolar	0 to +10V 0 to +5V 0 to +1V	10V 5V 1V	2.44mV 1.22mV 244μV	+1.22mV +0.610mV +0.122mV	9.99634 4.99817 +0.99963V
Bipolar	-10V to +10V -5V to +5V -1V to +1V	20V 10V 2V	4.88mV 2.44mV 488μV	-9.99756 -4.9988 -0.99976V	9.99268 4.99634 +0.99927V
General Equation	V_1 to V_2	$V_2 - V_1$	$\frac{V_2 - V_1}{2^n}$(2)	V_1 + 1/2LSB	V_2 - 3/2LSB

NOTES:
1. For other ranges, compute the proper input voltages using the general equation.
2. n = resolution (12 bits for MP32BG/CG).

The gain adjustment is made in much the same manner. However, the data associated with the CPX instruction in the calibration program must be changed from 0000_{16} to $0FFF_{16}$.

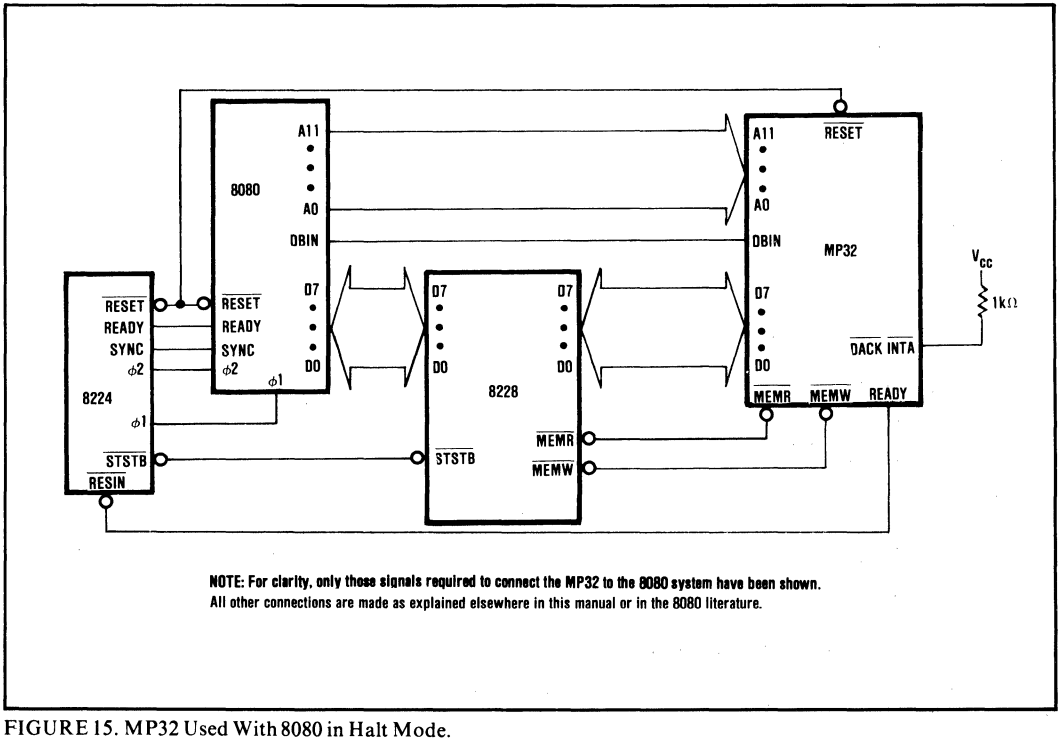
CALIBRATION WHEN USED WITH OTHER MICROPROCESSORS

The same technique used in calibrating the MP32 with the 8080 and 6800 can be used with any processor. Repetitive conversions are made around the "edge" of an output digital step or transition (the lowest for offset, the highest for gain), and then look for 50% of the conversions to be on each side of the edge. The program should be written to convert with the input at the transition voltage a large number of times and record in two registers the number of conversions that fall on each side of the transition voltage. When the numbers are approximately equal (within 10_{16}), the converter is calibrated. This must be done for offset first, then gain. Refer to Table IV for the high and low transition voltages.

Again, the unit should be allowed to warm up for 15 minutes with power applied prior to calibration.

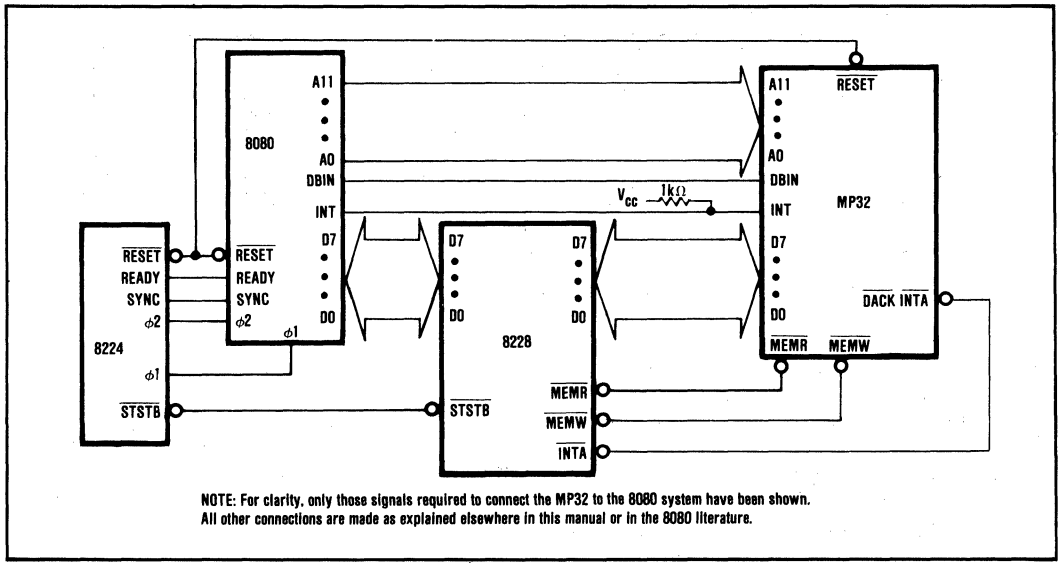
INTERFACE CONNECTION DIAGRAMS

The MP32 is designed to easily interface with most micoprocessors. The following pages illustrate the use of the MP32 with several different CPU's. The basic software to operate the units is also shown except where previously discussed in the text.



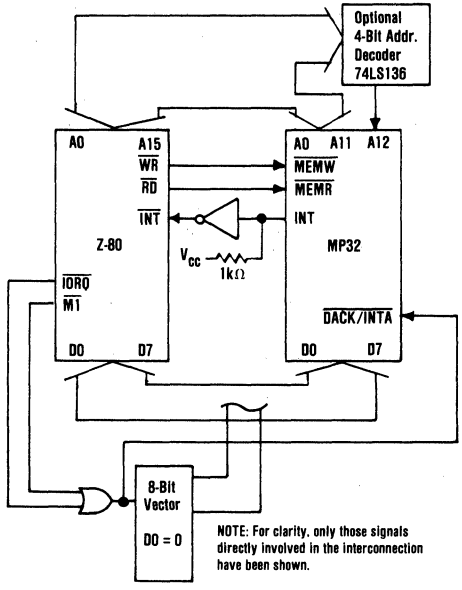
NOTE: For clarity, only those signals required to connect the MP32 to the 8080 system have been shown. All other connections are made as explained elsewhere in this manual or in the 8080 literature.

FIGURE 15. MP32 Used With 8080 in Halt Mode.



NOTE: For clarity, only those signals required to connect the MP32 to the 8080 system have been shown. All other connections are made as explained elsewhere in this manual or in the 8080 literature.

FIGURE 16. MP32 Used With 8080 in Interrupt Mode.



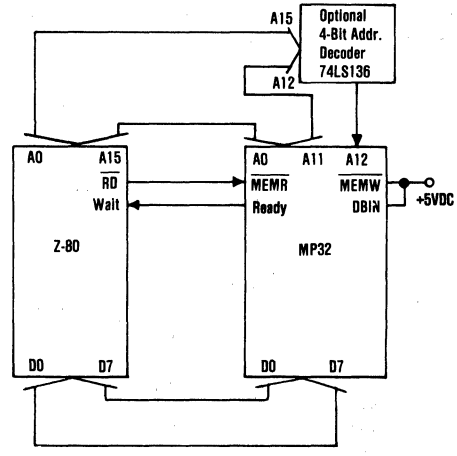
NOTE: For clarity, only those signals directly involved in the interconnection have been shown.

Z-80 is initialized to interrupt MODE 2
Conversion is started by these instructions: LDA, 0
LD (XXXX), A
The following routine is used to service the interrupt:

```
INTR:   PUSH HL          ;Save HL register pair
        LD HL, (XXXX)    ;Read data
        LD (YYYY), HL    ;Store data in memory
        POP HL           ;Restore HL register pair
        RETI
```

XXXX is the starting address of the desired channel.
YYYY is the starting address of the locations in memory where data is stored.

FIGURE 17. MP32 Used With Z-80 (Interrupt Mode).



NOTE: For clarity, only those signals directly involved in the interconnection have been shown.

Program to READ and STORE 16 channels of data using Block Transfer Instruction.

```
LD HL, NN        ;NN point to channel 0 MP32
LD DE, MM        ;MM points to the first location of the destination
LD BC, 40H       ;Byte counter (2 bytes channel x 16) = 32₁₀
LDI              ;Load and increment
JP PE, LOAD      ;Has last byte been transferred?
```

FIGURE 18. MP32 Used With Z-80 (Halt Mode).

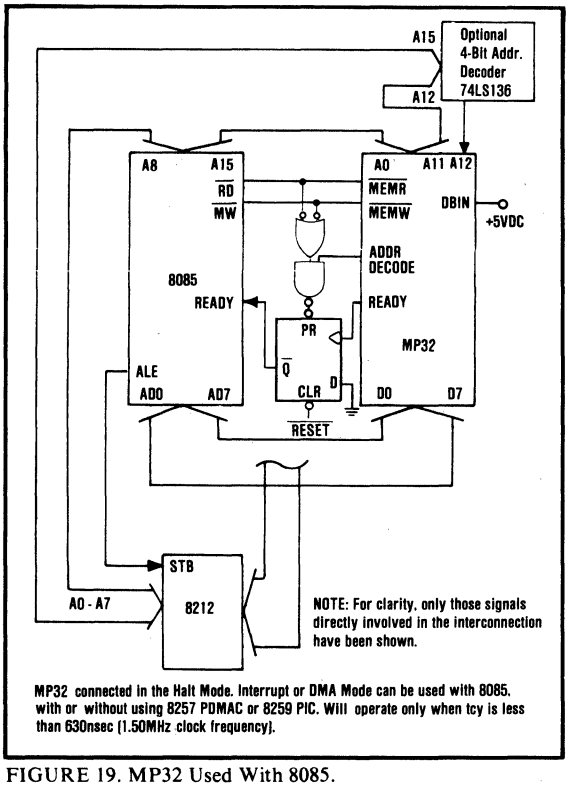


FIGURE 19. MP32 Used With 8085.

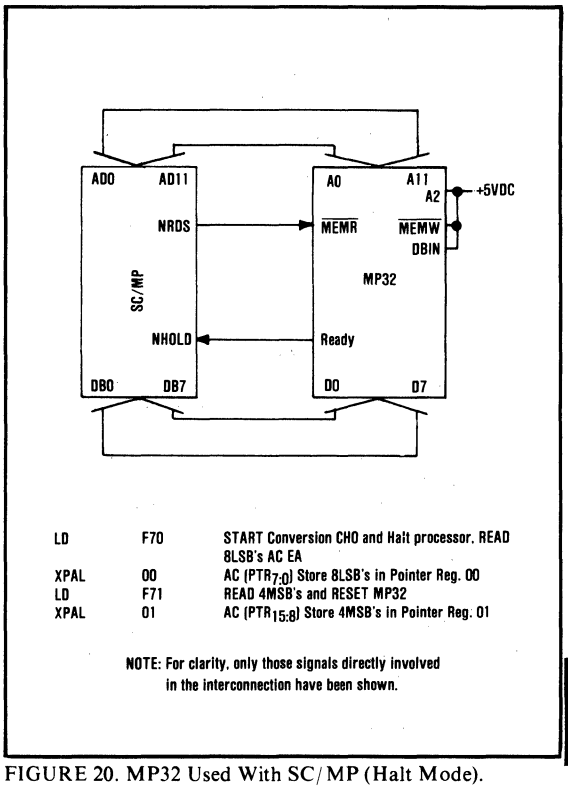


FIGURE 20. MP32 Used With SC/MP (Halt Mode).

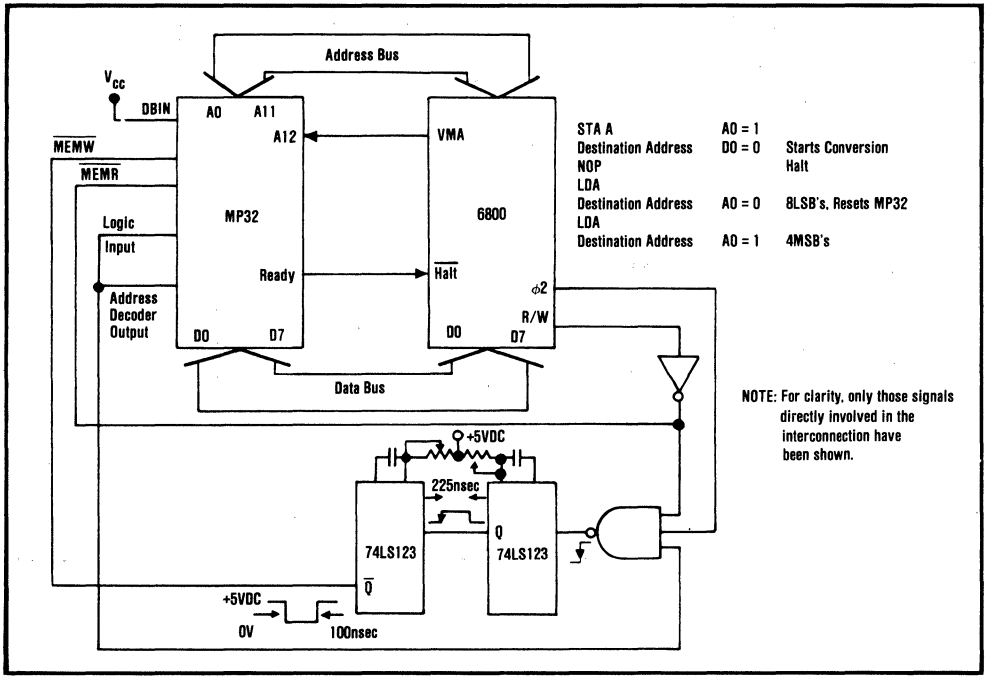


FIGURE 21. MP32 Used With 6800.

APPLICATION NOTE

DATA ACQUISITION FROM THERMOCOUPLE INPUTS

Thermocouples are often used as temperature sensors for porcess control systems. Thermocouples are characterized by temperature coefficients of 10μV/°C to 70μV/°C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the MP32 is operated with an instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wire runs from thermocouple to measuring device often pick up large common-mode noise signals of 60Hz or higher frequencies. When the MP32 is used as an 8-channel differential input system, the high common-mode rejection of the instrumentation amplifier will reject common-mode noise. To minimize differential mode noise, the signal wire should be twisted and if possible shielded. As a rule, an unshielded twisted pair is better than a coax, and a shielded, twisted pair is still better. In applications where these wiring practices can not always be observed, a differential RC filter may be used. Figure 22 shows such a system.

The 10kΩ resistors and 10μF capacitor provide low-pass filtering (f_c = 0.8Hz) and the optional 1MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth-grounded to prevent common-mode voltages from exceeding the ±5V range of the multiplexer. If the sensor is earth-grounded, the 1MΩ resistors are not required. The 1MΩ resistors do not enter into an error calculation for input errors because the low resistance of the sensor shorts any differential voltage that might be caused by the offset (difference current) of the amplifier. Offset or difference current is merely the difference between the bias currents of the two inputs. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip may be monitored to allow the observed thermocouple emf to be cold-junction compensated. Figure 22 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer. Its output sensitivity is approximately 2mV/°C.

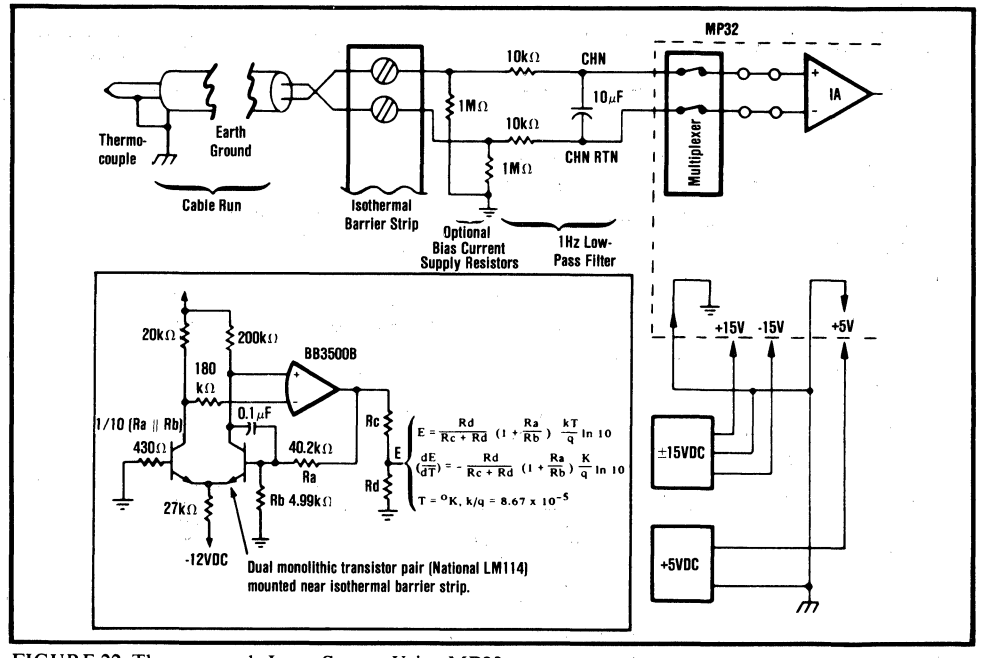
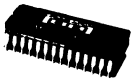


FIGURE 22. Thermocouple Input System Using MP32.

BURR-BROWN®

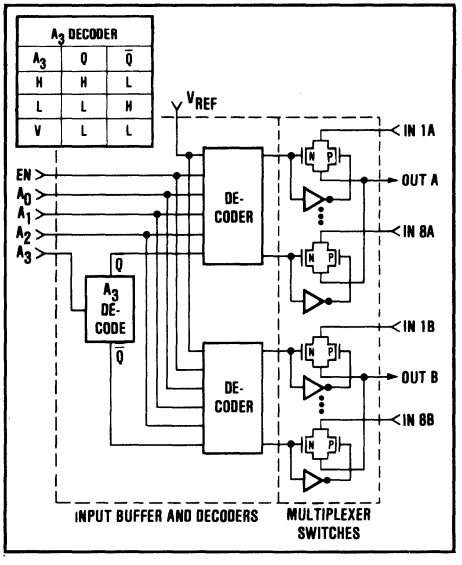
MPC800



High Speed CMOS ANALOG MULTIPLEXER

FEATURES

- HIGH SPEED
  - 100nsec access time
  - 800nsec settling to 0.01%
  - 250nsec settling to 0.1%
- USER-PROGRAMMABLE
  - 16-channel single-ended or
  - 8-channel differential
- SELECTABLE TTL or CMOS COMPATIBILITY
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER
- 28-PIN HERMETIC DUAL-IN-LINE PACKAGE



DESCRIPTION

The MPC800 is a high speed multiplexer that is user-programmable for 16-channel single-ended operation or 8-channel differential operation and for TTL or CMOS compatibility.

The MPC800 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC800KG for operation from 0°C to +75°C and the MPC800SG for operation from -55°C to +125°C.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-463

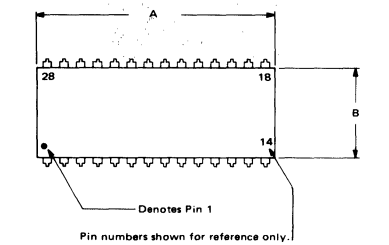
SPECIFICATIONS

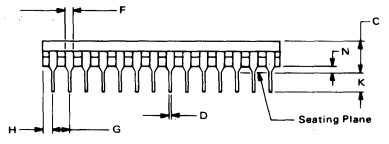
ELECTRICAL

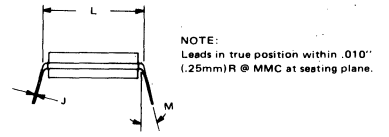
At T_A = +25°C and ±V_{CC} = 15V, unless otherwise noted.

MODEL	MPC800KG, MPC800SG			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Voltage Range	-15		+15	V
Maximum Overvoltage	-V_{CC} -2		+V_{CC}, +2	V
Number of Input Channels				
Differential	8			
Single-Ended	16			
Reference Voltage Range(1)	6		10	V
ON Characteristics(2)				
ON Resistance (R_{ON}) at +25°C		620	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature	See Typical Performance Curves			
R_{ON} Mismatch		< 10		Ω
ON Channel Leakage		0.04		nA
Over Temperature Range		0.6	100	nA
ON Channel Leakage Drift	See Typical Performance Curves			
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.01		nA
Over Temperature Range		0.38	50	nA
OFF Channel Input Leakage Drift	See Typical Performance Curves			
OFF Channel Output Leakage		0.035		nA
Over Temperature Range		0.48	100	nA
OFF Channel Output Leakage Drift	See Typical Performance Curves			
Output Leakage (All channels disabled)(3)		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
-16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL(4)				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	μA
I_{AL}		4	25	μA
TTL Input Overvoltage	-6		6	V
CMOS				
Logic "0" (V_{AL})			0.3V_{REF}	V
Logic "1" (V_{AH})	0.7 V_{REF}			V
CMOS Input Overvoltage	-2		+V_{CC} +2	V
Address A_3 Overvoltage	-V_{CC} -2		+V_{CC} +2	V
Digital Input Capacitance		5		pF
Channel Select(5)				
Single-Ended	4-bit binary code one of 16			
Differential	3-bit binary code one of 8			
Enable	Logic "0" inhibits all channels			
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		525		mW
Allowable Total Power Dissipation(6)			1200	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+35, -39		mA
At 100kHz Switching Speed		+25, -29		mA
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Cross Talk(7)	See Typical Performance Curves			
T_{OPEN} (Break before make delay)		20		nsec
Access Time at +25°C		100	150	nsec
Over Temperature Range		120	200	nsec
Settling Time(8)				
to 0.1% (20mV)		250		nsec
to 0.01% (2mV)		800		nsec
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
Channel Input Capacitance, C_S (off)		2.5		pF
Channel Output Capacitance, C_O (off)		18		pF
Input to Output Capacitance, C_{DS} (off)		0.02		pF

MECHANICAL







DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.360	1.475	34.54	37.47
B	.500	.550	12.70	13.97
C	– –	.220	– –	5.59
D	.015	.021	0.38	0.53
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.007	.013	0.18	0.33
K	.100	– –	2.54	– –
L	.600 BASIC		15.24 BASIC	
M	– –	15°	– –	15°
N	.020	.090	0.51	2.29

PIN CONFIGURATION

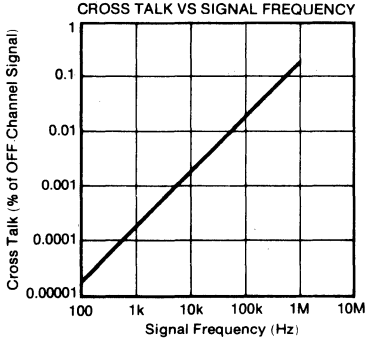
TOP VIEW

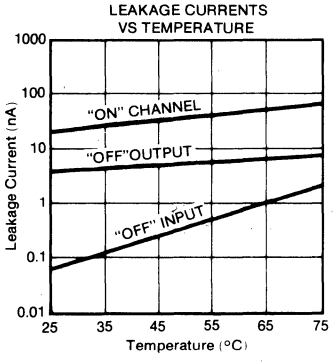
+V_{CC}	1	28	OUT A
OUT B	2	27	-V_{CC}
NC	3	26	IN 8/8A
IN16/8B	4	25	IN7/7A
IN15/7B	5	24	IN6/6A
IN14/6B	6	23	IN5/5A
IN13/5B	7	22	IN4/4A
IN12/4B	8	21	IN3/3A
IN11/3B	9	20	IN2/2A
IN10/2B	10	19	IN1/1A
IN9/1B	11	18	ENABLE
GND	12	17	A_0
V_{REF}	13	16	A_1
A_3	14	15	A_2

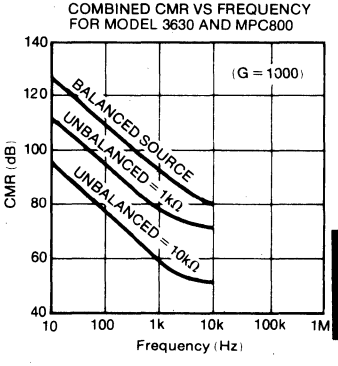
MODEL	MPC800KG, MPC800SG			
PARAMETER	MIN	TYP	MAX	UNITS
TEMPERATURE				
MPC800KG				
Specification	0		+75	°C
Storage	-65		+150	°C
MPC800SG				
Specification	-55		+125	°C
Storage	-65		+150	°C

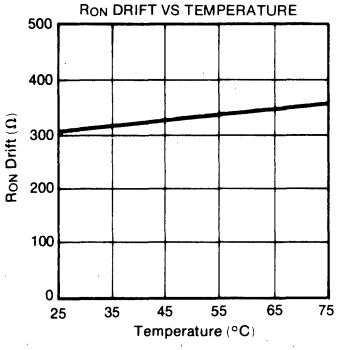
NOTES:
1. Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility.
2. $V_{IN} = \pm 10V$, $I_{OUT} = 100\mu A$.
3. Single-ended mode.
4. Logic levels specified for V_{REF} (pin 13) open.
5. For single-ended operation, connect output A (pin 28) to output B (pin 2) and use A_3 (pin 14) as an address line. For differential operation connect A_3 to $-V_{CC}$.
6. Derate 8mW/°C above $T_A = +75°C$.
7. 10V, p-p, sine wave on all unused channels. See Typical Performance Curves.
8. For 20V step input to ON channel, into 1kΩ load.

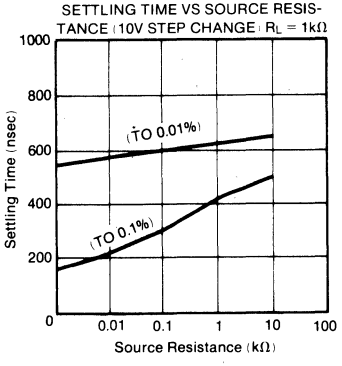
TYPICAL PERFORMANCE CURVES











DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

RESISTIVE LOADING ERRORS

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.002% loading error and 10kΩ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\epsilon\ (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where $R_S = R_{source}$
R_L = Load Resistance
R_{ON} = Multiplexer ON resistance

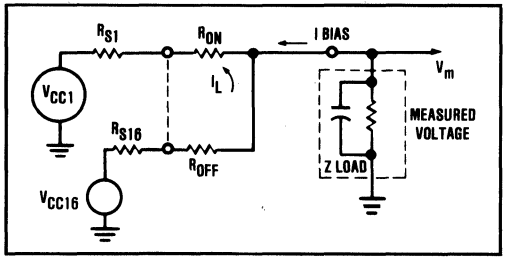


FIGURE 1. MPC800 Static Accuracy Equivalent Circuit (Single-ended Operation).

Input Offset Voltage

Bias and leakage currents generate an input Offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of 19μV if a 1000Ω source is used, and 118μV if a 10kΩ source is used. In general, for the MPC800 the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_{source}) \text{ where}$$

I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

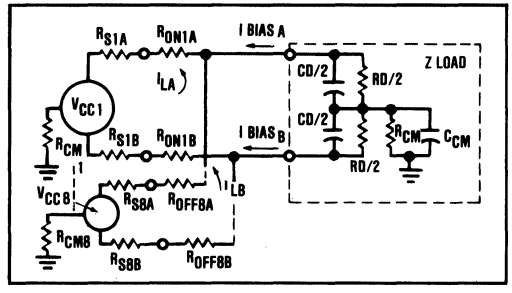


FIGURE 2. MPC800 Static Accuracy Equivalent Circuit (Differential Operation).

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC800 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low level signal applications

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC800 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RC's. For the MPC800 the internal capacitance is approximately 20pF differential or 40pF single-ended. With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40nsec. This means the source resistance should be kept to less than 2kΩ (assume high load resistance) to maintain fast settling times.

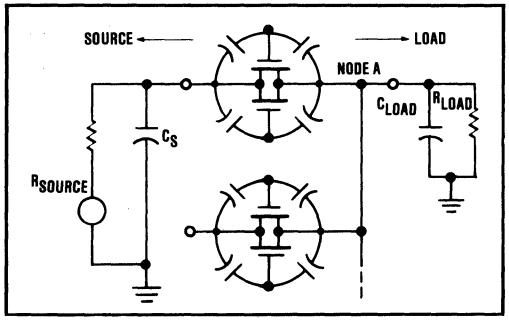


FIGURE 3. Settling Time Effects (Single-ended).

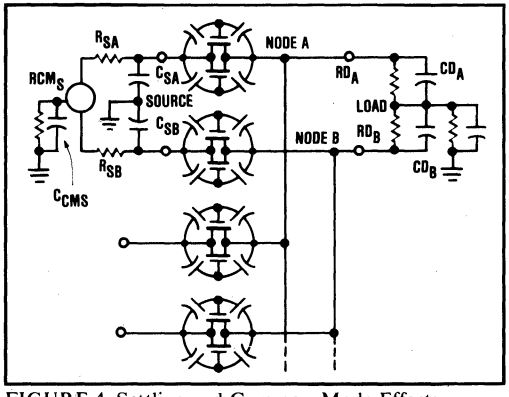


FIGURE 4. Settling and Common-Mode Effects (Differential).

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 7 differential or 15 single-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (DIFFERENTIAL MODE ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC800 and Burr-Brown's model 3630 Instrumentation Amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.

- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.
- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION & OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC800 use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 13) open or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

16-CHANNEL SINGLE-ENDED OPERATION

To use the MPC800 as a 16-channel single-ended multiplexer, output A (pin 28) is connected to output B (pin 2) to form a single output, then all four address lines (A_0, A_1, A_2 and A_3) are used to address the correct channel.

The MPC800 can also be used as a dual 8-channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

8-CHANNEL DIFFERENTIAL OPERATION

To use the MPC800 as an 8-channel differential multiplexer, connect address line A_3 to $-V_{CC}$ then use the remaining three address lines (A_0, A_1 and A_2) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC800 used as 16-channel single-ended multiplexer or 8-channel dual multiplexer.

USE A_3 AS DIGITAL ADDRESS INPUT					"ON" CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

For 16-channel single-ended function, tie "out A" to "out B, for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

MPC800 used as 8-channel differential multiplexer.

A_3 CONNECT TO $-V_{CC}$				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

CHANNEL EXPANSION

Single-tier Expansion

Up to four MPC800's can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC800's can be connected to two nodes to form a 64-channel differential multiplexer. Programming is accomplished with a six-bit address and a 1 of 4 decoder for 64-channel single-ended expansion (see Figure 5) or an eight-bit address and a 1 of 8 decoder for 64-channel

differential expansion. The decoder drives the enable inputs of the MPC800, turning on only one multiplexer at a time.

Two-tier Expansion

Up to seventeen MPC800's can be connected in a two-tier structure to form a 256-channel single-ended multiplexer (see Figure 6) or up to nine MPC800's can be connected in a two-tier structure to form a 64-channel differential multiplexer. Programming is accomplished with a 8-bit address.

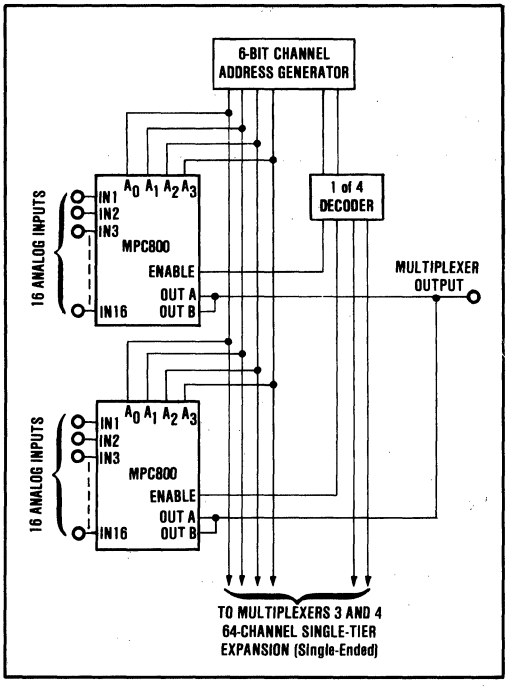


FIGURE 5. 32- to 64-Channel, Single-tier Expansion.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one-channel group is failed (8 or 16) in the multitiered configuration.

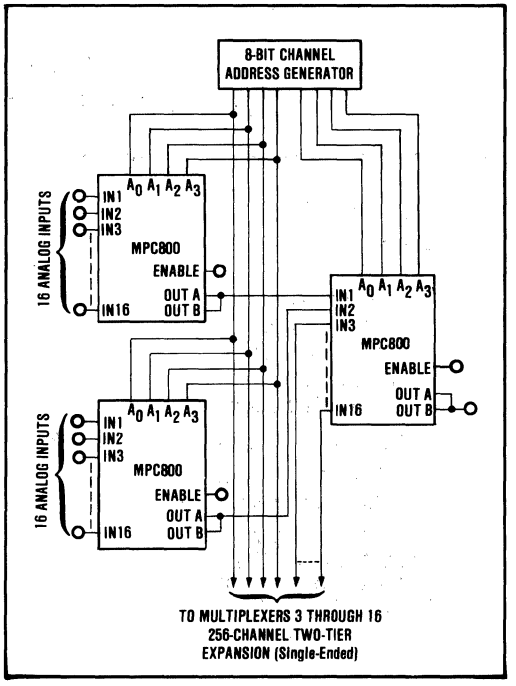


FIGURE 6. Channel Expansion up to 256 Channels using 16 x 16 Two-tiered Expansion.

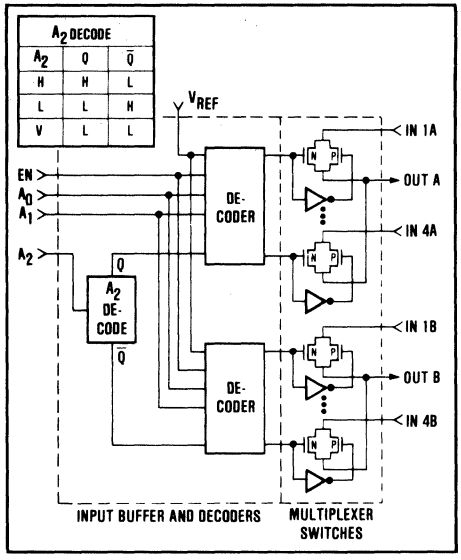
BURR-BROWN®

MPC801

High Speed CMOS ANALOG MULTIPLEXER

FEATURES

- HIGH SPEED
  - 80nsec access time
  - 800nsec settling to 0.01%
  - 250nsec settling to 0.1%
- USER-PROGRAMMABLE
  - 8-channel single-ended or
  - 4-channel differential
- SELECTABLE TTL or CMOS COMPATIBILITY
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- SELF-CONTAINED WITH INTERNAL CHANNEL ADDRESS DECODER
- 18-PIN HERMETIC DUAL-IN-LINE PACKAGE



DESCRIPTION

The MPC801 is a high speed multiplexer that is user-programmable for 8-channel single-ended operation or 4-channel differential operation and for TTL or CMOS compatibility.

The MPC801 features a self-contained binary address decoder. It also has an enable line which allows the user to inhibit the entire multiplexer thereby facilitating channel expansion by adding additional multiplexers.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, low ON resistance, high OFF resistance, low feedthrough capacitance, and fast settling time.

Two models are available, the MPC801KG for operation from 0°C to +75°C and the MPC801SG for operation from -55°C to +125°C.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

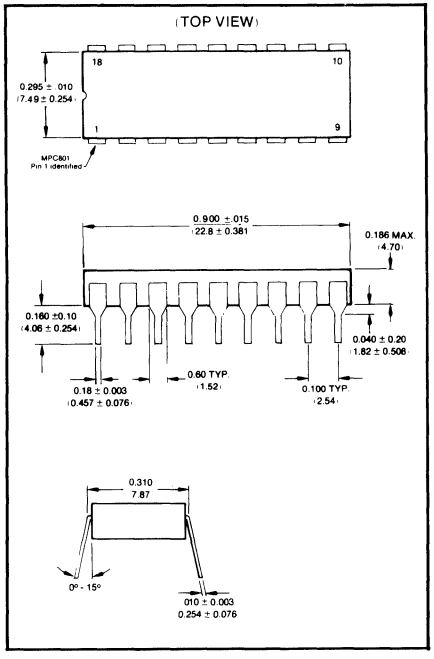
SPECIFICATIONS

ELECTRICAL

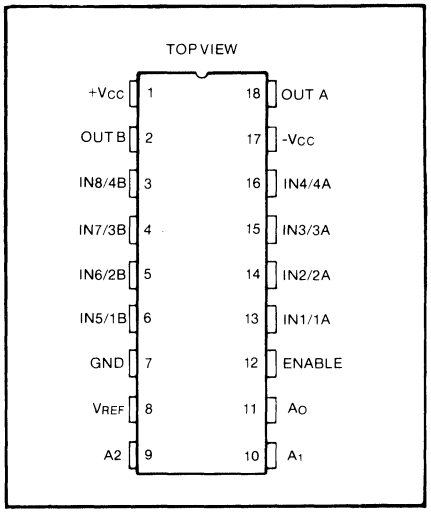
At T_A = +25°C and ±V_{CC} = 15VDC unless otherwise noted.

MODEL	MPC801KG, MPC801SG			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT				
ANALOG INPUT				
Voltage Range	-15		+15	V
Maximum Overvoltage	-V_{CC} -2		+V_{CC} +2	V
Number of Input Channels				
Differential	4			
Single-Ended	8			
Reference Voltage Range(1)	6		10	V
ON Characteristics(2)				
ON Resistance (R_{ON}) at +25°C		500	750	Ω
Over Temperature Range		700	1000	Ω
R_{ON} Drift vs Temperature	See Typical Performance Curves			
R_{ON} Mismatch		< 10		Ω
ON-Channel Leakage		0.1		nA
Over Temperature Range		0.3	50	nA
ON Channel Leakage Drift	See Typical Performance Curves			
OFF Characteristics				
OFF Isolation		90		dB
OFF Channel Input Leakage		0.05		nA
Over Temperature Range		0.6	50	nA
OFF Channel Input Leakage Drift	See Typical Performance Curves			
OFF Channel Output Leakage		0.1		nA
Over Temperature Range		0.30	50	nA
OFF Channel Output Leakage Drift	See Typical Performance Curves			
Output Leakage (All channels disabled)(3)		0.02		nA
Output Leakage with Overvoltage				
+16V Input		< 0.35		mA
-16V Input		< 0.65		mA
DIGITAL INPUTS				
Over Temperature Range				
TTL(4)				
Logic "0" (V_{AL})			0.8	V
Logic "1" (V_{AH})	2.4			V
I_{AH}		0.05	1	μA
I_{AL}		4	20	μA
TTL Input Overvoltage	-6		6	V
CMOS				
Logic "0" (V_{AL})			0.3V_{REF}	V
Logic "1" (V_{AH})	0.7 V_{REF}			V
CMOS Input Overvoltage	-2		+V_{CC} +2	V
Address A_2 Overvoltage	-V_{CC} -2		+V_{CC} +2	V
Digital Input Capacitance		5		pF
Channel Select(5)				
Single-Ended	3-bit binary code one of 8			
Differential	2-bit binary code on of 4			
Enable	Logic "0" inhibits all channels			
POWER REQUIREMENTS				
Over Temperature Range				
Rated Supply Voltage		±15		V
Maximum Voltage Between Supply Pins			33	V
Total Power Dissipation		360		mW
Allowable Total Power Dissipation(6)			725	mW
Supply Drain (+25°C)				
At 1MHz Switching Speed		+14, -12.5		mA
At 100kHz Switching Speed		+12.5,-12.5		mA
DYNAMIC CHARACTERISTICS				
Gain Error		< 0.0003		%
Cross Talk(7)	See Typical Performance Curves			
T_{OPEN} (Break before make delay)		20		nsec
Access Time at 25°C		80	125	nsec
Over Temperature Range		110	150	nsec
Settling Time(8)				
to 0.1% (20mV)		250		nsec
to 0.01% (2mV)		800		nsec
Common-Mode Rejection (Differential)				
DC		> 125		dB
60Hz		> 75		dB
OFF Channel Input Capacitance, C_S (off)		1.9		pF
OFF Channel Output Capacitance, C_O (off)		10		pF
OFF Input to Output Capacitance, C_{DS} (off)		0.02		pF

MECHANICAL



PIN CONFIGURATION



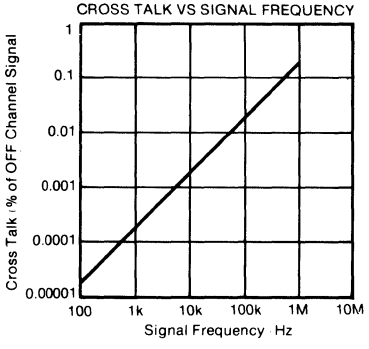
MPC801

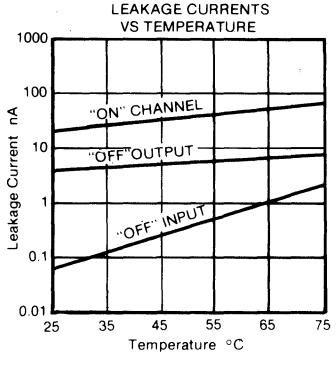
ELECTRICAL (CONT)

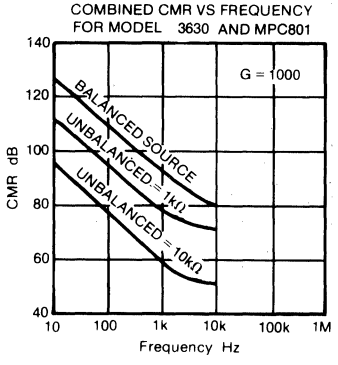
MODEL	MPC801KG, MPC801SG			
PARAMETER	MIN	TYP	MAX	UNITS
TEMPERATURE				
MPC801KG				
Specification	0		+75	°C
Storage	-65		+150	°C
MPC801SG				
Specification	-55		+125	°C
Storage	-65		+150	°C

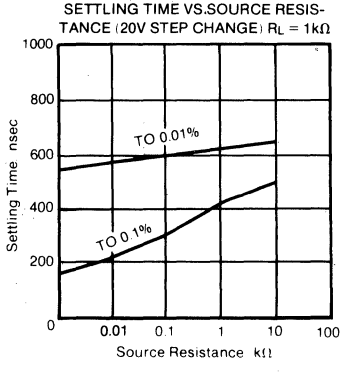
NOTES:
1. Reference voltage controls noise immunity, normally left open for TTL compatibility and connected to V_{DD} for CMOS compatibility.
2. $V_{IN} = \pm 10V$, $I_{OUT} = 100\mu A$.
3. Single-ended mode.
4. Logic levels specified for V_{REF} (pin 8) open.
5. For single-ended operation, connect output A (pin 18) to output B pin 2, and use A_2 (pin 9) as an address line. For differential operation connect A_2 to $-V_{CC}$.
6. Derate 8mW/°C above $T_A = +75°C$.
7. 10V, p-p, sine wave on all unused channels. See Typical Performance Curves.
8. For 20V step input to ON channel, into 1kΩ load.

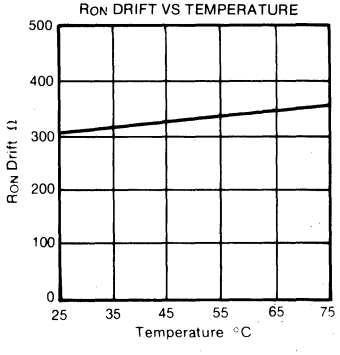
TYPICAL PERFORMANCE CURVES











DISCUSSION OF PERFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current, and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

RESISTIVE LOADING ERRORS

The source and load impedances will determine the ON resistance loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000Ω source resistance will present less than 0.002% loading error and 10kΩ source resistance will increase source loading error 0.02% with a $10^8\Omega$ load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1):

Source and Multiplexer Resistive Loading Error

$$\epsilon\,(R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\% \text{ where}$$

$R_S = R_{source}$
R_L = Load resistance
R_{ON} = Multiplexer ON resistance.

Input Offset Voltage

Bias and leakage currents generate an input Offset voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA, a leakage current of 1nA, and an ON resistance of 700Ω will generate an offset voltage of 19μV if a 1000Ω source is used, and 118μV if a 10kΩ is used. In general, for the MPC801 the Offset voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_{source}) \text{ where}$$

I_B = Bias Current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{source} = Source resistance.

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low level signals with full scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

Load (Output Device) Characteristics

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

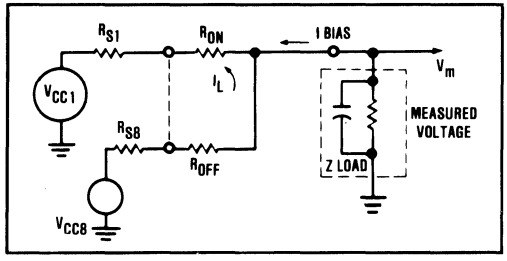


FIGURE 1. MPC801 Static Accuracy Equivalent Circuit (Single-ended Operation).

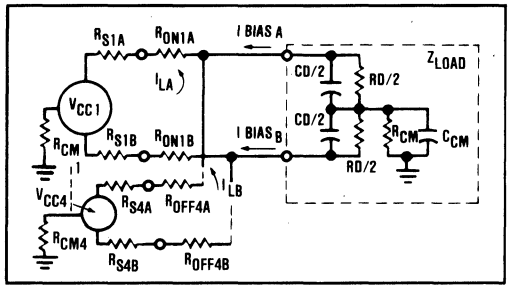


FIGURE 2. MPC801 Static Accuracy Equivalent Circuit (Differential Operation).

Source Characteristics

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC801 is used for multiplexing high level signals of 1V to 10V full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low level signal applications

SETTLING TIME

Settling time is the time required for the multiplexer to reach and maintain an output within a specified error band of its final value in response to a step input. The settling time of the MPC801 is primarily due to the channel capacitance and a combination of resistances which include the source and load resistances.

If the parallel combination of the source and load resistance times the total channel capacitance is kept small, then the settling time is primarily affected by internal RC's. For the MPC801 the internal capacitance is approximately 10pF differential or 20pF single-ended.

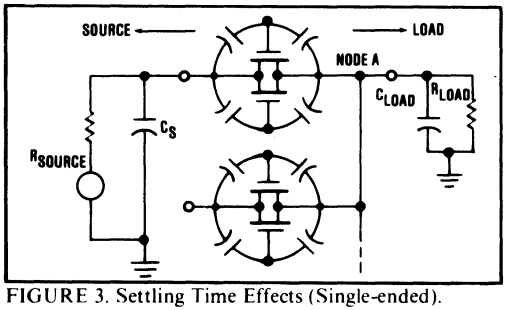


FIGURE 3. Settling Time Effects (Single-ended).

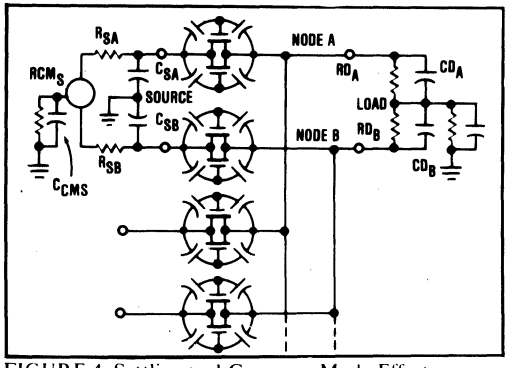


FIGURE 4. Settling and Common-Mode Effects (Differential).

With external capacitance neglected, the time constant of source resistance in parallel with load resistance and the internal capacitance should be kept less than 40nsec. This means the source resistance should be kept to less than 4kΩ (assume high load resistance) to maintain fast settling times.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the 3 differential or 7 single-ended OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance, and junction capacitances in series with the R_{ON} and R_{source} impedances of the ON channel. Crosstalk is measured with a 20V, pk-pk, 1000Hz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

COMMON-MODE REJECTION (DIFFERENTIAL MODE ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. Protection is provided for common-mode signals of ±2V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC801 and Burr-Brown's model 3630 Instrumentation Amplifier is 120dB at DC to 10Hz with a 6dB/octave rolloff to 80dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model 3630 instrumentation amplifier connected for a gain of 1000 and with source unbalance of 10kΩ, 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch.
- Load impedance mismatch.
- Multiplexer impedance and leakage current mismatch.

- Load and source common-mode impedance.

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

INSTALLATION & OPERATING INSTRUCTIONS

The ENABLE input, pin 12, is included for expansion of the number of channels on a single-node as illustrated in Figure 5. With the ENABLE line at a logic 1, the channel is selected by the Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to logic 1.

For the best settling time, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pullup resistors are recommended.

To preserve common-mode rejection of the MPC801 use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

LOGIC LEVELS

The logic level is user-programmable as either TTL-compatible by leaving the V_{REF} (pin 8) open or CMOS-compatible by connecting the V_{REF} to V_{DD} (CMOS supply voltage).

8-CHANNEL SINGLE-ENDED OPERATION

To use the MPC801 as an 8-channel single-ended multiplexer, output A (pin 18) is connected to output B (pin 2) to form a single output, then all three address lines (A_0, A_1, and A_2) are used to address the correct channel.

The MPC801 can also be used as a dual channel single-ended multiplexer by not connecting output A and B, but then only one channel in one of the multiplexers can be addressed at a time.

4-CHANNEL DIFFERENTIAL OPERATION

To use the MPC801 as an 4-channel differential multiplexer, connect address line A_2 to $-V_{CC}$ then use the remaining two address lines (A_0 and A_1) to address the correct channel. The differential inputs are the pairs of A_1 and B_1, A_2 and B_2, etc.

TRUTH TABLES

MPC801 used as 8-channel single-ended multiplexer or 4-channel dual multiplexer.

USE A_2 AS DIGITAL ADDRESS INPUT				"ON" CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

For 8-channel single-ended function, tie "out A" to "out B", for dual 4-channel function use the A_2 address pin to select between MUX A and MUX B, where MUX A is selected with A_2 low.

MPC801 used as 4-channel differential multiplexer.

A_2 CONNECT TO $-V_{CC}$			"ON" CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

CHANNEL EXPANSION

Single-tier Expansion

Up to eight MPC801's can be connected to a single node to form a 64-channel single-ended multiplexer or up to eight MPC801's can be connected to two nodes to form a 32-channel differential multiplexer. Programming is accomplished with a 6-bit address and a 1 of 8 decoder (Figure 5). The decoder drives the enable inputs of the MPC801, turning on only one multiplexer at a time.

Two-tier Expansion

Up to nine MPC801's can be connected in a two-tier structure to form a 64-channel single-ended multiplexer (Figure 6) or up to five MPC801's can be connected in a two-tier structure to form a 16-channel differential multiplexer. Programming is accomplished with a 6-bit address.

SINGLE VS MULTITIERED CHANNEL EXPANSION

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced Offset), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-

node configuration, data cannot be taken from any channel, whereas only one channel group is failed (4 or 8) in the multitiered configuration.

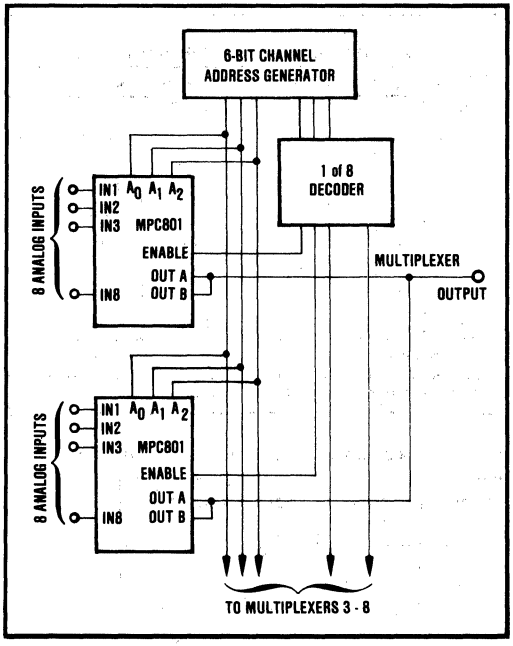


FIGURE 5. 64-Channel, Single-Tier, Single-Ended Expansion.

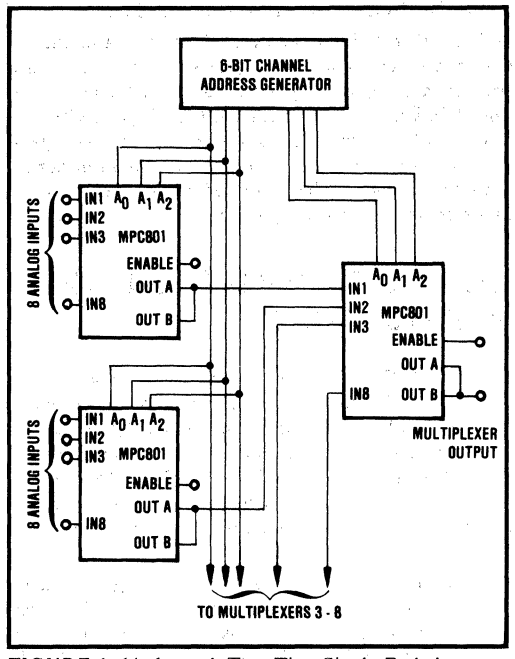
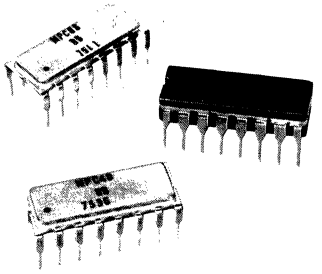


FIGURE 6. 64-channel, Two-Tier, Single-Ended Expansion.

BURR-BROWN®



MPC4D
MPC8S

CMOS ANALOG MULTIPLEXERS

FEATURES

- LOW POWER CONSUMPTION
  CMOS analog switches
  15mW at 100kHz
- PROTECTS SIGNAL SOURCES
  Break-before-make switching
- HIGH THROUGHPUT RATE
- RELIABLE MONOLITHIC CONSTRUCTION

DESCRIPTION

The MPC8S is a single-ended monolithic 8-channel analog multiplexer and the MPC4D is a monolithic 4-channel differential input/output multiplexer. The digital and analog inputs are protected from overvoltage inputs that exceed either power supply. These CMOS devices feature self-contained binary channel address decoding and are compatible with DTL, TTL, or CMOS input levels. Channel interaction is eliminated during overvoltage conditions and also in the event of a power loss. They are packaged in a 16-pin DIP and dissipate typically 7.5mW.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-356

DESCRIPTION

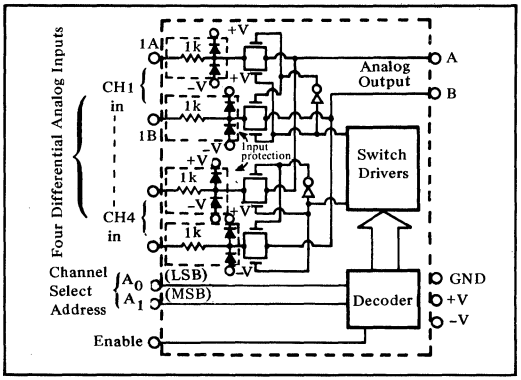
The MPC8S is a single-ended monolithic 8 channel analog multiplexer and the MPC4D is a monolithic differential input/output channel analog multiplexer constructed with failure protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200 kHz from signal sources of up to ±10 volts amplitude.

These DTL/TTL/CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable an 8 channel group (MPC8S) or a 4 channel group (MPC4D) facilitating channel expansion in either single-mode or multi-tiered matrix configurations.

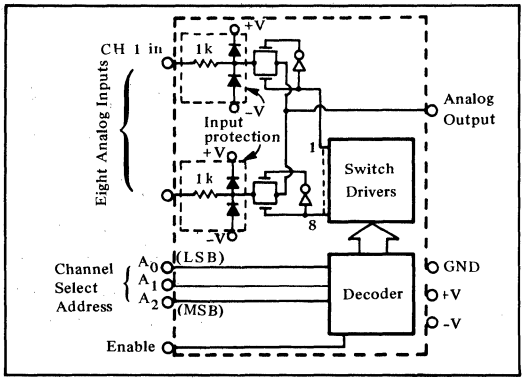
Digital and analog inputs are failure protected from either overvoltages that exceed the power supplies or from the loss of power.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

These devices are housed in compact 16 pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are in pin and package compatible with the 508/509 series.



FUNCTIONAL BLOCK DIAGRAM – MPC4D



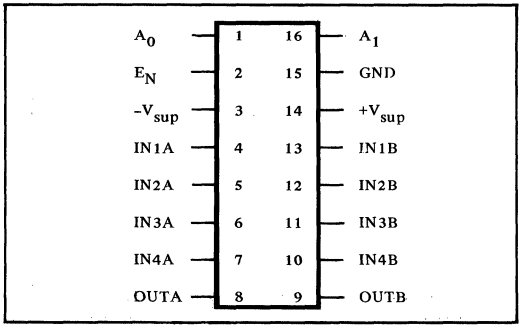
FUNCTIONAL BLOCK DIAGRAM – MPC8S

A_1	A_0	E_N	"On" Switch Pair
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

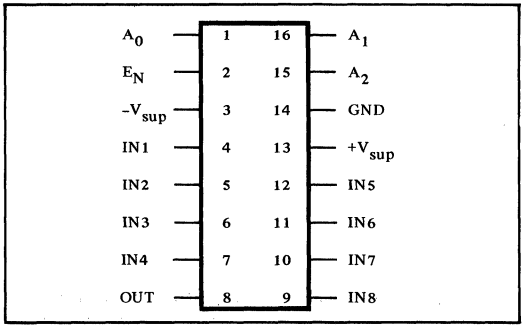
TRUTH TABLE –MPC4D

A_2	A_1	A_0	E_N	On Switch
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE – MPC8S



MPC4D PIN DIAGRAM



MPC8S PIN DIAGRAM

SPECIFICATIONS

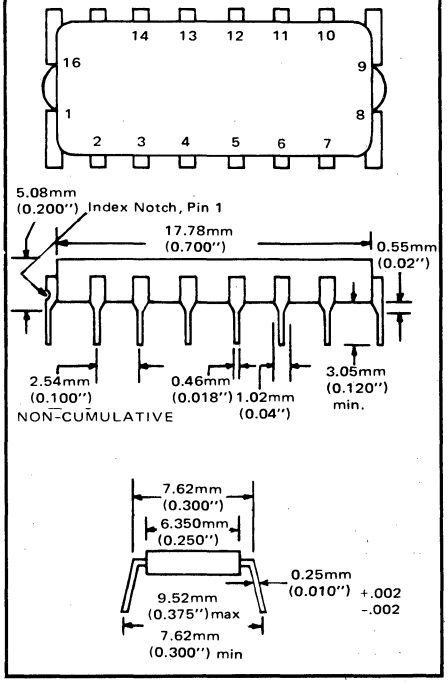
Typical for following conditions: V + = +15V, V - = -15V, $R_{source} \leq 1000\ \Omega$, $T_A = 25°C$ unless otherwise noted.

ELECTRICAL

MODELS	MPC8S	MPC4D	Units
INPUT			
ANALOG INPUT			
Voltage Range	±15		V
Maximum Overvoltage	+V supply +20		V
	-V supply -20		V
Current at Maximum Overvoltage per channel[1]	±18		mA
Number of Input Channels			
Single-ended	8		
Differential		4	
ON Characteristics			
ON Resistance (R_{ON})			
Typical	1.5		kΩ
Maximum	1.8		kΩ
R_{ON} Drift vs. Temperature (0°C to +75°C)	0.25		%/°C
R_{ON} Mismatch			
Channel-to-channel	50	50	Ω
Differential	N/A	50	Ω
Input Leakage (I_L)	0.1		nA
Input Leakage Drift	See Figure 9		
OFF Characteristics			
OFF Resistance	10^{11}		Ω
Output Leakage			
(All channels disabled)	0.2		nA
Input Leakage[6]	0.02		nA
Leakage Drift	See Figure 9		
Output Leakage with Input Overvoltage			
of +35V	1		nA
of -35V	1		μA
DIGITAL INPUTS			
Logic "0" (V_L)[1][2]	-V supply ≤ V_L < 0.8 at 1 nA		V
Logic "1" (V_H)[1][2]	+4V ≤ V_H ≤ + V supply at 1 nA		V
Channel Select	3 bit binary code - one of eight	2 bit binary code - one of four	
Enable	Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel.		
POWER REQUIREMENTS			
Rated Power Supply Voltages	±15		V
Supply Range			
+Supply	+5 to +20		V
-Supply	-5 to -20		V
Supply Drain			
At 1 MHz Switching Speed	+4, -2		mA
AT 100 kHz Switching Speed	±0.5		mA
Typical Power Consumption DC to 10 kHz	7.5		mW
DYNAMIC CHARACTERISTICS			
Gain Error (20 MΩ load) maximum	0.01		%
Crosstalk[3]	0.005		% of OFF channel signal
Settling Time[4]			
To ±2mV ±(0.01%)	5		μs
To ±20mV ±(0.10%)	2		μs
Common-mode Rejection (minimum)	N/A	120	dB
Switching Time			
Turn ON	0.5		μs
Turn OFF	0.3		μs
Recovery Time from Input Overvoltage Pulse of 35V for 100 μsec			
To 0.01%	150		μs
To 0.10%	15		μs
OUTPUT			
Voltage Range	±15		V
Capacitance to Ground	25	12[5]	pF
Capacitance Mismatch	N/A	±10	%
TEMPERATURE			
Specification	0 to +75		°C
Storage	-65 to +150		°C

MPC4D AND MPC8S

16 Pin Ceramic Lead Frame TOP VIEW



NOTES:

1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to 0.75 watt for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Maximum overvoltage is ±Vsupply ±4 volts at ±15 mA.
3. 20 volt peak-to-peak 1000 Hz sinewave; $R_{SOURCE} = 1000\Omega$, same signal on all unused channels.
4. For 20 volts between switched channels, $R_{SOURCE} = 1000\Omega$. See Figure 5 for settling time vs. source impedance (R_S).
5. From each side of MPC4D to ground.
6. Leakage measurement made with all OFF channel inputs fed in parallel to +20 volts.

DISCUSSION OF PERFORMANCE

Static Transfer Accuracy

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

SINGLE-ENDED MULTIPLEXER STATIC ACCURACY

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of 10^8 ohms or greater will keep resistive loading errors to 0.002% or less for 1000 ohm source impedances. A 10^6 ohm load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000 ohm source resistance will present less than 0.001% loading error and 10,000 ohm source resistance will increase source loading error to 0.01% with a 10^8 ohm load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

INPUT OFFSET VOLTAGE

Bias current generates an input OFFSET voltage as result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10 nanoamperes will generate an offset voltage of 20μV if a 1000 ohm source is used, and 200μV if a 10,000 ohm source is used. In general, for the MPC8S, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_S)$$

where I_b = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{SOURCE} = Source resistance

DIFFERENTIAL MULTIPLEXER STATIC ACCURACY

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10 to 100 millivolts.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications. Refer to Figure 2.

LOAD (OUTPUT DEVICE) CHARACTERISTICS

- Use devices with very low bias current. Generaly, FET input amplifiers should be used for low level signals less than 50mV RSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be 10^{10} ohms or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC4D is used for multiplexing high-level signals of ±1 volt to ±10 volts full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

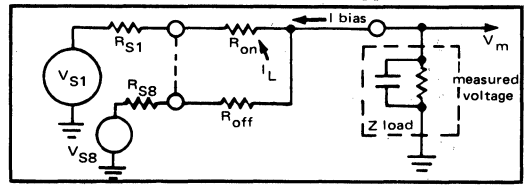


FIGURE 1: MPC8S Static Accuracy Equivalent Circuit.

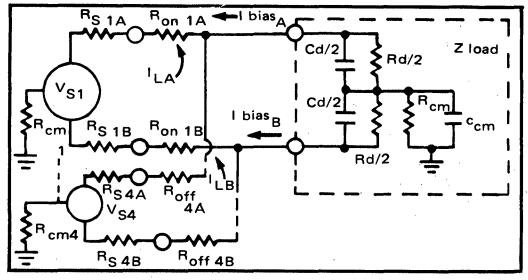


FIGURE 2: MPC4D Static Accuracy Equivalent Circuit.

SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\frac{dV}{dt}$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figure 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. If effect, the amplitude of the transients seen at the source and load are:

$$dV_{load} = \frac{i}{C}\,dt$$

where $i = C\frac{dV}{dt}$ of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in Figure 5. This graph shows the settling time for a 20 volt step change on the input. The settling time for smaller step changes on the input will be less than that shown in Figure 5.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10 volt signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the three (MPC4D) or seven (MPC8S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the R_{ON} and R_{SOURCE} impedances of the ON channel. Crosstalk is measured with a 20 volt pk-pk 1000 Hertz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in Figure 6.

COMMON-MODE REJECTION (MPC4D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC4D, protection is provided for common-mode signals of ±20 volts above the power supply voltages with no damage to the analog switches.

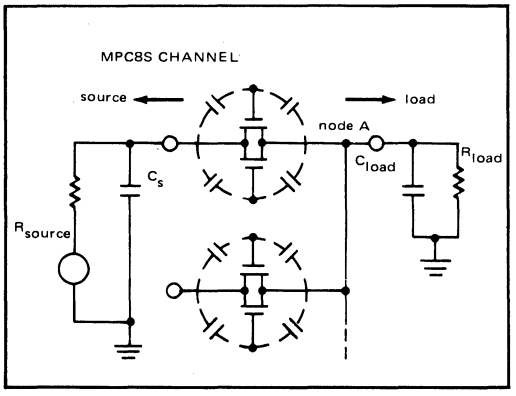


FIGURE 3: Settling Time Effects – MPC8S

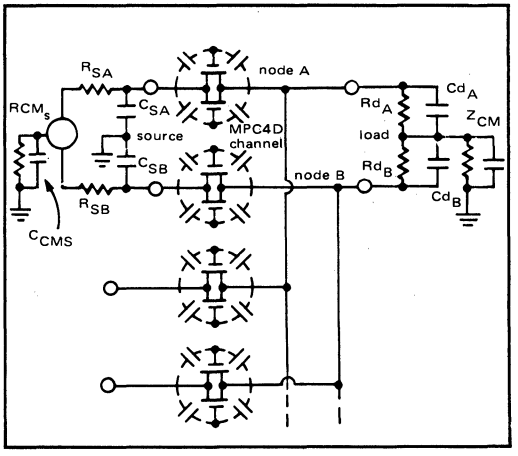


FIGURE 4: Settling & Common-Mode Effects – MPC4D.

The CMR of the MPC4D and Burr-Brown's model 3660 Instrumentation Amplifier is 120 dB at DC to 1 Hz with a 6 dB/octave rolloff to 70 dB at 1000 Hz. This measurement of CMR is shown in Figure 8 and is made with a Burr-Brown model 3660 Instrumentation Amplifier connected for a gain of 1000 and with source unbalance of 1kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

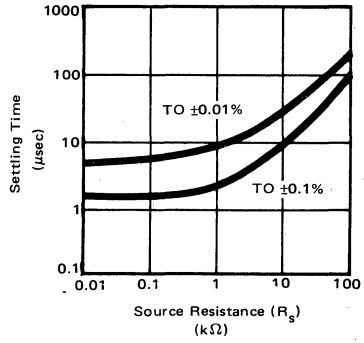


FIGURE 5. Settling time vs source resistance for 20 volt step change.

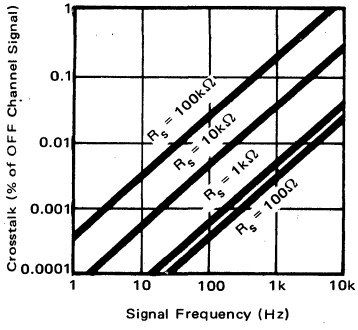


FIGURE 6. Crosstalk vs signal frequency.

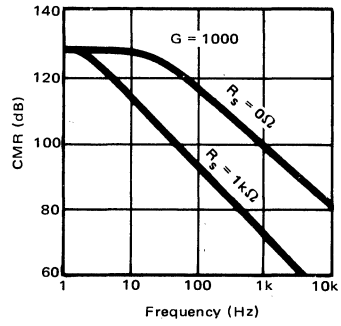


FIGURE 7. CMR vs frequency for Model 3660 IA and MPC4D (G = 1000).

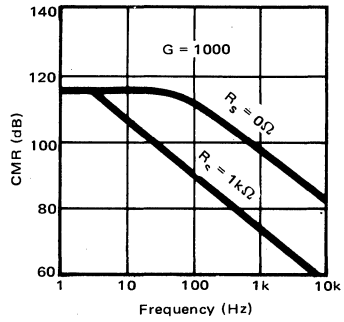


FIGURE 8. Combined CMR vs frequency for Model 3670 IA (G = 1000) and MPC4D.

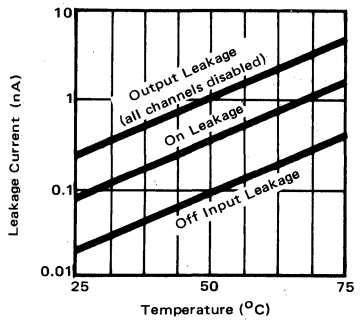


FIGURE 9. Leakage current vs temperature.

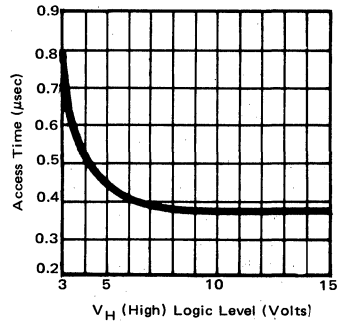


FIGURE 10. Access time vs logic level (high).

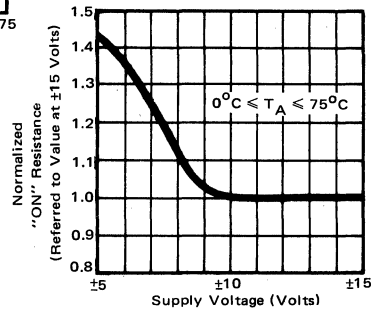


FIGURE 11. Normalized "ON" resistance vs supply voltage.

OPERATION & INSTALLATION INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 12. With ENABLE line at a logic 1, the channel is selected by the 2 bit (MPC4D) or 3 bit (MPC8S) Channel Select Address (see the Truth Tables on page 5-136) If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15 volt and/or -15 volt supply voltage is absent or shorted to ground, the MPC4D and MPC8S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Footnote 1, page 5-137).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended. See Figure 10 (access time).

To preserve common-mode rejection of the MPC4D, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

SINGLE-ENDED MULTIPLEXER (MPC8S)

Up to 32 channels (4 multiplexers) can be connected to a single node, or up to 64 channels using 9 MPC8S multiplexers on a two-tiered structure as shown in Figure 12 and 13.

DIFFERENTIAL MULTIPLEXER (MPC4D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 x 1 or 16 channels using a 4 x 4 configuration.

SINGLE NODE EXPANSION

The 32 x 1 configuration is simply eight MPC4D units tied to a single node. Programming is accomplished with a 5 bit counter, using the 2 LSB's of the counter to control Channel Address inputs A_0 and A_1 and the 3 MSB's of the counter to drive a 1 of 8 decoder. The 1 of 8 decoder then is used to drive the ENABLE inputs (pin 2) of the MPC4D multiplexers.

TWO TIER EXPANSION

Using a 4 x 4 2-tier structure for expansion to 16 channels, the programming is simplified A 4-bit counter output does not require a 1 of 8 decoder. The 2 LSB's of the counter drive the A_0 and A_1 inputs of the four first tier multiplexers and the 2 MSB's of the counter are applied to the A_0 and A_1 inputs of the second tier multiplexer.

Single vs. Multi-Tiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single node configuration, data cannot be taken from any channel, where as only one channel group is failed (4 or 8) in the multi-tiered configuration.

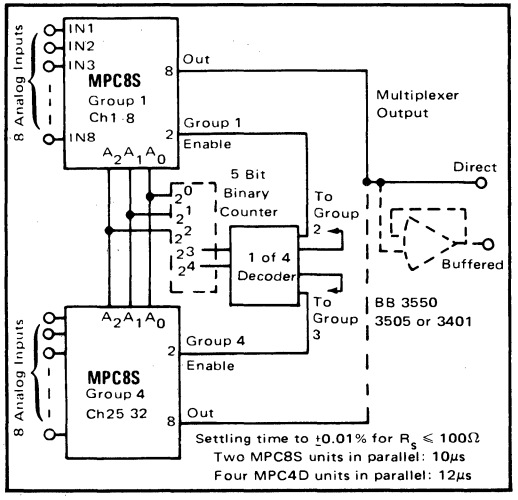


FIGURE 12. 32 Channel, Single-Tier Expansion.

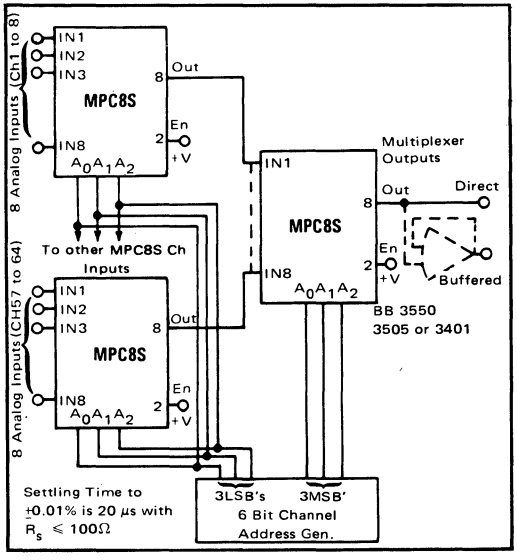


FIGURE 13. Channel Expansion Up to 64 Channels Using 8X8 Two-Tiered Expansion.

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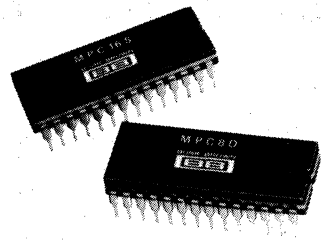

MPC8D
MPC16S

CMOS ANALOG MULTIPLEXERS

FEATURES

- LOW POWER CONSUMPTION
  - CMOS analog switches
  - 15mW at 100kHz
  - 7.5mW standby power
- COMPACT DESIGN
  - Self-contained with internal channel address decoder
  - 8-channel dual (MPC8D) for differential inputs or
  - 16-channel (MPC16S) for single-ended inputs
  - 28-pin 0.600 inch-wide space-saving package
- WILL NOT SHORT SIGNAL SOURCES
  - Break-before-make switching
- FAST SWITCHING SPEEDS PROVIDE HIGH THROUGHPUT RATES
  - 7µsec settling to 0.01%
  - 3µsec settling to 0.1%
- WIDE SUPPLY RANGE
  - ±7VDC to ±20VDC

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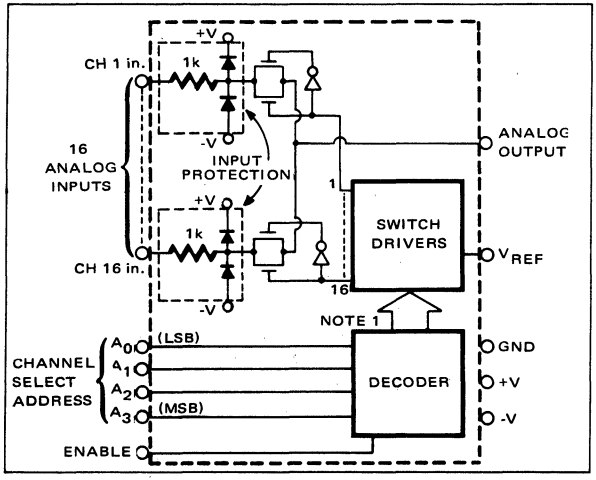
DESCRIPTION

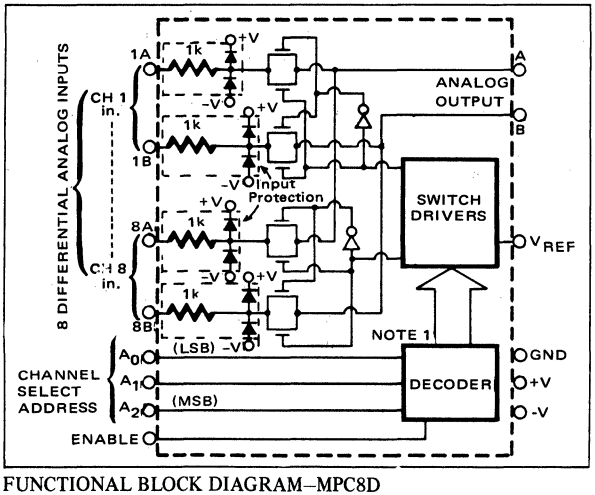
The MPC16S is single-ended monolithic 16 channel analog multiplexer and the MPC8D is a monolithic dual 8 channel analog multiplexer constructed with failure protected CMOS devices. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200 kHz from signal sources of up to ± 10 volts amplitude.

These DTL/TTL/CMOS compatible devices feature self-contained binary channel address decoding. An ENABLE line is also made available which allows the user to individually enable a 16 channel group (MPC16S) or an 8 channel group (MPC8D) facilitating channel expansion in either single-node or multi-tiered matrix configurations.

Digital and analog inputs are failure protected from either overvoltages that exceed the power supplies or from the loss of power.



FUNCTIONAL BLOCK DIAGRAM–MPC16S

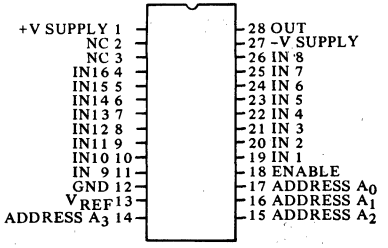


FUNCTIONAL BLOCK DIAGRAM–MPC8D

NOTE: 1 Inputs protected.

High quality processing is employed to produce CMOS FET analog channel switches which have low leakage current, high OFF resistance, low feedthrough capacitance and fast settling time.

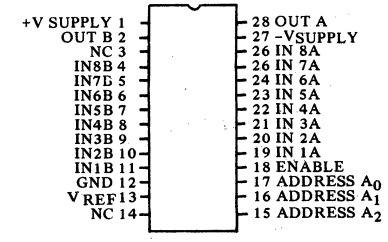
These devices are housed in compact 28 pin dual-in-line packages, and are specified for operation over a 0°C to +75°C temperature range. They are pin and package compatible with the 506/507 series.



MPC16S PIN DIAGRAM

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

TRUTH TABLE–MPC16S



MPC8D PIN DIAGRAM

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE–MPC8D

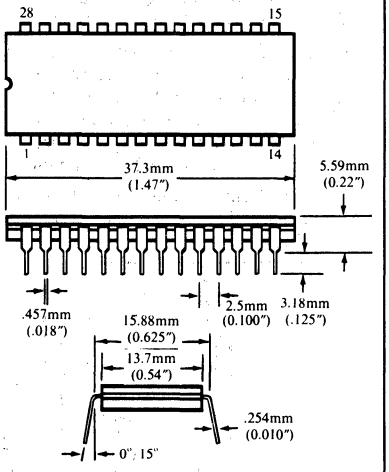
MPC8D

ELECTRICAL SPECIFICATIONS

Typical for following conditions:
V+ = +15 V, V- = -15 V, $R_{source} \leq 1000\ \Omega$, $T_A = 25^oC$ unless otherwise noted.

MODELS	MPC16S	MPC8D	Units
INPUT			
ANALOG INPUT			
Voltage Range	±15		V
Maximum Overvoltage	+V supply +20		V
	-V supply -20		V
Current at Maximum Overvoltage per Channel (1)	±18		mA
Number of Input Channels			
Single-Ended	16		
Differential		8	
Reference Voltage Range(2)	+6 to +10		V
ON Characteristics			
ON Resistance (R_{ON})			
Typical	1.3		kΩ
Maximum	1.8		kΩ
R_{ON} Drift vs. Temperature (0°C to +75°C)	0.25		%/°C
R_{ON} Mismatch			
Channel-to-channel	50	50	Ω
Differential	N/A	50	Ω
Input Leakage (I_L)	1.0		nA
Input Leakage Drift	See Figure 9		
OFF Characteristics			
OFF Resistance	10^{11}		Ω
Output Leakage (all channels disabled)	0.2		nA
Input Leakage (7)	0.02		nA
Leakage Drift	See Figure 9		
Output Leakage with Input Overvoltage			
of +35 V	1		nA
of -35 V	1		µA
DIGITAL INPUTS			
Logic "0" (V_L)(1)(3)	-V supply $\leq V_L < 0.8$ @ 1 nA		V
Logic "1" (V_H)(1)(3)	+4 $\leq V_H \leq$ +V_{supply} @ 1 nA		V
Channel Select	4 bit binary code – one of sixteen	3 bit binary code – one of eight	
Enable	Logic "0" (low) disables all channels. Logic "1" (high) enables channel select to turn on selected channel.		
POWER REQUIREMENTS			
Rated Power Supply Voltages	±15		V
Supply Range			
+ Supply	+7 to +20		V
- Supply	-7 to -20		V
Supply Drain			
At 1 MHz Switching Speed	+4, -2		mA
At 100 kHz Switching Speed	±0.5		mA
Typical Power Consumption			
DC to 10 kHz	7.5		mW
DYNAMIC CHARACTERISTICS			
Gain Error (20 MΩ load) maximum	0.01		%
Crosstalk (4)	0.005		% of OFF channel signal
Settling Time(5)			
To 2 mV (0.01%)	7		µs
To 20 mV (0.10%)	3		µs
Common-Mode Rejection (minimum)	N/A	120	dB
Switching Time			
Turn ON	0.5		µs
Turn OFF	0.3		µs
Recovery Time from Input Overvoltage Pulse of 35 V for 100 µsec			
To 0.01%	150		µs
To 0.10%	15		µs
OUTPUT			
Voltage Range	±15		V
Capacitance to Ground	50	30(6)	pF
Capacitance Mismatch	N/A	±10	%
TEMPERATURE			
Specification	0 to +75		°C
Storage	-65 to +150		°C

MECHANICAL SPECIFICATIONS



NOTES:

1. Total power dissipation due to input overvoltage current flowing in the input protection circuitry must be limited to one watt for both (a) normal operation with power supplies turned on or (b) during a fault condition when the supplies are shorted to ground.
2. Reference voltage controls noise immunity level. Normally not used (pin 13 left open).
3. Maximum overvoltage is $\pm V_{supply}$ ±4 volts @ ±15 mA. Logic levels specified are for V_{REF} (pin 13) open. For V_{REF} = +10 V, $V_{H\ MIN}$ = +6 V.
4. 20 volt peak-peak 1000 Hz sinewave; R_{source} = 1000 Ω, same signal on all unused channels.
5. For 20 volts between switched channels, R_{source} = 1000 Ω. See Figure 5 for settling time vs. source impedance (R_S).
6. From each side of MPC8D to ground.
7. Leakage measurement made with all OFF channel inputs fed in parallel to +20 volts.

DISCUSSION OF PEFORMANCE

STATIC TRANSFER ACCURACY

The static or DC transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

SINGLE-ENDED MULTIPLEXER STATIC ACCURACY

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
DC offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- Keep loading impedance as high as possible. This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of 10^8 ohms or greater will keep resistive loading errors to 0.002% or less for 1000 ohm source impedances. A 10^6 ohm load impedance will increase source loading error to 0.2% or more.
- Use sources with impedances as low as possible. A 1000 ohm source resistance will present less than 0.001% loading error and 10,000 ohm source resistance will increase source loading error to 0.01% with a 10^8 ohm load impedance.

Input resistive loading errors are determined by the following relationship: (see Figure 1)

Source and Multiplexer Resistive Loading Error

$$\in_{(R_S + R_{ON})} = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\% \text{ where } \begin{array}{l} R_S = R_{source} \\ R_L = \text{load resistance} \\ R_{ON} = \text{multiplexer ON resistance.} \end{array}$$

INPUT OFFSET VOLTAGE

Bias current generates an input OFFSET voltage as a result of the I_R drop across the multiplexer ON resistance and source resistance. A load bias current of 10 nanoamperes will generate an offset voltage of 20μVolts if a 1000 ohm source is used, and 200μVolts if a 10,000 ohm source is used. In general, for the MPC16S, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_b + I_L)(R_{ON} + R_{SOURCE})$$

where I_b = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_{SOURCE} = Source resistance

DIFFERENTIAL MULTIPLEXER STATIC ACCURACY

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full scale ranges of 10 to 100 millivolts.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low level multiplexing applications.

LOAD (OUTPUT DEVICE) CHARACTERISTICS

- Use devices with very low bias current. Generally, FET input amplifiers should be used for low level signals less than 50 mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50 mV FSR. Bias current matching will determine the input offset.
- The system DC common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be 10^{10} ohms or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC8D is used for multiplexing high-level signals of 1 volt to 10 volts full scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

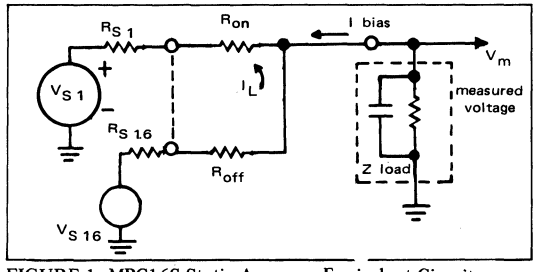


FIGURE 1: MPC16S Static Accuracy Equivalent Circuit.

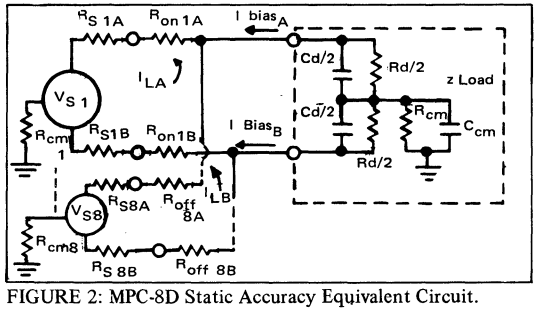


FIGURE 2: MPC-8D Static Accuracy Equivalent Circuit.

MPC8D

SETTLING TIME

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation $i = C\frac{dV}{dt}$, the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figure 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The tradeoff for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_{load} = \frac{i}{C}\,dt$$

where $i = C\frac{dV}{dt}$ of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in Figure 5. This graph shows the settling time for a 20 volt step change on the input. The settling time for smaller step changes on the input will be less than that shown in Figure 5.

SWITCHING TIME

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10 volt signal change between channels.

CROSSTALK

Crosstalk is the amount of signal feedthrough from the seven (MPC8D) or fifteen (MPC16S) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel OFF resistance and junction capacitances in series with the R_{ON} and R_{SOURCE} impedances of the ON channel. Crosstalk is measured with a 20 volt pk-pk 1000 Hertz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in Figure 6.

COMMON-MODE REJECTION (MPC8D ONLY)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC8D, protection is provided for common-mode signals of ±20 volts above the power supply voltages with no damage to the analog switches.

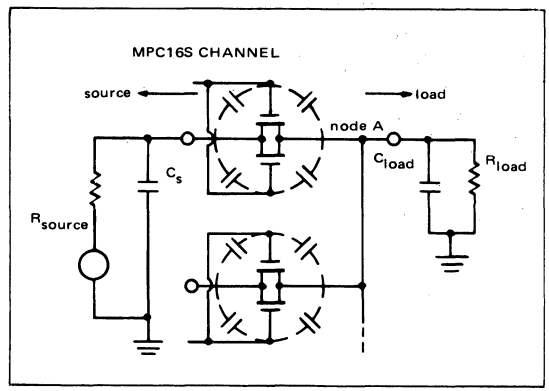


FIGURE 3: Settling Time Effects–MPC16S.

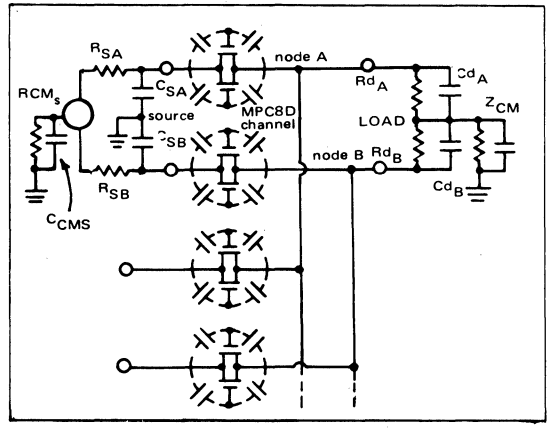


FIGURE 4: Settling & Common-Mode Effects–MPC-8D.

The CMR of the MPC8D and Burr-Brown's model 3660 Instrumentation Amplifier is 110 dB at DC to 1k Hz with a 6 dB/octave rolloff to 70 dB at 1000 Hz. This measurement of CMR is shown in Figure 8 and is made with a Burr-Brown model 3660 instrumentation amplifier connected for a gain of 1000 and with source unbalances of 10 k, 1 kΩ and no unbalance.

Factors which will degrade multiplexer and system DC CMR are:

- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR rolloff is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

TYPICAL PERFORMANCE CURVES

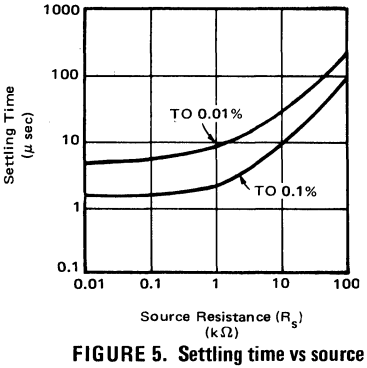


FIGURE 5. Settling time vs source resistance for 20 volt step change.

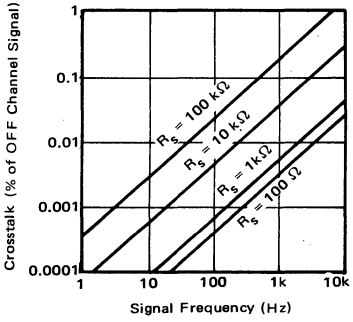


FIGURE 6. Crosstalk vs signal frequency.

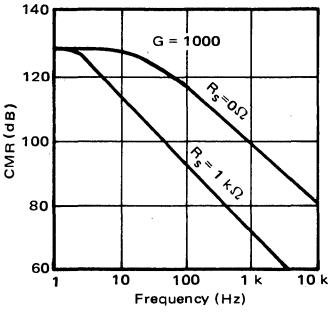


FIGURE 7. CMR vs. frequency for Model 3660 IA and MPC8D (G = 1000).

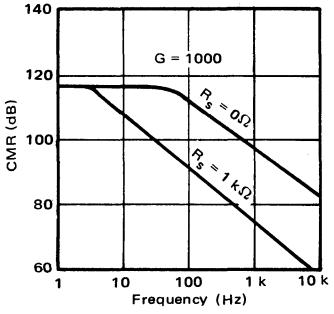


FIGURE 8. Combined CMR vs. frequency for Model 3670 IA and MPC8D (G = 1000).

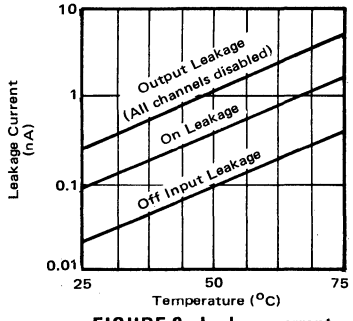


FIGURE 9. Leakage current vs temperature.

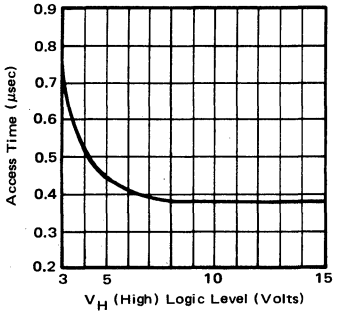


FIGURE 10. Access time vs logic level (high).

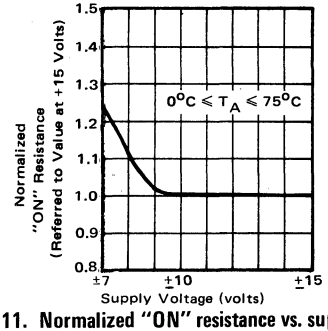


FIGURE 11. Normalized "ON" resistance vs. supply voltage.

The ENABLE input, pin 18, is included for expansion of the number of channels on a single node as illustrated in Figure 12. With the ENABLE line at a logic 1, the channel is selected by the 3 bit (MPC8D) or 4 bit (MPC16S) Channel Select Address (see the Truth Tables on page 6-275. If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15 volt and/or -15 volt supply voltage is absent or shorted to ground, the MPC8D and MPC16S multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded (see Footnote 1, page 6-276).

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended. See Figure 10 (access time).

To preserve common-mode rejection of the MPC8D, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as closely as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

SINGLE ENDED MULTIPLEXER (MPC16S)

Up to 64 channels (4 multiplexers) can be connected to a single node, or up to 256 channels using 17 MPC16S multiplexers on a two-tiered structure as shown in Figures 12 and 13.

DIFFERENTIAL MULTIPLEXER (MPC8D)

Single or multi-tiered configurations can be used to expand multiplexer channel capacity up to 64 channels using a 64 x 1 or 8 x 8 configuration.

SINGLE NODE EXPANSION

The 64 x 1 configuration is simply eight MPC8D units tied to a single node. Programming is accomplished with a 6 bit counter, using the 3 LSB's of the counter to control Channel Address inputs A_0, A_1 and A_2 and the 3 MSB's of the counter to drive an 8 or 1 decoder. The 8 of 1 decoder then is used to drive the ENABLE inputs (pin 18) of the MPC8D multiplexers.

TWO TIER EXPANSION

Using an 8 x 8 2-tier structure for expansion to 64 channels, the programming is simplified. The 6 bit counter output does not require an 8 of 1 decoder. The 3 LSB's of the counter drive the A_0, A_1 and A_2 inputs of the eight first tier multiplexers and the 3 MSB's of the counter are applied to the A_0, A_1 and A_2 inputs of the second tier multiplexer.

Single vs. Multi-Tiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single node configuration, data cannot be taken from any channel, whereas only one channel group is failed (8 or 16) in the multi-tiered configuration.

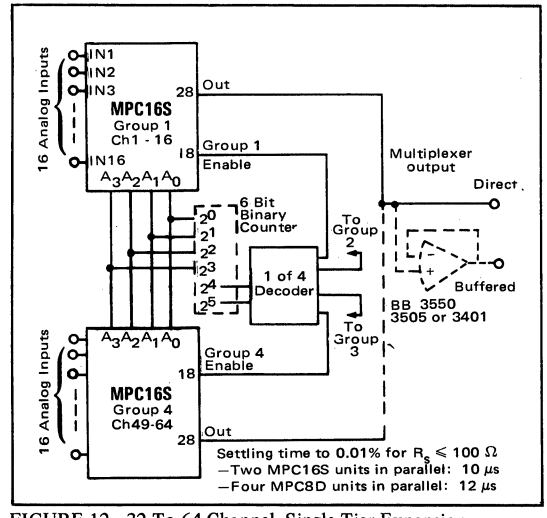


FIGURE 12. 32 To 64 Channel, Single-Tier Expansion.

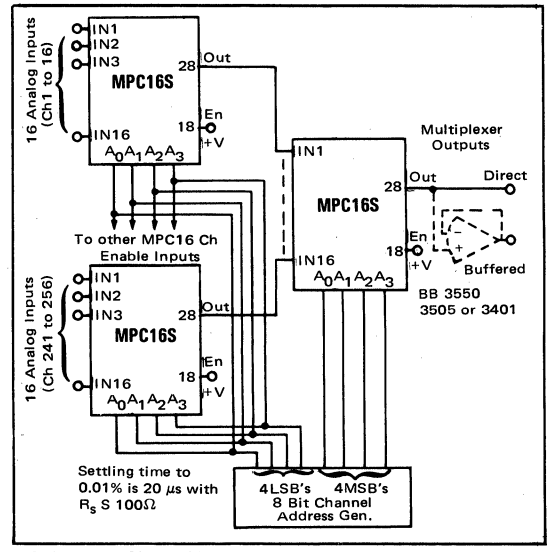


FIGURE 13. Channel Expansion Up To 256 Channels Using 16 x 16 Two Tiered Expansion.

BURR-BROWN®

PCM50KG
DESIGNED FOR AUDIO

ADVANCE INFORMATION
Subject to Change

16-Bit Hybrid DIGITAL-TO-ANALOG CONVERTER

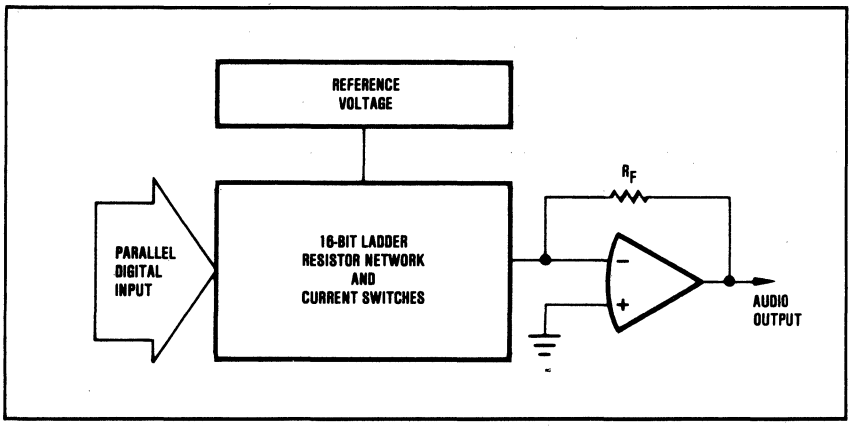
FEATURES

- 16-BIT RESOLUTION
- 5μsec SETTLING TIME Typ
- 0.003% THD (FS Input, 16 Bits) Typ
- 0.02% THD (-15dB, 16 Bits) Max
- 96dB DYNAMIC RANGE
- EIAJ STC-007-COMPATIBLE
- LOW COST
- PIN-COMPATIBLE WITH DAC71-COB-V

DESCRIPTION

The PCM50 is designed for PCM audio applications and is compatible with EIAJ STC-007 specifications. The PCM50 may be operated as either a 16-bit or a 14-bit converter. It features wide dynamic range, low distortion, and has a very-fast settling time.

The PCM50 contains an internal voltage reference. It uses state-of-the-art IC and laser-trimmed thin-film components. The converter combines high quality and high performance with low cost.



PCM50

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

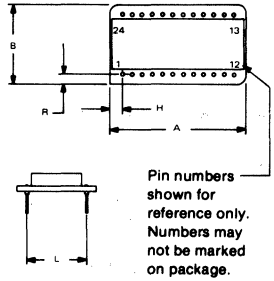
SPECIFICATIONS

ELECTRICAL

(T_A = +25°C and rated power supplies unless otherwise noted.)

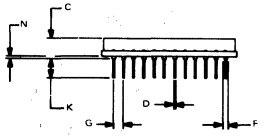
MODEL	PCM50KG MIN	PCM50KG TYP	PCM50KG MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Dynamic Range		96		dB
Logic Levels (TTL-Compatible)(1)				
Logic "1" (at +40µA)	+2.4		+5.5	VDC
Logic "0" (at -1.6mA)	0		+0.4	VDC
TRANSFER CHARACTERISTICS				
Gain Error(2)		±0.1	±0.5	%
Offset Error(2)		±10	±25	mV
Differential Linearity Error (at major carry)		0.0015		% of FSR(4)
TOTAL HARMONIC DISTORTION(3)				
V_O = ±FS at f = 400Hz				
14-Bit Resolution		0.004		%
16-Bit Resolution		0.003		%
V_O = -15dB at f = 400Hz				
14-Bit Resolution		0.02		%
16-Bit Resolution		0.01	0.02	%
V_O = -60dB at f = 400Hz				
14-Bit Resolution		4.2		%
16-Bit Resolution		1.9		%
DRIFT (Over Specified Temperature Range)				
Total Bipolar Drift (includes gain, offset, and linearity drift)		±25	±50	ppm of FSR/°C
SETTLING TIME (To ±0.006% of FSR)				
Output: 20V Step		5		µsec
1LSB Step(5)		3		µsec
Slew Rate		20		V/µsec
WARM-UP TIME	1			Min
OUTPUT				
ANALOG OUTPUT				
Ranges		±10		V
		±5(6)		V
Output Current		±5		mA
Output Impedance (DC)		0.05		Ω
Short-Circuit Duration		Indefinite To Common		
POWER SUPPLY				
SENSITIVITY				
+5VDC		±0.002		% of FSR/% V_S
-15VDC		±0.02		% of FSR/% V_S
+15VDC		±0.002		% of FSR/% V_S
POWER SUPPLY REQUIRMENTS				
Voltage, V_S	±14.5	±15	±15.5	VDC
	+4.75	+5	+5.25	VDC
Supply Drain, ±15VDC (no load)		±25		mA
+5VDC (logic supply)		±20		mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating (derated specs)	-25		+85	°C
Storage	-55		+100	°C

MECHANICAL



Pin numbers shown for reference only. Numbers may not be marked on package.

Note:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



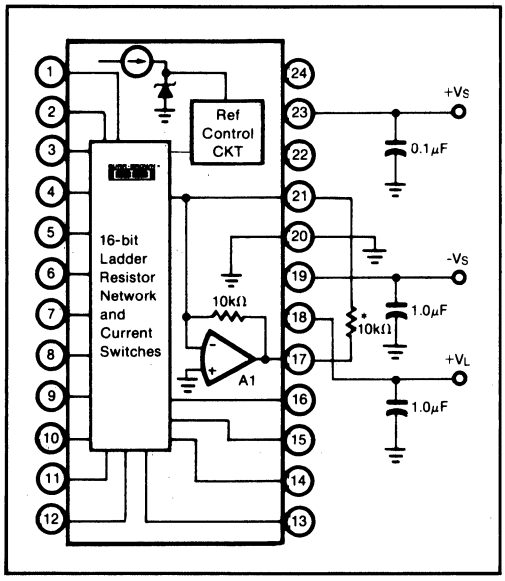
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

CASE: Black Ceramic
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

NOTES:

1. Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output (V_O) as logic 0 varies from 0.0V to +0.4V and logic 1 changes from +2.4V to +5.0V on all inputs is less than 0.006% of FSR.
2. Adjustable to zero with external trim potentiometer. (Applies only to ±10V operation.)
3. The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. A block diagram of a measurement circuit is shown in Figure 3. Burr-Brown calculates THD from the measured linearity errors using equation (2) in the section on "Total Harmonic Distortion", and specifies that the maximum THD measured with the circuit shown in Figure 3 will be less than the limits indicated.
4. FSR means Full Scale Range and is 20V for ±10V range and 10V for ±5V range.
5. LSB is for 14-bit resolution.
6. An external 10kΩ ±0.1 resistor (TCR ≤ ±50ppm/°C) must be connected from pin 21 to pin 17 to obtain a ±5V output range.

CONNECTION DIAGRAM



*±0.1% resistor (required only for ±5V output range).

PIN ASSIGNMENTS

Pin No.	
1	Bit 1 (MSB)
2	Bit 2
3	Bit 3
4	Bit 4
5	Bit 5
6	Bit 6
7	Bit 7
8	Bit 8
9	Bit 9
10	Bit 10
11	Bit 11
12	Bit 12
13	Bit 13
14	Bit 14
15	Bit 15
16	Bit 16 (LSB)
17	AUDIO OUT
18	+5VDC
19	-15VDC
20	COMMON
21	SUMMING JUNCTION
22	GAIN ADJUST
23	+15VDC
24	TEST POINT

THEORY OF OPERATION

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the minus full scale point (all bits Off), and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion (THD) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error, that is useful in audio applications. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications. The resolution of a D/A converter can be expressed in terms of Dynamic Range. The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution, or 96dB for a 16-bit converter. The actual or useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

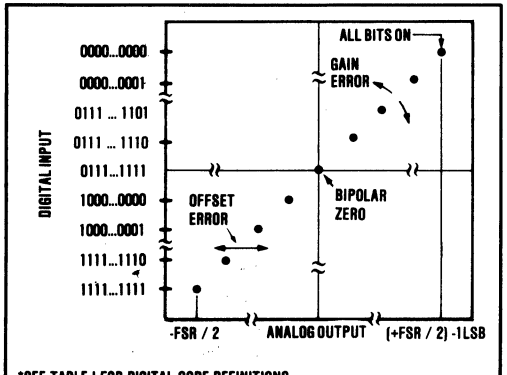


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT CODES

The PCM50 accepts complementary digital input codes in binary format. It may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes. See Table I.

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES			
		COB	CTC*
	MSB LSB	Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000...000	+Full Scale	-1LSB
Mid Scale	0111...111	Zero	-Full Scale
All bits OFF	1111...111	-Full Scale	Zero
	1000...000	-1LSB	+Full Scale

*A TTL inverter must be connected between the MSB input signal and bit 1 (pin 1) to obtain CTC input code.

DISCUSSION OF SPECIFICATIONS

The PCM50 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are total harmonic distortion, drift, gain and offset errors, and settling-time effects on accuracy. This DAC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figure 5.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM50 power supply sensitivity is specified for ±0.02% of FSR/% V_S, for -15VDC supplies and ±0.002% of FSR/% V_S, for +5VDC and +15VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

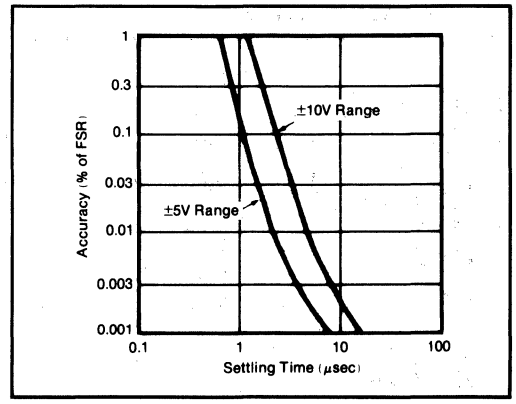


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.006% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics to the value of the rms fundamental and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM50 is shown in Figure 3. A timing diagram for the control logic is shown in Figure 4. The digital input code

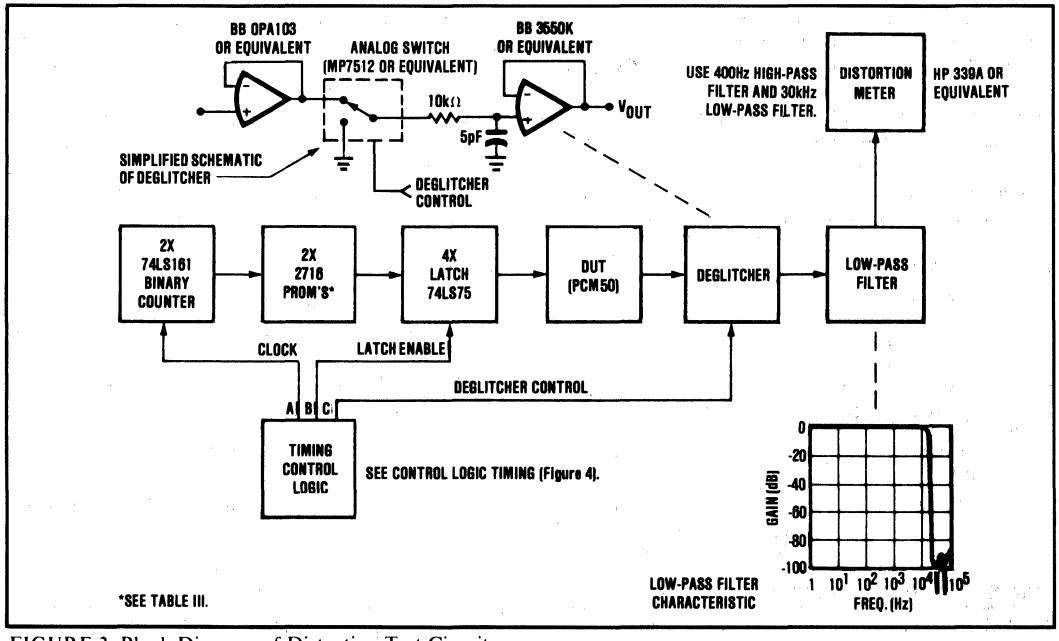


FIGURE 3. Block Diagram of Distortion Test Circuit.

stored in the PROM as well as the output obtained from an ideal PCM50, the value of an ideal sine wave, and the inherent quantization error are given in Tables III and IV. If we assume that the error due to the test circuit is negligible, then the rms value of the PCM50 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}[E_L(i) + E_Q(i)]^2} \qquad (1)$$

where N is the number of squares, $E_L(i)$ is the linearity error of the PCM50 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \qquad (2)$$

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM50 the test period was chosen to be 22.7μsec (44.056kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 400Hz and the amplitude of the input signal is -15dB down from full scale.

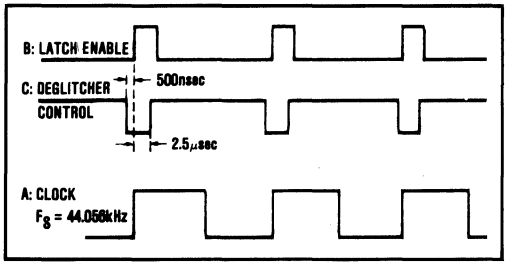


FIGURE 4. Control Logic Timing for PCM50 Distortion Test Circuit.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the PCM50.

EXTERNAL OFFSET AND GAIN ADJUST

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in Figure 5 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (20% carbon or better) should be located close to the PCM50 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 6, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust (pin 22) to Common (pin 20) to prevent noise pickup. Refer to Figure 7 for relationship of offset and gain adjustments for bipolar D/A converters.

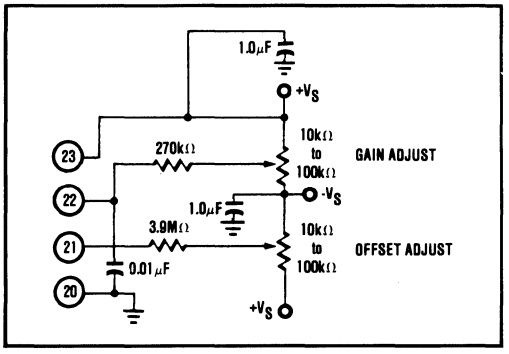


FIGURE 5. External Offset and Gain Adjust.

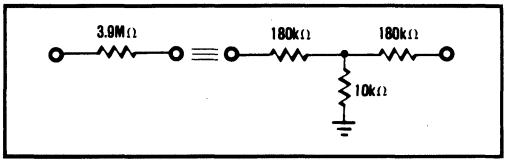


FIGURE 6. Equivalent Resistances.

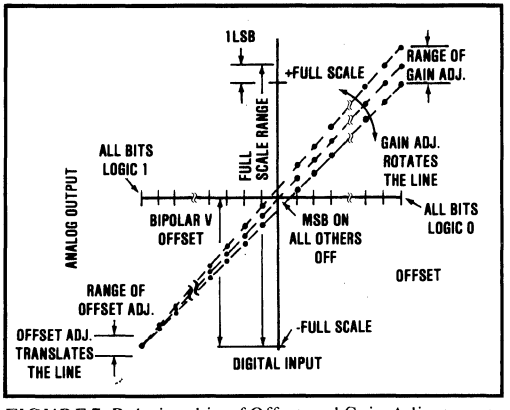


FIGURE 7. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

Apply the digital input code that should produce the maximum negative output voltage. The PCM50 is internally connected for a 20V FSR range where the maximum negative output voltage is -10V. See Table II for corresponding codes and Figure 5 for offset adjust-

ment connections. Offset adjust should be completed prior to gain adjust.

GAIN ADJUSTMENT

Apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and Figure 5 for gain adjustment connections.

TABLE II. Digital Input and Analog Output Relationships.

DIGITAL INPUT CODE	16-BIT RESOLUTION	14-BIT RESOLUTION
Complementary Bipolar Offset Binary COB ±10V		
One LSB	+305μV	+1.22mV
All Bits On 00..00	+9.99969V	+9.99878V
All Bits Off 11..11	-10.0000V	-10.0000V
±5V*		
One LSB	+152μV	+610μV
All Bits On 00..00	+4.99848V	+4.99939V
All Bits Off 11..11	-5.0000V	-5.0000V

*An external 10kΩ ±0.1% resistor must be connected from pin 17 to pin 21 to obtain ±5V range (see Connection Diagram).

INSTALLATION CONSIDERATIONS

If 16-bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5VDC through a 1kΩ resistor.

Figure 8 shows the connection diagram for a PCM50. Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance (R_L) is constant, R_1 simply introduces a gain error that can be removed during initial calibration. R_2 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{L\,min}/2^{16}$ to reduce voltage drops due to wiring to less than 1 LSB. For example, if $R_{L\,min}$ is 5kΩ, then R_1 should be less than 0.08Ω. R_L should be located as close as possible to the PCM50 for optimum performance.

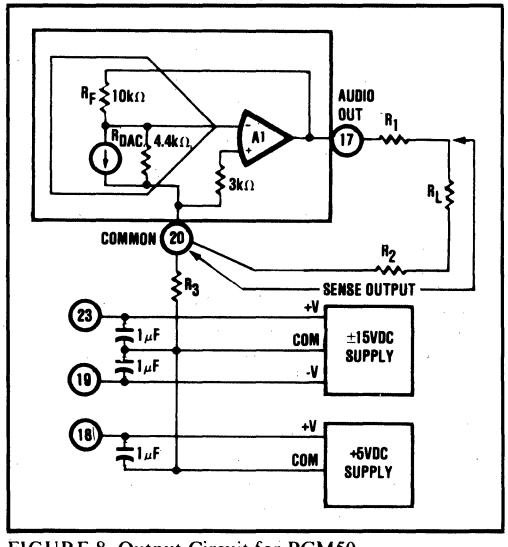


FIGURE 8. Output Circuit for PCM50

The PCM50 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

(NOTE: It is recommended that the digital input lines of the PCM50 be driven from inverters or buffers of TTL input registers to obtain best results.)

APPLICATIONS

A single PCM50 can be used for both the left and right channel as shown in Figure 9. Note that a Sample/Hold is not required.

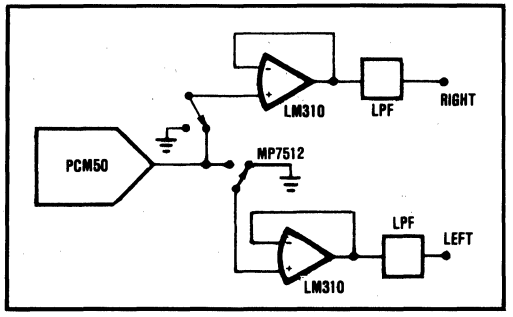


FIGURE 9. PCM50 Used for Stereo.

Table III shows the hex code loaded into the PROM's of the Distortion Test Circuit, Figure 3, for 14-bit values and Table IV shows the hex code for 16-bit values. Values are for a 400Hz sine wave (-15dB of full scale); all values are in volts.

TABLE III. Hex Code for 14-Bit Values (-15dB Output in 20V Full Scale Range).

CODE#	HEX CODE	IDEAL DAC OUT (Volts)	IDEAL SINE VALUE (Volts)	QUANTIZING ERROR (Volts)
1	7FFF	0.000000	0.000000	0.000000
2	7EB3	.101318	.101520	.000201
3	7D67	.202637	.202709	.000072
4	7C1F	.302734	.303236	.000502
5	7AD7	.402832	.402775	-.000057
6	7997	.500488	.500999	.000511
7	7857	.598145	.597590	-.000555
8	7723	.692139	.692231	.000092
9	75F3	.784912	.784614	-.000298
10	74CF	.874023	.874439	.000415
11	73AF	.961914	.961410	-.000504
12	729F	1.044922	1.045246	.000325
13	7197	1.125488	1.125673	.000185
14	709B	1.202393	1.202428	.000035
15	6FAB	1.275635	1.275261	-.000374
16	6ECB	1.343994	1.343934	-.000060
17	6DF7	1.408691	1.408223	-.000468
18	6D33	1.468506	1.467920	-.000586
19	6C7F	1.523438	1.522828	-.000610
20	6BDF	1.572266	1.572769	.000503
21	6B4B	1.617432	1.617580	.000148
22	6AC7	1.657715	1.657115	-.000600
23	6A5B	1.690674	1.691244	.000570
24	69FB	1.719971	1.719857	-.000113
25	69AF	1.743164	1.742861	-.000303
26	6977	1.760254	1.760179	-.000075
27	6953	1.771240	1.771756	.000516
28	693F	1.777344	1.777554	.000210
29	693F	1.777344	1.777554	.000210
30	6953	1.771240	1.771756	.000516
31	6977	1.760254	1.760179	-.000075
32	69AF	1.743164	1.742861	-.000303
33	69FB	1.719971	1.719857	-.000113
34	6A5B	1.690674	1.691244	.000570
35	6AC7	1.657715	1.657115	-.000600
36	6B4B	1.617432	1.617580	.000148
37	6BDF	1.572266	1.572769	.000503
38	6C7F	1.523438	1.522828	-.000610
39	6D33	1.468506	1.467920	-.000586
40	6DF7	1.408691	1.408223	-.000468
41	6ECB	1.343994	1.343934	-.000060
42	6FAB	1.275635	1.275261	-.000374
43	709B	1.202393	1.202428	.000035
44	7197	1.125488	1.125673	.000185
45	729F	1.044922	1.045246	.000325
46	73AF	.961914	.961410	-.000504
47	74CF	.874023	.874439	.000415
48	75F3	.784912	.784614	-.000298
49	7723	.692139	.692231	.000092
50	7857	.598145	.597590	-.000555
51	7997	.500488	.500999	.000511
52	7AD7	.402832	.402775	-.000057
53	7C1F	.302734	.303236	.000502
54	7D67	.202637	.202709	.000072
55	7EB3	.101318	.101520	.000201

CODE#	HEX CODE	IDEAL DAC OUT (Volts)	IDEAL SINE VALUE (Volts)	QUANTIZING ERROR (Volts)
56	7FFF	0.000000	0.000000	0.000000
57	814B	-.101318	-.101520	-.000201
58	8297	-.202637	-.202709	-.000072
59	83DF	-.302734	-.303236	-.000502
60	8527	-.402832	-.402775	.000057
61	8667	-.500488	-.500999	-.000511
62	87A7	-.598145	-.597590	.000555
63	88DB	-.692139	-.692231	-.000092
64	8A0B	-.784912	-.784614	.000298
65	8B2F	-.874023	-.874439	-.000415
66	8C4F	-.961914	-.961410	.000504
67	8D5F	-1.044922	-1.045246	-.000325
68	8E67	-1.125488	-1.125673	-.000185
69	8F63	-1.202393	-1.202428	-.000035
70	9053	-1.275635	-1.275261	.000374
71	9133	-1.343994	-1.343934	.000060
72	9207	-1.408691	-1.408223	.000468
73	92CB	-1.468506	-1.467920	.000586
74	937F	-1.523438	-1.522828	.000610
75	941F	-1.572266	-1.572769	-.000503
76	94B3	-1.617432	-1.617580	-.000148
77	9537	-1.657715	-1.657115	.000600
78	95A3	-1.690674	-1.691244	-.000570
79	9603	-1.719971	-1.719857	.000113
80	964F	-1.743164	-1.742861	.000303
81	9687	-1.760254	-1.760179	.000075
82	96AB	-1.771240	-1.771756	-.000516
83	96BF	-1.777344	-1.777554	-.000210
84	96BF	-1.777344	-1.777554	-.000210
85	96AB	-1.771240	-1.771756	-.000516
86	9687	-1.760254	-1.760179	.000075
87	964F	-1.743164	-1.742861	.000303
88	9603	-1.719971	-1.719857	.000113
89	95A3	-1.690674	-1.691244	-.000570
90	9537	-1.657715	-1.657115	.000600
91	94B3	-1.617432	-1.617580	-.000148
92	941F	-1.572266	-1.572769	-.000503
93	937F	-1.523438	-1.522828	.000610
94	92CB	-1.468506	-1.467920	.000586
95	9207	-1.408691	-1.408223	.000468
96	9133	-1.343994	-1.343934	.000060
97	9053	-1.275635	-1.275261	.000374
98	8F63	-1.202393	-1.202428	-.000035
99	8E67	-1.125488	-1.125673	-.000185
100	8D5F	-1.044922	-1.045246	-.000325
101	8C4F	-.961914	-.961410	.000504
102	8B2F	-.874023	-.874439	-.000415
103	8A0B	-.784912	-.784614	.000298
104	88DB	-.692139	-.692231	-.000092
105	87A7	-.598145	-.597590	.000555
106	8667	-.500488	-.500999	-.000511
107	8527	-.402832	-.402775	.000057
108	83DF	-.302734	-.303236	-.000502
109	8297	-.202637	-.202709	-.000072
110	814B	-.101318	-.101520	-.000201

TABLE IV. Hex Code for 16-Bit Values (-15dB Output in 20V Full Scale Range).

CODE#	HEX CODE	IDEAL DAC OUT (Volts)	IDEAL SINE VALUE (Volts)	QUANTIZING ERROR (Volts)
1	7FFF	0.000000	0.000000	0.000000
2	7EB2	.101624	.101520	-.000104
3	7D67	.202637	.202709	.000072
4	7C1D	.303345	.303236	-.000109
5	7AD7	.402832	.402775	-.000057
6	7995	.501099	.500999	-.000099
7	7859	.597534	.597590	.000056
8	7723	.692139	.692231	.000092
9	75F4	.784607	.784614	.000007
10	74CE	.874329	.874439	.000110
11	73B1	.961304	.961410	.000107
12	729E	1.045227	1.045246	.000019
13	7196	1.125793	1.125673	-.000120
14	709B	1.202393	1.202428	.000035
15	6FAC	1.275330	1.275261	-.000069
16	6ECB	1.343994	1.343934	-.000060
17	6DF9	1.408081	1.408223	.000142
18	6D35	1.467896	1.467920	.000024
19	6C81	1.522827	1.522828	.000001
20	6BDD	1.572876	1.572769	-.000107
21	6B4B	1.617432	1.617580	.000148
22	6AC9	1.657104	1.657115	.000010
23	6A59	1.691284	1.691244	-.000040
24	69FB	1.719971	1.719857	-.000113
25	69B0	1.742859	1.742861	.000002
26	6977	1.760254	1.760179	-.000075
27	6951	1.771851	1.771756	-.000094
28	693E	1.777649	1.777554	-.000095
29	693E	1.777649	1.777554	-.000095
30	6951	1.771851	1.771756	-.000094
31	6977	1.760254	1.760179	-.000075
32	69B0	1.742859	1.742861	.000002
33	69FB	1.719971	1.719857	-.000113
34	6A59	1.691284	1.691244	-.000040
35	6AC9	1.657104	1.657115	.000010
36	6B4B	1.617432	1.617580	.000148
37	6BDD	1.572876	1.572769	-.000107
38	6C81	1.522827	1.522828	.000001
39	6D35	1.467896	1.467920	.000024
40	6DF9	1.408081	1.408223	.000142
41	6ECB	1.343994	1.343934	-.000060
42	6FAC	1.275330	1.275261	-.000069
43	709B	1.202393	1.202428	.000035
44	7196	1.125793	1.125673	-.000120
45	729E	1.045227	1.045246	.000019
46	73B1	.961304	.961410	.000107
47	74CE	.874329	.874439	.000110
48	75F4	.784607	.784614	.000007
49	7723	.692139	.692231	.000092
50	7859	.597534	.597590	.000056
51	7995	.501099	.500999	-.000099
52	7AD7	.402832	.402775	-.000057
53	7C1D	.303345	.303236	-.000109
54	7D67	.202637	.202709	.000072
55	7EB2	.101624	.101520	-.000104

CODE#	HEX CODE	IDEAL DAC OUT (Volts)	IDEAL SINE VALUE (Volts)	QUANTIZING ERROR (Volts)
56	7FFF	0.000000	0.000000	0.000000
57	814C	-.101624	-.101520	.000104
58	8297	-.202637	-.202709	-.000072
59	83E1	-.303345	-.303236	.000109
60	8527	-.402832	-.402775	.000057
61	8669	-.501099	-.500999	.000099
62	87A5	-.597534	-.597590	-.000056
63	88DB	-.692139	-.692231	-.000092
64	8A0A	-.784607	-.784614	-.000007
65	8B30	-.874329	-.874439	-.000110
66	8C4D	-.961304	-.961410	-.000107
67	8D60	-1.045227	-1.045246	-.000019
68	8E68	-1.125793	-1.125673	.000120
69	8F63	-1.202393	-1.202428	-.000035
70	9052	-1.275330	-1.275261	.000069
71	9133	-1.343994	-1.343934	.000060
72	9205	-1.408081	-1.408223	-.000142
73	92C9	-1.467896	-1.467920	-.000024
74	937D	-1.522827	-1.522828	-.000001
75	9421	-1.572876	-1.572769	.000107
76	94B3	-1.617432	-1.617580	-.000148
77	9535	-1.657104	-1.657115	-.000010
78	95A5	-1.691284	-1.691244	.000040
79	9603	-1.719971	-1.719857	.000113
80	964E	-1.742859	-1.742861	-.000002
81	9687	-1.760254	-1.760179	.000075
82	96AD	-1.771851	-1.771756	.000094
83	96C0	-1.777649	-1.777554	.000095
84	96C0	-1.777649	-1.777554	.000095
85	96AD	-1.771851	-1.771756	.000094
86	9687	-1.760254	-1.760179	.000075
87	964E	-1.742859	-1.742861	-.000002
88	9603	-1.719971	-1.719857	.000113
89	95A5	-1.691284	-1.691244	.000040
90	9535	-1.657104	-1.657115	-.000010
91	94B3	-1.617432	-1.617580	-.000148
92	9421	-1.572876	-1.572769	.000107
93	937D	-1.522827	-1.522828	-.000001
94	92C9	-1.467896	-1.467920	-.000024
95	9205	-1.408081	-1.408223	-.000142
96	9133	-1.343994	-1.343934	.000060
97	9052	-1.275330	-1.275261	.000069
98	8F63	-1.202393	-1.202428	-.000035
99	8E68	-1.125793	-1.125673	.000120
100	8D60	-1.045227	-1.045246	-.000019
101	8C4D	-.961304	-.961410	-.000107
102	8B30	-.874329	-.874439	-.000110
103	8A0A	-.784607	-.784614	-.000007
104	88DB	-.692139	-.692231	-.000092
105	87A5	-.597534	-.597590	-.000056
106	8669	-.501099	-.500999	.000099
107	8527	-.402832	-.402775	.000057
108	83E1	-.303345	-.303236	.000109
109	8297	-.202637	-.202709	-.000072
110	814C	-.101624	-.101520	.000104

BURR-BROWN®

PCM51JG
DESIGNED FOR AUDIO

ADVANCE INFORMATION
Subject to Change

16-Bit DIGITAL-TO-ANALOG CONVERTER

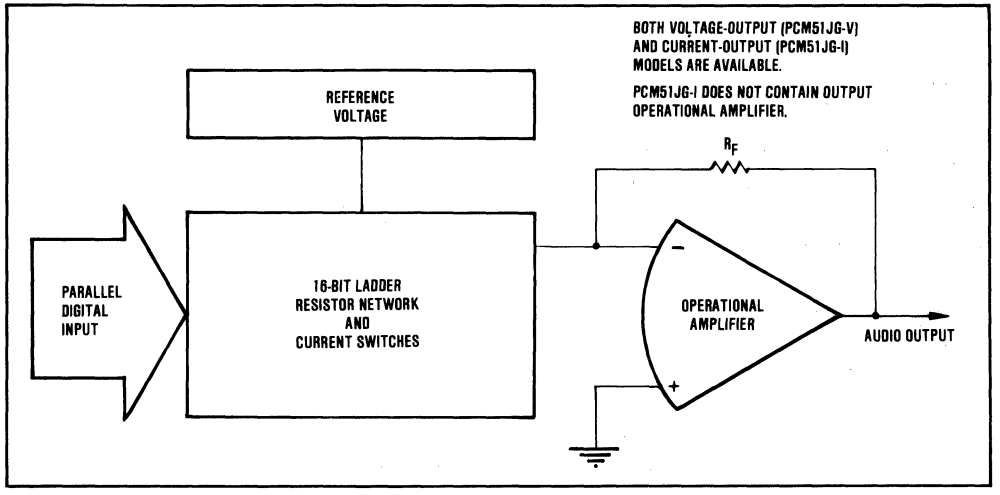
FEATURES

- 16-BIT RESOLUTION
- 350nsec SETTLING TIME, typ (I Model)
- 5μsec SETTLING TIME, typ (V Model)
- 0.006% OF FSR MAX DIFFERENTIAL LINEARITY ERROR (0.0025% typ)
- 0.0025% THD (FS Input, 16 Bits), typ
- 0.012% THD (-15dB, 16 Bits), typ
- 96dB DYNAMIC RANGE
- EIAJ STC-007 COMPATIBLE
- PIN COMPATIBLE - DAC71 & PCM50
- LOW COST

DESCRIPTION

The PCM51 is designed for PCM audio applications and is compatible with EIAJ STC-007 specifications. The PCM51 may be operated as either a 16-bit or a 14-bit converter. It features wide dynamic range, low differential linearity error, low distortion, and has a very-fast settling time.

The PCM51 contains an internal voltage reference. It uses state-of-the-art IC and laser-trimmed thin-film components. The converter combines high quality and high performance with low cost.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

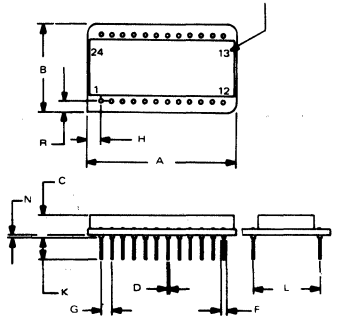
(T_A = +25°C and rated power supplies unless otherwise noted.)

MODEL	PCM51JG MIN	PCM51JG TYP	PCM51JG MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Dynamic Range		96		dB
Logic Levels (TTL-Compatible)(1)				
Logic "1" at +40µA	+2.4		+5.5	VDC
Logic "0" at -1.6mA	0		+0.4	VDC
TRANSFER CHARACTERISTICS				
Gain Error		±0.1	±0.5	%
Bipolar Zero Error(2)		±10	±100	mV
Differential Linearity Error at Bipolar Zero		0.0025	0.006	% of FSR(3)
TOTAL HARMONIC DISTORTION(4)				
V_O = ±FS at f = 400Hz				
14-Bit Resolution		0.004		%
16-Bit Resolution		0.0025	0.005	%
V_O = -15dB at f = 400Hz				
14-Bit Resolution		0.023	0.06	%
16-Bit Resolution		0.012	0.04	%
V_O = -20dB at f = 400Hz				
14-Bit Resolution		0.04		%
16-Bit Resolution		0.025		%
V_O = -60dB at f = 400Hz				
14-Bit Resolution		4.2		%
16-Bit Resolution		1.9		%
DRIFT (Over Specified Temperature Range)				
Total Bipolar Drift (includes gain, offset, and linearity drift)		±25	±50	ppm of FSR/°C
SETTLING TIME (To ±0.006% of FSR)				
Voltage Model, PCM51JG-V				
Output: 20V Step		5		µsec
1LSB Step(5)		3		µsec
Slew Rate		20		V/µsec
Current Model, PCM51JG-I				
Output: 1mA Step				
10Ω to 100Ω load		350		nsec
1kΩ Load(6)		350		nsec
WARM-UP TIME	1			Min
OUTPUT				
ANALOG OUTPUT				
Voltage Model, PCM51JG-V				
Ranges		±10		V
		±5(7)		V
Output Current		±5		mA
Output Impedance (DC)		0.1		Ω
Short-Circuit Duration		Indefinite To Common		
Current Model, PCM51JG-I				
Range		±1		mA
Output Impedance		3		kΩ
POWER SUPPLY				
SENSITIVITY				
-15VDC		±0.02		% of FSR/% V_S
+15VDC		±0.002		% of FSR/% V_S
POWER SUPPLY REQUIRMENTS				
Voltage, V_S	±14.5,	±15	±15.5	VDC
Supply Drain, +15VDC (no load)		±25		mA
-15VDC		-40		mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating (derated specs)	-25		+85	°C
Storage	-55		+85	°C

MECHANICAL

NOTE: Leads in true position. Within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



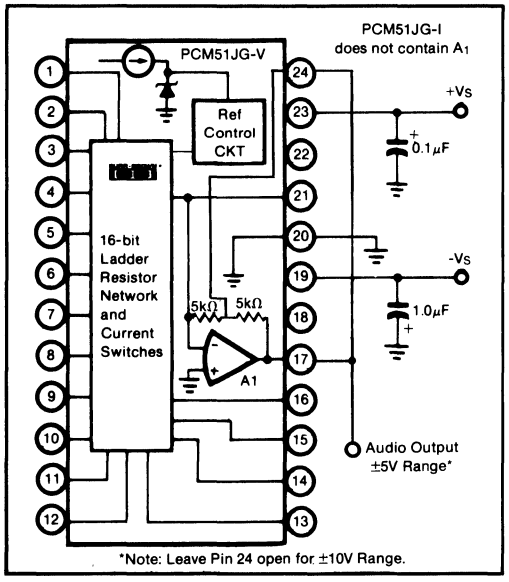
CASE: Black Ceramic
MATING CONNECTOR: 245MC
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	.085	.105	2.16	2.67

NOTES:

1. Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output (V_O) as logic 0 varies from 0.0V to +0.4V and logic 1 changes from +2.4V to +5.0V on all inputs is less than 0.006% of FSR.
2. Adjustable to zero with external trim potentiometer.
3. FSR means Full Scale Range and is 20V for ±10V range and 10V for ±5V range.
4. The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. A block diagram of a measurement circuit is shown in Figure 3. Burr-Brown calculates THD from the measured linearity errors using equation (2) in the section on "Total Harmonic Distortion", and specifies that the maximum THD measured with the circuit shown in Figure 3 will be less than the limits indicated.
5. LSB is for 14-bit resolution.
6. Measured with an active clamp, as shown in Figure 10, to provide a low impedance for approximately 200nsec.
7. Connect pin 24 to pin 17 to obtain ±5V range.

CONNECTION DIAGRAM



PIN ASSIGNMENTS

Pin No.	PCM51JG-I	Pin No.	PCM51JG-V
1	Bit 1 (MSB)	1	Bit 1 (MSB)
2	Bit 2	2	Bit 2
3	Bit 3	3	Bit 3
4	Bit 4	4	Bit 4
5	Bit 5	5	Bit 5
6	Bit 6	6	Bit 6
7	Bit 7	7	Bit 7
8	Bit 8	8	Bit 8
9	Bit 9	9	Bit 9
10	Bit 10	10	Bit 10
11	Bit 11	11	Bit 11
12	Bit 12	12	Bit 12
13	Bit 13	13	Bit 13
14	Bit 14	14	Bit 14
15	Bit 15	15	Bit 15
16	Bit 16 (LSB)	16	Bit 16 (LSB)
17	±10V RANGE SELECT	17	AUDIO OUT
18	NO CONNECTION	18	NO CONNECTION
19	-15VDC	19	-15VDC
20	COMMON	20	COMMON
21	IOUT	21	SUMMING JUNCTION
22	NO CONNECTION	22	NO CONNECTION
23	+15VDC	23	+15VDC
24	±5V RANGE SELECT	24	±5V RANGE SELECT

THEORY OF OPERATION

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Offset or Bipolar zero errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the minus full scale point (all bits Off), and Offset drift shifts the line left or right over the operating temperature range. Most of the offset and gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the bipolar zero voltage is virtually unaffected by variations in the reference voltage. Total Harmonic Distortion (THD) is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications. The resolution of a D/A converter can be expressed in terms of Dynamic Range. The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution, or 96dB for a 16-bit converter. The actual or useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

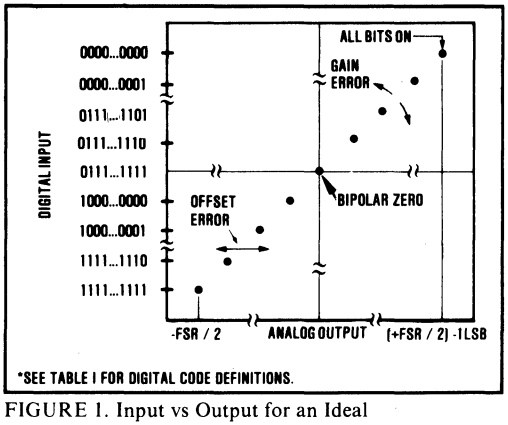


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT CODES

The PCM51 accepts complementary digital input codes in binary format. It may be connected by the user for

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES			
		COB	CTC*
	MSB LSB	Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000...000	+Full Scale	-1LSB
Mid Scale	0111...111	Zero	-Full Scale
All bits OFF	1111...111	-Full Scale	Zero
	1000...000	-1LSB	-Full Scale

*A TTL inverter must be connected between the MSB input signal and bit 1 (pin 1) to obtain CTC input code.

either complementary offset binary (COB) or complementary two's complement (CTC) codes. See Table I.

DISCUSSION OF SPECIFICATIONS

The PCM51 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are total harmonic distortion, differential linearity error, bipolar zero error, parameter shifts with time and temperature, and settling-time effects on accuracy. This DAC is factory-trimmed and tested for all critical key specifications.

BIPOLAR ZERO ERROR

Initial bipolar zero error (Bit 1 "ON" and all other bits "OFF") is factory-trimmed to typically ±20mV (±100mV maximum) at +25°C. This error may be trimmed to zero by connecting the external trim potentiometer shown in Figure 6.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at bipolar zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM51 is factory-trimmed to typically ±0.0025% of FSR (±0.006% of FSR, maximum).

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the offset and gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM51 is designed so that these drifts are in opposite directions so that the bipolar zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM51 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very-low to further enhance their stability.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM51 power supply sensitivity is specified for ±0.02% of FSR/% V_S, for -15VDC supplies and ±0.002% of FSR/% V_S, for +15VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME (PCM51JG-V)

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

Settling times are specified to ±0.006% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

SETTLING TIME (PCM51-JG-I)

Two settling times are specified to a ±0.006% of FSR. Each is given for current model connected with two different resistive loads: 10Ω to 200Ω and 1000Ω. Current-output model settling time is particularly important if the PCM51JG-I is going to be used to build a successive-approximation A/D converter. See Figure 11.

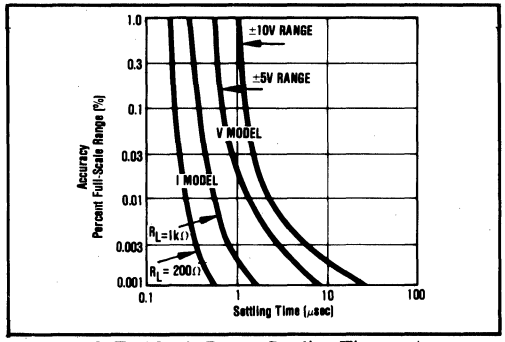


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics to the value of the rms fundamental and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM51 is shown in Figure 3. A timing diagram for the control logic is shown in Figure 4. The digital input code stored in the PROM as well as the output obtained from an ideal PCM51, the value of an ideal sine wave, and the inherent quantization error are given in Tables III and IV. If we assume that the error due to the test circuit is negligible, then the rms value of the PCM51 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{1/N \sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2} \quad (1)$$

where N is the number of squares, $E_L(i)$ is the linearity error of the PCM51 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \epsilon_{rms}/E_{rms} = \frac{\sqrt{1/N \sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \quad (2)$$

This expression indicates that, in general, there is a correlation between the THD and the square root of the

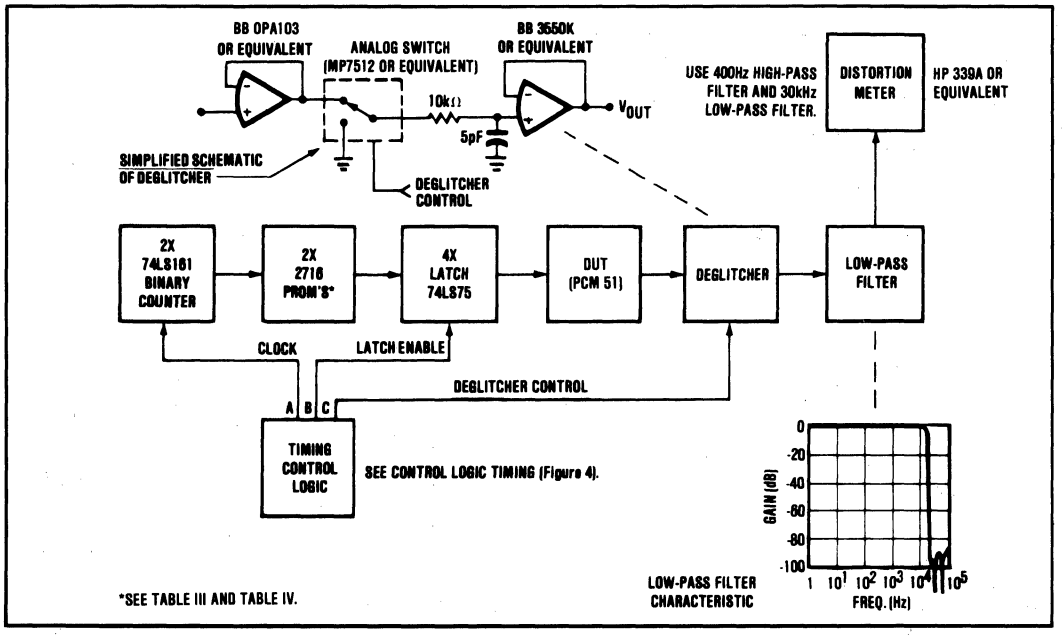


FIGURE 3. Block Diagram of Distortion Test Circuit.

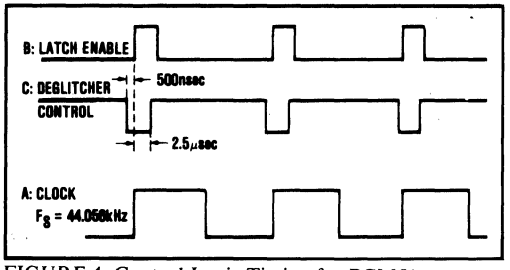


FIGURE 4. Control Logic Timing for PCM51 Distortion Test Circuit.

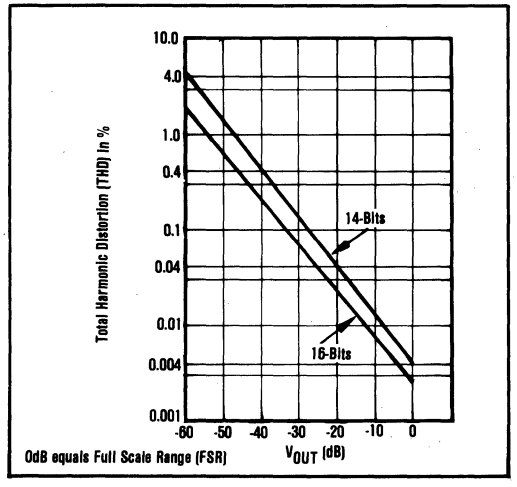


FIGURE 5. Total Harmonic Distortion (THD) vs V_{OUT}.

sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM51 the test period was chosen to be 22.7μsec (44.056kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 400Hz and the amplitude of the input signal is -15dB down from full scale.

Figure 5 shows the typical THD as a function of output voltage.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the PCM51.

EXTERNAL BIPOLAR ZERO ADJUST (OPTIONAL)

In some applications the bipolar zero error may require adjustment. This error may be adjusted to zero by installing an external potentiometer as shown in Figure 6.

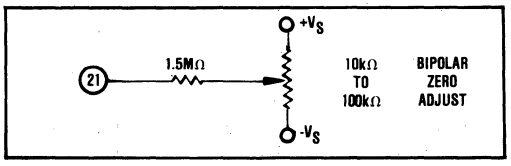


FIGURE 6. Optional External Bipolar Zero Adjust.

The TCR of the potentiometer should be 100ppm/°C or less. The 1.5MΩ resistor (20% carbon or better) should be located close to the PCM51 to prevent noise pickup. Refer to Figure 7 for the relationship of bipolar zero adjust on the D/A converter transfer function.

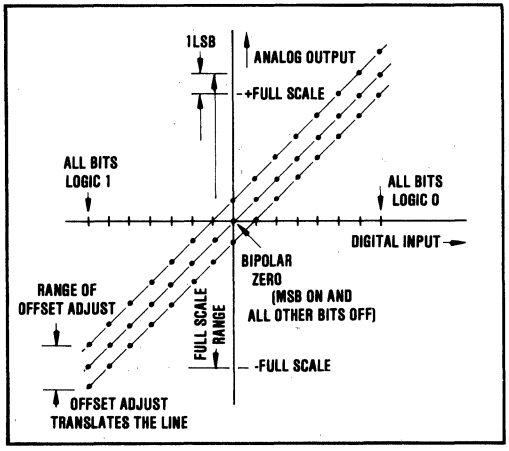


FIGURE 7. Affect of Offset Adjustment on a Bipolar D/A Converter Transfer Function.

ADJUSTMENT PROCEDURE

Apply the digital input code that should produce zero volts output (bit 1 or MSB "ON" and all other bits "OFF"). Adjust the offset potentiometer until zero volts is obtained.

Table II shows the ideal plus and minus full scale voltages and LSB values for both 14- and 16-bit resolution and ±10V, ±5V, and ±1mA output ranges.

TABLE II. Digital Input and Analog Output Relationships.

	OUTPUT CODE			
	VOLTAGE		CURRENT	
DIGITAL INPUT CODE	16-Bit Resolution	14-Bit Resolution	16-Bit Resolution	14-Bit Resolution
Complementary Bipolar Offset Binary COB ±10V or ±1mA				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits On (00..00)	+9.99969V	+9.99878V	-0.99997mA	-0.99988mA
All Bits Off (11..11)	-10.0000V	-10.0000V	+1.0000mA	+1.0000mA
±5V or ±1mA*				
One LSB	+152μV	+610μV	0.031μA	0.122μA
All Bits On (00..00)	+4.99848V	+4.99939V	-0.99997mA	-0.99988mA
All Bits Off (11..11)	-5.0000V	-5.0000V	+1.0000mA	+1.0000mA

*Connect pin 24 to pin 17 to obtain ±5V Range.

INSTALLATION CONSIDERATIONS

If 16-bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5VDC through a 1kΩ resistor.

Figure 8 shows the connection diagram for a PCM51. Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance (R_L) is constant, R_1 simply introduces a gain error. R_2 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_1 should be less than 0.08Ω. R_L should be located as close as possible to the PCM51 for optimum performance.

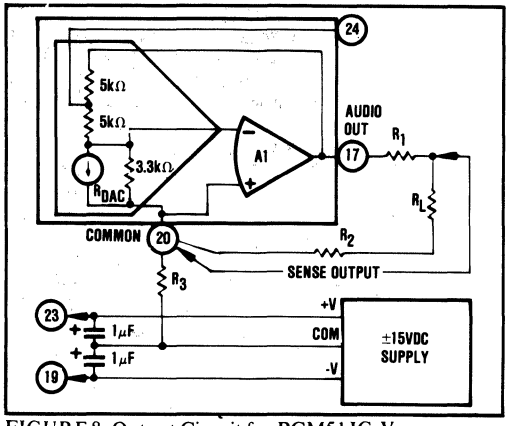


FIGURE 8. Output Circuit for PCM51JG-V.

The PCM51 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

See Figure 9 for the connection diagram of a PCM51JG-I current-to-voltage converter. R_1 through R_4 represent lead and contact resistances.

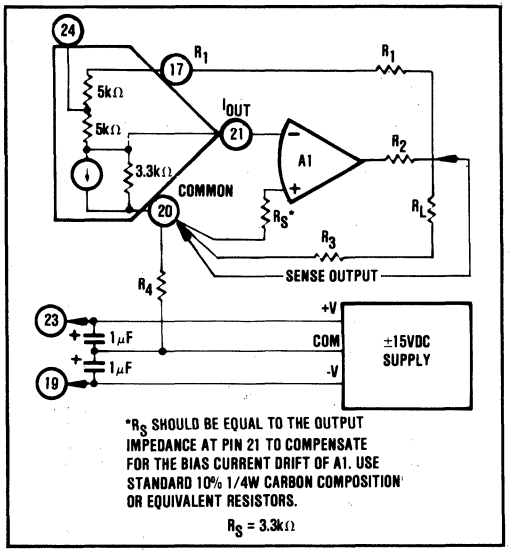


FIGURE 9. Preferred External Op Amp Configuration for PCM51JG-I

APPLICATIONS

A single PCM51 can be used for both the left and right channel as shown in Figure 10. Note that a Sample/Hold is not required.

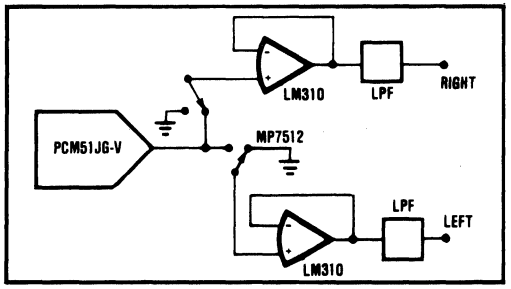


FIGURE 10. PCM51 Used for Stereo.

An A/D converter can be constructed using the PCM51JG-I shown in Figure 11.

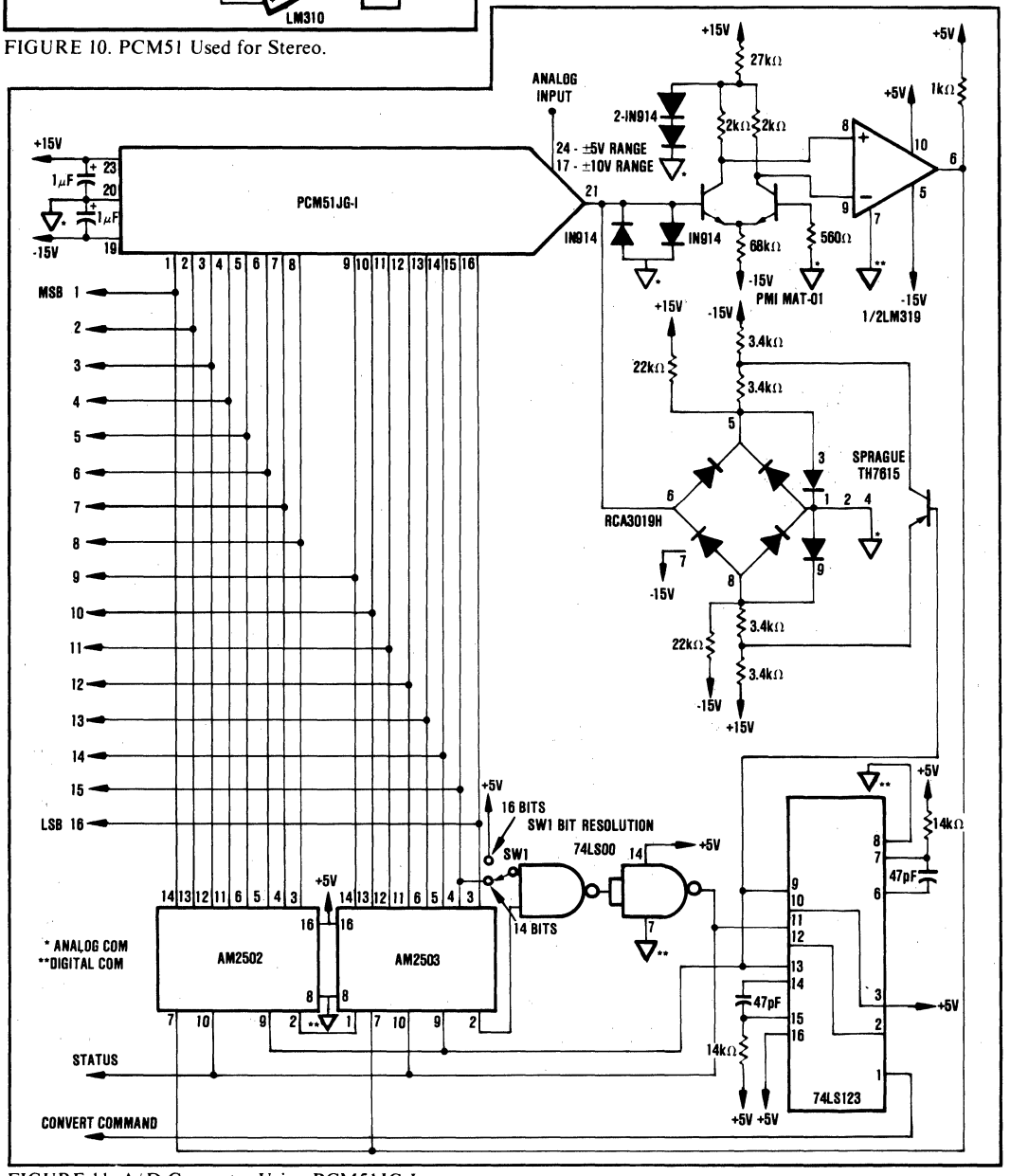


FIGURE 11. A/D Converter Using PCM51JG-I.

Table III shows the hex code loaded into the PROM's of the Distortion Test Circuit, Figure 3, for 14-bit values and Table IV shows the hex code for 16-bit values. Values are for a 400Hz sine wave (-15dB of full scale); all values are in volts.

TABLE III. Hex Code for 14-Bit Values (-15dB Output in 20V Full Scale Range).

CODE#	HEX CODE	IDEAL DAC OUT (Volts)	IDEAL SINE VALUE (Volts)	QUANTIZING ERROR (Volts)
1	7FFF	0.000000	0.000000	0.000000
2	7EB3	.101318	.101520	.000201
3	7D67	.202637	.202709	.000072
4	7C1F	.302734	.303236	.000502
5	7AD7	.402832	.402775	-.000057
6	7997	.500488	.500999	.000511
7	7857	.598145	.597590	-.000555
8	7723	.692139	.692231	.000092
9	75F3	.784912	.784614	-.000298
10	74CF	.874023	.874439	.000415
11	73AF	.961914	.961410	-.000504
12	729F	1.044922	1.045246	.000325
13	7197	1.125488	1.125673	.000185
14	709B	1.202393	1.202428	.000035
15	6FAB	1.275635	1.275261	-.000374
16	6ECB	1.343994	1.343934	-.000060
17	6DF7	1.408691	1.408223	-.000468
18	6D33	1.468506	1.467920	-.000586
19	6C7F	1.523438	1.522828	-.000610
20	6BDF	1.572266	1.572769	.000503
21	6B4B	1.617432	1.617580	.000148
22	6AC7	1.657715	1.657115	-.000600
23	6A5B	1.690674	1.691244	.000570
24	69FB	1.719971	1.719857	-.000113
25	69AF	1.743164	1.742861	-.000303
26	6977	1.760254	1.760179	-.000075
27	6953	1.771240	1.771756	.000516
28	693F	1.777344	1.777554	.000210
29	693F	1.777344	1.777554	.000210
30	6953	1.771240	1.771756	.000516
31	6977	1.760254	1.760179	-.000075
32	69AF	1.743164	1.742861	-.000303
33	69FB	1.719971	1.719857	-.000113
34	6A5B	1.690674	1.691244	.000570
35	6AC7	1.657715	1.657115	-.000600
36	6B4B	1.617432	1.617580	.000148
37	6BDF	1.572266	1.572769	.000503
38	6C7F	1.523438	1.522828	-.000610
39	6D33	1.468506	1.467920	-.000586
40	6DF7	1.408691	1.408223	-.000468
41	6ECB	1.343994	1.343934	-.000060
42	6FAB	1.275635	1.275261	-.000374
43	709B	1.202393	1.202428	.000035
44	7197	1.125488	1.125673	.000185
45	729F	1.044922	1.045246	.000325
46	73AF	.961914	.961410	-.000504
47	74CF	.874023	.874439	.000415
48	75F3	.784912	.784614	-.000298
49	7723	.692139	.692231	.000092
50	7857	.598145	.597590	-.000555
51	7997	.500488	.500999	.000511
52	7AD7	.402832	.402775	-.000057
53	7C1F	.302734	.303236	.000502
54	7D67	.202637	.202709	.000072
55	7EB3	.101318	.101520	.000201

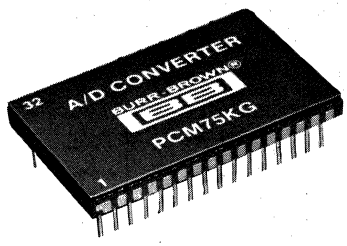
CODE#	HEX CODE	IDEAL DAC OUT (Volts)	IDEAL SINE VALUE (Volts)	QUANTIZING ERROR (Volts)
56	7FFF	0.000000	0.000000	0.000000
57	814B	-.101318	-.101520	-.000201
58	8297	-.202637	-.202709	-.000072
59	83DF	-.302734	-.303236	-.000502
60	8527	-.402832	-.402775	.000057
61	8667	-.500488	-.500999	-.000511
62	87A7	-.598145	-.597590	.000555
63	88DB	-.692139	-.692231	-.000092
64	8A0B	-.784912	-.784614	.000298
65	8B2F	-.874023	-.874439	-.000415
66	8C4F	-.961914	-.961410	.000504
67	8D5F	-1.044922	-1.045246	-.000325
68	8E67	-1.125488	-1.125673	-.000185
69	8F63	-1.202393	-1.202428	-.000035
70	9053	-1.275635	-1.275261	.000374
71	9133	-1.343994	-1.343934	.000060
72	9207	-1.408691	-1.408223	.000468
73	92CB	-1.468506	-1.467920	.000586
74	937F	-1.523438	-1.522828	.000610
75	941F	-1.572266	-1.572769	-.000503
76	94B3	-1.617432	-1.617580	-.000148
77	9537	-1.657715	-1.657115	.000600
78	95A3	-1.690674	-1.691244	-.000570
79	9603	-1.719971	-1.719857	.000113
80	964F	-1.743164	-1.742861	.000303
81	9687	-1.760254	-1.760179	.000075
82	96AB	-1.771240	-1.771756	-.000516
83	96BF	-1.777344	-1.777554	-.000210
84	96BF	-1.777344	-1.777554	-.000210
85	96AB	-1.771240	-1.771756	-.000516
86	9687	-1.760254	-1.760179	.000075
87	964F	-1.743164	-1.742861	.000303
88	9603	-1.719971	-1.719857	.000113
89	95A3	-1.690674	-1.691244	-.000570
90	9537	-1.657715	-1.657115	.000600
91	94B3	-1.617432	-1.617580	-.000148
92	941F	-1.572266	-1.572769	-.000503
93	937F	-1.523438	-1.522828	.000610
94	92CB	-1.468506	-1.467920	.000586
95	9207	-1.408691	-1.408223	.000468
96	9133	-1.343994	-1.343934	.000060
97	9053	-1.275635	-1.275261	.000374
98	8F63	-1.202393	-1.202428	-.000035
99	8E67	-1.125488	-1.125673	-.000185
100	8D5F	-1.044922	-1.045246	-.000325
101	8C4F	-.961914	-.961410	.000504
102	8B2F	-.874023	-.874439	-.000415
103	8A0B	-.784912	-.784614	.000298
104	88DB	-.692139	-.692231	-.000092
105	87A7	-.598145	-.597590	.000555
106	8667	-.500488	-.500999	-.000511
107	8527	-.402832	-.402775	.000057
108	83DF	-.302734	-.303236	-.000502
109	8297	-.202637	-.202709	-.000072
110	814B	-.101318	-.101520	-.000201

TABLE IV. Hex Code for 16-Bit Values (-15dB Output in 20V Full Scale Range).

CODE#	HEX CODE	IDEAL DAC OUT (Volts)	IDEAL SINE VALUE (Volts)	QUANTIZING ERROR (Volts)
1	7FFF	0.000000	0.000000	0.000000
2	7EB2	.101624	.101520	-.000104
3	7D67	.202637	.202709	.000072
4	7C1D	.303345	.303236	-.000109
5	7AD7	.402832	.402775	-.000057
6	7995	.501099	.500999	-.000099
7	7859	.597534	.597590	.000056
8	7723	.692139	.692231	.000092
9	75F4	.784607	.784614	.000007
10	74CE	.874329	.874439	.000110
11	73B1	.961304	.961410	.000107
12	729E	1.045227	1.045246	.000019
13	7196	1.125793	1.125673	-.000120
14	709B	1.202393	1.202428	.000035
15	6FAC	1.275330	1.275261	-.000069
16	6ECB	1.343994	1.343934	-.000060
17	6DF9	1.408081	1.408223	.000142
18	6D35	1.467896	1.467920	.000024
19	6C81	1.522827	1.522828	.000001
20	6BDD	1.572876	1.572769	-.000107
21	6B4B	1.617432	1.617580	.000148
22	6AC9	1.657104	1.657115	.000010
23	6A59	1.691284	1.691244	-.000040
24	69FB	1.719971	1.719857	-.000113
25	69B0	1.742859	1.742861	.000002
26	6977	1.760254	1.760179	-.000075
27	6951	1.771851	1.771756	-.000094
28	693E	1.777649	1.777554	-.000095
29	693E	1.777649	1.777554	-.000095
30	6951	1.771851	1.771756	-.000094
31	6977	1.760254	1.760179	-.000075
32	69B0	1.742859	1.742861	.000002
33	69FB	1.719971	1.719857	-.000113
34	6A59	1.691284	1.691244	-.000040
35	6AC9	1.657104	1.657115	.000010
36	6B4B	1.617432	1.617580	.000148
37	6BDD	1.572876	1.572769	-.000107
38	6C81	1.522827	1.522828	.000001
39	6D35	1.467896	1.467920	.000024
40	6DF9	1.408081	1.408223	.000142
41	6ECB	1.343994	1.343934	-.000060
42	6FAC	1.275330	1.275261	-.000069
43	709B	1.202393	1.202428	.000035
44	7196	1.125793	1.125673	-.000120
45	729E	1.045227	1.045246	.000019
46	73B1	.961304	.961410	.000107
47	74CE	.874329	.874439	.000110
48	75F4	.784607	.784614	.000007
49	7723	.692139	.692231	.000092
50	7859	.597534	.597590	.000056
51	7995	.501099	.500999	-.000099
52	7AD7	.402832	.402775	-.000057
53	7C1D	.303345	.303236	-.000109
54	7D67	.202637	.202709	.000072
55	7EB2	.101624	.101520	-.000104

CODE#	HEX CODE	IDEAL DAC OUT (Volts)	IDEAL SINE VALUE (Volts)	QUANTIZING ERROR (Volts)
56	7FFF	0.000000	0.000000	0.000000
57	814C	-.101624	-.101520	.000104
58	8297	-.202637	-.202709	-.000072
59	83E1	-.303345	-.303236	.000109
60	8527	-.402832	-.402775	.000057
61	8669	-.501099	-.500999	.000099
62	87A5	-.597534	-.597590	-.000056
63	88DB	-.692139	-.692231	-.000092
64	8A0A	-.784607	-.784614	-.000007
65	8B30	-.874329	-.874439	-.000110
66	8C4D	-.961304	-.961410	-.000107
67	8D60	-1.045227	-1.045246	-.000019
68	8E68	-1.125793	-1.125673	.000120
69	8F63	-1.202393	-1.202428	-.000035
70	9052	-1.275330	-1.275261	.000069
71	9133	-1.343994	-1.343934	.000060
72	9205	-1.408081	-1.408223	-.000142
73	92C9	-1.467896	-1.467920	-.000024
74	937D	-1.522827	-1.522828	-.000001
75	9421	-1.572876	-1.572769	.000107
76	94B3	-1.617432	-1.617580	-.000148
77	9535	-1.657104	-1.657115	-.000010
78	95A5	-1.691284	-1.691244	.000040
79	9603	-1.719971	-1.719857	.000113
80	964E	-1.742859	-1.742861	-.000002
81	9687	-1.760254	-1.760179	.000075
82	96AD	-1.771851	-1.771756	.000094
83	96C0	-1.777649	-1.777554	.000095
84	96C0	-1.777649	-1.777554	.000095
85	96AD	-1.771851	-1.771756	.000094
86	9687	-1.760254	-1.760179	.000075
87	964E	-1.742859	-1.742861	-.000002
88	9603	-1.719971	-1.719857	.000113
89	95A5	-1.691284	-1.691244	.000040
90	9535	-1.657104	-1.657115	-.000010
91	94B3	-1.617432	-1.617580	-.000148
92	9421	-1.572876	-1.572769	.000107
93	937D	-1.522827	-1.522828	-.000001
94	92C9	-1.467896	-1.467920	-.000024
95	9205	-1.408081	-1.408223	-.000142
96	9133	-1.343994	-1.343934	.000060
97	9052	-1.275330	-1.275261	.000069
98	8F63	-1.202393	-1.202428	-.000035
99	8E68	-1.125793	-1.125673	.000120
100	8D60	-1.045227	-1.045246	-.000019
101	8C4D	-.961304	-.961410	-.000107
102	8B30	-.874329	-.874439	-.000110
103	8A0A	-.784607	-.784614	-.000007
104	88DB	-.692139	-.692231	-.000092
105	87A5	-.597534	-.597590	-.000056
106	8669	-.501099	-.500999	.000099
107	8527	-.402832	-.402775	.000057
108	83E1	-.303345	-.303236	.000109
109	8297	-.202637	-.202709	-.000072
110	814C	-.101624	-.101520	.000104

BURR-BROWN®



PCM75
DESIGNED FOR AUDIO

ADVANCE INFORMATION
Subject to Change

16-Bit Hybrid ANALOG-TO-DIGITAL CONVERTER

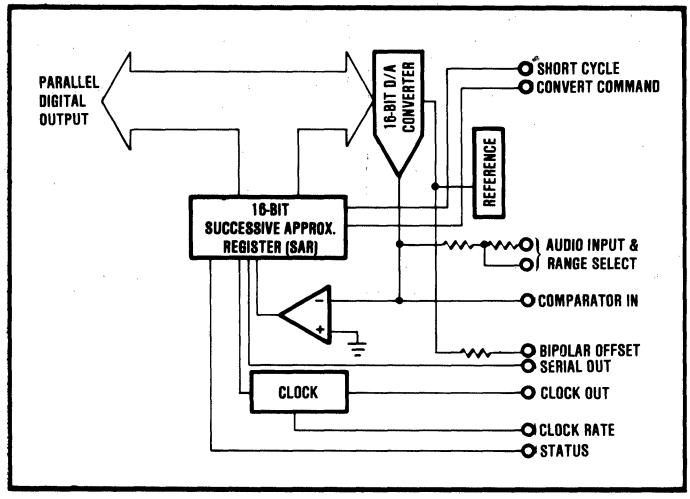
FEATURES

- 16-BIT RESOLUTION
- 90dB DYNAMIC RANGE
- 0.004% THD (FS Input, 16 Bits)
- 0.02% MAX THD (-15dB, 16 Bits)
- 17μsec MAX CONVERSION TIME (16 Bits)
- 15μsec MAX CONVERSION TIME (14 Bits)
- 8μsec CONVERSION (Reduced Specs)
- EIAJ STC-007-COMPATIBLE
- INTERNAL 16-BIT DAC AVAILABLE TO USER

DESCRIPTION

The PCM75 is designed for PCM Audio applications and is compatible with EIAJ STC-007 specifications. The internal 16-bit digital-to-analog converter is available for the designer to utilize in the playback mode, thus saving the cost of an additional DAC. The conversion time can be reduced from 15μsec to 8μsec with some increase in distortion. Distortion is specified on the data sheet to assure performance in critical audio applications.

The PCM75 is a low cost, high quality, 16-bit successive approximation analog-to-digital converter. The PCM75 uses state-of-the-art IC and laser-trimmed thin-film components and is packaged in a bottom-brazed ceramic 32-pin dual-in-line package. The converter is complete with internal reference and clock.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-441

SPECIFICATIONS

ELECTRICAL

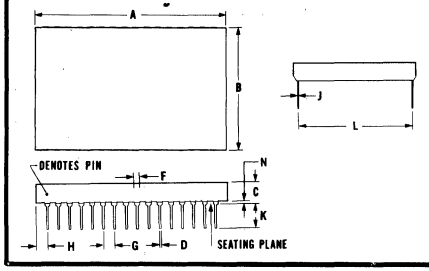
At 25°C and rated power supplies unless otherwise noted.

MODEL	PCM75KG			PCM75JG			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
DYNAMIC RANGE(1)		90			90		dB
INPUT							
ANALOG							
Voltage Ranges, Bipolar		±2.5, ±5, ±10			±2.5, ±5, ±10		V
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			2.5		kΩ
0 to +10V, ±5V		5			5		kΩ
0 to +20V, ±10V		10			10		kΩ
DIGITAL(2)							
Convert Command	Positive pulse 50nsec wide (min) trailing edge ("1" to "0" initiates conversion)						
Logic Loading			1			1	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error		±0.1(3)			±0.1(3)		%
Offset Error, Bipolar		±0.1(3)			±0.1(3)		% of FSR(4)
Differential Linearity Error (major carry)		±0.0015			±0.003		% of FSR
Inherent Quantization Error		±1/2			±1/2		LSB
TOTAL HARMONIC DISTORTION (THD)(1)							
V_{IN} = ±FS at f = 400Hz							
14-Bit Resolution		0.006			0.008		%
16-Bit Resolution		0.004			0.006		%
V_{IN} = -15dB at f = 400Hz							
14-Bit Resolution		0.025			0.03	0.05	%
16-Bit Resolution		0.015	0.02		0.021		%
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			0.003		% of FSR/%V_S
+5VDC		0.001			0.001		% of FSR/%V_S
CONVERSION TIME(5) (14 Bits)			15			15	µsec
(16 Bits)			17				µsec
WARM-UP TIME	5			5			min
DRIFT							
Gain			±20			±20	ppm/°C
Offset, Bipolar			±15			±15	ppm of FSR/°C
OUTPUT							
DIGITAL							
(All codes complementary)							
Parallel							
Output Codes(6)							
Bipolar		COB, CTC(7)			COB, CTC(7)		
Output Drive	2			2			TTL Loads
Serial Data Code (NRZ)		CSB, COB			CSB, COB		
Output Drive	2			2			TTL Loads
Status	Logic "1" during conversion			Logic "1" during conversion			
Status Output Drive	2			2			TTL Loads
Internal Clock							
Clock Output Drive	2			2			TTL Loads
Frequency(8)		933			933		kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		1.55			1.55		W
Rated Voltage, Analog	±14.5	±15	±15.5	±14.5	±15	±15.5	VDC
Rated Voltage, Digital	+4.75	+5	+5.25	+4.75	+5	+5.25	VDC
Supply Drain +15VDC		+45			+45		mA
Supply Drain -15VDC		-35			-35		mA
Supply Drain +5VDC		+70			+70		mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (derated specs)	-25		+85	-25		+85	°C
Storage	-55		+100	-55		+100	°C

NOTES:

1. The measurement of total harmonic distortion (THD) and Dynamic Range is highly dependent on the characteristics of the sample/hold amplifier, the digital-to-analog converter, the deglitcher, and the low-pass filter. To accurately measure THD and Dynamic Range, the accuracy of each device should be better than 16-bit accuracy. A block diagram showing the measurement technique Burr-Brown uses is shown in Figure 4.
2. DTL/TTL compatible, i.e., Logic "0" = 0.8V max. Logic "1" = 2.0V min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.
3. Adjustable to zero. (See "Optional External Gain and Offset Adjustment.")
4. FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR.
5. Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Additional Optional Connections" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified max conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to bit 15 (pin 15) for 14-bit resolution.
6. See Table I. CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Two's Complement.
7. CTC coding obtained by inverting MSB (pin 1).
8. Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz. See Figures 12 and 13 and Table III.

MECHANICAL



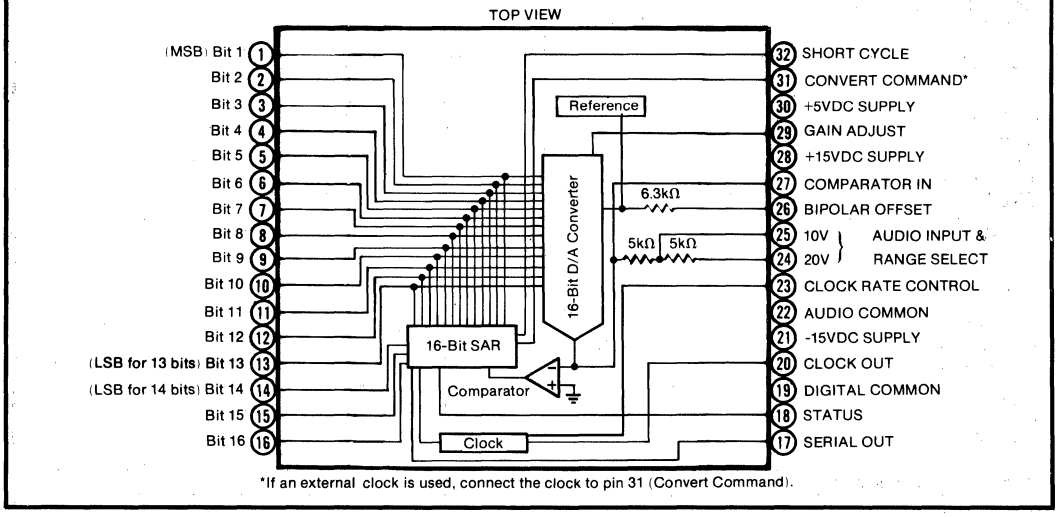
Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Ceramic
MATING CONNECTOR:
2302MC
WEIGHT: 13 grams (0.46oz.)
HERMETICITY:
Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.678	1.712	42.62	43.48
B	1.079	1.101	27.41	27.97
C	.180	.210	4.57	5.33
D	.016	.020	.41	.51
F	.045	.055	1.14	1.40
G	.100 BASIC		2.54 BASIC	
H	.089	.106	2.26	2.69
J	.009	.012	.23	.30
K	.200	.210	5.08	5.33
L	.900 BASIC		22.86 BASIC	
N	.015	.035	.38	.89

LEADS IN TRUE POSITION WITHIN .010" (.25 MM) R @ MMC AT SEATING PLANE

CONNECTION DIAGRAM



*If an external clock is used, connect the clock to pin 31 (Convert Command).

THEORY OF OPERATION

The accuracy of a successive-approximation A/D converter is described by the transfer function shown in Figure 1. All successive-approximation A/D converters have an inherent Quantization Error ±1/2LSB. The remaining errors in the A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits Off), and Offset drift shifts the line left or right over the operating temperature range. Total Harmonic Distortion (THD) is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error, that is useful in Audio Applications. To be useful, THD should be specified for both high level and low level input

signals. This error is unadjustable and is the most meaningful indicator of A/D converter accuracy for Audio Applications. The resolution of an A/D converter can be expressed in terms of Dynamic Range. The Dynamic Range is a measure of the ratio of the smallest signals the converter can resolve to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution, or 96dB for a 16-bit converter. The actual or useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.

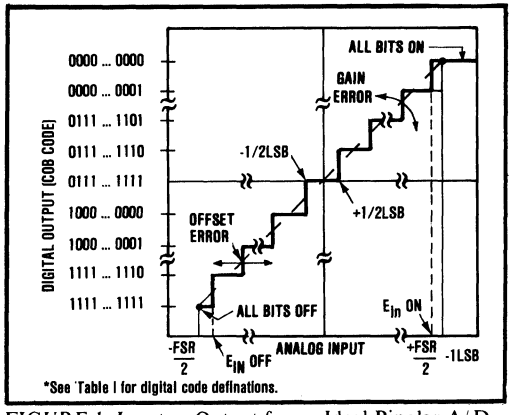


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exits. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output).

DEFINITION OF DIGITAL CODES

Parallel Data

Two binary codes are available on the PCM75 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary offset binary (COB) for bipolar input signal ranges. Complementary two's complement (CTC) may be obtained by inverting MSB (pin1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 14-, 15-, and 16-bit resolutions. Figure 3 shows the connections for 14-bit resolution, parallel data output, with ±5V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line; they are CSB and COB. The serial data is available only during conversion and appears with the MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

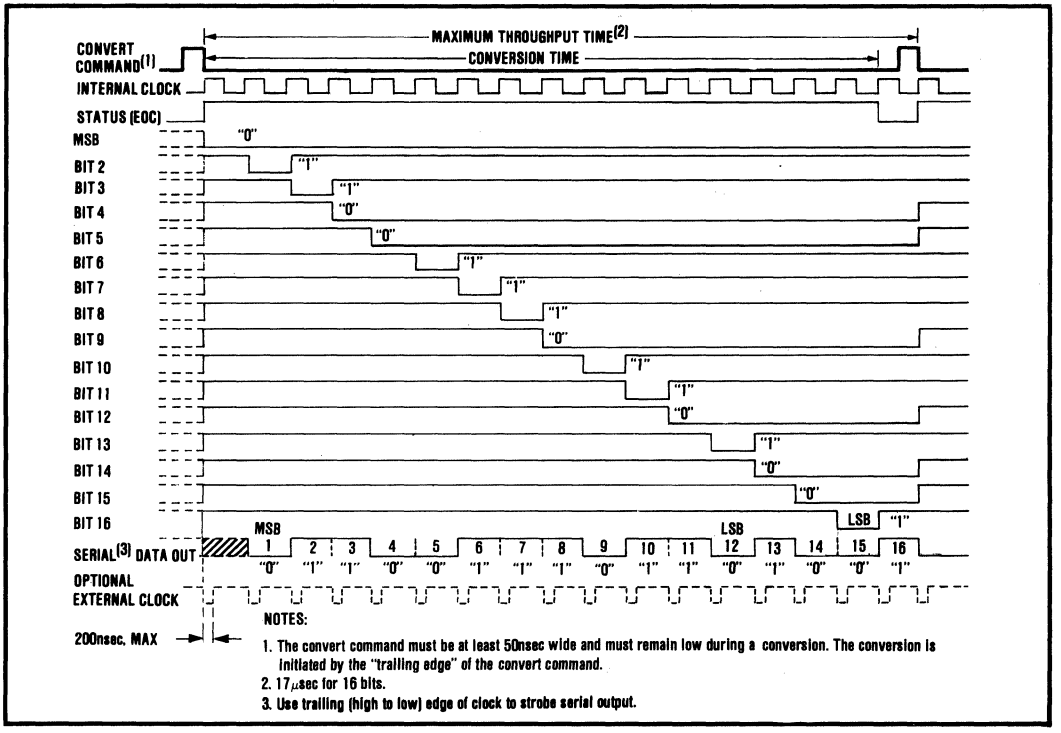


FIGURE 2. Timing Diagram.

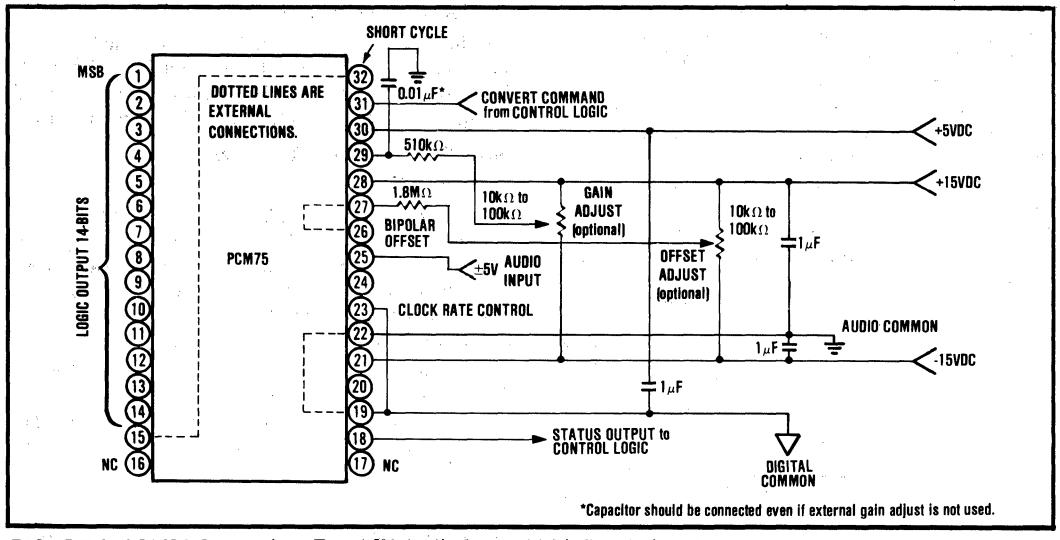


FIGURE 3. PCM75 Connections For: ±5V Audio Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES						
Audio Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 16	305μV	153μV	77μV	153μV	77μV	305μV
	n = 15	610μV	305μV	153μV	305μV	153μV	610μV
	n = 14	1.22mV	610μV	305μV	6.0μV	305μV	1.22mV
Transition Values							
MSB LSB							
000...000(4)	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB	+20V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111...110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

(1) COB = Complementary Offset Binary
(2) CTC = Complementary Two's Complement - obtained by inverting the most significant bit, MSB (pin 1).
(3) CSB = Complementary Straight Binary
(4) Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The PCM75 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter in audio applications are total harmonic distortion, drift, gain and offset errors, and conversion time effects on accuracy. The ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory trimmed to typically ±0.1% of FSR (typically ±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10 and 11.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM75 power supply sensitivity is specified for ±0.003% of FSR/%V, for ±15VDC supplies and ±0.0015% of FSR/%V, for +5VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics to the value of the rms fundamental and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM75 is shown in Figure 4 along with a timing diagram for the control logic. If we assume that the error due to the test circuit is negligible, then the rms value of

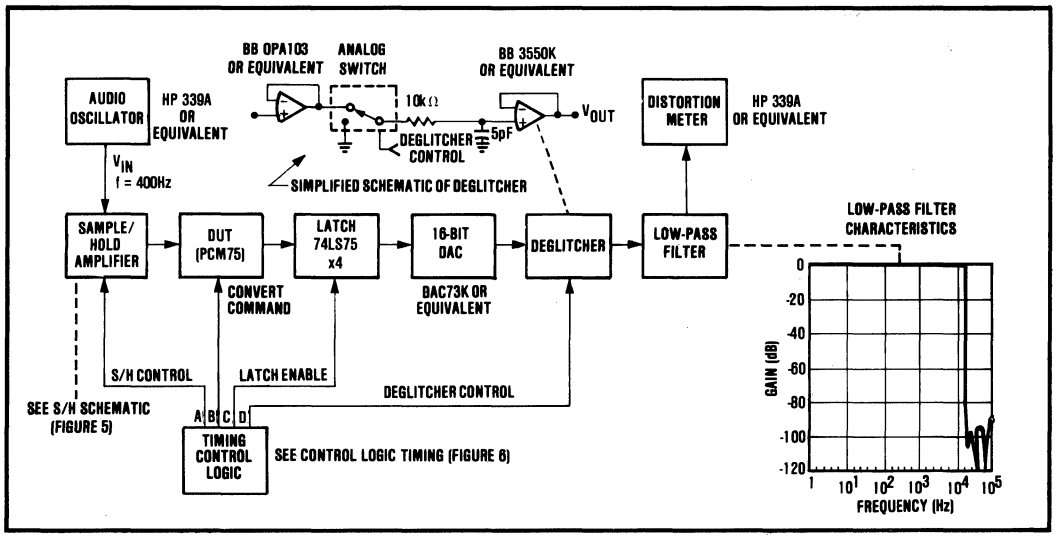


FIGURE 4. Block Diagram of Distortion Test Circuit.

the PCM75 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2}$$

where N is the number of samples, $E_L(i)$ is the linearity error of the PCM75 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\%$$

This expression indicates that there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the A/D is directly correlated to the THD because the digital output words from the A/D vary according to the amplitude and frequency of the sine wave input as well as the sampling frequency.

For the PCM75 the test sampling period was chosen to be 22.7μsec which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 400Hz and the amplitude of the input signal is 0dB (full scale) and -15dB.

ACCURACY VS CONVERSION TIME

Figures 14 and 15 show the relationship of THD vs input voltage level for the PCM75 with both 14-bit and 16-bit resolution and conversion times of 8μsec and 15μsec. Notice that the distortion level is reduced by increasing the resolution from 14 to 16 bits due to the reduced quantization error. Conversely, decreasing the conversion time of the PCM75 from 15μsec to 8μsec increases the distortion level due to dynamic linearity errors resulting from insufficient settling time for the internal D/A converter and comparator.

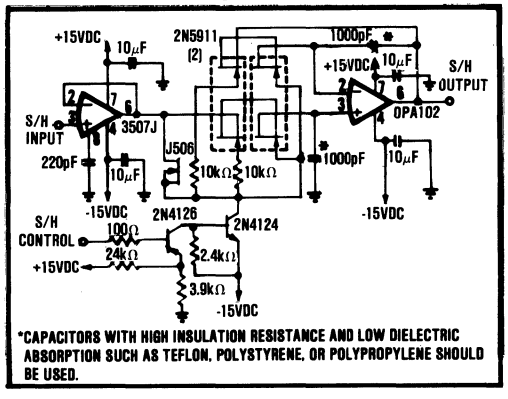


FIGURE 5. Schematic of Sample/Hold Amplifier.

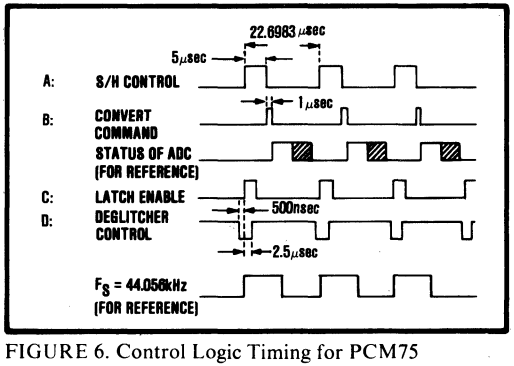


FIGURE 6. Control Logic Timing for PCM75 Distortion Test Circuit.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and Digital Common are not connected internally in the PCM75 but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC. Bypass the 1μF electrolytic type capacitors with 0.01μF ceramic capacitors for improved high frequency performance.

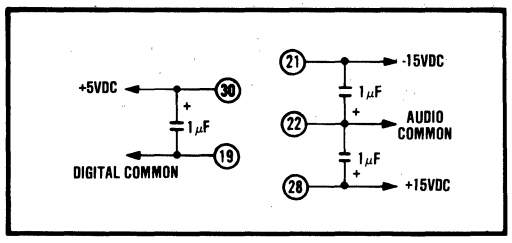


FIGURE 7. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

TABLE II. PCM75 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (pin 1).

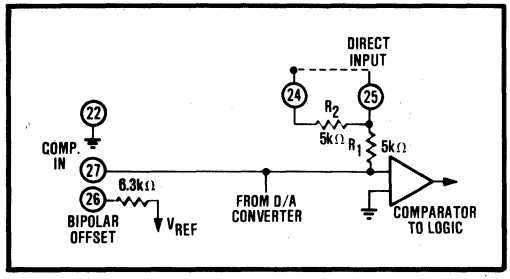


FIGURE 8. PCM75 Input Scaling Circuit.

INPUT IMPEDANCE

The input signal to the PCM75 should come from a low impedance source, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the PCM75.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the PCM75 as shown in Figure 9.

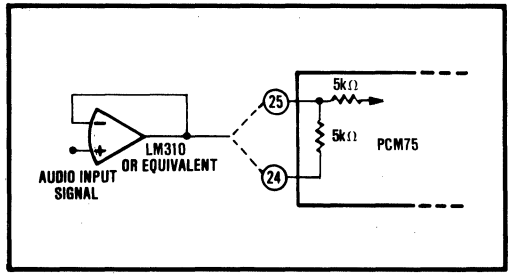


FIGURE 9. Buffer Amplifier for PCM75 Input.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 10 and 11. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 10. Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN}^{OFF}).

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

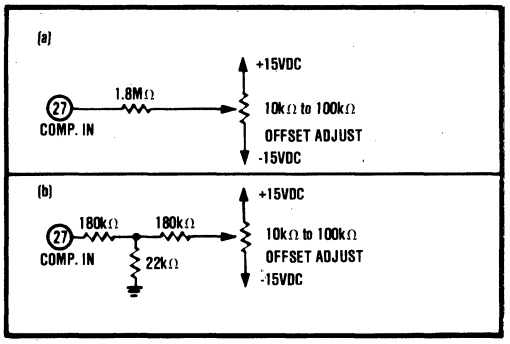


FIGURE 10. Two Methods of Connecting Optional Offset Adjust With a 0.4% of FSR Range of Adjustment.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 11. Sweep the input through the end point transition voltage that should cause an output transition to all bits on (E_{IN}^{ON}). Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}. Table I details the transition voltage levels required.

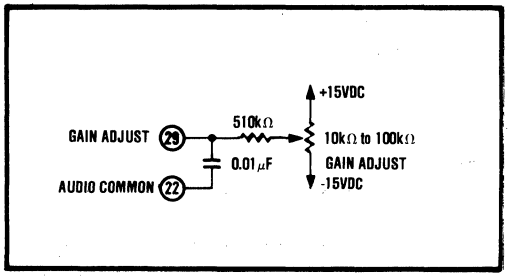


FIGURE 11. Connecting Optional Gain Adjust With a 0.6% Range of Adjustment.

OUTPUT DRIVE

Normally all PCM75 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

ADDITIONAL OPTIONAL CONNECTIONS

The PCM75 may be operated with faster conversion times for resolutions less than 14 bits, if a higher THD is acceptable, by connecting the Clock Rate (pin 23) and the Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

TABLE III. Short Cycle and Clock Rate Control Connections for 12- to 16-Bit Resolutions.

Resolution (Bits)	16	15	14	13	12
Connect Pin 32* to	Open	Pin 16	Pin 15	Pin 14	Pin 13
Connect Pin 23 to	Pin 19	Pin 19	Pin 19	Pin 30	Pin 30
Conversion Time (Typical) μsec	17	16	15	10	8

*For resolutions less than 16 bits also connect a 2kΩ resistor from +5V to pin 32.

If a more precise adjustment of conversion time is desired than can be obtained by simply connecting the Clock Rate (pin 23) to Digital Common or +5V, as indicated in Table III, the Clock Rate pin may be connected to an external multiturn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figure 12. The typical conversion time vs the Clock Rate Control voltage is shown in Figure 13. The effect of varying the conversion time and the resolution on the total harmonic distortion is shown in Figures 14 and 15.

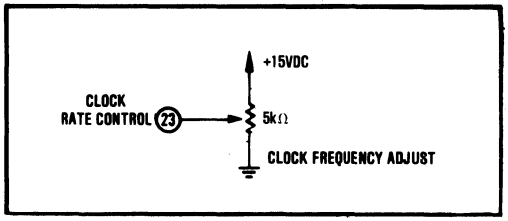


FIGURE 12. Clock Rate Control, Optional Fine Adjust.

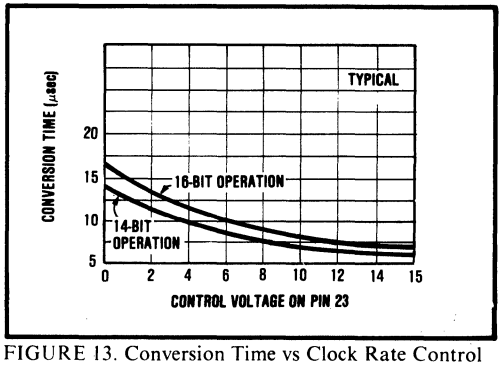


FIGURE 13. Conversion Time vs Clock Rate Control Voltage.

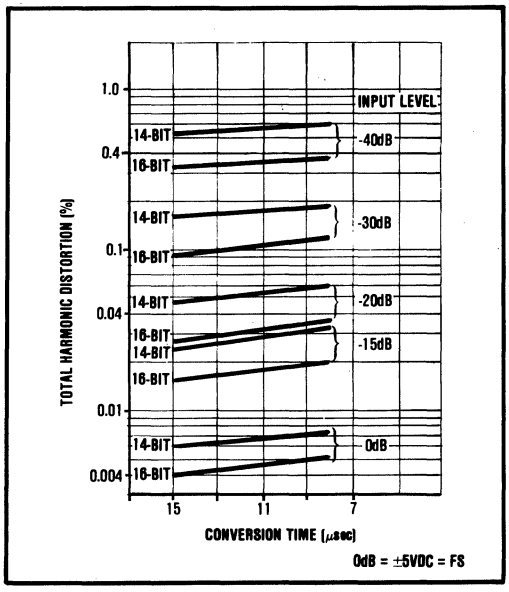


FIGURE 14. Total Harmonic Distortion vs Conversion Time.

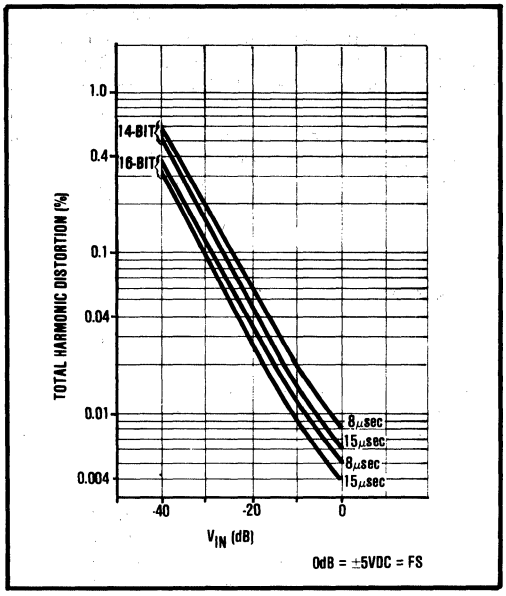


FIGURE 15. Total Harmonic Distortion vs Input Voltage Level.

EXTERNAL CLOCK

If an external clock is used, connect it to the Convert Command, pin 31. The convert command waveform as shown in Figure 2 is then not used on pin 31. The internal clock signal will still appear on pin 20 and its waveform can vary from that shown in Figure 2. The external clock pulse, as applied to pin 31, must be a negative-going pulse with a width between 100nsec and 200nsec as shown in Figure 2 and in Figures 16, 17, and 18.

Figure 16 shows continuous conversion using an external clock waveform, with the correct duty cycle applied directly to pin 31. A new conversion will automatically be initiated by the (n + 2) clock pulse where n is the resolution of the PCM75.

Figure 17 shows how to shape the waveform to apply to pin 31 when using an external clock that has an arbitrary duty cycle.

Figure 18 shows how to obtain continuous external clock conversion initiated by the rising edge of an external clock pulse only when an additional convert command pulse is high.

In all cases when using an external clock, the frequency of the external clock must be lower than the frequency of the internal clock. The internal clock normally runs at 933kHz when the Clock Rate Control, pin 23, is connected to digital common. Higher internal clock frequencies can be obtained by connecting the Clock Rate Control, pin 23, to positive voltages; +5V is often convenient to use. See Figure 13 for relative increases.

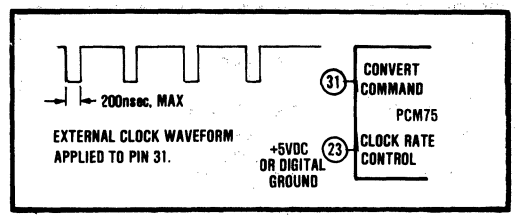


FIGURE 16. Continuous Conversion Using an External Clock.

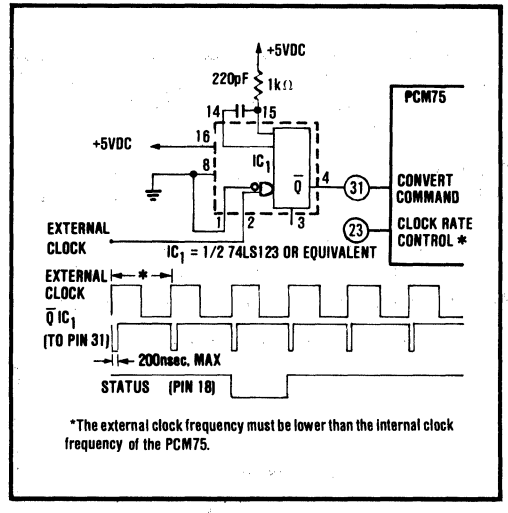


FIGURE 17. Continuous Conversion Using an External Clock That Has an Arbitrary Duty Cycle.

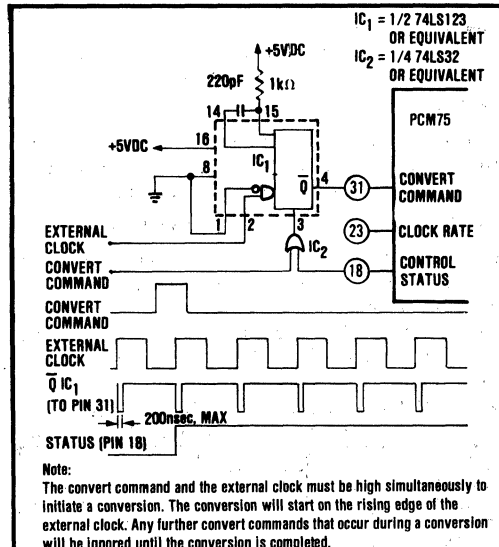


FIGURE 18. Continuous Conversion Initiated by the Rising Edge of an External Clock Pulse, Only When an Additional Convert Command Signal is High.

DESCRIPTION OF A/D - D/A OPERATION

The PCM75 was designed so that the internal D/A converter can be made available to the user as shown in Figure 19. The D/A converter portion of the PCM75 requires only ±15VDC supplies and analog common for operation. Therefore, floating the +5VDC supply pin (pin 30) turns off the internal clock, successive approximation register (SAR), and comparator without affecting the operation of the DAC. Note that the +5VDC line must appear as a high impedance to the PCM75 or damage may result to the SAR digital outputs when they are used as digital inputs for operation of the D/A converter.

This circuit provides a low cost alternative to using a separate A/D and D/A converter in applications where the operation of only one device is required at any given time. The current settling time of the D/A portion of the PCM75 is about 1μsec to within ±0.003% of the final value. The voltage settling time is dependent upon the characteristics of the output amplifier (A_1).

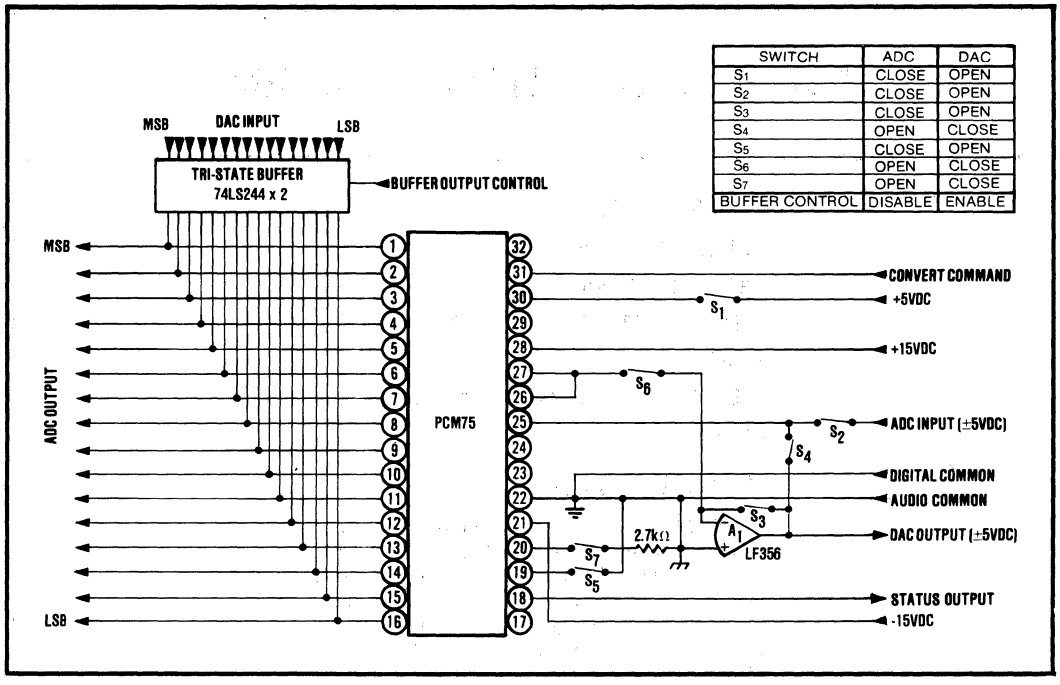


FIGURE 19. PCM75 Used Both as an A/D Converter and as a D/A Converter.

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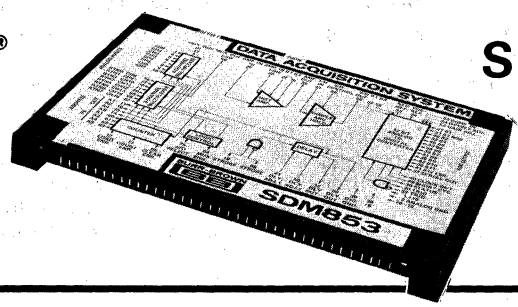


SDM853

DATA ACQUISITION SYSTEM

FEATURES

- SAVES DESIGN TIME
- RELIABLE - 168-hour bake
- LOW LEVEL OR HIGH LEVEL INPUTS
- SAVES SPACE
- FLEXIBLE - Up to four modes of operation
- LOW COST

DESCRIPTION

The SDM853 is a complete 8- or 16-channel data acquisition system in a compact 4.6" x 3.0" x 0.375" metal case. This system differs from most in that it can acquire and digitize low level or high level analog signals. A built-in high quality instrumentation amplifier allows input signal ranges of ±10mV to ±10V. This means that the SDM853 can be connected to low level sensors such as thermocouples and strain gauges without external signal conditioning.

This expandable module accepts either 16 single-ended or 8 differential inputs and converts the multiplexed data signals into 12-bit digial words with an accuracy of ±0.025% at throughput rates of up to 33,000 samples per second.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-354A

DISCUSSION OF PERFORMANCE

The SDM853 is a complete modular "off the shelf" data acquisition system. With this system it is possible to configure complete data acquisition systems in one-fourth the space for a fraction of the cost previously possible.

These systems contain all the components necessary to multiplex and convert ±10mV to ±10V analog data into equivalent digital outputs yielding resolutions of 2.4μV to 2.4mV. The minimum throughput sampling rates are up to 30 kHz for 12 bit and up to 43 kHz for 8 bit resolution. The model SDM853 contains an analog multiplexer which can be connected in a 16 channel single ended or 8 channel differential mode, instrumentation amplifier, sample/hold, 12 bit successive approximation A/D converter and programming logic. The amplifier and sample/hold are not internally interconnected. This allows maximum application flexibility. These systems can be expanded without limit using Burr-Brown's MPC-16S and MPC-8D monolithic multiplexers. Figure 1 shows the components of the SDM853. The system is designed to be mounted on a printed circuit card. The only requirement for system operation are input signals, power and the interconnection of the system components into the desired operating configuration.

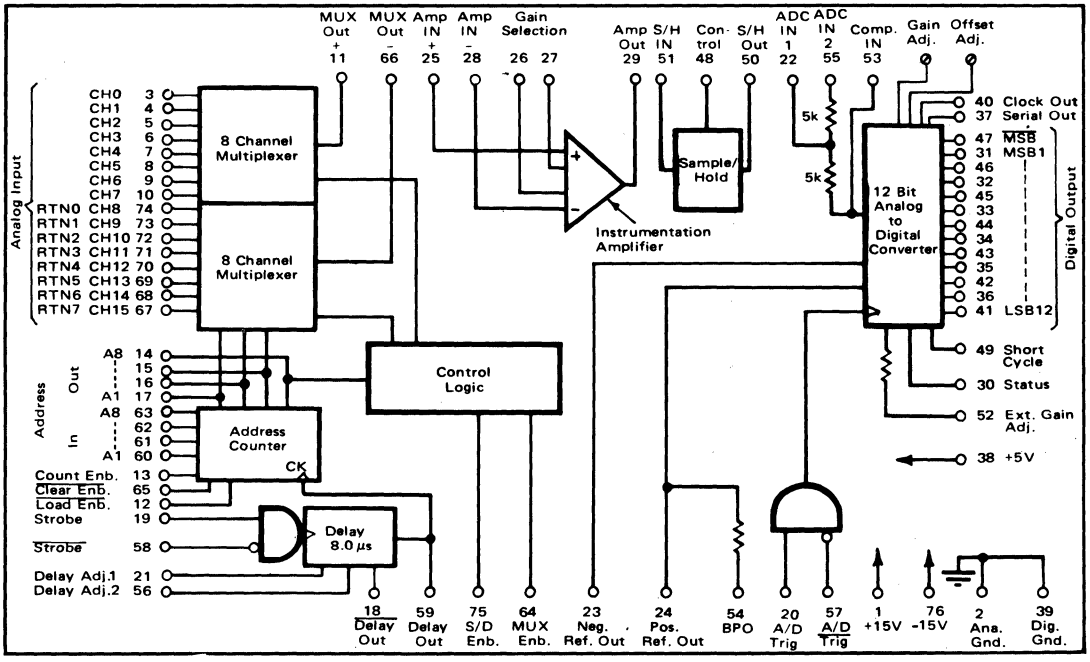


FIGURE 1. SDM853 Block Diagram.

ANALOG MULTIPLEXER

Two one of eight CMOS analog multiplexers are used to allow user selection by external jumpers of 16 single ended channel or 8 double ended channel operation. In 16 channel operation the multiplexer may be used in a pseudo differential mode by connecting the amplifier inverting input to a common, remote, signal ground. Channel selection is by a 3 or 4 bit binary word stored in a presettable address counter. Channel capacity is expandable without limit.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity, and external gain programming with an external resistor. With the gain programming pins open, the gain is unity. Gain may be selected from unity to 60 dB.

SAMPLE AND HOLD AMPLIFIERS

The sample and hold amplifier is a complete, stand alone, sample and hold circuit featuring buffered output, 7μsec acquisition time, and 30nsec aperture time. Input, output and mode control functions are brought to separate connector pins. This allows maximum system flexability for performing such functions as automatic gain ranging with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a ceramic packaged, 12-bit converter featuring 24μsec conversion time and 0.01% accuracy. Thin-film networks and current switching are used to assure linearity over wide temperature ranges.

ADDRESS COUNTER

A 4-bit binary address counter is connected to the multiplexer. This counter may be externally loaded, cleared, clocked or enabled. The address outputs are brought to connector pins for convenient system control.

DELAY TIMER

The delay timer is provided to allow for the settling time of the multiplexer, amplifier, and sample and hold circuits. The delay time is adjustable over a wide range by an external potentiometer and/or external capacitor. This allows for the longer settling time of the instrument amplifier at high gains.

CONTROL LOGIC

Delay and ADC trigger functions are edge-triggered and gated. Counter control functions are synchronous with the counter clock which is internally connected to the delay timer output.

CHANNEL EXPANSION

The number of analog input channels of these systems can easily be increased using Burr-Brown's MPC8D and MPC16S CMOS multiplexers. the MPC8D is an 8-channel differential model and the MPC16S is a 16-channel single-ended model. These are latch-free devices which contain internal binary decoding, TTL or MOS logic levels, and may be integrated into a system with minimum external logic.

SYSTEM PERFORMANCE

The SDM853 can be configured to continuously sequence through all analog channels, to accept random addresses or to sequence through all analog channels on command from an external trigger.

The status signal, pin 30, is connected to the strobe not input of the delay timer, pin 58, for normal program sequencing with a minimum throughput sampling rate of 30kHz for 12-bit resolution.

By using "overlap" programming, the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 32kHz for 12-bit and 43kHz to 8-bit resolution. This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting the status signal, pin 30, to the strobe input of the delay timer, pin 19, and extending the delay time. The internal logic will then select analog channel (n + 1) while channel n is being converted.

SYSTEM PERFORMANCE

(Typical at 25°C and rated supplies)

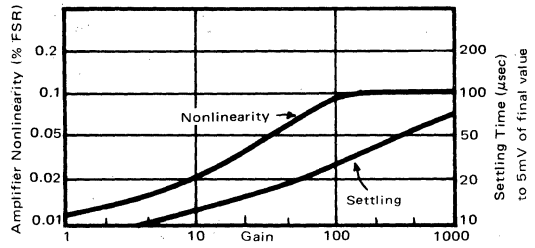


FIGURE 2. Nonlinearity and Settling Time vs. Amplifier Gain.

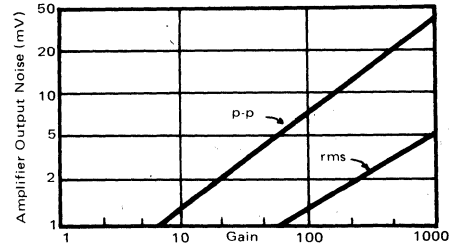


FIGURE 3. Output Noise vs. Amplifier Gain.

System Gain	System Accuracy	Throughput Rate (Channels/sec)		Delay Time (μsec)	
V/V		Normal	Overlap	Normal	Overlap
1	±0.025% FSR	30k	32k	9	31
10	±0.035% FSR	25k	32k	18	
100	±0.08% FSR	20k	32k	25	31
1000	±0.1% FSR	10k	14k	70	70

TABLE I. Throughput Rate vs. Gain for Normal and Overlap Modes.

FSR	ADC Range	Amplifier Gain	Resolution	Delay for Settling to ±0.2% (μsec)	Delay for Settling to ±0.05% (μsec)	Delay for Settling to 0.01% (μsec)
20V	±10V	1	4.88mV	7	8	9
1V	0 to 10V	10	244μV	10	15	18
0.1V	0 to 10V	100	24.4μV	20	25	30
10mV	0 to 10V	1000	2.44μV*	60	70	-

TABLE II. This table shows the delay timer setting required to allow for the settling time of the instrumentation amplifier to the accuracies specified. Add the 24μsec conversion time of the A/D converter to the above delay times to obtain channel conversion times. * Depends on desired S/N ratio.

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	SDM853
TRANSFER CHARACTERISTICS	
Throughput Rate, min	30kHz, 33μsec/channel
Resolution	12 Bits
Number of Channels	16 single-ended/8 differential
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	1 to 1000
Amplifier gain equation	$G = 1 + 20k\Omega/R_{EXT}$ [1]
Max. input voltage without damage	±16V
Max. input voltage for multiplexer operation [6]	±10.24V
Input impedance	100MΩ, 10pF OFF channel 100MΩ, 100pF ON channel
Bias current	
25°C	20nA
0°C to 70°C	50nA
Differential Bias Current (25°C)	10nA
Differential Bias Current Drift	0.1nA/°C
Amplifier output noise (Gain = 100, R_s = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage, max	400μV
Amplifier voltage offset drift	2 + 20/GμV/°C
ACCURACY [2]	
System RSS accuracy at 25°C (Gain = 1)	±0.025% FSR [3] at 30kHz throughput
Linearity (Gain = 1)	±1/2LSB, at 30kHz throughput
Differential linearity (Gain = 1)	±1/2LSB, at 30kHz throughput
Quantizing error	±1/2LSB
Gain error	Adjustable to zero
Offset error	Adjustable to zero
Power supply sensitivity	±0.005% FSR/% change of supply voltage
STABILITY OVER TEMPERATURE	
System accuracy drift, max	±30ppm/°C of reading
Linearity drift	±3ppm of FSR/°C
DYNAMIC ACCURACY	
Sample & Hold aperture time	30nsec
Aperture time uncertainty	±5nsec
Error for full scale transition between successively addressed channels	1LSB at 30kHz
Differential amplifier CMRR (Gain = 1)	74dB at 1kHz 65dB at 3kHz (100dB at 60Hz Gain = 1000)
Channel cross talk	80dB down at 2kHz, for OFF channel to ON channel
Sample & Hold feedthrough	80dB down at 5kHz
Sample & Hold decay rate	10μVμsec
OUTPUT	
Output Coding (Complementary)	Unipolar Straight Binary, Bipolar Offset, Binary Two's Complement
Gain trim [4]	Adjustable to zero error
Offset trim [4]	Adjustable to zero error
A/D Conversion Time	24μsec
Delay	9μsec nominal, externally adjustable from 5.5μsec to 14μsec [5]
POWER REQUIREMENTS	±15VDC ±3% at +50mA, 5mV, rms, ripple -15VDC ±3% at -75mA, 5mV, rms, ripple +5VDC ±5% at +300mA, 25mV, rms, ripple
ENVIRONMENTAL	
Operating temperature	0°C to 70°C
Storage temperature	-25°C to +85°C
Relative humidity	95% noncondensing

1. With R_{EXT} between pins 26 and 27.
2. No missing codes guaranteed.
3. FSR means Full Scale Range.
4. Gain and Offset controls are located in the module. The adjustment ranges are ±0.1% FSR for Gain and ±0.1% FSR for Offset.
5. Adjustable to 10 seconds with external capacitor.
6. For differential operation with gain > 1, the common-mode input voltage range is ±5V.

DIGITAL INPUT SPECIFICATIONS

Address inputs	One standard TTL load, positive true
Coding	4-bit binary
Load Enable	One standard TTL load, negative true, address loaded with strobe inputs.
Clear Enable	One standard TTL load, negative true, address loaded with strobe inputs.
Strobe & Strobe	One standard TTL load, STROBE and $\overline{\text{STROBE}}$ edge trigger the delay timer and clock the address counter. STROBE must be high to enable $\overline{\text{STROBE}}$ and $\overline{\text{STROBE}}$ must be low to enable STROBE.
Count Enable	Two standard TTL loads, positive true, logic "0" allows the Strobe inputs to trigger the delay timer, but prevents the MUX address counter from being clocked.
ADC trigger	One standard TTL load, a positive going edge at TRIG initiates conversion, a negative going edge at $\overline{\text{TRIG}}$ initiates conversion; $\overline{\text{TRIG}}$ must be "0" to enable TRIG; TRIG must be "1" to enable $\overline{\text{TRIG}}$.
Short cycle	One standard TTL load, logical 1 for 12-bit resolution, connected to the N + 1 bit output for N bit resolution.
Multiplexer Enable	
Multiplexer Enable	Two standard TTL loads, logical 1 enable multiplexer output and logical 0 turns off all channels.
S/D select	Two standard TTL loads, logical 1 enables 16-channel single-ended operation and logical 0 enable 8-channel differential operation.

DIGITAL OUTPUT SPECIFICATIONS

Data outputs	
Parallel B1, B1 . . . B12	2 Standard TTL loads, negative true.
Serial out	2 Standard TTL loads, negative true, time serial data output beginning with B1, (see timing diagram).
Address outputs	5 Standard TTL loads, positive true, 4-bit binary code, internal 2kΩ pull-up resistors.
Delay out (Delay Out)	5 Standard TTL loads high (low) during the delay period, triggered by $\overline{\text{Strobe}}$ and Strobe inputs.
Clock	5 Standard TTL loads for synchronizing serial out data (see timing diagram).
Status	5 Standard TTL loads, high during the A. D converison.

SYSTEM TIMING DIAGRAMS

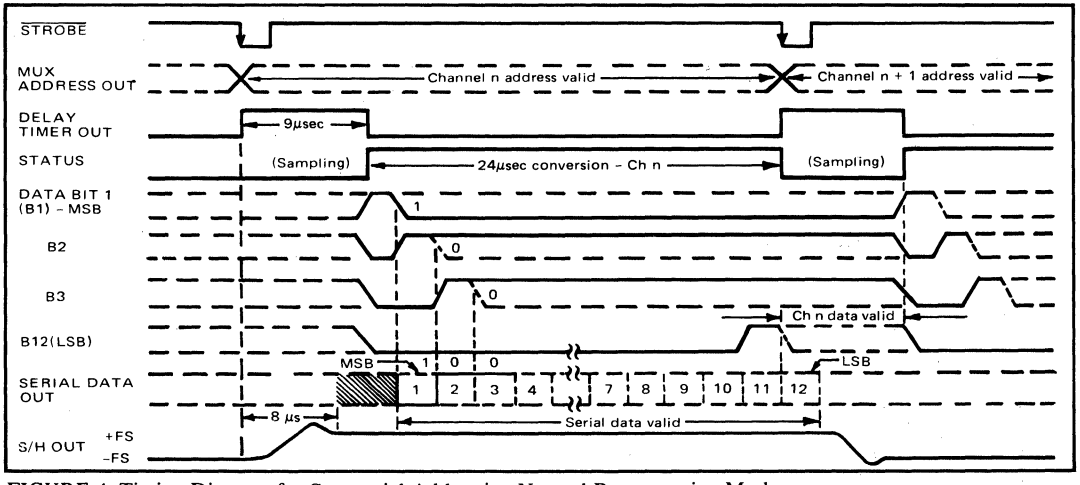


FIGURE 4. Timing Diagram for Sequential Addressing Normal Programming Mode.

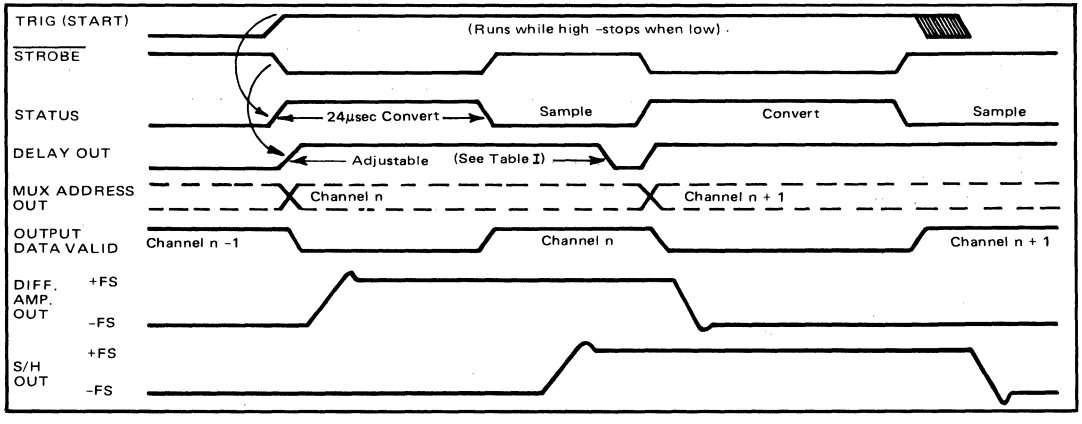
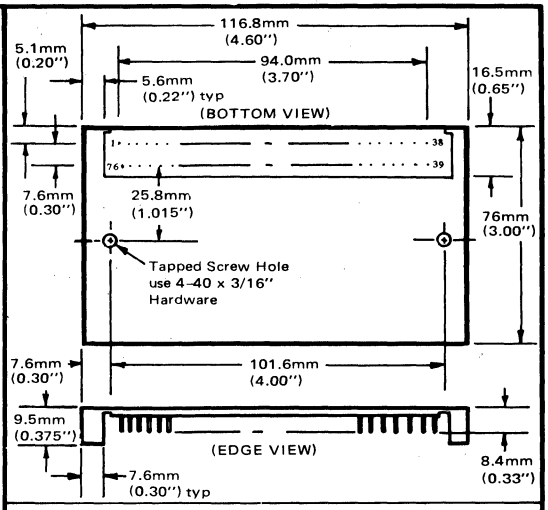


FIGURE 5. Timing Diagram for Sequential Overlap Programming Mode. (Delay must be adjusted to status pulse.)

PACKAGE AND PIN CONFIGURATION

SDM853 CONNECTOR PIN DIAGRAM

+15V	1	76	-15V
ANA. GND.	2	75	S/D ENB
CH 0 IN	3	74	CH 8 IN (0 RTN)
CH 1 IN	4	73	CH 9 IN (1 RTN)
CH 2 IN	5	72	CH 10 IN (2 RTN)
CH 3 IN	6	71	CH 11 IN (3 RTN)
CH 4 IN	7	70	CH 12 IN (4 RTN)
CH 5 IN	8	69	CH 13 IN (5 RTN)
CH 6 IN	9	68	CH 14 IN (6 RTN)
CH 7 IN	10	67	CH 15 IN (7 RTN)
MUX OUT HI	11	66	MUX OUT LO
$\overline{\text{LOAD ENB}}$	12	65	$\overline{\text{CLR ENB}}$
COUNT ENB	13	64	MUX ENB
A8 OUT	14	63	A8 IN
A4 OUT	15	62	A4 IN
A2 OUT	16	61	A2 IN
A1 OUT	17	60	A1 IN
$\overline{\text{DLY.}}$	18	59	DLY.
STROBE	19	58	$\overline{\text{STROBE}}$
ADC TRIG	20	57	ADC $\overline{\text{TRIG}}$
DLY. ADJ. 1	21	56	DLY. ADJ. 2
R1	22	55	R2
NEG REF OUT	23	54	BPO
POS. REF OUT	24	53	COMP IN
AMP IN HI	25	52	GAIN ADJ.
G2	26	51	S/H IN
G1	27	50	S/H OUT
AMP IN LO	28	49	SHT. CYC.
AMP OUT	29	48	S/H CONTROL
STATUS	30	47	$\overline{\text{B1}}$
B1 MSB	31	46	B2
B3	32	45	B4
B5	33	44	B6
B7	34	43	B8
B9	35	42	B10
B11	36	41	B12 LSB
SER OUT	37	40	CLK. OUT
+5	38	39	DIG RTN



CASE MATERIAL: Insulated Steel
CONNECTOR PINS: Gold Flashed
WEIGHT: 145 grams (5 oz.)

MOUNTING INSTRUCTIONS:

MOUNTING FLUSH ON PC CARD

1. Use strip connectors or two 14 pin and three 16 pin low profile IC sockets (shipped with each unit).
2. Use 4-40 x 3/16" (4.8mm) LG Pan HD Hardware to secure the SDM853 to PC Card.

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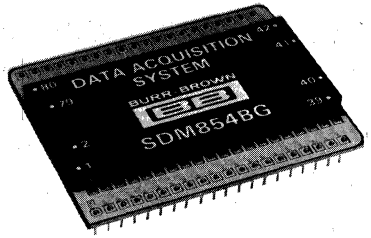


SDM854

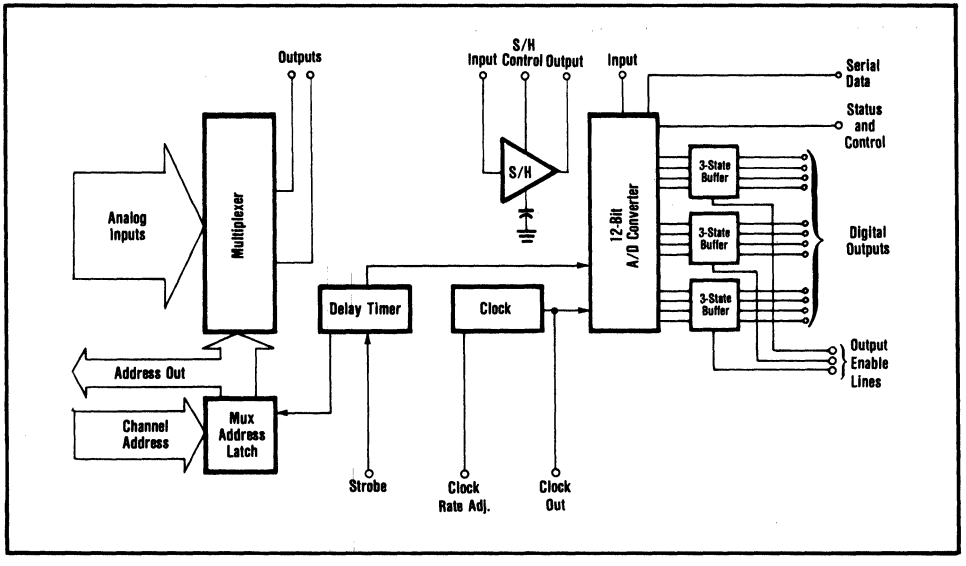
HYBRID DATA ACQUISITION SYSTEM

FEATURES

- MINIATURE SIZE
- LOW COST
- 12-BIT, ±0.012% LINEARITY ERROR
- INPUTS UP TO ±10 VOLTS
- WIDE TEMPERATURE RANGE
- SELECTABLE 16 SINGLE, 8 DIFFERENTIAL INPUTS
- THREE-STATE OUTPUT BUFFERS

DESCRIPTION

The SDM854 is a complete data acquisition system contained in a miniature 2.2" x 1.7" x 0.22" (55.9mm x 43.2mm x 5.6mm) ceramic package. This system offers all the functions available in large modular data acquisition systems. Inputs up to ±10V can be accepted and low-level inputs can be accommodated by connecting an external instrumentation amplifier to the output of the multiplexer and to the input of the sample/hold amplifier. Digital resolution is 12 bits with accuracy of ±0.024% at a throughput rate of 27kHz.



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PDS-423A

SYSTEM DESCRIPTION

The SDM854 contains all components necessary to multiplex and convert analog signals up to ±10V into equivalent digital outputs. Throughput sampling rates are from 27kHz (12-bit resolution) to 70kHz (8-bit resolution) in the overlap mode of operation. The SDM854 can be configured to accept either 8-channel differential or 16-channel single-ended signals and can be expanded almost without limit with external multiplexers. Three-state outputs are provided for easy interface to microprocessor and other bus-structure systems. The system components are illustrated in Figure 1 and described in the following paragraphs.

ANALOG MULTIPLEXER

The analog multiplexer consists of two CMOS integrated circuits. Pin interconnects are used to select 16-channel single-ended or 8-channel differential operation. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting an external amplifier's inverting input to common remote signal ground. Channel selection is made by an internally latched 3- or 4-bit binary word, for differential or single-ended operation respectively.

SAMPLE/HOLD

A complete stand-alone circuit, the sample/hold amplifier features buffered output, 10μsec acquisition time, and 100nsec aperture time.

Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions, such as automatic gain ranging, with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a 12-bit, 25μsec converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or two's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution or accuracy.

THREE-STATE OUTPUT BUFFERS

Digital outputs of the ADC are internally buffered by LSTTL three-state buffers. Three separate enable lines are brought out for easy interfacing to 4-, 8- or 16-bit data buses. $\overline{\text{MSB}}$ and BUSY are also buffered by separate three-state devices, each with its own enable line.

ADDRESS LATCH

Outputs of the 4-bit TTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input. It may be loaded through 4 address inputs. Other inputs are LOAD and $\overline{\text{CLEAR}}$. The 3 least significant bits are used for 8-channel differential mode addressing.

DELAY TIMER

A delay timer allows settling time for the multiplexer and sample/hold circuits before conversion begins. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time if an external instrumentation amplifier is used and is operating at high gains, or shorter settling time for lower resolution operation.

CHANNEL EXPANSION

The number of analog input channels of the SDM854 can be easily increased by using Burr-Brown's MPC8D (8-channel differential) and MPC16S (16-channel single-ended) multiplexers. These are latch-free devices which contain internal binary decoding at TTL or MOS levels and may be integrated into a system with minimal external logic.

SYSTEM PERFORMANCE

The SDM854 is configured for random channel selection. With the addition of an external counter they can be

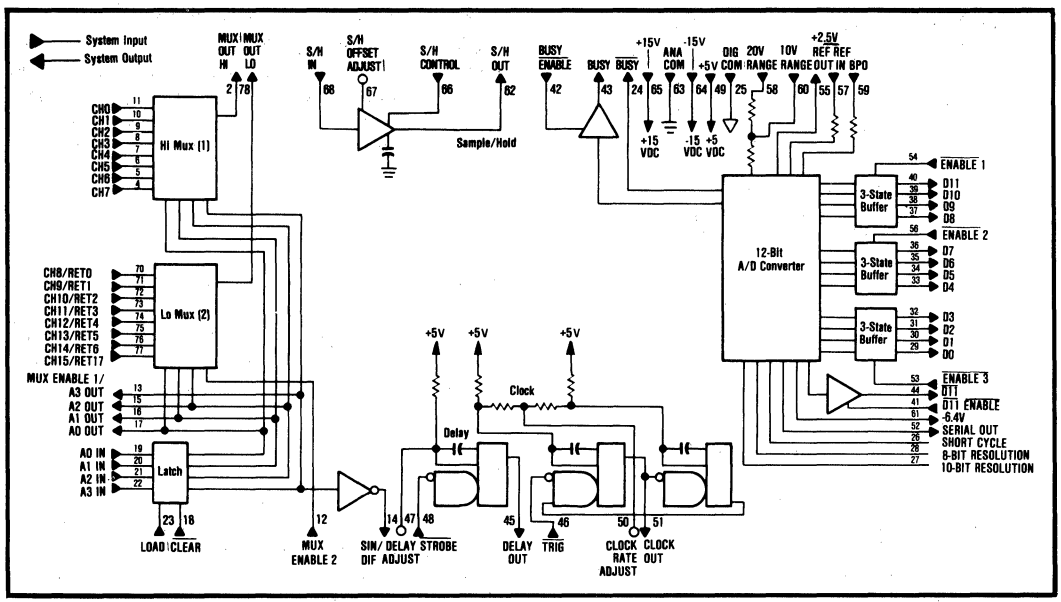


FIGURE 1. SDM854 Block Diagram.

configured to continuously sequence through all analog channels or sequence through all analog channels on command from an external trigger.

With the appropriate 4-bit (single-ended) or 3-bit (differential) channel address on the latch inputs, and DELAY OUT (pin 45) tied to the LOAD input (pin 23), a negative going edge is applied to the $\overline{\text{STROBE}}$ input (pin 48). This starts the delay timer, latches the multiplexer address, and allows the input signal to pass through the multiplexer, and sample/hold before starting the A/D conversion. The DELAY OUT signal (pin 45) is also connected to the $\overline{\text{TRIG}}$ input (pin 46) and the A/D conversion is initiated on the negative-going edge. The S/H CONTROL input (pin 66) is connected to $\overline{\text{BUSY}}$ (pin 24) so that the sample/hold is in the HOLD mode during the A/D conversion.

By using overlap programming the settling time effects of the analog multiplexer and external instrumentation amplifier (if used) can be reduced, extending throughput sampling rates up to 27kHz for 12-bit and 70kHz for 8-bit resolution (ADC short-cycled). This mode of operation is most useful when converting low-level inputs to accommodate the increased settling time of the external instrumentation amplifier. Overlap programming is accomplished by connecting $\overline{\text{BUSY}}$ to $\overline{\text{STROBE}}$ and S/H CONTROL; DELAY OUT to LOAD and $\overline{\text{TRIG}}$. In this mode of operation the address of the next channel to be converted is latched and the output of the external instrumentation amplifier allowed to settle to a new value during the present conversion.

DIGITAL INPUT SPECIFICATIONS

Address Inputs (A0 - A3)	One standard LSTTL load, positive true
Address Coding	4-bit binary
LOAD	One standard LSTTL load, positive true, address loaded on positive edge.
$\overline{\text{CLEAR}}$	One standard LSTTL load, negative true, low level clears address latch.
$\overline{\text{STROBE}}$	One standard TTL load, high-to-low transition triggers the delay timer.
$\overline{\text{TRIG}}$	One standard TTL load, a negative going edge initiates the A/D conversion.
SHORT CYCLE	One standard LSTTL load, logic 1 for 12-bit resolution. Connect to "8-bit" or "10-bit" for 8- or 10-bit resolution.
$\overline{\text{ENABLE 1}}$, $\overline{\text{ENABLE 2}}$, $\overline{\text{ENABLE 3}}$, $\overline{\text{D11 ENABLE}}$, BUSY $\overline{\text{ENABLE}}$	One standard LSTTL load, a low level enables the 3-state output.
S/H CONTROL	TTL compatible, 10μA maximum input current. Logic 0 = Hold mode, Logic 1 = Sample (track) mode.
MUX ENABLE 2	TTL compatible, 2μA input current, logic 0 enables multiplexer 2 (channels 8-15).

DIGITAL OUTPUT SPECIFICATIONS

Parallel Data Outputs	5 standard TTL loads, positive true 3-state.
Serial Output	2 standard TTL loads, positive true, NRZ, time serial data output beginning with D11 (see Timing Diagram).
$\overline{\text{D11}}$	5 standard TTL loads, positive true, 3-state.
$\overline{\text{BUSY}}$	5 standard TTL loads, low during A/D conversion.
BUSY	5 standard TTL loads, high during A/D conversion, 3-state
CLOCK OUT	5 standard TTL loads, for synchronizing serial out data (see Timing Diagram).
Address Outputs (A0 - A3)	5 standard TTL loads, positive true
DELAY OUT	5 standard TTL loads, high during delay period, triggered by Strobe input.
SIN/DIF	5 standard TTL loads, high while addressing channels 0-7, low while addressing channels 8-15. This output can go as high as 12V. It is still TTL-compatible with I_{OH} limited to <20μA above 5V.

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS				
Resolution	12			Bits
Number of Analog Channels		16SIN/8DIF		
Throughput Rate (Normal mode)				
SDM854AG	33	35		kHz
SDM854BG	25	27		kHz
Throughput Rate (Overlap mode)				
SDM854AG	38	40		kHz
SDM854BG	27	29		kHz
ANALOG INPUTS				
ADC Input Voltage Ranges		0 to +10, ±5, ±10		V
Mux Input Voltage Range				
Absolute max without damage			±35	V
For linear operation			±15	V
Mux Input Impedance, OFF Channel			10^{11}	Ω
Mux Input Impedance, ON Channel		1.5	1.8	kΩ
Input Leakage, OFF Channel		0.02		nA
Output Leakage, All Channels Disabled		0.2		nA
Output Leakage with Input Overvoltage of				
+35V		1		nA
-35V		1		μA
TEMPERATURE STABILITY				
System Accuracy				
Unipolar		±15	±25	ppm/°C
Bipolar		±10	±20	ppm/°C
Linearity Drift			±2	ppm/°C of FSR
REFERENCE VOLTAGES				
Positive Output	+2.490	+2.500	+2.510	V
Positive Output Drift		±5	±10	ppm/°C
Negative Output	-6.0	-6.4	-6.8	V
Negative Output Drift		±15	±10	ppm/°C
ACCURACY				
Throughput Accuracy				
0 to +10V, ±5V, ±10V, AG			±0.048	% of FSR(1)
0 to +10V, ±5V, ±10V, BG			±0.024	% of FSR
Linearity				
AG			±0.024	% of FSR
BG			±0.012	% of FSR
Differential Linearity				
AG		±0.024	±0.048	% of FSR
BG		±0.012	±0.024	% of FSR
Quantizing Error			±0.012	% of FSR
System Gain Error(2)		±0.1	±0.3	%
System Offset Error(2)		±0.1	±0.3	% of FSR
Power Supply Sensitivity +15V		±0.0007		%/%ΔV
Power Supply Sensitivity -15V		±0.0007		%/%ΔV
Power Supply Sensitivity +5V		±0.001		%/%ΔV
DYNAMIC ACCURACY				
Sample/Hold Characteristics				
Aperture Time		100		nsec
Acquisition Time		10		μsec
Feedthrough (10V step)		±1.4		mV
OUTPUTS				
Digital Output Coding		Binary, Offset Binary, Two's Complement		
Serial Output Coding		Nonreturn to zero (NRZ)		
ADC Conversion Time(3)		25	30	μsec
Clock Frequency(3)		520		kHz
Delay(4)		15		μsec

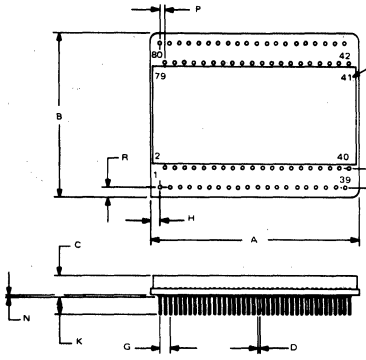
PARAMETER	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS				
Rated Voltage for Specified Accuracy	±14.5 +4.75	±15 +5	±15.5 +5.25	V V
Quiescent Current				
+15VDC		+10	+20	mA
-15VDC		-35	-50	mA
+5VDC		+170	+220	mA
Power Dissipation		1300	1750	mW
ENVIRONMENTAL				
Specification Temperature Range	-25		+85	°C
Operating Temperature Range	-40		+85	°C
Storage Temperature Range	-55		+125	°C

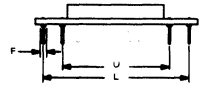
NOTES:
1. FSR means Full Scale Range (FSR is 20V for ±10V range).
2. Adjustable to zero.
3. Conversion time and clock frequency can be externally adjusted from (13μsec (f_{clock} = 1.0MHz) to 110μsec (f_{clock} = 118kHz). (Conv. times are for 12-bit resolution.) (See Figure 9.)
4. Can be externally adjusted from 3μsec to 300μsec.

PIN DESIGNATIONS

NC	1	80	NC
MUX OUT HI	2	79	NC
NC	3	78	MUX OUT LO
CH7	4	77	CH15/RET7
CH6	5	76	CH14/RET6
CH5	6	75	CH13/RET5
CH4	7	74	CH12/RET4
CH3	8	73	CH11/RET3
CH2	9	72	CH10/RET2
CH1	10	71	CH9/RET1
CH0	11	70	CH8/RET0
MUX ENABLE 2	12	69	NC
MUX ENABLE 1/A3 OUT	13	68	S/H IN
SIN/DIF	14	67	S/H OFFSET ADJUST
A2 OUT	15	66	S/H CONTROL
A1 OUT	16	65	+15VDC
A0 OUT	17	64	-15VDC
$\overline{\text{CLEAR}}$	18	63	ANA COM
A0 IN	19	62	S/H OUT
A1 IN	20	61	-6.4V REF OUT
A2 IN	21	60	10V RANGE
A3 IN	22	59	BIPOLAR OFFSET
$\overline{\text{LOAD}}$	23	58	20V RANGE
$\overline{\text{BUSY}}$	24	57	+2.5V REF IN
DIG COM	25	56	$\overline{\text{ENABLE 2}}$
SHORT CYCLE	26	55	+2.5V REF OUT
10-BIT RESOLUTION	27	54	$\overline{\text{ENABLE 1}}$
8-BIT RESOLUTION	28	53	$\overline{\text{ENABLE 3}}$
D0 LSB	29	52	SERIAL OUT
D1	30	51	CLOCK OUT
D2	31	50	CLOCK RATE ADJUST
D3	32	49	+5VDC
D4	33	48	$\overline{\text{STROBE}}$
D5	34	47	DELAY ADJUST
D6	35	46	$\overline{\text{TRIG}}$
D7	36	45	DELAY OUT
D8	37	44	$\overline{\text{D11}}$
D9	38	43	BUSY
D10	39	42	BUSY $\overline{\text{ENABLE}}$
D11 MSB	40	41	$\overline{\text{D11}}$ $\overline{\text{ENABLE}}$

MECHANICAL





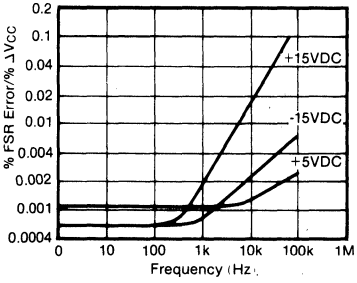
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	

NOTE:
Leads in true position within 0.015" (0.38mm)R at MMC at seating plane.

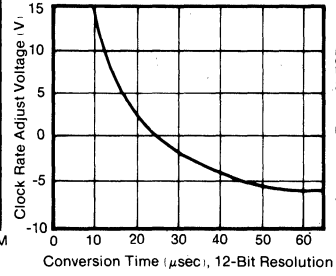
MATERIAL: Alumina
WEIGHT: 32 grams (1.2 oz)
MATING CONNECTOR:
2350MC (set of four 20-pin strips) or
0422MC (assembled unit)

TYPICAL PERFORMANCE CURVES

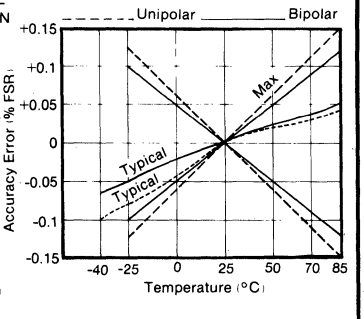
POWER SUPPLY REJECTION VS POWER SUPPLY RIPPLE FREQUENCY



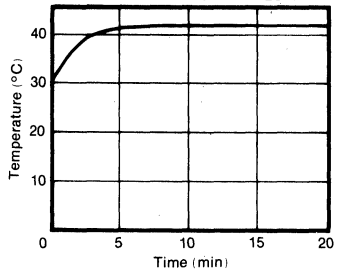
A/D CONVERSION TIME VS CLOCK RATE CONTROL VOLTAGE, 12-BIT RESOLUTION



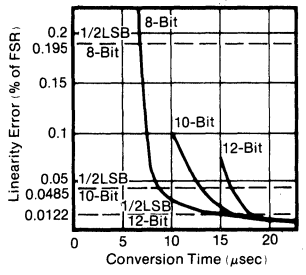
SYSTEM ACCURACY DRIFT



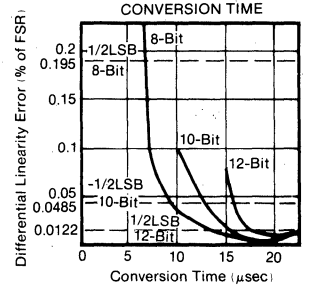
CASE TEMPERATURE VS TIME WITH NO HEAT SINK OR AIR FLOW



A/D CONVERTER LINEARITY ERROR VS CONVERSION TIME



A/D CONVERTER DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME



DESCRIPTION OF PIN FUNCTIONS

NUMBER	DESIGNATION	DESCRIPTION
Pin 1	NC	No connection.
Pin 2	MUX OUT HI	High output of the analog input multiplexer. Connect to pin 78 (MUX OUT LO) and pin 68 (S/H/IN) for single-ended input operation.
Pin 3	NC	No connection.
Pins 4 thru 11	CH7-CH0	The first 8 (of 16) analog inputs for single-ended operation or for 8-channel differential input operation.
Pin 12	MUX ENABLE 2	Connect to pin 14 (SIN/DIF) for single-ended input operation. Connect to pin 13 (MUX ENABLE 1) for differential input operation.
Pin 13	MUX ENABLE 1/ A3 OUT	Leave open for single-ended input operation. Connect to pin 12 (MUX ENABLE 2) for differential input operation. Also, A3 output line.
Pin 14	SIN/DIF	Single/Differential input operation. Connect to pin 12 (MUX ENABLE 2) for single-ended operation. Leave open for differential input operation.
Pins 15, 16, 17	A0 OUT - A2 OUT	Output lines from input channel address latch (A3 OUT is on pin 13).
Pin 18	$\overline{\text{CLEAR}}$	A low on this line clears the address latch causing the SDM854 to address channel 0 regardless of the information present on AO IN - A3 IN. Connect to +5VDC or to user logic circuitry.
Pins 19, 20, 21, 22	AO IN - A3 IN	Address lines that select one of 16 analog input signals (CH0-CH15). 0000 selects channel 0 and 1111 selects channel 15. Connect A3 to ground for 8-channel differential operation. The address is latched with a positive TTL edge on the LOAD (pin 23).
Pin 23	LOAD	A positive TTL edge on this pin latches the input channel address present on AO IN - A3 IN (pins 19, 20, 21, 22).
Pin 24	$\overline{\text{BUSY}}$	This signal will be low during the A/D conversion (≈25μsec). Output data is not valid while this signal is low. Connect to S/H CONTROL (pin 66).
Pin 25	DIG COM	Digital common. Connect to ANA COM (pin 63) as close to the SDM854 as possible.
Pin 26	SHORT CYCLE	This pin allows short cycling the A/D converter for lower resolutions thereby obtaining faster conversion times. Connect to +5VDC (pin 49) for 12-bit resolution, (pin 27) for 10-bit resolution, or (pin 28) for 8-bit resolution.
Pin 27	10-BIT RESOLUTION	To short cycle to 10-bit resolution connect to pin 26. Otherwise, make no connection.
Pin 28	8-BIT RESOLUTION	To short cycle to 8-bit resolution, connect to pin 26. Otherwise, make no connection.
Pins 29 thru 40	D0-D11	12-bit data bus, 3-state low power Schottky TTL-compatible.
Pin 41	$\overline{\text{D11}}$ $\overline{\text{ENABLE}}$	$\overline{\text{D11}}$ (pin 44) is enabled when $\overline{\text{D11}}$ $\overline{\text{ENABLE}}$ is low.
Pin 42	BUSY $\overline{\text{ENABLE}}$	BUSY (pin 43) is enabled when BUSY $\overline{\text{ENABLE}}$ is low.
Pin 43	BUSY	3-state output that will be high only while an A/D conversion is in process. Output data is not valid while this signal is high.
Pin 44	$\overline{\text{D11}}$	$\overline{\text{MSB}}$. Use instead of D11 when two's complement output is required.
Pin 45	DELAY OUT	This pulse is used to delay the beginning of the A/D conversion to allow for the settling of the multiplexer and sample/hold.
Pin 46	$\overline{\text{TRIG}}$	A negative TTL edge on this pin initiates the A/D conversion. Connect to DELAY OUT (pin 45).
Pin 47	DELAY ADJUST	When the SDM854 is addressed, an internal delay of approximately 15μsec is initiated to allow for multiplexer and sample/hold settling time. The delay can be shortened for faster lower-resolution operation.
Pin 48	$\overline{\text{STROBE}}$	A negative TTL edge on this pin initiates the DELAY OUT pulse.
Pin 49	+5VDC	**+5VDC at 200mA maximum, 170mA typical.**
Pin 50	CLOCK RATE ADJUST	Varying the voltage at this pin changes the clock frequency and thereby changes the conversion speed of the A/D converter. Connect to DIG COM (pin 25) for 12-bit operation (25μsec A/D conversion time). Connect to +5VDC for 10-bit operation and connect to +15VDC for 8-bit operation (see page 11).
Pin 51	CLOCK OUT	A/D converter clock output. Output is present only during A/D conversion. N + 1TTL pulses are output at a 520kHz rate where N is the resolution.
Pin 52	SERIAL OUT	Serial output data in NRZ format is synchronous with CLOCK OUT (pin 51) signal. Use negative edge of CLOCK OUT to strobe each bit.
Pins 53, 54, 56	$\overline{\text{ENABLE 3}}$/ $\overline{\text{ENABLE 1}}$/ $\overline{\text{ENABLE 2}}$	3-state enable lines for data bus D11 - D0 (MSB = D11). $\overline{\text{ENABLE 1}}$ (pin 54) enables D11 - D8; $\overline{\text{ENABLE 2}}$ (pin 56) enables D7 - D4; $\overline{\text{ENABLE 3}}$ (pin 53) enables D3 - D0. A low on the enable line enables data outputs.
Pin 55	+2.5V REF OUT	Positive voltage reference output. Connect to REF IN (pin 57) (through 50Ω) for unipolar or bipolar operation (unless an external reference is used). Also connect to BPO (pin 59) (through 25Ω) for bipolar operation.
Pin 57	+2.5V REF IN	Reference voltage input. Connect to +2.5V REF OUT (pin 55) (through 50Ω resistor or 100Ω pot) or use external +2.5V reference (+2.5V ±10mV at 0.5mA required).
Pin 58	20V RANGE	A/D converter input resistor. Leave open unless an external 1A with a gain greater than 2 is used. (Input multiplexers are limited to ±6V maximum input voltage.)
Pin 59	BIPOLAR OFFSET	A/D converter bipolar offset. Connect to REF OUT (pin 55) through a 25Ω resistor or a 50Ω pot for bipolar operation. Leave open for unipolar operation.
Pin 60	10V RANGE	A/D converter input resistor. Using without 1A: connect to S/H OUT (pin 62) for ±5V max input operation.
Pin 61	-6.4V REF OUT	Negative voltage reference output. Maximum current drain from this point without degradation of specifications is 200μA.
Pin 62	S/H OUT	Sample/hold output. Connect to 10V RANGE (pin 60) or 20V RANGE (pin 58) for normal operations.

DESCRIPTION OF PIN FUNCTIONS

NUMBER	DESIGNATION	DESCRIPTION
Pin 63	ANA COM	Analog common. Connect to DIG COM (pin 25) as close to the SDM854 as possible.
Pin 64	-15VDC	-15VDC at 30mA typical.
Pin 65	+15VDC	+15VDC at 30mA typical.
Pin 66	S/H CONTROL	A low signal on this line causes the sample/hold to enter the hold mode. Connect to $\overline{\text{BUSY}}$ (pin 24).
Pin 67	S/H OFFSET ADJUST	Offset adjust for sample/hold (see Figure 8).
Pin 68	S/H IN	Input to sample/hold amplifier. Connect to MUX OUT HI (pin 2) and MUX OUT LO (pin 78).
Pin 69	NC	No connection.
Pins 70 thru 77	CH8-CH15 RET0 - RET7	Analog inputs 8 through 15 for single-ended operation or analog returns 0 through 7 for differential input operation.
Pin 78	MUX OUT LO	Multiplexer output for CH8-CH15 (single-ended) or RET0-RET7 (differential). Connect to MUX OUT HI (pin 2) and S/H IN (pin 68) for single-ended operation.
Pin 79	NC	No connection.
Pin 80	NC	No connection.

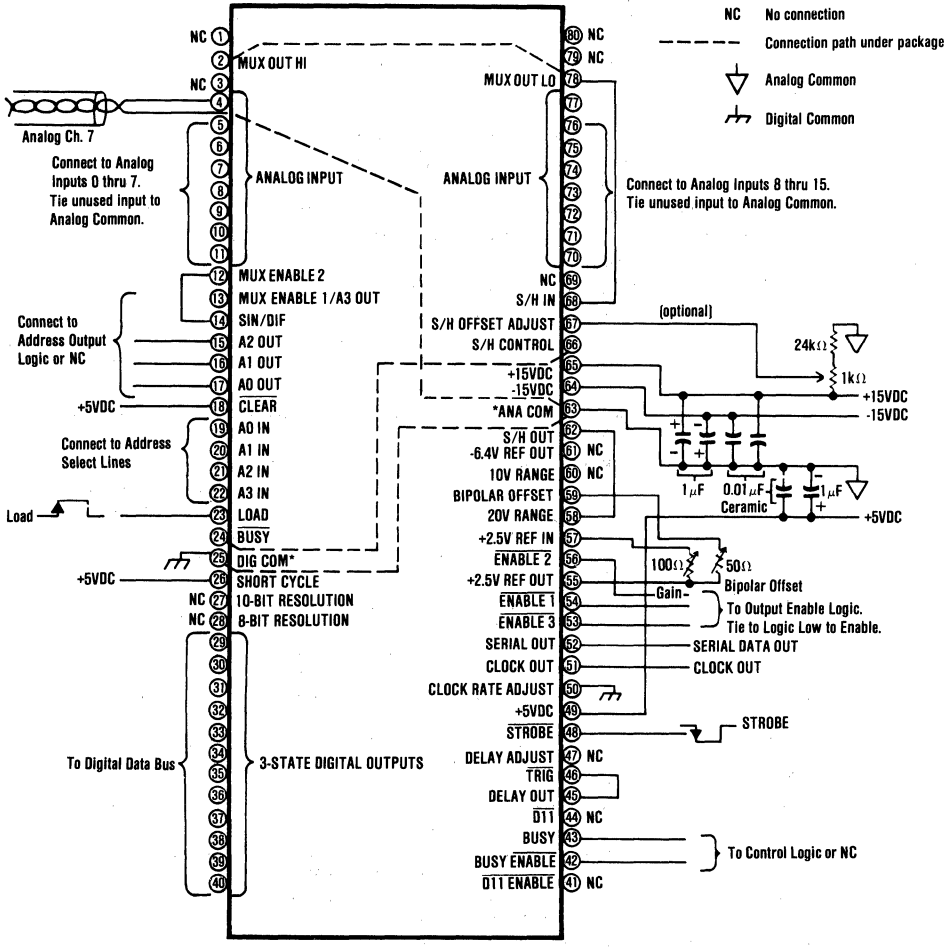


FIGURE 2. Connection Diagram for SDM854 Operating Under These Conditions:
Analog Input: Bipolar, single-ended; Reference Voltage: Internal; Resolution: 12-bits; Mode: Normal; Digital Output: Binary.

SETUP PROCEDURE

INPUT CONNECTIONS

Unused analog inputs must be connected to ANA COM, pin 63. When long leads are connected to the inputs, care must be taken that leads do not pick up excessive noise from external equipment and wiring. When low-level applications are undertaken, it is usually advisable to operate the system as an 8-channel, differential input system. This will require an external differential amplifier to be wired in between the output of the multiplexer and the sample/hold amplifier. In this way any noise will be common to both input wires, and will be rejected by the instrumentation amplifier. For best noise rejection use twisted shielded pair cable. The inputs of the SDM854 are protected from damage by voltage as high as ±35 volts and from short spikes well in excess of this for a few microseconds; however, careful wiring and cable routing practices are recommended.

Single-Ended Inputs

For single-ended inputs connect pin 2 and pin 78 (MUX OUT HI and MUX OUT LO) to pin 68 (SAMPLE/HOLD amplifier input), all unused inputs to the multiplexer and all signal returns to pin 63 (ANA COM).

Differential Inputs With External Instrumentation Amplifier

Connect the signal inputs to pins 4 through 11, and their returns to 77 through 70. Connect pin 12 to 13. Connect pins 2 and 78 to the noninverting and inverting input of the amplifier respectively. The output of the amplifier is connected to pin 68.

SAMPLE/HOLD

Connect S/H CONTROL, pin 66, to the ADC $\overline{\text{BUSY}}$ output, pin 24.

ANALOG-TO-DIGITAL CONVERTER INPUT VOLTAGE RANGE

The analog-to-digital converter is essentially a current input device having a current input range of 0 to 2mA. The input may be considered a virtual ground summing point. To convert voltage to current, a center tapped 10kΩ resistor is internally connected to this summing point. This is illustrated in Figure 3.

The interconnection of the ADC pins and the S/H OUT, pin 62, are shown in Table I.

TABLE I. ADC Range Jumpers.

Input Range (V)	Jumper
0 to +10	59 Open, 60 to 62, 58 Open
-5 to +5	59 to 55, 60 to 62, 58 Open
-10 to +10	59 to 55, 58 to 62, 60 Open

NOTE: Input ranges in Table I apply to ADC only.

OUTPUT CODE

For unipolar binary and offset binary use D11 (pin 40) for the most significant bit. Two's complement binary is obtained by using pin 44, $\overline{\text{D11}}$, as the most significant bit. One's complement code may be obtained by a different offset adjustment in the calibration procedure. Two's complement and one's complement codes are usually used only for bipolar signal ranges. For 12-bit resolution, SHORT CYCLE (pin 26) is left open or taken to +5VDC. Connect pin 26 to pin 27 (10-bit) or pin 28 (8-bit) to obtain lower resolution. The conversion time will be shortened by the following formula:

(Conversion Time) = (25μsec) x [1 - (12-R/13)]
where R is the resolution desired.

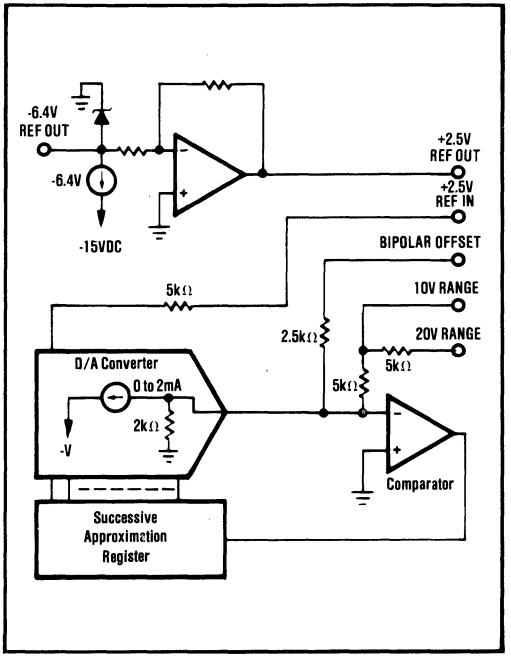


FIGURE 3. Analog-to-Digital Converter.

NORMAL AND OVERLAP MODE

The two basic modes of system operation are normal and overlap. In normal operation the channel address, N, is loaded or clocked into the address latch. The addressed channel will remain selected during its analog-to-digital conversion. In overlap mode channel N + 1 is selected while channel N is being converted. This can be used to increase the system throughput rate by allowing the multiplexer and external instrumentation amplifier to settle while a conversion is being made. In this way the throughput rate is limited by the sample/hold acquisition time and the analog-to-digital converter conversion time. For this reason, the overlap mode is more desirable for low-level signals. Table II and Figures 4 and 5 provide additional timing details. At high signal levels a high source resistance may increase the multiplexer settling time to an extent which makes the overlap mode desirable.

Normal Mode Connections

Connect DELAY OUT, pin 45 to $\overline{\text{TRIG}}$, pin 46.

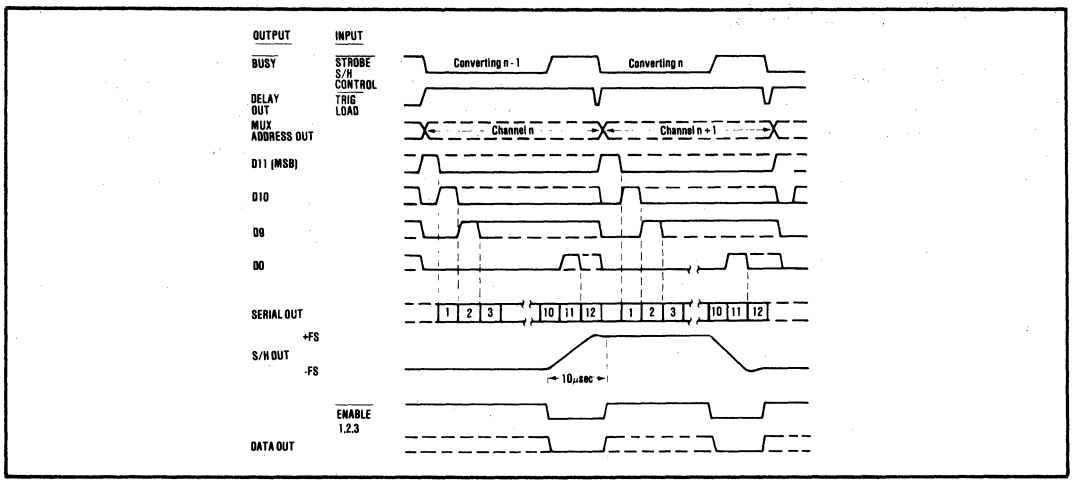


FIGURE 4. System Timing for Overlap Operation.

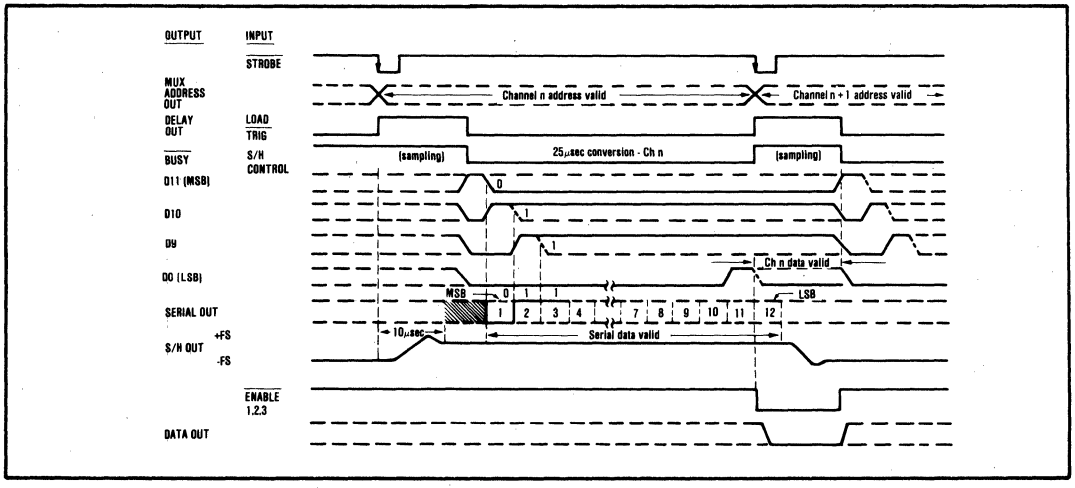


FIGURE 5. System Timing for Normal Operation.

Overlap Mode Connections

Connect $\overline{\text{BUSY}}$, pin 24 to $\overline{\text{STROBE}}$, pin 48, and DELAY OUT, pin 45 to TRIG, pin 46. Adjust the delay as described in the following paragraph.

DELAY ADJUSTMENT

The delay timer may be adjusted with an external capacitor or resistor from DELAY ADJUST (pin 47) to +5VDC. A capacitor will increase the delay to allow for increased settling time while a resistor will decrease the delay to allow for increased throughput rate with an external high speed instrumentation amplifier or lower resolution operation.

The values of R and C versus delay are shown in Figures 6 and 7.

GROUNDING CONSIDERATIONS

The circuit configuration of a high speed successive approximation A/D converter is such that low-level analog and digital signals are in close proximity. In fact the two circuits are actually interconnected; for this reason no AC noise voltage should be allowed to exist between digital and analog ground. Digital and analog ground should be connected as close to the unit as possible. In a typical application an SDM module will be used near a computer. For best results the SDM digital ground should be connected to the computer's +5VDC supply ground at the supply terminal. The ±15VDC supply ground should be left floating, if possible. The Burr-Brown Model 546 +5VDC to ±15VDC DC/DC converter is a convenient way to do this. For single-ended systems, signal returns are connected to analog ground.

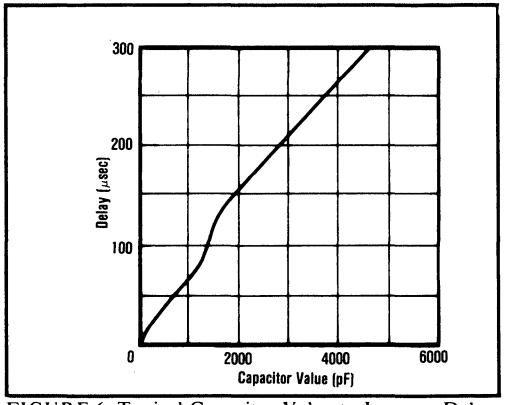


FIGURE 6. Typical Capacitor Value to Increase Delay Time*

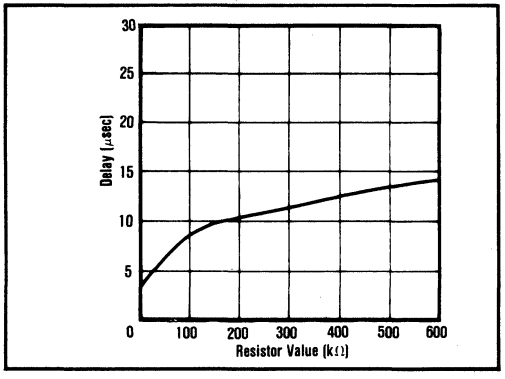


FIGURE 7. Typical Resistor Value to Decrease Delay Time.*

*Capacitor or resistor is connected from pin 47 to +5V supply.

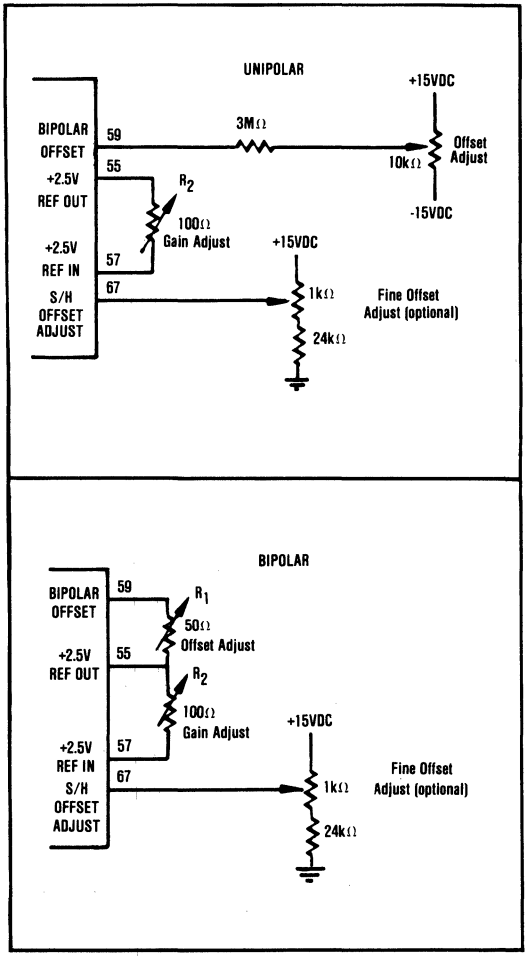


FIGURE 8. External Gain and Offset Adjustment.

CALIBRATION PROCEDURE

GAIN AND OFFSET ADJUSTMENT

External gain and offset adjustment potentiometers are shown in Figure 8. Cermet pots with a T.C.R. of ±100ppm/°C or less should be used. The adjustments shown each have a range of ±0.3% of the Full Scale Range.

If adjustment of gain and offset is not required R1 and R2 should be replaced with 25Ω and 50Ω resistors respectively. These resistors should be low T.C. (<±100ppm/°C) metal film or equivalent.

The S/H OFFSET ADJUST (pin 67) may be used as a fine offset adjustment.

The easiest way to calibrate the device is to connect a voltage source to multiplexer input CH0 (either differential or single-ended input operation may be used). Channel zero will be addressed by simply connecting $\overline{\text{CLEAR}}$ to DIG COM.

After the CH0 voltage source has been addressed, set it to the most negative value of the input range being used plus 1/2LSB. Twelve-bit LSB voltage values are given in Table III. Connect a triggering source to $\overline{\text{STROBE}}$ and adjust the offset potentiometer until all output bits are logic 0 with bit DØ dithering between logic 0 and 1. Change the source voltage to the most positive value of the input range minus 3/2LSB. Adjust the gain potentiometer until all output bits are logic 1 with bit D0 dithering between logic 1 and 0. When a resolution less than 12 bits is used, the LSB voltage is given by the formula in Table II where N is the number of output bits. One's complement coding is obtained by shifting the previous adjustments up by 1/2LSB using the offset potentiometer.

TABLE II. LSB Values for 12-Bit Resolution.

$$\text{LSB (Volts)} = (\text{Range})/(2^N)$$

Range	LSB Voltage (12-Bits)
5V	1.22mV
10V	2.44mV

SDM854

CLOCK RATE ADJUSTMENT

To obtain higher throughput rates at lower accuracy the A/D clock rate can be adjusted by varying the voltage on the clock rate adjust pin. This point should be connected to digital common for 12-bit accuracy, +5VDC for 10-bit accuracy, or +15VDC for 8-bit accuracy giving conversion times of 25μsec, 15μsec and 10μsec respectively. The conversion speed can also be continuously varied from about 13μsec to 110μsec (12-bit resolution) with a potentiometer as shown in Figure 9.

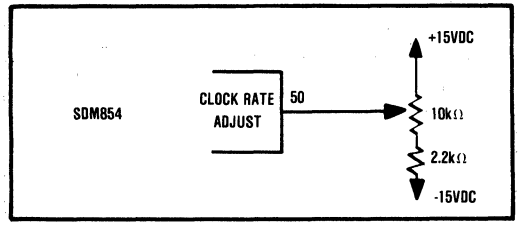


FIGURE 9. Clock Rate Adjustment.

CHECKOUT PROCEDURE

Checkout is essentially accomplished by the calibration procedure. Before the unit is plugged into a new installation, it is well to go over the pin connection list to be sure that all 80 pins have been properly connected in the setup. Linearity and monotonicity may be verified by varying the input voltage over the complete range during the calibration procedure.

LATCH

Latch operation can be verified by connecting a pulse generator to the LOAD input. The address inputs (A0 IN - A3 IN) should appear at the address outputs (A0 OUT -A3 OUT).

MULTIPLEXER

To check the multiplexer connect a voltmeter to the multiplexer output (pin 2 and pin 78) and observe that the output changed when the address was changed.

SAMPLE/HOLD

The sample/hold circuit can be checked during the calibration procedure by observing the output of the S/H OUT (pin 62) with an oscilloscope. The waveform should be approximately as in Figure 10.

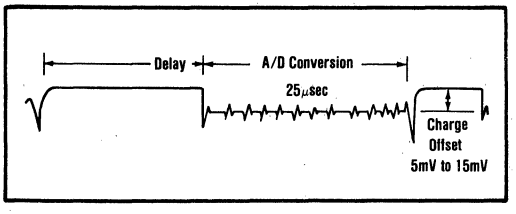


FIGURE 10. Sample/Hold Output Waveform.

The charge offset will vary in a linear manner from about 5mV for -10V to 15mV for +10V. This is compensated for by the offset and gain adjustments of the A/D converter. The spikes during conversion are normal noise caused by the converter operation.

ANALOG-TO-DIGITAL CONVERTER

The ADC can be checked out as an individual circuit element. Connect a fixed voltage to either 20V RANGE (pin 58) or 10V RANGE (pin 60). After adjusting the gain and offset errors as described on page 10, the digital output should represent the analog input as shown in Table III. To enable the three-state buffers, pins 53, 54 and 56 should be connected to logic 0.

TABLE III. Delay Timer Settings for Specified Settling Time Accuracies Using an External Burr-Brown 3630 Instrumentation Amplifier.

Full Scale Input Range	ADC Range	Amplifier Gain	Resolution	Delay Timer Setting, μsec		
				To ±0.2%	To ±0.05%	To ±0.01%
20V	±10V	1	4.88mV	60	75	100
1V	0 to +10	10	244μV	50	60	75
0.1V	0 to +10	100	24.4μV	100	115	150
10mV	0 to +10	1000	2.44μV	500	700	1000

In overlap, when the external amplifier multiplexer settling time is less than the ADC conversion time, set the delay timer for the ADC conversion time plus the sample hold acquisition time (30μsec plus 10μsec). When the external amplifier multiplexer settling time exceeds the ADC conversion time plus the S/H acquisition time, set the delay timer for the external amplifier multiplexer time.

APPLICATION NOTES

CHANNEL CAPACITY EXPANSION

The SDM854 may be easily expanded to any number of channels by using Burr-Brown Models MPC8D and MPC16S. The MPC8D is an 8-channel double-ended multiplexer, and the MPC16S is a 16-channel single-ended multiplexer. The devices are CMOS FET units which can operate from supply voltages up to ±20VDC. They feature latch-free operation with full input protection. Binary decoding and level shifting circuits are included. Logic levels are jumper selectable for TTL or CMOS. Packaging is a 28-pin DIP.

There are two methods for using these devices for channel capacity expansion. The SDM854 multiplexer may be expanded by shunt or series connected multiplexers. Shunt connection refers to connecting the output of several multiplexers together and enabling each in sequence. The disabled devices present a very high resistance to the common output line. The disadvantages to this scheme are increased leakage current and output capacitance. For these reasons shunt connections are usually used only when it is desired to expand the capacity by a factor of two or three. A shunt connected system logic diagram is shown in Figure 11. Forty-eight single-ended

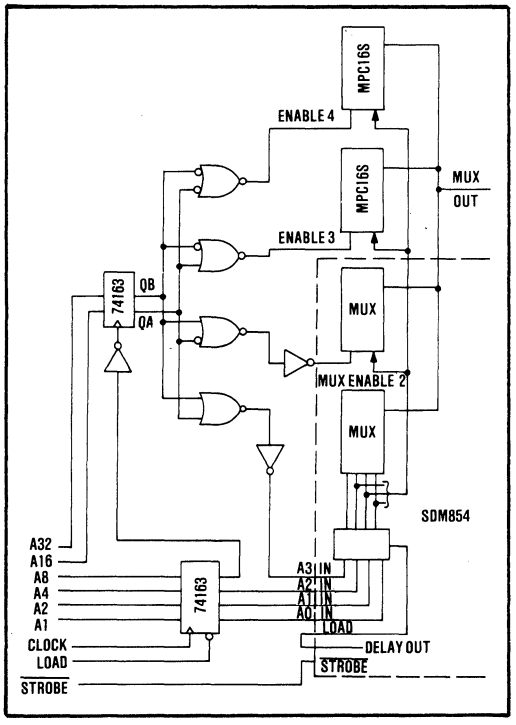


FIGURE 11. Shunt Connected Multiplexer System, 32 Single-Ended Channels.

channels are indicated; however, 24 double-ended channels could easily be realized by using two MPC8D's and connecting the two-sided outputs appropriately. For large systems series connected expansion is usually used. In this method the outputs of a second tier of multiplexers are connected to the inputs of the SDM854 multiplexer. This allows up to 256 single-ended or 128 double-ended channels to be addressed. A third tier can be used for 4096 single or 2048 double-ended channels. A logic diagram of a series system is shown in Figure 12. Double-ended operation can be obtained by using the MPC8D instead of the MPC16S and connecting the SDM854 for double-ended operation.

SEQUENTIAL ADDRESSING

Simply adding an external counter will allow sequential addressing of all 16 input channels (see Figure 13).

MULTIPLEXER CIRCUIT OPERATION

At the address and enable inputs a voltage is interpreted as a logic "1" if it is greater than 2.4 volts; and "0" if less than 0.8 volts.

When an input channel has been selected the "on resistance" from input to output is 3kΩ. The input capacitance for each channel is approximately 7pF, while the output capacitance is approximately 25pF for each 8-channel multiplexer. A circuit model of an ON channel is shown in Figure 14.

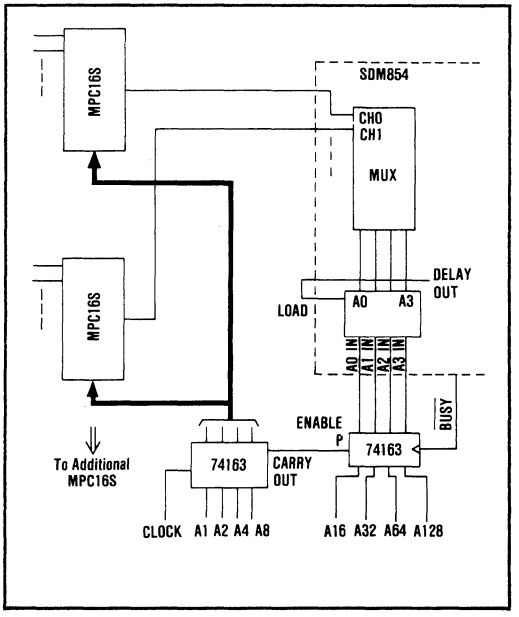


FIGURE 12. Series Connected Multiplexers, 256 Single-Ended Channels (Sequential Addressing).

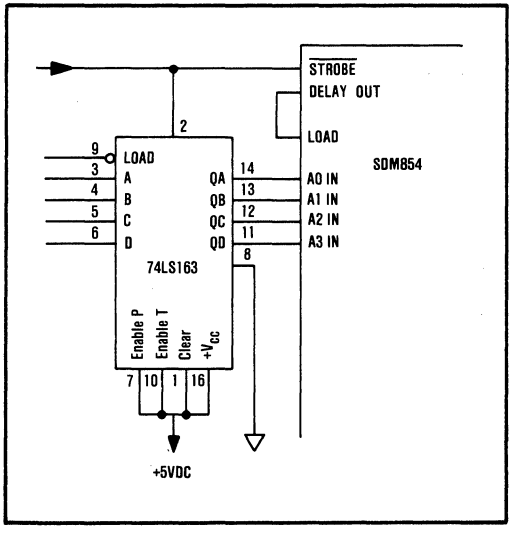


FIGURE 13. Sequential Addressing.

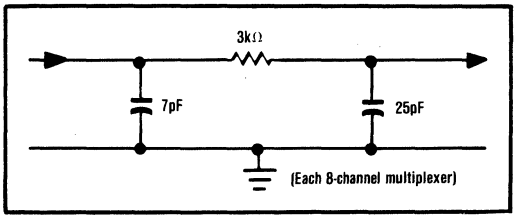


FIGURE 14. ON Channel Circuit Model.

This model is very important when high speed switching of high output impedance sources is required. For example, if the full accuracy and resolution of the system is required, the signal at the output of the multiplexer must be allowed to settle to about 0.01%. If the source impedance is 1kΩ, the 7pF can be neglected and the multiplexer has a time constant of 2.8kΩ x 50pF = 140nsec. It requires approximately 9 time constants to settle to 0.01%; 1.26μsec is well within the 15μsec of the SDM854 delay timer. However, if the source impedance had been 10kΩ, the 0.01% settling time would have approached 6μsec. For high speed multiplexing of higher impedance sources, it will usually be desirable to parallel the 7pF input capacitor with a large capacitor; however, this could limit the source bandwidth. In any case there is no point in making it any larger than 10^4 times the output capacitance, or 0.5μF. When this size storage capacitor is used, the output time constant is 1.8kΩ x 50pF = 90nsec. This means that the system settling time is essentially determined by the settling time of a differential amplifier and sample hold circuit. For switching of large signals it must be remembered that the ON resistance is the channel resistance of a FET, and, as such, it is a nonlinear function of the applied voltages. Any FET will current limit at its I_{DSS} value. As a result, the previous calculations are only an approximation derived from a linearized model. The settling time to 0.01% for a 20V step is approximately 4.0μsec for source impedance less than 1kΩ.

The analog and digital inputs have reverse biased diode circuits which prevent damage from discharge of static electricity. However, it is still wise to take reasonable precaution against static discharge.

BINARY SCALING

Binary scaling of the A D converter provides LSB voltages of 2.5mV, 2.5mV, and 5.0mV for voltage ranges of 0 to 10.24V, -5.12V to +5.12V, and -10.24V to ±10.24 respectively. These may be obtained by adding external resistors in series with input resistors of the A D converter. Metal film resistors with temperature coefficients of less than 100ppm °C are recommended. This is shown in Figure 15.

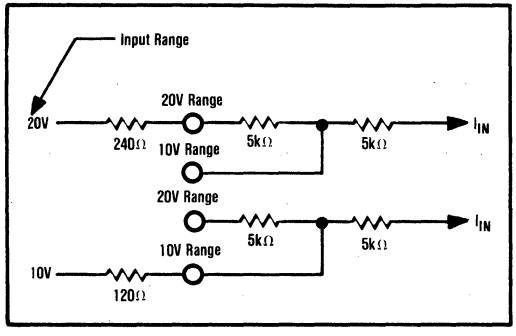


FIGURE 15. Binary Scaling.

USING AN INSTRUMENTATION AMPLIFIER WITH THE SDM854

When low-level signals are being converted, such as with thermocouples, strain gauges, etc., it will be necessary to use an instrumentation amplifier (IA) with the SDM854 to utilize the full dynamic range of a 12-bit system. This can be done by connecting the IA between the multiplexer and sample hold amplifier because the output of the multiplexer and the input of the sample hold amplifier are both brought out separately on the SDM854.

There are two ways an external IA can be connected to increase the versatility of the system. The most accurate way is to use the amplifier in a true differential mode as shown in Figure 16, where a Burr-Brown 3630 is connected

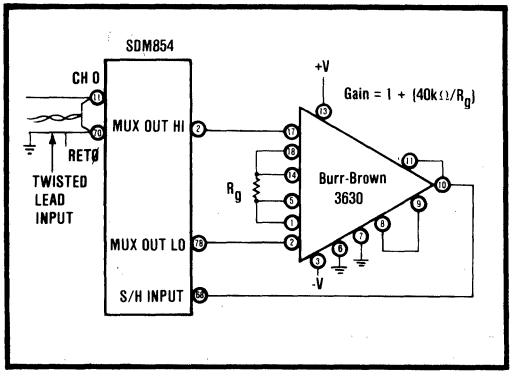


FIGURE 16. Instrumentation Amplifier Connection for True Differential Input.

to the SDM854 for differential operation. This configuration is ideal where the input lines run over a long distance or through noisy environments. For best results the input links should be in twisted shielded pairs with the shield grounded at one end to prevent ground loop currents from forming.

A second way to use an IA is in the pseudo-differential mode as shown in Figure 17. This method is ideal if all of

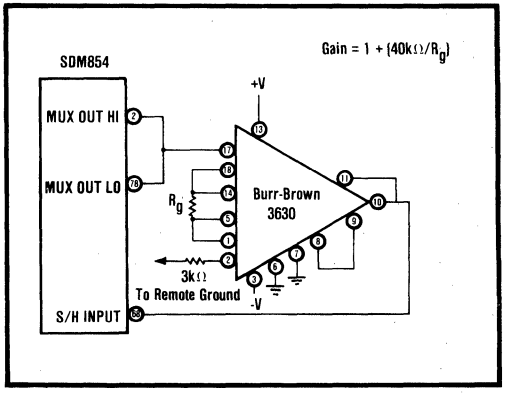


FIGURE 17. Instrumentation Amplifier Connection for Pseudo-Differential Input.

the input signals come from the same general area and at the same ground potential. In this application the inverted input of the IA can be used as a ground sense line. The IA will then reject the difference in ground potential and any common noise pick up from the ground sense line and the signal path. Care should be taken to match the impedance to ground from both inputs of the IA. This will insure the rejection of bias current effects from the IA. For better noise rejection the input lines should be grouped and shielded with the shield grounded at one end as in the true differential connection. One advantage of the pseudo-differential connection is that the multiplexers are operated in the single-ended mode allowing for 16 different input signals versus only 8 inputs in the true differential operation.

In both the true differential and pseudo-differential operation care should be taken in choosing the correct IA to maintain the high accuracy and linearity of the system.

Some of the important characteristics are:

1. Linearity error $\leq 0.012\%$ at all gains
2. Offset current drift $\leq 1/2LSB/(Gain)(R_{source})\Delta T$
3. CMRR $> CM_{signal}/1/2LSB$
4. Offset voltage drift $< 1/2LSB/(GAIN)\ \Delta T$
5. High input impedance $> R_{source} \times 10^4$

The importance of initial offsets are somewhat minimized by the capability to cancel out offset at several points in the system. The Burr-Brown 3630 was chosen for this application because of its high linearity, good drift spec and CMRR characteristics. Some of the accuracy calculations for the Burr-Brown 3630 are as follows:

Nonlinearity = $\pm 0.002 + 10^{-5}$ (Gain) % FS at G $\leq$ 100
nonlinearity is $\leq 0.003\%$FS
Input impedance = $10^9\Omega$ so source impedance up to 100kΩ can be used.
Voltage offset drift at Gain = 100
$0.25\mu V/^{\circ}C \leq 1.22mV$ $100\Delta T$ so $\Delta T \leq 49^{\circ}C$
for errors $\leq$ 1 2LSB.
CMRR at Gain = 100 is 110dB
CM range = 10V/1.22mV = 78dB.

THERMOCOUPLE TEMPERATURE ACQUISITION

Thermocouples are often used as temperature sensors for process control systems. Thermocouples are characterized by temperature coefficients of $10\mu V/^{\circ}C$ to $70\mu V/^{\circ}C$ and operating ranges of minus hundreds to plus thousands of degrees centigrade. When the SDM854 is operated with an external instrumentation amplifier gain of 100 to 1000, it may be connected directly to these devices. However, electronic instrumentation is usually mounted in a temperature controlled environment with long runs of thermocouple wire to the actual point of temperature measurement. These long wire runs often pick up large common-mode noise signals of 60Hz or higher frequencies. When the SDM854 is used as an 8-channel differential input system, the high common-mode rejection of the external instrumentation amplifier will reject common-mode noise. To minimize differential mode noise, signal wires should be twisted and possibly shielded. As a rule, an open twisted pair is better than a coax, and a shielded, twisted pair better still. In applications where these wiring practices cannot always be observed, a differential RC filter may be used (see Figure 18).

The 10kΩ resistors and a $10\mu F$ capacitor provide low-pass filtering ($f_c = 0.8Hz$) while the 1MΩ resistors supply bias current to the instrumentation amplifier. The remote sensor should be earth grounded to prevent common-mode voltages from exceeding the $\pm 15V$ range of the multiplexer. This will usually supply bias current; however, the resistors provide a back up. It is not obvious what resistance the bias currents of the amplifiers will see. The 1MΩ resistors do not enter into an error calculation for input drift because the low resistance of the sensor shorts any differential current of the amplifier. Offset or difference current is merely the difference between the bias currents of each input. See page 15 for a worst-case error analysis of the input filter for multiplexed data acquisition systems. The 1MΩ resistors could have been put on the output side of the multiplexer eliminating the

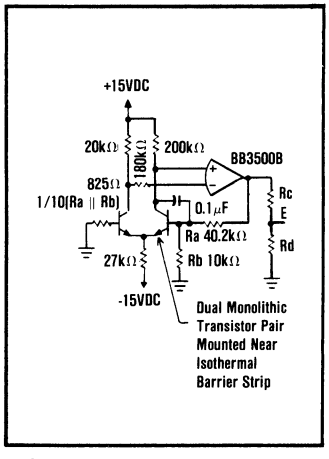


FIGURE 18. Thermocouple Inputs.

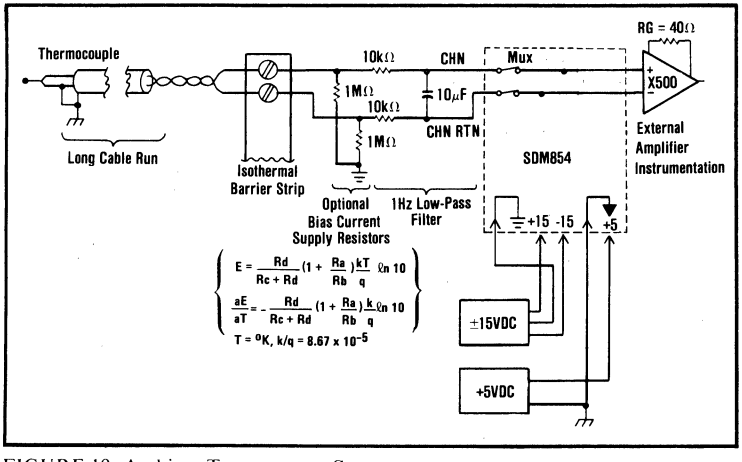


FIGURE 19. Ambient Temperature Sensor.

need for repeating them for each input; however, this would have loaded the 10kΩ resistors of the filter causing a possible 1% error for static conditions.

To complete a thermocouple system it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary barrier strip in an enclosed cabinet with even air circulation is usually adequate. The temperature of this barrier strip must be monitored to allow the observed thermocouple emf to be cold junction compensated. Figure 19 shows an excellent circuit for this purpose. Its output is connected to one of the input channels to supply ambient temperature data to the system computer.

INPUT FILTER DESIGN FOR LOW-LEVEL SYSTEMS

When the SDM854 is used to acquire low-level sensor data, it is often desired to place a low-pass, passive filter on each input. This is usually done to reduce any differential mode, power line frequency pickup. Figure 20 shows such a circuit.

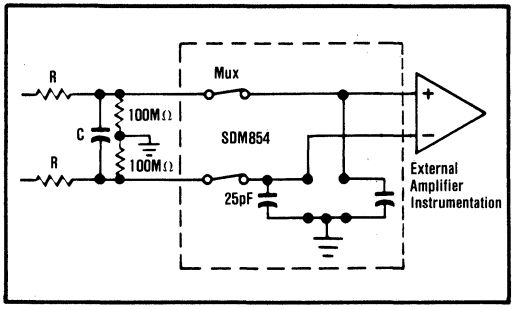


FIGURE 20. Input Filter Design for Low-Level System.

This circuit is deceptive in its simplicity. Actually four errors sources should be considered in its design. They are loading, offset current, charge transfer, and pump out current.

The static loading error is simply the resistive divider created by the filter resistors and the 100MΩ input resistance. For low-level sensors, 0.1% system accuracy is usually adequate. Thus R should be less than 10^{-3} x (100MΩ) = 100kΩ. However, if the inputs are scanned at a high speed, and between scans the multiplexer can be addressed to a unique channel having a lower resistance, higher filter resistance can be tolerated because the large filter capacitor will act as a voltage source during the 30μsec to 100μsec period required to read each channel. The filter capacitors will then recharge between scans.

The input offset current caused by the bias currents of the external instrumentation amplifier as well as any leakage current of the multiplexer will cause an error voltage proportional to the size of the filter resistors ($E = I_{OS} \times 2R$). Of course, this is a static error and as for loading error, may not be important for some operating conditions. If all channels have the same resistance most of this error may be corrected by the offset adjustment of the analog-to-digital converter. If the offset current drift is 0.1nA °C the error is 2R x 0.1nV °C. For 10kΩ resistors this would be 2μV °C.

When the multiplexer scans, charge will be transferred from the filter capacitor to the 25pF output capacitance of the multiplexer. For less than 0.1% of full scale error, the filter capacitor must be large than 25000pF. This assumes that adjacent channels may differ by the full scale voltage.

Pumpout current refers to charge being transferred from the filter capacitor to the multiplexer capacitance at time intervals short enough that the filter capacitor does not have time to recharge between scans. At high scan rates this may be considered a DC current which may add to the offset current. Assume a 10μF capacitor sampled once per millisecond. For a 20mV full scale range, the maximum effective current is (20mV x 25pF) 1msec = 0.5nA. If the filter resistors are 10kΩ, a 0.5nA x 20kΩ = 10μV error is created.

When no input filter is used, the signal source must be able to charge the multiplexers and any cable capacitance during the channel acquisition time of the multiplexer and external amplifier. This is discussed on page 13. When all of these errors as well as the basic 2.0μV °C input offset voltage drift of the external amplifier are considered, the overall system accuracy may be estimated.

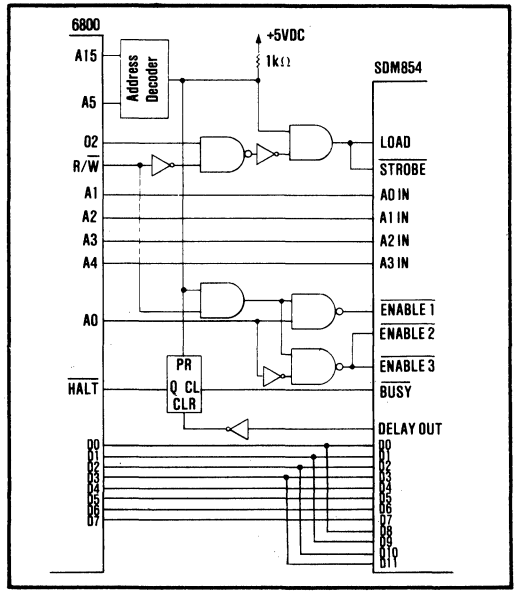


FIGURE 21. SDM854 Interfaced to 6800 Microprocessor.

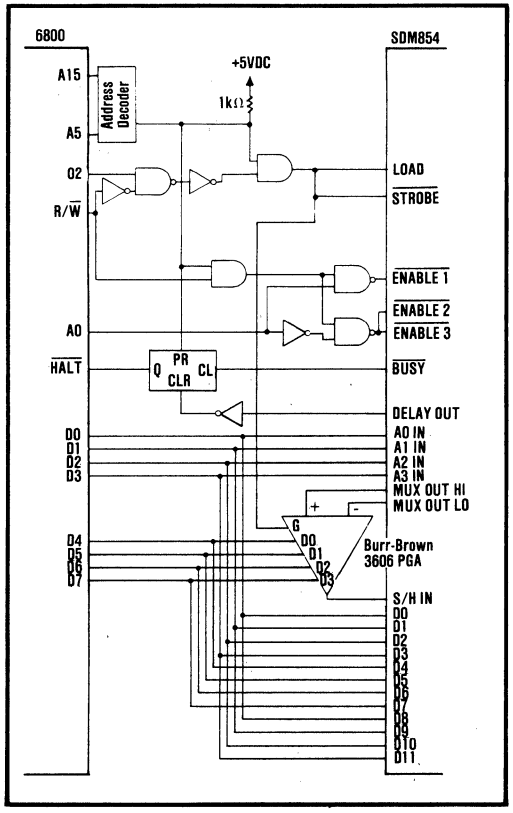


FIGURE 22. SDM854 and 3606 PGA Interfaced to 6800.

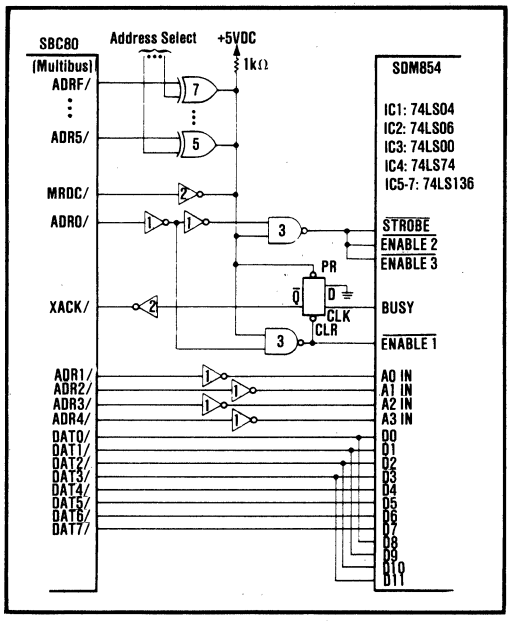


FIGURE 23. SDM854 Interfaced to SBC80 Multibus.

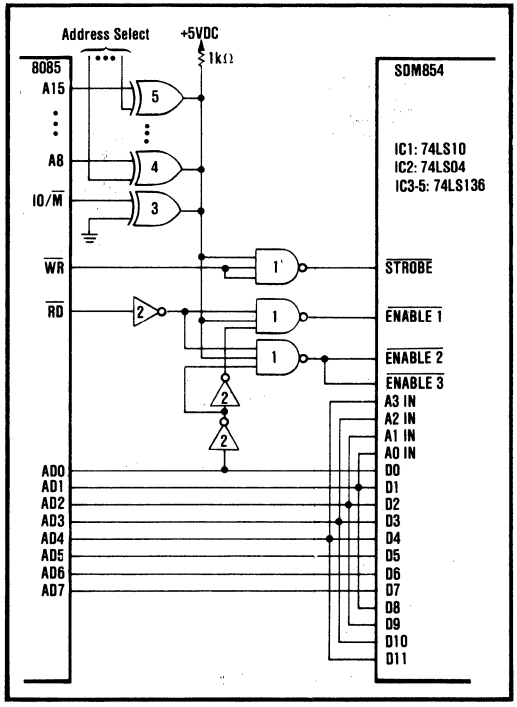


FIGURE 24. SDM854 Interfaced to 8085.

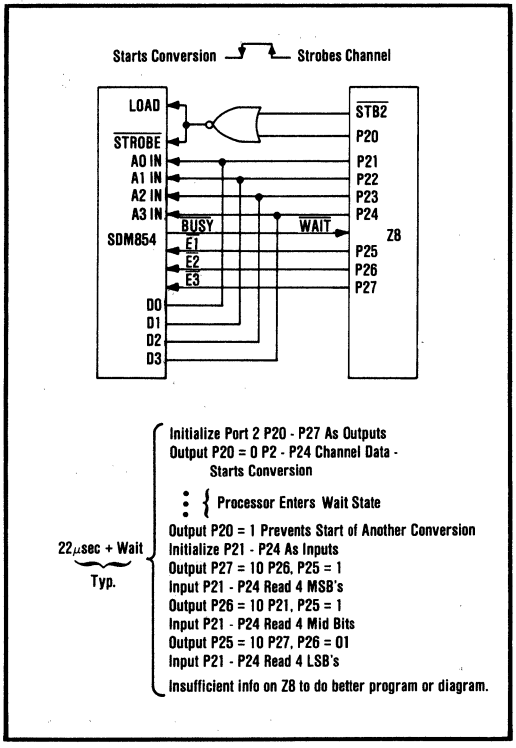
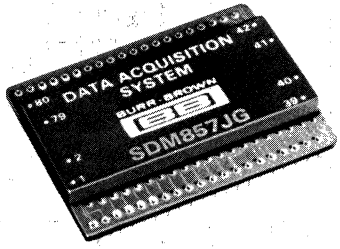


FIGURE 25. SDM854 Interfaced to Z8.

BURR-BROWN®



SDM856
SDM857

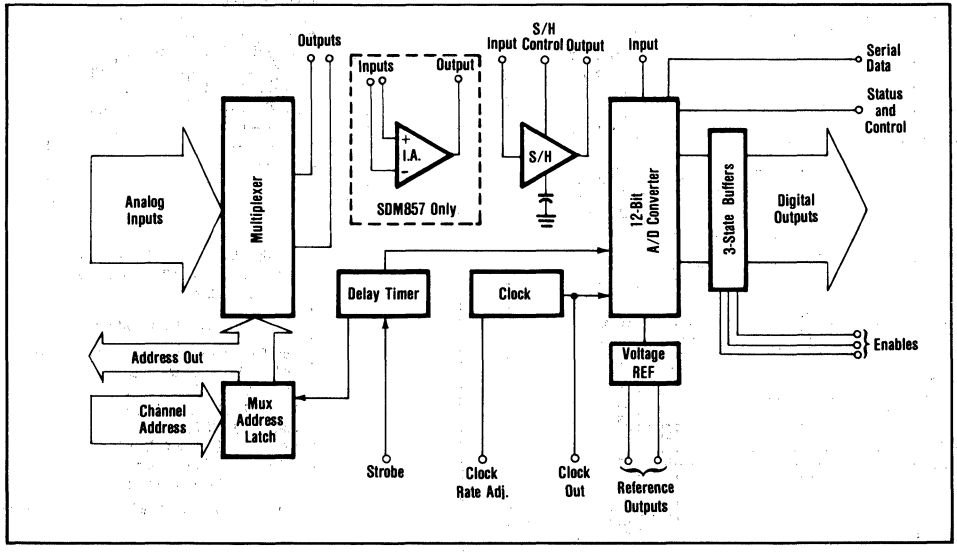
HYBRID DATA ACQUISITION SYSTEM

FEATURES

- MINIATURE SIZE
- LOW COST
- 12-BIT, 0.024% ACCURACY
- INSTRUMENT AMP OPTION
- LOW LEVEL INPUTS (SDM857)
- SELECTABLE 16 SINGLE, 8 DIFFERENTIAL INPUTS
- THREE-STATE OUTPUT BUFFERS
- 60kHz THROUGHPUT RATE WITH 8-BIT ACCURACY

DESCRIPTION

The SDM856 and SDM857 are complete data acquisition systems contained in a miniature 2.2" x 1.7" x 0.22" (55 x 43 x 5.6mm) ceramic package. These systems offer all the functions available in large modular data acquisition systems and are available with an optional internal instrumentation amplifier (SDM857). Inputs as low as ±50mV can be accepted by the SDM857; thermocouples, strain gages, and other low level signal sensors don't require external signal conditioning. Both models are fully expandable from the basic 16 channel single-ended or 8 channel differential input capability. Digital resolution is 12 bits with accuracy of ±0.024% at a throughput rate of 25kHz (SDM856KG).



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DISCUSSION OF PERFORMANCE

INTRODUCTION

SDM857 contains all components necessary to multiplex and convert analog signals as small as 0 to +50mV and as high as ±5V into equivalent digital outputs. Throughput sampling rates are from 18kHz (12 bit resolution) to 40kHz (8 bit resolution). A complete low drift instrumentation amplifier allows selection of gains from 2 to 1000 with one external resistor. SDM856 is identical to SDM857, but does not include the instrumentation amplifier. This provides the option of adding an external instrumentation amplifier for specific requirements such as high speed, digital programming, etc. Throughput sampling rates as high as 60kHz (8 bit resolution) can be obtained with the SDM856. Both models can be configured to accept either 8 channel differential or 16 channel single-ended signals and can be expanded almost without limit with external multiplexers. Three-state outputs are provided for easy interface to microprocessor systems. Figure 1 illustrates all system components.

ANALOG MULTIPLEXER

The analog multiplexer consists of two CMOS integrated circuits. Pin interconnects are used to select 16 channel single-ended or 8 channel differential operation. In single-ended operation the multiplexer can be used in a pseudo-differential mode by connecting the amplifier inverting input to common remote signal ground. Channel selection is made by an internally latched 3 or 4 bit binary word, for differential or single-ended operation respectively.

INSTRUMENTATION AMPLIFIER (SDM857 only)

Offering low drift and high accuracy, the internal instrumentation amplifier may be programmed by a single external resistor for gains from 2 to 1000. With gain programming pins open, the gain is two.

SAMPLE AND HOLD

A complete stand alone circuit, the sample and hold amplifier features buffered output, 10μsec acquisition time, and 100nsec aperture time.

Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions, such as automatic gain ranging, with no loss of aperture time.

ANALOG TO DIGITAL CONVERTER

The ADC is a 12-bit, 25μsec converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or two's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution.

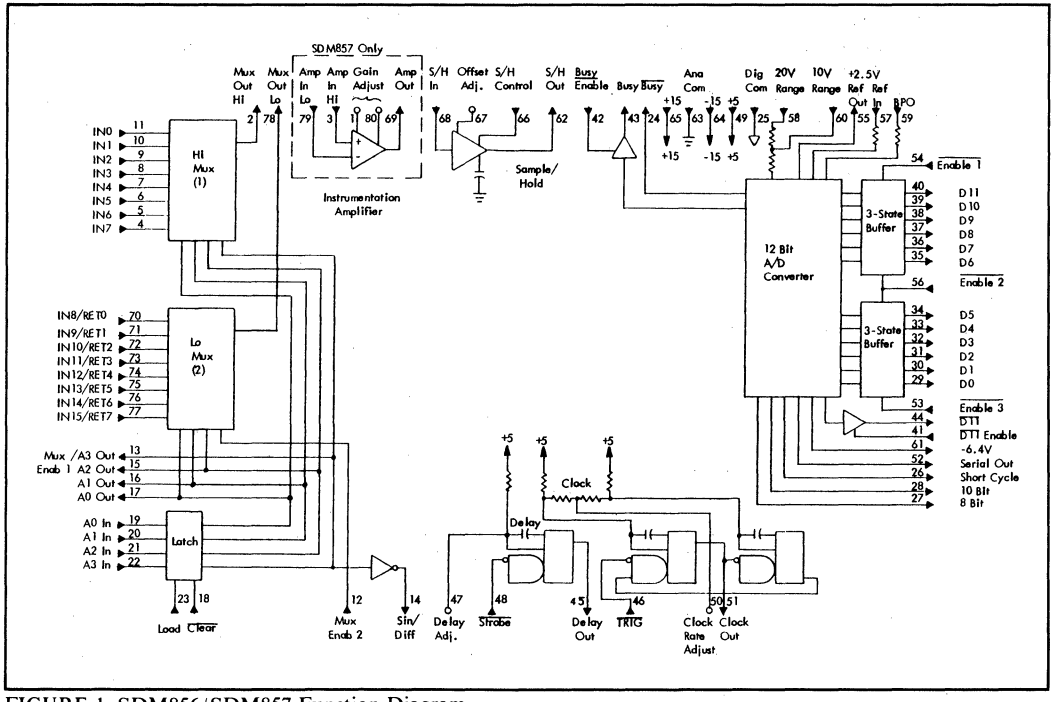


FIGURE 1. SDM856/SDM857 Function Diagram.

DISCUSSION OF PERFORMANCE (CONTINUED)

THREE-STATE OUTPUT BUFFERS

Digital outputs of the ADC are internally buffered by LSTTL three-state buffers. Three separate enable lines are brought out for easy interfacing to 4, 8 or 16 bit data buses. D11 (MSB) and BUSY are also buffered by separate three-state devices, each with its own enable line.

ADDRESS LATCH

Outputs of the 4-bit TTL register latch are connected to the address inputs of the multiplexer. This latch serves as an address storage register for the selected analog input. It may be loaded through 4 address inputs. Other inputs are LOAD and CLEAR. The 3 least significant bits are used for 8 channel differential mode addressing.

DELAY TIMER

A delay timer allows settling time for the multiplexer, amplifier and sample/hold circuits before conversion begins. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time of the instrumentation amplifier when operating at high gains, or shorter settling time for lower resolution operation.

CHANNEL EXPANSION

The number of analog input channels of the SDM856 and SDM857 can be easily increased by using Burr-Brown's MPC8D (8 channel differential) and MPC16S (16 channel single-ended) multiplexers. These are latch-free devices which contain internal binary decoding at TTL or MOS levels and may be integrated into a system with minimal external logic.

SYSTEM PERFORMANCE

SDM856 and SDM857 are configured for random channel selection. With the addition of an external counter they can be configured to a) continuously sequence through all analog channels or b) sequence through all analog channels on command from an external trigger.

With the appropriate 4-bit (single-ended) or 3-bit (differential) channel address on the latch inputs, and DELAY OUT, pin 45, tied to the LOAD input, pin 23, a negative going edge is applied to the STROBE input, pin 48. This starts the delay timer, latches the multiplexer address, and allows the input signal to pass through the multiplexer, instrumentation amplifier and sample/hold and settle to its final value before starting the A/D conversion. The DELAY OUT signal (pin 45) is also connected to the TRIG input (pin 46) and the A/D conversion is initiated on the negative-going edge. The S/H CONTROL input (pin 66) is connected to BUSY (pin 24) so that the sample/hold is in the HOLD mode during the A/D conversion.

By using overlap programming the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 29kHz for 12-bit and 67kHz for 8-bit resolution (ADC short-cycled). This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting BUSY to STROBE and S/H CONTROL and DELAY OUT to LOAD and TRIG. In this mode of operation the address of the next channel to be converted is latched and the output of the instrumentation amplifier allowed to settle to a new value during the present conversion.

SYSTEM TIMING DIAGRAMS

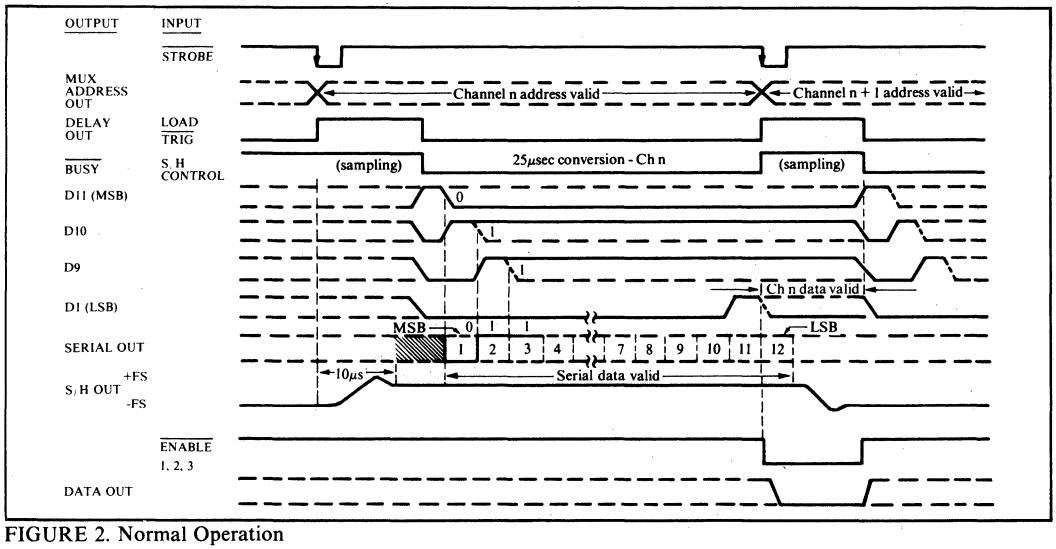


FIGURE 2. Normal Operation

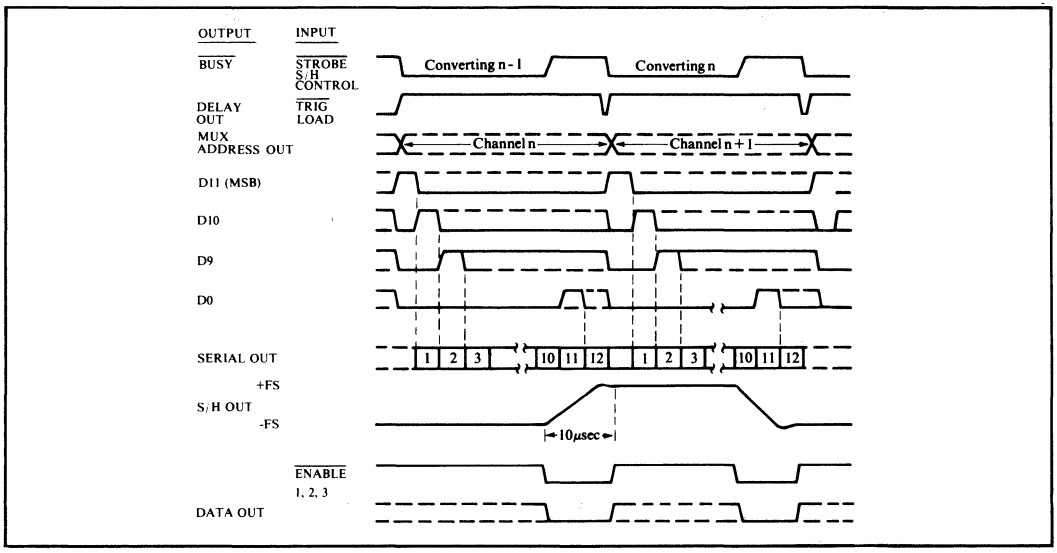


FIGURE 3. Overlap Operation

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	SDM856/SDM857			
TRANSFER CHARACTERISTICS	MIN	TYP	MAX	UNITS
Resolution	12			Bits
Number of Channels	16 single-ended/8 differential			
Throughput Rate				
SDM856JG	25			kHz
SDM856KG	25			kHz
SDM857JG	18			kHz
SDM857KG	18			kHz
ANALOG INPUTS				
ADC Gain Ranges		0 to +5, ±5, ±10		V
Input Voltage Range				
Absolute max without damage			±20	V
For linear operation			±6	V
Input Impedance, OFF Channel		5 x 10^9||10		Ω||pF
Input Impedance, ON Channel		5 x 10^9||100		Ω||pF
Amplifier Characteristics (SDM857 only)				
Gain Range	2		1000	
Gain Equation		G = 2 + 20kΩ/R_{EXT}[1]		
Input Bias Current at +25°C			±50	nA
0 to +70°C		±1.1		nA/°C
Offset Current at +25°C			±20	nA
0 to +70°C		±0.6		nA/°C
Input Offset Voltage		±0.1		mV
Input Offset Voltage Drift (G > 100)		±4		μV/°C
Output Noise (10Hz - 10kHz)				
G = 100, R_S = 500Ω		400		μVrms
Common-mode Rejection (DC) G = 2		90		dB
G = 1000		97		dB
Sample/Hold DC Characteristics				
Input Impedance		10^{10}		Ω
Bias Current		50		nA
Output Offset Voltage		7		mV
REFERENCE VOLTAGES				
Positive Output	+2.490	+2.500	+2.510	V
Positive Output Drift		±5		ppm/°C
Negative Output	-6.0	-6.4	-6.8	V
Negative Output Drift		±5		ppm/°C
ACCURACY				
Throughput Accuracy				
0 to +5V, ±5V ranges JG			±0.048	% of FSR[2]
0 to +5V, ±5V ranges KG			±0.024	% of FSR
0 to +50mV, ±50mV JG (SDM857 only)			±0.11	% of FSR
0 to +50mV, ±50mV KG (SDM857 only)			±0.08	% of FSR
Linearity (G = 1)				
JG			±0.024	% of FSR
KG			±0.012	% of FSR
Differential Linearity (G = 1)				
JG		±0.024		% of FSR
KG		±0.012		% of FSR
Quantizing Error			±0.012	% of FSR
System Gain Error[3]		±0.1		%
System Offset Error[3]		±0.1		% of FSR
Power Supply Sensitivity +15V		±0.0007		%/%ΔV
Power Supply Sensitivity -15V		±0.0007		%/%ΔV
Power Supply Sensitivity +5V		±0.001		%/%ΔV
TEMPERATURE STABILITY				
System Accuracy Drift[4] Unipolar			±25	ppm/°C
System Accuracy Drift[4] Bipolar			±20	ppm/°C
Linearity Drift			±2	ppm of FSR/°C
DYNAMIC ACCURACY				
Sample Hold Characteristics				
Aperture Time		100		nsec
Feedthrough (10V step)		±1.4		mV
Amplifier CMRR at 60Hz G = 2		90		dB
Amplifier CMRR at 60Hz G = 1000		95		dB
Amplifier Overload Recovery Time		200		μs
OUTPUTS				
Digital Output Coding		Binary, Offset Binary, Two's Complement		
Serial Output Coding		Non-return to zero (NRZ)		
ADC Conversion Time[5]		25	30	μsec
Clock Frequency[5]		520		kHz
Delay[6] SDM856		15		μsec
Delay[6] SDM857		30		μsec
POWER REQUIREMENTS				
Rated Voltage for Specified Accuracy	±14.5, +4.75	±15, +5	+15.5, +5.25	V
Quiescent Current				
SDM856 +15		+10		mA
SDM856 -15		-35		mA
SDM856 +5		+120		mA
SDM857 +15		+15		mA
SDM857 -15		-40		mA
SDM857 +5		+120		mA
Power Dissipation SDM856		1300		mW
Power Dissipation SDM857		1400		mW
ENVIRONMENTAL				
Specification Temperature Range	0		+70	°C
Storage Temperature Range	-25		+85	°C

TABLE I. Electrical Specifications

NOTES:
1. R_{EXT} is the external gain-setting resistor. (Connect between pins 1 and 80.)
2. FSR means Full Scale Range, e.g., FSR is 10V for ±5V range.
3. Adjustable to zero.
4. Includes gain, offset, and linearity drifts.
5. Conversion time and clock frequency can be externally adjusted between 13μsec (f = 1.0MHz) to 110μsec (f = 118kHz). (Conv. times are for 12-bit resolution.)
6. Can be externally adjusted from 3μsec to 300μsec.

DIGITAL INPUT SPECIFICATIONS

Address Inputs (A0 - A3)	One standard LSTTL load, positive true
Address Coding	4-bit binary
Load	One standard LSTTL load, positive true, address loaded on positive edge.
$\overline{\text{Clear}}$	One standard LSTTL load, negative true, low level clears latch.
$\overline{\text{Strobe}}$	One standard LSTTL load, high-to-low transition triggers the delay timer.
$\overline{\text{TRIG}}$	One standard LSTTL load, a negative going edge initiates the A/D conversion.
Short Cycle	One standard LSTTL load, logical 1 for 12-bit resolution connect to "8-bit" or "10-bit" for 8- or 10-bit resolution.
$\overline{\text{Enable 1}}$, $\overline{\text{Enable 2}}$, $\overline{\text{Enable 3}}$, $\overline{\text{D11 Enable}}$, $\overline{\text{Busy Enable}}$	One standard LSTTL load, a low level enables the 3-state output.
S/H Control	TTL compatible, 10μA maximum input current. Logic 0 = Hold mode, Logic 1 = Sample (track) mode.
Mux Enable 2	TTL compatible, 2μA input current, Logic 0 enables multiplexer 2 (channels 8-15).

DIGITAL OUTPUT SPECIFICATIONS

Parallel Data Outputs	5 standard TTL loads, positive true, 3-state.
Serial Output	2 standard TTL loads, positive true, NRZ, time serial data output beginning with D11 (see Timing Diagram).
$\overline{\text{D11}}$	5 standard TTL loads, positive true, 3-state.
$\overline{\text{Busy}}$	5 standard TTL loads, low during A/D conversion.
Busy	5 standard TTL loads, high during A/D conversion, 3-state
Clock Out	5 standard TTL loads, for synchronizing serial out data (see Timing Diagram).
Address Outputs (A0 - A3)	5 standard TTL loads, positive true
Delay Out	5 standard TTL loads, high during delay period, triggered by $\overline{\text{Strobe}}$ input.
Sin Diff	5 standard TTL loads, high while addressing channels 0-7, low while addressing channels 8-15.

TYPICAL PERFORMANCE CURVES

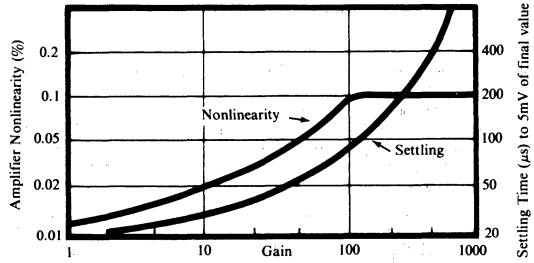


FIGURE 4. Nonlinearity and Settling Time vs. Amplifier Gain

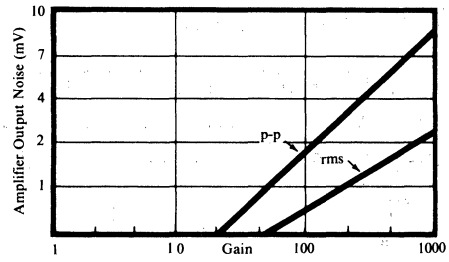


FIGURE 5. Output Noise vs. Amplifier Gain

THROUGHPUT ACCURACY AND TIMING RELATIONSHIPS

System Gain		System Accuracy		Throughput Rate (Channels/sec)		Delay Time (μsec)	
V/V		KG	JG	Normal	Overlap	Normal	Overlap
1	856 only	±0.024%	±0.048%	25k	29k	15	35
2	857 only	±0.024%	±0.048%	18k	29k	30	35
10	857 only	±0.035%	±0.06%	18k	29k	30	35
100	857 only	±0.08%	±0.11%	9k	11k	90	90
500	857 only	±0.1%	±0.15%	2.4k	2.6k	390	390

TABLE II. Throughput rate and delay time vs gain for normal and overlap modes.

Full Scale Input Range	ADC Range	Amplifier Gain	Resolution	Amplifier/Multiplexer Settling Time (μsec)		
				To ±0.2%	To ±0.05%	To ±0.01%
10V	-10 to +10	2	2.44mV*	8	10	20
1V	0 to +10	10	244μV	12	14	24
0.1V	0 to +10	100	24.4μV	65	80	90
20mV	0 to +10	500	4.88μV*	320	390	450

TABLE III. This table shows the delay timer setting required to allow for the settling time of the instrumentation amplifier to the accuracies specified.

*Depends on desired S/N ratio.

In overlap, when the Amplifier/Multiplexer settling time is less than the ADC conversion time, set the delay timer for the ADC conversion time plus the sample and hold acquisition time (10μs). When the Amplifier/Multiplexer settling time exceeds the ADC conversion time plus the S/H acquisition time, set the delay timer for the Amplifier/Multiplexer settling time.

CONNECTION DIAGRAM

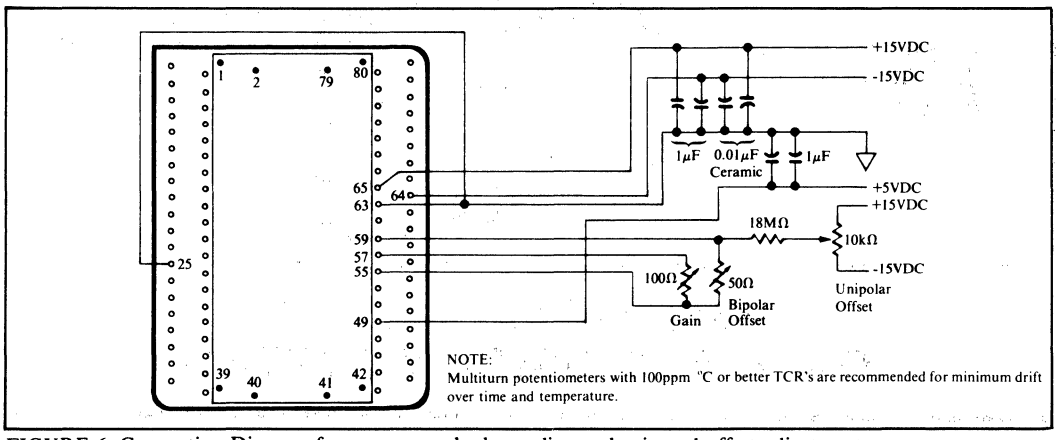


FIGURE 6. Connection Diagram for power supply decoupling and gain and offset adjustment.

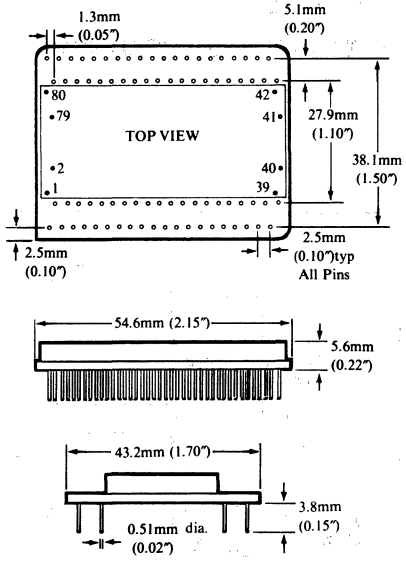
PACKAGE AND PIN CONFIGURATION

PIN CONNECTIONS

Pin		Pin	
*1	IA Gain Adjust	41	DI1 Enable
2	Mux Out High	42	Busy Enable
*3	Amp In High	43	Busy
4	CH7	44	DI1
5	CH6	45	Delay Out
6	CH5	46	TRIG
7	CH4	47	Delay Adjust
8	CH3	48	Strobe
9	CH2	49	+5V Supply
10	CH1	50	Clock Rate Adjust
11	CH0	51	Clock Out
12	Mux Enable 2	52	Serial Out
13	A3 Out	53	Enable 3
14	Single/Differential	54	Enable 1
15	A2 Out	55	+2.5V Ref Out
16	A1 Out	56	Enable 2
17	A0 Out	57	+2.5V Ref In
18	Clear	58	20V Range
19	A0 In	59	BPO
20	A1 In	60	10V Range
21	A2 In	61	-6.4 Ref Out
22	A3 In	62	S/H Out
23	Load	63	Analog Common
24	Busy	64	-15V Supply
25	Dig. Common	65	+15V Supply
26	Short Cycle	66	S/H Control
27	10-bit Resolution	67	S/H Offset Adjust
28	8-bit Resolution	68	S/H Input
29	D0 (LSB)	*69	IA Out
30	D1	70	CH8/RET0
31	D2	71	CH9/RET1
32	D3	72	CH10/RET2
33	D4	73	CH11/RET3
34	D5	74	CH12/RET4
35	D6	75	CH13/RET5
36	D7	76	CH14/RET6
37	D8	77	CH15/RET7
38	D9	78	Mux Out Low
39	D10	*79	Amp In Low
40	D11 (MSB)	*80	IA Gain Adjust

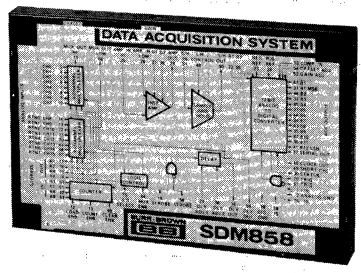
*For SDM857 only. Make no connection in SDM856.

MECHANICAL SPECIFICATIONS



MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz.)
PINS: Pin material and plating composition comform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)
MATING CONNECTOR: 2350MC (Set of four 20 pin strips)

BURR-BROWN®



SDM858

Low-Level Input, 12-Bit DATA ACQUISITION SYSTEM

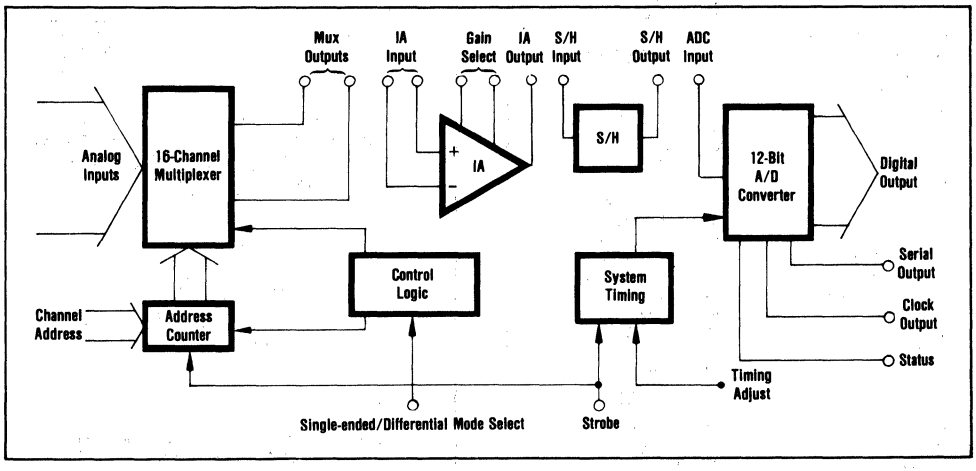
FEATURES

- HIGH ACCURACY WITH LOW LEVEL INPUT SIGNALS
- LOW COST
- SAVES DESIGN TIME
- RELIABLE - 70°C BAKE FOR 160 HOURS
- SAVES SPACE
- FLEXIBLE - FOUR MODES OF OPERATION

DESCRIPTION

The SDM858 is a complete 8- or 16-channel data acquisition system in a compact 4.6" x 3.0" x 0.375" metal case. This system is specifically designed to give high accuracy with low level analog input signals. A built-in high quality instrumentation amplifier allows input signal ranges of ±5mV to ±10V. It is especially useful with thermocouple and strain gage inputs since it yields only ±0.025% (of Full Scale Range) error at a gain of 100.

This expandable module accepts either 16 single-ended or 8 differential inputs and converts the multiplexed data signals into 12-bit digital words with an accuracy of ±0.025% at throughput rates of up to 8000 samples per second.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SYSTEM DESCRIPTION

The SDM858 contains all the components necessary to multiplex and convert ±5mV to ±10V analog data into equivalent digital outputs yielding resolutions of 2.4μV to 4.88mV. It has been designed specifically to acquire and convert low level signals. The throughput sampling rate is 8kHz for 12-bit resolution at a gain of 10. This system contains an analog multiplexer (which can be connected for 16-channel single-ended or 8-channel differential signals), instrumentation amplifier, sample/hold circuit, 12-bit successive approximation A/D converter, and control and timing logic. The amplifier and sample/hold are not internally connected, allowing maximum application flexibility. These systems can be expanded almost without limit using Burr-Brown's MPC16S, MPC8D, MPC8S, and MPC4D monolithic multiplexers. The SDM858 is designed to be mounted on a printed circuit card. The only requirements for system operation are input signals, power, and the interconnection of system components into the desired operating configuration. The components of the SDM858 are shown in Figure 1 and described in the following paragraphs.

ANALOG MULTIPLEXER

Two, one-of-eight, CMOS analog multiplexers are used to allow user selection (by external jumpers) of 16 single-ended channel or 8 differential channel operation. In 16-channel operation the multiplexer may be used in a pseudo-differential mode by connecting the amplifier inverting input to a common, remote, signal ground. Channel selection is by a 3- or 4-bit binary word stored in a presettable address counter.

INSTRUMENTATION AMPLIFIER

The SDM858 instrumentation amplifier has been optimized for low drift and high accuracy with analog inputs as low as ±5mV full scale. Input noise and thermal feedback have been minimized to improve accuracy when amplifying such signals as thermocouple and strain gage outputs. The gain is programmed with an external resistor connected between pins 26 and 27. Gain may be selected from 1 to 2000.

The amplifier used in the SDM858 is the Burr-Brown Model 3630. More information is available in the 3630 product data sheet.

SAMPLE/HOLD

The sample/hold circuit is a complete monolithic unit featuring buffered output and maximum acquisition and aperture times of 52μsec and 200nsec. Input, output, and mode control functions are brought to separate connector pins. This allows maximum system flexibility for performing such functions as automatic gain ranging with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a ceramic-packaged, 12-bit converter featuring 24μsec conversion time and 0.01% accuracy. Stable thin-film networks and current switching are used to assure linearity over wide temperature ranges.

ADDRESS COUNTER

A 4-bit binary address counter is connected to the multiplexer. This counter may be externally loaded, cleared, clocked, or enabled. The address outputs are brought to connector pins for convenient system control.

DELAY TIMER

The delay timer is provided to allow for the settling time of the multiplexer, amplifier, and sample/hold circuits prior to start of conversion. The delay time is adjustable over a wide range by an external potentiometer and/or external capacitor. This allows for the longer settling time of the instrumentation amplifier at high gains. The timer is adjusted at the factory for optimum operation at a gain of 100.

CONTROL LOGIC

Delay and ADC trigger functions are edge-triggered and gated. Counter control functions are synchronous with the counter clock which is internally connected to the delay timer output.

CHANNEL EXPANSION

The number of analog input channels of these systems can easily be increased using Burr-Brown's CMOS multiplexers. These latch-free devices contain internal binary decoding, TTL or MOS logic levels, and may be integrated into a system with minimum external logic. The following devices offer a variety of input channel configurations.

MPC4D	4-channel differential
MPC8D	8-channel differential
MPC8S	8-channel single-ended
MPC16S	16-channel single-ended

SYSTEM PERFORMANCE

The SDM858 can be configured to continuously sequence through all analog channels, to accept random addresses or to sequence through all analog channels on command from an external trigger.

The STATUS signal, pin 30, is connected to the $\overline{\text{STROBE}}$ input of the delay timer, pin 58, for normal program sequencing with a minimum throughput sampling rate of 2kHz for 12-bit resolution and a gain of 100. A throughput rate of 8kHz with 12-bit resolution can be achieved for a gain of 10 by decreasing the delay time.

By using "overlap" programming, the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced slightly. Overlap programming is accomplished by connecting the STATUS signal, pin 30, to the STROBE input of the delay timer, pin 19, and extending the delay time. The internal logic will then select analog channel (n + 1) while channel n is being converted.

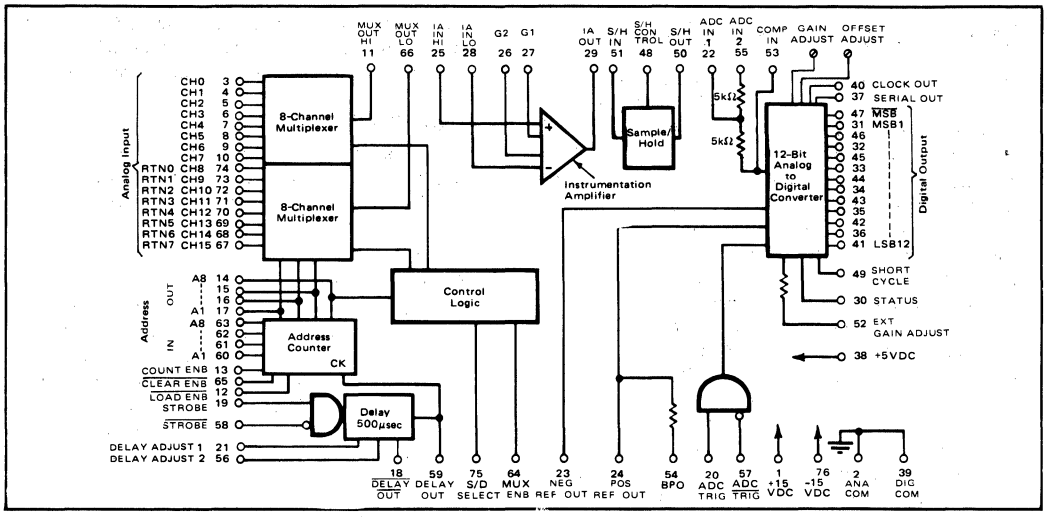


FIGURE 1. Detailed Block Diagram of SDM858.

SPECIFICATIONS

ELECTRICAL	
Typical at +25°C with ±15VDC and +5VDC power supplies unless otherwise noted.	
MODEL	SDM858
TRANSFER CHARACTERISTICS	
Throughput Rate, min	
G = 1	8kHz, 125µsec/channel
G = 100	2kHz, 500µsec/channel
G = 1000	1kHz, 1msec/channel
G = 2000	500Hz, 2msec/channel
Resolution	12 bits
Number of Channels	16 single-ended or pseudo-differential/8 differential
ANALOG INPUTS	
ADC Voltage Input Ranges	0 to +5V, 0 to +10V, ±2.5V, ±5V, ±10V
Amplifier Gain Range	1 to 2000
Amplifier Gain Equation	$G = 1 + (40k\Omega/R_{EXT})$[1]
Max. Input Voltage without Damage	±16V
Max. Input Voltage for Multiplexer Operation	±10.24V
Common-Mode Input Voltage, max	
G = 1	±10V
G > 1	±5V
Input Impedance	100MΩ, 10pF OFF channel 100MΩ, 100pF ON channel[2]
Bias Current	
+25°C	±10nA, typ; ±30nA, max
0°C to +70°C	±20nA, typ; ±60nA, max
Differential Bias Current	±10nA, typ; ±30nA, max
Differential Bias Current Drift	±0.4nA/°C typ; ±1.0nA/°C, max
Amplifier Input Offset Voltage, max	±25 ±(200/G)µV
Amplifier Voltage Offset Drift, max	±0.75 ±(10/G)µV °C
vs Supply, max	±2 ±(200/G)µV V
vs Time	±2 ±(40/G)µV mo
Amplifier Input Noise	
Voltage	
0.01Hz to 10Hz	1.2µV, p-p
10Hz to 1kHz	1.0µV, rms
Current	
0.01Hz to 10Hz	70pA, p-p
10Hz to 1kHz	20pA, rms
Amplifier Output Noise (G = 100, R_S = 500Ω)	
0.01Hz to 10Hz	0.12mV, p-p
10Hz to 10kHz	0.32mV, rms
Thermal Feedback[3]	0.1µV V_{Input}
Channel-to-Channel Input Voltage Error[4]	±5µV

ACCURACY[5]	
System Accuracy, max (Gain = 100)	±0.025% FSR[6] at 2kHz throughput rate
Linearity	±[1/2 + (G/2400)] LSB
Differential Linearity (Gain = 100)	±1/2LSB at 2kHz throughput rate
Quantizing Error	±1/2LSB
Gain Error	Adjustable to zero
Offset Error	Adjustable to zero
Power Supply Sensitivity	±0.005% FSR/% change of supply voltage
STABILITY OVER TEMPERATURE	
System Offset Drift, max ($Z_{IN} \leq 400\Omega$)	
G = 1	±5ppm of FSR/°C
G = 10	±7ppm of FSR/°C
G = 100	±30ppm of FSR/°C
G = 1000	±300ppm of FSR/°C
G = 2000	±600ppm of FSR/°C
System Gain Drift,[7] max	
G = 1	±35ppm of reading/°C
G = 10	±80ppm of reading/°C
G = 100	±85ppm of reading/°C
G = 2000	±85ppm of reading/°C
ADC Offset Drift (Unipolar)	±3ppm of FSR/°C
ADC Offset Drift (Bipolar)	±15ppm of FSR/°C
ADC Linearity Drift	±3ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	125nsec, typ; 200nsec, max
Sample/Hold Acquisition Time (to 0.025%)	26μsec, typ; 52μsec, max
Error for Full Scale Transition Between Successively Addressed Channels	
G = 1	±1LSB at 8kHz
G = 100	±1LSB at 2kHz
G = 1000	±2LSB at 1kHz
G = 2000	±4LSB at 500Hz
Amplifier CMRR, min; 1kΩ Source Imbalance	
G = 1, f = 60Hz	86dB
G = 1, f = 1kHz	70dB
G = 10, f = 60Hz	96dB
G ≥ 100, f = 60Hz	100dB
Channel Cross Talk	-80dB at 2kHz, OFF channel to ON channel
Sample/Hold Feedthrough	±0.007% of 20V
Sample/Hold Decay Rate, (+70°C)	1μV/μsec, typ; 10μV/μsec, max
OUTPUT	
Output Coding (Complementary)	Unipolar straight binary, bipolar offset binary, binary two's complement
Gain Error[8]	Adjustable to zero
Offset Error[8]	Adjustable to zero
A/D Conversion Time	24μsec typ, 30μsec max
Delay	470μsec nominal, externally adjustable[9]
POWER REQUIREMENTS	+15VDC ±3% at +65mA, ripple < 5mV, rms -15VDC ±3% at -75mA, ripple < 5mV, rms +5VDC ±5% at 300mA, ripple < 25mV, rms
ENVIRONMENTAL	
Operating Temperature	0°C to 70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	95% noncondensing

NOTES:
1. With R_{EXT} between pins 26 and 27.
2. With multiplexer output connected to 1A input.
3. Drift due to internal heating.
4. Error due to thermoelectric effects of dissimilar metal junctions.
5. No missing codes guaranteed.
6. FSR means full scale range.
7. Exclusive of gain resistor drift.
8. Gain and offset controls are located in the module. The adjustment ranges are ±0.1% FSR for gain and ±0.1% FSR for offset.
9. Adjustable to 10 seconds with external capacitor, to 50μsec with an external resistor.

DIGITAL INPUT

Address inputs	One standard TTL load, positive true
LOAD ENABLE	One standard TTL load, negative true, address loaded with strobe inputs.
CLEAR ENABLE	One standard TTL load, negative true, address cleared with strobe inputs.
STROBE & $\overline{\text{STROBE}}$	One standard TTL load, STROBE and $\overline{\text{STROBE}}$ edge trigger the delay timer and clock the address counter. STROBE must be high to enable $\overline{\text{STROBE}}$ and $\overline{\text{STROBE}}$ must be low to enable STROBE.
COUNT ENABLE	Two standard TTL loads, positive true, logic "0" allows the Strobe inputs to trigger the delay timer, but prevents the MUX address counter from being clocked.
ADC TRIGGER	One standard TTL load, a positive going edge at TRIG initiates conversion, a negative going edge at $\overline{\text{TRIG}}$ initiates conversion; $\overline{\text{TRIG}}$ must be "0" to enable TRIG; TRIG must be "1" to enable $\overline{\text{TRIG}}$.
SHORT CYCLE	One standard TTL load, logic "1" for 12-bit resolution, connected to the N + 1 bit output for N bit resolution.
MULTIPLEXER ENABLE	Two standard TTL loads, logic "1" enables multiplexer output and logic "0" turns off all channels.
MULTIPLEXER ENABLE	Two standard TTL loads, logic "1" enables 16-channel single-ended operation and logic "0" enables 8-channel differential operation.
S D SELECT	

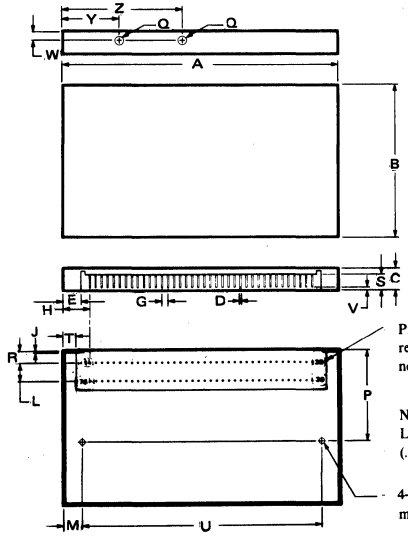
DIGITAL OUTPUT

Data outputs	
Parallel B1, B1 . . . B12	2 Standard TTL loads, negative true.
SERIAL OUT	2 Standard TTL loads, negative true, time serial data output beginning with B1.
Address outputs	5 Standard TTL loads, positive true, 4-bit binary code, internal 2kΩ pull-up resistors.
DELAY OUT and $\overline{\text{DELAY OUT}}$	5 Standard TTL loads high (low) during the delay period, triggered by $\overline{\text{STROBE}}$ and STROBE inputs.
CLOCK OUT	5 Standard TTL loads for synchronizing serial out data.
STATUS	5 Standard TTL loads, high during the A D converison.

PIN DESIGNATIONS

+15VDC	1	76	-15VDC
ANA COM	2	75	S/D SELECT
CH0 IN	3	74	CH8 IN (RTN0)
CH1 IN	4	73	CH9 IN (RTN1)
CH2 IN	5	72	CH10 (RTN2)
CH3 IN	6	71	CH11 IN (RTN3)
CH4 IN	7	70	CH12 IN (RTN4)
CH5 IN	8	69	CH13 IN (RTN5)
CH6 IN	9	68	CH14 IN (RTN6)
CH7 IN	10	67	CH15 IN (RTN7)
$\overline{\text{MUX OUT HI}}$	11	66	MUX OUT LO
LOAD ENABLE	12	65	$\overline{\text{CLEAR ENABLE}}$
COUNT ENABLE	13	64	MUX ENABLE
A8 OUT	14	63	A8 IN
A4 OUT	15	62	A4 IN
A2 OUT	16	61	A2 IN
$\overline{\text{A1 OUT}}$	17	60	A1 IN
DELAY OUT	18	59	$\overline{\text{DELAY OUT}}$
STROBE	19	58	$\overline{\text{STROBE}}$
ADC TRIG	20	57	ADC TRIG
DELAY ADJUST 1	21	56	DELAY ADJUST 2
R1	22	55	R2
NEG REF OUT	23	54	BPO
POS REF OUT	24	53	COMP IN
IA IN HI	25	52	GAIN ADJUST
G2	26	51	S/H IN
G1	27	50	S/H OUT
IA IN LO	28	49	SHORT CYCLE
IA OUT	29	48	S/H CONTROL
STATUS	30	47	$\overline{\text{B1 (MSB)}}$
B1 MSB	31	46	B2
B3	32	45	B4
B5	33	44	B6
B7	34	43	B8
B9	35	42	B10
B11	36	41	B12 LSB
SERIAL OUT	37	40	CLOCK OUT
+5VDC	38	39	DIG COM

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	4.580	4.620	116.33	117.35
B	2.980	3.020	75.69	76.71
C	.350	.380	8.89	9.65
D	.018	.021	0.46	0.53
E	.280	.320	7.11	8.13
G	.100 BASIC		2.54 BASIC	
H	.420	.480	10.67	12.19
J	.017	.023	0.43	0.58
L	.300 BASIC		7.62 BASIC	
M	.270	.330	6.85	8.38
P	1.480	1.520	37.59	38.61
Q	.130	.170	3.30	4.32
R	.170	.230	4.32	5.84
S	.235	.285	5.97	7.24
T	.170	.260	4.32	6.60
U	3.980	4.020	101.09	102.11
V	.030	.070	0.76	1.78
W	.130	.180	3.30	4.57
Y	.930	.970	23.62	24.64
Z	1.980	2.020	50.29	51.31

Pin numbers shown for reference only. Numbers may not be marked on package.

NOTE:
Leads in true position within .015" (.38mm)R at MMC at seating plane.

4-40 thread, 190" (4.83mm) min. depth, 2 places.

CASE MATERIAL: Insulated Steel
CONNECTOR PINS: Gold Flashed
WEIGHT: 145 grams (5 oz.)

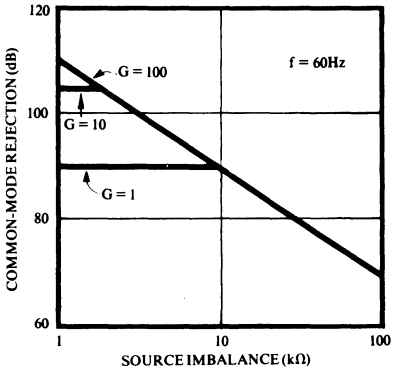
MOUNTING INSTRUCTIONS:
(Mounting flush on PC Card.)

1. Use strip connectors or two 14-pin and three 16-pin low profile IC sockets (shipped with each unit).

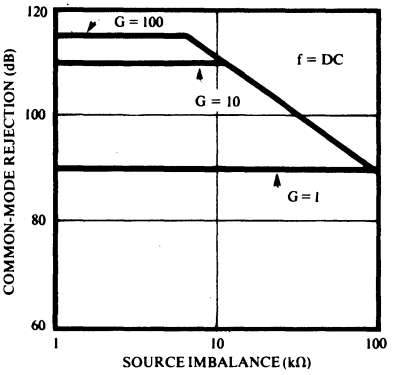
2. Use 4-40 x 3/16" (4.8mm) LG Pan HD Hardware to secure the SDM858 to PC Card.

TYPICAL PERFORMANCE CURVES

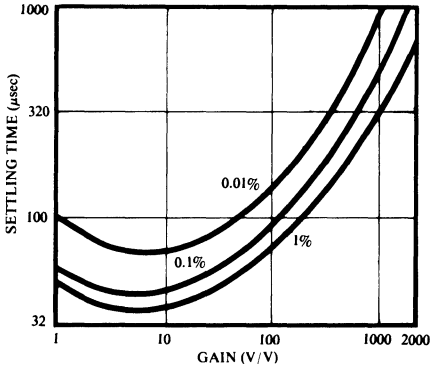
AMPLIFIER COMMON-MODE REJECTION VS SOURCE IMPEDANCE IMBALANCE



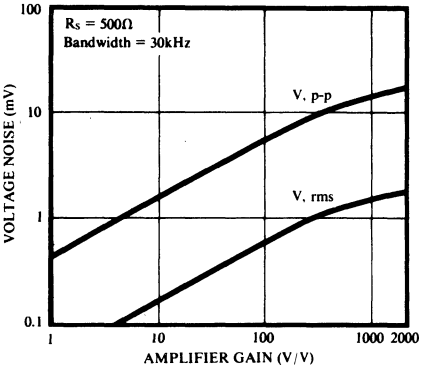
AMPLIFIER COMMON-MODE REJECTION VS SOURCE IMPEDANCE IMBALANCE



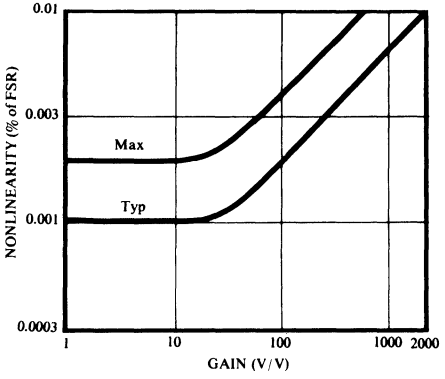
AMPLIFIER SETTLING TIME VS GAIN



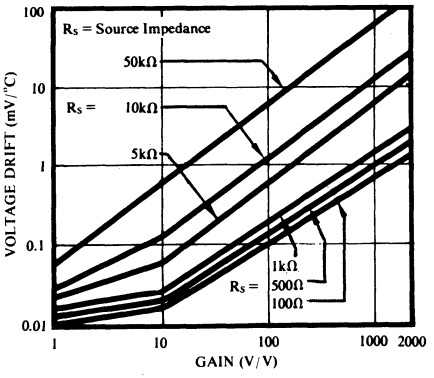
SYSTEM NOISE VS AMPLIFIER GAIN



AMPLIFIER NONLINEARITY VS GAIN



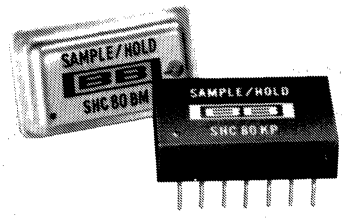
AMPLIFIER OUTPUT OFFSET VOLTAGE DRIFT VS GAIN



SDM858

BURR-BROWN®

SHC80



Fast IC SAMPLE/HOLD AMPLIFIERS

FEATURES

- 14-PIN DIP PACKAGE
- 10μsec ACQUISITION TIME
- COMPLETE WITH HOLDING CAPACITOR
- ±0.01% ACCURACY
- -25°C TO +85°C TEMPERATURE RANGE (SHC80BM)

DESCRIPTION

Ultra-linear performance and fast acquisition speeds - that's the combination that makes the SHC80 models ideal for your demanding data acquisition and control applications.

The SHC80 acquires and holds up to ±10V analog signals to an accuracy of ±0.01% of full scale. Acquisition time is 12μsec for a 20V step of 10μsec for a 10V step. High performance results from the use of internally compensated circuits normally found only in larger, more expensive sample/holds.

Two models give you a choice of operating temperature range: the SHC80KP (0°C to +70°C) in an epoxy package, also the SHC80BM (-25°C to +85°C) in a hermetic metal case. You'll find these units well suited for:

Data Acquisition Systems
Data Distribution Systems
Analog Delay Circuits
Pulse Amplitude Modulation Circuits
Waveform Amplitude Measurement

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PDS-348 Printed in U.S.A. July, 1978

SPECIFICATIONS

Typical at 25°C with rated supply and 1000pF internal capacitor unless otherwise noted.

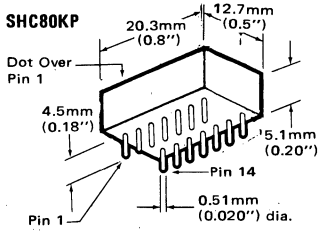
ELECTRICAL

MODELS	SHC80KP	SHC80BM	Units
INPUT			
ANALOG INPUT			
Voltage Range	±10	±10	V
Maximum Safe Input Signal	±15	±15	V
Impedance	$10^8 \parallel 5$	$10^8 \parallel 5$	Ω/pF
Bias Current	400	400	nA
DIGITAL INPUT			
(TTL/MOS Compatible)	Voltage +5V	Voltage +15V	current
Mode Control	Logic Supply	Logic Supply	
"Sample" - Logic "1"	2 < e < 8V	5.5 < e < 15V	+50nA
"Hold" - Logic "0"	0 < e < 0.8V	0 < e < 3.5V	-50μA
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Dynamic Nonlinearity (max)	±0.01(3)	±0.01	% of 20V
@ min "Hold" time	1000	1000	μs
Gain	+1.0	+1.0	V/V
Gain Error	0.01	0.01	% of 20V
Throughput Offset (max) (adj. to zero)	2	2	mV
Droop Rate (max)	0.5	0.5	mV/mS
Droop Rate (typ)	0.2	0.2	mV/mS
Throughput Nonlinearity	±0.005	±0.005	% of 20V
Noise (RMS) (10Hz to 100kHz)	100	100	μV RMS
Supply Rejection (0 to 50kHz)	200	200	μV/V
ACCURACY DRIFT			
Gain Drift	2	2	ppm of 20V/°C
Offset Drift	20	20	μV/°C
Droop Rate(1)			
@ 70°C (max)	10	10	mV/mS
@ 85°C (max)	–	25	mV/mS
DYNAMIC CHARACTERISTICS			
Full Power Bandwidth(2)	75	75	kHz
Output Slew Rate	5	5	V/μs
Aperature Time	40	40	ns
Aperature Time Jitter	1	1	ns
Acquisition Time to 0.01%			
10V Step (max)	10	10	μs
20V Step (max)	12	12	μs
Feedthrough in Hold Mode	±0.02	±0.005	% of Input Step
Charge Offset (max)	2	2	mV
Sample to Hold Transient			
Peak Amplitude	150	150	mV
Settling to 1mV	1	1	μs
OUTPUT			
ANALOG OUTPUT			
Voltage Range (min)	±10	±10	V
Current Range (min)	±5	±5	mA
Impedance	0.5	0.5	Ω
TEMPERATURE			
Specification	0 to +70	-25 to +85	°C
Storage	-25 to +85	-55 to +125	°C
POWER SUPPLY			
Rated Voltage	±15	±15	V
Range	±14.5 to ±15.5	±14.5 to ±15.5	V
Current	±20	±20	mA
LOGIC SUPPLY			
Rated Voltage	+5	+5	V
Range	+4.75 to +15.5	+4.75 to +15.5	V
Current	1	1	mA

(1) May double every 10°C over temperature. (2) Small signal bandwidth 750kHz.
(3) ±0.015 including feedthrough for SHC80KP.

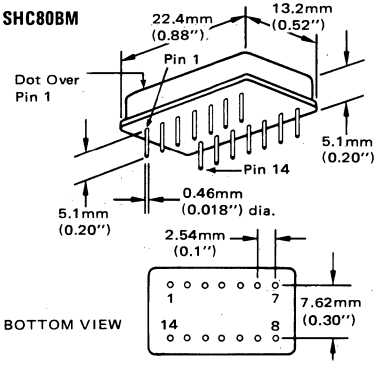
MECHANICAL

EPOXY PACKAGE



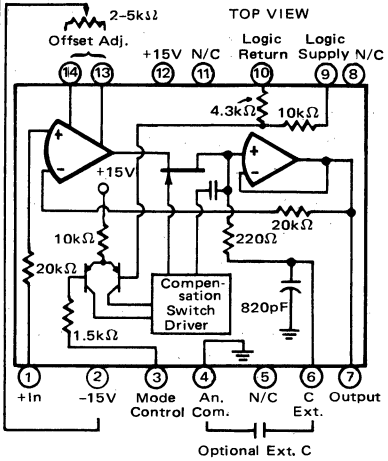
Pin Spacing: 2.54mm (0.1")
Row Spacing: 7.62mm (0.30")
Mating Connector: 145MC

METAL PACKAGE



Case: Metal
Pin Material and plating Composition conform to Method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

Connection Diagram



Note: No connection should be made to pins 11 & 5. Pin 8 is not internally connected.

SHC80

DEFINITION OF SPECIFICATIONS

DYNAMIC NONLINEARITY

This is the total nonadjustable input-to-output error. It includes errors due to throughput nonlinearity, droop, thermal transients and feedthrough; in short, all errors that cannot be adjusted to zero for a 10 volt input change after a 10μsec acquisition time and a one millisecond hold time. Offset errors may be adjusted to zero by the offset control, but gain errors must be removed by a gain adjustment elsewhere in the system. (Gain adjust not included in SHC80.)

GAIN ACCURACY

The difference due to amplifier gain errors between INPUT and OUTPUT voltage when in the "sample" mode.

DROOP RATE

The voltage decay at the output during the "hold" mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

The amount of input voltage change that appears at the output when the amplifier is in the "hold" mode.

THROUGHPUT – NONLINEARITY

The total charge offset and gain nonlinearity, i.e., the inaccuracy due to these two errors that cannot be corrected by gain and offset adjustments. Throughput – nonlinearity is specified over the 20 volt input range.

THROUGHPUT OFFSET

The sum of sample offset and charge offset.

CHARGE OFFSET

The offset that results from charge transferred from the holding capacitor to the gate capacitance of the switching FET. This charge is partially restored by a special compensation circuit when the unit goes into the "hold" mode.

ACQUISITION TIME

The time required for the output to settle to its final value within a given error band when the Mode control is switched from "hold" to "sample". See Figure 2.

APERTURE TIME

The time required to switch from "sample" to "hold". It is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

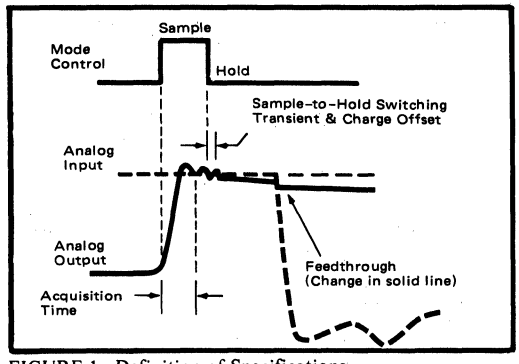


FIGURE 1. Definition of Specifications.

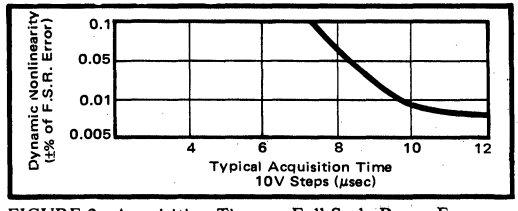


FIGURE 2. Acquisition Time vs. Full Scale Range Error.

OPERATING INSTRUCTIONS

OPTIONAL EXTERNAL CAPACITOR SELECTION

The value of the external capacitor determines the droop, charge offset, and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table.

Figure 3 shows the behavior of acquisition time with added external capacitance. The behavior of droop with external C is determined by:

$$\text{Droop} = \frac{dv}{dt} = \left(\frac{0.5 \times 10^{-9}}{800\ \text{pF} + C_{ext}\ \text{pF}}\right) \frac{\text{mV}}{\text{mS}}$$

Capacitors with high insulation resistance and low dielectric absorption, such as teflon or polystyrene should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor to minimize droop errors.

OFFSET ADJUSTMENT

Connect a 2k ohm to 5k ohm multi-turn potentiometer with a max TCR or 150 ppm/°C as shown in the Connection Diagram, and adjust the offset with the input grounded. During the adjustment, the sample/hold should be switching continuously between the "sample" and the "hold" mode. Adjust the error to zero when the unit is in the "hold" mode. This procedure insures that charge offset as well as amplifier offset error will be removed.

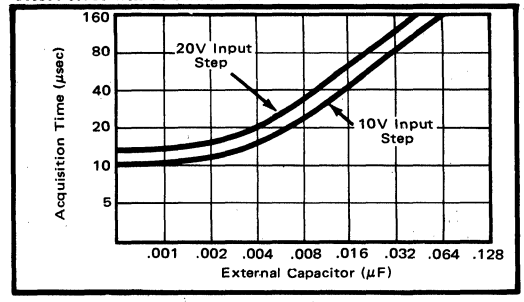


FIGURE 3. Acquisition Time vs. External Capacitor.

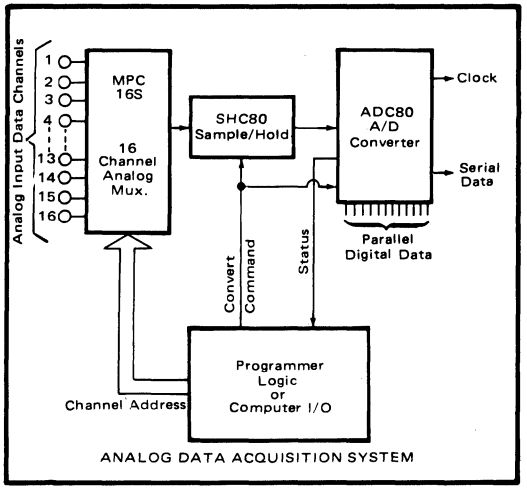
LOGIC THRESHOLD PROGRAMMING

Pin 10 is normally connected to the logic return and pin 9 to a positive logic supply. The logic threshold is determined by the 4.3kΩ and 10kΩ resistors shown in the connection diagram. The threshold is 1.5V for logic operated on a +5V supply and 4.5V for a +15V logic supply. If it is not convenient to connect a logic return and supply to the SHC80, pin 10 may be connected to the analog return and pin 9 to +15V for 15V logic or to +15V, through a 27kΩ resistor for 5V logic. The mode control switching transistors have sufficient current gain to allow the mode control pin to be driven from MOS logic. The mode control polarity may be reversed by connecting an externally-derived threshold voltage to pin 3 and by connecting pins 9 and 10 to the mode control source.

APPLICATIONS

DATA ACQUISITION SYSTEM

The SHC80 makes an excellent device for reducing aperture time and eliminating conversion noise from high gain circuitry in data acquisition systems. When it is combined with Burr-Brown's 16 channel MPC-16S Analog Multiplexer and ADC80 A/D Converter, you have a compact 16 channel data acquisition system with 25 kHz throughput sampling rates and ±0.02% (RSS) system accuracy.



ANALOG DATA ACQUISITION SYSTEM

SIMULTANEOUS SAMPLE/HOLD

Time correlation of sampled data signals may be implemented by using one sample/hold for each analog signal prior to input to an analog multiplexer. The SHC80's low aperture time of 40 nanoseconds practically eliminates channel-to-channel time slew. The throughput sampling rate and the number of data channels will determine the maximum "hold" time and hence, the worst case droop error of the sample/hold in the last channel to be sampled prior to the next "refresh" or sample/hold command. This droop error may be minimized by adding external capacitance to the SHC80 as shown in Figure 3.

The droop error is computed by:

MAX DROOP ERROR (CHANNEL N) = (T x n)(Droop rate)

Where $T = \frac{1}{\text{System Sampling Rate}}$ and

n = number of multiplexer data channels.

EXAMPLE:

For a 10 bit, 32 channel system with throughput sample rate of 25 kHz, assuming no external capacitance, the droop error of channel N is:

Droop Error $(E_D) = (\frac{1}{25k} \times 32)(500 \times 10^{-3}) = 640\mu V$.

For ±10 volt input signal range and 10-bit resolution, the resolution of ±½ LSB is ±9.77 mV. This droop error is less than 0.032 LSB (negligible), and no external C is needed to reduce the droop of the SHC80.

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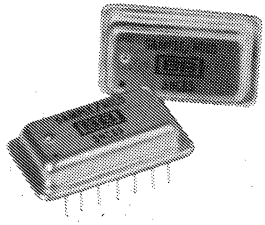


SHC85
SHC85ET

Fast IC
SAMPLE/HOLD AMPLIFIERS

FEATURES

- 14-PIN DIP PACKAGE
- 5μsec ACQUISITION TIME
- COMPLETE WITH HOLDING CAPACITOR
- ±0.01% ACCURACY
- -55°C TO +125°C TEMPERATURE RANGE (SHC85ET)

DESCRIPTION

The SHC85 is designed to acquire and hold up to ±10VDC analog signals to an accuracy of ±0.01% of full scale range in 5μsec for a 20-volt step or 4.5μsec for a 10VDC step. Featuring internally compensated circuits normally found only in more expensive and larger sample/holds, the SHC85 offers ultra-liner performance and fast acquisition speeds for the most demanding data acquisition and control applications.

Two models are available: the SHC85 is specified for 0°C to 70°C operation, and the SHC85ET is specified for -55°C to +125°C operation.

The SHC85/SHC85ET are well suited for use in:

Data Acquisition Systems
Data Distribution Systems
Analog Delay Circuits
Pulse Amplitude Modulation Circuits
Waveform Amplitude Measurement

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-321

SPECIFICATIONS

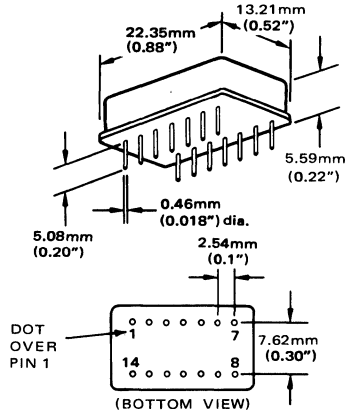
Typical at 25°C with rated supply and a 1000 pF internal capacitor unless otherwise noted.

ELECTRICAL

MODELS	SHC85	SHC85ET	UNITS
INPUT			
ANALOG INPUT			
Voltage Range	±10	±10	V
Maximum Safe Input Signal	±15	±15	V
Resistance	10^8	10^8	Ω
Bias Current	50	50	nA
DIGITAL INPUT (TTL Compatible)			
Mode Control	Voltage	Current	
"Sample" - Logic "1"	+2.0V < e < +8V	50 nA	
"Hold" - Logic "0"	0V < e < +0.8V	-50 μA	
TRANSFER CHARACTERISTICS			
ACCURACY (25°C)			
Dynamic Nonlinearity (max)	±0.01	±0.01	% of 20V
@ min. "Hold" Time	1000	1000	μs
Gain	+1.0	+1.0	V/V
Gain Error	±0.01	±0.01	% of 20V
Throughput Offset (max)(adj to zero)	2	2	mV
Droop Rate (max)	0.5	0.5	mV/ms
Droop Rate (typical)	0.125	0.125	mV/ms
Throughput Nonlinearity	±0.005	±0.005	% of 20V
Noise (rms) (10 Hz to 100 kHz)	100	100	μV
Supply Rejection (0 to 50 kHz)	100	100	μV/V
ACCURACY DRIFT			
Gain Drift	±2	±2	ppm of 20V/°C
Offset Drift	±25	±25	μV/°C
Droop Rate			
@ 70°C (max)	10	10	mV/ms
@ +125°C (max)	---	200	mV/ms
DYNAMIC CHARACTERISTICS			
Bandwidth (Full Power)(1)	200	200	kHz
Output Slew Rate	20	20	V/μs
Aperture Time	30	30	ns
Acquisition Time (to ±0.01%)			
10 V Step (max)	4.5	4.5	μs
20 V Step (max)	5.0	5.0	μs
Feedthrough in Hold Mode	±0.005	±0.005	% of step change
Charge Offset (max) @ 0V Input	±2	±2	mV
Sample-to-Hold Transient			
Peak Amplitude	50	50	mV
Settling to 1 mV	0.5	0.5	μs
OUTPUT			
ANALOG OUTPUT			
Voltage Range	±10	±10	V
Current Range	±10	±10	mA
Impedance	0.1	0.1	Ω
TEMPERATURE			
Specification	0 to +70	-55 to +125	°C
Storage	-55 to +125	-55 to +125	°C
POWER SUPPLY			
Rated Voltage	±15	±15	VDC
Range	±14.5 to ±15.5	±14.5 to ±15.5	VDC
Current	±13	±13	mA

(1) Small signal bandwidth is 3MHz.

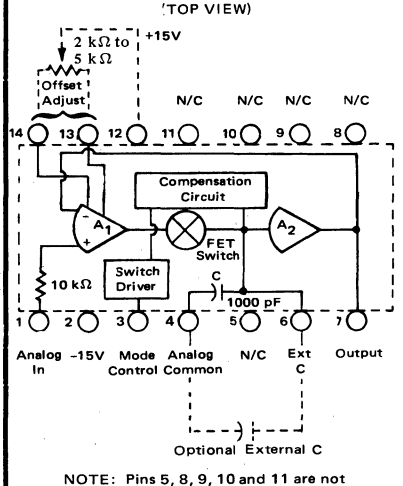
MECHANICAL



Case: Metal
Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883, (except paragraph 3.2)

Mating Connector: 0145 MC

CONNECTION DIAGRAM



NOTE: Pins 5, 8, 9, 10 and 11 are not internally connected.

SHC85

DEFINITION OF SPECIFICATIONS

DYNAMIC NONLINEARITY

This is the total nonadjustable input to output error. This specification includes throughput nonlinearity and errors due to droop, thermal transients and feedthrough, in short, all errors that cannot be adjusted to zero for a 10 volt input change after a 5 μsecond acquisition time and a one millisecond hold time. Offset errors must be adjusted to zero by the offset control and gain errors must be adjusted to zero by a gain adjustment elsewhere in the system (gain adjust not included in SHC85).

GAIN ACCURACY

The difference due to amplifier gain errors between INPUT and OUTPUT voltage when in the "sample" mode.

DROOP RATE

The voltage decay at the output when in the "hold" mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

The amount of the input voltage change that appears at the output when the amplifier is in the "hold" mode.

THROUGHPUT - NONLINEARITY

The total charge offset and gain nonlinearity. That is, the inaccuracy due to these two errors that cannot be corrected by gain and offset adjustments. Throughput - nonlinearity is specified over the 20 volt input range.

THROUGHPUT OFFSET

The sum of sample offset and charge offset.

CHARGE OFFSET

The offset that results from charge transferred from the holding capacitor to the gate capacitance of the switching FET. This charge is partially restored by a special compensation circuit when the unit goes into the "hold" mode.

ACQUISITION TIME

The time required for the output to settle to its final value within a given error band, when the Mode control is switched from "hold" to "sample". See Figure 2.

APERTURE TIME

The time required to switch from "sample" to "hold". The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

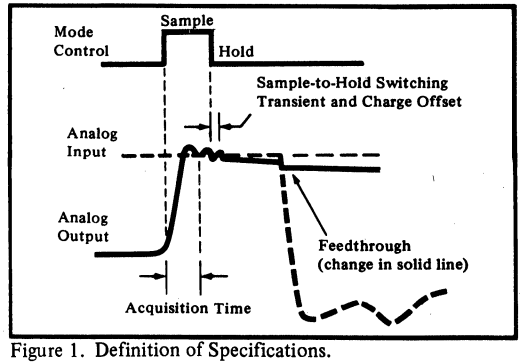


Figure 1. Definition of Specifications.

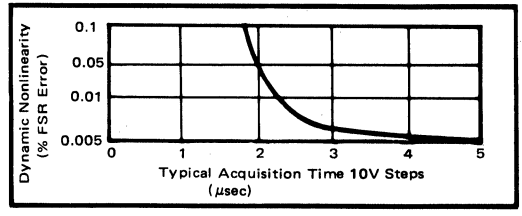


Figure 2. Acquisition Time vs. Full Scale Range Error.

OPERATING INSTRUCTIONS

OPTIONAL EXTERNAL CAPACITOR SELECTION

The value of the external capacitor determines the droop, charge offset and acquisition time of the sample/hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table.

Fig.3 shows the behavior of acquisition time with added external capacitance. The behavior of droop with external C is determined by:

$$\text{Droop} = \frac{dv}{dt} = \frac{0.5 \times 10^{-9}}{1000\ \text{pF} + C_{ext}}$$

Capacitors with high insulation resistance and low dielectric absorption, such as teflon or polystyrene should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize leakage currents from the capacitor; this will minimize droop errors.

OFFSET ADJUSTMENT

Connect a 2k to 5k ohm multi-turn potentiometer with a TCR of 150 ppm/°C or less as shown in the Connection Diagram. The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the "sample" and the "hold" mode. The error should then be adjusted to zero where the unit is in the "hold" mode. In this way, charge offset as well as amplifier offset will be adjusted.

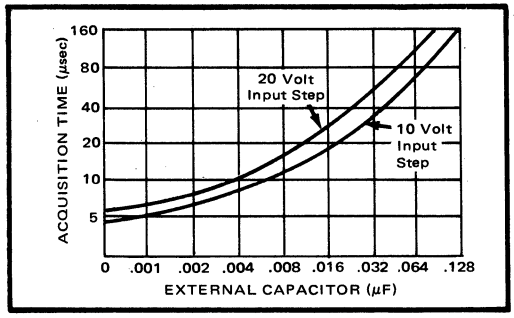
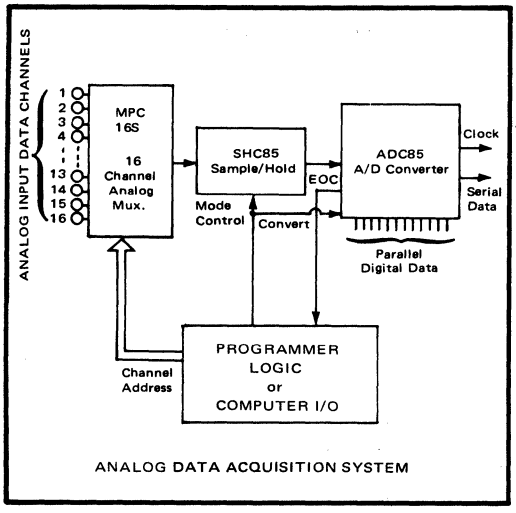


Figure 3. Acquisition Time vs. External Capacitor.

APPLICATIONS

DATA ACQUISITION SYSTEM

The SHC85 makes an excellent device for reducing aperture time in a data acquisition system. When combined with Burr-Brown's 16 channel MPC-16S Analog Multiplexer and ADC85 10 or 12 bit A/D Converter, you can have a compact 16 channel data acquisition system with 50 kHz to 65 kHz throughput sampling rates and 0.02 percent (RSS) system accuracy.



ANALOG DATA ACQUISITION SYSTEM

SIMULTANEOUS SAMPLE/HOLD

Time correlation of sampled data signals may be implemented by using one sample/hold for each analog signal prior to input to an analog multiplexer. The SHC85 low aperture time of 30 nanoseconds practically eliminates channel-to-channel time slew. The throughput sampling rate and the number of data channels will determine the maximum HOLD time and hence, the worst case droop error of the sample/hold in the last channel to be sampled prior to the next "refresh" or sample/hold command. This droop error may be minimized by adding external capacitance to the SHC85 as shown in Figure 3.

The droop error is computed by:

MAX DROOP ERROR (CHANNEL N)=(T x n)(Droop rate)

Where $T = \frac{1}{\text{System Sampling Rate}}$ and

n = number of multiplexer data channels

EXAMPLE:

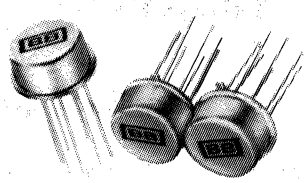
For a 10 bit, 32 channel system with throughput sample rate of 50 kHz, assuming no external capacitance, the droop error of channel N is:

$$\text{Droop Error}(E_D) = \left(\frac{1}{50k} \times 32\right)(500 \times 10^{-3}) = 320\,\mu V$$

For ±10 volt input signal range and 10 bit resolution, the resolution of ±½ LSB is ±9.77 mV. This droop error is less than 0.016 LSB (negligible), and no external C need be added to reduce the droop of the SHC85.

BURR-BROWN®

SHC298AM



Low Cost Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10μsec ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20μV, RMS
- RELIABLE MONOLITHIC CONSTRUCTION
- $10^{10}\,\Omega$ INPUT RESISTANCE
- TTL/PMOS/CMOS-COMPATIBLE LOGIC INPUT

DESCRIPTION

The SHC298AM is a high performance monolithic sample/hold circuit which features very high DC accuracy with fast acquisition times and a low droop rate. With the addition of one external holding capacitor, 12-bit accuracy can be achieved with a 6msec acquisition time. Droop rates less than 5mV/min can be achieved with a one microfarad holding capacitor.

The fully differential logic inputs have low input current, and are compatible with TTL, PMOS, and CMOS logic families. The input offset adjustment can be made using a single external potentiometer and resistor, and the adjustment does not degrade input offset drift.

The SHC298AM will operate with power supplies ranging from ±5DC to ±18VDC. It is available in a hermetically sealed 8 lead low profile package, and is specified for a temperature range from -25°C to +85°C. The SHC298AM is the best price/performance bargain in its class. It is well suited for use in data acquisition systems, data distribution systems, analog delay circuits, and pulse amplitude modulation circuits.

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PDS-373

SPECIFICATIONS

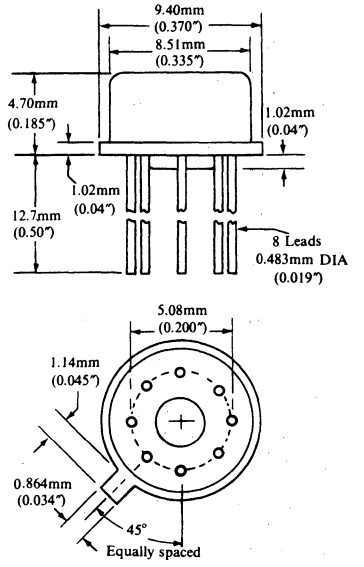
Specifications at T_A = +25°C with rated supplies with 1000 pF holding capacitor unless otherwise noted.

ELECTRICAL

MODELS	SHC298AM MIN	SHC298AM TYP	SHC298AM MAX	UNITS
INPUT				
ANALOG INPUT				
Voltage Range	±(V_{CC}-2.5)			Volts
Maximum Safe Input Signal		±V_{CC}		Volts
Resistance		10^{10}		Ohms
Bias Current		10	50	nA
DIGITAL INPUT	Pin 7	Pin 8	Circuit State	
Mode Control Truth Table	0V	+2.4V	Sample (Track)	
	0V	+0.8V	Hold	
	+2.4V	+2.8V	Hold	
	+0.8V	+2.8V	Sample (Track)	
Mode Control and Mode Control Reference Input Current			10	µA
Differential Logic Threshold		1.4		Volts
TRANSFER CHARACTERISTICS				
ACCURACY (25°)				
Throughput Nonlinearity for Hold Time < 1ms		±0.010	±0.015	% of 20V
Gain		+1.0		V/V
Gain Error		±0.004	±0.010	%
Input Voltage Offset (adj to zero)		±2	±7	mV
Droop Rate		±25	±125	µV/ms
Charge Offset		±15	±25	mV
Noise (rms) 10 Hz to 100 kHz		10	20	µV
Power Supply Rejection		±25	±50	µV/V
ACCURACY DRIFT				
Gain Drift		3	4	ppm/°C
Input Offset Drift		15	45	µV/°C
Charge Offset Drift C = 1000 pF		50	150	µV/°C
C = 10,000 pF		20	50	µV/°C
Droop Rate at T_A = +85°C		1	10	mV/ms
DYNAMIC CHARACTERISTICS				
Full Power Bandwidth, C = 1000 pF	75	125		kHz
C = 10,000 pF	10	16		kHz
Output Slew Rate, C = 1000 pF	7	10		V/µs
C = 10,000 pF	1.4	2		V/µs
Aperture Time				
Negative Input Step		125	200	ns
Positive Input Step		30	45	ns
Acquisition Time (C = 1000 pF)				
to ±0.01%, 10V step		6	10	µs
to ±0.01%, 20V step		8	12	µs
to ± 0.1%, 10V step		5	9	µs
to ±0.1%, 20V step		7	11	µs
Sample-to-Hold Transient				
Peak Amplitude		160		mV
Settling to 1 mV		1.0	1.5	µs
Feedthrough (Response to 10V Input Step)		±0.007	±0.015	% of 20V
OUTPUT				
ANALOG OUTPUT				
Voltage Range	±(V_{cc} -2.5)			Volts
Current Range	±2			mA
Impedance		0.5	4	Ohms
TEMPERATURE				
Specification		-25 to +85		°C
Operating		-55 to +125		°C
Storage		-55 to +150		°C
POWER SUPPLY				
Rated Voltage		±15		VDC
Range[1]	±4.75		±18	VDC
Current		±4.5	±6.5	mA

(1) Logic voltage on pin 8 should not exceed V_{cc} - 1 volt.

MECHANICAL

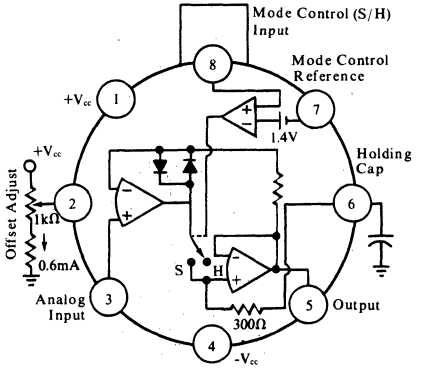


Pin Material and Plating Composition: Conforms to MIL-STD-883 method 2003 (solderability)

Hermeticity: Fluorocarbon (gross leak) and Helium 5 x 10^{-8}cc/sec (fine leak)

Connector: None

PIN CONFIGURATION



TYPICAL PERFORMANCE CURVES

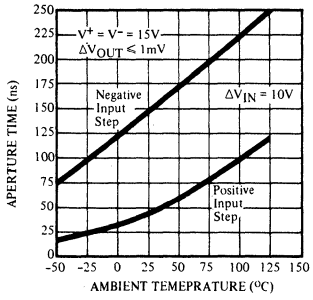


FIGURE 1. Aperture Time

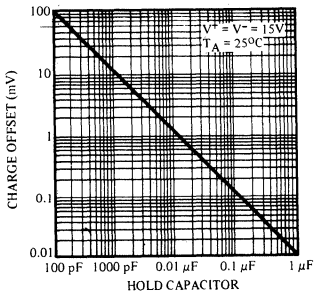


FIGURE 2. Charge Offset

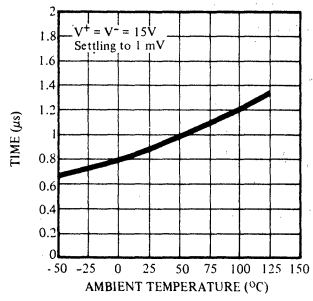


FIGURE 3. Sample-to-Hold Transient Settling Time

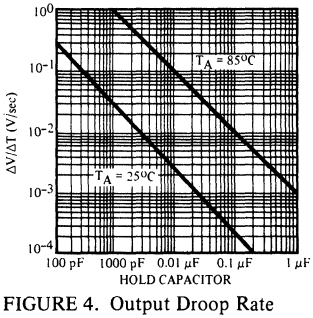


FIGURE 4. Output Droop Rate

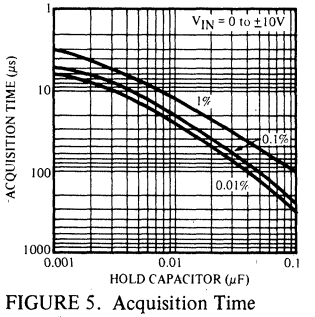


FIGURE 5. Acquisition Time

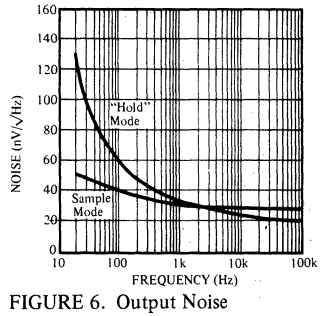


FIGURE 6. Output Noise

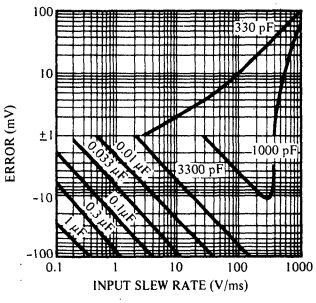


FIGURE 7. Dynamic Sampling Error

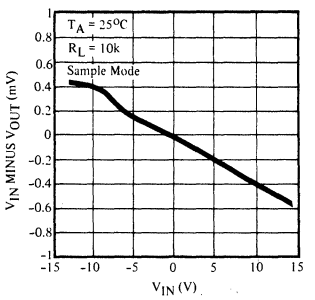


FIGURE 8. Gain Error

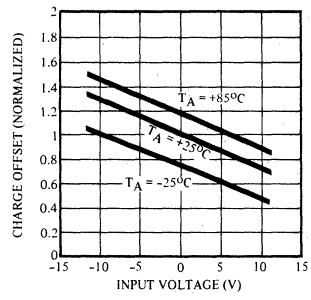


FIGURE 9. Charge Offset

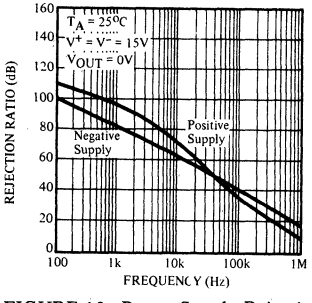


FIGURE 10. Power Supply Rejection

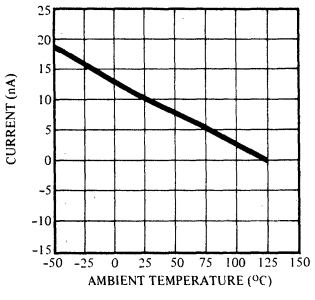


FIGURE 11. Input Bias Current

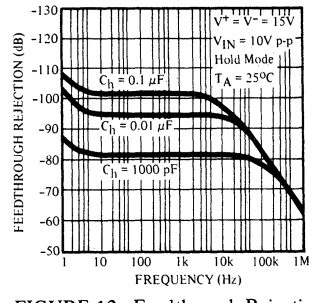


FIGURE 12. Feedthrough Rejection (Hold Mode)

DISCUSSION OF SPECIFICATIONS

THROUGHPUT-NONLINEARITY is defined as total Hold mode, non-adjustable, input to output error caused by charge offset, gain non-linearity, one millisecond of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000 pF holding capacitor, 10 volt input changes, 10μsec acquisition time, and one millisecond Hold time.

GAIN ACCURACY is the difference between INPUT and OUTPUT voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

APERTURE TIME is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME is the time required for the Sample and Hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

CHARGE OFFSET is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

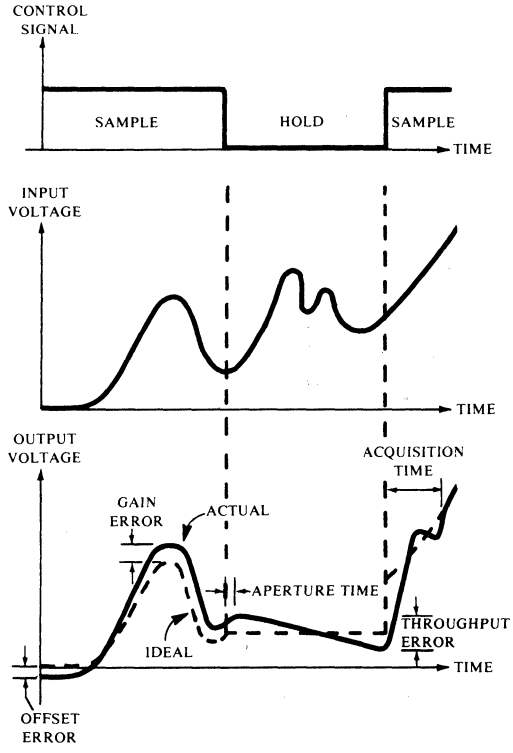


FIGURE 13. Sample-Hold Errors

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as teflon, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce charge offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001μF capacitor. With a capacitor of 0.01μF the droop will reduce to approximately 2.5μV/ms and the charge offset to approximately 1.5mV. Figure 5 shows the behavior of acquisition time with changes in external capacitance.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the Sample/Hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001μF capacitor is used, it will not be possible to adjust the full offset error at the Sample Hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298AM may be used to hold data for conversion with an analog to digital converter or used to provide Pulse Amplitude Modulation (PAM) data output.

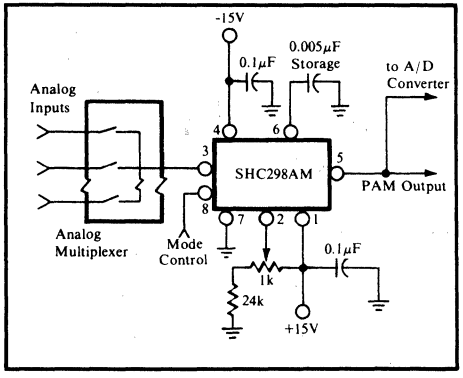


FIGURE 14. Data Acquisition

DATA DISTRIBUTION

The SHC298AM may be used to hold the output of a digital to analog converter whose digital inputs are multiplexed.

TEST SYSTEMS

The SHC298AM is also well suited for use in test systems to acquire and hold data transients for human operators or for other parts of the test system such as comparators, digital voltmeters, etc.

With a 0.1 μF storage capacitor, the output may be held 10 seconds with less than 0.1% error. With a 1 μF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

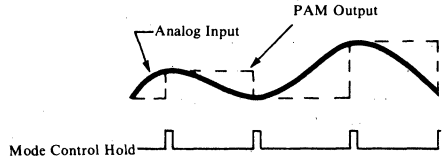


FIGURE 15. PAM Output

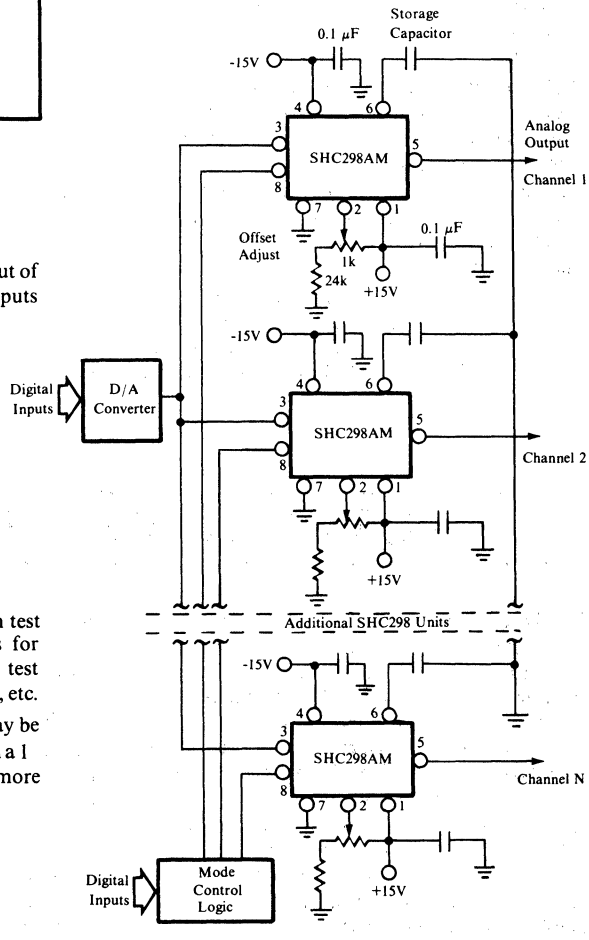


FIGURE 16. Data Distribution

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the Sample and Hold plus the conversion time of the analog to digital converter. If two or more Sample and Holds are used with a high speed multiplexer, the acquisition time of the Sample and Hold can be virtually eliminated. While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second Sample and Hold will have acquired this data by the time the conversion is complete. Then, the Sample and Holds reverse roles and another channel is addressed. For low level systems, an instrumentation amplifier and double-ended multiplexer may be connected to the Sample and Hold inputs. The settling time of the multiplexer, instrumentation amplifier, and Sample and Hold can be eliminated from the channel conversion time as before.

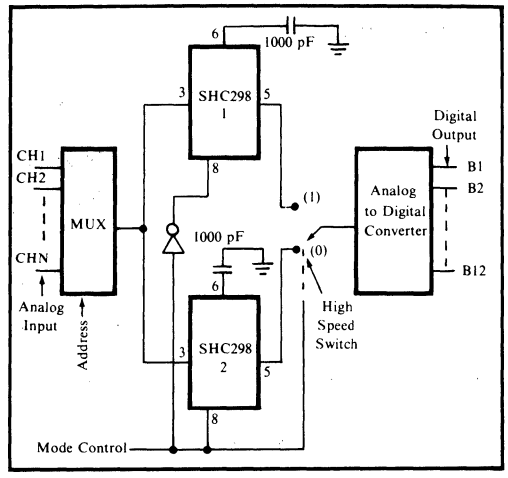
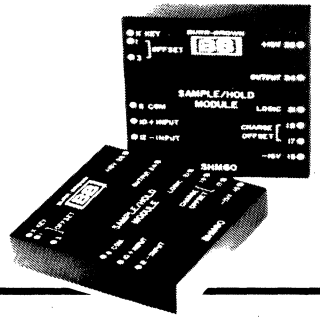


FIGURE 17. "Ping-Pong" Sample/Holds

BURR-BROWN®

SHM60



High Speed SAMPLE/HOLD

FEATURES

- 1μsec ACQUISITION
- .01% ACCURACY
- SELECTABLE GAINS - ±1 to ±1000
- 12nsec APERTURE TIME
- LOW FEEDTHROUGH - 0.005%

DESCRIPTION

Designed for use with fast A/D and D/A converters and analog multiplexers, the Burr-Brown Model SHM60 high-speed sample/hold acquires analog signals of up to ±10V amplitude and settles to 0.01% in less than 1.5μsec for a 20V input step, and in less than 1μsec for a 10V input step. Both analog input terminals are available for user selection of gains from unity to 1000.

Internal compensation of charge storage effects and dielectric absorption are provided to assure accurate and fast operation. The SHM60 dynamic nonlinearity of 0.01% is specified for hold periods of up to 15μsec to simplify the user's task of computing system throughput error for specific operating conditions.

The 2" x 2" x 0.4" encapsulated modular package operates from ±15VDC power and is compatible with Burr-Brown's line of fast A/D and D/A converters such as Models ADC85 and ADC80 and ADC84 A/D converters, and DAC85, DAC80 and DAC85 D/A converters.

A few of the more popular applications for the SHM60 are:

A/D converter aperture error reduction
Time correlation of sampled signals
i.e., simultaneous sample/hold
Multiplexing D/A converter outputs
Generation of pulse-amplitude-modulation
(PAM) telemetry signals
Analog memory for analog computations

... and many more.

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PDS-310A

SPECIFICATIONS

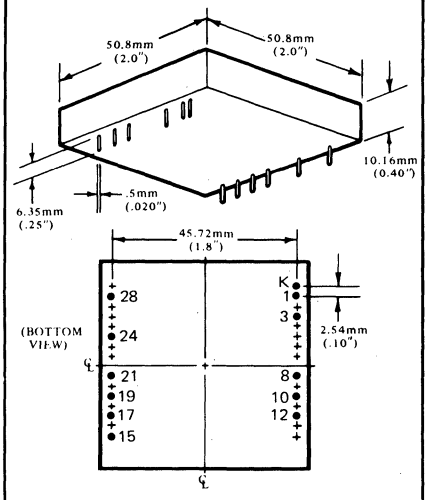
Typical at 25°C and rated supplies unless otherwise noted.

ELECTRICAL

MODEL	SHM60			
	Min	Typ	Max	Units
INPUT				
ANALOG INPUT				
Signal Voltage	-10		+10	V
Maximum Safe Input[1]	-15		+15	V
Impedance		10^{11}		Ω
Bias Current		50		pA
DIGITAL INPUT (Mode Control)[2]				
Sample Mode (Logic 1)				
at 100 μA Source	+2.4		+5.0	V
Hold Mode (Logic 0)				
at 50 nA Sink	0.0		+0.8	V
Rise Time for Specified Performance			5	nsec
INPUT POWER				
+15V Supply Voltage Range	+14.55	+15	+15.45	Vdc
-15V Supply Voltage Range	-14.55	-15	-15.45	Vdc
Quiescent Current				
+15V Supply - Sample Mode		25		mA
- Hold Mode		17		mA
-15V Supply - Sample Mode		15		mA
- Hold Mold		15		mA
TRANSFER CHARACTERISTICS				
ACCURACY at Gain of 1 V/V[3]				
Dynamic Nonlinearity[4]		±0.005	±0.01	% of 20V
Gain Error		±0.005	±0.01	% of 20V
Throughput Offset (Adj. to Zero)[5]		3		mV
Droop Rate		1	5	μV/μsec
Dielectric Absorption[4]		±0.005		% of ΔV
Noise		100		μV rms
Common Mode Rejection Ratio	10^{-4}			V/V
Power Supply Rejection		10	30	ppm/%
ACCURACY DRIFT (0°C to +70°C)				
Throughput Drift		±2		ppm of 20V/°C
Droop Rate		doubles every 10°C		
DYNAMIC CHARACTERISTICS				
Bandwidth (Full Power)		400		kHz
Output Slew Rate		25		V/μsec
Acquisition Time (to ±0.01%)				
10V Step		0.8	1	μsec
20V Step		1.2	1.5	μsec
Aperture Time		12		nsec
Sample-to-Hold Transient				
Peak Amplitude		50		mV
Settling to .01%			200	nsec
Feedthrough in Hold Mode			±0.005	% of Step Change at input
OUTPUT				
Voltage Range	±10			V
Current Range	±20			mA
Impedance (Short Circuit Protected)			1.0	Ω
TEMPERATURE				
Specification	0 to +70			°C
Storage	-55 to +125			°C

NOTES:
1. Input should never exceed supply by more than 0.6 volts.
2. Shottky TTL compatible.
3. Gain is user selectable.
4. For 1 μsec SAMPLE and 15 μsec HOLD times.
5. Includes voltage and charge offsets.

MECHANICAL

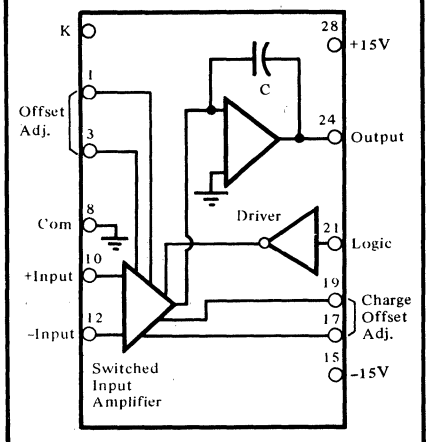


Dimensions in parentheses are in inches.

WEIGHT: 56.7 grams (2 oz)
MATING CONNECTORS:
2300 - P.C. Card and Terminals
2301 - Set of 2 - 16 Pin Connector Strips
PINS: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].

CONNECTION DIAGRAM

(TOP VIEW)



SHM60

DISCUSSION OF SPECIFICATIONS

ACCURACY

All SHM60 sample/hold units are tested for accuracy and are factory trimmed to assure that all units meet critical specifications.

DYNAMIC NONLINEARITY

This is the unadjustable throughput error from input to output for a 1 microsecond SAMPLE period and a 15 microsecond HOLD period. Errors included in this specification are throughput nonlinearity, dielectric absorption, droop, thermal transients and feedthrough. Offset errors must be adjusted to zero with an offset trim control and gain errors must be adjusted to zero with a gain trim control elsewhere in the system.

ACCURACY – UNITY GAIN OPERATION

The initial accuracy of the SHM60 is ±0.01% maximum of full scale range when operated as a unity gain voltage follower.

GAIN and OFFSET ERRORS - GAINS OTHER THAN UNITY

The SHM60 should be treated in the same manner as an operational amplifier when gains other than unity are employed. The gain setting resistor parameters such as absolute accuracy and tracking ratio must be considered when computing error effects for gains other than unity.

THROUGHPUT DRIFT

The input to output accuracy drift over a 0°C to +70°C temperature range is the throughput drift - it is ±2 ppm/°C or ±0.0002% of 20 volts.

THROUGHPUT OFFSET

The output offset voltage encountered in the HOLD mode after sampling a grounded input is throughput offset. This error includes charge offset at zero volts input as well as amplifier d.c. voltage offsets.

ACQUISITION TIME

The acquisition time of the SHM60 is defined as shown in Figure 1. This is the time required for the SHM60 to turn on, slew and settle to 0.01% of the input voltage when the mode is changed from HOLD to SAMPLE.

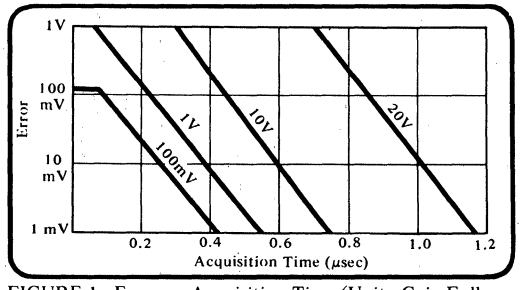


FIGURE 1. Error vs. Acquisition Time (Unity Gain Follower).

SAMPLE-TO-HOLD SWITCHING TRANSIENT

When the mode control is changed from SAMPLE -to-HOLD, the switching transient that appears on the output is the sample-to-hold switching transient.

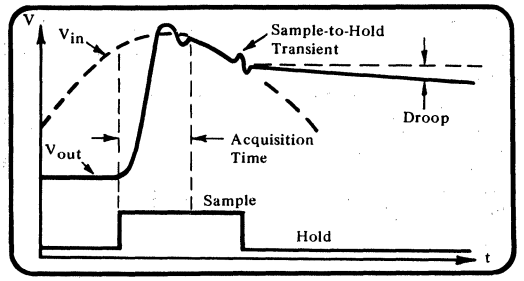


FIGURE 2. Definition of Acquisition Time Droop and Sample-to-Hold Transient.

DROOP RATE

Droop in a sample/hold is the voltage decay at the output due to output amplifier bias current when operating in the HOLD mode. To determine the effects of droop on system accuracy, the droop rate is multiplied by the HOLD period.

FEEDTHROUGH

The amount of input voltage change seen at the output when the sample/hold is in the HOLD mode is feedthrough error. The low feedthrough error of 0.005% preserves the accuracy of the sampled signal and can be used to increase the throughput sample rate, especially in time multiplexed applications.

APERTURE TIME

Aperture time is the delay between the time the sample/hold is given the command to HOLD the input signal and the time that this actually occurs. The SHM60 aperture time of 12 nanoseconds is sufficiently small to make aperture errors negligible for most applications.

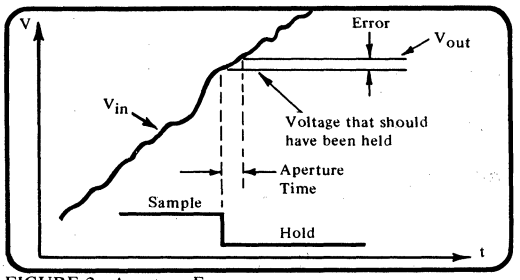


FIGURE 3. Aperture Error.

SYSTEM ERROR CONSIDERATIONS

The 1 μsec acquisition time and 12 nanoseconds aperture window of the SHM60 offer an excellent way of reducing system sampling error at high throughput rates for sinusoidal data. Taking the maximum slope of a sine wave at the zero crossing where maximum sampling error occurs, the error voltage as a percentage of full scale is proportional to the product of frequency and aperture time (Δt):

$$\% \text{ Aperture Error} = \frac{\Delta V}{V} \times 100 = 2\pi f \Delta t \times 100$$

where ΔV = Aperture error
V = Peak signal amplitude
f = Maximum signal frequency
Δt = Aperture time

INSTALLATION and OPERATING INSTRUCTIONS

OPTIONAL VOLTAGE and CHARGE OFFSET ADJUSTMENTS

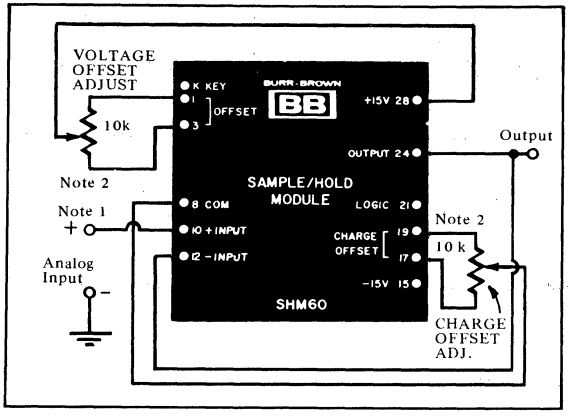


FIGURE 4. Optional CHARGE and VOLTAGE OFFSET Adjustment Connections.

Throughput OFFSET error may normally be adjusted to zero with a single external VOLTAGE OFFSET adjust control, as shown in Figure 4. A small CHARGE OFFSET error of 1 mV to 3 mV in the HOLD mode may occur. This CHARGE OFFSET error may also be adjusted to zero with an optional external CHARGE OFFSET adjustment as shown in Figure 4.

NOTES:
1. The analog input signal should not be run under or over the module as this may degrade feedthrough in the HOLD mode.
2. Potentiometers should have a TCR of 100 ppm/^{o}C or less.

- Care must be taken to provide a good low impedance common as there is an appreciable amount of current returned to the power supplies.
- Power supply bypass capacitors are provided in the module, but additional bypassing may be required if excessive noise is present on the power supply lines.

CONNECTIONS FOR GAINS OTHER THAN UNITY

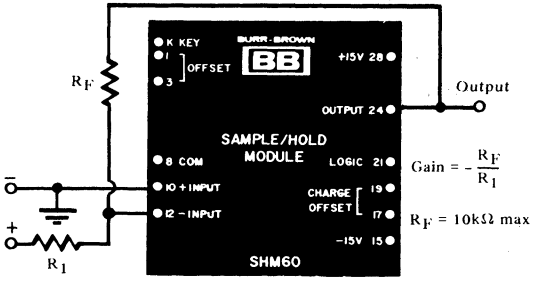


FIGURE 5. SHM60 Connections for Inverting GAIN.

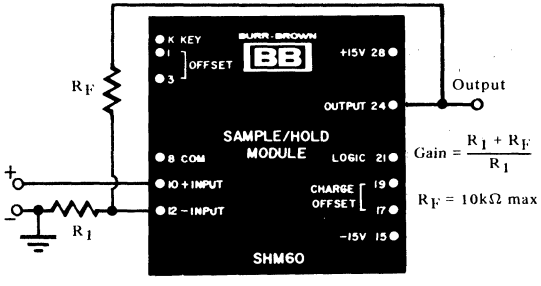


FIGURE 6. SHM 60 Connections for Non-Inverting GAIN.

Although optimum performance is at unity gain, the SHM60 may be operated to provide gains ranging from ±1 to ±1000 as shown in Figures 5 and 6. For these configurations, the unit may be treated as an operational amplifier. Acquisition time will get longer as gain increases, approximately 2.5 μsec settling to ±0.01% for a gain of 5 and 4 μsec for a gain of 10 for 10 volt output steps. Voltage drift can be computed as with an op amp using 10 μV/^{o}C as the input drift.

NOTES:
- Gain accuracy and drift is dependent on the absolute accuracy and thermal tracking properties of the gain setting resistors R_1 and R_F. Metal film or better quality low drift resistors are recommended.
- Charge offset is independent of gain, and is referred to the output.

BURR-BROWN®

VFC12
VFC15
VFC12LD
VFC15LD

VOLTAGE-TO-FREQUENCY CONVERTERS

APPLICATIONS

A/D CONVERSION - 13-bit accuracy

DPM FRONT END - 3+ digits accuracy

LONG-LINE SIGNAL TRANSMISSION
Increase noise immunity using only one transmission line

OPTICAL ISOLATION
Use simpler isolation techniques than with analog isolation and with only one isolator

FEED RATE GENERATOR AND CONTROL
0.05% accuracy over 0°C to +70°C

FEATURES

LOW COST

ONE SIGNAL LINE TRANSMISSION COMPACT
1.5" x 1.5" x 0.4" module package

ACCURATE
0.005% linearity gives you 13-bit accuracy

STABLE
10ppm/°C max gain drift (LD versions) gives you excellent stability over temperature

VERSATILE
Many simple-to-implement scaling options
Unipolar or bipolar operation - VFC15

CONVENIENTLY SCALED
1kHz per volt

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-314

GENERAL DESCRIPTION

Voltage-to-frequency conversion is a simple and low cost method of converting analog signals into an equivalent digital form. The output is a TTL/DTL compatible digital pulse train whose repetition rate is proportional to the amplitude of the analog input signal; these pulses have constant width and constant amplitude.

The Burr-Brown Model VFC12 accepts 0 to 10 volt analog signals and is pin compatible with Teledyne Philbrick's Model 4701. The Model VFC15 accepts either 0 to 20 volt or 0 to 20 mA current analog signals.

The VFC12 operates over a DC to 10 kHz frequency range and the VFC15 operates over a DC to 20 kHz frequency range.

The low 0.01% nonlinearity error of these V/F converters makes them excellent for use in applications where digital resolutions of 12 or 13 bits are desired. These 1.5" x 1.5" x 0.4" modular units are completely self-contained and require only ±15 Vdc power and input signal. The gain and offset are adjustable with external potentiometers. A number of optional configurations to scale the input or output for best compatibility with your system are easily realized with simple external circuitry.

THEORY OF OPERATION

The Model VFC12 and Model VFC15 are ultra-linear voltage-to-frequency converters that provide a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. To understand the operation of the circuit consider the block diagram in Figure 1.

Amplifier A1 is connected in an integrator configuration. The integrator capacitor C begins charging at a constant rate in response to the input voltage until the output of A1 reaches a certain potential V_{ref}. At this time a comparator triggers a frequency-controlling charge dispenser which removes a precision amount of charge from C. The frequency at which this charge transfer occurs is linearly related to the input voltage.

A1 need not be an exceptionally high-gain or fast slewing operational amplifier. As long as the average current at the summing junction of A1 is zero, the frequency of oscillation must be directly proportional to the input voltage with little dependence on the gain or speed of A1.

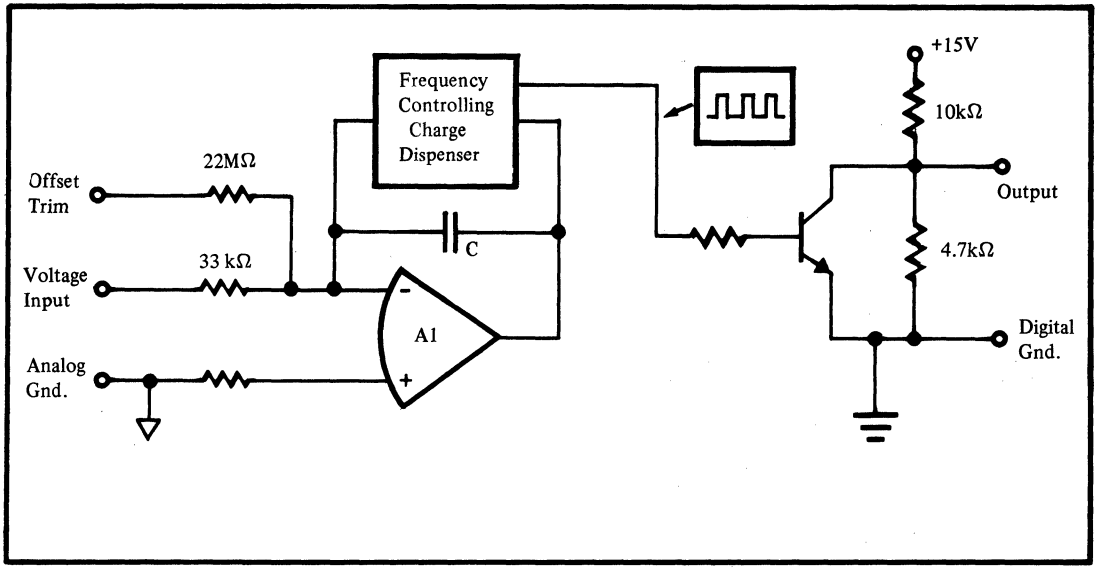


FIGURE 1. Functional Block Diagram of Model VFC12.

SPECIFICATIONS

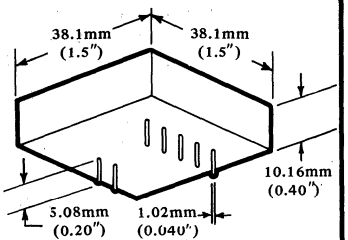
ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

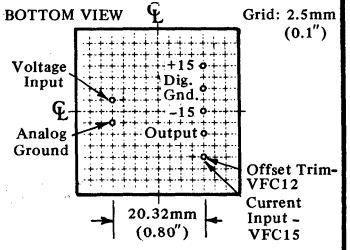
MODEL	VFC12	VFC12LD	VFC15	VFC15LD	UNITS
FREQUENCY RANGE	10		20		kHz
INPUT					
ANALOG INPUT					
Voltage Range	0 to +10		0 to +20		V
Overrange (min)	100		10		% of FSR(1)
Impedance	33		33		kΩ
Maximum Safe Input Voltage	22		22		V
INPUT POWER					
Rated Voltages(2)	±15 ±10%				Vdc
Supply Drain					
Typical	±16				mA
Maximum	±20				mA
TRANSFER CHARACTERISTICS					
TRANSFER EQUATION	$f_{out} = 10^4 \frac{V_{in}}{10}$				Hz
ACCURACY					
Full Scale Gain Error(3)	Adjustable				
Offset Error(4)					
Typical	±0.002		±0.001		% of FSR
Maximum	±0.01		±0.005		% of FSR
Linearity Error (max)					
V_{in} = +1 mV to +10 V	±0.01	±0.005	–		% of FSR
V_{in} = +1 mV to +20 V	–		±0.01	±0.005	% of FSR
Power Supply Sensitivity	±0.005				% of FSR/%
STABILITY (0°C to +70°C)					
Full Scale Drift (Gain + Offset)					
Voltage Input					
Typical	20	8	20	8	ppm of FSR/°C
Maximum	50	10	50	10	ppm of FSR/°C
Current Input	N/A		35	15	ppm of FSR/°C
Stability vs. Time					
Full Scale Drift					
Per day	±100				ppm of FSR
Per month	±200				ppm of FSR
Input Offset Drift					
Per day	±10				ppm of FSR
Per month	±20				ppm of FSR
Offset Drift					
Typical	±2				ppm of FSR/°C
Maximum	±5				ppm of FSR/°C
RESPONSE					
Settling Time for 10V Input Step	2 output pulses of new frequency plus 20 μsec				
Overload Recovery Time	1 to 2 pulses of new frequency				
TEMPERATURE RANGE					
Specification	0 to +70				°C
Operating (derated specifications)	-25 to +85				°C
Storage	-55 to +125				°C
OUTPUT					
Waveform	Train of TTL/DTL compatible pulses				
Pulse Characteristics					
Logic 1 (High)	4.7 ±0.5				V
Logic 0 (Low)	0.2 ±0.1				V
Pulse Width	30				μsec
Fan Out	10 TTL Loads				
Impedance	3				kΩ
Capacitive Load (max)	1000				pF

(1) FSR = Full Scale Range and is 10V for VFC12 and 20V for VFC15.
(2) A regulated supply with 1% or less ripple is recommended.
(3) Adjusted at factory for 9.900V = 10 kHz.
(4) May be externally adjusted to zero.

MECHANICAL

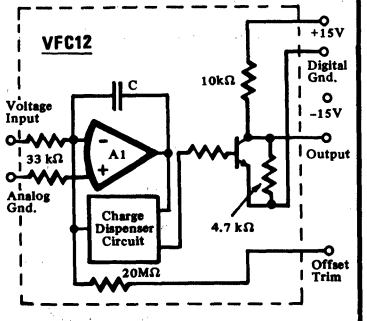


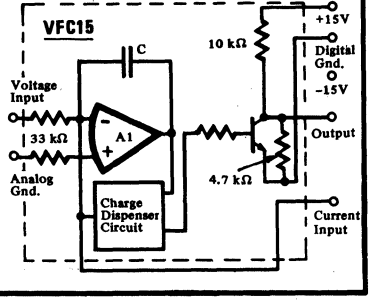
Dimensions in inches are shown in parentheses.



MATERIAL:
Case: Diallyl Phthalate or Epoxy Shell
Pin material and plating composition conform to Method 2003 (solderability) of Mil-Std-883 [except paragraph 3.2].
Weight: 25 grams (0.875 oz)
Mating Connector: 1400 MC

CIRCUIT DIAGRAMS





DISCUSSION OF SPECIFICATIONS

DYNAMIC SIGNAL RANGE

The VFC12 is specified to operate over a DC to 10 kHz frequency range for an input voltage of 0 to +10 volts. Since this unit has a specified overrange of 100%, it is possible to extend the input signal and output frequency ranges to 20 volts and 20 kHz respectively. However, the linearity is not guaranteed over this range. If the extended range of operation is desired, Burr-Brown recommends using the VFC15 for greater than 10 volt and 10 kHz operation. In addition to the extended voltage and frequency range, the VFC15 has its input summing junction made available for applications requiring current-to-frequency conversion and bipolar input signals up to ±10 volts.

Figure 2 depicts the transfer function of these units. The input current-to-frequency transfer function for the VFC15 is shown for a calibrated 1000 ohm shunt resistor (see page 6-365).

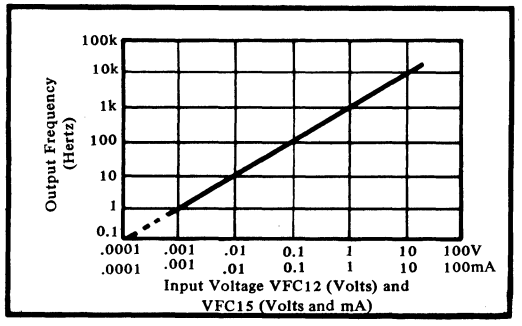


FIGURE 2. Voltage or Current-to-Frequency Characteristic.

ACCURACY

The transfer linearity of these V/F converters is one of the most meaningful measures of accuracy since initial full scale and offset errors are externally adjustable to zero. All VFC12 and VFC15 units are factory calibrated for maximum linearity error of 0.01% of full scale range input signals. Although Burr-Brown guarantees a maximum linearity error of ±0.01% of full scale, the linearity error of these units is typically less than ±0.002% of full scale. The use of regulated power supplies with better than 1% regulation is recommended in order to maintain the accuracy of these units. The 0.01% linearity makes these units excellent for use as a front end for 10 to 12 bit resolution A/D converters, and for highly accurate transfer of analog data over long lines in noisy environments.

FREQUENCY STABILITY vs. TEMPERATURE

Frequency drift is factory tested with the offset and full scale calibration made at 25°C, and is expressed as parts per million of full scale range vs. temperature. Typically, full scale drift is ±20 ppm/°C over the operating temperature range for VFC12 and VFC15. VFC12LD and VFC15LD have typical full scale drifts of 8 ppm/°C.

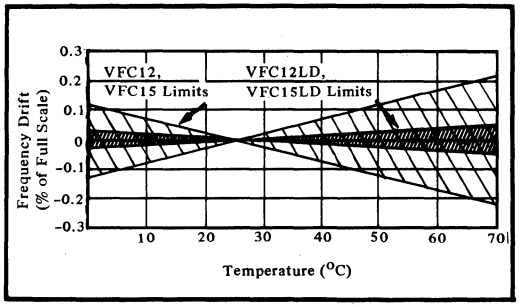


FIGURE 3. Frequency Drift vs. Temperature with Calibration made at 25°C.

FULL SCALE AND OFFSET DRIFT

All units are tested for full scale and offset drift over a 0°C to +70°C operating temperature range. Internal temperature compensation is provided for ±50 ppm/°C maximum full scale drift and ±5 ppm/°C offset drift for VFC12 and VFC15. Maximum full scale drift for VFC12LD and VFC 15LD is ±10ppm/°C. If external full scale and offset trim adjustments are provided, the temperature coefficient of the external components must be added to the specified drift components as shown on page 5-183 to determine the total thermal coefficients of drift.

RESPONSE

The settled response of these units to changes in input signal is specified for an input signal step change of 10 volts and is 20 microseconds plus 2 output pulses of new frequency. For 10 volt input signal steps, the VFC12 operating at 10 kHz full scale frequency range, the step response settling is 220 μsec; for the VFC15 operating at 20 kHz full scale frequency range, the step response settling is 120 μsec. Figure 4 shows the typical response of these units to instantaneous changes in the input signal.

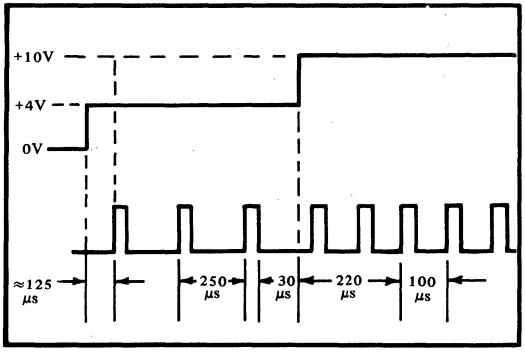


FIGURE 4. Typical Response to Instantaneous Changes in the Input Voltage.

INSTALLATION AND OPERATING INSTRUCTIONS

INSTALLATION

The VFC12 and VFC15 are designed for installation on a flat mounting surface such as a printed circuit board or a chassis. The pins may be hand or dip soldered; for plug in installations, the accessory connector (1400MC) or mounting jacks may be installed on a chassis or p.c. board.

Particular attention should be given to wire or p.c. conductor path routing. All input signal lines should be as short as possible, and coupling from power supply lines should be minimized

For best results, the power supply should have 1% or better regulation and low ripple and noise. The Burr-Brown Model 550 series ±15 volt output modular power supplies provide excellent regulation, and are recommended for use with these V/F converters. Normally external power supply bypass capacitors are not required. However, if a good quality low ripple power source is not available, 1 μF or larger external bypass capacitors are recommended in order to prevent interference from power supply effects.

CAUTION: Do not short Output to -15 Volt Pin.

EXTERNAL CONNECTIONS

FULL SCALE AND OFFSET ADJUSTMENTS

The VFC12 and VFC15 V/F converters are factory calibrated to meet all specifications. However, FULL SCALE and OFFSET may be user adjusted when absolute accuracy better than the specified initial accuracies are required.

These units are factory calibrated to provide a FULL SCALE output frequency of 10 kHz for an input voltage of 9.900 V ±0.05% and may be calibrated to provide 10.000 kHz output frequency for an exact input voltage of 10.000 volts. OFFSET is factory calibrated to provide an output frequency of 1 ±0.2 Hz for an input voltage of 1.0 millivolts.

Normally, OFFSET need not be adjusted unless absolute accuracies of better than ±0.004% are required.

ADJUSTMENT PROCEDURE

Select external potentiometers with low drift coefficients to preserve the drift characteristics of the V/F converter. The drift effects must be added to the ±50 ppm/°C specified FULL SCALE temperature coefficient. For example, external component contribution of R_1 to drift will be:

$$\left[\frac{R_1}{33\,k + R_1} \times \text{Tempco } R_1\right] /^{\circ}C$$

To calibrate these units, first apply +1.0 mV to the analog input terminals and adjust R_2 for f_{out} = 1.0 Hz. Then apply +10.000 volts to the input and adjust R_1 for f_{out} = 10.000 kHz. Interaction between R_1 and R_2 is generally negligible due to the low initial offset voltage; however, repeating the above calibration will insure precise calibration.

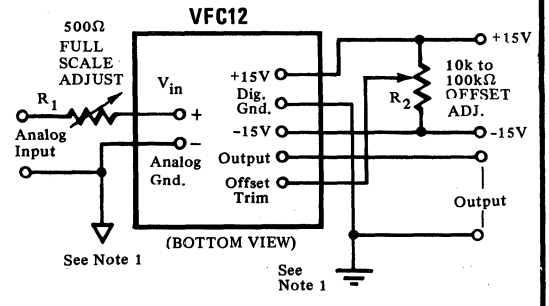


FIGURE 5. VFC12 Optional FULL SCALE and OFFSET Adjustments.

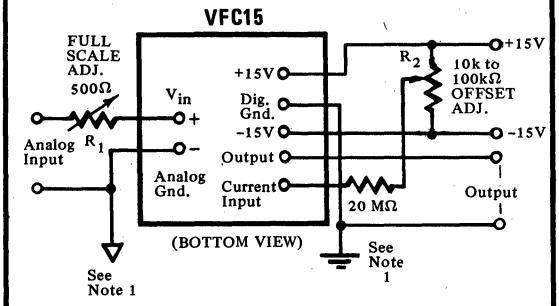


FIGURE 6. VFC15 Optional FULL SCALE and OFFSET Adjust for Voltage Input Signals.

NOTE 1: Digital and Analog grounds should be tied together as close as possible to the power supply common.

OPERATING OPTIONS

CURRENT-TO-FREQUENCY CONVERSION

A method of obtaining direct conversion of input currents of 0 to 10 mA for Model VFC12 and 0 to 20 mA for Model VFC15 corresponding to output frequency ranges of 0 to 10 kHz and 0 to 20 kHz respectively is described in Figure 7. Figure 7 describes a calibrated 1000 ohm shunt resistance across the voltage input terminals. Full scale output is calibrated by adjusting the 1000 ohm shunt performing the usual offset adjustments.

The second technique, described in Figure 8, is a simple current divider into the summing junction (CURRENT INPUT) of the VFC15. This method offers the advantage of limiting the voltage swing on the input terminal to a 3.8 to 5.55 volt range for a 0 to 20 mA input current range, depending on the value of the full scale adjustment potentiometer, offering better compliance to the current source. OFFSET may be adjusted as shown on page 6-364.

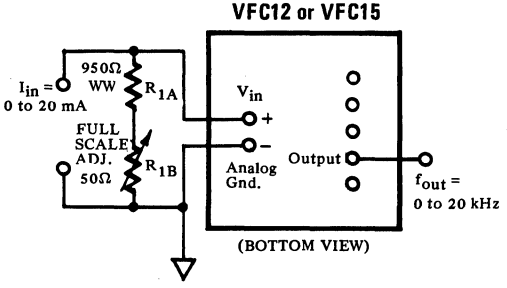


FIGURE 7. VFC15 Current-to-Frequency Conversion using Voltage Input Terminals.

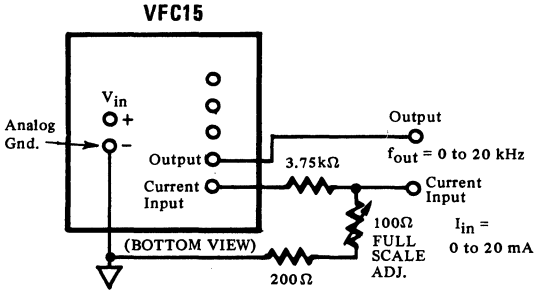


FIGURE 8. VFC15 Current-to-Frequency Conversion using Current Input Terminal.

SCALING FOR BIPOLAR INPUT VOLTAGE RANGE

The summing junction (CURRENT INPUT) of the VFC15 is made available for scaling the unit to accept ±5 volt or ±10 volt input signals. An external reference and scaling resistors must be connected to the CURRENT INPUT. OFFSET is adjusted as shown on page 6-364.

Figures 9a and 9b show an example with a +10 volt reference. The reference regulation and drift should be low in order to preserve signal accuracy. The output frequency range for these input voltage ranges will be centered at 5 kHz for the ±5 volt range and at 10 kHz for the ±10 volt range. The corresponding output frequency ranges will be:

SIGNAL RANGE	INPUT SIGNAL	OUTPUT FREQUENCY (kHz)
±5 V	-5 V	0
	0 V	5
	+5 V	10
±10 V	-10 V	0
	0 V	10
	+10 V	20

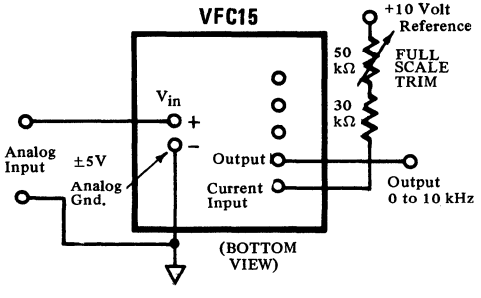


FIGURE 9a. Scaling the VFC15 for ±5 volt Bipolar Operation.

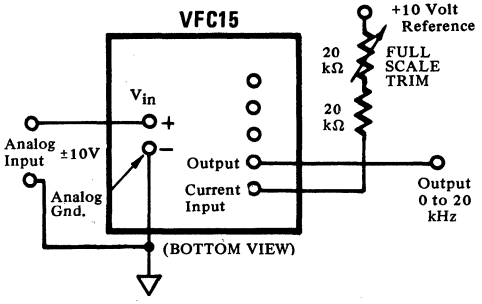


FIGURE 9b. Scaling the VFC15 for ±10 volt Bipolar Operation.

SQUARE-WAVE OUTPUT

A type D flip-flop in a frequency dividing configuration provides a convenient method of obtaining a variable width square wave output from the VFC12 or VFC15 as shown in Figure 10. The output of the V/F converter is used to drive the clock input of the flip-flop.

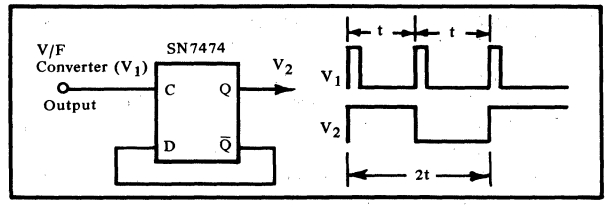


FIGURE 10. Square Wave Output Using a Type D Flip-Flop.

DRIVING HIGH NOISE IMMUNITY LOGIC

A pullup resistor to +15 volts on the V/F converter output as shown in Figure 11 provides 4 volt noise immunity for driving high noise immunity logic (HNIL).

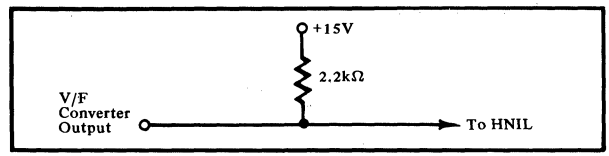


FIGURE 11. Pullup Resistor for Driving HNIL.

OUTPUT ISOLATION

Optical coupling the V/F converter outputs provides an excellent method of obtaining 500 Vdc or 1000 Vac p-p isolation between the V/F converter and a receiving device. The isolation is accomplished digitally, preserving signal accuracy. The common mode capability of the circuit shown in Figure 12 is limited only by the optical isolator and the power supply.

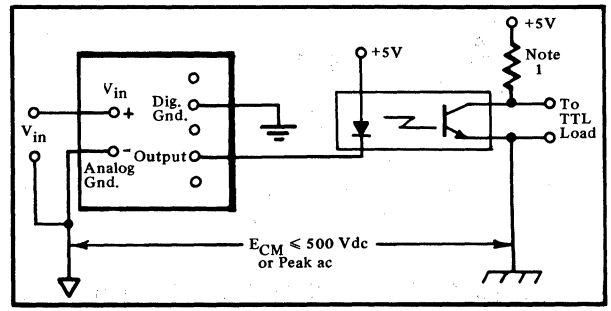


FIGURE 12. Optical Isolation of V/F Converter Output.

NOTE 1: This +5 V supply is isolated from the +5 V supply used for the diode.

SCALING FOR 1kHZ OUTPUT FREQUENCY RANGE

Two methods are described in Figures 13 and 14 for obtaining a 1 kHz full scale V/F converter using the VFC12 or VFC15.

GAIN ATTENUATION

In the circuit of Figure 13 the input is attenuated by a 10:1 divider. This technique is the least expensive to implement but has the disadvantage of added thermal drift of the external components and does not permit the V/F converter to operate over the most linear portion of its frequency range.

FREQUENCY DIVISION

Figure 14 illustrates the best method of obtaining a 1 kHz frequency range using an external decade counter. The disadvantages of the gain attenuation technique are overcome, but this technique is more expensive to implement.

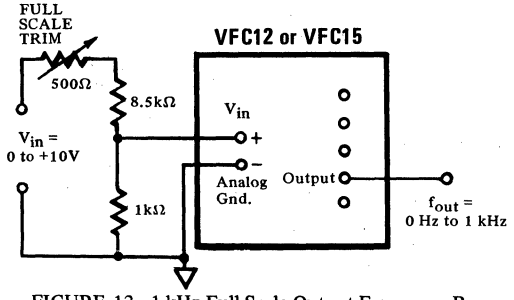


FIGURE 13. 1 kHz Full Scale Output Frequency Range Using Input Attenuation Network.

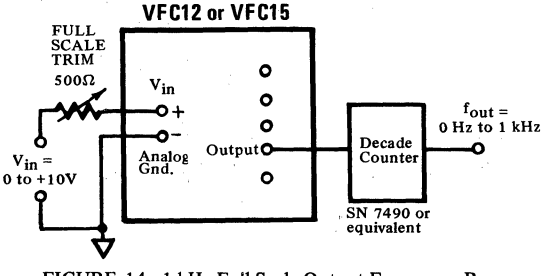
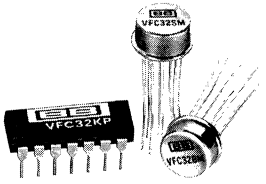


FIGURE 14. 1 kHz Full Scale Output Frequency Range Using Decade Counter.

BURR-BROWN®



VFC32

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- RELIABLE MONOLITHIC CONSTRUCTION
- HIGH LINEARITY
  ±0.01% max at 10kHz FS
  ±0.05% max at 100kHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- VOLTAGE OR CURRENT INPUT
- OUTPUT DTL/TTL/CMOS COMPATIBLE

APPLICATIONS

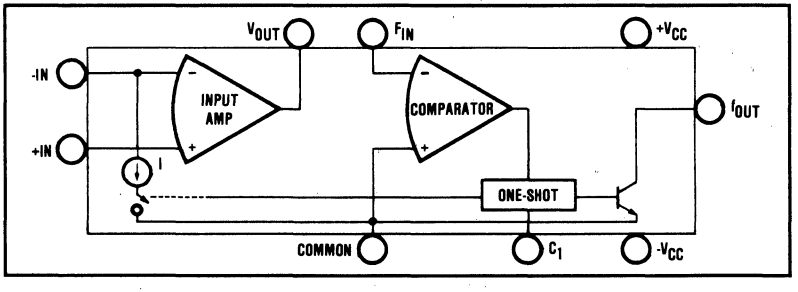
- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC32 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

The converter requires two external resistors and two external capacitors to operate. Full scale frequency and input voltage are determined by one resistor (in series with -IN) and two capacitors (one-shot timing and input amplifier integration). High linearity is achieved with relatively few external components, e.g., ±0.01% at 10kHz. The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$).

The VFC32 is available in three models and two package configurations. The TO-100 versions are hermetically sealed, and specified for the -25°C to +85°C and -55°C to +125°C ranges, and the epoxy dual-in-line unit is specified from 0°C to +70°C.



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PDS-372B

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

		VFC32KP			VFC32BM			VFC32SM			
CHARACTERISTICS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT (V/F CONVERTER)	$F_{OUT} = V_{IN} / 7.5\ R_1C_1$, Figure 6, Input Amp										
Voltage Range(1)											
Positive Input		>0		+0.25mA x R_1	*		*	*		*	V
Negative Input		>0		-10	*		*	*		*	V
Current Range(1)		>0		+0.25	*		*	*		*	mA
Bias Current											
Inverting Input			20	100		*	*		*	*	nA
Noninverting Input			100	250		*	*		*	*	nA
Offset Voltage(2)			1	4		*	*		*	*	mV
Differential Impedance		300 || 10	650 ||10		*	*		*	*	kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		*	*		MΩ || pF
INPUT (F/V CONVERTER)	$V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9, Comparator										
Impedance (Comp In)		50 || 10	150 || 10		*	*		*	*		kΩ || pF
Logic "1"		+1.0		+V_{CC}	*		*	*		*	V
Logic "0"		-V_{CC}		±0.05	*		*	*		*	V
Pulse-width Range		0.1		150k/F_{MAX}	*		*	*		*	μsec
ACCURACY											
Linearity Error(3)	0.01Hz ≤ oper freq ≤ 10kHz		±0.005	±0.010(4)		*	*		*	*	% of FSR(5)
	0.1Hz ≤ oper freq ≤ 100kHz		±0.025	±0.05		*	*		*	*	% of FSR
	0.5Hz ≤ oper freq ≤ 500kHz		±0.05			*			*		% of FSR
Offset Error Input Offset Voltage(2)			1	4		*	*		*	*	mV
Offset Drift(6)			±3			*			*		ppm of FSR/°C
Gain Error(2)			5			*	*		*	*	% of FSR
Gain Drift(6)	f = 10kHz		±75			±50	±100		±70	±150	ppm/°C
Full Scale Drift (offset drift & gain drift)(6)(7)	f = 10kHz		±75			±50	±100		±70	±150	ppm of FSR/°C
Power Supply Sensitivity	f = DC, ±V_{CC} = 12VDC to 18VDC			±0.015			*			*	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, Logic "0"	I_{SINK} = 8mA	0	0.2	0.4	*	*	*	*	*	*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*		*	*	μA
Voltage, Logic "1"	External pull-up resistor required (see Figure 4)			V_{PU}			*			*	V
Pulse Width	For Best Linearity		0.25/F_{MAX}			*			*		sec
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			*			*	nsec
OUTPUT (F/V CONVERTER) V_{OUT}											
Voltage	I_O = 7mA	0 to +10			*			*			V
Current	V_O = 7VDC	+8			*			*			mA
Impedance	Closed loop			1			*			*	Ω
Capacitive Load	Without oscillation			100			*			*	pF
DYNAMIC RESPONSE											
Full Scale Frequency				500(8)	*			*			kHz
Dynamic Range		6			*			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		(9)			*			*		
Overload Recovery	< 50% overload		(9)			*			*		
POWER SUPPLY											
Rated Voltage			±15								V
Voltage Range		±11		±20					*		V
Quiescent Current		*	±5.5	±6.0		*	*		*		mA
TEMPERATURE RANGE											
Specification		0		+70	-25		+85	-55		+125	°C
Operating		-25		+85	-55		+125	-55		+125	°C
Storage		-25		+85	-65		+150	-65		+150	°C

*Specification the same as VFC32KP

NOTES:
1. A 25% duty cycle (0.25mA input current) is recommended where possible to achieve best linearity. Up to 50% duty cycle (0.5mA) is recommended above 200kHz.
2. Adjustable to zero. See Offset and Gain Adjustment section.
3. Linearity error is specified at any operating frequency from the straight line intersecting full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section. Above 200kHz, it is recommended all grades be operated below +85°C.
4. ±0.015% of FSR for negative inputs shown in Figure 7. Positive inputs are shown in Figure 6.
5. FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).
6. Exclusive of external components' drift.
7. Positive drift is defined to be increasing frequency with increasing temperature.
8. For operation above 200kHz up to 500kHz, see Discussion of Specifications and Installation and Operation sections.
9. One pulse of new frequency plus 1μsec.

ABSOLUTE MAXIMUM RATINGS

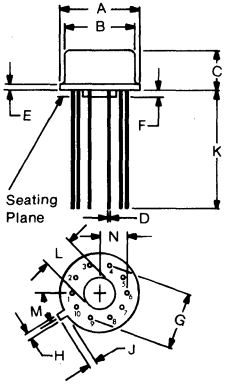
Supply Voltages	±22V
Output Sink Current (I_{FOUT})	50mA
Output Current (V_{OUT})	+20mA
Input Voltage, -Input	±Supply
Input Voltage, +Input	±Supply
Storage Temperature Range	
VFC32BM, SM	-65°C to +150°C
VFC32KP	-25°C to +85°C

MECHANICAL

VFC32BM, VFC32SM TO-100 PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

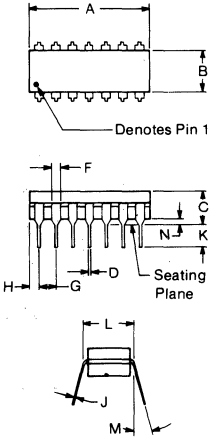
Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

VFC32KP EPOXY DUAL-IN-LINE

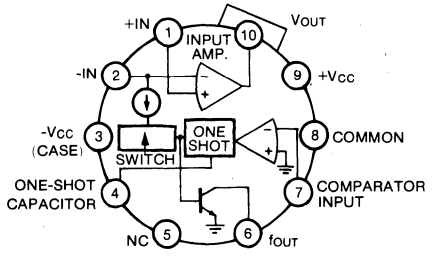
NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.660	.785	16.76	19.94
B	.220	.280	5.59	7.11
C	--	.200		5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.030	.095	0.76	2.41
J	.008	.015	0.20	0.38
K	.100	--	2.54	--
L	.300 BASIC		7.62 BASIC	
M	--	15°	--	15°
N	.020	.050	0.51	1.27

PIN CONFIGURATIONS

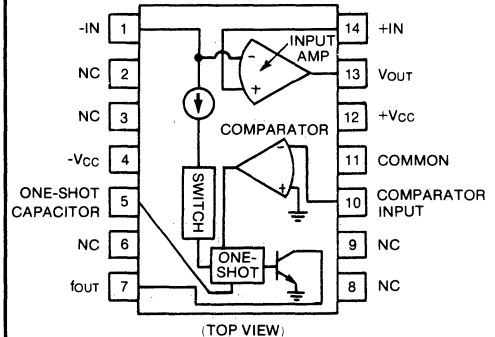
VFC32BM, VFC32SM
TO-100 PACKAGE



(TOP VIEW)

NC = NO INTERNAL CONNECTION.
EXTERNAL CONNECTION PERMITTED.

VFC32KP
EPOXY DUAL-IN-LINE PACKAGE



(TOP VIEW)

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (90% of full scale input or frequency and 0.1% of full scale called zero). Linearity is the true measure of voltage-to-frequency converter's performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. For a given full scale frequency, the linearity error decreases with decreasing operating frequency as shown in Figure 2. Also, best linearity is achieved at lower gains ($\Delta F_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC32 makes the device an excellent choice for use as the front end of A/D converters with 8- to 12-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire serial data transmission).

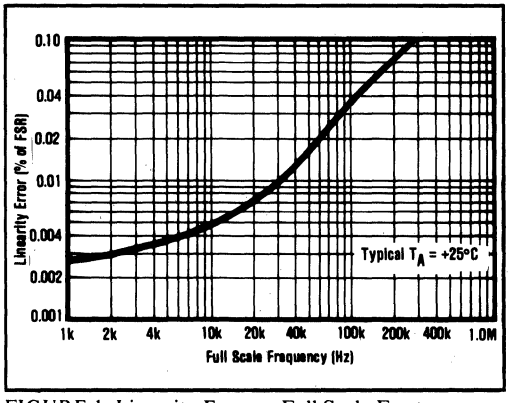


FIGURE 1. Linearity Error vs Full Scale Frequency. (25% Duty Cycle)

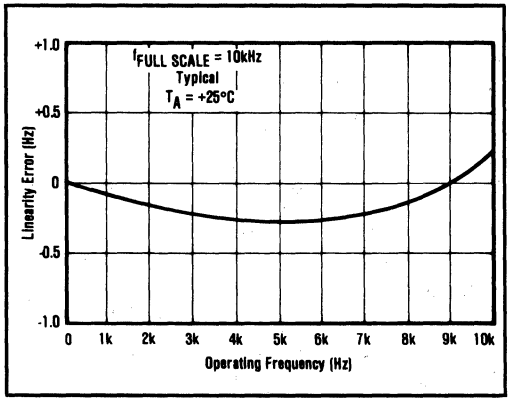


FIGURE 2. Linearity Error vs Operating Frequency. (25% Duty Cycle)

FREQUENCY STABILITY vs TEMPERATURE

The full scale frequency drift of the VFC32 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 100kHz, and this should be taken into account for specific applications. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC32. Above 200kHz, it is recommended all grades be operated below +85°C with higher duty cycle (up to 50%) and higher output transistor collector current (up to 15mA). Linearity will, however, be degraded.

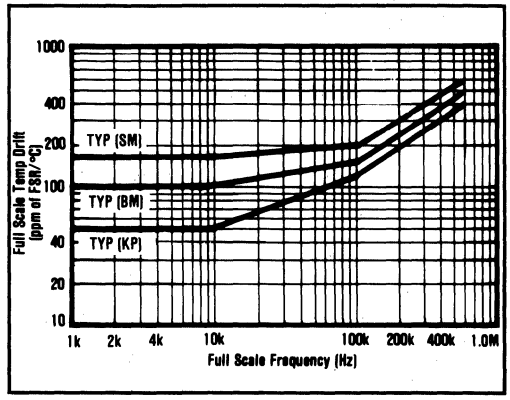


FIGURE 3. Full Scale Drift vs Full Scale Frequency. (25% Duty Cycle)

RESPONSE

Response of the VFC32 to changes in input signal level is specified for a full scale step, and is 1 microsecond plus 1 pulse of the new frequency. For a 10 volt input signal step with the VFC32 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 40 microseconds.

THEORY OF OPERATION

The VFC32 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage in Figure 4.

Essentially, the input amplifier acts as an integrator that produces a 2-part ramp. The first part is a function of the input voltage, and the second part dependent on the current sink. When a positive input voltage is applied at V_{IN}, a constant current will flow through the input resistor, causing the voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time, the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and integrating components. When the ramp reaches a voltage close to zero, the comparator will cause the one-shot to fire. The one-shot period is determined by an internal 7.5V reference and C_1. The f_{OUT} signal will then change logic

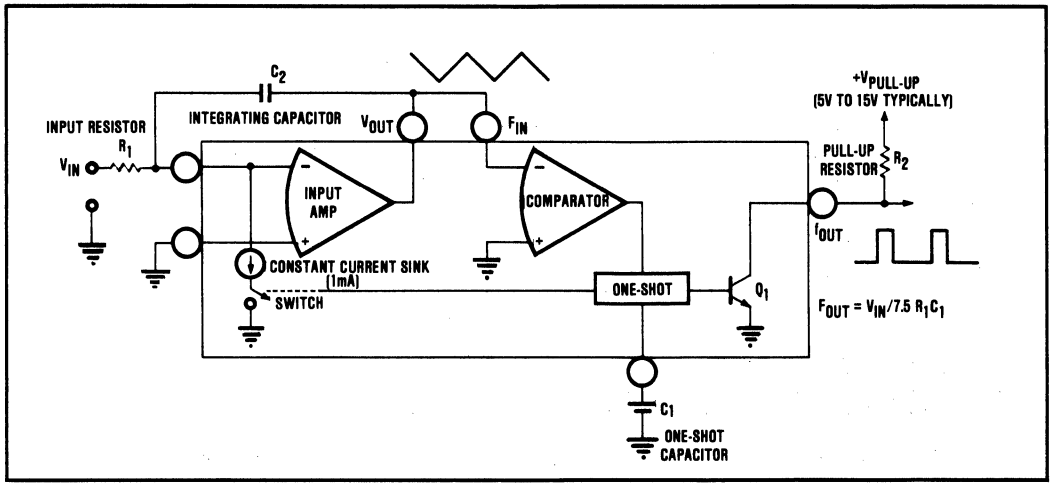


FIGURE 4. Functional Block Diagram of the VFC32.

states, going from a "0" to a "1", and the switch will close, enabling the constant current sink. The ramp voltage will then change direction and begin to ramp up. Since V_{IN}/R_1 is always set up to be less than 1mA, the current in the integrating capacitor will flow toward the summing junction, and the ramp voltage rate of change will be;

$$\frac{dV}{dt} = \frac{\frac{V_{IN}}{R_1} - 1mA}{C_2}.$$

Before the ramp voltage can saturate the input amplifier, the one-shot will reset, disabling the current sink, changing the output state back to logic "0", and restarting the cycle. Since the integrating capacitor C_2 affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to V_{IN}/R_1, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

To operate the VFC32 as a highly linear frequency-to-voltage converter, open the connection between V_{OUT} and f_{IN}, and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}, and a positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. For details see Installation and Operating Instructions.

The total VFC period is determined by the following equations, which is shown graphically in Figure 5.

$$f_o = \frac{1}{t}$$

$$t = t_1 + t_2 \text{ and } i = c\, dv/dt$$

$$t = \Delta V_{OUT}\, t_1 \frac{C_2}{V_{IN}/(R_1)} + \Delta V_{OUT}\, t_2 \frac{C_2}{V_{IN}/(R_1) - 1mA}$$

and:

$$-\Delta V_{OUT} t_1 = +\Delta V_{OUT} t_2$$

$$t_2 = C_1 \frac{7.5V}{1mA}$$

The equations reduce to:

$$f_o = \frac{V_{IN}}{7.5(R_1)\, C_1}$$

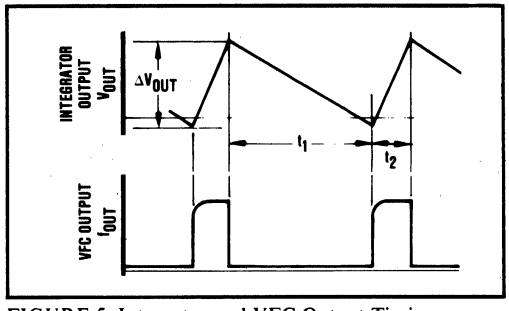


FIGURE 5. Integrator and VFC Output Timing.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). It is measured at the full scale input voltage, which gives the full scale output frequency, F_{FS}.

$$D = \frac{t_2}{t_1 + t_2} = PW \times F_{FS}$$

$$PW = \frac{D}{F_{FS}}$$

Duty cycle is related to the maximum input current and the 1mA (nominal) current sink. By reducing the equations for t_2 and f_o:

$$D = \frac{V_{IN}\ max/(R_1)}{1mA} = \frac{I_{IN}\ max}{1mA}$$

A 25% duty cycle or less is recommended to achieve the best linearity. This corresponds to a maximum input current of 0.25mA. However, for frequencies above 200kHz a higher duty cycle (up to 50%) will provide more stable high temperature operation at a sacrifice in linearity.

In general, designs with the VFC32 include: (1) Choosing F_{MAX}, (2) Choosing the duty cycle (D = 0.25 typically), (3) Determining the one-shot PW, and (4) Calculating C_1, C_2, R_1, R_2, and R_3.

INSTALLATION AND OPERATING INSTRUCTIONS

The VFC32 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

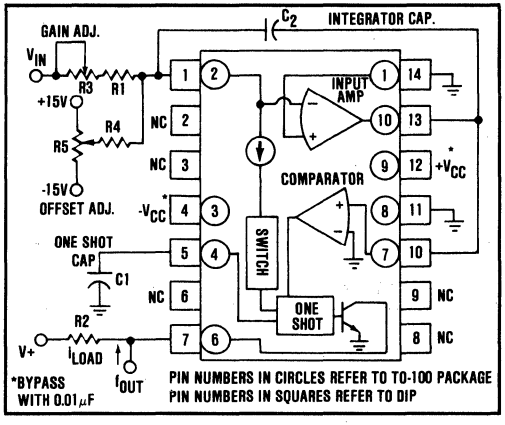


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

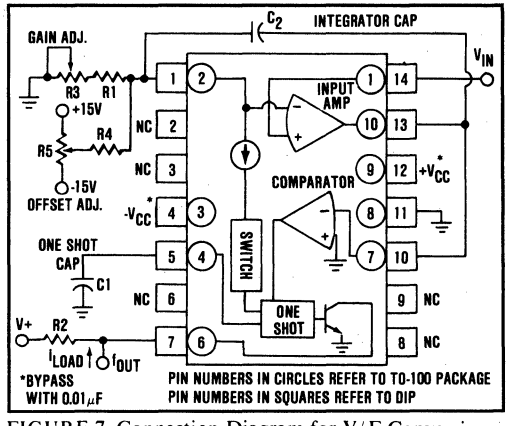


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

Differential inputs are also possible (in Figure 7 lift ground on R_3 and drive R_3 and pin 14 differentially). Note, no CMR will be present.

The full scale frequency and full scale input voltage (current) are established by the selection of values for R1, C2, and C1. Most applications will require a gain adjustment pot (R3), but the offset adjust network (R4, R5) can be omitted if input offset voltages of 1mV to 4mV can be tolerated. R2 is an output pull up resistor and its value depends on the pull up voltage and output drive requirements.

EXTERNAL COMPONENT SELECTION CRITERIA

One-shot Capacitor, C1. This capacitor determines the duration of the output pulse, and is a function of the full scale frequency, according to this equation:

$$C1(pF) = [33 \times 10^6 / f_{MAX}] - 30$$

Above 425kHz use 47pF

Select the closest standard value to the capacitance given by the equation. The initial tolerance of this capacitor is not critical since R3 will be adjusted to remove initial gain errors. The temperature drift is critical, since it will add directly to the errors in the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize the parasitic capacitance at this connection to the VFC32 and C1 should be mounted as close as possible. Figure 8 shows pulse width and FS frequency for various values of C1.

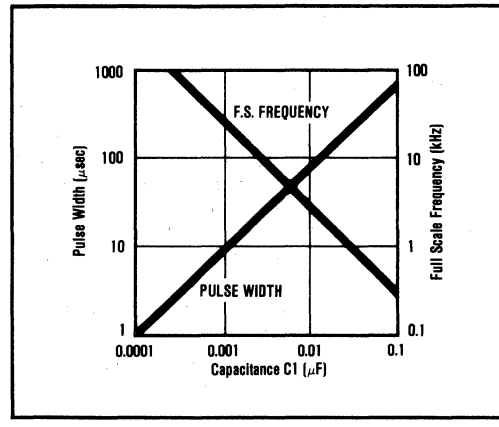


FIGURE 8. Output Pulse Width (D = 0.25) and Full Scale Frequency vs External One-shot Capacitance.

Input Resistor R1 and R3. R1 and R3 determine the magnitude of the current which charges the integrator capacitor. It is a function of the full scale input voltage, according to this equation for 25% duty cycle.

$$R1\ (k\Omega)\ [90\% - \%\ tolerance\ C1] \times V_{IN}\ max/0.25mA$$

R1 is scaled down by [1-(initial C1 tolerance + 0.1)] to allow the addition of a series gain adjusting pot, R3.

$$R_3\ (k\Omega) = V_{IN}\ max/0.25mA - R_1$$

R1 should have a very low temperature coefficient since this drift adds directly to the errors in the transfer function. If the input signal is a current rather than a voltage, R1 and R3 should be replaced with a short circuit, and the full scale input current should be 0.25mA (25% duty cycle). Removal of gain error then requires adjustment of C1.

Integrating Capacitor C2. C2 is a function of the full scale frequency, according to this equation:

$$C_2(\mu F) = 10^2/f_{MAX} \text{ below } 100kHz$$
$$0.001\mu F \text{ min above } 100kHz$$

Select the closest standard value to the capacitance given by the equation. The initial tolerance and temperature stability are not critical since these errors do no affect the transfer function. Since the leakage current of the capacitor introduces a gain error, select a capacitor with leakage that is small compared to the full scale input current e.g., 0.25mA. A mylar type is recommended.

Output Pull Up Resistor R2. The open collector output can sink up to 8mA and still be TTL-compatible. Select R2 according to this equation:

$$R_2 \text{ min } (\Omega) = V_{PULLUP}/(8mA - i_{LOAD})$$

A 10% carbon composition resistor is suitable for use as R2.

Above 200kHz up to 500kHz it is recommended higher duty cycles up to 50% (I_{IN}=0.5mA) and a pull-up resistor that permits 15mA to flow in the output transistor be used. At this speed, capacitive loading should be minimized to 100pF or less to allow the output voltage time to rise to logic one. Due to the large collector current, the logic zero may rise above +0.4V. This may require an interface circuit such as diode clamp or voltage comparator for coupling to TTL inputs. Note, that linearity will degrade. Also, it is recommended to stay below +85°C at high frequencies.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC32 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C3 to make t <0.1tp (See Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero, to insure that the input signal at pin 10 crosses the threshold. Errors are nulled following the procedure given on this page, using 0.001X full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC32 is 0.02% of FSR/% max. To maintain ±0.02% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Trimming Components R3, R4, R5.

R5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R4 can be a 20% carbon composition resistor with a value of 10MΩ.

R3 nulls the gain errors of the converter and compensates for initial tolerances of R1 and C1. Its total resistance should be at least 20% of R1, if R1 is selected 10% low (see R1 equation). Its temperature coefficient should be no greater than five times that of R1, to maintain a low drift of the R3 - R1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 X full scale.
2. Adjust R5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

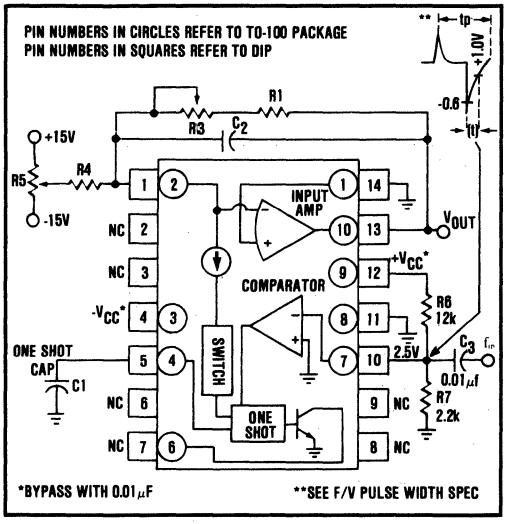


FIGURE 9. Connection Diagram for F/V Conversion.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1

$C_1 = [33 \times 10^6/f_{MAX}] - 30$
$= [33 \times 10^6/100kHz] - 30$
$= 300pF$

Choose a 300pF NPO ceramic capacitor with ±1% tolerance.

Selecting R_1 and R_3 (for D=0.25; for D=0.5 use 0.5mA)

$R_1 = [90\% - \%$ tolerance of $C_1] \times V_{IN}$ max / 0.25mA
$= [0.9 - 0.1] \times 10V/0.25mA$
$= 32k\Omega$

Choose a 32.4kΩ metal film resistor with ±1% tolerance.

$R_3 = 10V/0.25mA - R_1$
$= 8k\Omega$

Choose a 10kΩ cermet potentiometer

Selecting C_2

$C_2 = 10^2/F_{MAX}$
$= 10^2/100kHz$
$= 0.001\mu F$

Choose a 0.001μF mylar capacitor with ±5% tolerance.

Selecting R_2

$R_2 = V_{PULLUP}/(8mA - i_{LOAD})$
$= 5V/(8mA - 1.6mA)$, one TTL-load = 1.6mA
$= 781\Omega$

Choose a 750Ω 1/4-watt carbon composition resistor with ±5% tolerance.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC32 ideal for a variety of VFC applications. High accuracy allows the VFC32 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 12-bits.

Figures 10 - 14 show typical applications of the VFC32.

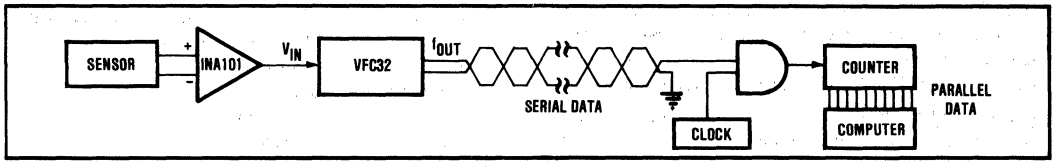


FIGURE 10. Inexpensive A/D with Serial Transmission of Digital Data.

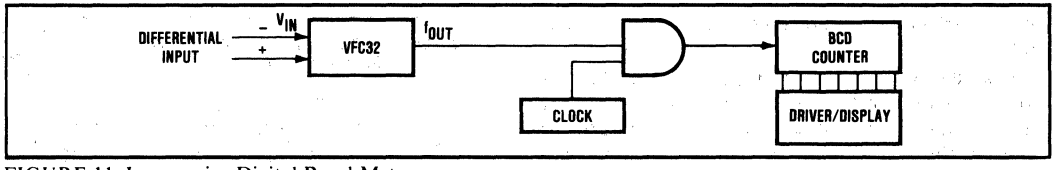


FIGURE 11. Inexpensive Digital Panel Meter.

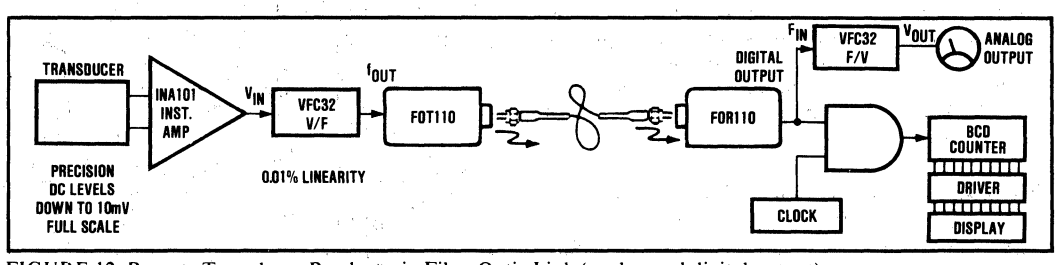


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

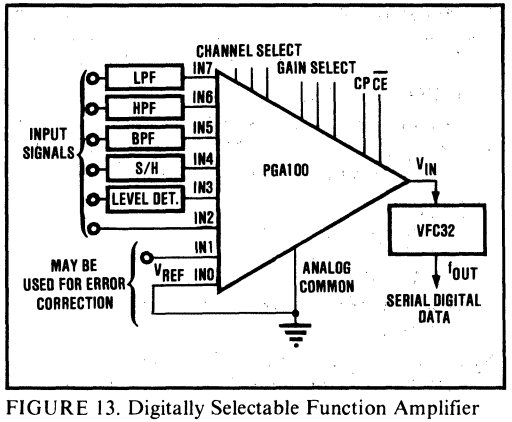


FIGURE 13. Digitally Selectable Function Amplifier with Serial Data Output.

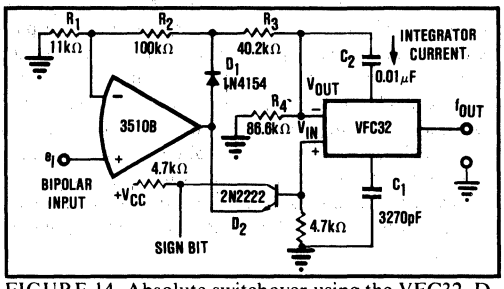


FIGURE 14. Absolute switchover using the VFC32. D_1 and D_2 switch on alternately as polarity of input signal changes, thus maintaining direction of integrator current. V/F converter cannot distinguish between signal polarities of the same magnitude and so generates the same frequency for both.

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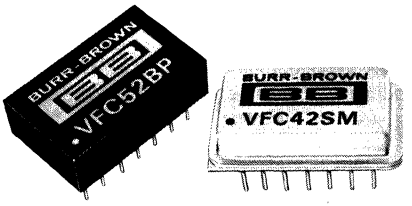


VFC42
VFC52

VOLTAGE-TO-FREQUENCY AND FREQUENCY-TO-VOLTAGE CONVERTER

FEATURES

- V/F OR F/V CONVERSION
- TWO FREQUENCY RANGES
  10kHz (VFC42)
  100kHz (VFC52)
- LOW NONLINEARITY
  ±0.01% max (VFC42)
  ±0.05% max (VFC52)
- MINIMAL EXTERNAL COMPONENTS REQUIRED
  Add only one external resistor for V/F operation
- 6 DECADE DYNAMIC RANGE
- OUTPUT DTL/TTL/CMOS COMPATIBLE

DESCRIPTION

VFC42 and VFC52 are hybrid microcircuits which can be connected as voltage-to-frequency or frequency-to-voltage converters. They provide a simple, low cost method of converting analog signals into an equivalent digital form. The digital output is an open collector which can be made compatible with DTL, TTL, or CMOS logic. The output is a train of constant-amplitude, constant-width pulses whose repetition rate is proportional to the amplitude of the analog input voltage. In the frequency-to-voltage mode the pulses become the input and the proportional DC voltage, the output.

Both models are offered in epoxy (-25°C to +85°C) and hermetic metal (-25°C to +85°C and -55°C to +125°C) 14-pin DIP packages.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-390

THEORY OF OPERATION

VFC42 and VFC52 hybrid voltage-to-frequency converters provide a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. To understand the circuit's operation see Figure 1.

The input amplifier is connected in an integrator configuration. When a positive input voltage is applied at V_{IN}, a constant current flows through the input resistor causing voltage at f_{IN} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_2$. During this time the constant current sink is disabled by the switch. When the ramp reaches zero volts, the comparator causes the one-shot to fire. The f_{OUT} signal then changes states, going from logic 0 to logic 1 and the switch closes, enabling the constant current sink. Ramp voltage then changes direction and begins to ramp up. Since V_{IN}/R_1 is always set to be less than 1mA, current in the integrating capacitor flows toward the summing junction and ramp voltage range of change will be

$$\frac{dV}{dt} = \frac{\left(\frac{V_{in}}{R_1}\right) - 1mA}{C_2}$$

Before the ramp voltage can saturate the input amplifier, the one-shot resets, disabling the current sink, changing the output state back to logic 0 and restarting the cycle.

To operate VFC42 and VFC52 as highly linear frequency-to-voltage converters, open the connection between V_{OUT} and f_{IN} and connect V_{IN} to V_{OUT}. The input frequency should be coupled through a capacitor to f_{IN}. A positive output voltage proportional to f_{IN} will be generated at the V_{OUT} connection. An external capacitor connected between pins 13 and 14 (paralleling C2) should be added to reduce output ripple. Refer to Operating Instructions, page 5, for detailed information on F/V operation.

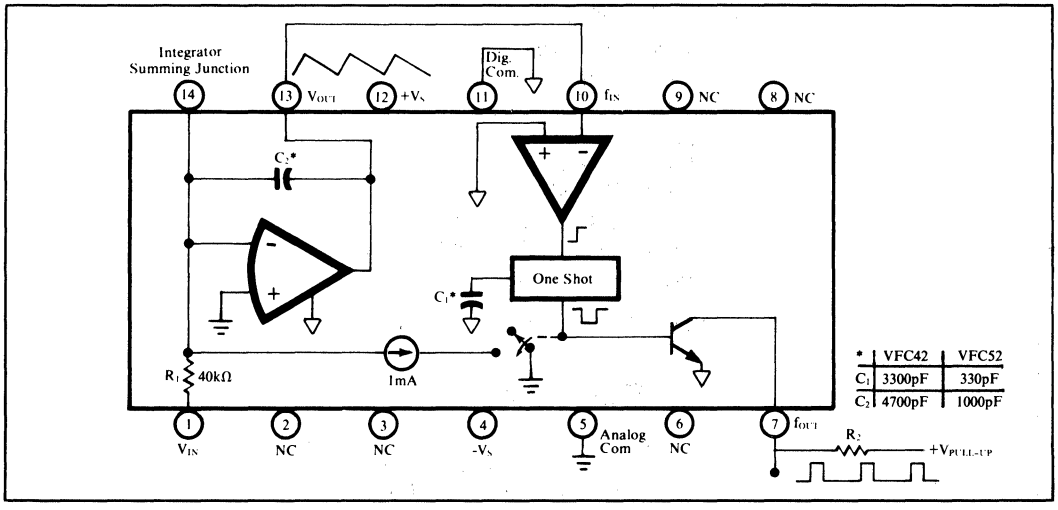


FIGURE 1. Functional Block Diagram

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity, the maximum deviation of the actual transfer function from a straight line drawn between the end points (full scale input and zero input), is the true measure of a VFC's performance and is a function of full scale frequency. The high linearity of VFC42 and VFC52 makes these devices an excellent choice for use in A/D converters with 10 (0.05%) and 12 bit (0.012%) accuracy and for highly accurate analog data transfer over long lines in noisy environments.

FREQUENCY STABILITY VS TEMPERATURE

Frequency stability vs temperature is expressed as parts per million of full scale range per °C. Since frequency drift is a function of the specified temperature range, the "SM" models will meet the lower drift specifications of the "BM" models over the narrower -25°C to +85°C temperature range. Error sources do not drift linearly over temperature, consequently the units drift much less at higher temperatures.

RESPONSE TIME

Response time of VFC42 and VFC52 to input signal level changes is specified for a full scale step and is 1 μsec plus 1 period of the new frequency. Typical settling time to within rated linearity for a positive input voltage step of +10V is 101 μsec for VFC42 and 11 μsec for VFC52.

ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C and ±15VDC power supplies unless otherwise noted.

MODEL	VFC42			VFC52			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Full Scale Frequency		10			100		kHz
INPUT							
Analog Input (V/F)							
Voltage Range	0		+10	0		+10	V
Current Range	0		+0.25	0		+0.25	mA
Input Bias Current (pin 14)							
Inverting Input		20	100		20	100	nA
Input Offset Voltage							
(trimmable to zero)		100	200		100	200	μV
Input Impedance (pin 1)	32	40	48	32	40	48	kΩ
Frequency Input (F/V) (pin 10)							
Logic Levels							
Logic "0"	$-V_{CC}$		-0.6	$-V_{CC}$		-0.6	V
Logic "1"	+1.0		$+V_{CC}$	+1.0		$+V_{CC}$	V
Pulse Width Range (t_2, Fig. 6)	0.1		15	0.1		1.5	μsec
Impedance	1 ‖ 10	1.2 ‖ 10		1 ‖ 10	1.2 ‖ 10		MΩ ‖ pF
TRANSFER CHARACTERISTICS							
Transfer Functions	$f_{OUT} = V_{IN}$ (1.00 x 10^3) $V_{OUT} = f_{IN}$ (10.0 x 10^{-4})			$f_{OUT} = V_{IN}$ (1.00 x 10^4) $V_{OUT} = f_{IN}$ (10.0 x 10^{-5})			Hz VDC
Accuracy							
Full Scale Gain							
(adjustable to zero)		0.1	0.2		0.1	0.2	%
Linearity Error							
0.01Hz ≤ F ≤ 10kHz		0.005	0.01				% of FSR[1]
0.1Hz ≤ F ≤ 100kHz					0.025	0.05	% of FSR
Offset Error (pin 1)		0.001	0.002		0.001	0.002	% of FSR/%
Power Supply Sensitivity[2]		0.0015	0.002		0.0015	0.002	% of FSR/%
Temperature Stability							
Analog Input							
Full Scale Drift (gain & offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Offset Drift							
Grade: BP		±1	±3		±1	±3	ppm of FSR/°C
BM		±1	±3		±1	±3	ppm of FSR/°C
SM		±1	±3		±1	±3	ppm of FSR/°C
Frequency Input							
Full Scale Drift (gain & offset)							
Grade: BP (hot/cold)[3]		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
BM		±15/±50	±30/±100		±20/±50	±30/±150	ppm/°C
SM		±30/±60	±50/±100		±30/±60	±50/±150	ppm/°C
Dynamic Response							
Settling Time to within linearity specification for full scale input step	1 period of new frequency + 1μsec			1 period of new frequency + 1μsec			
Overload Recovery Time	1 period of new frequency + 1μsec			1 period of new frequency + 1μsec			
OUTPUT							
Voltage Output							
Voltage Range	0 to +10			0 to +10			V
Output Current	+10			+10			mA
Output Impedance (closed loop)			1			1	Ω
Capacitive Load			100			100	pF
Frequency Output (open collector)							
Pulse Characteristics							
Logic "1"			$+V_{PULL-UP}$			$+V_{PULL-UP}$	V
Logic "0" (at I_o ≤ -8mA	0		+0.4	0		+0.4	V
Pulse Width	20	25		2.0	2.5		μsec
Output Sink Current							
(Logic "0", ≤ 0.4V)			8			8	mA
Output Leakage Current							
(Logic "1")			100			100	nA
Fall Time							
I_{OUT} = -5mA, C_{LOAD} = 500pF			400			400	nsec
POWER SUPPLY REQUIREMENTS							
Rated Supplies		±15			±15		V
Supply Range	±9		±20	±9		±20	V
Supply Drain (independent of operating frequency)		±5.5	±6.5		±5.5	±6.5	mA

ELECTRICAL SPECIFICATIONS CONTINUED:

Specifications at T_A = +25°C and ±15VDC power supply unless otherwise noted.

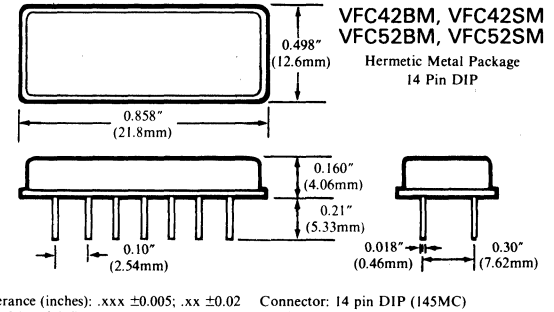
MODEL	VFC42			VFC52			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE							
Specification							
Grade: BP, BM	-25		+85	-25		+85	°C
SM	-55		+125	-55		+125	°C
Operating							
Grade: BM, SM	-55		+125	-55		+125	°C
BP	-55		+100	-55		+100	°C
Storage							
Grade: BP, BM, SM	-55		+125	-55		+125	°C

TABLE I. Electrical Specifications

ABSOLUTE MAXIMUM RATINGS above which unit may be damaged.	
Supply Voltages	±22V
Output Sink Current (F_{output})	50mA
Output Current (V_{output})	+20mA
Input Voltage, Pin 14	±Supply
Input Voltage, Pin 1	±Supply
Storage Temperature Range	
Grade: BP, BM, SM	-55°C to +125°C

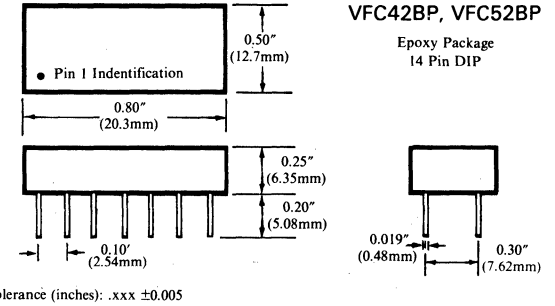
NOTES:
1. % of FSR = % of Full Scale Range.
2. Rated at full scale input and ±15V supplies.
3. Hot = +20°C to highest rated temperature; cold = lowest rated temperature to +20°C.

MECHANICAL SPECIFICATIONS



Tolerance (inches): .xxx ±0.005; .xx ±0.02 Connector: 14 pin DIP (145MC)
Case Material: Base - gold-plated kovar Cap - nickel-plated kovar or steel
Pin material and plating compositions: Conforms to Mil-Std-883, Method 2003 (solderability) except paragraph 3.2 (aging). Hermeticity: Conforms to Mil-Std-883, Method 1014,Condition C, Step 1, Fluorocarbon (gross leak) and Condition A, Helium, 5 x 10^{-7}cc/sec (fine leak)

FIGURE 2. Hermetic Metal Package Specifications



Tolerance (inches): .xxx ±0.005
.xx ±0.02
Connector: 14 pin DIP (145MC)
Case Material: epoxy

Pin material and plating composition:
Conform to Method 2003 (solderability)
of Mil-Std-883 (except paragraph 3.2).

FIGURE 3. Epoxy Package Specifications

CONNECTION DIAGRAMS

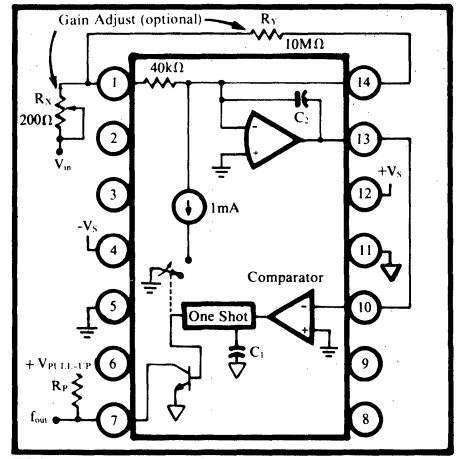


FIGURE 4. Connection Diagram for V/F Operation

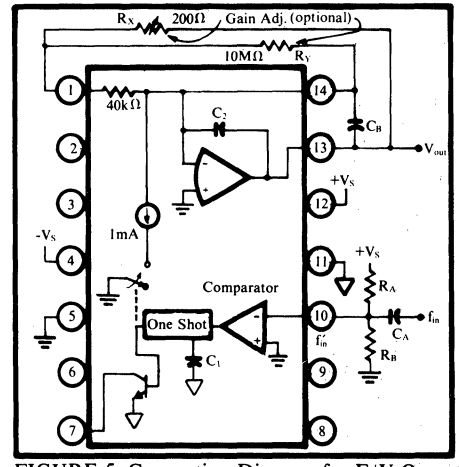


FIGURE 5. Connection Diagram for F/V Operation

OPERATING INSTRUCTIONS

VFC42 and VFC52 can be connected for either V/F or F/V operation. Only one external component, the output pull-up resistor, is required for V/F operation. F/V operation requires the pull-up resistor and input biasing components. Gain error is the most significant error in either configuration and may be nulled out with the optional trim circuit (R_X and R_Y). The offset error is laser trimmed at the factory and no external adjustment is required.

Power Supply Consideration: Power supplies stable to within ±1% are recommended to maintain conversion accuracy. Each supply should be by-passed with 0.01μF capacitors located as close to the VFC as possible.

VOLTAGE-TO-FREQUENCY OPERATION

Calculating the Value of Pull-Up Resistor, R_P: The open collector output can be used to drive DTL, TTL, CMOS or discrete circuits. The maximum collector current allowed for TTL circuits in logic 0 is 8mA. R_P may be calculated by this equation:

$$R_P \text{ min} = V \text{ pull-up}/(8mA - i_{LOAD}).$$

A 10% carbon composition resistor is suitable for this purpose. The collector current may be as great as 30mA if a logic 0 voltage of 1.0V is tolerable.

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Figure 4. Apply positive full scale voltage to the input and adjust R_X until 10kHz ±1Hz (VFC42) or 100kHz ±10Hz (VFC52) is obtained at f_{OUT}. R_X and R_Y should have temperature coefficients of < 500ppm. These external components will add less than 5 ppm/°C to temperature drift.

FREQUENCY-TO-VOLTAGE OPERATION

Input Characteristics: VFC42 and VFC52 can be connected as frequency-to-voltage converters as shown in Figure 5. f_{IN} should be a positive pulse train with minimum pulse width of 1.0μsec and rise and fall times of ≤ 300nsec. The input train (f_{IN}) is differential and applied to the input of the comparator (pin 10). Refer to Figure 6. Threshold voltage of the comparator lies between -0.6 and +1.0V. When comparator input is less than -0.6V it triggers the one shot.

Selecting R_A, R_B, and C_A: Input components R_A, R_B and C_A are selected so that the trigger voltage (V_T) is more negative than -0.6V and transition time (t_2) is between 0.3 and 15 μsec for VFC42 and between 0.3 and 1.5 μsec for VFC52. Table II gives values for input components for several common signal sources. Values for R_A, R_B and C_A may be selected by the user when input signal characteristics differ from those listed. Conditions described above for trigger voltage and transition time must be observed.

Equations to calculate trigger voltage and transition time are:

$$V_T = V_B + V_{in}(e^{-t_i/\tau} - 1)$$

$$t_2 = -\tau \ell n \left[\frac{1 - V_B}{V_{in}(e^{-t_i/\tau} - 1)} \right]$$

V_B = Bias voltage on pin 10
V_{in} = Input pulse amplitude
t_1 = Input pulse width
τ = Time constant of R_A, R_B, C_A as connected

If input pulse amplitude is greater than $+V_S$ - 1V, a voltage larger than $+V_S$ will be applied to pin 10. Since this may damage the unit, a diode connected across R_A with the cathode tied to $+V_S$ is required.

Output Characteristics: Selecting C_B: Output ripple voltage amplitude is inversely proportional to the input frequency and to the value of the integrating capacitance, $C_2 + C_B$. Ripple, therefore, will be greatest at low frequencies and at small values of $C_2 + C_B$. Conversely, time required for the output to settle is directly proportional to the value of $C_2 + C_B$ and is least with small values of $C_2 + C_B$. There is, therefore, a trade-off between output ripple amplitude and output settling time.

Because ripple amplitude is greatest at lowest input frequency it is at this point where the trade-off will usually be made. Ripple voltage and integrating capacitance value are related in this manner:

$$C_B = \frac{-(25 \times 10^{-6})t_{sec}}{\ell n \left[1 - \frac{V_{Ripple}}{30V}\right]} \text{ farads}$$

where t is equal to 25 μsec in the VFC42 and 2.5 μsec in the VFC52 and C is the integrating capacitance.

Input Type	V_{INPUT} (V)		V_{BIAS} (V)	VFC42			VFC52		
	Low	High		R_A (kΩ)	R_B (kΩ)	C_A (pF)	R_A (kΩ)	R_B (Ω)	C_A (pF)
TTL	≤+0.4	≥ +2.8	+1.1	12	1.0	1000	8.2	680	680
5V CMOS	≤+0.5	≥ +4.5	+1.2	18	1.6	2200	9.1	820	680
10V CMOS	≤+1.0	≥ +9.0	+1.1	12	1.0	2200	6.2	510	680
15V CMOS	≤+1.5	≥+13.5	+1.1	12	1.0	2200	6.2	510	680

TABLE II. F/V Input Component Selection.

Calculating output response time versus integrating capacitance is an iterative process and is plotted in Figure 7. These curves are for zero to full scale input frequency transitions. If faster response time with lower ripple voltage is desired, a low pass filter can be connected in series with the output

Gain Adjustment Procedure: Connect R_X and R_Y as shown in Figure 5. Apply full scale frequency to the input and adjust R_X until full scale voltage is +10V ±1mV (discounting ripple). R_X and R_Y should have temperature coefficients of < 500 ppm. These external components will add less than 5 ppm/°C to temperature drift.

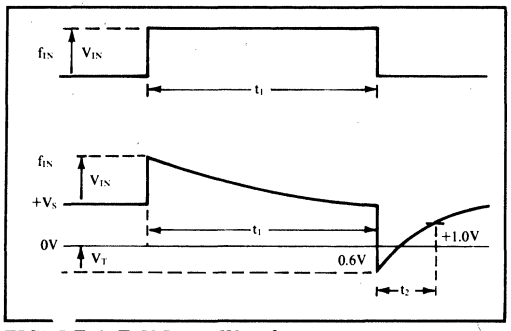


FIGURE 6. F/V Input Waveforms

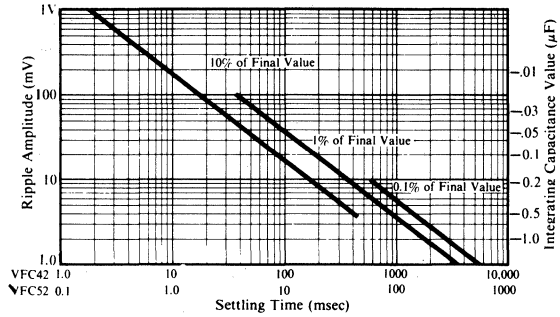


FIGURE 7. F/V Mode Output Settling Time vs. Ripple Voltage Amplitude for Full Scale Frequency Change

APPLICATION

VFC42 and VFC52 can be used to convert analog data into a digital pulse train for transmission over long lines through high EMI environments. Illustrated in Figure 8 is a V/F, F/V combination that can be used to transmit analog data of 0 to +10V span over a 100Ω shielded, twisted-pair. The voltage ripple amplitude at the output will be 10mV for a 10V output and the settling time for a full scale 0 to +10V change is 60 milliseconds.

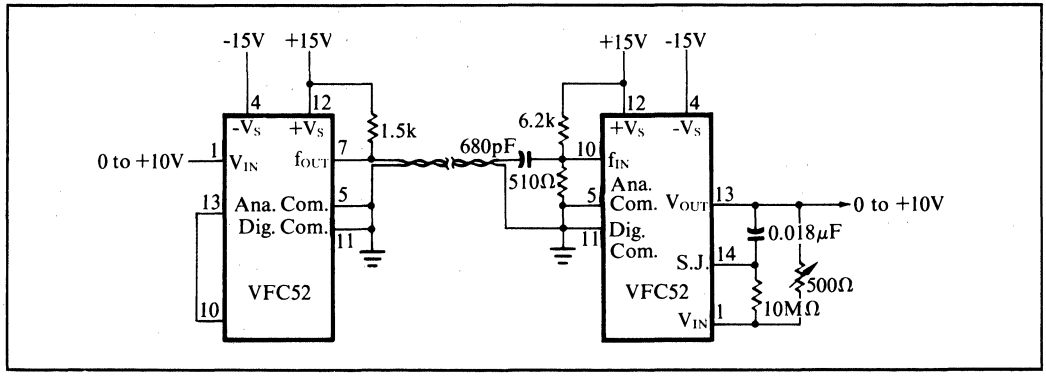


FIGURE 8. V/F, F/V Data Transmission Circuit

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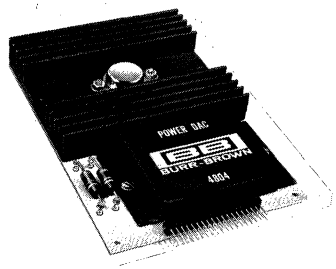


4804

Low Cost 12-BIT POWER DAC

FEATURES

- DIGITALLY PROGRAMMABLE VOLTAGE SOURCE ±30VDC, 1A Continuous Output
- RESISTOR-PROGRAMMED VOLTAGE RANGE AND CURRENT LIMIT
- LOW COST
- INPUT STORAGE REGISTER
- ±1/2LSB MAXIMUM NONLINEARITY

DESCRIPTION

The 4804 Power DAC offers versatility and low cost in automatic test equipment and process control applications. The output range is ±30VDC at 1A with built in current limiting at ±1.2A. By adding one external resistor, you can select any full scale output range less than ±30VDC and still maintain 12-bit resolution. Also, the current limiting can be varied by changing the value of two easily accessible resistors. The package was designed for mounting on a PC card and can dissipate up to 20W internally in free air with no external heat sinking required.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-335A

DETAILED DESCRIPTION

GENERAL

The 4804 consists of a 12-bit storage register with strobed inputs, a 12-bit digital-to-analog converter, and a power output stage. By changing the input code according to Table I, the output voltage may be varied between ±30V with output currents up to 2A continuous. The maximum internal power dissipation for various output conditions is described in Figure 3 and 5. Care must be taken not to exceed the power dissipation limits for the thermal environments described in the figures.

No external adjustments or components are required to achieve the specified accuracy. If improved performance is required, two adjustments will null the offset and gain errors. The procedures for adjusting these parameters are described on page 6-385.

To minimize noise levels in the 4804 the analog and digital signal returns are not internally connected. For proper operation, these two grounds must be externally connected together.

STORAGE REGISTER

The storage register consists of 12 integrated-circuit, positive-edge-triggered flip-flops utilizing TTL circuitry. The logic levels at the register inputs are transferred to the D/A converter on the positive-going edge of the strobe pulse. Strobing occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the strobe input is at either the high or low level, the inputs to the register have no effect on the D/A converter inputs. The strobe and register are fully compatible with most TTL or DTL circuits.

DIGITAL-TO-ANALOG CONVERTER

The D/A converter stage accepts the digital output from the storage register and converts it into a bipolar analog signal according to Table I.

To reduce gain and offset errors below the specified values, OFFSET ADJUST and GAIN ADJUST trim points are provided. Follow the procedure shown on 6-385.

POWER AMPLIFIER

The power amp stage buffers the D/A converter signal and provides the power output capability. Connecting the ±30V RANGE pin to the output will preset the full scale range to ±30V, giving the transfer function described in Table I; i.e. 1 LSB = 14.65mV. R_F and R_S were selected for optimum temperature stability to minimize gain drift errors, and the offset of the Power Amplifier has been nulled at the factory. By connecting a resistor between the V_{OUT} RANGE ADJUST pin and the output, a variety of full scale ranges can be selected while maintaining 12-bit resolution.

For optimum stability, the external resistor should have a T.C. which is less than ±10ppm/°C. The ±35V inputs to the power amplifier may be reduced if full scale ranges less than ±30V are desired. To maintain the best accuracy, these supplies should not be reduced below ±15V. Since the 4804 output current is derived from the ±35V power inputs, the current-carrying capability of these power supply connecting leads should be considered.

R_P and R_M determine the output positive and negative current limits, respectively, of the output. They have been preselected for current limiting of ±1.2A, typ. The current limiting can be changed by replacing R_P and R_M with other values according to the following formula:

$$R = \frac{1.2V}{I_{current\ limit}}$$

It is not necessary that R_P and R_M be the same value. Since the output current of the 4804 flows through these resistors, the power dissipation of R_P and R_M should be considered. Both resistors are stud mounted for easy accessibility.

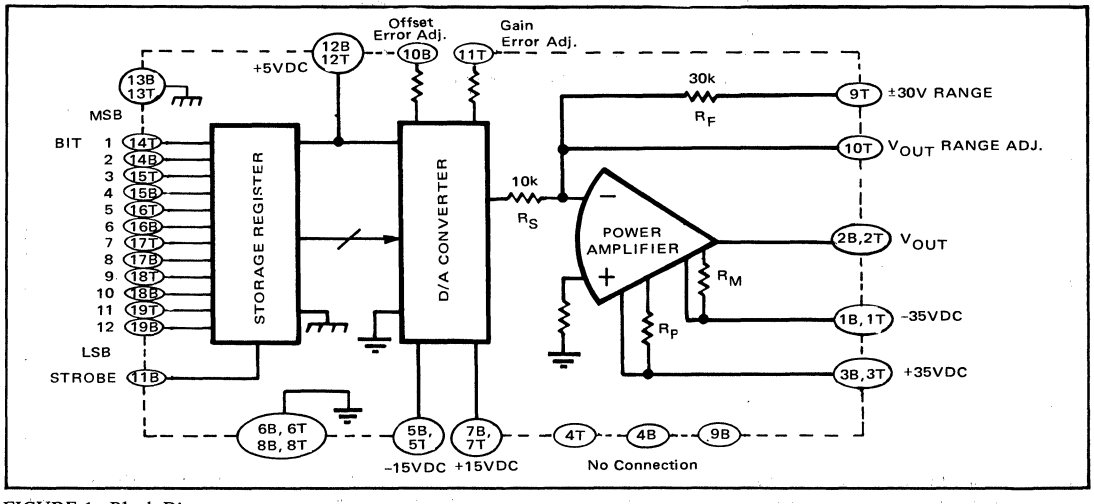


FIGURE 1. Block Diagram

SPECIFICATIONS

Typical at 25°C, rated power supplies, and V_{out} range = ±30 unless otherwise noted.

ELECTRICAL

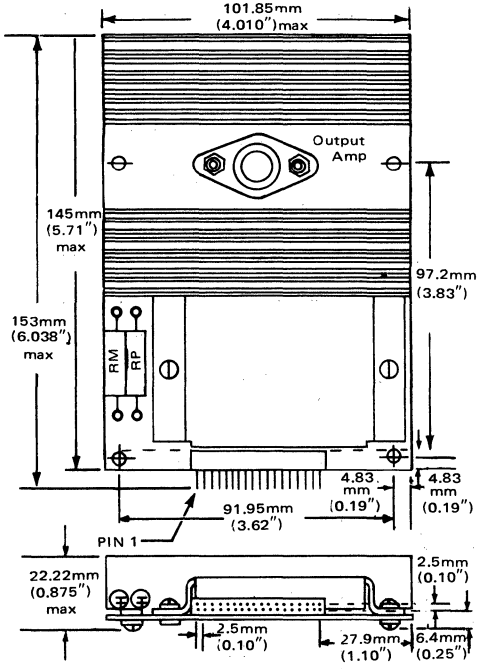
INPUT	
Resolution	12 bits
Logic levels (TTL/CMOS Compatible)	
Logical "1"	$+2V < e_{in} < +5.5V$ @ ≤ +0.1mA
Logical "0"	$0V < e_{in} < +0.8V$ @ ≤ -0.36mA
Digital Input Coding	offset binary (see Table I.)
TRANSFER CHARACTERISTICS	
TOTAL ACCURACY	
V_{out} Range = ±30V	±0.05% of reading
Individual Error Contributors	
Linearity Error (0°C to +70°C)	±½LSB max
Differential Linearity Error	±½LSB max
Output Offset Voltage	±3mV max
Drift (0°C to +70°C)	
Gain	±50ppm/°C max
Output Offset Voltage	±70μV/°C max
Differential Linearity	±2ppm/°C
Power Supply Sensitivity	
+15V Supply	2mV/V }
-15V Supply	2mV/V }
+ 5V Supply	6mV/V } for V_{out} = ±30V range
±35V Supplies	400μV/V }
Settling Time (to within 0.01% of final value for any input change)	100μsec max
OUTPUT	
Voltage Range @ I_{out} = 1.0A	±29.985V (= 30V -1LSB)
Output Current	(see Figure 5 and Note 1.)
Factory Adjusted Output Current Limit	1.2A typ
Output Resistance	1Ω max
POWER SUPPLY REQUIREMENTS	
Rated Voltages	±15VDC, +5VDC, ±35VDC
Power Supply Operating Ranges	±5%
Supply Drain	
±15V	±25mA
+5	+80mA
±35V	±40mA ±output current
TEMPERATURE RANGE	
Specification	0°C to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C

NOTE 1: Output amplifier is capable of sourcing or sinking 2 amps continuously. Resistors R_M and R_P have been selected to current limit the output current to ±1.2 A typ. To increase I_{out} capability, or modify the current limit setting, replace R_M and R_P according to instructions on page 6-382. Internal power dissipation should be considered, especially at low output voltages.

ABSOLUTE MAXIMUM RATINGS

+5V Supply	+7V
±15V Supplies	±20V
±35 Supplies	±40V
Digital Inputs	+7.0V with +5V supply = +7V
Power Amp Case Temp	+125°C
Output Amplifier Power Dissipation	20W max in free air, derate 0.2W/°C above +25°C
Output Current	See Figure 5 and Note 1

MECHANICAL



Material: Extruded, black-anodized, aluminum heat sink and discrete components mounted on glass epoxy printed circuit board.

4804 Connector: Amp 2 - 86479 - 3

Recommended mating Connectors: PC card: 0806MC
Flexable: Scotchflex 3417 - 0000

Diameter of mounting holes: 3.56mm (0.14")

PIN CONNECTIONS

BOTTOM	PIN	TOP
-35V	1	-35V
Output	2	Output
+35V	3	+35V
N.C.	4	N.C.
-15V	5	-15V
Ana. Com.	6	Ana. Com.
+15V	7	+15V
Ana. Com.	8	Ana. Com.
N.C.	9	+30V Range
Offset Adj.	10	V_{out} Range Adj.
Strobe	11	Gain Adj.
+5V	12	+5V
Dig. Com.	13	Dig. Com.
Bit 2	14	Bit 1
Bit 4	15	Bit 3
Bit 6	16	Bit 5
Bit 8	17	Bit 7
Bit 10	18	Bit 9
Bit 12	19	Bit 11

TYPICAL PERFORMANCE CURVES

(Typical @ 25°C and ±15VDC Power Supplies unless otherwise noted)

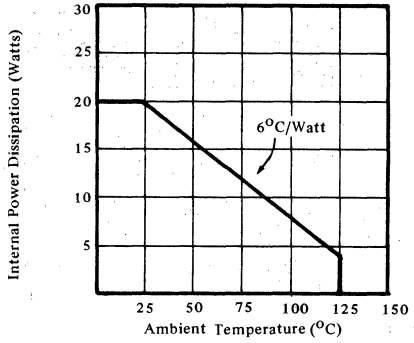


FIGURE 2. Power Derating Curve.

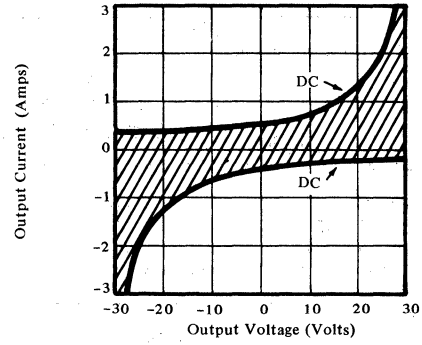


FIGURE 3. Safe Operating Area.

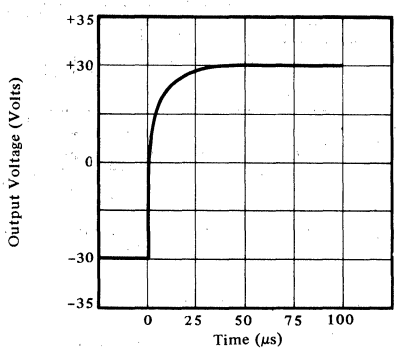


FIGURE 4. Pulse Response.

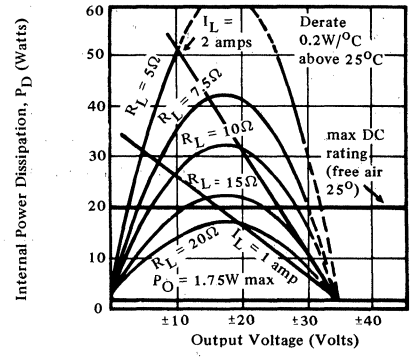


FIGURE 5. Output Amplifier Power Dissipation vs. Output Voltage.

DIGITAL INPUT CODES VS. V_{OUT}		
INPUT CODE MSB LSB	**NOMINAL OUTPUT VOLTAGE**	
	±30V RANGE	**VARIABLE RANGE**
1111 11111 111	+30.000V	$+10.000\left(\frac{R_G}{10k}\right)$ V
1111 1111 1110	+29.985V	$+9.995\left(\frac{R_G}{10k}\right)$ V
1000 00000 000	+14.65mV	$+4.88\left(\frac{R_G}{10k}\right)$ mV
0 11111111 111	0.000V	0.000V
0 111111111 10	-14.65mV	$-4.88\left(\frac{R_G}{10k}\right)$ mV
0000000000001	-29.971V	$-9.990\left(\frac{R_G}{10k}\right)$ V
000000000000	-29.985V	$-9.995\left(\frac{R_G}{10k}\right)$ V

TABLE I.

PROCEDURES FOR ADJUSTING OFFSET AND GAIN ERRORS...

OFFSET AND GAIN ADJUSTMENT

The offset and gain of the D/A converter stage may be trimmed using externally connected OFFSET ADJUST and GAIN ADJUST potentiometers. The adjustment procedure is outlined below. Since the GAIN ADJUST is connected to a high impedance point in the D/A converter, a ceramic capacitor connected between this point and analog common is recommended to minimize noise pickup. The offset error should always be nulled before adjusting the gain error potentiometer.

OFFSET ADJUST PROCEDURE

Apply the digital code which could give the maximum positive voltage output and adjust the OFFSET ADJUST potentiometer for the proper output voltage. For example, if the 4804 is connected for a full scale range of ±30V, apply all ones to the input and adjust the potentiometer for an output of +30.000V.

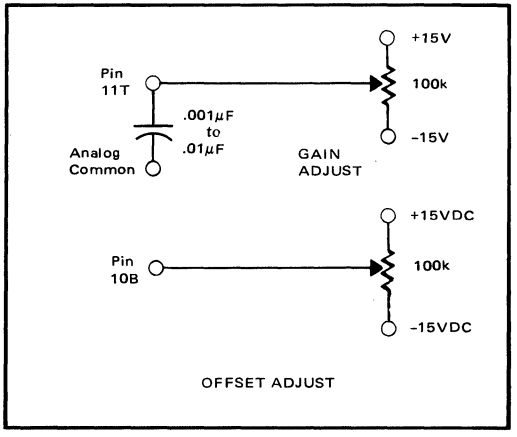


FIGURE 6.

GAIN ADJUST PROCEDURE

Apply the digital code which should give the maximum negative voltage output, and adjust the GAIN ADJUST potentiometer for the proper output voltage. For example, if the 4804 is connected for a full scale range of ±30V, apply all zeros and adjust the potentiometer for an output of -29.985V.

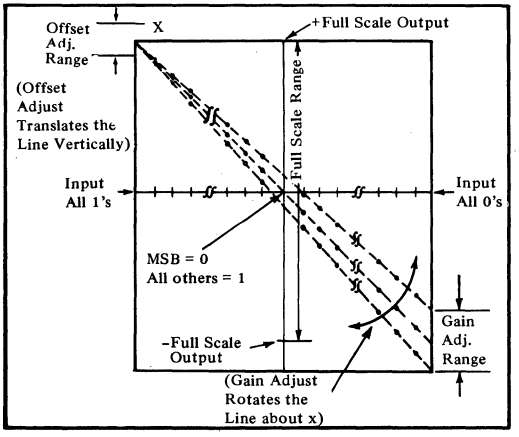


FIGURE 7.

4804

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The 4804 accepts TTL and CMOS compatible input codes in binary format. Table I shows the output voltage for selected inputs.

ACCURACY

Total Accuracy is the maximum deviation from the ideal output over the full output range. It is tested at 25°C and represents the maximum allowed value of the sum of the individual errors. The total accuracy is specified as a maximum with the 4804 in the ±30V range configuration. If an output range less than ±30V is selected, the accuracy will improve as the power amplifier gain is reduced.

Lineary Error for the 4804 is specified as a maximum over the temperature range of 0°C to +70°C. This means that the analog output will not vary by more than ±½ LSB maximum from an ideal straight line drawn between the "all bits ON" and "all bits OFF" end points.

Differential Linearity is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error spec of ±½ LSB means that the output voltage step sizes can be anywhere from ½ LSB to 3/2 LSB when the input changes from one adjacent input state to the next.

Monotonicity over 0°C to +70°C is guaranteed in the 4804. This insures that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is measure of the change in the full scale range analog output over temperature. The GAIN DRIFT is determined by testing the end point differences at 0°C, +25°C and +70°C, calculating the GAIN ERROR with respect to the 25°C value, and dividing by the temperature change. This specification is expressed in ppm/°C.

Offset Drift is a measure of the actual change in the output with all bits OFF (all 0's) over the specified temperature range, and is measured at 0°C, +25°C and +70°C.

The maximum change in OFFSET is referenced to the OFFSET at 25°C divided by the temperature range. This drift is expressed in parts per million of full scale ranges per °C (ppm of FSR/°C).

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the effect of a power supply voltage variation on the 4804 output. It is defined as a change in output voltage per change in supply voltage with the ±30V output range. Power supply rejection is improved if a full scale range less than ±30V is selected.

OPERATING INSTRUCTIONS

REMOTE SENSING

In applications requiring that the load be located some distance from the Power DAC, the line resistance from the 4804 to the load can cause significant error, especially during operation at high currents. To minimize this problem, connect the circuit with the line resistance inside the feedback loop of the output amplifier, as shown in Figure 8. This technique effectively divides the line resistance by the open loop gain of the output amplifier (94 dB min, with R_{LOAD} 5Ω). To minimize noise pickup, the external feedback resistor should be located as close as possible to the 4804.

Since the amplifier must still overcome the voltage drop in the line inside the feedback loop, the dynamic range of the load voltage will be reduced by approximately I_{LOAD} x R_{LINE}. Proper grounding of the 4804, load, and digital stimulus will also reduce errors caused by ground loops.

THERMAL CONSIDERATIONS

The absolute maximum internal power dissipation of the output amplifier is 20 watts in free air at 25°C. Derate by 0.2W/°C above 25°C. Thermal resistance from amplifier junction to ambient is 6°C/watt. Figure 5 shows internal power dissipation as a function of otuput voltage and load resistance with ±35V supply voltages.

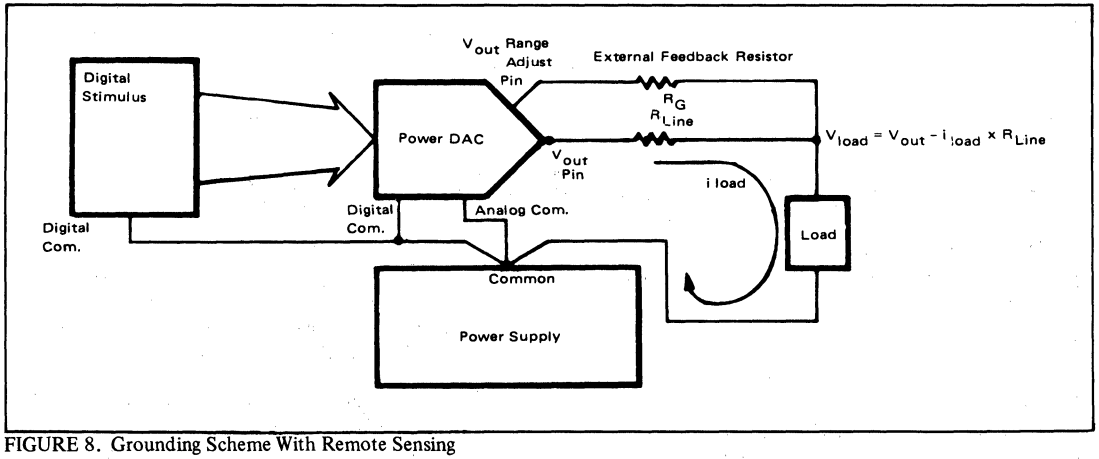
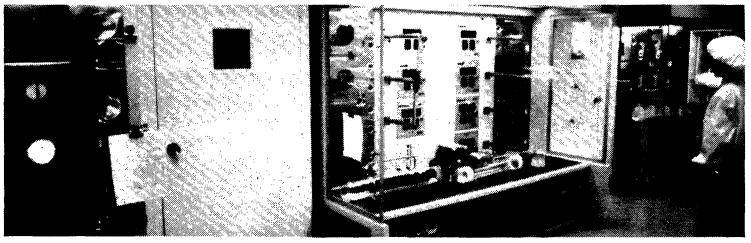
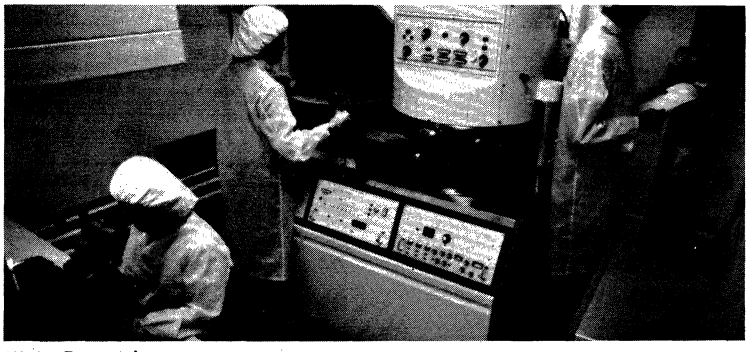


FIGURE 8. Grounding Scheme With Remote Sensing

MILITARY PRODUCTS GROUP



Wafer Processing



Wafer Processing

High quality products for demanding military and industrial applications are produced by our Military Products Group in a totally separate facility within Burr-Brown's complex.

Reliability is designed and manufactured-into our Military Products under the guidance of MIL-M-38510.

All product families are fully specified from -55°C to +125°C with up to three performance grades and two product assurance levels (/883B and /MIL).

The /883B models are 100% screened to MIL-STD-883, level B, method 5004 or 5008. The /MIL models have additional requirements of 10% PDA and QCI consisting of groups A and B on each inspection lot.

How stringently our Military Products group controls and documents the assembly and testing of its products is described in the product flow section that follows.

All materials used by the Military Products group have unique component specifications to assure their conformity to MIL-STD-883, methods 2010 and 2017.

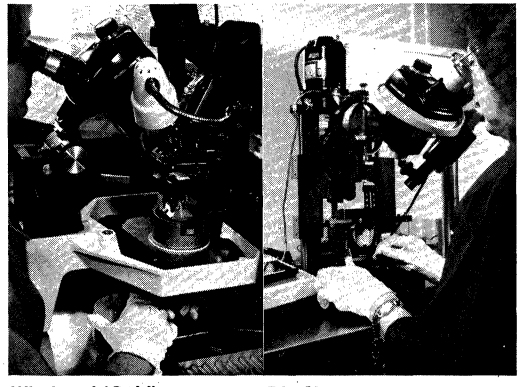
Environmental control in our clean room areas meets and often exceeds Federal Standard 209B requirements for particle count. ESD (electrostatic discharge) procedures are fully observed through every stage of material handling, product assembly, testing, storage and shipment. Operator training, certification and re-certification conform to MIL-M-38510.

MTTF data is based on actual product performance, not just calculated values. Qualification reports and test data are available. All data sheets follow military slash sheet format and, because of their completeness, can be transferred directly to your drawings with minimal modification. This standard QPL slash sheet format simplifies your requests to government agencies for non-standard parts approval.

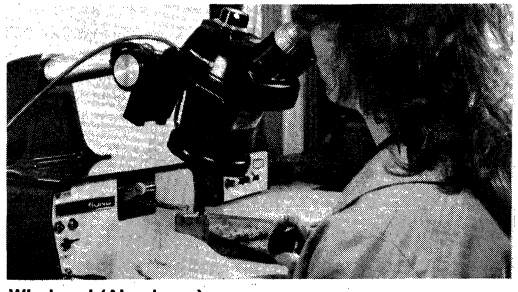
A CONTROLLED MANUFACTURING FACILITY DEDICATED EXCLUSIVELY TO MILITARY QUALITY PRODUCTION

- PERSONNEL - All production and quality control personnel directly involved with fabrication, inspection, testing and handling perform their functions according to appropriate MIL specs.
- TRAINING - Operator training and certification programs provide trained personnel qualified to assemble and test the products. Certification requires classroom training and written examinations for initial certification. Periodic written exams must be passed to maintain certification.
- WORK-IN-PROCESS ENVIRONMENT - All work-in-process is stored in a nitrogen environment. Critical assembly processes; die visual, die attach, wirebond and all inspections are performed under laminar flow hoods - equipped with ion grids - in a class 100 environment.
- ENVIRONMENTAL CONTROL - Clean room procedures, which conform to Federal Standard 209B, provide class 10,000 clean air exceeding the class of 100,000 requirement of MIL-STD-883.
- MATERIAL CONTROL - Each product has a complete and current flow chart and flow sheet to assure accurate processing through assembly and test. Each manufacturing lot contains the lot numbers of its components listed by the quality control inspection identification (QCID number) all traceable back to the incoming vendor's lot number.
- MANUFACTURING LOT CONTROL - Each lot has a unique flow sheet which documents lot number, parts list, operation, quantity, date of operation and operator's identification.
- EQUIPMENT CALIBRATION - Performed under the guidance of MIL-STD-45662.
- QUALIFICATION - All /MIL models are initially qualified per MIL-STD-883, method 5004 or 5008, groups A, B, C and D as described in the products' detailed specification.
- STATIC CONTROL - To minimize static (ESD) damage, antistatic smocks, stainless steel table tops, stainless steel work-in-process trays, ground straps, ion grids under laminar flow hoods and anti-static shipping materials are used.
- RECORD RETENTION - All flow sheets containing process data and inspection records are retained for three years.

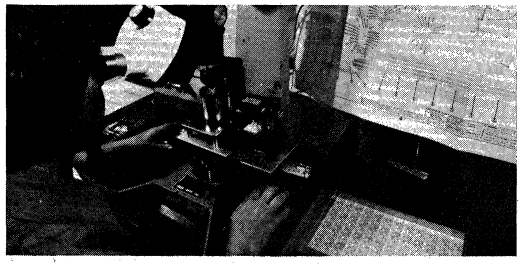
Assembly Under Laminar Hood



Wirebond (Gold) **Die Shear**

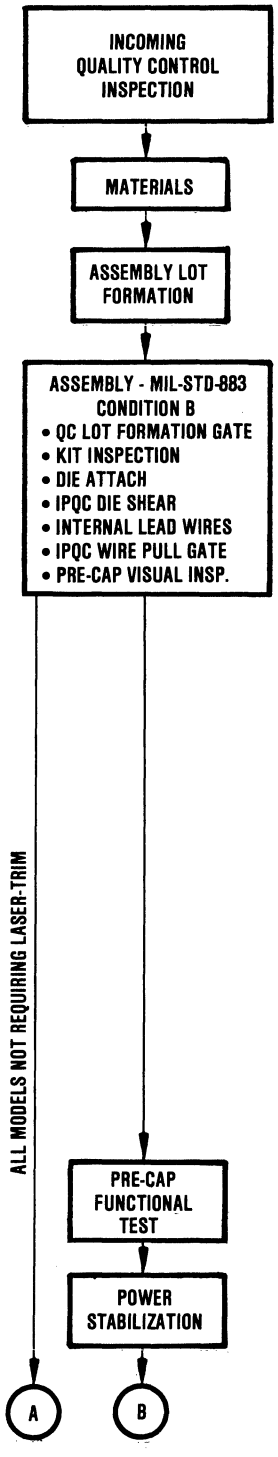


Wirebond (Aluminum)



Die Attach

PRODUCT FLOW



Assures that all materials meet requirements of the applicable component specification. Usage tests are performed and vendor lot traceability begins.

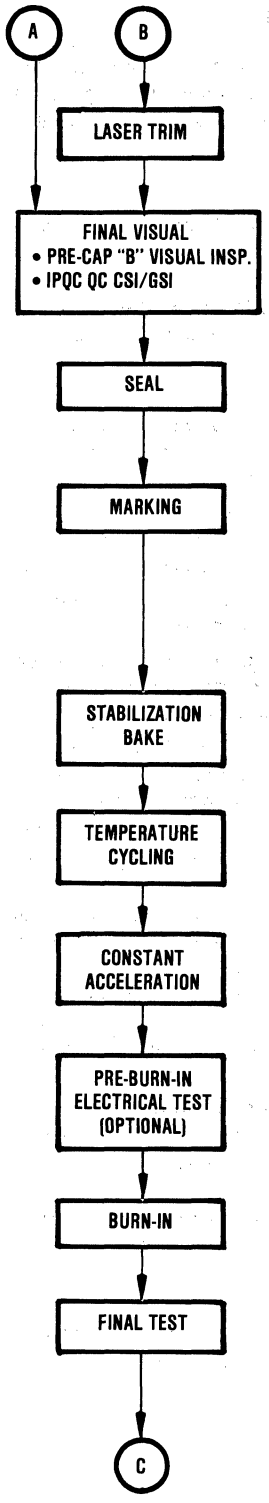
All material is maintained in a bonded stockroom to assure traceability.

Orgination of manufacturing flow sheets, bill of material, materials and lot traceability records.

- QC Lot Formation Gate - matches flow sheet, bill of materials and traceability records with materials issued from the stockroom
- Kit Inspection - piece parts and die are 100% visually inspected to methods 2010 and 2017.
- Die Attach - eutectic (providing low ohmic contact) and non-conductive epoxy (cured at 25°C above storage temperature in nitrogen).
- In Process Die Shear Gate - performed to method 2019 on each manufacturing lot. Assures the integrity of the die attach method.
- Internal Lead Wires - Wires are of the same metal as the die metalization. Aluminum ultrasonic wirebond machines are mounted on shock tables to insure quality bonds. Gold-to-gold wirebonds are performed with thermosonic wirebond machines.
- In Process Wire Pull Gates - bonding operations are monitored at the beginning of each shift, every four hours, with a new lot, new operator or a machine adjustment. Both destruct and non-destruct tests are performed and the length and width of each wirebond is measured to verify conformance to method 2010 or 2017.
- Pre-Cap Visual Inspection - Although not required by MIL-STD-883 it is performed by Burr-Brown to method 2010 or 2017.

Performed on all products that require laser trimming.

All products that require laser-trimming receive a 72-hour burn-in, in nitrogen, at +125°C.



Resistor networks are laser-trimmed to meet applicable specifications.

- Pre-Cap "B" Visual Inspection - a 100% visual inspection to method 2010 or 2017.
- In Process QC Pre-Cap "B" Visual Gate - performed to method 2010 or 2017. (Source Inspection performed if required.)

Following a vacuum bake at +125°C (to meet method 5004 or 5008 moisture content requirements) products are welded, gold/tin or glass sealed.

Marking is in accordance with MIL-M-38510 and consists of;

- Part number
- Seal date code
- Manufacturer's identification (BURR-BROWN®)
- Manufacturer's designating symbol (CEBS)
- Country of origin

A 24-hour minimum bake at +150°C per MIL-STD-883, method 1008, condition C.

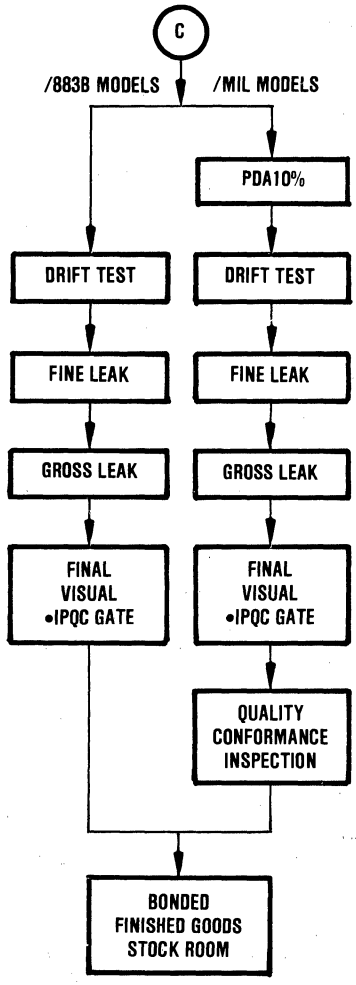
Ten cycles, from -65°C to +150°C per MIL-STD-883, method 1010, condition C.

Performed to MIL-STD-883, method 2001, in the Y_1 axis only.

Product performance is compared to the specified DC parameters at 25°C.

Total burn-in time is 160 hours minimum at an ambient temperature of +125°C per MIL-STD-883, method 1015.

Product performance is compared to the specified DC parameters at 25°C. All 25°C parameters specified in the data sheets are read and recorded.



The assembly lot PDA (percent defective allowable) cannot exceed 10%.

All drift parameters as specified in the data sheet are 100% tested at -55°C, -25°C, +25°C, +85°C and +125°C.

100% test to MIL-STD-883, method 1014, test condition A.

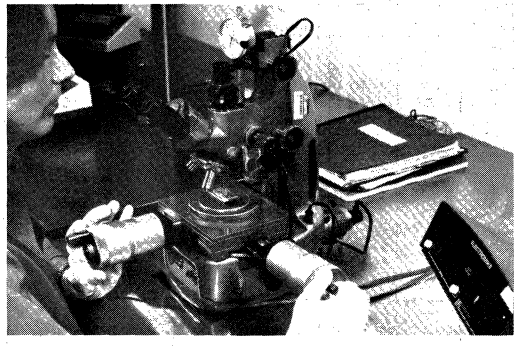
100% test to MIL-STD-883, method 1014, condition C.

100% external visual inspection to MIL-STD-883, method 2009.

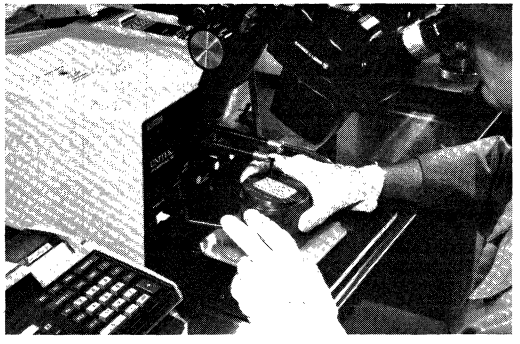
- Final Visual Quality Control Gate - to MIL-STD-883, method 2009.

Groups A and B inspection of MIL-STD-883, method 5005 or 5008 are performed on each inspection lot. Groups C and D inspections are performed when agreed to by contract. A report of the most recent Groups C and D inspections is available from Burr-Brown at a nominal charge.

This product flow illustrates major operations only. Space does not allow a complete description of the numerous details of all operations. Processes and flows may change to conform to latest revisions or to improved product performance and quality.



Bond Measurement



Wire Pull

SELECTION GUIDE
Military Products

ANALOG-TO-DIGITAL CONVERTERS

Model	Resolution Bits	Linearity ±LSB, max	Conversion Time µsec, max	Gain Drift ±ppm/°C, max	Input Range V	Temperature Range	Package	Price(4) ($) Unit	Page
ADC87/MIL(1)	12	1/2	8	15	±2.5,	MIL	32-pin DIP	415.00	7-7
ADC87/883B	12	1/2	8	15	±5,	MIL		325.00	7-7
ADC87	12	1/2	8	15	±10,	MIL		290.00	7-7
ADC87U/883B	12	1/2	8	15	0 to +5,	MIL		270.00	7-7
ADC87U	12	1/2	8	15	0 to +10	MIL		230.00	7-7

DIGITAL-TO-ANALOG CONVERTERS

Model	Resolution Bits	Linearity ±LSB, max	Monotonicity	Gain Drift ±ppm/°C, max	Settling Time max	Output Ranges	Temperature Range	Package	Price(4) ($) Unit	Page
DAC87-CBI-V/MIL	12	1/2	-55°C/+125°C	20	7	±2.5,	MIL	24-pin DIP	275.00	7-23
DAC87-CBI-V/B	12	1/2	-55°C/+125°C	20	7	±5,	MIL		225.00	7-23
DAC87-CBI-V	12	1/2	-55°C/+125°C	20	7	±10,	MIL		180.00	7-23
DAC87U-CBI-V/B	12	1/2	-25°C/+85°C	20	7	+5,	MIL		165.00	7-23
DAC87U-CBI-V	12	1/2	-25°C/+85°C	20	7	+10	MIL		125.00	7-23

MULTIPLIERS

Model	Accuracy at 25°C ±%, max	Accuracy at 125°C ±%, max	Feedthrough ±mV, max	Output Offset ±mV, max	Output V, mA, min	Temperature Range	Package	Price(4) ($) Unit	Page
4213WM/883B	1/2	4	50	25	±10, ±5	MIL	TO-100	125.00	7-92
4213WM	1/2	4	50	25		MIL	TO-100	110.00	7-92
4213VM/MIL	1	4	100	30		MIL	TO-100	95.00	7-92
4213VM/883B	1	4	100	30		MIL	TO-100	68.00	7-92
4213VM	1	4	100	30		MIL	TO-100	53.00	7-92
4213UM/883B	1	2*	100	50		MIL	TO-100	45.00	7-92
4213UM	1	2*	100	50		MIL	TO-100	35.00	7-92

*at +85°C.

VOLTAGE-TO-FREQUENCY CONVERTERS

Model	V_{IN} Range V	F_{OUT} Range kHz, max	Linearity % FSR, max	Full Scale Drift ppm FSR/°C, max	Temperature Range	Package	Price(4) ($) Unit	Page
VFC32WM/883B	±10	500	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100	50.00	7-61
VFC32WM	±10	500	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100	40.00	7-61
VFC32VM/MIL	±10	500	±0.01 at 10kHz	-400, +150 at 200kHz	MIL	TO-100	60.00	7-61
VFC32VM/883B	±10	500	±0.01 at 10kHz	-400, +150 at 200kHz	MIL	TO-100	45.00	7-61
VFC32VM	±10	500	±0.01 at 10kHz	-400, +150 at 200kHz	MIL	TO-100	35.00	7-61
VFC32UM/883B	±10	500	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100	30.00	7-61
VFC32UM	±10	500	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100	20.00	7-61

OPERATIONAL AMPLIFIERS

Description	Model	Offset Voltage at 25°C ±mV, max	Offset Voltage drift ±µV/°C max	Bias Current nA, max	Bandwidth Unity Gain MHz, min	Slew Rate V/µs,min	ts ±0.01% ns	Compensation	Output V, mA, min	Temp. Range	Package	Price(4) ($) Unit	Page
Wideband	OPA600VM/MIL(2)	2	20	-100pA	5000,†, A = 1000	400	125	external	±10, ±200	MIL	16-pin DIP	315.00	7-45
	OPA600VM/883B	2	20	-100pA		400	125			MIL		250.00	7-45
	OPA600VM	2	20	-100pA		400	125			MIL		225.00	7-45
	OPA600UM/883B	5	80	-100pA		400	150			MIL		195.00	7-45
	OPA600UM	5	80	-100pA		400	150			MIL		175.00	7-45
FET Low Drift	OPA105WM/MIL(3)	0.25	2	-1pA	1	0.9	--	Internal	±10, ±5	MIL	TO-99	75.00	7-35
	OPA105WM/883B		2		1	0.9	--			MIL		57.00	7-35
	OPA105WM/ OPA105VM/MIL(3)		2		1	0.9	--			MIL		47.00	7-35
			5		1	0.9	--			MIL		55.00	7-35
	OPA105VM/883B		5		1	0.9	--			MIL		43.00	7-35
	OPA105VM		5		1	0.9	--			MIL		35.00	7-35
	OPA105UM/883B		15		1	0.9	--			MIL		30.00	7-35
	OPA105UM		15		1	0.9	--			MIL		25.00	7-35
General Purpose Bipolar	3500R/MIL	5	20	±30	1	0.6	--	internal	±10, ±10	MIL	TO-99	45.00	7-73
	3500R/883B	5	20	±30	1	0.6	--			MIL		30.00	7-73
	3500U/883B	5	20*	±30	1	0.6	--			MIL		25.00	7-73
Precision Bipolar	3510VM/MIL	0.12	2	±25	0.25	0.5	--	internal	±10, ±10	MIL	TO-99	45.00	7-84
	3510VM/883B	0.12	2	±25	0.25	0.5	--	internal	±10, ±10	MIL	TO-99	30.00	7-84

†Gain-bandwidth product. -25°C/+85°C.

NOTES: 1) ADC87/MIL available in the 2nd quarter of 1982. 2) OPA600VM/MIL available in the 2nd quarter of 1982. 3) OPA105/MIL available in the 3rd quarter of 1982. 4) Qty. disc. available.

BURR-BROWN®

ADC87/MIL SERIES

MODEL NUMBERS:

ADC87/MIL ADC87U/883B
ADC87/883B ADC87U
ADC87

REVISION NONE
JANUARY, 1982

12-BIT -55°C to +125°C Military ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **HI-REL MANUFACTURE**
- **ACCURATE**
  - **±1/2LSB max Linearity Error**
  - **±0.1% FSR max Full Scale Absolute Accuracy**
  - **±15ppm max Gain Drift**
- **8μsec MAX CONVERSION TIME**
- **-55°C TO +125°C OPERATION**
- **COMPLETE**
  - **Internal Reference**
  - **Internal Buffer**
  - **Internal Clock**
- **MIL-STD-883 SCREENING**

DESCRIPTION

The ADC87/MIL Series is a high performance, analog-to-digital converter. It features ±1/2LSB linearity, ±0.1% full scale accuracy, ±15ppm drift, 8μsec conversion time, -55°C to +125°C operation and optional MIL-STD-883 screening.

The ADC87 uses successive approximation. It resolves the most significant bit first, then the second bit, then the third, etc. Successive approximation is the most popular high performance design as it is fast and accurate.

The ADC87 is a hybrid microcircuit. It is complete with an internal reference, an input buffer amplifier and an internal clock. The converter may be short cycled to provide faster conversions to less resolution. Five analog input ranges, ±2.5V, ±5V, ±10V, 0 to +10V and 0 to +20V, are available, and the digital output data is available in parallel and serial format. All digital outputs and inputs are TTL compatible. Standard power supply voltages, ±15VDC and +5VDC, are required.

Two electrical performance grades are available. The premium grade operates from -55°C to +125°C and is designed for military, aerospace, and demanding industrial applications. The U grade has specifications from -25°C to +85°C and from -55°C to +125°C. Applications include test equipment, shipboard, and ground support equipment where operation is normally between -25°C and +85°C and full temperature range operation must be assured.

The ADC87/MIL Series is manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions which assures inherent quality and provides for long product life. The ADC87 is hermetically sealed in a metal, welded, dual-in-line package.

Three product assurance levels are available: Standard, /883B and /MIL. The Standard product assurance level offers Hi-Rel manufacturing where many MIL-STD-883 screens are performed routinely. The /883B product assurance level, /883B suffix, offers Hi-Rel manufacturing plus 100% screening per MIL-STD-883 method 5008 (class B). The /MIL product assurance level, /MIL suffix, offers Hi-Rel manufacturing, 100% screening per MIL-STD-883B method 5008 and 10% PDA. Quality assurance further processes /MIL devices, by performing group A and B inspections on each inspection lot and group C and D inspections periodically and when specified on the customer's purchase order. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
ANALOG-TO-DIGITAL CONVERTER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detailed requirements for a precision 12-bit, integrated circuit, analog-to-digital converter.

1.2 Part number. The complete part number is as shown below.

ADC87		/MIL
Basic model number	Grade (see 1.2.1)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, analog-to-digital converter.
There are two electrical performance grades. The premium grade has no grade designation in the part number and features specifications and tests from -55°C to +125°C. The U grade has a U grade designation in the part number and features specifications and tests from -25°C to +85°C, and specifications from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinquishes the product assurance levels as follows:

Hi-Rel Product Designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
/883B	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is as defined in Figure 1. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±18VDC
Supply voltage, V_{DD}	+7VDC
Analog inputs (pins 24 and 25)	±25VDC
Buffer input	±18VDC
Digital inputs	+5.5VDC
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60sec)	+300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: +4.75VDC to +5.25VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A	Maximum θ J-A
32-lead can	Figure 1	1500mW at T_A = 125°C	7°C/W	25°C/W	32°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510, except that organic and polymeric materials may be used for substrate and die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-STD-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. All dice utilized are glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

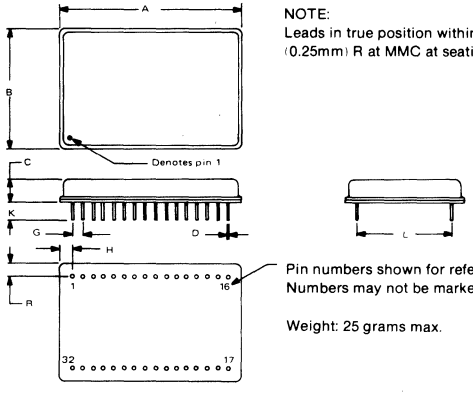
3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connection. The circuit diagram and terminal connections are shown in Figure 2.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Input Range. The analog input range is as specified in Table V when externally connected as shown therein.

3.3.2 Output Code. Coding is complementary binary. The digital output codes corresponding to analog input voltages are shown in Table VI.



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only.
Numbers may not be marked on package.

Weight: 25 grams max.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

FIGURE 1. Case Outline (Triple-Wide DIP Configuration).

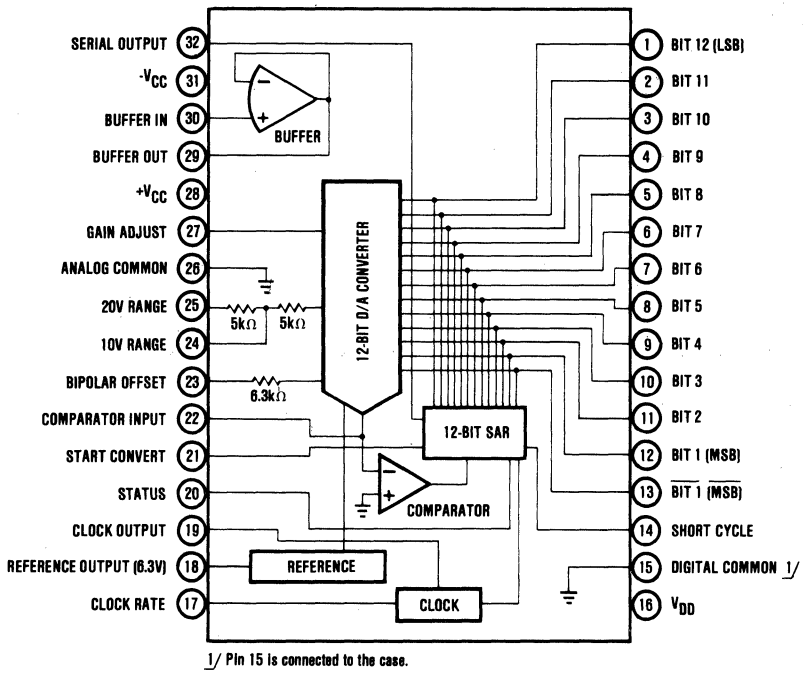


FIGURE 2. Circuit Diagram and Terminal Connections (Bottom View).

3.3.3 Transfer Function. An A/D converter represents an analog input voltage in a digital output format. The converter resolves the analog input into 12 bits of resolution, or 2^{12}, or 4096 voltage segments. For each voltage segment there is a unique digital output code.

The ideal transfer curve, as shown in Figure 3, is a "stair-case" connecting the extremes of the analog input range. Minus full scale (-FS) corresponds to digital 1111 1111 1111, the first transition occurs at -FS +1/2LSB, each bit is 1LSB wide, and +FS -1LSB corresponds to digital 0000 0000 0000. An ideal straight line connects each end point and the center of each bit. Note, the coding is complementary.

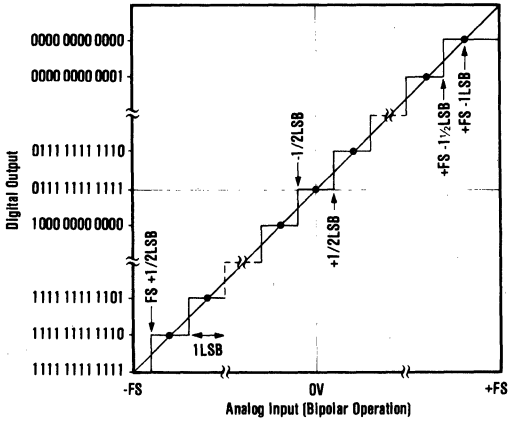
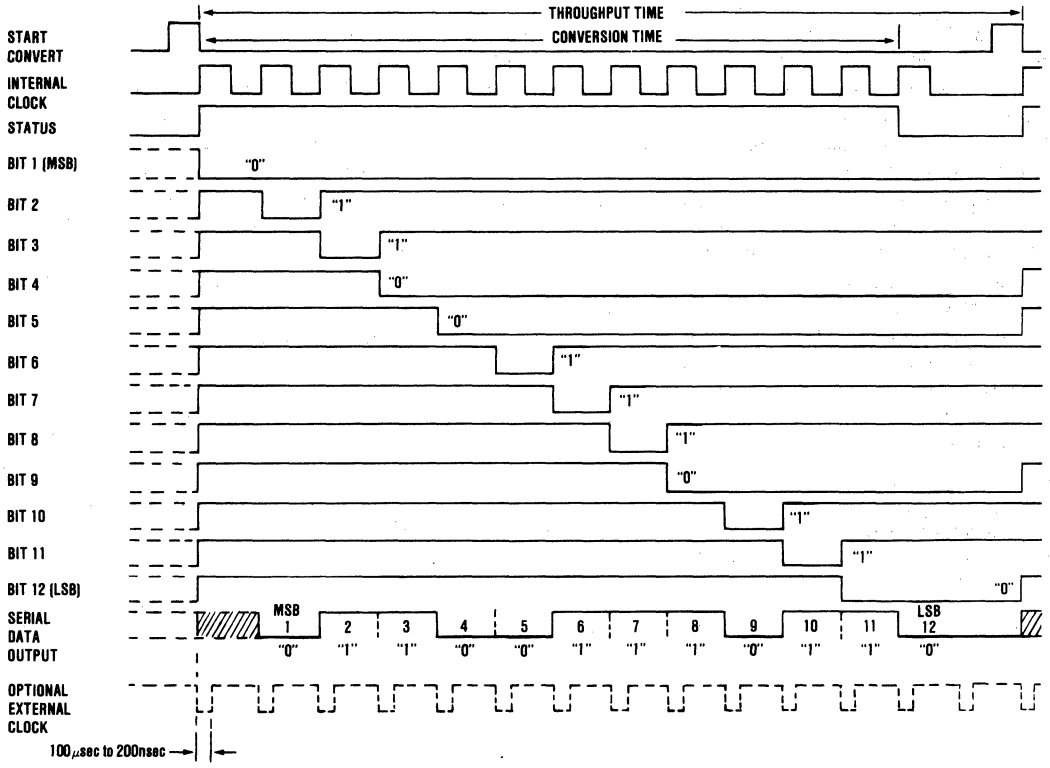


FIGURE 3. Ideal A/D Converter Transfer Function.

The 'basic' converter is unipolar in design; that is, 0VDC analog input produces one digital extreme and plus full scale VDC produces the other digital extreme. There are two unipolar input ranges. For bipolar operation, a bias (bipolar offset) is introduced into the input such that 0VDC analog input produces midscale digital output. This allows plus and minus analog inputs (see Figure 3). There are three bipolar input ranges.

The errors from the ideal transfer function are specified in Table I. Linearity and Differential Linearity are the most meaningful ADC87 accuracy indicators, as they are not externally adjustable. They are factory laser-trimmed. Zero error and gain error are laser-trimmed and may be externally nulled if necessary for the application. The inherent quantization uncertainty due to resolving or quantizing the analog input into bits is ±1/2LSB.

3.3.4 Timing Considerations. The timing diagram is shown in Figure 4. A start convert, positive going pulse, initiates a conversion. The most significant bit (MSB) is determined during the second clock pulse, and each successive bit is determined during the next 11 clock pulses. When conversion is complete, Status output drops to Logic 0. Digital output data is available in parallel or serial format. Serial output data may be strobed out bit-by-bit, during the clock period after the bit is determined. If desired, an external clock may be used. Further information is available in Applications Information, paragraph 7.



1. Start Convert must be at least 50nsec wide and must remain low during conversion. Conversion is initiated by the Start Convert trailing edge. Once a conversion has begun, a second start pulse will not reset the converter.
2. Parallel data will be valid 140nsec after status goes low and remains valid until another conversion is initiated.
3. Serial data will be valid 140nsec after an internal clock rising edge and 200nsec after an external clock falling edge.
4. When using an external clock, conversion is initiated by the falling edge of the first clock pulse following status going low. The converter will continuously convert.

FIGURE 4. Timing Diagram.

3.3.5 Zero error and gain error adjustment. Zero error and gain error may be externally nulled using the circuits shown in Figure 6. See Applications Information, paragraph 7.4.

3.3.6 Required external connections. For specified accuracy and speed, connect Clock Rate, pin 17, to 0VDC, pin 15.

For a 12-bit conversion cycle, connect Short Cycle, pin 14, to Logic 1, pin 16. See Applications Information, paragraph 7, for additional information.

3.4 Electrical test requirements. Electrical test requirements are as specified in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin (U.S.A.)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /MIL Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability, for /MIL, is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

Screening for the standard model, includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition A), and external visual inspection per MIL-STD-883, method 5008, hybrid class.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /MIL Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

1/ A 4-digit date code, indicating year and week of seal, is marked on 883B and (none) Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics.

(T_A = -55°C to +125°C, Supply Voltages ±15VDC and +5VDC, unless otherwise specified.)

CHARACTERISTICS	CONDITIONS	LIMITS						UNITS
		ADC87/MIL* ADC87/883B ADC87			ADC87U/883B ADC87U			
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION		12			•			Bits
ANALOG INPUTS								
Input Voltage Ranges: Unipolar			0 to +5, 0 to +10			•		V
Bipolar			±2.5, ±5, ±10			•		V
Direct Input Impedance: 0 to +5V, ±2.5V			2.5			•		kΩ
0 to +10V, ±5V			5			•		kΩ
±10V			10			•		kΩ
Buffer Amplifier: Gain Accuracy			±0.01			•		%
Input Impedance	T_A = +25°C		50		•	•		MΩ
Input Bias Current	T_A = +25°C		100			•		nA
Offset Voltage	T_A = +25°C		2	5		•		mV
Settling Time	20V step to ±0.01% FSR		2			•		µsec
DIGITAL INPUTS								
Start Convert Command: 1/								
Positive Pulse Width		50			•			nsec
Logic Loading				1			•	TTL Load 2/
Short Cycle Logic Loading				1			•	TTL Load
Logic Levels: Logic "1"		2			•			V
Logic "0"				0.8			•	V
(All Digital Inputs)								
DIGITAL OUTPUTS								
Parallel Data Coding: 3/								
Unipolar Ranges			CSB			•		
Bipolar Ranges			COB, CTC			•		
Output Drive		2			•			TTL Loads
Serial Data Coding (NRZ) 3/			CSB, COB			•		
Output Drive		2			•			TTL Loads
Status Bit Coding			Logic 1 During Conversion					
Output Drive		2			•			TTL Loads
Internal Clock Output Drive		2			•			TTL Loads
Logic Levels: Logic "1"		2.4			•			V
Logic "0"				0.4			•	V
(All Outputs)								
TRANSFER CHARACTERISTICS**								
Zero Error, Bipolar 4/	+25°C		±0.02	±0.05		±0.02	±0.07	% FSR 5/
(Bipolar Major Transition Error)	-25°C to +85°C					±0.05	±0.15	% FSR
	-55°C to +125°C		±0.05	±0.1			±0.3	% FSR
Full Scale Absolute Accuracy Error, 4/	+25°C		±0.05	±0.1		±0.05	±0.15	% FSR
Bipolar 6/	-25°C to +85°C					±0.1	±0.25	% FSR
	-55°C to +125°C		±0.1	±0.2			±0.6	% FSR
Gain Error 4/	+25°C		±0.05	±0.1		±0.05	±0.1	%
	Drift 7/		±10	±15		±10	±15	ppm/°C
Zero Error, Unipolar 4/	+25°C	+0.05	+0.10	+0.15	+0.05	+0.10	+0.2	% FSR
	-25°C to +85°C					±0.15	±0.3	% FSR
	-55°C to +125°C		±0.15	±0.2			±0.6	% FSR
Full Scale Absolute Accuracy Error, 4/	+25°C		±0.1	±0.2		±0.1	±0.25	% FSR
Unipolar	-25°C to +85°C					±0.2	±0.4	% FSR
	-55°C to +125°C		±0.2	±0.3			±0.9	% FSR
Linearity Error	+25°C		±1/4	±1/2		•	•	LSB 8/
	-25°C to +85°C					±1/2	±1	LSB
	-55°C to +125°C		±1/2	±1			±4	LSB
	Drift			±2			•	ppm of FSR/°C
Inherent Quantization Uncertainty			±1/2			•		LSB
Differential Linearity Error	+25°C		±1/4	±1/2		•	•	LSB
	-25°C to +85°C						±1	LSB
	-55°C to +125°C			±1			±3	LSB
	Drift		±2			•		ppm of FSR/°C
No Missing Codes		-55		+125	-25		+85	°C
Monotonicity		-55		+125	-25		+85	°C
Zero Adjustment Range		0.3	0.4		•	•		% FSR
Gain Adjustment Range		0.5	0.55		•	•		% FSR
DYNAMIC CHARACTERISTICS**								
Conversion Time 9/			7.5	8		•	•	µsec
Internal Clock Frequency 9/		1.5	1.6		•	•		MHz

*ADC87/MIL are available second quarter 1982.

TABLE I. Electrical Performance Characteristics (cont).

T_A = -55°C to +125°C, Supply Voltages ±15VDC and +5VDC, unless otherwise specified

CHARACTERISTICS	CONDITIONS	LIMITS						UNITS
		ADC87/MIL, ADC87/883B, ADC87			ADC87U/883B, ADC87U			
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE								
Internal Reference: Voltage		6.0	+6.3	6.6	*	*	*	V
Drift	-55°C to +125°C			±5			*	ppm/°C
External Current				200			*	µA
POWER SUPPLY								
Power Supply Range: ±15V Supply		±14.5	±15	±15.5	*	*	*	V
+5V Supply		+4.75	+5	+5.25	*	*	*	V
Quiescent Current: +15V			35	45		*	*	mA
-15V			35	45		*	*	mA
+5V			40	50		*	*	mA
Power Consumption	Quiescent		1300	1500		*	*	mW
Power Supply Rejection: +15VDC			±0.002			*		% FSR/%V_{CC}
-15VDC			±0.002			*		% FSR/%V_{CC}
+5VDC			±0.001			*		% FSR/%V_{CC}
THERMAL CHARACTERISTICS								
Operating Temperature Range	Ambient	-55		+125	-55		+125	°C
Storage Temperature Range	Ambient	-65		+150	-65		+150	°C
Thermal Impedance: Case to Ambient, θ_{CA}			20			*		°C/W
Junction to Case, θ_{JC}			5			*		°C

*Specifications the same as ADC87/MIL.
**Transfer and dynamic characteristics are specified without the optional buffer amplifiers.

NOTES:
1/ Trailing edge (logic 1 to logic 0) initiates conversion.
2/ A TTL Load is defined as 40µA max at V_{IN} = 2.4VDC (logic 1), and -1.6mA max at V_{IN} = 0.4VDC (logic 0).
3/ CSB = Complementary Straight Binary; COB = Complementary Offset Binary; CTC = Complementary Two's Complement. Serial and parallel output data is in Nonreturn to Zero (NRZ) format. See Output Coding and Timing Diagram.
4/ Externally adjustable to zero. This specification is without external adjustment.
5/ FSR = Full Scale Range. The ±10V analog input range is a 20V FSR. The ±5V or 0 to 10V input range is a 10V FSR.
6/ Applies to +Full Scale and to -Full Scale.
7/ Gain drift is defined as the absolute value of the change from +25°C to the hot temperature, plus the absolute value of the change from +25°C to the cold temperature, and that quantity divided by the temperature span. This is a 3-point drift. The hot temperature change is usually greater than the cold temperature change.
8/ ±1LSB = ±0.024% FSR.
9/ Conversion time is defined as the width of the status pulse. It is specified using the internal clock, with Clock Rate, pin 17, connected to 0VDC and Short Cycle, pin 14, connected to logic 1.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MODELS / MIL-STD-883 TEST REQUIREMENTS (HYBRID CLASS)	ADC87/MIL	ADC87/883B, ADC87	ADC87U/883B, ADC87U
	Subgroups (see Table III)		
Interim electrical parameters (preburn-in) (method 5008)	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 7	1, 2, 3, 4, 7	1, 2U, 3U, 4, 7
Group A test requirements (method 5008)	1, 2, 3, 4, 7	--	--
Group C end point electrical parameters (method 5008)	Table IV delta limits and limits	--	--
Additional electrical subgroups performed prior to Group C inspections	5, 6	--	--

*PDA applies to subgroup 1 (see 4.3.d)

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	CONDITIONS 1/	LIMITS ADC87/MIL ADC87/883B ADC87 MIN	LIMITS ADC87/MIL ADC87/883B ADC87 MAX	LIMITS ADC87U/883B ADC87U MIN	LIMITS ADC87U/883B ADC87U MAX	UNITS
1	Zero error, bipolar 2/	±10V range 3/		±10		±14	mV
T_A = +25°C	Full scale error, -FS bipolar 2/	±10V range 3/		±20		±30	mV
	Full scale error, +FS bipolar 2/	±10V range 3/		±20		±30	mV
	Gain error 2/	±10V range		±20		±20	mV
	Linearity error			±1/2		±1/2	LSB
	Differential linearity error 4/			±1/2		±1/2	LSB
	No missing codes		Pass		Pass		Pass/fail
	Internal reference voltage		+6.0	+6.6	+6.0	+6.6	V
	Zero error, unipolar 2/	0 to +10V range 3/	+5	+15	+5	+15	mV
	Full scale error, unipolar 2/	0 to +10V range 3/		±20		±20	mV
	Gain error, unipolar 2/	0 to +10V range		±10		±10	mV
2	Zero error, bipolar	±10V range 3/		±20			mV
T_A = +125°C	Full scale error, -FS bipolar 2/	±10V range 3/		±40			mV
	Full scale error, +FS bipolar 2/	±10V range 3/		±40			mV
	Gain drift	See subgroup 3					
	Linearity error			±1			LSB
	Differential Linearity error			±1			LSB
	No missing codes		Pass				Pass/fail
2U	Zero error, bipolar 2/	±10V range 3/				±30	mV
T_A = +85°C	Full scale error, -FS bipolar 2/	±10V range 3/				±50	mV
	Full scale error, +FS bipolar 2/	±10V range 3/				±50	mV
	Gain drift	See subgroup 3U					
	Linearity error					±1	LSB
	Differential linearity error					±1	LSB
	No missing codes				Pass		Pass/fail
3	Zero error, bipolar 2/	±10V range 3/		±20			mV
T_A = -55°C	Full scale error, -FS bipolar 2/	±10V range 3/		±40			mV
	Full scale error, +FS bipolar 2/	±10V range 3/		±40			mV
	Gain drift	5/		±54			mV
	Linearity error			±1			LSB
	Differential linearity error			±1			LSB
	No missing codes		Pass				Pass/fail
3U	Zero error, bipolar 2/	±10V range 3/				±30	mV
T_A = -25°C	Full scale error, -FS bipolar 2/	±10V range 3/				±50	mV
	Full scale error, +FS bipolar 2/	±10V range 3/				±50	mV
	Gain drift	6/				±33	mV
	Linearity error					±1	LSB
	Differential linearity error					±1	LSB
	No missing codes				Pass		Pass/fail
4							
T_A = +25°C	Conversion time			8		8	µsec
5							
T_A = +125°C	Conversion time			8		8	µsec
6							
T_A = -55°C	Conversion time			8		8	µsec
7	Quiescent current	No load, all bits logic 1					
T_A = +25°C	+V_{CC}			45		45	mA
	-V_{CC}			45		45	mA
	V_{DD}			50		50	mA
	Power consumption	Quiescent		1500		1500	mW
	Zero adjustment range	±10V range	±60		±60		mV
	Gain adjustment range	±10V range	±100		±100		mV
	MSB inverted output		Pass		Pass		Pass/fail
	Serial output		Pass		Pass		Pass/fail

NOTES:

1/ ±V_{CC} = 15VDC, V_{DD} = 5VDC, no load, without the optional buffer amplifier, unless otherwise specified. The internal clock is used. Clock Rate, pin 17, is connected to 0VDC. Short Cycle, pin 14, is connected to logic 1.

2/ Without external adjustment.

3/ For the ±10V range: bipolar +FS is ideally at +9.995117VDC; bipolar zero is ideally at 0.000VDC; bipolar -FS is ideally at -10.000VDC. For the 0 to +10V range: unipolar +FS is ideally at +9.997559VDC; unipolar zero is ideally at 0.000VDC. Refer to Figure 3 and Table VI.

4/ Monotonicity is assured by differential linearity ≤±1LSB.

5/ The absolute value of the gain change from +25°C to +125°C, is added to the absolute value of the gain change from +25°C to -55°C. This provides a 3-point drift.

6/ The absolute value of the gain change from +25°C to +85°C, is added to the absolute value of the gain change from +25°C to -55°C. This provides a 3-point drift.

TABLE IV. Group C, End Point Electrical Parameters.
(T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC)

TEST	LIMIT	DELTA
Zero error, bipolar	20mV	10mV
+Full scale error, bipolar	30mV	10mV
-Full scale error, bipolar	30mV	10mV
Gain error, bipolar	30mV	10mV
Linearity	1LSB	1/2LSB
Differential linearity	1LSB	1/2LSB

TABLE V. Analog Input Range Selection Connections.

	DIRECT INPUT						BUFFERED INPUT				
Input Range	Input Signal to Pin	Input Impedance	Required External Pin Connections				Input Signal to Pin	Input Impedance	Required External Pin Connections		
±2.5V	24	2.5kΩ	30 to 26	29 open	23 to 22	22 to 25	30	50MΩ	29 to 24	23 to 22	22 to 25
±5V	24	5kΩ	30 to 26	29 open	23 to 22		30	50MΩ	29 to 24	23 to 22	
±10V	25	10kΩ	30 to 26	29 open	23 to 22		30	50MΩ	29 to 25	23 to 22	
0 to +5V	24	2.5kΩ	30 to 26	29 open	23 to 26	22 to 25	30	50MΩ	29 to 24	23 to 26	22 to 25
0 to +10V	24	5kΩ	30 to 26	29 open	23 to 26		30	50MΩ	29 to 24	23 to 26	

TABLE VI. Ideal Analog Input Voltage vs Digital Output Code.

	DIGITAL OUTPUT CODE			
	MSB LSB	MSB LSB	MSB LSB	
Input Range	1111 1111 1111	0111 1111 1111	0000 0000 0000	1LSB
±2.5V	-2.500V	0V	+2.498779V	1.2207mV
±5V	-5.000V	0V	+4.997559V	2.4414mV
±10V	-10.000V	0V	+9.995117V	4.8828mV
0 to +5V	0V	+2.500V	+4.998779V	1.2207mV
0 to +10V	0V	+5.000V	+9.997559V	2.4414mV

NOTE:
Analog voltages are the center of the bit range. Transitions occur 1/2LSB before and 1/2LSB after the bit center.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specified by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1.The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition A, Y_1 axis only.
b. Interim and final electrical test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = 125°C$ minimum
   (4) Test duration is 160 hours minimum
d. Percent defective allowable (PDA). The PDA, for the /MIL Hi-Rel product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
e. External visual inspection need not include measurement of case and lead dimensions.

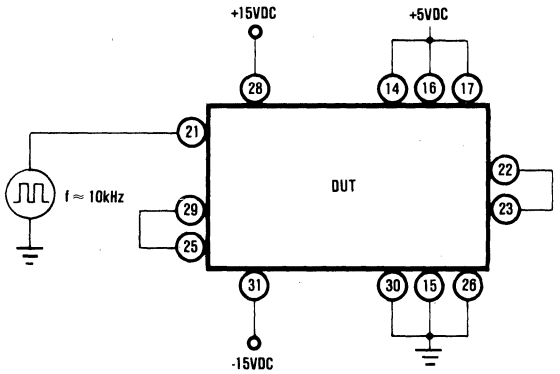


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Group D, subgroup 1, seal test, of MIL-STD-883, method 5008, is performed on each lot of packages procured. Groups C and D inspections (except for subgroup 1, seal test) of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodicaly performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table I, and as follows:
a. Tests are specified in Table II herein.
b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table II, and as follows:
a. Particle impact noise detection test is not required.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table III, and as follows:
a. Operating life test (MIL-STD-883, method 1005) conditions:
(1) Test condition B
(2) Test circuit is Figure 5 herein
(3) $T_A = 125°C$ minimum
(4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table IV, and as follows:
a. Particle impact noise detection test is not required.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:
a. Complete part number (see paragraph 1.2).
b. Requirements for certificate of compliance, if desired.

6.4 Definitions.

Full Scale Absolute Accuracy Error. Full scale absolute accuracy error is the difference between the ideal and the actual, unadjusted, analog input voltage at the full scale points. It applies to unipolar plus full scale, bipolar minus full scale, and bipolar plus full scale. Absolute accuracy includes zero, gain, linearity, and noise errors and, when specified over temperature, includes the drifts of these errors. It is measured at the first or last transition, as appropriate. The error is expressed in LSBs or % of FSR.

Bipolar Zero Error. Bipolar zero error is the difference between the ideal and the actual analog input voltage for the digital output code 0111 1111 1111. It is measured at the 1000 0000 0000 to 0111 1111 1111 transition which ideally occurs at 0VDC -1/2LSB.

Bipolar zero error is also known as bipolar major transition error.

Unipolar Zero Error. Unipolar zero error is the difference between the ideal and the actual analog input voltage for the digital output code 1111 1111 1111 (unipolar). It is measured at the 1111 1111 1111 to 1111 1111 1110 transition which ideally occurs at 0VDC +1/2LSB.

Gain Error. Gain error is the difference between the ideal and the actual analog input voltage span. It applies to both unipolar and bipolar input ranges. It is measured between the first transition and the last transition which is ideally FSR -2LSB.

Gain error in some literature describes what is defined herein to be unipolar full scale error and bipolar plus full scale error.

Offset Error. This term is not used with the ADC87. Offset error in some literature describes what is defined herein to be unipolar zero error and/or bipolar minus full scale error.

Linearity Error. Linearity error is the difference between the ideal and the actual bit transition when zero error and gain error equal zero.

Differential Linearity Error. Differential linearity error is the difference between the ideal and the actual bit step width. Zero differential linearity error means each bit step width is 1LSB. A maximum differential linearity error of ±1/2LSB means a bit step width may be between 1/2LSB and 3/2LSB.

Monotonicity. Monotonicity is the condition where the digital output code remains the same or increases for an increasing analog input signal.

Quantization Uncertainty. Quantization uncertainty is the inherent uncertainty of being able to determine the analog voltage which produces a digital code. Because the analog input voltage is divided or quantized into a finite number of bits, each digital code represents an analog voltage span equal to 1LSB. Quantization uncertainty is ±1/2LSB. Its magnitude may be reduced only by using a higher resolution converter.

6.5 Microcircuit group assignment. These microcircuits are Technology Group F as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. APPLICATIONS INFORMATION

7.1 Layout. To produce clean, noise-free, accurate conversions, high frequency layout techniques should be used. Wide, low inductance conductor patterns, short and direct external component leads, power supply decoupling, and a ground plane are recommended. Long runs should be avoided. Coupling and runs, which might cause input-to-output coupling, should be avoided. High impedance points should be given special consideration. The input to the buffer, the comparator input (particularly sensitive) and the external adjustment pins are sensitive. Shielding by Analog Common or ±15VDC supply patterns my be helpful.

7.2 Grounding. A ground plane under the ADC87 is recommended.

Analog Common (pin 26) and Digital Common (pin 15) must be connected together and to the analog system ground. Preferably, connect both commons directly to the ground plane under the ADC87. If these commons must be run separately, use wide conductor patterns and connect a 0.01μF ceramic capacitor between the commons at the unit. The case is connected to Digital Common, pin 15.

7.3 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum capacitor and a 0.01μF ceramic capacitor from each power supply to the ground plane. Locate the capacitors close to the converter.

7.4 Optional External Zero and Gain Adjustments. The ADC87 zero error and gain error are factory laser-trimmed to position the staircase transfer function within Table I specifications. Optionally, two adjustments null zero error and gain error (see Figure 6).

Zero adjustment moves the entire staircase left-to-right. For unipolar ranges, -FS, 0VDC, is nulled. For bipolar ranges, midscale, 0VDC, is nulled. (Alternately, bipolar -FS may be nulled.)

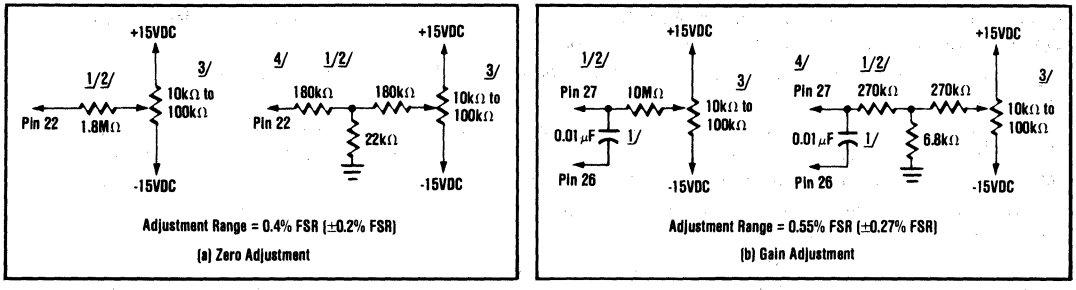
Gain adjustment adjusts the span of the staircase. Adjustment effectively rotates the staircase about -FS. For unipolar and bipolar ranges, zero adjustment should be made first, then +FS error is nulled.

Adjustments should be made after a 10 minute warm-up. Fixed, selected resistors may be substituted for the potentiometers after the adjustments have been determined, if desired. If adjustments are not used, pin 22 (zero adjust) should only be connected as required for analog input range selection and pin 27 (gain adjust) should be either grounded (recommended) or open.

7.4.1 Zero Adjustment Procedure. For the selected unipolar range, apply the analog input voltage at which the 1111 1111 1111 to 1111 1111 1110 transition ideally occurs, 0VDC +1/2LSB. While continuously converting, adjust the zero potentiometer until the transition "flickers".

For the selected bipolar range, apply the analog input voltage at which the 1000 0000 0000 to 0111 1111 1111 transition ideally occurs, 0VDC -1/2LSB. While continuously converting, adjust the zero potentiometer until the transition "flickers".

7.4.2 Gain Adjustment Procedure. Make zero adjustment first. For all input ranges, apply the analog input voltage at which the 0000 0000 0001 to 0000 0000 0000 transition ideally occurs, +FS -3/2LSB. While continuously converting, adjust the gain potentiometer until the transition "flickers". For bipolar ranges, repeat zero and gain adjustments as they are interactive.



Notes:
1/ Locate as close as possible to the converter to minimize noise pickup.
2/ 5% carbon composition or better.
3/ Use multiturn potentiometers with 100ppm/°C TCR or less to minimize drift with temperature.
4/ An attentuator network may be substituted for the series resistor for lower impedance and lower noise susceptibility.

FIGURE 6. Optional External Zero and Gain Adjustment Circuits.

7.5 Start Convert and Status. To start a conversion, a positive pulse with a minimum pulse width of 50nsec must be applied to the Start Convert terminal, pin 21. The trailing edge (falling edge) resets the converter, starts the internal clock and initiates a conversion. The start convert input must remain logic 0 during conversion, as the internal clock is stopped by logic 1 and the output will be erroneous. Another start convert pulse during a conversion does not reset and restart a conversion; it may momentarily stop the internal clock and produce an erroneous output.

Status output, pin 20, is logic 1 during conversion. When a conversion is complete, Status drops to logic 0 and the internal clock is turned off. Refer to the timing diagram, Figure 4.

7.6 Continuous Conversion. The ADC87 will continuously convert, commencing a new conversion immediately after the last conversion, when wired to accept an external clock. See paragraph 7.8 and Timing Considerations, paragraph 3.3.4. Alternately, the internal clock may be used with a new start convert common every 8.7μsec or slower.

7.7 Internal Clock and Clock Rate. The ADC87 is specified and tested using the internal clock. The internal clock is factory adjusted to 1.6MHz with Clock Rate, pin 17, connected to 0VDC (Digital Common). Under these conditions, the ADC87 will meet all the conversion speed and accuracy specifications.

The internal clock frequency may be increased or decreased by applying a positive or negative voltage to Clock Rate, pin 17 (see Figure 7). The circuits shown in Figure 8 may be used. Increasing the clock frequency decreases the conversion time; however, linearity errors increase as shown in Figures 9 and 10. Decreasing the clock frequency is accomplished by using a negative voltage or using an external clock (see paragraph 7.8).

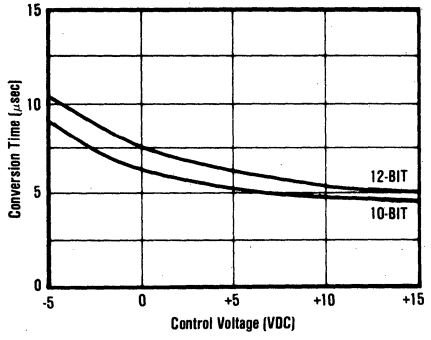
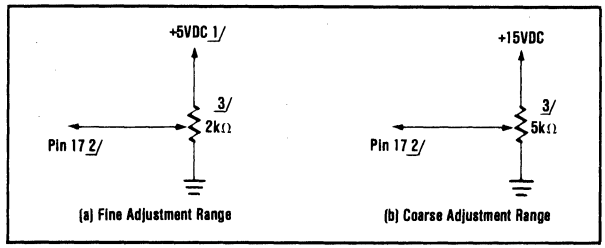


FIGURE 7. Clock Rate Control Voltage.



Notes:
1/ Use negative supply to decrease the clock frequency.
2/ Pin 17 is not connected to 0VDC when using clock rate adjustment potentiometer.
3/ Multiturn potentiometer with 100ppm/°C TCR or less.

FIGURE 8. Clock Rate Adjustment, Optional.

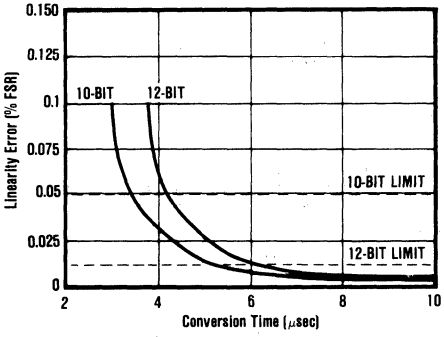


FIGURE 9. Linearity vs Conversion Time.

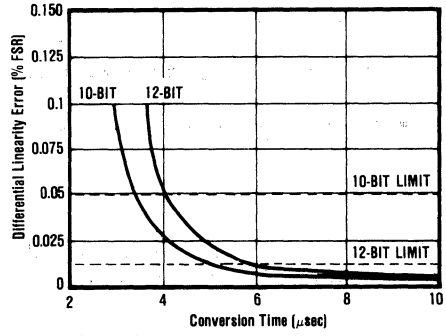


FIGURE 10. Differential Linearity vs Conversion Time.

7.8 External Clock. An external clock may be used with the ADC87 for synchronization or special timing applications. The external clock frequency must be lower than the internal clock frequency. However, the internal clock frequency may be increased; see paragraph 7.7.

The external clock is connected to the Start Convert terminal, pin 21. The normal, start convert positive pulse signal is not required. The external clock must be a negative-going pulse, 100nsec to 200nsec wide, at a frequency lower than the internal clock. The falling edge (leading edge) of the external clock starts the internal clock. The internal clock completes one cycle, then ceases as the Start Convert terminal, pin 21, is logic 1 at that time. The next external clock falling edge turns on the internal clock again, for one cycle. The Clock Output signal, pin 19, displays the internal clock synchronized to the lower, external clock frequency. A conversion is complete and Status output drops to logic 0 after 13 clock pulses.

The converter will provide continuous conversions as long as the external clock signal is present. A conversion is complete when Status output drops to logic 0. Status remains logic 0 for one external clock period. The next conversion starts on the next falling edge of the external clock following conversion completion. Conversions cease when Start Convert input is logic 1.

A circuit to generate an external clock signal from a clock with an arbitrary duty cycle is shown in Figure 11. A circuit to generate an external clock signal from a convert command is shown in Figure 12.

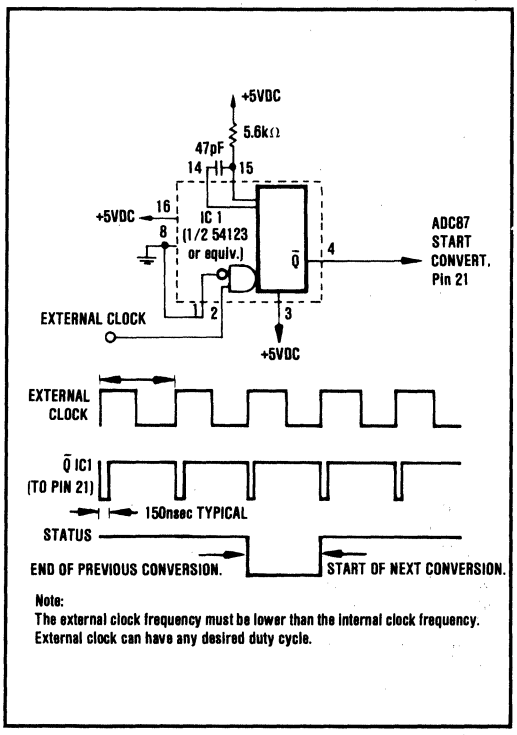


FIGURE 11. Continuous Conversion Using External Clock with Arbitrary Duty Cycle.

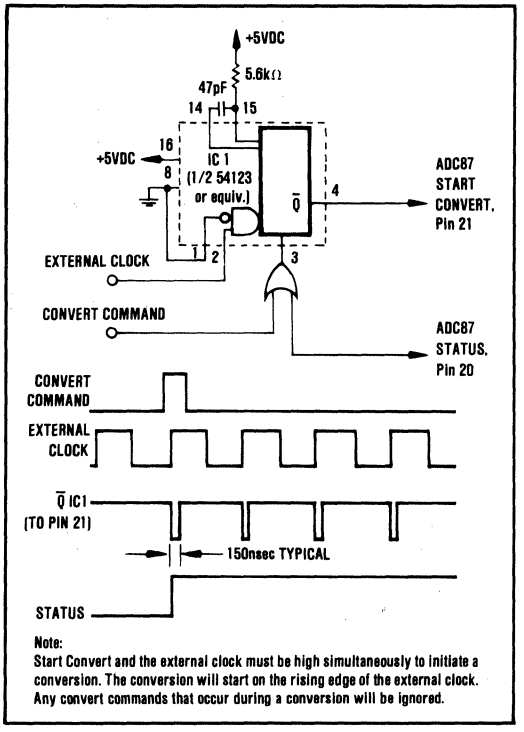


FIGURE 12. Conversion Initiated by Convert Command Using Continuous External Clock.

7.9 Short Cycle. The ADC87 conversion cycle may be stopped prior to converting all 12 bits. This provides faster conversions to less resolution. For conversions to n bits, connect the n + 1 bit output to Short Cycle, pin 14. The remaining bits are truncated.

Figure 13 shows a complete cycle and a short cycle to 10 bits. For 10 bits the internal clock frequency has been increased to provide the minimum conversion time. See Clock Rate, paragraph 7.7.

Resolution (bits)	12	10
Clock Rate connect pin 17 to pin	15	16
Short Cycle connect pin 14 to pin	16	2
Conversion Speed μsec, max	8	5

FIGURE 13. Short Cycle Connections.

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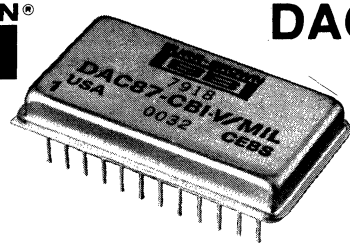


DAC87/MIL SERIES

MODEL NUMBERS:

DAC87-CBI-V/MIL	DAC87U-CBI-V/B
DAC87-CBI-V/B	DAC87U-CBI-V
DAC87-CBI-V	1/

REVISION B
OCTOBER, 1981

12-Bit -55°C to +125°C Military DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **HI-REL MANUFACTURE**
- **COMPLETELY SPECIFIED, -55°C to +125°C**
- **ACCURATE**
  - **±1/2LSB max Linearity, over temperature**
  - **±20ppm/°C max Gain Drift**
  - **±0.2% Total Error, over temperature**
  - **Monotonic, over temperature**
- **OPTIONAL MIL-STD-883 SCREENING**
- **DAC85 PIN-COMPATIBLE**
- **COMPLETE - INTERNAL REFERENCE AND OUTPUT AMPLIFIER**

DAC87 MIL

DESCRIPTION

The DAC87/MIL Series is a high performance, 12-bit, TTL-compatible, -55°C to +125°C digital-to-analog converter in a metal, welded, hermetically sealed package, and it is manufactured on a separate hi-rel production line. It is pin-compatible with DAC85 converters and has five user-selected output ranges. Each DAC is a complete device with an internal output amplifier and an ultra-stable reference.

The DAC87/MIL Series is designed for high accuracy, wide temperature applications. The total accuracy without external trim adjustments is ±0.1% of FSR, decreasing to only ±0.3% of FSR over -55°C to +125°C. With external offset and gain trim adjustments at +25°C, the total accuracy is less than ±0.2% of FSR over -55°C to +125°C. Gain drift is less than 20ppm/°C. Linearity error, contributed mostly by the internal current switches and resistive ladder, is reduced by laser trimming to less than ±1/2LSB over temperature. Differential linearity is less than ±1LSB over temperature thereby guaranteeing monotonicity from -55°C to +125°C.

There are two electrical performance grades and three product assurance levels allowing a wide application/budget choice. The DAC87-CBI-V model/grade features excellent performance from -55°C to +125°C and finds wide military, aerospace, and industrial applications. The DAC87U-CBI-V model/grade features excellent performance from -25°C to +85°C, and guarantees specifications from -55°C to +125°C. Applications include test equipment, shipboard, ground support, and shirt-sleeve environments where operation is between -25°C and +85°C but full temperature operation must be assured.

The three product assurance levels available are: standard; /B (100% screened per MIL-STD-883 method 5008, hybrid class, class B); and /MIL (100% screened, plus PDA = 10%, plus Groups A and B testing on each inspection lot, plus Groups C and D performed initially, periodically, and when specified on the customer's purchase order). See paragraph 1.2.2 for more details. Each device is manufactured in a hi-rel environment with clean room conditions which assures "built-in" quality.

1/ Current output models are also available. Contact Burr-Brown.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
DIGITAL-TO-ANALOG CONVERTER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a 12-bit, TTL-compatible, integrated circuit, digital-to-analog converter.

1.2 Part Number. The complete part number is as shown below.

DAC87		—	CBI	—	V	/MIL
Basic model number	Grade (see 1.2.1)		Input coding (Complementary Binary)		Voltage output 1/	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, 12-bit, digital-to-analog converter. The input coding is complementary binary. The device may be externally pin-connected for either Complementary Straight Binary (CSB) or Complementary Offset Binary (COB) coding (see Tables V and VI).

There are two electrical performance grades. The premium grade has no grade designation in the part number and features specifications and tests from -55°C to +125°C. The U grade has a U grade designation in the part number and features specifications and tests from -25°C to +85°C, and specifications from -55°C to +125°C.

Electrical specifications are shown in Table I; electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel Product Designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
	Additional electrical testing is performed on /MIL models.
/B	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is as defined in Figure 1. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage, V_{CC}	±18VDC
Supply voltage, V_{DD}	0VDC to +18VDC
Data input voltage	-1VDC to +7VDC
Output short circuit duration	Unlimited 2/
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60sec)	+300°C
Junction temperature	T_J = 175°C

1/ Current output models are also available. Contact Burr-Brown.
2/ Short circuit may be to ground only. Rating applies to 115°C case temperature or 65°C ambient temperature.

1.2.5 Recommended operating conditions.

Supply voltage range	V_{CC}: ±14.5VDC to ±15.5VDC V_{DD}: +4.75VDC to +5.25VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
24-lead can	Figure 1	1350mW at T_A = 125°C	7°C/W 1/	37°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microcircuits.

3. REQUIREMENTS

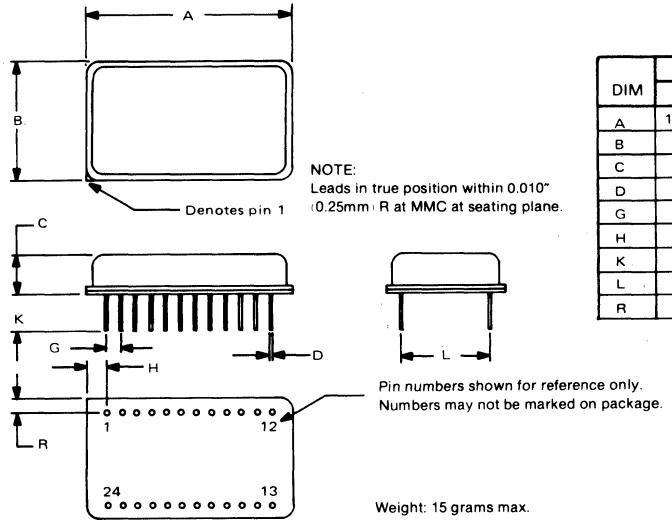
3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1. Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510 except organic and polymeric materials may be used for substrate and die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

FIGURE 1. Case Outline (Double-Wide DIP Configuration).

1/ Rating applies to normal device operation. For the output short circuit condition, the maximum θJ-C of the output die of 100°C/W must be applied to the output short circuit current.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice utilized are glassivated.

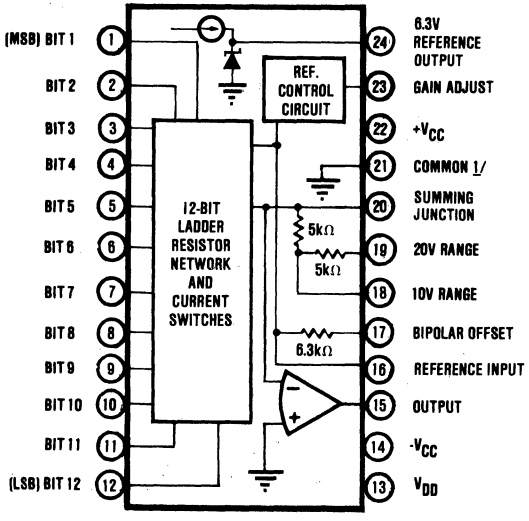
3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Offset and gain error adjustment. The DAC is capable of being externally adjusted to zero offset error and to zero gain error using the circuits in Figure 3. See applications information, paragraph 7.3.

3.3.2 Input coding. The input coding is complementary binary. The digital input code to yield the corresponding output voltage for the output ranges is specified in Table V.

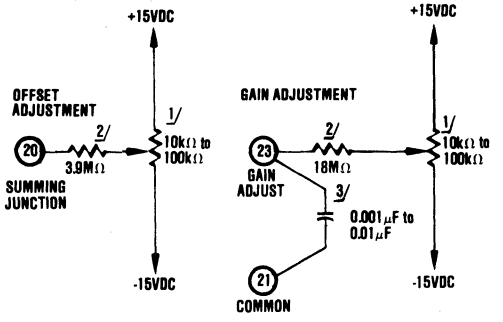
3.3.3 Output range. The output range is specified in Table VI when externally connected as shown therein.

3.4 Electrical test requirements. Electrical test requirements are specified in Table II. The subgroups of Table III and limits of Table IV which constitute the minimum electrical test requirements for screening, qualification, and quality conformance, are specified in Table II.



1/ Pin 21 is connected to the case.

FIGURE 2. Terminal Connections.



1/ ≤100ppm/°C.
2/ ±20% carbon composition or better. Locate close to the DAC87 to prevent noise pickup.
3/ Ceramic.

FIGURE 3. Offset and Gain Error Adjustment Circuits.

TABLE I. Electrical Performance Characteristics.

CHARACTERISTICS	CONDITIONS 1/	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V			LIMITS DAC87U-CBI-V/B DAC87U-CBI-V			UNITS 2/
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION		12			12			Bits
DIGITAL INPUTS								
Input voltage								
Logic "1"	T_A = +25°C	2.0		5.5	*		*	V
	-55°C ≤ T_A ≤ +125°C	2.4		5.5	*		*	V
Logic "0"	T_A = +25°C	0		0.8	*		*	V
	-55°C ≤ T_A ≤ +125°C	0		0.4	*		*	V
Input Current								
Logic "1"	V_{IN} = 2.4V			+40			*	μA
Logic "0"	V_{IN} = 0.4V	-1.6		0	*		*	mA
ACCURACY								
Total error, untrimmed 3/	T_A = +25°C			±0.10			*	% of FSR
Unipolar	-25°C ≤ T_A ≤ +85°C						±0.25	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.30				% of FSR
Bipolar	T_A = +25°C			±0.10			*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.25	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.30				% of FSR
Total error, trimmed 3/ 4/								
Unipolar	T_A = +25°C		±0.006	±0.0122		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.15	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.20				% of FSR
Bipolar	T_A = +25°C		±0.006	±0.0122		*	*	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.15	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.20				% of FSR
Linearity error	T_A = +25°C		±0.25	±0.50		±0.25	±0.50	LSB
	-25°C ≤ T_A ≤ +85°C						±0.50	LSB
	-55°C ≤ T_A ≤ +125°C			±0.50			±3	LSB
Differential linearity error 5/	T_A = +25°C		±0.50	±0.75		±0.50	±0.75	LSB
	-25°C ≤ T_A ≤ +85°C						±1.0	LSB
	-55°C ≤ T_A ≤ +125°C			±1.0			±3	LSB
Monotonicity temperature range 5/		-55		+125	-25		+85	°C
Offset error 6/								
Unipolar 7/	T_A = +25°C		±0.02	±0.05		±0.02	±0.05	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.068	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.08				% of FSR
Bipolar 7/	T_A = +25°C		±0.02	±0.05		±0.02	±0.05	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.10	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.10				% of FSR
Offset temperature sensitivity 7/								
Unipolar	-25°C to +85°C					±1	±3	ppm of FSR/°C
	-55°C to +125°C		±1	±3				ppm of FSR/°C
Bipolar	-25°C to +85°C						±10	ppm of FSR/°C
	-55°C to +125°C		±5	±10			±30	ppm of FSR/°C
Offset adjustment range		±0.15	±0.2		*	*		% of FSR
Gain error 6/ 8/								
Unipolar 7/	T_A = +25°C		±0.05	±0.10		±0.05	±0.10	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.20	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.25				% of FSR
Bipolar 7/	T_A = +25°C		±0.05	±0.10		±0.05	±0.10	% of FSR
	-25°C ≤ T_A ≤ +85°C						±0.20	% of FSR
	-55°C ≤ T_A ≤ +125°C			±0.25				% of FSR
Gain temperature sensitivity 7/								
Unipolar	-25°C to +85°C					±10	±20	ppm/°C
	-55°C to +125°C		±10	±20				ppm/°C
Bipolar	-25°C to +85°C					±10	±20	ppm/°C
	-55°C to +125°C		±10	±20			±60	ppm/°C
Gain adjustment range		±0.2	±0.3		*	*		% of FSR
DYNAMIC CHARACTERISTICS								
Slew rate		10	20		*	*		V/μsec
Settling time	ΔV_O = 20V to ±1/2LSB		5	7		*	*	μsec
	ΔV_O = 10V to ±1/2LSB		3	6		*	*	μsec
	ΔV_O = 1LSB to ±1/2LSB		1.5	3		*	*	μsec
ANALOG OUTPUT								
Output voltage range 9/				±10			*	V
Output current 10/		±5			*			mA
Output resistance, DC			0.05	0.2		*	*	Ω
Output short circuit current	T_A = +25°C	±5		±40	*		*	mA

DAC87 MIL

TABLE I. Electrical Performance Characteristics (cont).

CHARACTERISTICS	CONDITIONS 1/	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MIN	TYP	MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	TYP	MAX	UNITS 2/
INTERNAL REFERENCE								
Internal reference voltage (V_R)		±6.0	±6.3	±6.6	*	*	*	V
Internal reference temperature sensitivity	-25°C to +85°C					±5	±10	ppm of V_R/°C
	-55°C to +125°C		±5	±10			±30	ppm of V_R/°C
Output current from internal reference	for specified V_R			200			*	µA
POWER SUPPLY								
Power supply range								
+V_{CC}		+14.0	+15	+16.0	*	*	*	V
-V_{CC}		-14.0	-15	-16.0	*	*	*	V
V_{DD}		+4.75	+5	+15.5	*	*	*	V
Power supply sensitivity								
±V_{CC}	±V_{CC} = 15V ±0.5V		±0.002	±0.004		*	*	% of FSR/%V_{CC}
V_{DD}	V_{DD} = 5V ±0.25V		±0.001	±0.002		*	*	% of FSR/%V_{DD}
Power supply current (quiescent)								
±V_{CC}	T_A = +25°C		±20	±30		*	*	mA
	-55°C ≤ T_A ≤ +125°C			±30			*	mA
V_{DD}	T_A = +25°C		20	25		*	*	mA
	-55°C ≤ T_A ≤ +125°C			25			*	mA
TEMPERATURE RANGE								
Operating		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C

*Specification same as DAC87-CBI-V

NOTES:

1/ ±V_{CC} = 15V, V_{DD} = 5V, -55°C ≤ T_A ≤ +125°C, unless otherwise specified.

2/ FSR = Full Scale Range (Example: The FSR is 20V for ±10V range, 10V for ±5V range, and 10V for 0 to +10V range.) LSB = Least Significant Bit.

3/ Total error includes all errors at any fixed power supply voltage within the recommended supply voltage range, including the internal reference, linearity error, offset error, and gain error.

4/ Offset and gain externally trimmed to zero error at T_A = +25°C.

5/ Monotonicity is assured by testing differential linearity to ±1LSB maximum.

6/ Externally adjustable to zero.

7/ The reference error is included.

8/ The offset error is specified separately and is not included herein.

9/ The output voltage range is determined by external conditions (see Table VI).

10/ Limit is assured by testing output resistance where R_{LOAD} = 2kΩ.

TABLE II. Electrical Test Requirements

(The individual tests within the subgroups appear in Table III)

MODELS / MIL-STD-883 test requirements (hybrid class)	DAC87-CBI-V/MIL	DAC87-CBI-V/B DAC87-CBI-V	DAC87U-CBI-V/B DAC87U-CBI-V
	Subgroups (see Table III)		
Interim electrical parameters (preburn-in) (method 5008)	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4	1, 2, 3	1, 2U, 3U
Group A test requirements (method 5008)	1, 2, 3, 4	--	--
Group C end point electrical parameters (method 5008)	Table IV delta limits and limits	--	--
Additional electrical subgroups performed prior to Group C inspections	2C, 3C, 5, 6	--	--

*PDA applies to subgroup 1 (see 4.3.d)

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufactuer's designating symbol (CEBS)
f. Country of origin (U.S.A.)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and trainings, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding, for the /MIL Hi-Rel product designation are in accordance with MIL-M-38510.

1/ A 4-digit date code, indicating year and week of seal, is marked on /B and (none) Hi-Rel product designations.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for /MIL and /B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

Screening for the standard model, (none) Hi-Rel product designation, includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition D), and external visual inspection per MIL-STD-883, method 5008, hybrid class.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the MIL Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MIN	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MAX	UNITS
1	Offset error, bipolar	5	±10V range (ideal value = -10.000V)		±10		±10	mV
T_A = +25°C	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) 2/		±20		±20	mV
	Linearity error, bipolar	5	±10V range 3/ 4/					
			For + bit errors		+2.44		+2.44	mV
			For - bit errors		-2.44		-2.44	mV
	Differential linearity error, bipolar	5	±10V range 4/ 5/		±3.66		±3.66	mV
	Total error, untrimmed, bipolar	5			±20		±20	mV
	Total error, trimmed, bipolar	6/			--		--	
	Internal reference voltage	5		+6.0	+6.6	+6.0	+6.6	V
	Input voltage	--	Logic "1", all inputs, V_{in} = 5.0VDC to 2.0VDC, measure ΔV_o		±4		±4.8	mV
		--	Logic "0", all inputs, V_{in} = 0VDC to 0.8VDC, measure ΔV_o		±4		±4.8	mV
	Input current	--	Logic "1", each input, V_{in} = +2.4VDC		+40		+40	µA
		--	Logic "0", each input, V_{in} = +0.4VDC	-1.6	0	-1.6	0	mA
	Power supply current	5	No load $+V_{CC}$		30		30	mA
		5	No load $-V_{CC}$		30		30	mA
		5	No load V_{DD}		25		25	mA
	Output resistance	5	$R_o = \frac{(V_o \text{ no load}) - (V_o 2k\Omega \text{ load})^*}{5mA}$		0.2		0.2	Ω
	Output short circuit current	--	R_{load} = 1Ω, V_o = +FS and -FS	±5	±40	±5	±40	mA
	Power supply sensitivity	5	±10V range, V_o = +FS, ΔV_{CC} = +0.5V and -0.5V		±2.6		±2.6	mV
			±10V range, V_o = +FS, ΔV_{DD} = +0.25V and -0.25V		±2.0		±2.0	mV
	Offset adjustment range	4	±10V range	±30		±30		mV
	Gain adjustment range	4	±10V range	±40		±40		mV
	Offset error, unipolar	5	0 to +10V range (ideal value = 0.00V)		±5		±5	mV
	Gain error, unipolar	5	0 to +10V range (ideal value = +9.997559V) 2/		±10		±10	mV
	Total error, untrimmed, unipolar	5	0 to +10V range		±10		±10	mV
2	Offset error, bipolar (V_{OE})	5	±10V range (ideal value = -10.000V)		±20			mV
T_A =+125°C	Gain error, bipolar (G_E)	5	±10V range (ideal value = +9.995117V) 2/		±50			mV
	Offset temperature sensitivity, Bipolar	--	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE125} - V_{OE25}}{100°C}$		±0.20			mV/°C
	Gain temperature sensitivity, Bipolar	--	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E125} - G_{E25}}{100°C}$		±0.40			mV/°C
	Linearity error, bipolar	5	±10V range, 3/ 4/					
			For + bit errors		+2.44			mV
			For - bit errors		±2.44			mV
	Differential linearity error, bipolar	5	±10V range 4/ 5/		±4.88			mV
	Total error, untrimmed, bipolar	5	±10V range		±60			mV

*V_o = +full scale

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MIN	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MAX	UNITS
	Total error, trimmed, bipolar	5	±10V range 7/		±40			mV
	Internal reference voltage	5		+6.0	+6.6			V
	Internal reference temperature sensitivity	--	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R125} - V_{R25}}{100°C}$		±63			µV/°C
2C T_A = +125°C	Power supply current	5	No load $+V_{CC}$		30			mA
		5	No load $-V_{CC}$		30			mA
		5	No load V_{DD}		25			mA
2U T_A = +85°C	Offset error, bipolar (V_{OE})	5	±10V range (ideal value = -10.000V)				±20	mV
	Gain error, bipolar (G_E)	5	±10V range (ideal value = +9.995117V) 2/				±40	mV
	Offset temperature sensitivity, Bipolar	--	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE85} - V_{OE25}}{60°C}$				±0.20	mV/°C
	Gain temperature sensitivity, Bipolar	--	±10V range, $\frac{\Delta V_{GE}}{\Delta T} = \frac{G_{E85} - G_{E25}}{60°C}$				±0.40	mV/°C
	Linearity error, bipolar	5	±10V range, 3/ 4/					
			For + bit errors				+2.44	mV
			For - bit errors				-2.44	mV
	Differential linearity error, bipolar	5	±10V range 4/ 5/				±4.88	mV
	Total error, untrimmed, bipolar	5	±10V range				±50	mV
	Total error, trimmed, bipolar	5	±10V range 7/				±30	mV
	Internal reference voltage	5				+6.0	+6.6	V
	Internal reference temperature sensitivity	--	$\frac{\Delta V_R}{\Delta T} = \frac{V_{R85} - V_{R25}}{60°C}$				±63	µV/°C
3 T_A = -55°C	Offset error, bipolar	5	±10V range (ideal value = -10.000V)		±20			mV
	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) 2/		±50			mV
	Offset temperature sensitivity, Bipolar	--	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-55}}{80°C}$		±0.20			mV/°C
	Gain temperature sensitivity, Bipolar	--	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-55}}{80°C}$		±0.40			mV/°C
	Linearity error, bipolar	5	±10V range 3/ 4/					
			For + bit errors		+2.44			mV
			For - bit errors		-2.44			mV
	Differential linearity error, bipolar	5	±10V range 4/ 5/		±4.88			mV
	Total error, untrimmed bipolar	5	±10V range		±60			mV
	Total error, trimmed bipolar	5	±10V range 7/		±40			mV
	Internal reference voltage	5		+6.0	+6.6			V
	Internal reference temperature sensitivity		$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R\ 55}}{80°C}$		±63			µV/°C
3C T_A = -55°C	Power supply current	5	No load $+V_{CC}$		30			mA
		5	No load $-V_{CC}$		30			mA
		5	No load V_{DD}		25			mA
3U T_A = -25°C	Offset error, bipolar	5	±10V range (ideal value = -10.000V)				±20	mV
	Gain error, bipolar	5	±10V range (ideal value = +9.995117V) 2/				+40	mV
	Offset temperature sensitivity, Bipolar	--	±10V range, $\frac{\Delta V_{OE}}{\Delta T} = \frac{V_{OE25} - V_{OE-25}}{50°C}$				±0.20	mV/°C
	Gain temperature sensitivity, Bipolar	--	±10V range, $\frac{\Delta G_E}{\Delta T} = \frac{G_{E25} - G_{E-25}}{50°C}$				+0.40	mV/°C
	Linearity error, bipolar	5	±10V range 3/ 4/					
			For + bit errors				+2.44	mV
			For - bit errors				-2.44	mV
	Differential linearity error, bipolar	5	±10V range 4/ 5/				±4.88	mV
	Total error, untrimmed bipolar	5	±10V range				±50	mV
	Total error, trimmed bipolar	5	±10V range 7/				±30	mV
	Internal reference voltage	5				+6.0	+6.6	V
	Internal reference temperature sensitivity		$\frac{\Delta V_R}{\Delta T} = \frac{V_{R25} - V_{R\ 25}}{50°C}$				±63	µV/°C

TABLE III. Group A Inspection (cont).

SUBGROUP	PARAMETERS	TEST CIRCUIT FIGURE	CONDITIONS 1/	LIMITS DAC87-CBI-V/MIL DAC87-CBI-V/B DAC87-CBI-V MIN	MAX	LIMITS DAC87U-CBI-V/B DAC87U-CBI-V MIN	MAX	UNITS
4 T_A = +25°C	Settling time Slew rate	6 6	To ±1/2LSB, ΔV_O = 20V ΔV_O = 20V, 10% to 90%	 10	7			µsec V/µsec
5 T_A = +125°C	Settling time Slew rate	6 6	To ±1/2LSB, ΔV_O = 20V ΔV_O = 20V, 10% to 90%	 10	7			µsec V/µsec
6 T_A = -55°C	Settling time Slew rate	6 6	To ±1/2LSB, ΔV_O = 20V V_O = 20V, 10% to 90%	 10	7			µsec V/µsec

NOTES:
1/ $\pm V_{CC}$ = 15VDC, V_{DD} = 5VDC, Logic 1 = 4V, Logic 0 = 0.2V, no load, unless otherwise specified.
2/ Offset error corrected to zero.
3/ The individual bit errors that are positive are switched on and compared to 1/2LSB. The individual bit errors that are negative are switched on and compared to 1/2LSB. This guarantees ±1/2LSB maximum linearity error.
4/ Offset error and gain error correction factors for the Device Under Test (DUT), if any, are applied to the DUT output voltage before comparing the DUT output voltage to the ideal output voltage. This is the basis for linearity error and differential linearity error relative to a straight line through the end points of the transfer function.
5/ Differential linearity error is tested at all combinations of the four most significant bits.
6/ Total error, trimmed, (bipolar) is the same as linearity error, bipolar.
7/ Offset and gain errors adjusted to zero at T_A = +25°C.

TABLE IV. Group C, End Point Electrical Parameters.
(T_A = +25°C, $\pm V_{CC}$ = 15VDC, V_{DD} = +5VDC)

Test	Limit	Delta
Total error, untrimmed, bipolar	±0.15% of FSR	±0.12% of FSR
Linearity error, bipolar	±1.0LSB	±0.75LSB
Differential linearity error, bipolar	+1.2LSB, -1.0LSB	±0.6LSB
Monotonicity	Yes	--
Offset error, bipolar	±0.125% of FSR	±0.10% of FSR
Gain error, bipolar	±0.25% of FSR	±0.25% of FSR

TABLE V. Ideal Output Voltage vs Digital Input Code.

Output Range	Digital Input Code (Complementary 12-Bit Binary) 1111 1111 1111	0111 1111 1111	0000 0000 0000
-2.5V to +2.5V	-2.500V	0	+2.498779V
-5V to +5V	-5.000V	0	+4.997559V
-10V to +10V	-10.000V	0	+9.995117V
0 to +5V	0	+2.500V	+4.998779V
0 to +10V	0	+5.000V	+9.997559V

NOTES:
1. One LSB = 1.2207mV for a 5-volt full scale range. One LSB = 2.4414mV for a 10-volt full scale range. One LSB = 4.8828mV for a 20-volt full scale range.
2. Digital input codes are shown with the MSB listed first.

TABLE VI. Output Range Selection.

Output Range	Required External Pin Connections			
-2.5V to +2.5V	15 to 18	17 to 20	19 to 20	16 to 24
-5V to +5V	15 to 18	17 to 20	19 NC	16 to 24
-10V to +10V	15 to 19	17 to 20	19 to 15	16 to 24
0 to +5V	15 to 18	17 to 21	19 to 20	16 to 24
0 to +10V	15 to 18	17 to 21	19 NC	16 to 24

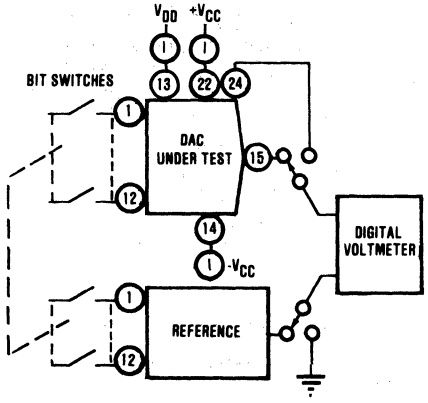


FIGURE 5. Test Circuit - Simplified.

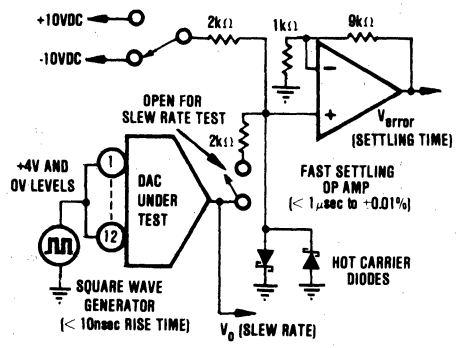


FIGURE 6. Slew Rate and Settling Time Test Circuit.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, medhod 5008, except as modifed herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 7 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

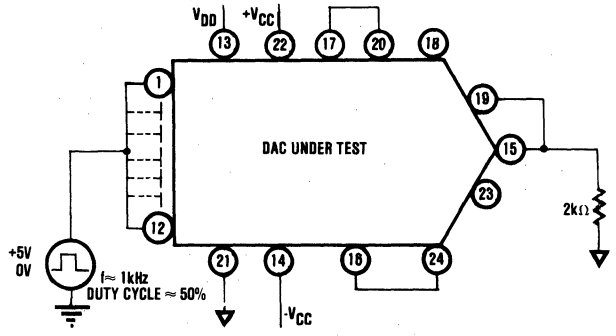


FIGURE 7. Test Circuit-Burn-in and Operating Life Test.

d. Percent defective allowable (PDA). The PDA, for /MIL Hi-Rel product designations only, is 10 percent and includes both parametric and catastropic failures. It is based on failures from group A, subgroup 1 test after

cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Group D, subgroup 1, seal test, of MIL-STD-883, method 5008, is performed on each lot of packages procured. Groups C and D inspection (except for subgroup 1, seal test) of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table I, and as follows:

a. Tests are specified in Table II herein.

b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table II and as follows:

a. Particle impact noise detection test is not required.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table III, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 7 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table IV and as follows:

a. Particle impact noise detection test is not required.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2)

b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Offset error. Offset error is the difference between the ideal analog output voltage and the actual output voltage, when all the input bits are off (digital input code 1111 1111 1111).

Gain error. Gain error is the difference between the ideal analog output voltage span and the actual output voltage span, between when all the input bits are off (digital input code 1111 1111 1111) and when all the input bits are on (digital input code 0000 0000 0000).

Linearity error. Linearity error is the difference between the ideal analog output voltage and the actual output voltage, when the offset error and the gain error equal zero.

Differential linearity. Differential linearity is the difference between the ideal (1LSB) analog output voltage change, for 1-bit change in digital input code, and the actual output voltage change. A differential linearity of ±1LSB means that the output can change anywhere from 0LSB to 2LSB when the input changes from one adjacent input code to the next. Differential linearity of ±1LSB or less guarantees monotonicity.

Monotonicity. Monotonicity is the condition where the analog output increases or remains the same for an increase in input codes.

Unipolar output. Unipolar is an output characteristic that displays zero volts output at one input extreme and full scale volts output at the other input extreme.

Bipolar output. Bipolar is an output characteristic that displays full scale output voltage at one input extreme and the opposite full scale output voltage at the other input extreme.

6.5 Microcircuit group assignment. These microcircuits are in Technology Group F as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. APPLICATIONS INFORMATION

7.1 Power Supply Decoupling. For optimum performance and noise rejection, each power supply should be decoupled by connecting a 1μF tantalum capacitor from each power supply pin to the ground plane.

7.2 Power supply sensitivity. Power supply sensitivity is specified in Table I. Power supply sensitivity versus ripple frequency is shown in Figure 8.

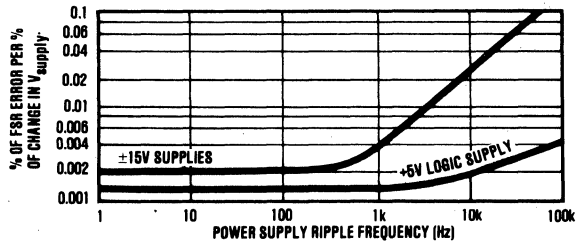


FIGURE 8. Typical Power Supply Sensitivity vs Power Supply Ripple.

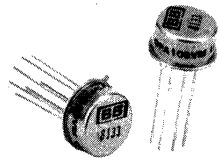
7.3 External offset and gain error adjustment. The untrimmed accuracy of the DAC87/ MIL Series is very good and is adequate for many applications. However, when the initial offset and gain errors are greater than what can be allowed in the application, the circuits shown in Figure 4 may be connected and the offset and gain errors may be adjusted to zero.

7.3.1 Offset adjustment. Apply the digital input code, 1111 1111 1111, which should produce zero volts output for the unipolar ranges, or minus full scale for the bipolar ranges. Adjust the offset potentiometer until the output, for the output range being used, is exactly as depicted in Table V.

7.3.2 Gain adjustment. Apply the digital input code, 0000 0000 0000, which should produce positive full scale. Adjust the gain potentiometer until the output, for the output range being used, is exactly as depicted in Table V.

BURR-BROWN®

OPA105/MIL SERIES



MODEL NUMBERS:

OPA105VM/MIL	OPA105WM/MIL
OPA105VM/883B	OPA105WM/883B
OPA105VM	OPA105WM
OPA105UM/883B	REVISION NONE
OPA105UM	FEBRUARY, 1982

FET Input Military OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, 1pA, max
- HIGH INPUT IMPEDANCE, $10^{13}\Omega$
- ULTRA-LOW DRIFT, $2\mu V/°C$, max
- LOW OFFSET VOLTAGE $250\mu V$, max
- LOW QUIESCENT CURRENT, 1.5mA, max
- HERMETICALLY SEALED TO-99 PACKAGE

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS

DESCRIPTION

The OPA105/MIL Series is a low bias current operational amplifier. Guaranteed low initial offset voltage ($250\mu V$, max) and associated drift versus temperature ($2\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. This feature, and guaranteed low bias current (1pA, max), allow greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA105/MIL Series include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA105/MIL Series allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-468

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a FET input, low bias current, low drift, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

OPA105	V	M	/MIL
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single operational amplifier. Three electrical performance grades are provided. The W grade features $\pm 2\mu V/^{\circ}C$ drift (-55°C to +125°C). The V grade features $\pm 5\mu V/^{\circ}C$ drift (-55°C to +125°C). The U grade features excellent performance ($\pm 15\mu V/^{\circ}C$) from -25°C to +85°C and guarantees performance from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel product designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter. Additional electrical testing is performed on /MIL models.
/883B	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is A-1 (8-lead can, TO-99) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC [1]
Differential input voltage range	±40VDC [1]
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited [2]
Lead temperature (soldering, 60sec)	300°C
Junction temperature	$T_J = 175^{\circ}C$

1.2.5 Recommended operating conditions.

Supply voltage range	±5VDC to ±20VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-A
8-lead can	Figure 1	225mW at $T_A = 125^{\circ}C$	220°C/W

1 The absolute maximum input voltage is equal to the supply voltage.
2 Short circuit may be to ground only. Rating apples to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

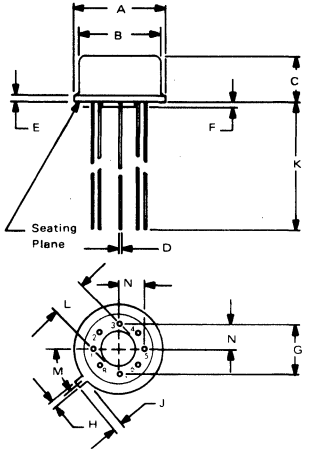
3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510. See Figure 1 for the case outline.



Note:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	-	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 1. Case Outline (TO-99) Package Configuration.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice are glassivated.

3.2.9 Schematic Circuit. The schematic circuit is shown in Figure 3.

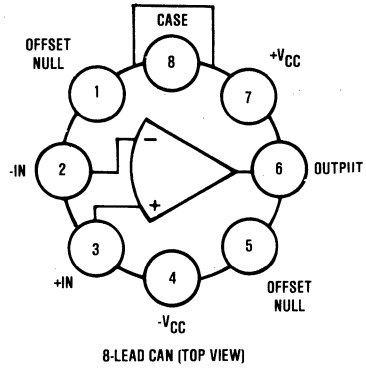


FIGURE 2. Circuit Diagram and Terminal Connections.

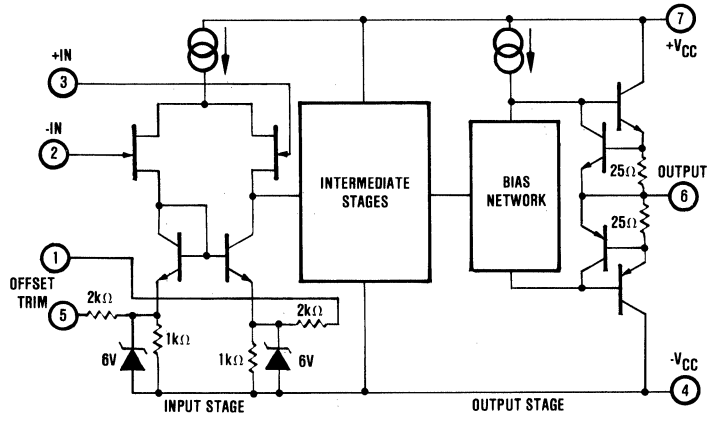


FIGURE 3. Simplified Schematic Circuit.

3.3 Electrical Performance Characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Additional Electrical Performance Characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 4. If nulling is unnecessary for the application, delete the three components and make no connections.

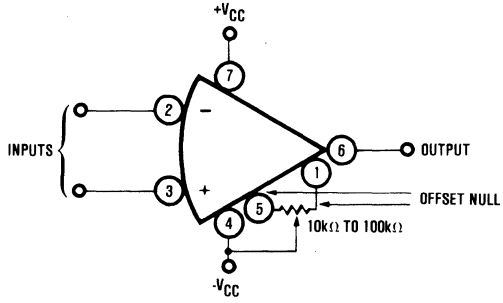


FIGURE 4. Offset Null Circuit.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated at any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code [1]
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin (U.S.A.)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the /MIL Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for /MIL Hi-Rel product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component log. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

OPA105 MIL

[1] a 4-digit date code, indicating year and week of seal, is marked on 883B and (none) Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics.

All characteristics at -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise specified.

CHARACTERISTIC	SYMBOL	CONDITIONS	OPA105WM/MIL** OPA105WM/883B OPA105WM			OPA105VM/MIL** OPA105VM/883B OPA105VM			OPA105UM/883B OPA105UM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN												
Open-Loop Voltage Gain	Avs	R_L = 2kΩ, V_O = ±10V, F = 0Hz; T_A = +25°C	106	112		*	*		*	*		dB
		R_L = 2kΩ, V_O = ±10V, F = 0Hz; -55°C ≤ T_A ≤ +125°C	100	106		*	*		*	*		dB
RATED OUTPUT												
Voltage	V_O	R_L = 2kΩ	±10	±12		*	*		*	*		V
Current	I_O		±5	±10		*	*		*	*		mA
Impedance	Z_O	T_A = +25°C		3			*			*		kΩ
Load Capacitance(1)	C_L	T_A = +25°C	500	1000		*	*		*	*		pF
Short Circuit Current	I_{OS}	To Ground	10	25		*	*		*	*		mA
DYNAMIC RESPONSE												
Bandwidth	BW	Unity Gain-Small Signal T_A = +25°C		1			*			*		MHz
Bandwidth	BW	Full Power T_A = +25°C	14	20		*	*		*	*		kHz
Slew Rate	SR	R_L = 2kΩ, T_A = +25°C	0.9	1.3		*	*		*	*		V/μsec
Settling Time (0.1%)	T_S	T_A = +25°C		9			*			*		μsec
Settling Time (0.01%)	T_S	T_A = +25°C		20			*			*		μsec
Overload Recovery(2)	T_r	T_A = +25°C		4	15		*	*		*	*	μsec
INPUT OFFSET VOLTAGE												
Initial Offset	V_{IO}	T_A = +25°C			±250			*			*	μV
Temperature Sensitivity	DV_{IO}	$\frac{V_{OS}(T_A) - V_{OS}(+25°C)}{\Delta T}$										
		-55 ≤ T_A ≤ +125°C			±2			±5			±25	μV/°C
		-25 ≤ T_A ≤ +85°C									±15	μV/°C
vs Power Supply	PSRR	V_{CC} = ±5, V_{CC} = ±20VDC			±74			*			*	dB
INPUT BIAS CURRENT												
Initial Bias	I_b	T_A = +25°C			1			*			*	pA
vs Supply Voltage		T_A = +25°C		0.005			*			*		pA/V
INPUT OFFSET CURRENT												
Initial Offset	I_{OS}	T_A = +25°C		±0.2			*			*		pA
INPUT IMPEDANCE												
Differential		T_A = +25°C		10^{13} ‖ 1.6			*			*		Ω ‖ pF
Common-Mode		T_A = +25°C		10^{15} ‖ 1.8			*			*		Ω ‖ pF
INPUT NOISE												
Voltage	e_n	f_O = 10Hz T_A = +25°C		55			*			*		nV/√Hz
		f_O = 100Hz T_A = +25°C		35			*			*		nV/√Hz
		f_O = 1kHz T_A = +25°C		30			*			*		nV/√Hz
		f_O = 10kHz T_A = +25°C		25			*			*		nV/√Hz
		f_B = 0.1Hz to 10Hz T_A = +25°C		3			*			*		μV/, p-p
Current	i_n	f_B = 0.1Hz to 10Hz T_A = +25°C		0.01			*			*		pA, p-p
		f_B = 10Hz to 10kHz T_A = +25°C		0.03			*			*		pA, rms
		f_O = 1kHz T_A = +25°C		0.6			*			*		fA/√Hz
INPUT VOLTAGE RANGE												
Differential	V_{ai}	T_A = +25°C	±20			*			*			V
Common-Mode		T_A = +25°C	±10	±12		*	*		*	*		V
Common-Mode Rejection	CMRR	V_{IN} = ±10V T_A = +25°C	76	86		*	*		*	*		dB
POWER SUPPLY												
Rated Voltage				±15			*			*		VDC
Voltage Range			±5		±20	*		*	*		*	VDC
Quiescent Current	Q			1.0	1.5		*	*		*	*	mA
TEMPERATURE RANGE (ambient)												
Operating			-55		+125	*		*	*		*	°C
Storage			-65		+150	*		*	*		*	°C

*Same as OPA105W Grade. **OPA105WM/MIL and OPA105VM/MIL available 4th quarter 1982.

NOTES:

1. Stability guaranteed with Load Capacitance ≤ 500pF and a 100Ω resistor in series with pin 6 for units manufactured prior to January 1, 1982.
2. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
3. Bias current is tested and guaranteed at T_A = +25°C. For higher temperature the bias current doubles every +10°C.

3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition B), and external visual inspection per MIL-STD-883, method 5008, hybrid class.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for /MIL Hi-Rel product designation, is in accordance with MIL-M-38510, expect as modified in paragraph 4.4 herein. The mircocircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883B REQUIREMENTS (hybrid class) / MODELS	OPA105WM/MIL	OPA105WM/883B OPA105WM	OPA105VM/MIL	OPA105VM/883B OPA105VM	OPA105UM/883B OPA105UM
Interim electrical parameters (pre burn-in) (method 5008)	1, 4	1, 4	1, 4	1, 4	1, 4
Final electrical test parameters (method 5008)	1*, 2, 3, 4	1, 2, 3, 4	1*, 2, 3, 4	1, 2, 3, 4	1, 2U, 3U, 4
Group A test requirements (method 5008)	1, 2, 3, 4	---	1, 2, 3, 4	---	---
Group C end point electrical parameters (method 5008)	Table IV Limits and Delta limits	---	Table IV Limits and Delta Limits	---	---
Additional electrical subgroups performed prior to Group C inspections	4C, 5, 6	---	4C, 5, 6	---	---

*PDA applies to subgroups 1, 4 (see 4.3d)

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC}$ = 15V unless otherwise specified	LIMITS OPA105WM/MIL OPA105WM/883B OPA105WM MIN	MAX	OPA105VM/MIL OPA105VM/883B OPA105VM MIN	MAX	OPA105UM/883B OPA105UM MIN	MAX	UNITS
	V_{IO}	4001			±250		±250		250	µV
	I_{IB}	4001			±1		±1		±1	pA
	V_O		R_L = 2kΩ	±10		±10		±10		V
1	I_Q				1.5		1.5		1.5	mA
T_A = +25°C	CMRR	4003	V_{CM} ±10V	76		76		76		dB
	PSRR		V_{CC} = ±5V, V_{CC} = ±20V	74		74		74		dB
2 T_A = +125	DV_{IO}	4001	$\frac{V_{OS}\ (+125) - V_{OS}\ (25)}{100}$		2		5			µV/°C
2U T_A = +85°C	DV_{IO}	4001	$\frac{V_{OS}\ (+85) - V_{OS}\ (25)}{60°C}$						15	µV/°C
3 T_A = -55°C	DV_{IO}	4001	$\frac{V_{OS}\ (25) - V_{OS}\ (-55)}{80}$		2		5			µV/°C
3U T_A = -25°C	DV_{IO}	4001	$\frac{V_{OS}\ (25) - V_{OS}\ (-25)}{50}$						15	µV/°C
4	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	106		106		106		dB
T_A = +25°C	SR	4002	R_L = 2kΩ, V_O = ±10V	0.9		0.9		0.9		V/µsec
4C T_A = +25°C	T_r		50% Input Overdive		15		15			µsec
5 T_A = +125°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	100		100				dB
6 T_A = -55°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	100		100				dB

TABLE IV. Group C, End Point Electrical Parameters

(T_A = +25°C, $\pm V_{CC}$ = 15VDC, V_{CM} = 0V)

TEST	LIMIT	DELTA
V_{IO}	±250μV	±125μV
I_{IB}	±1pA	±0.8pA

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply;

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.
b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) T_A = +125°C minimum
   (4) Test duration is 160 hours minimum
d. Percent defective allowable (PDA). The PDA, for /MIL Hi-Rel product designation only, is 10 percent and includes both parametric and catastropic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
e. External visual inspection need not include measurement of case and lead dimensions.

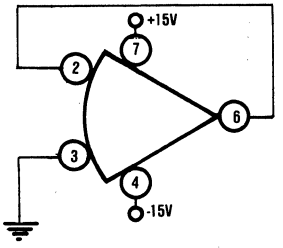


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, is performed on each lot. Group D, subgroup 1, seal test, of MIL-STD-883, method 5008, is performed on each lot of packages procured. Groups C and D inspections (except for subgroup 1, seal test) of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table I, and as follows:

a. Tests are specified in Table II herein.
b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table II, with the exception that particle impact noise detection test is not required.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table III, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table IV, with the exception that particle impact noise detection test is not required.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

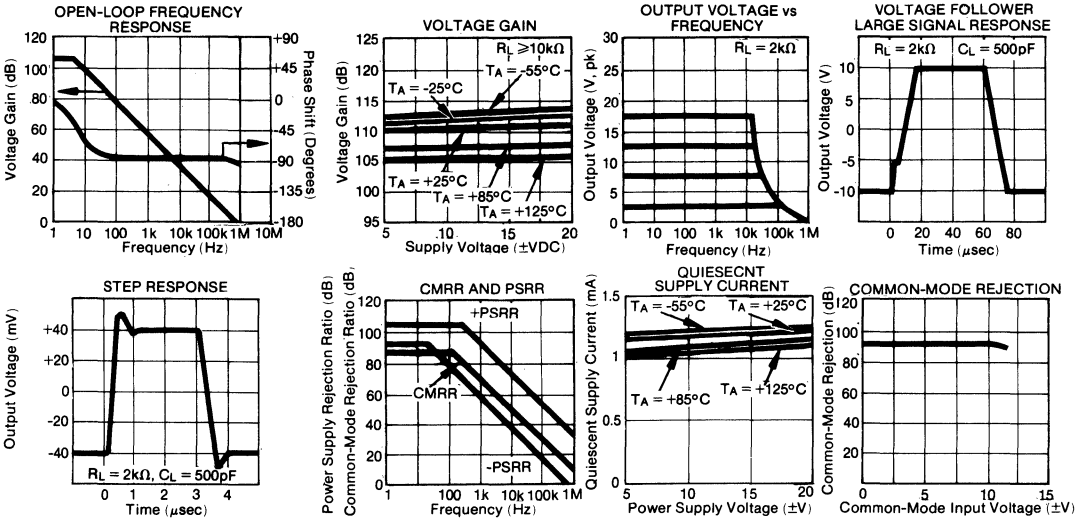
a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These mircocircuits are assigned to Technology Group F as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. ELECTRICAL PERFORMANCE CURVES.

(Typical at $T_A = +25°C$ and $\pm V_{CC} = 15VDC$ unless otherwise specified).



8. APPLICATION INFORMATION

8.1 Offset Voltage Adjustment. Although the OPA105/MIL Series has a low intital offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C for every 100μV of offset adjustment.

8.2 Guarding and Shielding. The ultra-low bias current and high input impedance of the OPA105/MIL Series are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA105/MIL Series.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the amplifier's bias current of the OPA105/MIL Series. To avoid leakage problems, it is recommended that the signal input lead of the OPA105/MIL Series be wired to a Teflon standoff. If the OPA105/MIL Series is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low input impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard. The resistor R_3 shown in Figure 5 is optional. It may be used to compensate effects of very large source resistances. However note that its use would also increase the noise due to the thermal noise of R_3.

8.3 Thermal Response Time. Thermal response time is an important parameter in low drift operational amplifiers like the OPA105/MIL Series. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA105/MIL Series is 20 seconds.

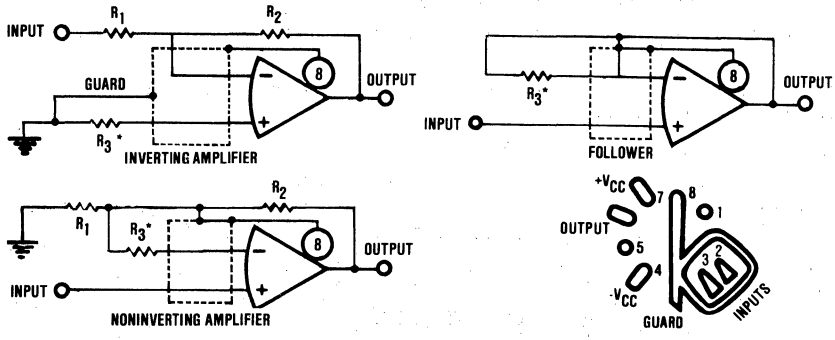


FIGURE 5. Connection of Input Guard.

BURR-BROWN®

OPA600/MIL SERIES

MODEL NUMBERS:

OPA600VM/MIL OPA600UM/883B
OPA600VM/883B OPA600UM
OPA600VM

REVISION NONE
FEBRUARY, 1982

Fast Settling - Wideband OPERATIONAL AMPLIFIER

FEATURES

- **FAST SETTLING**
  80nsec to ±0.1%
  115nsec to ±0.01%
- **FULL DIFFERENTIAL FET INPUT**
- **-55°C TO +125°C OPERATION**
- **LARGE OUTPUT**
  ±10V, ±200mA (50Ω)
- **GAIN-BANDWIDTH PRODUCT - 5GHz**

APPLICATIONS

- **VOLTAGE CONTROLLED OSCILLATOR DRIVER**
- **LARGE SIGNAL, WIDEBAND DRIVERS**
- **HIGH SPEED DAC OUTPUT AMPLIFIER**
- **VIDEO PULSE AMPLIFIER**

DESCRIPTION

The OPA600 is a wideband operational amplifier specifically designed for fast settling to ±0.01% accuracy. It is stable, easy to use, has good phase margin with minimum overshoot, and it has excellent DC performance. It utilizes a FET input stage to give low input bias current in contrast to the higher currents usually associated with very-fast amplifiers. Its DC stability with temperature is outstanding. Its -3dB bandwidth of 100MHz is available at a closed loop gain of 10. The slew rate exceeds 400V/μsec. All of this combines to form an outstanding amplifier for large and small signals.

Settling time is the best measure of this amplifier's total dynamic capability. High accuracy with fast settling is achieved by the large open-loop gain, which provides the accuracy at the upper frequencies. The thermally balanced design maintains this accuracy without droop or thermal tail. External compensation allows the user to optimize the settling time in his application.

The OPA600 is built to be reliable and is designed to operate from T_A = -55°C to +125°C. It is a hybrid microcircuit in a welded, hermetic, metal package and is available with MIL-STD-883 screening. The circuit is built on an alumina substrate which has a metallic attach to the package for good thermal transfer and reliable high temperature operation. The metal package provides electrostatic shielding. The circuit uses thin-film resistors and all glassivated, high speed silicon die. The gold or aluminum wirebonds utilized produce a monometallic system wherever possible, eliminating metal migration, a time-temperature reliability problem. The amplifier is actively laser-trimmed and is thoroughly tested. Reliability is emphasized during each phase of manufacture.

The OPA600 is useful in a broad range of video, high speed, and ECM applications. It is particularly well suited to operate as a voltage controlled oscillator (VCO) driver. It makes an excellent digital-to-analog converter output amplifier. It is a workhorse in test equipment where fast pulses, large signals, and 50Ω drive are important. It is a good choice for sample/holds, integrators, fast waveform generators, and multiplexers.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a hybrid, fast settling, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

OPA600	V	M	/MIL
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, operational amplifier. Two electrical performance grades are provided, the U grade and the V grade. The V grade offers the higher performance. Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel product designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter. Additional electrical testing is performed on /MIL models.
/883B	Standard Model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline (16-lead can) is as defined in Figure 6. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±17VDC
Input voltage range	±17VDC 1/
Differential input voltage range	±25VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	A few seconds 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±9VDC to ±16VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A
16-lead can	Figure 4	2.6W at T_{CASE} = +125°C	See Applications Information	35°C/W

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Duration is limited by device heat sinking (thermal resistance). Short circuit may be to ground only.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510, except that organic and polymeric materials (epoxy) are used for attach of some of the die. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

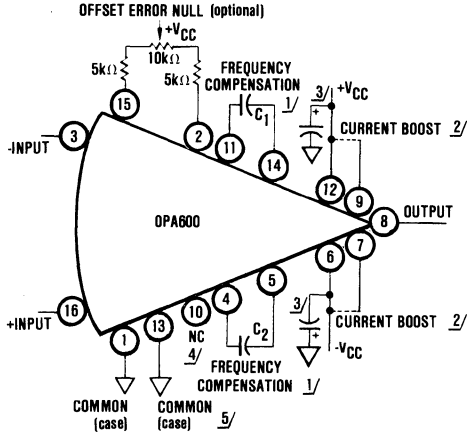
3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

3.2.8 Glassivation. All dice utilized are glassivated.



1/ Refer to Figure 4 for recommended frequency compensation.
2/ Connect pin 9 to pin 12 and connect pin 7 to pin 6 for maximum output current. See Application Information for further information.
3/ Bypass each power supply lead as close as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended.
4/ There is no internal connection. An external connection may be made.
5/ It is recommended that the amplifier be mounted with the case in contact with a ground plane for good thermal transfer and optimum AC performance.

FIGURE 1. Circuit Diagram and Terminal Connections.

3.2.9 Schematic Circuit. The schematic circuit is shown in Figure 2.

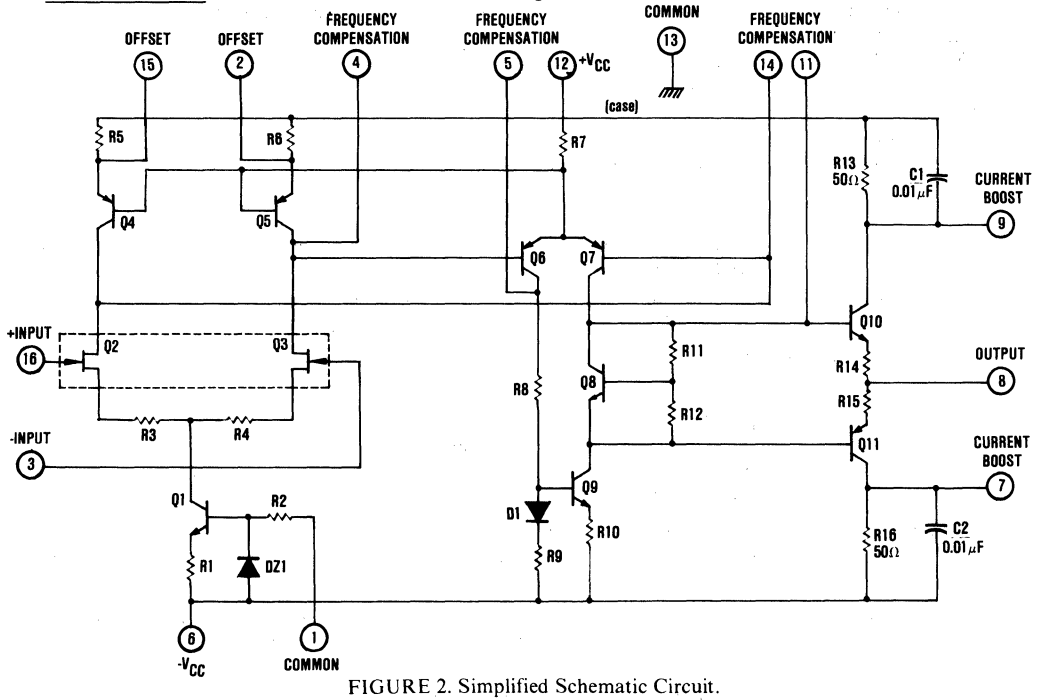


FIGURE 2. Simplified Schematic Circuit.

3.3 Electrical Performance Characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Additional Electrical Performance Characteristics. Electrical performance characteristic curves are shown in paragraph 7.

3.3.2 Offset error null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 3. If nulling is unnecessary for the application, delete the three components and make no connections.

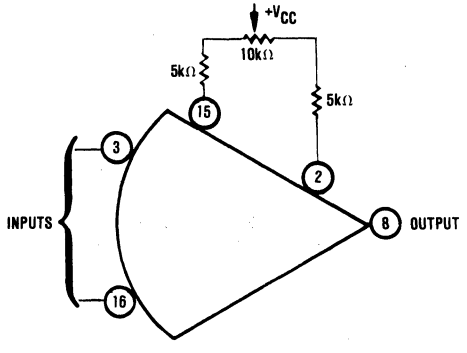


FIGURE 3. Offset Null Circuit.

3.3.3 Frequency compensation. The amplifier must be externally frequency compensated. See Figure 4.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Index point
b. Part number (see paragraph 1.2)
c. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin (USA)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding, for the /MIL Hi-Rel product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for /MIL Hi-Rel product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

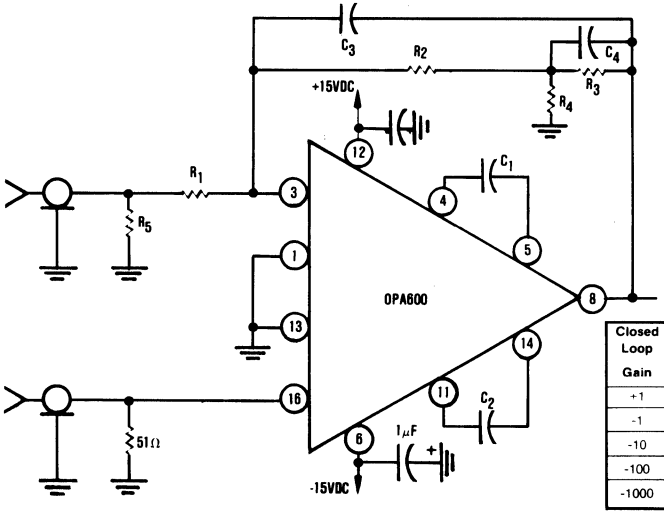
3.9 Screening. Screening for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

Screenin for the standard model, includes Burr-Brown QC4118 internal visual inspection, stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), constant acceleration (condition B), and external visual inspection per MIL-STD-883, method 5008, hybrid class.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for /MIL Hi-Rel product designation, is in accordance with MIL-M-38510, expect as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.



Closed Loop Gain	R_1	R_2	R_3	R_4	C_1, C_2	C_3	C_4	R_5
+1	open	100	short	open	6.8	0	0	--
-1	620	620	short	open	3.3	4.7	0	56
-10	100	1k	short	open	1	2.2	0	100
-100	100	3.3k	3.3k	3.2k	0	1	0	100
-1000	100	3.3k	3.3k	116	0	0	4.7	100

Note: Resistance is in ohms, capacitance is in pF, gain is volts/volt.

FIGURE 4. Recommended Amplifier Circuits and Frequency Compensation.

1/ a 4-digit date code, indicating year and week of seal, is marked on /883B and (none) Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics

All characters from -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise noted.

			OPA600VM/MIL** OPA600VM/883B OPA600VM			OPA600UM/883B OPA600UM			
CHARACTERISTICS	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OUTPUT									
Voltage (V_O)	R_L = 2kΩ		±10	±11		•	•		V
	R_L = 50Ω 1/		±9	±10		•	•		V
Current (I_O)	R_L = 50Ω 1/		±180	±200		•	•		mA
Current, pulse (I_{OP})	R_L = 50Ω 2/		±180	±200		•	•		mA
Resistance (R_O)	Open-loop, DC			75	150		•	•	Ω
Short Circuit Current (I_{SS})	To ground only t_{MAX} = 1sec 3/			250	300		•	•	mA
DYNAMIC RESPONSE									
Settling Time, ±0.01% 4/ (T_S)	ΔVO = 10V	T_A = 25°C		115	125		125	150	nsec
		T_A = -25°C to +85°C					135	165	nsec
		T_A = -55°C to +125°C		125	140			175	nsec
±0.1%	ΔVO = 20V	T_A = +25°C		105	130		•	•	nsec
	ΔVO = 10V	T_A = +25°C		80	105		•	•	nsec
±1%	ΔVO = 20V	T_A = +25°C		80	105		•	•	nsec
	ΔVO = 5V	T_A = +25°C		55	75		•	•	nsec
Post Settling Time Stability (T_S+) 5/	±0.01%	t = 1μsec to 500msec		0.5	1		•	•	mV
Gain-Bandwidth Product (open-loop) (GBP)	C_C = 0pF, G = 1 V/V	T_A = +25°C		150			•		MHz
	C_C = 0pF, G = 10V/V	T_A = +25°C		500			•		MHz
	C_C = 0pF, G = 100V/V	T_A = +25°C		1.5			•		GHz
	C_C = 0pF, G = 1000V/V	T_A = +25°C		5			•		GHz
	C_C = 0pF, G = 10,000V/V	T_A = +25°C		10			•		GHz
Bandwidth (BW) -3dB, small signal 6/	G = +1V/V	T_A = +25°C	100	125		•	•		MHz
	G = -1V/V	T_A = +25°C	75	90		•	•		MHz
	G = -1V/V	T_A = -55°C to +125°C	70	90	135	•	•		MHz
	G = -10V/V	T_A = +25°C	80	95		•	•		MHz
	G = -10V/V	T_A = -55°C to +125°C	70	95	135	•	•	•	MHz
	G = -100V/V	T_A = +25°C	15	20		•	•		MHz
	G = -1000V/V	T_A = +25°C	5	6		•	•		MHz
Full Power Bandwidth (BW_{FP})	V_O = ±5V, G = -1V/V, C_C = 3.3pF, R_L = 100Ω	T_A = +25°C		13	16		•	•	MHz
Slew Rate (SR)	V_O = ±5V, G = 1000V/V, C_C = 0pF, R_L = 100Ω	T_A = +25°C		500			•		V/μsec
	V_O = ±5V, G = -1V/V, C_C = 3.3pF, R_L = 100Ω	T_A = +25°C	400	440		•	•		V/μsec
		T_A = -55°C to +125°C	350			•			V/μsec
Phase Margin	G = -1V/V, C_C = 3.3pF	T_A = +25°C		40			•		Degrees
GAIN									
Open-Loop Voltage Gain (A_{OL})	f = D.C., R_L = 2kΩ	T_A = +25°C	86	94		•	•		dB
		T_A = -55°C to +125°C	74			•			dB
INPUT									
Offset Voltage (V_{IO}) 7/		T_A = +25°C		1	2		2	5	mV
		T_A = -25°C to +85°C						10	mV
		T_A = -55°C to +125°C			4			15	mV
Offset Voltage vs Temperature (V_{IO} vs T)		T_A = -25°C to +25°C					50	80	μV/°C
		T_A +25°C to +85°C					25	80	μV/°C
		T_A = -55°C to +25°C		10	20			100	μV/°C
		T_A = +25°C to +125°C		10	20			100	μV/°C
Bias Current (I_B)		T_A = +25°C	0	-20	-100	•	•	•	pA
		T_A = +25°C to +125°C	0	-20	-100	•	•	•	nA
Offset Current (I_{OS})		T_A = +25°C		20	50		•	•	pA
		T_A = -55°C to +125°C		20	50		•	•	nA

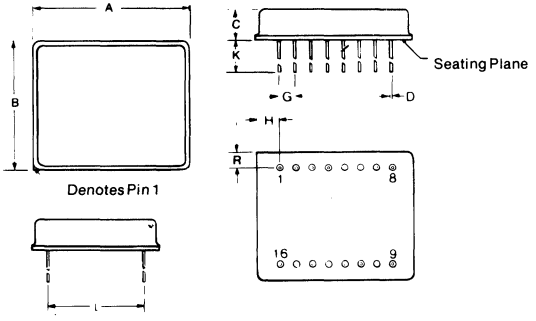
TABLE I. Electrical Performance Characteristics (cont)

All characteristics from -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise noted.

		OPA600VM/MIL** OPA600VM/883B OPA600VM			OPA600UM/883B OPA600UM			
CHARACTERISTICS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply Rejection (PSR)	V_{CC} = ±15V, ±1V T_A = +25°C		200	500		*	*	µV/V
Common-Mode Voltage Range (CMV)	T_A = +25°C	-10		+7	*		*	V
Common-Mode Rejection (CMR)	V_{CM} = -5V to +5V T_A = +25°C	60	80		*	*		dB
Impedance (Z_{IN})	Differential T_A = +25°C		10^{11} || 2			*		Ω || pF
	Common-mode T_A = +25°C		10^{11} || 2			*		Ω || pF
Voltage Noise (e_n)	f = 10kHz T_A = +25°C		20			*		nV/$\sqrt{Hz}$
POWER SUPPLY								
Rated			±15			*		VDC
Operating Range		±9		±16	*		*	VDC
Quiescent Current			±30	±38		*	*	mA
TEMPERATURE RANGE (ambient)								
Operating		-55		+125	-55		+125	°C
Storage		-65		+150	-65		+150	°C
θ_{JC} (junction to case)	See applications information							
θ_{CA} (case to ambient)			35			*		°C/W

*Specifications the same as V grade. **OPA600VM/MIL available in 2nd quarter 1982.

NOTES:
1/ Pin 9 connected to +V_{CC}, pin 7 connected to -V_{CC}. Observe power dissipation ratings.
2/ Pin 9 and pin 7 open. Single pulse t = 100nsec. Observe power dissipation ratings.
3/ Pin 9 and pin 7 open. See paragraph 8.8.
4/ G = -1V/V, C_C = 3.3pF, R_L = 100Ω. Optimum settling time may be achieved by individually compensating each device. Refer to paragraph 8.3.
5/ Post settling time stability is a measure of the pulse droop, or thermal tail, after the output has settled.
6/ Compensation per paragraph 8.3.
7/ Adjustable to zero.



NOTES:
1. Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.
2. Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.968	.972	24.59	24.69
B	.793	.797	20.14	20.24
C	.201	.211	5.11	5.36
D	.016	.020	0.41	0.51
G	.100 BASIC		2.54 BASIC	
H	.130	.140	3.30	3.56
K	.230	.270	5.84	6.86
L	.600 BASIC		15.24 BASIC	
R	.093	.102	2.36	2.60

FIGURE 5. Case Outline.

TABLE II. Electrical Test Requirements.
(The individual tests within the subgroups appear in Table III)

MODELS / MIL-STD-883 TEST REQUIREMENT (hybrid class)	OPA600VM/MIL	OPA600VM/883B OPA600VM	OPA600UM/883B OPA600UM
	Subgroups (see Table III)		
Interim electrical parameters (pre burn-in) (method 5008)	1	1	1
Final electrical test parameters (method 5008)	1*, 2, 3, 4, 7, 9, 10, 11	1, 2, 3, 4, 7, 9	1, 2, 2U, 3, 3U, 4, 7, 9
Group A test requirements (method 5008)	1, 2, 3, 4, 7, 9, 10, 11	--	--
Group C end point electrical parameters (method 5008)	Table IV limits and delta limits	--	--
Additional electrical subgroups performed prior to Group C inspections	None	--	--

*PDA applies to subgroup 1 (see 4.3.d)

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC}$ = 15V, unless otherwise specified	LIMITS OPA600VM/MIL OPA600VM/883B OPA600VM MIN	LIMITS OPA600VM/MIL OPA600VM/883B OPA600VM MAX	LIMITS OPA600UM/883B OPA600UM MIN	LIMITS OPA600UM/883B OPA600UM MAX	UNITS
1	V_{IO}	4001	V_{CM} = 0	-2	+2	-5	+5	mV
T_A = +25°C	I_{IB}	4001	V_{CM} = 0	0	-100	0	-100	pA
	+PSRR	4003	+V_{CC} = 15V, ±1V, -V_{CC} = 15V	-500	+500	-500	+500	µV/V
	-PSRR	4003	+V_{CC} = 15V, -V_{CC} = 15V, ±1V	-500	+500	-500	+500	µV/V
	CMR	4003	V_{CM} = -5V to +5V	60		60		dB
	I_O	4005			38		38	mA
2	V_{IO}	4001			+4	-15	+15V	mV
T_A = +125°C	$\frac{\Delta V_{IO}}{\Delta T}$	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (+125°C)}{100°C}$	-20	+20	-100	+100	µV/°C
2U	V_{IO}	4001				-10	+10	mV
T_A = +85°C	$\frac{\Delta V_{IO}}{\Delta T}$	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (+85°C)}{60°C}$			-80	+80	µV/°C
3	V_{IO}	4001		-4	+4	-13	+13	mV
T_A = -55°C	$\frac{\Delta V_{IO}}{\Delta T}$	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (-55°C)}{80°C}$	-20	+20	-100	+100	µV/°C
3U	V_{IO}	4001	$\frac{V_{IO}\ (+25°C) - V_{IO}\ (-25°C)}{50°C}$			-9	+9	mV
T_A = -25°C	$\frac{}{\Delta T}$					-80	+80	µV/°C
4	V_O	4004	R_L = 2kΩ	±10		±10		V
T_A = +25°C	I_O	4004	R_L = 50Ω, pin 9 to +V_{CC}, pin 7 to -V_{CC}	±180		±180		mA
	Avs	4004	R_L = 2kΩ, f = 0Hz, V_O = ±10V	86		86		dB
7	V_O	4004	R_L = 2kΩ, ±V_{CC} = 16VDC	±11		±11		V
T_A = +25°C	V_O	4004	R_L = 2kΩ, ±V_{CC} = 12VDC	±7		±7		V
9	ts	4002	To ±0.01%, Figure 10 final value at t = 1µsec		125		150	nsec
T_A = +25°C	SR	4002	G = -1, V_O = ±5V, Figure 10 10% to 90%	400		400		V/µsec
	T_{S+}		t = 1µsec to 500msec (ts to ±0.01%, ΔVo = 10V)		1			mV
10	ts 1/	4002	To ±0.01%, Figure 10		140			nsec
T_A = +125°C								
11	ts 1/	4002	To ±0.01%, Figure 10		140			nsec
T_A = -55°C								

NOTE:

1/ This test required for /MIL suffix only. Sample test per MIL-STD-105 level II, 4.0% AQL, normal inspection.

TABLE IV. Group C, End Point Electrical Parameters.

(T_A = +25°C, ±V_{CC} = 15VDC)

TEST	LIMIT	DELTA
Input Offset Voltage	2mV	1mV
Open-Loop Voltage Gain	86dB	6dB
Settling Time (to 0.01%, ΔVo = 20V, G = -1)	125nsec	25nsec

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specified by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for / MIL and / 883 Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 6 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for /MIL Hi-Rel product designation only, is 10 percent and includes both parametric and catastropic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

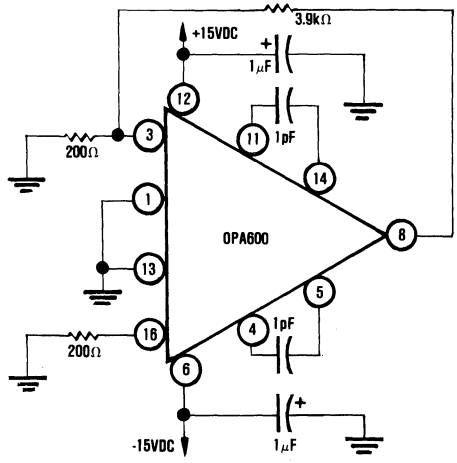


FIGURE 6. Test Circuit Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Group D, subgroup 1, seal test, of MIL-STD-883, method 5008, is performed on each lot of packages procured. Groups C and D inspections (except for subgroup 1, seal test) of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table I, and as follows:
   a. Tests are specified in Table II herein.
   b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table II and as follows:
   a. Particle impact noise detection test is not required.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table III, and as follows:
   a. Operating life test (MIL-STD-883, method 1005) conditions:
      (1) Test condition B
      (2) Test circuit is Figure 6 herein
      (3) $T_A = 125°C$ minimum
      (4) Test duration is 1000 hours minimum
   b. End point electrical parameters are specified in Table II herein.
   c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table IV, and as follows:

a. Particle impact noise detection test is not required.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2)

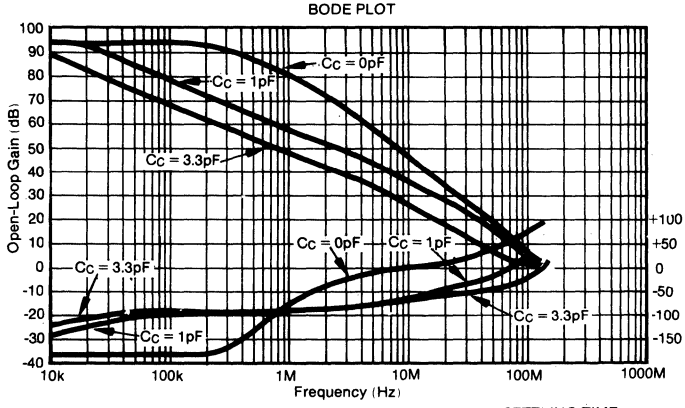
b. Requirement for certificate of compliance, if desired.

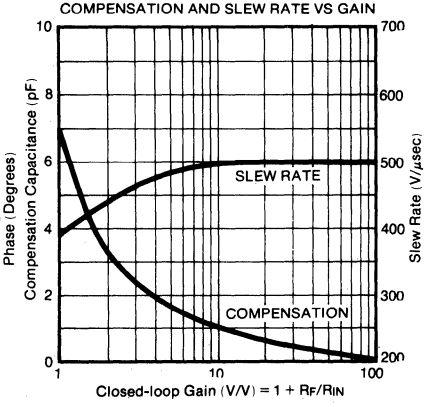
6.4 Microcircuit group assignment. These mircocircuits are assigned to Technology Group F as defined in MIL-M-38510, Appendix E.

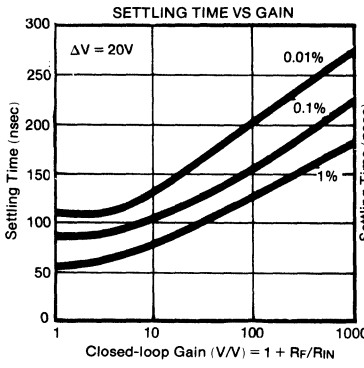
6.5 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

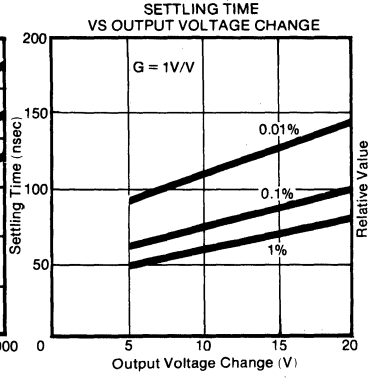
7. ELECTRICAL PERFORMANCE CURVES

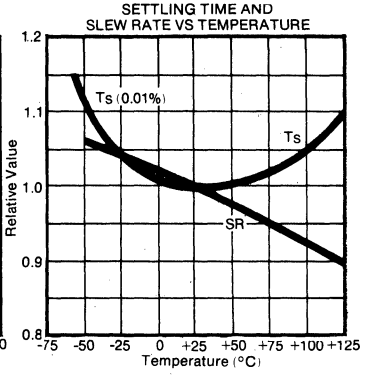
(Typical at T_A = +25°C and ±V_{CC} = 15VDC, unless otherwise specified).

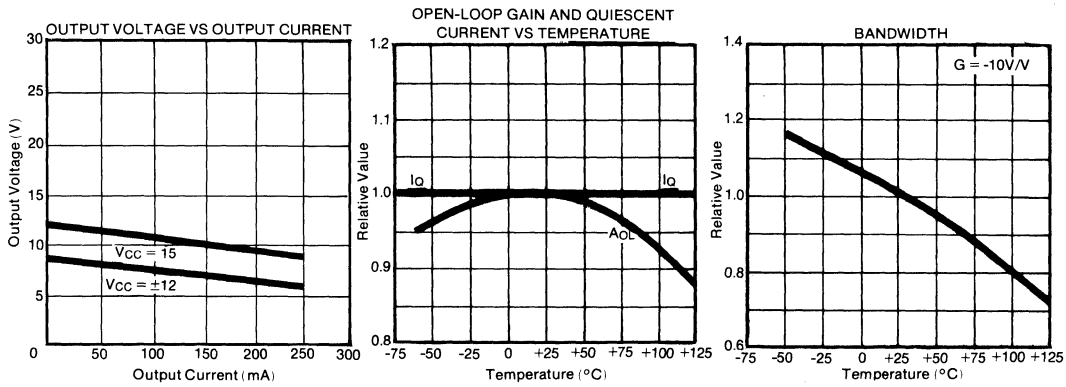












8. APPLICATIONS INFORMATION

8.1 Wiring precautions. The OPA600 is a wideband, high frequency operational amplifier with a gain-bandwidth product exceeding 5GHz. This capability can be realized by observing a few wiring precautions and using high frequency layout techniques. Of all the wiring precautions, grounding is the most important and is described in detail in the next section.

In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths and should be as short as possible. The entire physical circuit should be as small as is practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the input terminals of the amplifier and compensation pins. Stray signal coupling from the output to the input should be minimized. All circuit element leads should be as short as possible and low values of resistance should be used. This will give the best circuit performance as it will minimize the time constants formed with the circuit capacitances and will eliminate stray, unwanted tuned circuits.

8.2 Grounding. Grounding is the most important applications consideration for the OPA600, as it is with all high frequency circuits. Ultra-high frequency transistors are used in the design of the OPA600 and oscillations at frequencies of 500MHz and above can be stimulated if good grounding techniques are not used. A ground plane is highly recommended. It should connect all areas of the pattern side of the printed circuit that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pickup. It eliminates parasitic circuits from what would otherwise be long, component leads.

Point-to-point wiring is not recommended. However, if point-to-point wiring is used, a single-point ground should be used. The input signal return, the load signal return and the power supply common should all be connected at the same physical point. This eliminates common current paths or ground loops which can cause unwanted feedback.

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A 1μF CS13 tantalum capacitor is recommended. A parallel 0.01μF ceramic may be added if desired. This is especially important when driving high current loads. Properly bypassed and modulation free power supply lines allow full amplifier output and optimum settling time performance.

OPA600 circuit common is connected to pins 1 and 13; these pins should be connected to the ground plane. The input signal return, load return, and power supply common should also be connected to the ground plane.

The case of the OPA600 is internally connected to circuit common, and as indicated above, pins 1 and 13 should be connected to the ground plane. Ideally, the case should be mechanically connected to the ground plane for good thermal transfer but because this is difficult in practice, the OPA600 should be fully inserted into the printed circuit board with the case very close to the ground plane to make the best possible thermal connection. If the case and ground plane are physically connected or are in close thermal proximity, the ground plane will provide heat sinking which will reduce the case temperature rise. The minimum OPA600 pin length will minimize lead inductance, thereby maximizing performance.

To repeat, proper grounding is the single most important aspect of high frequency circuitry.

8.3 Compensation. The OPA600 uses external frequency compensation so that the user may optimize the bandwidth or settling time for his particular application. Several performance curves aid in the selection of the correct compensations capacitance value. The Bode plot shows amplitude and phase versus frequency for several values of compensation. A

related curve shows the recommended compensation capacitance versus closed-loop gain.

Figure 4 shows a recommended circuit schematic. Component values and compensation for amplifiers with several different closed-loop gains are shown. This circuit will yield the specified settling time. Because each device is unique and slightly different, as is each user's circuit, optimum settling time will be achieved by individually compensating each device in its own circuit, if desired. A 10% to 20% improvement in settling time has been experienced from the values indicated in Table I.

The primary compensation capacitors are C_1 and C_2 (see Figure 4). They are connected between pins 4 and 5 and between pins 11 and 14. Both C_1 and C_2 should be the same value. As Figure 4 and the performance curves show, larger closed-loop configurations require less capacitance and improved gain-bandwidth product can be realized. Note that no compensation capacitor is required for closed-loop gains equal to or above 100V/V. If upon initial application the user's circuit is unstable, and remains so after checking for proper bypassing, grounding, etc., it may be necessary to increase the compensation slightly to eliminate oscillations. Do not over compensate. It should not be necessary to increase C_1 and C_2 beyond 10pF to 15pF.

The flat high frequency response of the OPA600 is preserved and high frequency peaking is minimized by connecting a small capacitor in parallel with the feedback resistor (see Figure 4). This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resistances. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator is recommended to avoid using a large value resistor with its long time constant.

For heavy capacitive loads, greater than 50pF, refer to the section on capacitive loads, paragraph 8.6. For particularly difficult applications where the wiring layout may not be the best or where there may be 1000pF loads, parasitics, strays, long lead lengths, changing capacitive loads, etc., doublet compensation is recommended. This is discussed in paragraph 8.12 and is shown in Figure 9. This circuit offers increased stability at the expense of increasing the settling time by approximately 50%. Also, this circuit is especially useful for functional testing at low frequency and incoming inspection.

8.4 Settling time. Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

Settling time is a complete dynamic measure of the OPA600's total performance. It includes the slew rate time, a large signal dynamic parameter, and the time to accurately reach the final value, a small signal parameter that is a function of bandwidth and open-loop gain. Performance curves show the OPA600 settling time to ±1%, ±0.1%, and ±0.01%. The best settling time is achieved in low closed-loop gain circuits.

Settling time is dependent upon compensation. Under-compensation will result in small phase margin, overshoot or instability. Over-compensation will result in poor settling time. Refer to paragraph 8.3.

Figure 4 shows the recommended compensation to yield the specified settling tine. Improved or optimum settling time may be achieved by individually compensating each device in the user's circuit since individual devices vary slightly from one to another as do user's circuits.

8.5 Slew rate. Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or the small signal bandwidth. Slew rate is dependent upon compensation and decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve.

8.6 Capacitive loads. The OPA600 will drive large capacitive loads (up to 100pF) when properly compensated and settling times of under 150nsec are achievable. The effect of a capacitive load is to decrease the phase margin of the amplifier which may cause high frequency peaking or oscillations. A solution is to increase the compensation capacitance, somewhat slowing the amplifier's ability to respond. The recommended compensation capacitance value as a function of load capacitance is shown in Figure 7. (Use two capacitors, each with the value indicated.) Alternately, without increasing the OPA600's compensation capacitance, the capacitive load may be buffered by connecting a small resistance, usually 5Ω to 50Ω, in series with the Output, pin 8.

For very-large capacitive loads, greater than 100pF, it will be necessary to use doublet compensation. Refer to Figure 9 and paragraph 8.12. This places the dominant pole at the input stage. Settling time will be approximately 50% slower; slew rate should increase. Load capacitance should be minimized for optimum high frequency performance.

Because of its large output capability, the OPA600 is particularly well suited for driving loads via coaxial cables. Note that the capacitance of coaxial cable (29pF/foot of length for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

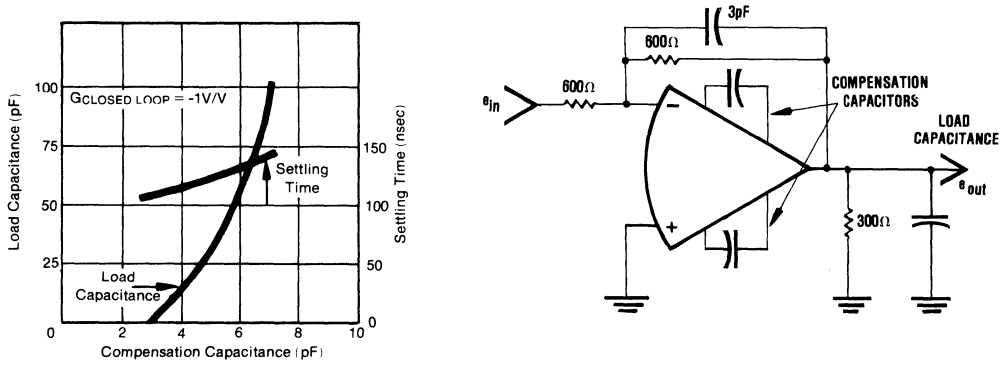


FIGURE 7. Capacitive Load Compensation and Response.

8.7 Offset voltage adjustment. The offset voltage of the OPA600 may be adjusted to zero by connecting a 5kΩ resistor in series with a 10kΩ linear potentiometer in series with another 5kΩ resistor between pins 2 and 15, as shown in Figure 3. It is important that one end of each of the two resistors be located very close to pins 2 and 15 to isolate and avoid loading these sensitive terminals. The potentiometer should be a small, noninductive type with the wiper connected to the positive supply. The leads connecting these components should be short, no longer than 0.5-inch, to avoid stray capacitance and stray signal pick-up. If the potentiometer must be located away from the immediate vicinity of the OPA600, extreme care must be observed with the sensitive leads. Locate the two 5kΩ resistors very close to pins 2 and 15.

Never connect $+V_{CC}$ directly to pin 2 or 15. Do not attempt to eliminate the 5kΩ resistors because at extreme rotation, the potentiometer will directly connect $+V_{CC}$ to pin 2 or pin 15 and permanent damage will result.

Offset voltage adjustment is optional. The potentiometer and two resistors are omitted when the offset voltage is considered sufficiently low for the particular application. For each microvolt of offset voltage adjusted, the offset voltage temperature sensitivity will change by $\pm 0.004 \mu V/^{\circ}C$.

8.8 Current boost. External ability to bypass the internal current limiting resistors has been provided in the OPA600. This is referred to as current boost. Current boost enables the OPA600 to deliver large currents into heavy loads (±200mA at ±10V). To bypass the resistors and activate the current boost, connect pin 7 to $-V_{CC}$ at pin 6 with a short lead to minimize lead inductance and connect pin 9 to $+V_{CC}$ at pin 12 with a short lead.

CAUTION - Activating current boost by bypassing the internal current limiting resistors can permanently damage the OPA600 under fault conditions. See paragraph 8.9.

Not activating current boost is especially useful for initial breadboarding. The 50Ω (±5%) current limiting resistor in the collector circuit of each of the output transistors causes the output transistors to saturate; this limits the power dissipation in the output stage in case of a fault. Operating with the current boost not activated may also be desirable with small-signal outputs (i.e.±1V) or when the load current is small.

Each resistor is internally capacitively-bypassed (0.01μF, ±20%) to allow the amplifier to deliver large pulses of current, such as to charge diode junctions or circuit capacitances and still respond quickly. The length of time that the OPA600 can deliver these current pulses is limited by the RC time constant.

The internal voltage drops, output voltage available, power dissipation, and maximum output current can be determined for the user's application by knowing the load resistance and computing:

$$V_{OUT} = 14 \left(\frac{R_{LOAD}}{50 + R_{LOAD}} \right)$$

This applies for R_{LOAD} less than 100Ω and the current boost not activated. When R_{LOAD} is large, the peak output voltage is typically ±11V, which is determined by other factors within the OPA600.

8.9 Short circuit protection. The OPA600 is a short-circuit-protected for momentary short to common (<5sec), typical of those encountered when probing a circuit during experimental breadboarding or troubleshooting. This is true only if pins 7 and 9 are open (current boost not activated). An internal 50Ω resistor is in series with the collector of each of the output transistors which under fault conditions will cause the output transistors to saturate and limit the power dissipation in the output stage. Extended application of an output short can damage the amplifier due to excessive power dissipation.

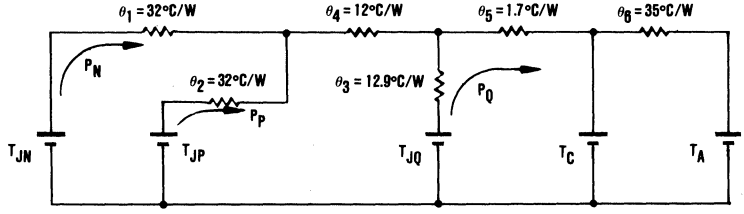
The OPA600 is not short-circuit-protected when the current boost is activated. The large output current capability of the OPA600 will cause excessive power dissipation and permanent damage will result even for momentary shorts to ground.

Output shorts to either supply will generally destroy the OPA600 whether the current boost is activated or not.

8.10 Heat sinking and power dissipation. The OPA600 is intended as a printed circuit board mounted device and as such, does not require a heat sink. It is specified for ambient temperature operation from -55°C to +125°C. However, the power dissipation must be kept within safe limits. At extreme temperature and under full load conditions, some form of heat sinking will be necessary. The use of a heat sink, or other heat dissipating means such as proximity to the ground plane will result in cooler operating temperatures, better temperature performance, and improved reliability.

The thermal model used to describe the OPA600 is more complete than is usual for operational amplifiers. The thermal resistances for the output stages have been separated from the thermal resistrance for the balance of the OPA600. For most monolithic op amps and hybrids, thermal properties are usually represented by one thermal resistance, θJC; and in general, that is fairly accurate because the total power dissipation is low and the heat that is generated is in one area. For packaged power transistors, thermal properties are also accurately represented by one thermal resistance, θJC; all the power is dissipated in one point source. The OPA600 op amp however, has a large power handling capability and large power dissipations occur in different locations within the amplifier under differing load conditions.

The total power dissipation within the OPA600 is the sum of all the individual sources of dissipation. By making some simplifying assumptions and neglecting second order effects, the dissipations are grouped into three sources - quiescent power, NPN output transistor power, and PNP output transistor power. Using the thermal model shown in Figure 8 and the absolute maximum junction temperature rating (derate the maximum, if desired) and solving the Thevenin equivalent simultaneous equations that result, the user can determine junction, internal substrate, and case temperatures. It will be apparent that the output stages contribute significantly to the thermal rise. Under light loading, the requirements to dissipate the generated heat are much less than the requirements to dissipate heat under full load conditions at a maximum temperature. Using this expanded thermal information allows the user to safely apply the OPA600.



T_{JN} = Junction temperature of NPN output transistor.
T_{JP} = Junction temperature of PNP output transistor.
T_{JQ} = Worst case temperature of any device in the balance of the amplifier.
T_C = Case temperature.
T_A = Ambient temperature.
θ_1, θ_2 = Thermal resistance, output transistors.
θ_3, θ_4 = Thermal resistance, substrate.
θ_5 = Thermal resistance, substrate attach and package.
θ_6 = Thermal resistance, case to ambient.
P_N = Worst case power dissipation in the NPN output transistor.
P_P = Worst case power dissipation in the PNP output transistor.
P_Q = Quiescent power dissipation.

FIGURE 8. OPA600 Thermal Model.

Below are two examples of using the thermal model.

1. Find the worst case internal junction temperature rise above ambient.

Conditions: $P_Q = 1$ W
$P_N = P_P = 0.1$ W
no heatsink

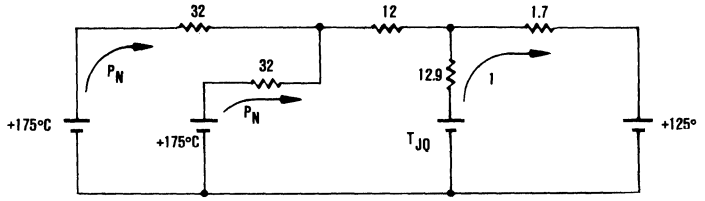
Solution: $T_{JN} = 80.7P_N + 48.7P_P + 36.7P_Q + T_A$
$T_{JN} - T_A = 49.6°C$
as $P_N = P_P$ $T_{JP} - T_A = 49.6°C$
$T_{JQ} = 49.6P_Q + 36.7P_N + 36.7P_P + T_A$
$T_{JQ} - T_A = 57°C$

Answer: 57°C

2. Find the maximum output stage power dissipation allowed with a maximum case temperature of +125°C and not exceeding the maximum junction temperature of +175°C.

Conditions: $P_Q = 1$ Watt
$P_N = P_P$

Solution:



$T_{JN} = P_N\ 32 + (P_N + P_P)12 + (P_N + P_P)\ 1.7 + P_Q\ 1.7 + T_C$
$175 = 59.4\ P_N + 1.7 + 125$
$P_N = 0.813W$

Checking T_{JQ}: $T_{JQ} = (1)\ 12.9 + (2x\ 0.813 + 1)\ 1.7 + 125$
$T_{JQ} = 142°C$ (i.e. $< 175°C$)

Answer: 0.813W may be dissipated in each output transistor.

It may be necessary to physically connect the OPA600 to the printed circuit board ground plane, attach fins, tabs, etc., to dissipate the generated heat. Because of the wide variety of possibilities, this task is left to the user. For all applications it is recommended that the OPA600 be fully inserted into the printed circuit board and that the pin length be short. Heat will be dissipated through the ground plane and the AC performance will be its best. See paragraphs 8.1 and 8.2

8.11 Testing. For static and low frequency dynamic measurements, the OPA600 may be tested in conventional operational amplifier test circuits, provided proper grounding techniques are observed, excessive lead lengths are avoided, and care is maintained to avoid parasitic oscillations. See the above sections, especially paragraphs 8.1 and 8.2. The circuit in Figure 9 is recommended for low frequency functional testing, incoming inspection, etc. This circuit is less susceptible to stray capacitance, excessive lead length, parasitic tuned circuits, changing capacitive loads, etc. It does not yield optimum settling time. We recommend placing a resistor (approximately 300Ω) in series with each piece of test equipment, such as a DVM, to isolate loading effects on the OPA600.

To realize the full performance capabilities of the OPA600, high frequency techniques must be employed and the test fixture must not limit the amplifier. Settling time is the most critical dynamic test and Figure 10 shows a recommended OPA600 settling time test circuit schematic. Good grounding, truly square drive signals, minimum stray coupling, and small physical size are important.

The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. A circuit that generates a ±5V flat topped pulse is shown in Figure 11.

Every OPA600 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

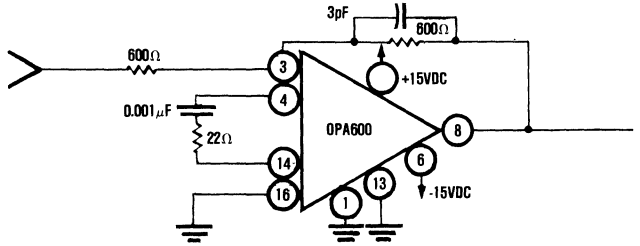


FIGURE 9. Amplifier Circuit for Increased Stability.

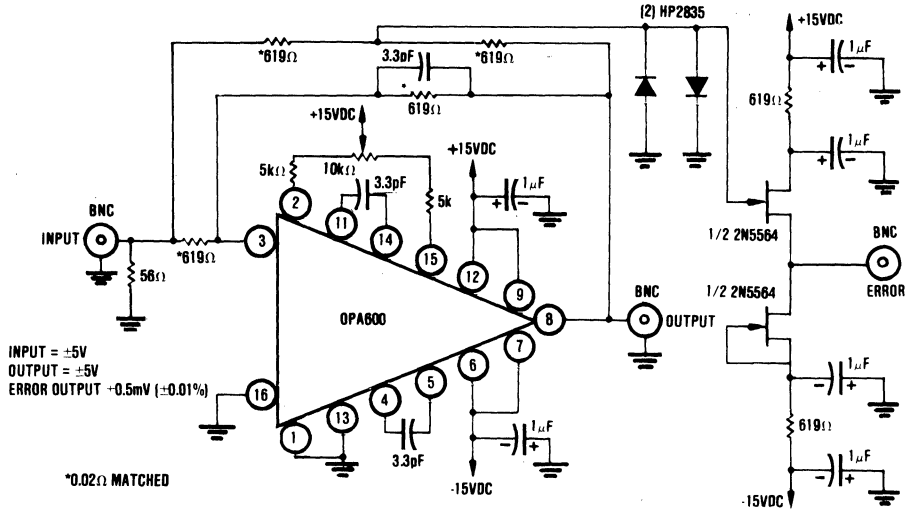


FIGURE 10. Settling Time and Slew Rate Test Circuit.

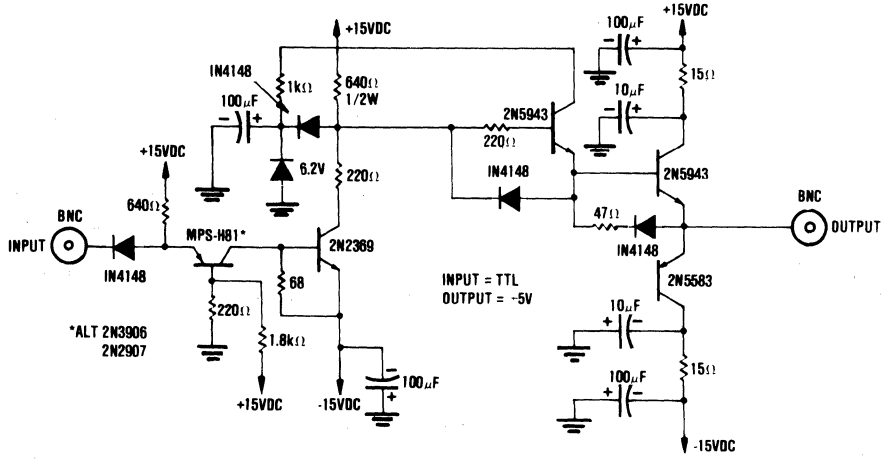


FIGURE 11. Flat Top Pulse Generator.

8.12 Increased Slew Rate. The OPA600 slew rate may be increased by using an alternate compensation shown in Figure 9. The slew rate will increase between 700 and 800V/μsec typical with 0.01% settling time increasing to between 175 and 190nsec typical and 0.1% settling time increasing to between 110 and 120nsec typical.

For alternate doublet compensation refer to Figure 9. For a closed-loop gain equal -1, delete C1 and C2 and add a series RC circuit (R = 22Ω, C = 0.001μF) between pins 14 and 4. Make no connections to pins 11 and 5. Absolutely minimize the capacitance to these pins. If a connector is used for the OPA600, it is recommended that sockets for pins 11 and 5 be removed. For a PC board mount, it is recommended that the PC board holes be overdrilled for pins 11 and 5 and adjacent ground plane copper be removed. Effectively this compensation places the dominant pole at the input stage, allowing the output stage to have no compensation and to slew as fast as possible. Bandwidth and settling time are impaired only slightly. For closed-loop gains other than -1, different values of R and C may be required.

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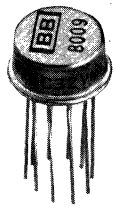

VFC32/MIL SERIES

MODEL NUMBERS:

VFC32WM/883B
VFC32WM
VFC32UM/883B
VFC32UM
VFC32VM/MIL
VFC32VM/883B
VFC32VM

REVISION NONE
OCTOBER, 1981

VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- **HIGH LINEARITY**
  - **±0.006% max (13 bits) and ±0.01% max (12 bits) at 10kHz FS**
  - **±0.05% max at 100kHz FS**
  - **±0.2% max at 0.5MHz FS**
- **HI-REL MANUFACTURE**
- **6-DECADE DYNAMIC RANGE**
- **OUTPUT DTL/TTL/CMOS COMPATIBLE**
- **V/F OR F/V CONVERSION**

DESCRIPTION

The VFC32 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple, low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

The converter requires two external resistors and two external capacitors to operate. One external resistor and one external capacitor set up the full scale frequency, with a guaranteed nonlinearity of ±0.2% maximum at 500kHz. The other capacitor is the one-shot capacitor; for best performance it should have a low temperature coefficient. The other resistor is a noncritical open collector pull-up resistor.

The VFC32/MIL Series converter is available in three electrical performance grades. The V grade has 200kHz specifications and tests. The W grade has premium linearity, ±0.006% of FSR, and premium full scale accuracy temperature coefficient of 100ppm/°C. The U grade is specified from -25°C to +85°C and from -55°C to +125°C. It is primarily for high performance test equipment, shipboard, ground support and industrial applications, where operation is normally between -25°C and +85°C and full temperature operation must be assured. All are packaged in welded, hermetically-sealed, TO-100 cans.

All devices are manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions to assure "built-in" quality.

Three product assurance levels are available: standard, /883B, and /MIL. The standard models have many MIL-STD-883 screens performed routinely. The /883 suffixed devices are 100% screened per MIL-STD-883 method 5004 class B and each /MIL suffixed device is Hi-Rel manufactured, 100% screened per MIL-STD-883 method 5004 class B, and has 10% PDA.

Quality assurance further processes /MIL devices, performing group A and B inspections on each inspection lot and group C and D inspections periodically and when specified on the customer's purchase order. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

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PDS-449

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
VOLTAGE-TO-FREQUENCY CONVERTER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a very linear, voltage-to-frequency converter. For the description of operation see paragraph 3.3.3.

1.2 Part Number. The complete part number is as shown below.

VFC32	V	M	MIL
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, voltage-to-frequency converter; it will also function as a single, frequency-to-voltage converter. Three electrical performance grades are provided. The V grade features specifications and tests at 200kHz. The W grade features premium linearity (13 bits) and premium full scale accuracy. The U grade features specified and tested performance from -25°C to +85°C and maintains -55°C to +125°C operation.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the product assurance level class B, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level as follows:

Hi-Rel Product Designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 class B screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
/883B	Standard model, plus 100% MIL-STD-883 class B screening.
(none)	Standard model including 100% electrical testing.

1.2.3. Case outline. The case outline is A-2 (10-lead can, TO-100) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±22VDC
Input voltage range, +input, pin 1	±22VDC 1/
Input voltage range, -input, pin 2	±22VDC 1/
Output pull-up supply voltage (V_{PU})	±22VDC 1/ 2/
Output sink current, pin 6	16mA
Comparator input voltage	±22VDC 1/
Output current pin 10	±20mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ V_{PU} is the supply voltage connected to pin 6 via R_2, see Figure 2.

1.2.5 Recommended operating conditions.

Supply voltage range	±11VDC to ±20VDC
Output pull-up supply (V_{PU})	+4.5VDC to +20VDC
Input voltage range, (V_{IN})	0VDC to +[0.00025 x (R_1 + R_3)]VDC 1/ 2/
	-10VDC to 0VDC 3/
Input current range, pin 2	0mA to +0.25mA
	0mA to +0.50mA 2/
Full scale frequency	100kHz 4/
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A	Maximum θ J-A
10-lead can (TO-100)	A-2	225mW at T_A = 125°C	70°C W	150°C W	220°C W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1. Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4. Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The microcircuit die is glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

3.2.9 Schematic circuit. The functional schematic circuit is shown in Figure 1.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown within paragraph 7.

3.3.2 Connection diagram. The connection diagrams for voltage-to-frequency operation are shown in Figures 2 and 3. The connection diagram for frequency-to-voltage operation is shown in Figure 4.

1/ For positive input voltages (see Figure 2).
2/ For frequencies 100kHz to 500kHz 50% duty cycle is recommended (see paragraph 3.3.3.1).
3/ For negative input voltages (see Figure 3).
4/ For best line linearity.

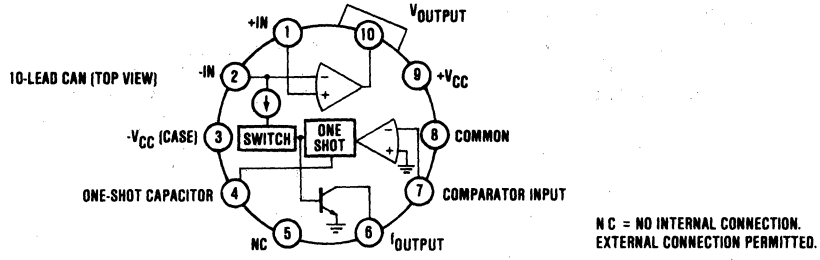


FIGURE 1. Terminal Connections and Functional Schematic Circuit.

3.3.3. Description of Operation. The input amplifier of the VFC is connected as an integrator (see Figure 2). When a positive input voltage is applied at V_{IN}, a constant current, $V_{IN}/(R_1 + R_3)$, will flow through the input resistor, $(R_1 + R_3)$, charging capacitor C_2. At this time the current sink is disabled as the switch is open and the VFC output, pin 6, is logic "0". The voltage at the amplifier output (comparator input) will ramp down from a positive voltage toward zero, according to $dv/dt = V_{IN}/[(R_1 + R_3)C_2]$. When the ramp reaches a voltage close to zero ($\approx$ -0.6V), the comparator changes state, and fires the one shot. Note, this period of time is a function of the input voltage, V_{IN}.

As the one-shot fires, the VFC output, pin 6, changes from logic "0" to logic "1", and the switch closes enabling the 1mA current sink. The length of time the one shot fires is determined by a reference (7.5V) within the one shot and the external one shot capacitor C_1. Note, this period of time is not a function of the input voltage. For good over temperature performance C_1 must have a low temperature coefficient. When the current sink is enabled, the current in the integrating capacitor, C_2, reverses direction and flows toward the summing junction. This occurs because the constant input current, $V_{IN}/(R_1 + R_3)$, is set up to always be less than the 1mA current sink. The voltage at the amplifier output ramps up according to $dv/dt = [(V_{IN}/(R_1 + R_3)) - (1mA)]/C_2$. Before the ramp voltage saturates the amplifier, the one shot resets.

When the one shot resets, the switch opens, the current sink is disabled, the VFC output changes back to logic "0" and the cycle repeats.

The total VFC period is determined by the following equations:

$$f_o = \frac{1}{t}$$

$$t = t_1 + t_2$$

$$t = \Delta V_{OUT}\, t_1 \frac{C_2}{V_{IN}/(R_1 + R_3)} + \Delta V_{OUT}\, t_2 \frac{C_2}{V_{IN}/(R_1 + R_3) - 1mA}$$

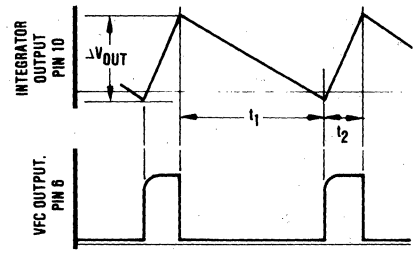
and:

$$-\Delta V_{OUT}\, t_1 = +\Delta V_{OUT}\, t_2$$

$$t_2 = C_1 \frac{7.5V}{1mA}$$

The equations reduce to:

$$f_o = \frac{V_{IN}}{7.5\,(R_1 + R_3)\,C_1}$$



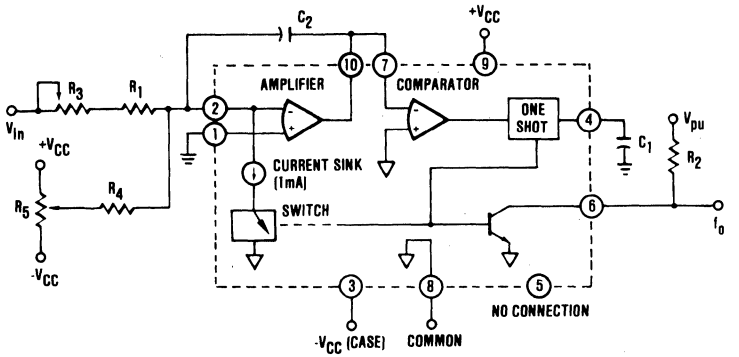
Note, the output frequency is not dependent upon C_2, and the temperature coefficients of R_1, R_3, and C_1 are critical to the VFC's over-temperature performance. These temperature coefficient effects must be added to the drift specifications of the integrated circuit itself.

3.3.3.1 Duty cycle. The duty cycle (D) of the VFC is the percent the one-shot period (t_2) is of the total VFC period ($t_1 + t_2$). It is measured at the full scale input voltage, which is the full scale frequency.

$$D = \frac{t_2}{t_1 + t_2}$$

Duty cycle is related to the maximum input current and the 1mA (nominal) current sink. By reducing the equations for t_2 and f_o:

$$D = \frac{V_{IN}\,max\,/\,(R_1 + R_3)}{1mA} = \frac{I_{IN}\,max}{1mA}$$



TRANSFER FUNCTION

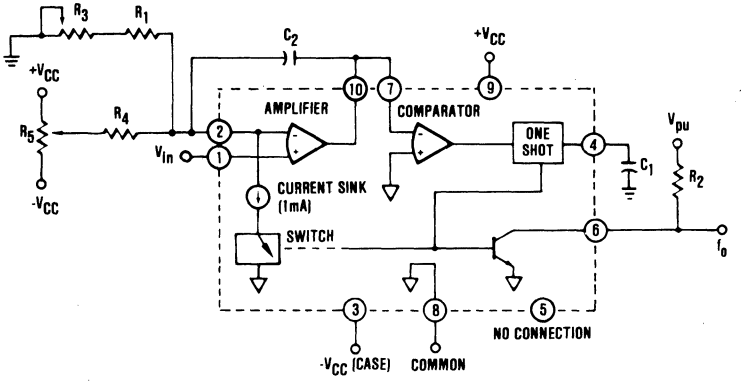
$$f_o = \frac{V_{IN}}{7.5\,(R_1 + R_3)\,C_1}$$

V_{cc} = ±15VDC
V_{pu} = 5VDC
V_{in} = 0VDC to +10VDC
f_o = ≈4Hz to 10kHz

EXTERNAL COMPONENTS

R_1 = 30kΩ R_5 = 50kΩ
R_2 = 1.2kΩ C_1 = 3300pF (D = 0.25)
R_3 = 20kΩ C_2 = 0.01μF
R_4 = 10MΩ

FIGURE 2. Connection Diagram, Voltage-to-Frequency Operation, Positive Input.



TRANSFER FUNCTION

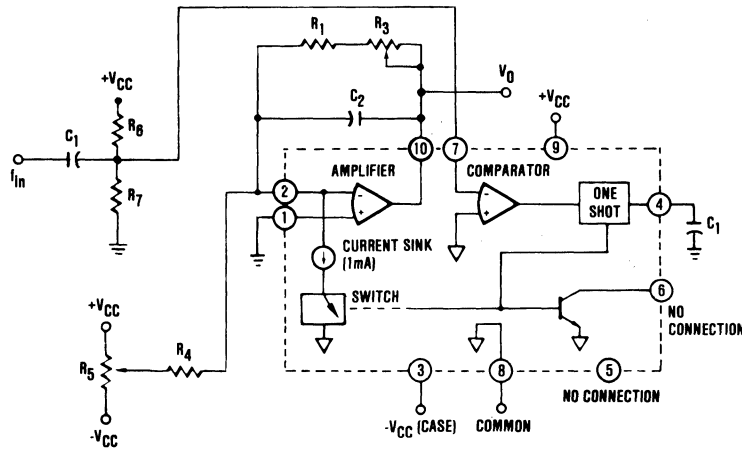
$$f_o = \frac{-V_{IN}}{7.5\,(R_1 + R_3)\,C_1}$$

V_{cc} = ±15VDC
V_{pu} = 5VDC
V_{in} = -10VDC to +0VDC
f_o = ≈4Hz to 10kHz

EXTERNAL COMPONENTS

R_1 = 30kΩ R_5 = 50kΩ
R_2 = 1.2kΩ C_1 = 3300pF (D = 0.25)
R_3 = 20kΩ C_2 = 0.01μF
R_4 = 10MΩ

FIGURE 3. Connection Diagram, Voltage-to-Frequency Operation, Negative Input.



TRANSFER FUNCTION

$V_o = 7.5\,(R_1 + R_3)\,C_1\,f_{in}$
V_{cc} = ±15VDC
f_{in} = 10Hz to 10kHz (TTL)
V_o = ±0.01VDC to +10VDC

EXTERNAL COMPONENTS

R_1 = 30kΩ R_6 = 12kΩ
R_3 = 20kΩ C_1 = 3300pF (D = 0.25)
R_4 = 10MΩ C_2 = 0.01μF
R_5 = 50kΩ C_3 = 0.01μF

FIGURE 4. Connection Diagram, Frequency-to-Voltage Operation.

External component selection is typical. See paragraph 3.3.3.

The duty cycle (D) may be selected by the user to any value $\leq 70\%$ ($D \leq 0.70$). The 70% limit is due to component tolerances, offset, temperature effects, etc., and allowing 0.70mA as the minimum value for the 1mA (nominal) current sink, the worst case, maximum input current, $V_{IN}/(R_1 + R_3)$, is 0.50mA.

The normal, recommended duty cycle is 25% ($D = 0.25$) because this yields the best linearity. This is a maximum input current, $V_{IN}/(R_1 + R_3)$, of 0.25mA. The value of the external capacitor C_1 is the primary determinant of duty cycle and it is selected first; it determines the period t_2. Then the maximum input current, $V_{IN}/(R_1 + R_3)$, is computed to satisfy the VFC transfer function, which determines the total VFC period, $t_1 + t_2$.

For frequencies above 100kHz, the recommended duty cycle is 50% ($D = 0.50$); that is, 0.50mA maximum input current. This provides additional time for t_2 and compensates for the inherent delay time within the integrated circuit. This additional time allows the output transistor to turn off, providing a logic "1" output pulse, especially at elevated temperature.

3.3.4. External component selection. Refer to Figures 2, 3, and 4 for examples of external components' selection. One-shot capacitor C_1. This capacitor determines the duration of the logic "1" output pulse. For a 25% duty cycle ($D = 0.25$), 0.25mA maximum input current, use the first equation and select the closest standard value. For any duty cycle, D, use the second equation.

$$C_1\,(pF) = \frac{33 \times 10^6}{f_{MAX}} - 30 \quad \text{or} \quad C_1\,(pF) = \frac{D \times 133 \times 10^6}{f_{MAX}} - 30$$

The initial tolerance of this capacitor is not critical because R_3 can be adjusted to remove the initial gain error. The temperature coefficient is critical because it adds directly as a transfer function error. An NPO ceramic type capacitor is recommended. Every effort should be made to minimize parasitic capacitance and C_1 should be mounted as close as possible to the VFC.

Input resistor $R_1 + R_3$. $R_1 + R_3$ determines the magnitude of the input current which charges the integrating capacitor C_2. The total resistance is calculated according to

$$R_1 + R_3 = \frac{V_{IN}\ max}{I_{IN}}$$

Normally, I_{IN} is 0.25mA; refer to paragraph 3.3.3.1. R_1, as a percentage of the R_1 and R_3 total resistance, should be 90% minus the percent initial tolerance of C_1. R_3 is the initial gain error adjustment, and as a percentage of the $R_1 + R_3$ total resistance, R_3 should be 20% plus twice the percent initial tolerance of C_1. The initial tolerance of R_1 and R_3 are not critical, but the temperature coefficients are critical because they add directly as transfer function errors. If the input signal is current rather than a voltage, R_1 and R_3 are replaced with a short circuit, and the removal of a gain error then requires adjustment of C_1.

Trimming components R_4 and R_5. R_5 nulls the offset voltage of the input amplifier (VFC offset error). It should have a resistance between 10kΩ and 100kΩ and a temperature coefficient less than or equal to 100ppm/°C. R_4 should be 10MΩ and may be a 20% carbon composition resistor.

Output pull-up resistor R_2. Select a 10% carbon composition resistor according to

$$R_{2\ min} = \frac{V\ pull\text{-}up}{8mA - I_{from\text{-}the\text{-}load}}$$

For high frequency operation, $f \geq 100kHz$, it is necessary to minimize the capacitive loading of the output terminal, pin 6, to allow the open collector output voltage to rise rapidly to logic "1". One way to shorten the time constant formed by the pull-up resistance and the capacitance at this node is to lower the pull-up resistance. Do not exceed 16mA collector current. Note that the output saturation voltage will exceed 0.4V. The best way to shorten the time constant is to minimize the capacitive loading. The use of a TTL buffer is effective.

Integrating capacitor C_2. C_2 is a function of the full scale frequency and is selected according to

$$C_2\,(\mu F) = \frac{10^2}{f_{max}} \qquad (0.001\mu F\ minimum)$$

Select the closest standard value to the calculated value. The initial tolerance and temperature coefficient are not critical since C_2 does not appear in the transfer function. The leakage current of C_2 is critical as it introduces a gain error. Select a capacitor type with small leakage compared to the full scale input current (0.25mA); a mylar type is recommended.

Frequency-to-voltage operation R_6, R_7, C_3.
To interface with TTL logic, the input should be coupled through a capacitor (C_3), and the minus input to the comparator, pin 7, biased near +2.5V (see Figure 4). The converter will detect the falling edge of the input pulse train as the voltage at

pin 7 crosses -0.6V. The converter will reset as the voltage at pin 7 goes positive and crosses +1.0V. Choose C_3 for an appropriate R_6, R_7, C_3 time constant such that the time, t, from -0.6V to +1.0V, meets the specified pulse width range requirements (Table I). For input signals with amplitudes less than 5V, it will be necessary to bias pin 7 closer to zero to insure that the input signal at pin 7 crosses the -0.6V threshold. Errors may be nulled (see paragraph 3.3.5) using 0.001 of full scale frequency to null the offset, and full scale frequency to null the gain error.

Power supply bypass capacitors. Each power supply should be bypassed to ground as close as possible to the converter with 0.01μF capacitors.

3.3.5. Offset and gain error null. The VFC is capable of being nulled to zero offset and zero gain error using the circuits shown in Figures 2, 3, and 4. R_5 effects zero offset error; R_3 effects zero gain error.

The offset and gain error null adjustment procedure is:

a. Apply an input voltage that should produce an output frequency of 0.001 of full scale.
b. Adjust R_5 for 0.001 of full scale frequency.
c. Apply full scale input voltage. 1/
d. Adjust R_3 for full scale frequency.
e. Repeat steps a through e.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

3.4 Electrical Tests. Electrical test requirements are as specified in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2).
b. Inspection lot identification code. 2/
c. Manufacturer's identification (BURR-BROWN®).
d. Manufacturer's designating symbol (CEBS).
e. Country of origin (U.S.A.).

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions for /MIL and /883B Hi-Rel product designations, including rebonding, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3.

For the standard model, Hi-Rel product designation (none), routine manufacturing processing includes Burr-Brown internal visual inspection, stabilization bake, fine leak, gross leak, constant acceleration, and external visual inspection per MIL-STD-883, method 5004, class B.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /MIL Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to mircocircuit delivery.

NOTE:
1/ For optimum linearity it is recommended that gain error nulling be performed at 90% of full scale frequency rather than at 100% of full scale frequency.
2/ A four-digit date code, indicating year and week of seal, is marked on 883B and (none) Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics

All characteristics T_A = -55°C to +125°C, $\pm V_{CC}$ = 15VDC, unless otherwise specified.

CHARACTERISTICS	CONDITIONS	VFC32 V GRADE MIN	VFC32 V GRADE TYP	VFC32 V GRADE MAX	VFC32 W GRADE MIN	VFC32 W GRADE TYP	VFC32 W GRADE MAX	VFC32 U GRADE MIN	VFC32 U GRADE TYP	VFC32 U GRADE MAX	UNITS
INPUT (V/F CONVERTER)											
Bias current	T_A = +25°C										
Inverting input			10	40		•	•		•	•	nA
Noninverting input			50	100		•	•		•	•	nA
Offset voltage 1/	T_A = +25°C		1	4		•	•		•	•	mV
Differential impedance	T_A = +25°C	330 ‖ 10	650 ‖ 10		•	•		•	•		kΩ ‖ pF
Common-mode impedance	T_A = +25°C	300 ‖ 3	500 ‖ 3		•	•		•	•		MΩ ‖ pF
INPUT (F/V CONVERTER)											
Impedance	T_A = +25°C	50 ‖ 10	150 ‖ 10		•	•		•	•		kΩ ‖ pF
Logic "1"		+1.0		+V_{CC}	•		•	•		•	V
Logic "0"		-V_{CC}		-0.6	•		•	•		•	V
Pulse-width range		0.1		150k/F_{MAX}	•		•	•		•	µsec
ACCURACY											
Linearity error 2/	T_A = +25°C: 0.01Hz ≤ oper freq ≤ 10kHz		±0.005	±0.010 3/		±0.003	±0.006		±0.005	±0.010	% of FSR 4/
	T_A = +25°C: 10kHz ≤ oper freq ≤ 100kHz		±0.025	±0.050		•	•		•	•	% of FSR
	T_A = +25°C: 100kHz ≤ oper freq ≤ 500kHz		±0.050	±0.200		•	•		•	•	% of FSR
Offset error (input offset voltage) 1/	T_A = +25°C			±4			•			•	mV
Offset drift 5/	-25°C to +85°C									±3	ppm of FSR/°C
	-55°C to +125°C			±3			±3			±9	ppm of FSR/°C
Gain error 1/	T_A = +25°C		5	10		•	•		•	•	% of FSR
Gain drift 5/	f = 10kHz -25°C to +85°C						±100			±150	ppm/°C
	f = 10kHz -55°C to +125°C			±200			±100			±300	ppm/°C
Full scale drift (offset drift & gain drift) 5/ 6/	f = 10kHz -25°C to +25°C				-100	-50	0	-150		+50	ppm of FSR/°C
	+25°C to +85°C				0	+25	+100	-50		+150	ppm of FSR/°C
	f = 10kHz -55°C to +25°C	-200	-50	+100	-100	-50	0	-300		+100	ppm of FSR/°C
	+25°C to +125°C	-100	+50	+200	0	+50	+100	-100		+300	ppm of FSR/°C
	f = 200kHz -55°C to +25°C	-400	-200	0							ppm of FSR/°C
	+25°C to +125°C		0	±150							ppm of FSR/°C
Power supply sensitivity	f = DC, $\pm V_{CC}$ = 12VDC to 18VDC		±0.030	±0.040		•	•		•	•	% of FSR/%
OUTPUT (V/F CONVERTER) (open collector output)											
Voltage, logic "0"	I_{SINK} = 8mA	0	0.2	0.4	•	•	•	•	•	•	V
Leakage current, logic "1"	V_O = 15V		0.01	1.0		•	•		•	•	µA
Voltage, logic "1"	External pull-up resistor required (see Figure 2)			V_{PU}			•			•	V
Pulse width			0.25/F_{MAX}			•			•		sec
Fall time	I_{OUT} = 5mA, C_{LOAD} = 500pF			400			•			•	nsec
OUTPUT (F/V CONVERTER)											
Voltage	I_O = 7mA	0 to +10			•			•			V
Current	V_O = 7VDC	+10			•			•			mA
Impedance	Closed loop			1			•			•	Ω
Capacitive load	Without oscillation			100			•			•	pF
DYNAMIC RESPONSE											
Full scale frequency		500			•			•			kHz
Dynamic range		6			•			•			decades
Settling time	(V/F) to specified linearity ΔV_{IN} = 10V		7/			•			•		
Overload recovery	<50% overload		7/			•			•		
POWER SUPPLY											
Quiescent current	T_A = +25°C		±4.5	±6.0		•	•		•	•	mA
TEMPERATURE RANGE (ambient)											
Operating		-55		+125	•		•	•		•	°C
Storage		-65		+150	•		•	•		•	°C

*Specification the same as V grade.

NOTES:

1/ Adjustable to zero. See paragraph 3.3.5.

2/ Linearity error is specified at any operating frequency from the straight line intersecting 90% of full scale frequency and 0.1% of full scale frequency. See paragraph 7.

3/ ±0.015% of FSR for negative inputs.

4/ FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).

5/ Exclusive of external components' drift.

6/ Positive drift is defined to be increasing frequency with increasing temperature.

7/ One pulse of new frequency plus 1µsec.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MODELS / MIL-STD-883 test requirement (class B)	VFC32VM/MIL	VFC32VM VFC32VM/883B	VFC32WM VFC32WM/883B	VFC32UM VFC32UM/883B
	SUBGROUPS (SEE TABLE III)			
Interim electrical parameters (preburn-in) (method 5004)	1	1	1	1
Final electrical test parameters (method 5004)	1*, 4, 5, 6	1, 4, 5, 6	1, 4, 5, 5U, 6, 6U	1, 4, 5, 5U, 6, 6U
Group A test requirements (method 5005)	1, 4, 5, 6	--	--	--
Groups C and D end point electrical parameters (method 5005)	Table IV	--	--	--
Additional electrical subgroups for group C inspection	2, 3	--	--	--

*PDA applies to subgroup 1 (see 4.3.c)

TABLE III. Group A Inspection.

SUBGROUP	PARAMETERS	CONDITIONS $+V_{CC}$ = 15V, unless otherwise specified	LIMITS VFC32 V GRADE MIN	 MAX	 VFC32 W GRADE MIN	 MAX	 VFC32 U GRADE MIN	 MAX	UNITS
1	Input offset voltage			4		*		*	mV
T_A = +25°C	Input bias current (inverting input)			40		*		*	nA
	Input bias current (noninverting input)			100		*		*	nA
	Output logic "0"	Pin 6 I_{SINK} = 10mA		0.4		*		*	V
	Output leakage current (logic 1	Pin 6 V_{OUT} = 15V		1.0		*		*	µA
	Quiescent current	$+V_{CC}$ and $-V_{CC}$		±6.0		*		*	mA
2									
T_A = +125°C	Output logic "0"	Pin 6 I_{SINK} = 8mA		0.4		*			V
3									
T_A = -55°C	Output logic "0"	Pin 6 I_{SINK} = 8mA		0.4		*			V
4									
T_A = +25°C	Gain error, unadjusted	f = $f_{FULL\ SCALE}$= 200kHz		±20					kHz
	Linearity error	f = 200kHz		±200					Hz
	$f_{FULL\ SCALE}$ = 200kHz 1/	f = 150kHz		±200					Hz
		f = 100kHz		±100					Hz
		f = 50kHz		±100					Hz
		f = 10kHz		±20					Hz
		f = 5kHz		±20					Hz
		f = 1kHz		±20					Hz
	Gain error, unadjusted	f = $f_{FULL\ SCALE}$= 10kHz				±1		±1	kHz
	Linearity error	f = 10kHz				±0.6		±1	Hz
	$f_{FULL\ SCALE}$ = 10kHz 1/	f = 7kHz				±0.6		±1	Hz
		f = 5kHz				±0.6		±1	Hz
		f = 1kHz				±0.6		±1	Hz
		f = 0.5kHz				±0.6		±1	Hz
		f = 0.1kHz				±0.6		±1	Hz
5									
T_A = +125°C	Full scale drift	f = 200kHz 2/ +25°C to +125°C	-3.0	+3.0					kHz
	Full scale drift	f = 10kHz 2/ +25°C to +125°C			0	+100			Hz
5U									
T_A = +85°C	Full scale drift	f = 10kHz 2/ +25°C to +85°C			0	+60	-30	+90	Hz
6									
T_A = -55°C	Full scale drift	f = 200kHz 2/ -55°C to +25°C	-6.4	0					kHz
	Full scale drift	f = 10kHz 2/ -55°C to +25°C			-80	0			Hz
6U									
T_A = -25°C	Full scale drift	f = 10kHz 2/ -25°C to +25°C			-50	0	-75	+25	Hz

*Limits the same as V grade.

NOTE:

1/ Linearity error is adjusted or normalized to zero at 90% of full scale frequency and at 0.1% of full scale frequency.

2/ Subtract the frequency at the colder temperature from the frequency at the hotter temperature.

TABLE IV. Groups C and D, End Point Electrical Parameters (T_A = +25°C, $\pm V_{CC}$ = 15VDC).

TEST	LIMITS
	VFC32VM/MIL
Input Offset Voltage	4mV
Input Bias Current (-)	40nA
Input Bias Current (+)	100nA
Full Scale Drift	±3kHz (Hot)
	-6.4kHz, 0Hz (Cold)

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005 except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices. The following additional criteria apply:

a. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
b. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) T_A = +125°C minimum
   (4) Test duration is 160 hours minimum
c. Percent defective allowable (PDA). The PDA, for /MIL Hi-Rel product designations only, is 10 percent based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter test prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
d. External visual inspection need not include measurement of case and lead dimensions.

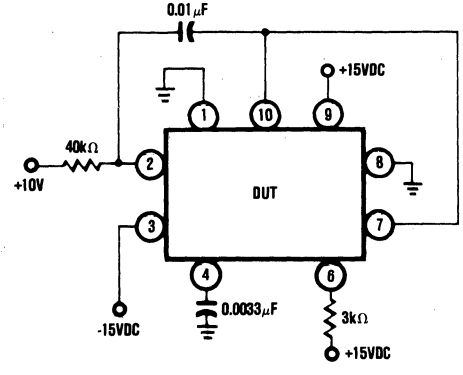


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5005, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5005. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table I, and as follows:

a. Tests are specified in Table II herein.
b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table II (class B).

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table III, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.

4.4.4. Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table IV, and as follows:

a. End point electrical parameters are specified in Table IV herein.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group D as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. Caution - these microcircuits may be damaged by electrostatic discharge. Precautions should be observed at all times.

7. DISCUSSION OF SPECIFICATIONS.

7.1 Linearity. Linearity is the maximum deviation of the actual transfer function from the straight line intersecting 90% of the full scale frequency (90% of full scale input) and 0.1% of the full scale frequency (≈ zero input). Linearity is the true measure of a VFC's performance. Linearity error is a function of the full scale frequency as shown in Figure 6. For a given full scale frequency the linearity error decreases with decreasing operating frequency as shown in Figure 7. To allow the user to benefit with improved linearity at lower frequencies, linearity error is specified in bands of operating frequency (see Table I).

7.2 Frequency stability versus temperature. The full scale frequency drift of the VFC32 versus temperature is shown in Figure 8. The temperature coefficient effects of the external components (especially R_1 and C_1) must be added to the drift of the converter.

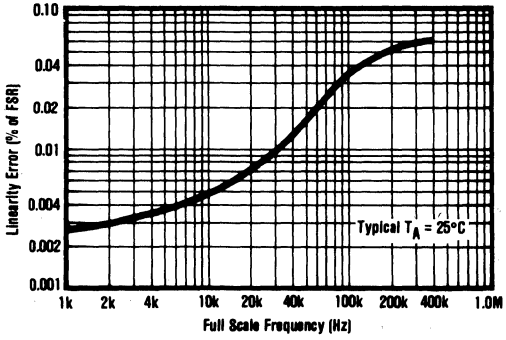


FIGURE 6. Linearity Error vs Full Scale Frequency.

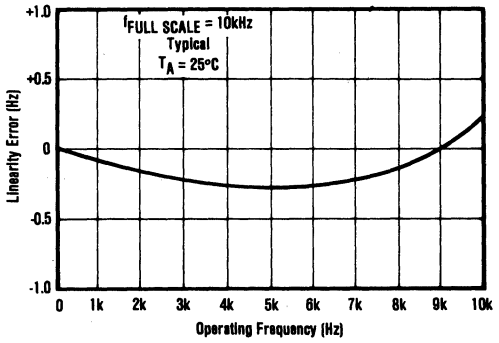


FIGURE 7. Linearity Error vs Operating Frequency.

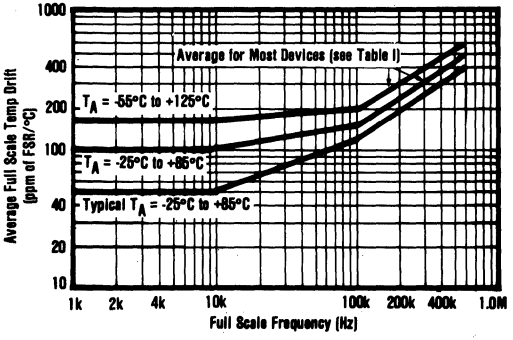


FIGURE 8. Full Scale Drift vs Full Scale Frequency.

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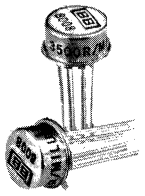


3500/MIL SERIES

MODEL NUMBERS:
3500R/MIL
3500R/883B
3500U/883B

REVISION A
OCTOBER, 1981

General Purpose - Military OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, ±30nA, MAX
- LOW DRIFT, ±20μV/°C, MAX
- LOW NOISE, 1.4μV, rms
- WIDE SUPPLY RANGE, ±3VDC to ±20VDC
- INTERNAL COMPENSATION
- HI-REL MANUFACTURE

APPLICATIONS

- GENERAL PURPOSE AMPLIFIER
- ANALOG COMPUTATION
- PRECISION BUFFER
- LOW DRIFT INTEGRATOR
- BRIDGE AMPLIFIER
- STABLE REFERENCE CIRCUITS

DESCRIPTION

The 3500 IC op amps are designed for low input current while maintaining slew rate and bandwidth adequate for most applications. The low input bias current is achieved by a unique bias current cancelling circuit. This method insures that the bias current remains low over the full temperature and common-mode voltage ranges. The same circuitry gives the amplifier high impedance, both differential and common-mode.

The 3500 is also a low noise IC op amp. Both current and voltage noise are low, including the low frequency "flicker" and "popcorn" noise which usually prevent the use of IC op amps for low-level signal processing.

The 3500 is internally compensated for unconditional stability for all feedback configurations, even with capacitive loads. The slew rate is independent of supply voltage level. The input stage of the 3500 series exhibits no latch-up when the common-mode voltage range is exceeded. The input impedance remains high with differential inputs as high as ±30 volts, thus the amplifier can be used as a sensitive comparator. The output stage is internally current-limited to provide protection against continuous short circuits. The 3500 is interchangeable with 741 type amplifiers but gives greatly improved performance.

These devices are manufactured in a hi-rel environment with clean room conditions which assures "built-in" quality. Each device is 100% internally visually inspected per MIL-STD-883 method 2010 and after the cap is welded on, the balance of the MIL-STD-883 method 5004 class B screening is completed.

The /MIL suffixed devices are processed further by Quality Assurance, performing groups A and B inspections on each inspection lot and groups C and D inspections when specified on the customer's purchase order. A report containing the most recent groups A, B, C, and D tests is available for a nominal charge.

The R grade devices offer the best performance over the ambient temperature range of -55°C to +125°C. However, if the operating ambient temperature range will not exceed -25°C to +85°C, such as with test equipment, the U grade device provides full performance at lower cost.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DETAILED SPECIFICATION MICROCIRCUITS, LINEAR OPERATIONAL AMPLIFIER MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

3500	R	/MIL
Basic model number	Grade (see 1.2.1)	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single, operational amplifier. Two electrical performance grades are provided, the R grade and the U grade, with the R grade offering the higher electrical performance.

1.2.2 Device class. The device class is similar to the product assurance level class B, as defined in MIL-M-38510.

The Hi-Rel product designator portion of the part number distinquishes the product assurance level as follows.

Hi-Rel product designator	Requirements
/MIL	Basic model, plus 100% MIL-STD-883 class B screening with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
/883B	Basic model, plus 100% MIL-STD-883 class B screening.

1.2.3 Case outline. The case outline (8-lead can) is as defined in Figure 4. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC 1/
Differential input voltage range	±40VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±3VDC to ±20VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ C-A
8-lead can	FIGURE 4	225mW at T_A = 125°C	70°C W	220°C W

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead finish is gold plate. The lead material and finish is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The microcircuit die is glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

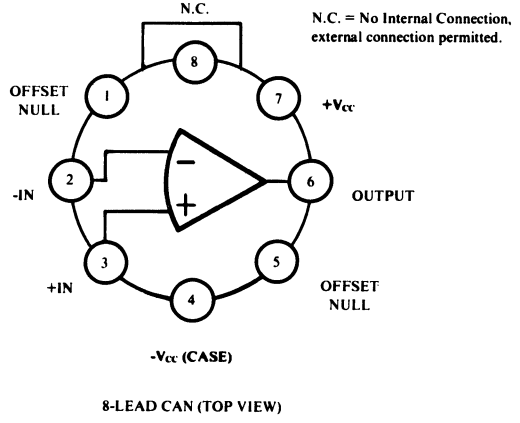


FIGURE 1. Terminal Connections.

FIGURE 2. Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Offset and gain error null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 2. If nulling is unnecessary for the application, delete the potentiometer and make no connections.

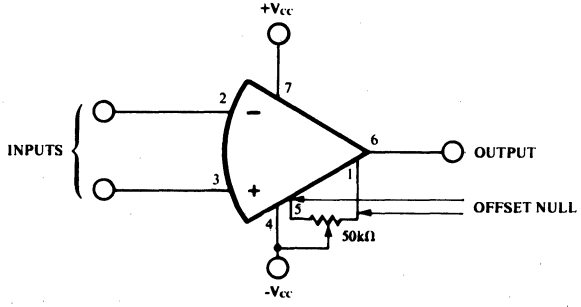


FIGURE 2. Offset Null Circuit.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated at any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table III. The sub-groups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcirucit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin (U.S.A)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions for the MIL Hi-Rel product designation, including rebonding, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening is in accordance with MIL-STD-883, method 5004, class B, except as modified in paragraph 4.3 herein.

For the /MIL Hi-Rel product designator, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection for the MIL Hi-Rel product designation is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

1/ A four-digit data code, indicating year and week of seal, is maked on /883B Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics.

All characteristics at -55°C ≤ T_A ≤ +125°C, $\pm V_{CC}$ = 15VDC, unless otherwise specified.

Characteristics	Symbol	Conditions		3500R/MIL 3500R/883B Min	Typ	Max	3500U/883B Min	Typ	Max	Units
OUTPUT										
Voltage	V_O	R_L = 1kΩ		±10	±12		*	*		V
Current	I_O	R_L = 1kΩ		±10			*			mA
Resistance	R_O				2			*		kΩ
Current, short circuit	I_{OS}	To ground	T_A = 25°C	±10	±22		*	*		mA
OPEN-LOOP VOLTAGE GAIN	A_{VS}	f = 0Hz, No load		93	106		*	*		dB
DYNAMIC RESPONSE										
Bandwidth	BW	Unity gain	T_A = 25°C	1	1.5	2	*	*	*	MHz
			-55°C ≤ T_A ≤ +125°C	0.75	1.2		*	*		MHz
Bandwidth, full power	BW_{FP}		T_A = 25°C	10	25		*	*		kHz
Slew rate	SR		T_A = 25°C	0.6	1.2		*	*		V/μsec
			-55°C ≤ T_A ≤ +125°C	0.4			*			V/μsec
INPUT										
Offset voltage	V_{IO}	V_{CM} = 0	T_A = 25°C		±2	±5		*	*	mV
Offset voltage temperature sensitivity	$\Delta V_{IO}/\Delta T$		-25°C ≤ T_A ≤ +85°C						±20	μV/°C
			-55°C ≤ T_A ≤ +125°C			±20			±60	μV/°C
Bias current	I_B	V_{CM} = 0	T_A = 25°C		±10	±30		*	*	nA
Bias current temperature sensitivity	$\Delta I_B/\Delta T$		-25°C ≤ T_A ≤ +85°C						±1.0	nA/°C
			-55°C ≤ T_A ≤ +125°C			±1.5			±3.0	nA/°C
Offset current	I_{IO}	V_{CM} = 0	T_A = 25°C		±10	±30		*	*	nA
Offset current temperature sensitivity	$\Delta I_{IO}/\Delta T$		-25°C ≤ T_A ≤ +85°C					±0.5	±1.0	nA/°C
			-55°C ≤ T_A ≤ +125°C		±0.7	±1.5			±3.0	nA/°C
Power supply rejection	PSRR		T_A = 25°C		±40			*		μV/V
Common-mode voltage range	CMV	Linear operation	T_A = 25°C	±11	±12		*	*		V
Common-mode rejection	CMR	V_{CM} = ±10V	T_A = 25°C	90	100		*	*		dB
			-55°C ≤ T_A ≤ +125°C	80			*			dB
Impedance	Z_{IS}	T_A = 25°C	Differential		10^7 ‖ 3			*		Ω ‖ pF
			Common mode		10^9 ‖ 3			*		Ω‖ pF
Noise voltage	e_n	0.3Hz to 10Hz	T_A = 25°C		2	3		*	*	μV, p-p
		10Hz to 10kHz	T_A = 25°C		1.4	2		*	*	μV, rms
Noise, current	i_n	0.3Hz to 10Hz	T_A = 25°C		200	300		*	*	pA, p-p
		10Hz to 10kHz	T_A = 25°C		35	100		*	*	pA, rms
POWER SUPPLY										
Quiescent current	I_Q		T_A = 25°C		±2.5	±3.5		*	*	mA
TEMPERATURE RANGE (ambient)										
Operating				-55		+125	-55		+125	°C
Storage				-65		+150	-65		+150	°C

Notes:
*Specifications the same as 3500R/MIL.

TABLE II. Electrical Test Requirements.
(The individual tests within the subgroups appear in Table III.)

MODELS / MIL-STD-883 Test Requirement (class B)	3500R/MIL	3500R/883B 3500U/883B
	SUBGROUPS (see Table III)	
Interim electrical parameters (pre burn-in)(method 5004)	1	1
Final electrical test parameters (method 5004)	1*, 2, 4, 5, 6	1, 2A, 4, 5, 6
Group A test requirements (method 5005)	1, 2, 4, 5, 6	---
Groups C and D end point electrical parameters (method 5005)	Table IV delta limits and limits	---
Additional electrical subgroups for group C inspections	7	---

*PDA applies to subgroup 1 (see 4.3d)

TABLE III. Group A Inspection

Subgroup	Symbol	MIL-STD-883 method or equivalent	Conditions $\pm V_{CC}$ = 15V unless otherwise specified	Limits 3500R/MIL 3500R/883B Min	3500R/MIL 3500R/883B Max	3500U/883B Min	3500U/883B Max	Units
1	V_{IO}	4001			±5		±5	mV
T_A = 25°C	I_B	4001			±30		±30	nA
	I_{IO}	4001			±30		±30	nA
	I_Q	4005			±3.5		±3.5	mA
	CMR	4003	V_{CM} = ±10V	90		90		dB
2	$\Delta V_{IO}/\Delta T$	4001			±20			µV/°C
T_A = +125°C	$\Delta I_B/\Delta T$	4001			±1.5			nA/°C
to T_A = -55°C	$\Delta I_{IO}/\Delta T$	4001			±1.5			nA/°C
2A	$\Delta V_{IO}/\Delta T$	4001					±20	µV/°C
T_A = +85°C	$\Delta I_{IB}/\Delta T$	4001					±1.0	nA/°C
to T_A = -25°C	$\Delta I_{IO}/\Delta T$	4001					±1.0	nA/°C
4	A_{VS}	4004	f = 0Hz, no load	93		93		dB
T_A = 25°C	SR	4002		0.6		0.6		V/µsec
5	A_{VS}	4004	f = 0Hz, no load	93		93		dB
T_A = +125°C	SR	4002	G = +1, ΔV_o = 10V, R_l = 1kΩ	0.4		0.4		V/µsec
6	A_{VS}	4004	f = 0Hz, no load	93		93		dB
T_A = -55°C	SR	4002	G = +1, ΔV_o = 10V, R_l = 1kΩ	0.4		0.4		V/µsec
7	e_n		0.3Hz to 10Hz		3			µV, p-p
T_A = 25°C			10Hz to 10kHz		2			µV, rms
	i_n		0.3Hz to 10Hz		300			pA, p-p
			10Hz to 10kHz		100			pA, rms

TABLE IV. Groups C and D, End Point Electrical Parameters
(T_A = +25°C, $\pm V_{CC}$ = 15, V_{CM} = 0V)

Test	Limit	Delta
V_{IO}	±5mV	±2.5mV
I_{IB}	±36nA	±30nA

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5005 except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order.

Burr-Brown has performed and successfully completed qualification inspection as described below. The qualification report is available from Burr-Brown.

When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

4.3 Screening. Screening is in accordance with MIL-STD-883, method 5004, class B, and is conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition D, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 3 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for the / MIL Hi-Rel product designation only, is 10 percent based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5004, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter test prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

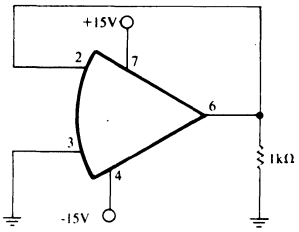


FIGURE 3 Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5005, are performed on each inspection lot. Groups C and D inspections of MIL-STD-883, method 5005, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5005. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table I, and as follows:

a. Tests are specified in Table II herein.

b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table II (class B).

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table III, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 3 herein
   (3) $T_A = 125°C$ minimum
   (4) Test duration is 1000 hours minimum

b. End point electrical parameters are specified in Table II herein.

c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5005, Table IV, and as follows:

a. End point electrical parameters are specified in Table IV herein.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

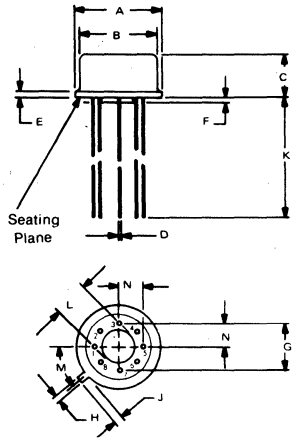
a. Complete part number (see paragraph 1.2)

b. Requirement for certificate of compliance, if desired.

6.4 Substitutability. Mircocircuits furnished under this specification are similar to Burr-Brown model 3500.

6.5 Microcircuit group assignment. These mircocircuits are assigned to Technology Group D as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.



NOTE:
Leads in true position within 0.10" (25mm) R at MMC at seating place.
Pin numbers shown for reference only. Numbers may not be marked on package.
Weight: 3 grams max.

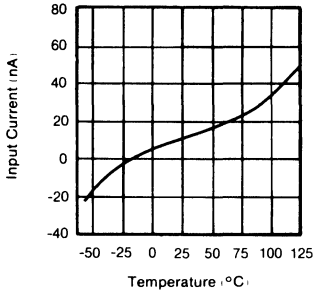
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 4. Case Outline (TO-99 Package Configuration).

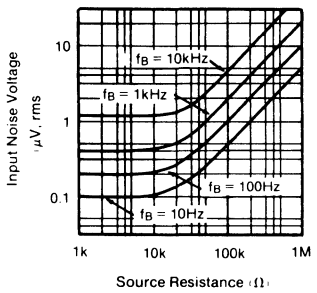
7. ELECTRICAL PERFORMANCE CURVES.

(Typical at T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise specified).

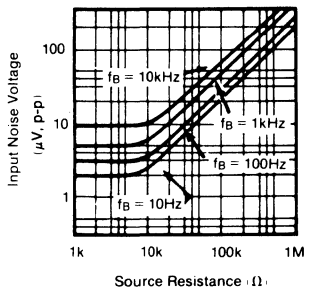
INPUT BIAS CURRENT vs. TEMPERATURE



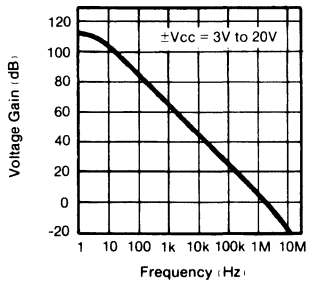
RMS INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



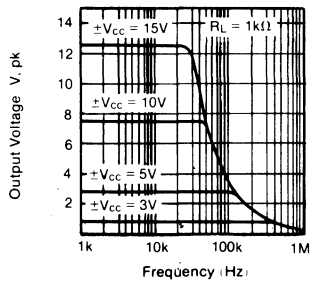
P-P INPUT NOISE VOLTAGE vs. SOURCE RESISTANCE



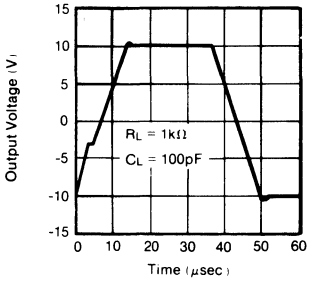
OPEN-LOOP FREQUENCY RESPONSE



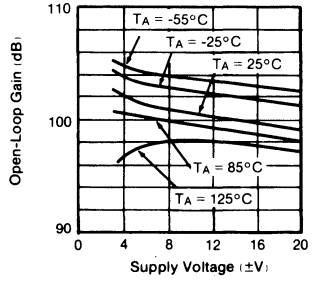
OUTPUT VOLTAGE vs. FREQUENCY



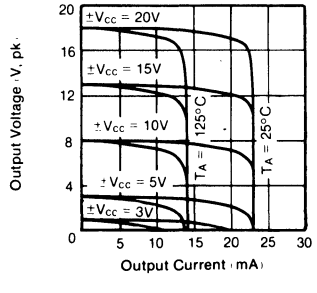
VOLTAGE FOLLOWER STEP RESPONSE



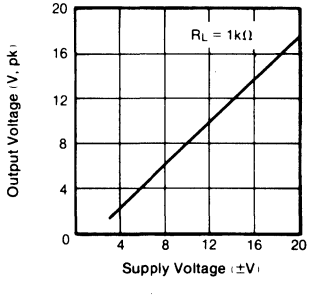
VOLTAGE GAIN vs. SUPPLY VOLTAGE



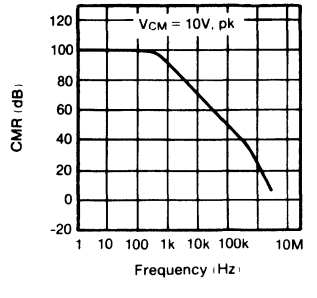
OUTPUT VOLTAGE vs. OUTPUT CURRENT



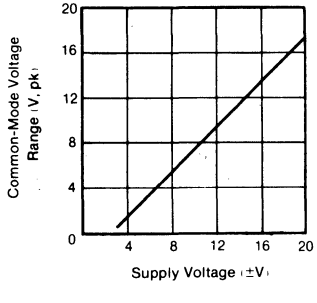
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



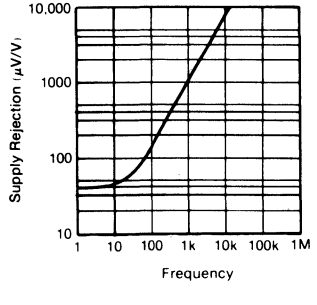
COMMON-MODE REJECTION vs. FREQUENCY



COMMON-MODE RANGE vs. SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs. FREQUENCY



3500R MIL

8. APPLICATIONS INFORMATION

8.1 Offset Adjustment. The input offset voltage of the Model 3500 may be adjusted to zero by connecting a 50kΩ potentiometer between pins 1 and 5 with the wiper arm connected to negative supply (Figure 5a). This provides an adjustment range of approximately ±10mV. This offset control is optional and may be omitted if the specified offset is considered sufficiently low.

Adjustment of the input offset voltage of the 3500 will affect the voltage drift to some extent. A rough "rule-of-thumb" is ±3μV/°C change of drift for each 1.0mV of offset adjustment. This is true of other IC op amps, such as the 741, 101, etc., but is usually masked by the greater drift of these units. However, in low drift amplifiers, this effect must be considered. By use of a transistor as in Figure 5b the effect of the offset adjustment on drift can be substantially reduced (by approximately a factor of six).

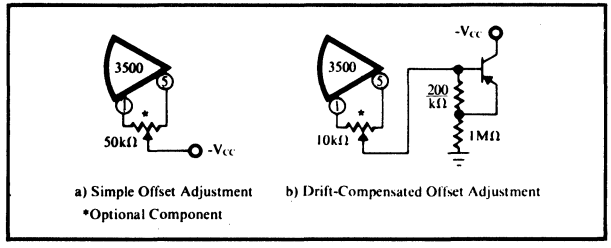


FIGURE 5. Offset Adjustment Techniques.

8.2 Bias Current Effects. Input bias current of the amplifier creates additional offset voltages by flowing in the impedances of the signal source and the feedback network. Although the bias currents of the 3500 are quite small, their effects may be appreciable when these impedances are large. The bias currents at the two inputs tend to be equal and the difference current smaller than either. Thus equalizing the resistance from each input to common, as in Figure 6, is an effective means of reducing DC offset due to bias current.

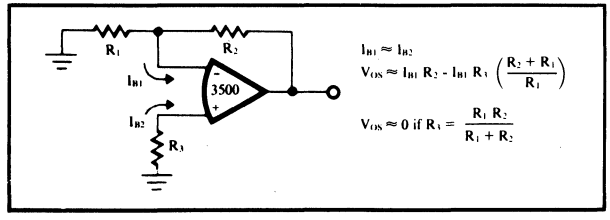


FIGURE 6. Minimization of Bias Current Effects.

8.3 Operation on a Single Supply. Although virtually any op amp can be operated on a single supply if input and output voltage limitations are observed, the Model 3500 is particularly suitable for such use. Its wide supply range of ±3VDC to ±20VDC translates to a single supply operating range of 6VDC to 40VDC, plus or minus. Two possible modes of operation on a single supply are shown in Figure 7. The following conditions must be observed to keep the amplifier within its linear region of operation.

1) $+2 < V_O < (V_{CC} - 2)$

2) $+3 < V_{IN} < (V_{CC} - 3)$. Figure 7b.

When operating on a single supply ($+V_{CC}$), shorting the output to common is equivalent to a short to supply and the internal power dissipation is approximately twice that which occurs for a short to common with balanced supplies of $\pm(V_{CC}/2)$. This dissipation may exceed safe limits for single supply voltages greater than 20V and must be prevented by use of a series limiting resistor or other device, if short circuit protection is desired.

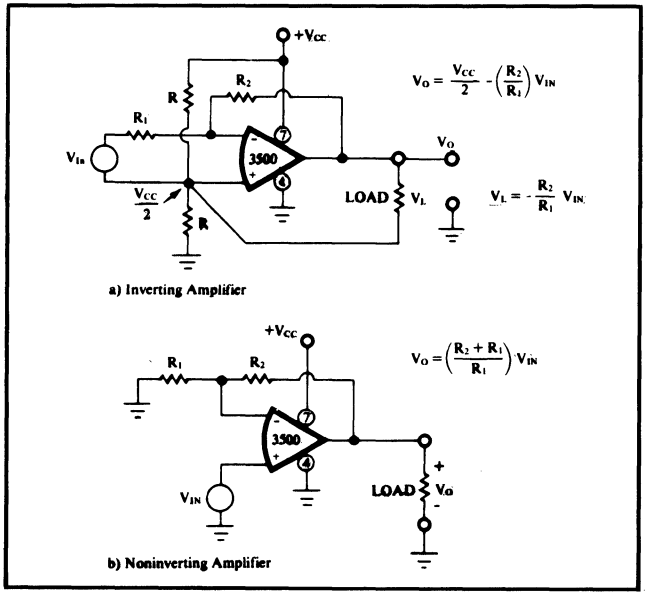
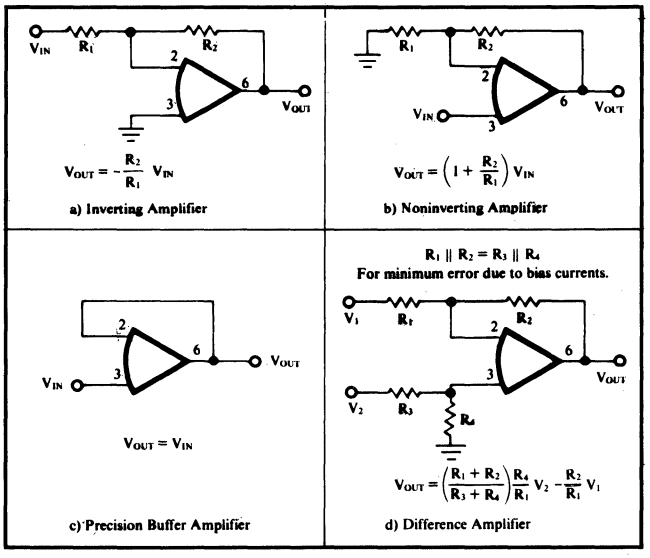


FIGURE 7. Operation on a Single Supply.

8.4 Wiring Precautions. In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 0.001μF ceramic capacitor from pins 7 and 4 to the power supply common.

8.5 Typical Applications.



BURR-BROWN®

3510VM/MIL

REV. NONE
NOVEMBER, 1978
Amendment 1 Incorporated
April, 1979

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
MONOLITHIC, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic, low offset voltage drift, integrated circuit operational amplifier.

1.2 Part number. The complete part number is as shown below.

3510	V	M	/MIL
Basic model number	Grade	Metal package	Hi-Rel product designator

1.2.1 Device type. The device is a single, operational amplifier.

1.2.2 Device class. The device class is similar to the product assurance level class B, as defined in MIL-M-38510.

1.2.3 Case outline. The case outline (8-lead can) is as defined in Figure 5. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC 1/
Differential input voltage range	±40VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1/ The absolute maximum input voltage is equal to the supply voltage.

2/ Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

1.2.5 Recommended operating conditions.

Supply voltage range ---------- ±3VDC to ±20VDC
Ambient temperature range ---------- -55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
8-lead can	Figure 5	225mW at T_A = 125°C	70°C/W	220°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.
SPECIFICATION
MILITARY
MIL-M-38510 - Microcircuits, general specification for.
STANDARD
MILITARY
MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead finish is gold plate. The lead material and finish is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

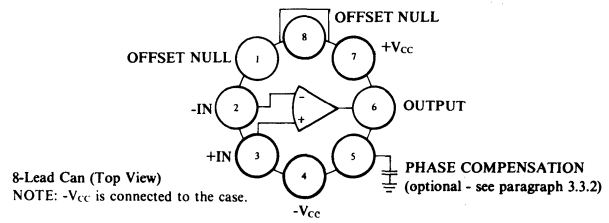


FIGURE 1. Terminal Connections.

3.2.8 Schematic circuit. The schematic circuit is shown in Figure 2.

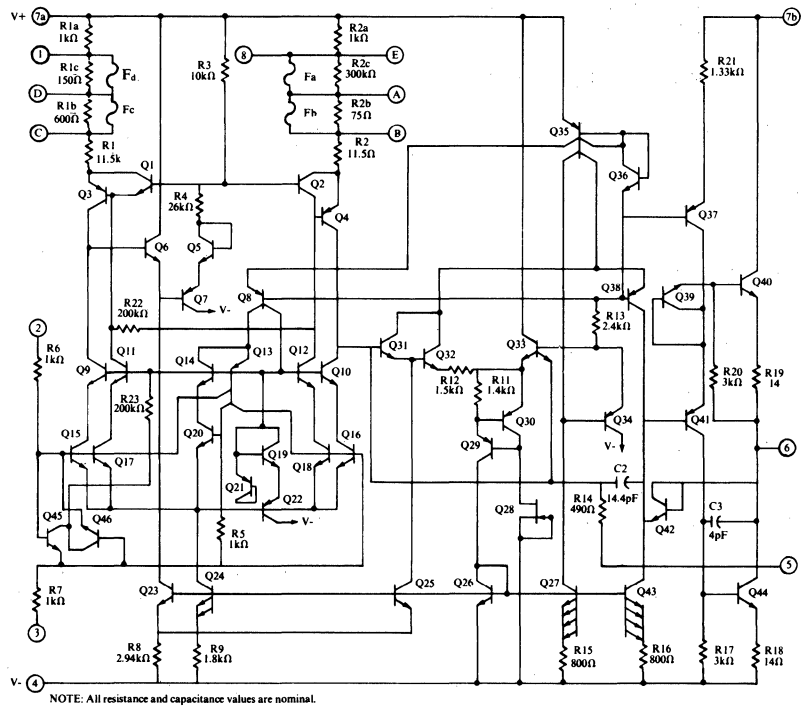


FIGURE 2. Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

3.3.1 Offset and gain error null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 3.

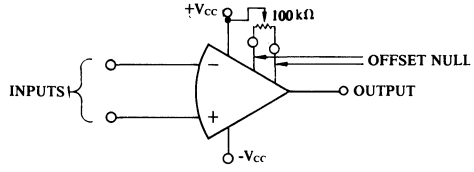


FIGURE 3. Offset Null Circuit.

3.3.2 Frequency compensation. The amplifier is free of oscillation when operated at a gain of 10 or greater with no external compensation and a source resistance of $\leq$10kΩ and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table III. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code
c. Manufacturer's identification
d. Manufacturer's designating symbol
e. Country of origin

TABLE I. Electrical Performance Characteristics.

Characteristics	Symbol	Conditions ($\pm V_{CC}$ = 15V, unless otherwise specified)		Limits Min	Limits Max	Units
Input offset voltage	V_{IO}		T_A = 25°C		±120	µV
			-55°C ≤ T_A ≤ +125°C		±350	µV
Input offset voltage temperature sensitivity (unnulled V_{IO})	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from -55°C to +25°C			±2	µV/°C
		ΔT_A from +25°C to +125°C			±2	µV/°C
Input offset current	I_{IO}		T_A = 25°C		±15	nA
			-55°C ≤ T_A ≤ +125°C		±55	nA
Input offset current temperature sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from -55°C to +25°C			±0.4	nA/°C
		ΔT_A from +25°C to +125°C			±0.4	nA/°C
Input bias current	I_{IB}		T_A = 25°C		±25	nA
			-55°C ≤ T_A ≤ +125°C		±85	nA
Input bias current temperature sensitivity	$\frac{\Delta I_{IB}}{\Delta T}$	ΔT_A from -55°C to +25°C			±0.6	nA/°C
		ΔT_A from +25°C to +125°C			±0.6	nA/°C
Power supply rejection ratio	+PSRR	+V_{CC} = 10V -V_{CC} = -15V	T_A = 25°C		3	µV/V
Power supply rejection ratio	-PSRR	+V_{CC} = 15V -V_{CC} = -10V	T_A = 25°C		3	µV/V
Input voltage common-mode rejection	CMR	V_{CM} = -10V to +10V	T_A = 25°C	110		dB
Adjustment for input offset voltage	V_{IO} ADJ (±)			±1.5		mV
Output short circuit current (for positive output)	I_{OS} (+)		+25°C ≤ T_A ≤ +125°C	10	30	mA
			-55°C ≤ T_A ≤ +25°C	10	40	mA
Output short circuit current (for negative output)	I_{OS} (-)		+25°C ≤ T_A ≤ +125°C	10	30	mA
			-55°C ≤ T_A ≤ +25°C	10	40	mA
DC power dissipation (quiescent)	P_D	±V_{CC} = 20V	T_A = -55°C		170	mW
			T_A = +25°C		150	mW
			T_A = +125°C		130	mW
Single-ended input impedance (noninverting input)	Z_{IS1}		T_A = 25°C	1.5		MΩ
			-55°C ≤ T_A ≤ +125°C	1.0		MΩ
Single-ended input impedance (inverting input)	Z_{IS2}		T_A = 25°C	1.5		MΩ
			-55°C ≤ T_A ≤ +125°C	1.0		MΩ
Output voltage swing (maximum)	V_{OM}		R_L = 10kΩ	±11		V
			R_L = 1kΩ	±10		V
Open-loop voltage gain (single-ended) 1/	A_{VS} (±)	R_L = 2kΩ f = 0Hz	T_A = 25°C	120		dB
			-55°C ≤ T_A ≤ +125°C	114		dB
Open-loop voltage gain (single-ended) 1/	A_{VS} (±)	R_L = 2kΩ f = 0Hz	±V_{CC} = 3V T_A = 25°C	95		dB
Bandwidth, unity gain, small signal	BW		T_A = 25°C	0.25		MHz
Slew rate	SR (±)	V_{OUT} = ±10V, R_L = 1kΩ, A = +10, T_A = 25°C		0.5		V/µsec
Bandwidth, full power	BW_{FP}	V_{OUT} = ±10V, R_L = 1kΩ, A = +10, T_A = 25°C 2/		7		kHz
Input noise voltage	e_n	T_A = 25°C	0.1Hz to 10Hz		4.0	µV, pk-pk
			f_o = 1kHz		25	nV/√Hz
Input noise current	I_n	T_A = 25°C	0.1Hz to 10Hz		250	pA, pk-pk
			f_o = 1kHz		0.7	pA/√Hz

1/ Note that gain is not specified at $V_{IO\ ADJ}$ extremes. Some gain reduction is usually seen at $V_{IO\ ADJ}$ extremes.
2/ This parameter is untested. It is guaranteed by the slew rate test.

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared by Burr-Brown in fullfillment of the product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding, are in accordance with MIL-M-38510.

TABLE II. Electrical Test Requirements.

MIL-STD-883 test requirement (class B)	Subgroups (see Table III)
Interim electrical parameters (pre burn-in)(method 5004)	1A
Final electrical test parameters (method 5004)	1A*, 2A, 3A, 4A
Group A test requirements (method 5005)	1A, 2A, 3A, 4A, 7
Groups C and D end point electrical parameters (method 5005)	Table IV delta limits and limits
Additional electrical subgroups for group C inspections	1C, 2C, 3C, 4C, 5, 6

*PDA applies to subgroup 1A (see 4.3.c)

TABLE III. Group A Inspection.

Subgroup	Symbol	MIL-STD-883 method or equivalent	Test	Conditions $\pm V_{CC}$ = 15V, unless otherwise specified	Limits Min	Limits Max	Units
1A T_A = 25°C	V_{IO}	4001	1			±120	µV
	I_{IO}	4001	2			±15	nA
	I_{IB}	4001	3			±25	nA
	+PSRR	4003	4	$+V_{CC}$ = 10V, $-V_{CC}$ = -15V		3	µV/V
	-PSRR	4003	5	$+V_{CC}$ = 15V, $-V_{CC}$ = -10V		3	µV/V
	CMR	4003	6	V_{CM} = -10V to +10V	110		dB
	$I_{OS}(+)$ 1/	3011	7	5sec. min 2/	10	30	mA
	$I_{OS}(-)$ 1/	3011	8	5sec. min 2/	10	30	mA
	P_D	4005	9			105	mW
	$V_{IO\ ADJ}$		10		±1.5		mV
1C T_A = 25°C	$Z_{IS}1$		11		1.5		MΩ
	$Z_{IS}2$		12		1.5		MΩ
2A T_A = 125°C	V_{IO}	4001	13			±350	µV
	$\Delta V_{IO}/\Delta T$		14	$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}\text{ (test 13)} - V_{IO}\text{ (test 1)}}{100°C}$		±2	µV/°C
	I_{IB}	4001	15			±50	nA
	$\Delta I_{IB}/\Delta T$		16	$\frac{\Delta I_{IB}}{\Delta T} = \frac{I_{IB}\text{ (test 15)} - I_{IB}\text{ (test 3)}}{100°C}$		±0.6	nA/°C
	I_{IO}	4001	17			±20	nA
	$\Delta I_{IO}/\Delta T$		18	$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}\text{ (test 17)} - I_{IO}\text{ (test 2)}}{100°C}$		±0.4	nA/°C
2C T_A = 125°C	$V_{IO\ ADJ}$		19		±1.5		mV
	$Z_{IS}1$		20		1.0		MΩ
	$Z_{IS}2$		21		1.0		MΩ
3A T_A = -55°C	V_{IO}	4001	22			±310	µV
	$\Delta V_{IO}/\Delta T$		23	$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}\text{ (test 22)} - V_{IO}\text{ (test 1)}}{80°C}$		±2	µV/°C
	I_{IB}	4001	24			±85	nA
	$\Delta I_{IB}/\Delta T$		25	$\frac{\Delta I_{IB}}{\Delta T} = \frac{I_{IB}\text{ (test 24)} - I_{IB}\text{ (test 3)}}{80°C}$		±0.6	nA/°C
	I_{IO}	4001	26			±55	nA
	$\Delta I_{IO}/\Delta T$		27	$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}\text{ (test 26)} - I_{IO}\text{ (test 2)}}{80°C}$		±0.4	nA/°C
3C T_A = -55°C	$V_{IO\ ADJ}$		28		±1.5		mV
	$Z_{IS}1$		29		1.0		MΩ
	$Z_{IS}2$		30		1.0		MΩ
4A T_A = 25°C	V_{OM}	4004	31	R_L = 10kΩ, $\pm V_{CC}$ = 20V	±16		V
	V_{OM}	4004	3/	R_L = 1kΩ	±10		V
	A_{VS}	4004	32	R_L = 2kΩ, V_{OUT} = ±10V, f = 0Hz	120		dB
	SR(±)	4002	33	V_{OUT} = ±10V, R_L = 1kΩ, A = +10	0.5		V/µsec
4C T_A = 25°C	A_{VS}		34	$\pm V_{CC}$ = 3V, R_L = 1kΩ	95		dB
5 T_A = 125°C	A_{VS}		35	R_L = 1kΩ, V_{OUT} = ±10V	114		dB
6 T_A = -55°C	A_{VS}		36	R_L = 1kΩ, V_{OUT} = ±10V	114		dB
7 T_A = 25°C	e_n		37	f_B = 0.1Hz to 10Hz		4.0	µV, pk-pk
	i_n		38	f_n = 0.1Hz to 10Hz		250	pA, pk-pk

NOTES:

1/ Due to significant power dissipation and associated device heating, these tests shall always be the last tests performed in any given sequence, followed by operational verification.

2/ The five second minimum test duration for I_{OS} test shall apply only for group A sampling inspections. For screening final electrical test, test duration for I_{OS} may be reduced to be consistent with automated test procedures.

3/ This parameter is untested. It is guaranteed by the conditions of the slew rate test.

TABLE IV. Groups C and D, End Point Electrical Parameters.
.(T_A = 25°C, $\pm V_{CC}$ = 15, V_{CM} = 0V)

Test	Limit	Delta
V_{IO}	±180μV	±60μV
I_{IB}	±45nA	±20nA
I_{IO}	±17.5nA	±2.5nA

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing processes which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening is in accordance with method 5004 of MIL-STD-883, class B, except as modified in paragraph 4.3 herein. All microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening is in accordance with method 5004 of MIL-STD-883, class B, and is conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria apply:

a. Interim and final electrical test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
b. Burn-in test (method 1015 of MIL-STD-883) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) T_A = 125°C minimum
   (4) Test duration is 160 hours minimum
c. Percent defective allowable (PDA). The PDA is 10 percent based on failures from group A, subgroup 1A test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameters tests prior to burn-in are omitted, then all screening failures are included in the PDA. The verified failures of group A, subgroup 1A after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.
d. External visual inspection need not include measurement of case and lead dimensions.

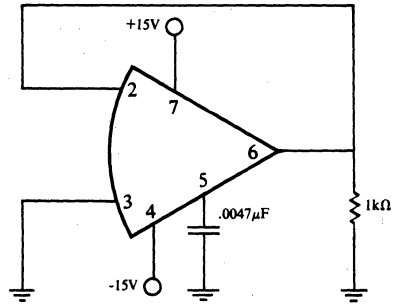


FIGURE 4. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of method 5005, MIL-STD-883, are conducted on each inspection lot. Groups C and D inspections of method 5005, MIL-STD-883, are not required unless specifically required by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of method 5005, MIL-STD-883. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in Table I of method 5005 of MIL-STD-883 and as follows:

a. Tests are specified in Table II herein.
b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in Table II (class B) of method 5005 of MIL-STD-883. The package does not contain a desiccant and, therefore, the internal water vapor content test is not required.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in Table III of method 5005 of MIL-STD-883 and as follows:

a. Steady state life test (method 1005 of MIL-STD-883) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 4 herein
   (3) T_A = 125°C minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table IV herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in Table IV of method 5005 of MIL-STD-883 and as follows:

a. Internal water-vapor content test is not required.
b. End point electrical parameters are specified in Table IV herein.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

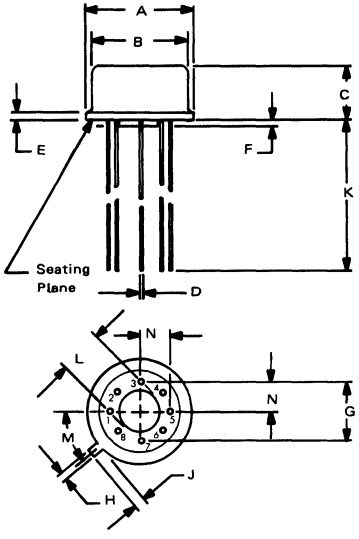
6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:
a. Complete part number (see paragraph 1.2).
b. Requirement for certificate of compliance, if desired.

6.4 Substitutability. Microcircuits furnished under this specification are similar to Burr-Brown model 3510.



NOTE:
Leads in true position within .010"
(.25mm) R at MMC at seating plane.

Pin numbers shown for reference only.
Numbers may not be marked on package.

Weight: 3 grams max.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 5. Case Outline (TO-99 Package Configuration).

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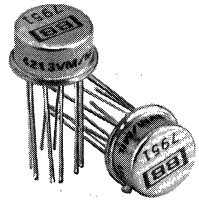


4213/MIL SERIES

MODEL NUMBERS:

4213WM/883B
4213WM
4213UM/883B
4213UM
4213VM/MIL
4213VM/883B
4213VM

REVISION A
NOVEMBER, 1981

Military
MULTIPLIER - DIVIDER

FEATURES

- **HI REL MANUFACTURE**
- **ACCURATE**
  - **±1/2% TOTAL ERROR (W grade)**
  - **±1% TOTAL ERROR (V and U grades)**
- **4-QUADRANT MULTIPLICATION**
  2-QUADRANT DIVISION
- **NO EXTERNAL COMPONENTS NECESSARY**
- **DIFFERENTIAL INPUT**
- **MIL-STD-883B SCREENING**
- **-55°C TO +125°C SPECIFICATIONS**

DESCRIPTION

The 4213/MIL Series is a high performance, precision multiplier/divider with a total full scale error of ±1/2% or ±1%. It is intended for transducer and analog computation applications; it will also square, square root, and perform trigonometric computations. It has differential inputs and is ideal for instrumentation applications. The operating range is -55°C to +125°C. The 4213/MIL is a hybrid microcircuit consisting of a monolithic bipolar IC and a precision laser-trimmed thin-film network. It is assembled into a hermetic TO-100 (10-lead can).

These devices are manufactured on a separate Hi-Rel manufacturing line with impeccable clean room conditions which assures "built-in" quality and provides for a long product life.

The 4213/MIL Series is available in three electrical performance grades. The W grade features premium accuracy (±1/2% total error, ±50mV feedthrough, and ±25mV offset error). The V grade features ±1% total error, ±100mV feedthrough, and ±30mV offset error. The U grade has excellent performance from -25°C to +85°C and is also specified from -55°C to +125°C. U grade applications include test equipment, shipboard, ground support, and industrial applications where operation is normally between -25°C and +85°C and full temperature operation must be assured.

Three product assurance levels are available: standard, /883B, and /MIL. The standard models have many MIL-STD-883 screens performed routinely. The /883B suffixed devices are 100% screened per MIL-STD-883 method 5008 hybrid class (class B). /MIL suffixed devices feature Hi-Rel manufacture, 100% screening per MIL-STD-883 method 5008 hybrid class, and a 10% PDA. Quality assurance further processes /MIL devices, performing group A and B inspections on each inspection lot and group C and D inspections periodically and when specified on the customer's purchase order. A report containing the most recent group A, B, C, and D tests is available for a nominal charge.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

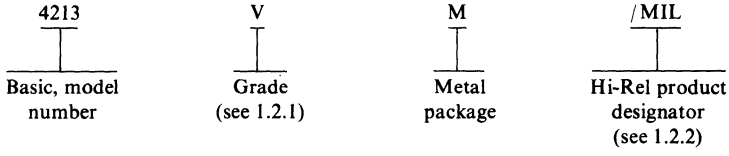
PDS-458

DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
MULTIPLIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a precision, integrated circuit multiplier.

1.2 Part Number. The complete part number is as shown below.



1.2.1 Device type. The device is a single, four-quadrant, analog multiplier; it will also function as a single, two-quadrant, analog divider, a squarer, a square rooter, etc. (see paragraph 8.3). Three electrical performance grades are provided. The W grade features premium accuracy of ±1/2% total error, ±50mV feedthrough and ±25mV offset error. The V grade features ±1% total error, ±100mV feedthrough and ±30mV offset error. The U grade features excellent performance from -25°C to +85°C and guarantees performance from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device Class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance level as follows:

Hi-Rel product designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B performed on each inspection lot, plus Groups C and D performed initially and periodically thereafter.
/883	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model, including 100% electrical testing.

1.2.3 Case outline. The case outline is A-2 (10-lead can, TO-100) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range (X, Y, and Z inputs)	±20VDC 1/
Differential input voltage (X, Y, and Z inputs)	±40VDC 1/
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited 2/
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = 175°C

1/ The absolute maximum input voltage is equal to the supply voltage.
2/ Short circuit may be to ground only. Rating applies to +125°C case temperature or +75°C ambient temperature at ±15VDC supply voltage.

1.2.5 Recommended operating conditions.

Supply voltage range	±8.5VDC to ±20VDC
Ambient temperature range	-55°C to +125°C
Input voltage range ($\pm V_{CC}$ = 15VDC)	±10VDC

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C	Maximum θ J-A
10-lead can (TO-100)	A-2	225mW at T_A = 125°C	70°C/W	220°C/W

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements, the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510, except that organic and polymeric materials are used for die attach. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Glassivation. The dice utilized are glassivated.

3.2.6 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.7 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.8 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 1.

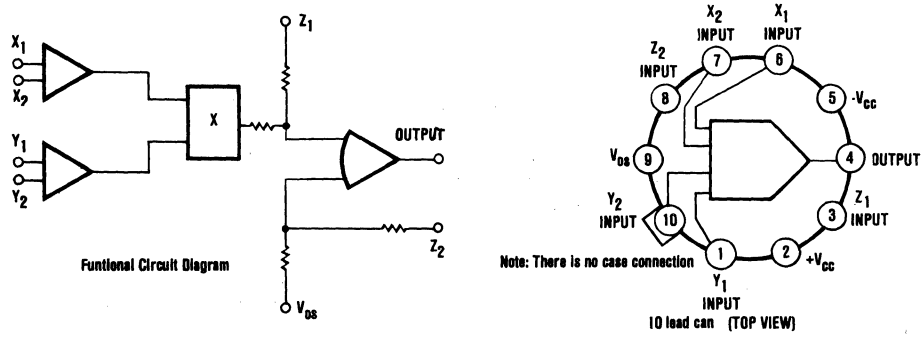


FIGURE 1. Functional Circuit Diagram and Terminal Connections.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C, unless otherwise specified.

TABLE I. Electrical Performance Characteristics.

All characteristics T_A = -55°C to +125°C, $\pm V_{CC}$ = 15VDC, unless otherwise noted.

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMITS 4212WM/883B 4213WM MIN	TYP	MAX	4213VM/MIL 4213VM/883B 4213VM MIN	TYP	MAX	4213UM/883B 4213UM MIN	TYP	MAX	UNITS
ACCURACY												
Total Error	E_T	Each quadrant T_A = +25°C			1/2			1			1	±% of FSR
		-25°C to +85°C									2	±% of FSR
		T_A = -55°C			3			3			4	±% of FSR
		T_A = +125°C			4			4			8	±% of FSR
Feedthrough												
X Input	FT_X	V_X = 20V, p-p T_A = +25°C		30	50		30	100			100	±mV, p-p
		V_Y = 0, f = 50Hz -55°C to +125°C			100			200			200	±mV, p-p
Y Input	FT_Y	V_X = 0, f = 50Hz T_A = +25°C		25	40		25	80			80	±mV, p-p
		V_Y = 20V, p-p -55°C to +125°C			80			180			180	±mV, p-p
Nonlinearity												
X Input	LIN_X	V_X = 20V, p-p, V_Y = ±10V T_A = +25°C		0.08			*			*		±% of FSR
Y Input	LIN_Y	V_Y = 20V, p-p, V_X = ±10V T_A = +25°C		0.01			*			*		±% of FSR
INPUT												
Input Resistance	R_{IN}	X, Y, Z inputs, pin 9 open	3.5	10		*	*		*	*		MΩ
Input Bias Current	I_{IB}	X, Y, Z inputs T_A = +25°C		1.4	2.5		*	*		*	*	μA
		-55°C to +125°C			6			*			*	μA
Input Voltage Range	V_{IN}	Rated Operation	±10			*			*			V
Common-mode Rejection	CMR	+10V, -6V	60			*			*			dB
DYNAMIC CHARACTERISTICS												
Small Signal Bandwidth ±3dB	BW_{3dB}	X and Y inputs T_A = +25°C	450	550		*	*		*	*		kHz
Bandwidth ±1 flatness	$BW_{1\%}$	X and Y inputs T_A = +25°C	70			*			*			kHz
Full Power Bandwidth	BW_{FP}	T_A = +25°C	130			*			*			kHz
Slew Rate	SR	X and Y inputs T_A = +25°C	20			*			*			V/μsec
OUTPUT												
Output Voltage	V_{OM}	R_L = 2kΩ, C_L = 1000pF	10			*			*			±V
Output Resistance	R_O	Closed loop		1.5	10		*	*		*	*	Ω
Output Noise	N	T_A = +25°C { 1Hz to 10kHz			200			*			*	μV, rms
		{ 1Hz to 10MHz			1000			*			*	μV, rms
Output Offset Error 1/	V_{OO}	T_A = +25°C			25			30			50	±mV
		-25°C to +85°C									100	±mV
		-55°C to +125°C			100			100			200	±mV
Output Offset Error Temperature Sensitivity	$\frac{\Delta V_{OO}}{\Delta T}$	-25°C to +85°C									1.7	±mV/°C
		-55°C to +125°C			1.0			1.0			2.0	±mV/°C
Short Circuit Current	I_{OS}	T_A = +25°C	5		20	*		*	*		*	mA
		-55°C to +125°C	5		30	*		*	*		*	mA
POWER SUPPLY												
Power Supply Range			8.5	15	20	*	*	*	*	*	*	±V
Power Dissipation, Quiescent		T_A = +25°C		150	180		*	*		*	*	mW
		-55°C to +125°C			225			*			*	mW
TEMPERATURE RANGE (AMBIENT)												
Operating			-55		+125	*		*			*	°C
Storage			-65		+150	*		*			*	°C

*Specifications same as 4213WM

NOTE:

1/ Externally adjustable to zero.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Transfer functions. The transfer functions for multiplier and divider connections are shown in Figure 2.

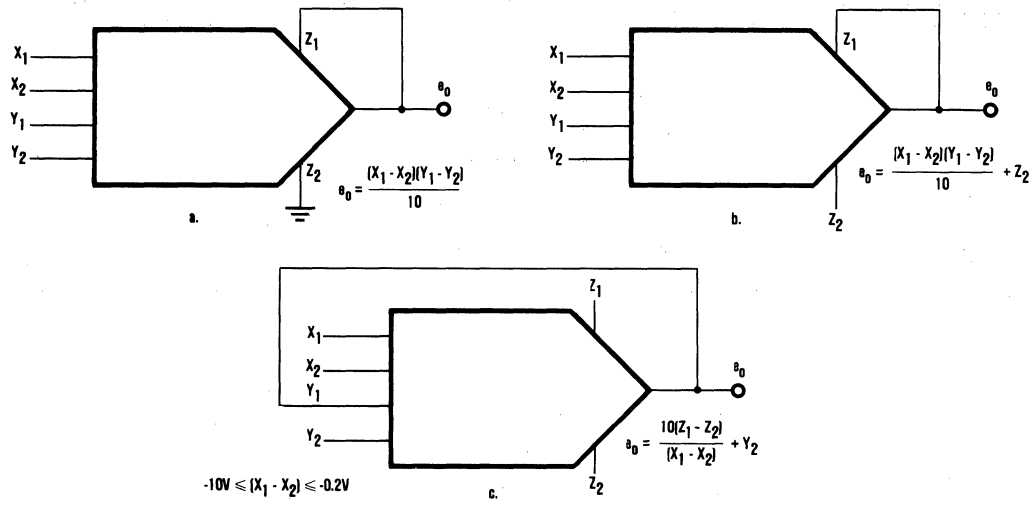


FIGURE 2. Transfer Functions.

3.3.3 Output offset error null. The multiplier is capable of being nulled to zero offset error using the circuit in Figure 3.

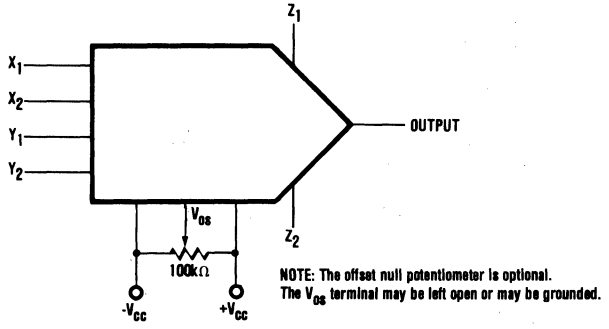


FIGURE 3. Offset Null Circuit.

3.4 Electrical tests. Electrical test requirements are specified in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883 TEST REQUIREMENTS (HYBRID CLASS) / MODELS	4213WM/883B 4213WM	4213VM/MIL	4213VM/883B 4213VM	4213UM/883B 4213UM
	Subgroups (see Table III)			
Interim electrical parameters (pre burn-in) (method 5008)	1	1	1	1
Final electrical test parameters (method 5008)	1, 2, 3, 4, 5, 6	1*, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6	1, 2U, 3U, 4, 5U, 6U
Group A test requirements (method 5008)	--	1, 2, 3, 4, 5, 6, 4A	--	--
Group C end point electrical parameters (method 5008)	--	Table IV limits and delta limits	--	--
Additional electrical subgroups performed prior to Group C inspections	--	1C, 2C, 3C, 5C, 6C, 7C	--	--

*PDA applies to subgroup 1 (see 4.3.d)

TABLE III. Group A Inspection.

SUBGROUP	PARAMETER SYMBOL	CONDITIONS $\pm V_{CC}$ = 15VDC, pin 9 open unless otherwise specified	LIMITS 4213 V GRADE MIN	4213 V GRADE MAX	4213 W GRADE MIN	4213 W GRADE MAX	4213 U GRADE MIN	4213 U GRADE MAX	UNITS
1 T_A = +25°C	V_{OO} I_{IB} P_D	X_1 Input		±30 2.5 180		±25 2.5 180		±50 2.5 180	mV µA mW
1C T_A = +25°C	CMR R_{IN} R_O I_O	X = Y = +10V to -6V	60 3.5 5	 10 20					dB MΩ Ω mA
2 T_A = +125°C	V_{OO}			±100		±100			mV
2U T_A = +85°C	V_{OO}							±100	mV
2C T_A = +125°C	I_{IB} $\frac{\Delta V_{OO}}{\Delta T}$ P_D CMR	X_1 Input $\frac{\Delta V_{OO}}{\Delta T} = \frac{V_{OO}\ (+125°C) - V_{OO}\ (+25°C)}{100°C}$ X = Y = +10V to -6V	 60	6 ±1 225					µA mV/°C mW dB
3 T_A = -55°C	V_{OO}			±100		±100			mV
3U T_A = -25°C	V_{OO}							±100	mV
3C T_A = -55°C	I_{IB} $\frac{\Delta V_{OO}}{\Delta T}$ P_D CMR	X_1 Input $\frac{\Delta V_{OO}}{\Delta T} = \frac{V_{OO}\ (-55°C) - V_{OO}\ (+25°C)}{80°C}$ X = Y = +10V to -6V	 60	6 ±1 225					µA mV/°C mW dB
4 T_A = +25°C	E_T FT_X FT_Y	Each quadrant X = 20V, p-p; Y = 0; f = 50Hz X = 0; Y = 20V, p-p; f = 50Hz		±1 100 80		±1/2 50 40		±1 100 80	% mV, p-p mV, p-p
4A T_A = +25°C	V_{OM}	R_L = 2kΩ, C_L = 1000pF		±10					V
5 T_A = +125°C	E_T	Each quadrant		±4		±4			%
5U T_A = +85°C	E_T	Each quadrant						±2	%
5C T_A = +125°C	V_{OM} FT_X FT_Y	R_L = 2kΩ, C_L = 1000pF X = 20V, p-p; Y = 0; f = 50Hz X = 0; Y = 20V, p-p; f = 50Hz		±10 200 180					V mV, p-p mV, p-p
6 T_A = -55°C	E_T	Each quadrant		±3		±3			%
6U T_A = -25°C	E_T	Each quadrant						±2	%
6C T_A = -55°C	V_{OM} FT_X FT_Y	R_L = 2kΩ, C_L = 1000pF X = 20V, p-p; Y = 0; f = 50Hz X = 0; Y = 20V, p-p; f = 50Hz		±10 200 180					V mV, p-p mV, p-p
7C T_A = +25°C	$BW_{1\%}$ $BW_{1\%}$ SR SR BW_{3dB} BW_{3dB} BW_{FP} N N	X = 20V, p-p; Y = 10V X = 10V; Y = 20V, p-p X = +20V-step; Y = 10V; R_L = 2kΩ X = 10V; Y = +20V-step; R_L = 2kΩ X = 1V, rms; Y = 10V X = 10V; Y = 1V, rms R_L = 20kΩ, V_o = ±10V f_B = 1Hz to 10kHz f_B = 1Hz to 10MHz	70 70 20 20 450 450 130	 200 1000					kHz kHz V/µsec V/µsec kHz kHz kHz µV, rms µV, rms

TABLE IV. Group C, End Point Electrical Parameters.

(T_A = 25°C, $\pm V_{CC}$ = 15VDC)

Test	Limit	Delta
E_T	1.0%	0.66%
V_{OO}	±60mV	25mV

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
c. Manufacturer's identification (BURR-BROWN®)
d. Manufacturer's designating symbol (CEBS)
e. Country of origin (U.S.A)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, for the /MIL Hi-Rel product designation, including rebonding, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability or interchangeability of the microcircuit without full or partial requalification.

3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

For the standard model, Hi-Rel product designation (none), routine manufacturing processing includes Burr-Brown internal visual inspection, and stabilization bake, fine leak, gross leak, burn-in (72 hours, performed preseal), constant acceleration (condition D) and external visual inspection per MIL-STD-883 method 5008 hybrid class.

For the /MIL Hi-Rel product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for the /MIL Hi-Rel product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

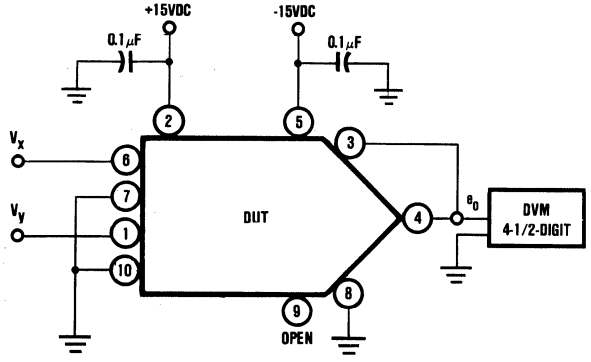


FIGURE 4. Test Circuit for Total Error.

1/ A four-digit date code, indicating year and week of seal, is marked on /883B and (none) Hi-Rel product designations.

PROCEDURE:
1. Set $V_x = V_y = +10.000VDC \pm 1mV$, measure $E_o = E_{o1}$.
2. Set $V_x = V_y = -10.000VDC \pm 1mV$, measure $E_o = E_{o2}$.
3. Set $V_x = +10.000VDC \pm 1mV$ and $V_y = -10.000VDC \pm 1mV$, measure $E_o = E_{o3}$.
4. Set $V_x = -10.000VDC \pm 1mV$ and $V_y = +10.000VDC \pm 1mV$, measure $E_o = E_{o4}$.
5. Calculate $V_{o1} = |E_{o1} - 10|$, $V_{o2} = |E_{o2} - 10|$, $V_{o3} = |E_{o3} + 10|$ and $V_{o4} = |E_{o4} + 10|$.
6. V_{ox} is the largest of V_{o1}, V_{o2}, V_{o3} or V_{o4}.

$$E_T(\%) = \frac{V_{ox}}{10} \times 100$$

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008 except as modified herein.

4.2 Qualification. Qualification is not required unless specified by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C, and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The qualification report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition D, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Burn-in test (MIL-STD-883, method 1015) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum
   (4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for the /MIL Hi-Rel product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

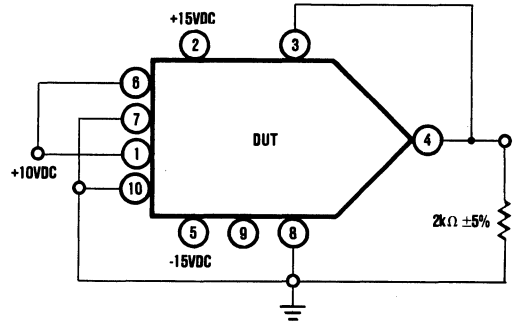


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, are performed on each inspection lot. Group D, subgroup 1, seal test, of MIL-STD-883, method 5008, is performed on each lot of packages procured. Groups C and D inspections of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table I, and as follows:

a. Tests are specified in Table II herein.
b. Tests previously performed as part of final electrical test need not be repeated.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table II and as follows:

a. Particle impact noise detection test is not required.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table III, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition B
   (2) Test circuit is Figure 5 herein
   (3) $T_A = 125°C$ minimum
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table IV, and as follows:

a. Particle impact noise detection test is not required.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Definitions.

Total error. Total error (E_T) is the difference between the actual output voltage and the ideal output voltage expressed as a percentage of the maximum output voltage, 10 volts. It is the sum of the individual errors and includes feedthrough and output offset voltage.

Feedthrough. Feedthrough (FT_X or FT_Y) is the output voltage when the ideal output voltage is zero (i.e., $X = 0$, $Y = \pm V$ or $X = \pm V$, $Y = 0$).

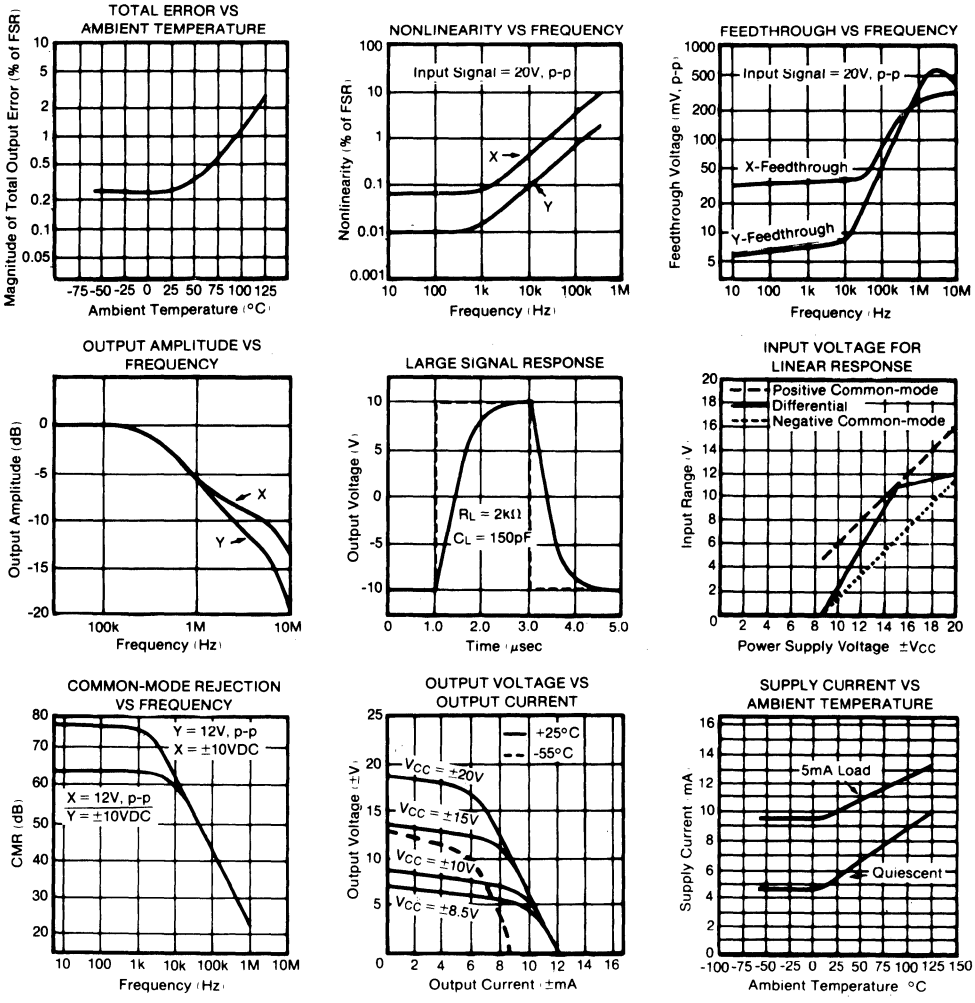
6.5 Microcircuit group assignment. These mircocircuits are assigned to Technology Group F as defined in MIL-M-38510, Appendix E.

6.6 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

6.7 Power Supply Sequencing. Apply, and remove, both supplies together. Alternatively, apply the positive supply first. Permanent damage may occur if the minus supply is applied with an input greater than +6VDC.

7. ELECTRICAL PERFORMANCE CURVES.

(Typical at T_A = +25°C and ± V_{CC} = 15VDC unless otherwise specified.)



8. APPLICATIONS INFORMATION

8.1 Power supply decoupling. For optimum performance and to prevent frequency instability due to power supply lead inductance, each power supply should be decoupled by connecting a 1μF tantalum capacitor from each power supply pin to ground (power supply common).

8.2 Capacitive loads. Stable operation is maintained with capacitive loads up to 1000pF, except for the square root mode which is limited to 50pF. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

8.3 Typical Applications.

8.3.1 Multiplication. The basic connection for four-quadrant multiplication is shown in Figures 2a and 2b. Optional offset nullling is shown in Figure 3. Feedthrough may be minimized by applying an external nulling voltage to the X and/or Y input, as appropriate. Usually, the nulling voltage is applied to X_2 or Y_2. If Z_2 input is not used, it should be grounded.

Figure 6 shows how to achieve a scale factor larger than 0.1 (i.e., a denominator less than 10). A larger scale factor is electrically advantageous in some applications, but this has the disadvantage of proportionately increasing the output offset voltage. Note, the offset may be nulled as shown in Figure 3. Also, the small signal bandwidth is reduced to about 50kHz.

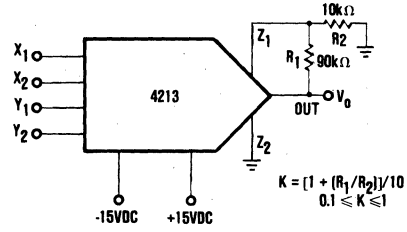


FIGURE 6. Connection for Unity Scale Factor.

8.3.2 Division. The basic connection for two-quadrant division is shown in Figure 2c.
Divider error is approximately

$$\epsilon_{divider} = \frac{10\epsilon_{multiplier}}{X_1 - X_2}$$

Note, the divider error will become very large for small values of $(X_1 - X_2)$. A 10 to 1 denominator range is a practical limit.

8.3.3 Squaring. The basic connection is shown in Figure 7.

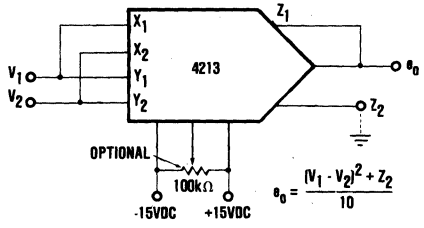


FIGURE 7. Squaring Connection.

8.3.4 Square Root. Figure 8 shows the connection for taking the square root of the voltage $V_{Z1} - V_{Z2}$. The diode prevents a latching condition which could occur if the input momentarily changed polarity. The load resistance R_L must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$ to provide the current necessary to operate the diode. The output offset should be nulled for optimum performance; allow the input to be its smallest expected value and adjust R_1 for the proper output voltage. The square root mode accuracy is then approximately that of the multiply mode.

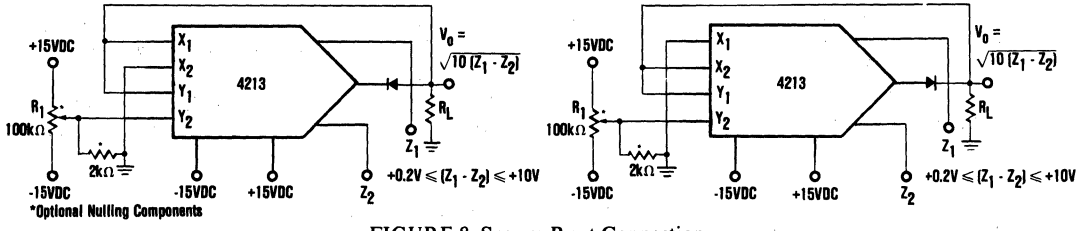


FIGURE 8. Square Root Connection.

8.3.5 Percent. The circuit of Figure 9 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1.

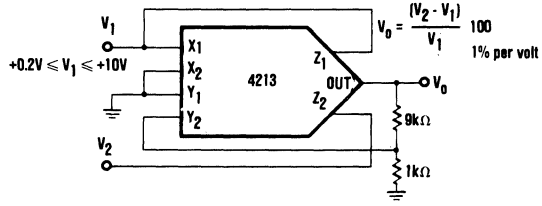


FIGURE 9. Percentage Computation.

8.3.6 Sine Function Generator. The circuit in Figure 10 uses implicit feedback to implement the following sine function approximation: $V_O = (1.5715V_1 - 0.004317V_1^3)/(1 + 0.001398V_1^2) = 10 \sin(9V_1)$.

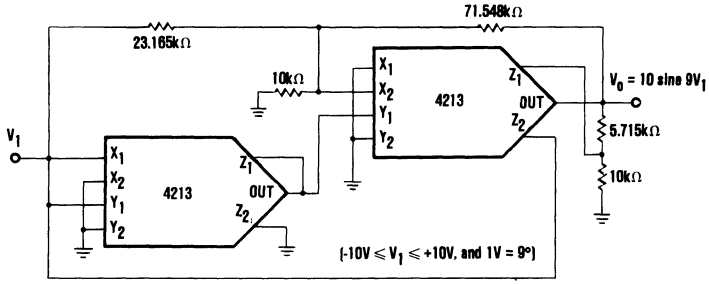


FIGURE 10. Sine Function Generator.

8.3.7 Single-phase Power Measurement. Figure 11 shows a circuit for measurement of single-phase instantaneous and real power.

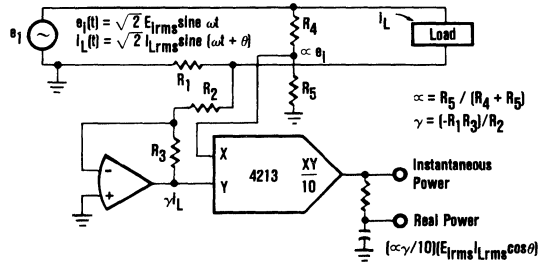


FIGURE 11. Single-Phase Instantaneous and Real Power Measurement.

MODULAR POWER SUPPLIES

Well-regulated DC power is usually required to power modern electronic circuits. Over the years electronic circuits have changed in terms of size and performance. Packaged in small integrated circuit packages or in hybrid modules, more and more electronic circuits now provide significantly improved performance. Burr-Brown encapsulated power supplies have kept up with changing times. We provide a broad line of reliable, self-contained, ready to use power supplies, at low cost, to meet OEM and design engineers' power supply requirements.

Burr-Brown standard series AC/DC power supplies and DC/DC converters provide maximum flexibility in systems design. They are particularly useful for powering analog interface circuitry involving operational amplifiers, A/D and D/A converters, instrumentation and isolation amplifiers, analog circuit functions, and so forth, in digital and analog systems. A wide range of output voltage and current ratings are available; international input voltage ratings are also available.

The AC/DC supplies are available in both the PC board-mountable and chassis-mountable versions. The chassis mount type provides the same reliable performance as the PC board mount type, but the input and output connections are made on a terminal strip via screw terminals rather than pins. They are useful in applications where use of PC boards or sockets is either undesirable or impractical.

The DC/DC converters are available in small encapsulated PC board-mountable packages. They provide high input-output isolation, making them suitable in computer interface applications where, if necessary, the analog circuitry can be "floated" completely independent of digital ground. Specially designed DC/DC converters are available for use with optically-coupled isolation amplifiers and for applications where isolation voltage ratings of 3000 volts and more are required.

All Burr-Brown power supplies are extensively tested before and after encapsulation to ensure reliable operation. Computerized automatic testing equipment is used to implement stringent quality control. Years of linear and digital engineering expertise have gone into the design and manufacture of Burr-Brown products. Most of these power supplies are available from stock in both small and large quantities.

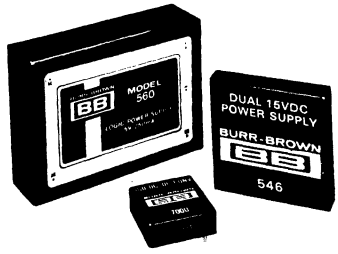
SELECTION GUIDE
Modular Power Supplies

AC/DC CONVERTERS										
Description	Model	Rated Output	Rated Input	Regulation No Load to Full Load	Regulation Overrated Line Volt.	Output(1) Ripple/Noise	Package	Price ($) Unit	Price ($) 100's	Page
Dual ±15VDC Supply P.C.B. Mount	550	±15V, ±25mA	105VAC to 125VAC, 50Hz to 400Hz (2) (3) (4)	±0.1%	±0.05%	2mV	Module	35.25	22.50	8-3
	551	±15V, ±50mA		±0.05%	±0.05%	0.5mV	Module	52.00	38.25	8-3
	552	±15V, ±100mA		±0.05%	±0.05%	0.5mV	Module	65.50	46.50	8-3
	553	±15V, ±200mA		±0.05%	±0.05%	0.5mV	Module	88.50	68.75	8-3
	554	±15V, ±350mA		±0.02%	±0.02%	0.5mV	Module	106.00	84.50	8-3
Dual ±15VDC Supply Chassis Mount	556	±15V, ±200mA	105VAC to 125VAC, 50Hz to 400Hz (2) (3) (4)	±0.05%	±0.05%	1mV	Module	75.50	59.00	8-3
	558	±15V, ±500mA		±0.05%	±0.05%	1mV	Module	107.00	83.75	8-3
5VDC Supply P.C.B. Mount	560	5V(5), ±250mA	105VAC to 125VAC, 50Hz to 400Hz (2) (3) (4)	±0.1%	±0.05%	1mV	Module	53.50	38.25	8-3
	561	5V(5), ±500mA		±0.1%	±0.05%	1mV	Module	63.25	44.00	8-3
	562	5V(5), ±1000mA		±0.1%	±0.05%	1mV	Module	86.75	63.25	8-3

DC/DC CONVERTERS									
Description	Model	Input	Output	Isolation	Leakage Current	Package	Price ($) Unit	Price ($) 100's	Page
Regulated	546	4.5VDC to 5.5VDC 400mA	Single-Bipolar ±15V, 120mA	300V	Not Specified	Module	92.00	80.25	8-3
Isolated	700	10VDC to 18VDC 89mA	±10VDC to ±18VDC (±1V tolerance) at 60mA total	1500Vp	1μA, max	Module	43.30	33.80	8-7
	700U(6)	10VDC to 18VDC 89mA	±10VDC to ±18VDC (±1V tolerance) at 60mA total	2000Vp	1μA, max	Module	39.10	28.95	8-7
	710(7)	10VDC to 18VDC 100mA	Four sets of outputs each set: ±10VDC to ±18VDC (±1V tolerance) at 76mA total all outputs	1000Vp	1μA, max	Module	52.00	37.50	8-9
	722	5VDC to 16VDC 120mA	Two-Bipolar ±15V, 64mA	3500V(8)	1μA at 240V, 60Hz	DIP	35.95/	25.95/	8-13
	722BG			8000V(9)			43.70	32.30	8-13
	724	5VDC to 16VDC 125mA	Four-Bipolar ±8V	1000V(8) 3000V(9)	1μA at 240V, 60Hz	DIP	47.40	35.00	8-17

NOTES: 1) At full load, rms (max). 2) 205VAC to 240VAC, 50Hz to 400Hz option available. 3) 90VAC to 110VAC, 50Hz to 400Hz option available. 4) 220VAC to 260VAC, 50Hz to 400Hz option available. 5) Connect as +5V or -5V. 6) Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Model 700M and 700UM are similar to Models 700/700U but, in addition, they are 100% screened to patient connected circuit requirements for the leakage current (par. 27.5) and withstand voltage (par. 31.11) of UL544. Additional charge for 700M or 700UM. See Product Data Sheet for complete specifications. 7) Model 710 provides 4 channels (sets) of isolated outputs. See Product Data Sheet for complete specifications. 8) Input to output, continuous. 9) Input to output, 5sec, minimum.

BURR-BROWN®



MODULAR AC/DC AND DC/DC POWER SUPPLIES

FEATURES

- PC BOARD-COMPATIBLE
- CHASSIS MOUNTABLE
- HIGH RELIABILITY, FULLY TESTED
- LOW INSTALLED COST
- COMPLETELY SELF-CONTAINED

DESCRIPTION

Burr-Brown standard series power supplies and DC/DC converters provide maximum flexibility in systems design. They are particularly useful for powering analog interface circuitry in digital and analog systems and have a wide range of output voltage and current ratings. They are completely self-contained, ready to use encapsulated units. For most OEM users they eliminate engineering start-up/documentation costs and manufacturing delays at prices generally far below internal manufacturing costs.

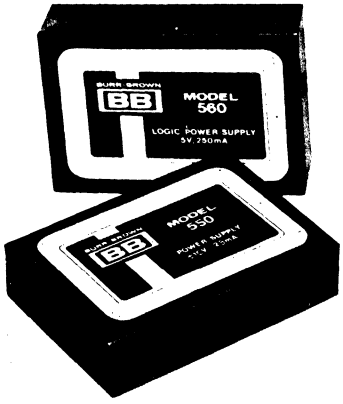
The AC/DC power supplies have a current limiting circuit in the output stage, designed to withstand output short-circuit-to-common or substantial overload conditions for long periods of time, without causing damage to the power supply.

In applications where isolation between input and output is an essential requirement (such as powering isolation amplifier input and output stages) the Burr-Brown isolated DC/DC converters provide up to 1500VDC of isolation protection.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

MODULAR AC/DC POWER SUPPLIES

- PC BOARD/CHASSIS MOUNT TYPE
- ±15VDC DUAL OUTPUTS, +5VDC SINGLE OUTPUT
- 25mA TO 1000mA CURRENT CAPABILITY
- CURRENT-LIMITED OUTPUTS FOR SHORT CIRCUIT PROTECTION
- INTERNATIONAL AC INPUT VOLTAGE OPTIONS AVAILABLE



SPECIFICATIONS COMMON TO ALL AC/DC POWER SUPPLIES

Input Voltage: 105VAC to 125VAC, 50Hz to 400Hz. For international AC input voltages see options E, F, and H.

Input Isolation: 50MΩ

Breakdown Voltage: 500V, min.

Output Voltage: Error, ±1%; temperature coefficient, ±0.02%/°C

Output Protection: Current limiting protection for output to withstand overloads and direct short circuits to ground to prevent excessive temperature within the unit.

Rated Operating Temperature: -25°C to +71°C. May be operated at higher temperatures with proper derating.

Storage Temperature: -25°C to +85°C.

DC/DC CONVERTERS, ±15VDC OUTPUT

- REGULATED ±15VDC FROM UNREGULATED DC INPUT
- DIFFERENT DC INPUT VOLTAGE RANGES AVAILABLE
- HIGH CURRENT CAPABILITY WITH CURRENT LIMIT PROTECTION
- ISOLATED DC/DC CONVERTERS, 75% EFFICIENCY AT FULL LOAD
- LOW COUPLING CAPACITANCE (8pF)
- HIGH ISOLATION VOLTAGE (1500VDC)
- LOW EMI, SHIELDED AND UNSHIELDED UNITS
- UP TO FOUR FULLY ISOLATED OUTPUT CHANNELS (Model 710)
- SMALL SIZE

AC/DC CONVERTERS

	Dual ±15VDC Supplies							5VDC Logic Supplies		
	PC Board Mount					Chassis Mount		PC Board Mount		
Model	550	551	552	553	554	556	558	560	561	562
RATED OUTPUT										
Voltage (nom)	±15V	±15V	±15V	±15V	±15V	±15V	±15V	5V[1]	5V[1][2]	5V[1][2]
Current (max)	±25mA	±50mA	±100mA	±200mA	±350mA	±200mA	±500mA	250mA	500mA	1000mA
RATED INPUT										
Voltage	105 - 125VAC, 50 - 400Hz					105 - 125VAC 50 - 400Hz		105 - 125VAC, 50 - 400Hz		
Options[3]	E, F, H					E,F,H		E, F, H		
REGULATION										
No load to full load (max)	±0.1%	±0.05%	±0.05%	±0.05%	±0.02%	±0.05%	±0.05%	±0.1%	±0.1%	±0.1%
Over rated line voltage (max)	±0.05%	±0.05%	±0.05%	±0.05%	±0.02%	±0.05%	±0.05%	±0.05%	±0.05%	±0.05%
OUTPUT RIPPLE AND NOISE										
At full load, rms (max)	2mV	0.5mV	0.5mV	0.5mV	0.5mV	1mV	1mV	1mV	1mV	1mV

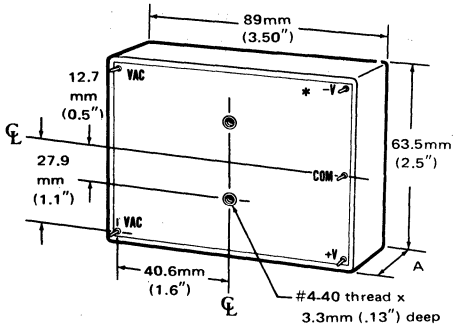
DC/DC CONVERTERS ±15VDC Output

	Low Profile	Isolated[6]	
MODEL	546	700/700U[4]	710[5]
RATED INPUT			
Voltage	4.5VDC to 5.5VDC	10VDC to 18VDC	10VDC to 18VDC
Current, Quiescent	400mA, max	20mA at ±3mA load	40mA at total output of 24mA
Current, full load	1.8A, max	89mA max at ±30mA load	100mA at total output of 76mA
RATED OUTPUT			
Voltage (no load)	±15V	$\pm V_{IN}$ w/1V tolerance	4 sets of $\pm V_{IN}$ w/1V tolerance
Current	120mA, max	total 60mA, max	total 76mA max; any single output -60mA, max
Short circuit current	180mA, max	120mA, max	120mA, max
REGULATION			
Line at full load	0.1%, max	—	—
Load, zero to full load	0.02% typ, 0.1% max	35mV/mA	75mV/mA
OUTPUT VOLTAGE TEMP COEFFICIENT	±3mV/°C	—	—
OUTPUT RIPPLE	10mV peak, typ; 20mV peak, max; 0.8mV, rms max	±15mV peak at ±3mA load; ±80mV peak, max, at ±30mA load	±25mV peak at ±3mA load; ±80mV peak; max, at ±9.5mA load
INPUT-OUTPUT ISOLATION			
Test voltage, 5sec at 60Hz		4200Vp/5000Vp	2200V, rms
Voltage, continuous, derated	300VDC	1500Vp/2000Vp	600V, rms, 1000Vp
Impedance	$10^{10}\Omega$ || 50pF	$10^{10}\Omega$ || 5pF/$10^{10}\Omega$ || 3pF	$10^{10}\Omega$ || 8pF
Leakage current at 240V/60Hz, tested		1μA, max	1μA, max
TEMPERATURE RANGE			
Operating	0°C to 71°C	-25°C to +85°C	-25°C to +85°C
Storage	-55°C to +100°C	-55°C to +125°C	-55°C to +110°C

1. The output may be connected as +5V or -5V.
2. These 5V supplies have over-voltage protection which limits the output voltage to 7V (max) in a fault condition.
3. International input voltage rating available. Specify: E option - 205VAC to 240VAC, 50Hz to 400Hz.
   F option - 90VAC to 110VAC, 50Hz to 400Hz.
   H option - 220VAC to 260VAC, 50Hz to 400Hz.
4. Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Model 700M and 700UM are similar to Models 700/700U but, in addition, they are 100% screened to patient connected circuit requirements for the leakage current (par. 27.5) and dielectric withstand voltage (par. 31.11) of UL544. See Product Data Sheet for complete specifications.
5. Model 710 provides 4 channels (sets) of isolated outputs. See Product Data Sheet for complete specifications.
6. For newer designs, the models 722 and 724 (hybrid isolated DC/DC converters) which are smaller in size and better in performance are recommended. Please refer to models 722 and 724 product data sheets.

PACKAGE DRAWINGS

DRAWING NO. 1



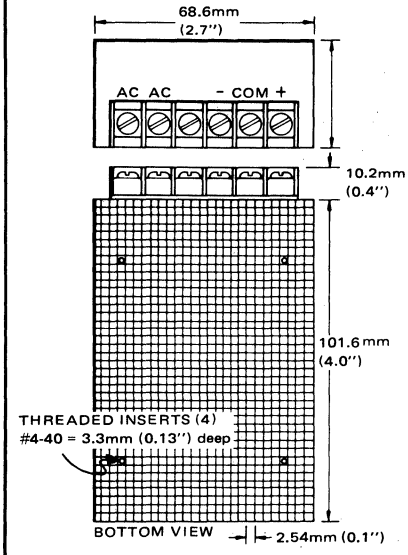
Pin Diameter 1.02mm (0.04")
* No Connection for Models 560, 561, 562.

For Models 550, 551, 560 – A = 22.2mm (0.875")
Weight: 340 grams (12 oz)

For Models 552, 553, 561, 562 – A = 32mm (1.25")
Weight: 425 grams (15 oz)

For Model 554 – A = 4.1cm (1.62")
Weight: 750 grams (26 oz)

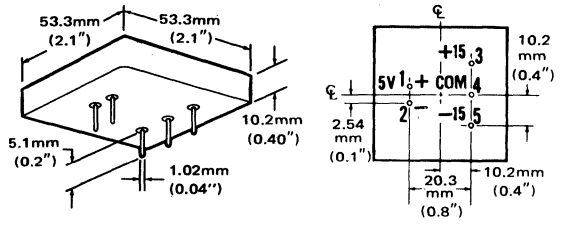
DRAWING NO. 2



For Model 556 – A = 36.6mm (1.44")

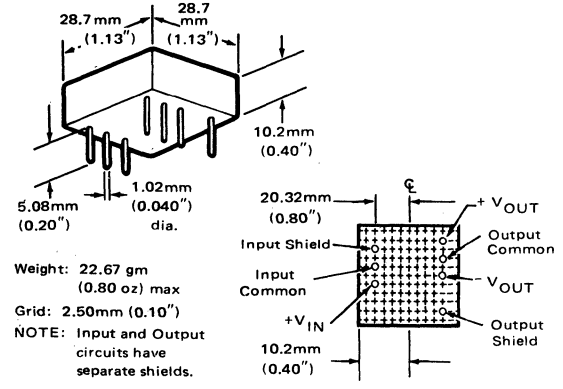
For Model 558 – A = 50.8mm (2.00")

DRAWING NO. 3 Model 546



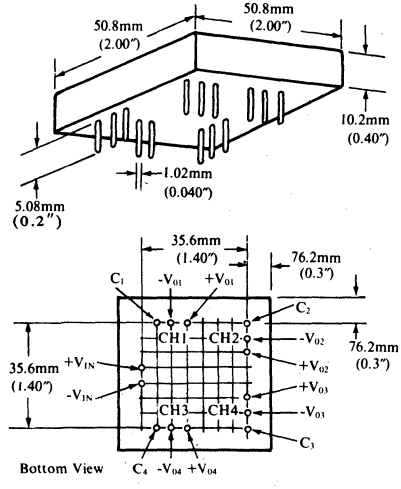
WEIGHT - 50 grams (1.7 oz)

DRAWING NO. 4 Model 700



Weight: 22.67 gm
(0.80 oz) max
Grid: 2.50mm (0.10")
NOTE: Input and Output
circuits have
separate shields.

DRAWING NO. 5 Model 710



Weight: 25 grams (0.9 oz.)
Grid: 5.08mm (.20")

BURR-BROWN®

700/700U

ISOLATED DC-TO-DC CONVERTER

FEATURES

- HIGH BREAKDOWN VOLTAGE 5000V PEAK
- LOW LEAKAGE CAPACITANCE ≅3pF
- SHIELDED AND UNSHIELDED UNITS
- COMPLETELY SPECIFIED

BENEFITS

- HIGH VOLTAGE RATING PROTECTS EXPENSIVE INSTRUMENTATION
- LOW LEAKAGE CURRENT PROTECTS HUMAN LIFE
- EXCELLENT ISOLATION CMR IMPROVES SYSTEM PERFORMANCE
- SHIELDING PREVENTS ELECTROSTATIC AND EMI PROBLEMS

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTATION
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The Model 700 converts a 10VDC to 18VDC input to a dual output of the same value as the input voltage. The internal hybrid integrated circuit reduces size and cost. A self-contained frequency stable 130kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation. Regulation and short circuit protection, if desired, can easily be added (see Figure 3). Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

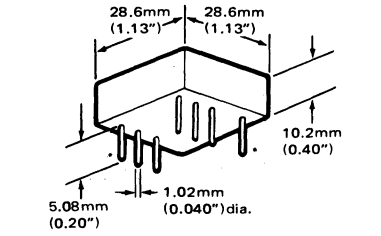
(Typical at 25°C with 15V supply unless otherwise noted.)

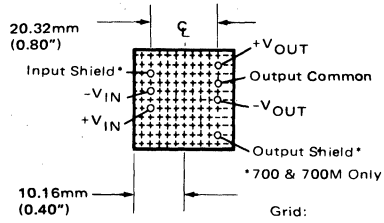
ELECTRICAL

MODEL	700/700M	700U/700UM
INPUT		
Voltage Range(1)	10V to 18V	
Current @ ±3 mA Load	20 mA	
Current @ ±30 mA Load	89 mA, max.	
Ripple Current @ ±3 mA Load	±3 mA, peak	
Ripple Current @ ±30 mA Load	±25 mA, peak	
ISOLATION(2)		
Voltage, Test, 5 sec. @ 60 Hz	4200Vp	5000Vp
Voltage, Continuous, derated	1500Vp	2000Vp
Impedance	10G Ω‖5 pF	10G Ω‖3 pF
Leakage Current @ 240V/60 Hz	1 μA, max.	1 μA, max.
OUTPUT		
V_{out} @ ±3 to ±30 mA Load	$\pm V_{in}$ with ±1V tolerance	
Operating Current total of both outputs	60 mA max.	
Safe Nondestructive Current at 25°C	120 mA max.	
Sensitivity to Input Voltage	1.08V/V	
Load Regulation	35 mV/mA	
Ripple Voltage @ ±3 mA Load	±15 mV, peak	
Ripple Voltage @ ±30 mA Load	±80 mV, peak max.	
Balance of +V and -V @ +I = -I	±20 mV	
TEMPERATURE RANGE		
Operating	-25°C to +85°C	
Storage	-55°C to +125°C	

NOTES: 1. Derate to 16V max between $+V_{in}$ and $-V_{in}$ above 70°C.
2. A medical grade unit is available which is 100% screened to Patient Connected Circuit requirements for the leakage current (par. 27.5) and dielectric withstand voltage (par. 31.11) of UL544. Specify 700M or 700UM.

MECHANICAL





Material: Black Epoxy
Weight: 22.67 gm (0.80 oz.) max
Grid: 2.50mm (0.10")
Pin: Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

NOTE: Input and Output circuits have separate shields.

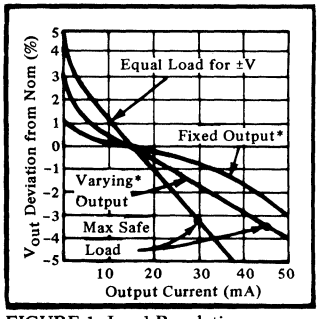


FIGURE 1. Load Regulation.

*For one output with constant 15 mA load and varying current on other output. (A minimum load of 3mA is recommended for each output).

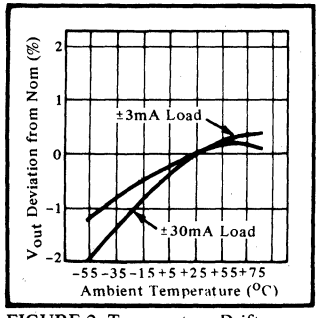


FIGURE 2. Temperature Drift.

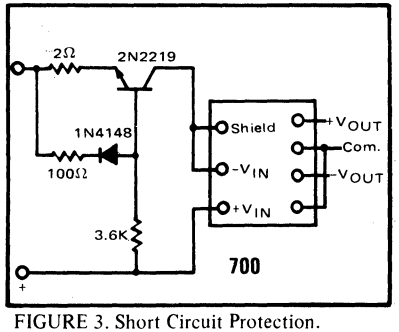


FIGURE 3. Short Circuit Protection.

Use with Isolation Amplifiers:

When the Model 700/700U is used with isolation amplifiers such as the Burr-Brown 3650 and 3652 special attention should be given to current ratings to avoid over designing. Since the isolation amplifiers do not draw max. current simultaneously from the +V and -V Model 700/700U terminals, it is possible to drive more isolation amplifiers per Model 700/700U than one might initially expect. The Model 700/700U is capable of providing a total output current of 60 mA balanced or unbalanced between the two outputs. A minimum load of 3 mA is recommended for each output.

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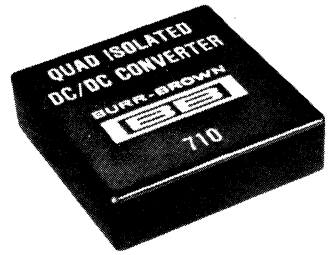

710

QUAD-ISOLATED DC-TO-DC CONVERTER

FEATURES

- FOUR ISOLATED ±10VDC to ±18VDC OUTPUTS
- DRIVES FOUR 3650/3652 ISOLATION AMPS
- HIGH BREAKDOWN VOLTAGE, 2200VDC TEST
- LOW LEAKAGE CAPACITANCE, 8pF
- LOW LEAKAGE CURRENT, 1μA @ 240V/60Hz
- LOW COST PER ISOLATED CHANNEL

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The Model 710 converts a single 10VDC to 18VDC input into four dual isolated outputs of the same value as the input voltage. The converter is capable of providing a total of 76mA at rated output voltage accuracy and can provide isolated power to four independently isolated 3650/3652 optically coupled isolation amplifiers with the entire assembly mounted on one 5" x 7" card.

Extensive use is made of hybrid integrated circuits to reduce size and cost. A self-contained frequency stable 130 kHz oscillator drives switching circuitry which is designed to minimize the common problem of spiking due to transformer saturation.

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PDS-367A

DESCRIPTION

OUTPUT CURRENT RATINGS

The Model 710 is capable of providing a total of 76mA of output current divided among its eight outputs. The maximum current available from any one output is shown in Figure 9. A minimum average current of 3mA is recommended for each output in order to maintain output voltage accuracy. Thus, the current may be balanced (such as +9.5mA and -9.5mA) or unbalanced (such as +16mA and -3mA). The best output voltage accuracy will be obtained under balanced conditions.

Channels may be connected in series or parallel for higher voltage or current. For parallel operation connection of channel 1 to 2 or channel 3 to 4 will result in lowest ripple.

In some cases the 710 may drive larger loads than would be apparent from a cursory examination of the specifications. For example, see Figures 1 and 2. The most total current drawn from the pair of $+V_o$ and $-V_o$ output is $I_{max} + I_Q$ (not 2 x I_{max}). For the 3650 this is a maximum of 12mA +1.2mA = 13.2mA (instead of 24mA).

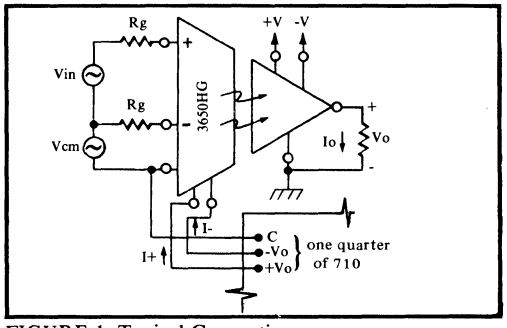


FIGURE 1. Typical Connection

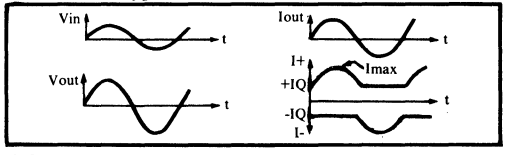


FIGURE 2. Waveforms

ISOLATION VOLTAGE RATINGS

It is important that the user understand the significance of the continuous derated isolation voltage specification and its relationship to the actual test voltage applied to the unit. Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated minimum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000$ V. This relationship is appropriate for conditions where the system transient voltages are not well defined.* Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

* Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS I-109 and ICS I-111.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 710 in order to protect it from damage in situations where too much current is demanded from the outputs – such as a short circuit from an output to its common. The circuit limits the input current to approximately 100 mA for an input voltage of 15 VDC (for β of 2N2219 of 50).

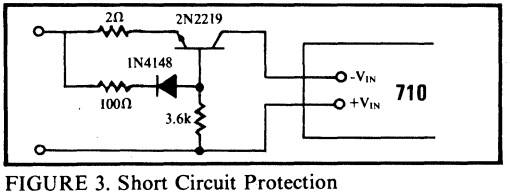


FIGURE 3. Short Circuit Protection

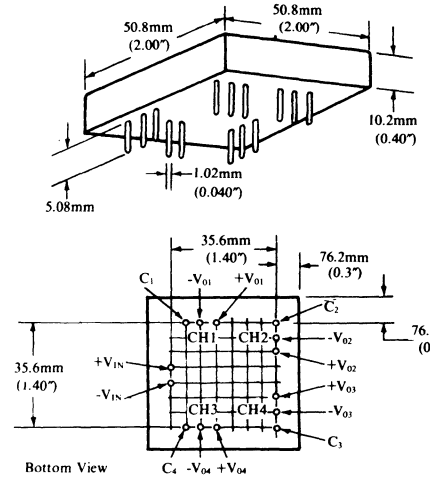
SPECIFICATIONS

Typical at 25°C with 15V supply unless otherwise noted.

ELECTRICAL

MODEL	710
INPUT	
Voltage Range[1][2]	10V to 18V
Current at Total Output Current of 24mA	40mA
Current at Total Output Current of 76mA	100mA, max.
Ripple at Total Output Current of 24mA	15mA, peak
Ripple at Total Output Current of 76mA	40mA, peak
ISOLATION[3]	
Voltage, Test, 5 sec.[4]	2200V, rms at 60Hz
Voltage, Continuous, derated, minimum[4]	600V, rms AC, 1000VDC
Impedance	10GΩ || 8pF
Leakage Current at 240V/60 Hz	1μA, max
OUTPUT	
Voltage Accuracy[5]	See Figure 8
Current for Rated Accuracy: Total of all currents	76mA, max
: Any one output	60mA, max
Total Safe Nondestructive Current at 25°C	1200mA, max
Sensitivity to Input Voltage	1.08V/V
Load Regulation[6]	75mV/mA
Ripple Voltage at ±3mA Load	±25mV, peak
Ripple Voltage at ±9.5mA Load	±80mV, peak max
Balance of +V and -V at +I = -I	±20mV
ΔV_{out} vs Temperature -25°C to +85°C	3.0%
TEMPERATURE RANGE	
Operating	-25°C to +85°C
Storage	-55°C to +110°C

MECHANICAL



Material: Black Epoxy
Weight: 25 grams (0.9 oz.)
Grid: 5.08mm (.20")
Pin: Material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

NOTES:
1. Derate to 16V max between $+V_{IN}$ and $-V_{IN}$ above 70°C.
2. Operation down to 5V is possible with reduced output current and accuracy.
3. Isolation specifications are applicable to input to output isolation as well as channel to channel isolation.
4. See discussion on previous page; 2200V, rms = 3000V peak.
5. A minimum output current of ±3mA per channel is recommended to maintain output voltage accuracy.
6. Load regulation for one channel with other channels at ±9.5mA load.

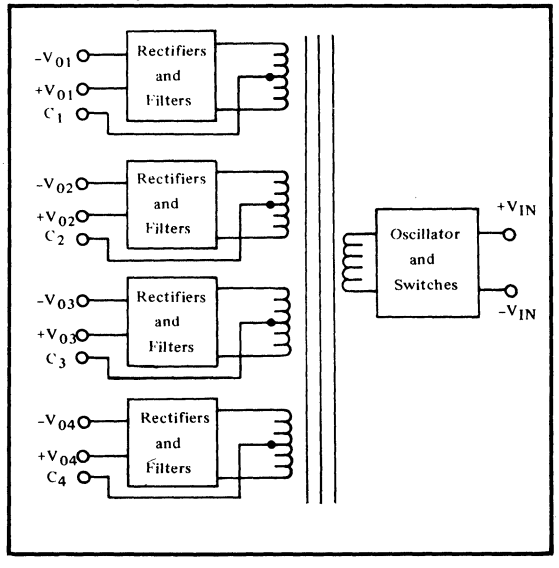


FIGURE 4. Functional Diagram

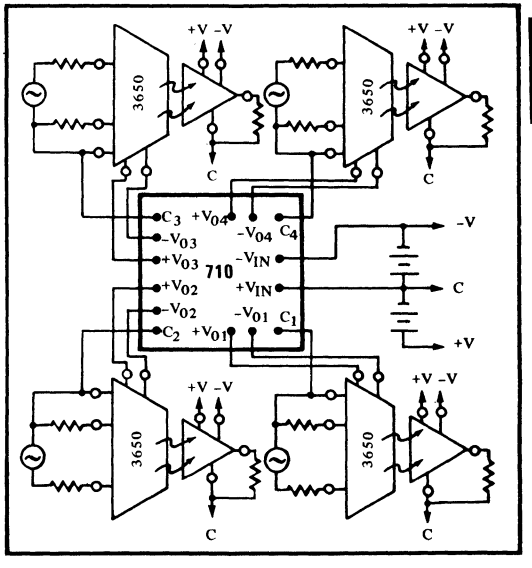


FIGURE 5. Typical Connection with Four 3650 Isolation Amplifiers.

TYPICAL PERFORMANCE CURVES

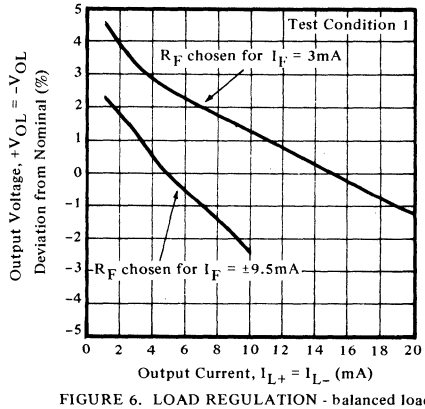


FIGURE 6. LOAD REGULATION - balanced load

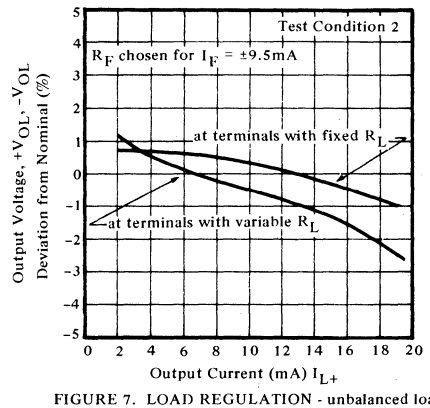


FIGURE 7. LOAD REGULATION - unbalanced load

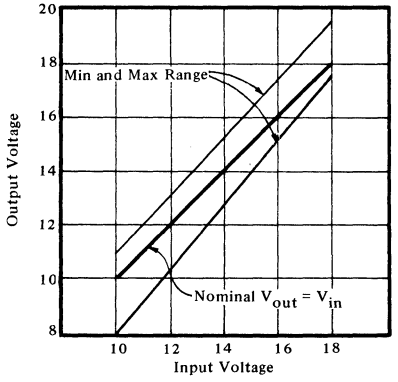


FIGURE 8. OUTPUT VOLTAGE ACCURACY VS INPUT VOLTAGE

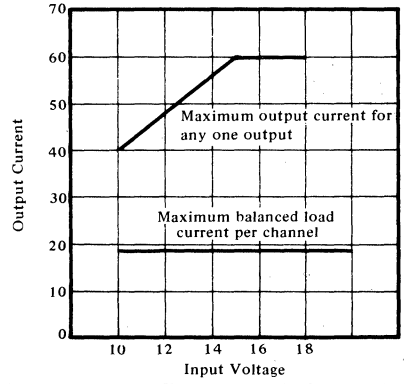


FIGURE 9. OUTPUT CURRENT RATINGS TO MAINTAIN OUTPUT VOLTAGE TOLERANCE

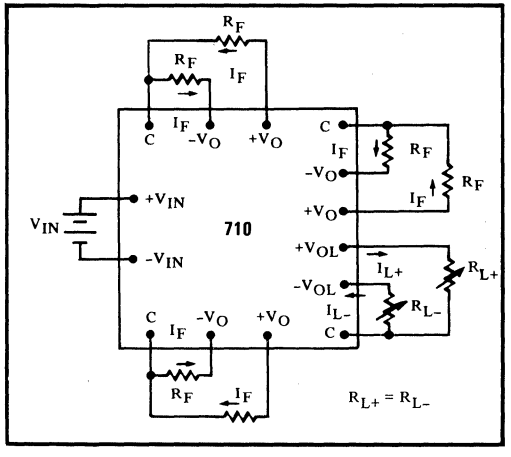


FIGURE 10. Test Condition 1: Balanced Load

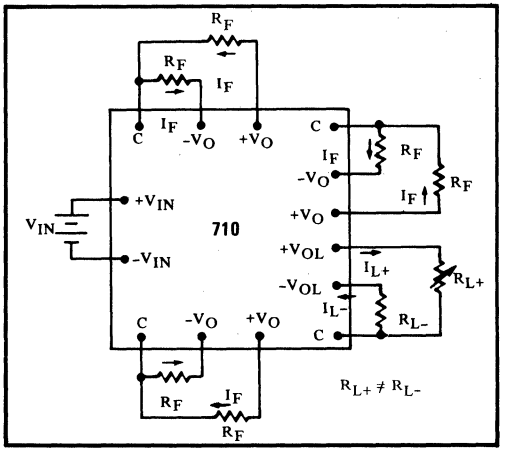


FIGURE 11. Test Condition 2: Unbalanced Load

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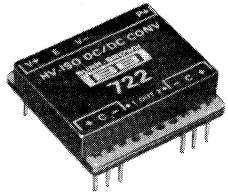
722



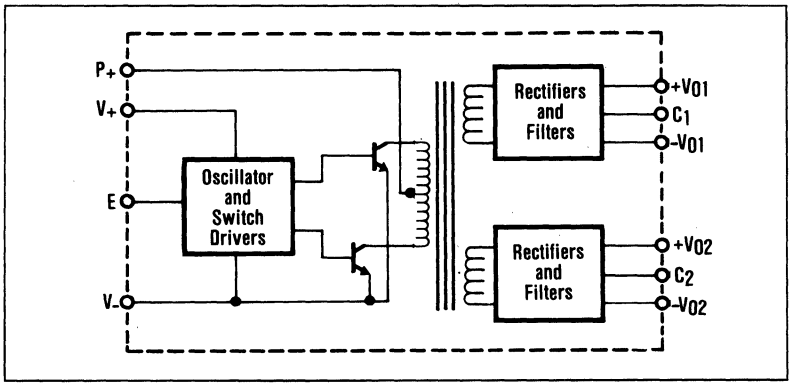
DUAL ISOLATED DC/DC CONVERTER

FEATURES

- DUAL ISOLATED ±5 TO ±16V OUTPUTS
- HIGH BREAKDOWN VOLTAGE, 8000V TEST
- LOW LEAKAGE CURRENT, <1μA AT 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE, 27.9mm x 27.9mm x 7.6mm (1.1" x 1.1" x 0.3")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION



DESCRIPTION

The 722 converts a single 5VDC to 16VDC input into a pair of bipolar output voltages of the same value as the input voltage. The converter is capable of providing a total output current of 64mA at rated voltage accuracy and up to 250mA without damage.

The two output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage or in parallel for higher output current, as a single channel isolated DC/DC converter.

Integrated circuit construction of the 722 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 900kHz oscillator drives switching circuitry which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.

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DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 722 is capable of providing 64mA divided among its four outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

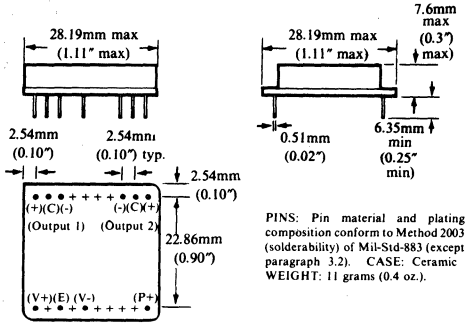
The fact that the two outputs of the 722 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows Burr-Brown's 3650 Optically Coupled Isolation Amplifier connected in three-port configuration. One of the 722 channels provides power to the 3650's input. The other channel supplies power to the 3650's output. The amplifier's input and output are isolated from each other and the system's power supply common. In this configuration the 722's channel-to-channel isolation specification applies to the amplifier input-to-output voltage.

Figure 3 illustrates how the 722 may provide isolated input power to the input stage of two 3650's connected in the two-port configuration. Power for the output stage is provided by the system +15V and -15V supplies. Input stages are isolated from each other and from the system supply. In this situation the 722's input-to-output isolation specification applies to the amplifiers' input-to-output voltages while the channel-to-channel 722 specification applies to the voltage existing between "I/P Com # 1" and "I/P Com # 2."

(1) "output" denotes a single output terminal (+V or -V) and its associated common
(2) "channel" denotes a pair of outputs (+V and -V) and their associated common

MECHANICAL



SHORT CIRCUIT PROTECTION

The circuit in Figure 2 may be added to the input of the 722 to protect it from damage in situations where too much current is demanded from the outputs - such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

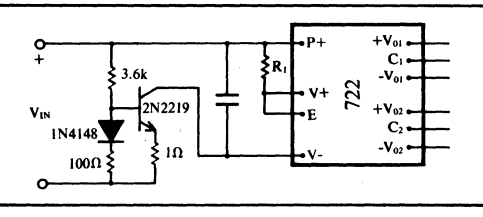


FIGURE 2. Short Circuit Protection

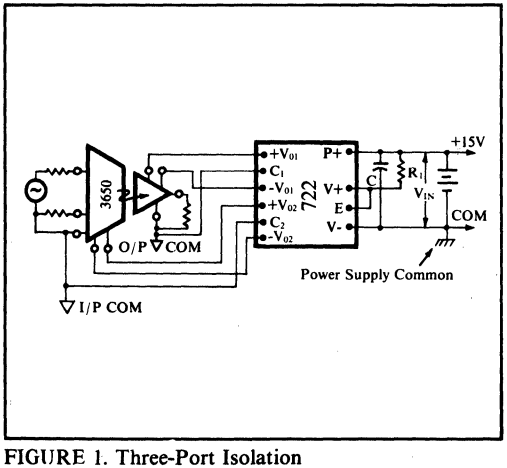


FIGURE 1. Three-Port Isolation

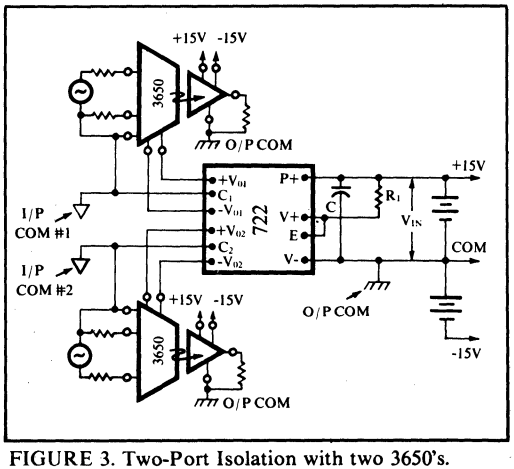


FIGURE 3. Two-Port Isolation with two 3650's.

ELECTRICAL SPECIFICATIONS

Specifications at T_A = +25°C, V_{IN} = 15VDC, C = 0.47μF, R_1 Selected per Typical Performance Curve.

PARAMETER	CONDITIONS	722			722BG			722MG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
Rated Input Voltage			15								VDC
Input Voltage Range[1]		5		16							VDC
Input Current	Total output current = 12mA		50								mA
	Total output current = 64mA		105	120							mA
	Total output current = 64mA at T_A = +85°C		120								mA
	Total output current = 160mA		-	-		225	275		-	-	mA
Input Ripple[2]	Total output current = 12mA		3								mA, pk
	Total output current = 64mA		6								mA, pk
	Total output current = 160mA		-			12					mA, pk
ISOLATION											
Test Voltages[3]	Input-to-output, 5 seconds, min			8000							V, pk
	Input-to-output, 1 minute, min			-			-			2500	V, rms
	Channel-to-channel, 5 seconds, min			5000							V, pk
Rated Voltage[3]	Input-to-output, continuous			3500							V
	Channel-to-channel, continuous			2000							V
Isolation Impedance	Input-to-output		10||6								GΩ||pF
Leakage Current[4]	Input-to-output, 240V, 60Hz			1							μA
OUTPUT											
Rated Output Voltage[5]	I_{Load} = 3mA per output	15.4		16.0							VDC
	I_{Load} = 16mA per output	14.3		15.3							VDC
	I_{Load} = 40mA per output	-	-	-	13.7	14.2	15.0	-	-	-	VDC
Output Current	Total of all outputs			200							mA
	Any one output[6]	3		100							mA
Load Regulation			Note 5								
Ripple Voltage	I_{Load} = 3mA per output		15								mV, pk
	I_{Load} = 16mA per output		35	100							mV, pk
	I_{Load} = 40mA per output		-			50					mV, pk
Tracking Error Between Dual Outputs	Balanced loads		±100								mVDC
Sensitivity to Input Voltage Changes			1.13								V/V
Output Voltage Temperature Coefficient	$T_A = T_{Specification\ Range}$		±0.02								%/°C
TEMPERATURE											
Specification	$I_{Load} \leq$ 16mA per output	-25		+85							°C
	$I_{Load} \leq$ 40mA per output	-25		+60							°C
Storage		-55		+125							°C
Junction Temperature				+125							°C

*Specifications same as 722.

NOTES:
1. For ambient temperature above 70°C the input voltage is 12.5V max. The input voltage remains 16V max if case temperature is kept below 85°C.
2. External capacitor across "P+" to "V-" pins and 12" of #24 wire to V_{IN}.
3. See "Isolation Voltage Ratings" on page 2 of data sheet.
4. Reference UL544, paragraph 27.5, Leakage Current.
5. See "Typical Performance Curves".
6. A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.

INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 722 are shown in Figures 1 and 3. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-"; the only requirement is that "P+" and "V+" must be positive with respect to "V-."

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor R_1. The value of R_1 as a function of V_{IN} is shown in the TYPICAL PERFORMANCE CURVES section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5V to +7.5V positive with respect to "V-". If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to V- at all times (including transients). If necessary, diode clamps should be put across these inputs.

The "E" pin enables the converter when connected to "V+" and disables it when connected to "V-."

An external capacitor, "C", (0.47μF ceramic) is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 722 is not internally shielded, external shielding may be appropriate in applications where RFI at the 900kHz nominal oscillator frequency is a problem. A shield, model 100MS, is available.

Each output is filtered with an internal 0.22μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

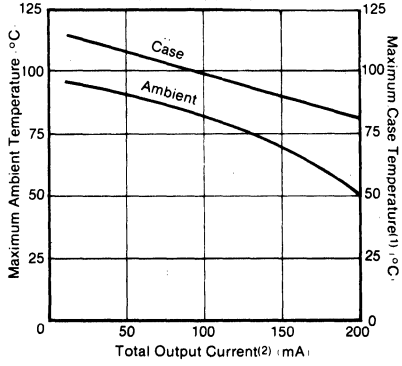
TYPICAL PERFORMANCE CURVES

Specifications at T_A = +25°C, V_{IN} = 15VDC, C = 0.47µF, R_1 selected per typical performance curve.

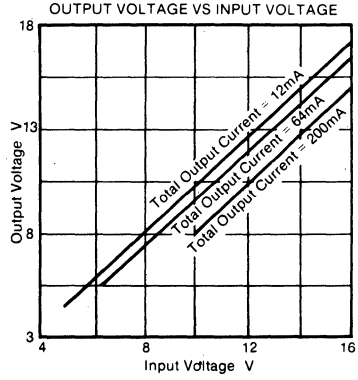
SELECTION OF R_1 OR EXTERNAL VOLTAGE V+ FOR MINIMUM INTERNAL POWER DISSIPATION

		Maximum Output Current From Any Single Output		
		<16mA	16mA to 30mA	>30mA
Input Voltage V	>13	1.3kΩ	820Ω	510Ω
	11 to 13	820Ω	510Ω	200Ω
	9 to 11	510Ω	200Ω	0Ω
	8 to 9	200Ω	0Ω	-
	<8	0Ω	-	-
→ V+EXT		6.5V	7.5V	9.0V

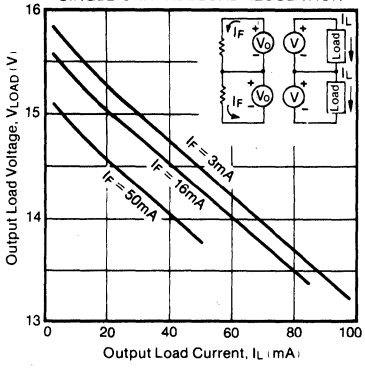
MAXIMUM SAFE OPERATING TEMPERATURE VS TOTAL OUTPUT CURRENT



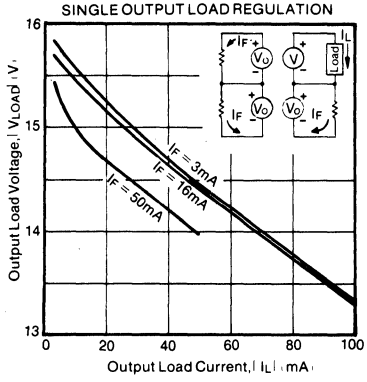
OUTPUT VOLTAGE VS INPUT VOLTAGE



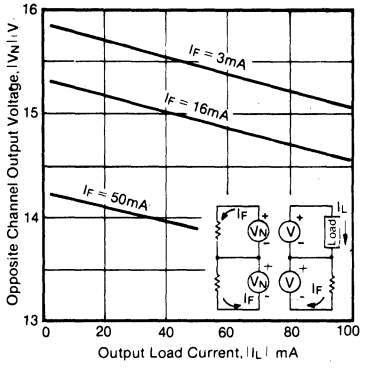
SINGLE-CHANNEL LOAD REGULATION



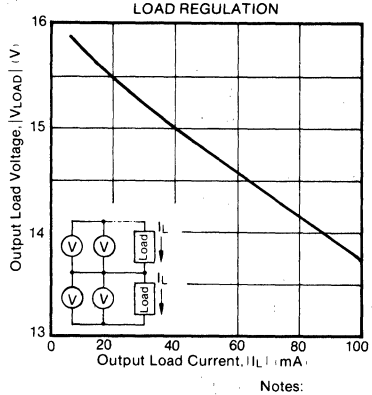
SINGLE OUTPUT LOAD REGULATION



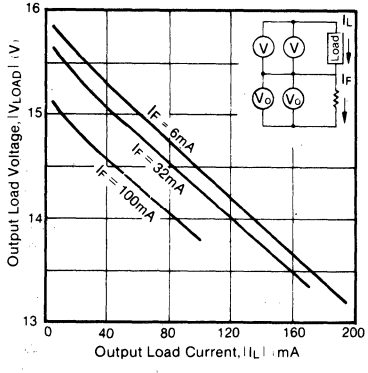
CHANNEL-TO-CHANNEL INTERACTION



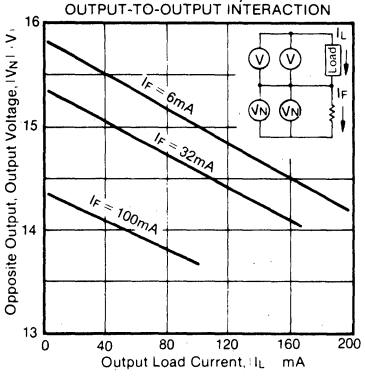
PARALLEL OUTPUT BALANCED LOAD REGULATION



PARALLEL OUTPUT UNBALANCED LOAD REGULATION



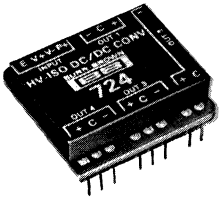
OUTPUT-TO-OUTPUT INTERACTION



Notes:
(1) Using a 104mm x 19mm x 1.6mm aluminum strip mounted to the bottom of the case with heat sink compound.
(2) Total output current is the sum of the currents for each individual output.

BURR-BROWN®

724



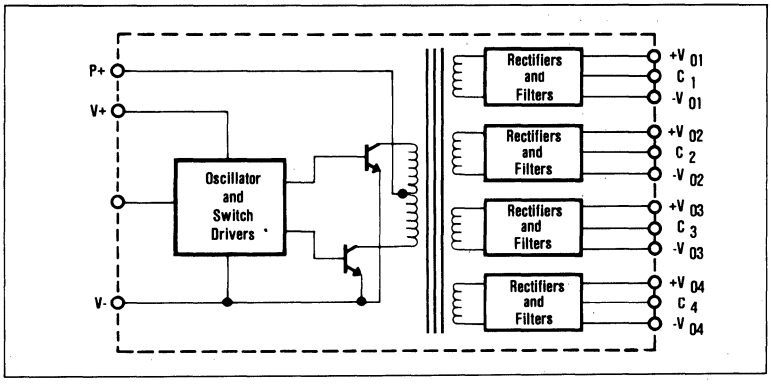
QUAD ISOLATED DC/DC CONVERTER

FEATURES

- QUAD ISOLATED ±8V OUTPUTS
- HIGH BREAKDOWN VOLTAGE, 3000V TEST
- LOW LEAKAGE CURRENT, <1μA AT 240V/60Hz
- LOW COST PER ISOLATED CHANNEL
- SMALL SIZE, 27.9mm x 27.9mm x 6.6mm (1.1" x 1.1" x 0.26")

APPLICATIONS

- MEDICAL EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- TEST EQUIPMENT
- DATA ACQUISITION SYSTEMS
- NUCLEAR INSTRUMENTATION



DESCRIPTION

The 724 converts a single 5VDC to 16VDC input into four pairs of bipolar output voltages of approximately half the input voltage. The converter is capable of providing a total output current of 128mA at rated voltage accuracy and up to 500mA without damage.

The four output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage, or in parallel for higher output current as a single channel isolated DC/DC converter.

Integrated circuit construction of the 724 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction which includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 800kHz oscillator drives switching circuitry which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.

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DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 724 is capable of providing 128mA divided among its eight outputs[1]. A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels[2] may be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the four outputs of the 724 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows two of Burr-Brown's 3650 Optically Coupled Isolation Amplifiers connected in three-port configuration. Two of the 724 channels provide power to the 3650's inputs. The other channels supply power to both 3650's outputs. Each amplifier's input and output are isolated from each other and the system's power supply common. Isolation specification applies to the amplifier input-to-output voltage isolation specification.

Figure 2 illustrates how the 724 may provide isolated input power to the input stage of four 3650's connected in the two-port configuration. Power for the four output stages is provided by the system +15VDC and -15VDC supplies. Input stages are isolated from each other and from the system supply. In this situation the 724's isolation specification applies to the amplifier's input-to-output voltage and to the voltage existing between any two I/P COM terminals.

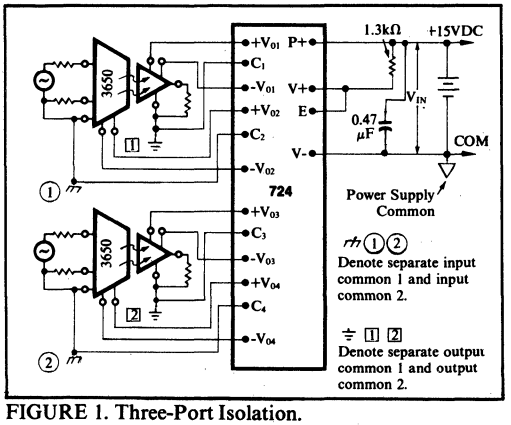


FIGURE 1. Three-Port Isolation.

ISOLATION VOLTAGE RATINGS

Since a "continuous" test is impractical in a product manufacturing situation (implies infinite test duration) it is generally accepted practice to perform a production test at a higher voltage (i.e., higher than the continuous rating) for some shorter length of time.

The important consideration is then "what is the relationship between actual test conditions and the continuous derated maximum specification?" There are several rules of thumb used throughout the industry to establish this relationship. Burr-Brown has chosen a very conservative one: $V_{test} = (2 \times V_{continuous\ rating}) + 1000V$. This relationship is appropriate for conditions where the system transient voltages are not well defined.[3] Where the real voltages are well defined or where the isolation voltage is not continuous the user may choose to use a less conservative derating to establish a specification from the test voltage.

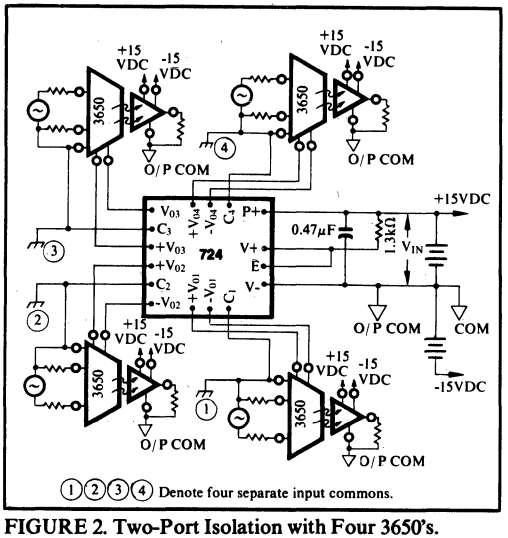


FIGURE 2. Two-Port Isolation with Four 3650's.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 724 to protect it from damage in situations where too much current is demanded from the outputs - such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for β of 2N2219 of 50).

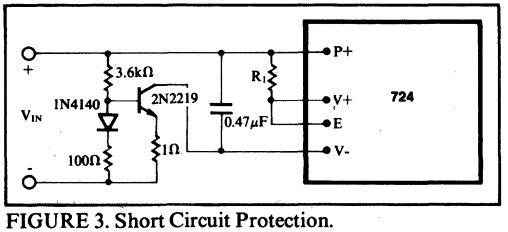


FIGURE 3. Short Circuit Protection.

(1) "output" denotes a single output terminal (+V or -V) and its associated common
(2) "channel" denotes a pair of outputs (+V and -V) and their associated common
(3) Reference National Electrical Manufacturers Association (NEMA) Standards Parts ICS 1-109 and ICS 1-111.

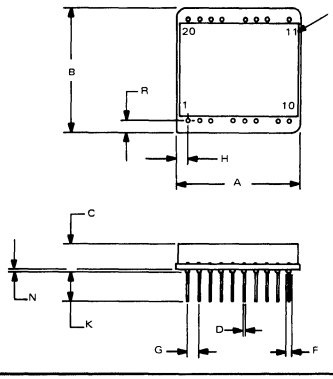
ELECTRICAL SPECIFICATIONS

At 25°C with V_{IN} = 15V, R_L = 1.3kΩ, C = 0.47μF unless noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT					
Input Voltage		5	15	16	VDC
Input Current	Σ I_{OUT} = 24mA		50		mA
	Σ I_{OUT} = 128mA, 25°C		110	125	mA
	Σ I_{OUT} = 128mA, 85°C		120		mA
Input Ripple[1][5]	Σ I_{OUT} = 24mA, C = 0.47μF		10		mA, pk
	Σ I_{OUT} = 128mA, C = 0.47μF			25	mA, pk
ISOLATION					
Test Voltage[2]	Input-to-output, 5sec min			3000	VDC
	Channel-to-channel, 5sec min			3000	VDC
Rated Voltage[2]	Input-to-output, continuous			1000	VDC
	Channel-to-channel, continuous			1000	VDC
Isolation Impedance	Input-to-output		10 || 6		GΩ || pF
Leakage Current	Input-to-output, 240V/60Hz			1.0	μA
OUTPUT					
Voltage[3]	At 15V input I_L = 3mA	8.0	8.5	9.0	V
	I_L = 16mA	7.5	7.9	8.3	V
Current for Rated Voltage	Total of all outputs			128	mA
	Any one output[4]	3			mA
Total Safe Nondestructive Current	Total of all outputs			500	mA
	Any one output			200	mA
Load Regulation[3]			Note 4		
Ripple Voltage[5]	I_L = 3mA		35		mV, pk
	I_L = 16mA			200	mV, pk
Difference of $+V_0$ and $-V_0$	$+I_L = -I_L$		±30		mV
Sensitivity to Input Voltage Change			0.63		V/V
Output Voltage Change Over Temperature	-25°C to +85°C		2		%
TEMPERATURE RANGE					
Operating		-25		+85	°C
Storage		-55		+125	°C

NOTES:
1. 0.47μF external capacitor across "P+" to "V-" pins and 12" of # 24 wire to V_{IN}.
2. See "Isolation Voltage Ratings" on preceding page. The input to output and channel to channel continuous AC rating is 700V, rms.
3. See "Typical Performance Curves."
4. A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.
5. Test bandwidth 10MHz, max.

MECHANICAL



Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.080	1.120	27.43	28.45
B	1.080	1.120	27.43	28.45
C	.235	.285	5.97	7.24
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.350	3.81	8.89
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.100 BASIC		2.54 BASIC	

NOTE:
Leads in true position within .010" (.25mm) R at MMC at seating plane.

PIN POSITION	PIN DESIGNATION
1	$+V_{04}$
2	C_4
3	$-V_{04}$
4	No pin present
5	$+V_{03}$
6	C_3
7	$-V_{03}$
8	No pin present
9	$+V_{02}$
10	C_2
11	$-V_{02}$
12	No pin present
13	$+V_{01}$
14	C_1
15	$-V_{01}$
16	No pin present
17	P+
18	V-
19	V+
20	E

INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 724 are shown in Figures 1 and 2. Primary power (V_{IN}) is applied at the "P+" and "V-" terminals. The common or ground for V_{IN} may be connected to either "P+" or "V-"; the only requirement is that "P+" and "V+" must be positive with respect to "V-."

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor R_1. The value of R_1 as a function of V_{IN} is shown in the "Typical Performance Curves" section. Alternately, voltage for the "V+" terminal may be obtained from a separate source. "V+" should be +5VDC to +7.5VDC positive with respect to "V-." If a separate source is used, the V+ input must be applied before the "P+" input to avoid possible damage to the unit. P+ and V+ must remain positive with respect to V- at all times (including transients). If necessary, diode clamps should be put across these inputs.

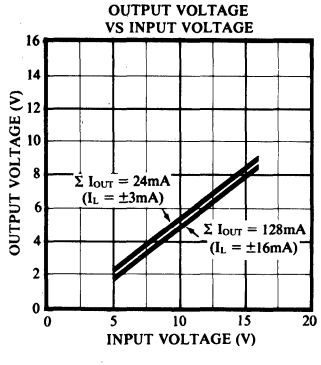
The "E" pin enables the converter when connected to "V+" and disables it when connected to "V-."

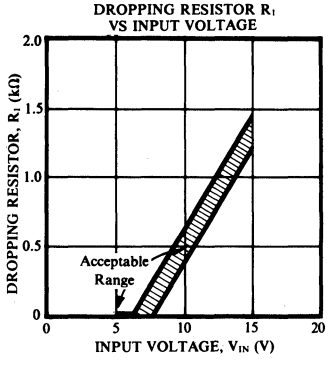
An external capacitor, "C", (0.47μF ceramic) is used to reduce input ripple. It should be connected as close to the "P+" and "V-" pins as practical. Input leads to these terminals should also be kept as short as possible. Since the 724 is not internally shielded, external shielding may be appropriate in applications where RFI at the 800kHz nominal oscillator frequency is a problem. A shield, model 100MS, is available.

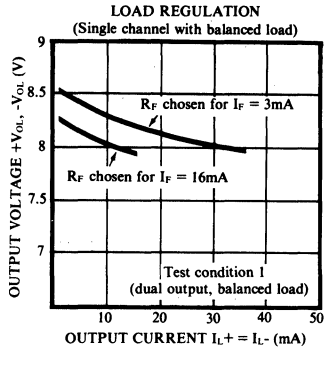
Each output is filtered with an internal 0.047μF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10μF between each output and its common.

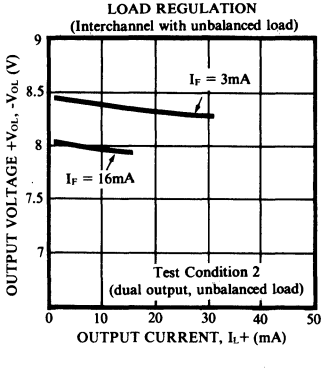
TYPICAL PERFORMANCE CURVES

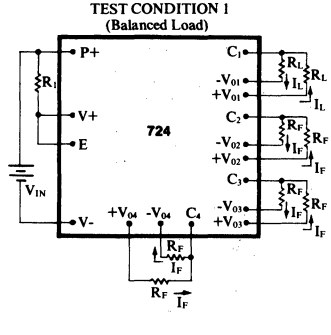
All specifications typical at 25°C unless otherwise noted.

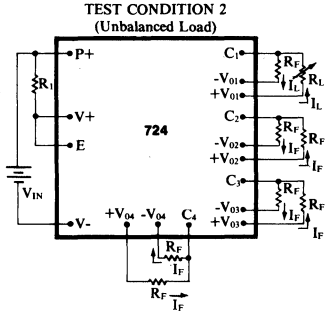












DATA ENTRY AND DISPLAY TERMINALS

MICROTERMINAL

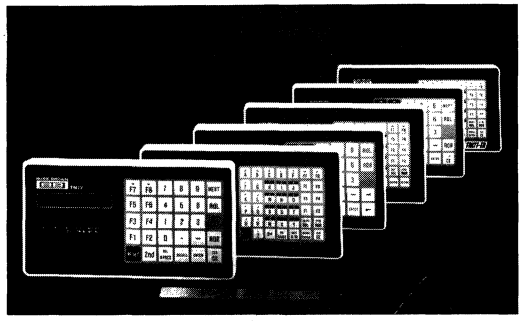
If your system's data entry/control/display requirements are sophisticated, but limited in volume you don't need to buy big, expensive and fragile CRT's or printing terminals to do the job efficiently.

"Microterminals" - uniquely flexible in application versatility - are designed expressly to fill the human interface demands of widely dispersed control and communications networks - in machine and process control, energy management systems, inventory control and factory floor data collection and information processing systems. Microterminals, because of their interface flexibility, appearance, size, durability and easy installation, function equally well as consoles and control centers for instruments and small systems. They also perform as I/O terminals in diagnostic applications.

Data may be entered through the standard keyboard as well as through integral bar code and magnatic stripe readers.

Tough, water-resistant front panel protects LED displays and indicators as well as keyboard. Tactile feedback confirms operator entry.

Buffered data features reduce on-line input/output time with the CPU and improve accuracy of operator



inputs. Because of its design simplicity, the Microterminal concept doesn't require special operator skills or training. Depressing a single function key initiates complex preprogrammed action by the CPU. These functions are defined in your CPU's software.

Microterminals' very compact design and simple mounting on any flat surface make them quickly adaptable to new or existing applications. They measure only 216mm x 114mm x 15mm (8.5" x 4.5" x 0.6"). When ordered in OEM quantities the front panel can contain your corporate or system logo.

	MICROTERMINAL									
	TM71(1)(2)	TM71B	TM71-I/O	TM70	TM77(1)	TM77B	TM77-I/O	TM76	TM25	TM27
	High Speed	Bar Code Reader	Digital I/O	Low Cost Alpha	Simple Keyboard	Bar Code Reader	Digital I/O	Simple Keyboard	Low Cost	Low Cost Polled
Display: Type	Alpha-numeric	Alpha-numeric	Alpha-numeric	Alpha-numeric	Alpha-numeric	Alpha-numeric	Alpha-numeric	Alpha-numeric	Numeric/ Hex	Numeric/ Hex
Display: Number of Characters	16	16	16	12	16	16	16	12	8	8
Display: Input Buffer Size (characters)	80	5x50	80	36	80	5x50	80	36	8	8
Display: Character Height	0.14"	0.14"	0.14"	0.14"	0.14"	0.14"	0.14"	0.14"	0.3"	0.3"
Display: LED Indicators	2	2	10	2	2	2	10	2	7	5
Display: LED Status Indicators	4	4	4	3	3	3	3	1	0	1
Keyboard: Type	Alpha-numeric	Alpha-numeric	Alpha-numeric	Alpha-numeric	Numeric	Numeric	Numeric	Numeric	Numeric/ Hex	Numeric/ Hex
Keyboard: Number of Characters	80	80	80	80	10	10	10	10	10/16	16
Keyboard: Function Keys	14	16	14	8	14	16	14	8	7	6
Bar Code Reader	No	Yes	No	No	No	Yes	No	No	No	No
Digital Inputs	No	Yes	Yes	No	No	Yes	Yes	No	No	Yes
Digital Outputs	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
RS-232-C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
RS-422	No	Yes	No	No	No	Yes	No	No	No	Yes
20mA Current Loop	Yes	No	Yes	Yes	Yes	No	Yes	Yes	Yes	No
Baud Rate	110-19200	110-19200	110-19200	300 & 1200	110-19200	110-19200	110-19200	300 & 1200	300	300-4800
Non-polled	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Polled	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes(3)	Yes
User EPROM	Yes	No	Yes	No	Yes	No	Yes	No	No	No
Power Supply	+5VDC 650mA	+24VAC/DC 400mA	+5VDC 850mA	+5VDC 500mA	+5VDC 650mA	+24VAC/DC 400mA	+5VDC 850mA	+5VDC 500mA	+15VDC 250mA	+8 to +12VDC 400mA
Price: 1-9 quantity	$595.00	$1495.00	$695.00	$450.00	$595.00	$1495.00	$695.00	$450.00	$249.00	$250.00
100-249 quantity	$385.00	--	$450.00	$290.00	$385.00	--	$450.00	$290.00	$182.00	167.00
Page	9-42	9-60	9-42	9-27	9-42	9-60	9-42	9-27	9-5	9-19

NOTES: 1) TM71MS and TM77MS include an integral magnetic stripe reader. Request prices. 2) TM71M meets Hi-Rel environmental specifications, -55°C to +65°C temp range. 3) TM25 Multidrop: 1-9 quantity - $325.00; 100-249 quantity - $237.00.

DTP-05
POWERED DESK-TOP STAND

BURR-BROWN®

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

DESCRIPTION

The DTP-05 is a desk-top stand for use with Burr-Brown's line of microterminals. It may be used with the TM70, TM71, TM76, TM77, TM71-I/O, and TM77-I/O. The DTP-05 provides +5VDC power at 1A. Also included are switches to control microterminal option selections, such as baud rate, parity, and polling address. Two versions are available, the DTP-05 with 110VAC input and the DTP-05E with 220 VAC input.

MICROTERMINAL MOUNTING INSTRUCTIONS

Microterminals may be bolted to the DTP-05 by following the assembly procedures below:

1. Unplug power cord. High voltages are present on the internal circuit board even with power switch off.
2. Remove the four bolts accessible from sides of the unit.
3. After separating the unit into two halves, carefullly remove the six screws and washers which hold the circuit board to the top of the enclosure.
4. Remove the six nuts that retain the standoffs on the top portion of the enclosure and discard the nuts.
5. Place the microterminal face down on a flat surface and position the top of the enclosure on the back of the microterminal, lining up the holes in the top of the enclosure with the mounting holes in the microterminal.
6. Connect the top of the enclosure to the microterminal by screwing the standoffs through the top of the enclosure into the mounting holes on the microterminal. A star washer should be installed between the standoff and the top of the enclosure. Do not over tighten.
7. Replace the circuit board with the six retaining screws and washers. Reconnect and secure the top and bottom sections of the enclosure as described above.

OPTION SWITCHES

Option switches on the DTP-05 are used to select between groups of microterminals and to select parity, baud rate, and polling address. As shipped, these units are set up for 300 baud, mark parity, nonpolled, with the front panel reset enabled and set for the TM71/TM77 family. The option switches are accessible through an opening in the bottom of the enclosure. The switch markings are silkscreened on the printed circuit board. The dual-in-line option switches are marked either "on" or "closed" to indicate that the switch is shorted. The table below refers to closed as the shorted configuration.

OPTION SWITCH	LOGIC 1	LOGIC 0
P0	Open	Closed
P1	Open	Closed
B0	Open	Closed
B1	Open	Closed
B2	Open	Closed
$\overline{A0}$	Closed	Open
$\overline{A1}$	Closed	Open
$\overline{A2}$	Closed	Open
$\overline{A3}$	Closed	Open

Two switches are used to select between the TM70/TM76 and the TM71/TM77 family. These switches are labeled GND (switch S2-3) and EN (switch S2-4). The table below shows how these switches are configured to select between microterminal families.

FAMILY	MODEL	GND	EN
TM71 Family	TM71	Closed	Open
	TM77	Closed	Open
	TM71-I/O	Closed	Open
	TM77-I/O	Closed	Open
TM70 Family	TM70	Open	Closed
	TM76	Open	Closed

The front panel RESET key of the microterminal is enabled by the switch marked R1 and R0 (S2-1). In the closed position the RESET key is enabled; in the open position the RESET key is disabled.

OPTION SELECTION

The tables below show the switch position needed to select options: The TM71 family includes the TM71, TM71-I/O, TM77, and TM77-I/O. The TM70 family includes the TM70 and TM76.

Option Switch Positions for TM71 Family

TM71 PARITY BIT	P1	P0
Space	Closed	Open
Even	Closed	Closed
Odd	Open	Closed
Mark	Open	Open

TM71 BAUD RATE	B2	B1	B0
300	Open	Open	Open
600	Open	Open	Closed
1200	Open	Closed	Open
2400	Open	Closed	Closed
4800	Closed	Open	Open
9600	Closed	Open	Closed
19200	Closed	Closed	Open
110	Closed	Closed	Closed

TM71 ADDRESS	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$
0 (0000)	Open	Open	Open	Open (nonpolled)
1 (0001)	Open	Open	Open	Closed
2 (0010)	Open	Open	Closed	Open
3 (0011)	Open	Open	Closed	Closed
• •	•	•	•	•
• •	•	•	•	•
• •	•	•	•	•
15 (1111)	Closed	Closed	Closed	Closed

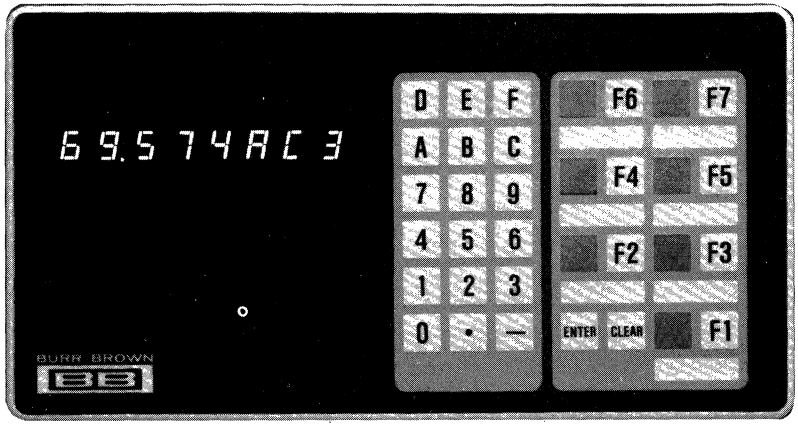
Option Switch Positions for TM70 Family

TM70 PARITY BIT	P1	P0
Even	Closed	Closed
Odd	Closed	Open
Space	Open	Closed
Mark	Open	Open

TM70 BAUD RATE	B0	B1	B2
300	Open	Not Used	
1200	Closed		

TM70 ADDRESS	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$
0 (0000)	Open	Open	Open	Open (nonpolled)
1 (0001)	Open	Open	Open	Closed
2 (0010)	Open	Open	Closed	Open
3 (0011)	Open	Open	Closed	Closed
• •	•	•	•	•
• •	•	•	•	•
• •	•	•	•	•
15 (1111)	Closed	Closed	Closed	Closed

TM25
USER'S GUIDE



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PDS-426B

TABLE OF CONTENTS

DESCRIPTION

The TM25 is a small, low cost, industrial quality computer terminal. It is available with an 8-digit hexadecimal display and with either a numeric or hexadecimal keyboard. It also contains seven function keys and seven function lights. The TM25 serial computer interface transmits and receives ASCII characters using 20mA current loop or RS232C/V.24 transmission standards. Information is transmitted at 300 baud.

The TM25 communications protocol is available in single-drop and multidrop versions. In the single-drop version, one TM25 is connected to one communications interface. In the multidrop version, a number of TM25's can be connected to one communications interface. The single-drop version is described beginning on this page. The multidrop version is described beginning on page 6.

The function keys and lights of the TM25 were designed to let the TM25 be easily customized to a specific application. When a function key is depressed, the adjacent function light is lit. Any number of function keys may be depressed. When data is transmitted from the TM25, the status of the function light is encoded in two ASCII characters. Likewise, any function light may be turned on or off by command from the serial interface.

The function lights allow the computer to send messages and direct the action of the terminal user. The function keys allow the user to transmit specific information to the computer, thus considerably extending the versatility of the TM25.

For example, the TM25 may easily be used as part of a multiple channel temperature controller. One function key is used along with a number from the keyboard to indicate the temperature point of interest. A second function used with a keyboard-entered number fixes the setpoint temperature. The third and fourth function keys indicate to the computer that the user is entering alarm limit data. A fifth function key can be used to cause the computer to display the current temperature of a specific point or to display each temperature point in sequence. The computer can indicate that a temperature point is out of limits by flashing the TM25 displays.

As an alternative, if the function lights are used as prompts, the computer could lead the operator through the various data gathering steps by lighting the proper function lights. For instance, in a factory floor data acquisition system, lighting the first function light can be used to tell the operator to start a sequence by entering operator's badge number. The second function light would indicate that the operator should enter the lot number. The third function light then would indicate the number of units in the lot that passed to the next stage.

These discussions assume that the function keys/lights are labeled. Labeling can be done by writing on the special white label surface below each function light or affixing a stick-on label in the same position. In OEM quantities, the front panel of the TM25 can be customized for a moderate cost.

The TM25 is available in four versions:

	Keyboard	Protocol
TM25 - 300NT	Numeric	Single-drop
TM25 - 300HT	Hexadecimal	Single-drop
TM25 - 300NM	Numeric	Multidrop
TM25 - 300HM	Hexadecimal	Multidrop

SINGLE-DROP MODE

DISPLAY

The TM25 has two display areas:

1) The 8-digit display
2) The seven function lights (light emitting diodes - LED's)

DIGIT DISPLAY

Each TM25 has an 8-digit display implemented with seven segment LED's. The display also features an embedded decimal point which does not use any of the eight digit positions and a minus sign which does use one of the eight digit positions. Any hexadecimal character (0 - F) may be displayed as shown in Figure 1.

FIGURE 1. TM25 Hexadecimal Display.

Digits appear in the display as transmitted from the computer on the serial interface. If numeric only data is transmitted, then numeric only data will appear. If hexadecimal data is transmitted, hexadecimal data will appear.

Digits appear in the display as keys are depressed. With a numeric keyboard, only numeric digits will appear in the display due to key depressions. The computer, however, may transmit any characters, 0 - F, to the display regardless of the keyboard.

As keys are depressed, the digits appear in the right-most position and move to the left across the display as subsequent keys are depressed.

When the CLEAR key is depressed, the display is blanked except for the right-most digit which will show as a zero with a trailing decimal point. When the first digit key is depressed, the zero is replaced by the digit that was depressed. The trailing decimal point remains in the right-most position unless a decimal point is subsequently entered from the keyboard. The decimal point appears to the right of each digit. Only one decimal will appear on the display in any one number.

The minus sign will appear only in the position to left of the numeric or hexadecimal number displayed. The minus sign must be the first character entered in order to display a negative entry.

FUNCTION LIGHTS

Each TM25 has seven function lights (LED's). Each function light is physically placed beside its corresponding function key.

Any or all of the seven function lights may be turned on by command from the computer via the serial interface or by the user depressing the corresponding function keys.

When the CLEAR key is depressed, all function lights are turned off.

KEYBOARD

Two keyboards are available for the TM25:

1) Numeric keyboard including seven function keys.
2) Hexadecimal keyboard including seven function keys.

The TM25 keyboard is implemented with an embossed polycarbonate cover over key domes. This provides a waterproof front panel and keys with tactile feedback.

NUMERIC KEYBOARD

The numeric keyboard includes the digits 0 through 9, seven function keys, a minus sign, decimal point, CLEAR and ENTER. A TM25 front cover with a numeric keyboard is shown in Figure 2.

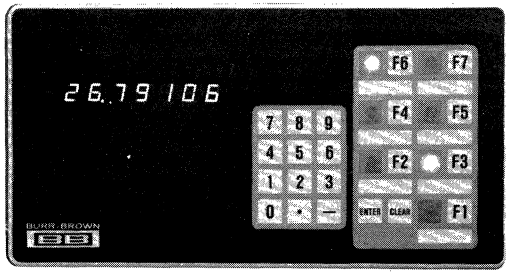


FIGURE 2. TM25 With Numeric Keyboard.

HEXADECIMAL KEYBOARD

The hexadecimal keyboard includes the digits 0 through F, seven function keys, minus sign, decimal point, CLEAR and ENTER. A TM25 front cover with a hexadecimal keyboard is shown in Figure 3.

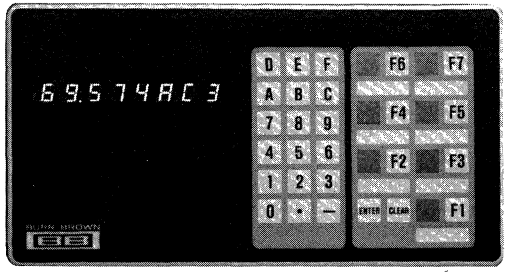


FIGURE 3. TM25 With Hexadecimal Keyboard.

ENTER KEY

After data keys (or the CLEAR key) have been depressed (causing digits to appear in the display and/or function lights to turn on) the ENTER key may be depressed. The ENTER key causes the data appearing in the digit display and in the function lights to be transmitted on the serial interface. When the ENTER key is depressed in this manner, the displays will blink once. If the ENTER key is depressed again before any new data keys are depressed, no further transmission will be made. If a transmission from the computer is received after a data key is depressed, but before the ENTER key is depressed, the data will be held in the TM25 input buffer until the ENTER key is depressed. At this time the data received from the computer will be transferred from the input buffer to the display.

CLEAR KEY

When the CLEAR key is depressed, the digit display is blanked except for the right-most digit which becomes a zero with a trailing decimal point. At the same time, all function lights are turned off.

The CLEAR key may be used to clear improper data before the ENTER key is depressed. It may also be used to blank the display after an ENTER. If the CLEAR key is depressed followed by the ENTER key, the TM25 will transmit a zero followed by Z_1Z_2 characters indicating all function lights are off.

If a transmission from the computer has been received and is holding in the TM25 input buffer, it will be transferred to the display when CLEAR is depressed.

MINUS SIGN KEY

To make a negative entry, the minus sign key must be depressed before any numeric or hexadecimal keys (including the decimal point) are depressed. The function keys may be depressed before or after the minus sign key.

COMMUNICATIONS PROTOCOL

The serial interface of the TM25 transmits standard ASCII characters with 20mA current loop and EIA RS232C/V.24 conditioning. When the ENTER key is depressed, the data message is transmitted to the computer.

COMMUNICATIONS TERMINOLOGY

[DDD] Data to or from the 8-character digit display. Zero to eight characters plus optional imbedded decimal point may be transmitted. Leading minus sign is one character. If no characters are transmitted to the TM25 the digit display is cleared. The most significant digit is transmitted first.

Z_1Z_2 Data to function lights or from function keys. On transmission to the terminal, Z_1Z_2 may be one, two or no characters. If no characters, all message lights cleared. If one character, it is interpreted as Z_1. If two characters, they are interpreted as Z_1 and Z_2. On transmissions from the terminal, Z_1 and Z_2 are always transmitted.

CR Carriage Return

LF Line Feed

COMPUTER TO TERMINAL TRANSMISSION

The following information is transmitted by the computer to a TM25:

[DDD]	[Delimiter]	[Z_1Z_2]	[Delimiter]

Delimiter: The delimiter may be a CR or LF.

DDD: The digit data may be hexadecimal or numeric regardless of the model of TM25 used. The most significant digit is always transmitted first.

If function data [Z_1Z_2] is not sent, the first [Delimiter] may be CR LF or CR CR; [Z_1Z_2] and the second [Delimiter] are eliminated as shown below:

[DDD] CR LF or [DDD] CR CR

The terminal will "turn off" the function lights with this transmission. If [DDD] is greater than eight characters, all characters after the first eight will be ignored. If [DDD] is no characters, the digit display will be completely blanked. Examples of various [DDD] information are shown in Table I.

TABLE I. Examples of Digit Displays.

[DDD]	Digit Display
8732371	8732371.
3.2371	3.2371
-25.71	-25.71
-14	-14
83721555312	83721555.

If a terminal key is being depressed while the computer is transmitting data to the terminal, the portion of the transmission which occurred before the key was depressed will not be received. A key depression occurring after the final [Delimiter] will not affect the transmission. A transmission to the TM25 must occur at least 4msec after the end of a TM25 to computer transmission. Also, the TM25 requires a 40msec delay after receiving a message before it can receive another one.

TERMINAL TO COMPUTER TRANSMISSION

The following information is transmitted to the computer from the TM25 when the ENTER key is depressed:

[DDD] CR LF [Z_1Z_2] CR LF

The minimum [DDD] which can be transmitted to the computer is one character. [DDD] consists of only the numbers 0 through 9 for numeric keyboards and 0 through F for hexadecimal keyboards for transmission to the computer.

FUNCTION CHARACTERS

Function lights F1 through F7 can be turned on or off by the computer. The function lights are controlled by the transmission of two printable ASCII characters - Z_1 and Z_2. The control bits for lights F1, F2, F3, and F4 are encoded in four bits of Z_1 (b_1 - b_4). The control bits for F5, F6, and F7 are encoded in three bits of Z_2 (b_1 - b_3). Bits b_5, b_6, and b_7 of Z_1 are fixed as 100; bits b_4, b_5, b_6, and b_7 of Z_2 are fixed as 1010. Table II shows the encoding of Z_1 and Z_2.

TABLE II. Z_1 and Z_2 Character Encoding.

	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Z_1	1	0	0	F4	F3	F2	F1
Z_2	1	0	1	0	F7	F6	F5

The same format is used to indicate that one or more function keys have been depressed. When the ENTER key is depressed, the status of all the function keys is encoded in characters Z_1 and Z_2.

One, two or no characters may be transmitted to the terminal. If no characters are sent, the message lights are cleared. If one character is sent, it will be interpreted as Z_1; Z_2 message lights are then cleared. If two characters are sent, they are interpreted as Z_1 and Z_2. Both characters are always transmitted from the terminal.

When transmitted from the microterminal, a bit equal to Logic 1 (MARK) indicates that a function key was depressed. When transmitted from the computer, a bit equal to Logic 1 (MARK) turns on that function light. For example, if only the F1 key is depressed, Z_1 is transmitted as 1000001. Likewise, if only function light F1 is to be turned on and all other lights turned off (or left off) the Z_1 and Z_2 characters which the computer must transmit to the TM25 are: Z_1 - 1000001, Z_2 - 1010000. The ASCII characters which these codes represent are listed in Tables III and IV. In the above example Z_1 (1000001) is A and Z_2 (1010000) is P. As noted previously, Z_2 would not need to be transmitted to turn off all Z_2 function lights.

TABLE III. Z_1 Characters.

ASCII Code							ASCII Char.
b_7	b_6	b_5	b_4 F4	b_3 F3	b_2 F2	b_1 F1	Z1
1	0	0	0	0	0	0	@
1	0	0	0	0	0	1	A
1	0	0	0	0	1	0	B
1	0	0	0	0	1	1	C
1	0	0	0	1	0	0	D
1	0	0	0	1	0	1	E
1	0	0	0	1	1	0	F
1	0	0	0	1	1	1	G
1	0	0	1	0	0	0	H
1	0	0	1	0	0	1	I
1	0	0	1	0	1	0	J
1	0	0	1	0	1	1	K
1	0	0	1	1	0	0	L
1	0	0	1	1	0	1	M
1	0	0	1	1	1	0	N
1	0	0	1	1	1	1	O

TABLE IV. Z_2 Characters.

ASCII Code							ASCII Char.
b_7	b_6	b_5	b_4	b_3 F7	b_2 F6	b_1 F5	Z_2
1	0	1	0	0	0	0	P
1	0	1	0	0	0	1	Q
1	0	1	0	0	1	0	R
1	0	1	0	0	1	1	S
1	0	1	0	1	0	0	T
1	0	1	0	1	0	1	U
1	0	1	0	1	1	0	V
1	0	1	0	1	1	1	W

TABLE V. ASCII Characters.

ASCII Graphic	Hexadecimal Code	Octal Code	Decimal Code	b_7	b_6	b_5	b_4	b_3	b_2	b_1
CR	0D	15	13	0	0	0	1	1	0	1
LF	0A	12	10	0	0	0	1	0	1	0
0	30	60	48	0	1	1	0	0	0	0
1	31	61	49	0	1	1	0	0	0	1
2	32	62	50	0	1	1	0	0	1	0
3	33	63	51	0	1	1	0	0	1	1
4	34	64	52	0	1	1	0	1	0	0
5	35	65	53	0	1	1	0	1	0	1
6	36	66	54	0	1	1	0	1	1	0
7	37	67	55	0	1	1	0	1	1	1
8	38	70	56	0	1	1	1	0	0	0
9	39	71	57	0	1	1	1	0	0	1
A	41	101	65	1	0	0	0	0	0	1
B	42	102	66	1	0	0	0	0	1	0
C	43	103	67	1	0	0	0	0	1	1
D	44	104	68	1	0	0	0	1	0	0
E	45	105	69	1	0	0	0	1	0	1
F	46	106	70	1	0	0	0	1	1	0
G	47	107	71	1	0	0	0	1	1	1
H	48	110	72	1	0	0	1	0	0	0
I	49	111	73	1	0	0	1	0	0	1
J	4A	112	74	1	0	0	1	0	1	0
K	4B	113	75	1	0	0	1	0	1	1
L	4C	114	76	1	0	0	1	1	0	0
M	4D	115	77	1	0	0	1	1	0	1
N	4E	116	78	1	0	0	1	1	1	0
O	4F	117	79	1	0	0	1	1	1	1
P	50	120	80	1	0	1	0	0	0	0
Q	51	121	81	1	0	1	0	0	0	1
R	52	122	82	1	0	1	0	0	1	0
S	53	123	83	1	0	1	0	0	1	1
T	54	124	84	1	0	1	0	1	0	0
U	55	125	85	1	0	1	0	1	0	1
V	56	126	86	1	0	1	0	1	1	0
W	57	127	87	1	0	1	0	1	1	1

CHARACTER CODE

The character code used is the American Standard Code for Information Interchange (ASCII) (see Table V) and ISO 646-1973(E) Standard. The order of bit transmission is that commonly used and specified by ISO and ANSI as shown in Figure 4.

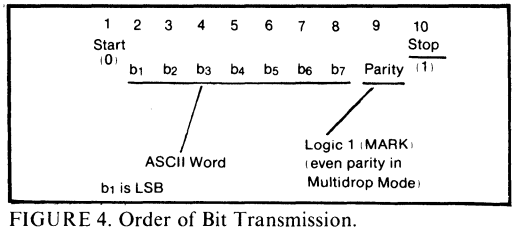


FIGURE 4. Order of Bit Transmission.

OPERATION

The TM25 is intended to be connected via a serial ASCII interface to a computer.

DATA DISPLAY

A transmission to the TM25 will cause digits to appear in the digit display and/or function lights to turn on. The display will remain unchanged until a new transmission from the computer or until data is entered from the keyboard. When a new transmission is received from the computer, the displays will take on the new values instantly when the final [Delimiter] is received. When the first key is depressed, the digit and function lights are cleared while that digit or light appears.

DATA ENTRY

As digit keys are depressed, the character appears on the right-most position of the digit display. As subsequent keys are depressed, the previously entered characters move to the left while the most recently entered digit appears in the right-most position. This operation is similar to that of a calculator.

POWER-UP INITIALIZATION

On power-up, all buffers and displays are initialized to zero. Serial output will be initialized to Logic 1 (MARK).

FLASHING DISPLAY

TM25's display can be made to flash very easily under computer control. Assume that [D1] are the digit display characters and [Z] the function light characters which will be flashed. The following sequence will flash these characters:

[D1] CR [Z] LF Displays D1 and Z
<DELAY>
CRLF
Blanks Display
[D1] CR [Z] LF
<DELAY>
CRLF
Repeat

The <DELAY> generated in the computer will determine the length of time the displays are on. The display will remain blanked for the length of the transmission time of the display data, 165msec to 429msec.

SERIAL INTERFACE

The TM25 serial interface provides both EIA RS232C/V.24 and 20mA current loop conditioning simultaneously.

CONNECTOR

A 25-pin female connector (type DB-25S) is provided on the rear of the TM25 (see Figure 5). Both the RS232C/V.24 and 20mA current loop are available through this connector. The mating 25-pin male connector (type DB-25P) with plastic shield assembly and mounting screws is available from Burr-Brown as 2525MC.

The 2525MC consists of:

1. Male HDP connector - 205208-1
2. Individual pins (solder connector) - 1-66506-0
3. Hand tool to insert pins in connector - 91067-2
4. Male screw retainer kit - 205980-1
5. Shield Assembly - 205718-1

The AMP Inc. part number is listed for each item.

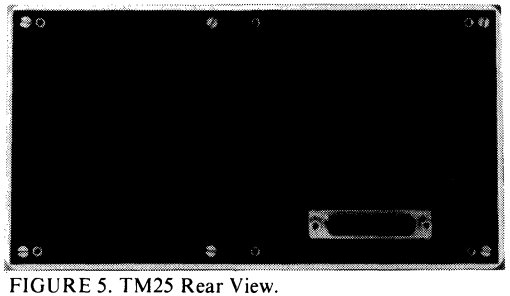


FIGURE 5. TM25 Rear View.

Connector Pinout

Pin Number	Function
1	Ground - Current loop
2	Terminal to computer - EIA RS232C/V.24
3	Computer to terminal - EIA RS232C/V.24
4	Not used
5	Not used
6	Not used
7	Ground - Current loop
8	Not used
9	Not used
10	Not used
11	Current loop power
12	(+) Terminal to computer - Current loop
13	(+) Computer to terminal - Current loop
14	Not used
15	+15VDC power supply input
16	Not used
17	Not used
18	Current loop power
19	Not used
20	Not used
21	Not used
22	Not used
23	Not used
24	(-) Terminal to computer - Current loop
25	(-) Computer to terminal - Current loop

EIA RS232C/V.24 SPECIFICATIONS

The EIA RS232C/V.24 interface is a voltage signal.

COMPUTER TO TERMINAL

MARK = Logic 1 - −3V to −15V voltage level
SPACE = Logic 0 - +3V to +15V voltage level

TERMINAL TO COMPUTER

MARK = Logic 1 - Nominal −10V
SPACE = Logic 0 - Nominal +10V

Interconnection

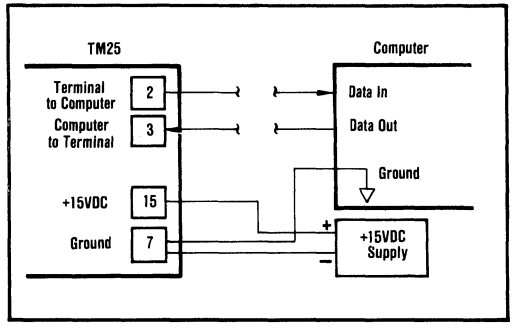


FIGURE 6. EIA RS232C/V.24 Interconnection Diagram.

CURRENT LOOP SPECIFICATIONS

The current loop is optically isolated.

COMPUTER TO TERMINAL & TERMINAL TO COMPUTER

MARK = Logic 1 - 20mA
SPACE = Logic 0 - 0mA

Interconnection

There are two ways of connecting the TM25 current loop to a computer:

1. External power source
2. Internal power source

EXTERNAL POWER SOURCE (see Figure 7)

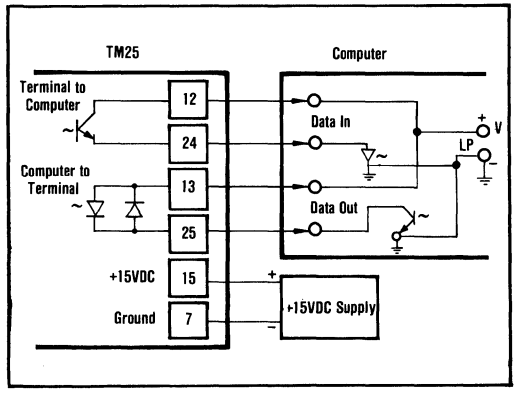


FIGURE 7. Current Loop Interconnection Diagram with External Power Source.

With an external power source, the TM25 is electrically isolated from the computer.

INTERNAL POWER SOURCE (see Figure 8)

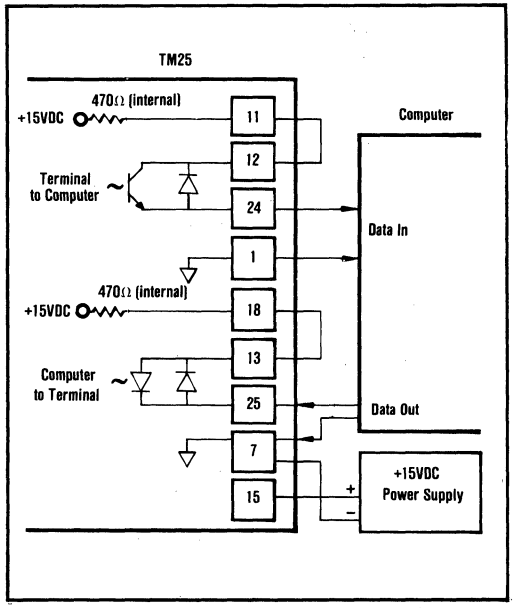


FIGURE 8. Current Interconnection Diagram with Internal Power Source.

When using the internal power sources, of course, the TM25 is not electrically isolated.

TTL Interface

With external pull up/pull down resistors, the current loop will interface to TTL levels.

POSITIVE LOGIC (see Figure 9)

MARK = Logic 1 - +5V
SPACE = Logic 0 - +0.4V

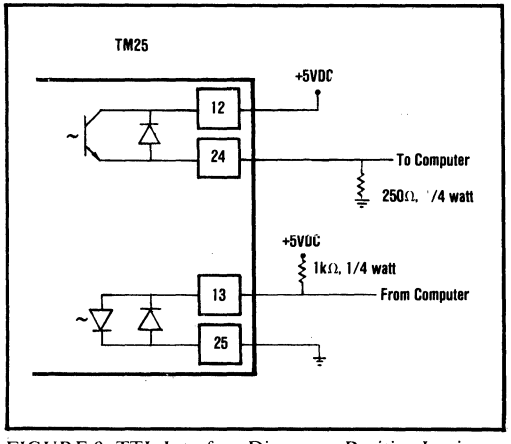


FIGURE 9. TTL Interface Diagram - Positive Logic.

NEGATIVE LOGIC (see Figure 10)

MARK = Logic 1 - +0.4V
SPACE = Logic 0 - +5V

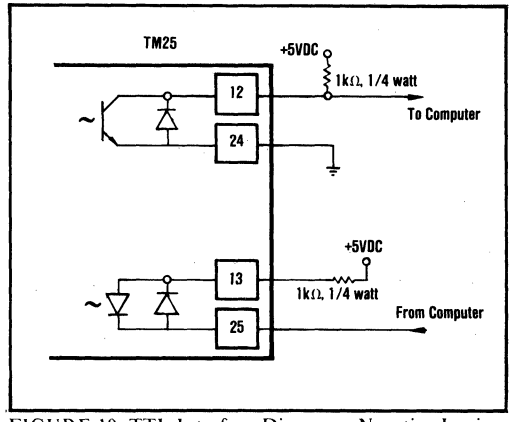


FIGURE 10. TTL Interface Diagram - Negative Logic.

TRANSMISSION DISTANCE

TABLE VII. Transmission Standards Distance Limitations.

Conditioning	Maximum recommended transmission distance
RS232C/V.24	15 meters (50 feet)
Current Loop	1500 meters (5000 feet)

A distance limitation for current loop that should be considered is the compliance of the loop power source.

The forward voltage drop across the input diode is 1.5V max. The loop power source must be able to drive 1.5V plus the voltage drop produced by the resistance of the wire in the communications line.

The resistance of wire 1mm in diameter (#18AWG) is 4Ω per 100-meter loop (13Ω per 1000-foot loop). The voltage drop caused by the resistance of the wire is 0.08V per 100-meter loop (0.25V per 1000-foot loop). The resistance of wire 0.5mm in diameter (#24AWG) is 16Ω per 100-meter loop (51Ω per 1000-foot loop), so that voltage drop will increase by a factor of four.

MULTIDROP MODE

In the Multidrop Mode, a number of TM25's may be connected to the same serial link. Each terminal has a user-set drop address (0 - 99). Data transmitted to that address by the computer will be displayed by the desired terminal. The computer must poll the terminals on a loop to check for data to be output. A TM25 will ignore any transaction which is not directed to its address. If a parity error is detected in a transmission, the addressed terminal will transmit an error message. When a transmission is received from the computer, the TM25 will transmit an acknowledgement if no errors have been detected.

DISPLAY

The display operates as in the single-drop mode, except that when the ENTER key is depressed, the digit display and any active function lights will blink until the computer polls the TM25 to allow it to transmit the data. When the data has been transmitted, the display will stop blinking. It will contain the data that was ENTERed.

KEYBOARD

The keyboard is the same as in the single-drop mode.

ENTER KEY

The ENTER key operates as in the single-drop mode, except that when the ENTER key is depressed, the data entered is transferred to the output buffer. The data remains displayed in the digit display and function lights blink until the computer polls the unit to allow the data to be transmitted. After the microterminal transmits the data, the displays will stop blinking, but the data will remain.

CLEAR KEY

The CLEAR key operates as in the single-drop mode.

MINUS SIGN KEY

The minus sign key operates as in the single-drop mode.

COMMUNICATIONS PROTOCOL

The serial interface transmits standard ASCII characters with 20mA current loop and EIA RS232C/ V.24 conditioning. Parity is even.

All commands sent to a TM25 in the multidrop mode begin with the start of address character "#" (ASCII 43_8), and two digits representing the terminal address. The command characters ">" (ASCII 76_8) or "?" (ASCII 77_8) follow the terminal address. The ">" character indicates data is being transmitted to the terminal. The "?" character indicates that the computer is polling the terminal (requesting information).

COMMUNICATIONS TERMINOLOGY

[ADRS] Terminal Address - a 2-digit decimal number between 00 and 99.

[DDD] Data to or from the 8-character digit display. Zero to eight characters plus optional imbedded decimal point may be transmitted. Leading minus sign is one character. If no characters are transmitted to the TM25, the digit display is cleared. The most significant digit is always transmitted first.

Z_1Z_2 Data to function lights or from function keys. On transmission to the terminal, Z_1Z_2 may be 0, 1 or 2 characters; if no characters, all message lights cleared; if one character, it is interpreted as Z_1. In a transmission from the terminal, Z_1 and Z_2 are always transmitted.

CR Carriage Return

LF Line Feed

Start of Address Character

> Input Command

? Output Command

$ Acknowledgement

* Parity Error

COMPUTER TO TERMINAL DATA TRANSMISSION SEQUENCE

Computer to Terminal

The following information is transmitted by the computer to a TM25:

[ADRS] > [DDD] [Delimiter] [Z_1Z_2] [Delimiter]

[Delimiter]: The delimiter may be a CR or LF

[DDD]: The digit data may be hexadecimal or numeric regardless of the model of TM25 used.

If function data [Z_1Z_2] is not sent, the first [Delimiter] may be CRLF or CRCR; [Z_1Z_2] and the second [Delimiter] are eliminated as shown below:

[ADRS] > [DDD] CR LF or

[ADRS] > [DDD] CR CR

The terminal will "turn off" the function lights with this transmission. If [DDD] is greater than 8 characters, all characters after the first 8 will be ignored. If [DDD] contains no characters, the digit display will be completely blanked. There should be no blanks between characters.

Terminal to Computer

If the data was properly received at the terminal, an acknowledgement will be sent by the terminal to the computer. If a parity error is detected, a parity error message will be sent by the terminal to the computer. If no transmission is received by the computer from the terminal, the data was not received.

ACKNOWLEDGEMENT: # [ADRS] $ CRLF

PARITY ERROR: # [ADRS] * CRLF

The acknowledgement will be sent within 30 communication bit times (100msec) after transmission to terminal.

The parity error message will be transmitted as soon as it is detected. (This can be during the original computer to terminal transmission.)

If a terminal key is being depressed while the computer is transmitting data to the terminal, the data will not be received and the terminal will not respond.

TERMINAL TO COMPUTER DATA TRANSMISSION SEQUENCE

Computer to Terminal

The computer must ask for data from a terminal. It polls each terminal by sending this information:

[ADRS] ? [Delimiter]

[Delimiter]: The delimiter may be CR, LF or CRLF

There should be no blanks between characters.

Terminal to Computer

The terminal responds by transmitting the data in its output buffer or a parity error message if a parity error was detected.

DATA: [DDD] CR LF [Z_1Z_2] CR LF

PARITY ERROR: # [ADRS] * CR LF

The minimum [DDD] which can be transmitted to the computer is one character. For transmissions to the computer [DDD] consists of only the numbers 0 - 9 for numeric keyboards and 0 - F for hexadecimal keyboards.

The terminal will respond within 30 communication bit times (100 milliseconds). If a terminal key is being depressed while the terminal is being polled, it will not respond.

The parity error message will be transmitted as soon as it is detected. (This can be during the original computer to terminal transmission.)

FUNCTION CHARACTERS

Function characters are received and transmitted as in the single-drop mode.

CHARACTER CODE

The character code used is same as in the single-drop mode except that parity is even.

EXTRANEOUS CHARACTERS

The TM25 will recognize "#" as the start of data transmission. Any ASCII character that occurs in the header during an input transaction, but which does not conform exactly to the input format specified, will cause the terminal to ignore the entire data transaction.

The data in [DDD], [Z_1Z_2], and [Delimiter] are treated as in the single-drop mode. See the Appendix.

[ADRS] ? [Delimiter]

[ADRS] > [DDD] [Delimiter] Z_1Z_2 [Delimiter]

In the above transmissions from computer to terminal,

1. # [ADRS] ? and
2. # [ADRS] >

must be transmitted exactly as specified.

OPERATION

The TM25 in the multidrop mode is intended to be connected via a serial ASCII interface to a computer.

DATE ENTRY AND DISPLAY

A computer to terminal data input transmission will send data to the terminal's input buffer.

1. If data keys have been depressed but the ENTER key has not, the data transmitted to the terminal will remain in the input buffer. When the terminal's ENTER or CLEAR key is then depressed, the data will be transferred from the input buffer to the display. (If ENTER is depressed, the operator-entered data will be transferred to the output buffer to await an output command from the computer.)
2. In all other cases, the data is transferred directly to the display after the [Delimiter] is received.

The data in the display will remain in the display until the terminal receives another input transmission from the computer or until data is entered from the keyboard.

When data keys are depressed and then the ENTER key, the display will blink until polled by the computer.

As digit keys are depressed, the character appears on the right-most position of the digit display. As subsequent keys are depressed, the previously entered characters move to the left while the most recently entered digit appears in the right-most position. This operation is similar to that of a calculator.

DATA TRANSMISSION

When the computer asks for data (# [ADRS] ? CR) the terminal will transmit the contents of its output buffer. The data in the output buffer is not changed with an output transmission. If the computer continues to ask for data, the same information will be sent each time until new data is ENTERed from the keyboard (i.e., until the ENTER key is depressed). (The data in the output buffer remains the same even if the CLEAR key is depressed.)

OTHER

All other operation is the same as the single-drop mode.

SERIAL INTERFACE

The serial interface specifications and connector are the same as in the single-drop mode.

NUMBER OF TERMINALS PER LINE

A number of TM25's can be connected in series on a 20mA current loop (see Figure 11).

The number of terminals which can be connected on one communications line is limited by operational, and electrical considerations:

Electrical Considerations. The forward voltage drop across the input diode is 1.5V max. The loop power supply must be able to drive 1.5V for each TM25 in series. Thus with four TM25's on a line, 6V is required to drive the diodes. The current loop circuitry at the computer and the resistance of the wire in the communications line also produce voltage drops. Using the internal current source, up to eight terminals can be reliably operated on one communications line.

Operational Considerations. A typical data transmission to the terminal requires 0.4 seconds; terminals can be polled at a rate of six per second; a typical data transmission to the computer requires 0.4 seconds. The number of terminals on a single line should be such that you may update or poll at an adequate rate.

In addition, each computer to terminal transmission will cause the displays of all TM25's connected to the serial line to dim. Therefore, the number of computer to terminal transmissions (such as polling) should be minimized to reduce display dimming.

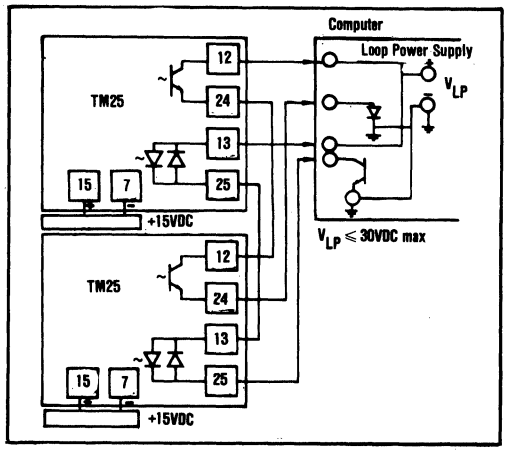


FIGURE 11. Typical Multidrop Connection via Current Loop.

The current loop interface of the TM25 multidrop terminal may be connected to a computer with only EIA RS232C serial ports by using the following EIA/current loop converters.

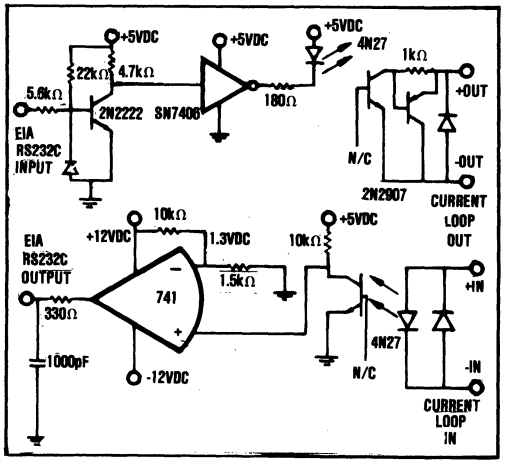
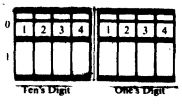


FIGURE 12. EIA/Current Loop Converter.

ADDRESS SELECTION

Two dip switches accessable from the rear of the TM25 select the terminal's address. Any address from 0 to 99 can be chosen:

Each digit is BCD encoded as shown below:



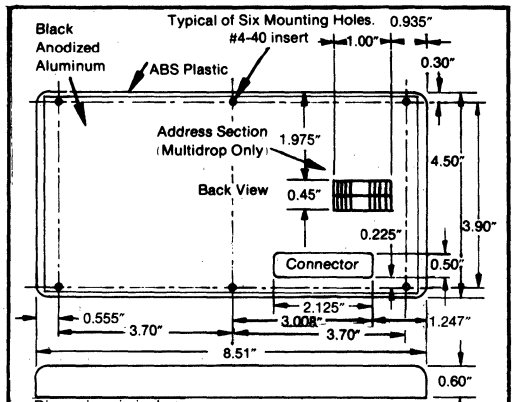
NOTE:
Switches on some units may be numbered 1 through 8.

SWITCH / DIGIT	1	2	3	4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
N A	0	1	0	1
N A	1	1	0	1
N A	0	0	1	1
N A	1	0	1	1
N A	0	1	1	1
N A	1	1	1	1

SPECIFICATIONS

DIGIT DISPLAY	SINGLE-DROP AND MULTIDROP
Number of Digits	8 plus decimal point
Type of Digit Display	7 segment
Characters Displayed	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F, minus sign
Character Height	7.6mm (0.3")
FUNCTION LIGHTS	
Number of Lights	7
Type of Light	Red, LED
KEYBOARD	
Type of Keyboard	Numeric or Hexadecimal
Number of Function Keys	7
MATERIAL	
Front Panel	Polycarbonate
Back Panel	Black Anodized Aluminum
Case	ABS Plastic
The front cover will be attacked by these chemicals.	Chlorinated or Fluorinated Hydrocarbons PVC plasticizing agents Amines
DO NOT USE FLUOROCARBONS (TMC, Freon, etc.) TO CLEAN!	
SERIAL INTERFACE	
Conditioning	RS232C/V.24 and 20mA Current Loop
Baud Rate	300 baud
RS232C	
Output Voltage	
Logic 1	-10VDC
Logic 0	+10VDC
Input Voltage	
Logic 1	-3VDC to -15VDC
Logic 0	+3VDC to +15VDC
20mA Current Loop	
Input	
Forward Voltage Drop	1.5V max at 30mA/1.3V max at 10mA
Output	
Saturation Voltage	1.3V max at 30mA
Breakdown Voltage	30V max
TEMPERATURE RANGE	
Operating	0°C to +70°C
Storage	-40°C to +85°C
POWER SUPPLY	
Voltage	+15VDC ±5%
Current	250mA max
WEIGHT	290 grams (10 oz)

MECHANICAL



Dimensions in inches.

Mounting Screws: #4-40, 7/16" - 6 included with each TM25. Burr-Brown model 25MK consists of six #4-40, 7/16" mounting screws, if extras are needed. Maximum allowable screw depth: 0.375"

APPENDIX

ADDITIONAL CHARACTERS

As indicated in the Communications Protocol section, transmission from the TM25 to the computer will be:

1. [DDD]: 0 - 9 (numeric or 0 - F (hexadecimal), decimal point, minus sign.
2. Z_1: @, A - O
3. Z_2: P - W

These are the only characters which can be transmitted from a TM25.

For transmission to a TM25, the microterminal will respond to exactly the same characters as shown above, that is:

1. [DDD]: 0 - 9 or 0 - F, decimal point, minus sign.
2. Z_1: @, A - O
3. Z_2: P - W

The TM25 will also respond to other ASCII characters to provide the same digit display (0 - F) and to turn on function lights if these characters are transmitted to the TM25. For Multidrop version, the header protocol must be exactly as specified. The TM25 will not respond to any other characters.

Table A-I shows the entire 128-character ASCII character set.

Table A-II shows the characters which will appear in the digit display for each ASCII character transmitted in [DDD]. Notice that all characters in columns 1 through 7 will appear as characters 0 - F in the digit display. Any ASCII character from column 0 will be interpreted by the TM25 as a [Delimiter].

Table A-III shows the function lights which will be "turned on" or "turned off" by each ASCII character transmitted to the TM25 in [Z_1Z_2].

If for example, PQRSTUVW were transmitted to the TM25 as [DDD], 01234567 would appear in the digit display. If 11 were transmitted to the TM25 as [Z_1Z_2], function lights F1 and F5 would light.

It is recommended for simplicity, that the computer transmit the same character set to the TM25 as the TM25 transmits to the computer.

TABLE A-I. ASCII Character Set.

				b_7	0	0	0	0	1	1	1	1
				b_6	0	0	1	1	0	0	1	1
				b_5	0	1	0	1	0	1	0	1
b_4	b_3	b_2	b_1	COLUMN / ROW	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	ø	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	|
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	_	o	DEL

TABLE A-II. Digit Display Characters.

			b_7 b_6 b_5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4	b_3	b_2	b_1	COLUMN / ROW	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL CR	DLE 0	SP 0	ø 0	@ 9	P 0	◣ 0	p 0
0	0	0	1	1	SOH CR	DC1 1	! 1	1 1	A A	Q 1	a 1	q 1
0	0	1	0	2	STX CR	DC2 2	" 2	2 2	B B	R 2	b 2	r 2
0	0	1	1	3	ETX CR	DC3 3	# 3	3 3	C C	S 3	c 3	s 3
0	1	0	0	4	EOT CR	DC4 4	$ 4	4 4	D D	T 4	d 4	t 4
0	1	0	1	5	ENQ CR	NAK 5	% 5	5 5	E E	U 5	e 5	u 5
0	1	1	0	6	ACK CR	SYN 6	& 6	6 6	F F	V 6	f 6	v 6
0	1	1	1	7	BEL CR	ETB 7	' 7	7 7	G 0	W 7	g 7	w 7
1	0	0	0	8	BS CR	CAN 8	(8	8 8	H 1	X 8	h 8	x 8
1	0	0	1	9	HT CR	EM 9	) 9	9 9	I 2	Y 9	i 9	y 9
1	0	1	0	10	LF CR	SUB A	* A	: A	J 3	Z A	j A	z A
1	0	1	1	11	VT CR	ESC b	+ b	; b	K 4	[b	k b	{ b
1	1	0	0	12	FF CR	FS C	, C	< C	L 5	\ C	| C	¦ C
1	1	0	1	13	CR CR	GS d	- -	= d	M 6	] d	m d	} d
1	1	1	0	14	SO CR	RS E	. .	> E	N 7	^ E	n E	~ E
1	1	1	1	15	SI CR	US F	/ F	? F	O 8	— F	o F	DEL F

This table indicates the character that will appear on the digit display for each ASCII character.

TABLE A-III. Z_1 and Z_2 Characters.

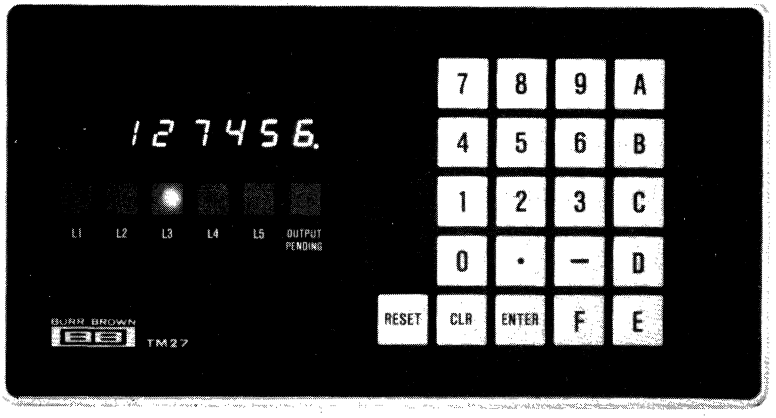
				b_7	0	0	0	0	1	1	1	1
				b_6	0	0	1	1	0	0	1	1
				b_5	0	1	0	1	0	1	0	1
b_4	b_3	b_2	b_1	COLUMN / ROW	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL CR 0000	DLE 0000	SP 0000	ø 0000	@ 0000	P 0000	` 0000	p 0000
0	0	0	1	1	SOH CR 0001	DC1 0001	! 0001	1 0001	A 0001	Q 0001	a 0001	q 0001
0	0	1	0	2	STX CR 0010	DC2 0010	" 0010	2 0010	B 0010	R 0010	b 0010	r 0010
0	0	1	1	3	ETX CR 0011	DC3 0011	# 0011	3 0011	C 0011	S 0011	c 0011	s 0011
0	1	0	0	4	EOT CR 0100	DC4 0100	$ 0100	4 0100	D 0100	T 0100	d 0100	t 0100
0	1	0	1	5	ENQ CR 0101	NAK 0101	% 0101	5 0101	E 0101	U 0101	e 0101	u 0101
0	1	1	0	6	ACK CR 0110	SYN 0110	& 0110	6 0110	F 0110	V 0110	f 0110	v 0110
0	1	1	1	7	BEL CR 0111	ETB 0111	' 0111	7 0111	G 0111	W 0111	g 0111	w 0111
1	0	0	0	8	BS CR 1000	CAN 1000	(1000	8 1000	H 1000	X 1000	h 1000	x 1000
1	0	0	1	9	HT CR 1001	EM 1001	) 1001	9 1001	I 1001	Y 1001	i 1001	y 1001
1	0	1	0	10	LF CR 1010	SUB 1010	* 1010	: 1010	J 1010	Z 1010	j 1010	z 1010
1	0	1	1	11	VT CR 1011	ESC 1011	+ 1011	; 1011	K 1011	[1011	k 1011	{ 1011
1	1	0	0	12	FF CR 1100	FS 1100	, 1100	< 1100	L 1100	\ 1100	1100	¦ 1100
1	1	0	1	13	CR CR 1101	GS 1101	- 1101	= 1101	M 1101	] 1101	m 1101	} 1101
1	1	1	0	14	SO CR 1110	RS 1110	. 1110	> 1110	N 1110	^ 1110	n 1110	— 1110
1	1	1	1	15	SI CR 1111	US 1111	/ 1111	? 1111	O 1111	— 1111	o 1111	DEL 1111

This table indicates the function lights that will be "turned on" or "turned off" for each ASCII character.

Z_1: XXXX = F4 F3 F2 F1

Z_2: XXXX = Don't Care F7 F6 F5

TM27
USER'S GUIDE



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PDS-469

INTRODUCTION

If your system's data/entry/control/display requirements are sophisticated but limited in volume, you don't need to buy big, expensive, and fragile CRT's or printing terminals to do the job efficiently.

The TM27 is a low cost approach to the problem of remote data entry, utilizing an RS-422 interface to accommodate the use of a multiterminal loop arrangement. While designed as numeric only entry, the availability of function keys and lights, digital inputs and digital outputs, and the extended character set of the unit allows for a wide variety of responses and messages to be communicated.

The TM27 "microterminal" features a numeric/hexadecimal keyboard and display. The TM27 uniquely flexible in application versatility is designed expressly to fill the human interface demands of widely dispersed control and communications networks in factory data collection, machine and process control, energy management systems, inventory control, and information processing.

Microterminals, because of their interface flexibility, appearance, size, durability, and easy installation, function equally well as consoles and control centers for instruments and small systems. They also perform as input/output terminals in diagnostic applications.

You don't need interface expertise to put the TM27 to work for you...it communicates in serial ASCII with RS-422 conditioning. Baud rates are 300 to 4800 bits per second.

The intended environment for this unit is "multidropped", host-controlled, polled operation. This operation is inherently half-duplex. The terminals are prohibited from transmitting until requested to do so by the host controller. Any entry made previous to pushing the ENTER key may be corrected by the operator, but once ENTER is pressed, no further entry will be accepted until the host requests transmission of the message. An output pending LED indicates that a message is waiting to be polled by the host.

A tough, water resistant front panel protects LED displays and indicators as well as a numeric keyboard. Tactile feedback, and character display confirm operator entry and, because of its design simplicity, the microterminal concept doesn't require special operator skills or training. Depressing a single function key initiates preprogrammed action by the CPU. These functions may be defined in your CPU's software.

The TM27's very compact design and simple mounting on any flat surface makes it quickly adaptable to new or existing applications. It measures only 216mm x 114mm x 15mm (8.5" x 4.5" x 0.6"). When ordered in OEM quantities the front panel can contain your corporate or system logo.

You can enter and display numeric and hexadecimal data. A 21-key keyboard allows you to enter messages of up to eight characters plus decimal point. An 8-character display permits review and editing of data entered before transmission. Thirty-six different characters can be displayed. Two 8-character message buffers are provided to hold output and input messages.

The keyboard can be locked out by CPU command. Five LED indicators are independently controlled by the CPU. The five independent LED's are driven by TTL-compatible signals which are also available on the back panel connector. These may be used to remotely control external equipment such as audible annunicators.

OPERATION

DESCRIPTION

The TM27 is a numeric microterminal which may be used as a remote or local data entry and output terminal for a host computer system. It is intended to provide a low cost, small size, alternative to a CRT terminal. It is suitable for applications with a limited amount of data interchange, as compared to applications requiring a typewriter-style keyboard and multiline display or hard copy output.

The TM27 features a dust proof front panel including a 21-key keyboard, 8-character display, and five host-computer-controllable light emitting diodes (LED's). The keyboard features raised embossing with tactile feedback. In addition, a 26-pin, rear panel connector features RS-422 data transmit and data receive. The connector is also used to provide power, communications rate selection (300 to 4800 bps), remote reset in, and reset out address. The host-controllable LED's are driven by TTL-compatible signals which are brought out to the back panel connector.

Up to six 1-character function messages may be defined by the host system. Function messages may be transmitted to the host by pressing the front panel function message keys.

For all following descriptions the terms input and output shall refer to input to and output from the TM27.

When the terminal receives a transmission, the data is stored in the input buffer and typically displayed. However, if keyboard data is being entered before the beginning of the host-to-terminal transmission, the input data will remain in the input buffer until either ENTER or CLEAR is pressed, at which time the input data will be displayed.

The TM27 utilizes a 12-character input buffer, allowing the reception of eight displayable characters and a decimal point. The remaining three bytes are intended to buffer commands from the host. This insures that the terminal can always respond to input, thus allowing the host to reset it if necessary.

As each key is pressed, it is entered into the output buffer

and the display but not transmitted. When the ENTER key is pressed, the output buffer is made ready for transmission, as indicated by the output pending LED. When the host sends the polling command ('Request Buffer') while the output pending LED is on, the TM27 will transmit the buffer to the host. The buffer is prefixed by its 2-digit address to verify the source of the message.

In the event there was an error in the transmission (wrong address, parity error, etc.), the buffer can be requested again by the "Retransmit Buffer" command. If the "Request Buffer" command had been sent again, a null message consisting of the terminal's two-digit address followed by a carriage return would be transmitted to indicate no new data had been entered. This distinguishes between repeated data and new data.

When the host sends messages or commands to the TM27, they must be prefixed by two ASCII digits in the range 00 to 63. Address 00 is a special case which is accepted by all terminals addressed from 01 to 63. This allows a single message to be received by all terminals on the multidrop line at the same time.

A number of microterminals may be connected to a single communications port using the RS-422 interface.

OPERATING INSTRUCTIONS

READY CONDITION

When power is applied to the TM27, the display will show a "0." in the left-most character position as the ready indicator. In addition, pressing RESET and CLEAR will cause the ready condition to be entered. Note that in some installations the RESET key may be disabled when the unit is installed.

RECEIVING AN INPUT MESSAGE

When the TM27 receives an input message, it will appear in the display from left-to-right when the carriage return is received. The internal message buffer holds up to eight displayable characters. For input messages larger than eight characters, only the first eight characters are retained. The host system must terminate each input message with a carriage return (CR). The carriage return is not displayed in any way and is not included in the eight characters. When the carriage return is received, the display will be loaded with the eight characters of the message.

Receipt of another message after (CR) causes the input buffer to be cleared except for the characters of the new message. Also, if a character key is pressed to start an output message, the display shows the keyboard data only.

COMPOSING AN OUTPUT MESSAGE

As each character key is pressed, the displayed message grows from left-to-right. After eight keys have been pressed (nine characters including decimal point) the display is full. If more than eight characters are pressed, only the first eight are retained. The message may be edited by pressing CLEAR and inputting the message again. When the operator wishes to end the message, it is only necessary to press ENTER. When the ENTER key is pressed at the end of the line, the display remains until new data is entered from keyboard.

FUNCTION KEYS

The host system may define up to six 1-character function messages to be stored in TM27 random access memory. The operator may send these to the host by pressing the A through F keys. When A through F are pressed prior to being defined by the host, the letters A - F are transmitted. Function messages may not be defined from the keyboard.

NONDISPLAYABLE CHARACTERS AND MISCELLANEOUS INFORMATION

When ASCII control characters (less than decimal 32) are sent to the TM27, they are not shown on the display. A function message may be any ASCII character greater than decimal 31.

DETAILED KEY DESCRIPTIONS

NUMERIC KEYS

These keys are used for data input from the keyboard. Characters enter the display in the left-most position. After eight characters have been pressed (nine characters including one decimal point) the display is full.

FUNCTION MESSAGE KEYS

These keys are used to input function messages from the keyboard. The function message may be one of the default letters A through F or it may be one RAM based user-defined character. When no user-specified character definition has been provided, the one character default letter A-F appear. For output, the default letter will be transmitted unless the host has defined the function character. In this case the character will be transmitted as defined.

The six function characters are put in the buffer by pressing the A through F keys.

RESET

The RESET key allows the TM27 operator to initialize the internal functions. Pressing RESET is equivalent to turning on the power. Pressing RESET will cause RAM based message definitions to be initialized to the power-up default characters. A "0." will be displayed in the left-most display position. This key may be disabled at installation.

ENTER KEY

ENTER is used to enable transmission with a trailing carriage return.

CLEAR

Pressing CLEAR causes the current data in the display to be cleared. Function LED's and defined function messages are unaffected. If no input message is waiting for display, a "0." appears in the left-most display position in the response to pressing CLEAR.

APPLICATIONS

COMMUNICATIONS PROTOCOL

CHARACTER CODES

The TM27 sends and receives 7-bit, asynchronous ASCII character codes with a start bit, one parity bit (either even/odd parity or marking), and at least one stop bit. When in marking state, the parity bit is ignored while receiving, but is set to a logic 1 while transmitting. Characters with parity error are ignored without notifying the host computer. P1 jumpers select the data receive and transmit rate. This rate may be 300, 1200, 2400 or 4800 bits per second. P1 jumpers are described in the Installation section.

Function codes are transmitted as defined or default to the letters A through F.

Upon power-up or reset, function keys default to A through F, the keyboard is unlocked, and the display contains "0". ASCII codes less than 20 (hexadecimal) (32 decimal) are not displayed if part of a message. Other codes that are sent as part of a message but not defined in the character set of this terminal have no defined indicator and may appear in the display in any form. To insure that the display does not contain meaningless patterns, the user must make sure only codes defined in the character set are transmitted as part of a message.

Examples of compatible host to TM27 connections:

HOST	TM27
1. 7 bits + 2 stop bits	7 bits + mark + 1 stop bit
2. 7 bits + parity + 1 stop bit	7 bits + parity + 1 stop bit
3. 7 bits + parity + 2 stop bits	7 bits + parity + 1 stop bit
4. 7 bits + mark space + 1 or 2 stop bits	7 bits + mark + 1 stop bit

Remember that since communications are asynchronous and the standby state is the marking state, extra stop bits and marking bits are always acceptable. When parity is disabled, the TM27 does not test for parity bit mark or space on input.

CARRIAGE RETURN

For an input message, the TM27 requires that the message be terminated by a carriage return. Carriage return is not counted as one of the input characters.

FUNCTION MESSAGES

Function messages 1-character in length may be defined by sending XX(ESC)Dz(a)(CR). The z represents the function message number 1 through 6. The "a" represents any ASCII character greater than decimal 32. Defined messages may be deleted by sending a new definition or XX(ESC)Dz(CR). XX(ESC)D0(CR) deletes all function message definitions. XX is the two-digit address between 00 and 63. The display buffer shows the defined function character when a definition is present in RAM. The defined function message is transmitted on output. When no message has been defined, A through F is shown in the display.

COMMAND DESCRIPTIONS

The TM27 accepts 12 different types of Escape (ESC) sequences which serve as special commands to the TM27. These commands consist of character strings starting with the 2-digit address followed (shown as XX below) by the ASCII control character (ESC) and terminated with a carriage return (CR). Intervening characters form the particular command. XX is a decimal number from 00 to 63.

XX(ESC)A(CR)
The A command polls the TM27 for any new output message which has been entered from the TM27 keyboard. This command may be used only once per message. If another A command is sent before a new message is ready, XX(CR) will be the reply indicating an empty buffer.

XX(ESC)B(CR)
The B command polls the TM27 for a message in its output buffer. It may be used to cause the TM27 to transmit one entered message any number of times until new data is entered from the keyboard.

XX(ESC)C(CR)
The C command will clear the input buffer allowing for the input of new data regardless of the previous contents of the buffer.

XX(ESC)Dz(a)(CR)
The D command used with a message is used to define function characters in the TM27's RAM. The z can be any number character from 1 through 6 for function characters 1 through 6. When "a" is not included in the escape sequence, the z function message definition is deleted. If z equals 0, all function message definitions are deleted. When function messages are deleted from RAM, they assume the default values A through F. "a" must be an ASCII code above decimal 32.

XX(ESC)EYn(CR)
The E command controls the function lights: when n=1, turn on function light; when n=0, turn off function light. Y is the number of the function light. Only values of Y from 1-5 are valid arguments, all others are ignored.

XX(ESC)Hp(CR)
Parity control. For p=0, marking; for p=1, odd parity; p=2, even parity. Default is marking parity.

XX(ESC)Jn(CR)
The J command will lockout keyboard entry (n=1) until it is turned off (n=0) or reset occurs.

XX(ESC)K(CR)
The K command transmits the contents of the input buffer. This permits comparison between what the terminal has received and what the host has sent as a check on communications lines and circuits.

XX(ESC)LD(CR)
The L command controls turnaround delay. D is in the range of 1 to 9, corresponding to 10msec to 90msec turnaround delay. Default is 10msec.

XX(ESC)N(CR)
The N command reads the three TTL inputs. The TM27 response is XXr(CR) where r is a value between 0 and 7. r is the octal representation of the three digital inputs (I1, I2, I3).

r	I3	I2	I1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

XX(ESC)T(CR)
The T command effectively resets the terminal. All buffers are cleared, the display is reset, function lights are turned off, and keyboard activity is interrupted. Function definitions are not altered and the keyboard will not be unlocked if previously locked.

XX(ESC)U(CR)
The U command combines the operation of the A command and the N command. The U command polls the TM27 for any new output message that has been entered from the keyboard and also reads the three TTL inputs. The TM27 response to the U command is XX(MESSAGE)(CR)XXr(CR). XX is the 2-digit address of the TM27. r is a value between 0 and 7. r is the octal representation of the three binary inputs (b1, b2, b3) as described above.

PROTOCOL

Computer to Terminal

XX(message(CR)	Input (message) for display
XX(ESC)A(CR)	Transmit request
XX(ESC)B(CR)	Retransmit request
XX(ESC)C(CR)	Clear input buffer
XX(ESC)DZa(CR)	Define function as "a"
XX(ESC)DZ(CR)	Clear function
XX(ESC)DO(CR)	Delete all function messages
XX(ESC)EYn(CR)	Function light and TTL output Y control
XX(ESC)Hp(CR)	Parity control
XX(ESC)Jn(CR)	Keyboard lock control
XX(ESC)K(CR)	Remote enter
XX(ESC)LD(CR)	Turnaround delay
XX(ESC)N(CR)	Read TTL inputs
XX(ESC)T(CR)	Clear all
XX(ESC)U(CR)	Reads transmit buffer and TTL inputs

Terminal To Computer

XX(MESSAGE)(CR)	Response to (ESC)A,B,K commands
XX(CR)	Response to (ESC)A,B,K commands if buffer is empty
XXr(CR)	Response to N command

NOTES:
1. XX are any decimal digits. Only multidrop addresses in the range from 00 to 63 have any significance. 00 as an address is special in that any and all terminals will respond regardless of their preset address. Caution, all terminals will transmit a message if polled with address 00, thus if more than one terminal is on the loop a polling command with address 00 should not be transmitted.
2. Function definition "a" limited to one character (any ASCII code above decimal 32 acceptable).
3. n=0 is off (disable feature) n=1 is on (enable feature).
4. Parity p is 0 to 2.
5. Y is a number from 1 to 5.
6. D is turnaround delay. Values of 1 to 9 are valid.
7. Z is a number from 1 to 6.

INSTALLATION

The TM27 is connected to a flat panel surface with six #4-40, 7/16-inch machine screws using the mechanical dimensions given in the Specifications section. A connector cutout should be provided as indicated in the Mechanical Dimensions illustration.

BACK PANEL CONNECTIONS

The front panel RESET key is disabled until RESET IN and RESET OUT are connected by a soldered jumper on the back panel mating connector.

Figure 1 shows the 26-pin connector P1. Table I is a listing of pin functions for connector P1, Table II is the baud rate table, and Table III is a listing of Polling Addresses.

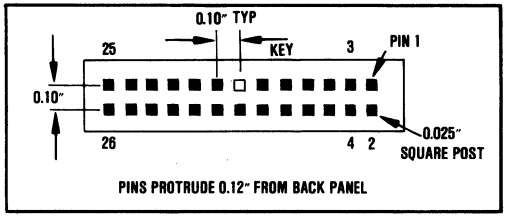


FIGURE 1. 26-pin Connector P1 Back-Panel View.

TABLE I. List of Connector P1 Pins.

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	14	I3 (Digital IN)
2	+POWER SUPPLY	15	L4 (Digital Out)
3	+OUT (RS-422)	16	RESET OUT
4	L1 (Digital Out)	17	L5 (Digital Out)
5	-OUT (RS-422)	18	A0
6	L2 (Digital Out)	19	A5
7	-IN (RS-422)	20	A1
8	I1 (Digital In)	21	A4
9	+IN (RS-422)	22	A2
10	I2 (Digital In)	23	B0
11	L3 (Digital Out)	24	A3
12	RESET IN	25	B1
13	GROUND	26	GROUND

TABLE II. Baud Rate Selection.

BAUD RATE	B1	B0
300	1	1
1200	1	0
2400	0	1
4800	0	0

1 = connect to power supply.
0 = connect to ground.

TABLE III. Polling Address Selection.

POLLING ADDRESS	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	
0	0	0	0	0	0	0	Universal
1	0	0	0	0	0	1	Address
2	0	0	0	0	1	0	
3	0	0	0	0	1	1	
4	0	0	0	1	0	0	
5	0	0	0	1	0	1	
6	0	0	0	1	1	0	
7	0	0	0	1	1	1	
8	0	0	1	0	0	0	
9	0	0	1	0	0	1	
10	0	0	1	0	1	0	
11	0	0	1	0	1	1	
12	0	0	1	1	0	0	
13	0	0	1	1	0	1	
14	0	0	1	1	1	0	
15	0	0	1	1	1	1	
16	0	1	0	0	0	0	
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
•	•	•	•	•	•	•	
63	1	1	1	1	1	1	

1 = connect to power supoply.
0 = connect to ground.

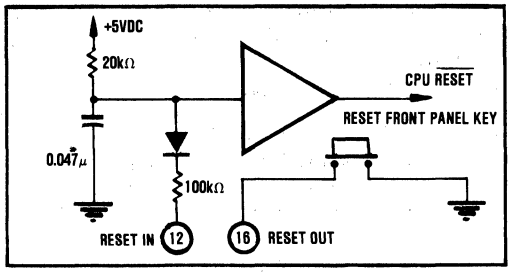


FIGURE 2. Reset in and Reset Out Equivalent Circuit.

POWER SUPPLY

The power supply voltage range accepted by the TM27 is 8VDC to 12VDC. The power supply voltage is this wide a range to allow straightforward distribution of low voltage operating power. Above 40°C, the maximum power supply voltage applied to the TM27 is linearly derated to 10VDC at 60°C.

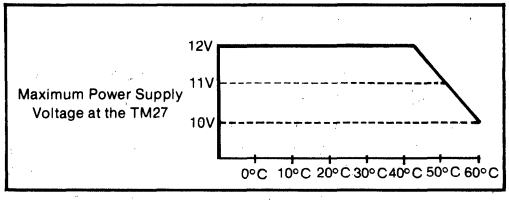
The 8VDC to 12VDC range allows for use of a power supply with little regulation and/or for the power supply voltage drop of the power lines. The length of line from the power supply to the TM27 determines the voltage drop. The voltage at the TM27 must not be less than 8VDC. For example, the resistance of wire 1mm in diameter (#18AWG) is 4Ω per 100-meter loop (8Ω for a 600-foot loop). The TM27 typically draws 0.25A. The voltage drop caused by the current is 1V (4Ω x 0.25A) per 100-meter loop (2V for a 600-foot loop). The resistance and voltage drops of wire 2mm in diameter (#12AWG) is one-fourth of the above numbers. With a 12VDC power supply, the wire resistance voltage drop must be limited to 4V or less. Therefore, with one TM27, a 400-meter (1200-foot) loop of 1mm diameter (#18AWG) copper wire is the longest run possible. If 2mm diameter (#12AWG) wire is used, the distance can be four times as great: 1600 meters (4800 feet). If more than one TM27 is powered from the same power supply and on the same wire, the length of wire is reduced proportionally. Therefore, with two TM27's in basically the same location, the length of power supply wire is reduced to one-half.

The following chart indicates the maximum length of power supply wire possible with specific numbers of TM27's at the end of the wire assuming a 12VDC power supply. Each TM27 is assumed to draw 0.25A.

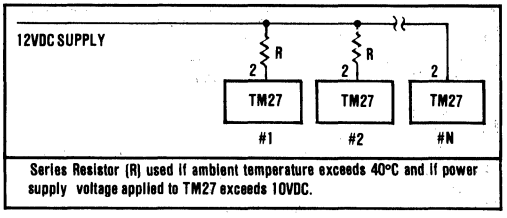
NUMBER OF TM27's	SIZE OF WIRE		
	2mm (#12AWG)	1mm (#18AWG)	0.5mm (#24AWG)
1	1600m/4800'	400m/1200'	100m/300'
2	800m/2400'	200m/600'	50m/150'
4	400m/1200'	100m/300'	25m/75'
10	160m/480'	40m/120'	10m/30'
20	80m/240'	20m/60'	5m/15'

Maximum power supply wiring distance.

The maximum power supply voltage applied to the TM27 should be linearly derated from 12VDC at ambient temperatures of 40°C to 10VDC at 60°C as shown below:



If the power supply voltage applied to a TM27 exceeds the recommended levels shown above a resistor must be inserted in series with pin 2 to reduce the power supply voltage at the terminal as shown below:



The series resistance value (R) should typically be a 5Ω resistor to reduce the power supply voltage by up to 1V or a 10Ω resistor to reduce the voltage by up to 2V. In the example above, assume the power line voltage drop to units #1 and #2 is approximately 1V with a 12VDC power supply; this means that the voltage applied to these units is about 11V. Therefore, a 5Ω resistor should be used to provide another 1V drop to each TM27 if the ambient temperature exceeds 40°C. With unit #N, however, assuming the power line voltage drop is 3V, the power supply voltage applied to the TM27 is 9VDC and no series resistor is required at any temperature.

SPECIFICATIONS

DISPLAY

Number of Characters	8
Internal Buffers:	
Input Buffer	8 Characters
Output Buffer	8 Characters
Type of Digit Display	7 Segment LED
Character Height	7.6mm (0.3")

FUNCTION LIGHTS

Host-Controlled Lights	5
Type of Light	Red, LED

KEYBOARD

Type of Keyboard	Numeric, A-F
Number of Function Keys	6
User-Programmable	Yes, One Character Each

MATERIALS

Front Panel	Polycarbonate
Back Panel	Black Anodized Aluminum
Case	ABS Plastic
The front panel will be attacked by these chemicals:	Chlorinated Hydrocarbons Fluorinated Hydrocarbons PVC Plasticizing Agents Amines

DO NOT USE FLUOROCARBONS (TMC, FREON, ETC.) TO CLEAN!

DIGITAL OUTPUTS

Digital Outputs	5 at 1LSTTL Load TTL-Compatible

SERIAL INTERFACE

Conditioning	RS-422 Signal Levels	
	Mark	Space
Transmit	(Logic 1)	(Logic 0)
+OUT (pin 3)	0V	+5V
-OUT (pin 5)	+5V	0V
Receive		
-IN (pin 7)	0V	+5V
+IN (pin 9)	+5V	0V

Baud Rate	300, 1200, 2400, 4800
Parity Bit	Even, Odd, Mark
Number of Terminals per Serial Interface	1 to 63
Communications Delay	1msec between messages
Maximum Transmission Distance	
RS-422	1200 meters (4000 feet)

TEMPERATURE RANGE

Operating	0°C to +60°C*
Storage	0°C to +60°C

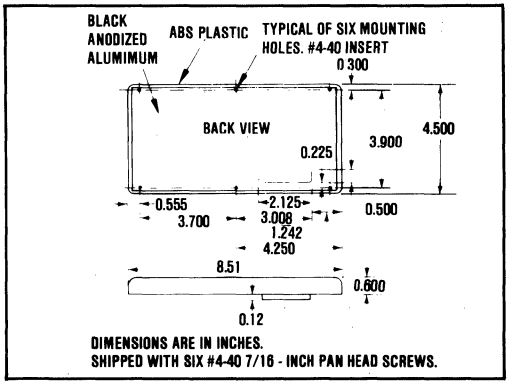
POWER SUPPLY

Voltage Range	
0°C to +40°C	8VDC to 12VDC
+40°C to +60°C	8VDC to 10VDC*
Current	250mA typical 300mA max

WEIGHT 290 grams (10 oz.)

*between +40°C and +60°C the maximum applied power supply voltage should be linearly derated from 12VDC to 10VDC.

MECHANICAL DIMENSIONS



OPTIONS

None

ACCESSORIES

26-pin Mating Connector - 2026MC

ORDERING INFORMATION

TM27 is the full part number for the TM27

APPENDIX

ASCII AND DISPLAYABLE CHARACTERS

The ASCII coded character set is to be used for the general interchange of information among information processing systems, communications systems, and associated equipment. The characters to the right of the slash are the characters which are displayable by the TM27. Transmitting nondisplayable characters from columns 2 through 7 to the TM27 will cause unpredictable characters to appear. Characters from columns 1 and 2 transmitted to the display will be ignored except for Escape (27 decimal) and Carriage Return (13 decimal).

b7 / b6 / b5 / Bits					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4	b3	b2	b1	COLUMN → / ROW ↓	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP / SPACE	0 / 0	@ / a	P / P	' / '	p
0	0	0	1	1	SOH	DC1	!	1 / 1	A / A	Q	a	q
0	0	1	0	2	STX	DC2	" / "	2 / 2	B / b	R / r	b / b	r / r
0	0	1	1	3	ETX	DC3	#	3 / 3	C / C	S / S	c / c	s
0	1	0	0	4	EOT	DC4	$	4 / 4	D / d	T	d / d	t
0	1	0	1	5	ENQ	NAK	%	5 / 5	E / E	U / U	e	u / u
0	1	1	0	6	ACK	SYN	&	6 / 6	F / F	V	f	v
0	1	1	1	7	BEL	ETB	' / '	7 / 7	G / G	W	g	w
1	0	0	0	8	BS	CAN	(	8 / 8	H / H	X	h / h	x
1	0	0	1	9	HT	EM	)	9 / 9	I / I	Y	iy	y
1	0	1	0	10	LF	SUB	*	:	J / J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[/ [	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l / l	|
1	1	0	1	13	CR	GS	- / -	= / =	M	] /]	m	}
1	1	1	0	14	SO	RS		>	N / N	^	n / n	~
1	1	1	1	15	SI	US	/	?	O / O	— / _	o / o	DEL

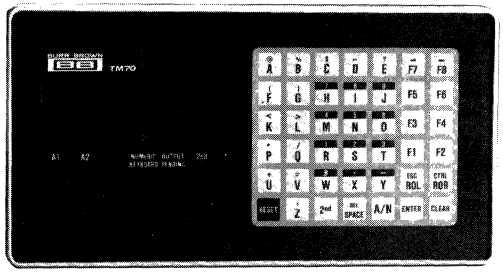
Control (CTRL) characters, i.e., CTRLX is CAN, etc.

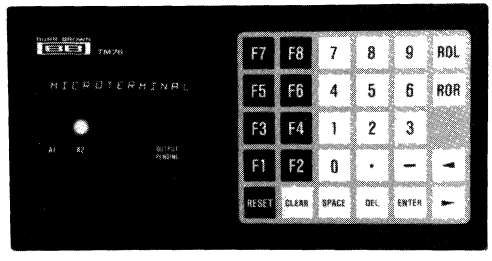
DECIMAL EQUIVALENTS OF ASCII CHARACTERS

Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic
000	NUL	022	SYN	044	,	066	B	088	X	110	n
001	SOH	023	ETB	045	–	067	C	089	Y	111	o
002	STX	024	CAN	046	.	068	D	090	Z	112	p
003	ETX	025	EM	047	/	069	E	091	[	113	q
004	EOT	026	SUB	048	0	070	F	092	\	114	r
005	ENQ	027	ES	049	1	071	G	093	]	115	s
006	ACK	028	FS	050	2	072	H	094	^	116	t
007	BEL	029	GS	051	3	073	I	095	—	117	u
008	BS	030	RS	052	4	074	J	096	`	118	v
009	HT	031	US	053	5	075	K	097	a	119	w
010	LF	032	SP	054	6	076	L	098	b	120	x
011	VT	033	!	055	7	077	M	099	c	121	y
012	FF	034	"	056	8	078	N	100	d	122	z
013	CR	035	#	057	9	079	O	101	e	123	{
014	SO	036	$	058	:	080	P	102	f	124	¦
015	SI	037	%	059	;	081	Q	103	g	125	}
016	DLE	038	&	060	<	082	R	104	h	126	~
017	DC1	039	'	061	=	083	S	105	i	127	DEL
018	DC2	040	(	062	>	084	T	106	j		
019	DC3	041	)	063	?	085	U	107	k		
020	DC4	042	*	064	@	086	V	108	l		
021	NAK	043	+	065	A	087	W	109	m		

LF = Line Feed, FF = Form Feed, CR = Carriage Return, DEL = Rubout.

TM70 AND TM76 MICROTERMINALS USER'S GUIDE





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PDS-448

TABLE OF CONTENTS

INTRODUCTION

If your system's data entry/control/display requirements are sophisticated but limited in volume, you don't need to buy big, expensive, and fragile CRT's or printing terminals to do the job efficiently.

The TM70 "microterminal" features a full alphanumeric keyboard and display while the TM76 has an alphanumeric display and a simplified numeric keyboard with larger keys. The TM70 and the TM76 - uniquely flexible in application versatility - are designed expressly to fill the human interface demands of widely dispersed control and communications networks - in machine and process control, energy management systems, inventory control and factory floor data collection, and information processing. Microterminals, because of their interface flexibility, appearance, size, durability, and easy installation, function equally well as consoles and control centers for instruments and small systems. They also perform as I O terminals in diagnostic applications.

You don't need interface expertise to put microterminals to work for you...they communicate in serial ASCII with RS232C or 20mA current loop conditioning. Baud rates are 300 or 1200 bits per second.

A tough, water resistant front panel protects LED displays and indicators as well as a full alphanumeric keyboard. Tactile feedback, display blinking, and character display confirm operator entry and, because of its design simplicity, the microterminal concept doesn't require special operator skills or training. Depressing a single function key initiates preprogrammed action by the CPU. These functions may be defined in your CPU's software.

These microterminals' very compact design and simple mounting on any flat surface make them quickly adaptable to new or existing applications. All models measure only 216mm × 114mm x 15mm (8.5" x 4.5" x 0.6"). When ordered in OEM quantities the front panel can contain your corporate or system logo.

You can enter and display alphanumeric data. A 42-key keyboard (shiftable to generate 52 characters including A-Z and 0-9) allows you to receive or enter messages up to 36 characters long. A 12-character display - with horizontal scroll-left or scroll-right keyboard controls - permits review and editing of data entered before transmission in the polled mode. A 36-character message buffer is provided to hold output and input messages.

Display features include CPU control of scrolling. The keyboard can also be locked out by CPU command. Two LED indicators (A1, A2) are independently controlled by the CPU, three LED's indicate terminal status. The two independent LED's are driven by open-collector TTL signals which are also available on the back panel connector. These may be used to remotely control external equipment such as audible annunciators.

It is important to realize that while the microterminal products including the TM70 and the TM76 have many features, normal operation is very uncomplicated. Virtually untrained operators can use the microterminal products productively. Most special features are invisible to the operator. A typical application consists of a series of host-system-supplied operator prompts. To each prompt, the operator simply keys in a short number or message and pushes the ENTER key. The function message keys may be used to further simplify operator responses.

OPERATION

TM70 GENERAL DESCRIPTION

The TM70 is an alphanumeric "microterminal" which may be used as a remote or local data entry and output terminal for a host computer system. It is intended to provide a low cost, small size, alternative to a CRT terminal. It is suitable for applications with a limited amount of data interchange, as compared to applications requiring a typewriter-style keyboard and multiline display or hard copy output. The TM76 is the same as the TM70 with the exception that it features a simplified numeric-only keyboard with larger keys.

The TM70 features a dust proof front panel including 52 characters on a 42-key keyboard, 12-character alphanumeric display, two host-computer-controllable light emitting diodes (LED's), and three status LED's. The keyboard features raised embossing with tactile feedback. In addition, a 25-pin, D-style, rear panel connector features RS232C and current loop data transmit and data receive. The connector is also used to provide power, communications rate selection (300 or 1200 bps), remote reset in and reset out, and parity selection. The host-controllable LED's, labeled A1 and A2 on the front panel, are driven by open collector TTL signals which are brought out to the back panel connector.

Up to eight 4-character function messages may be defined by the host system. After definition by the host, these messages are called by the host for display by sending a 2-character code (ESC) *r*; where *r* may have the values 1 through 8. Function messages may be retransmitted to the host by pressing the front panel function message keys. Thus, they may be used as extensions of the input message to the TM70 or as function messages to be transmitted by the TM70 operator to the host system.

For all following descriptions the terms input and output shall refer to input to and output from the TM70. Internal operation of the TM70 is easily conceived as a 12-character display and 36-character message buffer. The display may be filled, under operator control, with any contiguous 12-character section of the message buffer. Display contents are displayed to the operator through 12 alphanumeric LED characters. A host-sent command may be used to cause the 36-character message to continuously scroll across the display. The message buffer is handled differently in nonpolled mode than in polled mode. Nonpolled mode and polled mode operation are described in the following paragraphs.

NONPOLLED OPERATION

In nonpolled operation as each character key is pressed, it is immediately transmitted without being displayed. Therefore, it is necessary for the host to echo the key to

the terminal for display.
The ENTER key will transmit the ASCII CR (carriage return) character. Nonpolled operation is similar to the operation of a standard CRT terminal.

POLLED OPERATION

In multidrop mode, as each key is pressed, it is entered into the buffer and the display and not transmitted. The host cannot echo characters in this mode. When the ENTER key is pressed, the buffer is made ready for transmission, as indicated by the OUTPUT PENDING status LED. When the host sends the polling command ('Request Buffer') while OUTPUT PENDING is on, the TM70 will begin to transmit the buffer to the host. The buffer is prefixed by its 2-digit address to verify the source of the message.

In the event there was an error in the transmission (wrong address, parity error, etc.), the buffer can be requested again by the "Retransmit Buffer" command. If the "Request Buffer" command had been sent again, a null message would be transmitted to indicate no new data had been entered. This distinguishes between repeated data and new data.

When the host sends messages or commands to the TM70, they must be prefixed by two ASCII digits in the range 00 to 15. Address 00 is a special case which is accepted by all terminals addressed from 01 to 15. This allows a single message to be received by all terminals on the multidrop line at the same time.

The 20mA current loops should be used in polled operation. See page 7 for suggested connections. A number of microterminals may be connected to a single communications port using the current loops. The number may be limited to less than 15 by electrical considerations on some circuits. At 10mA the forward drop across the output optical coupler transistor is 1.3V. Fifteen of these total 19.5VDC. If the host current source comes from +12VDC, this obviously won't work. If -12VDC is available, 15 units can be connected as shown in Figure 5.

TM76 GENERAL DESCRIPTION

The TM76 is intended for those applications where an alphanumeric display terminal with numeric and function key data input is adequate. The TM76 keyboard has the advantage that it is less complicated for the untrained or inexperienced operator.

The TM76 is functionally identical to the TM70 except for the keyboard functions. The TM76 has larger, but fewer keys than the TM70. The TM76 offers a numeric (0-9) keyboard with function keys. Keyboard functions of the TM70 which do not appear on the TM76 are not available. The numeric keyboard and 2nd lights are unnecessary and have been deleted. Figures 1 and 2 show the front panels of the TM70 and TM76.

The keys of the TM76 are 38% larger and placed on 0.65-inch centers as compared to the 0.5-inch centers of the TM70. This is the same spacing as used on touch tone telephones and allows operators with gloved hands to easily use the keyboard. As can be seen from Figures 1 and 2, the keyboard appears much larger and easier to use. For a description of the TM76 key functions, refer to those same keys described for TM70 in the Detailed Key Descriptions section.

All matters concerning control features, communications protocol, and product specifications not related to the keyboard are as for TM70.

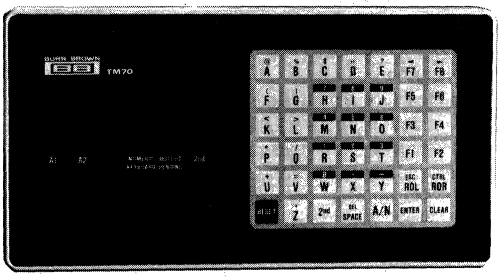


FIGURE 1. TM70 Front Panel.

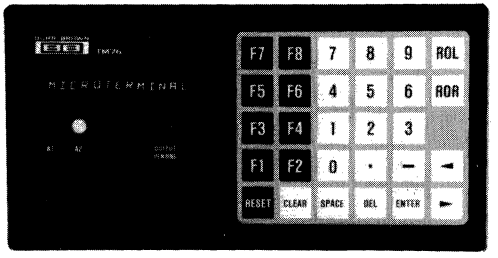


FIGURE 2. TM76 Front Panel.

SELF-TEST MODE

The TM70 has provision for performing a self-test diagnostic routine. Self test is entered by holding down any key while RESET is pressed and released. The message 'RAM␣ROM␣I/O␣' is put in the display buffer and the write/read memory test is performed. If the memory test passes, a '+' is put after 'RAM'; if there was a failure, a '—' is put in the display.

Similarly, a program ROM checksum is calculated and compared with a ROM stored checksum. The same pass/fail indicator is displayed. The I/O is tested by a write/read cycle to the internal I/O device, and a rotating test is performed on the Status LED's.

This sequence is then repeated until RESET is pressed and released while no other key is pressed. This will allow the TM70 to perform a normal power-up. The TM70 is off-line and will not receive or transmit while in self-test mode.

Self test can be accomplished only if the back panel connector reset jumper is connected between pins 19 and 21.

OPERATING INSTRUCTIONS

READY CONDITION

When power is applied to the TM70, the display will show

the ready indicator, which is a ^ in the left-most character position. In addition, pressing RESET and CLEAR will cause the ready condition to be entered. Note that in some installations the RESET key may be disabled when the unit is installed.

RECEIVING AN INPUT MESSAGE

When the TM70 receives an input message, it will appear in the display from left-to-right until the 12-character display is filled. After 12 characters the message will scroll to the left as each character is received. The internal message buffer holds up to 36 characters. For input messages larger than 36 characters, only the first 36 characters are retained. The host system must terminate each input message with a carriage return (CR). The carriage return is not displayed in any way. When the carriage return is received, the display will be reloaded with the first 12 characters of the message. In most installations this will appear to happen instantaneously. When an input message has been received, it may be examined by using the message control keys ROL, ROR, ◄, and ►. These cause a message up to 36 characters in length to move left and right in the 12-character display. Their functions are further described in the detailed key descriptions.

Receipt of another character after (CR) causes the display and message buffers to be cleared except for the characters of the new message. Also, if a character key is pressed to start an output message, the display and message buffer are cleared of the preceding input message. During normal operation an input message replaces any previous output message. The host may clear the display and message buffer by sending a message consisting of a single blank and a carriage return.

COMPOSING AN OUTPUT MESSAGE

As each character key is pressed, the displayed message grows from left to right. After 12 keys have been pressed, the message scrolls to the left. All characters are retained until 36 characters have been pressed. If more than 36 characters are pressed, only the first 36 are retained. The message may be edited by pressing CLEAR and inputting the message again or by using the delete key, DEL. Note that upper labels are entered by first pressing 2nd, prior to each upper label. When the operator wishes to end the message, it is only necessary to press ENTER. When the ENTER key is pressed at the end of the line, the next character entered will cause the message and display buffers to be cleared except for the first character of the new line.

FUNCTION KEYS

The host system may define up to eight 4-character function messages to be stored in TM70 random access memory. The operator may send these to the host by pressing the F1 through F8 keys. When F1 through F8 are pressed prior to being defined by the host, &z (z = 1 through 8) is transmitted. Function messages may not be defined from the keyboard.

NONDISPLAYABLE CHARACTERS AND MISCELLANEOUS INFORMATION

When nondisplayable ASCII characters are sent to the TM70, they are not shown on the display. However, function messages may contain nondisplayable characters, which will be transmitted correctly but displayed as # when buffered in multidrop mode. This applies to all 128 characters of the ASCII set.

The decimal point takes a full character position.

DETAILED KEY DESCRIPTIONS

ALPHABET AND SPECIAL CHARACTER KEYS [A] [B] etc.

These keys are used for data input from the keyboard. To enter the upper character, press the 2nd key prior to each upper character. Characters enter the display in the left-most position. After 12 characters have been pressed, previous characters move one character position to the left when a new character is entered.

ALPHABET AND NUMERIC KEYS [T] [Y] etc.

These keys are used to enter characters from the keyboard. The upper characters are entered by pressing 2nd prior to each upper character. This is called the Alpha mode. An alternate mode is called Numeric mode. In this mode these upper characters may be entered by only pressing the key. In the Numeric mode pressing 2nd first will cause the lower character to be entered. The keyboard is put in Numeric mode by pressing the A N key. The Numeric Keyboard LED is on while the keyboard is in Numeric mode. To exit Numeric mode press A N again. Alpha mode is the power-up and Reset mode.

FUNCTION MESSAGE KEYS [F1] [F2] etc.

These keys are used to input function messages from the keyboard. The function message may be one of the default strings &z or it may be a RAM based user defined string. When no user specified string definition has been provided, the two characters of the default string appear. For a user defined value, the one to four characters of the string definition appear in the display. The z denotes 1 through 8 for function messages 1 through 8.

All function messages are transmitted to the TM70 on the communications line as (ESC)z. For output, the default string will be transmitted unless the host has defined the function message. In this case the message will be transmitted as defined.

The eight function messages are put in the buffer by pressing the F1 through F8 keys or by the host transmitting (ESC)z.

When no message has been defined by the host, default strings appear in the display as &z. The z will be 1 through 8 for a total of eight values.

FUNCTION MESSAGE AND DISPLAY CONTROL KEYS [◄ F7] [► F8] etc.

These keys, when used as function message keys, are the same as the previously defined function keys. When used

with the 2nd key, they move the display buffer to the right-most 12 characters (◄), or to the left-most 12 characters (►), of the message buffer.

DISPLAY CONTROL AND TERMINAL CONTROL KEYS (ESC ROL) (CTRL ROR)

ROL/ROR

Pressing ROL will cause the message to move one character position to the left or until the last character of the message being examined is in the right-most position of the display. Pressing ROR causes the message to move one character to the right or until the first character of the message under examination is in the left-most display position. When held down, ROL and ROR auto-repeat.

ESCAPE

When ROL is prefixed by 2nd, the ASCII control code (ESC) is produced. In multidrop mode this is displayed as #.

CONTROL

When ROR is prefixed by 2nd, the next alphabetic character is converted to the corresponding ASCII control code which in multidrop mode is displayed as #.

RESET (RESET)

The RESET key allows the TM70 operator to initialize the internal functions. Pressing RESET is equivalent to turning on the power. Pressing RESET will cause RAM based message definitions to be initialized to the power-up default strings. The ready indicator (^) will be displayed in the left-most display position. This key may be disabled at installation. RESET is also used to enter self-test mode, see page 2.

SECOND KEY (2nd)

The second key, 2nd, is used to enable the upper labels of those keys having upper labels. For example, the key sequence (2nd) (+ U) (+ U) causes +U to be transmitted. When the keyboard is in Alpha mode as indicated by the Numeric Keyboard status LED being off, (2nd) (2 S) causes 2 to be transmitted. Pressing 2nd prior to a key which has no upper label causes the lower label to be transmitted and the internal 2nd mode cleared, as indicated by the '2nd' LED going off.

SPACE AND DELETE (DEL SPACE)

Space causes a space to be transmitted.The action of the DEL key depends on the mode. In normal mode the DEL key causes the ASCII DEL character to be transmitted when it is pressed. If the host echos the DEL back to the TM70, the last character in the buffer will be deleted. In multidrop mode the DEL key will delete the last character held in the buffer if there is one.

ALPHA/NUMERIC KEY (A/N)

Pressing the A/N key causes the keyboard to enter the Numeric mode. The upper white on black labels become lower labels not requiring the 2nd key before entry. The lower labels become upper labels and require the use of the second key for entry. The front panel Numeric LED comes on to indicate the keyboard is in Numeric mode. Press A/N to return to Alpha mode. Alpha mode is also the power-up and reset mode.

ENTER KEY (ENTER)

ENTER is used to terminate an output message with a carriage return in normal mode and to enable transmission with a trailing carriage return in multidrop mode. See also the sections on Polled and Nonpolled Operation.

CLEAR (CLEAR)

Pressing CLEAR causes the message buffer and display to be cleared. The Numeric Keyboard LED goes off meaning the terminal is in Alpha mode. A1, A2 LED's and defined function messages are unaffected. RESET has the same function as CLEAR, but in addition clears A1, A2 LED's and defined function messages. The ready indicator (^) is displayed in the left-most display position in response to pressing clear.

APPLICATIONS

COMMUNICATIONS PROTOCOL

CHARACTER CODES

The TM70 sends and receives 7-bit, asynchronous ASCII character codes with a start bit, one parity bit, and two stop bits. One, one and one-half, or two stop bits will be accepted for input. When parity is disabled, a mark or space, as determined by P1 jumpers, is inserted for the parity bit. Parity may be even or odd and is selected by jumpers on P1. Characters with parity errors are displayed as #. These jumpers also select the data receive and transmit rate. This rate may be 300 or 1200 bps. P1 jumpers are described in the Installation section.

Examples of compatible host to TM70 connections:

Host	TM70
1. 7 bits + 2 stop bits	7 bits + mark + 2 stop bits
2. 7 bits + parity + 1 stop bit	7 bits + parity + 2 stop bits
3. 7 bits + parity + 2 stop bits	7 bits + parity + 2 stop bits
4. 7 bits + mark space + 1 or 2 stop bits	7 bits + mark space + 2 stop bits

Remember that since communications are asynchronous and the standby state is the marking state, extra stop bits and marking bits are always acceptable. The TM70 does not test for bit 8 mark or space on input.

CARRIAGE RETURN

For an input message, the TM70 requires that the message of up to 36 characters in length be terminated by a carriage return. Carriage return is not counted as one of the input characters.

FUNCTION MESSAGES

Function messages of up to four characters in length may be defined by sending (ESC) D z(MESSAGE)(CR). The

z represents the function message number 1 through 8. Defined messages may be deleted by sending a new definition or (ESC) D z(CR). (ESC) D 0(CR) deletes all function message definitions.

To call a function message, the host sends (ESC) z within a normal message or merely (ESC) z (CR). This causes the function message to be entered into the 36-character message buffer. The display buffer shows the defined function message when a definition is present in RAM. The defined function message is transmitted on output. When no message has been defined, &z is shown in the display. &z is also transmitted in an output message when no function message has been defined.

COMMAND DESCRIPTIONS

The TM70 accepts nine different types of Escape (ESC) sequences which serve as special commands to the TM70. These commands consist of character strings starting with the ASCII control character (ESC) and terminated with a carriage return (CR). Intervening characters form the particular command.

(ESC) A (CR)

The A command polls the TM70 for any new output message which has been entered from the TM70 keyboard. This command may be used only once per message.

(ESC) B (CR)

The B command polls the TM70 for any new or old message in its output buffer. It may be used to cause the TM70 to transmit one entered message any number of times.

(ESC) Dz (MESSAGE) (CR)

The D command used with a message is used to define function messages in the TM70's RAM. The z must be any number character from 1 through 8 for function messages 1 through 8. When the MESSAGE is not included in the escape sequence, the z function message definition is deleted. If z equals 0, all function message definitions are deleted. When function messages are deleted from RAM, they assume the default values &z.

(ESC) En (CR)

This command is used to set the A1 LED on or off. If n = 1, the LED is turned on. It is turned off for n = 0. The back panel A1 TTL output is pulled low when the LED is on.

(ESC) Fn (CR)

This command serves for A2 as the previous E command does for A1.

(ESC) Gn (CR)

When n = 1 the display continuously scrolls through the message buffer. Scrolling is stopped with n = 0.

(ESC) Jn (CR)

When n = 1 the TM70 keyboard is locked out. The keyboard is enabled if n = 0.

INPUT MESSAGE SUMMARY

Host CPU to TM.

(MESSAGE) (CR)	; input message
(ESC) A (CR)	; request buffer
(ESC) B (CR)	; retransmit buffer
(ESC) Dz (MESSAGE) (CR)	; define function message
(ESC) Dz (CR)	; delete function message
ESC) D0 (CR)	; delete all function messages
(ESC) En (CR)	; output to A1 LED
(ESC) Fn (CR)	; output to A2 LED
(ESC) Gn (CR)	; set scroll mode
(ESC) Jn (CR)	; set keyboard lockout

NOTE: Parenthesis are not actually encoded. Shown for copy clarity only. No imbedded blanks allowed. Lower case letters represent variables.

OUTPUT MESSAGE SUMMARY

TM to Host CPU.

(Character)	; response to pressing a key in non-polled mode.
(MESSAGE) (CR)	; response to ENTER key, (ESC) A (CR), or (ESC) B (CR).
(CR)	; response to (ESC) A (CR), when output buffer is empty or has previously been accessed with (ESC) A (CR). (ESC) B (CR) may be used to obtain previously transmitted messages. If the buffer has been cleared or reset, (CR) is transmitted in response to (ESC) B (CR).

NOTES:

1. z = function message number 1 through 8.
2. n = control character, 0 = off, 1 = on.
3. In polled mode all messages, commands, and replies will have a 2-digit address prefix (see Polled Operation section).

INSTALLATION

The TM70 is connected to a flat panel surface using six, 4-40, 7/16-inch machine screws using the mechanical dimensions given in the Specifications section. A connector cutout should be provided as indicated.

BACK PANEL CONNECTIONS

The front panel RESET key is disabled until RESET IN and RESET OUT are connected by a soldered jumper on the back panel mating connector. The communication rate may be set to 1200 bits per second by connecting pin 11 to the ENABLE pin. If pin 11 is left unconnected, the communication rate will be 300bps. Parity and word

format may be selected by connecting pins 9 to 10 to the ENABLE pin as indicated by the zeros in Table I. Logic one is obtained by leaving the pin unconnected. The format is 7 bits plus a mark, space or parity bit. Remember that the communications are asynchronous; therefore, it is always acceptable to have more than the required number of stop and/or marking bits.

Nonpolled operation is obtained by having $\overline{A0}$ through $\overline{A3}$ open. This represents address 0000. Polling address 01 is obtained by connecting $\overline{A0}$ to ENABLE.

Connector wiring for P1 (see Figure 3) may be accomplished with the aid of Tables I, II, III, and IV.

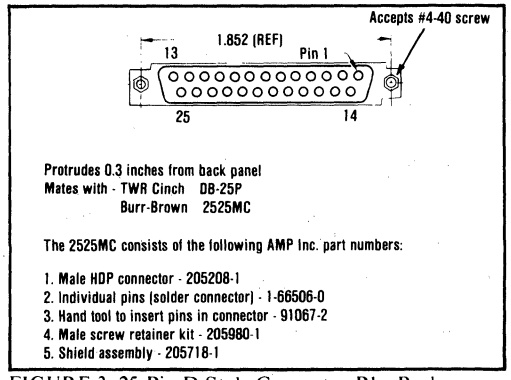


FIGURE 3. 25-Pin D Style Connector P1 - Back Panel View.

TABLE I. Setting the Parity Bit.

P1	P0	Parity Bit
0	0	Even
0	1	Odd
1	0	Space
1	1	Mark

Logic 1 is open.
Logic 0 is jumpered to ENABLE (pin 2).
Stop bits: 1, 1-1/2, or 2 bits on input
2 stop bits on output.
Parity errors displayed as $\frac{1}{4}$.
Mark/space not detected on input.
Logic 1 = Mark

TABLE II. Polling Address Selection.

Polling Address	$\overline{A0}$	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$
0	0	0	0	0 Nonpolled
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Logic 1 is jumpered to ENABLE (pin 12)
Logic 0 is open

TABLE III. Setting the Baud Rate.

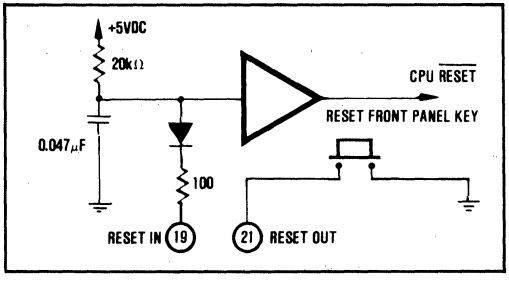
Baud Rate	B0
300	1
1200	0

TABLE IV. Listing of Connector P1 Pins.

See Note	Pin	Function	
4	1	Supply RTN	
	2	TX	RS232C
	3	RX	RS232C
5	4	REQUEST TO SEND	OUTPUT
5	5	CLEAR TO SEND	INPUT
1	6	A1 LED	
4	7	Signal Ground	
1	8	A2 LED	
	9	P0	
	10	P1	
	11	B0	
2	12	ENABLE	
	13	(NO CONNECTION)	
	14	+5VDC	
	15	-IN	20mA Current Loops
	16	+IN	20mA Current Loops
	17	-OUT	20mA Current Loops
	18	+OUT	20mA Current Loops
3	19	RESET IN	
6	20	DATA TERMINAL READY	OUTPUT
3	21	RESET OUT	
7	22	$\overline{A0}$	Polling Address
	23	$\overline{A1}$	Polling Address
	24	$\overline{A2}$	Polling Address
	25	$\overline{A3}$	Polling Address

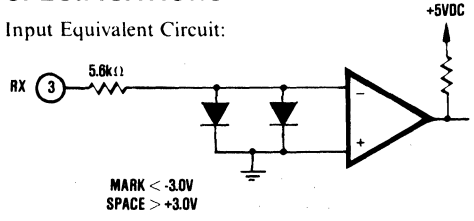
NOTES:
1. A1 and A2 are logic low (< 0.4V at 1.6mA sink) when LED is on.
2. 0 = Jumper to ENABLE (pin 12); 1 = Open, for P0, P1 and B0.
3. To enable RESET, jumper between RESET IN and RESET OUT.
4. Supply RTN and Signal RTN internally connected.
5. Pins 4 and 5 are internally connected.
6. Pin 20 is internally connected to +12V through 1500Ω.
7. Nonpolled mode is address 0000 with pins 22 through 25 open.
   1 = Jumper to ENABLE. 0 = Open.

RESET IN AND RESET OUT EQUIVALENT CIRCUIT

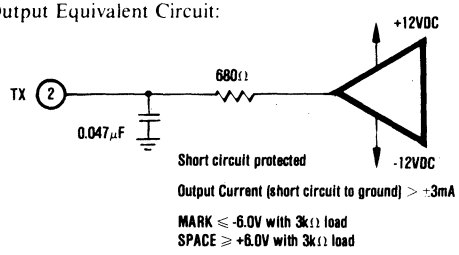


RS232C ELECTRICAL SPECIFICATIONS

Input Equivalent Circuit:



Output Equivalent Circuit:



Maximum recommended transmission distance is 15 meters (50 feet).

CURRENT LOOP COMMUNICATIONS WIRING CONNECTIONS

TM70 units may be connected to one or more hosts by using the two 20mA current loop circuits. Optical coupling devices are used to electrically isolate TM70 from these circuits. Figures 4 and 5 illustrate connections to typical host communications circuits.

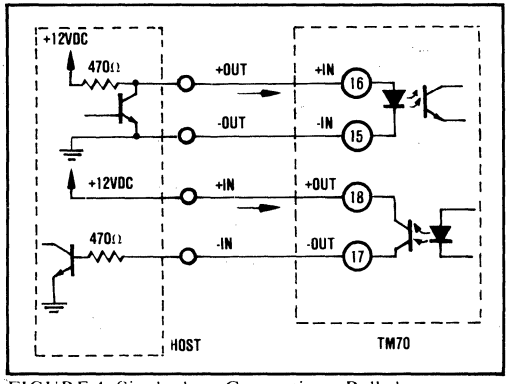


FIGURE 4. Single-drop Connection - Polled or Nonpolled Operation.

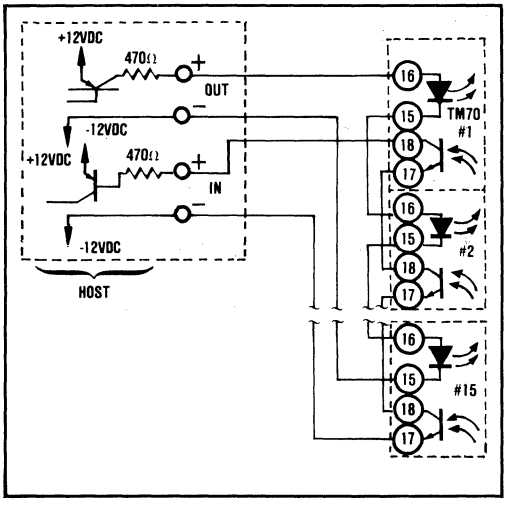


FIGURE 5. Multidrop Connection - Polled Operation.

CURRENT LOOP ELECTRICAL SPECIFICATIONS

Input Voltage Drop	≤ 1.3V at 35mA ≤ 1.2V at 20mA ≤ 1.2V at 10mA
Input Minimum Current	10mA
Input Maximum Current	35mA
Output Voltage Drop	≤ 1.3V at 10mA ≤ 1.3V at 20mA ≤ 1.4V at 35mA
Output Current Minimum	20mA

Output Voltage Drop x Output Current must be ≤ 250mV.

Output Current must be limited by the external circuit.

Maximum applied voltage is 30VDC.

Maximum recommended transmission distance is 1500 meters (5000 feet).

LOOP POWER SOURCE

A distance limitation for current loop that should be considered is the compliance of the loop power source.

The forward voltage drop across the output transistor is 1.3V maximum. The loop power source must be able to drive 1.3V plus the voltage drop produced by the resistance of the wire in the communications line.

The resistance of wire 1mm in diameter (#18AWG) is 4Ω per 100-meter loop (13Ω per 1000-foot loop). The voltage drop caused by the resistance of the wire is 0.08V per 100-meter loop (0.25V per 1000-foot loop). The resistance of wire 0.5mm in diameter (#24AWG) is 16Ω per 100-meter loop (51Ω per 1000-foot loop), so that voltage drop will increase by a factor of four. The sum of output transistor drops and wire resistance drops must be held within the compliance range of the current supplying circuit. As an example, with 10 microterminals and 1000 feet of #18AWG wire, the loop power supply must be: 10 terminals x 1.3V per terminal = 13V plus 0.25V for wiring for a total of 13.25V.

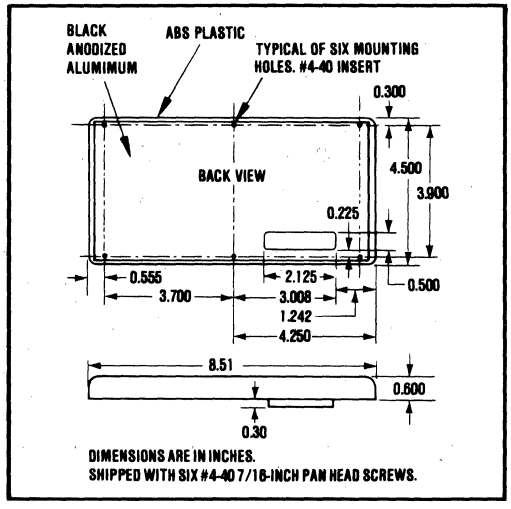
SPECIFICATIONS

DISPLAY	
Number of Characters	12, alphanumeric
Internal Buffer	36 characters
Type of Digit Display	16 segment
Character Height	3.6mm (0.14")
FUNCTION LIGHTS	
Host Controlled Lights	2
Status Lights	3/1
Type of Light	Red, LED
KEYBOARD	
Type of Keyboard	Alphanumeric/Numeric
Number of Function Keys	8
User Programmable	Yes, up to 4 characters each
MATERIALS	
Front Panel	Polycarbonate
Back Panel	Black Anodized Aluminum
Case	ABS Plastic
The front panel will be attacked by these chemicals:	Chlorinated or Fluorinated Hydrocarbons PVC Plasticizing Agents Amines

DO NOT USE FLUOROCARBONS (TMC, FREON, ETC.) TO CLEAN!

TTL OUTPUTS	
TTL Outputs	2 at 1LSTTL Load Open collector
SERIAL INTERFACE	
Conditioning	RS232C/V.24 and 20mA Current Loop
Baud Rate	300, 1200
Parity Bit	Even, Odd, Space, Mark
Number of Terminals per Serial Interface	1 to 15
Communications Delays	None - TM70/76 do not require delays between messages or commands
Maximum Transmission Distance	
RS232C/V.24	15 meters (50 feet)
20mA Current Loop	1500 meters (5000 feet)
RS232C	
Output Voltage	
Logic 1	-10VDC
Logic 0	+10VDC
Input Voltage	
Logic 1	-3VDC to +15VDC
Logic 0	+3VDC to +15VDC
20mA Current Loop	
Input	
Forward Voltage Drop	1.3V max at 30mA/1.2V max at 20mA
Output	
Saturation Voltage	1.3V max at 20mA
Breakdown Voltage	30V max
TEMPERATURE RANGE	
Operating	0°C to +60°C
Storage	0°C to +60°C
POWER SUPPLY	
Voltage	+5VDC ±5%
Current	600mA max
WEIGHT	290 grams (10 oz.)

MECHANICAL DIMENSIONS



OPTIONS

None

ACCESSORIES

25-pin Mating Connector - 2525MC

ORDERING INFORMATION

TM70 is the full part number for the TM70
TM76 is the full part number for the TM76

APPENDIX

AMERICAN NATIONAL STANDARD CODE FOR INFORMATION INTERCHANGE

This coded character set is to be used for the general interchange of information among information processing systems, communications systems, and associated equipment.

b7 b6 b5 / Bits				0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4	b3	b2	b1	COLUMN → / ROW ↓ 0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	ıy	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	|
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	—	o	DEL

Control - CTRL characters, i.e., CTRLX is CAN, etc.

DECIMAL EQUIVALENTS OF ASCII CHARACTERS

Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic
000	NUL	022	SYN	044	,	066	B	088	X	110	n
001	SOH	023	ETB	045	–	067	C	089	Y	111	o
002	STX	024	CAN	046	.	068	D	090	Z	112	p
003	ETX	025	EM	047	/	069	E	091	[	113	q
004	EOT	026	SUB	048	0	070	F	092	\	114	r
005	ENQ	027	ES	049	1	071	G	093	]	115	s
006	ACK	028	FS	050	2	072	H	094	^	116	t
007	BEL	029	GS	051	3	073	I	095	—	117	u
008	BS	030	RS	052	4	074	J	096	`	118	v
009	HT	031	US	053	5	075	K	097	a	119	w
010	LF	032	SP	054	6	076	L	098	b	120	x
011	VT	033	!	055	7	077	M	099	c	121	y
012	FF	034	"	056	8	078	N	100	d	122	z
013	CR	035	#	057	9	079	O	101	e	123	{
014	SO	036	$	058	:	080	P	102	f	124	|
015	SI	037	%	059	;	081	Q	103	g	125	}
016	DLE	038	&	060	<	082	R	104	h	126	~
017	DC1	039	'	061	=	083	S	105	i	127	DEL
018	DC2	040	(	062	>	084	T	106	j		
019	DC3	041	)	063	?	085	U	107	k		
020	DC4	042	*	064	@	086	V	108	l		
021	NAK	043	+	065	A	087	W	109	m		

LF = Line Feed, FF = Form Feed, CR = Carriage Return, DEL = Rubout.

DISPLAYABLE CHARACTERS

CHARACTER SET

D6 D5 D4 D3 \ D0 D1 D2	0 0 0	1 0 0	0 1 0	1 1 0	0 0 1	1 0 1	0 1 1	1 1 1
0 1 0 0								
0 1 0 1								
0 1 1 0								
0 1 1 1								
1 0 0 0								
1 0 0 1								
1 0 1 0								
1 0 1 1								

NOTE: All nondisplayable characters entered from keyboard are displayed as .

COMMUNICATIONS CHECKOUT PROGRAMS

The following programs are provided as examples of short programs written in high level languages which might be used to verify that a TM70 is properly connected to a computer communications port. They are not intended as full applications programs, although they might be used as seeds for the development of a particular application. The BASIC programs were tested at 300 baud. Depending upon the speed of the particular BASIC installation, the programs may or may not be able to keep up at 1200 baud. This is due to the fact that the polling program inputs and outputs one character per statement. The nonpolled BASIC program should work at the higher data rate since it receives and then echoes character-by-character as the operator presses each TM70 key. The third program is written in FORTRAN. It reads and writes entire character lines and works at higher data rates. However, it uses calls to two system programs that are available on many Digital Equipment Corporation PDP 11/34 RSX-11M systems. They are GETADR and WTQIO. GETADR finds the addresses of LINE and POL variables. WTQIO sends the polling command and reads the command immediately.

It is not intended that these programs will work in systems other than the ones for which they were written. However, programs of similar brevity should be possible with any computer system. The nonportability of the programs is due to their use of various system features. The BASIC programs use a terminal driver called AT: to initialize the communications port. The FORTRAN program uses calls to system-supplied subroutines GETADR and WTQIO.

CHARACTER ECHO FROM BASIC

```
10  OPEN "O" #1, "AT:" 'SET UP UART; AT: MUST BE LOADED FROM SYSTEM LEVEL
20  REM FILE "TM70S" USED TO VERIFY COMMUNICATIONS CONNECTION TO TM70
30  REM NONPOLLED OPERATION IS ASSUMED
40  REM
50  REM ..... MAIN PROGRAM .....
60  REM
70  REM LOOP UNTIL A CHARACTER COMES IN AND THEN ECHO THE CHARACTER
80  REM SUBTRACT 128 SINCE TM70 SETS BIT 8
90  IF(INP(229) AND 1) <> 1 THEN GOTO 150
100 C = INP(224) -128
110 OUT 224,C
120 REM DELAY TIL CHARACTER IS TRANSMITTED
130 FOR J = 1 TO 20
140 NEXT J
150 GOTO 90
160 STOP
170 END
```

The numbers 224 and 229 are I/O addresses for the communications port.

```
10  OPEN "O", #1, "AT:" SET UP THE UART; AT: MUST BE LOADED AT SYSTEM LEVEL
20  REM FILE "TM70P" USED TO VERIFY COMMUNICATIONS CONNECTION TO TM70
30  REM POLLED OPERATION ASSUMED
40  DIM C(36)
50  REM
60  REM ..... MAIN PROGRAM .....
70  REM
80  REM POLL FOR INPUT
90  GOSUB 380
100 REM GET INPUT LINE
110 GOSUB 270
120 REM PRINT INPUT LINE, BUT SUPPRESS ADDRESS AND CARRIAGE RETURN
130 FOR J = 3 TO I
140 PRINT CHR$ (C(J));
150 NEXT J
160 REM PRINT CARRIAGE RETURN IF MORE THAN ADDRESS HAS BEEN RECEIVED
170 IF(I>3) THEN PRINT CHR$(13)
180 GOTO 90
190 STOP
200 END
210 REM
220 REM ..... LINE INPUT ROUTINE .....
230 REM
240 REM TEST INPUT STATUS AND LOOP TIL A CHARACTER IS RECEIVED
250 REM SUBTRACT 128 SINCE TM70 SETS BIT 8
260 REM RETURN WHEN CARRIAGE RETURN IS FOUND
270 I = 1
280 IF(INP(229) AND 1) <> 1 THEN GOTO 320
290 C(I) = INP(224) -128
300 IF(C(I) = 13) THEN GOTO 330
310 I = I + 1
320 GOTO 280
330 RETURN
340 REM
350 REM ..... POLLING ROUTINE .....
360 REM
370 REM TRANSMIT THE SEQUENCE 01(ESC)A(CR) TO POLL TM70
380 OUT 224,48 : GOSUB 440
390 OUT 224,49 : GOSUB 440
400 OUT 224,27 : GOSUB 440
410 OUT 224,65 : GOSUB 440
420 OUT 224,13 : GOSUB 440
430 RETURN
440 REM
450 REM ..... DELAY TIL CHARACTER IS TRANSMITTED .....
460 REM
470 FOR K = 1 TO 20
480 NEXT K
490 RETURN
```

Note that the 01(ESC)A(CR) sequence is accomplished by outputting 48, 49, 27, 65, 13 to the I O address 224. These numbers are merely the decimal equivalents of the ASCII binary values of the corresponding characters of the tables on page 7. For example, 0 is given as $0110000 = 2^5 + 2^4 = 32 + 16 = 48$.

The numbers 224 and 229 are I O addresses of the communications port.

POLLING TM70 FROM FORTRAN

This program was run on DEC's FORTRAN IV under RSX11M version 3.2. The program continuously polls a TM70 addressed as unit 1. Any new message from the terminal will be printed on the console until the message STOP is received. This ends the program. The TM70 is connected to the host computer as terminal 17 (TT17:). It uses the system supplied subroutine GETADR to obtain the address of the LINE and POL variables. The system supplied subroutine WTQIO sends the polling message and receives the response immediately.

```
      PROGRAM TMDEMO
      INTEGER PARAMS(6),TEMP(2)
      LOGICAL*1 LINE(80),POL(5)
      DATA PARAMS(2) 80 ,PARAMS(3) 0 ,PARAMS(5) 5 ,PARAMS(6) 0
      DATA POL(1) '0' ,POL(2) '1' ,POL(3) 27 ,POL(4) 'A' ,POL(5) 13
      CALL GET ADR(TEMP,LINE,POL)
      PARAMS(1)=TEMP(1)
      PARAMS(4)=TEMP(2)
C     ASSIGN TERMINAL 17 AS LOGICAL DEVICE 6
      CALL ASSIGN(6,'TT17:')
      WRITE(5,100)
100   FORMAT('POLLING TERMINAL 1')
C     MAIN PROGRAM - POLL TIL "STOP" IS RECEIVED
200   LINE(3)=' '
      CALL WTQIO("4400,6,3,,,PARAMS)
      IF (LINE(3).EQ.'') GOTO 200
      WRITE(5,260) LINE
260   FORMAT('',80A1)
      IF (LINE(3) .NE.'S') GOTO 200
      IF (LINE(4) .NE.'T') GOTO 200
      IF (LINE(5) .NE.'O') GOTO 200
      IF (LINE(6) .NE.'P') GOTO 200
      STOP
      END
```

MICROTERMINAL OPTION CONNECTION SUMMARY

The RS232C and 20mA current loop pin connections are contained in the rear panel DB-25 connector. All options are selected by interconnecting pins on the same connector. The option selections are summarized below. The DB-25 connector pinout is shown in Table IV on page 6. All other tables referred to below are also on page 6.

Parity

Parity selection (pins 9 and 10) is shown in Table I. With both parity pins open, the microterminal will operate with Mark parity.

Baud Rate

Baud rate selection (pin 11) is shown in Table III. With pin 11 open, the microterminal will operate at 300 baud.

Polling Address

Polling address selection (pins 22, 23, 24, and 25) is shown in Table II. With all polling address pins open, the microterminal will operate in the nonpolled mode.

TM71, TM77, TM71-I/O, AND TM77-I/O MICROTERMINALS USER'S GUIDE

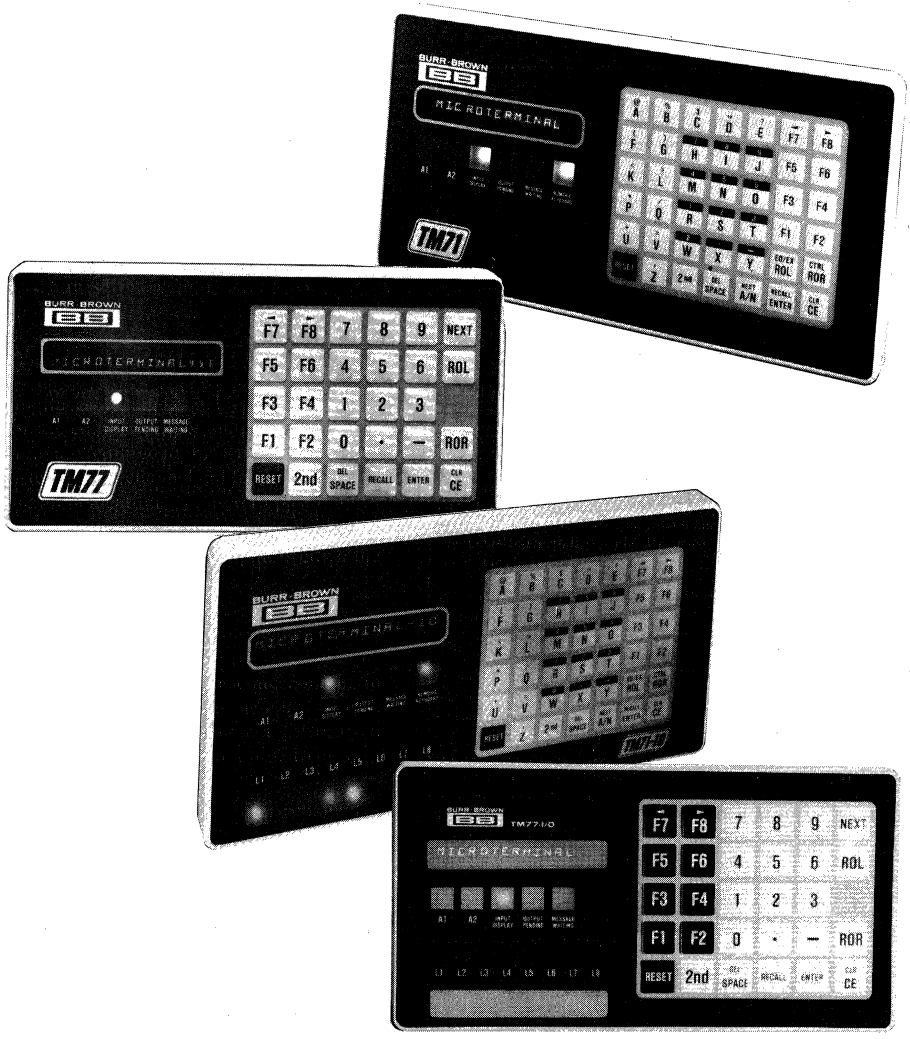


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TABLE OF CONTENTS

INTRODUCTION

If your system's data entry/control/display requirements are sophisticated but limited, you don't need to buy big, expensive and fragile CRT's or printing terminals to do the job efficiently.

"Microterminals" - uniquely flexible in application versatility - are designed expressly to fill the human interface demands of widely dispersed control and communications networks - in machine and process control, energy management systems, inventory control and factory floor data collection, and information processing. Microterminals, because of their interface flexibility, appearance, size, durability, and easy installation, function equally well as consoles and control centers for instruments and small systems. They also perform as I/O terminals in diagnostic applications.

You don't need interface expertise to put microterminals to work for you...they communicate in serial ASCII with RS-232-C or 20mA current loop conditioning. Baud rates range from 110 to 19,200.

A tough, water resistant front panel protects LED displays and indicators as well as a full alphanumeric keyboard. Tactile feedback, display blinking, and character display confirm operator entry.

Buffered data features reduce on-line input/output time with the CPU and improve accuracy of operator inputs. And, because of its design simplicity, the microterminal concept doesn't require special operator skills or training. Depressing a single function key initiates complex preprogrammed action by the CPU. These functions may be defined in your CPU's software or in local read only memory, for which a socket is provided.

This user's guide describes four products: TM71, TM77, TM71-I/O and TM77-I/O. All units feature 80-character buffers, a 16-character alphanumeric display, and serial ASCII interface. The TM71 and TM71-I/O provide alphanumeric keyboards. The TM77 and TM77-I/O provide numeric keyboards. The I/O versions, TM71-I/O and TM77-I/O, provide additional TTL inputs and outputs for interface to external equipment.

Microterminals' very compact design and simple mounting on any flat surface make them quickly adaptable to new or existing applications. All models measure only 216mm x 114mm x 15mm (8.5" x 4.5" x 0.6"). When ordered in OEM quantities the front panel can contain your corporate or system logo.

You can enter and display alphanumeric data. The TM71's 42-key keyboard (shiftable to generate 80 characters including A-Z and 0-9) allows you to receive or enter messages up to 80 characters long. A 16-character display - with horizontal scroll-left or scroll-right keyboard controls - permits review and editing of data entered before transmission. In the edit mode you can backspace and advance the cursor position and insert and delete characters.

Two 80-character buffers are provided for keyboard generated data. The output buffer holds a message being written, reviewed or edited; the transmit buffer holds a prepared message ready for CPU acceptance. This feature allows a second message to be prepared while the first awaits transmission.

Similarly, two 80-character buffers are available for incoming CPU-generated messages. The receive buffer holds an incoming message until it can be transferred to the input buffer where it is displayed for the operator's action. With this feature, the operator can visually review a CPU input while a second instruction from the CPU can be received and held until called up for display.

Display features include CPU control of scrolling, flashing, or blanking. The keyboard can also be locked out by CPU command. Two LED indicators are independently controlled by the CPU while four LED's indicate terminal status. The TM71-IO and TM77-I/O have an additional eight independently controlled LED indicators as well as two back panel I/O ports.

It is important to realize that while these microterminal products have many features, normal operation is very uncomplicated. Virtually untrained operators can use the microterminal products productively. Most special features are invisible to the operator. A typical application consists of a series of host-system-supplied operator prompts. To each prompt the operator simply keys in a short number or message and pushes the ENTER key. The function message keys may be used to further simplify operator responses. Function key messages may be transmitted immediately on depression.

OPERATION

DESCRIPTION

The four models described in this user's guide are TM71, TM77, TM71-I/O and TM77-I/O. All models operate in basically the same way. They are described below. For simplicity's sake, only the TM71 will be referred to after the description section. For all matters concerning control features, communications protocol, user PROM, and product specifications not relating to the keyboard or I/O ports, all units are identical.

TM71

The Model TM71 is an alphanumeric "microterminal" which may be used as a remote or local data entry and output terminal for a host computer system. It is intended to provide a low cost, small size, alternative to a CRT terminal. It is suitable for applications with a limited amount of data interchange, as compared to applications requiring a typewriter-style keyboard and multiline display or hard copy output.

The TM71 features a dust proof front panel including 80 characters on a 42-key keyboard, 16-character alphanumeric display, two host-computer controllable, light emitting diodes (LED's), and four status LED's. Character height is 0.14". The keyboard features raised embossing with tactile feedback. In addition, a 25-pin, D-style rear panel connector features RS-232-C data transmit, data receive, and modem control functions. The connector is also used to provide power, baud rate

selection (110, 300, 600, 1200, 2400, 4800, 9600, 19200 bps), remote reset in and out, parity selection, a polling address, and 20mA current loop.

TM77

The TM77 is intended for those applications where an alphanumeric display terminal with numeric and function key data input is adequate. The TM77 keyboard has the advantage that it is less complicated for the untrained or inexperienced operator.

The TM77 is functionally identical to the TM71 except for the keyboard functions. The TM77 has larger, but fewer keys than the TM71. The TM71 offers a numeric (0-9) keyboard with function keys. Keyboard functions of the TM71, which do not appear on the TM77, are not available. The numeric keyboard light is unnecessary and has been deleted.

The keys of the TM77 are 38% larger and placed on 0.65-inch centers as compared to the 0.5-inch centers of the TM71. This is the same spacing as used on touch tone telephones and allows operators with gloved hands to easily use the keyboard. As can be seen from the following figure, the keyboard appears much larger and less forbidding of use. For a description of the TM77 key functions, refer to those same keys described for TM71 in the Detailed Key Description section.

TM71-I/O

The TM71-I/O is identical to the TM71 but with the following additional features. The front panel has eight additional host-computer controllable LED's The rear panel has an additional 20-pin connector. This connector provides a TTL-compatible, 8-bit bidirectional port (port A) and 8-bit output only port (port B). The output only port indicates the status of the additional eight front panel LED's. The bidirectional port has input and output strobes and may be used by the host system as a general purpose remote input/output port.

TM77-I/O

The TM77-I/O is identical to the TM77 with the addition of the I/O port features described above for the TM71-I/O.

Up to 14 function messages may be defined by the host system. After definition by the host, these messages are called for display by the host sending a 3-character code [ESC] ZZ; where ZZ may have the values 01 through 08 and 21 through 26. Function messages may be re-transmitted to the host by pressing the front panel function message keys. Thus they may be used as extensions of the input message to the TM71 or as function messages to be transmitted by the TM71 operator to the host system. In addition, a PROM socket is provided for nonvolatile storage of function messages.

For all the following descriptions the terms input and output shall refer to input to the TM71 and output from the TM71. Internal operation of the TM71 is easily conceived as five buffer memories as indicated in the block diagram in Figure 1. In addition, function messages are stored in a separate RAM or PROM memory area. The receive buffer receives incoming messages of up to 80 characters and when the message is complete, it is usually automatically transferred to the input buffer. The display buffer is then filled with the first 16 characters of the input message. The operator may then scroll the input message through the display buffer. Alternately, the host computer can cause the message to continuously scroll through the display buffer. The contents of the display buffer are displayed to the operator through 16 alphanumeric characters. The output buffer which serves as temporary storage for keyboard entries is transferred to the transmit buffer when the ENTER key is pressed. At that time the message is transmitted to the host or, in polled operation, held until the host requests the message.

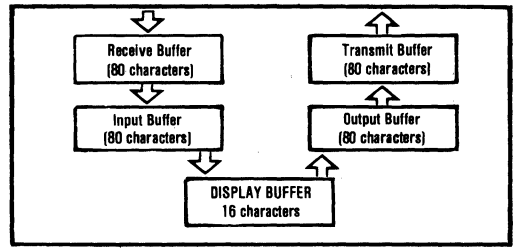


FIGURE 1. TM71 Buffers.

Further insight into the operation of the TM71 can be gained by viewing its operation in terms of modes and status conditions. The TM71 has three major operating modes and four status conditions.

Operating Modes	Status Conditions
Ready	Message Waiting
Message Composition	Output Pending
Edit	Input Display
	Numeric Keyboard

OPERATING MODES

Ready

The Ready mode is the standby mode; it is entered by pressing CE, 2nd CLR, or RESET. The symbol Λ in the output display indicates the Ready mode. The other display positions are blank. Ready mode is exited when any character or function message is entered into the output buffer from the keyboard or when the terminal is put in Edit mode. The ready indicator will not be visible when an input message is being displayed; however, the terminal may be internally in Ready mode.

Message Composition

Message Composition mode is entered from the Ready mode or Edit mode. If the terminal is in the Ready mode, entering any character or function message from the

keyboard causes the terminal to enter Message Composition mode. It is indicated by having a character in the output buffer. A space is the only character that can leave the display buffer blank. Nondisplayable characters are displayed as 井 . Message Composition mode may also be entered from the Edit mode by pressing 2nd ED/EX.

Message Composition mode is exited by pressing CE, 2nd CLR, RESET, ENTER, or 2nd ED/EX. The latter causes the terminal to enter Edit mode.

Edit

Edit mode may be used to modify the contents of the output buffer. It is not essential to be able to use the Edit mode in order to operate the TM71. It is entered by pressing 2nd ED/EX and is exited by pressing 2nd ED/EX again or CE, 2nd CLR, ENTER, or RESET. Edit mode is indicated by the presence of the underscore cursor in the display while the output buffer is being displayed.

STATUS CONDITIONS

Numeric Keyboard

Numeric Keyboard status is used to provide a convenient numerical key pad in the center of the keyboard; it is entered by pressing A/N. If the terminal is in Numeric Keyboard mode, it is exited by pressing A/N. Numeric Keyboard is indicated by the Numeric Keyboard LED being on.

Message Waiting

Message Waiting status is the condition of being in Message Composition mode when the host sends an input message. The Message Waiting LED comes on to indicate a new input message is in the input buffer and may be viewed at the operator's convenience by pressing 2nd RECALL, ENTER, or CE. When any of these actions are taken, the Message Waiting LED goes off until the host sends another message while the terminal is in Message Composition mode. In addition, if the host sends a new message before the input buffer has been examined, the message is held in the receive buffer. The message to be transferred to the input buffer.

Output Pending

Output Pending status occurs when the terminal is used in a polled configuration, as determined by rear panel connector jumpers, and an output message has been enabled by the ENTER key. The message is actually transmitted when the host polls the terminal. Until this happens the Output Pending LED comes on. In many installations this will happen so quickly that the operator may never actually see the LED come on. However, if the host were temporarily occupied with another task, the operator would know that the message had not been transmitted. The message actually enters the transmit buffer and waits there until the terminal is polled. A second output message may be composed in the output buffer; however, if ENTER is pressed for the second message before the Output Pending LED goes off, the first message is lost.

Input Display

The Input Display LED indicates when the display buffer is viewing the input buffer. This can happen in two ways. When the terminal is in Ready mode, an input message will automatically switch the display buffer to the input buffer causing the Input Display LED to come on. The Ready Indicator will no longer be visible; however, the terminal is still in the Ready mode.

When the terminal is in Message Composition mode, pressing 2nd RECALL switches the display buffer to the input display causing the Input Display LED to come on. The terminal is still in Message Composition mode. Pressing 2nd RECALL a second time will return the display buffer to its former position in the output buffer.

POLLED MODE

Up to 15 TM71's may be operated on one host communication port. This is referred to as polled operation. This is made electrically possible by using the 20mA communications current loop circuits. These circuits feature optical isolators to allow multiple input and multiple output loops to be series connected together. The host then uses a 2-digit drop number, unique to each TM71 on the loop, to address each TM71 terminal. Correspondingly, each TM71 prefaces each of its output messages with its drop number. Details of polled operation are contained in the Communications Protocol section and in the Installation Section.

Figures 2, 3, 4 and 5 show the front panel of the four models.

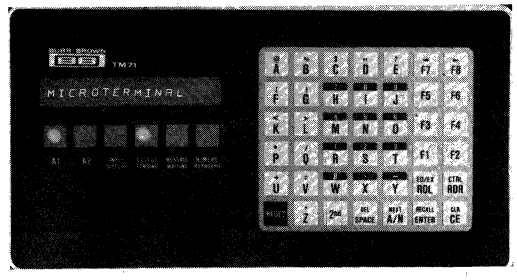


FIGURE 2. TM71 Front Panel.

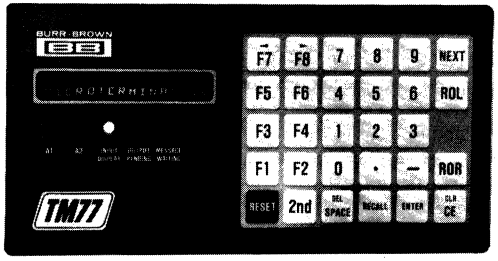


FIGURE 3. TM77 Front Panel.

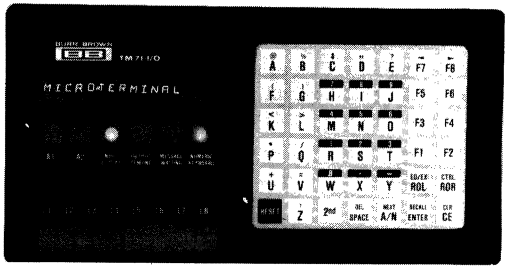


FIGURE 4. TM71-I/O Front Panel.

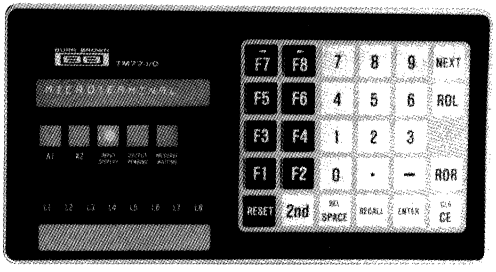


FIGURE 5. TM77-I/O Front Panel.

OPERATING INSTRUCTIONS

When power is applied to the TM71, the Input Display LED will come on and the display will show the Ready Indicator which is a ^ in the left-most character position. A message consisting of up to 80 characters, including spaces, may be entered from the keyboard. Pushing the ENTER key causes the message to be transmitted to the host computer. The message will be sent each time ENTER is pressed; this is indicated by the display blinking. In Polled mode the Output Pending LED will come on until the host takes the message. The output buffer may be cleared by pressing CE. Pressing a key to start a new message will automatically clear the output buffer. The Ready Indicator will appear after the output buffer has been cleared by CE. In addition, the Function Message keys may be used to enter up to 14 different function messages into the output buffer.

In Ready mode, when a message is received from the host computer, the first 16 characters of the message appear on the display. The Input Display LED comes on to indicate the display buffer is filled with a section of the input buffer. The entire message may be viewed by using the ROL and ROR keys. When one of these keys is held down, the message will scroll through the display at approximately six characters per second. When any character key is pressed, the Input Display LED goes out and the character appears in the left of the display with the rest of the display blanked. As other character keys are pressed, the message grows from left to right. For upper key characters, the 2nd key is pressed first. It must be pressed prior to each upper key character. 2nd DEL deletes the last character. If DEL is held down, characters will be deleted at approximately six characters per second.

To facilitate the composition of long output messages, a line editor is available by using the 2nd ED/EX key sequence. The Editor is described in the Display Control, Edit, and Control Keys section.

Internally, the TM71 consists of 80-character receive and input buffers, a 16-character display buffer, and 80-character output and transmit buffers. The display buffer is used to scan either the input buffer or the output buffer. It is switched from one to the other by pressing 2nd RECALL. When the display buffer is displaying the input buffer, the front panel Input Display LED will be on.

Complete operating details are contained in the following section.

DETAILED KEY DESCRIPTIONS

ALPHABET AND SPECIAL CHARACTER KEYS [@ A] [% B] etc.

These keys are used for data input from the keyboard. To enter the upper character press the 2nd key prior to each upper character. Characters enter the display in the left-most unused position. After 16 characters have been entered, previous characters move one character position to the left when a new character is entered. After 80 characters are input, no more characters are accepted.

ALPHABET AND NUMERIC KEYS [T] [Y] etc.

These keys are used to enter characters from the keyboard. The upper characters are entered by pressing 2nd prior to each upper character. This is called the Alpha mode. An alternate mode is called Numeric mode. In this mode an upper character may be entered by only pressing the key. In the Numeric mode pressing 2nd first will cause the lower character to be entered. The keyboard is put in Numeric mode by pressing the A/N key. The Numeric keyboard LED is on while the keyboard is in numeric mode. To exit Numeric mode press A/N. Alpha mode is the power-up and Reset mode.

FUNCTION MESSAGE KEYS [F1] [F2] etc.

These keys are used to input function messages from the keyboard. The function message may be one of the default strings &XX or it may be a host defined string. When no host specified string definition has been provided, the three characters of the default string appear. For a host defined value, the last 16 characters of the string definition appear in the display.

Incoming function messages appear with their first 16 characters in the display.

The first eight function messages are put in the output buffer by pressing the F1 through F8 keys and the remaining six by pressing 2nd F1 through 2nd F6.

When no message has been defined, default messages appear in the display as &ZZ. ZZ represent 01 through 08 or 21 through 26 for a total of 14 values.

FUNCTION MESSAGE AND DISPLAY CONTROL KEYS [◄ F7] [► F8]

These keys, when used as function message keys, are the same as the previously defined function keys. When used with the 2nd key, they move the display buffer to the right-most 16 characters (◄), or the left-most 16 characters (►), of the input or output buffer. In Edit mode the display cursor (underscore) goes to the end (◄) or start (►) of the message.

DISPLAY CONTROL, EDIT, AND CONTROL KEYS

[ED/EX ROL] [CTRL ROR]

Display Control Keys

In normal operation pressing ROL will cause the message to move one character position to the left or until the last character of the message being examined is in the right-most position of the display. Pressing ROR causes the message to move one character to the right or until the first character of the message under examination is in the left-most display position. Holding eight key down causes the display to scroll by at approximately six characters per second until the first character is in the left-most, or the last character is in the right-most character position for messages of more than 116 characters.

Display Editing Keys

The ED/EX key is used to put the TM71 in or out of Edit mode. In Edit mode DEL, ROL, ROR, ◄ and ► may be used for easy editing of any message contained in the 80-character output buffer. Edit mode is indicated in the display by an underscore which is used as the Edit cursor. The cursor "points" to the immediate character to its left. The key sequence 2nd DEL deletes the character. If DEL is held down, characters are deleted at the rate of six characters per second. ROL and ROR move the cursor one position to the left or right. If ROL or ROR are held down, they cause the cursor to scroll left or right. When the cursor points to the first or last character, it will not move further to the left or right, respectively. When the cursor reaches the left or right end of the display, the message begins to scroll right or left, respectively. The cursor continues to point at the left-most or right-most character of the display.

In Edit mode the display is effectively shortened to 15 characters since the underscore cursor does not actually "underscore" the character to which it points. ◄ causes the display buffer to display the right-most 15 characters with the cursor in the right-most position. ► does the same for the left-most 15 characters with the cursor in the right-most position.

When the display buffer is filled with part of a host-sent input message, the message may be transferred to the output buffer without transmission by pressing 2nd ED/EX. The TM71 will then be in Edit mode with the Edit cursor at the right end of the input, now the output, message section being examined. The previous contents of the output buffer are lost.

Function messages may be edited. The following example illustrates the use of the editor.

Edit Mode Example:

KEYSTROKES	DISPLAY	ACTION
	XXZZYYY	Delete ZZ and put ABCD in its place
2nd ED EX	XXZZYY	Enter Edit mode (underscore cursor)
ROL ROL ROL	XXZZ_YYY	Move Cursor
2nd DEL 2nd DEL	XX_YYY	Delete two characters
A	XXA_YYY	Enter A
BCD	XXABCD_YYY	Enter B, C, D
2nd ED EX	XXABCDYYY	Exit Edit mode

NOTES:

1. The underscore indicates Edit mode.
2. The cursor may be moved with ROL and ROR.
3. ROL and ROR stop at the ends of the output line.
4. Filling the 80-character output buffer prevents the display from responding to any attempt to insert or append more characters.
5. Holding ROL or ROR down causes the cursor to move toward the beginning or end of the line at approximately six characters per second.
6. When there are no characters in the output buffer, the TM71 will not enter the Edit mode. Deleting all characters causes the TM71 to exit Edit mode.
7. The ASCII underscore is also a valid character.

Control Key

The key sequence 2nd CTRL followed by any letter of the alphabet causes the corresponding 26 ASCII characters to be put in the output buffer. These characters are listed in the Appendix.

In addition, 2nd CTRL F1 causes the ASCII Escape (ESC) character to be put in the output buffer.

The 2nd CTRL D sequence has special meaning to the TM71. It is the ASCII EOT character. This character is an end of transmission character. When the TM71 operates with some host computer operating systems, it is sometimes desirable to send a message without a carriage return. The key sequence, MESSAGE 2nd CTR D ENTER, causes MESSAGE to be sent without a carriage return. This is often desirable in conjunction with other control characters. For example, in many operating systems CTRL C is used to return from a particular system program to the keyboard monitor program. The keyboard monitor responds with some acknowledgement character or prompt. It will not usually expect a carriage return with control characters since control characters are often used to interrupt other operations. Thus, since the TM71 has a one line display, 2nd CTRL C ENTER will cause the prompt to be missed because the CR is interrupted by the monitor as a null line response to the prompt. In fact this causes most operating systems to return to the previous operation and prevents access to the keyboard monitor. Entering 2nd CTRL C 2nd CTRL D ENTER causes the TM71 to suppress the carriage return that is normally appended to output messages. This allows the prompt to be viewed in the TM71 display. A function key may be programmed to provide a CTRL D sequence.

RESET

The RESET key allows the TM71 operator to initialize the internal functions. Pressing RESET is equivalent to turning on the power. Pressing RESET will cause host defined messages to be lost. RESET may be disabled when the TM71 is installed.

SECOND KEY [2nd]

The second key, 2nd, is used to enable the upper label of the next key pressed. For example, the key sequence [2nd] [U] [U] causes +U to be displayed and stored in the output buffer. When the keyboard is in Alpha mode as indicated by the Numeric keyboard status LED being off, [2nd] [S] causes 2 to be displayed and stored.

SPACE AND DELETE KEY [DEL SPACE]

Space causes a blank to be entered into the output buffer. The right-most character becomes a blank. DEL deletes the right-most character. DEL does not enter the ASCII character DEL into the output buffer.

In Edit mode DEL causes the character to the left of the cursor to be deleted.

ALPHANUMERIC AND NEXT KEY [NEXT A/N]

Pressing the A/N key causes the keyboard to enter the Numeric mode. The upper white-on-black labels become lower labels not requiring the 2nd key before entry. The lower labels become upper labels and require the use of the 2nd key for entry. The front panel Numeric LED comes on to indicate the keyboard is in Numeric mode. Press A/N to return to Alpha mode. The Alpha mode is also the power-up and Reset mode.

Pressing 2nd NEXT causes any input message waiting in the Receive Buffer of the block diagram in Figure 1 to be transferred to the Input Buffer. This will be necessary when an input message is received while the terminal is holding a previous input message. This condition is indicated by both Input Display and Message Waiting LED's being on.

ENTER AND RECALL KEY [RECALL ENTER]

ENTER is used to send output messages to the host system. When the TM71 is in Ready mode, the receipt of an incoming carriage return, CR, causes the display buffer to be loaded with the first 16 characters of the input message. The Input Display LED will come on. When the TM71 is in Message Composition or Edit mode, receipt of an incoming CR causes the Message Waiting LED to come on. The operator may finish any output message and send it to the host by pushing ENTER. If it is desired to examine the input message before entering or even completing the output message, the RECALL key may be pressed causing the display buffer to be filled with the first 16 characters of the input message. The Input Display LED will come on. The input message may be examined by using ROL and ROR. Pressing RECALL a second time will cause the display register to be filled with the 16 characters of the output buffer it contained when RECALL was pressed the first time. The Message Waiting LED is turned off, and remains off, after the first input message access with the RECALL key. Accessing the input message a second time fills the display buffer with the 16 characters it contained when the output message was accessed. Thus, if required, the operator can work through the input message composing an output message in response to small sections of the input message.

Pressing ENTER while in Edit mode causes the TM71 to exit Edit mode and transmit the output buffer.

While examining an input message, pressing ENTER will cause the input message to be transferred to the output

buffer and transmitted to the host. Any previous contents of the output buffer will be lost. The Input Display LED is on when the display buffer contains a section of the input buffer. When the display buffer is filled with part of an input message, the message may be transferred to the output buffer without transmission by pressing 2nd ED/EX. The TM71 will then be in Edit mode with the cursor at the right end of the input (now the output) message section being examined. The previous contents of the output buffer are lost. The input buffer retains the original message.

CLEAR ENTRY AND CLEAR ALL KEY [CE]

Pressing CE causes the TM71 to exit Message Composition mode and the Ready Indicator to come on. The output buffer is cleared. Pressing 2nd CLR causes the TM71 to exit Message Composition mode, clears output and input messages, clears Message Waiting LED, clears Output Pending LED, and causes the Ready Indicator to appear. Host-specified function messages are unaltered. Pressing RESET, if enabled by the back panel jumper, has the same effect; plus, it sets function messages to their default power-up condition.

When the TM71 is in Edit mode, pressing CE or 2nd CLR causes the terminal to exit Edit mode and go into the Ready mode.

2nd CLR clears the receive buffer but does not clear the transmit buffer. Although the Output Pending LED goes off, the host may still read the transmit buffer.

APPLICATIONS

CONTROL FEATURES

Certain input messages may be used by the host system to put the TM71 in special modes. These messages, which begin with the ASCII Escape character (ESC), are described below. See also the Input Message Summary part of the Communications Protocol section.

(ESC)A(CR)	Requests the transmit buffer. Used only in Polled Mode. The A command works only once per ENTERed message. The second time the A command is used for the same message, a carriage return only is transmitted.
(ESC)B(CR)	Requests retransmission of the transmit buffer. The B command can be used to get a second transmission of a message if for instance the first transmission has a parity error.
(ESC)C(CR)	Clears the input buffer.
(ESC)DZZ(MESSAGE(CR)	Used to define function messages in RAM, ZZ is the function message number from 01 to 08 and 21 to 26. (MESSAGE) is the function message. If (MESSAGE) is not present, the function message is deleted.
(ESC)En(CR)	Controls the A1 LED and the A1 TTL output. For n=1 the LED is "on" and the TTL output "low". For n=0 the LED "off" and the TTL output "high".
(ESC)Fn(CR)	Controls the A2 LED and A2 TTL output. For n=1 the LED is "on" and the TTL output "low". For n=0 the LED is "off" and the TTL output "high".
(ESC)Gn(CR)	Causes any input message being observed through the display to scroll continuously from right to left at approximately six characters per second when n=1. n=0 disables scroll.
(ESC)Hn(CR)	Causes any input display message to flash with a 50% data cycle approximately three times per second when n=1. When n=0 flash is disabled.
(ESC)In(CR)	Causes any output message to blank when n=1. The input buffer will still be displayed. n=0 disables blanking.
(ESC)Jn(CR)	Locks out the keyboard from use when n=1. The RESET key is not disabled. Keyboard lockout is disabled with n=0.
(ESC)K(CR)	Causes the input buffer to be transferred to the transmit buffer and transmitted. This command is useful in testing communications lines and circuits. A message transmitted by the host CPU to the microterminal will be returned to the host by the terminal after receipt of the K command.
(ESC)LDDD(CR)	Sets turnaround delay. Turnaround delay is the time that the microterminal waits after it receives a command to transmit, before it actually transmits. DDD sets the delay in increments of 10 milliseconds from 0 to 2.54 seconds. This delay has a default value of 40 milliseconds.
(ESC)M(CR)	Causes the digital input to port A to be transmitted to the host CPU as a single ASCII character.
(ESC)N(CR)	Causes the digital input to port A to be transmitted to the host CPU as three decimal digits - 000 to 255.
(ESC)O(CR)	Causes port A to operate in continuous ASCII mode. In this mode, data strobed into port A is immediately transmitted as a single ASCII character. ASCII characters transmitted from the host CPU to the terminal are output immediately. (ESC) terminates continuous mode.
(ESC)P(CR)	Causes port A to operate in continuous decimal mode. In this mode, as data is strobed into port A, it is immediately transmitted as three decimal digits followed by a carriage return. Likewise, three decimal digits followed by carriage return from the host CPU is immediately output as the 8 bits of port A. (ESC) terminates continuous mode.
(ESC)Qa(CR)	Causes one ASCII character, "a", to be output on port A.
(ESC)RDDD(CR)	Causes the decimal number DDD to control the output of port A. DDD is a number between 000 and 255.
(ESC)SDDD(CR)	Causes the decimal number DDD (000 to 255) to control the output of port B.

Function Messages

The TM71's RAM has 415 character locations which may be used for function messages. The function messages may be any length less than or equal to 80 characters as long as the total number of characters does not exceed 415. This memory is assigned dynamically by the TM71 software. This means up to five messages may be 80 characters each if only five are defined. Attempting to exceed this boundary will cause unpredictable results. Alternately, a maximum of 14 messages of 29 characters each could be defined; they may be of differing lengths. When a PROM is used to define function messages, 14 messages 80 characters in length may be defined for a total of 1120 characters. RAM definitions may be made even when the PROM is present. The RAM definitions

are used by the TM71 until the RAM definitions are deleted, then the PROM definitions are used. This may be done with the RESET key or from the host.

Function messages may contain all 128 characters of the ASCII set.

When control ASCII characters are part of normal input messages, they are stripped; however, they may be part of commands such as function message definitions.

All function messages are transmitted to the TM71 as (ESC)ZZ where ZZ represents 01 through 08 and 21 through 26 for function messages 1 through 14. For output &ZZ will be used as a default string if no message definition has been made in RAM or PROM. In this case the message will be transmitted as defined.

The sequence (ESC)ZZ is considered part of a message. Do not confuse it with one of the (ESC) commands in the Input Message Summary section. For example, (ESC)01 (CR) is a complete and normal input message; it causes function message 01 to be put in the input buffer.

See Figure 6 which shows the Displayable Characters.

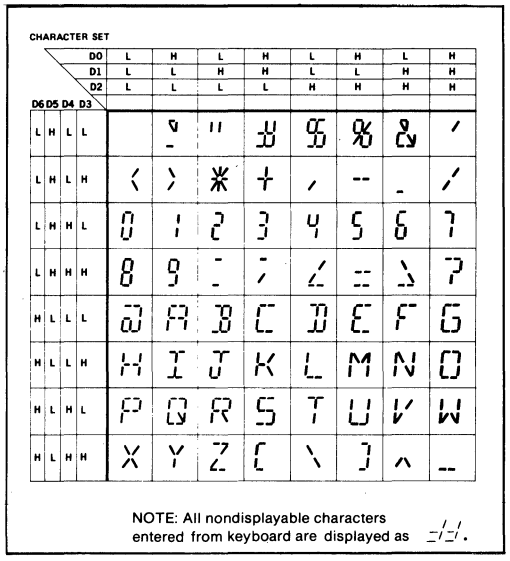


FIGURE 6. Displayable Characters.

IMMEDIATE TRANSMISSION OF FUNCTION KEYS

A function message can be transmitted immediately if the ASCII control character RS (Record Separator) is the last character of the definition. When this character is encountered while getting the function message from RAM or PROM, it is treated as if the ENTER key were pressed. This causes the function message to be transmitted along with any characters that were in the buffer when the function key was pressed.

This feature, when used with CTRL D, allows function messages to have a completely user-determined end of line character string. This is accomplished by defining a function message as follows:

(ESC)D02(MESSAGE)(CTRL D)(RS)(CR)

When the F2 function key is pressed, (MESSAGE) preceded by any contents of the output buffer, is immediately transmitted. (MESSAGE) may include any type of line terminator such as (LF)(CR), (CR)(LF), or (ETX). (CTRL D) prevents the TM71 from adding a (CR) and (RS) causes immediate transmission without the use of the ENTER key.

The use of (RS) is especially important for high priority control messages for which it is desired that only one key be pressed.

The only restriction on the message is the use of (CR). (CR) may be contained in PROM-defined function messages but not in host-defined messages. This is necessary because an imbedded (CR) will terminate the function defination.

CTRL X

The control CAN (CTRL X) of the ASCII set has special meaning to the TM71. When it is the first character of an input message, or the first character after the address characters in Polled operation, the TM71 will clear its receive and input buffers of previous messages and blink the Message Waiting LED. The new message will be in the input buffer and a command will be executed. This may be important for high priority messages to the operator. If the operator leaves the TM71 in Message Composition mode and two messages have been received, the first message will be in the input buffer and the second in the receive buffer. A third message or command will not be received unless (CTRL X) is used to clear the receive and input buffers. When the TM71 is in Ready mode, all messages come to the input buffer and the terminal goes to input display status. In this case the (CTRL X) has no effect on operation.

TURN AROUND DELAY

When commands that cause an automatic reply are sent from the host, TM71 can delay its reply for a programmable turn around time. The purpose of this feature is to allow the TM71 to operate with any host, terminal handler software which cannot accept input immediately following the carriage return of a host output message. This is the case in many host systems. This delay has a default value of 40 milliseconds. This may be changed by the host by using the command string (ESC)LDDD(CR) where DDD represents 000 through 255. This number sets the delay in increments of 10 milliseconds from 0 to 2.54 seconds. Delay may also be set by the user PROM. RAM-defined delays will override PROM-defined delays.

TM71 SELF TEST AND DEMONSTRATION

The TM71 may be exercised without a host system by connecting +5VDC power. If TX (pin 2) is jumpered to RX (pin 3), the TM71 can receive its own messages and commands. For example, it is possible to send, receive, and scroll a message as follows:

Key sequence: (CE)HELLO(ENTER)(2nd)(CTRL)(F1)
G1(ENTER)(2nd)(RECALL)

This key sequence will cause the word HELLO to banner across the display. (CE)HELLO(ENTER) clears the output buffer and sends HELLO to the input buffer. The TM71 automatically switches to input display indicated by the input display LED coming on. (2nd)(CTRL)(F1) enters (ESC) in the output buffer.

The TM71 switches to output display causing the input display LED to go off. Since (ESC) is nondisplayable, a 卄 appears in the display. G1(ENTER) then completes the banner command and sends it to the TM71 receive buffer. (2nd)(RECALL) switches the terminal to input display and the bannering HELLO is observed.

COMMUNICATION DELAYS

Some operations require a delay before the TM71 can accept another message or command. When a function message is defined, the TM71 requires at least 150 milliseconds before another message or command can be received. A host message which calls a predefined function message requires 2 milliseconds for each function message called before another message or command can be received. The TM71 provides buffer space for one message and one command. Delays may be required between two commands or between two messages.

When software is written in a high level language, delays between messages will normally occur. When programs are written in assembly language on small systems such as single board computers, it may be necessary to design delays into the system software. Should the need arise, this is easily accomplished for high level languages as well. It is recommended that I/O commands for TM71-I/O be followed by a 40 millisecond delay. Note: Delay timing must start after the receipt by the terminal of the carriage return delimiter.

CTRL D

Carriage returns can be suppressed on output by entering (MESSAGE) 2nd CTRL D ENTER. This is useful when interfacing to some host operating systems as was explained in the Display Control, Edit, and Control Keys section. CTRL D is the ADCII end of transmission character (EOT). A function key may be programmed to provide CTRL D.

COMMUNICATIONS PROTOCOL

The TM71 sends and receives 7-bit, asynchronous ASCII character codes with one parity bit and two stop bits. One or two stop bits will be accepted for input. When parity is disabled, a mark or space, as determined by P1 jumpers, is inserted for the parity bit. Parity may be even or odd and is selected by jumpers on P1. Characters with parity errors are displayed as nondisplayable characters ( ). These jumpers also select the data receive and transmit rate. This rate may be 110, 300, 600, 1200, 2400, 4800, 9600, or 19,200 bps.

Each message transmitted from TM71 is terminated with a carriage return character. When operated in Polled mode, each message is preceded with its 2-character polling drop number. This is not counted as part of the 80-character message.

For an input message, the TM71 requires that the message of up to 80 characters in length be terminated by a carriage return. Line feeds following a carriage return are discarded; otherwise they are displayed as non-displayable characters. Line feed will be ignored as the first character of a message. Carriage return is not counted as one of the input characters. In Polled mode the message must begin with a drop number 00 through 15. This is followed by up to 80 characters plus a carriage return. When the host polls the TM71, it must send XX(ESC)A(CR) where XX is the drop number of the particular TM71 (01 to 15). Drop number 00 causes an input message to be received by all terminals.

FUNCTION MESSAGES

Function messages of up to 80 characters in length may be defined by sending (ESC)DZZ(MESSAGE)(CR). In Polled mode this would be XX(ESC)DZZ(MESSAGE)(CR). ZZ represents the function message number 01 through 08 or 21 through 26. When a user PROM has been installed, these definitions are still valid and take the place of any PROM message until RESET is pushed, power-up, or the message is deleted. Defined messages may be deleted by sending a new definition or (ESC)DZZ(CR). (ESC)D00(CR) deletes all function message definitions.

To call a function message to the display from the host, the host sends (ESC)ZZ within a normal message or merely (ESC)ZZ(CR). The display buffer shows the defined function message when a definition is present in RAM or PROM. The defined function message is transmitted on output. When no message has been defined, &ZZ is shown in the display of input and output messages. &ZZ is also transmitted in output messages when no function message has been defined.

It is important to remember the distinction between the host defining a function message and entering a message in the input buffer. The host may define them without entering them when they are for use by the operator through the function message keys.

INPUT/OUTPUT PORTS

The TM71-I/O and TM77-I/O have, in addition to all the features of the TM71 and TM77, an 8-line output port (port B) and an 8-line input and output port (port A). These ports connect to a 20-pin connector on the back panel. Port A has an input strobe and an output strobe. Port B connects to an additional eight LED's on the front panel.

Port B data is encoded as three ASCII characters and represents the decimal numbers 000 through 255. The three characters control the status of the eight output bits of port B or port A in decimal mode. The decimal number corresponds to the value of the eight-bit port as shown below:

PORT B or PORT A								DECIMAL
B7	B6	B5	B4	B3	B2	B1	B0	DDD
0	0	0	0	0	0	0	0	000
0	0	0	0	0	0	0	1	001
0	0	0	0	0	0	1	0	002
0	0	0	0	0	0	1	1	003
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Port A has two data modes: Decimal and ASCII. Decimal mode is the same as that for port B. In addition, single ASCII characters may be input and output from port A one character per operation. This is called ASCII mode.

In ASCII mode, the seven least significant bits of port A are set equal to the value of the ASCII character. The following chart shows the data that is transferred through port A in ASCII mode.

PORT A								ASCII
A7	A6	A5	A4	A3	A2	A1	A0	CHARACTER
X	0	0	0	0	0	0	0	NUL
X	0	0	0	0	0	0	1	SOH
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
X	0	1	1	0	0	0	0	0
X	0	1	1	0	0	0	1	1
X	0	1	1	0	0	1	0	2
X	0	1	1	0	0	1	1	3
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
X	1	0	0	0	0	0	0	@
X	1	0	0	0	0	0	1	A
X	1	0	0	0	0	1	0	B
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
X	1	1	1	1	1	1	1	DEL

X - NOT USED

These units may also be used for continuous input and output from port A. In the continuous mode the unit will only respond to the input message (ESC) which stops continuous input and output. In this mode, protocol is mostly determined by the host and the device connected to port A.

In summary, input/output through port A may be ASCII or decimal mode as well as continuous or noncontinuous.

To characterize the operation of port A, four cases are considered.

Decimal, Noncontinuous. On input the eighth bit may be a one or zero. If the host cannot control the eighth bit, merely send two stop bits. The TM71 will interpret the first stop bit as the eighth bit ($B_8 = 1$) and the second as the stop bit. On output the TM71 will set the eighth bit to one or zero as determined by its connector jumpers. Use "bit eight equals one" to simulate two stop bits if the host expects two stop bits. This is the case when no jumpers are connected. Decimal mode takes three characters to form a number from 000 through 255. This number gives full control to the eight output bits of port A. For input from port A, the eight bits are translated to a number from 000 through 255 and transmitted to the host as three ASCII characters. The most significant digit is received and sent first. This mode is convenient for applications programs written in a high level language such as BASIC or FORTRAN. The I/O statements of such languages will allow the applications program to communicate directly with port A without the need to call assembly language subroutines.

When even or odd parity is enabled on the TM71, and parity errors are found in port A data from the host, the data is not put on port A. Characters are sent to the host with the parity bit set appropriately.

Decimal, Continuous. In this port A mode, data may be sent from the host as a continuous stream of 3-character data as follows:

DDD(CR)DDD(CR) ---

Parity is not checked and the eighth bit has the same consideration as discussed in the Decimal, Noncontinuous section. Input from port A is handled in a similar way. Each input strobe causes DDD(CR) to be sent to the host. If port A is strobed faster than the transmission line can take the data, more than three characters will be sent between carriage return characters. The last three will indicate the data correctly at the time of the last strobe. Decimal continuous mode is entered by the command string (ESC)P(CR).

When parity is enabled, a parity error in any of the three data characters will cause port A output to not change. Input from port A will have the appropriate parity bit added for transmission to the host.

ASCII, Noncontinuous. In this mode a single ASCII character is received from the host and output on port A. No check of the eighth bit is made. The eight bit considerations are the same as discussed in the Decimal, Noncontinuous section. On input from port A the eighth bit is set according to the jumpers on P1. A port output is illustrated by the string (ESC)Qa(CR). The "a" represents any of the 128, 7-bit, ASCII characters.

When a parity error is detected in the host input data, no output to port A is made. For input from port A the parity bit is set appropriately, and the string (a)(CR) is transmitted to the host.

ASCII, Continuous. This mode is entered by the host sending the string (ESC)O(CR). The host sends a continuous stream of characters DDD---. The (ESC) character terminates continuous operation. Bit 8 is not checked or altered by the TM71, input from the port is transmitted as received. This means that the TM71-I/O does not alter eight bit data. The host and the device connected to port A may send and receive parity if they choose. Thus, the TM71-I/O serves only as a serial-to-parallel and parallel-to-serial converter.

Any error in the continuous stream from the host causes that character not to be sent. Input from the port will have a correct parity bit set by the TM71-IO.

The decimal numbers from 000 through 255 represent all the 256 possible combinations of eight bits. Thus, each of the eight bit lines may be individually controlled.

BINARY TO DECIMAL CONVERSION

To convert from the desired binary bit pattern to the corresponding decimal number the following method may be used.

b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1

$$DDD = \sum_{N=1}^{8} 2^{N-1} = 1b_1 + 2b_2 + 4b_3 + 8b_4 + \text{---} + 128b_8$$

Additional features are illustrated in Tables I, II, III, and IV and in the Control Features section.

TABLE I. Input Message Summary - Nonpolled Operation.

HOST TO TM	DESCRIPTION
(MESSAGE)(CR)	input message
(ESC)A(CR)	request transmit buffer
(ESC)B(CR)	retransmit transmit buffer
(ESC)C(CR)	clear input buffer
(ESC)DZZ(MESSAGE)(CR)	define function message
(ESC)DZZ(CR)	delete function message
(ESC)D00(CR)	delete all function messages
(ESC)En(CR)	output to A1 LED
(ESC)Fn(CR)	output to A2 LED
(ESC)Gn(CR)	scroll display control
(ESC)Hn(CR)	flash display control
(ESC)In(CR)	blank display control
(ESC)Jn(CR)	keyboard lockout control
(ESC)K(CR)	remote ENTER
(ESC)LDDD(CR)	set turnaround delay
TM71-I/O and TM77-I/O Only	
(ESC)M(CR)	read port A ASCII
(ESC)N(CR)	read port A Decimal
(ESC)O(CR)	port A continuous ASCII
(ESC)P(CR)	port A continuous Decimal
(ESC)Qa(CR)	output "a" to port A, ASCII mode
(ESC)RDDD(CR)	output to port A, Decimal mode
(ESC)SDDD(CR)	output to port B
(ESC)	halt continuous IO

NOTES:
1. Parentheses are not actually encoded. Shown for copy clarity only.
2. (ESC) control commands may not be embedded in messages.
3. n = 1 for ON; n = 0 for OFF.
4. ZZ is function number, 01 to 08 and 21 to 26.
5. "a" is ASCII character.

TABLE II. Input Message Summary - Polled Operation.

HOST TO TM	DESCRIPTION
XX(MESSAGE)(CR)	input message
XX(ESC)A(CR)	request transmit buffer
XX(ESC)B(CR)	retransmit transmit buffer
XX(ESC)C(CR)	clear input buffer
XX(ESC)DZZ(MESSAGE)(CR)	define function message
XX(ESC)DZZ(CR)	delete function message
XX(ESC)D00(CR)	delete all function messages
XX(ESC)En(CR)	output to A1 LED
XX(ESC)Fn(CR)	output to A2 LED
XX (ESC)Gn(CR)	scroll display control
XX(ESC)Hn(CR)	flash display control
XX(ESC)In(CR)	blank display control
XX(ESC)Jn(CR)	keyboard lockout control
XX(ESC)Kn(CR)	remote ENTER
XX(ESC)LDDD(CR)	set turnaround delay
TM71-I/O Only	
XX(ESC)M(CR)	read port A, ASCII
XX(ESC)N(CR)	read port A, Decimal
XX(ESC)Qa(CR)	output to port A, ASCII mode
XX(ESC)RDDD(CR)	output to port A, Decimal mode
XX(ESC)SDDD(CR)	output to port B

NOTES:
1. Continuous I/O not allowed in polled operation.
2. A poll address of 00 on an input message or command will be accepted by all terminals, but any transmission will be suppressed from the terminals.
3. n = 1 for ON; n = 0 for OFF.

TABLE III. Output Message Summary - Nonpolled Operation.

TM TO HOST	DESCRIPTION
(MESSAGE CR)	response to ENTER, (ESC)A(CR), (ESC)B (CR), or (ESC)K(CR)
a(CR)	response to XX(ESC)M(CR), ASCII mode
XXDDD(CR)	response to XX(ESC)N(CR), Decimal mode
XX(CR)	response to XX(ESC)A(CR), (ESC)B(CR), or (ESC)K(CR) when output buffer is empty.

TABLE IV. Output Message Summary - Polled Operation.

TM TO HOST	DESCRIPTION
XX(MESSAGE)(CR)	response to XX(ESC)A(CR), XX(ESC)B(CR), or XX(ESC)K(CR)
XXaCR	response to XX(ESC)M(CR), ASCII mode
XXDDD(CR)	response to XX(ESC)N(CR), Decimal mode
XX(CR)	response to XX(ESC)A(CR), (ESC)B(CR), or (ESC)K(CR) when the buffer is empty.

NOTES:
1. XX = polling drop number 01 through 15.
2. ZZ = function message number 01 through 08 or 21 through 26.
3. a = ASCII character to or from port A.
4. DDD = Decimal number 000 through 255 transmitted as three characters.
5. n = control character 0 = off, 1 = on.

USER PROGRAMMABLE READ ONLY MEMORY (PROM)

A 2716 type, 450 nanosecond, EPROM may be inserted into an internal 24-pin socket. This memory may be used to define the function messages, baud rate, polling address, and parity.

Address (Hex)	Memory Content	Comments
0000	AA (Hex)	used to identify ROM presence
0001	0,0,0,0,0,B2,B1,B0	Baud Rate } If FFH control
0002	0,0,0,P0,0,P1,0,0	Parity } reverts to
0003	0,0,0,0,A3,A2,A1,A0	Polling Address } P1 jumpers
0004		Turnaround Delay
0005		XOFF character
0006		XON character
0007		Function Messages
•		
•		
•		
USER PROM MEMORY MAP		

Location 0000 must contain an AA (hex) to indicate that the user PROM is in place.

The baud rate is set between 110 and 19,200 bits per second by entering 00 (hex) through 07 (hex) in location 0001.

Parity is set in location 0002 by entering 00 (hex) for even parity; 10 (hex) for space parity; 04 (hex) for odd parity; or 14 (hex) for mark parity.

The polling address may be 00 to 0F Hex. 00H is nonpolled operation. 01 through 0F represents units 1 through 15.

Turnaround delay is a delay from the time a host command is received until the reply message begins. Unless specified by PROM or RAM, the TM71 uses a delay of 40 milliseconds. The delay can be specified by the PROM in units of 10 milliseconds by putting 00 Hex through FE Hex in location 0004 Hex; FF Hex must not be used. Delays may be from 0 through 2540 milliseconds.

Two line control characters may be put in locations 0005 Hex and 0006 Hex. If this feature is not desired, load these locations with 00 Hex. The first location contains the XOFF character; the second location contains the

XON character. The purpose of these characters is to facilitate the TM71 operation with existing terminal handlers and operating systems such as Digital Equipment Corporation's RSX-11M. These software systems assume multiline terminals and they often respond with several lines in rapid succession. Most systems will provide some means of halting and restarting output. Control S and Control Q are used by RSX-11M. The TM71 will use any two ASCII characters except NUL (00) to automatically halt the next line until the operator presses NEXT, then another line will be received. When this feature is invoked, null lines are ignored; however, lines of one character in length will come to the input buffer. This is necessary to allow the TM71 to recognize its own commands. This feature cannot be invoked by the host; a PROM must be used. When this feature is used, the TM71 operator may log on to an operating system and run a customer-supplied TM71 service program.

Each function message in sequence should be preceded by length byte which gives the number of bytes (characters) in the message as a binary number. The maximum number of message bytes is 1120; the maximum number of messages is 14. If not all messages are to be defined, use a zero length byte to indicate an undefined function message.

Unused locations in the higher address locations should be filled with 00 Hex. Function messages may still be defined in RAM. RAM defined messages are used in place of ROM messages until deleted.

For example, if the first function message were to be STOP, address 0007 would contain 04 Hex to indicate a 4-character message. If all other messages were to be undefined in ROM, the function message memory space would be as follows:

Address	Memory Contents	
0007	04	
0008	53	STOP
0009	54	
000A	4F	
000B	50	
000C	00	
000D	00	
⋮	⋮	
0018	00	

INSTALLATION

Installation of the TM71 consists of mechanical mounting and back panel connector wiring. The TM71 is designed to be mounted on a flat surface. Its back panel provides six threaded holes for attachment; screws are provided. In addition, cutouts must be provided for access to and clearance for P1 and P2. Required mechanical dimensions are discussed later.

Connector wiring for P1 (see Figure 7) may be accomplished with the aid of Tables V, VI, and VII. It is only necessary to connect +5V power, supply return, data transmit (TX), data receive (RX), and signal return to make the TM71 functional. Note that supply return and signal return are internally connected. Without further connections the TM71 will operate at 300 bps, a marking parity bit, nonpolled operation, and the front panel RESET key disabled. Bit rate, parity, and polling operation are set by connecting the indicated pins to supply return on the mating connector. The RESET key is enabled by connecting a jumper between pins 19 and 21 of P1. Request to Send and Clear to Send RS-232-C functions are operative if required by the host system or modem. Clear to Send input is active if left open circuited. Data Terminal Ready output is continuously active. Detailed connection diagrams are provided in Figures 11 and 12.

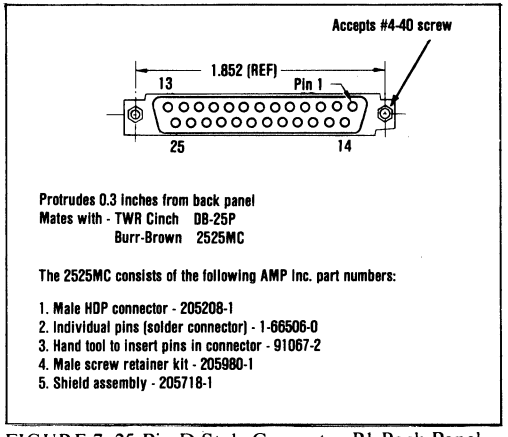


FIGURE 7. 25-Pin D Style Connector P1 Back Panel View.

The 20-pin connector P2 is shown in Figure 8.

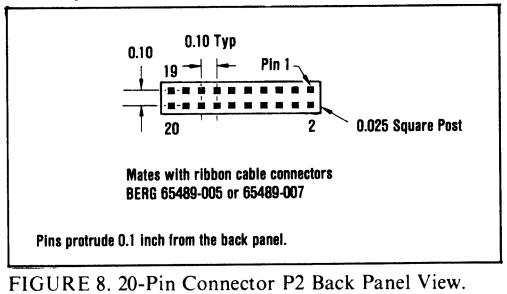


FIGURE 8. 20-Pin Connector P2 Back Panel View.

The RESET key will be disabled at installation if no jumper is installed from pin 19 to pin 21 of P1. When this jumper is removed, the RESET function may be done by a remote switch or a TTL signal through Pin 19. When the jumper is installed, the front panel RESET key may be used to initialize external devices. A "wired OR" connection may also be made.

TABLE V. Listing of Connector P1 Pins.

1	Supply RTN	
2	TX	RS-232-C
3	RX	
4	Request to Send Output	
5	Clear to Send Input	
6	A1 LED (Note 1)	
7	Signal Ground	
8	A2 LED (Note 1)	
9	Parity P0	(Note 2)
10	Parity P1	
11	BAUD B0	
12	BAUD B1	
13	BAUD B2	
14	+5VDC Power Supply	
15	-IN	20mA Current Loops Communication
16	+IN	
17	-OUT	
18	+OUT	
19	RESET IN (Note 4)	
20	Data Terminal Ready Output	
21	RESET OUT	
22	$\overline{A0}$	Polling Address (Note 3)
23	$\overline{A1}$	
24	$\overline{A2}$	
25	A3	

NOTES:
1. A1 and A2 are logic low (< 0.4V at 1.6mA sink) when LED is on.
2. 0 = Jumper to supply return. 1 = Open.
3. 1 = Jumper to supply return. 0 = Open. Address 0000 is nonpolled operation.
4. TTL compatible. Low = Reset.
   Open collector TTL output may be wire ORed with Reset Out (pin 21).

TABLE VI. Setting the Baud Rate

BAUD RATE	B2	B1	B0
300	1	1	1
600	1	1	0
1200	1	0	1
2400	1	0	0
4800	0	1	1
9600	0	1	0
19200	0	0	1
110	0	0	0

Default Baud Rate: 300
0 = Jumper to Supply Return. 1 = Open.

TABLE VII. Setting the Parity Bit.

PARITY BIT	P1	P0
SPACE	0	1
EVEN	0	0
ODD	1	0
MARK	1	1

(MARK = Logic 1)

Default Parity: MARK
0 = Jumper to Supply Return. 1 = Open.

ADDRESS	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$
00 (non-polled)	0	0	0	0
01	0	0	0	1
02	0	0	1	0
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
15	1	1	1	1

Default Address: 00 1 = Jumper to Supply Return.
0 = Open.

Interface to the P2 I/O ports may be accomplished by reference to Table VIII and Figures 9 and 10.

TABLE VIII. Listing of Connector P2 Pins - TM71-I/O.

Pin		
1	B0	Port B, output only
2	B1	
3	B2	
4	B3	Front panel LED's
5	B4	0 = LED ON
6	B5	
7	B6	
8	B7	
9	Signal GND	
10	A0	
11	A1	
12	A2	
13	A3	
14	A4	Port A, input and output
15	A5	
16	A6	
17	A7	
18	$\overline{OS}$	Output strobe
19	$\overline{IS}$	Input strobe
20	Signal GND	

NOTES:
1. Logic positive true for Port A. Negative for Port B.
2. Logic low < 0.4V at 1.6mA. Logic high > 3.5V at 100μA.
3. Mating connector Berg 65489-005 or -007.

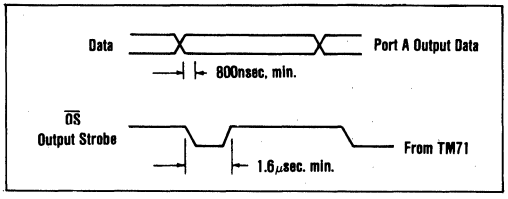


FIGURE 9. Port A Output Timing.

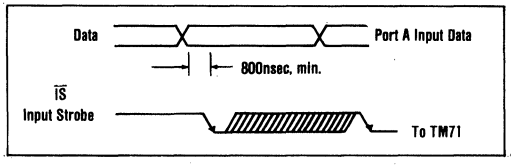


FIGURE 10. Port A Input Timing.

CURRENT LOOP COMMUNICATIONS WIRING CONNECTIONS

TM71 units may be connected to one or more hosts by using the two 20mA current loop circuits. Optical coupling devices are used to electrically isolate TM71 from these circuits. Figures 11 and 12 illustrate connections to typical host communications circuits.

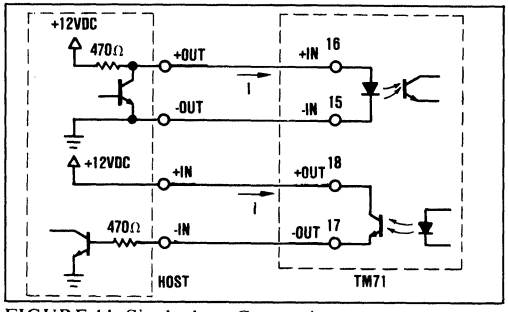


FIGURE 11. Single-drop Connection - Polled Operation.

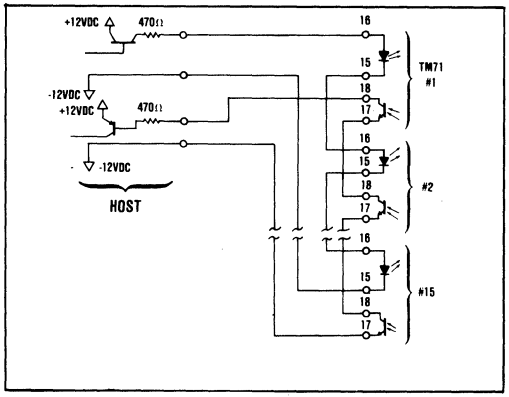


FIGURE 12. Multiple-drop Connections - Polled Operation.

CURRENT LOOP ELECTRICAL SPECIFICATIONS

Input Voltage Drop	≤ 1.3V at 35mA
	≤ 1.2V at 20mA
	≤ 1.2V at 10mA
Input Minimum Current	10mA
Input Maximum Current	30mA
Output Voltage Drop	≤ 1.3V at 10mA
	≤ 1.3V at 20mA
	≤ 1.4V at 35mA
Output Current Minimum	20mA

Output Voltage Drop x Output Current must be ≤ 250mW.

Output Current must be limited by the external circuit.

RS-232-C ELECTRICAL SPECIFICATIONS.

Figures 13 and 14 shown the equivalent input and output circuits.

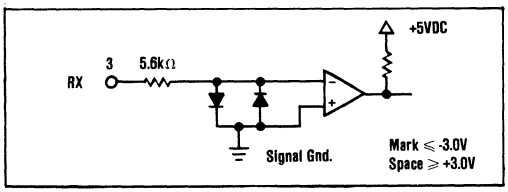


FIGURE 13. Input Equivalent Circuit.

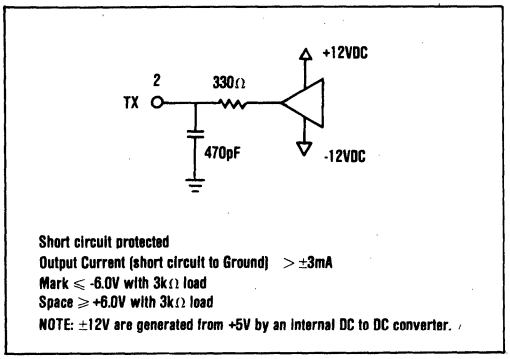


FIGURE 14. Output Equivalent Circuit.

In addition to Transmit (pin 2) and Receive (pin 3) the TM71 supports three other RS-232-C signals:

Request To Send output, RTS, (pin 4)
Clear To Send input, CTS (pin 5)
Data Terminal Ready output, DTR, (pin 20)

These three modem control signals utilize positive logic. In contrast, the data signals on the Transmit and Receive pins use a negative logic (i.e., logic 1 is a negative voltage and logic 0 is a positive voltage). For the modem control signals, the active state (logic 1) is a positive voltage and the inactive state (logic 0) is a negative voltage.

When the TM71 is ready to transmit data, it activates the Request To Send output. When the Clear To Send input is activated, the TM71 transmits. The Data Terminal Ready output from the TM71 is always Active indicating to the host that power is applied and the terminal is available. The three modem control signals do not need to be connected for the TM71 to operate properly. The Clear To Send input is Active if left open.

USER PROM INSTALLATION INSTRUCTIONS

The TM71 has a 24-pin socket on its printed circuit board which will accept 2716 type parts. To install a user PROM, use the following procedure.

- Set the unit face down on a flat surface.
- Remove the six back panel retaining screws.
- Carefully pry the back panel away from the case.
- Remove the four 4-40 nuts which hold the printed circuit board in the case.
- Carefully lift the printed circuit board from the case. Note that the board is connected to the keyboard with a 15-pin, pin and socket connector near the middle of the board. Thus, some resistance will be felt.
- Do not misplace the nylon spacers which are around the four printed circuit board retaining screws under the printed circuit board.
- Put the PROM in the 24-pin socket taking care to not bend the pins and to avoid static electric discharge. The orientation of the part is shown on the printed circuit board.

Note: The PROM sockets may be filled with a protective substance. The PROM should be inserted through this substance.

- Inspect the part and socket to be sure all 24 pins went into the socket.
- Reassemble in the reverse order. Tighten the nuts and screws firmly but do not over-tighten.
- Avoid using penetrating antiloosening products on the internal nuts as they will make it difficult to change the PROM should that become necessary. A nonpenetrating product, which may be removed if necessary, may be used.

MECHANICAL DIMENSIONS

Figure 15 shows the mechanical dimensions for the TM71 and TM71-IO.

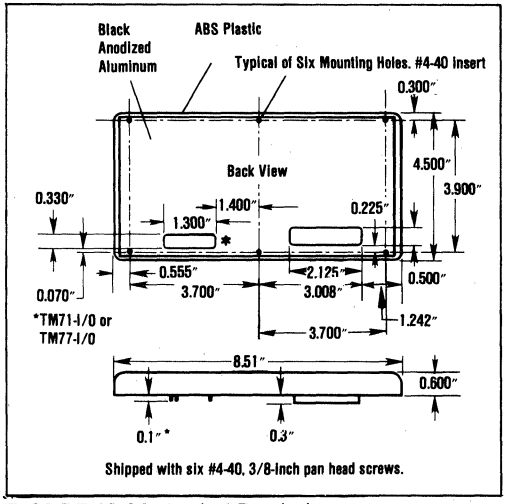


FIGURE 15. Mechanical Deminsions.

POWER REQUIREMENTS

+5VDC ±0.25VDC at 0.65A for Model TM71 and TM77.
+5VDC ±0.25VDC at 0.85A for Model TM71-I/O and TM77-I/O.

ENVIRONMENTAL SPECIFICATIONS

0°C to 60°C.
95% relative humidity noncondensing.
Contact factory for extended temperature range.

FACTORY OPTIONS

None

ACCESSORIES

25-pin mating connector - 2525MC.
20-pin mating connector for I/O ports - 2020MC.

ORDERING INFORMATION

TM71 is the full part number for TM71.
TM71-I/O is the full part number for TM71-I/O.
TM77 is the full part number for TM77.
TM77-I/O is the full part number for TM77-I/O.
2525MC is the full part number for 2525MC.
2020MC is the full part number for 2020MC.

APPENDIX

AMERICAN NATIONAL STANDARD CODE FOR INFORMATION INTERCHANGE.

This coded character set is to be used for the general interchange of information among information processing systems, communications systems, and associated equipment.

TABLE X. ASCII Character Set.

B_{its} b7 b6 b5					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4	b3	b2	b1	COLUMN / ROW	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	iy	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	|
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	—	o	DEL

Control (CTRL) characters, i.e., CTRLX is CAN, etc.

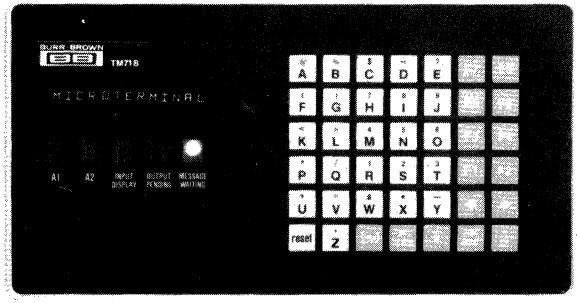
DECIMAL EQUIVALENTS OF ASCII CHARACTERS

Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic	Decimal Code	ASCII Graphic
000	NUL	022	SYN	044	,	066	B	088	X	110	n
001	SOH	023	ETB	045	–	067	C	089	Y	111	o
002	STX	024	CAN	046	.	068	D	090	Z	112	p
003	ETX	025	EM	047	/	069	E	091	[	113	q
004	EOT	026	SUB	048	0	070	F	092	\	114	r
005	ENQ	027	ES	049	1	071	G	093	]	115	s
006	ACK	028	FS	050	2	072	H	094	^	116	t
007	BEL	029	GS	051	3	073	I	095	—	117	u
008	BS	030	RS	052	4	074	J	096	`	118	v
009	HT	031	US	053	5	075	K	097	a	119	w
010	LF	032	SP	054	6	076	L	098	b	120	x
011	VT	033	!	055	7	077	M	099	c	121	y
012	FF	034	"	056	8	078	N	100	d	122	z
013	CR	035	#	057	9	079	O	101	e	123	{
014	SO	036	$	058	:	080	P	102	f	124	|
015	SI	037	%	059	;	081	Q	103	g	125	}
016	DLE	038	&	060	<	082	R	104	h	126	~
017	DC1	039	'	061	=	083	S	105	i	127	DEL
018	DC2	040	(	062	>	084	T	106	j		
019	DC3	041	)	063	?	085	U	107	k		
020	DC4	042	*	064	@	086	V	108	l		
021	NAK	043	+	065	A	087	W	109	m		

LF = Line Feed, FF = Form Feed, CR = Carriage Return, DEL = Rubout.

TM71B AND TM77B MICROTERMINAL/BAR CODE READER USER'S GUIDE

ADVANCE INFORMATION
Subject to Change



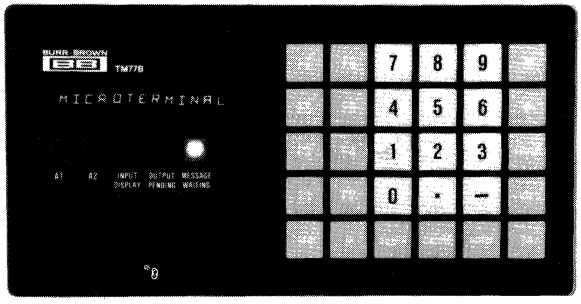


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TABLE OF CONTENTS

INTRODUCTION

If your data collection tracking requirements call for bar code inputs, as well as display and limited keyboard entry, you don't need to buy big, expensive and fragile CRT's with outboard bar code readers. The TM77B and TM71B "microterminals" provide a display and keyboard terminal integrated with a high performance bar code reader.

"Microterminals" - uniquely flexible in application versatility - are designed expressly to fill the human interface demands of widely dispersed control and communications networks - in shop floor control, in factory data collection, inventory control, WIP monitoring, libraries, machine and process control, energy management systems, and information processing. Microterminals, because of their interface flexibility, appearance, size, durability, easy installation, function equally well as consoles and control centers for instruments and small systems. They also perform as input/output terminals in diagnostic applications.

You don't need interface expertise to put microterminals to work for you...they communicate in serial ASCII with RS-422 or RS-232-C conditioning. Baud rates range from 110 to 19,200.

A tough, water resistant front panel protects LED displays and indicators as well as a full numeric keyboard (TM77B) or alphanumeric keyboard (TM71B). Tactile feedback, audible signals, display blinking, and character display confirm operator entry.

Buffered data features reduce on-line input/output time with the CPU and improve accuracy of operator inputs. Because of its design simplicity the mircroterminal concept doesn't require special operator skills or training. Depressing a single function key initiates complex preprogrammed action by the CPU. These functions may be defined in your CPU's software.

Microterminals' very compact design and simple mounting on any flat surface make them quickly adaptable to new or existing applications. All models measure only 218mm x 117mm x 34mm (8.6" x 4.6" x 1.35"). When ordered in OEM quantities the front panel can contain your corporate or system logo.

You can display alphanumeric data with both units. A 30-key numeric keyboard (TM77B) or a 42-key alphanumeric keyboard (TM71B) allows you to enter messages up to 80 characters long. A bar code reader allows you to input messages up to 50 alphanumeric characters long. A 16-character display - with horizontal scroll-left or scroll-right keyboard controls - permits review of data entered before transmission.

Two 80-character buffers are provided for keyboard generated data. The output buffer holds a message being written or reviewed; the transmit buffer holds a prepared message ready for CPU acceptance. This feature allows a second message to be prepared while the first awaits transmission.

Five 50-character buffers are provided, if needed, for stacking bar code messages prior to output to the host processor.

Similarly, two 80-character buffers are available for incoming CPU-generated messages. The receive buffer holds an incoming message until it can be transferred to the input buffer where it is displayed for the operator's action. With this feature, the operator can visually review a CPU input while a second instruction from the CPU can be received and held until called up for display.

The bar code reader can operate in two modes: Auto Wand and Manual Wand. In the Auto Wand mode, scanned data is transferred to the transmit buffer for transmission. In the Manual Wand mode, scanned data is transferred to the output buffer at which time keyboard data may be added to the buffer. Transmission is then initiated by depressing the ENTER key. In both modes, bar code scanned data is shown in the mircoterminal display.

Display features include CPU control of scrolling, flashing, or blanking. The keyboard can also be locked out by CPU command. Two LED indicators are independently controlled by the CPU and three LED's indicate terminal status.

It is important to realize that while the microterminal products including this one have many features, normal operation is very uncomplicated. Virturally untrained operators can use the microterminals productively. Most special features are invisible to the operator. A typical application consists of a series of host-system-supplied operator prompts. To each prompt the operator simply scans a bar code or keys in a short number or message. The function message keys may be used to further simplify operator responses.

OPERATION

DESCRIPTION

The TM77B is a numeric keyboard, alphanumeric display "terminal". The TM71B is an alphanumeric "microterminal". Both units include a bar code reader. They may be used as a remote or local data entry and output terminal for a host computer system. They are intended to provide a rugged, low cost, small size, alternative to a CRT terminal and bar code reader. They are suitable for applications with a limited amount of data interchange, as compared to applications requiring a typewriter-style keyboard and multiline display or hard copy output. Figures 1 and 2 show the front panel of the TM71B and TM77B respectively.

In the remainder of this User's Guide, only the TM77B will be referred to. All information, however, applies to both the TM77B and the TM71B. The only difference is the expanded alphanumeric keyboard of the TM71B.

The TM77B features a dust proof front panel including 13 pre-defined characters and eight function keys on a

30-key keyboard, 16-character alphanumeric display, a bar code reader, two host-computer-controllable light emitting diodes (LED's), and three status LED's. Character height is 0.14". The keyboard features raised embossing with tactile feedback. In addition, a 25-pin, D-style rear panel connector is used to provide power, baud rate selection (110, 300, 600, 1200, 2400, 4800, 9600, and 19,200bps), remote reset in and out, parity selection, a polling address, and RS-422 or RS-232-C interface. There is an additional 14-pin connector, located on the rear panel, which supplies an 8-bit bidirectional port, port A, as well as control input and output strobes which may be used by the host system as a general purpose remote input/output port.

Up to eight function messages may be defined by the host system. After definition by the host, these messages are called for display by the host sending a 3-character code (ESC)ZZ, where ZZ may have the values 01 through 08 and 10 through 19. Function messages may be transmitted to the host by pressing the front panel function message keys. Thus they may be used as extensions of the input message to the TM77B or as function messages to be transmitted by the TM77B operator to the host system.

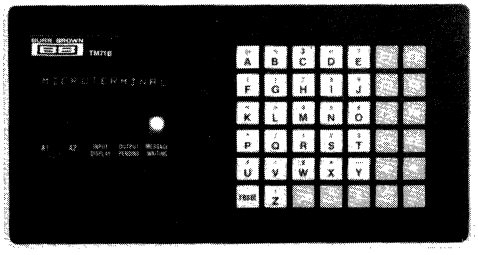

FIGURE 1. TM71B Front Panel.

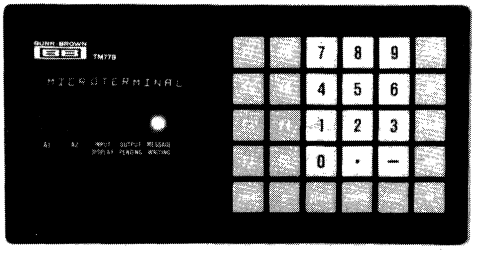

FIGURE 2. TM77B Front Panel.

For all the following descriptions the terms input and output shall refer to input to, and output from, the TM77B. Internal operation of the TM77B is easily conceived as buffer memories for data received and transmitted via the serial interface, as indicated in the block diagram in Figure 3. In addition, the bar code reader provides five 50-character buffer memories for scanned data. Function messages are stored in a separate RAM memory area. The receive buffer receives incoming messages of up to 80 characters and when the message is complete, it is usually automatically transferred to the input buffer. The display buffer is then filled with the first 16 characters of the input message. The operator may then scroll the input message to continuously scroll through the display buffer. The contents of the display buffer are displayed to the operator through 16 alphanumeric characters. The output buffer which serves as temporary storage for keyboard entries is transferred to the transmit buffer when the ENTER key is pressed. At that time the message is transmitted to the host, or in polled operation, held until the host requests the message.

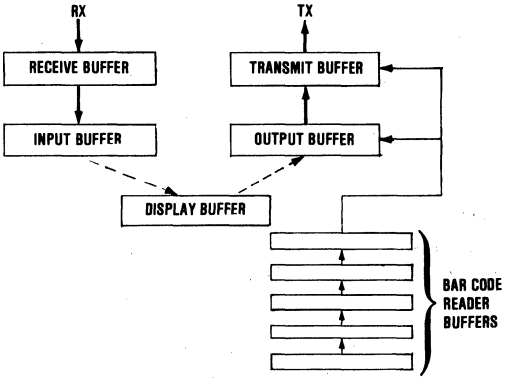

FIGURE 3. TM77B Block Diagram.

Further insight into the operation of the TM77B can be gained by viewing its operation in terms of modes and status conditions. The TM77B has four operating modes and four status conditions.

OPERATING MODES	STATUS CONDITIONS
Ready	Message Waiting
Message Composition	Output Pending
Auto Wand	Input Display
Manual Wand	

OPERATING MODES

READY MODE

The Ready mode is the standby mode; it is entered on power-up or by pressing CE, CLR, or RESET. The symbol ^ in the output display indicates the Ready mode. The other display positions are blank. Ready mode is exited when any character or function message is entered into the output buffer from the keyboard or the bar code wand. The ready indicator will not be visible when an input message is being displayed; however, the terminal may be internally in Ready mode. When the TM77B is in the Ready mode, the receipt of an incoming carriage return CR, causes the display buffer to be loaded with the first 16 characters of the input message. The Input Display LED will come on.

MESSAGE COMPOSITION MODE

Message Composition mode is entered from the Ready mode. If the terminal is in the Ready mode, entering any character or function message from the keyboard causes the terminal to enter Message Composition mode. It is indicated by having a character in the output buffer. A space is the only character that can leave the display buffer blank. Nondisplayable characters are displayed as #. Receipt of an incoming CR causes the Message Waiting LED to come on. Message Composition mode is exited by pressing CE, CLR, RESET or ENTER.

AUTO WAND MODE

Auto Wand mode will append valid data read in the bar code reader to any data in the output buffer of the TM77B, and transfer the output buffer to the transmit buffer. The data in the transmit buffer will be immediately transmitted in Single-Drop mode, or transmitted when polled by the host CPU in Polled mode.

MANUAL WAND MODE

Manual Wand mode will append valid data read in by the bar code reader to any data in the output buffer of the TM77B. This data will not be transmitted to the host processor until the ENTER key is depressed or until the ENTER command is read by the bar code reader. Keyboard data may be entered before or after bar code data is read. Any number of bar code reads may be accepted to the output buffer up to the 80-character limit. Bar code readings are not stacked in the five bar code buffers.

COMMUNICATIONS MODES

The TM77B operates in both the Polled and Nonpolled Communcations modes. In the Nonpolled mode, one microterminal is connected to each host serial communication port. In the Polled mode, up to 63 microterminals may be connected to each host serial communications port.

Nonpolled Mode

In the Nonpolled mode, when a keyboard message is prepared and the ENTER key depressed, the data is immediately transmitted. In the Manual Wand mode, the data is also immediately transmitted when ENTER is depressed. In the Auto Wand mode, bar code data is automatically transmitted when a valid read is performed.

Polled Mode

In the Polled mode, when a keyboard message is prepared and the ENTER key depressed, the data is transferred to the transmit buffer. In the Manual Wand mode, the data is also transferred to the transmit buffer when the ENTER key is depressed. In the Auto Wand mode, bar code data is automatically transferred to the transmit buffer when a valid read is performed.

The transmit buffer is transmitted to the host processor when the host sends the polling command (Request Buffer). The Output Pending LED indicates that a message has been transferred to the transmit buffer, but the host has not yet polled the microterminal.

In the event there was an error in the transmission (wrong address, parity error, etc.), the buffer data can be requested again by the retransmit buffer command. If the request buffer command is sent again, a null message is transmitted to indicate no new data has been entered. This distinguishes between repeated data and new data.

When the host sends messages or commands to the TM77B, they must be prefixed by two ASCII digits in the range 00 to 63 (see Table I). Address 00 is a special case which is accepted by all terminals addressed from 01 to 63. This allows a single message to be received by all terminals on the multidrop line at the same time.

TABLE I. Polling Address Selection.

ADDRESS	$\overline{AE}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	
00	0	0	0	0	0	0	Nonpolled
01	0	0	0	0	0	1	
02	0	0	0	0	1	0	
03	0	0	0	0	1	1	
31	0	1	1	1	1	1	
32	1	0	0	0	0	0	
33	1	0	0	0	0	1	
63	1	1	1	1	1	1	

Address lines $\overline{A0}$ through $\overline{A4}$:
Logic 0 = open
Logic 1 = jumper to signal ground.

Address extension $\overline{AE}$:
Logic 0 = open
Logic 1 = jumper to ENABLE, pin 18.

The RS-422 interface must be used when more than one TM77B is connected to the communications interface. See Illustration section for suggested connections. Up to 63 microterminals may be connected to a single communications part using RS-422. Since terminals are connected to the RS-422 interface in parallel, removing one terminal does not break the line or interface with operation of the remaining terminals.

ERROR CONTROL PROTOCOL

The TM77B has two types of error control modes - Normal mode and Extended Control mode.

In Normal mode, data transmitted to the TM77B may contain parity for each character. If the microterminal receives a character with a parity error, that character will be ignored but the remainder of the transmission will be received.

In Extended Control mode, the TM77B monitors parity for each incoming character as well as a checksum for each message. If the message is received correctly, the TM77B will transmit an acknowledgement to the host CPU. If the TM77B detects a parity or checksum error, the entire message is ignored and a message is sent to the host CPU indicating that an error has been received.

STATUS CONDITIONS

MESSAGE WAITING

Message Waiting status is the condition of being in Message Composition mode when the host sends an input message. The Message Waiting LED comes on to indicate a new input message is in the input buffer and may be viewed at the operator's convenience by pressing RECALL, ENTER or CE. When any of these actions are taken, the Message Waiting LED goes off until the host sends another message while the terminal is in Message Composition mode. In addition, if the host sends a new message before the input buffer had been examined, the message is held in the receive buffer. The Message Waiting LED stays on until the operator presses RECALL. This causes the message to be transferred to the input buffer.

OUTPUT PENDING

Output Pending status occurs when the terminal is used in a polled configuration, as determined by rear panel connector jumpers, and an output message has been enabled by the ENTER key. The message is actually transmitted when the host polls the terminal. Until this happens the Output Pending LED stays on. In many installations this will happen so quickly that the operator may never actually see the LED come on. However, if the host were temporarily occupied with another task, the operator would know that the message had not been transmitted. The message actually enters the transmit buffer and waits there until the terminal is polled. A second output message may be composed in the output buffer; however, if ENTER is pressed for the second message before the Output Pending LED goes off, the first message is lost.

INPUT DISPLAY

The Input Display LED indicates when the display buffer is viewing the input buffer. This can happen in two ways. When the terminal is in Ready mode, an input message will automatically switch the display buffer to the input buffer causing the Input Display LED to come on. The Ready Indicator will no longer be visible; however, the terminal is still in the Ready mode.

When the terminal is in Message Composition mode, pressing RECALL switches the display buffer to the input display causing the Input Display LED to come on. The terminal is still in Message Composition mode. Pressing RECALL a second time will return the display buffer to its former position in the output buffer.

OPERATING INSTRUCTIONS

When power is applied to the TM77B, the Input Display LED will come on and the display will show the Ready Indicator which is a Λ in the left-most character position. A message consisting of up to 80 characters, including spaces, may be entered from the keyboard. Pushing the ENTER key causes the message to be transmitted to the host computer. The message will be sent each time ENTER is pressed; this is indicated by the display blinking. A bar code may be transmitted to the host computer by scanning a valid sequence. In Polled mode the Output Pending LED will come on until the host takes the keyboard or bar code message. The output buffer may be cleared by pressing CE. Pressing a key to start a new message will automatically clear the output buffer has been cleared by CE. In addition, the Function Message keys may be used to enter up to 16 different function messages into the output buffer.

In Ready mode, when a message is received from the host computer, the first 16 characters of the message appear on the display. The Input Display LED comes on to indicate the display buffer is filled with a section of the input buffer. The entire message may be viewed by using ROL and ROR keys. When one of these keys is held down, the message will scroll through the display at approximately six characters per second. When any character key is pressed, the Input Display LED goes out and the character appears in the left-most part of the display with the rest of the display blanked. As other character keys are pressed, the message grows from left to right. DEL deletes the last character. If DEL is held down, characters will be deleted at approximately six characters per second.

The TM77B will power-up in Auto Wand mode. The unit can be software-switched from one mode to another. Internally, the TM77B consists of 80-character receive and input buffers, a 16-character display buffer, 80-character output and transmit buffers, and five 50-character bar code data buffers. The display buffer is used to scan either the input buffer or the output buffer. It is switched from one to the other by pressing RECALL. When the display buffer is displaying the input buffer, the front panel Input Display LED will be on. Complete operating details are contained in the following section.

DETAILED KEY DESCRIPTIONS

NUMERIC KEYS

The numeric keyboard includes the digits 0 through 9, a minus sign and decimal point.

FUNCTION MESSAGE KEYS [*] [F1] [F2] etc.

These keys are used to input function messages from the keyboard. The function messages may be one of the default strings &XX or it may be a user-defined string. When no user-specified string definition has been provided, the three characters of the default string appear. For a user-defined value, the last 16 characters of the string definition appear in the display.

Incoming function messages appear with their first 16 characters in the display.

The first eight function messages are put in the output buffer by pressing F1 through F8 keys and the remaining eight by pressing #/F1 through #/F8.

When no message has been defined, default messages appear in the display as &ZZ. ZZ represents 01 through 08 for function keys F1 - F8 and 11 through 18 for keys #/F1 through #/F8 for a total of 16 values.

DISPLAY CONTROL [◄] [►]

In normal operation pressing [◄] will cause the message to move one character position to the left or until the last character of the message being examined is in the right-most position of the display. Pressing [►] causes the message to move one character to the right or until the first character of the message down causes the display to scroll by at approximately six characters per second until the first character is in the left-most, or the last character is in the right-most character position. Thus, in the Manual Wand mode, valid bar code data which is transferred to the output buffer can be inspected by pressing [◄] and [►].

RESET [RESET]

The RESET key allows the TM77B operator to initialize the internal functions. Pressing RESET is equivalent to turning on the power. Pressing RESET will cause host-defined messages to be lost. RESET may be disabled when the TM77B is installed.

SPACE KEY [SPACE]

SPACE causes a blank to be entered into the output buffer. The right-most character becomes a blank.

DELETE KEY [DELETE]

DELETE deletes the right-most character.

ENTER KEY [ENTER]

ENTER is used to send messages from the output buffer to the host system. The ENTER key is used to input bar code data when in the Manual Wand mode.

RECALL KEY [RECALL]

If it is desired to examine the input message before entering or even completing the output message, the RECALL key may be pressed which causes the display buffer to be filled with the first 16 characters of the input message. The Input Display LED will come on. The input message may be examined by using [◄] and [►]. Pressing RECALL a second time will cause the display register to be filled with the 16 characters of the output buffer it contained when RECALL was pressed the first time. The Message Waiting LED is turned off, and remains off, after the first input message access with the RECALL key. Accessing the input message a second time fills the display buffer with the 16 characters it contained when the output message was accessed. Thus, if required, the operator can work through the input message composing an output message in response to small sections of the input message.

CLEAR ENTRY AND CLEAR ALL KEY [CE] [CLR]

Pressing CE causes the TM77B to exit Message Composition mode and the Ready Indicator to come on. The output buffer only is cleared.

Pressing CLR causes the TM77B to exit message Composition mode, clears Output Pending LED, and causes the Ready Indicator to appear. The output, input, and receive buffers are cleared. The transmit buffer is not cleared. Although the Output Pending LED goes off, the host may still read the transmit buffer. Host-specified function messages are unaltered. Pressing RESET, if enabled by the back panel jumper, has the same effect; plus it sets function messages to their default power-up condition and clears the transmit and five bar code buffers.

AUDIBLE OUTPUT

The TM77B has audible outputs for the following functions:

1. Successful bar code scan audible output. A single tone "beep" indicates that a bar code has been successfully scanned.
2. Buffer full audible alarm. A dual tone alarm signal indicates that the five bar code buffers (in Auto Wand mode) or the 80-character output buffer (in Manual Wand mode) are full and the terminal will not accept further inputs until data is transmitted.
3. BEL code audible output. A single tone "beep" indicates that a key has been depressed. This feature is normally not enabled. It is enabled under control of the host CPU
4. Key depression audible indication. A single tone "beep" indicates that a key has been depressed. This feature is normally not enabled. It is enabled under control of the host CPU (ESC)Un(CR).

The audible output signal is available as a TTL level signal, BEEPER, on pin 10 of the P1 connector. BEEPER is active whenever the audible alarm is sounding. BEEPER is a positive true level which goes "high" when activated.

APPLICATIONS

CONTROL FEATURES

Certain input messages may be used by the host system to put the TM77B in special modes. Much of this is explained by the input messages of the Input Message Summary part of the Communications Protocol section. Additional comments are provided here.

SCROLL DISPLAY mode causes any input message, being observed through the display, to circulate continuously from right to left at approximately six characters per second.

FLASH DISPLAY causes any input buffer display to flash with 50 percent duty cycle approximately three times per second.

BLANK DISPLAY causes any output buffer display to have all segments off. The input buffer will still be displayed.

KEYBOARD LOCKOUT inhibits use of the keyboard, except RESET.

SCROLL and FLASH may be stopped by use of CE, CLR, or RESET. BLANK DISPLAY and KEYBOARD LOCKOUT may be terminated from the keyboard with RESET.

REMOTE ENTER causes the input buffer to be transferred to the transmit buffer and sent to the host computer. It will also transmit bar code read data from the output buffer to the host computer if the TM77B is in the Manual Wand mode. REMOTE ENTER may be used to test the TM77B, communications lines and host processor communications circuits.

REMOTE CLEAR causes the same action as pressing CLR. That is, the receive, input, and output buffers are cleared.

The TM77B RAM has 415 character locations which may be used for function messages. The function messages may be any length less than or equal to 70 characters as long as the total number of characters does not exceed 415. This memory is assigned dynamically by the TM77B software. This means up to five messages may be 70 characters each if only five are defined. Attempting to exceed this boundary will cause unpredictable results. Alternately, a maximum of eight messages of 50 characters each could be defined. The RAM definitions are used by the TM77B until the RAM definitions are deleted. This may be done with the RESET key or from the host processor.

Function messages may contain any of the 128-character ASCII set.

When control ASCII characters are part of normal input messages, they are stripped; however, they may be part of commands such as function message definitions.

All function messages are transmitted to the TM77B as (ESC)Z where ZZ represents 01 through 08 and 10 through 19. For output, &ZZ will be used as a default string if no message definition has been made in RAM. In this case the message will be transmitted as defined.

The sequency (ESC)ZZ is considered to be part of a message. Do not confuse it with one of the (ESC) commands in the Input Message Summary Section. For example, (ESC)1(CR) is a complete and normal input message; it causes function message 1 to be put in the input buffer. Refer to Figure 4 which shows the Displayable Characters.

CTRL X (Communication line entry only)

The control character CAN(CTRL X) of the ASCII set has special meaning to the TM77B. When it is the first character of an input message, or the first character after the address characters in Polled operation, the TM77B will clear its receive and input buffers of previous messages and blink the Message Waiting LED once. A new message following CRTL X will be in the input buffer. A command following CTRL X will be executed. This may be important for high priority messages to the operator. If the operator leaves the TM77B in Message Composition mode and two messages have been received, the first message will be in the input buffer and the second in the receive buffer. A third message or command will not be received unless (CTRL X) is used to clear the receive and input buffers. When the TM77B is in Ready mode, all messages come to the input buffer and the terminal goes to input display status. In this case the (CTRL X) has no effect on operation.

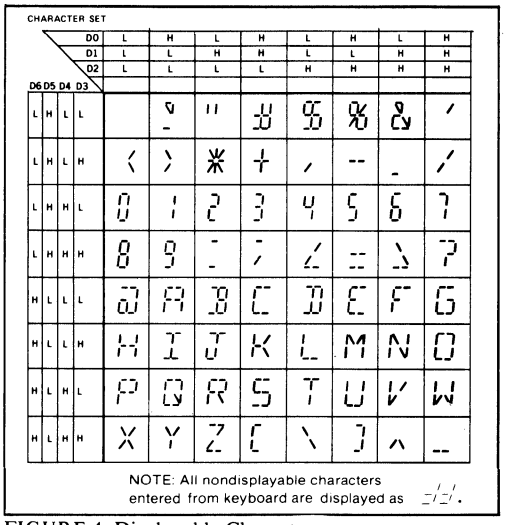

FIGURE 4. Displayable Characters.

TURN AROUND DELAY

When commands that cause an automatic reply are sent from the host, the TM77B can delay its reply for a programmable turn around time. The purpose of this feature is to allow the TM77B to operate with any host terminal handler software which cannot accept input immediately following the carriage return of a host output message. This is the case in many host systems. This delay has a default value of 40msec. This may be changed by the host by using the command string (ESC)LDDD(CR) where DDD represents 000 through 254. This number sets the delay in increments of 10msec from 0 to 2.54 seconds.

SELF TEST MODE

The TM77B has provision for performing a self-test diagnostic routine. Self Test is entered by holding down any key while RESET is pressed and released. The message "RAMxxxROMxxxI/Oxxx" is put in the display buffer and the write/read memory test is performed. If the memory test passes, a "+" is put after "RAM"; else if there is a failure a "-" is put in the display.

Similarly, a program ROM checksum is calculated and compared with a ROM stored checksum. The same pass/fail indicator is displayed. The I/O is tested by a write/read cycle to the internal I/O device, and rotating test is performed on the Status LED's.

This sequence is repeated until RESET is pressed and released while no other key is pressed, which will then allow the TM77B to perform a normal power-up. During Self Test mode the TM77B is off-line and will not receive or transmit to a host processor.

Self Test can only be accomplished if the back panel connector reset jumper is connected between pins 19 and 21.

COMMUNICATION DELAYS

Some operations require a delay before the TM77B can accept another message or command. When a function message is defined, the TM77B requires at least 150msec before another message or command can be received. A host message which calls a predefined function message requires 1msec for each function message called before another message or command can be received.

When software is written in a high level language, delays between messges will normally occur. When programs are written in assembly language on small systems such as single board computers, it may be necessary to design delays into the system software. Should the need arise, this is easily accomplished for high level languages as well. It is recommended that I/O commands to control port A for TM77B be followed by a 40msec.

IMMEDIATE TRANSMISSION OF FUNCTION MESSAGES

A function message can be transmitted immediately if the ASCII control character RS (Record Separator) is the last character of the definition. When this character is encountered while getting the function message from RAM or PROM, is is treated as if the ENTER key were pressed. This causes the function message to be transmitted along with any characters that were in the buffer when the function key was pressed.

This feature, when used with CTRL D, allows function messages to have a completely user-determined end-of-line character string. This is accomplished by defining a function message as follows: (ESC)D02(MESSAGE)(CTRL D)(RS)(CR).

When the F2 function key is pressed, (MESSAGE) preceded by any contents of the output buffer, is immediately transmitted. (MESSAGE) may include any type of line terminators such as (LF) or (EXT). (CTRL D) prevents the TM77B from adding a (CR) and (RS) causes immediate transmission without the use of the ENTER key.

The use of (RS) is especially important for high priority control messages for which it is desired that only one key be pressed.

The only restriction on the message is the use of (CR). (CR) may not be contained in host-defined function messages. This is necessary because an imbedded (CR) will terminate the function definition.

COMMUNICATIONS PROTOCOL

The TM77B sends and receives 7-bit asynchronous ASCII character codes with one parity bit and two stop bits. One or two stop bits will be accepted for input. When parity is disabled, a mark or space as determined by P1 jumpers is inserted for the parity bit. Parity may be even or odd and is selected by jumpers on P1.

Characters with parity errors are displayed as non-displayable characters ■. These jumpers also select the data receive and transmit rate. This rate may be 110, 300, 600, 1200, 4800, 9600, or 19,200bps.

Each message transmitted from the TM77B is terminated with a carriage return character. When operated in Polled mode, each message is preceded with its 2-character polling drop number. This is not counted as part of the 80 character message.

For an input message, the TM77B requires that the message of up to 80 characters in length be terminated by a carriage return. Line feeds following a carriage return are discarded; otherwise they are displayed as non-displayable characters. Line feeds will be ignored as the first character of a message. A carriage return is not counted as one of the input characters. In Polled mode the message must begin with a drop number 00 through 63. This is followed by up to 80 characters plus a carriage return. When the host polls the TM77B, it must send (ESC)XXAA(CR) where XX is the drop number of the particular TM77B (01 to 63). Drop number 00 causes an input message to be received by all terminals.

Function messages of up to 80 characters in length may be defined by sending (ESC)DZ(MESSAGE)(CR). In Polled mode this would be XX(ESC)DZ(MESSAGE)(CR). Z represents the function message number 1 through 8. Defined messages may be deleted by sending a new definition or (ESC)kDZ(CR). (ESC)D0(CR) deletes all function message definitions.

To call a function message to the display from the host, the host sends (ESC)ZZ within a normal message or merely (ESC)ZZ(CR). The display buffer shows the defined function message when a definition is present in RAM. The defined function message is transmitted on output. When no message has been defined, &ZZ is shown in the display of input and output messages. &ZZ is also transmitted in output messages when no function message has been defined.

It is important to remember the distinction between the host defining a function message and entering a message in the input buffer. The host may define function messages without entering them when they are for use by the operator through the function message keys.

USER INPUT/OUTPUT PORT

The TM77B has one 8-line input/output port, referred to as Port A. It is accessed through a 14-pin connector. Each line will drive one TTL load.

Port A is a user I/O port. It is a fully bidirectional bus, with an input strobe and an output strobe. It has two data modes - Decimal mode and ASCII mode. In Decimal mode, the data is encoded as three ASCII characters and represents the decimal numbers 000 through 255. In ASCII mode, port data is encoded as single ASCII characters.

Port A has two operational modes - continuous and noncontinuous. In the Noncontinuous mode data is

transferred one ASCII character (ASCII mode) or three decimal numbers (Decimal mode) per host processor command. In the Continuous mode data may be continuously transferred in and out of the port. The terminal responds only to the input message (ESC) which stops continuous input and output. In this mode, protocol is mostly determined by the host and the device connected to Port A. In the Continuous mode, the display holds the last display data and the keyboard is locked out. The Continuous mode is only usable in the Nonpolled mode.

To summarize, port A has two data modes (ASCII and Decimal), two operational modes (Continuous and Non-continuous) and may be used with or without parity.

To characterize the operation of Port A, eight cases must be considered:

Decimal, Noncontinuous, No Parity

Decimal mode uses three characters to form a number from 000 through 255. This number gives full control to the eight output bits of Port A. For input from Port A, the eight bits are translated to a number from 000 through 255 and transmitted to the host as three ASCII characters. The most significant digit is received and sent first. This mode is convenient for applications programs written in a high level language such as BASIC or FORTRAN. The I/O statements of such languages will allow the applications program to communicate directly with Port A without the need to call assembly language subroutines.

On data input from the host processor, the eighth bit of each character may be a one or zero. If the host cannot control the eighth bit, it merely sends two stop bits. The TM77B will interpret the first stop bit as the eighth bit (B8=1) and the second as the stop bit. On output the TM77B will set the eighth bit to one or zero (mark or space) as determined by its connector jumpers. Use "bit eight equals one" to stimulate two stop bits if the host expects two stop bits. This is the case when no jumpers are connected (Mark parity).

Decimal, Noncontinuous Parity

This mode operates exactly as the previous mode except that parity is used. When parity error are found in Port A data from the host, the data is not output to Port A. Characters are sent to the host with the parity bit set appropriately.

Decimal, Continuous, No Parity

In this mode, Port A data may be sent from the host as a continuous stream of 3-character data as follows:
DDD(CR)DDD(CR)

Input from Port A is handled in a similar way. Each input strobe causes DDD(CR) to be sent to the host. If Port A is strobed faster than the transmission line can take the data, more than three characters will be sent between carriage return characters.

The last three will indicate the data correctly at the time of the last strobe. Decimal Continuous mode is entered by the command string (ESC)P(CR). Parity is not checked and the eighth bit has the same consideration as discussed in Decimal, Noncontinuous, No Parity.

Decimal, Continuous, Parity

The port operates in this mode exactly as in the previous mode except that parity is used. When a parity error is found in any of the three data characters from the host, the data is not output to Port A. Input from Port A will have the appropriate parity bit added for transmission to the host.

ASCII, Noncontinuous, No Parity

In this mode, a single ASCII character is received from the host and output to Port A. Bit 8 of Port A is not controlled. No check of the eighth bit input to Port A is made. The eighth bit considerations of the serial communications line characters are the same as discussed in the Decimal, Noncontinuous, No Parity. On input from Port A the eighth bit of the serial characters transmitted to the host is set according to the jumpers on P1 as a mark or space. A port output is illustrated by the string (ESC)Qa(CR). The "a" represents any of the 128, 7-bit, ASCII characters.

ASCII, Noncontinuous, Parity

In this mode, the port operates exactly as in the previous mode except that parity is used. When a parity error is detected in the host input data, no output to Port A is made. For input from Port A to the host, the parity bit is set appropriately, and the string (a)(CR) is transmitted to the host.

ASCII, Continuous, No Parity

In this mode the host sends a continuous stream of characters (a)(a)(a)... Input from Port A to the host is handled in a similar way. Bit 8 is not checked or altered by the TM77B, input from the port is transmitted as received. This means that the TM77B does not alter 8-bit data. The host and the device connected to Port A may send and receive parity if they choose. Thus, the TM77B serves only as a serial-to-parallel and parallel-to-serial converter. This mode is entered by the host sending the string (ESC)O(CR). The continuous operation (ESC) character terminates continuous operation.

ASCII, Continuous, Parity

In this mode, the port operates as in the previous mode except that the terminal uses parity. If a parity error is detected in the continuous stream from the host, the character with the error will not be output to Port A. The terminal will set the parity bit on data input from the port.

DECIMAL MODE

The decimal numbers from 000 through 255 represent all the 256 possible combinations of eight bits. Thus, each of the 8-bit lines may be individually controlled.

To convert from the desired binary bit pattern to the corresponding decimal number the following method may be used.

b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1

$$DDD = \sum_{N-1}^{8} 2^{N-1} = 1b, 2b_2 + 4b_3 + 8b_4 + \text{----} + 128b_8$$

Additional features are illustrated in Tables II, III, IV, and V and in the Control Features section.

COMMAND DESCRIPTIONS

The TM77B accepts a number of different Escape (ESC) sequences which serve as special commands. These commands consist of character strings starting with the ASCII control character (ESC) and terminated with a carriage return (CR).

(ESC)A(CR)

The A command polls the TM77B for any new output message which has been entered from the keyboard or bar code reader. This command may be used only once per message and is used only in Polling mode.

(ESC)B(CR)

The B command polls the TM77B for any new or old message in its output buffer. It may be used to cause the TM77B to transmit one entered message any number of times.

(ESC)C(CR)

The C command clears the input buffer.

(ESC)DZZ(MESSAGE)(CR)

The D command used with a message is used to define function messages in the TM77B RAM. The ZZ must be any number character from 01 through 08 and 10 through 19. When the MESSAGE is not included in the escape sequence, the ZZ function message definition is deleted. If ZZ equals 00 and the message is not included, all function message definitions are deleted. When function messages are deleted from RAM, they assume the default values &ZZ.

(ESC)En(CR)

This command is used to set the A1 LED on or off. If n=1, the LED is turned on. It is turned off for n=0. The back panel A1 TTL output is pulled low when the LED is on.

(ESC)Fn(CR)

This command serves for A2 as the previous E command does for A1.

(ESC)Gn(CR)

When n=1, the display continuously scrolls through the input buffer. Scrolling is stopped with n=0.

(ESC)Hn(CR)

When n=1, the display flashes message in the input buffer. The flashing is stopped with n=0.

TABLE II. Input Message Summary - Nonpolled Operation.

(MESSAGE)(CR)	Input message
(ESC)A(CR)	Request transmit buffer
(ESC)B(CR)	Retransmit transmit buffer
(ESC)C(CR)	Clear input buffer
(ESC)DZ(MESSAGE)(CR)	Define function message
(ESC)DZ(CR)	Delete function message
(ESC)DO(CR)	Delete all function messages
(ESC)En(CR)	Output to A1 LED
(ESC)Fn(CR)	Output to A2 LED
(ESC)Gn(CR)	Scroll display control
(ESC)Hn(CR)	Flash display control
(ESC)In(CR)	Blank display control
(ESC)Jn(CR)	Keyboard lockout control
(ESC)K(CR)	Remote ENTER
(ESC)LDDD(CR)	Set turnaround delay
(ESC)M(CR)	Read port A ASCII
(ESC)N(CR)	Read port A Decimal
(ESC)O(CR)	Port A continuous ASCII
(ESC)P(CR)	Port A continuous Decimal
(ESC)Qa(CR)	Output "a" to port A, ASCII mode
(ESC)RDDD(CR)	Output to port A, Decimal mode
(ESC)T(CR)	Clears input, receive and output buffers
(ESC)Un(CR)	Keyboard audible indication control
(ESC)Vm(CR)	Auto Wand/Manual Wand control
(CONTROL)X	Clears receive and input buffers
(ESC)	Halt continuous I/O.

NOTES:

1. Parenthesis are not actually encoded. Shown for copy clarity only.
2. (ESC) control commands may not be embedded in messages.
3. n = 1 for ON: n = 0 for OFF.
4. Z is function number, 1 to 8
5. "a" is ASCII character
6. m = 1 for Auto Wand; m = 0 for Manual Wand.

TABLE III. Input Message Summary - Polled Operation.

XX(MESSAGE)(CR)	Input message
XX(ESC)A(CR)	Request transmit buffer
XX(ESC)B(CR)	Retransmit transmit buffer
XX(ESC)C(CR)	Clear input buffer
XX(ESC)ZZ(MESSAGE)(CR)	Define function message
XX(ESC)ZZ(CR)	Delete function messages
XX(ESC)DO(CR)	Delete all function messages
XX(ESC)En(CR)	Output to A1 LED
XX(ESC)Fn(CR)	Output to A2 LED
XX(ESC)Gn(CR)	Scroll display control
XX(ESC)Hn(CR)	Flash display control
XX(ESC)In(CR)	Blank display control
XX(ESC)Jn(CR)	Keyboard lockout control
XX(ESC)K(CR)	Remote ENTER
XX(ESC)LDDD(CR)	Set turnaround delay
TM77B	
XX(ESC)M(CR)	Read port A, ASCII
XX(ESC)N(CR)	Read port A, Decimal
XX(ESC)Qa(CR)	Output to port A, ASCII mode
XX(ESC)RDDD(CR)	Output to port A, Decimal mode
XX(ESC)T(CR)	Clears input, receive, output buffers
XX(ESC)Un(CR)	Keyboard, audible indication control
XX(ESC)Vm(CR)	Auto Wand/Manual Wand control

NOTES:

1. Continuous I/O not allowed in polled operation.
2. A poll address of 00 on an input message or command will be accepted by all terminals, but any transmission will be suppressed from the terminals.
3. n = 1 for ON; n = 0 for OFF.

TABLE IV. Output Message Summary - Nonpolled Operation.

MESSAGE(CR)	Response to ENTER, (ESC)A(CR), (ESC)B(CR) or (ESC)K(CR)
a(CR)	Response to (ESC)M(CR), ASCII mode
DDD(CR)	Response to (ESC)N(CR), Decimal mode
(CR)	Response to (ESC)A(CR), (ESC)B(CR), or (ESC)K(CR) when output buffer is empty.

TABLE V. Output Message Summary - Polled Operation.

XX(MESSAGE)(CR)	Response to XX(ESC)A(CR), XX(ESC)B(CR), or XX(ESC)K(CR)
XXaCR	Response to XX(ESC)M(CR), ASCII mode
XXDDD(CR)	Response to XX(ESC)N(CR), Decimal mode
XX(CR)	Response to XX(ESC)A(CR), (ESC)B(CR), or (ESC)K(CR) when the buffer is empty.

NOTES:
1. XX = polling drop number 01 through 16.
2. ZZ = function message number 01 through 08 or 10 through 19.
3. a = ASCII character to or from port A.
4. DDD = Decimal number 000 through 255 transmitted as three characters.
5. n = control character 0 = off, 1 = on.

(ESC)In(CR)

When n=1, data in the output buffer from the keyboard or bar code reader is not displayed. Data from the host processor in the input buffer is displayed normally. Data is transmitted normally even when the output display is blanked. Blanking is stopped when n=0.

(ESC)Jn(CR)

When n=1, the keyboard is locked out. The keyboard is enabled if n=0. This command does not affect bar code data.

(ESC)K(CR)

The K command moves data from the input buffer to the transmit buffer for immediate transmission. This command is used for testing communications circuits and lines.

(ESC)LDDD(CR)

This command sets the delay time from receipt of a command from the host processor to the automatic replay. DDD is 000msec to 255msec. Default is 40msec.

(ESC)M(CR)

Reads port A once in ASCII mode, one character.

(ESC)N(CR)

Reads port A once in Decimal mode, three characters.

(ESC)O(CR)

Sets port A to continuous, ASCII mode, nonpolled only.

(ESC)P(CR)

Sets port A to continuous, Decimal mode, nonpolled only.

(ESC)Qa(CR)

Outputs one character, "a", to port A, ASCII mode.

(ESC)RDDD(CR)

Outputs three characters, "DDD", to port A, Decimal mode.

(ESC)T(CR)

The T command clears input and output buffers and places the TM77B in Ready mode. Action is same as using the CLR key.

(ESC)Un(CR)

The U command controls the keyboard audible indication signal. When n = 1, an audible signal indicates each key depression. When n=0, there is no audible signal on key depression. n=0 is default state.

(ESC)Vm(CR)

When m=1, the Auto Wand mode is enabled. When m=0, the Manual Wand mode is enabled.

CONTROL X

The control X command character clears receive and input buffers even if both are full. This command is the only one without the ESCAPE character and not terminated with a carriage return (CR). The sequence (CONTROL X)(ESC)T(CR) guarantees that the receive, input and output buffers are cleared.

INSTALLATION

Installation of the TM77B consists of mechanical mounting and back panel or edge connector wiring. The TM77B is designed to be mounted on a flat surface. Its back panel provides six threaded holes for attachment; screws are provided. In addition, cutouts must be provided for access and clearance to connectors P1 and P2. Required mechanical dimensions are discussed later.

Connector wiring for P1 (see Figure 5) may be accomplished with the aid of Tables VI, VII, and VIII. It is only necessary to connect +5V power, supply return, data transmit (TX), data receive (RX), and signal ground to make the TM77B functional. Note that supply return and signal ground are internally connected only if the 5VDC power supply option is used. Without further connections the TM77B will operate at 300bps, a marking parity bit, nonpolled operation, and the front panel RESET key disabled. Baud rate and polling addresses are set by connecting the indicated pins to signal ground (pin 7) on the mating connector. Parity and $\overline{AE}$, the polling address extension, are set by connecting the indicated pins to ENABLE (pin 18). The RESET key is enabled by connecting a jumper between pin 19 and pin 21 of P1. Request to Send and Clear to Send RS-232-C functions are operative if required by the host system or modem. Clear to Send input is active if left open-circuited. Data Terminal Ready output is continuously active (detailed connection diagrams are provided in Figures 10 and 11).

The RESET key will be disabled at installation if no jumper is installed from pin 19 to pin 21 of P1. When this jumper is removed, the RESET function may be done by a remote switch or a TTL signal through Pin 19 (see Figure 6). When the jumper is installed, the front panel

RESET key may be used to initialize external devices. A "wired OR" connection may also be made.

TABLE VI. Listing of Connector P1 pins.

	RS-232-C			RS-422	
1	Supply Return		1	Supply RTN	
2	TX	RS-232-C	2	+OUT	RS-422
3	RX		3	-OUT	
4	Request to Send Output		4	+IN	
5	Clear to Send Input		5	-IN	
6	A1 LED		6	A1 LED	
7	Signal Ground		7	Signal Ground	
8	A2 LED		8	A2 LED	
9	$\overline{A4}$		9	$\overline{A4}$	
10	BEEPER		10	BEEPER	
11	BAUD B0		11	BAUD B0	
12	BAUD B1		12	BAUD B1	
13	BAUD B2		13	BAUD B2	
14	24VAC/5VDC Power In		14	24VAC/5VDC Power In	
15	Parity P0		15	Parity P0	
16	Parity P1		16	Parity P1	
17	Address Extension		17	Address Extension	
18	ENABLE		18	ENABLE	
19	RESET IN		19	RESET IN	
20	Data Terminal Ready Output		20	Data Terminal Ready Output	
21	RESET OUT		21	RESET OUT	
22	$\overline{A0}$	Polling Address	22	$\overline{A0}$	Polling Address
23	$\overline{A1}$		23	$\overline{A1}$	
24	$\overline{A2}$		24	$\overline{A2}$	
25	$\overline{A3}$		25	$\overline{A3}$	

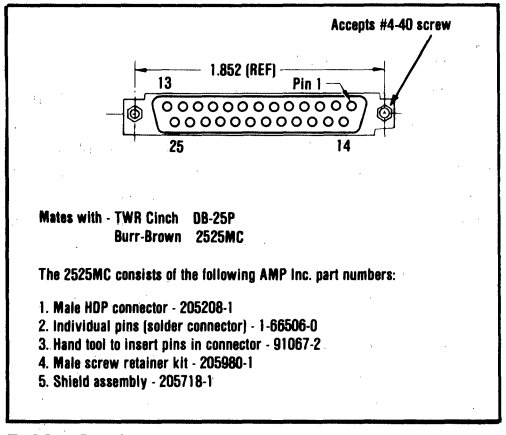

FIGURE 5. 25-Pin D Style Connector P1 Back Panel View.

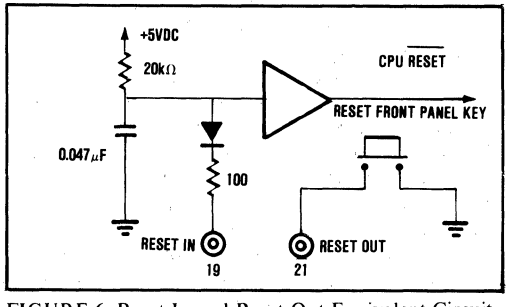

FIGURE 6. Reset In and Reset Out Equivalent Circuit.

TABLE VII. Baud Rate Selection.

Baud Rate	B2	B1	B0
300	1	1	1
600	1	1	0
1200	1	0	1
2400	1	0	0
4800	0	1	1
9600	0	1	0
19200	0	0	1
110	0	0	0

Logic 0 = jumper to signal ground (pin 7)
Logic 1 = open

TABLE VIII. Parity Bit Selection.

Parity Bit	P1	P0
SPACE	0	1
EVEN	0	0
ODD	1	0
MARK	1	1

(MARK = Logic 1)
Parity errors displayed as # Mark/Space not detected on input

Logic 0 = jumper to ENABLE (pin 18)
Logic 1 = open

Interface to the P2 I/O ports (shown in Figure 7) may be accomplished by reference to Figures 8 and 9 and Table IX.

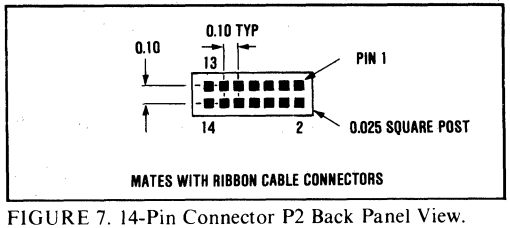

FIGURE 7. 14-Pin Connector P2 Back Panel View.

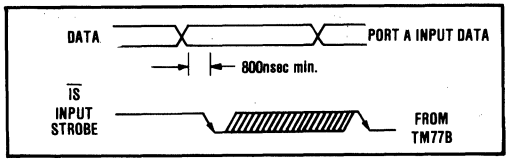

FIGURE 8. Output Timing.

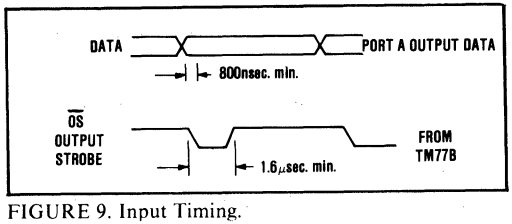

FIGURE 9. Input Timing.

TABLE IX. Listing of Connector P2 Pins - TM77B.

1	Signal Ground
2	A0
3	A1
4	A2
5	A3
6	A4 Port A: Input and Output
7	A5
8	A6
9	A7
10	$\overline{OS}$ Output Strobe
11	$\overline{IS}$ Input Strobe
12	Signal Ground
13	24VAC
14	24VAC Return

NOTES:
1. Logic positive true for port A.
2. Logic low 0.4V at 1.6mA.
   Logic high 3.5V at 100μA.
3. Mating connector - Burr-Brown model 2014MC.

RS-422

RS-422 electrical connections are in Figure 10. All terminals are connected in parallel. Note that resistors are recommended at the end of the transmission lines

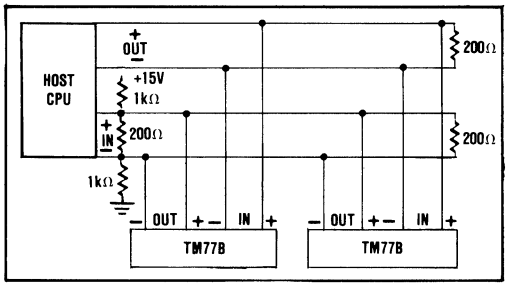

FIGURE 10. RS-422 Electrical Connections.

RS-232-C

Figures 11 and 12 show the RS-232-C equivalent input and output circuits.

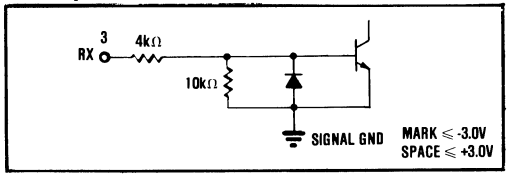

FIGURE 11. Input Equivalent Circuit.

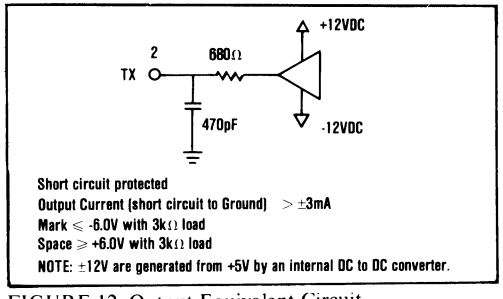

FIGURE 12. Output Equivalent Circuit.

SPECIFICATIONS

DISPLAY	
Number of Characters	16-alphanumeric
Internal Buffers	
Receiver	80 characters
Input	80 characters
Output	80 characters
Transmit	80 characters
Bar Code	5 x 50 characters
Type of Digit Display	16-segment
Character Height	3.6mm (0.14")
FUNCTION LIGHTS	
Host Controlled Lights	Two
Status Lights	Three message waiting/ output pending/ input display
Type of Light	Red, LED
KEYBOARD	
Type of Keyboard	Alphanumeric/Numeric
Number of Function Keys	Sixteen
User Programmable	Yes, up to 70 Characters each
MATERIALS	
Front Panel	Polycarbonate
Back Panel	Black Anodized Aluminum
Case	ABS Plastic
The front panel will be attacked by these chemicals:	Chlorinated or Fluorinated Hydrocarbons PVC Plasticizing Agents Amines
DO NOT USE FLUOROCARBONS (TMC, FREON, ETC.) TO CLEAN.	
TEMPERATURE RANGE	
Operating	0°C to +50°C
Storage	0°C to +60°C
POWER SUPPLY	
Nominal Voltage Range	15VAC to 28VAC 22VDC to 40VDC
Current	420mA
WEIGHT	580 grams (20 oz.)
COMMUNICATION INTERFACE	
Maximum Transmission Distance	
RS-422	1200 meters (4000 feet)
RS-232-C/V.24	15 meters (50 feet)
RS-422	
Differential Output Voltage (open circuit)	5V
Output Impedance (when active)	100Ω
Output Impedance (when inactive or (power off)	250kΩ

Differential Input Voltage	6V or less
Input Impedance	6000Ω (minimum)
RS-232-C	
Modem Control Signals	Yes
Output Voltage	
Logic 1	-10VDC
Logic 0	+10VDC
Input Voltage	
Logic 1	-3VDC to +15VDC
Logic 0	+ 3VDC to +15VDC

BAR CODE READER

Codes Available
- Code 39
- UPC/EAN
- Two of five
- Interleaved two of five
- Codabar

Other codes available upon request

MECHANICAL DIMENSIONS

Figure 13 shows the mechanical dimensions for the TM77B

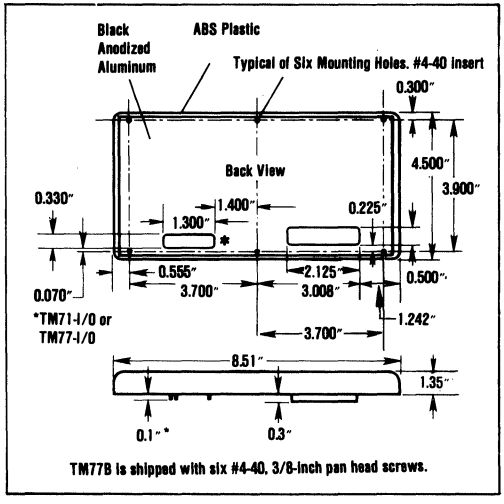

FIGURE 13. Mechanical Dimensions.

DIGITAL INPUT/OUTPUT PORT

TTL Compatible	Yes
Number of I/O Lines	Eight
Input strobe	One
Output drive	One TTL load

ENVIRONMENTAL SPECIFICATIONS

0°C to 50°C
95% relative humidity noncondensing
Contact factory for extended temperature range

ACCESSORIES

25-pin mating connector - 2525MC
14-pin mating connector for I/O ports - 2014MC

MICROCOMPUTER I/O SYSTEMS

This full line of μC compatible I/O boards is available off-the-shelf. Design features let you put your microcomputer-based system together fast, using these analog and digital I/O's that offer: simple software requirements; memory-mapped designs; up to 64 input channels per board; analog inputs and outputs on the same board; 8- or 12-bit resolutions; software programmable gains; relay outputs; isolated digital I/O. Plug compatible with Intel, DEC, National, Motorola, Rockwell, Zilog, Synertek, AMC and others.

SELECTION GUIDE

DIGITAL I/O

Compatible With	Microperipheral Model	Digital Input	Digital Output	Number Channels	Isolated	Features	Price ($) 1 - 9	Page
Motorola(1) and Rockwell(2)	MP701		•	16	•	Relay output	335.00	10-2
	MP702		•	32	•	Relay output	555.00	10-2
	MP710	•		24	•	Contact closure input	410.00	10-4
	MP710-NS	•		24	•	Voltage input	335.00	10-4
Intel(3) and National(4)	MP801		•	16	•	Relay output	335.00	10-6
	MP802		•	32	•	Relay output	555.00	10-6
	MP810	•		24	•	Contact closure input	410.00	10-8
	MP810-NS	•		24	•	Voltage input	335.00	10-8

ANALOG I/O

Compatible With	Microperipheral Model	Analog Input	Analog Output	Inputs High Level	Inputs Low Level	Analog Resolution	Number Channels Input	Number Channels Output	Features	Price ($) 1 - 9	Page
DEC(5)	MP1104		•			12		4	General purpose	550.00	10-10
	MP1216	•		•	•	12	32 SE		General purpose	550.00	10-12
	MP1216-PGA	•		•	•	12	32 SE		PGA(8)	695.00	10-12
Zilog(6)	MP2216	•		•	•	12	32 SE		General purpose	665.00	10-15
	MP2216-AO	•	•	•	•	12	32 SE	2	AI/AO on one board	825.00	10-15
Motorola(1) and Rockwell(2)	MP7104		•			12		4	General purpose	725.00	10-17
	MP7105-NS		•			12		4	General purpose	808.00	10-17
	MP7208	•		•	•	12	8 DIF		General purpose	725.00	10-17
	MP7216	•		•	•	12	16 SE		General purpose	725.00	10-17
	MP7218	•		•	•	12	16 SE		Low cost	450.00	10-21
	MP7408	•		•	•	8	16 SE		Low cost	375.00	10-23
	MP7408-AO	•	•	•	•	8	16 SE	2	AI/AO on one board	489.00	10-23
	MP7408-NS	•		•	•	8	16 SE		Low cost	289.00	10-23
	MP7408-NS-AO	•	•	•	•	8	16 SE	2	AI/AO on one board	409.00	10-23
	MP7432	•		•	•	8	64 SE		Low cost	489.00	10-23
	MP7432-AO	•	•	•	•	8	64 SE	2	AI/AO on one board	609.00	10-23
	MP7432-NS	•		•	•	8	64 SE		Low cost	409.00	10-23
	MP7432-NS-AO	•	•	•	•	8	64 SE	2	AI/AO on one board	532.00	10-23
	MP7504		•			8		4	Isolated outputs	695.00	10-25
	MP7608	•		•	•	12	8 DIF		Overvoltage protect.	595.00	10-27
	MP7608-I	•		•		12	8 DIF		4mA to 20mA inputs	595.00	10-27
Intel(3) and National(4)	MP8304		•			12		4	General purpose	695.00	10-29
	MP8305		•			12		4	General purpose	518.00	10-29
	MP8305-NS		•			12		4	General purpose	550.00	10-29
	MP8316-I		•			12		16	4mA to 20mA inputs	650.00	10-33
	MP8316-V		•			12		16	Voltage output	550.00	10-33
	MP8418	•		•	•	12	32 SE		General purpose	595.00	10-35
	MP8418-AO	•	•	•	•	12	32 SE	2	AI/AO on one board	795.00	10-35
	MP8418-PGA	•		•	•	12	32 SE		PGA(8)	650.00	10-35
	MP8418-PGA-AO	•	•	•	•	12	32 SE	2	PGA(8)	850.00	10-35
	MP8418-EXP	•		•	•	12	96 SE		Use with MP8418	495.00	10-39
	MP8608	•		•	•	8	8 DIF		Low cost	470.00	10-41
	MP8608-AO	•	•	•	•	8	8 DIF	2	AI/AO on one board	625.00	10-41
	MP8616	•		•	•	8	16 SE		Low cost	375.00	10-41
	MP8616-AO	•	•	•	•	8	16 SE	2	AI/AO on one board	470.00	10-41
	MP8632	•		•	•	8	64 SE		Low cost	589.00	10-41
	MP8632-AO	•	•	•	•	8	64 SE	2	AI/AO on one board	750.00	10-41

NOTES: 1) Micromodule and EXORciser®. 2) SYSTEM 65. 3) MULTIBUS™, SBC80, ICS80 and Intellec MDS, compatible. 4) BLC80. 5) LSI-11, LSI-11/2, LSI-11/23, PDP-11/03, and PDP-11/23. 6) Z-80 MCB and Z-80 MCZ. 7) Software programmable gain.

10

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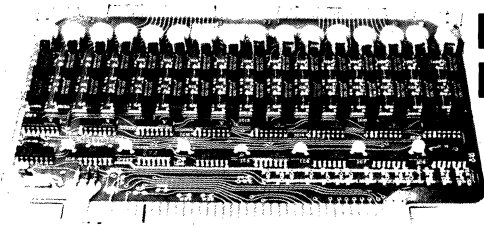
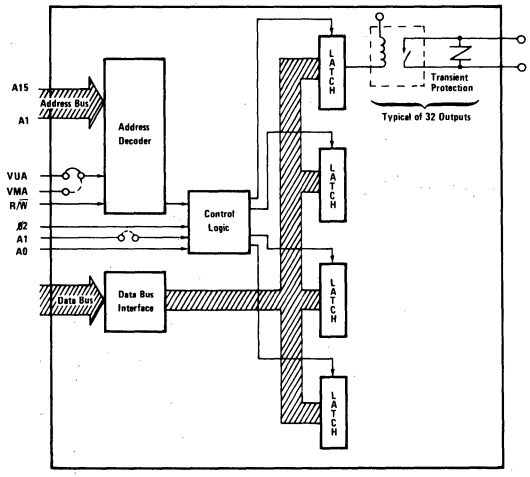


MP701
MP702

MICROCOMPUTER DIGITAL OUTPUT SYSTEMS



DESCRIPTION

The MP701 and MP702 are digital output microperipheral boards designed to be used with Motorola 6800 microcomputer systems. The microperipheral boards are electrically and mechanically compatible with Motorola's Micromodule and EXORciser development system. The MP701 has 16 digital output channels, and the MP702 has 32 digital output channels. Each digital output channel is implemented with a protected reed relay.

Relays are used to provide low "on-impedance", high output current and output isolation. Each output is isolated from the computer bus up to 600VDC and from channel to channel up to 300VDC. This means that the computer is protected from voltage transients and malfunctions. In addition, since each channel is isolated, the voltage switched by each line is not critical, and ground loops are avoided. The varistors protect each relay contact by suppressing high voltage transients such as those encountered in inductive circuits.

These boards appear as memory locations to the user. Data written on the data bus controls the status of each output. A "1" will close an output, a "0" will open an output. Any memory write command may be used. Each write command controls the status of eight channels. Address bits A0 and A1 on the MP702 and A0 on the MP701 select which set of eight outputs are controlled. The remainder of the address lines are used to select the board itself. Because the address block occupied by each board is user selectable, it can be placed anywhere in memory.

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SPECIFICATIONS

Typical at +25°C and rated supplies unless otherwise noted.

ELECTRICAL

NUMBER OF CHANNELS	
MP701	16
MP702	32
DIGITAL OUTPUT	
Watts DC (resistive load) max	10 watts
Amps (resistive load) max	.5 amps
Voltage (resistive load) max	28 Vrms
Life (resistive load) min	10^6 operations
Initial contact resistance max	.2 ohms
Actuate Time	250μsec
De-Actuate time	250μsec
Bounce time	150μsec
TRANSIENT PROTECTION	
Continuous power rating	250mW
Discharge capacity	30 watt-seconds
COMPUTER BUS	
All signals compatible with Motorola EXORciser and Micromodules system	
Logic Loading	1 LSTTL
Output Coding	0 Open Contact 1 Close Contact
POWER REQUIREMENTS	
Voltage	5VDC, ±5% volts
Supply Drain max, MP701	.4 amp
Supply Drain max, MP702	.7 amp
ISOLATION VOLTAGE	
Between microcomputer bus and outputs	600VDC
Between outputs	300VDC
OPERATING TEMPERATURE	0 to +70°C

MECHANICAL

Compatible with Micromodules and Exorciser card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

50 pin output edge connector on board.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). a Scotchflex connector is available from 3M: 3415-0001.

OPERATING INSTRUCTIONS

PROGRAMMING

Each digital output channel appears as one bit of memory to the microcomputer. The channels are selected in groups of eight by A0 on the MP701 and by A1-A0 on the MP702. Writing a 1 to an output channel closes the output contact; writing a 0 to an output channel opens the output contact. Once an output is defined, it will remain in that state until redefined by another write to that byte. For example, to open channels 0, 2, 6, and close channels 1, 3, 4, 5, 7 with an MP702 as shipped from the factory execute:

```
LDA #$BA
STA $91FC
```

where BA (1011 1010) is the data written to the board and 91FC is the address of channels 0-7. Refer to Table I for a description of which data and address lines control which output channels.

Data Bus	ADDRESS LINES (A1, A0) 00	01	10	11
$\overline{D7}$	7	15	23	31
$\overline{D6}$	6	14	22	30
$\overline{D5}$	5	13	21	29
$\overline{D4}$	4	12	20	28
$\overline{D3}$	3	11	19	27
$\overline{D2}$	2	10	18	26
$\overline{D1}$	1	9	17	25
$\overline{D0}$	0	8	16	24

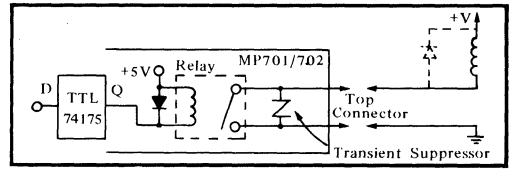
Channel Number

TABLE I. Data - Address - Channel Relationship.
0 = open, 1 = close.

The MP701 and MP702 are passive during a read to their memory locations. Therefore, other memory or I/O devices may be placed at the same address without interfering with the microperipheral's activities.

DIGITAL OUTPUT CHANNEL

Each output is capable of switching an inductive load. Transient suppressors are used across each output switch to protect the output relay from damage due to surges when the contact is opened. A typical output circuit and the load circuit that it might drive are shown in the figure below.



Each relay is rated to .5 amps and 100 volts maximum. The transient suppressor reduces the maximum voltage to 28Vrms.

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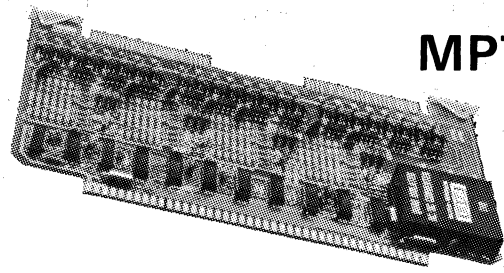
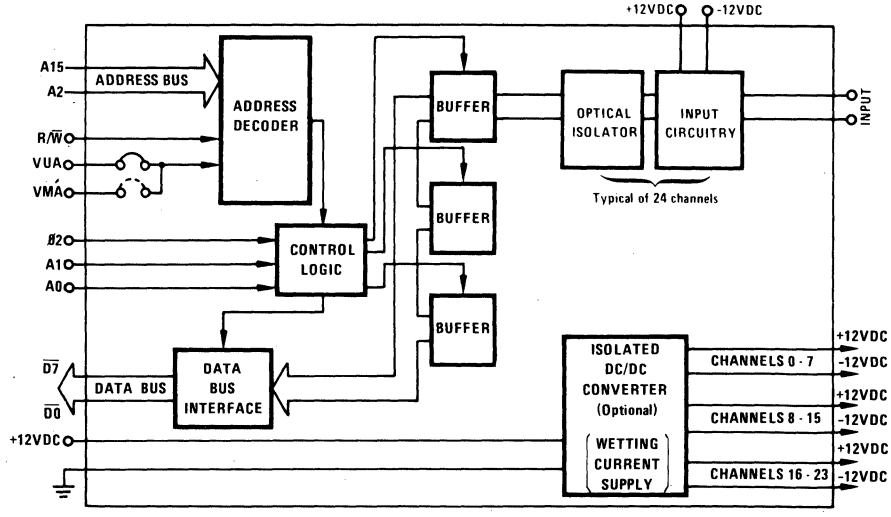


MP710

MICROCOMPUTER DIGITAL INPUT SYSTEM

A 24-CHANNEL ISOLATED DIGITAL INPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE/EXORciser® AND ROCKWELL SYSTEM 65



FEATURES

- ISOLATED FROM COMPUTER BUS AND CHANNEL TO CHANNEL
- CONTACT CLOSURE OR VOLTAGE INPUTS
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Easy to program
  - Operates from computer power supply
- 70°C BURN-IN

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DESCRIPTION

This microperipheral board provides 24 digital input channels that interface electrically and mechanically with Motorola Micromodule® and EXORciser® microcomputers. It is contained on a single printed circuit board that operates from the computer's +5VDC power supply. Digital inputs enter through a card edge connector located opposite the bus connector.

The MP710 operates with dry relay contacts - MP710-NS operates with voltage inputs (wet relay contacts). The MP710 may be modified by jumper selection to operate with voltage or contact closure inputs, or a mixture of both. Inputs are arranged in groups of eight. Each group is isolated from other groups and from the computer bus up to 600 VDC. Isolation between inputs is 300 VDC (MP710-NS). Isolation protects the computer from voltage transients and malfunctions. In addition, since each input is isolated, the voltage switched by each line is not critical and ground loops are avoided.

MP710's are programmed as memory locations. Each input is one memory bit and any read command may be used. When the board is read, logic 0 represents an open contact (low voltage); logic 1, a closed contact (high voltage). Each read command inputs the status of eight channels. Address bits A0 and A1 select the set of inputs to be read. The remainder of the address lines are used to select the board itself. The address block occupied by each board is selectable and can be located anywhere in memory.

® Motorola

INSTALLATION

These units are shipped from the factory ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and wiring the input connector.

MECHANICAL

Compatible with Micromodule and EXORciser card spacing.

Minimum card spacing: 12.7mm (0.5″).

Microcomputer bus connector required: 86 pin PC edge connector with 0.156″ contact centers (SAE-43D/1-2).

Two 50 pin output edge connectors on board.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

SPECIFICATIONS

Typical at +25°C and rated supplies unless otherwise noted.

ELECTRICAL

INPUT CHARACTERISTICS	
Number of Channels	24
Input Impedance	15kΩ
Input Delay Times	
Open to closed	25μs, max
Closed to open	100μs, max
VOLTAGE SENSE	
MP710-NS	
Minimum voltage to detect a logic 1	17V
Maximum voltage to detect a logic 0	4V
CONTACT CLOSURE SENSE	
R_{closed}	
MP710 (on board ±12V supply)	6kΩ, max
MP710-NS	
at 24V across contacts	6kΩ, max
at 48V across contacts	30kΩ, max
at 60V across contacts	58kΩ, max
R_{open}	
MP710 (on board ±12V supply)	80kΩ, min
MP710-NS	
at 24V across contacts	80kΩ, min
at 48V across contacts	175kΩ, min
at 60V across contacts	235kΩ, min
Maximum voltage (V_S) across input without damage	
MP710	120VAC, rms, max 60VDC, max
MP710-NS	168VAC, rms, max 84VDC, max
ISOLATION VOLTAGE	
Between microcomputer bus and inputs	600VDC
Between inputs (MP710-NS only)	300VDC
Between groups of 8 inputs	600VDC
POWER REQUIREMENTS	
MP710	+5VDC ±5% at 400mA +12VDC ±5% at 100mA
MP710-NS	+5VDC ±5% at 400mA
COMPUTER BUS	
All signals compatible with Motorola Micromodule and EXORciser systems	
Logic loading	1 LSTTL Load
Input coding	Logic 0: open contact Logic 1: close contact
TEMPERATURE RANGE	
Operating	0 to +70°C

TABLE I. Electrical Specifications

DEFINITION OF SPECIFICATIONS

INPUT DELAY TIME

OPEN TO CLOSED - The delay required to detect an input contact closure switching from open to closed.

CLOSED TO OPEN - The delay required to detect an input contact closure switching from closed to open.

CONTACT CLOSURE IMPEDANCES

R_{CLOSED} - The impedance of an input contact closure when closed. R_{CLOSED} specifications are the maximum impedance allowed to reliably detect a closure. See Figure 1.

R_{OPEN} - The impedance of an input contact closure when open. R_{OPEN} specification is the lowest impedance allowed to reliably detect an open contact. See Figure 1.

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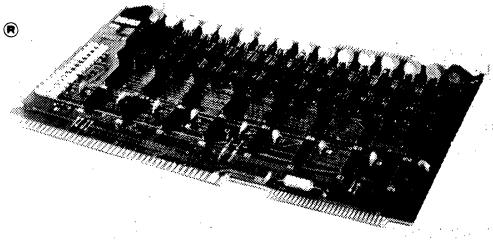
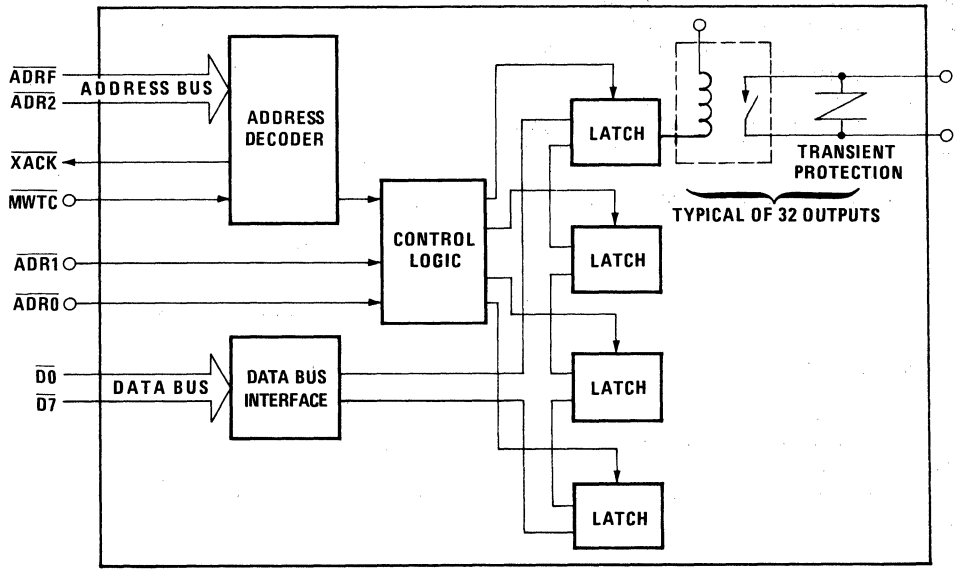


MP801
MP802

MICROCOMPUTER DIGITAL OUTPUT SYSTEMS

A 16- OR 32-CHANNEL RELAY OUTPUT SYSTEM COMPATIBLE WITH INTEL SBC80 AND INTELLEC MDS MICROCOMPUTERS



FEATURES

- ISOLATED FROM COMPUTER BUS AND CHANNEL TO CHANNEL
- TRANSIENT PROTECTION
- EASY TO PROGRAM AND USE
- MEMORY-MAPPED
- BURNED-IN

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DESCRIPTION

The MP801 and MP802 are digital output (contact closure) microperipheral boards that are electrically and mechanically compatible with Intel's SBC80 and Intellec MDS microcomputer systems. The MP801 offers 16 digital output channels and the MP802, 32 digital output channels.

Each channel is implemented by a protected reed relay and can handle up to 10 watts. Relays provide low "on-impedance" and high output current and isolate output channels from the computer bus and from channel to channel. Isolation insures that ground loop problems are avoided. The computer is protected from component failures caused by voltage transients and malfunctions occurring in the outside world.

MP801 and MP802 appear as memory locations and data written on the data bus controls the status of each output. A logic 1 will close an output. A logic 0 will open an output. Any memory write instruction may be used.

SPECIFICATIONS

Typical at +25°C and rated supplies unless otherwise noted

ELECTRICAL

NUMBER OF CHANNELS	
MP801	16
MP802	32
DIGITAL OUTPUT	
Watts DC (resistive load) max	10 watts
Amps (resistive load) max	0.5 amps
Voltage (resistive load) max	28 Vrms
Life (resistive load) min	10^6 operations
Initial contact resistance max	0.3 ohms
Actuate Time	1msec
De-Actuate time	250μsec
Bounce time	150μsec
TRANSIENT PROTECTION	
Continuous power rating	250mW
Discharge capacity	30 watt-seconds
Leakage current through transient suppressor at 28V	5mA
COMPUTER BUS	
All signals compatible with Intel SBC 80 and MDS Systems	
Logic Loading	1 LSTTL
Output Coding	0 Open Contact 1 Close Contact
POWER REQUIREMENTS	
Voltage	5VDC, ±5%
Supply Drain max, MP801	0.3 amp
Supply Drain max, MP802	0.5 amp
ISOLATION VOLTAGE	
Between microcomputer bus and outputs	600VDC
Between outputs	300VDC
OPERATING TEMPERATURE	0 to +70°C

TABLE I. Electrical Specifications

MECHANICAL

Compatible with SBC 80 and Intellec MDS card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Two 50 pin output edge connectors on board. One is used for MP801, both are used for MP802.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

OPERATING INSTRUCTIONS

PROGRAMMING

Each digital output channel appears as one bit of memory to the microcomputer. The channels are selected in groups of eight by $\overline{ADR0}$ on the MP801 and by $\overline{ADR1}$-$\overline{ADR0}$ on the MP802. The remainder of the address lines are used to select the board itself. Because the address block occupied by each board is user selectable, it can be placed anywhere in memory. Writing a logic 1 to an output channel closes the output contact; writing a logic 0 to an output channel opens the output contact. Once an output is defined, it will remain in that state until redefined by another write to that byte. For example, to open channels 0, 2, 6, and close channels 1, 3, 4, 5, 7 with an MP802 as shipped from the factory execute:

```
MVI   A, BAH
STA   F700H
```

where BA (1011 1010) is the data written to the board and F700 is the address of channels 0-7. Refer to Table II for a description of which data and address lines control which output channels.

Data Bus	ADDRESS LINES (A1, A0)			
	00	01	10	11
$\overline{D7}$	7	15	23	31
$\overline{D6}$	6	14	22	30
$\overline{D5}$	5	13	21	29
$\overline{D4}$	4	12	20	28
$\overline{D3}$	3	11	19	27
$\overline{D2}$	2	10	18	26
$\overline{D1}$	1	9	17	25
$\overline{D0}$	0	8	16	24

TABLE II. Data - Address - Channel Relationship. Logic 0 = open, Logic 1 = close.

The MP801 and MP802 are passive during a read to their memory locations. Therefore, other memory or I/O devices may be placed at the same address without interfering with the microperipheral's activities.

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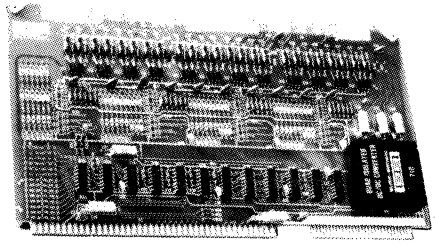
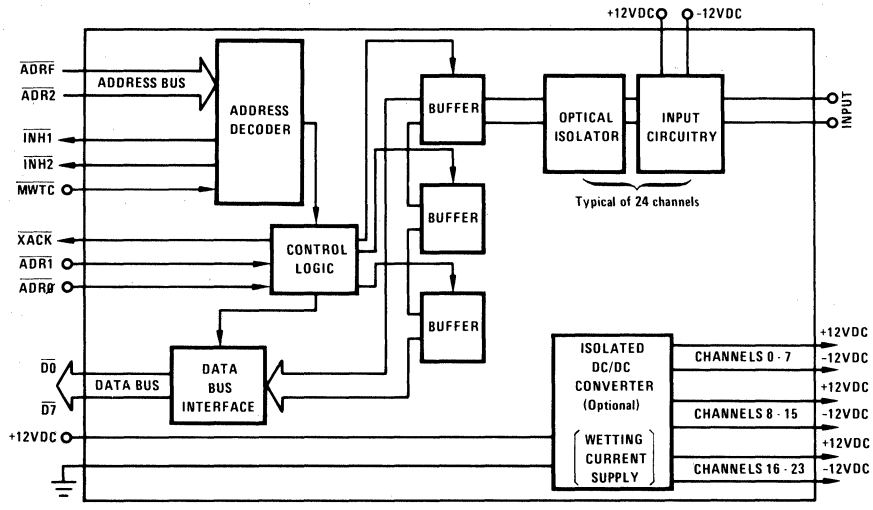


MP810

MICROCOMPUTER DIGITAL INPUT SYSTEM

A 24-CHANNEL ISOLATED DIGITAL INPUT SYSTEM COMPATIBLE WITH INTEL SBC80, NATIONAL BLC80 AND INTELLEC MDS



FEATURES

- ISOLATED FROM COMPUTER BUS AND CHANNEL TO CHANNEL
- CONTACT CLOSURE OR VOLTAGE INPUTS
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Easy to program
  - Operates from computer power supply
- 70°C burn-in

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DESCRIPTION

The MP810 and MP810-NS are 24 channel, optically isolated, digital input microperipheral boards that are electrically and mechanically compatible with Intel SBC80, National BLC80 and Intellec MDS microcomputer systems. Each printed circuit board operates from the computer's power supplies. Digital inputs enter through card edge connectors located opposite the bus connector.

The MP810 operates with dry relay contacts. The MP810-NS operates with voltage inputs (wet relay contacts). The MP810 may be modified by jumper selection to operate with voltage or contact closure inputs, or a mixture of both. Inputs are arranged in groups of eight. Each group is isolated from other groups and from the computer bus up to 600VDC. Isolation between inputs is 300VDC (MP810-NS). Isolation protects the computer from voltage transients and malfunctions. In addition, since each input is isolated, the voltage switched by each line is not critical and ground loops are avoided.

MP810's are programmed as memory locations. Each input is one memory bit, therefore any memory read instruction may be executed. When the board is read, logic 0 represents an open contact (low voltage); logic 1, a closed contact (high voltage). Each read command inputs the status of eight channels. Address bits ADR0 and ADR1 select that set of inputs to be read. The remainder of the address lines are used to select the board itself. The address block occupied by each board is selectable and can be located anywhere in memory.

INSTALLATION

These units are shipped from the factory ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and wiring the input connector.

MECHANICAL

Compatible with SBC80, BLC80 and Intellec MDS spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Two 50 pin input connectors on each board.

A mating connector is available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab). A Scotchflex connector is available from 3M: 3415-0001.

SPECIFICATIONS

Typical at +25°C and rated supplies unless otherwise noted.

ELECTRICAL

INPUT CHARACTERISTICS	
Number of Channels	24
Input Impedance	15kΩ
Input Delay Times	
Open to closed	25μs, max
Closed to open	100μs, max
VOLTAGE SENSE	
MP810-NS	
Minimum voltage to detect a logic 1	17V
Maximum voltage to detect a logic 0	4V
CONTACT CLOSURE SENSE	
R_{closed}	
MP810 (on board ±12V supply)	6kΩ, max
MP810-NS	
at 24V across contacts	6kΩ, max
at 48V across contacts	30kΩ, max
at 60V across contacts	58kΩ, max
R_{open}	
MP810 (on board ±12V supply)	80kΩ, min
MP810-NS	
at 24V across contacts	80kΩ, min
at 48V across contacts	175kΩ, min
at 60V across contacts	235kΩ, min
Maximum voltage (V_S) across input without damage	
MP810	120VAC, rms, max 60VDC, max
MP810-NS	168VAC, rms, max 84VDC, max
ISOLATION VOLTAGE	
Between microcomputer bus and inputs	600VDC
Between inputs (MP810-NS only)	300VDC
Between groups of 8 inputs (MP810, MP810-NS)	600VDC
POWER REQUIREMENTS	
MP810	+5VDC ±5% at 400mA +12VDC ±5% at 100mA
MP810-NS	+5VDC ±5% at 400mA
COMPUTER BUS	
All signals compatible with Micrcomputer bus	
Logic loading	1 LSTTL Load
Input coding	Logic 0: open contact Logic 1: close contact
TEMPERATURE RANGE	
Operating	0 to +70°C

TABLE I. Electrical Specifications

DEFINITION OF SPECIFICATIONS

INPUT DELAY TIME

OPEN TO CLOSED - The delay required to detect an input contact closure switching from open to closed.

CLOSED TO OPEN - The delay required to detect an input contact closure switching from closed to open.

CONTACT CLOSURE IMPEDANCES

R_{CLOSED} - The impedance of an input contact when closed. R_{CLOSED} specification is the maximum impedance allowed to reliably detect a closure See Figure 1.

R_{OPEN} - The impedance of an input contact closure when open. R_{OPEN} specification is the lowest impedance allowed to reliably detect an open contact.

MP810

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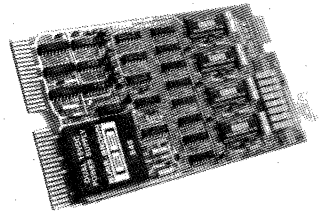


MP1104

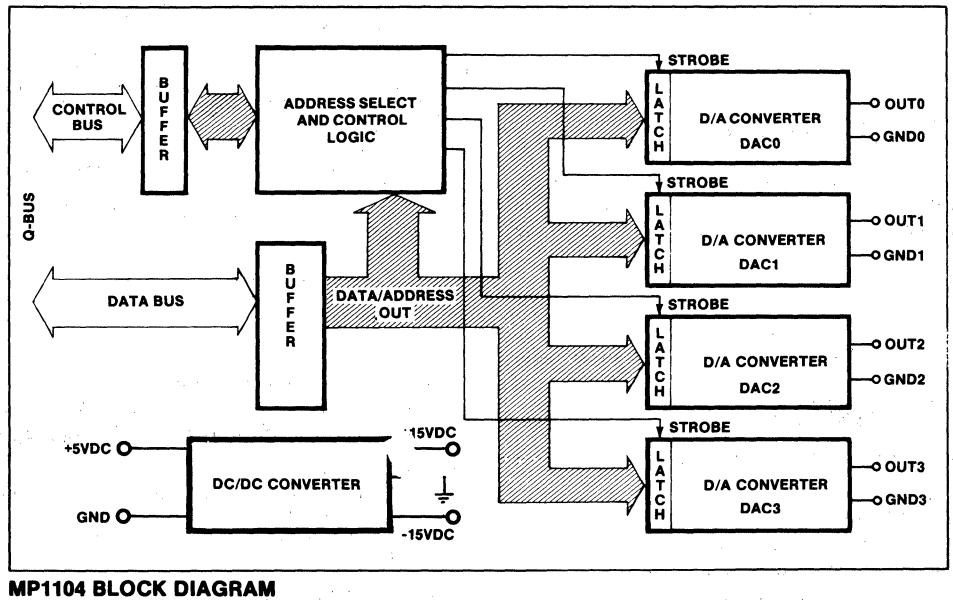
MICROCOMPUTER ANALOG OUTPUT SYSTEM

A 4-CHANNEL ANALOG OUTPUT SYSTEM COMPATIBLE WITH DIGITAL EQUIPMENT CORP. LSI-11, LSI-11/2, LSI-11/23, PDP-11/03, AND PDP-11/23 MICROCOMPUTERS

DESCRIPTION

The MP1104 analog output peripheral is electrically and mechanically compatible with and interfaces directly to DEC's Q bus.

The MP1104 consists of four 12-bit D/A converters with address decoding and control logic. It also includes a DC/DC converter for operation from the computer's 5VDC supply. The MP1104 is burned-in before shipment.



MP1104 BLOCK DIAGRAM

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PDS-417

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG OUTPUT	MP1104
OUTPUT CHARACTERISTICS	
Number of Channels	4
Output Voltage Ranges (Jumper Selectable)(1)	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA
Output Impedance	0.01Ω
Short Circuit Protection	Yes
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Output Settling Time, max(2)	10μsec
ACCURACY	
Output Accuracy, max(3)	±0.025% FSR(4)
Temperature Coefficient of Accuracy Drift(5)	±30ppm of FSR/°C
POWER REQUIREMENTS	
MP1104	+5V ±5% at 1.25A
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Relative Humidity	95% of noncondensing

NOTES:
1. Factory set for ±10V range.
2. Settling to ±0.01% of FSR for a full scale change.
3. Includes linearity errors with gain and offset errors adjusted to zero.
4. FSR means Full Scale Range.
5. Includes offset drift, gain drift and linearity drift.

MECHANICAL

Compatible with DEC LSI-11, LSI-11/2, LSI-11/23, PDP-11/03, and PDP-11/23 card spacing.

Minimum card spacing: 12.7mm (0.5").

Analog Output Connector: one 20-pin PC edge connector on top edge of board.

Analog Output Mating Connector:

Mating connector available from Burr-Brown: 2220MC (Viking #3VH10/1JN5, solder tab)

A flat cable connector is available from Berg: 65764-001

OPERATING INSTRUCTIONS

INSTALLATION

MP1104 is shipped from the factory calibrated and ready to use. Installation consists of plugging the card into any empty slot in the computer and wiring the analog connector.

PROGRAMMING

The MP1104 is programmed as memory locations and any memory write instruction can be used. The D/A converter input occupies the 12 least significant bits of a word. The address block occupied by the MP1104 is user-selectable and can be placed anywhere in the upper 4k of memory.

MP1104's are jumpered at the factory with a base address of 170440 (channel 0). Channel one is at location 170442, channel two is at location 170444, and channel three is at location 170446 (see Table I).

TABLE I. D/A Converter Data Assignments.

WRITE DATA															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

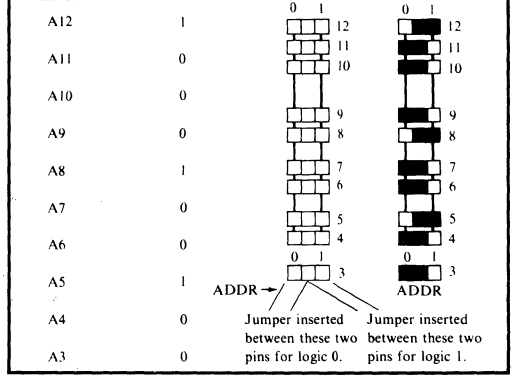
MEMORY MAP	
Channel 0	Base Address
Channel 1	Base Address +2
Channel 2	Base Address +4
Channel 3	Base Address +6

ADDRESS MODIFICATION

The base address of a board can be set to any 4-word boundry by properly jumpering (with push-on sockets) its address selector. The base address set at the factory is 170440. To change the sense of a bit simply remove the present jumper and insert the jumper for that bit (see Tables II and III).

TABLE II. Base Address Jumpers.

ADDRESS LINES	FACTORY SET VALUE	JUMPER MATRIX LAYOUT	FACTORY SET VALUES
A12	1	0 1 / 12	0 1 / 12
A11	0	11	11
A10	0	10	10
A9	0	9	9
A8	1	8	8
A7	0	7	7
A6	0	6	6
A5	1	5	5
A4	0	4	4
A3	0	0 1 / 3	0 1 / 3



ANALOG OUTPUT RANGE SELECTION

Each D/A converter is wire wrap jumpered at the factory for ±10V operation with two's complement coding. It is possible, however, to alter jumpers on the board for other output voltages and coding. When making a change, just remove those jumpers indicated for the present range and replace them with the jumpers required for the desired range.

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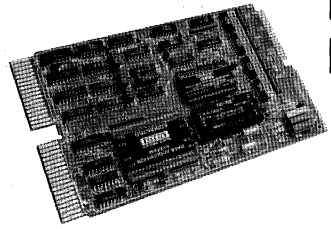


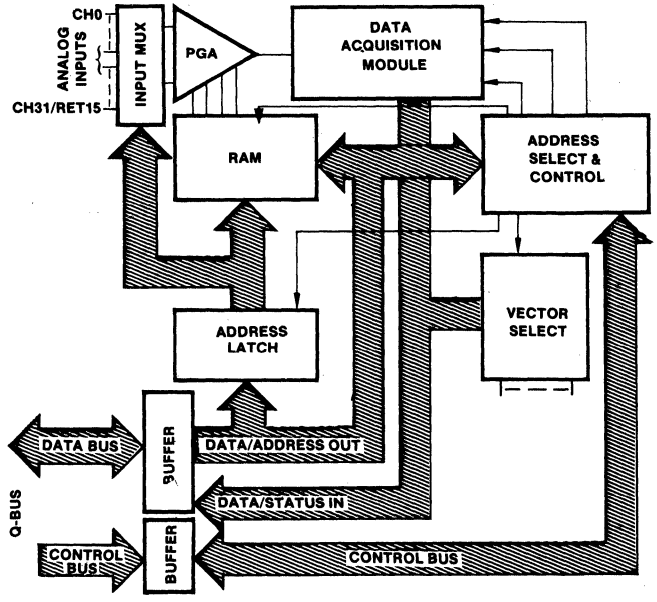
MP1216
MP1216-PGA

MICROCOMPUTER ANALOG INPUT SYSTEMS

A 32-CHANNEL ANALOG INPUT SYSTEM COMPATIBLE WITH DIGITAL EQUIPMENT CORPORATION LSI-11, LSI-11/2, LSI-11/23, PDP-11/03 AND PDP-11/23 MICROCOMPUTERS

FEATURES:

- HIGH AND LOW LEVEL INPUTS
- SOFTWARE PROGRAMMABLE GAIN (1 to 1024) AMPLIFIER OPTION
- EASILY PROGRAMMED
- BURN-IN



DESCRIPTION

The MP1216 analog input peripherals are electrically and mechanically compatible with and interface directly to DEC's LSI-11/2 family. The boards use one dual-wide card slot.

The MP1216 includes: over-voltage protection to 26VDC; an analog multiplexer; resistor programmed instrumentation amplifier (MP1216), or a software programmable amplifier with gains of 1 to 1024 (MP1216-PGA); sample/hold amplifier and; a 12-bit A/D converter.

These units are 16-channel differential (user strapable as 32-channel single-ended) analog input systems.

Gains of 1 to 1024 are software selectable for the programmable amplifier version (MP1216-PGA), and the gain for each channel is stored in an on-board RAM. The proper gain for each channel is then selected automatically by the MP1216-PGA.

The MP1216-PGA is particularly recommended for low-level inputs.

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SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG INPUT SECTION	MP1216/MP1216-PGA
INPUT CHARACTERISTICS	
Number of Channels	32 single-ended or 16 differential
ADC Gain Ranges (jumper selectable)[1]	±10V, 0-10V
Amplifier Gain Ranges	
Resistor Programmable[2] (MP1216)	1 to 1000
Software Programmable (MP1216-PGA)	1 to 1024
Maximum Input Voltage without Damage[3]	±26V
Input Impedance	100MΩ, 10pF OFF Channel 100MΩ, 100pF ON Channel
Bias Current	
Resistor Programmable	±20nA
Software Programmable	±15nA
Amplifier Input Offset Voltage	
Resistor Programmable	±400μV
Software Programmable	±40μV
Amplifier Input Offset Voltage Drift	
Resistor Programmable	±2μV/°C
Software Programmable	±0.5μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Conversion Time, max G = 1	
Resistor Programmable[4]	40μsec
Software Programmable	375μsec
Conversion Time, max G = 1024	
Resistor Programmable	100μsec
Software Programmable	375μsec
ACCURACY	
System Accuracy at +25°C, max[5] G = 1	±0.025% FSR[6]
System Accuracy at +25°C, max G = 1024	
Resistor Programmable	±0.1% FSR
Software Programmable	±0.05% FSR
System Output Noise G = 1, rms	
Resistor Programmable	1mV
Software Programmable	1mV
System Output Noise G = 1024, rms	
Resistor Programmable	15mV
Software Programmable	2mV
Linearity	±1/2LSB
Differential Linearity	±1/2LSB
Quantizing Error	±1/2LSB
Gain Error	Adjustable to zero[7]
Offset Error	Adjustable to zero
Monotonicity[8]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE (Bipolar)[9]	
System Accuracy Drift, max G = 1	±45ppm of FSR/°C
System Accuracy Drift, max G = 1024	
Resistor Programmable	±200ppm of FSR/°C
Software Programmable	±100ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	125nsec
Aperture Time Uncertainty	±5nsec
Differential Amplifier CMRR G = 1	74dB (DC to 1kHz)
Channel Crosstalk	80dB down at 1kHz, for OFF Channel to ON Channel
POWER REQUIREMENTS	
MP1216/MP1216-PGA	+5V ±5% at 1.0A
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Relative Humidity	95% noncondensing

NOTES:
1. Factory set for ±10V range.
2. Factory set for Gain = 1.
3. With power off (±36 volts with power on).
4. With delay inhibited, 22μsec.
5. Includes linearity errors with gain and offset errors adjusted to zero.
6. FSR means Full Scale Range.
7. When any one gain range is adjusted to zero gain error, the gain error for any other range is less than ±0.02% when using the software programmable amplifier.
8. No missing codes guaranteed.
9. Includes offset drift, gain drift, and linearity drift.

MECHANICAL

Compatible with LSI-11, LSI-11/2, LSI-11/23, PDP-11/03 and PDP-11/23 card spacing.

Minimum card spacing: 12.7mm (0.5").

Analog Input Connector: One 40-pin analog edge connector on board for analog inputs.

Analog Input Mating Connector:
Mating connector available from Burr-Brown: 2240MC (Viking #3VH20/1JN5 solder tab); a flat cable connector is available from Berg: 65764-007.

OPERATING INSTRUCTIONS

INSTALLATION

MP1216 is shipped from the factory calibrated and ready to use. Installation consists of plugging the card into any empty slot in the computer and wiring the analog connector. See Figure 1 for the block diagram.

PROGRAMMING

This peripheral is programmed as memory locations; any memory reference instruction can be used. Two 16-bit memory locations are used. One for the Read/Write data register; the other for the Control Status register (see Figure 2). The addresses occupied by each MP1216 are user selectable and can be placed anywhere in the upper 4K of memory.

On MP1216-PGA's (with software programmable gain amplifiers) an on-board random access memory (RAM) is used to store the gain for each channel.

When the Gain Control bit (D8) of the Write Data Register is a logic 1, the data contained in bits D9-D12 of the same register are written to the on-board RAM to control the gain for the channel also written in the same word (bits D0-D4). On subsequent operations if the Gain Control bit is a logic 0, the programmable gain amplifier will use the gain already stored in on-board RAM for that channel.

These boards are factory set with Data Register at location 170402 and the Status/Control Register at location 170400.

A conversion is started by writing the channel number to bits D0-D4 of the data register. This write operation selects the proper analog multiplexer channel and starts a delay one-shot which allows time for the multiplexer, instrument amplifier and sample/hold amplifier to settle to the new channel's value. At the end of the delay time, the sample/hold amplifier is switched to the hold mode and the A/D converter starts its conversion.

When the conversion is complete, the board can be operated in one of two modes:

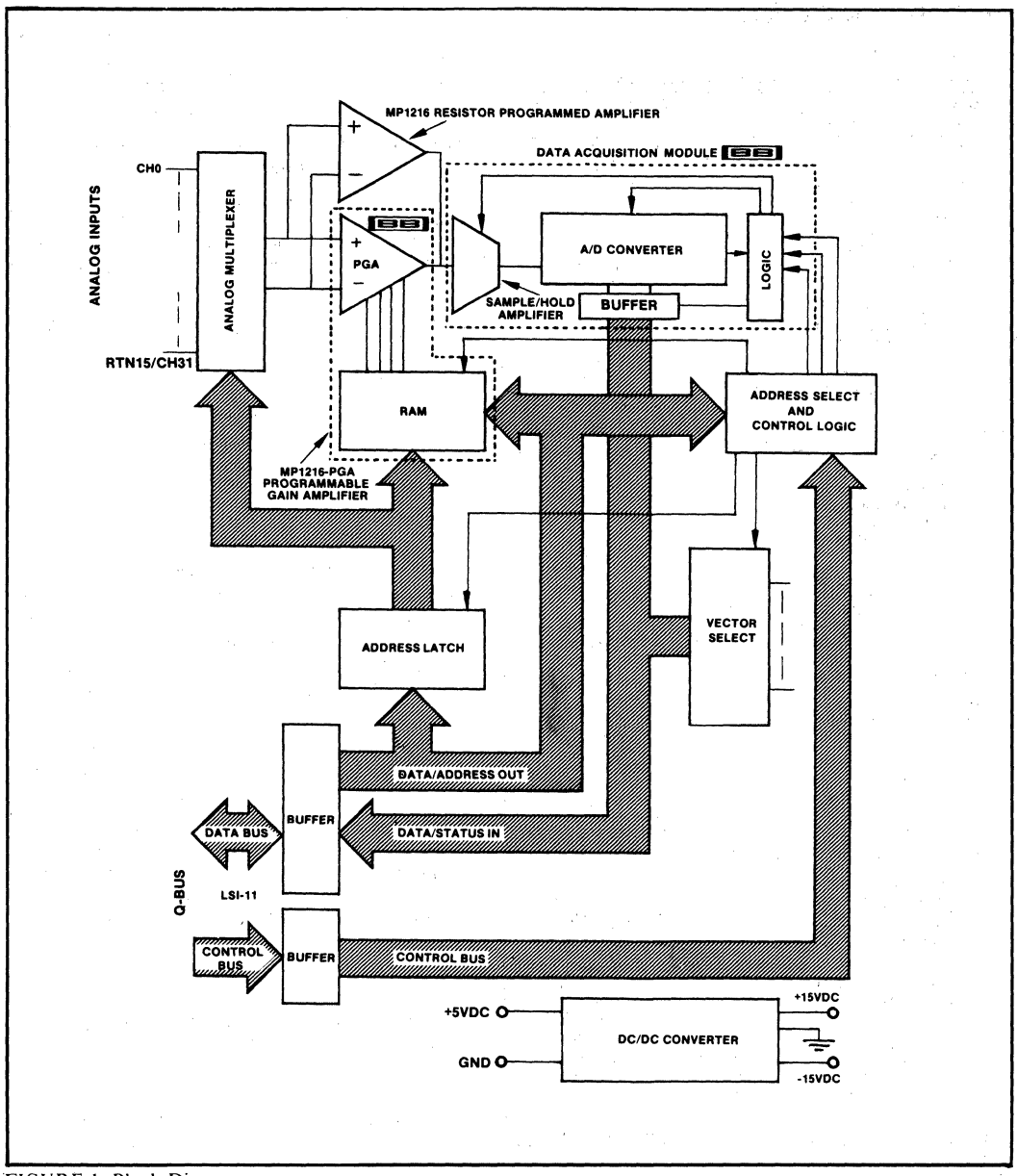

FIGURE 1. Block Diagram.

Interrupt Mode

In the Interrupt Mode, when the conversion is complete, the MP1216 asserts the bus interrupt request line (BIRO). When the LSI-11 responds with a bus interrupt acknowledgement (BIAKI), the MP1216 asserts the bus reply line (BRPY) and gates an interrupt "vector" onto the bus. The vector address is selected by jumpers on the board. The Interrupt Mode is enabled by writing a logic 1 to bit D6 of the Control Register.

Polling Mode

In the Polling Mode, the CPU must periodically scan bit D7 of the STATUS Register to determine if the conversion is complete. A logic 1 indicates that conversion is complete. A read of the Data Register will then produce the data word. The board is in the Polling Mode if the Interrupt Mode is disabled by writing a logic 0 to bit D6 of the Control Register.

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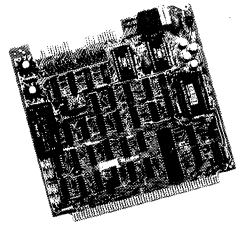


MP2216

MICROPERIPHERAL ANALOG INPUT/OUTPUT SYSTEM

A 12-BIT 32 CHANNEL ANALOG INPUT/ 2 CHANNEL ANALOG OUTPUT SYSTEM COMPATIBLE WITH ZILOG MICROCOMPUTERS

FEATURES

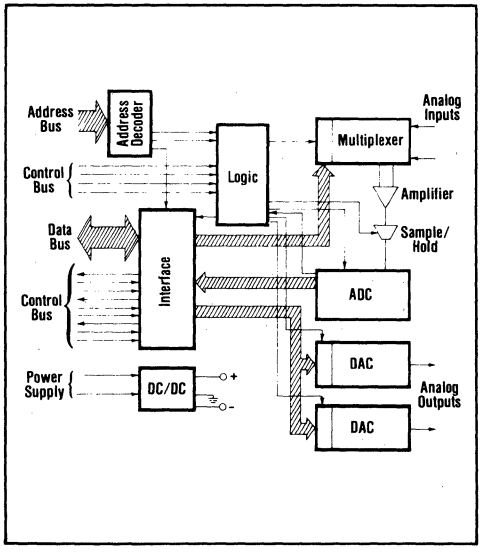
- ANALOG I/O ON THE SAME BOARD
- OPERATES FROM COMPUTER POWER SUPPLY
- HIGH LEVEL OR LOW LEVEL INPUTS
- BURNED-IN

DESCRIPTION

Completely compatible with Zilog's Z-80 MCB® and Z-80 MCS series of microcomputers, MP2216 provides a single board 12-bit resolution analog input/output system. The input section accepts 16 differential or 32 single-ended channels. Inputs ranging from millivolts to volts can be digitized because of MP2216's variable gain instrumentation amplifier.

Two optional channels of analog voltage are provided in the output section of the MP2216. The input data for each digital-to-analog converter is double buffered to minimize output glitches during a data update. Several output ranges and bipolar or unipolar operation are selected by on-board programming.

The MP2216 is mechanically, electrically and logically compatible with the Zilog systems. Power is derived from the +5V logic supply. Logic levels and drive capacity are matched to the system bus. Interfacing is accomplished primarily through a Z-80 PIO contained within the system.



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PDS-392

THEORY OF OPERATION

The MP2216 interfaces with the Z-80 I/O bus occupying 10 locations for the complete input/output system. The first four locations are required for the PIO. The next two locations transfer input channel address and board status. The remaining locations are used to pass data to the two digital-to-analog converters.

Data can be acquired from the analog inputs in either the POLLING or INTERRUPT mode:

POLLING MODE - A conversion is initiated by writing the analog channel address to the address register. The program must then periodically test the conversion bit in the status register to determine when the conversion is completed. During initialization of the MP2216's PIO, the interrupt enable must be reset (both ports) to prevent generation of interrupts.

The following program may be used to input a channel of data to the BC register pair:

```
LDA, XX          Load accumulator with channel address (XX) of data
                 to be converted.
OUT (YY), A      Outputs channel address to MP2216's address
                 register (location YY). This starts conversion.
  :
  :              Other software if desired for conversion time.
STATUS IN A, (ZZ)  Input status bit from location ZZ.
BIT 0, A         Test status bit.
JP Z, STATUS     Jump to STATUS until conversion is complete.
IN A, (WW)       Transfers the least significant byte to the
                 accumulator. WW is PIO port A DATA register.
LD C, A
IN A, (WW + 1)   Transfers the most significant byte to the
                 accumulator. WW + 1 is PIO port B DATA register.
LD B, A
```

INTERRUPT MODE - After setting the board's PIO interrupt enable and vector address, conversion is initiated by writing to the address register. Program execution may then continue until the conversion is complete. At that point the system PIO generates an interrupt vector causing the CPU to begin execution of the MP2216's interrupt service routine. Software for this mode is the same as that of the polling mode, but without the status loop.

Outputting of data from the MP2216's two digital-to-analog converters is straightforward. Each converter occupies two addresses on the I/O bus. The least significant 8 bits of the 12-bit data word are written to the first of these data words while the four most signficant bits are written to the second data word.

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG INPUT SECTION	
INPUT CHARACTERISTICS	
Number of Channels	32 single-ended/16 differential
ADC Gain Ranges (Jumper Selectable)	0 - 5V, 0 - 10V, ±2.5V, ±5V, ±10V
Amplifier Gain Ranges (resistor programmable)	1 to 1000
Maximum Input Voltage Without Damage	±26 volts
Input Impedance	100MΩ, 10pF OFF Channel
	100MΩ, 100pF ON Channel
Bias Current	20nA
Differential Bias Current	10nA
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Throughput Time (max) G = 1	45μsec/channel
Throughput time (max) G = 1000	100μsec/channel
ACCURACY	
System Accuracy G = 1 (max)[1]	±0.025% FSR[2]
System Accuracy G = 1000	±0.1% FSR
Linearity	±1/2 LSB
Differential Linearity	±1/2 LSB
Quantizing Error	±1/2 LSB
Monotonicity[3]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE[4]	
System Accuracy Drift (max) G = 1	±30 ppm of FSR/°C
System Accuracy Drift (max) G = 1000	±80 ppm of FSR/°C
DYNAMIC ACCURACY	
Sample and Hold Aperture Time	30ns
Aperture Time Uncertainty	±5ns
Differential Amplifier CMR	74dB (DC to 1kHz)
Channel Crosstalk	80dB down at 1kHz, for OFF channel to ON chann
ANALOG OUTPUT SECTION	
OUTPUT CHARACTERISTICS	
Number of Channels	2
Output Voltage Range (strap selectable)	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA
Output Impedance	1Ω
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Output Settling Time (max)	10μsec
ACCURACY	
Output Accuracy	±0.0125% FSR
Temperature Coefficient of Accuracy	±30 ppm of FSR/°C
POWER REQUIREMENTS	
MP2216, MP2216-AO	+5V ±5% at 1.6 amp
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Relative Humidity	95% noncondensing

TABLE I. Electrical Specifications

NOTES:
1. Includes offset errors, gain errors, linearity errors.
2. FSR means Full Scale Range.
3. No missing codes guaranteed.
4. Includes offset drift, gain drift and linearity drift.

SYSTEM CONFIGURATIONS

The MP2216 microperipheral board is available in two versions.
MP2216-AO: All features of the MP2216 system are included in this configuration.
MP2216: Provides all features except the two digital-to-analog converters.

MP8004: Cable assembly - two required.

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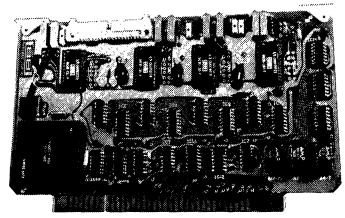


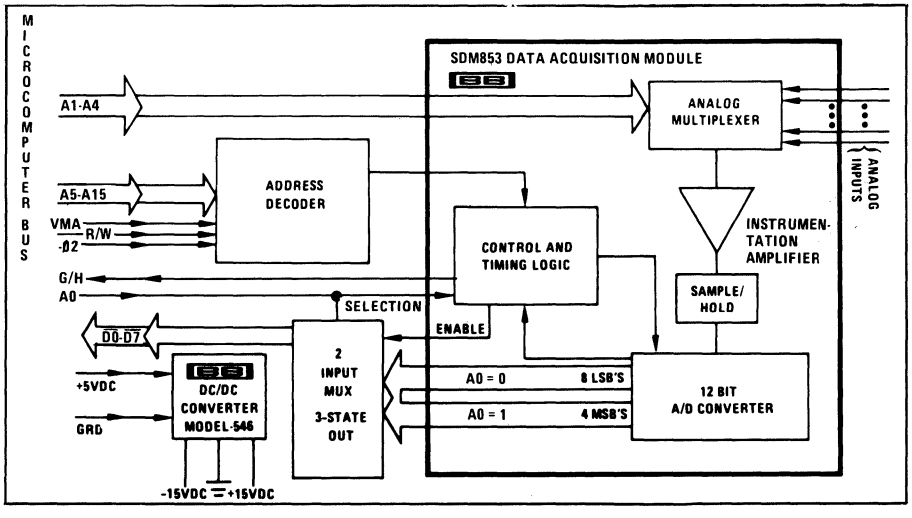
MP7104
MP7208
MP7216

MICROCOMPUTER ANALOG I/O SYSTEMS

MP7104 - Analog Output System
MP7208 - Data Acquisition System
MP7216 - Data Acquisition System

FEATURES

- COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser®
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Operates from +5VDC power supply
- EASY TO USE
  - All cabling and connectors are included



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PDS-352B

DESCRIPTION

These microcomputer peripherals provide two much needed functions that interface directly to Motorola's Micromodule and EXORciser microcomputers. The functions are: 1) Analog Data Acquisition and 2) Analog Output. The devices are electrically and mechanically compatible with Motorola microcomputers. Each analog system is contained on a single printed circuit board that is treated as memory input and output by the CPU. The cards will mate to any memory or I/O slot. The analog interface for each system is at a flat cable connector at the opposite edge of the board from the bus connector.

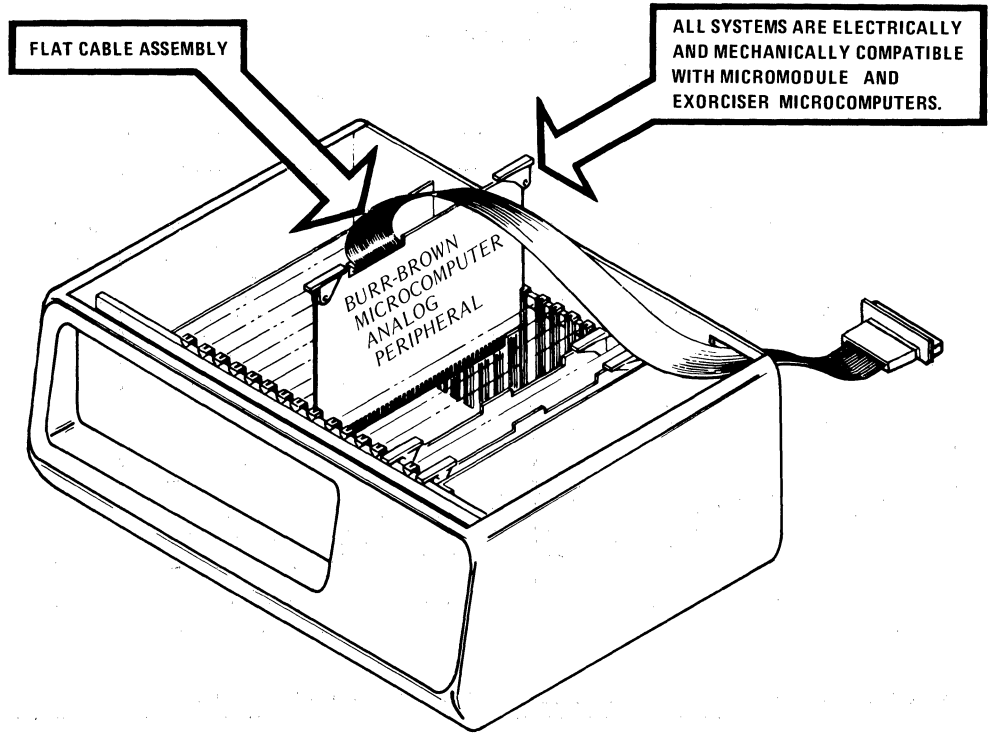
The Data Acquisition Systems consist of the MP7208, an 8 channel differential input system; and the MP7216, a 16 channel single-ended input system. Burr-Brown's SDM853 modular data acquisition system is used to implement these systems. The data acquisition systems include an input multiplexer, high gain instrumentation amplifier, sample/hold and 12 bit A/D converter along with all the necessary timing, decoding and control logic. The model 546 DC/DC converter (+5V to ±15V) is also used so that only the microcomputer's +5VDC power supply is required.

The MP7104, an analog output system, provides four analog output channels (using four of Burr-Brown's hybrid 12 bit DAC80 D/A converters). This board also contains the 546 DC/DC converter to assure operation on +5VDC power. The input of the D/A converters are double buffered so that a complete 12 bit word can be strobed into a D/A converter's input register to minimize output glitches.

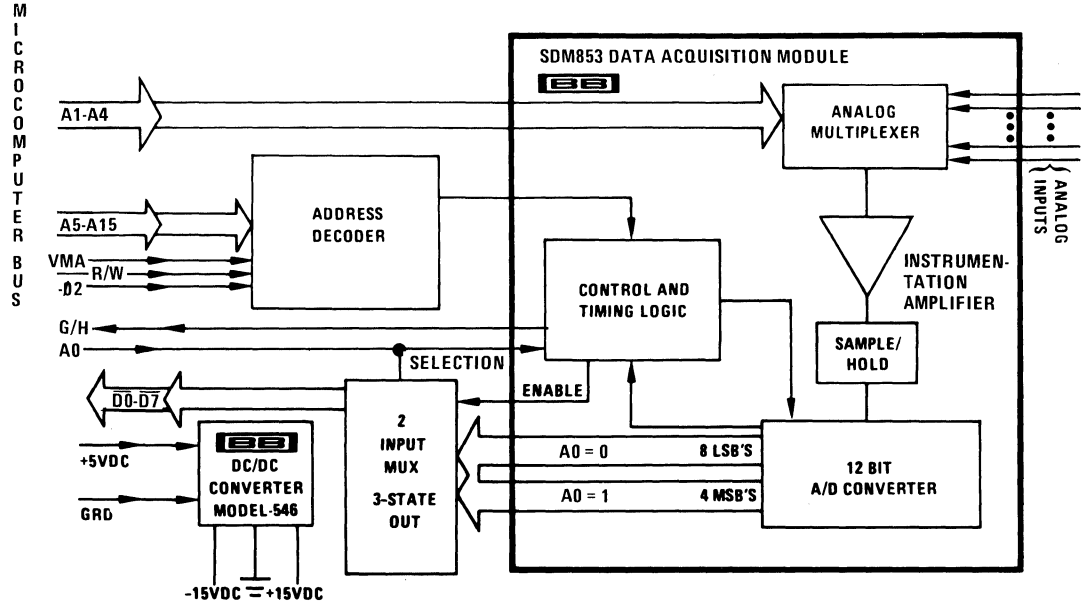
THEORY OF OPERATION

When programming with these peripherals, they are treated as memory locations. Both the A/D converter output and the D/A converter input are 12 bit words so two 8 bit memory locations are needed for each channel. But, because the address block occupied by each peripheral is switch selectable, it can be placed anywhere in memory. Since these units are treated as memory, a single instruction is all that's needed to set the input of a D/A converter. For instance, the STX (write) instruction followed by the proper address is used to write data from the index register to the MP7104. The four most significant bits are written first followed by the eight least significant bits. Through double buffering in the MP7104 only one 12 bit data transfer is made to the DAC to minimize glitching.

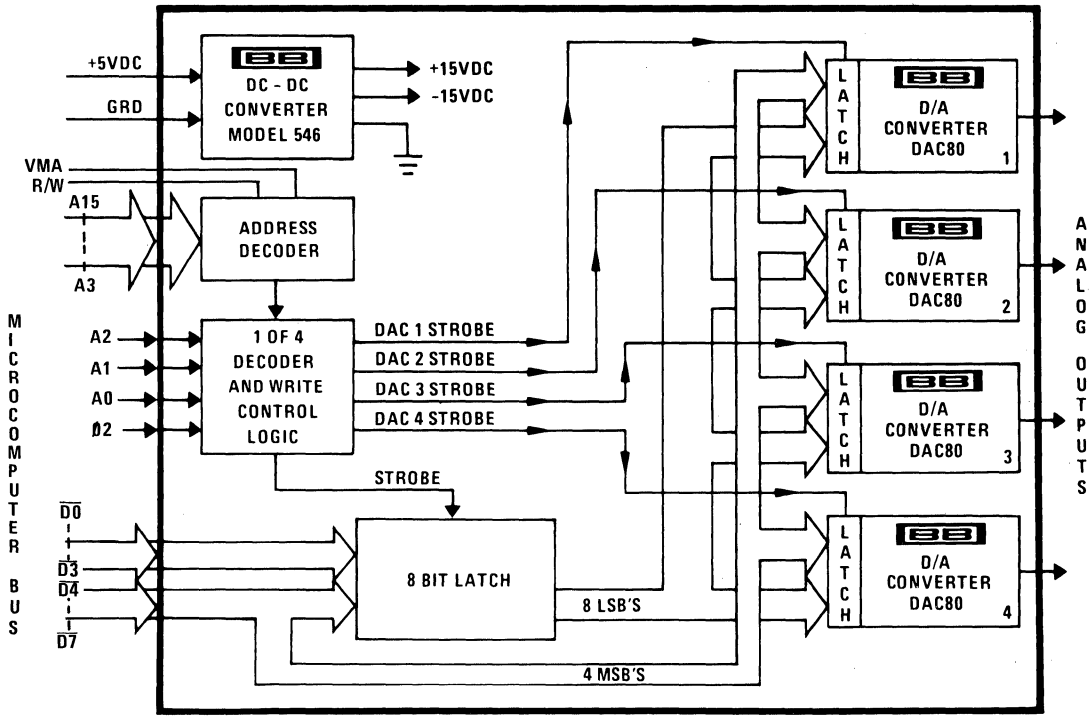
All of these systems are jumpered at the factory with the first channel at address $EF00_{16}$ (that's 1110 1111 0000 0000 in binary). Each subsequent channel is two memory locations past the start of the last channel so that the second channel is at location $EF02_{16}$ (1110 1111 0000 0010).



ANALOG INPUT SYSTEM - MP7208/7216



ANALOG OUTPUT SYSTEM - MP7104



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT	
Number of analog inputs	
8 channel differential	MP7208
16 channel single-ended	MP7216
Input voltage range[1]	±10mV to ±10V
Input current loop ranges (resistor programmable)	4-20mA, 10-50mA
ADC gain ranges (strap selectable)	±10V, 0 to 10V, 0 to 5V ±5, ±2.5V
Amplifier gain range (resistor programmable)	1 to 1000 V/V
Amplifier gain equation (resistor programmable)	$G = 1 + 20k\Omega / R_{EXT}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C	20nA
0 to 70°C	50nA
Amplifier output noise (Gain = 100 R_S = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage (max)[4]	400μV
Amplifier input offset voltage drift (max)	$2 + \frac{20}{G}$ μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy, ±10V range (max)	±0.025% FSR[2]
±10mV range	±0.1% FSR
Temperature coefficient of accuracy	
±10V range (max)	±0.003% FSR °C
±10mV range	±0.01% FSR °C
Conversion time ±10V range	33 microseconds
±10mV range	100 microseconds
CMRR (for differential inputs)	74 dB (DC to 2000 Hz)
Sample hold aperture time	30ns
DIGITAL INPUT/OUTPUT	
All signals are compatible with Micro-computer bus	
Output coding	Bipolar, Two's Complement; unipolar, straight binary
An analog input channel is selected by:	A1 through A4
The output data bits are read into:[3]	$\overline{D0}$ through $\overline{D7}$
POWER REQUIREMENTS	
MP7208, MP7216	+5VDC ±5% at 1 amp, 25mV ripple
MP7217-NS, MP7209-NS	+5VDC ±5% at +500mA, 25mV ripple +15VDC±3% at +50mA, 5mV ripple -15VDC ±3% at -75mA, 5mV ripple
TEMPERATURE RANGE	
Temperature	0 to 70°C
ANALOG OUTPUT	
Number of analog outputs: 4	MP7104
Output voltage range[1]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time	< 10 microseconds
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy (max)	±0.0125% FSR
Temperature coefficient of accuracy	
Unipolar	±0.003% FSR/°C
Bipolar	±0.0045% FSR/°C
DIGITAL INPUT/OUTPUT	
All signals are compatible with Micro-computer bus	
An analog output channel is selected by:	A1 and A2
The input data bits are read by:	$\overline{D0}$ through $\overline{D7}$
POWER REQUIREMENTS	
MP7104	+5VDC ±5% at +1 amp, 25mV ripple
MP7105-NS	+5VDC ±5% at +500 mA ±5mV ripple +15VDC±3% at +100mA, 5mV ripple -15VDC ±3% at -100mA, 5mV ripple
TEMPERATURE RANGE	
Temperature	0 to 70°C

OPERATING INSTRUCTIONS

INSTALLATION

The MP7104, MP7208 and the MP7216 are shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot in the EXORciser or with a Micromodule and routing the board's mating I/O cable to the back panel. The cable supplied with each board is shielded and, in the case of the MP7104, provided with the proper terminations.

PROGRAMMING

Programming of these analog I/O boards is easily accomplished since all are treated as memory locations. The MP7104 uses any memory reference instruction that can write data from the index and stack point registers or the accumulators. In a similar manner a channel in the MP7208 or MP7216 can be read by any memory reference instruction that can read data into the index and stack pointer registers or the accumulators.

The voltage data for these boards is represented by a 12 bit two's complement binary number. Each bit has a value of 4.88mV, with the polarity of the voltage indicated by the sign of the binary number. Since the index, stack pointer and A and B accumulator pair registers are 16 bits long and the data word is 12 bits, the MP7208 and MP7216 set these unused bits to the same value as the most significant bit of the data. This assures the proper representation of the data's sign.

Each board is set at the factory for a block of addresses beginning at EF00. Any analog data channel requires two memory locations since the digital data is 12 bits. The most significant 4 bits of data are always located in an even location while the remaining 8 bits are located in the next higher location. Thus, the first analog channel is located at EF00 and EF01 while the second analog channel is located at EF02 and EF03. When moving data, all boards require that the most significant bits (even addresses) be referenced first. In addition, the MP7208 and MP7216 systems require the most significant data to be read followed by a NOP instruction for proper starting of the conversion process. This can be illustrated as shown below:

```
LDAA    EF00    Starts conversion of CH0
NOP             Allows processor to halt
                during conversion
LDX     EF00    Reads data as soon as
                conversion is complete
```

(1) Connected at the factory for ±10V range.
(2) FSR is Full Scale Range (i.e., 20V for ±10V range, 10V for 0 to +10V range).
(3) The 4 MSB's when conversion is complete, followed by the 8 LSB's.
(4) Adjustable to zero.

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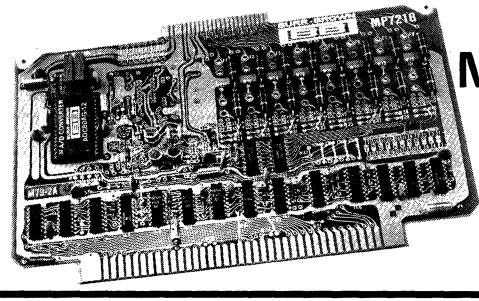
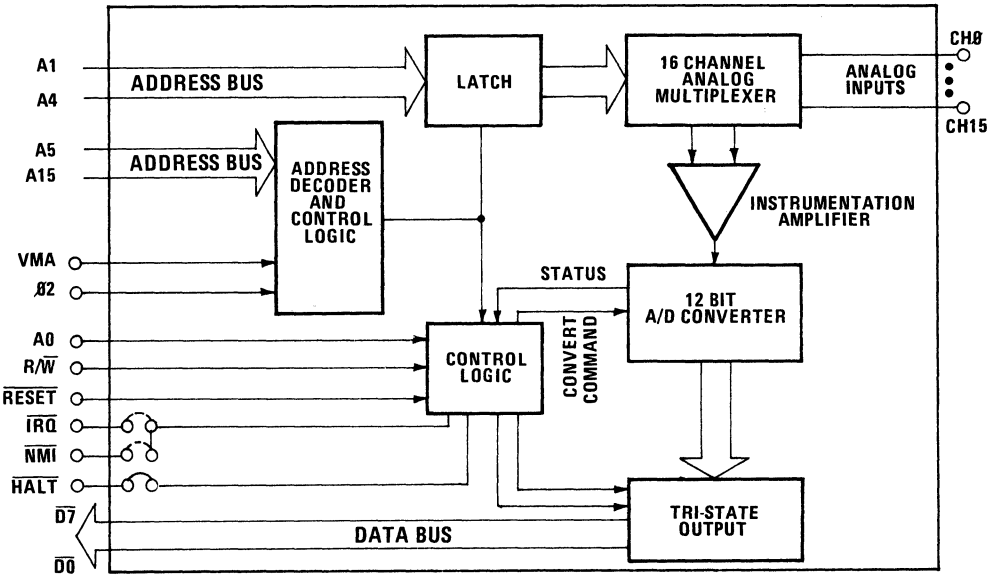


MP7218

MICROCOMPUTER ANALOG INPUT SYSTEM

A LOW-COST 12-BIT, 16-CHANNEL ANALOG INPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® MICROCOMPUTERS



FEATURES

- 70°C BURN-IN
- OPERATES FROM COMPUTER'S ±12VDC, +5VDC POWER SUPPLY
- ACCEPTS LOW LEVEL INPUTS
- EASY TO PROGRAM

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DESCRIPTION

The MP7218 is an analog input microperipheral board designed to be used with Motorola's Micromodule and EXORciser® microcomputer systems. It is electrically and mechanically compatible with these systems. The analog system is contained on a single printed circuit board that is treated as memory by the CPU. The analog interface is at a connector on the opposite edge of the board from the bus connector.

This data acquisition system includes 25V input overvoltage protection, an analog multiplexer, high gain instrumentation amplifier, and 12 bit A/D converter along with all the necessary timing, decoding and control logic. The unit operates from the microcomputer's +5VDC and ±12VDC power supplies. The MP7218 is capable of interfacing ±10mV to ±5V signal levels.

When programming with this peripheral, it is treated as memory. The A/D converter output is a 12 bit word so two 8 bit memory locations are needed for each channel. Address bits A15-A5 select the board and A4-A1 select the analog input channel to be digitized. To start a conversion the board is written to using an STA or similar instruction. After conversion data remains in the output latches waiting to be read until another conversion is initiated. This unit may be used with or without halting the CPU or in the interrupt mode.

The MP7218 is jumpered at the factory with the first channel at address $93E0_{16}$, the second at $93E2_{16}$, etc. By changing jumpers, the boards may be placed anywhere in memory.

SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT	MP7218
Number of analog inputs	8 differential/16 single-ended(1)
Input range	±10mV to ±5V(2)
ADC gain ranges (strap selectable)	0 to 5V ±5V, ±2.5V
Amplifier gain range	1 to 1000
Factory set gain	1
Amplifier gain equation (resistor programmable)	$G = 1 + 20k\Omega/R_{EXT}$
Input overvoltage protection	±25V
Input impedance, DC	100 megohms
Bias current 25°C 0 to 70°C	 20nA 50nA
Amplifier output noise (Gain = 100 R_S = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage, max	400μV
Amplifier input offset voltage drift, max	(2 + 20/G)μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy, (±5V range, max) ±10mV range	±0.025% FSR(3) ±0.1% FSR
Temperature coefficient of accuracy range, max ±5V ±10mV range	 ±0.004% FSR/°C ±0.01% FSR/°C
Conversion time ±5V range ±10mV range	50 microseconds 100 microseconds
CMRR (for differential inputs)	90dB (DC to 60 Hz)
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
Output coding	Bipolar, two's complement(4)
Logic loading (all inputs)	One LSTTL load
Data bus output drive	20 TTL loads
$\overline{HALT}$, $\overline{IRQ}$, $\overline{NMI}$ output drive	10 TTL loads
POWER REQUIREMENTS	
Power supply voltages	+5VDC at 100mA, +12VDC at 50mA -12VDC at 75mA
Range for rated accuracy	4.75V to 5.25V and ±11.4V to ±12.6V
TEMPERATURE RANGE	
Temperature	0°C to 70°C

(1) Connected at the factory as 8 channels differential.
(2) Connected at the factory for ±5V range.
(3) FSR is Full Scale Range (i.e., 10V for ±5V range, 5V for 0 to +5V range).
(4) Straight binary jumper selectable. (W80, W81)

MECHANICAL CHARACTERISTICS

Compatible with EXORciser and Micromodule card spacing.

Minimum card spacing: 12.7mm (0.5″)

Microcomputer bus connector required: 86 pin PC edge connector with 0.156″ contact centers (SAE-43D/1-2).

Analog connector: 50 pin PC edge connector with 0.100″ contact centers. Burr-Brown part number: 2250MC (Viking # 3VH25/1JN5 - solder tab). Scotchflex cable connector also available from 3M (# 3415-0001).

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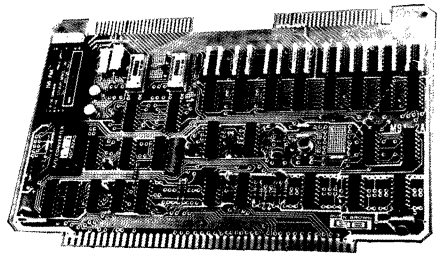
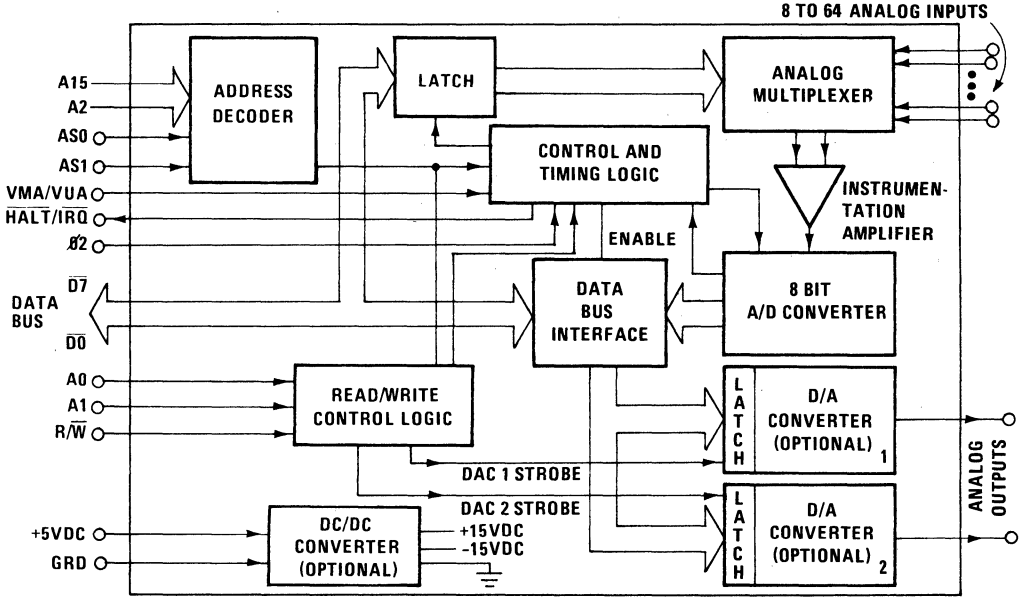


MP7408
MP7432

MICROCOMPUTER ANALOG I/O SYSTEM

A LOW-COST 64-CHANNEL ANALOG INPUT/2 CHANNEL ANALOG OUTPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® SYSTEMS



FEATURES

- EASY TO PROGRAM
  Systems are treated as memory
- REDUCES SYSTEM DEVELOPMENT TIME
- EASY TO USE
  8 to 64 input channels on one board
  Analog input and output on one board
  High level or low level inputs
- 70°C BURN-IN

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PDS-378

DESCRIPTION

This microcomputer peripheral provides two functions that interface directly to Motorola's Micromodule and EXORciser microcomputers. The functions are: (1) Analog Data Acquisition and (2) Analog Output. Both analog input and output systems are contained on a single printed circuit board that is treated as memory input or output by the CPU. The analog interface is at connectors on the opposite edge of the board from the bus connector.

The Data Acquisition System is available with up to 32 channels differential (64 channels single-ended) on one board. It includes an input multiplexer, high gain instrumentation amplifier, 8-bit A/D converter along with all the necessary timing, decoding and control logic. This system can digitize low level or high level analog signals. The gain of the internal instrumentation amplifier can be programmed with a single external resistor to allow input signal ranges as low as ±2.5mV. This means that the MP7400 can be connected to low level sensors such as thermocouples and strain gauges without external signal amplification. A DC/DC converter (+5V to ±15V) is also available so that only the computer's power supply is required. The Data Acquisition System is available with two optional 8-bit D/A converters to provide analog output in addition to input on the same board.

THEORY OF OPERATION

When programming these peripherals, they are treated as memory locations. Any memory reference instruction can be used. Two memory locations are used by the analog input system. One location is used to select the channel and start conversion. The same location provides status information when read. The other location contains the converted data. The analog output system also uses two memory locations, one for each channel.

Because these units are treated as memory, a minimum of instructions are needed to read an input channel or to set the output of a D/A converter. The MP7400's versatile memory mapped operation allows it to be used with or without halting the CPU or in the interrupt mode.

All of these units are jumpered at the factory for address 95F0 through 95F3.

SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT/OUTPUT SYSTEM

ANALOG INPUT

Number of analog inputs	
8 differential (16 signal-ended)[5]	MP7408
32 differential (64 single-ended)[6]	MP7432
Input voltage range[1]	±5mV to ±5V
ADC gain ranges[1] (strap selectable)	±10V, 0 to 10V 0 to 5V ±5V, ±2.5V
Amplifier gain range[1] (resistor programmable)	1 to 1000
Amplifier gain equation	$G = 100k\Omega / R_{EXT}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C (max)	+300nA
0°C to 70°C	-2nA/°C
Amplifier input offset voltage drift	$\pm\left(5 + \frac{1000}{G}\right)$ μV/°C

ANALOG INPUT TRANSFER CHARACTERISTICS

Resolution	8 bit binary
Throughput accuracy ±5V range (max)	±0.4% FSR[2]
Throughput accuracy ±10mV range	±0.5% FSR
Temperature coefficient of accuracy	
±5V range (max)	±0.02% FSR/°C
±10mV range	±0.07% FSR/°C
Conversion time ±5V range (max)	44 microseconds
Conversion time ±10mV range (max)	84 microseocnds
CMRR (for differential inputs)[3]	66 dB (Gain = 2) 86 dB (Gain = 100)

ANALOG OUTPUT

Number of analog outputs	2
Output voltage range[4]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time (max)	< 5 microseconds

ANALOG OUTPUT TRANSFER CHARACTERISTICS

Resolution	8 bit binary
Throughput accuracy (max)	±0.4% FSR
Temperature coefficient of accuracy	
Unipolar	±0.005% FSR/°C
Bipolar	±0.01% FSR/°C

DIGITAL INPUT/OUTPUT

All signals are compatible with Motorola Microcomputer Bus	
Output coding	Bipolar, two's complement; Unipolar, straight binary
An analog input channel is selected by:	$\overline{D0}$ through $\overline{D5}$
An analog output channel is selected by:	A0
The input/output data bits are read through:	$\overline{D0}$ through $\overline{D7}$

POWER REQUIREMENTS

MP7408, MP7432	+5VDC +5% at 1 amp
MP7408-NS, MP7432-NS	+5VDC ±5% at 500mA +15VDC ±5% at 40mA -15VDC ±5% at 40mA
With analog output MP7408-AO, MP7432-AO	+5VDC ±5% at 2 amp
MP7408-NS-AO, MP7432-NS-AO	+5VDC ±5% at 500mA +15VDC ±5% at 100mA -15VDC ±5% at 100mA

TEMPERATURE RANGE

0°C to 70°C

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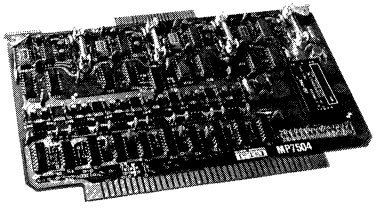
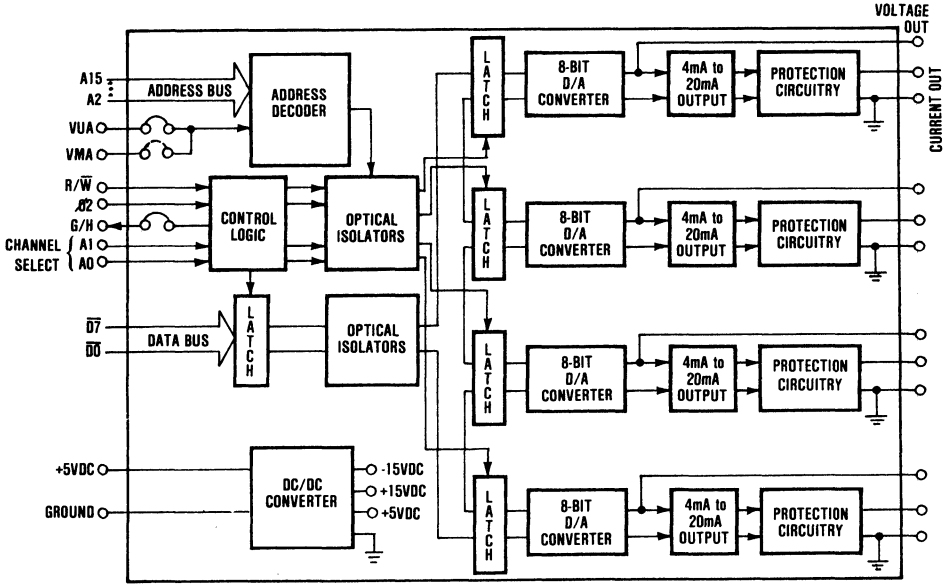


MP7504

MICROCOMPUTER ANALOG OUTPUT SYSTEM

A 4-CHANNEL, 8-BIT ISOLATED ANALOG OUTPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® MICROCOMPUTERS



FEATURES

- OUTPUT ISOLATION/OUTPUT PROTECTION
- REDUCES SYSTEM DEVELOPMENT TIME
  - System engineered and specified
  - Plug compatible
  - Operates from computer power supply
  - Easy to program
- COMPATIBLE WITH ROCKWELL SYSTEM 65
- MOTOROLA MICROMODULE AND EXORciser COMPATIBLE
- 4-CHANNEL ANALOG OUTPUT SYSTEM
- 4mA TO 20mA OUTPUT
- 70°C BURN-IN

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PDS-385A

DESCRIPTION

This microcomputer peripheral, burned in at 70°C to increase reliability and reduce aging shift, provides four optically-isolated 8-bit fused analog outputs that interface directly with Motorola's Micromodule and EXORciser microcomputers. The MP7504, electrically and mechanically compatible with these MPU's, is contained on a single printed circuit board that operates from the computer's +5 VDC power supply. Analog interface is through a card edge (direct) connector located on the opposite edge of the board from the bus connector.

The MP7504 which outputs 4mA to 20mA and 0-10V on each channel is programmed as memory locations. The address block used by each peripheral is selectable and can be placed anywhere in memory. A single instruction sets the input of a D/A converter.

ELECTRICAL SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

MODEL	MP7504
ANALOG OUTPUT	
Number of analog outputs	4
Output current range	4mA to 20mA
Maximum load	400Ω
Compliance	8V
Output settling time	50μsec
Output voltage range	0-10V at 5mA
Output impedance	1Ω
Output settling time	30μsec
TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
One LSB (voltage)	39.1mV
One LSB (current)	62.5μA
Throughput accuracy, max	±0.4% of FSR
Temperature coefficient of accuracy	
Voltage output	±50ppm of fSR/°C
Current output	±150ppm of FSR/°C
ISOLATION	
Isolation voltage between microcomputer bus and outputs	600VDC
DIGITAL INPUT/OUTPUT	
All signals compatible with microcomputer bus	
Logic loading (all inputs)	One LSTTL load
Analog output channels selected by:	A0, A1
Input data read by:	$\overline{D0}$-$\overline{D7}$
POWER REQUIREMENTS	
Rated voltage	+5VDC
Range for rated accuracy	4.75VDC to 5.25VDC
Supply drain at 5VDC	1.2A, typical; 1.8A max
TEMPERATURE RANGE	
Operating	0°C to 70°C

MECHANICAL

Compatible with Micromodule and EXORciser card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers (SAE-43D/1-2).

Analog Connector: 50-pin output P.C.B. edge connector. A mating connector is available from Burr-Brown:

2250MC (Viking # 3 VH25/1JN5, solder tab).

A Scotchflex connector (3415-0001) is available from 3M.

OPERATING INSTRUCTIONS

PROGRAMMING

Because this analog output board is treated as memory, programming is simple. The MP7504 uses any memory reference instruction that can write data from the CPU.

Each board is factory set for a block of addresses beginning at 94FC. Each analog data channel requires one memory location. When a data word is written to the MP7504 it is stored in an input latch. The optical isolators following the input latch require 15 microseconds to transfer new data to the D/A converter latches. Do not write to the board during this transmission period. To insure proper operation, use one of these modes:

1) HALT mode (shipped in this mode):

Jumper W33 is installed. The conversion command (write instruction) is followed with a NOP instruction. In this mode, the board halts the processor during data transfer sequences. For example:

STAA 94FE	Transfers data in accumulator to MP7504 for channel 2.
NOP	Allows MP7504 to halt processor for 15 microseconds during transfer of data to channel 2.

2) COUNT DOWN mode

Jumper W33 is removed. Software control does not permit the program to write to the board for 15 microseconds. For example:

STAA 94FE	Transfers data in accumulator to MP7504 for channel 2.
⋮	{ System software does not allow another write to the MP7504 for 15 microseconds.

CHANNEL	FACTORY SET LOCATION
0	94FC
1	94FD
2	94FE
3	94FF

TABLE I. Analog Output Channel Locations.

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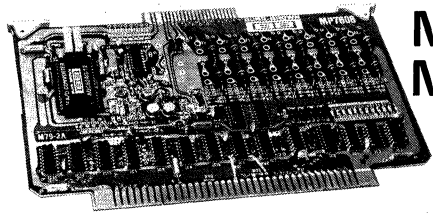
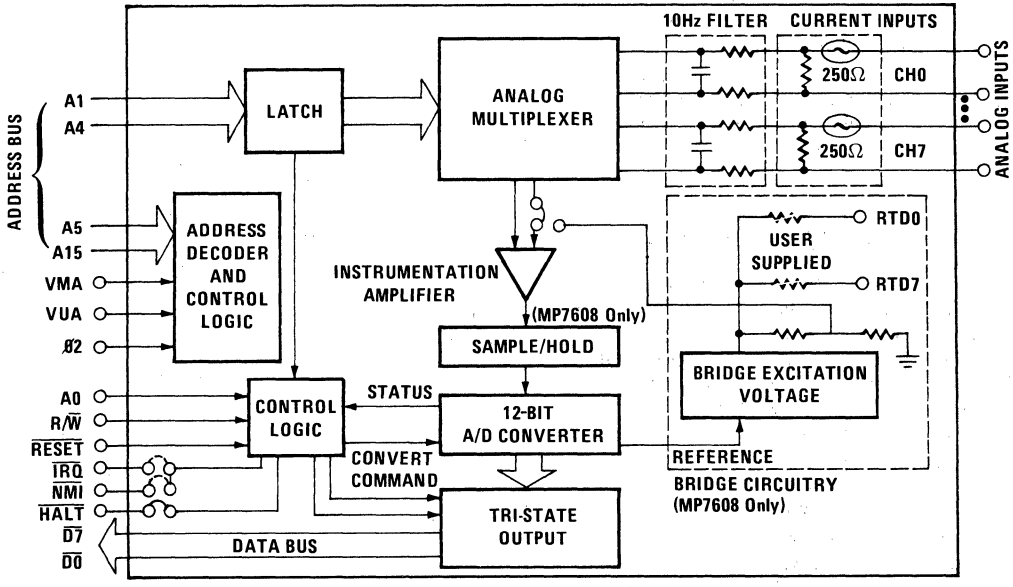


MP7608
MP7608-I

MICROCOMPUTER ANALOG INPUT SYSTEMS

A 12-BIT, 8-CHANNEL "INDUSTRIAL" ANALOG INPUT SYSTEM COMPATIBLE WITH MOTOROLA MICROMODULE AND EXORciser® MICROCOMPUTERS



FEATURES

- CURRENT-LOOP INPUTS
- HIGH OR LOW LEVEL VOLTAGE INPUTS
- INPUTS PROTECTED TO 200VDC
- CURRENT INPUTS FUSED
- IMMUNE TO NOISE
  Input filter on each channel
  Differential inputs
- BRIDGE INPUTS
- 70°C BURN-IN

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PDS-380

DESCRIPTION

The MP7608 and MP7608-I are analog input microperipheral boards designed to be used with Motorola's Micromodule and EXORciser microcomputer systems. They are electrically and mechanically compatible with Motorola microcomputers. Each analog system is contained on a single printed circuit board that is treated as memory by the CPU. The analog interface for each system is at a connector at the opposite edge of the board from the bus connector.

These data acquisition systems include 200V input overvoltage protection, an input filter, analog multiplexer, high gain instrumentation amplifier, sample/hold and 12 bit A/D converter along with all the necessary timing, decoding and control logic. They operate from the microcomputer's +5VDC and ±12VDC power supplies.

The MP7608 is a voltage input system capable of interfacing ±10mV to ±5V signal levels. Excitation and bridge circuitry is also included on this board for interface to sensors such as RTD's and strain gages. The MP7608-I is a current input system designed to interface to 4-20mA current loop signals. The MP7608-I also includes input fuses to protect the 250Ω precision input current resistors.

THEORY OF OPERATION

When programming with these peripherals, they are treated as memory locations. The A/D converter output is a 12 bit word so two 8 bit memory locations are needed for each channel. Address bits A15-A5 select the board and A4-A1 select the analog input channel to be digitized. To start a conversion the board is written to using an STA or similar instruction. The data remains in the output latches waiting to be read until another conversion is initiated. These peripherals may be used with or without halting the CPU or in the interrupt mode.

The MP7608/MP7608-I are jumpered at the factory with the first channel at address $93E0_{16}$, the second at $93E2_{16}$, etc. By changing jumpers, the boards may be placed anywhere in memory.

SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ELECTRICAL

ANALOG INPUT	MP7608-I	MP7608
Number of analog inputs	8 differential(1)	8 differential(1)
Input range	0-20mA(2)	±10mV to ±5V(3)
ADC gain ranges	±10V, 0 to 10V, 0 to 5V	±10V, 0 to 10V, 0 to 5V,
(strap selectable)	±5V, ±2.5V	±5V, ±2.5V
Amplifier gain range	1 to 500	1 to 500
Factory set gain	1	1(5)
Amplifier gain equation	$G = 1 + 20k\Omega/R_{EXT}$	$G = 1 + 20k\Omega/R_{EXT}$
(resistor programmable)		
Input overvoltage protection	±200V	±200V
Input filter	One pole RC, 10Hz	One pole RC, 10Hz
Input impedance, DC	250Ω	100 megohms
Bias current		
25°C	20nA	7nA
0 to 70°C	50nA	10nA
Amplifier output noise	1.2mV rms; 7mV p-p	0.5mV rms; 3mV p-p
(Gain = 100 R_S = 500Ω)		
Amplifier input offset voltage, max	400μV	200μV
Amplifier input offset voltage drift, max	2 + 20/G μV/°C	1 + 20/G μV/°C
TRANSFER CHARACTERISTICS		
Resolution	12 bits binary	12 bits binary
Throughput accuracy,		
±5V or 0-20mA range, max	±0.025% FSR(4)	±0.025% FSR(4)
±10mV range	±0.1% FSR	±0.1% FSR
Temperature coefficient of accuracy		
±5V or 0-20mA range, max	±0.004% FSR/°C	±0.004% FSR/°C
±10mV range	±0.01% FSR/°C	±0.01% FSR/°C
Conversion time ±5V or 0-20mA range	60 microseconds	175 microseconds
±10mV range	125 microseconds	525 microseconds
CMRR (for differential inputs)	90dB (DC to 60Hz)	90dB (DC to 60Hz)
DIGITAL INPUT/OUTPUT		
All signals are compatible with Microcomputer bus		
Output coding	unipolar, straight binary	bipolar,(6) two's complement
Logic loading (all inputs)	one LSTTL load	one LSTTL load
Data bus output drive	20 TTL loads	20 TTL loads
$\overline{HALT}$, $\overline{IRQ}$, $\overline{NMI}$ output drive	10 TTL loads	10 TTL loads
POWER REQUIREMENTS		
Power supply voltages	+5VDC at 100mA, +12VDC at 50mA, -12VDC at 75mA	+5VDC at 100mA, +12VDC at 50mA, -12VDC at 75mA
Range for rated accuracy	4.75V to 5.25V and ±11.4V to ±12.6V	4.75V to 5.25V and ±11.4V to ±12.6V
TEMPERATURE RANGE		
Temperature	0 to 70°C	0 to 70°C

(1) May be connected as 16 channels single-ended without input filtering.
(2) May be set up to accept voltage signals.
(3) Connected at the factory for ±5V range.
(4) FSR is Full Scale Range (i.e., 10V for ±5V range, 5V for 0 to +5V range).
(5) Gains of 5 and 100 can be attained by adding jumpers.
(6) Unipolar straight binary is jumper selectable (W80, W81).

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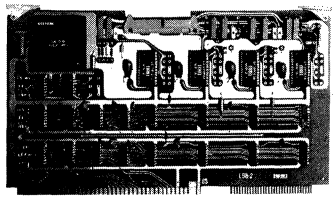


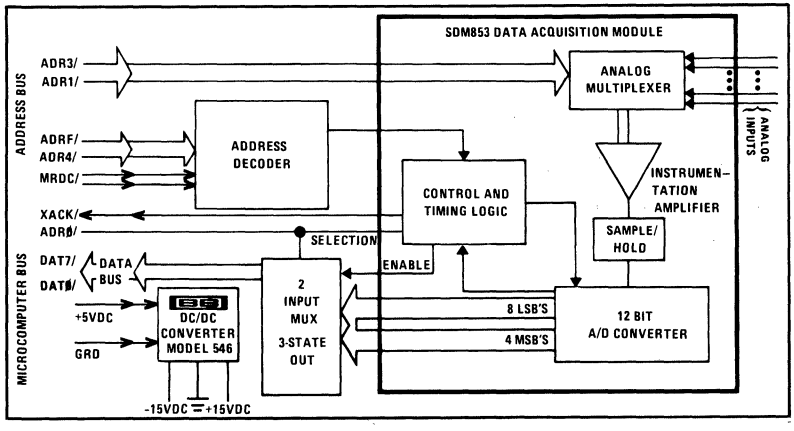
MP8304
MP8408
MP8416

MICROCOMPUTER ANALOG I/O SYSTEMS

INTEL - SBC80 and Intellec MDS Compatible
NATIONAL BLC80 Compatible
MP8304 - Analog Output System
MP8408 - Data Acquisition System
MP8416 - Data Acquisition System

FEATURES

- EASY TO PROGRAM
  Systems are treated as memory
- REDUCES SYSTEM DEVELOPMENT TIME
  System engineered and specified
  Operates from computer's +5VDC power supply if desired
- EASY TO USE
  All cabling and connectors are included



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DESCRIPTION

These microcomputer peripherals provide two much needed functions that interface directly to Intel's SBC80/10 and Intellec MDS microcomputers. The functions are: 1) Analog Data Acquisition and 2) Analog Output. The devices are electrically and mechanically compatible with any SBC80/10 and Intellec MDS. Each analog system is contained on a single printed circuit board that is treated as memory input or output by the CPU. The cards will mate to any memory or I/O slot. They are compatible with the 0.6" spacing of the SBC80/10 or the 0.75" spacing of the Intellec MDS. The analog interface for each system is at a flat cable connector at the opposite edge of the board from the bus connector.

The Data Acquisition systems consist of the MP8408, an 8 channel differential input system; and the MP8416, a 16 channel single-ended input system. Burr-Brown's SDM853 modular data acquisition system is used to implement these systems. The data acquisition systems include an input multiplexer, high gain instrumentation amplifier, sample/hold and 12 bit A/D converter along with all the necessary timing, decoding and control logic. The model 546 DC/DC converter (+5V to ±15V) is also used so that only the computer's +5VDC power supply is required.

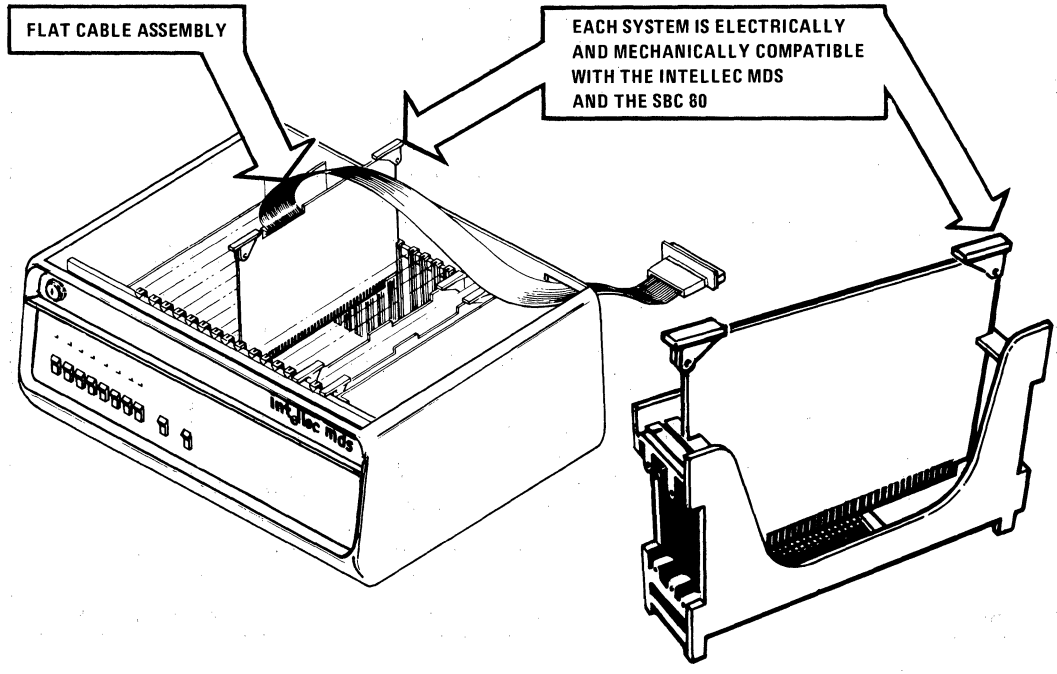
The MP8304, an analog output system, provides four analog output channels (using four of Burr-Brown's hybrid 12 bit DAC80 D/A converters). This board also contains the 546 DC/DC converter to assure operation on +5VDC power. The input of the D/A converters are double buffered so that a complete 12 bit word can be strobed into a D/A converter's input register to minimize output glitches. All of these systems are also offered in an OEM version without the DC/DC converter and cable.

THEORY OF OPERATION

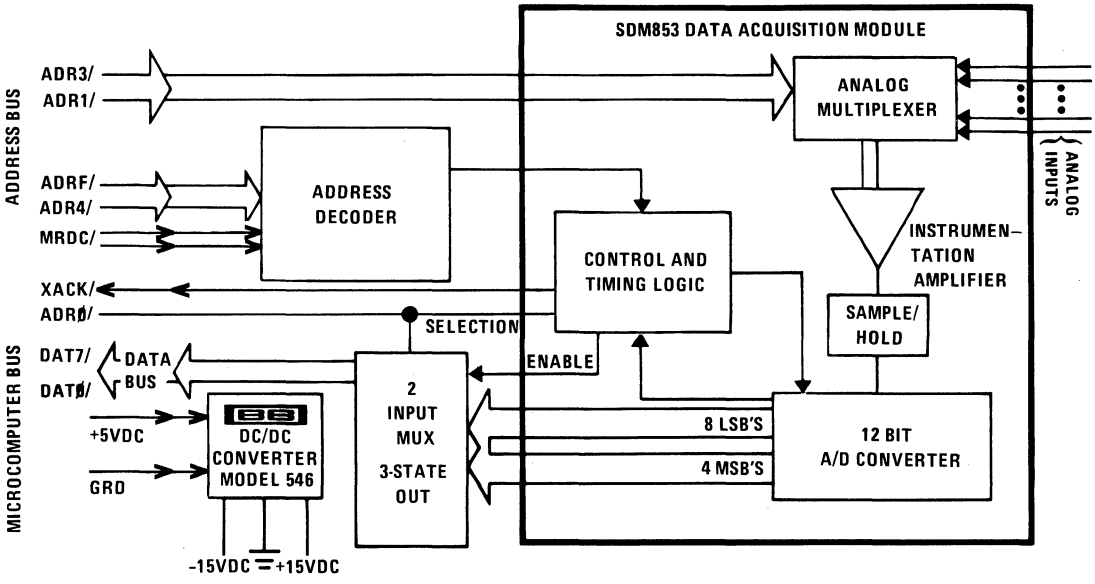
When programming with these peripherals, they are treated as memory locations. Both the A/D converter output and the D/A converter input are 12 bit words so two 8 bit memory locations are needed for each channel. But because the address block occupied by each peripheral is user selectable, it can be placed anywhere in memory. Existing memory can be overlapped since the peripherals inhibit all other memory that occupies the same memory locations.

Because these units are treated as memory, a single instruction is all that's needed to read an input channel or to set the input of a D/A converter. For instance, the LHLD (load) instruction followed by the proper address is used to read data from the MP8408 or MP8416. It will automatically select the desired channel, initiate conversion and when conversion is complete, transfer the A/D converter output for that channel to the 8080's H and L registers. The eight least significant bits are read first followed by the four most significant bits.

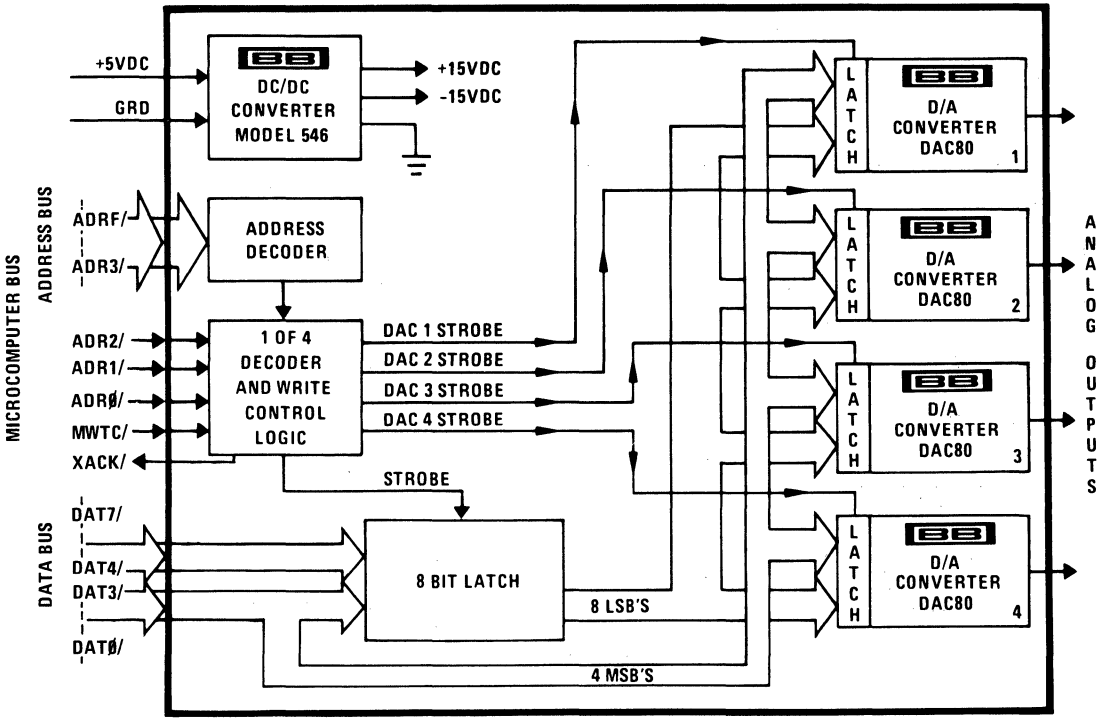
All of these systems are jumpered at the factory with the first channel at address $F720_{16}$. Each subsequent channel is two memory locations past the start of the last channel so that the second channel is at location $F722_{16}$.



ANALOG INPUT SYSTEM - MP8408/8416



ANALOG OUTPUT SYSTEM - MP8304



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT SYSTEMS	MP8408/MP8416
ANALOG INPUT	
Number of analog inputs	
8 differential	MP8408
16 single-ended	MP8416
Input voltage range[1]	±10mV to ±10V
Input current loop ranges (resistor programmable)	4-20mA 10-50mA, etc.
ADC gain ranges (strap selectable)	±10V, 0 to 10V, 0 to 5V ±5V, ±2.5V
Amplifier gain range (resistor programmable)	1 to 1000 V V
Amplifier gain equation	$G = 1 + 20\ k\Omega\ R_{EXT}$ (resistor programmable)
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C	20nA
0°C to 70°C	50nA
Amplifier output noise (Gain = 100 R_x = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage (max)[4]	400μV
Amplifier input offset voltage drift	$2 + \frac{20}{G}$ μV °C
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy ±10V range (max)	±0.025% FSR[2]
±10mV range	±0.1% FSR
Temperature coefficient of accuracy	
±10V range (max)	±0.003% FSR °C
±10mV range	±0.01% FSR °C
Conversion time ±10V range	33 microseconds
±10mV range	100 microseconds
CMRR (for differential inputs)	74 dB (DC to 2000 Hz)
Sample/hold aperture time	30ns
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
Output coding	Bipolar, Two's Complement; unipolar, straight binary
An analog input channel is selected by:	ADR1/ through ADR4/
The output data bits are read into:[3]	DAT0/ through DAT7/
POWER REQUIREMENTS	
MP8408, MP8416	+5VDC ±5% at 1 amp, 25mV ripple
MP8417-NS, MP8409-NS	+5VDC ±5% at +500mA, 25mV ripple +15VDC ±3% at +50mA, 5mV ripple -15VDC ±3% at -75mA, 5mV ripple
TEMPERATURE RANGE	
Temperature range	0°C to 70°C
ANALOG OUTPUT SYSTEMS	**MP8304**
ANALOG OUTPUT	
Number of analog outputs	4
Output voltage range[1]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA (strap selectable)
Output impedance	1Ω
Output settling time	< 10 microseconds
TRANSFER CHARACTERISTICS	
Resolution	12 bits binary
Throughput accuracy (max)	±0.0125% FSR
Temperature coefficient of accuracy	
Unipolar	±0.003% FSR/°C
Bipolar	±0.0045% FSR/°C
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer bus	
An analog output channel is selected by:	ADR1/ and ADR2/
The input data bits are read by:	DAT0/ through DAT7/
POWER REQUIREMENTS	
MP8304	+5VDC ±5% at +1 amp, 25mV ripple
MP8305-NS	+5VDC ±5% at +1 amp, 25mV ripple +15VDC ±3% at +100mA, 5mV ripple -15VDC ±3% at -100mA, 5mV ripple
TEMPERATURE RANGE	
Temperature range	0°C to 70°C

OPERATING INSTRUCTIONS

INSTALLATION

The MP8304, MP8408 and the MP8416 are shipped from the factory calibrated and ready for immediate use. Installation requires only plugging the card into any empty slot in the computer and routing the board's mating I/O cable. Cable placement is shown on page 10-30. The cable supplied with each board is shielded and, in the case of the MP8304, provided with the proper termination.

PROGRAMMING

Programming of these analog I/O boards is easily accomplished since all are treated as memory locations. The MP8304 uses a single SHLD instruction to load any of its four digital to analog converters from the H and L registers. In a similar manner a channel in the MP8408 or MP8416 is read by a single LHLD instruction.

The voltage data for these boards is represented by a 12 bit two's complement binary number. Each bit has a value of 4.88mV, with the polarity of the voltage indicated by the sign of the binary number. Since the H and L register pair is 16 bits long and the data word is 12 bits, the MP8408 and MP8416 set these unused bits to the same value as the most significant bit of the data. This assures proper representation of the data's sign.

Each board is set at the factory for a block of addresses beginning at F720. Any analog data channel requires two memory locations since the digital data is 12 bits. The least significant 8 bits of data are always located in an even location while the remaining 4 bits are located in the next higher location. Thus, the first analog channel is located at F720 and F721 while the second analog channel is located at F722 and F723. These boards can occupy the same address space as memory since they inhibit memory whenever they become active.

MECHANICAL CHARACTERISTICS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 12.7mm (0.5")

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers.

40 pin analog connector (3M - 3432) provided on board. Mating connector (for OEM versions) is 3M - 3417. Recommended cable also by 3M; 3476/40.

(1) Connected at the factory for ±10V range.
(2) FSR is Full Scale Range (i.e., 20V for ±10V range, 10V for 0 to +10V range).
(3) The 4 MSB's when conversion is complete, followed by the 8 LSB's.
(4) Adjustable to zero.

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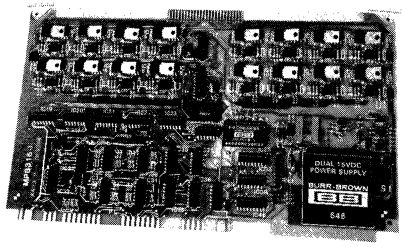


MP8316-I
MP8316-V

MICROCOMPUTER ANALOG OUTPUT SYSTEM

FEATURES

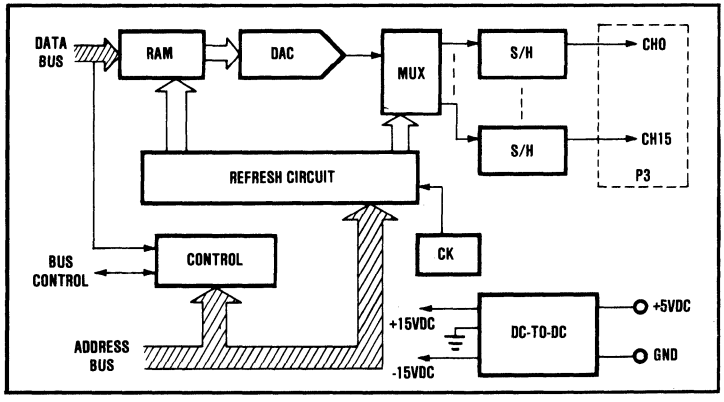
- 16 CHANNELS
- 0 - 24.57mA or ±10V OUTPUTS
- SINGLE GAIN AND OFFSET ADJUSTMENT
- MEMORY MAPPED or I/O OPERATION
- UP TO 20-BIT ADDRESS BUS
- 12-BIT RESOLUTION
- MULTIBUS™ COMPATIBLE

Multibus™ - Intel Corp.

DESCRIPTION

Dynamic analog outputs allow the MP8316 to provide high channel density on a single board. This approach frees system space for other peripherals and minimizes per channel power requirement. An on-board DC-to-DC converter powers the MP8316 from the system +5VDC supply. Channel data is stored in an on-board RAM and used by the refresh circuit to update outputs. Each channel is factory-adjusted to allow system calibration to be accomplished with a single gain and offset adjustment. Memory mapped or I/O operation is a jumper-programmable option on the board.

Two models of the MP8316 are available. Both models have 16 analog outputs and 12-bit resolution. The current output model (MP8316-I) will sink up to 24.57mA on each channel and is well suited for 4mA to 20mA operation. The voltage output model (MP8316-V) can be jumpered for bipolar or unipolar operation. Both units conform to Intel's Multibus™ specification.



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PDS-438

SPECIFICATIONS

ELECTRICAL

Typical at 25°C and rated power supplies unless otherwise specified.

MODEL	MP8316-I	MP8316-V
OUTPUTS		
Type	Current sink	Voltage
Number of Channels	16	16
Resolution	12-bit	12-bit
Range	0 to 24.57mA 10V min 80V max 1W max	±10V, ±5V, ±2.5V 0 to +10V 0 to +5V at 5mA max
ACCURACY		
Total Accuracy(1) max	±0.1% FSR(2)	±0.07% FSR
Offset Error	±1/2LSB (0.012%)	±1/2LSB (0.012%)
Linearity	±1/2LSB	±1/2LSB
Gain Error	0.1% FSR	0.05% FSR
Crosstalk	±1/2LSB	±1/2LSB
Temperature Coefficient	±50ppm/°C	±30ppm/°C
TIMING		
Refresh Scan Time	845μsec	845μsec
Charge Time per Scan	46.2μsec	46.2μsec
Settling Time		
to 0.1% of FSR	8.5msec	3.5msec
to 1/2LSB	11msec	5msec
DATA HOLD TIME ON BUS	200nsec	200nsec
BUS CONFIGURATION	Multibus ™	Multibus ™
POWER		
+5V ±5% (system bus)	1.5A	1.5A
ENVIRONMENT		
Operating Temperature	0°C to +70°C	
Relative Humidity	95% noncondensing	

NOTES:

1. With gain and offset error calibrated as described under Calibration, includes linearity error, channel-to-channel offset error, channel-to-channel gain error and crosstalk.
2. FSR is full scale range.

MECHANICAL

Compatible with Intellec MDS and iSBC-604/614 card spacing.
Minimum card spacing: 15.2mm (0.6").
Microcomputer bus connector required: 86-pin PC edge connector with 0.156" contact centers.
50-pin analog edge connector on board for analog outputs, 0.100" contact centers.
Mating connectors:
Burr-Brown 2250MC (Viking #3VH25/1JNS, solder tab).
3M Corporation 3415-0001 (Scothflex, for flat cable).

THEORY OF OPERATION

The dynamic output approach uses a single digital-to-analog converter (DAC) to drive all 16 outputs. Digital data for each channel is stored in an on-board RAM and analog output data for each channel is stored in separate sample/hold circuits. The refresh circuit contains a channel counter that selects the appropriate DAC input from RAM for the channel being updated and multiplexes the DAC output to the appropriate channel sample/hold. Thus, the output data is updated independent of the host CPU. The CPU changes data in RAM by a write operation to the appropriate channel. When this occurs, the refresh circuit disables the multiplexer to prevent output glitches and to allow the CPU to change the RAM data.

Table I describes the Multibus™ control signals used by the MP8316. The pinout of the bus connector (P1) conforms to the Multibus™ specifications. Control lines BPRN/ and BPRO/ are connected so that the MP8316 will not interfere with multiple processor operation when the serial priority technique is used. The auxiliary connector (P2) is not used.

TABLE I. Description of Control Lines.

Control Line	Description
INIT/	This signal resets the system.
INH 1/	Prevents RAM from responding.
INH 2/	Prevents ROM from responding.
MWTC/	Memory write command.
IOWC/	I/O write command.
XACK/	Slave acknowledge to host CPU that data has been taken from data bus for write operation or that valid data has been placed on the bus for read operation.
BPRN/	BUS PRIORITY IN - indicates that no higher priority module is requesting the bus.
BPRO/	BUS PRIORITY OUT - passed to BPRN/ input of the next lower priority module.

OPERATING INSTRUCTIONS

INSTALLATION

The MP8316 comes factory-adjusted and ready for use. Analog outputs are available on connector P3. Current outputs require an external current source (see Figure 1).

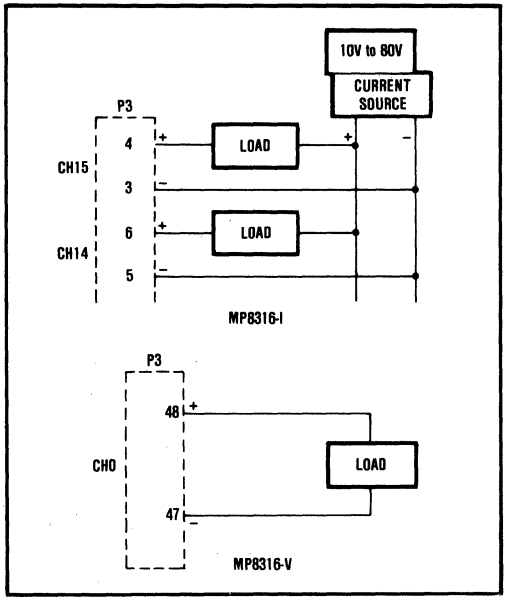

FIGURE 1. Connections for Current and Voltage Outputs.

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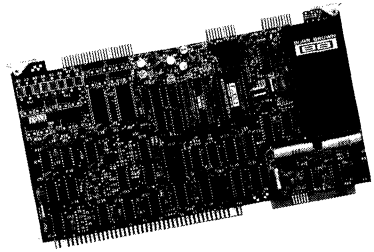


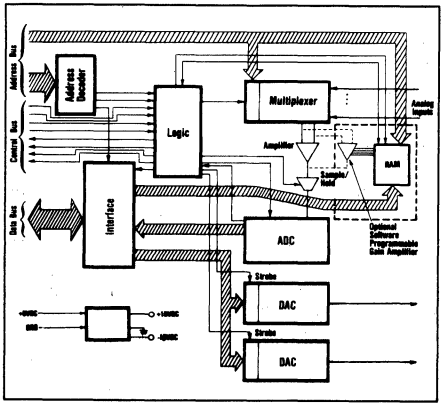
MP8418

MICROCOMPUTER ANALOG I/O SYSTEMS

A 31-CHANNEL ANALOG INPUT, 2-CHANNEL OUTPUT SYSTEM COMPATIBLE WITH INTEL SBC80, INTELLEC® MDS AND NATIONAL BLC-80 MICROCOMPUTERS

FEATURES

- HIGH AND LOW LEVEL INPUTS
- SOFTWARE PROGRAMMABLE GAIN (1 to 1024) AMPLIFIER OPTION
- ANALOG INPUT AND OUTPUT ON ONE BOARD
- EASILY PROGRAMMED
- MEMORY MAPPED
- LOW COST
- BURN-IN



DESCRIPTION

The MP8418 series of analog I/O peripherals are electrically and mechanically compatible with and interface directly to Intel's MULTIBUS® and other microcomputers of similar configuration. These analog systems are treated as memory by the CPU.

The analog input portion of the MP8418 includes: over-voltage protection to 26VDC; provision for up to eight 4mA to 20mA inputs; an analog multiplexer; resistor programmed instrument amplifier or, a software programmable amplifier (gain of 1 to 1024); sample/hold amplifier and; a 12-bit A/D converter. An optional analog output system is included on the same board. It consists of two 12-bit D/A converters with double buffered inputs to minimize glitches, and control logic.

MP8418 is a 15-channel differential (user strapable as 31 channel single-ended) analog input system. With one expander board the system can be expanded to 63 differential channels (strapable as 127 single-ended channels). Another input channel is grounded on the board so that it may be used as ground reference for automatic calibration.

Gains of 1 to 1024 are software selectable for the programmable amplifiers and the gain for each channel (up to 127 channels) may be stored in an on-board RAM if desired. The proper gain for each channel is then selected automatically by the MP8418.

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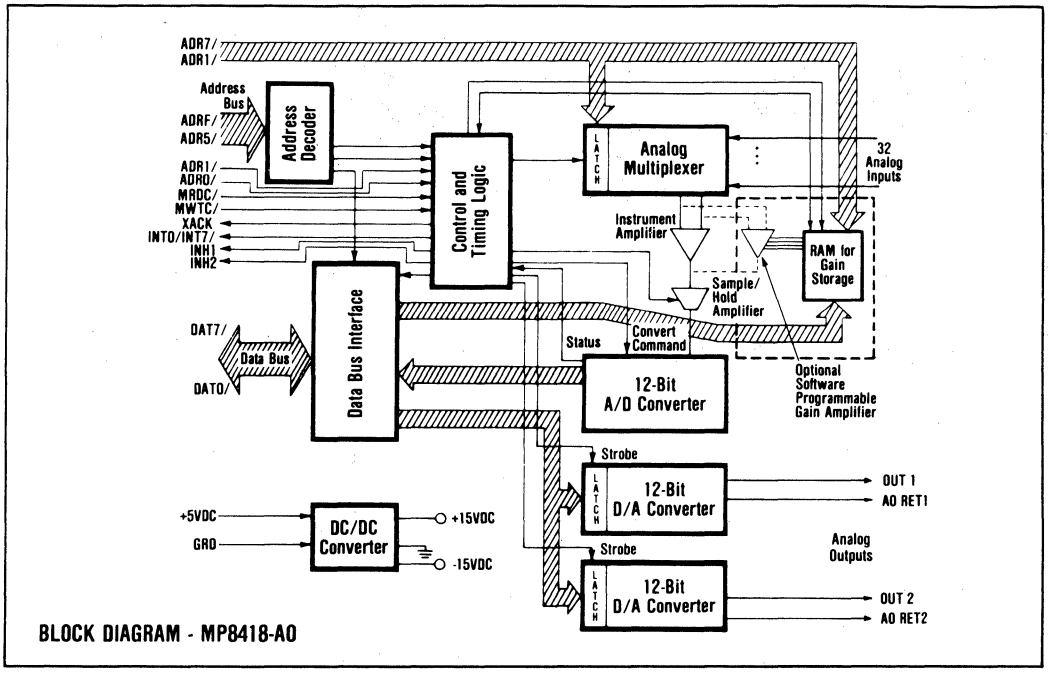

BLOCK DIAGRAM - MP8418-AO

MECHANICAL SPECIFICATIONS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 15.2mm (0.6").

Microcomputer bus connector required: 86-pin PC edge connector with 0.156" contact centers.

One 50-pin analog edge connector on board for analog inputs.
Mating connector available from Burr-Brown:
2250MC. (Viking #3VH25/1JN5, solder tab);
from 3M: 3415-0001 (Scotchflex).

Two 20-pin analog edge connectors on board for analog outputs and analog input expansion.
Mating connector available from Burr-Brown:
2220MC. (Viking #3VH10/1JN5).

OPERATING INSTRUCTIONS

INSTALLATION

MP8418 is shipped from the factory calibrated and ready to use. Installation requires only plugging the card into any empty slot in the computer and wiring the analog connector.

PROGRAMMING

This peripheral is programmed as a memory location and any memory reference instruction can be used. Both the A/D converter output and D/A converter input are 12-bit words, therefore, two memory locations are needed for each channel. The address block occupied by each MP8418 is user selectable and can be placed anywhere in memory.

Because these peripherals are treated as memory, a minimum of instructions are needed to read an input channel, or to set the input of a D/A converter. For example: when the MP8418 is connected in the HALT mode, the LHLD (load) instruction followed by the proper address can be used to read data from an analog input channel. It will automatically select the desired channel, initiate conversion and when conversion is complete, transfer the A/D converter output to the 8080's H and L registers. The eight least significant bits (LSB's) of the data word are transferred to the CPU first followed by the four most significant bits (MSB's). The four MSB's are in data bus positions 0 - 3. A single SHLD instruction can be used to write data to one analog output channel. The eight LSB's are written first, followed by the four MSB's (in D0-D3). When the four MSB's are written to the board, all twelve bits of the data word are transferred simultaneously to the D/A converter input.

ADC/DAC Bit Placement

	D7	D6	D5	D4	D3	D2	D1	D0
Low Byte	B_3	B_2	B_1	B_0	B_1	B_2	B_1	B_0
High Byte	X	X	X	X	B_{11}	B_{10}	B_9	B_8

On MP8418's, with the software programmable gain amplifier, an on-board random access memory (RAM) may be used to store the gain for each channel. In this

mode, (Control Register D4 = 1), the proper gain is automatically selected from the RAM when a channel is converted. If the RAM is not used (Control Register D4 = 0), the amplifier gain must be written to an on-board register (Control Register D0-D3).

All these systems are jumpered at the factory with a base address of $F700_{16}$. Each subsequent channel is two memory locations past the start of the last channel, consequently channel one is at location $F702_{16}$, channel two is at location $F704_{16}$, etc.

The input system operates in several modes:

INTERRUPT MODE: A read instruction to the board (ADR0 = 0) starts the conversion. An interrupt is generated at the end of the conversion. The interrupt can be connected to any of eight vector locations and may also be disabled by software. Control Register D6 = 1 enables interrupt for interrupt mode.

POLLING MODE: A read to the board starts the conversion. The interrupt is disabled by software and the CPU may then read the status word to determine when conversion is complete. Control Register D6 = 0 disables interrupt for polling mode.

HALT MODE: a read instruction to the board starts the conversion. The MP8418 halts the CPU until conversion is complete, at which point the data is transferred to the CPU. Only one instruction is needed to start conversion and to transfer data to the CPU (an LHLD or POP referenced to the channel's LSB's can be used).

CONTINUOUS MODE: A read instruction to the board starts the conversion. The CPU is not halted, but reads the status of the MP8418 to determine when conversion is complete (Control Register D6 = 0) - or the CPU waits for an interrupt (Control Register D6 = 1). When conversion is complete, the CPU reads the data. The read instruction is addressed to the next channel to be converted. The data from the last conversion is thus transferred to the CPU and conversion is started for the next channel.

EXTERNAL TRIGGER: This mode allows a conversion to be started independent of the CPU. A read instruction is required to set the proper channel. Once the board has been set, a low to high transition of the EXTERNAL TRIGGER input (P5, pin 20) will start conversion. End of conversion can be detected by polling or interrupt technique. Data is obtained by any read command. The external trigger will start conversion independent of other board functions. The busy input (P5, pin 19) goes high at the start of conversion and goes low when the MSB of the converted data is read by CPU.

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG INPUT SECTION	MP8418
INPUT CHARACTERISTICS	
Number of Channels	31 single-ended/15 differential
ADC Gain Ranges (Jumper Selectable)[1]	0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
Amplifier Gain Ranges	
Resistor Programmable[2]/Software Programmable	1 to 1000/1 to 1024
Maximum Input Voltage Without Damage[3]	±26 volts
Input Impedance	100MΩ, 10pF OFF Channel
	100MΩ, 100pF ON Channel
Bias Current (25°C)	±20nA
Bias Current (0 to 70°C)	±50nA
Differential Bias Current	±10nA
Amplifier Input Offset Voltage G = 1000	
Resistor Programmable/Software Programmable	±400μV/±4μV
Amplifier Input Offset Voltage Drift G = 1000	
Resistor Programmable/Software Programmable	±2μV/°C/±1μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Throughput Time (max) G = 1	
Resistor Programmable/Software Programmable	38μsec/350μsec
Throughput Time G = 1024	
Resistor Programmable/Software Programmable	100μsec/350μsec
ACCURACY	
System Accuracy at +25°C (max)[4] G = 1	±0.0325% FSR[5]
System Accuracy at +25°C[4] G = 1024	
Resistor Programmable/Software Programmable	±0.1% FSR/±0.05% FSR (max)
Linearity	±1/2LSB
Differential Linearity	±1/2LSB
Quantizing Error	±1/2LSB
Gain Error	Adjustable to Zero[6]
Offset Error	Adjustable to Zero
Monotonicity[7]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE (Bipolar)[8]	
System Accuracy Drift (max) G = 1	±45ppm of FSR/°C
System Accuracy Drift G = 1024	±100ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	125nsec
Aperture Time Uncertainty	±5nsec
Differential Amplifier CMRR G = 1	86dB (DC to 60Hz)
Channel Crosstalk	80dB down at 1kHz, for OFF Channel to ON Channel
ANALOG OUTPUT SECTION (AO option)	
OUTPUT CHARACTERISTICS	
Number of Channels	2
Output Voltage Ranges (Strap Selectable)	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA
Output Impedance	1Ω
Short Circuit Protection	Yes
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Output Settling Time (max)	10μsec
ACCURACY	
Output Accuracy	±0.0125% FSR
Temperature Coefficient of Accuracy	±30ppm of FSR/°C
POWER REQUIREMENTS	
MP8418/MP8418-PGA	+5V ±5% at 1.2A
MP8418-AO/MP8418-PGA-AO	+5V ±5% at 2.0A
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Relative Humidity	95% noncondensing

NOTES:
1. Factory set for ±10V range.
2. Factory set for Gain = 1.
3. With power off. ±36 volts with power on.
4. Includes linearity errors with gain and offset errors adjusted to zero.
5. FSR means Full Scale Range.
6. When any one gain range is adjusted to zero gain error, the gain error for any other range is less than ±0.02% when using the software programmable amplifier.
7. No missing codes guaranteed.
8. Includes offset drift, gain drift and linearity drift.

FACTORY MODE CONNECTIONS	
MODEL	FACTORY SET MODE
MP8418	HALT
MP8418-AO	HALT
MP8418-PGA	POLLING INTERRUPT*
MP8418-PGA-AO	POLLING INTERRUPT*

Note: Any model can be connected in any mode.
*Int 1 Factory Set

TABLE I. Programming Mode Connections.

JUMPER REQUIRED	
Halt Mode	JP17, JP29, JP30, JP81
Polling and Interrupt Mode	JP17, JP29, JP81
Continuous Mode	JP17, JP31, JP82
External Trigger Mode	JP16, JP29, JP81

TABLE II. Mode Selection Jumpers.

JUMPERS REQUIRED FOR INTERRUPT VECTOR	
INT0/	JP70
INT1/	JP71
INT2/	JP72
INT3/	JP73
INT4/	JP74
INT5	JP75
INT6/	JP76
INT7/	JP77

TABLE III. Interrupt Selection.

MEMORY MAP

Factory Set	ADR7 ... ADR0		READ		WRITE	
F700	0000 0000	CH0	8LSB's of offset		N/A	GAIN 0*
F701	0000 0001	IN	STATUS		CONTROL	
F702	0000 0010	CH1	LSB		N/A	GAIN 1*
F703	0000 0011	IN	MSB		N/A	
F704	0000 0100	CH2	LSB	CH0 OUT	LSB	GAIN 2*
F705	0000 0101	IN	MSB	or GAIN	MSB	
F706	0000 0110	CH3	LSB	CH1 OUT	LSB	GAIN 3*
F707	0000 0111	IN	MSB	or GAIN	MSB	
F708	0000 1000	CH4	LSB		N/A	GAIN 4*
F709	0000 1001	IN	MSB		N/A	
			⋮		⋮	
F71E	0001 1110	CH15	LSB		N/A	GAIN 15*
F71F	0001 1111	IN	MSB		N/A	
F710	0001 0000	CH16	LSB		N/A	GAIN 16*
F711	0001 0001	IN	MSB		N/A	
			⋮		⋮	

N/A - Not used.

*Used only on PGA versions when RAM gain storage is used.

A read instruction (other than a STATUS REGISTER read) should not be made to the board during a conversion. Contact factory for more details.

STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
Convert Complete	Interrupt Enable	Write* Enable	RAM* Enable	--------	GAIN X*	----------	

*Used only on versions with software programmable amplifier.

Convert Complete - The bit is low during conversion. It goes high on completion of conversion and remains high until the MSB of a data word is read.

Interrupt enable: status of interrupt enable
Write enable: status of write enable
RAM enable: status of RAM enable
GAIN X: current value stored in PGA GAIN control register.

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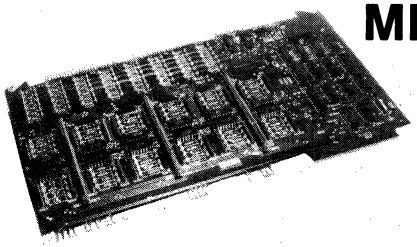


MP8418-EXP

MICROCOMPUTER ANALOG INPUT EXPANDER FOR MP8418

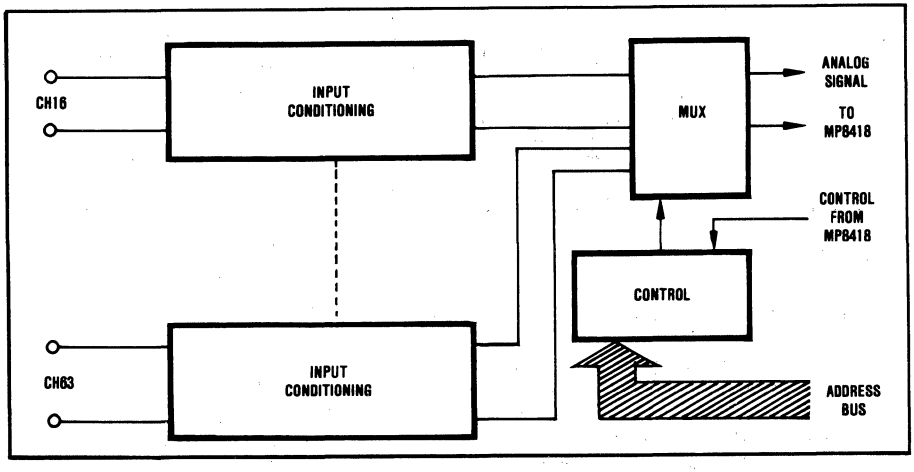
FEATURES

- 48 DIFFERENTIAL CHANNELS/ 96 SINGLE-ENDED CHANNELS
- SOLID STATE MULTIPLEXING
- 26V OVERVOLTAGE PROTECTION WITH DIODE CLAMPS
- MULTIBUS™ COMPATIBLE

Multibus™ - Intel Corp.

DESCRIPTION

MP8418-EXP is a bank of multiplexers that expand the analog input channel capacity of the MP8418 series microperipheral. Differential input capability is expanded from 15 channels to 63 channels. Single-ended capability is expanded from 31 channels to 127 channels. Control signals and power are passed to the expander from the MP8418. The analog input signal is passed to the MP8418 from the expander. Multiplexer channel addresses are latched on the expander board. The expander occupies the memory space immediately above the MP8418. Gain, data conversion, and bus interface are performed by the MP8418. Channel gains can be stored in a RAM on the PGA versions.



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PDS-436

SPECIFICATIONS

ELECTRICAL

Inputs	48 differential 96 single-ended
Input Protection	26V
Power +5V +15V -15V	110mA (from system bus) 30mA (from MP8418) 20mA (from MP8418)

See MP8418 Specifications for all other input characteristics.

MECHANICAL

Compatible with Intellec MDS and iSBC-604/614 card spacing.
Minimum card spacing: 15.2mm (0.6").
Microcomputer bus connector required: 86-pin PC edge connector with 0.156" contact centers.
Two 50-pin analog edge connectors on board for analog inputs.
Mating connectors:
Burr-Brown 2250MC (Viking #VH25/1JN5), solder tab;
3M Corporation: 3415-0001 (Scotchflex).
Interface Cable: 20-conductor ribbon cable with a card edge connector mass terminated on each end, available from Burr-Brown:
MP8005, 1" long
SM50123-001, 9.5" long

INTERFACE CONNECTOR

Bottom	P5		Top
+15VDC	1	2	+15VDC
Analog GND	3	4	Analog GND
-15VDC	5	6	-15VDC
Dig GND	7	8	Addr. Out
Dig GND	9	10	EXP/
Dig GND	11	12	Dig GND
Analog GND	13	14	Analog GND
Analog GND	15	16	Analog GND
Analog GND	17	18	IA IN-
Analog GND	19	20	IA IN+

INSTALLATION

If possible, adjacent slots in the system should be used for the MP8418 and MP8418-EXP. This is particularly important for low level operation where longer cables introduce noise and offset errors. Analog inputs connect to P3 and P4. Connector P5 on the MP8418-EXP connects to P4 on the MP8418 to interface the two units (see Figure 1). Tables I and II show jumper configurations for the expander and additional jumper changes required on the MP8418.

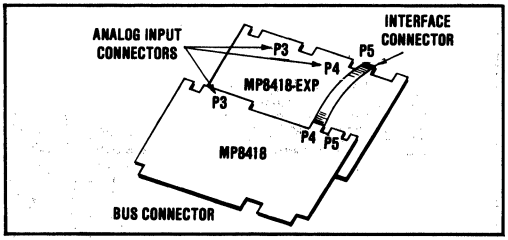

FIGURE 1. System Interface.

TABLE I. Jumper Requirements for Differential Operation.

	MP8418	MP8418-EXP
Install	JP44, 45 JP33, 36 JP66, 67, JP3, 4, 7	JP2 JP3
Remove	JP42, 39 JP2, 5	JP1

TABLE II. Jumper Requirements for Single-ended Operation.

	MP8418	MP8418-EXP
Install	JP44 JP33, 37 JP66, 67, 68 JP2, 5	JP1
Remove	JP39, 42, 43, 36, 45 JP3, 4, 7	JP2 JP3

INPUT NETWORK

The input network is shown in Figure 2. The switch shown represents two CMOS multiplexers in series. Input protection is provided by the series resistors and diode clamps. The clamps prevent the multiplexer inputs from exceeding the supply voltages. An optional resistor (R) allows the user to convert current inputs to voltage that can be detected by the MP8418. The optional capacitor (C) in combination with the input resistors form a low-pass filter. Low-leakage high-quality capacitors should be used to minimize errors. The optional resistor and capacitor are only useful for differential operation.

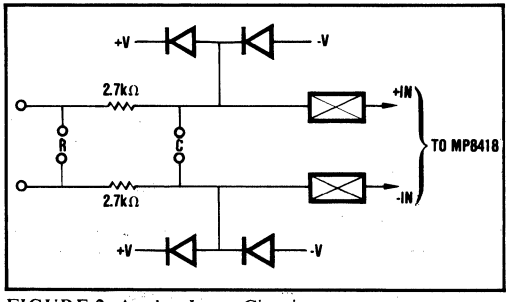

FIGURE 2. Analog Input Circuit.

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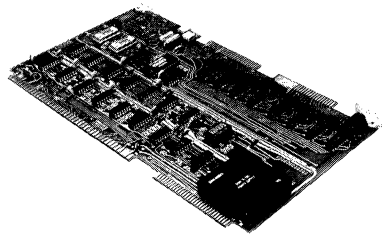
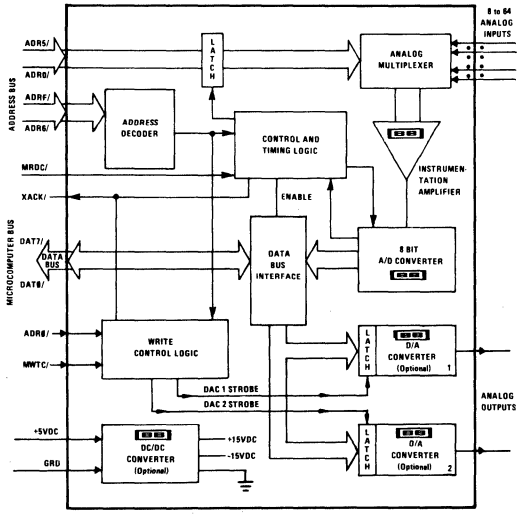


MP8608
MP8616
MP8632

MICROCOMPUTER ANALOG I/O SYSTEMS

FEATURES

- INTEL-SBC80 and INTELLEC MDS COMPATIBLE
- NATIONAL-BLC80 COMPATIBLE
- LOW COST
- 70°C BURN-IN
- EASY TO PROGRAM
  Systems are treated as memory
- REDUCES SYSTEM DEVELOPMENT TIME
  System engineered and specified
  Operates from computer's +5VDC
  power supply if desired
- EASY TO USE
  8 to 64 input channels on one board
  Analog input and output on one board



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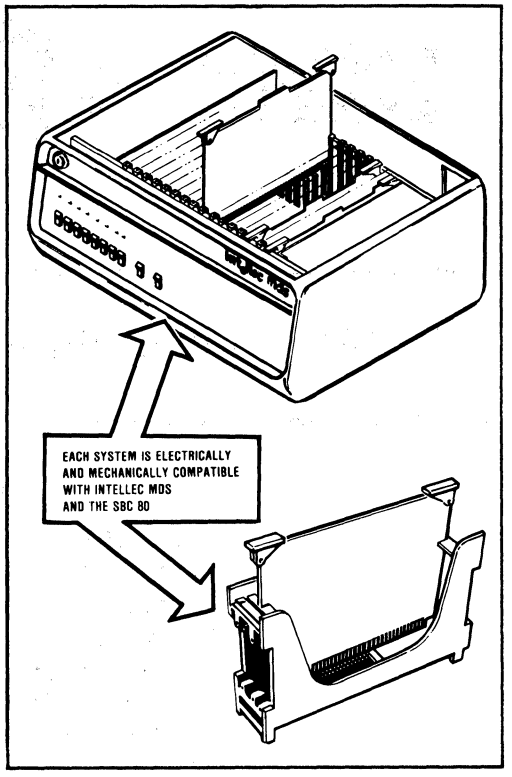
DESCRIPTION

These microcomputer peripherals provide two functions that interface directly to Intel's SBC80 and Intellec MDS microcomputers. The functions are: (1) Analog Data Acquisition and (2) Analog Output. The devices are electrically and mechanically compatible with any SBC80 and Intellec MDS. Both analog input and output systems are contained on a single printed circuit board that is treated as memory input or output by the CPU. The cards will mate to any memory or I/O slot. They are compatible with the 0.6" spacing of the SBC80 or the 0.75" spacing of the Intellec MDS. The analog interface for each system is a connector at the opposite edge of the board from the bus connector.

The Data Acquisition system is available with up to 64 channels single-ended on one board. It includes an input multiplexer, high gain instrumentation amplifier, 8-bit A/D converter along with all the necessary timing, decoding and control logic. A DC/DC converter (+5V to ±15V) is also available so that only the computer's power supply is required. The Data Acquisition System is available with two optional 8-bit D/A converters to provide analog input and output on the same board.



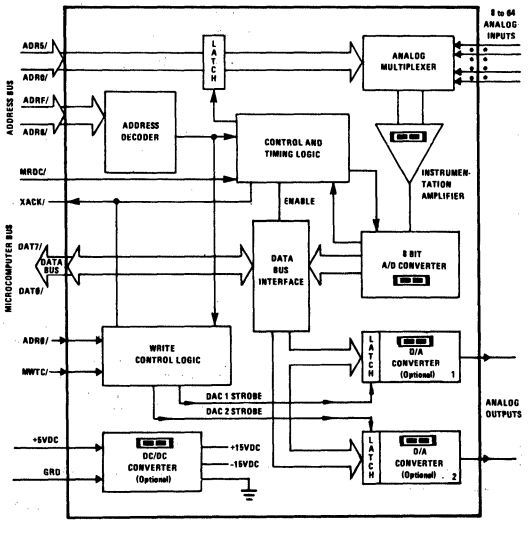
THEORY OF OPERATION

When programming with these peripherals, they are treated as memory locations. Any memory reference instruction can be used. Both the A/D converter output and the D/A converter input are 8-bit words so one memory location is needed for each channel. Because the address block occupied by each peripheral is user selectable, it can be placed anywhere in memory.

Because these units are treated as memory, a minimum of instructions are needed to read an input channel or to set the input of a D/A converter. For instance, the LHLD (load) instruction followed by the proper address can be used to read data from two successive analog input channels. It will automatically select the desired channel, initiate conversion and when conversion is complete, transfer the A/D converter output for the first channel to the 8080's L register and the second channel to the H register. Likewise a single LDA instruction can be used to read one analog input channel.

All of these systems are jumpered at the factory with the first channel at address $F700_{16}$. Each subsequent channel is one memory location past the start of the last channel so that the second channel is at location $F701_{16}$.

ANALOG INPUT/ OUTPUT SYSTEM



SPECIFICATIONS

All specifications typical at 25°C unless otherwise noted.

ANALOG INPUT/OUTPUT SYSTEM	
ANALOG INPUT	
Number of analog inputs	
8 differential	MP8608
16 single-ended	MP8616
32 differential or 64 single-ended [5]	MP8632
Input voltage range[1]	±10mV to ±5V
ADC gain ranges[1]	±10V, 0 to 10V, 0 to 5V
(strap selectable)	±5V, ±2.5V
Amplifier gain range[1]	1 to 1000 V/V
(resistor programmable)	
Amplifier gain equation	$G = 100k\Omega / R_{EXT}$
Input overvoltage protection	±15V
Input impedance	100 megohms
Bias current	
25°C (max)	+300nA
0°C to 70°C	-2nA °C
Amplifier input offset voltage	±2mV
Amplifier input offset voltage drift	$\pm(5 + \frac{1000}{G})$ μV/°C
ANALOG INPUT TRANSFER CHARACTERISTICS	
Resolution	8 bit binary
Throughput accuracy ±5V range (max)	±0.4% FSR[2]
±10mV range	±0.5% FSR
Temperature coefficient of accuracy	
±5V range (max)	±0.02% FSR/°C
±10mV range	±0.07% FSR/°C
Conversion time ±5V range	44 microseconds
±10mV range	84 microseconds
CMRR (for differential inputs)[3]	66 dB (Gain = 2)
	86 dB (Gain = 100)
ANALOG OUTPUT	
Number of analog outputs	2
Output voltage range[4]	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V
	at 5mA (strap selectable)
Output impedance	1Ω
Output settling time (max)	< 5 microseconds
ANALOG OUTPUT TRANSFER CHARACTERISTICS	
Resolution	8 bits binary
Throughput accuracy (max)	±0.4% FSR
Temperature coefficient of accuracy	
Unipolar	±0.005% FSR/°C
Bipolar	±0.01% FSR/°C
DIGITAL INPUT/OUTPUT	
All signals are compatible with Microcomputer Bus	
Output coding	Bipolar, two's complement; Unipolar, straight binary
An analog input channel is selected by:	ADR0/ through ADR5/
An analog output channel is selected by:	ADR0/
The input/output data bits are read through:	DAT0/ through DAT7/
POWER REQUIREMENTS	
MP8608, MP8616, MP8632,	+5VDC ±5% at 1 amp, 25mV ripple
With analog output	
MP8608-AO, MP8616-AO, MP8632-AO	+5VDC ±5% at 2 amp, 25mV ripple
TEMPERATURE RANGE	
	0°C to 70°C

(1) Connected at the factory for ±5V range (ADC range = ±10V, Gain = 2).
(2) FSR is Full Scale Range (i.e., 10V for ±5V range).
(3) DC to 60Hz with 1kΩ source unbalance.
(4) Connected at the factory for ±10V range.
(5) Connected at the factory as 32 differential.

OPERATING INSTRUCTIONS

PROGRAMMING

Programming of this analog I/O board is easily accomplished since all channels are treated as memory locations. Any memory reference instruction can be used. A single STA instruction may be used to load the accumulator contents to one of the D/A converters. Likewise a single LDA instruction can be used to read an analog input channel.

Single instructions can also be used to set the inputs of both D/A converters and read two adjacent analog input channels. An SHLD instruction referenced to DAC 1 will load the contents of the L register into DAC 1 and the contents of the H register into DAC 2. An LHLD instruction will read the channel addressed and the next higher channel. The channel addressed will be transferred to the L register and the next higher channel to the H register. Of course, any MOV instruction may also be used if direct addressing is not desired.

The normal operation of this board halts the CPU during the conversion time of the analog input system. This is because the software in this mode is simpler than in any other (i.e., only one instruction required!). If the halt feature is not desirable, it may be disabled.

For operation without halting the CPU, the conversion should be started by using a single channel memory reference instruction (LDA or MOV). Then the CPU should execute a routine which will take longer than the conversion time (44 to 84 microseconds). When the CPU now uses an LDA or MOV referenced to the same memory location, the converted data will be transferred to the CPU.

The voltage data for these boards is represented by an 8-bit two's complement binary number. With a ±5V range, each bit has a value of 39.1mV, with the polarity of the voltage indicated by the sign of the binary number.

Each board is set at the factory for a block of addresses beginning at F700. Any analog data channel requires one memory location. Thus the first analog channel is located at F700 while the second analog channel is located at F701.

MECHANICAL CHARACTERISTICS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 12.7mm (0.5").

Microcomputer bus connector required: 86 pin PC edge connector with 0.156" contact centers.

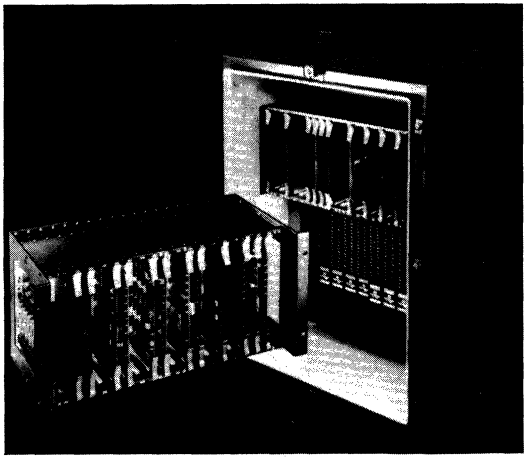
50 pin analog edge connector on board.

Mating connector available from Burr-Brown: 2250MC (Viking # 3VH25/1JN5, solder tab); from 3M: 3415-0001 (Scotchflex).

INDUSTRIAL SYSTEMS PRODUCTS

IOS2000

A Complete I/O System That Makes I/O Handling Easy...Reduces Control System Costs



Using its preprogrammed microprocessor, IOS2000 can be the sensory center of your control system. Fully expandable, transparent to CPU and operator, IOS2000 reduces system design/installation costs - is burdenless to your CPU/software.

Remotely located, this intelligent front-end collects and conditions sensor inputs - sends them to your CPU already digitized and preprocessed. Operating in a closed loop, IOS2000 responds to CPU commands - generates contact closure outputs to turn on lights, motors...generates analog output voltages and currents to modulate valves, establish set points, etc.

Routine sensor signal conditioning and intelligent internal housekeeping programs automatically occur every time an operator communicates with IOS2000.

Up to 15 clustered IOS2000 systems can be connected to one ASCII serial communications line. As a result, up to 10,000 I/O's can be handled. Use IOS2000 as extended front ends in stand-alone applications using programmable terminals or CPU's. Plug-in modules let you add sensors, outputs, more power in the field as demand grows. Rack mounted card cages, remote termination panels, NEMA-4 enclosures plus I/O options let you match IOS2000 exactly to your needs.

CS450

A Stand-Alone Measurement and Control System That's Easy To Install, Program, Operate

Spell out your process, control, measurement or test steps in logical operational sequence using our BASIC-400 that speaks your language. Use preprogrammed keyboard "Function" keys to simplify commands for untrained operators.

Your program, once written into CS450's memory, is transferred to disk and or cassette tape storage where it becomes a permanent program that can be re-run as you wish. AUTOSTART automatically reloads your stored program into CS450's operating memory. The operator does not load the program and, in fact, CS450 can start up and control processes without operator involvement.

Mass storage, printer, alarm, process I/O, AUTOSTART, real time clock and calendar are built into a compact table top or rack mount package. CRT is an option. Up to seven analog, digital and discrete I/O boards plug into CS450's Multibus™ compatible card cage. Connect sensor inputs control outputs and you're ready to run!

CS430: rugged, lower cost...uses dual minicassette tape drives rather than dual disk drives which are standard on CS450. All other functions are identical.

Multibus™ - Intel Corp.

11

MCS100
DATA ACQUISITION SYSTEM

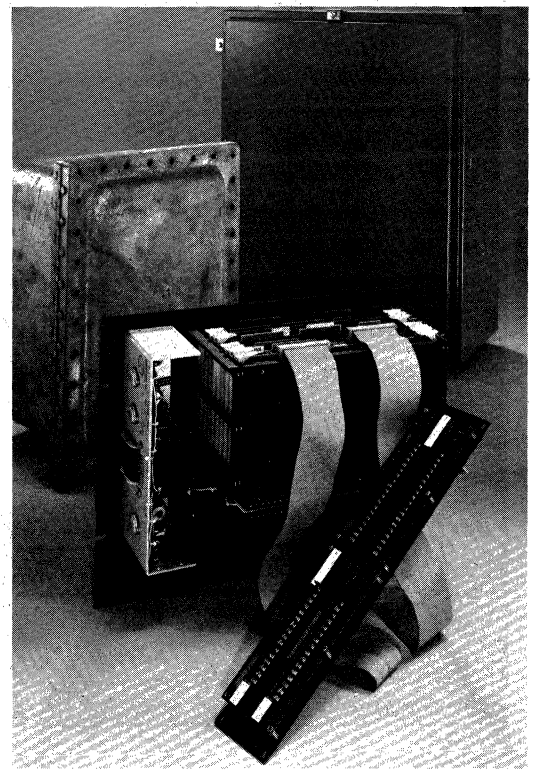
Truly Cost Effective Analog and Digital I/O

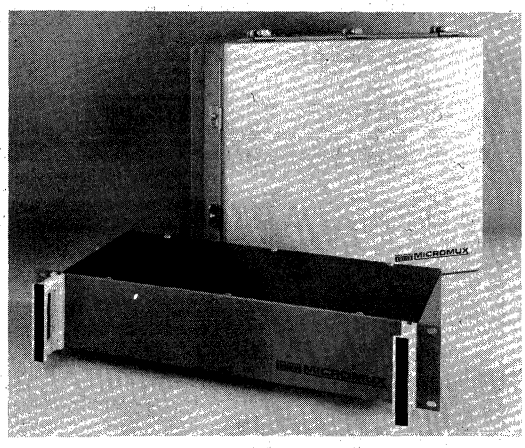
Now remote I/O is a practical option because MCS100 significantly reduces the total design, installation and operating costs of data acquisition and control systems. Because of its modular design - and Multibus™ capability - you can purchase a system configured for today's needs, but be assured that you can expand it later with minimum problems and cost.

This versatile system eliminates most signal conditioning while maintaining data accuracy over industrial temperature ranges of 0 to +50°C. It offers both analog and digital inputs and outputs incorporating Burr-Brown's full range of I/O functions. Up to nine of these Multibus™ compatible I/O cards can be placed in each card cage. Memory-mapped I/O addressing simplifies programming. Open card cage and rack mount chassis, plus NEMA and explosion-proof enclosures options, add installation flexibility to MCS100.

Up to 16,320 inputs/outputs can be handled when 15 MCS100's are multidropped on one serial communications line. CPU operator involvement as well as maintenance procedures are sharply reduced. Costly fragile calibration equipment is not required.

Multibus™ - Intel Corp.





MICROMUX

A Two-Wire System That Takes The Cost... Complication Out of Remote Data Acquisition

Locate a MICROMUX Remote Transmitter near monitoring points, input up to 16 analog or digital signals: thermocouples, voltage and current signals, discrete voltage. Inputs are converted to multiplexed digital signals which are transmitted, not by 32 wires, but by a single-wire pair to the receiver.

Locate the MICROMUX Receiver near your CPU. It receives signals from up to four remote transmitters, converts them to three-digit BCD format. This continuously updated information is stored in the receiver's memory.

Rugged transmitters - designed for heavy industrial applications - are housed in environmentally sealed steel enclosures. Use of approved safety barriers makes the unit "intrinsically safe".

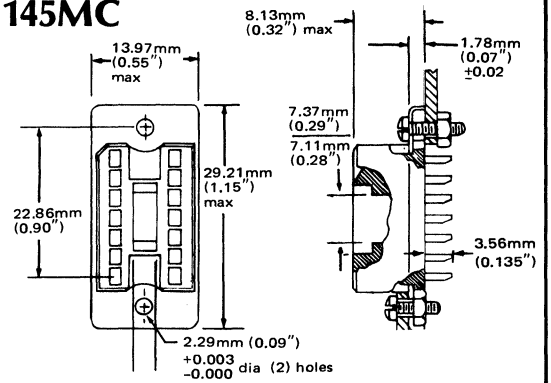
Sending digitally encoded data through high noise interference areas protects its accuracy. An ASCII compatible, 20mA current loop (2400 baud) serial interface is standard. RS232C with 110-2400 baud is an **option. Up to 8 MICROMUX Receivers (handling up to 512 channels** of sensor inputs) can be connected to a single serial communications port on your CPU. Programming is similar to that used for most ASCII peripherals.

ACCESSORIES

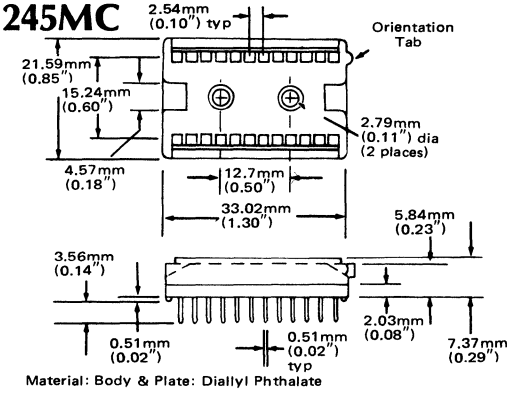
This section contains illustrations and information on the mating connectors and heat sinks available for use with various Burr-Brown products. The type of connector and/or heat sink required by the product is specified within the product data sheet. Prices are available from your nearest Burr-Brown representative.

MATING CONNECTORS

145MC

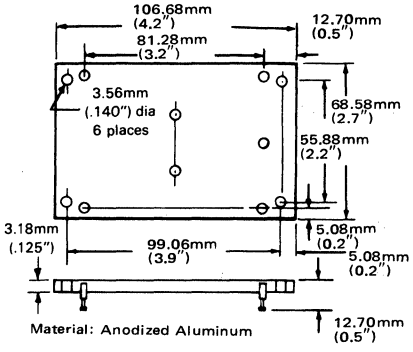


245MC



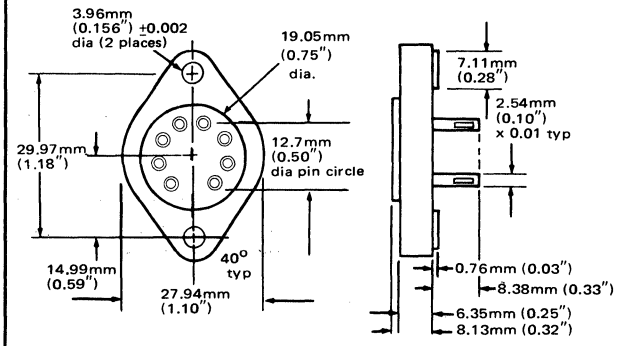
Material: Body & Plate: Diallyl Phthalate

548MC

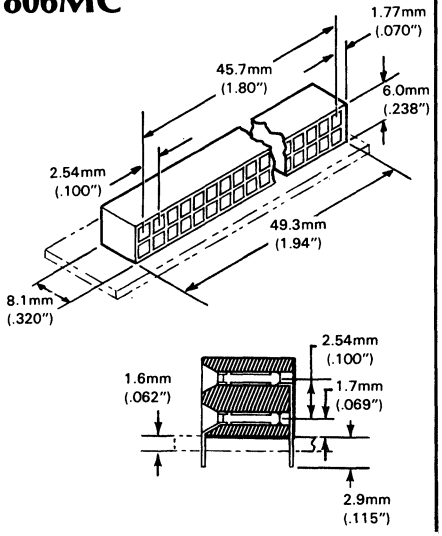


Material: Anodized Aluminum

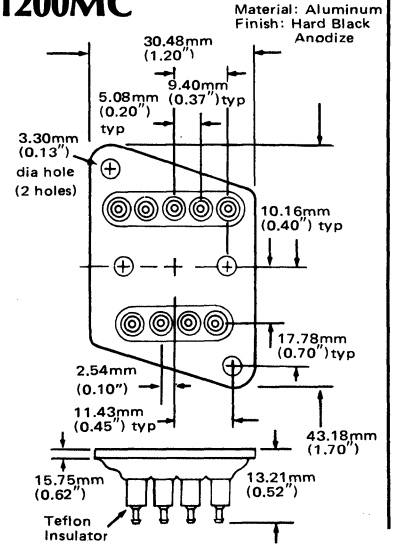
803MC



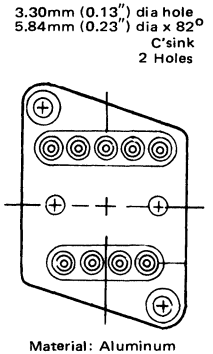
806MC



1200MC



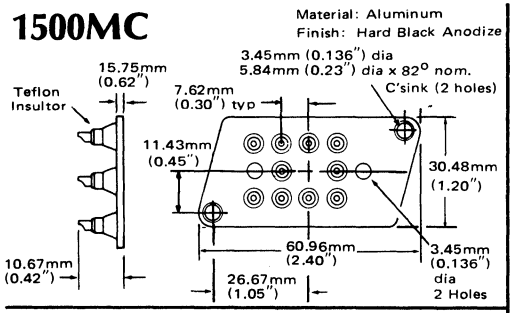
1400MC*



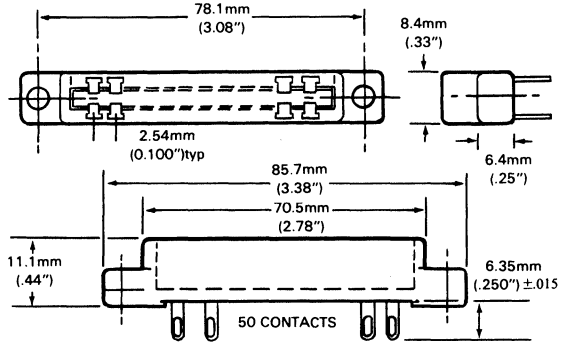
Material: Aluminum
Finish: Hard Black Anodize

* Identical to 1200MC except for mounting holes.

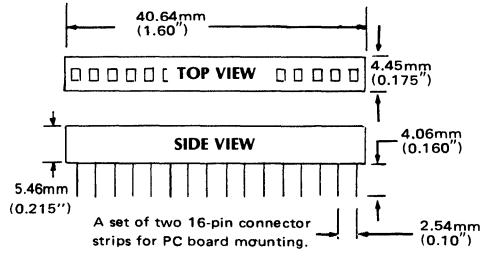
1500MC



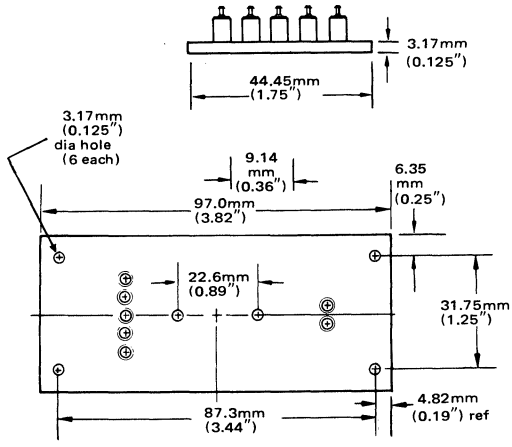
2250MC



2302MC



2800MC

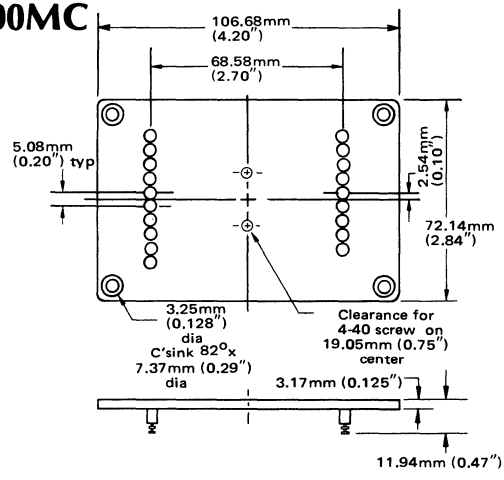


2401MC

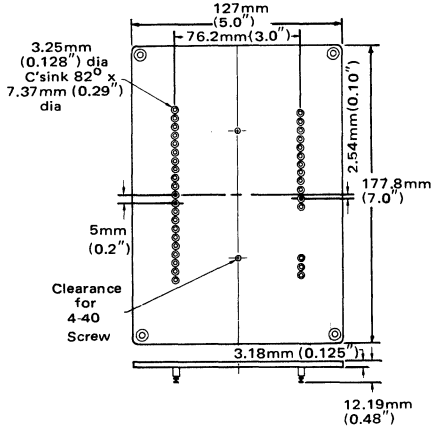
Identical to 2302MC except each connector strip length is 45.72mm (1.80")

A set of four 18-pin connector strips for PC board mounting.

4400MC



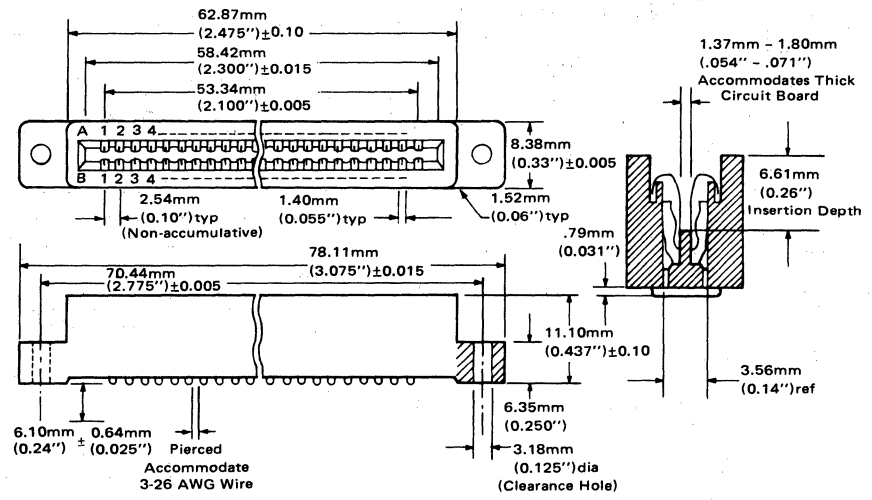
4800MC



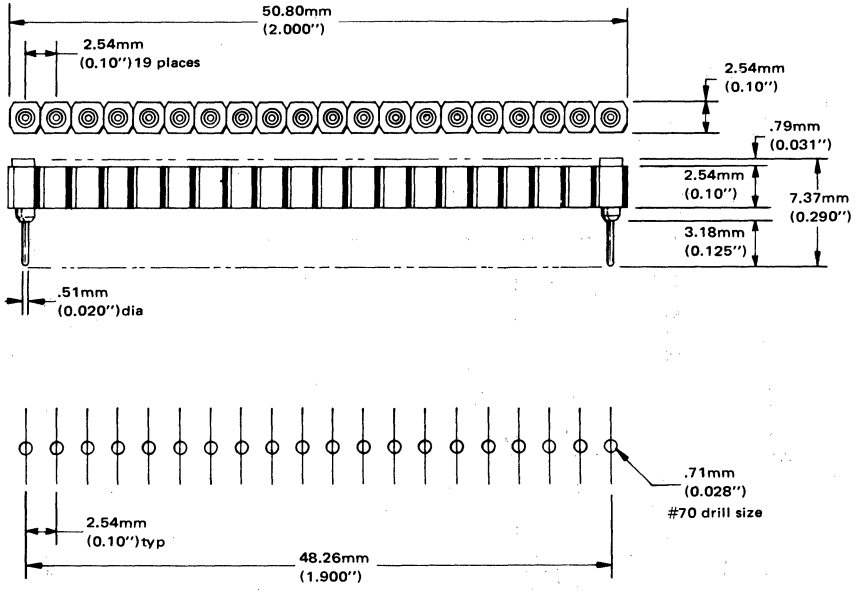
ACCESS.

MATING CONNECTORS

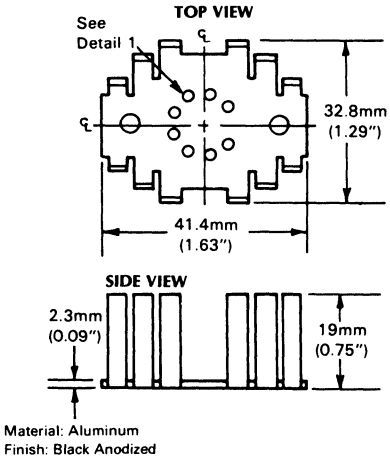
2201MC



2350MC

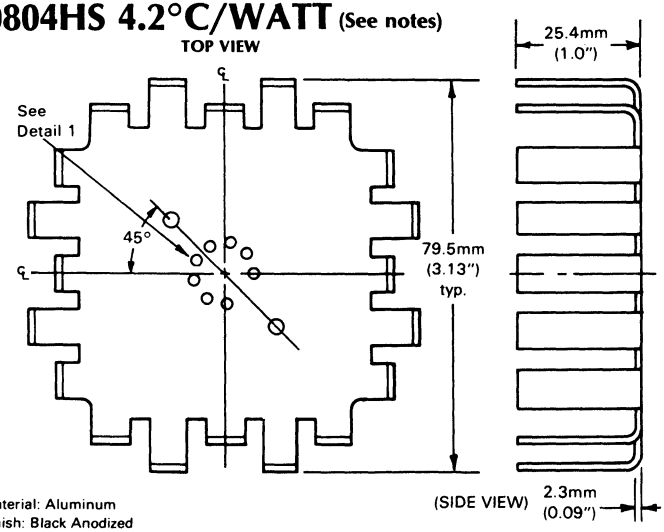


0803HS 12°C/WATT
(See notes)



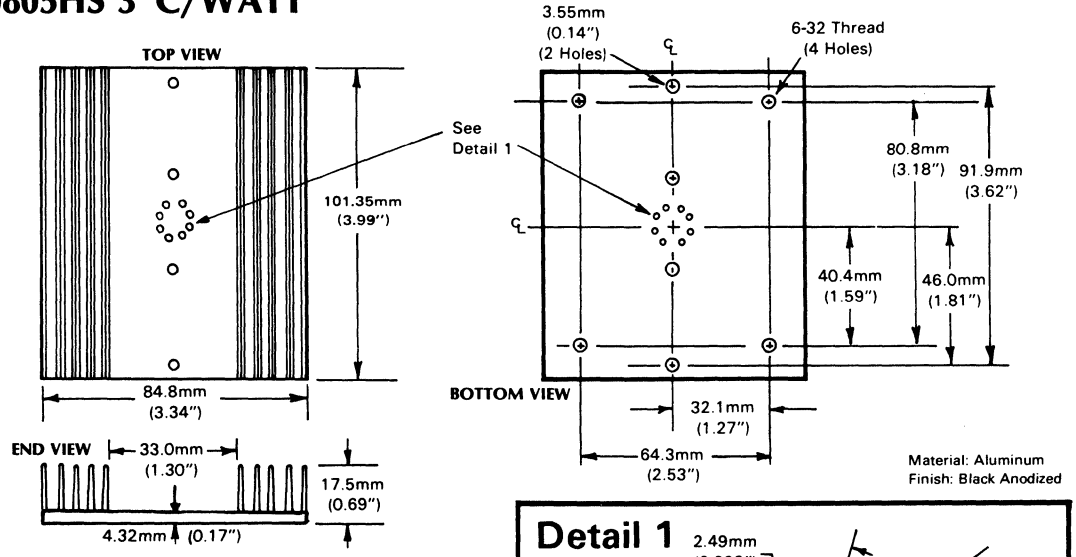
Material: Aluminum
Finish: Black Anodized

0804HS 4.2°C/WATT (See notes)



Material: Aluminum
Finish: Black Anodized

0805HS 3°C/WATT

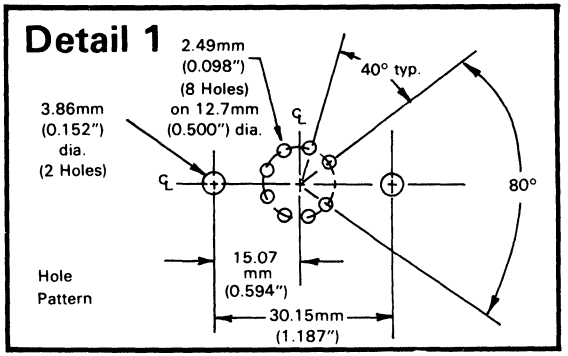


Material: Aluminum
Finish: Black Anodized

*NOTES

1. Thermal resistance specified are for natural connection. Heatsinks 0803HS and 0804HS are mounted on 6" x 6" x 1/16" G-10 PC board.
2. A thin-film of heatsink compound(Dow Corning 340 or equivalent) between the heatsink and the TO-3 device is recommended.

Detail 1



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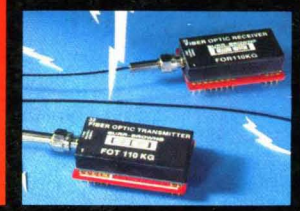
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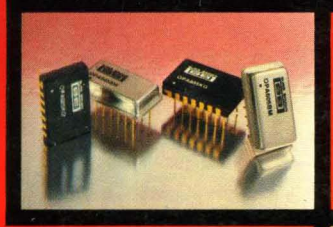
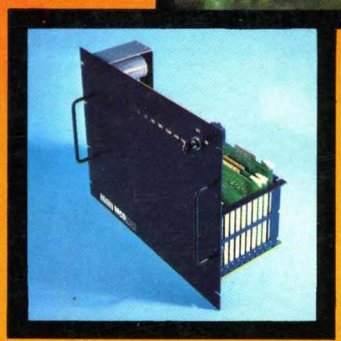
FOR110KG
FIBER OPTIC TRANSMITTER
FOT 110 KG






CS450